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# ETI CIRCUITS BOOK: No. 2

## IDEAS AND DATA FOR EXPERIMENTERS FULL CONTENTS OVERLEAF

EDITED BY JIM PERRY

PUBLISHED MARCH 1978

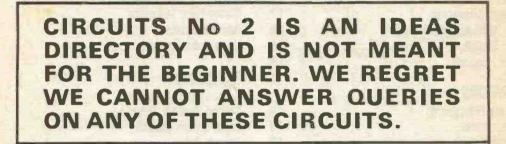
For a long time we have published a section in Electronics Today International specifically for the experimenter-Tech Tips. This has always been one of the most popular sections of the magazine, due mainly to the tremendous variety of circuits that find their way into it.

But by the very nature of being a monthly feature, it becomes impossible (without some form of filing system) to remember particular circuits — or compare them with similar ones.

Our answer to this problem is this series of Circuits Books, this issue includes an enlarged data section and uses other sources besides Tech Tips — to produce an invaluable experimental source book. (We never were modest at ETI!).

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ALARMS **Comprehensive Burgiar Alarm** SCR Alarms **Car Radio Protector** Fire Alarm, Simple

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### POWER SUPPLIES

Current Source. Drift Free	
Constant Current, High Voltage	
Output Voltage, Adjustment	
High Voltage, Variable Regulator	
Switched Output	
Dual PSU	
Mobile Power Supply	
Converting Single to Dual	
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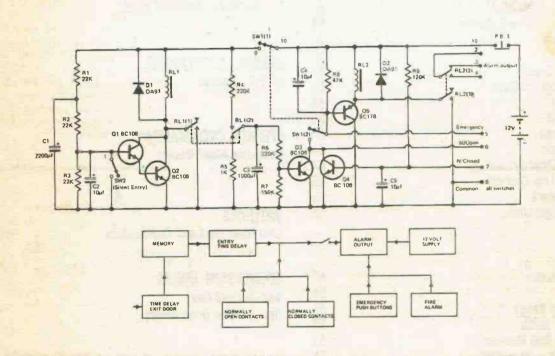
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### **Comprehensive Burglar Alarm**

Examination of the block diagram will show the overall operation of this alarm circuit. SWI is the main on/off switch and should be key operated. PBI is the reset control, and should be either hidden or wired in parallel with a third set of contacts on SWI — this is to prevent the alarm being disabled without a key.

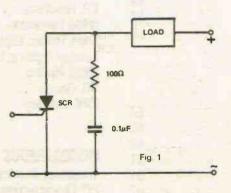
SW1 is a normally closed contact on the exit door. When leaving the delay section disables RL1 for about 2 minutes and also on entry. If this exit is used and the alarm is not siwtched off before the 2 minutes are up — the alarm will sound.

The rest of the circuitry is quite straightforward. Q3 and Q4 are used to ground the base of Q5 if an alarm condition exists. Q5 operates RL2 which is used to sound a bell or siren externally.



#### SCR Alarms

In some SCR circuits the SCR will tend to 'switch on' the moment the dc supply voltage is applied, at the SCR's gate. This is because the SCR is sensitive to the rate at which the supply voltage is applied, and if this rate of rise exceeds a certain level, switch-on will occur. The effect may be eliminated by connecting a series resistor/capacitor combination across the SCR. This is known as dv/dt suppression and its effect is to slow down the rate of voltage rise. A diode, connected in the same effective polarity as the SCR, may be paralleled across the resistor for maximum effectiveness. In most applications the values shown in Fig. 1 will prove effective.

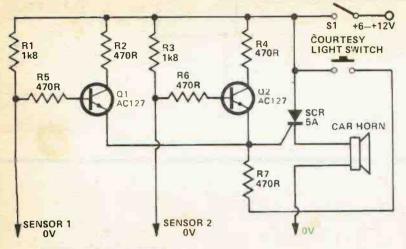


False triggering can also be caused by transients induced into the gate circuits. This is a very common problem with a number of burglar alarms — even commercially made ones from manufacturers who should know better. The most commonly used SCR burglar alarm circuit is basically that shown in Fig. 2. In this configuration, the gate of the SCR is connected to the positive rail via a 10k resistor, but an external loop interconnecting a number of normally closed trip switches, effectively clamps the gate at zero potential. However if any switch is opened, or if the external loop is cut, the SCR will immediately be triggered into conduction, thus energizing a series connected bell.

The problem with this circuit is that although the gate of the SCR appears to be held very firmly at zero potential by the external loop, transient energy induced into the external loop by electro-magnetic phenomena (caused by lightning, arc welders, fluorescent lighting starters etc) can reach quite

#### **Car Radio Protector**

Many circuits have appeared for protecting radios and stereos in softtop motor cars whose interiors are readily accessible to thieves. These circuits however, have the disadvantages of high parts count and expensive relays to switch on and latch the alarm. The circuit operates as follows: sensor leads 1 and 2 are connected to the chassis of the equipment to be protected, therefore holding the bases of Q1 and Q2 at earth potential and thus switched off. If one of the sensor leads is broken, current flows to the base of the respective transistor and switches it on. This gates the SCR and



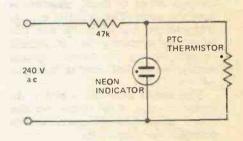
sounds the alarm. The self-latching characteristics of the SCR now make the transistor and its sensor lead inoperative and the alarm can only be stopped by switching off the concealed switch, S1.

To prevent thieves tampering with the wiring, a seperate car horn and courtesy light switch (obtained from a breaker's yard) were fitted under the bonnet. If thieves cut the normal horn wires the alarm is unaffected; also any attempt to lift the bonnet to disconnect the battery will trigger it. The sensor leads are multistrand flexible cable with only one strand connected to the equipment, therefore easily broken while trying to remove it from the dashboard.

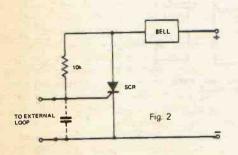
The transistors used are not critical and most NPN. general purpose transistors should suffice. The stand-by current is very low (typ. 13mA), and therefore is designed to be left switched on. The owner can never forget to switch on the alarm when leaving the vehicle. He must, however, switch off before lifting the bonnet.

### Fire Alarm, Simple

A voltage divider made up of a resistor and positive temperature co-efficient thermistor has its incremental voltage fed to a neon indicator lamp. The thermistor is used as the temperature sensor. Its value is such that under normal ambient conditions the neon voltage across it is. below striking voltage for the neon. If a fire causes the thermistor to heat up, its resistance rises, and the neon ignites giving a visual alarm. The value of the PTC thermistor is selected to give the necessary resistance change to ignite the particular neon lamp used. An audible alarm can be activated by adding suitable electronic circuitry.



high voltage levels at the 'open' SCR end of the loop. And these levels are more than sufficient to trigger a sensitive SCR.



In some instances this type of false triggering can be overcome by connecting a 2uF capacitor between

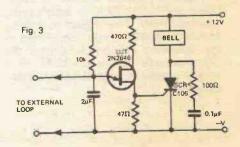
ETI CIRCUITS No. 2

the SCR's gate and cathode but generally speaking it is bad practise to connect long 'aerials' directly to the gate circuit of an SCR.

A better solution is to use a UJT as a 'buffer stage' — as shown in Fig. 3. This will ensure that the gate circuit is totally immune from false triggering no matter how long the external circuit.

False triggering may also be caused by switching transients if long external leads are used in the anode or cathode circuit of the SCR. This sometimes occurs with burglar alarms and other control and warning systems if a bell (or other load) is located some distance away from the SCR.

This problem can almost invariably be overcome by using dv/dt suppression (as shown in Fig. 1). In extreme cases it may be necessary to use a 5uF capacitor and a 5k series resistor, but values of 0.1uF and 1k will generally suffice.

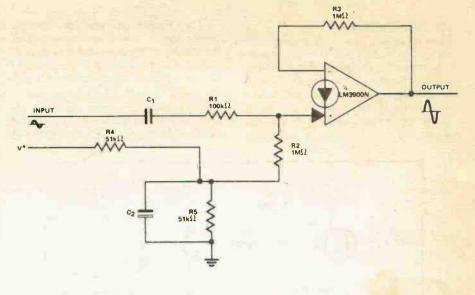


7

### Non-Inverting Amplifier

The circuit shows an amplifier which provides an output in phase with the input. The gain is equal to  $R_3/(R_1 + r_2)$  where  $r_4$  is the small signal impedance of the input diode. The value of  $r_4$  is equal to 0.026 divided by the current passing through  $R_2$  to the non-inverting input.

The capacitor values should be chosen so that the impedance of these components is considerably less than the circuit impedance at the points concerned.



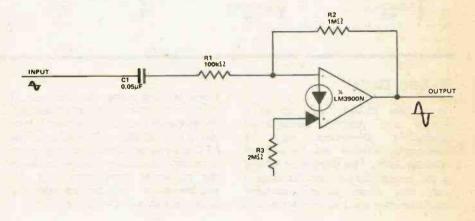
### AC Amplifier, Simple

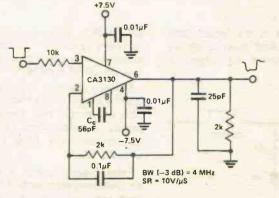
The gain is approximately equal to  $R_2/R_1$  or 10 with the circuit values shown. The means potential at the output is half the supply voltage. The value of  $R_3$  should be twice that of  $R_2$ , since the current passing through either of these resistors is then the same. The positive supply and ground connections are not shown for simplicity, but  $R_3$  should be returned to the same positive supply line as that used to feed pin 14.

The circuit provides a phase inverted output. Any ripple on the power supply line will appear on the output at half amplitude.

### **Voltage Follower**

Operational amplifiers with very high input resistances, like the CA3130, are particularly suited to service as voltage followers. Figure shows the circuit of a classical voltage follower, using the CA3130 in a split-supply configuration. The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.





#### **Flexible Response**

Figure 1 gives the circuit of a high input-impedance amplifier with a nominal voltage gain of 48 and a bandwidth of from 10 Hz to at least 50 kHz. In the prototype the measured value of input impedance was 10M Ω at 1 kHz. This value will vary slightly with frequency and with the particular layout employed, but in any case is likely to be as high as will normally be required for most applications.

As an ac connection, via a is provided at the capacitor. non-inverting input there would be no dc return for bias current, at that input, if  $R_3$  were not present. The value of  $R_3$  is 47 k however, bootstrapping is used to raise the apparent value of R<sub>3</sub> to the value of 10 megohm as quoted, in the following manner.

Due to the extremely high gain of the op. amp, and to the feedback between the output and the inverting input pin 2, there is very little difference in the signal levels at the +ve and -ve inputs, and, since C1 has a negligible reactance, there is similarly very little difference in signal voltage at either end of R3. Accordingly, very little signal current can flow into R3 from the signal input, thus R3 appears, to the input signal, to be many times its actual value.

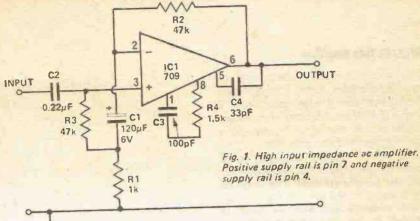
With the op. amp. arranged in the non-inverting configuration, the voltage gain is:

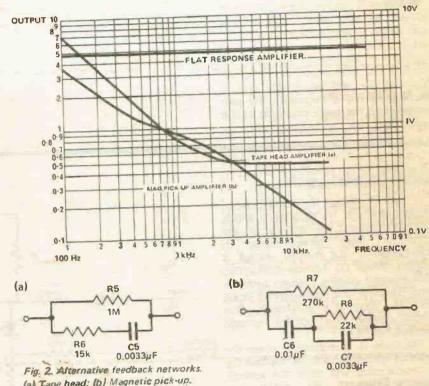
$$Av = \frac{R_1 + R_2}{R_1} = 48$$

This amplifier set-up is most likely be used in the design of a to pre-amplifier for an oscilloscope or millivoltmeter, where the high value of input impedance is necessary in order to load the circuit under test as little as possible.

In audio applications, a 'tailored' frequency response is often called for; for example, the output of a tape replay head should be fed to a stage with a gain rising at 6dB per octave below about 2.5 kHz, and a flat response above that frequency. (The actual value of the break frequency depends on the tape speed and the particular replay characteristic employed). Such a response is readily arrived at by replacing R, of Fig. 1 with the network shown in Fig. 2a.

At high frequencies  $C_5$  has a reactance low compared to  $R_6$  and hence it can be ignored. Thus the gain





(a) Tape head; (b) Magnetic pick-up.

is determined by  $R_6$  alone (although  $R_5$  is in parallel its value is large enough to be disregarded). As the frequency is lowered, the reactance of C<sub>5</sub> rises and consequently the feedback is reduced, so giving the frequency response shown in Fig. 3a. Resistor R<sub>5</sub> provides a dc connection for the negative input of the op. amp, and limits the gain at very low frequencies.

The voltage gain of this circuit at high frequencies is about 16 times; this will make the tape head output comparable to that from a magnetic pick-up. If more gain is called for, this is best done by increasing the value of

R<sub>6</sub> and reducing the value of C<sub>5</sub> in proportion.

What if a response suitable for pre-amplification of the output of magnetic pick-up is required? In this case the network of Fig. 2b is a suitable replacement for R<sub>2</sub> in the original circuit; the overall response of the stage is now as given in Fig. 3b.

Similar reasoning to that given for the tape head amplifier applies here also - the gain rises at lower frequencies as  $C_6$  reactance becomes larger, falling at the higher frequencies as the reactance of  $C_6$  and  $C_7$  both fall. As before,  $R_7$  sets the low-frequency gain.

### Hi Z, Hi Gain Amplifier

This circuit has been designed so that it provides both a high input impedance and a high gain using a simple amplifier. With the component values shown, the input impedance is one megohm and the gain 100.

The voltage applied to  $R_2$  is made equal to the output voltage (which is half the supply voltage). The value of  $R_2$  is equal to the sum of  $R_3$  and  $R_4$ ; these resistors set the dc bias. If desired,  $R_2$  may be made 4 megohms and its lower end connected to the V<sup>+</sup> supply.

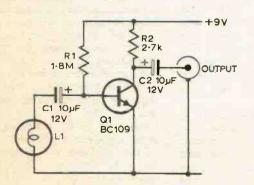
Resistors  $R_4$  and  $R_5$  form a potential divider so that only 1/100 of the alternating output voltage is developed across the  $C_2 - R_5$  circuit. This fraction of the output voltage is fed back to the inverting input via  $R_3$ . As  $R_3$  and  $R_1$  are equal, the gain is  $R_4/R_5$ . As  $R_5$  is decreased, the gain approaches the open loop gain of the amplifier.

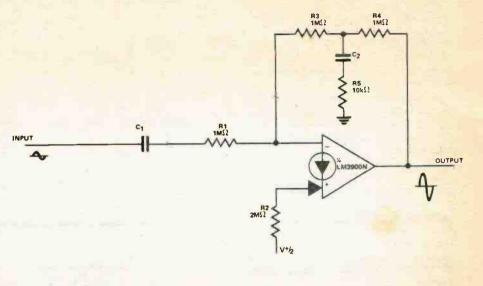
### Voltage Controlled Amplifier

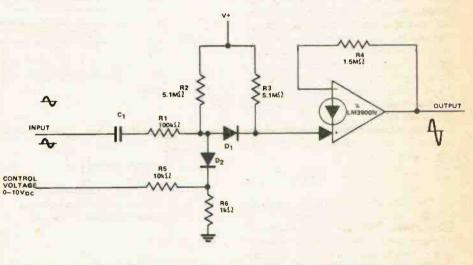
A current flows from the positive supply through  $R_3$  to provide a bias which prevents the output of the amplifier from being driven to saturation as the control voltage is varied. When  $D_2$  is non-conducting, the currents passing through both  $R_2$ and  $R_3$  enter the non-inverting input and the gain is a maximum. This occurs when the control voltage approaches 10 V.

The gain is a minimum when the control voltage is zero. In this case  $D_2$  is conducting and only the current passing through  $R_3$  enters the non-inverting input of the amplifier.

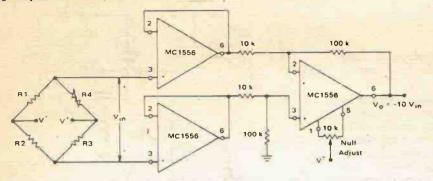
### **Recording Pickup**







It is often inconvenient to interfere with a circuit to take an audio tap off for recording etc. However by using a telephone pickup coil and placing this near the coil of almost any loudspeaker, excellent quality may be obtained with no direct electrical connection. The varying magnetic flux in the loudspeaker is induced directly into the coil. As the output may be low for some uses the very simple amplifier shown in the circuit will raise the level. This may not work well with some TV sets due to high frame pulses from the transformer which may cause a low frequency buzz though this depends on the proximity to the loudspeaker. **High Impedance Bridge** 

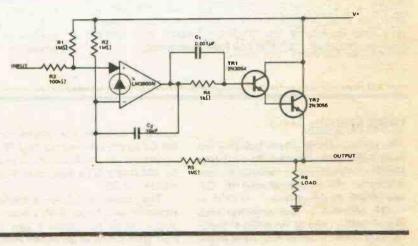


The MC1556 operational amplifier may be used as a voltage follower in a bridge amplifier application. The high input impedance avoids loading effects on the bridge and transforms the impedance down to a level where a third amplifier used in a differential mode can provide voltage gain, 10 in this case. The third amplifier employs the standard offset adjust circuit to provide nulling capability for the configuration.

Although the circuit is shown forcomplementary supply voltages, it lends itself well to operation from a single supply since the bridge can be operated just as well from the single supply. One must, however, provide for biasing the now-grounded 100 k $\Omega$ resistor to half the supply voltage using a simple resistive divider. Also, of course, the output is no longer referenced to ground, but to half the supply voltage.

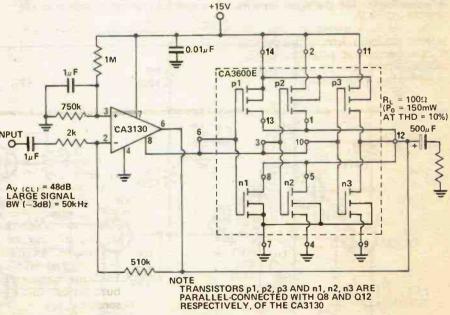
### **Direct Coupled Power**

In the circuit, the output from an LM3900N amplifier is fed to a Darlington pair of power transistors. This circuit can deliver over three amps into a suitable load when the transistors are correctly mounted on heat sinks.



### **CMOS Power Booster**

The current-sourcing and sinking capability of the CA3130 output stage is easily supplemented to provide power-boost capability. In the circuit three COS/MOS transistorpairs in a single CA3600E IC array are shown parallel connected with the output stage in the CA5130. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15V operation. This arrangement boosts the currenthandling capability of the CA3130 output stage by about 2.5.

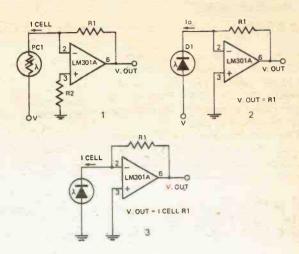


### **Photocell Amplifiers**

Amplifiers for photoconductive, photodiode and photovoltaic cells are shown in Figures 1, 2 and 3 respectively.

All photogenerators display some voltage dependence on both speed and linearity. It is obvious that the current through a photoconductive cell will not display strict proportionality to incident light if the cell terminal voltage is allowed to vary with cell conductance. Somewhat less obvious is the fact that photodiode leakage and photovoltaic cell internal losses are also functions of terminal voltage. The current-to-voltage converter neatly side-steps gross linearity problems by fixing a constant terminal voltage, zero in the case of photovoltaic cells and a fixed bias voltage in the case of photo-conductors or photodiodes.

Photodetector speed is optimized by operating into a fixed low load impedance. Currently available photovoltaic detectors show response times in the microsecond range at zero load impedance and photoconductors, even though slow, are materially faster at low load resistances.



The feedback resistance, R1, is dependent on cell sensitivity and should be chosen for either maximum dynamic range or for a desired scale factor and should be chosen to minimize bias current error over the operating range.

### 12 Volt PA System

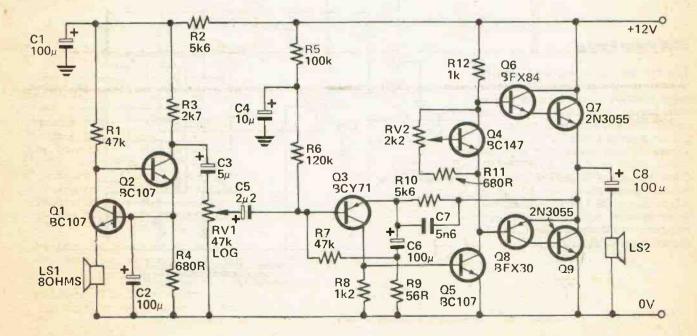
This circuit was originally built for use in a negative earth car. A miniature speaker, impedance immaterial, is connected in the emitter circuit of Q1, and acts as a microphone.

Q1 operates in the common base mode and a highly amplified signal appears at its collector. Q2, used in the common emitter mode, provides further amplification and the signal from its collector is fed via the blocking capacitor C3 to the volume control RV1.

Overall de-stabilisation is provided by obtaining Q1's base bias from the emitter of Q2.

The power amplifier is fairly conventional and fitted with a heavy duty output stage to enable a pair of  $3\Omega$  P.A. type horns to be driven in parallel. Under these conditions 8W is available. A single  $3\Omega$  unit can be driven to 4W.

Since the unit is intended for the reproduction of speech a wide bandwidth is not required and C7 is incorporated to roll off the response above 5kHz. C6 also provides a rapid roll off in the bass region. Q7 and Q9 should be fitted to a 5" x 4" finned heatsink and the body of Q4 should be thermally in contact with this.



### **Class A Amplifier**

The main advantage of class A amplifiers is the absence of crossover distortion. Against this major advantage must be weighed the disadvantage of permanently hot heatsinks and large capacity power supplies.

The circuit shown here contains several novel features and will deliver 5W of pure class A sound into an 8 ohm load.

Q1 and Q2 form, with the associated components, a high quality voltage amplifier with overall ac and

#### dc feedback applied from the collector of Q2 via R6 to the emitter of Q1.

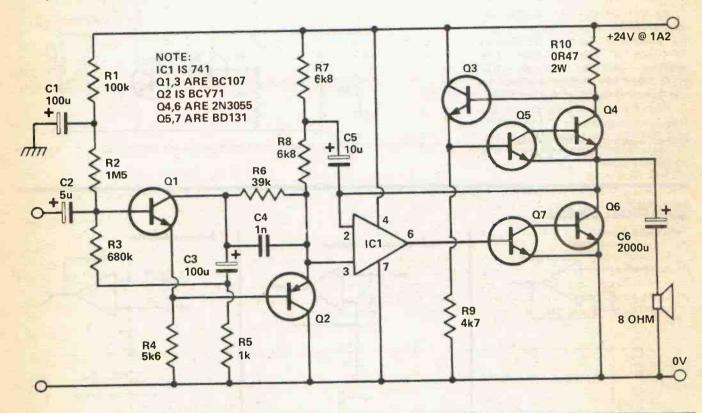
The output stage proper, consists of Q6 and Q7 connected as an emitter follower darlington pair. These transistors are driven by IC1, a 741 op amp, and are included in the latter's feedback loop.

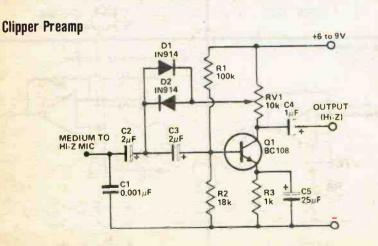
These three form a near perfect output stage with an input impedance of several megohms and a bandwidth extending from dc to over 100KHz.

Quiescent current is provided by the constant current source Q3, Q4, Q5, R9 and R10. The use of a constant current source here effectively isolates the output from line variations and ripple.

With the components shown, the circuit has a bandwidth of 10Hz - 30KHz -3db, a distortion of less than 0.1% before the onset of clipping, an input impedence of  $1.5M\Omega$  and a sensivity of 180mV for full output.

Transistors Q4 to Q7 must be mounted on an adequate heatsink, a 5" by 4" finned type is suitable, but must be mounted vertically and in such a position as to allow ample ventilation.





high average Maintaining а for mobile modulation level communications transmitters improves the considerably of a transmitter, effectiveness especially under difficult conditions. This circuit provides a small amount

of preamplification as well as variable clipping level (preset).

The two diodes should be a matched pair or clipping will not be symmetrical.

It is possible to mount the complete unit in many styles of hand-held microphone cases.

### **Headphone** Amplifier

The circuit will deliver full orchestral levels to four pairs of stereo headphones connected in parallel across the output.

Input signals are coupled to the non inverting input of a 741 op amp via the volume control RV1.

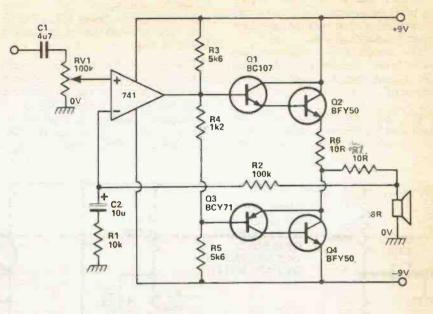
This IC is used to drive a quasi-complementary output stage consisting of Q1-4

Quiescent current in the output transistors is provided by the voltage drop across R7 and local feedback provided by R6 in Q2's emitter circuit.

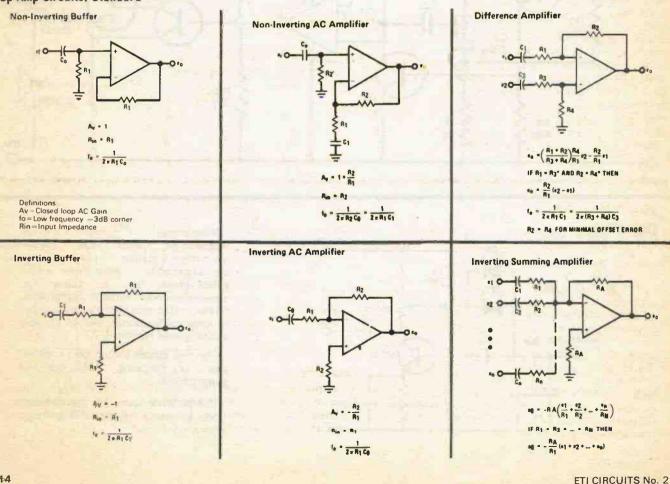
R6 is included to render the whole amplifier short circuit proof (to protect Q2 and Q4). Overall feedback is applied from the end of R6 so this 'earthy' component has negligible effect on the damping factor of the amplifier.

With the components shown the frequency response is -3dB at 4Hz and 100KHz, distortion below 0.1% at 1KHz (50mW out, 80 load), and sensitivity 60mV.

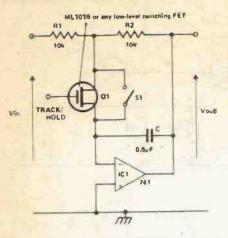
ONE CHANNEL ONLY SHOWN



#### **Op-Amp Circuits, Standard**



### **Track and Hold Circuit**



When the switch is closed (or the FET conducting), circuit is behaving

### Track and Hold, Simple>

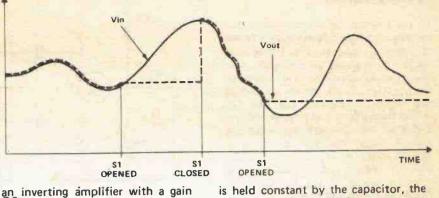
When the control input is high the output tracks the input but when it goes low the output remains frozen at the value it was at the instant of transition. The operation of the circuit is generally self-evident and it may be regarded as two voltage followers, one consisting of two oamps with the output following the input, the other is just the second op-amp which "follows" the voltage stored on the capacitor. It is advisable to take care with the layout as with all op-amp circuits due to the huge open loop gain of these devices. The value chosen for C is a compromise between slewing rate," that is the rate at

### ADSR Envelope Shaper

When a negative going trigger pulse is, applied to the input, IC2(c) disconnects the 'release' pot, the bistable is set and the 'attack' pot connected to C1. C1 charges up to the threshold voltage of IC1(c) where the bistable is reset. IC2(b) causes C1 to discharge to the level set on the 'sustain level' pot. If S1 is in position '1', when the trigger pulse goes high again IC2(c) causes C1 to discharge via the 'release' pot.

During the time IC1(a) is high C2 is charged up forcing the output of IC1(d) low. Once IC1(a) has gone low C2 begines to discharge and after a





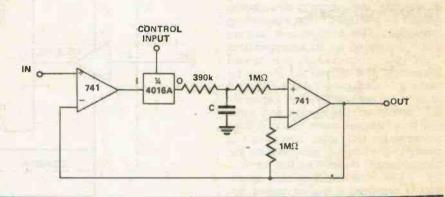
as an inverting amplifier with a gain of  $\frac{B2}{B1}$ . As the inverting terminal of op amp is a virtual earth, the the capacitor is kept charged to the output voltage by the op amp. When the switch is opened (and the FET nonconducting) the voltage at the output

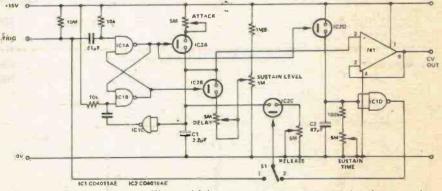
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current demands of the next stage being met by the op amp. Note that the value of C should be chosen such that its impedance at the operating frequency is large compared to R1 and R2.

which the circuit tracks a sudden change of input and "holding ability" which is the length of time, the circuit seems to optimise the performance. will hold a signal without unreasonable decay. To give some sort of

guide, for a 10kHz square wave to the control input, a 0.01µF capacitor The value of the resistors is also worth experimenting with.



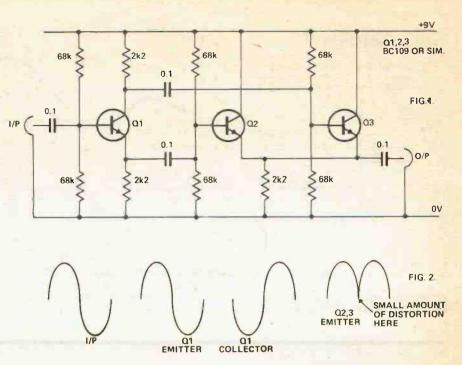


while IC1(d)'s output will go high again. When S1 is in position '2' the sustain is controlled by the monostable thus formed. It is retriggable so

that should a second trigger arrive before the cycle has completed the cycle will restart. The 741 buffers the output.

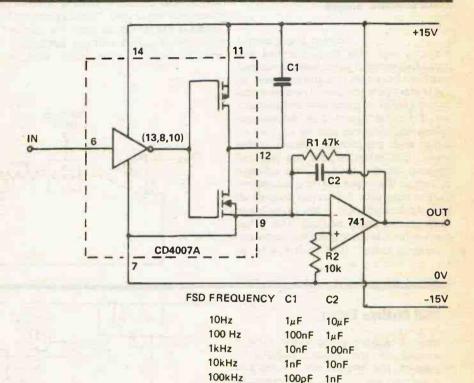
### **Frequency Doubler**

This is a simple three transistor circuit to raise an audio frequency by a factor of two i.e., one octave. Q1 is connected as a phase splitter with antiphase signals appearing at it's collector and emitter. These signals are fed to two emitter followers Q2 and Q3, which have a common emitter resistor, and thus add the two anti-phase signals. A degree of distortion is inevitable as shown in Fig. 2, but is acceptable for speech and soloists and produces a sound similar to the Chipmunks or Pinky and Perky.



### Frequency to Voltage Converter

Figure shows a linear frequency to voltage converter which works by charging a capacitor up once for every input cycle, the charge to do so being passed by a MOSFET into a summing amplifier. The component values given are based on an approproxiate five volt output for the given frequency. The resistor B1 should be made a  $100k\Omega$  preset if it is required to set a range exactly. The capacitor C2 "smooths" the output and need not be changed from 10µF if fastresponse on the upper ranges is not needed. The linearity achieved on the top range will depend on the particu-lar ''741'' used and if reliable operation is required a higher speed opamp should be used.

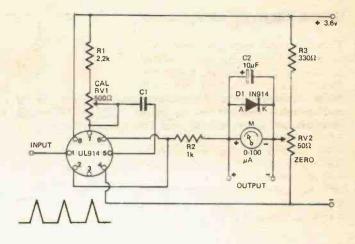


### Frequency Meter, Analogue

This circuit may be used as a pulse counter, tachometer, or if preceded by a Schmitt trigger, an analogue frequency meter.

Output linearity better than 2% can be obtained with duty cycles of less than 30%. The meter is selected so that it reads full scale when the duty cycle of the uL 914 is 30%. The choice of C1 and the meter sensitivity determines the range of measurement.

Potentiometer RV1 is used to calibrate the meter to full scale deflection, and resistor R2 counteracts the slight zero offset of the saturated IC. Diode D1 protects the meter.

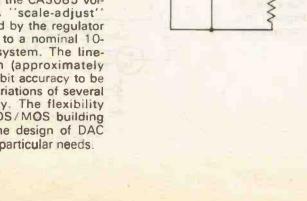


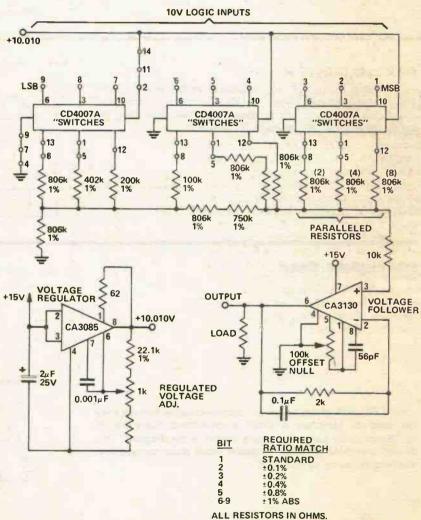
### Digital to Analogue Convertor

The circuit of a 9-bit Digital to Analog Converter (DAC) is shown. This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide film resistors, a CA3130 op-amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with COS/MOS input logic, e.g. 10volt logic levels are used in the circuit.

The circuit uses an R/2R voltageladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole doublethrow switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tollerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

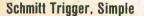
A single 15-volt supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10volt level in this system. The linevoltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.





### Schmitt Trigger, Without Hysteresis

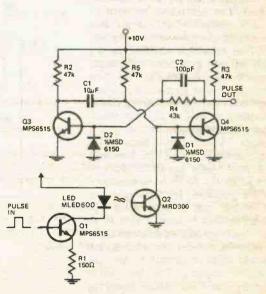
By replacing the common-emitter resistor in a conventional Schmitt by a zener diode, the hysteresis normally associated with these circuits is eliminated.

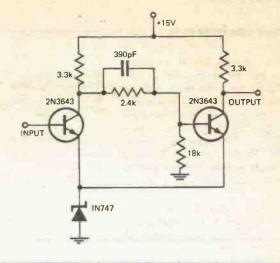


One cheap IC, uL914, can be used as an extremely simple and effective Schmitt trigger suitable for many applications. Hysterisis of the circuit is about 0.1 Volt. This may be varied by altering the values of R1 and R2.

Pulse Lengthener, Optical

An LED and phototransistor optical-coupler system may be used to lengthen a three microsecond pulse to 55 milliseconds by using the values shown in the diagram. This allows complete isolation between input pulse circuits and the lengthener to be obtained.





INPUT

INPUT

OUTPUT

V4

1.4

1.3

3.6

Q+3,6v

8200

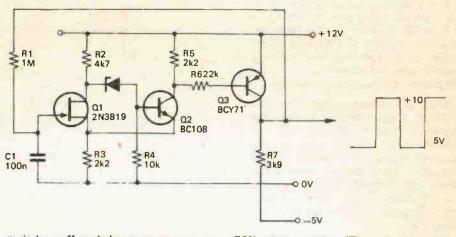
D1 UL914

R2 2752 OUTPUT

### Square Wave, Low Frequency

A drawback of low frequency oscillators using bipolar transistors or TTL logic is that the timing capacitor usually has to be a high value electrolytic. Using a field effect transistor at the input of a schmitt trigger, means a low value capacitor can be employed. The trigger by Q1 and Q2 has a hysterisis of approximately 3V. This is controlled by the 3V zener.

With C1 uncharged Q1 is off and Q2 is forward biased. The voltage at the source of Q1 is approximately  $\pm 4V$ . Q2 conducts, thus turning on TR3. The output is therefore at  $\pm 10V$ . C1 then charges via R1 and the gate voltage of Q1 goes positive. When the gate voltage is sufficiently positive Q1 conducts, turning off Q2. The positive feedback from the emitter of Q2 to the source of Q1 ensures a rapid switch off. Q3 also



switches off and the output goes to -5V. Capacitor C1 now discharge towards -5V, but when the voltage across C1 falls by approximately 3V, Q1 ceases to conduct, turning on Q2.

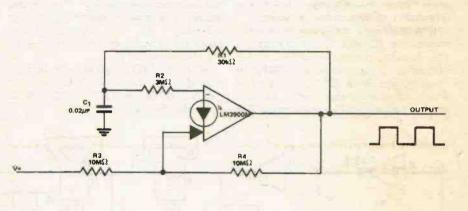
The collector load of Q3 is connected to a negative supply giving a 50% duty cycle. (The circuit still oscillates if R7 is connected to 0V but the duty cycle will change, the output remaining at 0V for a longer period than at +10V).

With the components as shown the frequency of the output is approximately 0.025Hz.

#### Square Wave Generator

The multiple amplifiers in the LM3900N device are very suitable for use in waveform generators at frequencies of up to about 10 kHz. Voltage controlled oscillators (the frequency of which is dependent on an input voltage) can also be designed using the device.

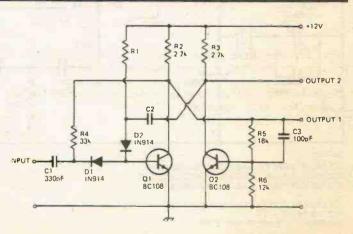
A simple square wave generator is shown. The capacitor  $C_{11}$  alternately charges and discharges between voltage limits which are set by  $R_{2r}$   $R_{3}$ and  $R_{4}$ . The circuit is basically of the Schmitt trigger type, the voltages at which triggering occurs being approximately V+/3 and 2V+/3.



### Monostable Multivibrator

The time constant T of this circuit is equal to  $0.7 R_1C_2$ . Where T is in seconds,  $R_1$  in ohms and  $C_2$  in farads. For example when  $R_1 = 10 k$  and  $C_2 = 100 microfarads$  the time constant will be one second.

Capacitor C<sub>2</sub> may be selected over wide a range and R<sub>1</sub> may be a potentiometer 100 k maximum. Outputs 1 and 2 provide pulses of opposite polarity but the rise time of output 2 is long due to the charging current of C<sub>2</sub>.



### Triangular Waveform Generator

A triangular waveform generator can be made by using one amplifier of a LM3900N device as an integrator and another amplifier as a Schmitt trigger circuit. A suitable circuit is shown, it has the unusual advantage that only the one power supply is required.

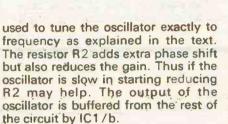
When the output voltage from the Schmitt trigger circuit is low, the current flowing through  $R_2$  is integrated by  $C_1$  to produce the negative slope of the triangular wave at output 1. When the output 2 voltage from the Schmitt trigger is high, current flows through  $R_2$  to produce the rising part of the waveform at output 1.

The output waveform will have good symmetry if  $R_1 = 2R_2$ . The output frequency is given by the equation:

### Marker Generator

The marker generator is a constantfrequency oscillator driving into a CMOS divider chain. Switchable outputs from the divider chain are selected to drive a pulse generator.

The oscillator is IC1a in which R1 biases the IC into linear operation. The crystal determines the basic frequency of operation at 4 MHz in conjunction with C1, 2, 3 and 4 which appear to the frystal as one parallel capacitor. The capacitor C2 is



 $f = V^+ - V_BE$ 

2R1C1V

R1 MΩ

82 510652 C1 0.001/JF

R3

R4

INTEGRATOR

IC2 is a CMOS dual type D flip flop that divides the 4 MHz by four to provide an out put of 1 MHz, the 2 MHz also being brought out. A further dual division by 10 is provided by IC3 which therfore provides outputs of 100 kHz and 10 kHz.

where  $R_1 = 2R_2$ ,  $V_{BE}$  is the steady

voltage at the inverting input (0.5 V)

and V is the difference between the

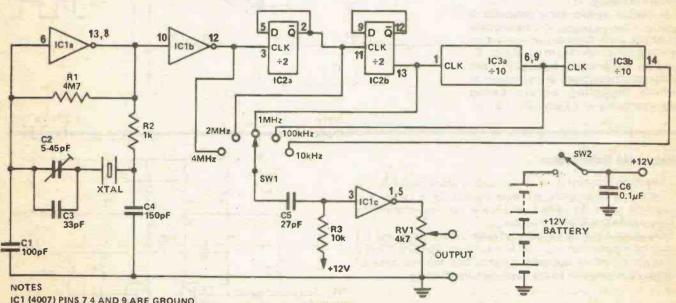
tripping points of the Schmitt trigger.

CHMITT TRIGGER

A5 120kΩ OUTPUT 1

OUTPUT 2

The required output is selected by SW1 and applied to C5 and R3 which differentiate the squarewave output of the divider. The waveform is then amplified and squared by IC1/c to provide an output train of narrow pulses, the amplitude of which may be varied by means of RV1.



IC1 (4007) PINS 7.4 AND 9 ARE GROUND IC2 (4013) PINS 6.4,8,10 AND 7 ARE GROUND IC3 (4518) PINS 8,7 AND 15 ARE GROUND

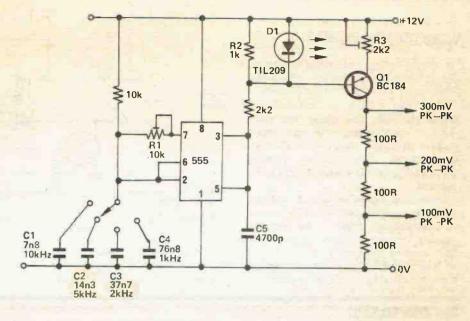
IC1 PINS 14, 2 AND 11 ARE +12V IC2 PIN 14, IS +12V IC3 PINS 2, 10 AND 16 ARE +12V

### **Voltage and Frequency Calibrator**

This circuit provides simultaneous voltage and frequency calibrations by generation of a precision squarewave.

The 555 timer IC is used in a slightly unusual configuration, having the advantage that an exact 50:50 mark/space ratio may be attained by trimming R1. The frequncy of oscillation may be set between 10 kHz and 1 kHz by switching timing capacitors C1-4. C5 decouples the internal reference potential-divider of the 555 from supply-transients.

The squarewave output from pin 3 of the IC, while stable in frequency, is not stable in peak-to-peak voltage as this depends on the supply voltage. This is used to switch on and off a temperature-compensated constantcurrent source Q1. R2 ensures that the current-source turns off completely when pin 3 goes high. The currentsource output, trimmed by R3 to be exactly 1 mA, drives a resistor ladder network so that a series of precise squarewave voltages are generated. The advantage of current drive rather



than voltage drive for this sort of network is that calibration is much easier. A simple ladder network is shown by way of example, and more complex ones may simply be constructed to give a wider variety of output voltages. The non-standard component values used were obtained by paralleling standard values. For the timing capacitors several in parallel had to be used, and only the resultant value is shown on the diagram.

### VCO, Simple

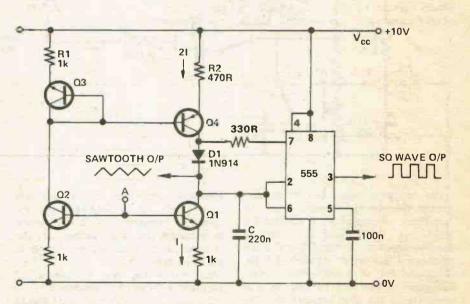
This circuit generates sawtooth and triangle waveforms at a frequency set by an external control voltage.

Current source Q1 draws a current I from timing capacitor C. Simultaneously current source Q2 draws the same current from current mirror Q3, Q4; this is set up (by R1 and R2) to deliver (from the collector of Q4) twice the current leaving Q2.

Hence C receives a current 2 I from the top rail, at the same time delivering I to the bottom rail, the net effect being that the capacitor is charged by a constant current I, its voltage rising linearly until the 555's upper trigger point (at 2/3Vcc) is reached.

The output (pin 3) then goes low, as does the open-collector discharge output at pin 7. The latter shunts the output of the current mirror to earth, D1 becoming reverse-biased and isolating C.

Now only current source Q1 is connected to the timing capacitor which is now linearly discharged by current I. In this way C is alternately charged and discharged. When the voltage on C falls to the 555's lower trigger point at 1/3Vcc, the output and discharge pins go high, and the



cycle recommences; the repetition frequency is determined by the magnitude of I, which is set by the voltage applied at the input point A.

With the component values shown, the frequency range is from approx.

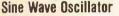
2.5 kHz to less than 10 Hz, as the control voltage varies from +10 V to zero; the frequency is directly proportional to the control voltage. Other ranges may be obtained by altering the value of C.

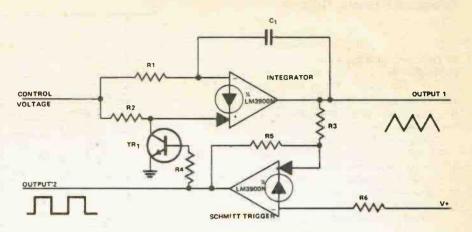
### **Voltage Controlled Oscillator**

A simple voltage controlled oscillator circuit which produces both triangular and square wave outputs is shown.

Then the output of the Schmitt trigger is high, the clamp transistor  $TR_1$  is conducting and the input current passing through  $R_2$  is shunted to ground. The current passing through  $R_1$  causes a falling ramp to be formed.

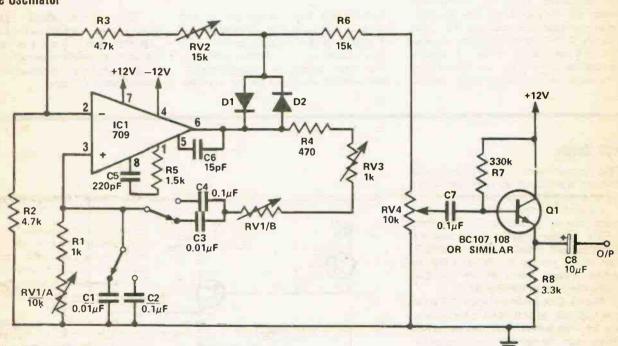
When the Schmitt circuit changes state, its output switches  $TR_1$  to the non-conducting state. The current flowing through  $R_2$  can be made twice that flowing through  $R_1$  ( $R_2 = R_1/2$ ) so that the rising part of the ramp has a similar slope to the negative part.





The greater the value of the control voltage, the greater the frequency of oscillation. However,

the voltage must exceed the constant input voltage ( $V_{BP}$ ) or the circuit will fail to oscillate.



The oscillator makes use of the well known Wien-bridge network to set the frequency of operation. A resistor (in this case RV1a and R1) and a parallel capacitor (either C1 or C2) are connected to further resistors (RV1b, RV3 and R4) in series with a further capacitor (either C3 or C4). It is a property of the Wien network that the junction of the two RC arms, has, at a single frequency only, a voltage in phase with, but smaller than, that applied to the whole network. Since, in the oscillator, this in-phase voltage is fed to the non-inverting terminal of the op. amp. it constitutes positive

feedback, and thus oscillations will occur and be maintained at one specific frequency – a frequency determined by the values of the resistors and capacitors employed in the Wien network.

So much for the frequency of oscillation. What of its amplitude?

Consider for a moment what would happen if, with the oscillator already giving a sine wave output, the output amplitude should increase for some reason. If it continues to do so, eventually the voltage will become so large that it will be limited by the supply rails and a clipped sine wave will result. Conversely, if the amplitude of oscillation should decrease, then oscillations will eventually die away to nothing.

Such variations in amplitude can easily arise due to temperature changes etc., and will in any case occur as the frequency is altered, due to tolerances in the capacitor values and tracking errors in the twin gang potentiometer.

Thus, some means of automatic gain control is essential in order to maintain a constant output amplitude. It will be recalled that the signal voltage applied to the op. amp. non-inverting input was smaller than

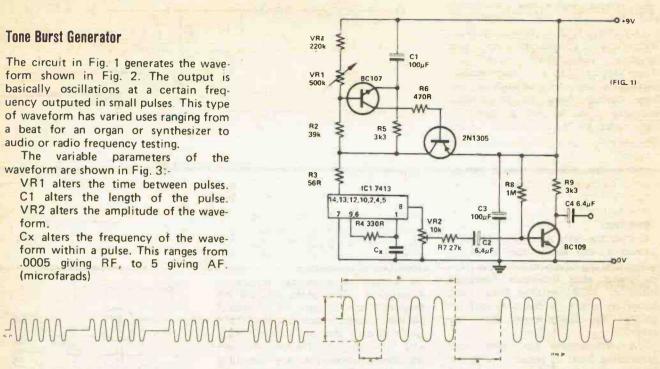
### **Tone Burst Generator**

The circuit in Fig. 1 generates the waveform shown in Fig. 2. The output is basically oscillations at a certain frequency outputed in small pulses. This type of waveform has varied uses ranging from a beat for an organ or synthesizer to audio or radio frequency testing.

The variable parameters of the waveform are shown in Fig. 3:-

VR1 alters the time between pulses. C1 alters the length of the pulse. VR2 alters the amplitude of the waveform

Cx alters the frequency of the waveform within a pulse. This ranges from .0005 giving RF, to 5 giving AF. (microfarads)



the output voltage due to the attenuation in the Wien network. To maintain oscillation the op. amp. must have a gain equal or exceeding this attentuation - which is in fact x3. The desired gain is obtained by selecting the ratio of feedback resistance to input resistance of the inverting input (RV2 + R3)/R2.

If the overall gain, including feedback, exceeds unity the circuit will produce sine wave oscillation at a frequency set by the Wien network.

Stabilisation of the gain is brought about by the action of diodes D1 and

D2. When the instantaneous output voltage is close to zero, neither diode conducts, since even a germanium diode requires 0.4 volts or so forward voltage to bias it on. Consequently, the negative feedback loop is open (giving maximum gain) and, under the action of the positive feedback via the Wien network, oscillations build up rapidly. As soon as their amplitude is

sufficient to bias on either D1 or D2 (depending on the polarity of the output voltage swing), then R2, R3 and RV2 provide negative feedback, so limiting oscillations to a convenient level.

Re-inforcement of such oscillations takes place close to each zero crossing when D1 and D2 are open i.e. non-conducting; the setting of RV2 determines the final amplitude.

This method of stabilisation does give rise to a very small amount of crossover distortion, but the effect of this can be minimised by setting VR2 for the largest possible sine wave without clipping. In any event, some distortion is a small price to pay for such a simple, easy-to-get-working sine wave oscillator and, further, it is a low level of distortion - some class B audio amplifiers are worse!

Range switching is confined to a choice of two ranges, in the interest of simplicity and cheapness, but more ranges could easily be provided if the

constructor is so inclined.

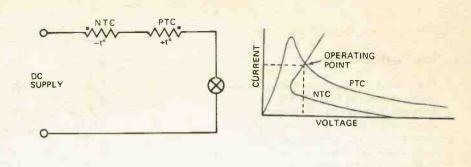
A simple emitter-tollower output stage completes the unit, with a logarithmic potentiometer as a level control, enabling the output to be set from 1 V rms down to 10 mV rms or SO.

With wiring up completed and thoroughly checked, switch on and, if possible, monitor the output on an oscilloscope. No 'scope? Then a pair of headphones, of reasonably high impedance, can be used instead. Set RV4 about half way, S1 to "low" and RV1 about half way. If there is no output, adjust RV2; clockwise rotation should give increased output. With an ac meter, measure the signal level at the junction of D1, D2 and RV2. Adjust RV2 for 3 volts rms. This will ensure the highest output level

(thus reducing the effect of crossover distortion) consistent with sine wave operation (no clipping). This should provide about one volt rms at the output.

### **Thermistor Oscillator**

A simple very low frequency oscillator can be made hv interconnecting one positive temperature co-efficient and one temperature negative co-efficient thermistor in series. For conditions of oscillation the characteristics of the two devices have to be chosen carefully. The operating point is determined by the intersection of the two curves.

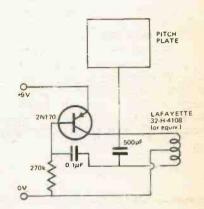


#### Theremin

This is the only musical instrument known to the writer that is played without being touched! The Theremin is named after Professor Theremin who, in 1928, amazed New York audiences when he demonstrated his ability "to obtain music from the ether".

The instrument has two rods protruding from its housing, each one forming one 'plate' of a capacitor. The performer's hands become the second 'plates' when held near the rods. The capacitive changes engendered in one rod controls the pitch of the tone, the other rod responding by varying the amplitude of the output.

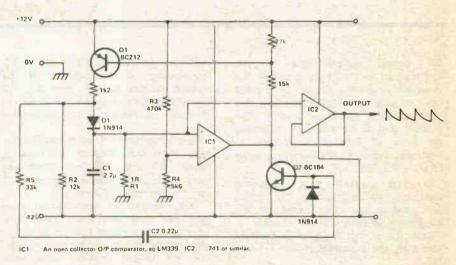
A simple experimental circuit is illustrated. The plate should be around 30cm. square. It is placed next to a radio receiver tuned to a fairly strong station around 900 kHz. The slug of the coil is then adjusted to obtain the most pleasing tone. When the hand is moved near the plate, the picth of the tone will change.



### **Exponential Waveform Generator**

This circuit produces a waveform that decays exponentially from a set voltage to near-zero, and then rapidly resets to re-start the cycle.

Initially C1 is charged to +12V, and Q1, Q2 are both off. The timing capacitor there discharges slowly through R1, the exponentially decaying voltage appearing at low impedance at the output of unity gain buffer IC2. R2 prevents the leakage current from Q1 affecting the discharge as D1 is reverse-biased. When the voltage on C1 reaches a value just above zero that is set by R3, R4, the open-collector O/P of IC1 goes low, turning on Q1 and rapidly recharging C1. IC1 of course reverts to its original state almost at once, but the recharge mode is prolonged for several milli-



seconds by the positive feedback loop through R5, C2 and Q2, to ensure C1 charges fully. After this time C2 is also fully charged, and Q2 turns off, turning off Q1, and allowing the slow discharge of C1 to begin again. With the component values shown,

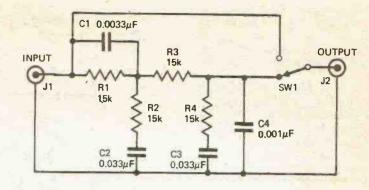
each cycle lasts about ten seconds.

#### Loudness Control

Many modern high quality amplifiers have loudness controls built in. In most instances they are manually switched into circuit when required — in a few amplifiers the circuit is switched in at all times.

Nevertheless there are innumerable older or present-day low-priced amplifiers that are not fitted with loudness compensation — and it is for units such as these that this simple project has been designed.

The device shown is for a mono amplifier — two are required for stereo amplifiers. It can be very simply assembled on tag strips or matrix board, and, when completed connected between your preamplifier and main amplifier. If yours is an integrated unit it should be readily possible to break into the volume control circuit — just connect the unit in series with the slider terminal of the potentiometer. Screened leads may be necessary of long lengths are required.

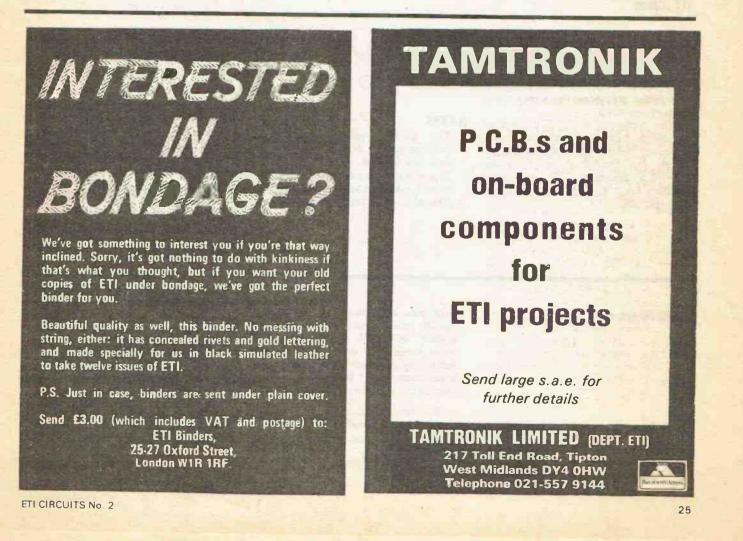


We would like to emphasize that this is a 'compromise' circuit. Ideally a loudness control must be designed specifically to suit the amplifier for which it is intended. Also the degree of loudness compensation should be related to the volume control setting.

This latter requirement involves replacing the existing volume control by a suitably tapped potentiometer a device that is not readily available "off the shelf" — so the circuit shown here introduces a fixed amount of compensation that is adequate for moderate listening levels.

This circuit will suit most amplifiers quite well – and in any case can be adjusted by minor variation of component values if required.

Switch SW1 should be a double-pole double-throw type if stereo operation is required.





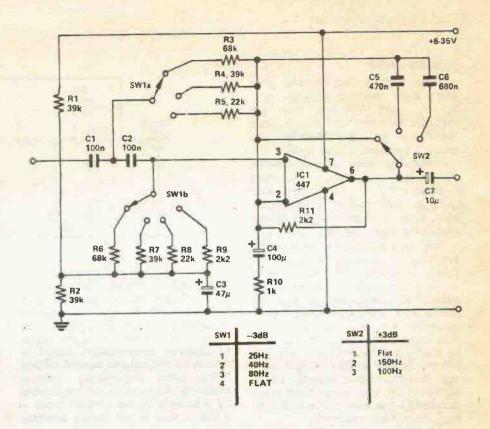
### **Bumble Filter, Switchable**

The circuit shown provides a cut-off at 25, 40, or 80Hz, C1 and C2 in conjunction with R3 - 9, form second order Butterworth filters with 12db/ octave roll-off below the turnover frequency.

Unlike most designs, the feedback is taken from the inverting input. In practise this works well once the signal at this point follows exactly that at the non-inverting input.

A useful feature is the deep bass boost provided by the feedback loop proper.

S2 in position 3 gives a +3db point at 100Hz whilst position 2 provides a +3db point at 150Hz. A supply 6-35V DC at 10mA is required.

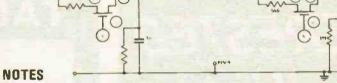


### VCF, Cheap

Readers intending to build the dynamic noise limiter may be interested in the following circuit.

The circuit consists of two RC low pass filters connected by a unity gain buffer (inverting).

The n-channel MOSFETs are used as voltage controlled resistors to vary the cut-off frequency of the two filters which are controlled by a voltage entered at points X – The additional resistors limit the variation to limits of 5 and 50kHz.



- 1. The control voltage should be positive-going, not negative-going as in the original.
- 2. Signal input should be resticted to 50mV, when distortion will be low.
- 3. The cut-off is less sharp than the

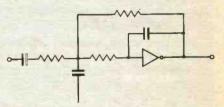
DNF VCF so less trouble can be expected from changes in bandwidth, as such changes will be less obvious.

4. A high impedance buffer is required at the output.

### **CMOS** Filters

High pass and low pass filters may be readily constructed using CMOS inverters (CD4007 CD4069 74C04) since these have only a single complementary pair, and hence lower power dissipation and less likelihood of instability. A form of Sallen and Key:

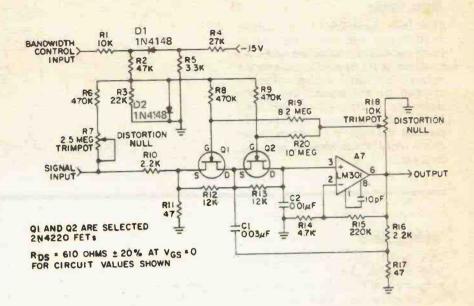
Standard equations are used to determine component values. It is recommended that passband gain be restricted to unity.



### FILTERS

### **Voltage Controlled Filter**

An input attenuator (R10 and R11) limits the signal amplitude presented to the FETs to about 0.1 volt p-p at 0 VU to ensure low distortion. Output amplifier A7 makes up exactly for this loss. An op amp having external frequency compensation was used here so that this relatively high-gain stage could be tailored for flat response to 15 kHz (a 741 could be used, but would roll off slightly above 10 kHz). Resistors R16 and R17 attenuate the output signal by an amount equal to the gain, so that this amplifier doubles as the unity-gain buffer required for filter operation. The highest cutoff frequency is dictated by minimum FET resistance and capacitors C1 and C2. The latter should have values in a ratio of about 3:1 to produce the desired Butterworth response.



#### **Tone Control**, Active

The input signal is applied to the non-inverting input of the IC which is a Siemens TAA861 operational amplifier. Bass and treble boost and cut are controlled by the potentiometers RV1 and RV2 respectively.

Control range is 20 dB of boost or cut at 50 HZ and 15 dB boost or 20 dB of cut at 12 kHz.

The overall gain of the circuit at 1 kHz is 15 dB and the input impedance is greater than 80 k ohm. Total harmonic distortion for 2.4 volts output is less than 0.5% and remains below 4% for up to 3.5 volts output.

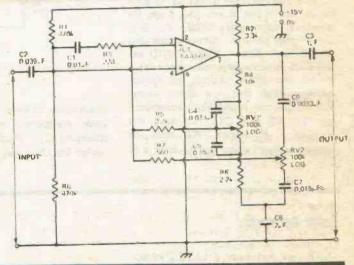
Correct law for the potentiometer is antilog. This may be obtained by using slide potentiometers which are mounted in reverse (end-for-end) to normal.

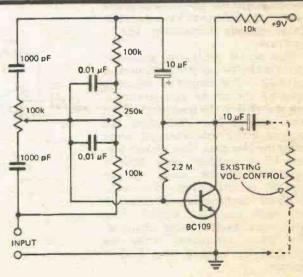
Note that equalization is not incorporated in this preamplifier.

#### **Tone** Control Circuit

This simple single-transistor circuit will give approximately 15 dB boost or cut at 100 Hz and 15 kHz respectively. A low noise audio type transistor is used, and the output can be fed directly into any existing amplifier volume control to which the tone control is to be fitted.

The gain of the circuit is near unity when controls are set in the "flat" position.

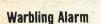




## SPECIAL EFFECTS

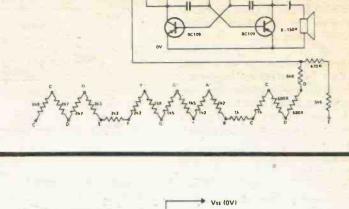
### Organ, Simple

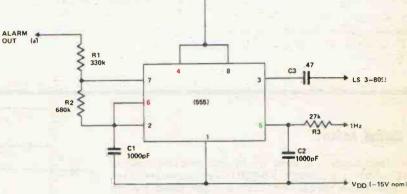
The tone generator is an astable multivibrator with one of the resistors being variable to change the notes. An amplifier could be used to increase the volume, but quite a high volume is attained by the astable. Due to the simplicity of the circuit the wave form is rather irregular in shape. (To produce the note, the probe is moved across metal strips wired to points A, B, C etc.)



This device gives a two-tone alarm from a digital clock. It may be used with any CMOS alarm clock chip having an active high alarm output and 1Hz (optional) output. It was built to work with a CT7001 chip and requires no interface components.

The 555 operates in normal astable mode when the alarm goes high (ie point (a) approaches VSS). Pin 5 is the normal control voltage input and swings from almost VSS to VDD via the 27K resistor at a 1Hz rate. This causes the audio output to switch between high and low tones, above and below the frequency determined by R1, R2 and C1. To vary the frequency difference, R3 may be altered within wide limits, but it is



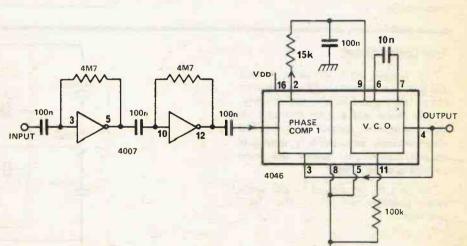


inadvisable to keep it below 15K. The basic frequency is best varied by changing C1. Audio output may be varied by changing C3 (depending on LS impedance). In the original, a  $35\Omega$  speaker was used with -12V VDD and was sufficient to rouse an expert heavy sleeper.

### **Guitar Synthesiser**

This circuit uses a CMOS Phase Locked Loop, the 4046, to produce a very unusual sound from a guitar, which sounds something like a syntheiser.

The signal from the guitar is amplified by two of the amplifiers in the 4007. The amplified signal is used by the phase comparator to lock the VCO to the frequency of the note played. The VCO does not oscillate until a note is played, when using the low pass filter shown (i.e. the 15 k resistor and 100 n capacitor). If the value of the resistor is increased, the VCO oscillates continuously at about 1 kHz (with no input signal). This gives very smooth note changes. The basic frequency may be changed by varying the 100 k resistor.

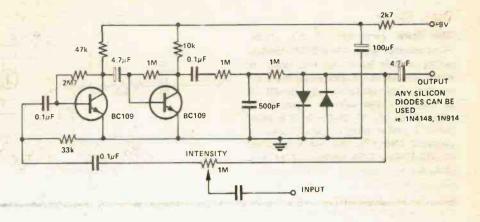


min

# SPECIAL EFFECTS

### **Guitar Fuzz**

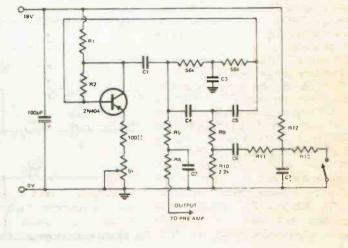
The input signal is amplified by the two transistors. The distorted output is then clipped by the two diodes and the high frequency noise is filtered from the circuit via the 500pF capacitor. The 1 M pot adjusts the intensity of the fuzz, but this tends to make the unit oscillate, so a 33k resistor is put between the input and ground to stop this. When the pot is at minimum intensity the unit may be switched off to allow normal playing.



### Drum Simulating

A variety of percussive sounds may be obtained with variations on a simple twin-T oscillator of the type illustrated. The table is given as a guide to the frequency determining and envelope shaping components.

	DRUM	TOMITOM	BONGO	BLOCKS	
85	22K	82K	82K	330K	
R6	10K	82K	82K	not used	
R9	2.7K	6,8K	6.8K	6.8K	011 14 1
R11	82K	22K	27K	not used	
R12	TM	0 56M	EM	154	
R13	2,7K	2.7K	27K	6 8K	
C1	01	0 047	0.047	0 047	
C2	0.1	0.01	0.01	not used	
C3	0.1	0.047	0.033	0.01	
C4	0.1	0.027	0.015	0.0033	
CS	0.1	0.027	0,015	0.0033	
C7	0.1	0.1	0.01	01	



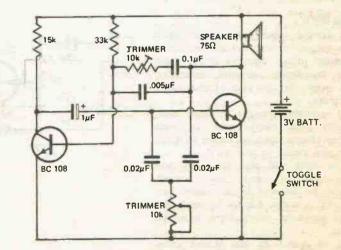
### Fishcaller, Transistorised

A lot of controversy exists among amateur fishermen as to the effectiveness of "fish-callers". Some swear by them, others just shake their heads.

watt 10"

Here's an inexpensive way of finding out. The two-transistor circuit drives the speaker. Varying the two potentiometers produces a wide variety of sounds. You may be lucky and hit on one that will bring in the big ones.

An inexpensive waterproof housing is a *thick-walled* polythene bag with a few lead sinkers inside. An on-off toggle switch can be manipulated without opening the bag when switching power on and off. The bag opening is sealed with good quality electrical tape to make system waterproof. Tape seal should be renewed after each use.

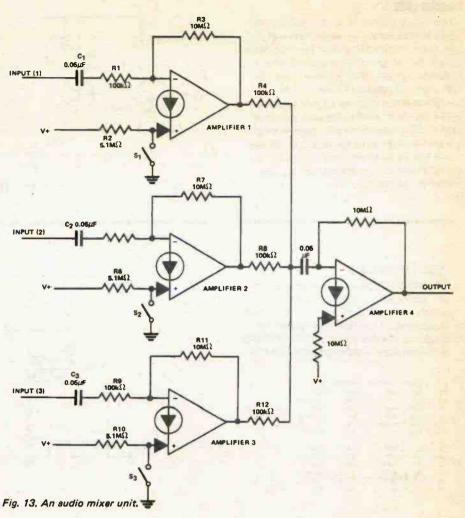


### MIXERS.

#### **Audio Mixer**

The amplifiers of a LM3900N device can be conveniently used to make a mixer unit for audio purposes; the unit enables three separate audio signals to be mixed together to produce a composite output. The circuit shown provides this facility using only a single LM3900N device and also enables any one channel to be selected by switches. The currents passing through the resistors  $R_{4\nu}$   $R_{8}$ and  $R_{12}$  are summed in the input circuit of the fourth amplifier.

If  $S_1$  is open, amplifier 1 will be driven to saturation by the current passing through  $R_2$ . It will therefore be inactive.



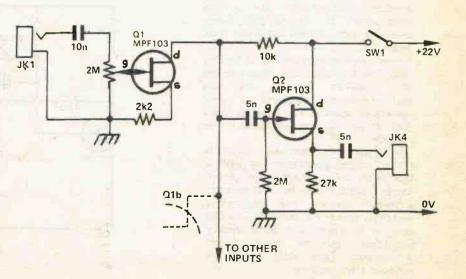
#### **Basic Mixer**

This simple mixer circuit will work with two or three channels, providing excellent input isolation and exceptional frequency response, extending well over the top end of the audio spectrum.

It is usable by one or more instruments plus microphone, or with special effects, such as mixing an input with pink noise, to give 'surf'.

The unit will give 8db gain, and since low-level signals are involved, should be housed in an aluminium box. If a mains supply is used, the usual anti-hum precautions must be taken.

It is useful to use scaled slider potentiometers, so that effects may be re-created.



ETI CIRCUITS No. 2



### **Switched Mixer**

The circuits illustrated first appeared in "dB", March 1969. It is, in essence, a twelve-channel ring sequencing device, with provision for external trigger. When the switch is at 'interrupt' a single 12-event sequence occurs. The start button is pressed to insert a pulse into the ring generator and, by pressing this button more than once, it is possible to generate highly complex sound patterns, as the multiple pulses follow each other round the ring.

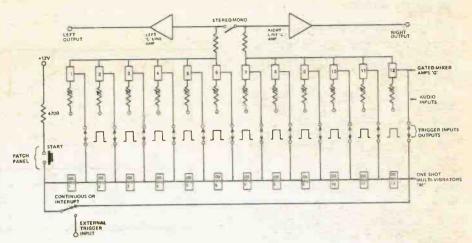
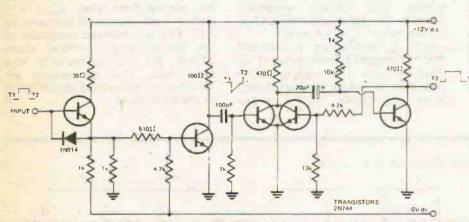
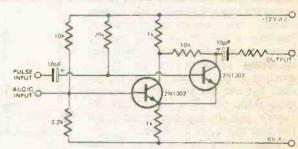


Fig. 1. Twelve channel switching mixer.





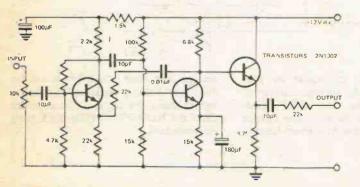


Fig. 2. Circuit details of switching mixer shown in Fig. 1. TOP: One-shot multivibrator 'm'. CENTRE: Gated mixer-amplifier 'G'. BOTTOM: Lineamplifier 'L'.

### DETECTORS & COMPARATORS.

### Low Battery Warning

The prototype of this device will be used in a hospital operating theatre in conjunction with battery operated medical equipment (powered by four 'pen-light' cells).

A moving coll voltmeter was not appropriate as, in the designers' experience, medical staff have difficulty in interpreting a voltmeter – and sometimes find themselves half way through an operation with exhausted batteries. Therefore, the requirements for the indicator were that:

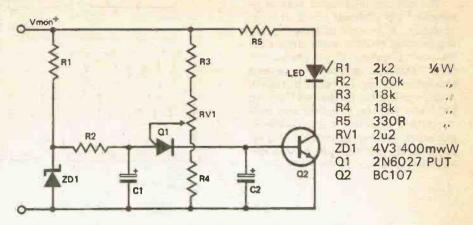
1) the display be eye catching, easily understandable and provide a sense of urgency as the battery approaches exhaustion;

2) provide adequate warning of battery failure (at least 1 hour);

3) current consumption of the indicator be low in relation to the main equipment;

4) preferably, be more rugged and cheaper than a moving coil meter.

The design was based on a programmable unijunction transistor (PUT), because its threshold characteristics can be well defined, arranged to flash a light emitting diode (L.E.D.) indicator.



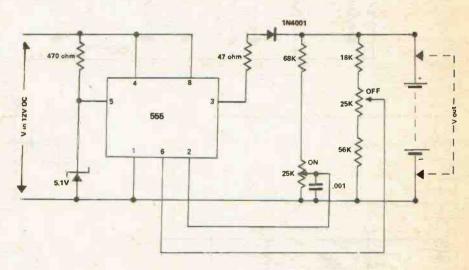
The circuit is shown in Fig. 1. The PUT (Q1) is used in a relaxation oscillator circuit. As the voltage being monitored  $(V_{mon})$  falls, the voltage on the gate  $(V_g)$  falls whilst the anode voltage  $(V_a)$  remains essentially constant. Oscillation commences when  $V_a$  falls below  $V_a$  by 0.6 volts.

 $V_g$  falls below  $V_a$  by 0.6 volts. As  $V_{mon}$  falls further,  $V_g$  falls and the PUT triggers at lower values of  $V_a$ . Thus the cycle time shortens and the frequency of flashing increases giving a sense of urgency as the battery approached exhaustion. Transistor Q2 and C2 act as a pulse stretcher and amplifier to drive the L.E.D. display. In the prototype the trigger point can be adjusted from 4.5-5.5 volts and the current drain when V<sub>mon</sub> is 6 volts is 1 mA (controlled primarily by R1). This is considered acceptable as the device being monitored draws 17 mA. All the requirements have been met. The components are mounted on the printed circuit board of the main device.

### **Battery Voltage Monitor**

The 555 timer can conveniently function as the heart of an automatic battery charger, the circuit is intended to maintain a full charge on a standby battery supply for an instrument that is always connected to the mains, whether in use or not. It can also be used for the charger unit for pocket calculators, etc. The circuit uses the timer's two on-chip comparators, the flip flop and driver amplifier.

A zener provides a reference voltage somewhere near the battery voltage with an allowance for adjustment. The two potential divider networks supply the comparators with adjustable voltages, one for LOW (switch on) and the other for HIGH (switch off). When on, the output gives a maximum of 10V and when off gives 0V, the maximum current is 150mA which is limited by the 47 ohms and protected by the diode.



The circuit is calibrated by substituting a variable voltage supply for the NiCd batteries. The HIGH adjustment is set first so that the output switches off at the maximum battery voltage and then the LOW is set for minimum battery voltage. It is simplest to leave the output disconnected from the resistor until after the setting up procedure.

### DETECTORS & COMPARATORS

### **Recording Level Meter**

The circuit shows a two-stage voltage amplifier driving a recording level meter. The AC signal input is amplified, rectified, and the resultant DC voltage shown on the meter. The circuit can be used with a taperecorder or audio mixer and should be fed from a point early in the pre-amp. Current consumption in a no-signal state is 2.8mA. The 12K preset gives a variation in sensitivity. The meter can be any general purpose type.

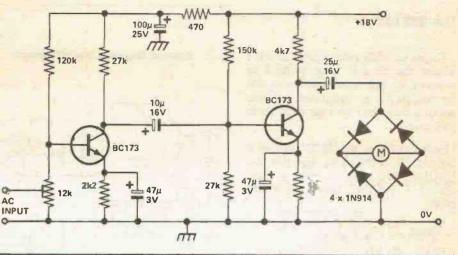
### **Comparator Voltmeter**

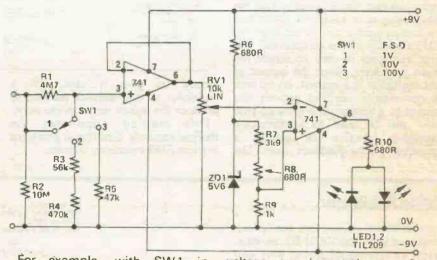
This circuit, although simple, is capable of accurate voltage measurement. The input is applied to the high impedance input of IC1 via the attenuator comprising of R12, 19 R5 inclusive.

Since this IC is used as a unity gain buffer, the output at pin 6 is equal to the input voltage at pin 3, but at a low impedance. IC2 is connected as a comparator driving a pair of LEDs, D1 and D2.

The inverting input samples a portion of the unknown input voltage, whilst the non-inverting input is connected to a 1V reference obtained from the stable voltage across ZD1.

In use RV1 is adjusted till D2 just illuminates. At this point, if the control knob is of the 0 - 10 calibrated type, the pointer will Indicate the input voltage.



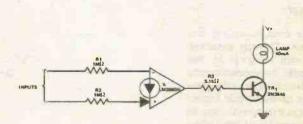


For example, with SW1 in position 2, and with a reading of 2 on RV1, the input voltage will be 2V. With a little practice, the voltage can be read to  $\pm 2\%$ . comparable to a moving coil instrument. The input impedance on all ranges is  $3.2M\Omega$ .

### **Voltage Comparator**

The circuit shows how an LM3900N amplifier may be employed to compare two input voltages and to indicate the result by means of a small lamp. If the input voltage connected to the non-inverting input is appreciably more positive than the other input, the output of the amplifier will provide a positive voltage which renders the TR<sub>2</sub> conducting. The lamp will then be illuminated.

One of the inputs may be a reference voltage so that one can then compare a single input voltage against this constant reference.



### DETECTORS & COMPARATORS

### **True RMS Detector**

To get an RMS value when you can't afford the time it takes to heat an element, try this technique. It may not be feasible for a multimeter but how about a sampling voltmeter good up to 600 kHz?

Mathematically, the RMS value of a function is obtained by squaring the function, averaging it over a time period T and then taking the square root:

$$V_{RMS} = \sqrt{\frac{1}{T}} \int_{0}^{t} V^{2} dt$$

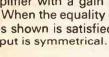
a practical sense this same In technique can also be used to find the RMS value of a waveform. Using two multipliers and a pair of op amps, an RMS detector can be constructed. The first multiplier is used to square the input waveform. Since the output of the multiplier is a current, an op amp is customarily used to convert this output to a voltage. The same op amp may also be used to perform the averaging function by placing a capacitor in the feedback path. The

#### **Positive Peak Detector**

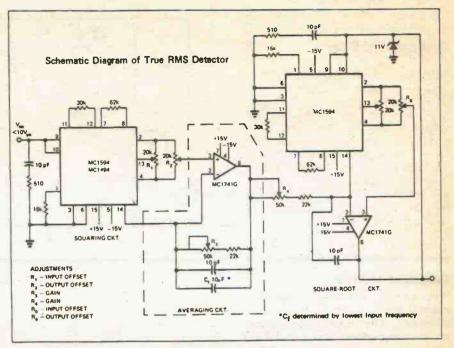
Peak-detector circuits are easily implemented with the CA3130, as illustrated: It should be noted that with large-signal inputs, the bandwidth of the peack-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA3130 limits the bandwidth in this case.

### **True RMS Convertor**

An absolute-value circuit, using the CA3130 is shown. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier negative such that the 1N914 diode effectively disconnects the amplifier from the signal path. During the negativegoing excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to -R2/R1. When the equality of the two equations shown is satisfied, the full-wave output is symmetrical.



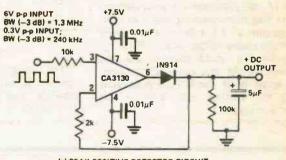
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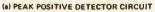


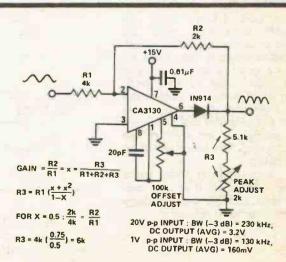
second op amp is used with a multiplier as the feedback element to produce the square root configuration. This method eliminates the

thermal-response time that is prevalent in most RMS measuring circuits.

The input-voltage range for this circuit is from 2 to 10 Vpk. For other ranges, input scaling can be used. Since the input is dc coupled, the output voltage includes the dc components of the input waveform.







### DETECTORS & COMPARATORS

### Temperature Sensor, Differential

The circuit is comprised of three parts (i) the differential temperature sensor (ii) a differential amplifier to provide gain (iii) a switiching circuit to monitor the output from the differential amplifier.

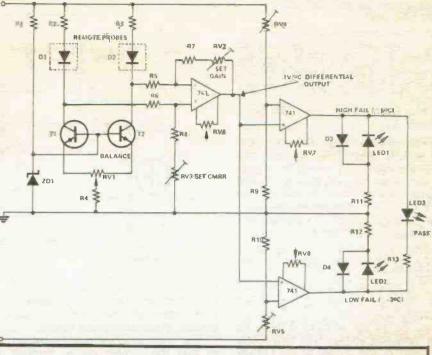
Two diodes D1 and D2 are used as probes for the sensor. A small preset, RV1 provides fine adjustment of the current through each branch so as to give zero differential output between D1 and D2 when they are at the same temperature.

A gain of 500 must be provided at the differential output to provide a useful voltage to switch the LED's (....ie IV corresponding to 1°C.) RV2 provides fine adjustment of the gain and RV3 adjusts the CMRR.

A potential divider network is set up by RV4, R9, R10, RV5 to provide the necessary switching voltages for the voltage comparators, thus enabling LED1 or LED2 or LED3 for voltages set up by RV4 and RV5...ie.. -3V and +5V.

### SETTING UP

- 1. Adjust offset-null on all Op. Amps for zero output by connecting input terminals together and taking to ground and adjusting either RV6, RV7 and RV8.
- 2. Adjust CMRR for differential amplifier by shorting input terminals and connecting to +15V line, then adjusting RV3.
- 3. Apply probes D1 and D2 to a liquid, say at room temperature," and adjust RV1 until there is zero output across collectors of T1 and T2.



RV2,RV3	100k	3 Operational Amplifiers	741
RV1	$100\Omega$	ZD1	400mW.3V3
PRESETS		LED3	miniature GREEN
R11,R12	1.2k	LED1,LED2	miniature REC
R9	390Ω	D3,D4	1N914
R7,R8	910k	D1,D2	1N4004
R5,R6	2k	DIODES	
R4,R10,R13	1k	T1,T2	BC108
R2,R3	51k	TRANSISTORS	
81	2.2k	RV6,RV7,RV8	10
RESISTORS		RV4,RV5	2.2

4. Apply probe D1 to a liquid at a temperature 10°C different from above, then adjust gain control RV2 until there is 10V at the diff. amplifier output. The CMRR

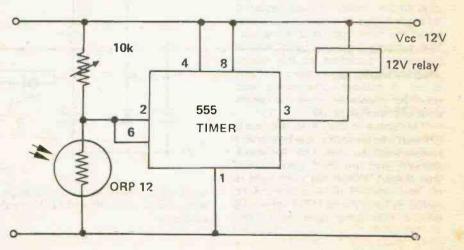
should again be set.

5. Adjust RV4 and RV5 so that the comparators switch at -3V and +5V corresponding to -3°C and +5°C.



A very useful schmitt trigger can be made by utilising a single 555 timer with its trigger and threshold inputs connected together. The schmitt has a very low input current (1.5uA) and can directly drive a relay taking up to 200mA of current.

The circuit shows a 555 schmitt being used to energise a relay when the light level on a photoconductive cell falls below a preset value; the relay energises when the voltage on pins 2 and 6 is greater than 2/3Vcc and de-energises when the voltage falls



below 1/3Vcc. This gives a hysteresis of 1/3Vcc. The circuit can be used in many other similar applications where

a high input impedance and low output impedance are required with the minimum component count.

### INDICATORS

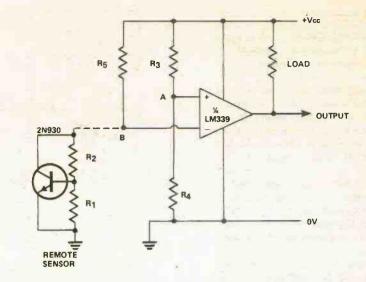
#### Temperature Sensor, Remote

The circuit shows a temperature sensing device which can be used to indicate at a remote point when the temperature passes through a certain value or to give an alarm when this occurs.

The sensing unit itself contains a 2N930 transistor. The base-emitter voltage of this device appears across R1 and (as the base current is far less than the collector current) the voltage at the upper end of R2 will be the emitter-base voltage multiplied by (R2 + R1)/R1. The base-emitter voltage changes with a temperature coefficient of -2.2mV/OC and this change is multiplied by the same factor before being applied to the LM339 circuit.

The potential at point A is set by the resistors R3 and R4. As the temperature of the sensor transistor rises, the voltage at point B falls. At the time this voltage falls below that at point A, the output of the LM339 voltage comparator will go 'high'. If, however, the input connections to the LM339 are reversed, the output will go 'low' when the temperature of the sensor falls below the preset point.

The LM339 contains four separate voltage comparators in one package; only one of these comparators is used in the circuit shown. The other three comparators could be used with



another three temperature sensing transistors so that an indication is given when the temperature passes through three other preset values.

The value of R5 should be chosen so that the current passing through the remote sensor unit is about  $10\mu$ A. If the temperature range over which operation is required is narrow, the ratio R2/R1 may be large so that the system is very sensitive to small temperature variations. A potentiometer may be substituted for R3 and R4 so that the temperature at which the comparator switches is variable. The voltage at point B is highly linear over a very wide temperature range (about -65°C to +150°C) and therefore the potentiometer which replaces R3 and R4 can be given a linear calibration.

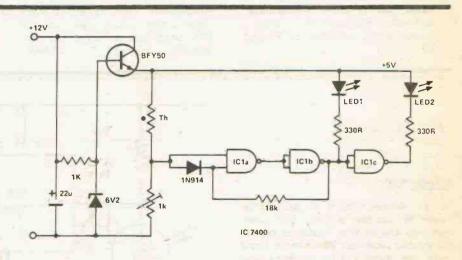
A feedback resistor may be connected from the output to the noninverting input to provide a small amount of hysteresis (so that the temperature at which the output changes when the temperature is rising is different from that when it is falling); one then has the basis of a thermostat.

The output current has a maximum value of about 15mA.

### Warmth Indicator

A simple indicator was required for a gas fridge in a caravan to show when the pilot light had gone out. The sensing element used was a thermistor, attached to the outlet which is 'warm' when the pilot light is on. A rod-type thermistor was used for cheapness, with a resistance of about 3k at 20° C.

Two gates of the 7400 provide a Schmitt trigger with a low hysterysis (determined by the 18k feedback resistor) and the third gate inverts that output. When the pilot light is on, the input of IC1a is high, IC1c output is logic 0 and LED2 (green) is on. If the pilot light fails, the



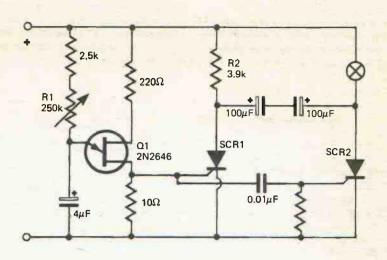
temperature falls, all gates change state, LED2 goes off and LED1 (red) comes on.

The temperature at which the changeover takes place is set by the 1k preset.

# INDICATORS

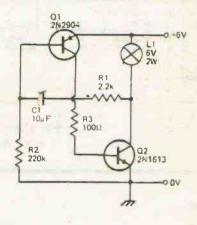
### Warning Flasher

This circuit will operate reliably from noisy or fluctuating power supplies and unlike many multivibrator circuits - is inherently self-starting when power is applied. In this circuit unijunction transistor Q1 is used as a relaxation oscillator supplying -a continuous train of pulses to the gates of the SCRs. Assume that SCR2 has been triggered into conduction and that lamp 2 is energized. The next trigger pulse from Q1 triggers SCR1, this discharges C2 and the resultant commutation pulse turns off SCR2. The resistor R2 in the anode of SCR1 is of a value high enough to prevent SCR1 from latching on. SCR2 is retriggered by the next triggering pulse from Q1. Using the component values shown, the flash rate of this circuit is adjustable - by R2 - from 35 to 150 flashes a minute.



#### Transistorised Flasher

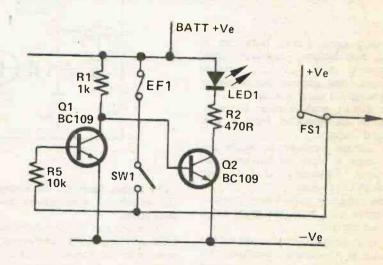
This simple circuit will flash a 6 volt lamp at a rate determined by the size of capacitor C1. It is most economical on power as it only draws current when the lamp is ON. When the lamp is OFF both transistors are biased OFF.



#### **Blown Fuse Indicator**

Base current for Q1 is taken from the 'earthy' side of FS1. Q1 will conduct its collector voltage falling to zero. Q2 base will also be zero, switching LED 1 off.

If FS1 were to 'blow' or cease to exist, depart for its maker, have a rest, go to sleep, peg out, become inoperative, deceased, out of order, or duff, kick the bucket, bite the dust, pass away, self destruct, become no longer intact, or cease to conduct in any way, due to war, flood, corrosion or act of God etc., Q1 would switch off, causing its collector to rise to 12 V, switching Q2 and LED 1 on. R2 is the current limit resistor for LED 1. SW1 will bypass FS1 via emergency fuse 1, until FS1 can be replaced.



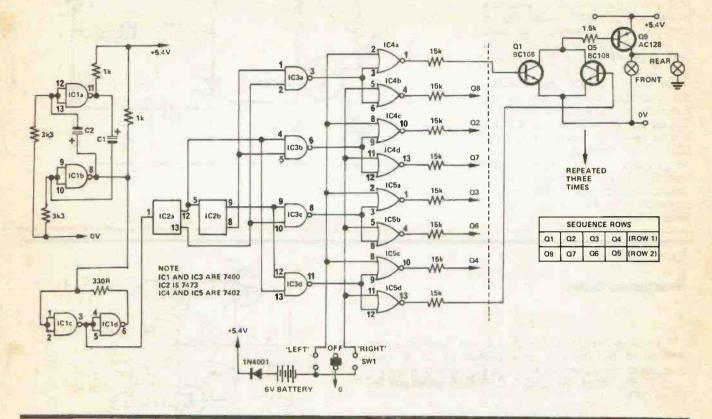
## INDICATORS

### **Novel Indicators**

Since a bicycle has no effective width, normal indicator lamps placed on each side do not give a clear indication of direction when seen from a distance,

#### especially at night.

The circuit shown is a four stage ring counter which sequentially drives four yellow lamps giving an impression of movement i.e. towards the left or right. Lamp sequencing rate can be altered by changing C1 and C2. (50uF was found to be about right). Oscillator pulses are shaped by schmitt trigger IC1b. The decoding and output gating are performed by ICs 3, 4, and 5. Driver transistors Q1 to Q8 can be any low current, medium gain NPN silicon.



**Neon Tube Flasher** 

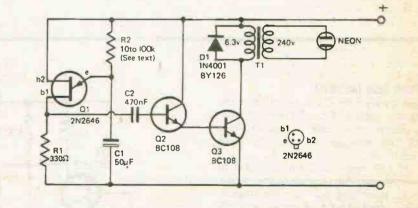
Flashing neon globes have use in many applications, however their relatively high working voltage precludes their general use where a mains supply is not available.

This circuit enables neon tubes cr bulbs to be operated from a low voltage dc supply.

The voltage required to ignite the neon tube is obtained by using an ordinary filament transformer (240-6.3V) in reverse.

Battery drain is quite low – being in the region of 1 to 2 milliamps for a nine volt battery.

Q1 is a unijunction transistor and operates as a relaxation oscillator. Its frequency of operation is determined by R2-C1.



The pulses from Q1 are directed to Q2 which in turn drives Q3 into saturation.

The sharp rise in current through the 6.3V winding of the transformer as Q3 goes into saturation induces a high voltage in the secondary winding causing the neon to flash.

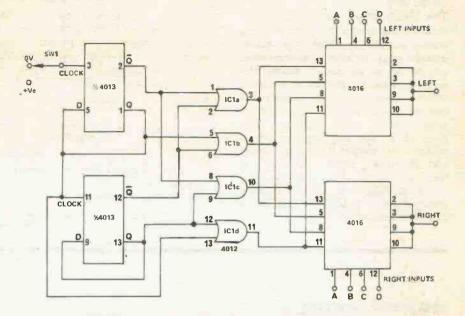
The diode D1 protects the transistor from high voltage spikes generated when switching currents in the transformer.

### Stereo Input Selector

Four different inputs can be switched through by the continual pressing of SW1.

IC1 is a dual 'D' type flip flop. The Q outputs are connected to the D inputs so that the clock inputs are divided by two. The two flip flops are connected in series, giving a two-stage binary counter.

IC2 is a quad AND gate. This is used to decode the four states of the counter. The outputs are used to control the quad switches at IC3 and IC4 (4016AE).

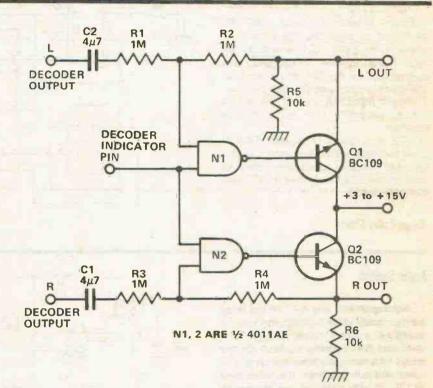


## Stereo Switch, Simple

A device to switch the audio from a stereo tuner only when a stereo signal is being received.

Two CMOS NAND gates and two transistors are employed. One of the inputs from each gate is connected together and to the indicator output of the decoder IC.

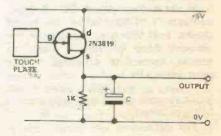
The other gate inputs are connected to the emitter's of Q1 and Q2 respectively, by means of the feedback resistors R2 and R4. On reception of a stereo signal the indicator output of the decoder goes high and the feedback resistors' bias the gates into the linear region passing the signal. On reception of a monosignal or interstation noise, no signals pass through the gates, the circuit providing a mute function.



### Logic Touch Switch

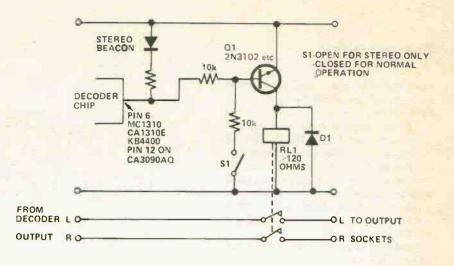
An n-channel field-effect transistor is the basis of this simple trigger. In its quiescent state the voltage at the output is about 3V. When the plate is briefly touched with a finger, the minute currents between the body and the plate alter the electric field at the gate of the transistor. The effect is to cause a drop in output voltage. It falls almost to zero and can be used to trigger a TTL flip-flop. This can be constructed in the usual way, using two NAND gates from a 7400 IC. If several triggering circuits are required, it is more convenient to use the 74118 sextuple bistable latch.

The value of the capacitor is inot critical, but 10uF is convenient. The touch-plate can be the second copper etched an a circuit-board, a square of aluminium foil, or simply a drawingpin pressed into an insulating support.



## Stereo Only

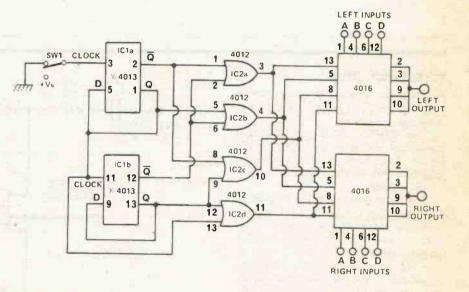
This circuit allows only stereo broadcasts to be outputed by a tuner using either a 1310 or 3090 type stereo decoder chip. In both cases the stereo beacon driver is used to switch the audio output of the tuner. When a stereo signal is being received the beacon driver output is low which turns the Q1 and energises reed relay RL1. The two contacts which switch the output lines are closed and the stereo signal is available at the tuner output sockets. RL1 can be any reed relay with a coil resistance greater than 120 ohms and two normally open contacts.



## Input Selector, Sequencing

Four different inputs can be switched through by the continual pressing of SW1. IC1 is a dual 'D' type flip flop. The Q outputs are connected to the D inputs so that the clock inputs are divided by two. The two flip-flops are connected in series, giving a two stage binary counter.

IC2 is a quad OR gate. This is used to decode the four states of the counter. The outputs are used to control the quad switches of IC3 and IC4 (4016AE).

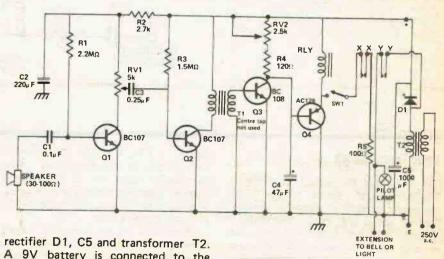


#### **Audio Switch**

Contacts X-X and Y-Y of the relay are normally open. When the relay is energised, current flows through SW1, X-X and R5, thereby locking on the relay. At the same time contacts Y-Y close and current from the secondary of T2 is available at the extension lead sockets, to operate the remote bell or lamp.

If the lock-on switch SW1 is open, contacts Y-Y open when the sound ceases, and this is satisfactory if the warning lamp or bell is likely to receive immediate attention. The pilot lamp LP1 is of aid when setting the unit, as with SW1 open it will show at what sound level operation is being obtained.

For occasional use battery operation is possible by omitting the silicon



rectifier D1, C5 and transformer T2. A 9V battery is connected to the positive and negative points shown, with an on-off switch in circuit. Quiescent current is about 6mA,

which is not very heavy and will allow a long period of working from a PP9 or similar battery.

680R

BC169C

5V1 ZENER

+9.V

OC

0V

0

### **Touch Switch, Thermo**

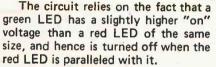
The following touch switch works on the temperature dependence of the forward voltage of silicon diodes. At 0 C this is about 650mV, but drops by 2mV per C increase in temperature.

When a finger is placed on D3 and D4 the voltage at A will drop below that at B and the O/P of the Op-Amp will go high, causing a TTL compatible pulse to appear at C. D1 and D2 provide compensation against ambient temperature changes. VR1 is initially set so that VA is greater than VB by about 10mV.

The system has the intrinsic advantage that it may be used in moisture-prone conditions in which ordinary touch switches would be most unsatisfactory due to their principle of operation.

### **LED** Changeover Circuit

This configuration allows a green LED to be turned off and a red LED turned on by the operation of one 'make" contact only, thus simplifying the design of circuitry to indicate, for example, safe/unsafe or standby/on states.



5k1

100k

R

RV1

5k6

10k

741

100k

10k

100n

114

1N914

1N914

1N914

1N914

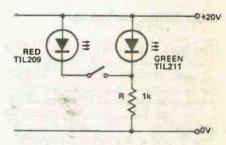
D1

D2

D3

D4

For the diode types shown, R should be chosen to give a current drain of about 20mA from the chosen supply rail voltage.



LOAD

1k

0

O +V

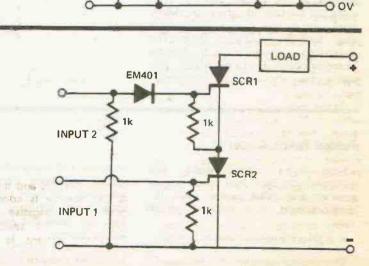
INPUT 2

## **OR Gate. SCR**

An 'OR' gate, again using C106s, is shown. Here, an input to either 1 or 2 will energize the load.



rigure shows how a pair of C106s may be used as an 'AND' circuit capable of switching up to four amps. In this circuit, unless inputs 1 and 2 occur simultaneously, no voltage can exist across the load.



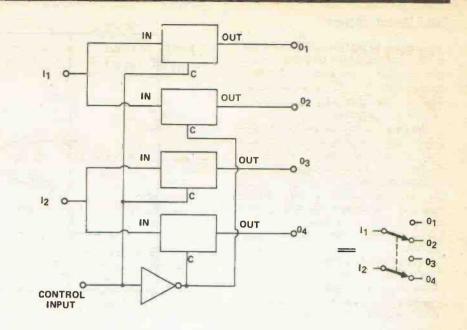
> 1k

INPUT 1

0

## **4016 DPDT Switch**

It should be appreciated that the output impedance of the switch is fairly high and so for low signal distortion, a load greater than  $10k\Omega$  is necessary. Using a high supply voltage (10-15V) also helps to achieve this end. The gates will pass signals above the 10MHz mark but as the frequency becomes higher, crosstalk between the switches and distortion will inveitably increase.

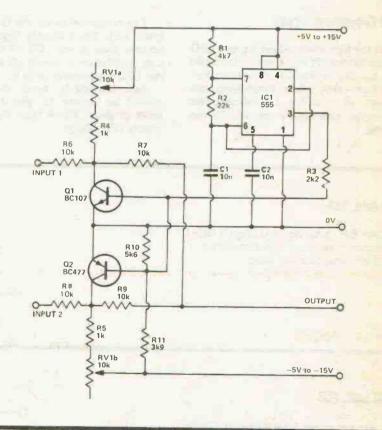


#### Beam Splitter, Oscilloscope

The basis of the beam splitter is a 555 timer connected as an astable multivibrator, components R1, R2 and C1 being selected to give approximately equal high/low pulses of about 3 kHz.

Resistor R3 couples the output of the oscillator to the npn/pnp pair Q1 and Q2. When the output of the oscillator is low, resistors R10 and R11 allow Q2 to be on so that any signal applied to input 2 is effectively shortcircuited via resistor R8 to the common line of the power supply. At the same time, the npn transistor Q1 is off, so that any signal at input 1, plus a positive voltage provided by RV1a and R4, appears at the output via R7.

Conversely, when the output of the oscillator is high, Q1 is biased on whilst Q2 is off. A signal at input 2 plus a negative voltage via RV1b and R5 appears at the output via R9. Thus signals at the two inputs are alternately displayed on the oscilloscope with a clear separation between them. The separation is controlled by the tandem potentiometer RV1a/b which also varies the amplitude of the traces.



#### **Twilight Switch, Automatic**

Here is a circuit which will automatically light your porch light or activate any other device when the ambient light drops below a certain level.

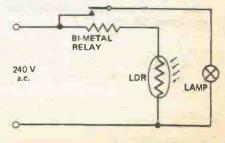
A light dependent resistor is used in series with a relay.

The resistor has a value in excess of 1 megohm when illuminated, this drops

to below 110 ohms when dark.

It is important that the LDR be positioned in such a place as not to receive any spurious illumination as this will cause the relay to drop out intermittently.

A bimetallic strip type relay will give sufficient delay to ensure that incident light flashes have no influence.



## SEQUENCE & TIMING

#### **Time Delay Switch**

IC1a is provided with resistive and capacitive feedback to form an integrator with initial conditions. IC1b is in an ''open loop" mode so that its output is either high or low depending on its inputs, and changes state when the output of IC1a goes more negative than the voltage set at ZD2. When the output of IC1b goes positive the transistor Q1 biases hard on switching the SCR on. Diodes D1-D4 are to make the SCR conduct on both halves of the mains wave form

The delay period is set by the components ZD1, ZD2; C, RV1, and

R. If ZD1 is chosen to be OV5 and ZD2 at 5V, then the maximum delay period is given by T = 10.C.R.

$$RV1 = \frac{ZD2}{ZD1} \times R \le 10.F$$

The meter is a voltmeter with a fsd equal to the value of ZD2. The switch then operates when the meter reaches fsd. The meter can therefore be calibrated to show remaining delay with OV equal to T and fsd equal to zero.

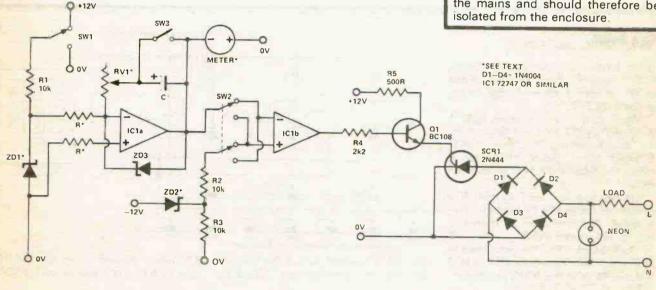
SW2 changes round the inputs of the op-amp so that the output either swings from high to low, or, low to high. SW3 is to reset the time delay which it does by discharging the capacitor. ZD3 should be chosen

to be a value slightly higher than ZD2, this is to stop the capacitor charging beyond a set limit and therefore overloading the meter. SW1 is the run-hold switch. When the switch is at +12 volts the integrator charges the capacitor. When the switch is set to OV the charging of the capacitor is stopped until the switch is set back to 12 volts

Q1 is a buffer to avoid loading on the IC and to trigger the SCR. The supply voltage should be 12-0-12 and does not need to be well smoothed as the zener diodes set the timing function.

### Warning

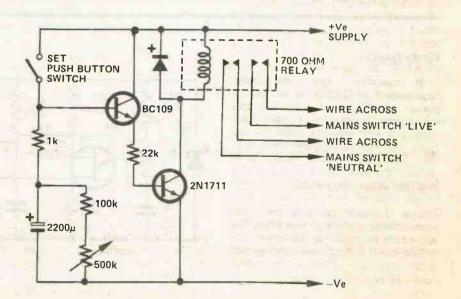
The circuitry is not isolated from the mains and should therefore be



## **Snooze Delay Unit**

When the Set switch is depressed the large electrolytic capacitor is charged via the limiting resistor (1k). This charge causes the BC109 to conduct which supplies enough base current to switch on the 2N1711 space and operate the relay. The relay contacts are wired in parallel with the mains switch so that if the mains switch is now turned off, the equipment will continue

The supply voltage is taken from the equipment in which the unit is fitted and will determine the choice of relay. The maximum delay being 1.75 hours.

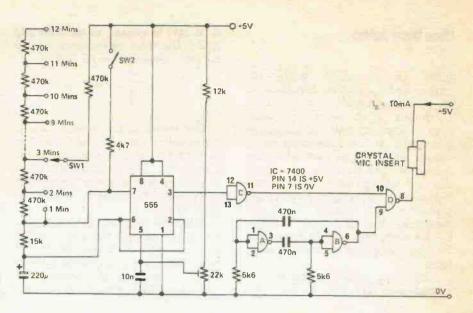


## SEQUENCE & TIMING

## Timer, 1-12 Minutes

The circuit is centred around the NE555V timer which provides a logic 0 level at pin 3 every 1 - 12 minutes, depending upon the position of the 12 way switch (SW1). SW2 is a pushbutton switch which synchronises the first pulse (originally a switch circuit was fitted to the reset pin, 4, but the first timing period was never the same as the subsequent periods). The variable 22k resistor allows a degree of fine adjustment for the timing period.

Gates A and B form a tone generator. Gate C inverts the output of the NE555V so that a logic '1' is fed to gate D at the end of each timing period. Thus a tone burst of a few seconds is produced by the transducer (any surplus crystal microphone insert should be suitable).



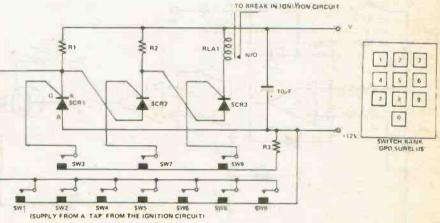
## **Code Switch**

When button 3 is pressed R3 'Gates' SCR 1, which remains on with a load of R1. It also supplies voltage to the anode of SCR 2.

When button 7 is pressed SCR 2 is 'Gated' by R3 also, and held on by R2, thus supplying the anode of SCR' 3, which when 'Gated' by button 9 closes the relay and makes an external circuit.

It can also be used to switch a circuit off depending on how the relay is wired. This would be an advantage in a home intruder alarm.

Components: The Thyristors can be any type and values for R1 and 2 selected to hold the SCR's in conduct-

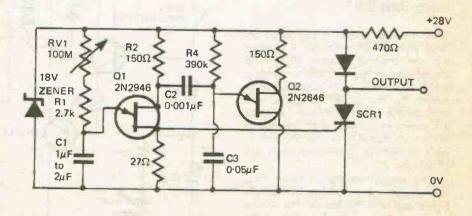


ion. R3 is selected to suit the thyristors. The remaining buttons, 1,2,4,5,6,

8,0 when pressed short out SCR1, thus switching off any following SCR.

#### **Timing Circuit**

In operation, the peak point requirement of UJT Q1 is reduced to about 1/1000 of its normal requirement by pulsing its upper base with a ¾ volt negative pulse derived from the free running oscillator UJT Q2. This regular pulse momentarily reduces the peak point voltage of Q1 and thus allows the peak point current to be supplied from C1 rather than R1, as it would be with the more conventional circuits of this type. The pulse rate of oscillator Q2 is not very critical but it should have a period that is less than one fiftieth of the overall time delay.



## SEQUENCE & TIMING

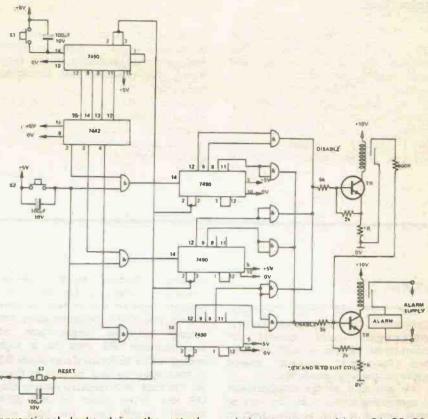
### **Combination Lock**

The circuit and switching system is simplified by the use of a multiplex system. S1 inputs pulses to the decade counter 7490. The resulting BCD is decoded by the 7442. It is the decimal output of this which carries out the multiplexing via the AND-gates.

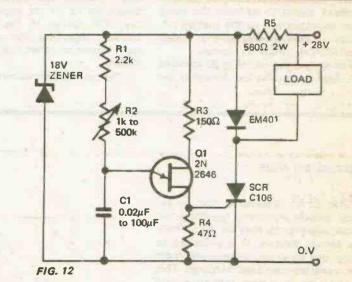
S2 inputs pulses which are transferred to the other 7490 decade counters by the AND-gate multiplex system. The BCD output from the 7490's is taken to the AND-gates whose outputs control the Alarm 'Disable' and 'Enable' switch system.

The 'Disable' function effectively prevents TR2 from being biased on and hence prevents the 'Enable' Reed relay from working.

This circuit has several advantages over conventional electronuc combination locks as only two switches need be installed on the object to be guarded, regardless of the number of figures in the combination. The value of the example combination is 314. The alarm is triggered if any of these digits is exceeded in value. While the circuit is capable of directly driving an actuator it is recommended that it is only used to disable an alarm system —



conventional locks doing the actual locking. (To operate the example the



and accurate, repeatable timing is required — some provision must be made to ensure that C1 is discharged to zero before each timing sequence. This can most easily be done by interconnecting a pair of switch contacts with the reset system so as to momentarily short out C1 whenever the circuit is reset.

Temperature compensation for this circuit is provided by R3. Increasing the value of this resistor causes the circuit to have a positive temperature coefficient. It is possible to obtain zero coefficient over a small range of ambient temperatures by optimizing R3.

## **Flexible Timer**

The precision time delay circuit shown will provide accurate and repeatable time delays adjustable from a few milliseconds to a minute or two. This is a very flexible circuit in which the operating cur nt and voltage depends only on the choice of SCR.

The timing sequence may be initiated either by applying power to the circuit – or by opening a shorting switch wired across C1. Timing capacitor C1 is charged via R1 and R2 until the voltage across C1 reaches the peak point voltage of the UJT Q1. When this occurs, Q1 fires, generating a pulse across R4, triggering the SCR, and applying power to the load. Holding current for the SCR is provided via R5 and D1.

The circuit is reset by momentarily removing the supply voltage.

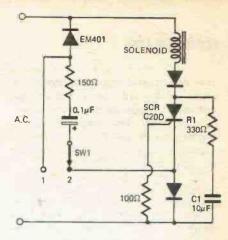
If the circuit is to be used in an application where both rapid cycling

# POWER CONTROL

## Impulse Power

This circuit is often used in electrically powered stapling machines, impulse hammers etc, and causes load current to flow through the load for one complete half-cycle of the ac supply whenever SW1 is actuated (i.e. moved from its normal position (1) to energise-load position (2)). The circuit is arranged so that the SCR is always triggered at the beginning of a positive half-cycle of the ac supply, even though the switch may be closed randomly at any timeduring the previous two preceding half-cycles.

Resistor R1 and capacitor C1 should be chosen so that their series combination supplies just sufficient holding current for the SCR for one complete half-cycle.



#### Half-Wave Control

One of the most common applications for SCR phase control systems is speed control of commutator motors – such as those used for food mixers, sewing machines, pottery wheels etc.

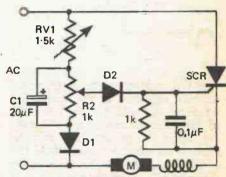
However one of the disadvantages of controlling motor speed by varying input power is that as the effective power input is reduced to slow down the motor – the torque available is reduced as well.

This may be overcome by using a feedback signal to advance the firing angle in proportion to the load on the motor — thus increasing the power input if more torque is required.

The circuit shown in Fig 20 achieves this load compensating function by

deriving a feedback signal from the armature back-emf (produced by the residual field of the motor). In this circuit, the SCR is triggered when the voltage on the wiper arm of potentiometer R2 rises to a high enough value to forward bias diode D2 - thus allowing gate current to flow. As the back emf tends to reverse bias D2, the firing point of the SCR depends largely upon the back emf and this in turn is a function of speed. If the motor is loaded, the speed reduces, thus also reducing the back emf - hence D2 becomes forward biased earlier in the cycle (triggering the SCR earlier in the cycle), and thereby supplying the motor with more power to offset the effect of the loading.

The component values shown are

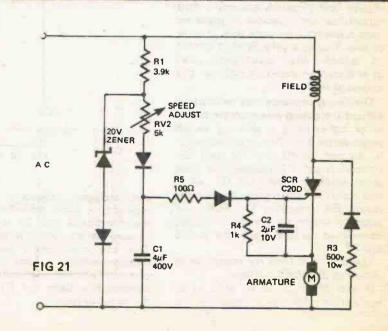


suitable for most fractional horsepower motors — for optimum results it will be necessary to adjust component values to suit the motor used.

The circuit described above will provide stepless speed control over a wide range of motor speed — but tends to cause jerky operation at low speeds.

#### improved Half-Wave

The above drawbacks can be almost entirely overcome by using the circuit shown. As may be seen from the circuit diagram, it is necessary to bring out separate connections from the armature and field windings. This is generally a simple operation and providing it can be done the circuit will provide stepless speed control down to virtual standstill. In this circuit the 20V zener diode provides a constant voltage for the discharge of C1. Capacitor C2 and resistor R4 are connected from gate to cathode of the SCR to stabilize the circuit by preventing the SCR from being triggered by extraneous signals.

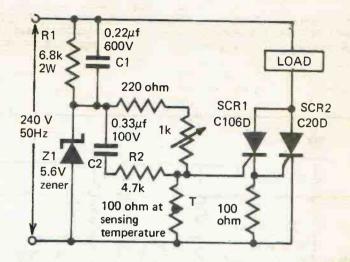


#### Zero Switching

A very simple yet effective zero voltage switching provides halfwave control only, but is satisfactory for commercial applications where the heating elements can be designed to suit.

The circuit is extremely stable and unaffected by quite large variations in line voltage and ambient temperature. The response time depends upon the characteristics of the thermistor which is used – times of one to two seconds are typical. The sensing differential is around  $\chi^0F$  at normal ambient temperature.

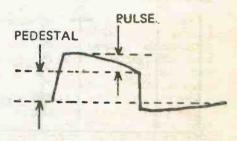
The Zener diode Z1 forms a voltage pedestal of 5.6 volts nominal amplitude by clipping the incoming positive half-cycle of mains voltage. This pedestal is differentiated by R2. C2 and associated resistors to form a pedestal of reduced amplitude with a pulse superimposed on top of the pedestal. This waveform is applied to the gate of SCR1. The capacitor C1, which is connected in parallel with R1, provides a leading phase shift to the pedestal so that SCR1 is triggered into conduction by the peak of the positive decaying pulse which is superimposed on the pedestal. It does this at the beginning of the positive going half-cycle



of line voltage appearing at the anodes of both SCRs.

The thermistor controls the amplitude of the pedestal and thus provides a semi-proportional control with a small temperature differential.

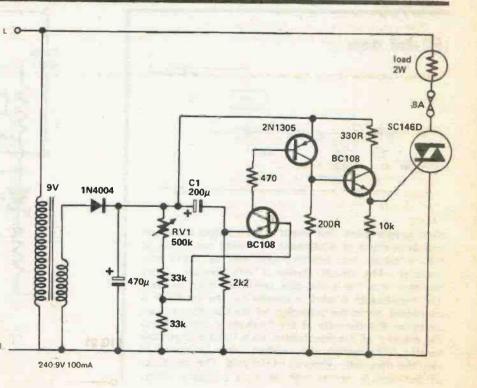
The lock-in configuration of SCR1 and SCR2 reduces the effects of ambient temperature variations. The cost of this circuit is very low compared to a phase control circuit of the same power handling capacity as no rfi components are required.



## **Triac Lamp Flasher**

The circuit is a relatively simple triac lamp flasher, probably of most interest to those in the disco business. The flasher will handle a load of up to 2kW with a variable flash rate of about 20/ 200 flashes per minute, achieved by altering the value of RV1.

C1, the timing capacitor, can be experimented with to obtain the most satisfactory results. Even though little power is dissipated in the triac (15W on full load), it should be mounted on a heatsink.

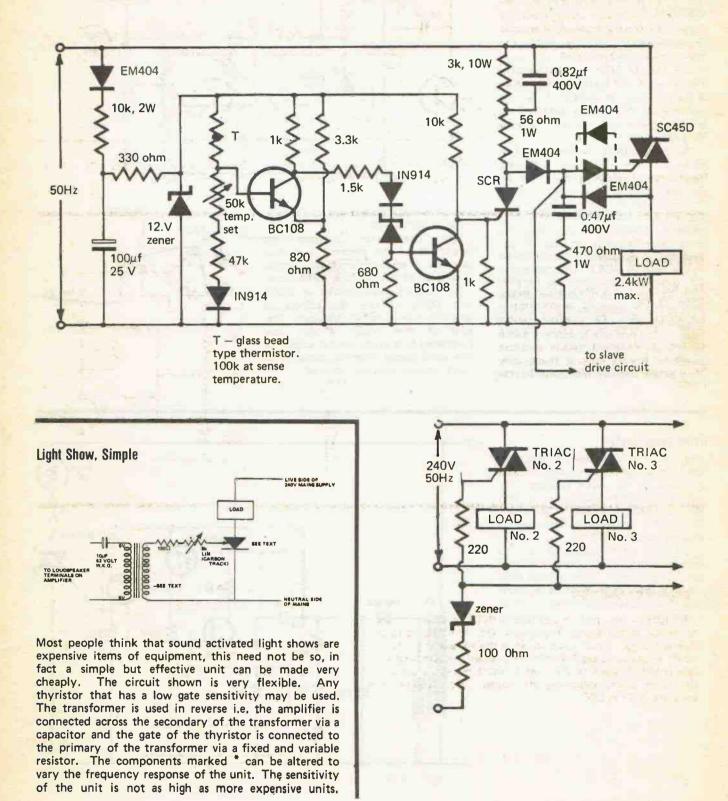


# -POWER CONTROL-

## POWER CONTROL.

### **Triac Slave Controller**

The circuit shown will provide full-wave control of heating loads of almost any size. The triggering circuit will drive Triacs of any size from 1 amp up to 125 amps. In addition almost any number of additional Triacs can be slave driven by the main triggering circuit. The differential of this circuit is approximately  $\pm$  1/6°C. This circuit has a semi-proportional action, and is suitable for applications where large amounts of power have to be controlled accurately and at low cost.



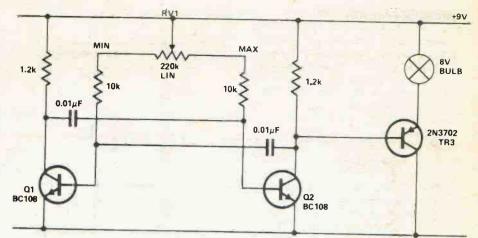
## POWER CONTROL

## DC Lamp Intensity

A simple and inexpensive unit for reducing the brilliance of a lamp and at the same time reducing the current drain, thus increasing battery life considerably. A power saving does not happen by merely inserting a resistor in series with the bulb, hence the reason for the above circuit.

Q1 and Q2 form an astable multivibrator, the RV1 varying the mark/ space ratio. The output from Q2 collector is fed to Q3 base, either satuating Q3 or turning it off. Varying the mark/space of the lamp.

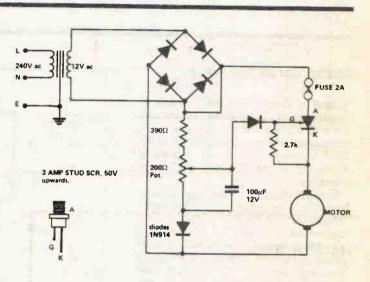
A notable point is that as Q3 is either fully 'on' or 'off' it need not be a high wattage type. As an



- example, when Q3 is satuated, Vce = 0.3V approx, and the lamp current is
- 0.2A the power across Q3 is  $W = V \times 1$ = 0.3 x 0.2 = 0.06.

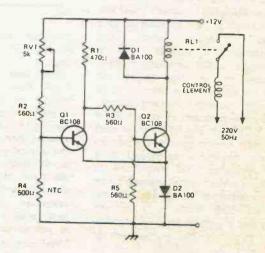
## Train Speed Control

The following is a low voltage adaptation of the type of speed control popularly used to regulate power drills. It gives very good starting torque and excellent speed regulation of the model. A reversing switch may be incorporated in the leads to the motor.



## **Temperature Controller**

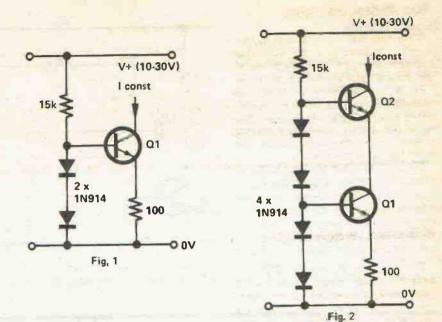
A negative temperature coefficient (NTC) resistor is used to sense temperature. Transistors Q1 and Q2 form a Schmitt trigger which switches when the voltage at the base of Q1 increases above 1.4 volts. Thus when the temperature falls below that set by RV1 the Schmitt changes state and the relay opens switching the heater 'ON'. Regulation accuracy is 1° to 2°C.



## **Current Source, Drift Free**

The conventional type of constantcurrent source, as shown in Fig.1, will drift in output current immediately after switch-on. This is because of the voltage drop across Q1, causing a significant amount of power to be dissipated in the transistor, heating it and its Vbe. Hence the output current slowly increases after switch-on, typically reaching a stable value about two minutes later. In tests the current increased by about 4% for a small signal transistor dissipating 100mW.

This effect is greatly reduced by the configuration shown in Fig.2, which fixes the voltage across Q1 at a very low level by virtue of the commonbase transistor Q2. The main voltage drop occurs across Q2, leaving about 600 mV across Q1, this being set up by the two extra diodes in the bias chain, (D1, D2) which fix the emitter potential of Q2.



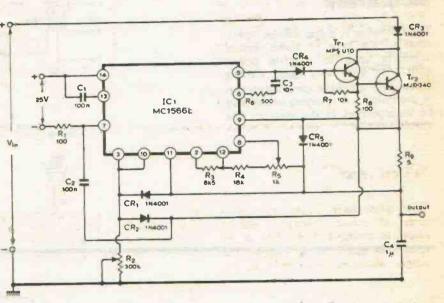
### **Constant Current, High Voltage**

WHEN a constant current source is required and the various advantages offered by the use of IC's are to be exploited, an input voltage limit of 40 or, possibly, 50 V is normally necessary if the IC's are not to be damaged.

Neil Wellenstein, an applications engineer working Motorola's Phoenix, Arizona, laboratories, discovered a means of obtaining a variable constant current supply with input voltages as high as 750 V using a standard regulator IC. In fact, the input voltage is limited only by the breakdown voltage of the series pass transistors employed.

The IC used by Wellenstein was the Motorola MC1566L which has the ability to "float" on its own output However, when used voltage. conventionally, a voltage sensitive error occurs in the constant current mode and this is large enough to prevent the device from being used as a precision constant current source, Normally the constant current feature of the MC1566L would only be used to provide short circuit protection when the device is employed as a voltage regulator. The magnitude of the current error is small enough to be of no consequence in this application.

The MC1566 contains a current sensing and a voltage sensing amplifier which "float" on the output voltage and which are supplied from an on-chip regulator. The on-chip



regulator receives its input from an auxiliary 25 V supply external to the chip.

When used conventionally a constant 1 mA flows from pin 3 through a resistor to ground to establish the reference voltage for the voltage sensing amplifier. The error voltage appears between pins 8 and 9. When the device goes into the current limit mode (short circuit conditions) part of the 1 mA output from pin 6 can flow through a diode to pin 9 thereby upsetting the error voltage and producing a voltage sensitive gutput current error.

Wellenstein discovered by reversing the roles of the voltage and the current

sensitive amplifiers, he could eliminate this problem altogether. The net effect is that any portion of the reference current that appears in the load must pass through the current sensing resistor (R9) which cannot be bypassed as was previously the case.

The maximum input voltage to the circuit is limited by the series-pass transistor. In the case of the MJE340 shown, the maximum input voltage is 300 V. The circuit provides a constant current output which is adjustable from 200  $\mu$ A to 100 mA; above 10 mA take care not to exceed the ratings of the MJE340. At both the 200  $\mu$ A and the 1 mA settings, output impedance exceeds 20 M ohms.

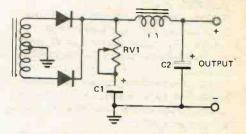
## Output Voltage, Adjustment

When the output voltage of a power supply comes out a little higher than expected it can be adjusted by making the simple addition illustrated above. R1 is a 500 ohm or 1000 ohm potentiometer (10 watt rating) inserted in series with the input filter capacitor. Adjust it to give the correct

### voltage under load.

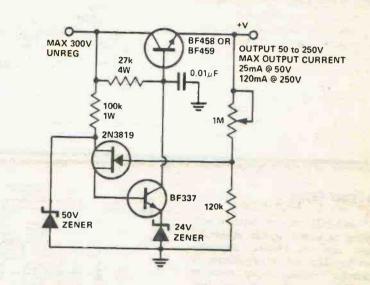
For low voltage supplies (i.e. up to 50 V or so) a 50 ohm or 100 ohm pot might be more suitable.

The pot could be connected between the negative lead of C1 and ground and would not then need to be insulated.



## High Voltage, Variable Regulator

This regulator is ideal for SSB linear amplifier tube screens. It would also have application in the repeller supply for a reflex-klystron microwave oscillator. CRO deflection amplifier supply is another possible application. Regulation is about 0.5%. The output transistor will need to be mounted on a small, insulated heatsink. A BF459 is preferred (30V Vceo) as the BF458 is sailing a bit close to the wind when the output is



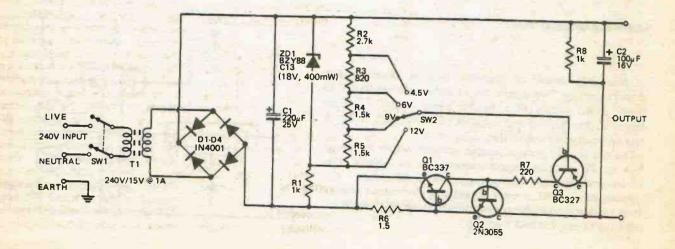
### Switched Output

down to 50 V.

THIS little power supply provides a range of switch selectable output regulated voltages from 4.5 to 12 volts, selectable by a switch. The supply will provide up to 400 mA

and the output can withstand a short circuit without damage. It is therefore ideal for the experimenter or for use with high drain appliances.

Nominal output voltage 12V, 9V, 6V and 4.5V Output current 0 – 400mA Current limit approx. 500mA



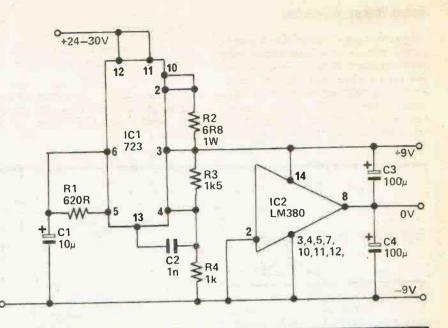
### **Dual PSU**

Anyone who experiments with opamps will need a dual stabilised power supply. The circuit shown was designed to power up to twenty 741s simultaneously.

IC 1 is used to provide an output voltage of 18 V at pin 10. R2 sets the short circuit current at 100 mA and should be rated at 1 W.

IC 2 is used as a precision short circuit proof voltage divider.

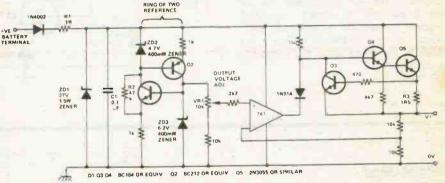
A 9.0.9 V supply has been found in practise to cater for most op-amps with the notable exception of the CA3130 which has a maximum supply rating of 16 V.



### **Mobile Power Supply**

R1, C1 and ZD1 provide clipping and smoothing of supply spikes, while D1 protects against reverse polarity connection. The reference voltage is provided by the ring-of-two, since in this configuration the zeners bias constant-current sources for each other, the output across ZD3 is almost totally independent of supply variations. R2 ensures the ring starts reliably.

A set fraction of the reference voltage is applied, via VR1, to the 741, which in conjunction with current amplifiers Q4, Q5 forms a negative feedback loop to maintain the output voltage constant. It may be set



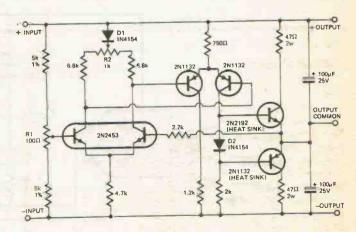
between 10 and 6 volts, so, for instance, most battery cassette equipment may be driven. Short circuit protection is provided by Q3; when the output current exceeds 400mA sufficient voltage is dropped across R3 to turn on Q3, which shunts drive away from the base of Q4 and hence prevents the output current from rising further.

#### **Converting Single to Dual**

Operational amplifier circuitry requires double-ended power supplies. This simple circuit converts a conventional single ended supply to a double ended operation. Once adjusted, the positive and negative rails will track within a few millivolts without further adjustment.

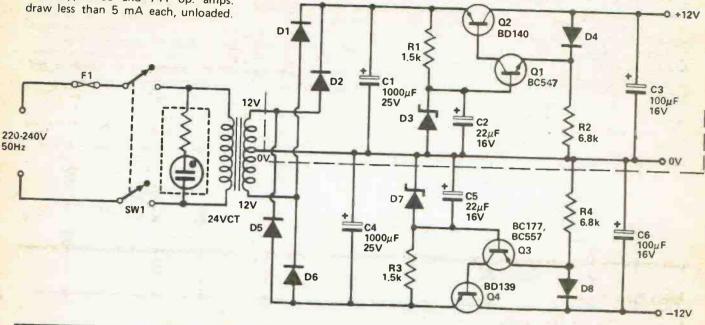
The circuit will provide output voltages within the range five to 25 volts at output currents up to 100mn. The corresponding supply voltage range is 10 to 50 volts.

Potentiometer R1 is used to balance the output voltage (test by precision divider network) and potentiometer R2 is adjusted to provide best tracking.



## **Op-Amp Supply**

The rated output, of 100 mA from either side, will be found to be more than adequate for the intended use, since type 709 and 741 op. amps. draw less than 5 mA each unloaded

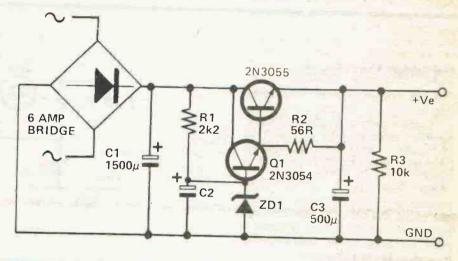


## Low Ripple PSU

The power supply circuit shown may be used where a high current is required with a low ripple voltage (such as in a high powered class AB amplifier when high quality reproduction is necessary).

Q1, Q2 and R2 may be regarded as a power darlington transistor. ZD1 and R1 provide a reference voltage at the base of Q1. ZD1 should be chosen thus: ZD1 = Vout -1.2.

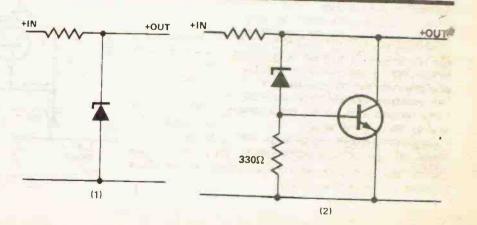
C2 can be chosen for the degree of 'smoothness' as its value is effectively multiplied by the combined gains of Q1/Q2, if 100 $\mu$ F is chosen for C2, assuming minimum hfe for Q1 and Q2, C= 100 x 15(Q1) x 25(Q2)= 37,000  $\mu$ F.



## Zener Assistance

The simple zener shunt of diagram (1) may not handle sufficient current if the zener available is of low wattage. A power transistor will do most of the work for the zener in circuit (2).

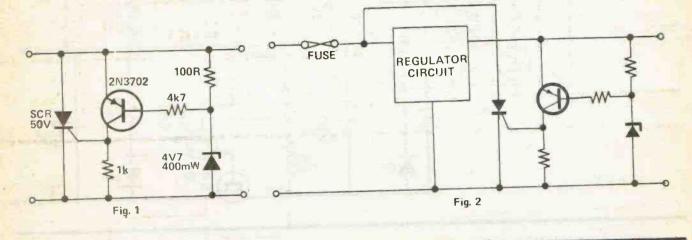
The output voltage is increased by 0.7V but it is stabilisation rather than exact voltage which is often required.



#### Crowbar, Simple

This circuit provides overvoltage protection in case of voltage regulator failure or application of an external voltage. It is intended to be used with a supply offering some form of short circuit protection, either foldback, current limiting or simple fuse. The circuit is less effective in the latter case however, as a good deal of damage can be done in the time taken to blow a fuse. The most likely application is a 5V logic supply, since TTL is easily damaged by excess voltage. The values chosen in Fig.1 are for a 5V supply, although any supply up to about 25V can be protected by simply choosing the appropriate zener diode. When the supply voltage exceeds the zener voltage +0.7V, the transistor turns on and fires the thyristor. This shorts out the supply, and prevents the voltage rising any further. In the case of a supply with only fuse protection, it is better to connect the thyristor across the unregulated supply as shown in Fig.2 to prevent damage to the regulator circuit when the crowbar operates.

The thyristor should have a current rating about twice the expected short circuit current and a maximum voltage greater than the supply voltage. The circuit can be reset by either switching off the supply, or by breaking the thyristor circuit with a switch.



## Low Voltage, Short Protection

These shart circuit protected stabilisers give 6, 7.5 and 9 V from an automobile battery supply of 13.5 V nominal, however, they will function just as well if connected to a smoothed dc output from a transformer/rectifier circuit.

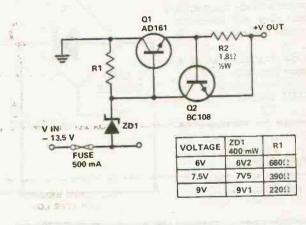
Two types are shown for both positive and negative earth systems. The power transistors in each case can be mounted on the heatsink without a mica insulating spacer thus allowing for greater cooling efficiency.

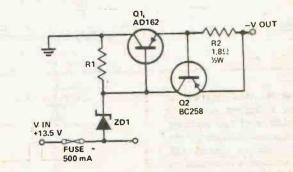
Both circuits are protected against overload or short-circuits.

The current cannot exceed a value of 330 mA. Under normal operating conditions the voltage across R2 does not rise above the 500 mV necessary to turn Q2 on and the circuit behaves as if there was only Q1 present.

If excessive current is drawn, Q2 turns on and cuts off Q1 protecting the regulating transistor.

The accompanying table gives the values of R1 for different zener voltages.



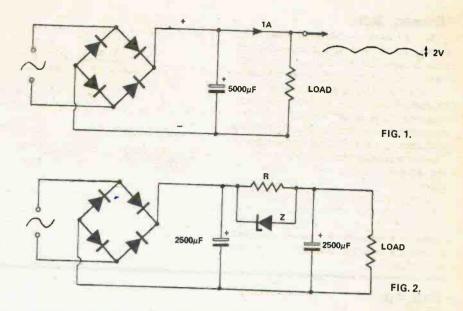


## Low Ripple at Low Current

In the normal circuit (Fig. 1) the ripple at 1 amp is at least 2 volts. Cheap power amps use this circuit (with low supply ripple rejection) and produce annoying amounts of hum at low signal levels.

In the circuit in Fig. 2 the ripple is considerably reduced at low levels and at high currents the supply voltage is only minimally affected.

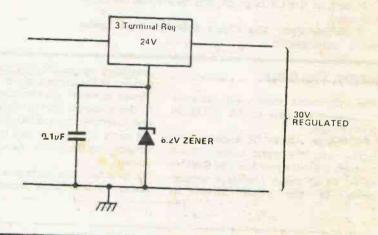
Maximum low ripple current (Im) = Vz/R where Ptot R must be more than  $Vz^2/R$  = Im Vz. IM = maximum total current so Ptot = IM-Im Vz. A typical set of values for Im =  $\frac{1}{2}$ Amp is Vz = 3V, R = 1½ ohms.



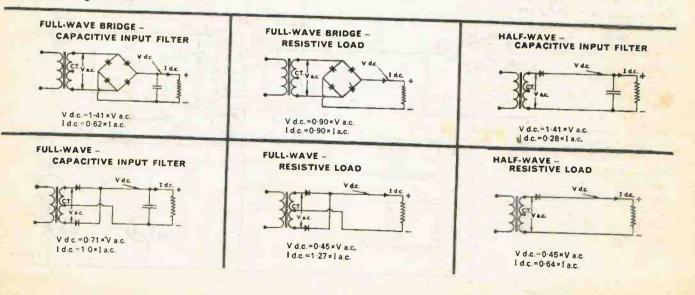
## **30 Volt Regulators**

Three-terminal voltage regulators are available in 5,9,12,15,18 and 24V types. If you require a 30V supply use a 24V regulator with a 6.2V zener diode in the earth lead as shown. This increases the volatge to 30V. A  $0.1\mu$ F capacitor should be connected across the zener diode as shown.

The zener should be of suitable wattage rating. In a similar manner for 27V use a 3.3V zener or for 33V a 9.1V zener.



## Standard Configurations

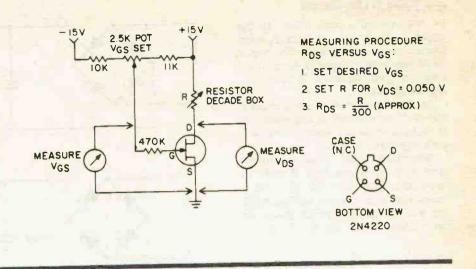


CIRCUITS No. 2

## TEST

### FET Testing. Static

A transistor socket will facilitate changing FETs. A good procedure is to first measure  $R_{DS}$  at  $V_{GS} = 0$ . Then increase  $V_{GS}$  (negatively for N-channel FETs) until  $RD_{DS}$  is about three times the zero-bias value; this corresponds to a mid-range cutoff frequency where matching is the most critical. With this  $V_{GS}$  setting try different FETs until a 10 percent or better match is found. If  $R_{DS}$  values seem to cluster higher or lower, try another unit as a reference and try matching to it. When matched units afe found, check the match at minimum  $R_{DS} = +0.5V$ ) and at 10 times this value of  $R_{DS}$ . A 20 percent mismatch can be tolerated at these extremes.



### **Diode Tester**

- This is a diode tester with light emitting diodes. If we change the polarity of the diode under test the appropriate LED will light.
- If both of the LEDs go on, this means that the diode is shorted.
- If neither light, this means that the diode under test is open circuit.

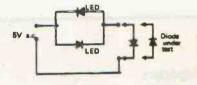
#### Ammeter, Wide Range

The instrument shown will measure currents from  $1\mu$ A to 1A F.S.D. in seven ranges.

IC1 is connected as a unity gain buffer and the input current flows through the resistor selected by SW1 to earth. In so doing a voltage proportional to the input current is developed across the resistor and this appears at the output, pin 6.

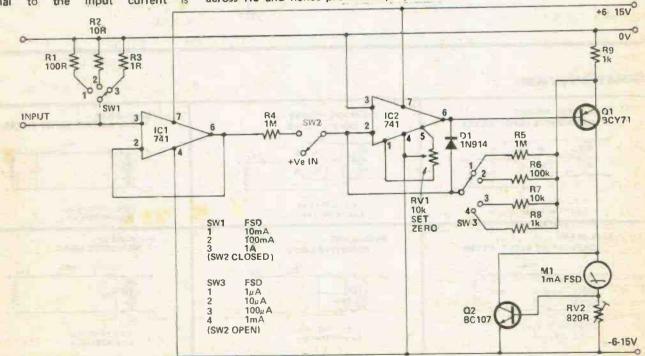
Small currents are measured by IC2. In this mode the current flows into the non inverting input. Since this is a virtual earth, the output will generate a voltage proportional to the input current.

In practice, this voltage is developed across R9 and hence provides a prop-



ortional current through Q1 and M1.

 $Q_2$  and RV1 form a meter protection circuit and the latter component should be adjusted so that  $Q_2$  starts to conduct at F.S.D. D1 is included to prevent damage to the base emitter junction of Q1 in the event of an input of wrong polarity.



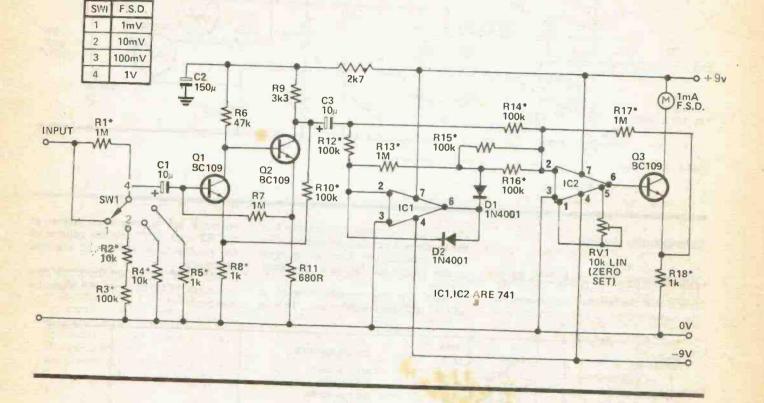
## Millivoltmeter. Audio

This circuit was conceived as an easily built instrument offering a  $\pm 2\%$  accuracy.

Q1 and Q2 are connected as a high gain feedback pair with a fixed gain of 100. IC 1 and IC 2 form a precision-full wave rectifler with a gain of 10 over a bandwidth extending from below 20 Hz to above 50 kHz.

The gain of the whole circuit therefore is 1000 and input signals above 1 mV must be attenuated. No setting up is required except for the zero adjustment of RV1. Input impedance is 1 MO2 on all ranges.

Resistors marked with an asterisk are 1% types.



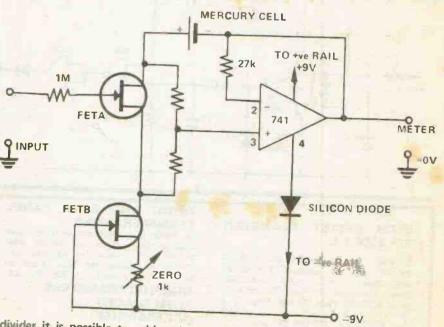
## DC Probe, 100 000 Megohm

The input current of a junction FET, usually less than 1nA, flows out of the gate, and is constant at a particular temperature, provided the voltage across the device is constant. By making the gate positive to the source this leakage current can be made to flow back into the device, reducing the input current almost to zero.

FET A should be a low loss, low Vp device (ideally Vp should be about 0.5V). FET B must be somewhat higher but is less critical, the bargain pack is usually a good source of such devices. Forward bias should be about 150mV and current through the FETs about 400mA.

The mercury cell holds the voltage across the input FET constant at 1.5V (1.35V plus 150mV) and the silicon diode in the op amp's negative lead prevents the cell from discharging when the power is off.

By adjusting values in the potential



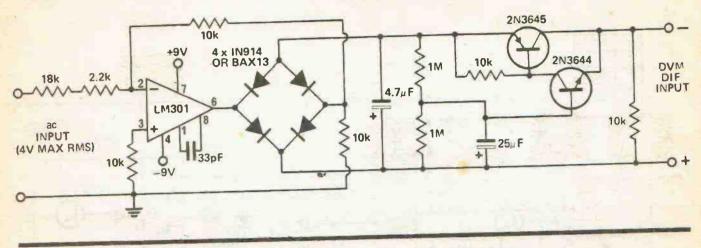
divider it is possible to achieve input currents within a few picoamps either

way and to measure the voltage on a small capacitor without changing it.

## Measuring RMS with a DVM

The above circuit may be used for measuring the RMS value of ac (sinewave) with a dc digital voltmeter. It has a frequency response to beyond 10 kHz and will measure signals as low as 400 mV. The error rises at low, frequencies, somewhat below 50 Hz, to about 4% mean. The LM301 supply may be as low as  $\pm 4V$ . or up to  $\pm 15V$ , if desired, with reduced sensitivity at the lower voltage.

The DVM input must be floating and a differential input is required. To increase the input range a step attenuator may be used.



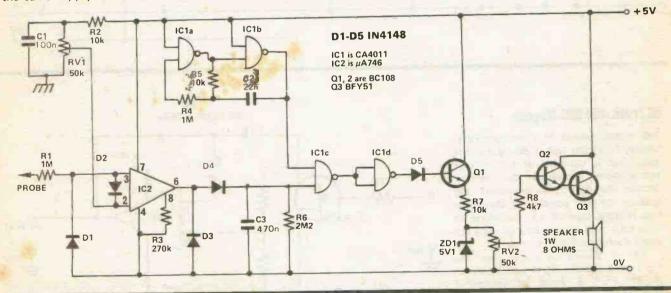
## Logic Indicator, Audible

The indicator will work with either TTL or CMOS circuits. A useful feature is that the unit can be powered by the same supply as the one supplying the circuit under test. Logic state 1 at the probe will produce an audible tone on the loudspeaker. A switching signal at the probe also activates the loudspeaker.

RV1 sets the threshold level at which IC2 will switch on. This is

normally set at maximum (wiper at the R2 end). RV2 sets the volume of the audible tone, and can be adjusted as required.

IC2 can be substituted by the equivalent LM748, but R3 must be removed first.



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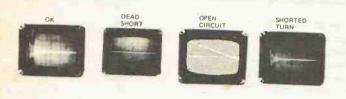


## Transformer-Inductor Tester

Transformers and inductors can be checked for open circuits, short circuits, shorted turns, etc., by this very simple method.

The inductance to be checked is connected across the Y-input terminals of a CRO and the time-base output coupled to the Y-input via a small capacitor. The retrace edge of the timebase ramp will set the inductance ringing, and a decaying oscillation will result.

Various conditions are shown in the accompanying illustrations – these have been photographed directly from an oscilloscope. From left to right, the photographs show –



## Pulse Catcher Probe

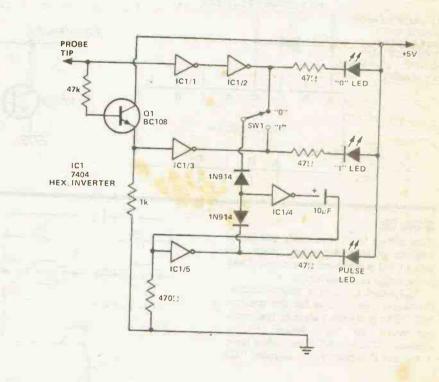
When working on digital equipment it is very often desirable to know the state of various points of the circuit. Usually an oscilloscope is used, however a very short duration pulse is usually hard to see unless the scope is a sophisticated wide-bandwidth type.

This logic probe has its own readout which illuminates a LED indicating whether the point tested is a logical "O" or "1".

It also indicates the presence of a high speed pulse, whether positive or negative going, (SW1 selects the polarity). This LED will also indicate a pulse train.

An inexpensive TTL Hex inverter is used. Power is derived from the five volt supply to the circuit being tested.

Having connected the earth and +5 V leads a simple check is to connect the probe tip to the 5 V supply and then to earth. The "1" and "O" LEDs should light in turn.



## JFET Test, Quick

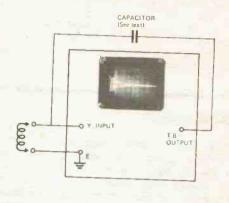
A quick test of an N or P-channel JFET is possible using only a standard mulitmeter ohmmeter.

With the ohmmeter connected between source and drain (polarity unimportant) the channel resistance (about  $200\Omega$ ) will be read. If the gate is now touched with a finger once or twice, the channel resistance should rise to about  $10M\Omega$  indicating pinch off. If this does not happen the FET may be assumed not working. Electrostatic pickup from the "mains" charges the gate capacitance and pinches off the FET. The time it takes for the channel resistance to

return to normal gives an indication of the gate leakage resistance of the FET.

The relatively low gate leakage resistance, and the high resistance between the finger and the mains helps to prevent destruction of the FET whilst it is being tested in this way.

no fault — a dead short — an open circuit — a shorted turn. The capacitor should be between 100pF and 1000pF for inductances down to 2 mH. It should be decreased for inductances lower than 2 mH. Meaningful results can be obtained for inductances as low as 50 uH. Timebase speed should be increased as inductance is decreased.

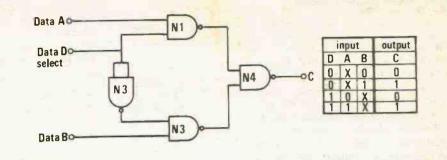


## Data Selector, Two Way

When the "DATA SELECT" terminal is at logical'0', the output of N1 is held high, whilst information presented on the "DATA B" terminal is transferred to the output of the circuit. Similarly, when the "DATA SELECT" terminal is at logical "1", the output of N3 is held high, whilst "DATA A" is transferred to the output. In a parallel data system one 7400 would be used for each bit.

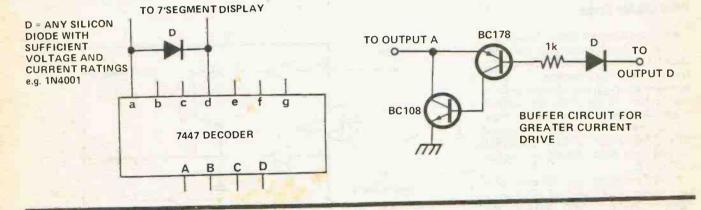
## 7 Segment Improvement

The display font of some 7-segment output devices produce the digit 6 without the top bar. Examination of the font reveals that whenever the bottom segment ('d' segment) is on, so is the top segment ('a' segment) for all



the other digits. Hence all that is needed is a diode connected so as to light segment 'a' whenever segment 'd' is on. The diagram shows the idea applied to a 7447 decoder. The drive capability of the device may be exceeded by this addition, so a buffer circuit may be required as shown.

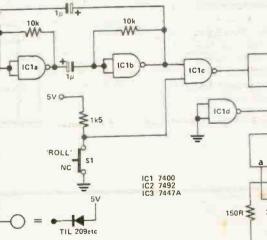




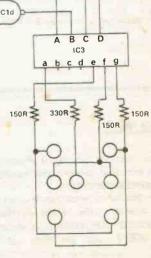
#### **3** Chip Die

This differs from previously published circuits in that decoding, count and drive LED is achieved by a single 7 segment decoder/driver chip.

IC1a and b form a multivibrator, providing clock pulses for the counter IC2. IC1c gates the pulses to the counter when the 'roll' switch, S1, is opened. IC1d is used to provide a logic 1 for the B input of the decoder, IC3



COUNT	DECODER INPUT	DIE		
0	2	5		
1	3	3		
2	6	6		
3	7	1		
4	10	4		
5	11	2		
0	2	5		



IC2

## Hex to 7 Segment

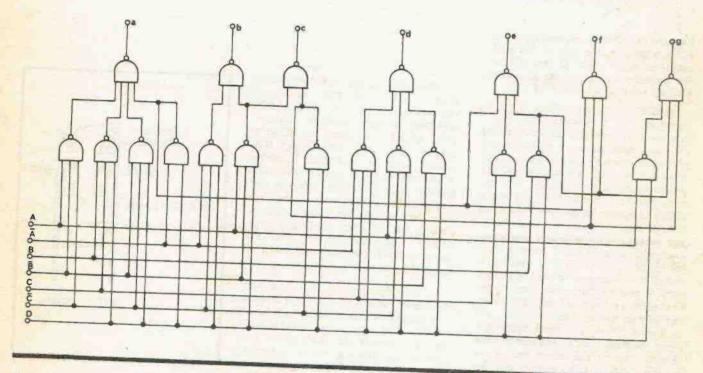
The circuit described below provides an extension to the 7448 BCD to seven-segment decoder, converting it into a hexadecimal to seven-segment decoder which will give the numerals 0-9 and the characters A,B,C,D,E, and F as output for a four bit binary input. (Inputs of A, $\overline{A}$ , $\overline{B}$ , $\overline{B}$ , $\overline{C}$ , $\overline{D}$  are needed with an inverting buffer - fan out 30 on the  $\overline{D}$  input.)

The 7448 is disabled by bringing the blanking input low when the input is greater than 0111<sub>2</sub> (i.e. D is connected to B1/RBØ on the 7448.) Outputs from the 7448 and the add-on decoder are OR-ed together creating a single seven-segment output.

											The state of the s	-	-	-		
9	0	0	. 0	0	0	0	0	0	-	-	-	-	0			-
	0	0	0	0				0		-		-		-	Ţ	-
æ	0	0	0	0	0	0		0		0	-		-	0	+	-
σ	0	0	0	0	0	0				-		-	-	-	-	-
U	0	0	0	0	0	0		0				-	-	-	-	0
٩	0	0	0	0	0	0				-		0	-	-		0
a.	0	0	0	0	0	0	-							-	0	0
-+-		-		-	-						-	a	-	0	-	
$\triangleleft$	0	-	0	-	0	-	0	_	A		~			-		
80	0	0	-	-		0	0	_	0	-	0	-	0	-	0	<del>,</del>
U	0	0	0	0	-		-							0	-	-
0	0	0.	0				0	-		0	0	0	-	-	-	-
	-			_	_	<u> </u>	9	0	-	Γ.	-	-	-	-	-	-

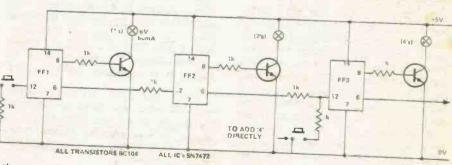
TRUTH TABLE for the 'add-on' decoder. Note that when the input is  $0110_2$  (610) a logical one is inserted in

the 'a' column to provide the resulting seven-segment '6' with a cap, thus differentiating it from a 'B'.



## **Binary Calculator**

This simple circuit allows infinite addition in binary (base 2). The circuit can be split into many identical stages, each consisting of a flip flop and lamp driver. An input of 'state 1' initiates the first flip flop. Hence the 1's lamp is on. A second pulse alters the first F.F to switch off the lamp and send a pulse to the second flip flop which illuminates the (2's) lamp. The third pulse causes F.F1 to light its lamp without altering the second. This means that the 1's and 2's lamps are on (1+2+=3) a total count of three. This on/off process continues for all



#### the stages.

There is no limit to the total count of the circuit, Each additional stage doubles the count. i.e: 9 stages, total count is 511. To enter large numbers a press button shorts the input of the intermediate stage to OV via a 1k resistor.

#### TTL Keyer

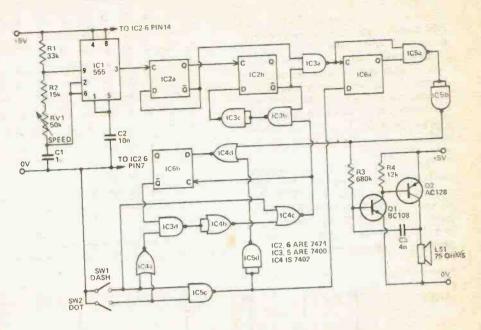
This device can be used to send perfectly spaced Morse at very high speeds - up to twice as fast as with an ordinary Morse key. It uses six integrated circuits, and also requires two special switches, SW1 and SW2, which are described later.

To describe the operation of the circuit fully would take up over a page of ETI, and so a simplified explanation is given here. IC1 is a 555 timer connected as an astable multivibrator, whose frequency is varied by RV1. The output is fed to IC2a, a D flipflop, which divides the input frequency by 2, producing a square-wave with a 1:1 mark-space ratio (dots).

If SW1 and SW2 are both open, the D inputs of IC2b and IC6a are both at logic 0, so that the dots from IC2a are inverted by IC3a, but blocked by IC5a. IC5b output is a 0, and so the audio oscillator made up of Q1 and Q2 and the associated components is disabled and no tone is fed to the speaker.

If SW2 is closed, IC6a's D input becomes logic 1. However IC6a's output can only change state on the rising edge of a clock pulse (i.e. the beginning of a dot). Hence if a dot has already started when SW2 is closed, it will not get through to the speaker, but the next dot will, because it will make IC6a's Q output to go to 1. Hence the dots now get through to the oscillator and successively enable and disable it, causing dots to be heard coming from the speaker. When SW2 is opened, if a dot is in progress it will continue until it has finished, and then at the beginning of the next dot, IC5a output will go low and no more dots will be heard. There is a short delay between the beginning of the dot and the Q output going low, which does cause a short 'blip' at IC5b output, but the blip is too fast to be heard.

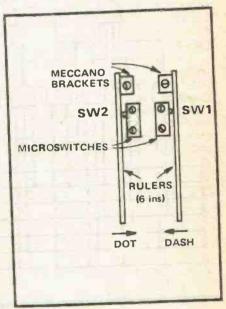
If SW2 is closed, but SW1 open, IC4c output goes to 1 and IC2b's Q output is effectively shorted to its D input. This causes IC2b to divide the string of dots from IC2a by two. The outputs of IC2a and IC2b are combined by IC3a to produce a waveform with a 3:1 mark-space ratio (dashes). These are passed on to the audio oscillator just as before. The dashes, like the dots, are self-completing. Notice that IC4c output determines whether dots or dashes are produced.



While SW1 or SW2 is closed, IC6b's D input is fed from IC4c output and clock pulses come from IC5b. If SW1 and SW2 are both operated together, IC4a allows the output of IC6b to pass to IC4c, and IC4d inverts IC4c output again, so that IC6b O output is shorted to its D input. Thus IC6b changes state every time a dot or dash begins at the output, and causes alternate dots and dashes to be produced. This is useful when sending a letter like C (dash-dot-dash-dot), as the switches SW1 and SW2 each need to be closed and opened just once.

It was found after the unit had been built, that it was difficult to send a letter like A (dot-dash) at high speed because SW1 had to be closed a fraction of a second after SW2, which was difficult to achieve at the first attempt. Hence IC5d and IC4d were added. When both switches are released, IC6b input becomes 0. A clock pulse is then applied to IC6b by the 'blip' described earlier. This makes the output go high, and if now SW1 and SW2 are closed simultaneously, the first thing to be heard in the speaker will be a dot.

SW1 and SW2 are push-button microswitches, and these are operated by means of a lever arrangement as shown in the diagram. Plastic rulers were used on the unit built because they are flexible.



The component values shown around IC1 give a speed range of 11-30 words per minute. The upper limit can be raised by decreasing R2. I have so far reached a speed of 20 wpm on the unit, after only a week or so of using it. As it stands it is a Morse practise unit, but if IC5b output is taken to a transistor driving a relay, the relay contacts could be used in place of an ordinary Morse key in a C.W. transmitter.



## **ASCII Keyboard**

This circuit uses a 16 key calculator keyboard to generate the 7 bit ASCII code, using two hex numbers to define ASCII character.

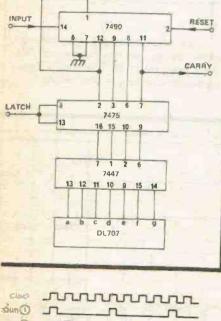
If, for example, the code for A (41 hex) is required, '4' is pressed first. After 10mS (to avoid switch bounce) the binary code from the diode matrix is latched into three D-type flip-flops. '1 is now entered. This time, after the 10mS delay, a 200uS pulse is produced by the second 74121. If the ENABLE input is low, a negative pulse appears on the STROBE output, while the ASCII code for A appears on the other outputs. If the enable input is high, the circuit remains in its initial state with the strobe pulse disabled.

### **Counter-Display Module**

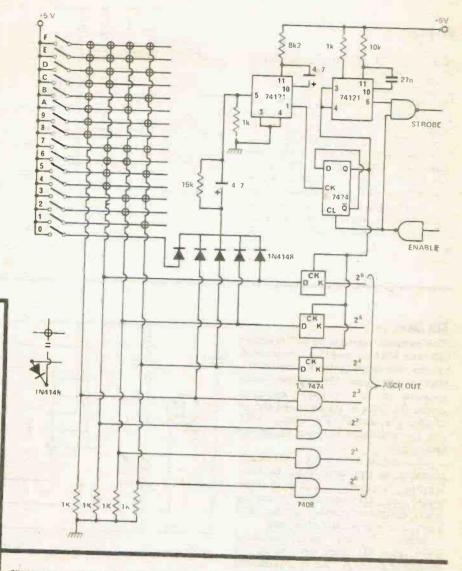
The signal is connected to the input line of the 7490 decade counter. When the 'latch' is high, the display will follow the count. When the 'latch' goes low, the display holds.

The module may be constructed on two pieces of veroboard, the boards being held together by wire soldered at each corner.

In order to cascade, common up all the latch hold and reset lines, and connect the carry line to the input line of the next module.

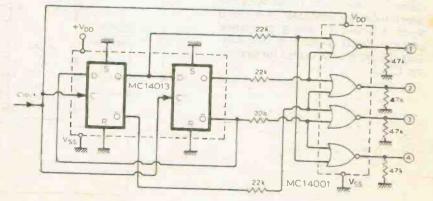






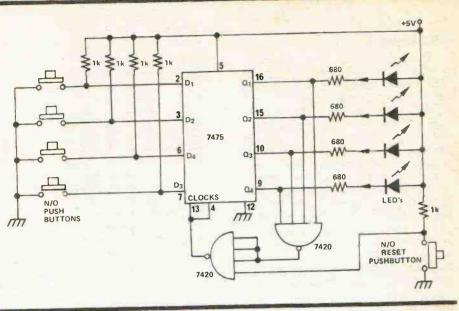
## Multiphase Clock Generator

The circuit shown, uses only two CMOS ICs, was designed by Michel Burri of Motorola's Geneva applications laboratories. It will produce a pulse on each of the four output lines in turn. These pulses do not overlap one another. Operation of the circuit is self-evident from an examination of the schematic; however, it is interesting to note that the power supply of the MC14001 is derived from the clock input. The maximum operating speed of this circuit is about 1 MHz.



#### Windicator

With two TTL ICs and a handful of other components, a circuit can be constructed that will indicate which of four buttons was pressed first, as well as lock out all other entries. It is thus suitable for quizzes, games of Snap and the like. The appearance of a logic D at one of the Q outputs, lights the appropriate LED and locks out other entries by taking the clock input low. The TTL outputs are capable of sinking 10 TTL loads or 16mA. Running the LEDs at 5mA leaves adequate margin to sink the 1 load of the 7420 gate.



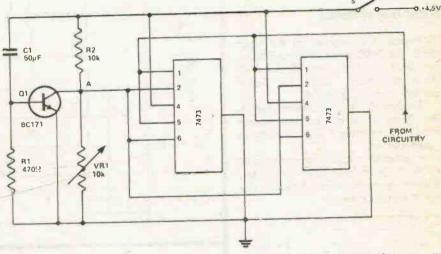
## Self-Clear

The network consists of two resistors R2 and VR1 arranged as a potential divider, the latter being shunted with a non linear load Q1 whose value depends on the voltage developed across R1. This is related to the charge of the capacitor C1. The resistor VR1 was made variable to make the design less critical.

As soon as S is closed, C1 starts charging; at the same time the baseemitter junction is being forward biased and O1 conducts, bypassing VR1. Voltage at point A is "low" and a set pulse is produced, therefore.

When the charge on C1 reaches a given value, Q1 stops conducting and voltage at point A rises to a stabilized value which is approx. 4.5 VR1/(R2 + VR1).

Component values are not critical although R1 and R2 must be close to

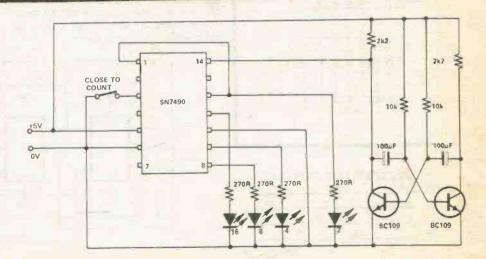


the indicated values.

Any NPN silicon transistor will work the prototype being assembled with the BC171. VR1 adjustment depends, amongst other things, on the number of flipflops and must be adjusted in each particular case to give best results.

## **LED Counter**

The astable multivibrator is used to generate pulses which operates the four integrated bistables. The 7490 gives a binary counting sequence and the 7490 gives a BCD count, This circuit is very useful for testing the IC's.



## Fuel Gauge, Digital

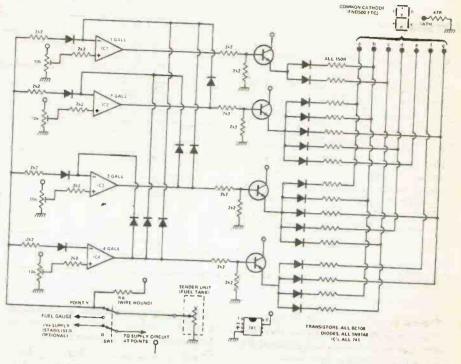
This circuit will give a digital readout of tank capacity in gallons, up to the 4 gallon mark. As the sender is of a log. nature, and knowing you have at least 4 gallons in the tank I did not find it necessary to provide a greater figure display.

The switch is a means of switching to fuel gauge. The voltage across the sender unit must not exceed five volts, thus, the resistance of RX must be 2.5x resistance of sender, when the tank is empty, presuming that the resistance is high on an empty tank. Disconnecting the output of a sender unit on a car fuel tank, and wiring it in series with a resistor RX we create a positive potential at point Y, relative to earth, which varies in relationship to the fuel level. Connecting point Y to the inverting input of a 741 op. amp., and using a trimmer at the non-inverting input, a condition is created whereby the output of the IC is either + or -, depending on the fuel level. A corresponding voltage, which represents X gallons, can be set at pin 3, and a drop in fuel will give an increase in potential at pin 2, which will result in a negative output, at pin 6. In the circuit above, voltage drop may cause one particular IC to go negative, but still be at a level to give another IC a positive output.

## Immobilisation, Automobile

In order to discourage theft of an automobile, many people incorporate a 'secret' switch to break the ignition circuit (usually in series with the key switch). This system is very easily bypassed using 'jumper' leads.

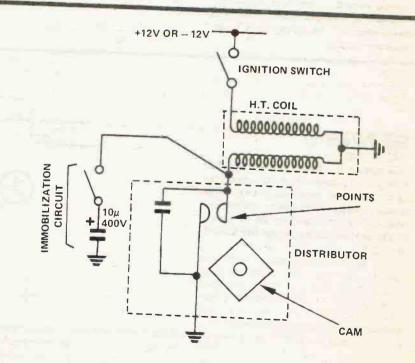
A more effective method of immobilisation is shown in Fig.1, also using a 'secret' switch. A 10uF/400V capacitor is switched across the points preventing the ignition being started; at the same time this prevents the use of 'jumper' leads.



In the case of IC4 (representing 4 gallons), the voltage at point Y may be of a level to give IC4 a + output, but also be lower at pin 3 on ICs 3, 2 and 1. This would mean that the non-inverting inputs would, in each case, also be positively biased, giving a positive output from each IC. To overcome this positive feedback from pin 6, of any IC

which has a positive output, is fed to inverting inputs to preceding ICs causing those particular ICs to 'turn off'.

The outputs from pin 6 of each IC may then be used to drive individual indicators, or the discrete decoder which drives a seven segment display as shown in the circuit.



# MISCELLANEA

## **Emergency Lights**

Basically it's a 240 volt mains operated device that provides low voltage dc power, and switches instantaneously and automatically to battery operation in the event of power failure. When power is restored the unit automatically reverts to mains operation and recharges the battery.

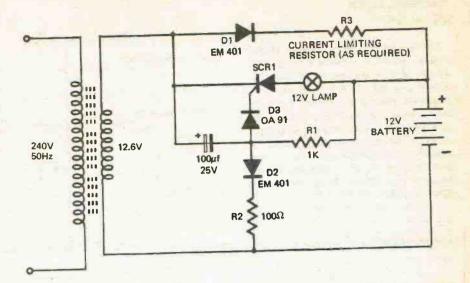
The unit may be used to provide emergency lighting in hospitals, or dark corridors, as an automatic battery change-over supply for intrúder alarm systems, or as a power failure alarm for heaters or deep freeze systems.

The circuit may be used in many different forms with circuit component values and battery ampere/hour capacity chosen to suit individual applications.

Figure 1 shows a circuit designed to supply 12.0 volts at 1.0 Amp, this may be increased to at least 2.0 Amps if the SCR is mounted on a heat sink.

Transformer T1 is a standard filament transformer with a secondary winding capable of supplying 12.6 Volts rms. Any SCR capable of handling a couple of Amps may be used for SCR1. We suggest a C106 series, primarily because they are generally available from most parts suppliers.

In theory, capacitor C1 should be non-polarised because, during emergency operation, it is reverse-charged to the SCR gate triggering voltage.



The 12 volt lamp shown in this circuit should be rated at 12 watts or less - this may be increased to 24 watts if the SCR is mounted on an adequate heat sink.

W

This rarely exceeds half a volt and in practise standard electrolytics may be used without fear of breakdown.

Resistor R3 must be chosen to limit the charging current of the battery to a safe level. This level varies from one type of battery to another — most nickel cadmium batteries, may be trickle charged continuously at 1/100th of their Ampere/hour rating — i.e., a one A/h battery may be continuously charged at 1/100th of an Amp = 10 mA.

The value of R3 may be calculated as:-

$$R3 = \frac{Vs - VB}{Ic} \times 1000$$

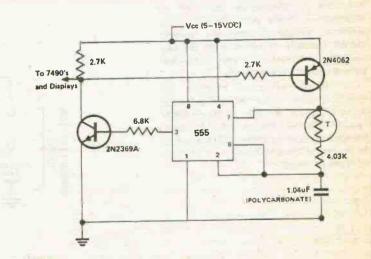
here		Supply voltage from transformer
	VB = Ic =	Battery voltage Charging current in milliamps

If in doubt, the maximum safe continuous charging current can be ascertained from the supplier or manufacturer of the battery that you have chosen.

To modify the circuit for other applications it is necessary to choose a transformer having an output about 5 or 10% higher than the standby battery, and rated to provide the load current required. The SCR must also be chosen with voltage and current ratings suited to the application.

## Digital Thermometer

This circuit we haven't tried yet but it looks very good, anybody who tries it, let us know how you get on. The circuits output frequency varies in a nearly linear manner from 38 to 114Hz as the temperature changes from 37°F to 115°F. The 555 is set up in the normal astable configuration with one resistor replaced by a thermistor/ resistor network and the other replaced by a transistor. The transistor's near zero on-resistance and very high offresistance results in equal charge and discharge intervals that depend only one the thermistor/resistor network. The thermistor is one with a value of 5000 ohms at 25°C and a resistance ratio of

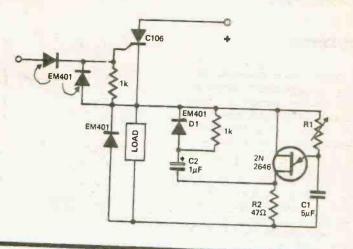


9.06:1 over the temperature range 0°C to 50°C. The capacitors need to be temperature stable and may need to be hand selected and added to give the

best results. It would seem that a similar circuit for Centigrade might also be possible – any ideas?

## SCR One Shot

The circuit shown is a 'one shot' or pulse generator. Here an incoming signal triggers the SCR and energizes the load. The load voltage energizes the UJT timing circuit. After a time determined by R1/C1, the UJT fires, and a pulse generated across R2 is coupled to the cathode of the SCR through D1 and C2. The SCR's cathode is momentarily lifted above the anode voltage and the SCR turns off.



MISCELLANEA

0+1

INPUT 2

OOV

EM401

LOAD 2

SCR2

### SCR Multivibrator

A triggered multivibrator - an input to 1 energizes load 1. A subsequent input to 2 energizes load 2, thus turning off SCR1 and deemergizing load 1.



Now for the dc meter amplifier which uses a 741 type IC. The values shown give full scale deflection on a 1 mA meter with only 10µA flowing into the input.

Circuit function depends on there being negligible difference between the voltages at the two inputs of an op. amp, when arranged in a negative feedback configuration. Accordingly, whatever voltage is applied to the non-inverting terminal, that is, across R1, will appear at the inverting terminal, that is, across R<sub>3</sub>. However,  $R_3$  is only 1/100th of the value of  $R_1$ , so that the current through R3 must be 100 times larger than that through R1. It is, of course, the current through R<sub>3</sub> that flows through the meter, and it is worth noting that the value of this current is not affected by resistor R2 in series with the meter provided of course that R2 is not too large to allow the required meter current to flow. The value of R2 is chosen here to limit meter current to about twice the FSD current, so providing a useful safety device should an unexpectedly high voltage be applied to the non-inverting terminal.

Thus we have a circuit incorporating a meter of 1 mA basic

**R5** +Ve 10k 22k RV1 67 M1 **R**2 SET ZERC 10k 6.8k 1mA R6 **C1** 10k 11 0.1µF **R4** +Ve 741 1k IC1 -Ve **R1** INPUT 1k 83 33

- OV

LOAD

SCR1

16

INPLIT 1

EM401

sensitivity but which appears to be a meter of 100 times that sensitivity.

Resistor R<sub>4</sub> is included to improve the performance with regard to drift, of the meter reading, as temperature changes cause changes in the op. amp. bias currents. It is best selected by experiment, although the value given was found to be satisfactory with three individual 741's.

The voltage at the slider of RV, is fed via R7 to the inverting input to

provide a means of setting the meter zero. It can, if desired, be used to give a centre zero, so producing a 5  $\mu$ A-0-5  $\mu$ A meter. The capacitor  $C_1$  ensures that the gain falls at high frequencies.

With a basic sensitivity of 10 µA., this amplifier enables a dc voltmeter of 100 kohm per volt to be constructed, by connecting the appropriate resistor in series with the input. The value of the resistor is given by: R = 100 V kilohms

where V is the input voltage

required to give FSD Note that the basic meter of 1mA is a type of movement that is much more robust, and yet cheaper, than others of greater sensitivity.

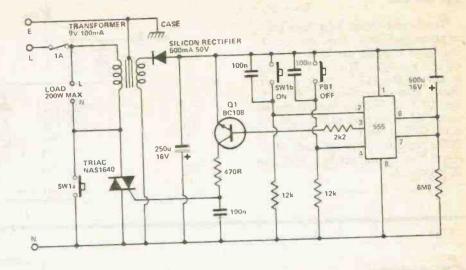
## MISCELLANEA

## Night Light, Automatic

This circuit was devised to turn off a bedroom light after a period of an hour. It could, however, be used to control any load up to a maximum of 200W. At the end of the period the unit switches off both itself and the load.

The timing period is generated by a standard 555 timer in monostable mode controlled by SW1b and PB1. For reliable operation timing capacitor C should be selected for low leakage. The output of the timer switches Q1 which in turn controls the gate current for the triac. During the timing period the triac is fully turned on so there is no degradation of the waveform across the load or RFI due to switching transients.

To initiate the timing period mains must be applied to the transformer to provide a DC supply for the timing circuitry. This is achieved by momentarily bypassing the triac with one pole of the ON switch, SW1a. Because this switch must also provide power to the load



it must be rated accordingly. SW1b is used to trigger the 555 and start the timing period. Q1 will then be turned on, providing gate current to turn on the triac. When SW1 is released the supply and the load is maintained until the end of the timing period. PB1 is provided so that the load can be switched off at any time. It may be omitted if this feature is not required.

Great care must be exercised with this circuit as all components are connected to mains neutral even when inactive.

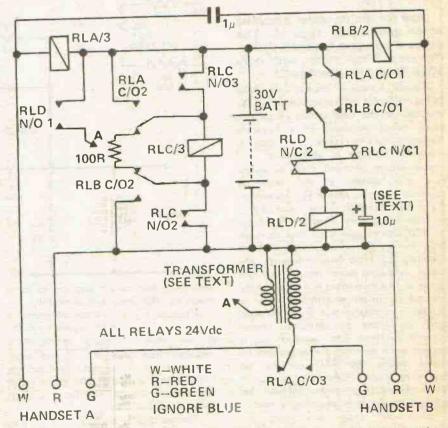
## **Telephone Circuit**

If handset A is lifted, RLA is activated changing over contacts RLA energising RLD. RLD has a pair of N/C contacts wired in series with its coil and this causes the relay to vibrate. The contacts would not however, change over fully, and a capacitor is wired in parallel and stores enough charge to allow the relay to change fully. The value of the capacitor will depend on the type of relay being used but the value selected should be chosen to cause the relay to vibrate at about 25 Hz.

A second set of contacts is wired in series with the transformer, which in the prototype was an old 250 to 125 V transformer with the 125 V winding being used as the primary. The output of the transformer is fed to the third set of contacts of RLA which selects which telephone is to be rung.

On lifting the other handset relay RLB will energise and the exclusive OR arrangement of contacts RLA and RLB will inhibit the bellringing circuit.

To prevent either bell ringing again if one of the handsets is replaced RLC is included. When both handsets are raised RLC energises and is self-latching, one set of its contacts being in series with RLD. When both handsets



are replaced, RLC is shorted through the 100 Ohm resistor and turns off, resetting the bellringing circuit. The 1 uF capacitor provides the required coupling for speech between the two handsets.

ETI CIRCUITS No. 2

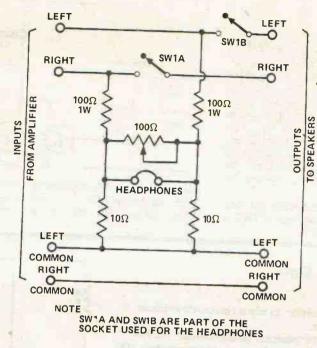
## Headphone Adaptor

HEADPHONES have impedances which range from 8 ohms to 2 k ohms or more and handle a typical maximum power of 500 mW. To limit the power that may be delivered into the 8 ohm types, commercial amplifiers generally supply the headphones from the amplifier output via series resistors of around 220 ohms.

Although this technique allows the use of practically any type of headphones without fear of damage the series resistor drastically reduces the amount of damping the amplifier can apply to the phones.

A further problem with headphone listening is that the stereo separation is unnatural in that there is little right channel information fed to the left ear and vice versa.

This simple little adaptor is inserted between the amplifier and the leads to the speakers. It restores damping, by supplying the phones from a 10 ohm source, and has a blend control by which the separation between channels can be varied to obtain a more natural sound.



Fiy. 1. Circuit diagram of the headphone adaptor.

SCELLANEA

7400 14p	1.4.4	C-MOS ICa	OP. AMPS	NESSIV IA			
7401 18p	74107 36p 74109 60p	4000 2		8p NE543K 22	50	MJE3055 800 2N2908/A	220 DIODES DEBUDOS
7402 18p	74110 600			op /US	DR DIGO CPRUM 77	75p /#PF102/3 2N2907/A	250 8Y122 13- 000000
74C02 25p 7403 180	74111 75p	4006 12		0.0 744	P 2102.2 BALL	40p 2N392688	So OAT RECTIFIER
7403 18p 7404 24p	74112 86p		1p LM318N 17	50 747	D 2117.2	211282000	0A81 .155 1A 1000
7405 250	74116 216p	4008 18	Op LM324N 13	0p 748	D 2111	MPSA06 370 203053	TIP 0485 150 14 4000
7406 435	74119 160p		70 LM348N 13	Op 776	2706 EPROM 61	MFSA12 620 740004	220 0.590 9p ZA 50V.
7407 43p	74120 1300		and the second sec	5p 3900 70	2716 EPROM EA	0 MP3455 400 2N3055	550 0401 P 24 100V
7408 22p	74121 32p	4012 2	1 LINEAR LCs	ALF CO. A.F.	SUBOA CPU E1	1 Marsung 12p 2N3442	1510 04 200 P 2A 200V
7409 22p 7410 18p	74122 52p 74123 75p	4013 51	BR AV 2 8238 85	P NESSZB AND	AV 5 3278	Leocara and an and an	54p 0A202 100 10 10 000
7411 259	74123 750	4014 90	00 C120204	P NE565 160	ALCOOC TO LINE	3 MOCIEC	560 1N916 60 44 1000
7412 250	74126 650	4015 90	P CA1026	P NE566 200		- OC28 90p 242301 4	14p IN918 7p 44 4000
7413 40p	74128 820	4017 100	P CA3048 250	180	P MC6620 RAM 64	20 0C35 90p 2N3706/7	MAL LOVE OP 64 LOVE
7414 85p	1/4132 81p	4018 110			p MCE850 RAM 75	50 paces 300 2N3708 9	140 1M4005 200 64 100V
417 40p	74136 81p 74141 85p	4019 57	P CATORDE	P SN76002H		Op 820105 205 2N3773 3	120p 3 Mart 4 8 4 10
420 18p	74141 85p 74142 300p	4020 140	P CA30895 354	P SN76008 280	B 110 24	P TIP29A SON THISBY	27p 1N5401 115p
421 430	74145 850		PICA3090A0 424	SN76013N 175	AC125 6 20p 91167 25	P 1129C 820 233821	50p 1185404:720p 1100 1000
422 28p	74147 2050	4022 140	P ICL7106 C1	0 SHIDOISND 160	P AC176 200 85172 28	p TIP3CA 601 MISSON	AT ZENERS 27
423 36p	74148 160p	4024 82	400		AC187/8 200 BF178 30		22n 2.7433V 254. 400V
426 33p	74150 130p	4025 23	P LM377N 200	5N76023ND 160.	AD149 800 BF179 35	TIR310 200 2N3905 G	220 400mily 11p 43
427 400	74151 81p 74153 81p	4026 200	P LM380N Sta	P 3/0515 756	AD161 45p BF180/1 35	p TIP324 630 2N40258	19p 1W 22p
428 400		4028 110	P LM381N 134	310		P TP32C 850 7441170	TRIACS
430 TEp	74155 97p	4029 120	LM389N 160	TBA120		P TIP33A 87p 2N4125 4	Plantic Una Emmi
	74158 970	4030 87	150	TBA6418 300		TIP344 1200 244409	38 400V 85p
433 43p 437 37p		4040 150	P MC13610	P TBA651 226		TIP345 2N4427 5	17n 04 400% 154 400V
438 370		4042 97	MC14951 490	15A800 111	AF239 48p 8F200 40c	TIP35A 342- 2746877 6	10p 84 500y 107p 200
440 180	74151 130n	4046 150	P MC 4961 112	TRA000 125p	BC107/8 10p BF2448 34	p THP3SC 2900 745179 7	50 870 0000
441 85p	74162 1300	4047 1500	MC3340P 180	T042020 100p	BC108/8 10p 8F2565 60; 8C109 10p 8F257 34	11P36A 2970 286705	40
442 75p		4849 64	150	ZNARA	8C109 10p 8F257 34p BC109/C 11p 8F258 33p	TIRSUL 3800 2N5401 6	
43 120p		4050 588	NEESS 2201	444246 4345	8C117 270 8F259 485	TIP41C 84- 2N5457/8 4	Op orn as and TH 206 But
45 1080		4054 1200	NESES	41425E 432p	BC147 Sp BF337 32p	TIP424 76 205458 4	P 1788 12 100 TH 211 Game 24
46 1089	74167 3200	4055 140p 4056 145p			BC148 Bp BFR39 34p SC157 11p BFR40/1 34p	TIP-12C 960 2N6107 m	ORP 60 900 TIL32 Intrared at
and a state	74170 2600	060 1300	Plastic-TO220-3 Ter		BC158/9 130 BFP79 34-	TIP2015 760 2N6027 6	2N5777 400 8.2 Red 16
50 18p		068 30p	minals	/0L02 70m	8C169C 15p 8FR80/1 34p	TES43 400 2118247 200	Dp Gran 20
51 180		069 30p		78L12 70p	BC172 11p BFR88 37p	210234 140	
53 18p	74175 970 4	071 30p 072 30p	1000 1150	15V 78L15 70p	8C177 20p 8PW10 90p 8C178 17p 8FX29 30p	2N698 430 3N979 70	2 15 40/B( TOP / 30
	74176 130p 4	073 450	6V 7806 115p	100mA -ve 1092		2017UB 8 220 3N140 BT	34 400V STUD
no iop		U/8 30p	7914 7000 1130	5V 79L05 80p	8C182/3 12p 8FX30 34p	2N918 43p 3N141 90	15A 400V Plastic 220
72 320		081 30p	15V 7815 115p	12V 79L12 400	8C184 14p BFX86/7 300	2N1131/2 200	IGA GOOV Prostic AND
73 360	74182 1500 4	082 30p 093 104p	TBV 7818 1150	15V 79L12 40p 79L15 80p	8C187 32p 8FX88 30p 8C212 14p 8FY50 32p	2N1304/5 75m 00000 120	
74 37p	74184 2600 4	510 1400	24¥ 7824 115p	Langer		2N1306/7 750 40000	
	14103 180p 4	511 140p	1 Amp'	LM309K TO3 150p	8C214 160 8FY52 220	ZANG 13 Z2p 40361/2 43	213525 54 4000 TOSA
76 378	74100 400	510 130o	5V 7905 160m	LM327N DHL 275p	BC461 40p 8FY90 50p	2N1891 32 40409/10 75	2NALAL BA GOOV Plastic 2000
80 54p	74191 1200 4	518 110p 528 110p	12V 7912 160n		BC478 32p BRY39 48p	2N2102 000 1000 325	2N5064 0.84 30V T092 36p
	74192 1200 1.	528 110p 4433 E14	15V 7915 160p	78+8700	ETER? BR. HARTER AU	2N2160 120p 40595 90p	
82 90p 1	4193 120p 1.	4533 5400	24V 7924 160p	7805K TO3 150p	8CY70 20p MJ481 175	2N2219 22p 40835 60	LOW PROPILE DIL
	11105 110	4583 150p	Heat smit 17" /W 25p		BCY71 24p MU491 2160	2/23/69 96- 40638 1400	AUGACIS BY TEXAS
5 120p 1	4198 1300 0	ther 301 160n	suitable for TO220	VARIABLE	10131/2 65p MJ2501 250p	201340 - 40673 900	12pm 12p 27 min 14
56 38n 7	4197 130p 9	301 160p 302 175p		PRALAMENT UIL 450	HD140 00 000000 1300	21/2646 520 40871 900	15 pm 13p 24 pm 40p
19 340p 7	-198 270p 83	308 3250	100-1		B0140 B0p MJE2955 130p B0758 225p MJ3001 250p	2N2904/A 22n +00775	18 50 30 480
		10 2750	100mA ++++ 1092 SV 78105 700	LM317 TO220 3250		diversuo/A ZZp	20 pm 275 40 pm 60p
2 580 7		111 275p	socos rop	TL430 TO92 70p	VAT inclusive	Drices - add 25- 50	
3 36p 7		12 160p	DISPLAYS		man Govt Coller	prices - add 25p P8	P - no other extras
4 90p 7	5325 4000 91	16 250p	3015F Minitron	200p DRIVERS	MAIL	TO CIC OIGOIS ACCEDI	9.0
	601 175p 93	18 2760	FND500/507 Red DL704/DL707 Red	130p /5491 84p	ORDER TECH	NOMATI	the second state of the second state of
5 90p 9 7 290p 9	502. 175p 93	21 1600		160p /5492 96p		NUMATI	CITO
00 1400		22 150p	TILSI2/313 Ret	250p 9386 200p 120p 9370 200p	ONLY		VLID.
		24 2500	TIL321/322 Rad	130 9374 200		st Road, London NWS	

ETI CIRCUITS No. 2

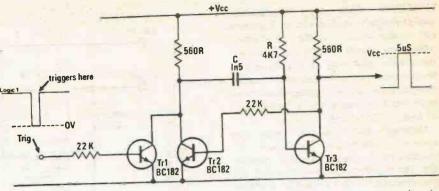
Telex: 922800

# MISCELLANEA

## **Rising Edge Trigger**

The diagram shows a method of triggering a conventional monostable on the rising edge of a short negative-going pulse. The additional transistor, TR1, provides good isolation between the output pulse and the triggering circuitry. The circuit shown gives a pulse of 5 $\mu$ sec duration, but of course the usual design formula  $\tau = 0.65$  RC can be used to determine circuit values for other pulse widths.

One slight disadvantage of this circuit is that the collector of TR2 is



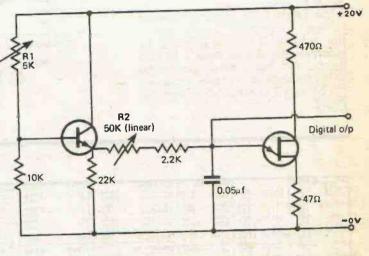
held down by the triggering waveform, so the switch-on of TR3 is not regenerative. For this reason the falling edge of the output pulse is not as fast as it might be, but is sufficient for most purposes.

## Position Transducer, Digital

A shaft angular-position to digital output transducer is shown in this circuit.

Rotating the angular position potentiometer R2 will provide a digital output varying from approximately 200 Hz to 2000 Hz.

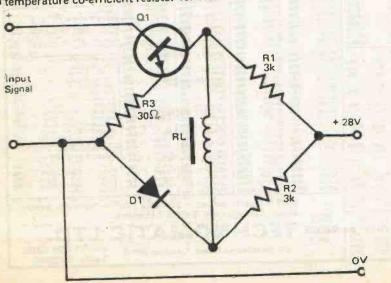
The 5k trim potentiometer R1 provides a rate adjustment of a further 50%. This trim adjustment is independent of the main timing potentiometer.

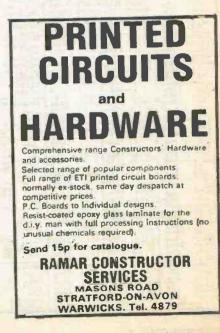


### **Temperature Stabilized Relay**

Accurate relay trip-point operation can be obtained over an ambient temperature range from -50°C to +90°C using this simple circuit.

The temperature sensitivity of the silicon transistor Q1 is balanced out by the silicon diode D1. Gain/temperature stabilization may be obtained if required by using a positive temperature co-efficient resistor for R3.





ETI CIRCUITS No. 2

Basic solid state crystal oscillator circuit techniques are by now well established, most circuits being adaptations of the well-known vacuum tube technology such as the Pierce, Hartley, Clapp and Butler oscillator and use both bipolar and FET devices. Whilst these circuits basically fulfil their intended purpose, there are many applications which require something different or where performance needs to be reliably characterised.

Presented here are a variety of circuits, for a range of applications from LF through the VHF range, that are not commonly found in current amateur use or literature.

## MODES OF OPERATION

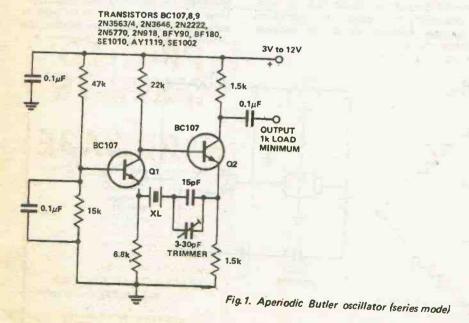
A point not often appreciated, or just forgotten, is that quartz crystals can oscillate in a parallel resonant mode and a series resonant mode. The two frequencies are separated by a small amount, typically 2-15 kHz over frequency range. The series the resonant frequency is lower in frequency than the parallel. A crystal specified and calibrated for use in the parallel mode may be satisfactorily used in a series resonant circuit if a capacitor equal in value to its specified load capacitance (usually 20,30, 50 or 100 pF) is connected in series with the crystal. Sadly, you can't invert the process for series resonant crystal in parallel mode circuits. The series mode crystal will oscillate higher than its calibrated frequency in this case and it may not be possible to capacitively load it down sufficiently.

Overtone crystals operate in the series mode usually on the third, fifth or seventh overtone, and the manufacturer normally calibrates the crystal at the overtone frequency. Operating a crystal in the parallel mode and multiplying the frequency three or five times produces quite a different result from operating the same crystal in the series mode on its third or fifth overtone. When ordering overtone crystals avoid confusion and specify the frequency you want, not the apparent fundamental frequency.

Fundamental crystals in the range 500 kHz to 20 MHz are usually specified for parallel mode operation but series mode operation can be requested. For low frequency crystals, up to 1 MHz, either mode can be specified. Overtone crystals generally cover the range 15 MHz to 150 MHz.

## WIDE RANGE or APERIODIC OSCILLATORS

Oscillators that do not employ tuned circuits can be very useful, whether they are simply used as 'crystal checkers' or some other purpose. Particularly for LF crystals, tuned circuits can be bulky. However, they aren't without their traps. Some crystals are prone to oscillation on unwanted modes, particularly the DT and CT cut crystals used for LF quartz oscillators. It is wise to check that the output is on the correct frequency and no mode instability is evident. Reducing feedback at the higher frequencies usually cures this. In extreme cases, the idea has to be



abandoned and an oscillator having a tuned circuit used instead, (LF crystal oscillators are discussed later).

The first circuit is an emitter-coupled oscillator, a version of the Butler circuit.

The output of the circuit in Fig. 1 is essentially sine wave; reducing the emitter resistor of O2 increases the harmonic output. By doing this, a 100 kHz crystal produces good harmonics through 30 MHz. It is a series mode circuit.

A variety of transistors may be used. For crystals above 3 MHz, transistors with a high gain-bandwidth product are recommended. For crystals in the 50 kHz to 500 kHz range, transistors. with high LF gain, such as the 2N3565 are recommended. Also, for crystals in this range, permissable dissipation is usually less than 100 microwatts and amplitude limiting may be necessary. Low supply voltage, consistent with reliable starting, is recommended. Modifying the circuit by the addition of diodes - as shown in Fig. 3 - is a better method, and starting performance is improved. The circuit will oscillate up to at least 10 MHz with appropriate transistors and emitter resistor values. An emitter follower or source follower buffer is recommended. Similar comments to the above apply to Fig. 2. An emitter follower buffer is included in this circuit. Both circuits are slightly frequency sensitive to power supply voltage changes and load variations. A load of 1 k or greater is recommended.

TTL IC can be used in crystal oscillator circuits but many published circuits have poor starting performance or suffer from non-repeatability owing to wide paramater spreads in IC's. The circuit in Fig. 4. has been tried by the writer over the range 1 MHz to 18 MHz and can be recommended. It is a series mode oscillator and suits AT-cut crystals. The output is about 3 volts peak to peak, square wave up to about 5 MHz beyond which it is becomes more like half-sine pulses. Starting performance is excellent, often a critical factor with TTL oscillators,

### LOW FREQUENCY CRYSTAL OSCILLATORS

Crystals in the range 50 kHz to 500 kHz require special considerations not encountered with the more common AT or BT cut HF crystals. The equivalent series resistance (which determines 'activity' – that figure of merit of days of old) is much greater and their permissable dissipation is

# CRYSTAL OSCILLATORS

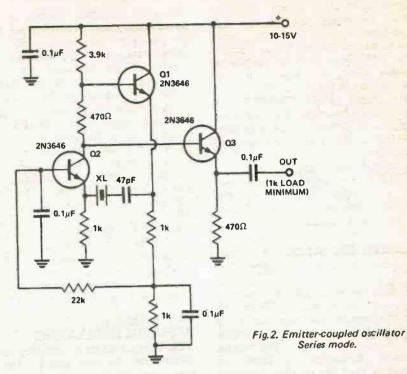
limited to less than 100 microwatts, preferably 50 microwatts or less.

The circuit in Fig. 5 is a series mode oscillator. It has the advantage of not requiring a tuned circuit, and has a choice of sine or square wave output. For crystals in the range 50-150 kHz, 2N3565 transistors are recommended although the author has found BC107's satisfactory. Either type will suffice for crystals in the range 150 kHz to 500kHz. If you find the crystal has a very high equivalent series resistance, in which case increase R1 to 270 ohms and R2 to 3.3 k. For square wave operation, C1 is 1 uF (or a value close to, or above it). For sine wave output, C1 is not in circuit. Amplitude limiting is unnecessary. Sine wave output is about 1 V rms, square wave output about 4 V peak to peak.

The circuit in Fig. 6 is a modified form of the Colpitts oscillator, with the addition of resistor Rf to control feedback. Capacitors C1 and C2 should be reduced by preferred values as the frequency is increased. At 500 kHz, values for C1 and C2 should be around 100 pF and 1500 pF respectively.

The circuit as shown gives sine wave output with the second harmonia about 40 dB down (or greater). This can be reduced by careful trimming of Rf and C1. Note that, at the reduced level of feedback necessary to achieve this, it takes some 20 seconds for the oscillator to reach full output. Output is about 2 to 3 volts peak to peak.

If you need an output rich in harmonics, the simple addition of a 0.1 uF capacitor, across the emitter

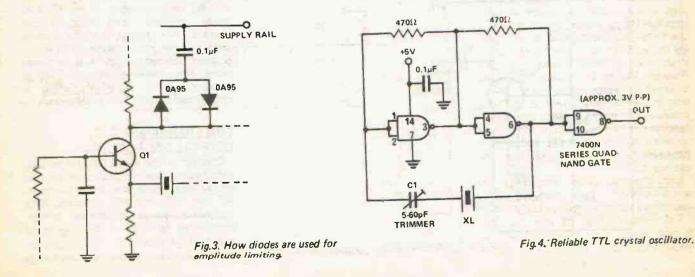


resistor will achieve this. Output then rises to about 5 V peak to peak. Power supply voltage can be reduced in this case to lower crystal dissipation.

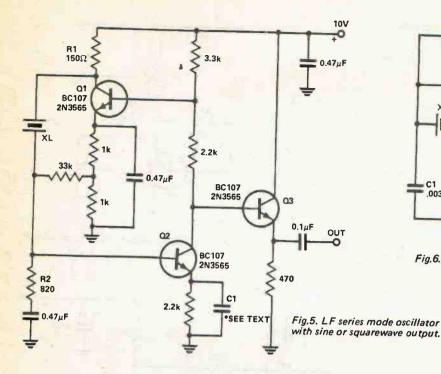
Other transistors can be used, but bias and feedback may have to be adjusted. For cantankerous crystals determined to oscillate in modes other than those you wish, the circuit of Fig.7 is recommended. Feedback is controlled by tapping down the collector load of Q1. Amplitude limiting is necessary to keep the crystal dissipation within limits. For 50 kHz crystals the coil should be 2 mH and its resonating capacitor 0.01 uF. Output is about 0.5 V rms, essentially sine wave. The use of an emitter follower or source follower buffer is recommended. If a parallel mode crystal is used the 1000 pF capacitor shown in series with the crystal should be changed to the crystal's specified load capacitance (usually 30, 50 to 100 pF for these crystals).

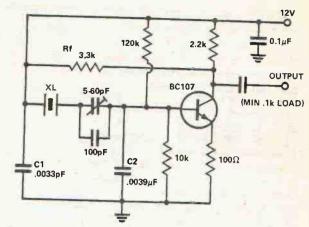
### HF CRYSTAL OSCILLATOR CIRCUITS

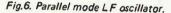
Solid state circuits for the popular AT-cut HF crystals are legion. However, results aren't always what one would expect. Most fundamental crystals up to 20 MHz are usually specified for parallel mode operation. However; such crystals can be used in series mode oscillators by putting the



## CRYSTAL OSCILLATORS







specified load capacitance in series with the crystal as mentioned previously. Both types of circuit are detailed here.

A useful oscillator for the range 3 to 10 MHz that does not require a tuned circuit is given in Fig. 8 (a). It is, of course, the same circuit as Fig.6. The circuit can be used down to 1 MHz if C1 and C2 are increased to 470 pF and 820 pF respectively. It can be used up to 15 MHz if C1 and C2 are reduced to 120 pF and 330 pF. Respectively. This circuit is recommended for non-critical applications where high harmonic output is wanted, or not а consideration.

The addition of a tuned circuit as in 8(b) reduces harmonic output considerably. A tuned circuit with as high a Q as possible is recommended. In a 6 MHz oscillator, I have obtained the following results. With a coil Q of 50 the 2nd harmonic was 35 dB down. With a Q of 160, it was -50 dB! Resistor Rf can be adjusted (increase slightly) to improve this. The output is also increased with a high Q coil. As previously noted, with reduced feedback it takes some tens of seconds to reach full output from switch on, however, frequency stability is excellent.

Operation at other frequencies is accomplished by changing the capacitors and coil appropriately.

This circuit (Fig. 8) can also be turned into a very effective VXO. A small inductance is placed in series with the crystal and one of the capacitors in the feedback circuit is made variable. An ordinary two-gang 10-415 pF (or thereabouts) broadcast tuning capacitor will do the job nicely. Both gangs are paralleled. The tuning range depends on the crystal used, the inductance of L1 and the frequency. A greater range is usually obtainable with the higher frequency crystals. Stability is excellent, approaching that of the crystal.

#### A VHF OSCILLATOR-MULTIPLIER

The circuit in Fig. 10 is a modification of the 'Impedance Inverting' overtone oscillator. Normally, with the impedance inverting circuit the collector is either untuned or grounded for RF. The collector can be tuned to twice or three times the crystal frequency To reduce the output at the crystal frequency, a double tuned circuit is recommended. DO NOT tune the collector to the crystal frequency, otherwise the circuit will oscillate at a frequency not

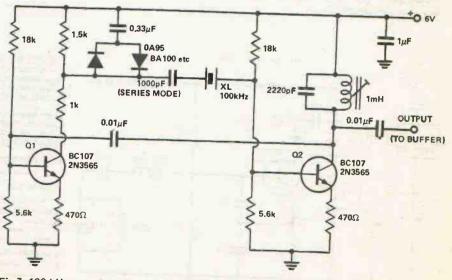


Fig.7. 100 kHz crystal oscillator (with tuned circuit).

## CRYSTAL OSCILLATORS

controlled by the crystal. It is

advisable to keep the collector lead as

excellent. All outputs other than the wanted output were at -60 dB or

greater. Noise output is at least 70 dB

below the wanted output. It makes an

excellent conversion oscillator for VHF/UHF converters. Almost 2 V of

RF is available at the hot end of L3

(author's prototype at 30 MHz). A

recommended. As indicated on the diagram, different circuit values are necessary for different transistors. Strays in individual construction may

also necessitate variations. L1 can be used to pull the crystal onto

Slight variations in frequency (about 1 ppm) occur when tuning L2 and L3 and also with load variations. However, in practise, these turn out to

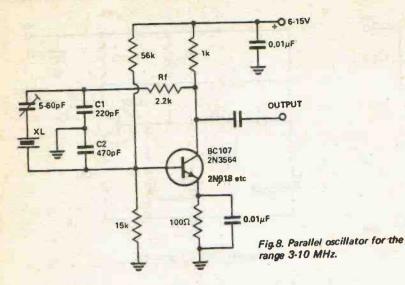
regulated

Zener

frequency.

be of no consequence.

short and direct as possible. Results with this



circuit

supply

are

is

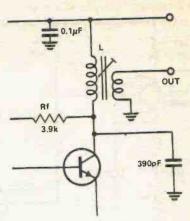
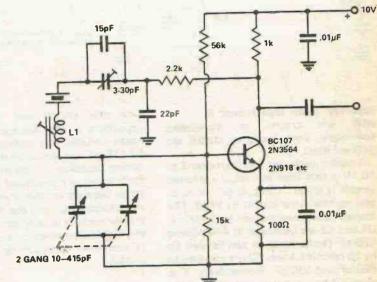
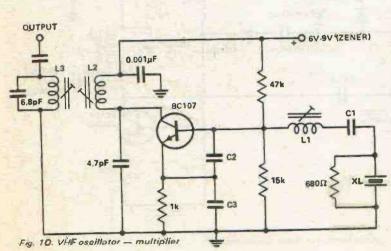


Fig.8b. Adding a coil to the circuit shown in Fig.8.







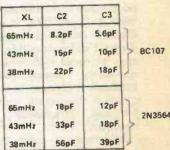
65 MHz Xtal 130 MHz OUTPUT L1 = NEOSID AZ ASSEMBLY (4mm FORMER & F29 SLUG) WOUND WITH 12 TURNS OF 4.55 mm ENAMEL WIRE, CLOSEWOUND

12/3 = NEOSID, DOUBLE ASSEMBLY 7300 CAN, TWO 722/1 FORMERS, F29 SLUGS, WOUND WITH 5 TURNS, 0.63mm ENAMEL, CLOSEWOUND

#### C1 = 33 OR 39 pF

43 MHz Xtal 130 MHz OUTPUT L1 = 20 TURNS 0.4mm AS ABOVE L2/3 = AS ABOVE C1-= 56pF

38MHz Xtal 116 MHz OUTPUT L1 = 24 TURNS 0.4mm AS ABOVE L2/3 = 9 TURNS 0.63mm AS ABOVE C1 = 68pF OR 100pf



ETI CIRCUITS No 2

Speaker crossover networks are auite simple to design - if you have a computer to calculate the component values. So we presented a Honeywell computer time-sharing terminal with the task. Here are the results - crossover design made easy.

N MODERN high-fidelity systems the loudspeaker must cover a range of frequencies from 30 Hz to at least 15 kHz.

Generally this requires the use of two or more speakers in each enclosure. each speaker operating within a controlled frequency range.

The extent of that part of the sound frequency spectrum handled by each speaker is controlled by 'crossover' or frequency dividing' networks consisting of two or more filters.

A two speaker system usually has a two-way network consisting of a high-pass filter and a low-pass filter. The high-pass filter limits the low frequency response of the high frequency speaker, and the low pass filter limits the high frequency response of the low frequency speaker.

A three speaker system will usually have a three-way network. This will consist of a high-pass filter, a band-pass filter, and a low pass filter. The high and low-pass filters act in a similar manner as those in a two-way system. The band-pass filter controls the frequency range of the mid-range speaker.

The effect, in theory at least, is a smooth transition from one speaker to another over the total frequency range of the system.

For a multi-speaker system to have a substantially flat response, it is essential that each speaker in the system has a usable frequency range BOHMS overlapping the next. For example the bass speaker in a two speaker system have a response that is may substantially flat from say, 70 Hz to 3 kHz. The high frequency speaker chosen for this system would probably have a usable frequency range from 500 Hz to 15 kHz. Thus the overlap is 2.5 kHz.

#### DETERMINING THE CROSS-OVER POINT

A crossover network for the system outlined above would be designed to operate somewhere between 800 Hz and 1 kHz.

A three-way system would probably be designed to crossover at 400 to 500 Hz and again at 5 kHz.

The optimum crossover frequency may be easily determined by studying the frequency response curves of the speakers to be used and arranging for the crossover to take place before the response of a given speaker unit falls off, or the movement of the diaphragm becomes non-linear. Few bass speakers, for example, have any really usable response beyond 2 to 3 kHz. The range of the frequency spectrum covered by the mid-range unit must be restricted to those frequencies at which the displacement of the diaphragm does not exceed the manufacturer's rating.

It should of course be quite clearly understood that the sole purpose of a crossover network is to control the operating range of each speaker. It is to prevent a tweeter with a cone travel of a few thousands of an inch from being driven by a 50 Watt amplifier at 35 Hz - and to ensure that a bass speaker does not have hysterics trying to emulate Victoria de los Angeles.

A crossover network cannot be used to correct for deficiencies in the record player, amplifier, speaker drive units or enclosure design.

#### GRAPHI

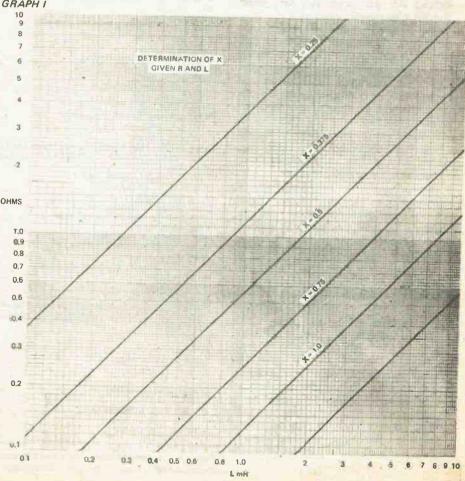
#### **DIFFERENT TYPES OF FILTER**

Figure 1 shows a typical frequency response for a crossover network (operating point 1 kHz) consisting of a low-pass filter and a high-pass filter. The graph does in fact show three different pairs of filters, each having a different rate of attenuation.

In practise an attentuation of 6 dB per octave is generally inadequate. The rate of cut-off is not always sufficient to protect the mid-range and high frequency drive units from being overdriven.

An attenuation rate of 12 dB per octave is commonly used, although 18 dB per octave filters are sometimes chosen. For amateur design it is advisable to stick to the 12 dB per octave filter.

Both series and parallel filters are used. Series filters are used only in two-speaker systems. Most commercially built networks use the parallel configuration because component values are the same for each filter and this reduces inventory costs. Apart from cost the parallel network has slightly better electrical characteristics in the transmission and



attenuation bands. Nevertheless the design data given later in this article covers both series and parallel networks.

Apart from the series and parallel configurations, filters used for crossover networks are known as 'constant k' or 'm derived'. It is not the amateur to for essential understand the difference between the two types. Basically the 'constant k' networks are limited to a cut off rate of 12 dB per octave, whilst the 'm derived' networks can operate at cut off rates of 18 dB per octave. The 'm derived network' is often used by designers of top quality speaker systems as the design approach permits closer control of impedance and attenuation characteristics.

#### **INSERTION LOSS**

One of the most important design considerations is that the filter does not introduce any appreciable loss (this is called 'insertion loss') between the amplifier and the speaker drive units. The insertion loss — which is usually quoted in dBs — is caused by the dc resistance of the coils, together with the shunt and series reactance of the circuit elements. The insertion loss of a well designed filter should not exceed 0.5 dB (preferably less than this for high power systems).

For speaker systems driven by amplifiers of less than 30 Watts or so, an insertion loss of 0.5 dB is quite acceptable. But a manufacturer of high power systems will usually try to reduce the insertion loss below 0.5 dB if economically feasible — for the power absorbed by a 0.5 dB filter at 100 Watts input will exceed 10 Watts.

Insertion losses are minimized by using coils of low dc resistance, and capacitors of low power factor.

(Apart from the insertion loss, a further loss of approx 3 dB will occur at the crossover frequency. This is because the amplifier power is divided more or less equally between the two speakers at this frequency. This loss is inevitable whenever a crossover network is used — but in practise it is hardly ever apparent to the ear.)

Speaker drive units used in multiple speaker systems should all have similar nominal impedances. Thus, if the bass driver is an eight ohm unit so also should be the mid-range (if used) and high frequency units. If twin units are used for any part of the spectrum such as twin tweeters — then each speaker should be twice the nominal impedance of each of the remaining speakers, the twin speakers should then be connected in parallel. (Two 16 SYD 0134 HONEYWELL G265 TIME-SHARING SYD. ON TTY 41 AT 18:52 USER NUMBER--- S8 5004 MODERN MAGAZINE H. PROJECT ID---BARRY SYSTEM---BAS NEW OR OLD--NEW NEW FILE NAME -- FILTERS READY . TAPE READY 15 PRINT USING 18 LS 1.2 1.3 1.4 C1 C2 C3 C4 C5 L.1 18: FREQ. 20 PRINT 35 READ R 37 READ M DIM F(25) 40 FOR I = 1 TO 22 50 READ F(I) 60 70 LET W=2\*3.14159\*F(I) LET Z=R\*W 80 90 LET X=2E6/Z 110 GOSUB 500 120 LET C1=X 130 LET X=1E6/(Z+Z\*M) 150 GOSUB 500 160 LET C2=X 170 LET X=1E6/Z 190 GOSUB 500 195 LET C3=X 200 LET X=1E6/(2\*Z) 220 GOSUB 500 230 LET C4=X 240 LET X=1E6\*(1+M)/Z 255 GOSUB 500 260 LET C5=X 270 LET X=1000\*(1+M)\*R/W 280 GOSUB 500 285 LET L1=X 290 LET X=1000\*R/W 295 GOSUB 500 300 LET L2=X 310 LET X=1000\*R/(2\*W) 320 GOSUB 500 330 LET L3=X 340 LET X=2\*1000\*R/W 3 50 GOSUB 500 360 LET L4=X 370 LET X=1000\*R/(W+W+M) 380 GOSUB 500 390 LET L5=X 450 PRINT F(I); TAB(10); C1; TAB(16); C2; TAB(22); C3; TAB(28); C4; TAB(34); C5; 460 PRINT TAB(40); L1; TAB(46); L2; TAB(52); L3; TAB(58); L4; TAB(64); L5 480 NEXT I 500 IF X<100 THEN 520 505 LET X=INT(X+.5) 510 GOTO 600 520 IF X<10 THEN 540 525 LET X=INT(X\*10+.1)/10 530 GOTO 600 540 IF X<1 THEN 560 545 LET X=INT(X+100+.5)/100 550 GOTO 600 560 LET X=INT(X\*1000++5)/1000 600 RETURN 700 DATA 8 710 DATA 0.6 100, 150, 200, 250, 300, 350, 400, 500, 600, 750, 1000, 1250, 1500 7 20 DATA 730 DATA 2000, 2500, 3000, 3500, 4000, 5000, 6000, 7500, 10000 999 END RIN USED 33 UNITS BYE TOTAL TTY MINUTES = 35 TOTAL CRU'S USED. = 33 \*\*\* OFF AT 19:27

This is the computer programme used to calculate the alrcuit component values in the crossover networks. Copyright – Electronics Today International.

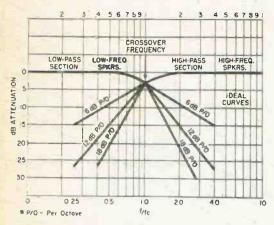


Fig. 1. Typical frequency response curves of a two-way crossover network. The graph shows three different pairs of filters, each having a different rate of attenuation.

ohm speakers connected in parallel will reflect an 8 ohm load impedance to the crossover network.)

#### CALCULATING COMPONENT VALUES

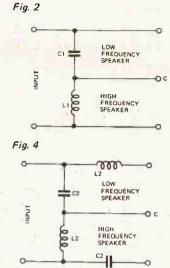
Calculation of the component values for crossover networks is a long tedious business. Unless you have a computer that is!

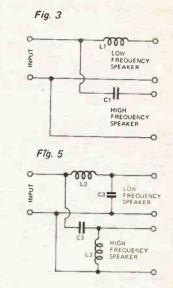
The programme – specially written by our Engineering Manager, Barry Wilkinson – is reproduced elsewhere in this article. Component values have been calculated for both 'constant k' and 'm derived' filters and for speakers of both 8 ohm and 15 ohm nominal impedance; complete design data is given for all crossover frequencies from 1.00 Hz through 10 kHz.

#### CONSTRUCTION

The actual construction of filter networks is quite simple. Air-cored coils are normally used (iron-cored coils can introduce distortion) and these are very simple to wind. (Design data for winding these coils is included in this article.)

Standard (non-polarized) electrolytic capacitors are not suitable for crossover networks, as even low leakage types have an unacceptable power factor for this application. Special non-polarized electrolytics are made by some firms specifically for crossover networks — but it is significant that many of the top speaker manufacturers will only use paper capacitors for this purpose.





Constant k crossover networks. Fig. 2 – series type, 6dB/octave. Fig. 3 – parallel type, 6dB/octave. Fig. 4 – series type, 12dB/octave. Fig. 5 – parallel type, 12dB/ octave.

When choosing capacitors for crossover networks ensure that the capacitors' rated dc working voltage is never exceeded by the peak voltage of the signal.

#### **DESIGN PROCEDURE**

- 1. Determine crossover frequencies and attenuation required (i.e. 6dB, 12dB or 18dB per octave).
- Decide whether filter is to be series or parallel – as explained earlier the parallel type has some advantages over its series counterpart.
- 3. Select the appropriate circuit from Fig. 2 9,

- Establish component values for required speaker impedance (and either 'constant k'' or 'm derived' design) from computer print-out.
- 5. Design coils using data provided.

#### **COIL DESIGN**

Any coil used in a crossover network has a certain amount of dc resistance – and this resistance will dissipate a proportion of amplifier power. Thus, the dc resistance of the coils should be as low as economically possible. A reasonable compromise – where the amplifier power does not exceed 30 Watts continuous power output per

FREQ.	C 1	C2	СЗ	Li	L2	L3
100 150 200 350 350 400 500 600 750 1000 2500 2500 3500 4000 5000 4000 5000 7500	199 133 99.5 79.6 66.3 56.8 49.7 39.8 33.2 26.5 19.9 13.3 9.95 7.96 6.63 5.68 4.97 3.98 3.32 2.65 1.99	281 188 141 113 93.8 80.4 70.3 56.3 46.9 37.5 28.1 22.5 18.8 14.1 11.3 9.38 8.04 7.03 5.63 4.69 3.75 2.81	$ \begin{array}{c} 141\\ 93.8\\ 70.3\\ 56.3\\ 46.9\\ 40.2\\ 35.2\\ 28.1\\ 23.4\\ 18.8\\ 14.1\\ 11.3\\ 9.38\\ 7.03\\ 5.63\\ 4.69\\ 4.02\\ 3.52\\ 2.81\\ 2.34\\ 1.88\\ 1.41\\ \end{array} $	12.7 8.49 6.37 5.09 4.24 3.64 3.18 2.55 2.12 1.7 1.02 .849 .637 .509 .424 .364 .318 .255 .212 1.7 1.02 .849 .637 .509 .424 .318 .255 .212 .17 .127	9 6 4.5 3.6 3 2.57 2.25 1.8 1.5 1.2 .9 .72 .6 .45 .36 .3 .257 .225 .18 .15 .12 .09	18 12 9 7.2 6 5.14 4.5 3.6 3 2.4 1.8 1.44 1.2 .9 .72 .6 .514 .45 .36 .3 .24
						• 18

COMPONENT VALUES FOR CONSTANT-K LOUDSPEAKER CROSSOVER NETWORKS INEUCTANCE IN MILLIHENRIES CAFACITANCE IN MICROFARADS SPEAKER IMPEDANCE = 8 OHMS

channel – is to keep the dc resistance below one ohm.

The coil design that will provide the highest inductance in proportion to the dc resistance is that shown in Fig. 10. In this drawing the radius of the circular winding bobbin is shown as 'x' and all other dimensions are related to this.

Construction of the bobbin is not critical and it can be made from cardboard, or a combination of a wooden core and cardboard cheeks. Metal must not be used.

- The design procedure is as follows:- TURNS (N) 1. Determine the bobbin size required.
- This is done by using Graph I. This graph indicates bobbin size ('x' measurement) required to accommodate coils of different sizes and dc resistances. For example a 5.5mH coil wound on a 0.75" former (remember that this refers to the measurement shown as 'x') will have a dc resistance of 1.4 ohms - if wound on a 1" former the resistance would be 0.7 ohms. As the dc resistance should be preferably less than 1.0 ohm, the " former should be used.
- Graph II shows the number of turns required to provide the required inductance for various bobbin sizes. In our example 290 turns are required.
- 3. Graph III shows the wire gauge required. In our example 290 turns on a 1" bobbin would require 15.3 B&S. The nearest standard size is 16G so this is the wire size used.
- 4. The coil should be layer wound using enammeled copper wire. As the operating voltage is quite low, no interlayer insulation is required. Graph IV shows the dc resistance of

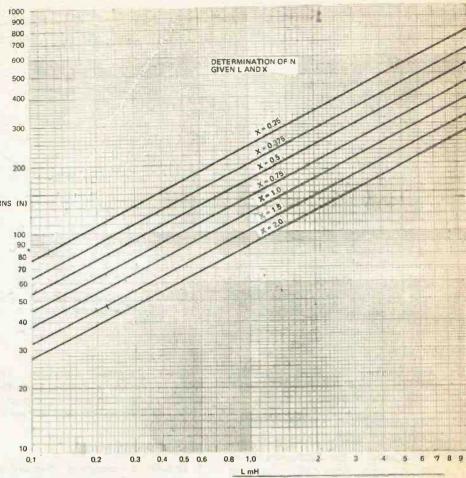
the coil given the wire gauge and former size, providing the former is filled completely. In our case the resistance shown is 1.0 ohm — but as we have only 290 turns whereas the filled bobbin accommodates about 350 turns the resistance would be about 0.8 ohm. This is sufficiently close to our design requirement and would be acceptable for a low power amplifier.

Figure 11 provides the approximate weight of wire used for fully wound coils of each size.

#### THREE-WAY CROSSOVER NETWORKS

These differ from two-way networks only in that they include a mid-range filter.

A three-way 12 dB per octave parallel crossover is shown in Fig. 12.



The midrange section is a bandpass filter consisting of a low pass filter (L3B and C3B) and a high pass filter (L3A and C3A).

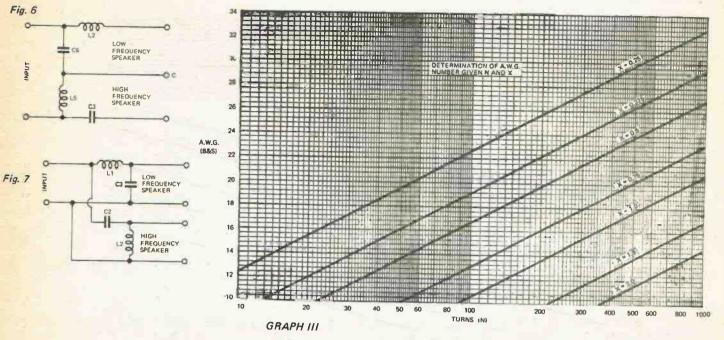
The design procedure is firstly to establish the values of the low pass section L3 and C3. Circuit elements L3A and C3A, in the mid-range filter, must also cross over at the same frequency as the low pass filter, and thus have the same values as L3 and C3.

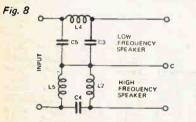
The values of L3B is the same as L3C as also are C3B and C3C. The values of

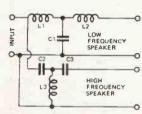
FREQ.	C1	C2	C3	LI	L2	L3
100	106	150	75	23,.9	16.9	33.8
150	70.7	100	50	15+9	11.3	22.5
200	53 • 1	75	37 . 5	11.9	8.44	16.9
250	42.4	60	30	9 . 55	6.75	13.5
300	35.4	50	25	7.96	5.63	11.3
350	30+3	42.9	21.4	6.82	4.82	9.65
400	26.5	37 • 5	18.8	5.97	4.22	8.44
300	21.2	30	15	4.77	3 . 38	6.75
600	17.7	25	12.5	3.98	2.81	5.63
750	14+1	20	10	3 • 18	2.25	4.5
1000	10.6	15	7.5	2.39	1 . 69	3 . 38
1250	8 • 49	12	6	1-91	1.35	2.7
1500	7.07	10	5	1 • 59	1.13	2.25
2000	5.31	7.5	3.75	1 • 19	.844	1.69
2500	4.24	6	3	•955	.675	1.35
3000	3 • 54	5	2.5	• 79 6	. 563	1+13
3500	3.03	4.29	2.14	• 682	.482	.965
4000	2.65	3.75	1.88	• 59 7	.422	.844
5000	2.12	3	1 + 5	• 477	.338	.675
6000	1.77	2.5	1.25	• 39 8	- 28 1	- 563
7500	1 • 41	5				

COMPONENT VALUES FOR CONSTANT-K LOUDSPEAKER CROSSOVER NETWORKS INDUCTANCE IN MILLIHENRIES CAPACITANCE IN MICROFARADS

SPEAKER IMPEDANCE = 15 OHMS







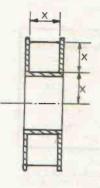


Fig. 10. Recommended dimensions of bobbin design. All dimensions are related to 'x' - thus if the measurement specified for 'x' is 1" then the winding width and depth are both 1' and the bobbin internal diameter is 2".

M-derived crossover networks. Fig. 6 – series type, 12 dB/octave. Fig. 7 – parallel type, 12 dB/octave. Fig. 8 – series type, 18 dB/octave. Fig. 9 – parallel type, 18 dB/octave.

Fig. 9

these components are determined for the changeover frequency of the mid-range and tweeter speakers.

Four and five way networks are designed in a similar fashion.

The component values quoted for the three way 'constant k' 'network described above can be converted to an 'm derived network' by the following equations.

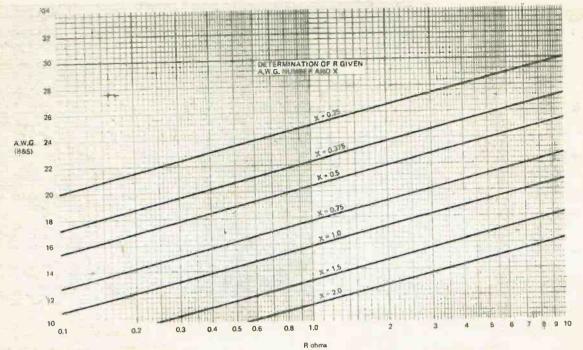
L3, L3B = 
$$(1 + m) \frac{R_o}{\omega c}$$
 Henry  
L3A, L3C =  $\left(\frac{R}{\omega c}\right)$  Henry  
C3A, C3C =  $\left(\frac{1}{1+m}\right) \left(\frac{1}{\omega c R c}\right) \times 10^6 \mu F$   
C3B =  $\left(\frac{10^6}{\omega c R c}\right) \mu F$ 

Electronics Today International would like to thank Mr LC. Hansen for his very valuable assistance in providing design data for the coils described in this article.

FREQ.	C1	C2	C3	C4	C 5	L 1	L2	L3	L4	L5
FREQ- 100 220 250 300 350 400 500 600 750 1000 1250 2500 2500 3500	C1 398 265 199 159 133 114 99 79 66 53 39 31.8 26.5 19.9 15.9 13.2 11.5	124 82.9 62.1 49.7 41.4 35.5 24.8 3 20.7 12.4 8 9.95 6 8.29 6.22 4.97 2 4.14	C3 199 133 99.4 79.55 66.3 56.8 49.7 33.1 26.5 19.9 15.9 13.2 9.95 7.96 6.63 5.68	C4 99.4 66.3 49.7 33.1 28.4 24.8 19.9 16.5 13.2 9.95 7.96 6.63 4.97 3.98 3.32 2.84	C5 318 212 159 127 106 90.9 79.5 63.6 53 42.4 31.8 25.4 21.2 15.9 12.7 10.6 9.09	L1 20.3 13.5 10.1 8.15 6.79 5.82 5.09 4.07 3.4 2.72 2.04 1.63 1.36 1.02 .815 .679 5.82	12.7 8.49 6.37 5.09 4.24 3.64 3.18 2.55 2.12 1.7 1.27 1.27 1.02 .847 .509 .424	6.37 4.24 3.18 2.55 2.12 1.82 1.59 1.27 1.06 .849 .637 .509 .424 .318 .255 .212	25.4 16.9 12.7 10.1 8.49 7.28 6.37 5.09 4.24 3.4 2.55 2.04 1.7 1.27 1.02 .849	7.96 5.31 3.98 3.18 2.65 2.27 1.99 1.59 1.33 1.06 .637 .531 .398 .318 .265
4000	9.95	3 • 11	4.97	2.49	7.96	• 509	• 364 • 318	• 18 2 • 1 59	• 728 • 637	• 227 • 199
6000 7500	6•63 5•31	2.07	3.32	1.66	5.31	• 407 • 34 • 272	•255 •212 •17	• 127 • 106 • 08 5	• 509 • 424 • 34	•159 •133 •106
10000	3.98	1.24	1.99	.995	3 - 18	• 204	• 127	• 0 6 4	.255	• 08

COMPONENT VALUES FOR M-DERIVED LOUDSPEAKER CROSSOVER NETWORKS INDUCTANCE IN MILLIHENRIES CAPACITANCE IN MICROFARADS M=0.6 SPEAKER IMPEDANCE = 8 OHMS

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GRAPH	111
-------	-----

'x' inches	Weight (ozs.)
0.25	0.5
0.375	1.75
0.5	4.25
0.75	14
1.00	33
1.50	110
1000 1000 500	

Fig. 11 – This table shows the weight of wire used for fully wound coils of each size of 'x'.

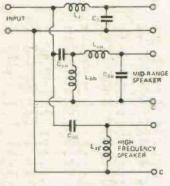


Fig. 12. Three-way 12 dB per octave parallel crossover.

FREQ.	C 1	CS	C3	C4	C 5	L1	L2	L3	L4	L,S
100 150 200 250 350 400 500 600 750 1000 1250 1500 2500 3000 2500 3000 3500	$\begin{array}{c} 212\\ 141\\ 106\\ 84.8\\ 70.7\\ 60.6\\ 53\\ 42.4\\ 35.3\\ 28.3\\ 28.3\\ 28.3\\ 21.2\\ 16.9\\ 14.1\\ 10.6\\ 8.49\\ 7.07\\ 6.06\\ 5.31\\ 4.24 \end{array}$	66.3 44.2 33.1 26.5 22.1 18.9 16.5 13.2 11 8.84 6.63 5.31 4.42 2.65 2.21 1.89 1.66 1.33	106 70-7 53 42-4 35-3 30-3 26-5 21-2 17-6 14-1 10-6 8-49 7-07 5-31 4-24 3-54 3-54 3-54 3-63 2-65 2-12	53 $35 \cdot 3$ $26 \cdot 5$ $21 \cdot 2$ $17 \cdot 6$ $15 \cdot 1$ $13 \cdot 2$ $10 \cdot 6$ $8 \cdot 84$ $7 \cdot 07$ $5 \cdot 31$ $4 \cdot 24$ $3 \cdot 545$ $2 \cdot 12$ $1 \cdot 77$ $1 \cdot 52$ $1 \cdot 77$ $1 \cdot 52$ $1 \cdot 33$ $1 \cdot 06$	170 113 84.8 67.9 56.5 48.5 42.4 33.9 28.3 22.6 16.9 13.5 11.3 8.49 6.79 5.66 4.85 4.24 3.4	38 • 2 25 • 4 19 • 1 15 • 2 12 • 7 10 • 9 9 • 55 7 • 64 6 • 37 5 • 09 3 • 82 3 • 06 2 • 55 1 • 91 1 • 53 1 • 27 1 • 09 • 9 • 55 7 • 64 6 • 37 5 • 09 3 • 82 3 • 06 2 • 55 1 • 91 1 • 53 1 • 27 1 • 09 • 9 • 55 7 • 64 6 • 37 5 • 09 3 • 82 3 • 06 2 • 55 1 • 91 1 • 53 1 • 27 1 • 09 • 95 5 • 76 6 • 76 6 • 77 5 • 99 5 • 76 6 • 77 6 • 77 7 • 64 7 • 70 7 • 64 7 • 70 7 • 64 7 • 70 7 •	$\begin{array}{c} 23.8\\ 15.9\\ 11.9\\ 9.55\\ 7.96\\ 6.82\\ 5.97\\ 4.77\\ 3.98\\ 3.18\\ 2.39\\ 1.91\\ 1.59\\ 1.91\\ 9.55\\ .796\\ .682\\ .597\\ .477\end{array}$	11-9 7-96 5-97 4-77 3-98 2-39 1-99 1-99 1-19 -955 -796 -597 -477 -398 -341 -298 -239	47.7 31.8 23.8 19.1 15.9 13.6 11.9 9.55 7.96 6.37 4.77 3.82 2.39 1.91 1.59 1.36 1.19 9.55 7.96	14.9 9.95 7.46 5.97 4.97 4.97 4.97 4.97 4.97 4.97 4.97 4
6000 7500 10000	3 • 54 2 • 8 3 2 • 12	1 • 1 1 • 88 4 • 663	1 • 77 1 • 41 1 • 06	•884 •707 •531	2.83 2.26 1.7	• 637 • 509 • 382	• 398 • 318 • 239	• 199 • 159 • 119	· 637 · 477	· 199 · 149

COMPONENT VALUES FOR M-DERIVED LOUDSPEAKER CROSSOVER NETWORKS INDUCTANCE IN MILLIHENRIES CAPACITANCE IN MICROFARADS M=0.6

SPEAKER IMPEDANCE = 15 OHMS

## BATTERIES

1	System	Anode	Cathode	Electrolyte	Open current voltage,	Typical operating yoltage,		apacity <sup>a</sup> Wh/I	
	Primary systems Leclanche	Zn (Hợ)	MnO <sub>2</sub> (C)	NH4CI-ZnCI2	1.6	0.9-1.4	23	30	most common form of the dry
	Alkaline Zn-MnOz	Zn(Hg)	MnO <sub>2</sub> (C)	кон	1.52	0.9-1.2	30	33	cell; extensive applications; sloping discharge curve suitable for greater drain rates
ŕ	nercury cell (Rubin),	Zn(Hg)	HgO(C)	KOH-ZnO	1.35	1.30	40	53	than Leclanche cells; sloping discharge curve constant voltage during discharge; heavier drains and higher
r	Mg-MnO2	Mg	MnO <sub>2</sub> (C)	MgBr <sub>3</sub> , Li <sub>2</sub> CrO <sub>4</sub>	2.0	1. <mark>6-1.8</mark>	30	46	capacity than Leclanche cells higher capacity and voltage than Leclanche cell; 35-40% of magnesium consumed in hydrogen liberation during
a	ir-depolarised Zn	Zn (Hg)	0 <sub>2</sub> (C)	КОН	1.36	1.1-1.2	60 <sup>b</sup>	70 <sup>b</sup>	discharge utilizes oxygen from air; wet type used for railway signals, home radios; dry type available but
Z	n-AgO	Zn	AgO	кон	1.8	1.4-1.5	35	53	moisture loss a problem one-shot, high-drain-rate reserve cell; also available in another
Z	n-PbO <sub>2</sub>	Zn	PbO2	H <sub>2</sub> SO <sub>4</sub>	2.5	2.0-2.3	18	26	form as a secondary battery one-shot, high-drain-rate reserve
Z	n-CuO	Zn(Hg)	CuO	NaOH	1.06	0.9-1.0			cell low operating voltage; used
	n-Cl <sub>2</sub> b-PbO <sub>2</sub> -HClO <sub>4</sub>	Zn Pb	ZnCl <sub>2</sub> PbO <sub>2</sub>	CI2 HCIO4	2.1 2.0	1.5-1.9 1.6-1.8	11	19	principally for railway signals one-shot, high-drain-rate cell one-shot, high-drain reserve types
th	ermal cell	Ċa	PbCrO4(Ni)	LICI, KC1 fused	2.8	2.2			used for military applications must be heated to melt
									electrolyte, one-shot, high-drain, military type cell
IV	lg-Cu <sub>2</sub> Cl	Mg	Cu <sub>2</sub> Cl	MgCl <sub>2</sub>	1.4	1.1-1.3	25	30	one-shot, high-drain reserve cell; may be activated with sea
M	lg-AgCl	Mg	AgCI	MgCl2	1.6	1.3-1.5	54	75	water one-shot, high-drain reserve cell with very high capacity; may
Z	n-V <sub>2</sub> O <sub>3</sub>	Zn	V <sub>2</sub> O <sub>3</sub>	NH4 OH, ethylene glycol, boric acid	1.2	1.2			available commercially as a blas cell providing stable voltage at
	leston standard	Cd(Hg)	Hg	HgSO <sub>4</sub> , CdSO <sub>4</sub>	1.019	1.2			zero current over long periods used as a voltage standard
.SO	lid electrolyte	Ag	CuBr <sub>2</sub>	AgBr	0.75				power source for radiation warning devices; charging source for low-leakage
Fe	ry cell	Zn	0 <sub>2</sub> (C)	NH <sub>4</sub> Cl	1.2	0.7			capacitors used extensively in foreign countries for telegraphy and
Źn	o-AgrO	Zn	Ag <sub>2</sub> O	KOH or NuOH	1.6	1.5	33	49	telephone service; performs efficiently at low drains small sealed primary cell for electric wrist watch or hearing
In-	·HgO	In	HgO	КОН	1.15	1.05			aid use; hermetically sealed
(pi	(perimental cells rimary) organic thode	Mg	<i>m-</i> dinitro- benzene	MgBr <sub>2</sub>	1.65	1.15 <sup>d</sup>	56	65	hermetically sealed une of the more promising of a large number of organic
	id electrolyte	Ag	¥203	4.1					compounds being considered; multistep discharge
			•203	Agi	0.46	0.38-0.46 <sup>d</sup>			typical of a variety of similar systems that could be made commercially if applications warranted: thin flat cells
Al-	MnO <sub>2</sub>	AL	MnO <sub>2</sub>		24				providing 100 V/in. of battery length
	-2		MI102	AICI3,(NH4)2Cr2O7	1,7	1.3			higher capacity and voltage than Leclanche cell; wasteful corrosion of aluminium
Mg	-Bi <sub>2</sub> O <sub>3</sub>	Mg	Bi <sub>2</sub> O <sub>3</sub>	MgBr <sub>2</sub>	1.6	1.0	6		remains a major problem operates 0.2-0.3 V lower potential than HgO-Zn system but otherwise has similar
lead	ondary cells d acid son			H₂SO₄ KOH	2.2 1.6	1.95-2.05 1.2-1.4	10 10	20 13	voltage-time discharge characteristics conventional lead storage cell much longer useful life than lead
		Cd	Ni oxides	кон	1.35	1110	10		storage cell but lower capacity and more expensive
	NIO			KOH, ZnO	1.35	1.1-1.3	10		cell sealed
	AgO				1.8	1.4-1.5	35	53 v	rery high capacity and suitable for high discharge rates but smaller number of cycles than
		Cd	AgO I	КОН	1.4	1.0-1.1	30	33 9	NI-Cd or lead storage cells reater number of cycles than
				КОН	1.5		8		vailable only as a completely
3 80	ssed on total weight of	commonly	y available size	of commercial cells.					sealed cell

a Based on total weight of commonly available size of commercial cells. b Exclusive of O2 consumed from air. c Average voltage for light-drain application, d 2 X 10-10 A/in.2 drain for the first 7 yr of cell life.

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## **CONVERSION TABLES-**

-	8		7		6	1	5		4	3		2		1	
Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal
0	0	0	0	0	0	0	0	0	0	0	0	0	.0:	0	0
1	268,435,456	1	16,777,216	1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	536,870,912	2	33,554,432	2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	805,306,368	3	50,331,648	3	3 145,728	3	196.608	3	12,288	3	768	3	48	3	3
4	1.073,741,824	4	67:108,864	4	4,194,304	4	262,144	4	16.384	4	1,024	4	64	4	4
5	1,342,177,280	5	83,886,080	5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	1,610,612,736	6	100,663,296	6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	1,879,048,192	7	117,440,512	7	7,340,032	-7	458,752	7	28,672	7	1,792	7	112	7	7
8	2,147,483,648	8	134,217,728	8	8,388,608	8	524,288	8	32,768	8	2.048	8	128	8	8
9	2,415,919,104	9	150,994,944	9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	2.684,354,560	A	167,772,160	A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
В	2,952,790,016	8	184,549,376	В	11,534,336	8	720,896	8	45,056	В	.2,816	В	176	8	11
G	3,221,225,472	С	201,326,592	С	12,582,912	С	786,432	C	49,152	С	3,072	C	192	C	12
D	3,489,660,928	D	218,103,808	D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	3,758,096,384	E	234,881,024	E	14,680.064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	4,026,531,840	F	251.658,240	F	15,728.640	F	983,040	F	61,440	F	3,840	F	240	F	15
-	8		7		6		5		4		3		2	_	İà

#### TO CONVERT HEXADECIMAL TO DECIMAL

- Locate column of decimal numbers corresponding to left-most digit or letter of hexadecimal select from this column and record number that corresponds to position of hexadecimal digit or letter. 1
- Repeat step 1 for next (second from left) position. Repeat step 1 for units (third from left) position. 2
- 3 Add numbers selected from table to form decimal number. 4

#### TO CONVERT DECIMAL TO HEXADECIMAL

- (A) select from table highest decimal number that is equal to or less than number to be converted. 1
- 2
- than number to be converted. (B) Record hexadecimal of column containing selected number. (C) Subtract selected decimal from number to be converted. Using remainder from step 1 (C) repeat all of step 1 to develop second position of hexadecimal (and remainder). Using remainder from step 2 repeat all of step 1 to develop units position of hexadecimal. Combine terms to form hexadecimal number. 3 л

#### Decimal-Hex-Octal-Binary-ASCII

Dec Octal Hex Pattern 7 6'5 4 3 2 1	ASCII Character	7 6 5 4 3 2 1 7 6 5 4 3 2 1	ASCII haracter
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	Special Characters SEACE	$7654321$ $7654321$ 43         53         2B         0 1 0 1 0 1 1 1         +         86         126         56         1 0 1 0 1 1 1           44         54         2C         0 1 0 1 1 1 0 1         -         87         127         57         1 0 1 0 1 0 1 1         1 0 0 0           46         56         2D         0 1 0 1 1 1 0         -         88         130         58         1 0 1 1 0 0 0         1           47         57         2F         0 1 0 1 1 1 0         -         89         131         59         1 0 1 1 0 1 0         1           48         61         31         0 1 1 0 0 0 0 $\phi$ 91         133         5B         1 0 1 1 0 1 0         1           49         61         31         0 1 1 0 1 0 0         4         95         137         5F         1 0 1 1 1 1 0         1           53         66         36         0 1 1 1 0 1 0         5         96         140         60         1 0 0 0 0         0           54         66         36         0 1 1 0 1 0 1         1 0 1 0         1 0 1 0 0         1 0 0 0 0 0         1 0 0 0 0 0           55         67         37 <t< td=""><td>VWXYZ[//]↑↓ abcdefghijklmnopqrstuvwxyz  </td></t<>	VWXYZ[//]↑↓ abcdefghijklmnopqrstuvwxyz
41 51 29 0 0 1 0 1 0 0 1 42 52 2A 0 1 0 1 0 1 0		85 125 55 1 0 1 0 1 0 1 U — means special characters or co	des not used.

ETI CIRCUITS Na. 24

#### **CMOS/TTL COMPARISON**

Logic family	Noise Immunity Volts	Prop. delay nS	Fan Out	Max. Toggle Speed MHZ		upply Volt ninal Min. V		Power Diss. per package mW (typ)	Decoupling and other requirements
74 Series 74H Series 74S Series 74LS Series CMOS	0.4 0.4 0.3 0.3 4.5	9 6 3 9 30	10 10 10 10 >50	125	5.0 5.0 5.0 5.0	4.75 4.75 4.75 4.75 3.0	5.25 5.25	60 40 8	0.1 uF Ceramic capacitor for every 8 packages to eliminate switchingcurrentspike No special precautions

#### TTL BIPOLAR LOGIC

The 74 Series of transistor-transistor logic is a medium speed family of saturating integrated circuit logic designed for general digital logic application requiring clock frequencies to 30MHz and switching speeds in the 7-11 nS range under moderate capacitive loading.

The circuits are identified by a multiple emitter input transistor and an active "pull up" in the upper output network. Clamp diodes are provided at each input to limit the undershoot that occurs in typical system applications such as driving long that occurs in typical system applications such as driving long interconnect wiring. The active pull-up output configuration provides low output impedance in the high output state. The resulting low impedances in both output states ensures excellent a.c. noise immunity and allows a high-speed operation with capacitive loads.

#### COMPLEMENTARY MOS (CMOS)

LOGIC DATA-

Complementary MOS is the newest of the general-purpose logic families

The following are primary design features of the whole of the COS/MOS and McMOS ranges.

Double diode protection on all inputs.

Noise immunity typically 45% of VDD, 30% of VDD minimum.

\_

Buffered output compatible with MHTL and Low Power TTL. Low quiescent power dissipation: 25nW typ. per package. Wide power supply voltage: 3-18 Volt dependent on type. \_

Single supply operation. \_

High fanout: greater than 50 High input impedance: 10<sup>15</sup> ohms typ. Low input capacitance: 5pf typ.

#### **TTL FUNCTIONS**

Device	Description	7481	10 Ma Astron El contra del
7400	Quad 2-input Positive NAND Gate	7481	16-bit Active Element Memory
7401	Quad 2-input Positive NAND Gate (open collector o/ p)	7484	2-bit Binary Full Addder
7401A	Quad 2-input Positive NAND Gate (open collector o/p)	7485	16-bit Active Element Memory
7402	Quad 2-input Positive NOR Gate (open collector o/p)	7486	4-bit Comparator
7403	Quad 2-input Positive NAND Gate (open collector o/p)		Quad 2-input Exclusive Or Gate
7404	Hex Inverter	7489	64-bit RAM (16 x 4W)
7405A	Hex Inverter (open collector o/p)	7490	Decade Counter
7406	Hex Inverter / Buffer 30V o/p	7491	8-bit Shift Registers
7407	Hex Buffer 30V o/p	7492	Divide-by-twelve Counter
7408	Quad 2-input Positive AND Gate	7493	4-bit Binary Counter
7409	Quad 2-input Positive AND Gate	7494	4-bit Shift Registers (Parallel-In, Serial-Out)
7410	Triple 3-input Positive NAND Gate	7495	4-bit Right Shift, Left Shift Register
7412	Triple 2 input NAND Cate	7496	5-bit Shift Registers (Dual Para-in, Para-Out)
7413	Triple 3-input NAND Gate (open collector o/p) Dual 4-input Schmitt Trigger	74100	8-bit Bistable Latch
7414	Schmitt Hex Inverter Buffer	74107	Dual J-K Master Slave Flip Flop
7416	How Inverter / Putter 1 St	74121	Monostable Multivibrator
7417	Hex Inverter / Buffer 15V o/p	74122	Monostable Multivibrator with reset
7420	Hex Buffer 15V o/p	74123	Dual Monostable Multivibrator with reset
7421	Dual 4-input Positive NAND Gate	74124	Universal Pulse Generator
7426	Dual 4-input AND Gate	74138	3 line to 8 line Decoder / Demultiplexer
7427	Cuad 2-input High Voltage Interface NAND Gate	74141	BCD-to-Decimal Decoder / Driver
7428	Triple 3-input NOR Gate	74145	BCD-to-Seven Segment Decoder / Driver 15V output
7430	Quad 2-input NOR Buffer (Fan Out 30)	74150	16-bit Data Selector
7432	8-input Positive NAND Gate	74151	8-bit Data Selector (with strobe)
7433A	Quad 2-input OR Gate	74153	Dual 4 to 1 line Data Selector 1 MPX
7437	Quad 2-input NOR Buffer 15V	74154	4 line to 16 line Decoder
7438A	Quad 2-input NAND Buffer	74155	Dual 2-to-4 line Decoder / DeMPX (totem pole output)
7441A	Quad 2-input NAND Buffer 15V	74156	Dual 2-to-4 line Decoder / DeMPX (open collector output)
7442	BCD-to-Decimal Decoder / Nixie Driver	74157	Quad 2 line to 1 line Selector
7445	BCD-to-Decimal Decoder	74160	Synchronous Decade Counter
7446A	BCD-to-Decimal Decoder / Driver 30V output o/c	74162	Synchronous Decade Counter
7447	BCD-to-Seven Segment Decoder/Driver 30V/40mA	74163	Synchronous Binary Counter
7447A	BCD-10-Seven Segment Decoder/Driver 15V/20mA	74164	8-bit Shift Register, Serial In-Parallel Out
7448	BCD-to-Seven Segment Decoder/Driver 15V/40mA	74165	8-bit Shift Register, Parallel In-Serial Out
7450	BCD-to-Seven Segment Decoder / Driver	74174	Hex Type "D" Flip Flop
7451	Expandable Dual 2 wide, 2 i/p AND-OR-INVERT Gate	74175	Quad "D" Flip Flop with common reset
7453	Dual 2 wide, 2 i/p AND-OR-INVERT Gate	74180	8-bit Odd/ Even Parity Generator / Checkers
7454	Expandable 4 wide, 2 i/p AND-OR-INVERT Gate	74181	4-bit Arithmetic Logic Out
	4 wide 2-input AND-OR-INVERT Gate	74182	Carry-Look-Ahead Unit
7460	Dual 4-input Expander	74190	Synchronous Up/Down Decade Counter (Single Cluck Unit)
7470	Positive Edge-triggered J-K Flip Flops	74191	Synchronous Up/Down 4-bit Binary Counter
7472	J-K Master-Slave Flip Flops (AND inputs)	74192	Synchronous 4-bit Up/ Down Counter
7473	Dual J-K Master Slave Flip Flops	74193	Synchronous 4 bit Up / Down Counter
474	Dual D-Type Edge Triggered Flip Flops	74195	Synchronous 4-bit Up/Down Counter
475	4-bit bistable latch = Quad bistable latch	74195	Synchronous 4-bit Parallel Shift Register with J-K Inputs
476	Dual J-K Master Slave Flip Flops + preset and clear	74200	50Mhz Presettable Decade Counter / Latch (Bi-Quinary)
		74200	256-bit Random Access Memory (RAM)

## LOGIC DATA

#### **CMOS FUNCTIONS**

Device	Description		Diff
CD4000	Dual 3-Input NOR gate plus Inverter	CD4052	Differential 4-Channel Multiplexer
CD4001	Quad 2-Input NOR Gate	CD4054	4-Line Liquid Crystal Display Driver
CD4002	Dual 4-Input NOR Gate	CD4056	BCD-7-Segment Decoder/Driver
CD4006	18-Stage Static Shift Register	CD4059	Programmable Divide-by-N Counter
CD4007	Dual Complementary Pair Plus Inverter	CD4060	14-Stage Counter and Oscillator
CD4008	4-Bit full Adder with Parallel Carry	CD4061	256-Word X 1-Bit Static Ram
CD4009	Hex Buffer / Converter (Inverting)	CD4066	Quad Bilateral Switch
CD4010	Hex Buffer/Converter (Non-Inverting)	CD4068	8-Input NAND Gate
CD4011	Quad 2-Input NAND Gate	CD4069	Hex Inverter
CD4012	Dual 4-Input NAND Gate	CD4070	Quad Exclusive OR Gate
CD4013	Dual D' Flip-Flop with Set/Reset	CD4071	Quad 2-Input OR Gate
CD4014	8-Stage Static Shift Register	CD4077	Quad Exclusive NOR Gate
CD4015	Dual 4-Stage Static Shift Register	CD4081	Quad 2-Input AND Gate
CD4015	Quad Bilateral Switch	CD4082	Dual 4-Input AND Gate
	Decade Counter/Divider	CD4085	Dual 2-Wide 2-Input AOI Gate
CD4017	Presettable Divide-By-''N'' Counter	CD4086	Expendable 4-Wide 2-Input AOI Gate
CD4018	Quad AND-OR Select Gate	CD4093	Quad 2-Input NAND Schmitt Trigger
CD4019		CD4099	8-Bit Addressable Latch
CD4020	14-Stage Binary Ripple Counter	CD4510	BCD UP/DOWN Counter
CD4021	8-Stage Static Shift Register	CD4511	BCD TO7-Segment Decoder / Driver
CD4022	Divide-by-8 Counter / Divider	CD4514	1 to 16 Decoder (Output High)
CD4023	Triple 3-Input NAND Gate	CD4515	1 to 16 Decoder (Output Low)
CD4024	7-Stage Binary Counter	CD4516	Binary UP/DOWN Counter
CD4025	Triple 3-Input NOR Gate	CD4518	Dual BCD UP Counter
CD4026	Decade Counter / Divider	CD4528	Dual Retriggerable Monostable
CD4027	Dual J K Master Slave Flip-Flop	MC14502	Strobed Hex Inverter / Buffer
CD4028	BCD TO-Decimal Decoder	MC14517	Dual 64-bit Static Shift Register
CD4029	Presettable Up/Down Counter		The second
CD4030	Quad Exclusive-OR Gate	MC14521	24 State Frequency Divider
CD4035	4-Stage Parallel IN/OUT Shift Register	MC14522	Programmable divide by N-4 bit Counter (BCD)
CD4040	12-Stage Binary Ripple Counter	MC14526	Programmable divide by N-4 bit Counter (binary)
CD4042	Quad Clocked "D" Latch	MC14534	Real Time 5-Decade Counter
CD4046	Micropower Phase-Locked Loop	MC14536	Programmable Timer
CD4049	Hex Buffer/Converter (Inverting)	MC14543	BCD-to-Seven Segment Latch / Decoder / Driver
CD4050	Hex Buffer/Converter (Non-Inverting)	MC14553	Three-Digit BCD Counter
CD4051	Single 8-Channel Multiplexer	MC14566	Industrial time base Generator



By popular demand we have designed higher powered versions of our well known modules. The CE 1704 which gives 170W into 4 ohms and the CE 1708 which gives 170W into 8 ohms are physically similar to the onginal types and have the same combination of compatible performance features which makes CRIMSON amplification audiby superior to the competition and the only choice if you have an ear for music. We have also produced suitable power supplies which again use our superto TOROIDAL TRANSFORMERS, only 50mm high, with a 120-240 primary and single bolt fixing.

Write of phone for more information and biased opinion	Nrite of	phone h	or more	information	and	biased	opinion
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POWER AMPLIFIER MODULES	Home	Europe	T.H.O.	Typically <.02%
CE 608 60W/8 phms 35-0-35Y	£16.30	£16.60		any power. littz. 8
CE 1004 100W/4 ohms 36-0-35Y	£19.22	£19.30	T	Charles .
CE 1008 100W /8 etims 45-0-45V	. 123.22	£23.00	TLD: Sine Rate Limit	: lesignificant ; 20V/µS
	£29.12		S/N flatie	: 11048
CE 1708 170W/8 0hms 60-0-60V	. £31,90	£31.04	Freg. Réspense	: 10Hz-35kHz,
TOROIDAL POWER SUPPLIES			cond- machanes	-348
CFS 1 for 2 x CE 608 or 1 x CE 1004	\$14.47	£18.40	Stability	: Unconditional
CPS 2 tor 2 x CE 1004 2/4 x CE 508		\$20.57	Pretection	.: Brives any load
CPS 3 for 2 x CE 1008 or 1 x CE 1704		£21.35		safety
CFS 4 for T x CE 1008		£19.18	Sessitivity	: 775m¥ (250m¥ er
CPS 5 for 1 x CE 1708	. 122.68	£26.50		100mV on Request
CPS 5 for 2 x CE 1704 or 2 x CE 1709		£27.70	Size	: 120 x 80 x 25mm
HEATSINKS				
Light Daty 50mm 2 C/W	£0.90	E1.30	CRI	MSON
Medium Power 100mm 1,4 C/W	E1.60	£2.40		
Bisco/Broup 150mm J.P.C/W	A E2.30	£3.65	ELE	KTRIK
THERMAL CUT-OUTS				ar new address and
Recommended for improved reliability,				er: Stamford House.
70 C for use with free hir heatsink	\$1.60	E1.90		Leicaster LE1 BNL.
400 For use with fan cooled heatsink			Telephane (0533)	
and the second				
Home prices include V A 1 and 1 problem European prices include ca				

Profilem European prices include carriage. Insurance and handling, payment in Starling by bank draft, P.O., International Giro or Money Order. Outside Europe, please write for specific guote by return. Send SAE or two International Reply Coupons for full Internative. Favourable trade quantity price list on request. High quality pre-amp circuit 20p

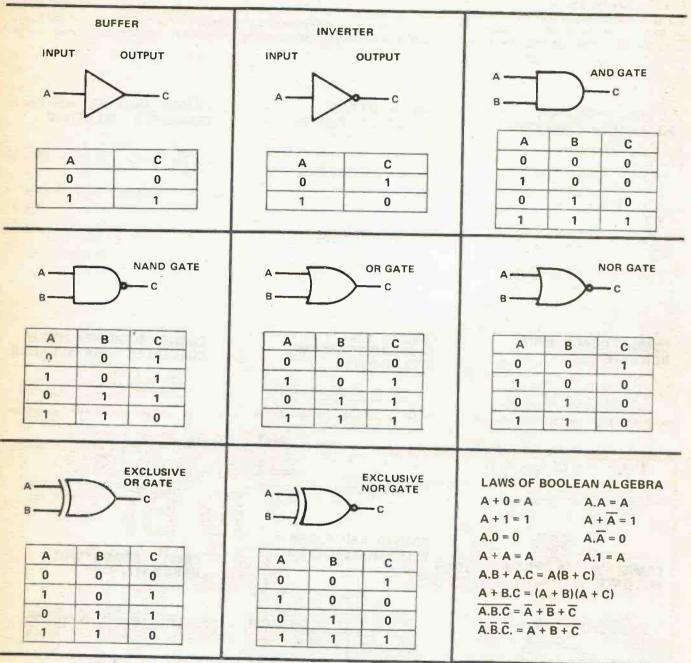
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## DETAILS INSIDE BACK COVER

1	DELTA DELTA
	DISPLAYS: '%" Red LED FND 500 £1.20 each. 6 for £6.48 NSB5LL30 '4'' Red stick of 4 £4.32, 5LT02 stick of 4 Green £5.40
	CLOCK CHIPS: MK50253N Alarm 12/24 hr 4/6 dig E5.40. MM5385 E4.32. MK50362N Calendar E7.56.6 Digit Counter 50395/6/7 E9.18.
2	MICRO PROCESSORS: 280 CPU £21.60. CTC & PIO £15.12. MK4096N 300nS-4K & 1 Dyn RAM £6.75. 1702A UV PROM 450nS £10.80.
	BATTERY RECHARGER SET: Merns Adaptor with 4 way plug, 4 x AA(1).2V) NICeds plus holder £8.64, AA NiCads separately £1.20.
	BARON (ET) 6 GOWER ROAD, ROYSTON, HERTS Tel. (0763) 43695 Use Access and Barclaycard

#### **TRUTH TABLES**

T



J.K. Flip F CLR

CLK

Flop							
		INPUTS			OUTPUT	S	7.
1 -	CLR	CLK	J	K	Q	ā	1
Þā	0	X	X	X	0	1	Qo
-0	1	л	0	0	Qo	Qo	1
•	1	л	1	0	1	0	1
1.3	1	л	0	1	0	1	TOG
	1	л	1	1	TOG	GLE	

-HIGH LEVEL PULSE,	DATA
IS TRANSFERRED ON	
ING EDGE OF PULSE.	

LOGIC DATA-

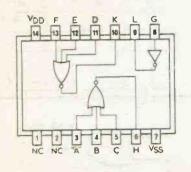
-THE LEVEL OF Q BEFORE INDICATED INPUT CON-DITIONS WHERE ESTAB-LISHED.

TOGGLE -EACH OUTPUT CHANGES TO ITS COMPLEMENT ON EACH ACTIVE TRANSIENT (PULSE OF CLOCK).

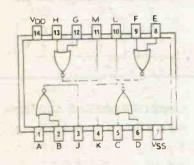
## LOGIC DATA

Every time we produce a circuit using CMOS chips we nag our readers to be careful how they treat them. Nonetheless we still receive countless telephone tales of wor to the common testimony of blown, melted, or otherwise deceased CMOS. So let us all kneel on our conductive-rubber mats facing magnetic north (wearing our earthed wrist-bands) and repeat the litany against static - Thou shalt not touch the pins, but ye shall leave the bloody thing in its black foam until the moment of the hot iron arrives. Got that? Good.

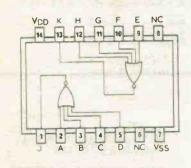
#### CD 4000A DUAL 3-INPUT NOR GATE PLUS INVERTER



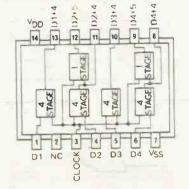
#### CD4001A QUAD 2-INPUT NOR GATE



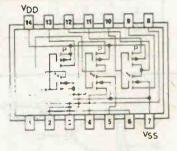
#### CD4002A DUAL 4-JNPUT NOR GATE



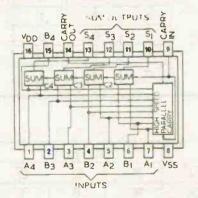
#### CD4006A 18-STAGE STATIC SHIFT REGISTER



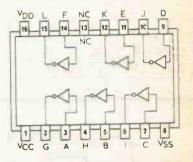
#### CD4007A DUAL COMPLEMENTARY PAIR WITH INVERTER



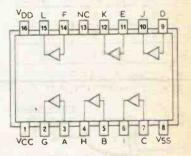
#### CD4008A 4-BIT ADDER WITH PARALLEL CARRY



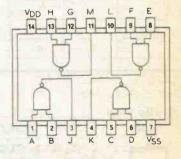
#### CD4009A, 4049A HEX BUFFER CONVERTER - INVERTING

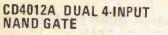


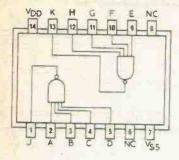
#### CD4010A, 4050A HEX BUFFER Converter --- Non-Inverting



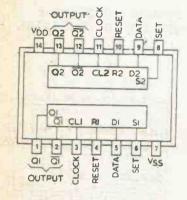
#### CD4011A QUAD 2-INPUT NAND GATE



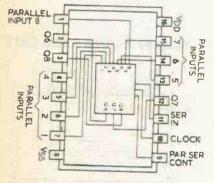




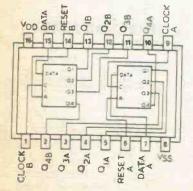
CD4013A DUAL D-TYPE FLIP-FLOP WITH RESET



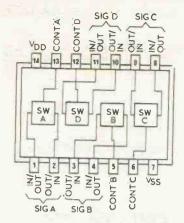
#### CD4014A 8-STAGE STATIC SHIFT REGISTER



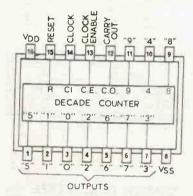
#### CD4015A DUAL 4-STAGE SHIFT REGISTER



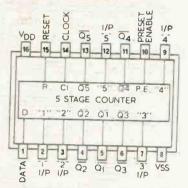
#### CD4016A, 4066A QUAD SWITCH



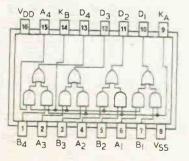




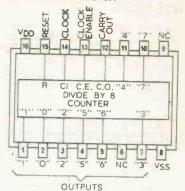
#### CD4018A PRESETTABLE DIVIDE-BY-N COUNTER



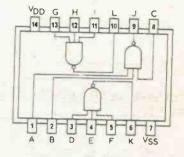
CD4019A QUAD AND OR SELECT GATE



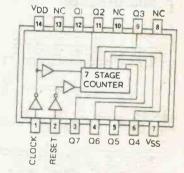
#### LOGIC DATA CD4022A DIVIDE BY 8 COUNTER-DIVIDER



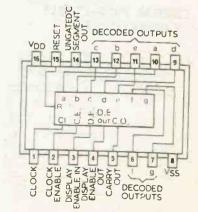
#### CD4023A TRIPLE 3-INPUT NAND GATE



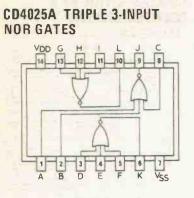
CD4024A 7-STAGE BINARY COUNTER



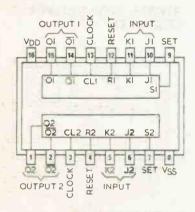
#### CD4026A DECADE COUNTER-DIVIDER



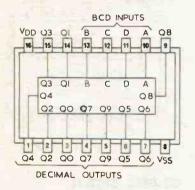
## LOGIC DATA-



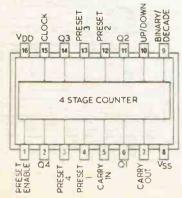
CD4027A DUAL J-K FLIP-FLOP



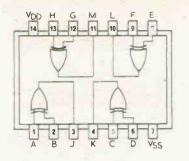
#### CD4028A BCD TO DECIMAL DECODER



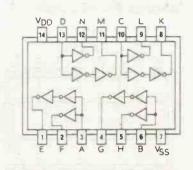
#### CD4029A PRESETTABLE UP-DOWN COUNTER



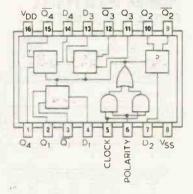
CD4030A QUAD EX-OR GATES



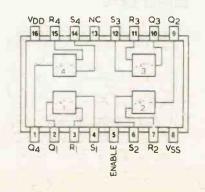
#### CD4041A QUAD TRUE COMPLEMENT BUFFER



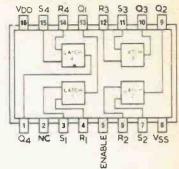
#### CD4042A QUAD D-TYPE LATCH (CLOCKED)



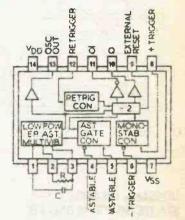
#### CD4043A QUAD 3-STATE NOR R/S LATCH



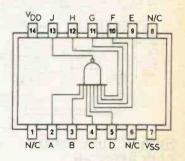
#### CD4044A QUAD 3-STATE NAND R/S LATCH



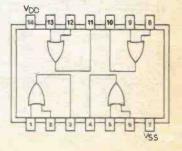
#### CD4047A MONOSTABLE ASTABLE MULTIVIBRATOR



#### CD4068B 8-INPUT NAND GATE



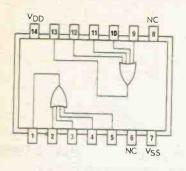
CD4071B QUAD 2-INPUT OR GATE



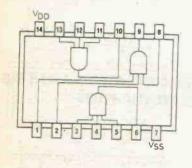
ETI CIRCUITS No. 2.

LOGIC DATA

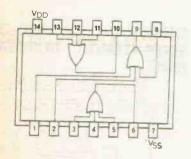
CD4072B DUAL 4-INPUT OR GATE



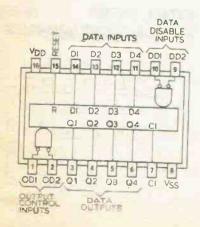
CD4073B TRIPLE 3-INPUT AND GATE



CD4075B TRIPLE 3-INPUT **OR GATE** 

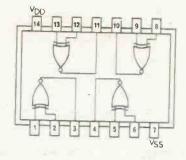


CD4076B QUAD D TYPE FLIP-FLOP

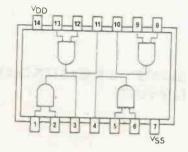


ETI-CIRCUITS No. 2

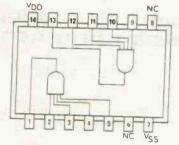
CD4077B QUAD EX NOR GATES



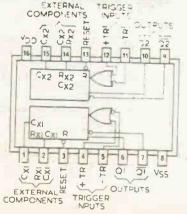
CD4081B QUAD 2-INPUT AND GATE

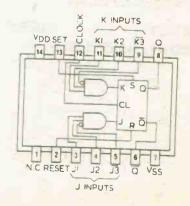


CD4082B DUAL 4-INPUT AND GATE

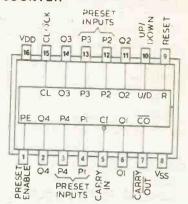


CD4528 DUAL RETRIGGERABLE MONOSTABLE CD4096B GATED J-K FLIP-FLOP EXTERNA:

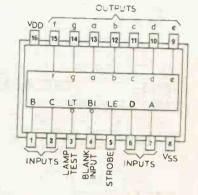




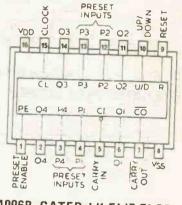
CD4510B BCD UP-DOWN COUNTER



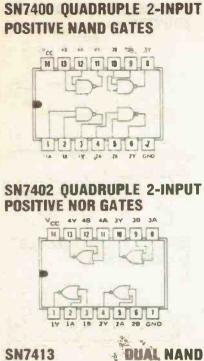
CD4511B BCD-TO-7-SEGMENT DECODER/DRIVER



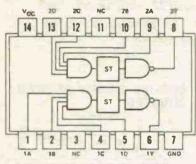
CD4516B BINARY UP-DOWN COUNTER



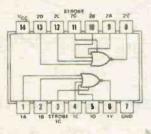
## LOGIC DATA



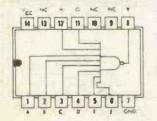
SCHMITT TRIGGERS



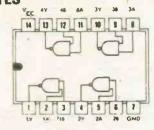
SN7425 DUAL 4-INPUT NOR GATES WITH STROBE



SN7430 8-INPUT POSITIVE NAND GATES



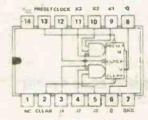
SN7401 QUADRUPLE 2-INPUT OPEN-COLLECTOR NAND GATES



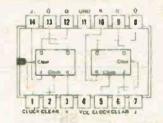
SN7404 HEX INVERTERS

## 

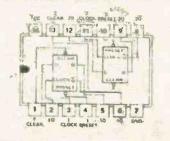
SN7472 J-K MASTER SLAVE FLIP-FLOPS



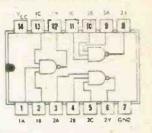
SN7473 DUAL J-K MASTER-SLAVE FLIP-FLOPS



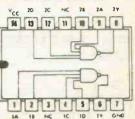
SN7474 DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS



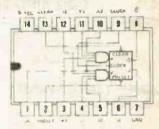
#### SN7410 TRIPLE 3-INPUT POSITIVE NAND GATES



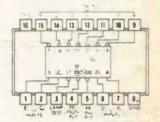
SN7420 DUAL 4-INPUT POSITIVE NAND GATES



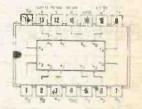
#### SN74104 GATED J-K MASTER-SLAVE FLIP-FLOPS



SN7447A BCD-TO-SEVEN-SEGMENT DECODER/ DRIVE

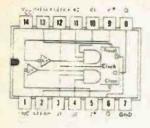


#### SN7481, SN7484 16-BIT ACTIVE-ELEMENT MEMORIES

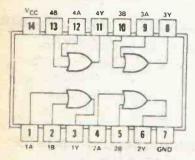


ETI CIRCUITS No. 2

#### SN7470 EDGE-TRIGGERED J-K FLIP-FLOPS

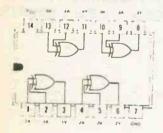


#### SN7432 QUADRUPLE 2-INPUT POSITIVE-OR GATES

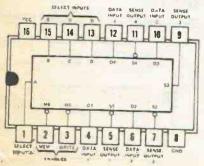


SN7475 4-BIT BISTABLE

#### SN7486 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

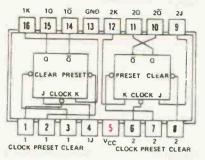


#### SN7489 64-BIT READ/WRITE MEMORY

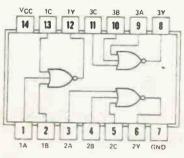


TI CIRCUITS No. 2

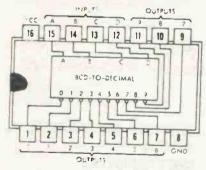
#### SN7476 DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH PRE-SET AND CLEAR



#### SN7427 TRIPLE 3-INPUT POSITIVE-NOR GATES

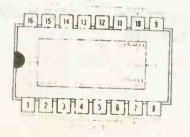


SN7445, SN74145 BCD-TO-DECIMAL DECODER/DRIVERS



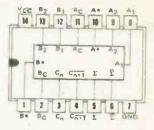
#### SN74160 THRU SN74163 SYNCHRONOUS 4-BIT COUNTERS

SN74160, SN74161 SYNCHRONOUS COUNTERS WITH DIRECT CLEAR SN74162, SN4162 FULLY SYNCHRONOUS COUNTERS

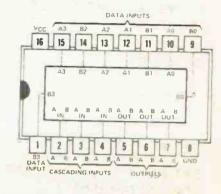


#### SN7480 GATED FULL ADDERS

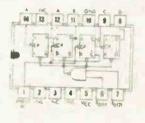
-LOGIC DATA



#### SN7485 4-BIT MAGNITUDE COMPARTORS

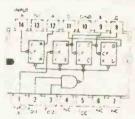


#### SN7492 DIVIDE-BY-TWO AND DIVIDE-BY-SIX COUNTERS

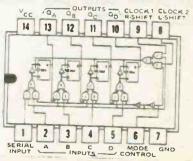


SN7492 4 COUNTERS

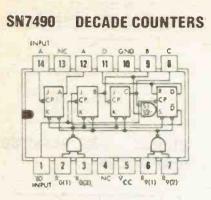
4-BIT BINARY



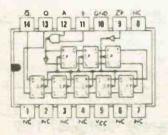
#### SN7495A 4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS



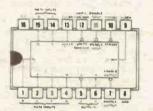
## LOGIC DATA



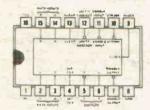
SN7491A 8-BIT SHIFT REGISTERS



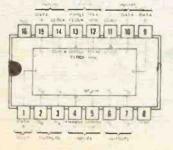
#### SYNCHRONOUS RATE MULTIPLIERS SN7497



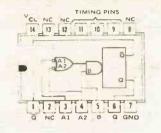
#### SN74167



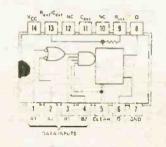
SN74190, SN74191 SYNCHRONOUS UP/DOWN COUNTERS WITH MODE CONTROL



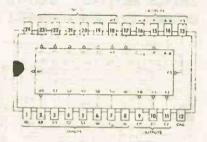
#### SN74121 MONOSTABLE MULTIVIBRATORS



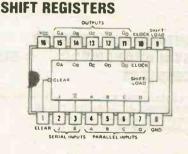
SN74122 RETRIGGERABLE MULTIVIBRATORS WITH CLEAR



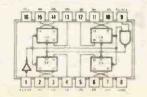
SK74181 ARITHMETIC LOGIC UNITS



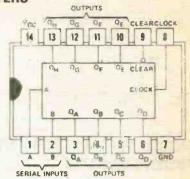
SN741954- BIT PARALLEL ACCESS



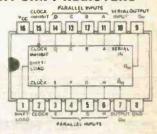
SN74175 QUAD D-TYPE FLIP-FLOP



#### SN74164 8-BIT PARALLEL-OUT SERIAL SHIFT REGIS-TERS

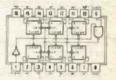


SN74165 PARALLEL-LOAD 8-BIT SHIFT REGISTERS

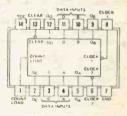


#### SN74174 FLIP-FLOP

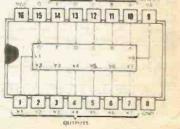
HEX D-TYPE



#### SN74176 & SN74177 PRESET DECADE & BINARY COUNTER



SN74184, SN74185A CONVERTERS



ETI CIRCUITS No 2

#### **MPU Glossary**

- ACCUMULATOR The register where arithmetic or logic results are held. Most MPU instructions manipulate or test the accumulator contents ACCESS TIME Time take for specific byte of storage
- to become available to processor. CIA Asynchronous Communication Inter-face Adapter. Inter-face between asynchronous peri-ACIA
- pheral and an MPU ALU Arithmetic and Logic Unit. The part of the MPU
- where arithmetic and logic functions are performed. ASCII American Standard Code for Information
- Interchange Binary code to represent alphanu-
- merchange Binary code to represent alphanu-meric special and control characters. ASSEMBLER Software which converts assembly language statements into machine code and checks for non valid statements or incomplete definitions
- ASSEMBLY LANG Means of representing programme statements in mnemonics and conveniently handling memory addressing by use of symbolic terms. ASYNCHRONOUS. Operations that initiate a new
- operation immediately upon completion of current
- one -- not timed by system clock. BASIC Beginner's All Purpose Symolic Instruction Code An easy to learn, widely used high level anguage
- BAUD Measure of speed of transmission line. Number of times a line changes state per second Equal to bits per second if each line state represents logic 0 or 1
- BAUDOT CODE 5 bit code used to encode alphanumeric data BCD Binary Coded Decimal Means of representing
- decimal numbers where each figure is replaced by a binary equivalent
- BENCHWARK A common task for the implementation of which programmes can be written for different MPUs in order to determine the efficiency of the different MPUs in the particular application
- BINARY The two base number system. The digits are 0 or 1 They are used inside a computer to represent the two states of an electric circuit.
- BIT A single binary digit BREAKPOINT Program address at which execution will be halted to allow debugging or data entry
- BUFFER Circuit to provide isolation between sensitive parts of a system and the rest of that system
- BUG A program error that causes the program to mallunction
- BUS The interconnections in a system that carry parallel binary data. Several bus users are connected to the bus, but generally only one "sender" and one "receiver" are active at any one nstant
- BYTE A group of bits the most common byte size is eight bits
- CLOCK The basic timing for a MPU chip COMPILER Software which converts high level language statements into either assembly language statements, or into machine code.
- CPU Central processor unit. The part of a system which performs calculation and data manipulation tunction
- CROM Control Read Only Memory
- CRT Cathode Ray Tube. Often taken to mean complete output device CUTS Computer Users Tape System Definition of
- system for storing data on cassette tape as series of tones to represent binary 1's and 0's. DEBUG The process of checking and correcting any
- program errors either in writing or in function DIRECT ADDRESSING An addressing mode where
- the address of the operand is contained in the nstruction

ETI CIRCUITS No. 2

- DMA Direct Memory Access. DUPLEX Transfer of data in two directions simultaneously ENVIRONMENT The conditions of all registers.
- flags, etc. at any instant in program EPROM Electrically Programmable Read Only
- Memory Memory that may be erased (usually by ultra violet light) and reprogrammed electrically. EXECUTE To perform a sequence of program steps

- EXECUTION TIME. The time taken to perform an instruction in terms of clock cycles. FIRMWARE Instructions or data permanently stored
- in ROM FLAG A flip flop that may be set or reset under software control
- FLIP-FLOP Two state device that changes state when clocked
- FLOPPY (DISK) Mass storage which makes use of flexible disks made of a material similar to
- magnetic tape FLOW CHART A diagram representing the logic of a
- computer program
- GLITCH Noise pulse HALF DUPLEX Data transfer in two directions but only one way at a time HAND SHAKE System of data transfer between CPU
- and peripheral whereby CPU asks peripheral if it will accept Gata and only transfers data if
- answer' is yes HARD COPY System output that is printed on paper HARDWARE All the electronic and mechanical
- components making up a system. HARD WIRE Circuits that are comprised of logic gates wired together, the wiring pattern determining the overall logic operation
- HASH Noisy sig signal The base 16 number system Character set is decimal 0 to 9 and letters A to F
- HIGH LEVEL LANGUAGE Computer language that is
- easy to use but which requires compiling in machine code before it can be used by an MPU HIGHWAY As BUS. IMMEDIATE ADDRESSING. Addressing mode which
- uses part of the instruction itself as the operand data INDEXED ADDRESSING A form of indirect
- addressing which uses an Index Register to hold the address of the operand
- INDIRECT ADDRESSING. Addressing mode where the address of the location where the address of the operand may be found is contained in the nstruction
- INITIALISE. Set up all registers flag, etc., to defined conditions
- INSTRUCTION. Bit pattern which must be supplied to an MPU to cause it to perform a particular function INSTRUCTION REGISTER MPU register which is
- used to hold instructions fetched from memory INSTRUCTION SET The repertoire of instruction The repertoire of instructions
- that a given MPU can perform. INTERFACE Circuit which connects different parts of
- system together and performs any processing of signals in order to make transfer possible ie. serial – parallel conversion) INTERPRETER An interpreter is a software routine
- which accepts and executes a high level language program, but unlike a compiler does not produce intermediate machine code listing but converts
- each instruction as received INTERRUPT A signal to the MPU which will cause it to change from its present task to another.
- K Abbreviation for 2<sup>10</sup> = 1028 KANSAS CITY (Format): Definition of a CUTS based cassette interface system. LANGUAGE. A systemmatic means of communicat-
- ing with an MPU. LATCH Retains previous input state until overwrit-
- ten Last In First Out Used to describe data stack
- LOOPING Program technique where one section of program the loop) is performed many times over.
- MACHINE LANG. The lowest level of program The only language an MPU can understand without Interpreter
- MASK Bit pattern used in conjunction with a logic operation to select a particular bit or bits from machine word MEMORY The part of a system which stores data
- working data or instruction object code) MEMORY MAP Chart showing the memory
- allocation of a system MEMORY MAPPED I/O A technique of implement
  - ing I O facilities by addressing I/O ports as if they
- were memory locations. MICRO CYCLE Single program step in an MPUs Micro program. The smallest level of machine program step.

MICRO PROCESSOR: A CPU implemented by use of

LOGIC DATA

- large scale integrated circuits. Frequently, implemented on a single chip MICRO PROGRAM Program inside MPU which controls the MPU chip during its basic
- fetch/execute sequence MNEMONIC A word or phrase which stands for another longer) phrase and is easier to remember MODEM Modulator / demodulator used to send and
- receive serial data over an audio link. NON VOLATIVE Memory which will retain data
- content after power supply is removed, e.g. ROM. BJECT CODE. To bit patterns that are presented to OBJECT the MPU as instructions and data O/C Open Collector Means of tieing together O/P's
- from different devices on the same bus OCTAL Base 8 number system Character set is
- decimal 0-8 P CODE Operation Code A bit pattern which
- specifies a machine operation in the CPU OPERAND Data used by machine operations
- PARALLEL. Transfer of two or more bits at the same
- time PARITY Check bit added to data, can be odd or even
- parity In odd parity sum of data 1's + parity bit is
- PERIPHERAL Equipment for inputing to or outputting from the system e.g., teletype, VDU. etc.)
- PIA Peripheral Interface Adapter-
- POP Operation of removing data word from LIFO stack PORT A terminal which the MPU uses to
- communicate with the outside world PROGRAMS: Set of MPU instructions which instruct
- the MPU to carry out a particular task PROGRAM COUNTER Register which holds the address of next instruction (or data word) of the
- program being executed PROM Programmable read only memory. Proms are
- special form of ROM, which can be individually programmed by user. PLICH
- Operation of putting data to LIFO stack Random Access Memory. Read write memory
- Data may be written to or read from any location in this type of memory. REGISTER: General purpose MPU storage location that will hold one MPU word.
- that will hold one MPU word. RELATIVE ADDRESSING Mode of addressing whereby address of operand is formed by combining current program count with a displacement value which is part of the instruction. ROM: Read Only Memory. Memory device which has its data content established as part of manufacture and cannot be changed.
- and cannot be changed. SCRATCH PAD. Memory that has short access time
- and is used by system for short term data storage RIAL Transfer of data one bit at a time SERIAL
- SIMPLEX Data transmission in one direction only
- SOFTWARE Programs stored on any media. SOURCE CODE The list of statements that make up a
- program STACK A last in first out store made up of registers or memory locations used for stack.
- STATUS REGISTER. Register that is used to store the condition of the accumulator after an instruction has been performed e.g. Acc = 0. SUB ROUTINE A sequence of instructions which
- SUB ROUTINE A sequence of instructions which perform an often required function, which can be called from any point in the main program SYNTAX. The grammar of a programming language TRAP. Vector). Pre-defined location in memory which
- the processor will read as a result of particular
- condition or operation TRI STATE Description of logic devices whose outputs may be disabled by placing them in a high
- impedance state TTY Teletype TWO'S COMPLEMENT ARITHMETIC System of TTY
- performing signed authmetic with binary numbers: UART Universal Asylichippnous Receiver Transmitter VDU. Video Display Unit. VECTOR Memory address provided to the processor

VOLATILE Memory duries provider to the processor volatile Memory devices that will lose data content if power supply removed i.e. RAMI WORD Parallel collection of binary digits much as

93

byte

## MISCELLANEOUS DATA\_

### BIPOLAR TRANSISTORS

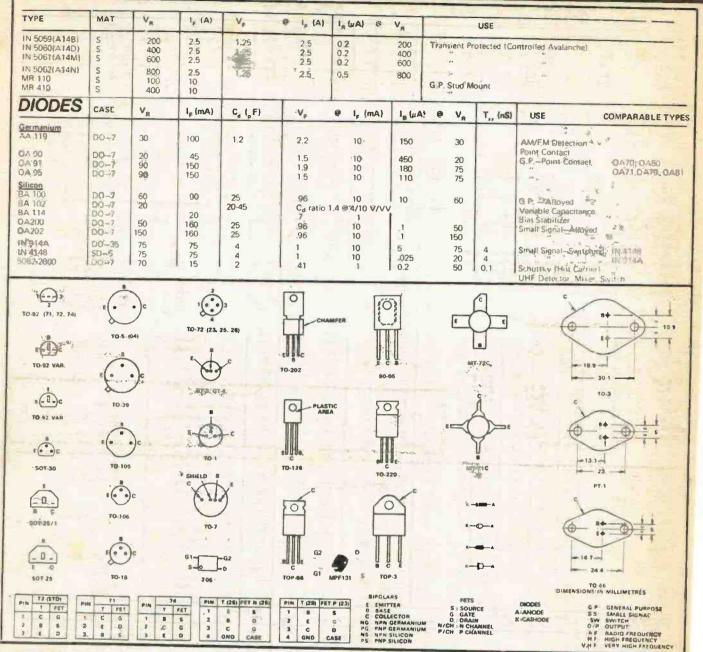
TYPE	CASE	POL		Vcb	IC mA	Vce	s @ IC mA	Hfe @	IC mA	Ft MHz	e IC mA	Ptot mW	Use	Comparable Types
C107	GT3 TO-1	NG	15	15	10			30-160	.3	2	.3	80	Low Noise Audio	AC125-2N406
C126	TO-1	PG	12 12	32 32	100			100	2	1.3	10 10	216	Audio Driver Audio Driver	2N406 2N406
C127	TO-1	NG	12	32	500			105	50	1.5	10	340	Audio O/P	AC187
C128	TO-1	PG	16	32	1000	.6	1A	60.175	300	1	10	260	Audio O/P	AC188
C132 C187	TO-1 TO-1	PG NG	12	32 25	200	.35	200 1A	115	50	1.3	10	216	Audio O/P	AC188
C188	TO-1	PG	15	25	2000	.6	14	100-500		1	10	800	Audio O/P Audio O/P	AC127 AC128
D149	TO-3	PG	30	50	3500	.7	3A	30-100	1A	.3	500	32W	G.P. O/P	0C26,AU106
D161	PT1	NG	20	32	3000	.6	1A	80.320	500	.02	300	4W	Audio Amp.	AD165,2N1218,2N129
D162	PT1 TO-7	PG	20	32	3000	.4	1A	80-320	500	= .015	300	6W	Audio Amp.	AD143,AD152,AD427
F115	TO-7	PG PG	15 15	32 32	10			150	1	75 75	1	75	H.F. Amp. H.F. Amp.	AF144, AF194, 2N3127
F116	TO-7	PG	15	32	10	Б		150	i	75	- i - i	75	H.F.Amp.	AF146, AF185, 2N2273 AF135, AF136, 2N3127
F117	TO-7	PG	15	32	10			150	1	75	1	75	H.F. Amp.	AF136, AF197, 2N5354
F118 5215	TO-7 TO-3	PG	20	70	30	5	30	35	10	175	10	375	V,H,F, Amp.	BFW20
SZ16	TO-3	PG PG	60 32	100 60	10A 10A	.4	10A 10A	20-55 45-130	1A 1A	.2	1A 1A	30W 30W	H.C. Sw, H.C. Sw,	OC28 OC29,AD138,AD723
Z17	TO-3	PG	- 32	60	10A	.4	10A	25-75	IA	.22	IA	30W	H.C. Sw.	0C35,AD424
SZ 18	TO-3	PG	32	100	10A	.4	10A	30-110	1A	.22	1A	30W	H.C. Sw.	OC36
107	TO-18	NS	45	50	100	.2	100	110-450		300	10	300	S.S. Amp.	BC207,8C147,BC182
108	TO-18 TO-18	NS NS	20 20	30 30	100	2	100 100	110-800	2	300 300	10 10	300 300	S.S. Amp. Low Noise S.S. Amp.	BC208,BC148,BC183
1090	TO-18	NS	20	30	100	2	100	420-800	2	300	10	300	Low Noise High Gain	BC209,BC149,BC184 BC209C,BC184C,BC14
157	SOT-25	PS	45	50	100	.25	100	75-260	2	150	10	300	S.S. Amp.	BC177,BC307,BC212
158	SOT-25	PS	25	30	100	.25	100	75-500	2	150	10	300	S.S. Amp.	BC178,BC308,BC213,
159 177	SOT-25 TO-18	PS PS	20 45	25 50	100	.25	100 100	125-500	2	150	10	300	S.S. Amp.	8C179,8C309,8C214
178	TO-18	PS PS	25	30	100	.25	100	75-260	2	150 150	10 10	300 300	S.S. Amp. S.S. Amp.	BC157,BC307,BC212 BC158,BC308,BC213
179	TO-18	PS	20	25	100	.25	100	125-500	2	150	10	300	S.S. Amp	BC159,8C309,8C214
182(L)	SOT-30	NS	50	10	200	.25	10	100-480	2	150	10	300	S.S. Amp.	8C107,8C207,8C147
183114	SOT-30	NS	30	45	200	.25	10	100-850	2	150	10	300	S.S. Amp.	BC 108, BC 208, BC 148
184(1)	(TO-92/74 SOT-30 (TO-92/74	NS	30	45	200	25.	10	250-850	2	150	10	300	Low Noise, High Gain	BC109,BC209,BC149
86 107	TO-18 TO-106	PS NS	25 45	40	200	.5	50 10	40-200	2	50	50	300	G.P. Amp.	8C213.8C177.8C158
208.	TO-106	NS	20		200			110-220	2	150	10	300	S.S. Amp,	BC107,8C182,BC147
209	TO-106	NS	20	25	200	25	10 10	110-800	2 2	150 150	10	300	S.S. Amp. Low Noise, High Gain	BC108,BC183,BC148 BC109,BC184,BC149
12(L)	SOT 30	PS	50	60	200	25	10	60-300	2	200	10	300	S.S. Amp.	8C307,8C157,8C177
213(L)	SOT-30	PS	30	45	200	.25	10	80-400	2	200	10	300	S.S. Amp.	BC308,8C158,8C178
214(L)	ITO-92/74 SOT 30 (TO-92/74	PS	30	45	200	25	10	80-400	2	200	• 10	300	S.S. Amp.	
327.	TO-92	PS	45	-	1000	0.7	500	100-600	100	100	10	800	O/P	2N3638
337	TO-92	NS	45	-	1000	07	500	100-600	100	200	10	800	O/P	2N3642
547 548	507-30 507-30	NS.	45 30	.50 30	100	8 .6	100	110-800	2	300 300	10	500	S.S. Amp.	8C107 8C207 8C147
549	SO7-30	NS	30	30	100	.6	100			300	10	500 500	S.S. Amp. Low Noise S. Sig.	8C108, BC208, BC148 BC109, BC209, BC149
549C	507-30 I	NS	30	30	100	6	100	1	2	300	10	500	Low Noise, High Gain	8C109C,8C149C
635	TO-92(74)	NS	45	45	1A	5	500	40 250	150	130	500	1W	Audio O/P	3C639
536 539	TO-92(74) TO-92(74)	PS NS	45 80	45 100	1A 1A	5	500 500	40-250 40-160	150 150-	130	500	1W	Audio O/P	8C640
540	TO 92174)	PS	80	100	1A	5	500	40-160	150	130 130		1W 1W	Audio O/P Audio O/P	MU9610,TT801 MU9660,TT800
Y70	TO-18	PS	40	50	200	.5	50	50	10	250	50	350	G. P.	BC212
V71	TO 18	PS	45	45	200	5	50		10	200	50	350	G.P.	BC212
V72 137	TO-18 TO-12G	PS NS	25 60	25 60	200 1A	5	50	50	10	200	50	350	G.P.	BC213
138	TO-126	PS	60	60		5 5	500 500	40-160	150 150	250 75	500	8W WB	G.P. O/P G.P. O/P	BD139 BD140
139	TU-126	NS	60	100	IA	.5	500	40-160	150	250	500	BW	G.P. 0/P	40409
40	10-126	PS	80	100	IA	5	500	40.160	150	75	500	87	G.P. O/P	40410
62 63	TO-126 TO-126	PS VS	60 60	60 80	4A 4A	2.5	1.5A 1.5A	750	1.5A	7	1.GA	36W	High Gain Darl, O/P	80266
56A	TO-220	PS	80	80	8A	20	3A	750 750	1.5A 3A	7	1.5A	36W 60W	High Gain Darl, O/P High Gain Darl, O/P	BD267
67A	TO:220	NS	80	100	84	2	3A	750	3A	7		60W	High Gain Darl, O/P	
(64A	TO3	75	80	03	12A	2.5	5A	1000	SA	7	5A	117W	Darl, O/P	
105A 20	TO-3 TO-3	NS INS	60 60	80	12A 15A	2.5	5A 4A	1000 20-70	SA 4A	7	5A 4A	117W 115	Darl O/P	2012065
15	TO-72[281	NS	30	50	30			45-165	4A	230	44	145	Power O/P V.H.F. Amp.	2N3055
57	TO-72(28)		30	40	25		15.11	26	4	350	4	130	T.V. I.F. Amp.	
73	TO-72(28)	NS	25,	40	25			37	7	550	5	230	T.V. I.F. Amp.	
77	TO-39 TO-39	NS	60	100	50			20 20	15 30	120 120	10	795 1.7W	T.V. Video Amp.	BF336
79	TO-39	NS	115	250	50		- 1	20	20	120	10	1.7W	T.V. Video Amp. T.V. Video Amp.	8F336 BF338
80	TO-721251	NS	20	30	20			13	2	675	2	150	U.H.F. Amp.	BF200
84	10.72(28)	NS	20	30	30			75-750	1	300	1	145	H.F. Amp.	
85 94	TO-72(28) SOT-25.11	NS NS	20 20	30 30	30			34-140 65-220	1	220 260		145 250	H,F. Amp	8F 195
	SOT 25/1.	NS	20	30	30			35-125	1 1	200		750	H,F, Amp. H,F, Amp	BF185
82	TO 72051	NS	20	JU	20		-	15	3	650	3	150	V.H.F. Amp.	BF180
95	TO-39	NS	180	185	100			20-60	30	136		3W	Video Amp.	
100 136		NS	200	300	100			20.60	30	130		3W	Video Amp.	
00 36 37	TO-39	CV1		80	100	2	150	20-60 30	30 150	130 60	50	3W 2.86W	Video Amp G, P	
00 36 37 38	TO-39	NS	35	00						- 10				
100 136 137 138 150	TO-39 TO-39		- 1	60	14		150		150	50	_	2 86W	GP	
100 136 137 138 150 151 152	TO-39 TO-39 <b>TO</b> -39 TO-39	NS NS NS	30 20	60 40	1A 1A	35 .35	150 150	40 60	150 150	50 50	50 50	2.86W 2.86W	G. P. G. P.	
900 136 137 138 150 151	TO-39 TO-39 TO-39	NS NS	30	60	1A 1A 10A	35		40			50			

ETI CIRCUITS No. 2

## \_\_\_\_MISCELLANEOUS DATA\_

		POL	-		10		a.e	114		-				liete		ANEUUS VAIA
TYPE MJE 2955	CASE 90-05	MA	T Vce	Vcb	IC mA	-	@ IC mA	Hte	mA	Ft			Use	1500		Comparable Types
MUE3055 MU9610	90-05 152	PS NS NS	60 - 60 30	70 70 40	10A 10A 2A	1.1	4A 4A	20-70 20-70	4A 4A	2	50 50	0 90W		Power (		T.IP2955 TIP3055
MU9611	152.01	NS	30	40	2A	0.4	1.5A	1		70	25		0/P			TT801 TT801
MU9660 MU9661	152 152-01	PS	30 30	40 40	2A 2A	0.4	1:5A			70	25 25	0 1W	0/P 0/P			TT800 TT800
NSD106 NSD206	TO-20213		100	140		.2-9	100	50-150		80	50		Driv	er - 0/P er - 0/P		11600
OC26 OC28	10-3 10-3	PG	30 60	50 100	3.54 10A	.7	3A 10A	30-100		.3	50	0 32W	G.P.	O/P		AD149
0C44N	TO-1 GT-3	PG	5	15 15	10		100	45-225	5 1	75	1A	85	R.F			ASZ15 AF125,AF135,AF172
0070	GT-3 GT-3	PG	10 10	30 30	50 50			30	5	3	3	85	G.P.	Amp Amp		AF132, AF185, AF196 AC121, AC126, 2N1190
0672	GT 6	PG	16	32	250			30-75 45-120	3 10	.6 35		125		Amp 10 O/P		AC126,2N2429 AC122,AC125,AC162
0C74N 0C75	GT 3	PG PG	10 . 10	20 30	300 50	.6	300	60-150 60-130		1		550 125		io O/P Amp		AC125, AC180, AC192
TIP318 TIP328	TOP-66 TOP-66	NS PS	80 80	80 80	3A 3A	1.2	3A 3A	20 20	500 500	3	500 500	40W	Powe	er Amp - er Amp -		AC173,AC192
TIP2955 TIP3055	TOP3	P5 NS	70 70	100	15A 15A	1.1	4A 4A	20 20	4A 4A	.8	000	90W	Powe	er Amp -	- Sw.	MJE2955
TT797 37798	TO-39 TO-39	PS NS	60 60	60 80	1A 1A		70	40 120	100	8		90W 800	Audi	er Amp o Driver	- Sw.	MJE3055 TT800,NSD206
TT800	TO-39 10-39	PS NS	60 60	60 80	1A 1A			40-120 40-120	100	60 100		800 800	Audi	o Driver o Driver	- Sw	TT801,NSD106 TT797,NSD206
2N301 2N706A	TO-3	PG	32	40	3A			40-120 50	1A	60 2	1A	800 11W		o Driver o O/P	- Sw	TT798,NSD106 AT1138,0C26
21/2926	TO 18 TO 92(74)		15 25	25 25	200			20 150	10 2	200 100		300 200		Speed S	w	BC108 ejc
2N3053 2N3054	TO-39 TO-65	NS NS	40 55	60 90	700 4A	1.4	150 200	50-250 25	150 500	100 8	50 200	2 861	GP.	Switch		B0137 TIP31B
2N3055 2N3563	TQ-100	NS NS	60 12	90 30	15A 50	1.1	4A	20 20-200	4A 8	8 600	1A 8	1 15W	0/P -	- Sw		80720
2N3564 2N3565	TO-106	NS NS	15 25	30 30	100 50	.3 .35	20	20·500 150-600	15	400	15	200	R,F	- I.F. A	mp	8F173 8F167
2N3566 7N3567	10-105 10-105	NS NS	30 40	40 80	200 500	1	100	150-600		40	30	200 300	G.P.	Level An Amp. &	Sw.	8/108,8C208 18/2/83
2N 565 2N3589	10 105	NS NS	60 40	80 80	500 500	.25	150 150	40.120	1	60 60	50 50	300 300	G.P.	Amp. & S Amp. & S	Sw.	BC337
2N3638 2N3638A	TO-105	PS PS	25 25	25 25	500 500	.25	50 50	100-300	50	60 100	50 50	300 300	G.P. /	Amp. & S Amp. & S	św.	BC327
2N3640, 2N3641	10,105	PS	12	12	80	.2	10	100 30-120	50 10	150 300	50 10	300 200		Amp. & S ated Swit		BC558
2N3642 2N3643	TO-105	NS	30 ,45	60 60	500 500	.22 .22	150 150	40-120 40-120	150	250 250	50 50	350 350	G.P. A	Amp. & S	w.	BC337 BC337
2N3644	TO:105	NS PS	30 45	60 45	500 500	.22 1	150 300	100-300		250 200	50 20	350 300	G'P, A	Amp. & S Amp. & S	w.	BC337 BC327
2113945 2113702	TO 105 TO 92(74)	PS PS	60 25	60 40	500 200	1	300 50	115-300 60-300	500 50	200	20 50	300 360	GPA	mp. & S	w.	
21-3904 21-4250	TO 92 TO-106	NS PS	40 40	60 40	200 100	.25	10	100-300 250-400	!mA	50	50	310 200	Low L	evel Am	ρ.	BC213 BC167A,BF194
214258	TO-106 TO-92	PS NS	12 15	12 30	50 50	.5	50 10	30·120 20	10 3	700	10	200	Satúra	ted Sw	p.	BC559
2N4403 2N5580	TD-92 MT 71C	PS NS	40	40	600 600	.0		100-300 5		600 175→	4	200 310	G.P.	ted Sw.		BC307A 2N2904
2N5590 2N5591	MT-72C MT AC	NS	18 18	36 36	2A 4A		. 1	5	250 / 500	175→ 175→	3W 10W 25W	15W 30W	H.F M	obile R.	F	
2N587/1 40250	TO-3	PS NS	60 50	60 50	IA AA	1	4A	20-100	2.5A	4	250	70W 100W	Power	obile R. Transisti	or	2N5872,2N4908,MJ2955
40408	105- 10-39(H)	NS	80 80	50	700	1.4	1.5A 150 150	25 40-200	100 200	1 100		29W 1W	Power	Transisto Transisto	or	2N9054 8C639
40410	TO 39/HI	25	80		700	14		50-250 50-250	150 150	100		3M 3M	Power	Transisto Transisto	10	BD139 -BD140
FETS	CASE	BV GSS	GIUAI		Max @			IDSS (mA) Min	Max @	Vos	VGS	Y is lumi Min	Max @	e Vos	Ptot	Use/Comments
EIPF 103	TQ-021721 TO-02 21	25 25	10	4	8	15 15	1	2	20	15 15	0	2000	7500 5000	15 15	310 310	N/CH Jun titten - VHF
MPF 104 MRE 106		75 75	14		78	15	1G	24	9 16	15 15	0	1500 2000	5500° 6000	15 15 15	310	N/GH Junction Audio Sweet R N/CH Junction Audio Sweet Res N/CH Junction Audio Sw.
2N5457	10:92 721	25 25	1	5	6	15 15		4	10 5	15 15	0	2500	7000	15	-310	N/CH Junction - RE
2N5458		出办	1		7	1 <b>5</b> 15	10	2	6	15 15	0	1000 1500 2000	5000 5500	15	310	N/CH Junction - Audio Swy
245485		3	1		3	15 15	10	1	5 10	15 15	0	2000 3000	6000 6000	15	310 310	N/CH Junction - Audio Sw. N/CH Junction - VHF
BENTO		70 30						8	20	15	0	3500	7000 6500	15	310 <sup>-</sup> 300	N/CH Junction VHF N/CH Junction Audio to H.F.
BEWUR	10 72(35)	75 7 20			4	15		2	10 20	15 15	0		6500 6500		300 300	N/CH Junction Audio To H.F. N/CH Junction Audio To H.F.
NAR!	10/100	20				10.			30 30	15 10	0	10000	20000 6000	15 10	500 180	N/CH Dual Gite MOS, VHF Amp P/CH Junction - Audro, Sw.
DIODE		-	1	-	-	_	1		1		1					AUDIO, SW.
ТУРЕ	MAT	V,	8	I <sub>F</sub> (A	0	VF	e	1 <sub>6</sub> (A)	Ι <sub>R</sub> (μΑ	)@	V <sub>R</sub>		USE			
A 14 P A 15 A	WW.		00	2.5 5		1.25		2.5 5	0.5		1000	Transien G.P. Rec	t Protecte	diContr	olled A	valarichel
EM 4005	S		75 50	196		1.2 1.1		25 1	11		75		bile H. Du	Ry		
EAL 401 EM 404	5		0jj) IDO	. 1: 1		1.). 1.1		1	5		100	G.P. Nec	and a			
EM1410	evice.	10	00 50	1		11 1.1 1.1		1	5		400					
104 4002 189 4004	19.10	1			- 11-			1	5		50 100					
1N 4007	S	10	00	1		11 ~		1	5		400 1000	**				
		494			-			3	15		1000	P.1				

## MISCELLANEOUS DATA.



## **PROBLEMS**?

SUFFIXES 'k', 'm', 'M' etc after component values indicate a numerical multiplier or divider — thus

#### Multipliers

- k = X 1000
- M = X 1000 000
- G = X 1000 000 000

#### Dividers

- $u = \div 1000\ 000$
- n = ÷ 1000 000 000
- R = ÷ 1000 000 000 000

Where the numerical value includes a decimal point the traditional way of showing it was, for example, 4.7k. Experience showed that printing errors occurred due to accidental marks being

mistaken for decimal points. The Standard now calls for the ex-suffix to be used in place of the decimal point. Thus a 4.7 k resistor is now shown as 4k7. A 2.2 uF capacitor is now shown as 2u2 etc.

Some confusion still exists with capacitor markings. Capacitors used to be marked with multiples or submultiples of microfarads – thus 0.001 uF, 470 uF etc. Markings are now generally in sub-multiples of a Farad. Thus

- 1 microfarad (1u) = 1x10-6/F
- 1 nanofarad  $(1n) = 1 \times 10^{-9} F$
- 1 picofarad  $(1p) = 1 \times 10.12F$

OV on our circuits in this series means the same as - ve (an abbreviation for 'negative'

Unless otherwise specified all components in our drawings are shown as seen from above note however that component manufacturers often show them as seen looking into the pins.

Pin numbering of ICs — with the IC held so that the pins are facing away from you and with the small cut-out downwards pins are numbered anticlockwise starting with pin number 1 at bottom right.

The thin line on a battery schematic drawing is positive (+ve or just +).

- way round or in the wrong places.
- (b) Faulty soldering.
- (c) Bridges of solder between tracks (particularly with Veroboard) – breaks in Veroboard omitted – and/or whiskers of material bridging across Veroboard breaks.
- (d) Faulty components.

#### RESISTOR AND CAPACITOR LETTER AND DIGIT CODE (BS 1852)

#### MISCELLANEOUS DATA RESISTOR AND CAPACITOR COLOUR CODING

#### Resistor values are indicated as follows:

Q 47 O marked	R47	100 Ω marked	100R
1.0	1R0	1 kQ	1K0
4.7 Ω	4R7	10 kQ	10K
47 0	47R	10 M Q	10M
A letter following	the value	shows the tolerance.	
$r = \pm 1\%; G$	= ±2%:	J = ±5%; K = ±1	0%;
$M = \pm 20\%$			
833M =	= 0.330	+20%	

#### $6K8F = 6.8 k\Omega \pm 1\%$ .

Capacitor values are indicated as:

0.68 pF marked p68 6.8 pf 608 
 6.8 nf marked
 6n8

 1000 nF
 1u0

 6.8 uF
 6u8
 6p8 1n0 1000 pF 6u8

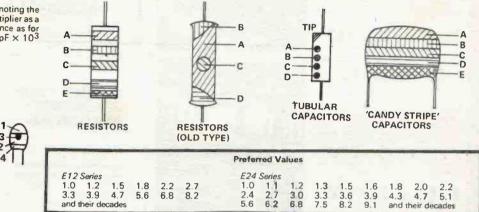
Tolerance is indicated by letters as for resistors. Values up to 999 pF are marked in pF, from 1000 pf to 999 000 pF (= 999 nF) as nF (1000 pF = 1 nF) and from 1000 nF (= 1 uF) upwards as uF. Some capacitors are marked with a code denoting the value in pF (first two figures) followed by a multiplier as a power of ten (3 = 10<sup>-9</sup>). Letters denote tolerance as for resistors but C =  $\pm 0.25$  pf. E.g. 123 J = 12 pF x 10<sup>3</sup>  $\pm 5\%$  = 12 000 pF (or 12nF).

#### **Tantalum Capacitors**

	1	2	3	4	
Black	-	0	×1	10 V	
Brown	=1	1	×10		
Red	2	2	×100		1~
Orange	3.4	.3	-		2.6
Yellow	4	4	-	6.3 V	2
Green	5	5	_	16 V	4
Blue	6	6		20 V	4
Violet	7	7	-		
Grey	8	8	×0.01	25 V	
White	9	9	×0.1	3 V	
			(Pink 35		

Colour	Band A	Band B	Band C (Multi Resistors	plier) (Capacitors	B and D (T	olerance) Capacit		Band e Resistors	I. Baluarta
				oupound's	Resistors	Up to 10 pF	Over 10 pF	Inesisions	Polyester Capacitors
Black		0	1	1	_	2 p0	±20%		
Brown	1	1	10	10	±1%	0 p1	±1%	-	
Red	2	2	100	100	±2%	1	±2%	_	250.v.w
Orange	3-	3	1 000	1 000+	-	_	±2.5%		200.1 11.
Yellow	4	4	10 000	10 000	-	-	_		-
Green	5	5	100 000	-		0 p5	±5%		-
Blue	6	6	1 000 000	-	-	1211	_	-	12
Violet	7	7	10 000 000	-	-	- 1	-	- 1	-
Grey	8	8	108	10 n	-	p25	- 1	_	-
White	9	9	10 <sup>9</sup>	100 n		1p0	±10%		_
Silver	- 1	-	0.01	-	±10%	-	-	_	_
Gold	- 1	- 1	0.1	-	±5%	(H) 1	E 1	_	_
Pink	- 1	- 1	-	-		-	- 1	Hi-Stab.	-

Note that adjacent bands may be of the same colour unseparated.



**Reference Notes** 

#### TI CIRCUITS No. 2



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