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# CIRCUIT techniques

## volume two

Second Printing

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An ELECTRONICS TODAY INTERNATIONAL publication

# ETI Circuit Techniques

## volume two

**Second Printing**

**Editor:** Roger Harrison
**Layout:** Bill Crump

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# Power supplies and voltage regulators

An in-depth look at practical power supply and voltage regulator circuits.

**Ray Marston**

TWO OF THE MOST common tasks facing the electronics designer or experimenter are those of designing basic power supply circuits to enable pieces of equipment to operate from ac power, and designing voltage regulator circuits to enable specific circuits to operate from well defined dc supply voltages over wide ranges of load current.

Both of these design tasks are reasonably simple. Basic power supply circuits consist of little more than a transformer-rectifier-filter combination, so all the designer has to do is select the circuit values, using a few very simple rules, to suit his own particular design requirements.

Voltage regulator circuits may vary from simple zener diode networks, designed to provide load currents up to only a few milliamps, to fixed voltage high current units for powering logic boards, etc, or to variable voltage high current units designed to act as general purpose pieces of test gear. We'll look at practical versions of all these examples in the next few pages.

## Power supply circuits

Basic power supply circuits are used to enable pieces of equipment to operate safely from ac mains power (rather than from batteries), and are simply designed to convert the ac mains voltage into an electrically isolated dc voltage of the value required by the actual circuitry of the equipment.

The basic power supply circuitry consists of little more than a transformer-rectifier-filter combination; the transformer is used to convert the ac line voltage into an electrically isolated and more useful ac value, and the rectifier-filter combination is used to convert the new ac voltage into the appropriate dc value.

Figures 1 to 4 show the four most useful transformer-rectifier-filter combinations you will ever need. The Figure 1 circuit provides a single-ended dc supply from a single-ended transformer and bridge rectifier combination, and gives a virtually identical performance to the centre-tapped transformer circuit of Figure 2. The circuits in Figures 3 and 4 both provide 'split' or 'dual' dc supplies and, again, give virtually identical performance. The rules for designing these circuits are very simple, as you'll see in a moment.

## Transformer-rectifier selection

The three most important parameters of a transformer are its *secondary voltage*, its *power rating*, and its *regulation factor*. The secondary voltage is always quoted in RMS terms at full rated power load, and the power load is quoted in terms of VA or watts (though VA is more widely used). Thus, a 15 V, 20 VA transformer will provide a secondary voltage of 15 V RMS when its output is loaded by 20 watts. When the load is removed (reduced to zero) the secondary voltage will rise by an amount specified by the *Regulation Factor*. Thus, the output of a 15 volt transformer with a 10% regulation factor (a typical value) will rise to 16.5 volts when the output is unloaded.

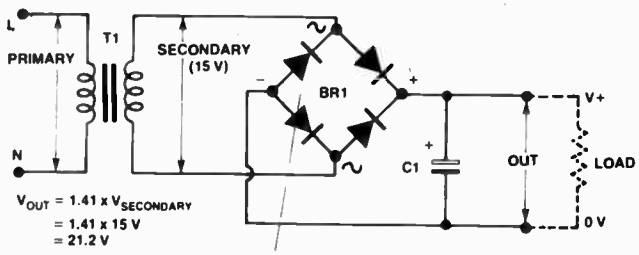



*Figure 1.* **Basic single-ended supply using a bridge rectifier module.**

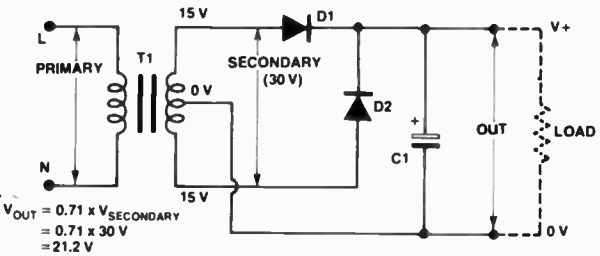



*Figure 2.* **Basic single-ended supply using a centre-tapped transformer.**

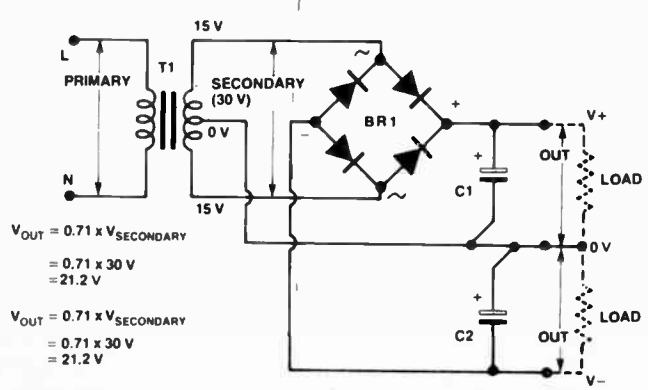



*Figure 3.* **Basic dual supply using a bridge rectifier module.**

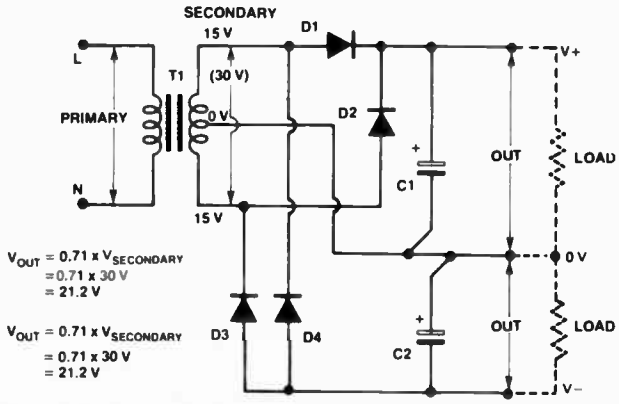



*Figure 4.* **Basic dual supply using individual diodes.**

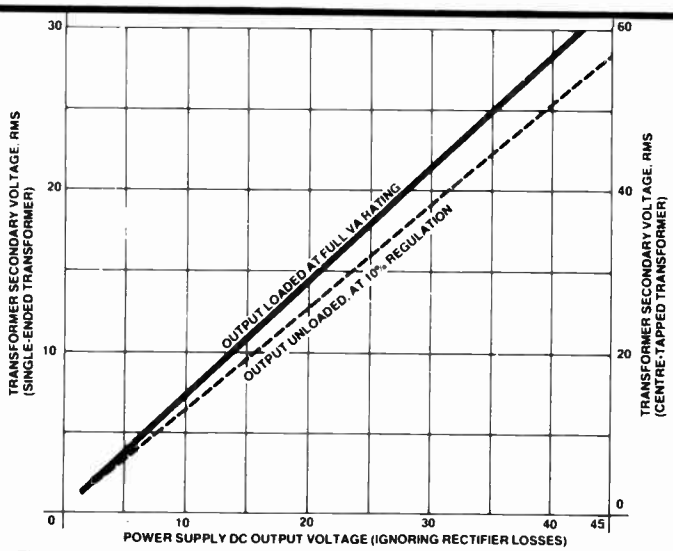



*Figure 5.* **Transformer selection chart (see text).**

Now, the most important point to notice here is that the RMS output voltage of the transformer secondary is *not* the same as the dc output voltage of the complete power supply. In fact, the dc output voltage of a fullwave rectified circuit is 1.41 (i.e:$\sqrt{2}$) times the RMS transformer voltage (ignoring rectifier losses) that is feeding the rectifier, as shown in the graph of Figure 5. Note here that this voltage is equal to 1.41 times the voltage of a single-ended transformer. Thus our single-ended 15 V RMS transformer with 10% regulation will in fact provide an output of about 21 volts at full rated load (just under 1 amp at a 20 VA rating) and 23.1 volts at zero load.

When rectifier losses are taken into account, the output voltages will be slightly lower than shown in the graph. In the 'two-rectifier' circuits of Figures 2 and 4, the losses amount to about 600 mV, while in the 'bridge' circuits of Figures 1 and 3 the losses amount to about 1.2 volts. The rectifiers should, for maximum safety, have continuous current ratings at least equal to the dc output currents, but preferably greater.

Thus the procedure for selecting a transformer for a particular problem is very simple. First, decide on the dc output voltage and current that are required; the product of these two values (allowing for slight rectifier losses) determines the minimum VA rating of the transformer. Next, consult the graph of Figure 5 to find the transformer secondary RMS voltage that corresponds to the required dc voltage. Simple?

## The filter capacitor

The purpose of the filter capacitor is to convert the fullwave rectified output of the rectifier — which consists of half-sinewave pulses — into a smooth dc output voltage. The two most important parameters of the capacitor are its *working voltage* and its *capacitance value*. The capacitance value determines the amount of ripple that will appear on the dc output voltage when current is being drawn from the circuit.

As a rule of thumb, in a fullwave rectified power supply operating from a 50 Hz power line, an output load current of 100 mA will cause a ripple waveform of about 700 mV peak-to-peak to be developed from a 1000u filter capacitor, the amount of ripple being directly proportional to the load current and inversely proportional to the capacitance value, as shown in the 'design guide' of Figure 6. In most practical applications, the ripple should be kept below 1-1.5 volts peak-to-peak under full load conditions. If very low ripple is required, the basic power supply can be used to drive a three-terminal voltage regulator, which can easily reduce the ripple by a factor of 60 dB or so at very low cost.

## Voltage regulator circuits

Voltage regulators may vary from simple zener-based circuits designed to provide load currents up to only a few milliamps, to fixed voltage high current circuits designed around 'fixed' three-terminal regulator ICs, or to variable voltage high current circuits designed around 'variable' three-terminal regulator ICs. We'll look at practical versions of all three types of circuit in the next couple of pages.

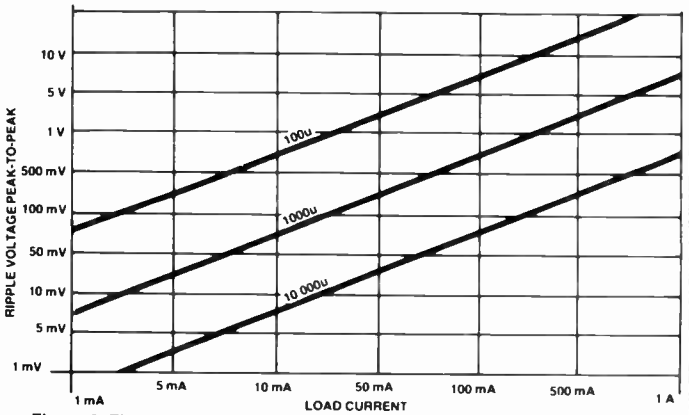



*Figure 6.* **Filter capacitor selection chart (see text).**

## Zener-based circuits

A zener diode can be used to produce a fixed reference voltage simply by using the connections shown in Figure 7. Here, a current of roughly 5 mA is passed through the zener diode from the supply line via limiting resistor R. Often, the supply voltage ($V_{in}$) may be subject to fairly wide variations, causing the zener current to vary over a similarly large range. So long as $V_{in}$ is always more than a few volts greater than the zener voltage and provided that the zener power rating is not exceeded, this variation has only a moderate influence on the output voltage of the zener, which typically has an effective output impedance of only a few tens of ohms.

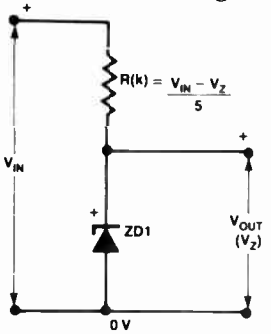



*Figure 7.* **Basic zener reference circuit. Bias is about 5 mA.**

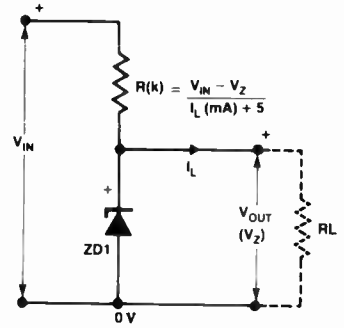



*Figure 8.* **Zener reg. can supply load currents up to a few tens of mA.**

A zener can be used as a very simple voltage regulator, providing maximum load currents up to a few tens of milliamps, by merely selecting the value of 'R' as shown in Figure 8. Here, when the designed maximum load current is being drawn only 5 mA flows through the zener; when zero load current is being drawn the zener passes 5 mA plus the maximum designed load current, and thus dissipates maximum power. It is important to ensure that the power rating of the zener is not exceeded under this 'no load' condition.

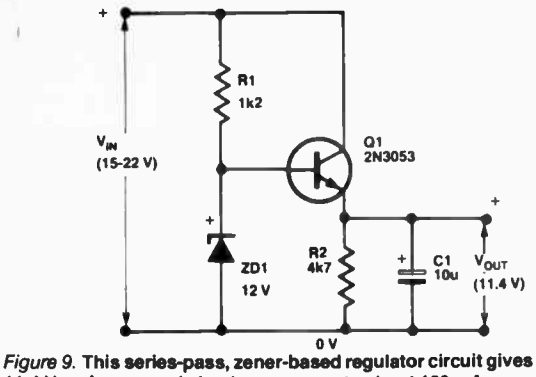



*Figure 9.* **This series-pass, zener-based regulator circuit gives an output of 11.4 V and can supply load currents up to about 100 mA.**

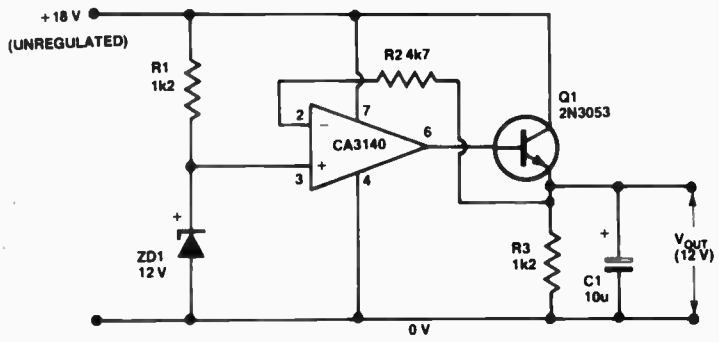



*Figure 10.* **Op-amp based reg. provides 12 V at up to 100 mA with excellent regulation.**

In most practical voltage regulator applications the zener is simply used to apply a 'reference' voltage to a high gain non-inverting buffer amplifier, which then supplies the required output power. The simplest example of this type of circuit is shown in the series-pass regulator circuit of Figure 9. Here, Q1 is wired as a voltage follower, its emitter remaining at about 600 mV below its zener-defined base voltage under all load conditions. The zener network provides the base drive current to Q1, this current being equal to the output load current divided by the current gain of the Q1 'buffer' stage. Clearly, the higher the gain of Q1, the better will be the output regulation of the circuit.

One way of improving the regulation of the Figure 9 circuit would be to use a Darlington or super-alpha pair of transistors in place of Q1. An even better solution is to use the op-amp plus transistor buffer stage shown in Figure 10. Here, the op-amp and Q1 are wired as a unity gain non-inverting dc amplifier with a near-infinite input impedance and near-zero output impedance. The output voltage tracks within a few mV of the zener reference value. The safe output current is limited to about 100 mA by the power rating of Q1; higher currents can be obtained if Q1 is replaced with a power Darlington transistor.

The Figure 10 circuit is very versatile. It can be made to generate any desired fixed voltage up to about 30 V maximum by simply using a suitable zener value and ensuring that the unregulated supply voltage is at least five volts greater than the zener value (up to 36 volts maximum). The circuit can be used as a variable voltage supply by simply wiring a potentiometer across the zener, with its slider taken to the non-inverting input of the 3140 op-amp; this op-amp can accept inputs all the way down to zero volts, enabling (for example) a 0-25 V supply to be easily implemented.

## Fixed three-terminal regulator circuits

Fixed voltage regulator design has been greatly simplified in the last decade by the introduction of three-terminal regulator ICs such as the '78xx' series of positive regulators and the '79xx' series of negative regulators. These ICs incorporate features such as built-in foldback current limiting and thermal protection. A wide range of three-terminal fixed voltage regulator ICs is available; standard current ratings are 100 mA, 500 mA, 1 A, and 3 A, and standard output voltage ranges are 5 V, 6 V, 8 V, 12 V, 15 V, 18 V and 24 V.

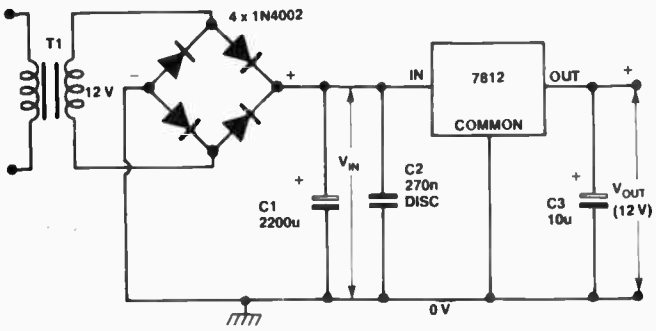



*Figure 11.* **Circuit employing a common three-terminal positive regulator.**

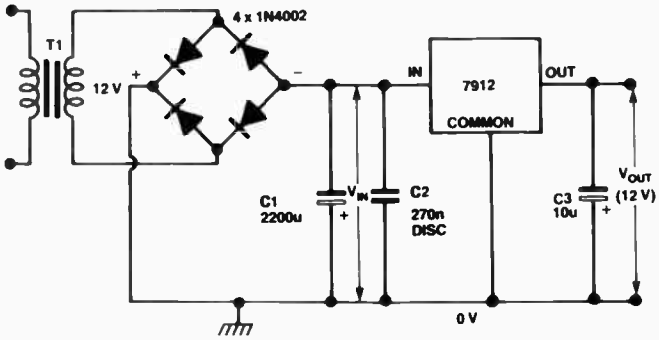
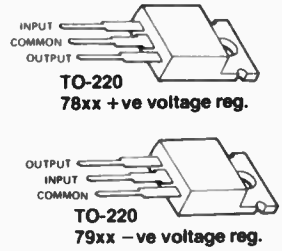



*Figure 12.* **Circuit using a common three-terminal negative regulator.**



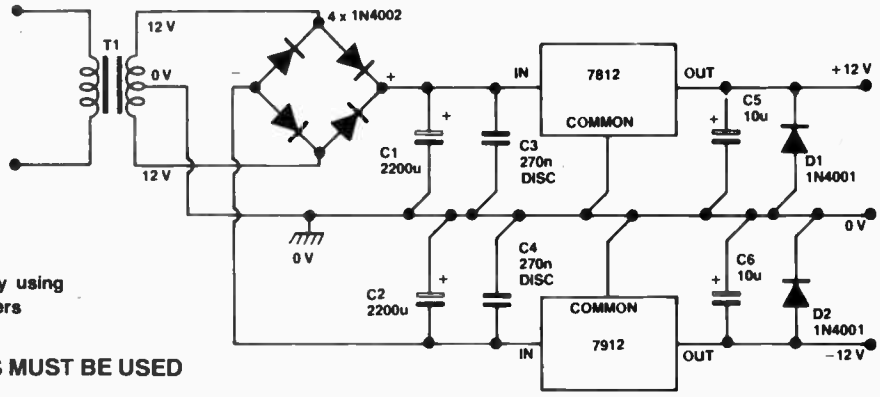




*Figure 13.* **Complete circuit of a dual supply using three-terminal regulators. This supply delivers +/– 12 V at up to 1 A.**

**WARNING: ADEQUATE HEATSINKS MUST BE USED**

Three-terminal regulators are remarkably easy to use, as shown in the basic circuits of Figures 11 to 13, which show the connections for making positive, negative and dual regulator circuits respectively. The ICs shown in these examples are 12 volt units with current ratings of 1 A, but the basic circuits are valid for all other voltage ratings, provided that the unregulated input voltage is at least three volts greater than the desired output voltage.

If the connection between the regulator's input and the rectifier's filter capacitor is more than 50 mm in length, then a capacitor is needed across the regulator's input terminals to maintain stability. Generally, all that is necessary is a 200n or greater value disc or plate ceramic capacitor, mounted right at the regulator's terminals using short leads. Alternatively a 2u2 or larger value tantalum could be used. You often see a capacitor connected across the regulator's output, too. Although not always necessary, a capacitor in this position reduces high frequency noise and improves transient response. A 100n or greater ceramic capacitor is recommended, or an electrolytic of 1u to 10u or so.

The output voltage of a three-terminal regulator is referenced to the 'common' terminal of the IC, which is normally (but not necessarily) grounded; most regulator ICs draw quiescent currents of only a few mA, which flow to ground via this 'common' terminal. The regulator output voltage can thus easily be raised above the designed value by simply biasing the 'common' terminal with a suitable voltage, making it easy to obtain 'odd-ball' output voltages from the regulator. Figures 14 to 16 show three ways of achieving this.

In figure 14 the bias voltage is obtained by passing the IC's quiescent current (typically about 8 mA) through RV1. This design is adequate in most applications, although the output voltage obviously shifts slightly with changes in quiescent current. The effects of such changes can be minimised by using the circuit of Figure 15, in which the RV1 bias voltage is determined by the sum of the quiescent current and the bias current set by R1 (12 mA in this example). If a fixed output voltage is required other than the designed value, it can be obtained by wiring a zener diode in series with the common terminal, as shown in Figure 16, the output voltage then being equal to the sum of the zener and regulator voltages.

The output current capability of a three-terminal regulator can be increased by using the circuit of Figure 17. Resistor R1 is wired in series with the regulator IC. At low currents, insufficient voltage is developed across R1 to turn Q1 on, so all the load current is provided by the IC. At currents of 600 mA or greater sufficient voltage (600 mV) is developed across R1 to turn Q1 on, so Q1 provides all currents in excess of 600 mA.

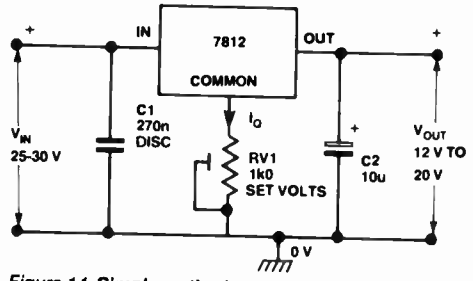



*Figure 14.* **Simple method to vary output voltage.**

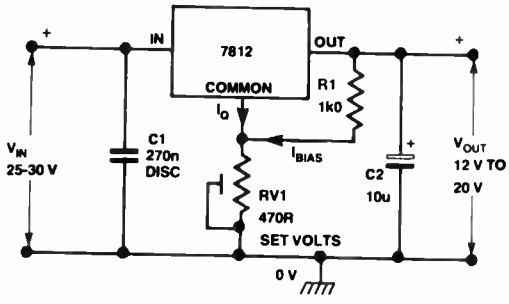



*Figure 15.* **Improved method of varying output voltage.**

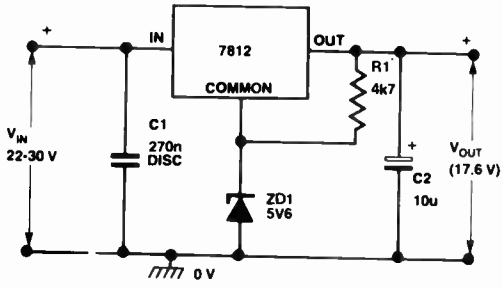



*Figure 16.* **'Jacking up' the output voltage using a zener.**

Finally, Figure 18 shows how the bypass transistor of the above circuit can be provided with overload current limiting via an 0R12 current-sensing resistor (R2) and turn-off transistor, Q2.

## Variable three-terminal regulator circuits

We've already seen that the outputs of '78xx' regulators can be varied over limited ranges by simply applying suitable variable voltages to their common or reference terminals, even though these ICs are designed as fixed regulators. If, however, you need to vary the output voltages over fairly wide ranges, a far better solution is to use one of the special variable three-terminal regulator ICs, such as the 317K or the 338K.

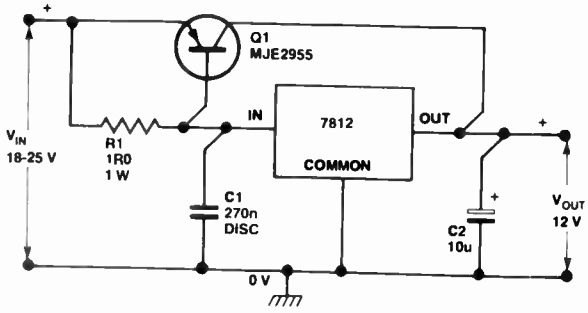



*Figure 17.* **Increasing the output current capacity of a three-terminal regulator. This will deliver 5 A at 12 V.**

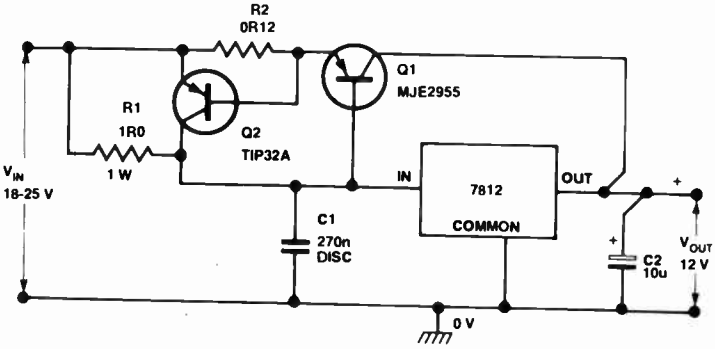
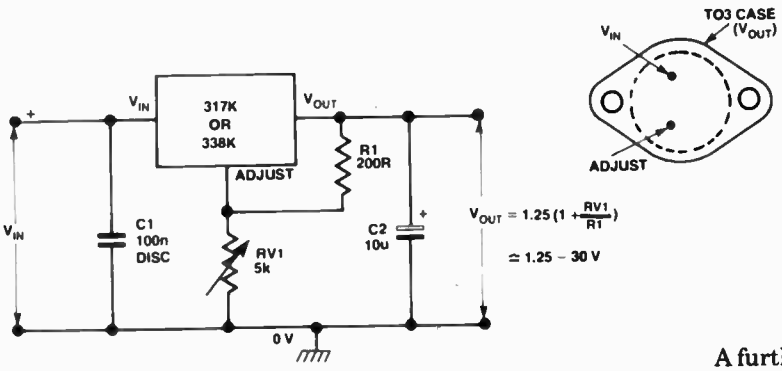



*Figure 18.* **Providing overload protection for the Figure 17 circuit. Q2 'robs' Q1 of base current when load current goes above 5 A.**




| PARAMETER | 317K | 338K |
|---|---|---|
| INPUT VOLTAGE RANGE | 4-40 V | 4-40 V |
| OUTPUT VOLTAGE RANGE | 1.25-37 V | 1.25-32 V |
| OUTPUT CURRENT RANGE | 1.5 A | 5 A |
| LINE REGULATION | 0.02% | 0.02% |
| LOAD REGULATION | 0.1% | 0.1% |
| RIPPLE REJECTION | 65 dB | 60 dB |

*Figure 19.* **Case outline, basic data and basic application circuit of the 317K and 338K variable-voltage three-terminal regulators.**

Figure 19 shows the outline, basic data and the basic variable-regulator circuit that is applicable to these two devices. Both devices have built-in foldback current limiting and thermal protection and are housed in TO3 packages, the major difference between the devices being that the 317K has a 1.5 amp current rating compared to the 5 A rating of the 338K. The major feature of both devices is that their 'output' terminals are always 1.25 volts above their 'adjust' terminals, and their quiescent or adjust-terminal currents are a mere 50 uA or so.

Thus in the Figure 19 circuit, the 1.25 volt difference between the 'adjust' and 'output' terminals causes several mA to flow to ground via RV1, thereby causing a variable 'adjust' voltage to be developed across RV1 and applied to the 'adjust' terminal. In practice, the output of the Figure 19 circuit can be varied over the approximate range 1.25 to 30 volts via RV1, provided that the unregulated input voltage is at least 3 V greater than the maximum output voltage. Naturally, alternative voltage ranges can be obtained by giving R1 and/or RV1 alternative values, but it should be noted that for best stability the R1 current must be at least 3.5 mA.

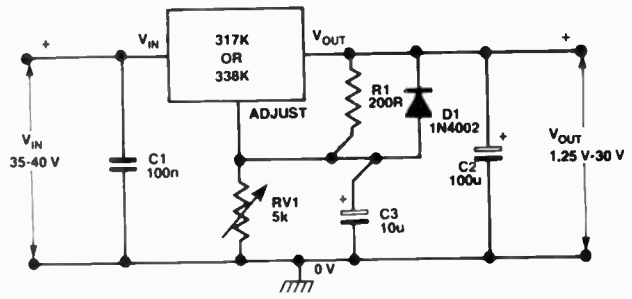



*Figure 20.* **This version of the variable-voltage regulator provides some 80 dB of ripple rejection.**

The basic Figure 19 circuit can be usefully modified in a number of ways. The basic ripple rejection factor of the Figure 19 circuit, for example, is about 65 dB, but this can be increased to 80 dB by wiring a 10u bypass capacitor across RV1, as shown in Figure 20, together with a protection diode connected as indicated, to prevent the capacitor discharging into the IC if the regulator output is short-circuited.

A further modification of the Figure 20 circuit is shown in Figure 21. Here, the transient output impedance of the regulator is reduced by increasing the C2 value to 100u; diode D2 is used to protect the IC against damage from the stored energy of this capacitor if an input short occurs.

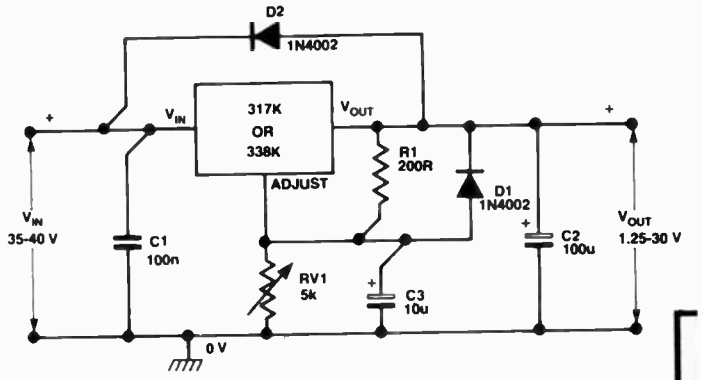



*Figure 21.* **This version has 80 dB ripple rejection, a low impedance transient response and full input and output short circuit protection.**

The minimum output voltage of the Figure 19 to 21 circuits is 1.25 volts. If you want the voltage to vary all the way down to zero, the circuits must be configured so that the adjust terminal goes to −1.25 V when RV1 is reduced to zero ohms. Figure 22 shows how this can be achieved, using a 35 V negative rail and a pair of series-connected diodes to clamp the low end of RV1 to −1.25 V.

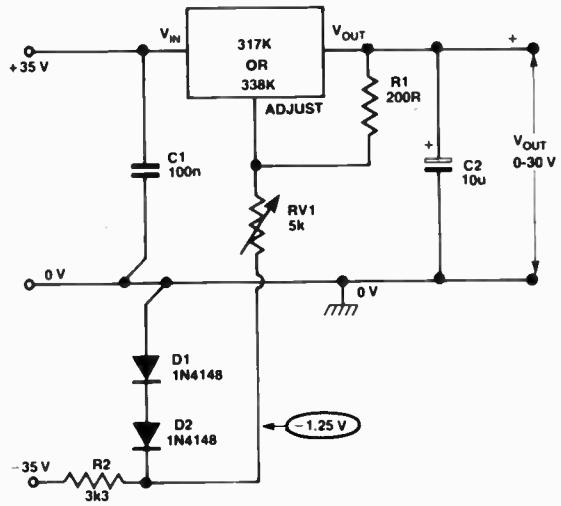



*Figure 22.* **How to provide variable output that goes from 0 V to 30 V.**

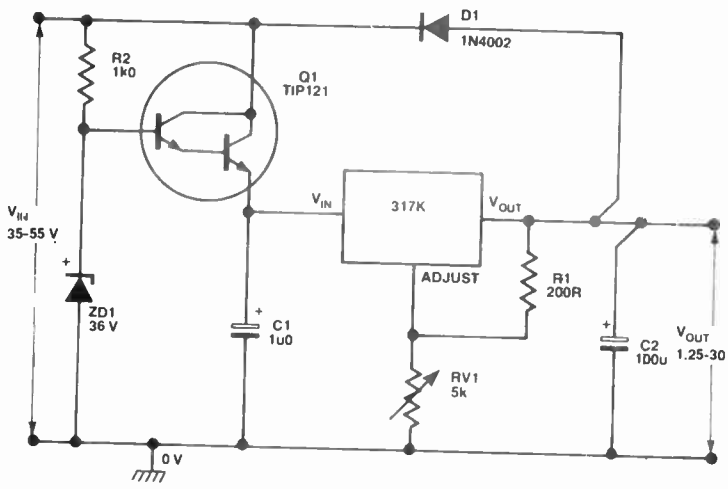



*Figure 23.* **This variable voltage unit uses a pre-regulator (Q1) to give input over-voltage protection and improved ripple rejection.**

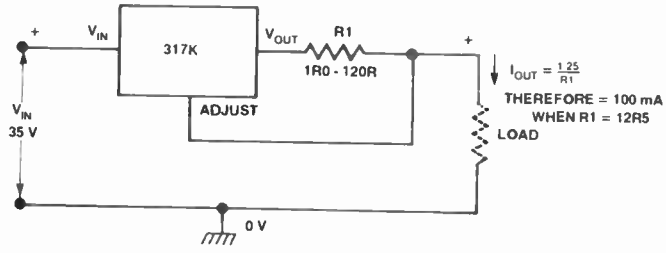



*Figure 24.* **A method of using the 317K as a precision current limiter or constant current generator.**

If you want to get the maximum possible voltage out of one of these regulators, you'll need to make sure that the input voltage does not exceed the 40 V rating of the IC. The best way to do this is to use a simple Darlington-plus-zener pre-regulator circuit, as shown in Figure 23, which enables you to use any unregulated input in the range 35 to 55 volts. Note that as well as giving input over-voltage protection, this pre-regulator also gives a further improvement in ripple rejection. If you want to use this circuit with a 5 A 338K regulator, you may need to reduce the value of R1 and beef up the power rating of the zener diode.

Finally, to complete this look at regulator circuits, Figure 24 shows how you can use the 317K as a precision current limiter or constant current generator in which the output current is determined by R1 and is virtually independent of the external load values. By suitable choice of R1, the constant-current magnitude can be set at any value between approximately 10 mA (R1 = 120R) and 1.25 A (R1 = 1R). Not bad for a two-component circuit! ●

# The Wien Bridge oscillator

**Probably the most popular type of low frequency sine wave oscillator as it is superior in virtually all respects to phase-shift types. Unfortunately it does not seem to be all that well understood. This article sheds some light on this most useful circuit.**

MOST STUDENTS of electronics – that includes hobbyists, you learn from your hobby don't you? – would be familiar with the "Wheatstone Bridge"; that often-handy technique for measuring unknown values of resistance. The Wien Bridge is an outgrowth of the Wheatstone Bridge. The basic circuit is shown in Figure 1.

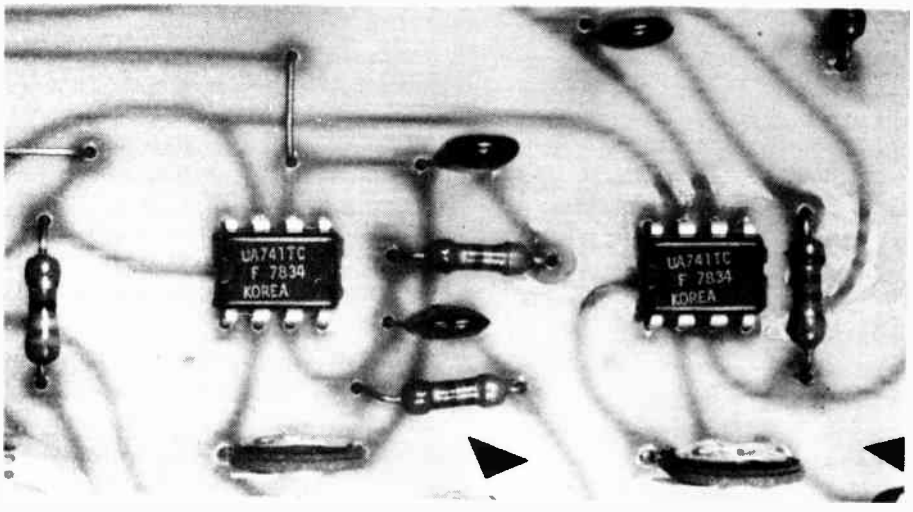
This circuit has some unique properties. The networks R1-C1 and R2-C2 form a potential divider between points A and B. Both networks have an impedance which decreases with frequency. At one frequency, and one frequency *only* (depending on the values of R1-C1 and R2-C2), the bridge will be balanced. That is, if a sinewave voltage is applied between A and B, no voltage will appear across C and D. Another interesting, and useful property of this bridge is that, at the balance frequency, the phase of the voltage across C and B will be *exactly* the same as that across A and B. The same will be true for harmonics of the balance frequency, *but*, the impedances of R1-C1 and R2-C2 will not be the same as at the balance frequency and the bridge will be unbalanced.

Well, how are these properties of the Wien Bridge used in an oscillator? The basic circuit of a Wien Bridge oscillator is shown in Figure 2. The component numbering of the Rs and Cs is the same as in Figure 1. We are assuming that the amplifier has good common-mode rejection, an infinite input impedance and zero output impedance. Fortunately, an op-amp is a reasonable approximation to this and the circuit as shown will work well with a common-or-garden 741 at frequencies up to 10 kHz.

The Wein Bridge components are connected such that positive and negative feedback is applied around the op-amp. This should be readily apparent from the way Figure 2 is drawn. The negative feedback is derived from the resistive potential divider R3 and R4. Positive feedback is provided by the potential divider R1-C1 and R2-C2. The amount of positive feedback through R1-C1 will *increase* with frequency as this network has a *decreasing* impedance as frequency increases. The parallel RC network formed by R2-C2 also has *decreasing* impedance with *increasing* frequency, tending to shunt the amount of applied positive feedback (via R1-C1) to ground. At the balance frequency, the applied positive feedback will be a maximum, falling at frequencies above and below the balance frequency. However, if the bridge is balanced, the positive feedback and the negative feedback will be equal ... and the circuit will not oscillate. *But*, if the amount of negative feedback provided by R3-R4 is chosen to be fractionally less than the positive feedback at the balance frequency, the circuit will oscillate. Since negative feedback predominates *at all other frequencies*, and the bridge remains unbalanced, harmonics of the balance (or resonant) frequency are suppressed and the waveform produced will be a sine wave of great purity.

In practice it is necessary to include some means of sensing the amount of negative feedback so that the amplifier gain can be held at the precise amount necessary to ensure oscillation. If the amount of negative feedback is too little, the waveform will be distorted. If too much, oscillation will not occur. Secondly, if the gain varies (for whatever reason) the feedback needs to be stabilised to prevent distortion and level variations.

**Twin Wien Bridge oscillator (from an ETI project) using lamps for stabilisation.**



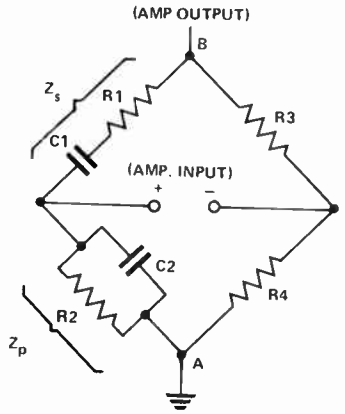
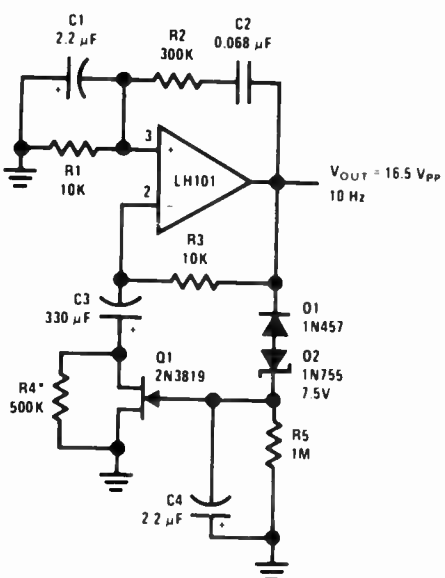



**Figure 1. Basic circuit of the Wien Bridge.**

The simplest way of doing this is to incorporate a thermistor or tungsten filament lamp in the negative feedback potential divider. If the latter is used for this purpose – and common light bulbs used for bezel lamps have tungsten filaments – it would replace R4 so that gain increases of the amplifier stage cause increased current in the lamp. This, in turn, would cause the temperature of the filament to rise, increasing its resistance, thus increasing the amount of negative feedback. The use of these temperature variable devices sets a limit on the lowest frequency at which the circuit can be used. When the period of oscillation is comparable to the thermal time constant of the particular light bulb or thermistor, the change in resistance over each cycle will bring about gain variations which result in distortion of the output waveform. Also, these devices have a "settling time" that prohibits the frequency from being changed quickly in a variable oscillator using this circuit.

**Figure 4. Example of a practical Wien Bridge oscillator with a FET in the feedback (courtesy National Semiconductor).**



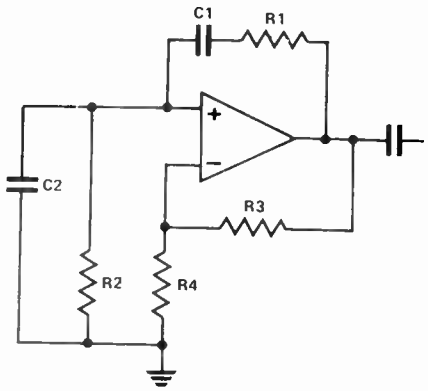




**Figure 2. Basic Wien Bridge oscillator circuit.**

The solution to these problems entails using a FET as part of the feedback element. The FET becomes part of R4 – as shown in Figure 3 – driven by an RC network between the op-amp output and the gate. In this way, the 'averaging time' of the circuit can be tailored to suit the job required. An example of a practical circuit is given in Figure 4.

A lot of the advantages, and the unique properties of the circuit, become apparent from a look at the mathematics involved; it's quite straightforward really.

The impedance of C1, at a certain frequency 'f', is given by:

$$Z_{C1} = \frac{1}{j\omega C1}$$

Where: $Z_{C1}$ = impedance of C1

$\omega = 2\pi f$,

$j = \sqrt{-1}$

So the total impedance, $Z_s$, of the series network R1-C1 is given by:

$$Z_s = R1 + \frac{1}{j\omega C1}$$

Since the impedance of capacitor C2 is also given by:

$$Z_{C2} = \frac{1}{j\omega C2}$$

Where: $Z_{C2}$ = impedance of C2

$\omega = 2\pi f$

$j = \sqrt{-1}$

and C2 is in parallel with R2, the total impedance of the parallel network R2-C2 ($Z_p$) is given by:

$$\frac{1}{Z_p} = \frac{1}{R_2} + \frac{1}{\frac{1}{j\omega C2}}$$

therefore: $$\frac{1}{Z_p} = \frac{1}{R_2} + j\omega C2$$

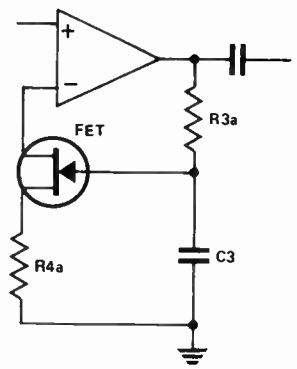



**Figure 3. Feedback stabilisation using a FET.**

Oscillation will occur when:

$$\frac{R3}{R4} = \frac{Z_s}{Z_p}$$

since it is this condition which will result in unity gain.

If we let R3 = 2 x R4, and substitute this in the equations for $Z_s$ and $Z_p$, this equation becomes:

$$\frac{2R4}{\frac{1}{R2} + j\omega C2} = R4\left(R1 + \frac{1}{j\omega C1}\right)$$

leading, approximately, to:

$$\omega^2 = \frac{1}{R1\ R2\ C1\ C2}$$

then $$2\pi f = \frac{1}{\sqrt{R1\ R2\ C1\ C2}}$$

and $$f = \frac{1}{2\pi\sqrt{R1\ R2\ C1\ C2}}$$

The major advantage of the Wien Bridge oscillator is its inherent stability and predictable frequency output. In other low frequency oscillators employing RC networks in the feedback, the frequency of oscillation is *directly* proportional to the values of the components in the network. In the Wien Bridge, you can see from the last equation that the frequency of oscillation is proportional to the *square root* of the component values in the network. The ease with which amplitude levelling and level stability can be achieved by using simple thermal devices in the negative feedback is another advantage. Thirdly, the low distortion possible with this circuit contributes greatly to its popularity.

On the other hand, to vary the frequency, two components have to be varied simultaneously – either C1/C2 or R1/R2. The fact that one of these is wholly 'above ground' complicates things – but it's not an insoluble problem as there are many Wien Bridge oscillators around! ●

# Lab Notes

# Gate, square, sine, modulate — with the 555 & 7555.

**Ray Marston**

The ubiquitous 555 timer chip, or its modern CMOS counterpart the 7555, can be readily used as a highly stable and cost-effective astable multivibrator. Although often used just as square wave generators, they're capable of performing some fairly fancy tricks.

THE OLD-FASHIONED 555 IC should be a fairly familiar component to the average hobbyist. It's the 'universal' square wave generator, pulser, gate and timer. But really, it's much more than that if you employ a little ingenuity in circuit design. The modern CMOS version, the 7555, is even more versatile than its predecessor. Apart from a wide variety of gating functions, the 555/7555 can perform tricks like ramp and sine waveform generation.

## Astable gate

The 555/7555 astable can be gated on and off in a variety of ways, to produce different output waveforms. Figure 1 shows the basic connections and the equivalent circuit of the standard 555/7555 astable. It is necessary to understand the operation of this basic circuit in order to appreciate the action of the various gating methods. In the following discussions, a 12 V supply rail is assumed in all circuits.

The first point to note about the Figure 1 equivalent circuit is that the IC contains a three-resistor potential divider, two voltage comparators, a flip-flop, a transistor and an output buffer.

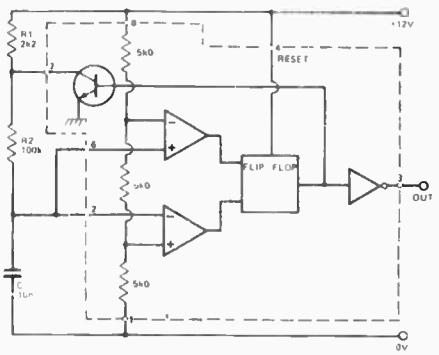



*Figure 1b.* **Equivalent circuit of the 555-type astable multivibrator.**

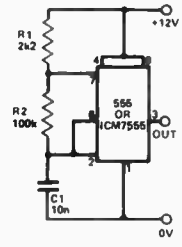



*Figure 1a.* **Basic circuit of the 555-type astable multivibrator.**

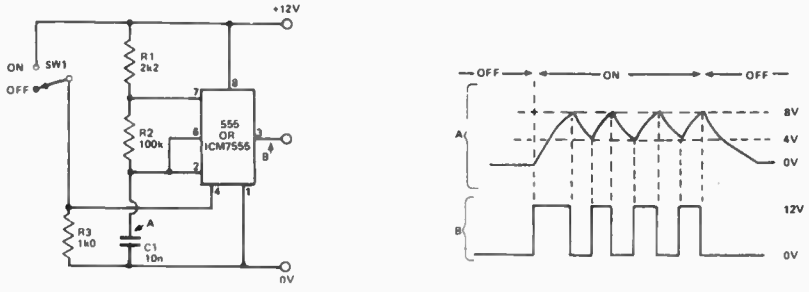



*Figure 2.* **Conventional way of gating the 555 astable, with resultant waveforms.**

The divider ratios are such that one-third of the supply voltage (i.e: 4 V) is set on the lower comparator and two-thirds of the supply voltage (i.e: 8 V) is set on the upper comparator. The circuit action is such that, in each operating cycle, C1 first charges up to 8 V through R1-R2, at which point the upper comparator activates the flip-flop and turns the internal transistor on; the transistor then discharges C1 through R2 until the C1 voltage falls to 4 V, at which point the lower comparator activates the flip-flop and turns the internal transistor off, causing C1 to recharge through R1-R2. The operating cycle is then complete and repeats ad infinitum. A ramp waveform with an amplitude that swings between 4 V and 8 V is generated across C1 and a rectangular waveform is generated at the output, pin 3.

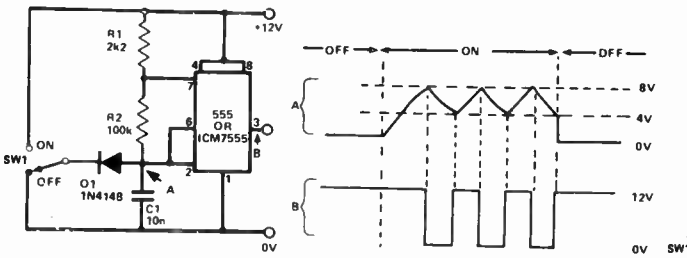



*Figure 3.* **Basic method of gating the 555 astable using C1, with resultant waveforms. Note that the period of the first half-cycle is longer than that of the succeeding half-cycles.**

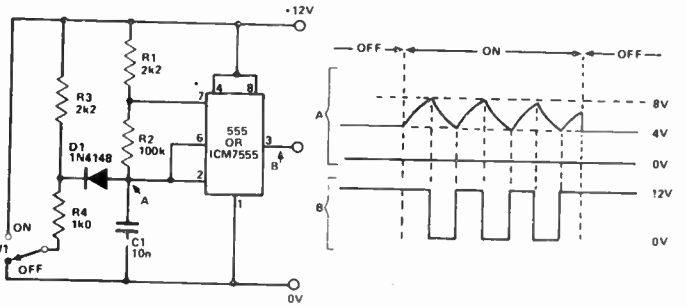



*Figure 4.* **Modification of the C1 gating scheme, giving constant-period half-cycles.**

The conventional way of gating the 555/7555 astable is with the pin 4 reset terminal, as shown in Figure 2. When this pin is pulled to ground (by a 1k resistor), the flip-flop output is driven high, thus discharging C1 through R2 and the transistor and also driving the output (pin 3) low. The resulting circuit waveforms are shown in the diagram. Note that, when the astable is gated on, the first half cycle is considerably longer than the succeeding half cycles. Also note that, when the astable is first gated off, the voltage across C1 takes a substantial time to decay to zero. The output is zero during the off condition.

## Alternative methods

One alternative method of gating the 555/7555 is shown in Figure 3. Here, when the circuit is gated on, D1 is back-biased and the astable operates in the normal way, but when the circuit is gated off D1 shorts out C1 and pulls point A to ground; in practice, of course, SW1 can be replaced by an electronic switching waveform (the output of a CMOS gate, etc). Note in this circuit that, when the astable is gated on, the first half cycle is again considerably longer than the succeeding half cycles, but that the C1 voltage falls abruptly to zero at gate-off. Also note that the output is high in the off state, here.

Figure 4 shows how the above circuit can be modified so that the duration of the first half cycle is almost equal to that of the succeeding half cycles. This is achieved by choosing the R3-R4 values so that the voltage across C1 is only a fraction below 4 V (one-third of supply volts) during the off condition. A substantially different set of waveforms can be obtained by choosing the R3-R4 values so that the voltage across C1 is a fraction below 8 V (two-thirds of supply volts) during the off condition, as shown in Figure 5.

It should be appreciated that the 555/7555 astable can only oscillate if its timing capacitor (C1) is free to swing between the 4 V and 8 V switching levels. This simple fact makes it possible to voltage-gate the astable by using the circuit of Figure 6. Here, the circuit produces output waveforms only when the input voltage exceeds 8 V. The circuit can be made to trigger at other levels by giving the op-amp an appropriate voltage gain factor.

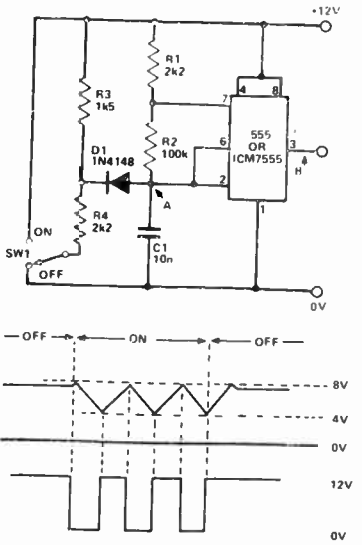



*Figure 5.* **This slight modification of the C1 gating scheme produces a considerable change in the circuit output waveforms.**

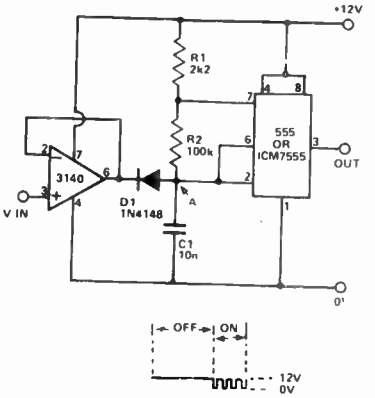



*Figure 6.* **The voltage-controlled astable produces an output only when $V_{in}$ exceeds two-thirds supply (8 V in this example).**

# Lab Notes

Finally, an alternative method of gating the 555/7555 astable is shown in Figure 7. Here, the circuit is gated off by driving the voltage across C1 above 8 V by D1. A feature of this circuit is that its 'B' output is low in the off condition.

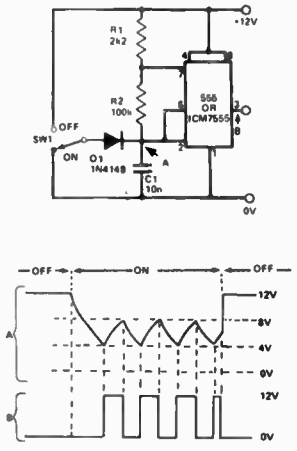



*Figure 7.* **This C1 gating scheme produces a 'B' output that is low in the off condition.**

## Asymmetrical astables

The basic 555/7555 astable generates near-symmetrical output waveforms, provided that R2 is large relative to R1 (giving near-equal C1 charge and discharge time constants). Figures 8 to 10 show alternative methods of generating non-symmetrical waveforms. In Figure 8, C1 charges through R1-R2 but discharges through R2 in parallel with R3-D1, to produce the waveforms shown. In Figure 9, C1 charges through R1 and R2 in parallel with R3-D1, but discharges through R2 only; this circuit is useful for providing narrow output pulses at the 'B' terminal.

Finally, in Figure 10, C1 charges through R1-R3-D2 and discharges through D1-RV1-R1-R2, to produce narrow output pulses at the 'B' terminal. This circuit is useful for generating variable-frequency constant-width pulses.

## Sine waves

Figure 11 shows how a sine wave signal can be obtained from a 555/7555 astable. Here, the symmetrical ramp waveform of C2 is buffered by Q1 and then ac coupled to the R1-R2-D1-D2 divider/limiter network. This network attenuates the ramp signal and then non-linearly removes the ramp's positive and negative peaks, to produce a sine-shaped waveform of about 1 V peak-to-peak amplitude at the output terminal. The distortion level of the resulting sine wave is typically of the order of 3% and its frequency can be varied from a few cycles per minute to several hundred kilohertz by suitable choice of the value of C2.

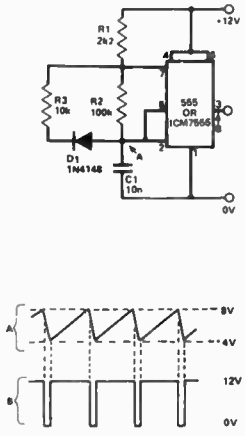



*Figure 8.* **A method of producing a non-symmetrical fixed ratio from the 555 astable.**

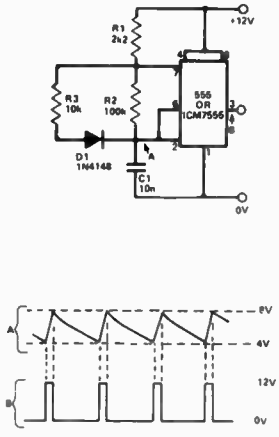



*Figure 9.* **Alternative method of producing a non-symmetrical fixed ratio output from the 555 astable.**

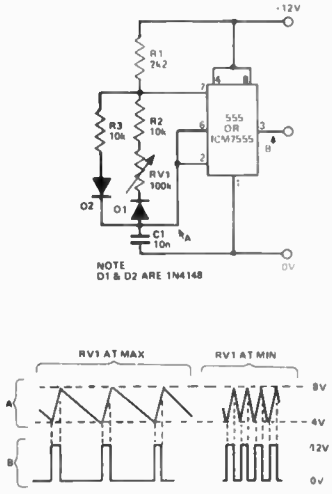



*Figure 10.* **A method of producing a non-symmetrical variable ratio output from the 555 astable.**

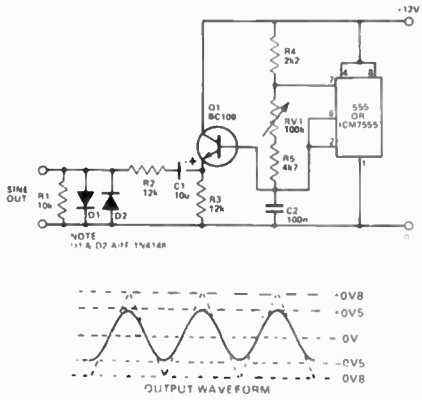


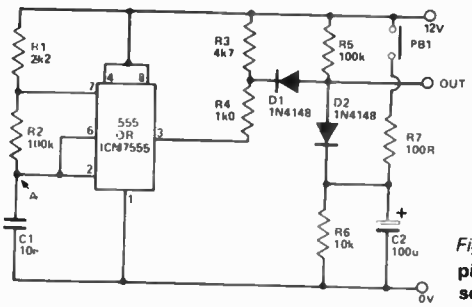

*Figure 11.* **A 555 sine wave generator with a range of 83 Hz to 1.4 kHz (via R1).**

## AM output

Figure 12 shows how the pin 3 square wave output of the 555/7555 astable can be amplitude-modulated to produce the typical attack-hold-decay envelope of a simple musical instrument or of a special-effects sound generator. The heart of the unit is the diode AND gate, or mixer, formed by D1-D2-R5. One input of this gate is fed from the output of the astable via R3-R4 and the other from across R6. The basic action of this gate is such that (ignoring the diode volt drops) its output amplitude is equal to the lesser of the two inputs.

Thus, when D1 is fed with the square wave output of the astable, the peak output of the unit will be zero when the voltage across R6 is zero, or 5 V when the voltage across R6 is 5 V, etc. In our circuit, R6 is shunted by electrolytic capacitor C2. Thus, when PB1 is pressed, a large voltage is applied to R6 and a large-amplitude square wave output is available. When PB1 is released, the voltage across R6 and the square wave output amplitude decay exponentially to zero (with a time constant of R6-C2), as shown in the diagram. The R3-R4 network is used to apply a slight offset bias to the rectangular input waveform, to ensure a full cut-off of the output waveform after PB1 is released.

Finally, Figure 13 shows how the above circuit can be modified to give extended decay times (via emitter follower Q1) and a buffered audio output (via emitter follower Q2). ●



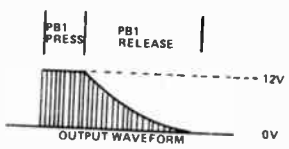




*Figure 12.* **A method of amplitude-modulating the pin 3 output off the 555 astable in music and sound generator applications.**

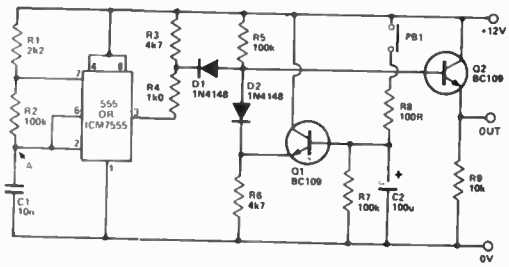



*Figure 13.* **A modification of the Figure 12 circuit to give extended decay times and a buffered output.**

# Lab Notes

# A look at the versatile 4046B

The 4046B CMOS chip is probably one of the most versatile and least-used of all the ICs in the CMOS range. The device glories in (or suffers from) the descriptive title of 'micropower phase-locked loop' and there is a widespread misconception amongst many electronics amateurs and professionals that the device can only be used in PLL-type applications. In fact nothing could be further from the truth.

**Ray Marston**

THE 4046B CONTAINS a pair of phase-comparators, a zener diode and one VCO or voltage-controlled oscillator. All of these sections are independently accessible via the IC pin-outs. The VCO section of the device is probably the most versatile and cost-effective voltage-controlled oscillator on the market. It produces a well-shaped symmetrical square wave output, has a top-end frequency limit in excess of 1 MHz, can be voltage-scanned through a 1 000 000:1 range (1 Hz to 1 MHz) when used with a single timing resistor or through any range from 1:1 to infinity (0 Hz to 1 MHz) when used with a pair of timing resistors.

If that were not enough, the voltage-controlled oscillator can also be independently gated on and off via an INHIBIT terminal, can be operated from any supply in the range 3-18 V and can, when used in conjunction with one of the 4046B's phase comparators, produce a two-phase output. The linearity of the VCO is typically a healthy 1% or so.

## 4046B VCO circuits

Figure 1 shows the internal block diagram and the pinouts of the 4046B phase-locked loop IC. The device contains two types of phase comparator, a VCO and a zener diode. In practical PLL applications, the VCO and one or other of the comparators are interconnected to form a 'loop', which causes the VCO to lock to the mean frequency of an input signal connected to pin 14.

For our present purposes the most important element of the IC is the VCO,

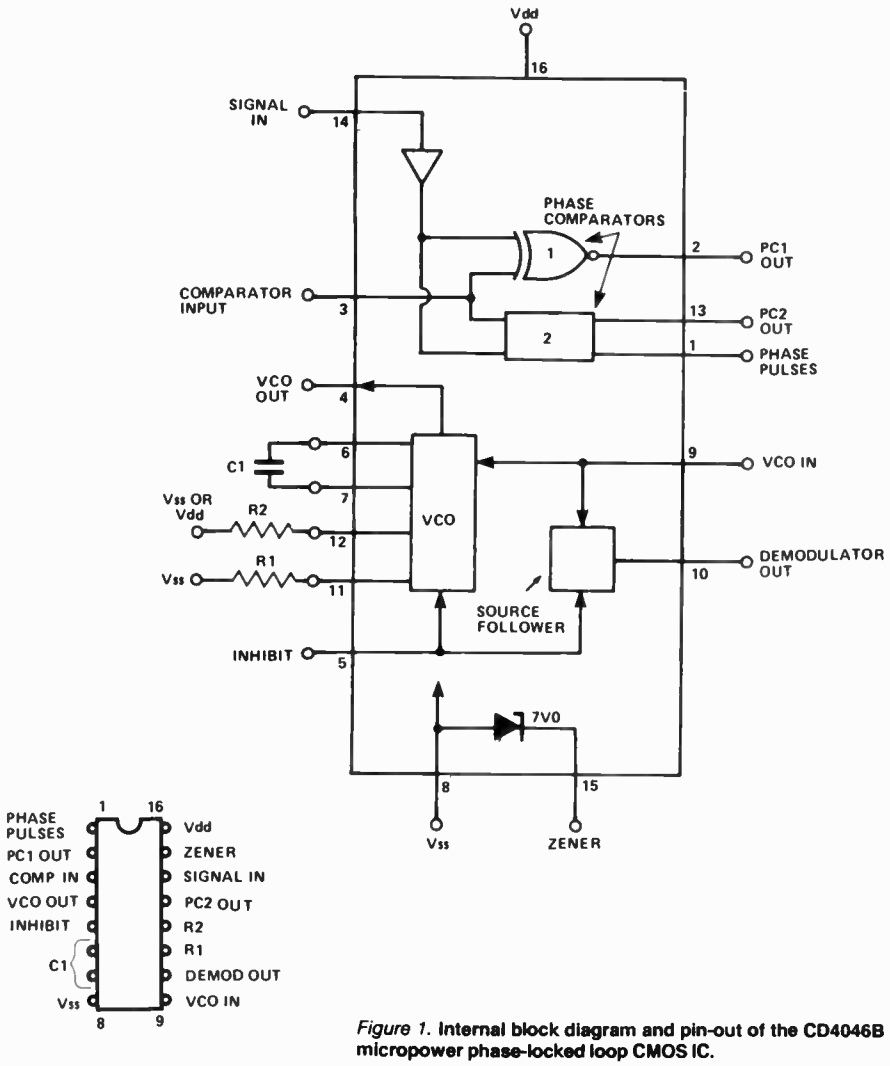



*Figure 1.* **Internal block diagram and pin-out of the CD4046B micropower phase-locked loop CMOS IC.**

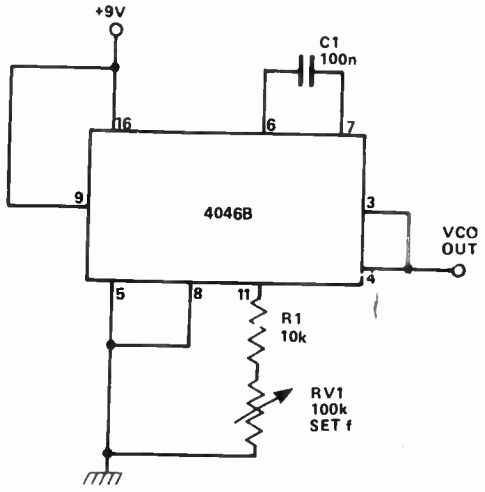



*Figure 2.* **Simple variable-frequency (200 Hz to 2 kHz) square wave generator.**

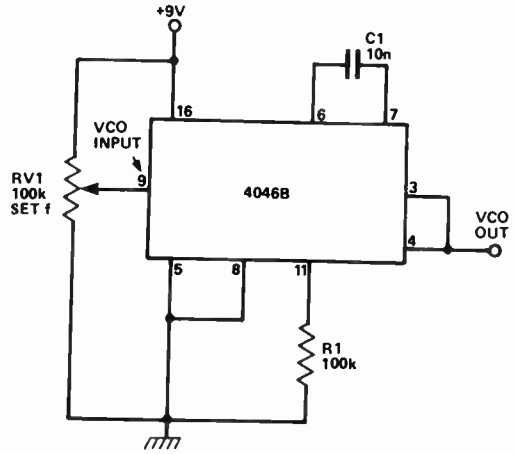



*Figure 3.* **Wide range VCO with frequency variable from near zero to 1.4 kHz via the pin 9 voltage.**

or voltage-controlled oscillator. The operating frequency of the oscillator is governed by the value of a capacitor connected between pins 6 and 7 (minimum value 50 pF), by the value of a resistor wired between pin 11 and ground (minimum value 10k) and by the voltage applied to VCO-input pin 9 (any value up to the supply voltage in use).

Figure 2 shows the simplest possible way of using the VCO section. Here, the pin 9 'voltage control' input is tied permanently high and the circuit acts as a basic square wave oscillator, with its frequency variable over a 10:1 range by RV1. Note at this point that the VCO output (pin 4) is tied directly to the pin 3 phase comparator input. If pin 3 is allowed to float, the comparators tend to self-oscillate at about 20 MHz and superimpose an HF signal on the top part of the VCO output waveform.

## Ranging far and wide

Figure 3 shows how to connect the 4046B as a wide-range VCO. Here, R1-C1 determine the top (maximum) frequency that can be obtained and RV1 controls the actual frequency via the pin 9 voltage. The frequency falls to near zero (a few cycles per minute) with pin 9 at 0 V. The effective control range of pin 9 varies from roughly 1 V below the supply value to 1 V above zero, i.e: RV1 has a 'dead' control area of several hundred millivolts at either end of its range.

Figure 4 shows how these 'dead' areas can be eliminated by wiring a silicon diode in series with each end of RV1. The circuit also shows how the minimum operating frequency can be reduced to absolute zero by wiring a high value resistor (R2) between pins 12 and 16. Note here that, when the frequency is reduced to zero, the VCO output randomly settles in either the logic 0 or logic 1 state.

Figure 5 shows how the pin 12 resistor can alternatively be used to determine the minimum operating frequency of a restricted-range VCO. Here, $f_{min}$ is determined by R2-C1 and $f_{max}$ is determined by C1 and the parallel resistance of R1-R2.

Figure 6 shows an alternative version of the restricted-range VCO, in which $f_{max}$ is controlled by R1-C1 and $f_{min}$ is determined by C1 and the series com-

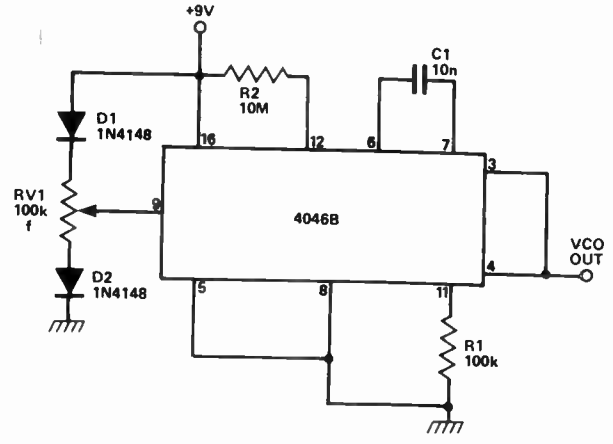



*Figure 4.* **Wide range VCO with frequency variable down to absolute zero.**

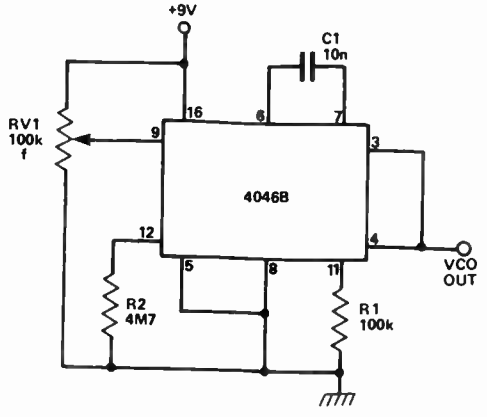



*Figure 5.* **Restricted range VCO with frequency variable from 60 Hz to 1.4 kHz by RV1. R2 acts as an offset resistor.**

# Lab Notes

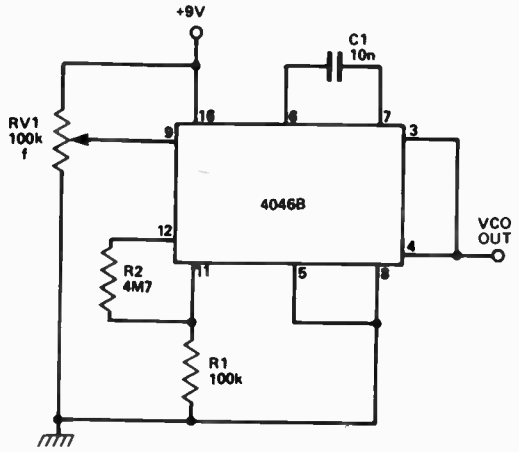



*Figure 6.* **An alternative restricted range VCO, in which $f_{max}$ is controlled by R1-C1 and $f_{min}$ by (R1 + R2)-C1.**

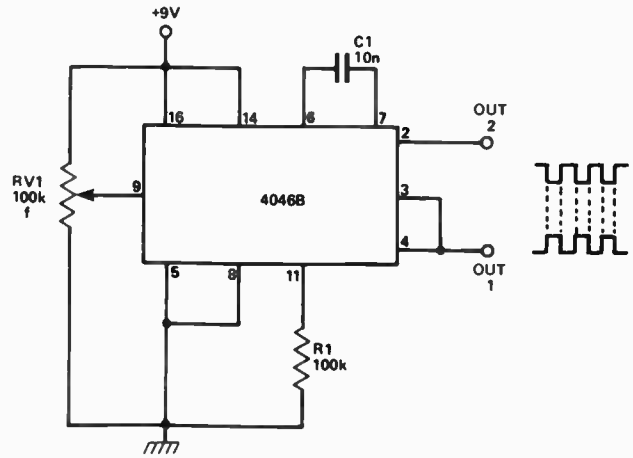



*Figure 7.* **A two-phase wide-range VCO.**

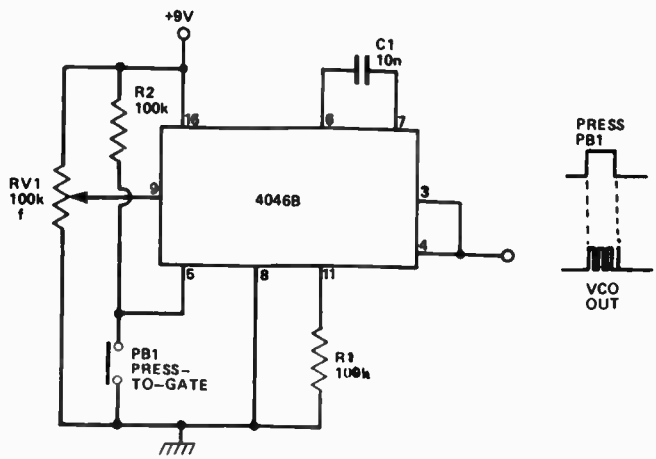



*Figure 8.* **A manually gated wide-range VCO.**

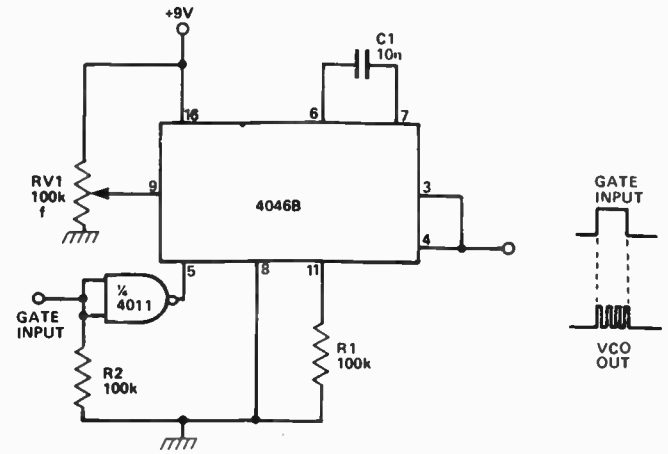



*Figure 9.* **An electronically gated wide-range VCO, using an external gate inverter.**

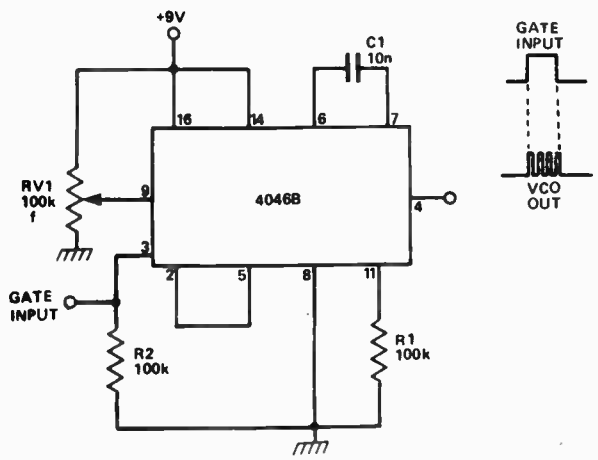



*Figure 10.* **An electronically gated wide-range VCO using the internal EX-OR phase detector for gate inversion.**

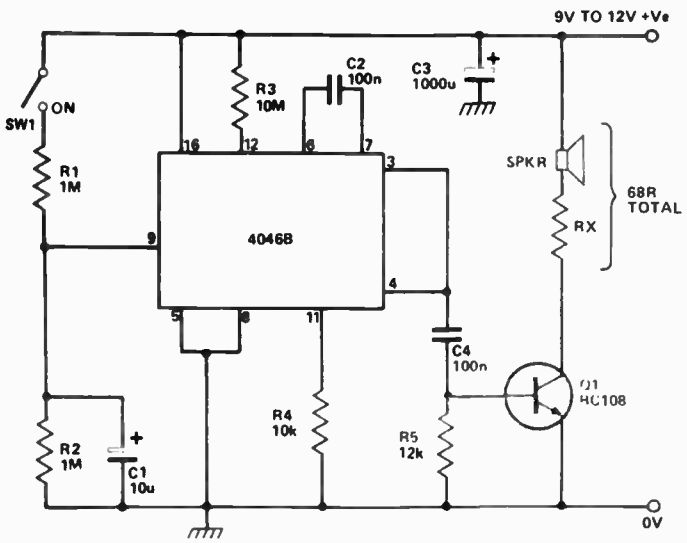



*Figure 11.* **An electronic siren giving slow rise and fall of its operating frequency.**

bination of R1 and R2. Note that, by suitable choice of the R1 and R2 values, the restricted-range VCO can be made to span any range from 1:1 to near infinity.

## Square pair

The VCO can be made to generate a pair of anti-phase square wave outputs by connecting its output to the phase-comparator input, taking the signal input (pin 14) high and taking the anti-phase output from pin 2. Figure 7 shows the connections. Note that this circuit makes use of the IC's built-in EX-OR gate (phase comparator 1).

The VCO section of the 4046B can be disabled by taking pin 5 of the package high (to logic level 1). This feature enables the VCO to be gated on and off by external signals. Figure 8 shows how the VCO can be manually gated via a pushbutton connected directly to pin 5, while Figure 9 shows how the circuit can be gated electronically by an external gate inverter. Alternatively, if the two-phase output facility is not required, the internal EX-OR phase detector can be used to provide gate inversion, as shown in Figure 10. Note in this latter case that pin 4 is not connected to pin 3.

## Sirens and sound effects

Figures 11 to 14 show some practical siren and sound effects generator VCO circuits. Figure 11 is a conventional siren circuit. When SW1 is closed, C1 charges exponentially via R1 and the VCO frequency rises slowly from zero to a maximum value. When SW1 is opened, C1 discharges via R2 and the operating frequency slowly decays to zero. The VCO output is ac-coupled to the speaker via C4 and Q1.

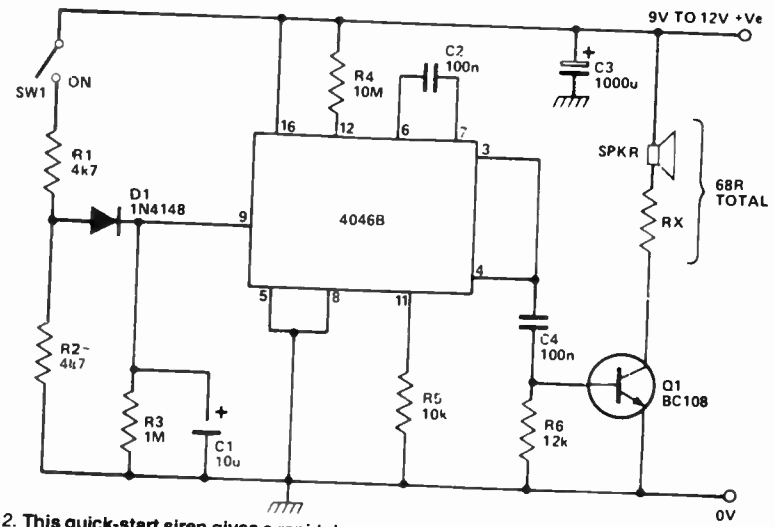



*Figure 12.* **This quick-start siren gives a rapid rise and slow fall of its operating frequency.**

The Figure 12 quick-start siren is similar to the above, except that C1 charges rapidly to half supply volts via R1, R2 and D1 when SW1 is closed and discharges slowly via R3 when SW1 is opened.

The Figure 13 circuit produces a 'phaser' sound when PB1 is closed. The 4011 astable is gated by PB1 and produces a chain of 4 ms pulses at intervals of 70 ms. Each pulse rapidly charges C2 via R3 and D2, to produce a high tone that then decays rapidly as C2 discharges via R5, only to be repeated again on the arrival of the next pulse.

The Figure 14 circuit generates either a pulsed tone or a warble tone signal (depending on the setting of SW1) when PB1 is closed. PB1 is used both to enable pin 5 of the 4046B and to gate on the 4001 astable, which then applies a rectangular (alternatively fully high and fully low) waveform to pin 9. In the pulsed mode the VCO generates zero frequency when pin 9 is low. In the warble mode it generates a tone that is 20% down on the high tone when pin 9 is low.

## Miscellaneous VCO circuits

Figures 15 to 17 show a miscellany of 4046B VCO circuits. The Figure 15 circuit is that of an FSK generator which produces a 2.4 kHz tone when a logic 1 signal is applied to pin 9 and a 1.2 kHz tone when a logic 0 signal is

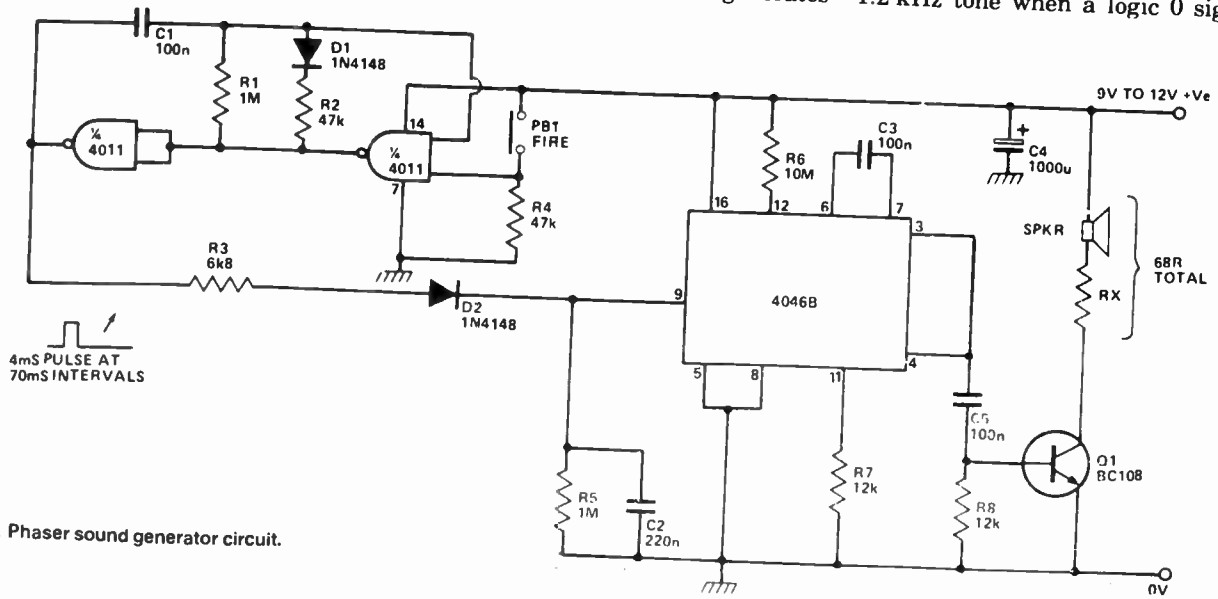



*Figure 13.* **Phaser sound generator circuit.**

# Lab Notes

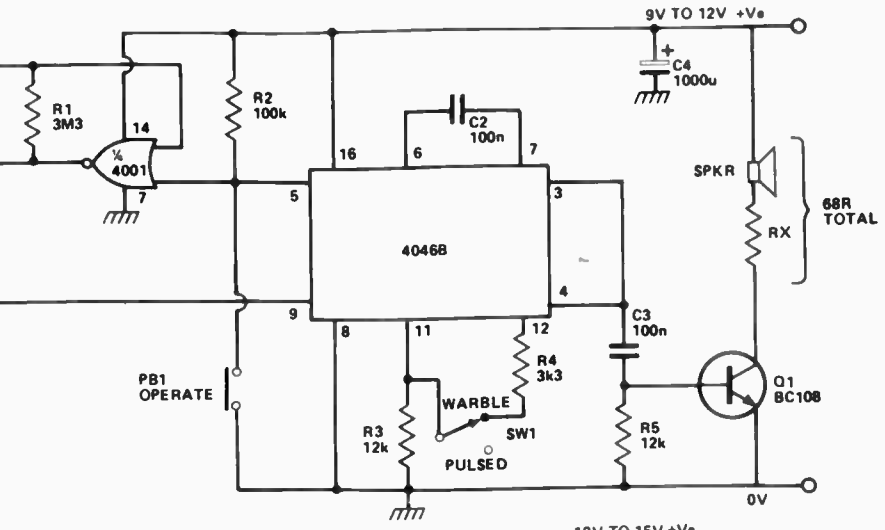



*Figure 14.* **Combined pulsed tone/warble tone alarm generator. The high tone is determined by R3, the low tone by (R3+R4).**

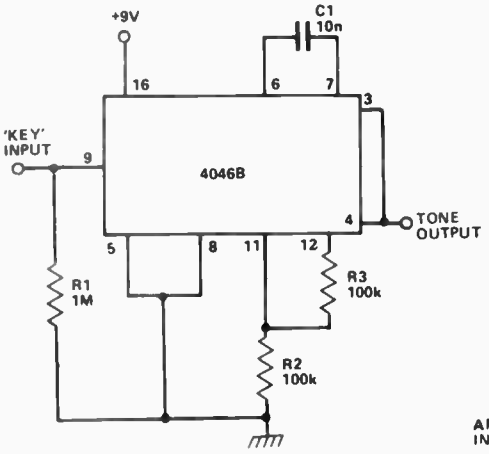



*Figure 15.* **FSK generator — logic 0=1.2 kHz, logic 1=2.4 kHz.**

applied. The high tone is controlled by R2 and the low tone by R2 and R3.

Figure 16 is a 220 kHz FM generator. The internal zener of the 4046B (pin 15) is used to provide a stable 7 V supply to the x20 3140 inverting amplifier, which is quiescently biased at 3.5 V by the R2-R3 potential divider. The pin 9 VCO signal is thus a mean 3.5 V potential amplitude modulated by an amplified version of the AF input signal, which thus frequency-modulates the output of the VCO.

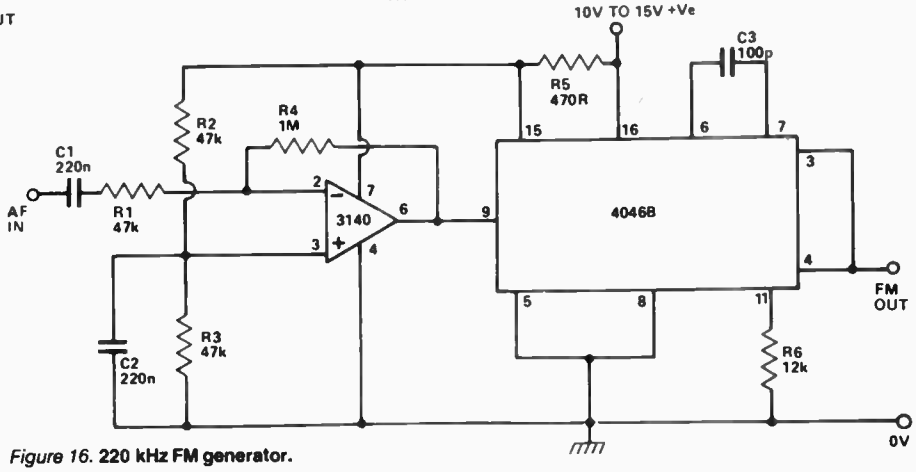



*Figure 16.* **220 kHz FM generator.**

## Running down

The Figure 17 circuit is that of a run-down clock generator of the type used in dice and roulette games. When PB1 is pressed, C1 charges to a high voltage via D2. Simultaneously, Q1 is biased on via D3-D4 and effectively connects R6 between pin 11 and ground. Under this condition, the VCO operates a high frequency (tens of kHz) and effectively generates a random number of clock pulses. When PB is released, Q1 turns off and the VCO timing is governed by R8. Simultaneously, C1 rapidly discharges to half supply volts via R1-R2-D1, so the VCO operates at only 100 Hz or so. C1 then slowly discharges via R3 and the VCO frequency slowly decays to zero over a period of about 15 seconds. ●

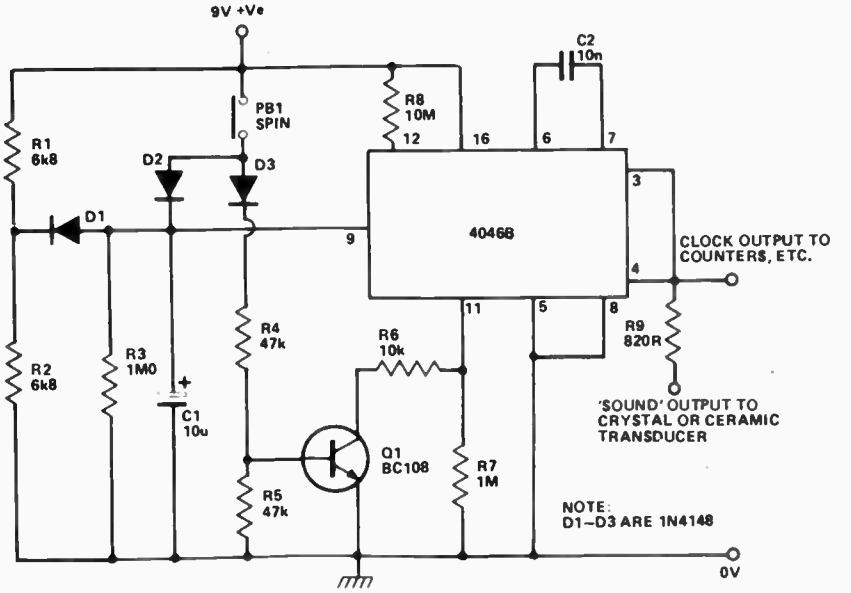



*Figure 17.* **Run-down clock/sound generator for use in dice/roulette games. The circuit is suitable for use with edge-sensitive clock circuits only. The output can be used to directly clock most types of counter and can be fed, via R9, to crystal or ceramic transducers to directly produce 'run down' sounds. When the run-down is complete this circuit may settle in either logic 0 or 1, so it cannot safely be used to clock level-sensitive circuitry.**

# Lab Notes

# Remote control systems

Multi-channel remote control systems have many applications outside the radio control of models. Here, our correspondent illustrates a number of circuits that readers may find useful — all using commonly available components.

**Ray Marston**

SIMULTANEOUS multi-channel remote control systems, giving either fully proportional or simple on/off action (or a combination of the two) are widely used by the model plane, boat and car fraternities. A typical system has eight channels, each using width-modulated pulses as control signals.

In the transmitter, eight manually actuated pots (in a proportional system) or switches (in an on/off system) are sequentially sampled at a fixed rate by an encoder circuit, which at each sample point generates a pulse with a width proportional to the state of the device being tested. The output of the encoder consists of a repeating series of 'frames' of eight width-controlled pulses followed by a synchronisation pulse, all presented in serial form.

Typically, in an 8-channel proportional system, the width of the controlled pulses may be variable from 0.5 ms to 1.5 ms (depending on the settings of individual control pots), the sync pulse width may be 3 ms, the sample period 2 ms and the frame width 20 ms.

## Servo code

The serial output of the encoder is coupled via a suitable 'link' to the input of a decoder circuit that is located in the remote receiver. The link may take the simple form of two wires (or only one if a ground return is used), or the more complex form of a modulated radio, ultrasonic, infrared, or magnetic signal, etc. The decoder circuit detects the sync pulse in each frame, and then counts the individual controlled pulses in the frame and routes each one to its own output terminal. There it may be fed to an electronic switch or a servo-mechanism which will reconstruct the original mechanical control movement that took place at the transmitter.

The 'heart' of the remote control system described above is the encoder and decoder. As already mentioned, the actual 'link' can take any one of a variety of forms. The basic control system is highly versatile and has a vast number of untapped potential applications. The number of channels that can be simultaneously controlled can range from two to dozens (or even hundreds). In on/off applications, the outputs can easily be binary decoded to give non-simultaneous on/off control of a vast number of remote devices: an 8-channel system can, for example, control 256 devices, or a 12-channel system can control 4096.

The system can readily be adapted to give remote operation of lamp dimmers, volume controls, 'combination' locks and garage doors, or independent on/off control of hundreds of household fittings via signals pumped down the mains wiring. You can even, if it takes your fancy, use the system to remote control a full-sized piano from the comfort of an armchair via a hand-held keyboard and an infrared link!

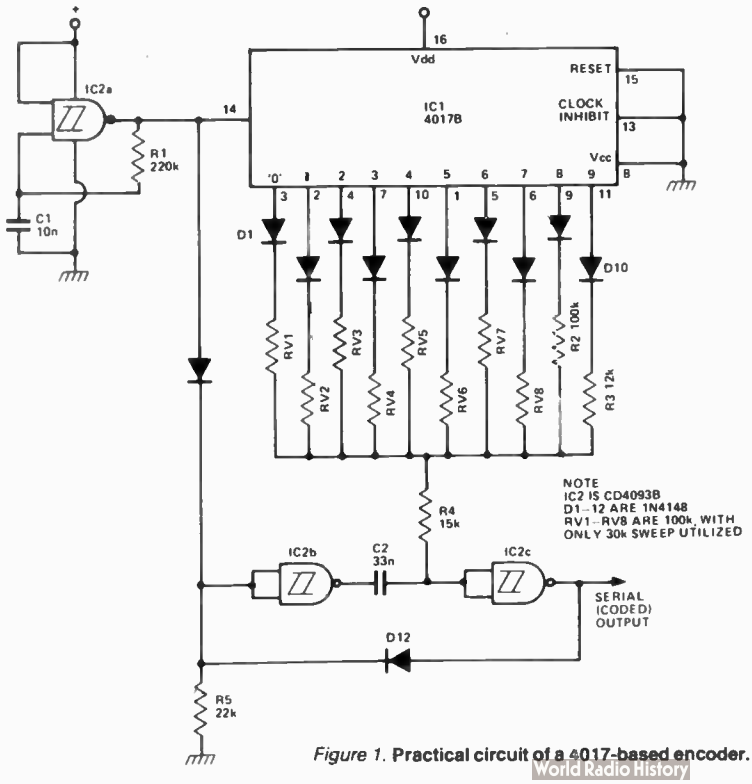



*Figure 1.* **Practical circuit of a 4017-based encoder.**

## An 8-channel proportional control encoder

Figure 1 shows the practical circuit of a 4017-based 8-channel encoder for use in simultaneous control systems. IC2a is a 500 Hz (2 ms) astable multivibrator that simultaneously feeds clock signals

to the input of the 4017 and trigger signals to the input of the IC2b-IC2c monostable multivibrator. In any given clock cycle, the period of the monostable is determined by C2-R4 and by the resistance value in series with the relevant 'high' output of the 4017. In clock cycles '0' to '7' the pulse widths are determined by the settings of RV1 to RV8 respectively. In the '8' clock cycle the pulse has a width equal to the clock cycle period (2 ms), and in the '9' clock cycle the pulse is fixed at about 1 ms, thus giving a composite 3 ms sync pulse from the eighth and ninth cycles. The system is designed to give a fixed 20 ms frame width.

Note that, in conformance with normal practice, only one third (or less) of the sweep ranges of RV1 to RV8 are utilised. In practice, component values may have to be altered slightly to give precise ranges of coded output pulse widths.

## An 8-channel proportional control decoder

Figure 2 shows the circuit of a decoder for use with the above system. The incoming 'coded' waveform is fed simultaneously to the clock terminal of the 4017 and to the trigger terminal (via C1-R1-D1) of the IC2c-IC2d monostable. IC2c of this monostable produces a negative-going pulse with a period slightly less than the 2 ms clock period (about 1.8 ms), and this negative pulse is ANDed with the positive clock signal by IC2a and IC2b to produce a reset output signal from the 3 ms input sync pulse, but not from the 'control' pulses, which all have periods significantly less than the 1.8 ms reference value.

Note that the value of R3 may have to be adjusted on test to set the correct reference period.

Outputs 1 to 8 of the 4017 are sequentially ANDed with the coded clock input signal once the counter has been reset by the sync pulse, so that each individual code pulse is routed to its own designated output terminal or channel. The individual outputs, which take the form of 0.5 ms to 1.5 ms pulses with repetition periods of 20 ms, can then be fed to suitable servos, etc, to convert the pulses into proportional mechanical movements.

## An 8-channel simultaneous on/off encoder

Multi-channel simultaneous on/off coder/decoder systems are technically no easier to implement than full proportional systems. In fact they are often more difficult. Figure 3 shows a practical example of a simultaneous 8-channel on/off control encoder.

Here, astable multivibrator IC2a simultaneously feeds 500 Hz clock signals to the 4017, to the IC3a-IC3b 200 $\mu$s monostable multi, and to one input terminal of the IC2b-IC2c AND gate. The other input of the AND gate is sequentially taken from the '0' to '7' outputs of the 4017 via any of the PB0 to PB7 switches that are closed, and directly from the '9' output. The outputs of the AND gate and the 200 $\mu$s monostable, plus the direct '8' output of the 4017, are all ORed to produce the final serial coded output across R4.

The final output waveform comprises 200 $\mu$s pulses and 1 ms pulses to represent off and on switch states respectively, plus a 3 ms sync pulse spanning the eighth and ninth clock cycles.

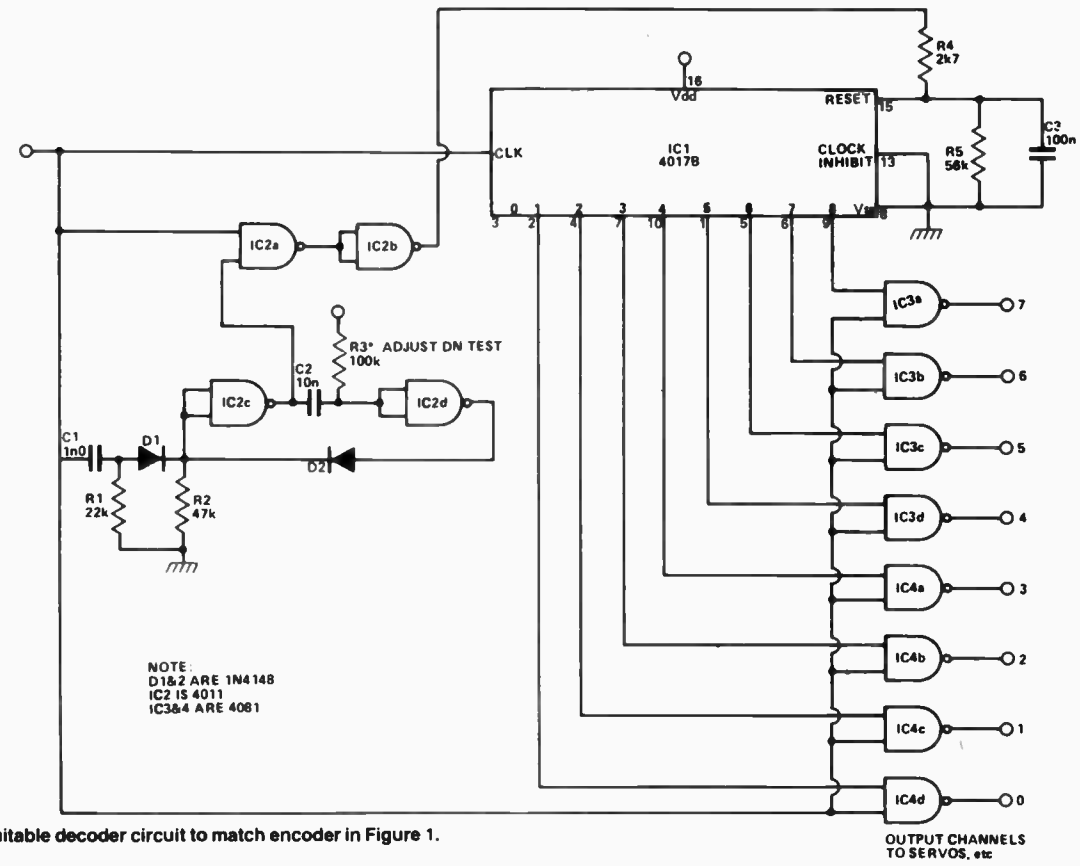



*Figure 2.* **Suitable decoder circuit to match encoder in Figure 1.**

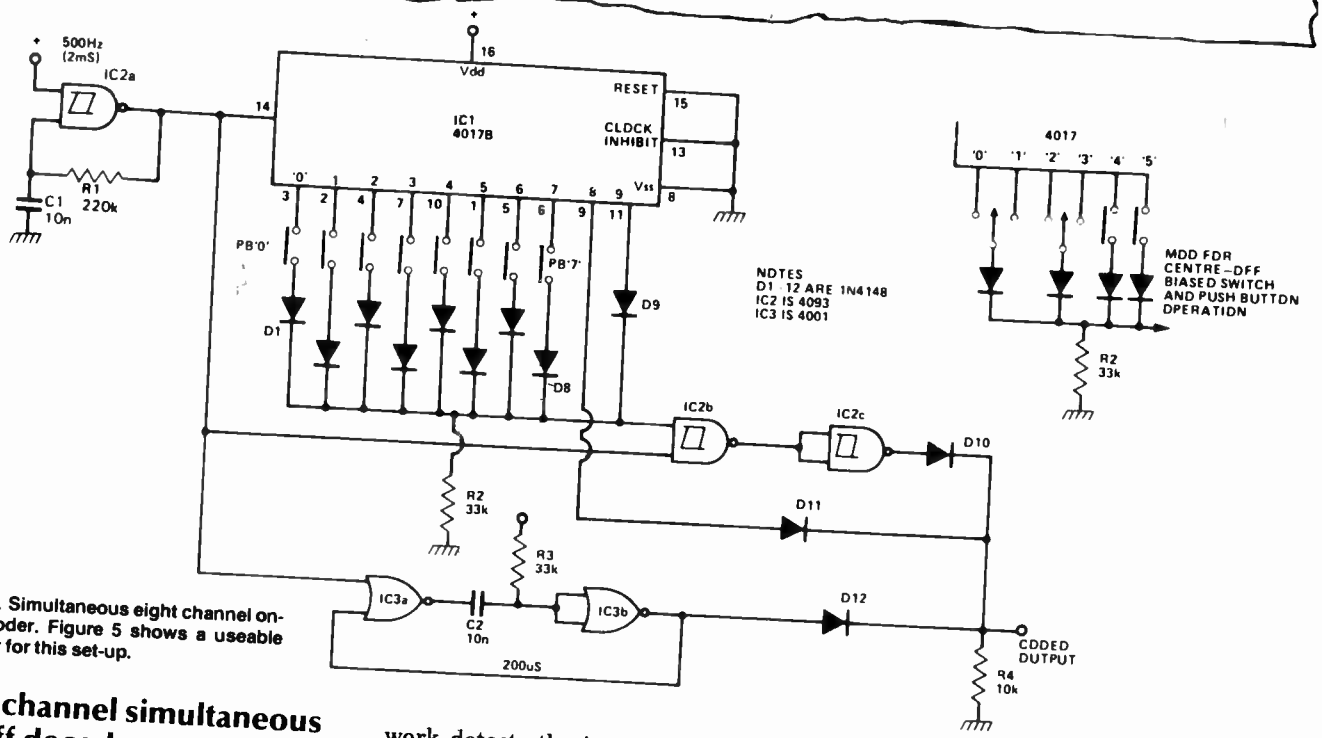



*Figure 3.* **Simultaneous eight channel on-off encoder. Figure 5 shows a useable decoder for this set-up.**

## An 8-channel simultaneous on/off decoder

Figure 5 shows a decoder circuit that is suitable for use with the above encoder. Here, the IC3a-IC3b-IC2a-IC2b network detects the input sync pulse and then resets the counter, and the IC3c-IC3d-IC2c-IC2d network detects 'wide' (1 ms) or 'on' code pulses and then ANDs the selected output of the 4017 via the IC4-IC7 array to produce a high potential on the appropriate output channel. Note that the purpose of the D-R-C network in each output channel is to convert a detected 'wide' pulse into

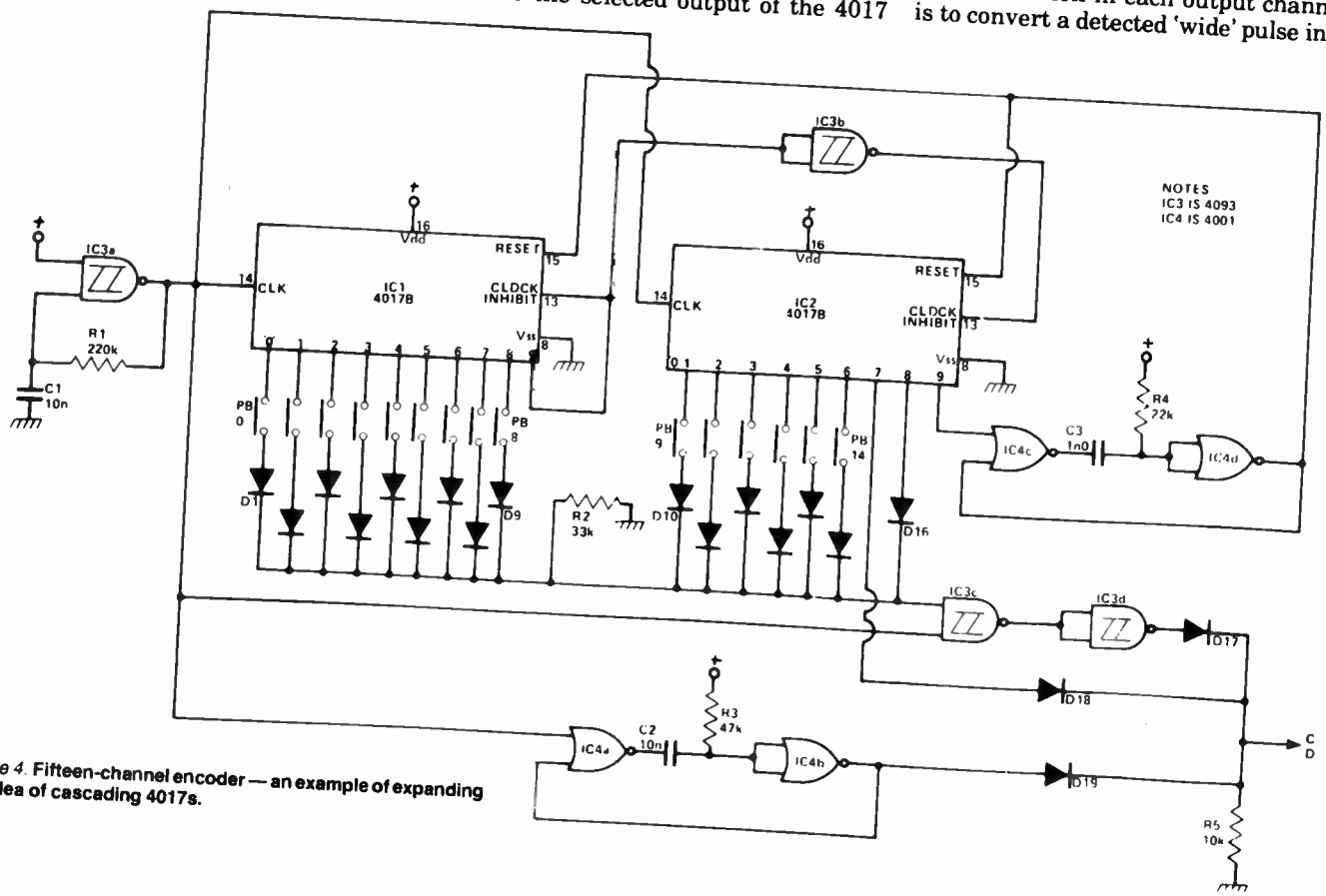



*Figure 4.* **Fifteen-channel encoder — an example of expanding the idea of cascading 4017s.**

a steady dc voltage that will remain high (or low) for greater than one frame period. Note that the (non-pulsed) outputs of the eight channels of this system can readily be binary decoded to make a total of 256 non-simultaneous channels available.

## Expanded multi-channel systems

All of the coder/decoder circuits presented here can be expanded to incorporate any number of channels (with appropriate increases in frame periods and miscellaneous timing component values) by using multi-stage 4017 counter networks in place of the single counters shown. Figure 4 shows the connections for a 15-channel system and more elaborate systems can obviously be built up on the same lines.

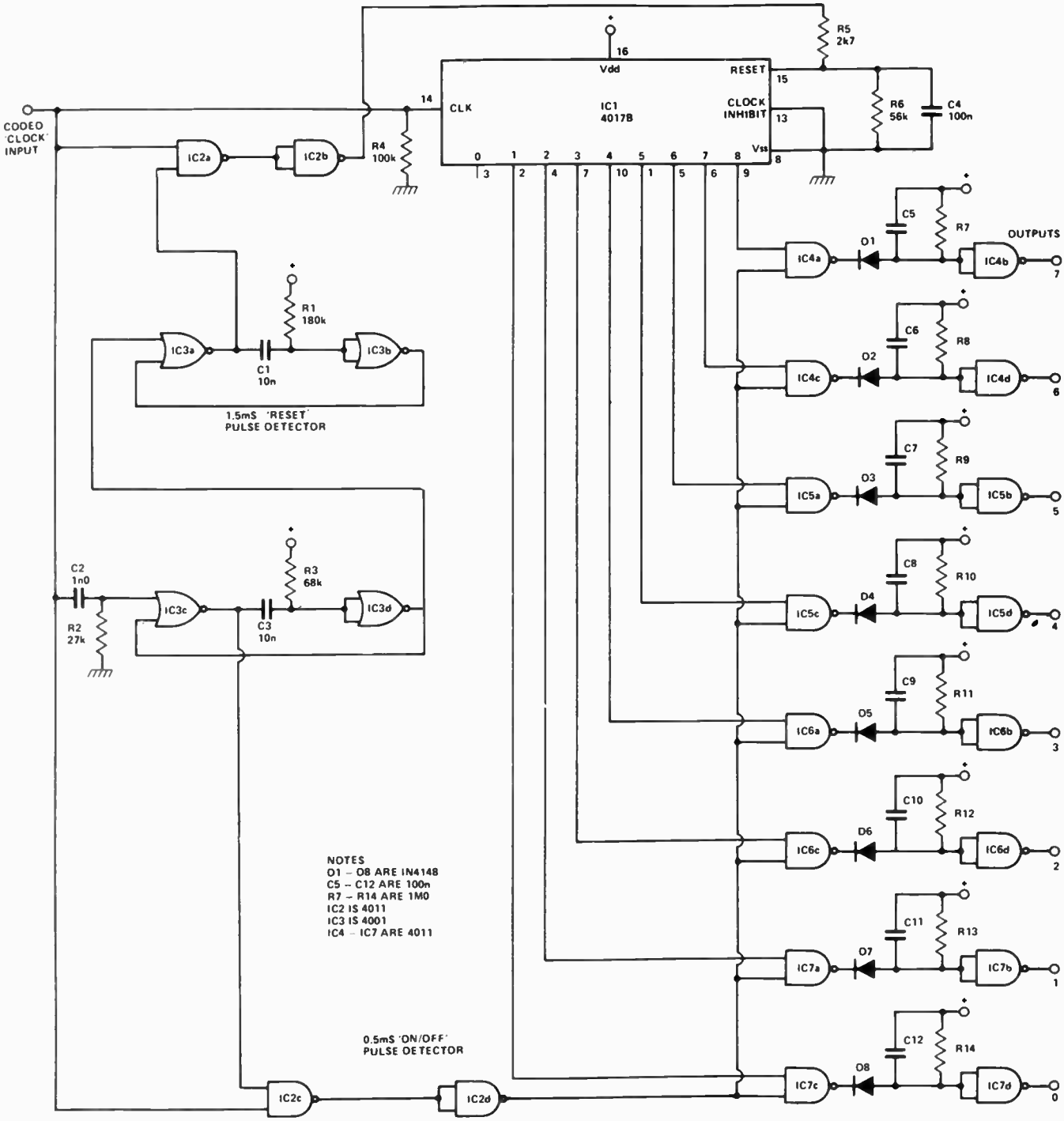



*Figure 5.* **Eight-channel decoder which will operate as a system with either encoder (Figures 3 or 4).**

# Lab Notes

# Electronic switching — using the 4066B

There are many applications where mechanical switches and relays just won't do the job you want. The answer? — an electronic switch. The most popular and versatile is the 4066B quad bilateral switch — a CMOS package containing four electronically actuated single-pole single-throw (SPST) switches.

**Ray Marston**

THE 4066B CMOS IC is described in the manufacturer's literature as a 'quad bilateral switch', a pretty fair description since the device contains four independent electronic switches, each capable of passing signals in either direction and being controlled (turned on or off) by a single high-impedance terminal. The switches have a very high off impedance, an on impedance of about 90 ohms, and can be used to switch both analogue and digital signals.

## Basic 4066B circuits

Figure 1 shows the outline and pin notations of the 4066B, which can be used with any supply voltage in the range 3 to 18 V. Note that, since the switches are of the bilateral type, either switch terminal can be used as the input or output.

Figure 2a shows the basic way of using the bilateral switch; each switch can be turned *off* (open circuit) by taking the control terminal to $V_{SS}$ *or* turned on by taking the control terminal to $V_{DD}$. In digital switching applications (Figure 2b) the IC can be used with a single-ended supply, with $V_{SS}$ at 0 V and $V_{DD}$ at the desired positive supply. In analogue switching applications (Figure 2c), a split power supply (either true or effective) must be used, with the positive rail to $V_{DD}$ and the negative to $V_{SS}$; in this case, of course, the maximum supply limits are restricted to ±9 V Typically, the bilateral switch introduces less than 0.5% signal distortion when used in the analogue mode.

Certain simple precautions must be observed when using the 4066B. First, the switch signals must in no circumstances be allowed to rise above the $V_{DD}$ voltage or fall below the $V_{SS}$ voltage. Each unused switch in the 4066B package must be disabled (see Figure 3) either by taking its control terminal to $V_{DD}$ or $V_{SS}$ (as most convenient), or by taking all three terminals to $V_{SS}$.

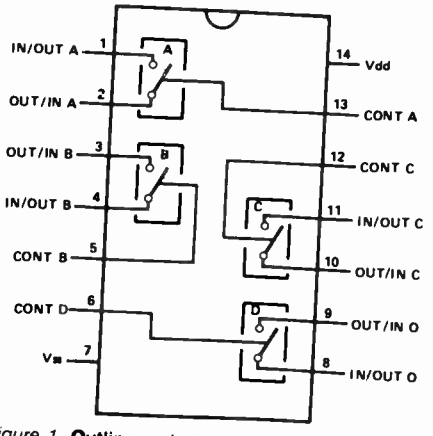



*Figure 1.* **Outline and pin notations of the 4066B quad bilateral switch.**

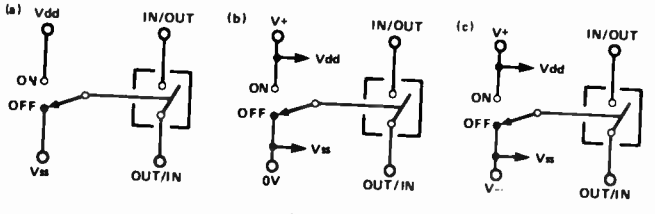



*Figure 2.* **(a) The basic bilateral switch is turned off by taking the control terminal to $V_{SS}$ and turned on by taking the control to $V_{DD}$. (b) In digital switching applications, $V_{DD}$ is V+ and $V_{SS}$ is 0 V. (c) In analogue switching applications where a split power supply is used, $V_{DD}$ must go to V+ and $V_{SS}$ to V−.**

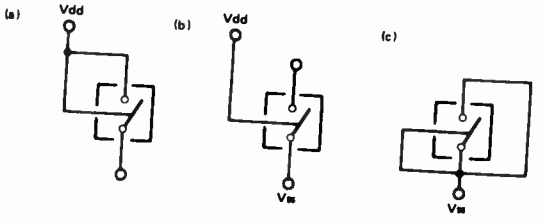



*Figure 3.* **Unused bilateral switches must be disabled, either by taking the control terminal to $V_{DD}$ and one of the switch terminals to $V_{DD}$ (a) or $V_{SS}$ (b), or by taking all three terminals to $V_{SS}$.**

# Lab Notes

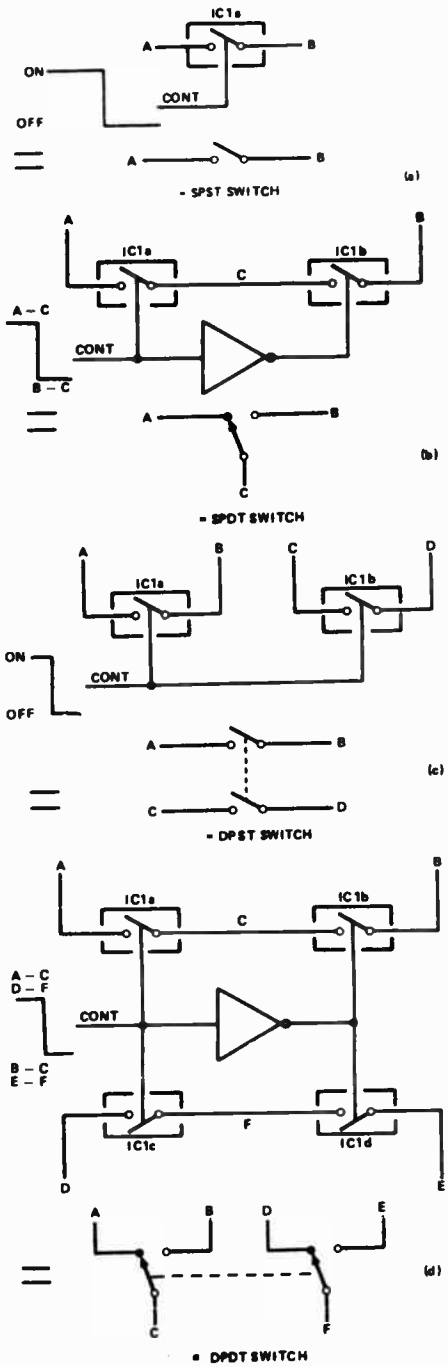



*Figure 4.* **Using the 4066B to implement the four basic switching functions.**

Figure 4 shows how the 4066B can be used to implement the four basic switching functions of SPST, SPDT, DPST and DPDT. Figure 4a shows the SPST connections, which we have already discussed. The SPDT function is implemented by wiring an inverter stage (a 4001 or 4011, etc) between the IC1a and IC1b control terminals as shown. The DPST switch (Figure 4c) is simply two SPST switches sharing a common control terminal, and the DPDT switch (Figure 4d) is two SPDT switches sharing a common inverter stage in the control line.

Note that the basic switching functions of Figure 4 can be expanded or combined in any desired way by simply adding extra switches/4066B packages, as appropriate. Thus, a 10-pole double-throw switch can, for example, be made by using five of the Figure 4d circuits and joining their control inputs together.

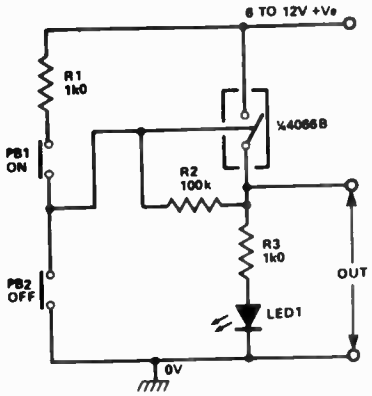



*Figure 5.* **Pushbutton latch using the 4066B.**

## Six latching circuits

Figure 5 shows how a 4066B switch can be used as a simple but very useful press-button activated latch; the LED is merely used to indicate the state of the latch, and can be replaced with a short circuit if preferred. Circuit operation is easily understood.

Suppose initially that the latch is off (switch open). In this case the output, and hence the control bias applied via R2, will be zero, so the switch will maintain its off state. If PB1 is now momentarily closed the control voltage will go high and turn the switch on, thus driving the output high and maintaining the control drive high (switch on) once PB1 is released. This new state will be maintained until PB2 is closed, at which point the switch will latch into the off state again. R1 is used in the circuit to ensure that a supply short will not occur if both buttons are pressed at the same time; with R1 in the position shown, the switch will turn off if both buttons are pressed at once; if R1 is moved to the low side of PB2, the switch will turn on if both buttons are pressed at once.

The Figure 5 circuit has a couple of interesting characteristics. First, the control bias resistor can be given any desired value up to practical limits.

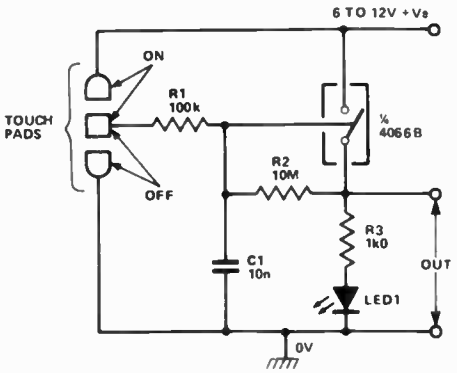



*Figure 6.* **A latching touch switch.**

Figure 6, for example, shows how the value can be increased to 10M to make a latching touch switch that can be activated by placing a finger across the upper or lower set of touch contacts. R1 and C1 are used to suppress hum signals and ensure positive switching.

Another useful feature is that, since the on resistance of the switch is only 90 ohms or so, the voltage loss across the switch can be quite low (90 mV at 1 mA); in practice, the on current should be limited to 10 mA maximum. Figure 7 shows how this low-loss effect can be used to connect or disconnect the power supply to a piece of electronic equipment (amplifier, test gear, etc).

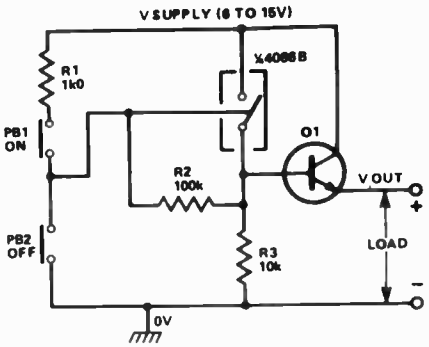



*Figure 7.* **This pushbutton activated power switch can be used to replace a conventional slide or toggle switch.**

When the switch is off, Q1 is cut off and the circuit consumes a typical standby current of less than 1 uA. When the switch is on, Q1 acts as a voltage follower with its base tied to the positive line via IC1a, so the output voltage is high. The actual voltage drop between the output and the supply is equal to the IC1a drop plus the base-emitter drop of Q1 and typically ranges from 600 to 800 mV. The available output current depends on the gain and current rating of Q1, but currents of a few hundred milliamps are readily available from a single transistor.

A slightly more efficient version of

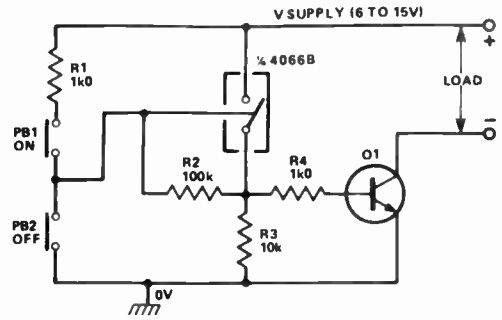



*Figure 8.* **An alternative version of the pushbutton power switch.**

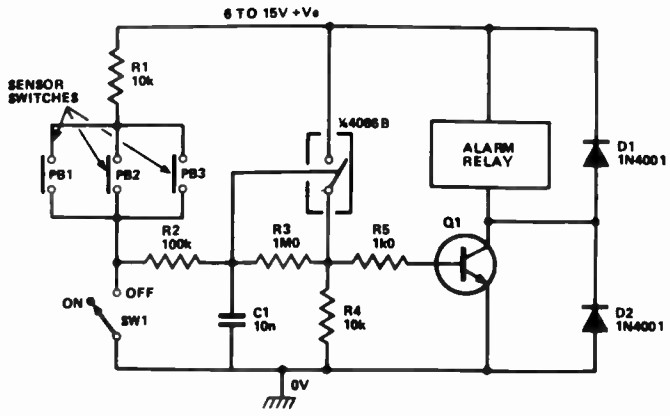



*Figure 9.* **A close-to-activate burglar/panic/fire alarm.**

the pushbutton power switch is shown in Figure 8. In this case the load is wired between the collector of Q1 and the positive supply rail. The voltage drop in this circuit is determined only by the saturation characteristics of Q1 and may typically be in the range 200 to 600 mV.

Figure 9 shows how the above circuit can be modified for use as a 'close-to-activate' burglar, panic or fire alarm, in which Q1 output feeds directly to a heavy duty 'alarm' relay which, in turn, actuates an external bell or siren. Any number of normally open sensors/switches can be wired in parallel in the 'PB' positions. The circuit consumes only a microamp or so when in the 'ready' or off mode.

Figure 10 shows the 4066 used in a multiplexer application where two inputs to a LED display (a pair of LM3915s) are switched alternately to provide a readout of 'average' and 'peak' signal levels. This was employed in our ETI-458 LED Level Meter, which featured 'twin-dot' display — the 'upper' dot showing peak signal level, the 'lower' one showing average. As the 4066 toggles between the two inputs the dot-mode display changes in like fashion. Because the toggling speed is so rapid (a few hundred Hertz), the persistence of vision makes the display seem to have two dots rather than one dot at a time. Two gates act as the multiplexing switches and two gates are arranged as an oscillator to drive them.

## Digital control

The 4066B can be used to digitally control or vary resistance, capacitance, impedance, amplifier gain or oscillator frequency in any desired number of discrete steps. Figure 11 shows how the four switches of a single 4066B can be used to vary the effective value of a resistance in 16 digitally controlled steps of 10k each. In practice, of course, the step magnitudes can be given any desired value (determined by the value of the smallest resistor) so long as the four resistors are kept in the ratio 1-2-4-8 and the on-resistance of 90 ohms is kept in mind.

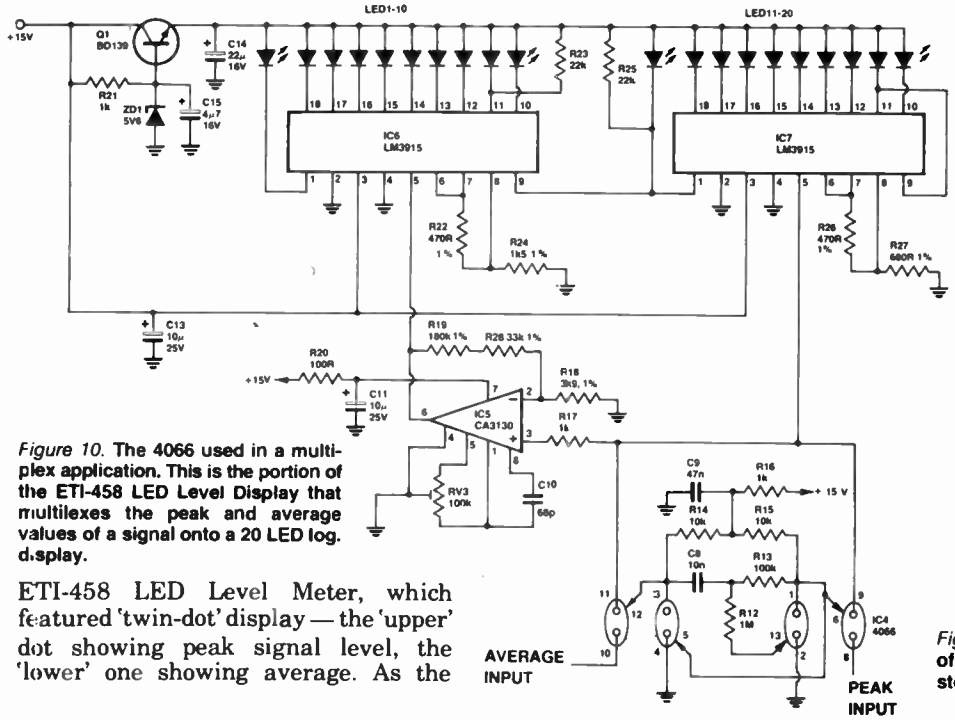
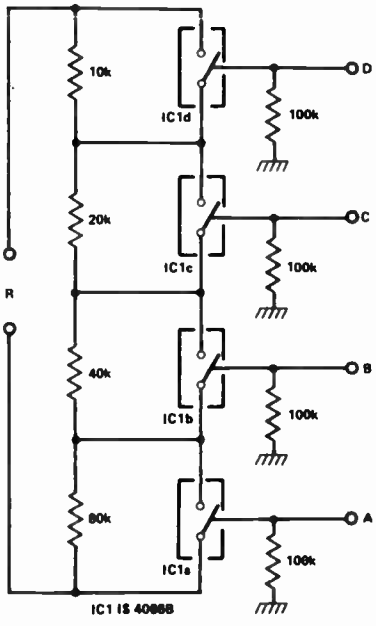


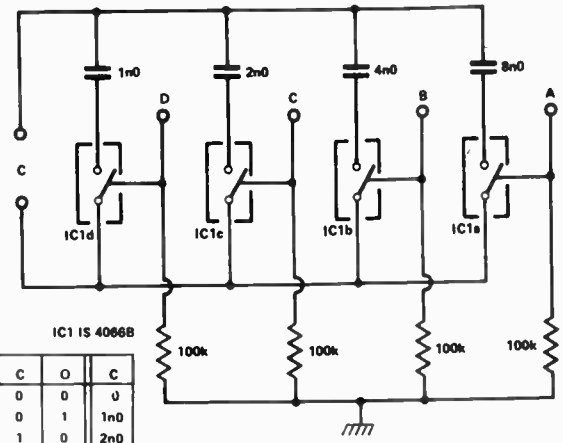

*Figure 10.* **The 4066 used in a multiplex application. This is the portion of the ETI-458 LED Level Display that multiplexes the peak and average values of a signal onto a 20 LED log. display.**




| A | B | C | D | R |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 150k |
| 0 | 0 | 0 | 1 | 140k |
| 0 | 0 | 1 | 0 | 130k |
| 0 | 0 | 1 | 1 | 120k |
| 0 | 1 | 0 | 0 | 110k |
| 0 | 1 | 0 | 1 | 100k |
| 0 | 1 | 1 | 0 | 90k |
| 0 | 1 | 1 | 1 | 80k |
| 1 | 0 | 0 | 0 | 70k |
| 1 | 0 | 0 | 1 | 60k |
| 1 | 0 | 1 | 0 | 50k |
| 1 | 0 | 1 | 1 | 40k |
| 1 | 1 | 0 | 0 | 30k |
| 1 | 1 | 0 | 1 | 20k |
| 1 | 1 | 1 | 0 | 10k |
| 1 | 1 | 1 | 1 | 0 |

*Figure 11.* **This circuit gives 16-step digital control of resistance. R can be varied from zero to 150k in steps of 10k.**

# Lab Notes




| A | B | C | O | C |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1n0 |
| 0 | 0 | 1 | 0 | 2n0 |
| 0 | 0 | 1 | 1 | 3n0 |
| 0 | 1 | 0 | 0 | 4n0 |
| 0 | 1 | 0 | 1 | 5n0 |
| 0 | 1 | 1 | 0 | 6n0 |
| 0 | 1 | 1 | 1 | 7n0 |
| 1 | 0 | 0 | 0 | 8n0 |
| 1 | 0 | 0 | 1 | 9n0 |
| 1 | 0 | 1 | 0 | 10n |
| 1 | 0 | 1 | 1 | 11n |
| 1 | 1 | 0 | 0 | 12n |
| 1 | 1 | 0 | 1 | 13n |
| 1 | 1 | 1 | 0 | 14n |
| 1 | 1 | 1 | 1 | 15n |

*Figure 12.* **A similar circuit to that of Figure 11 gives 16-step digital control of capacitance. C can be varied from zero to 15n in steps of 1n.**

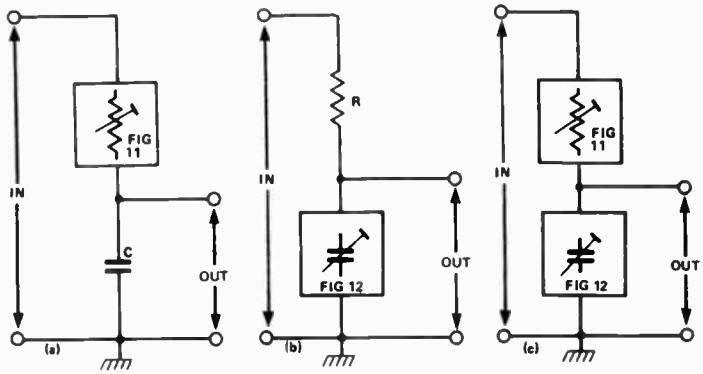



*Figure 13.* **Three ways of using the circuits of Figure 11 and Figure 12 to make a digitally-controlled first-order low pass filter.**

Figure 12 shows how four switches can be used to make a digitally controlled capacitor that can be varied in sixteen steps of 1n each. (Input capacitance is only around 8-10 pF).

Note that in the Figures 11 and 12 circuits the resistor/capacitor values can be controlled by operating the 4066B switches manually, or automatically using simple logic networks, microprocessors, up/down counters, and so on.

The circuits of Figures 11 and 12 can be combined in a variety of ways to make digitally controlled impedance and filter networks. Figure 13, for example, shows three different ways of using the circuits to make a digitally controlled first-order lowpass filter.

Digital control of amplifier gain can be obtained by hooking the 'resistance' circuit of Figure 11 into the feedback or input path of a standard op-amp inverting circuit, as shown in Figures 14 and 15. The gain of such a circuit is equal to $R_F/R_{IN}$, where $R_F$ is the feedback resistance and $R_{IN}$ is the input resistance. Thus, in the Figure 14 circuit, where the controlled resistance is in the feedback loop, the gain can be varied from zero to unity in 16 discrete steps of 'one fifteenth' each, i.e: giving a sequence of 0, 1/15, 2/15, 3/15, . . . , 14/15, 15/15.

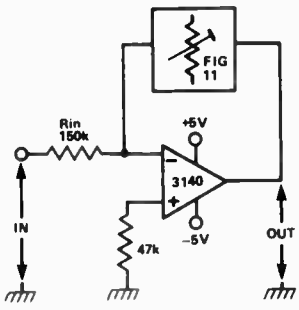



*Figure 14.* **Digital control of gain using the Figure 11 circuit. The gain can be varied between zero and unity in 16 steps.**

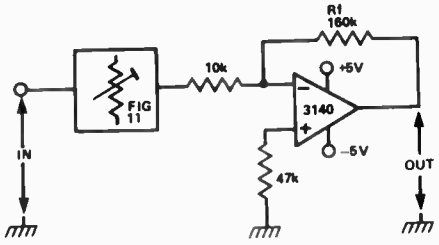



*Figure 15.* **This application of the Figure 11 circuit gives digital control of gain between unity and x16 in 16 steps.**

In the Figure 15 circuit, where the controlled resistance is in the input path, the gain can be varied from unity to x16 in 16 steps, giving a gain sequence of 1, 2, 3, 4, 5, 6, . . . Note that in both of these circuits, the op-amp uses a split power supply so the 4066B control voltage must switch between the negative and positive supply rails.

Figure 16 shows how the Figure 11 circuit can be used to digitally control the frequency of an oscillator in 16 discrete steps. In this example the circuit is that of a 555 astable, but the general control principle can be applied equally well to many other types of oscillator circuit.

Figure 17 shows how a trio of 4066B switches can be used to implement digital control of the decade range selection of 555 astable. Here, only one of the switches must be turned on at any time. Naturally, the circuits of Figures 16 and 17 can be combined to form a wide-range oscillator that can be digitally controlled by a computer, for example.

## Synthesised multi-gang pots

The synthesising principle is quite simple and is illustrated in Figure 18, which shows the circuit of a synthesised four-gang 10k-100k rheostat for use at signal frequencies up to about 15 kHz.

Here, the 555 is used to generate a 50 kHz (nominal) rectangular waveform whose mark/space ratio can be varied from 11:1 to 1:11 by RV1, and this waveform is used to control the switching of the 4066B stages. All the 4066B switches are fed with the same control waveform, and each switch is wired in series with a range resistor (RA, RB, etc), to form one gang of the 'rheostat' between the pairs of terminals, as shown.

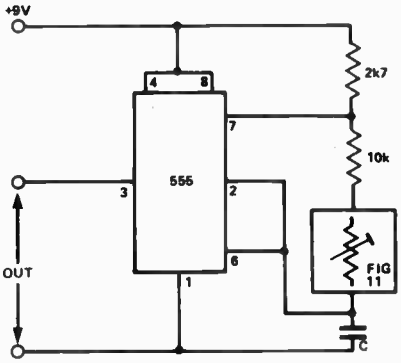



*Figure 16.* **Digital control of the frequency of a 555 astable. The frequency can be varied in 16 steps.**

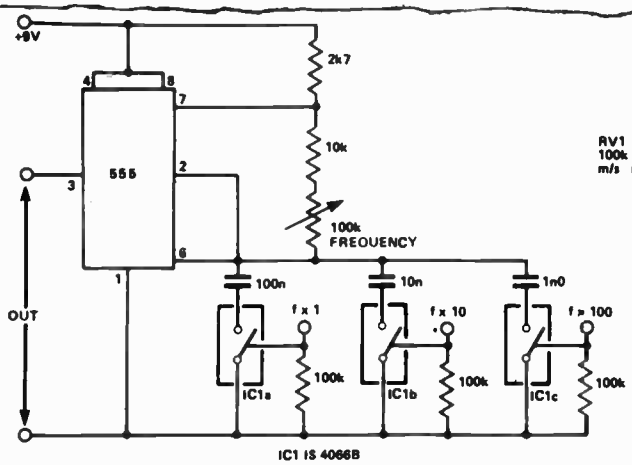



*Figure 17.* **Digital control of decade range switching of a 555 astable.**

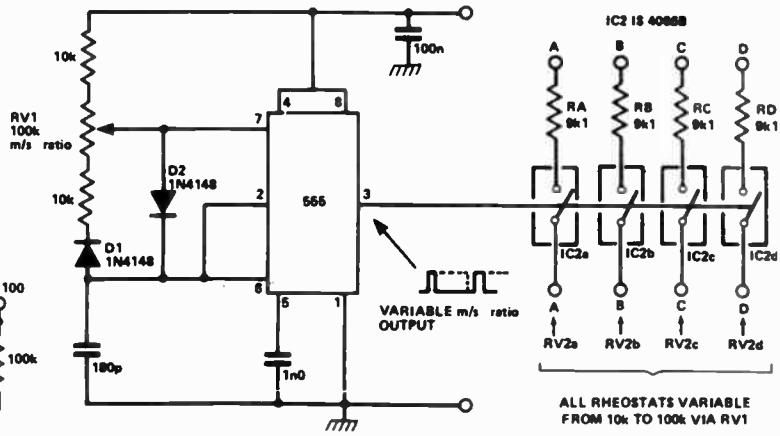



*Figure 18.* **Synthesised precision four-gang rheostat.**

Remembering that the switching rate of this circuit is very fast (50 kHz) relative to the rheostat's maximum signal frequency (15 kHz), it can be seen that the mean or effective value of the 'rheostat' resistance can be varied with mark/space ratio control RV1. Thus, if IC2a is closed for 90% and open for 10% of each duty cycle (mark/space ratio of 9:1), the apparent (mean) value of the resistance will be 10% greater than RA, i.e: 10k. If the duty cycle is reduced to 50%, the apparent RA value will double, to 18k2. If the duty cycle is further decreased, so that IC2a is closed for only 10% of each duty cycle (mark/space ratio 1:9), the apparent value of RA will increase by a decade, to 91k. Thus, the apparent resistance of each 'gang' of the 'rheostat' can be varied by RV1.

There are some important points to note about the Figure 18 circuit. First, the circuit can be given any desired number of 'gangs' by simply adding an appropriate number of switch stages and range resistors. Since all switches are controlled by the same mark/space ratio waveform, perfect tracking is automatically assured. Individual gangs can be given different ranges, without affecting the tracking, by giving them different range resistor values. The sweep range and the law of the rheostat can be changed by changing the characteristics of the mark/space ratio generator. ●

# Lab Notes

# The tender touch

If you ever get involved in the design of electronic equipment, there is a fair chance that you will eventually come across a circuit that requires the use of a 'press-to-do-something' switch. You'll then have to decide whether to use an electromechanical pushbutton switch or a solid-state 'touch' switch to do the job.

Ray Marston

THE MAIN disadvantages of the pushbutton switch are that it is unreliable, tends to be a bit expensive and is available only in those designs that manufacturers care to produce. These switches are also 'noisy' in that they generate contact-bounce spikes that can play havoc with fast digital circuitry.

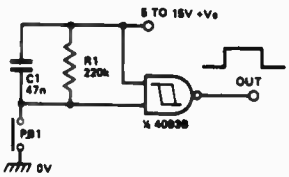



*Figure 1.* **Push-button debouncer circuit.**

This last-mentioned problem can be overcome by using the 'debouncer' circuit of Figure 1. Here, one quarter of a 4093B CMOS quad 2-input NAND Schmitt is used as a simple Schmitt trigger. When PB1 is closed, C1 charges rapidly to full supply volts and the Schmitt output switches high; when PB1 is released C1 discharges slowly via R1 until eventually the Schmitt output switches low again. The circuit is thus unaffected by switch contact bounce and produces a clean on/off signal at the Schmitt output.

Figure 2 shows a useful way of obtaining a toggle (alternate on-off) action from a simple pushbutton switch. The switch signal is debounced by R1-C1 and is then used to clock one half of the 4027B dual JK flip-flop, which divides the clock signal by two. Thus, the 4027B output goes high on one press, low on the next, high on the next and so on. One of these toggle switches can be built from each 4027B IC in the dual package.

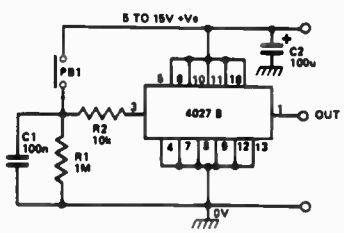



*Figure 2.* **Push-button toggle switch.**

## Touch switch circuits

The main advantages of solid-state switches are that they are reliable (they have no troublesome mechanical parts), can be less expensive than their electromechanical counterparts and can readily be produced in almost any shape or form that the designer or home constructor wishes.

Touch switch circuits come in three basic types (ignoring 'freak' circuits such as thermo-switches, etc). The crudest and least attractive of these are the 'resistive' types, which use the 'touched' or 'untouched' resistance change that occurs between two adjacent touch contacts to give activation.

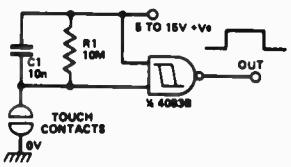



*Figure 3.* **Resistive touch switch.**

Figure 3 shows a typical resistive touch switch circuit. Normally, with the contacts untouched, R1 holds the Schmitt input high and its output is low. When a finger is used to bridge the two contacts the resulting skin resistance (less than 3M) pulls the Schmitt input low and drives its output high. C1 is used to 'debounce' the circuit. Figure 4 shows how the circuit can be modified to give 'toggle' action.

A very serious disadvantage of the resistive touch switch is that it can be disabled by moisture or contamination

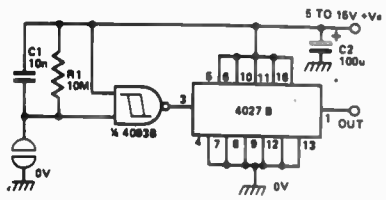



*Figure 4.* **Resistive touch toggle switch.**

bridging the contacts. Also, it may be disabled by persons with damp fingers or may be immune to operations by persons with very dry skins.

A great improvement in reliability is given by a second type of 'hum-detecting' touch switch. This type of circuit relies for its operation the fact that the human body acts as a kind of antenna that is coupled to the mains and carries a high-impedance mains signal. Figure 5 shows an example of this type of circuit. When the input contact is touched the hum pick-up signal is fed to the input of the first Schmitt stage via limiting resistor R2 and produces a full-amplitude square wave at the Schmitt output. This square wave is converted to dc and debounced by the D1-R3-R4-C1 network, and drives the final output of the second Schmitt high. The Schmitt output goes low again some 60 mS after the input touch is removed. Figure 6 shows how the above circuit can be modified to give toggle operation; D2 and C2 prevent unwanted feedback from the 4027B to the Schmitt.

## Capacitive touch proximity switches

The third and most important class of switch is those that work on the capacitive loading principle. In most simple cases, these circuits rely on the fact that the human body acts as a small

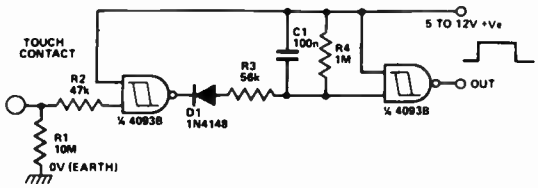



*Figure 5.* **Hum-detecting touch switch.**

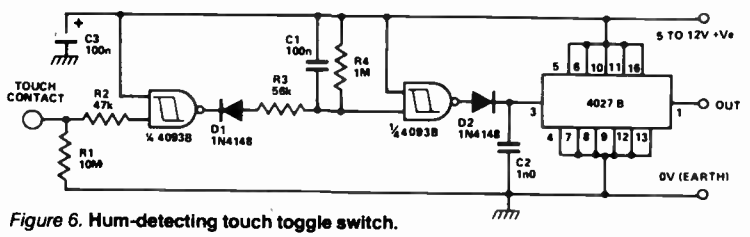



*Figure 6.* **Hum-detecting touch toggle switch.**

capacitor that is earthed at one end. The actual value of capacitance depends on physique and on environmental conditions, but is reckoned to have a value of 150-300p under normal domestic/industrial conditions.

Figure 7 shows a number of basic ways of using the body capacitance effect. In Figure 7a it causes loading of an HF oscillator, in Figure 7b it causes capacitive potential division and in Figure 7c it causes filtering of oscillator harmonics. Of particular interest is Figure 7d, which shows that these effects can be obtained without physical contact, by capacitive or 'proximity' coupling.

Figure 8 shows the practical circuit of a touch/proximity switch that works on the oscillator damping principle. The oscillator is a Colpitts, working at about 300 kHz. RV1 is carefully adjusted so that oscillation is barely sustained when the contact is untouched. Under this condition the rectified output of the oscillator drives Q3 to saturation and holds the circuit's output low. When the contact is touched the resulting capacitive loading kills the oscillator, causing Q3 to turn off and switch the output high. The output has relatively slow rise and fall times, but can be speeded up with a Schmitt circuit if required.

The zero volts line of the Figure 8 circuit should (ideally) be grounded. The touch contact must be made from a conductive material, but can be any shape or size that is desired; in most cases the 'contact' face can be covered with an insulating material without detracting from the circuit's performance. Pin-head sized contacts will require actual-contact operation, but 'contacts' with surface area of a square metre or so can be proximity-operated at ranges up to 20-40 centimetres.

Finally, Figure 9 shows the circuit of a touch switch that works on the capacitive-divider principle. Here, IC1 is wired as a ring-of-three oscillator working at a frequency of a few hundred kHz. The oscillator output is fed to a capacitive potential divider formed by C2 and the stray capacitance around D1 and the touch contact. The resulting potential divider output signal is rectified by D1-D2-C3-R2 and fed to the 3140 regenerative voltage comparator, which is adjusted (via RV1) so that its output is just switched to the low state when the input contact is untouched. When the contact is touched, the resulting capacitive loading increases the effective capacitance of the lower half of the potential divider, thereby reducing the divider's output voltage and causing the 3140 output to switch high. Figure 9b shows an add-on section that can be used to convert the circuit to toggle operation.

As in the case of the Figure 8 circuit, the zero volt line of Figure 9 should be grounded. The touch contacts can again be any desired shape or size. ●

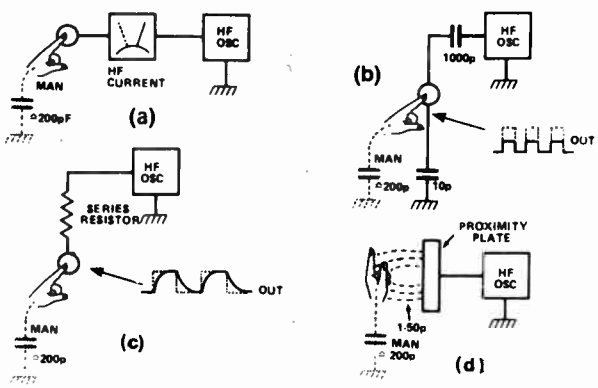



*Figure 7.* **Body capacitance effects on a touch contact. (a) Causes oscillator loading, (b) capacitive potential divider action or (c) degradation of oscillator waveform (harmonic filtering). (d) If contact is of sufficient area, loading and other effects can be obtained without physical contact, by capacitive or proximity coupling.**

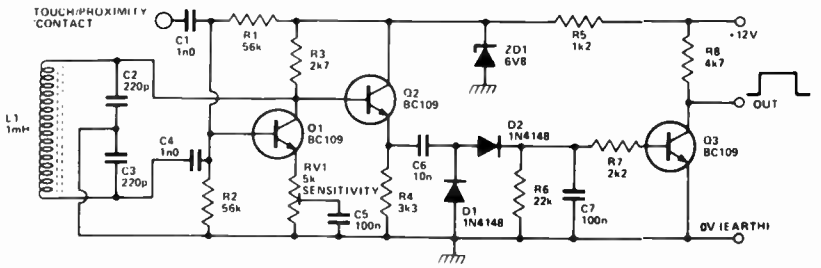



*Figure 8.* **Damped oscillator touch/proximity switch.**

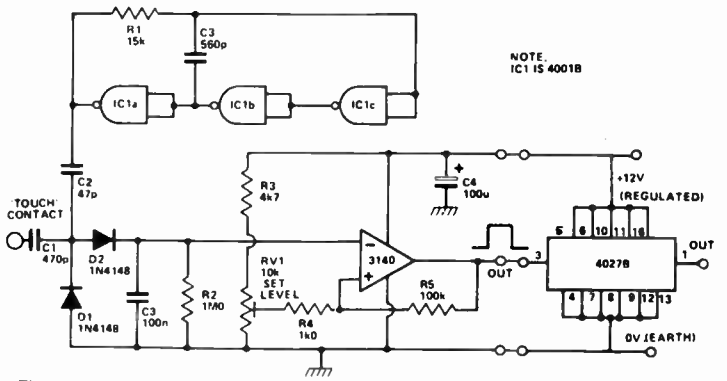
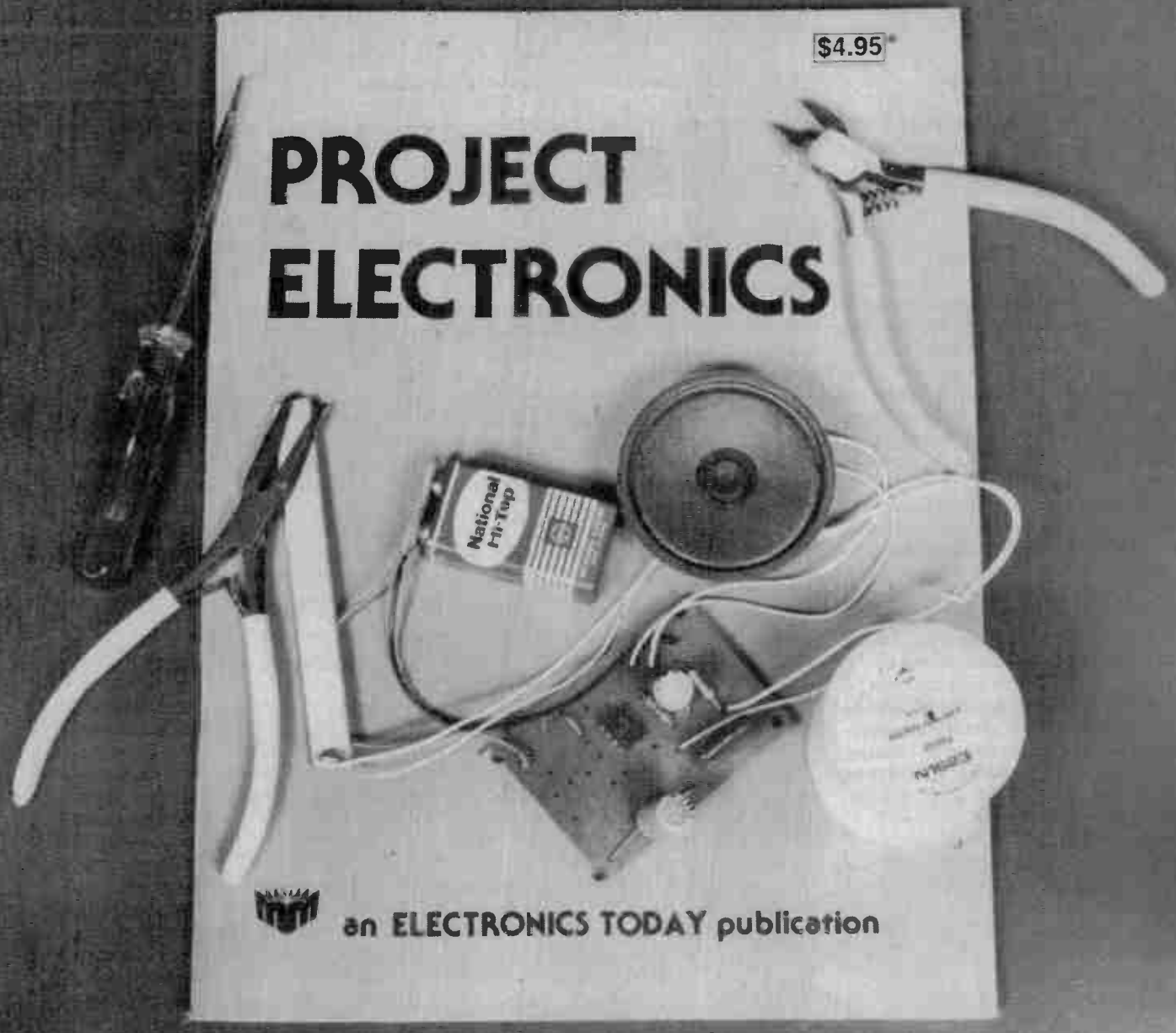
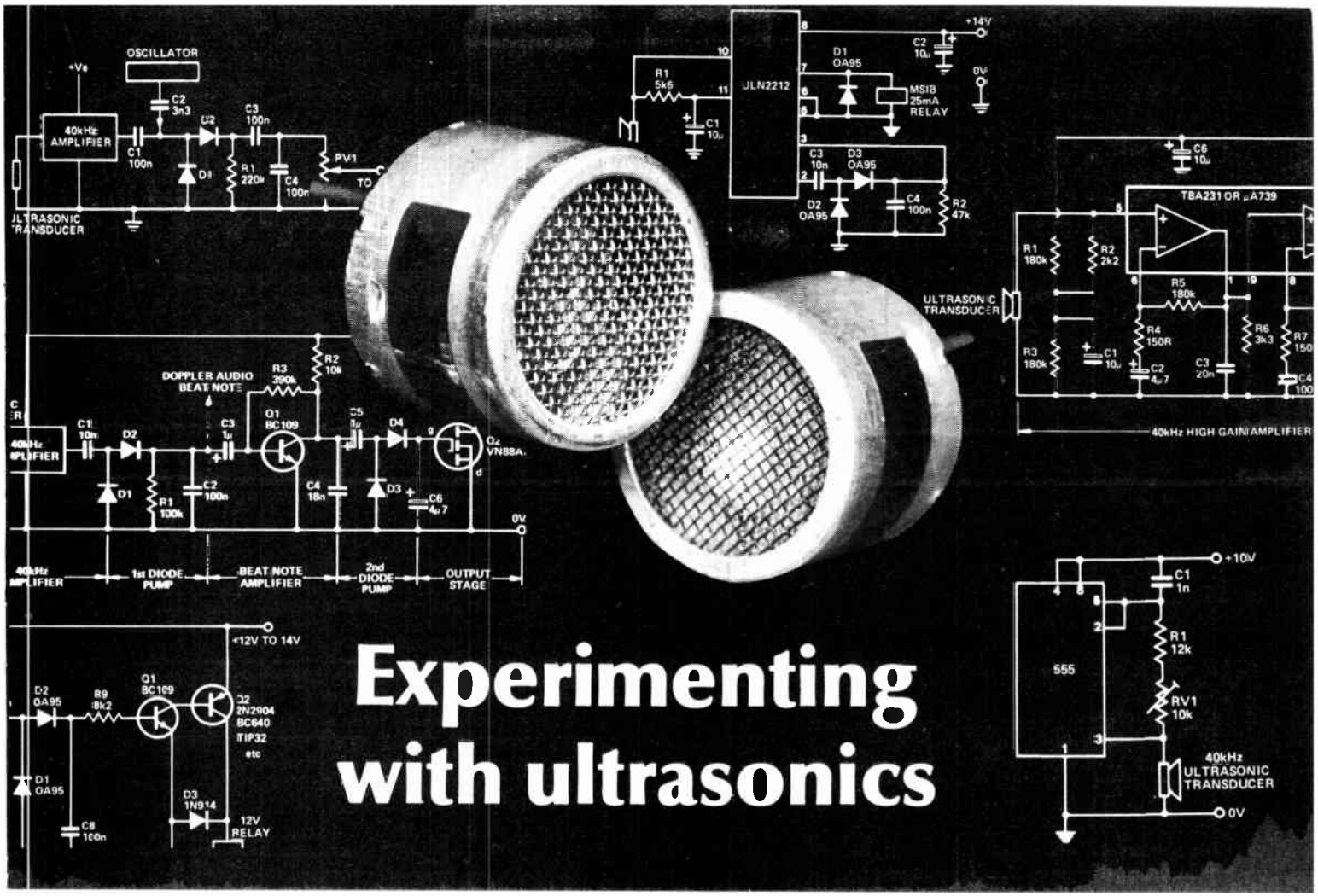



*Figure 9.* **Capacitive-divider touch switch (left) with modification for toggle operation (right).**

# Just starting out?




THIS BOOK has been specially designed and produced to meet the needs of newcomers to electronics. Students following the three-segment Industrial Arts syllabus at high school or embarking on the Electronics & Communications new 4 unit TAFE course will find the projects in this book an eminently practical introduction to the works of electronics. Project Electronics has been a runaway success since it was first published. There are 25 projects included, many are readily available as inexpensive kits, and the book also provides advice on tools, identifying components, troubleshooting, how to solder etc. Available from specialist electronics suppliers or direct from ETI Book Sales, Federal Publishing, 140 Joynton Ave, Waterloo, NSW 2017. Only $4.95 plus $1 postage and handling.




## Brian Dance

Inexpensive ultrasonic transducers can be used in a fascinating variety of gadgets and circuits, from garage door openers to 'bat detectors'.

MINIATURE ultrasonic transducers can be used to generate high frequency waves in air which cannot be heard yet which have a wide range of applications in remote control, short-distance communications and in the detection of intruders. This article reviews the type of circuits in which these transducers are normally employed and will provide the experimenter with plenty of ideas to try; practical circuits are given, without constructional details.

Two main types of ultrasonic unit will be discussed. **Transmitter units** are oscillators in which high frequency oscillations are fed to a transducer which produces ultrasonic air waves in much the same way as a loudspeaker produces audible air waves. If the waves from a transmitting transducer are allowed to fall onto a transducer in a receiver unit, very small signal voltages are developed by the receiver transducer and these signals may be suitably amplified to operate a relay or an alarm. The relay can be used to switch any other equipment, but some receiver units include complex logic circuits.

The main limitation in the use of ultrasonic air waves is the limited range over which they can operate — usually not much more than 30 metres. Although microwave beams can be used over much greater distances, ultrasonic systems are far simpler and cheaper. In addition, the waves are not radiated far outside the room or region concerned.

### Frequencies

The frequencies used are usually in the range 20 kHz to 60 kHz. The average adult can hear frequencies of up to about 15 kHz, but some young people can hear considerably higher frequencies, so this sets a lower limit of 20 kHz to 25 kHz. The uppermost frequency is set by the rapid increase in air absorption of the waves which occurs at frequencies above about 50 kHz and which limits the maximum range at which detection can occur. (Much higher frequencies — about 1 MHz to 10 MHz — are used in ultrasonic applications in medicine, whilst GHz ultrasonic frequencies can be used in acoustic microscopy, but no air transmission is then involved.)

Ultrasonic transducers can operate efficiently only near the resonant frequency of the ceramic piezo-electric element they contain. Most of the transducers on the market resonate at either 40 kHz or 25 kHz; the performance at these two frequencies is not so very different, but the 40 kHz

types are more directional.

An ordinary sound wave around 300 Hz has a wavelength of the order of one metre, so it is diffracted at the edges of common objects whose size is not much larger than the wavelengths concerned. Thus, ordinary sound bends around the edges of objects. However, the wavelength of 40 kHz waves in air is only about 8 mm; this is much smaller than most common objects found in a room so the waves are effectively stopped by objects of dimensions greater than a few centimetres. In practice this means that the ultrasonic transducers are strongly directional, the output from an ultrasonic transmitting transducer being about 10 dB down at $30^0$ from the direction in which the transducer faces. Similarly, the receiver sensitivity falls by a similar amount when the incoming waves are off the transducer axis.

In the open air, the ultrasonic transducers must be pointed approximately towards one another or little response will be obtained. In a room of a normal size, however, ultrasonic waves are reflected from walls and objects so that a single transmitter in a room will cause the whole room to be filled with ultrasonic waves.

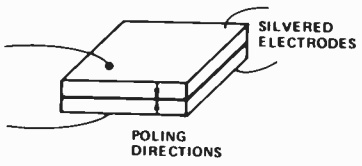
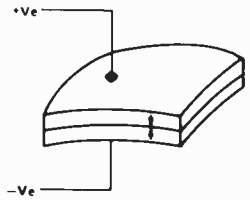



*Figure 1.* A piezo-electric ceramic element consists of two plates of opposite poling directions cemented together. When a voltage




is applied between the faces the plates bend and can transfer ultrasonic energy to the surrounding air.

## The transducers

An ultrasonic transducer consists of a square of piezo-electric ceramic material with metallized electrode surfaces deposited on its faces. The ceramic material is actually a bimorph element, which means that it consists of two separate layers fastened together, these layers having their electric dipoles aligned in opposite directions as illustrated in Figure 1.

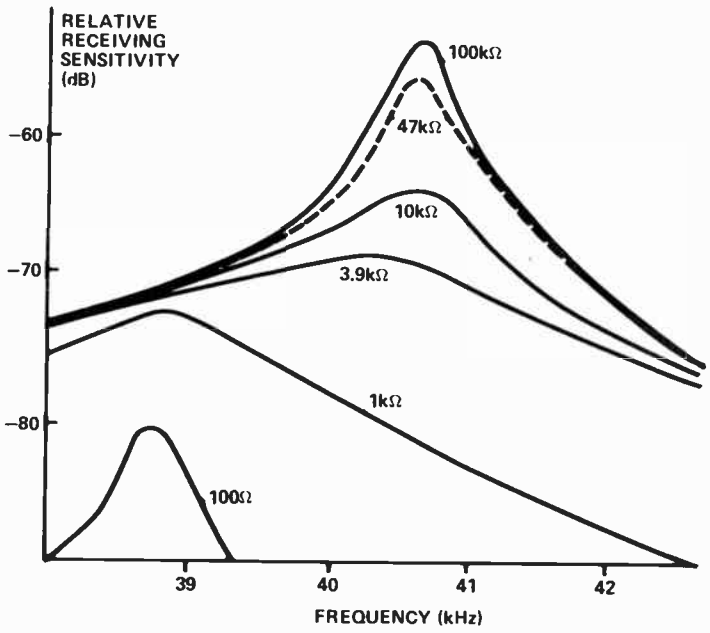



*Figure 2.* A set of curves showing how the frequency response of a sharply-peaked 40 kHz receiver transducer is affected by various values of load resistor.

The ceramic bimorph element is suitably mounted so that its vibrations are not damped by the mounting and is fixed inside a small case, which is usually cylindrical, measuring about 10-25 mm in diameter and about the same length. The front has an open mesh so that the ultrasonic waves can pass easily into or out from the ceramic element. If the transducer case is made of metal, the case should preferably be at ground potential.

The ceramic elements couple to the surrounding air with a reasonable degree of efficiency. The ultrasonic power output from a typical transducer can be of the order of 10% of the electrical power fed to that transducer.

Some suppliers offer types of ultrasonic transducer which are designed to be used as either transmitting or receiving transducers. Other types available have some differences between the transmitting and receiving transducers. Although the functions of these components may be interchanged, there will be some sacrifice in performance or in their safe ratings in many cases.

The writer performed some measurements on the frequency response of one type of transducer specifically designed for use in receiver units and obtained graphs similar to those of Figure 2, published by the manufacturer for various load resistors connected across the transducer terminals. It can be seen that if a load resistor of 10k is connected across the transducer terminals instead of 100k, a loss of about 10 to 12 dB in sensitivity results, but the bandwidth is considerably increased. At lower values of load resistor, the resonant frequency is reduced somewhat, but normally the effective load should not be less than a few kilohms.

When transducers specifically designed for use in transmitter units were used as receiving units, it was found that they behaved in the unloaded state rather like the receiver transducers would behave when loaded with about 4k7 to 10k. Thus, the transmitter devices have much flatter response curves. Transducers supplied for use as either transmitters or receivers were also found to have fairly flat response curves. One may guess then, that a receiver unit with a sharply peaked response may be ideal for the detection of weak ultrasonic signals in the presence of noise, but transmitter units are more broadly tuned so as to ensure that they can cover the receiver frequency peak.

## Transmitter circuits

One of the simplest ways of constructing an ultrasonic transmitter is to connect the transducer across the terminals of a signal generator set to the resonant frequency of the transducer. Either a sine wave or a square wave may be used, but care should be taken to ensure that the maximum permissible rating of the transducer is not exceeded. It is possible to use ultrasonic transducers under pulsed conditions, but care is needed to obtain good results.

It is possible to design oscillators for driving ultrasonic transducers using only a single transistor, but a feedback transformer is necessary and it is usually easier to design a two transistor astable circuit which requires no transformer. An astable circuit of this type, designed by Philips-Mullard for

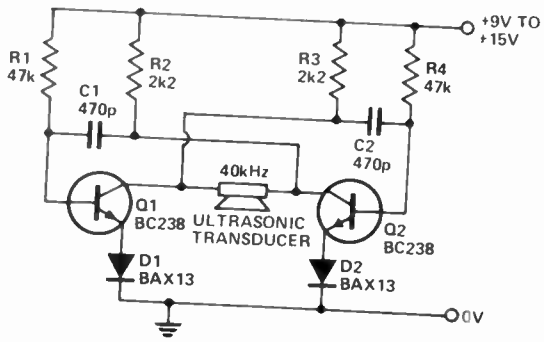



*Figure 3.* **An ultrasonic transmitter using discrete components. Synchronisation with the 40 kHz transducer is automatic. For 25 kHz operation, C1 and C2 should be increased to about 750 pF (560 pF and 180 pF in parallel). Most silicon NPN transistors can be used for Q1 and Q2; e.g: BC108, BC548 etc.**

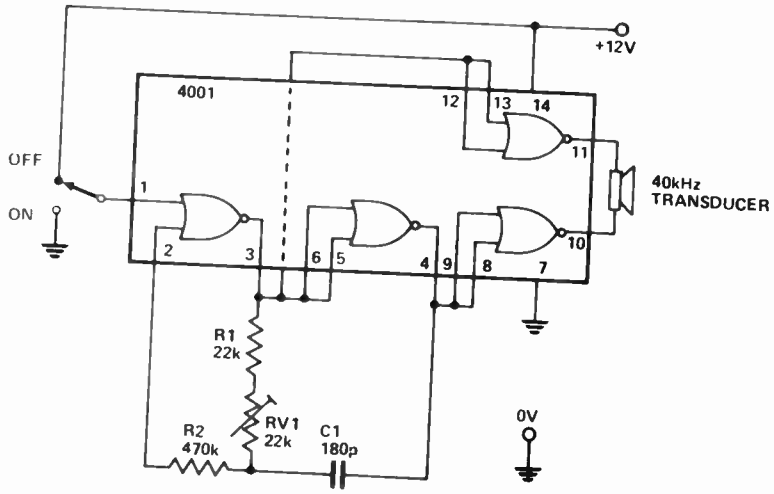



*Figure 5.* **A CMOS 4001 push-pull transmitter circuit. For 25 kHz operation, C1 should be increased to about 270 pF. A CMOS 4011 NAND gate can be used instead of the 4001 device but the ON and OFF connections to the switch are then reversed.**

their 36 kHz transducers, is shown in Figure 3. The diodes in the emitter circuits of the transistors suppress the reverse voltage peaks occurring between the base and the emitter; these peaks are likely to exceed the maximum permissible reverse value of 5 V for the transistor types shown and at the same time can give rise to frequency fluctuations. The diodes are not needed at low supply voltages, but the ultrasonic output is then lower.

The natural frequency of oscillation of the circuit in Figure 3 is determined by the time constants R1-C1 and R4-C2, but this natural frequency is made lower than the required frequency. When the ceramic piezo-electric element of the transducer is connected across the two collectors, the oscillations of the circuit make the transducer ring. The ringing transducer generates a voltage which causes premature triggering of a cut-off transistor so that the oscillator is synchronised to the transducer frequency. Thus, no trimming of the oscillator frequency is necessary in this particular circuit. Current consumption is about 5 mA with a 9 Vdc supply.

Circuits can usually be simplified by the use of integrated circuits instead of discrete components. Figure 4 shows how a 555 device can be used to drive an ultrasonic transducer at about 40 kHz. The preset resistor, RV1, should be adjusted for maximum current consumption which occurs when the 555 oscillator frequency matches the transducer frequency and maximum power is radiated. The 555 produces square waves with a mark-to-space ratio of about 1:1. If 25 kHz transducers are to be used, C1 should be increased to 1n5, alternatively R1 can be increased to about 18k.

Another simple ultrasonic transducer circuit is shown in Figure 5; it uses the 4001 quad two-input CMOS NOR gate. Two gates act as a square wave oscillator which drives the other two NOR gates in push-pull. The latter act as buffers and drive the transducer in push-pull, preventing any voltages from the transducer from affecting the oscillator itself. The oscillator frequency can be adjusted by means of the preset component VR1 so that maximum current is taken from the supply line. Capacitor C1 should be increased to 270p for 25 kHz operation.

The performance of each of the oscillators shown in Figures 3 to 5 inclusive is very similar.

More complex transmitter units can be made which radiate a modulated waveform or a pulse-coded waveform. For example, a 556 device (dual 555) can be employed to generate a 300 Hz signal to modulate the second 40 kHz oscillator of the 556; the advantage of using modulated ultrasonic waves is that the receiver can be made selective to the 300 Hz modulating frequency and reject noise.

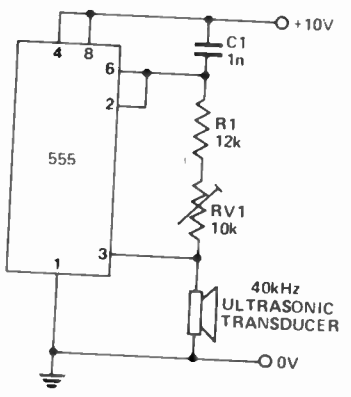



*Figure 4.* **A transmitter circuit employing a 555 timer/oscillator IC. For 25 kHz operation, C1 should be increased to about 1n5.**

## Receiver units

In the same way that the ceramic piezo-electric bimorph element bends when a voltage is applied across it (Figure 1), when ultrasonic waves fall on it, the bending of the element generates a small voltage across the transducer terminals. This voltage is a 40 kHz waveform, but unfortunately the amplitude is quite small. When the transmitting and receiving transducers are placed face-to-face and touching one another the voltage across the receiver transducer terminals is typically less than one volt, but at a distance of about 30 meteres the voltage across the receiving transducer falls to some tens of microvolts and any further increase in the distance between the transmitter and receiver will be likely to result in the signal being lost amongst the noise.

Thus, it is clear that an amplifier of considerable gain must follow the receiving transducer in the receiver unit. This amplifier may consist of discrete transistors, but the circuit can be considerably simplified by the use of one or more integrated circuits. In particular, it is interesting to note that the ICs developed for the amplification of 10.7MHz IF signals in FM receivers, or for amplification of the inter-carrier sound signal in television receivers, are very suitable for the amplification of ultrasonic signals from a receiving transducer.

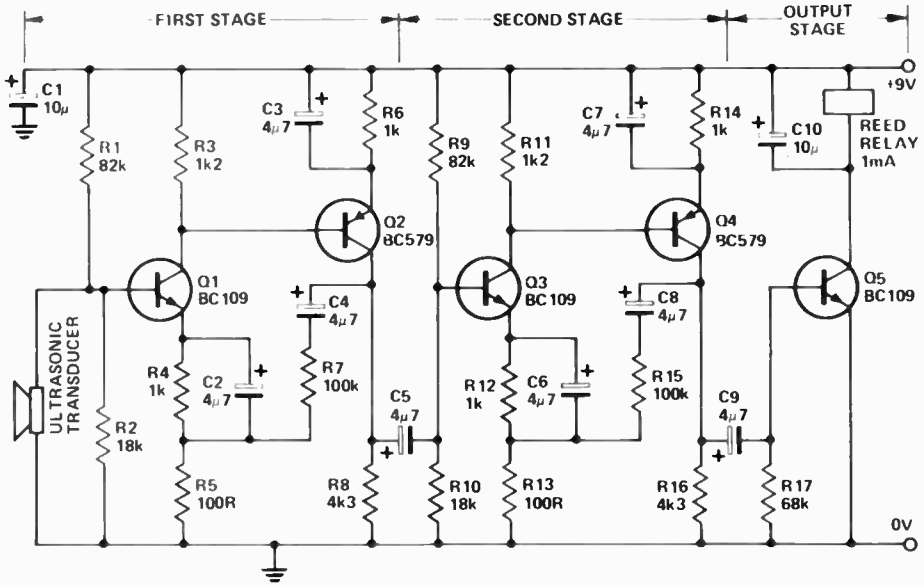



*Figure 6.* **An ultrasonic receiver circuit using discrete components. The reed relay closes when ultrasonic waves fall onto the input transducer.**

## Discrete components

A five-transistor discrete component receiver is shown in Figure 6. Each of the transistors employed is a high-gain, low-noise, small-signal type of the appropriate polarity. Q1 and Q2 provide the first stage amplification and this is followed by an identical second stage, Q3 and Q4, while Q5 controls a sensitive reed relay. When ultrasonic waves of the correct frequency (25 kHz or 40 kHz) fall on the transducer, the relay will operate.

The transducer can be connected directly to the base of Q1, since it has a very high dc impedance and will not affect the bias applied to Q1. The gain of the first stage is determined mainly by R7 and R5 and that of the second stage by R15 and R13. Either R7 or R15, or both, should be reduced if the circuit becomes unstable due to a poor layout or if a high sensitivity is not required.

When the distance between the transmitting and receiving transducers is quite small, it is possible to use only a single stage of amplification before the output stage.

When the 40 kHz voltage peaks across R17 exceed about 0.65 V, Q5 commences to conduct and only a little increase in the ultrasonic wave intensity will then cause the reed relay to close. Capacitor C10 smooths out the 40 kHz half-cycles of current passing through the reed relay.

It is important to note that a very sensitive reed relay must be employed in this circuit which closes with a current of no more than about 5 mA with a coil voltage of about 6 V. During the setting up of the circuit and when experimenting with it, it is instructive to insert a 10 mA meter in series with the reed relay coil. Although the reed relay can switch only a small current (perhaps 100 mA), this current can be used to perform any desired operation, including the control of a much larger relay.

## TAB231 Receiver

Another receiver circuit for the control of a relay is shown in Figure 7. A TAB231 (SGS-ATES) or the equivalent, uA739 (Fairchild) or a similar device, is employed as a 40 kHz two-stage amplifier. Resistors R1 and R3 provide a bias for the non-inverting (+) input of the left-hand amplifier to which signals from the transducer are also fed. Capacitor C1 effectively ties the junction of R1, R2 and R3 to common (0V) as far as alternating voltages are concerned, so the resistor R2 appears as a load across the transducer terminals and broadens the frequency response of the transducer (see Figure 2).

The gain of the first 40 kHz amplifier stage is set by the ratio of R5/R4, but the other components in the feedback network reduce the gain at low frequencies. The output from pin 1 is fed directly into the non-inverting input of the second amplifier stage and also provides a suitable bias for this input. The second stage is of a very similar design to the first stage except that some component values are modified to reduce unwanted noise and low-frequency gain which can cause problems.

The output from pin 13 is fed through C7 to a diode pump circuit. The latter converts the 40 kHz waveform into a steady voltage which appears across the diode pump output capacitor C8 which has its upper end positive when the ultrasonic waves are present on the receiving transducer. Each 40 kHz input wave passing through C7 causes a small amount of charge to flow through D2 to the capacitor C8 which thus becomes charged.

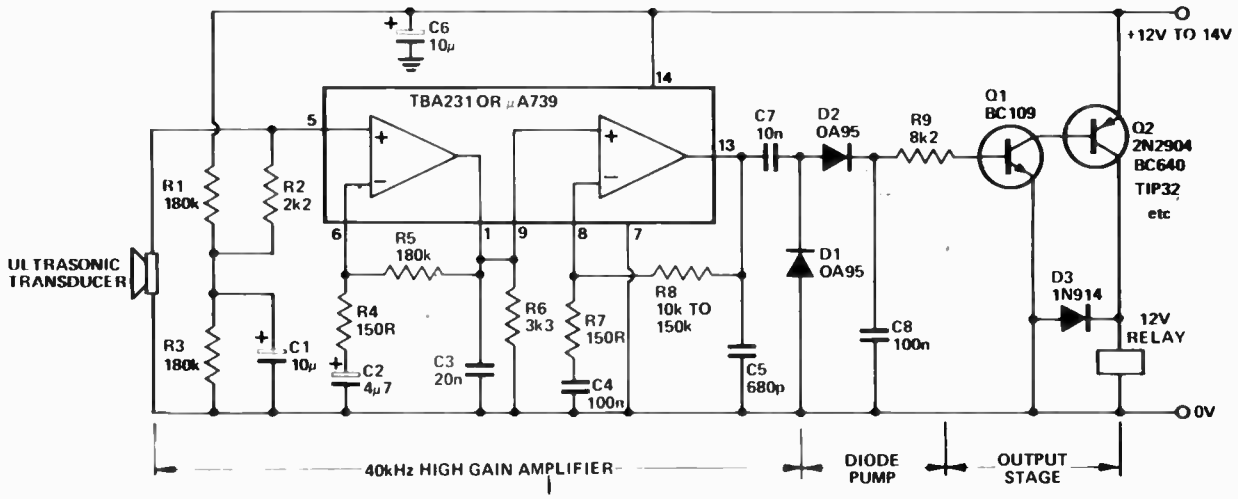



*Figure 7.* **Receiver circuit using the TBA231 or uA739 as a high gain amplifier.**

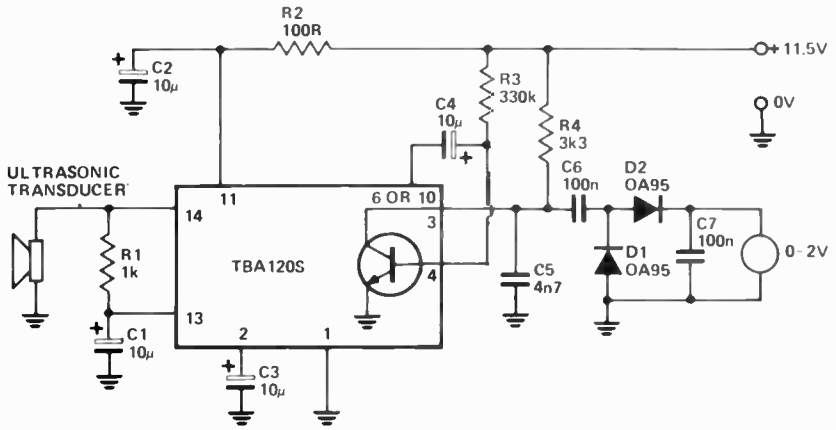



*Figure 8.* **A receiver employing the TBA120S as an amplifier and featuring a meter display.**

Charge from C8 passes through R9 and through the base-emitter junction of the transistor Q1; a collector current therefore flows in Q2, the output transistor, as well. The relay is therefore energised and its contacts close whenever ultrasonic waves fall onto the receiving transducer. The 2N2904 output transistor can switch a moderately large current, so a relay which requires a current of 150 mA or more can be employed. Such a relay can switch a substantial current through its contacts — perhaps 10 A in a 250 Vac circuit, so power levels of well over 1 kW can be controlled by this circuit directly.

The resistor R8 in Figure 7 may be adjusted to obtain the required gain. If the sensitivity is too high, spurious signals may cause the relay to close. In particular, the ringing of a telephone bell, even at a distance of some eight metres can cause the closing of the relay. The sensitivity can be reduced by reducing the value of R8. For some applications it is instructive to insert a meter (perhaps 100 mA FSD) in the 2N2904 emitter or collector circuit.

Transducers resonating at any frequency between about 20 kHz and 60 kHz may be employed in the circuits of Figures 6 and 7 with the component values shown. It is only in the transmitter circuits that component values must be slightly changed if transducer frequencies are altered so that the required frequency of oscillation is obtained.

## TBA120S circuit

The circuit of Figure 8 shows how a Philips TBA120S device may be used as a 40 kHz amplifier. The TBA120S is intended for use as an IF amplifier and an output may be taken from pin 6 or pin 10 through a 10n coupling capacitor, as shown, to the base of an internal transistor which is used to provide more gain. In the circuit, R4 forms the collector load and the capacitor C5 was found to be needed to prevent spurious oscillation.

The output of the diode pump in Figure 8 is shown connected to a 2V FSD meter, but it could also drive a two-transistor output stage such as that shown in Figure 7. Indeed, the parts of the circuits shown in this article can be regarded as building blocks which the experimenter can connect together in many different ways, although care may be needed to prevent oscillation.

## ULN-2212 circuit

A very simple receiver circuit for relay control can be made using one of the devices intended for use as a combined intermediate frequency and power amplifier (leaving any volume control circuit unused). The writer has used the LM1808, while the circuit of Figure 9 shows the use of a Sprague ULN-2212 device.

The section of the ULN-2212 intended for use as an intermediate frequency amplifier is used to amplify the 40 kHz signal from the ultrasonic transducer, the bias to the input pin 10 being applied through R1 from pin 11.

The output from pin 2 is coupled to the diode pump, D2 and D3, and the resulting positive potential is fed into the input of the power amplifier at pin 3. This power amplifier can pass enough current to control the relay connected in its output circuit (pin 7). As with the circuit in Figure 7, a diode is connected across the relay to shunt the reverse transient voltage produced when the relay coil current ceases to flow, since this voltage could damage the output device.

Although the circuit of Figure 9 is very simple, it is not so flexible or so sensitive as that of Figure 7.

The diodes shown in the diode pump circuits are germanium point-contact types (OA95), since these are switched to conduction by a potential of about 150 mV. Silicon diodes, such as the 1N914, can also be used in the diode pump circuits but they may not respond to weak signals as do the pump circuits using OA95s since they require about 0.65 V for forward conduction.

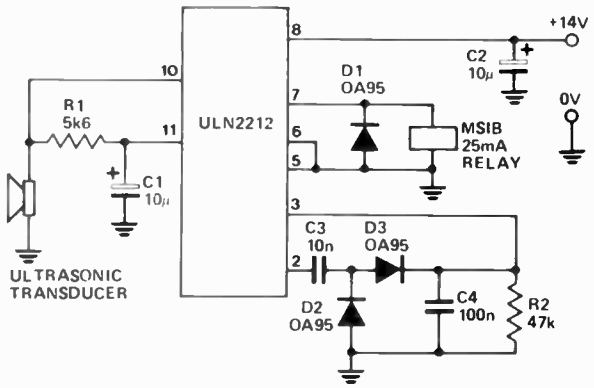



*Figure 9.* **This is one of the simplest possible circuits that will operate a relay from an ultrasonic transducer. The relay should be a sensitive type and may have whatever contact set is appropriate to your application.**

## Applications

The receiver circuits of Figures 6 to 9 inclusive can be employed in simple remote control applications in which one wishes to be able to press a button on a small hand-held transmitter unit in order to cause a relay to close in some equipment up to about 20 metres away. Unlike light beams, ultrasonic communications links are almost unaffected by the presence of rain, fog, snow, smoke or dust. Such a link could, for example, be used to call a person working in a garden shed into the house.

If an ultrasonic transmitter unit is mounted on the front bumper of a car, when the driver reaches his home he can transmit a short pulse of ultrasonic waves to a receiving unit near his garage door which causes his garage

door to be opened automatically by a motor, without the necessity for the driver to leave his vehicle. Similarly, he can close the garage door as he leaves home.

Ultrasonic links have been widely used for the remote control of television receivers, but they have now been largely displaced by infra-red links. The latter tend to be more complex than ultrasonic links, but they do offer the wider bandwidth desirable for the many channels of communication required to control a colour television receiver (which may possibly include a Teletext decoder).

If an ultrasonic transducer is placed in a sealed enclosure, such as the interior of a car or a refrigerator, a receiver unit fitted with a meter in its output stage can be moved around the outside of the enclosure to locate any small leaks in the sealing rubber. The ultrasonic waves can only escape from the interior through any such small leaks and this method of leak detection is generally much more convenient than, for example, waiting until it rains to see where the water enters one's vehicle!

The circuit of Figure 8, or the circuits of Figure 6 or 7 (if fitted with a meter output) are very suitable for this application.

Leaks in pressure or vacuum pipes generate ultrasonic waves which can be used to deflect a meter in a suitable receiver. Thus the leak can be located. Similarly, some types of electrostatic corona discharge produce ultrasonic waves which can be detected in much the same way. Generally however, it is better to convert the ultrasonic frequency into an audible frequency by a heterodyne technique, as discussed later.

A simple transmitter and receiver of the types discussed, operating at a fairly low gain, can be used as an intruder detector. If an intruder passes through the beam, the interruption of the beam operates a relay and this gives the required alarm. Ultrasonic systems have the advantage that the intruder cannot hear the signal. However, the Doppler system to be discussed is normally much more satisfactory than a simple transmitter and receiver, since the Doppler detector is triggered by movement anywhere in a protected room and it is not necessary for the intruder to actually pass through any given point in the beam. Nevertheless, a simple transmitter-receiver is adequate for the protection of a corridor or other narrow area through which an intruder must pass.

Another application for an ultrasonic transmitter-receiver circuit is the remote control of slide projectors. If one wishes to have remote control without connecting wires merely so that one can cause the next slide to be projected, a simple system like those described will suffice. If, however, one wishes to be able to return to an earlier slide and to be able to alter the focusing in either direction, then a four-channel link is needed. Multi-channel systems are most easily constructed using some of the special devices developed for television receiver control.

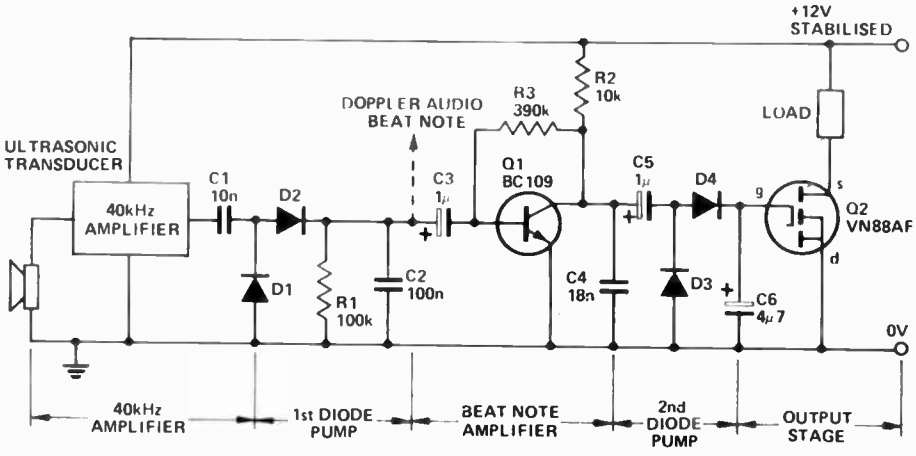



*Figure 10.* **Circuit of a receiver for a Doppler-type intruder detector.**

At one time, the police in certain countries used ultrasonic transmitters to switch on motorway warning lights for fog or ice by merely directing the beam at a receiver near the warning light without stopping their vehicle.

Another application is in vehicle safety belt security systems in which the safety belt emits an ultrasonic tone from a transducer fixed to it; the vehicle cannot be started unless the signal is being received by a transducer mounted near the windscreen. Slightly different frequencies cover the driver and front passenger seats.

## Doppler intruder detector

A Doppler intruder alarm receiver circuit is shown in Figure 10. When used with one of the transmitter circuits discussed previously (which should be operated from the same stabilised power supply), the circuit can detect the slightest movement anywhere within a room of the size found in a normal house. The 40 kHz amplifier shown in block form may consist of the discrete circuit shown in Figure 6, up to and including Q4 (so that C9 of Figure 6 corresponds with C1 of Figure 10). Alternatively, the 40 kHz amplifier may consist of that shown in Figure 7, in which C7 corresponds to C1 of Figure 10.

The ultrasonic transmitter is placed in the same room as the Doppler receiver unit of Figure 10, but the two transducers should not be placed so that they directly face one another. The transmitted frequency is reflected around the room from wall to wall and some of the signal will be picked up by the receiver unit. If anything moves in the room, a Doppler-shifted ultrasonic tone will be reflected from the moving object to the receiver so that the two separate frequencies will be amplified by the 40 kHz input amplifier.

The output from this amplifier is fed to the first diode pump circuit so that the difference frequency or beat note is developed across C2. Objects which are moving fairly rapidly in the room develop a beat note in the audio frequency band which can be heard if the signals across C2 (Figure 10) are fed to an audio amplifier. More slowly moving objects develop sub-audio frequencies but the use of large coupling capacitors in the remainder of the circuit ensures that a response to either audio or sub-audio frequencies is obtained. Ultrasonic frequencies are shunted to common through C2.

The beat frequency is coupled by C3 to a single transistor difference frequency amplifier, Q1. Any residual 40 kHz frequency components are filtered out by C4 and the low difference frequency is passed to the second diode pump circuit. This circuit will develop an appreciable voltage across C6 only when a Doppler shifted signal is present at the input in addition to the transmitted signal. The presence of the Doppler-generated signal across C6 can be used to switch on the VN88AF power MOSFET output stage which allows a current to flow through the load and thus sound the alarm.

The power MOSFET output stage of

Figure 10 has been included as an alternative to the two-transistor circuit of Figure 7. The output stage of Figure 7 can be used as the output of the Figure 10 Doppler receiver, and vice-versa.

The writer has also used a circuit of type shown in Figure 10 with a power Darlington output stage controlling a relay. The relay did not close if a person some four metres from the equipment remained absolutely still, but if he breathed in or out (even relatively slowly), the movement of his chest wall was enough to cause the relay to close without fail!

One of the problems with such extreme sensitivity is that of false alarms, since even the occasional false alarm in the middle of the night can cause a great deal of trouble! One should also remember that this circuit is sensitive to any stray ultrasonic frequencies such as the ringing of a telephone bell or even the rubbing of two surfaces together if they are near the transducers. If the transducer of the Doppler receiver of Figure 10 (or the transducer of any sensitive ultrasonic receiver) is tapped with the finger, a considerable response will always be obtained in either an output relay or output meter. It should be noted that a regulated power supply should be used for the Figure 10 circuit, otherwise stray changes in the power line voltage may give rise to false alarms.

The 40 kHz amplifier can be the same type as that used in Figure 6 or Figure 7, its output being fed to the diode pump of the Figure 11 circuit. In addition, signals from an oscillator operating at a frequency close to the frequency of the incoming signals are fed through C2 to the same diode pump circuit. The oscillator circuit can be that of Figure 4, but the output from pin 3 is connected to C2 of Figure 11 instead of to the ultrasonic transducer shown in Figure 4.

The difference frequency between the incoming signal and the oscillator is developed in the non-linear diode pump circuit of Figure 11. The components C3 and C4 filter out the ultrasonic frequency signals and the difference frequency is passed to an audio amplifier through the volume control RV1. Any audio amplifier with a gain of the order of 50 is suitable (such as many of the integrated circuit audio amplifiers on the market). Either a small loudspeaker or an earpiece may be used to produce the audible noise.

Experimenting with a 'bat detector' circuit is of great educational value and makes one appreciate what a vast world of ultrasonic tones we are missing! If one rubs the palms of one's hands together or rubs any two suitable surfaces in front of the face of the receiving transducer, one can hear the rubbing noise, since such rubbing

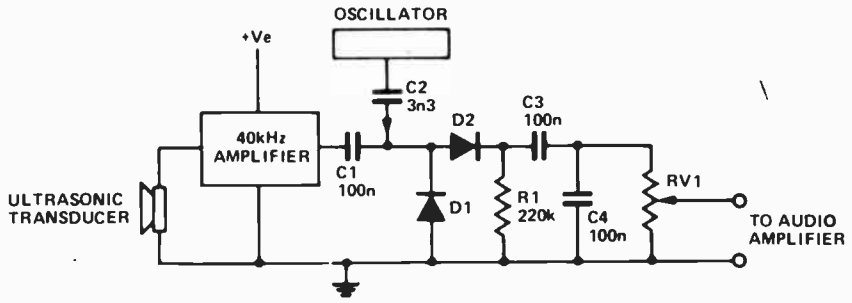



*Figure 11.* **Ultrasonic sounds can be rendered audible by 'heterodyning' the input to an ultrasonic transducer down to the audible frequency range. The frequency range covered depends on the particular transducer employed; i.e: a 25 kHz or a 40 kHz type.**

## Bat detector

A 'bat detector' converts incoming ultrasonic waves into audio signals which can be heard. In order to construct a bat detector which will respond to a wide range of ultrasonic frequencies, an expensive ultrasonic microphone is usually needed. However, reasonable results can be obtained using a cheap ultrasonic transducer in the type of circuit shown in Figure 11. No transmitter unit is needed.

generates ultrasonic waves. Snapping a finger and thumb together or blowing air through one's teeth are other simple ways of generating ultrasonic waves.

The performance of the Figure 11 circuit does not vary very much as one changes from 40 kHz to 25 kHz transducers, although one is listening to different frequency bands in the two cases. In addition, it does not make much difference whether one has the oscillator operating above or below the ultrasonic frequency to which one is listening. Indeed, no oscillator is required when receiving the ultrasonic waves from rubbing two objects together since the range of frequencies generated by such objects beat with one another.

The oscillator is required when receiving a note from an oscillator connected to an ultrasonic transmitting transducer (such as the circuits of Figures 3 to 5). The use of a transmitter with the bat detector circuit of Figure 11 results in a clear note being produced which it is easy to pick out amongst the noise. The writer found that the note could be detected when the distances between the transmitter and detector were as much as 35 metres in the open air. The maximum distances indoors are greater, since there is less stray ultrasonic noise to interfere with the wanted signal. In particular, ranges in a corridor can be considerably increased by reflections of the ultrasonic waves from the walls towards the receiving transducer. A further increase in the range can probably be obtained by placing the transmitting transducer or the receiving transducer, or preferably both, at the focus of parabolic reflectors.

It is interesting to note that bats emit ultrasonic vibrations between about 25 kHz to almost 160 kHz, whilst small rodents can emit vibrations from about 90 kHz down into the audible range. Insects such as grasshoppers and some moths emit frequencies up to about 80 kHz — 100 kHz. Some of these vibrations can be detected by the Figure 11 circuit, but for optimum results a purpose-built bat detector costing about $1000 is needed. The writer has used the Figure 11 type of circuit to detect the ultrasonic emissions from young mice a few days old by which they communicate with their mother.

## Conclusions

This article has been written to show the experimenter how he can use economical equipment for ultrasonic work. No attempt has been made to cover some of the more difficult aspects of the subject, such as voice modulation of ultrasonic waves for intercom systems or the measurement of distances by ultrasonic pulse techniques or the measurement of wind velocity. The aim has been rather to show what can be done easily by the use of simple circuits.

One can even use one of the circuits of Figures 3 to 5 inclusive to call a dog which has been trained to return to its master on hearing the ultrasonic tone, but it is advisable to use a relatively low frequency for this purpose (20 kHz to 25 kHz) to minimise air absorption and to use a frequency to which the dog is most sensitive. ●

# Lab Notes

# Zero-voltage switching with the CA3059

Ray Marston

The control of mains power employing triacs has wide application — light dimmers, motor controllers, etc — but the radio frequency interference (RFI) produced can be difficult to suppress. A more elegant solution is to switch the mains on and off at or near where it passes through the 'zero volt' point. This article discusses the technique with reference to an IC developed specifically for this application — the CA3059.

THERE ARE TWO basic ways of switching mains power to a load — either via a mechanical switch or via a solid state switch such as a triac. Mechanical switches are fairly slow-acting devices; they suffer from severe arcing at the moment of switching and generate a great deal of RFI (radio frequency interference) at switch-on and switch-off. This RFI can often be heard on domestic radio and TV sets and can cause malfunctioning of some electronic equipment (particularly digital equipment).

Triac switches are fast-acting devices and do not suffer from arcing problems. Nevertheless, they are still capable of generating considerable RFI at switch-on. Why? As the triac turns on, the load current may rise from zero to several amps in a mere couple of microseconds;

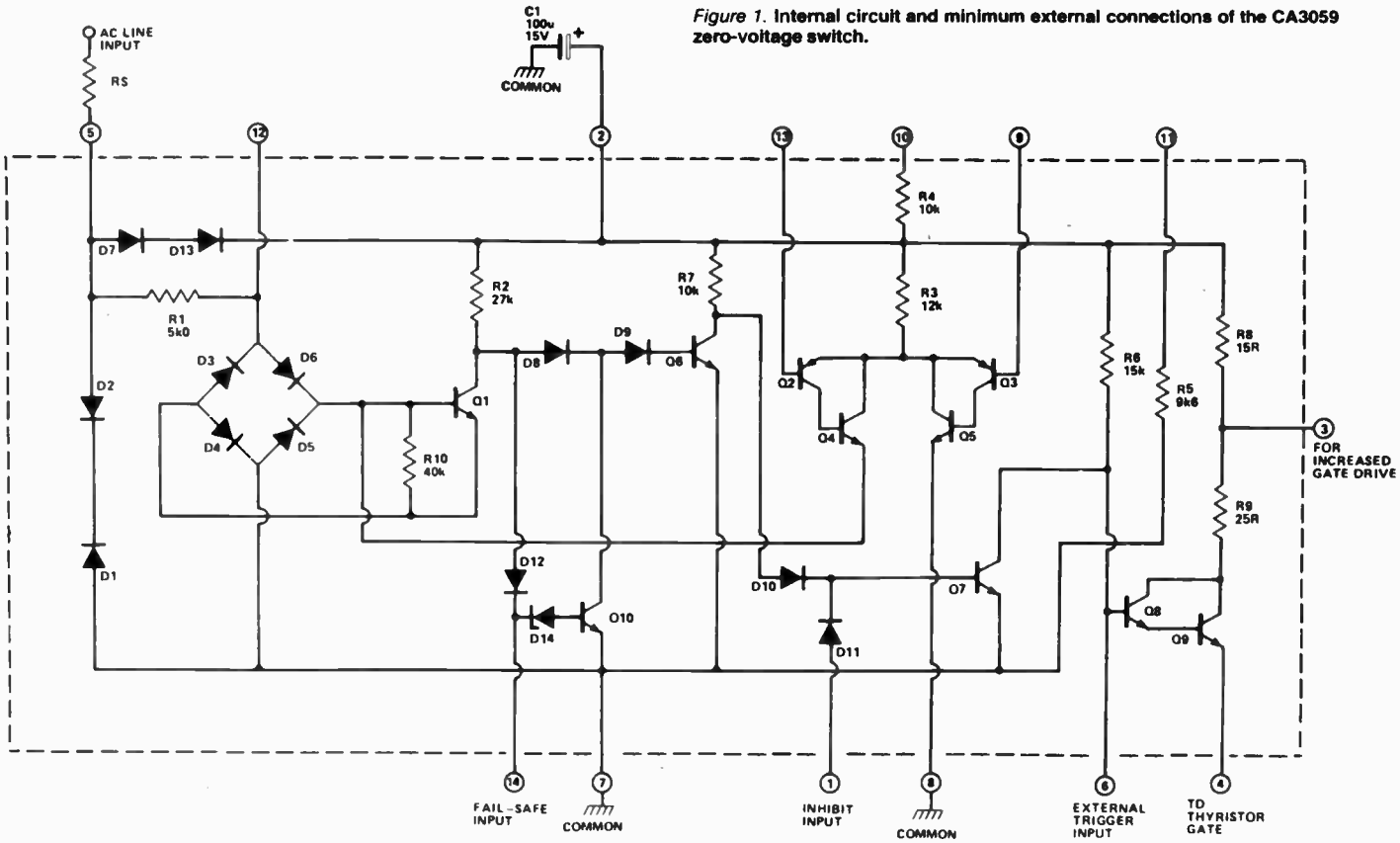



*Figure 1.* **Internal circuit and minimum external connections of the CA3059 zero-voltage switch.**

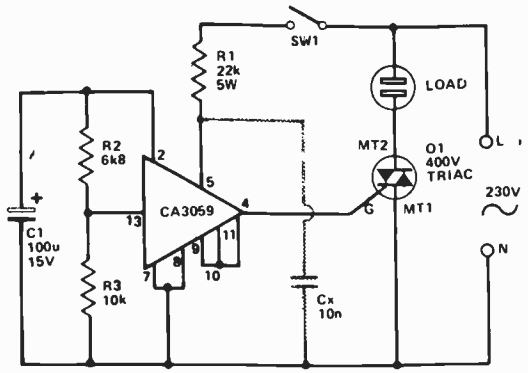



*Figure 2.* **A simple mains-switched zero-voltage switch. Cx may be used to overcome latching deficiencies of some triacs.**

since this current flows through the mains wiring, the wiring may radiate a great 'splurge' of RFI in response to this heavy surge current. The magnitude of the RFI is proportional to $\delta i/\delta t$ and can be reduced by either reducing the surge current amplitude or increasing the surge current rise time, or possibly both; once the triac has turned on, the subsequent large 'rise time' of the 50 Hz mains signal causes virtually zero RFI even when load currents of tens of amps are being drawn.

Thus the degree of triac switch-on RFI is proportional to the value of instantaneous mains voltage at the moment of triac turn-on. If a 100 ohm load is being driven from 230 Vac mains, the surge current will be 3.25 A if switch-on occurs at a 'crest' value of 325 V, or a mere 32.5 mA if switch-on occurs at a 'near zero-crossover' value of 3.25 V.

Triacs are self-latching devices. If they are turned on by a brief gate signal, they remain on until their main-terminal currents fall below a minimum 'holding' value of a few milliamps. They automatically turn off at the end of each mains half cycle as their main-terminal currents fall to near-zero. They can be turned on near the start of each half cycle as soon as their main-terminal currents are capable of exceeding the minimum holding value.

Thus, a triac can be persuaded to generate virtually zero switch-on RFI by feeding it with gate current *only* when the instantaneous mains voltage is close to the zero or crossover value at the start of each half cycle. This technique is known as 'zero-voltage switching'. Special zero-voltage triac-driving ICs are available from a number of manufacturers. One such device is the CA3059, manufactured by RCA.

## The CA3059 zero-voltage switch

The internal circuit and minimal external connections of the CA3059 zero-voltage switching IC are shown in Figure 1. The device is housed in a 14-pin DIL package and incorporates dc power supply circuitry, a zero-crossing detector, triac gate drive circuitry and a high-gain differential amplifier/gating network. Circuit operation is as follows.

Mains power is connected between pins 5 and 7 of the device via limiting resistor Rs (22k, 5 W when 230 V mains is used). D1 and D2 act as back-to-back zeners and limit the pin 5 voltage to ±8 V. On positive half cycles D7 and D13 rectify this pin 5 voltage and generate approximately 6.5 V across the 100 $\mu$F capacitor connected to pin 2. This capacitor supplies sufficient energy storage to drive all internal circuitry and provide adequate triac gate drive, with a few milliamps or so spare drive available for powering auxiliary (external) circuits.

Bridge rectifier D3-D6 and transistor Q1 act as a zero-voltage detector, their action being such that Q1 is turned on (driven to saturation) whenever the pin 5 voltage exceeds ±3 V. Gate drive to an external triac can be made via the emitter (pin 4) of the Q8-Q9 Darlington pair of transistors, but is available only when Q7 is turned off. When Q1 is turned on (pin 5 greater than ±3 V) Q6 is turned off through lack of base drive, so Q7 is driven to saturation via R7 and no triac gate drive is available from pin 4. Triac gate drive is thus available only when pin 5 is close to the 'zero-voltage' or crossover mains value. When gate drive is available, it is delivered in the form of a narrow pulse centred on the crossover point with pulse power supplied by C1.

## Vive la differential

The CA3059 incorporates a differential amplifier or voltage comparator, built around Q2 to Q5, for general purpose use. Resistors R4 and R5 are externally available for biasing one side to the amplifier. The emitter current of Q4 flows via the base of Q1 and can be used to disable the thyristor (pin4) gate drive by turning Q1 on. The configuration is such that the gate drive can be disabled by making pin 9 positive relative to pin 13. The drive can also be disabled by connecting external signals to pin 1 and/or pin 14.

## CA3059 switching circuits

Figure 2 shows the simplest possible way of using the CA3059 as a 'noiseless' switch with the zero-voltage switching provided via the IC and the triac and with on/off switching controlled by SW1. The circuit action is quite simple. The IC is connected to the mains via SW1 and limiting resistor R1; dc energy is stored by C1. The IC is wired in the 'enabled' mode by biasing the pin 9 side of the internal differential amplifier at half-supply (dc) volts via the pin 10 and 11 connections and by biasing the pin 13 side above half-supply via the R2-R3 divider network. Switch SW1 passes only a few milliamps of current and thus generates negligible RFI. The circuit can power mains loads such as lamps and heaters via a suitably rated triac.

The 'zero-voltage' triac-gate-drive pulse of the CA3059 is very narrow. In some applications, the pulse may terminate before the triac main-terminal currents have reached their minimum holding levels and self-latching may fail to occur. This problem can be overcome by wiring Cx as shown in Figure 2. This

# Lab Notes

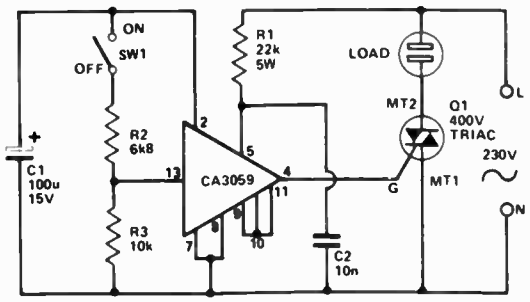



*Figure 3.* **Direct-switched zero-voltage switch.**

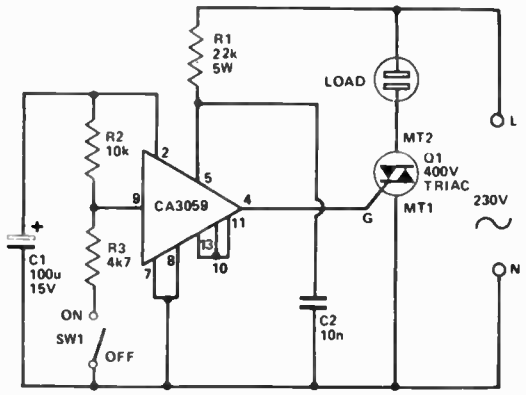



*Figure 4.* **An alternative and very useful method of direct-switching the CA3059 IC.**

capacitor, in conjunction with R1, gives a slight phase shift to the pin 5 signal and extends the 'zero-voltage' pulse further into the start of each mains half-cycle. A value of 10n is adequate in most applications.

The Figure 2 circuit consumes virtually zero mains power under the 'off' (SW1 open) condition. The only defect of the circuit is that SW1 operates at full mains voltage. This defect can be overcome by using the switch to directly enable or disable the CA3059 logic circuitry, as shown in Figures 3 and 4, but in this case the circuit consumes a few watts of power (via R1) when the circuit is in the off mode.

The Figures 3 and 4 circuits work by

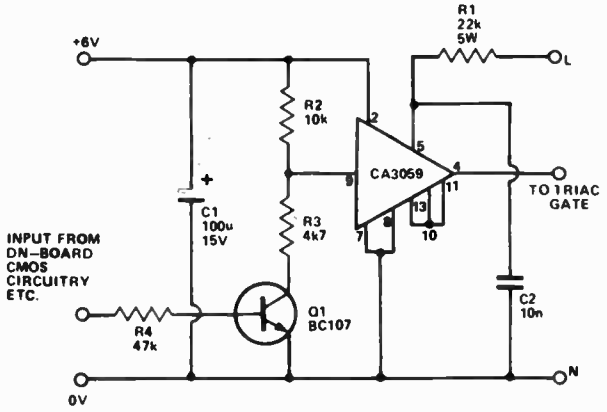



*Figure 5.* **One method of transistor-switching the CA3059 via on-board CMOS circuitry such as one-shots, astables, etc.**

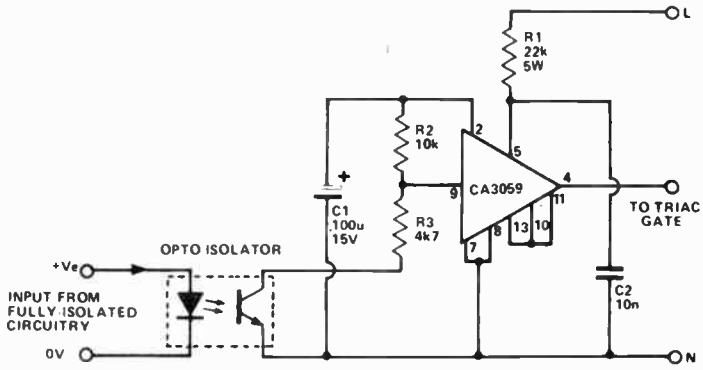



*Figure 6.* **A method of remote-switching the CA3059 via an opto-isolator.**

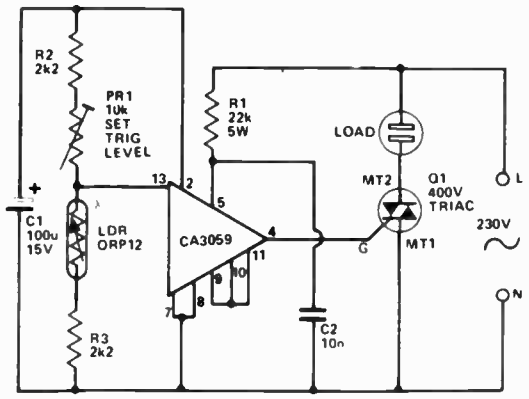



*Figure 7.* **A basic dark-activated zero-voltage switch.**

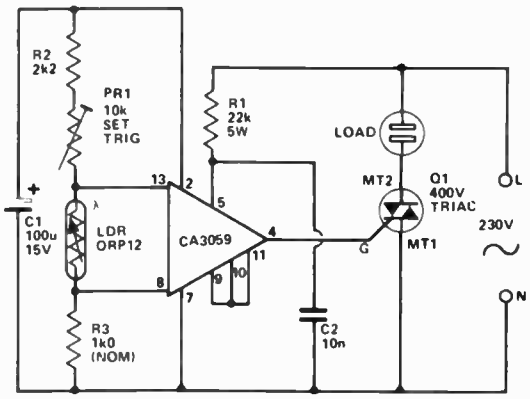



*Figure 8.* **A dark-activated zero-voltage switch with hysteresis provided by R3.**

using the switch to enable or disable the triac gate drive via the internal differential amplifier of the IC. Remember, the drive is enabled only when pin 13 is biased above pin 9. In the Figure 3 circuit, pin 9 is biased at half-supply volts and pin 13 is biased via R2-R3 and SW1. In Figure 4, pin 13 is biased at half-supply and pin 9 is biased via R2-R3 and SW1. In both circuits, SW1 handles maximum potentials of 6 V and maximum currents of 1 mA or so.

Note in Figure 4 that the circuit can be turned on by pulling R3 low or can be turned off by letting R3 float. Figures 5 and 6 show how this simple fact can be put to use to extend the versatility of the circuit. In Figure 5 the circuit can be turned on and off by transistor Q1, which in turn can be activated by on-board CMOS circuitry (such as one-shots, astables, etc) that are powered from the 6 V pin 2 supply.

In Figure 6, the circuit can be turned on and off by fully-isolated external circuitry via an inexpensive opto-isolator; the isolator needs an input current of only a milliamp or so to give the 'on' action.

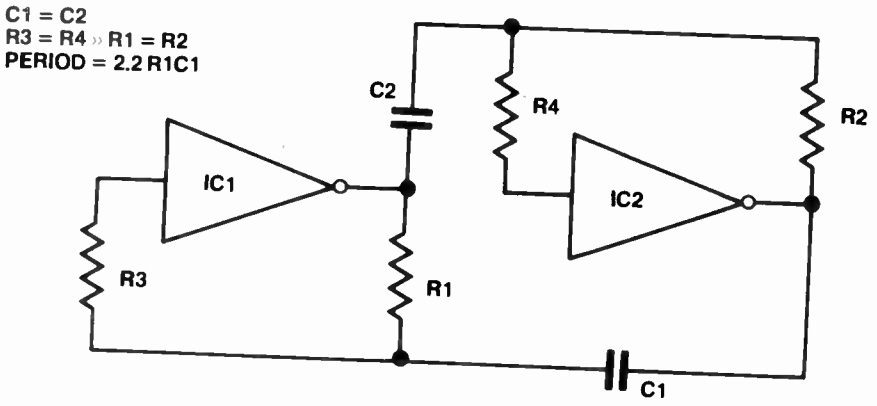
## CA3059 comparator circuits

The built-in differential amplifier of the CA3059 can readily be used as a precision voltage comparator that turns the triac on or off when one of the comparator input voltages goes above or below the other. If these input voltages are derived from transducers such as LDRs or thermistors, the on/off power control action can be controlled by ambient light levels or temperatures. Figures 7 and 8 show two practical circuits of this type.

Figure 7 shows the circuit of a simple dark-activated zero-voltage power switch. Here, pin 9 is tied to half-supply volts and pin 13 is controlled via the R2-PR1-LDR-R3 potential divider. Under bright conditions the LDR has a low resistance, so pin 13 is above pin 9, the triac is enabled and power is fed to the load. The precise threshold level of the circuit can be preset by PR1.

Figure 8 shows how a degree of hysteresis or 'backlash' can be added to the above circuit, so that the triac does not switch annoyingly in response to small changes (passing shadows, etc) in the ambient light level. The hysteresis level is controlled via R3, which can be selected to suit particular applications.

# Symmetric multivibrator using two inverting gates




**Dr. Ton Trancong**

THIS CIRCUIT provides a frequency fairly independent of supply voltage, the output having a near-perfect 1:1 duty cycle. It is based on the improved astable multivibrator circuit described in *ETI Circuit Techniques Volume 1*, p.68, and is useful when low power consumption and simplicity are the main considerations.

The circuit uses the dual RC relaxation circuits formed by R1C1 and R2C2, and is self-starting as it has no stable steady-state. While astable multivibrators using a single RC relaxation circuit suffer non-unity space-to-mark ratio due to the transfer voltage not being exactly halfway between the supply voltages, this circuit avoids the problem by using a dual relaxation circuit based on *two inverter sections on the same IC chip.*

The voltages applied to the gates of both inverters relax exponentially until one of them reaches its gate's transfer voltage. Hence the states of the inverters change instantaneously and the cycle repeats with the two inverters swapping their roles.

Resistors R3 and R4 should have a value of more than three times that of R1 and R2 for the RC relaxation circuits to behave as if R3 and R4 were infinite. However, too high values of R3 and R4 may affect the operation of the circuit as the voltages at the inputs of the inverters may then fail to follow the relaxation voltages. The only requirements for proper operation are that IC1 and IC2 must be sections of the same physical integrated circuit chip, and that corresponding components of the dual circuits must have the same nominal values.

In my particular application, I used a 4009 CMOS hex-inverter chip with R1 = R2 = 300k (20% tolerance), R3 = R4 = 1M (20% tolerance), C1 = C2 = 680p (10% tolerance) of the same production batches. The frequency obtained is fairly stable (with only 33% variation when the supply voltage varies between 3.3 V and 15 V) and its duty cycle is almost a perfect 1:1 over the whole permissible range of supply voltage. When the ratio R3/R1 = R4/R2 is high, the period of the circuit should have the value of 2.2R1C1; in my application it is about 400 ns.

# Lab Notes

# Using the LM 396 10A adjustable voltage regulator

**Barry Davis**

A new voltage regulator using a revolutionary IC fabrication technique has been introduced into the marketplace by National Semiconductor. It is the LM 196/396, a 10 ampere adjustable voltage regulator in a TO-3 package.

THIS NEW regulator has *all the protection features* that hobbyists have taken for granted in the lower power LM117/317 family. It is immune to blowout from excessive output current and all devices are 'burned-in' to guarantee the correct operation of the protection circuits under overload conditions.

The output voltage is adjustable over the range of 1.25 to 15 volts. *The maximum input-output voltage differential* ($V_{in}$ - $V_{out}$) *is 20 volts*, and higher output voltages are possible providing that this parameter is not exceeded. A full load current of 10 amperes is available at all output voltages; however, the maximum power dissipation (70 watts) and the junction temperature must be watched closely. At a load current of 10 amperes, the maximum permissible $V_{in}$ - $V_{out}$ differential is 7 volts. Under these conditions the power dissipated is —

$V_{in} - V_{out} \times I_{max}$

$= 7 \times 10 = 70$ watts.

The features of the regulator are:

- 10 A guaranteed output current.
- 70 W maximum power dissipation.
- Adjustable output from 1.25 to 15 V.
- 100°C burn-in thermal limit.
- Internal current power limiting.
- Input-output voltage differential is 20 V maximum.
- Dropout voltage is approximately 2.1 V.
- TO-3 Package.

The current limit and maximum power dissipation characteristics are shown in Figure 1a and 1b respectively.

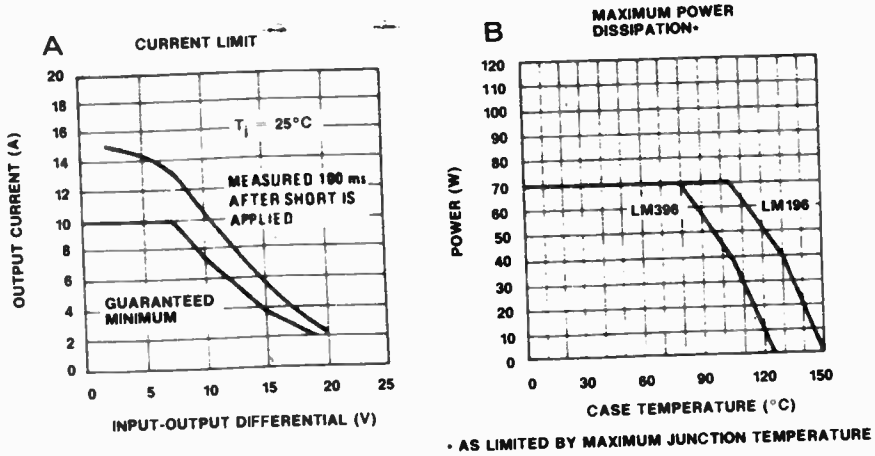



*Figure 1.* **Current limit and power dissipation**

## Application precautions

### 1. Heatsinking

The major limitation in the output current capability of the regulator is heatsinking. The regulator has extremely high power dissipation, 70 watts continuously, providing that the maximum junction temperature limit is not exceeded. These limits are:

LM 196 -55°C to +150°C

LM 396 0°C to +125°C

Careful attention must be paid to *all* junction thermal resistances. A good heat-conductive paste *must* be used when mounting the regulator on the heatsink. The regulator must also be bolted down nice and tight. To ensure

**ABOUT THE AUTHOR**

Barry Davis is a lecturer with the Telecommunications Division of the Royal Melbourne Institute of Technology, engaged in teaching full-time technician students. He has worked in all facets of the electronics industry and is the author of a number of radio and television correspondence courses on fundamentals and servicing for Stotts.

Barry Davis is also the author of a text book called 'Understanding dc power supplies', published by Prentice-Hall earlier this year. This book mentions the development of National Semiconductor's 'Moose-process' LM196/396 regulator which very recently became available — hence this article.

the selection of the correct heatsink, the procedure is as follows.

Calculate the *worst case continuous average power dissipation* in the regulator from the formula:

$P = (V_{in} - V_{out}) \times I_{out}$.

The voltage/current characteristics of the unregulated input must be accurate. A small change in input voltage can result in a large increase in the power dissipated by the regulator. For example, normal operating conditions are:

$V_{out} = 10$ V
$V_{in} = 14$ V
$I_{out} = 10$ A
$P = (14 - 10) \times 10$
$= 40$ watts.

If the input voltage increases by 10% to 15.4 volts:

$P = (15.4 - 10) \times 10$
$= 54$ watts

*— an increase in power dissipation of 35%.*

Therefore, the power supply circuit up to the regulator input (i.e: transformer, rectifier diodes, filter capacitor) plays an important role in the successful operation of the regulator itself. It should be built and tested to determine its average dc output voltage under full load with maximum input voltage. This circuit is shown in Figure 2.

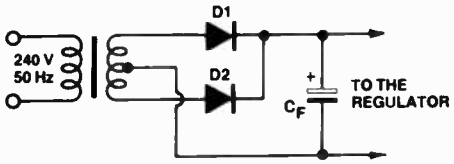
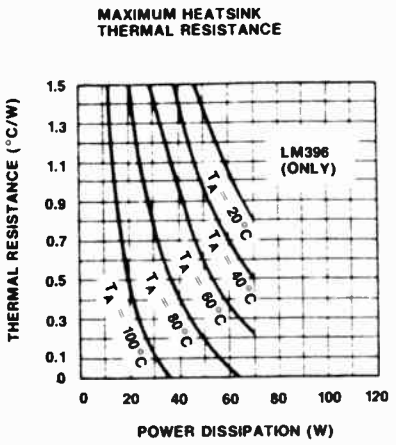



*Figure 2.* **Circuit prior to the regulator.**

The choice of $C_F$ is also very important. At *high* current levels the capacitor ripple current (RMS) is two to three times the dc output current. If the capacitor has an equivalent series resistance (ESR) of 0.05 ohms, this can cause internal power dissipation ($I^2R$) of 20 to 45 watts at an output current of 10 amperes.

The life of the capacitor 'derates' with increase in operating temperature, and the choice of a small-value capacitor is asking for trouble (about 2000 $\mu$F is used for the LM 317 circuit). A value of some *2000 $\mu$F per ampere of load current* is the minimum recommended value. Large values of capacitor will have longer life and will also reduce the ripple



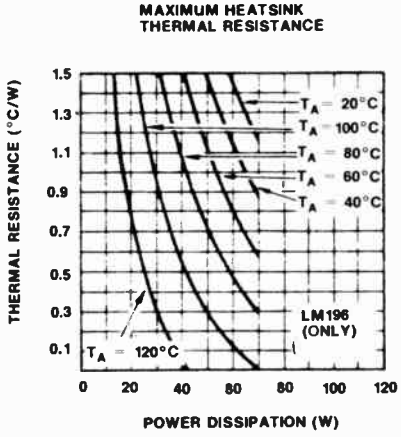




*Figure 3.* **Heatsink thermal resistance graphs ($T_A$ = Ambient temperature)**

level. This allows a lower dc input voltage to the regulator, which will result in savings in transformer and heatsink costs.

A further idea is to place several capacitors in parallel. This increases the capacitance, reduces the net series resistance and increases the heat dissipating area (i.e: shares it among the capacitors). Once the circuit in Figure 2 has been finalised and the average dc output voltage determined, the thermal resistance of the heatsink can be determined from the graphs in Figure 3, in degrees centigrade per watt (°C/W).

For conservative heatsinking it is recommended that you choose $T_A$ to be 35°C higher than anticipated.

The heatsink resistance generally falls into the range of 0.2°C/W - 1.5°C/W at a $T_A$ = 60°C. These are *large* heatsinks such as the Philips 45D6CB, 55D6CB, and the large Minifin. These must be mounted for best convection cooling and could also be cooled by a fan.

## 2. Transformers

Correct transformer ratings are extremely important in high current supplies. If the secondary voltage is too high, power will be wasted and cause unnecessary power dissipation in the regulator. However, if the secondary voltage is too low it may cause loss of regulation if the input voltage (i.e: mains) fluctuates excessively.

The following formula can be used to calculate the secondary voltage required using the circuit in Figure 2 (full wave centre tap).

$$V_{(RMS)} = \frac{V_{out} + V_{reg} + V_{Rect} + V_{Ripple}}{\sqrt{2}} \times \frac{V_{Nom}}{V_{Low}} \times (1.1) \quad (1)$$

Where:

1.1 is the factor accounting for load regulation of the transformer.

$V_{out}$ = dc regulated output voltage.

$V_{Reg}$ = Minimum $V_{in} - V_{out}$.

$V_{Rect}$ = Voltage drop (forward) across the diode at $3 \times I_{out}$.

$V_{Ripple}$ = Peak capacitor ripple voltage (½ p-p).

$$\text{i.e: } \frac{(5.3 \times 10^{-3})\, I_{out}}{2C}$$

C is the capacitor value in farads.

$V_{Nom}$ = Normal ac input (RMS).

$V_{Low}$ = Minimum ac input (RMS).

The current rating required can be calculated from the formula:

$$I_{RMS} = I_{out} \times 1.2 \quad (2)$$

Where $I_{out}$ = dc output current.

Transposing formula (2) we can calculate the value of filter capacitor required:

$$C = \frac{(5.3 \times 10^{-3})\, I_{out}}{2 \times V_{Ripple}} \quad (3)$$

The best way to appreciate these formulas in use is to calculate the values required for a power supply circuit. If we design a good mobile radio power supply, 13.8 volts at 10 amperes:

$V_{out}$ = 13.8 V
$I_{out}$ = 10 A
Assume $V_{Reg}$ = 2.2 V, $V_{Rect}$ = 1.2 V
$V_{Ripple}$ = 2 V p-p, $V_{Nom}$ = 240 V
$V_{Low}$ = 220 V
Using formula (1)

$$V_{(RMS)} = \left(\frac{13.8 + 2.2 + 1.2 + 1}{\sqrt{2}}\right)\left(\frac{240}{220}\right)1.1$$

$$= \frac{18.2}{\sqrt{2}} \times 1.09 \times 1.1$$

$$= 12.869 \times 1.09 \times 1.1$$

$$= \underline{15.4 \text{ volts (RMS)}}$$

Using formula (2)

$$I_{(RMS)} = 10 \times 1.2$$

$$= 12 \text{ amperes (RMS)}$$

The transformer must therefore be 240: 30 CT at 12 amperes. The centre tap (CT) will provide 15 volts secondary voltage for each diode.

The size of the filter capacitor required can be calculated using formula (3)

$$C = \frac{(5.3 \times 10^{-3})\ 10}{2 \times 1}$$

$$= 26500\ \mu F$$

The transformer, rectifier and filter circuit is now shown in Figure 4.

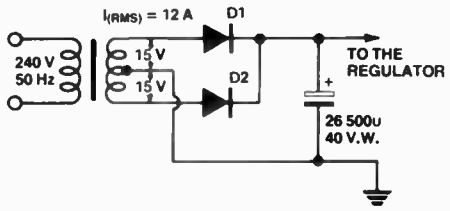



*Figure 4.* **Rectifier and filter circuit**

### 3. Diodes

The diodes used in the circuit must have a high dc current rating. The capacitor input filter draws high peak current pulses that are considerably higher than the average dc current. With a 10 amperes supply the average current is 5 amperes. The current pulses' duration and amplitude result in a long-term diode heating of approximately 10 amperes dc. Therefore the diodes should have a rating of at least 10-15 amperes. Also, the power supply may have to survive a short circuit and average current could rise to 15 amperes (see Figure 1a).

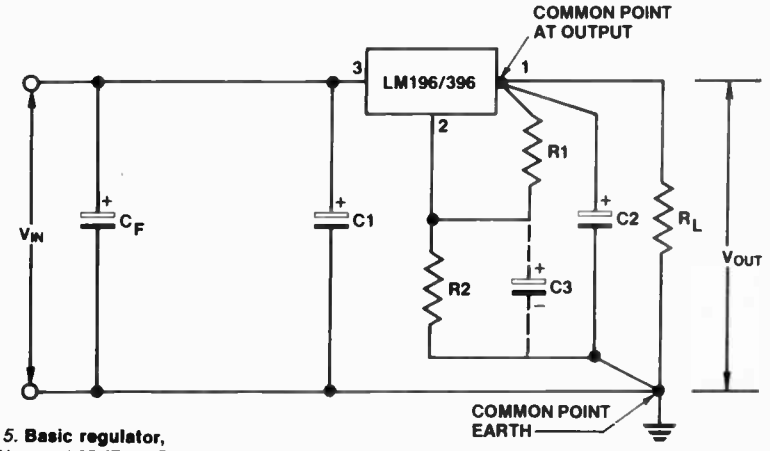



*Figure 5.* **Basic regulator,** $V_{out} = 1.25\ \frac{(R1 + R2)}{R1}$

Another important factor in the choice of diode is the surge current at switch on. The peak *surge current* is about *10-20 times the dc output current* (i.e: 100-200 A for a 10 A supply). (Note: smaller transformers and filter capacitors may be used in lower current supplies. This will reduce the surge current; unless you are sure of the worst case surges, do not economise on diodes.)

Stud-mounted diodes in a DO-4 or DO-5 package are recommended, such as IR 12F10B, IN3209 or 16F10 silicon rectifiers. Remember to choose the correct PIV for the type of transformer in use (PIV = $\sqrt{2}\ V_{Secondary}$).

### 4. Wiring

High load currents produce higher than normal voltage drops across the resistance of the wiring. It is suggested that 16-18 gauge wire is used for input and output connections, and the *length is kept to a minimum.*

The two resistors used to set the output voltage level are connected:

1. directly to a common point earth and
2. directly to the output of the regulator as shown in Figure 5.

## Components in Figure 5.

$C_F$ = Main filter capacitor 26 500 $\mu$F.

C1 = 4$\mu$7 tantalum. It is only necessary if the main filter capacitor is more than 150 mm away from the regulator. Connecting wire is 18 gauge or larger.

C2 = 4$\mu$7 tantalum. It is not absolutely necessary, but is recommended to maintain low output impedance at high frequencies.

C3 = 25 $\mu$F. Improves ripple rejection, output impedance, and noise. (Capacitor C2 should be close to the regulator if C3 is used).

R1 = 120 ohms. It should be a wirewound or metal film resistor, tolerance 1% or better.

R2 = calculated to set $V_{out}$; the same type of resistor as R1.

The value of R2 can be calculated from the formula:

$$R_2 = \left(\frac{V_{out}}{1.25}\right) \times R1 - R1$$

Example:

$V_{out}$ = 13.8 V
R1 = 120 ohms

$$R2 = \left(\frac{13.8}{1.25}\right) \times 120 - 120$$

$$= (11.04 \times 120) - 120$$

$$= 1324.8 - 120$$

$$= 1204.8 \text{ ohms.}$$

As stated earlier, the package is a TO-3 and the connections are shown in Figure 6.

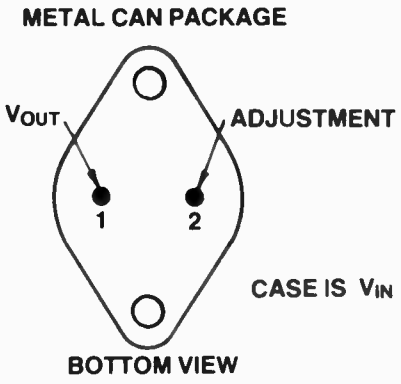



*Figure 6.* **Connection diagram**

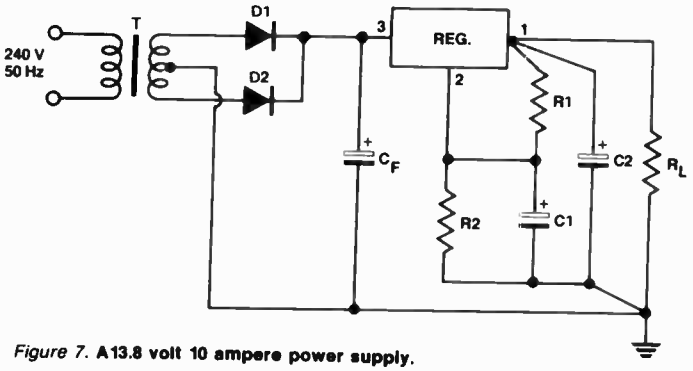



*Figure 7.* **A 13.8 volt 10 ampere power supply.**

The complete circuit can now be built, incorporating Figures 4 and 5. The circuit diagram of the final 13.8 V 10 A power supply is shown in Figure 7.

## Component values for Figure 7.

T = 240 : 30 CT at 12 amperes.
D1 = 16F10 DO-4 case.
D2 = 16F10 DO-4 case.
CF = 26500 $\mu$F 40 VW (ideally, capacitors in parallel).
C1 = 25 $\mu$F 16 VW.
C2 = 4$\mu$7 tantalum 16 VW.
R1 = 120 ohms 1% metal film.
R2 = 1k2 1% metal film.
Reg = LM396 on a 6" 55 or 65D heatsink.

$$V_{out} = 1.25\left(\frac{R1 + R2}{R1}\right)$$
$$= 1.25\left(\frac{120 + 1200}{120}\right)$$
$$= 1.25 \times 11$$
$$= 13.75 \text{ volts}$$

A highly desirable situation would be to *reduce* the power dissipated by the regulator. This can be achieved by supplying part of the output current around the regulator as shown in Figure 8.

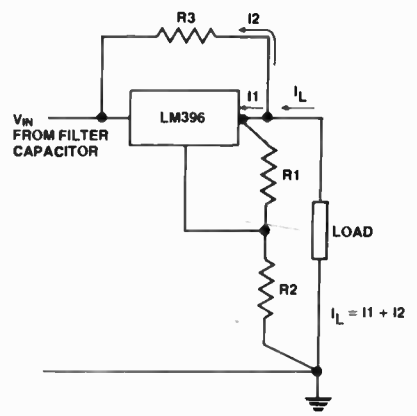



*Figure 8.* **Reducing regulator power dissipation**

Resistor R3 is selected to supply a portion of the load current. In this case a *minimum load must always be maintained*. This prevents the regulated output from rising uncontrolled. The value of R3 must be greater than:

$$\frac{V_{max} - V_{out}}{I \text{ min}} \text{ ohms}$$

Where: $V_{max}$ is worst case high input voltage.
$I_{min}$ is the minimum load current.
Power rating must also be considered and R3 must be rated at a minimum of:

$$\frac{(V_{in} - V_{out})^2}{R3} \text{ watts}$$

This circuit configuration will reduce the regulator power dissipation by a factor of 2 to 3, if the minimum load current is about 50% of the full load current.

## Precautions when using R3

1. The power rating of R3 must be *increased* to $\frac{(V_{max})^2}{R3}$ watts if continuous output short circuits are at all likely.
2. Under short circuit conditions the *overall circuit* power dissipation increases by $\frac{(V_{in})^2}{R3}$ watts.

The regulator and R3 will not be harmed (if R3 is the correct wattage), but the circuit components prior to the regulator (diodes, transformer) must be able to withstand the overload condition (i.e: the power rating is sufficient to handle the excess current).

The only problem with this technique is the large power rating required for resistor R3. If $V_{in} - V_{out} = 7$ volts and R3 = 2 ohms, the power dissipated by the resistor is:

$$\frac{(7)^2}{2} = 24.5 \text{ watts}$$

with 3.5 A of current passing through it.

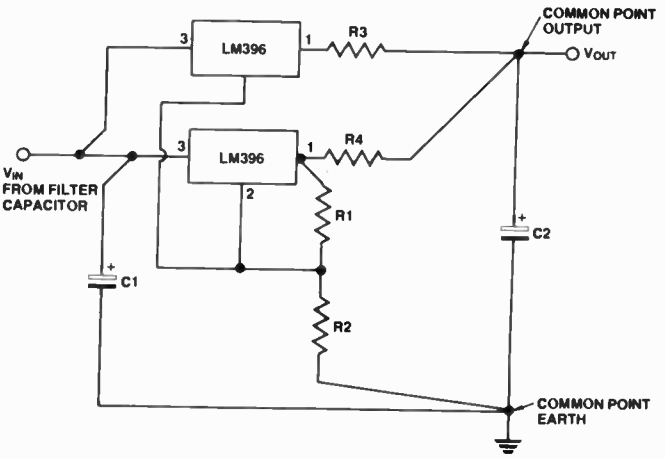



*Figure 9.* **Quasi-parallel regulators**
**R1 = 120 ohms**
**R2 chosen to set $V_{out}$**
**R3, R4 = 0.015 ohms**
**C1 = 4$\mu$7 tantalum**
**C2 = 100$\mu$F**

## High Current Output

Placing regulators in parallel is not recommended because they may not share the current equally. The regulator with the highest reference voltage will handle the highest current up to the time it current limits. Therefore, one regulator may be flat out handling 16 A while the other is cool and calm passing only 2 A. Reliability cannot be guaranteed under these conditions because of the high junction temperature of regulator one.

However, if load regulation is not critical, the regulators may be connected quasi-parallel, as shown in Figure 9. This circuit will share current to within 1 ampere, and in the worst case 3 amperes. However, the payoff is in the load regulation. It is degraded by 150 mV at 20 ampere loads compared to about 20 mV with 10 ampere loads. This should not cause too much of a problem in higher voltage power supplies. ●


### Acknowledgement

*This article was made possible by the courtesy of National Semiconductor. Data and basic circuits were taken from their publication 'LM196/LM396 10 Amp Moose Adjustable Voltage Regulator'.*

# HIGH VOLTAGE FOR LOW COST

by Walter Wills, Varo Semiconductor

**Simple diode-capacitor networks can be cascaded to deliver any desired voltage.**

IF YOU NEED a power supply for a high-voltage low-current application, your best bet is probably the voltage multiplier circuit. It's inexpensive. It's simple. And you can get any voltage you want by cascading multiplier stages. The voltage is limited only by the ratings of the components you use.

A voltage-multiplier circuit contains diodes and capacitors, with the devices connected to develop a dc output that is a multiple of the peak or peak-to-peak input voltage. There are two major variations of the circuit: multipliers that use an even number of diodes and those that use an odd number of diodes.

The basic rectifier circuits in Fig. 1. (equations assume perfect diodes and capacitors, loads are considered light) can be combined to form a complete family of half-wave multipliers. A full-wave multiplier can be made by combining two half-wave multiplier sections, one positive and one negative (Fig. 2), The major disadvantage of a full-wave multiplier is that the secondary side of the transformer nearest the core requires heavy insulation to withstand one-half the output voltage. Therefore inductive coupling is worse and efficiency lower than for a transformer used with the equivalent half-wave type. Thus half-wave multipliers are better for most high-voltage power supplies.

Figure 3 shows the two variations of half-wave multipliers. Each of these circuits consists of identical sections cascaded, except for the first stage in Fig. 3a. The first section of a multiplier with an odd number of diodes is a simple half-wave rectifier. This first section of a multiplier with an even number of diodes is a half-wave doubler. A basic rule of thumb for multiplier designs is: For waveforms that are symmetrical about zero, use an even number of diodes; for asymmetrical waveforms, use an odd number.

## CALCULATING THE OUTPUT VOLTAGE

The regulation of a multiplier with a load is a function of the input's source impedance, the values of the capacitors in the multiplier, the forward drop of the diodes and the turn-on and turn-off times of the diodes. The output voltage of a multiplier is approximately

$$V_{out} = N\frac{(V_1 + V_2)}{2} - \frac{N^3}{12Cf} \cdot I_{out}$$

Here N is the number of diodes or capacitors used for circuits like those shown in Fig. 3; $V_1$ is the positive peak input voltage; $V_2$ is the negative

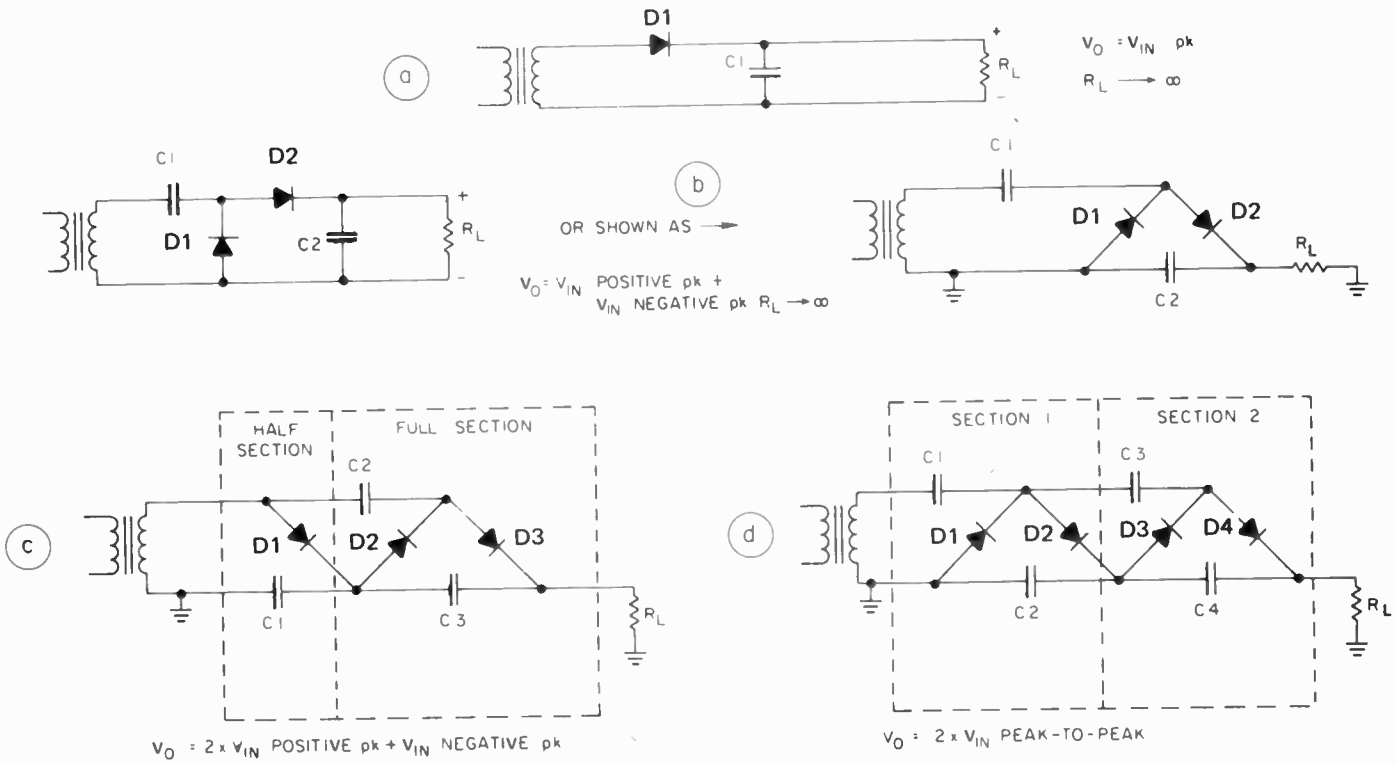



*Fig. 1. The basic half-wave rectifier circuit (a), can be modified to become a voltage doubler (b). Various higher output voltages can be obtained by adding further sections (c and d).*

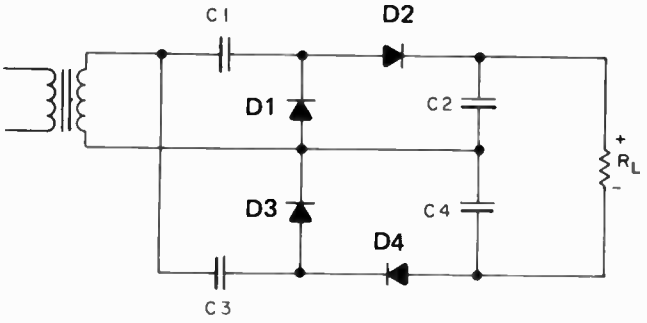



*Fig. 2. The full-wave voltage quadrupler circuit requires a transformer with heavy secondary insulation.*

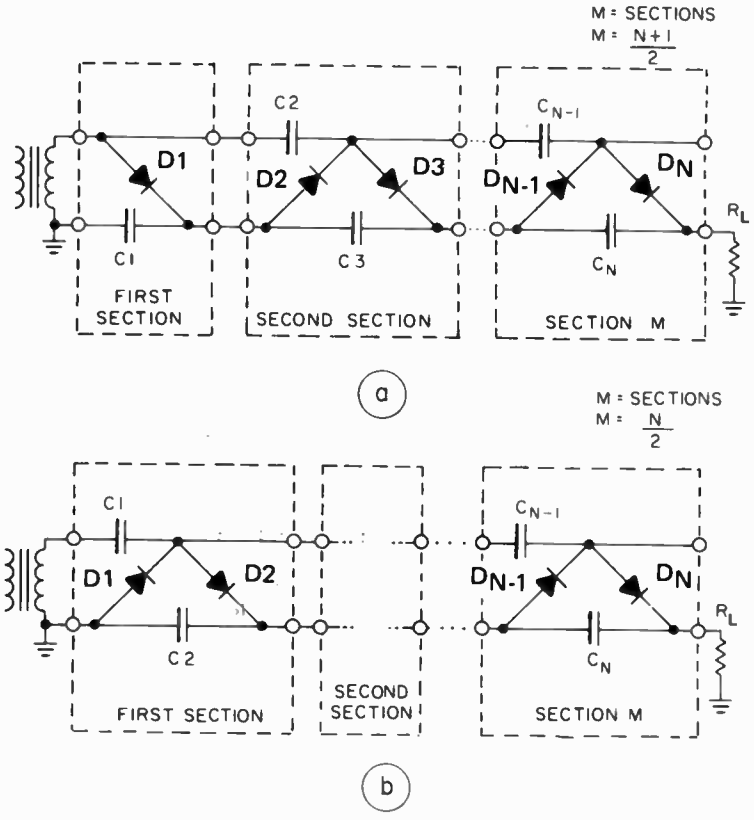



*Fig. 3. A multiplier with an odd number of diodes works best for assymetrical waveforms (a). An even number of diodes (b) is best for symmetrical waveforms.*

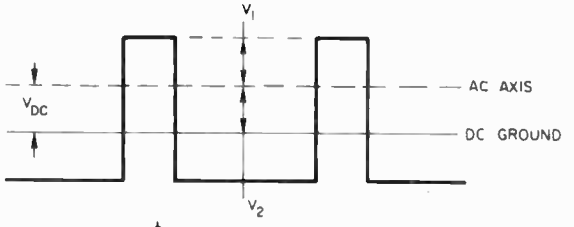



*Fig. 4. A recurring waveform with a positive peak $V_1$ and negative peak $V_2$ is used as an input for the voltage multiplier circuit described in Fig. 5.*

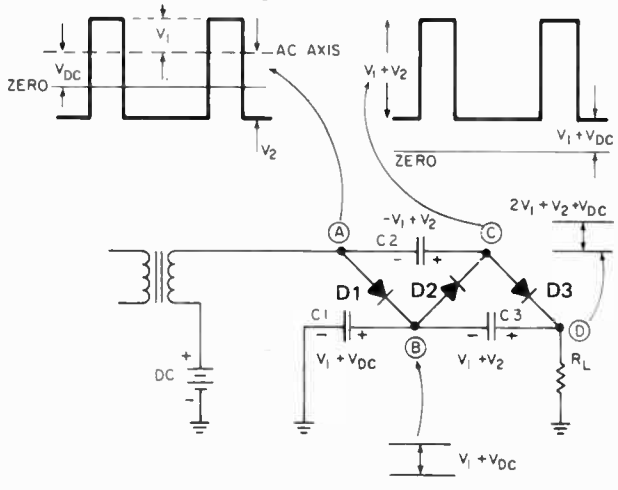



*Fig. 5. The voltage waveforms at different points within the multiplier circuit with an odd number of diodes show the transformation of the pulse waveform described in Fig. 4 into a much higher dc voltage.*

peak input voltage; C is the capacitance in farads; f is the frequency of the input, and $I_{out}$ is the current in amperes. This equation assumes a sufficiently large load capacitance, equal value capacitors, and ideal diodes. It will produce sufficiently accurate results for all practical purposes.

## WATCH DIODE SWITCHING CHARACTERISTICS

The turn-on and turn-off times of the diodes are important if high frequencies are involved. Both turn-on and turn-off must be kept fast, if regulation and efficiency are to be maintained.

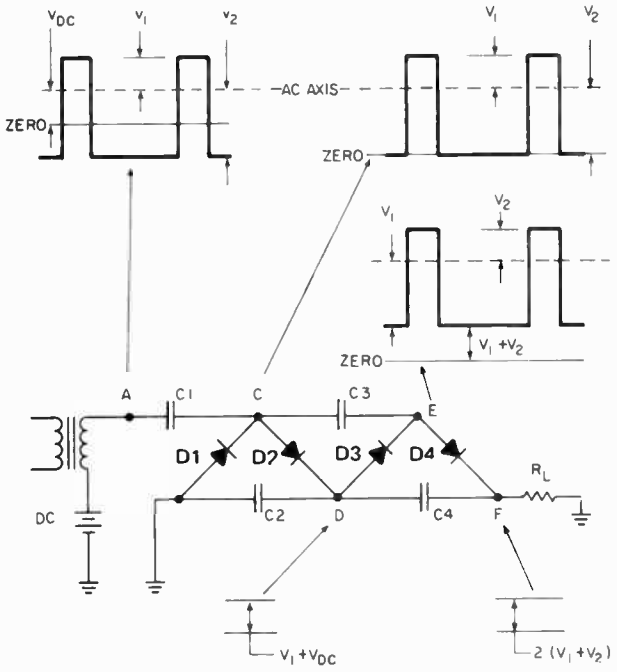
The forward voltage drop of the diodes is not a significant factor. For example, a typical multiplier, rated for 25 kV at 2 mA, has six diodes, each with a forward voltage drop of approximately 0.7 V at 10 mA. Thus the multiplier drops less than 5 volts across its diodes when operating.

The output regulation of voltage multipliers ranges from 100 V to 5 kV per milliamp of current. Some applications use regulation schemes to control power-supply output. Some common methods are shunt dc load, rectified pulse feedback and a saturable reactor in series with the high-voltage transformer. In other applications, it is desirable to have the output voltage sag with load — with very poor regulation built into the multiplier through selection of the capacitor's value.

The output voltage of a multiplier will always have some ripple in the output. Ripple is a function of load capacitance, input frequency, multiplier impedance and input-to-output coupling.

The load capacitance acts as a filter, and the effective series impedance of the multiplier limits voltage ripple. If regulation is not a consideration or if load current is almost constant, a series resistor can be added to the multiplier output. The series resistor will act with the load capacitance as an RC filter.

The high-frequency components of the input voltage are the most easily coupled into the output. But the higher frequencies are also easier to filter at the multiplier output when necessary. The most unpredictable ripple component, though, is generated by stray capacitive coupling of the input to the output terminal. This coupling is difficult to control. The mechanical layout of the multiplier can reduce it, and if more ripple reduction is required, an electrostatic shield can be used to isolate the output area further from the input.



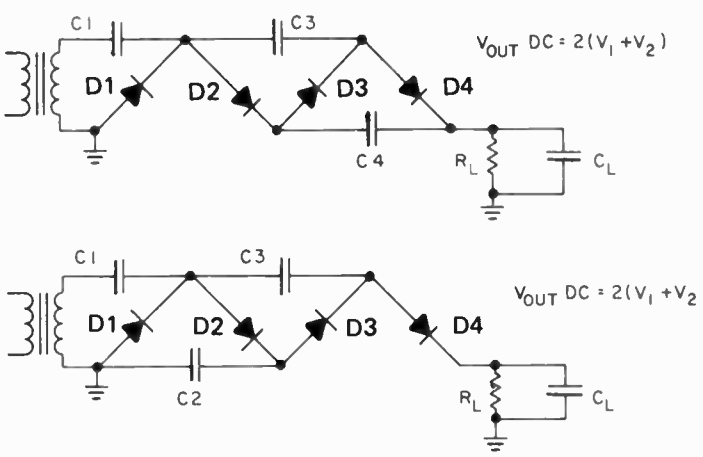







*Fig. 7. To reduce component cost and count if the load is capacitive remove one of the doubling capacitors.*

*Fig. 6. The multiplier circuit with an even number of diodes and the same input as described in Fig. 4 produces an even larger dc output voltage than the circuit of Fig. 5.*

## HOW MULTIPLIERS WORK

The multiplier circuit can handle any waveform, but the three most common for multiplication are sine, pulse (or square) and trapezoidal wave. The only waveform restrictions are that the rise and fall times of the input signal be slower than the diode switching time.

In the signal in Figure 4, $V_{in}$ is a recurring waveform composed of the positive peak V1, the negative peak V2 and an ac axis that can be displaced from dc zero by voltage Vdc.

Figure 5 shows the voltages at each point of a 1.5-section multiplier. The half-wave, 1.5-section multiplier (three-diode) operates as follows: during the positive peak of $V_{in}$, diode D1 conducts to charge C1 to a voltage equal to V1 + Vdc. Capacitor C2 acts as a coupling capacitor to couple $V_{in}$ to point C. Diode D2 conducts on the negative voltage peak at point C when the voltage tries to become more negative than the anode of D2 (the anode voltage of D2 is V1 + Vdc). Diode D3 conducts on the positive peak at point C and charges C3 to V1 + V2. The output, $V_{out}$, is the sum of the voltages on C1 and C3:

$$V_{out} = V1 + Vdc + V1 + V2 = 2V1 + V2 + Vdc.$$

Only dc voltages are applied to C1 and C3; these capacitors are therefore dubbed 'dc capacitors'. An ac voltage is applied to C2, which is called an 'ac capacitor'. If the input voltage is symmetrical about the zero axis, the multiplier output will be three times (either) peak voltage, $V_{out} = 3$ V1. This circuit is called a tripler. If, however, the waveform is such that V1 is much greater than V2, the output voltage is approximately twice V1. The circuit could be called a doubler. For clarity, we can use the diode count to define multiplier capability.

The operation of the four-diode multiplier — a two-section, half-wave unit — is similar to that of the three-diode multiplier (Figure 6). Capacitor C1 blocks the dc bias from the remainder of the multiplier and acts as a coupling capacitor to couple $V_{in}$ to point C. Diode D1 conducts when the negative voltage at point C becomes more negative than the anode of D1 (the anode of D1 is at 0 V). This causes C1 to charge to a voltage equal to V2 − Vdc and causes the positive peak at point C to reach V1 + V2.

The positive voltage at point C turns on D2 and charges C2 to V1 + V2. Capacitor C3 acts as a coupling capacitor to couple the input waveform at point C to point E. Diode D3 conducts when the cathode voltage becomes more negative than the anode voltage (the voltage at point D). The positive peak will be at a voltage equal to the voltage on C3 plus the peak voltage at point C. This positive voltage will cause D4 to conduct and charge capacitor C4 to V1 + V2. The output, $V_{out}$, is the sum of the voltages on C2 and C4.

$V_{out} = (V4 + V2) + (V1 + V2) = 2\,V1 + 2\,V2$.

Both C2 and C4 are dc capacitors. Points D and F are 'dc points', and C1 and C3 are ac capacitors. In both the odd-diode and even-diode circuits, the diode peak-inverse voltage (PIV) ratings should be at least V1 + V2. In the even-diode multiplier, C1 should have a voltage rating of at least V2. In the odd-diode multiplier, C1 should have a voltage rating of at least V1 + Vdc. All the other capacitors should have a voltage rating of at least V1 + V2. Negative output voltages can be obtained if the diode polarities are reversed.

## VARIATIONS FOR SPECIAL APPLICATIONS

For applications with a very high load capacitance, any one of the dc capacitors can be omitted in the multiplier and it will still function (Fig. 7).

While this appears to be a good way to reduce component costs and package size, consider what happens when the output terminal is arced to ground: the distribution of voltages on the diodes becomes unequal, which causes more stress on some diodes than others. The uneven distribution can cause a diode's peak inverse rating to be exceeded and a malfunction to occur. For better transient protection, leave all the capacitors in the circuit.

Many applications require a second voltage that is proportional to the output voltage. A tap at any dc point of the multiplier can be used. The ratio of the voltages can be determined if you examine the circuit up to the tap as a complete unit and the total multiplier as another.

Consider carefully the maximum average current. The multiplier current ratings are intended to keep the components cool enough to perform reliably. It will help, of course, if the high-voltage drive source has some maximum-load protection that reduces the input voltage if too much current is demanded.

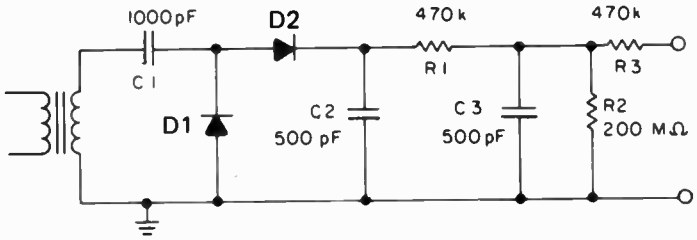



*Fig. 8. A voltage doubler can be combined with a filter to provide very low ripple outputs. (The example shown gives a 30 kHz, 10 kV, 50μA output)*

The multiplier must withstand all arcing, including that between the output lead and ground. and also direct shorts of the output lead to ground. The multiplier must sustain the peak current drawn by the arc or short as the internal capacitors discharge.

A resistor in series with the output lead serves two functions: (1) It reduces the Q of the oscillator circuit that is established during arcing, thus reducing considerably the stress on the diodes, and (2), it limits the peak current to a value that the diodes can handle safely. The value of this resistance must be high enough to do the limiting job but not so high as to promote arcing around or through the resistor body or overheating at maximum current drain when the output arcs to ground.

## CONSIDER THE MECHANICAL LAYOUT

The mechanical design, mounting method and location of the multiplier can all affect current capability.

Remember that very high voltages may be involved so pay particular attention to component layout and insulation — also ensure that there are no sharp edges that might otherwise initiate corona discharge. ●

# "Brilliance boost" for guitar

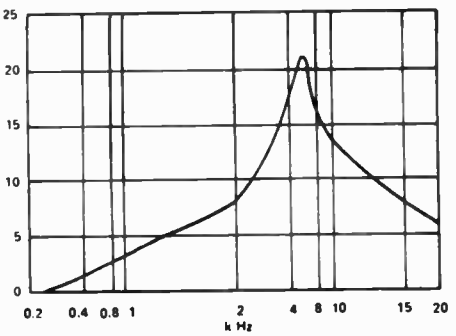
A TREBLE BOOSTER circuit can be used with a guitar, and other electronic musical instruments, to boost a range of the higher order harmonics and give a more "brilliant" sound. A circuit to achieve this has a fairly flat response at the bass and across most of the middle frequencies while the upper middle and most of the treble frequencies are given a substantial gain boost.

The circuit is basically just an op-amp (IC1) used in the non-inverting amplifier mode. The non-inverting input is biased by R4 and R5 via a decoupling network which is comprised of R3 and C3. C4 and C5 give dc blocking at the input and output respectively. With SW1 open there is virtually 100% negative feedback through R1, R2 and C1, giving the circuit unity gain and a flat response. Closing SW1 brings C2 into circuit, and this decouples some of the feedback through R1 and R2 at frequencies of more than a few hundred Hz, giving the required rising response.

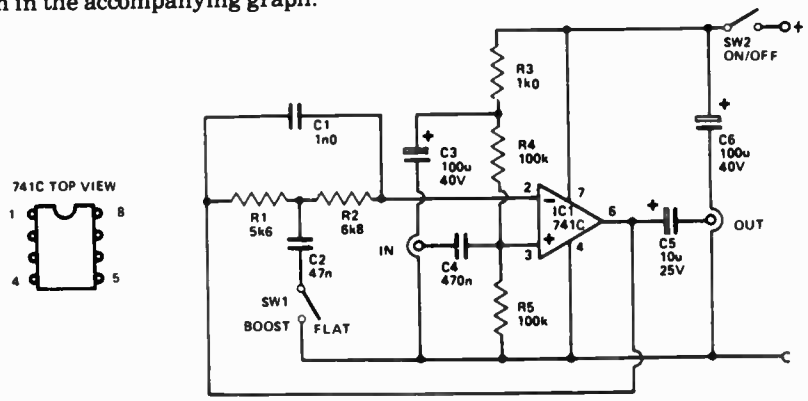
Feedback through C1 at high treble frequencies causes the response to fall away above about 5.5 kHz, and prevents the very high frequency harmonics from being excessively emphasised.

As the unit has unity gain at frequencies where boost is not applied it can simply be connected between the instrument and the amplifier.

It is normal to give only a modest amount of emphasis to the upper-treble in order to get good stability and a low noise level. This also prevents the output from sounding too harsh. The frequency response of this treble booster is shown in the accompanying graph.




THE FREQUENCY RESPONSE OF THE TREBLE BOOSTER



# Lab Notes

# "For members only . . ." — the exclusive OR gate

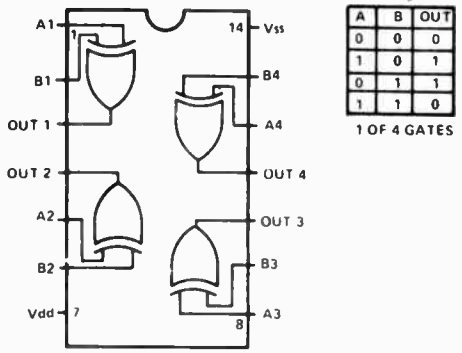
The 4070B quad EX-OR gate is one of the least known but most useful members of the commonly available family of CMOS quad two-input gate ICs. The device's gates can readily be used as programmable (inverting or non-inverting) pulse amplifiers, phase comparators, free-running or gated astables, or multi-bit magnitude checkers, etc. Pretty good for a cheap chip!

**Ray Marston**

THE OUTLINE and pin notations of the 4070B are shown in Figure 1, together with the truth table for each of the EX-OR gates in the package. The most important point to note here is that the output goes high only (EXclusively) if a logic 1 is applied to only one of the inputs (A OR B). The output takes a logic 0 state if identical inputs are applied to both inputs.

Figure 2 shows how individual gates can be used as programmable pulse amplifiers. With the connections shown in Figure 2a, the circuit functions as an inverting amplifier. In Figure 2b the amplifier acts in the non-inverting mode, while the Figure 2c circuit shows the connections for making a switch-programmable amplifier.

The EX-OR programmable amplifier can be used as the basis of a so-called scrambler system of the type used on security telephones, etc, by using the basic circuit shown in Figure 3. Here, in




| A | B | OUT |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

1 OF 4 GATES

*Figure 1.* **Pin notations, outline and truth table of the 4070B quad two-input EX-OR gate.**

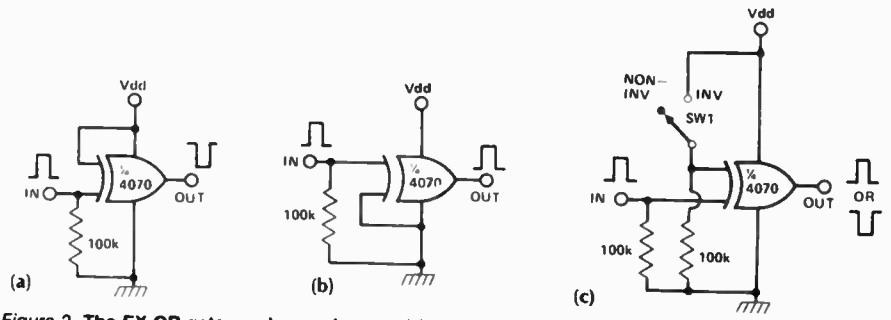



*Figure 2.* **The EX-OR gate can be used as an a) inverting, b) non-inverting, or c) switch programmable pulse amplifier.**

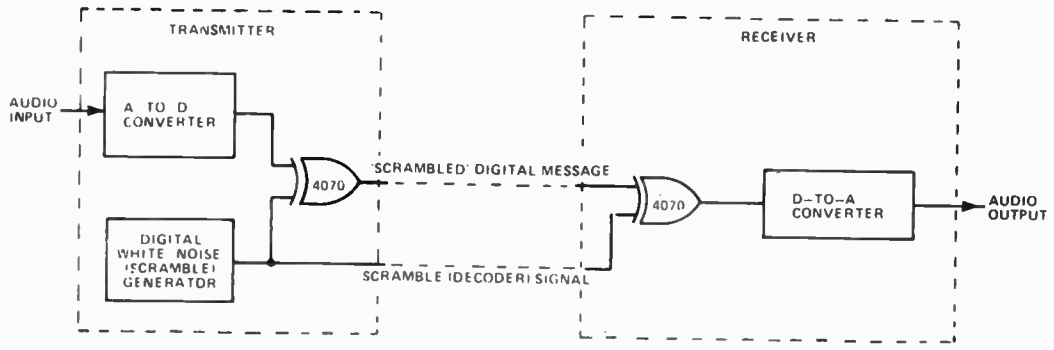



*Figure 3.* **Basic circuit of an audio (telephone, etc.) scrambler system.**

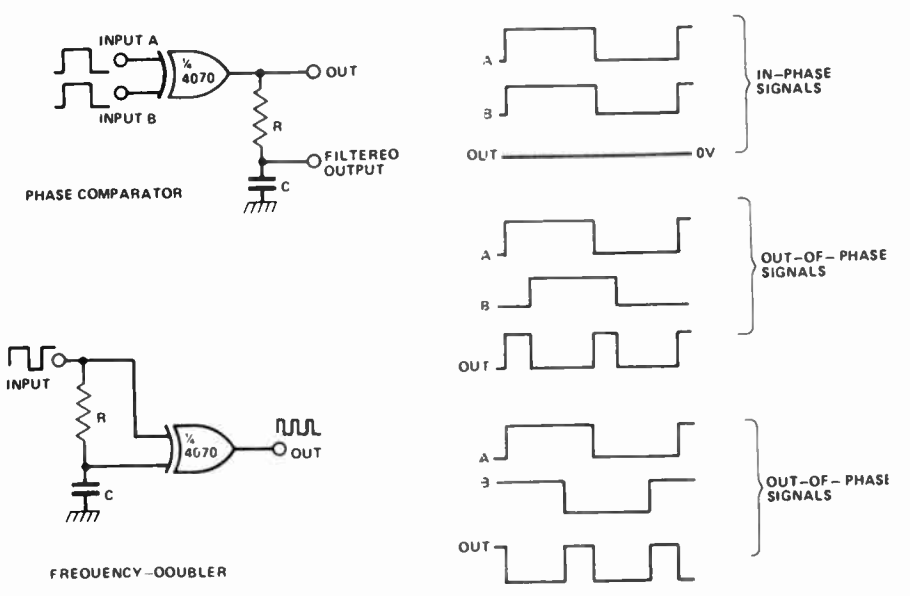



*Figure 4.* **An EX-OR gate can be used as both a phase comparator and a frequency doubler. Typical waveforms for the phase comparator circuit are shown on the right.**

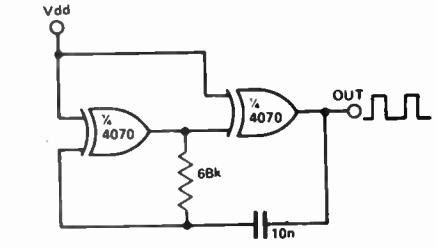



*Figure 5.* **A 1kHz EX-OR astable.**

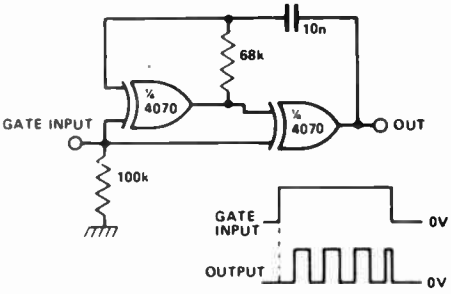



*Figure 6.* **A gated 1 kHz EX-OR astable.**

the transmitter, the audio signal is converted to digital form by an A-to-D converter and fed to one input of the EX-OR gate, while the other input is fed from a digital white noise or 'scramble' signal. The output of the EX-OR gate is thus inverted or non-inverted in a random manner and cannot readily be deciphered.

Both the scrambled message and the scramble signal are sent out (on separate lines) from the transmitter. At the receiver, the two signals are picked up and fed to the two inputs of a second EX-OR gate, where the digital analogue signal is restored (unscrambled) to its original form (the simple principle here is that if both gates are either inverted or non-inverted, the net effect will be an overall non-inversion of the signal). The restored digital signal is then converted back to analogue form by a D-to-A converter. Neat.

## More circuits

Figure 4 shows ways of using an EX-OR gate as a digital phase comparator and as a frequency doubler. The two circuits use the same basic principle of operation, so let's look at the phase comparator first. The comparator is meant to be fed with digital (ideally, square wave) signals that are identical in form and frequency but which may differ in relative phase. A digital signal is available directly at the output of the gate, or a dc signal may be available from an R-C low-pass output filter.

From the circuit waveforms, you can see that if both input signals are precisely in phase the two inputs will always be identical and the output will be zero. If, on the other hand, the two signals are not in phase, the output switches high at those points in the waveform where the two inputs are in opposite logic states. This situation occurs twice in each input cycle, so the output signal is frequency doubled. The pulse width of the output signal and thus the mean dc output levels of both the gate and the low-pass filter are directly proportional to the magnitude of the phase difference between the two input signals. The level is low with a small phase difference, rises to a maximum at 180° difference and then reduces again as the phase difference is shifted from 180° towards 360°.

From the above, it is easy to see how the Figure 4 frequency doubling circuit works. The digital input signal is fed directly to the 'A' input terminal of the EX-OR gate but is fed to the 'B' terminal through the phase-shifting network formed by R-C; the resulting phase-shift implements the frequency doubler action.

Figure 5 shows how a pair of EX-OR gates can be used to make a 1 kHz astable multivibrator or square wave generator. The circuit operates as a standard CMOS astable, the two gates being made to function as pulse inverters by taking one of their two inputs high.

Figure 6 shows how to modify the above circuit so that it functions as a gated 1 kHz astable circuit. Useful features of this design are that it uses a logic 1 (high) gate signal and its output goes to the logic 0 (zero) state when the astable is gated off.

## Magnitude comparators

We've already seen that the output of an EX-OR gate goes low if its two inputs are identical, or high if the inputs differ. The device can thus be used to compare a pair of digital bits, or a number of gates can be used to compare the magnitudes of a pair of multi-bit digital words. Figure 7 shows how a 4070B can be used to compare two four-bit words and give a high output if the two words are not identical. In Figure 7a, the

# Lab Notes

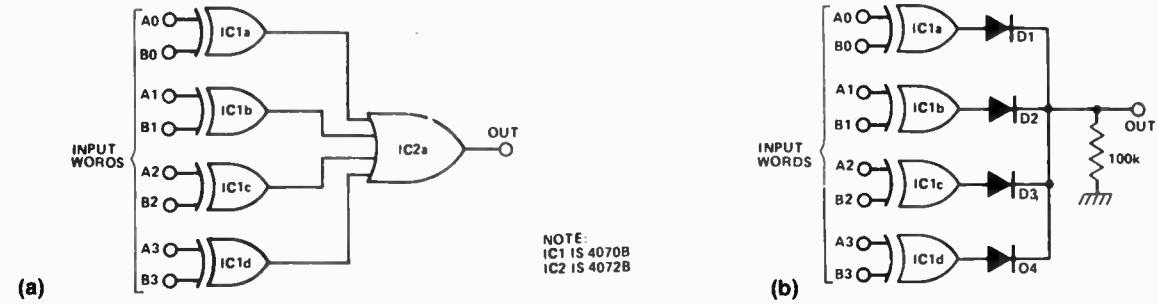



*Figure 7.* **Alternative ways of using a 4070B and a four-input OR gate to make a four-bit two-word comparator. The outputs go high if the two input words are not identical.**

| A | B | OUT |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

4077B TRUTH TABLE

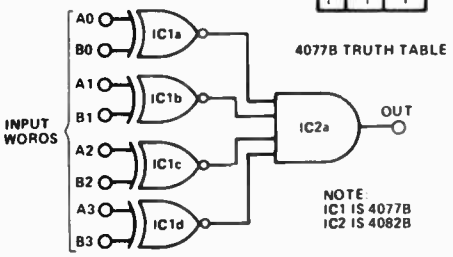



*Figure 8.* **Method of using 4077B EX-NOR gates to make a four-bit two-word comparator that gives a high output if the two input words are identical.**

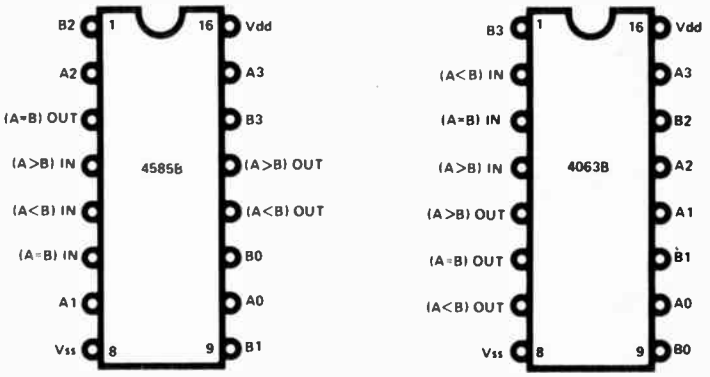



*Figure 9.* **The 4585B and the 4063B are four-bit magnitude comparator ICs.**

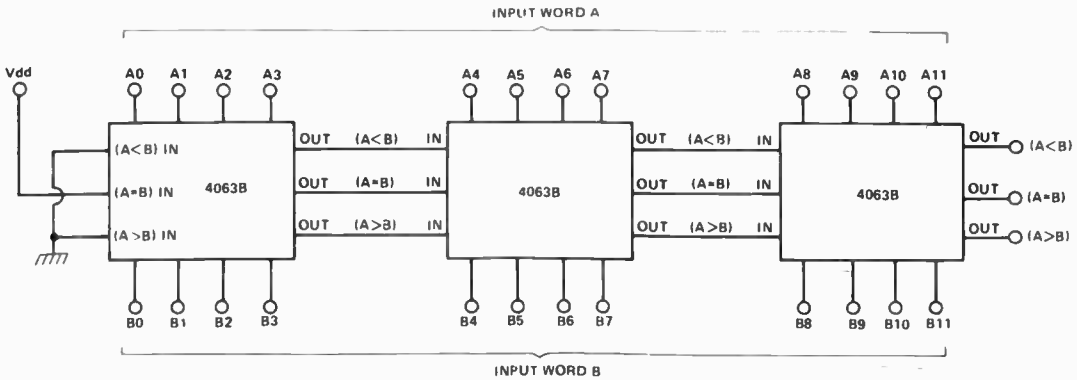



*Figure 10.* **Method of cascading three 4063Bs to make a 12-bit two-word comparator.**

outputs of the four EX-OR gates are ORed by one half of a 4072 dual four-input OR gate. In the Figure 7b circuit the outputs are ORed by a four-input diode gate.

An opposite action, in which the output goes high if the two words are identical, can be obtained by replacing the 4070B with a 4077B EX-NOR IC and ANDing the outputs by one half of 4082B, as shown in Figure 8. The 4077B has the same outline and pin notations as the 4070B.

The two magnitude comparator circuits described above are quite inexpensive and, clearly, are not particularly sophisticated. If a more sophisticated magnitude comparator performance is required, special chips such as the 4063B or 4585B four-bit magnitude comparators can be used. Figure 9 shows the outlines and pin notations of these two CMOS devices. Note that these chips have three outputs, one going high if the two words are identical, one if the 'A' word is greater than the 'B' word, and the remaining output going high if the 'A' word is less than the 'B' word. Obviously, only the one output can be high at any given time.

A useful feature of the 4063B and 4585B comparators is that they can readily be cascaded to compare words of any desired 'bit' length. Figure 10, for example, shows the basic connections for making a 12-bit comparator, using three cascaded ICs. When using these comparators, either singly or in cascade, note that the cascading inputs of the least significant comparator are connected as follows: (A<B) and (A>B) are biased low, and (A=B) is biased high. ●

# USING THE LM3900N

## Quad Norton Op-amp

THESE days it's nothing unusual to find four op-amps in a single integrated circuit package, but when the LM3900 was released by National Semiconductor in the mid-seventies very few linear devices were so closely-packed. The LM3900 contains four independent, internally compensated amplifiers in a single 14-pin dual-in-line encapsulation.

All four amplifiers are fabricated on a single silicon chip. Each amplifier contains seven transistors, a diode and a capacitor, whilst other internal components are used in the bias and power supplies.

The LM3900 has maintained its popularity over the years, partly because of its low cost (less than a dollar in 1982), but mainly because of its versatility and reliability.

### CONNECTIONS

The connections of the four separate amplifiers are shown in Fig.1. Each amplifier has a non-inverting input (marked +), an inverting input (marked −) and an output connection.

In addition, there is a single common positive supply connection and a common ground connection (negative supply line) for the whole device.

### INTERNAL CIRCUIT

Conventional high gain amplifiers employ a differential input stage to provide inverting and non-inverting inputs, but a rather different approach is employed in the LM3900N. A 'current mirror' is employed in the non-inverting input circuit, the current 'reflected' in this mirror being subtracted from that which enters the inverting input.

This type of amplifier therefore acts as a differential stage by amplifying the difference between two *currents* rather than the difference between two voltages (as in a conventional amplifier).

The type of amplifier used in the LM3900N may be referred to as a 'Norton' amplifier, since Norton is the name of the person who developed a theorem relating the *current* flowing in a circuit to the equivalent current generator and shunt impedance.

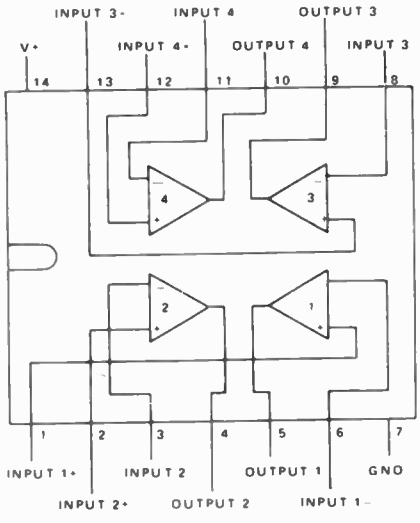



*Fig.1. The connections of the LM3900N.*

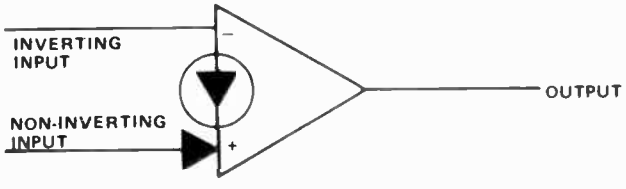



*Fig.2. The symbol for one of the Norton amplifiers of the LM3900N.*

### SYMBOL

The symbol recommended for each of the four Norton amplifier stages in the device is shown in Fig.2. This symbol distinguishes this type of amplifier from the standard operational amplifier symbol and avoids confusion in circuits.

The symbol of Fig. 2 contains an indication that there is a current source between the inverting and non-inverting inputs and implies that the amplifier uses a current mode of operation. In addition, the circuit symbol indicates that current is removed from the inverting input, whilst the arrow on the non-inverting input shows that this functions as a current input.

### PERFORMANCE

The LM3900N has the advantage that it can operate from a single supply voltage over the range of four volts to 36 volts. Most conventional operational amplifiers require supplies symmetrical with respect to ground (typically ± 15 V); the LM3900N can be used with such supply lines if desired.

The maximum peak to peak output amplitude of an LM3900N amplifier is only 1 V less than the supply voltage employed. The current consumed from the power supply is typically 6.2 mA (maximum 10 mA).

The typical voltage gain of each amplifier is 2800 or nearly 70 dB. The

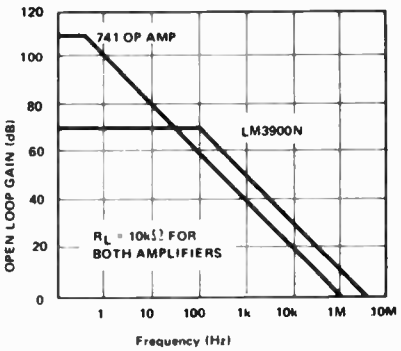



*Fig. 3. Comparison of the gain of the LM3900N with that of a 741 amplifier at various frequencies.*

minimum gain of any amplifier is 1200. The variation of this gain with frequency is compared with that of the well known type 741 operational amplifier in Fig. 3. It can be seen that the LM3900N amplifiers provide about 10 dB more gain at all frequencies above 1 kHz.

## APPLICATIONS

The Norton amplifiers used in the LM3900N device entail the use of somewhat different circuit design techniques than those used with conventional operational amplifiers.

The inverting input of the LM3900N amplifiers must be supplied with a steady biasing current. The current to the non-inverting input modulates that to the inverting input. The fact that current can pass between the input terminals leads to some unusual applications.

Both inputs of each of the amplifiers in the LM3900N are clamped by diodes so as to keep their potentials almost constant at one diode voltage drop (about 0.5 V) above the ground potential of pin 7. External input voltages must therefore be converted to input currents by placing series resistors in each input circuit.

## USE AS AN AC AMPLIFIER

The LM3900N forms a useful ac amplifier, since its output can be baised to any desired steady voltage within the range of the output voltage swing. The ac gain is independent of the biasing level and the single power supply required greatly simplifies circuit design.

A simple ac amplifier circuit is shown in Fig.4. The gain is approximately equal to R2/R1 or 10 with the circuit values shown. The mean potential at the output is half the supply voltage. The value of R3 should be twice that of R2 since the current passing through each of these two resistors is then the same. The positive supply and ground connections are not shown in Fig.4

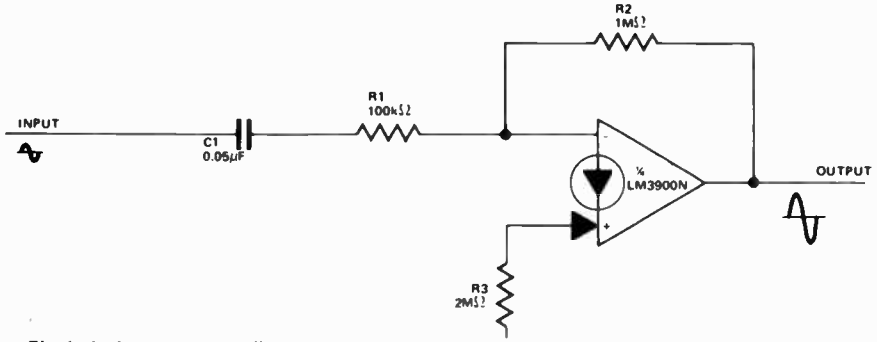



*Fig.4. A simple a.c. amplifier circuit.*

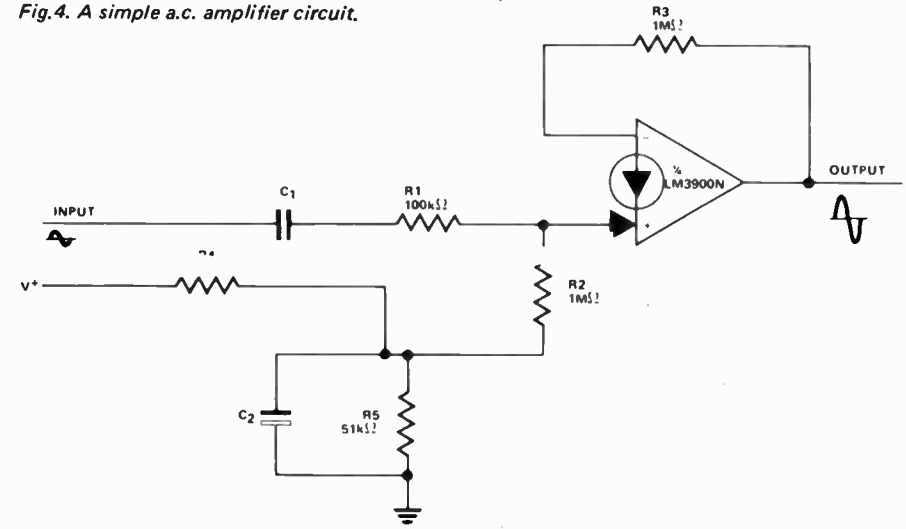



*Fig.5. A simple non-inverting a.c. amplifier.*

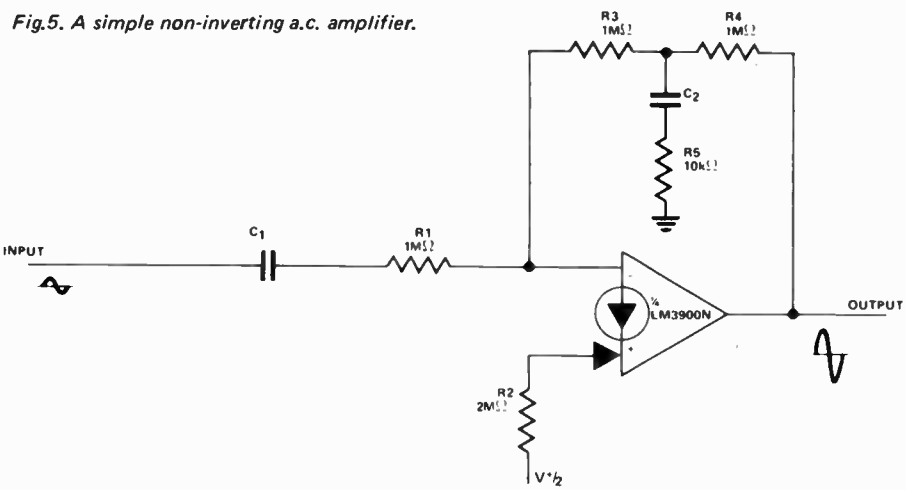



*Fig.6. An amplifier which has a high gain and a high input impedance.*

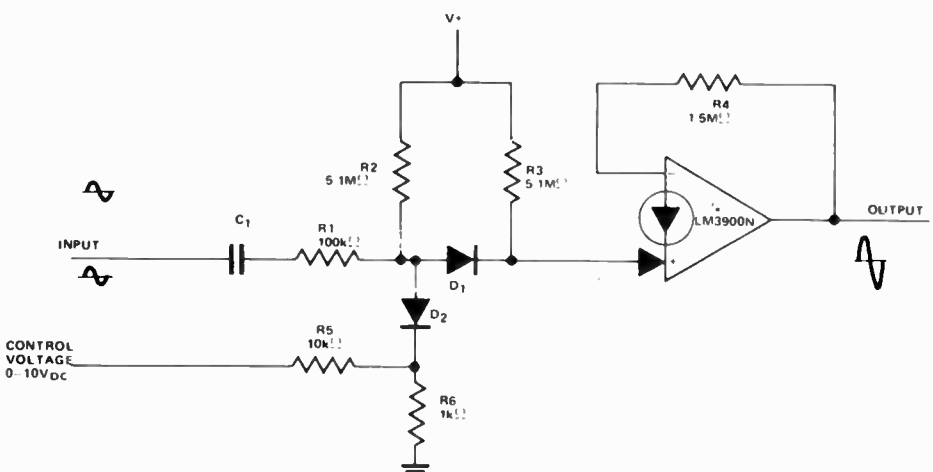



*Fig.7. An amplifier which has a gain controlled by an input voltage.*

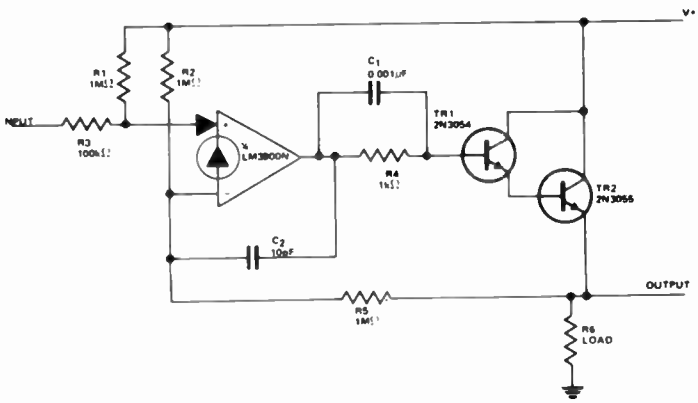



*Fig.8. A direct coupled power amplifier.*

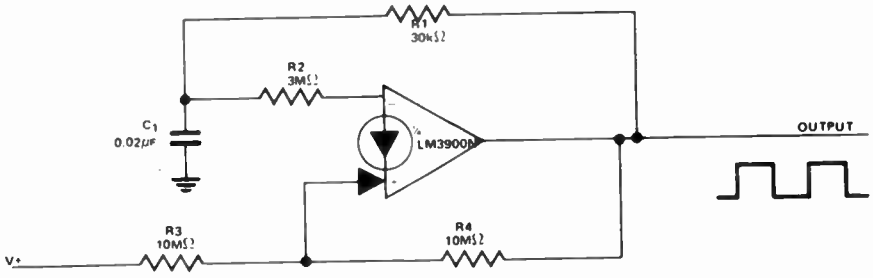



*Fig.9. A simple square-wave generator.*

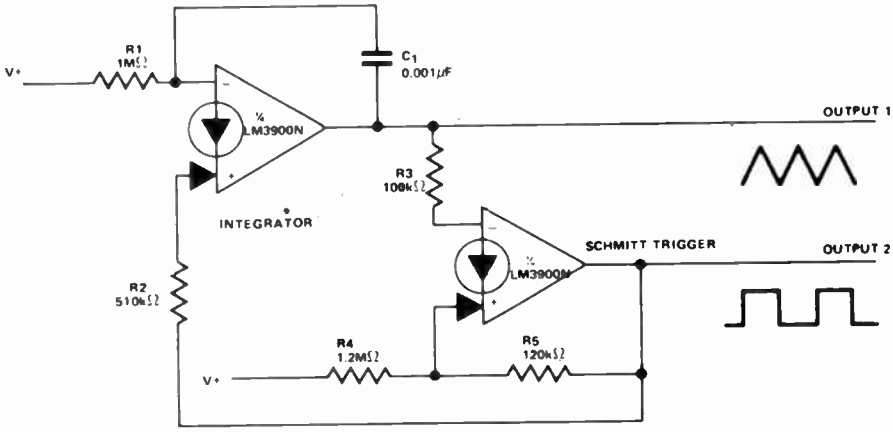



*Fig.10. A circuit for generating triangular and square-wave.*

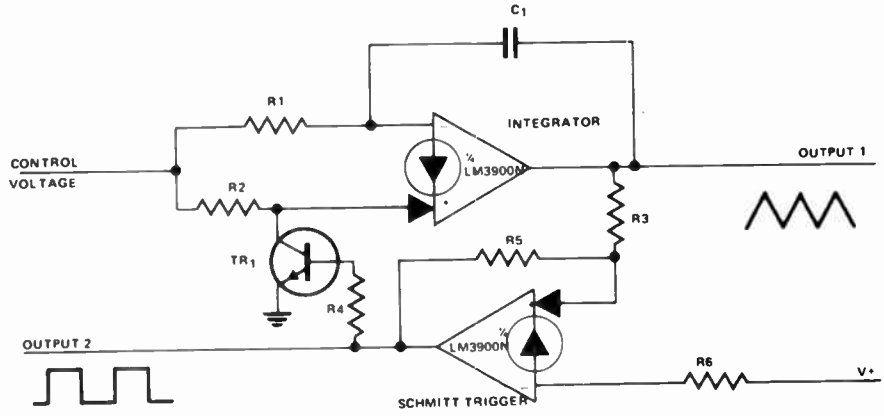



*Fig.11. A voltage controlled oscillator which produces triangular and square-waves.*

for simplicity, but $R_3$ should be returned to the same positive supply line as that used to feed pin 14.

The circuit of Fig. 4 provides a phase inverted output. Any ripple on the power supply line will appear on the output at half amplitude.

## NON-INVERTING AC AMPLIFIER

The circuit of Fig. 5 shows an amplifier which provides an output in phase with the input. The gain is equal to $R_3/(R_1 + r_d)$ where $r_d$ is the small signal impedance of the input diode. The value of $r_d$ is equal to 0.026 divided by the current passing through $R_2$ to the non-inverting input.

The capacitor values should be chosen so that the impedance of these components is considerably less than the circuit impedance at the points concerned.

## HIGH IMPEDANCE AND HIGH GAIN

The circuits of Figs. 4 and 5 have an input resistance, $R_1$ or 100 k ohm. If this resistor is increased to provide a higher input impedance, the gain of the circuit will fall. However, the circuit of Fig. 6 has been designed so that it provides both a high input impedance and a high gain using a simple amplifier. With the component values shown, the input impedance is one megohm and the gain 100.

The voltage applied to $R_2$ is made equal to the output voltage (which is half the supply voltage). The value of $R_2$ is equal to the sum of $R_3$ and $R_4$; these resistors set the dc bias. If desired, $R_2$ may be made four megohms and its lower end connected to the V+ supply.

Resistors $R_4$ and $R_5$ form a potential divider so that only 1/100 of the alternating output voltage is developed across the $C_2 - R_5$ circuit. This fraction of the output voltage is fed back to the inverting input via $R_3$. As $R_3$ and $R_1$ are equal, the gain is $R_4R_5$. As $R_5$ is decreased, the gain approaches the open loop gain of the amplifier.

## VOLTAGE CONTROLLED GAIN

An amplifier with a gain which can be controlled by the value of a steady applied voltage is shown in Fig. 7.

A current flows from the positive supply through $R_3$ to provide a bias which prevents the output of the amplifier from being driven to saturation as the control voltage is varied. When $D_2$ is non-conducting, the currents passing through both $R_2$ and $R_3$ enter the non-inverting input and the gain is of maximum. This occurs when the control voltage approaches 10 V.

The gain is a minimum when the control voltage is zero. In this case $D_2$ is conducting and only the current passing through $R_3$ enters the non-inverting input of the amplifier.

## DIRECT COUPLED POWER AMPLIFIER

In the circuit of Fig. 8, the output from an LM3900N amplifier is fed to a Darlington pair of power transistors. This circuit can deliver over three amps into a suitable load when the transistors are correctly mounted on heat sinks.

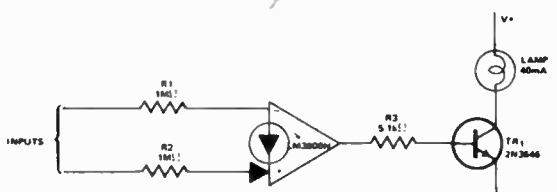


*Fig. 12. A voltage comparator with an indicator lamp.*

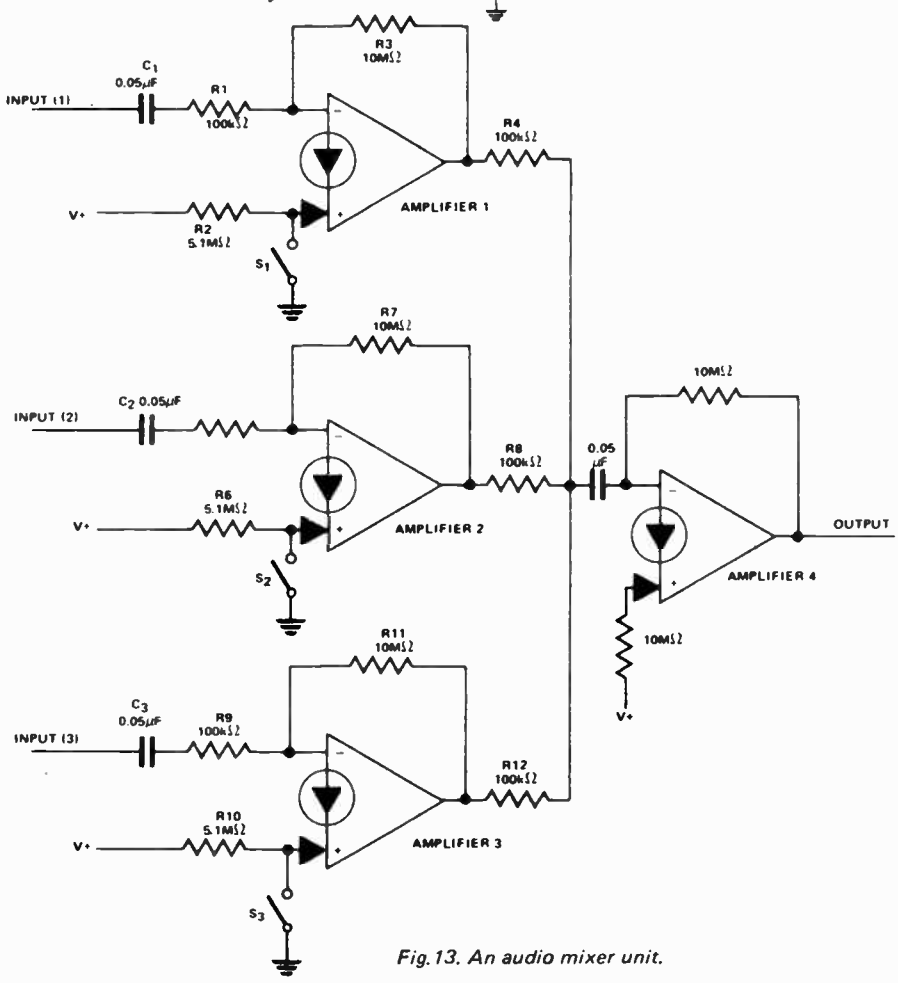



*Fig. 13. An audio mixer unit.*

## SQUAREWAVE GENERATOR

The multiple amplifiers in the LM3900N device are very suitable for use in waveform generators at frequencies of up to about 10 kHz. Voltage controlled oscillators (the frequency of which is dependent on an input voltage) can also be designed using the device.

A simple square wave generator is shown in Fig. 9. The capacitor $C_1$ alternately charges and discharges between voltage limits which are set by $R_2$ $R_3$ and $R_4$. The circuit is basically of the Schmitt trigger type, the voltages at which triggering occurs being approximately V+/3 and 2V+/3.

## TRIANGULAR WAVEFORM GENERATOR

A triangular waveform generator can be made by using one amplifier of a LM3900N device as an integrator and another amplifier as a Schmitt trigger circuit. A suitable circuit is shown in Fig. 10; it has the unusual advantage that only the one power supply is required.

When the output voltage from the Schmitt trigger circuit is low, the current flowing through $R_2$ is integrated by $C_1$ to produce the negative slope of the triangular wave at output 1. When the output 2 voltage from the Schmitt trigger is high, current flows through $R_2$ to produce the rising part of the waveform at output 1.

The output waveform will have good symmetry if $R_1 = 2R_2$. The output frequency is given by the equation:

$$f = \frac{V^+ - V_{BE}}{2R_1C_1V}$$

where $R_1 \cdot 2R_2$, $V_{BE}$ is the steady voltage at the inverting input (0.5 V) and V is the difference between the tripping points of the Schmitt trigger.

## VOLTAGE CONTROLLED OSCILLATOR

A simple voltage controlled oscillator circuit which produces both triangular and square wave outputs is shown in Fig. 11. As in Fig.10, one amplifier is employed as an integrator.

When the output of the Schmitt trigger is high, the clamp transistor $TR_1$ is conducting and the input current passing through $R_2$ is shunted to ground. The current passing through $R_1$ causes a falling ramp to be formed.

When the Schmitt circuit changes state, its output switches $TR_1$ to the non-conducting state. The current flowing through $R_2$ can be made twice that flowing through $R_1$ ($R_2 = R_1/2$) so that the rising part of the ramp has a similar slope to the negative part.

The greater the value of the control voltage in Fig.11, the greater the frequency of oscillation. However, the voltage must exceed the constant input voltage ($V_{BE}$) or the circuit will fail to oscillate.

## VOLTAGE COMPARATOR

The circuit of Fig. 12 shows how an LM3900N amplifier may be employed to compare two input voltages and to indicate the result by means of a small lamp. If the input voltage connected to the non-inverting input is appreciably more positive than the other input, the output of the amplifier will provide a positive voltage which renders $TR_2$ conducting. The lamp will then be illuminated.

One of the inputs may be a reference voltage so that one can then compare a single input voltage against this constant reference.

## AUDIO MIXER

The amplifiers of a LM3900N device can be conveniently used to make a mixer unit for audio purposes; the unit enables three separate audio signals to be mixed together to produce a composite output. The circuit shown in Fig. 13 provides this facility using only a single LM3900N device and also enables any one channel to be selected by switches. The currents passing through the resistors $R_4$ $R_8$ and $R_{12}$ are summed in the input circuit of the fourth amplifier.

If $S_1$ is open, amplifier 1 will be driven to saturation by the current passing through $R_2$. It will therefore be inactive.

## CONCLUSION

This short article has attempted to show a few of the numerous applications of this economical integrated circuit. Many more applications (such as phase locked loops, temperature sensing circuits, differentiators, tachometers, staircase generators, active filters, etc) are given in a report AN-72 produced by National Semiconductor.

# Lab Notes

# Transistor arrays

## — using the 3046/3056/3086 IC

**Peter Single**

Transistor arrays are a very useful electronic building block often overlooked by both hobbyists and professionals. This article describes a variety of circuits that can all be built using the 3046/3056/3086 — a common IC.

A transistor array consists of several transistors on the same piece of silicon. They are generally mounted in a 14- or 16-pin dual-in-line or T05 package. Because all the transistors are manufactured together, they are very well matched and because they are all on the same piece of silicon their thermal tracking is excellent.

Arrays may contain NPN transistors, 'super beta' NPNs, PNP transistors, zener diodes, transmission gates, SCRs and PUTs. The PNPs found in arrays are usually of inferior quality, having low $\beta$, low current handling capacity and poor frequency response. They are really only suitable for bias networks and similar low frequency applications.

### The substrate connection

All transistor arrays have a connection labelled 'substrate'. Often it is connected to the emitter at an NPN transistor, or it may simply be brought out to a pin on the IC. A cross section of two transistors in an array is shown in Figure 1. The substrate consists of P-type silicon which isolates the two transistors shown as long as the collector-to-substrate junctions remain reverse biased. This is achieved by connecting the substrate to the most negative part of the circuit.

Beware of tricks which use the collector-to-substrate diode. They are dangerous! Figure 2 shows why. The substrate forms a PNP transistor with the base of the NPN transistor, which generates a latch. This latch can be active unless the PNP transistor is held off by taking the substrate connection to the most negative part of the circuit. Remember, when designing with arrays, BEWARE THE SUBSTRATE CONNECTION!

Another point to watch is that if the power supply is connected the wrong way round the collector-to-substrate diode may be forward biased, which can often destroy the array.

An internal schematic and pin connection diagram for the 3086 is shown on page 63. A similar diagram is shown in the RCA Data Book, but with one significant error! *The substrate connection is pin 13 not pin 12.*

### Current mirrors

A very useful circuit configuration that is easily implemented with arrays is the current mirror. Figure 3 shows the basic circuit.

The collector current of a non-saturated transistor depends on the base-emitter voltage. If two identical transistors have identical base-emitter voltages their collector currents will be the same. In Figure 3, Q1 is diode connected and presents a low impedance to the input current. Transistor Q2, whose collector current mirrors that of Q1, is

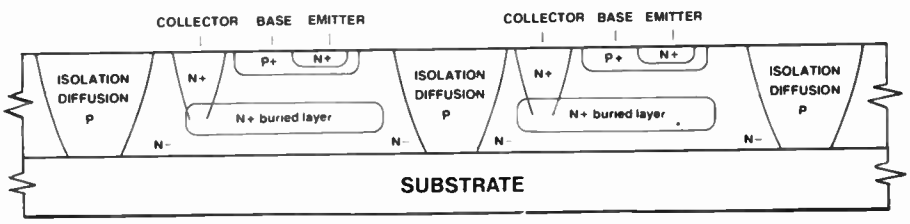



*Figure 1.* **Cross-section of two transistors in a transistor array IC.**

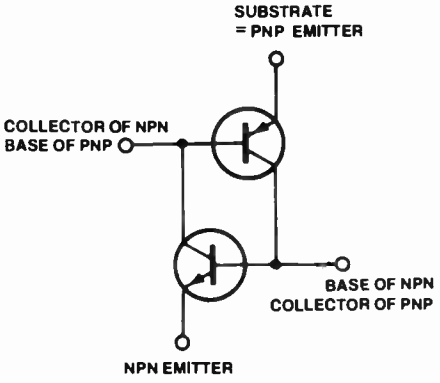



*Figure 2.* **Beware the collector-to-substrate diode!**

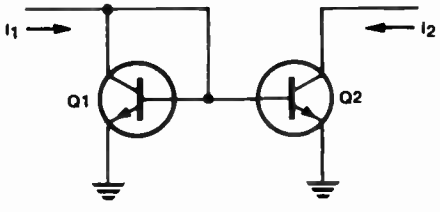



*Figure 3.* **Basic circuit of a current mirror. Connected like this, Q1 and Q2 on the array will have identical collector currents.**

# Lab Notes

## SELECTED DATA ON THE 3045/3046/3086 TRANSISTOR ARRAYS

### General Description

The 3045, 3046 and 3086 each consist of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the dc through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The 3045 is supplied in a 14-lead cavity dual-in-line package rated for operation over the full military temperature range. The 3046 and 3086 are electrically identical to the 3045 but are supplied in a 14-lead moulded dual-in-line package for applications requiring only a limited temperature range.

### features

- Two matched pairs of transistors
  $V_{BE}$ matched ±5 mV
  Input offset current 2μA max at $I_C$ = 1 mA
- Five general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure 3.2 dB typ at 1 kHz
- Full military temperature range (3045) −55°C to +125°C

### applications

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

### absolute maximum ratings ($T_A$ = 25°C)

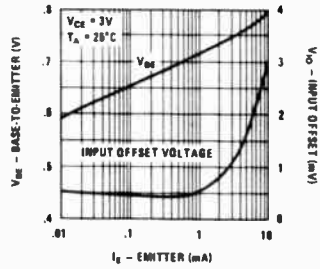
| | 3045 | | 3046/3086 | | |
|---|---|---|---|---|---|
| | Each Transistor | Total Package | Each Transistor | Total Package | Units |
| Power Dissipation: | | | | | |
| $T_A$ = 25°C | 300 | 750 | 300 | 750 | mW |
| $T_A$ = 25°C to 55°C | | | 300 | 750 | mW |
| $T_A$ > 55°C | | | Derate at 6.67 | | mW/°C |
| $T_A$ = 25°C to 75°C | 300 | 750 | | | mW |
| $T_A$ > 75°C | Derate at 8 | | | | mW/°C |
| Collector to Emitter Voltage, $V_{CEO}$ | 15 | | 15 | | V |
| Collector to Base Voltage, $V_{CBO}$ | 20 | | 20 | | V |
| Collector to Substrate Voltage, $V_{CIO}$ (Note 1) | 20 | | 20 | | V |
| Emitter to Base Voltage, $V_{EBO}$ | 5 | | 5 | | V |
| Collector Current, $I_C$ | 50 | | 50 | | mA |

### electrical characteristics ($T_A$ = 25°C unless otherwise specified)

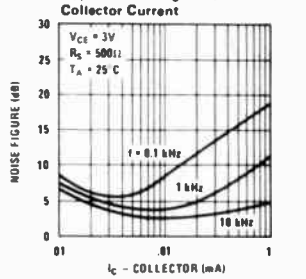
| PARAMETER | CONDITIONS | LIMITS 3045, 3046 MIN | LIMITS 3045, 3046 TYP | LIMITS 3045, 3046 MAX | LIMITS 3086 MIN | LIMITS 3086 TYP | LIMITS 3086 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Static Forward Current Transfer Ratio (Static Beta) ($h_{FE}$) | $V_{CE}$ = 3V, $I_C$ = 10 mA | 40 | 100 | | 40 | 100 | | |
| | $V_{CE}$ = 3V, $I_C$ = 1 mA | 40 | 100 | | 40 | 100 | | |
| | $V_{CE}$ = 3V, $I_C$ = 10 μA | | 54 | | | 54 | | |
| Input Offset Current for Matched Pair $Q_1$ and $Q_2$ ($\lvert I_{IO1} - I_{IO2} \rvert$) | $V_{CE}$ = 3V, $I_C$ = 1 mA | | 3 | 2 | | | | μA |
| Base to Emitter Voltage ($V_{BE}$) | $V_{CE}$ = 3V, $I_E$ = 1 mA | | 715 | | | 715 | | V |
| | $V_{CE}$ = 3V, $I_E$ = 10 mA | | 800 | | | 800 | | V |
| Magnitude of Input Offset Voltage for Differential Pair ($\lvert V_{BE1} - V_{BE2} \rvert$) | $V_{CE}$ = 3V, $I_C$ = 1 mA | | 45 | 5 | | | | mV |
| Magnitude of Input Offset Voltage for Isolated Transistors ($\lvert V_{BE3} - V_{BE4} \rvert$, $\lvert V_{BE4} - V_{BE5} \rvert$, $\lvert V_{BE5} - V_{BE3} \rvert$) | $V_{CE}$ = 3V, $I_C$ = 1 mA | | 45 | 5 | | | | mV |
| Temperature Coefficient of Base to Emitter Voltage $\left(\frac{\Delta V_{BE}}{\Delta T}\right)$ | $V_{CE}$ = 3V, $I_C$ = 1 mA | | −1.9 | | | −1.9 | | mV/°C |
| Collector to Emitter Saturation Voltage ($V_{CE(SAT)}$) | $I_B$ = 1 mA, $I_C$ = 10 mA | | 23 | | | 23 | | V |
| Temperature Coefficient of Input Offset Voltage $\left(\frac{\Delta V_{IO}}{\Delta T}\right)$ | $V_{CE}$ = 3V, $I_C$ = 1 mA | | 1.1 | | | | | μV/°C |

**Note 1:** The collector of each transistor of the 3045, 3046, and 3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

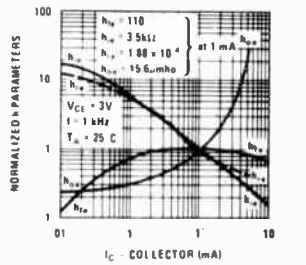
Typical Static Base To Emitter Voltage Characteristic and Input Offset Voltage for Differential Pair and Paired Isolated Transistors vs Emitter Current



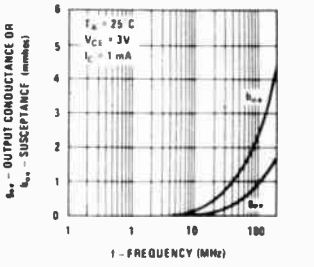

Typical Noise Figure vs Collector Current



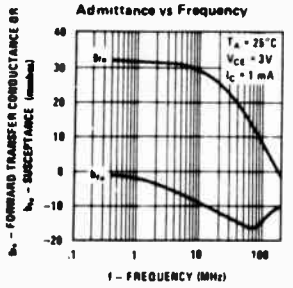

Typical Normalized Forward Current Transfer Ratio, Short Circuit Input Impedance, Open Circuit Output Impedance, and Open Circuit Reverse Voltage Transfer Ratio vs Collector Current



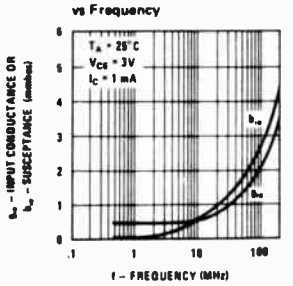

Typical Output Admittance vs Frequency



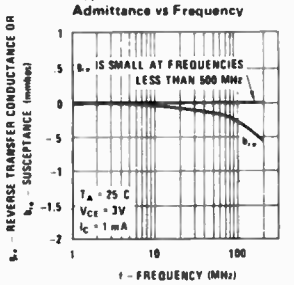

Typical Forward Transfer Admittance vs Frequency



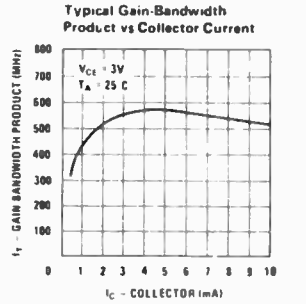

Typical Input Admittance vs Frequency




Typical Reverse Transfer Admittance vs Frequency




Typical Gain-Bandwidth Product vs Collector Current



connected as a dc-coupled common emitter amplifier and has a very high output impedance.

Current mirrors constructed from discrete components are not nearly as accurate because two discrete transistors chosen at random will rarely be identical. Also it requires extra construction to ensure that the transistors are held at the same temperature, because transistor characteristics are very temperature-dependent.

But two transistors on an array, having been manufactured side by side and being incorporated in the same piece of silicon, are very well matched. Errors in mirrors constructed using arrays are generally less than ten per cent.

A current mirror provides a regulated high impedance current sink. Its output will generally go to 200 mV from earth before the mirror transistor saturates, making it very useful for linear ramps, biasing networks and a host of other applications.

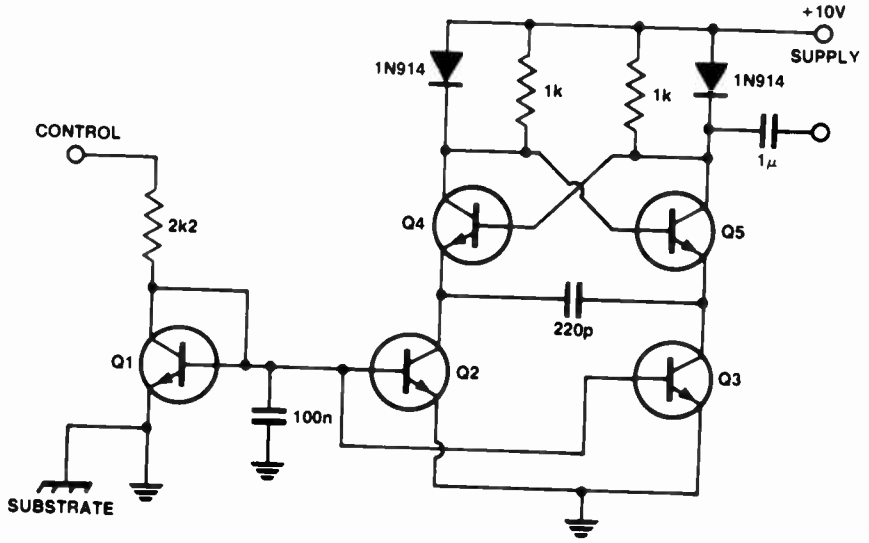



*Figure 4.* **Circuit of a voltage controlled oscillator. Transistors Q2 and Q3 in the array form a current mirror with Q1. The voltage at the 'control' input sets the collector currents of Q2 and Q3 which controls the oscillator frequency. Circuit oscillates around 10 MHz with 5 V on the control input.**

## Voltage controlled oscillator

A circuit for a voltage controlled oscillator is shown in Figure 4. It consists of a controlled bias system with Q2 and Q3 forming a current mirror with Q1. To understand the oscillator, imagine that Q5 is turned hard on. Transistor Q2 will slowly pull Q4's emitter low until Q4 starts to turn on. As it does so it will pull Q5's base low, turning Q5 off which turns Q4 harder on. This regenerative action continues until Q4 is fully on and Q5 off. Q3 then slowly starts to turn Q5 on and the process continues.

The rate of oscillation depends on the charging time of the capacitor between the collectors of Q2 and Q3. If the current through Q2 and Q3 decreases, the charging time increases and the oscillator frequency decreases. Because Q2 and Q3 mirror Q1, varying the current through Q1 will vary the oscillator frequency.

The circuit will oscillate at about 10 MHz with 5 V on the control pin. It can be made to run at 30 MHz by placing germanium diodes between collector and base of Q4 and Q5 and increasing the control voltage. The diodes should be inserted with their cathodes to the transistor bases to stop the transistors from saturating and storing charge in their bases. Such charge storage slows transistors down.

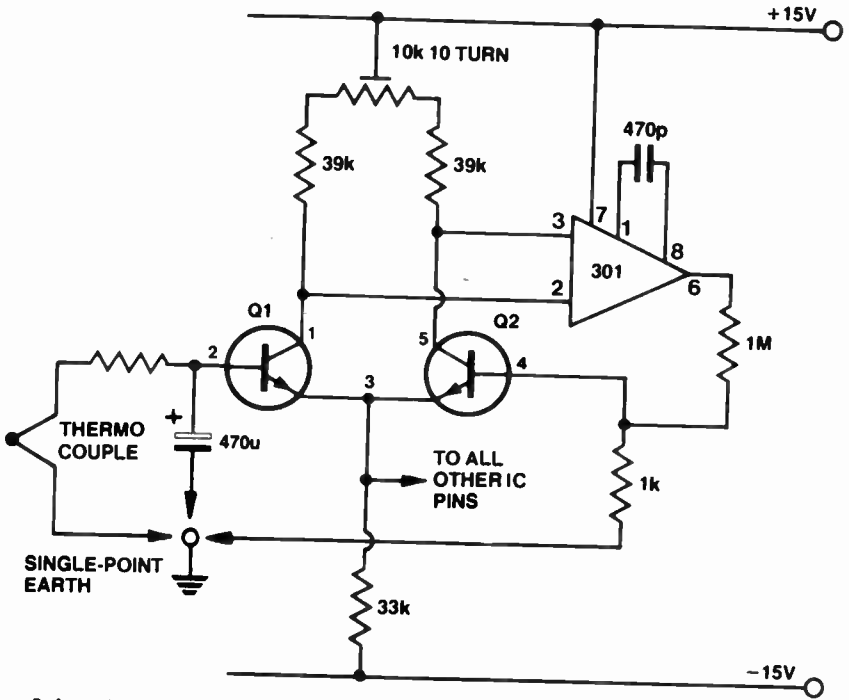



*Figure 5.* **A useful thermocouple amplifier. Input offset nulling is independant of temperature in this circuit, unlike many circuits.**

## Thermocouple amplifier

Figure 5 shows a circuit for an amplifier with a gain of 1000, suitable for use with thermocouples.

The biggest problem when using op-amps as thermocouple amplifiers is the temperature drift of the input offset voltage. Most methods of nulling the input offset are ineffective if the temperature varies. This circuit solves the problem by eliminating the input offset voltage

# Lab Notes

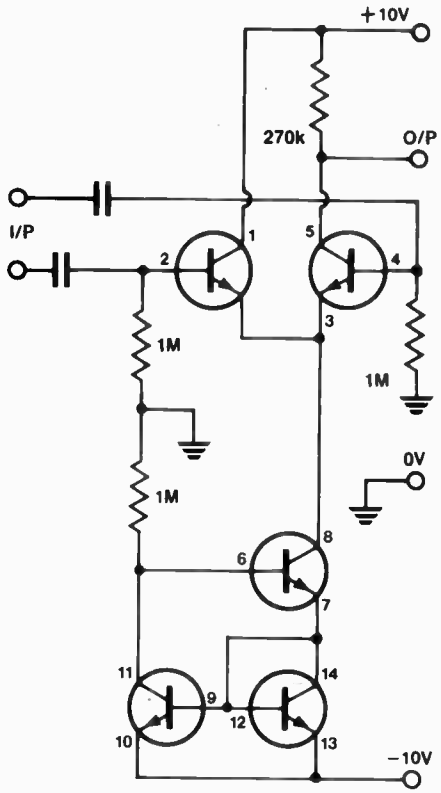



*Figure 6.* **This differential amplifier has a very high common mode rejection ratio (cmrr). Constant current source for the differential pair is a variation on the current mirror. Circuit is suitable for bio-electronic applications such as in a cardiac monitor or EMG.**

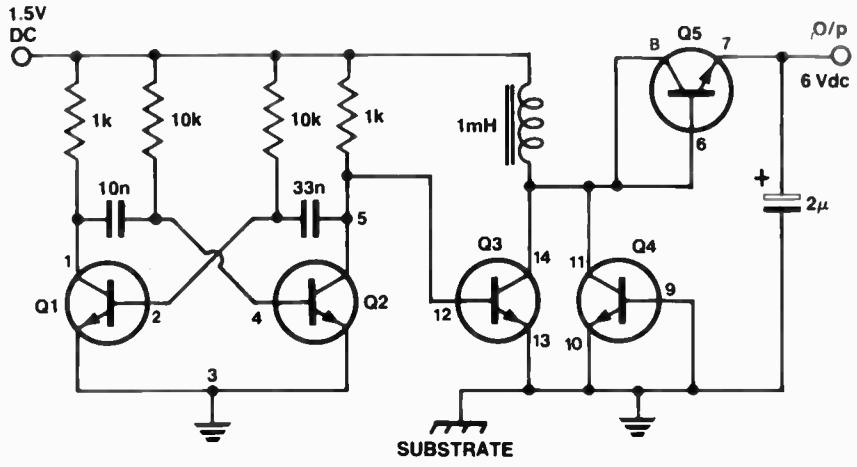



*Figure 7.* **This ringing choke inverter is just the thing for powering CMOS circuits from a single 1.5 V cell in portable applications. Operation is explained in the text.**

entirely. With a piece of wire replacing the thermocouple adjust the pot until the output of the amplifier is at 0 V. Since the bases of both Q1 and Q2 are at earth there is no input offset voltage.

This amplifier has very high open loop gain and will happily amplify any hum or other noise at its input. It will also oscillate through any capacitive coupling between output and input or between the supplies and the input. To avoid this, supplies should be well bypassed and earthing should be 'star' configured.

The substrate is not connected to the negative supply, because under extreme conditions the 20 V maximum collector-to-substrate voltage could be exceeded. However, no part of the array will ever go more negative than the substrate, so the circuit is quite safe.

The other transistors on the array should not be used as they may generate temperature gradients between Q1 and Q2.

## Differential amplifier

The circuit shown in Figure 6 has a very high common mode rejection ratio and is suitable for circuits such as cardiac monitors where the desired signal may be buried in a lot of common mode noise. It's a differential amplifier biased by a variation of a current mirror that has very high output impedance to improve the common mode rejection.

## Ringing choke inverter

This is a simple circuit, illustrated in figure 7, which generates about 6 V at 50 mA from a 1.5 V battery. It could be used to power CMOS from a single pen-light battery when a compact, portable circuit is required.

Transistors Q1 and Q2 form an astable multivibrator. When Q2 turns off, Q3 turns on and current flows through the inductor from the supply. The point 'A' on the waveform diagram (Figure 8) is the point where Q3 saturates. When Q2 turns on, cutting off Q3, the inductor tries to maintain the flow of current. Q5 is connected as a diode and current will flow through it until the voltage on Q4's emitter zeners the reverse biased junction. This is point 'B' on Figure 8.

When the inductor no longer has the energy to pump current into Q4 or Q5 it starts to oscillate (or ring) with its own parallel parasitic capacitance. This is point 'C' on Figure 8. The amplitude of

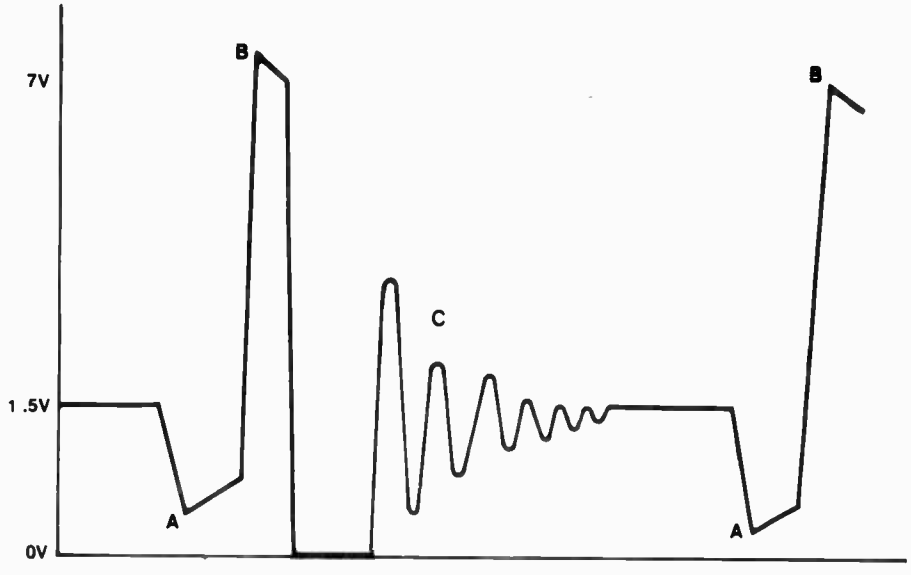



*Figure 8.* **Typical waveform at the collector of Q3 in the ringing choke inverter.**

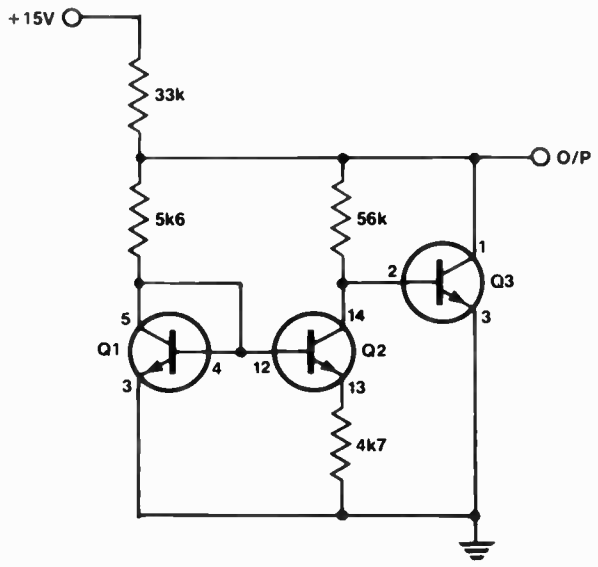



*Figure 9.* **Typical circuit of a 'band gap' voltage reference. This has excellent long term voltage and temperature stability. Output is 1.4 V, within 7 mV from 20°C to 100°C.**

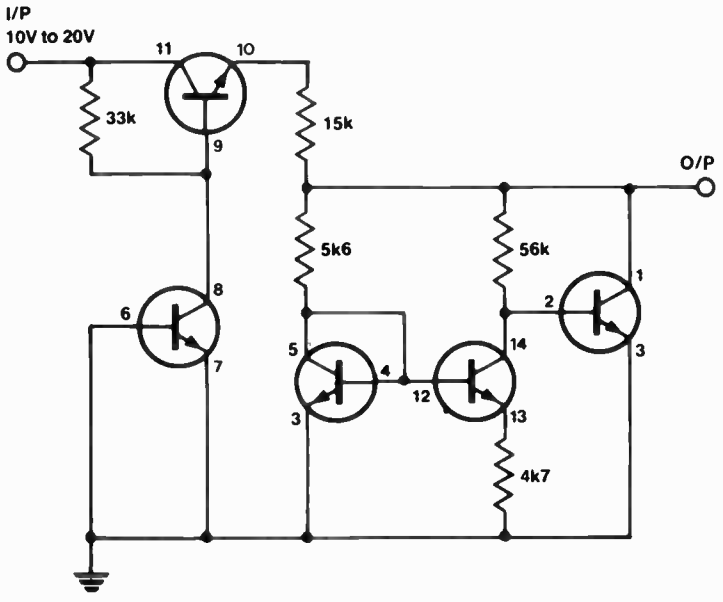



*Figure 10.* **Improved performance can be obtained from a band gap voltage reference by adding a pre-regulator. This employs one transistor in the array as a zener and the remaining transistor as a series regulator.**

the oscillation gradually decreases until Q3 is next turned on, restarting the whole process. The frequency of oscillation is a few kilohertz.

## Band gap reference

The band gap reference shown in Figure 9 is a voltage reference circuit with excellent temperature and long term stability. Its output is around 1.4 V and it may be used as a stable reference in 5 V systems.

The voltage generated on the emitter of Q2, being the difference between Q1's and Q2's base-emitter voltages, has a positive temperature coefficient. Since the current through Q2's emitter also flows through the 56k resistor, the voltage across this resistor also has a positive temperature coefficient. The base-emitter voltage of Q3 has a negative temperature coefficient. The values of resistors in the circuit have been chosen so that these temperature coefficients just cancel. My prototype varied by just 7 mV over the range from 20°C to 100°C.

To build a working band gap reference, high quality resistors must be used. Metal film types with 2% tolerance are best.

One problem encountered with this circuit is that its output varies slightly with the bias current through the 68k resistor. This can be overcome by providing the circuit with a pre-regulator, as shown in Figure 10. The pre-regulator uses the two remaining transistors on the array, one of which is connected as a zener diode.

If a high drive capability, or voltages greater than 1.4 V are required, then an op-amp or a non-inverting amplifier may be used as a follower. Figure 11 shows the connections. A 3140 op-amp makes an excellent follower as it may be operated from a single supply.

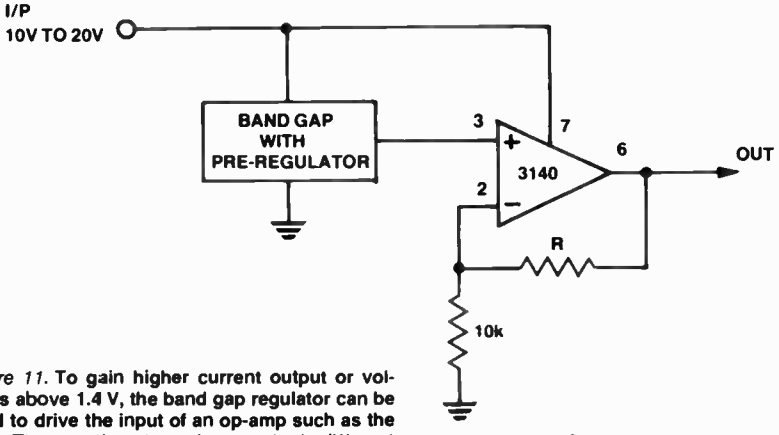
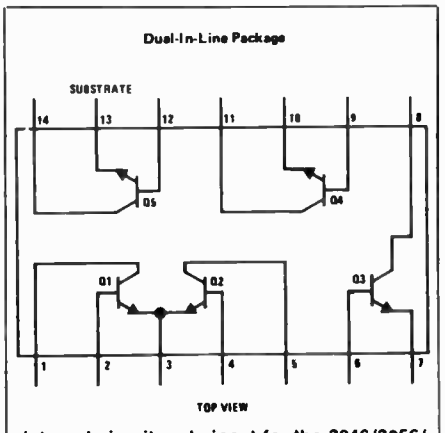



*Figure 11.* **To gain higher current output or voltages above 1.4 V, the band gap regulator can be used to drive the input of an op-amp such as the 3140. The equation shows how to obtain different outputs.**




**Internal circuit and pinout for the 3046/3056/3086.**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# Lab Notes

# Safety with CMOS

Certain elementary safety precautions must be taken when handling CMOS ICs or designing CMOS circuits. Ray Marston explains.

EARLY CMOS ICs earned a reputation for being easily damaged by static electricity, either when being handled or when being soldered into circuit boards, etc. Subsequently, manufacturers tried to overcome this 'fragility' problem by providing the ICs with extensive built-in input and output protection on each gate in each package. These protection networks do a fairly satisfactory job, but provide the designer with a few extra problems when employing CMOS circuits.

## CMOS protection networks

CMOS ICs are, by definition, metal-oxide semiconductor devices, in which the input signal is applied to the near-infinite impedance (about $10^{12}$ ohms) of the metal-oxide gate. Typically, the gate oxide has a breakdown voltage of about 80 V; if a gate oxide breakdown does occur, the resultant damage to the device is catastrophic and irreversible. To protect the CMOS against excessive input voltages (particularly arising from static energy), all modern CMOS ICs are provided with extensive built-in protection on all inputs and outputs.

Figure 1 shows the standard protection network that is used on the vast majority of B-series CMOS devices. Here, all diodes marked as 'D1' are used to prevent the input or output from swinging more than 600 mV below the $V_{SS}$ (0 V) rail, and all diodes marked as 'D2' are used to prevent the input or output from swinging more than 600 mV above the $V_{DD}$ (supply positive) rail. D3 is intended to prevent the $V_{DD}$ terminal from swinging negative to the $V_{SS}$ pin (electrostatically) when the device is being handled.

There are a couple of minor exceptions to the standard version of the protection network. One of these is the type used on the 4049B and 4050B series of hex buffer/converters which, as shown in Figure 2, have their inputs free to swing well above the $V_{DD}$ rail. These particular ICs are specifically intended for use in logic-level conversion applications, in which (for example) the input may come from a 12 V CMOS network but the output and the IC supply rail are matched to a 5 V TTL network.

Another exception is the 4066B type of transmission gate or bilateral switch, and its equivalents. These devices comprise a bilateral electronic switch and a switch-control network. In these circuits, all switch-control networks have the type of input protection shown in Figure 1, but the switches themselves have the simple protection network shown in Figure 3.

Note in Figures 1-3 that all diodes marked with asterisks are 'parasitic' devices, which just happen to occur fortuitously as an inherent part of the CMOS manufacturing process, while all other diodes are specifically designed into the circuits. Also note that the networks are intended only to give protection against 'normal' electrostatic discharge voltages. When the networks are subjected to ordinary dc signals, the diodes are liable to burn out if their forward currents exceed 10 mA or so, thereby causing possible catastrophic damage to the IC substrate.

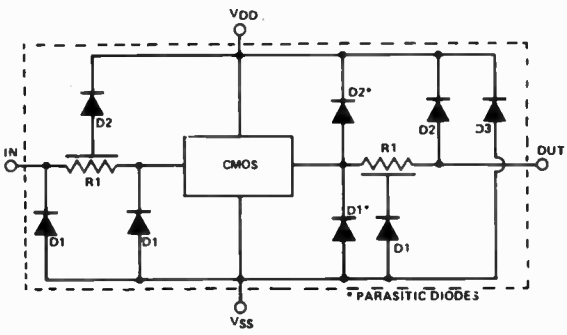



*Figure 1.* **These are the standard electrostatic discharge protection networks used on most B-series CMOS ICs. The two diodes associated with the resistors are distributed across the entire resistance, as shown.**

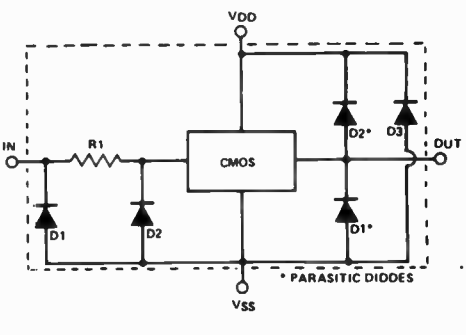



*Figure 2.* **This protection network is used on the 4049B and 4050B hex buffers. Note that the input is free to swing above the positive supply ($V_{DD}$) rail.**

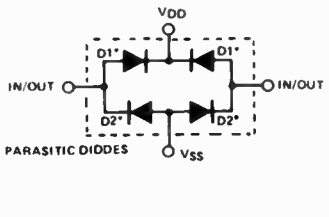



*Figure 3.* **The 4066B quad bilateral switch has standard B-series protection on its gate control input terminals, but has this simplified form of protection on its 'switch' elements.**

# Lab Notes

Major CMOS manufacturers such as RCA reckon that an electrostatically charged human body can be approximated by the circuit of Figure 4, in which the 'body' has an effective capacitance of 100 pF and a source resistance of 560R. The manufacturers have carried out extensive tests with this model by charging the 'body' to various

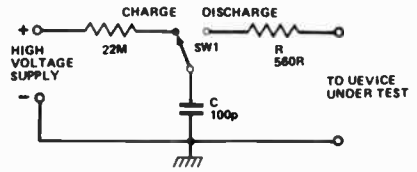



*Figure 4.* **Manufacturers use this equivalent-body discharge network when evaluating the capabilities of their CMOS protection networks.**

voltages and then discharging it (via the 560R series resistor) into different terminal combinations (input, output, $V_{SS}$, $V_{DD}$) of CMOS devices to establish worst-case capability figures for the three types of electrostatic-discharge protection networks. It should be noted in these tests that the 560R series resistor acts as a current-limiting voltage dropper, so the voltage actually reaching the CMOS device is far lower than the initial electrostatic voltage.

The results of the manufacturer's protection capability tests are shown in Figure 5. As you can see, the standard protection network can withstand a 4 kV electrostatic discharge. A quick calculation shows, however, that this represents a peak protection-diode current of several amps, yet we've already seen that these diodes can withstand dc currents of only 10 mA or so. Puzzled?

| PROTECTION NETWORK | WORST – CASE CAPABILITY |
|---|---|
| STANDARD B-SERIES 4049B AND 4050B 4066B BILATERAL SWITCH | 4 kV 1 kV TO 2 kV < 800 V |

*Figure 5.* **These are the worst-case capabilities of the three different CMOS protection networks, when tested with the network of Figure 4.**

## Up the junction

Just about the only way of destroying a diode is to literally vaporise its junction, and this can only be done by applying an adequate amount of power for sufficient time for the melting process to take place. Since a junction must inevitably be formed on a substrate, which has a finite mass, all junctions inevitably have a certain amount of thermal inertia and are, in fact, destroyed by energy overloads (power-time product), rather than by simple power overloads.

Consequently, it is quite normal to find that a diode rated at 1 A (for example) can, in fact, withstand brief current surges up to several hundred amps. Similarly, CMOS protection diodes, which have very low dc current ratings (10 mA), can withstand very high levels of surge current (several amps), provided that the surge current

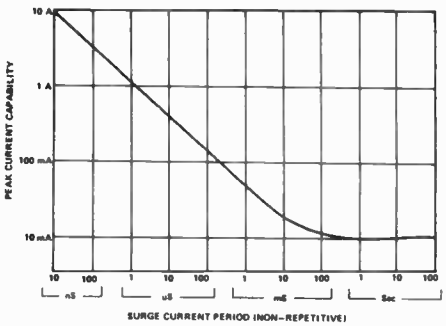



*Figure 6.* **Typical surge-current capabilities of CMOS protection diodes.**

duration is very brief. Figure 6 shows the typical surge current capabilities of these protection diodes. Remembering that the 100p — 560R 'human body' equivalent circuit has a time constant of a mere 56 nS, it no longer comes as a surprise to note that these diodes can withstand several amps of peak current from a 4 kV discharge!

## CMOS circuit design

By now you will have gathered that you can effectively destroy a CMOS device by simply blowing one or more of its 'protection' diodes with a dc current as low as 10 mA. Consequently, when designing CMOS circuits, precautions must be taken to ensure that excessive diode current cannot flow in the CMOS chips.

CMOS ICs can be 'blown' by excessive signals applied to either the input or the output terminals. If several CMOS stages are cascaded, empirical experience shows that a front-end 'blow' will usually destroy only a single device (because low energy levels are normally involved), but a rear-end (output) 'blow' will often have a ripple effect (because high energy levels are involved) and cause the destruction of all ICs in the chain.

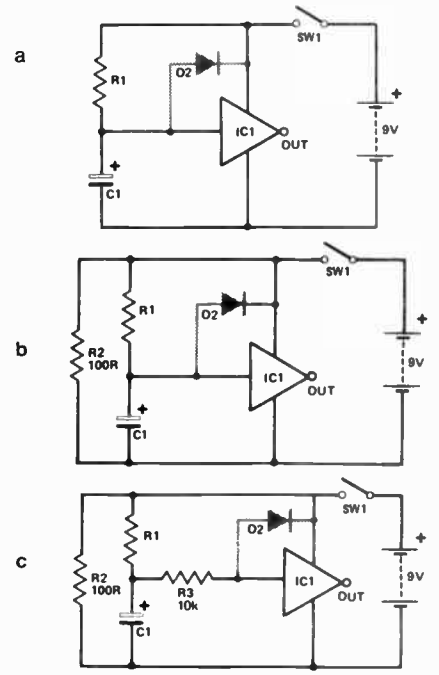



*Figure 7.* **Circuits (a) and (c) are safe, but circuit (b) will almost certainly cause front-end 'blow'. See text for explanation.**

The most common cause of front-end 'blow', and its cure, are illustrated in Figure 7. Here, a capacitor is connected directly between the IC gate and the 0 V line; when SW1 is closed, the capacitor charges up via R1 and eventually attains the full positive supply potential. When SW1 is opened (to switch the circuit off), C1 tries to discharge via D2, the 'upper' input protection diode of the gate.

In the Figure 7a circuit, the only discharge path for C1 is via D2 and the IC's supply terminals; consequently the discharge currents will be quite low and the IC will probably suffer no damage. In Figure 7b, on the other hand, a 100R resistor is connected across the supply terminals, so C1 will try to discharge to ground via D2 and R2, and the resulting 90 mA peak current will almost certain-

ly result in the destruction of the chip. In practice, R2 may well take the form of various resistors and semiconductor devices distributed throughout the total circuit.

Figure 7c shows the cure for the Figure 7b design problem, a 10k resistor wired in series with the gate to limit the C1 discharge currents to a safe value. Whenever you design CMOS circuits and have to connect a capacitor between a gate and the 0 V rail, always make sure that the capacitor discharge current is limited to a safe value, either by a series gate resistor or by some other factor.

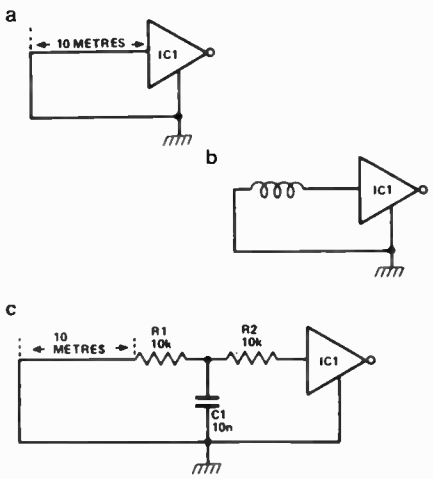



*Figure 8.* **Long input cables, as in (a), can be equivalent to an inductor (b), and present another front-end blowing hazard. The cure is simple (c).**

Figure 8 illustrates another possible cause of front-end 'blowing', and its cure. In Figure 8a, it seems that the IC's input is safely grounded by the 10 m of input cable (in practice, this cable may go to a low impedance sensor, etc), but in actual fact (Figure 8b) this cable will inevitably be inductive and can easily pick up unwanted radiation and possibly feed destructive signals to the IC input. Figure 8c shows that the circuit can be rendered safe with a simple filter (R1-C1) and a series gate resistor (R2).

## Back-end blowing

The most common cause of back-end blowing is unexpected back-EMFs (from inductive loads) reaching the CMOS output by breaking through from power-driving circuitry.

Inductive loads, such as relays, can generate surprisingly large back EMFs as their fields collapse at switch-off, as can be proved by connecting a relay in the 'buzzer' mode shown in Figure 9. Typically, a 12 V relay will generate a back-EMF of about 300 V! If you ever use CMOS to switch a relay or other highly inductive load using a transistor driver, always protect the transistor with a pair of 1N4001 diodes connected as shown in Figure 10a. If you want to be really safe, you can use another pair of similarly connected diodes to directly protect the output of the CMOS stage, as shown in Figure 10b. ●

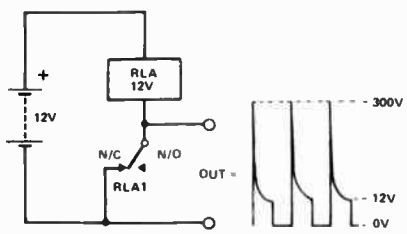



*Figure 9.* **This 'buzzer' circuit can be used to check the magnitude of the back-EMF from a relay. 300 V is typical!**

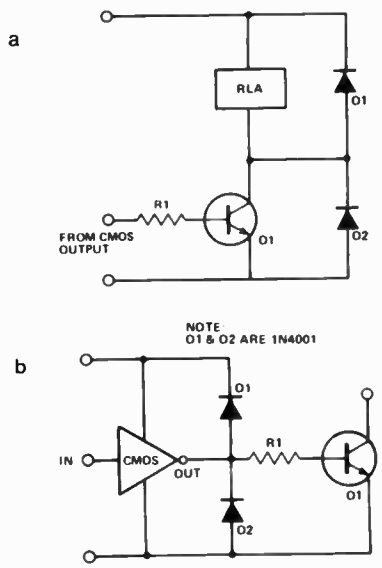



*Figure 10(a).* **A transistor relay-driver can be protected with a pair of diodes. (b) The output of a CMOS stage can be given added protection with a similar arrangement.**

# Lab Notes

# Walking rings . . . and other miracles

A common task facing the electronics designer is that of producing simple digital counter/divider networks which produce an output frequency or count rate that is some fixed fraction of an input frequency or count rate. Here's how to do it.

**Ray Marston**

DIGITAL DIVISION, or counting, is a fairly straightforward task – providing you know how (!), chiefly involving the manipulation of circuit 'blocks' to economically or conveniently do the task required. But, as the old saying goes, there's more than one way to skin a cat . . .*

## 4013 and 4027 flip-flops

The two most basic counter/divider ICs in the CMOS range are the 4013 dual D-type flip-flop and the 4027 dual J-K flip-flop. Figure 1 shows the outlines and pin notations of these two devices, which each contain two independent flip-flop stages sharing common supply connections. Each of these packages can be used to give division ratios or 2, 3 or 4.

A single 4013 'D' stage can be made to act as a divide-by-two counter by grounding its SET and RESET pins and coupling its DATA pin to its $\overline{Q}$ output, as shown in Figure 2a. A single 4027 J-K stage can be made to act as a divide-by-two counter by grounding its SET and RESET pins and connecting its J and K pins to the positive supply rail, as shown in Figure 2b. Both of these circuits change state on the positive-going transition of the input clock signal, which must have rise and fall times of less than 5 us. The 4013 is very fussy about the shape of its input clock signals and tends to be rather temperamental in operation. The 4027 is not too fussy about its clock signals and is very easy to work with.

## Ripple counters

Figure 3 shows how two divide-by-two 'D' or J-K flip-flop stages can be wired in series to give and overall division ratio of four ($2^2$). Figure 4 shows how three

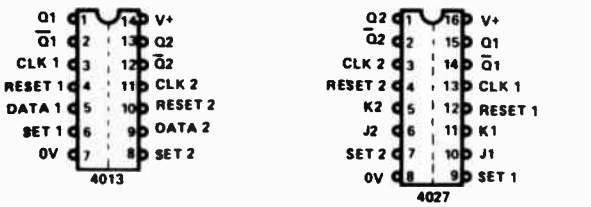



*Figure 1.* Outlines and pin notations for the versatile 4013 dual-D and 4027 dual J-K CMOS flip-flop ICs.

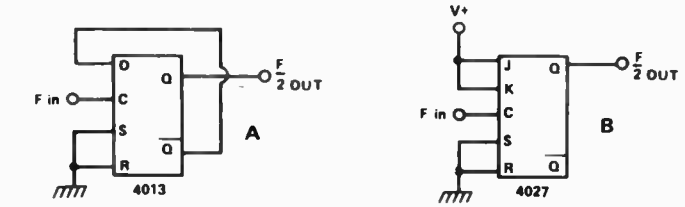



*Figure 2.* Divide-by-two counters made from D-type (left) and J-K (right) flip-flops.

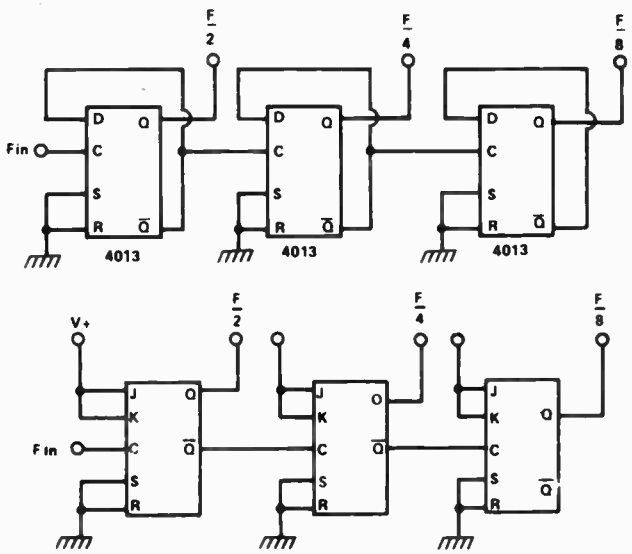



*Figure 4.* Two versions of a divide-by-eight ripple counter using D-type (top) and J-K (bottom) flip-flops.

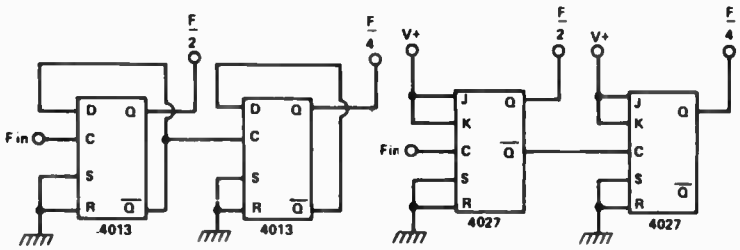



*Figure 3.* D-type and J-K versions of a divide- by-four ripple counter

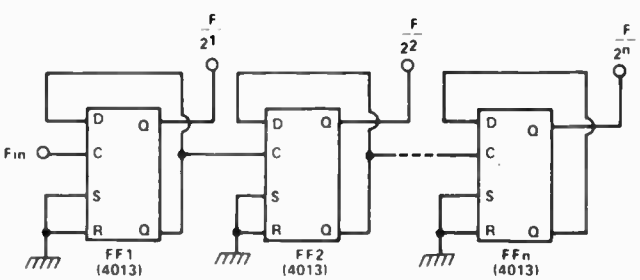



*Figure 5.* How a chain of D-type flip-flops can be linked to provide a divide-by-2 ripple counter.



*(Uh, sorry . . . no offence to cat lovers)

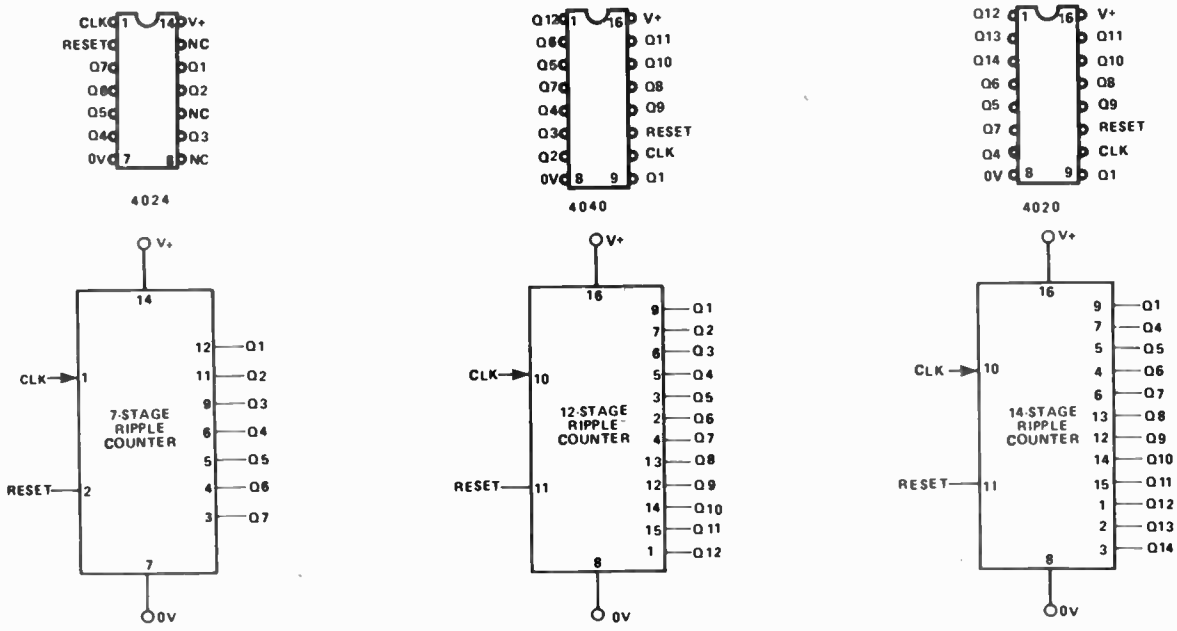



*Figure 6.* **Outlines (above) and functional diagrams (below) of three popular CMOS multi-stage ripple counter ICs.**

such stages can be wired in series to give a division ratio of eight ($2^3$). Note that each counter stage is clocked at precisely half the rate (an octave below) of the preceeding stage, so that the clock signal seems to 'ripple' through the counter chain. Also note that, as is made clear in Figure 5, the final division ratio is equal to $2^n$ where 'n' is the number of counter stages. Thus, four stages give a ratio of $2^4 = 16$, five stages give $2^5 = 32$, six give $2^6 = 64$, seven = 128 and so on.

A detail not made clear in the above diagram is that, since the counters of a 'ripple' circuit are effectively wired in series, the propogation delays of the individual stages in the counting chain add together to give a fairly long total delay at the end of the chain. If each stage has a delay or 100 ns and there are ten stages, the total propagation delay is 1 us. Consequently, the first output signal will not change state until 1 us after the arrival of the original input clock signal that initiates that change of state. The counter states of the 'ripple' type of counter are thus not in perfect synchrony with the original clock signal and this type of circuit is consequently known as an asynchronous counter.

The 4013 and 4027 counters can be cascaded to give any desired number of ripple stages. When more than two stages are required it is usually economic, however, to use a special-purpose MSI ripple-carry binary counter/divider IC. Figure 6 shows the outlines and functional diagrams of three popular ICs of this type.

The 4024 is a seven-stage ripple unit with all seven outputs externally accessible. It gives a maximum division ratio of 4096. The 4020 is a fourteen-stage unit with all outputs except 2 and 3 externally accessible; and it gives a maximum division ratio of 16 384.

Figure 7 shows the outline and functional diagram of a special-purpose ripple-carry unit, the 4060. This is another fourteen-stage unit, but does not have outputs 1, 2, 3 or 11 externally accessible. The special feature or the 4060 is that it incorporates a built-in clock oscillator circuit. The diagram shows the connections for using the internal circuit as either a crystal or an RC oscillator.

The 4020, 4024, 4040 and 4060 ICs

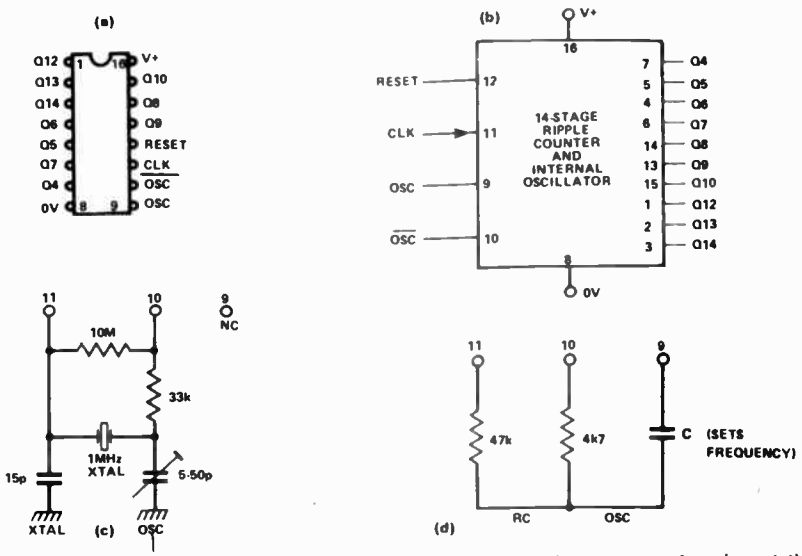



*Figure 7.* **Outline (a), functional diagram (b) and alternative oscillator connections (c and d) for the 4060 fourteen-stage ripple counter.**

# Lab Notes

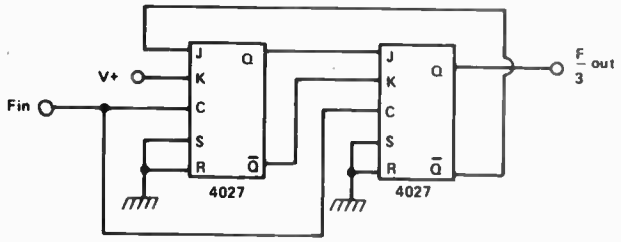



*Figure 8.* **A divide-by-three 'walking ring' or 'Johnson' counter using J-K flip-flops.**

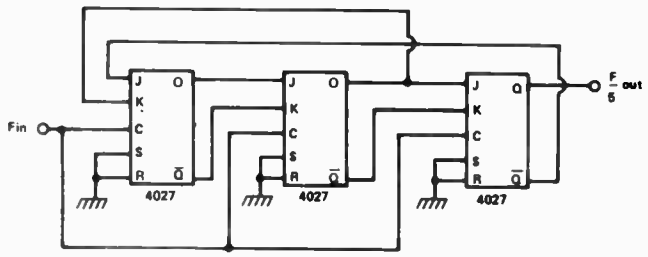



*Figure 9.* **A divide-by-five Johnson counter using J-K blocks.**

are all provided with Schmitt trigger action on their input terminals and trigger on the negative transition of each input pulse. All counters can be set to zero by applying a high level on the RESET line.

## 'Walking ring' or 'Johnson' counters

'Walking Ring' or 'Johnson' Counters An alternative to the ripple type of counter is the so-called 'walking ring' or 'Johnson' counter. In these counters, all stages are clocked in parallel and the stages are cross-coupled so that the response of one stage to a clock pulse depends on the states of the other stages.

Figure 8 shows the connections for making a divide-by-three counter from two J-K stages and Figure 9 shows the connections for making a divide-by-five counter.

A major advantage of the 'walking ring' or 'Johnson' counter is that, since all stages are clocked in parallel, the outputs of the completed counter are subjected to only a single stage or propogation delay. Consequently, the system gives synchronous operation and outputs give glitch-free decoding.

## 4018 divide-by-n counter

When count numbers greater than four are required, it is economic to use MSI ICs such as the 4018, rather than the 4013 or 4027. The 4018 is a five-stage 'Johnson' counter that can be made to divide by 2, 3, 4, 5, 6, 7, 8, 9 or 10 by merely cross-coupling its terminals in suitable ways. The IC features a Schmitt trigger on its clock input line and clocks on the positive transition of the input signal.

Figure 10 shows the outline and functional diagram of the 4018. Figure 11 gives methods of cross-coupling the IC to give division ratios from two to ten. On even division ratios, no additional components are needed. On odd ratios, a two-input AND gate is required in the feedback network. This gate can be a single 4081 AND stage, or can be made from two 4011 NAND stages.

## Greater-than-10 division

Even division ratios greater than ten can usually be obtained by simply cascading suitably scaled counter stages, as shown in Figure 12. Thus, a divide-by-two and a divide-by-six stage give a ratio of twelve, a divide-by-six and a divide-by-six give a ratio of 36 and so on.

Non-standard and uneven division ratios are obtained by using standard counters, such as the 4018, and decoding their outputs to generate suitable counter-reset pulses on completion of the desired count. ●

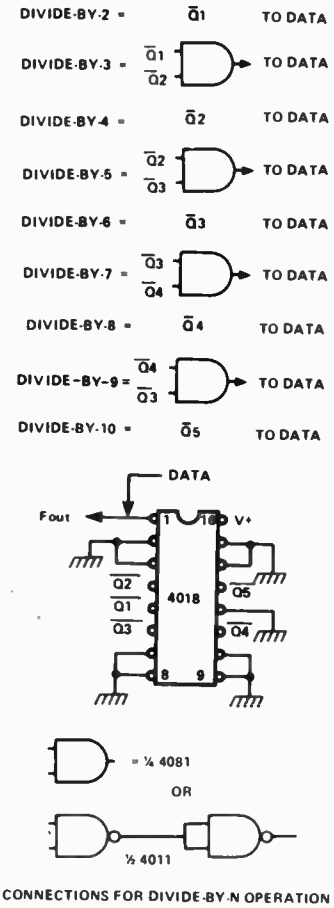



*Figure 11.* **Methods of connecting the 4018 for divide-by-two to divide-by-ten operation.**

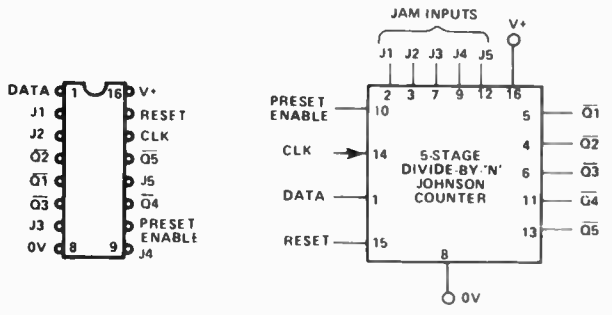



*Figure 10.* **Outline and functional diagram of the 4018 presettable divide-by-n counter.**

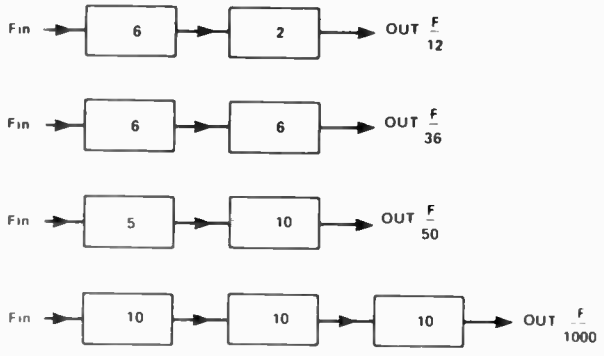



*Figure 12.* **Typical examples of division by numbers greater than ten.**

# Six-range FET dc voltmeter has 11M input impedance

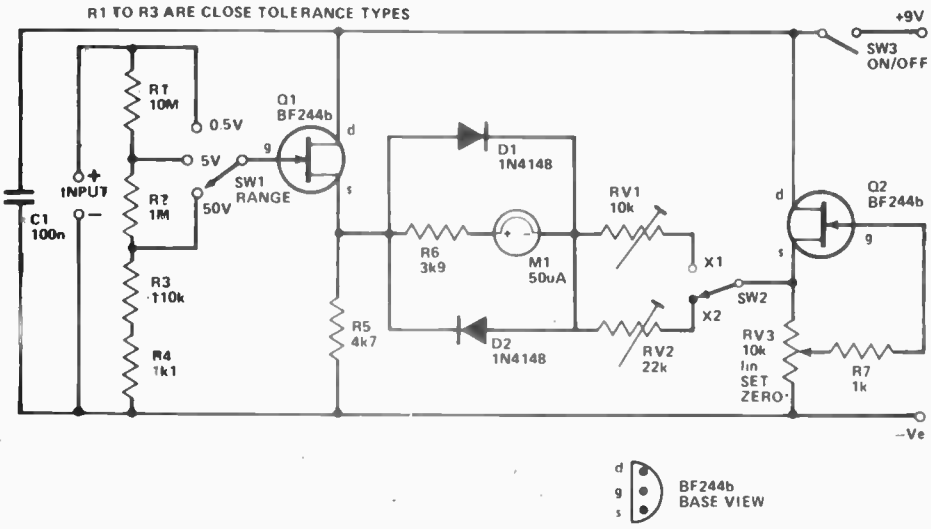
This circuit can be made as a handy add-on unit for a multimeter or as a stand-alone test instrument.

ALTHOUGH an ordinary multimeter is suitable for most dc voltage measurements, it can occasionally prove to be inadequate — usually just when you need it most! This is the case when making measurements on high impedance circuits which cannot supply the input current required to operate even a very sensitive moving coil meter of the type normally employed in a multimeter. The loading effect of the meter then causes the voltage at the test point to fall substantially, resulting in a misleading reading.

The problem is overcome by this FET voltmeter circuit which has six ranges, from 0.5 V (500 mV) to 100 volts full scale deflection (FSD). The circuit features an input impedance of a little over 11M on all ranges. This provides a sensitivity of more than 22M/volt on the half-volt (lowest) range, falling to a little over 110k/volt on the 100 V range. Most common multimeters have a sensitivity of 20k/volt, good quality types 50k/V and top-line models 100k/V, so this unit should compare quite favourably by the time you want to measure high voltages.

The high input impedance is achieved by using Q1 as a unity voltage gain buffer (source-follower). The FET has an inherently high input impedance. The actual input impedance is really set by the value of the series combination of the input attenuator consisting of resistors R1, R2, R3 and R4.

A simple voltmeter circuit is driven from the source of Q1. Ignoring the two diodes, D1 and D2, for the moment, the meter (M1) is arranged with several 'range' resistors in series: R6, RV1 and RV2. The latter two are switched to provide 'x1' and 'x2' ranges. In the x1 range, M1 has a full scale deflection sensitivity of 0.5 V, while in the x2 range it has an FSD sensitivity of 1 V. The unit is set up




by adjusting RV1 and RV2 to give the appropriate full scale readings.

As the input FET develops a small bias voltage across R5, the negative side of the meter circuit has to be 'biased up' to counteract a permanent meter deflection. This is provided by another FET connected as a source-follower, Q2. Its gate is returned to the source bias, a potentiometer, so that the 'zero point' on the meter may be adjusted. This arrangement also provides a measure of stability, and little 'drift' in the meter reading is noticeable.

Diodes D1 and D2 protect the meter against serious overloads. When the voltage drop across R6 and M1 exceeds about 550 - 600 mV, of either polarity, one diode or the other will conduct, shunting the meter with a low impedance, reducing any further increase in current flow through the meter. A high reverse voltage at the input may destroy Q2, but the meter will be protected.

A simple input attenuator is arranged to provide three basic ranges of 0.5 V, 5 V and 50 V full scale, in the x1 range, these double to 1 V, 10 V and 100 V respectively.

The circuit is not critical as to layout, apart from the usual precautions to avoid possible accidental shorts, but a good quality switch having excellent insulation resistance impervious to humidity variations should be employed for the RANGE switch, SW1. A switch with ordinary bakelite insulation would be unsatisfactory. The circuit need not be built as a stand-alone unit, but makes an excellent add-on for a multimeter that has a 50 uA current range. Alternatively, if your meter has a 0.5 V range and is protected, delete D1, D2 and R6, connecting the meter between R5 and the junction of RV1 and RV2.

If building it as a stand-alone unit, buy a meter with a good-sized face (80 mm wide, for example). If you can get a mirror-scale type, so much the better. ●

# Lab Notes

# The LM3914 — a versatile LED bargraph driver chip

This chip has rapidly become popular with hobbyists and professionals alike. It has a wide variety of potential applications and is easy to use.

**Ray Marston**

THE LM3914 is a highly versatile IC designed to sense an analogue input voltage and drive a line of 10 LEDs to give a visual analogue display in either a 'Dot' or 'Bar' format.

Figure 1 illustrates the appearance of the two alternative display modes when used to indicate 5 volts on a 10 volt scale. The unit acts as an inexpensive alternative to the conventional-indicating moving-coil meter. It does not suffer from 'sticking' problems, is unaffected by vibration and can be used in any attitude. However, intermediate values are not indicated.

The LM3914 can readily be used as the basis of a wide variety of 'indicator' and instrumentation projects in the home, the car, the workshop and miscellaneous audio and musical projects. One of the great attractions of the device is that it is very easy to understand and use. You don't need to be a BA or MSc to be able to fully comprehend its operating principle and learn

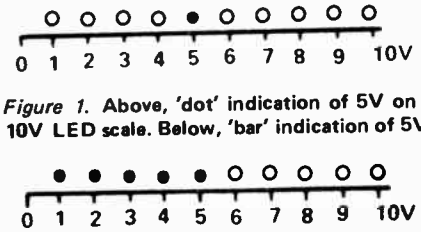



*Figure 1.* **Above, 'dot' indication of 5V on a 10V LED scale. Below, 'bar' indication of 5V.**

to adapt it to suit your own particular circuit requirement. This article explains the essential details of the device and shows several practical ways of using it in the next few pages.

## Basic principles

Figure 2 shows the equivalent internal circuit of the LM3914 together with the connections for making it act as a 10-LED voltmeter with a full-scale sensitivity of 1.2 volts.

The first point to note about the IC is that it contains a 10-resistor potential divider, wired between pins 4 and 6. The IC also contains ten voltage comparator circuits, each with its non-inverting (+) terminal taken to its own particular tap on the potential divider, but with all inverting (-) terminals of the comparators joined together and taken to the output of an input buffer amplifier. This buffer amplifier gives an output that is, for all practical purposes, identical to the voltage applied to input terminal 5 of the IC. The output of each one of the ten voltage comparators is individually available on one of the pins of the IC (pin 1 and pins 10 to 18) and is capable of 'sinking' a current of up to 30 mA.

The next point to notice is that the IC contains a built-in reference voltage source that provides a highly stable potential of 1.2 volts between pins 7 and 8. This source is of the 'floating' type, so that 1.2 volts is developed between pins 7 and 8 irrespective of whether pin 8 is tied to ground or held at some voltage above ground. In the diagram of Figure 2 we've shown pins 7 and 8 externally connected to potential divider pins 6 and 4 respectively, so in this particular case 1.2 volts is developed across the 10-resistor potential divider network of the IC.

The final point to notice about the IC is that it contains an internal logic network that can be externally programmed to give either a 'dot' or a 'bar' display or action from the outputs of the ten voltage comparators. In the 'dot' mode, only one of the ten outputs is enabled at any one time. In the 'bar' mode all outputs below and including the highest 'energised' output are enabled at any one time.

At this point, let's put together the

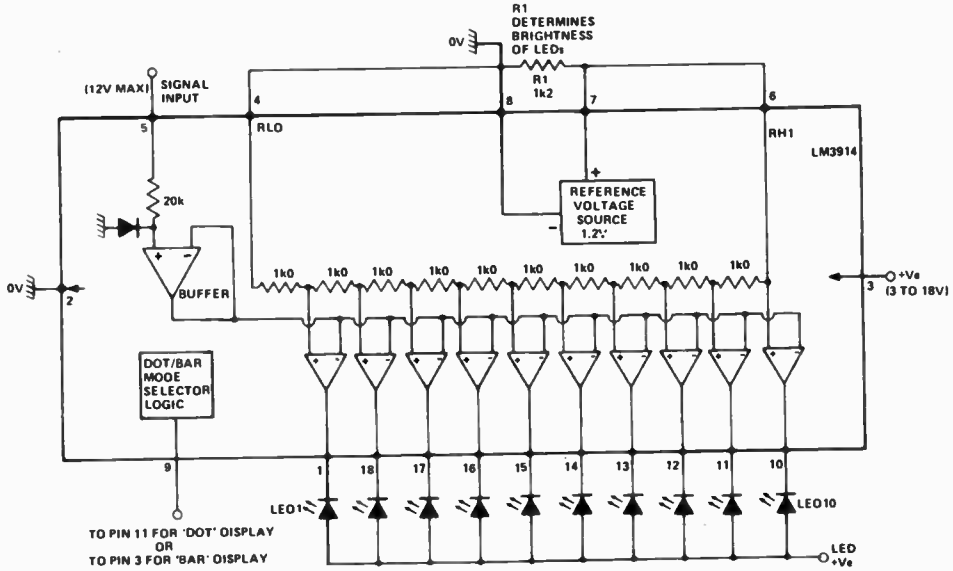



*Figure 2,* **Equivalent internal circuit of the LM3914 dot/bar LED indicator. This is the linear indicator chip in a series of three — the '15 is a log type, the '16 a VU type.**

basic information that we have already learned about the LM3914 and the circuit of Figure 2, and see how the entire circuit functions. Let's assume that the logic is set for 'bar' mode operation.

We already know that a reference of 1.2 volts has been set up across the 10-resistor divider, with the low (pin 4) end of the divider tied to ground (zero) volts. Consequently, 0.12 V is applied to the '+' input of the lowest voltage comparator, 0.24V to the next, 0.36 V to the next and so on. If we now apply a slowly rising voltage to input pin 5 of the IC, the following sequence of events takes place:

When the input voltage is zero, the outputs of all ten voltage comparators are high and none of the external LEDs are turned on. As the input voltage is slowly increased it eventually reaches and then rises above the 'reference' 0.12 volts value of the first comparator, which then turns on (its output conducts) and energises LED 1. As the input is further increased it eventually reaches the 0.24 V of the second comparator, which then also turns on and energises LED 2. At this stage both LED 1 and LED 2 are on. As the input voltage is progressively increased, more and more comparators and LEDs are turned on until eventually, when the input rises to and then exceeds 1.2 volts, the last comparator and LED 10 turn on, at which stage all ten LEDs are illuminated.

A similar kind of action is obtained when the LM3914 logic is set for 'dot' mode operation, except that only one LED turns on at any given time. At zero volts, none of the LEDs are on. At voltages above 1.2 (or whatever reference value is applied to the last comparator) only LED 10 is turned on.

At this stage, then, you can see that the LM3914 is a reasonably easy device to understand. Let's move on and look at some of the finer details of its operation.

## A closer look

There is one component in Figure 2 that we have not yet mentioned and that is R1. This resistor is wired between the pin 7 and pin 8 output terminals of the reference voltage source and determines or 'programmes' the ON currents of the LEDs. The current of each LED in fact approximates ten times the output current of the reference voltage source. The reference

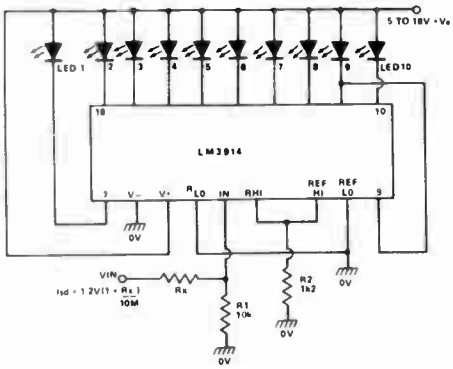



*Figure 3.* **Dot mode voltmeter. Rx may be switched to provide fsd reading from 1.2V to 1000V dc.**

can supply up to 3 mA of current, so the LEDs can be programmed to pass currents up to 30 mA.

Remembering that the reference develops 1.2 V, you can see that if a total resistance of 1 k2 is placed across the pin 7 — pin 8 terminals the reference will pass 1 mA and each LED will pass 10 mA in the ON mode. In Figure 2 the total resistance across the reference terminals is equal to the 1k2 of R1 shunted by the 10k of the IC's internal potential divider, so the reference actually passes about 1.1 mA and the LEDs conduct 11 mA. If R1 were removed from the circuit the LEDs would still pass 1.2mA due to the resistance loading of the internal potential divider on pins 7 and 8.

You'll notice from the above description that the IC can pass total currents up to 300 mA when it is used in the 'bar' mode with all ten LEDs on. The IC has a maximum power rating of only 660 mW, so there is a danger of exceeding this rating when the IC is used in the 'bar' mode. We'll return to this point later.

The IC can be powered from a dc supply in the range 3 to 25 volts. The LEDs can use the same supply as the IC or can be independently powered from supplies with voltages up to a maximum of 25 V. The voltage across the internal potential divider can have any value up to 25 volts maximum.

The internal reference amplifier produces a basic nominal output of 1 28 volts (limits are 1.2 V to 1.32 V), but can be externally 'programmed' to produce effective reference values up to 12 V (we'll show how later).

The input buffer of the IC has integral overload protection and can withstand inputs of up to plus or minus 35 V without damage.

The IC can be made to give either a 'dot' display by wiring pin 9 to pin 11, or a 'bar' display by wiring pin 9 to positive-supply pin 3.

## Practical ciruits: Simple dot mode voltmeters

The basic circuit of Figure 2 acts as a voltmeter that reads full-scale at an input of 1.2 volts. The range of the circuit can be changed in a variety of ways. The sensitivity can be increased, for example, by either interposing a dc amplifier between the input signal and pin 5 of the IC, or by reducing the reference voltage that is applied to the pin 4 — pin 6 terminals of the IC: in this latter case the IC will operate quite well with a reference voltage down to a couple of hundred millivolts.

The easiest and best way to reduce the sensitivity of the meter is to use the connections shown in Figure 3. Here, the basic circuit is that of a 1.2 V meter, but the input signal is applied to the IC via a potential divider formed by Rx and R1. Thus, the circuit can be made to read 12 volts full scale by giving Rx a value of 90k, so that Rx-R1 act as a 10:1 divider. This circuit can be used to read full scale voltages from 1.2 V up to about 1000 V.

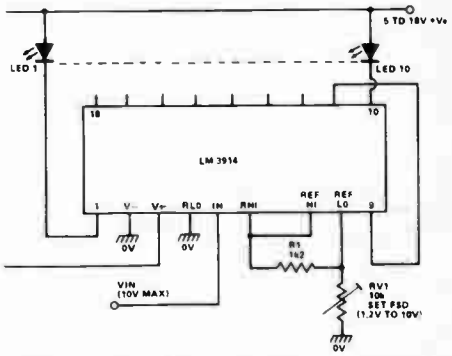



*Figure 4.* **An alternative 1.2V to 10V fsd dot mode voltmeter.**

An alternative connection is shown in Figure 4. In this case the input voltage is applied directly to pin 5 of the IC, but the reference voltage on the internal divider is made variable from 1.2 V to 10 V via RV1. You'll remember that the 'reference voltage' develops 1.2 V between pins 7 and 8, but this voltage is fully floating. By wiring RV1 between pin 8 and ground we can ensure that the output current of the reference flows to ground via RV1, thus providing a voltage that raises the pin 8 (and also pin 7) value considerably above zero volts. This increased voltage is applied to the top

(pin 6) end of the internal potential divider, which has its low end (pin 4) grounded and determines the full scale sensitivity of the circuit. This circuit has a useful voltage range of only 1.2 to 10 volts. The IC supply voltage must be greater than the required full scale voltage.

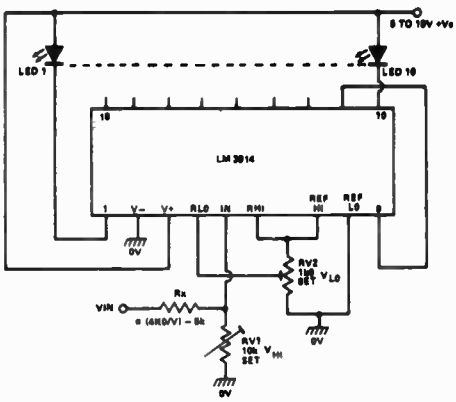


*Figure 5.* **Expanded scale dot mode voltmeter for the 10 - 15 V range.**

Figure 5 shows how the LM3914 can be used as an expanded scale voltmeter that reads (say) 10 V at minimum scale but 15 V at full scale. The secret of this circuit is that both the top and bottom ends of the internal potential divider (pins 6 and 4) of the IC are externally available, so the top and bottom limits of the scale can be individually set. In the diagram the top of the divider is fed from the 1.2 V reference, but the bottom is fed from the slider of RV2. The external input signal is applied to the IC via the Rx-RV1 potential divider. Thus, if 1.2V is set to the top of the divider and 0.8 V is set to the bottom and the input divider has a ratio of 20:1, the circuit will read 24 V at full scale and 16 V at minimum scale.

## Bar mode operation

The three basic voltmeter circuits of Figures 3 to 5 can be used with the IC connected in either the 'dot' or the 'bar' mode. When using the bar mode, however, it must be remembered that the power rating of the IC can easily be exceeded when all ten LEDs are on if an excessive voltage is allowed to develop across the output terminals of the IC. LEDs normally 'drop' about 2 volts when they are conducting, so one way around this problem is to power the LEDs from their own low-voltage (3 to 5 V) supply, as shown in Figure 6.

An alternative solution is to power the IC and the LEDs from the same source but to wire a current-limiting resistor in series with each LED, as shown in Figure 7, so that the output

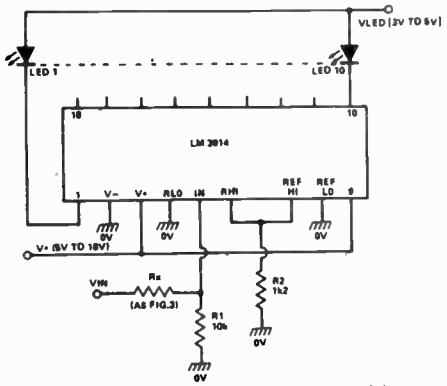


*Figure 6.* **Bar display voltmeter with separate supply for the LEDs. Rx may be switched to provide various fsd ranges as per figure 3.**

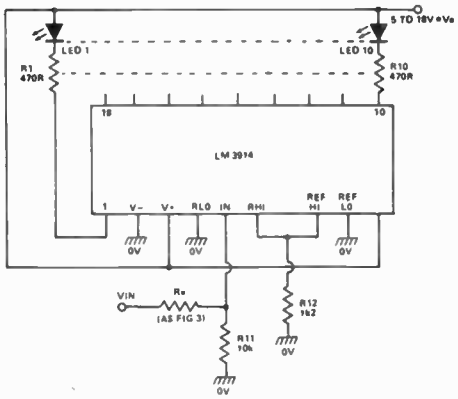


*Figure 7.* **Bar display voltmeter with common LED supply.**

terminals of the IC saturate when the LEDs are on.

## 20-LED voltmeters

Figure 8 shows how two LM3914s can be interconnected to make a 20-LED dot-mode voltmeter. Here, the input terminals of the two ICs are wired in parallel, but IC1 is configured so that it reads 0 to 1.2 volts and IC2 is configured so that it reads 1.2 volts to 2.4 volts. In the latter case, the low end of the IC2 internal potential divider is coupled to the 1.2 V reference of IC1 and the top of the divider is taken to the 'top' of the 1.2 V reference of IC2, which is raised 1.2 V above that of IC1.

The circuit of Figure 8 is wired for 'dot' mode operation. In this case pin 9 of IC1 is wired to pin 1 of IC2 and pin 9 of IC2 is wired to pin 11 of IC2. Note that a 22k resistor is wired in parallel with LED 9 of IC1 in this mode.

Figure 9 shows the connections for making a 20-LED 'bar' mode voltmeter. The connections are similar to those of Figure 8, except that pin 9 is taken to pin 3 on each IC, and a 470 ohm current limiting resistor is wired in series with each LED to reduce the power dissipation of the ICs. ●

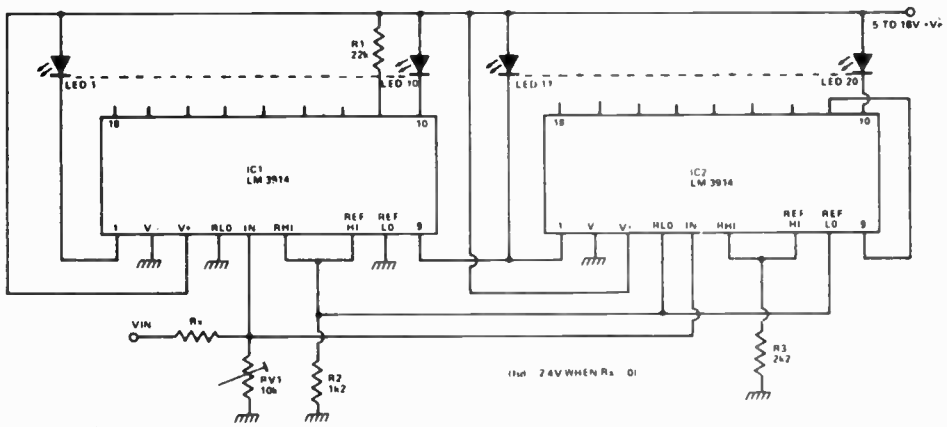


*Figure 8.* **Dot mode voltmeter with 20 LEDs. Full scale is 2.4 V when Rx is zero.**

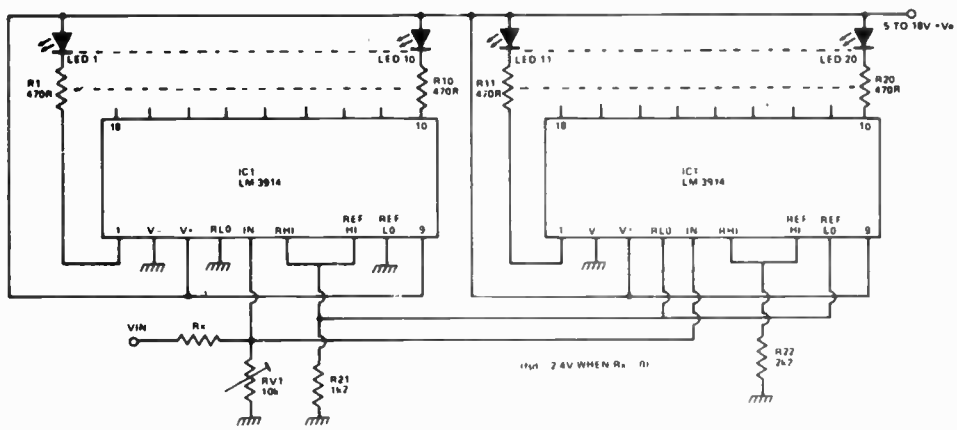


*Figure 9.* **Bar mode voltmeter version of above.**

# The junction FET — its haunts and habits

The first in a whole family of field effect transistors, the junction FET is found in many and varied applications. If you're new to electronics or unfamiliar with the device, this article should introduce you to the haunts and habits of the JFET.

**Brian Dance**

THE JUNCTION Field Effect Transistor or JFET is a small electronic device much like a transistor in appearance which normally has three connections, although a fourth connection is attached to the metal case of some types for high frequency screening. Junction field effect transistors are one of the two main types of field effect transistor, the other type being known as the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) or as the IGFET (Insulated Gate Field Effect Transistor).

Field effect transistors can be used as amplifiers and oscillators as well as for other applications for which an ordinary or bipolar transistor could be employed, but have particular advantages for certain applications. Field effect transistors are also used in the internal circuitry of integrated circuits.

## Connections

As in the case of npn and pnp bipolar transistors, junction field effect transistors can be obtained in two polarities, these being known as n-channel and p-channel types. A far wider variety of n-channel types is manufactured than p-channel devices, since they tend to have a better performance, but devices of both polarities are readily obtainable.

The electrodes and circuit symbols for the two types are shown in Figure 1. The current flowing in a channel between the drain and the source is controlled by a voltage applied to the gate electrode. The gate is therefore the input electrode and may be compared with the base of a conventional transistor. Similarly the drain and source may be compared with the collector and the emitter respectively.

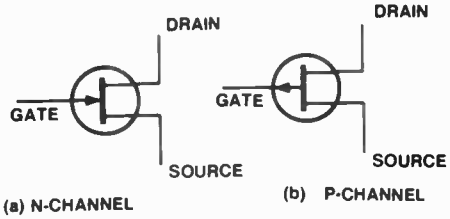



*Figure 1.* **Symbols for n-channel (a) and p-channel (b) junction FETs.**

One of the main differences between field effect transistors and bipolar transistors is that field effect transistors are essentially voltage amplifiers whereas bipolar transistors are basically current amplifiers. Thus the field effect transistor behaves more like the old thermionic valve in its circuits.

Field effect transistors tend to be more expensive than most of the common bipolar types — probably because the bipolar types are sold in much larger numbers. The economical 2N3819 n-channel field effect transistor is probably the most commonly used type and is very suitable for the readers who wish to carry out their first experiments with field effect transistors. This device is encapsulated in a black plastic or epoxy body and has the connections shown in Figure 2. The 2N3820 is a similar economical p-channel device.

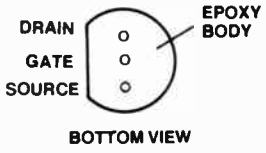



*Figure 2.* **Connections for the common 2N3819 plastic-encapsulated n-channel JFET.**

## High input impedance

One of the main advantages of a field effect transistor is that it has a very high input resistance and therefore takes very little current from the circuit which feeds it — typically far less than a microamp. This means that it has very little effect on the circuit which feeds it, even if this circuit has such a high output impedance that it can deliver only a very minute current.

In order that an n-channel device shall operate correctly and have a high input impedance at its gate, it must be suitably biased with its gate negative with respect to the other electrodes. Similarly the gate of a p-channel device has a high impedance when it is positively biased.

# APPLICATIONS

## Pierce oscillator

In the circuit of Figure 3 the field effect transistor is employed in a Pierce type of oscillator whose frequency is controlled by the quartz crystal shown. The advantage of using a field effect transistor in this type of circuit is that the gate imposes only a very small load from the crystal and therefore the quality factor or Q factor of the crystal is not appreciably affected, so excellent frequency stability can be obtained.

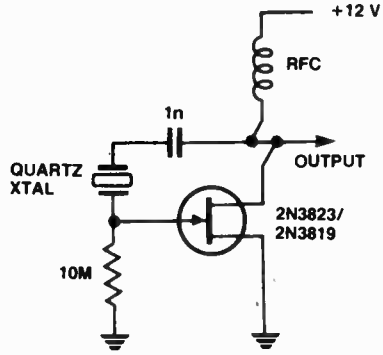



**Figure 3. A Pierce crystal oscillator (National Semiconductor).**

National Semiconductor recommend their 2N3823 n-channel device for use in this circuit, but the more economical 2N3819, which is made by the same type of process, is also suitable. The supply voltage is not at all critical, but the radio frequency chokes used in the supply lead should have a high impedance at the frequency of oscillation.

An advantage of this circuit is that one can change the crystal over quite a wide range of frequencies without making any other changes to the circuit and still obtain a satisfactory performance. The exact frequency range over

which the circuit will operate depends very much on the choke used and to some extent on the circuit layout.

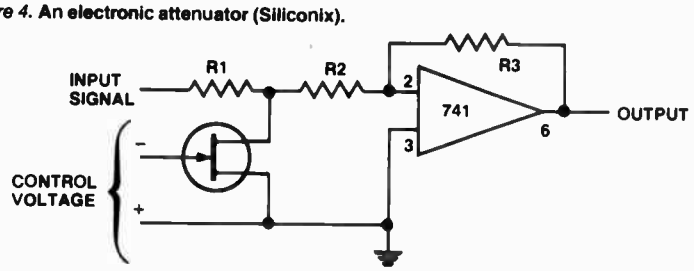
This type of circuit is suitable for use in a crystal calibrator for a receiver. If a 1 MHz crystal is employed, the output may be fed to a radio receiver to produce a signal at 1 MHz and at each multiple of 1 MHz up through the shortwave bands to provide calibration points.

## Electronic attenuator

A junction field effect transistor can be used as a variable resistor, the value of which is controlled by the voltage applied to the gate electrode. As the applied bias becomes smaller, the resistance between the drain and source electrodes falls.

This property is used in the circuit of Figure 4 to design an electronic attenuator for audio signals. When the negative control voltage applied to the gate electrode is relatively large, little drain current passes through the device and the circuit behaves as if the field effect transistor were not present. However, as the control voltage falls at the gate electrode, the drain draws current from the junction of R1 and R2 so that the output signal amplitude is attenuated progressively.

*Figure 4.* **An electronic attenuator (Siliconix).**




## Tone control

The circuit of Figure 5 is a tone control circuit with bass and treble boost and cut facilities. In this circuit the 2N3684 field effect transistor is used to enable the circuit to have a very high input impedance. It is used as a source follower circuit (analagous to an emitter follower) which provides a low output impedance signal coupled by a 1u capacitor to the tone control network. This network is in the feedback circuit of the LM301A operational amplifier circuit. The 2N3684 enables a good low-noise performance to be obtained.

## Lambda oscillator

A very simple sinewave oscillator is shown in Figure 6; it is essential that one n-channel and one p-channel field effect transistor are used in this circuit. The two source electrodes are connected together and the gate of each device is connected to the drain electrode of the other device. This type of connection produces a negative resistance region in the current/voltage graph for the circuit with a peak in the graph like a Greek lambda ($\lambda$) — hence the name given to this type of circuit.

It is only necessary to connect the dual device circuit in series with a parallel tuned circuit, as shown in Figure 6, to produce oscillations at the resonant frequency of the tuned circuit used. It will oscillate at any frequency from the low audio region up to some tens of MHz, but the gate capacities of the devices used prevent operation in the regions above 100 MHz.

It is interesting to note that two separate parallel tuned circuits may be connected in series with the lambda circuit instead of the single tuned circuit shown in Figure 6. If one of these tuned circuits resonates at an audio frequency and the other at a radio frequency, the output will consist of an amplitude modulated radio frequency oscillation. This is perhaps one of the simplest possible modulated signal generators!

The output voltage from the circuit of Figure 6 is equal to twice the steady

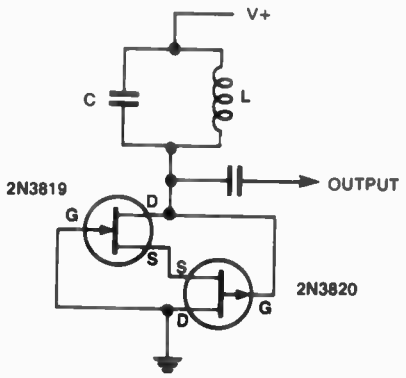



*Figure 6.* **Sinewave oscillator using a 'Lambda' circuit.**

power supply voltage applied to the circuit. Therefore this type of circuit can be very useful when one requires an output oscillation whose amplitude is accurately related to a steady applied voltage.

Complementary pairs of field effect transistors used in lambda circuits have other applications apart from simple oscillator uses.

## High impedance buffer stage

The circuit of Figure 7a shows a buffer or isolating amplifier which has a very high input impedance and low input capacitance. National Semiconductor recommend a 2N4416 field effect transistor for this circuit because it has a low input capacitance, but this is further reduced by the circuit feedback. The device is used as a source follower, so the voltage gain is about unity.

Although a 2N5139 pnp transistor is specified for this circuit, the 2N3906 plastic encapsulated type is much more readily available and is fabricated by the same process, so it can be used in this application.

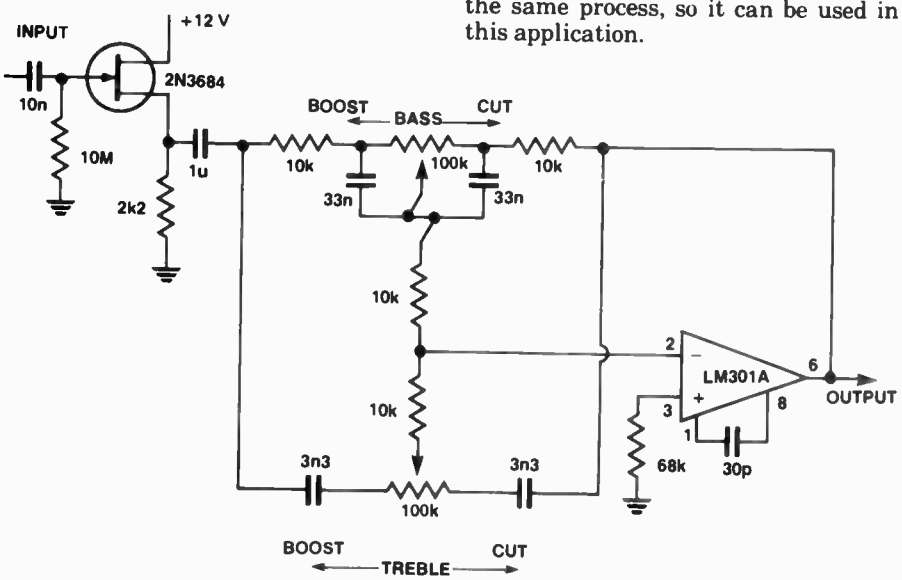



*Figure 5.* **High input impedance tone control circuit (National Semiconductor).**

## High impedance amplifier

The circuit of Figure 7b is very similar to that of Figure 7a except that the feedback circuit has been modified so that a voltage gain can be obtained. The circuit provides a gain of R2/R1 or 10 with the component values shown. Both the circuits of Figure 7 and of Figure 8 can be operated at high frequencies into the tens of MHz region.

## RF amplifiers

Junction field effect transistors are much used in the radio frequency stages of HF, VHF and UHF receivers, since they offer a noise performance equivalent to that of bipolar transistors with improved crossmodulation and intermodulation performance. Crossmodulation is the transfer of the modulation of one carrier onto the carrier of another signal. Intermodulation occurs when two or more signals outside the passband combine in the circuit to form a signal within the passband which causes interference with the wanted signal.

The better linearity of field effect transistors over bipolar transistors is responsible for this improvement. Mullard have quoted a 12 dB improvement in crossmodulation in a narrow-band FM receiver and a 20 dB improvement in a VHF broadcast receiver as having been achieved by the replacement of a bipolar mixer circuit with a junction field effect transistor circuit.

Figure 8 shows a high-performance amplifier using two JFETs connected in 'cascode' (series) with automatic gain control (AGC) applied to the gate of the upper device. The supply is applied to the 'cold' or 'ground' end of L2 via a feedthrough capacitor. Only the L-C values need be changed to operate this stage on other frequencies to the limits of the JFETs.

## Simple voltmeter

The high input impedance of a junction field effect transistor is used in the circuit of Figure 9 to produce a voltmeter with an input resistance of over 10M; in some measurements this high input impedance is necessary to prevent the current taken by a conventional voltmeter from dragging down the voltage being measured.

The input voltage being measured is divided by R1 and R2 so that a voltage of +0.2 V is present at the gate electrode when the full scale input voltage is applied for the range in question. In practice R1 should consist of a fixed resistor of a value somewhat less than that shown in the table, in series with a preset potentiometer so that the sensitivity of the range can be adjusted. If desired, R1 may be switched to provide a number of ranges.

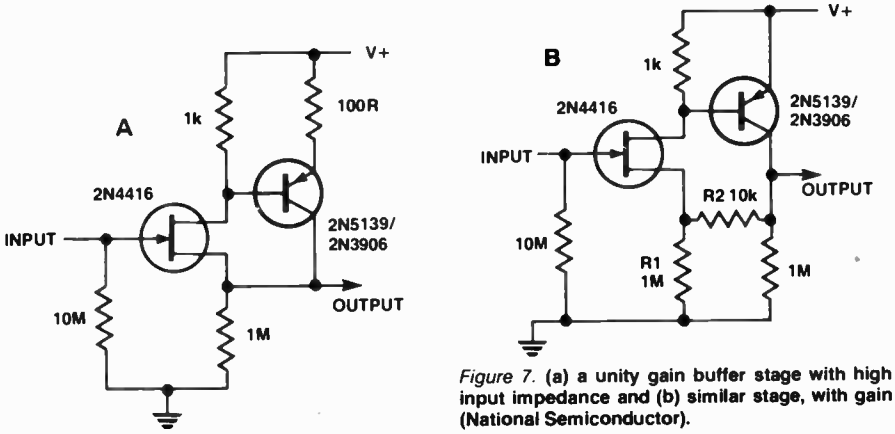



*Figure 7.* **(a) a unity gain buffer stage with high input impedance and (b) similar stage, with gain (National Semiconductor).**

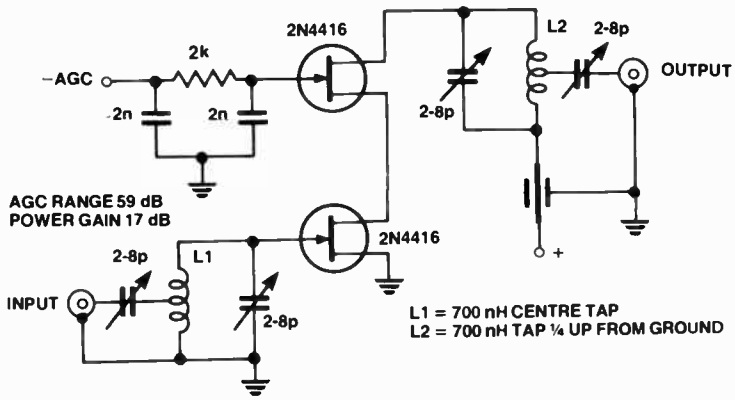



*Figure 8.* **Typical high-performance amplifier stage employing two FETs in 'cascode'. Values given for 200 MHz. A wide variety of RF FETs may be substituted (National Semiconductor).**

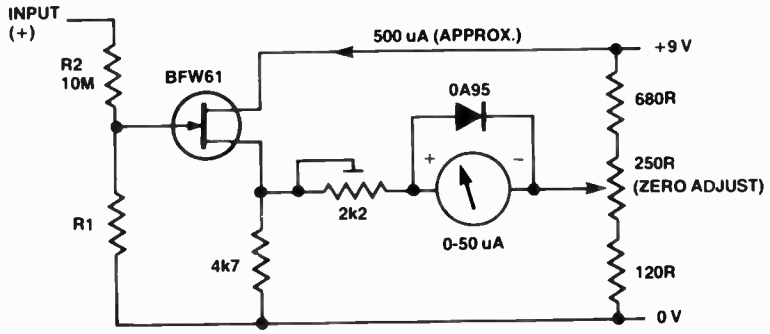



*Figure 9.* **High input impedance voltmeter. Note that a BFW10 could substitute for the BFW61 (Mullard).**

**Table showing the value of R1 to be used in Figure 9 for various ranges.**

| Meter range | R1 |
|---|---|
| 250 mV | 40M |
| 500 mV | 6M67 |
| 1 V | 2M5 |
| 10 V | 204k |
| 50 V | 40k |
| 100 V | 20k |
| 250 V | 8k |
| 500 V | 4k |

No two field effect devices have exactly the same characteristics, and the 2k2 resistor in series with the meter enables the full-scale meter current to be adjusted to allow for the characteristics of the particular device used. The diode protects the meter from overloading.

## PhotoFET

Photosensitive field effect transistors (photoFETs) can be made which have a window or a lens, so that any light falling on this window affects the junc-

tion and hence the drain current of the device in much the same way that light affects a phototransistor. However, photoFETs are not very common devices.

An application of a Teledyne Crystallonics photoFET as a light-controlled variable attenuator is shown in Figure 10. The drain-to-source resistance of the

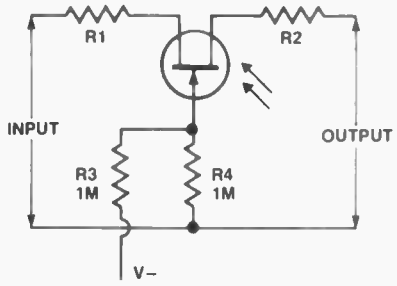



*Figure 10.* **Example of a light-controlled attenuator (Teledyne Crystallonics).**

photoFET is a function of the intensity of the illumination, so as more light shines on the device, the output rises. The negative voltage to which the resistor R3 is returned determines the range in which the drain-to-source resistance falls. Like other silicon photosensitive devices, the photoFET is sensitive to the red and near infrared regions of the spectrum, such as the radiation from an incandescent filament bulb.

# HOW DO THEY WORK?

An n-channel field effect transistor consists of a channel of n-type semiconductor material between the drain and the source surrounded by p-type material of the gate electrode. Almost all of the devices are made of silicon, but a few special devices are produced in other semiconductor materials. As shown in Figure 11, the gate normally receives a

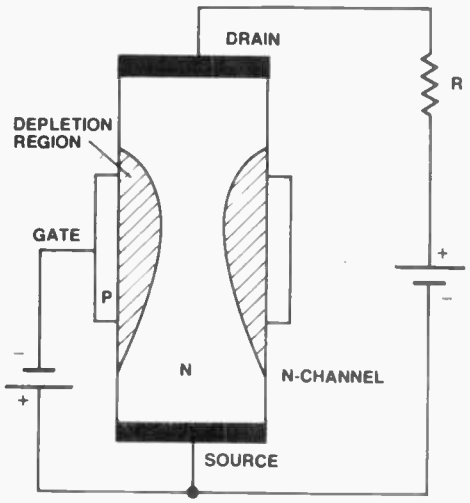



*Figure 11.* **Control of channel width in an n-channel device.**

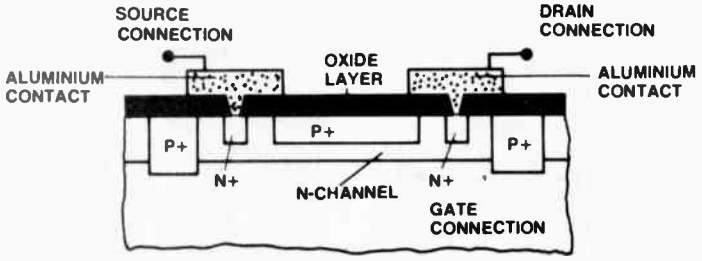



*Figure 12.* **Structure of a silicon planar device (Mullard).**

negative bias relative to the source and the drain a positive bias.

As the p-type gate material receives a negative bias, the junction formed between this material and the n-type channel is reverse biased. In any reverse-biased junction, a region which is depleted of charge carriers (electrons and holes) is formed. As this depletion region contains very few mobile charges, it acts almost as an insulator and has a very high resistance.

The gate is normally much more heavily doped than the channel material, since this results in the depletion region spreading fairly deeply into the channel and not very far into the material of the gate. As the drain is normally made positive with respect to the source electrode, the voltage between the drain and the negative gate is larger than that between the source and the gate. The electric field is therefore greater on the drain side of the gate electrode and this results in the depletion region becoming deeper on the drain side and thus producing a narrower channel on this side, as shown in Figure 11.

If the voltage applied to the gate becomes more negative, the depletion region goes deeper into the n-channel material until eventually the channel becomes completely cut off on the drain side of the gate. Very little drain current can then flow through the device. As the gate voltage becomes less negative, the channel opens again and becomes wider as the gate voltage approaches that of the source; the widening of the channel under the control of the gate voltage results in the channel current from the drain to source increasing.

As the gate-to-channel capacitance comprises a reverse-biased pn junction, the gate has a very high input resistance and passes only a very minute current (often in the pA region). However, the gate capacitance is appreciable and therefore an appreciable alternating current may flow to this electrode at high frequencies. Even when the gate and source potentials become equal, there is still a small depletion region and the gate input resistance is high. However, if the gate of an n-channel device receives a positive bias of more than about 0.65 V, current can flow in the gate circuit and this current may damage the device.

## Structure

The design of a modern field effect transistor is not implemented in the form of Figure 11, which has been used for explanatory purposes, but silicon planar technology is usually employed to produce a structure such as that of the Mullard/Philips BFW11 shown in Figure 12. This has a surface or planar structure which is covered with a protective layer of silicon dioxide at all points except where electrode connections are attached. This oxide layer prevents impurities from contaminating the surface of the material and thus producing unwanted currents.

The aluminium contacts at the source and drain electrodes allow current to flow from them into the heavily doped small n+ regions, which make good contact with the n-channel region. In some devices a number of n-type channels are connected in parallel to enable a larger current to flow at the expense of an increased gate capacitance.

## P-channel types

P-channel field effect transistors have the same type of structure as shown in Figures 11 and 12, but the p and n type materials are interchanged. The gate is made of n-type material and must therefore be biased positively, as shown in Figure 13. The drain is normally biased negatively.

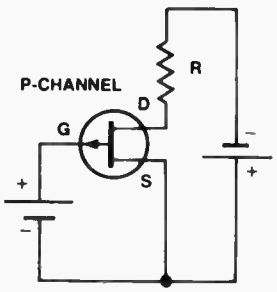



*Figure 13.* **A p-channel device requires supplies of the opposite polarity to those used with n-channel devices.**

## Limiting voltages

If the bias applied to the gate is taken far beyond that required for normal operation, a point will eventually be reached at which reverse breakdown occurs. Similarly there is a limit to the voltage which should be applied between the drain and the source electrodes. However, junction devices cannot be damaged by the ordinary electrostatic charges which can accumulate on people and clothing and which can damage MOSFET devices.

## Testing JFETs

It is relatively easy to check that a junction field effect transistor is able to function correctly. The circuit of Figure 14 may be used for an n-channel device and that of Figure 15 for a p-channel device.

If the gate is initially connected directly to the source (and not as shown), it will be found that the meter provides a reading of a few mA. This current is limited by the 1k resistor in the drain circuit to a safe value.

If the gate electrode is now connected to the 10M resistor as shown, the gate to channel junction is reverse biased. Thus the channel width decreases and with most devices the drain current will fall to zero in the circuits shown. As the gate circuit has a very high resistance, the voltage can be applied to it through a high-value resistor; indeed, it is interesting to note that the human body can be used in place of the 10M resistor shown when testing junction field effect devices.

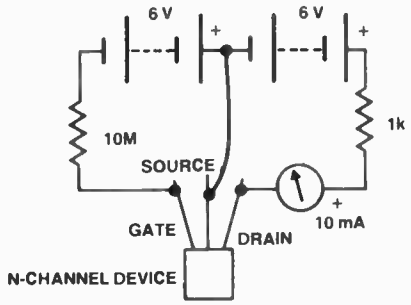



*Figure 14.* Testing an n-channel device.

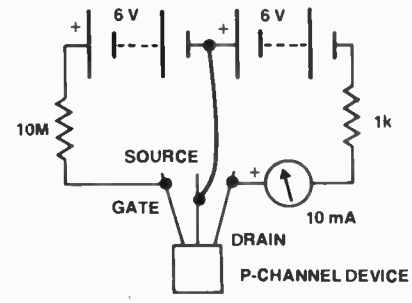



*Figure 15.* Testing a p-channel device.

If one wishes to test a device and does not know the connections, one can first find two connections in which a small current will pass in either direction. These are the source and drain connections.

A current should pass from the third electrode, the gate, only in one direction to either of the other two electrodes. If conduction takes place when the gate is positive, one has an n-channel device, whereas if conduction takes place when the gate is negative, the device is of the p-channel polarity.

One cannot easily determine which electrode is the drain and which is the source, but these electrodes are to some extent electrically interchangeable. ●

### USEFUL BOOKS

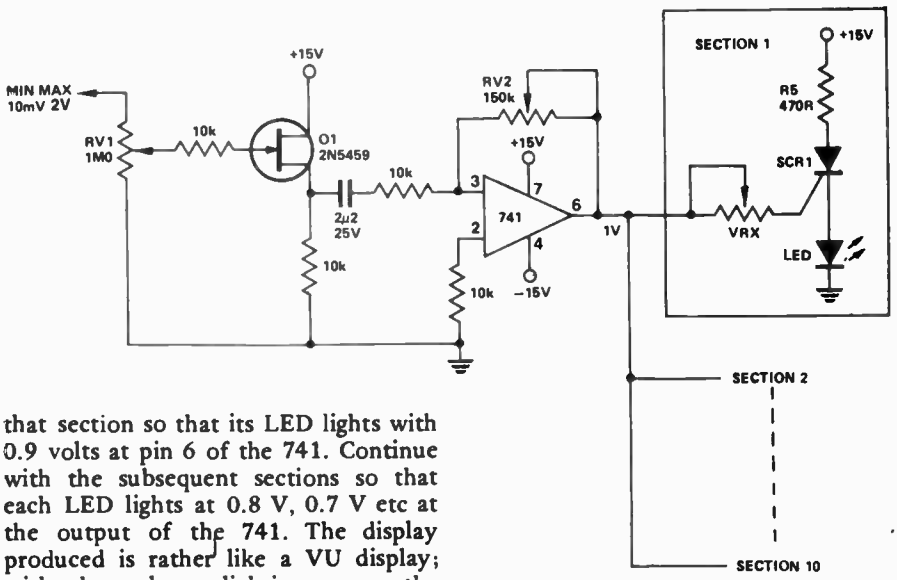
Two very useful books, though difficult to obtain, are: 'FET Databook' from National Semiconductor and 'Field Effect Transistors' from Philips.

# Sound to light modulator

Modulating a light, or a bank of lights, from a sound source (such as a tape recorder or record player) is an ever-popular topic so we dragged this circuit from the depths of our files.

A high impedance input is provided by a source-follower, Q1, so that the unit may be driven from either a high or low impedance source. An op-amp (a 741) then provides sufficient gain to trigger the SCR which drives the LED. As the input varies, the drive to the LED will vary, modulating the light output. Each 'Section' (1,2,3 . . .) drives a LED, all the LEDs being mounted in a row.

When setting up, RV1 and RV2 are adjusted so that with the maximum input voltage available, 1 V is available at pin 6 of the op-amp. Then VRX is adjusted so that the LED lights. Then Section 2 is tackled; adjust VRX for that section so that its LED lights with 0.9 volts at pin 6 of the 741. Continue with the subsequent sections so that each LED lights at 0.8 V, 0.7 V etc at the output of the 741. The display produced is rather like a VU display; with the column lighting up as the sound rises and falls.



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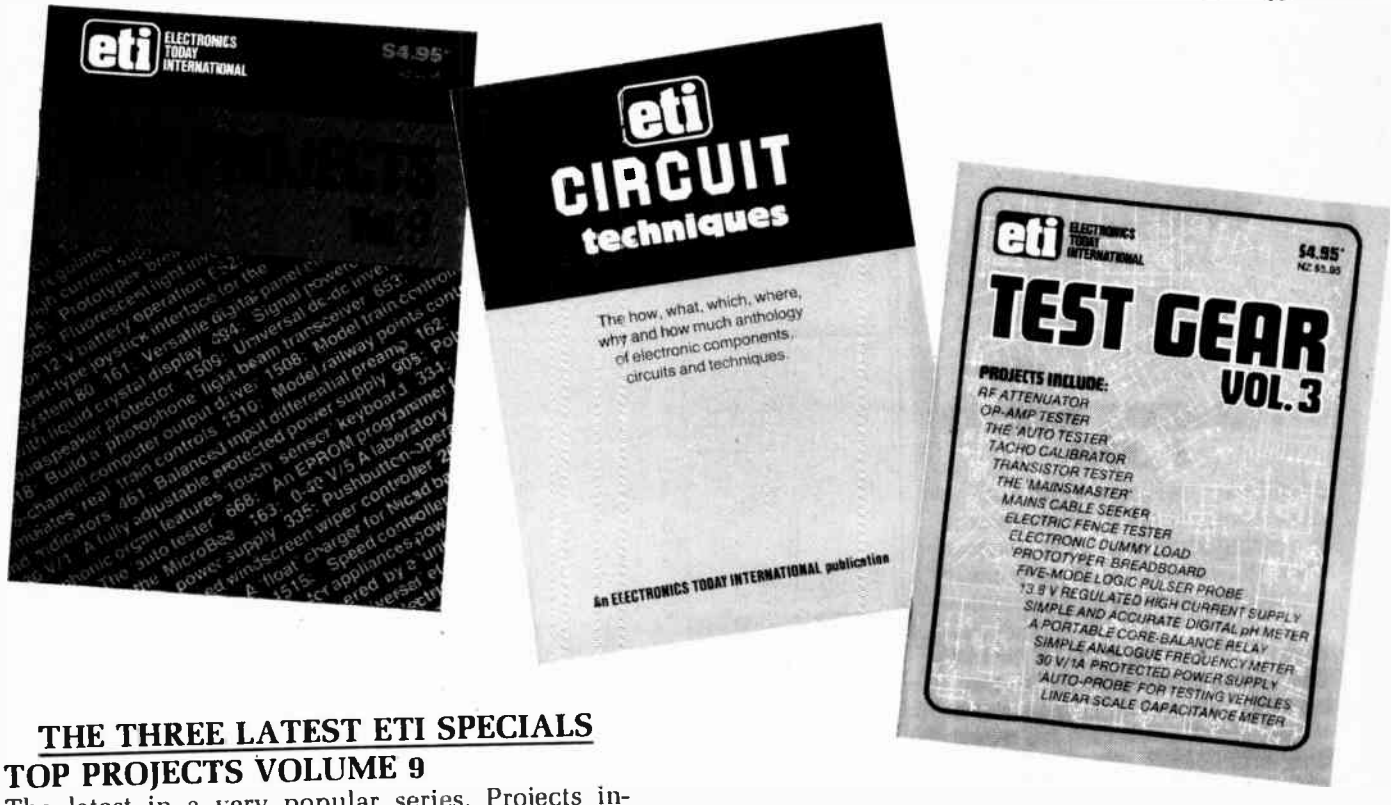


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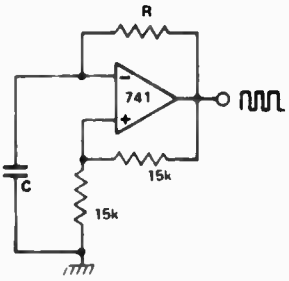
# Circuit source guide

Here is an abundance of circuits that should prove a useful, if not informative, source from which you can derive other circuits or assemble a circuit from a variety of 'blocks' to suit a particular application or solve a circuit problem. Tim Orr has assembled this anthology, covering applications that range from dc control to digital instrumentation, preamps to power supplies and more. You may have seen some of these ideas before, but there are bound to be plenty you haven't.

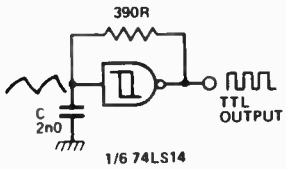
## GENERATORS

### Op-amp Oscillator




$F \sim \frac{1}{RC}$ (rule of thumb)

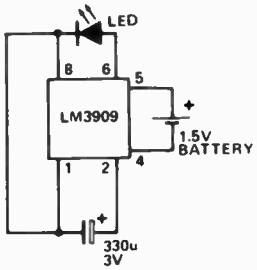
### TTL Oscillator



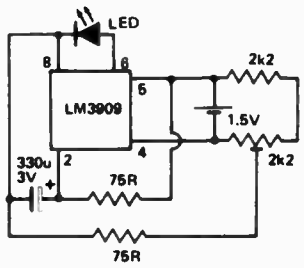

Vary C to change frequency
*Do not* increase the size of the 390R resistor

Frequency range = 1 Hz to 1 MHz

### LED Flasher

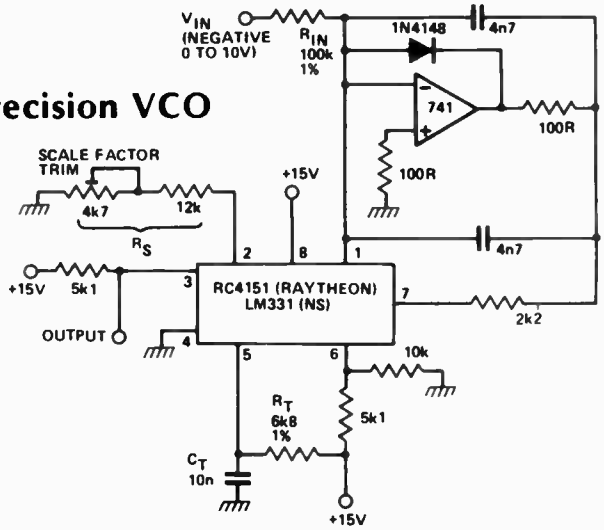



1 Hz flash rate
Average current drain = 0.32 mA
Circuit uses the timing capacitor to boost the output voltage




Variable flash rate 0 to 20 Hz

### Precision VCO



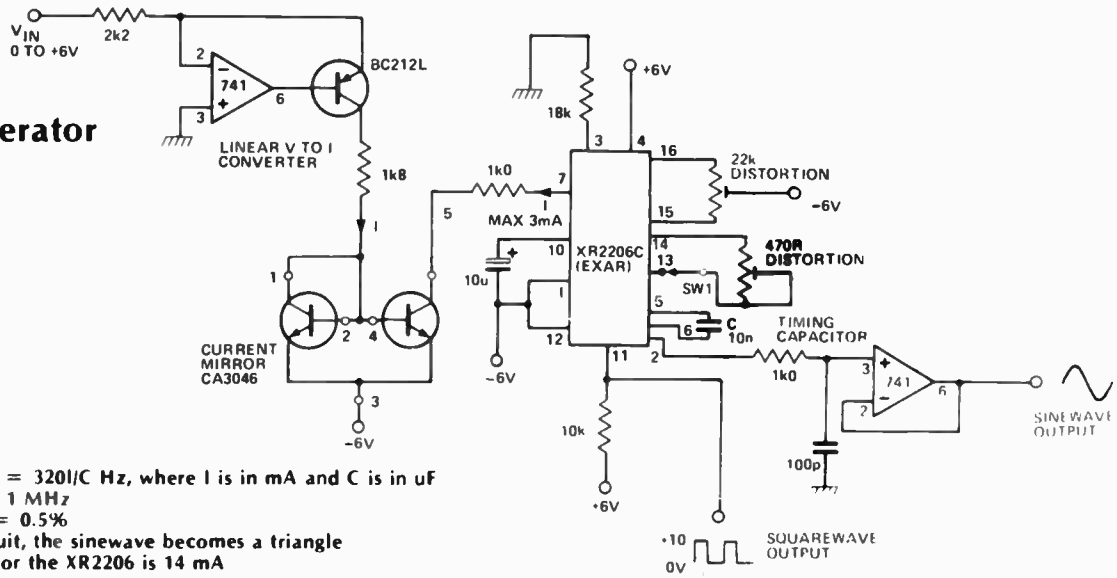

$F = (-V_{IN})/2.09 \times (R_S/R_{IN}) \times 1/(R_T C_T)$ Hz

Maximum frequency = 10 kHz
Linearity = 0.05%
Response time = 10 us
Op-amp powered from ± 15 V

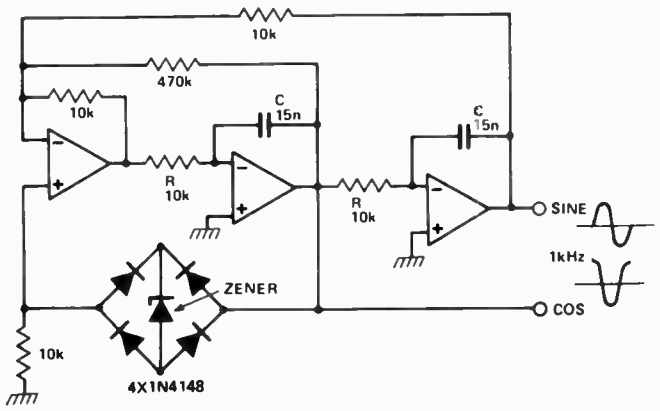
The LM331 is a precision voltage-to-frequency converter. In this application an additional op-amp is used to facilitate immediate response to changes of the input control voltage. The other advantage of the use of an additional op-amp is an increase in the sensitivity of the circuit to low control voltages. The limit here is the offset voltage and current for the particular op-amp used. The 741 specified is satisfactory although an improvement would be obtained if alternative devices were used, e.g: LM108, LM308A or LF351B.

Note that the 4n7 capacitor in the integrator should be a mylar capacitor to ensure accurate operation.

### Function Generator




Oscillation frequency F = 320I/C Hz, where I is in mA and C is in uF
Maximum frequency = 1 MHz
Best THD of sinewave = 0.5%
When SW1 is open-circuit, the sinewave becomes a triangle
Typical supply current for the XR2206 is 14 mA




## Dual Integrator Oscillator

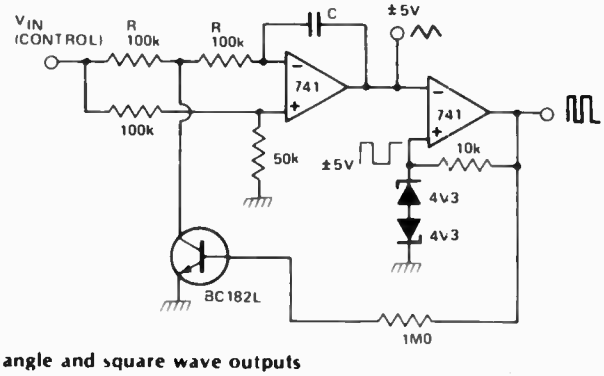
**Quadrature outputs (ie sine and cosine)**

**Output frequency** $F = \frac{1}{2\pi RC}$ **Hz**

**To change frequency, change both R's or both C's.**
**Maximum frequency ~ 20 kHz**
**Minimum frequency ~ 0.016 Hz using C = 1u0, R = 10M, and TL081 op-amps**
**Oscillation amplitude = 2x(zener voltage + 1V2) $V_{pp}$**

This oscillator provides two sinewave outputs with a phase shift of 90° with respect to each other, i.e: sine and cosine waveforms. The output frequency is relatively stable provided good components are used, and distortion figures below 0.1% are easily obtained.

## Linear VCO




**Triangle and square wave outputs**

**Output frequency** $F = (1.667 \times 10^{-7} \times V_{IN})/C$ **Hz**

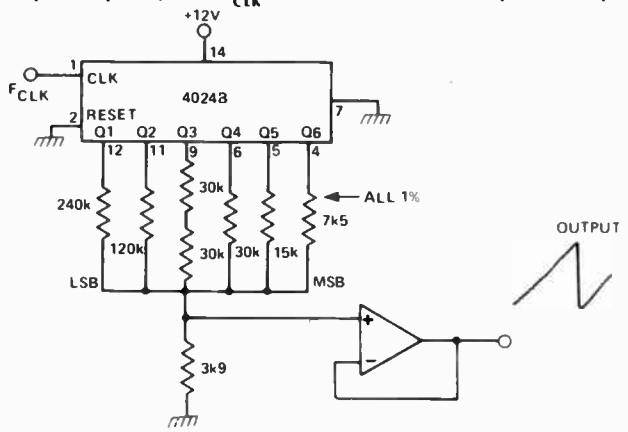
**If C = 1n0 and $V_{IN}$ = 10V, then F = 1.66 kHz**

**Changing both R's from 100k to 10k will increase F by x 10**

**For low frequencies use TL081 op-amps**
**Frequency range 0.1 Hz to 10 kHz**

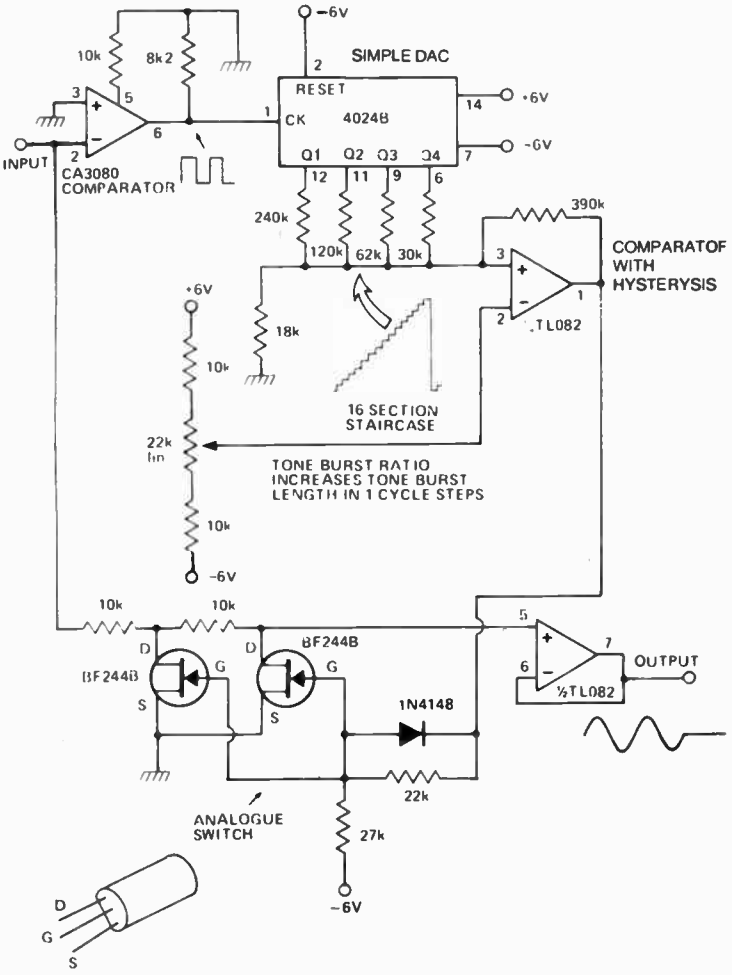
## Staircase Generator

**Output frequency** $F = F_{CLK}/64$ **Staircase is made up of 64 steps**




The 4024B is a CMOS seven-stage binary ripple counter. Upon receipt of a clock pulse the counter selects a combination of the resistors and increases the voltage at the output of the op-amp buffer. As with all edge-triggered devices the clock should be conditioned to have a single clean edge with a rise and fall time faster than 5 uS. The device clocks on the falling edge of the clock waveform.

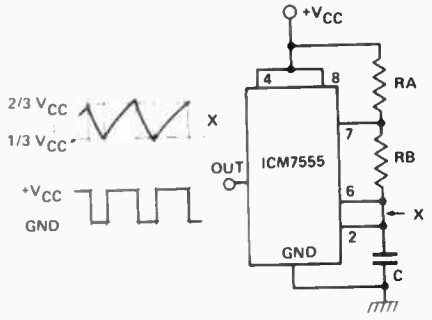
## Variable Length Tone Burst Generator




**Input is a sinewave or any other periodic waveform, maximum level ± 2 V, maximum frequency 100 kHz**
**Output is a tone burst variable from one cycle on, 15 cycles off to 15 cycles on, one cycle off**
**All devices powered from ± 6 V**

# GENERATORS

## CMOS 555 Oscillator

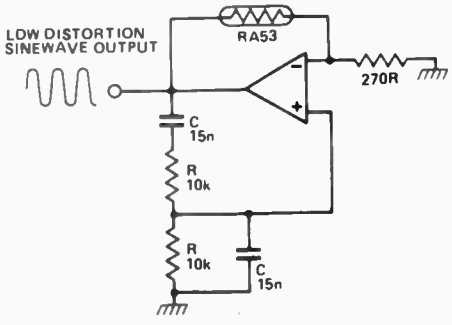



Output frequency F = 1.46/C(RA + RB)
C in farads, R in ohms
Quiescent current ~ 120 uA
Input current ~ 50 pA (this allows the use of resistors up to 10M in value)
Frequency range 0.001 Hz to 500 kHz
Supply range 2 to 18 V
Rise and fall time (pin 3) = 40 ns

| RA,RB | C | F |
|---|---|---|
| 10M | 10u TANT | 7.3 mHz |
| 1M0 | 1u0 | 0.73 Hz |
| 100k | 100n | 73 Hz |
| 10k | 10n | 7.3 kHz |
| 10k | 1n0 | 73 kHz |

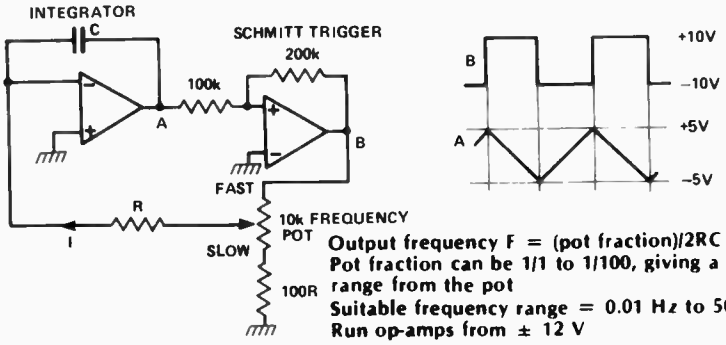
## Wien Bridge Oscillator

Output frequency $F = \frac{1}{2\pi RC}$ Hz




The RA53 is a negative temperature coefficient thermistor; it sets $A_V$ to 3 for stable oscillation.

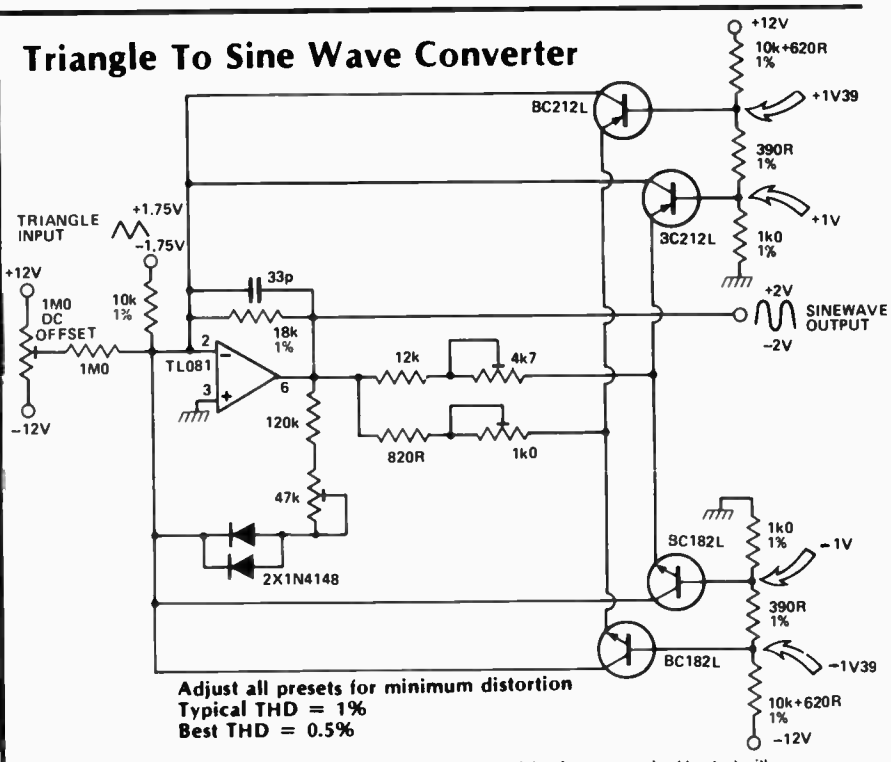
## Triangle/Square Wave Oscillator




Output frequency F = (pot fraction)/2RC
Pot fraction can be 1/1 to 1/100, giving a 100 to 1 range from the pot
Suitable frequency range = 0.01 Hz to 50 kHz
Run op-amps from ± 12 V

This oscillator provides both triangle and square wave outputs at a frequency that can be varied over a range set by the 10k pot. A dual op-amp such as the TL072 is suitable and would provide frequencies to beyond 50 kHz.

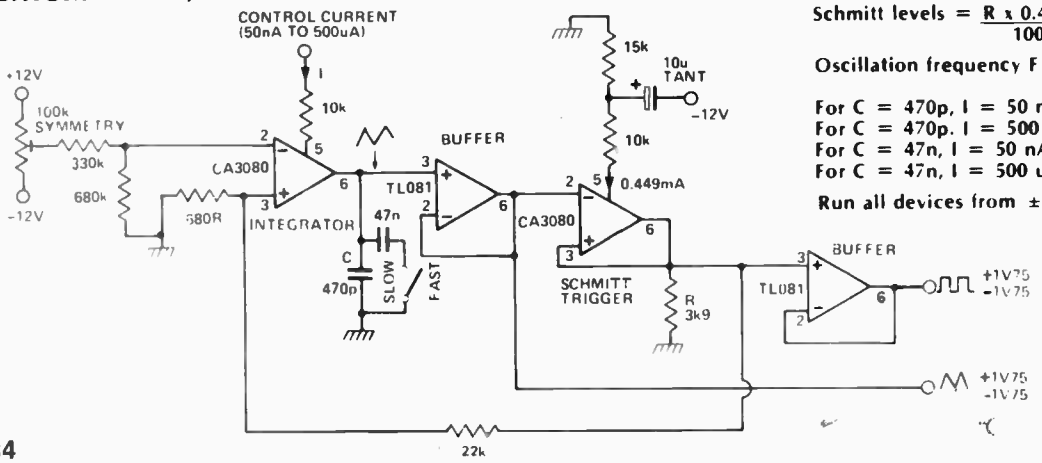
## Triangle To Sine Wave Converter




Adjust all presets for minimum distortion
Typical THD = 1%
Best THD = 0.5%

When designing a complete function generator it is often convenient to start with one of the triangle/square wave oscillators given earlier and convert the triangle wave into a sinewave. This is a particularly good method if a sweep oscillator is required, since sinewave sweep oscillators are extremely difficult to design. Some experimenting with the preset pots is necessary to obtain minimum distortion, although this is not particularly difficult.

## Linear VCO/Function Generator




Schmitt levels = $\frac{R \times 0.449}{1000}$ = 3.9 x 0.449 = ± 1V75

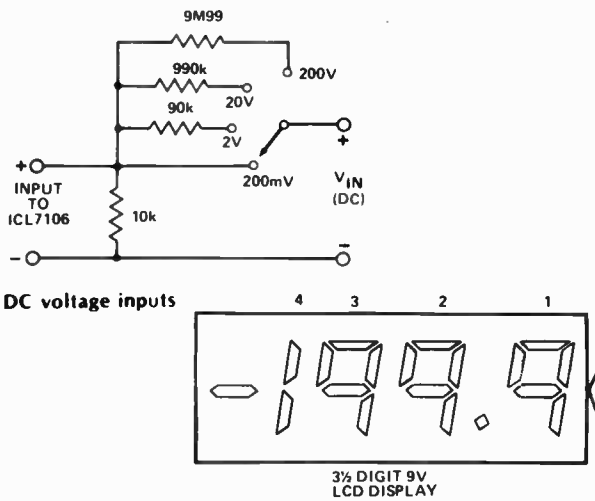
Oscillation frequency F = I/(C x 4 x 1.75) = I/7C Hz

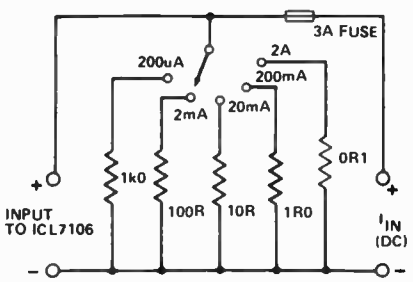
For C = 470p, I = 50 nA, F = 15 Hz
For C = 470p, I = 500 uA, F = 150 kHz
For C = 47n, I = 50 nA, F = 0.015 Hz
For C = 47n, I = 500 uA, F = 150 Hz

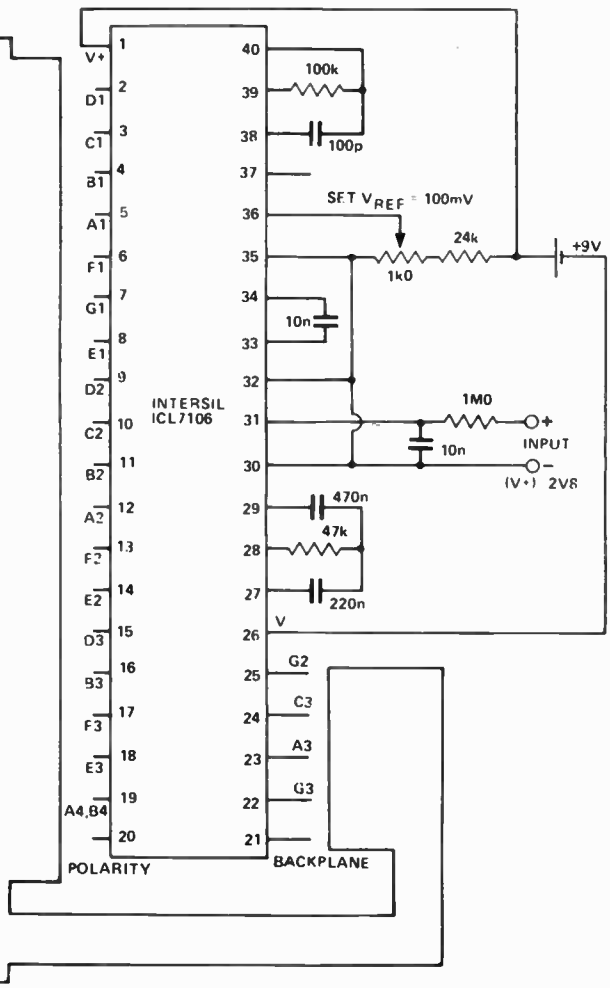
Run all devices from ± 12 V

# MEASUREMENT

## 3½ Digit LCD DVM



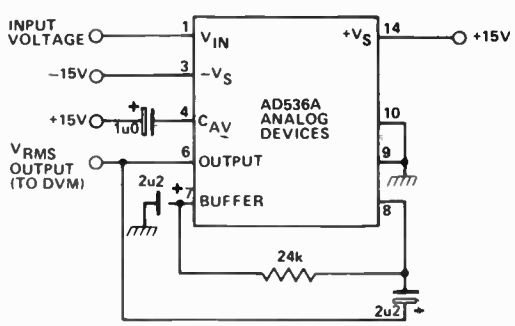

**Input voltage range = ±200 mV**
**Quiescent current = 0.8 mA**
**Common mode input range = (V+)−0V5 to (V−)+1V**
**Decimal point must be driven externally by EXORing the decimal point data with the backplane strobe**

The Intersil ICL7106 is a high-performance CMOS 3½-digit analogue-to-digital converter capable of driving a liquid crystal display directly. The device uses dual-slope integration to ensure accurate performance independent of component variation. The accuracy is guaranteed to ± 1 count in 2000 counts and draws only 10 mW from a 9 V battery. Intersil market a 'Single Chip Panel Meter Evaluation Kit' that contains all the necessary components for this circuit.

## True RMS Measurement

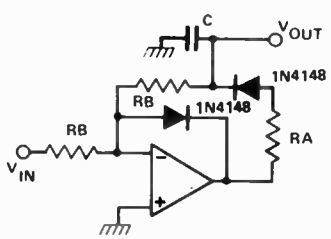
**Input voltage 7 $V_{RMS}$ maximum**
**Bandwidth: 300 kHz, $V_{RMS}$ > 0V1**
**Error of 1% for a crest factor of 7**

**Quiescent current = 1mA**
**60 dB range**



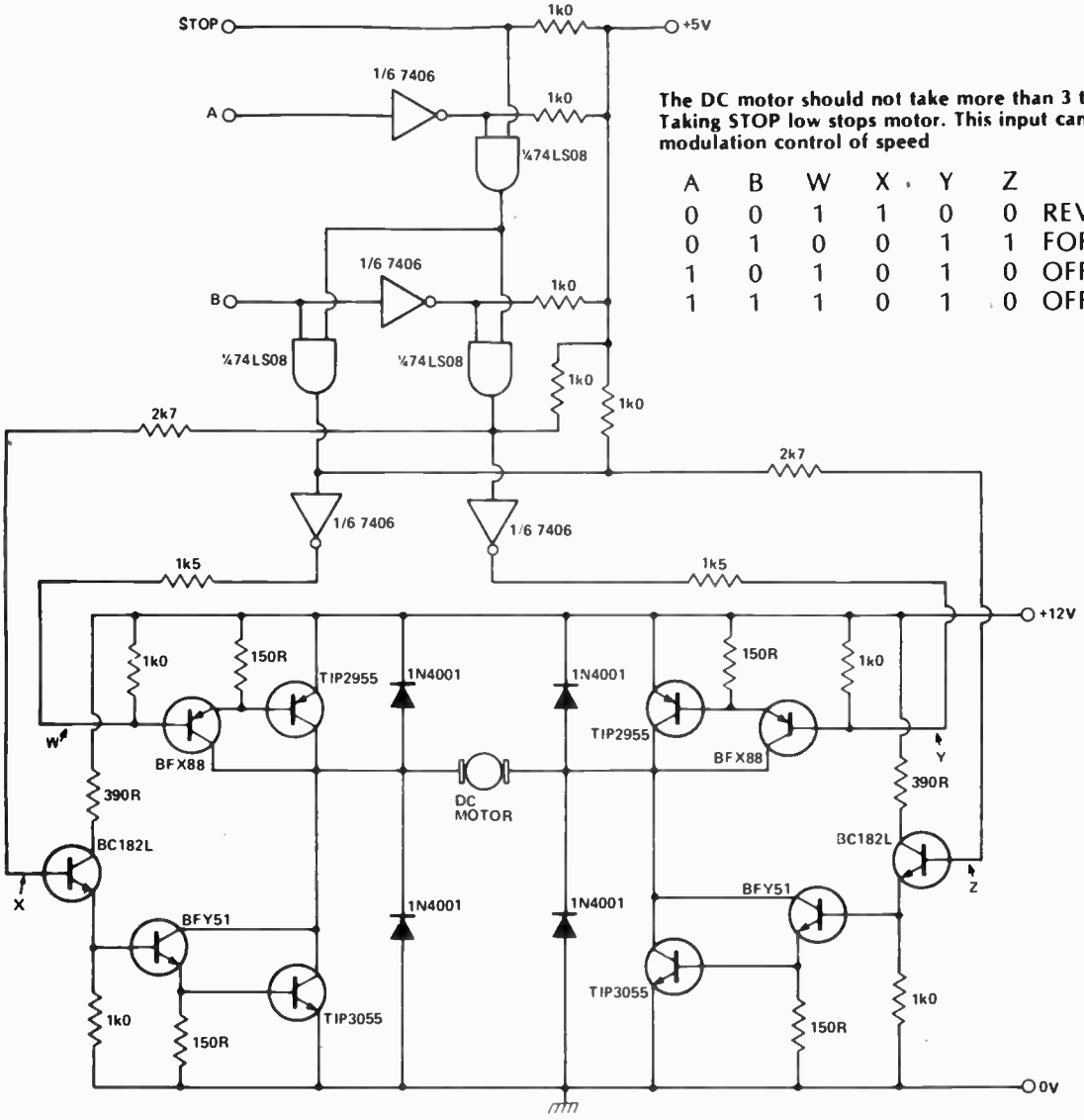

## Inverting Peak Voltage Detector

**Attack time constant = C.RA**
**Decay time constant = C.RB**




**This circuit works well at high frequencies**

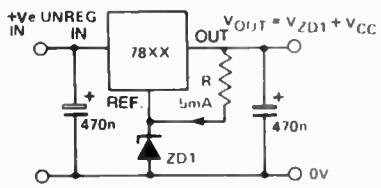
## Heavy Duty DC Motor Control




The DC motor should not take more than 3 to 4 A continuous current Taking STOP low stops motor. This input can be used for mark/space modulation control of speed

| A | B | W | X | Y | Z | |
|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | REVERSE |
| 0 | 1 | 0 | 0 | 1 | 1 | FORWARD |
| 1 | 0 | 1 | 0 | 1 | 0 | OFF |
| 1 | 1 | 1 | 0 | 1 | 0 | OFF |

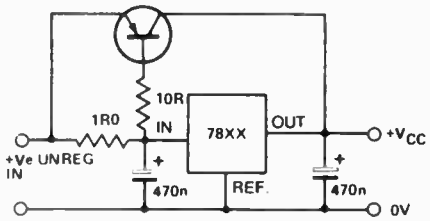
## Increasing Regulator Voltages




**Increasing the output voltage using a zener diode.**

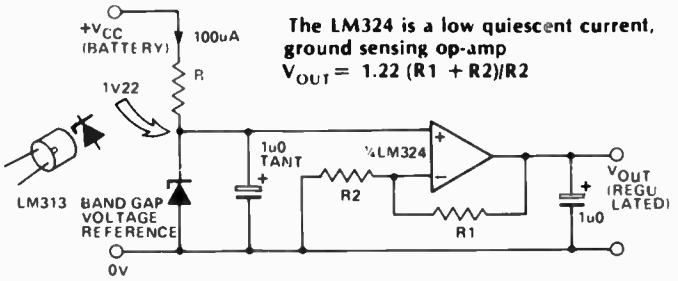
The output voltage of three-terminal voltage regulators can be increased by increasing the voltage on the reference or common lead on the regulator. This can be done as shown in the circuit diagram with the use of a zener diode. The resistor R should be selected to ensure sufficient current through the zener for a stable voltage reference.

## Increasing Regulator Currents




**Using a bypass transistor to increase the output current drive. The first 600 mA flows through the regulator, the rest via the external transistor.**

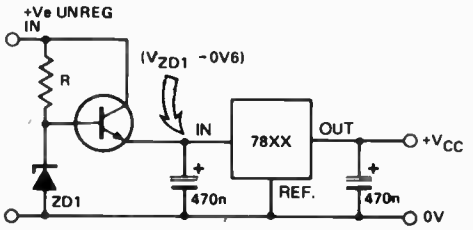
## Low Current/Precision Supply




**The LM324 is a low quiescent current, ground sensing op-amp**
**$V_{OUT}$ = 1.22 (R1 + R2)/R2**

This circuit is useful whenever a precision voltage reference is necessary or as a low current, well-regulated supply. The value of the resistor R is calculated from the battery voltage to ensure around 1 uA through the LM313. Use the equation R = $V_{cc}$ x 1000 ohms.

## Low Dissipation Regulator

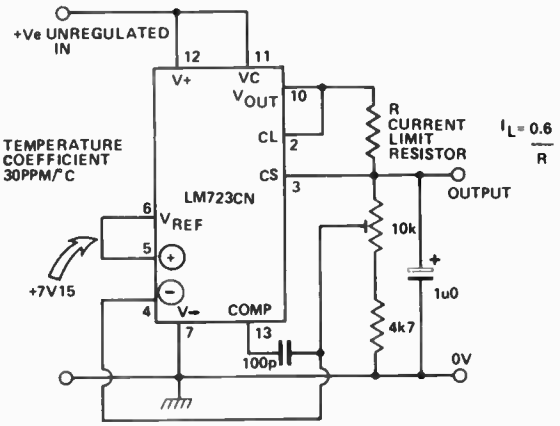



The three-terminal IC regulator is probably the most-used integrated circuit, offering a simple and effective solution to the problem of power supply design. These devices, however, have a maximum input voltage of around 35 V (40 V for some). The circuit shown here enables the regulator to function from a higher supply voltage by dropping the excess voltage across an external transistor. You should ensure that the voltage drop across the transistor is within the capabilities of the particular device used. The zener diode ZD1 sets the voltage that appears at the input of the IC regulator. (The actual voltage will be ZD1-0.6). The resistor R should be selected to ensure adequate current through the zener diode so that it will provide an effective voltage reference for the pass transistor. This is determined by the maximum power dissipation of the zener. Set the required power dissipation for the zener at about half its maximum rating then calculate the required zener current from Ohm's law; i.e: I = P/ZD1. The value of the required resistor is then given by R = (V e−ZD1)/I.

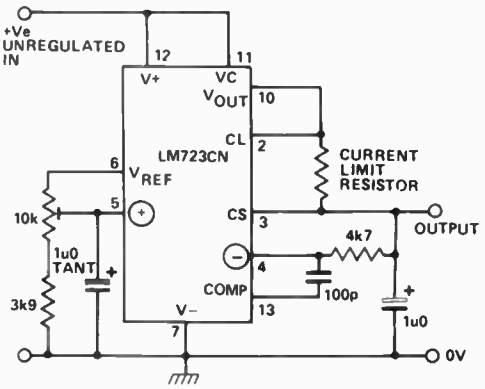
The circuit can also be used to decrease the power dissipation in the IC regulator. These require an input at least 2 - 3 volts above their rated output voltage. If this voltage is set by the zener the remainder of the power dissipation will be done by the pass transistor. Once again, ensure that the maximum power dissipation expected of the transistor is within its capability. If the device becomes excessively hot an additional heatsink should be used.

## Precision Power Supplies

**723 general specifications:**
**Maximum input voltage = 40 V**
**Maximum current output = 150 mA**
**Output voltage range = 2 to 37 V**



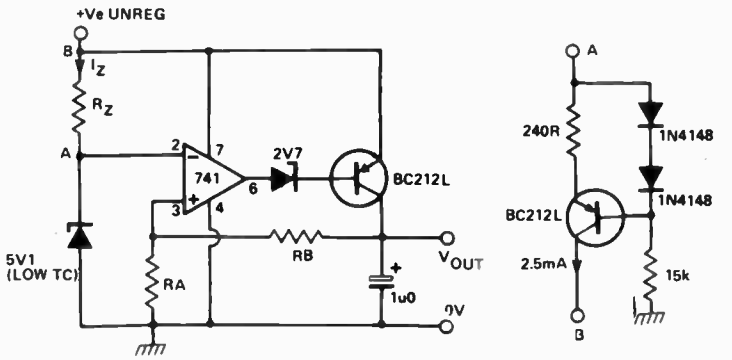

**Adjustable +7 V to +21 V**




**Adjustable +2 V to +7 V**

The 723 is a precision, variable voltage regulator. Output voltage is adjusted by the 10k preset and a current limit can be set by a suitable choice of resistor R.

## Battery Regulator




**Better regulation can be obtained by replacing RZ with this 2.5 mA current source. However, the unregulated supply rail must not drop below (5V1 + 1V2) = 6V3**

**Select $R_z$ for an $I_z$ of about 2.5 mA**

**$V_{OUT}$ = 5V1 X (RA + RB)/RA**

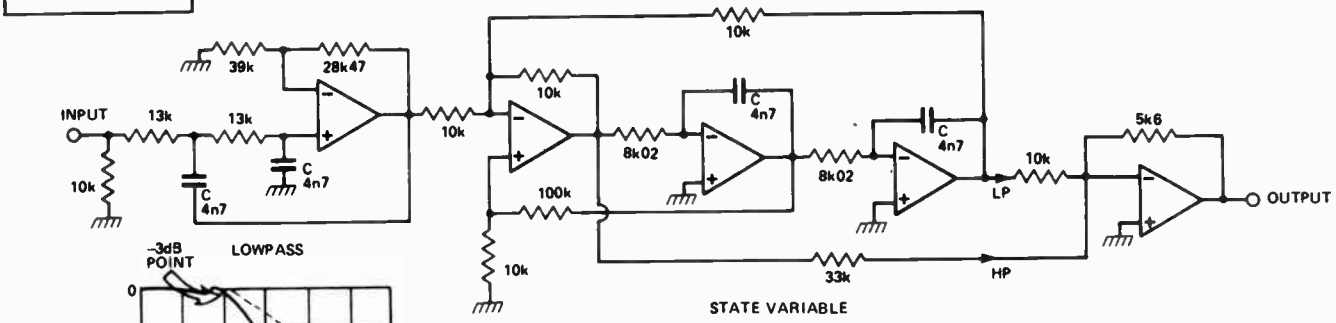
**Minimum $V_{OUT}$ ~6V**

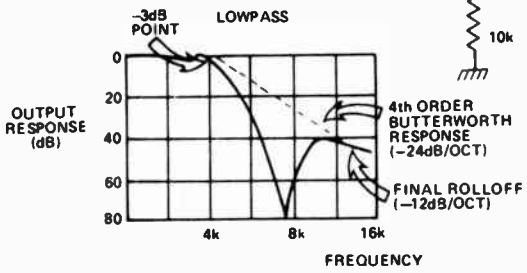
**Dropout voltage = $V_{CE}$(Q1 saturated) ~ 0V3**

**Keep $I_{OUT}$ less than 50 mA**

**A very low dropout voltage can be obtained by allowing Q1 to saturate. This gives maximum lifetime on battery power.**

# FILTERS




## 4th Order Elliptic lowpass

**Cutoff frequency is 4 kHz. To change cutoff frequency, scale capacitor C (four off)**

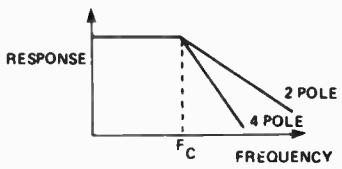
## Lowpass Active Filters

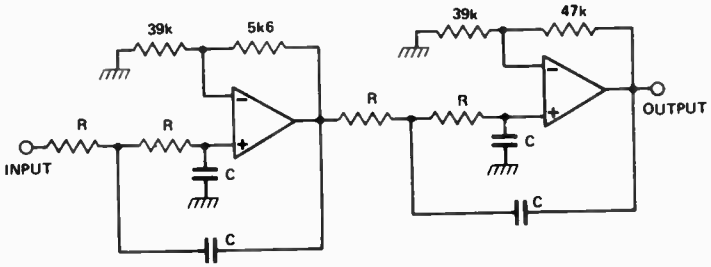
**Inputs must have a DC path to ground**

$$F_c = \frac{1}{2\pi RC}$$

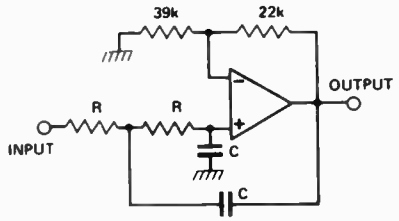
**2 pole roll-off = −12 dB/octave**
**4 pole roll-off = −24 dB/octave**

| R | C | $F_C$ |
|---|---|---|
| 107k | 15n | 100 Hz |
| 10k7 | 15n | 1 kHz |
| 10k7 | 1n5 | 10 kHz |



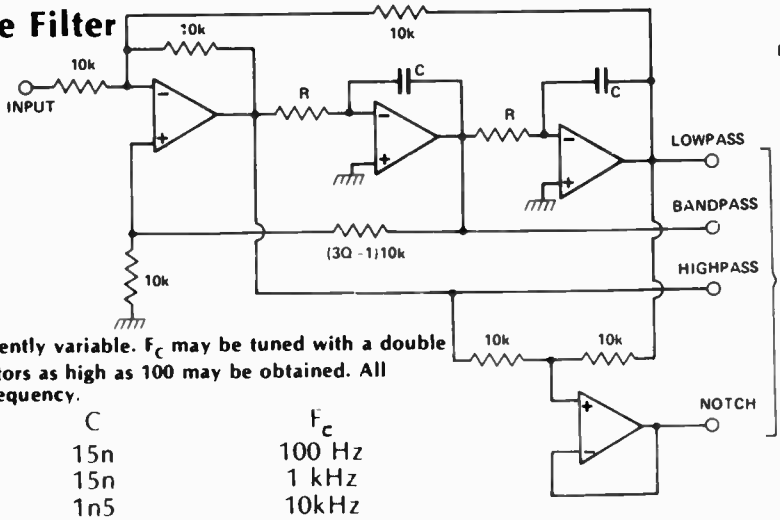

**4 pole Butterworth**

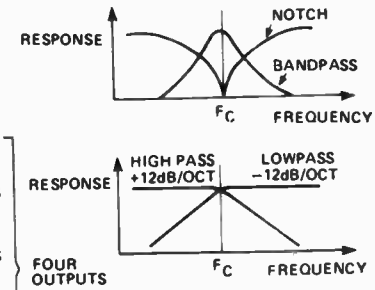



**2 pole Butterworth**

## State Variable Filter

$$F_c = \frac{1}{2\pi RC} \text{ Hz}$$



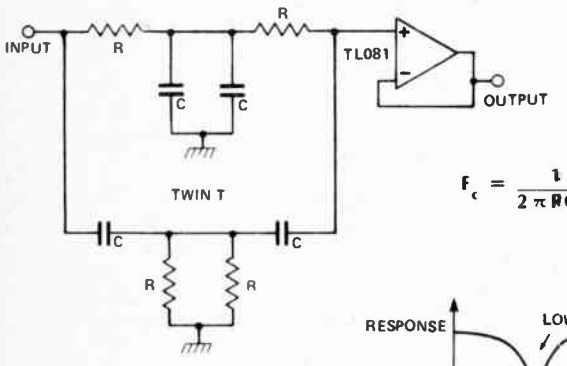




**Gain = Q**
**Q and $F_C$ are independently variable. $F_C$ may be tuned with a double gang pot (for R). Q factors as high as 100 may be obtained. All responses track with frequency.**

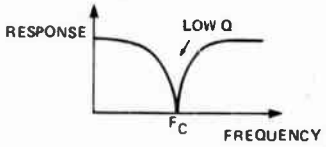
| R | C | $F_C$ |
|---|---|---|
| 107k | 15n | 100 Hz |
| 10k7 | 15n | 1 kHz |
| 10k7 | 1n5 | 10kHz |

## Active Notch Filter

**The two R's in parallel represent R/2**
**The two C's in parallel represent 2C**
**For 50 Hz, R = 680k, C = 4n7 (a hum remover)**

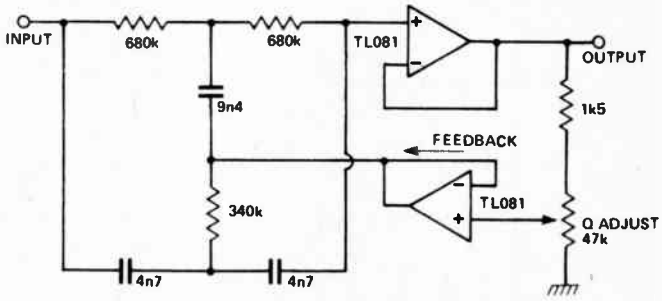


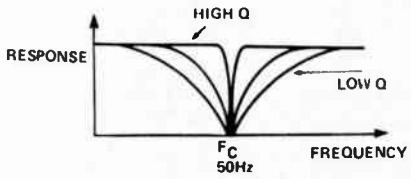

$$F_c = \frac{1}{2\pi RC}$$




A basic Twin-Tee notch. Rejection depends on component matching, so for best results use high-stability components.

## 50 Hz Notch, Variable Q

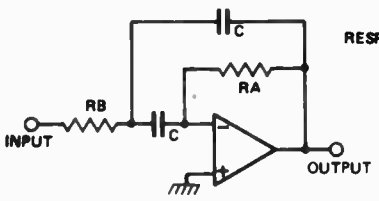


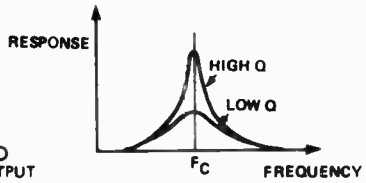




This is a modified version of the basic Twin-Tee notch filter. The Q can be adjusted by controlling the amount of feedback with the 47k potentiometer. The rejection offered by the circuit is determined by the matching of the passive components, but even with ordinary components a figure of 30 dB to 40 dB should be obtained.

## Bandpass Active Filter

$F_C = 1/2\pi C\sqrt{RA+RB}$
$Q = 1/2\sqrt{RA/RB}$
**Gain $= 2Q^2$**




$F_C$ = 1kHz, C = 15n

| RA | RB | Q | GAIN |
|---|---|---|---|
| 10k6 | 10k6 | 0.5 | x 0.5 |
| 21k2 | 5k3 | 1.0 | x 2.0 |
| 42k4 | 2k65 | 2.0 | x 8.0 |
| 84k8 | 1k32 | 4.0 | x 32.0 |

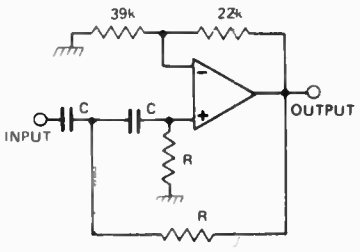
This is probably the most common bandpass filter. The circuit is really only useful for the relatively low Q shown. For a higher Q one of the more complex bandpass circuits should be used, such as the state variable filter.

## Highpass Active Filters

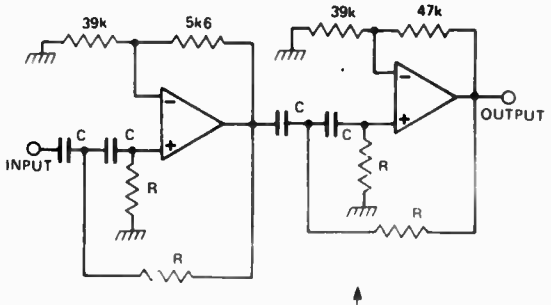
$$F_c = \frac{1}{2\pi RC} \text{ Hz}$$

2 pole roll-off = +12 dB/octave
4 pole roll-off = +24 dB/octave

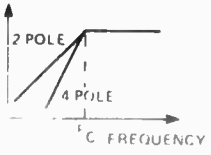
| R | C | F |
|---|---|---|
| 107k | 15n | 100 Hz |
| 10k7 | 15n | 1 kHz |
| 10k7 | 1n5 | 10 kHz |




2 pole Butterworth

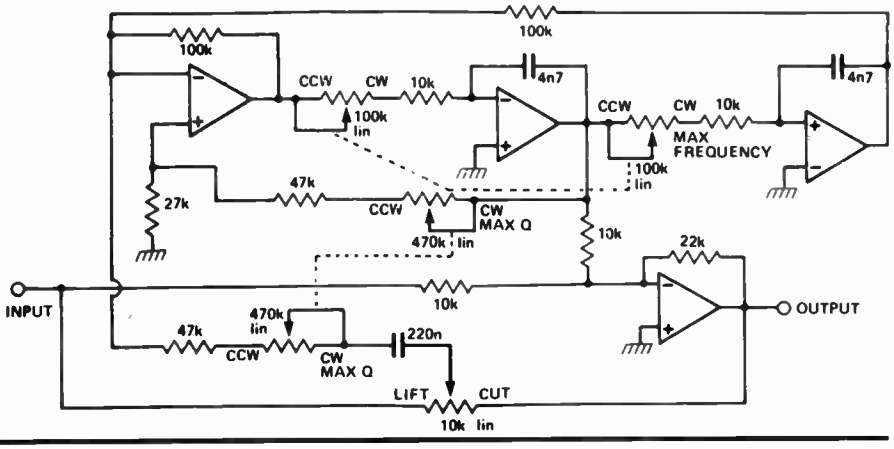



4 pole Butterworth

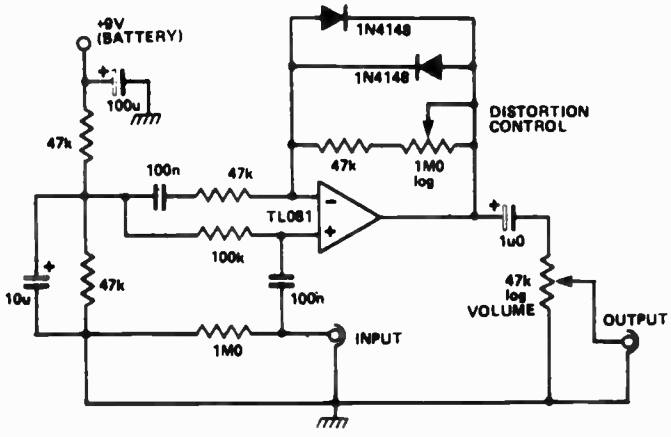


# MUSICAL

## Parametric Equaliser

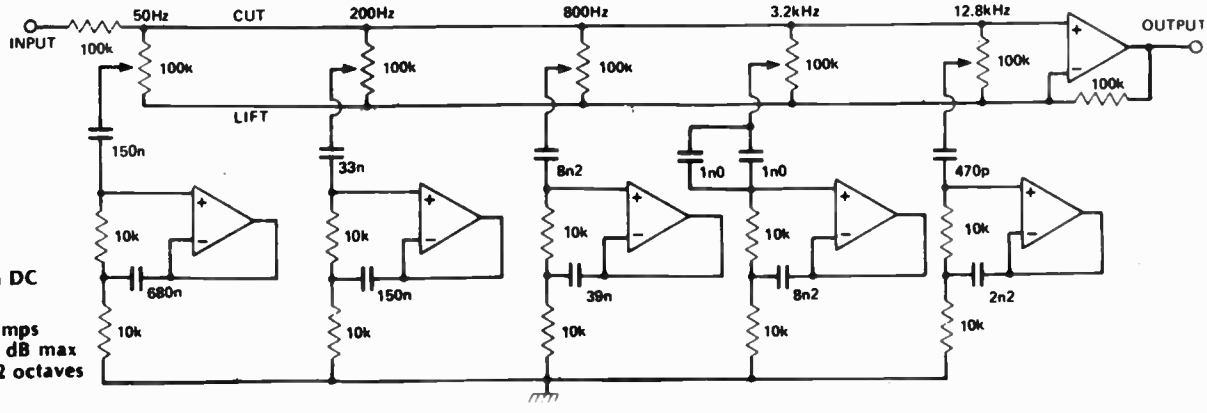




## Fuzz Unit For Guitar



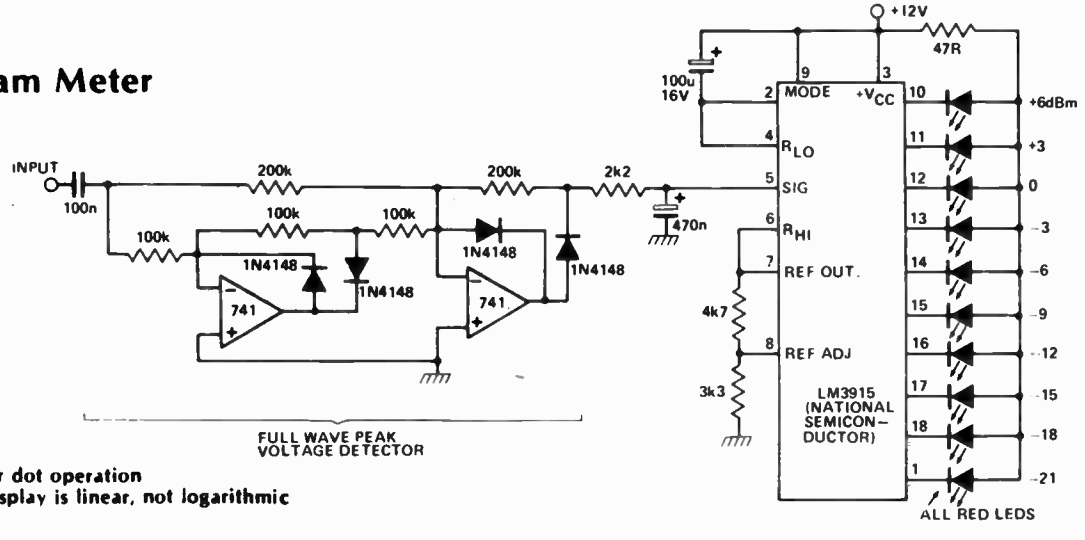

**The battery can be switched on via the jack socket (a stereo jack can be used).**

## Graphic Equaliser




**Input must have a DC path to ground**
**Use 741's for op-amps**
**Cut and lift = 13 dB max**
**Filter spacing = 2 octaves**

## LED Peak Program Meter

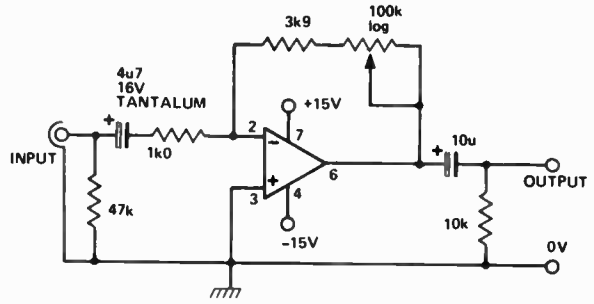



**Leave pin 9 open circuit for dot operation**
**If an LM3914 is used the display is linear, not logarithmic**

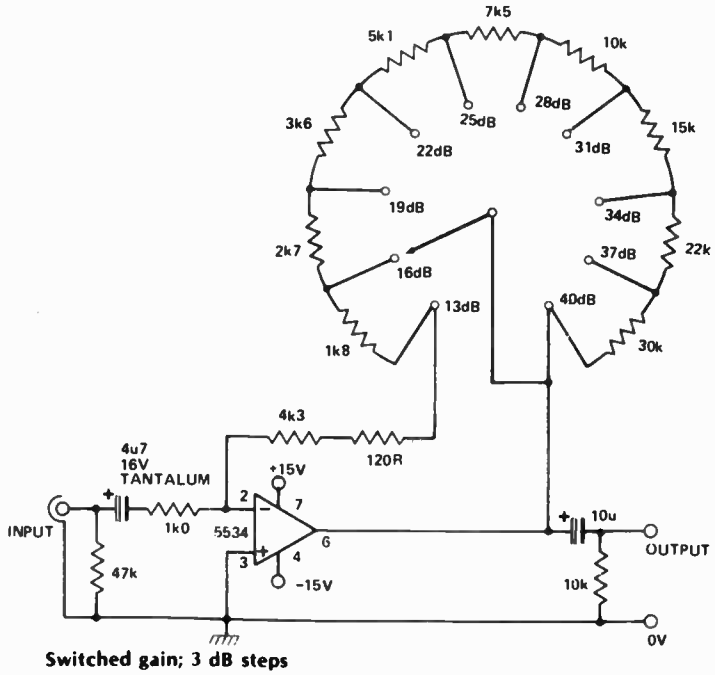
# AUDIO

## Low Impedance Source Preamp

**Very low input noise**
**Input noise = 4 nV$\sqrt{Hz}$**
**Equivalent input noise voltage = 0.56 $uV_{RMS}$ (20 kHz bandwidth)**
**Input impedance = 1k0 (suitable for microphone)**




**Variable gain; x 3.9 to x 100 (12 dB to 40 dB)**

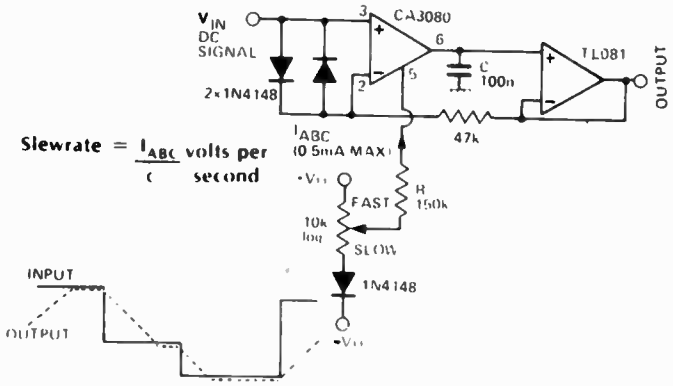



**Switched gain; 3 dB steps**

The NE5534N is a very low-noise op-amp specifically intended for audio applications. The device boasts one of the lowest noise figures of all op-amps combined with good slew rate and large signal bandwidth figures.

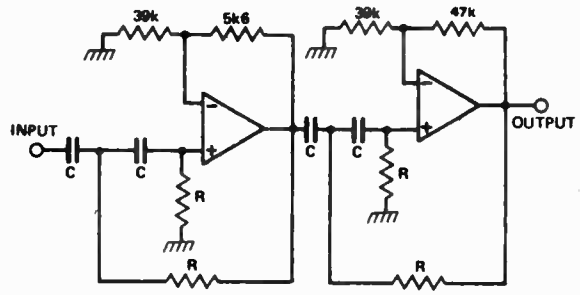
The lowest-noise devices have the designation NE5534AN. Suitable supply decoupling is essential if best results are to be obtained.

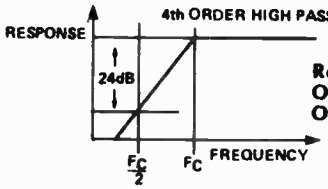
## Slew Limiter




Slewrate = $\frac{I_{ABC}}{C}$ volts per second

## Rumble Filter



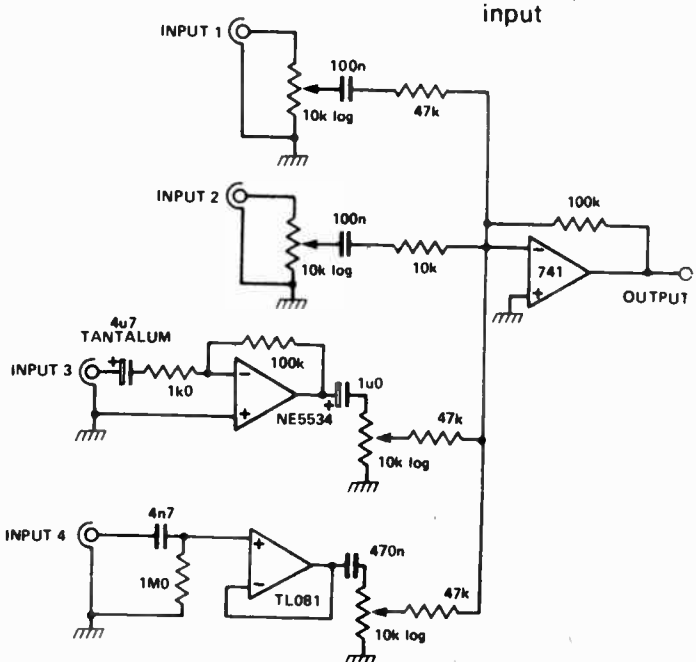




**Roll-off slope = 24dB/octave**
**Overall voltage gain = x 2.6 (8.3 dB)**
**Op-amps are 741's or RC4558**

| $F_C$ | C | R |
|---|---|---|
| 25 Hz | 100n | 62k |
| 50 Hz | 100n | 30k |
| 100 Hz | 100n | 15k |
| 200 Hz | 100n | 7k5 |
| | (5% tolerance) | |

## Simple Mixer

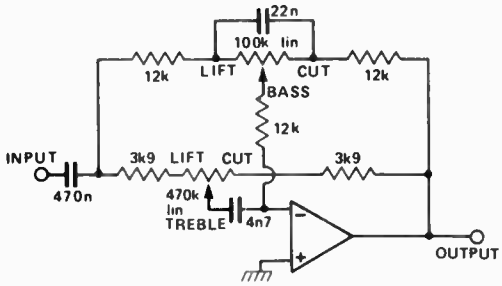
| INPUT | MAX GAIN | INPUT IMPEDANCE | SOURCE |
|---|---|---|---|
| 1 | +6 dB | 10k | line level |
| 2 | +20 dB | 5 to 10k | line level |
| 3 | +46 dB | 1k0 | low impedance microphone |
| 4 | +6 dB | 1M0 | high impedance input |




This simple mixer has been provided with four different types of input circuit. Any combination of these could however be used. Once again, the 741 limits the high frequency response and slew rate capabilities. To improve performance substitute the 741 for a faster device such as an NE5534N or TL071, etc.

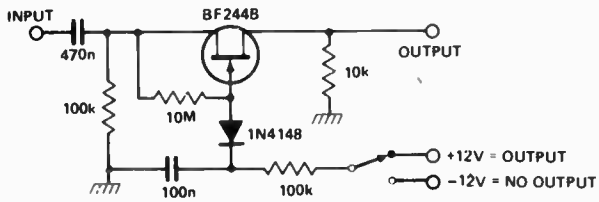
# AUDIO

## Bass And Treble Tone Control

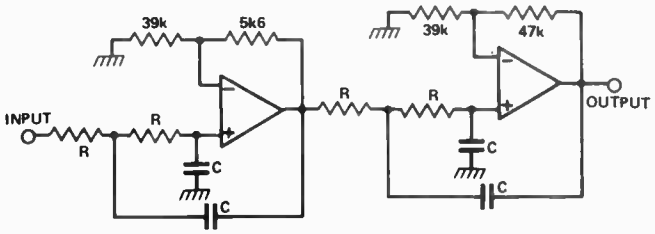



The op-amp can be any type suitable for audio work, e.g: TL071, NE5534N, etc.

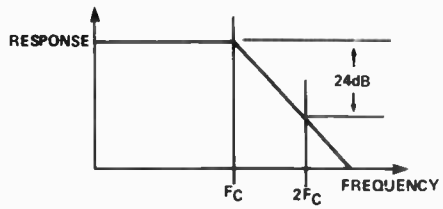
## FET Audio Switching




## Scratch Filter



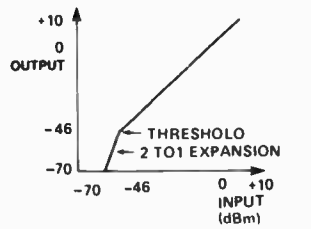

4th ORDER LOW PASS




**Input must have a DC path to ground**
**Roll-off slope = 24 dB/octave**
**Overall voltage gain = x 2.6 (8.3 dB)**
**Op-amps are 741's or RC4558**

| $F_C$ | C | R |
|---|---|---|
| 10 kHz | 1n5 | 10k |
| 7.5 kHz | 1n5 | 14k |
| 5 kHz | 1n5 | 20k |
| | (5% tolerance) | |

## Low Level Noise Gate/Expander




**Threshold = RB/RA $V_{pp}$**

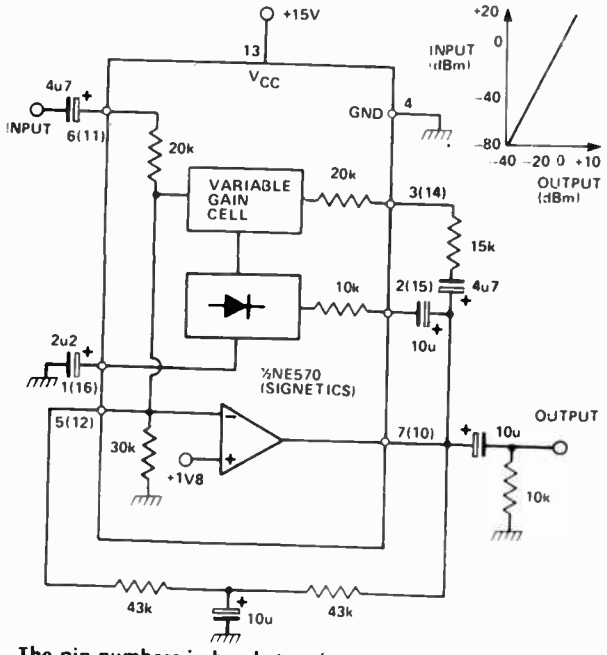



| RA/RB | THRESHOLD | |
|---|---|---|
| 30 | 33 $mV_{pp}$ | (−36 dBm) |
| 100 | 10 $mV_{pp}$ | (−46 dBm) |
| 300 | 3.3 $mV_{pp}$ | (−56 dBm) |

0 dBm = 2.2 $V_{pp}$

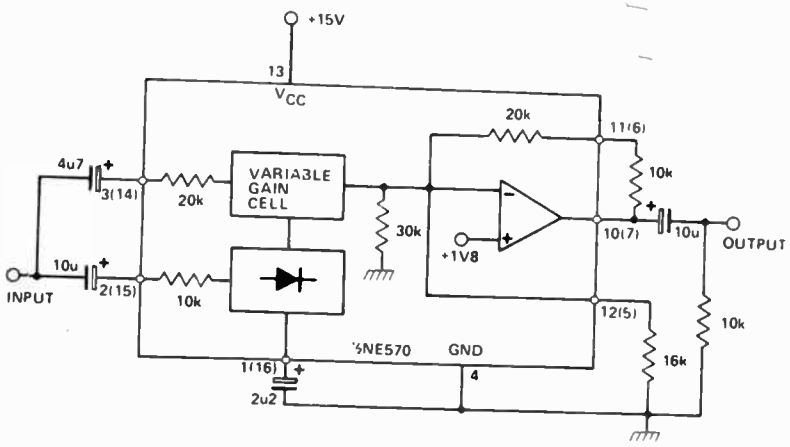
**RC increases the expansion rate, turning the unit into a noise gate.**
**With RC = 100k the effect is very abrupt; withRC = 10M the effect is very subtle.**

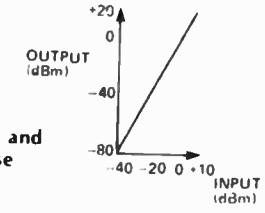
## Two-to-one Compressor




The pin numbers in brackets refer to the second circuit in the IC. Circuit can be used as a preconditioner in a noise reduction system.

## Two-to-one Expander

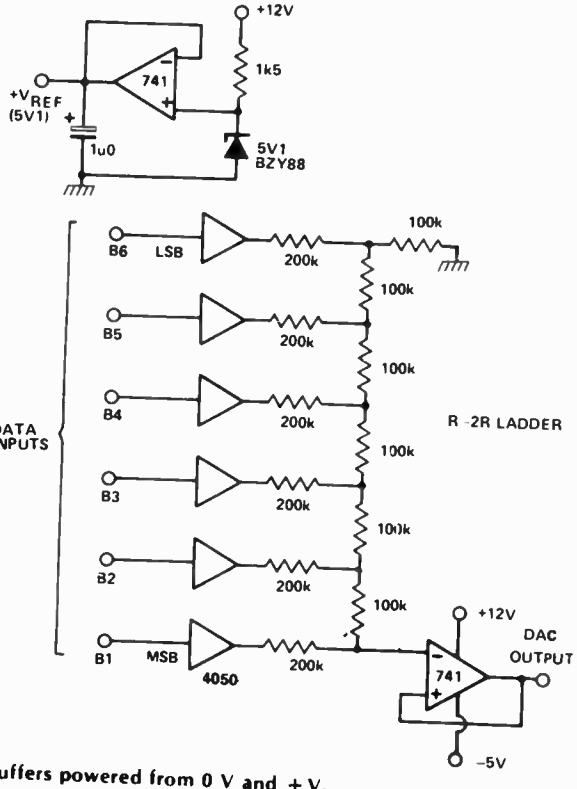


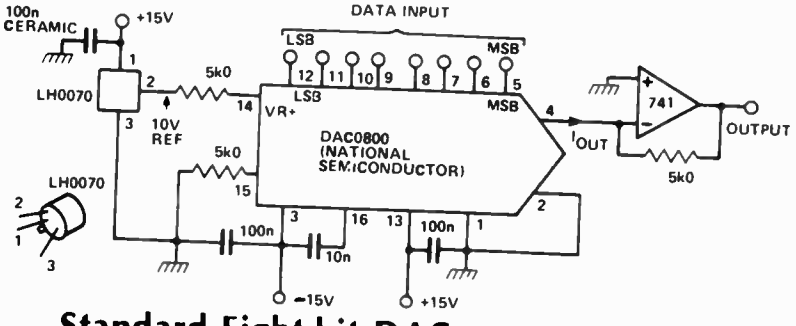

Circuit can be used to expand previously compressed signals, and hence to effect an overall noise reduction

# DIGITAL

## Six-bit DAC — 10-bit Precision

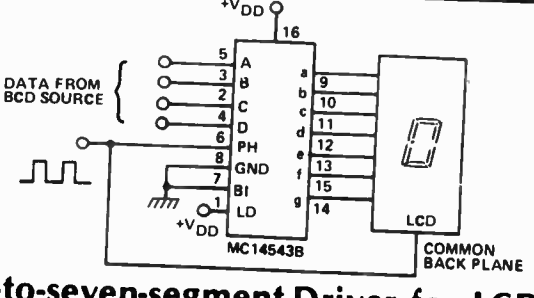



Buffers powered from 0 V and $+V_{REF}$
Resistors in ladder need 0.1% tolerance
DAC output has 64 steps




## Standard Eight-bit DAC

The DAC08 is a multiplying digital-to-analogue converter (DAC). The data input selects a number that is multiplied by the input reference current to determine the output current. For accurate results it is therefore necessary to supply the DAC with a reference current. This role is filled by using the LH0070 precision voltage reference and generating a reference current by dropping this voltage across an accurate resistance, the 5k0. If this accuracy is not important or if the LH0070 is difficult to obtain a zener diode or three-terminal voltage regulator could be substituted.

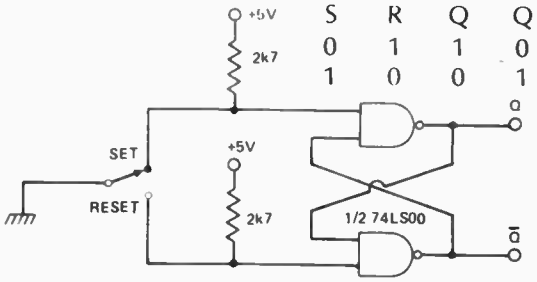



## BCD-to-seven-segment Driver for LCD

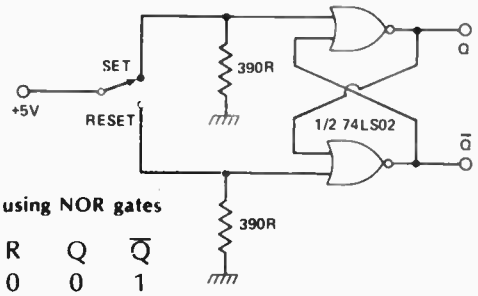
The use of liquid crystal seven-segment displays is becoming increasingly popular due to their low power consumption when compared with LED displays. A problem with LCD arises, however, due to its inability to cope with dc drive. The common or backplane must be supplied with a square wave to ensure that the display is not damaged. This circuit provides this function as well as the necessary BCD-to-seven-segment decoding.

# Debouncing Using Flip-Flops

Flip-flop using NAND gates



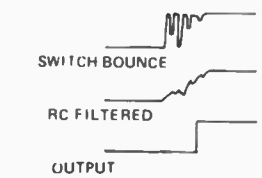

| S | R | Q | Q |
|---|---|---|---|
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |

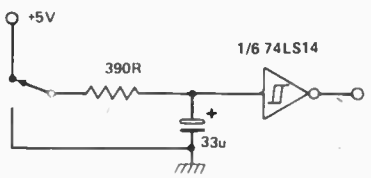


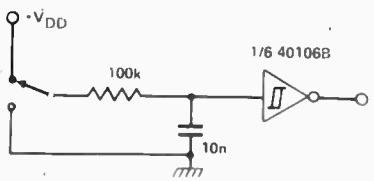

Flip-flop using NOR gates

| S | R | Q | $\overline{Q}$ |
|---|---|---|---|
| 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 |

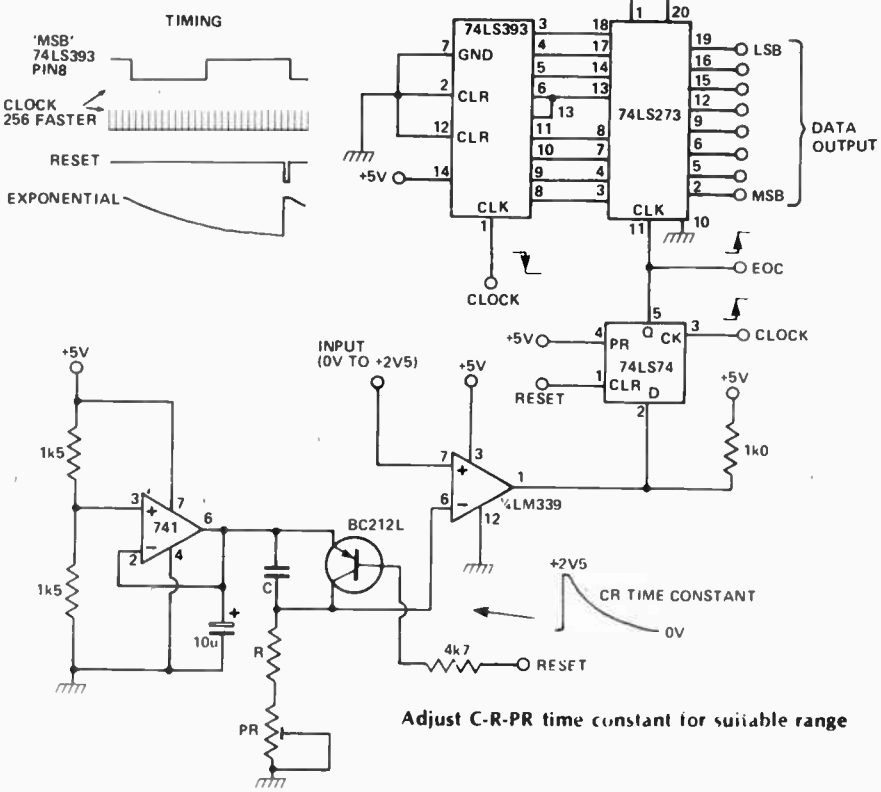
# Debouncing Using Schmitt Triggers



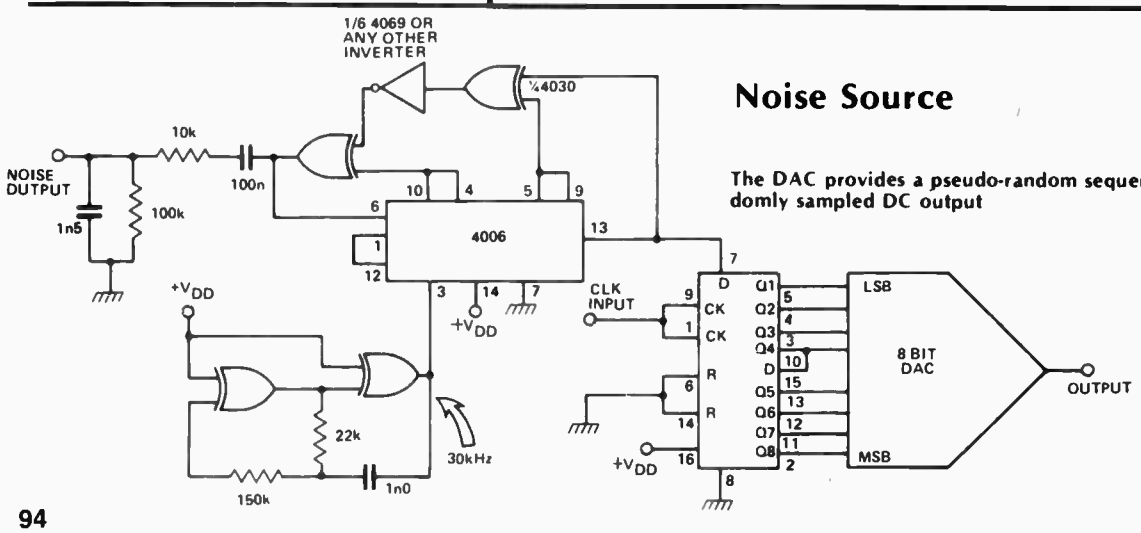




# Logarithmic ADC

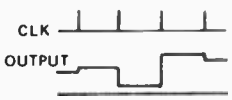



Adjust C-R-PR time constant for suitable range

# Noise Source

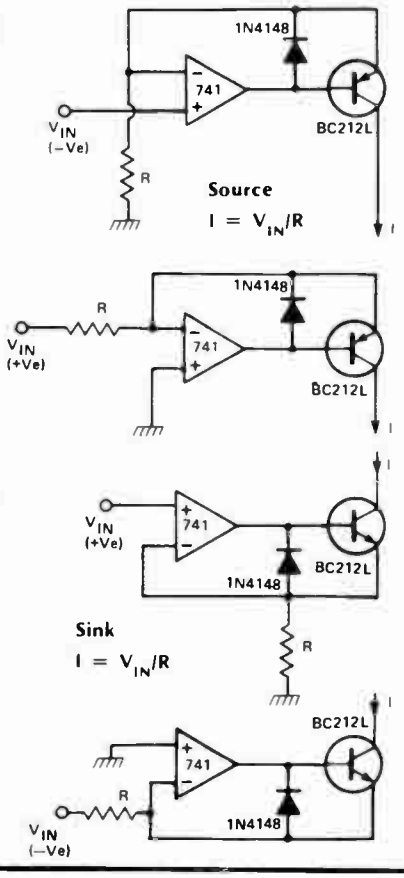


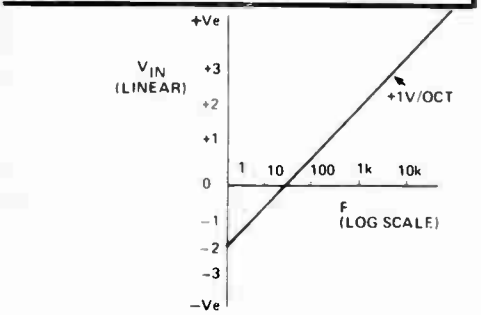

The DAC provides a pseudo-random sequence generator, with a randomly sampled DC output



# BUILDING BLOCKS

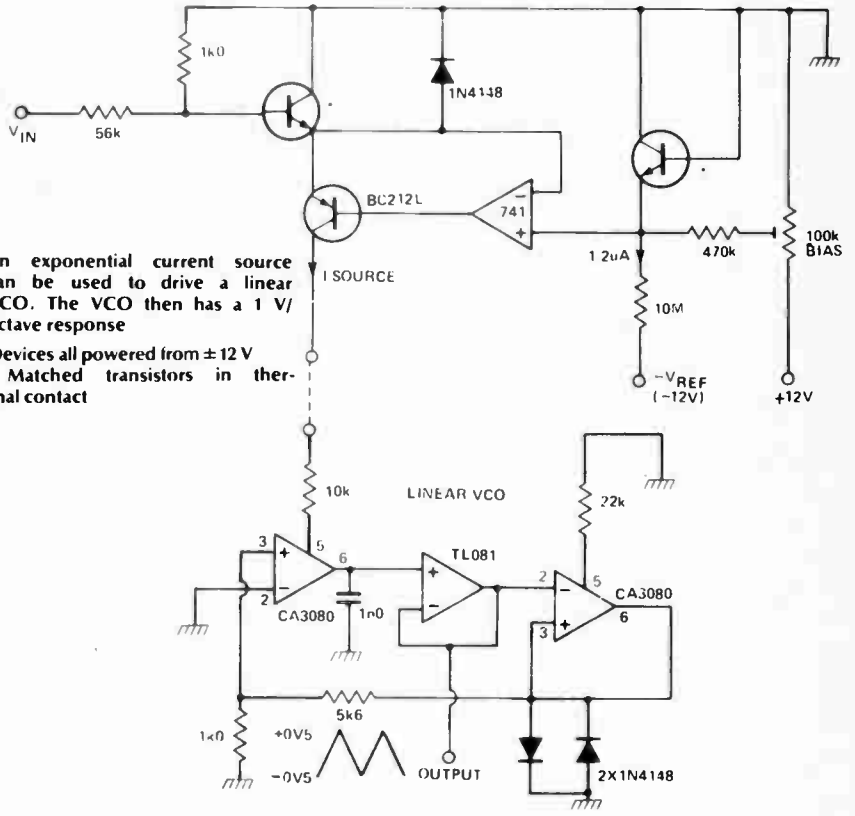
## Voltage-to-current Converters




Frequency response of a linear VCO driven by an exponential current sink

## Exponential Current Source

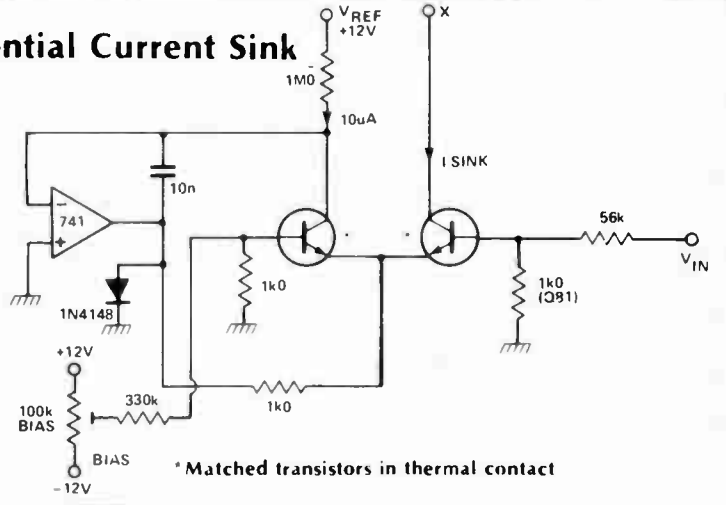



An exponential current source can be used to drive a linear VCO. The VCO then has a 1 V/octave response

Devices all powered from ± 12 V

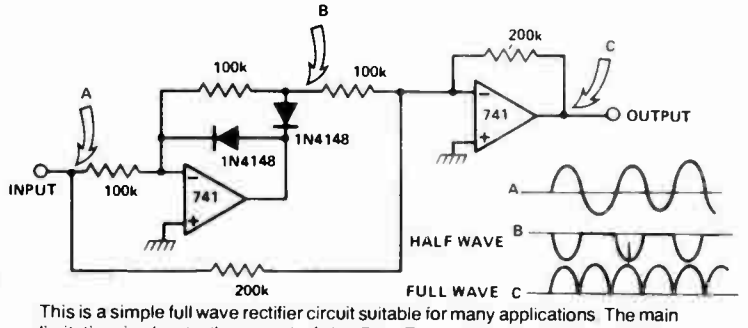
* Matched transistors in thermal contact

## Exponential Current Sink

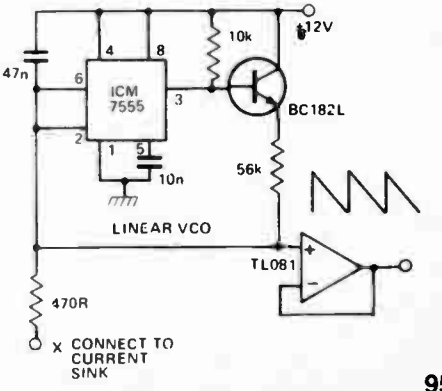



*Matched transistors in thermal contact

## Precision Full Wave Rectifier

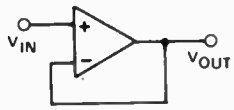



This is a simple full wave rectifier circuit suitable for many applications. The main limitation is due to the speed of the 741. For use above about 10 kHz an alternative op-amp should be used, such as the TL072.

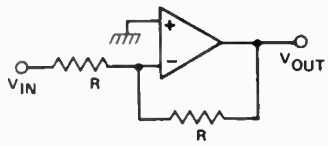


## BUILDING BLOCKS

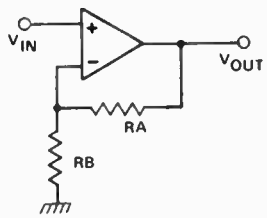
# Basic Op-amp Building Blocks



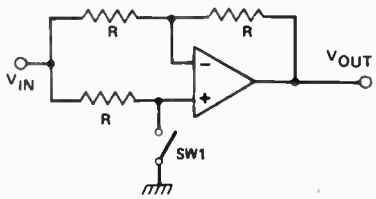

Voltage follower/buffer
Input must have a DC path to ground



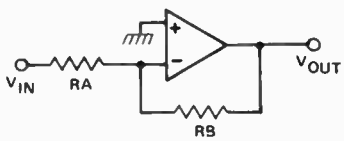

Inverter
Voltage gain = −1
input impedance = R




Non-inverting amplifier
Input must have a DC path to ground
Voltage gain = (RA + RB)/RP



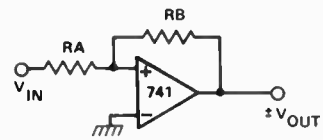

Inverter/non-inverter amplifier
Voltage gain = +1 with SW1 open
Voltage gain = −1 with SW1 closed



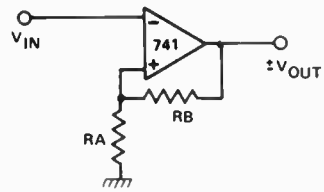

Inverting Amplifier
Voltage gain = −RB/RA
Input impedance = RA

The power supply and compensation are omitted from these diagrams. If internally compensated devices are used no additional compensation is necessary, i.e: 741, TL071, TL072, TL074, etc. If additional compensation is required consult the data sheets on the particular device used.

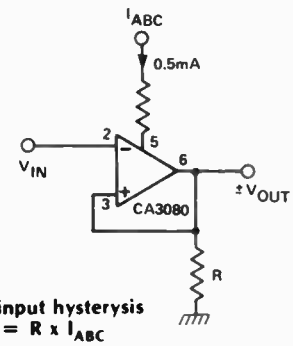
## Schmitt Triggers




Non-inverting; input hysterysis levels = ±(RA/RB)) x $V_{OUT}$




Inverting; input hysterysis levels = ±(RA/(RA + RB)) x $V_{OUT}$
Note that $V_{OUT}$ depends on the supply voltage and the individual op-amp

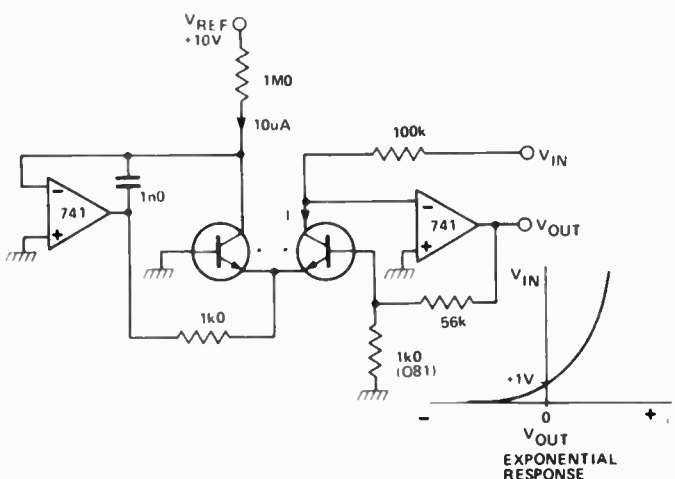



Transconductance type; input hysterysis levels = ±$V_{OUT}$; $V_{OUT}$ = R x $I_{ABC}$
R can be replaced by two 1N4148 diodes back-to-back

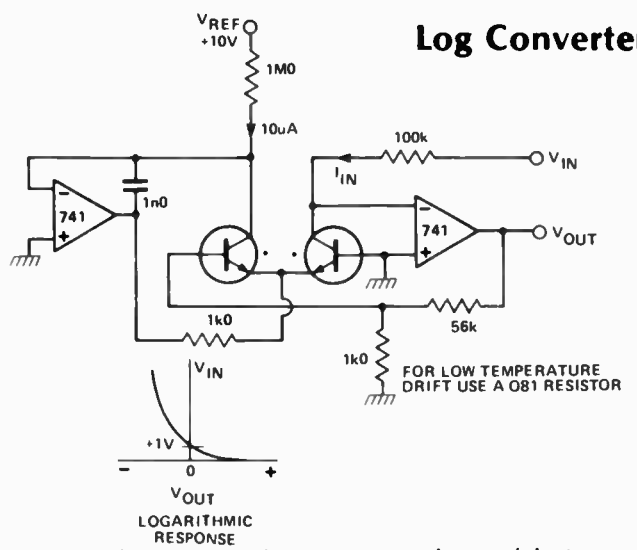
When trying to convert a slowly changing voltage into a step function with a well-defined leading edge a good Schmitt trigger is invaluable. This is a simple but effective trigger capable of good results in the audio passband. Once again, for higher frequency use substitute a faster op-amp for the 741. The Schmitt trigger works by using positive feedback to establish a 'deadband', a range of input voltages within which the output state will not change. The input voltage must exceed the higher limit in order to force the output high. Similarly, the input voltage must be taken below the lower limit to force the output low. The extent of this deadband is given in the equations.

## Antilog (Exponential) Converter

$V_{OUT}$ = I x 100k
The current I doubles for every 1 V increase of $V_{IN}$
When $V_{IN}$ = 0 V, I = 10 uA




## Log Converter

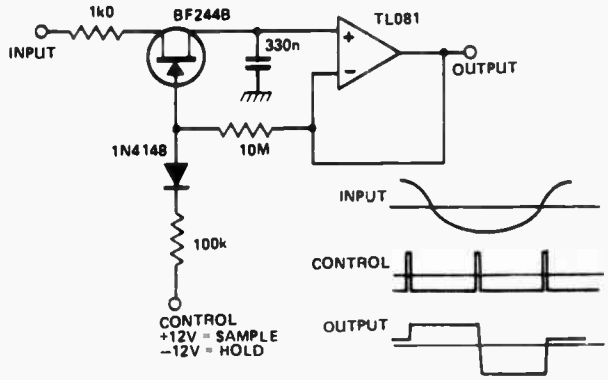



$V_{OUT}$ changes by 1 V for every octave change of the $I_{IN}$ current

*The matched transistors can be two BC212L in thermal contact, or a dual transistor (LM394), or pat of an array (CA3046)

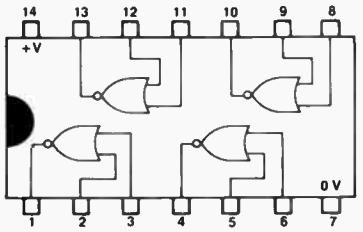
## FET Sample And Hold

Control = +12 V; sample
Control = −12 V; hold

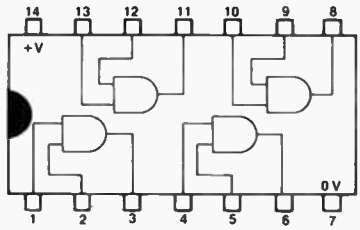



Use a printed circuit guard ring (connected to the output voltage) around the hold capacitor

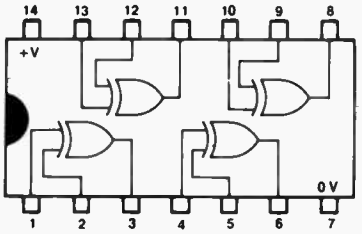
## Pinouts



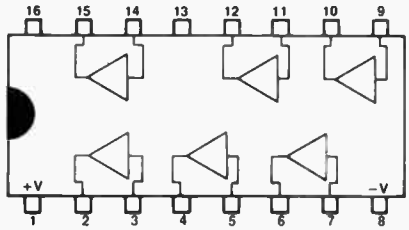

74LS02



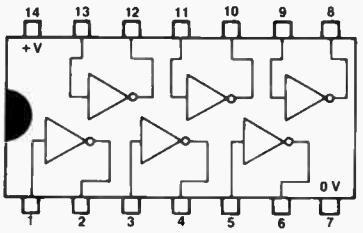

74LS08



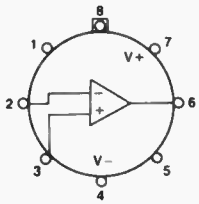

4030



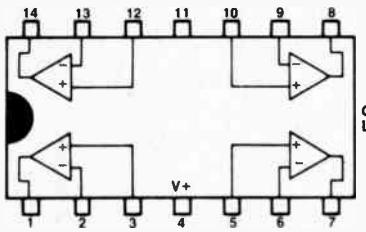

4050



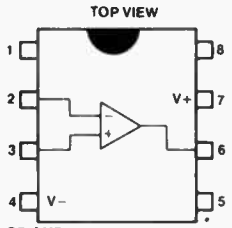

7406 (TTL)
40106B (CMOS — SCHMITT)
74LS14 (LS — SCHMITT)
4069 (CMOS)



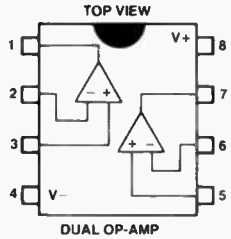

OP-AMP
741, LM108H, LM208H, LM308H, LM301



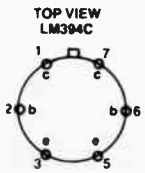

QUAD OP-AMP
LM324, TL074

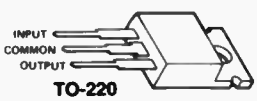



OP-AMP
741, NE5534, TL070, TL071, LM301




DUAL OP-AMP
TL072, TL082




TO-220
78xx +ve voltage reg.

# Measuring very low currents

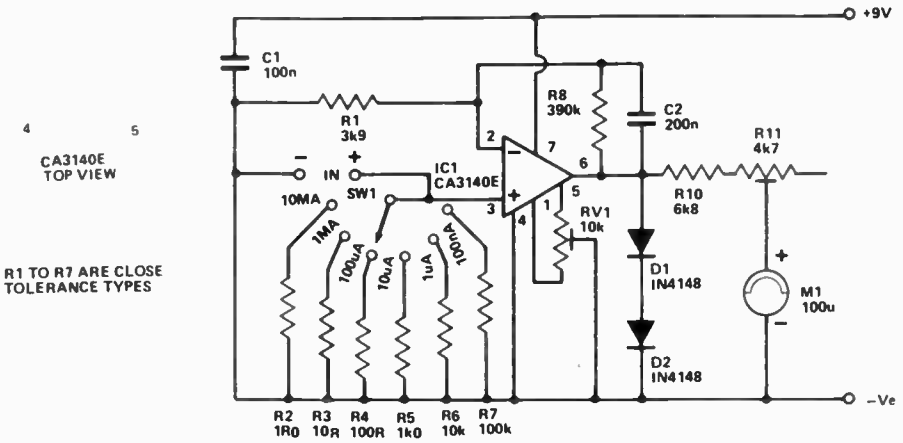
IT IS NOT POSSIBLE to accurately measure currents of a few microamps or less using an ordinary panel meter or multimeter. In order to make such measurements it is necessary to use an active circuit such as the one shown here. It can be built as a self-contained unit or used as part of an instrument requiring a highly sensitive current range.

This instrument will measure from 100 nanoamps ($10^{-7}$ amps) to 10 mA full scale, in six ranges. The higher ranges are included so that the instrument may be accurately calibrated and they generally overlap with the lower current ranges on many multimeters.

The meter, M1, is a 100 $\mu$A movement connected as a voltmeter having 1 V full scale deflection. Resistors R10 and R11 (a trimpot) are the 'multiplier' resistors. The trimpot is a calibration control, adjusted to give full scale meter deflection on the 10 mA or 1 mA ranges.

IC1 is an op-amp connected in the non-inverting mode and having a dc voltage gain of about 100 times (set by the feedback network R8 and R1). C2 reduces the ac gain to about unity to improve stability and immunity to stray pick-up. The non-inverting input of IC1 is biased to the 0 V rail by whichever of the range resistors (R2-R7) is selected by SW1. In theory, this gives zero output voltage and no meter deflection, but in practice it is necessary to compensate for small offset voltages using the offset null control, RV1.

Current in the circuit being measured flows into the instrument's input terminals. A voltage will be developed across the selected input resistor, one of R2 to R7. This voltage will be amplified by IC1 and will produce a positive meter deflection. Say the 10 mA range has been selected. The input current will flow through R2. If the input current is 5 mA, say, from Ohm's law, 5 mV will be developed across R2.




$$E = I.R$$
$$= 5 \times 10^{-3} \times 1$$
$$= 5 \text{ mV}$$

Now, IC1 has a gain of 100, as

$$\text{Gain} = \frac{R8}{R1}$$
$$= \frac{390 \times 10^3}{3900}$$
$$= 100$$

The voltage at pin 6 of IC1, with 5 mA flowing in the input, will be 500 mV, or half a volt. The meter will thus indicate half scale, giving a reading of 5 mA.

Successive ranges increase the sensitivity of the instrument by a factor of 10.

This arrangement relies on the fact that IC1 (a 3140) has a very high input impedance so that it does not 'load' the input resistor selected and affect the accuracy of the reading by drawing a significant amount of input current itself. The 3140 is a FET-input op-amp having a typical input impedance of 1.5 million megohms. Note that, to achieve reasonable accuracy, the input resistors R2 to R7 and the op-amp feedback resistors should all have a tolerance of 2 % or better.

Meter protection is provided by D1 and D2. Should the input current exceed the maximum for the range, the output of IC1 will rise higher than 1 V. If it exceeds about 1.2 V, the two diodes conduct, preventing any further rise in the output of IC1 and protecting the meter from any overload exceeding 20% of the rated input.

When adjusting the offset null control (RV1), start with its slider positioned at the end connected to pin 5 of IC1. The meter should show a strong deflection. Back off RV1 just far enough to zero the meter and no further.

The unit may be calibrated by a number of methods. A simple way is to obtain a variable power supply that will provide 10 V and a 10k 1% or 2% resistor. You will also need either a good mirror-scale multimeter or a digital multimeter.

Connect the resistor and the low current meter in series and connect across the output of the power supply. Also connect the multimeter across the output of the power supply (observe polarities). Select the 1 mA range on the low current meter and a suitable range on the multimeter. Turn the output of the power supply down and switch it on. Set the power supply to give a reading of 10 V on the multimeter. Do this carefully for best accuracy. Now, adjust R11 for full scale deflection. Your low current meter should now be calibrated. If you substitute a 1k, 1% or 2% resistor for the 10k resistor, you can check the calibration on the 10 mA range.