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## Specification

Memory Size: Variable from 8 bytes to 64 K bytes. Storage time at 32 KHz sampling rate: 2 seconds. Storage time af 8 KHz sampling rafe: 8 seconds. Longest replay time (for special effects): 32 seconds.
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Audio Bandwidih: Variable from 12 KHz to 300 Hz . Internal 4 pole tracking filfers for anti-aliasing and recovery.
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| :--- | :--- |
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## ETI gets it all together.



The AEW Nimrod - failed it's trials.

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TAG-END CAPACITORS: 64V: 2200 139p; 3300 198p; 4700 245p; 50V: 220011 Op; 3300 184p; 40V: 4700
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| POLYESTER CAPACITORS: Axial Lead Type 400V: 1nF, 1n5, 2n2, 3n3, 4n7, 6n8 $11 \mathrm{p} ; 10 \mathrm{n}, 15 \mathrm{n}, 18 \mathrm{n}, 22 \mathrm{n} 12 \mathrm{p} ; 33 \mathrm{n}, 47 \mathrm{n}$, 68 n 16 p ; 150 n 20 p ; 220n 30pi 330n 42; 470n 52p; 680n 1uF 88p; 2u2 82p. 1000V: 1nF 17 d; 10 nF 30p; 15 ก 40p; 22n 36p; 33n 42p; 47n, 100n 42p. |  |  |  | SIEMENS pcb Type Minlature poly Capacitors |
| :---: | :---: | :---: | :---: | :---: |
| POLYESTER RADIAL LEAD CAPACITORS: 250V 10n, 15n, 22n, 27n Bp; 33n, 47n, 68n, 100 n 8p; 150n, 220n 10p; 330n, 470n 15p; 680n 19p; 1u5 40p; 2u2 48p. |  | FEED-THROUGH CAPACITORS 1000pF/450V | 10p | 250V <br> inf, in5, 2n2, <br> 3n3, 4n7, 6n8, <br> 10n. $15 n 7$ |
| TANTALUM BEAD CAPACITORS 35V: 0.1uF, 0.22, $0.3315 \mathrm{p} 0.47,0.68$, 1.0. 1,5 16p; 2.2, 3.3 18p; 4.7. 6.8 22p 10 28p; 18V: 2.2, 3.3 16p; 4.7, 6.8, 10 18p; 15, 36p; 22 45p; 33, 4750p; 100 95p; 10V: 15, 22, 26p; 33,4750p; 100 80p; 6V: 100 55p. | POTENTION <br> Rotary 0.25 W <br> 470R: $1 \mathrm{~K} \&$ <br> Single Gang <br> 5K-2M <br> $5 \mathrm{~K}-2 \mathrm{M}$ <br> $5 \mathrm{~K}-2 \mathrm{M}$ | ERS: Carbon Track $9 \&$ LIN Vatues, inear only) <br> e Gang Log \& Lin <br> e Gang DP Switch <br> le Gang | $\begin{aligned} & 35 p \\ & 35 p \\ & 95 p \\ & 99 p \\ & \hline \end{aligned}$ | 18n, 22n, 27n, <br> $30 n 56$ <br> 22m,100n 11p <br> 100 V <br> $100 \mathrm{n}, 120 \mathrm{n}$ 10p <br> $150 n, 180 n-12 p$ <br> 220n. 2ion 15p |
| MYLAR FILM CAPACITORS <br> 100V: $1 \mathrm{nF}, 2,4,4 \mathrm{nF}, 10 \mathrm{f}_{\mathrm{p}} \mathbf{1 5 n F}, 22 \mathrm{n}$, 30n, 40n, 47n 7p; 56n, 100n, 200n 9pi 50V: 470nF 12p. | SLIDER POT <br> $0.25 \mathrm{~W} \log$ an <br> 5K-500K <br> Graduated | TIOMETERS near values 60 mm gle gang s for above | $\begin{aligned} & 80 p \\ & 45 p \\ & \hline \end{aligned}$ | $\begin{aligned} & 330 n_{3} 390 n 20 \mathrm{p} \\ & 470 n_{5} 580 \mathrm{n} 26 \mathrm{p} \\ & 680 \mathrm{n} \\ & \text { 1uF } 34 \mathrm{p} 2 \mathrm{p} 250 \mathrm{p} \end{aligned}$ |
| CERAMIC CAPACITORS 50V: <br> Range: 0.5 pF to $10 \mathrm{nF} 4 \mathrm{p} .15 \mathrm{nF}, 22 \mathrm{nF}$ 33 nF ; 47nF 5p. $100 \mathrm{nF} / 300 \mathrm{~V} 7 \mathrm{p}$. $200 \mathrm{nF} / 6 \mathrm{~V}$ 8p. <br> POLYSTYRENE CAPACITORS: | PRESET PO 0.1 W Miniatu Horizontal, 1 $0,25 \mathrm{~W}$ Large 0.25W Large | ITIOMETERS <br> Vertical or to 4 M7 OR to 3M3 Horz R to 4M7 Vertical | $\begin{array}{r} 8 p \\ 12 p \\ 12 p \end{array}$ | ACCESS Orders just phone your orders through We do the rest Tel. 092350234 |





## NEWS:NEWS:NEWS:NEWS:NEWS:NEWS:NEWS

DIGEST


Ferguson Monitors Developments
n what they see as a response to the demands of the technological revolution, Ferguson have introduced a $14^{\prime \prime}$ colour television set which has RGB and composite video inputs as well as the usual UHF aerial input. The new set is said to be designed with home computers, video games and video recorders in mind and its features include the ability to operate from at 12 or $24 V$ DC supply.

The MCO1 14" TX monitor colour television is based on Ferguson's existing TX90 chassis which is mains-isolated and features a fast warm-up CRT. Eight light-action switches select the TV channel or the RGB or composite video input, allowing the connectors to be left permanently in place at the rear of set and all switching to be carried out from the front.

The tuning presets associated with the channel selectors are concealed behind a hinged panel at the front of the set. A 3.5 mm output socket allows the MC01 to be used with headphones and a foldaway aerial is also buittin.

The RGB input features automatic sync polarity sensing and accepts TTL and analogue input signals. The composite video input has an adjustable pre-set gain control to ensure optimum performance over a range of input signal levels and both inputs accept a sound signal for reproduction through the set loudspeaker. Special leads will be available to connect the MC01 to most popular makes of home computer and there will also be a range of leads for use with Ferguson Videostar video recorders.

The MC01 is described as compact and lightweight and is said to offer low energy consumption. An optional adaptor allows the set to run from battery or other lowvoltage DC supplies and adjusts automatically for $\mathbf{1 2}$ or $\mathbf{2 4 V}$ opera-

## Professional Quads

Quad have produced a number of domestic hi-fi amplifier designs over the years, many of which have found their way into recording studios, theatres and other professional environments, but they have never produced an amplifier intended specifically for professional applications. Now, perhaps having noted the success of other companies who market Quad amplifiers in 19" rack format, Quad have introduced two rack-mounting amplifiers of their own, one single channel and one dual channel and both featuring XLR connectors for input and output.

The Quad 510 is a single channel power amplifier which can deliver at least 100 watts into any load from two to 100 ohms. A multipletapped output transformer allows
it to match a range of loads including 70 and 100 voli lines and a plugin card on the rear panel selects the appropriate taps. The input is 600 ohm bridging and both input and output are isolated so that amplifiers can be linked together to provide greater power outputs.

The 520 is a dual channel power amplifier which offers an output of 100 watts per channel into eight ohms and is available with optional balanced inputs. Both amplifiers use a refinement of the currentdumping concept which was used in the Quad 405 amplifier and for which the company received a Queen's A ward for Technological Innovation. No specifications are quoted but the performance is said to meet the demands of the most critical listener and construction and relia bility are said to be up to Quad's usual standards.
Quad Electroacoustics Ltd, St. Peters Road, Huntingdon, Cambridge PE18 7DB, tel 0480-52561.

tion. Ferguson say that the set will typically run for about eight hours from a fulty-charged standard (40A/h) car battery.
The company have also established an advisory service which they say is designed to help dealers and customers with queries relat-
ing to compatibility and upgrading on home computers. The service can be contacted on 01-807 3060. Thorn EMI Ferguson Ltd, Cambridge House; Great Cambridge Road, Enfield, Middlsex EN1 1UL, tel 01-363 5353.


## Static Alarm

Dage Eurosem have introduced a bench-top alarm unit which detects the presence of high voltage levels and gives an audible and visual warning. The alarm is intended for use wherever CMOS and other static-sensitive devices are being handled and requires no physical or electrical connection to the device or the operator.
The EVA-12 triggers when in the presence of voltages above 400 V and will typically detect a hazard
of 4-13kV (equivalent to a person walking across a vinyl floor) from a distance of between sixteen and thirty inches. The warning takes the form of an audible bleep and a flashing LED and continues for five seconds before the unit zeroes itself and returns to the alert mode. It measures $76 \times 38 \times 25 \mathrm{~mm}$ ( $3 \times 1.5 \times 1^{\prime \prime}$ ) and runs from a 9 V battery giving a typical operational life of six months.

For further information contact Dage (GB) Ltd, Eurosem Division, Rabans Lane, Aylesbury, Buckinghamshire HP19 3RG, tel 029633200.

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## NEWS:NEWS:NEWS:NEWS:NEWS:NEWS:NEWS

## High Density <br> ' ${ }^{\prime}$ <br> Connectors

Souriau have introduced a range of sub-miniature ' $D$ ' type connectors which have a closer pin-spacing than existing sub-miniature types and offer correspondingly higher numbers of contacts. Plugs and sockets with up to 78 ways are available, and in spite of their small size the connectors offer a performance which is generally comparable with that of other sub-miniature ' D ' connectors.
Designated the 8635 series, the new connectors come with either 15, $26,44,62$ or 78 contacts and are rated at 1000 volts RMS, 5A per contact maximum. No overall current rating for a connector is specified. The contacts are size 22 crimp on 0.76 mm ( $0.03^{\prime \prime}$ ) centres and the operating temperature range is from $-55^{\circ}$ to $+150^{\circ} \mathrm{C}$. The insulation material is a self-extinguishing thermosetting plastic manufactured to UL class 94 V -O and the shell is made from cadmium plated steel.
The connectors can be supplied in both rigid and float mounting versions and are also available with interfacial and back-end sealing gaskets. 8635 crimp connectors can also be ordered against equivalent MIL C-24308A (S*MA) series part numbers. For further information contact Souriau (UK) Ltd, Knaves Beech Industrial Estate, Loudwater, Nr High Wycombe, Buckinghamshire, tel 06285-24981.

## Music For The Newbrain

Would the reader who sent us the above project please get in touch with the editorial office - we've lost your name and address!

- Japanese component manufacturer Alps is setting up a new plant which will create 230 jobs when it opens in Milton Keynes next year and up to 400 jobs when it reaches full production. The plant willproduce parts for video recorders. In a separate statement, Cirkit have announced an increase in the range of Alps parts that they stock. The new lines will include microminiature Tactile switches, data entry switches, keytops and slide and rotary potentiometers. Cirkit Holdings PLC, Park Lane, Broxbourne, Hertfordshire EN 10 7NQ, tel 0992-444111.


## New Philips DSO

Philips have introduced a portable digital storage oscilloscope capable of sampling signals with a clock rate of up to 125 MHz . The dual-channel instrument has four memories, the contents of which can be displayed simultaneous or individually, and the user is able to program the trigger level control and all other trigger functions as well as all other switch functions.
The PM 3315's input circuitry enables analysis of repetitive signals to well over $\mathbf{6 0} \mathbf{~ M H z}$. Fast 125 MHz sampling allows single-shot capture up to 30 MHz with accurate reproduction. Even higher single-shot bandwidths are possible using computer data-analysis by means of the integral IEEE488/ IEC625 bus interface. A digital delay facility makes possible optimal use of the available memory depth by triggering from

nine screen divisions before the desired position to 9999 divisions after.
Tomeet the requirements of the fast growing world of TV applications, the PM 3315 also offers stable TV frame or field triggering. Other facilities include a plotmode output for an X-Y recorder and a chart-recording mode
allowing maximum internal storage of up to 40 hours. Control capability covers all front panel settings, including timebase and attenuator.
The PM 3315 costs $£ 5195$ plus VAT and is available from Philips Test and Measuring, Pye Unicam Ltd, York Street, Cambridge CB1 2PX, tel 0223358866.


## Long-Life Rechargeables

Yuasa have launched a range of lead-acid sealed rechargeable batteries which they claim have a life expectancy of ten years. The batteries have been designed with un-interruptible power supply applications firmly in mind and are said to be explosion proof and capable of retaining a high capacity under float-charge conditions.

The new range is designated the XL series and uses the same construction method as the existing NP range to make them completely leakproof. They are available in 6 and 12 volt versions with capacities of 66,88 and 110 Ah and 33, 44 and 55 A h respectively. They require constant-voltage charging and their nominal cell voltage is 2.23 V . A low specific-gravity electrolyte has been used to re-
duce float voltage and selfpoisoning, allowing the batteries to be used for long periods under float charge conditions without loss of capacity. A venting arrangement on the top of the batteries allows gases caused by overcharging to escape but will not allow flames to re-enter, thus removing the risk of explosion present with some vented cells.
The $X L$ range was designed specifically for telecommunications applications and the battery sizes meet these requirements rather than being directly compatible with similar batteries used in other sections of industry. They are expected to find applications in computers, test equipment, medical equipment and un-interruptible supply applications as well as in the telecommunications field.
Yuasa Battery Sales (UK) Ltd, Hawksworth Industrial Estate, Swindon, Wiltshire SN3 1DZ, tel 0793486818.

## The Little Chill

D CA are marketing a range of equipment cooling fans which have a fixing plate size of only 80 mm ( $\mathbf{3 . 1 5 5 ^ { \prime \prime } \text { ) square. Features }}$ claimed include low mechanical noise, zero electrical noise, low weight and long life, and the fans are expected to find wide application in domestic products as well as in office equipment, test gear and industrial equipment, etc.

The fans are available in 6,12 and 24V DC versions and operate at a speed of 4000 RPM to achieve an air flow of $0.95 \mathrm{~m}^{3} /$ minute. The mechanical noise is less than 21 dBA and PCA claim that electrical noise has been entirely eliminated. The full weight is $\mathbf{1 7 0}$ grams and the anticipated life expectancy is $\mathbf{1 0 , 0 0 0}$ hours for most models.
For further details contact $P$. Caro \& Associates Ltd, 2347 Coventry Road, Sheldon, Birmingham B26 3LS, tel 021-742 1328.


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## :NEWS:NEWS:NEWS:NEWS:NEWS

# Photo-Electric Switch With Integral Amplifier 

Sigma have introduced a photo-electric sensor which has a built-in amplifier. The unit can be used to detect liquid levels, passing objects, etc, requires no special cable to prevent noise problems and will operate with cable
lengths of up to $\mathbf{5 0}$ metres.
The PM-07 is a retro-reflective sensor which will detect transparent, translucent and opaque objects at distances of up to 25 mm ( $1^{\prime \prime}$ ) with no physical contact. It operates from a $12-24 \mathrm{~V}$ DC supply and has a response time of less than 5 ms . The case measures 7.5 mm square by 38 mm long and the operating temperature range is from minus $10^{\circ}$ to plus $55^{\circ}$ centigrade.
Further information is available from Sigma Ltd, Spring Road, Letchworth, Hertiordshire SG6 4AJ, tel 04626-3841.

# Blue LEDS 

Red, yellow and green LEDs using crystalline semiconductors such as gallium phosphorus and arsenic have been available for more than a decade, but LEDs which emit blue light have been expensive and have not been generally available. Two years ago, Siemens devised a method of manufacturing 'bluelight chips' at a considerably lower price, albeit without matching the price level of LEDs in the other colours, and having sounded out the market have decided to include the fourth colour in their 1985 product range.

The new blue LED, type SLB 5410 , operates at 480 nm and uses silicon carbide ( SiC ) as the source material. SiC has emerged as the optimum semiconductor for blue light only after years of research, and although it is costly to produce, it has significant advantages over ZnSe or GaN. The SLB 5410 has a forward voltage of typically 4 V at 20 mA , the corresponding figures being 10 V at 20 mA for ZnSe or GaN types. Typical outputlevels are 4 mcd at 20 mA measured in the optical central axis at a half-angle of eight degrees, and the device is mounted in a standard 5 mm plastic package.
The purity and reproductability of the blue LED's 480 nm radiation are unmatched. Further characteristics are high impulse stability,
a narrow spectral bandwidth and a very low ageing rate. These features make the LED suitable for use as a radiation source in spectroscopic, biophysical or medical applications, as a calibration source for TV camera and photographic equipment, and, later on, possibly even as a means for producing the blue luminous dots on flat screens.

The blue LED is less suitable for use as a mere on/off indicator than its red, yellow and green counterparts because, quite apart from higher costs, the angle of radiation and the intensity are lower than in conventional LEDs.

Siemens Limited, Siemens House, Windmill Road, Sunbury-on-Thames, Middlesex TW167HS, tel 09327-85691.



## Safety Cap

Not being the sort of company to bottle things up, Siemens have written to tell us about their latest innovation. They have introduced a range of tantalum electrolytic capacitors which are designed to overcome the risk of fire presented by conventional electrolytics when they are fed a voltage of the wrong polarity.
If an electrolytic capacitor is operated with reverse polarity, perhaps because of a fault in a piece of equipment, it will heat up
rapidly and may even explode. This effect is even more markedin tantalum capacitors which have a much higher charge density than other electrolytics. In an extreme case it is possible for the piece of equipment in which the capacitor is installed to catch fire as the result of such a fault.
Siemens have overcome this hazard by incorporating a fuse into their new $\mathbf{B} 45185$ series of tantalum capacitors. The fuse takes the form of a solder wire link in the cathode lead, and if the capacitor is operated with reversed polarity this link will quickly heat up and melt and the capacitor will fail harmlessly. They are available in four types with capacities ranging from 100n to 330 uF and with voltage ratings from 6.3 to 50 volts. The single-ended rectangular plastic package has climatic protection which meets the requirements of category FKE of the DIN 40040 standard and has been designed with automated assembly in mind.
For further information contact Siemens Lid, Siemens House, Windmill Road, Sunbury-onThames, Middlesex TW16 7HS, tel 09327-85691.

- Semiconductor Supplies international have brought out the autumn issue of their catalogue. Its 32 A4 pages list transistors, diodes, rectifiers, microprocessors and other ICs, LEDs, capacitors and resistors. Copies are available from Semiconductor Supplies International Ltd, Dawson House, 128-130 Carshalton Road, Sutton, Surrey SM1 4RS, tel 01-643 1126.
- The new Electrovalue catalogue actually came out last month but we couldn't find room to mention it. Never mind, it's valid until the end of January 1985 so it's still worth sending off for, and its 44 A5 pages list their largest ever range of general components, computers and accessories, books and test equipment. Copies are available free of charge from Electrovalue Ltd, 28 St. Judes Road, Englefield Green, Egham, Surrey TW20 0HB, tel 0784-33603.
- Once again, the quarterly figures show an increase in the number of business failures in the electrical industry. Business information company Dun \& Bradstreet Ltd
tell us that there were 585 company liquidations in the industry in the firstnine months of 1984, a four per cent increases over the figure for the same period of 1983. Bankruptcies among firms, partnerships and individuals in the industry totalled 88 over the same period, a $\mathbf{2 2 \%}$ increase over the 1983 figure. A small glimmer of hope appears in the news that the computer manufacturing industry (micros to mainframe) has strengthened its financial position in the last five years with only $\mathbf{2 3 \%}$ of firms now considered by Dun \& Bradstreet to be financially vulnerable compared with 45\% in 1979.
- Miller-Stephenson Chemicals have produced a spray-on conductive coating which is intended to absorb RFI and EMI over a broad frequency range. The coating is sprayed from an aerosol can, dries in fifteen minutes, is effective within minutes and provides over 78 dB attenuation at $1 \mathrm{MHz}, 49 \mathrm{~dB}$ at 10 MHz and 21 dB at 100 MHz . For details contact the distributors, $\mathbf{D}$. Fraser \& Company, 129 Kylepark Drive, Uddingston G71 7DD, tel 0698-813476.


# 01-208 1177 Technomatic Lid 01-208 1177 BBC Micro Computer System <br> <br> DISC DRIVES <br> <br> DISC DRIVES <br> These are fully cased and wired drives with slim line mechanisms 

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KP810£249 (a) JUKI $6100 £ 340$ (a) KAGA TAXAN KP910£369 (a)

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Serial Interface: $8143 \mathbf{£ 2 8}$ (c) 8148 with $2 \mathrm{~K} \mathbf{£ 5 7}$ (c)
Paper Roll Holder $£ 17$ (d) $\mathbf{F} \times 80$ Tractor Attachment $£ 37$ (b)
Ribbons: FX/RX/MX $80 £ 5$ (d) FX/RX/MX $100 £ 10$ (d) RX/FX80 Dust Cover £4.50 (d) KAGA TAXAN
R232 with 2 K Buffer $\mathbf{£ 8 5}$ (b) KP810/910 Ribbon $\mathbf{£ 6 . 0 0}$ (d)

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## - All modems listed below are BT approved

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The ultimate world standard modem coverall all common BELE and CCIT standards up to 1200 Baud Allows comsystem in the world The optional AUTO DIAL and AUTO ANSWER boards enhance the considerable facilities already provided on the modem. Mains powered E129(b). Auto Dial Board/Auto Answer Board E3O(c) each. Software lead

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1431 Std Res ............................................. 175 (a)
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This low cost intelligent eprom programmer can program 2716, 2516, 2532, 2732, and with an adaptor, 2564 and 2764 . Displays 512 byte page on $T V$ - has a serial and parallel VO routines Can botty il....
Adaptor for 2764/2564. $\mathbf{\Sigma 2 5 . 0 0}$ (c)

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UV1 B erases up to 6 eproms at a time. ... $\mathbf{f 4 7}$ (c) UV1T as above but with a timer £59(c) UV140 erases up to 14 epro UV141 as above but with a timer.......... $\mathbf{E 7 9}$ (b)

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| EDGE CONNECTORS |  |  | AMPHENOLCONNECTORSway plug Centronics |  |  |  | TELEPHONE CONNECTORS |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 2*6-way (commodore) | ${ }^{0.1} 1$ | 0.156.300 p |  |  |  |  | 4 way plug |  |  | 110 p |
|  |  |  |  |  |  |  | 6 way tang.skt |  |  |  |
| $2 \times 12$-way (vic 20) ${ }^{\text {20 }}$ |  |  |  |  |  |  |  |  |  |  |
|  |  | ${ }_{2200}^{1400}$ |  | plug |  | (solder) |  |  |  |  |
|  |  |  |  |  |  |  | 6 way |  |  |  |
| $2 \times 36$-way$1 \times 43$ way$2 \times 22$ way$2 \times 43$ way$1 \times 77-$ way$2 \times 50$-way $(S$ (00conn) | $\begin{aligned} & 250 \mathrm{p} \\ & 260 \mathrm{p} \\ & 190 \mathrm{p} \\ & 395 \mathrm{p} \\ & 400 \mathrm{p} \\ & 600 \mathrm{p} \end{aligned}$ | $\begin{aligned} & \text { Z } \\ & \overline{\text { Z00p }} \end{aligned}$ | 500 p (ibc) 500 p PCB Mtg Skt Ang Pin 24 way 700 p 36 way 750 p |  |  |  | RIBBON CABLE |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | GENDER CHANGERS25 way D type |  |  |  | $\begin{aligned} & 10 \text {-way } \\ & 16 \text {-way } \\ & 20 \text {-way } \\ & 26 \text {-way } \end{aligned}$ | $\begin{gathered} 40 \mathrm{p} \\ 60 p \\ 850 \\ \hline 850 \\ \hline 120 \end{gathered}$ |  | 180p |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  | Maie to Male. ........... $\mathbf{£ 1 0}$ <br> Male to Female <br> Female to Female......... $\mathbf{£ 1 0}$ |  |  |  |  |  | 64.w |  |
| EURO CONNECTORS |  |  |  |  |  |  | DIL HEADERS |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| OIN 41612 , |  |  | RS 232 JUMPERS |  |  |  | 14 pi |  |  | 100 p |
| $2 \times 32$ way Ang Pin 275p |  |  | 24" (25 way D) |  |  |  | 18 pin 60p . |  |  |  |
| $3 \times 32$ way St Pin 260 p |  |  | 24" Single | end May |  | ¢5.06 | 20 pi |  |  | 150p |
| $3 \times 32$ way Ang Pin 375pIDC Skt A + B275p |  |  | ${ }_{24}{ }^{24}$. ${ }^{\text {cemale female }}$ |  |  |  | 24 pin |  | 100 p |  |
|  |  |  | 24". Male | Male |  | ع10.00 ¢9,50 |  |  | p |  |
|  | 350p |  | ${ }^{24}{ }^{\text {"Ma }}$ | male |  | ${ }_{\text {¢9.50 }}$ | 40 pi |  | p | 225p |
| For $2 \times 32$ way please specify spacing ( $A+B, A+C$. |  |  | DIL SWITCHES ${ }_{\text {S0p }}$ |  |  |  | MISC CONNS <br> 21 pin Scart Connector.200p <br> 8 pin Video Connector.200p |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | 8 -way | 120p |  |  |  |  |  |  |  |  |


| 74 SEAIES |  | 773686 |
| :---: | :---: | :---: |
| 7400 | 30p |  |
| 7401 | 330 | 73393 1128 |
| 7402 | ${ }^{300}$ | $\begin{array}{ll}74439 \\ \\ 74434 & 1409 \\ 1000\end{array}$ |
| ${ }_{7}^{7403}$ | 300 | 7443\% 1.00 p |
| ${ }_{7405}$ | ${ }_{30 \mathrm{p}}^{30}$ | 74LS S |
| 7405 | 400 |  |
| ${ }_{7}^{7407}$ | 408 |  |
| 7409 | ${ }_{30}$ | $\begin{array}{lll}741502 & \\ 780\end{array}$ |
| 7410 | 30 p |  |
| 7419 | ${ }^{300}$ |  |
| 7812 | ${ }^{30 \mathrm{p}}$ |  |
| 7414 | 70. | ${ }_{74 \text { LSo9 }}{ }^{\text {280 }}$ |
| 7416 | 38p | ${ }_{74 \text { LS } 10}$ 28p |
| 7417 | 40 p | ${ }^{741511}{ }^{\text {28p }}$ |
| 7720 | ${ }_{\substack{30 \\ 30}}$ |  |
| 7421 <br> 7428 <br> 8. | ${ }_{\substack{\text { cigp }}}^{\text {ciop }}$ |  |
| 7423 | 38 p | ${ }_{7451515}{ }^{\text {28p }}$ |
| 7425 | 400 | ${ }^{7464520}$ |
| 7426 <br> 7427 <br> 185 | ${ }_{40 \mathrm{P}}^{40}$ |  |
| 7488 | ${ }_{43 \mathrm{p}}^{4}$ |  |
| 7430 | 30 p |  |
| ${ }_{7}^{7432}$ | 360 | P4LIS27 |
| 7433 | 330 |  |
| 7438 | ${ }_{409}$ |  |
| 7439 | 40 p | ${ }^{\text {T4LLS33 }}$ |
| 7740 | ${ }^{400}$ |  |
| ${ }_{7442 \mathrm{~A}}^{744}$ | ${ }_{70 \mathrm{p}}^{900}$ |  |
| 7444 | ${ }^{110}$ | 74L542 <br>  <br> 1850 |
|  | ${ }_{\substack{\text { coop } \\ \text { 100p }}}$ |  |
| ${ }_{7}^{74448}{ }^{746}$ | 1000 |  |
| ${ }_{7450}$ | ${ }_{\substack{1209 \\ 36 \mathrm{p}}}$ |  |
| 7451 | 35 p | 74LS55 <br>  <br> 180 |
| ${ }^{7453}$ | ${ }^{38 p}$ |  |
| 7454 7460 | cis |  |
| ${ }^{7470}$ | ${ }_{500}$ | ${ }_{74 \text { L57 } 6 \text { A }}$ 43p |
| ${ }_{7473} 7$ | 55p |  |
| 7473 | 年500 | ${ }^{744585}$ |
| 7474 <br> 7475 |  |  |
| 7476 | $45 \circ$ | ${ }^{74 L 591}$ |
| 7480 | ${ }^{655}$ |  |
| ${ }_{7}^{7483}{ }_{7}^{74}$ | $1800^{1050}$ 1050 |  |
| ${ }^{74844}$ | ${ }^{1250}$ | ${ }^{7} 7159696900$ |
| 7485 7886 | ${ }_{\text {120 }}^{1100^{2}}$ |  |
| 7489 | 210p |  |
| 7499 A | ${ }^{550}$ | ${ }_{744.5113}$ |
| 7491 | ${ }^{700}$ | ${ }^{74.51144} 45$ |
| ${ }_{7}^{74929 A}$ | ${ }_{\text {55p }}^{700}$ |  |
| ${ }_{7}^{7944}$ | ${ }^{1150}$ | 74.5 |
| ${ }^{74954}$ | ¢op |  |
| ${ }_{7} 7497$ | ${ }^{2100}$ | ${ }^{74 \text { LSt } 266} \mathbf{5 0 p}$ |
| ¢ 741400 | ${ }^{1800}$ |  |
| ${ }_{74109}$ | ${ }_{75 p}$ |  |
| 7410 | ${ }^{75 p}$ | 74.51388 |
| 7411 | 55p | 74.5139 60 p |
| ${ }_{7}^{74176}$ | $110{ }^{108}$ |  |
| 7419 74120 | ${ }^{1700}$ | (74LS14881400 |
| 74121 | 55p | ${ }^{7415152} 2000{ }^{\text {20, }}$ |
| ${ }^{74122}$ | ${ }^{700}$ | 7415153 700 |
| 74123 74125 | ${ }_{85 \mathrm{p}}^{809}$ |  |
| 74126 <br> 7128 | S5p |  |
| ( 741132 | ${ }_{75 p}$ |  |
| ${ }_{74136}$ | 700 | 74151604 750 |
| 74141 |  | ${ }^{7415151614} 750$ |
| 74142 7 | ${ }_{2708}^{250}$ |  |
| 74148 | ${ }^{270}{ }^{\text {p }}$ | ( |
| 7145 | ${ }^{1108}$ | 74551654110 D |
| 74147 7 | 1700 | (7415166A ${ }^{\text {7 }}$ |
| ${ }_{7} 74.150$ | 1.75 |  |
| ${ }_{7}^{74.51 / 4}$ | ${ }^{700}$ | ${ }^{74515179101808}$ |
| 74154 | ${ }^{1400}$ | - |
| 74155 | ${ }_{\text {Bop }}$ | $7451515{ }^{750}$ |
| $\xrightarrow{74156}$ | ${ }_{\text {cop }}^{1000}$ |  |
| 74459 | ${ }^{1759}$ |  |
| ${ }_{7}^{74160}$ | ${ }_{\text {rop }}$ |  |
| ${ }^{7} \mathbf{7 1 6 2}$ | ${ }^{1109}$ | ${ }^{74515193}$ |
| ${ }_{7}^{74164}$ | ${ }_{\text {l120 }}^{102}$ |  |
| 74465 71665 7 | ${ }^{110 p}$ | 74LA956 90 |
| 74166 74167 | ${ }^{14000}$ |  |
| $\xrightarrow{74170}$ | ${ }^{2000}$ |  |
| ${ }_{7}^{74172}$ | ${ }^{\text {liap }}$ |  |
| (74174 | ${ }^{\text {105p }}$ |  |
| ${ }_{74176}$ | 100p |  |
| ${ }_{\substack{74178 \\ 74179}}$ | cisop |  |
| ${ }_{74180}$ | ${ }^{1000}$ |  |
| 74181 | 3400p |  |
|  | , 1800 | ${ }^{7455256}$ |
| 980 | ${ }_{\substack{130 p \\ 180}}$ | (744525A $70{ }^{7}$ |
| ${ }_{74191} 7$ | ${ }^{1} 1000$ |  |
| ${ }^{74192}$ | ${ }^{115 p}$ |  |
| 74194 | ${ }^{1100}$ | ${ }_{74452866} 800$ |
| 74195 | cosp | ${ }^{741585731250}$ |
| ${ }_{74197}$ | ${ }^{110}$ |  |
| ${ }^{74198}$ | ${ }_{220}^{220}$ | ${ }_{74 L 5283}$ 85P |
| ${ }_{74229}$ | ${ }_{110 \mathrm{p}}^{220}$ |  |
| ${ }_{74251}^{74259}$ | ${ }_{150}^{100}$ | ${ }_{7415293} 900$ |
| ${ }_{7} 7426595$ |  |  |
| ${ }_{7}^{74273}$ | 2009 | ${ }_{74,529969009}$ |
| ${ }_{7}^{74278}$ | ¢ |  |
| ${ }^{744279}$ | 1009 | $74 \leq 53233308$ $74 \leq 5324 / 624$ |
| 74285 | ${ }^{320}$ | ${ }^{7415324 / 624} 35$ |
| 74290 | ${ }^{80 p}$ | 74L53442000 |
| 74298 | ${ }^{1800}$ | (1945353 |
| ${ }_{743655} 7$ | ${ }_{800}^{2000}$ | 74453562100 |
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1 voice coil. Res Freq 56 Hz Freq Resp
1/2 voice coil. Res. Freq 56 Hz . Freq Resp. to 20KHz. Sens 89 dB . PRICE $69.99+61.50 \mathrm{P} \mathrm{\& P}$ ea
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# ACTIVE BASS LOUDSPEAKER 

# The active loudspeaker design which appeared in the last four issues was ideal for those starting from scratch, but what about those who already have a loudspeaker system and simply want to improve it? Jeff Macaulay has been active on their behalf too. 

With one or two notable (and expensive) exceptions, domestic loudspeakers are almost incapable of reproducing sounds below about 50 Hz . The reasons for this are not too difficult to find. Even with the best of today's drive units a large cabinet is required to give extended bass response, and this is just not practical for modern-day lounges very few of which could be described as palatial.

True, it is possible to squeeze a few more hertz out of a small sealed box, but only at the expense of efficiency. The result is that amplifiers rated at nearly a kilowatt are required to produce anything like 'live' sound levels. Even a modest amount of bass boost will cause the midrange to go soggy, and the result in the bass register is just a boomy mess! So what is the solution?

Instead of giving your bank manager the pleasure of collecting vast amounts of interest on a loan for a new pair of speakers why not build the Neptune? It has been designed as a small add on unit which will extend the response of your existing speakers down to below 30 Hz . That is a whole octave lower than $99 \%$ of the speakers on the market can manage, and for a modest outlay to boot.

## Design Philosophy

Before delving deeply into the circuitry involved it will be as well to consider the design philosophy behind this project. As is well
known, the deepest note that a speaker system can produce is limited by the size of the cabinet into which it is mounted. This is because any driver has a fundamental resonance due to the mass of the cone and the compliance of the speaker surround.

Imagine the cone mass as a weight suspended on a spring, which represents the surround compliance, and you can easily visualise the system. Place the driver in a sealed box and the air trapped inside effectively stiffens the compliance,making the resonant frequency higher. The smaller the volume of the box the higher the resonance and the less bass you get out of it.

To get around this difficulty some radical thought is necessary. Below the resonant frequency the
response of the driver dies away at 12 dB \%octave. If we were to boost the signal at that rate below the resonant frequency we would obtain a flat response.

This is the method used here. Such a speaker would be useless above the resonant frequency of the cabinet because the response with the filter added rolls of at 12 dB /octave above resonance (see Fig 1). However, this response is exactly what is required for an add on bass unit as it will complement the falling response of the existing speakers.

As most of the money spent on a pair of speakers is invested in extending the response below 100 Hz , it would be pointless to waste what we have already paid for. The Neptune has therefore been designed as a bass augmenter.

Having decided the form our


Fig. 1 Response curves for the Neptune system.
bass speaker is to take there remains to be considered the matter of quantity and quality of output.

Unlike reflex and horn enclosures the sub-resonant principle has the advantage of not using resonant effects to obtain the desired response. In a reflex cabinet, for example, the extension in bass response is obtained at the expense of 'hangover'. That is, the cabinet is still resonating after the note has stopped. This effect can be minimised by competent design but it still gives this type of enclosure a bad name.

The quantity of bass generated by a pair of $8^{\prime \prime}(200 \mathrm{~mm})$ speakers operating in tandem is easily quantifiable, but to appreciate the problem some understanding of the principles involved is required. If you were to look at the typical power versus frequency curve of speech and music you would find that the peak output occurs at around 200 Hz , the lower midrange. Above and below this frequency the power requirement falls off rapidly, and at the lowest frequency of interest to us, 30 Hz it is some 12 dB down on the mean output at 200 Hz .

This means that, if the speakers are required to give a mean output of 96 dB SPL , the output required from the woofer would be some 84 dB SPL. This the Neptune can easily give provided it is positioned on the floor and against a wall to take advantage of sound reflection from these surfaces.

The KEF B200A was chosen for this project for two reasons. First, they are blessed with a long and linear cone excursion and second the choice of a well known and respected drive unit will satisfy those who would pick holes in anythingl

There is a tried and tested alternative, the Altai stocked PF81HR which has a similar performance in this application to the B200A's but is somewhat cheaper. For those on a budget these are recommended. Later upgrading simply means changing them for the B200's (see buylines).

In order to easily interface the speaker with existing stereo systems, a dedicated amplifier is required along with the active filter.

These are mounted within the cabinet so that interfacing is reduced to plugging the unit into the mains and one of the speaker outlets. You might think that outputs from both channels would be required but this is not so. To ensure that bass signals are not presented out of phase from normal speakers, the bass content of stereo records is mixed down to mono below 100 Hz . The signal of interest is therefore identical in both channels and can easily be obtained from one! This also has the advantage of preventing possible crosstalk between channels at higher frequencies and the woofer therefore has no deleterious effects on the stereo image.

To avoid hum loops the speaker electronics are not separately earthed. The unit is automatically earthed when

## BUYLINES

A designer-approved kit of parts for this project is available from Bewbush Audio, 26 Hastings Road, Pound Hill, Crawley, Sussex RH10 4AT. The kit includes all of the electronics and two PF81HR drive units but not the woodwork. It costs $\mathbf{£ 4 9 . 9 5}$ inclusive. The electronics alone can be supplied as a kit for $£ 29.95$ but note that Bewbush will not supply individual parts. B200A drive units are available from Wilmslow Audio and the Autona UL60 amplifier module is available from Bi-Pak. None of the other components should present any problems. PCBs will be included with the kits but are also available through our PCB Service.
connected by the amplifier earth. For this particular application nothing spectacular is required of the amplifier, especially as the bandwidth ceases at 90 Hz ! All that is necessary is the appropriate output power, about 30 W , and

## HOW IT WORKS

The full circuit of the woofer is shown in Fig. 2. Input signals are applied to the gain control RV1 via SK1. Q1 in conjunction with R1/2/3 and R4 forms a simple virtual earth amplifier. The gain is set by the ratio of R2 to R1 whilst C1 isolates the base of Q1 from DC ground.

The amplified signal from the collector of Q1 is DC coupled into the second stage formed around Q2. This transistor is used in the emitter follower mode and provides a low impedance drive for the amplifier module.

In order to equalise the output to the woofer a Butterworth filter is used. R5/6 and C2/3 form the second order network with a $\mathbf{- 3 d B}$ point below 20 Hz . The $Q$ of the filter with the chosen component values is close to the optimum 0.7 . Filters of this $Q$ give the
maximum rolloff rate consistent with low ripple in the passband.

R8 and C4 form a simple but effective decoupling network to provide the circuit with a ripple - free power line. To prevent any nasty and expensive damage to the drivers, the output is AC coupled by C5. In order to maintain a high damping factor down to low frequencies a large value electrolytic is required here.

Finally we come to the power supply proper which is thoroughly conventional. The mains voltage is both isolated and stepped down by the transformer T1. The raw secondary AC output is full wave rectified by BR1 and smoothing is provided by C6.

Notice that the drivers are wired in parallel. This means that the impedance seen by the power amplifier is some 4 ohms.


Fig. 2 The circuit of the filter/amplifier.
sufficient voltage gain. To avoid reinventing the wheel, a ready built power amp module is used.

## Construction

This breaks down neatly into three parts, the electronics, the mechanics and the cabinet, and construction of the electronics should be tackled first.

The layout of the filter/amplifier PCB is shown in Fig. 3. PCB pins or veropins were used in the prototype for connections to the board, and if you plan to do likewise it is a good idea to insert them before assembling any other components. Push them well home and then solder them to ensure a good connection. If you do not wish to use pins, simply solder flying leads onto the board in the normal way, enlarging the holes if necessary to allow the wires to pass through. The rest of the PCB assembly should present no problems, the only point to watch being the polarity of the various electrolytic capacitors and semiconductors.

The next stage of the construction is to drill the heatsink and mount the PCB assembly and the amplifier module. The details are given in Fig. 4. Note that 10 mm spacers have been used between the PCB and the amplifier, but if these are not available simply use nuts instead. It is important that there is good thermal contact between the amplifier heatsink and the main heatsink, so de-burr the mounting holes and make sure that no metal filings get trapped between the two surfaces when you assemble them. Finally, attach the bridge rectifier and C5 to the heatsink with 4BA nuts and bolts.

That takes care of the easy stuff -

| PARTS LIST - |  |
| :---: | :---: |
| RESISTORS (all $1 / \mathbf{W}, 5 \%$ ) |  |
| R1,8 | 18k |
| R2 | 390k |
| R3,5,6, | 100k |
| R4,7 | $4 \mathrm{4k7}$ |
| RV1 | 4 4 7 |
| Capacitors |  |
| C1 | 10u, 16V electrolytic |
| $\mathrm{C}^{\text {c }}$ | 100n polyester |
| C3 | 47 n polyester |
| C4 | 100u 16V electrolytic |
| C5 | 2,200u 25 V electrolytic |
| C6 | 5000 u 50 V electrolytic |
| SEMICONDUCTORS |  |
| Q1,2 | BC184L |
| BR1 | 100PIV 2A bridge rectifier |
| miscellaneous |  |
| Ls1, 2 | KEF B200A drive units (or Altai |
| 71 | PF81HR - see text) 30V, 1.5 A mains |
| \% | transiormer |
| SK1 | two-pole input socket to choice |

PCB; veropins or similar; Autona UL60 amplifier module; $6^{\prime \prime} \times 4^{\prime \prime}$ heatsink; 10 mm spacers; ' $P$ ' clip or strain relief bush; aluminium for control panel; capacitor clamps for C5 and C6; nuts, bolts, cable, etc.
the next stage is to assemble the cabinet itself. The cutting details are given in the cabinet parts list. You can purchase a large sheet of veneered chipboard and cut it up
yourself, but unless you have a good saw-bench and are resonably skilled in using it you will probably be better off purchasing the materials ready cut. Most DIY stores possess facilities to do this but you would do well to ask around and find somewhere with both the equipment and the skilled staff necessary to do a really good job. Even a small error will make construction much more difficult and the problems inherent in producing a neat end result and making it airtight will be multiplied considerably.

The cabinet has been designed for maximum rigidity, a fundamental requirement if rattles and buzzes are to be avoided. The rigidity is achieved by splitting the cabinet into two with an internal partition, and the panels are glued and screwed together with $11 / 4^{\prime \prime}$ self-tapping screws.

Another requirement of this design is that the cabinet should be airtight. In practise this is not a problem as long as all the joints are filled with an appropriate filler. A good seal around the drivers is also imperative but this is automatically achieved by using the gaskets provided.


Fig. 4 Mounting arrangements for the amplifier module and PCB.


Fig. 3 The overlay diagram of the filter PCB.



Assuming one has all the panels to hand construction can commence. Start by labelling each panel with the appropriate letter on its worst side, see Fig. 5. Find the partition panel (C) and drill a $1 / 4^{\prime \prime}$ ( 6 mm ) hole in it to take the wires from the drive unit. The position of this hole is far from critical, and anywhere near the centre of the panel will be fine!

Mark out the position of the screw holes on the panels and drill $1 / 8^{\prime \prime}(3 \mathrm{~mm})$ pilot holes through these positions. Choosing the best face, countersink these to take the screw heads. If a countersink is not available a good job can be done with a $3 / 8^{\prime \prime}$ twist drill turned by hand against the hole. The control panel aperture in the rear panel should also be cut at this stage.

It is best to mount the heatsink, capacitors and transformer onto the back panel before assembling the cabinet. Attach them using $5 / \mathbf{g m}^{\prime \prime}$ long No. 6. self-tapping screws and tighten down well to avoid the risk of strange buzzes etc caused by loose fittings. The interwiring of these parts is shown in Fig. 6, and 16/0.2 or a similar fairly heavy gauge wire should be used for all except the signal leads which must be single screened cable and the power leads between the PCB and amplifier which can be ordinary hook-up wire.

The cabinet itself can now be assembled. Start with the two long sides ( $B$ ) and glue and screw these into position against the rear panel (D). Similarly attach the two short sides (A) and finally the partition (C). In each case the screws should


Fig. 5 Construction of the cabinet.


Fig. 6 The positions of the principal components on the rear panel.


Fig. 7 Interwiring of the rear panel components.
be tightened into their countersunk holes until the heads are just below the surface of the wood.

Cut out a suitable piece of aluminium to form the control panel and drill holes to suit the potentiometer and input socket you plan to use. Wire these leaving $9^{\prime \prime}$ or so of free lead, drill suitable mounting holes in the rear panel of the cabinet and attach the control panel using self-tapping screws. Cut the free lead to length and solder it to the appropriate points on the PCB.


Fig. 8 Wiring of the components on the control panel.

Drill a ${ }^{1 / 4^{\prime \prime}}(6.3 \mathrm{~mm})$ hole in the rear panel, thread the mains lead through it and use a ' $P$ ' clip or other


Fig. 9 Front panel and drive unit mounting details.
retaining device to provide strain relief. Don't just tie a knot in the cable! Seal the hole around the cable with a suitable glue or filler so that the finished cabinet will be airtight. Complete the rear panel wiring by soldering leads to C 5 -ve and ground and leave the ends of these long ready for connection to the drive units.

Attention can now be turned to the front panel. Mark out the positions for the two drive units and use the template provided with them to mark the cut-outs and the mounting holes. The drive unit apertures can be cut by hand but it is much quicker to use a jig-saw attachment on a power drill. If the B200s are used, note that they are provided with ' $T$ ' nuts and drill the mounting holes out to $1 / 4^{\prime \prime}$ to accomodate these.

Assemble the prepared front panel into the cabinet and glue and screw it into place. Draw out the loudspeaker leads through one of the drive unit apertures, solder them onto one of the drive units and solder a second pair of leads in parallel. Return this second set of leads into the cabinet, pass them throught the hole previously drilled in the central partition and draw them out through the second drive unit aperture. Solder them onto the second drive unit, taking care to observe phasing, and the internal
wiring is complete. The unit should be left in this condition, with the drive units connected but not installed in the cabinet, while the initial testing is carried out.

Connect a lead to the input of the Neptune and fit a plug to the mains lead. Set the potentiometer on the control panel at minimum and switch on. Apart from the switch-on 'plop' no noise should be heard unless the ear is placed very close to one on the drive units. If there is no 'plop' or worse, if a loud hum appears, switch off immediately and check the wiring.

If all is well, advance the potentiometer towards maximum and touch the signal input terminal. This should produce a loud buzz. Again, if nothing happens, switch off and check the wiring carefully.

If this test, too, is successful, mount the two drive units in place. Don't forget to use the gaskets provided so as to ensure an air-tight seal. When this has been done, gently press one of the drive unit cones inwards using even pressure around the voice coil. The other cone should move outwards. If it doesn't, check carefully around the cabinet until you find the air leak responsible and plug it.

## Installation

No mains switching has been
provided on the Neptune because most modern stereo amplifiers are equipped with mains outlets and it is intended that one of these should be used. Such mains outlets are usually wired through the amplifier's on-off switch, so connecting the Neptune in this way removes the need to switch it on separately every time the stereo system is used. If your amplifier has such a socket, it is merely necessary to fit the appropriate plug to the mains lead, the most usual type being a shaver plug or an American-style twin flat-pinned plug. Leave about three metres or so of mains lead on the Neptune so that you can experiment with its positioning.

If your amplifier does not have a mains outlet, you will either have to fit an on-off switch to the Neptune or settle for plugging and unplugging the mains lead each time you use your stereo system. A mains switch could be added quite simply by enlarging the control panel slightly. Whichever approach you use, if the Neptune is switched independently of the amplifier you should always switch the amplifier on first and then the Neptune, never the other way around.

Connecting the input of the speaker to the output of your amplifier should pose no problems. With any luck you will have pressterminals on the amplifier into which the extra pair of leads can easily be inserted. If not, you will either have to make up an adaptor or add an extra socket on the back of your amplifier. Remember that you only need a connection from one channel of the amplifier and that it doesn't matter which one.

To set the unit up you will need a source of some description, preferably one offering signals containing male speech. A radio tuner set to Radio Four is probably best. Adjust the potentiometer on the control panel until there is no trace of 'boomyness' on the speech, then try the unit out with a music source. The bass response should have improved dramatically.

Experiment with the position and gain of the Neptune until you are satisfied with its performance. Remember that the best position is likely to be against the wall and floor and away from corners.

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# IC RELIABILITY 

## How reliable are standard ICs? What makes them not work properly?

Conventional wisdom has it that, after early failure, ICs are by and large pretty damn reliable. However, that doesn't mean that there aren't rogue or 'problem' devices - for example, see the telex reproduced here, about a device which was successfully used by a contributor to 'Electronics Monthly', but which has subsequently been withdrawn by the manufacturer.

```
84-10-30 14:2:1
8E11896ASFG
2372 GIMOSTG
3O OCT S4 ATTN: H ARMSTRONG TLX LON 3505
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Elsewhere in this issue, we carry details of a 'fix' for our original 64k DRAM card. This 'fix' was made necesary because we had a number of readers telling us that they couldn't get the dratted thing to work, and we couldn't get one that we had recently built ourselves to go - even after ammending the PCB in a couple of places!

Added to this we also had informal indications (ie, nothing you could quote anyone on) that the DRAM controller IC, 74 LS608, was a 'problem device'. So what makes a 'problem device'? We talked to Texas Instruments, the manufacturers of the device in question, to find out their side of the story.

Firstly, no one was aware of a specific problem with the '608, and we wouldn't identify the person who had told us that it was a 'problem device'. Although they could not locate any documentation to confirm it, there was the suggestion that there might have been some revisions to the die at a relatively early stage in the production run.

Looking at the DRAM card circuit, TI's engineers were not that happy about the delay sections formed by R1, C1, D1 and R2, C2, D2. The problem is that IC17a and $b$, the devices that immediately follow the delay circuits, are not Schottky devices, so the rise times from them would not be particularly fast, and this could cause problems with edge-triggered inputs. However, this was unlikely to be the cause of the problem here.

We then discussed the problems associated with the power-up of this and any other MSI device. This discussion was prompted by the section in the original article which suggested that some earlier production devices may have had problems with the power-on reset circuitry (which ties up with the suggestion that there may have been some revision of the die).

One of the problems with this and other computer add-on projects is that it is not possible to predict how power will be applied to the circuit - for instance, it may come on very quickly, there may be transients associated with ringing (although we hope that this sort of problem would be dealt with by most monolithic regulators), or the power might come on very slowly. The last of these is one possible cause of the problems with the DRAM card.

Different sections of a large or medium scale integrated device will start to function at different supply voltages. So if the supply voltage builds up very slowly after switch-on, it is possible, even likely in some cases, that fault conditions will develop that lead to a latch-up which will persist even when full power is applied to all sections.

Another problem is associated with ringing on input (or even output) lines. Readers will know how easy it is for a square-wave to acquire ringing - all it takes is a little unwanted inductance here, a little stray capacitance there, and bingo!, the square wave is ringing like Big Ben!

In a TTL (or CMOS) circuit, this can cause havoc. The problem is that the ringing excursions can take the input (or output) voltage above or below the positive or negative supply lines, respectively. This is a more manageable problem in discrete component circuits, because you always know what the real circuit is; however, with integrated circuits, there are always parasitic devices; eg transistors or thyristors, that have

## The TI Scare

Readers will remember that a little while back, it was alleged that possibly faulty chips had been sold on defence contracts. Quite a stir was created, with the story making the evening TV news and front pages of several papers.

The truth is a little more mundane, but in its own way equally alarming. According to a letter in the trade press (Electronics Times, 25 Oct) from Peter Van Cuylenburg, TI's MD, the ICs were properly tested. However, the tests did not conform to those laid down in the specifications for the devices, but, according to Mr Cuylenburg and to the Pentagon, the tests carried were actually more appropriate to the way the devices were to be used than the tests laid down in the specification.

However, no-one has yet explained how the wrong tests came to carried out and how it came to be that this was not picked up at a much earlier stage. This failure is, if anything, considerably more worrying than a few rogue devices finding their way into the system.
been produced inadvertently while making the wanted devices. This is as a direct consequence of all the devices on an IC being made on the same piece of silicon, and much of the design effort in laying out an IC is devoted to avoiding problems from parasitic devices.

The objective will be to ensure that, under normal operating conditions, the parasitic devices will all be biassed off. However, input and output conditions which exceed the supply lines - such as occur with ringing - can cause a parasitic device to come on, leading to the generation of a false logic state, or even to complete latch-up.

For example, some MOS DRAMs are very sensitive to over-shoot and under-shoot, and will latch up completely due to the presence of parasitic thyristors. However, so long as the signal lines do not exceed the supply lines, these devices will be perfectly reliable.

Whilst we're on the topic of supply lines, another problem is that they tend to be rather noisy, particularly in TTL circuits where fairly high currents are being switched. For this reason it is not good practice to tie any IC inputs to the positive supply line - although we
all do it. The safest option is to design around this in the first place, where this is possible, but otherwise tie inputs to the output of a spare gate, or use a pull-up resistor. Again, this is a particular problem with edgetriggered inputs, where noise on the supply line can lead to false triggering.

So do problem devices exist after all? TI are confident that all their devices meet the published specifications. That said, there will inevitably be some devices that will be rather more sensitive to circumstances of their use than one would like. Obviously, when introducing a new device, a semiconductor manufacturer cannot imagine - let alone test - all possible applications or circuit lay-outs. Basically, it is all too easy to inadvertently exceed the specification of an IC without realising it, and it will be only after extensive testing that you will find out what is going wrong. Fortunately, most devices are reasonably tolerant of minor violations on most of the specs.

Meanwhile, TI and ourselves will be investigating the 64 k DRAM card further, to see what has been causing the problem. We'll let you know of the outcome when we have something to report.
IC Testing

The testing that a standard IC goes through lasts all the way through its production process, and begins even before the wafer on which it is made is fabricated. The selection of materials, the growing of the crystal, the slicing of the crystal up into wafers and the growing of an epitaxial layer on the wafer are all closely monitored.

At every stage of the diffusion of dopants into the wafer checks are carried out on the resistivity of the silicon - obviously, this is influenced by the amount of impurity which has been absorbed.

Next, checks are performed on the test geometries that are placed on each wafer for no other reason. If you see a wafer before it is sliced up, you will notice that four or so dies are actually different from the rest - these are the test geometries, and simple go/no-go measurements can be carried out on these to detect gross faults.

The finished wafer then passes to a test bed where each die is tested as follows:

1. Basic electrical test;
2. Truth table check (does it do what it is supposed to do?);


Fig. 1 Typical IC failure rate against time - the actual timescale will vary, though.
3. Functional test (does it work in a circuit?)
4. Parametric test (does it live up to the fine print in the data sheet?).
Any dies that fail this test get a red dot of ink, and are discarded at the next stage, where the wafer is sliced up into dies and packaged. After packaging, every single IC goes through the same test programme again. Only after this do the ICs get 'symbolised' (ie, labelled).

The next stage is only carried out on military equipment or on larger dies, eg microprocessors; this is testing at an elevated temperature, and temperature cycling. This tests for two things: firstly, it will check to see that the die is properly mounted, otherwise the expansion and contraction will detach it; and it also accelerates early failures.

In fact operating at an elevated termperature greatly decreases the life of all devices, and one of the quality control tests that a competent manufacturer will be doing is testing samples of all devices at an elevated temperature to see how long they last. This can then be extrapolated back to devices used at normal temperatures to see if there is any sort of longevity problem with them.


Fig. 2. Long-term failure rate - electronic components should not wear out unless there are problems.

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# DRAM BOARD 

UPDATE

# Ahh! Doesn't it take you back to the balmy days of September 1983 when ETI first published its 64K DRAM board? The sheer technical excellence of the design, the excitement as you completed your very own memory card, the horror when you found it didn't work. Never mind, says Phil Walker, memories are re-made like this.... 

In September 1983 we ran a design for a 64 K DRAM board to connect to the Microtan 65 system or indeed any 6502 processor system. Although the original worked satisfactorily we received a number of letters from readers who could not get theirs to work. At first it looked as though there was a faulty batch of the 74LS608 controller chip around which the design was based but after a while it became apparent that it was "a problem device":

To overcome the shortcomings of the original design and to simultaneously incorporate some new features, last month's Experimenter's DRAM Card was designed. This removed the need for special ICs by using standard components. The only u nusual items were the $441616 \mathrm{~K} \times 4$ bit dynamic RAMs which were used because they allowed the PCB to be only partially populated when a significant proportion of the address space was not required.

Once this board was working on the author's 6502 system - which runs at 1.25 MHz , a little faster than the tangerine - it seemed reasonable that we should go back and do something for all those people who had built the 1983 project. To this end we have designed a small PCB which contains all the necessary control logic to replace both the 74LS608 and two other devices on the original board.

This PCB is mounted 'piggyback' fashion on the PCB once all the original control ICs and timing components have been removed.

All the original features relating to address space allocation are retained and the same PROM can be used. One thing which may be of interest to non-Tangerine users is that there is no longer any need for the $\varphi 1$ signal to be provided as all timing is taken from the edges of the $\varphi 2$ signal.

## The Circuit

This is identical in most respects to the control logic in last month's project. One significant difference is that the incoming select signal from the PROM is high to enable rather than low. However, since

## HOW IT WORKS

This is very much the same as for last month's Experimenter's DRAM Card project but we shall go through it briefly in relation to the original design.

All timing is performed relative to the rising and falling edges of the $\varphi_{2}$ signal from the 6502 processor. $\varphi 2$ is buffered by IC22a and by means of the delays in IC22b, C21 and 22. IC23 is triggered on both edges of 02 to produce the RAS pulse. The width of this pulse is controlled by RV21 in conjunction with C23 and R23.

A delayed version of the RAS signal is used as the MUX signal to operate the row/column address multiplexers. Shortly after this IC24a is clocked, and if $\varphi 2$ is currently high and the inverted SEL. line is low, the CAS output will go low and stay low until $\varphi 2$ goes low at the end of the processor access period. This keeps the data at the outputs available for longer when a read cycle is required. If $\varphi 2$ was low then the CAS output will stay high and a refresh operation will occur.

If all other conditions for a processor access cycle have been satisfied, to write data to memory the $R / W$ line will be low. This condition is gated with the state of the inverted $\varphi 2$ signal in IC22c and with the MUX signal in 1C22d. This ensures that the WE low condition is only asserted at the
requisite time.
At the end of each RAS pulse IC24b is clocked to sample the state of the $\varphi 2$ signal. The outputs of IC24b are used to enable and disable the address buffers and allow the processor or refresh addresses onto the memory chip address pins at the appropriate times. Doing it this way rather than with the $\varphi 1$ and $\varphi 2$ clock signals allows more settling time for the buffers and the refresh address counter before the RAS strobe occurs to start the next operation.

The last piece of circuitry to describe is the power-on-reset. This is produced by IC1b and c together with C25 and R21. D21 allows C25 to discharge rapidly when the power is turned off. By means of this circuit, IC23 and 24b are held in a defined state for a short while after power is applied. This allows the internal circuitry of the memories to become operational. This operation is required when power is applied, not when the processor is reset. Note also that eight RAS only cycles shouid by performed after the power-on-reset before the memories are fully operational. However this will usually be taken up by the system initialisation routines reading from ROM.


Fig. 1 Circuit diagram of the new control logic.
there is no G pin on the 4164 devices, the inverter which previously provided this signal can now be used to invert the SEL line and enable the data buffer at the appropriate time.

The other difference is in the $\overline{\text { WE }}$ circuitry. The lack of the G pin on the 4164 means that, if we want to connect the data - in and data out pins of the memory chips to the same data bus as in the original


Fig. 2 Timing diagram for the control logic showing how all of the signals are derived from $\varphi 2$.
design, the write cycle must be the so-called 'early write' detailed in the data sheet. This requires that the WE signal go low before the $\overline{C A S}$ signal goes low. If this is not done the data outputs of the memory chips will become active and may try to drive the data bus into a state opposite to that of the bus buffer.

## Construction

Construction of the PCB itself is quite straightforward. Remember that there are four wire links to be inserted as this is a single sided board. If height is likely to be a problem then solder the ICs directly into the PCB but otherwise use sockets. The other components are simple to install but the usual care should be taken to get polarities correct.

Assembly onto the main board should be postponed until the addon board has been tested. You will need access to a signal generator giving a 1 MHz TTL compatible square wave signal and an oscilloscope with which to see the results.

Connect a suitable +5 V supply to the board and check that the current drawn is not more than


Fig. 3 Component overlay of the PCB.

100 mA or so. Connect the SEL testpoint to 0 V and a 1 MHz square wave TTL compatible signal to the $\varphi 2$ test point and monitor the signals on the RAS, CAS and WE test points. Only RAS should show any activity at this stage and its low time should be set to about 300ns by means of RV21 (one half to three-quarters clockwise rotation). Both the CAS and WE signals should be high. A worthwhile check at this stage is to see that SKB pins 6 and 9 are switching at the same rate as the $\varphi 2$ signal but phase shifted from it. Also check that the MUX signal at SKA pin 11 is similar to the RAS signal but slightly delayed from it (RV22 should be set to approximately one quarter of its clockwise rotation). Note that the RAS and MUX signals are at twice the $\varphi_{2}$ frequency.

So far we have checked that IC21e, 22a \& b, 23 and 24b are working. Now set the SEL test point to +5 V , or just open circuit the link you previously inserted, and check that the CAS test point shows low pulses but only while $\varphi 2$ is high. The RAS to CAS delay time can be adjusted by means of RV22 if required but will only be critical if you have a slow processor.

There are only two other sections to check. Monitor the WE output and check that, with the R/W
input open circuit or logic high, this output is also permanently high. Applying a logic low or OV signal to the input should cause the WE output to produce a series of low pulses, at the same rate as $\varphi 2$ but with the same width as the MUX low signal. The WE pulses should only occur when $\varphi 2$ is high.

The last thing to check is the power-on-reset. If possible, monitor the RES test point and the voltage across C25. Temporarily short circuit C25 and check that the test point stays high for a few milliseconds after the short is removed.

By now you should have a fully tested board and will be ready to connect it to the original DRAM. First disconnect all the wires you used in the testing phase and connect 22 SWG tinned copper wires to the SKA and B positions. Cut these off flush with the top side of the board but leave them about 25 mm ( 1 inch) long on the wiring side.

Next remove IC16, 17 and 18 from the original PCB together with their sockets and R1 to 6, C1 to 6 and D1 to 3. If you have not corrected the original PCBs you should now connect IC1 pins 2 and 12 to 0 V , IC3 pin 9 to IC4 pin 9 and the tracks going to EC2a and 2 b to EC3a and 3b respectively instead.


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# THE OTHER END OF THE SCALE 

# Single-bit microcomputers are alive and well - and will soon be living in your washing machine or TV. James McGuigan, System Engineer at Motorola Semiconductor Products Sector, East Kilbride, introduces the MC6804P2 single - chip microcomputer. 

Single-chip microcomputers are set to invade our homes! Like Greek warriors, they'll be hiding inside Trojan horses, although these horses will look more like washing machines and TV sets.

Actually, it's all very logical and nothing to worry about. Mechanical controls are unreliable and expensive to make, and for some time electronic controls have been replacing them in a large range of applications. What could be more logical than using a single-chip microprocessor to replace a board-full of $\Pi \mathrm{L}$ or CMOS, and, at the same time, upgrading the 'intelligence' of the control unit.

This invasion will be self-reinforcing: the more devices use the single-chip microcomputers, the cheaper and better known they will become, and so more devices will use them. Prime targets will be TVs and videos, games, toys, cameras, motor vehicles, power tools and domestic appliances. For example, the device here could be used to control a TV set, tuning in the channel selected via a phaselocked loop, controlling the sound level by a voltagecontrolled potentiometer, and accepting instructions from a remote control unit.

Motorola's involvement in single-chip microcomputers started with them second-sourcing MOSTEK's MC3870. Motorola's first 'home-grown' single-chip device was the MC6801, which was on the market in 1978.

As you might expect, the MC6801 had quite a lot of the same circuitry the MC6800 microprocessor - why re-invent the wheel when you can use something that you know works? Additional circuitry included program memory (ROM) and data memory (RAM), besides input/output ports, a serial communications interface and a multifunction timer.

In 1979, the availability of improved chip fabrication techniques allowed the size of the chip die - the actual piece of silicon on which all the clever stuff is mounted - to be reduced. The technology used is refferred to as HMOS (High density n-MOS) and involved the use of interconnections on the silicon of 3.9 um width (by comparison, Motorola are presently preparing themselves to use tracks of 1 um or smaller). The size of the die makes quite a difference to the price of the final IC, so this change allowed the price to fall.

Also in 1979, Motorola introduced the MC6805P2. This was essentially a development from the 6801; it had been found that most applications did not require as sophisticated a register set as the 6801 provided, and so these were reduced. The RAM and ROM were reduced in size, and the timer was simplified, and the serial interface was dropped.


Fig. 1 Eight-bit parallel adder with ripple-through carry.
There are now a series of devices in the 6805 family, all with different bells and whistles added to make them more appropriate to particular control or other applications.

## All Change

The MC6804P2 represents a major change in direction for Motorola's single-chip computers. Not only has any resemblance to the 6800 been abandoned, but the whole basis for the architecture has been changed. The major difference is that the 6804 uses serial rather than parallel architecture. However, Motorola have managed to work the trick of making the 6804 appear to be an eight-bit device to the user. The whole purpose of this is to reduce thediesize, which, as we've already observed, reduces the cost of the finished IC. Let's take a closer look at what having serial architecture actually means.

Conventional microprocessors manipulate data in lots of eight bits, ie bytes. For example, the central processing unit (CPU) and data bus are eight bits wide. An address bus and program counter (PC) of 12 bits wide can access up to

4096 bytes (4K) of data.
With the 6804 family all the hardware is actually only one bit wide. All data transfers, arithmetic and address operations are carried out serially one bit at a time. This means that the CPU, data bus, address bus, program counter, timer and prescaler are all only one bit wide.

Consider, for example, an eight-bit arithmetic and logic unit (ALU). Within this ALU we have an eight-bit adder to add two eight-bit numbers $A$ and $B$ (and possibly a carry-in bit as well). The adder will have eight sum bits and a carry-out bit as its output.

The eight-bit adder will be made up of eight separate single-bit full adders as shown in Fig. 1, which shows a 'ripple-through' adder configuration. First of all the least significant bits AO and BO are added to Cin. The sum appears at SO and any carry 'ripples' through to be added to the sum of A1 and B1. This carries on until the eight-bit sum of $A$ and $B$ is calculated.

The eight-bit adder described above uses eight singlebit full adders plus three registers to hold A, B and their sum - this is a lot of hardware and consequently expensive. However, it is possible to make do with just one single-bit full adder as shown in Fig. 2. This serial adder is made up of one single-bit full adder, three shift registers and a D-type flip-flop.

When two eight-bit numbers are to be added, they are loaded into shift registers A and B. The least significant bit is to the right and the most significant bit is to the left. On each clock pulse, registers A and B are shifted one bit to the right. The bits which 'fall out' of the registers provide the inputs to the adder along with Cin. The adder's sum output is shifted into the SUM shift register. Any carry from this single-bit addition is latched by the D-type flipflop.


Fig. 2 Eight-bit serial adder using only one full adder.
Obviously, the serial method is somewhat slower but there is an enormous saving in hardware and, consequently, space. Consider now the above principles applied to microprocessors. If we can reduce the amount of on-chip hardware then considerable savings can be made in chip size. A smaller chip size means that more can be fabricated on to a silicon wafer. In turn, this means increased productivity and cheaper processors.

Of course, the serial approach is always going to be slower than parallel design but there are many applications in which speed is not critical. In any case, with the 6804 provision has been made to permit the use of very high clock speeds: the maximum external oscillator frequency for the 6804 P 2 is 11 MHz .

The following description applies mainly to the MC6804P2 version with mask-programmed program ROM; however, the soon to be released MC68705P3 EPROM version is similar to the point of pin-compatibility. Also, a wide range CMOS (as opposed to NMOS) devices are planned and these will also be very similar.

## In More Detail

Figure 3 shows the MC6804P2 block diagram. The CPU contains the ALU, control, stack and registers. Memory consists of three areas: program ROM (1K), data memory ( 64 bytes ROM and 32 bytesRAM) and the stack. The timer circuitry is made up of prescaler, counter and control



## Fig. 3 MC6804P2 block diagram.

registers and oscillator circuitry. The 6804P2 also has 20 versatile 1/O lines.

The CPU is similar to that of the 68705P3. However, there are some differences. The eight-bit accumulator is memory-mapped at address \$FF and has indirect registers which replace the index register on the 68705P3. The indirect registers are memory-mapped at locations $\$ 80$ and $\$ 81$.

There are only two condition code flags on the 6804P2, $C$ and $Z$, and there is no condition code register. The flags used for normal processing and interrupts are different. With interrupts, the processor automatically uses the interrupt-mode flags and, on return from interrupt, the normal-mode flags are used. Previous flag states will be used when switching from one set to another.

The stack is used to store subroutine and interrupt return addresses. It is a hardware stack, 12 bits wide and four levels deep (ie equivalent to a 48-bit shift register). Its last-in, first-out (LIFO) configuration eliminates the need for a stack pointer.

A crystal, R-C network or external signal can be used to generate the system clock. A mask option selects either the crystal or R-C network oscillator circuit.

The oscillator frequency is divided (internally) by four to produce the internal clock. This in turn is divided by twelve to produce a machine cycle. A machine cycle is the smallest unit needed to execute any operation and an instruction may need two, four or five machine cycles to execute.

To facilitate testing, a signature analysis circuit has been included on the chip. The circuit consists of two eight-bit shift registers (memory-mapped at addresses \$OA and \$OB) configured to perform a Cyclic Redundancy Check on the ROM. The CRC registers can also be utilised as a pseudo random number generator as a result of continuous CRC calculations being performed.

## Memory

The 6804P2 has 1 K of program memory which contains all instructions to be executed, immediate data and interrupt vectors. Figure 4 shows the 6804P2 memory map. Data space comprises 64 bytes of ROM for constants and tables, all 32 bytes of RAM and the I/O, timer and CRC registers. This configuration is different from the 68705P3 where program and data memory are combined in a von Neuman architecture (ie there is no distinction between program and data storage except that some areas - the EPROM sections - cannot normally be written to).

Note that only the PC is stored on the stack. Any other registers have to be saved in RAM by means of software and reloaded at the end of the subroutine or interrupt routine. On a stack push the bottom register always 'falls out' of the bottom of the stack. The stack should not be pulled more than four times in succession without any pushes.


Fig. 4 MC6804P2 address map.

## Timer

Timer circuitry for the MC6804P2 is shown in Fig. 5. The timer comprises an eight-bit timer counter register (TCR) with a seven-bit prescaler and a timer status control register (TSCR). These registers are all memory-mapped and are readable and writeable.

The TCR is clocked towards zero by the prescaler output. The prescaler is used to provide longer or shorter timer intervals by dividing the input clock. The prescaler tap is selected by bits 0-2 of the TSCR - giving a range of divide-by-1 to divide-by-128.

PSI, bit 3 of the TSCR, is used to initialise the prescaler (to \$FF) and inhibit counting when logic zero. The TCR is also inhibited but its contents are unchanged. When $\mathrm{PSI}=$ 1 the prescaler begins to count.

Unlike the 68705P3, the 6804P2's timer can operate in both input and output modes. Bit 5 of the TSCR, TOUT, selects output when high and input when low.

As an input, the TIMER pin is connected directly to the prescaler input. Therefore the prescaler is clocked by the signal on the TIMER pin. The prescaler then clocks the TCR which sets bit 7 of the TSCR (TMZ) when it reaches zero. TMZ can be tested by software to perform a timer function whenever it goes high.

Operation in the output mode is somewhat similar to that for input mode. With TOUT = 1, the TIMER pin is connected to the DOUT latch and the prescaler is clocked by the internal sync pulse. The positive-going TMZ transition latches the DOUT bit and provides it as an output for the TIMER pin. Note that TMZ can be set by writing zero to the TCR or by setting TMZ directly.

## Interrupt And Reset

Processing can be interrupted by applying a logic low signal to the IRQpin. Whether the negative-going edge or the actual low level is sensed is determined by a mask option. With the 68705P3, however, we have a choice of three interrupts, external, timer and software. The flowchart in Fig. 6 gives a detailed description of 6804P2 interrupt handling.

On power-up the interrupt mask is set. This blocks any


Fig. 6 Reset and interrupt processing flowchart.
'ghost' interrupts from occurring. To clear the interrupt mask the programmer should jump-to-subroutine (JSR) to an initialisation routine as the first instruction in a program. This initialisation routine should be terminated with an RTI instruction instead of TRS since RTI will not only restore the PC, but will also clear the interrupt mask.

During power-up a short delay - to allow the internal oscillator to stabilise - is needed before allowing the RESET line to go high. The configuration in Fig. 7 provides sufficient delay.

Interrupt and reset vectors on the 6804P2 are actually JMP instructions to the interrupt or reset routine which are placed at fixed addresses in the Program ROM. With the 6804P2, a vector fetch forces an address value into the PC, whereas with the 68705P3 a vector fetch forces an address value directly onto the address bus. Figure8shows the manner in which resets should be programmed.

## Input / Output Ports

All 201 /O lines are programmable as inputs or outputs by setting the corresponding bit in the appropriate data direction register (DDR) low or high respectively. On reset the port data registers are not initialised but all ports are configured as inputs. To avoid undefined levels it is a


Fig. 5 Timer block diag

# FEATURE : Single Chip Computer 



Fig. 8 Program flow after reset vector fetch.
good idea to write to the data registers before writing to the DDRs.

When programmed as outputs, the latched output data is readable as input data regardless of the logic levels at the output pin due to output loading. Figure 9 shows typical port circuitry.


Fig. 9 Typical I/O port circuitry.
All ports are LSTTL compatible as inputs and outputs. Port B outputs can also drive LEDs, with suitable current limiting resistors. The user can select one of two mask options (for all ports) as either pullup resistors for CMOS output compatibility or open-drain output; see Fig. 10 for typical port connections.


Fig. 10 Typical port connections.

## Software And Instruction Set

The MC6804P2 has a rather unique, byte-efficient, instruction set. There are 41 instructions with opcode and 17 assembler-recognised instructions. Figure 11 shows the 6804 P 2 opcode map. The instruction set is similar to the 68705P3 including true bit manipulation plus a 'move immediate data' instruction.

BSET/BCLR can set or clear any register or RAM bit. BRSET/BRCLR can be used to test any bit in data space (including ROM) and branch or not as a result of the bit's state. The C-flag is set to the value of the bit referenced by BRSET/BRCLR. Bit manipulation allows the user to have individual flags and to handle the I/O bits individually with ease.


Fig. 11 6804P2 op-code.

The 'move immediate data' instruction transfers immediate data into data RAM and has the format 'MVI ADDRESS DATA'. Previously, on the 68705P3, data had to be loaded and stored through the accumulator. This takes up 4 bytes of ROM but only 3 on the 6804P2 when the MVI instruction is used.

The implied instructions shown in Fig. 12, exist because the accumulator and indirect registers are in RAM. For example, bit manipulation of bit 7 of the accumulator and indirect registers can give pseudo-ops such as BRSET $7, \$ 80$ for 'branch if $X$ minus' (BXMI), BCLR $7, \$$ FF for 'ensure accumulator positive' and ADD \$FF for ASLA.

The 6804P2 has nine addressing modes. In summary these are immediate, direct, short-direct, extended, relative, bit set/clear, bit test and branch, register-indirect and inherent. Most of these modes are similar to those used on the 68705P3. However, short-direct, relative (-short), register-indirect and inherent addressing modes use only one byte.

There is no indexed addressing as on the 68705P3 but register-indirect addressing is the same except that an offset cannot be used. This addressing mode works on ASSEMBLER RECOGNISED INSTAUCTIONS (OERAVED)
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Fig. 12 Implied instruction set.

RAM location $\$ 80$ and $\$ 83$, ie the $X$ and $Y$ indirect registers and two others. A typical register-indirect instruction is CMP $(X)$ which compares the contents of the accumulator with the contents of the address pointed to by the indirect X-register.

## Summary

The Mc6804P2 is the first of a new family of Motorola single-chip microcomputers. Its unique architecture means that it can offer eight-bit power at a four-bit price.

As mentioned earlier, EPROM versions will soon be available and are ideally suited for use by hobbyists for a wide range of applications. Anyone used to working with Motorola's M6805 family will find the new 6804 range surprisingly simple to use.
(For further details of other single-chip microcomputers, we suggest 'Single Chip Microcomputers', Edited by Paul F. Lister, published by Granada publishing Ltd, ISBN O-246-12106-8).

ETI

# THE ETI READERS' SURVEY 

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mods
Designed from scratch
(with a few sections
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## 21.

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26 way
34 way
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50 way
60 way
SOC
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16 way
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| ETS | DIP PL | JGS | D-TYPE |  |
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| 0.88 | 14 way | 0.92 | PLUGS |  |
| 1.06 | 16 way | 1.06 | 9 way | 138 |
| 1.16 | 24 way | 1.60 | 15 way | 1.85 |
| 1.38 | 40 way | 2.40 | 25 way | 2.52 |
| 1.66 <br> 1.94 | TRANS |  | 37 way | 3.34 |
| 2.08 | CONN |  | RIBB | 迷 |


| 2.08 | CONNS. |  | RIBBON CA |
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| 278 | 10 way | 0.86 |  |
| 3.34 | 16 way | 1.17 |  |
|  | 20 way | 1.37 | 10 |
|  | 26 way | 1.67 | 14 |
|  | 34 way 40 way | 187 2.23 | 15 |
| 1.84 | D-TYPE |  | 20 |
| 3.14 | SOCKE |  | 25 |
| 3.80 4.90 | 9 way | 1.47 | 34 |
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# DIGITAL FRAMESTORE 

# Now we come to the two nitty-gritty bits of the circuitry - the conversion to and from digits, and the storage and retrieval of the digits in a hurry. Daniel Ogilvie shows how its done. 

with a clock rate of 13 MHz we have $1 / 13 \mathrm{MHz}=78 \mathrm{~ns}$ to convert the data and store it in memory. Of the readily available ADCs, the National Semiconductor ADC0800 takes 10 $\mu$ s; obviously, we will have to look for something rather more exotic for the ADC here.

Most common ADCs work by the successive approximation technique, which requires a number of clock cycles to obtain a digital representation of the incoming analogue signal. Even at high frequencies, the number of clock cycles would take an unacceptable length of time; for instance, if we were able to clock the ADCO800 at 10 MHz , it would still require 40 clock cycles to complete a conversion, which would mean that we would have to allow $4 \mu \mathrm{~s}$ for each conversion - still far too slow.

Successive approximation ADCs contain just one comparator, see Fig. 4, and what they do is to try the different bits in the latch, starting with the most significant and working down to the least significant, to see which should be on in the final result.

An alternative technique is used by flash (or parallel) converters; here, there are lots of comparators all tied to the input and to different points in the resistance ladder. The encoder logic has to decide which is the highest comparator which is on. The time taken for conversion is just the propagation delay of the comparators and the encoder. However, the big disadvantage of these ADCs is the complexity, as there has to be a comparator for every possible output word. So, for an n-bit converter, there have to be $2^{n}$ comparators, and this also means
that there have to be more resistors in the chain, and that the encoding logic has, necessarily, to be that much larger.

There are a number of flash converters on the market, the Ferranti ZN440 and the RCA CA3300 for example. The type we are going to use is the TRW TDC1014, which is a six-bit converter. Both eight-bit and four-bit versions are available and could be used instead; however, the four-bit version will not offer sufficient resolution for any serious application and the eight-bit version is very expensive, in effect containing four times the logic and comparators of the six-bit version. The six-bit version is a compromise.

The ADC is the single most expensive item in the framestore. It does contain a lot of very fast logic, including 64 latched comparators, for example. Its cost is about $£ 100$, and as we have seen there is no way round this. The framestore can, of course, be built without the ADC and used only to display images loaded by computer - not exactly a framestore then though is it?

## The Dynamic Ram

The DRAM is a significantly cheaper memory cell per byte than static RAM. It would be possible to design the framestore using fast (better than 70ns) access time static RAM, which would consume over $10016 \mathrm{~K} \times 1$, for example. These would require a second mortgage to acquire ( $\{10 /$ chip). So if only for financial reasons the DRAM would appear to be the right choice and the $64 \mathrm{~K} \times 1$ variant is the cheapest and most convenient available for us. However they do require more thought and circuitry to drive them. The problem of their slow access
time is discussed below. We will consider briefly here how to get data in and out of them.

You have probably noticed that the $64 \mathrm{~K} \times 1$ DRAM comes in a 16 -


Fig. 4 Two ways of converting analogue to digital: (a) sucessive approximation ADC; (b) 'flash' converter ADC.


Fig. 5 Circuit diagram of the converter section.
HOW IT WORKS - ADC/DAC

R1 terminates the video signal at the appropriate 75 ohms. Q1 buffers the video, and the signal is then AC coupled to driver transistor Q3 via C2 and R5. Q3 is needed because the input to IC1, the ADC, is quite capacitive ( 100 p ).

The DC level of the signal is determined by the clamping action of Q2, as follows. IC3 is a dual monostable, and it generates a $2 \mu \mathrm{~s}$ pube 3 / $\mu \mathrm{s}$ after the LNE signal goes low, which is every $64 \mu \mathrm{~s}$. This pulse is fed via Q4 to the gate of Q2, which turns this transistor on, shorting the negative end of $\mathbf{C 2}$ to the voltage set up by R6 and RV1.

The portion of the video waveform when this is happening is known as the 'back porch', and, by definition, it is reference black. So R6 and RV1 set the reference black level for the video signal. Clamping the waveform every $64 \mu \mathrm{~s}$ ensures that the tone of the image remains consistent across the screen.

The ADC is IC1, a IDC1014), which converts continuously at 13 MHz . 10 ns after the rising edge of the clock input, the video input is latched into its comparators and compared with the voltage fed to the reference input. This latching operation means that the input does not have to be held steady while the conversion is taking place.

On the falling edge of the clock signal, the comparator outputs are fed to a 63 -to-6 decoder. The outputs from the comparators essentially form a bargraph representing the video signal size: for example, if the video input is half the reference voltage, then half the comparators will be on and half will be off. The conversion logic takes the bargraph output and converts it into a sixbit binary word.

The binary word is latched into the ADC output on the next rising edge of the clock and the data becomes available 30 ns later. There is what is known as a one pipeline delay in the output, and the ADC takes in new data whilst converting the previous data.

The reference voltage is provided by ZD1 and this is buffered by IC2. RV2 allows the reference voltage to be changed which gives some control over the gain of the ADC; the lower the reference voltage, the lower the threshold between adjacent comparators in the ADC, so the smaller the change in the input signal that is required to change from one output binary word to the next.

IC5 is the DAC, TDC1016. It acquires data from the memory on the rising edge of the clock input provided that the data has been set up 20ns beforehand. The reference input,
provided by ZD2 and buffered by IC4, is used, with the digital data, to decide the size of the output voltage. The output of the DAC can be forced to $0 V$ (black) by the NDIS input and this is done outside the stored picture area to prevent rubbish being displayed.

The output of the DAC can drive the standard 75R line, but will provide only 500 mV output swing, which will give disappointing contrast on a monitor, which would be improved by amplifying the output. On the other hand, without termination, the output voltage swing can be 1 V but fast edges of the video could cause some slight overshoot, although it is unlikely that such edges would be generated by anything other than a computergenerated image.

In the circuit shown, we leave the choice of whether or not to terminate the output from the DAC with 75R up to you; the resistor required to do this is shown dotted. The black level of the output is set by the ratio of R20 to R21 and when a MIXED SYNC pulse is present, this point is shorted to OV by Q6 to provide a composite output.

Q5 provides a 75R drive capability for the video. No low-pass filtering has been used to reconstitute the video output, as this will almost certainly be performed by the monitor.
is performed by strobing RAS low and providing a sequential address address bus. However when DRAM is read it destroys the data in the cell which must be automatically

 picture and therefore by ensuring the RAS addresses are the loworder address lines, refresh is Speedy Shifting
To store a picture to

To store a picture to our
 bit word to be converted by the 78ns. We have (I hope) justified our WVYG isplsef ayt ing WVy गlpels that we can procure is 100 ns and
 -nof ssajor of sn molie jeyi sw yyd


 humble shift register. We can use

generate a write pulse; the data is pin package and yet would require
become valid. These are synchronously
loaded into the eight-bit data shift



The address inputs to the RAM have 33R resistors in series with them to damp possible destructive negative
voltage excursions on the address lines votage excursions on hae aldress ines
due to the high capacitance of the DRAM inputs and the PCB tracks.
Should we wish to load data into the
RAM we need to pull down the write
 time; this is handiled by the control card. Data from the ADC is clocked into
the shift registers. When eight bits have been loaded, the $Q$ outputs of the shift register are loaded into an eight-bit latch on the iosing edge of the transier

or the nex write cycle oo the board is
Any additional $/ \mathrm{O}$ for MPU access and will be discussed in

The type of RAM shown is Motorola counter which can make interfacing to an MPU a little easier. However any 64 K
 timings. The memory chips used cannot possibly work at the speed at which the frame-
store converts analogue to digital or vice versa; so the design here uses shift registers to convert eight serial bits parallel data word, which is then stored

 working at; however, this does have the disadvantage that effectively six
memory cards are required. for just one storage card; all the connections to this are paralleled with the other memory cards, except SI, the serial data input bit
from the ADC, SO, the serial data out to the same bit on the DAC, and MPUD, which is connected to one bit

The dynamic RAM is usually being ead. RAS is strobed
lower address bits ( $A 0$ - $A$ I) have settled. After the RAS hold time of the dynamic RAM the upper address lines are enabied and CAS is strobed low. The
16 -bit address bus is multiplexed to eight bits by the two 'LS257 two-to-one multiplexers. The select line is the to output of the control card. After the


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# SYSTEM FAILURE 

# The UK's defence industry isn't delivering - either in terms of reliability, which is this report's main concern, or in commercial and export terms. Dave Bradshaw has been talking to a very experienced engineer, working in defence, to find out why. 

Like it or not, each adult in the UK contributes several hundred pounds a year to the defence industry (the exact figure is not easy to calculate). A large proportion of our electronics engineers are employed in this industry, either directly or indirectly, and much the largest share of all research is conducted for military purposes.

With all this effort going on, it is important to ask whether we are getting value for money, because it would represent a huge waste of resources if we were not. To give value for money, a military system must work, ie it must be reliable. But there are are very serious question marks against the reliability of some systems. For example, when the Belgrano was sunk during the South Atlantic conflict, conventional torpedoes were used even though the submarine which did the sinking was believed to have 'Stingray' torpedoes aboard. Why? Could it be that the sub's captain didn't trust the high-tech torpedoes to do the job?

The problem with torpedoes is that if the first one misses, it gives the enemy warning that an attack is being mounted, which in turn gives time for preventative action to be taken. So a very high degree of reliability is necessary for torpedoes. On the other hand, another high-tech weapon, the Exocet, was used with devastating effect. Here, the circumstances are different, because if the weapon fails, it might not alert the enemy, but just crash into the sea. Even if the attacker is unlucky enough to alert the attacked, there is still ample time to launch another missile, because the target is slow-moving and the attacker is much faster.

So 'reliable' can mean different things in different circumstances. When there was a scare over some chips manufactured by TI not having been correctly tested, BAe publically stated that they had used the chips in question in the Rapier missile, and that the missile had an $80 \%$ success rate which was considered to be very good. In weapons terms, Rapier is a low-complexity, high-reliability weapon.

An example of about the most complex weapons system in service at the moment is the Tornado multirole combat aircraft. Each major 'service' on a Tornado takes about three months, and that will involve the stripping down of all the systems and sub-systems, and the thorough testing of them all, both individually and in an assembled state. However, by the time the Tornado has landed after its first flight, it has several systems that are not fully functional, and it has to go for further repairs. The F1-11 has similar problems.

It requires a major maintenance effort to keep aircraft like this functional. By contrast, the Harrier is very robust and simple, despite having a particularly highly stressed engine. And we've given Harrier technology away to the USA, because we preferred to concentrate on Tornado.

The remainder of this report will look at the factors that affect the reliability of military hardware. One of
the problems we have encountered, though, is that while there are countless examples of blunders committed in defence contracts, the actual examples we might be able to give are all covered by the Official Secrets act. In the vast majority of these cases, the details of the mistakes have very few if any defence implications. They do have very large implications for the companies involved in defence. It would be in the long term public interest if details were known - but they cannot be released. Perhaps this is one of the reasons why the British defence industry is losing ground in competing for orders against the Israeli and French industries?

## Specification

The specification is basically the document in which the customer says what is required. It is one of the most critical stages in the procurement of a piece of military equipment, and mistakes made here can be difficult if not impossible to rectify. There are a number of 'golden rules' - many of them little more than common sense - which should be followed, but which are all breached to a greater or lesser extent for much of the time. Let us take a look at the rules. They are:

1. The specification must say exactly what the customer wants. There is no room for vagueness, as this will inevitably by exploited in one way or another by one or more parties to the deal.
2. The buyer must understand the specification and all the implications of what is being asked for. This may seem obvious, but contracts are usually drawn up by non-technical staff, at least in part.
3. The contractor, designer, developer and producer must all understand the specification; again, there is a problem of the contract being negotiated by nontechnical staff, with the result that it may be inconsistent or open to several different interperetations in key areas.
4. The specification must be complete and must not leave anything out. Here there is the problem of the wrong priorities being emphasised in the drawing up of the spec, but there are additional problems. Military contracts generally run for around ten years from start to completion, but in 1984 it is impossible to predict what circumstances equipment will find on the (hopefully theoretical) battlefields of 1994. Also the sheer complexity of military items can make it virtually impossible to describe them fully - imagine trying to write a full description of a multi-role combat aircraft. 5. Another problem associated with the contracts running for so long is that you cannot be sure that the device will be used as it is designed to be used. If the design work is done ten years before deployment, the actual way it will be used cannot be predicted.
5. The device must be testable, and this must be built into it from the start. Inevitably, there will be aspects that cannot be tested, and it must be understood how


Fig. 1 Reliability declines with servicing.
much cannot be tested and how important that is to the system.
7. It must be possible to test the device without degrading it too much. One of the ironies with large-scale systems is that testing them actually makes them less reliable in the long run, see Fig. 1.

Let us pursue this question of testing a bit further. Large-scale weapons systems have some sort of self-test capability (ie BITE, built-in test equipment). Others, like missiles, will have an associated test box, so that you can plug the missile into a box of tricks that will then put the missile through its paces, testing the main routines that the missile's equipment will have to perform in actual use. This test might be a daily, weekly or monthly ritual, depending on the device in question.

Such a test can only give a partial check on the system, so periodically the whole missile will be taken apart, all the sub-systems in it tested, then it will be reassembled and given a full system test which will, so far as is possible without actually firing the missile off at a target, test the full system under simulated systems conditions.

There are several problems here. Firstly, without firing the missile, you can't fully test it - and there are major aspects of the operating environment you just cannot simulate. For example, you cannot simulate the launch satisfactorily. There are so many combinations of conditions that the missile may encounter that you cannot test them all.

There is a whole range of one-shot devices in any system that cannot be tested; these range from the warhead itself to explosive bolts. Testing these destroys them and they can only be replaced with similar items which, again, you can't test without destroying.

A further problem with mechanical parts of the system is that even after testing you cannot be sure that they will work. An example would be the wings and engine air-intake on a cruise missile. There are so many variables involved here that can prevent these from working, for example dirt or debris that entered the mechanisms during testing, or small mechanical deformations accidentally introduced in re-mounting the missile. All that you can say is that the mechanical bits worked when tested, but you cannot be sure that they will work the next time they're called upon.

There are particular problems with integrated circuits. After each step of building an IC - and this includes the different diffusion stages of the wafer - the IC is tested and inspected, to see that everything has been done properly. Once the IC is capped (encapsulated) you cannot go back to check on earlier stages, so you're confined to just checking to see that it
behaves, so far as you can test, in line with its specifications.

## Burnt Out?

One of the principles behind the reliability verification of systems is that of burn-in. The idea is to make sure that the large numbers of early-life failures that occur with any device - be this individual ICs or a largescale system - occur on the test bench rather than the battle-field. Failure early in the lifespan is somewhat tastelessly referred to as 'infant mortality'. These are usually caused by gross failure mechanisms due to manufacturing shortcomings (eg, dry joints, unsecured components, poor insulation, etc).

The idea is to create the worst possible operating conditions in which the device must operate, and subject it to these conditions for a period of time- typically 168 hours (one week) for high reliability ICs - and see if it fails. Individual devices, eg ICs, are burnt in, then they're assembled into boards and burn-in repeated, then the boards are assembled in sub-systems and the burn-in repeated, and finally the whole system is assembled and burnt in.

If the burn-in procedures are not adhered to fully, faults will get through and end up appearing in the finished items of equipment. Combined with the effects of long-term degradation, such infant mortality faults can appear to be random failures - except that these 'random' failures would be occuring rather more often than would be expected. However, it is difficult to distinguish between random failures and a quality control problem due to inadequate burn-in.

Manufacturers are under quite a lot of commercial pressure to curtail burn-in where possible. It costs a great deal of money and ties down resources. For example, assembling even the smallest system could take four weeks and tie up environmental testing facilities for that length of time as one week will be required for each stage - burning-in the components, the boards, the sub-systems and the system as a whole, albeit in different sections of the factory, or in different factories.

Even with an apparently adequate 'burn-in' programmme, we still come back to the problem that you cannot adequately reproduce the full operating conditions. For example, the way components are mounted can count for a lot. If they are mounted in such a way that they can vibrate, it is not unknown for them to go into a very destructive mechanical resonance during, say, the launch of a missile.

## Contracting

The commercial arrangements surrounding military contracts have strong repercussions on the reliabilities of the eventual products. Until recently, all contracts used to be on a cost-plus basis - the contractor would be paid as much as was spent on a particular project plus an agreed profit margin. As you might imagine, this was a licence to print money for the contractor, but it also encouraged very bad habits on the part of the customer.

The main problem was that the military would continue to change the specification of the equipment required right the way through the contract's life. These changes would be called 'enhancements', although they would frequently be incompatible with the
original specification. These 'enhancements' might be trivial - for example, the moving of a bracket - but they might also be quite large. An accumulation of apparently trivial changes can amount to a major design change.

During the typical contract life of ten years, the military would be going back to the contractor with 'enhancements' for virtually the full life of the contract, almost as a matter of course. Over ten years there will be a considerable change in the technology available, and the military wants to see the latest in technology incorporated into their toys. 'Enhancements' have the result that the system at the end of the project could be completely different from the concept at the start. Obviously, it has considerable repercussions for the reliability' of the system if there are a number of 'bolton' extras added at different stages of the design and development.

## Fixed Cost?

To overcome some of these problems, the present minister of defence, Michael Heseltine, has introduced what at first seems like a step in the right direction (no pun intended). The fixed - price contract is, in theory, exactly what it says - the contractor will get a fixed amount of money for doing a fixed job. This was introduced mainly to prevent the sort of price escalation that has been so common in defence contracts, but as a side-effect it should have got rid of the continuously varying spec. It hasn't.

The problem is that the eventual users of the equipment are still treating these contracts as cost-plus, and are demanding 'enhancements' from the contractors. Contractors are all too pleased to provide the enhancements requested - and even to make a few suggestions of their own -because, not unexpectedly, it will mean an increased price for the work. The customer can hardly object to this, and in any case, there could be no question of taking away the contract from one company and moving it to another, because that would extend the wait before the equipment comes into service.

Even if the military do not want 'enhancements', the contractor can easily find ways to increase the price because the specification and contractual terms are generally very loose, as is the monitoring of contracts. Just how loosely military contracts are monitored here can be judged in comparison to the way that NASA and ESA monitor their contractors' behaviour.

For example, if you are a sub-contractor to NASA, periodically you will recieve a visit at very short notice from a technical expert. The warning you get could be 24 hours or less. The expert will want to see all the work you are doing, how it is progressing, and will want to know the reasoning behind all the procedures you have adopted. Engineers who have been through this process describe it as 'very testing'. However, it would be unthinkable for the MoD to adopt a similar process here.

## Splitting It Up

Fixed price contracts are not the end of the changes the Government are introducing. The next stage is the putting out of every major stage of the contract to tender. So different companies would have the opportunity to bid at each of the stages; in a typical case,
these are: feasibility study; project definition; development; initial production; and quantity production.

The new system has only just been introduced, so it is not yet possible to see how it will work out in practice. The idea is to make contractors competitive in price at every stage of the process, but the major fear is that it might result in significantly less reliable endproducts.

The problem is that if different contractors do different stages in the process, there is a lack of the engineering continuity which is essential for high reliability through feasibility, definition, development and production. As has already been mentioned, contracts are not normally drawn up by technical staff, although there is technical involvement. The more separate contracts are placed, the more contracts have to be written and the more the problems associated with this come to matter. However, on top of this there are always many things that even competent engineers do not write down - these range from apparently insignificant details to underlying assumptions; indeed, it is more likely to be the latter, rather than the former, that don't get written down.

Even if everything of importance does get written down, the experience and enthusiasm of the engineers involved in the project cannot be transferred from one contractor to another. In particular, if an engineer gets involved in a job which is then taken away, it is unlikely that the next engineer will, at least initially, have the same experience and motivation.

One effect that may not be all that bad is that the switch to part-contracts may lead companies to develop - or buy-in - ranges of off-the-shelf components instead of developing new ones. For example, to produce a generator, the fastest solution is to use off-the-shelf components of engine, dynamo and voltage regulator, whereas at the moment a contractor would automatically design a special-purpose unit from scratch. The reason for this change is that contractors will have to bid for a large number of jobs at any one time - all of them of shorter duration than at present - and it will not be known what the next contract will require. So the flexibility of off-the-shelf units will be necessary.

Finally, an inevitable consequence of part-contracts will be that contractors will spend more on making proposals. Each proposal costs time and money, and the customer will end up paying for this in the long run. At present, it is not uncommon for the cost of making a proposal to be buried in the costs of existing contracts the system is so slack that contractors can allocate engineers' time to virtually anything they like. Whether fixed price contracts will eventually make it more difficult for costs to be hidden remains to be seen, but it is thought unlikely that it will make much difference.

## Design Discipline

A good example of the importance of design discipline has been documented for the cruise missile programme. The sub-contractor doing the software ran into problems, but instead of properly analysing the trouble, the approach adopted was to throw more money at it by bringing in more software engineers. This just compounded the problems. Prof. C. Brooks of the University of N. Carolina's computing department describes the nature of working on software with the following analogy: "The bearing of a child takes nine months, no matter how many women are assigned.

Many software tasks have this characteristic because of the sequential nature of debugging." In other words, you can't rush writing software, but that doesn't stop defence contractors trying.

In general, contractors start their FMECA study far too late in the life of contracts. FMECA stands for Failure Mode, Effects and Criticality Analysis, and it is concerned with looking at the likely shortcomings of the design in a very critical and analytical way. Starting this process any later than the early stages of design and development can greatly reduce its effectiveness. However, contractors will often not start this procedure until they've already realised that there is a problem ie, they're already in trouble and they're clutching at remedial straws. They throw money at the problem as a substitute for proper planning in the early stages.

Ideally, it should be written into any contract that the FMECA programme should start at some short interval - say 30 days - after the development contract has been awarded. This would then have to be very closely monitored to make sure that it really did happen. Very often an inquiry as to the progress on FMECA will result in the contractor hurriedly starting it up - but at too late a stage to have any real impact. The contractor will then pretend to the customer that the FMECA programme had been in hand all the time and they can get away with it because the MOD(PE) does not monitor effectively.

## Short Term Contracts

It should be possible to carry through most military contracts in a much shorter time than they presently occupy. We would suggest that a target of two years not ten - should be aimed for. A number of advantages would be incurred by going for much shorter time scales.

Firstly, the contractor and the customer would have to stick to the original specification. This would have the effect of 'freezing' the technology used at the time of design - but with only a two-year time lapse, this technology would still be in-date and not nearly obsolete, as would be the case with a ten-year contract.

Secondly, there would be a general reduction in price. Besides fixed price actually meaning that, the massive overheads incurred by having a job going on for so long would be reduced, as would the expenses involved in meetings. The main losers would be hoteliers, restaurants, travel agents and air-lines.

Finally, there would be the real opportunity to learn by mistakes. You can actually have an item of equipment out and in use at the time that you are looking at either the Mk. 2 version, or at the next generation of equipment.

As far as we can see, it is sheer inertia that is stopping this sort of development, not technical complexity. If compact disc players can be designed and developed, using entirely new technology, in the space of a couple of years or so, then why not a new command, control, communication system for the army? Yet the Ptarmigan system has been under development by Plessey for the last 12 years and is still not fully deployed.

## Conclusion

The way that the defence industry is organised at the moment, the products work despite the system, and mainly because of the dedication of individuals. A major reorganisation would result in a much less costly more effective industry, which would, in the long term, be better for all concerned.

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# DISTORTION METER 

# Writing in his Audio Design article in the August issue of ETI, John Linsley Hood offered to describe a simple yet sensitive distortion meter, assuming, that is, the editor didn't mind! Needless to say, the editor didn't mind at all. 

The ideal audio power amplifier, along with other pieces of audio signal handling gear which are not intended to modify the frequency response of a system, is well described by the old adage'a straight piece of wire with gain'. This implies that such equipment does not modify or impair the nature of the signal being handled, except to amplify or add muscle power.

However, if this is the specification, how do we check to see how well or badly this requirement is being met? This is, alas, something on which there is very little agreement between audio engineers or circuit designers. So, before we consider the hardware, we need to examine the job we want it to do.

In simple terms, what we want is that the output from an amplifier should be identical to the input, except that it might be bigger or smaller or perhaps with one part of the frequency spectrum enlarged or diminished with regard to another. This is an awkward bit, so let us leave that on one side for the moment and look just at the simple flat-frequency-response area.

When people first considered this problem, their thoughts turned to the examination of a continuous, fixed frequency sine waveform somewhere in the middle of the audible band, say at 1000 Hz . The logic of this was that any distortion of this waveform would lead, as could be shown by
mathematical analysis, to the generation of harmonics of the input signal, and these could be isolated and measured.

The problem with this approach is that it is highly artificial. We simply do not listen for instruction or enjoyment to steady single tones. Nevertheless, the technique is a useful one, especially if the output from the distortion meter can be examined on an oscilloscope. Quite a lot of information about its defects - yes, there are always some, if one looks hard enough - can then be gained, which allows the effects of changes to be assessed.

The most common of this kind of distortion meter is the simple 'notch filter', which will remove the incoming sine-wave signal and leave only the waveform impurities which have been added by the hardware we are testing.

The sort of result we would get

from this kind of test on an amplifier with cross-over distortion, or one driven into clipping, is shown in Fig. 1, $a$ and $b$. What the distortion meter is showing us, in both cases, is what kind of a waveform would have to be added to the distorted output in order to get back to the waveform with which we started. Clearly, there is a difference between these, which can point the experienced worker in the right direction to remedy the defect, especially if the input signal and distortion meter output waveforms can be displayed at the same time on a double-beam oscilloscope.

The most conspicuous audible effect of the presence of large amounts of 'low order' harmonic distortion, (ie. mainly 2 nd and 3 rd ) is that, as its name suggests, harmonic tones are added, which make the system sound rather shrill. Those of us with long


Fig. 1 Examples of the waveforms obtained by using a notch filter on distorted sine-waves.
memories will recall the sound of output pentode valves, which generated generous quantities of 3rd harmonic distortion, and for which the palliative was to stick a 10n capacitor across the primary of the output transformer. Triodes were much preferred, since they mainly generated only 2 nd harmonic distortion, and this was lower down in the frequency spectrum and therefore much less squawky.

Also, as one might guess, these 'low order' harmonics generate spurious waveforms which do, in fact, harmonise with the input signal; once one gets beyond the 3 rd harmonic in the 'odd' series, or beyond the 6th in the 'even' one, the tones become increasingly dissonant and objectionable to the listener.

This was one of the reasons why the first transistor amplifiers (whose residual crossover distortion produced 7 th, 9 th, 11 th, and other audibly dissonant odd harmonics) were so much worse, even at a $0.1 \%$ distortion figure, than the valve units they replaced.

However, back to valves. When, in the early post-war years designers began to consider seriously the requirements for high quality audio systems - at that time largely based on triode valve output stages, operated in pushpull to cancel as much of the even order harmonics as possible attention was drawn to the other defect, shown in Fig. 2. This was associated with non-linearity in the handling of the signal, and was the so-called intermodulation distortion, which led to a muddling of the tonal quality.

- If we take two separate and distinct audio signals as shown in Fig. 2a, and add them together as shown in Fig. 2b, and if we pass them through an amplifying stage having the sort of non-linear inputoutput characteristic shown in Fig. 2c, the result will be similar to that shown in Fig. 2 d , in which the gain of the amplifier is reduced as it swings into its upper voltage region.

The worse the non-linearity, the more the intermodulation effects between initially separate and distinct input signals. Also, as you can see from Figs. 2 e and 2 f , a different kind of non-linearity will produce a different kind of intermodulated output. Once again, the effects due to high order defects such as crossover distortion are worse, audibly, than those due to smooth bends in the trans-


Fig. 2 The introduction of intermodulation distortion as a result of passing two signals through a stage having non-linear characteristics.
fer characteristics of the system which provides yet one more reason why designers try to minimise the generation of the higher order harmonics.

The way in which intermodulation distortion is measured is by passing a pair of signals through the system, and then measuring the sum and difference products caused by the non-linearity of the system. For example, if two sinewave input signals are introduced, one, say, at 70 Hz and one at 3000 Hz , the result of the non-linearity in the amplifier would be to generate additional spurious signals at 2930 Hz and 3070 Hz . If these are filtered out and measured, the amount of distortion in the amplifier can be assessed.

Looking at this in practical terms, if the transfer curve of the amplifier is as shown in Fig. 2c where the gain of the system decreases as it swings more positive, and if we assume that the 3000 Hz signal is a small one riding piggyback on the much larger 70 Hz one, then, as the 70 Hz signal moves the operating point of the system from lower left to upper right, so the 3000 Hz signal will get bigger or smaller as shown in Fig. 2 d .

This is helpful as a yardstick in assessing amplifier quality in that it simulates the effect of typical audio signals which are composed of many different parts, all happening at once, and, in a poor
amplifier, with lots of intermodulation distortion, all getting jumbled up together into a kind of audio porridge.

The snags are two. The first of these is that it takes quite good audio filtering in the test instrument to separate out the 2930 Hz and 3070 Hz signals from the 3000 Hz one, which makes such meters expensive. The second snag is that, having got the answer in terms of the amount of intermodulation distortion, the designer isn't given much assistance in finding just where the problem lies. The simple THD meter, with a display on an oscilloscope, is much better in this respect.

A more recent technique, adopted by the French CCIR committee, employs two high frequency signals, such as $19,950 \mathrm{~Hz}$ and $20,050 \mathrm{~Hz}$. These give a frequency product appearing at 100 Hz , and it is easy to filter this out from the 20 kHz equal-amplitude carriers.

The argument offered in favour of this approach is that amplifiers, even nowadays, are much less good at 20 kHz in terms of their linearity than they are at, say, 1000 Hz . The counter argument is, of course, that we don't have ears like bats, so we are more interested in how the system behaves at 1000 Hz than what it does at 20 kHz .

Another very up-market technique is to put in a high-purity sine-
wave signal, or indeed as many of these as one feels inclined to use, and then display the output of the amplifier as a sweep of the frequency spectrum on a spectrum analyser. This is a development of the earlier 'Frequency Analyser' technique, in which the magnitudes of the outputs at various harmonic frequencies related to the input sinewave frequency could be displayed on a meter for individual analysis.

While spectrum analysis gives a very effective display of the amplifier output - 50 Hz warts and all - and the better modern ones are usable down to a noise threshold of -90 or -100 dB ( $0.003-$ $0.001 \%$ ), in all fairness, it is a bit difficult to see what one has got on the display or print-out if it is much below $-80 \mathrm{~dB}(0.01 \%)$.

All this kind of kit is very nice, and mouth-watering to contemplate if one is setting up a 'cost no object' test laboratory, but it is a bit remote from the more frugally financed DIY enthusiast. So what can one do for oneself?.

## The THD Meter

The most useful piece of gear which one can organise simply, and which will give amplifiers a clean bill of health - or otherwise as the case may be - is a simple Total Harmonic Distortion measuring instrument or THD meter for short.

This operates by 'notching out' the fundamental frequency of the input sinewave and leaving the distortion products, together with any hum and noise there may be in the amplifier output, to be measured on a millivoltmeter. The main snags with this approach are that it will show these hum and noise components as harmonic distortion in the final output to the meter, yet they are nothing to do with the linearity of the system as a whole and are likely to be completely innocuous, audibly, if one can't hear them from the normal sitting position when listening to the system.

Fortunately, it is a simple enough matter to identify which is which, even without access to the oscilloscope, by merely disconnecting the signal source from the amplifier, looking at what remains in numerical terms, and subtracting this from the original result. In order to get a result which is not over-generous to the unit on test, this must be done as an RMS subtraction - I will come to that later.


Fig. $3 \mathbf{a}$ and $\mathbf{b}$ - Two possible arrangements of the Wien network.


Fig. 4 The notch produced using the arrangement of Fig. 3b.

It is not a difficult matter to generate quite a good notch in a frequency response and tune it precisely to coincide with the frequency of one's test waveform, and there are several circuit choices available for doing this. Of these, the two most convenient and therefore the most commonly used are the RC 'parallel T' and the various arrangements of the Wien network, which I have shown in Fig. 3.

The interesting thing about the Wien network, C1, C2, R3 and R4 in Fig. 3a, is that it has zero phase shift and an attenuation of just 3 times at one specific frequency. If one makes R3 and R4 adjustable, this frequency can be altered. If C 1 and C 2 are not quite the same - in theory $\mathrm{C} 1=\mathrm{C} 2$ and $\mathrm{R} 3=\mathrm{R} 4$ the attenuation will not be exactly $3 x$, but this could be compensated
for by an adjustment to R1 or R2. The differential amplifier I have shown as IC1 would need to be a very good one for this kind of circuit to work well, so the alternative arrangement I have shown in Fig. 3b is preferable.

In this, the amplifier IC1 is used simply to invert the phase of the signal and amplify it by $2 x$. This utilises the feature of the Wien network that the impedance of $\mathrm{C} 1, \mathrm{R} 3$ is twice that of $\mathrm{C} 2, \mathrm{R} 4$ at the frequency where the phase shift produced by each part of the network is equal. So, if IC1 applies a signal to the upper half of the network which is exactly twice the size of that applied to the lower and of opposite phase, the output will come to a null at some frequency dependent on the values of $C$ and $R$ chosen, as I have shown in Fig. 4.

## PROJECT : Distortion Meter

If we want just to remove the input signal frequency, without attenuating the harmonics, the skirts of the notch must be steeper than those produced by the simple arrangement shown in Fig. 3. However, we can do this by applying a bit of negative feedback around the loop, as I have shown in schematic form in Fig. 5.

To tune the notch frequency so that it exactly coincides with the input signal frequency, we need to be able to adjust the value of either the Cs or the Rs in the network. Since the operating frequency is given by the equation
$F_{0}=\frac{1}{2 \pi} \sqrt{\text { C1 C2 R3 R4 }}$
the values of $C$ are too large, unless a very high impedance circuit is employed, to allow the use of a twin gang variable capacitor. In fact, if we want the value of $R 3$ and R4 to be $10 \mathrm{k}, \mathrm{C} 1$ and C2 will need to be 16 n for a notch frequency of 1 kHz . Lower frequencies would require proportionally larger values of capacitors.

It is possible to make such a system with an air-spaced twingang capacitor, but the necessarily high values of $R$ make the whole unit very sensitive to 'hum' pickup. Overall, I think it is easier to use variable resistors, which are easier to get and a lot more compact.

The necessary slow-motion adjustment can be obtained by the use of two resistors in series, one ten times the value of the other, when the high value resistors (as ganged pairs adjusted together) can be used as the coarse frequency adjustment, and the lower ones for fine trimming. This principal could be extended, of course, to employ three such twin gangs in series, to allow a very fine adjustment indeed.

Since the resistor which adjusts the gain of IC1 in Fig. 3, (R2), is a single potentiometer, a ten-turn variable resistor can be used in this position to adjust the gain of this limb so that a complete notch is obtained, with no residues of the input frequency remaining.

The final part of the system is a wide bandwidth millivoltmeter, to display the value of the distortion and noise residues remaining when the input sine-wave is removed.

Since we live in the real world, and there will inevitably be some hum pick-up somewhere in the


Fig. 5 Wien network with negative feedback to produce a sharper notch.
system we are testing, it is useful to incorporate a 50 Hz filter which can be switched in. Also, while we are doing that, we may as well include some HF filtering options, so that we don't measure the THD over too wide a frequency 'window', with its associated noise components.

Finally, it is very helpful, in tests where one is taking the measuring instrument to the gear being tested, to have a built-in signal source of adequate quality.

I am going to describe a relatively simple and low cost THD meter which incorporates the general ideas described above, and I propose to show this circuit in two forms, one a laboratory standard quality instrument operated from a mains input supply, and one a somewhat simpler unit operated from a single 9 V battery, which will be rather easier to make if the demands made upon it are less stringent.

I like battery operated instru-
ments myself because they are highly portable and don't cause problems with earth loops. However, if one wants high performance, it is impractical to demand very lower power consumption at the same time. If one then accepts a higher battery drain - say $\mathbf{1 0}^{-}$ 25 mA - it is expensive if one forgets to switch the instrument off after use, while any 'auto off' function may well switch it off right in the middle of a measurement, which is infuriating.

Hence the two versions of the unit. I have deliberately tried to make the battery operated system as economical in current consumption as possible without resorting to exotic ICs, and in both cases I have organised things so that the millivoltmeter is available as a separate input, so that it and the oscillator can be used on their own as a means, for example, of measuring frequency response.

To be completed next month.


The prototype, looking much the way most prototypes do at this stage in their development!


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# DIGITAL DELAY <br> LNE 

## Without further ado, we pass into the constructional stage of the project. Design and development by Ray Lowe.

First of all, before commencing construction, read all the article (including last month's part) thoroughly and don't rush at the construction when you do begin!

To keep costs down, we haven't used through-plated holes on the PCBs (these would add around $50 \%$ to the price of the PCBs); however, this does mean that rather a large
number of through-links have to be made. We would suggest spending an hour or so inserting and soldering all the linking pins, then all those components which have their leads used for throughconnections, afterwards carefully checking that you've got all the connections right.

A tip here is to support the board above the work surface and -
insert lengths of tinned wire through the hole positions before soldering them in a batch. Check very carefully for solder bridges very carefully for solder bridges
between tracks at every opportunity - a fine-tipped iron and fine tunity - a fine-tipped ion and fine
solder are strongly recommended as parts of the boards are a bit crowded! Making your own PCBs is not recommended for this reason, unless you have access to

## OOPS!

We suffered a loss of sync between the component numbering on the circuit diagram and the 'How it Works' text for the digital section, published last month. In the text:
IC24 becomes IC26
IC26 becomes IC25
IC27 becomes IC36
IC29a becomes IC33a
IC29b becomes IC33d
IC29c becomes IC33c
IC29d becomes IC33b
IC30 becomes IC24c
IC30d becomes IC24a
IC32, 33 becomes IC28, 29
IC35 becomes IC32
IC37 becomes IC30
SW11-SW8 should read SW1-SW8
SW9 becomes SW11
SW11 becomes SW9
D7 becomes ZD1
D8 becomes D6
R65 becomes R61
R69 becomes R62
On the circuit diagram, the junctions of R51-54 and R55-58 should be tied to +5 V , not 0 V , the line from the $0_{0}$ output of IC31 should be labelled CK, and this line also has a spurious unlabelled junction with IC32 that shouldn't be there. We are sorry for any confusion this may have caused!


Fig. 8 Circuit diagram of the analogue section.

## HOW IT WORKS - ANALOGUE SECTION

C1, C2 provide non-polarised ACcoupling to emitter follower Q1's base, which is biased by R1, R2. C3 provides HF filtering; Q1 is a low noise device. IC1a is connected as an inverting amplifier. Since the emitter follower has low output impedance, the stage gain is set by RV1 as R5/RV1 approx. DC blocking is provided by C4 so that IC1a's output swings about OV plus offset voltage. C5 limits the HF response: strict bandwidth limiting is desirable to minimise aliasing and overal system noise.

The amplified original signal is passed to RV3 and to the inverting preemphasis stage around IC1b. R6, R7, C6 provide roll-on starting at about 400 Hz whilst R10, C8 start roll-off at around 3.2 $\mathbf{k H z}$, thus mid range lift is produced.
The pre-emphasised signal is (low pass) anti-alias filtered by three MF10 second-order switched capacitor filter stages connected in series, giving $-36 \mathrm{~dB} /$ Octave cut off in total. The corner frequency of the filter is $1 / 50$ th of the square wave clock frequency applied to pins 10,11 . In this way, the Nyquist sampling criteria is always satisfied since the sampling frequency is synchronised to the cut off frequency via the system clock.
Some clock breakthrough occurs in the filters and this is removed by R19 and C9; subsonics are removed by

R20 and C10. The fully filtered signal is buffered by IC4 such that it swings about 0V. IC4 and IC5 are chosen to have a low input offset voltage of about 1 mV for a reason which will become apparent when you read on!
The buffered signal is fed to a 'signal polarity' comparator with hysteresis to elminate noise-induced switching in the absence of a signal. IC9 is the comparator, comprising, a highperformance op-amp with a high slew rate - so high that its output can swing between power rails within a microsecond, and respond very quickly indeed to the polarity of the signal on its inverting input. No frequency compensation is required in this application. R37 and R38 give approx 6.5 mV of hysteresis, which is sufficient if you consider that the polarity assigned to a 0 V signal is irrelevant.
D3 and R39 stop IC10b's data input from going - ve; IC10 is a dual positiveedge triggered D-type flip-flop. IC10b latches the comparator output state on receipt of every SC (start conversion) pulse. $Q$ and $\bar{Q}$ control CMOS switches IC6 $a, b$ such that either the inverted or uninverted signal, respectively, is selected at any sample time, so that the signal reaching IC6c is wholly positive (rectified).
The $Q$ values of IC10b form bit nine of the data word for a sample A/D con-

version. The bit nine 'bus' direction is controlled by the OE control line. ICGC and C11 form a sample-and-hold, updated on every SC pulse, and in conjunction they also perform low-pass filtering.

IC7 is a FET input op-amp with low offset voltage and low offset vs. temperature coefficient (FET inputs generally have higher offsets than bipolar). It also has very high input impedance so as not to load C11; however when switch IC6c is open this means that the non-inverting input/C11 node is at a very high impedance with respect to ground and is therefore susceptible to electromagnetic interference. Including R23 reduces this impedance from something like 100 Mohm to 680 kohm and interference is much reduced. R23 shorts the switch instead of going straight to ground in order that the discharge of C11 is minimised. IC7 acts as a voltage follower with gain of three, and the offset is nulled by adjustment of PR1. This output is A/D converted into data bits ' 1 ' to ' 8 '.
The delayed signal from the $D / A$ is low pass filtered by C18 in conjunction with the D/A's $\mathbf{4 k}$ output impedance, to remove $H F$ breakthrough, and the signal is then buffered by IC11. It is then accurately inverted by IC13, R42, R43. Analogue switches IC12 a,b select either the erect or inverted signal dependant upon the sign of 'bit nine' latched into IC10a by the D/A latch pulse. The sign of 'bit nine' is used in a way such that any signal, irrespective of original polarity, is only inverted once throughout the entire A/D \& D/A conversion process, thus minimising signal degradation.
The signal entering the second-order low pass filter stage of IC4b at pin 16 has been reconstructed to be bipolar about OV with 5V P-P amplitude. IC3b 'rounds off' the step-like waveform. The delayed but still pre-emphasised signal appears together with clock breakthrough at pin 20. Breakthrough is removed by R 26 and C14.

A fraction of the signal is fed back to be delayed again by applying it to the summing point of IC1b. The feedback fraction, which determines the echo decay rate, is governed by RV2. R8, R9 and $C 7$ counter the effect of roll-off on each extra traversal through this stage, however a slight treble cut remains, but this is useful because it tends to mask the quantisation distortion which builds up with each conversion process. R8 also prevents IC1b from going into HF oscillation, as might happen if C 7 were slightly inductive (it would be across the inputs when RV7 is fully off).

The delayed signal is also fed to the output mix control RV3 via deemphasis amplifier/buffer IC8a. Normally, Q2 has a -ve gate potential which holds its channel resistance very high. When -ve bias is removed, by shorting EXT to $O V$, the resistance falls to several hundred ohms which in conjunction with R27, severely attenuates the signal ie, shuts off the echo channel.

The desired blend between original and delayed signals is set by RV3 and the output is buffered by IC8b. Nonpolarised DC blocking for the output is done by C16 and C17. The output can drive low impedance headphones directly.


Fig. 9 Overlay for the analogue PCB.
PARTS LIST


## PROJECT : Delay Line



Fig. 10 Overlay for the digital section.
photo-etching gear.
Construct the PSU section first. What we would suggest doing is mounting the mains switch, the mains fuse and the transformer all in the case to start off with. As you'll be fiddling round with the boards, doing the assembly and setting up, it will probably be best not to mount the boards in the case until you have got the unit going properly, so initially link the transformer secondaries to the analogue board using longish lengths of wire. In any case, whatever you do, you must exercise suitable precautions for the mains side of the circuit. Clamp the mains cable firmly, so that it cannot pull free even with a strong pull. Use a suitable mains fuse, in a substantial panel-mounting fuse holder. Use the mains earth to earth the case and all other metalwork (except the regulator heatsinks, if you haven't used an insulating kit on them). There must be adequate clearances and/or insulation around the mains sections and associated components. On this last point, you will almost certainly find yourself
operating the unit without the lid on at some stage, so use heathshrink wrap, etc, to make sure that you can't accidentally touch live parts.

After the PSU section is constructed, connect it up to the mains and check that it does deliver + and -5 V . Then commence construction of the other sections of the circuits by inserting all the IC sockets (after, of course, disconnecting the unit from the mains!). Then re-connect the mains and check that + or -5 V appears across the correct pins. Insert resistors, capacitors, transistors and switches, checking all the time for secure joints and for solder-bridges. With the mains re-connected, check that the current drain is negligible and that the supply rails are at the correct voltage.

With the supply off, plug in the chips one at a time, starting with the least expensive, then reconnect the supply and check that the current drain is sensible and nothing gets too hot (although, with all the ICs inserted, the positive regulator will run warm).

Unplug the unit between tests, and remember to discharge your fingertips before handling the CMOS you can do this by touching an earthed metal case in your work area.

The last items to insert are the A-to-D, the D-to-A, the switched capacitor filters and the memory chips. To check operation of the unit, only two memory ICs are needed, IC15 and IC23, and as SRAMs are not cheap, it might be prudent to check that the unit is fully functional before you insert any more memory.

The final job before testing is to do all the inter-wiring between the PCBs and any controls, etc, not mounted directly on the PCBs, and to secure the boards firmly in the case.

## Setting Up

If all goes well, the unit should be operational as soon as it is switched on, however there is no harm in looking over one final time to see if there's anything you've missed. Do make certain that all is safe on the mains side - not just
for your own sake, but for the sake of the equipment you'll be connecting the unit to.

Circuit operation is quite easily checked using an oscilloscope see the timing diagram, Fig, 4 (given last month). However, the following is a suggested procedure for those constructors without access to a scope.

Connect the output from the unit to an amplifier and speaker, and apply an input signal. The first check is to see if the peak indicator glows with the gain and bandwidth set to maximum (although, this does depend on your input signal being above 200 mV or so) - if this doesn't work, the first point to check is the LED polarity. Next, check that with the mix control fully anti-clockwise, the original signal is heard; this will show whether or not there is signal continuity through the analogue board. If no signal is heard, go back and check your construction.

With the shortest delay setting, the mix control fully clockwise, repeat control fully anti-clockwise, freeze and percussion switches out, and the LFO depth control off, check that a delayed signal is heard. It may be distorted, but at the moment this is nothing to worry about.

Remove the input signal and adjust PR1 so that the unit's output is now silent for all bandwidth settings; check that distortion is at a minimum on low-level signals.
The unit should now be ready for mounting in the case. Any case should do, more or less, provided it is big enough to take the boards; however, you might wish to have details of the expansion board before choosing the case, and these will be given next month.


The insides of the prototype: a general-purpose PSU PCB was originally used, with a few mods here and there, so please don't look too closely! Also not recommended is duplicating the author's mains cable relief arrangements!

The one critical area is the cutout to take the PCB-mouted components; a suggested panel layout-out is shown in the photograph.

Once completed, and with the full memory complement that you've decided to use, the unit should be ready for use. So don't delay further...


Fig. 11 A suggested modification to make sure that a PSU over-voltage doesn't do too much damage.

BUYLINES

Rather surprisingly with the esoteric devices used in this project, the one semiconductor which might cause a few problems is a humble op-amp the LF411 (IC7), which was eventually traced to Maplin. A substitute type could be used here, but at the risk of increased cross over type distortion (a very low offset device is required). All the other semiconductors are available from Watford, Cricklewood, Technomatic and Rapid to name but a few, as well as Maplin.

The switches SW1-9 must have the correct lead spacing ( $0.15^{\prime \prime}$ between pins, $0.2^{\prime \prime}$ between rows) to fit on the PCB, but this should not create too many problems (for once, RS types are not suitable, as these fit a $0.1^{\prime \prime}$ matrix). The ones in the prototype were from Cirkit.


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