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## SHersounc * *

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Jj90 Stereo Mixer - this is a really versatile new mixer that enables the sional performance every a profes are two stereo inputs for magnetic cartridges, a stereo auxiliary input and mike input. Other 'plus' features are autopanning for fast or slow slider controls. modulation, in short everything


This versatile modular mixer, teatured as a constructional article in Practical Electronics can be built up to a maximum of 24 inputs, 4 outputs and an auxiliary channel. Each input channel has Mic and Line inputs, variable gain, bass and treble controls and a para metric middle frequency equalizer. There are send and return jacks, auxiliary, pan and fader controls and output and group switching. The output channels have PPM displays and record and studio outputs. The auxiliary channel also has a PPM display and there is a headphone monitor jack and a built-intalk-back microphone. The mixer modules plug into base units each of which takes up to 6 channels. To eliminate hum, the power supply is in a separate cabinet

SALES COUNTER Collect your order from the factory. Open 9-12/1-4.30 Mon-Thurs. Easy parking, no waiting

## KIT PRICES

Inout channel Output channel Auxiliary channe Blank Panel
$\begin{array}{rlr}\mathbf{£ 1 9 . 9 0} & \text { Base unit and wooden front } & £ 27.50 \\ £ 18.50 & \text { Pair of mahogany end cheeks } & £ 12.50 \\ £ 22.50 & \text { Power Supply and cabinet } & £ 19.50 \\ £ 3.00 & & \end{array}$

avinan
whole works - AND - under $£ 100$ complete' Complete kit $£ 97.50+$ VAT

## Star features**

TRANSCENDENT 2000 - Although only a 3 octave keyboard the '2000' features the same design ingenuity, careful engineering and quality components of its larger brethren. The kit is well within the scope of the first time builder - buy it, build it - play it! You will know you have made the right choice
Complete kit $£ 165.00$ + VAT

Digital Delay Line - With its ability to give delay times from 1.6 mSecs to up to 1.6 secs. Many powerful effects including phasing, flangine, A.D.T., chorus, echo \&

vibrato are obtained. The basic kit is extended in 400 mS steps up to 1.6 secs. Simply by adding more parts to the PCB.

Compare with units costing over $£ 1,0001$ Complete kit ( 400 mS delay)
$£ 130+$ VAT
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#### Abstract

FEATURES

DIGEST. .. 11 Our usual look at the news in electronics, together with our usual iconoclasm.

AUDIO DESIGN. .21 Here's a series for everyone form newcomer to expert, written by one of the leading writers in the field - John Linsley Hood.

IC UPDATE. 31 This month we're looking at some new ICs that you can buy right now - well, we hope you can, because we've already used one of them in a project.

TECH TIPS. .48 Normally any reader's circuit using a 555 doesn't take long to get sent back to source ( or worse, passed on to Hobby Electronics), but believe it or not, someone has found a new use for a 555 !

AUDIOPHILE .55 This month's audiophile is all about little boxes - ones with Videotone Minimax II written in one corner. Ron Harris sees if these bargain speakers live up to their promise.

\section*{READ/WRITE} .72 Here's where we let you get in on the act - this time we have your views on induction loops and holophony.


## PROJECTS

NICAD CHARGER/REGENERATOR.
Ever had that sinking feeling with rechargeable batteries - as they get older, so their capacities get smaller? Here's a project to fix all that.

UNIVERSAL EPROM PROGRAMMER. .37
The conclusion of this project - the software. But coming soon will be the ETI stand-alone programmer/emulator.

GRAPHIC EQUALISER. .41
Constructional details of our third octave graphic equaliser, the circuit of which we published last month - and details of a rather nice case that you can use for it.

## THE DIGGER

As we've said in rather greater length in the article, this item has little to do with Australia - it's title derives from the fact that it's a DIGital oscilloscope trigGER.

## Z80 CONTROLLER COMPUTER

 .59This month finds us looking at the circuits necessary to interface the controller to the controlled - an I/O board and an interrupt board

## 64K DRAM BOARD.

$\qquad$ .64
If you've got a 6502 or 6800 based micro, and you find you need some more memory - look no further. Even if you haven't but you'd like to find out how to use dynamic RAM, you'll find this article very illuminating.

## INFORMATION

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ETI BOOKS SERVICE.

## READERS SERVICES

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## 01-452 1500 TECHNOMATIC:LTD 01-450 6597

## BGB <br> Micro Computer <br> Please phone for availability



BBC Model A £299 BBC Model B £399 (incl VAT) Carr $£ 8 /$ unit Model A to Model B Fitting charge $\mathbf{£ 1 5}$ Individual upgrades also available

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| CONNECTOR SVSTEMS |  |  |
| :---: | :---: | :---: |
| JUMP LEADS | AMPHEMOL CONNECTORS |  |
| 4 f R Rlbbon Cable with heeders |  |  |
| 4 pin 16 pin 24 pin 40 pin | (centronix type) | 560p |
| 1 end 145p 165p 240p 300p  <br> 2 ends 2100 2300 <br> 3450 $640 p$  | 36 way Solder Socket |  |
|  | centronix type) | 60p |
| Mn Ribbon Cable with sockets | ay IDC Plug |  |
| 20 pln 28 pln 34 pln 40 pln | ntronix type) | 500p |
| 1 end 2 ends | 24 way Solder Plug |  |
| 2 ends 2800 385p 450p 640 p 24in Ribbon Ceble with D. Conn | (IEEE type) | 600p |
| 25 woy Male 500p Female Eeop | 24 way Solder Socket 24 way IDC Plug | 500p |
| R8232 CONNS (25 way D) ' |  |  |
| 24' ${ }^{\prime \prime}$ Single end Male ${ }^{\text {a }}$ (6.50 | EURO |  |
| 24", Single end Female $\mathbf{£ 6 . 0 0}$ | CONNECTORS |  |
| 24' 'Female-Female $\quad \mathbf{1 1 1 . 0 0}$ |  |  |
| $24^{\prime}$ 'Male-Male $\quad \mathbf{£ 1 0 . 0 0}$ | din STD |  |
| 24' Male-Female $\quad \mathbf{£ 1 1 . 5 0}$ | $\left\|\begin{array}{lll} \text { DIN STD } & \text { Plug } & \text { Skt } \\ 4161721 \text { way } & 170 \mathrm{p} & 170 \mathrm{p} \end{array}\right\|$ | 2x16 |
| DIL HEADERS | 4161731 way 100p 100p | $2 \times 23$ |
| older IDC | $16122 \times 32$ way 2800 300p | $2 \times 25$ |
| trpe type | Anded $2 \times 32$ way 3650 | 1 $\times 43$ |
| 14 pin ( 40p 100p | $16123 \times 32$ way 275p 380p | $2 \times 43$ |
| 16 pin 60p 110p | Angled $3 \times 32$ way ${ }^{\text {a }}$ 400p | 2×50 |
| 24 pin 100p 190p | $x 32$ way zidc $a+c$ - 60.5 | 77 |
| 40 pin 200p 205p | (for $2 \times 32$ way specify a + b or a $+c$ ) | 00 |



## RUGBY ATOMIC CLOCK

This Z80 micro controlled clock/calender receives coded time data from NPL Rugby. The clock never needs to be reset. The facilies include 8 independent alarms and for alarm there is a choice of melody or altornatively these can be used for electrical witching. A separate timer allows recording the count. Expansion facilities provided. See July/August ETI for details. Complete Kit $\mathbf{£ 1 2 0}+\mathbf{£ 2 . 0 0} \mathbf{p \& p}$

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20ith

* 24 hour 7 day timer
* 4 independent switch outputs directly interfacing to thyristor/triacs ait 7 seg. displays indicateal imo, ON/OFFand Reset Full details on request. Price for kit $\mathbf{£ 5 7 . 0 0}$


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FD55E 80 track 500kbytes unformatted
2 x FD55E 80 track SSDD 1 Mbyte unformatted
51/4" Mitsubishi M4853 Slim Line Mechanism 80 track DSDD 1 Mbyte unformatted
$2 \times$ M485 2 Mbytes
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Other parts for FORTH COMPUTER available please send SAE for details.
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cased + PSU £350
bare $£ 180$ Cased $£ 205$
Cased + PSU £475
bare £225 Cased £245
bare $£ 225$ Cased $£ 24$
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CRT Controller H/Book E5.55 Programming the $\mathbf{Z : O}$ E11.50 Z80 Microcomp. handbook 63.80 Programming the 6502 6502 Applications $\quad \mathrm{E10.20}$ 6502 Software Design 28.05 $\begin{array}{ll}6502 \text { Software Design } & \mathbf{E 1 0 . 5 2}\end{array}$ Large selection of databooks, inter facing books, books on BBC, etc in
stock. As for our list.

| 74 seriss |  | 74181 <br> 74182 <br> 74164 | $\begin{aligned} & 340 p \\ & 140 p \end{aligned}$ | 74LS 162A <br> 74LS163A <br> 74LS164 | $\begin{aligned} & r_{p} \\ & r_{p} \\ & r_{p} \end{aligned}$ | 74508 74 S 10 74511 | $\begin{aligned} & 80 p \\ & 80 p \\ & 7 s_{p} \end{aligned}$ | $\begin{aligned} & 4063 \\ & 4086 \end{aligned}$ | $\begin{gathered} \text { esp } \\ \text { 40p } \end{gathered}$ | LINEAR ICs |  |  |  |  |  | COMPUTER COMPONENTS |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 7400 | 300 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 27581 818 | ${ }^{811595}$ |  | GENE RATORS |
| 7401 | 30 p | 74185A | 100 p | 74LS185A | 110p | 74520 | s00 | 4068 | 25p |  | (19 |  |  | T0231 |  |  |  |  |  | ${ }^{811596}$ |  | 3-32513 |
| 7402 | 30 P | 74190 | 1309 | 74LS186a | 150p | 74522 | 800 | 4069 | $24 p$ | cma |  |  |  | 200 |  | ${ }^{2} 85000$ | 8279 | 11 |  | (12.1597 |  | Ro3-32513 |
| 7403 | 30 P , | 74191 | 130 p | 74LS166 | 130 p | 74530 | 800 | 4070 | $24 p$ | a MP9100c |  | LMT10 |  | T-10 | 0 | 6502 400p | 8282 | 300 p |  | 88.5120 | 300 | LC 850p |
| 7404 | 30 p | 74192 | $110 p$ | 74LS169 | 10 | 74332 | 100 | 4071 | 249 | A 1100 |  | LMT11 |  | тене\% |  | 6502 A 460p |  |  |  | 9802 | 3000 | kevboato |
| 7405 | 30 P | 74193 | $115 p$ | 74LS170 | '140p | 74537 | ${ }^{60}$ | 4072 | 24 p | AY-1.5080 |  | WTisc | 400 | твле20 | 75 | ${ }_{65 c 02}$ | ${ }^{8287}$ |  |  | ${ }^{98364} 9$ |  | Encoders |
| 7406 | 40p | 74195 | 110 | 74LS 173A | 100p | 74538 | 000 | 4073 | 240 | AY- 13350 | 450 p |  | 400 p |  |  | 6300 2300 |  |  |  |  | 1000 | AY 52376 |
| 7407 | 400 | 74195 | 100 | 74LS174 | Thp | 74540 | 600 | 4075 | 4 | AY-3-8910 AY 3 e912 | ${ }^{450}$ | LMm71 | 0 | T¢9800 | 00 | 0 | ${ }_{\text {ITS }}$ | c14 | 32 | 2020 | \%m | 740922 |
| 7408 7409 | 300 | 74196 74197 | 110p | 74LS181 | 2000 | 74551 74584 | ${ }_{45 p}$ | 4077 | p | ${ }^{\text {cse }}$ | 1100 | LM74 |  | TG820 | 170 | ${ }_{68096}^{609}$ | ${ }_{\text {TMS }}$ TM99092 |  | 0 | ${ }_{\text {z/ }}^{\text {zNa27E }}$ | ${ }^{3000}$ |  |
| 7410 | 300 | 74196 | 2200 | 74LS189 | 1009 | 74574 | 70 | 4078 | 225 | crscear cosme | ${ }^{1109}$ | Lm1011 | 00 | toxiolo |  | 68809 110 | TMS9991 | $\mathrm{cl}^{1 / 4}$ | 0 | zN4289 | ${ }^{1509}$ | mud pate |
| 7411 | 30 p | 74199 | 2200 | 74LS190 | $75_{0}$ | 74585 | 3000 | 4081 | 209 | cascos | mos | LM1014 | 48 | T01024 | $10 p$ | c3809E 112 | ${ }_{2}$ TMS99914 | 814 | 28 | 2N447E | 2100 | generators |
| 7412 7413 | 300 | ${ }^{74221}$ | 1190 1009 | 74LS 191 | ${ }^{750}$ | 74566 745112 | 1009 1809 | 4082 | ${ }^{250}$ | caseo |  | LMM1001 | 4 | T011708 |  | 68000-LB 538 | ${ }_{2}^{23094 P 10}$ | 30 | 3131 309 |  |  | C14411 ${ }^{\text {TSOP0}}$ |
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| 7418 | 30 | 74285 | 3800 | 74LS 194A | TP | 74S114 | 1200 | 4089 | 1200 | craseot |  | L11872 |  | tonzes |  | 60c39 7009 |  |  |  |  |  |  |
| 7417 | 400 | 74273 | 200 | 74LS195A | rp | 74S124 | 300 p | 4093 | 350 | arsocio | 819 |  | 4 | T |  | 8000A 4200\| | 280ecta |  | 32 | 2016 | 4009 | UAPT |
| 7420 | 30 p | 74276 | 1400 | 74LS196 | 00 | 74S132 | 100p | 4094 | \% |  | \% | Lurzi |  | trases |  | cossa 300p | zoma |  | - |  | ${ }_{2500} 40$ |  |
| 7421 | sop | 74278 | 170p | 74LS197 | $\infty 00$ | 745133 | 109 | 4095 | P | ${ }^{\text {cosilice }}$ | 400 | Lresce |  | T¢u2s03 |  | C85A 900 | TMenseo | 10 | OSteess 1100 | 21070 | 5000 |  |
| 22 | 30 | 74279 | 108 | 74LS221 | cop | 7 $74{ }^{\text {7 }} 13138$ | 100 | 4097 | ${ }_{2700}$ |  | 100 | Urase |  | Tou3610 | \% | 8036 E28 |  | 10 m | OSease mop | 21114.3 | 200 p | 000 |
| 7423 7425 | 40 p | 74285 | 3200 | 74LS241 | cop | 74S 139 | 100 | 4098 | ${ }^{2750}$ | CNTHOOE Culiele | 0 | Lucheo | 11009 | TEATO |  | 8088  <br> 8741 17509 <br> 12  | ${ }_{235004} 7139$ | mp | MC1489 | 2114.3 |  | MS602 460p |
| 7428 | 400 | 74290 | 100 | 74LS242 | 100 | 745140 | 100 p | 4099 | 100 | cas | 300 | LMM0914 | 2 m | TLO |  | 8748 | z800 |  |  | 4116-1 | ${ }^{2000}$ |  |
| 7427 | 400 | 74293 | 100 | 74LS243 | cop | 745151 | 1800 | 4501 | 30 | cas | 0 | Ims |  | Tome | 0 | TMS9900 514.50 |  |  | MC3469 | 4416.15 4532.20 |  | modulators |
| 7428 | asp | 74298 | 1200 | 74LS244 | 000 | 74S153 | 1500 | 4502 | ${ }^{58 p}$ |  |  | Lmse |  | TLOEA | 4 | TMS9935 $\quad 12$ |  |  | 33130 40 | ${ }_{48189}$ | 300 p | swite UHF 375 |
| 7430 | 309 | 74351 74385 | ${ }^{2009}$ | 74LLS245 | 1109 | 748157 | ${ }_{2000}^{200}$ | 4503 4504 |  | c7002 | 0 | Ms15131 |  | 1072 | 訨 | 0 | $28000 C^{1}$ | 200p | c34182 |  | 3700 |  |
| 7433 | 30 p | 74368A | 00 p | 74LS248 | 110p | 745183 | 3009 | 4505 | 360 | ci40es | 300 | ms15 | 40 | Trovi | 1100 | 2800 5500 |  |  | \% | 5516 | S530 | 12 MHz |
| 7437 | 300 | 7436A | cop | 74LS249 | 110p | 74S169 | 6509 | 4506 | 000 |  |  | MC13 |  | Toes |  | z80CMOS TSOp |  |  | 1024 mop | 6116 | 350 p | CRYST |
| 7438 | 400 | 74387A | cop | 74LS251 | 78 p | 74S174 | 3009 | 4507/4030 |  |  |  | MC1413 |  | T0e9 |  | (cmos zoi |  |  | 1441 | 6284 | ${ }_{7000}^{400}$ |  |
| 7439 7440 | 400 | 74368 A 74376 | 700 160 | 74LS253 | 750 000 | 745175 745188 | 3200 100 |  | ${ }^{3200}$ | Hat3se <br> cilile | 100 | MC1450 |  | Tloes | 180 |  |  | 5 | MC14412 ${ }^{\text {T00 }}$ | 62811 | 3400 |  |
| 7440 | 400 | 74376 | 1600 1100 | 74LSS2567A | 100 | 7 74.8188 | 1000 | 4510 | 1209 850 |  |  | MC1 |  | TL170 |  |  | EPRO | Ms | 10 |  | ${ }^{260 \mathrm{p}}$ | KHz ${ }_{\text {400p }}$ |
| 7441 7442 A | 6 | 74390 74393 | 112 | 74LS258A | 700 | 74S194 | 3000 | 4511 | 85p | 1cl7eso | 0 | Mc | 00 | Ua759 | 0 | SUPPORT | 16 | mop |  | 7is2 | ${ }_{350 p}^{2250}$ | OMHz 270p |
| 7443A | 100 p | 74490 | 1400 | 74LS259 | 1200 | 74S195 | 3000 | 4512 | 86p |  |  | masa |  | Ynz20 |  |  |  |  | UN20888 | 7152 | ${ }^{2350}$ |  |
| 7444 | 110 |  |  | 74LS260 | ${ }^{78 p}$ | 74S1 | 380 | 4513 | 1500 | -1C72188 |  | MFF100N | 400 | voneoia | 8 | 3242 mem |  | 09 |  | ${ }_{331422}$ | 9509 | $p$ |
| 7445 | 1000 | 74.5 |  | 74LS261 | ${ }^{1200}$ | 74s200 | $\begin{aligned} & 4800 \\ & 32000 \end{aligned}$ | 4514 | $\begin{aligned} & \text { 110p } \\ & 1100 \end{aligned}$ | 1 cm7217 | 700 | mrsoze 0 | 3 | uneoosa |  | ${ }_{3225} \mathrm{mp}$ | 2ses | $\underline{111}$ | UN27 | ${ }_{3025}$ | 8000 | 209 |
| 7464 744 A | 100 100 | 74LS00 | 24 | 74L2273 | 1250 | 74s225 | \$200 | 4516 | ${ }_{86}$ | ICMTSSS | 0 | Mrsos | Tmp | Uuzaon | 75 | ${ }_{6522}^{6520}$ |  | 40 | 10 p |  |  | 2509 |
| 7448 | 1200 | 74LS01 | $24 p$ | 74LS279 | 10 | 74S240 | 4000 | 4517 | 2200 |  | 30 | M L 282 | 0 | uneos |  | ${ }_{6522}^{63}$ | ${ }^{\text {2716-35 }}$ | 3 | 75109 130 |  |  |  |
| 7450 | sep | 74LS02 | 24 p | 74LS280 | 100 | 745241 | 4000 | 4518 | 48 | LC7130 | 30 | meea | 10 | unees |  | ${ }_{6551}^{6032}$ | ${ }_{2732}^{2732}$ |  | ${ }_{\text {75110 }}^{751120}$ |  |  | ${ }_{3} 10.276{ }^{\text {chemz }}$ |
| 7451 | ${ }^{359}$ | 74LS03 | 24 p | 74LS283 | 10 p | 74S244 | ${ }^{600}$ | 4519 | 320 | LC7137 | $\operatorname{mop}_{10}$ | NeS31 | 1100 | Uuraz | 100 | ${ }_{6921}^{6551}$ | ${ }_{\text {2732A }}$ | $\mathrm{mm}_{5}$ | ${ }_{75113}^{712} 1100$ |  |  | ${ }_{\text {coser }}^{3.5795}$ |
| 7453 7454 | 34 | 74LSO4 | 249 240 | 74LS290 | 0000 | 74S251 | 2500 2500 | 4521 | 1209 |  | ${ }^{120}$ | NESM | 100 | UPCCSE85 |  | ${ }_{68821}^{683}$ | ${ }^{27354-25}$ |  | 75114 |  |  | $\begin{array}{ll}4.004 & 140 p \\ 4.194 & 150 p\end{array}$ |
| 7480 | 850 | 74LSO8 | 24 p | 74LS293 | 10 p | 74S258 | 2500 | 4522 | $0 p$ | ${ }^{\text {L } 5353}$ | 0 | NESSS NESSA |  | UPCC 1158 |  |  |  | 250p | ${ }_{75121} 11000$ | ${ }_{24510}^{2021}$ | ${ }^{4000}$ |  |
| 7470 | sop | 74LS09 | 24 p | 74LS295 | Pp | 745280 | 1009 | 4526 | 79 | Lisssen | 1100 | Neses | 109 | XF210 |  | $8{ }^{40}$ | ${ }^{271728.30}$ | c5 | 75122 | 1185030 | 2000 | (1000 |
| 7472 | $\mathrm{ssp}_{\mathrm{p}}$ | 74LS10 | 24 p | 74LS297 | ${ }^{\text {cp }}$ | 74S261 | 3000 | 4527 | 100 | ${ }_{5} 5367$ | 1000 | NES56 | 100 | xR2200 |  | 3050 300 p |  | 5 | 751588 | ${ }^{1851403}$ | ${ }^{2000}$ | (10000 |
| $\begin{aligned} & 7473 \\ & 7474 \end{aligned}$ | 85 | 74LS11 | $24 p$ $24 p$ | 74LS298 | 100p | listis | 2280 | 4529 | ${ }_{100 p}$ | LM10C | 000 | NEE67 | \% |  |  | Ees5 |  |  | ${ }^{75159}$ | 775887 | ${ }^{2250}$ |  |
| 7475 | cop | 74LS 13 | 30 | 74LS321 | 3700 | 745268 | 2000 | 4531 | 75p | M 4307 | 0 | NEE71 | 30 | xpen |  | eses | Cont | ER | 75180 | 745288 75537 | 1800 | 7.00 150p |
| 7476 | $45^{\circ}$ | 74LS 14 | s00 | 74LS323 | 300p | 74S289 | 2280 | 4532 | ${ }^{65}$ | Unsoba | 140 | Neser |  | $\times \mathrm{x}$ |  | 6875 mp | CRT302\% | 518 | 75182 | 22523 | 130 p | (17.168 |
| 7480 | csp | 74LS 15 | 24 p | 74LS324 | ${ }^{3200}$ | 74S299 | ${ }^{580}$ | 4534 | 3200 | LM9310 | 30 | Ne5S32P | 100 | ${ }^{2009}$ | 10 | ${ }_{\text {815s }}^{8150}$ | CRTS |  | ${ }^{75172}$ | 825123 | $150 \cdot$ | ${ }_{8.867}^{1.869}$ |
| 7481 | 100 | 74LS20 | 24 p | 74LS348 | 00 | 745373 | ${ }_{4000}^{400}$ | 45388 | 750 | L 4318 | 1000 | NES639 | 1100 | İN19p |  | ${ }_{8156}^{8156}$ | Erasee | \% | ${ }^{75188}$ |  |  | $\begin{array}{ll}10.50 & 2509 \\ 1070 & 1500\end{array}$ |
| 7483 A 7484 A | 105p | 74LS21 | 249 $24 p$ | 74LS3533 | 1200 | 74S3387 | 205p | 4538 | 75p | LM319 | 100 |  | 100 | zNM23E |  | 8206 8212 | EFsess | ${ }_{20}^{28}$ | 75199 | ${ }_{\text {OTRTRO }}$ |  | $\begin{array}{ll}10.70 \\ 11.00 & \\ \text { l300 } \\ \text { 300 }\end{array}$ |
| 7485 | 110 p | 74LS24 | sop | 74LS356 | 2100 |  |  | 4541 | 800 | ${ }_{\text {Limas }}^{\text {Lima }}$ | 116 | Ploza |  | 2m |  | ${ }_{82218} 1200$ |  | 208 | 73500 |  |  | $\begin{aligned} & 12.00 \\ & 1509 \\ & 1800\end{aligned}$ |
| 7488 | 200 | 74LS26 | 24 p | 74LS383 | 00 |  |  | 4543 | 709 | Lı3362 | 120 | пCa138 |  |  |  | ${ }_{8228}^{822}$ |  |  | 75451 | ${ }^{7564}$ | ${ }_{80} 10$ |  |
| 7489 | 2100 | 74LS27 | 24 p | 74LS364 | 1000 | 4000 |  | ${ }_{4}^{4551}$ | 1000 2400 | L | 100 | RCA151 RCL5s | \% | 2M |  | ${ }_{8}^{82288}$ |  |  | ${ }_{75153}^{15483}$ | 8271 | ¢ 48 | 14.756 |
| $\begin{aligned} & 7490 A \\ & 7491 \end{aligned}$ | $8 s_{0}$ | 74LS28 74LS30 | 249 | 74LS3668 | 80p | 4000 | 200 | 4555 | 2400 |  | 0 | ${ }_{\text {R }}^{\text {Rckses }}$ | 0 |  |  | 8243 |  | c | 70, 70 | 8272. | ع12 | 15.00  <br> 18.00  <br>  2000 <br> $200 p$  |
| 7492A | 700 | 74LS32 | 24 p | 74LS367 | 800 | 4001 | 249 | 4556 | 800 | 588 | 000 | su | 218 |  | 20. |  | TMS99 | 10 | ${ }_{7091}^{75480}$ | FD1711 | 20 | $18.00 \quad 1700$ |
| 7493A | ${ }^{85}$ | 74LS33 | 24 p | 74LS3689 | 800 | 4002 | ${ }_{70}^{289}$ | 4557 | 2409 | LM37 | 30 | Sfrree | 3 |  |  | eassc. |  | 10 | 75992 | FD1791 | 820 | (19.432 $\begin{array}{ll}18.450 \\ 19 & 1509 \\ 1500\end{array}$ |
| 7494 | 1100 | 74LS37 | 24 p | 74LS373 | ${ }^{000}$ | 4006 | 700 | 4580 | 1400 | Ms300 | 100 | lill | 30 | 2musect |  | ezssac-5 |  |  | ${ }_{\text {¢T28 }}^{\text {gT2 }}$ | F1797 | 820 | 22000 |
| 7495A | ${ }^{00}$ | 74LS38 $74 \mathrm{LS40}$ | 249 240 | 74LLS374 | ${ }_{750} 0$ | 4008 | ${ }^{209}$ | 4588 | 2400 | Uscoian | 100 | SNTVA | 0 |  |  |  |  | ACE | ${ }_{\text {gros }}$ | W02793 | 278 | 24.00  <br> 48.000 1509 <br> 1750  |
| 7497 | 210 p | 74LS42 | cop | 74LS377 | 130 p | 4009 | 450 | 4569 | 1700 | 3 |  | SNFO2sell | 700 |  | 23 | ${ }^{8257 C-5}$ |  |  | ${ }_{\text {8797 }}^{\text {gre }}$ | W02797 | ع15 |  |
| 74100 | 1000 | 74LS43 | 1500 | 74LS378 | $\mathrm{csp}_{\mathrm{p}}$ | 4010 | 800 | 4572 | 45 | Lmas | 220 | TA7120 | 1009 | 2U230E | 40 |  | N0661 |  |  | wo2143 | ع12 | 101000 E12 |
| 74107 | cop | 744547 | 000 | 74L5379 | 1300 | 4011 | 24 p | ${ }^{4583}$ | cop | Lmaser | 1000 | TA7130 | 1400 |  |  |  |  |  |  |  | d | in Low |
| 74109 | 7sp | 744548 | 000 | 74LS381 | ${ }_{3250}$ | 4012 | 250 |  | 46 | Wess7 |  | ¢ATz20 |  |  |  | CLOCK |  |  |  |  | fle S | ckets |
| 74110 | top | 74LS49 | 100 p | 74LS385 | ${ }^{3250}$ | $\left\lvert\, \begin{aligned} & 4013 \\ & 4014 \end{aligned}\right.$ |  | $4{ }^{4585}$ |  | LM3 |  |  |  |  |  |  |  |  |  | 8 pin |  | 22 pin 50p |
| 74111 74116 | 889 1700 | 74LS51 | 24 p | 74LS390 | ${ }^{1009}$ | 4 | 700 | 4724 | 1800 7500 | $L_{\text {LIM392 }}$ | 110 | ${ }_{\text {TA732 }}^{\text {TA }}$ | ${ }_{1509}^{1509}$ |  |  | $\begin{aligned} & \text { C6818P } \\ & \text { AM58174AN } \end{aligned}$ |  | SAA50 | 60 | 14 pin | 30p | 24 pin 65p |
| 74118 | 1100 | 74LS55 | $24 p$ | 74LS3939 | 1009 | 4018 | 380 | 14412 14418 | 7509 |  |  |  |  |  |  |  |  |  | 41 | 16 pin | $35 p$ | 28 pin 65p |
| 74119 | 1700 | 74LS73A | 300 | 74LS399 | 1400 | 4017 |  | 14418 | 3009 |  | -LTA | GE | La |  |  | MSM5832RS |  | SAA50 | 11 | 18 pin | 40p | 40 pin 90 p |
| 74120 74121 | 1000 860 | 74LS74A | 359 | 74LS445 | 1200 | 4019 | cop | 14449 | 2600 |  |  | FXED | STIC |  |  |  | 350p | SAA50 | 900p | 20 pin | 45p |  |
| 74122 | 70 p | 74LS76A | 3 sp | 74LS487 | 1200 | 4020 | cop | 14995 | 4800 |  |  |  |  |  |  | LOWPROFILESO | com |  |  | WRAP SO |  |  |
| 74123 | cop | 74LS83A | 70 p | 74LS490 | 1800 | 4021 | ${ }^{000}$ | 145 | ${ }^{6050}$ | ${ }^{\text {SV }}$ |  | 7805 | 459 | 7805 |  | ${ }^{8} \mathrm{plin}$ 3pp | 22 pin |  |  | 50 p | 22 p | pin 75p |
| 74125 | ${ }^{\text {csp }}$ | 74LSE5 $74 L 586$ | 750 | 74LLS540 | 1000 1000 | 4023 | 700 300 | 14595 | 2000 3500 | 18V |  | 7808 7808 | ${ }^{500}$ | 7906 7900 |  | 14 pin 10p | ${ }^{24} \mathrm{ph}$ |  | 249014 pin |  | 2 | ${ }^{75 p}$ |
| 74126 74128 | ssp | 74LS86 74LS90 | 359 | 74LLS5608 | 1000 7000 | 4023 | 300 | 22100 | 3800 7000 | 12 V |  | 7812 7815 | 4 | 7912 7985 | 0 |  | ${ }_{20}^{28}$ pin |  |  | 42 | ${ }^{28} \mathrm{p}$ | 100p |
| 74132 | 75p | 74LS91 | 000 | 74LS610 | ${ }^{10000}$ | 4025 | 249 | 22102 | 700p | 18V |  | 7815 7818 | ${ }_{80} 809$ | ${ }_{7918} 7915$ | 80p |  |  |  | $30 \mathrm{p} \begin{aligned} & \text { 20, } \\ & \end{aligned}$ | 000 |  | 1509 |
| 74136 | 70p | 74LS92 | $\mathrm{scos}^{\text {P }}$ | 74LS612 | 10009 | 4026 | cop | 40014/4584 |  | 24 V |  | 7824 | 80p | 7924 |  |  |  |  |  |  |  |  |
| 74141 74142 | ${ }^{200}$ | 74L9893 | ${ }_{75 p}{ }_{\text {che }}$ | 74LS824 | ${ }_{2250} 280$ | 4028 | 809 | 40108 | $40^{2}$ | ${ }_{88}$ |  | 78L05 | 30 | 7905 | 4 | PT | TO-EL | CTR | ONICS |  |  | DIIVER |
| 143 | 270 | 74LS96 | 1000 | 74LS628 | 2285 | 4029 | 75p | 40095 | 120p | ${ }_{15}^{12 \mathrm{~V}}$ |  | ${ }_{7}^{7812}$ |  |  |  |  |  |  |  |  |  |  |
| 74144 | 270 | 74LS107 | 400 | 74LS629 | ${ }^{1250}$ | 4030 | -350 | 40097 | $00^{\circ}$ | 15 V |  | 8L15 |  |  |  |  |  |  |  | 700 |  |  |
| 74145 | 1100 | 74LS109 | 40 p | 74LS640 | Op | 4031 |  | 40098 |  |  |  |  |  |  |  |  |  |  | 311 | 650p |  |  |
| 74147 74148 | 1700 1400 | 74LS112 | ${ }_{469} 8$ | 74LS640-1 | 3000 | 4033 | 125p | 40101 | 1509 |  | OTHE | R REC | LA |  |  | FNDS |  |  |  |  |  | countens |
| 74150 | 175p | 7415114 | 459 | 74LS641 | 150 p | 4034 | 2500 | 40102 | 130 p | Frodrap |  |  |  |  |  | MAN71/0 | 00p |  | N8910 | 200 |  |  |
| 74151 A | 700 | 744.S122 | 700 | 74LS642-1 |  | 4035 | 70 p | 40103 | 2000 | LM309K |  |  |  |  |  | man3e | ${ }^{1759}$ |  |  | 75p |  | C928 |
| 74153 | ${ }^{200}$ | 74LS123 | cop |  | 3000 | ${ }_{4}^{4036}$ | $70 p$ | 40104 | 1200 1800 | LM323K |  | 3A |  |  | 50p | til32 | 75p 1200 |  |  | 120p |  | 1040 |
| 74154 74155 | ${ }^{1400}$ | ${ }^{74 L S 124 /}$ | 11400 | $\begin{array}{\|l} \text { 74LS643 } \\ \text { 74LS643-1 } \end{array}$ | 280p | 4038 | 1100 100 | 40105 | 1509 | 78H05KC |  | 5A |  |  | 750p | Thioo | 900 |  | 30 | 1000 |  |  |
| 74158 | 100 p | 74LS125 | cop |  | 300 p | 4039 | 2800 | 40107 | ${ }^{\text {scp }}$ |  |  |  |  |  |  | OPTO-ISC | OLAT | Rs |  |  |  |  |
| 74157 | 100 | 74LS 126 | 009 | 74LS644 | 3800 | 4040 | ${ }^{009}$ | 40108 | 3200 | Varishle Re | sto |  |  |  |  | MCT2 | Thlit |  |  | Please | note |  |
| 74159 | 178 s | 74LS132 |  | 74LS645 74LS645-1 | 200p | ${ }_{4041}^{4042}$ | 8sp | 40109 | ${ }^{220}$ | LM305AF |  |  |  |  |  | MCT26 ${ }^{\text {M }}$ | ${ }^{\text {Thlil13 }}$ |  |  | rices ar | subj | ject to |
| 74160 74161 | ${ }^{1100}$ | 74LS133 | ${ }_{\text {csp }} \mathbf{5 0}$ | 74LS645-1 | 4000 | 4042 | ${ }_{009} 00$ | 40110 | 225p 225p | LM317T |  |  |  |  | 40p | MOC3020 11074 | Thl16 |  |  | chan | with | hout |
| 74162 | $110 p$ | 74LS 138 | ssp | 74Ls668 | 109 | 4044 | 200 | 40147 | 2000 | Lм ${ }^{\text {L }}$ ¢ |  | 3A | VAR |  | 25p |  | N139 | 17 |  |  |  |  |
| 74163 | 110 p | 74LS139 | ssp | 74LS669 | 009 | 4045 | 100 p | 40163 | 1000 | LM350T |  |  | VAR |  | 00p | LED | S |  |  |  |  |  |
| 74164 | 1200 | 74LS 145 | $\mathrm{esp}_{\text {ct }}$ | 74LS670 | 170 | 4046 | 100 | 40173/4087 |  | LM396K |  |  | VAR |  | 515 | TIL209 Red |  |  |  |  |  |  |
| 74185 74166 | 110 p | 74LS147 | ${ }_{1750} 17$ | 74LS682 | 2800 3800 | ${ }_{4048}^{4047}$ | ${ }_{560} 80$ | 40174 | 1209 1000 | LM723N |  |  |  |  | 509 | TIL211 Green |  | 12 p |  |  |  |  |
| 74187 | ${ }^{14000}$ | 74LS 151 | ${ }^{1450}$ | 74LS687 | 3800 | 4049 | 30 | 40175 | 1009 | 79HGKC |  |  | VAR |  | 75p | TIL212 Yellow TII 220 Red |  | ${ }^{20}$ | We | also | ock | a large |
| 74170 | 200p | 74LS 152 | 200p | 74LS688 | ${ }^{380}$ | 4050 | 350 | 40192 | 1009 | 78GUIC |  | 1 A | VAR |  | P | TIL 212 Gree |  |  |  | of | Tr | ransistors, |
| 74172 | 4200 | 74LS 153 | ${ }_{150} 6$ | 74LS783 | $E 2$ | 5051 | ${ }^{85}$ | 40244 | 1500 | 79GUIC |  |  | VAR |  | 250p | Til. 226 Yellow |  | 22p | 2 p Diode |  |  | Rectifiers, |
| 74173 74174 | 140 | 74LS 154 | ${ }^{1509}$ | 7488 |  | ${ }_{4053}^{4052}$ | 800 | 40245 | $\begin{aligned} & 1800 \\ & 1600 \end{aligned}$ | Sinlating | gula | ars |  |  |  | (10) Bar Ar | rrays |  |  |  |  | - |
| 74174 74175 | 1108 | 74LS156 | ${ }_{\text {csp }} \mathrm{SSP}_{\text {c }}$ |  |  | 4504 | cop | 40373 | 100 p | SG3524 |  |  |  |  |  | Red (10) <br> Green (10) |  | $\begin{aligned} & 225! \\ & 225 \end{aligned}$ | p Triacs |  |  | rs |
| 74176 | 100 p | 74LS 157 | s00 | 74500 | cop | 4055 | 100 | 40374 | 1000 | TL494 |  |  |  |  |  | RECT | EDS |  | Zener |  | dease | call |
| 74178 | 1500 | 74LS 158 | csp | 74502 | 500 | 4056 | $\mathrm{acs}^{10}$ | 80c95 | ${ }_{75 p}^{78 p}$ | TL497 |  |  |  |  |  | Red, Green, Yellow | W | ${ }^{30}$ | p |  |  |  |
| 74179 74180 | $150 p$ | 744S160A | $\mathrm{rrp}_{19}$ | 74504 | S00 | 4080 |  | 80 C 97 | 78p | 78540 |  |  |  |  | 50p |  |  |  |  |  |  |  |


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## Typewriter Interface

We've come across what must be one of the more crazy situations in electronics - namely that you can't buy a daisy wheel printer for less than around $£ 400$, but you can buy a typewriter with a daisy wheel printing mechanism and a keyboard for just over $£ 200$ ! Needless to say, it didn't take one of our contributors long to get out his soldering iron and find out exactly how you can interface the typewriter in question to a micro - well, not a micro, but just about any micro! And the make of the typewriter, well, we're not foolish enough to tell you that until next month.

## Another New Series

Following on from our attempt to de-mystify audio, we're about to embark upon an even more arcane area, the mention of which will usually bring a look of despair to even the most hardened engineer's face machine code programming. This series will be so simple that even the Editor - a confirmed microphobe - will be able to understand it.

## And While We're Talking About Series ...

John Linsley Hood will be continuing his look at audio design with a discussion of ICs for audio applications and a look at some gremlins - noise and

## IC Update

Almost without us thinking about it, this seems to have sprung into being an established series in the magazine; well, it seems to be one of the most useful roles we can play - that of disseminating information on new devices. To try and counterbalance all these microbased projects (and to keep our Editor happy), we'll be looking at some up-to-date linear devices.

## ZX Backup Supply

This must be. one of the simplest projects we've published in a long while - and such a simple idea that it's surprising no one else has thought of it. What it does is to keep your ZX going if there should be a temporary supply interruption, or a blown fuse - or if grandfather should trip over the power connector!

## ALL THIS AND MORE IN THE OCTOBER ISSUE OF ETI, ON SALE SEPTEMBER 2ND. PLACE YOUR ORDER NOW, OR RISK MISSING OUT! <br> Articles described here are in an advanced state of preparation. However, circumstances may dictate changes to the final contents.



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watte R.M.S. 8 ohm speaker systems recently watt R.M.S. \& ohm speaker systems recently Belgium. Kits comprise Mullard woofer ( $8^{\prime \prime}$ or $5^{\prime \prime}$ ) with foam surround and aluminium voice coil. Mullard $3^{\prime \prime}$ high power domed tweeter. B.K.E. built and tested crossover based on Mullard
circuit, combining low loss components; glass circuit, combining low loss components, glass SUPERB SOUNOS AT LOW COST. Kits supplied in polystyrene packs complete with instructions. $8^{\prime \prime} 40 \mathrm{~W}$ system - recommended cabinet size 240 $\times 216 \times 445 \mathrm{~mm}$
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Designer spproved flat pack cabinet kits, including grill fabric. Can be finished with iron on $8^{\prime \prime}$ system cabinet kit $£ 8.00$ each $+\mathbf{6 2 . 5 0 P \& P}$ $5^{*}$ system cabinet kit $\mathbf{~} 7.00$ each $+\mathbf{\Sigma 2 . 0 0} \mathrm{P} \& P$


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 Output level: 400 mV to both left and right hand channels. Output Impedance: 10 K . Signal to noise
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$\times 11$ in. Clearance required under top panel 2in. Supplied complete with circuit diagram and connecting diagram. Attractive black and silver finish.
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Supplementary parts for 18 V D.C. (transformer, bridge rectifier and smoothing capacitor) ${ }^{\mathrm{E}} \mathbf{5} .50$.
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15" 100 watt R.M.S. (HI-FI, P.A., DISCO, BASS GUITAR) Die cast chassis, $\mathbf{2}^{\prime \prime}$ aluminim voice coil, white cone with
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# DIGEST 

## Worlds Smallest Colour TV

The first-ever LCD pocket colour television in the world has been developed in Japan by the Epson Corporation and Suwa Seikosha Company Ltd, the parent company of Epson (UK) Limited.
Measuring $16 \mathrm{~cm} \times 8 \mathrm{~cm} \times 2.8 \mathrm{~cm}$, the pocket TV utilizes new picture display devices invented by Seiko in its development of a TV watch. This flat display - which provides the key to the ultra-miniaturization represents a breakthrough in picture tube advancement and will play an important role in the progression towards a picture style colour TV, the technological goal of research organisations all over the world. Amongst the pocket TV's advantages Epsom claim no colour aberration at corners, or distortion of pictures, and good visibility in dark or light situations. There are no plans to market the TV in the UK. Epson (UK) Limited, Dorland House, 388 High Road, Wembley, Middlesex.

## Is It Clicket?

A new micro-miniature switch is available through Cambion Electronic Products, and it's called the Clicket. As you can see from the photograph, it's pretty small, with a 0.1" leading space, and it has a push-on, push-off action. Cambion Eletronic Products Division, Cambion Works, Castleton, nr Sheffield S30 2WR.


## Silicon On Insulator Success

Mitsubishi Electric Corporation has succeeded in manufacturing on an experimental basis a silicon-oninsulator (SOI) structure complementary metal oxide semiconductor (CMOS) device with the worlds shortest delay time of 280 picoseconds, using a laser beam recrystallization technique. This delay time is only a quarter of that of a conventional SOI device and even shorter than that of a device using a single-crystal silicon wafer.
Mitsubishi Electrics success in trial manufacture of the new SOI CMOS marks a major step toward the realization of three-dimensional integration - integration greater than the conventional very large scale integration (VLSI). To make a 3-D integrated circuit, it is necessary to cover integrated circuits on every tier of the multiple layers with oxide or nitride film for complete electrical insulation, and to place a single crystal of silicon on top of this film for the next ICs.
Transistors and other devices are integrated on the surface of single crystal silicon in conventional ICs. In the case of the SOI structure IC, singlecrystal silicon is formed on an insulator substrate; such as silicon oxide. When an SOI structure is employed, there is no malfunctioning from short circuits or in-terference, even if the distance between devices is made shorter
for higher integration.
In conventional methods of making an SOI structure, polycrystalline silicon is melted by a laser beam or an electron beam for recrystallization into a single crystal. But the single crystal thus formed is small and the direction of its growth is not fixed, causing electrical leakage and shortening of circuits.

Mitsubishi Electric solved these problems by developing a revolutionary recrystallization method, under which the scanning speed, the intensity and the direction of the laser beam are adjusted to control the direction and size of crystal. Mitsubishi Electric expect their SOI technology to have a wide variety of applications:- as the key technology for 3D integrated circuits of the future; for high speed and highly reliable CMOS LSI's without latch-up; and for thin film transistors for driving liquid crystal displays.
The work was performed under the management of the R \& D Association for Future Electron Devices as part of the R \& D project of Basic Technology for Future Industries, sponsored by the Agency of Industrial Science and Technology, MITI, Japan.

## Lead Free Solder

Jimi Heat of Watford announce the introduction of a new British made allpurpose solder to replace their widely acclaimed, imported, all-metal solder launched around 12 months ago.
Supa Solda is lead free, non corrosive and capable of handing all metals including aluminium. It can be shaped, polished and even chromed. Its relatively low melting point and capillary action is claimed to make it suitable for even the most delicate applications that formerly required expensive silver-based solders.

The suggested retail price of a 'bubble pack' of Supa Solda is $£ 1.65$ and it is available from Halfords and other selected retail outlets.


# NEWS:NEWS:NEWS:NEWS:NEWS:NEWS:NEWS 

## Z800 Details

Zilog have revealed details of their new Z800 family of $8 / 16$ bit microprocessors. The new CPU's will run on all existing $Z 80$ software at object code level and will provide up to five times greater performance operating at clock rates of 10 to 25 MHz . The $Z 800$ also saves board space and reduces system design costs by including DMA functions, counter/ timers, serial $\mathrm{I} / \mathrm{O}$ and refresh logic on the chip. Using these on-chip peripherals a small system can be designed with only the Z800 CPU, external memory and a clock crystal. An on-chip memory management unit (MMU) and cache/local memory are also included to increase the power and flexibility of the Z800.The MMU extends the Z800 CPU's logical addressing space up to 16 megabytes compared to the the Z80s maximum of 64 kilobytes. This is achieved by dividing the logical address space into pages which are mapped into larger physical memory. The MMU also provides all the features necessary to implement a virtual memory system transparent to the applications program.
The 256 byte cache memory on the Z800 chip provides the CPU with high speed access to instructions and data that would otherwise reside in slower external memory. Since this feature coupled with programmable bus timing allows the CPU clock speed to differ from the memory clock speed, fast processors (up to 25 MHz ) need not be accompanied by equally fast memory devices as was necessary with earlier designs. The Z800 CPU instruction set includes all those in the $Z 80$ set plus a number of new enhancements. New instructions allow the Z800 to perform 8 and 16-bit hardware and multiply and divide, 16-bit arithmetic, 16-bit load, system call (for controlled operating system access by the user) and test and set (for multi-processing support).
group of extended processing instructions similar to those used in the $Z 8000$ and $Z 80,000$ allows the Z800 CPUs to be used with any coprocessor compatible with Zilog's extended processing architecture, including the Z8070 floating point processor.
Several new addressing modes have also been added to the Z80 CPU's original set: index with a 16-bit displacement, base index, and stack pointer relative. A program counter relative mode exists for the Z80 chip but in the $Z 800$ chip it is enhanced to allow 16-bit displacement. Furthermore, the Z80 CPU register set has been improved by allowing byte access to both the IX and IY registers (providing four additional 8bit registers) and the use of two stack pointers instead of one.

Four versions of the $Z 800$ will be available, known as the Z8108, Z8116, Z8208, Z8216. The Z8108 and Z8208 are intended for the smaller systems and employ the same 8-bit non-multiplexed bus as the Z80, allowing them to be used with either the existing Z80 peripherals or the $Z 8500$ family. The Z8116 and Z8216 are 16-bit multiplexed Z-Bus devices and can, therefore be used with the same peripheral chips used by Zilog's 16-bit Z8000 CPUs, the Z8002, Z8001, Z8003 and Z8004.
Although all four Z800 CPUs have the peripheral support circuits integrated within the chip, only the $Z 8208$ and Z8216 include the necessary address lines to permit access to the UART and the DMA functions. The versions of the Z800 (Z8216 and Z8208) with all the peripheral features are supplied in 64pin packages and support extra signal such as bus buffer control, multiple interrupts and global bus Req/Ack. The Z8108 and Z8116 which do not allow access to the DMA and UART functions are supplied in 40-pin packages. The 64pin package used for the $Z 800$ has pin spacings of 70 mil , therefore the package is approximately the same size as the standard DIL 48-pin package, currently used by the Z8001 and the Z8010 MMU.
The Z800 CPU is aimed at traditional 8bit applications including personal computers, workstations, I/O processors, network controllers, etc, that now require 16 -bit performance to meet market demands. Zilog (UK) Limited, Zilog House, Moorbridge Road, Maidenhead, Berks, SL6 8PL.

## New, Large EPROMS

Now available in the UK from Bytech Ltd are the latest Intel range of UVErasable Proms. Both D2764 (8K x 8) and D27128 (16K x 8) devices are being stocked, in industry standard approved JEDEC 28 -pin packages. Both devices are available in a choice of 200, 250, 350 and 450ns access times.
The 2764 is a 5 V only, 65,536 -bit UV erasable and electronically programmable EPROM fabricated in HMOS technology. Access time is compatible to high performance microprocessors such as Intel's 8 MHz $8086-2$. In these systems the 2764 allows the microprocessor to operate without the addition of WAIT states devices is that the Output Enable (OE) is separate from the Chip Enable (CE). The (OE) control eliminates bus contention in multiple bus microprocessor systems. The standby mode reduces the power dissipation without increasing access time. The active current is 100 mA , whilst the standby mode is achieved by applying a TTL-high signal to the CE input. Bytech Ltd, Sutton's Industrial Park, London Road, Earlye, Reading RG6 1AZ

## Monolithic Microphone

Honeywell has developed a process for building zinc oxide acoustical microphones and microelectronics on single silicon substrates. The "mike-on-a-chip" offers high performance, sensitivity and reliability at a fraction of the cost and size of current available ceramic acoustic microphones.
The chip-sized microphone is made possible by a new Honeywell technique. The company recently developed a reproduceable process for depositing high-quality zinc oxide thin films, substances similar in electronic response to piezoelectric ceramics but compatible with standard integrated circuit processing. Honeywell used existing semiconductor processes and equipment to fabricate the zinc oxide thin-film sensors and electronic conditioning circuitry on silicon.
The advantages of Honeywell's integrated acoustical microphones over ceramic devices are many. The integrated microphones operate at frequencies down to 0.1 hertz, whereas ceramics lose sensitivity at about 20 hertz. The integrated sensors also offer greater reliability because they are solid state, there are no parts to glue or solder, as with ceramic devices. The Honeywell sensors are also smaller and lighter than their ceramic counterparts. In addition, the sensing element is a passive device and the electronics draw less than 40 milliwatts, which means it can remain working in the field for

## Industry's Fastest RAM

The industry's fastest RAM has been introduced by Motorola. It's the new bipolar 64-bit ECL RAM (MC1OH145) with an address time of 3 ns (typ) and 6ns (max). The MC10H145 is organised as a $16 \times 4$ memory array and is a member of the MECL 10KH family. These very high speeds were achieved through new circuit designs as well as advanced processing techniques. Because the device is a member of the 10KH family, its gate structure was changed from 10 K configuration to include both constant current source gates and a voltage regulator. Thee additions, as well as new configurations of logic, reduce gate delays thus producing these high speeds. Since the device is in the MECL 10 KH family it is processed with Motorola's new oxide isolated process called MOSAIC (Motorola Oxide Self-Aligned Implanted Circuit but it took them quite a while to think that one up:; which achieves smaller device geometries, improved bandwidth and reduced parasitic capacitances. The European Literature Centre, Motorola Semiconductors, 88 Tanners Drive, Blakelands, Milton Keynes.
months before requiring battery recharge or replacement.
Zinc oxide, like piezoelectric ceramic, produces an electrical charge when strained. However, zinc oxide is also pyroelectric, it produces a voltage change in response to thermal change, and this effect must be minimised in lowfrequency applications of this device. Honeywell eliminated the thermallyinduced voltage fluctuations through a unique design of concentric electrodes, that cancel all pyroelectric-induced electrical signals.
The "mike-on-a-chip" is very sensitive. It can detect one microbar of pressure (one bar equals one atmosphere or 14.69 pounds of pressure per square inch) and will exhibit signal-tonoise ratios of 5:1 at one microbar. Honeywell's "mike-on-achip" could have various applications, including hearing aids. Honeywell has applied for a patent on its integrated acoustical microphone technology.
Honeywell Control Systems Ltd, Honeywell House, Charles Square, Bracknell, Berkshire RG12 1FB.

## New Micro With ROM

The NEC uPD7809G contains the largest on-chip ROM capacity of 8 K among current commercially available products, as well as 256 bytes of RAM. In addition to the powerful instruction set with 16bit arithmetic/logic instructions, the device contains versatile functional blocks such as 8-comaparator input lines, watchdog timer, programmable wait, hold function, 16-bit event/timer counter, two 8-bit programmable timers and serial interface (UART). The new unique 8-bit comparator input lines can be used, for example, for direct interface with the keyboard and the watchdog timer will prevent the program from running out of control in a noisy environment.
The 7809 (seem to have seen that number before!) features a high speed instruction cycle time of 1uS, which under 12 MHz , allow much faster 16 -bit multiply/divide operations. It is estimated at 1.5 to 5 times faster than conventional micros.
In addition to on-chip memories of 8 K for ROM and 256 for RAM, external memory expansion up to 56 K bytes is also provided for, with battery back-up operation applicable to some on-chip RAM under stand-by mode.
NEC Electronics (UK) Limited, 116 Stevenson Street, New Stevenson, Motherwell ML1 4LT, Scotland.

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## VELLEMAN KITS

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K1874 Running Light Kit
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K2569 Three Tone Chime
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$\begin{array}{ll}\text { K2544 Complex Sound Generator } & 15.53 \\ & 10.26\end{array}$
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A Prestel microcomputer adaptor to give fullautodialing to your computer. All the usual Prestel facilities are added via this unit, plus many more, and, can operate lo any viewdata computer.

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The unit is not restricted to just the UK, for at least 28 countries use the Prestel viewdata format, so you can also mail-order from anywhere. The Prestel unit is suitable for most micro computers even the ZX-81, so at the push of a button, the technology of tomorrow is in your home today.

## ANTEX

| Soldering Irons |  |  | Iso-tip Cordless Iron <br> SS25 | 25 W |
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| Miniature low voltage |  |  |  |  |$\quad 31-90+$

## COMPONENTS

Device
Price. Z80A PIO 280A PIO 3.20

6800
6810
6821
6502CPU
$2114(200 \mathrm{~ns})$
2708
2716
2732
2532 (200ns)
ADC0816 (8 bit)

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ZX81 E.C.
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$\begin{array}{ll}\text { Spectrum E.C. } & 3.78 \\ \text { VIC } 20 \text { E.C. } & 378\end{array}$ $\begin{array}{ll}\text { VIC 2O E.C. } & 3.78 \\ 50 \text { Way E.C. } & 3.30\end{array}$ $\begin{array}{ll}50 \text { Way E.C. } & 3.30 \\ 18 \text { Way E.C. } & 2.80\end{array}$ $\begin{array}{ll}18 \text { Way E.C. } & 2.80 \\ 64 \text { Way E.C.Plug } & 2.50\end{array}$ 64 Way E.C. Socket 31 Way E. C. Plug 4.80
2.00 31 Way E. C. Socket

## No

K2543 Transistor Ignition
K2555 Digital Freq Counter for Receivers
K2566 3 Channel Coloured Light Organ
K2572 Universal Stereo Pre-Amplifier
K2574 Universal 4 Digit U/D counter with memory
K2574 Universal 4 Digit U/D counter
K2579 Universal Start/Stop Timer
K2583 Heating Controller
K1682 Microprocessor Univ
(no case)
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## NEWS:NEWS:NEWS:NEWS:NEWS:NEWS:NEWS



## Electronic Memo Pad

A unique totally British designed electronic memo pad which can carry out the functions of a calendar, diary, address book, note pad and a expense account log has been
launched into the UK by Domicrest Ltd. The unit measures 136 mm (W) x
$90 \mathrm{~mm}(\mathrm{H}) \times 9 \mathrm{~mm}(\mathrm{D})$ about the same size as a cigarette case, and will therefore fit in the pocket or the handbag. Called the Biztek Pad it will be percolating through. the shops with a retail price of $£ 69.95$,

## New Portables(??)

The portables market is getting just silly, as these two pictures show. Top is the latest offering in this field from Aiwa - it's styled so that all the various 'components' (the tuner, the cassette deck, etc) look like separate units all just glued together. Actually, you can detach the speakers, but when they're attached to the unit, a special port is opened between them and the main case, which brings a passive radiator into play and boosts the bass response. Total output power is 28 Watts per channel (peak), and the thing has a built-in five-band graphic equaliser (readers wanting a proper graphic equaliser should turn to page 41, where they'll find part two of our own, 28-channel equaliser). Price is a cool $£ 199.95$ (It's the CA-70, from Ai-ee-wah UK Ltd, 163 Dukes Road, Western Avenue, London W5 OSY).

The other of these monsters has as you can see, a B \& W TV as well as the usual tape and radio facilities. But won't you bump into people if you walk along holding the TV in front of you? And how strong do your arms

have to be the weight isn't stated in the press release? This beast costs $£ 149.95$ and is made by Heron Electronics, Heron House, 19 Marylebone Road, London NW1 5JL (confusingly, it's called the Ingersoll XK 500).

There must be a whole generation of youth growing up with one arm longer than the. other due to carrying these things around when will manufacturers think of fitting wheels to them?

## New cats for old!

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# NEWS:NEWS:NEWS:NEWS:NEWS:NEWS:NEWS 



## Cheap DMM

Possibly the best value for money handheld DMM in the UK is available from the House of Instruments and hi! distributors.
Metex type 3000 is a $31 / 2$ digit LCD hand held DMM with a basic DC accuracy of $0.5 \%$. It comes fully guaranteed for 12 months complete with test leads, battery, spare fuse, operating manual and free carrying case at $£ 29.50$ including post and packing (but exclusive of VAT).
There are 30 individual ranges of 1000 V , $10 \mathrm{amps}, 20 \mathrm{M}$ ohms, and diode test and zero check functions. Zeroing, overrange, polarity and low battery indication are all catered for automatically. Normal overload protection is provided as well as high voltage surge to approximately 3 KV . House of Instruments, Clifton Chambers, 62 High Street, Saffron Walden, Essex, CB10 1EE.

## New Line for TV

A slow-scan TV system currently undergoing field tests in prototype, will bring slow-scan television within reach of the average amateur pocket Designed and built by Davtrend Limited, it will be introduced in late summer with the launch of the Model SST-1000 SlowScan Receiver, which will be offered at the highly competitive price of less than £200.
The receiver will have facilities for accommodating a transmitter PCB that will upgrade the equipment for two-way communications. This PCB will be introduced at a later date to coincide with the launch of the full transceiver system, designated as the SST-2000 Slow-Scan Transceiver.
System specifications will be standard: that is, 128 by 128 discrete picture elements each encoded into 16 grey shades to produce one picture every 8.5 seconds. Davtrend Limited, Sanderson Centre, Lees Lane, Gosport, Hampshire PO12 3UL.

## Video Recorder Head Testers

Two Video-Head Testers have been added to the Leader range of test equipment marketed by Thandar Electronics designated LHC-909V (VHS) and LHC-909B (Beta) the tester will measure the amount of wear in video heads. The unit costs $£ 45.00$ plus VAT, and for further details contact Thandar Electronics Limited, London Road, St Ives, Huntingdon, Cambs, PE17 4HJ.

## New Cards Make Apples Grow

New from Hawk Electronic Test Equipment is a GP1B interface card which allows the Apple to become an IEEE 488 controller for test measurement and control. The board will run up to 14 separate controllable devices with a transmission path of up to 20 meters. The on-board software interfaces directly with basic and Applesoft strings, making the Apple into a powerful and east to use IEEE 488 GP1B controller. The price of the card is $£ 189.00$ inclusive.
Also form Hawk is a 32-channel I/O card for the Apple, which enables external control and data feedback for the Apple, with four 8-bit bi-directional I/O parts, four 16-bit timers, two serial to parallel, parallel to serial, parallel to serial register and handshake capability. The price of $£ 49.50$ also includes documentation and example program. Hawk Electronic Test Equipment, Bircholt Road, Parkwood Industrial Estate, Maidstone, Kent ME15 9XT.

From Owl Micro-Communications comes a new multi-function communications interface card that turns the Apple microcomputer into a highly versatile communications device, with applications ranging from electronic mail to IBM terminal emulation.
The new Owl Multicom card is available for the Apple II plus, Apple IIe and Apple III computers and provides all the standard communications interfaces - a V24 (RS232) serial interface for synchronous and asynchronous communications, a parallel printer interface and clock/timing functions from a single slot in the Apple Cardframe. Owl Micro-Communications, The Maltings, Station Road, Sawbridgeworth, Herts CM21 9LY.


## IMPECTRON SELL SHARP LC DISPLAYS

## Versatile LCD Display

A $175 \times 50 \mathrm{~mm}$ LCD display panel, featuring a fully programmable $240 \times 64$ dot matrix, has been introduced by Impectron Ltd. The panel, manufactured, by Sharp of Japan, is designated the Model LM-24002G and incorporates LCD display panel, CMOSLSI driver circuits and interconnection facilities.
The new unit is capable of displaying graphs, diagrams or animated pictures
as well as letters, figures or symbols Viewing angle is a minimum of $40^{\circ}$ whilst contrast ratio is typically 3.00 and response speed better than 300 milliseconds. The back of of the display contains ten CMOS control and driver chips, which ensure complete applications flexibility. Impectron Ltd, Foundry lane, Horsham, West Sussex RH13 SPX.

## Fibre Optic Photodiode

Norban Electro-Optics Limited, sole distributors of RCA fibre optic components in the United Kingdom, have launched a new trans-impedance pre-amplfier photo diode module for "second-window" fibre optic applications.
The RCA C30986E utilise the new Indium Gallium Arsenide PIN photo diode which has excellent responsivity between 900 nm and 1700 nm and it is ideal for use at the low attenuation wavelength of 1300 nm increasingly used in fibre optic systems.

The trans-impedance preamplifier employs a low-noise gallium arsenide FET front end and a cascode feedback circuit. An emitter follower stage been added for improved output coupling efficiency. Additional device features include a system bandwidth of typically 250 MHz end and a signal to noise ratio of typically 22 db for a bit error rate of 10-9. Norban Electro-Optics Ltd., Norban House, Boulton Road, Reading, Berks RG2 OLI.

## High Voltage Reed Relay

A new high-voltage reed relay developed by Hamlin Electronics uses a vacuum reed switch with tungsten contacts to give an excellent isolation interface, with hold-off voltages ranging from 5 kV up to 20 kV
DC. The new HE5100 Series is available with a selection of switching voltages from 3.5 kV DC to 17.5 kV DC. Minimum insulation resistance is $101^{\circ} 0$, and maximum initial con-tact resistance is 0.10 ; coil voltages are of $5,12,24$ and 48V DC.Hamlin Electronics Europe Limited, Diss, Norfolk, IP22 3AY.



## Standard

## features -

- High speed 24 K byte extended basic interpreter
- Powerful TMS9995 16 bit microcprocessor
- 48 bit floating point gives 11 digit accuracy
- High resolution ( $256 \times 192$ ) colour graphics
- Screen memory does not use up user memory space
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- Fast line drawing and point plotting basic commands
- High speed colour shape manipulation from basic
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- Real time clock included in basic
- Interval timing with $\mathbf{1 0 m S}$ resolution via TIC function
- Named load and save of basic or machine code programs
- Auto-run available for any program
- Powerful machine code monitor
- Assembler and Disassembler included as standard
- Auto line numbering facility
- Full renumber command
- Simple but powerful line editor
- Buffered i/o allows you to continue executing the program while still printing
- Flexible CALL statement allows linkage to machine code routines with up to 12 parameters
- Basic programs may contain spaces between key words to make programs readable without using more memory
- Over 34 K bytes available for basic programs
- Extended basic includes IF-THEN-ELSE
- Supports up to 16 output devices: Screen and cassette interfaces included as standard
- Supports bit manipulation of variables from basic
- Error trapping to a basic routine included
- Basic supports Hexadecimal numbers
- Separate 16K video RAM for graphics

International as a constructional project) you have access to highly advanced systems and software developed specially by MPE Ltd for the CORTEX. For business, education, R \& D - or simply increasing your knowledge and understanding of computers - it beats comparably priced off-the-shelf machines hands down!

| STATEMENTS IF | PRINT | TIME WAIT | RENUM BOOT | MAG <br> TOF | MWD BASE | @ | () | $\begin{aligned} & \text { INT } \\ & \text { LOG } \end{aligned}$ | $\begin{aligned} & \mathrm{POS} \\ & \mathrm{COL} \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ELSE |  | SAVE | GRAPH | TON | COMMANDS | \# | I) | SQR | MOD |
| ON |  | LOAD | TEXT | DIM | RUN |  | FUNCTIONS | SYS | RND |
| GOTO | 1 UNIT | MOTOR | PLOT | LET | SIZE |  | FNA-FNZ | TIC | KEY |
| GOSUB | BAUD | ESCAPE | UNPLOT | DEF | CONT | ; | ABS | SGN | OPERATORS |
| POP | CALL | NOESC | COLOUR | NEW | MON | \% | ADR | BIT | OR |
| REM | DATA | RANDOM | CHAR | END | DELIMITERS | \$ | ASC | CRB |  |
| FOR | READ | ENTER | SPRITE | BIT | DELIMITERS |  | ATN | CRF | AND |
| NEXT | RESTOR | LIST | SHAPE | CRB | TAB |  | SIN | MEM | AND |
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| market. Mitsubishi Electric (UK) Ltd., |
| Centre Point, 103 New Oxford Street, |
|  | London WC1A 1 EB.

## Shorts

- Mini discs are here! Advanced Memory Services Ltd., Woodside Technology Centre, Green Lane, Appleton, Warrington are now selling 3" Hitachi disc drives for the BBC micro, at $£ 225$ for the single version, and $£ 399$ for the double.
- Jingoistic jig: apparently British standards have been adopted for $98 \%$ of view data and Teletext TV sets throughout the world. But does it make us any money? It must have been done before, it seems such an obvious idea - GenRad Limited, Norreys Drive, Maidenhead, Berkshire have produced a noise dosimeter that can be worn in a shirt pocket.
- Jump on your micro! Crofton Electronics, 35 Grosvenor Road, Twickenham, Middlesex TW1 4AD have introduced a metal case for the BBC, at a price of $£ 39.50$ inclusive. They intend to introduce another version, with integral floppy disk housing.
- Take your floppy for a walk with a new Winchester/floppy disk exerciser from Monitest Ltd, Highdiffe House, 411-413 Lym-ington Road, Highcliffe, Christchurch, Dorset BH23 5EN. It's called the AVA 103D, and is intended as a piece of test equipment.
- A new leaflet, Power Darl-ingtons For Semiconductor Ignition (we think they mean for car engines) is available from Telefunken Electronic GmbH, Postfach 1109, D-7100, Heilbron, W. Germany.
- Now we really are getting into leaflet territory: PSP Electronics, Unit 2, 2 Bilton Road, Perivale, Greenford,


So far as we know, this has got absolutely nothing to do with electronics, but we thought that it might interest you anyway. It's a steam car that Acheson Colloids are sponsoring in an attempt on the land speed record for steam cars (set in 1906 at 129 mph ). In case you are wondering what's happened to our caption photo, none of us here seem to have quite the same warped sense of humour as Peter Green who used to do them!

Middlesex UB6 7DX have issued a leaflet on the range of connectors that they sell.

- Greenpar Connectors, PO Box 15, Harlow, Essex CM20 2ER have issued a leaflet on their coaxial cables.
- Could someone please tell us why around half the leaflets we're told about are for connectors? This one is from Thorn EMI Electrical Components Ltd., Great Cambridge Road, Enfield, Middlesex EN1 1UL, and it details electrical connectors to BS 9522 N0001.
- Cotswold Electronics Ltd., Unit T1 Kingsville Road, Kingsditch Trading Estate, Cheltenham GL51 9NX have issued a leaflet on their budget range of off-the-shelf transformers.
- A new range of Suzuki electronic products is now available in the UK through Craftmaster (UK) Ltd, Tower House, Lea Valley Trading Estate, London N18 3HR. The range includes some rather neat jack connectors and cables, microphones, pianos and a personal stereo amplifier/speaker.
- Sony UK have launched their own mag for CD users, which will be distributed free to owners of Sony players.
- There's something in the air - and it could be coming from the UoSAT satellite. A newsletter on this facility for amateurs is available from UoSAT Group, Dept of Electronic and Electrical Engineering, University of Surrey, Guildford, Surrey GU2 5XH (large SAE required).
- Camel Products have introduced a 4K ROM/RAM unit, along similar lines
as the unit reported in Digest, January ("High-Rise RAM"); however, this makes it only half the capacity of the ETI PseudoROM! Camel Products were too modest to attach their address to their press release, but it is One Milton Road, Cambridge CB4 1YU.
- More jingoism: Gould Micro Power Products Division, 11 Ash Road, Wrexham Industrial Estate, Wrexham LL13 9UF have been awarded a contract from NASA worth more than $\$ 100,000$ to provide zinc-air power packs for the Space Shuttle.
- Prentice-Hall International, 66 Wood End Lane, Hemel Hemptead, Hertfordshire HP2 4RG have released a booklet on the personal computing and micro books that they publish.
- It had to come! Zemco (UK) Ltd, 66 Earlsdon Street, Coventry CV5 6EL, have introduced a handlebar mounted computer for cyclists - so that you can keep a check on your speed, average speed, etc - all for $£ 19.95$ inclusive. Incidentally, your dear Editor saw one of these in use during the recent London to Brighton 'Fun Run', but it didn't seem to help its owner go any faster.
- Jackson Brothers have been busy producing new capacitors, including a nigh voltage air dielectric variable type (the TX5), a new precision trimmer (the MT5) and a differential sensor capacitor that can be used to measure angular displacements. Jackson Brothers (London) Ltd., Kingsway, Waddon, Croydon CR9 4DG.
- New catalogues! Electrovalue, 28 St Judes Road, Englefield Green, Surrey

TW20 0HB will send you theirs for free, but Bi-Pak, The Maltings, 63A High Street, Ware, Herts SG12 9AD will take 75 p plus 25 p p\&p off you for theirs.

- Axiom Electronics tell us that they now hold 'in-depth' stocks of the MC68008, a reduced data bus version of the 68000. Axiom Electronics Limited, Turnpike Road, Cressex Estate, High Wycombe, Bucks HP12 3NR.
- The latest edition of the IBA Technical Review has landed on our doorstep, and it contains a survey of recent developments in Teletext. ETI readers may obtain copies by sending a large SAE to IBA Information Service, Crawley Court, Winchester, Hants SO21 2QA.
- A new company has been formed to exploit the microprocessor and micro computing innovations at Bath University. Called Sirius Microtech Ltd., the company is at Ashchurch Industrial Estate, Tewkesbury, Gloucestershire, and it would surprise us at ETI if this were not one of many such companies to be formed.
- Rifa have introduced a longlife electrolytic capacitor specifically for use in switched mode PSUs, with low ESR and ESL. The PEH 179 series is available through RIFA AB, Market Chambers, Shelton Square, Coventry. - $A B$ Engineering Co have issued a catalogue of their range of tool kits for professional engineers. AB Enginering Co, Timber Lane, Woburn, Milton Keynes MK17 9PL.



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# AUDIO DESIGN 

The object of this series is to de-mystify audio design, and show that even a comparative beginner can design circuits that work, and work well. But don't let the apparent simplicity of the approach fool you - there will be something here for all, including the most experienced of our readers.

In this first part, John Linsley Hood looks at transistors, both bipolar and field effect, and how to do simple yet very useful calculations on them.

There is a great deal of satisfaction to be gained in building something to one's own design, and finding that it works as well as one had hoped, particularly if this is the sort of thing which one can do, on one's own, without the need for a lot of technical facilities or expensive components.

This is an advantage which we share with some of the manual crafts like pottery or carpentry, but with the additional benefit that if we are not pleased with what we have done, we can take it to pieces and re-use the parts. Moreover, the scope of electronics is exceedingly wide, and this adds enormously to the interest which it will give to the experimenter.

However, there is a truism in engineering that a good design will not necessarily cost more than a poor one, in materials and labour, indeed it may sometimes cost even less, but will give much more satisfaction in use, and may have a longer trouble-free service life. Therefore, it pays in electronics, as in other forms of engineering, to know ones materials and their strengths and weaknesses. In this part, I propose to have a look at the active components (bipolar transistors and FETs) which we are likely to wish to use, and to discuss the characteristics of the passive components (resistors; capacitors and inductors) only as and when we come across them in the circuit design, and when we need to be particularly concerned with their qualities in order to obtain the best results.

## Transistors Or ICs?

Most of the things which we need to do in audio circuit design can now be done just as well by the use of integrated circuits as they can be done by any assembly of transistors and separate components. Moreover, it is nearly always a lot cheaper to use an IC, if. a suitable one is available, and it will also occupy a lot less space.

Unfortunately (I say this sincerely, since I am as lazy as the next person, and I like my design work to be done for me ) there are still a few fields in which discrete component circuitry will perform rather better than the equivalent ICs, or in which suitable ICs are just not available. These are high voltage systems, with supply voltages in excess of some 45 volts, high power systems, very low noise circuitry (though ICs are beginning to make inroads here), and very high fidelity systems, particularly where these also involve low signal levels.

There are, indeed, some very good ICs of recent origin which are aimed specifically at the hi-fi field, and one would be foolish to ignore their existence, so I will talk
about some of these later. However, discrete component (resistor/transistor) circuitry is still the mainstay of audio electronics, so I will start with this.

## Bipolar Junction Transistors

These, the 'transistors' of common use, are now almost exclusively silicon planar devices, made from a slice of mono-crystalline, very high purity silicon, 500 to 750 microns thick, and 75 to 100 millimetres in diameter. During manufacture this slice is photographically masked in an intricate and repetitive series of patterns across its face, and controlled quantities of specific impurities are selectively diffused in a vacuum oven through the succeeding mask patterns, into the slice. This gives a construction of the type shown in cross section in Fig. 1, when the large slice is cut down into a thousand or more individual segments or 'dies'.


Fig. 1 (a) Cross section of a die; (b) a complete small-signal transistor.


NPN


PNP

Fig. 2 Transistor circuit symbols - these should be all too familiar to you!
When connections are attached to the impurity regions and the whole lot is encapsulated in a pea-sized piece of plastic, or, more expensively, mounted in a small hermetically-sealed metal container, this becomes the 'transistor' which is shown in the conventional circuit drawing of Fig. 2.
The enormous commercial success of the silicon transistor
transistor, which has now almost completely superseded the earlier germanium type, stems from the fact that this method of construction makes them very cheap to produce. I don't think that I am letting too many secrets out of the bag if I say that a large scale commercial user would probably be reluctant to pay more than 1 to $2 p$ each for these devices in any large quantity, and even at this price it is possible for the manufacturer to make a living.
Discrete junction transistors of this silicon planar type are, conveniently, available in NPN (positive supply line)and PNP (negative supply line) types, and they can be used for an enormous range of applications. However, the one which comes most readily to mind is that of a voltage amplifying stage of the type shown in. fig. 3(a) or (b). Of these, the circuit shown in 3(b) is much more predictable in its characteristics, and would therefore be preferred by the experienced circuit designer if a single transistor amplifying stage would be adequate for his purposes.

(a)

(b)

Fig. 3 (a) and (b) single transistor amplifier stages. Both these employ feedback in the setting of the operating point, but not in the signal path (assuming that the source output impedance is much lower than the value of R1 in (a).

That last comment is, however, an important one, in that the performance which can be gained from the use of a group of transistors, acting in combination, is so much. better than that of a single device that there is seldom any good reason for not using a more complex construction.
A typical two transistor amplifying stage, using complementary (NPN and PNP) devices is shown in Fig. 4.This employs some negative feedback (much more on this topic later on) to improve its linearity and bandwidth, and control its AC stage gain. With the circuit values shown, this has a gain of 100 , a bandwidth of $10-500 \mathrm{kHz}$, an output voltage swing of 28 V p-p, and, a distortion of less than $0.01 \%$, as compared with a gain of about 40 , a bandwidth of only about halt this, and a distortion of some $5 \%$ for the single transistor circuit.


Fig. 4 A two stage transistor amplifier with a gain of 100.
This type of circuit can be elaborated still further as shown in Fig. 5, which will amplify DC as well. However, I am running ahead a little too fast. If we are to make use of circuits of this type, we must first be able to decide upon


Fig. 5 DC amplifier (with a gain of 10) using an input iong-tailed pair, Q1 and Q2.
our component values and types, with the intended use in mind. So let us do this for the circuit of Fig. 3(b), and while we are at it examine why 3(b) is a better circuit than 3(a). All we need at this stage is a knowledge of Ohms Law, a little familiarity with transistor characteristics, and a pocket calculator!

A typical small-signal plastic encapsulated transistor will have a maximum permitted dissipation of around 300 milliwatts, a current gain of 100 to 500 , which will depend a little on collector current and a maximum operating voltage in the range $20-80$ volts, with 30 volts being a typical value. In addition, to make the transistor work, there will need to be a forward bias voltage between the base and emitter of some 0.55 volts at room temperature ( 0.2 volts for a germanium device).

So, let us choose a 30 volt supply line for Fig 3(b), and decide to have about 15 volts across the transistor itself. A collector current of 5 mA will give a dissipation of 75
milliwatts $\left(P_{\text {watts }}=\mathrm{VI}\right.$ or $\left.=I^{2} R\right)$, which is comfortably within its permitted range. This sort of collector current will also give a reasonable small signal performance. If we choose an emitter potential of 3 V , the required base voltage will be 3.55 volts, and the collector voltage will be 18 V , giving a voltage drop of 12 V across $\mathrm{R}_{3}$.

From the ohms law relationships $V=I R$, which can be rearranged as $R=V / I$ or $I=V / R$, where $V$ is in volts, $I$ is in amps, and $R$ is in ohms, we can work out that R3 should be $12 / 0.005$ or 2 k 4 ohms. For 3 volts dropped across R4, this resistance, which carries virtually the same current, will need to be $1 / 4$ of this, or 600 ohms. If we assume a minimum current gain for the transistor of 100, then the base current will be 50 uA . To make sure that this doesn't influence the voltage drop in the potential divider chain R1/R2 too much, let us make the current through this 0.5 mA , which gives values for these resistors, calculated as above, of $53 \mathrm{k} / 7 \mathrm{k} 1$, to provide a base voltage of 3.55 V .

Rounding these values off to the nearest 'preferred' values will give $R 1=56 k, R 2=6 k 8, R 3=2 k 7$ and $R 4=$ 680 ohms. This will not affect the desired operating potentials too much. At this sort of collector current, the input impedance of the transistor itself will be about $5 k$, giving an input impedance to the whole amplifier circuit of some $2 k 7$. $\left(R_{\text {in }}=1 /\left(1 / R 1+1 / R 2+1 / R_{\text {lx }}\right)\right)$. A calculator with a reciprocal $(1 / x)$ function make this kind of calculation very easy.

This leaves us only with the task of deciding what values to use for C1, C2 and C3, which will be determined by the lowest frequency we want to amplify. The impedance of a capacitor is given by the formula $Z_{c}=1 /(2 \pi f C)$, where $f$ is the frequency, in Hz , and C is the value of the capacitor, in Farads. C1 and C3 should both have impedances which are a bit smaller at this frequency than the input impedance ( $2 k 7$ ) and the output load impedance $\left(Z_{l}\right)$ presented to the circuit - say $10 \mathrm{k} . \mathrm{Z}_{\mathrm{C} 2}$ should be less
than R3/M, where $M$ is the hoped-for value of stage gain say $\times 100$. Doing these calculations gives $\mathrm{C} 1=6 \mathrm{u}, \mathrm{C} 2=$ 600 u and $\mathrm{C} 3=1.5 \mathrm{u}$, for a lowest operating frequency of 10 Hz .

The upper operating frequency will be determined mainly by the output stray capacitances of the circuit and its associated wiring, but could be a few hundred pF. The -3 dB point (at which the output is down to $70 \%$ of its original value) is that frequency at which $\mathrm{Z}_{\mathrm{C}_{\mathrm{s}}}$ is equal to R3 in parallel with ZL. The userful formula here is $f_{1}=1 / 2 \pi R 3 C S$. If $C S=300 \mathrm{p}$, ft will be 250 kHz .

Using the calculated resistor values shown above, we could swap transistors in the circuit of Fig. 3(b) with very little change in the DC operating conditions. How about Fig. 3(a)? In this case, the base current is determined by the collector-base voltage and the value of R1. If, as before, we make $\mathrm{V}_{\text {ce }}=15 \mathrm{~V}$, and decide on a collector current of 5 mA , then R2 will be 3 k . If we assume a current gain of 100 , then R1 $=14.45 / 0.00005=289 k$. However, suppose that the transistor current gain turned out to be 500, instead of 100, then the collector current would increase and the collector voltage would fall to about 5.5 V to preserve the status quo. The circuit would still work, but one wouldn't be able to get nearly as much output voltage swing before it began to clip. So, although simpler, and a bit cheaper in components, the circuit of Fig. 3(a) would be much more influenced by transistor characteristics than that of 3(b).

Going through the same sort of calcułations as above gives the component values shown for the two transistor circuits Figs. 4 and 5. A further advantage of the two transistor circuits not mentioned earlier is that the use of the internal negative feedback loop substantially increases the input impedance of the circuit, above the rather inconveniently low values given by the circuits of Fig. 3, which is typically a few kilohms.

The other frequently used transistcr circuit configurations are the common collector (collector at zero AC potential) also referred to as emitter follower, and the common base, which is used mainly in RF circuits or low impedance, very low noise circuit configurations.

These are shown in Figs. 6 and 7. Once again the emitter follower unity gain circuit can be improved by the use of more than one transistor, giving in a two-transistor form the very valuable compound emitter follower arrangement of Fig. 8. This has a very high input impedance, determined mainly by the input resistor network, and a very low output impedance, so that it can drive low impedance loads with very little loss of signal. Moreover, as a circuit, it has a verv low distortion indeed, and, with suitable transistors and operating values, also very low circuit noise, making it usable in a whole variety of low signal level arrangements. All in all, the two transistor compound emitter follower is one of the most useful of the unity-gain circuit building blocks, which can be made,
with complementary transistor types, to work from either a positive or a negative supply rail.

A word of warning is necessary at this point. All feedback circuits (and this includes those in Figs. 4,5,6 and 8) can oscillate if enough phase shift occurs within the input/output feedback loop. The emitter followers of Figs. 6 and 8 are very prone to this with suitable (though often unintended) combinations of lead inductance and stray circuit capacitance on input or output. To prevent this, it is useful to put a small value of resistance - a few hundred ohms will often suffice, or a bit more if the circuit conditions will tolerate this - in the input and output leads. This will not normally have any adverse effect on performance.

Combinations of transistors can be used to make oscillators and other waveform generators, but the numbers of circuits used for this are legion, and there is inadequate space to disucss these here, though they do have a part to play in audio testing.

## Field Effect Transistors

These come in two basic types, junction FETs - usually referred to as just FETs - and insulated gate FETs, normally known as MOSFETS, because of their construction (metal-oxide-silicon). Both types are made by much the same general manufacturing processes as bipolar transistors. However, they tend to be quite a bit more expensive, partly because they do use rather a larger area of the slice, but mainly because they are not made as discrete transistors in such large quanitities (though very large numbers are made in CMOS and NMOS ICs) and therefore don't benefit from the same economies of scale.

Both of these devices have a much higher input impedance than bipolar devices - usually measured in millions of megohms - but do not give as high a stage gain as junction transistors when used in equivalent circuits. Junction FETs are not much bothered by static electrical charges, though some care is needed in handling MOSFETs.However, having said that, the only instance I have ever come across of them failing in handling was when a colleage of mine soldered them into an earthed circuit with a soldering iron whose case was not earthed and floated somewhere around 120 VAC!

The junction FET, whose circuit drawing is shown in Fig. 9(a), is now almost exclusively used in small signal circuitry - though Sony did produce some high power ones, a few years ago - with maximum working voltages in the range up to 50 VDC, and dissipations of a few hundred milliwatts. It is, however, a very linear device with a very high dynamic impedance. MOSFETs are very fast devices, capable of operating up to the 500 MHz range, and, until comparatively recently, have been used almost exclusively as RF amplifiers. In the past few years, though, high power MOSFETs have come into service in audio output

Fig. 8 Compound emitter follower, with gain very close to unity and 300k input impedance.

Fig. 6 A basic emitter follower.


Fig. 7 Common base circuit, shown. as an RF amplifier.




Fig. 9 FET circuit symbols: (a) junction FETS and (b) N-channel MOSFETs (P-channel would have the small arrow on the source pointing in the opposite direction).
stages, where their fast response and good linearity has conferred useful advantages. On the debit side, they do need more careful treatment in circuit design (mainly because their very high speed makes wiring inductances and circuit capacitances important where they are not even noticed in normal power transistor output stages) if troubles are to be avoided, which is why there are still relatively few power MOSFET audio amps in general use.


Fig. 10 Single stage FET amplifier.
The design of FET amplifier stages follows similar general principles to those indicated earlier in respect of bipolar circuit designs, but with a few significant differences, which we can consider in relation to the single. FET amplifier circuit of Fig. 10, and the rather better two stage circuit shown in Fig. 11. To begin with, the normal junction FET is what is referred to as a 'depletion mode device, which is to say that it normally passes current, which is reduced by the application of a bias voltage \{negative in respect to an N channel device, and positive in respect of a P -channel one) to the gate electrode. This means that an input biasing network of the kind shown in Fig. 3 is unnecessary, and the correct operating conditions can be established by a resistor in the source lead, in an identical manner to that of cathode bias in the case of a thermionic valve.
The second practical difference is that, unfortunately, the characteristics of FETs are nowhere near as precisely


Fig. 11 (Left) Two stage FET amplifier with overall negative feedback gain will be 100 and input impedance will be 10 Megohms. Fig. 12 (right) Use of a junction FET as an adjustable constant current source.
controlled as in the case of the normal bipolar junction transistor, which will always begin to turn on at a forward bias between 0.5 and 0.6 V on its base. By contrast, the specification quoted by Motorola for their 2N5457 Nchannel small signal junction FET, which is quite a popular and representative type of device, merely claims a current, at zero bias, somewhere in the range 1 to 5 mA , a slope ( gm ) which lies between 1 and $5 \mathrm{~mA} / \mathrm{volt}$, and a cut-off negative gate voltage between -0.5 and -6 volts. Happi-ly these are extreme limit values quoted so that the users won't throw too many of their FETs back at them as being 'outside spec'. Nevertheless, although a typical 2N5457 might have a cut-off voltage of -2 to -3 V and a zero bias drain current of 2 mA .

In the case of the circuit shown in Fig. 10, the very low input leakage current means that we could make $R, 10 \mathrm{M}$, which lets us use a relatively small and cheap input capacitor, while still having a good LF response. For a drain current of 1 mA , a source bias resistor of 1 K will give an effective negative gate bias voltage of 1 V , and a 10 K drain resistor will give (at 20 V positive supply and 1 mA drain current) a drain voltage of +10 V . Unfortunately, this doesn't give a very good stage gain. The simple formula for stage gain, where one knows the device gm, is Gain $=g_{m} R_{L}$. is still 10 K , then the gain is 10 for a slope of $1 \mathrm{~mA} /$ volt.

To retain the FET advantage of a very high input impedance, while still having a useful stage gain, coupled with the ability to use the stage with normal load impedances, we need to use a two stage circuit such as that shown in Fig. 11. In this, by using a very high current gain (C grade) transistor for Q2, and remembering that the input impedance of a transistor amplifier stage depends at LF on its base current, which becomes less as the current gain B increases, we can operate the FET at a low drain current, and a fairly high resistor for R2. By making R2 and R4 of the same value, the voltage drop across both, due to the drain current $\left\{0.55 \_/ 27 \mathrm{k}\right.$ -20 uA ) will be 0.55 V , and the output DC voltage, at Q2 collector will be about +11 V , with the FET having, say, -1.5 V effective gate bias. As in the circuit shown in Fig. 4, the gain is controlled by negative feedback to a value of 100; and the circuit will have a good output swing, very low distortion, and a wide bandwidth. This circuit is also quite tolerate of FET characteristics, in that variations in cut-off voltage will only make smallish changes in the DC output level.

To summarise, apart from their very much higher input impedance, and their low intrinsic distortion characteristics, FETs tend to offer rather better noise levels in high impedance circuitry than bipolar devices, but for very low impedance circuits, as would be used, for example, in a moving coil head amp, even the best of the FETs are less good than suitably chosen bipolar types. At low impedances MOSFETs tend to be rather noisy. One very useful facility of the junction FET is its capability of being used as a 'two terminal' constant current source, as shown in Fig. 10. The ability of the source current flowing through the adjustable source resistor to bias the device to a drain current level which is almost completely independent of drain voltage, within its possi-ble working limits, makes an almost ideal arrangement for giving a constant, though adjustable, current source which is usable right up to the maximum gate-source voltage of the FET. This could be used to provide an almost perfect 'fail' for the long-tailed pair circuit (Q1 and Q2 in Fig. 5).

In the next part of this series, I propose to have a look, at ICs, and some of the circuit configurations which can be used with these in the audio field, before going on to look in rather greater detail at some of the problems such as noise and distortion and other unwanted effects.

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# NICAD CHARGER/ REGENERATOR 

## Many a Ni-Cad charger has graced these pages in the past; the NiCaddy is a bit different, in that it will regenerate the battery automatically for you. Design and development by Mike Punnett.

Nickel-cadmium cells are becoming increasingly popular as replacements for conventional dry batteries in a wide range of equipment. Properly used, they can give an enormous cost saving over the life of the equipment, but if misused, tend to fail early.

Since Ni-cads have a tendency to self-discharge over a few months, they have to be charged regularly. Furthermore, to avoid the inconvenience of a flat battery, they are often "topped up" with charge even when far from discharged. This leads to an effect known as whiskering, where fine deposits of cadmium build up, which can partially short-circuit the cell, as well as reducing the active electrode size. This leads to a loss of capacity; a 500 mAh cell may be reduced to 300 mAh after a year of light service and frequent charges.

It has been found that "cycling" Ni-cads can return them to an almost-new condition. This process involves discharging the battery hard (at the 1 hour rate, e.g. 500 mA for a 500 mAh battery), until it reaches the minimum safe voltage - Ni-cads can be easily damaged by over-discharging. A full charge at the 10 hour rate follows. This rather rough treatment disintegrates the whiskers of cadmium, and the full charge redeposits the metal on the electrodes. However, cycling Ni-cads "by hand" is a risky business, since they can easily be damaged.

The ETI Ni-Caddy was designed to cycle Ni-cads correctly and easily. It uses a minimum of components, and has two "programs": cycle and charge.

Operating the unit is very straightforward: the Ni -Cad is connected to it, and the appropriate button for the required program

Fig. 1 Circuit diagram.


The power supply section is quite straightforward, using a very simple voltage regulator. $\mathrm{V}_{\mathrm{CC}}$ is not critical, but the reference voltage, Vref, must be stable, even though the precise voltage is not important. With a separate regulating transistor (Q1) the circuit shown is quite adequate. The two reference levels (the points at which discharge and charge respectively terminate) are derived by RV1 and RV2.

IC1 is a dual comparator which has a number of advantages over similar units, including single-rail operation, the ability to accept inputs at nearground potential, very low offset, and open-collector outputs. In the circuit, the output of IC1a goes low to indicate that the battery has reached minimum voltage, and that of IC1 b goes low when maximum voltage is reached.

IC2 is wired as two flip-flops, one for discharging (IC2a,b) and one for charging (IC2c,d). Pressing "Cycle" sets the discharge flip-flop and clears the charge flip-flop (via 02). When the battery reaches minimum voltage, or "Charge" is pressed, the discharge flip-flop is cleared and the charge flip-flop is set. The battery reaching full charge clears the charge flip-flop but does not set the discharge flip-flop. The status LEDs are driven directly by the two flip-flops, which also drive the output stage. The latter consists of a discharge circuit when Q4 is turned on, the battery discharges through R11 - and a constant current circuit consisting of QJ and its ancillary components, which is turned on by an active-low signal (when IC2 pin 11 is high, QJ is driven fully off and passes no current).
pressed. Cycle mode discharges the battery to its minimum safe voltage, and then switches to charge mode, in which the unit functions as a constantcurrent charger, automatically turning off when the battery reaches full charge. If the $\mathrm{Ni}-\mathrm{Cad}$ is already below its minimum safe voltage when connected up, the unit will automatically enter charge mode, overriding the switches, which are reenabled when the battery rises above minimum safe voltage.

## Construction

Construction of the unit is quite straightforward, either on the PCB or Veroboard. Sockets are recommended for the ICs, particularly IC2 which is a CMOS device. Do not forget the three wire links on the PCB.

Table 1 gives component values for AA size $(500 \mathrm{mAh})$ cells (see later for details of use with other battery sizes). The circuit will work with batteries of up to eight cells. Remember that R11 will get hot, since the battery is discharged through this. For power ratings over 4 W , this component should be mounted off the board, preferably outside the box, to aid heat dissipation. Some of the transistors are fitted with heat sinks; Q1 has an aluminium heatsink (see overlay), Q3 and Q4 have pusj fit TO5 heat sinks.

## Testing and Calibration

Check the voltages across C3 and C4. Both should be in the range 1.6.5 17.4 V . If not, the power supply section should be investigated. The precise values do not matter, since the calibration will allow for some variability.

If the power supply is working properly, the unit can be calibrated. RV1 is set to the minimum safe voltage for the battery; this is 1.1 V per cell (4.4V for a four cell battery).

An accurate, high resistance voltmeter connected to pin 8 of IC1 will enable the voltage to be checked. RV2 (full charge voltage) must be set rather more accurately, since the step in voltage which a Ni-Cad exhibits as it reaches full charge is quite small. The best method is to set the voltage too high at first; about 1.7 V per cell on IC1 pin 11 is adequate. The operation of the unit is then checked with a

| No of <br> cells | D3 <br> voltage | R9 <br> ohms/watts | R10 <br> ohms/watt |
| :---: | :---: | :---: | :---: |
| 2 | 10 | $210 / 1$ | $4.7 / 2$ |
| 4 | 8.2 | $160 / 0.5$ | $10 / 4$ |
| 6 | 5.1 | $100 / 0.5$ | $13 / 7$ |
| 8 | 3.6 | $68 / 0.25$ | $18 / 10$ |


battery which is known to be in full working order; at this stage the circuit should perform as described above, except that it will not turn off after charging. The charging current can be checked; it should be 0.1 of the cell capacity (e.g. about 50 mA for 500 mAh (AA) batteries). The test battery is then left on charge for a long period - 20 hours, if flat. This guarantees that it stabilises at full charge voltage. Since the charging is constant-current, there is no risk of damaging the battery by charging for too long. At this point, VR2 can be slowly turned down until the circuit just switches off, and the setting re-checked. The unit is now completed.

## Modifications

The circuit was originally designed for AA size ( 500 mAh ) Ni -Cads, since these are the most widely used, but it can easily be adapted for other sizes by changing R9 and R10. These are calculated from the quoted values simply by reducing the resistance and increasing the wattage in proportion to the capacity; so for a 1 Ah six-cell battery, R9 would be 50R 1W and R10, 6R 15W. (The values do not have to be absolutely exact, of course). For cells over 1 Ah capacity, it is best to upgrade Q3 and Q4; since the circuit will be on for long periods it is advisable to rate components generously, especially heat sinks. Replacing Q3/Q4 with BD132/BD131 respectively, mounted off the PCB on a suitable heat sink, will enable the

## BUYLINES

[^0]PARTS LIST

unit to cope with cells up to about 4 Ah. As a rough guide, allow 1 Watt dissipation per Ah cell capacity when choosing heat sinks.
Remember that the heat sink on Q1 may need upgrading also. Allow a dissipation of 1.2 W per Ah cell capacity.

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|  | 36.04 | 200-300W | $4,8.8 .16 n$ | 5dB dynamic headroom |
| *PFA500 | 42.00 | 250-600W |  | Drives 70 l line direct. |
|  | 82.50 | mounted on | 74 Heat Exc | (see bolow). |

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## IC UPDATE

## Here are some more new ICs this month - ones that we do know you can buy!

## 74LS608 Memory Cycle Controller

- Provides correct timing for memory cycles
- read cycle
- write cycle
- read-modify;write. cycle.
_-"RAS"-only refresh cycle
- Page or normal modes
- Stand alone controller for CPU-to-memory interface
- Also designed to be part of a three-chip set consisting of LS600 through LS603, LS604 through LS607, and LS608 - RAS output is 3-state to share bus with LS600
- Critical times are user RC-programmable to optimise system performance

The LS608 memory cycle controller is designed to interface between a microprocessor and dynamic RAM memories. It contains six RS latches, five D-type flipflops, and more than 50 miscellaneous gates on a single chip. The LS608 combines maximum flexibility and ease of programming via RC nodes to allow optimum memory cycle performance.

After the user has selected and attached RC networks to pins 1, 12 and 15, the LS608 will deliver proper RAS, CAS, and READ/WRITE output signals to execute one memory cycle as the start input is switched from low to high. The actual cycle executed will depend upon steady state input conditions of the LS608 as indicated in the table below.

INPUT CONDITIONS

|  | INPUT CONDITIONS |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MEMORY CYCLE MODE |  |  |  |  |  |  |  |
| READ | H | H | H | L | H | † | L |
| WRITE PAGE | H | L | H | L | H | + | L |
| READ-MODIFY-WRITE | H | H | L | L | H | $t$ | L |
| READ | L | H | H | L | H | † | L |
| WRITE NORMAL | L | L | H | L | H | $t$ | L |
| READ-MODIFY-WRITE | L | H | L | L | H | t | L |
| REFRESH REFRESH |  |  |  | L | H | $\dagger$ | H |
| EXTERNAL REFRESH REFRESH |  |  |  | H | H |  | L |

Absolute Maximum Ratings
Supply voltage, $\mathrm{V}_{\mathrm{cc}}$
Input voltage
Off state output voltage
Operating free-air temperature range

PIN PIN NaME
i RC PRECHARGE
$2 \mathrm{P} / \mathrm{N} \operatorname{IN}$

3 R/W IN
.4 KMW $\mathbb{N}$
$5 \mathrm{R} / \overline{\mathrm{W}}$ OUT

6 RAS ENABLE IN
7 RAS OUT

8 GND
9 CAS OUT

11 ROW/COL (or MEMBSY) OUT

12 RC RAH
13 START $\mathbb{N}$
14 REFRESH IN
15 RC CAS LO


Fig. 1 Pin out of the 74 LS 608.

## Pin Function Table

## FUNCIONAL DESCRIPTION

User-programmable timing mode for precharge/CAS high and RAS high). When low, allows a normal read or write cycle. When high allows page mode read or write cycle. Holds RAS continuously low while CAS and column addresses are sequenced.
When high, initiates a read cycle (holds RNW OUT high) and, when low, initiates a write cycle (holds R/W OUT low) if pin 4 is high and pin 14 is low.
When low, enables read-modify-write cycle. R/W IN must be high at the stant of the RMW cycle.
When high, indicates a read cycle is in progress. When low, indicates a write cycle is in progress. Normally ties to a W memory input in a system.
When low, enables RAS output. When high, $\overline{R A S}$ ' is in the high-impedance or third state.
3-state row-address-strobe output controlled by RAS ENABLE IN. In the three-chip controlterset, the RAS output of the 'LS608 ties to the RAS output of the refresh controller (LS600 through LS603).
Device and substrate ground.
Column-address-strobe output.
When low, allows $\overline{\text { CAS }}$ to latch in low state. When high, latch is removed. Can be used to improve data retrieval during read cycle.

- Drives memory address multiplexer select input, and indicates BUSY condition to processor.
User-programmable timing mode ${ }^{\bullet}$ for row address hold time (high level at ROW/COL OUT).
When changed from low to high, initiates a memory cycle.
When high, enables RAS-only refresh cycle. User-programmable timing mode* for column address strobe low time.
5 -volt power supply terminal.
$16 \mathrm{~V}_{\mathrm{cc}}$ All timing modes require a resistor to $\mathrm{V}_{\mathrm{cc}}$ and a capacitor to ground Programmed time is approximately 0.29 RC.


NOTE: TAKING RAS EN HIGH TAKES RAS TO HIGH IMPEDANCE STATE AS INDICATED
Fig. 2 Normal read mode.


Fig. 3 Normal write mode.


Fig. 4 Normal read-modify-write mode.

Note that the read-modify-write cycle requires that R/W should go low at a suitable time after CAS (depending on the memory used). This cycle can be aborted (no write) by taking RMW high to terminate it, as shown in Fig. 5.


Fig. 5 Normal read-modify-write with abort after read.

Switching Characteristics (see waveforms for more detail) $\mathrm{V}_{\mathrm{cc}}-5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{C}_{\mathrm{L}}=45$ pf to GND

| PARAMETER | FROM (INPUT) | $\begin{gathered} \text { TO } \\ \text { (OUTPUT) } \end{gathered}$ | TEST CONDITIONS | MODE | TYP | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $t_{\text {Pht }}$ | START 1 | RAS | $R_{L}=667-R$ to $V_{c c}$ | NORMAL READ | 12 | ns |
| tor $^{\text {(1] }}$ | START i | $\overline{\text { RAS }}$ |  |  | 425 | ns |
| $\mathrm{taxil}_{\text {[2] }}$ | START 1 | $\overline{\text { CAS }}$ |  |  | 140 | ns |
| $t_{\text {mH }}$ [1] | START i | CAS |  |  | 405 | ns |
| $t_{\text {mel }}$ [2] | START 1 | RWW |  | NORMAL WRITE | 715 | ns |
| $t_{\text {min }}$ [1] | START i | R/W |  |  | 440 | ns |
| Cam | CAS HOLDI | CAS |  | NORMAL READ | 10 | ns |
| [mat [2] | START I | ROWICOL | $\mathrm{R}_{\mathrm{t}}=2 \mathrm{kO}$ to $\mathrm{V}_{\mathrm{cc}}$ |  | 125 | ns |
| ta..(3) | START i | ROWICOL |  |  | 670 | ns |
| 6 | RW ! | RW | R4L - 667 R to $\mathrm{V}_{\text {cc }}$ | NORMAL RMW | 14 | ns |
| Lnu[4] | RWW | RW |  |  | 355 | ns |
| tmu1 | RMWI | CAS |  |  | 40 | ns |
| tav[S] | RMWI | ROW/COL |  |  | 320 | ns |
| 601 | RAS ENJ | RAS | $\mathrm{R}_{\mathrm{L}}=667 \mathrm{R}$ to GND | NORMAL READ | 15 | ns |
| $4{ }^{1}$ | $\overline{\text { RAS ENI }}$ | RAS | $R_{L}=667$ R to $V_{\text {cc }}$ |  | 17 | ns |
| $t_{\text {m2 }}$ | RAS EN I | RAS | $R_{L}=667 \mathrm{R}$ to GND |  | 10 | ns |
| $\mathrm{tas}^{\text {c }}$ | RAS ENT | RAS | $R_{L}=667 \mathrm{R}$ to $\mathrm{V}_{\mathrm{cc}}$ |  | 17 | ns |

NOTE: Measurement point for all $t_{\text {PHz }}$ output pulses is 2.9 V . Measurement point for all $t_{\mathrm{p} 2}$ output pulses is 0.8 V . All other measurement points are 1.3 V .
[1] Depends on RC network at pin 12 ( $2 \mathrm{kO}, 180 \mathrm{pF}$ used for testing) and the RC network at pin 15 (Sk0, 180 pF ).
[2] Depends on RC network at pin 12 ( $2 \mathrm{kO}, 180 \mathrm{pF}$ ).
[3] Depends on RC network an pin 12 ( $2 \mathrm{k}, 180 \mathrm{pF}$ ), pin 15 (SkO $180 \mathrm{pF7}$, and pin 1 (SkO, 180 pF ).
[4] Depends on RC network at pin 1S (SkO, 180 pF).
[S] Depends on RC network at pin 1 (Sk0, 180 pF7.


Fig. 6 Typical circuit for use with 64 K by 1 DRAMs; for refresh, pin 14 is taken high, pin 13 is pulsed high, and refresh address is placed on the memory devices address pins.

# LF13331/2/3, LF13201/2 Quad Analogue Switches 



Fig. 7 Pin outs: LF1331 is four normally open switches with disable; LF13333 is two normally closed and two normally open with disable; LF13201/2 are as LF13331/2 but without disable.

These devices are a monolithic combination of bipolar and JFET technology producing the industry's first one chip quad JFET switch. A unique circuit technique is emoloved to maintain a constant resistance over the analog voltage range of $\pm 10 \mathrm{~V}$. The input is designed to operate from minimum TTL levels, and switch operation also ensures a break-beforemake action.
These devices operate from $\pm 15 \mathrm{~V}$ supplies and swing a $\pm 10 \mathrm{~V}$ analog signal. The JFET switches are designed for applications where a DC to medium frequency analog signal needs to be controlled.

## General Information

"ON" resistance are essentially independent of analog voltage or analog current. The leakage currents are typically less than 1 nA at $25^{\circ} \mathrm{C}$ and less than 100 nA at $125^{\circ} \mathrm{C}$ in both the "OFF" and "ON" switch states and introduce negligible errors in most applications. Each switch is controlled by minimum TTL logic levels at its input and is designed to turn "OFF" faster than it will turn "ON". This prevents two analogue sources from being transiently connected together during switching.

Because these analogue switches are JFET rather than CMOS, they do not require special handling.

## Logic Input

The logic input (IN\}, of each switch, is referenced to two forward diode drops (1.4V at $\left.25^{\circ} \mathrm{C}\right\}$ from the reference supply (YR\} which makes it compatible with DTL, RTL, and TTL logic families. For normal operation, the logic " O " voltage can range from 0.8 V to -4.0 V with respect to $V_{R}$ and the logic "1" voltage can range from 2.0 V to 6.0 V with respect to $\mathrm{V}_{\mathrm{R}}$, provided $\mathrm{V}_{\text {in }}$ is not greater than ( $\mathrm{V}_{\mathrm{cc}}$ - 2.5 V ). If the input voltage is greater than $\mathrm{Vcc}-2.5 \mathrm{~V}$, the input current will increase. If the input voltage exceeds 6.0 V or -4.0 V with respect to $\mathrm{V}_{\mathrm{R}}$, a resistor in series with the inputs should be used to limit the input current to less than $100 \mu \mathrm{~A}$.

## Analog Voltage

Each switch has a constant "ON" resistance ( $R_{\text {on }}$ ) for analog voltages from (Vee +5 V ) to ( $\mathrm{V}_{\mathrm{CC}}-5 \mathrm{~V}$ ). For analog
voltages greater than $\left(\mathrm{V}_{c c}-5 \mathrm{~V}\right)$, the switch will remain ON independent of the logic input voltage. For analog voltages less than $\left(\mathrm{V}_{\mathrm{EE}}+5 \mathrm{~V}\right)$, the ON resistance of the switch will increase. Although the switch will not operate normally when the analog voltage is out of the previously mentioned range, the source voltage can go to either $\left(\mathrm{V}_{\mathrm{Eg}}+36 \mathrm{~V}\right)$ or $\left(\mathrm{V}_{\dot{c}}+6 \mathrm{~V}\right)$, whichever is more positive, and can go as negative as $\mathrm{V}_{\mathrm{EE}}$ without destruction. The drain (D) voltage can also go to either $\left(\mathrm{V}_{\mathrm{tE}}+36 \mathrm{~V}\right)$ or $\left(\mathrm{V}_{\mathrm{cc}}+6 \mathrm{~V}\right)$, whichever is more positive, and can go as negative as ( $\mathrm{V}_{\mathrm{cc}}$ - 36V) without destruction.

## Analog Current

With the source (S) positive with respect to the drain (D), the $R_{o w}$ is constant for low analog currents, but will increase at higher currents ( $>5 \mathrm{~mA}$ ) when the FET enters the saturation region. However, if the drain is positive with respect to the source and a small analog current loss at


Fig. 8 Use of the disable node.

| "ON" Resistance | $V_{A}=0, I_{0}=1 \mathrm{~mA}$ | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 150 | 250 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | 200 | 350 | $\Omega$ |
| "ON"' Resistance Matching |  | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 10 | 50 | 0 |
| Analog Range |  |  | $\pm 10$ | $\pm 11$ |  | V |
| Logical "1" Input Voltage |  |  | 2.0 |  |  | V |
| Logical '00' Input Voltage |  |  |  |  | 0.8 | V |
| Delay Time "ON" | $V_{5}= \pm 10 \mathrm{~V}$ | $\mathrm{T}_{\text {A }}=25^{\circ} \mathrm{C}$ |  | 500 |  | ns |
| Delay Time ${ }^{\text {/ OFFF" }}$ | $V_{5}= \pm 10 \mathrm{~V}$ | $\mathrm{T}_{\text {A }}=25^{\circ} \mathrm{C}$ |  | 90 |  | ns |
| Break-Before-Make Time | $V_{5}= \pm 10 \mathrm{~V}$ | $\mathrm{T}_{\text {A }}=25^{\circ} \mathrm{C}$ |  | 80 |  | ns |
| Source Capacitance | Switch "OFF," $V_{S}= \pm 10 \mathrm{~V}$ | $\mathrm{T}_{\text {A }}=25^{\circ} \mathrm{C}$ |  | 4.0 |  | pF |
| Drain Capacitance | Switch "OFF," $V_{D}= \pm 10 \mathrm{~V}$ | $\mathrm{T}_{\text {A }}=25^{\circ} \mathrm{C}$ |  | 3.0 |  | pF |
| Active Source and Drain Capacitance | Switch "ON," $V_{S}=V_{0}=0 \mathrm{~V}$ | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 5.0 |  | pF |
| "OFF" Isolation | (Note 3) | $\mathrm{T}_{\wedge}=25^{\circ} \mathrm{C}$ |  | -50 |  | dB |
| Crosstalk | (Note 3) | $\mathrm{T}_{\wedge}=25^{\circ} \mathrm{C}$ |  | -65 |  | dB |
| Analog Slew Rate | (Note 4) | $\mathrm{T}_{\wedge}=25^{\circ} \mathrm{C}$ |  | 50 |  | V/ $/ \mathrm{S}$ |
| Disable Current | (Note 5) | $\mathrm{T}_{\wedge}=25^{\circ} \mathrm{C}$ |  | 0.6 | 1.5 | mA |
|  |  |  |  | 0.9 | 2.3 | mA |
| Negative Supply Current | All Switches "OFF," $\mathrm{V}_{\mathrm{s}}= \pm 10 \mathrm{~V}$ | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 4.3 | 7.0 | mA |
| Reference Supply Current | All Switches "OFF," $\mathrm{V}_{\mathrm{s}}= \pm 10 \mathrm{~V}$ | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 2.7 | 5.0 | mA |
| Positive Supply Current | All Switches "OFF," $V_{s}= \pm 10 \mathrm{~V}$ | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 7.0 | 9.0 | mA |

PARAMETER

Negative Supply Current
Reference Supply Current
Positive Supply Current

## CONDITIONS

$V_{A}=0, I_{0}=1 m A$
high analog currents is tolerable, a low $\mathrm{R}_{\text {ок }}$ can be maintained for analog currents greater than 5 mA at $25^{\circ} \mathrm{C}$.

## Power Supplies

The voltage between the positive supply ( $\mathrm{V}_{c c}$ ) and either the negative supply ( $\mathrm{V}_{\mathrm{E}}$ ) or the reference supply $\left(\mathrm{V}_{\mathrm{R}}\right)$ can be as much as 36 V . To accommodate variations in input logic reference voltages, $\mathrm{V}_{\mathrm{R}}$ can range from $\mathrm{V}_{\mathrm{EE}}$ to $\mathrm{V}_{\mathrm{CC}}$ -4.5 V ). Care should be taken to ensure that the power supply leads for the device never become reversed in polarity or that the device is never inadvertently installedbackwards in a test socket. If one of these conditions occurs, the supplies would zener an internal diode to an unlimited current, and result in a destroyed device.

## Disable Node

This node can be used, as shown in Fig. 8, to turn all the switches in the unit off independent of logic inputs. Normally, the node floats freely at an internal diode drop $(\approx 0.7 \mathrm{~V})$ above $\mathrm{V}_{\mathrm{R}}$. When the external transistor in Fig. 8 is saturated, the node is pulled very close to $V_{k}$ and the unit is disabled. Typically, the current from the node will be less than 1 mA .

## Absolute Maximum Ratings

Positive Supply - Negative Supply ( $\mathrm{V}_{\mathrm{cc}}-\mathrm{V}_{\mathrm{EE}}$ ) 36 V Reference Voltage $\quad \mathrm{V}_{\mathrm{EE}} \leqslant \mathrm{V}_{\mathrm{R}} \leqslant \mathrm{V}_{\mathrm{CC}}$ Logic Input Voltage

Analog Voltage

$$
\begin{aligned}
& V_{R}-4.0 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{IN}} \leqslant \mathrm{~V}_{\mathrm{R}}+6.0 \mathrm{~V} \\
& V_{E E} \leqslant V_{A} \leqslant V_{C C}+6 V ; V_{A} V_{E E}+36 V . \\
& \text { Moulded DIP (N Suffix) } 500 \mathrm{~mW} \\
& 0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C}
\end{aligned}
$$

Analog Current
Power Dissipation (Note 1)
Cavity DIP (D Suffix)
Operating Temperature Range

Note 1: For operating at high temperature the molded DIP products must be rated based on a $+100^{\circ} \mathrm{C}$ maximum junction temperature and a thermal resistance of $+150^{\circ} \mathrm{C}$ maximum junction temperature and are rated at $+100^{\circ} \mathrm{C} / \mathrm{W}$.
Note 2: Unless otherwise specified, $\mathrm{V} C \mathrm{C}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~V}_{\mathrm{R}}=0 \mathrm{~V}$, and limits apply; $-25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}+85^{\circ} \mathrm{C}$ for the LF13331, 2, 3 and the LF13201,2.
Note 3: These parameters are limited by the pin capacitance of the package.
Note 4: This is the analog signal slew rate above which the signal is distorted as a result of finite internal slew rates.
Note 5: All switches in the device are turned "OFF" by saturating a transistor at the disable diode as shown in Fig. 8. The delay times will be approximately equal to the ton or toff plus the delay introduced by the external transistor.


# Friday November 25th Saturday November 26th Sunday November 27th 

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# UNIVERSAL EPROM PROGRAMMER 

## To use our Universal EPROM programmer, you've got to have the software to drive it. Mike Bedford fills us in on what's needed.

The logical choice of programming language for a software package which is required to perform critical timing and which contains large frequently repeated loops, is assembler. On the other hand, the obvious choice of language for a package which is intended to run on a variety of different personal computers is BASIC. The software presented here is a compromise between the two: a BASIC program which performs the $1 / 0$ but which calls an assembler subroutine for the time critical or time consuming tasks.
The assembler routine starts at address 1C00, but this may need to be relocated in order to fit in with the memory map of some systems. If this routine is relocated, the variable MC on line 290 of the BASIC program will have to be changed to the decimal start address of the routine. Another portion of the BASIC program which may require tailoring to a particular system is line 310. The variable PA on this line contains the start address of the EPROM programmer hardware as selected by the links on the board. This address should also be updated in the assembler subroutine on line 23 which equates IC9PIA to the start address.
Microtan 65 BASIC uses the statement $\mathrm{I}=\mathrm{USR}(\mathrm{X})$ to call a machine code subroutine, having first POKE'd the low order byte of the M/C address to 34 and having POKE'd the high order byte to 35 . This is done on lines 4040-4060, 5030-5050, 6040-6060 and 7040-7060 of the BASIC program and may require modification on other machines.
Finally, the programming timing loop in the assembler routine assumes a processor clock frequency of the 750 KHz as used on the Microtan. The value loaded into register $Y$ on line 143 of the routine will have to be modified
accordingly for other clock speeds (use hexadecimal 27 for 1 MHz ).

As far as entering the program is concerned, the main BASIC program is rather long and it would be advisable to enter it in relatively small portions, saving it after the addition of each new section. This suggestion is made for two reasons: firstly it is difficult to concentrate for sufficiently long to enter the whole program at once without making errors; and, secondly it would be extremely frustrating if the computer were to crash for some reason after having typed in over 200 lines of code!

The assembler listing is rather long, and will only be of interest to readers wishing to modify the software. For this reason we haven't reproduced it here, but a copy may be obtained by sending a large
stamped addressed envelope (or international reply coupon) to the ETI office -please mark the outer envelope "PROGRAMMER
LISTING". Most users will find it easiest to enter the hex code directly.

Once the program and subroutine have been entered and recorded on cassette, it will be worthwhile investing some time carefully checking through the program. It is quite possible that a mistake may cause more than the appearance of the all too familiar SYNTAX ERROR on the screen: an error in the software could easily turn an EPROM programmer into an EPROM destroyer!

## Sample Run

On page 39 is a reproduction of

| 1000 | 4 C | 4 C | 1 C | 0000 | OU 00 | 00 | 00 | 0 | 0 | 0000 |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 ClO | 3 C | 3 C | 3C | 3434 | 3418 | 18 | 18 | 810 | 1010 | 1018 | 12 | 10 | 0 |  |  |
| 10.20 | 30 | 3 C | 34 | $343 C$ | $3 C 3 C$ | 3 C | 08 | 808 | 0808 | 0805 | 25 | 08 | 8 |  |  |
| 1C30) | 22 | 01 | 01 | 0101 | 0108 | 02 | 08 | 802 | 0206 | 0606 | 06 | 06 | 6 | 06 |  |
| 1 C 40 | 06 | 05 | 06 | 0101 | 0101 | 01 | 00 | 0 Ol | 0100 | 001 | 20 | 87 | 7 | 1 D |  |
| 1 CbO | UB | 1 C | C9 | 02 DO | 03 4C | BC |  | C 19 | 1930 | 308 D | 25 | BC | C 1 | 19 | 0 |
| $1 \mathrm{C60}$ | 8 B | 24 | BC | A9 34 | 8D 25 | BC | AE | E OC | OC 10 | IC BD | OD | IC | C 8 | d |  |
| 1 C 70 | BC | A9 | . 0 | 8D 20. | BC A9 | 3 C | 8D | d 25 | 25 BC | BC BD | 16 | 10 | C 8 |  |  |
| 1 C80 | BC | 20 | 9 C | 1 D 20 | 62 1D | DO | 03 | 34 | 4C 13 | 13 | 20 | 17 | 7 | 1 D | AD |
| $1 \mathrm{C9O}$ | 25 | BC | 49 | OB 8D | 25 BC |  |  | C 10 | ID AD | AD 2 |  |  |  |  |  |
| icao | A2 | (1) | AC | OB IC | FO 10 | 30 | 07 | 7 C9 | C9 FF | FF FO | BB | 4 C | C |  |  |
| 1 CB () | Cl | 35 | F) | B4 4C | 1310 | 81 | 35 | 3540 | 4 C 8 | 68 IC | 19 | 30 | O |  |  |
| ICCO | BC | A9 | FF | 8 D 24 | BC A9 | 34 | 8D | D 25 | 25 BC | BC AE | OC | c | BD | BD | D |
| 1CD) | 10 | 81 | 23 | BC A9 | 0088 | 20 |  | B BD | BD IF | IF IC |  |  |  |  |  |
| ICEO | 28 | 1 C | 8 D | 26 BC | 2) 9 C |  | 20 | 06 | 6210 | ID FO |  | 20 |  |  |  |
| ICFO | A2 | O) | A1 | 35 8D |  |  |  |  | 1 C BC |  |  |  |  |  |  |
| 1D()0 | 50 | 31 | 1 C | 9920 | BC AO | 10 | A2 | 2 FF | FF CA | CA 0 | FD | 88 | 8 D |  |  |
| 1 D10 | 4 C | Св | 1 C | 2087 | 1060 |  |  | 5 IC | IC 8D | 3D 22 | BC |  |  |  |  |
| 1 D20 | Fo | 09 | AD | un IC |  |  |  | C 52 | 5210 | D AD |  |  |  |  |  |
| 1030 | 10 | 8D | 20 | BC AD | 06 IC |  | 10 | 0 F0 | F0 08 | 8 AD | 20 |  |  |  |  |
| 1040 | 8 D | 2) | BC | AD 06 | IC 29 |  |  | 008 | 08 AD |  |  |  |  |  |  |
| 1 D 50 | 26 | BC | AD | 06 IC |  |  |  | 8 AD |  |  |  |  |  |  |  |
| 1D60 | BC | 60 | E | 3510 | 02 E6 |  | EE | EE 05 | 051 | C DO | 03 |  |  |  |  |
| 1 100 | AD | 06 | 1 C | 29 E7 | 8D 09 |  | AD | D 05 | 0510 | 1 C CD |  |  |  |  |  |
| 1 D80 | AD | 06 | 1 C | CD $\cup 8$ | IC 60 | 16 |  | 35 A4 | 1436 | 36 AD | 03 | 10 | C 85 |  |  |
| 1 100 |  |  |  | 8536 | 8E 03 |  | 8 | 04 | 04 |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Fig. 1 Hex dump of the machine code -see text for details of how to obtain the assembler listing, should you need it.


Fig. 2 The main BASIC program.

a printout obtained by running he EPROM programmer support package on a Tangerine Microtan system. Note that a base address of 2000 has been selected - this being the lowest reasonable-size area of RAM on the system, the BASIC program occupying about 6 K and the machine code routine being
located at 1C00.
In answer to the question about EPROM type, a response of 2716 was given. A 2716 EPROM was inserted into the ZIF socket when the first *? prompt was printed and this was tested for erasure using the (T)EST command. The program indicated that the device was not


XTP ${ }^{X}$ START, FINISH ADDRESSES? 0807,0007 0007 EPROM $=09$ MEMORY $=A F$

EPROM TYPE? 2732
STR

START, FINISH ADDRESSES? 0200,0210 OK

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# $1 / 3$ OCTAVE GRAPHIC EQUALISER 

## We conclude this studio-quality unit with the constructional details. Design by Dave Tilbrook, with additional work by Phil Walker.

The third octave equaliser divides the audio frequency band into 28 segments so a total of 28 slider pots are used.
Cutting the required slots in a front panel is an extremely difficult task so we strongly recommend using the special case from Newrad - see Bylines for details. We've deliberately chosen to use fairly small switches and indicator on the front panel - if you use larger ones, you can always enlarge the hole sizes.
Construction of the PCB is not difficult. The usual precautions should be taken with the orientation of all polarised components such as electrolytic capacitors, transistors, diodes and ICs. Note that the two voltage regulator ICs are mounted in the same direction.
Check the component overlay for the correct orientation. It is probably wise to leave the insertion of the quad op-amps until last since these are FET devices and are therefore more
sensitive to static electricity than the other components in the unit. Be careful when handling these devices before insertion on the board. Use an earthed soldering iron and discharge yourself by touching an earthed metal appliance before handling the ICs. The inputs are protected and should therefore be reasonably safe from damage by static electricity.
The method of construction we have chosen is to mount the slider pots directly on to the front panel (using short, countersunk M3 bolts) with the PCB behind.
The potentiometer wipers are attached alternately to the top and bottom of the PCB; if you use a type of pot that has only one wiper connection (as we did), then you'll have to make sure that adjacent pots are reversed on the front panel.

## Interwiring

Before we mounted the PCB into the case, we soldered leads into the correct position on the PCB
for joining onto the potentiometer wipers. Note that the tops and bottoms of the slider tracks should all be joined up before the board is mounted.

We mounted the board using metal struts and plastic pillars. The struts can be attached to the aluminium extrusion by sliding the head of a $1 / 2^{\prime \prime}$ (we really mean 12 mm !) M3 bolt into the aluminium extrusion, and then clamping this in the correct position using a nut (or three, in our case, to get the spacing of the strut correct). If you don't use plastic pillars, you'll have to make sure that the PCB tracks are not inadvertently earthed by the fixing screws.

We've left the drilling of the holes in the rear panel to you, as you'll almost certainly decide to use different connectors, etc, from us! Because the case is fairly compact (neat, in ETI speak) you'll need to take care over the positioning of the fuse, mains input socket and transformer, to make sure that you


## PROJECT



This photograph shows the connections between the slider pots on the front panel and the PCB - and the mounting of the front panel using struts and spacers. Note that we couldn't fit the prototype PCB into our equipment and had to make it in two sections hence the join!
don't foul the PCB. Remember that the earth on the input and output sockets must be kept separate from the case. But make sure that the case and the transformer are well earthed - we suggest making doubly sure by removing paint or
varnish around the earthing point(s) (on the inside, in the case!). To cut down mains hum, we used a screened twin cable for the internal mains lead - this needs to have adequate conductor and insulation thickness, though.


Fig 1 Overlay diagram for the PCB.

## PARTS LIST

We used universal adhesive to glue on the pot knobs, otherwise they all kept falling off!

## Power up

Once construction is complete, check all power supply wiring before powering up. This is especially important if a transformer has been included inside the case. In the latter case, make certain all 240 V connections are secure and check the chassis earth. If all is correct, power the unit up. The LED should light to indicate that the unit is on-

An equaliser in/out switch has been provided to ensure that a flat response can be obtained easily and without the necessity of changing the equalisation that may have • taken some time to set up. The equaliser is intended for use immediately before the power amplifier. If used in this. position the level control will probably not be used. In this case turn the control fully counterclockwise. The overall gain of the equaliser with the controls set at centre will be approximately unity. If the equaliser is intended for use from a typical line level output, the gain control can be used to supply the output levels needed by the power amplifier input.



## BUYLINES

The case is available by post only from Newrad Instrument Cases Ltd, Tiptoe Road, Wootton, New Milton, Hants BH25 551 for the special price of $£ 21.00$ all inclusive to ETI readers only (this is for either the rack mounting version we used or one with plain ends - please state which you require when ordering). The PCB is, as ever, available through our PCB service. We've already mentioned the slight problem of obtaining the capacitors and how we solved it, last month. None of the other components should present problems, though as you'll be buying a number of slider pots, it's obviously worth shopping around for a good price. The cheapest we found were those from Rapid, and that's where we bought ours from.

## 00PS!

Note that the value of R65-80 is 10 R , not 1 kO as shown on the circuit diagram. We recommend that you switch the unit out of circuit (using the EQ OUT switch) before removing or connecting the supply, because it is capable of issueing a nasty squalk!

## 

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Where a project has apparently been constructed correctly but does not work, we will need a description of its behavior and some sensible test readings and drawings of oscillograms if appropriate. With a bit of luck, by taking these measurements you'll discover what's wrong yourself. Please do not send us any hardware (except as a gift!);

Other than through our letters page, Read/Write, we will not reply to enquiries relating to other types of article in ETI. We may make some exceptions where the enquiry is very straightforward or where it is important to electronics as a whole;

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## OOPS!

We have in the past published small corrections to projects on the letters page, and major corrections separately. From now on corrections will appear on this page, and will be repeated for several months (just to increase our embarrassment). If a correction is too large to fit on here, we will publish it just once, but will note the fact that a correction does exist, and that copies of it can be obtained from us provided you send in an SAE. But please request copies only if you really do need them; if this service is abused, we may be forced to withdraw it.

ZX A to D (Jan '83)
D2 is shown the wrong way round on the overlay; wires on the RH side of the switch SW1 should go to top contacts. Some of the early PCBs had an error: pins $2 \& 4$ of IC1 should go to pin 16 (top) of edge connector (published foil pattern is OK).

Stage Lighting Unit (Jan, Feb, April, May '83)

Transformer specs are as follows: Primaries all 250 V ; secondaries T1: 0-6, 0-6 V, 12 VA tot; T2: 0-12, 0-12 V, 12 VA tot; D: 0-6 V, 3 VA. ICs 34, 35, 36 are 7805 SV regulators.

## ZX Sound Board Design Comp. results, Feb

 '83)The first line of the program has to be entered in reverse order to get it to go in (COS, GOSUB, COPY, ASN and RND are functions). The line should read:

10 REM :"Y -=?COS GOSUB 5 COP Y ?? ASN ?RNDF??RND

Alarm Module (March '83)
R21 Is 220k (parts list OK, circuit diagram wrong) Q5 is BC182L (left off parts list).

Max Min Thermometer (April '83)
A revised foil pattern was published in July ETI. To get original PCB to work, replace D4 and D5 with wire links, cut tracks from pins 7 and 8 on IC6, and solder 15k resistor across cut - remove ICs while doing this! (It's messy but it works.)

## Real Time Clock (April '83)

Frequency of XTAL1 is 32.768 kHz .
NDFL Power Amplifier (May '83)
C13 is 33 pF (parts list correct, circuit diagram wrong).
Table 1: lengths of wire quoted do not allow for lead lengths -add 40 mm or so to them. This is particularly important for L3. Resistors R29 and R30 can be wire wound types, it isn't necessary to use carbon types (their inductance will be small).

Flash Sequencer (July '83)
Q1 should be BC184L; Q2-5 should be BC182L.

## Telescope (August 1983)

We had a shower of annotation falling off our diagrams! On Fig. 1, C19 (below IC14) was not labeled nor was Q2 (above R1), and there were two C23s -one should be IC22 and it doesn't matter which. In Fig. 5, IC1 2 was not labeled. Unfortunately, there was a mistake in the correction (blush!): C14 is the $22 \mu \mathrm{~F}$ tantalum on the -5 V line.

Universal EPROM Programmer (August 1983)
We had the same problem with falling annotation as above. On the overlay, IC7 is between SK2 and SK1; IC6 is between SK1 and C10; IC1 1 is between R7 and R10.

## Z80 Controller Computer

Same problem yet again. On the overlay, SW1 is the rectangle beside IC5 and 6; a link through was missed to the right of pin 18 IC11.

## READER'S SERVICES



# FEATURE 

# TECH <br> TIPS 

## Dual Trace Unit <br> John Hesketh, <br> Pontefract

There have recently been two circuits published in ETI which allow two waveforms to be displayed simultaneously on a single beam oscilloscope. Both of these circuits have drawbacks, namely poor preamp performance, inadequate control over waveform position, a tendency towards instability and poor switching circuitry. The design shown overcomes these problems and will display waveforms clearly over the frequency range DC to 200 kHz .

The design may be divided into three sections, two preamplifiers (one for each channel) and a switching circuit. The switching circuit is identical to that in J. C. Harris's circuit (ETI Feb 82).

The input signal is applied to an attenuator network either via a 100n capacitor for AC coupling or directly
for DC coupling. The attenuated signal is then fed to IC1 which is wired for a gain of one and functions as an impedance matcher. This stage gives the instrument a high input impedance (approximately 9MO). A portion of the output signal from IC1 is derived via RV1, which serves as an amplitude control, and is fed to IC2 and associate components which is also wired for a gain of one. This stage provided a means of shifting the vertical position of the waveform by introducing a DC voltage onto the non-inverting input of IC2 via RV2. This stage inherently inverts the waveform and therefore a further inverting stage is employed (IC3 and associated components) to restore the original sense of the waveform. The outputs from the preamplifier's IC3/6 are fed into the signal switching arrangement consisting of IC7 and
IC8. The output from the electronic switch is then fed to the oscilloscope. In order that a wide range of
signal frequencies may be displayed, two modes of switching are employed. The two modes are 'chop' and 'alternate' and the mode of switching is determined by SW5. When displaying frequencies from DC to 15 kHz , it will be necessary to use the 'chop' mode but for frequencies above 15 kHz the 'alternate' mode should be used.

The settings of VC1-4 are quite critical at high frequencies ( 200 kHz ), and the following procedure should be adopted in order to obtain the optimum setting of these trimmers. (The procedure is described for channel No 1 as channel No 2 is identical). Inject a $200 \mathrm{kHz} 1 \mathrm{Vp}-\mathrm{p}$ square wave into channel No 1 input and set the attenuator switch (SW2) to the $1 / 1$ position. The setting of SW1 is unimportant. Set RV1 to maximum and RV2 to mid position. Connect an oscilloscope to the output of IC2 and adjust VC1 for a perfect square wave with no overshoot or corner rounding. Remove the oscilloscope and connect to the output of IC3. Adjust VC2 for a perfect square wave. Repeat the procedure for channel No 2.

Note that the circuit requires a split supply of $\pm 9 \mathrm{~V}$.


## Low-Cost Mains Time Delay Switch Alex Gray, <br> Emberton, Bucks

This circuit offers a cheap, reliable replacement replacement for mechanical. and pneumatic time-delay switches such as used for corridor lights. It can also be used to protect equipment which is upset by power being applied and removed too rapidly.
When the switch is closed and reopened, the load is switched on for a preset time -1.1 $\mathrm{R}_{1} \mathrm{C}_{1}$. During this period, the circuit also switches on its own power. At the end of the time-delay both the load and the circuit are disconnected. In the event of a circuit failure, the push button will still allow the load to be switched on for safety (e.g. in corridor lighting).

If the switch is a normal latching type, the load will be powered as long as the switch is closed, subject to a minimum period. This prevents rapid cycling of the power on and off and may be used to protect equip-ment susceptible to damage from this situation.
There are only three connections and the circuit may be wired in at the ceiling rose of a conventional 'looped through circuit without any additional wiring.


The usual precautions with mains wiring must be observed. In particular, remember that, although the 555 is on a 12 V supply, that supply is
superimposed on 240 V AC above earth. The switch and the 470nF capacitor must be types designed for mains operation.

## Karnaugh Map Display

## K. J. Beeden,

## Crawley

The Karnaugh map is a common way of representing the function of a four-input logic system. It is often taught in schools and colleges, when students are given a logic system and have to draw the Karnaugh map for it. This device allows the student to go away and test his map with the actual map generated by this device and a wired-up system on a breadboard.

IC5a and b form an astable, which clocks the 4-bit binary counter IC1. The outputs of this are fed into the quad true complements buffer, IC2, providing buffered true and inverted outputs to the system under test. The counter outputs are also used to decode the display -the three LSBs are used as select lines for the eight-way analogue switches, IC3 and 4, and the MSB is used to select the chip by connecting the true value to INH IC3 and the inverted (by IC5c) value into INH IC4.
The output of the system is connected to the input of IC5d,e,f. Thus if the output
output of the system is high for a given 4-bit number, then the output of IC5d, etc, will be low, and so current will flow from the +ve supply, via the selected analogue switch (resistance of which is conveniently about 160R) through the appropriate LED. If the output of the system is low, then the output of IC5d, etc, will be high, and so no current will flow.

This means that an illuminated LED represents a " 1 " from the system, and an unlit LED a "0".

Figure 2 shows the arrangements of LED's 1-16 required to obtain the desired Karnaugh map display.


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## THE DIGGER

No, no, it's nothing to do with tubes of amber nectar, billabongs, tucker bags or any other antipodean artifacts. Just a device for digging around in a digital circuit using an oscilloscope - a digital trigger. Design, development, and bad puns by Phil Walker.

The ETI Digger is a very simple device which will make fault finding on digital circuits very much easier. The basic unit is in reality an eight bit comparator which provides an output signal when the input. signal is the same as that set up on the unit's switches. The unit as described will handle up to eight logic inputs which will probably be sufficient for most purposes. However, it is designed so that additional units may be plugged into the first to expand the total capability in blocks of eight.

## Use

The unit must be provided with a normal TTL type +5 volt power supply (probably conveniently derived from the equipment under test $\}$. The output can then be taken to the external trigger input of your oscilloscope. In case you hadn't guessed, your next move is to set the scope to external trigger; you may have to adjust the trigger controls for best results, especially if the circuit under test contains ripple counters. The reason for this is that signal propagation delays in the devices will cause glitches in the

## HOW IT WORKS

[^1]

Fig. 1 Circuit diagram.
output from the Digger unit. This is not a fault, as the input conditions are in fact true, even if only for a short time. Actually this property of the Digger could be quite useful if you suspect this action in your own circuit.

The leads from the device can be connected to the test circuit in any order but remember to set the switches in the corresponding order
or your results will be wrong. It is a good idea to use the input nearest (he output as a clock input, as this will eliminate a good many ambiguities. Don't forget to set any unused input channels to HIGH or the unit will not trigger!

## The Circuit

The circuit for this device is very simple. Most of the work is



## PARTS LIST

| RESISTORS (1/4 W 5\% carbon film unless stated) |  |
| :---: | :---: |
| R1 | 2K2 |
| R2-R9 | 1 K (SIL resistor pack $8 \times 1 \mathrm{~K}$ ) |
| R10-R17 | 2K2 (SIL resistor pack $8 \times 1 \mathrm{~K}$ ) |
| CAPACITORS |  |
|  | 10uF 16V electrolytic |
| SEMICONDUCTORS |  |
| IC1, IC2 | 74LS85 |
| LED1-LED8 | 3 mm Red LED |
| MISCELLANEOUS |  |
| SW1-SW8 | 8 pole SPST DIL switch |
| 10 way PCB socket 0.11 pitch; 5 way PCB |  |
| socket, 0.1 " pitch; 5 way right angle PCB |  |
| plug 0.1" pitch; box (Vero G.P. plastic box |  |
| $72 \times 50 \times 25 \mathrm{~mm}$ 202-21025K); PCB; 10, 5 |  |
| way free plugs and 5 -w | way socket for above. |

done by the two ICs which are 74LS85 devices. These are TTL fourbit magnitude comparators, and give outputs which show whether one of the two four-bit binary numbers presented to their inputs is equal to, greater than, or less than the other. In addition to the normal inputs, there is also a set of inputs which take the outputs from another similar device. When these are connected, the final output depends on all the comparisons of all the inputs to the devices connected in this way.

The rest of the circuit is devoted to providing the requisite comparison inputs to the ICs and giving a visible indication of it. The method of doing this is to use resistors to hold the inputs normally at a low level, but with switches that can force them high via an LED which will light up to show that it has been selected. The logic inputs from the test circuit are provided with pull up resistors so as to define unused inputs.

## Construction

Construction of the PCB is quite simple so long as the ICs are inserted the right way round. The LEDs and capacitors must likewise be put in correctly. If you are going to use resistor packs as we did, the end with the dot or similar mark is the common terminal. Verify this with a meter if in doubt. If you use discrete resistors, mount them vertically and join all the top ends to the common terminal with a piece of stripped solid-core wire.

It will be necessary to use a 16 pin wire-wrap type socket for the DIL switch so that it can be positioned through a hole in the box. The LED leads will probably be long enough without extension. We would also recommend using ordinary sockets for IC1 and IC2.

There are 5 links to insert on the board as marked on the overlay which connect the inputs to SK2. Use thin insulated wire for these. Mounting the PCB in the box is a little tricky. First make sure that the corners have been cut off at the marks shown and check that the board will fit into the box. We found it easier to fit the PCB upside down in the box (with the track side facing the lid), so that only a little of the side walls have to be cut away to allow SK1, SK2 and PL1 to fit. Also a rectangular cut-out must be made in



Left: Overlay of the Digger; above: the Digger itself, less case.
the bottom of the box to allow SW1SW8 through. Finally eight 3 mm holes should be drilled for the LED's.
The PCB can now be bolted to the lid and the box put together. Connections to the outside world are made via the plugs and sockets. If you use rightangled plug parts, then a small piece of Veroboard soldered to them makes a robust connector. The socket should be a socket housing with crimp terminals. For greatest convenience the power connections can be made via the free socket and PL 1 while the trigger output goes from SK1. The switch can be mounted either way round in its socket allowing you the option of the test leads coming out of the top or bottom of the device, while the switch position is still up for high, for example.

## BUYLINES

Nothing in this project should cause much difficulty; the SIL resistors are fair-ly widely available from suppliers such as Watford, Cricklewood, etc. The con-nectors are available from Maplin, and the PCB is available through our very own service.

Two or more Diggers can be cascaded.
Two or more Diggers can be cascaded.





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# AUDIOPHILE 

## Audiophile returns with a look at a new version of an old favourite. Ron Harris (Who's he? -Ed) has been playing with little boxes.

What do you mean "Oh no, not again?" Thought you'd got rid of me, huh? It's not as easy as that my friends. Audiophile returns to ETI with a look at some new boxes with an old and revered name-Minimax 2.
The Minimax 2s are a two-unit ported design of tiny proportions. This is a complete redesign from the originals and the speakers have a lot to live up to.
All by themselves, the original Minimaxes practically rewrote the hi-fi gospel that speakers must be big to be credible. This led to a host of manufacturers taking a serious look at the idea of high performance small enclosures, witness the


The boxes in question, in semi-naked glory! Note the-bass reflex port: the old Minimaxes didn't have that!
plethora of imitations there are now.
Presumably the idea behind the redesign is to re-establish the Videotones as the leading small speakers and the indications are that they are selling very well. Celestions magnificent SL6s have unquestionably taken this field a good deal further forward, but at a price. The Minimax 2 s are considerably cheaper and are not intended to be directly competitive.

## Moving Experiences

The main problem with any small box is how to move the mass of air required to produce useful bass response when the speaker is too compact to house a large driver. Because the enclosure is smaller than the wavelength of the sound it is producing, cancellation occurs between the air mass in front of the driver and that behind the box. In short, as the unit tries to push the air away from it, instead of traveling outwards, the wave just 'wraps around' and dissipates most of its energy before reaching the listener.

This is why small speakers produce better bass close to a wall. You can't cancel a wall. The more solid the better, as the mass is what counts. As an added help, the bass driver should be of the long excursion variety in order to transfer as much energy into the air as possible. If you must use a small paddle then you have to move it further for the same effect as would be obtained with a larger surface area.

## Field Work

In order that the bass driver should be able to move freely and without inducing gross distortion, the coil and magnet within which it moves must be made longer also, so that the coil never moves out of the linear region of field and is therefore evenly driven at all signal levels.

Also, although a smaller set of wooden panels should be easier to damp, and thus have their resonances kept under control, in a real box any bracing material used is more likely to affect the overall sound quality. This is simp-ly because the volume of the bracing subtracts from the volume of the .enclosure, and the less there is to start with, the less left! It is the bass which suffers, so a trade off is required. Resonating panels will colour the sound, too much bracing will reduce the base ... hmm, perhaps we could launch a computer game called 'Design A Speaker'.

## In Use

Having now run briefly through the horrors of designing small speakers, how do the Minimax 2 s measure up? Despite all the pitfalls do they actually produce a creditable result? In a word yes. The originals were very worthy units and the Mark 2s should carry on the tradition admirably.

I wired in the units, somewhat unfairly, in a direct comparison to my usual reference speakers, KEF105 II's which are anything but small. The Minimax was positioned off the floor, clear of walls and for a second attempt on a shelf flat against the wall to simulate more usual conditions of usage.

The amplifier was a Denon PRA2000/POA3000 Class A set-up and the record source provided by the well trusted TD160S/SME III carrying a Shure V1 SV cartridge.

To those of you who think it 'unfashionable' to use an SME rude words and expletives. Unaffected by the frantic pursuit of something new for the sake of it often to the detriment of the results the SME continues to out-perform the pretenders. So there!

On an absolute scale the Minimax 2 is a worthwhile product. Taking into account its size, it is positively brilliant. Its greatest asset is the ability to project the sound image away from the enclosures, out into the room: This makes it very easy to forget the boxes and the size of them.

## The Wall

Used in 'free-space' i.e. clear of all room boundaries, the Minimax understandably loses body in its presentation. Given a wall to help out, however, it can make a nonsense of its dimensions.

The new high frequency unit appears to improve both the smoothness and the spread of the presentation. The image is now much less dependent upon the listener's position and is free of any noticeable frequency response irregularities. Integration between the two units is good and the mid-range has a good solid sound to it.

Someone used to big, free standing enclosures, with a good deal of power behind them, would of course notice the lack of bass extension at once. However, as a starting point in hi-fi, or as a compromise answer in a small room, the Minimax 2s have much to recommend them. At the low price of $£ 75$ per pair, they are very good value and should be listened to seriously if you are thinking of buying a pair of small speakers, for whatever purpose.

One word of caution, they are relatively inefficient and hooking up less than 20W a channel is unlikely to elicit the best results from these diminutive demons.


Above: the trusted reference. An SME III doing it's bit whilst sat on a Thorens TD160S. A great deal of mud has been slung at several excellent products lately, including the SME. Ignore it. Let your own ears decide. The SME will stand up to ANY properly conducted comparison (i.e. scientifically). If you think I'm getting upset you could be right. I'm thoroughly cheesed off with unqualified, unprincipled and unsound review techniques. A mandatory qualification for producing some of this stuff seems to be that the applicant must be able to prove he has achieved brain death. End of tantrum.
would recommend around 50W per channel, despite the manufacturer's indrawn breath of cowardice. Take it easy on the volume, to the extent of not pushing in Status Quo full up, and you will be returned a smooth, well imaged sound with good hi-fi extension and more bass than you thought feasible from a box this size!

## The Preamp And The Packing Case!

Also this month I was going to review Musical Fidelity's "The Preamp", an audiophile unit of modest cost and high aspirations. Due entirely to the fact that I am moving house and my entire reference system, nay life, is packed into cardboard boxes and is presently being shuffled through the lanes of Kent, I am unable to do so!

My apologies for this and as soon as normal service is resumed I will complete the findings. Meanwhile, have a topless photo.

Exit Ron Harris pursued by the office chapter of the Womens Liberation Movement, in a none-too benevolent mood.


The Preamp. Not royal, but well titled. Soon, all will be revealed in even more detail!


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# Z80 CONTROLLER COMPUTER 

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No computer can talk to the outside world on its own - it needs interfaces to achieve this. As we've already mentioned, MARVIN is a modular computer, and so his interfaces are built on separate boards. There are two types of interface - the I/O board, and the interrupt board, both of which we will now proceed to describe.

## HOW IT WORKS I/O BOARD

## The circuitry divides into three parts - the

 control logic (IC1 and 2), Port A (IC3 and 4) and Port B (ICS and 6). In fact there are four ports per board the input, and to enable the relevant IC. Note that separate but sharing the same addresses.The port selection logic is very simple; four AND gates are used to detect. when one of the ports is being addressed and to enable the relevant IC. Note that the selection signals are active low. Because the system is quite simple, it was not judged necessary to include cir-cuitry to avoid more than one port being enabled at once.

The output ports (ICs 3 and 5) are based on the 74LS373 octal 0-type transparent latches: while the EN G input is high, the outputs follow the in-puts. When EN $G$ is taken low, the lat-ches will be set to the current data. There is also an output control which may be useful in some circumstances. When this is taken high, the outputs from the 74LS373 go into a high impedance state, irrespective of the latch contents. However, the latches themselves are unaffected by the output control, and they will retain their cur-rent data, or can be set to new data. R1 and R2 keep the output control (OC) inputs, to ICs 3 and 5 respectively, low in the case of no external control signal.

The input ports (ICs 4 and 6) use 74LS244s: these are octal buffer/line drivers with tri-state outputs (the outcuts are connected directly to the data bus Internally, the buffers are in two groups of four, with separate gate inputs (G1 and G2), and when these inputs are taken low, whatever information is at their data inputs will be placed on to the data bus.

## The I/O Board

The I/O board is seen by the CPU board as two I/O ports, which we've labelled A and B. Each port
has eight output lines (ie, one byte in either direction) making a total of sixteen lines and eight either direction per board. As we


әq иеэ әдәчъ ‘чұиои 7 se р рәио!ұиәш uət 'ə!!) spueoq 0/I ən!t of dn presently configured
To write to a port, the CPU places the required data on the data bus and makes the WR and the relevant port selection line low. The data is actually latched into the port when one or both of
 łndu! әчł MO!|Oł I!!M słndłno әчł łu!̣od ұеч7 ו!

 to the port, with repeat data in the

 məishs әчł म! injəsn aq p!noj s!̣」
 any extent autonomous, e.g. it contains another processor. Note, pinoys sәu!! findłno әчł łеч7 ‘дәләмоч
 (with respect to Marvin's earth), otherwise damage may occur.
әЧł 'рәұכәןəs s! fod andu! ue иวчМ inputs to it are buffered on to the data

 errors.
 board to signal the CPU board that it wishes to transfer data - like a shy little wallflower at a noisy disco, it has to wait әчł səop กdכ әчł pue 'рәуse $\mathrm{s}_{\mathrm{i}}$ ?! !! ! un
 selection line low.

## Interrupt Board

This board is intended for use with external timing and triggering devices.
 make the CPU stop whatever it is doing and pay attention!

## PROJECT

Fig. 4 Overlay of the interrupt board.
Fig. 5 An example of how the port addresses can
be defined on the $1 / 0$ board itself. In this case,
port A has address 5 , port $B$ has address 0 . There
is no need to use pins unless you will be changing
around port addresses suite a lot -permanent wire
links should do the job otherwise.

Fig. 6 If you don't have a suitable power supply to hand, you'll have to build one. Here is a fairly standard circuit: allow current consumptions of 500 mA for the CPU board, 200 mA per
$/ / 0$ board, and 100 mA for the interrupt board. The transformer should be able to supply more than enough current to meet the maximum demand, and C1 should be about 5000uF per amp of supply current drawn.
шодя səu!! ן ןnp!n!pu! uni ueว no人 дәчә!ə the selection signals on the CPU board

 Fig. 5 shows an example of this.


| PARTS LIST <br> INTERRUPT BOARD |  |
| :---: | :---: |
| RESISTORS (1/4 W 5\%) |  |
|  |  |
| $\begin{aligned} & \text { CA } \\ & \text { C1 } \end{aligned}$ | 1nF ceramic or polystyrene |
| SEMICONDUCTORS |  |
|  | 74LS373 |
| IC2 | 7430 or 74LS30 |
| IC3 | 7414 or 74LS14 |
| D1, D2 | 1 N4001 |
| MISCELLANEOUS <br> PCB; one 14-pin DIL socket; one 20 -pin DIL socket; pins or edge connector as required |  |
|  |  |

> Construction
> Construction of both these boards should be absolutely straightforward. We recommend using sockets for all but the simplest of the TTL gates (ie, don't bother for IC1 and 2 on the I/O Board, or with IC3 on the Interrupt -Board). Don't forget to insert the wire links as shown, and if you're not bothering with edge connectors, you'll need to insert pins in the PCB next to the edge connector
 pins in the positions marked on the I/O
 ports -but see the I/O Port Identification Section first, and decide whether you'll
be changing around the system much.

## Making The Connections



 stated, you have a choice between using edge connectors (the rich
 use

provided, and these should normally be at logic high. If any line is pulled down to low, the CPU will accept the interrupt provided it has executed an enable interrupts (EI) command since the last interrupt occurred or disable interrupts (D1) command was executed. The CPU will not accept further interrupts until El has been executed again.
The CPU will complete executing the current instruction, then go to the interrupt servicing routine in the operating system. As described in the "How It Works" section, the interrupt board latches the data on the interrupt input lines when one makes the high-to-low transition, and then the monitor instructs the CPU to read this data. This will consist of all 1s except for the bit that corresponds to the input that's causing all the fuss. According to which bit it is that is zero, the CPU will look for the address of the next instruction to be executed from one of eight memory locations in RAM.
 generate another interrupt until the reset to high (and any other lines that have gone high in the mean time have also been reset).

## GET Bic



| Module Number | Output <br> Power <br> Werts <br> rms | $\begin{array}{\|c\|} \hline \text { Load } \\ \hline \text { impedonnes } \\ \Omega \end{array}$ | $\begin{aligned} & \text { DISTT } \\ & \text { T.H. } . \\ & \text { TVo.at } \\ & \text { 1KHz } \end{aligned}$ | $\begin{aligned} & \text { ORTION } \\ & \text { I.M.D. } \\ & \text { GOH2 } \\ & 7 \mathrm{KHz} 4: 1 \\ & \hline \end{aligned}$ | Supply Votrap Typ | Size mm | $\begin{aligned} & \text { WT } \\ & \mathrm{gms} \end{aligned}$ | Price Inc. VAT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| h:Y 30 | 15 | 4.8 | 0.015\% | <0.006\% | $\pm 18$ | $76 \times 68 \times 40$ | 240 | £8.4 |
| hyfio | 30 | 4.8 | 0.015\% | <0.006\% | $\pm 25$ | $76 \times 68 \times 40$ | 240 | ¢9.55 |
| HY6060 | $30+30$ | 4.8 | 0.015\% | <0.006\% | $\pm 25$ | $120 \times 78 \times 40$ | 420 | ¢18.69 |
| hyriz | 60 | 4 | 0.01\% | <0.006\% | $\pm 26$ | $120 \times 78 \times 40$ | 410 | £20.75 |
| HY128 | 60 | 8 | 0.01\% | <0.006\% | $\pm 35$ | $120 \times 78 \times 40$ | 410 | £20.75 |
| HY2n4 | 120 | 4 | 0.01\% | <0.006\% | $\pm 35$ | $120 \times 78 \times 50$ | 520 | £25.47 |
| HY248 | 120 | 8 | 0.01\% | <0.006\% | $\pm 50$ | $120 \times 78 \times 50$ | 520 | £25.47 |
| HY364 | 180 | 4 | 0.01\% | <0.006\% | $\pm 45$ | $120 \times 78 \times 100$ | 1030 | £38.41 |
| HY368 | 180 | 8 | 0.01\% | <0.006\% | $\pm 60$ | $120 \times 78 \times 100$ | 1030 | £38.41 |


| Module Number | Output Power Watts rms | $\begin{array}{\|c\|} \hline \text { Loond } \\ \text { Impeodorne: } \\ \Omega \\ \hline \end{array}$ | DISTORTION |  | Supply Voluge Typ | $\begin{aligned} & \hline \text { Size } \\ & \mathrm{mm} \end{aligned}$ | $\begin{array}{\|l\|} \hline \text { WT } \\ \text { gms } \end{array}$ | Price inc. VAT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | T.H.D. Typat 1KHz | $\begin{aligned} & \text { 1.M.D. } \\ & \text { 600Hz } \\ & 7 \mathrm{KHz} \mathrm{4:1} \end{aligned}$ |  |  |  |  |
| MOS 128 | 60 | 48 | <0.005\% | <0.006\% | $\pm 45$ | $120 \times 78 \times 40$ | 420 | £30.41 |
| MOS 248 | 120 | 48 | <0.005\% | <0.006\% | $\pm 55$ | $120 \times 78 \times 80$ | 850 | ¢39.86 |
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Input impedance: $100 \mathrm{~K} \Omega$.

Protection: Full load line. Slew Rate: 15v/ /ss. Risetime: Sus. S/N ratio: 100 db Frequency response ( -3 dB ) $15 \mathrm{~Hz}-50 \mathrm{KHz}$. Input sensitivity: $\mathbf{5 0 0 \mathrm { mV } \text { rms. }}$ input impedance: $100 \mathrm{~K} \Omega$. Damping factor: $100 \mathrm{~Hz}>400$.

| Module Number | Module | Functions | Current Required | Price ine. VAT |
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| PSU 43x | $1 \times \mathrm{MOS} 128$ | £16.70 | PSU 55X | $1 \times \mathrm{MOS} 248$ | £19.52 |
| PSU 51x | $2 \times \mathrm{HY} 128,1 \times \mathrm{HY} 244$ | £17.07 | PSU 71X | $2 \times \mathrm{HY} 244$ | ¢21.75 |


| $\begin{aligned} & \text { Moden } \\ & \text { Nurmber } \end{aligned}$ | For Use With | Price inc. VAT |
| :---: | :---: | :---: |
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# 64K DRAM BOARD 

# Mucking around in memory? Seeking space? Look no further, here's a bounty (no connection with those distracting TV ads) of bits, rapacious in real-estate, for your 6502 or 6800 system to gorge itself on. Design and development by Bob Campbell. 

Most microcomputer users find out fairly quickly that there is no such thing as too much memory. But even today with memory as cheap as it is, many systems are on sale with less, often considerably less than the 64 K that most eight-bit microprocessors are capable of addressing. The independent suppliers are usually very quick to-provide units to fill this gap, but one system not well covered in this respect is the Tangerine Micron/ Microtan 65. Until recently, there was only the TAN RAM, but now there is the CMOS alternative. However, despite advantages in power consumption and battery back-up, the CMOS unit, like the TANRAM, is large and fairly expensive. More than one board is required to provide the maximum possible memory. The approach here is to use the highest density dynamic RAM chips readily available and allow the user to access all of it except where it would clash with essential EPROM, I/O or CPU board RAM. This leads to an extremely flexible and cost ef-fective system. Although specifically designed for the Microtan 65 computer together with either a disc system or TUG's Eprom Storage Card (the MOS Disc concept) the design retains enough flexibility to accommodate almost any desired configuration of computer and operating system, the only prerequisite is a 6502 or 6800 CPU .

## Design

The board uses the latest 64 K by 1 bit dynamic RAM chips, TMS 4164-15. These are decoded into 641 K blocks, with all but four of the blocks used in its standard configuration. Making almost $61 / 4 \%$ of the RAM effectively redundant may at first sight seem a little extravagant, however even allowing for this the cost per $K$ is less than $£ 1.00$. If one adds the other savings on hardware, sockets, power supply requirements board space etc., the

64 k chip route stands out above all the other alternatives.

The heart of the system is the 74LS608 memory cycle-controller (MCC). This chip generates all the signals the RAM requires to perform the two types of cycles necessary for proper operation. The MCC generates these signals from the CPU's clocks 01 and 02 together with the decoded signal RE, RAM enable. It is important not to confuse this signal with the Tanbus signal RAME. The only signals used from the bus are the address and data lines together with R/W, 01 and 02 and because of this and the use of a PROM address decoder, this board is very flexible. in design and easily adapted to suit other systems.

## Dynamic RAMs

The two great advantages of dynamic RAM are its extremely low power consumption and its packing density. This is achieved by the design of the actual memory element which is in fact a very small capacitor. The logic level stored being defined by the presence or
absence of a charge on that capacitor. Because all capacitors have a finite leakage, the charge on the capacitors must be periodically topped up. This procedure is called refreshing and is accomplished by performing what is known as a RAS only refresh cycle.

This RAS only refresh cycle consists of first setting up an eight bit address at the input latches and strobing RAS low, while maintaining CAS high. The complete chip is refreshed when all 256 row addresses have been treated similarly. Data retention is assured if all these 256 cycles are completed at least once every 4 msec .

Apart from the necessity to refresh every 4 msec there is one other penalty to pay for the 16 pin packing density and that is the multiplexed address bus. Figure 1 shows the internal architecture of the 4164.

To address every memory element within the IC, 16 address bits must be applied; These are separated into the row address and the column - address, each latched onto the multiplexed address bus


Fig. 1 Internal architecture of the TMS4164 DRAMs used in the project.


Fig. 2 Processor and memory cycle controller timing.
upon the appropriate signal RAS or CAS.
In full, the memory cycle consists of five stages. Firstly the row address pins and RAS pulled low. Then the address multiplexers are switched placing the other eight bits, the column address, onto the address pins and CAS pulsed low. This last operation enables the chip and, depending on the status of the R/W line, enables the input or output buffers, thus completing a read or write cycle.
There are two other possible types of cycle, the page mode read/write and the read modify write cycles. However since neither of these apply to the 6502 or 6800 type of processor it is not necessary to consider them further here.
It is important to note that the 6502 operates in what is known as the early write cycle where the R/W line is set up long before CAS goes low. This enables the data in ( D ) and data out (Q) pins to be connected together and thus have a common data bus.

Obviously the sequence and timing of the two cycles, refresh and memory, is extremely important. The RAS only refresh cycle is particularly significant for two reasons: firstly, it is necessary to perform it regularly (256 times every 4 msec ), and secondly, it is effectively a dead cycle, when the CPU cannot access memory.
Refresh cycles can be carried out in either burst mode or hidden transparent mode. Burst refresh is a technique where all the memory elements are refreshed consecutively whilst the processor is held in a wait or halted state. This dead time is called the refresh overhead, which, more accurately, is defined as the ratio of the time taken to refresh all the memory elements and the maximum refresh interval. In well-designed systems with the 4 msec 64 K rams this overhead can be as low as $2 \%$. As the circuitry needed to maintain this type of refresh system is complex it is not commonly used outside the realms of very fast microcomputers, minis and mainframe systems.

The other technique, hidden refresh, is the more commonly used. This technique relies upon the fact that the CPU will always have a period within any instruction or machine cycle when it will not access the system bus, and one refresh cycle can be accomplished during this period. Thus after a maximum of 256 instruction cycles all the memory elements will have been serviced. This technique has the great advantage of a zero refresh overhead rate and is totally transparent to the CPU and thus the user.
In this design the two cycles, refresh and memory, are sequenced by the main CPU clocks 01 and 02 . While 01 is high, the CPU sets up the R/W and address lines, the rising edge of 02 signifying a valid memory address. This edge of 02 is normally used to enable the address and data buffers. Thus while 01 is high, the CPU is normally isolated from the system bus, and the refresh cycle can be accomplished during this period. In addition by using 01 to clock the eight bit refresh row address counter all 256 row addresses can be refreshed sequentially. Figure 3 shows exactly the relationship and timing of these events.

## PROM Program Design

The memory map of the RAM board is controlled directly by the TBP24S10 PROM, which acts as a complex address decoder. Before programming the PROM, the desired memory map must be established. The minimum requirement for most systems will be the system monitor, the I/0 area and unless there is a serial VDU as the screen, some screen memory. Some systems use a relocatable area of memory for the screen RAM, the video controller accessing the system bus directly. If the target system is of this type then no provision should be made for the screen RAM in the PROM program. Remember the overriding factor when designing the memory map is that there must not be two components within the system which have the same address. Taking the standard configuration of the Microtan as our worked example, the minimum memory map is as shown in Fig 4.
Once you've determined the memory map(s) required, the upper six address lines should be written out bit fashion (bit by bit ... ?). Each bit corresponds to a PROM address bit; however because of the PCB board layout, the one-to-one

Fig. 3 Memory timing for various operations and approximate timing round the MCC.

respondance is not in numerical order.
In addition, by using the two extra PROM address lines A7 and A8, there is the facility to have up to four programs and therefore four memory maps resident on the board at one time, selectable by means of the DIL switch SW1. Using the two tables 1 and 2 it is possible to calculate all the PROM addresses which are required to be 'blown'.

Remember that PROMs are not erasable, once a memory location is altered from the "all 1's" condition, it cannot be reversed. There is however an escape route if a mistake is, made during programming. The program is created by blowing only the operative bits within the data word from a 1 to a O.In this design, only one of the four bits available is used (bit 4). If an error is made during programming, then it is possible to use an alternative bit by breaking the PCB track at pin 9 IC15, installing a link to either pin 10, 11 or 12 (bits 1-3 inc.) and reprogramming the PROM using the appropriate data word. (Alternatively, this would make it possible to hold a total of 16 memory maps in the PROM).

It is beyond the scope of this article to describe the methods for actually programming the PROM, suffice to say that the amount of programming by nature of it's use, is small, so it would be feasible to use the switchbox type of programmer.

## Construction and Setting Up

The construction of the board is very straightforward, particularly if the PCB design presented here is followed exactly: there are, after all, only 18 ICs. The PCB is a double sided design but to keep costs down it doesn't use platedthrough holes. To make the necessary interconnections, track pins or short lengths of wire must be soldered between the two in the positions marked on the overlay diagram with a black dot. These pins must be soldered in first,

| AREA | HEX ADD | SIZE |
| :---: | :---: | ---: |
| A)TANBUG | FFFF | 2 K |
| RAM | F8OO |  |
|  | F7FF | 14 K |
| B) I/O | CO00 | 1 K |
|  | BFF |  |
| RAM | BCOO |  |
|  | BBFF | 46 K |
| C) CPU BOARD | 0400 | 1 K |
| RAM | $03 F F$ | 1 |

Fig. 4 Minimum memory map for the Microtan.

## PROJECT



## PARTS LIST




Fig. 5 Circuit diagram of the complete project.


Power lines \& decoupling capacitors. 1 u 0 all tantalum. 10 u tantalum or low leakage solid electrolytic.
prior to any other components, as there are some beneath the DIL sockets; । advise checking the continuity of each one thoroughly, as mistakes are difficult to rectify later. The remainder of the soldered components can be assembled in almost any order, but I've found that it pays to be systematic and to follow a list, checking off each component as it is soldered in.
All the usual checks should be carried out before the ICs are in-serted into their sockets. Particular attention should be given to avoiding solder bridges in the daisy chained RAM area of the board.
It is useful to insert the chips in three stages and perform some functional checks on the system at each stage. The first of these stages is to insert the PROM and all the TTL, with the exception of the 74LS608
(IC16) and the 74 LS245 data bus buffer (IC14). Now powering up the board on the bus can be performed with all the Tanex RAM and EPROM still resident without the risk of any memory conflict occurring. This procedure will allow you to check the following items with the system running.
A dual beam oscilloscope is really desirable particularly if you have
deviated from the timing component values for any reason. However it should be possible if you don't have access to a oscilloscope to use a good logic probe to check that all the appropriate signals are present.

The most relevant signals to check first are 01 and 02 and their complements 01, 02, RE and DBE should be active only when a valid address within your programmed memory map is accessed. Next check that the two address buffers, IC2 and IC11, are switching correctly

| SYSTEM ADDRESS |  |  |  |  |  |  |  |  |  |  |  | HEX ADD. | COMMENTS |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| A15 | A14 | A13 | A12 | A11 | A10 |  |  |  |  |  |  |  |  |
| 1 | 1 | 1 | 1 | 1 | 1 | FFFF | TANBUG |  |  |  |  |  |  |
| 1 | 1 | 1 | 1 | 1 | 0 | F800 |  |  |  |  |  |  |  |
| 1 | 0 | 1 | 1 | 1 | 1 | BFFF | I/O |  |  |  |  |  |  |
| 1 | 0 | 1 | 1 | 1 | 1 | BC00 |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 | 0 | 0 | $03 F F$ | CPU BOARD RAM |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 | 0 | 0 | 0000 |  |  |  |  |  |  |  |

Table 1 Revised system memory map.

Table 2. Programming sheet for the PROM.

| 64K DYNAMIC RAM BOARD PROM PROGRAMMING SHEET ... OF ... 4 |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYTEM ADDRESS PROM ADDRESS | SW1 | SW2 | 11 | 10 | 13 | 14 | 15 | 12 | HEX PROM ADD |
|  | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | BLOW TO 07 |
|  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
|  |  | 0 | 1 | 1 | 1 | 1 |  |  | 3 F |
|  | 0 | 0 | 1 | 0 | 1 | 1 |  | 1 | 2 F |
|  | 0 | 0 | 1 | 1 | 1 | 0 | 1 |  | 3B |

exactly $180^{\circ}$ out of phase with each other, and that the refresh address counter IC1 is functioning correctly as an eight-bit counter. The final check at this stage is to measure the pulse delay and shaper circuits formed by the diode/resistor networks and IC17. The three signals RAS cycle start (RCS), memory cycle start (MCS) and refresh (RFSH) should all correspond to the timing diagram in Figure 3. Any deviation should be adjusted by altering the value of the capacitor and/or resistor within the relevant RC network. However if the stated tolerances of the components are adhered to there should be no problems.
Having completed all the checks and adjustments so far the next stage is to insert the 74LS608 memory cycle controller, which should produce the necessary signals RAS, CAS, MUX and R/ W. These four main signals should be checked against the timing diagrams in Figures 2 and 3 . The important factors are the relationships between cycle start, CS, and RAS, MUX, CAS sequence and the RAS refresh cycle. The row address hold time RAH, CAS low and the precharge time are the major controlling times and are all programmable via the three RC networks on the 74LS608. Under standard conditions with the 750 KHz Microtan system clock these times have quite a large latitude. However with faster clock rates the times become proportionally more critical. All these times can be calculated from the memory data sheets.
One fault which may occur at this point has the symptoms RAS permanently low, CAS, MUX and R/W permanently high. If this situation exists try shorting very briefly pin 12 to ground. If the controller then starts to function correctly then the 74LS608 is at fault. I understand from Texas that on a number of the older batches of chips there is a fault with the power-on-reset circuit, newer batches, I am assured, are all O.K.
Having checked that all the relevant signals are present at the RAM chip sockets, the RAM chips themselves can now be inserted. Power down first. These are very static sensitive so take all the usual precautions, they are also upside down in relation to the other ICs on the board.

Be warned that if they are inserted with pin 1 to the upper edge of the board they will be irrevocably damaged, and at $£ 4.00$ each a mistake could be very expensive. Finally insert the data buffer IC13. With construction and testing completed there is still one task to finish before the board is inserted back into the rack and powered up. Remove all Tanex RAM and EPROM, and all other memory map conflicts, for example the hires graphics board, failure to do this will probably destroy ALL the memory components in the system.

After powering up the board in the now "minimised" system, unless you've chosen to create a memory map option which retains the Tanex EPROM your system will be running in Tanbug or TUG bug. The quickest way to check the RAM from here is to boot up Basic and XBUG from disc or ESC and let it do the check. 47103 BYTES FREE should appear as the message header. Note some difficulties may be experienced because the F7F7 error jump will not exist immediately. This will show up only if an error occurs during the boot up procedure e.g. miss keying; simply RESET and start again to recover.

Assuming this initial check appears to be OK then a more comprehensive memory test routine should be performed; the one published in the November 1981 issue of Computing. Today is most suitable. However it should be noted that these types of test do not pick out the periodic bit drop out and only extensive usage in BASIC or similar will show up this problem.

## Other Systems

The board relies only upon signals derived directly from the CPU 01, 02, R/W and the address and data buses. Since all these signals will be present in any 6502-6800 system, conversion is. relatively simple.
The only component that needs to be altered in anyway is the PROM which does all the decoding. The essential considerations are those concerning the design of the memory map and, in particular, possible address conflicts. Remember no two components, be they RAM or I/O should have the same address! A suggestion for those with a Microtan but no discs or ESC is to leave the XBUG EPROM resident (FOOOF7FF) and us the tape routines instead.

As so much detail has been given in the general section, this 'How It Works' is going to be fairly brief. During 01 high the main bus buffers IC11 and IC13 are disabled, removing the RAM from the system bus. The refresh row address counter IC1 is connected directly to the RAM ICs (IC3-10) via the enabled buffer IC2. The rising edge of 01 is first buffered by two OR gates and then, via the pulse generator network D1, C1, R1, IC17, it applies a pulse to the REFRESH ENABLE pin (14) of the memory cycle controller IC16. The same rising edge is delayed by D2, C2, R2, IC17, before reaching the CYCLE START pin 13 of IC16. This delay is necessary to satisfy the refresh hold time of the memory cycle controller, and must be maintained at 20 ns minimum. The MCC then responds by pulsing RAS low for a period of time determined by the RC network at pin 12, the row address hold time. The rising edge of RAS is the end of the refresh cycle.

The memory cycle starts with the rising edge of 02 (falling edge of 01) at which point the address bus buffer is enabled directly by 02 and assuming the address is within the memory map, the PROM output 04 is already high. This output combned with 02 produces via IC18 two signals DBE and RE.

DBE enables the data buffer IC13; RE delayed via $03, \mathrm{C} 1, \mathrm{R} 3, \mathrm{IC} 17$ is fed to the CYCLE START input of IC16 the memory cycle controller. This last event causes the MCC to start the actual memory access cycle. The RAS output (pin 7) goes low then, after the programmed RAH time, the R'W line is allowed to pass through and the MUX output then goes low switching over the address multiplexers IC12 and IC14 to the column address. CAS then goes low for a period of time CAS LO. All three outputs RAS, CAS, MUX then go high. This point should coincide with the falling edge of 02 when the data from or to the RAM is latched by either the CPU or the memory depending on the status of the RW line.

The next refresh cycle then occurs on the rising edge of 01 and so the system carries on until the power is removed.

Those who design their own PCBs should take care to heed the memory manufacturer's recommendations on decoupling and PCB layout around those chips. Particular attention should be given to the ground and power supply lines, which effectively surround each chip; the arrangement of interlocking fingers on the typical breadboard is definitely out. Similarly the decoupling of the TTL chips should be comprehensive enough to avoid too much power supply noise, a major culprit of periodic bit drop out. Lastly, the 74LS608 MCC gets hot, but since the lead-frame is directly coupled with both the substrate and the ground pin, a large area of copper around pin 8 should alleviate the problem and improve reliability. With regards to systems employing faster clock rates than 1 MHz , as long as, the RAH, PRECHARGE CAS low times and the refresh hold time for the MCC are satisfied (calculating them from the manufacturer's data sheets), no significant problems should occur.


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# READ/WRITE 

## Switch Troubles

Dear Sir,
I have recently had an unfortunate incident with an EPROM programmer, in which two PIRs and a 7805 regulator were destroyed. The incident happened when throwing a switch (which swapped a certain supply line between 25 V and 5 V ). The result was that the programmer went dead, along with the 5 V power supply and the two PIR's. (The 25 V supply was not affected as it was simply two car batteries in series.) The cause was simple, when the switch was half way across when switching over, it joined the 25 V and the 5 V supplies with the aforementioned results.

To be honest I now consider myself lucky that the 5 V power supply was only supplying the programmer, if it supplied the rest of the computer as well then I have no doubts. whatsoever that I would be left with a PCB of fried chips of the silicon sort of course.

To get to the point, I am now very wary about what switch I use for such purposes, and I would advise that others watch out for these type of switches, which should not really be sold.

Yours faithfully,

## R. P. D. Mallett,

Sandwich, Kent
P.S: If you don't believe that a firm would make such a switch then try out the enclosed one. (You can keep it!) P.P.S: Thanks for an excellent magazine!

This reader has demonstrated all too effectively that it's important to distinguish between make-before-break and break before-make types of switches! For instance, so far as we are aware, all toggle switches are break-before-make, and a large proportion (but not all) slider switches are make-before-break. In fact, it was a slider switch that was sent to us by the above correspondent.

## Induction Loops <br> Dear Sir,

I was very impressed by the excellence of the article on 'Inductance Loops' by Vivian Capel in the February 7983 issue of Electronics Today. It is a very clear exposition of the way to design an induction loop for hearing-aid users and to decide on the amplifier and transformers required for most systems.

As manufacturers of every sort of audio transformer for more than 40 years we have been approached on many occasions to give advice on inductor installation, particularly in churches, where frequently there is a limited budget and the volunteer from the congregation who undertakes the work is generally non-technical. In future we propose to refer him to Mr Vivian Capel's article and to co-operate by supplying the most reasonably priced transformers for the project. These can be specially designed without additional cost to fit in with the usual PA system amplifier already installed or separate amplifier if desired. The transformer audio outputs we have encountered within the last year or so are mostly between 20 and 700 watts, although last year in a large theatre up north, we supplied four 700 watt transformers which were used presumably for the stall, circles and gallery areas.
Inductor loops are not new although in connection with deaf aids they have come into prominence of recent years. In about 1934 - nearly 50 years ago- the following pioneering experiments were carried out by the undersigned who was building a new house at the time. It was decided for the purpose of listening to radio to install a continuous twin wire cable behind the wainscottin around every room in the house with sockets provided so that a loudspeaker could be plugged in anywhere and this still exists. Whilst working on inductor devices for HM Services at that time, it occurred to me that by putting my twin wires in parallel and feeding the loops in the rooms from my amplifier with two LS5 valves for output, I was creating an audio magnetic field everywhere. I then took various annealed mumetal rods about $1 / 4$ " diameter and tried them on different search coils which were connected to my very sensitive S.G. Brown A type adjustable gap earphones normally used for my ham radio reception
(my call sign then, and now was G205). Incidentally these phones had conical diaphragms like miniature moving coil speakers which were operated by a cantilever reed.

I found that by wearing the phones connected to the search coil I could sit in any room without being connected by wires and listen to the radio programs. It did occur to me that by having loops upstairs and downstairs I had a Helmholtz coil system which tended to give excellent magnetic field distribution, particularly in the middle of the room. (We use much smaller Helmholtz coils nowadays to determine the screening effect of mumet I can by taking voltages picked up by a search coil in air and then enclosed in the can).

All my experiments were published by me in an article in the Wireless World in the mid 1930's. I remember suggesting that the pick up device in cinemas and theaters could be in the form of a mumetal walking stick or umbrella stick fitted with a search coil, and for the ladies (shades of Queen Victoria) - a mumetal handle with search coil on lorgnette spectacles.

I do not claim to be the originator of induction loops but my amateur pioneering experiments were certainly carried out arid published more than 45 years ago.

Yours truly,
Dr G. A. V. Sowter,
Consultant to Sowter Transformers PO Box 36, Ipswich IP1 2EG

## Holophony

Dear E.T.I.
I was interested to read about Mr Zuccarelli and his Holophony in July ETI, and thought you might be interested to hear of my own experiments with the idea.
About 15 years ago, having built a stereo tape recorder, I then got to wondering why two microphones did not give a very clear recording when two ears were obviously adequate for us. The obvious difference seemed to be the ears.

I then conducted experiments at the dead of night under the bedclothes (not having an anechoic chamber!), trying to decide in the dark where the tick of a pocket watch appeared to come from. I discovered that the various lobes on the outer ear give us a means of judging direction of sound. By pressing down and 'blanking off' different bits of the ear I discovered which bit did which - those at the
top tell us about sound above the head, and the bits at the back are to do with front-back direction, and so on.

I then modeled two Plasticine ears and fitted them to omni-directional mic inserts. Fitted to a paper-mache head (filled with cloth , to damp self resonance), the results were quite spectacular - especially using headphones.

I enlisted the help of a few school friends and found that the 'head' gave quite repeatable results. We found we had to put felt 'hair' on the back to aid front-back discrimination.

There seemed to be some variation in perceived results between different people - which seemed to be due to variations in the size of ear, and different hair lengths.

When I was at university, I excitedly announced my findings to my tutor - who was at one time an accomplished recording engineer - He Said: "Oh yes, they did all that research in the '30's at Bell Telephone Labs!" So there I rather left it - but I am sure the principle has possibilities, although there will always be greater or lesser variations between the dimensions of the head and ears used to record and the head and ears which receive the recording, and therefore
some subjective variation of results. As to the idea being new - it seems that truly nothing is.

Yours sincerely
Richard Buswell
Buswell Machine Electronics Skelmersdale

We're now convinced that there is something more to the holophonic technique than we thought when we published Vivian Capel's report. This is due to Dave Bradshaw having had the opportunity of visiting Hugo Zuccarelli and hearing holophonic sound at first hand, through loudspeakers as well as headphones. We're hoping to do a full report on this at some stage in the future, time and space permitting, but in the meanwhile ETI readers might like to try explaining the results of the following experiment, that you can do for yourselves. It takes two people, one of whom we'll call the experimenter, and the other is the subject.

The subject should shut his or her eyes, and firmly jam a finger in one ear, so that all sound is excluded (so far as possible). The experimenter should take a box of matches (or a ring of keys) and shake it, moving it around the subject's head. The subject should be asked to point in the direction from which the sound is coming. Most people with normal hearing (provided their ears aren't blocked up with wax!) should be able to point approximately in the direction of the sound, even when it is on the other side of the head from the open ear. To make the conditions more stringent, you could start shaking the matches from this side, so that there is no possibility of the brain having a reference sound with which to refer the (ear lobe modified) sound to.
If any of our readers have access to an anechoic chamber we'd be most interested in hearing of the results of doing the above experiment in it. We'd also like to hear of anyone who has access to a conventional dummy head recording (Sennheiser did have such a recording, but their UK office was unable to help us).

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## Get moving with these new developments in UK Robotics

## - advanced electrohydraulic designs for education, industry and now available to the home constructor.

Hebot II is a turtle-type robot which takes programming Out of the two dimensional world of the VDU into the real three dimensional world Given a DC supply of $9-15 \mathrm{~V}$ it can perform a bewildering number of moves under computer control - forwards, backwards, left and right - with each wheel independently controlled it has blinking eyes. bleeps with a choice of two tones and has a solenoid operated pen to chart its progress Touch sensors coupled to ts shell return data, about its environment. to the computer for it to calculate evasive or exploratory action. Hebot II connects directly to an I/O port or alternatively with the universal interface board to the expansion bus of a $2 \times 81$ or other computer.


Up to the nano-second hard, firm and softwar Jevelopments embodied in a complete system. ega Hertz 16 bit CPU; 64K upwardly compatibl
DRAM; separate 16 K video DRAM and 24 K TI Powe Basic with overwrite. Supports up to four Disc drives o mixed type with 16 serial I/O ports. Programmable Baud rate and comprehensive $E$ Bus interface designed to support real world applications.
Very high resolution graphics gives 3D simulation in 16 colours on 36 prioritised planes of user definable characters. Software FORTH coming includes this trendy language along \& h NOS C/PM.

- fardware components available separately with details in Nov, Dec, and Jan issues of ETI. Software features include; Real time clock, full renumber command, buffered I/O to free machine whilst

Robotic experience is becoming as essential a subject as co puting MICROGRASP provides the lowest cost means of acquiring that experience but despite its ultra low price the robot has considerable versatility There are 5 axes each using a servo motor and there is feedback from each of the arm movements. Control is by any computer with an expansion bus - the ZX81 being particularly suitable Servoing is achieved with hardware on the interface board to keep programming simple and the robot is operated under BASIC commands with no computer specific software required. The interface board is memory mapped using only 64 bytes at any of 1024 switch selectable locations.
MICROGRASP robot kit with power supply Universal computer interface board kit 23 way edge connector
2X81 peripheral/RAM Pack splitter board
$£ 125.00$
$£ 48.50$ $£ 48.50$ £3.00 MICROGRASP, INTERFACE BOARD AND ZX81
printing, call to machine code routines, hexadecimal support and userfriendly textual error trapping messages.

If computers interest you then the Cortex will expand your understanding infinitely more than off the shelf machines. Use it in business, education, research or just play with the incredible graphics capability. At Powertran we are using these machines in conventional roles, in product control and R \& D. We shall coordinate the Cortex user group and distribute software for the TMS 9995 CPU. Complete 16 bit 64K computer kit £295.00 + VAT Complete 16 bit 64 K computer ready built $£ 395.00$ +VAT.
op of the range is the Genesis P102 which has dual speed control, continuous servo operation and double acting c. nders for increased torque on the wrist and arm rotation ons. The microprocessor based control system has addinal memory, position interrogation via the RS232C interace increasing the versatility of computer control and inputs are provided for machine tool interfacing.
e a s system READY BUILT $\quad £ 1950.00$ (Electronics Today International December issue on CORTEX


Example prices and specifications

Genesis S101
Base: $19.5 \times 11 \times 75$ Arm lift: $66^{\prime \prime}$

## Weight: 29 Kg

4 axis model in kit form £390 5 axis model in kit form 5 axis model Ready Built
Genesis P101
Genesis P10
Base: $19.5^{\prime \prime} \times$
Lifting capacity. $\times 7.5$
Arm lengths between axte Weight 34 Kg
4 axis model in kit form $£ 495$ 6 axis mode in kit form $£ 595$ 6 axis model Ready Bull Complete Systems as shown in Photograph above
Genesis S101
4 axis system in kit form $£ 635.50$ 5 axis system in kit form $£ 695.00$ 5 axis system Ready Built $£ 1355$ Genesis P101
4 axis system in kit form $£ 742.00$ 6 axis system in kit form $£ 852.00$ 6 axis system Ready Built $£ 1525$ All prices exclusive of VAT

GENESIS P102 PROCESSOR BOX, HAND HELD CONTROLLER AND CORTEX COMPUTER

With prices starting below $£ 1.000$ the Genesis range of general purpose robots provide a first rate introduction to robotics for both education and industry Each has a self-contained hydraulic power source. which enables loads of several pounds to be smoothly handled. The system operated from a single phase 240 or 120 V AC supply or a 12 VDC supply. The machine can be supplied with up to 6 axes each of which is fully independent but capable of simultaneous operation. Position control is achieved by means of a closed-loop feedback system based around a dedicated microprocessor. Movement sequences can be entered, stored and replayed by use of a hand held controller. alternatıvely the systems can also be interfaced to an external computer via a standard RS 232C link.


GENESIS S101 AND GENESIS P101 WITH PROCESSOR BOXES AND HAND-HELD CONTROLLERS

# MAME ALI THE PIGHT connections 

 with a MAPLN MODEM KITExchange programs with friends, leave or read messages from the various Billboard services. talk to computer bureaux, or place orders and check stock levels on Maplin's Cashtel service. A Maplin Modem will bring a whole new world to your computer and vastly increase its potential.
Now you can exchange data with any other computer using a 300 baud European standard (CCITT) modem and because the Maplin Modem uses this standard, you could talk to any one of tens of thousands of existing users.
Some computers need an interface and we have kits for the ZX81, VIC20/Commodore 64, Dragon and shortly Spectrum and Atari whilst the BBC needs only a short program which is listed in Project; Book 8. A Maplin Modem will add a new dimension to your hobby.
Order As LW99H (Modem Kit) excluding case. Price £39.95.
YK62S (Modem Case). Price $£ 9.95$
Full construction details in Projects Book 5.

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In Book 2 (XA02C) Home Security System : Train Controller for 14 trains on one circuit : Stopwatch with multiple modes : Miles-per-Gallon Meter.
In Book 3 (XA03D) ZX81 Keyboard with electronics : Stereo 25W MOSFET Amplifier : Doppler Radar Intruder Detector : Remote Control for Train Controller.
In Book 4 (XAO4E) Telephone Exchange for 16 extensions : Frequency Counter 10 Hz to 600 MHz : Ultrasonic Intruder Detector : $1 / 0$ Port for ZX81 Car Burglar Alarm: Remote Control for 25W Stereo Amplifier.

## LEARN ROBOTICS

## Great Projects <br> From E\&MM

Our new book "Best of E\&MM Projects Vol. 1" brings together 21 fascinating and novel projects from E\&MM's first year.

Projects include Harmony Generator, Guitar Tuner, Hexadrum. Syntom, Auto Swell, Partylite, Car Aerial Booster, MOSFET Amp and other musical, hi-fi and car projects.

Order As XH61R. Price $£ 1.00$.


[^0]:    Nothing to cause any problems here. PCB through PCB service page, case a la carte (to choice), semiconductors all readily available -when was the last time we published such a trouble-free project?

[^1]:    Not much to say here really. The LED, switch and resistor combination on four inputs to each IC provides a low when the switch is open and a high when it is closed. Also when the switch is closed the LED will light showing that a high has been selected for that channel.

    When the logic input pattern on the input pins matches that on the switches the output from each IC will change state and thus trigger a scope connected to the final output. The outputs from one IC will directly drive the cascade inputs of another and so extend the width of the comparison. The inputs from the test circuit are provided with pull up resistors so any unused input will appear as a high and this must be set on the cor-responding switch. Cl and C2 are pre-sent to decouple the supply rails. R1 is a pull up for the "=" cascade input.

