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Peter Green: Deputy Editor
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All that's new in electronics, at least for the last month or so.

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## AUDIO BUYING GUIDE

The special audio buying guide will tell you which system to buy to suit your pocket. There will be good, sensible advice on all aspects of system choice and upgrading, but none of the 'buy a Lynotrio Cystemdek for $£ 10,000$ and listen to it through Granny's hearing aid until you've paid off the mortgage' variety. Incidentally, we've inserted the CENSORED stickers for your own good, to prevent you from going out and buying any gear until you've read the guide (and bought next month's ETI, of course).


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# NEWS:NEWS:NEWS:NEWS:NEWS:NEWS:NEWS 

# DIG E ST 

## $£ 1000$ Reward

W
ell, that's got your attention - now here's the problem. It would seem that some light-fingered gentlemen have been at work in deepest Surrey. Aura Sounds Lid, sole importer of Wersi organs, pianos and accessories in the UK, suffered a burglary three days ago (that's Saturday 5th February as I write this) and several expensive items were stolen. Amongst the lost instruments was a computercontrolled rhythm unit, known in the trade as a Wersimatic CX 1 . The director of Aura, Mr. Arthur Griffiths says "The thief couldn't have stolen a more easily traceable item! This CX 1 is the only model of its type in the UK at the moment. Indeed, it is virtually a prototype and there are only 10 in existence world-wide. It is absolutely essential that we retrieve this instrument, and we are offering a reward for its recovery. Information leading to the return of the CX 1 and apprehension of the thief (thieves) concerned will carry with it a $£ 1000$ reward". Anyone who thinks they have in-

## A Safe Bet

- Here's another attention-getter for this page-can you stand the excitement? Nike Clark (for it is she) is unique, with a lot to of fer, says the British Safety Council, and that's why they've chosen her to help promote their Action Days. These will be staged to assist industry avoid the disruption of accidents and unnecessary losses by bringing all the latest relevant information, products, expertise and techniques within easy, cost-effective reach of companies all over the country.

The dates are Leeds (13/14 April), Cardiff (22/23 June), Plymouth (14/15 September), Middlesborough (12/13 October) and London (20 May). Anyone wishing some Action should contact Faye Rothwell, British Safety Council, 62/64 Chancellor's Road, London W6 9RS (telephone 01-741 1231 ext. 293)
formation should contact Mr. Griffiths at Aura Sounds Ltd, Royal Oak Centre, Brighton Road, Purley, Surrey (telephone $01-668$ 9733).


## Disc-continued

We continue the mini-floppy disc saga; Sony announced today (January 20th) that 13 leading floppy industry companies, composed of the following disc drive and media manufacturers, have agreed to support a mutually compatible 3.5" floppy disc format: Atari, Athana, BASF Systems Corporation, Fuji Photo Film Co. Ltd, Memorex Corporation, Mediá System Technology, Inc, Shugart Associates, Sony Corporation, TDK, 3M, Verbatim Corporation, Wabash Datatech, Inc and Xidex. "The major technological issues relating to compatibility have been settled," Sony said. "The compatibility will strengthen the
position of the $3.5^{\prime \prime}$ disk with a hard covering as the leading format for a microfloppy industry, as well as reduce costs and expand the potential market through greater second sourcing opportunities." The media itself holds up to 1 megabyte in a double-sided, 135 track per inch version. The media's hard covering protects the user's data, while the precise centring and proven 135 tracks per inch technology contribute to greater reliability by reducing the potential for positioning errors. Once the remaining specifications have been settled, Sony will grant non-exclusive manufacturing licenses to any qualified media manufacturer in order to promote widespread adoption of the standard by manufacturers.

## MegaMania Mania

Having reviewed a fair number . .of games for the January ETI, your intrepid Star Warrior/Deputy Editor had come to the conclusion that high-resolution machines like the Intellivision and Atari 400 rather left the Atari VCS out in the cold. A new game from ActiVision has changed all that, however, because it's so good it's almost worth buying a VCS just for this one cartridge. ActiVision have proved that it's the game design that counts, not the screen resolution. Using only the simplest of shapes they've produced a challenging and absorbing 'space shootout', one which led to the extraordinary sight of eight ASP employees crowded into the ETI workshop one night queueing to play. This is unprecedented, because said employees would normally be quaffing draughts of ale in the local tavern after work.

What does MegaMania involve? Each attack cycle consists of eight waves of Invader-type aliens with loony shapes - these are hamburgers, cookies, bugs, radial tyres, diamonds, steam irons, bow ties (!) and dice (personally I think they look more like lumps of cheese). There are no bases to hide under, which is tricky because some of the bad dies move from left to right, others move down the screen, and some do both. The screen wraps round from top to bottom and left to right so if you miss any they come back for another shot, but it's very easy to get trapped unless you can figure out the patterns and the best tactics for each
wave. The patterns of movement are, naturally, different for every cycle. Chris 'Fingers' Palmer of Personal Computing Today holds the office record at present with 216, 530 on option 1 , difficulty $b$, a pretty stiff target to beat. MegaMania costs £29.95 and, even though it's only February, gets our vote as game of the year. Go out and buy one. Now.

## Microtutor

We have received a letter - from Tangerine Computer Systems Ltd, designers of the Microtutor project that was featured in the August, September and October issues of ETI last year. In it they state that they have had many problems with it, paramount being their inability to obtain the necessary components. As a result of this they have taken the decision to withdraw the project from the market. Both we and Tangerine would like to offer our apologies to any readers who may have been inconvenienced by the situation.

## Cross Words

0ops! we forgot to give the winners of Crossword No. 5. They were John R. Baldwin of Dorset, A. R. Moss of Hampshire and Stuart McWilliam of West Yorks. Answers:
ACROSS: 1 Chassis. 4 All Pass. 10 Ambient. 11 Dry Cell. 12 PNP. 16 Mid Range. 17 Nanovolt. 18 SME. 19 Monitors. 21 Low Power. 23 Function, 26 Anodised. 29 Owl. able. 38 Voltaic. 39 P C Board 40 Hous ing. DOWN: 2 Hybrid. 3 IIT. 5 Hous Stereo. 7 Maximum. 8 Pan. 9 Flutter. 12 Press. 13 Panel. 14 Watt. 15 Loop. 20 NPN. 22 WPS. 23 Faraday. 24 Tone. 25 Notch. 26 Album. 27 Dial, 28 DIN lack. 31 Static. 33 RF Abin. 35 USB. 37 EOR. 38 VCO.


## NEWS:NEWS:NEWS:NEWS:NEWS:NEWS:NEWS

## Quartz Into Pint Pot?

The world's first analogue quartz chronograph wristwatch has been introduced by Seiko. The biggest and most experienced watch house worldwide, Seiko is renowned for its innovative achievements having many world firsts to its credit, including the recent introduction of the first television watch (see ETI Digest, September 82). Until now quartz chronographs with digital readouts have been commonplace but the introduction of the Seiko Analogue Quartz Chronograph is the result of many years of research and development. It is an achievement which is thought to be far in advance of any other watch house. Four independent micro-step motors have been successfully miniaturized into a small wristwatch module and it is this fact that has made possible the development of this new analogue quartz chronograph. Micro technlogy has also played an important factor in terms of design; the watch itself is much thinner than conventional chronographs with mechanical movements.

Other impressive technical features of this new Seiko model include a chronograph with a 5/100th second capability, a split time measurement facility, the ability to record two consecutive finishes, a tachymeter, and a remaining time indicator as well as a tally counter. All three chronograph hands go round once for demonstration purposes, by simply depressing the buttons. Four different models, one of which is a Sports 100 watch (water resistant to 100 metres), will be available in the shops in May. Each model has a stainless steel case and bracelet and the range of watches offers a choice of different colour dials and prices vary between $£ 110.00$ and $£ 140.00$ each retail.


## Shorts

- Anyone who fancies going back to school this summer is invited to attend the 1983 Electronic Systems Summer School at the University of Essex. Two courses are offered, 'Feedback and Communication Systems' and 'Digital and Computer Systems'. The school will run from Sunday evening, 10th July to Friday afternon, 15th July, and teachers wishing to obtain further detials of the courses should contact Mrs J. Mead, Dept. of Electrical Engineering Science, University of Essex, Colchester (telephone 0206862286 ext. 2358).
- Or perhaps you want to find out more about computer based training, in which case you should contact Sue Punch of Mills and Allen Communications Ltd 1-4 Langley Court, Long Acre, London WC2E 9JY (telephone 01-240 1307). They're holding a one-day course on CBT techniques and uses, followed by a twoday workshop on CBT and practical design. Dates are 23rd, 24th and 25th of March and the venue is in Central Londion.
- Can't imagine what's come

over Motorola's PR people: their new development system based on the MC6809 processor, XDOS operating system and BASIC-M compiler has been named the EXORset 100. Nought out of 10 for good taste, gentlemen
- As usual, we've received word of a number of catalogues this month: first off is one from Wavetek Electronics, the test and measurement equipment manufacturers. New products include a VHF frequency synthesiser, a $3.7-7.6 \mathrm{GHz}$ microwave signal generator, and a cross channel spectrum analyser. Free copies of the 210-page catalogue are available from Wavetek's new sales and service office at Tag Lane, Hare Hatch, Reading, Berks. RG10 9LT (telephone 073522 2124).
- OK Industries UK Ltd have produced the second one; it's a new 16-page full colour brochure describing the range of Elrack terminal enclosures, lab racks and computer desks. Lots of the stuff is 19" rack-sized and, although constructed to industrial standards, most:products in the range are suitable for the electronics amateur. OK Indusțries are at Dutton Lane, Eastleigh, Hants SO5 4AA (telephone 0703 610944).
- Finally the F.C. Lane Group hàve their 1982/83 catalogue out. which contains pots, fuses, resistors, ferrites, and a wide range of cohnectors and accessories, plus flat cable. Contact F.C. Lane Electronics Ltd, Slinfold Lodge, Horsham, West Sussex, RH13 7RN (telephone 0403 790661).
© The Blacksburg Group, Inc want to encourage as many radio amateurs and şhortwave listeners as possible to use the newlyassigned 10 MHz ( 30 metre) band. Their Slinky Dipole (good grief!) can do the job but requires new tuning information, which Blacksburg are giving away free to any Slinky Dipole owner. Simply send your name, address, and two International Reply Coupons for your Tuning Chart. The address is PO Box 242, Blacksburg,

Virginia 24060, USA.

- Got nothing booked for May 16-17th this year? Logical Solutions, Inc and Network Conferences are holding a seminar on the design for testability (what an awful word) of LSI/VLSI circuits, including components, subassemblies and systems. Full details from Network Conferences Ltd, Printers Mews, Market Hill, Buckingham, MK18 1JX (telephone 02802 5226).
- Had any wizard wheezes lately? A new book called "The Practical Guide for Pepple with a New Idea"' will help you through the jungle that comprises the modern patent process. It also contains information about marketing your idea effectively, choosing trademarks etc etc. The book iş available for $£ 5.95$ post paid from Laurence Shaw, George House, George Road, Edgbaston, Birmingham B15 1PG.
- Dragon 32 and Tandy TRS-80 colour computer owners will be pleased to hear that a new monthly magazine of USA origins and dealing exclusively with these computers is now available. A sample copy of "Rainbow" can be obtained by sending $£ 1.95$ plus a large 56p SAE to Elkan Electronics, Freepost, 11 Bury New Road, Prestwich, Man chester M25 6LZ (or ring 061-798 $7613-24$ hour service).
- A new company with an $80 \%$ British shareholding reckons that more than $£ 400$ million will be spent on constructing new cable TV networks in Britain by next year. Cable TV Construction Ltd will act as consultants and expects to create jobs for several hundred people.
- If you fancy interfacing your Commodore 64 or VIC 20 to a Centronics printer, Wego Com= puters of 22a High Street, Caterham, Surrey can sell you the necessary interface for your serial port. The device is completely compatible with the other port devices such as disc drives and draws its power from the printer. The cost is $£ 79$ plus VAT and the phone number is 088349235 if you want more information.


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## ZX81 MUSIC BOARD

 There have been a great many commercial and hobbyist designsfor ZX81 peripherals, but we feel this one is something special.
Full software listings will be given to help you use the board and
the price is low. Design and development by M. P. Moore.

Give your space invaders program real 'zapp' - this add-on board enables you to hear those little green monsters being blasted away. Plug in the board, load the software cassette, and with two instructions you have a wide range of on-board sounds for your computer games; or you can copy music for your ZX81 to play, or devise your own sound effects for use in your own programs. You can also mix your own sound effects with the on-board sounds if you wish.

The unit is a sound generator with a fusible-link memory programmed with sounds varying from gunshots to spaceships, and with a basic octave of notes from which a range of seven or more octaves of music is obtained. When
used with the software supplied it will bring ZX81 games to life with startling realism. The board will produce sounds with the basic 1 K ZX81 but its full potential is realised with a 16 K expansion, when the music program can provide a completely new use for those who are wondering what to do with their ZX81 now they have it.

A complete kit of parts is available (see Buylines), which also includes a comprehensive user's manual and software cassette A demonstration cassette containing on-board sounds and music generated by the add-on sound board is available at an all-inclusive price of 95 p. Petron Electronics have been good enough to grant us permission to publish both their PCB design and the complete
software listings, including the PROM hex dump, to satisfy those diehard readers who insist on doing everything themselves. However, given the low price of Petron's kit, which contains all the hardware required plus documentation, we think that this is the best way to go for cost-effectiveness, ease of construction and convenience.

## Construction

All components in the circuit are mounted on a single-sided PCB (see overlay): IC sockets are supplied for all ICs. Two screened leads provide the connection from the PCB to your amplifier; all other connections to the board are made via an edge connector which plugs straight into the back of the ZX81


The ZXB1 music and sound effects board, like most other $\mathbf{Z X}$ peripherals, plugs directly into the computer.


Fig. 1 Component overlay for the ZX81 sound board.
(or 16K RAM pack if used).
First of all solder the six IC sockets and then the six links: some of these are close to each other or to other components and the use of insulated wire is recommended. Now solder resistors R1 and R2 these resistors can be of any value between 1 k 0 and 1 k 8 . Solder the electrolytic capacitors C1 and C2, taking care to mount them the right way round (see overlay), and then capacitors C3 and C4. Finally, carefully insert and solder the edge connector leaving a gap of approximately 7 mm between the connector and the PCB. The pin corresponding to 9 V on the connector is not required and, for safety purposes, has been cut. Now carefully check all your soldered joints, preferably with a magnifying glass, and make sure that there are no bridges across any of the tracks

If the board is to be used with a stereo amplifier, cut the length of screened cable supplied in half and solder the inner cores to one end to the left and right outputs, and connect the outer cores (screen) to the point marked GND. Take care to insulate these wires so that they will
not short across other component leads. If you wish to use the board with a mono amplifier, connect a wire link between the two outputs and to this link connect the inner core of one of end of the screened cable, taking the screen to 0 V and insulating the cable as before. Connect the phono plugs (or one of them if you are using a mono amplifier) to the other end of the screened cable.

Now, carefully checking the orientation of the ICs, insert them into the IC sockets. Note that IC2 and IC6 are mounted in the opposite direction to the other ICs. With your ZX81 switched off, carefully plug the board into the back of the ZX81. If you have a 16 K RAM pack, plug this on first: the sound board will plug onto the back of your RAM pack. Switch on your ZX81 and wait for the inverse K prompt to appear on your screen.

## On-Board Sound Program

This program enables you to include the on-board sounds listed in Table 2 in your own programs. To use these sounds all you have to do is to load the first short program

PARTS LIST

| Resistors (all $\ddagger \mathrm{W}, 5 \%$ ) |  |
| :---: | :---: |
| R1, 2 | 1 k 2 |
| Capacitors |  |
| C1, 2 | 100u 16 V axial electrolytic |
| C3, 4 | 100n polyester |

Semiconductors

| IC1 | AY-3-8910 |
| :--- | :--- |
| IC2 | 741593 |
| IC3 | 74 C 20 |
| IC4 | 74 C 32 |
| IC5 | $74 \mathrm{C02}$ |
| IC6 | TBP28L22N |

Miscellaneous
PCB; edge connector; IC sockets; two off phono plugs; $2 \mathbf{m}$ of screened cable.

## BUYLINES

Petron Electronics supply a full kit of parts for the project. The kit includes the PCB and all components, and comes complete with a comprehensive user's manual and software cassette. The kit price is $£ 24.05$ all inclusive. The board is also available ready-built, together with manual and cassette, for £29.95. A demonstration cassette is available for $95 p$ all inclusive. The manual may be purchased separately for £1.25, refunded upon subsequent purchase of a kit. Petron Electronics may be found at 1 Courtlands Road, Newton Abbot, Devon.
from the software cassette and connect up your amplifier, keeping the volume fairly low. The following program will allow you to review the range of principal on-board sounds available before incorporating them in your own programs.

| 10 | PRINT "SOUND NO.?"' |
| :--- | :--- |
| 20 | INPUT S |
| 30 | POKE 16531,S |
| 40 | RAND USR 16514 |
| 50 | CLS |
| 60 | GOTO 10 |

In order to run this program type GOTO 10. *
The computer will now ask you the number of the sound you wish to hear: SOUND NO. ? As an example, type 153 NEWLINE. The computer will repeat this question after each sound. A continous sound (eg helicopter) must be silenced by typing 0 or another sound number.

In order to use these sounds in your own programs, enter your program without altering line 1 of program " $S$ ". At each point in your program where you require a sound to be generated, you simply include the following program lines:-


Close-up of the prototype board.

## TABLE 1

| TABLE 1 BCI |  |  |
| :---: | :---: | :--- |
| BC1 | BDIR | FUNCTION |
| 0 | 0 | INACTIVE |
| 0 | 1 | WRITE TO PSG |
| 1 | 0 | READ FROM PSG |
| 1 | 1 | LATCH ADDRESS |

EPROM DATA

| 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 00 | 00 | 00 | 00 | 00 | 00 | 1 F | 07 |
| 10 | 10 | 10 | FF | 28 | 09 | 69 | 00 |
| 00 | $3 B$ | 00 | 00 | 10 | FF | 32 | 08 |
| 96 | 02 | C 8 | 02 | 64 | 02 | 0 F | 00 |
| 10 | 10 | 10 | 3 C | 00 | 08 | 00 | 32 |
| 03 | 0 F | 00 | 10 | 10 | 10 | 3 C | 00 |
| 08 | 07 | 10 | 10 | 10 | FF | 05 | 09 |
| 07 | 08 | 10 | 10 | 96 | 03 | 08 | 07 |
| 10 | 00 | 10 | FF | 0 C | 0 F | BE | 00 |
| BE | 00 | BE | 00 | 00 | 38 | 10 | 10 |
| 10 | 00 | 01 | 09 | 5 F | 00 | 5 F | 00 |
| 5 F | 00 | 00 | 38 | 10 | 10 | 10 | 00 |
| 01 | 09 | 2 F | 00 | 2 F | 00 | 2 F | 00 |
| 00 | 38 | 10 | 10 | 10 | 00 | 01 | 09 |
| 17 | 00 | 17 | 00 | 17 | 00 | 00 | 00 |
| 10 | 10 | 10 | 00 | 03 | 09 | 19 | 00 |
| 32 | 00 | 41 | 00 | 1 E | 00 | 0 A | 0 A |
| 0 A | 6 E | 00 | 6 E | 00 | 00 | 00 | 09 |
| 10 | 0 C | 0 F | 10 | 96 | 03 | 08 | 1 F |
| 07 | 10 | 10 | 10 | FF | 64 | 09 | 5 A |
| 01 | 5 A | 01 | 5 A | 01 | 00 | 38 | 0 F |
| 0 F | 0 F | 05 | 01 | 05 | 01 | 05 | 01 |
| 00 | 38 | 10 | 10 | 10 | 00 | 19 | 09 |
| FA | 03 | 00 | 00 | 03 | 05 | 10 | 0 A |
| 10 | FF | 01 | 0 C | AO | 01 | 64 | 01 |
| 96 | 00 | 0 F | 30 | 10 | 10 | 10 | 32 |
| 02 | 09 | FF | 3 F | 10 | 10 | 10 | FF |
| 32 | 08 | 5 C | 0 F | 70 | 0 E | $\mathrm{A0}$ | 0 D |
| DC | 0 C | 28 | 0 C | 28 | 0 C | 68 | $0 B$ |
| D 2 | $0 A$ | 46 | $0 A$ | $9 A$ | 09 | 22 | 09 |
| 22 | 09 | AO | 08 | 28 | 08 | AE | 07 |

## PROGRAM 'S'



POKE 16531, x
RAND USR 16514
where $x$ is the number of the sound required from table 2.

The sound POKEd to 16531 remains the same until changed. Therefore, if you wish to repeat the same sound, there is no need to repeat POKE 16531,x - all you need to do is repeat the line RAND USR 16514.

Fast repetition of single sounds can be used to give a different effect. For example, the following program uses the rifle shot (sound 50) to generate a machine gun sound:

| 70 | POKE 16531,50 |
| :--- | :--- |
| 75 | FOR D 1 TO 40 |
| 80 | RAND USR 16514 |
| 85 | PAUSE 1 |
| 90 | NEXT D |

Now type GOTO 70 and the computer will generate a burst of machine gun fire.

Table 2 gives the principal sounds that may be obtained, but there are many other interesting sounds which you can find by experimenting with other numbers not listed in this table.

## HOW IT WORKS

IC6 is a fusible-link read-only memory (PROM) programmed with the data for all the on-board sounds and a basic octave of notes for music. This memory is accessed through the ports on IC1.

IC1 is a programmable sound generator (PSG), an AY-3-8910 which can be programmed to generate a wide range of sounds. Once data is written to this chip it produces and maintains the sound without continuous CPU maintenance, thus making it ideal for use with computer programs.

The PSG has three analogue outputs: outputs $A$ and $B$ are connected directly together and, via C1, connect to one channel of your amplifier; output $C$ is connected via C2 to the other amplifier channel. The board will, therefore, give a dual image effect when used with a stereo amplifier. If you wish to use a mono amplifier, the analogue output C is connected directly to $A$ and $B$.

IC3 and IC4a are used as an address decoder: the output of IC4a will be logic 0 when address lines A0, A1 and A4-A7 are $1 ; \overline{\mathrm{M} 1}$ must also be logic 1 . IC4b is used to provide a chip select signal for the PSG only when the Input/Output request (IORQ) is at logic 0 . Thus the output of IC4b will be 0 only when a read or write operation on the PSG is to be performed. Whenever the output of IC4b is logic 1, the outputs of IC5c and IC5d will be 0, BC1 aand and BDIR will both be 0 , and the PSG will be in the inactive state: see Table 2. (Since whenever it is deselected the 'inact' signal is sent, it is not necessary for the ZX81 program to send 'inact' to the PSG.)

IC5a and IC5b are used, together with IC5c and IC5d, to provide the necessary combinations of 0 and 1 for BC1 and BDIR. The output of IC4C drives the fusible-link PROM chip select input: this is to minimise the possibility of data bus contention between the PSG and the PROM should PSG port D accidentally be programmed as an output port, since IC4c output will only be 0 during a PSG read cycle.

The maximum clock frequency to the PSG is $\mathbf{2 ~ M H z}$. IC2 is a low power Schottky version of the 7493 counter and is used here to divide the ZX81 clock frequency by 2.
Next month we will conclude this project by giving full listings and explanations of software to play up to 833 chords of music; to devise your own sound effects; and to mix your effects with the on-board sounds.
TABLE 2

| Sound $N$ | Description | Continuous? | Sound $N$ | Description | Continuous? |
| :---: | :--- | :---: | :---: | :--- | :---: |
| 0 | Silence | - | 92 | Mid blip | No |
| 8 | Cannon fire | No | 106 | High blip | No |
| 9 | Pistol shot | No | 204 | Musical blip | No |
| 50 | Rifle shot | No | 57 | Steam engine | Yes |
| 64 | Missile | No | 145 | Steam engine with whistle | Yes |
| 18 | Sonar | Yes | 167 | Train horn lower note | Yes |
| 153 | Explosion | No | 178 | Train horn upper note | No |
| 190 | Helicopter | Yes | 32 | Propellor aeroplane | Yes |
| 28 | Fog horn | Yes | 39 | Jet plane on the ground | Yes |
| 29 | Fog horn | Yes | 134 | Jet plane flying | Yes |
| 21 | Compressor | Yes | 52 | Mechanical hammer | Yes |
| 99 | Waterfall | Yes | 49 | UFO | Yes |
| 101 | Waterfall | Yes | 131 | UFO | Yes |
| 121 | Low bong | No | 213 | UFO | Yes |
| 33 | Mid bong | No | 214 | UFO | No |
| 45 | High bong | No | 231 | UFO | Yes |
| 78 | Low blip | No |  |  |  |



Fig. 2 Complete circuit diagram for the ZX81 sound board.
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# DESIGNERS' NOTEBOOK 

## Who needs to bother winding miles of wire onto a bobbin when high voltages can be generated with some inverters and a handful of diodes and capacitors? Rory Holmes shows how it's done.

In this month's first Designer's Notebook we shall be looking at a variety of interesting voltage multiplier circuits that can be built using ordinary CMOS gates and common-or-garden $1 N 4148$ signal diodes. DC-to-DC converters for a number of applications became possible by simply driving voltage multiplier chains with an AC clock signal, again implemented with CMOS gates. The initial supply voltage can be multiplied both positively and negatively, to give for example a split rail op-amp supply from a standard 5 V TTI supply. Negative and positive voltage references used in analogue-to-digital conversion and other signal conditioning circuits can also be generated, as can general purpose high voltage bias rails.

By using a novel 'chain' of inverter gates to independently drive each node of a diode-capacitor ladder, some rather unique circuits result.

## Chain Reaction

First, let's look at the usual multiplier circuits shown in Fig. 1a. These are normally used with rectifier-type diodes, low frequency $A C$ inputs (sine waves) from transformers, and electrolytic smoothing capacitors. At first glance there seems to be no common pattern between them, and little similarity to the multiplier chains used in TVs and other EHT power supplies.


Fig. 1 Standard voltage multiplier circuits.


Fig. 2 A CMOS doubler circuit.
However, in all cases the AC input waveform is fed via capacitors to appear at those circuit junctions marked ' A ' in Fig. 1a, while those junctions marked ' $D$ ' will maintain a steady $D C$ potential relative to the earth point. We can thus redraw the circuits by connecting up the capacitors in two series chains (assuming their values are altered accordingly) and still preserve the same circuit action. One chain carries the AC signal, while the other accumulates the DC voltage shifts. Figure 1 b shows these redrawn circuits, which now appear as extensions of the standard ladder network. The doubler, of course, remains in its original form since it only has one set of capacitors.

Starting with the doubler, we can build a very simple DC-to-DC converter using one CMOS gate as shown in Fig. 2. The Schmitt inverter gate is configured as a square wave oscillator running at about 100 kHz - the multiplier capacitors C2 and C3 will therefore have a low impedance at this frequency, which is also within the switching speed capability of the 1 N 4148 s . For this reason, rectifier diodes such as the 1N4001, which have much slower switching speeds, cannot be used in these circuits.

The oscillator output at point ' $A$ ' will therefore be switching between the 0 V and 10 V supply levels. When the output is at logic low, capacitor C2 will charge up positively (in the direction of the arrow) via D1. D2 is reverse biased and so effectively out of circuit. When point ' $A$ ' goes high to +10 V the positive end of C 2 at ' B ' will be raised to +20 V . This reverse biases D1 and allows C3 to charge up through D2. The voltage on C3 is thus maintained at about +20 V less two diode drops (ie at 18 V 6 ) as the cycle repeats itself. This is known as a diode charge pump.

## Building An Extension

This principle can be extended using exactly the same chainlike structure as illustrated in the positive and negative multipliers of Fig. 3. In both cases the inverter gates are cascaded and driven from a square wave


Fig. 3a A two-stage positive voltage multiplier (multiples by +3 ). b. A two-stage negative voltage multiplier (multiplies by -2).
oscillator at around 100 kHz . Each inverter gate contributes its own output current (a maximum of around 2 mA ) via the capacitors into the multiplier chain: because of this, the available output current will always be the same no matter how many times the voltage is multiplied (two times in this case).

The positive multiplier output of Fig. 3a includes the initial positive supply potential, and so generates three times this voltage less the three diode drops of 0V7 each. The negative multiplier of Fig. 3b, on the other hand, is referenced to the ground rail, giving -2 times the voltage (again less the diode drops).

As mentioned before, all the diodes are 1N4148s: the multiplier capacitors $\mathrm{C} 2-4$ are all non-critical and may be anything from 10 nF to 100 nF . C4 may be a polarised tantalum capacitor of a few microfarads to provide further smoothing. Any type of CMOS gate which can be connected as an inverter could be used, as well as all the standard inverters, though the 4049B hex inverter offers slightly more output current. It's also possible to use the 74 C series types such as the 74 C 04 or 74 C 14 . Pin-outs for these chips are given in Fig. 4 and not on any of the circuit diagrams, since they differ from type to type.

The oscillator implementation and its frequency are also non-critical; you could experiment with anything


Fig. 4 Pin-outs for the standard hex inverter packages which may be used in the circuits given in this article.
from several kilohertz to several hundred kilohertz. Remember, though, that as the frequency decreases, the impedance for a given capacitor value will increase, so increasing the impedance of the multiplier output.

Table 1 lists out the different voltages you can expect from different chain lengths and supply voltages, based on the circuits of Fig. 3. The number of stages refers to the number of capacitors that are actively driven from inverter outputs. Using this table it becomes very easy to design a generator for any voltage requirement; the output voltage could be clamped to the exact level required using an ordinary zener diode regulator. But remember there isn't much current available, and as the output is loaded the voltage will decrease due to the supply impedance. The higher supply voltages will generally provide more output current.


Fig. 5A 110 V supply using one hex inverter IC.
As an example, Fig. 5 shows a longer multiplier designed to give 110 V and built using only one hex inverter IC, of the Schmitt trigger type (40106B). Using ceramic capacitors, this circuit could be built to a very small size.

## Operating Principles

How do these multipliers actually work - the doubler circuit of Fig. 2 is straightforward, but what about the longer types? Voltage multiplier explanations are usually notoriously difficult to follow, let alone understand, and


Fig. 6 Waveforms for a two-stage positive multiplier (idealised for clarity with diode drops ignored).
we shall therefore adopt a more graphic approach. If we measure the voltages at the lettered points in Fig. 3a and plot them against time, we get the waveforms shown in Fig. 6. These waveforms have been idealised for clarity no account has been taken of the voltage drops due to the diodes in the circuit. From these it can be seen that the voltage across C2 (the difference between the waveforms $A$ and $B$ ) is a constant 1 V , where V is the supply voltage, while that across capacitor C3 (between points C and D ) is 2 V . We also know that the final output voltage across C 4 is 3 V . Moving down the chain towards the final output, then, we find that each capacitor maintains a DC charge which increases in integer multiples of the supply voltage. How so?

Consider capacitor C2 in Fig. 3a. At power-on it is discharged but when point A switches low, it charges up

TABLE 1

|  | CMOS SUPPLY VOLTAGE |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 5 V |  | 10 V |  | 18V |  |
| OUTPUT POLARITY | + | - | + | - | + | - |
| NO. OF STAGES |  |  |  |  |  |  |
| 1 | 8.6 | 3.6 | 18.6 | 8.6 | 34.6 | 16.6 |
| 2 | 12.9 | 7.9 | 27.9 | 17.9 | 51.9 | 33.9 |
| 3 | 17.2 | 12.2 | 37.2 | 27.2 | 69.2 | 51.2 |
| 4 | 21.5 | 16.5 | 46.5 | 36.5 | 86.5 | 68.5 |
| 5 | 25.8 | 20.8 | 55.8 | 45.8 | 103.8 | 85.8 |
| 6 | 30.1 | 25.1 | 65.1 | 55.1 | 121.1 | 103.1 |
| 7 | 34.4 | 29.4 | 74.4 | 64.4 | 138.4 | 120.4 |

Table relating supply voltage and number of stages to the (unloaded) output voltage, for positive and negative output multipliers based on the circuits of Figs. 3a and 3b and allowing 0V7 for each diode drop.
to the supply voltage via D1 (neglecting diode drops). Point $B$ is therefore at supply voltage. When point $A$ switches high, then, point $B$ is raised to twice the supply voltage. Point $C$ must be at zero volts since it is the inverse of point A, so current flows via D2 (which is now forward biased) from point B into C3 until C3 is charged up to the voltage at $B$ (ie twice supply). The next clock pulse takes point $A$ low, so point $B$ is at supply less the voltage that has leaked into C3, and C2 is topped up via D1 again. Meanwhile point $C$ has switched to supply voltage, so point $D$ is now at three times supply and D2 is reverse biased, preventing C3 from discharging back into C2. C3 can discharge into C4 via D3, however, so the voltage across C4 is maintained at three times supply.

It should now be clear that no matter what the length of the multiplier, each capacitor in the chain maintains a steady DC charge which equals that on the previous one plus the supply voltage, and each capacitor tops up the next one in the chain on each alternate half-cycle. Figure


Fig. 7 How multiplier voltages accumulate down the chain.


Fig. 8 Charging paths for an extended multiplier chain. The diagrams only show those diodes which are forward biased (conducting) during alternate half cycles of the drive waveform.

7a, for example, shows five stages of a multiplier chain driven by a square wave signal, while Figs. 7b and 7c use a waveform to represent the voltage levels at each capacitor node for each half of the cycle. The direction and voltage of the DC charges on each capacitor is also shown remember these are constant as shown by the graph of Fig. 6.

Looking at C1 and C2 in Fig. 7b we can see that the positive (top) end of $C 1$ will be at $V$ volts ( $V$ is the supply voltage) while the positive end of C 2 is at 3 V volts ( 2 V of its own, raised up a further $V$ volts at the CMOS output). Diode D2 will therefore be reversed biased and effectively out of circuit. For similar reasons C 3 will be at 3 V volts (less that which has leaked away) and can therefore be charged up via D3 from C2. On the other half cycle in Fig. 7 c , however, C 3 will be raised up to 4 V volts by the CMOS output, while C2 returns to 2 V . So this time D3 is reverse biased and will not conduct. C 1 is now raised to 2 V and can thus charge C2 via D2. The conducting and nonconducting parts of the circuit for each half cycle are shown in Fig. 8, which gives a much clearer illustration of the diode charge pump action.

## The Appliance Of Science

Figure 9 shows the circuit of a split-rail power supply that generates $\pm 10 \mathrm{~V}$ from a 5 V supply input. It could beq


Fig. 9 A split-rail supply using one hex inverter package.
used to power low current op-amp circuitry and other CMOS circuits from a standard TTL power supply. Again, only one hex inverter pack is required and we recommend that the 4049 B is used with its slightly higher output current capability. The circuit takes advantage of the three cascaded inverters that drive the positive multiplier chain, by also using them to form a 'ring-of-three' oscillator. The multiplier chain is therefore self-oscillating!

The positive side in turn drives the negative chain of IC1d, e and f. From Table 1 we would expect the available output voltages to be +17 V 2 and -12 V 2 , which are then clamped to the $\pm 10 \mathrm{~V}$ levels by zeners ZD1 and ZD2. Series limiting resistors for the zener diodes are unnecessary due to the current-limitid output of the multiplier.

Figure 10 shows a variation on the previous circuit's positive multiplier section, using all six inverters to provide more output current at $\pm 10 \mathrm{~V}$. To achieve higher output currents, simply parallel the CMOS gates that drive the capacitor chain: the available currents will add together due to the nature of the CMOS output FETs. This technique is useful forCMOS operating at lowsupply voltages.

Figure 11 gives the circuit for a 24 -stage positive multiplier to generate a high-voltage, low-current supply. This could be used for a solid state 'megger' (high resistance meter and insulation tester). The 24 stages can be achieved using only four hex inverter packs, and will provide 433 V from an 18 V supply. This circuit illustrates the fact that the inverters may be wired up in any fashion so long as alternate capacitors receive opposite phases of the square wave.

The circuit will deliver at least 2 mA at 430 V ! - not lethal but pretty painful, so be careful. We suggest the addition of a 1 MO series resistor in the positive supply lead to limit the available current to about 400 uA . A 100 uA meter would provide suitable megohm readings.


Fig. 10 Paralleling inverter stages to give a higher current supply.


Fig. 11 A 433 V generator using a 24 -stage positive multiplier and an 18 V supply.


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# REAL TIME CLOCK/CALENDAR 

## It seems strange that many microcomputers cannot tell the time of day or the date when such a facility can be so useful to the programmer. Never fear, ETI is here, with a simple peripheral for 6502-based machines. Design by M.D. Bedford

Programmers who are familiar with mainframe or minicomputers will probably be aware that it is generally possible to access the actual time and date from within a program. Such a facility is known as a real time clock and is often not available on the more modest microcomputers. It is not difficult to see that a real time clock would enhance any system applications range from control programs, to the determination of the elapsed time between occurrences, to giving listings that professional touch by using the time and date in the header.

Two approaches are possible for the implementation of a real time clock - software or hardware. Traditionally, a software solution has been used in which a hardware interrupt is generated at regular intervals, probably every 20 milliseconds, these being counted by the interrupt handling routine which then calculates the time and date. Such a system obviously requires initialising and would prompt the user for the time and
date each time the computer was switched on (our own word processor uses this system - Ed). Quite apart from the possible inconvenience, this method is probably unsuitable for most microcomputer users as it would require modification of the monitor program in ROM to prompt for the time and date. On the other hand, it is possible to devise a hardware alternative with battery back-up which is transparent to the system when not being accessed and doesn't lose the time and date on power-down of the main system.

For these reasons a hardware approach is presented here. The design is primarily intended for the Tangerine Microtan system, the PCB given here being of such a size that it will plug directly into the system rack. From an electronic point of view, however, there is no reason why the board may not be used with any 6502-based computer.

## Functional Description

The real time clock, which may be configured to occupy any 16-byte block within the Tangerine


A bird's eye view of the completed project.

I/O area, has 16 registers as specified in Table 1. It will be noticed that 12 of the registers are used to store the time and date, two registers being used to store (in BCD format) any number which may take a value greater than nine. For example, the value of the minutes is calculated as (10*REGISTER 5) + REGISTER 4. Of these 12 registers, registers 1-3 are read-only, these 'seconds' registers being automatically set to zero on starting the clock.

Each time the clock is updated, ie every tenth of a second, a flipflop is set, writing a value of 15 to all the readable registers to indicate that an update has taken place since the last read. Reading a register under these conditions resets the flip-flop so that a further read will produce a valid result.

This board may also be used to generate interrupts at regular intervals, this function being controlled by register 15 as described in Table 2. Switch SW2 may be used to disable interrupts, a facility which is especially useful in view of the fact that this board does not reset at switch-on.

The remaining registers are write-only and have various control functions. Register 0 should have a value of 0 written to it to select non-test mode for normal operation. A value of 1, 2, 4 or 8 should be written into register 13 to indicate leap year, leap year +1 , leap year +2 , or leap year +3 respectively. A value of 1 written to register 14 will start the clock, whereas a value of 0 will stop it. Switch SW1 gives the board write-proteciton, hence obviating the accidental overwriting of the time and date once initialised. This facility does not affect register 15 so that interrupts may still be selected when the


Fig. 1 Circuit diagram of the real time clock/calendar. Non-Microtan owners will find a circuit to generate the IO signal in last month's ETI.
board is write-protected. Both switches are mounted so that 'down' selects the enabling of the appropriate function.

The battery back-up facility allows data to be retained when the computer is not switched on, hence avoiding the need to initialise the clock at power-on. The time and date will be retained for about three months with a fully charged battery and a minimum of one hours use every nine days will ensure that the battery remains in a state of full charge.

## Construction

If the printed circuit board layout presented here is adhered to,
construction should present no difficulties. Since the board is of a single-sided design, a number of wire links need to be fitted as shown on the component layout diagram. Sockets should be used throughout for the integrated circuits. It should be noted that the MM58174 IC is fabricated in CMOS and accordingly the usual precautions of not touching the pins of the IC and not soldering the board while the IC is in its socket should be adhered to.

We suggest that DIL headers plugged into DIL sockets should be used for the wiring of the selectable address links. A 16 -pin and an 8-pin socket should be used to make up the 24 -pin by $0.3^{\prime \prime}$ socket used for
these links. The required start address should be set up as follows: the start of the board is $16^{*}$ (the binary number represented by links 1-6) from the start of the Tangerine I/O area, where link 1 is the least significant bit. Making links $a$ and $b$ gives a 0 , making link c gives a 1 . So, for example, the following links will set up the board to start at 48 bytes from the start of the I/O area: link $6 a b$, link $5 a b$, link $4 a b$, link 3 $a b$, link 2 c , link 1 c . If the board is to be constructed to a different layout to suit non-Tangerine systems, the only points to be borne in mind are that C2, C3 and C4 should be well distributed around the board and that XTAL1, CV1 and C5 should be mounted close to IC7.

## HOW IT WORKS

The heart of the circuit, IC7, is the MM58174 real time clock which reads and writes four bits of data onto DB0-DB3. ALthough not absolutely necessary (since the top four bits could be masked out by programming), a neat hardware solution is provided by the use of IC8 to zero DB4-DB7 during read operations. The circuitry comprising IC1, IC6 and the DIL links gives a chip select for IC7 and IC8 when an address in the range selected by the links is accessed.

Since the MM58174 is specifically intended to interface with microprocessors such as the 8080 or Z80, the circuitry comprising IC3 and most of IC5 is required to generate the NRDS and NWDS signals from the 6502 $R / \bar{W}$ and $\phi 2$. Hence write protection
may be provided by blocking NWDS when SW1 is in the closed position. IC4 is used to detect when register 15 is being addressed (A0-A3 all high) and under these circumstances overrides the write protection.
IC2 is to buffer A0-A3 - in fact, the whole circuit is designed to present no more than one TTL load to any bussed signal.

D1 is used to pass the +5 V supply to IC7 when it is present, the battery being trickle-charged through R2 under these conditions. When the +5 V supply is not present, D1 prevents the battery from discharging through the power supply and IC7 is supplied with sufficient voltage to operate in standby mode via D2.

## TABLE 1

## List of Real Time Clock Registers

Reg No Function

Access Mode
PARTS LIST


TABLE 2

## DESCRIPTION OF INTERRUPT MODES

## Function

Value in Register 15
no interrupts
0 or 8
single interrupt after 60 seconds
repeated interrupts at 60 second intervals
single interrupt after 5 seconds
repeated interrupts at 5 second intervals
single interrupt after 0.5 seconds
repeated interrupts at 0.5 second intervals


Fig. 2 Component overlay for the real time clock.


## Programming

The following BASIC program is used for initialising the real time clock/calendar. The board should be write-enabled before running the program - however, if this is not done the user will be instructed to do so by the program. The program will fully validate the information given before writing it to the clock, to reduce the likelihood of human errors. We suggest that a time and date a few minutes ahead of the actual time is entered, the RETURN following the day of the week request being pressed exactly as this time arrives.
10 REM . . .MM58174 REAL TIME CLOCK INITIALISATION PROGRAM
20 DEF FNC $(I)=\operatorname{VAL}(M I D \$(T D \$$, I, 1))
$30 \operatorname{DEF}$ FNN $(\mathrm{I})=10 *$ FNC(I) + FNC( $1+1$ )
40 DIM DM(12)
50 DATA $31,28,31,30,31,30$, $31,31,30,31,30,31$
60 FOR I= 1 TO 12: READ DM(I):NEXT I
70 PRINT "MM58174 INITIALISATION"
80 INPUT "ENTER START ADDRESS OF BOARD'; AD
90 POKE AD, 0:REM . . . NON TEST MODE
100 POKE AD + 15, 0:REM... DISABLE INTERRUPTS
110 POKE AD + 14, 0:REM . . . STOP CLOCK
$1201=\operatorname{PEEK}(A D+4): 1=\operatorname{PEEK}(\mathrm{AD}+4)$
$130 \mathrm{~J}=15$ AND ( $\mathrm{I}+1$ ): POKE AD + 4, J
$1401=\operatorname{PEEK}(A D+4)$
150 IF I = J THEN 180
160 PRINT "WRITE ENABLE REAL TIME CLOCK - RETURN WHEN DONE'; :GET A\$
170 GOTO 120
180 INPUT "ENTER TIME AND DATE IN THE FORM HH MM DD/MM/YY'; TD\$
$190 \mathrm{HH}=\mathrm{FNN}(1)$
200 IF $\mathrm{HH}<0$ OR $\mathrm{HH}>23$ THEN 180
210 POKE AD + 7, FNC(1): REM . . . HOURS * 10
220 POKE AD + 6, FNC(2): REM . . .HOURS
$230 \mathrm{MM}=\mathrm{FNN}(4)$
240 IF $M M<0$ OR $M M>59$ THEN 180

250 POKE AD + 5, FNC(4):REM . . .
MINUTES * 10
260 POKE AD + 4, FNC(5):REM . MINUTES
$270 \dot{Y} Y=F N N(13)$
280 IF YY<0 OR YY > 99 THEN 180
290 YR =
$2 \uparrow(3-(Y Y-4 * \operatorname{INT}(Y Y / 4)))$
300 IF YR $=8$ THEN
DM $(2)=29:$ GOTO 320
$310 \mathrm{DM}(2)=28$
320 POKE AD + 13, YR:REM . . . YEAR STATUS
$330 \mathrm{MM}=\mathrm{FNN}(10)$
340 IF MM < 1 OR MM $>12$ THEN 180
350 POKE AD + 12, FNC(10):REM MONTH * 10
360 POKE AD + 11, FNC(11):REM ... MONTH
370 DD $=\mathrm{FNN}(7)$
380 IF DD $<1$ OR DD $>\mathrm{DM}(M M)$ THEN 180
390 POKE AD + 9, FNC(7):REM . . . DAY * 10
400 POKE AD + 8, FNC(8):REM . . . DAY
410 INPUT "ENTER DAY OF WEEK (1-7, $1=$ MONDAY $)^{\prime \prime}$; DW
420 IF DW $<1$ OR DW $>7$ THEN 410
430 POKE AD + 10, DW:REM . . . DAY OF WEEK
440 POKE AD + 14, 15:REM . . . START CLOCK
450 PRINT "WRITE DISABLE REAL TIME CLOCK"
460 STOP
470 END
To access the time and date from within a program, the following BASIC subroutine may be used: a few words of explanation are probably appropriate. Line 1040 clears the update flip-flop by reading the clock once. The following two lines then loop until a value of 15 is read, indicating that an update has just taken place and that a tenth of a second is available to read the registers before the next update. It is the requirement to read 11 registers in this 100 milliseconds time slot (in order to avoid the possiblity of an update occurring between the reading of two registers) which accounts for the strange appearance of much of the rest of the subroutine. The inherent slowness of BASIC on an eight-bit microcomputer dictated the
avoidance of FOR-NEXT loops, subscripted variables and numerical constants in the time-critical portion. The routine returns with numeric values of seconds, minutes ... months in R2-R7 respectively, an ASCII representation of the time in TM\$ and an ASCII version of the date in DT\$.
1000 REM . . .MM58174 READING ROUTINE
$1010 R 2=A D+2: R 3=A D+3: R 4=$ $A D+4: R 5=A D+5$
$1020 \mathrm{R} 6=A D+6: R 7=A D+7: R 8=$ $A D+8: R 9=A D+9$
$1030 R A=A D+10: R B=A D+11:$ $R C=A D+12$
$1040 \mathrm{Z}=\operatorname{PEEK}(\mathrm{AD}+2)$
1050 Z $=\operatorname{PEEK}(A D+2)$
1060 IF $Z<>15$ THEN 1050
1070 R2 = $\operatorname{PEEK}($ R2 2$):$ R3 $=\operatorname{PEEK}(R 3)$ : R4 $=\operatorname{PEEK}($ R4 $)$
1080 R5 = PEEK (R5):R6 = PEEK (R6): R7 $=$ PEEK (R7)
1090 R8 = $\operatorname{PEEK}($ R8 $):$ R9 $=\operatorname{PEEK}(R 9)$ : RA $=\operatorname{PEEK}($ RA $)$
$1100 \mathrm{RB}=\operatorname{PEEK}(\mathrm{RB}): \mathrm{RC}=\operatorname{PEEK}(\mathrm{RC})$
1110 TM $\$=\mathrm{CHR} \$(48+\mathrm{R} 7)+\mathrm{CHR} \$$ (48 + R6) +" $:^{\prime \prime}+\mathrm{CHR} \$(48+\mathrm{R} 5)$ + CHR $\$(48+$ R4)
1120 TM\$ = TM $\$+{ }^{\prime \prime}:{ }^{\prime \prime}+$ CHR $\$(48+-$ R3) + CHR $\$(48+\mathrm{R} 2)$
1130 DT $\$=\mathrm{CHR} \$(48+\mathrm{R} 9)+\mathrm{CHR} \$$ $(48+\mathrm{RB})+{ }^{\prime \prime}$ " $+\mathrm{MM} \$(\mathrm{RB}+$ 10*RC)
$1140 R 2=R 2+10^{*} R 3$
$1150 \mathrm{R} 3=\mathrm{R} 4+10^{* R 5}$
1160 R4 $=$ R6 $+10^{* R 7}$
1170 R5 $=R 8+10 * R 9$
1180 R6 = RA
$1190 R 7=R B+10^{*} R C$
1200 RETURN
Prior to calling the above subroutine, the following portion of program should be executed to store the names of the months in the array MM\$:
10 DIM MM\$(12)
20 DATA "JANUARY"
"FEBRUARY", "MARCH",
"APRIL", "MÁY", "JUNE"
30 DATA "JULY", "AUGUST",'
"SEPTEMBER", "OCTOBER",
"NOVEMBER"" "DECEMBER"
40 FOR $N=1$ TO 12: READ
MM $\$(\mathrm{~N}):$ NEXT $N$

## BUYLINES

The MM58174 real time clock/calendar IC is available from Cricklewood Electronics, Technomatic or Watford Electronics. The PCB-mounting switches and Nicad battery might be a bit tricky to find unless you have industrial contacts, but non-PCB types could be used and wires taken to the PCB pads; there's enough room on the PCB, which is available from our PCB Service as usual. See page 87. The Euro connector is stocked by Watford Electronics.

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## R\＆EW

気気事


# Could the end be in sight for semiconductors? Once again ETI gets a world exclusive, as Owen Bishop describes the revolutionary technology which is poised to take us through to the 21st Century. 

I$t$ seems an age since the Gemini spaceflights of the middle nineteen-sixties, yet then was born an entirely new concept in electronics which has only just been brought to production stage. Almost weekly we hear of spin-offs from space-age technology, but this is one which threatens to render obsolete almost all of today's circuit designs. Opto-technology, surface acoustic wave devices and bubble memories are out of the running before they have hardly begun to crawl.

FEVAs, Field Effect Voltage Amplifiers, were born in the sixties, grew up in the seventies and, in the eighties, are ready to take over all the functions that are performed by semiconductor and related devices today. Their full designation is SCFEVAs, which gives a clue to their origin, for this is an abbreviation of Space-Channel Field Effect Voltage Amplifiers. The space channel will soon replace all the $N$-channel and P-channel devices we take for granted nowadays.

## Serendipity

No, this is not the acronym for yet another complex electronic wonder but a word which means 'making unexpected discoveries by accident'. FEVAs began this way during one of the early space-walks of the Gemini missions. The immense potential of the discovery was realized immediately by astronaut Lee Old, but it is only today that the news is beginning to surface.

It happened like this. During their second spacewalk, the astronauts were engaged in a capsule-service practise routine. Their task was to insert a plug of expanded polystyrene into a recess in the rear of the capsule in order to enhance its aerodynamic qualities in readiness for re-entry into Earth's atmosphere. You may think that expanded polystyrene is an unlikely material for this purpose but it has several features in its favour. Its strength-to-mass ratio is one of the highest, a factor of immense importance in space travel. As any handyman knows, another advantage of expanded polystyrene is that it is easily cut, and as any handyman also knows, the best way of cutting it is to use a hot wire. The extremely high thermal insulating properties of expanded polysteyrene mean that a hot-wire cutter functions perfectly, even in the sub-zero temperatures of outer space. So it was to be a neat and well-thought-out manoeuvre, but then the unexpected happened.

## Blowing In The Wind

Whenever Lee switched on his hot-wire cutter, his colleague 'Gig' Potter was alarmed by intense activity on the Solar Wind Detector. This was an on-board experiment devised by the Department of Applied Physics of the University of Minniwaukee, the purpose of which was to monitor the streams of electrons being repelled from the Sun's chromosphere. When the wire was hot, the effect was like a solar gale! Lee immediately realized that there must be some kind of interaction between his hot wire and
the Solar Wind Detector. Electromagnetic interference was immediately ruled out, for the wire was not coiled and, in any event, was powered by direct current.

It must be that electrons from the atoms of the wire were being energised by the heating, were escaping from the confines of the wire and passing to the Solar Wind Detector. Maybe there was an electric field caused by the friction between Lee's space-gloves and the expanded polystyrene which was accelerating the electrons toward the detector.

## Back To Earth

We hear a lot about taking Earth-bound manufacturing technologies to space to gain the advantages of the conditions there, but this is a case of bringing the conditions of space down to Earth. Lee's penetrating insight told him that the key to implementing his discovery was to create space conditions on Earth, and the solution to this problem was blindingly simple. Take a suitable container and suck the air out of it! The space channel is, in fact, known in everyday parlance as a vacuum. Lee resigned his commission in order to devote himself full-time to promoting the commercial aspects of his discovery. But Lee was back on Earth in more senses than one! He soon came up against the incredulity and stultifying caution of the financial world, at whose door must be laid the blame for the excessive delay in bringing to the human race the farreaching benefits of this new technology.

## The FEVA Diode

Curiously enough, one of the key devices in this new range does not in fact amplify voltages. It mirrors the original space-walk conditions: enclosed in a sealed glass capsule (Fig. 1) is a hot wire and a metal plate. When the wire is heated by passing a current through it, and a potential difference is applied between the wire and the plate, electrons flow from the wire to the plate across the space channel. We have an electric current. As in the original scenario, the plate (corresponding to the solar wind detector) is unheated, so electrons do not flow from the plate to the wire. Current flows in only one direction, just as at a PN junction in semiconductors. These devices have taken their name from their semiconductor equivalent device and are known as FEVA diodes. But whereas we have to use highly purified silicon and rare metals such as antimony to manufacture a semiconductor device, the FEVA needs nothing but sweet nothingness to provide its conducting channel. Apart from the low-cost metals used for making the wire and plate, the FEVA is constructed entirely of re-cycled glass and plastic.

The story of the terminal pin design is an amusing one. Lee was looking for something to hold his prototype FEVA diode when he came across a handy four-pin socket which had resided for years unused in his junkbox (Fig. 2). He had never known the original purpose of this socket, for it had been in the box when it was donated to him by


Fig. 1 The prototype FEVA diode. The base is of formaldehyde-phenol plastic (known as Bakelite) and is not to be confused with the base of a transistor.
his grandfather. It suited the present purpose well and, such is the way of things once they have been found to suit, there was no real incentive to re-design the socket for later devices. The novel 'kite' configuration of the pins offers many advantages over the old-fashioned DIL array. As many electronics hobbyists known to their cost, it is so easy to insert the IC the wrong way round, but this is quite impossible with a FEVA.

## Field Effect Devices

If the FEVA diode is the counterpart of the semiconductor diode, the basic FEVA device typified by the PM2DX (Fig. 3) is the equivalent of the field effect transistor. The so-called 'grid' is a sheet of wire gauze cunningly introduced by Lee between the wire and plate to modulate the electric field and so regulate the flow of electrons in the space channel. A very small change in the potential of this plate has a significant effect on the current flowing through the device, simulating the effect of gate potential in a conventional FET, though the mechanism is somewhat different and at present less well understood. A resistor placed in series with the plate (or anode as it is now called, referring of course to the corresponding anode terminal of the semiconductor diode) develops a useful change of potential running to several tens of volts. Incidentally, these devices work at high voltages, levels that would reduce the ordinary FET to a bead of charred silicon!

## Integration

No sooner had the initial designs been proven in extensive laboratory and field trials than the logical follow-up was to put more than one device in the same capsule. An early example is the ECH21 frequency converter (Fig. 4), but already the OEMs, eager for the rapid and profitable returns that this new technology will generate for many decades to come, are pressing ahead with mind-boggling developments.

The first commercial product incorporating the new range of miniaturized FEVAs is to be launched in April 1983. This is a digital time-piece of elegant and sizable proportions. No need for the short-sighted to put on their specs to read this one! It comes with a durable PVC backpack for the battery power supplies, with a choice of embroidered shoulder straps for the ladies. Those of you who have a half-acre building-plot to spare and have planning permission for a five-storey block, will be pleased to know that the first 1-kilobyte FEVA-technology personal com-
puter is due to be launched in April 1984. The installation expenses may readily be recouped, for it incorporates heat-exchangers which may be connected as a thermal source for your local district-heating scheme.

In the meantime, hobbyists can throw away their magnifying glasses and turn to the man-sized technology of the future. Mauldin Electronics Ltd and Armpit International are both marketing a hobbyist familiarization conversion kit which includes an assortment of FEVAs, 3 kg of FEVA sockets, four square metres of 14 swg aluminium sheet for mounting the FEVA sockets ('chassis' is the newly coined term), a 50 W soldering iron with 8 mm bit, an oven-glove for use in handling hot FEVAs and a colourful but comprehensive wall-chart on first aid for electrocuted persons. Our own sister magazine, Spam Radio Today, is hoping to publish details of a transceiver project using these devices.

## Coming Of Age

The heady days of the development era of the FEVA are over. The name itself, harking back to the sixties, is nowadays thought to be too flippant for a technology which is to bring Britain back to world domination in the


Fig. 2 Yet another type of socket to add to the massive range we already have. Known as the UX4, it is the new standard socket for FEVA diodes, and is available in a range of attractive colours: black, brown, grey or buff.
electronics of the twenty-first century (and beyond?). There is a strong move afoot to rename FEVAs even before their first name becomes a byword to the man in the street. For one thing, with the advent of the Shuttle, space technology is becoming commonplace and no longer excites the imagination as it once did. The new name for this technology firmly faces facts, replacing 'space channel' by 'vacuum'. So if you never hear anything more about FEVAs, the wonder of our age, keep a sharp look-out for their new designation - Vacuum Linked Voltage Expanders. The new name is sticking well and already the back-room boys have affectionately shortened this to 'VALVE'.


Fig. 3 (Left) Pin-out schematic of the PM2DX, the basic FEVA amplifier.
Fig. 4 (Right) Pin-out schematic of the ECH21, the FEVA technology frequency counter. Is this the first step towards a computer in a capsule?

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# STAGE LIGHTING PART 3 

## Design by David Colven and Ian Cleverley.

## Setting Up

Set SW5, the manual/auto switch, to manual for the channel designated ' 0 '. Check that the master blackout switch is off, and that RV1 for that channel is set to minimum (the manual "slide pot). Set the speed-up switch SW4 to off, and turn PR8 to minimum. Now switch on the mains and set PR9 to midposition. Slide RV1 to maximum and adjust PR7 for maximum light output. Then slide RV1 to minimum and set PR8 to give minimum light output (the bulb should just glow). Repeat these adjustments until the light glows at the minimum setting of RV1 and is full on at the maximum setting.

To set up the auto-fade units, first set SW5 for the channel to automatic, with RV1 at minimum. Set PR6 on the channel to be calibrated to minimum and set the scene select switches to ' 00 '. Now, using the keyboard, program the channel, ' 00 ', the lighting level, ' 0 ', and the time duration, ' 37 '. Press the enter button; the display should now read '000 37'. Enter the following:

| SCENE | DATA |
| :---: | :---: |
| 01 | 00137 |
| 02 | 00237 |
| 03 | 00337 |
| 04 | 00437 |
| 05 | 00537 |
| 06 | 00637 |
| 07 | 00737 |

Remember to press the enter button after each entry of five digits. Now set the scene selector switches to ' 07 ' and press SW1. Set PR5 one-third of a
rotation clockwise from minimum, set PR13 to maximum, and adjust PR6 to give the maximum light output. Now set the scene selector switch to ' 00 ' and press SW1 again. Adjust PR1 for minimum light output (the light should just glow). Now by using the scene select switches and the scene change switch to step through the data sequence just programmed in, the remaining presets PR2,3,4,10,11 and 12 may be adjusted as appropriate to give the eight lighting levels.

To adjust for an even ramp rate, reset the scene select switch and press the scene change switch so as to compare the time between the light
rising to the preset level and falling to zero. If there is any difference, adjust PR5 until the time rise and fall times of the light level are about the same. Alternatively, if you have a scope you can inject a signal at pin 2 of IC29 and look at the output (pin 6). Adjust PR5 to give a square wave with equal markspace ratio.

This completes the setting-up for the first channel. Repeat for the other channels, but remember when programming to change the channel number as appropriate for the first two key presses (' 01 ' for the next cannel and so on).

PARTS LIST

| Resistors (all $1 / 4 \mathrm{~W}, 5 \%$ ) IC5 |  |  |  |
| :---: | :---: | :---: | :---: |
| R1 | 270R | IC5 ${ }^{\text {c }}$ | 74LS04 |
| R2-4 | 10k | IC6-9 | 74 7S75 |
| R5 | 100R | IC10-13 | 74LS47 |
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| R37,38 | 560R | IC19 | 74LS154 |
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| R40,42-50 | 1 k 0 | IC21 | 74LS00 |
| R41 | 1k5 | IC22 | 6116 |
| R88,89 | 470R | IC23,24 | 81 LS97 |
| Capacitors |  | Q1,2 | BC108 |
| C1,3,4,26 | 100n polycarbonate or | D21,22 | 1 N4148 |
|  | polyester | ZD1 | 2V7 400 mW zener |
| C2 | 33u 16 V tantalum | DISP1-5 | 0.5 " common-anode seven |
| C5 | 14035 V tantalum |  | segment displays |
| Semiconductors |  | Miscellaneous |  |
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# DESIGNING NDFL AMPS 

# The use of nested differentiating feedback loops (NDFLs) is a new technique for reducing audible-frequency distortion in an amplifier to a vanishingly low level. As the name implies, NDFLs rely on negative feedback, but they use it in a new way. Edward M. Cherry, Associate Professor of the Department of Electrical Engineering, Monash University, explains the theory involved. 

In order to understand just how far the new NDFL technique can improve an amplifier, we first need to know the fundamental limits to the reduction of distortion that can be achieved with conventional techniques. To begin with, we survey familiar negative-feedback theory.

Figure 1 is a block diagram of an amplifier with negative feedback. In this diagram, the forward path corresponds to the amplifier before feedback is applied, and its gain is traditionally designated by the Greek letter $\mu$. The feedback network returns a fraction $\beta$ of the output to the input circuit, where it is in some way subtracted from the true input to provide the actual input to the forward path.

In many practical amplifiers, the subtraction is accomplished by applying the input and feedback signals to the two inputs of a balanced differential first stage of the forward path. Figure 2 is an outline practical circuit. In this circuit the feedback factor $\beta$ is the attenuation of the network comprising $R_{F 1}$ and $R_{F 2}$

$$
\begin{equation*}
\beta=\frac{R_{\mathrm{F} 1}}{\mathrm{R}_{\mathrm{F} 1}+\mathrm{R}_{\mathrm{F} 2}} \tag{1}
\end{equation*}
$$

A typical value for an audio power amplifier might be $1 / 20$. The forward-path gain $\mu$ in Fig. 2 corresponds to gain from input to output when the feedback network is removed. A typical value for a simple audio power amplifier might be 1000 .

For Fig. 1 , the overall closed-loop gain A is given precisely by

$$
\begin{equation*}
A=\frac{\text { Output }}{\text { Input }}=\frac{\mu}{T+\mu \beta} \tag{2}
\end{equation*}
$$

The quantity $\mu \beta$ is called the loop gain. Physically, loop gain is the gain that would be observed if the feedback 'loop' in Fig. 1 was cut at some point, a signal was injected into one side of the cut, and the resulting signal at the other side of the cut was measured.

If the values of $\mu$ and $\beta$ are such that loop gain is small compared with unity, the closed-loop gain is very nearly equal to the forward-path gain (that is, the gain without feedback)

$$
\underset{\mu \beta<1}{A}
$$

However, if loop gain is large compared with unity, the closed-loop gain approaches the reciprocal of the feed-


Fig. 1 Block diagram of a feedback amplifier.
back factor and becomes almost independent of the forward-path gain

$$
\begin{gather*}
\mathrm{A} \vec{\beta}>1 / \beta  \tag{4}\\
\mu \beta
\end{gather*}
$$

The quantity $1 / \mathrm{B}$ is often called the demanded gain, as it is the value the overall closed-loop gain would take in ideal circumstances.
As a numerical example, if we suhstitute the above values $\mu=1000$ and $\beta=1 / 20$ into Equation 2, the gain of our 'typical' audio power amplifier works out as $\mathrm{A}=19.6$. The approximate Equation 4 predicts $A \rightarrow 20$, within $2 \%$ of the correct answer.

The quantity $1+\mu \beta$ occurs often in feedback theory. It is called the return difference $F$.

$$
\begin{equation*}
F=1+\mu \beta \tag{5}
\end{equation*}
$$

Physically, return difference has the significance

$$
\begin{equation*}
F=\frac{\text { forward-path gain }}{\text { closed-loop gain }} \tag{6}
\end{equation*}
$$

For values of loop gain greater than about 10, loop gain and return difference are almost equal - in our 'typical' example the value are 50 and 51 respectively.

Simplified treatments of feedback theory show that, if the distortion generated in the forward path (that is, the amplifier without feedback) at a particular output signal amplitude is $D_{\mu^{\prime}}$ then the resulting closed-loop distortion $D_{A}$ at the same output signal amplitude is

$$
\begin{equation*}
\mathrm{D}_{\mathrm{A}}=\mathrm{D}_{\mu} / \mathrm{F} \tag{7}
\end{equation*}
$$

Distortion is improved when feedback is applied to an amplifier by a factor equal to the return difference. In our 'typical' amplifier, $F=51$; if the distortion without feedback happened to be $10 \%$, then feedback should reduce the distortion to $0.196 \%$.

More rigorous treatments of feedback theory show that Equation 7 is no more than a poor approximation to the truth. In the first place, real amplifiers are far more complicated than Fig. 1 suggests, because several different feedback paths (not all intentional!) can be identified. For example, the collector-base capacitances of transistors inevitably provide some unintended feedback at high frequencies. There is a very real problem in interpreting just


Fig. 2 Outline circuit of an audio power amplifier.
what loop gain and return difference mean when there is more than one feedback loop. Once the correct interpretation is established, return difference invariably turns out to be a function of frequency, and the reduction of distortion corresponding to Equation 7 depends on the value of return difference at the frequency of the distortion, not the frequency of the input. Feedback therefore, does not reduce all distortion components equally.

Finally, it is found that the closed-loop distortion of an amplifier can contain new components that were not present in the distortion that existed in the forward path before feedback was applied. These new distortion components initially increase as loop gain is increased, but they fall away again towards zero as loop gain is made large.

Despite all these complications, the fact remains that adequate negative feedback, properly applied, does reduce distortion. Why, then, do amplifier designers not simply apply some arbitrarily large amount of feedback and reduce amplifier distortion to the vanishing point?

## TIM, IIM, PIM, . . .

In the last 10 years or so, readers of audio magazines have been made aware of a conjecture that goes something like this:
"Harmonic distortion and the usual intermodulation distortion decrease with increasing feedback. Transient intermodulation distortion (TIM) increases with increasing feedback, and is approximately directly proportional to the feedback. Therefore, there is an optimum value for the feedback at which the subjective distortion sensation is least. This optimum feedback is unlikely to exceed about 20 dB ."
More recently, there has been conjecture that heavy overall feedback should be applied with caution if interface intermodulation distortion (IIM) is to be avoided. An amplifier should provide a low open-loop output impedance so that the need for feedback-generated loudspeaker damping is minimised.

There has also been conjecture that negative feedback, which reduces the usual intermodulation distortion, may increase phase intermodulation distortion (PIM) by converting amplitude nonlinearities into phase nonlinearities.

Unequivocally, none of these conjectures has any basis in the new NDFL amplifiers. As an aside, there is a
substantial body of opinion that none of these conjectures has any basis, full stop; interested readers should refer to References 1-9.

## Instability And Oscillation

A fundamental limit to the amount of feedback that can be applied to an amplifier is set by the onset of instability and oscillation.

If the magnitudes of the forward-path gain and demanded gain of the idealised Fig. 1 are plotted versus angular frequency $\omega$ (in radian/second) on logarithmic scales, the resulting graph looks something like Fig. 3. The 3 dB bandwidth of the amplifier without feedback is $1 / \tau_{\mu}$ and the gain-bandwidth product (at which gain drops to unity) is $1 / \tau_{1}$.

Because the graph is on logarithmic scales, the separation between the curves of forward-path gain and demanded gain is the loop gain (remember that, to divide two numbers, you subtract their logarithms; if you divide $\mu$ by $1 / \beta$, you get $\mu \beta$ ). The magnitude of loop gain falls to unity at the frequency $1 / \tau_{\mathrm{x}}$ where the curves intersect and their separation is zero (remember that the logarithm of unity is zero).

By a similar argument, return difference is the separation between the curves of forward-path gain and closedloop gain, as indicated in Fig. 3.

We could make a similar graph to Fig. 3, showing the phases of $\mu$ and $1 / \beta$. Again, the phase of loop gain would turn out to be the separation between the two curves. However, there is a remarkable piece of mathematics due to Bode, who used a transformation evolved by Hilbert (1862-1943), which shows that there is a relation between the magnitude and phase of the response of any linear system. Subject to some qualifications, our proposed graph of the phases is completely predictable from Fig. 3 and contains no new information. Interested readers may refer to Chapter 14 of Bode's book (Reference 10) but are warned that it is anything but easy going!

As an example, many readers will know that, if the forward-path in Figs. 1 and $\overline{\mathrm{B}}$-ias a high-frequency cut-off rate variously described as single pole, $20 \mathrm{~dB} /$ decade, or 6 $\mathrm{dB} /$ octave, then its phase shift is $45^{\circ}$ at the 3 dB cut-off frequency $1 / \tau_{\mu}$, and is asymptotic to $90^{\circ}$ at very high frequencies.

In 1932, Nyquist applied a theorem which dates back to Cauchy (1789-1857) to derive the condition for a feedback amplifier to be stable and free from oscillation. If a polar plot is made of the magnitude and phase of return difference as frequency is varied, a vaguely 'snail-shaped' curve results. Such a polar plot is called a Nyquist diagram. Subject again to some qualifications, the stability criterion for a feedback amplifier is that its polar plot of return difference should not enclose the origin. Figure 4


Fig. 3 Logarithmic plots of gain versus frequency for Fig. 1.
shows one example each of a stable situation and an unstable situation.

Because the phase of return difference can be predicted from Fig. 3 via Bode's result a Nyquist diagram can also be constructed from Fig. 3 and the onset of instability can be predicted. In 1945 Bode showed that Ny quist's criterion could in fact be expressed in terms of the gradients of the curves in Fig. 3, thereby eliminating the work of finding the phase explicitly and plotting the Nyquist diagram. Bode's exact rule is complicated, but a useful paraphrase is
"If in graphs such as Fig. 3 the separation between the forward-path gain and demanded gain decreases toward zero at a rate not exceeding $30 \mathrm{~dB} /$ decade, the amplifier is unlikely to oscillate."
This paraphrase makes no allowance for the tolerances on components. It assumes, in effect, that everything about the forward path is well known and constant. In the audio context, the paraphase takes no cognizance of the fact that the capacitance of the leads that connect an amplifier and loudspeaker is anything but well known. A more conservative rule, applicable to the audio context, is therefore
'In graphs such as Fig. 3, the separation between the forward-path gain and demanded gain should not decrease towards zero at a rate exceeding 20 dB/decade."
transistors is a fraction of a nanosecond, but for power transistors of the ubiquitous 2N3055 class the transit time may be as long as a few tenths of a microsecond. Thus, the output stage of Fig. 2 may have a pole in the vicinity of 1 MHz .

As we saw in the previous section, the unity-loop-gain frequency $1 / \tau_{\mathrm{x}}$ in Fig. 3 must be substantially less than the frequency of all poles except the dominant pole $1 / \tau_{\mu}$ if an amplifier is to be stable. If the power transistors are of the 3055 class then, no matter how fast the other transistors may be, there is going to be one pole at about 1 MHz . Therefore $1 / \tau_{x}$ must be chosen to correspond to something like 200 kHz . Even with more modern power transistors, $1 / \tau_{\mathrm{x}}$ is restricted to about 1 MHz . The art of designing a stable power amplifier involves choosing the lag compensating capacitor $C$ such that $1 / \chi_{x}$ is appropriate to the transistors actually used.

The geometry of Fig. 3 is such that, no matter how $\mu, \beta$ and $\tau_{\mu}$ are separately chosen, the return difference $F(\omega)$ at any angular frequency $\omega$ cannot exceed

$$
\begin{equation*}
F(\omega) \leqslant 1 / \omega \tau_{x} \tag{8}
\end{equation*}
$$

Thus, if $1 / \tau_{x}$ is designed to correspond to 200 kHz , return difference at 20 kHz cannot exceed 10 ( $=20 \mathrm{~dB}$ ), and cannot exceed $200(=46 \mathrm{~dB}$ ) at 1 kHz . An amplifier that boasts 80 dB of feedback ( $\mathrm{F}=10,000$ at low frequencies) must have $1 / \tau_{\mu}$ corresponding to about 20 Hz ; return difference must begin falling above 20 Hz , and the former


Fig. 4 Nyquist's stability criterion. The curves are polar plots of return. difference for changing frequency.

The practical consequence is that the forward path of an audio amplifier with conventional resistive feedback should have a single dominant pole which sets the fall-off of gain at frequencies above $1 / \tau_{\alpha}$. The second and subsequent poles should lie at frequencies substantially above $1 / \tau_{\mathrm{x}}$ (the frequency where the separation reaches zero), because each pole contributes a $20 \mathrm{~dB} /$ decade downwards slope to the graph of forward-gain path.

## Maximum Available Feedback

In Fig. 2, the first stage is a long tailed pair with a current mirror at its output; the input and feedback signals are applied to the two bases to perform the subtraction process of Fig. 1. The second stage provides a large voltage gain, and the lag compensating capacitor $C$ provides the dominant pole of the forward path corresponding to $1 / \tau_{\mu}$ in Fig. 3. The third stage is a complementary class-B emitter follower whose function is to transfer the output voltage from the second stage to the loudspeaker load. In practice, the transistors in the second and third stages are often Darlingtons, and the input transistors are often replaced by FETs.

In any similar amplifier, there is at least one pole associated with the finite transit time of electrons through each transistor. The transit time for typical small-signal
values at 1 kHz and $20 \mathrm{kHz}(46 \mathrm{~dB}$ and 20 dB ) still apply.
Returning now to Equation 7, the effectiveness of feedback in reducing distortion is set by the frequency of the distortion, not the frequency of the input. The audible frequency range is generally reckoned to extend to about 20 kHz and, with the foregoing constraints, return difference at this frequency cannot exceed 10. Remembering that 20 kHz is the third harmonic of 6.667 kHz , we see that feedback cannot reduce offensive odd-harmonic distortion of mid-treble input signals by more than a factor of 10. Remembering too that 20 kHz is the seventh harmonic of 2.857 kHz , we see that feedback cannot reduce crossover distortion of mid-range input signals by more than a factor of 10 .

Until recently there has been no way around this problem except to increase the unity-loop-gain frequency $1 / \tau_{\mathrm{x}}$, and this demands that the frequencies of the transistor poles must be increased if stability is to be preserved. Fragile, expensive power transistors, with narrow bases to achieve short transit times, become mandatory.

## The NDFL Approach

There is, however, another solution to the stability problem. If the forward-path gain has two dominant poles, so that its gain falls at $40 \mathrm{~dB} /$ decade, the rate of closure


Fig. 6 Logarithmic plots of gain versus frequency for Fig. 5.
between the graphs of forward-path gain and demanded gain would still be $20 \mathrm{~dB} /$ decade provided the demanded gain itself were to tall at $20 \mathrm{~dB} /$ decade. In essentials, this requires that the usual frequency-independent resistive feedback factor $\beta$ should be replaced by something having a frequency dependence of the form $\omega \tau_{F}$ (remember that the demanded gain is the reciprocal of the feedback factor). Mathematicians tell us that a linearly rising frequency response corresponds to differentiation with respect to time and, in hardware terms, a capacitive feedback network will perform just this action.

Figure 5 shows the outline of an amplifier incorporating nested differentiating feedback loops. Notice first that the forward path has been separated into a number of stages, whose mid-frequency gains are $\mu_{1}$ to $\mu_{N}$ respectively. The variable $s$ is what mathematicians call complex frequency; for sinusoidal signals its magnitude is equal to the angular frequency $\omega$ of the sinusoid. Factors of the form ( $1+s \tau_{x}$ ) represent a frequency response that rises proportional to frequency above the frequency $1 / \tau_{x}$ - that is, they represent a zero. Similarly, factors of the form $1 /(1+s \tau$ ) represent a frequency response that falls inversely proportional to frequency above the frequency $1 / \tau_{0}$ - that is they represent a pole. Thus, the stages in Fig.


Fig. 8 The ( $\mathrm{N}-2$ )th loop of Fig. 5.

5 have special frequency responses: all stages except the first have a pole at $1 / \tau_{\text {: }}$, and all except the first and last two have a zero at $1 / \tau_{x}$.

Notice also that there are differentiating feedback networks, each denoted by $\mathrm{s} \tau_{\mathrm{f}}$, linking the output back to various points in the forward path. The resulting feedback loops are arranged one inside another, like a nest of Chinese boxes - hence the name nested differentiating feedback loops.

The amplifier is completed by an overall resistive feedback network $\beta$.

If we removed all the feedback from Fig. 5, the forward-path gain would be shown in Fig. 6: constant up to the frequency $1 / \tau_{0}$, then falling at an ( $N-1$ )-pole rate ( $20(N-1) \mathrm{dB} /$ decade) up to $1 / \tau_{x}$, and finally levelling off somewhat to a two-pole rate ( $40 \mathrm{~dB} /$ decade).

If we now applied just the overall resistive feedback $\beta$, the return difference would be as shown in Fig. 6. Distortion would be reduced by a constant large amount, approximately $\mu_{1} \mu_{2} \ldots \mu_{N} \beta$, at all frequencies up to $1 / \tau_{0}$. Choosing $1 / \tau_{0}$ to correspond to 20 kHz would virtually


Fig. 7 The inner loop of Fig. 5.
eliminate audible-frequency distortion. But the amplifier would be unusable because of oscillation.

The rate of closure of the forward-path gain and demanded gain curves breaks the rule of $20 \mathrm{~dB} /$ decade. Let us see how inclusion of the nested differentiating feedback loops solves the problem.

Figure 7 shows just the last two stages and the inner differentiating feedback factor. This 'clump' is a feedback amplifier in its own right, and Fig. 7 shows its forward-path gain (that is, the gain of the last two stages without any feedback), the demanded gain, and the resulting closedloop gain. Although the forward-path gain falls at a twopole rate ( $40 \mathrm{~dB} / \mathrm{decade}$ ), the demanded gain falls at a one-pole rate ( $20 \mathrm{~dB} / \mathrm{decade}$ ), and their rate of closure is $20 \mathrm{~dB} /$ decade. By itself, this 'clump' is stable.

Figure 8 shows what happens when we add the antepenultimate stage and another differentiating feedback factor. Again this 'clump' can be considered as a teedback amplifier in its own right. Provided we choose.

$$
\mu_{N-2}=\tau_{0} / \tau_{\mathrm{x}}
$$

the various gains line up as shown. The forward-path gain is the combined gain of stage ( $N-2$ ) and stages $(N-1)$ and $N$ with their local feedback, and this is the middle solid curve in Fig. 8. The demanded gain is the dashed curve passing through $1 / \tau_{f}$. Once again the forward-path gain and demanded gain close at $20 \mathrm{~dB} / \mathrm{decade}$, so the stability criterion is satisfied for this larger 'clump'.


Fig. 9 Complete plots of gain versus frequency for fig. 5.

And so it goes on. We can add more stages and differentiating feedback factors, and each time the curves line up as required for stability provided we choose

$$
\begin{gather*}
\mu_{1} \mu_{\mathrm{N}-1} \mu_{\mathrm{N}} \mathrm{~B}=\left(\tau_{0} / \tau_{\mathrm{x}}\right)^{2}  \tag{9}\\
\tau_{\mathrm{F}}=\mu_{1} \beta \tau_{\mathrm{x}}  \tag{10}\\
\mu_{\mathrm{K}}=\tau_{0} / \tau_{\mathrm{x}} \text { for } 2 \leqslant \mathrm{k} \leqslant \mathrm{~N}-2 \tag{11}
\end{gather*}
$$

Figure 9 shows the gain curves for the complete amplifier.
In designing an NDFL amplifier, the starting point is to choose the frequency $1 / \tau_{\mathrm{x}}$ so that the various transistor poles are sure to lie at substantially higher frequencies. Next choose the frequency $1 / \tau_{0}$ up to which the return difference should remain constant; 20 kHz is a suitable value for audio amplifiers. After this, the circuit more or less designs itself via Equations 9-11. above.

## Outline Practical Circuit

Figure 10 shows how an amplifier of the basic topology of Fig. 2 can be modified to include two NDFLs. Interested readers should refer to references 11, 12 for more details.

Notice first that the lag compensating capacitor, C, in the penultimate stage of Fig. 2 has been removed in Fig. 10. In its place are two capacitors (C) linking the output back to various points in the forward path. These capacitors are the feedback networks of the nested differentiating feedback loops.

The output stage has been changed to include a modified form of Thiele's load-stabilising network. Some form of LRC filter is required to locate one of the poles correctly, and with the circuit shown we get double value from the components.

The input stage itself is unchanged, but an inexpensive small capacitor in the overall feedback network $\beta$ can be used to correct the group delay and improve the reproduction of transient waveforms.

Another essential addition is an amplifying stage between the two nested differentiating feeback factors. This rather peculiar circuit (which dates back to Rush in 1964) seems largely to have been forgotten. It uses one NPN transistor and one

Fig. 10 Outline circuit for an NDFL amplifier.

PNP to provide a well-defined gain (13).
As already suggested, once the demanded gain $1 / \beta$ and the critical frequency $1 / \tau_{x}$ are chosen, the circuit almost designs itself. The equations are:

$$
\begin{gather*}
\frac{\mathbf{R}_{f 1}}{R_{f 1}+R_{f 2}}=\beta,  \tag{12}\\
\mathrm{RC}=\beta \tau_{\mathrm{x}},  \tag{13}\\
\mathrm{R}_{\mathrm{Y}} C_{\mathrm{Y}}=\tau_{\mathrm{X}},  \tag{14}\\
\tau_{\mathrm{L}}=(\sqrt{3}-1) \tau_{\mathrm{x}} . \tag{15}
\end{gather*}
$$

All stage gains and poles and zeros automatically look after themselves.

Figure 11 (a) shows the 5 kHz square-wave response of Fig. 10 as built from $5 \%$-tolerance resistors, 20\%-tolerance capacitors, and unselected production transistors. Evidently the circuit is 'designable'; Equations 12-15 really do predict component values for good transient response.

A nice feature of the modified Thiele circuit in Fig. 10 is that, when the load is made capacitive (a well-known source of high-frequency oscillation in amplifiers), the voltage waveform at the FEEDBACK POINT is the waveform the amplifier would have delivered into its nominal resistance load. Figures 11 (b) and (c) illustrate this; the violent ringing in Fig. 11 (b) is simply an LC resonance between the filter inductor and the load capacitance, and is in no way indicative of approaching instability.

Figure 12 shows details of the 1 kHz sinusoidal response under overdrive conditions. Note the quick,


Fig. 115 kHz square wave response of Fig. 10.

(a) 8 ohm resistance load.

(b) 8 ohm and 2 uF parallel load.

(c) waveform at feedback point for (b).


Fig. 131 kHz harmonic
distortion.

## clean recovery.

An amplifier has been built in which the circuit can be switched from Fig. 2 to Fig. 10, to illustrate the improvement in performance of adding two NDFLs. Figure 13 compares the measured third-harmonic distortions of 1 kHz . Notice how the distortion of Fig. 10 drops away to below three parts per million at small signal amplitudes. Such behaviour is more typical of class-A amplifiers than class-B amplifiers, and may account for the clean sound of NDFL amplifiers.

Crossover distortion associated with incorrect bias of the output stage is one of the most audibly annoying forms of distortion. Audio amplifiers based on Fig. 2 sometimes have a type of crossover distortion that does not show up
in normal measurements. Correct biasing of the output stage relies on close tracking of the thermallycompensated biasing device and the power transistors. At best the biasing device can be thermally bonded to the power transistor case. More usually it is bonded to the heatsink, but there is no way it can simultaneously sense the actual junction temperatures of all the power transistors. Under rapidly-fluctuating dynamic signal conditions, the junction temperatures may be wildly different from each other and from the case or heatsink temperatures, and therefore the biasing may be wrong.

Figure 14 compares the static cross-over distortion of Figs. 2 and 10 when the bias is deliberately set 0V5 too low. Dynamic mistracking of the biasing circuit should not introduce audible crossover distortion in an NDFL amplifier.

One final point. The NDFL technique maximises the return difference (and hence minimises distortion components) at frequencies up to $1 / \tau_{0}$. Above this frequency the return difference falls away rapidly, and distortion rises. Choosing $1 / \tau_{0}$ to correspond to 20 kHz winimises audible-frequency distortion, but does not minimise ultrasonic distortion.

For example, a common specification for audio power amplifiers is their THD at 20 kHz . The harmonics of 20 kHz lie at $40 \mathrm{kHz}, 60 \mathrm{kHz}, 80 \mathrm{kHz}$, and so on. All are ultrasonic (and hence inaudible) and the NDFL technique does not minimise them. A measurement of THD at 20 kHz may therefore give a quite misleading indication of an NDFL amplifier's audible performance. Valid objective tests include the SMPTE and CCIF tests for two-tone intermodulation distortion, the proposed IEC test for TIM (14), Cordell's proposed three-tone test for TIM (15) and the proposed test for input-output intermodulation distortion IOD (6). The distinguishing feature of all these tests is that they measure the distortion at audible frequencies.

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## ORGAN part 3

## Design by Richard Watts.



Fig. 1 Circuit diagram of the rhythm section of the Victory organ, including the handclap generator.

This month we conclude the description of the organ circuitry ready for the constructional notes next month. Before doing so, some minor notational changes are required due to continuing development work on the prototype and the consequent re-allocation of certain switches. In Fig. 1 of the February article, the terminal marked R15 (by D6) is now C17, and the terminal marked C15 in Fig. 4 of last month's article should be connected to +12 V , not +5 V . Mark these changes, spread out the two previous issues for reference, and away we go with the rhythm unit.

## I Got Rhythm

The heart of the rhythm unit is the M258 ROM (IC24). This has a maximum capacity of 8 K , organised as 16 rhythms of 32 counts with 16 outputs. In fact this is not all used, as some rhythms have only a 24 count requirement. All inputs to and outputs from the IC are active low.

When the rhythm on/off switch is on, connector C13 is taken low. This low is applied to inverter IC21e, which causes a high to be input to pin 26 of the ROM. Although this is a bidirectional connection capable of outputting sync pulses, it is used in this

case as the reset input. The low on terminal C16 is also taken to pin 1 of IC22a. This NOR gate, together with IC22b, R169, R170, C64 and the tempo potentiometer (which is connected a across terminals R9, R10) form the rhythm clock generator. The clock input is supplied to pin 27 of the M258. Selection of a rhythm is achieved by switching four input lines (pins 7, 19, 9 and 20) which the IC then decodes using an internal four-to- 16 line decoder.

The 16 rhythms are available from nine switches such that each of the first eight is used for two rhythms, called up by the ninth switch (called program $1 / 2$ ). The eight rhythm switches are mechanically latched and self-cancelling on a new selection. The switches connect +5 V to each of the terminals R2 to R8 which connect to triple three-input NOR gate IC25, used here as an eight-to-three line encoder. Notice that the leftmost rhythm switch does not connect to any points, but due to the mechanical cancelling action of the switches removes +5 V from any of the NOR gate inputs, thus giving the eighth state of all outputs high. The program selector switch provides the fourth bit of information to pin 20 of IC24. The final input requirements are that pins $28,14,3$ and 1 be at +5 V and pin 2 at ground. This covers the input requirements for the M258: now to the outputs.

Timing within the M258 is arranged such that each count of a rhythm lasts for two cycles of the clock input. The 16 active-low outputs normally remain active for one clock cycle only, but eight of them have the option that they may remain active for the whole count (two clock cycles). This gives the facility of selecting whether the output is pulsed per clock cycle or can be either high or low. In the first state the output must always return to high; in the second it may not, depending on programming. In this ETI organ application pins 5 and 11 are programmed in the second manner: their full purpose in life will be described later.

Output pins $17,21,23,12,18$ and 16 are all used to control the automatic bass patterns when the walking bass 1 and 2 features are selected. If walking bass 1 is selected, point C9 is taken low and enables the NOR gates on the outputs from pins 17, 21 and 23. These gates act as inverters and supply positive pulses through diodes D53-55 to pins 8 -10 of both the M108 and M208 ICs.


Fig. 2 Connection details for the rhythm switch.

The effect of this is to cause any bass note being played (from either the lower keyboard or the pedals) to be varied in accordance with the codes appearing on pins $8-10$. When walking bass 2 is selected, point C9 is pulled high through R220 to +5 V since the grounding by the walking bass switch is cancelled; point C11 is also taken low. This now enables the outputs from the other set of M258 pins (12, 16 and 18) to control the bass note.

Triggering for the bass envelope is is developed in either of these modes from pin 12 of the M108/208 which provides an active-low pulse named TDB (trigger decay bass) every time the bass code changes. This pulse is inverted by either IC5b or IC5d, which are enabled since the selection of either walking bass 1 or 2 removes the high ( +12 V ) from point C10. This turns off IC7a, thus letting the input of IC6a go high and hence its output low. This low enables the NOR gates as inverters and allows them to pass trigger pulses to the bass output gating circuits. If both walking bass 1 and 2 are switched off while the rhythm is still running, the outputs from the M258 are prevented from passing through the NOR gates (IC27a-d and IC22c,d) and their outputs will be low. Point C10 going high also enables other triggering arrangements for the bass since the TDB signal will no longer be present. If either walking bass 1 or 2 is selected and the rhythm switched off then all the outputs from the M258 will be disabled (high) and therefore all the outputs from the NOR gates will be low. Pin 8 of the M108/208 is now taken high by point C 16 from the rhythm on/off switch via D59.

Bass trigger changeover is made by point C17 going low (through the rhythm on/off switch) and pulling the input to inverter IC6a low via D6. Point C17 going low also causes IC2a to turn off momentarily due to the coupling by C 8 . This briefly removes $\overline{\mathrm{FS}}$ from B 6 ,
latched output at pin 7 of the M208. This is necessary to ensure that, when the rhythm is stopped, the pedals do not continue of their own accord. This momentary disable circuitry is also used on the input side of the M108 to cancel any memorised chord if the rhythm is switched off. It is worth pointing out here that the M258 and the NOR gates supplying the bass codes run from +5 V while the $\mathrm{M} 108 / 208$ run from +12 V . This does not cause a problem since the bass code inputs of the M108/208 will accept anything from +4 V to +18 V as a high level input on these pins when running from +12 V itself.

The M258 output pin 24 is a downbeat indicator and goes low on the first : count of any selected rhythm. This signal is connected to four parallel inverters from IC21 to provide current drive to the LED downbeat indicator. Output pin 8 was discussed last month with the lower manual rhythm guitar voice and is used to trigger this voice. The length of decay for the rhythm guitar is determined by the state of output pin 11: this output is one which has the steady state output programmed. If this pin is high the discharge time of C54 is long, thus giving a long chord from the guitar. If the pin is low the discharge time is shortened by putting R145 across C54 and thus giving the short guitar chord. This feature is very important in providing a good, musically interesting backing, and emulates the 'real' guitarist's performance more correctly.

## Rhythm Voices

Eight different 'instruments' can be triggered by the M258 outputs. These are cymbal long, cymbal short, cymbal strike tone, handclap, tom-tom, clave, snare drum and bass drum. The bass drum, clave and tom-tom all use similar damped oscillator circuits but with different resonant frequencies. As an example of their operation, the clave voice is triggered by pin 10 of IC24. The
oscillator comprises IC25a, R182,183, C68 and C69, the resistors and capacitors determining the frequency of oscillation. Normally the circuit does not oscillate but when a low appears on pin 10 of the M258 a pulse is generated by C67, D46 and R181 which causes the circuit to oscillate momentarily. -This damped oscillation synthesizes the sound of the clave and is fed via R225 to IC12b, which is the rhythm mixer/preamp. After decoupling by C88 and the output impedance raised by the series resistance R231, the rhythm sounds pass to the rhythm volume control and then to the final mixer/preamp. Q18 is connected to the rhythm on/off switch so that with the switchoff, Q18 is turned on and shorts out any residual rhythm noise.

The cymbal voice is more complex than any other because of its importance in rhythms. It is developed by triggering a mixture of two noise sources and, optionally, a cymbal strike tone generator which also doubles as cymbal voicer. The first noise source develops white noise and comprises the reverse-biased base-emitter junction of Q19 connected to Q20, which is the amplifier. The output level of this circuit is adjusted by PR7 and is coupled through R191 and C72 to the base of Q15.


Fig. 3 The wiring of the expansion socket.

The other noise source is responsible for the metallic 'ring' content of the cymbal sound and comprises hex Schmitt inverter IC28 and quad EXOR gate IC29. IC28 is used to form six oscillators, which are EXORed in various combinations and and finally mixed together and coupled via C76 and R197 to the emitter of Q15.

The cymbal trigger pulse from pin 3 of the M258 passes via C70 and causes Q15, normally biased off by R190, to conduct and output a mixture of the two noise sources to its collector, where it is filtered by IC25b. The duration of the cymbal sound is largely determined by how long C71 in the base circuit of Q15 remains discharged. If the M258 output on pin 5 is not active, ie is high, C71 will be charged fairly quickly via R185 (22k) and D48 in parallel with R190. If, however, pin 5 is low, C71 will take much longer to charge through R190 (4M7) alone. These two time constants give the long and short cymbal sounds. Output pin 5 is the other output referred to which does not always return to its high state with each clock cycle. The cymbal strike tone is derived from output pin 4 and makes use of the cymbal filter as a damped oscillator. By careful programming of the ROM, excellent hi-hat effects can be produced in conjunction with the short cymbal sound.

The snare noise trigger is from pin 22 of the M258 and is inverted by IC21f. This positive-going pulse is then coupled via C78 to the emitter follower Q16: D50, R202, C79 and R203 provide shaping for the pulse which is fed to the base of Q17. This transistor is also fed with white noise from Q19, 20 and is normally off: hence no snare no ise. When the trigger pulse arrives, Q17 is switched on and amplifies the white noise, which then appears on its collector. Thus the snare drum noise is developed from a passive strike tone, resultant from the fast rise time of the trigger, together with the white noise. The drum part of the snare is produced by the tom-tom generator IC26a.

The last voice on the rhythm unit is the handclap generator, which is gradually appearing on commercial units and will become an industry standard during the year. The generator is enabled by taking pin 2 of IC30a (a NOR) low. Note that IC30 is connected to $a+12 \mathrm{~V}$ supply, which is necessary for one of the gates to be used else-
, where on the organ. (This highlights one other useful feature of the M258 - all


Fig. 4 Circuit diagram of the PSU and amplifier (component numbers restart from 1).
outputs are open-drain and can therefore be pulled up to whatever voltage is required. A quick look at the schematic will show this feature used to effect.) The positive-going output from IC30a pin 3 is fed to Q21, which gates white noise from Q19,20, and also to IC30b,c which are connected as a monostable. The rising and falling edges of this monostable will trigger the damped oscillator of IC31a, producing two beats of the handclap. This is overlayed with white noise from Q21 and filtered by IC31b. Both sound components are summed in the rhythm mixer IC12b.

## Amplifier/Power Supply

The power supply is of a standard configuration, the $\pm 18 \mathrm{~V}$ supplies being used for the amplifier IC. The 12 V supply is obtained from a 7812 regulator IC fed from the +18 V rail and the +5 V (used only in the rhythm section) is derived from the +12 V by Q1.

The power amplifier is an integrated circuit type TDA2030L. Its output is fed to a four ohm loudspeaker via a headphone socket which breaks the connection to the speaker when
used. Signal reduction for headphone use is made by a 100 R resistor attached to the headphone socket.

The input to the power amplifier is made via IC3c (part of a 4016) which is used to keep the audio line disconnected for a short period immediately after switch-on. This eliminates spurious outputs from both the generator ICs and the rhythm unit caused by switching transients. The audio line both into and out of IC 3 c is biased at +6 V by R 4 and R 7 , fed from the junction of R8,9 and C9. This is necessary since IC3 is running from a single supply.

At switch-on, IC 3 c is off because pin 5 is tied to ground through R6. C7 is allowed to charge through R5 until the voltage on C 7 is sufficient to turn on IC3a and IC3b, which are connected in parallel. This then applies the +12 V to pin 5 of IC3c, turning it on and connecting the audio line to the power amplifier.

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Prices for kits of organ parts are available on application to Leighton Electronic Services, 17 Bridge Street, Leighton Buzzard, Beds LU7 7AH (tel. 0525 382504). A demo cassette is available for $£ 1.95$.

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# DESIGNER'S NOTEBOOK 2 

# Our second Notebook topic is that much-misunderstood beast, the switched mode power supply. P.S. Wilson of International Rectifier gives a step-by-step explanation of the various types and design examples. 

The term 'switching mode power supply' is used to describe DC-to-DC converters and AC-to-DC converters which operate on a switching principle. Using switching techniques, voltage step-up and voltage inversion can be achieved, as well as the more common voltage step-down function. The advantages of using switching techniques over a linear solution are the reduction in the size of components (such as power transformers and output filter capacitors) by operating at high frequency, and dramatic improvements in efficiency, since the power elements are either fully turned 'on' or 'off' and do not operate in the linear mode. The disadvantages of switching mode solutions are increased noise and radio frequency interference (RFI) which is generated during the switching transitions. Circuit complexity is increased, as in addition to the control circuit, a power switch, rectifier, high frequency transformer or inductor and drive circuitry is required.

Switching mode solutions are, however, costcompetitive with linear power supplies in off-line applications at and above the 100 W level. Switch mode power supplies are also used at lower power levels in DC-to-DC converters where there is a special requirement such as high efficiency, for example in solar energy conversion, or small size for mobile communications equipment.

## Basic Principles

The circuit and waveforms in Fig. 1 illustrate the basic principle of the switching mode supply by comparison with a linear regulator. The circuit configuration shown is for a voltage step-down conversion. When switch SW1 is closed the input supply voltage is applied to the inductor L1, and current flow in the inductor will rise with a ramp waveform, charging capacitor C1 and also supplying the load connected at the output of the supply. When SW1 is opened (equivalent to turning off a semiconductor device) the inductor current diverts into the rectifier, D1. The voltage at circuit node ' $P$ ' falls instantaneously to a rectifier forward voltage drop below the 0 V line, and the current flow in the inductor follows a negative ramp waveform. The power supply load is now supplied both from the inductor and from the output capacitor, C1. When SW1 again closes, D1 becomes reverse biased and the inductor is again connected to the input supply. In the steady state condition, the positive volt-second product applied to the inductor must balance the negative volt-second product applied when the rectifier conducts. The voltage at the output of the supply is regulated by controlling the 'on'/'off' ratio, or duty cycle of the switch SW1. Because the switching element is either 'on' or 'off' the power loss is small and the efficiency of the supply approaches $100 \%$.

Comparison with the linear regulator (Fig. 1b) shows an efficiency of approximately $V_{0} / V_{\text {IN }}$.

Figure 2 illustrates how, by rearranging the circuit elements SW1, L1 and D1, voltage step-up and voltage inversion can be achieved. Provided that the current flowing in L1 does not fall to zero between the conduction phases of SW1, the circuit configuration in Fig. 2a can be said to provide a 'non-pulsating' output current. This feature allows low output ripple voltage to be achieved. The configuration shown in Fig. 2b, however, will exhibit a 'pulsating' output current as the inductor current is diverted from the output when SW1 closes. The input current flow, however, can be arranged to be non-pulsating, so reducing the ripple voltage on the input supply. The voltage inverting circuit, Fig. 2c has pulsating current waveforms at both input and output terminals.

To overcome this apparent restriction on operating mode, transformer-coupled circuits can be used. The voltage conversion achieved is then defined by the transformer turns ratio and the polarity of the output rectifiers. Figure 3 illustrates the most common circuit configurations in use today. In addition to increasing flexibility, the transformer-coupled solution offers the option of an isolated output supply.

Figure 3 a shows a transformer-coupled circuit configuration analagous to the voltage step-up circuit in Fig. 2b. The dots against the transformer windings indicate



Fig. 2 Circuit configurations to achieve different $V_{1 N} / V_{\text {our }}$. (a) Voltage step-down. (b) Voltage step-up. (c) Voltage inversion.
their polarity. SW1 and D1 conduct during opposite phases of the drive signal, that is, they conduct nonsimultaneously.

Figure 3 b is analagous to the voltage step-down circuit in Fig. 2a. SW1 and D1 conduct simultaneously. During the switch 'off' time, current flow in L1 is diverted through a second rectifier, D2. The purpose of the third winding on the transformer is to reset the magnetic core of the transformer during the switch 'off' time. If this was not done, the magnetic core would become DC-biased and may saturate, resulting in poor performance (low efficiency and high pulse currents in the primary winding and SW1).

Figure 3c, the push-pull converter, is again analagous to the circuit in Fig. 2a. The difference between this circuit configuration and the forward converter shown in Fig. 3b is that the transformer is biased bidirectionally by switches SW1 and SW2 which conduct alternately. Consequently the 'reset' winding shown in Fig. 3b is not required. The output filter components L1, C1 operate at twice the switching frequency, allowing some size reduction. Each switching device (SW1, SW2) passes only one half of the output current divided by the transformer turns ratio, n. Consequently this solution may be preferred to the solution shown in Fig. 3b at higher power levels (greater than 100 W ).

Figure 3d ịlustrates a type of push-pull converter commonly used in off-line applications. Its main advantage, apart from the automatic resetting of the transformer core, is that the maximum voltage seen by either switch does not substantially exceed the input supply line voltage. Consequently, 400 V switches can be used when working directly from the rectified 240 V mains supply. Capacitor C2 prevents DC biasing of the transformer core which may otherwise arise through asymmetry in the switching waveforms of SW1 and SW2. Capacitors C3, C4 effectively divide the supply to the transformer by two.

Finally, Fig. 3e represents a further modification to the
basic forward converter in Fig. 2a. The capacitors C3, C4 in the previous figure are replaced by two more switches; SW3, SW4. DC magnetisation of the transformer core is prevented by capacitor C2. The full supply voltage is now applied across the transformer primary as switches SW1 and SW4 and then SW2 and SW3 close simultaneously. The maximum voltage applied to any of the switches will not exceed the supply voltage significantly. This 'full bridge' configuration is used in high power switching power supplies where the size and cost of capacitors C3, C4 to replace the switches would be prohibitive. The same circuit configuration is used to drive reversible DC motors.

Switching power supplies can use capacitive elements as the energy transfer medium, rather than magnetic components which have been considered so far. Generally, capacitive circuits are limited to use at high frequency (greater than 10 kHz ) and relatively low power levels. Figure 4 shows a capacitive voltage multiplier and a voltage inverting circuit. An example of such a circuit, which is available in integrated form, is the ICL7660 from Intersil Inc.

Operation of the circuit in Fig. 4a is as follows. Initially, SW2 is closed and SW1 'off'. Capacitor C1 is charged to $V_{\text {iN }}$ through rectifier D2 and SW2. SW2 then opens and SW1 is closed. This causes the voltage seen at the anode of rectifier D 1 to rise from $\mathrm{V}_{\mathbb{N}}$ to a value determined by the relative sizes of capacitors $\mathrm{C} 1, \mathrm{C} 2$. When $\mathrm{C} 1=\mathrm{C} 2$, the voltage at the output of the supply will rise toward $2 \mathrm{~V}_{1 \mathrm{~N}}$. SW1 is then opened and SW2 closed to repeat the cycle.

The circuit in Fig. 4b operates on the same principle. SW1 charges capacitor C 1 to $\mathrm{V}_{\mathbb{I N}}$. SW2 is then closed, taking the cathode of rectifier D1 negative to a value determined by $\mathrm{C} 1, \mathrm{C} 2$. Capacitor C 1 is then recharged through SW1 and D2.

## What Semiconductor?

As is inferred by the name 'switching mode' the semiconductor devices required for this application are primarily switching devices. The requirements for the switches are:

- Low conduction losses.
- Fast switching times.
- Voltage rating to match the circuit configuration and input supply voltage.
- Ability to withstand an overload.
- Good safe operating area (SOA) when used in an inductive load switching circuit.
These requirements can be met, largely, by a wide variety of bipolar transistors, thyristors and SCRs. More recently, power MOSFETS have been introduced with voltage and current ratings suitable for use in switching power supplies (current ratings to 40 A and voltage ratings to 500 V ). These devices offer substantial advantages over bipolar transistors in the following areas:
- Low gate drive power - simplifying the driver stage.
- Fast switching times which are largely temperature insensitive - allowing operation at frequencies greater than 50 kHz .
- Good overload capability - the device is not limited by gain or second breakdown. Power dissipation is the limiting factor.
- The positive temperature coefficient of 'on' resistance assists current sharing when devices are parallelconnected to achieve higher current ratings.
Rectifiers for switching power supplies have similar requirements to the switching devices. The type of rectifier used is governed by the circuit application as indicated in Table 1.

Monolithic switching regulator circuits of limited output power capability are available (Fairchild uA78S40,


Fig. 3 Transformer-coupled switching mode circuits.
(a) Flyback converter. (b) Single-ended forward converter. (c) Push-pull converter. (d) Half bridge circuit. (e) Full bridge circuit.

Texas TL497A), and the trend toward integrated power functions can be expected to accelerate. There are a number of integrated control circuits for switching mode power supplies available, allowing the control circuit board complexity to be reduced. The functions available in these circuits include: an oscillator, a voltage reference, a regulator, a current limit function and a driver stage. Some of the more common devices are: Philips TDA1060 which is pin-for-pin compatible with the Signetics NE5560, the Silicon General SG3524 which is multi-sourced, the Texas Instruments TL494 which is also available from Motorola, Fairchild and Fujitsu (as MB3759) and the Motorola MC3420.

TABLE 1

Application
High Frequency Switching

High Current, Low Voltage Switching

High Voltage Switching

## Magnetic Component Design

Magnetic components are used in the majority of switching mode power supplies. It is, generally, only at low power and high frequency that capacitive circuits can be used. Magnetic components are used not only as high frequency transformers and DC inductors, but also as drive transformers, providing isolation between the control circuit and the power switching elements, and as current sensing elements.

Some of the criteria for the selection of a magnetic component as a high frequency transformer core are:

- Operating frequency range.
- Maximum magnetic flux density.
- Loss coefficient at the operating frequency.
- Available winding area.
- Primary to secondary coupling factor, and isolation. Ferrite cores in a variety of shapes and materials are available. Metal powder cores, laminated and tape wound cores are also available for specialist applications.


## Transformer Design

As an example, consider the design of a switching mode transformer to operate at 50 kHz in a half bridge circuit (refer to Fig. 3d). The input voltage is $310 \mathrm{~V}+5 \%$, $10 \%$ and the output required is 5 V at 40 A .
Step 1. Select a core material suitable for operation at 50 kHz and a core size commensurate with the power loading. Example: Mullard FX3740 core, A16 material; Philips EC52/24/14 core, 3C8 material.
Step 2. Calculate the number of primary turns required to avoid saturation of the transformer core under worst case loading. Check that the worst case core losses do not cause excessive core operating temperature. Check that the winding area is adequate. Check that the magnetising current is less than $10 \%$ of the load current for efficient


Fig. 4 Capacitive converter circuits. (a) Capacitive voltage multiplier. (b) Capacitive voltage inverter.
operation. Example: Worst case loading will occur with maximum input supply voltage and maximum duty cycle for the switches.

$$
V_{I N} \max \frac{\delta \max }{f_{o}}=\widehat{B} \cdot A e \cdot n
$$

where $\mathrm{V}_{\text {IN }} \max$ is the maximum voltage applied to the transformer

$$
=\frac{310+5 \% \cdot V}{2}
$$

$=50 \mathrm{kHz}$

## $f_{0}$ is the operating frequency

$\begin{aligned} & \mathrm{B} \\ & \mathrm{B} \text { is the peak working flux density of the core, at elevated } \\ &= 200 \mathrm{mT}\end{aligned}$ temperature
$=200 \mathrm{mT}$
Ae is the magnetic cross secitonal area of the core $=180$ $\mathrm{mm}^{2}$
n is the minimum required number of turns
Hence $n_{\text {min }}=40.7$ turns
Working at a peak flux of 200 mT , at 50 kHz , core losses are approximately 1 W 8 . This corresponds to a rise in core temperature above ambient of approximately $20^{\circ} \mathrm{C}$. Assuming a conversion efficiency of $70 \%$, the input power requirement is 286 W . The lowest input voltage, applied across the transformer primary is $(310-10 \%) / 2 \mathrm{~V}=139 \mathrm{~V}$. This gives a primary winding current, assuming 0.9 duty cycle, of approximately 2A3. .

Assuming a current density in the transformer winding of $4 \mathrm{~A} / \mathrm{mm}^{2}$, the cross-sectional area of wire used for the primary winding should be $0.57 \mathrm{~mm}^{2}$, corresponding to a wire of diameter 0.85 mm . Assuming a packing factor of two (because a circular cross-section conductor is used) the winding area consumed by the primary winding will be $2 \mathrm{n} \times 0.57 \mathrm{~mm}^{2}=46.7 \mathrm{~mm}^{2}$. The available winding area on the core, after making an allowance for isolation is $304 \mathrm{~mm}^{2}$. The primary winding will take only $1 / 6$ of the available area.

The magnetising inductance of the winding is determined by:

$$
\mathrm{L}_{\mathrm{m}}=\frac{\mu_{\mathrm{o}} \mu_{\mathrm{a}} \mathrm{n}^{2} \mathrm{Ae}}{l_{\mathrm{e}}}
$$

where $L_{m}$ is the magnetising inductance in Henries
$\mu_{o}$ is the permeability of free space $=4 \times 10^{-7} \mathrm{H} / \mathrm{m}$
$\mu_{a}$ is the amplitude permeability of the core $=10^{3}$
$I_{e}$ is the magnetic path length in the core $=105 \mathrm{~mm}$

$$
L_{m}=3.62 \mathrm{mH}
$$

The peak magnetising current is given by the equation:

So

$$
\begin{gathered}
\quad \frac{V_{i n} \min }{2}=\frac{2 \cdot L_{m} I_{m} f_{o}}{\delta \max } \\
I_{m}=\frac{V_{i n} \min . \delta \max }{4 . L_{m} \cdot f_{o}}=86 \mathrm{~mA}
\end{gathered}
$$

The peak magnetising current represents $4 \%$ of the load current, which is acceptable.
Step 3. Establish the transformer turns ratio. Example: The voltage required at the secondary winding of the transformer is a function of the power supply output voltage ( 5 V ), the duty cycle of the switches SW1, SW2, and the voltage dropped across the rectifiers and resistance of the output inductor L1. Disregarding the circuit losses initially, the transformer output voltage can be found by balancing the volt-second products for the output inductor in the minimum input supply condition, when the duty cycle is 0.9 .

$$
\left(V_{x}-V_{o}\right)=\left(V_{o}+V_{f}\right)(1-\delta)
$$

where $V_{x}$ is the transformer output voltage.
$V_{0}$ is the supply output voltage
$=5 \mathrm{~V}$
$\delta$ is the duty cycle
$V_{F}$ is the rectifier forward drop
$=0.9$
$=1 \mathrm{~V}$

$$
V_{x}=5 V 7
$$

To this figure must be added the circuit losses, $V_{F}+I_{0} \cdot R_{L}$,
where $I_{O}$ is the rated output current, and $R_{L}$ is the series resistance of L 1 and the circuit wiring.

A minimum output voltage of 7 V can be used. The minimum input voltage is 139 V , so the transformer turns ratio is 20:1. Assuming a primary winding of 40 turns (marginally below the minimum, resulting in a slightly higher peak flux density, $\widehat{\mathbf{B}}$, which can be tolerated in this example), each secondary winding comprises two turns.
Step 4. Transformer winding design. The correct design of the transformer windings will result in a reproducible and efficient transformer design. The conductor size and placement can have a significant effect on winding losses in a high frequency design. Example: The primary winding consists of 40 turns of 0.85 mm diameter wire, which can be wound in two layers each comprising 20 turns. The available winding breadth on the transformer core is approximately 20 mm after an allowance of 4 mm at either end for isolation. The secondary consists of two windings, each of two turns. The conductor for these windings is in strip form, being 8 mm in width and 0.625 mm thick. The windings are wound side by side on the former. Electrostatic screens and isolation are wound between primary and secondary windings. Worst case windings losses arise at maximum loading. Primary winding loss is 3 W 4 maximum, and the secondary winding loss 1W25 watts maximum. When added to the transformer core losses of 1W8 the worst case transformer loss is 6 W 45 at a core temperature of $100^{\circ} \mathrm{C}$. The transformer is capable of operating in ambient temperatures up to $35^{\circ} \mathrm{C}$ without additional heatsinking. (Core data and ratings are drawn from the manufacturers' literature).

## Inductor Design

The operating conditions of the magnetic core in the inductor are significantly different from those of the switching mode transformer. The core must withstand a DC magnetising field, without saturation. For this reason, an air gap is commonly introduced into a magnetic circuit. This can be either in the form of a single gap introduced, say, in the centre pole of an ' $E$ ' core, or can be a distributed gap throughout the core material. The distributed gap solution presents a lower radiated magnetic field. When a gapped core is used, the magnetic flux is sorted mainly in the gap. There are small flux excursions as the load current ramps up and down. As an example, consider the design of an output filter inductor to be used with the 50 kHz transformer previously designed. The operating frequency will be 100 kHz . The maximum output current is 40 A and the minimum output current for continuous current flow in the inductor is 4 A .
Step 1. Calculate inductance value required, and the energy storage capability required. Example: The minimum voltage applied to the inductor by the transformer secondary winding is 5 V 7 with a 0.9 duty cycle. The current in the inductor can be allowed to rise by 8 A maximum during this time if the current flow is to remain continuous when the output loading is minimum, ie 4 A .

$$
\left(V_{I N} \min -V_{0}\right)=L \min . \quad \frac{l_{L} \cdot f o}{\delta \max }
$$

where $V_{\mathbb{I N}} \min$ is the voltage applied to the inductor $=5 \mathrm{~V} 7$ $V_{0}$ is the output supply voltage $=5 \mathrm{~V}$ Lmin is the minimum inductance value $I_{L}$ is the peak to peak inductor current $=8 \mathrm{~A}$ fo is the operating frequency $=100 \mathrm{kHz}$
$\delta$ max is the switch duty cycle
$=0.9$

## $1 \mathrm{~min}=1.6$ microhenries

The energy storage capability is $L . I_{m}{ }^{2}$ where $I_{m}$ is the peak current flowing in the inductor $=44 \mathrm{~A}$, so $\mathrm{L} . \mathrm{I}_{\mathrm{m}}{ }^{2}=3.1 \mathrm{~mJ}$.

Step 2. Select a suitable inductor core and determine the air gap required (if it is not a distributed gap material). The majority of magnetic core manufacturers provide selection charts/guides for this purpose. Example: Philips core EC35/17/10 with a 0.9 mm air gap will meet the energy storage requirement (equivalent to the Mullard FX3720).
Step 3. Calculate the number of turns required and determine the inductor losses. The core data gives an effective permeability or an $A_{L}$ value (inductance per turn of the coil) for gapped cores, which enables the number of turns to be calculated and rounded up to the nearest half turn. The inductor losses are primarily in the winding and these can be determined using a similar method to that used to calculate the transformer winding losses. Example: For the Philips EC35/17/10 core with a minimum air gap of 0.9 $\mathrm{mm}, 4$ turns are required to give an inductance of 1.6 microhenries. The winding losses can be written as $\mathrm{I}_{\mathrm{eff}}{ }^{2} \cdot \mathrm{~F}_{\mathrm{R}} \cdot \mathrm{R}_{\mathrm{DC}}$ where
$I_{\text {eff }}$ is the RMS current flowing in the inductor winding
$F_{R}$ is a resistance multiplier to account for high frequency operation
$R_{D C}$ is the $D C$ resistance of the winding.
The high frequency impedance of the winding is a minimum for a conductor of thickness 0.57 mm . Making the winding with copper strip of thickness 0.5 mm and width 20 mm gives a $100^{\circ} \mathrm{C}$ AC winding resistance of 0.58 mR . The winding loss is 0W93, resulting in an inductor temperature rise above ambient of $18^{\circ} \mathrm{C}$ when fully loaded.

## Drive Transformer Design

Various approaches to the design can be made, though the choice is frequently restricted by the operating conditions and the drive requirements of the semiconductor switch. Thyristors and power MOSFETS can be driven by pulse transformers. The length of the trigger pulse and the circuit impedance are designed to comprehend the drive requirements of the worst case drive. Bipolar transistors require a continuous base current supply which often results in a larger transformer core being needed. The need for a wide variation in switch duty cycle often results in the drive supplied to the switching device being compromised: the forward base current supplied during long duty-cycle operation may be the bare minimum to maintain the transistor in saturation. At short duty-cycles the base current supplied can be far in excess of the device requirements, compromising its switching performance. This effect is less severe when power MOSFETS are used as the switches, since they do not exhibit storage time effects.

As an example, conside the design of drive transformers for power MOSFETS when used as the switches in the 50 kHz switching mode power supply. A single transformer with two primary and two isolated secondary windings culd be used. A disadvantage of this approach, however, is the absence of negative gate bias to turn off the MOSFETs at any duty cycle other than the maximum of 0.5 , which would give poor noise immunity in normal operation. Instead, separate transformers are used and the magnetising energy stored in the transformer core during the conduction phase is used to assist turn-off. The transformer design is similar to that required for a singleended forward converter, Fig. 3b.

Step 1. Select a suitable magnetic material and core size. Example: The operating frequency is 50 kHz and the average current flow in the windings will be low. A core material with a high permeability is desirable to maintain a low level of magnetising current. Winding area is a significant factor in determining the core size and will depend on the isolation voltage rating desired. For this application consider the Philips core P1418 in 3B7 material, with an $\mathrm{A}_{\llcorner }$
value of $2,200 \mathrm{nH} / 1000$ turns and a total winding area of $9.4 \mathrm{~mm}^{2}$.
Step 2. Calculate the number of turns required for the primary winding and the magnetising inductance and current. Example: To avoid core saturation when operating at maximum duty cycle, with a supply voltage of 15 V , the minimum number of turns required in the primary winding is given by:

$$
V_{\text {in }} \cdot \frac{\delta \max ^{\iota}}{f_{o}}=\widehat{B} \cdot \text { Ae. } n_{\text {min }}
$$

where $\mathrm{V}_{\text {IN }}$ is the supply voltage
$=15 \mathrm{~V}$
$\delta$ max is the maximum duty cycle
$=0.45$
$f_{o}$ is the operating frequency $\quad=50 \mathrm{kHz}$
$\bar{B}$ is the peak magnetic flux density in the core $=180 \mathrm{mT}$ Ae is the magnetic cross sectional area of the core $=25.1$ $\mathrm{mm}^{2}$
$\mathrm{n}_{\text {min }}$ is the minimum number of primary turns
Hence $\mathrm{n}_{\text {min }}=30$ turns
The magnetising inductance, with $n$, the number of turns equal to $n_{\text {min }}$ is given by:
where:

$$
n_{\min }=10^{3} \sqrt{\frac{L_{M}}{A_{L}}}
$$

$\mathrm{L}_{M}$ is the magnetising inductance in millihenries
$A_{L}$ is the inductance factor in nanohenries/ 1000 turns
2,200
Hence $L_{m}=2.0 \mathrm{mH}$
The magnetising current at maximum duty cycle is

$$
I_{M}=\frac{V_{\mathbb{I N}} \cdot \delta \max }{L_{M} \text { fo }}=67.5 \mathrm{~mA}
$$

Step 3. Check that the winding area on the ferrite core is adequate. Example: To calculate the winding area required for the primary winding, we must first estimate the average current flow. The current required to drive the power MOSFET IRF720, which would be used in this application, at 50 kHz , is low compared to the magnetising current ( 1.7 mA averaged over a switching cycle). So, the average magnetising current level can be assumed. A suitable wire gauge is 0.1 mm diameter. Because of handling difficulties, a 0.2 mm wire may be preferred. The winding area consumed is approximately $20 \%$ of the total winding area of the transformer. Assuming that the drive transformer has a $1: 1$ turns ratio, giving a $\pm 15 \mathrm{~V}$ gate drive to the power MOSFET, the winding area is adequate, after an allowance for isolation spacing has been made.
Step 4. Calculate the minimum permitted drive pulse for safe turn-off. Example: Because this design relies on the transformer magnetising energy to switch off the power MOSFET, a minimum drive pulse must be defined where by the magnetising energy equals the worst case turn-off energy for the MOSFET. Turn-off energy requirements for the MOSFET $=\mathrm{Q}_{\mathrm{C}} \cdot \Delta \mathrm{V}$ where $\mathrm{Q}_{\mathrm{C}}$ is the maximum gate charge figure.

$$
\Delta V \text { is the gate voltage swing }
$$ Magnetising energy in the transformer

$=\left(\mathrm{V}_{\mathrm{IN}} \cdot \mathrm{t}_{\mathrm{on}} \mathrm{min}\right)^{2} / \mathrm{L}_{\mathrm{M}}$ where $t_{o n} \min$ is the duration of the minimum drive pulse. Equating these figures, assuming $\mathrm{Q}_{\mathrm{C}}=17 \mathrm{nC}$ for the IRF720 device, gives a minimum drive pulse of $\mathrm{t}_{\mathrm{on}} \mathrm{min}=$ 2.15 microseconds, which represents a minimum duty cycle, at 50 kHz , of 0.22 .

In the June ETI we will be publishing a switching mode power supply similar to the half bridge design used for the examples here: the project will look more closely at the functions of the actual controller IC.

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Time was when a maximum-
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interface to control equipment.
Design by Phil Walker. MAX/MIN THERMOMETER

This project can monitor the temperature of its surroundings while storing the maximum and minimum temperatures reached in digital form. While the normal readout is by analogue meter, the data on the maximum and minimum temperature can be read out as two eight-bit numbers, possibly into a micro system or other type of data or control system. The unit will store its information until the mains supply is switched off or the reset button is activated. Switching the readout mode will not change the date.

Units such as this are useful for checking the central heating, making sure that the greenhouse is not getting too hot or cold, weather forecasting, or even checking the freezer. With a few simple mods it would be possible to convert the unit to an under or over temperature alarm and program it digitally. (This is left as an exercise for the reader - please don't write to us!)

## The Circuit

This can be considered as several main blocks. First we have the clock generator which produces a series of narrow pulses at a fairly low frequency. These pulses are deliberately made narrow to avoid the possibility of spurious clock pulses being generated by the comparator circuits when the analogue output voltage from the $D$ -to-A converters changes. These clock pulses are applied to gating circuits which will allow them to go
on to the D-to-A converters only when conditions are correct.

The D-to-A converters used in this project are of a type which contain an internal eight-bit counter. This allows us to make an A-to-D converter with few external components. Moreover we can stop and start the conversion process whenever required.

The method used for A-to-D conversion is to reset the counters to all zeros at which time the analogue output voltage will fall to 0 V , and then supply clock pulses to the counter until the analogue
output rises sufficiently to cause a comparator to change output states and cut off the clock pulses. The analogue output voltage from the $D$ -to-A converter will now match the voltage at the other input to the comparator and will stay at this level until the other input voltage changes in such a way that the comparator changes state again and re-enables the clock pulses to the counter.

The two configurations used in this project both work in this way, except that one D-to-A output is used direct for the ' $M A X$ ' detector


Fig. 1 Block diagram of the max/min thermemeter ('cos it remembers - geddit?).


Fig. 2 Component overlay for both boards.
while the other is inverted, such that it starts at maximum volts and falls towards 0 V as the counter increments. This is used to drive the ' $\mathrm{MIN}^{\prime}$ ' detector circuit. The result of the circuitry is that one D-to-A
output follows and stores the maximum voltage while the other follows and stores the minimum. The other input to the comparators mentioned above is a voltage proportional to temperature.

## PARTS LIST



In the first instance this is generated as a current by a LM334Z IC. The current through this device is directly proportional to absolute temperature. This current is fed into the summing input of an operational amplifier together with a constant offset current derived from the reference voltage source of the D-to-A converter. The resultant current generates a voltage at the output of the op-amp suitable for driving the comparator inputs.

The final part of the circuit is the readout. This is provided by a moving coil meter driven by a high impedance buffer. This can be switched to read 'MAX', 'MIN' or 'ACTUAL' temperatures over the ranges -25 to $+100^{\circ} \mathrm{C}$ or 0 to $+25^{\circ} \mathrm{C}$.

## Construction

Construction of the PCB for this project should cause no problems. The main things to be careful with are remembering to insert the four wire links, the orientation of the ICs, diodes, capacitors etc and BR1. R13 can be either a single 20k $1 \%$ resistor as shown, two 10k $1 \%$ resistors or even an $18 \mathrm{k} 5 \%$ and a 4 k 7 preset. Pads are available on

Fig. 3 Complete circuit diagram.


## HOW IT WORKS

IC3a, R1 and C6 form the master clock circuit, which generates a square wave of around 50 Hz or so. This is differentiated by C7 and R2 and the positive spikes only are passed via D2 on to IC3b and IC3C. Only when the other inputs to these gates are high will the spikes be inverted and passed on to the D-to-A converters, IC4 and IC5, as clock pulses. IC3d, R4, R5 and C8 take the input from PB1 and produce a suitable reset signal for the two DACs. This can, however, be overridden by a direct input via D1 (take terminal low to reset), allowing remote control by a computer, for example.

The D-to-A converters, IC4 and IC5, contain an internal counter which can be used when pin 2 of the device is high. This condition is maintained by R7. The counter is reset by a low on pin 3 and will respond to clock pulses on pin 4. After reset the output from the device is at 0 V : at each clock pulse the output voltage rises by 10 mV to a maximum of $2 V 55$ (another clock pulse at this point will take it back to 0 V ). The output from IC4 is compared with the output from the temperature sensor circuit by comparator IC6c and while it is lower, IC6c output will be high, so IC3b pin 5 will be high and enable the clock signal to IC4. While this condition persists the output from IC4 will rise steadily until it equals
and exceeds the output from the sensor circuit. Now the output from IC6c will go low, IC3b input will be low and no more clock pulses will reach IC4. The output from IC4 will stay at the same level until either the temperature sensor voltage exceeds it again or the rese function is used. The output from IC4 is thus a measure of the maximum temperature reached, since it can only increase unless reset.

The circuit around IC5 works in a very similar way except that its output is inverted by ICGa such that the voltage presented to the comparator IC6d starts at 2V55 and falls to 0 V as the counter in IC5 is incremented. In this case the output from IC6d is high while the output from IC6d is higher than the output from the temperature sensor circuit. This means that the voltage from IC6d will start from 2V55 at reset and fall until it matches the output from the temperature sensor. It will stay at that level until the temperature sensor output falls to a lower level or the reset is operated. This means that the output from IC6d is a measure of the minimum temperature, since it can only decrease unless reset.

The temperature sensor device is an LM334Z. This IC is designed as a constant current device but has a linear
emperature coefficient. In effect the current is proportional to the absolute temperature $\left(0^{\circ} \mathrm{C}=273^{\circ} \mathrm{K}\right.$ or Ab solute). In this circuit R12 supplies a constant 255 uA from the voltage reference terminal of IC5 to the virtual earth (inverting) input of IC6b. The temperature sensor IC8 is set up so that it takes this amount of current at $-25^{\circ} \mathrm{C}$ : this means that the output voltage of IC6b will be $0 \vee$ at this temperature. As the temperature rises the current drawn by IC8 will increase and the output voltage from IC6b must ise so that the extra can be sent through R13. The voltage across R 13 will be directly proportional to the temperature rise. Setting of the sensor current is accomplished by PR2 and R21.

The normal method of indication for this project is by means of a moving coil meter, with SW1 selecting the display of the maximum, minimum or actual temperature. IC7 is normally used as a high impedence buffer but by means of PB2 its gain can be increased to $x 5$ for greater ease of reading in the range of 0 to $25^{\circ} \mathrm{C}$. The sensitivity of the meter is set by PR1.

The power supplies for this project are quite simple but a mains-derived type was felt to be desirable as the drain on the +5 V rail is in the region of 70 mA .
the PCB for all these options.
C1 and C2 may be vertical or horizontally mounted as desired, although we had to make C2 an axial type so as not to foul any of
the components mounted on the front panel of our tight-fit case. Take care to ensure that the mains input to the board cannot touch the rear panel (use insulating tape if
necessary). Use a cable clamp to secure the wire. Wiring to the front panel components is straightforward: the sensor PCB is connected to the main board via a


## OPERATION OF VOLTAGE INVERTER



OPERATION OF

length of cable and a three-pin DIN connected on the front panel. The length of the wire is not critical so long as its insulation is good; however, care must be taken to keep the polarity correct.

For those people using the same meter as us (see Buylines), we've reproduced the artwork we drew for our prototype meter scale at the back of the magazine with the foil patterns (page XX). If you wish you can cut it out (get Mummy to help you with this) and use it to replace the existing scale.

## Setting Up

The Meter Circuit. Zero the meter mechanically with the power off. Connect the input of IC7 (pin 3) to point ' $A$ ' (marked on the overlay diagram at the junction of R10 and R12) instead of to the wiper of SW1, apply the power and set the meter to full scale deflection using PR1. Remove the power and restore the connection from IC7 input to SW1 wiper.

The Sensor Circuit. Ensure that the total value of R13 is twice that of R12. If desired, R13 can be two $10 \mathrm{k} 1 \%$ resistors in series, or an 18 k $5 \%$ resistor and a 4 k 7 trimmer if a 20k $1 \%$ device is not available. Pads have been provided on the PCB for one or two resistors or a resistor and a preset - the alternative positions are shown dotted on the overlay. The theoretical value for R13 is actually $2.016 \times \mathrm{R} 12$ but this sort of value is not easily available.

Connect the sensor, switch on the power and with the sensor immersed in a melting ice and water mixture, adjust PR2 until a reading of $0^{\circ} \mathrm{C}$ is obtained (one-fifth of full scale deflection). The unit should now be ready for use: coverage will be $-25^{\circ} \mathrm{C}$ to $+100^{\circ} \mathrm{C}$ in increments of $0.5^{\circ} \mathrm{C}$ approximately ( 256 steps) for the maximum and minimum functions, while the actual temperature is continuous.


A close-up of the sensor probe; we used a cermet preset for stability.

## PROJECT: Thermometer




Fig. 4 (Above) The pin-out for the ZN425E digital-to-analogue converter.
(Right) Inside the box, you can see how cramped things are, and inexperienced constructors may wish to use a bigger box than the one we specify in Buylines. This is especially the case if you intend to fit some kind of interface socket for a digital readoul of the data, to a control unit, for example. We didn't bother on the prototype.


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# CONFIGURATIONS 

# Power corrupts, and absolute power corrupts absolutely. At least, it can burn out the odd diode or two. This month lan Sinclair examines the area of power supplies and some of the facts you aren't often told. 

Power packs, you might think, are among the simpler of electronic circuits to design, and yet there is probably more cut-and-try used in the power supply section of a circuit than in all the rest of the circuitry that you construct. The reason seems to be a lack of coherent explanations of the action of the reservoir capacitor - only too often you are simply told that it "provides an earth route for $A C$ ripple ${ }^{\prime \prime}$, and no more. We have to start this month, then, by putting that sort of misconception to rights.


Fig. 1 Simple half-wave rectifier circuit with no reservoir capacitor. The waveform is unidirectional, but certainly not what we would call DC.

Consider for the sake of simplicity, a half-wave rectifier circuit and a load (Fig. 1). The waveform across the load will consist of about half of the input waveform, the positive half in this example because of the way we have chosen to connect the diode - reverse the diode and you will select the negative half of the wave. This type of output is called a unidirectional wave - the peaks are in one direction (positive) only, with no negative peaks - but it isn't exactly anyone's idea of DC. A DC voltmeter connected to the load of this circuit reads what DC voltmeters always read, the average voltage, which is around $\mathrm{E}_{\mathrm{o}} / \pi$; approximately $0.32 \mathrm{E}_{\mathrm{o}}$, assuming that the diode is 'perfect' in the sense of having no forward voltage drop across it. We can allow for the forward drop, which can't be neglected if the output voltage is low, by subtracting its value from $E_{0}$, the peak $A C$ input. This is only an approximation, but it is good enough for practical purposes.


Fig. 2 A half-wave circuit with a reservoir capacitor added. The capacitor charges to the peak voltage of the input wave, and the charged capacitor supplies the load while the diode is reverse-biased.


Fig. 3 This shows why the peak reverse voltage on the diode is doubled when a reservoir capacitor is used.

## Bring On The Reserves

Now when a reservoir capacitor is connected to the circuit (Fig. 2), things change considerably. To start with, imagine that the load resistance is very high, so that only a small amount of current is being taken. Instead of the rectifier conducting for the whole positive cycle of the AC wave, it now conducts only for a tiny fraction of the time of the wave, right at the peak. The reason is that the first


Fig. 4 The waveform of ripple, caused by the time constant of the reservoir capacitor and load resistance.
half-cycle, when the supply is switched on, will charge the reservoir capacitor to the peak positive value of the AC wave, less the forward diode drop, and when the AC input at the anode of the diode drops below this value, the diode will cut off. From this moment until the next positive peak of the wave comes along, all the current that is supplied to the load is supplied from the reservoir capacitor, which is why it's called a reservoir! Far from just being a bypass for $A C$, the reservoir is the main store and supplier of DC to the load.

All the current that dribbles out from the capacitor results in the voltage across the capacitor dropping as its charge is drained, so that the diode has to supply this
charge again next time it conducts. You don't get something for nothing - the diode passes large currents for short time intervals instead of conducting steadily over a half-cycle as it did when no reservoir was used. The overall result is that the diode has to be able to pass peak currents that are many times greater than the average current, it spends most of its time cut off, the maximum reverse voltage across the diode is twice the AC peak voltage (see Fig. 3), and there is a 'ripple' on the output wave which is caused by the drop in voltage as the reservoir capacitory discharges (Fig. 4). The waveform of this ripple is a sawtooth, rich in harmonics, not simply a piece of left-over sine wave as some explanations would hint at, so that it is a potent source of hum interference in the rest of the circuit.

The approximate amplitude (peak to peak) of the ripple is given by $\mathrm{It} / \mathrm{C}$, where I is the average current drawn by the load, C is the size of reservoir capacitor, and t is the time between positive wavepeaks. Using units of milliamps for 1 , microfarads for C and milliseconds for t , we get units of volts for the amplitude of ripple. For example, if you draw 100 mA from a 1000 uF capacitor with a half-wave rectifier for which $t$ is about 20 mS , then the


Fig. 5 A summary of the conditions for common power supply configurations.
ripple amplitude is $(100 \times 20) / 1000$, or 2 V , which isn't exactly negligible. Using a full-wave rectifier, which recharges the capacitor at 10 mS intervals, you get a 1 V ripple. I his tormula isn't toolproof - it applies only when you have the situation in hand, and will give silly answers if the reservoir capacitor is much too small or if the amplitude of the AC input is very small, but it's a good guide to realistic values for power supplies generally.

The voltage output of the circuit with no load current is equal to the $A C$ peak voltage, but as the load current increases, the ripple also increases and the average DC output drops until it can become almost as low as the value you would get with no reservoir, $0.32 \mathrm{E}_{\mathrm{o}}$ for half-wave, and twice as much as for full-wave (bridge or splitsecondary type of circuit). Figure 5 summarises the operating conditions for different rectifier configurations. Ripple, and the drop of output voltage when output load


Fig. 6 An elementary stabiliser - the power transistor in this example would be a medium-power type with a high value of $h_{i f}$.
current is taken, can be minimised by increasing the size of the reservoir capacitor. Obviously, it is also an advantage to have a short time between recharging the reservoir, so that high-frequency supplies need less in the way of reservoir capacitance - one of the many reasons for the popularity of switch-mode power supplies these days.

## A Stable Situation

Another defensive measure is stabilisation. Stabilisation does not mean that some circuit is used which will miraculously bump up the voltage output from the reservoir capacitor, it simply means making the best of what you have. Suppose you have a nominal 8 V supply, and that at the full planned output current of 150 mA it can have a 2 V peak-to-peak ripple. This value implies that the voltage will drop momentarily as low as 6 V twice on each AC cycle, assuming that full-wave rectification is used, so that if we use only 5 V of this supply, these changes caused by ripple will not affect the 5 V output at all. This is the action of a stabiliser - it's a circuit which is a voltagedropper, but arranged so that the drop is variable, keeping the output voltage constant while the input voltage varies.

A stabiliser has to operate so as to fulfil two requirements. First it must keep its output voltage constant as the input voltage varies, and second, it must keep the output voltage constant as the load current varies. The two may sound identical at first glance, but they are not - the first calls for the output to be constant while the voltage across the stabiliser is varying, the second calls for the combination of the stabiliser and the rest of the power pack to have almost zero internal resistance.

Figure 6 shows a very basic form of stabiliser. The voltage at the output is set by the value of the zener diode, and because of the voltage across the base-emitter of a transistor, the output voltage will be around 0V6 less than the zener diode voltage. This should ensure that the voltage of the output is stabilised against changes at the input resistances of the order of a few milliohms can be ob-


Fig. 7 A block diagram of the comparator type of power supply stabiliser. This type is rarely built nowadays because of the ready availability of IC equivalents.
tained using circuits of this type.
crease to some extent as the load current increases. Nevertheless the stabilisation is better than it would be in the absence of the circuit (something wrong if it were not!), and can be improved by amplifying the signal to the base of the regulator transistor - a variation on the circuit is shown in Fig. 7. The output voltage is compared with the zener voltage, and the output of the comparator is used to control the base of the regulator transistor. Very low output resistances of the order of a few milliohms can be obtained using circuits of this type.

I've drawn the circuit as a block diagram because it isn't very often nowadays that we have to build stabilisers with separate components. The reason, of course, is the
ready availability of IC regulators, particularly the 78
series. These take advantage of being ICs (so that circuit complications are not a problem for production, only for design) to incorporate features such as current foldback, meaning that the current will be regulated if there is any risk of over-dissipation. This ought to prevent overload and give these regulators a very long life - I say ought, because in my experience these regulators quite frequently fail, and I suspect that the fold-back arrangements are not always completely effective.

The 78 series covers most of the 'popular' supply voltages, but if we should want an odd value then a modification to the circuitry, as shown in Fig. 8, can do the


Fig. 8 Varying the output voltage of an IC stabiliser. A variable resistor is illustrated, but a fixed value resistor could be used once the correct value has been established.
needful, at the expense of a slight loss in stabilisation. Similarly, if we want a lot more current from the output than the normal 78 series can supply, then we can use the IC to control an external transistor, as shown in Fig. 9. Circuits like these can cope with about 99 per cent of our needs.

## Switching The Subject

Having mentioned switch mode power supplies, however, I feel I should explain further because, unless you follow the development of TV circuitry, you may not have come across details of them (though a switch mode supply was used in the venerable Apple 2 computer, and a switch mode supply is now used in the BBC computer atter early users complained that the old version burned the varnish off their tables). Basically the principle is to


Fig. 9 Increasing the current-handling capability of an IC stabiliser. The stabiliser handles the rated current, and any amount beyond this value is handled by the auxiliary transistor circuit, preserving voltage stability.
dispense with a mains transformer, and rectify the mains voltage so as to produce a high voltage DC. By dispensing with the resistance of a mains transformer, and by using a reservoir capacitor of surprisingly modest capacitance (but rated for 500 V !), this supply voltage can be quite stable. It is then applied to a switching circuit which charges a capacitor several thousand times per second and discharges it just as frequently into the primary of a transformer which, because it operates with highfrequency signals, can be small and well-insulated. The outputs of this transformer are rectified, and need only small reservoir capacitances because of the high frequency that is used. There is no need for a stabiliser of the oldfashioned wasteful type either, because the output voltage can be sampled by a comparator, and the output of the comparator used to alter the switching times. The idea is that if the output voltage drops, the switch can spend more time passing current into the primary of the transformer; if the output voltage is too high, the switching circuits cut off earlier. There is no waste involved - what is not used is held in the reservoir capacitor ready for the next switching operation.


Fig. 10 An outline of a switched mode power supply. No values are shown, because the transformer is a critical component and the other circuitry can be obtained in IC form.

The main advantage is that the supply runs astonishingly cool, with no huge heatsinks needed for the regulator. The advantages for TVs and computers are obvious - 1 remember one computer which left scorch marks and which could have served as a sandwich toaster. Another advantage is that no AC voltage adjuster is needed - whatever the mains voltage happens to be will be compensated for by the switching process, and there are ICs which will take care of the whole operation. For a more detailed description of the operation of switched mode power supplies, see Designer's Notebook on page 63.

One point of caution concerns servicing. If you are working on a switch mode power supply, remember that it uses high voltages, and that part of the circuit is always live to the mains when it is operating. On many TV receivers, in accordance with the belief that a designer worth his salt will make the inside of a TV as dangerous as possible in order to kill off amateur mechanics, the whole chassis is live or at least not isolated from the mains. The growing trend to make TVs in monitor form so that they can be connected directly to video recorders instead of by the ridiculous method of re-modulating the signal may at last bring us electrically into line with the rest of the world in this respect.

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