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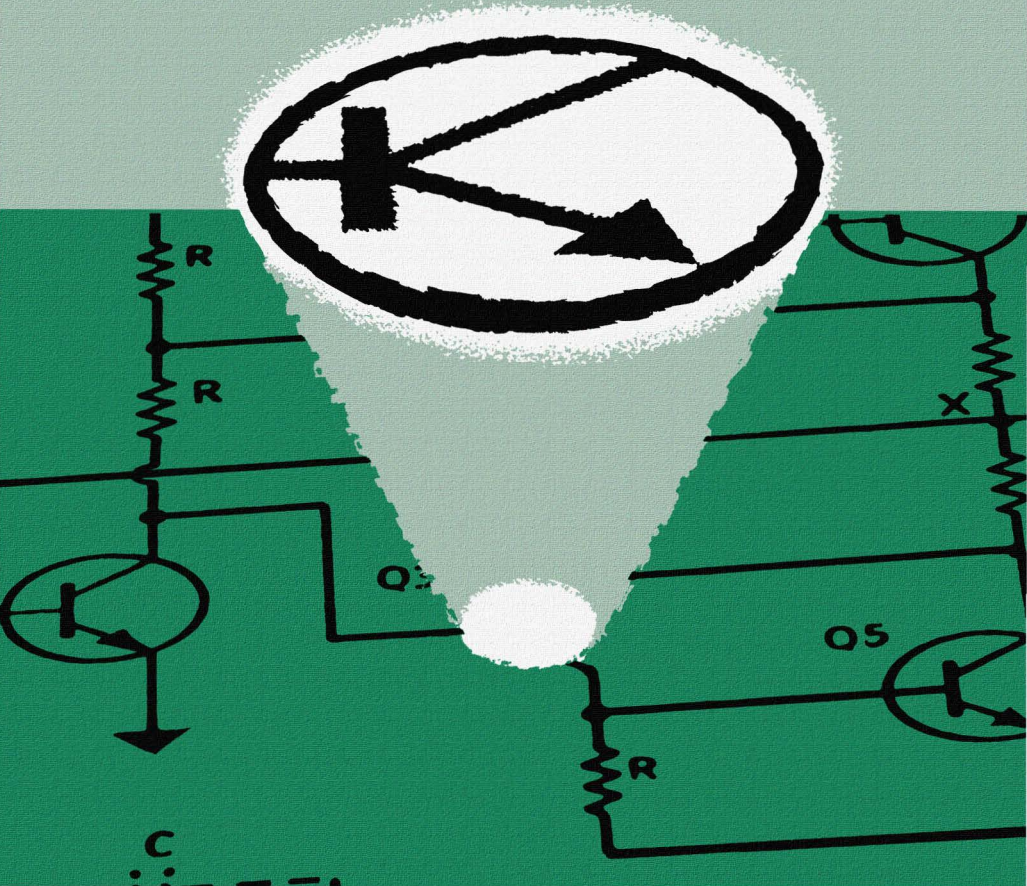
By Mannie Horowitz



PRACTICAL DESIGN WITH TRANSISTORS

by

Mannie Horowitz

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PREFACE

Semiconductor solid-state physics is an exceptionally complex subject. Since all transistor circuit characteristics can be derived from the basic science, this has proven to be a valuable and rewarding, although involved and complex, approach to semiconductor circuit design.

The circuit designer, the senior engineer, the junior engineer, and the technician, are seldom if ever interested in the basic science. They are concerned with designing a diode or transistor into a practical circuit without "sweating out" the semiconductor physics. The performance of the semiconductor in a particular application and its operation in a manner which will insure reliability are his main considerations. This book is aimed at this type of practical circuit designer. It supplies the technician and junior engineer with enough factual material to complete independent valid circuit designs.

The transistor is treated here only as a circuit component exhibiting specific characteristics and limitations. The physics is referred to loosely and only when absolutely required. The discussion centers upon the device and its applications to modern technology.

Derivations of specific formulas are omitted except where continuity of presentation would be disturbed. Equations are derived only when knowledge of the process is useful in circuit designs other than those presented as examples in the text.

As a general rule, the equivalent circuit will be shown or derived and the equations for the circuit will be presented. The manipulation of these equations may be omitted without loss of continuity. The solution will then be presented with an asterisk (*) next to the equation number to indicate that this is the significant equation describing a particular circuit or phenomenon. Examples are presented throughout the text to demonstrate the practical use of the final circuit equation as it is applied to determine specific circuit components and configuration performance. Frequently,

equations are presented to allow the designer to use outdated but currently available transistor data sheets in modern circuit design.

Although aimed at the technician, the solution to the equations and the various examples can be used as a basis for design by the senior engineer working with semiconductors. Much of the text will serve as a useful handbook.

The discussion in the text starts with the semiconductor diode and its many aspects in the modern circuit. Power supplies, filter circuits, and diode characteristics are among the topics. Zener diode regulators, tunnel diodes, and other diodes are also detailed.

In the transistor circuit sections, the dc bias and stabilization conditions are the first consideration. Next, the use of semiconductors in audio and rf amplifiers with a varying input signal are discussed. A chapter is devoted to power amplifiers, due to the light this discussion throws on all transistor applications.

Several chapters are devoted to pulse and switching circuits. This type of circuit is useful in many transistor applications.

A complete chapter is spent on power supply regulators because of their importance to transistor circuitry. This is in addition to the section on zener regulators in the first chapter.

The final chapter is a discussion of silicon controlled rectifiers, unijunction transistors, and the field-effect transistor. Descriptions of the devices and their circuit applications are presented.

A basic knowledge of radio, electronics, and electrical circuits is assumed. Where it is deemed necessary, however, a review of this information is presented in a concise manner.

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Chapter 1

SEMICONDUCTOR DIODES

The diode is the simplest commonly used semiconductor device. Its applications seem to be without bounds, but each diode has specific charactristics and limitations. To extend the versatility, special diodes have been designed for power supply, af, rf, switching, and regulating circuits, as well as for other applications.

The junction diode which consists of two different types of semiconductor materials placed in intimate contact with each other, is the most popular type in use today.

Semiconductors frequently function in low-voltage, low-current applications. Rather than dealing with large quantities such as amperes, small amounts of current such as milliamperes (1/1000 of an ampere) or microamperes (1/1,000,000 of an ampere) are more likely to flow through the circuit. It is necessary to convert readily from, for example, amperes to milliamperes, and back again. Such conversions will be pursued as a matter of course. Exponential notations will be used where convenient. The reader should become familiar with all these common forms.

As for exponential notations, numbers are conveniently expressed as powers of 10. 10^n means 10 multiplied by itself n times.

$10^2 = 10 \times 10 = 100$
$3 \times 10^3 = 3 \times 10 \times 10 \times 10 = 3000$
$6.2 \times 10^5 = 6.2 \times 10 \times 10 \times 10 \times 10 \times 10 = 620{,}000.$

10^{-n} denotes a number divided by 10, n times.

$10^{-2} = 1/(10 \times 10) = 1/100$
$50 \times 10^{-3} = 50/(10 \times 10 \times 10) = 50/1000$
$3.7 \times 10^{-5} = 3.7/(10 \times 10 \times 10 \times 10 \times 10) = 3.7/100{,}000.$

When numbers with exponents are multiplied by each other, the exponents are added. If numbers with exponents are divided one into the

other, subtract the exponent in the denominator from the exponent in the numerator.

$10^2 \times 10^3 = 10^5$
$(3 \times 10^2) \times (2 \times 10^3) = 6 \times 10^5$
$(8 \times 10^3)/(2 \times 10) = 4 \times 10^2$
$(9 \times 10^{-3})/(3 \times 10^{-1}) = 3 \times 10^{-2}$.

Several of the exponents have been given special notations. Prefixes added to the basic unit indicate the multiplier of that unit. This multiplier can be expressed as an exponent of 10. Thus, 1 milliamp $= 10^{-3}$ amps; 7 millivolts $= 7 \times 10^{-3}$ volts. Table 1-1 lists the prefixes used in this book.

Table 1-1. Prefixes Used in This Book

Prefix	Portion of Basic Unit	Abbreviation for Prefix
milli-	10^{-3} (1/1000)	m
micro-	10^{-6}	μ
nano-	10^{-9}	n
pico-	10^{-12}	p
kilo-	10^3 (1000)	k
mega-	10^6	M

Since there are 1000 milliamperes (mA) for each ampere, amperes must be multiplied by 10^3 if it is to be converted to milliamperes. Similarly, a millivolt (mV) must be multiplied by 10^3 if it is to be converted to microvolts (μV).

SEMICONDUCTORS

All materials are artificially grouped in categories of conductors, semiconductors, and insulators. Materials that conduct electricity well are copper and silver. These are the most frequently used conductors. Copper has been used as hook-up wire and as the conducting element on printed circuit boards for many years. Silver contacts are commonly used on switches.

Rubber, glass, and amber have been known as good insulators since the early experiments with static electricity. Plastic, cotton, and enamel have been used as insulators to cover wire. For all practical purposes, these materials resist any flow of electrons.

Germanium and silicon are the two basic elements used in most semiconductor devices, and although these semiconductor materials are fair insulators at low temperatures, their conduction increases as the temperature rises.

If a material such as arsenic, antimony, or phosphorous (called impurities) were added to the basic element, extra electrons would move around in the material. The material formed when the impurity is added to the silicon or germanium is characterized by a lower resistance than the pure germanium or silicon. It has an excess of negative charge and is referred to as an *n-type* semiconductor.

Similarly, if indium, aluminum, or gallium is added to the basic element, a shortage of electrons (positive charge) exists in the combined material. This shortage of electrons is referred to as an excess of holes and the material is a *p-type* semiconductor.

The Junction Diode

A junction diode consists of pieces of n-type and p-type semiconductor materials in intimate contact with each other. They form a p-n junction at the surface of mutual contact.

Some of the free electrons from the n-material diffuse or spread across the junction to the p-material. Similarly, free holes enter the n-region and concentrate around the junction as shown in Fig. 1-1, because of the mutual attraction between the charges. The diffusion continues until there is so great a negative charge built up at the junction in the p-region, that it repels the efforts of more electrons from the n-region to wander across the junction. A similar barrier is set up in the n-region to oppose the migration of an excess number of holes across the junction. The region at the junction establishes a state of nonconducting equilibrium.

If a dc voltage source, such as a battery, were connected across the diode, with the n-region connected to the positive terminal and the p-region connected to the negative terminal, the depletion region (the area near the junction with the holes and electrons that have crossed the junction) would be reinforced, and there would be no conduction.

By reversing the connections to the battery so that the n-region is connected to the negative terminal and the p-region to the positive terminal, the electrons from the n-region and the holes from the p-region would receive enough added energy to jump the barrier formed by the holes and electrons in the depletion region, and there would be current through the semiconductor.

From this, two general practical statements can be made which apply to many circuits involving diodes and transistors.

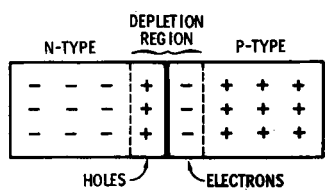
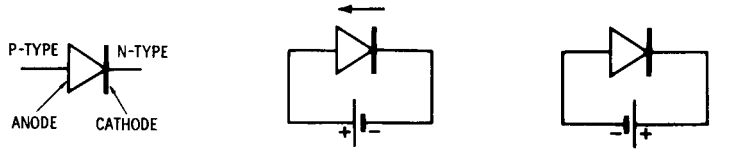


Fig. 1-1. P-n junction diode showing depletion region with holes and electrons that have migrated across the junction.

1. There will be conduction if the n-type material in a junction diode is made negative with respect to the p-type material (forward bias).
2. Conduction will not take place if the n-region is made positive with respect to the p-region (reverse bias). There are two notable exceptions to this rule. For one, there is some leakage current when the diode is reverse biased. A second and more pronounced exception is due to the breakdown voltage of the junction, beyond which conduction will be considerable.

A diode is shown symbolically in Fig. 1-2A. The arrow represents the p-type material and the bar represents the n-type slab. In Fig. 1-2B, the battery is connected so that the diode conducts, while in Fig. 1-2C, the diode resists the current.

It is generally assumed that electrons flow from the negative terminal of the battery, through a load or a semiconductor device, back to the positive terminal. It is this convention of electron current flow that is followed throughout the book. The arrow in the symbol of the diode (and transistor) points opposite to the direction of electron flow. This arrow must be made positive with respect to the bar if there is to be electron current through the diode.



(A) Symbol of a diode. (B) Forward-biased diode. (C) Reverse-biased diode.

Fig. 1-2. Diode symbol and bias conditions.

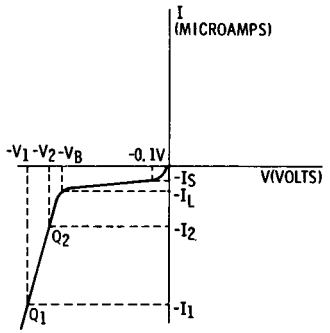
Reverse-Bias Characteristics

The semiconductor diode has many applications. Some of these tasks will utilize the forward characteristics of the diode, while others will apply the reverse properties. These are best described by reference to the characteristic curves which usually show the amount of current through a diode at specific applied voltages.

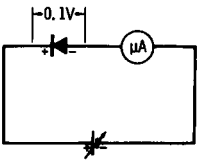
The curve in Fig. 1-3 is a plot of the reverse characteristic of a conventional silicon junction diode. Since the diode is reverse biased (Fig. 1-2C), the curve is in the third quadrant. Here, the voltage applied to the diode, as well as the current through the diode, are negative.

Figure 1-3 illustrates the method for determining the amount of dc current through the diode for a specific applied voltage, V_1, across the diode.

First, draw a vertical line from $-V_1$ volts on the horizontal axis to the diode curve. The line intersects the diode curve at Q_1. Next, draw a hori-



(A) Characteristic curve of reverse-biased diode.



(B) Circuit employed to determine the saturation current.

Fig. 1-3. Describing and measuring the characteristics of the reverse-biased diode.

zontal line from Q_1 to $-I$ microamps on the vertical axis. It intersects this axis at $-I_1$ microamps. Thus, with $-V_1$ volts across the diode, there will be $-I_1$ microamps of current. This construction may be repeated for any applied voltage. It is repeated in the drawing for a reverse voltage of $-V_2$ volts.

The diode has definite dc and ac resistances, which vary with the portion of the curve under consideration. The dc resistance of the diode is calculated using Ohm's law. At point Q_1, $R_{dc} = -V_1/-I_1$. (Be sure that all units are converted to volts and amps before determining the resistance in ohms). At Q_2, $R_{dc} = -V_2/-I_2$. The dc resistance differs at various points on the curve.

Ac resistance is different from dc resistance. Ac currrent and voltage varies with time and through one or more cycles.

Assume an ac voltage is placed across the diode in such a manner as to cause the voltage across the diode to vary from $-V_1$ to $-V_2$. This can be done if the diode is biased by a dc supply to a point midway between $-V_1$ and $-V_2$. How it is accomplished is not important at this time. The only concern is that the voltage will alternate between $-V_1$ and $-V_2$. What is the ac resistance or impedance of the diode for this voltage?

The ac resistance is actually the reciprocal of the slope of the diode curve. It can be determined from the formula:

$$r_{ac} = \frac{V_1 - V_2}{I_1 - I_2} \qquad (1\text{-}1)$$

The ac resistance will vary considerably at different parts of the curve due to changes in the slope.

Several points on the curve characterize the diode when it is reverse-biased.

I_S is the saturation current in the reverse direction and is due to the temperature of the material. This current remains unchanged no matter

what reverse voltage is applied across the diode. The germanium diode saturation current approximately doubles for every 10°C rise in temperature; in silicon diodes, the current just about doubles with every 6°C rise in temperature. The saturation current of silicon diodes is so low, even at high temperatures, that in this respect, silicon is frequently preferable to germanium for use in diodes.

The saturation current can be read from the curve as the current flowing when there is an applied reverse voltage of −0.1 or −0.2 volt. The test setup in Fig. 1-3B can be used in the laboratory to measure I_S. Here, the supply voltage B is adjusted until −0.1 or −0.2 volt is across the diode. The microammeter will indicate the saturation current.

The reverse current does increase in magnitude above I_S as the reverse voltage is raised. The rise is not due to the saturation current. It results from a leakage current caused by surface conditions and impurities. This leakage current, $-I_L$, rather than saturation current, is usually stated on diode specification sheets.

As the reverse voltage is raised, a value, $-V_B$, is reached at which the current begins to increase rapidly in the negative direction. This occurs even when a small negative voltage is applied. $-V_B$ is known as the breakdown voltage. Effectively, the current increases rapidly while the applied voltage remains relatively constant. This is the basis of operation of the zener or avalanche voltage-regulator diode, to be discussed in detail later in this chapter.

In silicon diodes, when the breakdown voltage is above approximately −6 volts, breakdown is caused by an avalanche phenomenon. This is a secondary emission effect due to collision of particles in the semiconductor. Below approximately −5 volts, the breakdown is of the zener type and is produced by a strong electric field in the diode. Between −5 and −6 volts, the breakdown is due to a combination of the two effects. The breakdown voltage is much more abrupt for voltages above −6 volts than when it is caused by the zener phenomenon. Diodes designed primarily for use within the reverse breakdown region, and as voltage regulators, are called zener diodes, regardless of the physical phenomenon.

Many diodes used as power rectifiers do not exhibit sharp breakdown characteristics. Diodes which do have these attributes are referred to as sharp avalanche breakdown devices. They will boast low ac resistance and the ability to dissipate as much power when current flows in the reverse direction as they can dissipate when forward biased. Sharp avalanche diodes are most desirable in any circuit where high transient voltage peaks are present. They should be used in power supplies.

Forward-Bias Condition

The curve in Fig. 1-4 describes the diode when it is forward biased and conducting more readily than in the reverse-biased mode. The current increases exponentially. Up to V_1, the increase in current is very slow,

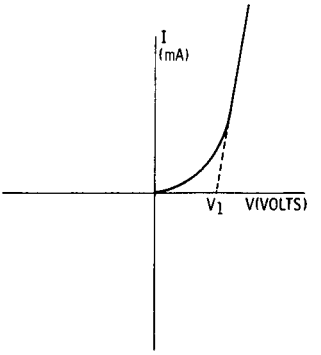


Fig. 1-4. Characteristic curve of a diode in the forward-biased mode.

and may be considered at zero milliamps. After V_1, the current rises rapidly as the voltage applied across the diode is increased. The forward current, I_F, is related to the reverse saturation current, I_S, by the formula:

$$I_F = I_S(10^{5000(\frac{V}{T+273})} - 1) \qquad (1\text{-}2)$$

where,

I_F is the forward current,
I_S is the reverse saturation current,
V is the voltage across the diode when it is forward biased,
T is the temperature in degrees Celsius.

In applying Equation 1-2, it is usually most desirable to determine the voltage across the diode with a specific forward current through the diode. In this case, Equation 1-2 can be transformed to:

$$V = \frac{(T+273)}{5000}\log_{10}\frac{(I_F + I_S)}{I_S} \qquad (1\text{-}3)$$

The constants in the equation are as indicated for Equation 1-2. It is important to remember that the voltage across a forward-biased germanium diode is about 0.1 or 0.2 volt. For the silicon devices, it ranges from 0.6 to 0.8 volt in most instances.

An example of the use of Equation 1-3 involves the circuit in Fig. 1-5. Assume that a diode is connected in series with a 3000-ohm resistor to a 6-volt battery. The anode is positive with respect to the cathode, so it is forward-biased. Assume that there is a 2-microamp saturation current. The diode resistance is negligible, compared to the 3000-ohm series re-

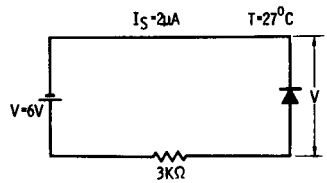


Fig. 1-5. Circuit for finding voltage across a diode when I_S and supply voltage are known.

sistor. What is the voltage across the diode if the ambient temperature is 27°C?

In order to find V, the known quantities must be substituted into Equation 1-3.

T, the temperature, is stated as 27°C, so $T + 273 = 300$.

I_S, the saturation current, is stated as 2 microamps or 2×10^{-6} amps.

I_F, the forward current, can be derived from Ohm's law, $I_F = V/R$. R is the total resistance in the circuit. It is 3000 ohms plus the diode resistance. Since the diode resistance is negligible compared to 3000 ohms, this latter number is effectively the total circuit resistance. V is the supply voltage, or 6 volts. Then the forward current in the circuit is $I_F = V/R = 6/3000 = 2 \times 10^{-3}$ amp $= 2$ mA.

Substituting these values into Equation 1-3 yields:

$$V = \frac{300}{5000} \log_{10} \frac{(2 \times 10^{-3}) + (2 \times 10^{-6})}{(2 \times 10^{-6})} = 0.18 \text{ volt}$$

which is a reasonable value for a germanium diode. This can be derived from the diode curve using the construction shown in Fig. 1-6.

Draw the resistive load line of the circuit in Fig. 1-5 over the diode

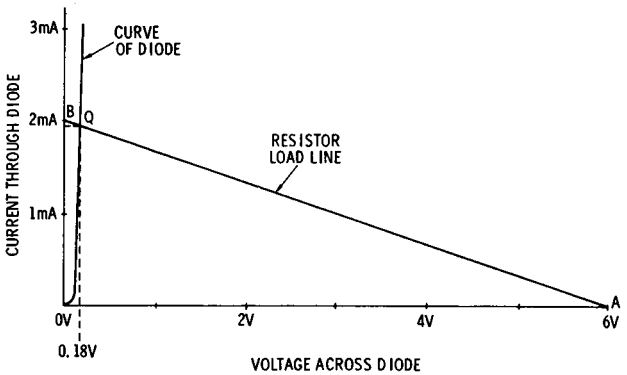


Fig. 1-6. Load line on a diode curve.

curve in Fig. 1-6. This type of construction is actually a plot of two simultaneous equations. One equation is the curve of the diode usually provided by the manufacturer of the device. The second is a curve of the circuit involving the diode, resistor, and battery. The point at which the two curves intersect is the solution to the equations. The actual current through the circuit and the specific voltage across the diode can be determined from this point of intersection.

The load line may be evolved by locating two points on the graph and connecting them with a straight line.

One point on the load line is found by assuming that there is zero current through the circuit, so that the voltage across the diode is the supply

voltage (6 volts in this case). Put a dot on the 6 volts, 0 mA point ("A") on the horizontal axis of the graph.

A second point may be located by assuming that there is zero volts across the diode. This is a point on the vertical axis. In this case, the entire voltage is across the resistor. By Ohm's law, (6 volts/3000 ohms) equals 2 mA. Put a dot on the 0 volts, 2 mA point "B" on the vertical axis of the graph.

Connect points "A" and "B" with a straight line. It crosses the diode curve at point "Q." At "Q," the diode current and voltage are almost identical to the calculated values. The voltage across the 3000-ohm resistor is about $6 - 0.18$, or 5.82 volts.

The slight discrepancy between the plotted and the calculated results is caused by the fact that in the latter case the dc resistance of the diode was ignored. This dc resistance is, by Ohm's law, approximately equal to (0.18 volt/2 mA) = 90 ohms. Hence, the total circuit resistance is about 3000 ohms + 90 ohms = 3090 ohms and the actual current is 6 volts/3090 ohms = 1.95 mA. This is about identical to the current determined from the plot.

The ac forward impedance, if desired, can be derived as discussed above, using Equation 1-1 and the curve in Fig. 1-6. A close approximation to the ac impedance can also be found from the formula:

$$r_{ac} = \frac{8.75 \times 10^{-2} (273 + T)}{I_F} \qquad (1\text{-}4)$$

where,

I_F is the forward current in mA,
T is the temperature in degrees Celsius,
r_{ac} is the ac forward impedance.

The important fact to remember is that the forward ac impedance at room temperature (about 25°C) is:

$$r_{ac} = \frac{26}{I_F} \qquad (1\text{-}5)^*$$

The forward ac impedance increases linearly with temperature.

The diode in the example has a dc forward resistance of 90 ohms at 2 mA, while the ac forward impedance is 26/2 mA or 13 ohms. There is a considerable difference between the two values.

The discussion and equations stated above apply only to junction diodes. The shunt capacitance of this type of device is low enough so that it can be applied to many rf circuits. Detection or rectification applications at frequencies above 10 MHz should use the lower capacity point contact diode which is composed of a metallic point as the anode, in contact with a semiconductor behaving as the cathode. Point contact diodes are characterized by relatively high forward resistance and high reverse leakage currents.

An ideal diode is usually credited with zero resistance when forward biased, and with infinite resistance up to the breakdown voltage when biased in the reverse direction. Resistance, breakdown voltages, etc., are added to the idealized symbol of the diode to generate a practical equivalent circuit. It is this concept of the diode that is applied to the power supply.

THE POWER SUPPLY

The power supply is conventionally thought of as a device to convert ac power to dc power. The basic circuit of a half-wave supply is shown in Fig. 1-7.

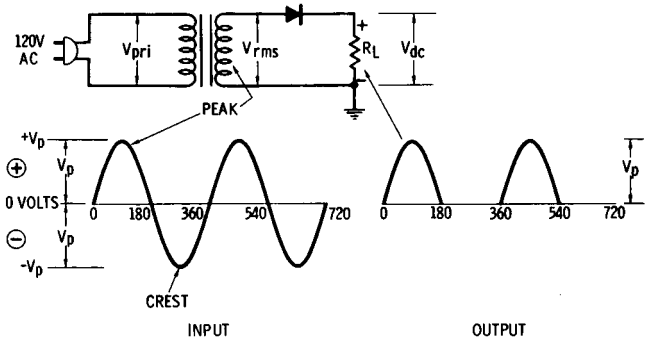


Fig. 1-7. Basic half-wave power supply.

At the secondary of the transformer, the sinusoidal voltage is V_{rms}. It varies repeatedly between the positive peak $+V_p$ and the negative crest of $-V_p$ volts. The complete cycle is divided into 360°.

The average voltage over a complete cycle is zero since all portions of the positive half of the cycle from 0° to 180°, are cancelled by all portions of the negative half of the cycle from 180° to 360°. Despite this, the voltage during each half of the cycle, in conjunction with the current, can supply power to a load. The effective voltage over a half-cycle is $V_p/2$ and over the complete cycle is $V_p/\sqrt{2}$. These two important numbers are the rms voltages of a half-wave and full-wave sinusoidal cycle, respectively.

In Fig. 1-7, during the portion of the cycle when the upper half of the secondary winding of the transformer is positive with respect to the lower half, the diode conducts, and a voltage is developed across R_L with the polarity shown. During the second half of the cycle, the voltage across the diode is in the reverse direction, and there is no conduction. The shape of the output voltage is shown in the figure. Note the half-cycle pulses with peak voltages, V_p. It is dc because the sinusoidal half cycles are only in one direction—positive with respect to ground in this instance. The output is a pulsating dc that has an rms value of $V_p/2$. Because the

negative half of the cycle has been eliminated, there is also an average dc voltage across the resistor. It is V_p/π.

The total equivalent representation of this circuit includes the impedance of the transformer and diode, in series with the rest of the components. The impedance of the diode is usually so small as to be negligible. The transformer impedance, R_T, can be calculated from the formula:

$$R_T = R_s + \left(\frac{V_{rms}}{V_{pri}}\right)^2 R_p \qquad (1\text{-}6)$$

where,

R_T is the transformer impedance,
R_p is the primary winding resistance,
R_s is the secondary winding resistance,
V_{rms} is the unloaded voltage across the secondary for a specific rms supply voltage, V_{pri}.

If the impedance of the transformer is not negligible compared to the resistance of the load, the peak output voltage is not truly equal to the peak supply voltage. This can be deduced from the equivalent circuit involving the voltage source and the transformer impedance in Fig. 1-8.

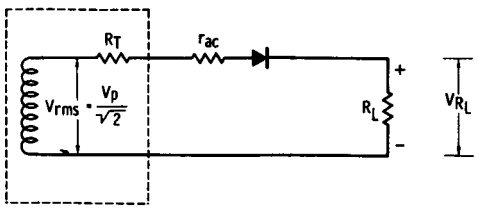


Fig. 1-8. Equivalent circuit of impedances in Fig. 1-7.

R_T is one arm of a voltage divider, with R_L as the other arm. The peak voltage, V_{PR_L}, across R_L is:

$$V_{PR_L} = \frac{R_L}{R_T + R_L} V_P \qquad (1\text{-}7)$$

where,

R_L is the load resistance,
R_T is the transformer resistance,
V_{PR_L} is the peak voltage across the load,
V_P is the peak supply voltage.

However, R_T is usually so small that it is negligible when compared to R_L.

The transformer impedance is important in determining the regulation of the circuit. Regulation is the amount the output voltage varies with changes in current through the circuit. (These changes may be due to variations in current demanded by the load.) The percent of regulation is defined by the formula:

$$\% \text{ Regulation} = \frac{V_2 - V_1}{V_1} 100 \tag{1-8}$$

where,

V_2 is the dc voltage across the load when R_L is open circuited,
V_1 is the dc voltage across the load when R_L is at its rated value.

Smaller numbers for percent of regulation are most desirable. Obviously, regulation is best when R_T is at a minimum.

R_L itself may not vary physically, but a nonlinear load on the power supply, such as a transistor, may be the equivalent of a variable load resistance. The device may draw different quantities of current at various times during its operating cycle. If the current variations are large, good regulation is usually desirable. The permissible voltage change with specific current variations should be indicated when specifying a power transformer.

Another important characteristic of a power supply is the ripple content in the output. Actually, the purpose of the power supply is to convert the ac into pure dc. There is usually some ac riding on the dc at the load. This ac is undesirable ripple. The ripple factor, r, is determined from the formula:

$$r = \frac{\text{rms voltage components across the load}}{\text{average dc voltage across the load}} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \tag{1-9}$$

The numerator is the difference between the dc and the rms ripple components.

In the example in Fig. 1-7, the rms voltage across the load is $V_p/2$; the average dc voltage is V_p/π. These numbers, divided by R_L, are the rms and average currents, respectively. The ratio of the two is:

$$\frac{I_{rms}}{I_{dc}} = \frac{V_p/2R_L}{V_p/\pi R_L} = \frac{\pi}{2} = 1.57$$

and the ripple factor from Equation 1-9 is 1.21. This is quite high.

One other important factor in power-supply design is efficiency: the ratio of the dc power at the load to the ac power input to the system. It can be determined from the formula:

$$\text{efficiency} = \frac{P_{Load}}{P_{ac\ input}} \times 100\% = \frac{40.6}{1 + \frac{R_T + r_{ac}}{R_L}} \tag{1-10}$$

for the circuit shown in Fig. 1-17.

The diode can be specified from circuit requirements. The peak inverse voltage, or the peak voltage across the diode when it is not conducting is V_p or $\sqrt{2}\,V_{rms} = 1.41_{rms}$. This is the peak ac secondary voltage. The peak current, I_p, is equal to the peak supply voltage divided by the total resistance in the circuit, or $I_p = V_p/(R_T + R_L)$. (The diode resistance is

assumed to be negligible here.) This is the minimum recurring peak current for which the diode need be rated. The average diode current is:

$$I_{AV} = \frac{I_p}{\pi} = \left(\frac{1}{\pi}\right)\frac{V_p}{R_T + R_L}.$$

There is no large initial surge current, and, thus, this type of rating is not a factor in choosing a diode for use in the circuit under discussion.

If the power dissipated by the diode causes the temperature of the diode to greatly exceed 25°C, a heat sink may be required. An estimation of the power dissipation can be made if it is assumed that the current through the diode is sinusoidal. Multiply the average diode current ($I_{AV} = I_p/\pi$) by the voltage across the diode. For safety, assume that this voltage is 0.3 volt for germanium units and 1 volt for silicon. Power is the product of the voltage across the diode and the average current.

Heat is generated in the rectifier because of the power it must dissipate. A good rectifier should be capable of readily conducting heat away from the junction to the surrounding air. Plastic diodes perform better than their glass counterpart in this function. However, glass devices are usually hermetically sealed against moisture, while the plastics only offer resistance to this type of contamination. The large rectifiers require heat sinks to aid in the cooling process. The discussion of heat sinks will be covered in the chapter on power amplifiers.

A diode or rectifier should be capable of dissipating as much power when current flows in the reverse direction, as it does when it is forward biased. The sharp avalanche diodes boast this characteristic and are thus desirable for use in power supplies where sharp transient peaks present on the line or in the circuit may appear across the rectifier.

The power transformer can be specified for the vendor from the accumulated data, as follows:

For an average output voltage of V_p/π, the transformer secondary must supply an rms input voltage of $V_p/\sqrt{2}$. Setting up the ratio of rms to output voltage, the secondary rms voltage is $\pi/\sqrt{2}$ or 2.22 multiplied by the average output voltage. Also specify the desired load current at this voltage. The minimum acceptable regulation of the circuit may be controlled by indicating a maximum or minimum voltage at a specific circuit current in addition to the one used as the center design value.

The permissible operating temperature of a power transformer is an important factor when specifying this component. Indicate to the manufacturer the maximum ambient temperature around the transformer. Also, specify the maximum winding temperature you require: 90°C is a good winding temperature in a conservative design, although most transformers can be operated safely with temperatures up to 105°C.

The supply just described has too much ripple to be suitable for most applications; however, a capacitor across the load resistor will smooth much of the ripple. The effect of this capacitor is seen in Fig. 1-9.

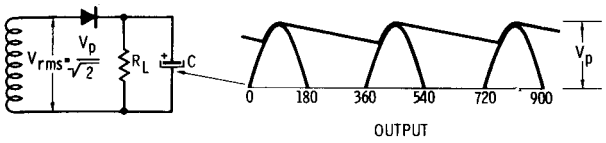


Fig. 1-9. Effect of capacitor C on ripple.

The half-cycle output of Fig. 1-7 is redrawn here. The capacitor across the load is charged to the peak voltage by the half-cycle pulses. The capacitor begins losing its charge the moment the pulse drops from its peak. The voltage across the capacitor will discharge only until the next pulse recharges it to the peak value. The thick curve on top of the signal indicates the shape of the voltage across the capacitor and load resistor. Note how much smoother this dc voltage is than the voltage depicted in Fig. 1-7.

The ripple factor is a function of the size of the capacitor across the load, as well as the size of the load. The variation of ripple factor with the size of these components is shown in Fig. 1-10. A power-line frequency of 60 Hz is assumed here as well as throughout the remainder of the discussion. C is the capacitance in farads across the load, R_L in ohms. (If R_L is unknown, it can be calculated from Ohm's law. R_L is equal to the dc voltage across the load divided by the dc current at that voltage.)

The output voltage is related to R_L, C, and the ratio of the impedance of the transformer, R_T, to the resistance of the load, R_L. Mathematically, the ratio is R_T:R_L. The curve plotting this information is shown in Fig. 1-11A.

As an example of the use of the chart in Fig. 1-11A, assume that you require 20 volts dc across a load resistor of 10 ohms. A filter capacitor of 1000 μF (10^{-3} farads) is across the 10-ohm load resistor. Assume $R_T = 5$ ohms. The factor to be derived from this data is the rms voltage required across the secondary of the transformer to provide 20 volts dc across the 10-ohm load.

First, calculate the product of R_L and C. It is $10 \times 10^{-3} = 10^{-2}$ or .01. Locate .01 on the horizontal axis of the graph in Fig. 1-11A. Draw a vertical line from this point.

Next, the transformer impedance is 5 ohms. The ratio of this to the load resistor is 5/10 or 0.5. Locate the curve plotted for this ratio by finding 0.5 next to the specific curve near the right hand vertical axis. Note where this curve crosses the line previously drawn from 0.01 on the R_LC axis. Draw a horizontal line from this point to the vertical axis. It crosses this axis at the point where the ratio of V_{R_L}/V_{rms} equals 0.46.

The solution to the problem can now be found by applying simple arithmetic. In order to get 20 volts across the load V_{R_L}, the rms voltage across the secondary of the transformer must be $V_{rms} = V_{R_L}/0.46 = 20/0.46 = 43.5$ volts.

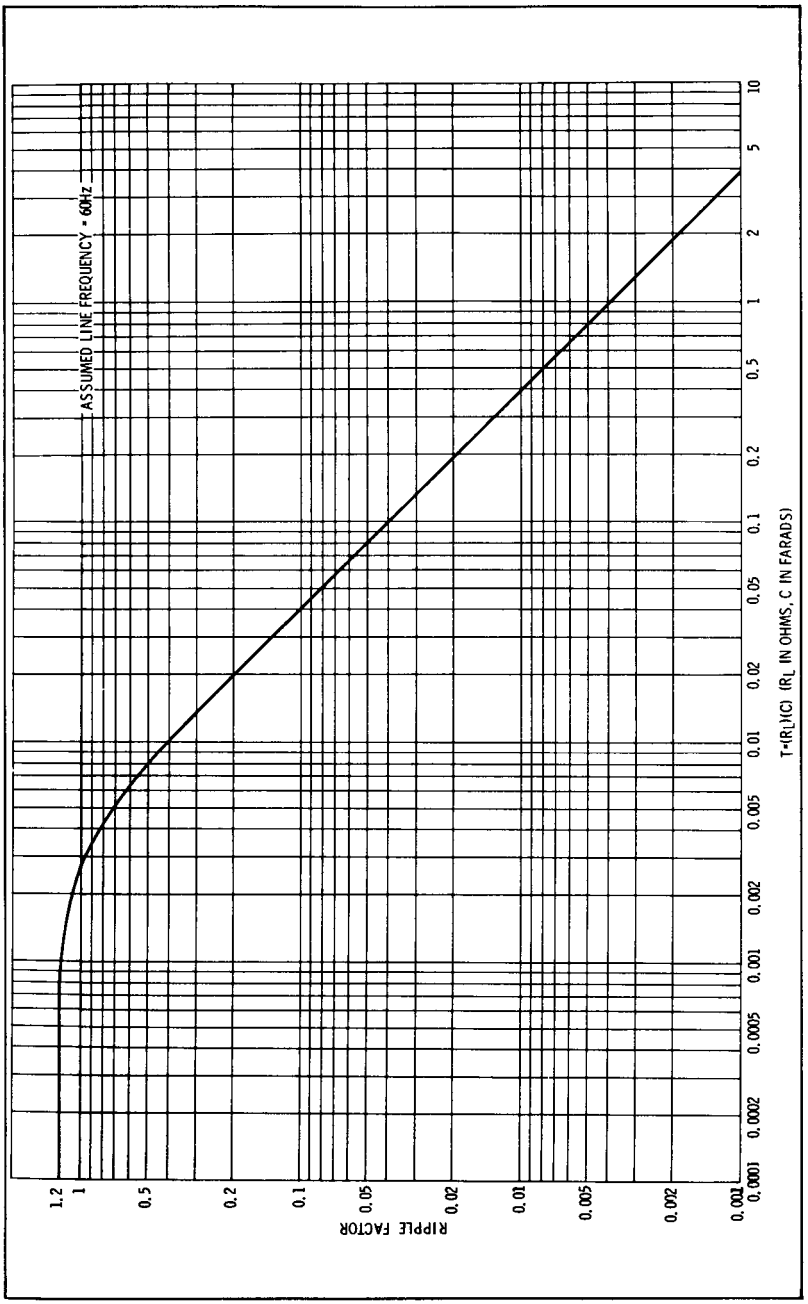
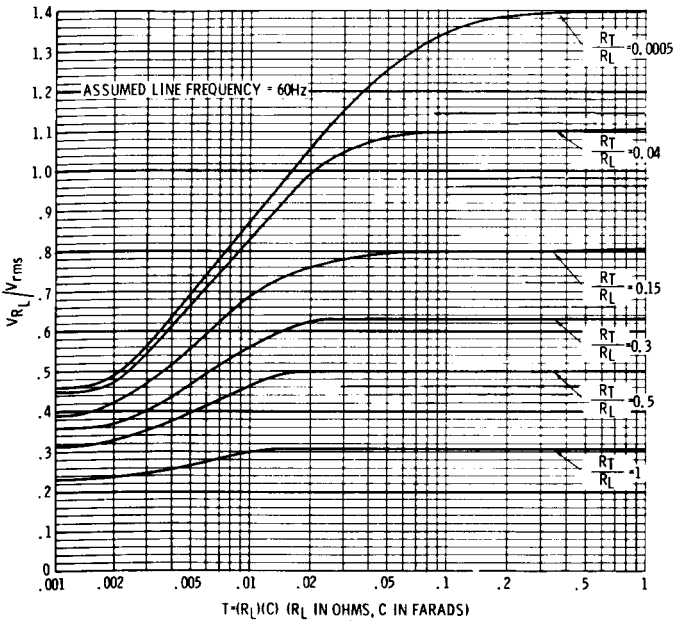
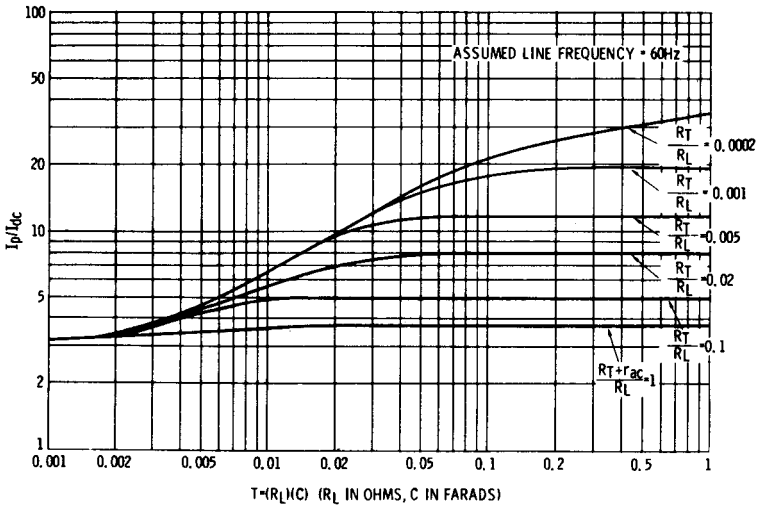


Fig. 1-10. Half-wave circuit ripple factor plotted for different values of R_LC.



(A) Plot to determine dc voltage across R_L from rms voltage across transformer.



(B) Plot to determine peak diode current from average load current.

Fig. 1-11. Determining peak diode current and dc voltage.

The following information should be provided to specify the transformer. The rms voltage across the secondary is 43.5 volts. The output across the 10-ohm load resistor is 20 volts at 2 amps ($I_{R_L} = V_{R_L}/R_L = 20/10 = 2$ amps). Also indicate that the circuit is of the half-wave type using a 1000-μF capacitor input filter. Note the maximum permissible temperature of the transformer windings.

As for the diode, the steady-state current it conducts, I_{dc}, is 2 amps, or the same amount of current as flows through the load. However, when a capacitor input filter is used, the diode must be capable of conducting more than the steady-state current. It should be overrated by about 40 percent. In the example, it should be capable of conducting at least 2 amps plus 40 percent of 2 amps, or $2 + 0.8 = 2.8$ amps.

Since the voltage across the diode is, for safety reasons, assumed at 1 volt, the power dissipated by the semiconductor is 2 amps $\times$ 1 volt, or 2 watts. The peak inverse voltage across the diode is double the peak voltage across the secondary of the transformer, or $2 \times (43.5)\ (1.414) = 123$ volts. The repeated peak current through the diode can be determined from the curve in Fig. 1-11B. Find the curve for the ratio R_T/R_L. Next, calculate CR_L and locate the vertical line on the curve representing this product. Note where the vertical line intersects the R_T/R_L curve. Draw a line to the vertical I_p/I_{dc} axis on the right-hand scale. Calculate I_p. Should R_L be a variable, the repeat peak current will also vary. Use the largest value when specifying the diode.

An input filter capacitor causes a very large initial surge current through the diode. This is because the capacitor is effectively a short when the power is first applied. It behaves as a partial short until it charges to its final voltage. This short is across the load, R_L. The only component that remains in the circuit when the short is across the load is R_T. If R_T is assumed to be 5 ohms, the peak surge current, I_{ps}, that the diode must be able to support is the peak of the supply voltage divided by R_T, or $43.5 \times (1.414)/5 = 12.3$ amps. It must withstand this for a period of time (time constant) equal to $\tau = CR_T = 1000 \times 10^{-6}(5) = 5 \times 10^{-3}$ secs.

Manufacturers specify the permissible surge current in several different ways. One method indicates the maximum permissible current that can be sustained over one cycle of supply voltage. If the power-supply frequency is 60 Hz, the time for the cycle is 1/60 second or 16.7×10^{-3} secs. If the specification for a particular diode states, for example, a nonrepetitive permissible surge current of 20 amps over one cycle, it means that 20 amps is permitted on an initial surge if the time constant, τ, is less than 16.7×10^{-3} secs. In the example cited, the current is 12.3 amps and τ is 5×10^{-3} secs. The current for the period of time is well within the surge specification for this diode. If the current in the example were more than 20 amps or the period of time more than 16.7×10^{-3} secs, the life of the diode under these surges would be limited.

Other manufacturers indicate maximum surge current when τ is equal to or less than ½ cycle or 8.35×10^{-3} secs. In this case, the surge current must not exceed the specified value if the time constant of the circuit is equal to 8.35×10^{-3} or more. Attempts should be made to stay within the surge limit even if τ is less than 8.35×10^{-3} secs.

Many manufacturers supply curves indicating the permissible surge current for different values of τ.

Another method specifies the diode's permissible surge by an $I_{ps}^2\tau$ rating, for this product is proportional to energy. The data indicate that as long as the product of the circuit constants is maintained within this factor, the operation of the diode is within safe limits. In the example, this product would be $(12.3)^2 \times (5 \times 10^{-3}) = 0.756$ amp²secs. This means that any diode rated at 0.756 amp²secs or more is satisfactory.

This specification should be used with considerable reservation. A safety factor of 10 should be added for a conservative design. Thus, a reasonable diode for the application should have at least an $I_{ps}^2\tau$ rating of 10×0.756 or 7.56 amp²secs.

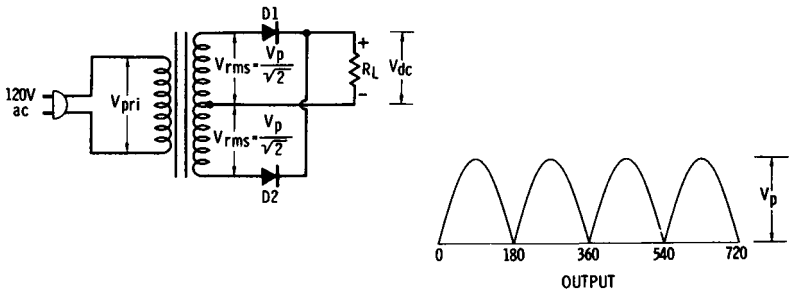


Fig. 1-12. Full-wave power supply.

The half-wave circuits discussed thus far can be extended and improved by use of the full-wave power supply in Fig. 1-12. In the circuit in Fig. 1-7, a pulse of the voltage appears across R_L every other half-cycle. As can be seen from the output curves of Fig. 1-12, the spaces between the half-cycles have been filled in. The circuit is arranged so that each diode conducts for an alternate half-cycle and the two half-cycles add across the load, R_L, as shown.

The transformer secondary is divided into two parts by means of a lead from the center of the winding. V_{rms} volts is across each half of the secondary. The peak voltage across the load resistor is V_p. The rms voltage across the load is $V_p/\sqrt{2}$, the same as for an ordinary sine wave. The average output voltage is $2V_p/\pi$, or double the average voltage for the half-wave circuit of Fig. 1-7. Transformer and diode calculations are not unlike those for the half-wave rectifier circuit. In this case, the average current through each diode is only half of the current through the load.

As was the case with the unfiltered half-wave rectifier circuit, the ripple across R_L in Fig. 1-12 is high. The resultant dc with ripple appearing across the load cannot be used in many circuit applications, for the ripple factor is 0.48. The major ripple component in this example is 120 Hz; in the half-wave circuit it was 60 Hz. Although the situation is better than in the half-wave circuit, this ripple is still much too high, and must be reduced. Once again, a capacitor, C, must be added across the load resistor, R_L. As before, the ripple can be determined from the curves.

Use Fig. 1-13 to find the ripple factor if R_T is 1/10 of R_L or less. Fig. 1-14 may be used to determine the output voltage. The maximum dc out-

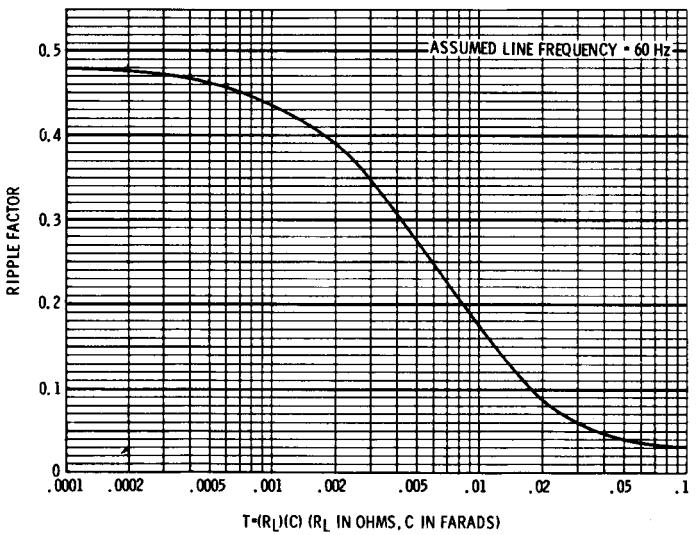


Fig. 1-13. Ripple factor versus R_LC.

put voltage across the load for a specific ac input voltage is achieved when 377 CR_T is between 0.2 and 0.4.

When using either curve, it should be noted that R_T refers to the equivalent impedance seen across one half of the secondary winding of the transformer. V_{rms} is the voltage across half the secondary winding.

In order to determine the diode specifications correctly, it must first be noted that the circuit consists of two half-wave arrangements. The dc current through each diode is half the load current. The determination of the diode surge current and circuit time constants involves one half the transformer secondary voltage and impedance as well as the entire capacitor across the load.

A more economical design uses the full-wave bridge circuit of Fig. 1-15. A smaller transformer can be used because, for the same dc output current,

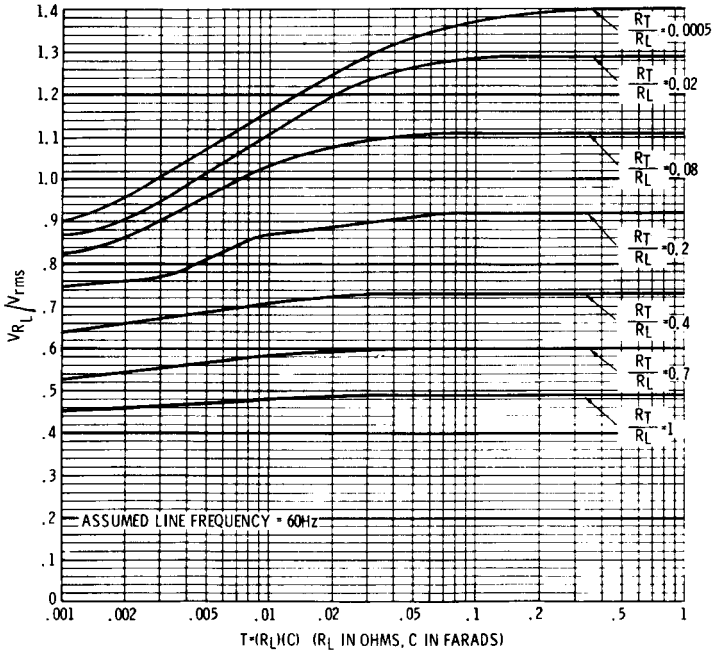


Fig. 1-14. Plot to determine dc voltage across R_L from V_{rms} volts across half the secondary winding.

less rms transformer current is required here than in the previous full-wave circuit. Although twice the number of diodes are used, the inverse peak voltage across each device is equal to V_p of the supply voltage, or (1.41) V_{rms}. It was double this for the circuit in Fig. 1-21.

DIODES IN SERIES

In some applications, the breakdown voltage capability of an available diode is insufficient. Several diodes may be connected in series so that a greater peak inverse voltage may be applied to the combination than may be placed across any one of the devices individually. The resistors and capacitors shown in Fig. 1-16 should be connected across the diodes to swamp differences in the individual devices.

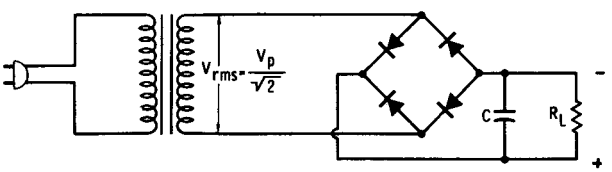


Fig. 1-15. Full-wave bridge circuit.

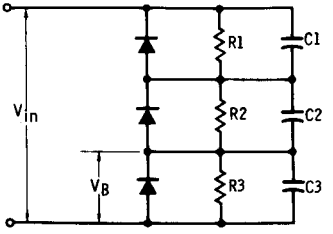


Fig. 1-16. Diodes connected in series.

Resistors are connected across each diode so that the applied voltage is divided equally between them. C1, C2 and C3 assure that transients are shared equally.

Resistors R_1, R_2 and R_3, should each be approximately half the reverse resistance of each diode. The value of the resistors is determined from Equation 1-11,

$$R \leq 500 \frac{V_B}{I_R(\text{max.})} \qquad (1\text{-}11)$$

where,

V_B is the peak inverse voltage to appear across each diode,
$I_R(\text{max})$ is the maximum specified reverse diode current in mA,
R is the value of the resistor across any one diode: R_1, R_2, or R_3.

The power dissipated by R is,

$$P_R = \frac{\left(\frac{V_B}{\sqrt{2}}\right)^2}{R}$$

where,

P_R is the power dissipated by R,
V_B is the peak voltage across R.

The capacitor across a particular diode is usually made three times the rated capacitance of the zero-biased diode.

A diode may be switched rapidly in and out of conduction, and the switching may generate some instability in the form of a decaying oscillation. A 2- or 3-ohm resistor is frequently placed in series with the diode to assure rapid dissipation of the oscillating energy and to let it settle quickly to a steady state.

ZENER DIODES

Approximately 0.6 volt is developed across silicon diodes biased in the forward direction. If a variable load (with a high impedance relative to that of the diode) is placed across the forward-biased semiconductor, the

voltage across the load will be maintained at about 0.6 volt, even if the current required by the load varies considerably.

Should a reverse-biased voltage be applied to the semiconductor, the diode will break down at a specified voltage, $-V_B$. As the voltage is made more negative than $-V_B$, the current increases at an extremely rapid rate. If the current is limited to a specific value by external circuitry, the diode will not disintegrate. Despite the increasing current through the diode, the voltage across the semiconductor will remain fairly constant. A relatively constant voltage will also be maintained across any load connected in parallel with the diode, if the impedance of the load is high compared to the impedance of the diode.

A drawing of a zener diode and a typical curve describing its characteristics are shown in Fig. 1-17. Only the reverse characteristic to be discussed here has been drawn. The forward characteristic is the same as for any other forward-biased junction diode. Ideally, $-V_B$ is a constant while "I" can vary from zero to minus infinity. "I" must be limited so that the power dissipation rating of the diode is not exceeded.

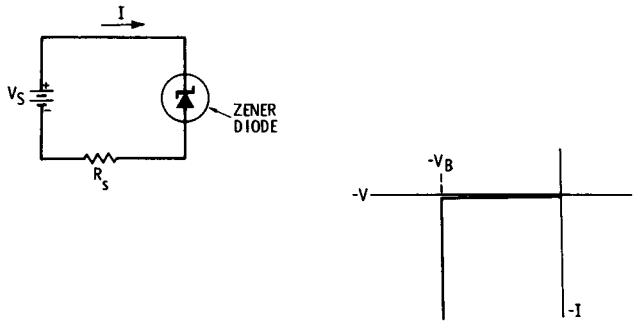


Fig. 1-17. Zener diode circuit with ideal curve.

Several zener characteristics should be noted here. First, the zener breakdown voltage is temperature-dependent. When the breakdown voltage is in the zener region, or less than 5 to 6 volts, the zener voltage decreases with an increase in temperature. In the 5- to 6-volt region, the zener voltage remains relatively unchanged despite temperature variations. In the avalanche region, above about 6 volts, the zener voltage increases as the temperature rises.

The forward-biased diode voltage decreases as the temperature rises (-2.5 mV/°C). The voltage across the reverse-biased diode, when operated in the avalanche region, increases with temperature. The temperature variation in the avalanche region can be compensated for, if necessary, by connecting a forward-biased diode of sufficient current-carrying capability in series with the reverse-biased zener. Do not forget to add the drop in the forward-biased diode (about 0.6 volt) to the zener voltage to

(A) Diodes as individual units. (B) Diodes combined into one package.

Fig. 1-18. Zener diodes with temperature compensation.

determine the total voltage across the combination. Examples of this are shown in Fig. 1-18. In Fig. 1-18A, the diodes are individual units, while in Fig. 1-18B they are combined into one package.

A second important characteristic can best be described if you refer to the curve in Fig. 1-17. A sharp breakdown point is shown at V_B. This is reasonably true of diodes working in the avalanche region. For diodes operated in the zener region, this breakdown point is rounded and quite indecisive. The designer can bypass the region by choosing a minimum zener idling current. It is usually made equal to about 10% of the maximum current rating of the diode. Another factor guiding the idling current choice is that zener diodes are noisy in the low current region.

The third zener characteristic of importance is the ac resistance. The ac resistance of a forward-biased diode was discussed previously. The actual resistance of a reverse-biased device was derived using Fig. 1-3A. The zener-diode resistance can be derived in a similar fashion from its characteristic curve.

The circuit in Fig. 1-17 will be used to derive the information required to make use of the diode as a regulator, and, for demonstration purposes, the curve in Fig. 1-19 will be used to represent the diode. It is assumed that the zener diode used here has a relatively high impedance.

The supply voltage is nominally V_S. It varies from V_{S1} to V_{S2} with power-line voltage changes. The diode impedance is assumed to be negligi-

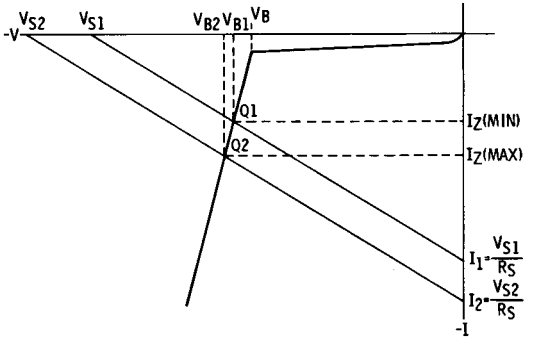


Fig. 1-19. Zener diode curve with load lines.

ble compared to that of the series resistor in the circuit, R_S. The required information to be derived from this data is how much the output voltage across the diode will change when the input supply jumps from V_{S1} to V_{S2} volts.

The load lines for R_S, with supply voltages V_{S1} and V_{S2}, must be drawn over the diode curve to examine the operation of the circuit. First, assume the supply voltage is V_{S1}. With no current, the entire supply voltage will be across the diode. The intersection of $-V_{S1}$ volts and 0 mA is one point on the load line. Mark $-V_{S1}$ on the horizontal axis.

Next, assume there is 0 volts across the diode. The current through the circuit is $I_1 = V_{S1}/R_S$. There is a current of I_1 mA when there is 0 volts across the diode. Mark I_1 on the vertical axis. With a straight line, connect the two points just located. The line crosses the diode curve at Q_1. Draw a vertical line from Q_1 to the axis at V_{B1}. This is the voltage across the diode when the input voltage is V_{S1}. Draw a horizontal line from Q_1 to the axis at I_Z (min). This is the current through the diode under the same conditions.

Repeat this procedure, assuming that the supply voltage shifted to V_{S2}. Locate V_{B2} on the horizontal axis. Note that $V_{B2} - V_{B1}$ is much less than $V_{S2} - V_{S1}$. For a large input voltage variation there is only a small voltage change across the diode. However, the current through the diode will vary from I_Z (min) to I_Z (max).

The voltage across a load, R_L, connected in parallel with the diode, would be subjected to the same good voltage regulation as the diode, if the impedance of the load were considerably higher than the impedance of the diode. A circuit of this type is shown in Fig. 1-20.

The equation for the voltage drops around the circuit in the drawing is:

$$V_S = R_S (I_{R_L} + I_Z) + V_B$$

where,

I_{R_L} is the current through the load,

I_Z is the current through the zener diode.

The information stated in the equation is derived from the following factors: The sum of the two currents through the load and zener, equals the current through R_S, the series resistor. The voltage across R_S is, by Ohm's law, the resistance of R_S multiplied by the total current, $I_{R_L} + I_Z$. This, in addition to the nominal and rated breakdown voltage across the diode, V_B (which is identical to the voltage across R_L) must be equal to the supply voltage, V_S.

Two factors may vary in a circuit of this type. These are the supply voltage, the load resistor (or load current, I_{R_L}), or both. First assume that only the supply voltage varies. This case has been depicted graphically in Fig. 1-19.

In order to determine the components in the circuit, it is necessary to start with the basic equation stated above. The zener idling current is assumed to be about 0.1 I_{R_L} so that the total current through the circuit is $0.1I_{R_L} + I_{R_L}$, or $1.1I_{R_L}$. The maximum size of the series resistor is:

$$R_S = \frac{V_{S1} - V_B}{1.1I_{R_L}} \text{ ohms} \qquad (1\text{-}12)^*$$

where,

V_{S1} is the minimum value of the supply voltage.

The resistance of the physical component in the actual circuit should not be significantly less than the calculated value.

The maximum current through R_S is:

$$I_{R_L} + I_Z\,(\max) = \frac{V_{S2} - V_B}{R_S} \text{ amps} \qquad (1\text{-}13)$$

where,

V_{S2} is the highest supply voltage,

I_Z (max) is the maximum zener current.

The power dissipated by the series resistor is derived from the general power equation, $P = V^2/R$:

$$P_S = \frac{(V_{S2} - V_B)^2}{R_S} \text{ watts.} \qquad (1\text{-}14)^*$$

The maximum power dissipated by the zener is $I_Z(\max)V_B$, or from Equation 1-13:

$$P_Z\,(\max) = \left(\frac{V_{S2} - V_B}{R_S} - I_{R_L}\right) V_B \text{ watts.} \qquad (1\text{-}15)^*$$

If the input voltage is constant at V_S, and the load current varies from a maximum I_{R_L} (max) to a minimum I_{R_L} (min) due to a variation of load resistance, R_L, the maximum allowable series resistor that can be used is:

$$R_S = \frac{V_S - V_B}{1.1\ I_{R_L}\ (\max)} \text{ ohms.} \qquad (1\text{-}16)^*$$

This is based on the obvious fact that the maximum allowable voltage across the series resistor is the resistance multiplied by the maximum current through the resistor. The power dissipated by the resistor is:

$$P_S = \frac{(V_S - V_B)^2}{R_S} \text{ watts} \qquad (1\text{-}17)^*$$

and the maximum power dissipated by the diode is:

$$P_Z\,(\max) = \left[\frac{(V_S - V_B)}{R_S} - I_{R_L}\ (\min)\right] V_B \text{ watts} \qquad (1\text{-}18)^*$$

Should I_L vary from I_{R_L} (max) to I_{R_L} (min) while the supply voltage also varies, use the following equation for the maximum size of the series resistor:

$$R_S = \frac{V_{S1} - V_B}{1.1 I_{R_L}\,(\text{max})} \text{ ohms} \qquad (1\text{-}19)^*$$

The power dissipated by R_S is:

$$P_S = \frac{(V_{S2} - V_B)^2}{R_S} \text{ watts} \qquad (1\text{-}20)^*$$

Then zener diode dissipates a maximum of:

$$P_Z\,(\text{max}) = \left[\frac{(V_{S2} - V_B)}{R_S} - I_{R_L}\,(\text{min})\right] V_B \qquad (1\text{-}21)^*$$

The application of the formulas to the circuit in Fig. 1-20 is self-evident.

Assume, in one case that load resistor, R_L, is fixed at 75 ohms. A regulated 7.5 volts is required across this resistor. Hence, the reverse breakdown voltage of the zener diode must be 7.5 volts. Furthermore, a nominal 30-volt dc supply is available, and it can vary from 26 to 34 volts. The requirement is to specify a commercially available zener diode and series resistor.

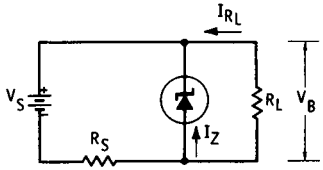


Fig. 1-20. Zener diode with output load.

Since the load draws a constant current, the resistance of R_S can be found from Equation 1-12. The constant current drawn by the load, from Ohm's law, is $I_{R_L} = 7.5$ volts/75 ohms $= 0.1$ amp. Hence,

$$R_S = \frac{26 - 7.5}{1.1\,(0.1)} = \frac{18.5}{0.11} = 168 \text{ ohms}$$

The commercially available resistor that most nearly matches this value is 150 ohms $\pm 10\%$. The resistor must be capable of dissipating at least the power determined from Equation 1-14. It is:

$$P_S = \frac{(34 - 7.5)^2}{150} = \frac{26.5^2}{150} = \frac{700}{150} = 4.65 \text{ watts}$$

With the resistor completely specified, the zener diode can now be determined. The V_B is 7.5 volts. The minimum power it must be capable of dissipating, from Equation 1-15, is:

$$P_Z = \left(\frac{34 - 7.5}{150} - 0.1\right) 7.5) = (0.077)\,(7.5) = 0.5775 \text{ watt}$$

The best regulation is achieved when the impedance of the diode is small compared to the 75-ohm load resistor.

In a second example, assume the supply is firmly fixed at 30 volts. However, the load resistor varies from 60 to 90 ohms. It is desirable to maintain a fixed 7.5 volts across the load. Using the same circuit as before, what must be the characteristics of the series resistor and the zener diode?

From Ohm's law, the current through R_L when R_L is maximum is I_{R_L} (min) $= 7.5/90 = 0.083$ amp. When the load resistor is at its minimum value, I_{R_L} (max) $= 7.5/60 = 0.125$ amp. From Equation 1-16, the maximum series resistor must be:

$$R_S = \frac{30 - 7.5}{1.1(0.125)} = \frac{22.5}{0.1375} = 163 \text{ ohms}$$

Once again, a commercially available 150-ohm, $\pm 10\%$ resistor can be used. The maximum power dissipated by this resistor, from Equation 1-17 is:

$$P_S = \frac{(30 - 7.5)^2}{150} = 3.37 \text{ watts}$$

The maximum power dissipated by the zener diode can be determined from Equation 1-18:

$$P_Z = \left(\frac{30 - 7.5}{150} - 0.083\right) 7.5 = (0.067)\ (7.5) = 0.5 \text{ watt}$$

In a similar manner, Equations 1-19, 1-20, and 1-21 may be used to determine the required series resistor and zener diode, if both the load resistor (or load current) and the supply voltage vary. This last case occurs most frequently in practical applications.

Zener Filters

A zener diode may be used to replace a capacitor in a power-supply filter circuit. This becomes obvious when it is recalled that the variable input voltages used to derive the previous equations may change at a random rate with power line excursions. The ripple on the dc produced by a filtered power supply may be thought of as a variation of the dc input voltage. This periodic variation may frequently be eliminated by a zener diode rather than a filter capacitor. A numerical example should serve to demonstrate the mechanism.

The basic circuit using a 7.5-volt zener diode as a filter is shown in Fig. 1-21. A 30-volt dc supply has a 3-volt rms ripple superimposed upon it. The impedances of the series resistor, zener diode, and load resistor are indicated in the drawing, as is the zener breakdown voltage. Calculate the power dissipated by the diode, the dc voltage across R_L and the diode, and the ripple voltage across the load.

Before solving the problem, two items must be discussed briefly. The first is Thevenin's theorem.

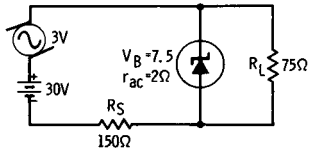
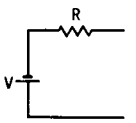


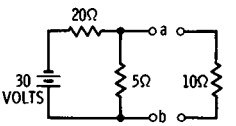
Fig. 1-21. Circuit describing zener diode as a filter.

The equivalent circuit of a power supply is a voltage, V, in series with a resistor, R. This is shown in Fig. 1-22A. Through the use of Thevenin's theorem, complex circuits can be reduced to this form. A numerical example and the method of reducing the circuit to this arrangement are derived with the help of the figure.

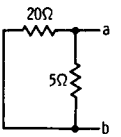
In Fig. 1-22B, a 30-volt supply is in series with a 20-ohm resistor. A 5-ohm resistor is connected across this combination. If a 10-ohm load were connected across the 5-ohm resistor from "a" to "b", what would be the



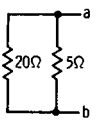
(A) Equivalent circuit of a power supply.



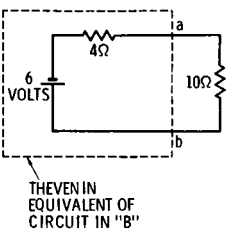
(B) Circuit for determining voltage across 10-ohm load resistor.



(C) Thevenin equivalent impedance with power supply shorted.



(D) Fig. 1-22C redrawn.



(E) Thevenin equivalent of circuit in Fig. 1-22B.

Fig. 1-22. Steps in determining Thevenin equivalent circuit.

voltage across the 10-ohm load resistor and what resistance would the 10-ohm load see at terminals a-b?

The Thevenin conversion and the solution to the problem can be accomplished in three simple steps.

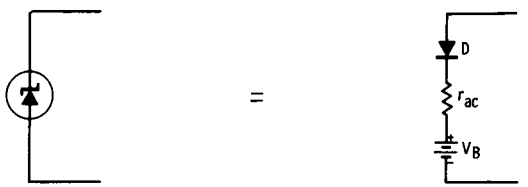
1. Remove the load. Consider the circuit when the 10-ohm resistor is not connected to the terminals a-b.
2. Determine the Thevenin equivalent voltage by calculating the potential at the output terminals a-b. From voltage divider equations, it is,

$$[5/(20+5)]\,30 \text{ volts} = (5/25)\,30 = 6 \text{ volts.}$$

3. Determine the Thevenin equivalent impedance of the network at terminals a-b with the supply voltage shorted. From Figs. 1-22C and D it can be seen that the impedance is the parallel combination of the 20-ohm and 5-ohm resistors. Using the equation for resistors connected in parallel, the equivalent single resistor is $(20 \times 5)/(20+5) = 100/25 = 4$ ohms.

The Thevenin equivalent of the circuit has now been completely derived. It is drawn in Fig. 1-22E, with the 10-ohm load resistor in place. It is obvious that the 10-ohm resistor across terminals a-b, sees a 4-ohm power-supply impedance. The voltage across the load can be determined using the voltage divider equation. It is, $[10/(4+10)]\,6 = 60/14 = 4.286$ volts.

The second item required for the solution of the problem related to Fig. 1-21, is the equivalent circuit of the zener diode. It is shown in Fig. 1-23. The zener diode does not conduct until its breakdown voltage is exceeded. It acts as if a battery equal to its breakdown voltage were in the circuit. There can be no conduction until the battery voltage is exceeded.



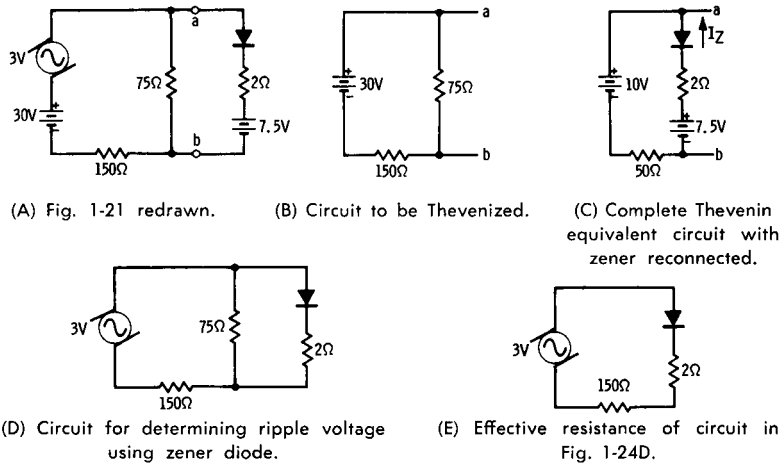
(A) Zener diode. (B) Equivalent circuit.

Fig. 1-23 Zener diode and its equivalent.

There is also an ideal diode in the equivalent zener circuit, which permits conduction in one direction only. The significant zener conduction takes place when it is reverse-biased. An ideal diode will conduct only when it is forward-biased. It must be shown in the equivalent circuit as a diode connected opposite in direction to that of the actual zener. A resistor in series with the diode and battery, and equal to the ac impedance of the zener diode, completes an equivalent circuit representation for the reverse-biased zener diode.

We now can return to Fig. 1-21 and calculate all the required information. Redraw the circuit as in Fig. 1-24A, replacing the zener diode with its equivalent circuit.

Initially, disregard the zener diode and ac ripple and find the Thevenin equivalent of the rest of the dc circuit shown in Fig. 1-24B. The Thevenin equivalent voltage at a-b is $V = 30[75/(75 + 150)] = 10$ volts. The equivalent resistance looking into terminals a-b with the voltage source shorted is the parallel equivalent of the 75-ohm and 150-ohm resistors, or 50 ohms. This dc Thevenin equivalent circuit is drawn in Fig. 1-24C with the zener reconnected.



(A) Fig. 1-21 redrawn. (B) Circuit to be Thevenized. (C) Complete Thevenin equivalent circuit with zener reconnected.

(D) Circuit for determining ripple voltage using zener diode. (E) Effective resistance of circuit in Fig. 1-24D.

Fig. 1-24. Steps in the solution of problem for circuit in Fig. 1-21.

The voltage across the zener diode (across a-b) is the zener equivalent circuit battery voltage, 7.5 volts, plus the voltage drop across the 2-ohm zener resistance. The second voltage is equal to the 2 ohms multiplied by the current through the entire circuit. This current, I_Z, can be found by writing an equation for all the voltage drops around the circuit, and solving the equation for I_Z.

10 volts = (50 ohms) (I_Z amps) + (2 ohms) (I_Z amps) + 7.5 volts and simplifying,

$$52\, I_Z = 2.5 \text{ volts}; \quad I_Z = 2.5/52 = 0.048 \text{ amp}$$

Then the voltage across the 2-ohm resistor is 2 ohms $\times$ 0.048 amp = 0.096 volt.

By adding this to the 7.5 equivalent zener battery voltage, the total voltage across the zener diode is found to be 7.5 V + 0.096V = 7.596 V. The error is usually insignificant if only the voltage of the zener were considered, rather than the sum of the rated voltage and the voltage developed across the zener equivalent circuit resistance. The voltage developed across the zener resistance was likewise ignored in the previous discussion of zener regulators.

The power dissipated by the zener is equal to the current through the diode multiplied by the breakdown (or diode equivalent battery) voltage. It is:

$$P_Z = (I_Z)\ (V_B) = (0.048)\ (7.5) = 0.36 \text{ watt}$$

A small correction factor can be added to consider the power dissipated by the 2-ohm resistance. It is $(I_Z^2)2$ ohms $= (0.048)^2 \times 2 = 0.0046$ watt. The total power dissipated by the zener diode is the sum of these two powers or 0.36 watt + .0046 watt = 0.3646 watt.

The ripple voltage using the zener diode may be calculated from the ac equivalent of the circuit in Fig. 1-24D. If the 75-ohm load is considered swamped by the 2-ohm zener resistance, the circuit becomes that in Fig. 1-24E. The ripple voltage across the 2-ohm resistor, by use of voltage divide methods, is $V_r = 3[2/(150 + 2)] = 0.0396$ volt. Hence, a 3-volt ripple was reduced to about 0.0396 volt—an improvement of approximately 76 to 1. ing

STABISTOR VOLTAGE-REFERENCE DEVICE

The voltage across the forward-biased germanium diode was accepted above as being 0.2 volt while the forward-biased silicon device was stated as having a forward voltage of 0.6 or 0.7 volt. These are more or less the voltages at which the respective devices start conducting a significant amount of current. Realistically, the voltage increases considerably with current through the device. Single junction germanium diodes can, at high current, have as much as 0.6 volt developed across the forward-diode junction, while more than one volt may be measured across a forward-biased silicon diode when there is a large amount of current passing through this device.

Over a limited current range, the voltage across the forward-biased diode varies little with changes in current. The stabistor takes advantage of this characteristic. The device is specified so that there is a specific fixed voltage across the diode coincident with a particular amount of current through the stabistor. The voltage across the device must remain relatively fixed over a specified, but limited, current range. Should a load be placed across the diode, the voltage across the load and the stabistor is held relatively constant with variations of current. This is especially true if the resistance of the load is large when compared to the resistance of the stabistor. The action of the diode in this forward-biased regulating role is not unlike that of the reverse-biased zener device.

WHITE NOISE GENERATOR

White noise, used in audio tests as a "hiss," consists of frequencies of identical energies over the entire audible spectrum.

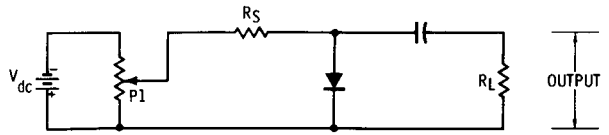


Fig. 1-25. White-noise generator.

Some p-n junction diodes, when biased in the reverse direction as is the case of the zener diode, generate noise as the avalanche breakdown voltage is approached. Specially selected diodes produce true white noise when they are operated well into the breakdown region.

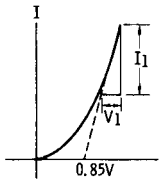
A typical white-noise generator circuit is shown in Fig. 1-25. The voltage is adjusted by the potentiometer, P1, until the diode is in the white-noise region. The noise across the diode is also developed across the high-impedance output load, R_L. R_S limits the diode current to safe values.

COMPLETE EQUIVALENT CIRCUIT

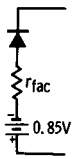
The equivalent circuit of the zener diode (Fig. 1-23B) can be used to represent any reverse-biased diode. They all have reasonably distinct reverse breakdown voltages, V_B, and reasonably constant impedances after the breakdown voltage is reached. The reversed leakage resistance is ignored here, as it is usually negligible when compared to all other resistances in the circuit.

The same equivalent circuit can be used for diodes biased in the forward direction. However, the forward-biased diode curve is not characterized by a distinct voltage equivalent to the breakdown voltage, V_B. Also, r_{ac} is not well defined.

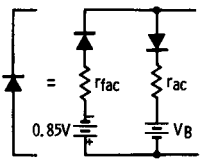
The broken line in Fig. 1-26A may be regarded as the linear approximation for the forward-biased diode curve. It runs along much of the actual curve. The forward ac resistance can be calculated from $r_{fac} = V_1/I_1$. It may intersect the horizontal axis at about 0.2 volt for germanium diodes and 0.85 volt for silicon devices. A fairly complete diode equivalent circuit, including the forward and reverse characteristics, is shown in Fig. 1-26C.



(A) Curve for forward-biased diode.



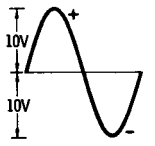
(B) Equivalent circuit for forward-biased diode.



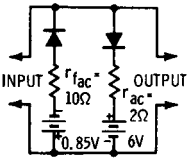
(C) Complete equivalent circuit showing forward- and reverse-biased conditions.

Fig. 1-26. Forward- and reverse-biased conditions.

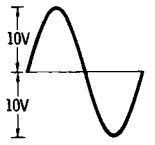
Assume that a sine wave with 20 volts peak-to-peak is fed from a voltage source across the hypothetical diode in Fig. 1-27. (A source that supplies a constant voltage to a load, regardless of the current demanded by the circuit, is a voltage source. The equivalent circuit of the supply in Fig. 1-22A, is a voltage, V, in series with a resistor, R, equal to zero. In the practical case, R is very small compared to the size of the load impedance.) A perfect voltage source will not be affected by the diode. The voltage across the diode will be a pure sine wave.



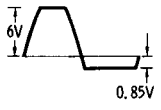
(A) Input to diode.



(B) Equivalent circuit of diode.



(C) Voltage across diode from voltage source.



(D) Voltage across diode from current source.

Fig. 1-27. Effect of diode on sine wave.

The voltage produced by a current source across a diode, does not fare as well. (A current source supplies a constant current to a load, regardless of the demand by the circuit or the size of the load. In Fig. 1-22A, this may loosely be represented by a voltage supply, V, in series with an infinite resistor, R. In practical cases, R is large compared to the size of the load impedance.) As the supply voltage across the equivalent circuit in Fig. 1-27 rises from 0 to +6, the voltage across the diode follows the normal sine waveshape for it does not conduct. Once it starts to conduct, the voltage across the diode will remain constant at the 6-volt reverse-breakdown until the supply drops below this. Thereafter, the sinusoidal shape is resumed.

When the top of the diode becomes negative with respect to the bottom (second half of the input cycle) and the diode is in the forward conducting mode, the voltage across the diode maintains its sinusoidal form until −0.85 volt, the voltage at which it starts to conduct. The voltage remains constant until the supply once again drops below this value. (Actually, the voltages are slightly greater than the 6 and −0.85 volts noted, as there is a voltage drop in the resistors of the equivalent circuit).

Since the diodes in practical circuits are not fed from ideal constant current or voltage supplies, the shape of the voltage across the diode is between the two output voltage curves shown in Fig. 1-27. Other discrepancies from the curves are due to forward and reverse impedances of the diode and their nonlinear characteristics.

SWITCHING TRANSIENTS

In the ideal case, a diode can be switched instantaneously from a forward conducting state to a reverse nonconducting state, and back again to the forward mode. In each instance, the switching is not smooth. There is a time lag before the diode reaches the quiescent condition for the particular mode of operation.

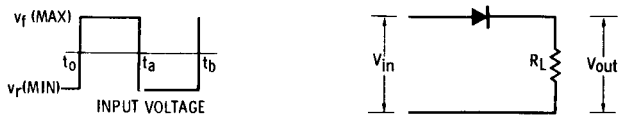
In the circuit of Fig. 1-28B, the voltage drop across the load, R_L, is much larger than the voltage across the forward-biased diode. The forward current in the circuit is a function of the supply voltage and the size of the load resistor. It is relatively independent of the voltage drop across the diode.

Initially, the square-wave voltage (Fig. 1-28A) fed to the circuit is negative and to equal to v_r (min). This results in a reverse-biased, nonconducting diode, since the anode is negative with respect to the cathode.

The diode is switched on at time t_o, when the input voltage is v_f (max). It remains at v_f (max) until time t_a, when the input voltage reverts to v_r (min) and once again the diode is reverse-biased. This curve is repeated in Fig. 1-29A. The various transients in the circuit are drawn below the square-wave input used for switching the diode. It is helpful to examine each time interval individually.

Before t_o, when the input is at v_r(min), the diode does not conduct. The current through the diode is shown in Fig. 1-29D. In this state, there is a minute leakage current. A small negative voltage is developed across the load due to this current, as shown in Fig. 1-29C. The voltage across the load at all portions of the switching cycle is shown in this curve, while Fig. 1-29B describes the voltage across the diode. When the diode does not conduct, it is effectively an open circuit, and the entire supply voltage (less the voltage drop across the load due to the leakage current) is across the diode.

After time t_o, the diode is put into the forward-bias condition by the square wave. The maximum forward current through the circuit is de-



(A) Input signal. (B) Diode circuit.

Fig. 1-28. Input signal fed to diode circuit (diode is not driven into reverse-breakdown region).

termined by the size of the load resistor and is equal to $i_f(max) = v_f(max)/R_L$, by Ohm's law. As shown in Fig. 1-29D, the diode is conducting during this portion of the cycle, and the voltage across the diode rises to a peak value. This voltage, shown in Fig. 1-29B, is due to the diode behaving as a resistor rather than as a semiconductor while it is being switched. The size of this hypothetical resistor determines the size of the peak voltage across the diode, since $v = i_f(max)\ (R_b)$, where R_b is the

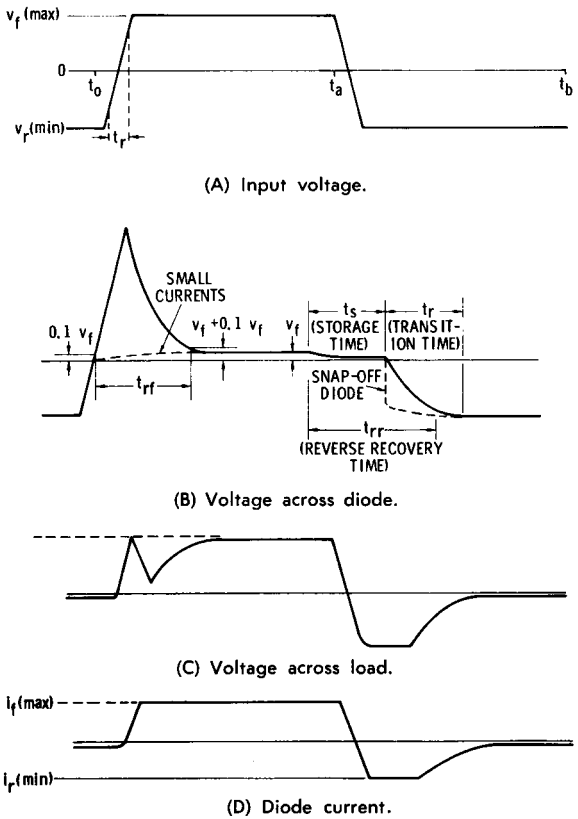


Fig. 1-29. Current and voltage for Fig. 1-28.

resistance of the diode at the instant it is switched on. Overshoot increases as the forward diode current (i_f) is increased and the rise time (t_r) of the input signal is decreased. (Rise time is the time it takes for the input of the square wave to rise from 10% to 90% of its final value. It is illustrated in Fig. 1-29A.) If the forward current is low, there is no peak, but the signal takes the shape of the broken line shown in the forward-bias portion of the curve in Fig. 1-29B.

The voltage across the diode then drops to v_f. This is the approximate 0.6 volt for silicon diodes and the 0.2 volt for germanium devices, as discussed above.

The voltage across the load rises to its peak value at the instant the diode is turned on. This is equal to R_L multiplied by the steady-state forward current in the circuit, $i_f(max)$. The voltage then drops and once again rises to a constant level. The voltage across R_L is the difference between the supply and diode voltages.

The forward recovery time, t_{rf}, covers the period of time from the instant the diode starts to conduct until it reaches some point within 10% of v_f. The latter point is 10% greater than v_f if there is overshoot and 10% less than v_f if the diode voltage rises slowly as shown by the dotted line curve marked "small currents."

The diode voltage remains at v_f until time t_a, when the input voltage switches to a negative value. The diode current drops rapidly to $v_r(min)/R_L$, as seen in Fig. 1-29D. The diode voltage remains positive for a short period, known as storage time, t_s. It then gradually drops to a constant value, $v_r(min)$. This interval of time, t_r, is known as the transition time. The reverse recovery time (t_{rr}) is the period of time from t_a to the time the diode is a specific high impedance, or conducts only a low leakage current.

Practically the entire supply voltage is then across the open circuit diode, as before time zero. Here, too, the voltage across the load is the difference between the input voltage and the voltage across the diode.

Special diodes have been developed to improve the characteristics. As can be seen by the broken line in Fig. 1-29B, the "snap-off" or charge-storage diode, reduces the transition time tremendously.

The hot-carrier diode has practically ideal switch characteristics. There is virtually no overshoot, and it can be used up to microwave frequencies.

The junction of the hot-carrier diode is a metal and a semiconductor. The generated noise is minute. When it is forward-biased, there is about 0.25 volt across the device. One important precaution—current surges must be carefully limited to safe values.

PIN DIODES

The different types of switching diodes that will perform at extremely high rf frequencies are scarce indeed. Many diodes will function up to about 200 or 300 MHz. Above this frequency, we must turn to special devices, such as the PIN diodes. Even these devices are so frequency sensitive that limits are set by the package in which they are mounted.

The diode is composed of three sections. There are the usual p- and n-type semiconductor materials. Sandwiched between the p- and n-slabs is an intrinsic or pure layer of high resistivity material. The breakdown voltage is a function of the width of the intrinsic region.

The operation of the PIN diode can be divided into two bands separated, more or less, at a frequency f_o. Below f_o, the diode performs as if it were the conventional junction device with all its inherent nonlinearity and rectification properties. Above f_o, the diode is a pure resistor. It does not rectify at these frequencies. The resistance is dependent upon the dc current flowing through the device and, at room temperature, is approximately equal to 48/I, where I is the dc current through the diode expressed in milliamperes. It may vary from 1 ohm to over 10,000 ohms. The frequency at the dividing point, f_o, is equal to $1/6.28\tau$, where τ is referred to as the *recombination lifetime* of the device.

Changing the dc across the device changes the rf resistance. It will thus behave as a switch acting as a short circuit when the resistor is low, and acting as a relatively open circuit when the resistance is high. If an audio signal is applied across the diode, the variation in resistance will conform to the applied intelligence. Hence, the PIN diode can serve in a modulating function, as well as in an rf switching capacity.

CAPACITIVE DIODES (VARACTORS)

Reverse-biased diodes behave like capacitors whose capacitance varies with the applied voltage. The capacitance of a junction diode may be as high as 100 pF. It is related to the applied voltage by the formula $1/V_r^{1/3}$ to $1/V_r^{1/2}$, where V_r is the reverse voltage applied across the diode. The relationship between voltage and capacity is highly nonlinear. The capacity increases as the reverse voltage across the diode is reduced or made slightly positive. The Q (the ratio of the capacitive reactance to the resistance) can be as low as 50, but is more likely to be near 300.

In using ordinary diodes in rf circuits, the capacitance may become an important factor. Although exact values of the diode capacitance are rarely stated in diode specifications, its existence must not be ignored in design work.

Varactors are specifically designed to afford the maximum capacitance range. They may be grouped into several categories separated by the frequency range in which the semiconductor is designed to operate, and the power it can dissipate.

The equivalent circuit of the varactor diode is a capacitor, C, in series with a voltage-dependent resistor, R. The important cutoff frequency characteristic, f_c, can be derived from these two values:

$$f_c = \frac{1}{2\pi RC} \tag{1-22}$$

where,

f_c is the cutoff frequency of the diode in Hz,
R is the equivalent resistance in ohms,
C is the equivalent capacitance in farads.

This is the frequency at which the Q of the diode is equal to 1, because:

$$Q = \frac{1}{2\pi fRC} \tag{1-23}$$

where,

f is any frequency in Hz at which the diode is used.

The voltage breakdown characteristic, V_B, as well as the maximum power dissipated, must be considered in all designs.

The diode capacitor (varactor) has ben used to replace mechanical tuning elements in rf circuits. The frequency of a resonant circuit is adjusted by varying the voltage across the diode. A typical tank circuit is shown in Fig. 1-30.

The varactor may also be used in switching, limiting, harmonic generation, and parametric amplification applications.

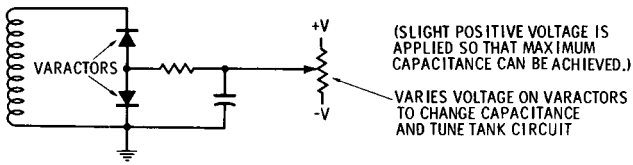


Fig. 1-30. Typical circuit using a varactor.

LIGHT-SENSITIVE P-N JUNCTION DIODES

Semiconductor diodes have been designed to relate the intensity of light impinging on the device with one of the characteristics of the device. These diodes may be classified into two major groups. In one group, the photoconductive semiconductor is a device whose *resistance* varies inversely with the increase in intensity of the light flux. The second group of light-sensitive devices are photovoltaic cells. Here, a *voltage* proportional to the intensity of illumination is developed across the terminals of the semiconductor.

The most frequently used materials for photoconductive semiconductor devices are germanium, silicon, lead sulphide, and cadmium sulfide. The resistance in the dark of devices made from these and other semiconductor materials is theortically infinite. Due to thermal conditions, there is some finite resistance even when there is no light present. This is referred to as "dark resistance," and may be as high as 10^8 ohms. Under lighted conditions, the resistance may fall to below 1000 ohms. The voltage across the diode must be kept within the specified values so that it will not avalanche. The power dissipation of the device must also be limited.

The diode is a frequency-dependent device. In general, cadmium sulphide cells respond to visible light, while lead sulphide and germanium are more sensitive to the infrared section of the electromagnetic spectrum.

The noise produced by the device is in the order of the magnitude of noise generated by a resistor of like value. Noise increases with ambient temperature, as does the dark current. Hence, the dark current can be used as a measure of the noise.

Photovoltaic devices, known as sun batteries, generate voltages that are in no way related to the area of the cell. The voltage is solely dependent on the light intensity hitting the cell, and can be as high as 0.6 volt per individual device. The current produced by the device *is* dependent on the area of the cell, the intensity of the light, as well as the size of the load driven by the device. It is in the order of magnitude of several milliamperes.

The current counterpart of the photovoltaic component is the photodiode. It acts as a high resistance current generator when reverse biased. The current varies with the intensity of light absorbed by the diode.

The LED (Light Emitting Diode) differs from the other devices in that the diode emits light as a current passes through the junction in the forward direction. Different materials are required to produce the various colors of the visible and infrared spectrum.

TUNNEL DIODES

The final semiconductor device considered in this chapter is the p-n junction tunnel diode. It is somewhat different from the other types of diodes because its characteristics enable it to function as an oscillator, amplifier, or switch. This is due to the relatively large amount of impurities in the semiconductor material.

The curve of the voltage-current relationship is shown in Fig. 1-31. Note the broken line showing the curve for the ordinary diode. Several spe-

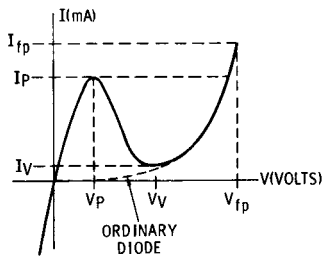


Fig. 1-31. Characteristic curve of a tunnel diode.

cific points on the tunnel diode curve are of interest to the designer.

At zero voltage, the current is zero. It rises immediately to a peak current, I_p mA, when the voltage rises to V_p volts. This increase in current is in the first of the two positive resistance sections of the characteristic curve. It is followed by a negative resistance section where the current drops to the valley current, I_v, when the valley voltage is V_v (about 300 to 400

mV). It turns up once again (following the conventional diode characteristic with a positive resistance) to a maximum allowable peak current of I_{fp} when the forward peak voltage is V_{fp}. In some specifications, I_p and I_{fp} coincide, resulting in a lower value of V_{fp}.

The equivalent circuit of the diode in the negative resistance region is a negative resistance, $-R_N$, shunted by a capacitance in series with an inductance and the series resistance of the inductance. These factors limit the frequency at which the diode may be used.

The ratio of peak-to-valley current is an important factor frequently stated in specification, as is the negative resistance, $-R_N$, of the device between I_p and I_v.

Some of the parameters are temperature-dependent. On the plus side, the unit as a whole is not affected to any great degree by nuclear radiation.

The peak voltage and current are relatively free of change due to temperature. The valley current, however, increases rapidly with an increase in temperature and the valley voltage decreases at the rate of -1 mV/°C. The negative resistance decreases about -0.4 ohm for each degree of rise in temperature.

Diodes are made of different materials and applicable to different circuits and functions. Silicon diodes have a low I_p:I_v ratio—approximately 3:1. The negative resistance can be approximated from the ratio $220/I_p$. Silicon diodes are used mainly as switches operating in high ambient temperatures. Germanium units have a higher I_p:I_v ratio—in the order of 6:1. Its negative resistance is about $120/I_p$, and it has relatively good stability with temperature variations. Gallium-arsenide diodes, used exclusively in oscillators, have an I_p:I_v ratio greater than 10:1, and a negative resistance approximately equal to that of the silicon units. Gallium antimonide is the lowest noise unit of the lot. While its minimum I_p:I_v ratio is about 12:1, its negative resistance is the lowest of all—about $60/I_p$. In general, all these diodes can be damaged by heat and static electricity. They should be handled with caution.

Biasing the Tunnel Diode

The diode can be biased in any one of three ways: monostable, astable, and bistable. The various modes of operation can best be illustrated using the circuit in Fig. 1-32. Here, the dc bias is obtained from a battery. A pulse is then fed to the circuit to upset the quiescent condition.

If biased in the monostable mode, the load line can cross the curve at either positive resistance region. This is shown in Fig. 1-33A.

Assume first that the supply is at voltage V for load line (1) as shown in Fig. 1-33B. When a positive pulse is applied to the diode, it raises the bias voltage and the current rises along the curve to V_p-I_p. Unstable in this condition, the voltage jumps to V_f while the current remains at I_p. Since the pulse is of short duration, the current and voltage drop to V_v-I_v, jump to V_x-I_v, and climb once again to the Q starting point. The idealized

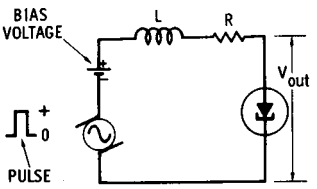
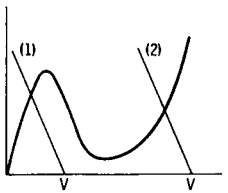
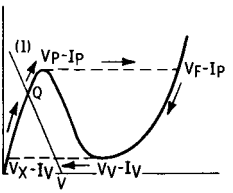


Fig. 1-32. Pulse fed to tunnel diode biased by a battery.

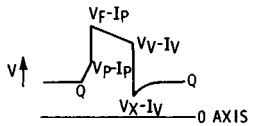
curves of the output voltage and diode current for the circuit of Fig. 1-32 are shown in Figs. 1-33C and 1-33D, respectively.



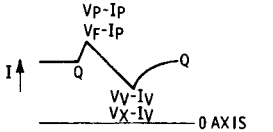
(A) Monostable.



(B) Current path and relative voltage.



(C) Output voltage for Fig. 1-32.



(D) Diode current for Fig. 1-32.

Fig. 1-33. Tunnel-diode curve with load line(s).

A similar analysis can be made if load line (2) in Fig. 1-33A is the monostable load line. In either case, the mode of operation can be used in a relaxation oscillator or switching circuit. In the astable mode, as used in amplifiers or oscillators, the load line crosses the negative-resistance region, as shown in Fig. 1-34A. Here, the load line starts at Q, but a pulse causes it to rise to V_p-I_p and pursue the same course as shown in Fig. 1-33B.

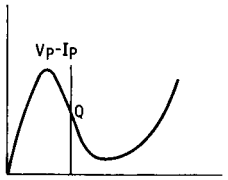
The bistable circuit load line is shown in Fig. 1-34B. This bias mode is used in relaxation oscillators and switching circuits.

Assume the action starts when the diode is biased at Q. If the pulse is large enough in the positive direction to raise the load line above the V_p-I_p point, the line shifts for an instant to the location in Fig. 1-34C. The new stable bias point will stabilize at Q1 as shown in Fig. 1-34B.

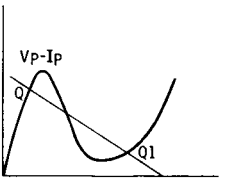
If the next pulse is in the negative direction, and is of adequate amplitude to move the load line so that it is below V_v-I_v for an instant (Fig. 1-34D), the quiescent point will reset itself at Q.

The tunnel diode has three basic functions: oscillator, switch, and amplifier. Its use as a switch (e.g., to perform high-speed logic functions) has

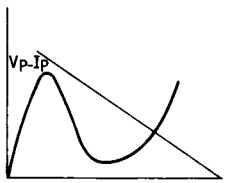
been discussed previously. The important parameters here are the peak and valley voltages and currents. The capacitance of the diode and associated inductance are important in determining the switching speed limits.



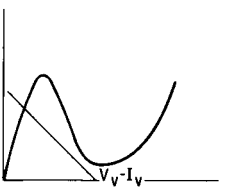
(A) Astable load line.



(B) Bistable load line.



(C) Load line shifts with high-level pulse.



(D) Large negative pulse shifts load line below V_V — I_V momentarily.

Fig. 1-34. Tunnel-diode curve.

When it is used as an amplifier, the diode is biased in the negative resistance region, and is connected to an L-C resonant tank circuit. The negative resistance cancels a portion of the positive resistance inherent in tank circuits. In this application, the negative resistance is obviously an important parameter. The noise generated by the diode should be low. It is directly proportional to the negative resistance and I_o, the inflection current. (I_o is the current when the diode is biased at the approximate center of the negative resistance region of the curve.)

As an oscillator and modulator, the tunnel diode is usually biased in the negative-resistance region of the curve. In mixer and relaxation-oscillator applications. the bias should be in the positive-resistance region nearest zero. All parameters are reasonably important in this application. The frequency of oscillation is always less than the resistive cutoff frequency f_{ro} of the diode.

Note the reverse characteristic of the tunnel diode in Fig. 1-31. The reverse current starts to rise at 0 volts, and continues to increase. The reverse breakdown voltage is 0 volts. Should it be required to get relatively high current at 0 volts, the diode can be biased in the reverse direction. The efficiency of rectification is very high. A diode operated in this fashion is known as a back diode or tunnel rectifier.

In the forward direction, the specially designed back diode has a slight peak current that is almost independent of voltage when small forward voltages are applied.

Chapter 2

THE BIPOLAR TRANSISTOR

A transistor is essentially a diode with an additional n-type or p-type slab, forming two p-n junctions. If the p-type material is sandwiched between two n-type slabs, an npn transistor is formed. In a pnp transistor, the n-type material is between two p-type slabs.

Effectively there are two diodes. The middle slab is known as the base, one end slab is referred to as the emitter, and the other as the collector. The base-emitter diode or junction is normally forward biased and the base-collector junction is reverse biased.

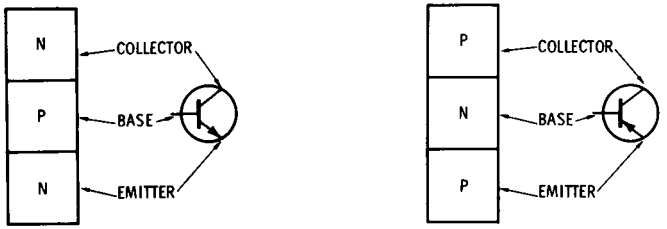
The current through the lead connected to the collector is related to the current in the base lead. The collector current is approximately beta (β) multiplied by the base current. Hence the transistor may be thought of as a diode (base-emitter junction) with a current gain of β. Similiarly, the current through the collector lead is approximately alpha (α) times the current in the emitter lead. Alpha and beta are two current-gain factors to be used extensively throughout the text.

THE BASIC CONCEPT

The two types of transistors, npn and pnp, are drawn in Fig. 2-1. As was the case with the diode, the direction of the electron current is opposite to the direction of the arrow in the symbol.

In the npn device, the base must be made positive with respect to the emitter, if there is to be current through this junction. Current will flow from the emitter to the base in the direction opposite to that depicted by the arrow in the symbol.

For the pnp device, the base-emitter junction must be biased opposite in polarity to that of the npn transistor, if there is to be current from the base to the emitter. The emitter must be made positive with respect to the base. Once again, the arrow in the symbol points opposite to the direction of the electron current.



(A) Npn transistor. (B) Pnp transistor.

Fig. 2-1. Schematic representations.

As in the case of all forward-biased diodes, a voltage is developed across the base-emitter junction. This is the usual diode voltage—about 0.2 volt for germanium transistors and 0.6 volt or somewhat more for silicon devices.

When the base-emitter junction is in the conducting mode, the ac resistance in series with the emitter lead is referred to by the symbol r_e and known as the emitter resistance. It is equal to $26/I_E$, where I_E is the emitter current expressed in milliamps. This is identical to the resistance of the forward-biased diode.

The base current, multiplied by a factor of beta, is the major portion of current in the collector. Beta is merely a number indicating the ratio of collector current to base current. In a similar fashion, the major portion of the current in the collector may be related to the current in the emitter. The collector current is alpha times the emitter current. Alpha is a ratio relating the collector to the emitter current. It is always less than "1" for the junction transistor.

The total collector current is due to two major factors. One is the gain of the transistor: αI_E or βI_B. The second factor is due to the leakage current through the reverse-biased base-collector junction.

In order to avoid confusion, from this point on, the collector current due to the gain of the device will be referred to simply as collector current. The symbol is I_C. The collector current due to all factors will be called total collector current and will have the symbol I_C (total).

The collector is usually reverse biased with respect to the base. In the npn transistor, the base is made of p-type material and the collector (as the emitter) of n-type slabs. To reverse bias the base-collector junction, the collector is made positive with respect to the base.

Because the base and collector in the pnp transistor are composed of n-type and p-type slabs, respectively, the collector is reverse biased by making it negative with respect to the base.

Summing up: If a transistor is to conduct, the base-emitter junction must be forward biased and the base-collector junction reverse biased. This is shown in Fig. 2-2. Should both junctions be reverse biased, there will be no conduction of current from the emitter through the collector.

The actual operation of the device can be determined using the pnp transistor in Fig. 2-3 as an example. The details apply equally to the npn transistor. In the latter instance, however, the current is in the opposite direction.

The total current, I_E, is in the emitter. It is generally safe to assume that this is the maximum current through any element of the transistor.

(A) Type npn. (B) Type pnp.

Fig. 2-2. Relative voltages as normally applied to transistors.

Most of I_E is in the collector lead as well. The portion of I_E in the collector is equal to α (alpha). Mathematically, α is:

$$\alpha = I_C/I_E. \qquad (2\text{-}1)^*$$

The collector current is equal to αI_E. α must be less than "1" for the collector current is always less than the emitter current. Usually α is greater than 0.95 and is frequently indistinguishable from "1."

The tiny portion of emitter current left for the base is $I_B = I_E - I_C = I_E - \alpha I_E = I_E(1 - \alpha)$.

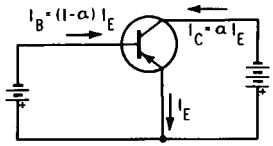


Fig. 2-3. Current division in a transistor.

The npn transistor operates in the same manner; only the direction of current is reversed. (Examples throughout the text will usually involve the npn transistor. Everything will apply as well to the pnp device except that the polarities of the supply voltage must be reversed.)

Despite the fact that the forward and reverse biases are set by voltages, the transistor operates essentially as a current device. The voltage between the base and emitter must be applied in such a manner that there is a specific base current, I_B. The voltage between the emitter and collector must be applied in the proper polarity to allow collector current through the transistor. The relative voltage between the base and collector must be such that there is no current through this reverse biased junction. (Actually, there is a leakage current through this junction.)

Beta (β) has been defined as the current gain existing between the base and collector. If the base current is $I_B = (1 - \alpha)\ I_E$ and the collector current is $I_C = \alpha I_E$, the dc current gain of the device is:

$$\beta = \frac{I_C}{I_B} = \frac{\alpha I_E}{(1-\alpha)} I_E = \frac{\alpha}{1-\alpha} \qquad (2\text{-}2)^*$$

This relates the current gain (or loss) from emitter to collector (α), to the current gain from the base to collector, β. Similarly, if β is the known quantity, α can be determined from the relationship:

$$\alpha = \frac{I_C}{I_E} = \frac{\beta}{\beta + 1} \qquad (2\text{-}3)^*$$

The two equations relate two important quantities which are used in the various modes of operation.

The transistor is normally connected into a circuit in one of three ways: the common base, common emitter, and common collector. They are also referred to as grounded base, grounded emitter, and grounded collector, respectively.

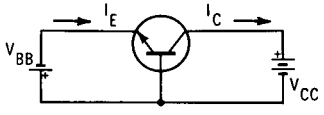


Fig. 2-4. Common-base or grounded-base circuit.

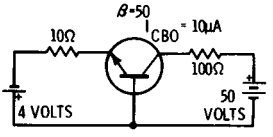


Fig. 2-5. Common-base example.

Common Base

A drawing of the common base circuit is shown in Fig. 2-4. Here, the input and output voltages are considered with respect to the base. The emitter-base junction is forward biased by the V_{BB} supply. The collector-base junction is reverse biased by the V_{CC} supply. The transistor will conduct current from the emitter to the collector (or vice versa) only when the supplies are connected with the polarities shown.

The total current through the collector is α multiplied by the emitter current or αI_E plus the additional leakage current through the reverse-biased base-collector junction. This leakage current, I_{CBO}, or simply I_{CO}, is the current from the collector to the base junction with the emitter open. It is the current through the collector when the emitter current is zero. The total collector current is:

$$I_C \text{ (total)} = \alpha I_E + I_{CBO} \qquad (2\text{-}4)$$

An example, to determine the operating point of a transistor, uses the circuit and information furnished in Fig. 2-5. A silicon transistor with a

beta of 50, is assumed. The voltage across the base-emitter junction of a silicon transistor is approximately 0.6 volt. The current entering the emitter, by Ohm's law, is:

$$I_E = \left(\frac{4 \text{ volts} - 0.6 \text{ volt}}{10 \text{ ohms}}\right) \text{amps} = \left(\frac{3.4}{10}\right) (1000) \text{ mA}$$

Note that at first, I_E was expressed in amps. To convert the current to mA (milliamps), the solution to the equation was multiplied by 1000, since there are 1000 milliamps for each amp. Hence

$$I_E = 3.4 \times 10^2 \text{ mA}.$$

The dc emitter resistance, r_E, as well as the dc base resistance, r_B, are negligible compared to the effect of the resistance of the 10-ohm emitter resistor.

The collector current due to the emitter-base current is αI_E. From Equation 2-3, $\alpha = \beta/(1+\beta) = 50/51 = 0.98$. The collector current is $(0.98)\ (3.4 \times 10^2)$ mA $= 3.34 \times 10^2$ mA.

The contribution of the leakage current to the collector current is 10 microamps, and is negligible in this case. The voltage drop across the 100-ohm resistor is (100 ohms) $(3.34 \times 10^2$ mA) = (100 ohms) (.334 amps) = 33.4 volts. The voltage between the base and collector is the collector supply voltage less the drop in the 100-ohm collector resistor, or 50 volts − 33.4 volts = 16.6 volts. This, added to the 0.6 volt from the base to emitter, is the collector-emitter voltage. It is 16.6 + 0.6 = 17.2 volts.

Most of the power dissipated by the transistor is in the collector circuit. From the equation equating power to the product of voltage and current, the transistor dissipates 17.2 volts × 0.334 amp or 5.75 watts.

It is interesting to note that while there is less collector current than emitter current there is a voltage gain. With 4 volts at the input, 33.4 volts was developed across the 100-ohm output load resistor. This is due to the difference of impedance in the two circuits.

Now, superimpose an ac signal on the 4-volt dc emitter supply voltage, and let the peak-to-peak voltage of the signal be 2 volts. The input will vary from 3 to 5 volts because the 1-volt peak ac is added to the 4-volt bias during one half of the cycle, and subtracted during the second half. Find the peak-to-peak ac voltage across the 100-ohm load resistor in the collector circuit.

The emitter current is (5 volts − 0.6 volt)/10 ohms, or 0.44 amp at the peak of the ac signal and (3 − 0.6 volt)/10 ohms or 0.24 amp at the crest of the ac input. The respective collector currents are alpha multiplied by the emitter currents, or (0.98) (0.44) = 0.431, and (0.98) (0.21) = 0.235. At the peak of the signal, the voltage across the 100-ohm resistor is 100 ohms × 0.431 amp or 43.1 volts. At the crest, the voltage drops to 100 ohms × 0.235 amp = 23.5 volts. The peak-to-peak voltage across the

100-ohm resistor is the difference of the two calculated values or 43.1 volts − 23.5 volts = 19.6 volts.

With 2 volts peak-to-peak at the input, there is 19.6 peak-to-peak signal volts at the output. This is a voltage gain of 19.6/2 or 9.8. This is about the same as the ratio of the resistor in the collector circuit to the resistor in the emitter circuit. The following rule can thus be stated:

IN THE COMMON BASE CONFIGURATION, USING HIGH BETA TRANSISTORS, THE AC VOLTAGE GAIN IS APPROXIMATELY EQUAL TO THE RATIO OF THE IMPEDANCE IN THE COLLECTOR CIRCUIT TO THE IMPEDANCE IN THE EMITTER CIRCUIT. THE EMITTER AND COLLECTOR CURRENTS ARE ABOUT EQUAL.

The power gain is equal to the current gain multiplied by the voltage gain. Since the current gain in high beta transistors is practically equal to "1," the power gain is approximately equal to the voltage gain.

Also note that there is no phase shift between the input and output signals. They are both at their peaks and crests at the same instant of time.

Common Emitter

A drawing of the most-used configuration, the common-emitter transistor circuit, is shown in Fig. 2-6. Of all arrangements this circuit can supply the maximum power gain. There is also current and voltage gain.

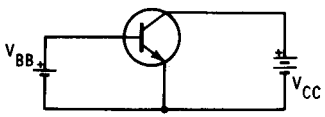


Fig. 2-6. Common-emitter circuit.

Input and output voltages are referred to the emitter. The base-emitter junction is forward biased by virtue of the polarity of V_{BB}. V_{CC} reverse biases the collector with respect to the emitter. The base-collector junction is reverse biased since the base voltage is only about 0.2 volt above the emitter voltage for germanium devices, and 0.6 or 0.7 volt higher than the emitter voltage where silicon units are involved.

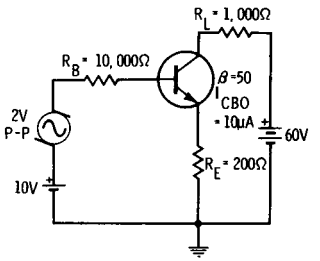
The collector current is beta times the base current. There is an additional leakage current, I_{CBO}, through the base-collector junction due to this reverse-biased diode. Because the collector current is beta multiplied by the base current, the collector current due to leakage is $(\beta)I_{CBO}$ and equal to I_{CEO}. I_{CEO} is the collector-to-emitter current, with the base open. The total collector current due to leakage current and base current is:

$$I_C \text{ (total)} = \beta I_B + \beta I_{CBO} = \beta I_B + I_{CEO} \qquad (2\text{-}5)$$

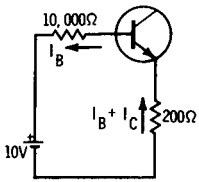
A practical circuit is shown in Fig. 2-7A. The dc bias circuit for the base-emitter diode is lifted out of Fig. 2-7A and is shown in Fig. 2-7B. The base current is determined by the 10-volt battery in series with the 10,000-ohm resistor, the 200-ohm resistor, the dc emitter resistance (r_E),

the resistance in the base, and the voltage drop across the junction. Let us consider each of these factors.

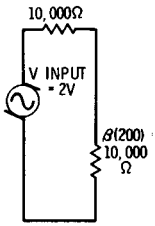
The total dc voltage supplied to the circuit is the 10 volts. The drop across the junction reduces the total available voltage. Assuming a silicon transistor, this drop is about 0.6 volt. Hence, the total voltage affecting the base current is $10 - 0.6$ volts, or 9.4 volts.



(A) Common-emitter circuit.



(B) Base circuit of Fig. 2-7A.



(C) Input impedance of Fig. 2-7A.

Fig. 2-7. Practical common-emitter circuit.

The total resistance in the circuit consists of four items:

1. One item is the 10,000 ohms in the base circuit. Only base current is in this resistor.
2. The base resistance is a resistor in the transistor that is theoretically in series with the base. I_B is the only current through this resistor. Only the dc resistance, r_B, may be considered in the base equivalent circuit. However, it is usually negligible compared to all other resistors.
3. The 200-ohm resistor in the emitter passes two currents. These are the base and the collector currents which add up to the emitter current. Written mathematically, $I_E = I_B + I_C = I_B + \beta I_B = (1 + \beta) I_B$. If beta is much larger than "1," as it usually is, the emitter current is $I_E = \beta I_B$. Because of this, the resistor in the emitter has a larger effect on the base current than just its 200 ohms. It behaves as if a resistor equal to $\beta \times 200$ were in the base circuit. In this case, it is $50 \times 200 = 10{,}000$ ohms.

4. The dc emitter resistance, r_E, is usually negligible. It should not be confused with the ac emitter resistance, r_e, which is equal to $26/I_E$ when I_E is expressed in milliamperes. The r_E is usually much smaller than r_e.

To sum up, the base current is determined by the total voltage in the base-emitter circuit (10 volts − 0.6 volt = 9.4 volts) and the total resistance. The total resistance is the 10,000-ohm resistor, plus the base resistance, plus the 10,000-ohm resistance due to the 200-ohm resistor in the emitter multiplied by the beta of 50, plus the emitter resistance reflected into the base circuit. The base and emitter resistors are negligible. The base current can be found from the Ohm's law equation:

$$I_B = \frac{9.4 \text{ volts } (1000)}{10{,}000 + (200)(50)}$$

As in the previous problem, the equation is multiplied by 1000 so that I_B will be expressed in milliamps. Solving for I_B, it is equal to 0.47 mA = 0.47×10^{-3} amps.

The total collector current is beta multiplied by the base current or $50 \times 0.47 = 23.5$ mA plus beta multiplied by I_{CBO} or $50 \times 10 \times 10^{-6} =$ 0.5 mA. The sum of the two factors is 24 mA = 24×10^{-3} amps. The voltage across the 1000-ohm resistor is 1000 ohms $\times$ 24×10^{-3} amps = 24 volts.

The voltage across the transistor, from the emitter to the collector, is 60 volts less the sum of the voltage across the 1000-ohm resistor (24 volts) and the voltage across the 200-ohm resistor. The current through the 200-ohm resistor is $I_E = I_C + I_B = 24 \times 10^{-3}$ amps $+0.47 \times 10^{-3}$ amps $= 24.47 \times 10^{-3}$ amps. The voltage across the resistor is $I_E \times 200$ ohms $= 24.47 \times 10^{-3} \times 200 = 4.894$ volts.

The voltage across the transistor is $60 - 24 - 4.894 = 60 - 28.894 =$ 31.106 volts .The power dissipated in the collector circuit is I_C (total) $\times$ $V_C = (24 \times 10^{-3}$ amps) (31.106 volts) = 0.747 watt.

The primary factor that must be noted from this problem is that, when seen from the base of the transistor, the resistance in the emitter appears as if it is multiplied by a factor of beta. Similarly, the resistance in the base circuit will appear divided by beta when viewed from the emitter circuit.

A procedure similar to that employed for finding the ac voltage gain of the common base circuit can also be used here. The approximate voltage gain of the transistor for the circuit in Fig. 2-7 is the ratio of the resistor in the collector circuit to the resistor in the emitter circuit or $1000/200 = 5$. The voltage gain of the transistor may also be defined as the ratio of the ac voltage across the collector load resistor or between the collector and ground, to the voltage between the base and ground. The following derivation can be used to prove that the two statements of gain are identical.

The greatest portion of the ac load in the collector circuit is R_L. The ac current in this circuit is βI_b or beta multiplied by the ac current going into the base. The ac output voltage across the load resistor is $\beta I_b R_L$.

The major part of the impedance in the base circuit is due to the resistor, R_E, in the emitter. Looking into the base, this impedance is βR_E. The ac base current is I_b. The voltage at the input circuit is therefore $\beta R_E I_b$.

The ratio of the two voltages, defined as the voltage gain of the transistor, is $\beta I_b R_L / \beta I_b R_E = R_L / R_E$. Hence, both statements of gain are identical.

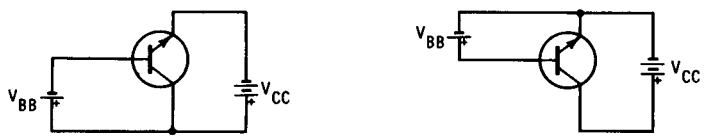
The overall voltage gain of the circuit is less than the voltage gain of the transistor itself. There is an input resistor of 10,000 ohms in series with the voltage supply. The input voltage is divided between this resistor and the input impedance of the transistor. This input impedance is $\beta R_E =$ 50 (200 ohms) = 10,000 ohms (See Fig. 2-7C). Utilizing the voltage divider equation, the voltage at the base is equal to 10,000/(10,000 + 10,000) $V_{input} = \frac{1}{2}$ (V_{input}). The overall circuit voltage gain is only one-half the previously calculated ac gain of the transistor, or 2.5.

Since the current gain of the transistor is β, the power gain is β multiplied by the voltage gain or $\beta R_L / R_E$.

There is a 180° phase shift between the input and output voltages. When the voltage at the base is at a peak in the cycle, it is at its crest at the collector.

Common Collector

In the common collector circuit in Fig. 2-8, the input and output voltages are stated with respect to the collector. The transistor is in the conducting mode when the supplies are connected as shown in Fig. 2-8A or 2-8B.



(A) Bias battery base-to-collector. (B) Bias battery base-to-emitter.

Fig. 2-8. Two versions of the common-collector circuit.

The ratio of the emitter current, I_E, to the base current, I_B, is $I_E/I_B = 1/(1-\alpha)$, from Fig. 2-3. If α is large, approximately equal to "1," the current ratio is approximately equal to β. The current gain of this arrangement is just about equal to the current gain of the common emitter circuit, or β.

The total emitter current is $(\beta + 1)$ multiplied by the total base current. If there is no base-to-collector leakage, it is simply $(\beta + 1) I_B$. Should there be leakage (and it is assumed that all the leakage current is through the base emitter junction), the total emitter current is:

$$I_E \text{ total}) = (\beta + 1) I_B + (\beta + 1) I_{CBO} = I_C + I_B + I_{CEO} + I_{CBO} \quad (2\text{-}6)$$

A practical circuit is shown in Fig. 2-9. Note the similarity between this and the one in Fig. 2-7A.

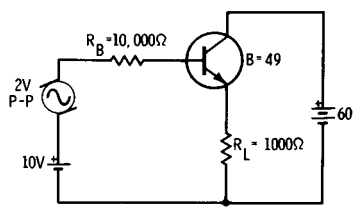
The dc base current is primarily due to the 10-volt supply minus the 0.6-volt drop across the base-emitter junction, the 10,000-ohm resistor in the base circuit, and, finally, the 1000-ohm load resistor reflected into the base circuit as $(\beta + 1)\ (1000) = 50{,}000$ ohms.

(It was previously stated that the impedance reflected into the base circuit due to the resistor in the emitter circuit is β multiplied by the emitter resistor. It is more accurate to multiply this resistor by $(\beta + 1)$, a practice followed in this particular example, although in practical design work, $(\beta + 1)$ is essentially equal to β).

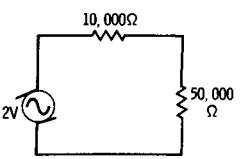
The total resistance in the base circuit is 10,000 ohms + 50,000 ohms = 60,000 ohms. The dc base current is $(10 - 0.6)$ volts/60,000 ohms = 1.57×10^{-4} amps. Assuming zero leakage current, the emitter current, from Equation 2-6, is equal to $(\beta + 1)I_B = 50\ (1.57 \times 10^{-4}\ \text{amps}) = 7.85 \times 10^{-3}$ amp. The voltage across the load resistor is $I_E R_L = (7.85 \times 10^{-3}\ \text{amps})\ (1000\ \text{ohms}) = 7.85$ volts.

(It is interesting to note here that if it is assumed that $(\beta + 1)$ is so large as to be indistinguishable from β, the emitter current can be calculated to be $49(1.57 \times 10^{-4}\ \text{amps}) = 7.69 \times 10^{-3}$ amps and the voltage across the load resistor would then amount to $(7.69 \times 10^{-3})\ (1000) = 7.69$ volts. The difference between this and the more accurately calculated value is $7.85 - 7.69 = 0.16$ volt with an approximate 2% error. The error is negligible in transistor work. However, the purist may object to this practical liberty in the approximation, for if leakage current were present, the collector current would, on paper, be higher than the emitter current. Although of no practical significance in the designed circuit, it does contradict an earlier stated rule which notes that emitter current must be more than the collector current and equal to the sum of the base and collector currents.)

The collector supply is 60 volts. The voltage across the transistor is $60 - 7.85 = 52.15$ volts. With an emitter (and hence collector) current of about 7.85×10^{-3} amps, the power dissipated by the transistor is $52.15 \times 7.85 \times 10^{-3} = 0.41$ watt.



(A) Common-collector circuit.



(B) Base circuit of Fig. 2-9A.

Fig. 2-9. Practical common-collector circuit.

The 2 volts peak-to-peak ac signal superimposed on the 10-volt supply will force the supply to vary from 9 to 11 volts. When the supply is at 9 volts, the current through the emitter circuit is approximately $[50(9 - .6)]/60{,}000 = 7.00 \times 10^{-3}$ amps. The voltage across R_L, by Ohm's law, is $(7 \times 10^{-3})\ (1000) = 7$ volts.

During the portion of the cycle when the supply is at 11 volts, the emitter current is $[50(11 - .6)]/60{,}000 = 8.67 \times 10^{-3}$ amps. The voltage across R_L is $(8.67 \times 10^{-3})\ (1000) = 8.67$ volts. The peak-to-peak ac voltage across R_L is 8.67 volts − 7.00 volts = 1.67 volts.

With a 2-volt ac signal input, the ac output is 1.67 volt. The voltage gain of the overall circuit is less than "1." In this case the voltage gain is 1.67/2 or 0.836.

The ac voltage across the 50,000-ohm impedance in the voltage divider formed by R_B and the reflected impedance of R_L into the base circuit, βR_L, (see Fig. 2-9B) is $[50k/(50k + 10k)]\,2$ or 1.67. This is the same as the output voltage previously calculated as appearing across R_L. This situation can exist only if the ac voltage gain of the *transistor circuit itself* is equal to "1." In actual common collector circuits, the ac voltage gain of the transistor circuit is only slightly less than "1." This does not include the losses due to the resistance of the source.

The input impedance to the transistor is βR_L. The output impedance seen by some external load looking back into the emitter and R_L, is the impedance in the base circuit divided by beta, in parallel with the emitter resistor. In the example, it is 10,000 ohms/β in parallel with 1000 ohms or $10{,}000/49 \approx 200$ ohms in parallel with 1000 ohms. Using the equation for two resistors in parallel, the output impedance is $(200 \times 1000)/(200 + 1000) = 166$ ohms.

THE SWITCH

The transistor can be used as a switch. Consider the common emitter circuit in Fig. 2-10. The collector load current is to be switched on and off by the 40-volt peak-to-peak square wave in the base circuit. Assume that the voltage drop across the base-emitter junction is negligible. The quiescent current through the base circuit is $20/20{,}000 = 10^{-3}$ amps, when zero square-wave signal is applied. The current in the collector circuit is

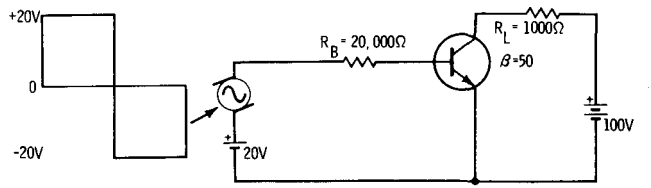


Fig. 2-10. A transistor switch.

$\beta I_B = 50 \times 10^{-3}$ amps, so that the voltage drop across the load resistor, R_L, under quiescent conditions, is 50×10^{-3} amps $\times$ 1000 ohms = 50 volts.

If the square-wave voltage is applied, during the positive half of the cycle it would raise the base voltage to +20 volts above the bias to a total of +40 volts. The base current will then become 40 volts/20,000 ohms = 2×10^{-3} amps. If $\beta = 50$, the collector current is (50) (2×10^{-3} amps) = 100×10^{-3} amps and the voltage across R_L = (1000) (100×10^{-3}) = 100 volts. Since the collector supply is 100 volts, 0 volts remains across the transistor. This is one limiting condition. With a pulse of +20 or more volts superimposed upon the 20-volt bias, the maximum collector current will be 100×10^{-3} amps because the entire 100-volt supply is then across the 1000-ohm resistor in the collector and 0 volts remains to be across the transistor.

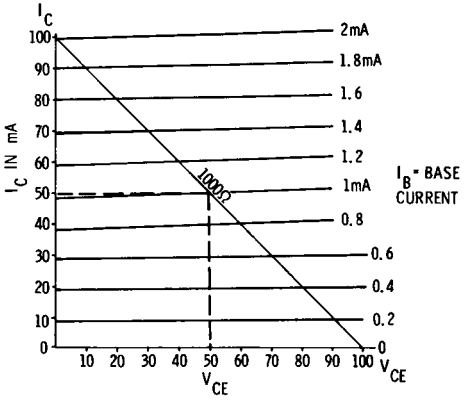


Fig. 2-11. Plot of collector voltage versus collector current.

At the other extreme, when the square wave is in the negative half of its cycle, producing −20 volts, and this −20 volts is superimposed upon the +20-volt bias supply, 0 volts remains as the supply for the base circuit. With no voltage in the base, there will be only leakage current through the collector. Ignoring this, the collector is zero. The voltage across the load resistor is 0 amps multiplied by R_L, or zero. With 0 volts across R_L, the entire 100-volt supply is across the transistor. A negative 20 volts or more will keep the transistor switched off.

Forty volts or more peak-to-peak signal is required to switch the transistor in this example from a maximum conducting to a nonconducting state. This can be demonstrated with the family of $V_{CE} - I_C$ curves in Fig. 2-11.

The voltage from the collector to the emitter is plotted along the horizontal axis and the collector current is plotted along the vertical axis. The collector current is dependent primarily on the base current.

Now, draw a load line for the collector circuit in Fig. 2-10. This is accomplished in several easy steps similar to those described in Chapter 1 in the discussion on diode load lines.

1. Assume that there is 0 mA of collector current. There is no voltage drop across the load resistor. All the supply voltage is across the transistor. In the example, this is 100 volts. Mark the 0 mA, 100 volts point on the horizontal axis in Fig. 2-11.
2. When there is 0 volts across the transistor, the supply voltage is across the load resistor. In this example, the collector current under these conditions is 100 volts/1000 ohms = 100 mA. Mark the 0 volts, 100 mA point on the vertical axis in Fig. 2-11.
3. Connect the two points marked in steps 1 and 2. This is the load line for the collector circuit.
4. Determine the quiescent base current. This is the condition when no ac voltage is superimposed on the dc supply voltage. It is 20 volts/20,000 ohms = 1 mA. Mark the point, Q, where the 1 mA base current curve crosses the load line.
5. The quiescent collector voltage and collector current can be determined by extending vertical and horizontal lines from the Q point. This procedure has been described previously. The quiescent collector voltage is 50 volts and collector current is 50 mA.

Should the base current swing to 2 mA, the collector current rises to 100 mA and the collector voltage drops to zero. This is the condition when the +20 volts of the square wave is superimposed on the 20-volt supply. Any further increase in base current does not change the collector voltage or current.

Should the base current swing to 0 mA, the collector voltage (or voltage from emitter to collector) rises to the supply voltage of 100 volts and the collector current drops to zero. This is the condition when the superimposed square wave drops 20 volts or more.

It is instructive to follow the transistor current and voltage excursions as the input signal varies. The voltage and current variations are tied to the load line. Any "collector voltage-collector current-base current" condition must be a point on the load line. All input signal variations are considered as points traveling up and down the load line.

Chapter 3

BIASING THE TRANSISTOR

The information in Chapter 2 can be used to design many transistor circuits. With a little ingenuity and a lot of good luck, the circuits will even perform well.

Two factors should be considered at this time. The first is that a transistor is a complex device. It is temperature-sensitive, and it has many voltage, current, and power limitations. The frequency range in which a particular device can perform effectively is severely limited.

The second factor is the economic impracticality of designing haphazardly and using only basic circuit configurations as drawn in Chapter 2. Two separate power supplies are costly. Poor designs may use more components and semiconductor devices than are absolutely necessary. Minimizing the number of components used in a design reduces the chance of component failure. There are also fewer sources of distortion and less of a tendency toward instability.

Details concerning the technology of transistors and other semiconductors are developed throughout the remainder of this book. Practical applications, analysis and design procedures are presented to indicate methods of applying the derived information.

This chapter details six methods used to bias the transistor. Bias is used to set the specific quiescent operating point, Q, for the transistor. As before, the base-emitter junction is forward biased and the base-collector junction is reverse biased. The base current is adjusted to yield a specific collector current.

The circuits have frequently been assigned names, each attempting to best describe the particular arrangement. In this book, the circuits will be referred to by number to avoid confusion.

A change from earlier cumbersome schematic notations will start with this chapter. Previously, a battery had been drawn to indicate the supply voltage. Beginning with Fig. 3-1, the supply voltage will be shown by the

notation V_{CC}, V_{BB}, or simply by the size of the voltage and the polarity. In this type of notation, the end of the supply not shown is assumed at ground unless there is information to the contrary.

BIAS CIRCUITS

Bias Circuit I

The first arrangement to be discussed is depicted in Fig. 3-1A. The voltage across the base-emitter junction is V_{BE}. The leakage current through the base-collector junction is I_{CBO}.

The voltage supplying power to the collector circuit is also used as the source for base current. The only component connecting the supply voltage, V_{CC}, to the base is resistor R_B.

The base circuit of Fig. 3-1A has been redrawn in Fig. 3-1B. The total resistance in the circuit is R_B, the dc base resistance r_B, and the dc emitter resistance r_E .When viewed from the base circuit, the last resistance must be multiplied by β. Stated mathematically, the resistance in the base circuit is $R_B + r_B + \beta r_E$. The total voltage across this combination of resistors is V_{CC} minus the voltage drop from the base to the emitter, or $V_{CC} - V_{EB}$.

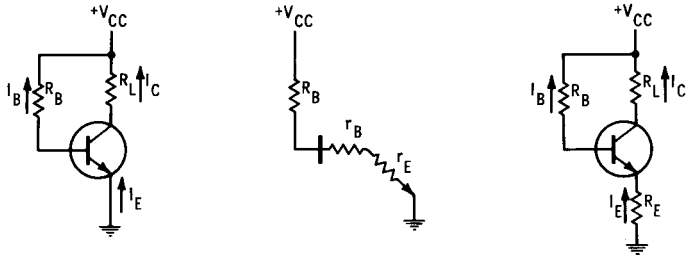
Assuming that V_{BE}, r_B, and βr_E are all negligible, the base current, I_B, from Ohm's law, is V_{CC}/R_B. Some or all of the negligible factors may be added to the equation if more accuracy is required.

Fig. 3-1A differs from Fig. 3-1C in that an emitter resistor is added to the latter. In this case, the emitter resistor must be multiplied by β when reflected into the base circuit. Now, the base current becomes:

$$I_B = \frac{V_{CC}}{R_B + \beta R_E}$$

The total quiescent collector current, from Equation 2-5 is:

$$I_C(\text{total}) = \beta I_B + \beta I_{CBO}$$



(A) Common-emitter circuit. (B) Fig. 3-1A with r_B and r_E shown. (C) Common-emitter circuit with emitter resistor added.

Fig. 3-1. Bias circuit I.

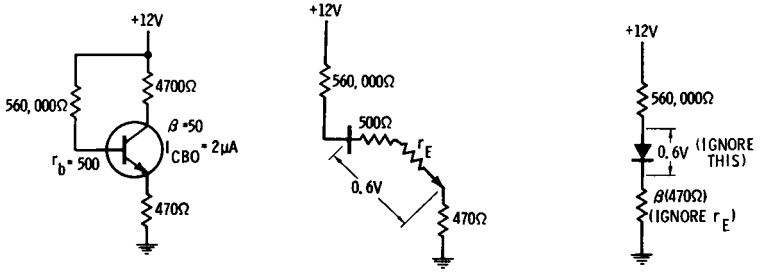
Using the component values shown in Fig. 3-2A, determine the collector current, the voltage across the 4700-ohm load resistor, and the voltage across the transistor. It is a silicon device.

The base-emitter junction circuit is shown in Fig. 3-2B. The total resistance in the circuit is:

$$R_{Base}(\text{total}) = 560{,}000 + 500 + \beta r_E + \beta 470$$

Since βr_E is usually negligible,

$$R_{Base}(\text{total}) = 584{,}000 \text{ ohms.}$$



(A) Common-emitter circuit with values shown.

(B) Base circuit for Fig. 3-2A.

(C) Equivalent circuit from +12V through base to emitter to ground.

Fig. 3-2. Problem using bias circuit I.

Assuming that there is a 0.6-volt drop across the base-emitter junction, the total voltage affecting the base current is $12 - 0.6 = 11.4$ volts. The base current, from Ohm's law, is:

$$I_B = \frac{11.4 \times 1000}{584{,}000} \text{ mA.}$$

Once again, the equation is multiplied by 1000 so that I_B will be expressed in milliamps.

Simplifying the expression, the base current becomes:

$$I_B = 1.95 \times 10^{-2} \text{ mA}$$

The error incurred by ignoring r_B and r_E is negligible.

The total collector current (remembering that $2\ \mu A = 2 \times 10^{-3}$ mA) is:

$$I_C(\text{total}) = \beta I_B + \beta I_{CBO} = 50(1.95 \times 10^{-2}) + 50(2 \times 10^{-3})$$
$$= 0.975 + 0.1 = 1.075 \text{ mA}$$

The voltage across the 4700-ohm load resistor is $4700 \times 1.075 \times 10^{-3} A = 5.05$ volts. The current through the 470-ohm emitter resistor is

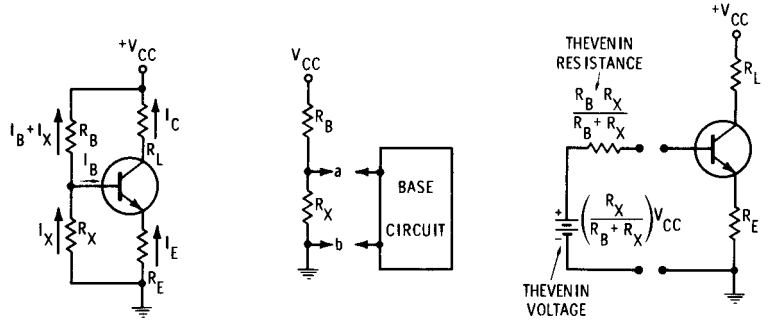
equal to the sum of the total collector and base currents (see Equation 2-6) or $I_C(\text{total}) + I_B + I_{CBO} = (1.075 + 1.95 \times 10^{-2} + 2 \times 10^{-3})$ mA = 1.097×10^{-3} amps. The voltage across the 470-ohm emitter resistor is about 470 ohms $(1.097 \times 10^{-3}\text{A}) = 0.515$ volt. The voltage across the transistor V_{CE}, is $12 - 5.05 - 0.515 = 6.44$ volts. The power dissipated by the transistor is $V_{CE} \times I_C(\text{total}) = 6.44 \times 1.075 \times 10^{-3} = 7.52 \times 10^{-3}$ watts or 7.52 milliwatts (mW).

It is interesting to repeat that problem ignoring the base-emitter voltage drop and the base and emitter resistances.

The base circuit is shown in Fig. 3-2C. The base current is $12/(560{,}000 + 50 \times 470) = 12/(560{,}000 + 23{,}500) = 2.065 \times 10^{-2}$ mA. This differs from the more accurate calculation by a factor of $2.065 \times 10^{-2} - 1.95 \times 10^{-2} = 0.015 \times 10^{-2}$ mA, or $(0.015 \times 100)/1.95 = 0.77\%$. This is a negligible error in most cases. In many of the ensuing examples, r_B, r_E and V_{BE} will be ignored.

Bias Circuit II

To complicate the matter and help maintain temperature stability, a resistor, R_X, is added to the circuit. This is shown in Fig. 3-3A.



(A) Circuit using temperature-stabilizing resistor, rx. (B) Base circuit of Fig. 3-3A. (C) Thevenin equivalent circuit of network connected to input.

Fig. 3-3. Bias circuit II.

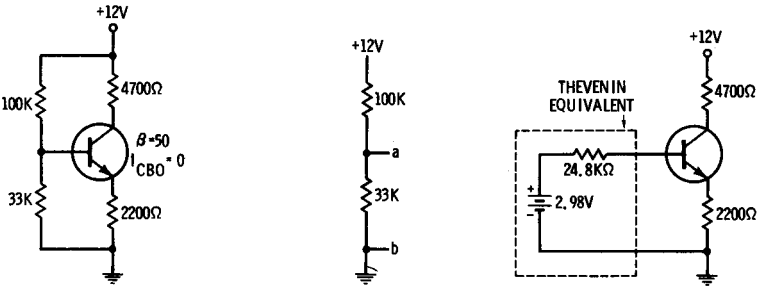
The current through R_B is divided between the base and R_X. The Thevenin equivalent (see the section on zener filters in Chapter 1) of the network feeding the base circuit is used to determine the base current. The network in the base circuit is shown in Fig. 3-3B. The components of the Thevenin equivalent of the network are determined as follows:

With the base-emitter diode removed, the voltage across R_X is $[R_X/(R_B + R_X)]\ V_{CC}$. This is the Thevenin equivalent voltage. Short the supply voltage. V_{CC} is at ground. R_B is across R_X. The two resistors in parallel, or $R_BR_X/(R_B + R_X)$, is the Thevenin equivalent resistance. The

complete Thevenin equivalent circuit of the network, connected to the input of the transistor, is drawn in Fig. 3-3C.

The base current can be determined as before. It is the Thevenin voltage minus the base-emitter voltage (if it is of significant magnitude), divided by the sum of the Thevenin equivalent resistance, $R_B R_X/(R_B + R_X)$ and βR_E. (Ignore r_B and r_E in this particular example.) The collector current can be determined as in the previous example.

In the circuit in Fig. 3-4A, it is required to determine the collector current, the collector-emitter voltage, and the power dissipated by the transistor, using the components shown. Assume that there is a germanium device in which the base-emitter voltage is negligibly small—less than 0.2 volt.



(A) Circuit of Fig. 3-3A with component values shown. (B) Circuit of Fig. 3-3B with component values shown. (C) Equivalent circuit of Fig. 3-3C with values indicated.

Fig. 3-4. Numerical example using bias circuit II.

First, calculate the circuit at the base of the transistor in accordance with Thevenin's theorem. Separate the input resistor network from the base circuit to obtain the arrangement shown in Fig. 3-4B. Using the voltage divider equations, the Thevenin equivalent voltage across terminals a-b is:

$$V_{TH} = \left(\frac{33 \times 10^3}{100 \times 10^3 + 33 \times 10^3}\right) 12 = 2.98 \text{ volts}$$

Short the 12-volt supply to ground. The Thevenin equivalent resistance, R_{TH}, determined by looking into the output terminals, is the two resistors in parallel, or:

$$R_{TH} = \frac{(33 \times 10^3)\ (100 \times 10^3)}{33 \times 10^3 + 100 \times 10^3} = \frac{3300 \times 10^6}{133 \times 10^3} = 24.8 \times 10^3\ \Omega$$

The network, replaced with its Thevenin equivalent, is shown in Fig. 3-4C, connected to the base circuit.

The current through the base circuit is determined by the 2.98 Thevenin equivalent voltage and the resistive sum of the 24.8 kΩ Thevenin equivalent resistance and β multiplied by the resistor in the emitter. This resist-

ance is $50 \times 2200 = 110\,k\Omega$. The sum of the two resistors is $24.8\,k\Omega + 110\,k\Omega = 134.8\,k\Omega$. The base current, I_B, is $2.98V/134.8\,k\Omega = 2.2 \times 10^{-2}$ mA.

The collector current, I_C, is $\beta I_B = 50 \times 2.2 \times 10^{-2} = 1.1$ mA.

The voltage across the 4700-ohm resistor is $(1.1 \times 10^{-3}A) \times (4700\,\Omega) = 5.18$ volts. The voltage across the $2200\,\Omega$ resistor is infinitesimally more than $(1.1 \times 10^{-3}A)\,(2200\,\Omega) = 2.42$ volts.

The total supply is 12 volts. The voltage across the transistor is the difference between the supply voltage and the voltage across the collector and emitter resistors or $12 - 5.18 - 2.42 = 4.4$ volts.

The power dissipated by the transistor is the product of the voltage across the transistor and the collector current, or (4.4 volts) $(1.1 \times 10^{-3}$ amps$) = 4.85 \times 10^{-3}$ watts or 4.85 mW.

Bias Circuit III

Some specialized circuits require a positive and negative voltage, each with respect to ground, to control the base current. In this case, the bias circuit in Fig. 3-5A can be used.

To calculate the base current, first separate the components in the base-emitter circuit from the transistor. Now, use the Thevenin theorem to obtain the equivalent circuit for the bias network. This is redrawn in Fig. 3-5B.

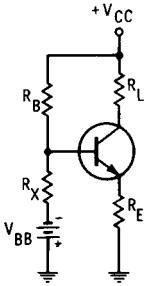
The superposition theorem should be used along with the Thevenized network. The theorem states that if there is more than one voltage or current source acting on a circuit, consider the effects on the circuit of one source at a time and then add the cumulative effects of all the individual sources.

In order to accomplish this, all but one source must be disabled for each calculation. A short circuit across a voltage source disables it. As for the current source, at least one of the leads must be opened to deaden it.

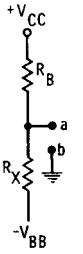
Returning to Fig. 3-5B, the bias network is separated from the base circuit of the transistor. As is obvious from Fig. 3-5A, the transistor circuit was originally connected to the network between the junction of the two resistors and ground. It has been separated at this point to facilitate the calculations. The Thevenin equivalent of the resistive circuit should be determined between points "a" and "b."

Disable the $-V_{BB}$ supply by shorting it to ground. The circuit is now as shown in Fig. 3-5C. The voltage between "a" and ground "b" using voltage divider equations is $+V_{CC}[R_X/(R_B + R_X)]$.

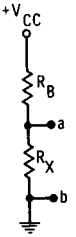
Remove the short across $-V_{BB}$ and short the V_{CC} supply to ground. This is the circuit in Fig. 3-5D. The voltage between "a" and ground "b" due to $-V_{BB}$ using the voltage divider equation is $-[R_B/(R_B + R_X)]\,V_{BB}$. Now, remove the short across $+V_{CC}$. Using the superposition theorem, the Thevenin equivalent voltage is found to be the sum of the two voltages just determined, or:



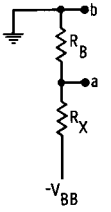
(A) Common-emitter circuit with bias battery V_{BB}.



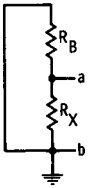
(B) Fig. 3-5A showing input circuit separated from transistor.



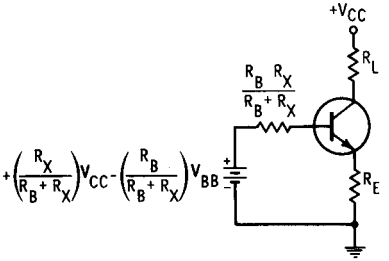
(C) Fig. 3-5B with V_{BB} disabled.



(D) Fig. 3-5B with V_{CC} shorted and V_{BB} enabled.



(E) Thevenin equivalent resistance (all voltage sources shorted).



(F) Complete circuit including Thevenin equivalent circuit.

Fig. 3-5. Bias circuit III.

$$V_{TH} = +\frac{R_X}{R_B + R_X} V_{CC} - \frac{R_B}{R_B + R_X} V_{BB} \qquad (3\text{-}1)$$

The Thevenin equivalent resistance between "a" and "b" can be found shorting all voltage sources, as in Fig. 3-5E. The equivalent resistance between "a" and "b" is the calculated value of R_B in parallel with R_X.

$$R_{TH} = \frac{R_B R_X}{R_B + R_X} \qquad (3\text{-}2)$$

The complete circuit, including the Thevenin equivalent, is shown in Fig. 3-5F. The analysis of this is identical to that of bias circuit II.

The numerical example in Fig. 3-6A involves two power supplies—+12 volts and −7 volts. The base-emitter voltage is negligible, as are the base and emitter resistances.

Calculate the bias circuit according to the Thevenin theorem. The voltage at the base with respect to ground, due to the +12-volt supply is $+[150\,k\Omega/(150\,k\Omega + 100\,k\Omega)]12 = 7.2$ volts when the −7 volt supply is shorted to ground. The voltage at the base with respect to ground, due to the −7 volt supply is $-[100\,k\Omega/(150\,k\Omega + 100\,k\Omega)]\ 7 = 2.8$ volts when the +12 volt supply is shorted to ground. The Thevenin equivalent voltage is the sum of these two voltages or $+7.2 - 2.8 = 4.4$ volts.

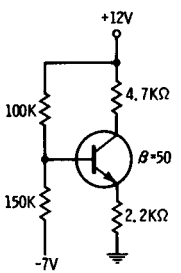
The Thevenin equivalent resistance can be found by shorting both power supplies to their ground terminals. R_{TH} is the parallel combination of the two resistors in the bias circuit or $(100\,k\Omega)\ (150\,k\Omega)/(100\,k\Omega + 150\,k\Omega) = 60\,k\Omega$. The resulting equivalent circuit is shown in Fig. 3-6B. The procedure in solving for the various currents through this transistor is identical to that used in the previous problem.

Bias Circuit IV

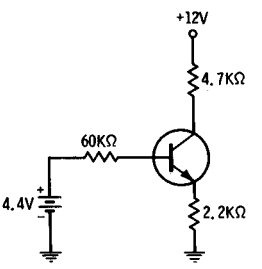
In another common circuit, the emitter resistor is returned to a fixed voltage rather than to ground. An arrangement of this type is shown in Fig. 3-7A.

The base-emitter circuit has been redrawn in Fig. 3-7B. The supply is shown as a battery. The emitter current passes through the supply and R_E. The emitter current has no effect on the voltage source,$-V_{EE}$, because as an ideal voltage source, it has zero internal impedance. I_E can develop a voltage, $I_E R_E$, only across R_E. Only R_E must be multiplied by β when reflected into the base circuit. The voltage generating the base current remains unaltered by multiplication factors whether the supply is in the emitter or base circuit.

The total base circuit resistance, ignoring r_B and r_E, is $R_B + \beta R_E$. The supply voltage is V_{EE}, and the base current is approximately $V_{EE}/(R_B +$

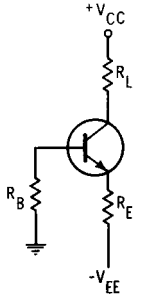


(A) Fig. 3-5A with values indicated.

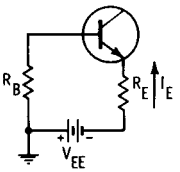


(B) Fig. 3-5F with values indicated.

Fig. 3-6. Numerical example using bias circuit III.



(A) Circuit with emitter returned to a fixed voltage.



(B) Base-emitter circuit of Fig. 3-7A redrawn.

Fig. 3-7. Bias circuit IV.

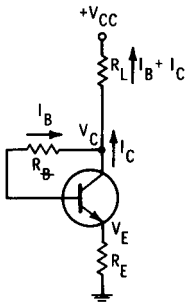
βR_E). As usual, the collector and emitter current is approximately equal to beta multiplied by the base current. The voltages across R_L and R_E are the collector or emitter current multiplied by the respective resistor.

The voltage at the collector with respect to ground is $+V_{CC} - I_C R_L$. The voltage at the emitter with respect to ground is $-V_{EE} + I_E R_E$. The voltage across the transistor is the difference of these two voltages, or $V_{CC} - I_C R_L + V_{EE} - I_E R_E$. It is the sum of the two supply voltages minus the voltage drops across R_L and R_E.

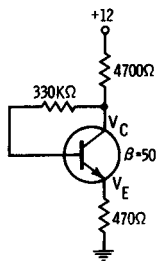
Bias Circuit V

The bias circuit in Fig. 3-8 is unique in that the collector voltage, rather than the power supply voltage, is used to determine the base current. R_B completes a feedback circuit to be discussed in a later chapter.

The voltage across the load resistor, R_L, is R_L multiplied by the total current through this resistor. In a perfect transistor, the total current through R_L would be the sum of the base and collector currents, $I_B + I_C$.



(A) Circuit where collector voltage is used to determine base current.



(B) Fig. 3-8A with numerical values indicated.

Fig. 3-8. Bias circuit V.

Since I_B is much less than I_C, the voltage across R_L is about $I_C R_L$, or the supply voltage minus the voltage drop across the load resistor.

The base current is determined from the collector voltage, R_B and βR_E. It is $I_B = V_C/(R_B + \beta R_E)$. The collector current is the base current multiplied by β.

Using the numbers in Fig. 3-8B, the voltage at the collector is $V_C = 12 - (4700)I_C$. The voltage at the emitter is $V_E = (470)I_E \approx (470)I_C$. The voltage across the transistor, V_{CE}, is $12 - (4700)I_C - (470)I_C = 12 - (5170)I_C$.

If the voltage across the base-emitter junction is considered negligible compared to that across the transistor, V_{CE} appears across the 330 kΩ resistor. Since all the base current is through this resistor, the base current is $I_B = [12 - (5170)I_C]/330\ k\Omega = 3.64 \times 10^{-5} - 1.57 \times 10^{-2} I_C$. Because $I_C = \beta I_B$, $I_B = 3.64 \times 10^{-5} - (1.57 \times 10^{-2})\ (50 I_B)$. Solving for I_B, it is equal to 2.04×10^{-5} amps. The collector current is $\beta \times 2.04 \times 10^{-5} = 1.02$ mA.

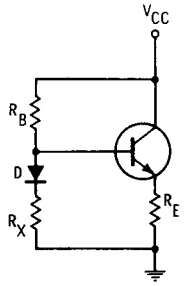


Fig. 3-9. Bias circuit VI using a diode for temperature stabilization.

Bias Circuit VI

Many of the circuits discussed above are designed with the primary goal of maintaining a constant bias despite variation of the ambient temperature around the transistor. In Fig. 3-9, a diode is used for temperature stabilization. This is essentially bias circuit II with an additional forward-biased diode in the base circuit.

In Chapter I, it was pointed out that the voltage across a diode changes −2.5 mV for every degree Celsius rise. Every forward-biased diode has this or a similar characteristic. The voltage across the forward-biased base-emitter junction varies by the same −2.5 mV per degree Celsius.

In Fig. 3-9, the voltage across the forward-biased diode is equal to the voltage between the base and emitter, if both devices are maintained at the same temperature, and they are both constructed in a similar fashion of the same material. Because R_E and the base-emitter junction are in parallel with R_X and the diode, the voltages across the parallel connected components are identical. Since the voltages across the diodes are equal, the voltages across R_X and R_E are equal

The analysis of this circuit is identical to that of bias circuit II. Ignore the diode and base-emitter voltages and proceed with the mathematical methods previously employed.

DESIGN

Various bias methods are used for different significant reasons. Stability of one sort or another is a prime consideration in choosing the bias circuit. The designation of a particular circuit and the selection of components to be used in the circuit are the concerns of the designer. Previously, the various bias methods were analyzed. Here, the discussion will center upon the design procedures.

Although long, complex formulas (which are often useless to the designer) can be developed, this method will not be pursued here. Only procedures providing practical results, however approximate, will be described.

Actual examples illustrating usable methods will be detailed in the various steps of the design. In each example, the collector supply is assumed at 20 volts. A silicon transistor with a $\beta = 100$ and an $I_{CBO} = 0$ will be used. It will be required to design a circuit with a minimum ac voltage gain of 10 so that the ratio of the collector to the emitter resistor will be at least 10 : 1. The transistor should idle at about 5 mA with a V_{CE} of approximately 10 volts (quiescent condition). The base current is $I_C/\beta = 5 \times 10^{-3}\text{A}/100 = 5 \times 10^{-5}$ amps.

Using these numbers, it is now possible to proceed with the design of the bias circuits. All results will be approximate yet adequate in most instances. They can be checked and trimmed further in the laboratory.

In Fig. 3-1A, the gain will be more than 10 because the resistor in the emitter is zero. With a 20-volt supply and 10 volts from collector to emitter, the voltage across R_L must be 10 volts. Because the collector current is 5 mA, $R_L = V_{R_L}/I_C = 10 \text{ volts}/5 \times 10^{-3} \text{ amps} = 2000$ ohms. The closest standard 10% resistor is 2200 ohms.

The current through R_B is 5×10^{-2} mA. The voltage across R_B is 20 volts $-$ 0.6 volts $=$ 19.4 volts. (The 0.6 volt is the base-emitter voltage of a forward-biased silicon transistor). From Ohm's law, $R_B = 19.4 \text{ volts}/5 \times 10^{-5} \text{ amps} = 390{,}000$ ohms.

For the circuit in Fig. 3-1C (as well as the other bias arrangements), if there is to be 10 volts across the transistor, the voltage across $R_L + R_E$ must be equal to 20 volts $-$ 10 volts $=$ 10 volts. Assuming that the collector and emitter currents are identical (5×10^{-3} amps), $R_L + R_E = 10 \text{ volts}/5 \times 10^{-3} \text{ amps} = 2000$ ohms. For a gain of 10, the ratio of R_L/R_E must be equal to 10/1 or more. Assuming that $R_L/R_E = 10/1$; $R_L = 10R_E$. There are now two equations with two unknowns:

$$R_L + R_E = 2000$$
$$R_L = 10R_E$$

Substituting the latter equation into the former:

$$10R_E + R_E = 2000;\ 11R_E = 2000;\ R_E = 182 \text{ ohms.}$$

And since $R_L = 10R_E$, $R_L = 10(182) = 1820$ ohms.

The standard 10% resistors with the closest values are 180 ohms and 1800 ohms. The ratio is 10 to 1, indicating that the gain will be 10 when the resistors R_L and R_E are exactly 180 ohms and 1800 ohms, respectively. To assure that the gain will be at least 10, the 1800-ohm resistor can be made larger. Choose the next larger standard value of 2200 ohms. Under the worst conditions, when the 180-ohm emitter resistor is 10% high and the 2200-ohm collector resistor is 10% low, the gain will be:

$$\text{Gain} = \frac{2200 - 10\%\ (2200)}{180 + 10\%\ (180)} = \frac{2200 - 220}{180 + 18} = \frac{1980}{198} = 10.0$$

We will also be within the specification for a gain of at least 10 if $R_L = 1800$ ohms and $R_E = 150$ ohms. Either combination of resistors may be used in the circuit to get the proper minimum gain. In this example, it will be assumed that $R_L = 2200$ ohms and $R_E = 180$ ohms. The voltage from emitter to ground, or across the 180-ohm emitter resistor is about $I_C R_E = (5 \times 10^{-3})\ 180 = 0.9$ volt. Using $R_L = 2200$ ohms and $R_E = 180$ ohms, the base circuit will now be designated for the various bias arrangements.

In Fig. 3-3, R_X is usually less than 10 times R_E. This relationship is derived from stability considerations to be discussed in the next chapter. Assume that R_X equals 1800 ohms. Since the voltage across R_X is the same as that across the 180-ohm emitter resistor plus V_{BE}, or 0.9 volt + 0.6 volt, the current through the 1800-ohm resistor is 1.5 volt/1800 ohms = 8.3×10^{-4} amps.

The base current is 5×10^{-5} amps. The sum of the base current and the current through R_X equals the current through R_B. This is $8.3 \times 10^{-4} + 5 \times 10^{-5} = 8.8 \times 10^{-4}$ amps. The voltage across R_B is $20 - 1.5 = 18.5$ volts. R_B is thus made equal to 18.5 volts/8.8×10^{-4} amps = 21,000 ohms. The closest standard 10% resistor to be used in this circuit is 22,000 ohms.

The design of the bias circuit in Fig. 3-5A requires only a slight variation from that just discussed. The voltage across R_X is the sum of V_{BB}, the voltage across R_E and V_{BE}. In this case, it is $V_{BB} + 0.9 + V_{BE}$. If $V_{BB} = 6$ volts, V_{R_x} is $6 + 0.9 + 0.6 = 7.5$ volts.

Assuming that R_X is 1800 ohms, (determined as in the previous problem), the current through this resistor is 7.5 volts/1800 ohms = 4.17×10^{-3} amps. R_B is determined as before.

The circuit in Fig. 3-7 requires a somewhat different approach. Assume that V_{EE} is -10 volts. In order to maintain approximately 10 volts across R_L, it must remain at 2200 ohms. To maintain the emitter at about 0.9 volt with respect to ground, the voltage across R_E is $V_{EE} + 0.9$ volt = 10.9 volts. Because I_C is approximately equal to I_E, the emitter resistor should

be 10.9 volts/5×10^{-3} amps = 2180 ohms. Use the nearest standard 10% resistor. In this example, it is 2200 ohms. The voltage across this resistor is about (2200 ohms) (5×10^{-3} amps) = 11 volts. Since $V_{EE} = 10$ volts, the emitter is at 11 − 10 or +1 volt with respect to ground, or close to 0.9 volt.

All the base current, 5×10^{-5} amps, is through R_B. The voltage across R_B is equal to the voltage from the base to ground. It is V_{BE} plus the voltage at the emitter or 0.6 + 1 = 1.6 volt. R_B = 1.6 volt/5×10^{-5} amps = 32,000 ohms. Use the standard 33,000-ohm, 10% resistor. Bypass the emitter resistor with a large capacitor to get the required ac gain. This technique will be discussed in a later chapter.

In Fig. 3-8A, the base and collector current pass through R_L. The base current is usually negligible compared to the collector current. If R_L = 2200 ohms and $I_C = 5 \times 10^{-3}$ amps, the voltage at the collector is 20 volts − (5×10^{-3} amps) (2200 ohms) = 9 volts.

The voltage at the emitter is (5×10^{-3} amps) (180 ohms) = 0.9 volt. The voltage at the base is 0.9 volt + V_{BE} = 1.5 volts.

The voltage across R_B is the difference between the collector and base voltage or 9 volts − 1.5 volts = 7.5 volts. The base current through R_B is 5×10^{-5} amp. The resistor, R_B, should be equal to 7.5 volts/5×10^{-5} amps = 150,000 ohms.

The circuit in Fig. 3-9 is unique in two ways. R_E is the output load in an emitter-follower circuit. If 10 volts is to appear across this resistor when there is 5×10^{-3} amps through the circuit, the resistor must be equal to 10 volts/5×10^{-3} amps = 2000 ohms. Using the nearest standard value, the resistor is physically 2200 ohms. The emitter will be at (2200 ohms) (5×10^{-3} amps) = 11 volts with respect to ground.

The base-emitter voltage drop cannot be ignored. The voltage at the base is equal to 11 volts + V_{BE}. This same voltage is across the series combination of the diode and R_X. The voltage across the diode just cancels V_{BE}, if they are at the same temperature. Thus, the 11 remaining volts that are across R_E must also be across R_X.

R_X should be less than ten times the size of R_E, as will be determined in the next chapter. Assume it is 22,000 ohms. The current through R_X is then 11 volts/22,000 ohms = 5×10^{-4} amps.

The current through R_B is 5×10^{-4} amps + 5×10^{-5} amps (the base current) = 5.5×10^{-4} amps. The voltage across R_B is 20 − 11 − V_{BE}. Hence, R_B must be $(20 - 11 - V_{BE})/(5.5 \times 10^{-4})$. If V_{BE} is about 0.6 volt for the silicon transistor and diode, R_B = 15,300 ohms. Use a 15,000-ohm, 10% standard resistor.

Note that the ac voltage gain of the circuit is about "1." It is not a common-emitter circuit, but of the common-collector variety. All circuits of this type have a gain of somewhat less than "1." The bias method that has been discussed here can be used for high-gain common-emitter circuits as well.

A CORRECTION FACTOR

One transistor resistance has been ignored throughout the discussion. It is shown in Fig. 3-10.

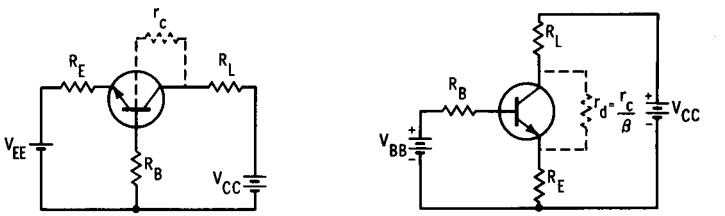
There is a resistance across the elements in the output circuit of the transistor. In Fig. 3-10A, the collector resistance, r_c, is between the collector and base, while in Fig. 3-10B, the resistance r_d is between collector and emitter. Usually, r_d ranges from 10,000 to 100,000 ohms and r_c is beta times as large. The sizes of these resistances can be determined from the characteristic curves of the transistor. Because it is difficult to determine r_c, the method for determining r_d will be illustrated in Fig. 3-11; r_c can be determined from r_d by simply multiplying it by β.

First, determine the approximate quiescent base current. Also approximate the quiescent collector current and collector-emitter voltage from the considerations discussed above.

Now, mark two points on the straight portion of the I_{BQ} curve, approximately equidistant from Q. Draw horizontal and vertical lines to the axis and note the currents and voltages.

$$r_d = \frac{V_{CE2} - V_{CE1}}{I_{C2} - I_{C1}} \qquad (3\text{-}3)^*$$

To determine β, first extend the vertical line from V_Q to I_{B2}. Mark points (1) and (2) where this line intersects I_{B1} and I_{B2}, respectively. Draw horizontal lines to the I_C axis. Mark points I_{C3} and I_{C4} on the axis.



(A) Circuit showing collector-to-base resistance R_c.

(B) Circuit showing collector-to-emitter resistance r_d.

Fig. 3-10. Collector resistance considerations.

$$\beta = \frac{I_{C4} - I_{C3}}{I_{B2} - I_{B1}} \qquad (3\text{-}4)^*$$

and

$$r_c = \beta r_d \qquad (3\text{-}5)^*$$

From a similar construction, r_c can be determined on a curve plotting I_C against V_{CB} for the different values of emitter current. However, the curves are essentially horizontal and do not provide even reasonably accurate information.

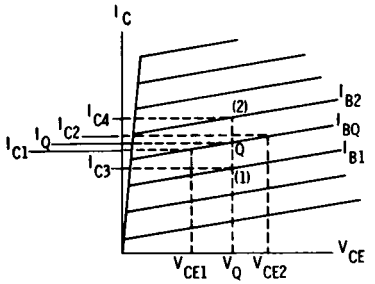


Fig. 3-11. Theoretical transistor curves.

For circuits similar to those in Fig. 3-10B, the collector current has been shown equal to $\beta I_B + I_{CEO}$. There is an additional collector current due to r_d. This current is V_{CE}/r_d. If r_d is not much larger than R_L, r_d cannot be ignored. In this case, the current due to r_d must be added to βI_B and I_{CEO} to determine the total collector current, I_C. The collector-to-emitter voltage can easily be derived from:

$$V_{CE} = V_{CC} - I_C(R_L + R_E) \tag{3-6}$$

where,

I_C is the total collector current.

The collector current due to r_d is:

$$I_C = V_{CE}/r_d = (V_{CC} - I_C R_L - I_C R_E)/r_d \tag{3-7}$$

In Fig. 3-12, numbers have been substituted for the symbols that were used in Fig. 3-10B. Here, the base current is $I_B = 10$ volts/$(47{,}000 + \beta 22)$ $= 2.09 \times 10^{-4}$ amps. The collector current component due to this is $(2.09$

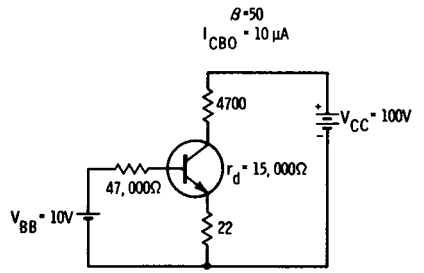


Fig. 3-12. Circuit taking r_d into account.

$\times 10^{-4})\beta = 10.4 \times 10^{-3}$ amps. The collector current due to I_{CBO} is $(10 \times 10^{-6})\beta = 0.5 \times 10^{-3}$ amps. The collector current due to βI_B and I_{CBO} is $(10.4 \times 10^{-3}) + (0.5 \times 10^{-3}) = 10.9 \times 10^{-3}$ amperes. Using Equation 3-7, add the effect of r_d, which is equal to 15,000 ohms. The total collector current is:

$$I_C = 10.9 \times 10^{-3} + \frac{V_{CE}}{r_d} = 10.9 \times 10^{-3} + \frac{V_{CC} - I_C (R_L + R_E)}{r_d}$$

$$= 10.9 \times 10^{-3} + \frac{100 - 4.722 \times 10^3 I_C}{15 \times 10^3}$$

Simplifying and solving, $I_C = 13.4 \times 10^{-3}$ amps.

The impedance of the transistor is r_d and r_c in the grounded emitter and grounded base configurations, respectively, at the collector circuits. If the impedance in the base circuit is low, the output resistance approaches r_c, as is the case in the common-base circuit. If the impedance in the base circuit is high, the output impedance approaches r_d, the impedance of the common-emitter circuit.

The effects of r_d are more far-reaching than just to set the bias conditions. Consider the transistor as a source of current, βI_B. A change in I_B is denoted by the symbol ΔI_B, and a change in I_C is ΔI_C. The change in current at the collector, ΔI_C, due to a change in current at the base. ΔI_B, is divided between R_L and r_d. Using standard current divider equations, the change in current through R_L is:

$$\Delta I_{R_L} = \left(\frac{\beta r_d}{r_d + R_L}\right) \Delta I_B \tag{3-8}$$

An effective value of β, when determining ac gain is $\beta r_d/(r_d + R_L)$. Let us call this β_{eff}.

The input impedance due to R_E is more accurately, though not precisely, determined from $(\beta_{eff})R_E$. The ac current gain is β_{eff} and the voltage gain is β_{eff} (R_L/R_{BR}), where R_{BR} is all the impedance reflected into the base circuit. In all cases where r_d is negligible compared to R_L, the gain and impedance revert to the originally stated, simpler forms. Usually, r_c is so large as to be negligible, and will therefore not be discussed further.

Chapter 4

STABILIZING THE BIAS POINT

It does no good to perform sophisticated calculations to set an optimum quiescent collector current if it will shift radically with temperature changes. Methods must be devised to maintain I_C at or near its calculated value despite temperature and other variations. I_{CBO}, V_{BE}, α, β, all vary with temperature and are the four major contributors to the drift of the quiescent collector current. The effect of the shift of idling current can best be illustrated through the use of Fig. 4-1.

The quiescent base current due to the bias circuit when the transistor is operated at 25°C is $(V_{CC} - V_{BE})/R_B$ equals $(6V - 0.6V)/4.7 \times 10^5$ ohms equals 1.15×10^{-5} amps. The collector current due to I_{CBO} is I_{CEO}, (the collector to emitter current with the base circuit open), which is $\beta I_{CBO} = 10^{-6}$ amps. The total collector current is 1.15×10^{-3} amps plus 10^{-6} amps $\approx 1.15 \times 10^{-3}$ amps. The voltage across the 3300 ohm load resistor is $(1.15 \times 10^{-3})\ (3.3 \times 10^3) = 3.85$ volts. The voltage across the transistor is $6 - 3.85 = 2.15$ volts.

Now assume that the transistor is at 85°C. From the graph in Fig. 4-2 (to be discussed later), I_{CBO} jumps to about 10^{-5} amps. Then $I_{CEO} = \beta I_{CBO} = 100 \times 10^{-5} = 10^{-3}$ amps. The collector current due to I_B remains at 1.15×10^{-3} amps. The total collector current is the collector current due to the base current added to the collector current due to I_{CEO} or $1.15 \times 10^{-3} + 10^{-3} = 2.15 \times 10^{-3}$ amps. The voltage across the 3300-ohm resistor is $(2.15 \times 10^{-3})\,(3.3 \times 10^3) = 7.1$ volts. The voltage across the transistor is equal to the supply voltage less the voltage across the transistor, or $6 - 7.1$ volts, or -1.1 volts. Since the voltage cannot be less than zero, the transistor is in saturation. In this type of operation, the collector current is independent of the base current. The collector-base junction is forward biased internally although a voltmeter measurement at the transistor leads shows that the opposite is true. Saturation will be discussed further in the chapter on power amplifiers and in the chapter on transistor switches.

The first calculation was made at the usual ambient temperature of 25°C. The second calculation was made with the temperature of the tran-

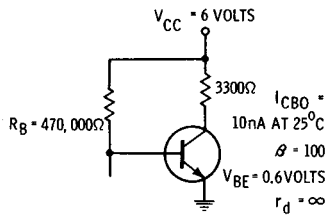


Fig. 4-1. Transistor (silicon) in saturation.

sistor raised to 85°C. The quiescent operating conditions at these two temperatures were quite different for the same circuit components. The changes due to temperature are further complicated by the variation of several parameters with the quiescent collector current. The parameters that vary with collector current are α, β, V_{BE}, V_{CE}, I_E, r_e, r_c, r_b, and I_{CBO}.

In addition to these factors, the bias conditions are affected by supply voltage changes and manufacturing tolerances. As to the latter, it should be recalled that β has been assigned a specific value for use in the calculations. But β is not a constant. Besides the variation of β with collector current, every transistor type is divided into several β groups. The β within a specific group may vary by more than a factor of 1:3. Equipment must be so designed that these variations are not significant. At additional cost, manufacturers will divide specific transistor types into closer tolerance β groups. The ratio, even in the latter case, seldom falls below 1:2.

EFFECT OF I_C ON THE PARAMETERS

The quantities α and β are interrelated. Both usually decrease at extremely low and extremely high values of collector current. At high currents, this phenomenon is known as "alpha crowding." Some manufacturers use curves to specify the variation of β with I_C. The specified parameters are relatively constant over the major portion of the operating range.

Given a specific resistive collector load, the emitter-to-collector voltage will, of course, vary with I_C. Assuming that there is no resistor in the emitter circuit, the emitter-to-collector voltage, V_{CE}, across a transistor is equal to the supply voltage minus the product of the collector current and the resistor in the collector circuit. The transistor is usually biased at about half the collector supply voltage, or $V_{CC}/2$. The collector voltage will then be capable of swinging from zero to V_{CC} and the collector current will simultaneously be capable of swinging from the maximum collector current (equal to twice the quiescent current) to zero.

The base-to-collector voltage, V_{CB}, and the emitter-to-collector voltage, V_{CE}, are interrelated and are almost equal. They differ only by the forward voltage drop from the base to the emitter, V_{BE}. As a general rule, α, β, I_{CBO}, r_b, r_c and r_d increase with V_{CB}, and r_c and r_d will decrease as the base-emitter diode enters the reverse-biased region, $-V_{BE}$. Normally, the

collector current affects V_{CE}, but the effect of V_{CE} on the collector current is negligible.

Since I_C, I_E, and I_B are closely interrelated, an increase in I_E usually signals a comparable increase in the other two factors. Since r_e is related to I_E, it will decrease as I_E rises.

EFFECT OF TEMPERATURE ON I_C

Both α and β vary with temperature. They usually increase with temperature up to a peak, at which time they may start to decrease.

V_{BE} decreases with temperature rise at the rate of -2.5 mV/°C. Since the base current is dependent on this voltage, I_B will also be affected by the temperature. In turn, I_C will change.

I_{CBO} approximately doubles for every 10°C rise in the temperature of germanium transistors, and for every 6°C rise in the temperature of silicon units. This approximation is shown graphically in Fig. 4-2. All calculations based on this graph lead to approximate answers. There are variations from transistor to transistor. In the curve, the solid line represents silicon transistor characteristics while the broken line curve is for germanium devices.

In using the curves, the temperature can be read on the horizontal axis of Fig. 4-2. A vertical line is drawn straight up to the curve for the silicon or germanium device, as required. A horizontal line is then drawn from the point of intersection to the vertical axis. The ratio of I_{CBO} at the temperature of interest to I_{CBO} at 25°C can be read on the vertical axis. If the relationship is determined from either curve marked "X(1)," there is no correction factor—the ratio is taken as shown at the left-hand vertical axis. If the ratio is to be determined from any of the other curves, multiply the ratio by the factor indicated next to the curve.

As an example, assume $I_{CBO} = 3$ nanoamps $= 3 \times 10^{-9}$ amps at 25°C. What is I_{CBO} at 125°C if a silicon transistor is involed?

First, draw a vertical line from the 125°C point on the horizontal axis to the solid line curve. Draw a horizontal line from the point of intersection to the vertical axis. The ratio of $I_{CBO}@T$ to $I_{CBO}@25°C$ is shown as about 100. However, the curve that was used is marked $X(10^3)$. The true ratio is $100 \times 10^3 = 100{,}000$. Equate this to $I_{CBO}@T/I_{CBO}@25°C$ and solve for I_{CBO}. It is:

$I_{CBO}@T = (100{,}000)I_{CBO}@25°C = (10^5)(3 \times 10^{-9}) = 3 \times 10^{-4}$ amps. I_{CEO} is beta at 125°C multiplied by the I_{CBO} just calculated.

BIAS AND STABILITY

An important factor affecting collector current when the temperature changes is I_{CBO}. A stability factor relating the change in collector current to the change in reverse leakage current due to all factors is:

$$S = \frac{\Delta I_C}{\Delta I_{CBO}} ; \Delta I_C = S(\Delta I_{CBO}) \qquad (4\text{-}1)^*$$

where,

Δ indicates a change in the quantity or a difference in size of a quantity under different conditions.

Verbally, Equation 4-1 states that I_C will change by an amount equal to S multiplied by the change in I_{CBO}. Another way of saying this is that for every change of I_{CBO}, there will be a change in I_C equal to a factor S multiplied by the change in I_{CBO}. S depends upon the particular circuit in which the transistor is being used.

Two other major factors that affect the collector current are the base current, I_B (as a function of the base-emitter voltage, V_{BE}), and the α

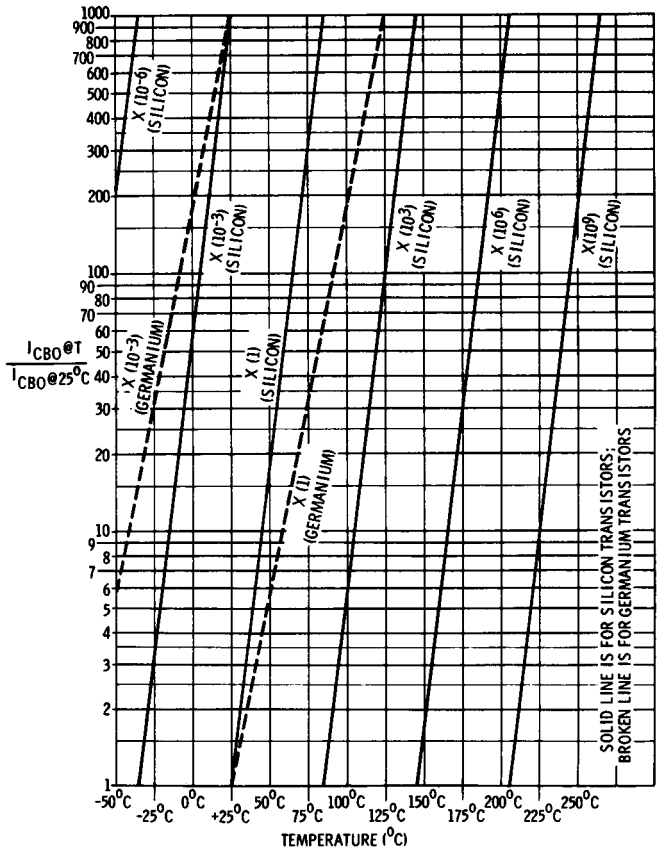


Fig. 4-2. Variation of I_{CBO} with changes in temperature.

or β of the transistor. Compared to I_{CBO}, the effects of these factors are minor.

I_B is a function of the base circuit supply voltage, V_{BB}. A stability factor, S_E, can be defined to relate the change in collector current to the change in V_{BB}:

$$S_E = \frac{\Delta I_C}{\Delta V_{BB}}\ ;\ \Delta I_C = S_E(\Delta V_{BB}) \qquad (4\text{-}2)^*$$

Since I_C also depends on α and β, a stability factor, S_β, can be defined to relate the change in collector current to the change in β (or α):

$$S_\beta = \frac{\Delta I_C}{\Delta \beta}\ ;\ \Delta I_C = S_\beta(\Delta \beta) \qquad (4\text{-}3)^*$$

The three stability factors should be derived for the various bias arrangements discussed in Chapter 3. Rather than show the derivations of the equations, the results of the mathematical operations will be stated here, complete with practical approximations. V_{BE} will be assumed negligible.

The procedure for deriving the stability factors involves the use of calculus. An equation is set up stating the collector current for a particular circuit. It is then differentiated with respect to I_{CBO} to determine S, differentiated with respect to V_{BB} to determine S_E, and differentiated with respect to β to determine S_β.

Qualitatively, we should note that all current entering the base appears to be multiplied by a factor of β in the collector. Stability is improved if I_{CBO} can be kept out of the base.

Stability Formulas for the Various Bias Arrangements

Two groups of equations are necessary to derive the relationship between the collector current, the circuit components, and the transistor parameters. The first group consists of two equations stating information about the device. These statements are true for any bias circuit. They are:

1. $I_E = I_B + I_C$.
2. $I_C = \beta(I_B) + (\beta + 1)I_{CBO}$.

The second group of equations describes the particular base circuit used in a specific method of biasing the transistor.

In Fig. 4-3 (a drawing of bias circuit II) the bias supply voltage, V_{BB}, (which may at times be made common with, or equal to V_{CC}) must be equal to $R_B(I_B + I_X)$, the voltage across R_B, plus $I_X R_X$, the voltage across R_X. Since V_{BE} is negligible, the voltage across R_X is equal to the voltage across R_E, or $I_E R_E$ volts.

When the basic assumptions are substituted into the bias circuit equation, the relationship,

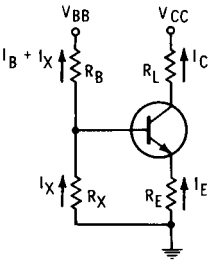


Fig. 4-3. Current through transistor for bias circuit II.

$$I_C = \frac{\beta R_X V_{BB} + (\beta + 1) I_{CBO} (R_E R_B + R_E R_X + R_B R_X)}{(\beta + 1) R_E (R_B + R_X) + R_B R_X} \tag{4-4}$$

is evolved. The various stability equations for this circuit are:

$$S = \frac{(\beta + 1)(R_E R_B + R_E R_X + R_B R_X)}{(\beta + 1) R_E (R_B + R_X) + R_B R_X} \tag{4-5}$$

$$S_E = \frac{\beta R_X}{(\beta + 1) R_E (R_B + R_X) + R_B R_X} \tag{4-6}$$

$$S_\beta = \frac{(R_X V_{BB} + I_{CBO} R_B R_X)(R_E R_B + R_E R_X + R_B R_X)}{[(\beta + 1) R_E (R_B + R_X) + R_B R_X]^2} \tag{4-7}$$

The equations apply to bias circuit VI. Ignore the presence of the diode. The stability will be better than indicated by the equations due to the action of the diode. This will compensate only for the variations of V_{BE} with temperature.

With only slight modification, the equations just stated will apply to bias circuits I and IV. In both instances, R_X is made equal to infinity since it does not exist in the circuit. The equation for collector current becomes:

$$I_C = \frac{\beta V_{BB} + (\beta + 1) I_{CBO} (R_E + R_B)}{(\beta + 1) R_E + R_B} \tag{4-8}$$

The stability equations simplify to:

$$S = \frac{(\beta + 1)(R_E + R_B)}{(\beta + 1) R_E + R_B} \tag{4-9}$$

$$S_E = \frac{\beta}{(\beta + 1) R_E + R_B} \tag{4-10}$$

$$S_\beta = \frac{(R_E + R_B) V_{BB} + I_{CBO} R_B (R_E + R_B)}{[(\beta + 1) R_E + R_B]^2} \tag{4-11}$$

For bias circuit I, V_{BB} in the equations is replaced by V_{CC}, while in circuit IV, it is replaced by V_{EE}.

The equations can be simplified further when R_E is not part of the circuit, as in Fig. 3-1A. In this case, R_E is made equal to zero in Equations 4-8 through 4-11.

Another bias circuit arrangement, not discussed as such, is shown in Fig. 4-4. Here, R_B is connected to the collector of the transistor. The collector current for this circuit is:

$$I_C = \frac{\beta R_X V_{CC} + (\beta+1) I_{CBO}[R_X(R_L + R_E + R_B) + R_E(R_L + R_B)]}{(\beta+1)[R_E(R_L + R_B + R_X) + R_X R_L] + R_B R_X} \tag{4-12}$$

The stability factors are,

$$S = \frac{(\beta+1)[R_X(R_L + R_E + R_B) + R_E(R_L + R_B)]}{(\beta+1)[R_E(R_L + R_B + R_X) + R_X R_L] + R_B R_X} \tag{4-13}$$

$$S_E = \frac{\beta R_X}{(\beta+1)[R_E(R_L + R_B + R_X) + R_X R_L] + R_B R_X} \tag{4-14}$$

$$S_\beta = \frac{[R_X V_{CC} + R_X R_B I_{CBO}][R_E(R_L + R_B + R_X) + R_X(R_L + R_B)]}{\{(\beta+1)[R_E(R_L + R_B + R_X) + R_X R_L] + R_B R_X\}^2} \tag{4-15}$$

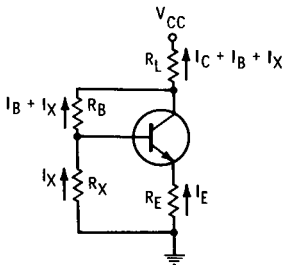


Fig. 4-4. Modification of bias circuit II.

Bias circuit V is identical to that in Fig. 4-4 with the exception that R_X has been omitted. Setting R_X equal to infinity, Equations 4-12 through 4-15 become:

$$I_C = \frac{\beta V_{CC} + (\beta+1) I_{CBO}(R_L + R_E + R_B)}{(\beta+1)(R_E + R_L) + R_B} \tag{4-16}$$

$$S = \frac{(\beta+1)(R_L + R_E + R_B)}{(\beta+1)(R_E + R_L) + R_B} \tag{4-17}$$

$$S_E = \frac{\beta}{(\beta+1)(R_E + R_L) + R_B} \tag{4-18}$$

$$S_\beta = \frac{(V_{CC} + I_{CBO} R_B)(R_L + R_E + R_B)}{[(\beta+1)(R_E + R_L) + R_B]^2} \tag{4-19}$$

USING STABILITY EQUATIONS

When analyzing the stability equations, it becomes obvious that some circuits are more stable than others in various respects. How can one determine which circuit to use?

S is a number that establishes the ratio of collector current change to the change of leakage current through the collector-base junction. The closer this number approaches "1," indicating that the change is small, the better the temperature stability of the circuit.

The use of this ratio can best be explained with an example. If the I_{CBO} of a germanium transistor at 25°C is 10 microamps, at 65°C it will be 160 microamps. This can be determined from the graph in Fig. 4-2. The change in I_{CBO} is $160 - 10 = 150$ microamps. Now assume that S equals 5. The change in collector current will then be $5 \times 150\ \mu A = 750$ microamps.

Is this change tolerable? Only the designer can determine this. Assuming the transistor operates properly at 25°C, the effect of the additional 750 microamps should be checked. If the transistor remains within a desired operating region, the stability of the circuit is satisfactory. If not, the circuit must be modified componentwise, or a more satisfactory bias method should be found.

In general, all the equations indicate that the stability with changes in I_{CBO} will be improved if R_E and R_L are large resistors and R_B and R_X are small. The circuit in Fig. 4-4 is superior to others because of the dc feedback from collector to base.

The stability with supply voltage change, S_E, is at its best when all resistors with the exception of R_X are made as large as practical.

In all circuits, R_X should be small and R_E, R_B, and R_L large, if collector current change with beta variation is an important factor.

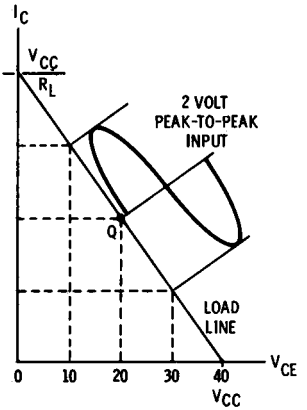
Where all three types of stability are important, make R_L and R_E as large as possible consistent with circuit requirements and R_X small. R_B is usually governed by the size of the other components in the circuit.

All circuits should be checked for stability by substituting the numbers into the appropriate equations. It is easier to change a paper design than an actual physical unit after it has gone through environmental testing. A small preproduction run of an item using random components should be made only after all calculations have been performed and all conditions satisfied mathematically.

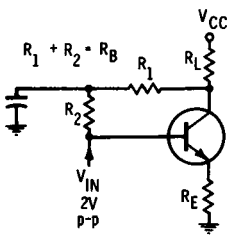
A proper design procedure is illustrated in the following practical example. Assume that you wish to design an audio amplifier for production, with a minimum gain of 10. The required output impedance is to be less than 5000 ohms. The input signal is 2 volts peak-to-peak with a source impedance of 1000 ohms. It is to operate through a temperature range of 0°C to 45°C. The power supply may be any value but can vary ±10% from the center. The only economical transistor available is a silicon device with a 40-volt collector breakdown rating, which can handle a maximum of 100 mA collector current. The maximum power dissipation is 200 mW. β varies from unit to unit; it ranges from 100 to 300 with the median unit at 200. The maximum I_{CBO} at 25°C is 0.1 microamp.

The design should start with the choice of a circuit. If the circuit is to have a gain of 10, it means that there is to be at least 20 volts peak-to-peak

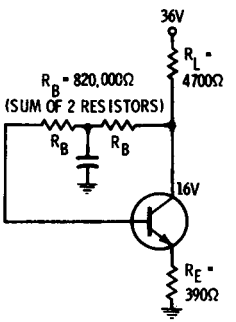
at the output. This is 10 times the 2 volts peak-to-peak fed to the input. The transistor is rated at 40 volts. Suppose we choose a 40-volt supply. Draw a temporary load line as shown in Fig. 4-5A. The load line connects two points at its extremes on the axis. At one point, it is assumed that the supply voltage is across the transistor with zero collector current. At the second point, there is 0 volt across the transistor, the entire supply voltage is across the load resistor, and the collector current is V_{CC}/R_L. This method for drawing the load line is identical to the ones previously employed.



(A) Load line (characteristic curves omitted).



(B) Bias circuit V.



(C) Bias circuit V with values indicated.

Fig. 4-5. Methods of solving problem.

If the transistor is biased so that the quiescent point is at the center of the load line, there will be 20 volts across the transistor when no signal is applied. When there is signal at the input, the collector must be capable of swinging the 20 volts required at the output. If the 20-volt swing is to be symmetrical about the quiescent voltage, the collector voltage will vary from 10 to 30 volts. The maximum possible collector voltage swing is from

0 to 40 volts. The 10- to 30-volt actual swing is a good part of the maximum possible excursion for the collector voltage. Reasonably good stability is required so that the Q point should not travel (at elevated temperatures) to a point too high or too low on the load line. The output swing must not be limited at either peak of the cycle. The quiescent point must never be such as to limit the swing to less than ± 10 volts about the Q point. The full ± 10-volt capability must exist if there is to be a relatively undistorted output voltage developed across the load resistor, and if the circuit is to provide a gain of 10.

As a first trial, choose bias circuit V, which is redrawn in Fig. 4-5B.

Make some educated guesses as to component values. The output impedance must be less than 5000 ohms. We can assure this by letting R_L be 5000 ohms or less. Choose the next smaller standard 10% resistor—4700 ohms.

The overall ac gain must be a minimum of 10. This would indicate that the ratio of R_L to R_E is 10. If we chose $R_E = 470$ ohms, the gain would be just 10. If the β of the transistor were at its minimum of 100, the input impedance would be $470 \times 100 = 47{,}000$ ohms. With a source impedance of 1000 ohms, the overall gain would be about 2% low. Choose the next lower standard resistor (390 ohms, 10%) so that we will always be assured of sufficient gain.

Although R_B provides ac as well as dc feedback, the gain can be increased to compensate for the loss due to the feedback. A technique frequently employed uses two resistors that add up to the required R_B. The junction of the two resistors is bypassed to ground with a capacitor. There will be dc feedback but no ac feedback at most frequencies, with no subsequent loss of ac gain. The size of the capacitor will be discussed in a later chapter.

The maximum voltage permissible across the transistor is 40 volts. The supply voltage can vary $\pm 10\%$. If we made V_{CC} equal to 40 volts, the supply voltage could rise 10% to 44 volts. It is wiser to choose a supply voltage that is 10% below the transistor breakdown value (in this case, 36 volts). It cannot exceed BV_{CE}, the collector-emitter breakdown voltage, even when the supply voltage is high.

The quiescent collector voltage should be about half the supply voltage, or 18 volts. The other half of the supply voltage will be developed across the emitter and collector resistors. Assume that the voltage across the emitter resistor is negligible when compared to the voltage across R_L.

The average collector current can be determined from the equation $I_C = (V_{CC}/2)/R_L = 18$ volts/4700 ohms $= 3.8$ mA. Because the average transistor has a β equaling 200, the design center for the base current is $3.8 \times 10^{-3}/200 = 19 \times 10^{-6}$ amperes. The voltage across the 390-ohm emitter resistor is about $(390)(3.8 \times 10^{-3}) = 1.48$ volt. The base-emitter voltage for a silicon transistor is about 0.6 or 0.7 volt. The voltage at the base is $1.48 + V_{BE}$, or about 2.1 volts. The voltage across R_B is the voltage at the

collector minus the voltage at the base or $18 - 2.1 = 15.9$ volts. The size of the resistor is $R_B = V_{CB}/I_B = 15.9/(19 \times 10^{-6}) = 840{,}000$ ohms. Select the standard 820,000-ohm 10% resistor for the circuit.

Now that the approximate circuit has been designed, check the results using Equations 4-16 through 4-19.

At 25 °C, with $\beta = 200$ and $V_{CC} = 36$ volts, the collector current is:

$$I_C = \frac{200(36) + 201(10^{-7})(4700 + 390 + 820{,}000)}{(201)(390 + 4700) + 820{,}000} = 3.93 \text{ mA}$$

This means that the voltage across the transistor is $36 - (3.93 \times 10^{-3})(4700 + 390) = 16$ volts. This equation provided us a solution more accurate than our original estimate of 18 volts. Using these center design parameters, the transistor can easily swing the ±10 volts above and below the quiescent 16 volts.

$$S = \frac{(201)(4700 + 390 + 820{,}000)}{(201)(390 + 4700) + 820{,}000} = 90$$

Ninety is a poor figure for S. Let us see what happens.

At 45 °C, $I_{CBO} = (0.1 \times 10^{-6})10 = 10^{-6}$ amps. (The multiplication factor, "10", is determined from Fig. 4-2.) I_{CBO} has increased by 10^{-6} amps $- 0.1 \times 10^{-6}$ amps $= 0.9 \times 10^{-6}$ amps, at 45 °C over its 25 °C value. The collector current increase is S times the change in I_{CBO} or $90 \times (0.9 \times 10^{-6})$ amps or 0.081×10^{-3} amps. The total collector current is 3.93 mA + 0.081 mA = 4.011 mA so that the voltage across the transistor is $36 - (4.011 \times 10^{-3})(4700 + 390) = 15.6$ volts. The transistor can readily swing ±10 volts about the 15.6-volt quiescent point without distortion.

At 0 °C, the ratio $I_{CBO}@T/I_{CBO}@25\,°C$ is approximately 50×10^{-3} from Fig. 4-2. Hence, I_{CBO} at 0 °C is $(0.1 \times 10^{-6})(5 \times 10^{-2}) = 0.005 \times 10^{-6}$ amps. I_{CBO} dropped $0.1 \times 10^{-6} - 0.005 \times 10^{-6} = 0.095 \times 10^{-6}$ amps. The collector current change is S times the change in I_{CBO} or $90 \times (0.095 \times 10^{-6}) = 8.55 \times 10^{-6}$ amps. This is negligible compared to the total current and will only slightly affect the quiescent voltage point. It need not be checked further.

The effect of supply voltage changes on the collector current can be checked with Equation 4-18.

$$S_E = \frac{200}{201(4700 + 390) + 820{,}000} = 1.09 \times 10^{-4}$$

If the voltage changes by 10% of 36 volts, or 3.6 volts, the collector current will change by $(1.09 \times 10^{-4})\,3.6 = 0.392$ mA.

When the voltage rises to 10% above the 36 center voltage, the collector current will be 3.93 + 0.392 = 4.322 mA and the quiescent voltage across the transistor is $36 + 3.6 - (4.322 \times 10^{-3})(4700 + 390) = 17.6$ volts. If the voltage drops 10% below 36, the collector current will be 3.93 − 0.392 = 3.538 mA and the voltage across the transistor is 36 −3.6 −

$(3.538 \times 10^{-3})\ (4700 + 390) = 14.4$ volts. In either case, the transistor can swing the required amount.

The change of collector current with β can be determined with Equation 4-19:

$$S_\beta = \frac{[36 + (10^{-7})8.2 \times 10^5]\,[4700 + 390 + 820{,}000]}{[201(.39 \times 10^3 + 4.7 \times 10^3) + 820 \times 10^3]^2}$$

$$S_\beta = 8.8 \times 10^{-6}.$$

If β changes by 100, the collector current will change by:

$$\Delta I_C = S_\beta \Delta\beta = 8.8 \times 10^{-6} \times 100 = 0.88 \times 10^{-3}$$

When $\beta = 300$, the collector current is 3.93 mA $\times$ 0.88 mA = 4.81 mA. The voltage across the transistor is $36 - (4.81 \times 10^{-3})(4700 + 390) =$ 10.5 volts. In this case, a $\pm$10-volt swing is barely possible.

Should $\beta = 100$, the collector current is 3.93 mA $-$ 0.88 mA = 3.05 mA. The voltage across the transistor is $36 - (3.05 \times 10^{-3})(4700 + 390) =$ 20.5 volts. The $\pm$10-volt swing can be executed easily.

A check should also be made to see if the transistor will operate properly if all three factors change the collector current in the same direction.

The maximum current that the transistor will be required to conduct is $V_{CC}/(R_L + R_E) = 39.6/(4700 + 390) = 7.8$ mA. Here, V_{CC} is the maximum value of supply voltage. This is well within the 100-mA rating.

The maximum power dissipated by the transistor collector junction occurs when the idling point is at the exact center of the maximum possible voltage and current swings. It is $(39.6/2)(7.8 \times 10^{-3}/2) = 77$ mW. This is also within the rating.

The overall design should work. It should be checked in the laboratory on a run of random components under the different environmental conditions.

STABILITY AND DC COUPLING

There are many schemes of direct-coupling one stage to another. The temperature stability of each stage is affected by the leakage current in the previous stage and the component arrangements within each amplifier.

Stability studies have been made on dc-coupled amplifiers. These equations are long and complex, offering little to the designer.

It is suggested that each stage be designed for the best stability characteristics within itself. Then the overall design should be checked in the laboratory at the extremes of the required operating temperature range.

Chapter 5

LOW-FREQUENCY SMALL-SIGNAL AMPLIFIERS

Up to this chapter, we were primarily concerned with dc-biasing the transistor and maintaining the stability within reasonable bounds. There was some reference made to ac gain in the problems.

In this chapter, the discussion centers on ac gain and ac impedance. The three different circuit arrangements will be detailed in this respect. The ac equivalents are shown for three circuit arrangements. As in the case with all ac signal equivalent circuits, the dc components have been omitted. However, it must be remembered that the dc bias currents do affect the values of the ac parameters.

In the interest of flexibility, several different equivalent circuits have been devised for each of the three arrangements. The *equivalent "T"* representation is popular since it looks very much like the actual transistor. The "h" or *hybrid equivalent* of the transistor circuit has been in widespread use for many years. Some manufacturers specify their transistors using the h-parameters.

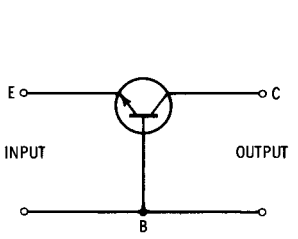
For a relatively complete presentation, these two equivalent circuits will be shown here and the meaning of the parameters will be discussed. The relationships between the two sets of parameters will be tabulated.

It should be remembered that most parameters vary with temperature, collector current, and collector-emitter voltage. Correction factors are frequently presented in the specification sheets detailing the parameter variations. When the correction factors are available, they should be applied to the specified parameters before the numbers are substituted into the equations.

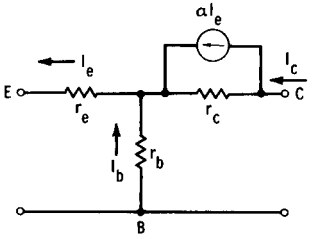
This chapter will look like a maze of numbers and equations. Actually, much of this information can be deduced from earlier discussions. The meanings of r_b, r_e, r_c, and r_d have been discussed previously. The data is organized here only for convenience and reference.

EQUIVALENT CIRCUITS

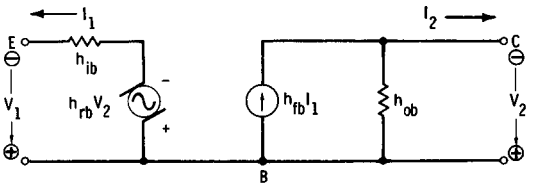
The common-base circuit and its equivalent "T" and equivalent "h" representations are shown in Fig. 5-1. Similar representations are presented in Fig. 5-2 and Fig. 5-3 for the common-emitter and common-collector circuits, respectively. In each case, the equivalent "T" circuit, shown in "B" of the figures, is self-explanatory. It resembles the transistor in the particular arrangement. The parameters remain the same for all types of circuits.



(A) Common-base circuit.



(B) Equivalent "T" circuit of Fig. 5-1A.



(C) Equivalent circuit of Fig. 5-1A indicating h-parameters.

Fig. 5-1. Common base and its equivalent circuit.

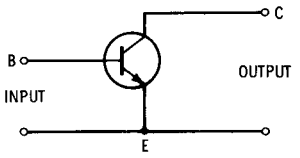
The emitter resistance, r_e, is equal to $26/I_E$ at 25°C, where I_E is expressed in milliamps. The ac emitter resistance evidently varies with the dc quiescent emitter current.

The resistance in the base is r_b, and r_c and r_d are collector resistances discussed in Chapter 3.

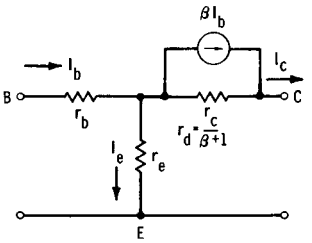
The collector resistance in the common-base configuration is r_c, and r_d is the collector resistance in the common-emitter configuration. Should the impedance between the base and emitter leads be small, the collector resistor approaches r_c, a large value. If the impedance between the base and emitter is large, the collector resistance approaches r_d, a small number. In either case, r_c and r_d are related by the equation $r_c = \beta r_d$.

A current gain factor appears in each output loop. In Fig. 5-1, it is αI_e while in Figs. 5-2 and 5-3, it is βI_b.

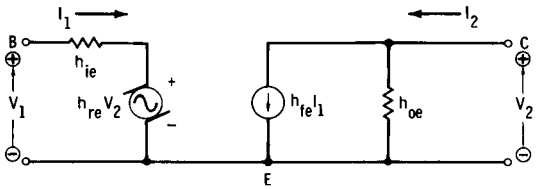
The ac and dc values of β differ from each other. Both ac and dc β can be determined from a set of collector curves; β should be derived at a specific value of collector-emitter voltage.



(A) Common-emitter circuit.



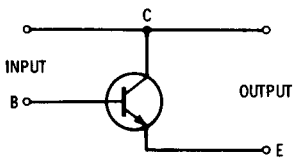
(B) Equivalent "T" circuit of Fig. 5-2A.



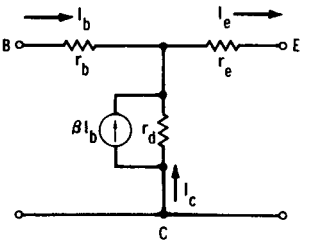
(C) Equivalent circuit of Fig. 5-2A indicating h-parameters.

Fig. 5-2. Common emitter and its equivalent circuit.

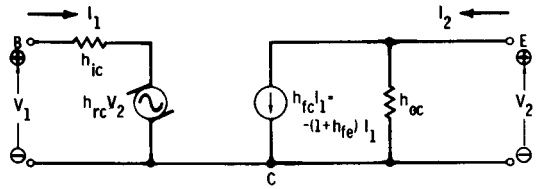
A hypothetical group of collector characteristic curves is shown in Fig. 5-4. Mark the collector-emitter voltage, V_{CEQ}, on the horizontal axis and draw a vertical line from this point. Next, draw horizontal lines from the points at which the V_{CEQ} line just drawn crosses the I_B base current plots.



(A) Common-collector circuit.



(B) Equivalent "T" circuit of Fig. 5-3A.



(C) Equivalent circuit of Fig. 5-3A indicating h-parameters.

Fig. 5-3. Common collector and its equivalent circuit.

The dc beta is the ratio of the collector current to the base current at any point on the V_{CE} line. It will vary with base current. β_{dc} is the dc current gain at a specific collector current. When the collector current is I_{C3}, for example, the direct current beta equals I_{C3}/I_{B3}.

The ac beta is the current gain for an ac signal. It is approximately equal to the ratio of the change of collector current to the change in base current causing it. It is different at the various portions of the display. Around I_{B3}, the ac beta is:

$$\beta_{ac} = \frac{I_{C4} - I_{C2}}{I_{B4} - I_{B2}}$$

The ac and dc beta frequently do not differ by a large factor. The relative ac and dc alphas can be derived from β using the equation $\alpha = \beta/(\beta + 1)$.

The equivalent "h" or hybrid equivalent circuits all appear in "C" of Figs. 5-1 through 5-3. The letter "h" indicates that a parameter refers to the hybrid circuit. The first subscript letter next to the "h" indicates the type of parameter. The second subscript letter describes the circuit to which the parameter refers. If the second subscript is "b," the parameter is for the common-base circuit; "e" refers to the common-emitter circuit; and "c" refers to the common-collector circuit.

The type of hybrid parameters has also been defined by numerical subscripts. The following is a list of comparative symbols and definitions of

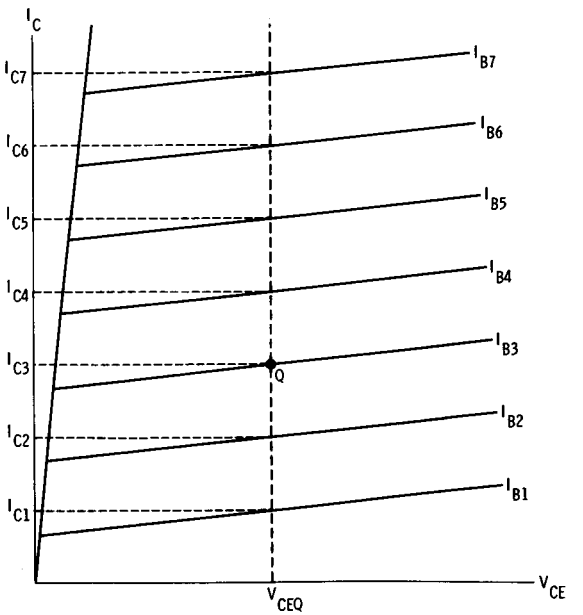


Fig. 5-4. Using collector characteristics to determine ac and dc beta.

the hybrid parameters. Refer to any of the figures to see where the symbols are used.

$h_{11} = h_i = V_1/I_1 =$ The input impedance when the output is short-circuited, as when $V_2 = 0$.

$h_{22} = h_o = I_2/V_2 =$ The output admittance when the input is open-circuited, as when $I_1 = 0$. The output impedance is $1/h_o$.

$h_{21} = h_f = I_2/I_1 = -\alpha$ for the common-base circuit. In the common-emitter circuit, it is equal to β. The ratio of the output current to the input current is h_f when the output is short-circuited, as when $V_2 = 0$. It is the current gain from the input to the output.

$h_{12} = h_r = V_1/V_2 =$ The ratio of the voltage at the input circuit fed back through the transistor from the output circuit, to the voltage at the output. Here, the input is open-circuited, as when $I_1 = 0$.

COMMON-BASE CIRCUIT

A common-base circuit is shown in Fig. 5-5. The various characteristics of the circuit can be determined with the "h" or "T" parameters. The equivalent "T" parameters produce equations similar to those used previously to determine the bias networks. Relatively accurate relationships will be derived using these parameters.

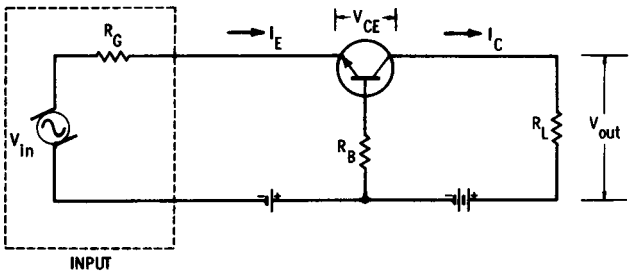


Fig. 5-5. Common-base circuit.

The input resistance of the transistor, or the resistance presented to the input source by the base circuit, is equal to the sum of the emitter resistance, r_e, and beta divided into the total resistance in the base circuit, $(r_b + R_B)/\beta$.

$$R_{in} = r_e + \frac{r_b + R_B}{\beta} \qquad (5\text{-}1)$$

The output resistance looking back into the collector-base circuit is more complex:

$$R_{out} = \frac{r_c[r_b + R_B + \beta(r_e + R_G)]}{\beta(R_B + r_b + r_e + R_G)} \tag{5-2}$$

The load resistor, R_L, looks into the transistor and sees R_{out}. Any load connected across R_L sees R_L in parallel with R_{out} or $R_L R_{out}/(R_L + R_{out})$.

The current gain is:

$$A_i = \frac{I_C}{I_E} = \alpha = \frac{\beta}{\beta + 1} \text{ (less than 1)} \tag{5-3}$$

while the voltage gain is the ratio of the output load impedance to the input impedance, or:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{R_L}{\frac{R_B + r_b}{\beta} + r_e + R_G} \tag{5-4}$$

If another load is across R_L, the R_L in the voltage gain equation no longer refers to the resistor in the circuit only, but to the resistance of the parallel combination of the load.

The power gain, G, is the voltage gain multiplied by the current gain. Numerically, it is slightly less than the voltage gain.

When h-parameters are listed in transistor specification sheets, they may be converted to the T-parameters. The h-parameters are stated at a specific quiescent collector current and collector-emitter voltage. Should the transistor be used under other quiescent conditions, the h-parameters must be changed so that the parameters will be correct for the actual I_B and V_{CE} at which the device is operating. Curves defining these correction factors are available for the different transistors. Make the corrections before applying the following equations.

Use Equations 5-5 through 5-9 to convert the h-parameters to T-parameters. Then use Equations 5-1 through 5-4 to determine gain and impedance.

$$r_e = h_{ib} - \frac{h_{rb}(1 + h_{fb})}{h_{ob}} = h_{ib} - \frac{h_{rb}}{h_{ob}(h_{fe} + 1)} \tag{5-5}$$

$$r_b = \frac{h_{rb}}{h_{ob}} \tag{5-6}$$

$$r_c = \frac{1}{h_{ob}} \tag{5-7}$$

$$r_d = \frac{r_e}{h_{fe}} = \frac{1}{h_{ob}h_{fe}} \tag{5-8}$$

$$\alpha = -h_{fb} = \frac{h_{fe}}{1 + h_{fe}} \tag{5-9}$$

$$\beta = -\frac{h_{fb}}{1 + h_{fb}} = \frac{\alpha}{1 - \alpha} = h_{fe} \tag{5-10}$$

COMMON-EMITTER CIRCUIT

The conventional common-emitter circuit is shown in Fig. 5-6. The equations describing this circuit are:

$$R_{in} = r_b + \beta(R_E + r_e) \tag{5-11}$$

This is the resistance in the base circuit added to β multiplied by the resistors in the emitter circuit.

$$R_{out} = r_d \frac{[(R_G + r_b) + (r_e + R_E)\beta]}{(R_G + r_b + r_e + R_E)} \tag{5-12}$$

$$A_i = \beta = \frac{\alpha}{1 - \alpha} \tag{5-13}$$

$$A_v = \frac{\beta R_L}{\beta(r_e + R_E) + r_b} \approx \frac{R_L}{R_E} \tag{5-14}$$

$$G = \frac{\beta^2 R_L}{\beta(r_e + R_E) + r_b} \tag{5-15}$$

G is the power gain. If another load is in parallel with R_L, R_{out} and R_L are treated as described in the common-base section.

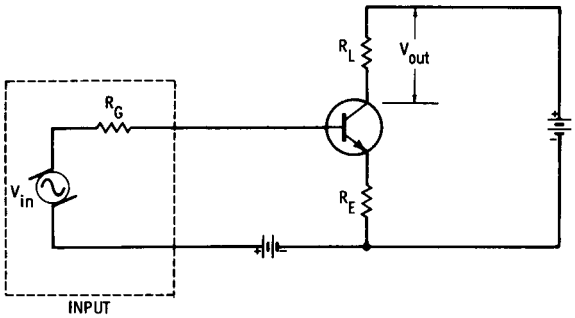


Fig. 5-6. Common-emitter circuit.

If the equivalent "h" parameters are specified by a manufacturer for the common-emitter mode of operation, the h-parameters should be converted to the common-base forms using the relationships:

$$h_{ib} = \frac{h_{ie}}{h_{fe} + 1} = r_e + (1 - \alpha) r_b \tag{5-16}$$

$$h_{rb} = \frac{h_{ie} h_{oe}}{h_{fe} + 1} - h_{re} = \frac{r_b}{r_c} \tag{5-17}$$

$$h_{fb} = -\frac{h_{fe}}{h_{fe} + 1} = -\frac{\beta}{\beta + 1} = -\alpha \tag{5-18}$$

$$h_{bo} = \frac{h_{oe}}{h_{fe} + 1} = \frac{1}{r_c} \tag{5-19}$$

Next, use Equations 5-5 through 5-10 to derive the equivalent "T" parameters for substitution into the common-emitter equivalent "T" equations.

COMMON-COLLECTOR CIRCUIT

A common-collector circuit is shown in Fig. 5-7. The equations for this circuit are:

$$R_{in} = r_b + \beta(R_E + r_e) \tag{5-20}$$

This is the resistance in the base in addition to beta multiplied by the sum of the resistances in the emitter circuit. Should another load resistor shunt

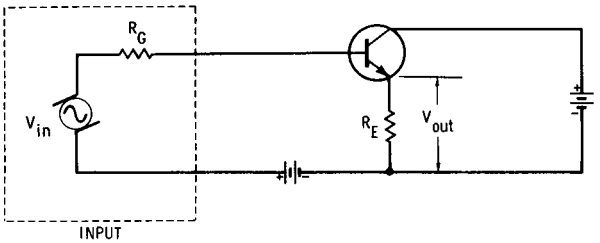


Fig. 5-7. Common-collector circuit.

R_E, the R_E in the equation changes to the resistance of the shunt resistor in parallel with R_E.

$$R_{out} = r_e + \frac{R_G + r_b}{\beta} \tag{5-21}$$

The impedance presented to the output load is the emitter resistance, r_e, plus β divided into the impedance in the base circuit. Impedances from the emitter circuit, when transferred to the base circuit, appear as if they were multiplied by β. In the reverse direction, impedances in the base circuit, when transferred to the emitter circuit, appear as if they were divided by β. Looking from an external load that may be connected across R_E, the load will see an output impedance equal to R_{out} in parallel with R_E.

$$A_v \approx 1 \tag{5-22}$$

$$A_i = \frac{1}{1-\alpha} \approx \beta \tag{5-23}$$

$$G = \frac{1}{1-\alpha} \approx \beta \tag{5-24}$$

If the equivalent "h" parameters are specified in the common collector mode, convert them to the common base equivalent "h" parameters using the equations:

$$h_{ib} = -\frac{h_{ic}}{h_{fc}} = r_e + r_b(1-\alpha) \tag{5-25}$$

$$h_{rc} = h_{rc} - 1 - \frac{h_{ic}h_{oc}}{h_{fc}} = \frac{r_b}{r_c} \tag{5-26}$$

$$h_{fb} = -\frac{h_{fc}+1}{h_{fc}} = -\alpha \tag{5-27}$$

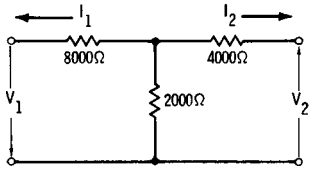
$$h_{ob} = -\frac{h_{oc}}{h_{fc}} = \frac{1}{r_c} \tag{5-28}$$

Now substitute these newly derived h-parameters into Equations 5-5 through 5-10 to determine the equivalent "T" parameters.

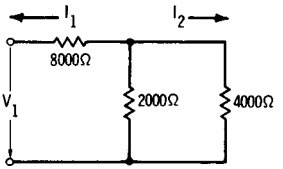
EXAMPLES

Now that we have armed ourselves with equations for all circuit situations, let us try solving some problems. The equations are approximations; our solutions will be even more approximate. In some instances, we will compare the solutions derived by logic to the solutions arrived at by using the equations. Each problem is designed to present information or to indicate methods in design and analysis.

The h-parameters can be determined for any circuit. The equivalent circuits using h-parameters are unchanged from those shown above for any arrangement. Only the sizes of the parameters change. Problem 1 is presented to provide insight into the equivalent "h" circuit.



(A) Equivalent circuit for problem 1.



(B) Fig. 5-8A with output shorted.

Fig. 5-8. Circuit for problem 1.

Problem 1—Determine the h-parameters for the circuit in Fig. 5-8A and draw the equivalent "h" circuit of Fig. 5-8A in Fig. 5-9. Calculate the gain and input and output impedances if an input voltage of V_{in} volts with a source resistance, R_G, of 1000 ohms were connected at the input and a load, R_L, of 9000 ohms were across the output.

The input resistance is h_i when the output is short-circuited. The circuit then appears as redrawn in Fig. 5-8B. The 4000-ohm resistor is in parallel with the 2000-ohm resistor, resulting in an equivalent parallel resistance of $(2000)(4000)/(2000+4000) = 1333$ ohms. The total resistance presented to V_1 is 8000 + 1333 ohms = 9333 ohms.

The reciprocal of the output resistance is h_o when $I_1 = 0$, or the input circuit is opened. The admittance at the output is $1/(4000 + 2000) = 1/6000 = I_2/V_2$. The 8000-ohm resistor is effectively connected to an open circuit and thus has no effect on h_o.

The current gain from input to output (h_f), is I_2/I_1, when $V_2 = 0$, or is shorted as shown in Fig. 5-8B. Solve for I_2 in terms of I_1.

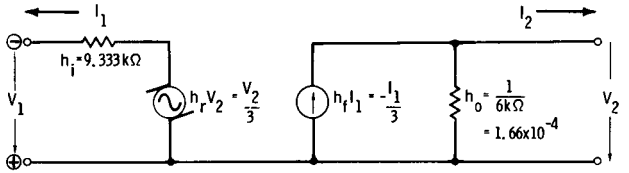


Fig. 5-9. Equivalent "h" circuit of Fig. 5-8A.

The total current, I_1, is divided between the 2000-ohm resistor and the 4000-ohm resistor. Using the current divider equation, the portion of I_1 passing through the 4000-ohm resistor is:

$$I_2 = -\frac{2000I_1}{2000 + 4000} = -\frac{I_1}{3}$$

The current ratio of I_2 to I_1 is:

$$h_f = -\frac{I_1/3}{I_1} = -\frac{1}{3}$$

The negative sign indicates that the currents are in opposite directions.

The ratio of voltage in the input circuit due to the voltage at the output, is h_r, when the input is open-circuited. If the input is open-circuited, there will be no current through the 8000-ohm resistor, and therefore no voltage drop across it. V_1 will be at the junction of all the resistors. V_1 is due to V_2. V_1, using the voltage divider equations, is:

$$V_1 = \frac{2000V_2}{4000 + 2000} = \frac{V_2}{3}$$

The reverse voltage ratio, V_1/V_2, is:

$$h_r = \frac{V_2/3}{V_2} = \frac{1}{3}$$

The equivalent "h" circuit can now be drawn in Fig. 5-9. This is the exact circuit previously drawn for the h-parameters of the transistor. This circuit can and has been used to represent the transistor. Assume that it represents some transistor configuration rather than the passive circuit it was derived from.

At the input, connect a voltage, V_{in}, with a resistance of R_G ohms. Assume a voltage, V_{out}, is across a load, R_L, at the output. The gains and impedances of this circuit can be calculated directly without converting to the equivalent "T" parameters. The formulas for this are:

$$R_{in} = h_i - \frac{h_r h_f R_L}{1 + h_o R_L} \tag{5-29}$$

$$R_{out} = \frac{h_i + R_G}{h_o(h_i + R_G) - h_r h_f} \tag{5-30}$$

$$A_v = \frac{h_f R_L}{h_i + R_L(h_i h_o - h_r h_f)} \tag{5-31}$$

$$A_i = \frac{h_f}{1 + h_o R_L} \tag{5-32}$$

$$G = A_v A_i \tag{5-33}$$

If in this example, R_L were 9000 ohms and R_G were 1000 ohms, the characteristics of the circuit would be:

$$R_{in} = 9.33 \times 10^3 - \frac{\left(\frac{1}{3}\right)\left(-\frac{1}{3}\right)(9 \times 10^3)}{1 + (1.66 \times 10^{-4})(9 \times 10^3)} = 9.73 \times 10^3 \text{ ohms}$$

$$R_{out} = \frac{9.33 \times 10^3 + 10^3}{(1.66 \times 10^{-4})(9.33 \times 10^3 + 10^3) - \left(\frac{1}{3}\right)\left(-\frac{1}{3}\right)} = 5.64 \times 10^3 \text{ ohms}$$

$$A_v = -\frac{\left(-\frac{1}{3}\right)\left(9 \times 10^3\right)}{9.33 \times 10^3 + 9 \times 10^3\left[(9.33 \times 10^3)(1.66 \times 10^{-4}) - \left(\frac{1}{3}\right)\left(-\frac{1}{3}\right)\right]} = \frac{1}{8.11}$$

$$A_i = \frac{\left(-\frac{1}{3}\right)}{1 + (1.66 \times 10^{-4})(9 \times 10^3)} = -\frac{1}{7.5}$$

It should be clearly noted here that h_i and h_f are the input impedance and current gain of the circuit, respectively, with the output terminals shorted. R_{in} and A_i are these factors with actual loads connected at the input and output.

Similarly, h_o and h_r are the output admittance and the ratio of input to output voltage (inverse of voltage gain) of the circuit, respectively, with the input open-circuited. R_{out} and A_v are the inverse of these same factors with the actual loads connected at the input and output.

Problem 2—Calculate the impedances and gains of the circuit in Fig. 5-10. The transistor parameters are stated in the figure.

Just by observing the components in the figure and the data supplied, we can arrive at some pretty good approximations of the gain and impedances in the circuit.

The voltage gain of the transistor itself is the ratio of the 4000-ohm resistor to the 400-ohm resistor, or 10.

The current gain is approximately equal to beta. In this example, $h_{fe} = 50$.

The input impedance of the device itself is $\beta(400\Omega) = 20{,}000$ ohms.

The output impedance is more than r_d and less than r_c. $1/h_{ob}$ is r_c because it is the reciprocal of the output impedance in the common-base mode of operation. $1/h_{ob} = 10^6$ ohms. Hence, $r_d = 10^6$ ohms$/\beta = 20{,}000$ ohms. The output impedance is between 20,000 ohms and 10^6 ohms. As we shall see, this range is not outlandishly large although the spread of numbers is large.

It should be emphasized that the data just derived refers to the device itself and not to the complete circuit. More on this will be discussed later. First let us calculate the gains and impedances using the h-parameters and formulas stated above. We will substitute the h-parameters into Equations 5-5 through 5-10 and get the equivalent "T" parameters. Then, Equations 5-11 through 5-15 will be used to derive the gains and impedances of the device and the circuit.

The data shown for the h-parameters in Fig. 5-10 is for one specific quiescent condition—when $I_C = 1$ mA and $V_{CE} = 5$ volts. The data must be corrected, because the actual idling conditions of the device differ from the idling conditions used in specifying the parameters. The approximate quiescent base current, can be derived with the methods of Chapters 3 or 4. The supply is 20 volts. The entire base current is through the 400,000-ohm resistor. The 400-ohm resistor appears to the supply as 400 ohms multiplied by β. Assuming that the ac and dc betas are equal, this product is $(400)(50) = 20{,}000$ ohms. The base current through the series combination of the 20,000Ω and 400,000Ω resistors is, if the base-emitter voltage is considered negligible, $I_B = 20$ volt/420,000 ohms $= 4.75 \times 10^{-5}$ amps. The dc collector current is about β times the base current or $(50)(4.75 \times 10^{-5}$ amps$) = 2.37 \times 10^{-3}$ amps. The quiescent voltage across the transistor is $20 - [(2.37 \times 10^{-3})\ (4{,}000 + 400)] = 9.6$ volts.

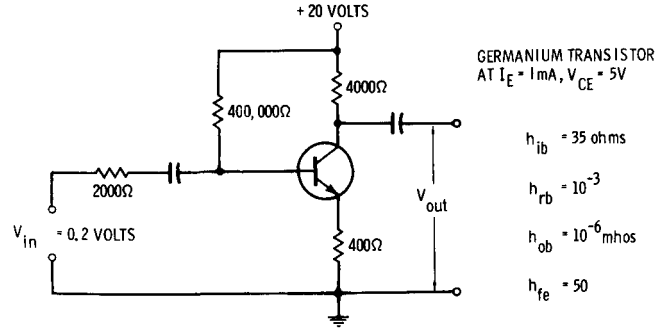


Fig. 5-10. Circuit for problem 2.

To sum up, the approximate collector-to-emitter quiescent voltage is 9.6 volts and the approximate quiescent collector current is 2.37 mA, which is also approximately equal to the emitter current. Although neither the current nor voltage figure is accurate, it is as close as we can get with the information available. Round off the numbers to facilitate working with them. Let $V_{CE} = 9.6$ volts and $I_E = 2.4$ mA.

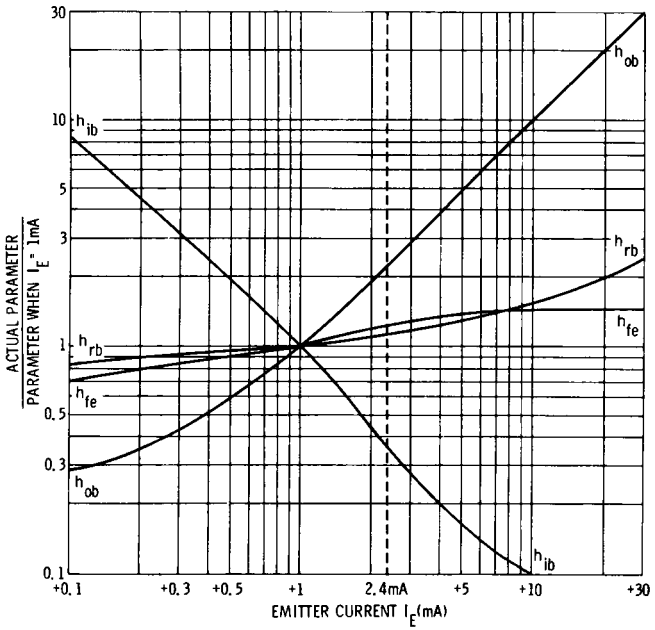


Fig. 5-11. Variation of h-parameters with emitter current.

This information will now allow us to correct the h-parameters for the quiescent collector-emitter voltage and emitter current in this circuit. Graphs or curves are frequently provided by transistor manufacturers to show how the h-parameters vary with I_C (or I_E) and V_{CE}. Use Figs. 5-11 and 5-12 to represent these characteristics for the transistor in this example.

In Fig. 5-11, the emitter current is plotted on the horizontal axis. The ratio of the h-parameters at the actual quiescent emitter current to the h-parameters for 1 mA emitter current, are shown on the vertical axis. The curves describe how the ratios change for different values of emitter current.

Mark the actual emitter current, 2.4 mA, on the horizontal axis, and draw a vertical line from this axis through the various curves. The ratio of the various h-parameters for the actual operating condition when $I_E = 2.4$ mA, to the h-parameter when $I_E = 1$ mA, are as follows:

For h_{ib} the ratio is 0.37:1. It is 1.2:1 for h_{rb}, 1.3:1 for h_{fe}, and 2.2:1 for h_{ob}. These are the emitter current correction factors.

The V_{CE} correction curves are drawn in Fig. 5-12. The collector-to-emitter voltage is shown along the horizontal axis. The ratio of the h-parameters at the actual quiescent V_{CE} to the h-parameters for 5 volts, are shown along the vertical axis. The curves are a plot of the changes in this ratio with the variation in V_{CE}.

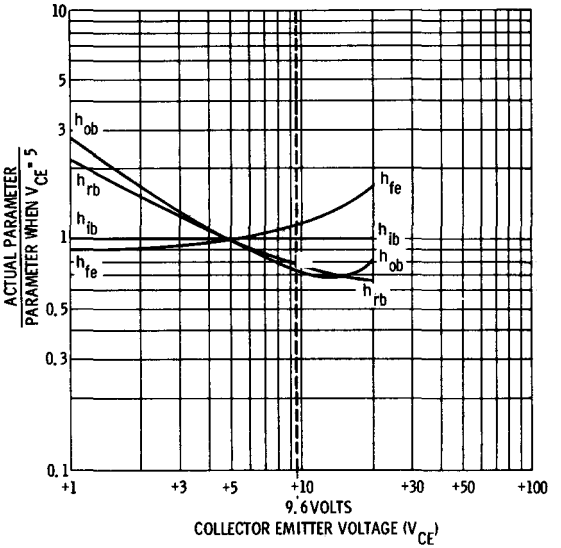


Fig. 5-12. Variation of h-parameters with collector-emitter voltage.

Mark the actual V_{CE}, 9.6 volts, on the horizontal axis. Draw a vertical line from this point. The correction factors for the various h-parameters due to this V_{CE} are as follows:

The ratio for h_{ib} is 1:1. It is 0.79:1 for h_{rb}, 1.2:1 for h_{fe} and 0.72:1 for h_{ob}.

The corrected parameters are equal to the particular parameter value at $I_E = 1$ mA and $V_{CE} = 5$ volts, multiplied by both correction factors just determined. The corrected parameters for $V_{CE} = 9.6$ volts and $I_E = 2.4$ mA, are:

$$h_{ib} = 35 \times 0.37 \times 1 = 13 \text{ ohms}$$
$$h_{rb} = 10^{-3} \times 1.2 \times 0.79 = 9.5 \times 10^{-4}$$
$$h_{ob} = 10^{-6} \times 2.2 \times 0.72 = 1.58 \times 10^{-6}$$
$$h_{fe} = 50 \times 1.3 \times 1.2 = 78; \; h_{fb} = -(78)/(78 + 1) = -0.987.$$

We can now use these corrected factors to determine the equivalent "T" parameters. From Equation 5-5:

$$r_e = 13 - \frac{9.5 \times 10^{-4}}{1.58 \times 10^{-6}\,(78+1)} = 5.4 \text{ ohms}$$

From Equation 5-6:

$$r_b = \frac{9.5 \times 10^{-4}}{1.58 \times 10^{-6}} = 600 \text{ ohms}$$

From Equation 5-10:

$$\beta = h_{fe} = 78$$

And from Equation 5-8:

$$r_d = \frac{1}{h_{ob}h_{fe}} = \frac{1}{(1.58 \times 10^{-6})\,(78)} = 8.1 \times 10^3 \text{ ohms}$$

Substituting this information into Equations 5-11 through 5-14, the impedances and gain of the device are:

$$R_{in} = 600 + 78(400 + 5.4) = 32.2 \times 10^3 \text{ ohms}$$

$$R_{out} = \frac{8.1 \times 10^3[(2000 + 600) + (5.4 + 400)78]}{2000 + 600 + 5.4 + 400} = 92.3 \times 10^3 \text{ ohms.}$$

$$A_v = \frac{78(4000)}{78(5.4 + 400) + 600} = 9.7$$

$$A_i = 78$$

We have just completed two solutions to the same problem. The first, very approximate, was only from fast observations of the circuit and the components in the circuit. The second was a reasonably accurate mathematical derivation using the formulas as well as the correction factors for the h-parameters.

The voltage gain, by the first approximation, was 10. This approximation is the ratio of the load resistor to the emitter resistor. More accuracy could be achieved if we added the transistor emitter resistance, ($r_e = 26/I_E \approx 26/2.37 = 11$ ohms) to the resistor in the emitter. The total resistance in the emitter circuit is then 400 ohms + 11 ohms = 411 ohms. The voltage gain from the ratio of the load resistor to this resistor combination is $4000/411 = 9.7$. This is identical to the gain when calculated using the more accurate methods.

(It is interesting to note that r_e determined here is 11 ohms, while when determined from the more accurate equation, it is 5.4 ohms.)

The approximate current gain is β, which does not vary much over the useful working range of small signal transistors. Hence, we assumed it to be 50, a figure stated in the original data. After correction factors were added, it was proven to be 78.

The input impedance was estimated at 20,000 ohms by considering only the 400-ohm resistor in the emitter. The more accurate calculated value was 32,200 ohms. The original input impedance estimation can be made more accurate by not ignoring r_e.

The output impedance from our calculation is 92,300 ohms. We estimated that it must be between 20,000 ohms and 1 megohm.

It must be noted that all the information determined thus far is more concerned with the performance of the transistor in the circuit than the complete circuit. The characteristics of the complete circuit will now be determined. First, let us determine the input impedance of the circuit as seen by the 0.2-volt source.

From the calculations, the input impedance of the transistor itself was found to be 32,200 ohms. The 400,000-ohm bias resistor shunts the base circuit to ac ground. (This resistor is from base to the 20-volt supply, which is at ac ground.) Hence, it is in parallel with the 32,200-ohm resistance. The equivalent input resistance of the parallel combination is $(400{,}000 \times 32{,}200)/(400{,}000 + 32{,}200) = 29{,}600$ ohms.

The voltage at the base of the transistor using the voltage divider equation is $(29{,}600/29{,}600 + 2000)\ 0.2 = 0.187$ volt. The voltage gain of the transistor itself has been calculated at 9.7. Hence, the output voltage will be $9.7 \times 0.187 = 1.82$ volts. The overall voltage gain of the circuit is $1.82/0.2 = 9.1$ volts.

The output impedance is the load resistor in parallel with the resistance of the device. This latter resistance has been calculated at 92,300 ohms. The output impedance offered by the transistor circuit is $(92{,}300 \times 4000)/(92{,}300 + 4000) = 3840$ ohms. The earlier estimated value of the output impedance (not including the effect of the 4000 ohm load resistor) was between 20,000 ohms and 1 megohm. When shunted by the 4000-ohm resistor, the estimated resistance looking back into the collector circuit of the transistor is between $(20{,}000 \times 4000)/(20{,}000 + 4000) = 3300$ ohms, and $(1{,}000{,}000 \times 4000)/(1{,}000{,}0000 + 4000) = 3980$ ohms. Neither value is excessively far from the calculated 3840 ohms; the worst error is 14.1%. We are reasonably safe in assuming that the load resistor, R_L is the impedance seen by a circuit when looking back into the transistor. The large latitude assumed in estimating the collector impedance is unimportant.

The total current delivered by the 0.2-volt, 2000-ohm source is equal to the source voltage divided by the sum of the source resistance, 2000 ohms and the input impedance of the transistor circuit. This is $(0.2 \text{ volts})/(2000 + 29{,}600) = 6.32 \times 10^{-6}$ amps. This current is divided between the base resistor, 400,000 ohms, and the transistor input resistance, 32,200 ohms. Using current divider equations, the base current is 6.32×10^{-6} $(400{,}000)/(400{,}000 + 32{,}200) = 5.85 \times 10^{-6}$ amps. The output current is β times this or $46.7 \times (5.85 \times 10^{-6}) = 0.457 \times 10^{-3}$ amps. The overall current gain of the circuit is $(0.457 \times 10^{-3})/(6.32 \times 10^{-6}) = 72$.

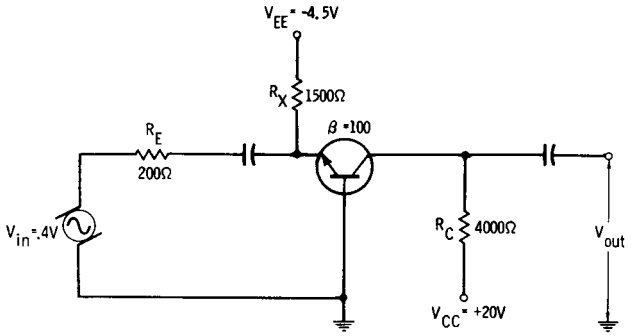


Fig. 5-13. Circuit for problem 3.

Problem 3—Calculate the vital statistics for Fig. 5-13. Use the minimum number of equations possible.

$$I_E = \frac{V_{EE}}{R_X} = \frac{4.5}{1500} = 3 \text{ mA} \approx I_C$$

$$V_{CE} = V_{CC} - I_c R_c = 20 - I_C(4000) = 8 \text{ volts}$$

$$A_v = \frac{R_C}{R_E} = \frac{4000}{200} = 20$$

$$V_{out} = A_v V_{in} = 20(0.4) = 8 \text{ volts}$$

$$A_i = \alpha = \frac{\beta}{\beta + 1} = \frac{100}{101} \approx 1$$

$$r_e = \frac{26}{I_E} = \frac{26}{3} = 8.66 \text{ ohms}$$

$$R_{in} = R_E + r_e + \frac{r_b + R_B}{\beta} \approx R_E + r_e = 208.66 \text{ ohms}$$

(The impedance of the 1500-ohm emitter resistor is negligible compared to all other resistance in the circuit.)

R_{out} is approximately equal to r_c in parallel with 4000 ohms. It is thus approximately equal to 4000 ohms.

Problem 4—Calculate the vital statistics for Fig. 5-14. Assume that all capacitors are short circuits for the ac signal.

I_B can be found using the Thevenin equivalent of the bias circuit. The Thevenin voltage is:

$$\left(\frac{220 \text{ k}\Omega}{1.5 \text{ M}\Omega + 220 \text{ k}\Omega}\right) 30 = 3.85 \text{ volts}$$

The Thevenin resistance is:

$$\frac{(1.5 \text{ M}\Omega)(220 \text{ k}\Omega)}{(1.5 \text{ M}\Omega + 220 \text{ k}\Omega)} = 192{,}000 \text{ ohms}$$

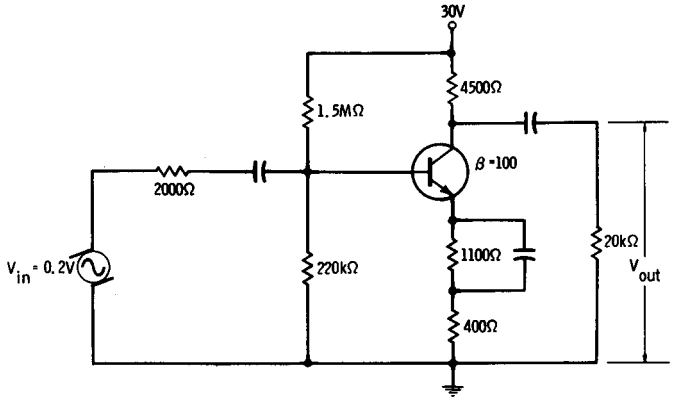


Fig. 5-14. Circuit for problem 4.

The dc base-emitter circuit, with the Thevenin equivalent of the bias circuit is drawn in Fig. 5-15A. The total resistance in the circuit is 192 $k\Omega + \beta(1100 + 400) = 192\,k\Omega + 100\ (1500\,\Omega) = 342{,}000$ ohms.

$$I_B = \frac{3.85 \text{ volts}}{342{,}000\Omega} = 1.12 \times 10^{-5} \text{ amps}$$

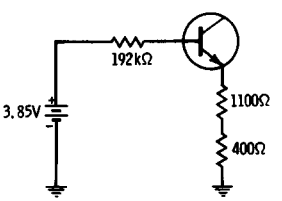
$$I_C = \beta I_B = 100(1.12 \times 10^{-5}) = 1.12 \times 10^{-3} \text{ amps} \approx I_E$$

$$V_{CE} = 30 - (4500 + 1100 + 400)\,1.12 \times 10^{-3} = 23.3 \text{ volts.}$$

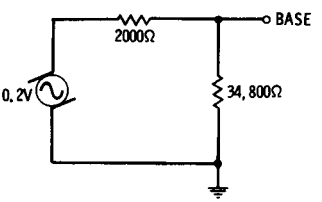
$$r_e = 26/1.12 = 23 \text{ ohms}$$

Having completed our analysis of the dc operating conditions, we can now turn to the ac portion of the circuit. As the 1100-ohm resistor in the cathode is shorted by a capacitor, the ac input resistance, R_{in}, of the transistor is $\beta(23 + 400) = 42{,}300$ ohms.

The ac load at the output is the 4500-ohm resistor in parallel with the 20,000-ohm output resistor. The equivalent resistance of these two components is 3670 ohms. It is also the output impedance of the circuit when looking toward the 20,000-ohm resistor. The 20,000-ohm resistor, how-



(A) Dc base circuit in Fig. 5-14.



(B) Ac base circuit in Fig. 5-14.

Fig. 5-15. The dc and ac base circuits in Fig. 5-14.

ever, sees a 4500-ohm load impedance when looking toward the collector circuit of the transistor.

A_v of the transistor itself is $Z_{out}/(R_E + r_e) = 3670/423 = 8.7$.

The voltage source sees a transistor input, R_{in} in parallel with the 220,000-ohm resistor. The combination is in parallel with the 1,500,000-ohm resistor. After the necessary calculations, the resistance seen by the voltage source is found to be 34,800 ohms. The circuit of the input resistance with the voltage source is shown in Fig. 5-15B. Using the voltage divider equation, the voltage at the base is 0.189 volt. This, multiplied by the ac voltage gain, is the ac output voltage: $V_{out} = 0.189(8.7) = 1.64$ volts. The overall voltage gain is $1.64/0.2 = 8.2$.

The overall current gain is the ratio of the ac current at the output to that provided by the 0.2-volt generator. The input current is 0.2 volt/$(2000\,\Omega + 34{,}800\,\Omega) = 5.44 \times 10^{-6}$ amps. The ac current at the output is 1.64 volts/$3670\Omega = 4.46 \times 10^{-4}$ amps. The ratio of the latter to the former, the overall ac current gain, is $4.46 \times 10^{-4}/5.44 \times 10^{-6} = 82$. It must be less than β.

Problem 5—Accumulate the vital statistics on Fig. 5-16. $\beta = 100$.

$$I_B = \frac{30}{10^6 + \beta(5000)} = \frac{30}{1.5 \times 10^6} = 2 \times 10^{-5} \text{ amps}$$

$$I_E = I_C = \beta I_B = 2 \times 10^{-3} \text{ amps}$$

$$V_{CE} = 30 - (2 \times 10^{-3})(5 \times 10^3) = 20 \text{ volts.}$$

$R_{in} = \beta(5000)$ in parallel with the 1-megohm resistor. It is $(1\,M\Omega)(500\,k\Omega)/(1\,M\Omega + 500\,k\Omega) = 330\,k\Omega$.

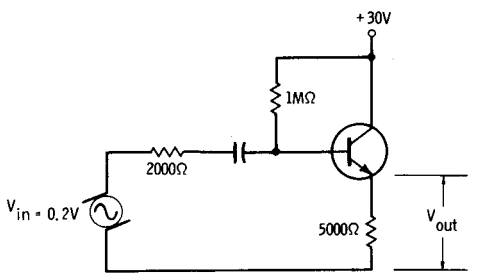


Fig. 5-16. Circuit used for solving problem 5.

R_{out} equals 5000 ohms in parallel with the sum of the resistance in the base circuit divided by β and r_e. The resistance in the base circuit is 1 megohm in parallel with the 2000-ohm source resistor or, effectively, 2000 ohms: $2000\,\Omega/\beta = 20\,\Omega$, and $r_e = 26/I_E = 13\,\Omega$. The total resistance in parallel with the 5000-ohm emitter resistor is $20\,\Omega + 13\Omega = 33$ ohms. The output impedance is thus very close to 33 ohms.

The ac voltage at the base can be determined from the circuit in Fig. 5-17. It is, through the voltage divider equation, equal to 0.199 volt. This is effectively the same voltage that is across the 5000-ohm resistor at the output.

The current supplied by the ac input is 0.2 volt/(330,000 + 2000) = 6.02×10^{-7} amps. This current is divided between the 1-megohm resistor and the base input resistance of $\beta \times 5000$ ohms or 500,000 ohms. The current entering the base is $1\,M\Omega(6.02 \times 10^{-7})/(1\,M\Omega + 500\,k\Omega) = 4.02 \times 10^{-7}$ amps. The current through the emitter is 0.199 volt/5000 ohms = 3.99×10^{-5} amperes. The current gain of the transistor is $(3.99 \times 10^{-5})/(4.02 \times 10^{-7}) \approx 100$ or β. The current gain of the circuit is $(3.99 \times 10^{-5})/(6.02 \times 10^{-7}) = 66$. The voltage gain is about 1. The product of this and the current gain is the power gain, which is nearly equal to the current gain.

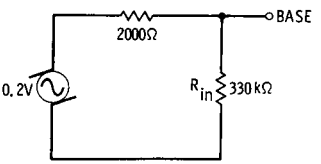


Fig. 5-17. Ac input circuit for Fig. 5-16.

NOISE

Small signal amplifiers are plagued by noise induced from environmental sources, by noise generated by the circuit components at the input to a transistor, and by noise from the transistor itself. Signal-to-noise ratios, stated in terms of voltage or power, are measurements of the relative amount of signal overriding the noise. When measured across the same or equal loads, the ratio can be expressed in decibel units:

$$dB = 10 \log_{10} \frac{P_{so}}{P_{no}} = 20 \log_{10} \frac{v_{so}}{v_{no}} \qquad (5\text{-}34)$$

where,

P_{so} is the signal power at the output of an amplifier,
P_{no} is the noise power at the output of an amplifier,
v_{so} is the signal voltage across a load, R_L, at the output of an amplifier,
v_{no} is the noise voltage across the same or equal value load R_L, at the output of an amplifier.

A chart relating dB to the voltage ratio is shown in Table 8-1.

Here, the discussion will center on the noise generated by the transistor and its associated circuits. Noise varies with bandwidth and with the audio frequencies involved. The noise at the output of a transistor circuit can be divided into three frequencies categories: 1. One type, known as *white noise,* covers the entire frequency spectrum. Here equal noise power

is present at all frequencies. This noise can be due to thermal phenomenon in the components, to *shot noise* generated by the random motion of charge in the semiconductor, and to *partition noise* because of emitter current division between the base and collector. 2. From zero Hz to a frequency f_1 (anywhere between 100 and 1000 Hz, depending upon the transistor), a semiconductor noise due to leakage and surface phenomena, is added to the white noise. It rolls off at the rate of 3dB per octave above zero Hz. This is referred to as the 1/f noise. 3. From a frequency f_2 in the high audio or low radio frequencies, on up to the limits of the circuit, there is an increase in noise with frequency at the rate of 6 dB per octave. This is not due to any particular source, but rather due to roll-off of transistor beta at the high frequencies.

The manufacturer of the bipolar transistor indicates the quality of a device using the *noise factor* ratio, F, or the *noise figure* ratio, NF. These are defined by the Equations 5-35 and 5-36, respectively.

$$F = \frac{P_{si}/P_{ni}}{P_{so}/P_{no}} = \frac{P_{no}}{GP_{ni}} = \frac{GP_{nit}}{GP_{ni}} \qquad (5\text{-}35)^*$$

$$NF = \log_{10} F \qquad (5\text{-}36)^*$$

where,

P_{si} is the signal power at the input,
P_{ni} is the noise power at the input and generated by the circuit components at the input,
P_{nit} is the total noise power at the input due to all sources,
G is the power gain of the transistor,
P_{so} and P_{no} were defined earlier.

Noise figure can be specified to consider noise over the entire band, or for 1-Hz bandwidth at 1 kHz (spot noise). The former figure, when specified, is the more exact indication of the quality of the device. Lower noise figures indicate that under proper loading conditions, the particular device will deliver less noise to the output than will be delivered by devices with higher noise figures.

The transistor circuit can be analyzed by separating the gain portion of the device from the noise generating sources. The generating sources, whether real or hypothetical, are then placed at the input of the noiseless amplifying device. The noise at the output due to all these sources and the gain portion, should be the same as the noise due to the actual transistor in the physical circuit.

There are three noise generating sources to be placed at the input to the noiseless equivalent amplifier: 1. A real noise voltage, v_{ni}, generated by the components at the input and transferred to the transistor; 2. A hypothetical noise voltage generator, v_n, representing noise voltage due to the transistor: 3. A hypothetical current noise generator, i_n, is also due to transistor noise. Let us pause to discuss the three noise sources.

Real Noise Generator v_{ni}

Assuming that the gain of an amplifier rolls off at the rate of 6 dB per octave at each end of the passband, a resistor at the input generates noise power equal to:

$$P_{ni} = 2.15 \times 10^{-23}(273° + °C)(f_H - f_L) \qquad (5\text{-}37)$$

where,

°C is the temperature of the resistor in degrees Celsius,
f_H is the upper frequency at which the gain of the amplifier has dropped 3 dB from its gain at the center frequency,
f_L is the lower frequency at which the gain of the amplifier has dropped 3 dB from its gain at the center frequency.

The maximum noise power will be transferred from the resistor to the circuit (available noise power) when the sizes of the noise generating resistor, R_G, and the resistance at the input to the circuit, R_{NI}, are equal. In this case, the voltage across either resistor is $v_{ni}/2$. The power at the input due to v_{ni} is thus $P_{ni} = (v_{ni}/2)^2/R_G = v_{ni}^2/4R_G$. It follows that:

$$v_{ni}^2 = 8.6 \times 10^{-23}(273° + °C)(f_H - f_L)R_G \qquad (5\text{-}38)$$

Should a capacitor, C_t, such as that due to a ceramic phonograph cartridge, shunt the input to the circuit, Equation 5-38 becomes:

$$v_{ni}^2 = 2.15 \times 10^{-24}(273° + °C)\left(\frac{f_H - f_L}{f_H f_L}\right)\left(\frac{1}{R_G C_t^2}\right) \qquad (5\text{-}39)$$

Hypothetical Noise Generators

A circuit involving hypothetical noise current and voltage generators at the input to the noiseless amplifier, is shown in Fig. 5-18. The noise at the output is due to $\bar{v}_n$ when the input to the amplifier is shorted. It is due to $\bar{i}_n$ when the input is open circuited. $\bar{v}_n$ generates a noise power at the input equal to $\bar{v}_n^2/4R_G$ while the noise power due to $\bar{i}_n$ is $\bar{i}_n^2 R_G/4$.

Total Noise

Combining equations 5-35, 5-37 and the $\bar{v}_n$ and $\bar{i}_n$ relationships, the noise factor is:

$$F = \frac{GP_{nit}}{GP_{ni}} = \frac{G(P_{ni} + \bar{v}_n^2/4R_G + \bar{i}_n^2 R_G/4)}{GP_{ni}}$$

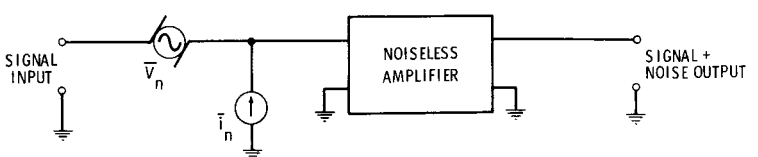


Fig. 5-18. Circuit with input signal and hypothetical noise generators.

which can be simplified to:

$$F = 1 + \frac{\bar{v}_n^2/R_G + \bar{i}_n^2 R_G}{8.6 \times 10^{-23}(273° + °C)(f_H - f_L)} \qquad (5\text{-}40)$$

and that it is at a minimum when $R_G = \bar{v}_n/\bar{i}_n$.
Using the equation, it can be shown that the minimum noise factor is:

$$F = 1 + \bar{v}_n\bar{i}_n/4.3 \times 10^{-23}(273° + °C)(f_H - f_L)$$

Using Equations 5-35 and 5-40, it can be shown that the total noise power at the input of the noiseless transistor is $P_{nit} = FP_{ni} = \bar{v}_{nit}^2/4R_G$, where $\bar{v}_{nit}$ is the total (real and hypothetical) noise voltage at the input. Solving for $\bar{v}_{nit}$, the total input noise voltage is:

$$\bar{v}_{nit} = [4FR_G(2.15 \times 10^{-23})(273° + °C)(f_H - f_L)]^{1/2} \qquad (5\text{-}41)$$

The ratio of the input signal, v_{si}, to $\bar{v}_{nit}$ of Equation 5-41, is the signal-to-noise ratio of the amplifier. It can be expressed in dB using the equation:

$$dB = 20 \log_{10} \frac{v_{si}}{\bar{v}_{nit}} \qquad (5\text{-}42)$$

Actual numbers should be plugged into Equations 5-41 and 5-42 to determine if the signal to noise ratio of an amplifier is satisfactory.

Chapter 6

LOW-FREQUENCY LARGE-SIGNAL AMPLIFIERS

In the previous chapter, small-signal equivalent circuits were presented and calculations were made using parameters based on these approximations. Many of the calculations can be performed without fully understanding the operation of the circuit.

This chapter describes large-signal amplifiers. Nebulous formulas cannot be applied to these circuits. The information presented here is probably the most significant in the design procedures. The insight gained from dealing with large-signal devices should help clarify previously acquired vague concepts.

Two groups of information are presented in this chapter: 1. The application of the transistor to power amplifiers; 2. Limitations of the transistor, thermal considerations and the determination of heat sink requirements.

CLASS-A AMPLIFIERS

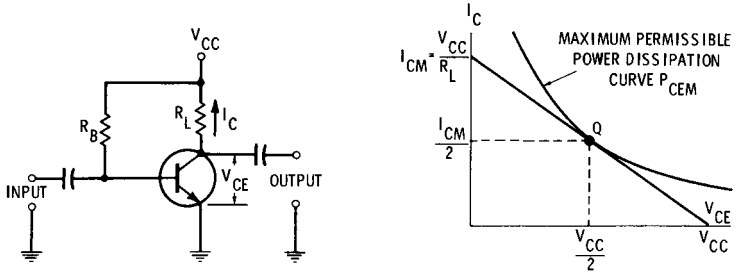
Class-A amplifiers are devices in which there is always collector current regardless of the time in the cycle of the applied signal. This type of amplifier was discussed under small-signal devices.

A typical class-A amplifier is shown in Fig. 6-1A. The maximum power limitations and the load line are shown in Fig. 6-1B.

A transistor is capable of dissipating a specific maximum amount of power, P_{CEM}, under a particular set of conditions. Power, as always, is the product of the current through a device and the voltage across it. Should a transistor be capable of dissipating a maximum of P_{CEM} watts, the product of V_{CE} and I_C must never exceed P_{CEM}. A hyperbolic curve plotting all points where $V_{CE} \times I_C = P_{CEM}$ can be drawn on the set of collector characteristic curves, as shown in Fig. 6-1B. (The actual base current curves have been omitted so that the drawing will not be cluttered.) If the tran-

sistor is to operate within its power rating, the load line of the circuit must be below the P_{CEM} curve and must never cross it. This statement will be modified in the discussion of class-B and class-AB power amplifiers.

In Fig. 6-1B, a load line that barely touches the hyperbola has been drawn through procedures outlined in previous chapters. It connects a point equal to the supply voltage, V_{CC}, on the horizontal axis with a point equal to the collector current, $I_{CM} = V_{CC}/R_L$, on the vertical axis. Any



(A) Class-A amplifier. (B) Maximum power curve.

Fig. 6-1. Class-A amplifier and curve.

load line that touches the hyperbola at one point, regardless of the size of R_L or V_{CC}, must touch the P_{CEM} hyperbola at $V_{CC}/2$ and $I_{CM}/2$. Since the load line does not touch the hyperbola at any other point, the maximum power, P_{diss} (max), is dissipated by the transistor when the voltage at the collector is $V_{CC}/2$ and the collector current is $I_{CM}/2$.

$$P_{diss}\,(\text{max}) = \frac{V_{CC}}{2} \times \frac{I_{CM}}{2} = \frac{V_{CC}I_{CM}}{4} \qquad (6\text{-}1)$$

since the load resistance is $R_L = V_{CC}/I_{CM}$:

$$P_{diss}\,(\text{max}) = \frac{V_{CC}^2}{4R_L} = \frac{I_{CM}^2 R_L}{4} \qquad (6\text{-}1\text{A})^*$$

P_{diss} (max) is equal to P_{CEM} when the load line is tangent to the maximum power dissipation hyperbola.

Now, let us assume that a sine wave has been fed to the amplifier. The construction in Fig. 6-2 shows the collector characteristics of a hypothetical transistor, the load line, and the effect of feeding a sine wave to the base of the transistor. The quiescent base current is set at I_{B4}. The sine wave swings the base current from I_{B1} to I_{B7} around I_{B4}. The collector current and voltage change during the cycle with the base current. These factors are tied to the load line.

As an example, at the instant the input signal swings the base current to I_{B6}, the collector current is an I_{C6} because the load line and I_{B6} intersect at this collector current. If a vertical line were extended from this point of

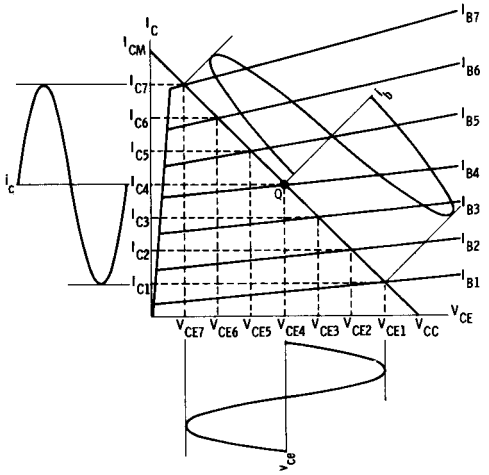


Fig. 6-2. Class-A output characteristics.

intersection, we find it would intersect the V_{CE} axis at V_{CE6}. This is the voltage between the emitter and collector, across the transistor, when $I_B = I_{B6}$. The difference between this and the supply voltage is across the load.

Suppose that the input current is at the instant in the cycle when the base current is I_{B2}. Draw a horizontal and a vertical line from the point at which I_{B2} and the load line intersect. The collector current, read on the vertical axis, is I_{C2}. The emitter-collector voltage across the transistor, read on the horizontal axis, is V_{CE2}. $V_{CC} - V_{CE2}$ is the voltage across the load at this moment.

As the sine wave swings the base current from I_{B4} to I_{B7}, it swings the collector and load current from I_{C4} to I_{C7}. (I_{C7} is about equal to I_{CM}). At the same time, the voltage across the transistor swings from V_{CE4} to V_{CE7}. (V_{CE7} is essentially zero.) The voltage across the load swings from $V_{CC} - V_{CE4}$ to $V_{CC} - V_{CE7}$. ($V_{CC} - V_{CE7}$ is about equal to V_{CC}.)

Similarly, when the sine wave goes from I_{B4} to I_{B1}, the collector and load current swing from I_{C4} to I_{C1} (I_{C1} is about equal to zero) and the collector-emitter voltage swings from V_{CE4} to V_{CE1}. (V_{CE1} is about equal to V_{CC}.) The voltage across the load resistor swings from $V_{CC} - V_{CE4}$ to $V_{CC} - V_{CE1}$. Since V_{CE1} is about equal to V_{CC}, $V_{CC} - V_{CE1}$ is very close to zero.

The overall base current swing is from I_{B1} to I_{B7}. During this excursion, the approximate swing of the collector and load current is from zero to I_{CM}. When the collector current is zero, there is no voltage drop across the load resistor and the entire supply voltage is across the transistor. The voltage across the transistor swings from V_{CC} to zero as the collector current swings from zero to I_{CM}. The voltage across the load swings from zero to V_{CC} as the load or collector current swings from zero to I_{CM}.

The peak-to-peak current swing through the load cannot exceed I_{CM}. The rms value of a sine wave is the peak current divided by $\sqrt{2}$. Since the peak current of a sine wave is half the peak-to-peak swing, or $I_{CM}/2$, the rms current is $I_{CM}/2\sqrt{2}$.

Similarily, the rms voltage is $V_{CC}/2\sqrt{2}$.

The power delivered to the load is the rms voltage multiplied by the rms current, or:

$$P_{R_L} = \frac{V_{CC}}{2\sqrt{2}} \times \frac{I_{CM}}{2\sqrt{2}} = \frac{V_{CC}I_{CM}}{8} = \frac{V_{CC}^2}{8R_L} = \frac{I_{CM}^2R_L}{8} \qquad (6\text{-}2)^*$$

This is the maximum power the transistor can deliver using the circuit in Fig. 6-1A.

Compare Equations 6-2 and 6-1A. The maximum power this circuit is capable of delivering to the load is equal to half the maximum power the transistor may dissipate.

Assume that there is no distortion. The output signal is perfectly symmetrical about the quiscent collector current, I_{C4}, and the quiescent collector-emitter voltage, V_{CE4}. Then $I_{C4} = I_{CM}/2$ and $V_{CE4} = V_{CC}/2$. These are the average values of the dc voltage and current through the circuit.

The power demanded from the power supply consists of the sum of the power dissipated by the transistor, the power dissipated by the load, and the power supplied to the base bias circuit. Compared to the first two, the last factor is negligible. Using only the first two items, the total input power delivered by the supply is:

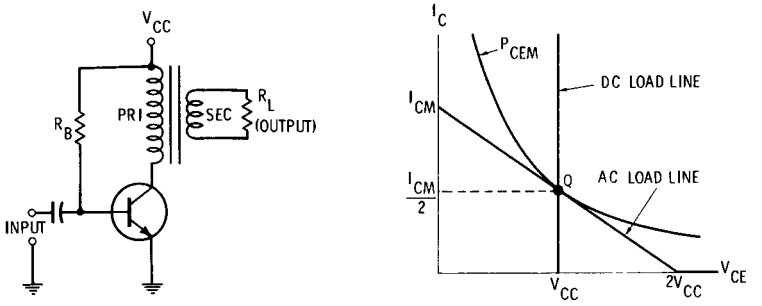
$$P_{CC} = \left(\frac{I_{CM}}{2}\right)\left(\frac{V_{CC}}{2}\right) + \left(\frac{I_{CM}}{2}\right)^2 R_L = \frac{I_{CM}^2R_L}{2} = \frac{V_{CC}^2}{2R_L} \qquad (6\text{-}3)$$

The efficiency of the circuit is the ratio of the ac power that can be delivered by the circuit to the amount of power that must be supplied by the power source. When multiplied by 100, efficiency is expressed as a percentage:

$$\%\ \text{eff.} = 100\left(\frac{P_{R_L}}{P_{CC}}\right) = \left(\frac{V_{CC}^2/8R_L}{V_{CC}^2/2R_L}\right) 100 = 25\% \qquad (6\text{-}4)$$

The maximum efficiency of this circuit is 25 percent. It can be improved if the power dissipated by the load were reduced. In Equation 6-3, it would be desirable to eliminate the $(I_{CM}/2)^2R_L$ term. This power is dissipated in the load resistor and contributes nothing to the output. The load resistor can be replaced by a transformer. A circuit of this type is shown in Fig. 6-3A.

A transformer has N_1 turns in the primary magnetically coupled to the N_2 turns in the secondary. If a voltage, V_1, is placed across the primary, a



(A) Transformer-coupled circuit. (B) Ac and dc load lines.

Fig. 6-3. Transformer-coupled circuits and load lines.

voltage, V_2, will appear across the secondary. Ignoring all transformer losses, the voltage and turns ratios are related by the equation:

$$V_1/V_2 = N_1/N_2 \tag{6-5}$$

Similarly, if there is a current, I_1, through the primary, there will be a current, I_2, through the secondary. They are related by the equation:

$$I_2/I_1 = N_1/N_2 \tag{6-6}$$

Multiplying Equation 6-5 by Equation 6-6:

$$\frac{V_1 I_2}{V_2 I_1} = \frac{N_1^2}{N_2^2} = \left(\frac{V_1}{I_1}\right)\left(\frac{I_2}{V_2}\right) = \frac{R_L'}{R_L} = \frac{N_1^2}{N_2^2}$$

or,

$$R_L' = (N_1/N_2)^2 R_L \tag{6-7}*$$

Equation 6-7 states that a resistor load in the secondary, R_L, appears as a resistance, R_L', reflected into the primary. R_L' is equal to R_L multiplied by the square of the turns ratio of the transformer.

Put this perfect transformer into the collector circuit of a transistor as shown in Fig. 6-3A.

The transformer, assumed perfect, has zero dc resistance. As a consequence, the dc load line is vertical from V_{CC} on the horizontal axis. This load line is drawn in the usual fashion in Fig. 6-3B. One point on the load line is at $I_C = 0$ and $V_{CE} = V_{CC}$. The other point is at $V_{CE} = 0$, $I_C = V_{CE}/R_p$. (R_p is neither the resistor R_L nor R_B shown in Fig. 6-3A. It is the dc resistance of the primary winding of the transformer—the actual dc resistance through which there is collector current.) Since R_p here equals 0, I_C is ∞. This determines a second point on the load line: $V_{CE} = 0$, $I_C = \infty$. For all practical considerations, the line extends straight up and parallel to the collector current axis. Normally, there is some resistance in the transformer winding and the second point on the dc load line is finite.

The quiescent conditions are determined from the dc portion of the circuit, which has nothing to do with the ac load. The quiescent collector voltage is V_{CC}, as there is no voltage drop across the perfect transformer. The quiescent collector current is on the load line at Q. Q must not be above the hyperbolic curve that describes the transistor power dissipation limits. The maximum power can be delivered to the load when Q is at the intersection of the dc load line and the P_{CEM} curve.

The ac load line is dependent on all the impedance in the primary of the transformer. If a perfect transformer is used, it is R_L', determined from Equation 6-7.

The ac load line can be drawn on the curve, as follows. Refer to Fig. 6-4 in which the dc load line is not perfectly vertical. It is assumed that there is a dc resistance in the primary winding of the transformer.

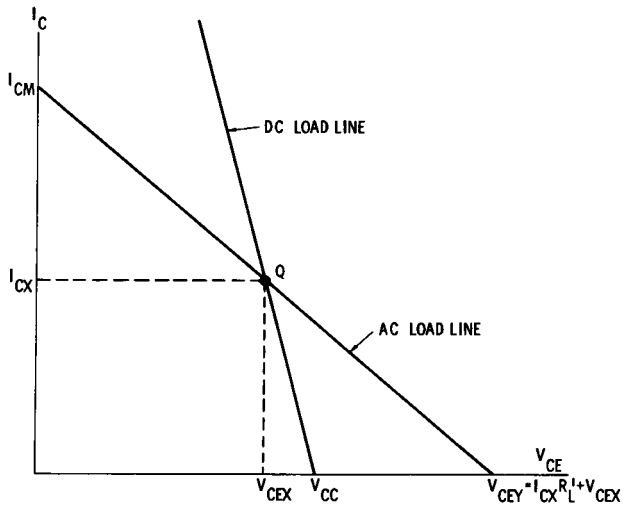


Fig. 6-4. Method for plotting ac load line.

1. Draw a dc load line using methods previously employed by connecting V_{CC} on the V_{CE} axis to V_C /R_{dc} on the I_C axis. R_{dc} is the sum of dc resistors in the collector circuit of the transistor.
2. Select a quiescent point on the dc load line and mark the point Q. It may be the point marked in Fig. 6-3, or any other point below the P_{CEM} curve.
3. Draw a vertical line from Q to the horizontal axis. In Fig. 6-3, where zero dc winding resistance is assumed, the vertical line is coincident with the dc load line. It intersects the horizontal axis at V_{CC}. In Fig. 6-4, it intersects the voltage axis at V_{CEX}.
4. Determine the resistance reflected from the secondary of the trans-

former into the primary winding. Through Equation 6-7, the reflected resistance, R_L' is: $R_L' = (N_1/N_2)^2 R_L$. R_L is the resistor load on the secondary winding.

5. Draw an ac load line, as shown. Here, $V_{CEY} - V_{CEX} = I_{CX}R_L'$. Plot the point $V_{CEY} = I_{CX}R_L' + V_{CEX}$ on the horizontal axis. Connect the Q point to V_{CEY} point and extend the line to the vertical axis. This is the ac load line. For this load resistor, all ac load lines will be parallel to the one just drawn, as they pass through other Q points. All Q points should be below the P_{CEM} hyperbola.

Several practical aspects should be noted in the design of this circuit. First, the dc load line in Fig. 6-4 is drawn in the usual way. One point must be V_{CC}. If the second point is too high on the vertical axis, falling off the graph, it may be calculated for another value of V_{CE}. For example, if V_{CE} is V_{CEX}, the dc collector current at this point is $I_{CX} = (V_{CC} - V_{CEX})/R_{dc}$, where R_{dc} is the sum of all the dc resistance in the collector circuit.

Next, the ac load line must pass through the Q point, which is on the dc load line. The Q point should be chosen so that the ac load line does not cross the peak power dissipation curve at any time. Should the Q point be changed, the new load line will be parallel to the original one because the load resistance is a constant. Regardless of the Q point, all load lines will be parallel to each other.

As a third factor, the ac load resistance is not merely the reflected resistance, R_L'; it is equal to the sum of the reflected resistance, the dc resistance of the primary winding of the transformer, and any other resistance in the collector and emitter leads of the transistor. Furthermore, the secondary winding of the transformer has been assumed to lack resistance. This is not absolutely true. The ac reflected resistance from the secondary winding is not due merely to R_L, but is due to the sum of R_L and the resistance of the secondary winding of the transformer.

Finally, the ac output travels up and down the ac load line just as it traveled along the dc load line in Fig. 6-2. If the output signal from the transistor is to be symmetrical, the voltage and current must swing equal amounts on either side of the quiescent value. The ac load line is usually chosen so that the one point is on the horizontal axis where $V_{CE} = 2V_{CC}$ with reference to Fig. 6-3 and at $V_{CEY} = 2V_{CEX}$ with reference to Fig. 6-4.

Referring to Fig. 6-3, the maximum possible voltage swing is $2V_{CC}$ and the maximum current swing is I_{CM}. The power delivered to the load is:

$$P_{R_L} = \left(\frac{2V_{CC}}{2\sqrt{2}}\right)\left(\frac{I_{CM}}{2\sqrt{2}}\right) = \frac{V_{CC}I_{CM}}{4} = \frac{V_{CC}^2}{4R_L'} = \frac{I_{CM}^2 R_L'}{4} \qquad (6\text{-}8)^*$$

while the average dc power dissipated by the transistor, or the power dissipated at the Q-point is:

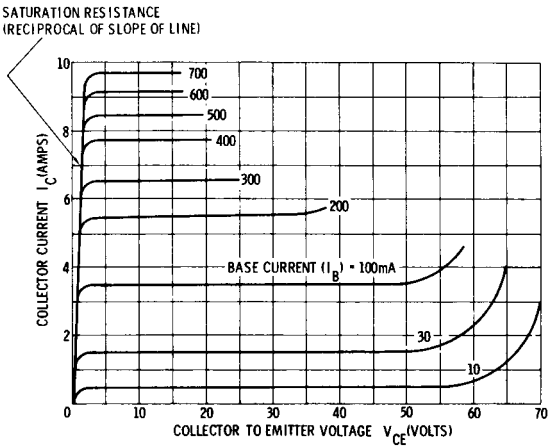
$$P_{diss} = V_{CC}\left(\frac{I_{CM}}{2}\right) = \frac{V_{CC}I_{CM}}{2} \qquad (6\text{-}9)$$

When comparing Equations 6-8 and 6-9, it becomes obvious that the transistor can deliver, at best, a power equal to half the power it dissipates. This is true in all class-A arrangements.

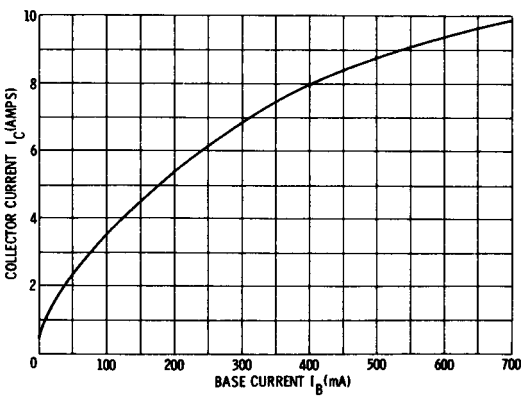
The power demanded from the supply is:

$$P_{CC} = (I_{CM}/2)V_{CC} \qquad (6\text{-}10)$$

since no additional power is lost in the load resistor and the power dissipated in the base circuit is negligible. The percent efficiency is now:



(A) Collector characteristics.



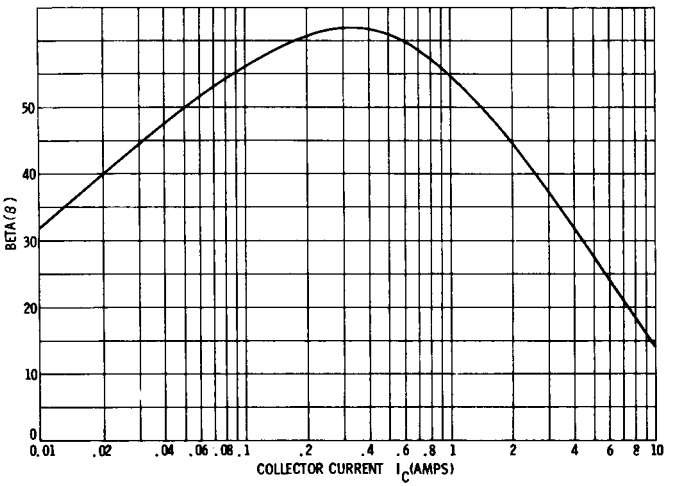
(C) I_C — I_B characteristic curve.

Fig. 6-5. Characteristics

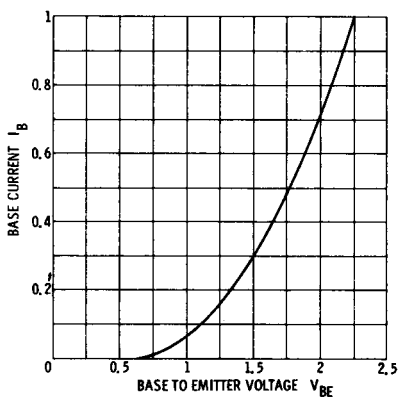
$$\% \text{ eff.} = \left(\frac{P_{R_L}}{P_{CC}}\right) 100 = \left(\frac{V_{CC}I_{CM}/4}{V_{CC}I_{CM}/2}\right) 100 = 50\% \qquad (6\text{-}11)$$

Class-A amplifiers, as a rule, should be distortion-free. However, there are several factors that lead to distortion. Many of these can be deduced from the curves of the 2N3055 silicon power transistor, in Fig. 6-5.

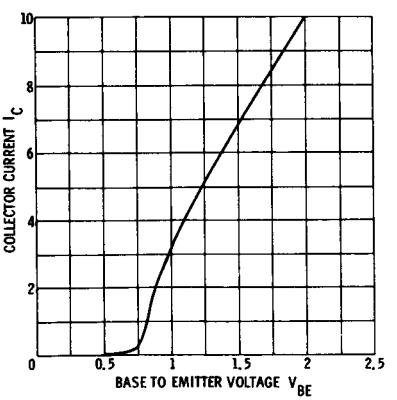
The curves of the collector family in Fig. 6-5A are not evenly spaced. Because β depends on the spacing, the current gain is not constant. The variation of β_{dc} with collector current is shown in Fig. 6-5B. Another



(B) Collector current as of function of β.



(D) V_{BE} — I_B curve.



Courtesy RCA

(E) V_{BE} — I_C curve.

of a 2N3055 transistor.

presentation of β nonlinearity is shown in Fig. 6-5C, where a plot is made of the change of collector current with base current.

Nonlinearity due to the diode characteristic of the base-emitter junction, is shown in Fig. 6-5D. The base current does not vary linearly with the base-emitter voltage.

If the output is to be undistorted, the collector current must have the same shape as the base-emitter voltage. This is desirable, as the input signal is from a voltage source and the output voltage developed across a load resistor, $I_C R_L$, is proportional to the collector current. It is fortunate that the nonlinearities in Figs. 6-5C and 6-5D tend to cancel. A curve of the collector current variation with base-emitter voltage changes is shown in Fig. 6-5E.

The impedance or resistance presented to the base-emitter junction of the output transistor (source impedance) has a decided effect on the distortion. There are analytic methods utilizing the curves in Figs. 6-5C and 6-5D, to derive the optimum size of the generator impedance. However, the most practical method to determine this is by trial and error in the laboratory. Zero ohms in series with the generator (a perfect voltage source) is usually optimum for minimum distortion. In some cases, however, the preferable source impedance is quite large.

The input signal may force I_C and V_{CE} to swing over the full length of the load line. There will be distortion at the extreme ends. The useful swing cannot extend to below I_{CEO} at one end of the load line. Reasonable swing is limited to the saturation voltage at the other extreme. The saturation resistance is the line extending about vertically from the vertex, as shown in Fig. 6-5A. The saturation voltage is V_{CE} at a particular collector current, I_C, on the near-vertical line. At 10 amperes, the saturation voltage for the 2N3055 is 2 volts. There is no useful transistor action below the 2 volts. Although not measurable at the leads, the base-collector junction is forward biased when the transistor is in saturation.

A Class-A Example

Design a class-A amplifier capable of delivering a minimum of 1 watt to an 8-ohm load. A 20-volt supply is available. Use the 2N3054, assuming that it can dissipate 5 watts with the heat sink available.

If 1 watt is required at the output, the transistor must be capable of dissipating at least 2 watts. The 5 watt device should be adequate.

The collector curves of the 2N3054 are shown in Fig. 6-6. Determine several points on the $P_{CEM} = 5$ watts curve and plot them on the drawing.

At 40 volts, the maximum permissible collector current is 5 watts/40 volts = 0.125 amp.

At 30.0 volts, it is 5 watts/30.0 volts = 0.166 amp.
At 20.0 volts, it is 5 watts/20.0 volts = 0.250 amp.
At 10.0 volts, it is 5 watts/10.0 volts = 0.500 amp.

At 5.0 volts, it is 5 watts/5.0 volts = 1.000 amp.
At 2.5 volts, it is 5 watts/2.5 volts = 2.000 amps.

Now connect all the points just determined. The ac load line must not extend above this maximum permissible power disspiation curve for this transistor.

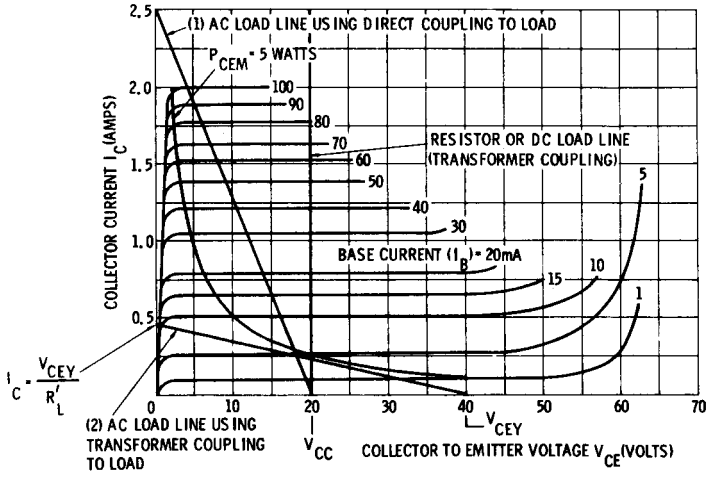


Fig. 6-6. Output characteristic curve of 2N3054.

The worst saturation condition shown in the curves in Fig. 6-6 is at 2 amps collector current. The minimum useful collector-emitter voltage with 2 amps of collector current is 2 volts. The transistor is in saturation when V_{CE} is less than 2 volts. The load line, at worst, must end at this voltage, as far as the voltage swing is concerned.

At the other end of a load line, 2 volts may be lost due to leakage current, I_{CEO}.

Using the information just accumulated, let us determine if the 8-ohm resistor can be used as a load and placed into the collector circuit, as in Fig. 6-1A.

From the 20-volt supply, 2 volts must be deducted due to the saturation voltage. A second 2 volts must be deducted to account for any loss of swing due to I_{CEO}. The output swing is limited to 16 volts, at best. If an 8-ohm load were placed in the collector circuit, line (1) in Fig. 6-6 would be the resultant load line. One point is at $I_C = 0$, $V_{CE} = 20$ volts and the second point is at $V_{CE} = 0$, $I_C = V_{CE}/R_L = 20/8 = 2.5$ amps. This circuit cannot be used because the load line is out of the P_{CEM} limits. It crosses the hyperbola. Furthermore, the power delivered to the load will be, from

Equation 6-2, equal to $V_{CC}^2/8R_L = 16^2/8(8) = 4$ watts. This is good, but far more than is required.

It should be noted that 16 volts rather than 20 volts was used in the equation for V_{CC}. Although V_{CC} is actually 20 volts, the voltage swing is limited to 16 volts due to I_{CEO} and the saturation voltage. Because this 16 volts determines the actual power that can be delivered to the load, it must be the figure substituted into this equation.

The maximum power dissipated by the transistor is at the midpoint of its swing. It is at 10 volts and 1.25 amps. The dissipated power is $10 \times 1.25 = 12.5$ watts.

Evidently, the transformer-coupled arrangement of Fig. 6-3A must be used.

It is assumed that the primary of the transformer has zero resistance. The dc load line is vertical from 20 volts on the V_{CE} axis in Fig. 6-6.

One point on the ac load line may be $2V_{CC}$ (or less) or 40 volts. However, the swing is limited by 4 volts due to the saturation and leakage. Add a 10 percent safety factor, so the total swing will be 32 volts. Add another 25 percent to the required 1 watt output power to account for output transformer losses. The output should then be 1.25 watts.

As the maximum peak-to-peak voltage swing across the primary of the output transformer is 32 volts, the peak voltage is $32/2 = 16$ volts and the rms voltage is $16/\sqrt{2}$. As the required output power is 1.25 watts, we can write an equation to determine R_L', the reflected ac resistance across the primary of the transformer.

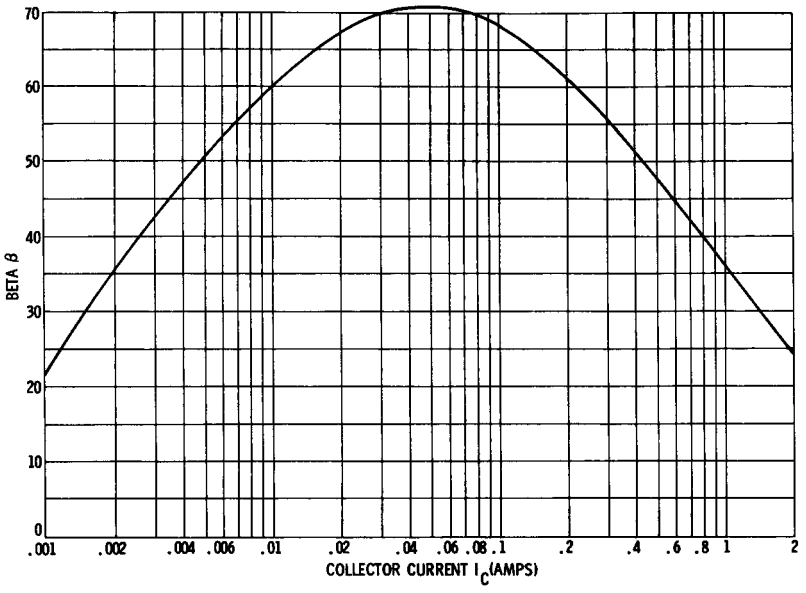
$$1.25 \text{ watts} = \frac{(16/\sqrt{2})^2}{R_L'} = \frac{128}{R_L'}$$

so that $R_L' = 128/1.25 = 102$ ohms.

Draw this load line on the curves in Fig. 6-6. One point is at $I_C = 0$, $V_{CEY} = 40$ volts. A second point is at $V_{CE} = 0$, $I_C = V_{CEY}/R_L = 40$ volts/102 ohms = 0.392 amp. This line falls comfortably within the power dissipation rating of the device. The maximum dissipation at the middle of the swing is 20 volts $\times$ 0.392/2 amps = 3.92 watts.

The quiescent dc collector current can be determined from the point where the dc load line and the ac load lines intersect. This is 0.196 amp. To account for the contingency when there is dc resistance in the primary winding of the transformer, and the dc load line is at a slight tilt, use a collector idling current of 0.2 amp in the calculation. The base current is about ⅔ the distance from the 1-mA to the 5-mA curves. It can be estimated at 3.6 mA.

A more accurate way of determining the base current is to use the curve in Fig. 6-7, which is a plot of β for different values of collector current. When the collector current is 0.2 amp, β is 63. The base current from this plot is 0.2 amp/63 = 3.2 mA. Use this more accurate value in your calculations.



Courtesy RCA

Fig. 6-7. Dc beta characteristic curve for 2N3054.

Returning to Fig. 6-3, when $V_{CC} = 20$ volts and $I_B = 3.2$ mA, R_B is equal to $20/(3.2 \times 10^{-3}) = 6260$ ohms. Use the closest 10% value of 6800 ohms.

The ratio of the impedances in the two windings of the transformer is $R_L'/R_L = 102/8$. The turns ratio is equal to $\sqrt{102/8} = 3.6{:}1$.

CLASS-B AMPLIFIERS

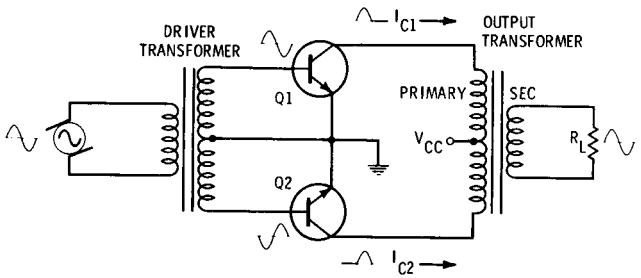
In this type of amplifier arrangement, each transistor conducts for ½-cycle only. Two transistors in a push-pull circuit are required to reproduce an entire sine wave.

A typical circuit is shown in Fig. 6-8A. A sine wave, fed to the driver transformer, appears in the secondary winding, as shown. An equal voltage is across each half of the secondary. The voltage at the base of Q1 is 180° out of phase with the voltage at the base of Q2. Each transistor conducts only during the portion of the cycle when the base is positive with respect to the emitter. The currents through the collectors are shown as I_{C1} and I_{C2}. They combine within the output transformer to recreate the composite signal which is delivered to the load, R_L.

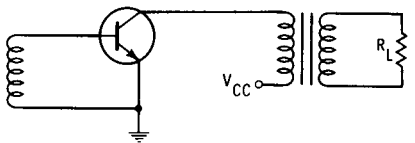
The voltage between the collector and ground of the transistor that is turned off is equal to V_{CC} plus the signal voltage across half the output transformer. The maximum voltage during the time the transistor is turned

off is $2V_{CC}$. This voltage can exist across the transistor even when it is turned on due to the phase shift of a reactive load, and in class-AB operation due to quiescent idling current.

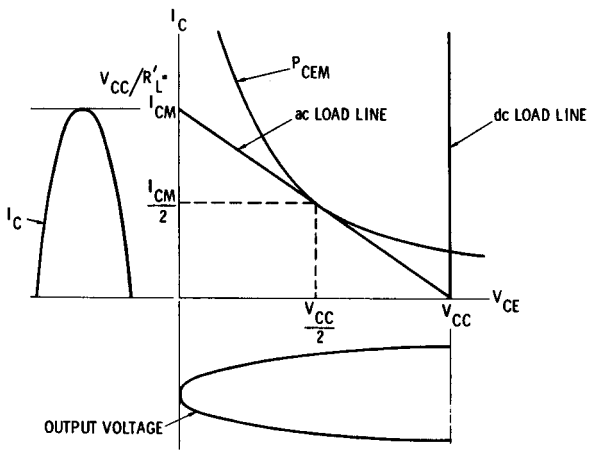
The voltage between the base and collector is greater than $2V_{CC}$. It is equal to $2V_{CC}$ plus the peak voltage across the base-emitter junction, when the transistor is not conducting. This latter voltage is determined by the maximum signal voltage at the base.



(A) Push-pull amplifier.



(B) One half of push-pull amplifier.



(C) Output curves for push-pull amplifier.

Fig. 6-8. Push-pull amplifier and curves.

The load reflected from the secondary to the entire primary of the output transformer is R_L'. The turns ratio of the entire primary to the secondary, from Equation 6-7, is:

$$(N_1/N_2)^2 = R_L'/R_L$$

For half the primary, the reflected load is R_L''. The turns ratio for this is:

$$\left(\frac{N_1/2}{N_2}\right)^2 = \frac{R_L''}{R_L} = \frac{N_1^2}{4N_2^2}$$

so that:

$$\left(\frac{N_1}{N_2}\right)^2 = \frac{4R_L''}{R_L} = \frac{R_L'}{R_L}$$

providing the information that $4R_L'' = R_L'$. From this we can conclude that the resistance seen by one transistor is one-fourth the resistance seen by the two transistors combined. As the turns ratio is doubled, the impedance ratio is multiplied by four.

In analysis and design of a push-pull circuit, it is convenient to consider one-half of the circuit at a time. This is drawn in Fig. 6-8B. The load that each transistor sees is R_L''. The load seen by both transistors is $4R_L''$.

The load lines in Fig. 6-8C are drawn as before. The dc load line is drawn vertically starting at V_{CC} on the horizontal axis. It is assumed that there is zero dc resistance in the transformer windings.

The ac load line starts at V_{CC} on the V_{CE} axis. A second point is $I_{CM} = V_{CC}/R_L''$ on the vertical axis. The line connecting these two points is the ac load line.

Assuming a sinusoidal input, one-half of the cycle is reproduced by each transistor in the push-pull pair. Each transistor will conduct only during the half-cycle when its base is positive with respect to the emitter. The collector current swing in each transistor is as shown. The collector-emitter voltage is drawn next to the V_{CE} axis.

The output voltage and collector current (for each transistor) are each one-half of a sinusoidal cycle. From the discussion on power supplies in Chapter 1, the rms value of a half-cycle is the peak voltage or current, divided by two. The average value of a half-cycle is the peak voltage or current divided by π. Refer to the discussion of half-wave rectifiers if you do not recall these relationships.

The maximum rms power delivered to the load by one transistor of a push-pull pair is:

$$P_{R_L''} = I_{rms}V_{rms} = \left(\frac{I_{CM}}{2}\right)\left(\frac{V_{CC}}{2}\right) = \left(\frac{I_{CM}}{2}\right)^2 R_L'' = \frac{\left(\frac{V_{CC}}{2}\right)^2}{R''_L} = \frac{V_{CC}^2}{4R_L''} \qquad (6\text{-}12)$$

This assumes that the voltage swings from V_{CC} to 0 volts and the current

swings from zero to I_{CM}. The swing from cutoff to saturation will be referred to as the "total range."

The maximum power dissipated by the transistor is at the center of the current or voltage swing. This point is where $I_C = I_{CM}/2$ and $V_{CE} = V_{CC}/2$. This power is:

$$P_{diss}(max) = (I_{CM}/2)\ (V_{CC}/2) = (I_{CM})^2 R_L''/4 = V_{CC}^2/4R_L'' \tag{6-13}$$

P_{R_L}'' is equal to P_{diss} (max). This means that the maximum sinusoidal rms power a transistor can deliver to a load, and not cross the P_{CEM} hyberbola, is equal to the maximum power the transistor dissipates at any point in the cycle.

The current delivered by the power supply to the transistor and its load is the average dc current in one half-cycle. This is I_{CM}/π. The supply voltage is V_{CC}. The power delivered to the circuit by the supply is:

$$P_{CC} = \frac{I_{CM}}{\pi} V_{CC} = \frac{V_{CC}^2}{\pi R_L''} = \frac{I_{CM}^2}{\pi} R_L'' \tag{6-14}$$

so that the efficiency expressed in percent is:

$$\% \text{ eff} = \left(\frac{P_{R_L}''}{P_{CC}}\right)100 = \frac{\frac{I_{CM}V_{CC}}{4}}{\frac{I_{CM}V_{CC}}{\pi}}\ 100 = \frac{\pi}{4}\ 100 = 78.5\% \tag{6-15}$$

The P_{CEM} hyperbola is a plot of the maximum instantaneous power that the transistor can dissipate. If the load line should cross this hyperbola, and the transistor is maintained in this state for a period of time, the transistor will destroy itself.

But the half-cycle of sine-wave voltage and current does not maintain the transistor in the area where there is overdissipation for any length of time. It passes through this unsafe area rapidly. This rapidity increases with the frequency of the applied signal.

In class-B operation, the load line may be permitted to cross the P_{CEM} curve. The power dissipated by the transistor, P_{diss}, should be averaged over the half-cycle. However, the P_{CEM} rating of a transistor must not be exceeded by P_{diss} for any size or type of signal.

In Fig. 6-8C, if the voltage swings only a portion of V_{CC}, let us say to a peak of kV_{CC} (k is a fractional part of the possible full range voltage), I_C can only swing a portion of I_{CM} and is equal to a peak of kI_{CM}. The power delivered to the load, R_L'', is:

$$P_{R_L}'' = \left(\frac{kI_{CM}}{2}\right)\left(\frac{kV_{CC}}{2}\right) = \frac{k^2 V_{CC} I_{CM}}{4} = \frac{k^2 I_{CM}^2 R_L''}{4} = \frac{k^2 V_{CC}^2}{4R_L''} \tag{6-16}$$

The power delivered by the supply is:

$$P_{cc} = \left(\frac{kI_{CM}}{\pi}\right)V_{CC} = \frac{kV_{CC}^2}{\pi R_L''} \qquad (6\text{-}17)$$

The power dissipated by the transistor is the difference between the power supplied by the source and the power delivered to the load, or:

$$P_{diss} = \frac{kV_{CC}^2}{\pi R_L''} - \frac{k^2 V_{CC}^2}{4R_L''} \qquad (6\text{-}18)$$

From Equation 6-12, the power delivered to the load when a transistor swings its full range is $V_{CC}^2/4R_L''$. The average power dissipated by the transistor over the half-cycle in this case can be shown from Equation 6-18 to be $(V_{CC}^2/R_L'')(1/\pi - 1/4)$, because k equals 1. This is also the average power dissipated by one transistor of the push-pull pair over a complete cycle for a full swing. As you recall, the power is dissipated by one transistor of the pair during one half-cycle only and no power is dissipated during the second half-cycle. The sum of the two, or the power dissipated by one transistor for a complete cycle, is equal to the power dissipated by it for only one half-cycle, because the second half-cycle adds nothing to the dissipation.

If the swing does not cover the full range, the transistor will deliver less than $V_{CC}^2/4R_L''$ watts. However, the transistor may dissipate a higher average power over the cycle in this case than when the swing is over the full range. The maximum average power is dissipated when the output power is about 40 percent of the maximum power the transistor can deliver. The maximum average power, dissipated when the output power is 40 percent of the maximum, is $V_{CC}^2/\pi^2 R_L''$. Comparing this with the maximum power the transistor can deliver:

$$\frac{P_{R_L''}}{P_{diss}} = \frac{\dfrac{V_{CC}^2}{4R_L''}}{\dfrac{V_{CC}^2}{\pi^2 R_L''}} \approx 2.5 \qquad (6\text{-}19)^*$$

In other words, if the signal is sinusoidal, the transistor can deliver 2.5 times the power it can dissipate safely, if the power it dissipates is averaged over a complete cycle. This is only for pure sinusoidal power and does not apply to other waveforms. The maximum power it can deliver refers to the output due to a full swing of the power supply voltage. Do not confuse the maximum *average* power a transistor dissipates *over the entire cycle* (Equation 6-19) with Equation 6-13, which shows the maximum power that a transistor can dissipate *at a particular instant in the cycle.*

The reason the transistor dissipates more average power when there is less output signal swing can be readily seen if the signal is a square wave. Assume that the square wave swings the collector-emitter voltage through

the total range. At the peak of the signal, the voltage across the load is V_{CC}, but the voltage across the transistor is zero. The power dissipated by the transistor is 0 volt multiplied by I_{CM} or zero. At the other extreme, with zero voltage swing, there is V_{CC} volts across the transistor, but the collector current is zero. Once again, the power dissipated by the transistor is zero. If the square wave were to swing the collector-emitter voltage to a value between zero and V_{CC}, collector current and collector-emitter voltage would exist simultaneously and power would be dissipated by the transistor.

A design can be made reasonably safe if the maximum output power a transistor can deliver is equal to twice the maximum power it can dissipate.

The discussion on class-B amplifiers thus far concerns itself with only one transistor of the push-pull pair. For the complete push-pull circuit, double the numbers for the power dissipation, power output, and power delivered to the circuit. The power ratios remain unchanged.

A Class-B Example

Design a class-B push-pull amplifier to deliver a minimum of 40 watts to an 8-ohm load. A 20-volt supply is available. Use two 2N3055 transistors. Assume that each transistor can dissipate a maximum of 20 watts.

Design the circuit for one transistor of the push-pull pair. The power to be delivered by the transistor is 20 watts. The circuit in Fig. 6-8A will be used.

Even though V_{CE} can swing 20 volts, 2 volts should be deducted due to the saturation voltage and an additional 2 volts deducted due to the leakage current. This leaves a possible 16-volt swing. Add a 10 percent safety factor, and we have now only $16 - 10\%(16) = 14.4$ volts to work with.

The output power is $P_{R_L}'' = 20 \text{ watts} + .25(20 \text{ watts}) = 25$ watts. The extra 25 percent of 20 watts takes into account losses due to the output transformer.

$$P_{R_L}'' = 25 \text{ watts} = \frac{V_{CC}^2}{4R_L''} = \frac{(14.4)^2}{4R_L''} = \frac{52}{R_L''} \quad \text{(from Equation 6-12)}$$

$$R_L'' = 2.07 \text{ ohms}$$

14.4 volts rather than 20 volts is used for V_{CC} for the voltage swing is limited to less than the size of the actual supply. As far as the signal is concerned, 14.4 volts is effectively V_{CC}.

The maximum current, $I_{CM} = 20 \text{ volts}/2.07 \text{ ohms} = 9.7$ amps. The maximum permissible collector current is 15 amps, so this is within the rating of the transistor. According to Fig. 6-5B, the β is 15 when the current is 9.7 amps.

The maximum instantaneous power dissipated by the transistor is (20 volts/2) (9.7 amps/2) = 48.5 watts. This is more than the 20-watt rating.

The load line will cross the $P_{CEM} = 20$ watts hyperbola. However, the average power dissipated by the transistor will be less than 48.5 watts.

The maximum power the transistor can deliver, if the swing covers the full range, is 48.5 watts (Equation 6-12) the same number as the maximum instantaneous power dissipated by the transistor. However, the transistor dissipates the maximum power when it is driven to an output of only 40% of the 48.5 watts, or 19.4 watts. Using equation 6-16:

$$P_{R_L}'' = 19.4 \text{ watts} = \frac{k^2 I_{cm}^2 R_L''}{4} - \frac{k^2 (9.7)^2 (2.07)}{4} = 48.8k^2$$

so that $k = \sqrt{19.4/48.8} = 0.63$. With this information, the power dissipated by the transistor is, through Equation 6-18:

$$P_{diss} = \frac{0.63(20)^2}{\pi 2.07} - \frac{(0.63)^2(20)^2}{4(2.07)} = 19.4 \text{ watts}$$

This is less than the 20-watt limit set by the manufacturer of the transistor. There should be no problem if only sinusoidal signals are used.

The resistance seen across one half of the primary of the transformer is 2.07 ohms. The impedance of the full primary is $4 \times 2.07 = 8.28$ ohms. If the secondary is to feed an 8-ohm load, the impedance ratio of the full primary to the full secondary is 8.28:8.

Since the circuit is operating class-B, no bias network is necessary. Each transistor is turned on when the base is positive with respect to the emitter.

CLASS-AB AMPLIFIER

Class-AB is a cross between class-A and class-B operation. The bias is so designed that the transistor conducts for less than a full cycle and more than half the cycle. The push-pull circuit must be used to reproduce a complete cycle of signal. The primary reason for class-AB operation is to minimize distortion—specifically crossover distortion.

A plot of the base-emitter voltage against the collector current for the 2N3055 is shown in Fig. 6-5E. This describes the transconductance, g_{fe}, of the transistor.

The dc transconductance at any one point, g_{FE}, is equal to:

$$g_{FE} = I_C / V_{BE} \qquad (6\text{-}20)$$

so that, for example, at $V_{BE} = 1.5$ volts, $g_{FE} = 6.7$ amps/1.5 volts $= 4.46$ mhos. Thus the dc collector current is 1.5 volts $\times$ 4.46 mhos when the base emitter voltage is 1.5.

The ac transconductance is the variation of collector current and base-emitter voltage about one particular base voltage:

$$g_{fe} = \Delta I_C / \Delta V_{BE} \qquad (6\text{-}21)$$

so that at $V_{BE} = 1.5$, assuming a base-emitter swing of ± 0.5 volts, g_{fe} will be (10 amps − 2.9 amps)/(2 volts − 1 volt) = 7.1 mhos.

The input signal to a power transistor is the base-emitter voltage, as discussed above. The collector current and output power are functions of the base-emitter voltage and transconductance. When two of the 2N3055

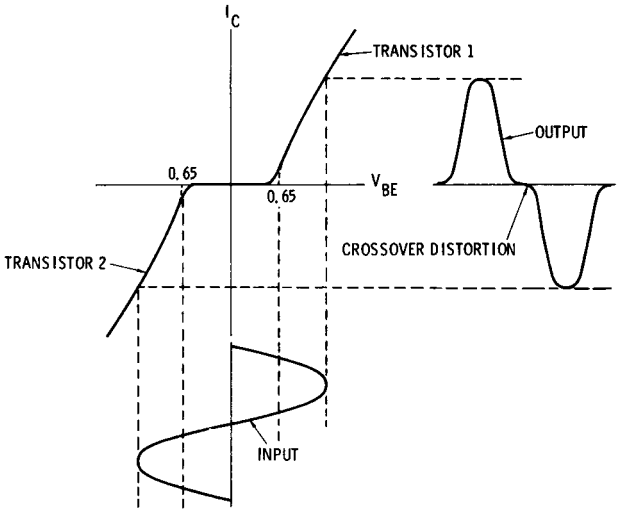


Fig. 6-9. Output due to crossover distortion.

curves are placed back-to-back for the composite representation of the push-pull operation, the output signal appears as shown in Fig. 6-9. There is no conduction when V_{BE} is somewhat below 0.65 volt. Hence there is crossover distortion due to the instantaneous pause when one transistor stops conducting and the other starts conducting.

Damage due to crossover does not end with distortion. The instantaneous cutoff of collector current sets up large voltage transients equal to five or six times the size of the supply voltage. This can cause the transistor to break down.

If the transistor were biased for a slight amount of quiescent collector current, the crossover distortion will be reduced or entirely eliminated. A composite curve for two transistors illustrating this is shown in Fig. 6-10.

The desirable minimum base-emitter voltage for the 2N3055 can be determined from the curve in Fig. 6-5E. Extend the upper and straight portion of the curve to the axis. The point where it crosses the axis is the minimum desirable V_{BE} or base-emitter idling voltage. The collector current for this base-emitter voltage can be read from the curve. Performance of the circuit can be improved if the collector idling current is raised to possibly 200 or 300 mA for large power transistors, although many man-

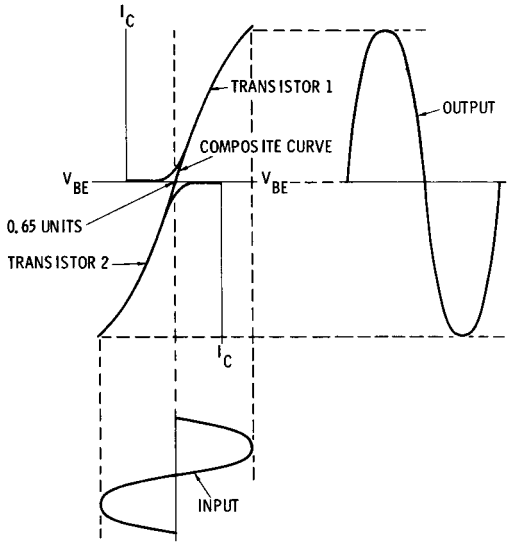


Fig. 6-10. How crossover distortion is eliminated.

ufacturers have found 10 to 25 mA satisfactory for the level of distortion they accept.

Distortion can be reduced further if the crossover point is not sharp, but is rather curved. Diodes in series with the collector or emitter leads of the push-pull transistors will provide this curved characteristic.

Distortion in class-B or class-AB circuits is a function of the source impedance, as was the case with the class-A arrangement. The optimum impedance is close to zero and should be determined experimentally.

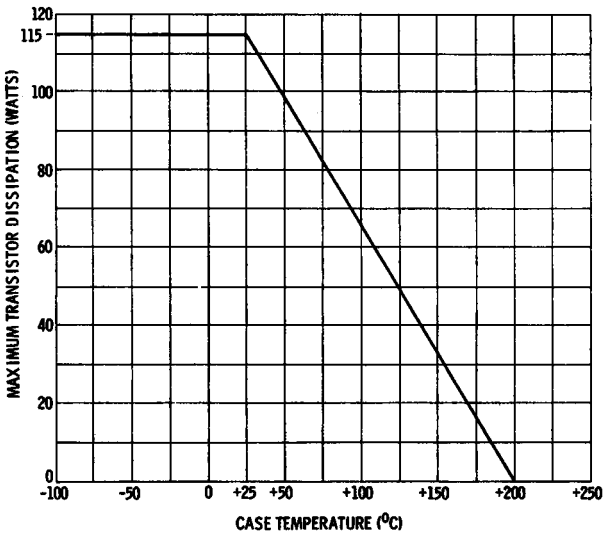
THERMAL CONSIDERATIONS

Power is dissipated at the collector junctions of the transistor. The amount of power that may be dissipated is limited by the maximum temperature at which the transistor will operate safely. At no time must this temperature be exceeded. The actual operating temperature should be considerably less than the maximum permissible junction temperature, where reliability is an important factor. The maximum junction temperature is about 100°C for germanium devices and 200°C for silicon transistors.

Heat must be conducted away from the junction to the case of the transistor, if the junction is not to be overheated by the continuous dissipation of power. This will happen if the case is cooler than the junction. However, there is a thermal resistance, θ_{JC}, between the junction and case which limits the heat carried from the junction to the case. This is not unlike the ohmic resistance in an ordinary dc circuit.

The case must also be cooled by the surrounding air if it is not to assume the junction temperature. There is a thermal resistance, θ_{CA}, between the case and the surrounding air that cools it.

The case temperature is an indication of how well heat is transferred from the junction. The temperature of the case is a function of θ_{JC} and θ_{CA}. A hot case means that little of the heat transferred from the junction to the case is radiated into the air. The transistor's ability to dissipate power decreases as the temperature of the case increases. A curve illustrating this for the 2N3055 is shown in Fig. 6-11. Other curves show the maximum permissible transistor dissipation as a function of the ambient temperature.



Courtesy RCA

Fig. 6-11. Power dissipation derating curve for a 2N3055.

If this curve is not available, it can usually be drawn from available transistor data. Mark the axes on graph paper as in Fig. 6-11. Put a dot at the point where 25 °C intersects the maximum power dissipation rating of the particular device. In this case, it is at 115 watts. Mark the 0 watts point at the maximum permissible operating temperature of the transistor. Connect these two points.

Some manufacturers supply the derating data in units of watts per degree Celsius. For the 2N3055, the derating factor is 0.66 watt/°C. The transistor's ability to dissipate power is reduced by 0.66 watt for every degree of rise of case temperature over 25 °C. If the case temperature were at 125 °C or a rise of 125 °C − 25 °C = 100 °C, the transistor would be able to safely dissipate only 115 watts − (0.66) 100 watts = 49 watts. This checks with the curve in Fig. 6-11.

The power dissipated by the transistor is related to the thermal resistance from the junction to the air, θ_{JA}, and the difference between the ambient temperature, T_A, and the junction temperature, T_J, by the equation:

$$P_{diss} = \frac{T_J - T_A}{\theta_{JA}} \qquad (6\text{-}22)^*$$

where,

θ_{JA} is the thermal resistance from junction to air,
T_A is the ambient temperature,
T_J is the junction temperature.

P_{diss} is measured in watts, T in °C, and θ in °C/watt.

The resistance, θ_{JA}, is composed of two thermal resistances, θ_{JC} and θ_{CA}, and θ_{CA} is frequently broken up into two smaller components—θ_{CS}, the thermal resistance from the case to the heat sink and θ_{SA}, the thermal resistance from the heat sink to the surrounding air.

A heat sink is a large piece of metal, preferably black anodized aluminum. The hot transistor, mounted on the sink, heats the metal, which in turn radiates the heat into the air. The metal may be flat, or it may have fins so that there is more surface in contact with the air. The resistance, θ_{CA}, is reduced if there is a heat sink, and $\theta_{CS} + \theta_{SA}$ is smaller than θ_{CA} would be without the sink.

The case of the transistor must make good contact with the heat sink if the thermal resistance between the sink and case is to be kept at a minimum. Silicon grease is used between the case and sink to minimize the thermal resistance from case to heat sink. Without grease, θ_{CS} is usually about 0.2°C/W. With grease, it is reduced by half.

The case is usually the collector of the transistor. Most circuit arrangements require the case to be insulated from the heat sink. A thin mica, teflon, or anodized aluminum washer is frequently placed between the case and heat sink. When using these washers, θ_{CS} rises to about 1.5°C/W with teflon, 0.8°C/W with mica, and 0.4°C/W with anodized aluminum. It is reduced to 0.8°C/W with teflon, 0.4°C/W with mica, and 0.3°C/W with aluminum washers, if silicon grease is used on both sides of the washer.

Formula 6-22 can be extended to the form:

$$P_{diss} = \frac{T_J - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}} \qquad (6\text{-}22A)^*$$

A thermal equivalent circuit utilizing this equation is shown in Fig. 6-12.

P_{diss}, the power dissipated in the transistor, acts like the current in an ordinary electric circuit. It takes the paths through resistors θ_{JC}, θ_{CS} and θ_{SA}. It develops heat across these resistors. The temperatures shown are all with respect to the ambient.

The temperature across resistor θ_{SA} °C/watt is $(P_{diss})\ \theta_{SA} = T_{SA}$. The temperature at A, or on the heat sink, is $T_{SA} + T_A$. T_A is the ambient temperature.

The temperature on the case at B is $(\theta_{CS} + \theta_{SA})P_{diss} + T_A$. The temperature difference between the sink and case is $(\theta_{CS})P_{diss}$.

In reality, each resistor is shunted by a capacitor indicating the time lag in removal of the heat.

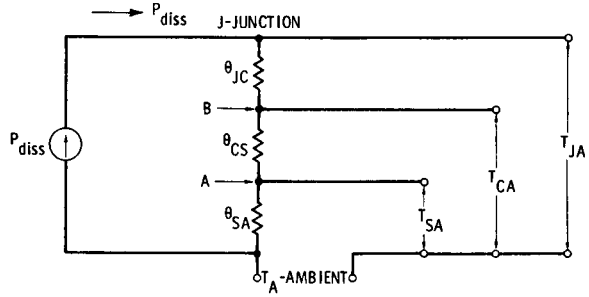


Fig. 6-12. Thermal equivalent circuit.

The material, size, and shape of the heat sink determine the thermal resistance, θ_{SA}. It is difficult to determine the exact heat sink required. In order to get a feel for the relationship between θ_{SA} and the size of the heat sink, the following approximate formula may be used for a sink made out of ⅛″ flat aluminum. The surface area, A, can be approximated from:

$$A \approx \frac{1500}{\theta_{SA}^2} \text{ square inches} \qquad (6\text{-}23)$$

A is the total area of the sink exposed to the air (not just the area on one side of the metal).

Some installations have fins mounted onto the top or side of the transistor, for use as a heat sink. This is not as effective as a sink on the bottom of the transistor because the collector junction is at the center of the base.

All this heat sinking is required if there is to be no thermal runaway, which occurs when there is more heat generated in the transistor than is removed during a specific period of time. The junction temperature must not increase more than the product of the increase in power dissipation and the thermal resistance.

The increase in collector current due to the rise in temperature is caused by the change in I_{CBO} and V_{BE} with temperature. The effect of V_{BE} is small compared to the effects of I_{CBO}. V_{BE} can be temperature-compensated by using the stabistor diode. I_{CBO} is considered here as the only important factor in the following stability formulae. For complete stability:

$$[V_{CC} - I_C(R_E + R_C)](S)(\theta_{JA})(I_{CBO}') < (273 + T_J)^2/A \quad (6\text{-}24)$$

where, in Equation 6-24

V_{CC} is the collector supply voltage,
I_C is the collector idling current,
R_E is the sum of all dc resistance in the emitter circuit such as resistors, transformer winding resistance, etc.
R_C is the sum of all dc resistance in the collector circuit such as resistors, transformer winding resistance, etc.
S is the stability factor discussed in Chapter 4. It is equal to $\Delta I_C/\Delta I_{CBO}$,
θ_{JA} is the thermal resistance, equal to $\theta_{JC} + \theta_{CS} + \theta_{SA}$,
I_{CBO}' is the maximum collector cutoff current at the maximum junction temperature at which the transistor may be operated safely. It can be determined from data supplied using Fig. 4-2,
T_J is the maximum rated junction temperature,
A is a constant equal to 8350 for germanium transistors and 14,800 for silicon devices,
$<$ is a symbol meaning less than.

The thermal resistance must at all times be less than

$$\theta_{JA} < \frac{T_J - T_A}{[V_{CC} - I_C(R_E + R_C)]\,[I_C + SI'_{CBO}]} \quad (6\text{-}25)$$

Most terms in Equation 6-25 were defined for Equation 6-24. T_A is the ambient temperature. There can be no thermal runaway if at least half the supply voltage is dropped across the sum of the dc resistance in the emitter, R_E, and the dc resistance in the collector, R_C.

RATING LIMITS AND PRECAUTIONS

There are a number of symbols used to indicate the limits of the power transistor. The absolute maximum ratings should never be exceeded, even by transients of extremely short duration.

BV_{CBO} is the breakdown voltage from the collector to the base with the emitter open.
BV_{CEO} is the breakdown voltage from the collector to the emitter with the base open.
BV_{CER} is the breakdown voltage from the collector to the emitter with a specific resistor between the base and emitter. This voltage is higher than BV_{CEO}.
BV_{CES} is the breakdown voltage from the collector to the emitter with the base shorted to the emitter. This voltage is higher than BV_{CER}.
BV_{CEV}, is the breakdown voltage from the collector to the emitter with the base-emitter junction reverse-biased.
$BV_{CE}(sus)$, the sustaining voltage, is the breakdown voltage at elevated collector current. An additional letter in the subscript indicates the resistance or voltage placed in the base-emitter circuit.

In addition to the primary breakdown voltages, currents, and powers, there is second breakdown. This is a limiting factor in power transistors only. The limiting factor in the small-signal, low-power device is the usual power dissipation curve discussed, although second breakdown is a possibility here, too.

Second breakdown seems to be due to a large amount of current through a minute area in the transistor. The high concentration of current, in addition to high voltage between the emitter and collector, produces breakdown between two semiconductor slabs. While the base exerts an influence over the collector current in controlling primary breakdown (ordinary conditions discussed previously), this is not the case when a transistor is in the second breakdown state. V_{CE} drops while the collector current rises, regardless of the applied current or voltage at the base. Because this is an irreversible phenomenon, the transistor is destroyed.

Transistors designed to operate at high frequencies are the most susceptible to second breakdown. Transistors with low thermal resistance are also good candidates for second breakdown.

Breakdown occurs whether the transistor is forward or reversed biased. In the forward-biased state, the safe energy level ($E = V_{CE} \times I_C \times t$, where t is the time duration of the voltage pulse) of a transistor depends primarily on V_{CE}. For any specific V_{CE}, the maximum safe energy level does not vary appreciably with I_C or t. The second breakdown will occur at lower collector current as V_{CE} is increased.

When designing a circuit in which the transistor is to be forward biased, two precautions should be observed to minimize the chances of second breakdown. First, choose a transistor with the poorest high frequency capabilities consistent with the design. Second, use the lowest possible collector to emitter voltage that will not adversely affect the performance.

When a transistor is reverse biased, or even opened or shorted, failures occur frequently with inductive loads at the output. These failures are due to second breakdown. In a plot on the collector characteristic, an inductive load is not a straight line, but appears as shown in Fig. 6-13. The voltage starts at V_{CC} when there is zero current through the inductor. When a signal is applied, the voltage rises across the inductor and drops to near zero across the transistor, while the collector current rises to I_{CM}. The energy stored in the inductor is $E = \frac{1}{2}(L)(I_{CM})^2$, where L is the inductance in henrys and E is the energy in joules.

When the signal is removed, the inductor retains its energy until the transient voltage is equal to the sustaining voltage. The inductor then discharges through the transistor. Because this decay time is small for high-frequency transistors, the voltage across the transistor is high.

It should be noted that the sustaining voltage increases tremendously with the reverse bias. Because of this higher voltage and higher current concentration, second breakdown is more apt to happen as the reverse bias is increased.

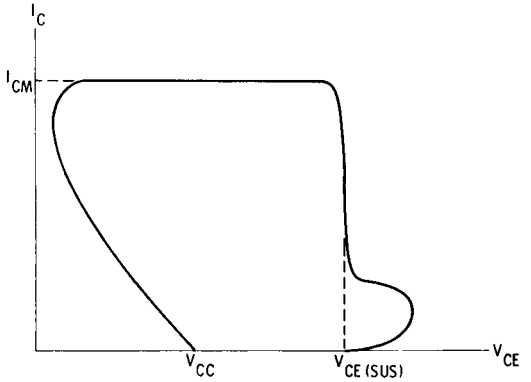


Fig. 6-13. An inductive load line.

Several factors must be observed to minimize second breakdown when the transistor is reverse biased: The resistor in the base-emitter circuit should be large while the base-emitter voltage should be small. A transistor should not be turned off rapidly from the conducting mode.

Each manufacturer supplies a set of safe operating curves. A typical group of these curves is shown in Fig. 6-14. They are derived on a statistical basis. The claim is that if the transistor $V_{CE} - I_C$ swings (on the load line or curve) are within these curves, there will be no second breakdown.

For example, if the duration of a pulse of one half-cycle is 5 ms, the ac load line (curve or ellipse) should be below and to the left of curve (1). If the pulse is up to 1 ms long, the load line should fall below curve (2). However, if the pulse is longer than 5 ms, the load line must also fall below curve (1). Use curve (3) for pulses that are 500 μs duration but less than 1 ms long. Use curve (4) as the limit when pulses are 50 μs duration but less than 500 μs long. No point representing a combination of dc collector current and collector to emitter voltage is to fall above the line marked (dc). Load lines due to long pulses should likewise be limited by the (dc) curve.

The time for a complete cycle is 1/frequency. If a sine wave is fed to an amplifier, use one half of this as the pulse duration time. It includes quite a large extra safety factor.

The $I_C - V_{CE}$ characteristics (load line or curve) of a circuit should be checked on a calibrated scope after a design has been completed. Set up a test so that the horizontal trace of the scope is a measure of V_{CE} and the vertical deflection is proportional to I_C. The curves should fall within the safe operating regions under all output load and input frequency conditions.

Example Three

As another example, design the heat sink and bias circuits for use with the amplifier in the class-B example. Assume that the maximum ambient temperature is 60°C. Make it into a class-AB amplifier.

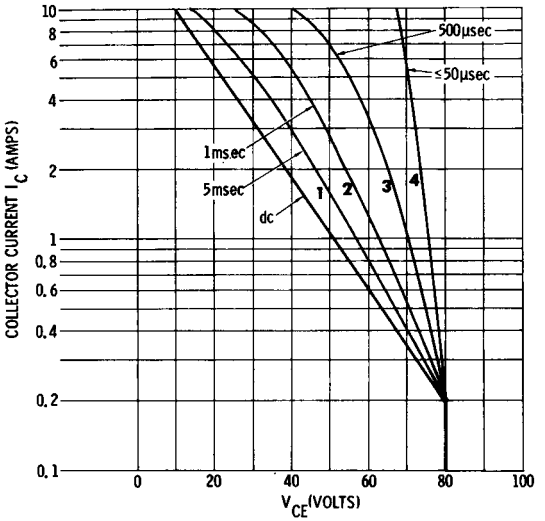


Fig. 6-14. Typical forward-biased safe operating curves.

In the graph in Fig. 6-5E, the curve crosses the V_{BE} axis when the base-emitter voltage is equal to about 0.75 volt. This is the minimum bias voltage that should be placed between the base and emitter of each transistor in Fig. 6-8A. The arrangement in Fig. 6-15 can be used. Assuming that R2 is 6.8 ohms, R1 can be determined from the voltage divider equations:

$$0.75 \text{ volt} = \left(\frac{R2}{R1 + R2}\right) 20 \text{ volts} = \left(\frac{6.8}{R1 + 6.8}\right) 20$$

Solving this, R1 = 174 ohms. Use a 150-ohm, 10 percent resistor even though 180 ohms and 10 percent is the closest standard value. This will produce the more desirable condition where V_{BE} and hence the collector idling current is somewhat higher than planned so that crossover distortion will be reduced even further.

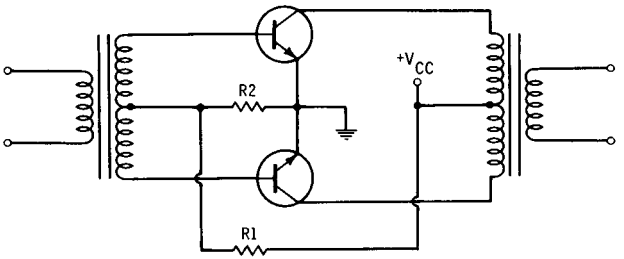


Fig. 6-15. Circuit of Fig. 6-8A with bias circuit added.

In the class-B example, each transistor must dissipate 19.4 watts. Let us round this off to 20 watts. It is not unreasonable to add this to the calculated dissipation considering that now additional power is dissipated due to the quiescent collector current required for class-AB operation. Furthermore, heat sink calculations are approximate and a bit of leeway is desirable.

The curve in Fig. 6-11 shows that if the transistor is to dissipate 20 watts, the maximum permissible case temperature is 170°C. The maximum thermal resistance from the case to the ambient is:

$$\theta_{CA} = \frac{T_C - T_A}{\text{diss}} = \frac{170°C - 60°C}{20} = 5.5°C/\text{watt}$$

Assume that the transistor is insulated from the heat sink with a mica washer. It is customary to use silicon grease on both sides of the washer. In this case, $\theta_{CS} = 0.4°C/\text{watt}$, so that $\theta_{SA} = 5.5°C/W - 0.4°C/W = 5.1°C/\text{watt}$. The surface area of a $\frac{1}{8}''$ flat aluminum heat sink, according to Equation 6-23, is about $A = 1500/\theta_{SA}{}^2 = 1500/26 = 58$ in^2. For both transistors in the push-pull circuit, this area is 116 square inches. This is the total exposed areas on both sides of the sink.

If Fig. 6-11 is not available but θ_{JC} and the maximum operating temperature are known, calculate $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ from Equation 6-22A and subtract $\theta_{JC} + \theta_{CS}$ from θ_{JA} to find θ_{SA}. The rest of the solution is as indicated above.

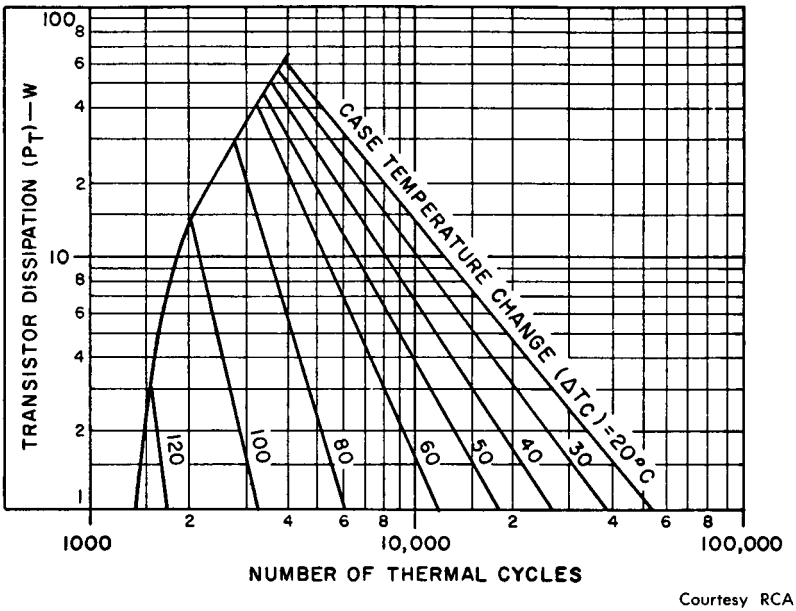
THERMAL-CYCLING RATING

It is well known that after sheet metal has been bent back and forth several times, it will break. A similar phenomenon can be observed with power transistors. After the device has been heated and cooled a number of times, there will be a mechanical breakdown. This can be due to metal fatigue, differences between the expansion of the chip and the metal to which it is attached, or cracks formed in the solder used in the device.

In many applications, the number of temperature changes or cycles can be a limit on the life of the device. RCA developed a chart relating the number of such thermal cycles a device is capable of withstanding to the power the device can dissipate. This relationship differs with the magnitude of the changes in temperature of the case. A chart for the 2N6100 transistor is shown in Fig. 6-16.

If we assume an average of 1000 cycles each year a consumer product is used, an item with a projected life of five years would require devices capable of withstanding 5000 cycles without breakdown. Should the case temperature change by 60°C during each cycle, the 2N6100 must be limited to a power dissipation of 12 watts. Should more power be dissipated, the transistor will probably not last the 5000 cycles. Similarly, higher case-temperature changes at the specified power dissipation will result in a

loss of transistor longevity. The case-temperature changes can frequently be held within desirable limits by using a proper heat sink.



Courtesy RCA

Fig. 6-16. Thermal cycles curve for RCA 2N6100 transistor.

Let us take this one step further. Assume that a transistor does not change an equal amount in temperature during each cycle. For example, let us assume that the transistor will operate for 30,000 cycles with a 20°C case-temperature change while dissipating 1.5 watts, and that it will operate for an additional 5000 cycles with a 50°C case temperature change while dissipating 10 watts. Is the device operating within its thermal limits?

In the first group of temperature changes, the maximum number of cycles permitted with a variation in case temperature of 20°C and 1.5 watts of dissipation is 40,000 cycles. The ratio of the actual number of cycles to the maximum permissible number of cycles for a 20°C case temperature change is $30{,}000/40{,}000 = 0.75$.

As for the second group of variations when the case temperature changes by 50°C and 10 watts is dissipated by the device, the maximum number of permissible cycles is 6500. The ratio of the actual number of cycles to the maximum permissible number of cycles for a 50°C temperature change while dissipating 30 watts is $5000/6500 = 0.77$.

If the sum of the two fractions is less than 1, the transistor is operating within its thermal-cycling rating. In this case, the sum is $0.75 + 0.77 = 1.52$. The transistor is not being used within its rating and will probably break down sooner than desired.

Chapter 7

COUPLED CIRCUITS

Practical amplifiers require more gain than can be derived from a single transistor stage. Each transistor circuit can provide just so much voltage, current, or power gain. To increase the flexibility, several transistors must be connected together. The first transistor in a circuit is designed to increase the gain a specific amount. The second transistor utilizes the amplified output from the first device, and increases the signal further. The overall gain from two devices is the product of the gains of the individual stages.

There are three methods frequently used to couple two transistor stages: RC coupling, direct coupling, and transformer coupling. They will be discussed in this sequence with appropriate examples.

RESISTANCE-CAPACITANCE COUPLING

A typical RC-coupled circuit is shown in Fig. 7-1. As a first approximation, assume C1, C2, and C3 are short circuits for the signal or ac voltages, and that they are open circuits for dc.

A signal voltage, V_{in}, is fed to the base of transistor Q1 throught C1. the dc bias conditions for this stage are established by R_{B1}, R_{E1}, and R_{C1}. The input voltage, V_{in}, is amplified by Q1. The voltage gain of this stage, when isolated from Q2, is approximately equal to R_{C1}/R_{E1}. The amplified signal is fed through C2 to the base of Q2. Ignoring R_L, the load resistor, the gain of Q2 is about R_{C2}/R_{E2}. R_{B2}, R_{E2}, and R_{C2} establish the quiescent dc conditions for Q2. The amplified signal is fed through C3 to the load resistor, R_L.

Using numbers, the design of an RC-coupled amplifier usually starts with the output stage. The circuit components around Q1 are determined later.

In Fig. 7-1, assume that the betas of Q1 and Q2 are both equal to 100; $V_{in} = 0.1$ rms volt of input signal; and 10 volts rms signal is required across the output load resistor, R_L. Let R_L be 5000 ohms. Determine the components and power supply required for a reasonably undistorted output.

The output is to be 10 rms volts and the input is 0.1 rms volt. The overall ac voltage must be as least $10/0.1 = 100$. The voltage gain of the first stage multiplied by the voltage gain of the second stage must equal 100 (or slightly more).

We could make the voltage gain of each stage equal to 10, so that the product of the gain of the two stages is 100. However, the gain of the second stage is usually made lower than that of the first stage. This is due to the normally small load impedance, R_L, fed by the output of the final stage of amplification.

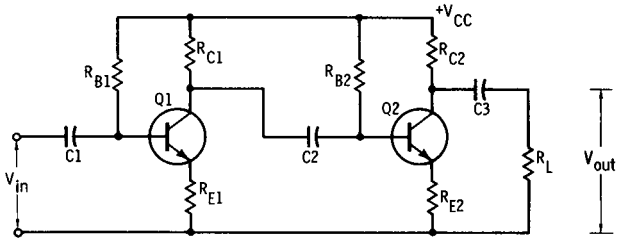


Fig. 7-1. Resistance-capacitance coupled circuit.

Transistor Q2 must develop 10 volts rms or 28.2 volts peak-to-peak across the 5000-ohm load resistor, R_L. This same voltage must be developed across R_{C2}. If R_{C2} is made large compared to the 5000-ohm resistor, the voltage swing across both resistors is limited, as shown in Fig. 7-2. In this drawing, the actual transistor output curves have been omitted for clarity. Only the ac and dc load lines are shown.

When the 5000-ohm resistor, R_L, is not in the circuit, the ac and dc load lines coincide and the collector voltage swing may range from V_{CC} to 0. Connecting the 5000-ohm resistor (through C3) across R_{C2}, reduces the ac load resistance to the parallel combination of R_{C2} ohms and 5000 ohms. Using Q as the quiescent point, the voltage swing is reduced to the maximum span from V_{CE2} to V_{CE1}. If the ac resistance is comparable in size to the dc resistance, the ac and dc load lines just about coincide and the ac voltage swing approaches the maximum 0 to V_{CC} volts. It is most desirable for R_{C2} to be much smaller than R_L. About 1/10 of R_L is an ideal size for R_{C2}. Realistically, R_{C2} is specified at 1/10 to 1/2 of R_L.

We have just determined that R_{C2} must be small compared to R_L. R_{E2} must be relatively large for stability purposes. The approximate voltage gain is R_{C2}/R_{E2}. Because this ratio is naturally small, the second stage will evidently have low gain. As noted before, the voltage gain of this stage is usually lower than the gain of the preceding stage. Let us try for a gain of 5. Then the ratio of the load in the collector circuit, equal to R_L in parallel with R_{C2} (refer to this as R_P), to the emitter resistor, R_{E2}, should be about 5.

If 28.2 peak-to-peak volts is to be developed across R_P, one fifth of 28.2 volts, or about 5.6 volts must be across R_{E2}. As the ac load is $R_P + R_{E2}$, the minimum voltage swing across this load is $28.2 + 5.6$ or 33.8 volts. Adding some leeway due to leakage current, we may assume that the ac load line will cross the V_{CE} axis at 36 volts. Since the collector to emitter voltage must swing $\pm 28.2/2$ or 14.1 volts on either side of the quiescent voltage, the maximum voltage at Q is $33.8 - 14.1 = 19.7$ volts. Use Q at 19 volts.

The dc load line must likewise pass through Q at 19 volts. If we assume the supply voltage is double the quiescent voltage, $V_{CE} = 38$ volts. One point on the dc load line is thus $V_{CE} = 38$ volts, $I_C = 0$ amperes. The second point is on the vertical axis when $V_{CE} = 0$ volts and $I_C = 38/(R_{C2} + R_{E2})$ amperes. At the quiescent point, the collector current is $I_C = \frac{1}{2}[38/(R_{C2} + R_{E2})] = 19/(R_{C2} + R_{E2})$.

Equating two relationships for the ac load line, we can determine R_{C2} and R_{E2}. One relationship derived from Fig. 7-2 is $R_{ac} = (36\text{-}19)/[19/(R_{C2} + R_{E2})]$. The second equation can be noted from the circuit in Fig. 7-1 where $R_{ac} = R_P + R_{E2} = [5000\ R_{C2}/(5000 + R_{C2})] + R_{E2}$. Equating both statements for the ac load resistance,

$$R_{ac} = \frac{17(R_{C2} + R_{E2})}{19} = \frac{5000\ R_{C2}}{5000 + R_{C2}} + R_{E2}$$

We design with the assumption that R_{C2} is much smaller than R_L, or that R_P is just somewhat smaller than R_{C2}. So if we let the ratio of R_P to R_{E2} equal 5, the ratio of R_{C2} to R_{E2} does not differ much from 5. If this ratio were made equal to 5.5, $R_{C2} = 5.5R_{E2}$. Substituting this into the above relationship, the solution to the equation is $R_{E2} = 132$ ohms and $R_{C2} = 730$ ohms. The standard 10 percent resistor for R_{E2} is 120 ohms, while for R_{C2} it is 680 ohms.

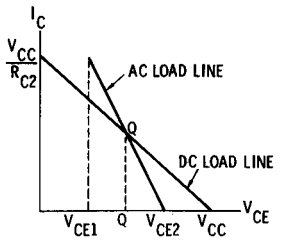


Fig. 7-2. Theoretical ac and dc load lines for Q2 in Fig. 7-1.

The second stage has a low output impedance. The ac resistance is $(5000)\ (680)/(5000 + 680) = 600$ ohms. If this stage were to have a gain of 10, R_{E2} must be made equal to 60 ohms. A small resistor in the emitter does not lend itself to good dc stability. Besides, the input impedance to transistor Q2 would be relatively small if R_{E2} is small—an undesirable condition.

R_{E2} previously was determined to be 120 ohms. The gain of the stage is thus $600/120 = 5$. If the combined gain of the two stages of amplification in this circuit is to be at least 100, the gain of the Q1 amplifier must be made equal to or more than $100/5 = 20$, which is not unreasonable. Some of the gain requirement can be removed from the first stage if we decrease R_{E2} a bit. Use the next lower standard resistor. Let $R_{E2} = 100$ ohms. The gain of Q2 then rises to $600/100 = 6$. Now, the gain of the first stage must be equal to $100/6 = 16.6$ or more. If we aim for a gain of 20 rather than 16.6, there will probably be sufficient leeway in the design.

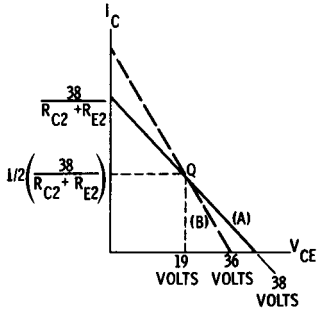


Fig. 7-3. Actual load lines for Q2 in Fig. 7-1.

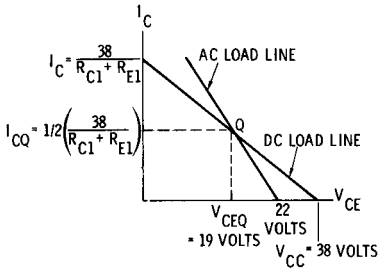


Fig. 7-4. Load lines for Q1 in Fig. 7-1.

We can now complete the design of Q2. From Fig. 7-3, the quiescent dc collector current is $(\frac{1}{2})[38/(R_{C2} + R_{E2})]$ amps $= 19/(680 + 100) = 24.4 \times 10^{-3}$ amps. The quiescent voltage across the 100-ohm resistor is $100 \times 24.4 \times 10^{-3} = 2.44$ volts. The base-emitter voltage is 0.6 volt. The total voltage from ground to the base is $2.44 + 0.6 = 3.04$ volts.

The dc base current is $I_C/\beta = 0.244 \times 10^{-3}$ amps. $R_{B2} = (38 - 3.04)/(24.4 \times 10^{-5} = 34.96/24.4 \times 10^{-5} = 143{,}000$ ohms. Use a standard 150,- $(24.4 \times 10^{-5}) = 34.96/24.4 \times 10^{-5} = 143{,}000$ ohms. Use a standard 150,000 ohm 10-percent resistor.

The impedance presented by the Q2 circuit to the output of Q1 is R_{B2} in parallel with βR_{E2}. As the latter is 10,000 ohms, the total input impedance to this last stage is 9350 ohms. The voltage required across the 9350-ohm impedance is the output voltage of Q2 divided by the gain of the stage, or 10 volts/6 = 1.66 rms volts. The peak-to-peak voltage across the 9350 ohms resistance as well as across R_{C1} must be $2.82 \times 1.66 = 4.67$ volts.

Draw the dc and ac load line curves for Q1 in Fig. 7-4. The dc load line connects $V_{CC} = 38$ volts with $I_C = 38/(R_{C1} + R_{E1})$. The ac load line must pass through the Q point. Choose this point at the center of the dc load line where $V_{CE} = 19$ and $I_{CQ} = (\frac{1}{2})[38/(R_{C1} + R_{E1})]$.

The gain of this stage is to be made equal to 20. Hence the ratio of the ac load impedance to the emitter resistance must be 20/1, or $R_{ac} = 20R_{E1}$. The size of R_{E1} is much smaller than that of R_{C1} and is considered neg-

ligible for the estimation of the dc load. However, it is not negligible in the gain calculations.

Since the required peak-to-peak ac voltage across the load is 4.67 volts, the peak voltage is $4.67/2 = 2.34$ volts. Add leeway by assuming this to be 3 volts. The ac load line will cross the V_{CE} axis at $V_{CEQ} + 3$ volts or 22 volts. This is one point on the ac load line; the other point is at Q. The total ac resistance in the collector, determined from the load line is:

$$\frac{22 - 19}{\frac{1}{2}\left(\frac{38}{R_{C1} + R_{E1}}\right) - 0} = \frac{3R_{C1}}{19}$$

since R_{E1} is much smaller than R_{C1}. The ac load resistance determined from the circuit components is R_{C1} in parallel with the equivalent input impedance of Q2, or 9350 ohms. It is $(9350)(R_{C1})/(9350 + R_{C1})$. Equating the two derivations for R_{ac}:

$$\frac{3R_{C1}}{19} = \frac{9350R_{C1}}{9350 + R_{C1}}$$

it can be shown that $R_{C1} = 50{,}000$ ohms. Use a standard 47,000-ohm, 10 percent resistor for R_{C1}.

R_{ac} is the 9350-ohm resistor in parallel with the 47,000-ohm resistor, or 7800 ohms. R_{E1} must be less than 1/20 of 7800 ohms, or 390 ohms. The gain of the first stage is thus designed at 20. Since the gain of the Q2 circuit was adjusted at 6, the overall calculated gain of the two stages is $20 \times 6 = 120$. This is well above the original requirement of 100.

The quiescent collector current is $\frac{1}{2}[38/(R_{E1} + R_{C1})] = 19/47{,}000 = 40.5 \times 10^{-5}$ amps. The base current is the collector current divided by beta or $(40.5)(10^{-5})/10^2 = 40.5 \times 10^{-7}$ amps. The voltage across the 390-ohm resistor is $390 \times 40.5 \times 10^{-5} = 0.158$ volt. The base-emitter voltage is about 0.6 volt. The voltage at the base is $0.6 + 0.158$ volt, or approximately 0.75 volt. The voltage across R_{B1} is $38 - 0.75 = 37.25$ volts. Hence $R_{B1} = 37.25/40.5 \times 10^{-7} = 9.2 \times 10^6$ ohms. The standard 10-megohm 10-percent resistor may be used.

The circuit will probably work well, but it should be checked in the laboratory with bogey transistors as well as with transistors varying on either side of its specification.

It is common practice to design the first stage of an amplifier for low noise. In this case, the collector voltage, collector current, and the impedance seen by the input of the first stage should be as small as practical. The following is a revision of the previous design, but this time the low noise requirements are included.

The input, V_{in}, must be presented with a specific impedance if the characteristics of this signal are not to be impaired. Assume that this impedance should be about 10,000 ohms. This low value of resistance can be designed into the circuit by adding a resistor, R_X, from the base of the

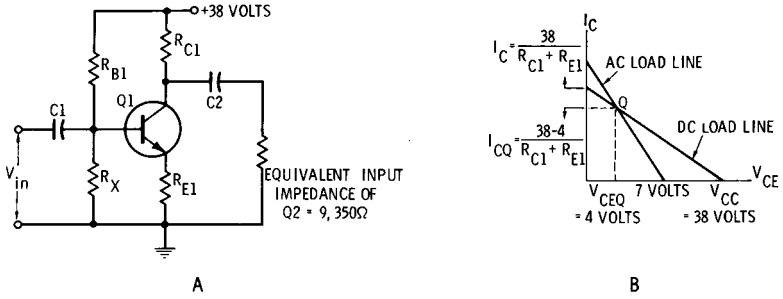


Fig. 7-5. Redesign of Q1 stage in Fig. 7-1 for low noise.

input transistor to ground. The new circuit of the first stage only, is now shown in Fig. 7-5A.

V_{CEQ}, the quiescent voltage, should be made small. Assuming that there is a maximum of 1 saturation volt for the transistor to be used, and that it requires a peak signal of 3 volts (as in the previous example), the minimum quiescent voltage for Q1 can be made equal to 1 volt + 3 volts = 4 volts.

(Saturation voltage, as discussed with reference to the curve in Fig. 6-5A, is the voltage at which the collector current drops rapidly as the collector emitter voltage is reduced. There is no useful amplifying action when V_{CE} is less than $V_{CE}(sat)$. For the 2N3055, with 10 amps collector current, $V_{CE}(sat)$ is 2 volts. It is 1 volt with about 4.5 amps collector current.)

The quiescent collector current is $(38-4)/(R_{C1}+R_{E1})$. Assume that R_{C1} is much greater than R_{E1} so that the quiescent current is $34/R_{C1}$.

The ac load line can intersect the V_{CE} line at any voltage above V_{CEQ} + 3 volts = 7 volts. The ac load resistance determined from the load line (Fig. 7-5B) is $(7-4)/[(34/R_{C1})-0] = 3R_{C1}/34$. The ac load resistance determined from the circuit as before is $9350R_{C1}/(9350+R_{C1})$. Equating the two values for R_{ac}:

$$\frac{3}{34}R_{C1} = \frac{9350R_{C1}}{9350+R_{C1}}$$

R_{C1} is equal to 97,000 ohms. Use the standard 100,000-ohm, 10-percent resistor here. R_{C1} is the major portion of the dc load line in Fig. 7-5B.

The ac impedance, from circuit values, is $(9350)(100{,}000)/9350 + 100{,}000) = 8550$ ohms. If this stage is to have a gain of 20, R_{E1} must be less than 1/20 of 8550 ohms, or 428 ohms. Use 390 ohms for R_{E1} and the gain of the first stage will be about $8550/390 = 22$, which is more than adequate.

The quiescent collector current is $(38\text{-}4)/(R_{C1}+R_{E1})$ or 34/100,000, which is about equal to 34×10^{-5} amps. This is less than the I_{CQ} in the previous calculation. The base voltage remains at about 0.75 volt. The base current is 34×10^{-7} amps because it is equal to I_C/β.

The required input impedance to this stage was stated as 10,000 ohms. The emitter resistance is $26/I_E = 26/0.34$ mA = 77 ohms. Adding this to R_E, the total resistance in the emitter circuit is 390 + 77 = 467 ohms. Reflected into the base circuit, this resistance must be multiplied by beta. In the base circuit, this resistance appears as a 46,700-ohm resistor. Since V_{in} must be offered 10,000 ohms, the 46,700 ohms resistance from the base to ground must be placed in parallel with other resistors connected from base to ground. R_X is placed from base to ground in Fig. 7-5A. R_{B1} is connected from base to ac ground. Thus, the parallel combination of 46,700 ohms, R_X, and R_{B1} must be 10,000 ohms. The parallel combination of R_X and R_{B1} (call this R_P) must be:

$$R_P = \frac{(10{,}000)\,(46{,}700)}{46{,}700 - 10{,}000} = 12{,}700 \text{ ohms} = \frac{R_{B1}R_X}{R_{B1} + R_X}$$

The base circuit and its Thevenin equivalent is drawn in Fig. 7-6. The Thevenin voltage for this circuit is:

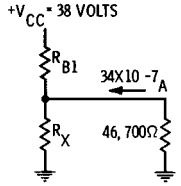
$$\frac{(38R_X)}{(R_{B1} + R_X)} \text{ volts} = [34 \times 10^{-7} \text{ amps}]\,[(12{,}700 + 46{,}700) \text{ ohms}] + 0.6 \text{ volts}$$

which simplifies to $R_{B1} = 46.5\ R_X$.

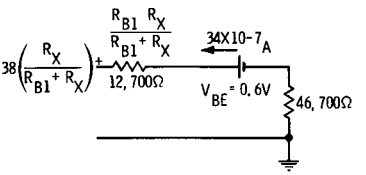
The Thevenin circuit relationship can be substituted into the previously derived equation $R_BR_X/(R_B + R_X) = 12{,}700$ ohms. Solving these relationships $R_{B1} = 590{,}000$ ohms and $R_X = 13{,}000$ ohms. Use standard 10-percent resistors in each case. Now, $R_{B1} = 560{,}000$ ohms and R_X becomes 12,000 ohms.

This solution provides us with more legitimate quiescent conditions than did the first solution. Either answer must be tested in the laboratory. Note that if V_{in} is not a perfect voltage source, its impedance must be considered in the gain calculations.

The voltage gain of either stage can be increased considerably if the emitter resistor is bypassed with a large capacitor. This will affect only the ac gain without reducing the bias stability of each stage. The voltage gain will then be equal to R_{ac}/r_e, where $r_e = 26/I_E$ with I_E expressed in milliamperes.



(A) Base circuit of Fig. 7-5.



(B) Thevenin equivalent of same circuit.

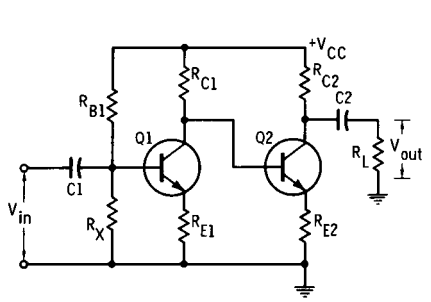
Fig. 7-6. Base current of Fig. 7-5 and its Thevenin equivalent.

The emitter resistance was omitted in voltage gain calculations. If the emitter resistance of 77 ohms were not ignored for the calculation, the gain of the first stage is $8550/(390+77) = 18.3$. The emitter resistance of the second stage is $26/I_{E2} = 26/24.4 = 1.07$ ohms, so that the voltage gain of this stage is $600/(100+1.07) = 5.9$. The overall gain for the two stages is $18.3 \times 5.9 = 108$.

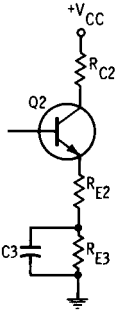
DIRECT-COUPLED AMPLIFIERS

Transistors may be connected to each other without coupling capacitors. A circuit of this type is shown in Fig. 7-7A.

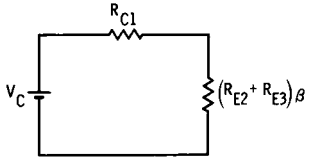
The design of this circuit is not very different from that of the capacitance-coupled type.



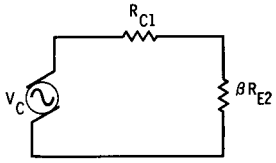
(A) Direct-coupled amplifier.



(B) Expansion of emitter circuit.



(C) Dc equivalent of the collector circuit.



(D) Ac equivalent of the collector circuit.

Fig. 7-7. Direct-coupled amplifier.

R_{C2} is determined as before. The voltage at the base of Q2, and hence the collector of Q1, is dependent upon the voltage across R_{E2}. Assuming that the base-emitter voltage of Q1 and Q2 is 0.6 volt, the voltage at the collector of Q1 is equal to 0.6 volt added to the voltage across R_{E2}. The quiescent collector voltage at Q1 must be determined as before, and the size of R_{E2} is determined from this.

The overall gain is still the product of the gains of the two individual stages. If Q2 has less gain than in the RC-coupled amplifier, the difference must be compensated for by the gain of Q1.

Using the numbers from the previous problem, let us determine values for components in the circuit in Fig. 7-7.

It was previously determined that $R_{C2} = 680$ ohms, $R_{E2} = 100$ ohms and the quiescent collector current, $I_{C2} = 24.4 \times 10^{-3}$ amps. The quiescent voltage across $R_{E2} = (24.4 \times 10^{-3})(100) = 2.44$ volts. The voltage at the base of Q2 (as well as at the collector of Q1) is $0.6 + 2.44$ volts $= 3.04$ volts.

The voltage at the collector, however, must be about 4 volts. To keep things in proper perspective, R_{E2} can be increased so that there will be the additional 1 volt at the base. R_{E2} must be increased by 1 volt/24.4 mA = 41 ohms. This additional resistance in the emitter will produce a considerable loss of gain. The emitter circuit can be augmented, as shown in Fig. 7-7B, by adding a resistor, R_{E3} (a standard 39-ohm 10-percent resistor) in series with the 100-ohm emitter resistor R_{E2}. Bypass the 39-ohm resistor with a large capacitor. The impedance of the capacitor should be less than 1/10 of R_{E3} (the emitter resistor) at the lowest frequency to be amplified. As you recall, the impedance of a capacitor is $1/6.28$ (fC), where C is in farads and f is in hertz.

The circuit for Q1 is determined as before, except that this time, the voltage drop across R_{C1} is due to the sum of the collector current through Q1 and the base current of Q2.

In analysis, the lead between the collector of Q1 and the base of Q2 should be broken. Calculate the collector circuit of Q1 according to the Thevenin theorem. Determine the voltage at the collector of Q1. It is V_C. Place this voltage in series with the parallel combination of R_{C1} and r_d (output resistance of Q1), which is usually equal to R_{C1}. This Thevenin equivalent circuit is placed across the input of Q2. The dc and ac equivalents of the collector circuit are shown in Figs. 7-7C and 7-7D, respectively.

The stability factor of this circuit is:

$$S = S_1\beta_2 \frac{R_{C1}}{R_{C1} + R_{E2}\beta_2} \tag{7-1}$$

If three such stages were coupled together, the stability factor would be:

$$S = S_1\beta_3\beta_2 \left(\frac{R_{C1}}{R_{C1} + R_{E2}\beta_2}\right)\left(\frac{R_{C2}}{R_{C2} + R_{E3}\beta_3}\right) \tag{7-2}$$

where,

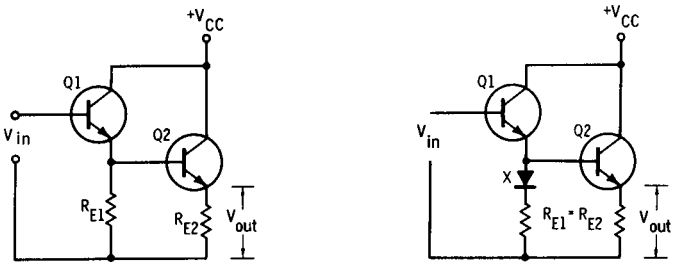
S is the change in current through the collector of the last stage due to ΔI_{CBO} in the first stage, Q1,

S_1 is the stability factor of Q1 as determined in Chapter 4.

Commonly used direct-coupled circuits are shown in Fig. 7-8. Q2, an emitter follower, is the load on Q1, which is also an emitter follower. The voltage gain is approximately equal to 1, while the current gain is equal to the product of the betas of the two transistors. In all respects, this combination acts as a single transistor with the total beta equal to the product of the betas of the two devices.

R_{E1} may be omitted or used as part of the resistance in the emitter of Q1. It is also across the base-emitter circuit of Q2. The voltage across R_{E1} is equal to the base-emitter voltage across Q2 plus the voltage across R_{E2}. This resistor, in conjunction with R_{E2}, determines the collector (or emitter) current through Q2.

Should the circuit be changed to that shown in Fig. 7-8B, an interesting and useful relationship will exist. Assuming that the diode X, has the same voltage characteristic as the base-emitter junction of Q2, and that $R_{E1} = R_{E2}$, then the currents through both resistors are identical due to identical voltage drops. Assuming that there is a negligible base current in Q2, the emitter current of Q2 is identical with that of Q1.



(A) Darlington circuit. (B) Darlington circuit with diode X added.

Fig. 7-8. Two versions of the Darlington circuit.

Direct coupling using complementary transistors is commonplace. Several circuits of this type are shown in Fig. 7-9.

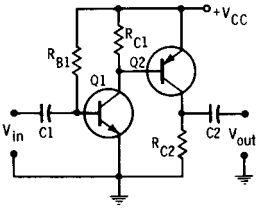
In Figs. 7-9A through 7-9D, the signal is fed to Q1. From Q1, the amplified output in Fig. 7-9A appears across R_{C1} in parallel with the input impedance of Q2. In Figs. 7-9B, 7-9C, and 7-9D, the output is across the input impedance of Q2 only. In the latter circuits, all the collector current from Q1 is transferred to the base of Q2 while no current is lost in R_{C1}. Q2 amplifies the signal further.

In the first four circuits, the size of the bias current is established by R_{B1} and V_{CC}. The collector current for Q1 is through the base-emitter junction of Q2. The collector current for Q2 is through R_{C2} to ground.

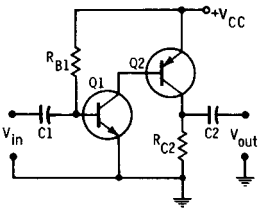
The overall β is the product of the betas of the two transistors. The voltage gain in Figs. 7-9A and 7-9B is the product of the voltage gains of the two stages.

In Figs. 7-9C and 7-9D, the voltage gain is unity, due to the placement of R_{C2} in the emitter circuit of Q1. Here, the output is fed back to Q1, which to the output load is an emitter follower. The input impedance is essentially the same as that of an emitter follower, with R_{C2} multiplied by the β of Q1 and the β of Q2.

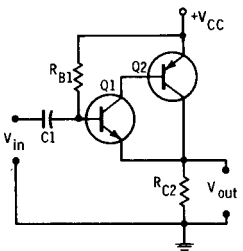
A more general version of the circuit in Fig. 7-9C is shown in Fig. 7-9E. This is quite useful in many applications. Assume that β_1 and β_2 refer



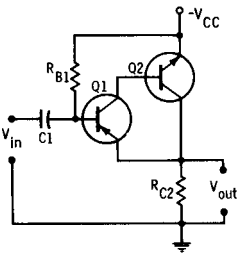
(A) Circuit where voltage gain is the product of the voltage gain of the two stages.



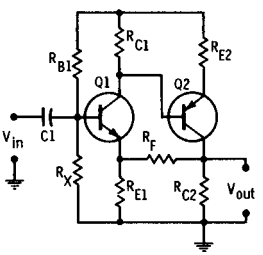
(B) Variation of Fig. 7-9A.



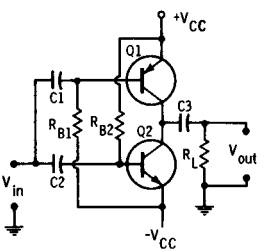
(C) Circuit with voltage gain of unity.



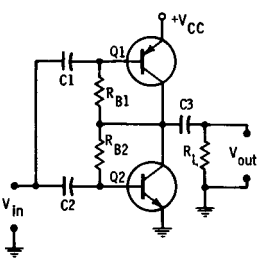
(D) Variation of Fig. 7-9C.



(E) General version of Fig. 7-9C.



(F) Push-pull circuit.



(G) Variation of Fig. 7-9F.

Fig. 7-9. Complementary transistor pairs in direct-coupled circuits.

to the current gains of Q1 and Q2, respectively. The approximate equations for the circuit are:

$$R_{in} = \frac{R_{B1}R_X}{R_{B1} + R_X} \tag{7-3}$$

$$R_{out} = \frac{R_F R_{C2}}{R_F + \beta_2 R_{C2}} \tag{7-4}$$

$$A_v = \frac{R_{E1} + R_F}{R_{E1}} \tag{7-5}$$

$$A_i = \beta_1 \beta_2 \tag{7-6}$$

$$G = \beta_1 \beta_2 \left(\frac{R_{E1} + R_F}{R_{E1}} \right) \tag{7-7}$$

Push-pull circuits can be evolved using complementary transistors, as in Figs. 7-9F and 7-9G.

Transistor Q1 conducts only on negative portions of the cycle and Q2 on positive portions. The two halves of the signal are developed across the load resistor, R_L, where it is recombined to form an amplified composite of the input.

Another form of the dc-coupled circuit uses two transistors in parallel. In this type of arrangement, the collector currents in both transistors should be equal. The best method of accomplishing this is by using independent but equal resistors in each emitter before tying them together. It is also useful to have independent but equal resistors in the two collector leads and in the two base leads, but the effect is not as pronounced as when the resistors are in the emitter leads.

The last of the dc-coupled amplifiers to be considered is the differential amplifier, a circuit of which is shown in Fig. 7-10. This is probably the most important configuration of all. Two voltages, V_{in1} and V_{in2}, are fed to the circuit. The output voltage is proportional to the difference of V_{in1} and V_{in2}. R_E should be large or synthesized by a constant-current source.

The amplifier would also work if only one source of signal were fed to the transistors. For example, assume that R_{B2} is shorted to ground. There

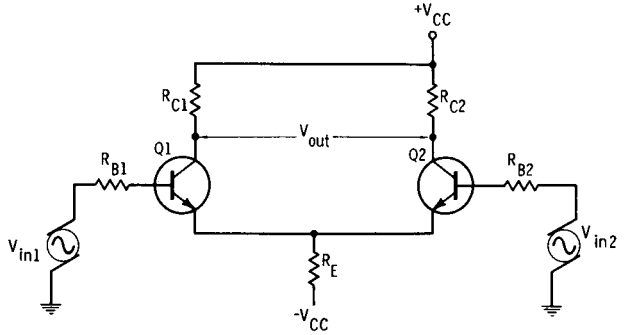


Fig. 7-10. Differential amplifier.

would still be signal at the collectors of both transistors. The output at collector Q1 would be 180° out of phase with the output at the collector of Q2.

The differential amplifier is used where good stability is required. If both transistors are bound to a common heat sink and are at identical temperatures, there will be no drift in V_{out} with changes in temperature.

Differential amplifiers can be coupled together, as shown in Fig. 7-11. The input signal is fed to and amplified by Q1, and it is further amplified by Q3. The output is V_{out1}.

The signal at the collector of Q2 is 180° out of phase with, but usually made equal to, the signal at the collector of Q1. The output from Q2 is amplified by Q4. The output here is V_{out2}.

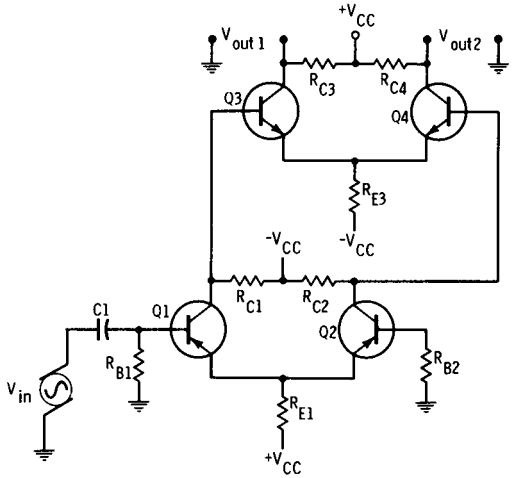


Fig. 7-11. Direct-coupled differential amplifiers.

The output voltages, V_{out1} and V_{out2}, are 180° out of phase and can be fed to the output stages of a push-pull power amplifier.

The sum of the currents through both halves of the differential amplifier should be constant. To do this, R_{E1} must be very large. It can be made large only if a large voltage is developed across the resistor. This would be the case if $+V_{CC}$ were extraordinarily big. A better job can be accomplished by using a constant-current source to replace R_{E1}, as shown in Fig. 7-12.

A reasonably constant voltage is developed across R_X. This constant voltage from the base to $+V_{CC}$ is maintained across R_E and the base-emitter junction. There will be a constant current through the transistor due to the constant voltage across R_E. This constant-current circuit can replace R_{E1} in Fig. 7-11.

The voltage across the junction and R_E of the constant-current source can be held tighter if R_X is replaced by a zener diode.

A constant-current source is the same as a high resistance. From Ohm's law, resistance is found to be equal to $\Delta V/\Delta I$, where ΔV is the change of voltage across a resistor due to ΔI, a change in current through the same resistor. As the change in current, ΔI, approaches 0, the ratio or equivalent

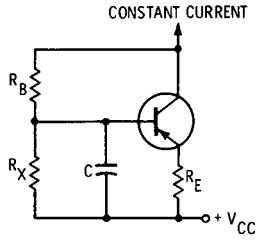


Fig. 7-12. Constant-current source.

resistance of the circuit approaches infinity. High resistance is an important characteristic of the constant-current source.

TRANSFORMER COUPLING

Transformer output stages were discussed in the chapter on power amplifiers. An example of coupling two transistors using a transformer should complete the study of this type of circuit.

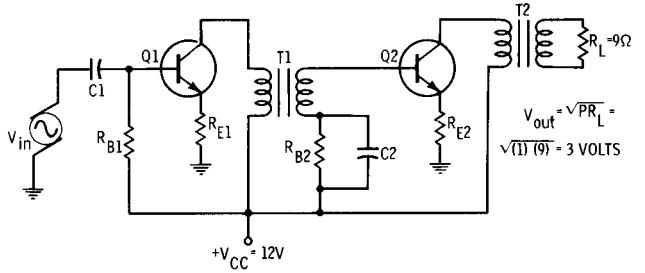
In the circuit in Fig. 7-13A, assume that the betas of Q1 and Q2 are both equal to 100. The base resistance is 500 ohms for Q2 and 0 ohms for Q1. Each transformer is 75 percent efficient. The required voltage gain of the circuit is 30 with an output of 1 watt across a 9-ohm load resistor. A 12-volt automobile battery is available as the power supply.

First, consider Q2 and the output circuit. One watt is to be developed across the 9-ohm load resistor. If the transformer is 75% efficient, at least 1 watt/0.75 = 1.33 watts must be delivered to the primary of T2. After adding a safety factor of 25 per cent due to losses in R_{E2}, saturation resistance or voltage, and I_{CBO}, the actual amount of power that is desirable at the primary, is $1.33 + 0.25(1.33) = 1.66$ watts.

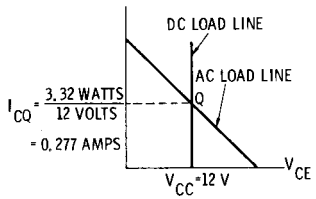
A transistor that can deliver 1.66 watts must dissipate double this power, or at least 3.32 watts. Assuming zero dc resistance in the primary winding and a 12-volt supply, the quiescent current is 3.32 watts/12 volts = 0.277 amp. In Fig. 7-13B, the load impedance is 12 volts/0.277 amp = 43.4 ohms. If we wish to have a gain of 10 in this stage, $R_{E2} + r_{e2}$ must be less than 43.4 ohms/10 = 4.34 ohms (r_{e2} is the emitter resistance of Q2.) Where I_{E2} is expressed in milliamps, r_{e2} is $26/I_{E3}$. Hence, r_{e2} is 26/277, which is very small. However, r_{e2} is seldom less than 1 ohm. Letting r_{e2} equal 1 ohm, R_{E2} can be made equal to 4.34 ohms − 1 ohm = 3.34 ohms. Use a standard 3.3-ohm resistor for R_{E2}.

In the base circuit, if the quiescent collector current of Q2 is 0.277 amp, the base current is 0.277 amp/$\beta = 0.277/100 = 2.77 \times 10^{-3}$ amps. As the supply for the base circuit is 12 volts, $R_{B2} + \beta R_{E2} =$ 12 volts/2.77×10^{-3} amps = 4340 ohms. Since $\beta R_{E2} = 100(3.3 \text{ ohms}) = 330$, $R_{B2} \approx 4340 - 330 = 4010$ ohms. Use the standard 3900-ohm resistor for R_{B2}.

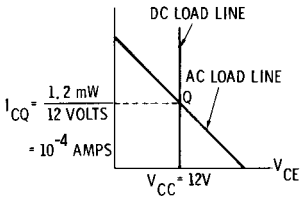
The impedance of C2 should be less than 1/10 that of R_{B2}, or less than 390 ohms at the lowest frequency to be amplified. Assume that this frequency is 20 Hz; hence $C = 1/2\pi(20)(390) = 20.3\ \mu F$.



(A) Two-stage transformer-coupled amplifier.



(B) Load lines for Q2.



(C) Load lines for Q1.

Fig. 7-13. Transformer-coupled circuit and load lines.

Returning to the output circuit, if the ratio of the primary impedance of T2 to the secondary impedance is 43.4 to 9, the voltage ratio, and hence turns ratio, of the transformer is $\sqrt{43.4/9} = 2.2{:}1$. Therefore, the gain of the output transformer is 1/2.2. The gain of Q2 is $43.4/(R_{E2} + r_{e2}) = 43.4/4.3 = 10.1$. The voltage gain from the base of Q2 to the 9-ohm load resistor is $(1/2.2)(10.1) = 4.55$. Since $V_{R_L} = \sqrt{PR_L}$, it is apparent that $\sqrt{(9 \text{ ohms})\ (1 \text{ watt})} = 3$ volts across the 9-ohm resistor, there must be 3 volts/4.55 = 0.66 volt at the base of Q2.

The input impedance to Q2 is $(R_{E2} + r_{e2})\beta + r_b = (3.3 + 1)100 + 500 = 930$ ohms. There must be $(0.66 \text{ volt})^2/930$ ohms = 0.47 mW at the base of Q2 if there is to be 1 watt across the 9-ohm resistor at the output. Adding 25 percent for transformer losses, $0.47 + 0.25(0.47) = 0.60$ mW must be delivered to the primary of T1. Q1 must then dissipate 2 ×

0.60 mW = 1.2 mW. Using a 12-volt supply, the quiescent collector current will be $(1.2 \times 10^{-3}$ watts$)/12$ volts $= 10^{-4}$ amps. Hence, the load impedance on Q1, according to Fig. 7-13C, is 12 volts$/10^{-4}$ amps = 120,000 ohms.

The ratio of the secondary to primary impedances of T1 is 930/120,000. The voltage ratio and voltage gain of the transformer is the square root of this ratio or $30.1/345 = 1/11.8$. Multiplying this by the gain of Q2 and T2, the gain from T1 to R_L is $(1/11.8) \times 4.55 = 1/2.66$. Q1 therefore must have a gain of $30 \times 2.66 = 80$ if the overall voltage gain of the circuit is to be 30. This can be accomplished by making the ratio of the primary impedance of T1, or 120,000 ohms, to $R_{E1} + r_{e1}$, to be equal to 80 (r_{e1} is the emitter resistance of Q). $R_{E1} + r_{e1}$ is then equal to 1500. If $r_{e1} = 26/I_{E1} = 26/10^{-1} = 260$ ohms (I_{E1} is the emitter current of Q1 in mA), then R_{E1} is $1500 - 260 = 1240$ ohms. Use the standard 1200-ohm, 10-percent resistor.

The base current of Q1 is the collector current divided by β or $10^{-4}/100 = 10^{-6}$ amps. Assuming that the 12-volt supply is used, $R_{B1} + \beta R_{E1} = 12$ volts$/10^{-6}$ amps $= 12 \times 10^6$ ohms. As βR_{E1} is negligible compared to R_{B1}, R_{B1} can be made equal to 12 megohms. It is preferable to apply bias circuit 2, discussed in Chapter 3, so that a smaller resistor can be used at the input of Q1.

The circuit should be checked carefully in the laboratory. It may not work properly due to the high voltage drive required at the base of Q2.

Chapter 8

SHAPING FREQUENCY RESPONSE

Frequency discrimination exists in each circuit of every piece of electronic equipment. All circuits will pass or restrain one group of frequencies to a greater degree than another range. The most that can be hoped for is that a circuit will affect all frequencies within a specific band in identical fashion.

FREQUENCY RESPONSE CURVES

Consider two basic circuits, each consisting of a resistor and a capacitor. In Fig. 8-1A, C is a capacitor with a reactance equal to:

$$X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C} \text{ ohms} \qquad (8\text{-}1)^*$$

where,

X_C is the capacitance reactance,
ω is the angular frequency equal to $2\pi f$,
π is a constant equal to 3.14,
f is the frequency in hertz,
C is the capacitance in farads.

Should the input voltage, V_{in}, be at a very high frequency, the reactance of the capacitor is small, and X_C, for all practical purposes, is equal to zero. The capacitor does not impede the current at high frequencies. The total input appears at the input. $V_{in} = V_{out}$.

When V_{in} is a dc voltage, and the frequency is zero, the reactance of the capacitor is infinite. There is no dc current through a capacitor. The total input voltage is across the capacitor. $V_{out} = 0$.

Between very high and very low frequencies, the capacitor behaves as an impedance that decreases as the frequency of the input signal rises. This frequency-discriminating phenemenon results in the gain curve shown in

(A) High-pass filter. (B) Low-pass filter.

Fig. 8-1. RC networks.

Fig. 8-2A. It is a plot of the ratio of output voltage to input voltage, expressed in dB.

An interesting point is that, at the frequency where V_{out} has dropped 3 dB from its maximum, f_o, the reactance of the capacitor is numerically equal to the resistor in the circuit. This frequency is:

$$f_o = \frac{1}{2\pi RC} \qquad (8\text{-}2)^*$$

The voltage has dropped 3 dB from its maximum at f_o. It dropped another 4 dB at $f_o/2$ and another 5dB at $f_o/4$. From there, it drops 6 dB each time f_o is reduced by a factor of 2. In other words, the output continues to drop at the rate of 6 dB per octave, after it has dropped the first 12 dB.

It can be considered in another way. After the output has dropped the first 12 dB, it continues to drop 20 dB each time the frequency is divided by 10. In other words, the output continues to drop at the rate of 20 dB per decade, after it has dropped the first 12 dB.

The approximation to the curve in Fig. 8-2A is shown in Fig. 8-2B. Here, it is assumed that the output has dropped 0 dB at f_o, and drops 6 dB per octave, or 20 dB per decade, for all frequencies below f_o. This approximation is frequently used in design work.

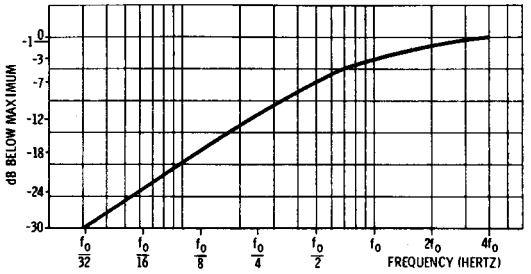
Equation 8-2 can also be used to determine f_o for the curve in Fig. 8-2C. This curve represents the output-to-input voltage ratio, expressed in dB, of the circuit in Fig. 8-1B. The eventual rolloff is at the rate of 6 dB per octave or 20 dB per decade. The approximate form is shown in Fig. 8-2D.

In all curves, the decibel is a way of noting the ratio between two voltages. It is a function of the ratio between the maximum output voltage to a lower voltage. Table 8-1 relates commonly used voltage ratios to their decibel equivalents.

In working with decibels, each time you multiply a voltage ratio, you add their equivalent in decibel notation. Thus $1.54{:}1 = 1.1{:}1 \times 1.4{:}1 =$ 1dB + 3dB = 4dB.

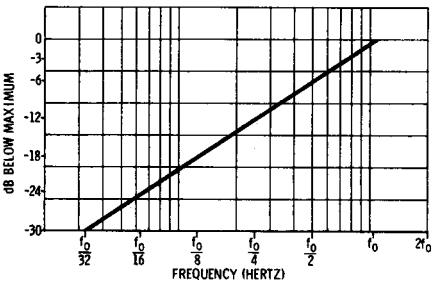
More Complex Curves

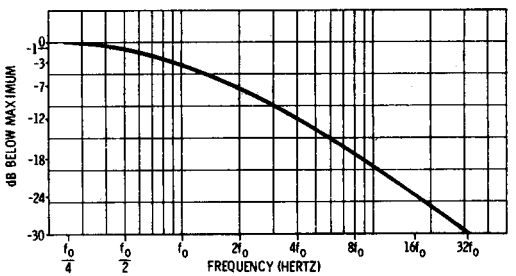
The circuits in Fig. 8-1A and 8-1B are the simplest types of high-pass and low-pass filters, respectively, possible with one resistor and one capacitor. They both provide a maximum of 6 dB per octave of attenuation.



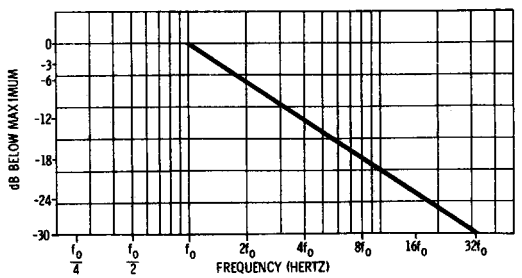
(A) Voltage versus frequency for RC filters.

(B) Approximation of Fig. 8-2A.





(C) Output-to-input voltage ratio of circuit in Fig. 8-1B.



(D) Approximation of Fig. 8-2C.

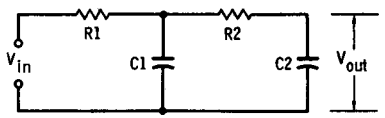
Fig. 8-2. Curves for RC filters.

Table 8-1. Relationship Between Voltage Ratio and dB Notation

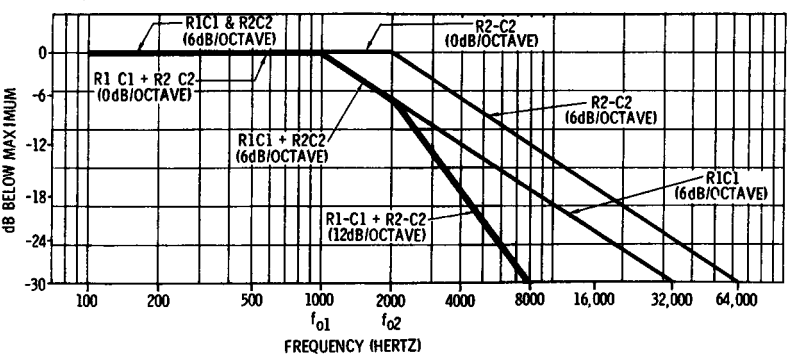
Voltage Ratio	dB
1.1 :1	1
1.4 :1	3
2 :1	6
2.24:1	7
3 :1	10
4 :1	12
6 :1	16
8 :1	18
10 :1	20
16 :1	24
32 :1	30
100 :1	40

Two or more such filters can be arranged in a circuit as shown in Fig. 8-3A. Here, f_{o1} for R1-C1 is $1/(2\pi$ R1 C1), and f_{o2} for R2-C2 is $1/(2\pi$ R2 C2). Assuming that f_{o1} is at 1000 Hz and f_{o2} is at 2000 Hz, the resulting approximate curves for the two values of f_o are as shown in Fig. 8-3B. The attenuation curves are first drawn for each RC network and are then added together. Each network contributes 6 dB per octave to the rolloff. Two such networks add up to a 12 dB per octave eventual rolloff. A similar circuit arrangement can be drawn for the high-pass filter. Other RC filter networks and their respective curves are shown in Fig. 8-4.

In the circuits discussed thus far, the output dropped to zero at either 0 Hz or ∞ Hz. The curve representing the characteristics of the circuit

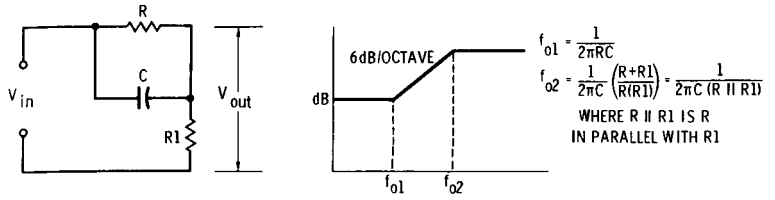


(A) Two low-pass filters.

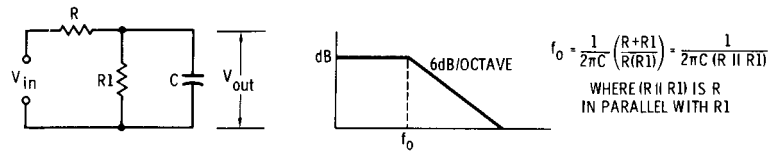


(B) Approximate curves for circuit in Fig. 8-3A.

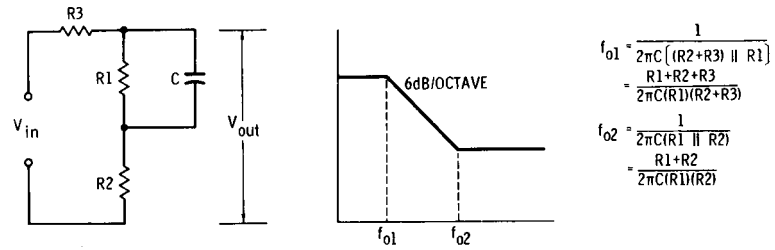
Fig. 8-3. Low-pass filters with associated curves.



(A) Variation of a high-pass filter and associated curve.



(B) Variation of a low-pass filter and associated curve.



(C) Low-pass filter with addition of R2.

Fig. 8-4. Low- and high-pass filters with associated curves.

in Fig. 8-4A does not drop to zero at any time. The minimum output remains at $V_{out} = V_{in}\ [R1/(R + R1)]$ until the first break-point or corner, f_{o1} Hz, is reached. From there, the output rises at the rate of 6 dB per octave until f_{o2} Hz. It remains constant from f_{o2} to infinite Hz.

In Fig. 8-4B, the output voltage is $V_{out} = V_{in}\ [R1/(R + R1)]$ until f_oHz. It then drops at the rate of 6 dB per octave.

The output voltage in Fig. 8-4C is $V_{out} = V_{in}\ [(R1 + R2)/(R3 + R1\ R2)]$ until f_{o1} is reached. Thereafter, it drops at the rate of 6 dB per octave until f_{o2}. The output voltage remains unchanged up to infinite hertz.

AN RC-COUPLED STAGE

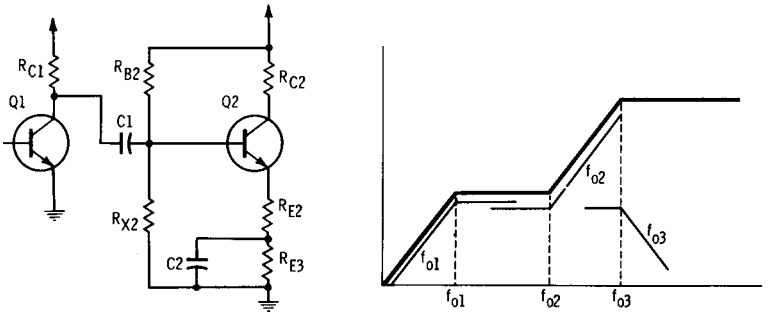
A typical RC-coupled stage is shown in Fig. 8-5A. The frequency response is affected by the various impedances in the circuit.

One breakpoint is due to the coupling circuit involving C1, the output impedance (R_{out}) of Q1, and the input impedance (R_{in}) of Q2. It is a

low-frequency rolloff similar to that produced by the circuit in Fig. 8-1A. The output voltage starts to drop at the rate of 6 dB per octave at the corner frequency, f_{o1} Hz. It continues dropping to 0 Hz.

$$f_{o1} = \frac{1}{2\pi C_1 (R_{in} + R_{out})} \tag{8-3}$$

The input impedance of Q2 is R_{B2} in parallel with R_{X2} in parallel with $\beta(R_{E2} + R_{E3} + r_e)$. The emitter resistance of Q2 is r_e. R_{E3} is negligible if the impedance of C2 is much smaller than R_{E2} at the frequency of f_{o1}. R_{out} is the output resistance of Q1 and is usually equal to R_{C1}.



(A) Capacitor-coupled amplifier. (B) Frequency response curve for Fig. 8-5A.

Fig. 8-5. Capacitive-coupled amplifier and associated curve.

A second corner frequency, f_{o2}, occurs when:

$$f_{o2} = \frac{1}{2\pi C_2 R_{E3}} \tag{8-4}$$

At this second frequency, the voltage starts to rise at the rate of 6 dB per octave.

At f_{o3}, the voltage begins to drop at the rate of 6 dB per octave, similar to the drop shown in Fig. 8-2C.

$$f_{o3} = \frac{1}{2\pi C_2}\left(\frac{R_{E3} + R_{EM}}{R_{E3} R_{EM}}\right) \tag{8-5}$$

where R_{EM} is the sum $R_{E2} + r_e +$ (resistance in base circuit)$/\beta$.

A typical curve of all these factors is shown in Fig. 8-5B. The thick line is the sum of the effects of the various curves; f_{o3} is larger than f_{o2} and f_{o1} can lie anywhere in the spectrum.

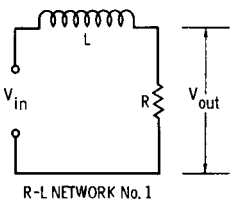
The calculations resulting from applying Equations 8-3 through 8-5 cannot be absolutely accurate due to the effect of capacitance reflected from the output of Q2 to its base circuit. The response curve must be checked in the laboratory when precise results are required.

A TRANSFORMER-COUPLED STAGE

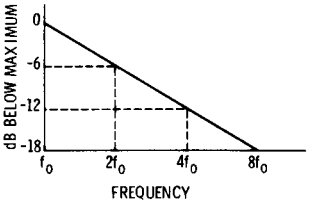
The RC networks can be replaced with their dual RL networks using a resistor and an inductor in each circuit. In Fig. 8-6, two RL networks are shown with their approximate curves. The corner frequency for an RL network is:

$$f_o = \frac{R}{2\pi L} \qquad (8\text{-}6)^*$$

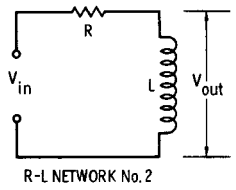
A transformer is an inductance. The frequency rolls off at both ends of the band due to the transformer in a circuit. The corner frequencies can be found with the help of Fig. 8-7 and Equation 8-6.



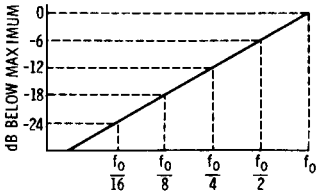
(A) RL network No. 1.



(B) Frequency response curve for circuit in Fig. 8-6A.

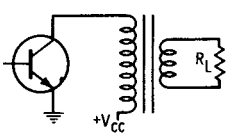


(C) RL network No. 2.

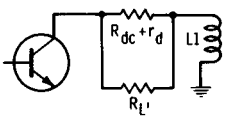


(D) Frequency response curve for circuit in Fig. 8-6C.

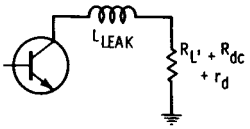
Fig. 8-6. RL networks and associated curves.



(A) Circuit with output transformer.



(B) Low-frequency rolloff for Fig. 8-7A.



(C) High-frequency rolloff for Fig. 8-7A.

Fig. 8-7. Output transformer and illustration of rolloff.

The major factors limiting the low frequencies are the inductance of the primary of the transformer and the load resistor, R_L, as reflected into the primary.

The inductance of the primary winding of the transformer is L1. The inductance of a coil, when reduced by the presence of dc current in the winding, is known as the incremental inductance. Substitute the incremental inductance for L into Equation 8-6 when determining a corner frequency.

Let R_L' be the resistance reflected into the primary due to R_L. According to Equation 6-7, $R_L' = (N_1/N_2)^2 R_L$, where N_1/N_2 is the turns ratio of the primary to the secondary of the transformer.

R_p is all the resistance in the primary circuit. It is the sum of all the resistance presented to the transformer by the transistor, and the dc resistance, R_{dc}, in the primary winding. In this case, it is about equal to r_d.

R_L' in parallel with $r_d + R_{dc}$ in conjunction with the incremental inductance, are the components determining the low-frequency characteristics of the circuit. The parallel resistance combination should be substituted for R in Equation 8-6. L in the equation is the incremental inductance. The equivalent circuit is shown in Fig. 8-6C and the curve is that shown in Fig. 8-6D.

To determine the characteristics at the high-frequency end of the spectrum, the leakage inductance must be considered. It is a stray inductance in series with the primary winding of the transformer. The leakage inductance is measured by checking the primary inductance when the secondary winding is shorted.

Add R_L' to r_d and R_{dc}. Substitute this for R and the leakage inductance for L in Equation 8-6 to determine the corner frequency at the high end of the band. The equivalent circuit is shown in Fig. 8-6A and the curve is shown in Fig. 8-6B.

In reality, there are a number of stray capacitors resonating with the leakage inductance. These produce bumps in the response, and rolloffs proceed at the rate of 12 dB per octave. The overall frequency response of the circuit should be determined by measurement rather than calculation if all factors are to be considered.

CONSTANT-K FILTERS

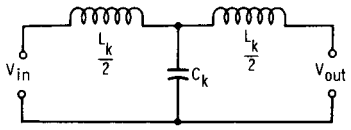
Filters are used in various circuits either to favor or exclude one frequency or group of frequencies. They can readily be adapted to transistor circuits.

The constant-K and m-derived filters discussed in this and the next two sections, involve a considerable amount of mathematical derivations. None of these will be presented here. Only the practical results of the complex mathematics will be considered. The components to be used in a circuit, the frequency characteristics, and how to use these filters to best advantage in a circuit are all the data the designer requires.

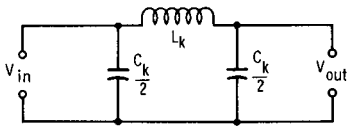
It will be assumed throughout the discussion, that the capacitors used in the filter circuits have very low dissipation factors. The entire Q is dependent on the inductors.

Filters usually take one of two forms—the T or π. The constant-K low-pass filters using both T and π arrangements are shown in Fig. 8-8.

A perfect low-pass filter does not attenuate or even affect the signal from 0 Hz to a cutoff frequency, f_c Hz. There is attenuation from f_c Hz to ∞ Hz. In practical filter circuits, the transition from the attenuation band to the conduction band is not as sharp as the definition would imply.



(A) Low-pass constant-K filter (T-section).



(B) Low-pass constant-K filter (π-section).

(C) Low-pass constant-K filter curves (T and π).

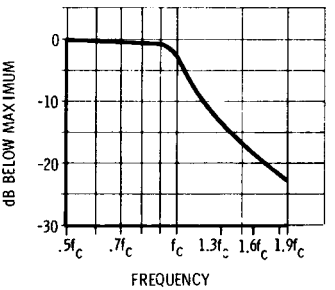


Fig. 8-8. Low-pass constant-K filters.

If the filter is terminated at both ends (input and output) in a load resistor equal to R ohms, the equations to find L_k and C_k in Figs. 8-8A and 8-8B are:

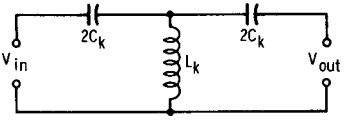
$$L_k = R/3.14f_c \qquad C_k = 1/3.14f_cR \tag{8-7}$$

The frequency response of both filter circuits is shown in Fig. 8-8C. The curve is relatively unaffected by the Q of the coil.

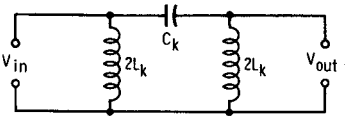
The constant-K high-pass filter attenuates frequencies from 0 Hz to f_c Hz, and passes frequencies from f_c Hz to ∞ Hz. The T and π sections are arranged as in Figs. 8-9A and 8-9B, respectively. The attenuation curve is shown in Fig. 8-9C. The curve, as in the case of the low-pass filter, is relatively unaffected by the Q of the coil. Here,

$$L_k = R/12.56f_c \qquad C_k = 1/12.56f_cR \tag{8-8}$$

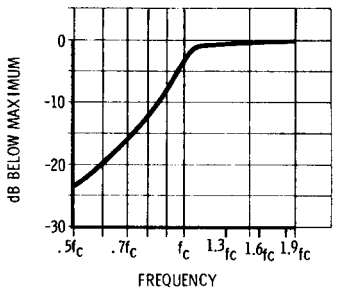
A bandpass filter attenuates frequencies from 0 Hz to F_1 Hz, and from f_2 Hz to ∞ Hz. It passes all frequencies between f_1 Hz and f_2 Hz. The



(A) High-pass constant-K filter (T-section).



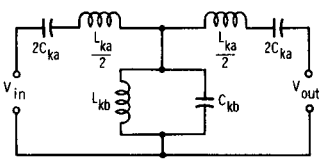
(B) High-pass constant-K filter (π section).



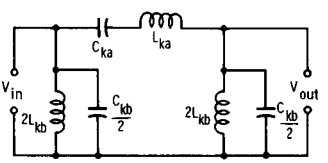
(C) Curve of rolloff of constant-K high-pass filter.

Fig. 8-9. High-pass constant-K filters.

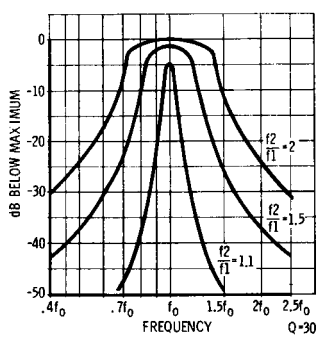
T-section and π-section arrangements of the bandpass constant-K filter are shown in Fig. 8-10. The attenuation curves are shown in Figs. 8-10C and 8-10D. Here, the Q of the coils does affect the curves. Curves for circuits using coils with Q's of 30 and Q's of 100 are shown in Figs. 8-10C and



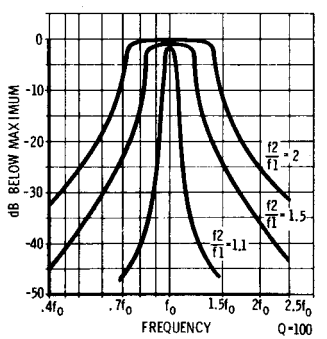
(A) Constant-K T section bandpass filter.



(B) Constant-K π section bandpass filter.



(C) Bandpass filter curve where Q = 30.



(D) Bandpass filter curve where Q = 100.

Fig. 8-10. Constant-K bandpass filters.

8-10D, respectively. Curves for other values of Q may be interpolated from these two drawings.

The sharpness of the attenuation characteristic is a function of the ratio of f_2:f_1. A range of curves for three different f_2:f_1 ratios is shown in Figs. 8-10C and 8-10D. The curves for other ratios may be interpolated from the drawing. The frequency f_o Hz, is a frequency between f_1 Hz and f_2 Hz, and is equal to $\sqrt{f_1 f_2}$.

The various components for the filter can be derived from the equations:

$$\begin{aligned} L_{ka} &= R/3.14(f_2 - f_1) & L_{kb} &= R(f_2 - f_1)/12.56 f_1 f_2 \\ C_{ka} &= (f_2 - f_1)/12.56 f_1 f_2 R & C_{kb} &= 1/3.14R(f_2 - f_1) \end{aligned} \qquad (8\text{-}9)$$

where R is the load resistance on either side of the filter.

The band-rejection filter attenuates frequencies between f_1 Hz and f_2 Hz while passing frequencies between 0 Hz and f_1 Hz and between f_2 Hz and ∞ Hz. The T-section and π-section circuits of this filter are shown in Figs. 8-11A and 8-11B, respectively. Here,

$$\begin{aligned} L_{ka} &= R(f_2 - f_1)/3.14 f_1 f_2 & L_{kb} &= R/12.56(f_2 - f_1) \\ C_{ka} &= 1/12.56R(f_2 - f_1) & C_{kb} &= (f_2 - f_1)/3.14 f_1 f_2 R \end{aligned} \qquad (8\text{-}10)$$

The curves for the various ratios of f_2:f_1 are shown in Fig. 8-11C and Fig. 8-11D.

THE M-DERIVED FILTERS

If sharper rolloff characteristics are required than are available from constant-K circuits, m-derived filters may be used.

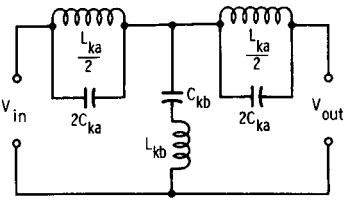
The following drawings and equations indicate the relationship between the components used in constant-K circuits and the components used in m-derived circuits. They are related to each other by a number, m, which can be any value between 0 and 1. When it is 1, the equation reverts to the constant-K form. When m is equal to 0.6, the match between the filter and the resistor load has been optimized. This is the assumed value in the discussion that follows.

The low-pass forms of the m-derived T sections and π sections are shown in Figs. 8-12A and 8-12B, respectively. The resulting attenuation curve is shown in Fig. 8-12C.

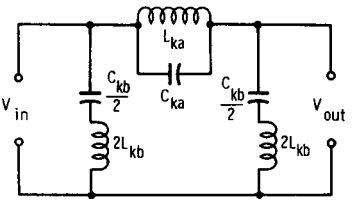
The components are related to L_k and C_k, derived above for the constant-K filter in Equations 8-7:

$$\begin{aligned} L_{ma} &= 0.6L_k & L_{mb} &= 0.267L_k \\ C_{ma} &= 0.267C_k & C_{mb} &= 0.6C_k \end{aligned} \qquad (8\text{-}11)$$

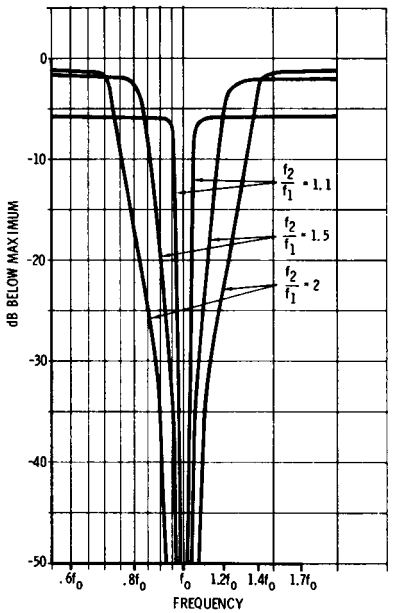
The same component values are used in the two end sections for the T and π arrangements. These are shown in Figs. 8-12D and 8-12E, respec-



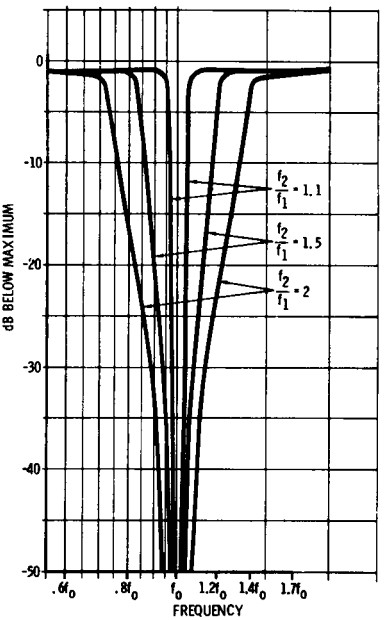
(A) T section constant-K band-elimination filter.



(B) Constant-K π section band-elimination filter.



(C) Band-elimination filter curve where Q = 30.



(D) Band-elimination filter curve where Q = 100.

Fig. 8-11. Constant-K band-elimination filters.

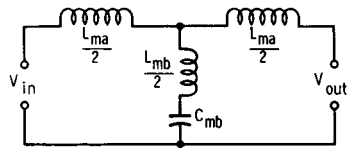
tively. The use of the end sections will be detailed later. It should be noted, however, that the curve in Fig. 8-12C is the result of using two end sections, and does not represent the effect of one end section by itself.

The high-pass m-derived T section and π section are shown in Figs. 8-13A and 8-13B. The curves for these circuits are shown in Fig. 8-13C. The end sections for use with the T filters are shown in Fig. 8-13D, while those for use with the π filters are shown in Fig. 8-13E.

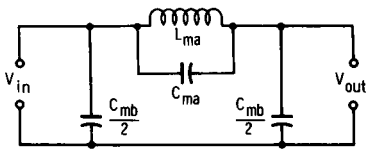
The components are related to those derived for the constant-K filter. Refer to Equation 8-8 to determine L_k and C_k.

$$\begin{aligned} L_{ma} &= 3.75L_k \qquad L_{mb} = 1.66L_k \\ C_{ma} &= 1.66C_k \qquad C_{mb} = 3.75C_k \end{aligned} \tag{8-12}$$

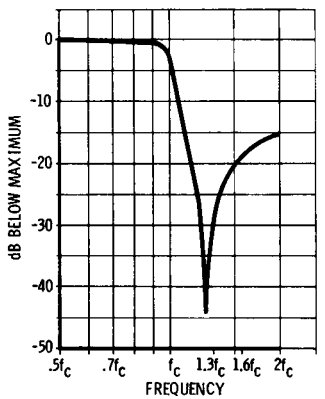
The T and π sections of the m-derived bandpass filter are shown in Figs. 8-14A and 8-14B, respectively. The curves plotting the variation of gain with frequency are shown in Figs. 8-14C and 8-14D. As before, $f_o = \sqrt{f_1 f_2}$. In each case, the curves for the different values of f_2:f_1 have been shown. In Fig. 8-14C, the Q of the coil is about 30, while in Fig.



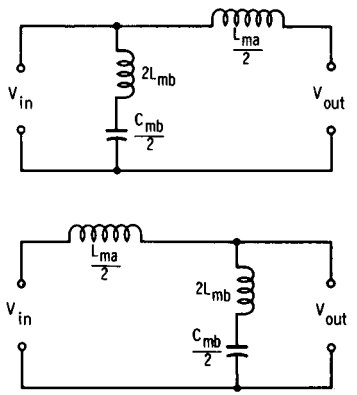
(A) Low-pass m-derived T section filter.



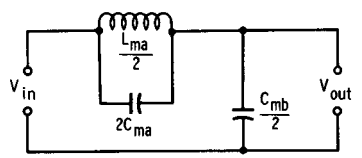
(B) Low-pass m-derived π section filter.



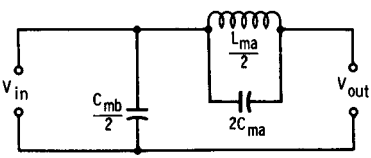
(C) Frequency response curve for low-pass m-derived filter.



(D) End sections for use with T filters.



(E)

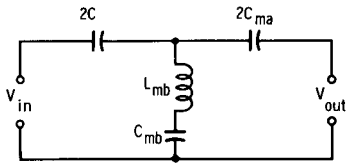


(E) End sections for use with π filters.

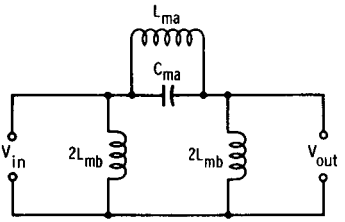
Fig. 8-12. Low-pass m-derived filters.

8-14D it is about 100. The attenuation characteristic for circuits with intermediate values of Q may be interpolated from the two sets of curves. The end sections for use with the T filter are shown in Fig. 8-14E, and the end section for use with the π filter is shown in Fig. 8-14F.

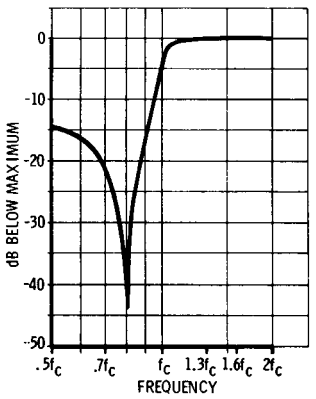
The components in the circuit are related to those derived in Equation 8-9:



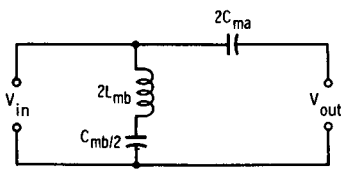
(A) High-pass m-derived T section filter.

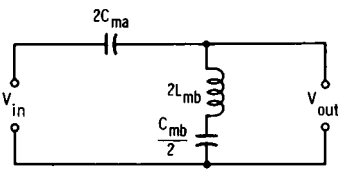


(B) High-pass m-derived π section filter.

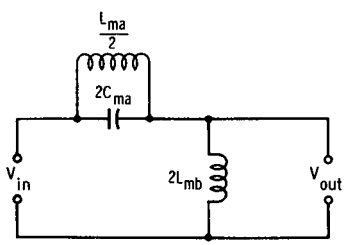


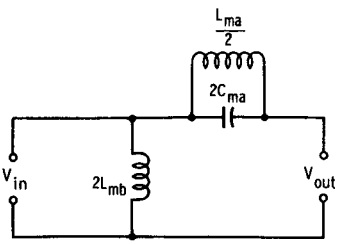
(C) Frequency-response curve of high-pass m-derived filters.





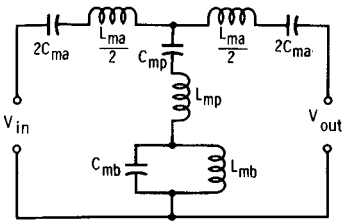
(D) End section for use with T filter.



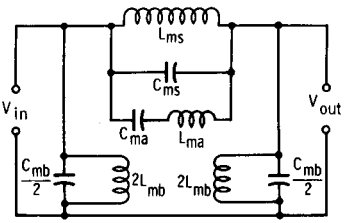


(E) End section for use with π filter.

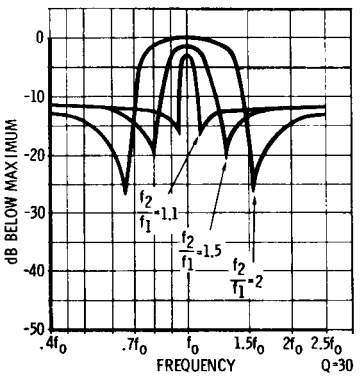
Fig. 8-13. High-pass m-derived filters.



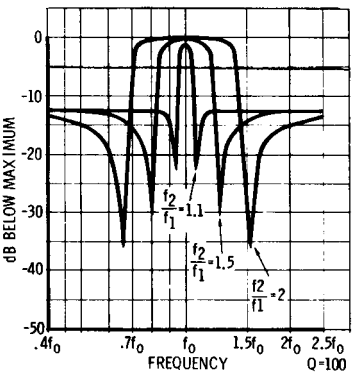
(A) T section.



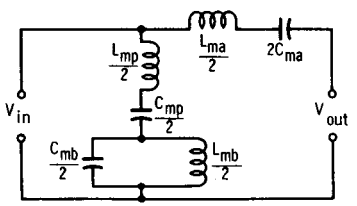
(B) π section.

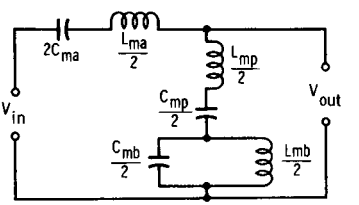


(C) Frequency response curve where $Q = 30$.

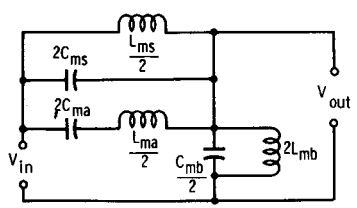


(D) Frequency response curve where $Q = 100$.

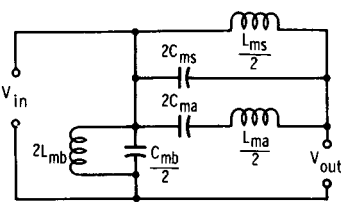




(E) End section for use with T filters.



(F)

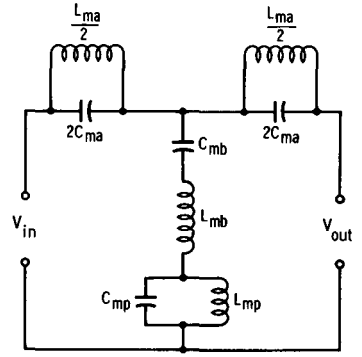


(F) End section for use with π filters.

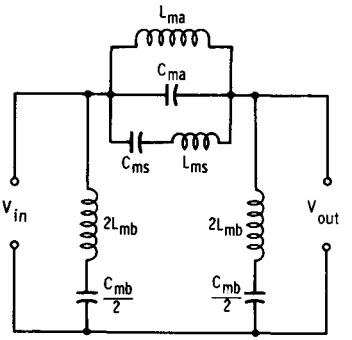
Fig. 8-14. M-derived bandpass filters.

$$L_{ma} = 0.6L_{ka} \qquad L_{mb} = 1.66L_{kb}$$
$$L_{mp} = 0.267L_{ka} \qquad L_{ms} = 3.75L_{kb}$$
$$C_{ma} = 1.66C_{ka} \qquad C_{mb} = 0.6C_{kb}$$
$$C_{mp} = 3.75C_{ka} \qquad C_{ms} = 0.267C_{kb} \qquad (8\text{-}13)$$

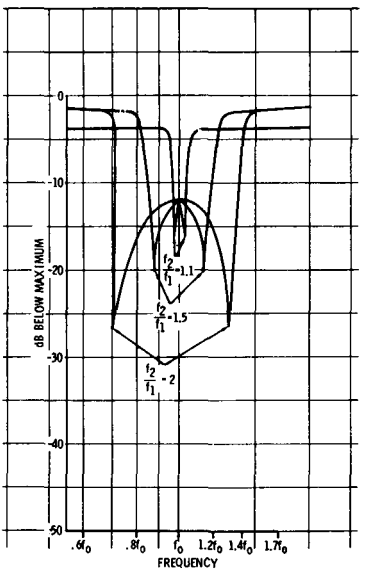
The T and π sections of the m-derived band-rejection filter are shown in Figs. 8-15A and 8-15B, respectively. The gain curves at the different frequencies and for three values of $f_2:f_1$ are shown in Fig. 8-15C and



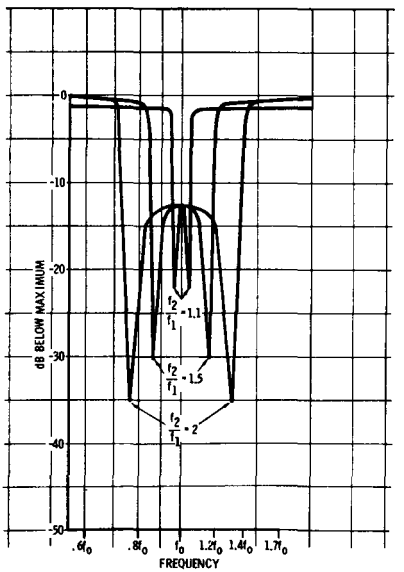
(A) T section.



(B) π section.



(C) Frequency response curve where Q = 30.



(D) Frequency response curve where Q = 100.

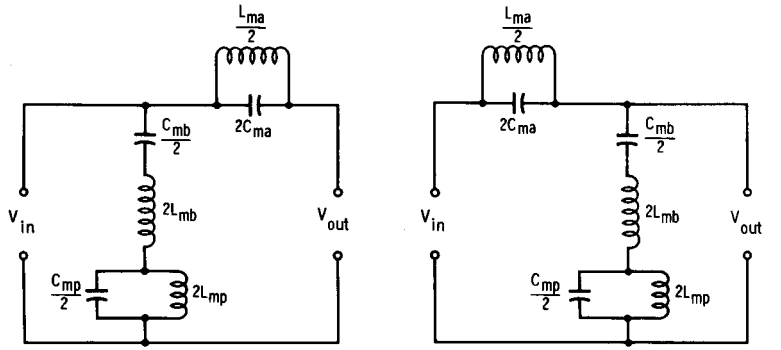
Fig. 8-15. M-derived

8-15D. In Fig. 8-15C, the Q of the coil is about 30, while in Fig. 8-15D it is about 100. The curves for different Q's may be found by interpolation. The end sections for use with the T filter are shown in Fig. 8-15E, and the end sections for use with the π filter are shown in Fig. 8-15F.

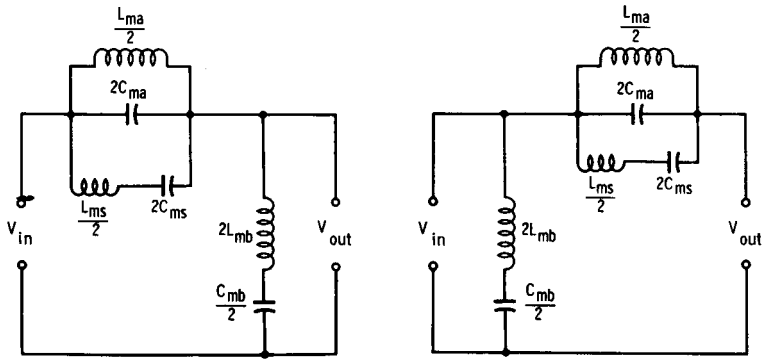
The components are related to those derived in Equation 8-10. Substitute the numbers into Equation 8-13.

DESIGNING A FILTER

Filters are designed so that they will match the resistance of the generator at the input and the resistance of the load at the output. The design is simplified if the load and generator have the same resistances. The equations listed previously assume this to be the case. A resistor value, midway between the input and output resistance, can be used for substitution into



(E) End sections for use with T filters.



(F) End sections for use with π filters.

band-elimination filters.

the equations as a compromise. However, the characteristic curves will vary somewhat from those shown in the drawings.

The input and output matching requirements are relatively easy to accomplish with transistor circuits. A filter may be fed from the collector circuit of a transistor. The input or generator resistance can be controlled by simply placing the proper resistor load in the collector.

The input resistance of a transistor following the filter is the output load on the filter. This resistance is controlled and adjusted so that the circuit will present the proper resistance to the output of the filter. In a transistor circuit the resistances seen by the filter at the input and output can be readily adjusted to nearly any desired value.

A filter is usually flanked on both ends by a half section. The complete filter may take one of the forms shown in Fig. 8-16, as well as many variations of these arrangements.

In Fig. 8-16A, the basic form of the filter is shown. In design, the function of the filter must first be determined—low-pass, high-pass, bandpass, or band-rejection. Next, it must be decided whether T or π sections are to be used. To do this, the components to be used in both types are calculated. From these calculations, it can be determined which type will use the more practical and less expensive components. The choice of π or T filter is usually made on this basis.

The components to be used in the m section of the filter are determined in two steps. First, the sizes of the inductors and capacitors of the constant-K filters are calculated. Elements composing the m-derived arrangement are determined from the components used in the constant-K filter.

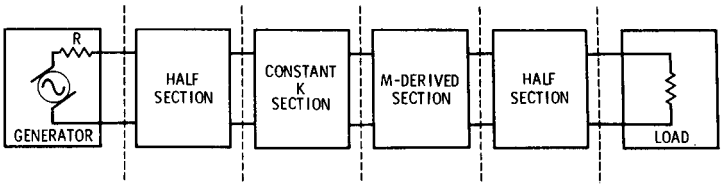
The various sections of the filter can then be arranged in a sequence as shown in Fig. 8-16A. The attenuation due to the entire filter is equal to the sum of the attenuations of each filter section.

As an example, assume that a high-pass filter is required. If the T section is to be used, the various parts of the filter are as shown in Fig. 8-16B. Should π sections be decided upon, the arrangement shown in Fig. 8-16C may be used.

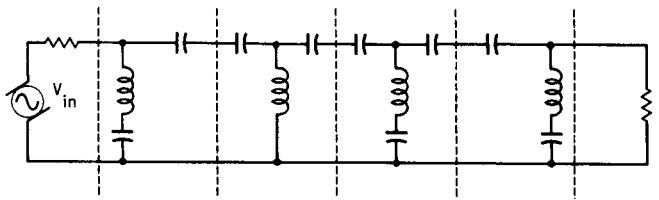
In Fig. 8-16B, two capacitors are connected in series at several points in the circuit. A single capacitor, equivalent in value to the two in series, may be used in place of the two components, in the final filter. Similarly, in Fig. 8-16C, a single inductor may be used to replace the two components connected in parallel. Should capacitors be connected in parallel and inductors in series, the appropriate substitutions may be made.

The attenuation due to each section of the filter may be determined from the applicable curves. The attenuation due to both half-sections is identical with that of one m-derived filter section.

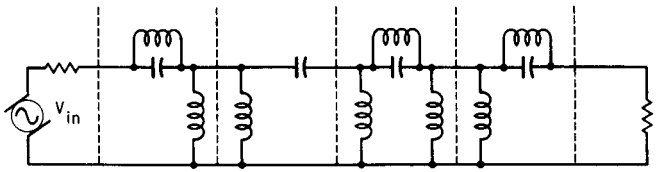
The arrangement shown in Fig. 8-16 can provide a considerable amount of attenuation. Should less attenuation be sufficient, a constant-K or m-derived section may be omitted. More sections may be added if additional attenuation is required.



(A) Block diagram of high-pass filter.



(B) Various parts of high-pass filter.



(C) Single inductors may be used to replace two inductors in parallel.

Fig. 8-16. Complete high-pass filter.

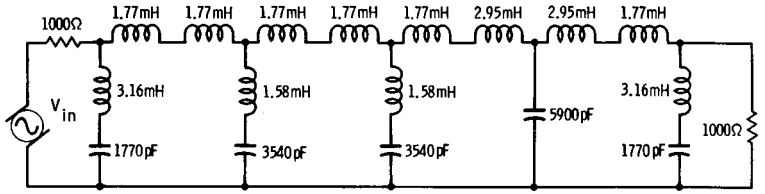
Let us now attempt a practical numerical problem. It is required in a particular application that only frequencies below 53,000 Hz be used. Attenuation must be 50 dB or more above 60 kHz.

A simple low-pass filter can be used to attenuate all frequencies above 60,000 Hz. From the curves in Figs. 8-8C and 8-12C, it can be noted that there is little attenuation until the frequency is $1.1f_c$. So let us make $1.1f_c$ equal to 60,000 Hz, the lowest frequency that must be reduced in amplitude. Then, f_c can be calculated to be 54,300 Hz.

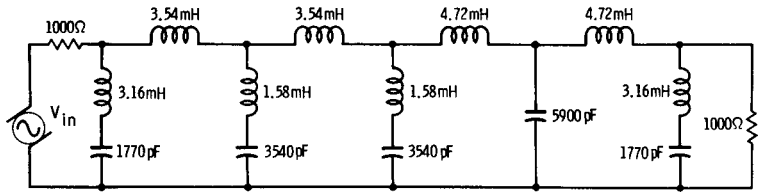
At 60 kHz ($1.1f_c$) each constant-K filter will attenuate the signal 7 dB (Fig. 8-8C) and each m-derived filter will attenuate it 15 dB (Fig. 8-12C). In order to get 50 dB or more attenuation at 60 kHz, at least three m-derived sections and one constant-K section should be used. In the actual filter, two m-derived sections and the end sections will make up the three required m-derived sections. The constant-K section is used for additional attenuation at 60 kHz, as well as to compensate somewhat for the rise in output of the m-derived section, as the frequency is increased.

For the sake of this example, use the T sections. Also assume that there is a 1000-ohm input and output resistance. This can easily be arranged if the filter is the coupling device between two transistors.

The constant-K sections from Fig. 8-8 and the inductors and capacitors determined from Equation 8-7, should be used. For the low-pass m-derived T section, use the designs in Fig. 8-12A and the two appropriate half-sections from Fig. 8-12D. The components are determined from Equation 8-11.



(A) Filter circuit showing component values.



(B) Final filter circuit with several components combined.

Fig. 8-17. Filter circuit.

In Fig. 8-17A, the raw filter is shown. In Fig. 8-17B, several components have been combined into single units.

It must be remembered that all filters discussed exhibit phase shift at different frequencies in the passband, in the stop band, as well as within the rolloff frequency range. Where this is important, more intense studies of the filters to be used should be made.

MODERN FILTERS

Good filters can be designed using the constant-K and m-derived curves and equations. However, new approximate techniques have been developed to design filters using charts and simplifying design procedures. Three different filters are currently in favor, each with a different characteristic.

The Butterworth filter has a smooth response in the passband and stop band. However, transition per number of components in the circuit, from the passband to the stop band, is not particularly sharp.

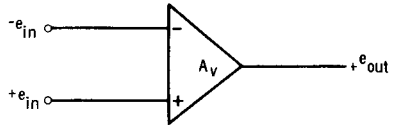
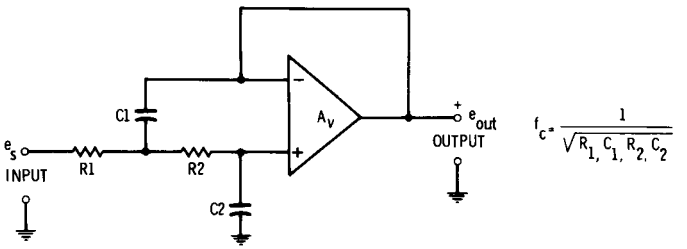
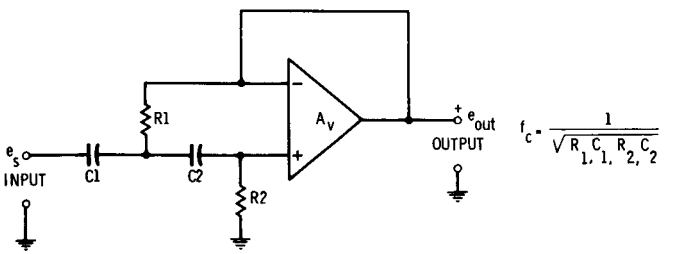


Fig. 8-18. Operational amplifier with differential inputs.

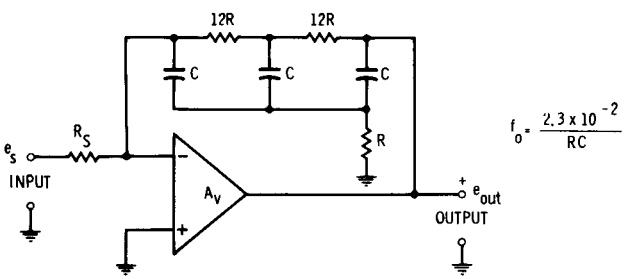
The Chebyshev filter has a smooth response in the stop band, but there is ripple in the passband. Hence, not all frequencies in the passband pass through the filter without some attenuation. However, the frequency cutoff is sharper than in the Butterworth design.



(A) Low-pass filter.



(B) High-pass filter.



(C) Bandpass filter.

Fig. 8-19. Feedback filters. R is in ohms and C is in farads.

The Cauer (elliptic function) filter has ripple in both the passband and the stopband. Here the transition between the two bands per number of components used is the sharpest.

The design of each of these filters is beyond the scope of this book. Detailed procedures and tables are available in the literature.

Filters are frequently placed into several feedback loops around amplifier stages. These are referred to as *active filters.* Some advantages over their passive counterparts are the possibility of extremely sharp transition between the passband and stop-band sections of the response, the elimination of the need for inductors, etc. As in the case with the passive filters discussed, active filters can be extremely complex to design from formulas and require extensive tables or curves for the more practical procedures. This information can be found in many of the publications available from filter manufacturers and in engineering periodicals. Space does not permit these curves to be presented here.

Feedback can simply be placed around an operational amplifier to perform various frequency-selective functions. Briefly, the gain of an operational amplifier with a differential input can be represented by a triangle with two inputs, as in Fig. 8-18. The output signal, $+e_{out}$, is out of phase with the signal fed to the upper input terminal, $-e_{in}$, and in phase with the signal fed to the lower input terminal, $+e_{in}$.

Drawings of low-pass and high-pass filters using the amplifier are shown in Fig. 8-19A and Fig. 8-19B, respectively, along with the frequency, f_c, at which the passband gain has rolled off 3dB. For the low-pass filter, the curve is similar to the one in Fig. 8-8C, and for the high-pass circuit it is similar to the one in Fig. 8-9C. The bandpass filter circuit and the formula to determine the center frequency is shown in Fig. 8-19C, while the curve is similar in form to one of those drawn in Fig. 8-10C. Note that none of the curves are identical (except by some unforseen coincidence) to those noted, but are referenced only to provide a general picture of the actual response.

Chapter 9

HIGH-FREQUENCY CONSIDERATIONS

In Chapter 5, two equivalent circuits, the equivalent "T" and the equivalent "h" were discussed.

A third equivalent circuit—the hybrid π—is useful in describing the high-frequency characteristics of the transistor. As you are aware, it is possible to change ordinary resistor or reactive circuits from delta (or pi) arrangements to the "T" form and back again. The same is true of circuits involving transistors. The various components in all equivalent circuits are interrelated.

THE HYBRID π EQUIVALENT CIRCUIT

A high-frequency equivalent circuit of the transistor is drawn in Fig. 9-1. The external base lead of the transistor is b. Inside the base, there is a point that cannot be reached by a lead. This point is b′; $r_{bb'}$ is the base spreading resistance between these two points. This resistance is relatively constant, although it does rise somewhat with collector-emitter voltage and temperature, while it decreases as the emitter current and frequency increase.

A resistance, $r_{b'e}$, shunted by a capacitance, $C_{b'e}$, connects the point inside the base to the emitter. The resistance, $r_{b'e}$ decreases as the collector current and temperature increase, and it increases as the collector-to-emitter voltage rises. $C_{b'e}$ remains relatively constant under all conditions.

A resistance, $r_{b'c}$, shunted by a capacitance, $C_{b'c}$, connects the point inside the base to the collector. Resistance $r_{b'c}$ is usually large enough, approaching infinity, to be omitted from the equivalent circuit. $C_{b'c}$ decreases as the collector current and collector-emitter voltage increase.

The transconductance, g_m, was discussed earlier. It is the change of collector current, ΔI_c, due to a change of base emitter voltage, ΔV_{be}. Mathematically it is:

$$g_m = \Delta I_c / \Delta V_{be} \qquad (9\text{-}1)$$

The current generator at the output of the transistor is $g_m V_{b'e}$. The resistance from the collector to the emitter is r_{ce}.

The α of the transistor varies with frequency. α_o is the low-frequency common-base current gain. At a frequency symbolized either by f_{hbo}, f_a, f_{ab}, or f_T, α has decreased 3 dB from its low-frequency value to $0.707\alpha_o$. This is the alpha cutoff frequency. Once α_o and f_a are known, α at any frequency can be found from the curve in Fig. 8-2C. In order to use this curve, substitute f_a for f_o on the horizontal axis. Note the ratio in dB at the frequency of interest. Find the voltage ratio represented by the dB ratio from Table 8-1 and multiply this fraction by α_o to determine α at the desired frequency.

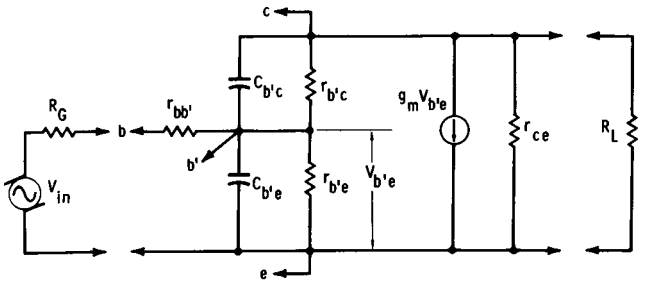


Fig. 9-1. Hybrid equivalent circuit.

Beta has decreased 3 dB from its low-frequency value at frequency $f_{\alpha e}$ or f_β. It is approximately equal to f_α/β_o, where β_o is the low-frequency common-emitter current gain at 1 kHz. At f_T (or f_α), β is 1. This frequency, f_T is also known as the gain-bandwidth product of the transistor, because it is equal to $f_\beta\beta$. As was the case with determining α at various frequencies, the β at a specific high frequency can also be determined from Fig. 8-2C.

Hybrid π Parameters

Many of the hybrid π parameters are difficult to measure. Instead approximate relationships have been derived between the hybrid π parameters and other factors and parameters more readily determined. The parameters are a function of the quiescent conditions and should be corrected for the conditions existing in the circuit in question. Some of these relationships are:

$$g_m = I_C/26 = 1/r_e \qquad (9\text{-}2)^*$$

where,

I_C is the quiescent collector current in milliamperes,

r_e is the emitter resistance.

$$C_{b'e} = g_m/2\pi f_\alpha \tag{9-3}$$

$$C_{b'c} \approx C_{ob} \tag{9-4}$$

where,

C_{ob} is the collector-to-base capacitance in the common-base equivalent circuit,

f_α is the alpha cutoff frequency.

$$r_{b'e} = \beta_o/g_m \tag{9-5}$$

where,

β_o is the current gain at low frequencies.

$$r_{bb'} = h_{ie} \tag{9-6}$$

Equation 9-6 is true at high frequencies. At low frequencies, $r_{b'e}$ should be subtracted from h_{ie}.

$$r_{b'c} = \beta_o/g_m h_{re} = r_{b'e}/h_{re} \tag{9-7}$$

$$r_{ce} = 1/(h_{oe} - g_m h_{re}) \tag{9-8}$$

See Chapter 5 for the definitions of the h parameters.

The above relationships can be used to great advantage in determining the voltage gain of a high-frequency circuit. The gain can be derived in different ways, each yielding a similar solution to a problem. In one method, we note that in the common-emitter mode of operation, the current gain is beta, corrected for the particular frequency involved. The voltage gain, A_v, of a common-emitter amplifier, is the ratio of the voltage between the collector and emitter, V_{ce}, to the voltage between the base and emitter, V_{be}. Stated mathematically and applying Ohm's law:

$$A_v = V_{ce}/V_{be} = I_C R_L/I_b R_i = \beta R_L/R_i \tag{9-9}$$

where,

R_L is the load resistor,

R_i is the input resistance,

I_c and I_b are the collector and base currents, respectively,

β is the common-emitter current gain, or the ratio of the change of the collector current, ΔI_C, to the change of base current, ΔI_B, at the specific frequency in question.

A second method for determining the gain makes use of the hybrid equivalent circuit in Fig. 9-1. In this circuit, there is a current generator at the output of the transistor, equal to $g_m V_{b'e}$, where g_m is the transconductance of the transistor and $V_{b'e}$ is the input voltage between a point inside the base and the emitter. The output voltage is developed across the load resistor, R_L, in parallel with r_{ce}. Because r_{ce} is much larger than R_L, r_{ce} is a negligible factor in calculating the output voltage. It is equal to:

$$V_{ce} = g_m V_{b'e} R_L \tag{9-10}$$

so that the voltage gain from a point inside the base to the output is:

$$A_v = V_{ce}/V_{b'e} = g_m R_L \qquad (9\text{-}11)^*$$

In a more general method the procedure is to find the gain at the midfrequencies using any of the equations studied in previous chapters. Then, find f_o, the frequency at which the midfrequency gain is down by 3dB. The voltage gain at any frequency above f_o can then be determined from the curve in Fig. 8-2C. It must be recalled that the curve continues to roll off at the rate of 6 dB per octave or 20 dB per decade beyond the −30 dB point shown on the curve.

The f_o must be determined from an equation based on the Miller effect. This equation can be derived from the following considerations.

The capacitance from point b′ to e in Fig. 9-1 is $C_{b'e}$. The impedance from b′ to c is $C_{b'c}$. The Miller effect states that in the equivalent circuit of a transistor, $C_{b'c}$ appears across $C_{b'e}$. But $C_{b'c}$ appears between b′ and e, multiplied by the voltage gain. The input circuit is shown in Fig. 9-2.

This circuit looks like the one in Fig. 8-4B. The high-frequency voltage gain is down 3 dB at the frequency f_o, when, from Equation 8-2:

$$f_o = \frac{1}{2\pi[(R_G + r_{bb'}) \,||\, r_{b'e}][C_{b'e} + C_{b'c} g_m R_L]} \qquad (9\text{-}12)$$

The output is down 3 dB at frequency f_o in Fig. 8-2C.

The current gain of the device itself can be determined from similar relationships. The output current is $g_m V_{b'e}$. The input current is the voltage between b′ and e divided by the impedance between b′ and e in Fig. 9-2. Refer to this impedance as $Z_{b'e}$. It includes the parallel combination of $C_{b'e}$, $C_{b'c} g_m R_L$, and $r_{b'e}$. The ratio of the output current to the input current is A_i.

$$A_i = \frac{g_m V_{b'e}}{V_{b'e}/Z_{b'e}} = g_m Z_{b'e} \qquad (9\text{-}13)^*$$

This information can be used in a practical example. Use the 2N3743 transistor. Here, $f_T = 30$ MHz, $\beta_o = 100$, $C_{ob} = 15$ pF and $h_{ie} = 40$ ohms. The idling current is 13 mA. This transistor feeds a 1000-ohm load. The input is 100 μV and the source impedance is $R_G = 30$ ohms. What is the voltage, current, and power gain at 700 kHz? Use the common emitter circuit. There is no emitter resistor.

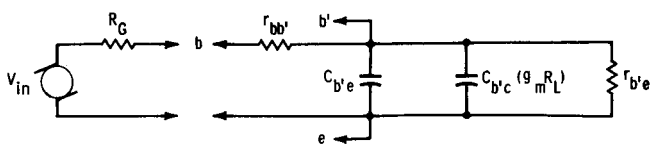


Fig. 9-2. Equivalent circuit of input including "Miller" effect.

First, calculate the factors to be substituted into Equation 9-12.

$R_G = 30$ ohms

$r_{bb'} = h_{ie} = 40$ ohms, from Equation 9-6.

$C_{b'c} = C_{ob} = 15 \times 10^{-12}$ farads, from Equation 9-4.

$g_m = I_C/26 = 13/26 = 0.5$ mho from Equation 9-2.

$r_{b'e} = \beta_o/g_m = 100/0.5 = 200$ ohms from Equation 9-5.

$C_{b'e} = g_m/2\pi f_T = 0.5/6.28(30 \times 10^6) = 2670$ pF, from Equation 9-3.

Substituting these factors in Equation 9-12, the voltage gain is 3 dB below the low-frequency gain when:

$$f_o = \frac{1}{2\pi[(30+40)||200][2670 \times 10^{-12} + (15 \times 10^{-12})(0.5)(10^3)]}$$
$$= 300{,}000 \text{ Hz.}$$

Fig. 8-2C and Table 8-1 show that the voltage gain at 700,000 Hz has dropped 8 dB or about 1/2.5 from the low-frequency gain. Also, f_β Hz is at $f_T/\beta = (30 \times 10^6/100) = 300{,}000$ Hz. It is only a coincidence here that f_o and f_β are at the same frequency.

Once again, according to Fig. 8-2C and Table 8-1, the current gain has dropped 8 dB or 1/2.5 from its low-frequency value at 700,000 Hz. The current gain is 1/2.5 of 100, or 40.

The low-frequency voltage gain is the ratio of the resistor in the collector lead to the resistance in the emitter. The resistor in the collis expressed in milliamps. This is $26/13 = 2$ ohms. The low-frequency voltage gain, which is the ratio of the two resistances, is $1000/2 = 500$.

This can also be determined from Equation 9-11: $g_m = 0.5$ and $R_L = 1000$. The voltage gain is $g_m R_L = 0.5(1000) = 500$. It checks with the formula using the ratio of collector impedance to emitter impedance.

At 700,000 Hz, the voltage gain is 1/2.5 of 500, or 200. The power gain, ignoring phase angle factors, is the current gain multiplied by the voltage gain, or $40 \times 200 = 8 \times 10^3$.

Results are approximate, but satisfactory in most instances. As in all work with transistors, the conclusions should be checked in the laboratory. Additional accuracy can be achieved if wiring capacity is added to $C_{b'e}$ and $C_{b'c}$.

Equation 9-12 changes little in form if an emitter resistor is included in the circuit. The emitter resistor, R_E, is reflected into the base circuit as a resistor equal to βR_E. This appears shunted by a capacitance equal to $[(C_{b'e} + C_{b'e}g_m(R_L + R_E)]/g_m R_E$. The input resistance is this combination added to $R_G + r_{bb'}$.

As for the Miller effect, $C_{b'c}$ now appears across $C_{b'e}$ as $C_{b'c}g_m(R_L + R_E)$. The new equation, after considerable manipulation, reduces to:

$$f_o = \frac{g_m(R_G + r_{bb'} + \beta R_E) + \beta}{2\pi\beta[R_G + r_{bb'} + R_E][C_{b'e} + C_{b'c}g_m(R_L + R_E)]} \qquad (9\text{-}14)$$

The frequency response is normally extended by use of the resistor in the emitter. This fact can be deduced when it is realized that the equivalent

of a parallel resistance-capacitance circuit shunts the emitter resistor. The RC network in the emitter emphasizes the high frequencies as demonstrated in Fig. 8-5, compensating somewhat for the rolloff.

RLC CIRCUITS

The equivalent circuit of an inductor can be drawn in two ways: as a resistor in series with the inductor, or as a resistor in parallel with the inductor. The equivalent circuits and their symbols are shown in Fig. 9-3.

An inductor stores energy in the magnetic field around the wires, and a capacitor stores energy by putting a stress on (polarizing) the dielectric material between the plates. Most of the stored energy can be returned to the rest of the circuit. The portion of the energy returned to the circuit depends on losses in the component, such as the resistance of the wire of the inductor. A single number, Q, describes the characteristic, indicating a figure of merit relating the amount of energy returned to a circuit to the amount of energy dissipated in the inductor or capacitor. For the series equivalent circuit of the inductor:

$$Q_L = 2\pi f L_s/R_s = 6.28\, f\, L_s/R_s \qquad (9\text{-}15)$$

where f is the frequency of the voltage impressed across the inductor and is normally referred to when specifying a coil. Similarly:

$$Q_L = R_p/2\pi f L_p = R_p/6.28\, f\, L_p \qquad (9\text{-}16)$$

for the parallel equivalent circuit. For practical values, the Q of the parallel equivalent circuit is equal to the Q of the series equivalent circuit.

Using these factors, the circuits in Fig. 9-3 can be converted from one form to the other. L_p, for all intents and purposes, is equal to L_s if Q is of

(A) Series representation of an inductor. (B) Parallel representation of an inductor.

Fig. 9-3. Representation of an inductor.

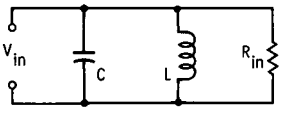
substantial size. In this discussion, they will be considered identical. R_p is related to R_s by the equation:

$$R_p = Q^2 R_s \qquad (9\text{-}17)$$

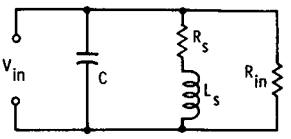
In the circuit in Fig. 9-4A, assume that a coil is to resonate with a capacitor at 200 kHz. The inductance is 5 mH or 5/1000 henry. The output of the resonant circuit is connected to the input of a transistor. The input

resistance, R_{in}, of the transistor is 100,000 ohms while the input capacitance is negligible compared to C. Determine C, Q_L (the Q of the inductor), and R_s of the inductor if the Q of the overall circuit is to be 10.

The circuit in Fig. 9-4A can be changed to that in Fig. 9-4B, where L is broken down into its equivalent series components, R_s and L_s. In Fig. 9-4C, the circuit is shown using the parallel equivalent form.



(A) Parallel resonant circuit.



(B) Fig. 9-4A with L broken down into its series components.

(C) Resistance across L_P, R_{in}.

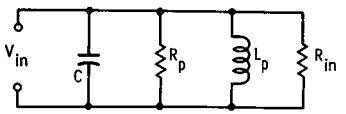


Fig. 9-4. Parallel resonant circuit and associated resistance.

Starting with the circuit in Fig. 9-4C, the resistance across L_p is R_{in} in parallel with R_p. Use the symbols $R_{in}||R_p$ to denote this combination. Since the Q must be about 10 for the circuit, $R_{in}||R_p = Q\,(2\pi)\,(f)\,(L_p) = 10(6.28)\,(2 \times 10^5)\,(5 \times 10^{-3}) = 62{,}800$ ohms, from Equation 9-16. R_p, from the equation of resistors in parallel, is equal to:

$$R_p = \frac{62{,}800\,R_{in}}{R_{in} - 62{,}800} = 169{,}000 \text{ ohms}$$

Using the values determined for R_p and L_p, the Q of the coil only, must be equal to:

$$Q_L = \frac{R_p}{6.28\,f\,L_p} = \frac{169{,}000}{6.28(2 \times 10^5)\,(5 \times 10^{-3})} = 27$$

(from Equation 9-16)

With Equation 9-17, R_s can be determined:

$$R_s = 169{,}000/(27)^2 = 230 \text{ ohms}$$

The resonant frequency, f_o, of the circuit can be found using the equation:

$$f_o = \frac{1}{2\pi\sqrt{LC}} \qquad (9\text{-}18)^*$$

where,

L is the inductance expressed in henrys,
C is the capacitance expressed in farads.

Applying this equation:

$$C = \frac{1}{(2\pi f_o)^2 L} = \frac{1}{[6.28\ (2 \times 10^5)]^2\,[5 \times 10^{-3}]} = 130\ \text{pF}$$

where,

pF is picofarads. $C = 130 \times 10^{-9}$ farads.

In a series resonant circuit, the voltage across the coil or capacitor is equal to QV_{in}, at the resonant frequency, V_{in} is the input voltage to the series combination. This relationship is the basis of theQ-meter.

On either side of resonance, the voltage across the inductor and capacitor drop. This is shown in Fig. 9-5. At two specific frequencies, f_L and f_H, the voltage will drop to 0.707 from the maximum output (3 dB). The bandwidth ($f_H - f_L$), resonant frequency, and Q_L are related by the equation:

$$Q_L = f_o/(f_H - f_L) \qquad (9\text{-}19)^*$$

The bandwidth in our problem is $f_H - F_L = f_o/Q_L = 2 \times 10^5/27 = 7.4 \times 10^3$ Hz. Hence, f_L is $(2 \times 10^5 - 7.4 \times 10^3/2)$ Hz, and f_H is $(2 \times 10^5 + 7.4 \times 10^3/2)$ Hz.

RC Circuits

The parallel R_p-C_p capacitor circuit is mathematically related to its series equivalent, as shown in Fig. 9-6. The equations are similar to those used in the conversions of the L-R circuits. It is assumed that the Q's in Figs. 9-6A and 9-6B are relatively large and equal. The errors incurred due to this assumption are usually negligible compared to other approximations frequently made for convenience.

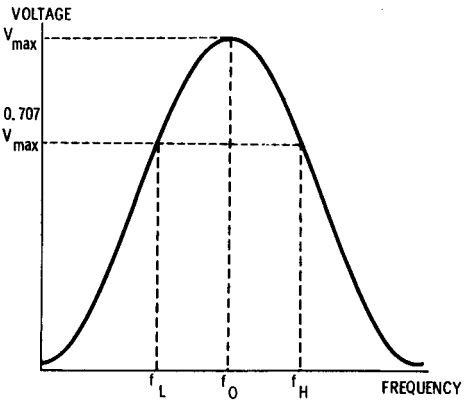
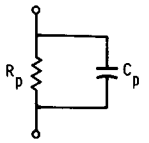
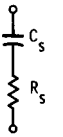


Fig. 9-5. Plot of bandwidth.



(A) Parallel R_p-C_p circuit.



(B) Series R_s-C_s circuit.

Fig. 9-6. Relationship of parallel R_p-C_p circuit to its series equivalent.

$$C_p = C_s \qquad (9\text{-}20)^*$$

$$R_p = Q^2 R_s \qquad (9\text{-}21)^*$$

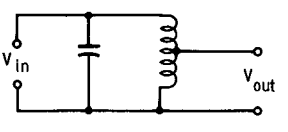
MATCHING WITH THE TUNED TRANSFORMER

In order to get good Q, the resonant circuit must not be shunted excessively. Schemes such as shown in Fig. 9-7 are employed with this goal in mind. These resonant circuits are normally connected between two transistor stages.

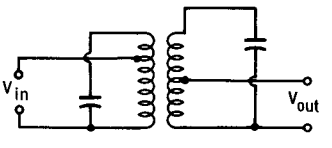
In Fig. 9-7A, V_{in} is fed from the relatively high output impedance of one transistor while V_{out} feeds the low input impedance of a second transistor. A typical circuit using this arrangement is shown in Fig. 9-8.

The total capacitance across all the turns of the coil consists of three capacitors:

1. The capacitor C,



(A) Circuit coupled from a high impedance (V_{in}) to a low impedance (V_{out}).



(B) Double-tuned circuit.

Fig. 9-7. Schemes for attaining high Q.

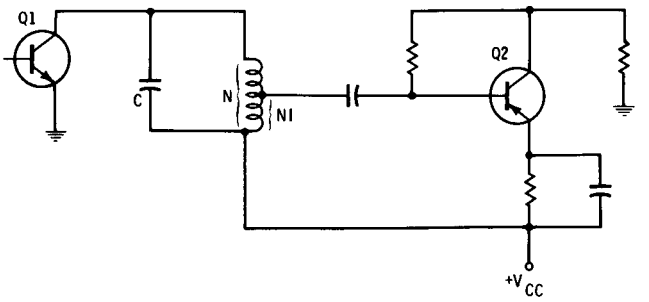


Fig. 9-8. Circuit using tapped coil for coupling.

2. The output capacitance of Q1, C_o,
3. The input capacitance to Q2, C_{in} multiplied by $(N/N1)^2$.

This is the ratio of the square of all the turns of the coil to the square of the turns from the tap on the coil to the $+V_{CC}$ supply. It is based on the conventional transformer impedance-matching equation.

It should be noted that C_o and C_{in} are complex functions of $C_{b'e}$, C_{ce}, f_o, $r_{b'b}$, etc. As a first (and sometimes a very wild) approximation, assume that $C_o = C_{ce}$ and $C_{in} = C_{b'e}$. But remember, these are only approximations. The actual capacitance may be very different and must be determined experimentally.

The turns ratio of the coil should be determined approximately from the equation:

$$(N/N_1)^2 = (R_o||R_p)/R_{in} \qquad (9\text{-}22)$$

where,

N and N_1 are the number of turns in the coil shown in Fig. 9-8,
R_o is the output resistance of Q1, equal approximately to r_d,
R_p is the parallel equivalent resistance of the coil across Q1. It is $Q_L^2R_s$ where R_s is the measured series equivalent resistance of the coil. Q_L is the Q of the coil itself.
R_{in} is the input resistance of Q2.

It is best to determine the proper ratios experimentally due to the difficulty in ascertaining the various factors to plug into Equation 9-22. Even if all these factors were precisely known, further experimental work would be required due to the leakage flux.

The double-tuned circuit in Fig. 9-7B is superior to the single-tuned one in Fig. 9-7A because it provides a sharper bandpass. As before, this arrangement requires tapped transformer windings to avoid excess loading of the tuned circuits.

INSTABILITY

The inputs and outputs of transistor circuits are connected through the internal mechanism of the device. Oscillation may occur.

One method of preventing oscillation is neutralization, in which a voltage is fed back to the base of the input transistor through a resistor, capacitor, or a parallel combination of the two, from a succeeding stage. The feedback voltage must be 180° out of phase with the signal at the base.

Another method of reducing the probability of oscillation is to shunt the output terminals of the transistor with a resistor. As an alternative, the load impedance can be made small.

A third method involves placing a resistor in series with one of the leads at the input of the transistor. An alternate method of accomplishing the same goal is to make the generator impedance large.

Chapter 10

FEEDBACK

In the discussion thus far, the characteristics of the transistor amplifiers were dependent on the transistor parameters. Gain, impedances, distortion, and other factors varied with β, r_e, $r_{b'b}$, etc. Feedback judiciously placed around a transistor can provide an amplifier with characteristics relatively unaffected by many of the parameters.

A feedback amplifier involves a sample of the output voltage or current fed back to the input. If a fed back voltage is applied out of phase and bucking the input signal, the feedback is negative and the overall gain of the amplifier is reduced. If the voltage fed back adds to the input signal, the overall amplifier gain is increased and the feedback is positive.

The signal fed back to the input can be related to either the output voltage or output current. In the former case, the system is known as voltage feedback, while in the latter case, it is obviously referred to as current feedback. A combination of the two types of feedback around one amplifier is known as compound feedback.

VOLTAGE FEEDBACK

The drawing in Fig. 10-1 represents a conventional transistor amplifier with a voltage gain of A_v. There is no feedback. Let V_{in} be the input voltage to the amplifier proper. Here, it is equal to V_s, the voltage supplied by the signal source. The output voltage is V_{out}, and the voltage gain of the amplifier stage is:

$$A_v = V_{out}/V_{in} \qquad (10\text{-}1)$$

Now, feed a portion of the output voltage back to the input (Fig. 10-2). This is known as series feedback since the signal fed back is applied in series with the input.

The portion of the output voltage fed back in series with the input is B. The portion of the input voltage, V_{in}, due to the output voltage is BV_{out}.

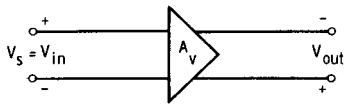


Fig. 10-1. Conventional transistor amplifier.

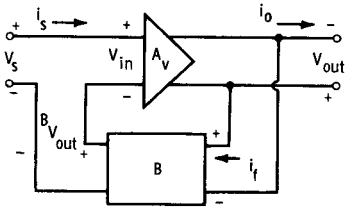


Fig. 10-2. Amplifier with voltage feedback.

In the figure, this voltage bucks the input signal, V_s. The voltage at the input to the amplifier proper, ignoring polarity, is:

$$V_{in} = V_s + B(V_{out}) \text{ or } V_s = V_{in} - B(V_{out}) \qquad (10\text{-}2)$$

The voltage gain of this circuit is:

$$A_f = \frac{V_{out}}{V_s} = \frac{A_v(V_{in})}{V_{in} - B(V_{out})} \qquad (10\text{-}3)$$

by substituting Equation 10-1 for the numerator and 10-2 for the denominator. Now, division of the numerator and denominator by V_{in} yields:

$$A_f = \frac{A_v}{1 - B\left(\frac{V_{out}}{V_{in}}\right)} = \frac{A_v}{1 - B(A_v)} \qquad (10\text{-}4)$$

which is the well-known feedback equation. The feedback factor is $[1 - B(A_v)]$. For negative or degenerative feedback, $B(A_v)$ is negative while for positive feedback arrangements, it is postive. With negative feedback, if $B(A_v)$ is much greater than 1, the gain of the overall circuit becomes 1/B. It does not vary with the gain of the amplifier so long as the product of the gain of the amplifier itself and B is in the order of magnitude indicated.

The noise and gain of an amplifier are reduced equally by a factor of $1/[1 - B(A_v)]$. Hence the signal-to-noise ratio remains unchanged with feedback.

There are many consequences of negative voltage when feedback is applied to an amplifier as shown.

The input impedance with voltage feedback, Z_{if}, is related to the input impedance without feedback by the relationship:

$$Z_{if} = Z_i[1 - B(A_v)] \qquad (10\text{-}5)$$

The output impedance with voltage feedback, Z_{if}, is related to the output impedance without voltage feedback, Z_o, by the relationship:

$$Z_{of} = Z_o/[1 - B(A_v)] \qquad (10\text{-}6)$$

Feedback also helps reduce distortion. The distortion with feedback, D_f, is related to the distortion without feedback, D, by the relationship:

$$D_f = D/[1 - B(A_v)] \qquad (10\text{-}7)$$

The bandwidth is likewise improved with inverse feedback. If the corner frequency (frequency at which the midband gain dropped 3 dB) of an amplifier is normally f_o, the corner frequency with feedback is f_{of}. They are related to each other by the equation:

$$f_{of} = f_o[1 - B(A_v)] \qquad (10\text{-}8)$$

for high frequencies. For low frequencies, Equation 10-8A applies:

$$f_{of} = f_o/[1 - B(A_v)] \qquad (10\text{-}8A)$$

Inverse feedback stabilizes the gain of an amplifier. Gain can vary radically (with parameters, temperature, components, etc.) in the amplifier shown in Fig. 10-1. This variation of gain is referred to as ΔA_v. Should feedback be applied, the change in gain is reduced to ΔA_f. Using the symbols previously assigned to gain with and without feedback, the variation in gain with feedback is related to the variation in gain without feedback by the equation:

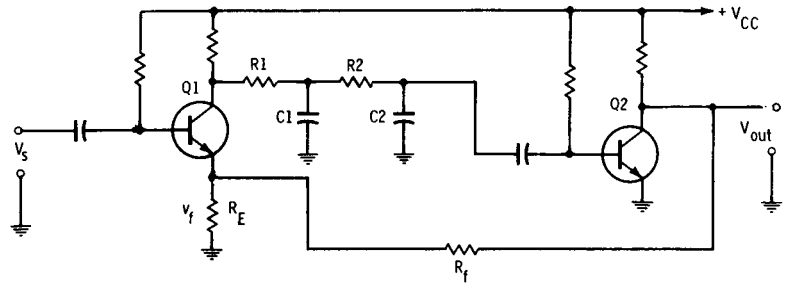
$$\Delta A_f = \frac{A_f}{A_v}\left(\frac{\Delta A_v}{1 - B(A_v)}\right) \qquad (10\text{-}9)$$

Amplifiers with feedback have a tendency to become unstable or to oscillate. There is no problem with stability if the feedback around an amplifier is negative at all frequencies. Once it turns positive, the amplifier may become marginally unstable or break into oscillation. Considering Equation 10-4, and assuming that $B(A_v)$ is equal to $+1$, the feedback is positive; the denominator in the equation is equal to zero, and the voltage gain with feedback is infinite. The amplifier becomes an oscillator.

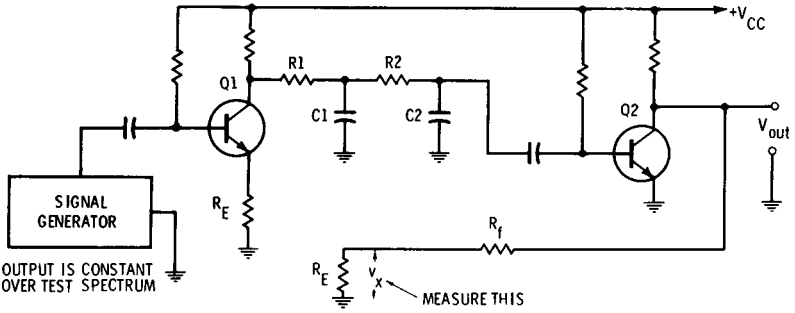
The probability of oscillation can be determined, with some accuracy, from the frequency response curve of the amplifier.

Using the two-stage amplifier in Fig. 10-3A as an example, assume that 20 dB of negative feedback is applied from the output at the collector of the second stage back to the emitter of the first. R1-C1 and R2-C2 are two networks producing high-frequency rolloff at the eventual rate of 12 dB/octave. The feedback loop is completed to the input through R_f, developing a voltage, V_f, across R_E to buck V_s.

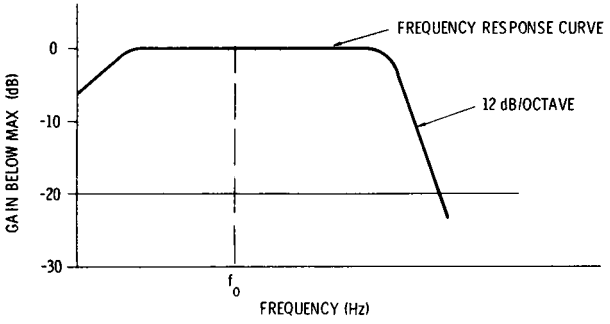
First, check the frequency response in the forward loop. To do this, disconnect R_f from the junction of the emitter and R_E. Substitute another resistor equal to R_E from R_f to ground. Feed a signal to V_s and measure the voltage, V_x, across the new R_E, as the frequency of the input signal generator is varied. The setup is shown in Fig. 10-3B. A plot of the frequency response of the forward loop, using this setup, is shown in Fig. 10-3C.



(A) Practical feedback amplifier.



(B) Method of measuring feedback.



(C) Frequency response of practical feedback amplifier.

Fig. 10-3. Practical amplifier with feedback.

The feedback with the loop closed in Fig. 10-3A is, let us say, supposed to be 20 dB. It can be checked as follows. At a midfrequency, note V_{out} in Fig. 10-3B. Now reconnect the feedback loop as in Fig. 10-3A: V_{out} should have dropped 20 dB or to 1/10 of the value first measured.

On Fig. 10-3C, draw a line 20 dB below maximum gain or flat frequency response. Note the rate of the rolloff as the frequency response

curve crosses the line indicating −20 dB. If this rate is less than 12dB/ octave, the amplifier is stable.

CURRENT FEEDBACK

With reference to Fig. 10-2, the voltage fed back to the input depends on the output voltage. In current-feedback amplifiers, the voltage fed back to the input depends on or is related to the output current. A drawing of this is shown in Fig. 10-4. The current is sampled as a voltage across R_T. A portion of the voltage, B, developed across the resistor, is

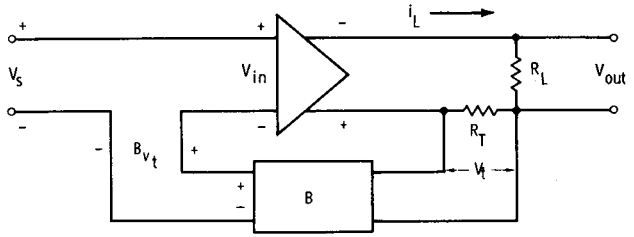


Fig. 10-4. Current feedback amplifier.

fed back to the input. If R_T is adjusted so that the required amount of voltage is fed back, the divider network determining B is not necessary. It has already been set by the size of R_T. When there is current feedback, the voltage gain of the circuit can be derived as follows:

The input signal voltage, V_s, is equal to the voltage at the input to the amplifier proper minus the voltage fed back.

$$V_s = V_{in} - B(V_t) \tag{10-10}$$

The voltage gain of the amplifier without feedback is, as stated in Equation 10-1,

$$V_{out} = A_v(V_{in}) \tag{10-1}$$

The voltage gain of the amplifier with feedback is,

$$A_f = \frac{V_{out}}{V_s} = \frac{A_v(V_{in})}{V_{in} - B(V_t)} \tag{10-11}$$

But

$$V_t = i_L R_T = \left(\frac{V_{out}}{R_L}\right) R_T \tag{10-12}$$

So that Equation 10-11 becomes,

$$A_f = \frac{A_V V_{in}}{V_{in} - \left(\frac{R_T}{R_L}\right) B(V_{out})}$$

$$= \frac{A_v}{1 - \left(\frac{R_T}{R_L}\right) B(A_v)} \qquad (10\text{-}13)$$

If there is no divider network between R_T and the input, B is made equal to 1.

The quantity $\frac{R_T}{R_L}$ B in Equation 10-13 can be assigned the symbol γ (gamma). If $\gamma(A_v)$ is much larger than 1, the voltage gain of the overall circuit is $1/\gamma$.

The effect of negative current feedback on an amplifier differs from the effect of negative voltage feedback only in that the former causes the output impedance to increase by the size of the feedback factor $[1 - \gamma(A_v)]$ while the latter causes it to decrease by the size of the feedback factor, $[1 - B(A_v)]$.

It is frequently desirable to determine the effect of the input signal voltage on the output current, when the amplifier employs current feedback. This feedback circuitry is applied to electronic voltmeters. Referring to Fig. 10-4, the load current, i_L, can be shown to be equal to the ratio of V_s to R_T, assuming that the amount of feedback is substantial.

SHUNT FEEDBACK CIRCUITS

Up to this point, series feedback has been considered. The signal fed back to the input was applied in series with the input signal source. In the shunt feedback circuit, the signal is fed back so that it is in parallel with the input signal source. Shunt feedback is frequently used in transistor circuits. An example of this is a feedback resistor connected from the collector to the base in a common-emitter circuit.

Everything mentioned thus far with reference to negative or inverse voltage series feedback also applies to inverse shunt feedback. But there is one exception. The input impedance is reduced by a factor $[1 - B_i(A_i)]$, where A_i is the current gain of a circuit before feedback is applied and B_i is the portion of the output current fed back to the input.

The circuit in Fig. 10-5 has been discussed with reference to Fig. 3-8, describing a biasing technique. The circuit is a shunt feedback arrangement returning a portion of the output signal to the base.

It may be considered in two ways. As a voltage feedback circuit, the output from the collector is split between R_B and the input impedance of the transistor, Z_i. In this case, B equals $Z_i/(R_B + Z_i)$. If R_B is much larger than Z_i, as is almost always the case, B is Z_i/R_B.

As a current feedback circuit, the collector current is split between the load resistor, R_C, and the base resistor, R_B. The portion of the current fed back to the base, B_i, is $R_C/(R_B + Z_i)$. Again assuming that R_B is much

Using numbers in Fig. 10-5, assume that R_C is 1300 ohms and that there is 1 mA of current through the collector circuit. The emitter resistance is 26/1 mA = 26 ohms. If V_{CC} is 2.6 volts, the voltage at the collector is 2.6 volts − 1 mA × 1300 ohms = 1.3 volts. Letting $\beta = 100$, the quiescent base current is 1 mA/100 = 10^{-2} mA. R_B must then equal 1.3 volts/10^{-2} mA = 1.3 × 10^5 ohms. The input impedance is $\beta(r_e) = 100(26) =$ 2600 ohms. Assume that R_G, the resistance of the signal source, is 100 ohms.

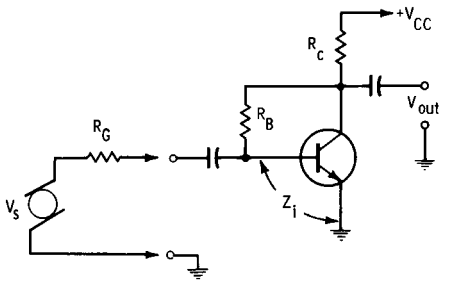


Fig. 10-5. Feedback circuit previously used for bias stabilization.

larger than Z_i, B_i becomes R_C/R_B. If $B_i(A_i)$ is large, A_{if}, the current gain with feedback, is R_B/R_C.

The voltage gain of the transistor circuit, excluding the effects of the resistance of the signal source and the feedback resistor, is $R_C/r_e = 1300/26 = 50$. This is A_v.

B, the voltage fed back, is Z_i/R_B. Z_i is the input impedance, 2600 ohms, in parallel with the 100-ohm source resistance, R_G. The equivalent parallel resistance of the two is 96 ohms. Since R_B is 130,000 ohms, B is 96/130,000 ≈ 1/1300.

The voltage gain with feedback is:

$$A_f = \frac{50}{1 + 50\left(\frac{1}{1300}\right)} = \frac{50}{1 + 0.038} = 48$$

Evidently, the voltage gain remains relatively unchanged when shunt feedback is added to the circuit. However, the current gain varies considerably. The current gain of the transistor without feedback is $\beta = 100$. Because of $B_i = R_C/R_B = 1300/130{,}000 = 1/100$, the current gain with feedback is:

$$A_{if} = \frac{100}{1 + 100\left(\frac{1}{100}\right)} = 50$$

It should be noted here that shunt feedback of the type illustrated in Fig. 10-5 can be placed around three stages. The feedback resistor con-

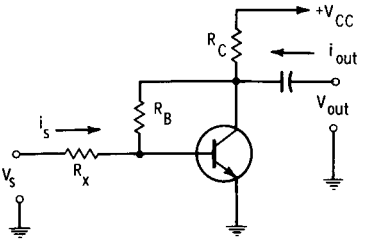


Fig. 10-6. Operational amplifier circuit.

nects the collector of the third transistor to the base of the first. The equations are identical with those used in the one-stage example, except that here the current gain without feedback is equal to the product of the current gains of the three stages.

The operational amplifier drawn in Fig. 10-6 is a variation of the shunt feedback circuit. In this circuit, it can be shown that the impedance between the base and ground is practically zero (virtual ground). If the gain of the amplifier stage is sizable, $V_{out}/V_s = R_B/R_X$ and $i_{out}/i_s = R_X/R_B$. The phase shift is 180° between the input and output.

Another shunt feedback arrangement is shown in Fig. 10-7. Here, B_i, the portion of the output current fed back, is equal to R_E/R_B. If $B_i(A_i)$ is much greater than 1, the current gain is equal to R_B/R_E. As in all shunt feedback arrangements, the input impedance with feedback is $Z_i/(1 - B_iA_i)$, where Z_i is the input impedance without feedback.

Should it be necessary to measure the forward gain of the amplifier without feedback, disconnect R_B from the emitter of Q2. Connect R_B to ground so that the bias on Q1 will not be upset.

As in all shunt feedback arrangements the voltage gain is only slightly affected by feedback. It is pronounced only when the feedback is very large.

SERIES FEEDBACK CIRCUITS

Another circuit we encountered previously is shown in Fig. 10-8. A portion of the collector current is sampled across the emitter resistor. The portion of the signal fed back for use in Equation 10-13 is $B(R_T/R_L) = \gamma = R_E/R_C$. If $A_v\gamma$ is large, $A_f = R_C/R_E$.

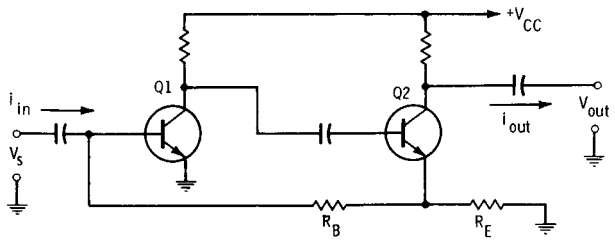


Fig. 10-7. Current feedback around two stages.

Using the conditions of the previous problem, assume that there is 1 mA of collector current, so that $r_e = 26$ ohms. Also, let $R_C = 1300$ ohms and $R_E = 104$ ohms. If R_E were not in the circuit (a short), the voltage gain is $R_C/r_e = 50$. Since $\gamma = R_E/R_C = 104/1300$, the voltage gain with feedback is:

$$A_f = \frac{50}{1 + 50\left(\frac{104}{1300}\right)} = \frac{50}{1+4} = 10$$

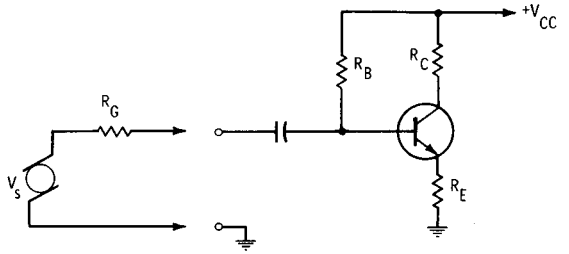


Fig. 10-8. Feedback circuit also used for bias stabilization.

Throughout the previous chapters, it was assumed that voltage gain is the ratio of $R_C/(R_E + r_e)$. Substituting the components of this circuit into the previously assumed relationship, gain is $1300/(104 + 26) = 10$. This result agrees with that determined using feedback theory. Current gain is relatively independent of the resistor in the emitter.

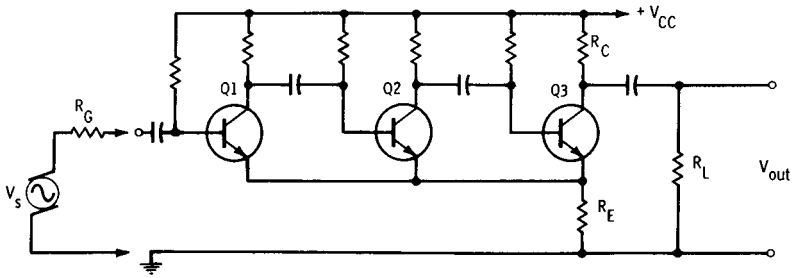
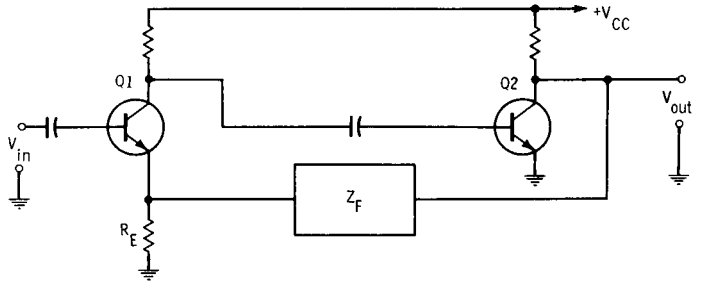


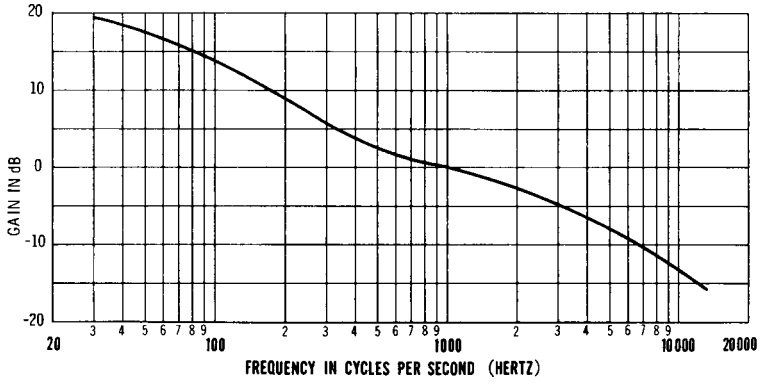
Fig. 10-9. Current feedback over three stages.

The emitter resistor may be common to more than one transistor stage, as in Fig. 10-9. Here, $\gamma = R_E/R_C$. If A_v is large, A_f is R_C/R_E. Should there be a load, R_L, across the output, γ becomes $R_E/(R_C||R_L)$ and the voltage gain is $(R_C||R_L)/R_E$ where $R_C||R_L$ is the equivalent resistance of R_C in parallel with R_L.

As before, the current gain is relatively unaffected by the presence of R_E.



(A) Feedback pair used in magnetic cartridge preamplifier circuit.



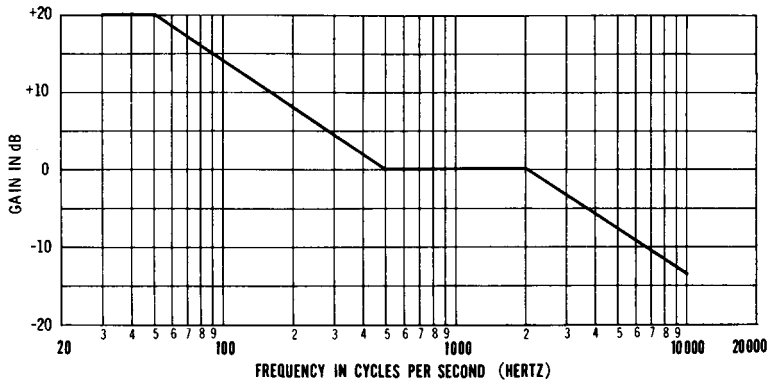
(B) Preamplifier frequency-response curve.

Fig. 10-10. Preamplifier

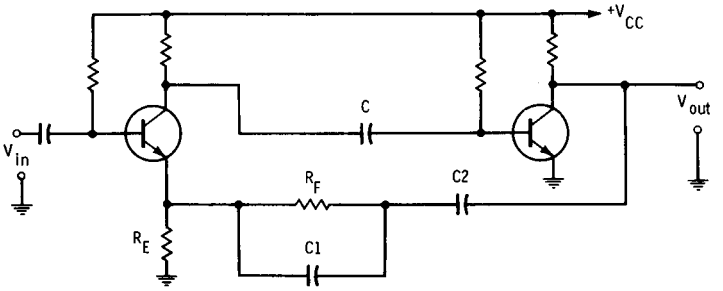
A popular circuit used in preamplifiers for magnetic phonograph cartridges is shown in Fig. 10-10A. The voltage at the output of the second transistor is fed back to the emitter of the first. Equation 10-4 is used to determine the gain of the circuit with feedback, where $B = R_E/Z_F$. If the gain in the forward loop is large, the gain with feedback is Z_F/R_E.

Z_F may be a resistor. In this case, gain is identical at all frequencies. Should it be desirable to have the gain vary with frequency, a reactive frequency discriminating circuit can be used to replace Z_F. For example, if Z_F is made into a capacitor, more high frequencies than low frequencies are fed back. Hence, the voltage gain of the overall circuit with feedback will be greater at the low frequencies than at the high frequencies.

The required frequency response for reproduction of the signal from a magnetic phonograph cartridge is shown in Fig. 10-10B. A straight line approximation to this curve has been drawn in Fig. 10-10C. This follows the format of the curve and approximations used in Fig. 8-2C. In Fig. 10-10C the gain is flat from 0 to 50 Hz, drops at the rate of 6 dB/octave to 500 Hz, is flat to 2100 Hz, and then drops again at the rate of 6 dB/



(C) Approximation of Fig. 10-10B.



(D) Preamplifier circuit showing R_F, C1, and C2 and in place of Z_F.

feedback.

octave. The circuit with the closed feedback loop in Fig. 10-10D will provide an amplifier whose characteristics follow the contour of the standard curve.

If the product of A_v and B is much greater than 1, the gain of the amplifier is Z_F/R_E. Z_F is $X_{C2} + (R_F||X_{C1})$, where $R_F||X_{C1}$ is the symbol for R_F in parallel with X_{C1}. X_{C1} and X_{C2} are the reactances of C1 and C2 respectively. After mathematical manipulation, Z_F is found to equal:

$$Z_F = \frac{1 + j\omega(R_F)(C1 + C2)}{j\omega(C2)(1 + j\omega(C1)(R_F)} \qquad (10\text{-}14)$$

where j shows a phase shift of 90° and $\omega = 6.28f$. The corner frequency is denoted by f.

The voltage gain with feedback is:

$$A_f = \frac{Z_F}{R_E} = \frac{1 + j\omega(R_F)(C1 + C2)}{j\omega(C2)(R_E)\,[1 + j\omega(C1)(R_F)]} \qquad (10\text{-}15)$$

To determine the corner frequency with an equation like Equation 10-15, each factor in the form of $(1 + jZ)$ must be made equal to $(1 + j)$. All other factors are equal to zero. For the numerator:

$$1 + j\omega(R_F)(C1 + C2) = 1 + j$$

and one corner frequency is:

$$f_1 = 1/[2\pi(R_F)(C1 + C2)] \qquad (10\text{-}16)$$

Two other corner frequencies can be determined from the denominator:

$$j\omega(C2)(R_E) = 0$$
$$f_o = 0 \qquad (10\text{-}17)$$

and:

$$1 + j\omega(C1)(R_F) = 1 + j$$
$$f_2 = 1/[2\pi(C1)(R_F)] \qquad (10\text{-}18)$$

Equation 10-17 indicates that the gain starts to drop at zero frequency and continues to f_1 Hz, as determined from Equation 10-16. In the curve in Fig. 10-10C, $f_1 = 500$ Hz. It drops again at f_2 Hz, determined from Equation 10-18. This is 2100 Hz for the curve in question.

In the typical circuit in Fig. 10-10D, R_E can be made equal to 200 ohms and R_F can be made equal to 33,000 ohms. According to Equation 10-18, $C1 = 1/[6.28(2100)(33{,}000)] = 2300$ pF and from Equation 10-16, $C2 = 1/[2\pi(500)(33{,}000)] = 9700$ pF. This assumes that C2 is much larger than C1. C, the coupling capacitor, can be made small so that the gain will not continue to rise below a frequency of 50 Hz. These components, adjusted more carefully in the laboratory, can produce the exact curve shown in Fig. 10-10B.

FEEDBACK AND THE RF CIRCUITS

Agc (automatic gain control) in a receiver is designed to maintain a constant average audio output or video contrast, regardless of the strength of the rf signal. Agc does not utilize feedback in the same sense as feedback has been discussed thus far. However, information is fed back from later stages in a receiver to the earlier rf and i-f amplifiers.

The signal strength is sensed and filtered after the second detector. It is fed back as a constant voltage to the bases of the mixer and amplifiers. The gain of a transistor varies with emitter current and collector voltage, when these are small. Hence, the rectified voltage applied to the base will control the rf gain.

Squelch circuits are used to silence a receiver until the received signal rises to a useful level, compared to the noise. They are also useful in reducing noise when tuning from one station to another.

A squelch transistor is connected to the first amplifier stage in such fashion as to cut it off. When the signal on the squelch transistor reaches

a predetermined magnitude, it turns on the first amplifier stage. The signal to do this job can be obtained from the agc line. The size of the signal required to turn on the circuit is adjusted with a threshold control.

The afc (automatic frequency control) provides for automatic readjustment of an oscillator frequency, if it should shift from its original setting. An arrangement to fulfil this function is frequently used to control the frequency of the rf oscillator in fm receivers and the horizontal oscillator in TV sets.

In the conventional fm radio system, the received signal is mixed with that of the local oscillator signal to form a difference frequency. This should be at the i-f frequency in a superheterodyne radio. A frequency detector at the end of the i-f chain produces an output proportional to the difference between the actual mixed signal and the required i-f signal. The polarity of the output indicates whether the difference frequency is greater or less than the i-f frequency. This voltage is then fed back to the oscillator where a transistor or diode is a capacitive element in the tank circuit. The voltage fed back controls the capacity of the diode or transistor, affecting the resonant frequency of the tank circuit and hence the frequency of oscillation.

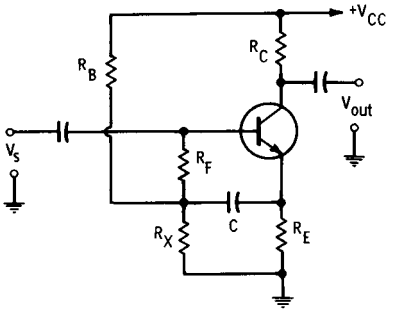
BOOTSTRAPPING

The size of the input impedance of a conventional common-emitter or common-collector circuit is limited by the bias resistors. The input impedance must always be less than the size of the resistor in the base circuit. The circuit in Fig. 10-11A provides a means of increasing the effective input impedance by using positive feedback, through C, from the emitter to the base. The gain of the overall loop is always less than one.

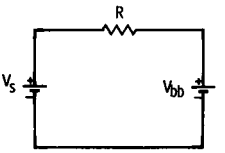
The operation of a bootstrap circuit can be understood with the help of Fig. 10-11B. If V_{bb} is shorted, the signal voltage, V_s, sees an impedance equal to $R = V_s(1/i_s)$, where i_s is the current through the circuit. If a voltage, V_{bb}, is added to the circuit, the current through the circuit is $i = (V_s - V_{bb})/R$, so that the impedance offered to V_s is $V_s(1/i) = V_s[R/(V_s - V_{bb})]$. If V_{bb} is made approximately equal to V_s, the denominator approaches zero and the impedance presented to V_s approaches infinity.

This is just what happens in Fig. 10-11A when the input signal voltage, V_s, and the voltage at the emitter (which is approximately equal to the voltage at the base) are applied at the two ends of R_F. It makes R_F appear much larger than it actually is. As R_F is between the bias resistors and the input, the input sees the impedance across R_F added to the impedances in the rest of the circuit.

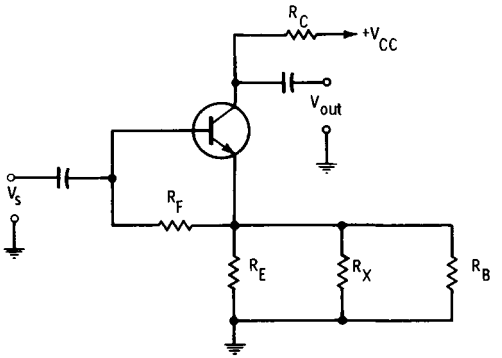
A reasonably accurate analysis involves Fig. 10-11C. C is large enough to be considered a short circuit at all frequencies involved. V_{CC} is at ac signal ground. Hence, R_B, R_X, and R_E are effectively in parallel with each other while R_F is in parallel with the base-emitter resistance of the tran-



(A) Bootstrap circuit.



(B) Illustration of feedback.



(C) Analysis of impedance of Fig. 10-11A.

Fig. 10-11. Bootstrap circuit and feedback.

sistor. If you even assume the base-emitter resistance to be equal to zero, shorting R_F, the input impedance is equal to $(R_B||R_X||R_E)\beta$, where $R_B||R_X||R_E$ is the symbol for the equivalent resistance of all three resistors connected in parallel.

FEEDBACK OSCILLATORS

It was indicated early in the discussion that if the feedback is positive and $B(A_v)$ is made equal to 1, that the gain with feedback is infinite. In this case, no ac input signal is required to produce an output. The amplifier is in a state of instability or sustained oscillation.

In a feedback oscillator, the gain of the amplifier and feedback loop must be equal to or must be greater than 1. The phase must be such that the signal fed back must add to any signal present at the input of the amplifier. One stage of amplification provides 180° phase shift. The other 180° must be supplied by the circuit around the amplifier. The sum of the two is 360°, making the phase at the input and output identical. There

must also be some frequency-selective circuit. This circuit should determine the one frequency at which the phase shift and gain are of the proper magnitude to produce oscillation.

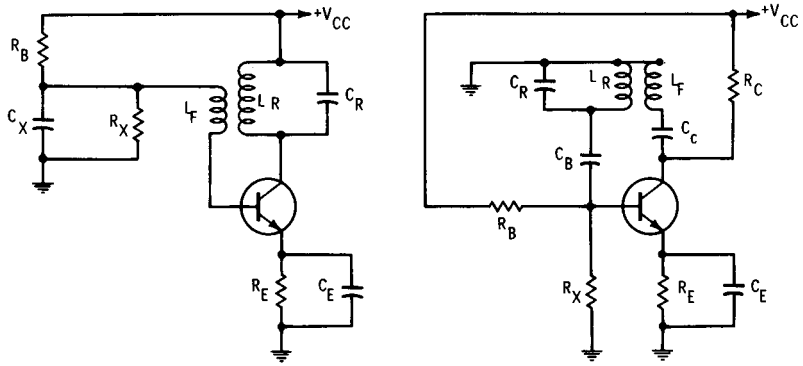
The magnitude of the sinusoidal oscillations is limited by the linear swing of the amplifier although rf oscillators are frequently biased class B or C for greater efficiency. In the latter instances, the transistor must be in a conducting mode to start the oscillations. It then transfers to a class-C mode of operation as the oscillations build up. The transfer from one mode to the other is accomplished through the use of an RC network in the emitter-base diode circuit. A voltage developed across the combination while the circuit is oscillating tends to reverse-bias the diode driving the transistor into the cutoff region for a large portion of the cycle.

In the feedback oscillator in Fig. 10-12A, a parallel resonant circuit formed by C_R and L_R is in the collector of the transistor. At resonance, $f_o = 1/2\pi\sqrt{L_R C_R}$, the impedance in the collector circuit is at a maximum and the phase shift due to the overall circuit is zero, or 360°. Any signal that may appear in the collector circuit (caused by random noise, voltage changes, etc.) is coupled inductively into the tickler coil, L_F, located near L_R. This signal is fed to the base of the transistor, where it is amplified and returned to the collector. The phase of the two inductors are arranged so that the feedback from the collector circuit to the base is positive. The circuit will oscillate at the resonant frequency.

Resistors R_B and R_X establish the bias voltage, while R_E is used for dc stabilization. C_E and C_X serve bypass functions.

The description of the circuit in Fig. 10-12B is identical to that just discussed, with the exception that the resonating components are in the base circuit.

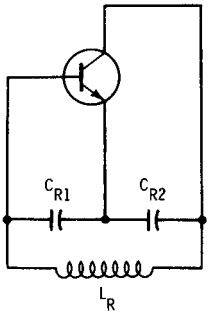
Other LC oscillator circuits are possible with capacitors or inductors to feed a portion of the output signal back to the input. A number of these



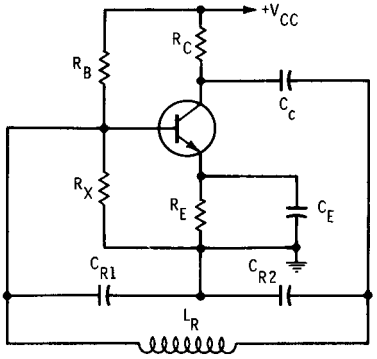
(A) Series feedback tuned-collector oscillator.

(B) Shunt feedback tuned-base oscillator.

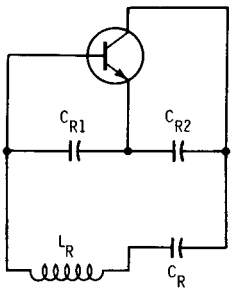
Fig. 10-12. Series and shunt feedback.



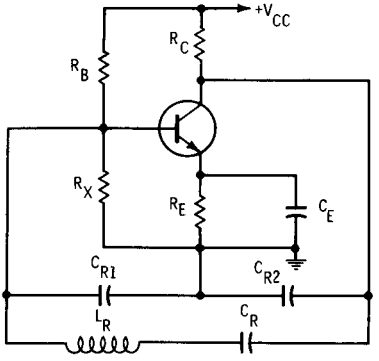
(A) Basic Colpitts oscillator.



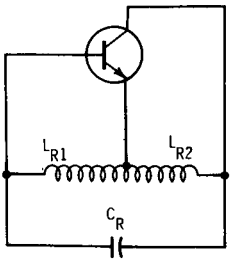
(B) Colpitts circuit with bias.



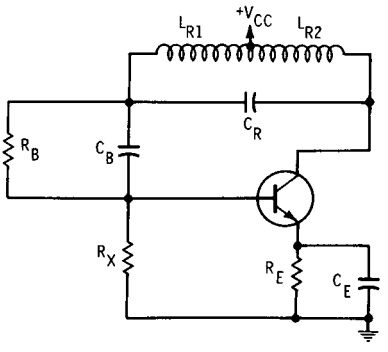
(C) Clapp oscillator.



(D) Clapp circuit with bias.



(E) Hartley oscillator.



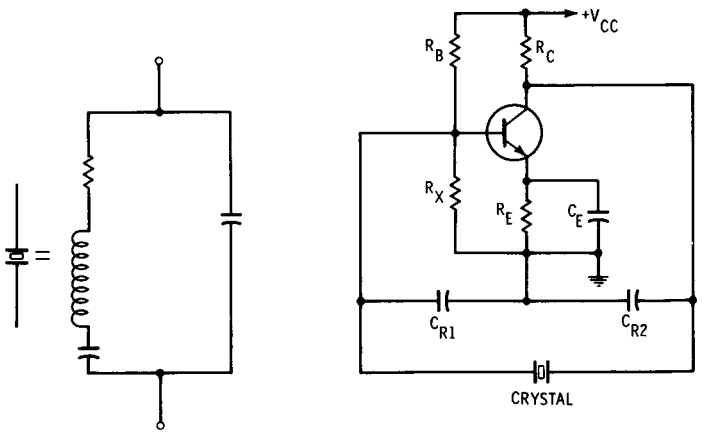
(F) Hartley circuit with bias.

Fig. 10-13. Typical oscillator circuits.

arrangements are shown in Fig. 10-13. In each case, R_B and R_X are the base bias resistors, R_C and R_E are the collector and emitter resistors, respectively, and C_R, C_{R1}, C_{R2}, L_R, L_{R1}, L_{R2}, and M (mutual inductance) are elements of the resonant and feedback circuits. Other capacitors serve coupling and by-pass functions.

In the Colpitts circuits in Figs. 10-13A and 10-13B, the resonant frequency is $f_o = 1/2\pi\sqrt{L_R C_{R1} C_{R2}/(C_{R1} + C_{R2})}$. It will oscillate if the beta of the transistor is greater than C_{R2}/C_{R1}.

The Clapp oscillator will oscillate if beta of the transistor is greater than C_{R2}/C_{R1}, as in the case of the Colpitts circuit. However, the frequency of oscillation is determined by the series combination of all capacitors in the resonant circuit. The primary advantage of the Clapp circuit over the Colpitts oscillator is better stability.



(A) Equivalent circuit of a crystal. (B) Crystal in Colpitts oscillator circuit.

Fig. 10-14. Crystal circuit and application.

The Hartley oscillator in Figs. 10-13E and 10-13F is resonant at about $f_o = 1/2\pi\sqrt{C_R (L_{R1} + L_{R2} + 2M)}$ and it will oscillate if the beta of the transistor is greater than $(L_{R1} + M)/(L_{R2} + M)$.

Coils in Hartley and Colpitts circuits are usually tapped when the circuit is used at low frequencies. This is to allow them to be used with practical capacitors in the resonant circuits.

A piezoelectric crystal behaves as a high-Q inductance-capacitance parallel resonant circuit, and is highly stable. Extremely stable oscillators use crystals instead of circuits with conventional components. The equivalent circuits of a crystal is shown in Fig. 10-14A. A crystal used in a Colpitts circuit appears in Fig. 10-14B.

A single transistor, in any circuit, shifts the phase 180° from the base to the collector. In order for the circuit to oscillate, the phase shift be-

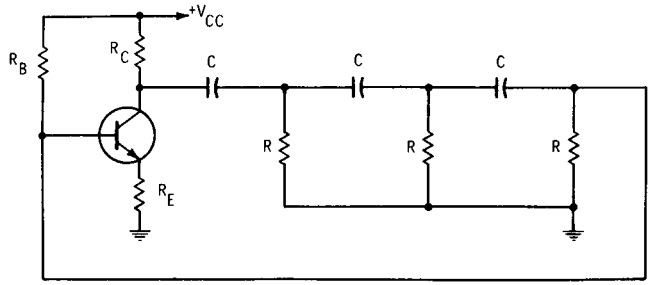


Fig. 10-15. An RC oscillator.

tween the base and collector must be 360°. The capacitive-inductive circuit around the transistor shifts the phase by the additional required 180°. The RC phase shift networks in Fig. 10-15 can do the identical job. Here, the frequency of oscillation is $f_o = 1/2\pi C\sqrt{6R^2 + 4\,RR_C}$. The circuit will oscillate if the beta of the transistor is greater than $(30R^2 + 4R_c^2 + 22RR_c)/RR_c$. Wien bridge or bridge T circuits may be used to replace the phase shift network shown here.

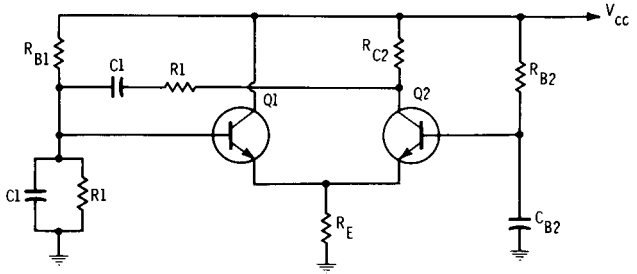


Fig. 10-16. Wien bridge oscillator in emitter-coupled circuit.

A variation of the RC circuit using two emitter-coupled transistors is shown in Fig. 10-16. The Wien bridge is used to select the frequency of oscillation. If the two resistors in the RC legs of the bridge are both equal to R1 and the two capacitors are C1, the circuit will oscillate at a frequency $f_o \approx 1/(6.28R1C1)$. Oscillation will occur only if the voltage gain of the amplifier without feedback exceeds 3.

Chapter 11

MODERN POWER AMPLIFIERS

An audio power amplifier is composed of many of the circuits discussed in the preceding chapters. The output may consist of a single-ended or push-pull power stage, feeding a load or speaker directly or through an output transformer. The various limitations imposed upon power amplifier stages and the circuits were discussed in Chapter 6.

The transistor is a power amplifier. Power must be fed to the input if power is to be delivered to a load at the output. Power is delivered to the output transistors from the preceding stage, the driver. The driver is not required to deliver as much power to the output transistors as they must deliver to the output load. Hence, the driver may be a smaller power device than the output stages.

Small power transistors, often called voltage amplifiers, feed the drivers.

In all push-pull arrangements, the transistor circuit is designed so that each output device conducts primarily for one half of the cycle. Phase inverters or complementary transistors are used to deliver signals to the output devices, so that they will conduct in this manner.

Any electronic circuit produces distortion. To minimize distortion, feedback is placed around the power amplifier. Voltage feedback is usually employed to minimize output impedance and distortion and improve the damping factor.

At this writing, the audio industry has more or less settled on three basic circuits used in an output-transformerless arrangement. The three circuits are analyzed in the following discussion.

DRIVER TRANSFORMERS

One arrangement uses a driver transformer for phase inversion. The basic circuit, shown in Fig. 11-1, uses two identical output transistors. Both are biased through the secondary windings of the driver transformer. Resistors R_B and R_X establish a quiescent collector current through the transistor so as to minimize crossover distortion.

Emitter resistors R_{E1} and R_{E2} serve several functions. While establishing local ac feedback in the emitter of each transistor, they help in dc bias stabilization. A third function is to limit the transistor current should the output load, R_L, be shorted. The resistors are usually a small fraction of an ohm so that the power meant for the output load will not be wasted here. In single-ended class-A amplifiers, about 0.5 to 1 volt is usually developed across the emitter resistor at quiescent conditions. The push-pull amplifier is frequently designed so that a voltage within this range is developed across the resistor R_{E1} or R_{E2}, when the output transistor delivers its peak current.

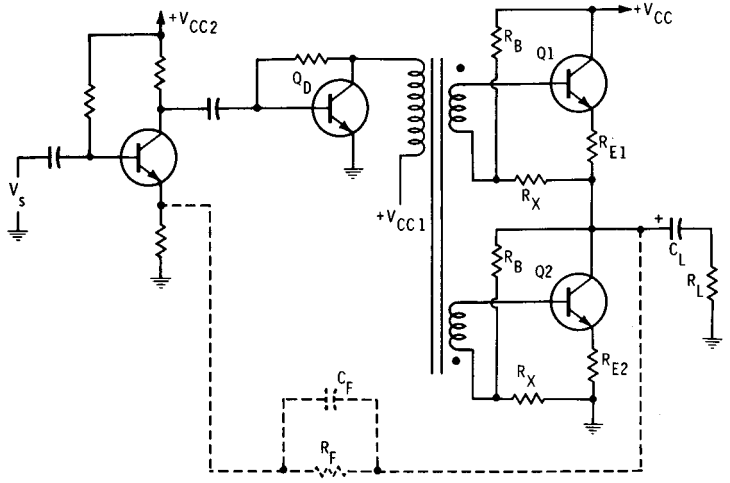


Fig. 11-1. Output circuit using driver transformer for phase inversion.

The two secondaries on the driver transformer are phased so that when signal is applied, one transistor will conduct while the other is idling. When a sine wave is applied, each transistor conducts for one-half cycle, since the base emitter junction is forward biased by the signal only for this period of time. The composite signal is reconstructed across R_L, the load.

A dot has been placed at one end of each secondary winding to indicate phasing. During the half of the cycle when the ends of the secondary windings with the dot are positive with respect to the other ends, only the upper transistor, Q1, will conduct. The peak of the input signal may be large enough to drive the transistor into saturation. During this instant in the cycle, the voltage across Q1 is close to zero. The transistor may be considered as shorted and the top of R_L is effectively connected to $+V_{CC}$. The peak voltage across Q2 is V_{CC} minus the small voltage drops across Q1 and R_{E1}.

During the other half of the cycle, Q2 will conduct. When Q2 is driven into saturation, the voltage across the load resistor will be equal to the voltage drop across Q2 and R_{E2}. The peak voltage across Q1 when it does not conduct, is V_{CC} minus the small voltages across Q2 and R_{E2}.

The turns ratio of the transformer is designed so that a desirable ac load impedance will be presented to the driver transistor, Q_D. Looking back into the secondary windings, each output transistor should see the impedance that will permit it to operate on the most linear portion of its characteristic curve.

In practical design work, transformers of different turns ratios should be tried until the optimum ratio is achieved. Considering many of the designs on the market, a large number of transformers have a primary to each secondary impedance ratio of 9:1. This is a good ratio to use initially. It should be modified from this point as the design of the circuit progresses and the transformer becomes the limiting factor in distortion.

The transformer should be capable of delivering enough power over the entire required frequency range, so that it will not limit the output. It should deliver usable signal several octaves on either side of the required output frequency range without any significant phase shift so that feedback can be placed around the circuit.

The driver stage can be a class-A power amplifier as shown. In some designs, the power this stage can deliver to the output transistors is limited to a specific value by the $+V_{CC1}$ supply voltage. This will, in turn, limit the amount of power the output stage can deliver to the load resistor or to an accidentally shorted output load.

The voltage-limited driver stage is somewhat of a protective device in the event the output load, R_L, gets shorted. However, the protection this circuit affords is limited. If the supply voltage is made too small, the amplifier will not be capable of delivering its rated power into a normal load without distortion. If the supply voltage is too large, the protection is nonexistent. A true protective circuit usually has some device sensing the output current.

The amplifier is completed through the use of a feedback resistor, R_F, from the output back to the emitter of the first voltage amplifier. C_F is used for phase correction and stability. The size of the capacitor can be determined experimentally. Feed a 10- to 20-kHz square wave to the input and note the output on a wideband oscilloscope. The capacitor is trimmed to the point at which there will be no ringing on the output signal while there is no rounding of the leading edge. Actually, it is adjusted for the most faithful reproduction of the square wave.

QUASI-COMPLEMENTARY CIRCUIT

The conventional quasi-complementary amplifier is shown in Fig. 11-2. Q2 and Q4 form the conventional Darlington amplifier circuit, as illustrated

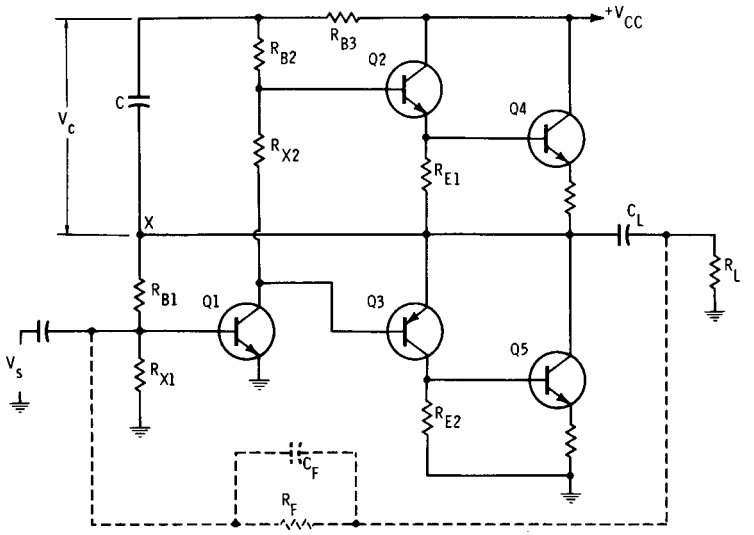


Fig. 11-2. Quasi-complementary amplifier.

in Fig. 7-8. Q3 and Q5 are the complementary amplifier pair of Fig. 7-9D. $R_{B3} + R_{B2} + R_{X2}$ add up to the output load resistor of transistor Q1. R_{X2} is small and may be considered as a short circuit in the ac portion of the analysis that follows. Note also that the voltage at X is $(1/2)V_{CC}$ when there is no signal applied to the amplifier.

Under quiescent conditions, the collector of Q1 is adjusted to the same potential as point X. When the collector at Q1 is positive with respect to X (due to an input signal), Q2 and Q4 conduct, and output power is developed across R_L. When an input signal swings the collector of Q1 negative with respect to X, Q3 and Q5 conduct. The two outputs combine across R_L to recreate the input signal.

The dc collector currents through Q4 and Q5 are determined by their respective base currents, which are, in turn, functions of the collector and base currents of Q2 and Q3, respectively.

The quiescent base-emitter currents of Q2 and Q3 are functions of the voltage developed across R_{X2}. This current will cause an operational shift toward class B when signals of different amplitudes drive the amplifier. The consequential crossover distortion can only be overcome by placing a considerable amount of feedback around the amplifier. In order to be capable of accommodating a large amount of feedback, the voltage gain of the circuit must be high. This can be accomplished by making the load resistor in the collector of Q1 large so that the ratio of the load resistor to the emitter resistance (ratio is voltage gain), is large. Capacitor C, in a bootstrap circuit (see Bootstraping in Chapter 10), provides positive feedback so that R_{B2} will appear much larger than it actually is.

Capacitor C also serves a secondary function. As the output voltage across R_L reaches its positive peak, point X in Fig. 11-2 is essentially at V_{CC}. Without capacitor C in the circuit, the emitter and base of Q2 would both be at V_{CC} and there would be no current through the transistor. Positive peaks could not drive the transistors into saturation. Dut to the clipping action which will occur before saturation, some power will be lost at the output.

Assume now that C is in the circuit. The voltage across the charged capacitor C remains constant at V_c. As the lower end of C is at point X and the upper end is at the junction of R_{B2} and R_{B3}, it maintains the junction at V_c volts above the voltage at X. This voltage is higher than $+V_{CC}$ during positive signal peaks. As V_c is across the sum of R_{B2} and the base-emitter junction of Q2, it will keep this transistor conducting at all times—even when the point X or the emitter is at $+V_{CC}$.

Under quiescent conditions, the voltage at X is $V_{CC}/2$. This is essentially the voltage across $R_{B2} + R_{B3}$. It is also the voltage across the capacitor $C + R_{B3}$. The voltage across $R_{B2} + R_{B3}$ will change with the output signal. However, the voltage across the capacitor, V_c, will remain constant until discharged. The presence of the charged capacitor is essential to maintain the voltage at the junction of R_{B2} and R_{B3} at $+V_c$ volts with respect to X. While being discharged, the voltage across C will maintain a current through R_{B2} and the base-emitter junction of Q2. This current keeps Q2 and Q4 in the conducting state.

R_{B2} is frequently made equal to R_{B3}. Since the total voltage across both resistors is $V_{CC}/2$, the voltage from X to the junction of the two resistors is $(1/4)V_{CC}$. The voltage from this junction to ground is $(3/4)V_{CC}$.

The voltage across and the current through R_{B2} must be maintained at all times. This voltage is the difference between the voltage at the junction of R_{B2} and R_{B3} and the voltage at the base of Q2, or approximately $(3/4)V_{CC} - (1/2)V_{CC}$. This is identical to the voltage which appears across C. Since C maintains the charge, it does not permit the voltage across R_{B2} to change.

R_{B2} is equal to the voltage across the resistor divided by the quiescent base current of Q2.

The time constants of $R_{B2}C$ must be such as to maintain the voltage across R_{B2} constant, even at the lowest frequency to be amplified.

R_{B1} and R_{X1} bias Q1. The voltage across R_{X2} is used to bias the base-emitter circuits of Q2 and Q3. R_{X2} may be replaced by diodes to establish the bias while stabilizing the circuit against temperature fluctuations. R_{E1} and R_{E2} are small resistors shunting the base-emitter junctions of Q4 and Q5, respectively. This serves to raise the collector-to-emitter breakdown voltage of the output transistors, since this breakdown voltage is lower when this junction is open-circuited.

The resistor R_F and capacitor C_F complete the feedback loop to the first transistor in a shunt feedback circuit.

FULLY COMPLEMENTARY CIRCUIT

The big disadvantage of the quasi-complementary amplifier is that the two halves of the push-pull circuit are different. While the two upper transistors form a Darlington amplifier, the two lower transistors are a compound combination of a complementary pair. The gains of both halves are almost identical. However, not all characteristics remain the same over the entire operating range. Amplifiers with precise characteristics have been designed using two Darlington amplifiers or two fully complementary circuits. Examples of these are shown in Fig. 11-3.

The resistor R_F and capacitor C_F complete the feedback loop to the base of the first transistor—a practical example of shunt-applied feedback.

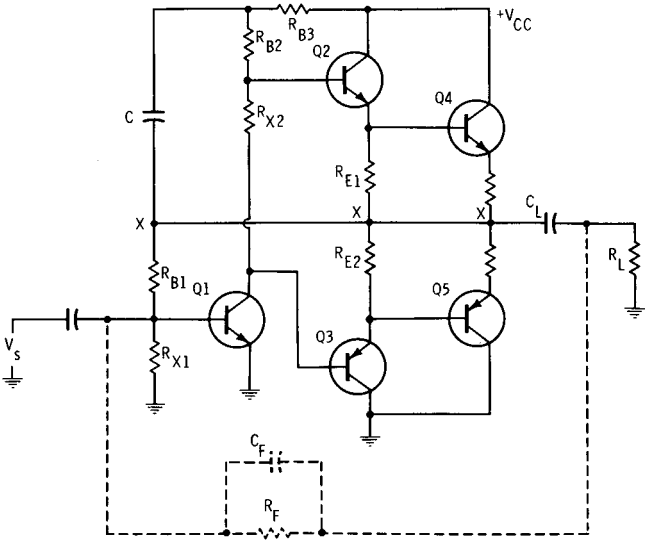
In Fig. 11-3A, a Darlington pair is used in each half of the push-pull circuit, while in Fig. 11-3B, a complementary combination is used. The two halves of the push-pull amplifier are identical in each arrangement. The resistor and capacitor components function as described for Fig. 11-2.

The capacitor coupling the amplifier to the load, R_L, is undesirable in any of the circuits for a number of reasons. First, there is a low-frequency rolloff within the audio band unless the capacitor is made very large—of the electrolytic variety. No matter how large, the low end will begin to roll off at some frequency. If the capacitor is included in the feedback loop, there will be a corner frequency which may make the amplifier unstable. Furthermore, electrolytic capacitors are nonlinear, and contribute to distortion. Finally, the capacitor must be charged through the output transistor. If, in the process, the transistor will handle more energy than it can dissipate safely, the transistor will be destroyed.

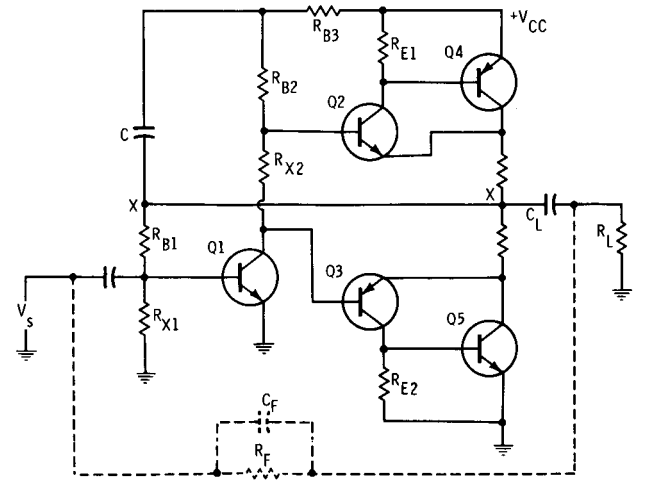
The capacitor prevents dc voltage from appearing across the load. If two power supplies were arranged as in Fig. 11-4 for the circuit of Fig. 11-3B, the capacitor is not required. If both halves of the amplifier are well balanced, the voltage at both ends of the load resistor, under quiescent conditions, will be at the same zero dc potential with respect to ground. The method of splitting the power supply can be used with any of the push-pull output circuits described. As previously discussed, R_{X2} is used to establish a voltage for biasing Q2 and Q3. It is usually replaced with forward-biased diodes for temperature stabilization purposes.

One of the requirements of this circuit is that the voltage drop across both output transistors be equal when no signal is applied. This necessitates that the quiescent currents through both Q4 and Q5 be maintained at their relative values, equal regardless of line and temperature changes. The single transistor driving this output circuit, as in Fig. 11-3, will let the relative output currents through Q4 and Q5 change under these variable conditions.

The differential amplifier provides a circuit in which dc conditions remain relatively constant despite environmental fluctuations. Transistors, carefully matched for tracking of β and V_{BE} variations with collector



(A) Darlington output.



(B) Complementary output.

Fig. 11-3. Darlington and complementary output.

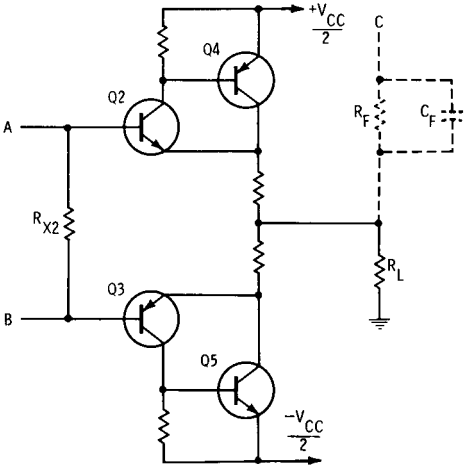


Fig. 11-4. Circuit eliminating output capacitor of Fig. 11-3B.

current and temperature, should be used. A typical circuit using differential amplifiers, based on the circuit in Fig. 7-11, is shown in Fig. 11-5. This circuit can be used to drive the phase inverter and output transistors in Fig. 11-4, or in any other amplifier similarly arranged.

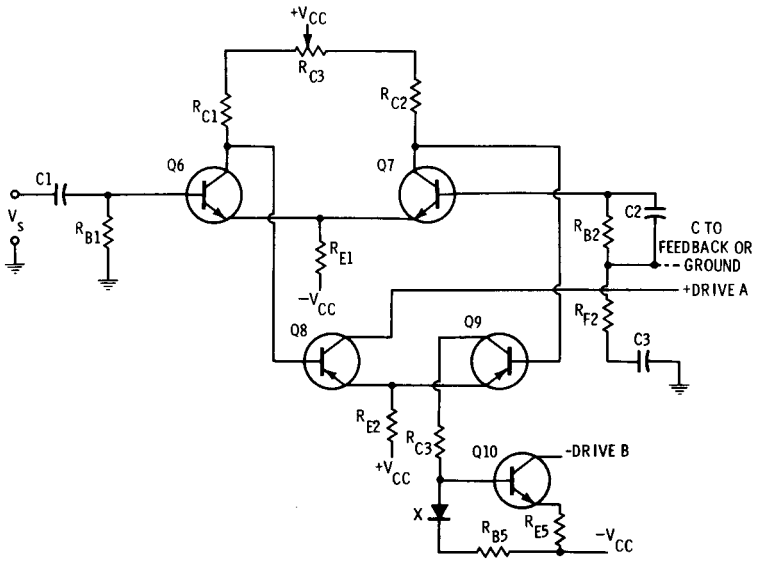


Fig. 11-5. Differential driver amplifier.

The input signal is fed to the base of Q6. The output appears at the collector, shifted 180°. Since Q6 and Q7 are a differential pair, the output also appears at the collector of Q7. The two outputs, 180° out of phase with each other, are direct-coupled to a second differential amplifier pair composed of Q8 and Q9. The signal swings the collector of Q8 from almost $+V_{CC}$ to ground. Thus, the drive for transistors Q2 and Q4 of Fig. 11-4 is taken from the collector of Q8.

The output of Q9 is 180° out of phase with the output of Q8. In order to supply the drive to transistors Q3 and Q5 in Fig. 11-4, the drive signal must be in phase with that supplied to Q2 and Q4. Hence, the output of Q9 is fed to Q10 for an additional 180° phase shift. R_{C3} is of the proper magnitude to reduce the signal fed to Q10 so that the output signal from Q10 will be equal to that of Q8. The phases of the signals at the collectors of Q8 and Q10 are identical due to the phase inversion in Q10. However, the signal swings the collector of Q10 from somewhat more than $-V_{CC}$ to ground. This is the proper signal required to drive Q3 and Q5 in Fig. 11-4.

The differential amplifier is used essentially to stabilize the dc conditions. It must deliver signals of the same phase to the two halves of the push-pull pair. Final phase inversion takes place in the power output section.

In a balanced differential amplifier, the components in each section are identical. Thus, R_{C1} equals R_{C2}, R_{B1} equals R_{B2} and a common resistor is used for the two emitters. It should be noted that R_{B2} must be connected to a dc ground return of some type. It may be connected directly to ground at C. The feedback resistor-capacitor combination at the output in Fig. 11-4 may be connected to this point. As far as dc is concerned, R_{B2} is returned to ground through the small feedback resistor and load. The ac feedback is developed across R_{F2}, which is bypassed to ground through C3.

An example should help clarify the purpose of many of the circuit components and indicate a design procedure. Assume that all connections at A, B, and C are made between the components in Figs. 11-4 and 11-5.

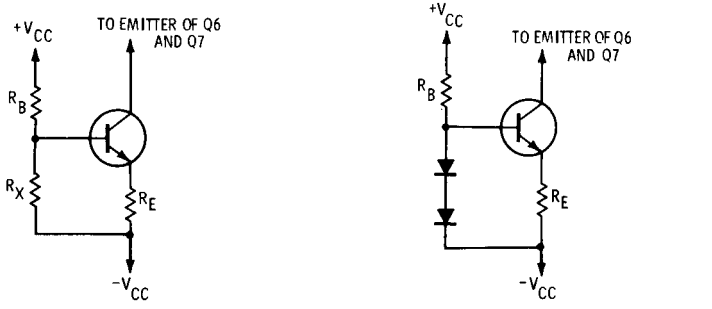
If the output transistors were called upon to deliver 3 amps at the peak of the current swing, and the minimum β of these transistors is 15, the maximum current required at the bases is 3 amps/15 = 200 mA. Similarly, if the minimum betas of Q2 and Q3 are 20, the maximum current required at the bases of these transistors is 200 mA/20 = 10 mA. Hence, the drivers Q8 and Q10 in Fig. 11-5 should be capable of delivering 10 mA to the bases of Q2 and Q3. Q9 should be designed for the same amount of current. Now assume that the minimum beta of each transistor in the driver section is 100 and refer to Fig. 11-5.

If there is to be 10 mA of current through the collector circuits of Q8 and Q9, there must be a total of 20 mA of current through R_{E2}. If R_{E2} were 100 ohms, the voltage across the resistor is 100 ohms × 20 mA = 2 volts. The voltage between the base of Q8 (and Q9) and $+V_{CC}$ is 2 volts plus the voltage across the base-emitter junction. If silicon transistors are used, the total voltage is 2 volts + 0.7 volt = 2.7 volts. This is the voltage

from the collectors of Q6 and Q7 to $+V_{CC}$. Consequently, 2.7 volts must be developed across the resistance composed of R_{C1} and one half of the resistance of the variable control R_{C3}. Similarly, 2.7 volts must be developed across R_{C2} and one half of the resistance of R_{C3}.

Let the sum of R_{C1} (or R_{C2}) and half of R_{C3} be equal to 2700 ohms. Because the voltage across each combination must be 2.7 volts, the circuit will operate properly if the collector currents of Q6 and Q7 are each equal to 2.7 volts/2700 ohms = 1 mA. For convenience, we can let $R_{C1} = R_{C2} = R_{C3} = (2700 + 2700)/3 = 1800$ ohms.

The emitters of Q6 and Q7 are at about 0 volts dc or at ground potential. The combined current through the two transistors, 2 mA, will be through R_{E1}. R_{E1} is returned to the $-V_{CC}$ supply so that it can be made large. Since the emitters should be at about ground potential, $R_{E1} = V_{CC}/2$ mA. One of the reasons for the large size of R_{E1} is to help maintain the sum of the currents through Q6 and Q7 constant at 2 mA, regardless of the size of the input signal. A constant-current source exhibiting an extremely high impedance is applicable here. Circuits of this type, illustrated in Fig. 11-6 can be used in place of R_{E1}.



(A) Constant-current source.

(B) Using forward-biased diodes to achieve a constant-current source.

Fig. 11-6. Constant-current source.

In Fig. 11-6A, R_B and R_X are connected across a large voltage, $2V_{CC}$. The current remains relatively constant through these resistors due to the large size of R_B. Hence, the voltage across R_X is constant. As this voltage appears across R_E and the base-emitter junction, the voltage across and current through R_E will not vary. The collector current will remain constant because it is closely related to the emitter current.

The constant-current source in Fig. 11-6B operates on the basis of a relatively constant voltage being maintained across two forward-biased diodes in the base circuit. As in Fig. 11-6A, the unvarying voltage in the base circuit is transferred to the emitter circuit. A constant voltage is developed across the emitter resistor establishing the emitter and collector currents. Hence, the emitter and collector currents are maintained constant.

In Fig. 11-5, R_{B1} and R_{B2} are adjusted to a convenient value which will be consistent with the required input impedance that V_c must see. It will determine how far off ground potential the emitters of Q6 and Q7 will be. These should be near ground potential if our previous calculations are not to be upset.

Q8 swings the + drive from $+V_{CC}$ to ground. The − drive must swing from ground to $-V_{CC}$. However, the phases of the two outputs must be identical. The signal at the collector of Q9 is 180° out of phase with its counterpart at the collector of Q8. The output from Q9 is fed to the base of Q10 to reverse the phase and alter this situation. Q10 swings the − drive from ground to $-V_{CC}$, which provides the proper signal for supplying Q3 and Q5 in Fig. 11-4. The circuitry is also arranged to make the amplitude of the − drive equal to that of the + drive.

If R_{B5} in Fig. 11-5 is made equal to R_{E5}, and the voltage across diode X is equal to that across the base-emitter junction of Q10, the voltage across and hence the current through both resistors will be identical. In the quiescent state, the currents through the collectors of Q8 and Q9 are equal. As discussed above, this current is 10 mA. If R_{B5} and R_{E5} were specified as being 100 ohms, the drops across each resistor is 10^{-2} amps $\times$ 10^2 ohms $= 1$ volt. The 1 volt across R_{B5} will force 10 mA of current through the collector circuit of Q10.

Since the voltage across the forward-biased diode is about 0.7 volt, the voltage across the sum of R_{B5} and the diode is 1.7 volts.

The voltage at the collector of Q9 is about the same as the voltage at the collector of Q8. They are both near ground potential. The voltage across R_{C3} is $V_{CC} - 1.7$, because there is a total of 1.7 volts across X and R_{B5}. As the current is 10 mA, R_{C3} is equal to $(V_{CC} - 1.7)/(10 \times 10^{-3})$.

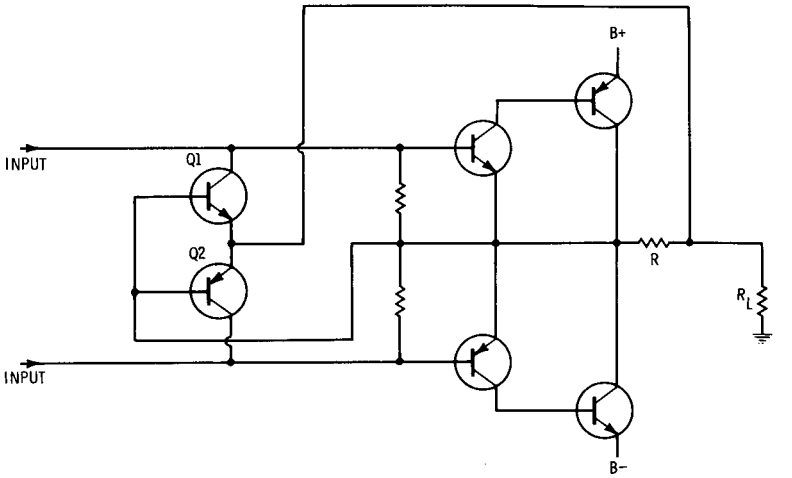
A considerable amount of feedback can be placed around this circuit to bring distortion down to the vanishing point.

This circuit is indeed complex. It requires intensive work in the laboratory to optimize all components. Furthermore, with large amounts of feedback, stability will be a problem. Careful adjustment of the forward loop frequency characteristics will be essential.

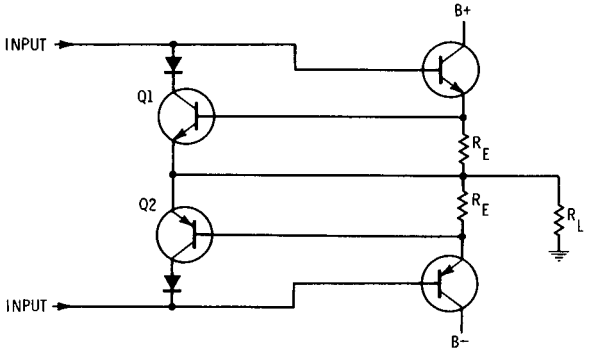
PROTECTION CIRCUITS

The output transistors of an audio amplifier are subject to breakdown, even in the event of only momentary abuse. While loaded with the specified impedance, output transistors can provide reliable service; but a short circuit at the output can force the output devices to deliver so much current that they will dissipate more power than they can handle safely. Despite the proper loudspeaker load at the output, an unusually inductive or capacitive impedance can, in some cases, upset the stability of an amplifier. Excess current can flow if the amplifier breaks into sustained or damped oscillations.

A number of circuits have been devised to provide protection for the output devices. In the two circuits shown in Fig. 11-7, the magnitude of the output current causes a voltage to be developed across a sensing resistor. This voltage is fed to the transistors Q1 and Q2 at the input of the driver stages. When the current at the output exceeds a predetermined level, the



(A) Output current sensed across resistor R in series with load.



(B) Output current sensed across R_E in each emitter lead.

Fig. 11-7. Protection circuits sensing output current.

voltage across the sensing resistor is of the proper magnitude to turn on Q1 and Q2, shorting the input signal at the drivers. As this signal does not reach the output devices, they cannot be destroyed.

A more sophisticated circuit, developed by RCA, not only is used to feed back information about the amount of current through the output

transistors, but also adds data about the size of the load. This can be explained with the help of the circuit in Fig. 11-8.

When excess current flows through the output transistor Q3 while the output load resistor R_L is shorted, the voltage developed across R_{E1} is divided between R1 and R3. It is sufficient to turn on Q1 and shunt signal away from the base of Q3. The same relationship holds true for the lower half of the circuit involving R_{E2}, R2, R4, Q2 and Q4.

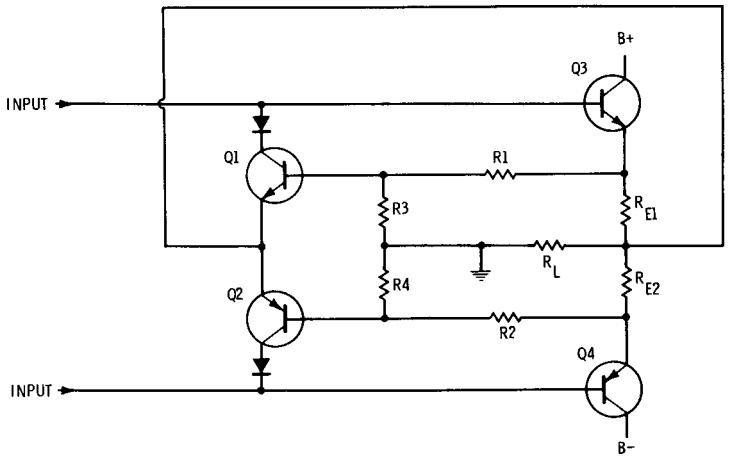


Fig. 11-8. Basic load-line limiting circuit.

Now assume the load resistor is equal to or larger than a predetermined value. When signal is flowing through this resistor, the voltage developed across R_L is applied to the base-emitter junctions of Q1 and Q2. This voltage will reverse bias these transistors. If Q1 and Q2 are to conduct under these conditions, the voltage developed across R_{E1} and R_{E2} must be greater than the sum of the voltage required to overcome this reverse bias and the voltage required to just turn on Q1 and Q2.

Hence the condition required to turn Q1 and Q2 on depends upon the collector (or emitter) current of the output devices and upon the size of the load. More current will flow when a large load is at the output and less when the load is small. The output transistors are protected against short circuits as well as against excess current transients. Very little else can be demanded of a protection circuit.

Chapter 12

TRANSISTOR SWITCHES

The transistor has been considered as an amplifier of ac signals. Audio circuits have been described in which the performance surpasses the quality of many pieces of vacuum-tube equipment.

The transistor, however, can also be a switch. A small pulse in the base circuit can turn the large collector current on or off. Any device or load in the collector circuit is activated by the presence or absence of current in that circuit.

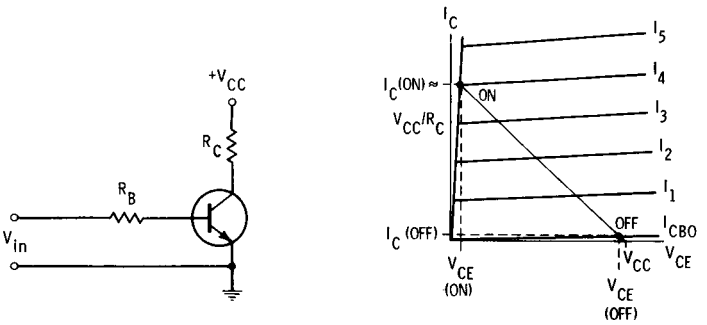
The semiconductor switch acts faster than its mechanical counterpart, but the switching is not as complete. When a mechanical switch is closed, an operation similar to a transistor being turned on, the resistance between the switch contacts is essentially zero. For the transistor, the collector-to-emitter resistance may be as high as several thousand ohms. Should the mechanical switch be open, the resistance between the contacts approaches infinite proportions. When the transistor is off, the resistance may be high, but never infinite. There is always some collector current.

SATURATED MODE SWITCHING

If the transistor is off, the circuit is usually designed so that there is only I_{CBO} through the collector. The supply voltage is across the transistor. It behaves as an open circuit. In the *on* state, the collector current is a function of the load in the collector and the supply voltage. This can be illustrated with the help of Fig. 12-1.

In the saturated mode of operation, the voltage across the transistor drops to near zero when the transistor is turned on. Practically the entire supply voltage is across the collector load. The transistor is effectively a short circuit, putting R_C between $+V_{CC}$ and ground. I_C is then equal to V_{CC}/R_C.

A switching transistor is normally either in the *on* or *off* state. As there is a small voltage across the transistor in the *on* condition and a small cur-



(A) Transistor switch. (B) Transistor in saturated mode switching.

Fig. 12-1. Transistor switching.

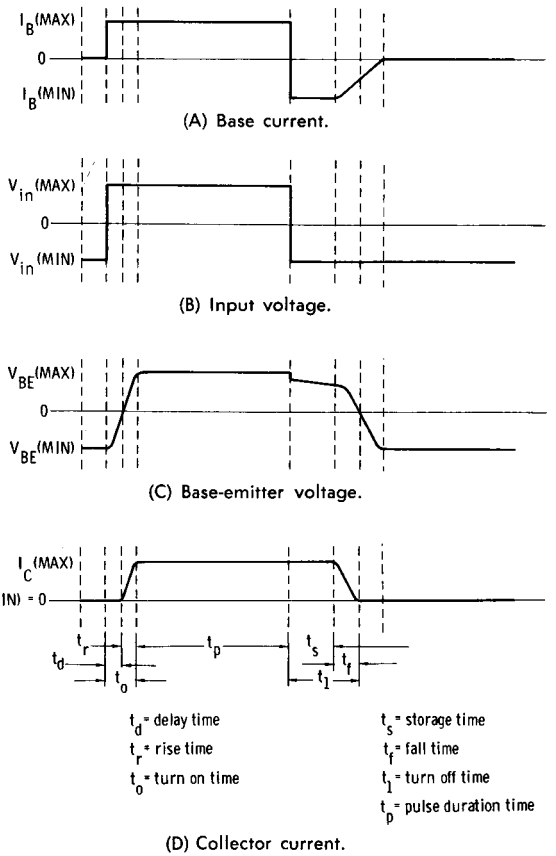


Fig. 12-2. Various voltage and currents of transistor switch.

rent in the *off* state, little power is dissipated by the transistor. A reverse bias is usually placed on the base to keep the current at a minimum (about I_{CBO}) in the *off* condition.

The switching is not instantaneous, but must go through a number of steps, illustrated in Fig. 12-2. All references to time are in microseconds.

The voltage in Fig. 12-2B is fed to the input terminal of the transistor circuit in Fig. 12-1A. The base-emitter diode behaves similarly to the diode switch described in Chapter 1. Although the base current in Fig. 12-2A starts without any delay, there is a delay time, t_d, until the base-emitter voltage reaches zero (threshold voltage in C of Fig. 12-2) and collector current can start. Delay time is defined as the period of time from when the turn-on pulse is initiated until the collector current reaches 10 per cent of its peak value, $I_C(max)$. It is directly proportionaly to the reverse bias and inversely proportional to the turn-on current.

In the sections describing high-frequency amplifiers, two capacitors were introduced: the capacitance from base to emitter and the capacitance from base to collector. These have influence over the duration of the next section of the curve, t_r, the rise time. This is the time it takes the collector current to rise from 10 percent to 90 percent of its maximum. The sum of t_d and t_r is known as the turn-on time.

From there, all remains stable during t_p, the pulse duration time, until the input signal delivers the turn-off pulse. A transistor in saturation will not go out of saturation instantly, since a capacitor stores a charge. This capacitor may be drawn as a component in the equivalent circuit of the transistor and exists only when the transistor is in saturation. The capacitor shunts the base-emitter and base-collector capacitors, which are always present in the high-frequency equivalent circuit. The storage capacitor must be discharged before the transistor will go out of saturation.

The base current turns negative without any delay and then gradually returns to zero. The base-emitter voltage remains positive for a while. The collector current does not change until that circuit comes out of saturation and the storage capacitor is discharged. The period of time from the turn-off pulse until the collector current comes out of saturation (drops to 90 percent of its maximum) is known as the storage time, t_s. The storage time increases the more the transistor is driven into saturation. It decreases if the reverse drive pulse is made larger.

The period of time that it takes the collector current to drop to zero is known as t_f, the fall time. The base current and base-emitter voltage then return to quiescent values and the transistor is turned off. The turn-off time is $t_s + t_f$.

In order to speed the switching action of the transistor, R_B in Fig. 12-1A may be shunted by a capacitor, C_B. A negative voltage may be applied to the base to stop any base-to-emitter current when the transistor is off, so that only I_{CBO} flows through the collector circuit. A complete drawing of this is shown in Fig. 12-3. The design procedure may be pursued as follows.

1. Determine the collector saturation current. It is $I_C(\text{sat}) = V_{CC}/R_C$. The base current must be capable of producing at least $I_C(\text{sat})$.
2. Calculate R_X. It is equal to $V_{BB}/I_{CBO}(\text{max})$, where $I_{CBO}(\text{max})$ is the maximum I_{CBO} rating of the transistor when operated at the highest temperature. V_{BB} must establish a negative current equal to $I_{CBO}(\text{max})$ to counter the $I_{CBO}(\text{max})$ that is ordinarily through the base-emitter junction of the transistor. Since the net I_{CBO} through the base-emitter junction will be zero, there will be only $I_{CBO}(\text{max})$, rather than the much larger I_{CEO}, through the collector circuit.

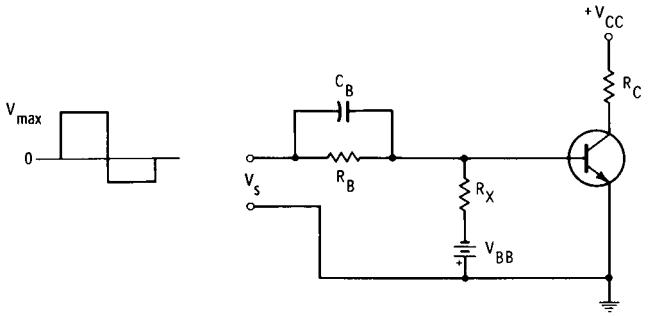


Fig. 12-3. Transistor switching circuit.

3. Plot the load line on the characteristic curve, as shown in Fig. 12-1B. Determine the base current needed to drive the transistor into saturation. It is I_4. The R_B-C_B circuit must conduct I_4, as well as $I_{CBO}(\text{max})$, to the base of the transistor to overcome the current supplied by V_{BB}. The voltage across R_B is the maximum input voltage, V_{max}, minus the voltage drop across the base-emitter junction of the transistor, V_{BE}. V_{BE}, as always, is about 0.2 volt for germanium transistors and 0.6 volt for silicon devices. Hence,

$$R_B = (V_{max} - V_{BE})/(I_4 + I_{CBO}(\text{max})) \qquad (12\text{-}1)$$

4. The rise time, which is determined from the speed required in the switching operation, can be reduced by overdriving the base circuit of the transistor. If f_β is the β cutoff frequency of the transistor, the required base current for a rise time of t_r can be calculated from:

$$I_B = I_C(\text{sat})/\beta(D) \qquad (12\text{-}2)$$

where,

D can be determined from the curve in Fig. 12-4.

5. Calculate the difference between the base current, I_B, for the required rise time, and the base current, I_4, through the resistor R_B, and just driving the transistor into saturation. This current, $I_B - I_4 = I_s$, is the current that must pass through the capacitor.

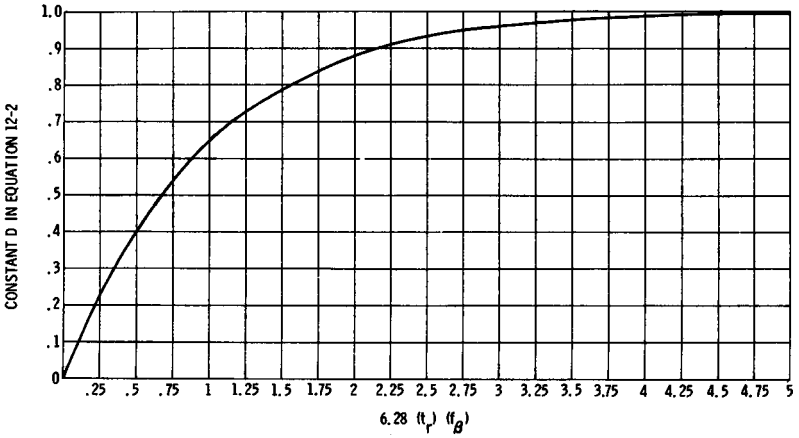


Fig. 12-4. Curve for determining "D" in Equation 12-2.

6. Calculate the capacitance from the formula:

$$C_B = (I_s)(t_r/V_{max}) \qquad (12\text{-}3)$$

where,

C_B is the capacitance in μF,
I_s is the current in amps.
V_{max} is the switching voltage in volts,
t_r is the rise time μs.

This equation is based on the well known formula, $C = Q/V$, where Q is the charge on the capacitor when a voltage V is across the capacitor. Actually, Q equals $I_s t_r$, the total charge on the capacitor after a time, t_r.

In Fig. 12-3, there is current through the load, R_C, only when the transistor is turned on. In Fig. 12-5, there is current through the load, R_L, when the transistor is turned off. Ignoring the diode, the voltage V_{CC} divides between R_C and R_L when the transistor is off. When it is on, the transistor is a short across R_L.

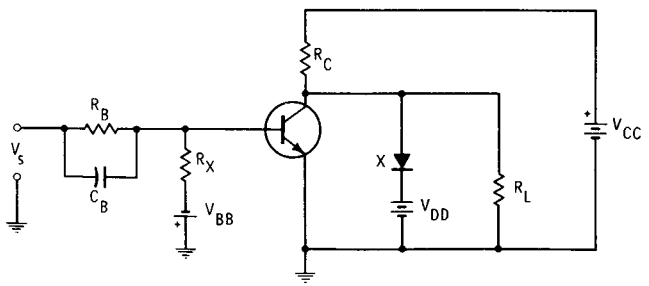


Fig. 12-5. Switching circuit with load grounded.

When the diode, X, is in the collector circuit, the voltage across R_L is clamped to the voltage across the diode plus V_{DD}. This protective circuit takes effect when the voltage across R_L exceeds V_{DD}, and the diode conducts.

The major advantage of this circuit is that the load is returned to ground.

In designing either type of switching circuit, latch-up must be avoided. This condition can be described with the help of Fig. 12-6.

A number of rated breakdown voltages have been noted on the drawing. The largest, BV_{CBO}, is the reverse breakdown voltage of the collector-base junction, with the emitter open. This is equivalent to the avalanche breakdown associated with the zener diode. It is the maximum voltage that can be applied to the transistor. At this voltage, the collector current rises rapidly with but a minute increase in collector voltage.

BV_{CEO} is the collector-to-emitter breakdown voltage, with the base junction open. It is the maximum collector voltage on the $I_B = 0$ curve.

The collector-to-emitter breakdown voltage is increased when there is a resistance between the base and emitter junctions of the transistor. The

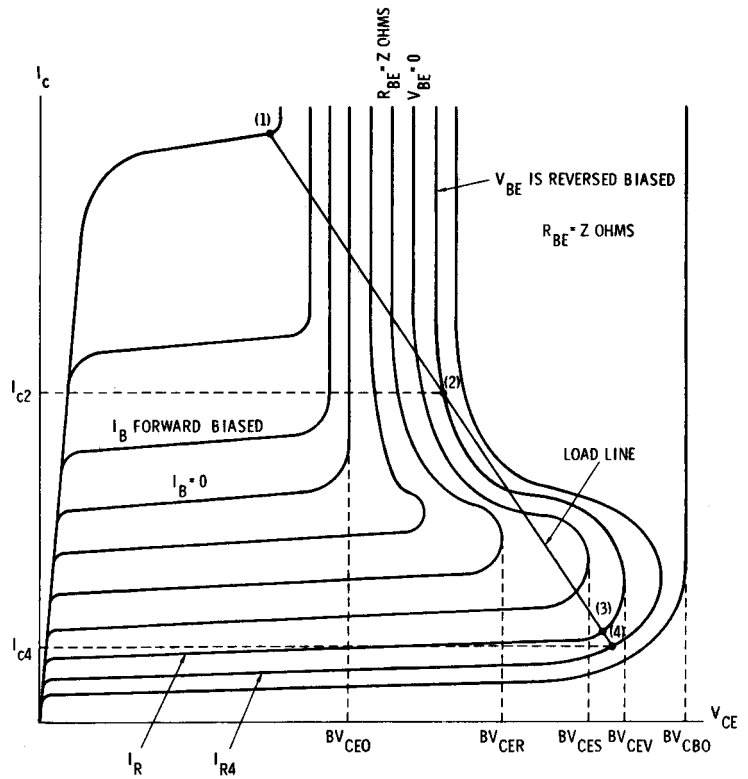


Fig. 12-6. Collector characteristics showing latch-up.

symbol for this is BV_{CER}. R may be indicated on the specification sheet although the data is frequently stated for a 10-ohm resistor.

Should the base be shorted to the emitter, the breakdown voltage increases to BV_{CES}. In this case, the base-to-emitter voltage is zero. A reverse-biased base-emitter junction, shunted by a resistor of R ohms will raise the breakdown voltage to BV_{CEV}.

Note that in the avalanche region, the collector-to-emitter voltage decreases as the current rises. If the load line in the switching circuit is as shown, the transistor will be on when the swing of the input pulse forces the collector current to (1). When turned off, let us say to a reverse base current I_R, the desired quiescent point is (3), so that there is little collector current when the voltage is at a maximum. Actually, as the base current is switched off to I_R from point (1), the collector current will be at I_{C2}, because it just crosses the I_R curve at this point. It is in a latch-up condition.

To get out of latch-up, the reverse base current must be increased so that the collector reaches I_{C4} at (4) on the I_{R4} curve. Only then can the quiescent point be returned to (3) on the I_R base current curve.

To avoid latch-up, the load line should be plotted on the characteristic curve, and the current swings should be noted. It is frequently insufficient to use only the BV_{CBO} and BV_{CEO} specification without curves to design a switching circuit.

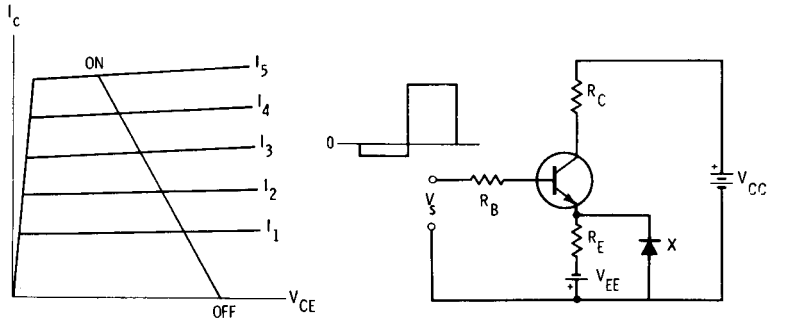
CURRENT MODE SWITCHING

In the saturated mode switching just discussed, the transistor is driven into the saturated region when switched on. Other switching modes are possible, in which the transistor is not driven into saturation. One of these, the subject of this section, is the current mode switch.

It is in the *on* condition of the transistor that we see the differences in the three possible switching modes. While the transistor is driven into saturation in the saturation mode, in the current mode it is usually near, but not quite in, saturation.

The curve showing current mode operation is drawn in Fig. 12-7A. Although there is more power dissipated here in the *on* condition than in the saturated mode of operation, current mode is highly desirable where fast switching speeds are required. Storage time problems are eliminated. The speed is increased with the distance that the *on* state is away from saturation. Operation is also reasonably independent of transistor parameter variations and noise. A high degree of dc stability is possible too. A typical current mode switching circuit is shown in Fig. 12-7B.

When the transistor is switched off, a complete circuit is formed with the emitter supply, V_{EE}, the emitter resistor, R_E, and the diode. In this condition, the voltage across the diode appears between the emitter and ground. Since this voltage will forward-bias the transistor into conduction, the input voltage must counter this to keep the transistor off. Hence, for the transistor to be off, the input voltage must be negative.



(A) Current mode switching. (B) Circuit using current mode switching.

Fig. 12-7. Transistor current mode switching.

When the input pulse is positive, the transistor is turned on. The diode will be turned off since the emitter current through R_E will bias the diode in the reverse direction.

The diode may be replaced by the base-emitter junction of a second transistor, as shown in Fig. 12-8. This is not unlike the differential amplifier discussed in chapter 11. It will provide two outputs 180° out of phase with each other. While V_{out2} is in phase with V_{in}, V_{out1} is out of phase with both V_{in} and V_{out2}.

Returning to Fig. 12-7B, the transistor can never be in saturation if the saturated collector current is greater than the current through the emitter. For current mode operation, V_{CC}/R_C must be greater than V_{EE}/R_E.

AVALANCHE MODE SWITCHING

Avalanche mode switching exceeds the speed of current mode switching. The curves and load line showing this mode of switching and the basic circuit are in Fig. 12-9.

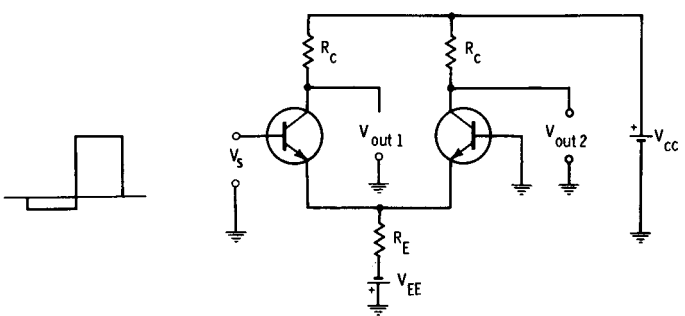
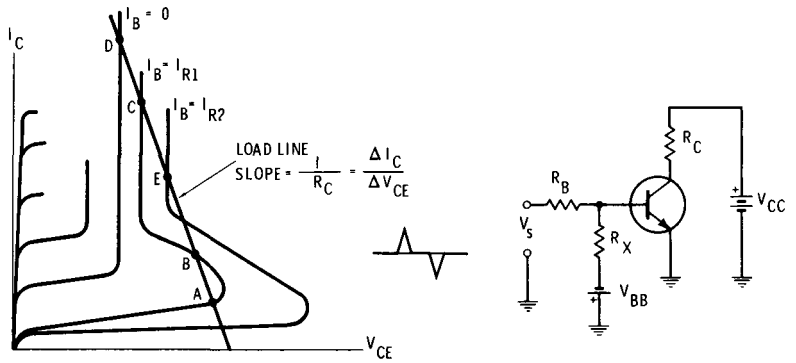


Fig. 12-8. Alternate current mode switching using differential amplifier.

V_{BB} reverse-biases the transistor so that operation is on the I_{R1} curve. Assume that this transistor is idling at A in the *off* condition. A positive pulse turns the transistor on, let us say to the $I_B = 0$ curve. Operation jumps to D on the curve. The pulse is removed in a short time and the operation must revert to the I_{R1} curve at C.

This portion of the curve is a negative resistance, which is characterized by instability. It can be shown that if the slope of the transistor curve is greater than the slope of the load line, $1/R_C$, the operation is stable. If the reverse is true, operation is unstable. Hence, C is a stable point on the curve.



(A) Avalanche mode switching. (B) Circuit using avalanche mode switching.

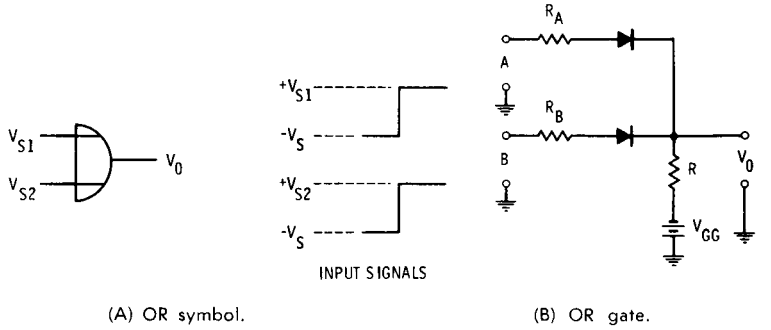
Fig. 12-9. Transistor avalanche mode switching.

The reverse pulse can force operation from C back to a point E on the I_{R2} curve. When the pulse is removed, the transistor will then revert to B on the I_{R1} curve. Since the slope at this portion of the curve is less than the slope of the load line, operation is unstable. It jumps to point A, a stable point on the positive resistance portion of the curve.

The switching action in the avalanche mode can be initiated by pulsing the base current or collector supply voltage. In the latter case, the load line is moved parallel to the load in its quiescent state, shifting the operating point from one base current curve to the other.

SWITCHING AND LOGIC CIRCUITS

Computers are based on pulses being fed to semiconductor circuits. The pulses, applied to a circuit, enable it to perform various operations. Various combinations are designed into complex systems to accomplish different jobs. All these combinations are based on five circuits: OR, AND, NOR, NAND, and inverter. The first four are presented in the following discussion. The fifth is not unlike the phase inverters discussed above.

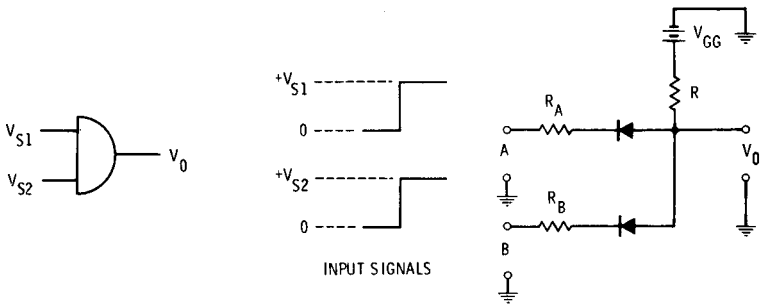


(A) OR symbol. (B) OR gate.

Fig. 12-10. OR gate and symbol.

The symbol for the OR gate is shown in Fig. 12-10A, and a schematic of an OR circuit is in Fig. 12-10B.

Initially, the $-V_{GG}$ supply is made equal to $-V_S$, the input voltage to the diodes. There is 0 volts across the diodes. They do not conduct because zero is below the cut-in voltage. If a positive pulse is applied to the anode of either diode, it will conduct. The output voltage, V_0, will rise from $-V_{GG}$ to a value determined by V_{S1} (or V_{S2}), $-V_{GG}$, R, R_A (or R_B), and the voltage drop across the diode. This voltage may be determined with superposition methods discussed in earlier chapters.



(A) AND symbol. (B) AND gate.

Fig. 12-11. AND gate and symbol.

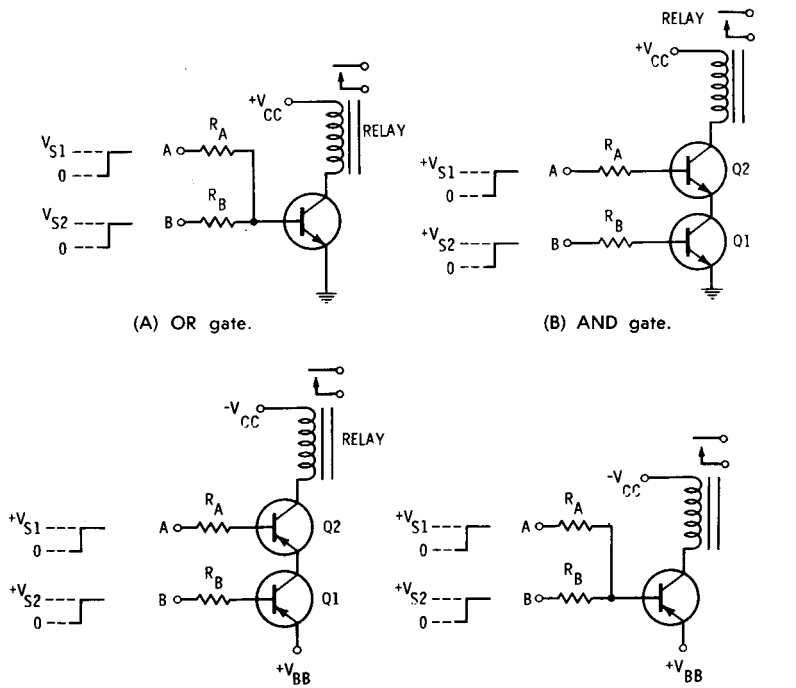
The symbol for an AND gate is shown in Fig. 12-11A and a schematic representation is drawn in Fig. 12-11B. The diodes are forward-biased by the supply voltage, $+V_{GG}$. V_0 is positive, and is determined by the components in the circuit. If the voltage at either A or B rises to V_{S1} (either being greater than $+V_{GG}$), the particular diode will be reverse-biased and will cease to conduct. The voltage at V_0 will remain low because only one diode is off while the second one is still on. Should both diodes stop conducting due to simultaneous application of pulses V_{S1} and V_{S2}, V_0 will rise to $+V_{GG}$ volts.

The NOR symbol is shown in Fig. 12-12A and the NAND symbol is shown in Fig. 12-12B. In the OR and AND circuits, the voltage at the output increased if the input pulse was positive. In the NOR and NAND circuits, the outputs of the previous arrangements are fed through a transistor phase inverter. Hence, the output goes negative if the input pulse is positive.

(A) NOR symbol. (B) NAND symbol.

Fig. 12-12. NOR symbol and NAND symbol.

The preceding discussion described the logic circuit with the inputs related to the output voltage. The circuits can also be designed to relate the input pulse to an output current. Typical circuits used to operate a mechanical relay are shown in Fig. 12-13. Only two pulse sources are drawn in each case. As many as are desired can be designed into the circuit.



(A) OR gate. (B) AND gate.

$(+V_{BB} < +V_{S1}; +V_{BB} < +V_{S2})$ $(+V_{BB} < +V_{S1}; +V_{BB} < +V_{S2})$

(C) NOR gate. (D) NAND gate.

Fig. 12-13. Current-operated logic circuits.

In Fig. 12-13A, a positive pulse at either A *or* B turns the transistor on and the relay is activated. In Fig. 12-13B, the positive pulses must be present at A *and* B to turn on the two transistors and activate the relay.

Pnp-type transistors are used in Fig. 12-13C and Fig. 12-13D. All transistors are normally turned on and the relay is activated. In Fig. 12-13C, positive pulses applied to either A or B will turn off the respective transistor. Positive pulses must be applied to A and B in Fig. 12-13D to turn the transistor off.

TRANSISTOR VOLTAGES IN THE VARIOUS STATES

In the chapters on class-A transistor amplifiers, we assumed that the voltage between the base and emitter of a silicon transistor is about 0.6 or 0.7 volt. The equivalent voltage for a germanium transistor was noted as about 0.1 or 0.2 volt. These approximations are sufficiently accurate for most calculations. Now, we must determine approximate diode voltages that apply to a switching transistor. The voltages vary somewhat from those previously noted.

When a transistor is off, the voltage from the base to the emitter of a silicon transistor can be assumed to be zero, while the voltage across the terminals of a germanium device is about −0.1. As the silicon transistor starts to conduct, however slightly, the base-emitter voltage reading will be about 0.5. In the case of a germanium device, it is about 0.1 volt. In saturation, the voltage across the base-emitter silicon junction is about 0.7 while that across the germanium junction is about 0.3 volt.

All these voltages vary somewhat with temperature. In the preceding chapters, it was assumed, for conservative designs, that the base-emitter voltage decreases 2.5 millivolts for each 1°C rise in temperature. The approximation of −2 millivolts/°C is the more usual case for use in switch designs. This number applies to all portions of the base-emitter voltage curves just detailed, and for germanium as well as silicon transistors.

In saturation, the collector-emitter voltage approaches zero. It is *not* zero. Lacking better details from the manufacturer of the transistor, it may be assumed that for silicon devices, the voltage is about 0.3. In the case of a germanium transistor, the voltage may be assumed to be 0.1. When the collector current is less than 10 mA, the collector-emitter saturation voltage varies only minutely with temperature. At high collector currents, the voltage will *increase* at about 0.2 millivolt for each 1°C rise in temperature.

These numbers are easy to remember. For silicon transistors, the base emitter voltage is 0 at cutoff, +0.5 when the transistor just starts to conduct, +0.6 when conduction is below saturation and 0.7 volt at saturation. For the germanium device, the equivalent voltages are −0.1, +0.1, +0.2 and +0.3.

The base-emitter temperature characteristic is negative at −2 mV/°C. The collector-emitter temperature characteristic is positive at +2 mV/°C.

Chapter 13

MULTIVIBRATORS

A multivibrator circuit usually consists of two transistors. In the quiescent state, one device is on and the other is off. They can be switched to reverse their states. During switching, both devices can be on simultaneously. In the conventional multivibrator circuit, regenerative or positive feedback is placed around two transistors. Should both transistors conduct, and the feedback is greater than 1, the circuit is unstable. The circuit must be unstable while switching. The circuit components can be so specified that the *on* transistor is operating either in the saturation or current mode.

Three different types of multivibrators are commonly used in electronic equipment.

The astable or free-running multivibrator is the equivalent of a feedback oscillator. It is stable for short periods of time, or quasi-stable. Both transistors interchange their *on* and *off* states continuously. During one portion of the cycle, one transistor is on while the second is off. The states are reversed during the second portion of the cycle.

On the other hand, the monostable or one-shot multivibrator has one stable state. Assuming that switching transistor No. 1 is on in the stable state and switching transistor No. 2 is off, a pulse can be applied to the circuit, turning transistor No. 1 off and transistor No. 2 on. After a period of time predetermined by the circuit components, the circuit will revert to the original condition. The transistors will remain in their original states until a second switching pulse is applied, once again reversing the states. After a period of time, the transistors will again revert to their original states awaiting other switching pulses.

The bistable multivibrator or flip-flop circuit has two stable states. Either transistor can be on or off. They will reverse states only on the application of a switching pulse. They will retain the new states until a second pulse forces the transistors to revert to the original states.

THE BISTABLE MULTIVIBRATOR

The simplest circuit uses base bias from a fixed voltage source, as shown in Fig. 13-1.

If the switches are operating properly, the *on* transistor is in saturation. The voltage from the emitter to the collector on this transistor is near zero. The *off* transistor behaves as an open circuit.

Assume that Q1 is in cutoff while Q2 conducts. Q1 is held in cutoff by virtue of the negative $-V_{BB}$ supply. The collector voltage of Q1 is at $+V_{CC}$. This voltage, applied to the base of Q2 through R_{C1}, counters $-V_{BB}$ to keep transistor Q2 turned on.

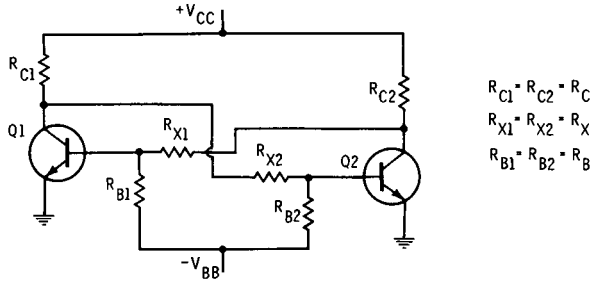


Fig. 13-1. Bistable multivibrator using fixed bias supply.

Should a positive pulse be applied to the base of Q1, this transistor will be turned on and the collector voltage will drop to zero. Q2 will be turned off because there will be no positive voltage to counter $-V_{BB}$.

A similar chain of events will be triggered by applying a negative pulse to the base Q2. It will be turned off. The collector voltage will rise to $+V_{CC}$. Applied to the base of Q1 through R_{X1}, it will counter $-V_{BB}$ and turn on Q1.

During the changing cycle from one state to the other, the circuit must be unstable. This is achieved when βR_C is greater than R_X. The loop gain will then be greater than 1.

The output voltage swing at either collector is approximately V_{CC} volts, because it is the difference of the voltages across either transistor in the *on* and *off* states.

In designing a circuit of this type, the collector saturation current, $I_C(\text{sat})$, may be chosen first. It must be within the ratings of the transistor. To be in saturation, the resistor in the collector, R_C, must be equal to or less than V_{CC} divided by the minimum collector saturation current. However, R_C must be large enough to limit transistor dissipation.

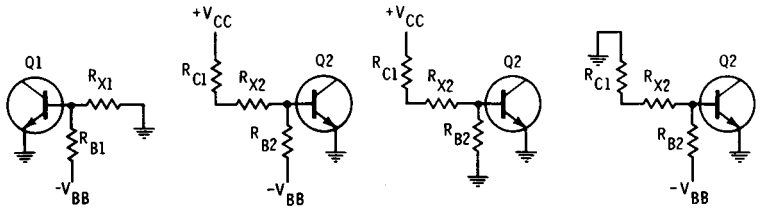
V_{BB}, R_{B1}, R_{B2}, R_{X1}, and R_{X2} are chosen with two criteria in mind. It must be possible to drive the *on* transistor into saturation. The *off* transistor should, at the same time, be biased below cutoff.

When Q2 is on, the voltage at its collector is almost zero. The collector and the end of R_{X1} connected to the collector are effectively at ground. The base circuit of Q1 can be reduced to that in Fig. 13-2A. The voltage at the base of Q1, using voltage divider methods, is:

$$-\frac{R_{X1}}{R_{B1}+R_{X1}}V_{BB}$$

This must be sufficiently negative to cut off Q1. Since I_{CBO} must be neutralized by the current resulting from the combination of $-V_{BB}$ and R_{B1}, $-V_{BB}/R_{B1}$ must be equal to or greater than $-I_{CBO}$.

The equivalent base circuit for the *on* transistor is shown in Fig. 13-2B. There is no current through Q1. There is only base current Q2 through R_{C1}, R_{X2}, and R_{B2}. The base current can be determined using superposition procedures. (See Chapter 3, bias circuit III for a description of this method.)



(A) Q1 off. (B) Q2 on. (C) Q2 on. (D) Q2 on.

Fig. 13-2. Base circuits of Fig. 13-1.

An example in the application of superposition techniques to multivibrator circuits involves finding the base current through Q2 in Fig. 13-2B.

First, short the $-V_{BB}$ source, as in Fig. 13-2C. R_{B2} is effectively connected to ground. Since the base-emitter junction is practically at ground potential, it is a short across R_{B2}. All current due to V_{CC} passes through the base-emitter junction and there is very little through R_{B2}. Since the voltage across this junction is relatively low, the base current due to V_{CC} is $V_{CC}/(R_{C1}+R_{X2})$.

Now restore $-V_{BB}$ and short V_{CC} as shown in Fig. 13-2D. The base-emitter junction is a relative short circuit across R_{C1} and R_{X2}. The base current due to $-V_{BB}$ is just about equal to $-V_{BB}/R_{B2}$.

The current through the base-emitter junction is $I_B = V_{CC}/(R_{C1}+R_{X2}) - V_{BB}/R_{B2}$. This base current, multiplied by the beta of the transistor, should provide more than enough collector current to drive the transistor into saturation.

V_{BE} was assumed to be zero. More accurate calculations can be made by assuming that the $V_{BE}(sat)$ voltage is across this junction. Use $V_{BE}(sat)$ data supplied by the manufacturer of the transistor or as specified in the

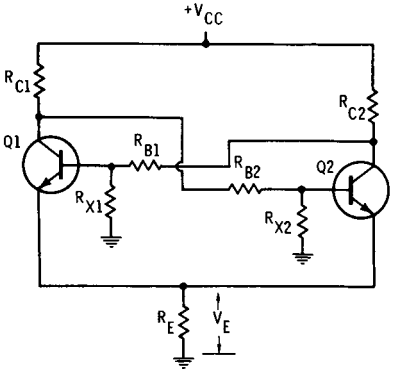


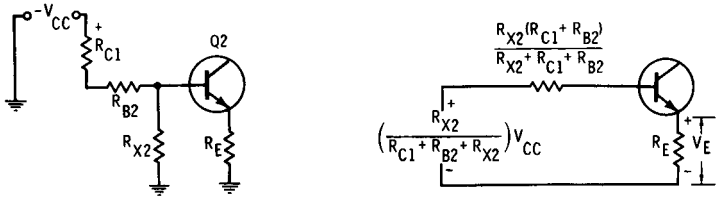
Fig. 13-3. Bistable multivibrator using one power supply.

discussion in the previous chapter. Similarly, the V_{CE} saturation voltage can be included in the equation determining the *off* voltage.

A bistable circuit requiring only one power supply is shown in Fig. 13-3. The voltage required to bias the transistor off, replacing $-V_{BB}$, is developed across the emitter resistor, R_E. Since there is current through one transistor while the other transistor is turned off, the voltage across R_E is equal to the saturation current of one transistor multiplied by the value of the emitter resistor.

When Q1 is off, there is only the sum of the current through R_{X2} and the base current of transistor Q2 through R_{C1}. The base circuit for Q2 is shown in Fig. 13-4A. It can be calculated with the Thevenin theorem described in Chapter 3. Breaking the connection at Q2, the voltage across R_{X2} is $[R_{X2}/(R_{C1}+R_{B2}+R_{X2})][V_{CC}]$, and the resistance seen looking across R_{X2} when V_{CC} is shorted is R_{X2} in parallel with the series combination of R_{C1} and R_{B2}. This is $R_{X2}\ (R_{C1}+R_{B2})/(R_{X2}+R_{C1}+R_{B2})$. The complete Thevenin equivalent of the base circuit is shown in Fig. 13-4B.

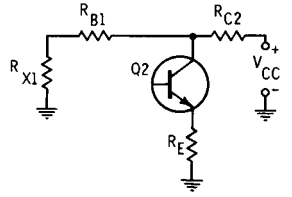
The collector circuit of Q2 can likewise be calculated. Using the circuit in Fig. 13-5A, break the connection at the collector of Q2. The voltage across $R_{B1}+R_{X1}$ is $[(R_{B1}+R_{X1})/(R_{B1}+R_{X1}+R_{C2})][V_{CC}]$. Looking back across R_{C2}, the Thevenin resistance is R_{C2} in parallel with the sum of R_{B1} and R_{X1}, or $R_{C2}\ (R_{B1}+R_{X1})/(R_{C2}+R_{B1}+R_{X1})$. The Thevenin equivalent of the collector circuit is shown in Fig. 13-5B.



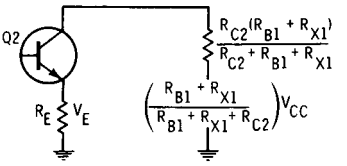
(A) Base of ON transistor, Q2 of Fig. 13-3. (B) Thevenin equivalent of Q2 base circuit.

Fig. 13-4. Base of ON transistor and Thevenin equivalent.

The base current is determined from Fig. 13-4B. Assuming zero volts across Q2, the collector is in saturation when the collector voltage, divided by the load resistor in Fig. 13-5B, is less than the possible collector current that is due to the base current. If the collector current just determined is less than βI_B, the transistor is in saturation.



(A) Collector circuit of ON transistor, Fig. 13-3.



(B) Thevenin equivalent of circuit in Fig. 13-5A.

Fig. 13-5. Collector circuit of ON transistor and Thevenin equivalent.

As Q2 is in saturation, Q1 must be off. Because Q2 is in saturation, the voltage across the transistor is approximately zero and the collector of Q2 is at $+V_E$ volts. This voltage is divided between R_{B1} and R_{X1}. It appears across R_{X1} as $[R_{X1}/(R_{X1}+R_{B1})][V_E]$. The voltage at the base of Q1 (see Fig. 13-6) can be found by subtracting the voltage across R_{X1} from V_E, because they are two opposing voltages connected in series with the base-emitter diode of Q1. If the voltages are of the proper magnitude, the transistor is cut off.

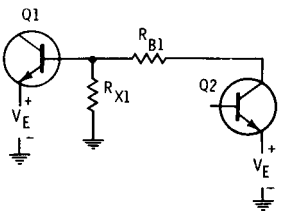


Fig. 13-6. OFF transistor of Fig. 13-3.

As before, the various saturation voltages across the transistor were not considered in the discussion. The calculations, as stated, can provide sufficiently accurate results. More precise calculations can be made using the saturation voltages and currents specified by the manufacturer of the particular transistor. The approximations stated in the previous chapter may be used.

In all circuits presented thus far, capacitors may be provided to shunt R_{B1} and R_{B2} to increase the switching speed, as described in Chapter 12.

A current-mode bistable multivibrator is used to improve switching speeds. The design must include some means of preventing the *on* transistor from going into saturation.

THE MONOSTABLE MULTIVIBRATOR

The monostable multivibrator has one stable state and one quasi-stable state. In Fig. 13-7, while the negative base supply voltage, $-V_{BB}$, acting through R_X keeps Q2 turned off, V_{CC} and R_{B1} supply the proper current to the base of Q1 to keep that transistor in saturation. C1 is used to couple any pulse that may appear at the collector of Q2 to the base of Q1. C2 is the speed-up or commutating capacitor discussed in the last chapter. The states are switched by applying a negative pulse to the base of Q1 or collector of Q2, thus turning off Q1.

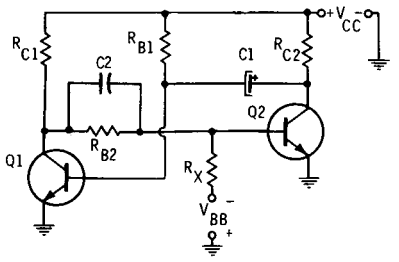


Fig. 13-7. Monostable multivibrator.

Throughout the following description, it will be assumed that the *off* transistor conducts zero current so that the voltage across the collector resistor of that transistor, due to the collector current, is zero. It will also be assumed that the *on* transistor is in saturation. In this case, the entire voltage drop is across the collector resistor and the voltage across the transistor is zero.

In the stable state, with Q2 off, the collector of Q2 is at $+V_{CC}$. The base of Q1 is slightly above ground potential. The voltage across C1, connected between these two points, is almost equal to V_{CC}, and C1 is charged with the polarity as shown.

Should Q1 be switched off, the collector voltage at Q1 will increase almost to $+V_{CC}$. The only voltage drop across R_{C1} will be due to the base current through Q2. The high positive collector voltage at Q1, when acting through R_{B2}, opposes the negative base voltage at Q2 due to $-V_{BB}$. Q2 will be turned on. When it is in saturation, the voltage at the collector of Q2 will be zero or at ground potential. The end of C1 connected to the collector is at ground potential. Since C1 retains its charge, it will bias the base of Q1 negative with respect to ground, cutting Q1 off until C1 discharges through Q2 and R_{B1}. The transistors will then revert to their stable states.

R_{B1} must be connected to a large voltage, preferably $+V_{CC}$ as shown in the drawing, if C1 is to discharge readily. The discharge time of C1 is equal to $0.69R_{B1}(C1)$. It increases somewhat with an increase in temperature, but the effect of the temperature on the discharge time is diminished if V_{CC} is large.

In the stable state, the collector current of the normally *on* transistor, Q1, is approximately V_{CC}/R_{C1} when the transistor is in saturation. The base current of this transistor is about equal to V_{CC}/R_{B1}. The transistor will be in saturation if the minimum collector current required for saturation, V_{CC}/R_{C1}, is equal to or less than beta multiplied by the base current, V_{CC}/R_{B1}.

As for the *off* transistor, the voltage present from the base to emitter of Q2 can be determined using the superposition methods discussed above. In this case, the saturation voltage of Q1 cannot be ignored. We will refer to it as $V_{CE}(sat)$. This is the voltage from the collector to ground of Q1.

Applying superimposition methods, first short $-V_{BB}$. The voltage at the base of Q2 due to $V_{CE}(sat)$ is $[R_X/(R_{B2}+R_X)]$ $[V_{CE}$ sat$]$.

Next, restore $-V_{BB}$ into the circuit and short $V_{CE}(sat)$. The collector of Q1 is thus shorted to ground. The voltage at the base of Q2 due to $-V_{BB}$ is $[R_{B2}/(R_{B2}+R_X)][-V_{BB}]$.

The voltage from the base to emitter is the sum of these two voltages or $-[V_{BB}R_{B2}-V_{CE}(sat)\ (R_X)]/(R_{B2}+R_X)$. The transistor is usually off when the base-emitter voltage is more negative than -0.1 for a germanium transistor and more negative than zero for a silicon device.

THE ASTABLE MULTIVIBRATOR

Neither of the two transistors remains indefinitely in any one state when they are arranged in an astable multivibrator circuit similar to that shown in Fig. 13-8. They keep alternating between *on* and *off* states despite the absence of an applied signal or pulse. Effectively, this circuit is the basis of a square-wave oscillator with feedback from the collector of one transistor to the base of the other.

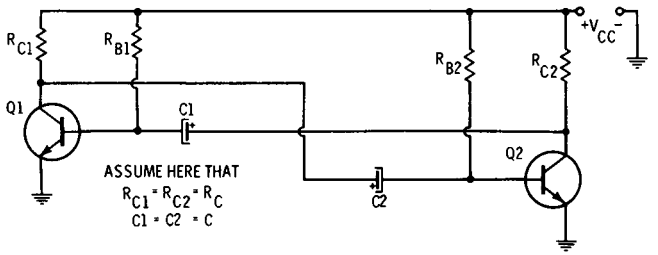


Fig. 13-8. Astable multivibrator.

Assume for the moment that Q1 is on and Q2 is off. The collector of Q2 is at the supply potential, V_{CC}. The collector of Q1 is near ground potential. (It is at $V_{CE}(sat)$ with respect to ground.) Since C2 has been charged during the previous half-cycle, there is a voltage across the capacitor in the direction noted in the drawing. The positive end is at ground

potential because the collector of Q1 is a ground. The negative end makes the base of Q2 negative with respect to ground, cutting it *off*.

While C1 is charging (through the base circuit of Q1 and through R_{C2}) to V_{CC} with the polarity as shown, C2 is discharging through R_{B2}. When the process has been completed, Q1 will be turned off and Q2 will be turned on.

The time for one half-cycle of the square wave is $0.69R_{B1}$ (C1), and the time for the second half-cycle is $0.69R_{B2}$ (C2). The time for a complete cycle is the sum of the two factors, and the frequency of oscillation

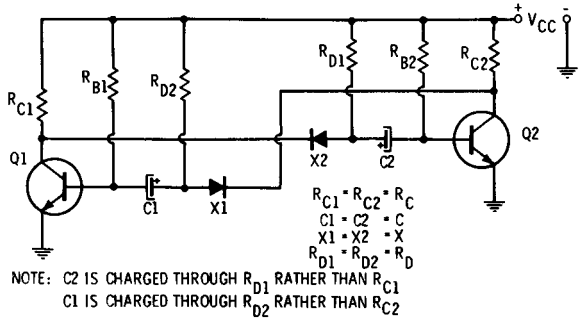


Fig. 13-9. Improved astable multivibrator.

is the reciprocal of this sum. If $C1 = C2 = C$ and $R_{B1} = R_{B2} = R_B$, the frequency of oscillation is $1/1.38(R_B)(C)$.

The circuit in Fig. 13-8 does generate square waves, but the rise time is poor. It is limited by the product of R_C and C, the time constant of the circuit. The presence of the time constant does not permit the collector voltage to jump to V_{CC} at the instant the *on* transistor is turned off, for there must be current through R_C to charge C while the states are being switched. Because of the delay in reaching the final collector voltage, V_{CC}, the leading edge of the square wave is frequently rounded rather than square. This drawback may be overcome with the help of the circuit in Fig. 13-9.

In Fig. 13-8, the collector voltage of the transistor that gets turned off rises from zero to $+V_{CC}$. However, it rises on an exponential basis due to the presence and the charging of C and the time constant R_CC. In Fig. 13-9, a diode is between R_C and C. The current through R_C cannot charge C because of the polarity of the diode. Hence, at the instant the *on* transistor turns off, its collector jumps to $+V_{CC}$ volts because there is no charging current through R_C and hence no time delay due to the R_CC time constant. The time constant is theoretically zero. C is charged through R_D rather than R_C. The frequency of oscillation is as stated for the circuit in Fig. 13-8.

Chapter 14

VOLTAGE REGULATORS

Zener diode circuit design procedures were outlined in the first chapter. The discussion was based on the fact that once the diode is biased in the reverse breakdown region, the voltage across the diode is relatively constant despite the variation in applied voltage to the overall circuit. The voltage across any load connected in parallel with the diode is equal to the diode breakdown voltage.

As a side benefit, the ripple across the diode and load is less than the raw power supply ripple because of the low ac diode impedance across the load. The circuit in Fig. 1-20 consists of a large resistor, R_s, in series with the low ac impedance of the zener diode. Due to voltage divider action, the ripple in the power supply is primarily developed across the large series resistor while very little ripple remains for the diode and load. Ripple is reduced when the series resistor is large and the zener diode impedance is small.

There are several practical design problems associated with this circuit. It is not always possible to obtain low-impedance zeners. The size of R_s is limited, because it must conduct all the load current as well as the zener diode current. Yet, the voltage across R_s must be of such dimensions that the zener diode is maintained in the breakdown region.

To overcome the drawbacks, the regulator R_s-zener diode circuit can be isolated from the load. The regulating circuit can be in the base circuit of a transistor, and the load may be placed in the emitter circuit. The zener diode will regulate the base circuit voltages directly, and, consequently, the voltage across the load in the emitter will remain constant. The base current is approximately equal to the load current divided by the beta of the transistor in question.

Regulator circuits can be conveniently divided into three groups—series, shunt, and feedback. The placement of the output load with respect to the transistor in the regulating circuit is the primary factor in determining if

the arrangement is a shunt or series regulator. Feedback may be applied to either circuit. In the feedback regulator circuit, usually of the series type, a portion of the output voltage is sensed and fed back to the regulating circuit for proper compensation.

SERIES REGULATOR

The series regulator in Fig. 14-1 is essentially an emitter follower with the potential from the base to ground maintained at the zener breakdown voltage. Since the emitter is a fixed voltage away from the base, the voltage across the load is also constant with respect to ground.

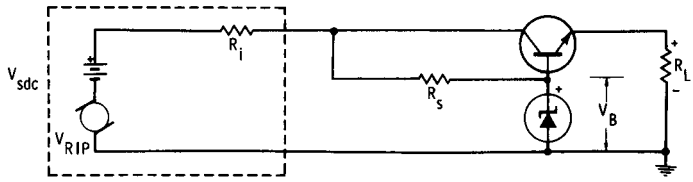


Fig. 14-1. Series regulator.

The dc portion of the unstable power supply is a voltage, V_{sdc}, in series with the internal impedance, R_i. Similarly, the ripple voltage in the supply is V_{RIP}. The path of the load and zener current is through R_i with the latter current being negligibly small. R_s, the resistor in series with the zener diode, limits zener current to safe values. Zener and base current are both through R_s. The voltage across the load resistor, R_L, is equal to the breakdown voltage, V_B, across the zener diode minus the base-emitter voltage of the transistor. Being in the active region, the base-emitter voltage of a germanium transistor will be assumed at 0.2 volt and that of a silicon transistor will be assumed at 0.6 volt. The transistor should be kept out of saturation at all times.

Regulation is improved if the output impedance of the transistor is small. According to Equation 5-21, the output impedance of an emitter follower is equal to the emitter resistance, r_e, of the transistor added to the impedance in the base circuit divided by beta, or $r_e + (r_b + R_z)/\beta$, where r_b is the base resistance and R_z is the zener diode impedance. This combination is in parallel with the load, R_L.

The emitter resistance, r_e, is a very important factor in setting the output impedance. It is equal to $26/I_E$, where I_E is the emitter current expressed in milliamps. I_E can be increased to make r_e and the output impedance smaller by shunting the load resistor, R_L, with a second resistor, R_E.

Once the operation of the series regulator is understood, the design of a circuit is conventional. As a numerical example, assume that 17.4 volts dc is to be developed across a load. The load current is to vary from 0.2 to 0.4 amp, depending on the input signal (assuming the load is a class-B

power amplifier), with ambient temperatures ranging up to 60°C. A dc supply voltage is available that will produce 36 volts when delivering 0.1 amp and 30 volts when delivering 0.5 amp. With normal line variations, the open circuit dc supply voltage can vary from 32 to 42 volts. Five percent ripple voltage is present on the dc supply. Hence, the input ripple voltage varies from $5/100 \times 32$ volts $= 1.6$ volts up to $5/100 \times 42$ volts $=$ 2.1 volts. The output ripple voltage should be kept to less than 0.5% or $5/1000 \times 17.4 = 0.087$ volt. Use the circuit in Fig. 14-1.

The impedance of the voltage source can be determined from the relationships between the supply voltage and supply current. It is $R_i = (36$ volts $- 30$ volts$)/(0.5$ amp $- 0.1$ amp$) = 15$ ohms.

The maximum base current through the transistor is approximately equal to the maximum emitter current divided by the beta of the transistor. Assuming that the beta is 80, the maximum base current is 0.4 amps$/80 = 5 \times 10^{-3}$ amps. As discussed in Chapter 1, there is minimum zener current when the regulated current through the load is at a maximum. The minimum zener current is usually taken as 1/10 the maximum base current or 5×10^{-4} amps. The zener and base current is $(5 \times 10^{-3}) + (5 \times 10^{-4}) = 5.5 \times 10^{-3}$ amps.

The voltage across the output load plus the voltage across the base-emitter junction of the transistor are equal to the breakdown voltage of the zener diode. In a silicon device, $V_B = 17.4$ volts $+ 0.6$ volt $= 18$ volts.

The voltage across R_i, with the maximum current through the load is the resistance of the supply multiplied by the load current. If the base and zener currents are negligible, the voltage across R_i is 15 ohms $\times$ 0.4 amp $= 6$ volts.

The minimum supply voltage is 32 volts. The minimum voltage across R_s is the open circuit supply voltage, minus the zener diode breakdown voltage, minus the maximum voltage across the internal resistance of the supply, or $32 - 18 - 6 = 8$ volts. Hence, R_s should equal the minimum voltage across the resistor divided by the maximum current through that resistor, or 8 volts$/5.5 \times 10^{-3}$ amps $= 1450$ ohms.

The transistor must not be in saturation at any time. When a silicon transistor is in saturation, the collector emitter voltage is at about 0.3 and for a germanium transistor, the voltage is about 0.1. It can safely be assumed that if there are several volts across the transistor, it is not in saturation. The base-to-collector voltage is equal to that across R_s, or 8 volts, and the base-emitter voltage is 0.6. Hence, there is $8 + 0.6 = 8.6$ volts across the transistor. It is definitely not in saturation.

The minimum base current is equal to the minimum emitter current divided by beta, minus the I_{CBO} of the transistor at the maximum temperature. Assume that the transistor to be used has a maximum I_{CBO} of 1 microamp at 25°C. The silicon transistor can operate properly up to a junction temperature of 175°C. Using Fig. 4-2, I_{CBO} at 175°C is $(32 \times 10^6)(1 \times 10^{-6}) = 32$ mA. Also, the minimum emitter current divided

by beta is 0.2 amp/100 = 2 mA. The minimum base current is thus negative, equal to 2 mA − 32 mA = −30 mA.

The maximum power dissipated by the zener diode is equal to the breakdown voltage, V_B, multiplied by the maximum zener current. The current through the zener is at a maximum when the emitter and hence

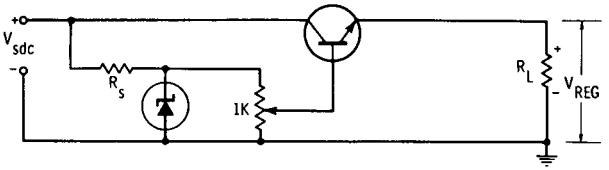


Fig. 14-2. Variable output from series regulator.

base current are at a minimum and the supply voltage is at a maximum. In this case, the voltage across $R_s + R_i$ is equal to:

$$[I_B(\min) + I_z(\max)]R_s + [I_B(\min) + I_E(\min) + I_z(\max)]R_i = V_{sdc}(\max) - V_B \quad (14\text{-}1)$$

where,

$I_B(\min)$ is the minimum base current,
$I_z(\max)$ is the maximum zener diode current,
$I_E(\min)$ is the minimum emitter current,
$V_{sdc}(\max)$ is the maximum open-circuit input voltage,
V_B is the breakdown voltage of the zener diode.

Substitute the numbers from the problem into Equation 14-1 to determine the maximum zener current:

$$[(-30 \times 10^{-3}) + I_z(\max)][1.45 \times 10^3] + [(-30 \times 10^{-3}) + (200 \times 10^{-3}) + I_z(\max)][15] = 42 - 18 = 24 \text{ volts}$$

Solve the equation for $I_z(\max)$. It is equal to .0436 amp. Hence, the power dissipated by the diode is 18 volts × .0436 amp = 0.785 watt.

Now determine the required maximum zener diode resistance. The maximum ripple from the supply, V_{RIP}, is 2.1 volts. The current due to this voltage is through the collector and base circuits. The impedance of the collector circuit approaches r_c, the collector resistance when the impedance in the base circuit approaches zero. It approaches $r_d = r_c/\beta$ when the impedance in the base circuit is high. In this case, due to the zener diode, the collector impedance is very high, about r_c. Therefore, almost all the ripple current through R_i enters R_s, and there is a negligibly small amount through the transistor. The total resistance of $R_i + R_s$ is 1450 + 15 = 1465 ohms. If only 0.087 volt ripple is to appear across the load and hence across the zener diode, the maximum impedance, R_z, of the diode can be calculated by voltage divider arithmetic as follows:

$$0.087 \text{ volt} = \left(\frac{R_z}{R_z + 1465}\right) 2.1$$

$$R_z \leqq 62\,\Omega$$

An 18-volt, 1-watt zener diode with a resistance of considerably less than 62 ohms, is readily available.

The maximum voltage developed between the supply and the emitter of the transistor is the maximum supply voltage less the voltage between the emitter and ground. This is equal to $42 - 17.4 = 24.6$ volts. The maximum power delivered to the transistor by the supply occurs when the transistor and supply impedances are equal. In this case, they would both be 15 ohms. Therefore, the maximum power is dissipated by the transistor when the emitter current is equal to the voltage developed between the supply and emitter terminals divided by twice the internal impedance of the supply. This emitter current is $24.6 \text{ volts}/2(15\Omega) = .82$ amp.

The 0.82 amp emitter current would be a valid number to use in determining the maximum power the transistor will dissipate, if it were less than the maximum load current required from the transistor. However, the maximum load current and maximum transistor current of 0.4 amp, is specified in the problem.

The voltage across the transistor with 0.4 amp through the load is the maximum supply voltage minus the voltage drops across R_i, minus the output voltage. This is equal to:

$$42 \text{ volts} - (15 \text{ ohms})(0.4 \text{ amp}) - 17.4 \text{ volts} = 18.6 \text{ volts}.$$

If a safety factor were to be added, the minimum drop across R_i would be used in determining the voltage across the transistor. Then this voltage is:

$$42 \text{ volts} - (15 \text{ ohms})(0.2 \text{ amp}) - 17.4 \text{ volts} = 21.6 \text{ volts}.$$

The maximum power dissipated by the transistor is 21.6 volts $\times$ 0.4 amp, or 8.64 watts.

The transistor should be capable of dissipating 8.64 watts in an ambient temperature of 60°C. Assuming that there is a permissible junction temperature of 200°C, the 2N3055 transistor should be capable of this. From Equation 6-22, $\theta_{JA} = (T_J - T_A)/P_{diss} = (200°C - 60°C)/8.64 = 16.1°C$ /watt. Since the thermal resistance from the junction to the case, θ_{JC} of the 2N3055 is 1.5°C/watt, $16.1 - 1.5 = 14.6$°C/watt remains as the maximum thermal resistance from the case to the ambient, θ_{CA}. This can be split into two factors—$\theta_{CS} + \theta_{SA}$—the thermal resistance from the case to the heat sink plus the thermal resistance from the heat sink to the surrounding air at ambient temperature. Assuming that a mica washer and silicon grease are used between the case and the heat sink, θ_{CS} is about 0.4°C/W, as discussed in Chapter 6. Hence θ_{SA} can be as high as $14.6 - 0.4 = 14.2$°C /watt. Using the "rule of thumb" in Equation 6-23, the area of the heat sink should be about $1500/\theta_{SA}^2 = 1500/14.2^2 = 7.45$ square inches. A

sink of about ½ (7.45) or 3.73 square inches on each side will be sufficient if the transistor is to operate at ambient temperatures up to 60°C. It is evident that if a larger heat sink is used, a transistor with less thermal capability can be employed.

Should the series transistor used in Fig. 14-1 be incapable of passing sufficient current, several transistors can be connected in parallel. Each transistor in the parallel combination will pass different amounts of current unless the betas of all devices connected in parallel are well matched. It is ideal if all transistors do pass identical amounts of current and thus divide the total current equally among them. A very small resistor may be placed in the emitter lead of each transistor in an attempt to equalize the currents. In the event that two transistors are paralleled, the emitter resistor to be placed in series with each emitter lead can be approximated, as illustrated in the following example.

Assume that there must be 17 amps through the two transistors. If we use the 2N3055, the beta range of the transistor, as specified by the manufacturers, is 20 to 70. In the worst case of mismatch, one transistor will have a beta of 20 and the other a beta of 70. The maximum allowable transistor current is 10 amps. If the transistor with the higher beta passes 10 amps, the base current into that transistor is $10/70 = 0.143$ amp. The lower beta transistor which would carry the remaining 7 amps of current, is to be supplied $7/20 = 0.35$ amp to its base. According to Fig. 6-5D, the base-emitter voltage for the transistor with 0.143 amp through its base is 1.2 volts and the base-emitter voltage for the transistor with 0.35 amp through its base is 1.6 volts. The approximate resistor to be placed in series with each emitter is the difference of the base-emitter voltages divided by the difference in collector currents, or $(1.6 \text{ volts} - 1.2 \text{ volts})/(10 \text{ amps} - 7 \text{ amps}) = 0.4 \text{ volt}/3 \text{ amp} = 0.133$ ohm.

The regulated output voltage can be made variable if the circuit in Fig. 14-2 is used. A potentiometer of about 1000 ohms is placed across the zener diode. The diode is maintained in the breakdown region by the R_s-diode circuit. The regulated voltage is the portion of the zener voltage at the wiper arm of the control minus the base-emitter voltage of the transistor. This is all accomplished at the expense of some of the regulating ability of the circuit.

In either series regulator circuit, it is advantageous to ripple reduction and regulation for the zener diode to see a high impedance. Hence, R_s as well as the impedance the zener sees at the base of the transistor, should both be large. To make the latter impedance large, two emitter-followers arranged in the Darlington pair, as in Fig. 14-3, can be used. The beta of the combination is the product of the betas of the two transistors. As an alternative, any of the complementary beta-multiplying circuits discussed in Chapter 7 may be used. In either case, the zener diode is required to compensate less base current variation than before. As an additional advantage, the output impedance seen by the load, R_L is greatly reduced.

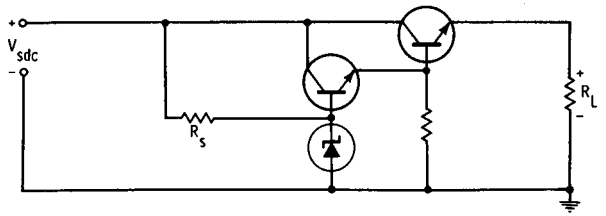


Fig. 14-3. Darlington pair used for better regulation. (Any beta multiplier circuit may be used.)

As for R_s, it should be, ideally, a constant-current source. The constant-current source was discussed in Chapter 11 with reference to the pre-driver circuit. It can be applied to any of the circuits discussed thus far. In Fig. 14-4, it is shown as it may be used with the circuit of Fig. 14-1. As before, the regulated output voltage is equal to the voltage across the zener diode less the base-emitter junction voltage of Q2.

The base current of Q2 is equal to the emitter or load current divided by the beta of that transistor. The collector current of Q1 is the sum of the base current and the current required by the zener diode. The collector current, and hence the emitter current of Q1, is determined by the two series-connected diodes, X1 and X2, as well as resistor R_{E1}. If the diode and transistor are silicon units, the voltage drop across each diode and the base-emitter junction of Q1 is about 0.6 volt. The diodes are connected in parallel with the series combination of R_{E1} and the base-emitter junction. Hence, the voltage from the positive V_{sdc} terminal to the base of Q1 is about 0.6 volt. The diodes are connected in parallel with the series combination of R_{E1} and the base-emitter junction. Hence, the voltage from the positive V_{sdc} terminal to the base of Q1 is 1.2 volts. Since the voltages across X2 and the base-emitter junction of Q1 are each 0.6 volt, the voltage across X1 and R_{E1} must also be 0.6 volt, due to the parallel arrangement. R_{E1} is chosen so that the current through R_{E1} and hence the emitter and collector current of Q1 are all equal to the sum of the base current of Q2 and the current through the zener diode: $R_{E1} = 0.6/(I_z + I_B)$.

Since the voltage at the emitter of Q1 is V_{sdc} minus the voltage across R_{E1}, and the voltage at the collector is the zener voltage, the voltage across

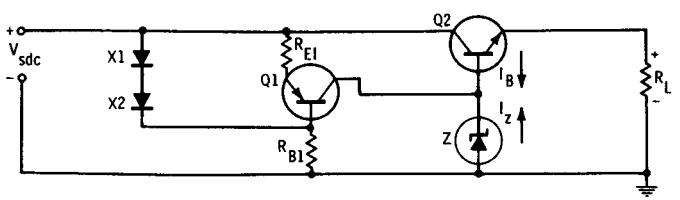
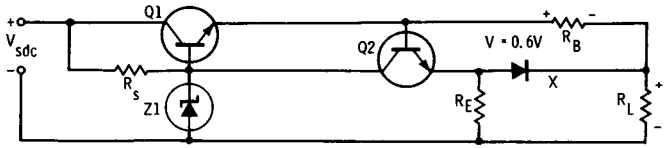


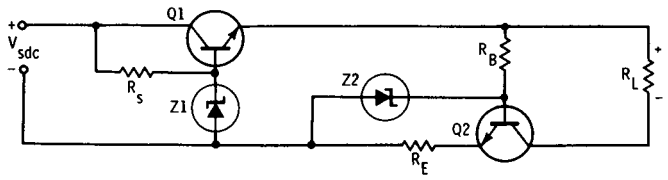
Fig. 14-4. Constant-current source used to replace R_s.

Q1 from emitter to collector is the difference of these two voltages. This, multiplied by the current just derived, is the power this transistor dissipates.

The current through diodes X1 and X2, as well as the current into the base of Q1, must be through R_{B1}. The base current of Q1 is equal to the emitter current just determined, divided by beta. The current through the diodes must be sufficient to keep them conducting, with a voltage drop of about 0.6 volt across each. The voltage across the resistor, R_{B1}, is the supply voltage less the 1.2-volt drop across the two diodes. Therefore, the resistor is equal to the voltage just determined divided by the sum of the diode current and base current of Q1.



(A) R_B, R_{E1}, X_{E1}, and Q2 used for overload protection.



(B) Series regulator with overload-protection components Z2, R_E, R_B, and Q2.

Fig. 14-5. Overload protection.

The impedance presented to the zener by Q1 depends on the size of the resistance in the base of that transistor. If it is low, the impedance seen by the zener diode approaches r_c, the common-base collector resistance; if the resistance is high, the impedance approaches r_d, which is equal to r_c/β, the common-emitter collector resistance.

A serious limitation on the regulator circuit is the series transistor. It is subject to breakdown by an accidental short which can be placed across the regulated output voltage. Circuits have been devised to protect the series transistor from such failure.

One method, used in low-current supplies, employs a current limiter. Should R_L be made equal to zero, a high impedance will appear in series with the shorted load. The circuit returns to normal operation when the short is removed.

Two arrangements are shown in Fig. 14-5. In both circuits, Q1, R_s, and Z1 are the elements ordinarily used in the regulator. The other components comprise the overload protection circuit.

In Fig. 14-5A, Q2 is normally off. Approximately 0.5 volt is required to turn on a silicon transistor and 0.1 volt is required to turn on a germanium device. Assume that Q2 is a silicon transistor and X is a silicon diode. The diode is kept on by virtue of the current through R_E. Being a silicon device, there is 0.6 volt across the diode. The transistor will be turned on when $0.5 + 0.6 = 1.1$ volts is developed from its base to the cathode of the diode (0.5 volt is required from the base to the emitter of the transistor if it is to be turned on). R_B is connected across the two devices. The size of the resistor is set to such value that when there is a predetermined current through the load, 1.1 volts will be developed across R_B, turning on Q2. Q2 will be on when there is any current equal to or greater than this predetermined amount through the load.

When Q2 is on, it draws current from R_s, so that less current remains for the base of Q1. Q1 is partially or entirely turned off, limiting the current through that transistor. Hence, there will be no excess current through Q1. Should the short or partial short be removed from the output, Q2 will be turned off and the regulator will operate normally.

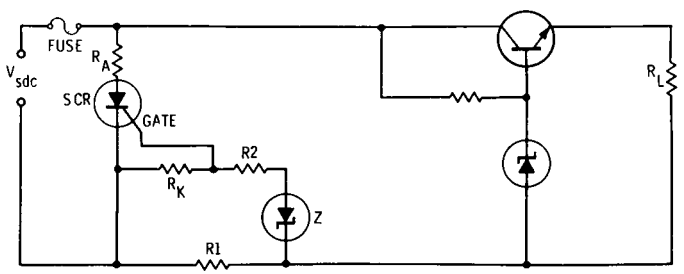


Fig. 14-6. Interruption-type overload protection circuit.

In the system in Fig. 14-5B, R_B keeps Q2 in saturation. Z2 is not in the breakdown region. If the current demanded by the load increases beyond a predetermined value, a relatively large voltage will develop across R_E. This voltage, added to that across the base-emitter junction of Q2, will drive Z2 into the breakdown region. Q2 will come out of saturation providing a high impedance in series with the load. Conditions will be restored to normal when the load current demand is reduced.

The disadvantage of the second circuit is the high power that transistor Q2 must dissipate. The entire load current is through this transistor.

Another method of protection uses a means of interrupting the circuit upon overload. A fast-acting fuse will only race the transistor to destruction. Circuits have been designed which force a large current through the fuse at the moment of overload. One such device, using an SCR (silicon controlled rectifier), is shown in Fig. 14-6. The SCR will be discussed in the next chapter. Suffice it to say here that the SCR is an ordinary diode

that conducts only when a relatively small positive voltage or current (with respect to the cathode) is applied to the third terminal, called the gate.

The SCR in this circuit is normally in a nonconducting state. R1 is chosen so that when a predetermined current flows through the load, the voltage developed across R1 will be sufficient to cause the zener diode, Z, to break down. The breakdown voltage of the diode is low so that R1 can be made small. R1 is equal to the zener breakdown voltage divided by the minimum overload current.

The gate current for the SCR is supplied through the zener diode. When the gate current is equal to or greater than a predetermined value, the SCR will conduct. This high surge of current through the SCR will cause the fuse to open (blow) rapidly. The fuse is chosen so that it will not blow under normal load current, but will blow rapidly once the normal load current is exceeded by a considerable factor. This considerable factor is supplemented by the current flowing through the SCR. R_A limits the SCR surge current to safe values. It is equal to the maximum unregulated voltage, $V_{sdc}(max)$, divided by the maximum allowable surge current through the SCR (or divided by the maximum allowable surge current flowing through the rectifier in the unregulated power supply, if the surge current rating of these rectifiers is less than the surge current of the SCR).

The gate current is set by R_K and R2. R_K is usually about 1000 ohms while R2 is a small resistor limiting the gate current to safe values.

SHUNT REGULATOR

The zener regulators discussed in Chapter 1 were used in shunt regulator circuits. The output load was connected across the diode. Similarly, in the following regulators to be discussed, the load shunts the transistor. In the basic circuit in Fig. 14-7, the voltage from the base to the collector is identical to the breakdown voltage across the zener diode. The voltage from the base to the emitter is the usual voltage developed across a forward-biased diode. As both voltages are relatively constant, a regulated voltage is developed across the series combination of zener diode and the base-emitter junction of the transistor. The load, R_L, is connected across the series circuit.

There are several advantages to this circuit over the zener shunt regulator discussed in Chapter 1. Here, there is only the base current through the diode. A small diode can therefore be used to regulate a large amount

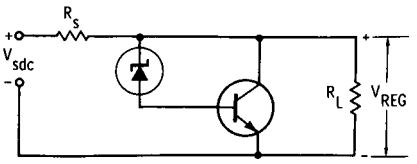


Fig. 14-7. Basic shunt regulator.

of current at the output of the transistor. Furthermore, the regulating capabilities of the circuit are improved by a factor of beta. Add to this the advantage that this circuit (as well as the zener shunt regulator) is short-circuit proof. About the only drawback is the power required from the source. This circuit absorbs more power than does the series regulator arrangement because considerable power is dissipated by R_s.

The current through R_s should remain constant regardless of load-current variations. If the output is shorted, there is no current through the transistor, while all the current is through R_s and the short. If the load, R_L, is infinite, all current will be through R_s and the transistor. In both conditions, the current through R_s is identical. The current through R_s remains constant even when it is divided between the transistor and the load.

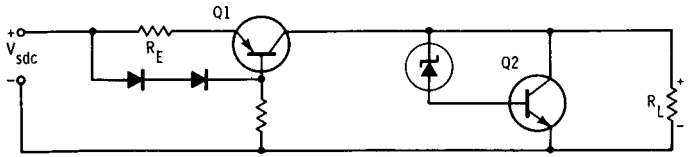


Fig. 14-8. Constant-current source replaces R_s for shunt regulator.

For good voltage regulation, the base and emitter resistances of the transistor, as well as the zener diode resistance, must all be small. The beta of the transistor and the series resistor, R_s, should be large. Since the current through R_s must be constant, the magnitude criterion can be satisfied by replacing R_s with a constant-current source, as shown in Fig. 14-8. The design of the constant-current source has been discussed in the section on series regulator circuits.

Good regulation requires the use of high beta transistors. Extremely high beta can be achieved using the Darlington pair arranged as in Fig. 14-9. The complementary circuits discussed in Chapter 7 may be used as alternates. In either case, the beta is the product of the betas of all transistors in the circuit. The base and zener current is the current through Q2, divided by this product.

The output voltage of the circuit in Fig. 14-7 is slightly greater than the voltage across the zener diode. Should less regulated voltage be re-

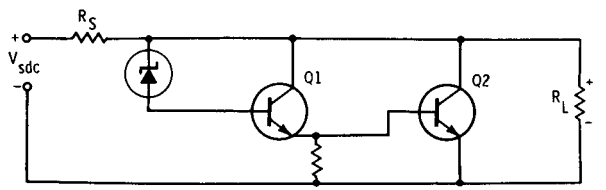


Fig. 14-9. Shunt regulator using Darlington pair.

quired, a voltage divider can be placed across the output. The circuit in Fig. 14-10 can be used if voltages considerably greater than the zener diode voltage are necessary. In this circuit, the output voltage is approximately:

$$V_{REG} = V_B[(R_X + R_B)/R_X] \qquad (14\text{-}2)$$

This follows from voltage divider considerations.

V_{REG} is slightly smaller than V_X. Neglecting the base current, the voltage at V_X is:

$$V_X = V_{sdc} - R_i(I_{out} + I_C) \qquad (14\text{-}3)$$

V_X can be calculated from this equation when R_i, the input impedance of the power supply, is known.

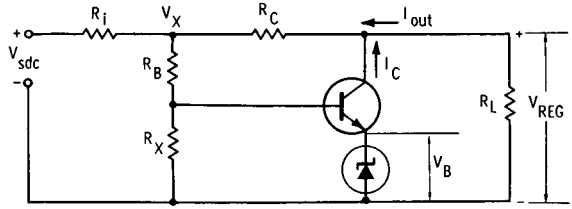


Fig. 14-10. Circuit providing regulated voltage greater than V_Z.

R_C can be determined experimentally. Vary the unregulated input voltage, V_{sdc}, and note the output at V_{REG}. Adjust R_C for the minimum variation of V_{REG} as V_{sdc} is varied. If R_C is made too big, it will be found that V_{REG} will drop as V_{sdc} is increased.

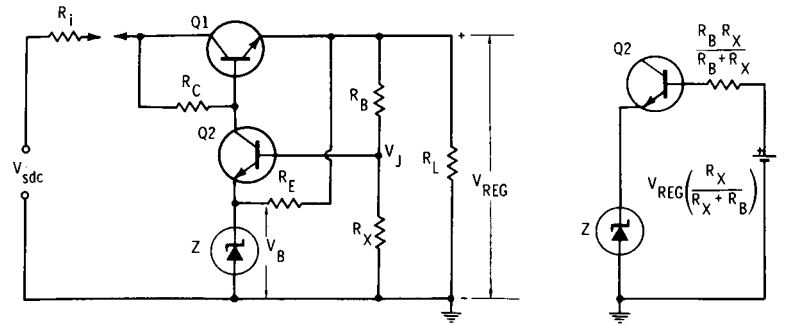
The ripple factor can be improved by connecting a large electrolytic capacitor from the collector to the base of the transistor. A capacitor at this point in the circuit appears as a much larger capacitor when reflected across the output load because of the current gain of the transistor. The output capacitance is approximately equal to $C(R_X/R_Z)$, where R_X is the resistor noted in Fig. 14-10, R_Z is the resistance of the zener diode or a resistor placed in the emitter circuit, and C is the capacitor connected from the collector to the base of the transistor.

FEEDBACK REGULATORS

A voltage regulator can serve one or more functions. It can deliver a regulated output voltage despite line, supply voltage, load resistance, or load current variations. All this was properly accomplished with shunt and series regulators discussed previously. The feedback regulator in Fig. 14-11A uses a variation of the operational amplifier circuit discussed with

respect to Fig. 10-6. It is an improvement over the types of regulating circuits described in the first two sections of this chapter.

In Fig. 14-11A, transistor Q1 responds to changes in relative voltages between the base and emitter of Q2. The regulated output voltage is sampled and applied to the base of Q2. The emitter voltage is maintained constant by virtue of the zener diode. Should the regulated voltage rise, the voltage at the base of Q2 will rise, as will the collector current. Both the base of Q1 and collector of Q2 derive their current through R_C. As current increases through Q2, there is a larger voltage drop across R_C. The lower voltage at the base of Q1 limits the base current. Consequently, the collector and emitter current of Q1, as well as the load current, is reduced, forcing down the voltage across the load resistor. The reverse will be the case should the voltage at the base of Q2 drop. This is the desired result of a voltage regulator.



(A) Feedback regulator. (B) Thevenin equivalent of Q2 base circuit.

Fig. 14-11. Feedback regulator and Thevenin equivalent of base circuit.

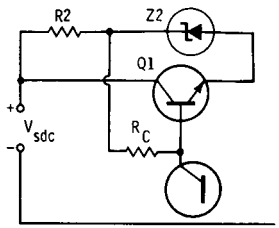
The regulated voltage is developed across R_B and R_X. The voltage at the junction of the resistors is fed back to the base of Q2. This voltage is a sampling of the regulated voltage, V_{REG}, as well as any variation of this regulated voltage. The Thevenin equivalent of the base circuit is a voltage equal to $[R_X(R_X + R_B)][V_{REG}]$, and a series resistance equal to $R_BR_X/(R_B + R_X)$. The sum of R_B and R_X should be much higher than the minimum value of the load resistance, R_L. If this requirement would force the Thevenin resistance to be high, R_B can be replaced with a zener diode. In this case, the Thevenin voltage would be $V_{REG} - V_Z$, where V_Z is the breakdown voltage of the diode replacing R_B, and the Thevenin resistance is slightly less than the resistance of that zener diode.

The voltage at the emitter of Q2 is the breakdown voltage, V_B, of the reference zener diode, Z, shown in the drawing. V_B plus the voltage from the base to the emitter of Q2 is the voltage V_J at the base, and hence at the junction of R_B and R_X. Assuming that R_B and R_X are small, the regulated voltage is a function of the relative sizes of R_B, R_X and V_J. It is approxi-

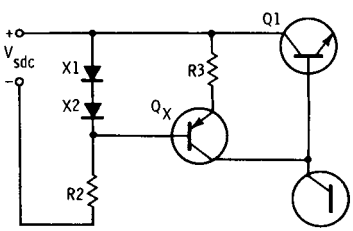
mately equal to $[(R_X + R_B)/R_X)][V_J] = [(R_X + R_B)/R_X][V_B + V_{BE}]$, where V_{BE} is the base-emitter voltage of Q2. Information is fed to Q1 about the variation of V_{BE} due to the change of V_J with respect to the reference voltage, V_B. Q1 reacts to the information by controlling the current fed to the output, maintaining V_{REG} constant.

The zener diode, Z, should be fed from a high impedance source. Most of the current through R_E is through the diode, and very little will be through the emitter of Q2. R_E is ideally a constant-current source.

The base of Q1 is fed current through R_C. Unfortunately, ripple and other variations of the unregulated supply, V_{sdc}, will be amplified by Q1 and appear at the output. Preregulators, using diodes as shown in Fig. 14-12, can be used to minimize many of these changes. In Fig. 14-12A, a constant voltage is developed across Z2, and applied to the base of Q1 through R_C. In Fig. 14-12B, the diodes X1, X2, and transistor Q_X provide a constant current to the base of Q1.



(A) Preregulator circuit using a zener diode.



(B) Preregulator using diodes X1 and X2, and transistor Q_X.

Fig. 14-12. Preregulators.

A problem will illustrate the design procedure. Assume that there is a dc supply varying from 40 to 60 volts. The impedance of the source is 4 ohms. The output load resistance is nominally 50 ohms. The required output is 25 volts. Use the circuit in Fig. 14-11A with any variation that may be required.

The zener diode breakdown voltage should be about half the output voltage. For convenience, it can vary from this value by as much as 70 percent. Since the output is 25 volts, a standard 12-volt diode would be adequate.

The average load current is the required output voltage divided by the nominal load resistance or (25 volts/50 ohms) = 0.5 amp. The current through resistor R_C should be less than 5 percent of the load current, or less than 25 mA. Assume this current to be 10 mA minimum. This is equal to the collector and emitter current of Q2 plus the base current of Q1.

The base current of Q1 should be about 10 percent of the current through R_C. This current is a minimum of $1/10 \times 10$ mA = 1 mA. (Hence, the minimum collector current through Q2 is 9 mA.) The beta of Q1

must be equal to the load current divided by the base current or (500 mA)/(1 mA) = 500. It is difficult to find a transistor with so high a beta; however, two transistors in a Darlington arrangement can be used. This is redrawn as Fig. 14-13. Assume that Q1 has a nominal beta of 25 and Q3 has a nominal beta of 20, so that the beta from the base of Q3 to the collector of Q1 is 25 × 20 = 500.

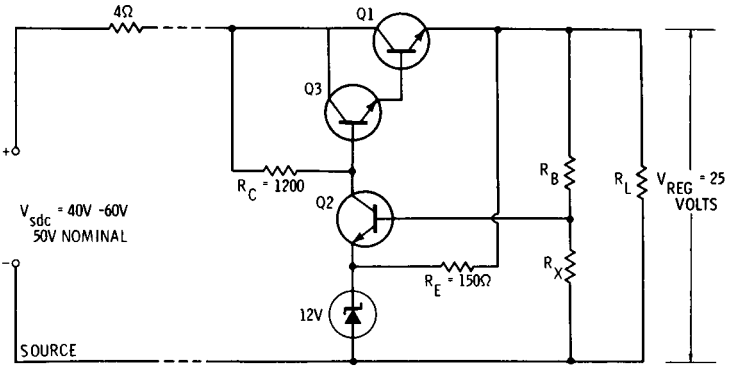


Fig. 14-13. Circuit illustrating solution to problem.

The 0.5 amp through the load is also through the 4-ohm resistance of the supply. The voltage across this resistor is 4 ohms × 0.5 amp, or 2 volts. As the minimum supply voltage is 40 volts, the voltage at the junction of the collectors of Q1 and Q3 and at R_C is 40 − 2 = 38 volts. The voltage at the emitter of Q1 is V_{REG} = 25 volts. Assuming that these are silicon transistors, the voltage from the emitter to the base of Q1 is 0.6, as is the voltage from the emitter to the base of Q3. Hence, the voltage at the base of Q3 is 25 volts plus 2 × 0.6 volt, or 26.2 volts.

The voltage across R_C is the 38 volts previously calculated minus the 26.2 volts, or 11.8 volts. The current through R_C was previously assumed to be 10 mA. R_C is equal to the voltage divided by the current, or (11.8 volts)/(10 mA) = 1180 ohms. A standard 1200-ohm resistor can be used.

The maximum voltage across Q1 and Q2 is the maximum unregulated supply voltage, 60 volts, minus the regulated voltage, 25 volts, which is equal to 35 volts. From this, subtract the 2 volts across the 4-ohm resistor, providing a maximum of 33 volts across Q1 and Q3. The collector current of Q1 is the load current, or 0.5 amp. The power dissipated by Q1 is 33 × 0.5 = 16.5 watts.

The maximum current through R_C is the difference of the maximum supply voltage and the 26.2 volts at the base of Q3, divided by R_C, or (60 − 26.2) volts/1200 ohms = 28 mA. In the absence of a load, where $R_L = \infty$, the entire 28 mA is through the collector of Q2. The voltage at the collector of Q2 is the same as at the base of Q3, or 26.2 volts. The emitter voltage is the breakdown voltage of the zener diode, or 12 volts.

Hence, the voltage from the emitter to the collector of Q2 is 26.2 volts − 12 volts, or 14.2 volts. The power that Q2 must dissipate is 14.2 volts multiplied by 28 mA of 0.397 watt.

The 28 mA of current through the emitter of Q2 is also through the 12-volt zener diode. If this current is sufficient to maintain the zener breakdown voltage at a constant level, the power dissipation capabilities of the diode do not have to exceed 28 mA × 12 volts = 0.335 watt. The diode voltage can be held more constant if it will pass a higher minimum current—let us say an additional current equal to 10 times the amount through Q2, or 100 mA. Resistor R_E will supply this additional current. The voltage across R_E is the regulated voltage minus the voltage across the zener diode, or 25 volts − 12 volts = 13 volts. Assuming that there is 100 mA additional zener current, R_E is 13 volts divided by 100 mA or 130 ohms. A standard 150-ohm, 10-percent resistor can be used.

The current through R_B and R_X should be much less than the current through R_L. Assume this current to be 1/100 of the current through R_L or 0.5 amp/100 = 5 mA. Since the voltage across R_X is approximately equal to the voltage across the zener diode plus the approximate 0.6 volt present from the base to the emitter of Q2, or 12.6 volts divided by 5 mA, R_X is found to equal 2520 ohms. A standard 2700-ohm resistor should be used.

The voltage across resistor R_B is the regulated voltage minus the voltage across R_X, or 25 volts − 12.6 volts = 12.4 volts. Since the current through this resistor is also 5 mA, R_B is equal to (12.4 volts)/(5 mA) = 2480 ohms. Use a standard 2200-ohm resistor.

The ratio of R_B to R_X can be adjusted in the laboratory for an accurate 25-volt regulated output. All other calculations should likewise be checked in the laboratory.

Chapter 15

THREE-TERMINAL SEMICONDUCTORS

The bipolar transistor considered throughout the text is not the only three-terminal semiconductor. The silicon controlled rectifier and unijunction transistor have been used extensively for many years, while the field-effect transistor is now just about as popular as its bipolar counterpart.

Other types of semiconductor devices are also being produced. We will devote the bulk of this chapter to the three popular ones just noted. In one chapter, it is impossible to present details of any one of these devices, let alone all three. However, device characteristics and limitations as well as design procedures, will be noted.

The first device to be considered is the thyristor or silicon controlled rectifier, abbreviated SCR. An application of this device was discussed in the previous chapter concerning a protection circuit for a power supply.

THE SCR

The SCR is basically a silicon diode. As with all other diodes, there is no conduction when it is reverse-biased (anode is negative with respect to the cathode) except when the reverse breakdown voltage is exceeded. Furthermore, the SCR does not conduct even when forward-biased except when the forward breakdown or breakover voltage is exceeded. The forward and reverse breakdown voltages are about equal.

The silicon diode can best be explained with the help of the curve in Fig. 15-1A and the circuit in Fig. 15-1B. When the diode is reverse-biased, the leakage current is small and less than the reverse blocking current, I_{RRM}, until the voltage V_{RRM} is exceeded. V_{RRM} is the peak-inverse voltage that may be repetitively applied across the diode. A higher voltage, V_{RSM}, is a transient or surge voltage that may be applied only on a nonrepetitive basis. The maximum permissible duration of the reverse surge current, I_{RSM}, for a half-cycle surge pulse, is 8.5 milliseconds.

If the diode is forward-biased, it will not conduct until the repetitive forward blocking voltage, V_{DRM}, is exceeded. The forward blocking current is I_{DRM}. When the forward voltage becomes as large as the breakover voltage, $V_{(BO)}$, it will drop instantly to V_{TM1}. (The difference voltage between V_{BO} and V_{TM1} is developed across R_L in Fig. 15-1B). The SCR current will then rise rapidly as the voltage across the diode is increased. In this portion of its operating characteristic, the device behaves much as

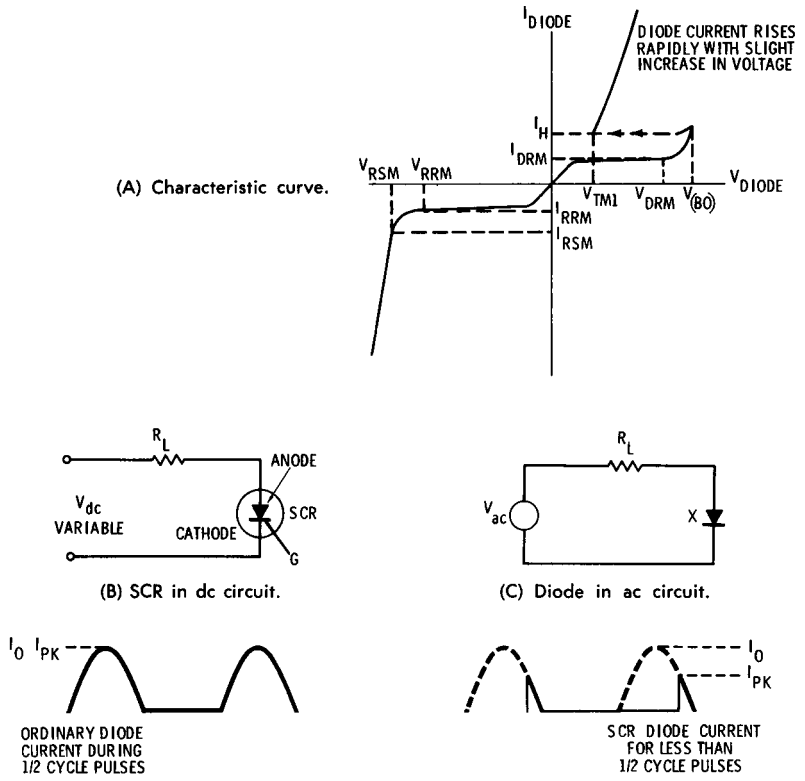


Fig. 15-1. Characteristics and application of SCR.

any ordinary silicon diode. The SCR will stop conducting only when the diode current drops below the holding current, I_H.

In Fig. 15-1B, the SCR is shown with a third terminal, marked G, for gate. This terminal forms a diode with the cathode of the SCR. If this terminal is made positive with respect to the cathode, even for a short period of time, the SCR will conduct even if the applied voltage is less than $V_{(BO)}$. The more positive the gate pulse is, the lower will be the

anode voltage required to put the SCR into the conducting mode. Published specifications indicate the gate current required to trigger the SCR when a specific voltage is applied between the anode and cathode. I_{GD} is the maximum gate current and V_{GD} is the maximum gate voltage that will not cause the SCR to be turned on.

Although gate triggering is the most desirable method to turn on the SCR, several other less orthodox methods can be used. Some of these are: the voltage from the anode to the cathode may be made much larger than its rated value; a voltage may be suddenly applied across the SCR; and the device may be subjected to high temperatures.

SCRs are rated for the maximum transient voltage that may be applied between the anode and cathode without causing the device to turn on. This is specified by a dv/dt rating, where dv is a change or increment in voltage, while dt, is a change or increment in time. Using the rating for the Westinghouse 2N690 as an example, dv/dt is specified at 100 volts per microsecond. If the slope of any pulse applied to the SCR is greater than this, the SCR will probably turn on. To avoid undesirable triggering from a sudden transient voltage, a 0.05-μF capacitor may be connected from the gate to the cathode.

Leakage current may be of sufficient magnitude to trigger the SCR. The device may be stabilized against such objectionable triggering by connecting from the cathode to the gate, a resistor of a value specified by the manufacturer of the device. The resistor should be as small as practical. The same result can be achieved by reverse-biasing the gate-cathode diode.

Even though large gate current pulses, I_g, can be used to trigger the SCR when voltages less than $V_{(BO)}$ are applied, the gate cannot turn the SCR off. It will stop conducting only when the current drops below I_H or a reverse voltage is applied across the SCR. When the device has been triggered, the gate no longer exerts any influence over its operation.

The gate must be driven sufficiently to be certain it will trigger the diode. The required firing current is inversely related to temperature. The gate current is limited by the maximum power, P_{GM}, it can dissipate, as well as by its maximum gate current, i_{GFM}, rating. Care must be exercised not to exceed the maximum reverse voltage, V_{GRM}, that may be applied between the gate and cathode, as well as the maximum current, i_{GR}, the gate may carry in the reverse direction.

Should the SCR be reverse-biased while the gate is positive, the reverse leakage current of the diode will increase considerably. Under these conditions, the SCR will dissipate extra power. The situation can be alleviated by connecting a series resistor-diode combination from the anode to the gate, with the cathode end of the diode connected to the anode of the SCR. The gate is thus clamped to the negative anode, reducing conduction from the gate to the cathode.

The gate may be fired from a low-impedance voltage source or a high-impedance current source. (The unijunction transistor, to be discussed in

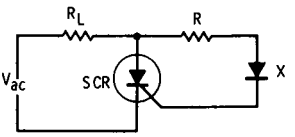


Fig. 15-2. Gate is fired from ac supply.

the next section, is frequently used for this purpose.) The circuit in Fig. 15-2 utilizes the ac supply applied to the SCR diode for triggering purposes. During the portion of the cycle when the upper power supply terminal is positive with respect to the lower one, diode X conducts, and the SCR is turned on. As for the second portion of the cycle, the reverse anode-cathode voltage on the SCR turns it off, and there is no voltage at the gate due to the diode, X.

The gate signal initiates the action of the SCR, but the SCR does not react instantly. There is a delay time, t_d, which extends from the instant the gate is fired until the SCR diode current reaches 10 percent of maximum value. Next, there is the rise time, t_r during which the diode current rises from 10 percent to 90 percent of its final value. The turn-on time, t_{on}, defined as the sum of the delay time and the rise time, depends primarily on the size of the gate pulse and indicates the time it takes the SCR to respond to the signal issued by the gate.

Similar to the turn-on time, there is a turn-off time. A reverse voltage across the SCR causes the diode to cease conducting. The diode current is reversed for a short period of time and then gradually returns to zero. The gate regains control of the situation only after the SCR is once again forward-biased. The period of time from when the diode current turns negative until the gate once again regains control is t_o, the turn-off time. The turn-on and turn-off times are serious limitations of the SCR. The turn-off time of low-current devices can be decreased by reverse-biasing the gate.

In the simple diode, it has been assumed that there is current for a full half of the sinusoidal cycle. Considering this, it is relatively simple to determine the peak, average, and rms current through the diode circuit. The peak current during a half-cycle, I_O, is V_{PK}/R_L, where V_{PK} is the peak voltage applied across the diode and load, R_L, as in Fig. 15-1C. For an ordinary diode that conducts for a full half-cycle, I_O is equal to I_{PK}. (See Fig. 15-1D). The average diode current, I_{AV}, during the conducting period for the full half-cycle is I_{PK}/π. The rms current for the full half-cycle is $I_{PK}/2$.

In the case of the SCR, triggering can be arranged so that the SCR will conduct for less than a half-cycle. Conduction can start after the cycle has passed through its peak. However, had there been conduction through the entire half of the cycle, I_O, the peak current would remain at V_{PK}/R_L. The peak current while the diode is in the conducting mode is I_{pk}. It is equal to the peak voltage across the circuit divided by R_L. The relationship between the four currents, I_O, I_{PK}, I_{AV}, and I_{RMS}, for diode conduction for

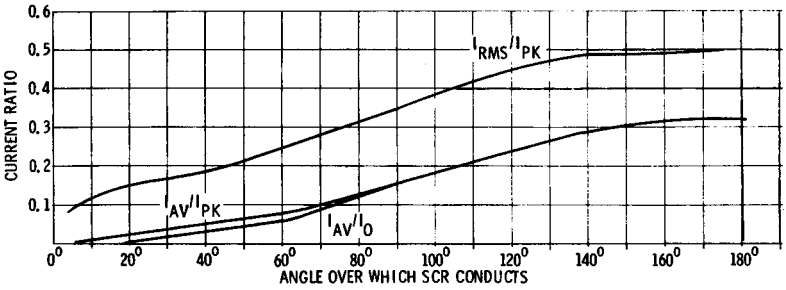


Fig. 15-3. Ratio of current through SCR for various conduction angles.

less than half a cycle, can be determined from Fig. 15-3. The power dissipated by the device is dependent upon the conduction angle. The heat generated by the power, as well as the heat sink requirements, have been discussed in Chapter 6.

Several precautions must be observed to avoid breakdown of an SCR. If an SCR is turned on slowly by the gate, there will be conduction through a small area of the semiconductor material in the diode which will produce hot spots in portions of the semiconductor. This may be avoided by turning the gate on with a large pulse. In an alternate method, the anode current rise time may be made so that the current will be low until the gate is fully turned on.

Forward-current transients can destroy diodes. While triggering the SCR due to a high dv/dt will not damage the device, the SCR cannot withstand, without damage, current pulses sharper than di/dt, at any time in the cycle. The increment or change in current is noted by di. A high di/dt will generate concentrations of heat within limited areas inside the chip of the device. Adding a capacitor from the anode to the cathode will suppress the transients. However, this capacitor will discharge through the SCR diode each time it is turned on, resulting in eventual breakdown. A resistor placed in series with the capacitor will alleviate this situation. The resistor may be about double the size of the load resistance.

Precautions must also be taken when more than one diode is connected into a circuit. The gates must be carefully turned on in the proper sequence or simultaneously. Should several SCRs be connected in series, each diode should be shunted with a parallel resistor-capacitor combination. The capacitor value ranges from 0.01 μF to 0.05 μF. The maximum size of the resistor can be determined as follows:

1. Subtract the maximum peak voltage, V_{PK}, that appears across all the SCRs connected in series, from the maximum voltage that may, from the ratings, be placed across the series string of diodes. The latter figure is the rated repetitive peak voltage per diode multiplied by the number of diodes connected in series.

2. Divide this by the number of diodes in the series circuit, minus one. Thus, if there are five diodes, divide the number determined in Step 1, by 4.
3. Multiply the result by 50 if the average forward current (from the rating) through the diode is at most 5 amps; multiply by 30 if the average current rating is up to 15 amps; multiply by 10 if the average current rating is up to 50 amps. Choose the largest multiplication factor from the above that may be used for the rating of the particular diode.
4. The resistor is determined from the previous three steps. The results are maximum values, and smaller resistors are most desirable. The resistors should be within a few percent of each other in actual value.

If SCRs are connected in parallel, resistors should be inserted in parallel with each gate lead to equalize the various gate impedances. The gates must be fired simultaneously. Means should also be provided so that the SCR diode currents will be divided equally among all diodes. Matched pairs may be used: An equal resistor may be placed in series with each diode. The total current through all SCRs connected in parallel should, for safety, be kept to about 80 percent of the rated current of all diodes in the circuit.

Just as the npn and pnp transistors are complementary devices, the SCR has its complementary counterpart, the PUT (Programmable Unijunction Transistor). Introduced by General Electric several years ago, the device behaves exactly as an SCR with but one exception. In order to turn on the PUT, a negative pulse is required at the gate with respect to the anode.

Other Thyristors

There are a number of variations of the SCR just described. The schematics of some of these devices are shown in Fig. 15-4.

While the SCR uses a positive voltage or current between the gate and cathode to turn the diode on, the LASCR (Light Activated Silicon Controlled Rectifier) can also be turned on by letting light hit an exposed portion of the device.

Another thyristor, the triac, is the equivalent of an SCR which can be triggered by bi-directional gate pulses to conduct in both directions, providing there is current during both halves of a cycle.

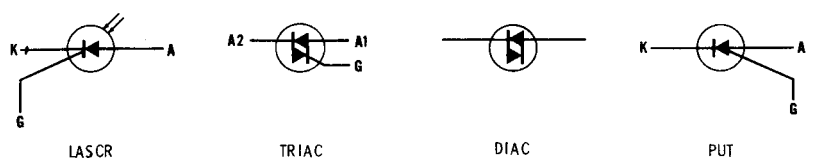
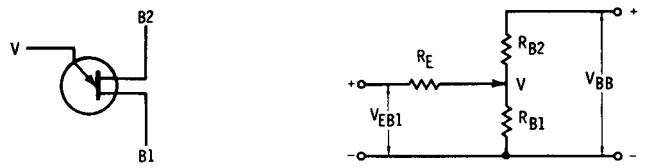


Fig. 15-4. Thyristors and triggers.

All of these devices are best turned on by a pulse applied to the gate. The Unijunction transistor can develop the required pulse for the SCR. The diac is a bi-direction device used to trigger triacs. The characteristic is such that it will not conduct in either direction until its breakover voltage is exceeded. Once the breakover is exceeded, the voltage across the diac drops rapidly, permitting a current pulse to flow through the diac and into the gate of the triac to which it is connected. If ac is applied to the diac-triac combination, the triac will conduct on both halves of the cycle. Neon bulbs behave in a manner similar to the diac as trigger devices, but at considerably higher breakover voltages.

THE UNIJUNCTION TRANSISTOR (UJT)

This device, originally known as a double-based diode, has three leads—two bases and an emitter. A p-n junction is formed between the emitter and a slab of n-type semiconductor material. As can be seen in Fig. 15-5A,



(A) Schematic representation. (B) Ohmic equivalent circuit.

Fig. 15-5. UJT symbol and equivalent circuit.

one base is designated B1, and the other, B2. An interbase resistance, R_{BB}, of 5000 to 10,000 ohms can be measured between the two base terminals. This resistance can be divided into two individual resistors, R_{B1} and R_{B2}, at the emitter junction, as shown in Fig. 15-5B. The ratio of R_{B1} to the sum of the two resistors is assigned the symbol η, known as the intrinsic stand-off ratio. Hence, the voltage at the junction of the two resistors is ηV_{BB}. V_{BB} is the applied potential from B1 to B2.

If the voltage applied to the emitter, V_{EB1}, is less than ηV_{BB}, the emitter junction is reverse-biased and there is only a leakage current, I_{EO}. Should V_{EB1} be larger than ηV_{BB}, the junction is forward-biased and there will be current through the diode from the emitter to B1.

R_{B1} decreases as the current increases. This action is regenerative because as the current increases, R_{B1} decreases, allowing a further increase in current. As R_{B1} decreases, the voltage drop across R_{B1} must also decrease, by Ohm's law. Since the voltage drop decreases as the current increases, the UJT acts as a negative resistance. Much of the value of this device is based on this characteristic. A typical curve describing this, as well as other aspects of the UJT, is drawn in Fig. 15-6.

Curve 1 is that of an ordinary diode. This curve depicts the characteristic of the diode formed by the emitter and B1, assuming that B2 is open. Under these conditions, there is no current through base 2.

Assume now that V_{BB} is connected from B1 to B2, and observe curve 2 in Fig. 15-6. When the emitter is reverse biased, there is a slight leakage current, I_{EO}. This current seldom rises above 10 micro-amps, even at the highest temperatures.

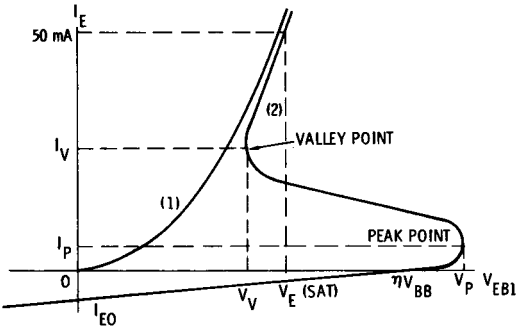


Fig. 15-6. Typical curve of UJT (2) and ordinary diode (1).

As the emitter voltage is increased about ½ volt (emitter-base junction voltage) beyond ηV_{BB}, the diode is forward-biased and the emitter starts to conduct. When the current is at I_P microamps, the emitter voltage is at its peak, V_P. The base-to-emitter voltage then drops as the current is increased (negative resistance) until a valley current, I_V, and a valley voltage, V_v, point is reached, at which the resistance of the UJT turns positive. Curve 2, the curve just described when there is current through B2, approaches diode curve 1. At the arbitrary values of emitter current of 50 mA (and $V_{BB} = 10$ volts), the emitter voltage is denoted as the saturation voltage.

V_P and η are relatively free from variation with temperature. If the variation is more than desired, a resistor in series with B2 will help the situation. V_P does depend linearly on V_{BB}, the voltage applied from B1 to B2. The peak current, I_P, decreases as V_{BB} and the temperature increase. As a whole, the unit is stable with temperature and voltage variations over a considerable period of time.

In many applications, the UJT is used as a sawtooth or pulse oscillator. The basic circuit is shown in Fig. 15-7. A sawtooth voltage appears at the emitter while a negative pulse is present at B2, and a positive pulse at B1. These pulses are formed when capacitor C_E discharges. R2, which ranges from 150 to 680 ohms, is primarily used for temperature compensation. It may be approximated by the equation:

$$R2 = \frac{0.5R_{BB}}{\eta V_{BG}} \qquad (15\text{-}1)$$

R1 depends on the size of the pulse required:

$$R1 < \frac{(R_{BB}(\min) + R_2)V_{out}}{V_{BG} - V_{out}} \qquad (15\text{-}2)$$

where,

$R_{BB}(\min)$ is the minimum interbase resistance specified by the manufacturer of the UJT,
V_{out} is the voltage of the pulse across R1,
$<$ means less than.

The pulse size will decrease as C_E decreases, and will depend to a large degree on the particular UJT used. The pulse size will be larger if a UJT with a low $V_E(\text{sat})$ is used.

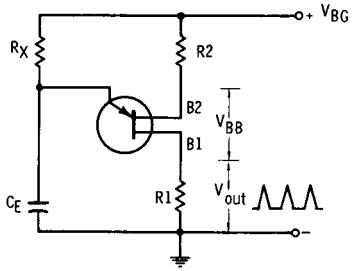


Fig. 15-7. Relaxation oscillator.

Initially, the capacitor is discharged, forcing the emitter to ground potential. As the emitter junction is reverse-biased, the UJT does not conduct. C_E is charged through R_X. When the emitter voltage is equal to the peak point voltage, the resistance of base 1, R_{B1}, drops. The capacitor is discharged through the emitter junction to about half of the saturation voltage, and the charging process is repeated. Oscillation is limited to frequencies below 1 MHz. The frequency of oscillation is about $1/R_XC_E$.

The emitter resistor, R_X, must intersect the curve in Fig. 15-6, in the negative resistance region of its characteristic. Hence, R_X must be somewhere between $(V_{BG} - V_P)/I_P$ and $(V_{BG} - V_V)/I_V$. On UJT specification sheets, you will find similarly numbered transistors that vary considerably in their V_P and I_P characteristics. It is best to use the maximum stated values for these parameters when determining R_X. If the load line crosses the characteristic curve at a point where the emitter current is less than I_P (cutoff region), the UJT will not trigger. If the load line crosses the curve at a point where the emitter current is more than I_V (saturation region), the UJT will probably not turn off. The emitter resistor should be kept to a minimum so that leakage current will have only a minor effect on the operation.

Devices having high valley current are useful as they allow a low value of emitter resistor to be used, negating the effects of leakage current and increasing the possible frequency of oscillation of the circuit. For low-

frequency oscillators, use a UJT specified to have a large I_P. Leakage current may become a considerable factor, however, if I_P is exceptionally large. It should be noted that the valley point current will increase as V_{BB} is raised, while the peak point current will decrease.

The UJT can be used to trigger an SCR by connecting the gate of the latter to the resistor in B1 of the former. In these applications, UJTs with large peak pulse voltage parameters are the most desirable.

The base-to-base voltage, V_{BB}, as well as the maximum emitter current and power dissipation are factors which must not be exceeded in any design.

THE FIELD EFFECT TRANSISTOR (FET)

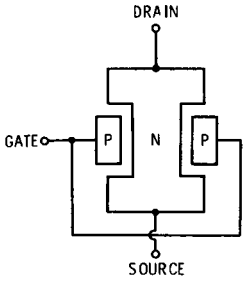
While the schematic presentation of the UJT and FET are very similar, the most obvious difference is that the UJT emitter junction is forward-biased while the FET input terminal (gate) is reverse-biased. Being similar to vacuum tubes in this respect, the characteristic curves of the FET are reminiscent of those in the pentode family.

There are two basic varieties of FETs. One type is referred to as the "Junction Field Effect Transistor," and will be abbreviated JFET. The other is the "Insulated Gate Field Effect Transistor," and the shorthand reference for this type is IGFET. The IGFET is identical with the MOS or MOST device, the latter initials being an abbreviation of "Metal Oxide Semiconductor Transistor." The primary differences between the JFET and IGFET lie in the input impedances and required bias voltages.

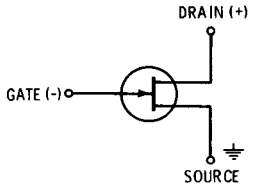
A drawing of the JFET and the schematic representations are shown in Fig. 15-8. The semiconductor slab connecting two JFET terminals, the source and drain, is known as the channel. The channel may be an n- or p-type material. The n-channel device and its schematic drawing are shown in Figs. 15-8A and 15-8B, respectively. Similarly, the p-channel device and representation are in Figs. 15-8C and 15-8D. A semiconductor material, opposite in type to the channel, is placed against the channel. This material, or transistor terminal, is called the gate. The voltages to be applied to the various terminals are usually as shown. All voltages are considered with respect to the source terminal, which in this drawing is at ground.

Although the n-channel JFET will be the center of the following discussion, all factors refer to the p-channel device as well, with only the voltage polarities reversed. Electron current flow for the n-channel device is from the terminal marked "source" to the terminal marked "drain."

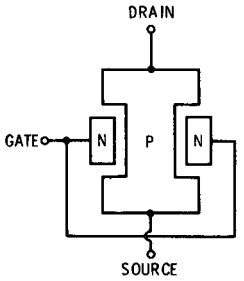
The amount of current between the source and drain is dependent on several factors. Up to a specific drain-to-source voltage, V_{DS}, the channel acts as a resistance. This resistance increases with an increase in temperature. The resistance of the p-channel device is about three times that of the n-channel transistor. The current is also a function of the size of the reverse voltage applied between the gate and source, V_{GS}. This can be clarified with the help of Fig. 15-9, which shows a typical set of JFET curves.



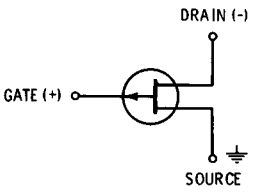
(A) N-channel JFET.



(B) Schematic symbol of n-channel JFET.



(C) P-channel JFET.



(D) Schematic symbol of p-channel FET.

Fig. 15-8. JFET and associated symbols.

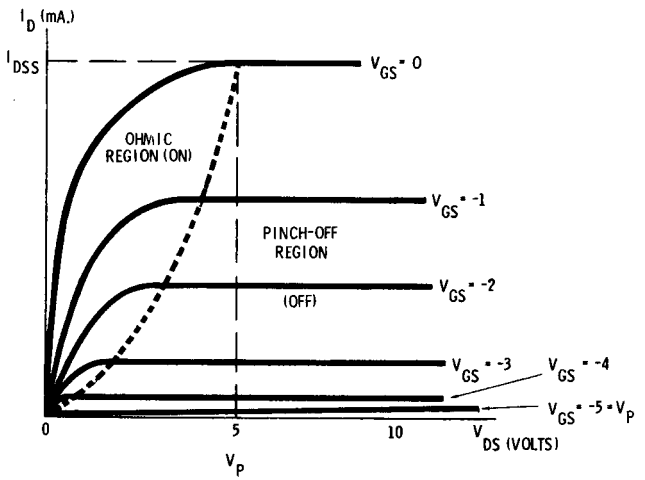


Fig. 15-9. Output (or drain) characteristics curves of JFET.

Following the curve $V_{GS} = 0$, the drain current, I_D rises relatively linearly to I_{DSS}. In this "ohmic region" (or *on* region), the current is dependent on the resistance of the channel material. This dependence ceases at V_P volts, the pinch-off voltage. The pinch-off voltage rises 2.2 millivolts for every degree Celsius rise in temperature. V_{DS} may be increased after V_P is reached, but the drain current remains relatively constant at I_{DSS}. I_{DSS} decreases as the temperature rises for JFETs and doubles for every 10°C rise in temperature for the IGFETs. In this "pinch-off region" (or *off* region), the output impedance of the transistor is very high.

As the gate is made more negative with respect to the drain, there is less current through the channel. Finally, a V_{GS} is reached where the current ceases. This is the pinch-off voltage. It is identical in value to the pinch-off voltage previously defined. Hence, the pinch-off voltage may be determined by finding the value of V_{GS} that halts the drain current, or it is the value of V_{DS} at which the drain current reaches saturation when V_{GS} is 0. The saturation current in the latter case is I_{DSS}.

The drain current is related to the pinch-off voltage, V_P, the current in the pinch-off region when the gate-to-source voltage is zero, I_{DSS}, and the gate-to-source voltage, V_{GS}. This relationship is defined by the equation:

$$I_D = I_{DSS}\left(1 - \left|\frac{V_{GS}}{V_P}\right|\right)^2 \qquad (15\text{-}3)$$

where,

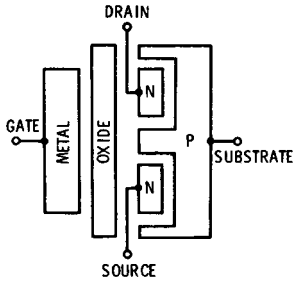
$|V_{GS}|$ is the absolute value of V_{GS},
$|V_P|$ is the absolute value of V_P.

IGFET

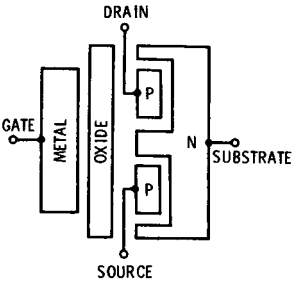
The IGFET is made in two basic arrangements, each not radically different from the JFET just discussed. Each arrangement may use an n-channel or a p-channel semiconductor. Hence, four types of IGFETs are common. All types are illustrated in Fig. 15-10. Once again, only the n-channel will be considered; p-channel transistors use similar mechanisms, but the terminal voltages must be reversed.

In Fig. 15-10A, the substrate (foundation) is a highly resistive p-slab. Two n-slabs are diffused (joined) into the p-material. An oxide insulator covers this combination. A metal gate placed over the insulator, in conjunction with the p-substrate, forms a capacitor. A positive voltage on the gate causes negative charges to be induced into the p-substrate. These charges allow conduction between the source and drain n-slabs. The greater the charge (or the more positive the voltage placed on the gate with respect to the source) the lower the resistance between the source and drain. Drain current is increased or enhanced by an increase in gate potential. Hence, the name enhancement-type transistor.

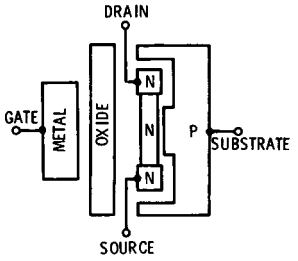
Depletion-type IGFETs behave very much like the JFETs. The drawings of these are shown in Figs. 15-10C and 15-10D with the schematic repre-



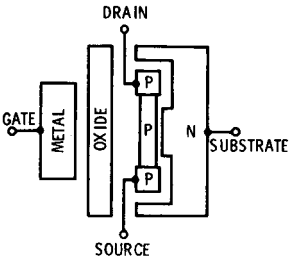
(A) N-channel (enhancement-type).



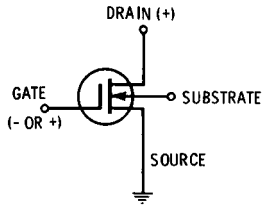
(B) P-channel (enhancement-type).



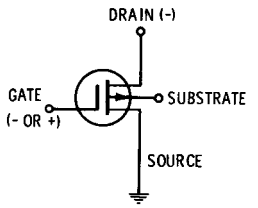
(C) N-channel (depletion-type).



(D) P-channel (depletion-type).



(E) Schematic symbol of n-channel IGFET.



(F) Schematic symbol of p-channel IGFET.

Fig. 15-10. Enhancement and depletion types of IGFETs.

sentation in Figs. 15-10E and 15-10F. Once again, only the n-channel device will be considered, with only polarity reversals being required to describe the p-channel transistor.

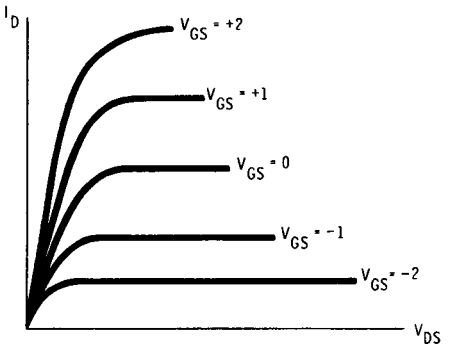
The depletion-type device is similar in structure to the enhancement-type IGFET, with the addition of a medium resistance n-channel connecting the source and drain. There is current between the source and drain even with low values of V_{DS} voltages. Negative gate voltages will cause the current to decrease. This device is most accurately described as both a depletion and enhancement type of IGFET.

The three FET devices are classified by type. Type A is a depletion-type transistor only, and is represented by the JFET. Type-B devices, such as the last one discussed, exhibit both depletion and enhancement char-

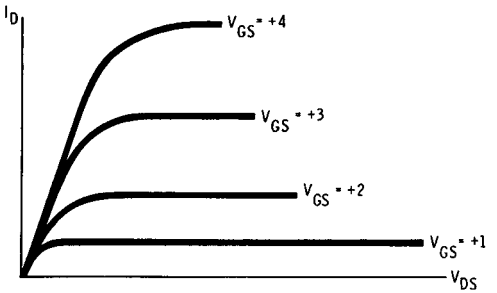
acteristics. Approximate curves are shown in Fig. 15-11A. Type-C devices are strictly enhancement-type. Figure 15-11B shows theoretical drain characteristic curves for this type of device.

Biasing the FET

One of the major differences in designing for the various type of FETs (n-channel devices are considered here—for p-channel devices, reverse the polarities) is the choice of bias voltage (negative, positive, or zero volts)



(A) Depletion and enhancement (type B).



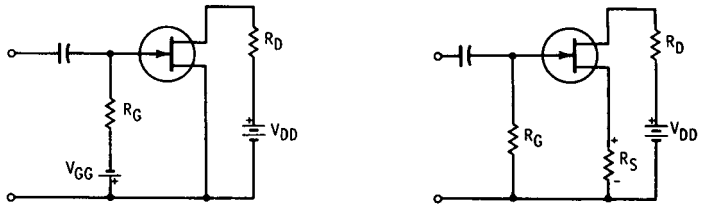
(B) Enhancement (type C).

Fig. 15-11. Depletion and enhancement curves.

to be applied to the gate with respect to the source. Positive or zero types of bias may be used on enhancement types of IGFETs. The IGFET never draws gate current regardless of the polarity of the bias voltage. The JFET does draw current when the n-channel device gate bias runs more than 0.5 volt positive. Negative bias is usually employed when using depletion-type transistors.

Two methods of achieving negative bias are shown in Fig. 15-12. In Fig. 15-12A, the gate is made negative by virtue of the bias supply voltage V_{GG}. The voltage from the gate to the source is equal to V_{GG} minus

$R_G I_{GSS}$, where I_{GSS} is the leakage current of the reverse-bias junction. I_{GSS} is similar to the I_{CBO} characteristic of the injection-type transistor. It is current from the gate to the channel when the source is shorted to the drain. In the JFET, it doubles for every 10°C rise in temperature. The broken line curve in Fig. 4-2 can be used to determine I_{GSS} at elevated temperatures when the leakage current at 25°C is known. As for the IGFET, the I_{GSS} leakage current is unaffected by temperature and is much lower than the leakage current of the JFET. Germanium FETs have higher leakage than do silicon devices. However, germanium transistors can operate down to −200°C, while the lower limit for silicon units is −50°C.



(A) Biasing with R_G and V_{GG}. (B) Biasing with R_G and R_S.

Fig. 15-12. Methods of biasing.

In Fig. 15-12B, a voltage developed across R_S is equal to that resistor multiplied by I_S, the quiescent source current. Since the source and drain currents are equal, this voltage is $I_D R_S$. The top or source end of the resistor, R_S, is positive with respect to ground. The gate is connected to ground through R_G. Hence, the source end of the resistor, or source, is positive with respect to the gate. This is the proper polarity for putting a negative bias on the FET. If the voltage due to leakage, $R_G I_{GSS}$ is negligible, the bias voltage from gate to source is equal to the voltage across R_S. In extreme cases, the voltage due to the leakage current can be subtracted from that across R_S.

Since feedback is developed across R_S for any ac signal input voltage, it will reduce the overall gain of the stage. This effect can be overcome by shunting R_S with a large capacitor. The impedance of the capacitor at the lowest frequency to be amplified should be equal to about one-tenth of the size of the resistor.

The latter method of bias is more desirable due to better dc stability, when compared to the former circuit. Stability can be improved by making R_S very large. A circuit to accomplish this is shown in Fig. 15-13. Here, the voltage from the gate to the source is:

$$V_{GS} = I_D R_S - V_{GG} - I_{GSS} R_G \qquad (15\text{-}4)$$

If $I_D R_S$ and V_{GG} are increased by equal amounts, V_{GS} will remain constant because the two voltages buck each other. However, the stability due to a large R_S will be improved.

Each transistor parameter is specified to be within a specific range rather than one absolute value. This cannot be ignored when biasing the device. The tolerable variation in drain current and gate-to-source voltage must be determined from the design and transistor data. If ΔI_D is the variation of drain current and ΔV_{GS} is the variation of gate to source voltage, Equation 15-4 shows that:

$$\Delta V_{GS} = \Delta I_D R_S - \Delta I_{GSS} R_G \qquad (15\text{-}5)$$

where ΔI_{GSS} is the change in gate current over the temperature range. Note that the V_{GG} term falls out from Equation 15-4. It is not a factor in Equation 15-5 since V_{GG} remains constant and thus does not affect the gate-to-source voltage change.

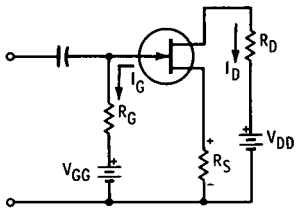


Fig. 15-13. Scheme to increase R_S.

As an example using the circuit in Fig. 15-13, assume that a transistor such as the 2N4222 can be biased at $V_{GS} = -2$ volts with a drain current of 4 mA. The gate leakage current, I_{GSS} is specified at 10^{-10} amps. The device is to be used up to temperatures of 150°C, at which the gate leakage current is specified as 10^{-7} amps. Hence, ΔI_{GSS} is $10^{-7} - 10^{-10} \approx 10^{-7}$ amps. Assume that the drain current in this design may vary by as much as 2 mA, so that $\Delta I_D = 2 \times 10^{-3}$ amps. We may also allow about 1 volt change in gate-to-source voltage, or $\Delta V_{GS} = 1$ volt. Inserting these numbers into Equation 15-5 yields:

$$1 = (2 \times 10^{-3})\, R_S - 10^{-7} R_G$$

Should R_S be chosen at 1000 ohms so that the $I_D R_S$ product does not vary by more than 2 volts, then R_G can be determined as follows:

$$1 = (2 \times 10^{-3})\, 1000 - 10^{-7}(R_G)$$

$$R_G = 10^7 \text{ ohms.}$$

Using Equation 15-4:

$$2 = (4 \times 10^{-3})\, 1000 - V_{GG} - 10^{-7}(10^7)$$

$$V_{GG} = 1 \text{ volt.}$$

A practical circuit assuming that V_{DD} equals 20 volts is shown in Fig. 15-14. The 1000-ohm resistor just determined can be used as R_S. The resistors in the bias circuit are determined here by solving two simultaneous

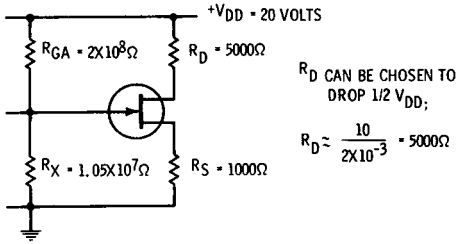


Fig. 15-14. Practical FET circuit.

equations. One equation, determined by using voltage divider methods to get the 1 volt at the gate (the V_{GS} just determined) is:

$$V_{GS} = 1 = \left(\frac{R_X}{R_{GA} + R_X}\right) V_{DD} \qquad (15\text{-}6)$$

The second equation considers the parallel combination of R_{GA} and R_X, which must be equal to $R_G = 10^7$ ohms, as just determined. Hence:

$$R_G = \frac{R_{GA}R_X}{R_{GA} + R_X} = 10^7 \qquad (15\text{-}7)$$

The circuit components will be determined by solving these two equations. The solutions are noted as Equations 15-8:

$$R_{GA} = \frac{R_G V_{DD}}{V_{GS}} = 2 \times 10^8 \text{ ohms} \qquad (15\text{-}8A)$$

$$R_X = \frac{R_G V_{DD}}{V_{DD} - V_{GS}} = 1.05 \times 10^7 \text{ ohms} \qquad (15\text{-}8B)$$

Amplifiers

The major differences in using a JFET or IGFET are the bias voltages and polarities. In the equations used to calculate the amplifier gain and the various impedances, both types of transistors are treated identically.

In the discussion of the bipolar transistor, beta was the most significant relationship. The gain provided by the FET is based on transconductance or mutual conductance, g_m (specified at a specific drain current), which relates the change in drain current, ΔI_D, to the change in gate to source voltage, ΔV_{GS}. The various symbols used to represent transconductance, as well as a relationship to other factors, are shown in Equation 15-9:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = g_{fs} = y_{fs} = \frac{2I_{DSS}}{V_P}\left(1 - \left|\frac{V_{GS}}{V_P}\right|\right) =$$

$$g_{mo}\left(1 - \left|\frac{V_{GS}}{V_P}\right|\right) = \frac{1}{r_{ds}}\left(1 - \left|\frac{V_{GS}}{V_P}\right|\right) = g_{mo}\left(\frac{I_D}{I_{DSS}}\right)^{1/2} \qquad (15\text{-}9)^*$$

where,

ΔV_{GS} is the change in gate to source voltage,
I_Di s the quiescent drain current,
ΔI_D is the change in drain current due to ΔV_{GS},
I_{DSS} is the drain current in the pinch-off (or off) region when $V_{GS} = 0$,
V_P is the pinch-off voltage,
$|V_{GS}|$ is the absolute value of the gate-to-source voltage ignoring the + or − signs,
$|V_P|$ is the absolute value of the pinch-off voltage ignoring the + or − signs,
g_{mo} is g_m when $V_{GS} = 0$ on the $I_D = I_{DSS}$ curve ($g_{mo} = 2I_{DSS}/|V_P|$),
r_{ds} is the resistance of the channel (from source to drain) when the transistor is operated in the ohmic (or *on*) region,
y_{fs} is the transadmittance and is equal to g_m at low frequencies. Use g_m at high frequencies as y_{fs} includes the capacities of the FET and will consequently be misleadingly high.

It should be noted that g_m and I_{DSS} drop 0.5% for every 1°C rise in temperature.

While g_m was defined as an ac transconductance, there is likewise a dc g_m or g_{FS}. It is the ratio of the drain current to the gate-to-source voltage at a particular point on the output curve. It differs from point to point on the curve.

With g_m fully defined, we can now proceed with a drawing of a practical small-signal equivalent circuit of the FET, shown in Fig. 15-15. The solid lines depict the JFET. The IGFET equivalent circuit is identical to the one

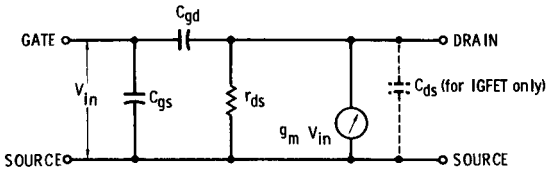


Fig. 15-15. Equivalent circuit of an FET.

shown, with the addition of a capacitor, C_{ds}, at the output. It is drawn in broken lines in the figure. C_{gs} and C_{gd} (C_{rss}) are the gate-to-source and gate-to-drain capacities, respectively. The sum of C_{gs} and C_{gd} is C_{iss}, the common source input capacities with the output shorted. While the output impedance of the JFET is resistive, that of the IGFET is primarily capacitive. It is equal to $1/g_{os} = 1/y_{os}$, the reciprocal of the output admittance. The output resistance from source to drain at the point of operation of the transistor is r_{ds}. When the transistor is operated in the *on* region, r_{ds} increases with temperature. The notation for the drain to source resistance is $r_{ds(ON)}$ when the transistor is fully on, and V_{GS} and V_{DS} are both zero.

The FET is usually used in any one of the circuit arrangements shown in Fig. 15-16.

In the common-source arrangement, the input and output impedances are high. The voltage gain is:

$$A_{VS} = g_m \left(\frac{R_D r_{ds}}{R_D + r_{ds}} \right) \qquad (15\text{-}10)$$

where,

r_{ds} is the output resistance from the source to the drain of the FET. The quantity in the parenthesis is the drain resistor in parallel with r_{ds}. It may be written as $R_D || r_{ds}$. The output load may consist only of the R_D shown in the various drawings. It may also consist of R_D in parallel with any direct or capacitance-coupled load placed across R_D. Assign R_L to represent this external load. The parenthesis in Equation 15-11 should be modified so that it will include R_L. The quantity in the parenthesis will become $R_D || r_{ds} || R_L$. A similar adjustment should be made to all equations below.

If R_S is not bypassed by C_S, the gain equation becomes:

$$A_{VS} = \frac{g_m (R_D || r_{ds})}{1 + g_m R_S} \qquad (15\text{-}11)$$

and the output resistance seen by any load at V_{out} is R_D in parallel with R_{out}, where:

$$R_{out} = r_{ds} + (1 + g_m r_{ds}) R_S \qquad (15\text{-}12)$$

R_{out} is usually negligible when compared to R_D.

The input resistance is essentially equal to R_G. The input capacity is:

$$C_{in} = C_{gs} + C_{gd}(1 + g_m R_D) \qquad (15\text{-}13)$$

The upper portion of the frequency response is basically controlled by C_{ds} and C_{gd}. If the generator feeding the amplifier is a voltage source, the resistance of the generator does not affect the frequency response. The gain is reduced 3 dB from that calculated with Equation 15-11, at:

$$f_o = \frac{1}{2\pi R_D (C_{ds} + C_{gd})} \qquad (15\text{-}14)$$

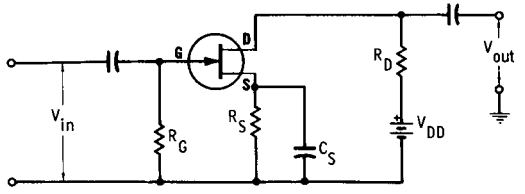
The rolloff curve follows that shown in Fig. 8-2C.

If the resistance of the generator is comparable to the input resistance of the amplifier, the gain is 3 dB below that predicted in Equation 15-11 at:

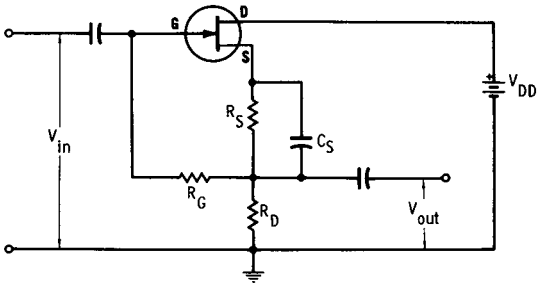
$$f_o = \frac{1}{2\pi R_{GA} [C_{gs} + C_{gd}(1 + g_m R_D)]} \qquad (15\text{-}15)$$

where R_{GA} is the resistance of the generator.

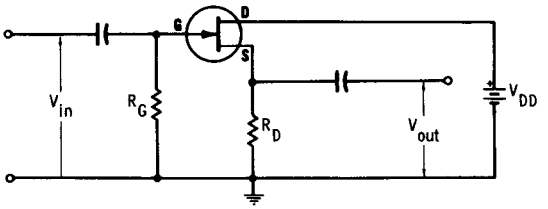
As an example, assume that in Fig. 15-16A, $R_G = 1$ megohm, R_S (not by-passed) is 620 ohms, and $R_D = 10{,}000$ ohms. The supply is 20 volts.



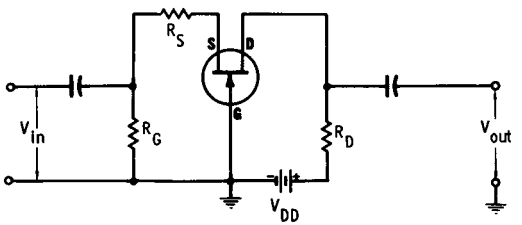
(A) Common source.



(B) Common drain.



(C) Common drain simple circuit.



(D) Common gate.

Fig. 15-16. FET circuit configurations.

A voltage source feeds this circuit so that $R_{GA} = 0$. In the transistor to be used, $V_P = 2$ volts, $I_{DSS} = 1$ mA, $r_{ds} = 10^5$ ohms, $C_{gs} = 5$ pF, $C_{gd} = 1.5$ pF and $C_{ds} = 0$. Calculate the drain current, voltage gain, input capacitance, output resistance seen by the load, and the frequency at which the gain dropped 3 dB.

According to Equation 15-3, the drain current is:

$$I_D = 10^{-3}\left(1 - \frac{|V_{GS}|}{|2|}\right)^2$$

Since there are two unknowns, a second equation relating I_D and V_{GS} is necessary. This can be derived from bias considerations, where:

$$V_{GS} = I_D R_S = 620 I_D$$

Solving the two equations, $I_D = 0.64$ mA and $V_{GS} = 0.4$ volt.

In order to determine the voltage gain, g_m should be calculated from Equation 15-9:

$$g_m = \frac{2I_{DSS}}{V_P}\left(1 - \frac{|V_{GS}|}{|V_P|}\right) = \frac{2 \times 10^{-3}}{2}\left(1 - \frac{0.4}{2}\right) = 8 \times 10^{-4}$$

The voltage gain, from Equation 15-11, is found to be:

$$A_V = \frac{8 \times 10^{-4}(10^4 || 10^5)}{1 + (8 \times 10^{-4})620} = 4.9$$

It is interesting to note that if R_S had been bypassed by a large capacitor, the voltage gain, using Equation 15-10, would have been $8 \times 10^{-4}(10^4 || 10^5) = 72.8$.

The input capacitor, according to Equation 15-13, is:

$$C_{in} = 5 \times 10^{-12} + 1.5 \times 10^{-12}\,[1 + 8 \times 10^{-4}(10^4)] = 18.5 \text{ pF}$$

and the resistance looking back from the load, R_D, to the transistors is, by Equation 15-12:

$$R_{out} = 10^5 + [1 + (8 \times 10^{-4})\,10^5]\,620 = 150{,}220 \text{ ohms}$$

while the frequency where the gain is reduced by 3 dB is, from Equation 15-14:

$$f_o = \frac{1}{2\pi(10^4)(15 \times 10^{-12})} = 10.6 \text{ MHz}$$

As for the common-drain (source follower) circuit in Figs. 15-16B and 15-16C, the gain is:

$$A_{VD} = \frac{g_m R_D}{1 + g_m R_D} = \frac{A_{VS}}{1 + A_{VS}} \approx 1 \qquad (15\text{-}16)^*$$

since $g_m R_D$ is the gain of the common-source circuit without feedback.

The input resistance of the circuit in Fig. 15-16C is simply the resistor in the gate, or R_G. For the circuit in Fig. 15-16B, it is:

$$R_{in} = \frac{R_G}{1 - A_{VD}} \tag{15-17}$$

Evidently, the input resistance for this circuit is a direct function of the gain. However, the input capacitance is lower for the common drain circuit than it is for the common source arrangement. It is:

$$C_{in} = C_{gd} + (1 - A_{VD})C_{gs} \tag{15-18}$$

As for the output, the resistance is approximately equal to:

$$R_{out} = \frac{R_D}{1 + g_m R_D} \approx \frac{1}{g_m} \tag{15-19}*$$

In all cases, R_D in the equation should be appropriately modified if there is an output load R_L across R_D.

As for the common gate circuit in Fig. 15-16D, the gain can be conveniently approximated from the equation:

$$A_{VG} = \frac{g_m R_D}{1 + g_m R_S} \tag{15-20}$$

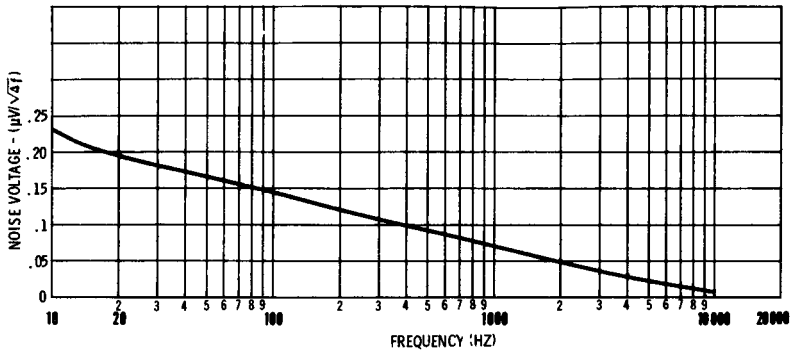
While the output resistance is about equal to R_D, the input resistance approaches:

$$R_{in} = \frac{g_m R_S + 1}{g_m} \tag{15-21}$$

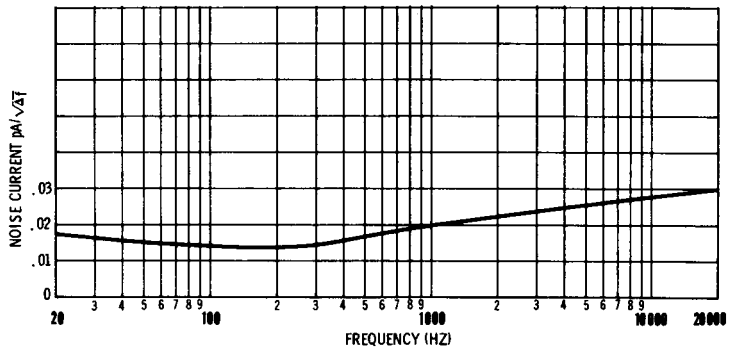
Noise

At the current state of the art, the JFET is superior to the IGFET in its noise characteristic. Manufacturers frequently supply curves for both types of field-effect transistors, showing how the noise figure (see definition in Equations 5-35 and 5-36) varies with the frequency being reproduced and the resistor at the input V_{DS} and I_D. A more informative set of curves shown in Fig. 15-17 relate $\bar{v}_n/\sqrt{\Delta f}$ and $\bar{i}_n/\sqrt{\Delta f}$ to the center frequency of the reproduced band. (See Fig. 5-18 and the discussion in Chapter 5 to review the signficance of $\bar{v}_n$ and $\bar{i}_n$, the hypothetical noise voltage and current generators at the input of a hypothetical noiseless amplifier.)

The $\sqrt{\Delta f}$ in the denominator at the ordinate axis is the noise bandwidth of the amplifier. It is sometimes written $\sqrt{\sim}$ or $\sqrt{\text{Hz}}$. The curve in Fig. 15-17A, for example, shows the noise voltage with a 1-Hz bandwidth. If the bandwidth is increased to, let us say 3, $\sqrt{\Delta f} = \sqrt{3}$. The equivalent noise voltage for this bandwidth is the $\bar{v}_n/\sqrt{\Delta f}$ read from the curve, multiplied by $\sqrt{3}$.



(A) Hypothetical noise voltage versus frequency.



(B) Hypothetical noise current versus frequency.

Fig. 15-17. Curves showing voltage and current versus frequency.

Some curves are drawn for bandwidths differing from 1 Hz. In this case, the noise reading from the curve should first be divided by the square root of the bandwidth used for the curve, and then multiply the result by the square root of actual bandwidth involved, as above.

Considering that all noise is reproduced over a specific bandwidth, it may not be self-evident as to which frequency to use to read $\bar{v}_n/\sqrt{\Delta f}$ from the curve. As f_H and f_L (see definition referenced to Equation 5-37) are known factors, the significant frequency on the curve in Fig. 15-17A is $f_o = \sqrt{f_H f_L}$.

All the above also applies to the current noise generator, $\bar{i}_n$, and to the curve in Fig. 15-18B.

From Equation 5-40, it can be shown that the total noise voltage, $\bar{v}_{nit}$, referred to the input of the transistor is:

$$\bar{v}_{nit} = (\bar{v}_{na}^2 + \bar{v}_{nia}^2 + v_{ni}^2)^{1/2} \qquad (15\text{-}22)$$

Each factor in the equation is a source of noise.

$\bar{v}_{na}$ is the noise voltage due to the equivalent noise voltage generator at the input of the noiseless transistor. Should the input impedance of the transistor be primarily resistive as in Fig. 15-16A, $\bar{v}_{na}$ is simply $\bar{v}_n$ as read from the curve in Fig. 15-17A. At frequencies where the input capacity of the transistor is the dominating factor of the input impedance, $\bar{v}_{na}$ is more complex and equal to:

$$\bar{v}_{na} = \frac{\bar{v}_n C_s}{C_{in} + C_s} \tag{15-23}$$

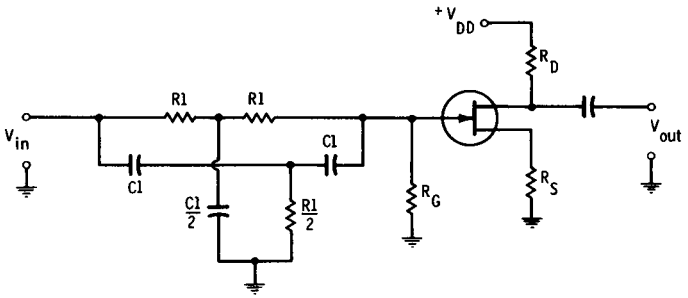
where,

C_{in} is the input capacity of the FET, equal to $C_{gs} + C_{gd}(A_{vs} + 1)$ from Equation 15-13,

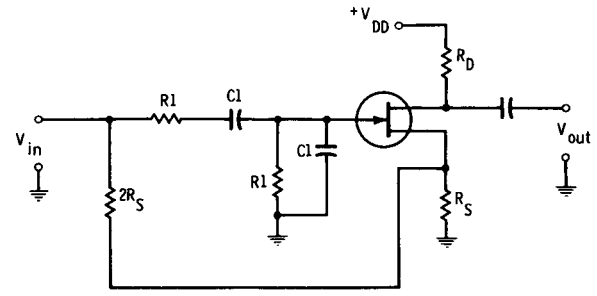
C_s is the capacity of a transducer at the input to the amplifier.

In a similar manner, $\bar{v}_{nia}$ is the noise voltage due to the equivalent noise current generated at the input of the noiseless FET. It is $\bar{i}_n R_G$ when R_G is the gate to source resistor in Fig. 15-16A. Should the capacity dominate the input here,

$$\bar{v}_{nia} = \frac{\bar{i}_n}{6.28 f_o (C_s + C_{in})^2} \tag{15-24}$$



(A) Twin-T filter.



(B) Wien-bridge filter.

Fig. 15-18. Notch or band-rejection filters.

The thermal noise generator voltage, v_{ni}, can be determined from Equations 5-38 or 5-39, depending upon whether the capacitance or resistance dominates the input circuit. C_t in Equation 5-39 is $C_s + C_{in}$.

In all the foregoing considerations, disregard R_G in the input impedance of C_t is less than 1/10 of R_G. Should R_G be 1/10 or less than the impedance of C_t, disregard the relationships involving the capacitance. Should both be equal or approach each other, calculate the various noise voltages both ways and use a value somewhere between the two calculations in each determination. The noise voltage chosen would depend upon which factor was more important at the input—the input resistor or the input capacitive impedance.

All factors are substituted into Equation 15-22 to determine the noise voltage at the input. Then compare it to the signal voltage at the input. Once again, if the load the signal sees is primarily a resistor, the input voltage at the amplifier, v_{sa}, is simply $R_G v_s/(R_{GA} + R_G)$ where, R_{GA} is the resistance of the voltage generator, R_G is the resistor at the input to the amplifier, and v_s is the open circuit terminal voltage of the generator. Should capacitive factors dominate:

$$v_{sa} = \frac{v_s C_s}{C_{in} + C_s} \tag{15-25}$$

As a rule of thumb, the noise due to the input resistor is at a minimum when it is equal to $\bar{v}_n/\bar{i}_n$, although the resistor is seldom a major factor in producing noise in an FET circuit. Noise will usually be minimized when the transconductance of the device and the resistor at the input are large, and the FET is biased at about $V_{GS} = 0$ along the I_{DSS} curve.

Filters

The earlier portion of Chapter 8 was devoted to passive RC and RL filters that are to be placed in transistor circuits. Unfortunately, bipolar transistors will load the circuits, changing the f_o frequency and possibly also changing the entire rolloff characteristic. The high input impedance of the FET is the ideal load on these filters. The characteristics are pretty much those obtained from the various calculations.

The twin-T and Wien bridge notch and band rejection filters have sharp response curves similar to those in Fig. 8-11. These filters are ideally suited to feed the high impedance at the input of the FET. Circuits are drawn in Fig. 15-18. The equation for f_o, the frequency with the greatest attentuation in both circuits, is $f_o = 1/6.28R1C1$. In Fig. 15-18B, R_S should be small. This order of magnitude dictates that the input is best driven by a low impedance such as an emitter follower.

The FET is also ideal for use in active filter circuit arrangements. A possible high-pass filter circuit is shown in Fig. 15-19. In this circuit, a low-pass network consisting of R1-C1, is inserted in the feedback circuit between the output and the differential amplifier consisting of Q1 and Q2.

Similar arrangements can be drawn for the low-pass, bandpass and band-rejection type filters.

Oscillators

FET oscillators have the major advantage over their bipolar counterparts, in that the stability of the former is far superior. The internal capacitances in the FET tend to compensate for other factors which may cause the frequency to drift with temperature.

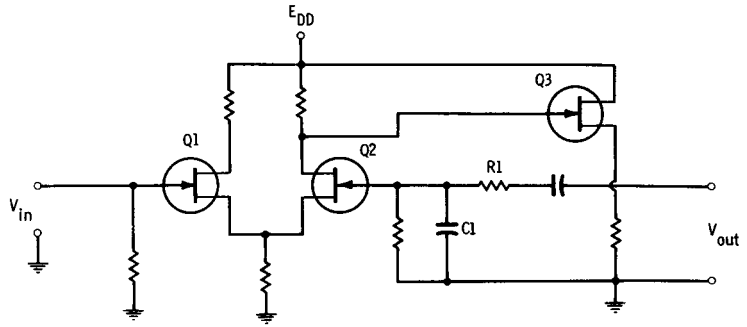


Fig. 15-19. Active high-pass filter.

The circuits are basically those shown in Fig. 10-13, with the substitution of the equivalent elements of the FET for those of the bipolar transistor. Biasing is the major concern in the proper design of an oscillator. Two arrangements are prevalent in current designs.

In one circuit, a resistor shunted by a capacitor is put in series with the gate. In general, the resistor is specified at about 1 megohm while the capacitive reactance is about 10 or 20 ohms at the oscillator frequency.

The second arrangement involves a parallel RC network in the source lead of the transistor. The drain current is properly stabilized because of the feedback. The size of the resistor depends on the class of operation required for the oscillator. For example, should it be desired that the transistor operate class-A, the bias should be set at half the saturation current. The shunting capacitor should fully bypass all signal in the source circuit, with the reactance being in the order of magnitude of 0.01 to 0.5 ohm.

The transistor used must be capable of providing sufficient gain at the frequency involved so that the circuit will start oscillating and be maintained in this state.

Variable Resistance

In the ohmic region of Fig. 15-9, it is obvious that at low drain-to-source voltage, the drain circuit of the transistor is a linear resistor. Each curve starts as a straight line from the apex of the axis. The resistance is the

reciprocal of the slope of each line, and may be roughly approximated from the equation

$$r_d = r_{ds(ON)} \left(\frac{V_P}{V_P - V_{GS}} \right) \tag{15-26}$$

where,

$r_{ds(ON)}$ is the resistance in the ohmic region when $V_{GS} = 0$.

The resistance is dependent upon the gate to source voltage. Only this voltage need be changed to vary a resistive component in the circuit. Thus the FET can be used as a voltage dependent variable resistor.

Switches

One of the major drawbacks in using the bipolar transistor as a switch is that the swing from the *on* to the *off* state is not accompanied at the output by a very large swing from a low to a high impedance. The output impedance variation from the *on* to the *off* state is considerably greater for the FET than it is for the bipolar device. It should be noted that the various capacities around the device do affect the switching speed.

Precautions

Several factors must be considered when designing with FETs.

BV_{GSS} is the reverse breakdown voltage between the gate and the channel when the source is shorted to the drain. Zener diodes are frequently placed from the gate to the substrate to limit the voltages to safe values. However, this reduces the input impedance to about 10^{10} ohms from about 10^{14} ohms.

Similar to BV_{GSS}, BV_{DSS} is the reverse breakdown voltage between the drain and substrate in IGFETs when the gate is shorted to the source.

In handling IGFETs, a static charge may be formed between the gate and the channel. The leads should be shorted together until after they have been soldered into the circuit.

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