Electronic Design 18

VOL. 24 NO. 18

FOR ENGINEERS AND ENGINEERING MANAGERS

SEPT. 1, 1976

Deciding between PLAs and µPs can cause serious headaches. Designers must consider product development time and total cost, software requirements, services of programmers, second sourcing, future design changes, speed of handling I/O control functions, physical size, and power needs. To help you decide, see p. 24.

Electronic Design® 18

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NEWS

TECHNOLOGY

PRODUCTS

DEPARTMENTS

Cover: Designed by Art Director Bill Kelly.

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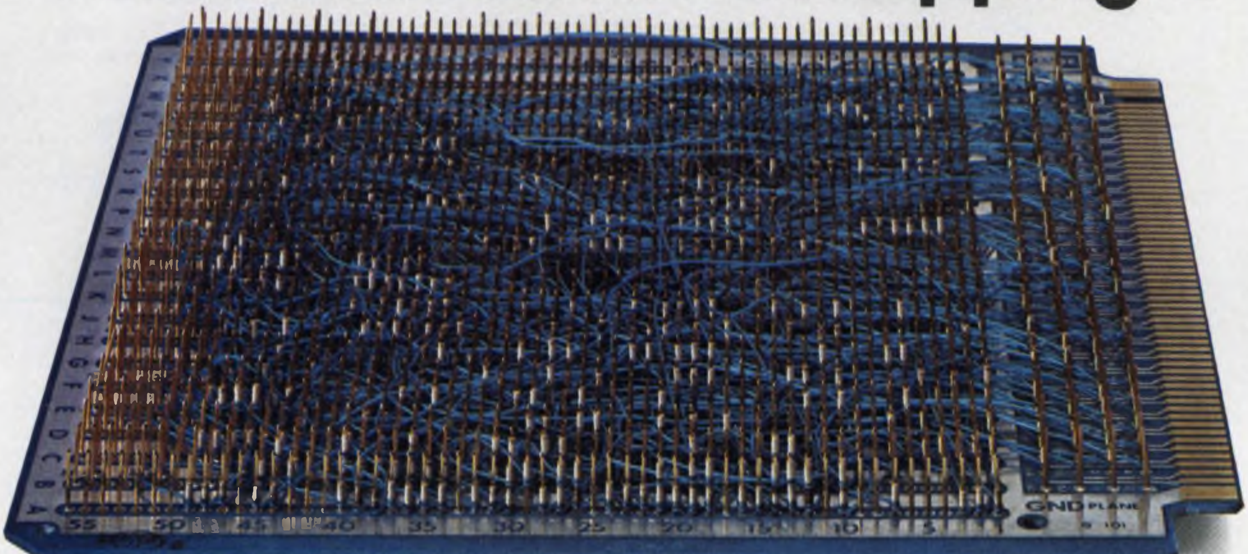
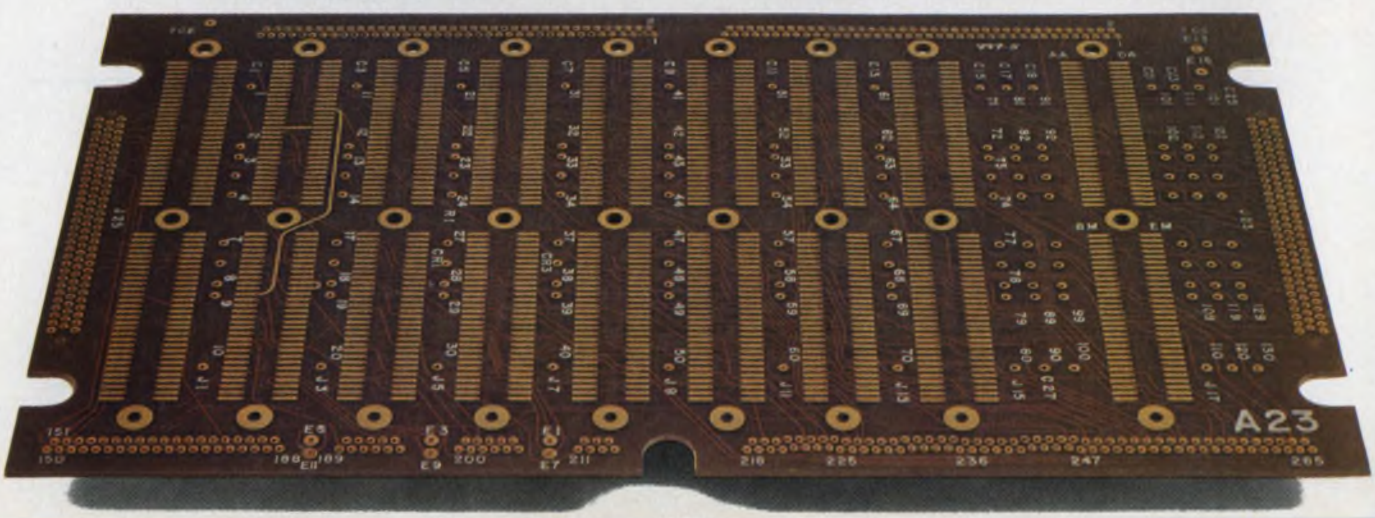
Compare Multiwire:™

costs less than wirewrapping...

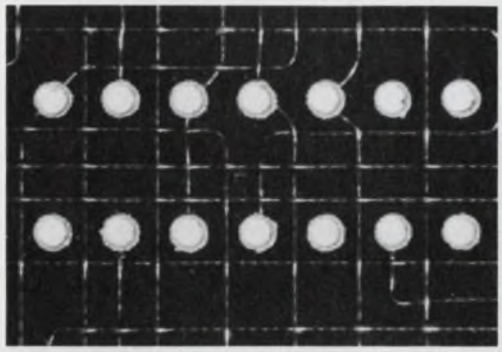


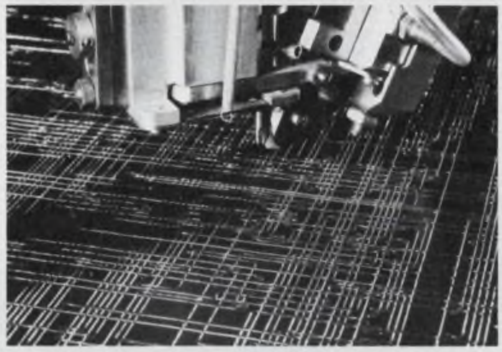
works better than multilayering.



Two major systems—wirewrapping and multilayering—have been used for complex electronic interconnection in the last 15 years. Despite improvements and refinements, each still has inherent disadvantages. That's why Multiwire was created by Photocircuits. It overcomes the disadvantages of wirewrapping and multilayering.

A Multiwire board is basically a customized pattern of insulated wires laid down on an adhesive-coated substrate by a machine operating under numerical control.





Multiwire vs. wirewrapping.

Today, interconnection costs are more important than ever. So take a long, hard look at a key advantage of Multiwire panels. They cost much less than wirewrapping in small or production quantities.

Here's an example of how much less: a Multiwire replacement of a 60 DIP wrapped-wire panel. Total tooling costs were just $750. In order quantities of 1000 pieces, the Multiwire boards at $45 each were more than $30 less than the wrapped-wire panel. (A 40% cost savings.) Multiwire prices also include a 100% continuity check.

But cost is not the only reason for the superiority of Multiwire over wirewrapping. There are also design advantages. For example, Multiwire offers two-dimensional packaging density equal to wirewrapping. But with Multiwire panels, you reduce board-to-board spacing. And Multiwire weighs much less too. So it can contribute substantially toward improving the envelope or three-dimensional package of your product.

Electrically, Multiwire is also superior. The extreme repeatability of the manufacturing process provides much higher electrical reliability as received—this is an important cost-saving factor. In addition, you get the controlled impedance characteristics required without variations.

Multiwire vs. multilayering

With Multiwire, reliability goes up and inspection cost goes down. Multiwire doesn't need extensive inspection—like multilayering does—for nicks, pinholes, hairline cracks, spacing violations and bridging. Yet Multiwire regularly yields better than 99% reliability at incoming inspection.

Compared to multilayering, designing a new Multiwire board is a far simpler operation. Component locations and a wiring list are all we need. Our computer-aided system does the rest.

Since the computer also takes care of deletions and/or additions, engineering changes are simplified. What's more, Multiwire makes it easier to find paths for interconnections, because the insulated wires can cross one another. For these reasons we can deliver finished Multiwire boards to your door in weeks rather than months.

The advantages of Multiwire over wirewrapping and multilayering vary from case to case. We'd like to help you evaluate possible time, cost, design and reliability benefits. For information and price estimates, call the Multiwire Marketing Department at 516-448-1111.

	Wrapped panels	Multi-layers	Multi-wire
Design & tooling cost	Low	Very High	Low
Design & tooling time	Short	Very Long	Short
1st piece delivery	Short to Very Short	Long	Short
Board cost in small quantities	High	High	Medium
Board cost in production quantities	High	Medium	Medium
2 dimensional packaging density	High	High	High
3 dimensional packaging density	Medium	High	High
Weight	High	Low	Low
Ease of changes	Excellent	Poor	Good
High speed electrical characteristics	Fair to Poor	Excellent	Excellent
Interchangeability with other techniques	Fair	Excellent	Excellent
Repairability	Excellent	Poor	Good
Controlled impedance	Poor	Good	Good
Electrical reliability as received	Fair	Good	Excellent

Multiwire from Photocircuits

Division of Kollmorgen Corporation, Glen Cove, New York 11542

CIRCLE NUMBER 4

Across the Desk

Bicentennial issue feeds the inner man

May I add my quiet squeak to the roar of compliments you and your editorial staff must be enjoying these days for your contribution to the history of electronics through your February 16 issue? Now that's what I call a real contribution!

I am the kind of guy who eats up documentaries on TV because they put things in perspective. That's what ELECTRONIC DESIGN has done for an entire industry and we are all in your debt. As a matter of fact, the essay is so delightful, that I am forcing myself to take it one chapter at a time. I generally reserve lunch hours for it so I can closet myself inconspicuously in my office and indulge my soul with your good writing and my body with a bologna on rye.

If you were thinking that a bologna on rye is an ideal sandwich for a public relations man—how could you?

Francis L. Kafka
Public Relations Manager
Micro Switch, Div. of Honeywell
11 W. Spring St.
Freeport, IL 61032

Software library is announced for SR-52

I have been waiting for quite a while for Texas Instruments to start a user software exchange program for the SR-52 as HP has done for the HP-65. However, such a program has not been forthcoming from TI to date, and after talking with Customer Service, I find there are no plans for one either. Therefore, I have decided to set up a software library for the SR-52.

I will publish an annual catalog of programs, and quarterly updates to it. All program submissions accepted by us will entitle the person submitting same to one free program from our library (or, at the beginning, a coupon to be exchanged later for the program of your choice). I am not trying to make any money on this, but only to break even on the deal. My reward will be the ability to use the programs submitted to the library. The first catalog will be published as soon as we have enough programs for it. The first update will be published about September if there is enough response.

Allyn T. Gallant
1526 Sunshadow Lane
San Jose, CA 95127

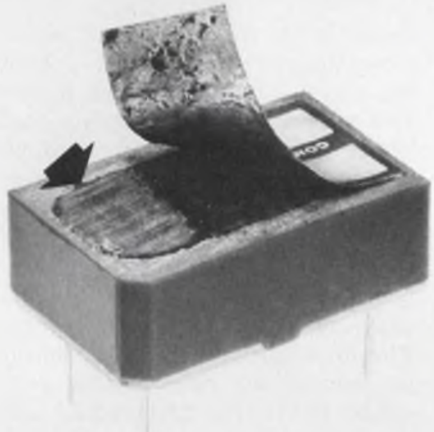
Misplaced Caption Dept.

When I said we needed more horsepower, that was just engineering jargon.

Sorry. That's Michelangelo da Caravaggio's "The Conversion of St. Paul," which hangs in the Church of Santa Maria del Popolo, in Rome.

Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Managing Editor, Electronic Design, 50 Essex St. Rochelle Park, N.J. 07662. Try to keep letters under 200 words. Letters must be signed. Names will be withheld on request.

The hole truth about crystal oscillators.



Unless you know about the holes in crystal clock oscillators, you don't know the whole truth about crystal clock oscillators.

So here's the truth about holes.

Oscillators with holes in them are called potted oscillators. We'd like to show you how one is made and tell you why it can go bad sooner.

Some oscillators have holes in their heads.

Look at the photo above. First, the crystal and other parts are attached to the base of the oscillator. Then a hollow cap (see the lighter part around the edges?) is put over this assembly and filled with epoxy. (See the dark center?) When the epoxy hardens, the manufacturer glues his label over the now filled hole. But what, you may ask, is wrong with that?

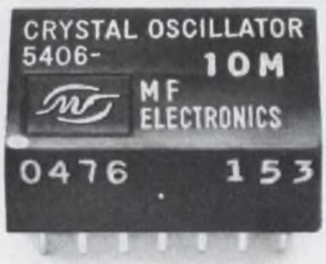
The truth of the matter is this: A label glued to an oscillator serves more to cover up than to inform.

As the epoxy hardens, air mixes with it. Air pockets form in which dirt and moisture can—and do—collect. It's dirt and moisture filling these holes that is the leading cause of oscillator failure. These holes also leave the unit open to all sorts of leaks, loose parts, and electrical shorting, all of which can lead to shortened oscillator life.

So the manufacturer puts his label over the potting hole, hoping that you won't notice what you can't see. (Some oscillators even have holes in their soles. Even though the label is stuck on top, the potting hole may be located on the underside of the oscillator.)

However it's done, it's a shame, the bad things most of our competitors are hiding under their good names.

The un-holey oscillator: It's molded. What a blessing.



There are oscillators made which are better than potted oscillators. They're called molded crystal oscillators. We at MF invented them and we're the only company that makes them.

A molded oscillator has no holes, no open spaces, nothing to hide and nowhere to hide it. Its crystal is hermetically sealed and set in a monolithic block of solid black plastic. There are no spaces for air to penetrate, no room for dirt or moisture to accumulate. Wave soldering can't even deteriorate the unit, so there's no danger of loose pins or joints.

A test that rings true.

One of our customers, who is also one of the country's largest users of crystal clock oscillators, tested the performance of various oscillators. He found that MF's molded oscillator lasted 3000 hours in an 85°C/85% relative humidity test. If you've ever done any oscillator testing yourself, you know how remarkable that is.

And there are no holes in our guarantee either.

At MF Electronics, we guarantee the molded oscillators we make for a full year. And that, in case you didn't know, is a full year longer than any of our major competitors will guarantee theirs.

And our prices are always competitive.

Simply stated, we make what we think are the best crystal oscillators you can buy. So that your product can be "the best you can buy."

And that's the whole truth.

THE MF GUARANTEE

MF Electronics warrants this molded crystal oscillator to be free from defects for one year from date of purchase.

Any oscillator found to be defective during this period may be returned to the factory, postage paid, for repair or, at our option, replacement without charge.

MF Electronics limits its liability to the repair and/or replacement of the returned MF oscillator.

MF ELECTRONICS CORP.

118 E. 25th St., New York, N.Y. 10010 (212) 674-5360 TWX: 710-581-4109

CIRCLE NUMBER 7

The hollow truth about crystal oscillators.

If you don't know what's wrong with most hollow crystal clock oscillators, you haven't got a very solid working knowledge of crystal clock oscillators.

So we'd like to take this opportunity to fill in those spaces in your logic.

These hollow oscillators are more properly known as hybrid oscillators. In the photo above we lifted the cap to show you how hybrid oscillators are made and why they can go bad sooner.

The parts that go into an oscillator are first miniaturized, then attached to a ceramic base. A metal cap is glued to this assembly and the resulting chamber filled with an inert gas.

But why, you want to know, is this so terrible?

A breath of fresh air can kill an oscillator.

What's wrong with hybrid oscillators is that they are glued together, a bond that is, at best, very tenuous. The oscillator might pass tests for hermeticity the day after it's made, but as time goes by, the glue can soften or crack, destroying the controlled atmosphere by letting the gas out and air, dirt and moisture in.

Once this happens, a hybrid oscillator is most susceptible to damage. As you can see, all its parts are fully exposed once you get under the metal cap. It's crystal isn't even sealed. (Even those oscillators with holes in them use standard crystals in hermetically sealed cases. A hybrid oscillator uses just a bare crystal.)

The solid oscillator.

There are oscillators made which are better than hybrid crystal oscillators. They're called molded crystal oscillators. We at MF invented them and we're the only company that makes them.

A molded oscillator has no holes, no open spaces, nothing to hide and nowhere to hide it. Its crystal is hermetically sealed and set in a monolithic block of solid black plastic. There are no spaces for air to penetrate, no room for dirt or moisture to accumulate. Wave soldering can't even deteriorate the unit, so there's no danger of loose pins or joints.

Two more solid reasons to use MF Oscillators.

3rd overtone crystals are used in MF's molded oscillators to provide greater electrical and mechanical stability in frequencies exceeding and including 20MHz.

And an MF molded oscillator is the only one made that meets the UL oxygen index guideline of 28%.

Because we're solid, your product is more solid.

At MF Electronics, we guarantee the molded oscillators we make for a full year. And that, in case you didn't know, is a full year longer than any of our major competitors will guarantee theirs.

And our prices are always competitive.

Simply stated, we make what we think are the best crystal oscillators you can buy. So that your product can be "the best you can buy."

And that's the solid truth.

THE MF GUARANTEE

MF Electronics warrants this molded crystal oscillator to be free from defects for one year from date of purchase.

Any oscillator found to be defective during this period may be returned to the factory, postage paid, for repair or, at our option, replacement without charge.

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MF ELECTRONICS CORP.

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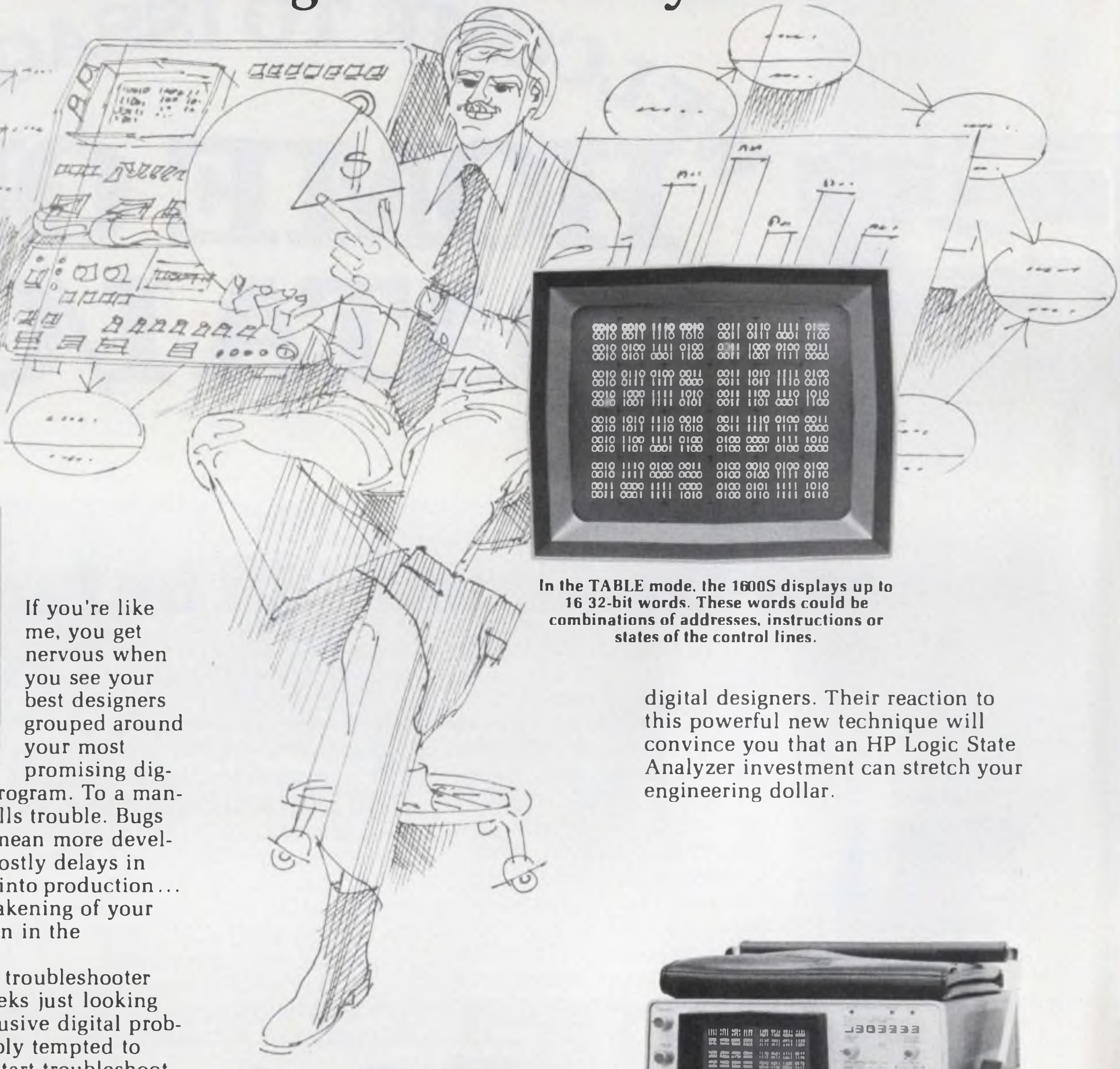
CIRCLE NUMBER 8

Let's talk about
YOUR ENGINEERING DOLLAR
and HP Logic State Analyzers.



In the TABLE mode, the 1600S displays up to 16 32-bit words. These words could be combinations of addresses, instructions or states of the control lines.

If you're like me, you get nervous when you see your best designers grouped around your most promising digital development program. To a manager, that often spells trouble. Bugs in the design that mean more development money...costly delays in getting the product into production... perhaps even a weakening of your competitive position in the marketplace.

When your best troubleshooter spends days or weeks just looking for the source of elusive digital problems, you're probably tempted to jump right in and start troubleshooting yourself.

Actually, there's a better solution. And it beats waiting, twiddling your thumbs, and hassling your designers. Give them the equipment they need to find the problem source quickly. I mean HP Logic State Analyzers—the latest and most effective tool I know of for digital design and troubleshooting.

They give your designers an operational view of program flow. Thirty-two channels let them see combinations of address, data and control, capturing 16 successive clock periods at one time. And for intermittent problems they can store and look back in time (negative time) to see what took place before a problem occurred. That's the kind of capability you probably wished your test equipment had when you were tackling similar types of digital problems.

Time and again, our customers have told us that HP Logic State Analyzers have saved hours, days, and even months of difficult digital troubleshooting.

Save yourself some anxious hours and unpleasant budget sessions. Find out how HP Logic State Analyzers can help your designers pinpoint problems quickly and help get your designs into production on time.

Send for our new 8-page brochure on Logic State Analyzers, and for information on data-domain application notes. Contact your local HP field engineer too, and ask him about HP's Logic State Analyzer application seminars. Then send your top digital designers. Their reaction to this powerful new technique will convince you that an HP Logic State Analyzer investment can stretch your engineering dollar.

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1507 Page Mill Road, Palo Alto, California 94304

CIRCLE NUMBER 11

Coming through...

with wire, cable and cord that delivers quality, performance, economy...

Belden has it: a total service capability. Extensive design and application know-how. What it takes to deliver complex cable configurations, special harnesses, cords, lead wires, and even special packages to fit your requirements.

Our specialists and engineers will meet with your people at your plant to discuss problems in processing, assembly, installation, ordering, human engineering, color coordination, physical and electrical parameters, opportunities for cost reduction. And when we can't help you using standard products, we'll innovate a solution to your problem.

Talk to a Belden specialist about your new applications, product ideas, processing problems—all your wire, cable and cord needs. He has thousands of standard items to draw from. And standard or special, he'll come through with the best wire buy around. For answers right now, phone:

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312-986-1600 Electrical Div. or mark No. 401 on reader service card
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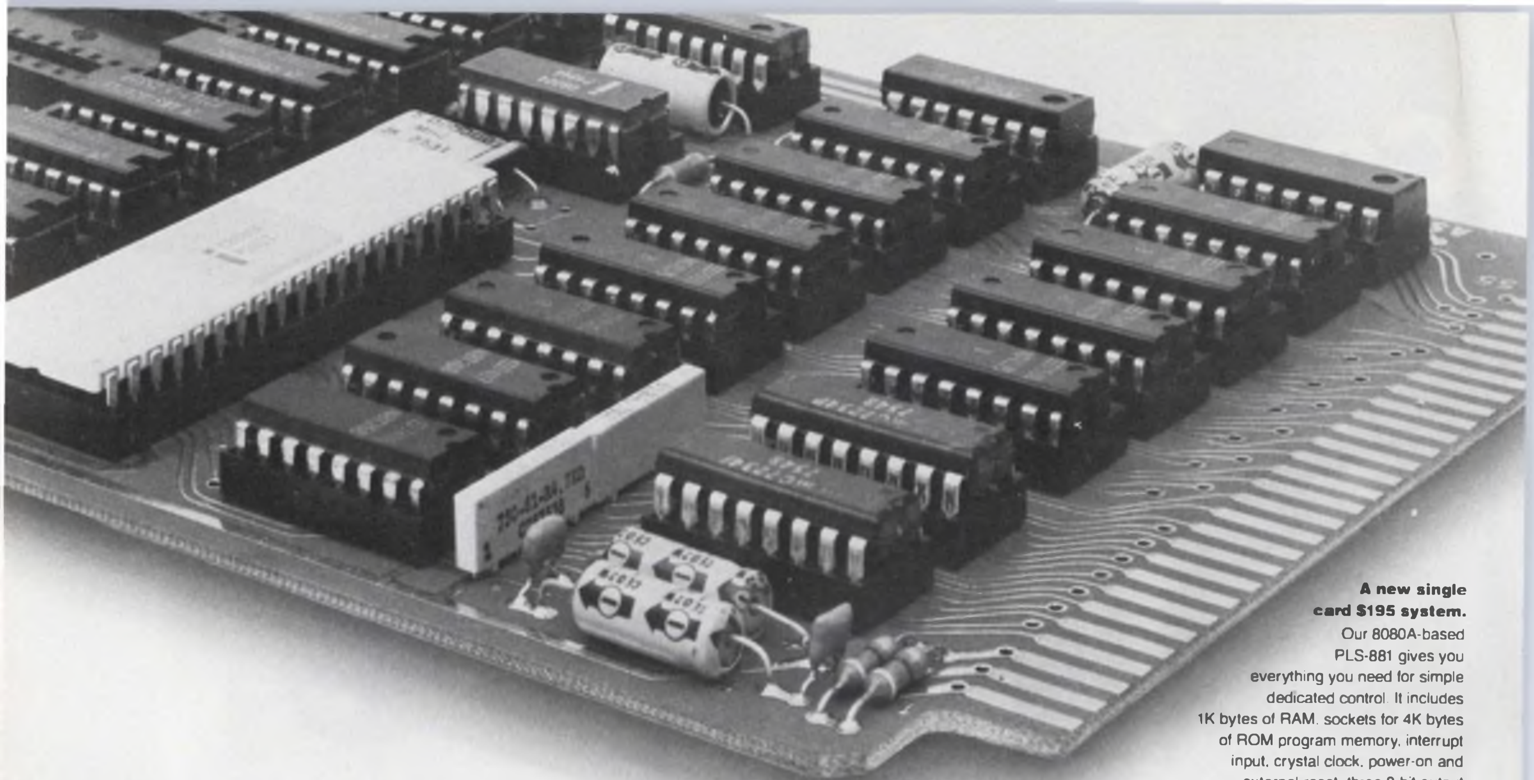
BELDEN

Coming through....
with new ideas for moving electrical energy

H-1-6



A new single card $195 system. Our 8080A-based PLS-881 gives you everything you need for simple dedicated control. It includes 1K bytes of RAM, sockets for 4K bytes of ROM program memory, interrupt input, crystal clock, power-on and external reset, three 8-bit output ports, and two 8-bit input ports. It costs only $195 in 100 piece quantities.

Bite-sized Pro-Log 8080A systems make big boards hard to swallow.

Simple, flexible, standardized Pro-Log 8-bit microprocessor systems a best buy for OEM's.

We sell 8080A, 6800 and 9002 microprocessor cards two ways; as complete single or multicard systems, or as individual CPU and support cards so you can build a system of your own.

Our cards are all standard 4.5" by 6.5" with 56 pin edge connectors. They fit into standard card racks. To keep you from being tied to a specific semiconductor manufacturer for parts, delivery and pricing, our 8080A and 6800-based systems use only second-sourced parts.

Buy 250 of any particular card and we throw in free its manufacturing and assembly plans and non-exclusive rights to manufacture it, allowing you to build your own hardware, relying on us as an established and dependable second source.

We've got 4-bit systems, instruments, education and literature, too.

4-bit 4040 and 4004 systems; 4- and 8-bit microprocessor system analyzers; PROM programers; a half-day economics seminar for decision makers; a three-day hands on design course for engineers; manuals and support documentation.

Call or write for data sheets or a free copy of The Microprocessor User's Guide.

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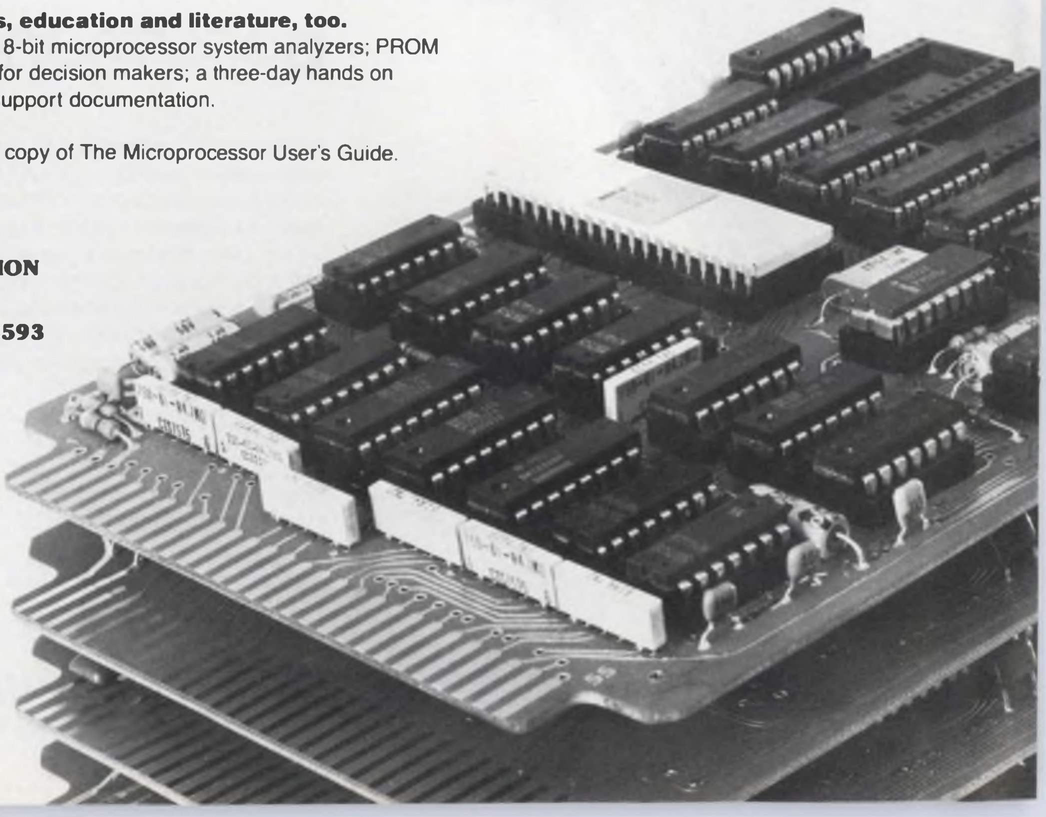
Monterey, CA 93940
Telephone (408) 372-4593
TWX 910-360-7082

See us at Wescon Booths 853-855
and at ISA Booth 948



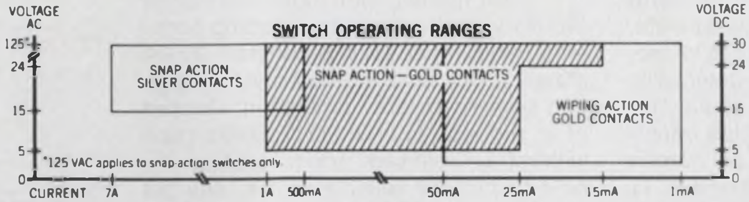
A new, expandable plug-in CPU card. Our "buffered bus" 8821 processor card implements the 8080A as a fully TTL buffered microprocessor. Add one I/O card and it becomes a complete two-card system. Or expand it to use full 8080A memory and I/O capability—it's compatible with all the Pro-Log ROM, RAM and I/O modules shown here plus many more. The 8821 costs only $190 in 100-piece quantities. We also have equivalent cards implementing the 6800 and 9002 microprocessors.

CIRCLE NUMBER 12

Dialight Switches

A switch for all reasons.

Reason 1: Dialight offers three switch configurations to meet all your needs—*snap-action switches with silver contacts* for moderate-level applications, *snap-action switches with gold contacts* for intermediate-level applications, and *wiping-action switches with gold contacts* for low-level applications. Each of these ranges is served by two switching actions—momentary (life: 600,000 operations) and alternate (life: 250,000 operations).

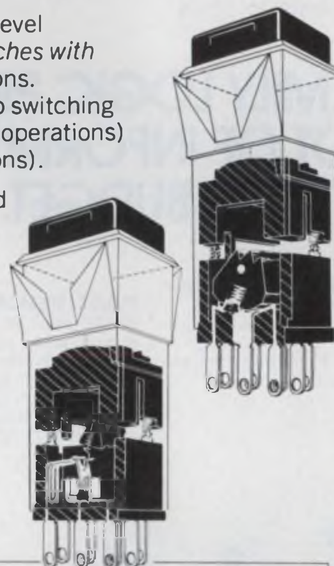


Reason 2: Dialight's snap-action and wiping-action switches come in a new modular design concept . . . a common switch body for either high or low current operation. All 554 series switches and matching indicators have the same rear-panel projection dimensions.

The snap-action switching mechanism guarantees a fast closing and opening rate. This insures that contact force and contact resistance are independent of the switch's actuation speed.

In the wiping-action switch, the contacts are under constant pressure (A unique Dialight design). This insures long life with a minimum build-up of contact resistance.

Both switch types are tease-proof.



PRODUCT SELECTOR GUIDE

SWITCHING ACTIONS	Snap-Silver contacts SPDT	Snap-Silver contacts DPDT	Snap-Gold contacts SPDT	Snap-Gold contacts DPDT	Wiping-Gold contacts SPDT	Wiping-Gold contacts DPDT
MOMENTARY	O	O	O	O	O	O
ALTERNATE	O	O	O	O	O	O

OPTIONS

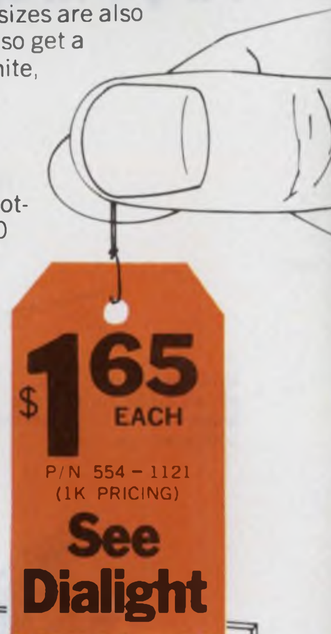
	PUSH BUTTON CAP SIZES ½" Sq.	⅝" Sq.	⅝" x ¾"	¾" Sq.	¾" x 1"
BEZEL MOUNTING TO ACCOMMODATE	O	O	O	O	O
BEZEL MOUNTING WITH BARRIERS TO ACCOMMODATE		O	O	O	O
PANEL MOUNTING TO ACCOMMODATE	O	O	O	O	O
MATCHING INDICATORS	O	O	O	O	O

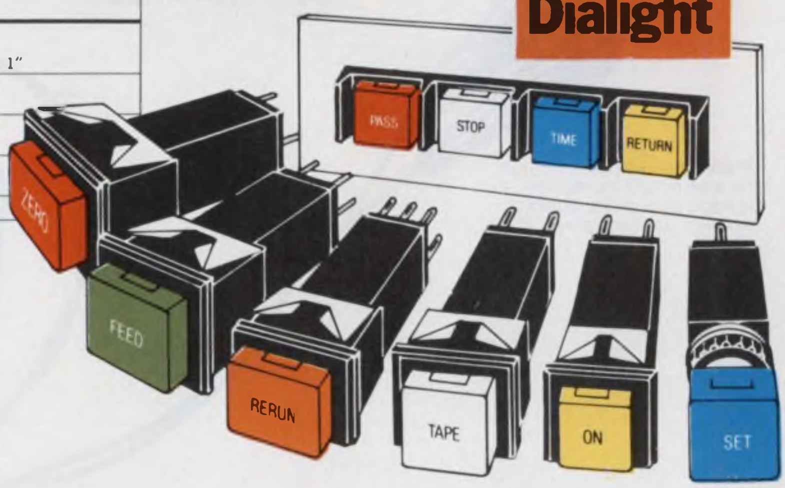
Reason 3: Dialight offers a wide variety of panel and snap-in bezel mounting switches with momentary and alternate action configurations in SPDT and DPDT types. There are over 240 switch variations to choose from.

The 554 illuminated switch, designed for front of panel lamp replacement, gives you a choice of five different bezel sizes . . . ¾" x 1", ⅝" x ¾", ¾" square, ⅝" square, and ½" square. The first four sizes are also available with barriers. You also get a choice of six cap colors . . . white, blue, amber, red, green, and light yellow . . . four different underlying filter colors . . . red, green, amber, and blue and a variety of engraved or hot-stamped legends . . . over 300 cap styles . . . over 100,000 combinations.

There is also a variety of terminal connections . . . solder blade, quick connect, and for PC board insertions.

Reason 4: Dialight's 554 series is designed as a *low cost* switch with *computer-grade quality.*





DIALIGHT
A North American Philips Company
203 Harrison Place, Brooklyn, N.Y. 11237
(212) 497-7600

CIRCLE NUMBER 13

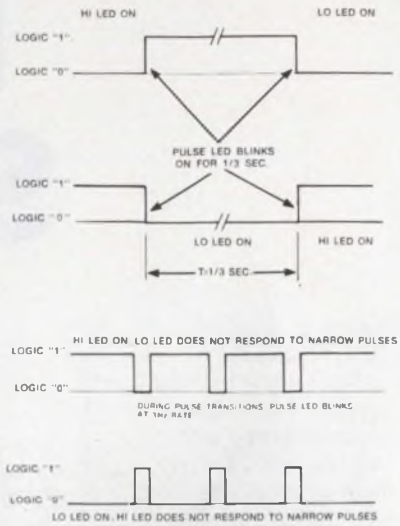
Logic Probe 1 is a compact, enormously versatile design, test and troubleshooting tool for all types of digital applications. By simply connecting the clip leads to the circuit's power supply, setting a switch to the proper logic family and touching the probe tip to the node under test, you get an instant picture of circuit conditions.

LP-1's unique circuitry—which combines the functions of level detector, pulse detector, pulse stretcher and memory—makes one-shot, low-rep-rate, narrow pulses—nearly impossible to see, even with a fast scope—easily detectable and visible. HI LED indicates logic "1", LO LED, logic "0", and all pulse transitions—positive *and* negative as narrow as 50 nanoseconds—are stretched to ⅓ second and displayed on the PULSE LED.

By setting the PULSE/MEMORY switch to MEMORY, single-shot events as well as low- rep-rate events can be stored indefinitely.

While high-frequency (5-10MHz) signals cause the "pulse" LED to blink at a 3Hz rate, there is an additional indication with unsymmetrical pulses: with duty cycles of less than 30%, the LO LED will light, while duty cycles over 70% will light the HI LED.

In all modes, high input impedance (100K) virtually eliminates loading problems, and impedance is constant for all states. LP-1 also features over-voltage and reverse-polarity protection. Housed in a rugged, high-impact plastic case with strain-relieved power cables, it's built to provide reliable day-in, day-out service for years to come.



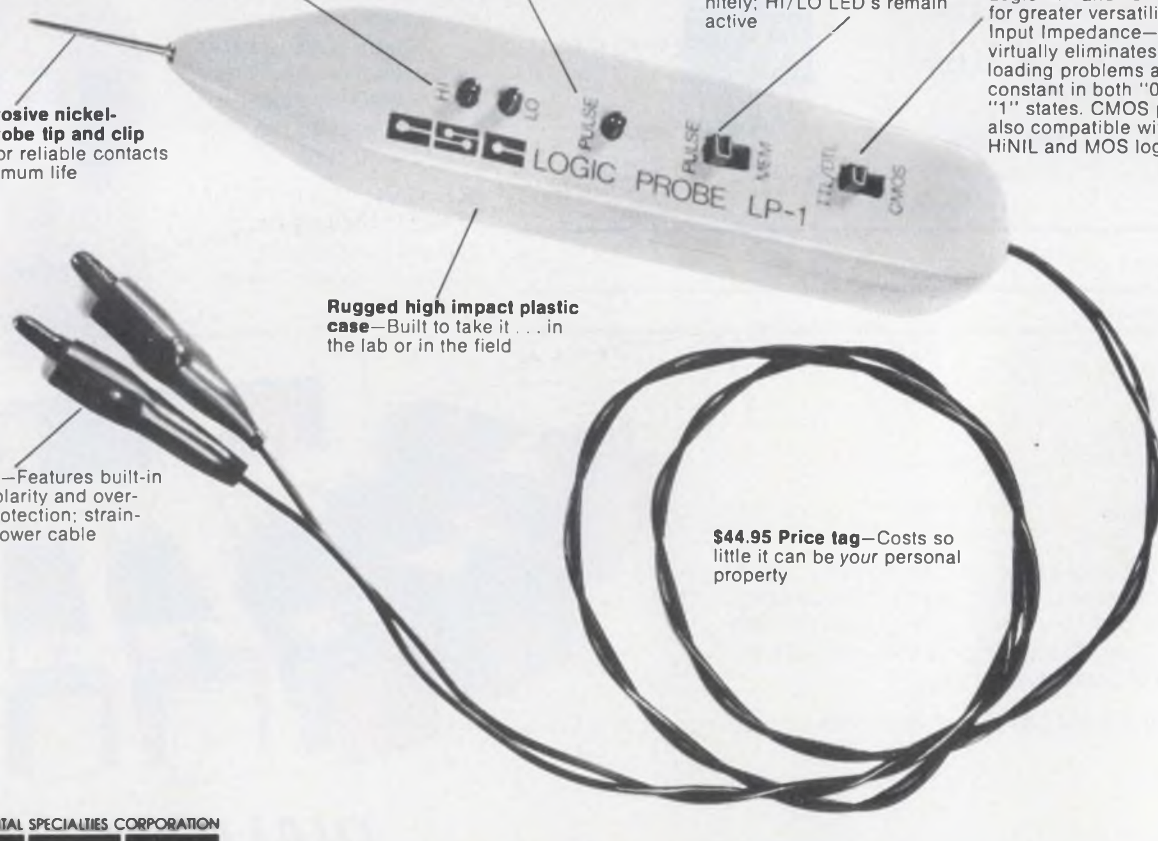
CSC'S MULTI-FAMILY LOGIC PROBE 1. AT $44.95, IT DIGS UP A LOT OF INFORMATION WITHOUT BURYING YOUR BUDGET.

PULSE LED—Lets you know what's going on—and off. Indicates positive *and* negative pulse and level transitions. LP-1 stretches pulses as narrow as 50 nanoseconds to full ⅓ sec. (3Hz pulse rate)

PULSE/MEMORY Switch—PULSE position detects and stretches pulses as narrow as 50 nanoseconds to ⅓ sec. Switch to MEMORY and it stores single shot and low-rep-rate events indefinitely; HI/LO LED's remain active

HI/LO LED's—Display level (HI-logic "1", LO-logic "0") of signal activity at node under test

Logic Family Switch—TTL/DTL or CMOS matches Logic "1" and "0" levels, for greater versatility. High Input Impedance—100K virtually eliminates circuit loading problems and is constant in both "0" and "1" states. CMOS position also compatible with HTL, HiNIL and MOS logic



Non-corrosive nickel-plated probe tip and clip leads—For reliable contacts and maximum life

Rugged high impact plastic case—Built to take it . . . in the lab or in the field

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$44.95 Price tag—Costs so little it can be *your* personal property

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Get the most from your COM, photocomposition or medical imaging system with RCA CRTs. Clear, sharp photographic records result from our special combination of electron gun design, phosphor material synthesis and fine-grain phosphor deposition. And you can count on us to meet your volume needs. The 5" dia. 4869 or 4870, with 1-2 mil line widths, have optically flat faceplates, magnetic deflection and electrostatic or magnetic focusing. Special needs? See us—we have others to suggest.

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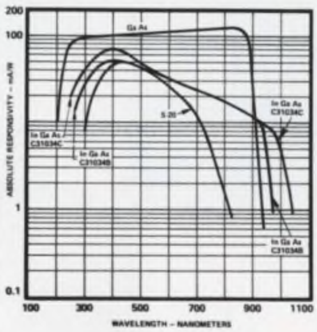

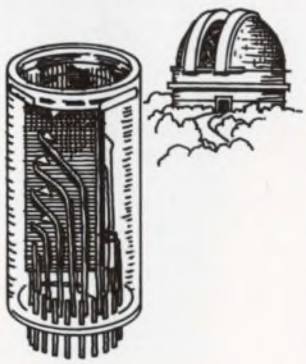

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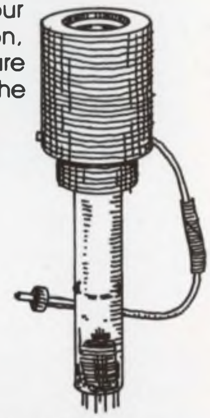

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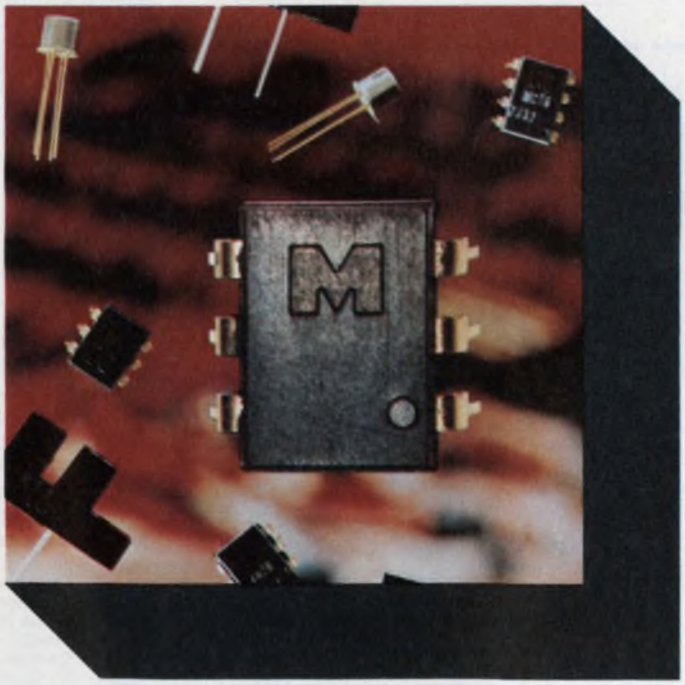
Transistor	TO-18 Metal Can	15%	1000
Darlington	6 Lead Plastic DIP	100%-200%	1500
Diode	6 Lead Plastic DIP	.15%	1500
Diode	TO-18 Metal Can	.10%	1000

Output Format	Package Types	Forward Blocking Voltages (V_{FXM})	Min. DC Isolation Voltage (V)
SCR	6 Lead Plastic DIP	200V-400V	1500
2 SCR's (Connected Anode to Cathode)	8 Lead Plastic DIP	200V	1500-2500

Output Format	Package Types	Typical Bandwidth	Min. DC Isolation Voltage (V)
Logic Gate	8 Lead Plastic DIP	0.1MHz-1.0MHz	2000

Output Format	Package Types	Collector Current (I_C) @ (I_F, V_{CE})
Transistor	Slotted Limit Switch	50μA @ 20mA, 10V 200μA @ 20mA, 10V
Darlington	Slotted Limit Switch	1.6mA @ 50mA, 1V 2.0mA @ 16mA, 1V
Darlington	Reflective Sensor Switch	50μA @ 50mA, 5V



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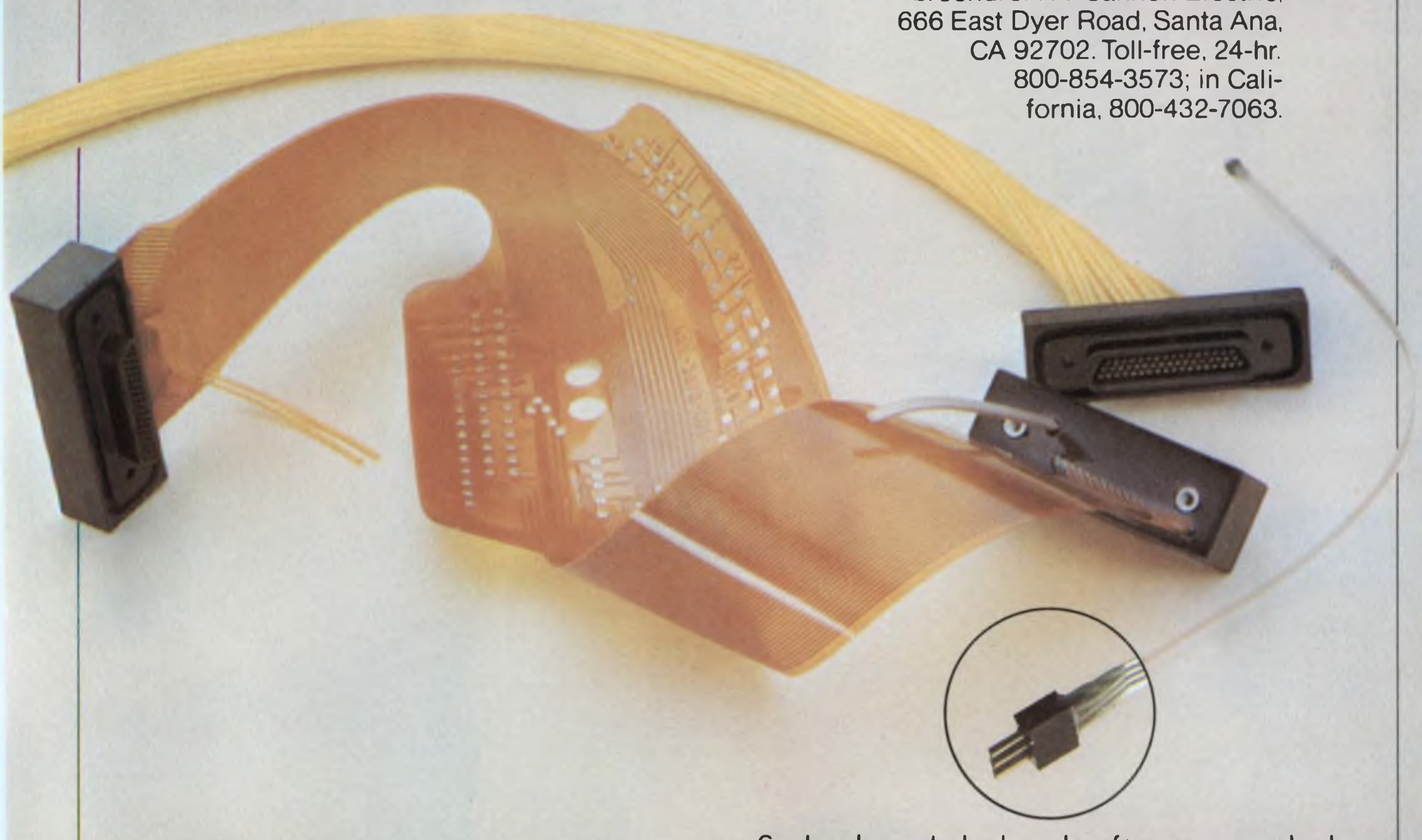

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CIRCLE NUMBER 19

SEPTEMBER 1, 1976

Performance of military systems monitored by μPs

Microprocessors are finding increased use in monitoring the performance of military systems. Two examples to be described at the Electronics and Aerospace Systems Conference (EASCON) Sept. 26-29 in Washington, DC, will be a combined performance monitor and fault diagnosis μP system for radar equipment and a low-cost, microprocessor-controlled security system.

The first system, which uses an 8080 μP, will be discussed in a paper entitled "Microcomputer Built-In Test for Radars" by Don Weidner, systems engineer at the Naval Electronics Laboratory Center in San Diego, CA.

This test system was designed to reduce the time to locate and to repair equipment, thus increasing the availability of the equipment. A microprocessor was chosen to scan some 180 to 200 points, depending upon the type of equipment being monitored, because it was compatible with the modular packaging of the equipment. (A dedicated minicomputer had been considered for the task, but was thought to be too large.)

In operation the μP might scan about 100 digital and 80 analog test points. The digital signals at these points are related to digital control and processing present in the radars, while the analog signals include everything else, such as receiver signals and power supply voltages.

In the performance-monitoring mode, the μP keeps track of the digital and analog values, and should one fall outside of limits, indicates a malfunction. In this case, the μP is programmed to switch to a diagnostic mode in which it performs an ordered search of the test points to locate the failure or the improper operation.

This system, Weidner will point out, will also detect the gradual degradation of radar operation that normally would have gone unnoticed for some time simply because the degradation was slow.

The test system has a LED numeric display. The numbers may indicate that a test should be performed because a problem has developed, or the μC output may be displayed as a numeric code to a needed repair.

All test points are accessible through front-panel switches. To check a point, the operator inserts the test index number through the switches and pushes a panel button. The LED display shows the value of the signal or information at that test point.

For a digital test point, the display will give the logic level and will show whether or not a driving pulse is present. For an analog test point, the readout will be like the one for a digital multimeter.

The low-cost, microprocessor-controlled security system to be used by the Navy will be described in a paper entitled "Shipboard Damage Control Monitoring System," by Lt. James Jordan of the Naval Post Graduate School, Monterey, CA. Jordan will point out that because the warships are divided into small compartments to prevent the spread of fire and flooding, the sources of such catastrophies are difficult to locate. Consequently, he proposes to use a low-cost, power-line carrier system like the one enabling intercoms to carry signals from fire and flood sensors in all compartments to a microprocessor-controlled scanning system. The security system would be tied in with damage control central and with alarms on the bridge and quarter-deck.

Standard microprocessors are suitable for this purpose because such a system would only need to monitor a sensor once every minute. Also, the size of the memory can easily be increased with the size of the ship.

27 geophones protect miners from rock bursts

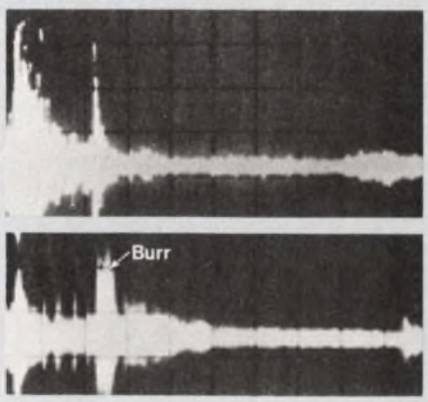
A network of 27 geophones monitored by an IBM System/7 computer has been installed a mile below the earth's surface in the Sunshine Mine in Idaho to detect, pinpoint and measure the intensity of rock noises which normally precede a rock burst.

The typical noise pattern before a burst is a series of snapping and popping noises which build up to a certain point and suddenly stop. The silence is usually broken by a rock burst.

The computer's job is to count noises and to warn of build-ups so that the specific area can be evacuated. If enough warning is given, the stress might be relieved by drilling holes to disperse the stress.

Acoustical die monitor will warn of faults

For years, punch press operators have noticed that a malfunction is preceded by a change in the sound the press makes. Now, an acoustical die monitor built by Westinghouse Electric's Control Products Division, Beaver, PA, will detect and interpret the vibrations creating these sounds: consequently, the operator will be warned that something is going to happen. The monitor will even shut the press down, if need be.



A new acoustical die monitor displays a normal audio signal (above) from a punch press and one (below) that reveals a serious burr.

The monitor can sense such deviations as double cuts, serious burrs, jams, defective strippers and broken or loose punches. Quick detection of these malfunctions will result in savings on maintenance and repairs as well as increased productivity with less downtime.

By reacting quickly to changes in operating conditions, the acoustical die monitor can also reduce problems resulting from feed failures, dullness in dies, loss of lubricant, foreign matter between dies, and the use of over-or under-sized material.

After the monitor is connected either to the bolster plate or directly to the die it is put in "standby" position. Then the operator starts the press and observes its run until he is satisfied that the press is operating properly. Next, he turns a key and depresses a "learn" button. For the next seven to 12 cycles of good operating conditions, the monitor translates incoming voltage signals into a useable constant, or signature. From then on, all subsequent stroke patterns are compared to the signature.

As long as each new incoming signal is similar to the signature, the monitor displays a green light. When something goes wrong—lubricant is lost or a die becomes dull—a white light flashes. If the monitor detects serious trouble, a red alarm indicator light goes on and the press is shut down—before it has even completed one additional stroke.

The unit is almost totally self-contained, with only four outside connections: a 120-volt power supply, a piezoelectric sensor of acceleration (the sensor to develop the montor's input), the sync pulse input, and the internal relay output.

Corning introduces 200-MHz optical cable

A 200-MHz-bandwidth, six-channel optical cable has been introduced by Corning Glass Works.

The new cable's frequency response is ten times better than the Corguide cable Corning introduced last year. It was manufactured by means of a doped-deposited silica process, producing a graded index of refraction in the individual strands.

In contrast, the Corguide cable was manufactured with a discrete step, or change, in the index of the cladding.

Maximum attenuation of the optical energy in each optical waveguide is 20 dB per km at a wavelength of 820 nm, the same as the earlier cable.

Each of the six waveguides has a smooth, low-modulus, polyurethane coating for protection and to minimize crosstalk. The six are stranded around a central strengthening member. The cable structure, originally developed for the U.S. Army Electronics Command, Ft. Monmouth, NJ, has two strands of high-strength, high-modulus plastic to further ruggedize the assembly (See ED No. 8, April 12, 1976, p. 40).

The new Corning cable is suited for high-data-rate communications applications, and is priced at $13.50 per meter. It is competitive with premium grades of coaxial cable.

Maximum optical crosstalk between waveguides in the cable is −80 dB per km at 647 nm.

Personal computing—the next consumer boom

Hot on the heels of the CB radio explosion comes the personal computer boom. Recognizing this fact, a group of computer owners from southern New Jersey got together to produce the first national convention dealing with computers for the consumer. Known as Personal Computing 76, the conference took place on August 28 and 29 in Atlantic City, NJ, and featured several technical sessions. Among the topics discussed were:

- A new input device which can be used to read data directly into a computer from the printed page.
- How to convert hardware designers into software designers.
- Standardization of techniques used to store data on inexpensive cassette recorders.

An easy way to overcome the problem of inputting available software into computers is to teach computers to read it directly from the printed page, says Walter Banks, head of the computer communications network group at the University of Waterloo in Canada.

In his presentation, Banks described a simple and inexpensive technique he has developed which would make it possible to read programs directly from magazine articles. To do this, he explains, the data are printed as a series of bars, similar in some ways to the codes now found on supermarket products. The width of the bars would vary to represent a ONE or ZERO, and seven bars would be used to represent each character. Codes could be made ASCII compatible.

Using this technique, Banks noted that it would be possible to print 17,500 bits of data on a 7.5-by-10-in. page. To read the data, a user would simply take a hand-held device and scan each line. Built in error correction codes could correct any reading errors. The cost for this whole system, he went on, would be between $25 and $50, a small price.

With micros invading almost every aspect of electronic design, it is very important to show hardware-oriented designers that they can use most of their hardware design techniques to produce the software necessary to run a micro. So said Timothy Barry of Logical Services Inc., Mountain View, CA—a company whose sole purpose is just that.

In his paper, "Converting Hardware Designers to Programmers," Barry pointed out that software designs can be broken down into building blocks just like hardware designs. By successively detailing these blocks as is done in standard hardware design, it is easy to come up with the needed software, he says. The only big difference is that where a hardware designer uses gates, registers, and other devices, the software designer uses subroutines, tables, and other software modules.

Another session at the conference covered the area of standards for the personal computing field.

Among the items discussed was a cassette interface standard that would permit recording of data on cheap recorders. A previous standard that was agreed to by a group of manufacturers and users in Kansas City last year was questioned. Opponents of the Kansas City standard pointed out that its 300 baud rate was too slow and that its Manchester coding format was redundant. Other faster interfacing schemes were proposed.

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CIRCLE NUMBER 20

PLAs or μPs? At times they compete, and at other times they cooperate

"The PLA (Programmable Logic Array) may soon be on its way out. It's going the way of the dinosaur and the dodo bird and will eventually be a museum piece. The microprocessor is pushing it out of existence."

"That's not so. The PLA is not only alive and doing well, but in fact a second generation is being spawned. New devices, now on the drawing boards, will be available soon."

These two views are rather extreme. But they do reflect the variety of opinions heard in today's fast-moving IC marketplace.

Samuel Derman
Associate Editor

Uncertainty about which of today's PLAs and μPs will still be available in the future is but one of the problems a design engineer must face in choosing between the two devices.

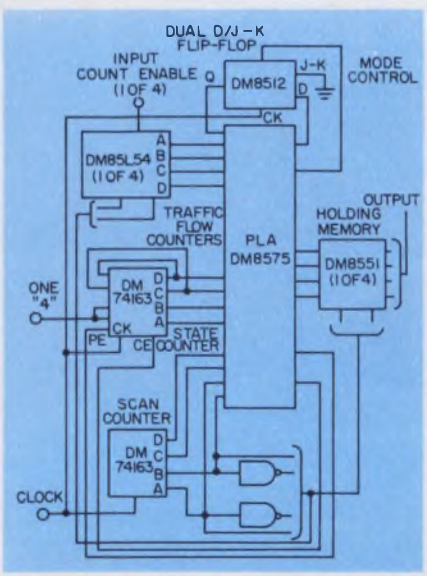
A Pandora's box of other problems exist, and the ultimate choice of whether to go to PLAs or to μPs must be based on careful evaluation of such factors as:

- Speed in getting a product to the market.
- Second sourcing.
- Power-supply requirements.
- Possible obsolescence of essential components.
- Provision for future design changes.
- Speed of handling input/output (I/O) functions.
- Total cost.
- The type of problem to be solved (PLAs and μPs are not equivalent devices).

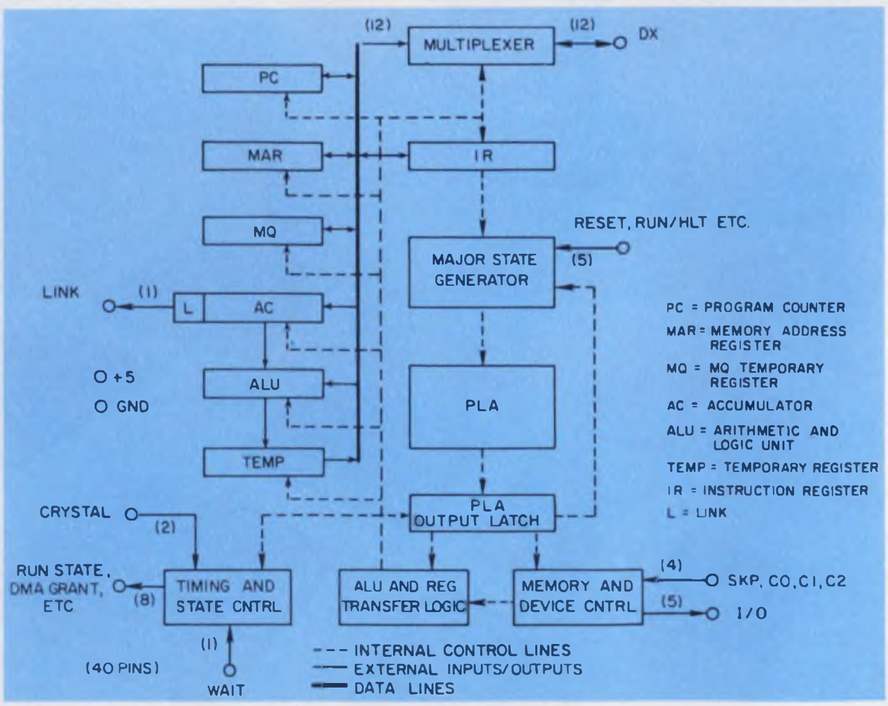
First come, first sold

Experts agree that a tidal wave of new IC-based consumer equipment is about to engulf the marketplace. They feel that already-existing items such as TV-games, automotive devices and point-of-sale terminals represent only the small, visible crest of an approaching flood.

For many manufacturers about to plunge into these turbulent waters the difference between success and failure may hinge on getting their device to the marketplace fast enough to beat out competitors. And achieving such a



1. **A PLA serves as the control element** to provide the timing interval in this traffic-light controller. Traffic flow in any of four directions is managed by this unit.



2. **The Intersil IM 6100, 12-bit microprocessor** is one of a number of μPs that use PLAs for sequencing the CPU.

fast design turn-around time may dictate that a Field Programmable Logic Array (FPLA) be used in place of a μP (or any other logic device)—at least at first.

FPLAs, in contrast to earlier mask-programmable units, can be programmed "on the spot" (see box). Any problems that are discovered can be corrected for, simply by programming a new unit and discarding the old one. Later on, as time permits, a mask can be designed so that mask-programmable arrays, which are more amenable to volume production—can be used.

An important point to note is that FPLA prices have been coming down, to the point where it's impossible to state flatly that mask devices are always cheaper for production runs.

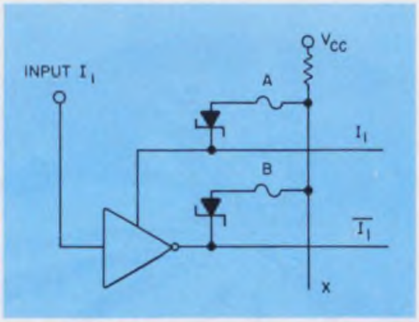
Prices as well as ease of programming the FPLA, must be carefully checked against the costs encountered in using a mask. And into the equation must be added the additional expense and anguish that inevitably accompanies the discovery of errors in the logic—after the mask has been delivered.

Applications abound

Like the ubiquitous μP, the PLA can be used to implement or simplify an increasing number of digital logic-based devices.

"A PLA can simplify many traditional ROM applications," says Dale Mrazek of National Semiconductor, Santa Clara, CA. One use he cites is in code conversion. Another is in traffic controllers.

"These controllers usually require a random set of simultaneous input variables to satisfy a particular state. The condition then allows an advance to the next controller state of the sequencer," he points out.



3. Fusible links in an FPLA allow the designer to form a wide variety of logic configurations. In this example, one input circuit is connected to an FPLA. The designer can select either the input, I_1, or its complement, $\bar{I}_1$, depending on whether he fuses link B or link A. The resulting signal appears on line X.

In systems such as traffic controllers the PLA is used in an area usually dominated by the μP—applications requiring a time sequence of operations.

For such applications, it may seem that the time and effort required to program the PLA may be less than that needed to develop the necessary μP software. But such a quick judgement may prove erroneous.

In the early stages of μP development, it would have been accurate to state that compared to the PLA, the μP was a more difficult device to program and debug. But today, many engineers are familiar with μPs, and the required software has gone through a "refining" process.

As a result, all one can say nowadays is that ease of programming —whether for a μP or a PLA—depends to a large degree on the skill and background of the user.

Gopol Ramachandran, senior applications engineer at Intersil, Cupertino, CA, cites an application where the FPLA is currently finding increased use.

Taking advantage of the FPLA's ability to decode a particular address rapidly, engineers are now using these devices to implement the ASCII standard interface bus (IEEE 488-1975).

An FPLA is connected to each piece of equipment on the line, with the FPLA serving as a decoder to determine which items of equipment is being "spoken to" at any particular moment.

Such a decoder can be implemented with random logic as well, or even with μPs, Ramachandran says, but the FPLA does it very simply and economically using only two items, an FPLA and a dual-D flip-flop.

In applications where speed of operation is important, the PLA wins over the μP hands down. The PLA basically senses the logic state of a set of inputs and delivers a particular output in response to these inputs. It's a one-shot operation, and the delay (from input to output) might be on the order of 100 ns or less. For the Signetics 82S100 and 82S101 Bipolar FPLAs for example, the spec sheets list the maximum propagation delay as 50 ns. The Intersil IM5200 FPLA has a maximum delay of 100 ns.

In contrast to the "one shot" action of the PLA, a μP must sequentially step through a series of operations to solve a given logic problem. This, of necessity, takes a longer time. A "logical decode" operation, for example which might take 50 ns using PLAs, would require about 15 to 30 μs

Characteristics of programmable logic

	Speed	Volume Cost/Function	Device Reliabiilty	Programming Method
Random Logic	0.7-200 ns	2 to 50¢/gate	Very High	Wire interconnects
PLA	50 ns	$25	High	Masks
FPLA	50 ns	$30	Medium	Fusible Links
ROMs	20-3000 ns	0.1 to 1¢/bit	High	Masks
PROMs	20-1500 ns	0.25 to 3.0¢/bit	Medium	Fusible Links
EAROMs	450-3000 ns	1-2¢/bit	Medium	Trapped Charges
RAMs	2-3000 ns	0.2 to 5¢/bit	Medium	Writing
CAMs	30-1000 ns	15¢/bit	Medium	Writing
Microprocessors	55-250 ns	$15 to $40/chip	High	Any or all of the above elements

if implemented with a single-chip MOS μP.

It's important, however, to restrict any comparisons of speed only to those (limited) applications that can be implemented by both devices.

Vive la difference

"PLAs and μPs currently do not serve exactly the same function," says Milt Baumwolspiner of Bell Labs, Holmdel, N.J. "It's not like comparing, say LEDs with liquid-crystal displays." PLAs and μPs often can complement each other, as for example when a PLA is used as part of a μP (see Fig. 2).

The non-equivalency of the PLA and μP is further emphasized by John Birkner of Monolithic Memories Inc., Sunnyvale, CA. "In the past, μPs have been used in high-performance applications such as airborne navigational computers or minicomputers. But the direction they're taking today is towards low-performance applications in which the μP is basically the only element needed," he says.

"In large-volume applications the PLA is fitting into the high-performance market, although for certain small applications a PLA and μP can work together."

A simple example, Birkner says is putting a latch at the output of a PLA to generate a sequencer. Such a sequencer can be used for a microcycle timing generator.

Birkner feels that present-generation PLAs find use in two main areas. The first is in micro-instruction decoders in minicomputer-like devices. Macro-instructions may be thought of as operation codes specifying particular subroutines.

The subroutines lead to micro-instruction sequences that directly perform operations such as fetching immediate values, or register or memory contents.

A second popular PLA application is for ROM patches. Suppose a PLA is used to decode an address—in a magnetic tape controller, for example. At some future time the microprogram for the controller may need revisions. Then, rather than throw away all his PROMs and program new ones, the engineer uses a PLA to decode the address locations he wants to change. The PLA can be used either to generate new data or to

All about PLAs

A PLA basically is an array of logic gates (ANDs, ORs, NANDS, NORS, etc.) all formed on a single IC chip. The gates can be joined together to form any combinatorial logic function desired. That is, given a certain digital input, the collection of gates will deliver a particular digital output.

The input signals first pass through a series of AND gates, resulting in a predetermined number of product terms being formed. In present-day PLAs and FPLAs this number runs anywhere from about 40 to 150. The product signals then pass through a set of OR gates to become the final output signals.

A typical FPLA, the Monolithic Memories Model 5780/6780, for example, comes configured with 14 inputs and 8 outputs. Depending on the logic state (one or zero) of each of these 14 inputs, a particular bit pattern will appear at the output. For example, The binary number 00010011000011 at the input might be the signal to cause the number 10010111 to appear at the output.

Figure 4 illustrates two elementary examples of how a PLA can be connected to implement a combinatorial logic function. These examples are based on a PLA with only one output (labelled F_y) instead of eight.

In the first example, the PLA is connected to synthesize the logic function

$F_y = \overline{C}\overline{D} + A\overline{B} + A\overline{C} + \overline{A}C$

Example 2 illustrates the synthesis of $F_y = ABC + \overline{A}\overline{C}D$

PLAs are currently available in two types, depending on the method used for connecting the logic gates.

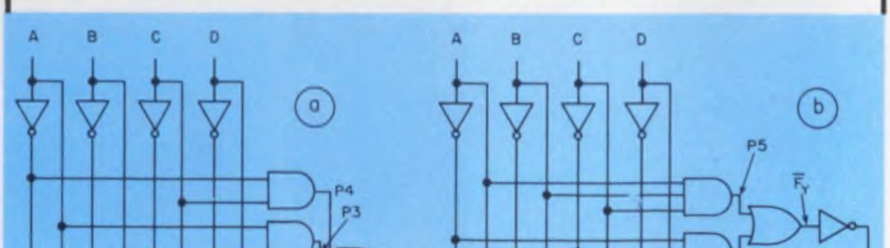
Mask programmable arrays, as the name suggests, use a predesigned overlay or mask as the final step in manufacture to form the desired connections.

Field programmable arrays, a more recent development, are manufactured with all their gates initially connected in all possible arrangements. The connections are made through Ni-Cr links, which may be selectively open-circuited (fused) by passing a high current through them. This capability allows the designer to achieve his desired logic synthesis.

Although both the PLA and the FPLA are programmable, they are not erasable. Once programmed, they cannot be changed. In practice, some changes can be made in an already programmed FPLA by blowing out still-intact links, but links, once open circuited, cannot be replaced.

A PLA needs only one power supply, in contrast to present-day μPs, which require anywhere from one to three. Current bipolar PLAs consume about 1/2 W. By contrast, a CMOS μP (RCA's 1802, for example) takes 30 to 40 mW. An MOS μP requires even more power, and a bipolar unit consumes the most.

Current manufacturers of PLAs and FPLAs include National Semiconductor, Monolithic Memories, Intersil, Signetics and Hughes.



4. **A simple PLA with only four inputs and one output** can still be configured to provide a large variety of logic functions. Two examples are shown above.

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CIRCLE NUMBER 23

call up another (new) PROM.

For example, if an item of information in location 39 in the PROM msut be changed, then the PLA is programmed to decode that particular location. Then, whenever the PLA senses that location 39 is wanted, it either provides new data or turns on another PROM.

"It's a way of preserving most of your original PROM by adding some patches," Birkner points out. "And if the PLA has terms left over, you can update your old PROM more than once."

Despite the large number of differences that separate the PLA and the μP, there is an area of similarity in the operation of both. Both may be programmed (but in different ways) to allow for design corrections or for future modifications.

The operation of the μP can be changed by changing its software —that is, by reprogramming its ROM. The older, mask-programmable array can be reprogrammed only by designing a new mask. The more recent FPLA is reprogrammed by burning out certain fusable links to form the desired logic pattern.

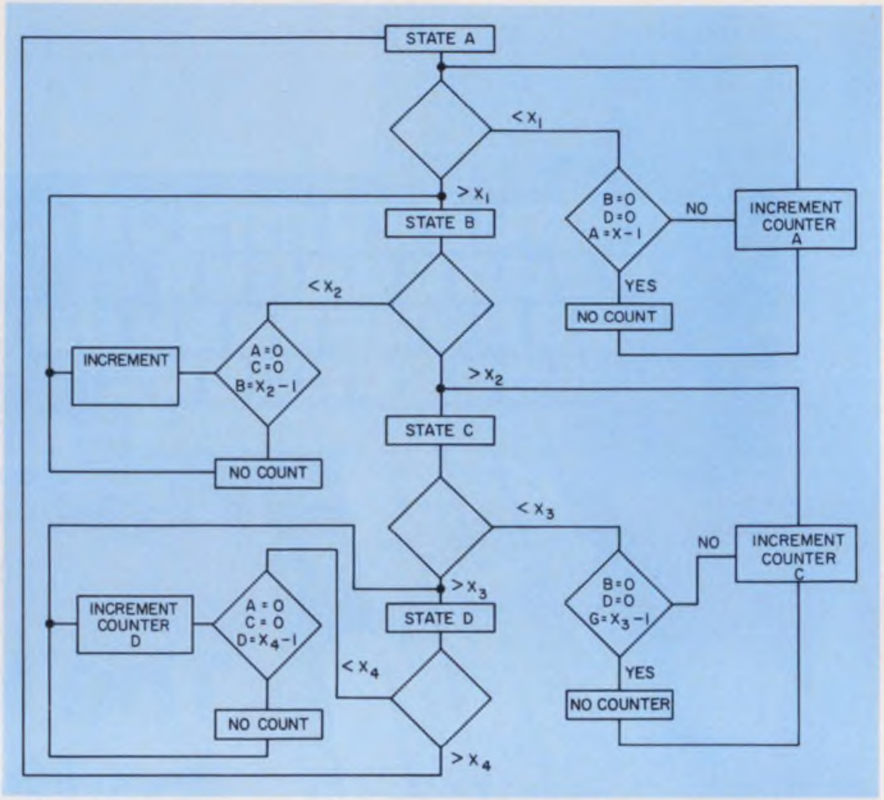
In designs where it is known that reprogramming will be necessary, it is usually the complexity of the design that will dictate whether a PLA or a μP offers the greater combination of advantages.

Although the PLA is basically a one-chip device, additional elements are often needed to realize a given design. Present-day μPs also generally require the combination of a number of chips of support circuitry to implement a particular application. The minimum number of such elements is two.

But μP designers are not sitting idly by, letting their chips pile up. One direction that μP design is heading, is toward combining the CPU with support circuitry, all on one element.

In the popular F-8 μP family, for example, the one-kilobyte Program Storage Unit (PSU) will be combined with the CPU, reports John Katsaros, marketing engineer at Fairchild Semiconductor, San Jose, CA. "This unit should be out next January," he says.

Reports indicate that Intel is also planning a similar chip, and the Texas Instruments TMS-1000



5. **The functions of the traffic controller** are shown in this state diagram. The controller checks all the other states to obtain the correct timing interval for the present state.

unit has been available for some time.

A peek at the crystal ball

What about the future?

Activity in the μP market is well publicized these days, with the latest efforts of manufacturers aimed at squeezing as much capability as possible onto one chip. This trend would remove one of the large drawbacks to wider μP application, namely the need for support chips.

Although the drive to build cheaper, high-voltage (4 and 8-bit) μPs continues unabated, there is still a great amount of effort in the higher-priced 16-bit units.

In the world of PLAs, optimism is not universal throughout the industry. Today's FPLAs (which have largely replaced the older mask-PLAs) are not competitive either in price or in speed with existing small-scale integration (SSI) and medium-scale integration (MSI) technology.

For example, a popular MSI circuit, the Priority Encoder Model 74148 can be synthesized by an FPLA. But when relative cost and speeds are compared, today's FPLA comes out far behind.

The Model 74148 is a 16-pin package, while the larger FPLA comes with 24. Even more important, the PLA sells for $15 to $20, while the MSI unit is now down to about 50 cents. Further, the MSI introduces a delay (input to output) of only about 20 ns as compared to 50 to 100 ns for the FPLA.

Unfavorable comparisons like these are providing incentives for improved designs by at least two FPLA manufacturers.

Easier use and speeds faster than 50 ns are some of the goals planned for tomorrow's FPLAs at Monolithic Memories. Lower prices are in the offing, too.

And at National Semiconductor, although engineers are reluctant to discuss their next-generation FPLAs, it's clear they will contain logic elements even more complex than today's versions.

"Tomorrow's FPLAs will attack the Model 7400 SSI and MSI market," says John Birkner of MMI. When these latest designs go on the market, the attack should become an exciting battle. ■■

Prototype optical telephone link being tested by Bell Laboratories

Circuit board containing experimental optical communications transmitter is removed from equipment bay. The lower black box contains the laser source; the upper box holds the control circuitry for the laser.

Successful six-month field tests of a prototype fiberoptic telephone link appear to have brought light-wave communications closer to practical use.

"This experiment represents a major step in preparing optical communications systems for metropolitan use," according to a spokesman for the Bell Laboratories-Western Electric facility in Atlanta, GA, the test site.

In the experimental system, each lightguide (containing 12 optical fibers) is connected at one end to a transmitter module that contains a double-hetero-junction gallium-aluminum-arsenide laser diode.

The module includes a laser modulator circuit that provides a 44.7 Mb/s transmission rate. Also included is a feedback circuit that compensates for temperature variations.

The other end of the light-guide is connected to a receiver module containing a silicon avalanche photodetector and signal-processing circuitry that converts the light pulses back to electrical signals.

The fiber lightguides are enclosed in a 2100-ft cable installed in ducts and manholes adjacent to the Atlanta laboratories. Some of the fibers are joined at their ends to form transmission paths up to several miles long.

50,000 calls possible

The half-in. diameter cable contains 144 lightguides and would be capable of carrying nearly 50,000 telephone calls. Each pair of lightguides can carry the equivalent of 672 telephone calls simultaneously for about four miles before optical repeaters are required.

The laser diodes transmitted at 0.82 microns to produce an average of 0.5 mW into the fiber lightguide units.

Glass rods are pulled into hair-thin fiber lightguides at Western Electric's Atlanta Works.

Average signal loss in the fibers —as measured in the experimental system after cabling and installation in ducts—is six decibels per kilometer (or ten dB/mile).

During the test a number of new system techniques and components were evaluated. These include a mass splice that permits simultaneous joining of all 144 fibers in a cable with no handling of individual fibers.

The first Bell System applications for such optical communications links are likely to be in carrying information digitally between telephone central offices in metropolitan areas. In such areas, space in underground cable ducts is limited and digital transmission is already used extensively. Also, distances between adjacent central offices in many cases are four miles or less; therefore, optical communications systems might not require repeaters to boost signals along a typical route.

Experiments with the system are scheduled to be continued until 1977, according to a Bell Labs spokesman. Commercial use, however, will depend on demand and cost factors, he notes. ■■

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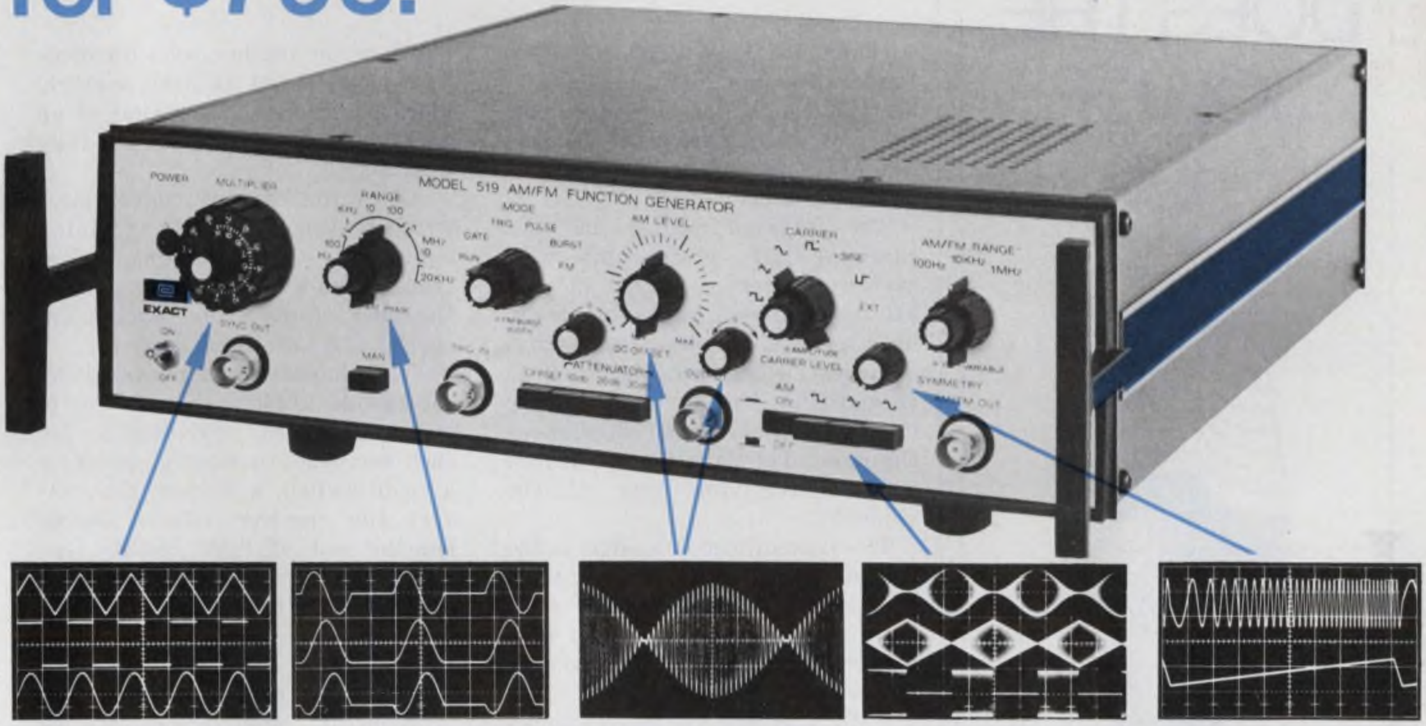

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INTERNAL AM/FM SOURCE. The AM/FM generator can be used to frequency modulate, sweep, gate, trigger or amplitude modulate the carrier generator. It can also be used to amplitude modulate an external carrier. Percent of modulation is adjustable from 0% through 100% on to double sideband suppressed carrier.

TRIGGER/GATE (Internal and External). The carrier generator can be triggered (single cycle) or gated (burst or cycles) manually or with an external signal when GATE or TRIG mode is selected. The AM FM generator is internally connected to the carrier generator to perform the gate and trigger functions when BURST or PULSE modes are selected.

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COMPACT. The Model 519 measures 30.5 cm wide x 8.9 cm high x 37.5 cm deep and weighs 5.22 kg. A rackmount option allows the 519 to be mounted in a 3.5 inch high standard 19 inch RETMA rack.

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CIRCLE NUMBER 25

Speech/hearing aid uses infrared light transmitter

Using infrared light waves to transmit audio signals, engineers at Siemens AG in Germany have come up with a new speech/hearing training system for hard of hearing children.

The infrared trainer has two channels—left and right—with carrier frequencies of 200 and 280 kHz respectively. Audio signals are used to modulate these carrier frequencies, which are then fed to IR-emitting diodes that radiate the coded light signal throughout the room. They are then picked up by the receiving sets of the students.

The transmitter is located at the teacher's desk and the signal is transmitted by cable to four radiators that are located in the four corners of the room. Each radiator contains 12 IR-emitting diodes.

With this system the transmitter's input power is 10 W. Only about 5% of this, or 500 mW, is converted to a useful optical signal. This value is far lower than the natural infrared radiation in open air, and thus is not harmful to the pupils or the teacher, says Siemens. The power level is high enough, however, to allow classrooms of up to 80 square meters to be fully illuminated.

As in the case of conventional wireless speech/hearing training equipment—where information is transmitted via a loop installed in the floor of the room—each pupil carries a headset and receiver.

Two channels are provided by the system to allow the receiver to be programmed individually for each ear. And, by simply operating a small switch, a student can convert the receiver into a stereo hearing aid of high quality, enabling pupils to communicate with each other in the school yard during breaks.

The 80-kHz spacing between the two channels permits high-fidelity reproduction of sounds in the 50 Hz to 15,000-Hz range. A big advantage of the infrared approach is that the radiation is absorbed by walls and doors, and interference between adjacent rooms is impossible.

Infrared speech/hearing aids enable hard-of-hearing students to converse with one another. A built-in optical system provides optimum reception.

NEWS

Micros help automate weather sensing for U.S. Air Force

Microcomputers will work alongside Air Force observers later this year to demonstrate automated techniques for airfield operation weather support. The micro-based climate monitor, known as the Modular Automated Weather System (MAWS), is expected to handle most of the observing and short-range forecasting chores of a base weather station without manual intervention. And, weather data will be processed faster, in greater detail and for a lower cost than is presently being done, says Capt. William R. Tahnk of the Air Force Geophysical Laboratory's Meteorology Division.

The heart of this "hands off" system, notes Tahnk, consists of five Intel 8080 microprocessors so configured that inputs and outputs of the system are greatly speeded up. Memory-mapped I/O is used where I/O devices are treated as memory locations, Tahnk explains.

Already existing transducers will be used to input data such as temperature, dewpoint, wind velocity, wind direction.

In addition, Air Force scientists are planning to install some advanced instrumentation of their own to feed data to the automated weather station. Forward scatter meters for visibility readings as well as automatic rain gauges, temperature/dewpoint and wind sets are among the devices to be included.

A big advantage of the micro-controlled weather monitor, says Tahnk, is that a tremendous increase in the number of samplings will be possible. Air Force observers presently are restricted to only a few observations hourly. With the automated system, however, several hundred wind measurements per minute will be possible. The field sensors will be wired into processors that are tied together by data links.

In operation, each processor instantaneously gathers raw data, converts them to meteorological variables and either stores the data or digitally transmits them to a supervisory control unit. ■■

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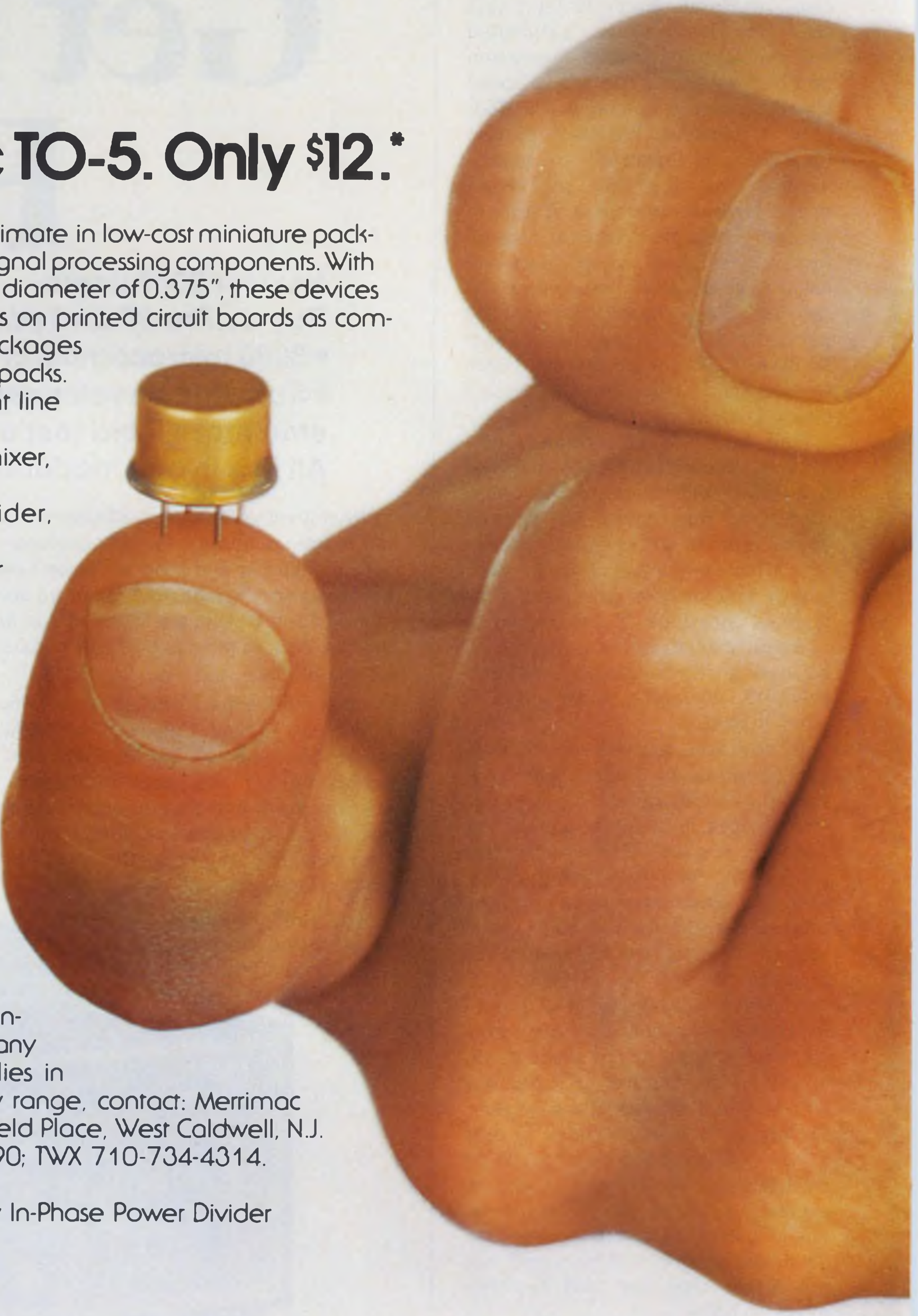

The Merrimac TO-5 is the ultimate in low-cost miniature packaging for a wide range of RF/IF signal processing components. With a height of only 0.3" and a base diameter of 0.375", these devices provide significant space savings on printed circuit boards as compared with other popular packages such as relay headers and flat packs.

Merrimac's TO-5 component line includes:

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- P-111 two-way 0/180° power divider, 5-300 MHz.
- P-112 three-way power divider, 1-200 MHz.
- C-114 10 db directional coupler, 5-500 MHz.
- C-115 20 db directional coupler, 5-500 MHz.
- Q-116 quadrature (90°) coupler, 30 MHz.
- H-118 hybrid junction, 5-300 MHz (0.5" height)

Merrimac can also supply these and other RF/IF components in relay headers and flat packs at low costs.

For complete information, including technical literature on any of these signal processing families in the 20 KHz to 2 GHz frequency range, contact: Merrimac Industries, Incorporated, 41 Fairfield Place, West Caldwell, N.J. 07006; telephone 201-228-3890; TWX 710-734-4314.

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CIRCLE NUMBER 30

Washington Report

New laser material offered by Air Force

The Air Force is offering to lend samples of a new laser material to other government agencies and contractors for studies of improved Q-switched laser operations.

The material is anisotropic yttrium aluminate doped with neodymium (Nd:Yalo$_3$) and was produced for the Air Force Materials Laboratory by Lamda-Airtron division of Litton Industries. It is considered a potential replacement for neodymium-doped yttrium aluminum garnet in solid-state lasers because it shows smaller thermal losses, doesn't require an external component to polarize the laser light and provides increased energy storage for Q-switched operations.

Potential applications include linearly polarized CW-pumped lasers for second harmonic generation or parametric oscillators, flash-pumped lasers and very efficient, flash-pumped, Q-switched lasers for aircraft and satellites. Lamda-Airtron has manufactured 40 rads of Nd: Yalo$_3$, the longest being four inches, at its plant at Morris Plains, N.J. The rods were tested by International Laser Systems, Orlando, FL.

Uniform Federal procurement policies due

Shortly after the new Federal fiscal year begins Oct. 1 all government agencies should be operating under a uniform procurement system for their major purchases.

The effort is under the direction of Hugh Witt, head of the Office of Federal Procurement Policy within the White House. With support from such industry groups as the Electronic Industries Assn. and the Aerospace Industries Assn., Witt put out a directive April 7 calling for all agencies to standardize their procurement policies by Oct. 5.

The basic points in the directive are that all agencies will designate a single person to be in charge of procurement and that uniform regulations will be adopted to reduce confusion by companies that deal with more than one agency.

Also as part of the drive toward improving government purchasing practices 17 of the largest agencies agreed to establish a new Federal Procurement Institute. Witt is chairman of the institute's 20-member policy board, which held its first meeting Aug. 12. Purpose of the institute is to train the more than 80,000 Federal employees involved in all phases of procurement.

New Electronics business in German-American tank

The U.S. electronics industry stands to gain from the decision by American and West German armies to standardize components used in a new tank.

The original plan had been to select a single tank based on two rounds of competition—first between the Chrysler and General Motors prototypes in the U.S. XM-1 program and later between the winner of that program and the German Leopard II tank. The winning firm would produce more than 3000 tanks at a total cost of around $5 billion.

The Germans protested that they couldn't expect a fair test of their tank in competition conducted under U.S. ground rules, and the General Accounting Office agreed. A compromise was struck under which each country would be responsible for certain items in a "hybrid" tank representing the best technologies of both countries.

This should give the U.S. electronics industry an edge since it has the more advanced fire-control systems, computers and sensors. Hughes Aircraft Co., for example, already supplies the fire-control system to the German Leopard family of tanks and is on the Chrysler subcontractor team. General Motors uses a fire-control system from its own Delco division on its XM-1 prototype.

Under an agreement signed between the two countries on Aug. 3, the U.S. will also supply all the forward-looking infrared (FLIR) night-vision devices to the new tanks of both countries. In return the U.S. agreed to give up its 105-mm gun.

Air Force, Navy agree on new aircraft jammers

The Air Force and Navy have agreed on a common electronic-warfare system, to be known as the dual mode adaptive self-projection jammer (ASPJ), for the next generation of fighter aircraft.

Among the aircraft that may use the ASPJ are the two new air-combat fighters, the Air Force F-16 and Navy F-18, and the advanced tactical fighter under study by the Air Force as a possible successor to the F-111.

Naval Aviation Facility, Indianapolis (NAFI) is managing the development phase of the program for both services and has awarded initial study contracts to ITT Avionics, Kuras-Alterman, Northrop (Hallicrafters), Raytheon and Sanders Associates. This fall one or more of these firms will be selected to do further development.

Basic purpose of the program is to equip fighters with improved jammers to make them less vulnerable to enemy radars, such as those used by the Soviets at their surface-to-air missile (SAM) sites. Inability to jam enemy SAM radars caused severe loss of U.S. aircraft in Vietnam.

In a parallel effort the Air Force has awarded a $3.9-million contract to Kuras-Alterman to improve the jamming capability of the EF-111A. That aircraft is intended to accompany U.S. fighters to their targets. The improved jammer, known as the Advanced Power Management System (APMS), may also be used in the Air Force F-15 fighter.

Capital Capsules: Under Air Force sponsorship, Questron Corp., of El Segundo, CA, is **studying ways to make microprocessors less vulnerable to nuclear radiation. . . . President Ford has nominated Dr. H. Guyford Stever to be his science advisor** despite opposition from conservative Republican senators. . . . **The Air Force and NASA are planning a new hypersonic aircraft capable of speeds up to mach 8 at a cost of $200 million.** . . .The Naval Research Laboratory has **successfully flight-tested a passive microwave radiometric sensing system for potential meteorological applications.**

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CIRCLE NUMBER 33

CIRCLE NUMBER 34

Wescon '76

A silver anniversary

In celebrating its 25th (silver) anniversary, this year's Western Electronic Show and Convention will be the largest since 1970—in terms of exhibitors, exhibits and anticipated attendance.

Some 30,000 to 35,000 visitors are expected to flock to the Los Angeles Convention Center September 14-17, to attend the 35 technical sessions and to visit the 725 booths which represent 400 companies.

This is the fourth consecutive "sellout" of exhibit space, a Wescon spokesman notes—about one-third larger than last year's Wescon at Brooks Hall in San Francisco.

Although the accent in the technical program is, once again, on the technology and applications of microcomputers and microprocessors, the sessions are quite diversified. Topics to be covered include: "The Engineer after 40," "The Electron and the Mind," "Optical-Fiber Communication," "Needs and Trends in Medical Electronics—1976," and "Surface Acoustic Wave Devices."

Among the more important technical papers are those in Session 23, which will focus on a selected cross-section of future technological developments in LSI. Papers will provide an overview on large-scale CCD memories, bipolar RAMs and low-power injection-logic devices.

Beyond the conventional assemblers, compilers

and still going strong

and development systems there are a number of new "tools" to aid the microprocessor user and designer. For example, a paper in Session 31, "Microprocessor Tools and Techniques," will answer the question: "When is it better to design a microcomputer using a set of chips than to buy a μC on a board?

Several domestic satellite communications systems are about to go into service around the world. Session 9 will describe such systems as the new Indonesian PALAPA; ANIK B, the latest addition to the Canadian satellite network; and the United States COMSTAR, a system for distributing television programs over the entire United States via satellite.

Session 29 on millimeter-wave technology will discuss the obvious features and peculiarities of a portion of the electromagnetic spectrum (30 to 300 GHz) that is drawing increased interest.

One of the hottest areas in instrumentation, the testing of microprocessors and μP-based systems, will be the subject of Session 17. Session 12 will cover the new IEEE interface bus.

The following editors contributed to this Wescon special report: Jules Gilder, Sam Derman, David Kaye and Jim McDermott.

The distinction between minis and micros continues to narrow

With the development of 8 and 16-bit microcomputers on a board, the distinction between minicomputers and microcomputers is vanishing fast. In some applications the choice between the two is obvious. But in others, hardware and software problems exist that will be explored in detail in Wescon Session 31.

Basic distinctions between the micros and the minis will be made by Ed Zanders, Data General, microNova product manager, in his Session 31 paper, "The Capabilities of Micros and Minis."

Microcomputers are designed for data-handling and I/O applications that require little in the way of high-performance or computational requirements, Zanders will say. Examples include the 8-bit microcomputers used in simple, low-cost data terminals, peripheral controllers or data communications equipment. Most of these applications use 8-k memories.

"We're finding that the 16-bit microcomputer is useful in traditional computer applications where large computational power is needed, such as for real-time use in instrumentation systems. Memories of 32 k are typical there, and high-level languages are the rule rather than the exception."

The packaging flexibility of a compatible microprocessor family, like the microNova, permits a relatively easy change in the level of processor or computer needed.

The big choice—chips or boards?

Zanders sees the scheduled OEM users of computers as using both micros and minis. Here, the important factor will be compatibility between the software and the I/O hardware for both systems. With compatible features like these the OEM will be able to put more of his design time into end-product features, where his expertise better applies.

For example, with full compatibility, the designer may start with a microcomputer on a board. He can later integrate downwards and increase his added value by replacing boards with chips, according to Zanders.

Or if the OEM's future needs call for expanded processing power, he can design software for his micro around a mini that later on can run the software already developed for the microcomputer.

When is it better to design a microcomputer using a set of chips than to buy a microcomputer on a board? That question will be answered in a Session 31 paper, "Packing Capabilities into Microcomputers and Minis," by George Adams of Intel.

Using a representative microcomputer design as an example Adams, product manager of the Santa Clara, CA firm, estimates that for OEM applications requiring from 10 to 500 or 600 systems per year, the board-level microcomputer has definite cost advantages to the designer. Beyond the 500 to 600-unit level, the use of component μPs offers savings for an OEM—provided he has the expertise and manpower to design, test and debug and generate the software for his system.

If the OEM doesn't have this talent, Adams believes the best course is to select an off-the-shelf microcomputer on a board. Then the OEM's engineers have the option of designing several systems using board-level components, in the same time as it would take to produce a single system of IC chips.

A major factor in the success or failure of a microcomputer design is software, and since hardware prices are currently decreasing, microcomputer software development costs are becoming a greater proportion of a user's over-all investment. That's what Duane Dickhut, engineering supervisor, Digital Equipment Corp., will emphasize in his Session 31 paper, "Evaluating Mini vs Microcomputer Software Development Tools."

To match the attractive hardware prices, microcomputer software development tools should retain the properties of minicomputer software, including flexibility and ease of use, according to Dickhut. But he will note also that micro development tools ought to offer a better price-performance ratio than do minis.

Get hands-on use of software

A prime recommendation by Dickhut will be to get some hands-on experience with each software development system that the user wants to buy. Go through the normal program-development loop of editing, assembling, linking and debugging—several times—with a test program to see how well the loop is human-engineered. See if the command constructions are consistent and logical.

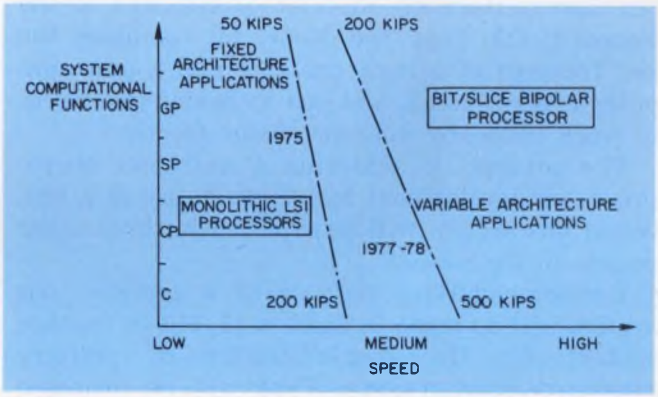
One of the key things that the assembler program should have is a macro facility, the capability of inventing new pseudo instructions, to make the program more useful in assembling instruction sets for μPs other than the ones for which the program was originally designed.

An example of a good macro facility is found in the MACRO-11 assembler under Digital Equipment's RT-11 operating system for the LSI-11-based PDP-11V03 microcomputer software/hardware development system, according to Dickhut.

Because of the growing proliferation of microprocessors, it is likely that more than one type will be used. As a result, Dickhut will suggest, a powerful software and development system should be chosen at the start so you can avoid the need to buy a development system for each μP.

Training the programmer will cost less because he only has to learn that one system. Although programming time will be spent developing a set of macros for each different microcomputer, the cost is relatively low compared to comparable minis and large scale machines because microcomputer instruction set and architecture are relatively simple.

Microprocessors were originally developed a few years ago for logic processing in controllers, not for data processing as in larger computers. Today most μPs are being designed and patterned after minicomputers—which do data processing—even though the μPs are primarily used for other purposes. This situation will be described by Matt Biewer, vice president of engineering for Pro-Log Corp., Monterey, CA in his paper, "Should You Use a Microcomputer to Replace Hard-wired Logic?" Biewer will explain why he sees the logic-processing area neglected, with logic-processing design penalties as the result.



Differences in instruction speeds separate fixed and variable microprocessor architectures. The Navy sees increased use of bit-slices in the next two years.

The architecture of early microprocessors like the Intel 4004 and 4040 and Rockwell's PPS-4, were better for control than the architecture of today's 8080 and 6800, Biewer insists. These early μPs had features like an internal stack plus a number of internal registers.

But with the 8080 the architecture is designed to manipulate memory, which is a data-processing function. This was accomplished by moving the 8080 stack out into the memory. Although it is easy to manipulate the external stack it becomes expensive in terms of the amount of time and the number of data cycles needed to get the data in and out of memory. Operations on internal registers, on the other hand, are rather quick and usually take one-word rather than multiple-word instructions.

The trend is reversed

But the trend to data-processing architectures, Biewer believes, is being reversed in some of the newer μPs now under development or being produced. One of these is Electronic Arrays' 9002, which was designed, with Pro-Log's advice, to include features like internal scratch-pad RAMs, internal registers and internal stacks. Although the 9002 chip is complicated it requires fewer external chips to support it than are required by competitive devices.

To solve the problems of multifamily microprocessor users, new universal design aids, development systems and debugging tools are beginning to emerge—components that can be used with most present and anticipated microprocessor systems. Examples of new or proposed approaches to universal microprocessor analysis and development systems will be featured in Session 16, "Universal Microprocessor Design Aids."

The newest hardware will be described in a Session 16 paper and demonstrated after the meeting. It will be Systron-Donner's Model 50 Microprocessor Analyzer. According to Dr. Zoltan Tarczy-Hornoch, director of research of the Concord, CA firm, the Model 50 combines the key features of a logic analyzer and a minicomputer control panel, and has sufficient generality to work with any microprocessor family.

The concept of achieving a universal microprocessor development tool through use of a universal bus system will be explored in three other papers in the session.

Recommendations for use of a common bus system will be made in Session 11, but in another context—for the standardization of military microprocessor systems. That will be proposed in a Session 11 paper, "Compatibility Among Families of μPs", by Hank Molloy, military program manager, Intel Corp. Molloy is also chairman of a newly organized task force on military microcomputer LSI, which is sponsored by the Electronic Industries Associates and the National Electronic Manufacturers Association.

To achieve any kind of standardization it is essential that bus structure characteristics be specified, Molloy will argue. Also, high-order languages will have to be used.

An example of how such languages can contribute to standardization, Molloy will point to Intel's PL/M. Two popular 8-bit μPs are the Intel 8080 and Motorola's 6800. While PL/M was generated by Intel for the 8080, PL/M compilers are available to translate the syntax into object code for the 6800.

The EIA/NEMA task force will study drafts of two new MIL-M-3851 microprocessor detail specs, the /400 for Motorola's 6800 and the /420 for Intel's 8080.

Results of Navy study

The Navy has been actively developing its own requirements for standardization. Its conclusions, reached after a six-month study of Navy microprocessor and microcomputer requirements, provide valuable advice for any designer seeking to standardize his harware choices.

Recommendations from the study will be presented in a Session 11 paper, "An Approach to Microprocessor/Microcomputer Standardization in Navy Systems", by Ralph Martinez and Reeve Peterson, Naval Electronics Laboratory Center, San Diego, CA.

Navy categorizes μP/μC systems

"We looked at 50 Navy systems including both nonmicroprocessor and microprocessor types," Martin says, "and were able to categorize most of the systems in terms of four degrees of functional complexity." These categories, which will be described in detail, include:

- General-purpose computation, such as data and message processing, and multitask efforts.
- Signal processing for real-time data acquisition and signal analysis.
- Dedicated processing such as in data formatting and display, and data acquisition and storage.
- Controllers for memory, I/O and instrumentation.

A fifth category included systems that have special requirements such as being able to withstand the full Military-Standard temperature range of −55 to 125 C, being capable of operating with very low input power, having speeds greater than 2-M instructions per second, and being capable of withstanding a radiation environment.

The Navy systems were compared on the basis of another important factor—speed, in terms of instructions executed per second (see figure).

Other special-system requirements that the paper will discuss include:

A high-order programming language.
Floating-point arithmetic hardware.
Direct memory access.
Integer multiply/divide hardware.
Vectored interrupts.
Microprogrammability.

All of the data from the study were correlated with the characteristics of μPs to determine which ones could satisfy which Navy processing requirements.

As a result of the study one principal recommendation is to immediately adapt an 8-bit CPU as an interim standard. This recommendation is made possible because 8-bit technology has matured enough that μPs able to meet existing and near-term requirements are already available, along with the necessary hardware and software support.

It was decided, however, that at this time the technology is not adequately developed to specify a standard for 16-bit or a bit-slice CPU.

Any one of several commercially available 8-bit CPUs, militarized and procured to Navy specs would be satisfactory for the 8-bit interim standard to be discussed in the paper. Here is the compatible family of building blocks that is required to support such a CPU, listed in the order of standardization priority:

CPU support
ROM/RAM memory
UART/USRT
Programmable ROM
Erasable PROM
Programmable parallel I/O interface
Programmable interval timer
Programmable interrupt controller
Programmable DMA controller
Multiply/divide unit

For packaging standardization it is recommended that the 8-bit μP or μC module set be designed and fabricated as part of the Navy Standard Electronic Module Program. The basic unit would be a PC card of 80 pins with an area of about 156 cm^2.

Details of other related requirements, such as hardware and software support programs, a standard instruction set, and proposed schedule of standards implementation will also be described in the paper. ■■

Semiconductors

Progress seen in CCD memories, bipolar RAMs and I²L logic

A peek into the future by semiconductor industry experts will be offered in Session 23, "Future LSI Technologies." Some of the advances to be predicted in this session are:

- 256-kilobit CCD memories that will be available in slightly more than 3 years.
- 16-kilobit bipolar RAMs that have a 100 ns access time.
- Low-power injection-logic devices that operate at higher speeds than Schottky counterparts.
- Rf LSI linear circuits that operate in the 500 MHz to 2 GHz region.

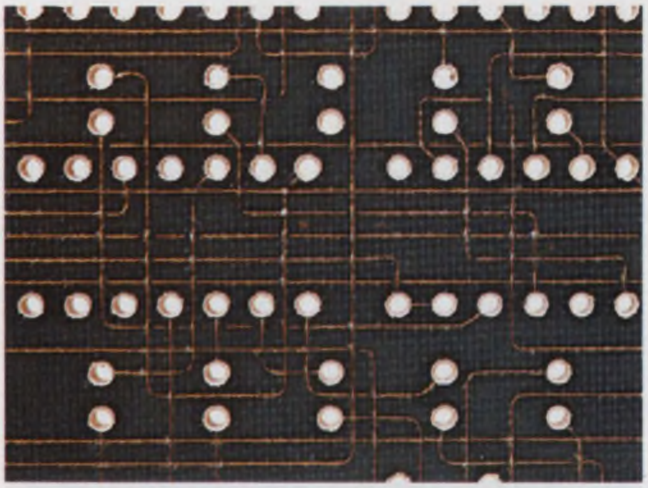
A 64-k CCD memory chip will be described in the first paper of the session, "CCD Large Scale Memory," by Robert Bower, president of Mnemonics, Cupertino, CA. Bower shows how modifying the basic design will make it possible to produce a 256-k chip.

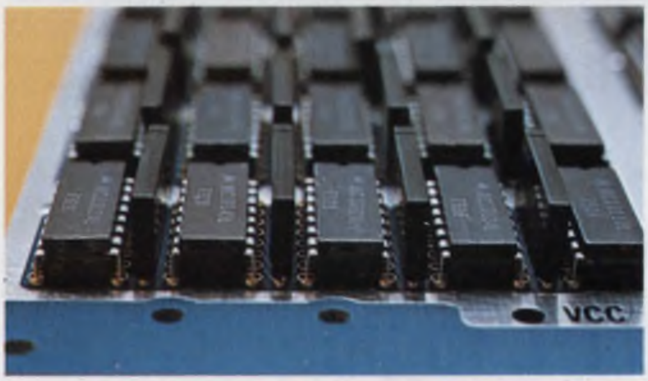
Ignoring the 64-k chips that both Intel and Fairchild are working on, Bower makes an "apples and oranges" comparison of the Mnemonics memory with currently available 16-k CCDs. He points out that his 64-k device is on a 218 by 235-mil chip and results in an area per cell of only 0.785 sq mils/bit, while the Intel 16-k has a cell area of 2.1 sq mils/bit and the Fairchild 16-k has a cell area of 2.7 sq mils/bit.

Further, the power consumed by his device at 1 MHz is only 0.5 μW/bit while the Intel and Fairchild memories require 9 μW/bit and 2.4 μW/bit, respectively. The big difference in power dissipation is caused by the different applications for which the CCD memories are designed. The 64-k chip is designed for slow-access applications in the millisecond range, and the smaller 16-k units are intended for use where 100 to 200-μs devices are needed.

The design of the Mnemonics chip is based on very conservative design rules and uses 8-μ lines and spaces. The high density is achieved by using a 2-phase offset-gate structure and a serial-parallel-serial configuration.

If a 128-k CCD memory is desired, says Bower, design tricks such as serial interlacing and electrode-per-bit structures can be used to double the density of the 64-k chip. A further doubling of memory density is possible by using multilevel encoding. In particular, the CCD is used as an analog memory that can store four amplitude levels of information. When converted by an analog-to-digital converter, the four amplitude levels result in 2 digital bits. Thus each CCD





High-speed logic-interconnection panels such as the Multiwire from Photocircuits (top) and the wrapped wire from Augat (bottom) will be discussed in Session 25. Multiwire is a good choice when constant impedance is necessary; wrapped wire is appropriate when flexibility is important.

cell can be used to store two bits instead of one bit, as is usually the case. By using the multilevel encoding scheme with the 128-k chip, a 256-k CCD memory will be possible. Bower says the industry should be sampling these large-memory devices by 1980.

16-k bipolar RAMs are possible

By using a very large scale integration (VLSI) technique it is also possible to build 16-k bipolar RAMs that have an access time of 100 ns, according to Barry Dunbridge, chairman of the session and an engineer with TRW's Systems Group in Redondo Beach, CA. In a TRW paper, "VLSI Bipolar Technology," advances in bipolar density will be discussed. The largest bipolar RAMs in commercial production today are 1-k devices, and 4-k units are now being sampled, he notes.

TRW is not contemplating going into the memory manufacturing business, Dunbridge says, even though 1-cm square bipolar chips can now be produced that contain as many as 100,000 devices. TRW will apply this technology to a 16-bit multiplier and a 128-bit shift register instead.

To achieve its high densities, TRW reduces the cell geometry by using 2 micron lines and employing current-mode logic, a modified form of ECL. The result is a high-density bipolar device that can operate at 100 MHz with a power-delay product of only 2-5 picojoules.

I^2L aiming at Schottky applications

Although it has only been out on the commercial marketplace for a short time, integrated-injection logic (I^2L) is already being considered as a low-power alternative to Schottky TTL logic.

A report on how I^2L is making inroads into Schottky territory will be given by Donald Romeo, an engineer at Northrop's Research and Technology Center, Hawthorne, CA, in his paper, "I^2L/LSI for Complex Logic Arrays."

Romeo will point out that in certain applications—such as ring oscillators—I^2L already outperforms Schottky, while other logic structures still require improvement before they become competitive. But the potential for I^2L is very good because it does not use resistors (as other bipolar approaches do) and thus makes it possible to increase density and speed by simply reducing line widths. That process is much harder to perform in a resistor-containing device because if the line width is changed so is the resistance.

Romeo will describe a test chip that was fabricated for the U.S. Army Electronics Command at Ft. Monmouth, NJ. The chip is 170 mils on a side and contains four 2-bit counters, two 32-bit shift registers and several ring oscillators with different layout parameters. The variety of oscillators is used to determine the dependence of speed on layout parameters.

The ring oscillators have a gate delay of 6 ns, which is comparable to that of a Schottky. The counters have a gate delay of about 10 ns, slightly longer than the delay of Schottky devices.

The performance of I^2L devices can be easily improved, Romeo will point out. One of the limitations of I^2L at present is the amount of charge stored in the emitter-base junction of the npn transistor. It takes a certain amount of time to supply that charge when the base is pulling up, and a certain amount of time to remove that charge when the base goes into cutoff. As a result, even moderate improvements in lithography —a factor of two decrease in line width, for example—will cause a factor of four decrease in area. These lithography improvements can be achieved by using X-rays and electron beams.

Because charge is proportional to the volume underneath the area, there will be a factor of four reduction in charge storage and almost a four-times increase in speed.

An oxide aligned transistor (OAT) technology that can be used to produce linear integrated circuits that operate in the 500-MHz to 2-GHz region will be discussed in this session's final paper, "Rf Goes LSI" by David R. Breuer of TRW Defense and Space Systems Group.

The OAT technology is similar to Fairchild's Isoplanar, and has already been used to produce 500-MHz phase-locked loop and a 2-GHz analog multiplier. Breuer will point out that ICs made with OAT technology can be used in the oscillator, preamp, amplifier and phase-locked-loop sections of communications receivers that replace discrete components now in use. Commercial availability of rf LSI devices will probably take another three years, mainly because there is no big market for them. ■■

Communications

More nations scheduled to receive own domestic satellite systems

On July 8th, a new communications satellite was launched into synchronous orbit, and with that event, Indonesia became the third member of an exclusive club—a group of nations that each possess their own domestic satellite communications network.

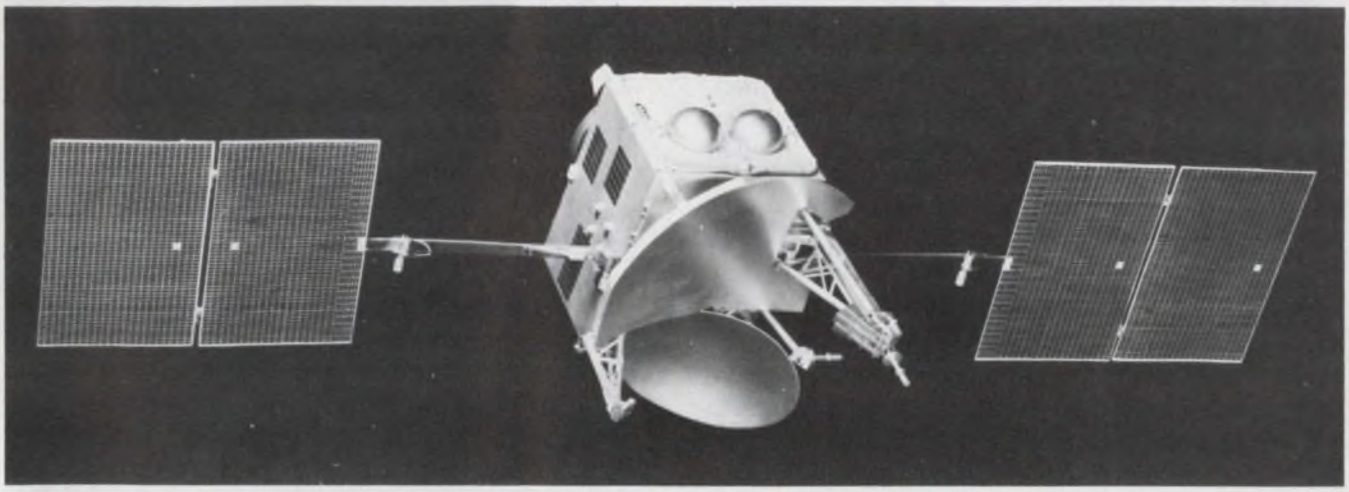
Built by Hughes Communications International, a subsidiary of Hughes Aircraft Co., El Segundo, CA, the Indonesian satellite is one of a growing number of similar national communications systems scheduled to go into service in the next two years.

Domestic communications satellite systems such as the new Indonesian PALAPA (a name signifying national unity) will be the subject of Session 9, "Near-Term Satellite Communications Systems."

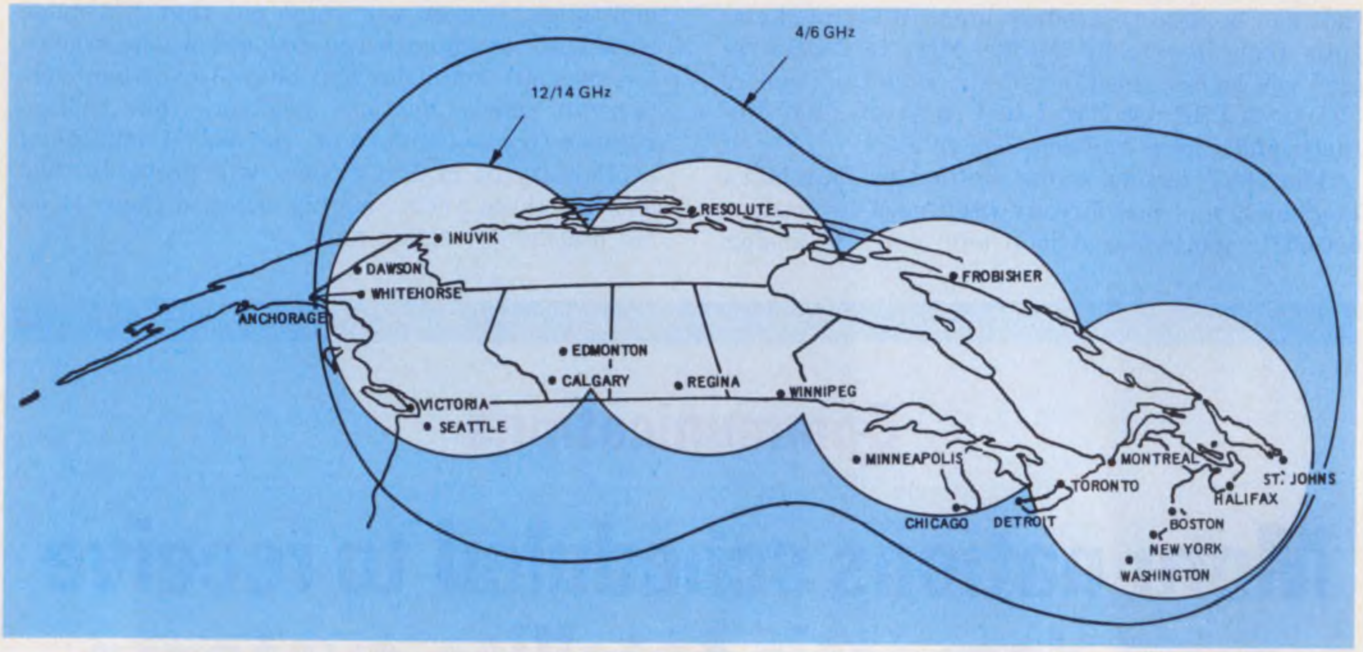
Among the other systems to be described at the session is ANIK B, the latest addition to the Canadian domestic satellite network. The United States domestic satellite COMSTAR, and a system for distributing television programs over the entire United States via satellite also will be described.

In another Wescon session, on such possible satellite uses as terrain mapping from space, the question, "Millimeter Wave Technology, Where Do We Stand, Where Do We Go?" will be debated.

Current and Future applications of millimeter waves for military as well as commercial inter-



1. **ANIK-B ,the new Canadian domestic satellite,** will operate in both the 4 to 6-GHz and the 12 to 14-GHz bands. It's scheduled for launch in early 1978. The satellite will be described in 9 session.



2. **Complete coverage of all provinces of Canada** is provided by the ANIK-B synchronous communications satellite. Coverage will include St. Johns, Newfoundland in the East, to beyond the Alaskan border.

ests will be examined in the light of present-day technology.

National networks

The Indonesian communications system grew out of a need to bring closer together that nation's 120 million people who are scattered over 5000 islands spanning more than 3000 miles of the South Pacific.

In addition to conventional heavy-route telephony between the main cities, a unique single-channel-per-carrier (SCPC) system is used to link 40 ground stations spread over the country's enormous area. Communications links can be set up between any two points as needed, all under the control of a central computer in the master control station in the capital, Jakarta.

Rather than have a frequency slot permanently assigned for service between cities A and B, in the Indonesian system, any two cities can be linked up via any available frequency. This method, the first for a domestic satellite system, saves on ground equipment and on number of needed frequencies.

These advantages will be discussed in a paper by Bruce Elbert and Charles Sanderson of Hughes Aircraft, El Segundo, CA.

Closer to home, Canada's ANIK B (Fig. 1), successor to that nation's first ANIK communications satellite, will provide increased coverage of the entire Canadian land area, stretching from St. Johns, Newfoundland in the East, to beyond the Alaskan border in the Northwest (Fig. 2).

The new satellite, scheduled for launch in early 1978, will transmit over the 4-6 and 12-14 GHz frequency ranges. Only the 4-6 GHz band was used in the earlier ANIK series. The new Canadian domestic satellite will be described in a paper by R. Hoedemaker of RCA-Astro Electronics Division, Princeton, NJ, the laboratory where the satellite was built.

Amid all this international satellite activity, the United States is embarking on a number of satellite programs of its own. Under a proposed new television distribution system, 165 Public Television stations located across the continental United States as well as in Alaska, Hawaii, Puerto Rico and the Virgin Islands, will gain access to Public TV programming via the existing WESTAR satellite.

The satellite-linked TV network, described by John Ball, director of engineering for Public Broadcasting Service, Washington, DC, will operate through a Master Origination ground terminal, 5 receive/transmit ground terminals, and approximately 145 receive-only stations.

Increased millimeter wave effort

A number of obvious features of millimeter waves make this portion of the electromagnetic spectrum (30 to 300 GHz) the subject of increased interest.

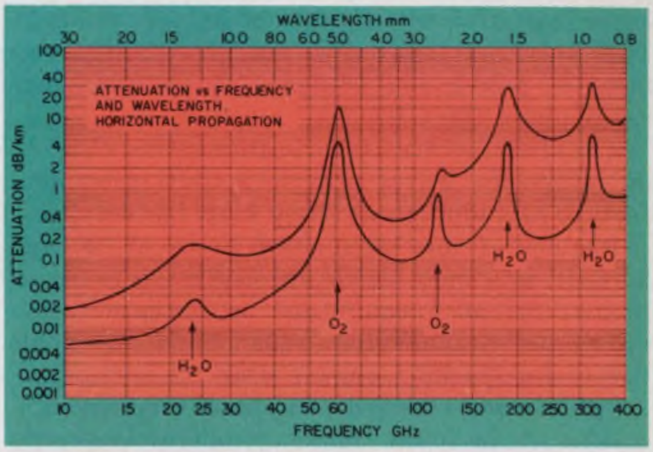
First, because of the very short wavelengths involved, millimeter-wave components can be built physically small, and the possibility exists of their being fabricated in the form of integrated circuits. "Millimeter Wave Circuits and Components," a paper by Egbert Maynard of the Naval Electronics Laboratory, San Diego, CA, will review developments in this frontier area.

"The primary thrust in millimeter-wave applications," Maynard reports, "will be broadband receivers for electronic warfare above 40 GHz, general-purpose and satcom in the 35-45 GHz range, and selected high-resolution radars (for example, low-angle trackers), in the 95 GHz and above region.

"Emphasis in component development should therefore be in broadband integrated low-noise receiver front ends, linear solid-state amplifiers at a 1 to 10-W level for TWT replacement, and high-power and duplexer elements at 95 GHz and above."

Other components, particularly the rapidly increasing variety of millimeter-wave transmission guides are described by Ashok Gorwara, a microwave consultant at Menlo Park, CA. Particularly promising with regards to ease of fabrication and compatibility with semiconductor devices, are slot line, image line, microstrip, and coplanar waveguide, to name just a few. Another structure, not as well known but displaying relatively low transmission loss, is fence guide, a modification of H-guide.

A second important feature of millimeter waves is the fact that antennas can be made small and yet provide adequate directivity. A well-known application is in missile guidance, but there are possibilities as well for automobile anti-



3. **Bands of high atmospheric attenuation** in the millimeter-wave domain permit secure short-range communications. Low-attenuation bands provide atmospheric windows for a variety of high-directivity radars.

collision radars and in radar-like devices to aid the blind.

Millimeter-wave sources to power these exotic radars will be the topic of Kenneth Weller of Hughes Aircraft Co., Torrance, CA. Such sources are well known by now, and include Impatt diodes, Gunn diodes, and gallium-arsenide FETs. Future work, he suggests, is in the direction of implemening these devices using newly develop-

Timetable to the technical sessions at WESCON '76

TUES. Sept. 14 10 AM	1. Microcomputer Applications	2. Mini Computer Power Supplies	3. Automated Microcircuit Interconnections Clinic	4. Active Microwave Systems for Space Applications	5. The Engineer After Forty (Panel)
TUES. Sept. 14 1:30 PM	6. Microprocessor Design Aids—The μP Manufacturer's Viewpoint	7. Pocket Calculator Update	8. ATE Hardware/Software Developments to Reduce Set-Up Costs	9. Near Term Satellite Communications Systems	10. Reliability Comparisons of Mfg. Process; Military and Commercial
WED. Sept. 15 10 AM	11. Microprocessor/Microcomputer Standardization in Industry & Government	12. Interfacing Microprocessor Instrumentation to the GPIB	13. Pattern Recognition Systems	14. Optical Fiber Communications, How, Why, When	15. The Electron and the Mind
WED. Sept. 15 1:30 PM	16. Universal Microprocessor Design Aids	17. Logic Analyzers: What Are They & Where Are They Going?	18. Graphic Display Information	19. Application of CTDs to Sampled Data Signal Process	20. Telecommunications for Civic and Social Services
THURS. Sept. 16 10 AM	21. Microcomputers for Fun and Profit	22. Needs and Trends in Medcial Electronics —1976	23. Future LSI Technologies	24. Surface Acoustic Wave Devices—Technology & Applications	25. High Speed Logic Interconnection Techniques
THURS. Sept. 16 1:30 PM	26. High Performance Building Blocks for Microprogrammed Systems	27. TV Games	28. Next Generation The LSI Computer System	29. Millimeter-Wave Technology: Where Do We Stand, Where Do We Go?	30. Professional Unions
FRI. Sept. 17 10 AM	31. Microprocessor Tools and Techniques	32. Single-Board Computers: The Emerging Micro vs. Mini Battle	33. Frequency and Time Control System	34. Automated Vehicle Location (AVL) Systems	35. ATE's Role in Field Service for Printed Circuit Boards

ed materials—indium phosphide for example. This particular substance can provide improvement in power and efficiency in the frequency range above 100 GHz.

The effects of atmospheric attenuation (Fig. 3) on millimeter waves provide a third prominent feature of radiation at these high frequencies.

Regions of low attenuation occur at 35, and 94 GHz, and these bands are beginning to be exploited for such equipment as fog-penetrating radar, terrain-mapping radar, and low-angle radars for tracking objects near the horizon.

The already-crowded conditions for communications in the lower-frequency microwave bands are also supplying incentive for increased effort in the "atmospheric window" of the millimeter-wave spectrum. Using circular waveguide as a transmission medium in the 40 to 110 GHz region, transmission of one-half million voice channels is possible over a single line. This is an increase by a factor of 1000 over the capability of present-day microwave links.

The regions of high attenuation are also under consideration as frequency bands for secure, short-range, point-to-point communication. Ship-to-ship communication is one such example. Communication between satellites is another. The possibility of eavesdropping by sensitive receivers on earth is eliminated by the ever-present attenuation of the earth's atmosphere.

Despite the wide variety of uses—projected as well as existing—for millimeter wave devices, the market is largely stagnant right now, according to Frederick Tischer, professor of electrical engineering at North Carolina State University, at Raleigh and chairman of the session.

"In the civilian sector there is some sort of lukewarm progress and also a lukewarm attitude towards progress," Tischer says. "The military are also sponsoring some work. But what we want to assess at this session is what can be done to make the progress more vigorous." Tischer believes most people shy away from developing new applications because presently available components are expensive. Likewise, because there are so few applications, the prices remain high.

A panel discussion occupying the second half of the millimeter-wave session will address itself specifically to this problem. ■■

Test and measurement

Action is in interfacing and testing μPs and microprocessor systems

The hottest area in instrumentation at the moment is the testing of microprocessors and systems that include the μP. At Wescon's Session 17, four new logic analyzers will be described—including the long-awaited logic state analyzer for μPs that Hewlett-Packard will be introducing at the show.

In general, much attention is focused on μPs—not only testing them and using them, but interfacing them, as well. For example, at Session 12 the new IEEE General Purpose Interface Bus will be considered in all of its ramifications. Much confusion surrounds the IEEE standard, and manufacturers are woefully inconsistent in the design of interfaces for connection to the bus.

HP's logic-state analyzer has the ability to solve three distinct types of problems, according to a paper by Tom Saponas and Jeff Smith of HP, Colorado Springs, CO. For one thing, they say, it will be possible to look at program flow and the I/O port simultaneously, for the first time. That will make it possible to relate problems on the interface line to program glitches.

It will also be possible for the first time to look at and record the information being written into and out of μP memory. Also, the analyzer will be able to capture transients. Other logic analyzers can do that already, but it will be a first for HP equipment.

An analysis of the uses and performance levels of current logic analyzers will be presented by Edward Jacklitch of Biomation, Cupertino, CA. He will note that some of the more useful features of current logic analyzers include: asynchronous recording at data rates of between 10 and 100 MHz; larger and larger memories; glitch catchers for transient analysis; timing-diagram displays; and "1," "0" data domain displays.

In the future it would be nice to be able to switch between timing-diagram and data-domain displays in the same instrument, Jacklitch says. He expects most future modifications will be oriented to specific μP-analysis, field-service and factory-floor applications.

In the area of μP analyzers, Jacklitch looks for ease of use, ability to talk to the user in hexadecimal notation and the ability to monitor data being written into—and read from—μP memory.

Put the μP in the logic analyzer

E-H Research Laboratories of Oakland, CA has put a μP into a logic analyzer and achieved some interesting performance features. Carver Hill will describe the new analyzer in his Session-17 paper.

"We can look for two parallel combinations of bit streams and trigger at a known point," he says. That allows the analyzer to search for a very well defined sequence of events and not start recording until that sequence shows up. Since the events in the sequence are user definable, you can also trigger on a combination of state sequences where one state is not there.

In addition, the instrument has a trigger delay that starts at a predetermined mark and then makes a decision about what to do when the delay expires. For example, a measurement might depend upon the time between two specific events. In that case, the first event triggers the delay and at the end of the delay the analyzer only starts recording if the second event has not yet occurred.

Other features that the μP adds are the ability to control the display and make it read certain pertinent data in a form desired by the user. The μP also can give the user visual cues to help in programming the instrument.

Murlan Kaufman of Tektronix in Beaverton, OR will describe how to pick a logic analyzer for your particular job. He'll discuss the hardware and software problems that can be solved with a logic analyzer that includes bus-oriented systems and random logic. He will show how designers can debug μPs, state machines and other computer-based systems. Even engineers in

An instrument that can be interfaced to the IEEE 488 General Purpose Interface Bus is the Dana 9000. This Microprocessing Timer/Counter contains a separate control panel for programming.

incoming inspection, manufacturing and electromechanical design will be shown how they can use logic analyzers to advantage.

Every paper in Session 17 will also discuss a new analyzer that the particular manufacturer represented is about to introduce.

Is the IEEE Interface Bus easy to use?

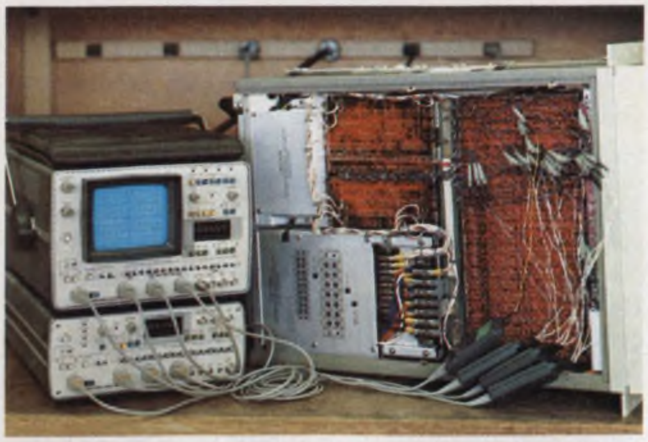
While everyone in Session 12 will sing the praises of the new IEEE General Purpose Interface Bus all will note that it is not yet easy enough to use. The interface bus is a standard technique for connecting as many as 15 stimulus and measurement instruments with a controller such as a minicomputer, a programmable calculator or a μP.

The characteristics of the standard will be discussed by Norbert Laengrich of Dana Laboratories, Irvine, CA. He'll talk about the history of interfacing, what the bus means to the user and the problem of interchangeability and control. He'll point out that the great advantage of the bus is that it allows configuring a system with equipment from several manufacturers without spending a great deal of engineering time. Further, such a system often can be changed without making you totally rewrite the program.

Laengrich will also give tips on writing program strings for applications requiring the bus.

Design advantages and limitations in connecting computational and readout equipment to the bus will be discussed by Stephen Baunach of Tektronix, Wilsonville, OR. He will reiterate the advantages cited by Laengrich and also note that a speed of 5000 cps, the limitation on the bus, is adequate for most systems because of the use of μPs and distributed processing with buffering.

Up to 8 channels of logic can be displayed and recorded at speeds of up to 50 MHz with the Biomation 851-D Logic Analyzer. Key features include a latch mode to capture glitches as narrow as 5 ns, 512-bits-per-channel of memory and combinational triggers.



The Hewlett-Packard 1600A and 1607A Logic State Analyzers couple together to form one of the most versatile analyzers available. On the 1600A display you can show up to 32 bits of logic state on up to 16 channels. This system can also display a map showing a sequence of logic states.

Baunach will also note that the speed is adequate for most applications—but might be slow for some. Another limitation is that not all manufacturers make instruments that communicate in the same format. Also, it is not always easy to convert from one format to another.

To help solve the command format problem, Peter Silvernale of Wavetek, San Diego CA will propose a command format for stimulus instruments that allows flexibility in formatting.

"Our format allows one name to be substituted for another," he says. "These names relate to sections of the instruments on the bus. The instrument will accept data in different formats."

Enter the bus user

Although he likes the IEEE bus standard, Eugene Fisher of Lawrence Livermore Laboratory, Livermore, CA will point out several problems that he finds, as a user. The main problem seems to be inadequate documentation. This is a problem with both the instrument manufacturers and the controller manufacturers. The manufacturers just don't explain how to use their equipment on the bus.

It is also difficult to program an instrument for use on the bus, he will point out. For example, a lot of instruments won't accept extraneous programming characters. Since these characters must be used in some instances and not in others, more instruments should just ignore these characters if they don't need them. "Perhaps," he notes, "it is time for the instrument manufacturers to get together on common bus formats and consistent programming techniques." ■■

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4		21	
6		22	
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18			

All Wescon 76 sessions (1-34) will be available on audio tape cassettes. Price is $5.00 each. Indicate tape requests by session number and include remittance as noted.

No. ______________

Total Sessions × $3 = $______________

Tape Cassettes × $5.00 = $______________

Plus $1 Mailing Charge = $______________

Total Cost = $______________

Make check payable to Wescon 76 and mail with this form to:

Wescon 76
999 N. Sepulveda Blvd.
El Segundo, CA 90245

Date ______________

____
Name

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Firm

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Street Address

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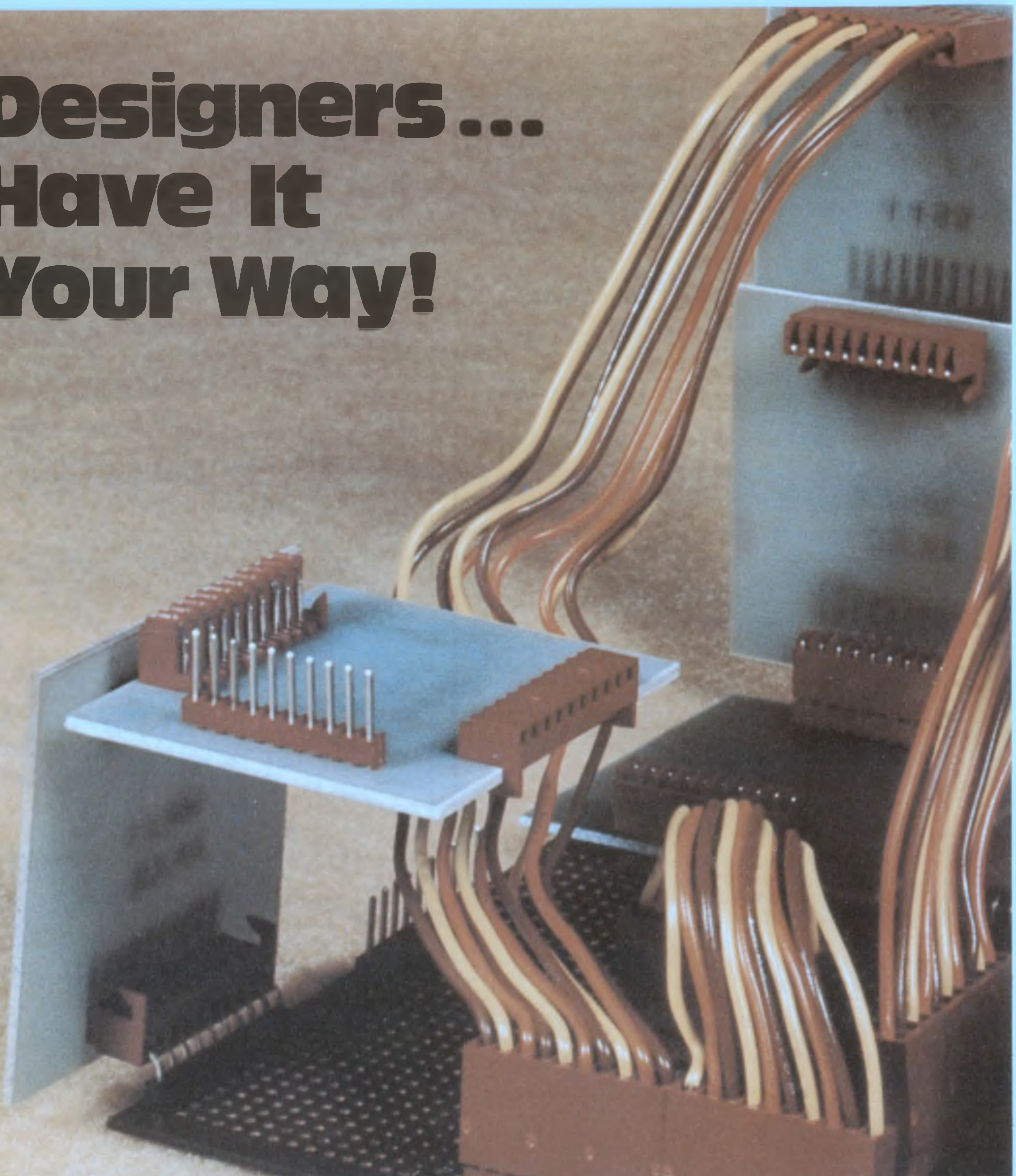
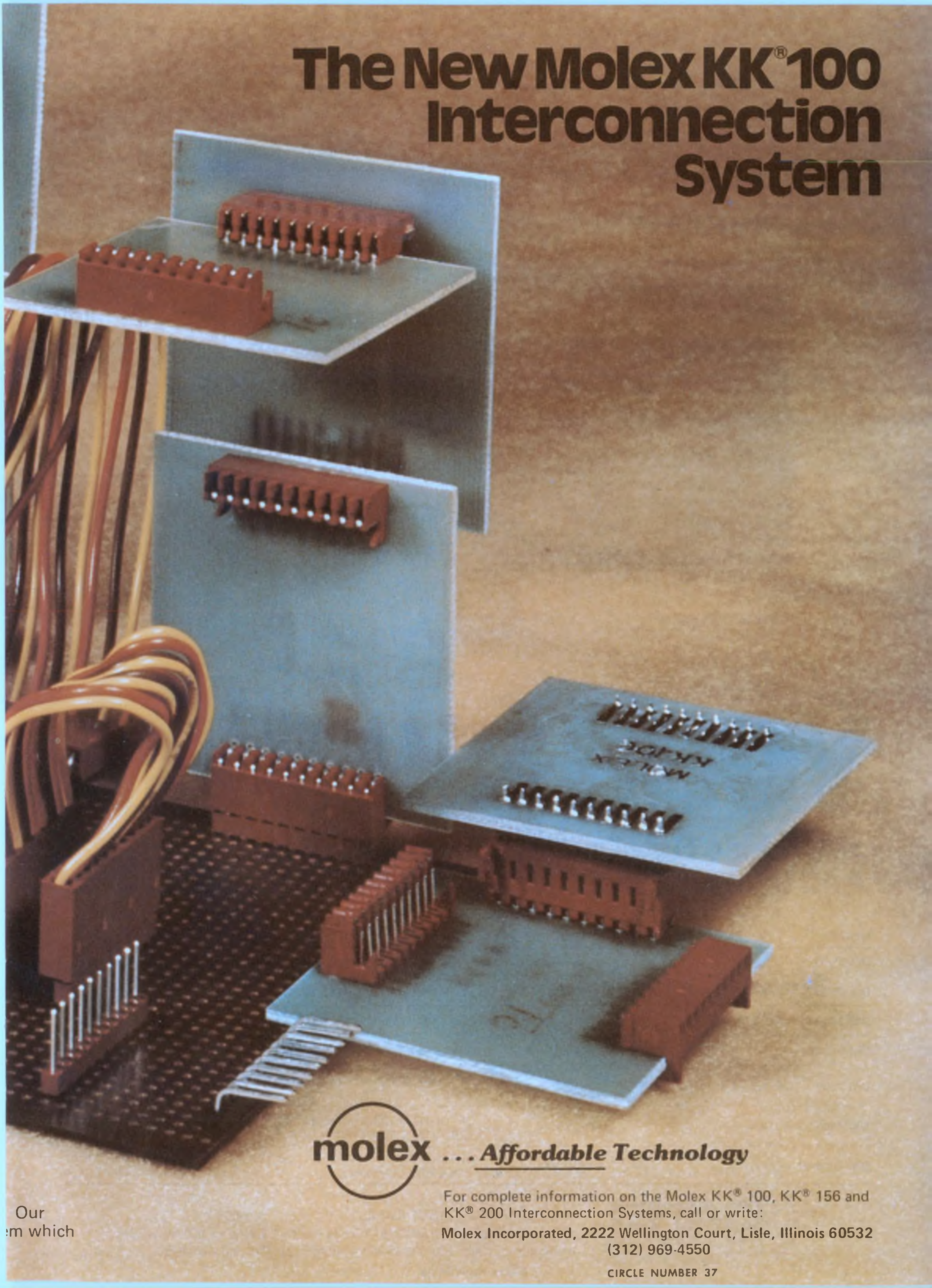
City, State, Zip Code

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CIRCLE NUMBER 37

Our
em which

Editorial

Scientific management

Jack was unhappy when old Charlie retired. At the traditional gold-watch ceremony, he worried about how Charlie's replacement would make out.

Charlie, you see, was comfortable to have around. In his quiet way, he got things done. He was responsible, among other things, for the production of a dozen people who turned out a critical subassembly.

Every day Charlie would send Jack a note saying, "Today we made 523. Seven didn't work so we did them over." Things always ran smoothly at Charlie's group. He liked his people and they liked him, so there was practically zero absenteeism except when somebody got seriously pregnant or something like that.

Then came Clarence, loaded with the latest management tools. He didn't believe in all this mollycoddling. He was going to produce demonstrable surges in production and, also, computer printouts of invaluable management information. By golly, he was going to bring the company into the 20th century.

He mounted a huge chart in his area and, every day, you could see production climb. At first, his group produced Charlie's average—about 520 subassemblies. Then the figures climbed—547, 583, 633 . . . It was phenomenal. Scientific management really worked.

And documentation? Never had Jack seen such a vast array of numbers. Unfortunately, he had other things to worry about, so he searched for the numbers he wanted—units manufactured (520, 547, 583, 633 . . .) and units rejected (7, 44, 98, 161 . . .)

"Hey, wait a minute," Jack shrieked. "I didn't see these reject figures on that chart. What's happening to the bad units?" "That's simple," Clarence told him, "we're putting them aside. We'll work on them some other time."

In the over-all picture, Clarence didn't cost the company a great deal of extra money. There was the extra computer time, the extra time Jack had to spend searching for the numbers he needed, quite a few parts wasted, sharply increased work-in-process inventory and lower net production. There was also significantly higher absenteeism and staff turnover because people wanted to produce for the benefit of their pride in workmanship rather than for a chart.

Clarence used the latest tools. Charlie had used the best tools—even if they were a bit old.

George Rostky

GEORGE ROSTKY
Editor-in-Chief

AMERICAN REVOLUTION BICENTENNIAL 1776-1976

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Maybe it's time we took the wraps off the rest of our line.
Everybody knows Garry makes great wire wraps. In fact, we're so well known for great wraps, it sometimes obscures the rest of our line: headers, racks, boards. A complete package. From LSI adaptor boards to ECL logic boards. From 6 pin header sockets to LED display sockets.
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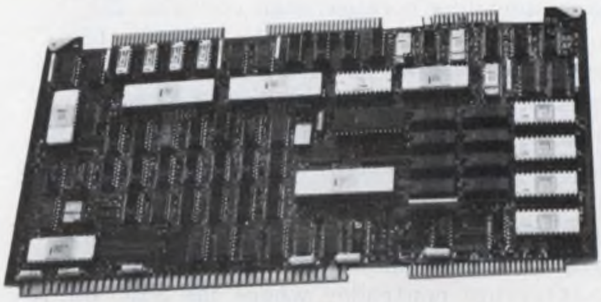
CIRCLE NUMBER 39

A second generation microcomputer takes on multiprocessing applications

A second-generation, single-board microcomputer system that is designed to be used in multiprocessing applications, has just been introduced by the Intel Corp. of Santa Clara, CA. Known as the SBC 80/20, the new system is a complete stand-alone computer on a single 6.75-by-12-inch printed circuit card. New features characteristic of this second generation unit are on-board multiprocessor bus-arbitration logic, a programmable interrupt controller, and two programmable counters.

Like its predecessor, the SBC 80/10, the SBC 80/20 includes the 8080A CPU, system clock, read/write memory, nonvolatile read-only memory, I/O ports and drivers, serial communications interface, and bus control logic and drivers on the board.

But unlike its predecessor, the SBC 80/20 may be connected to as many as seven other similar units via a parallel system bus for multiprocessor applications. The SBC 80/20s communicate with each other using shared memory as "mailboxes." With this method, one memory location is used as a status register,



and other memory locations carry data. When the SBC 80/20s read the status memory location and find they should input or output data, they read from or write data into memory.

The SBC 80/20s may communicate with one another using their built-in parallel I/O if the mailbox approach must be supplemented.

System-bus-access housekeeping is performed by a bus-control-logic IC on each SBC 80/20, an external, priority encoder and one-of-eight

(continued on page 64)

Low cost floppy-disc system records in IBM format

The Model FF-36, also called the Frugal Floppy, is based on another model made by the manufacturer, the FD-360. By eliminating the cabinet and power supplies the price has been reduced. The system records on floppy discs in the IBM format, an industry-wide standard.

The FF-36 contains the manufacturer's Model CF360 controller formatter, a floppy disc drive with daisy-chain capability, and all required connectors and cables. The system can be supplied with single (FF-36-1) or with dual (FF-36-2) drives.

The CF360 controller/formatter provides auto track and sector seek/verify, full sector I/O buffers and automatic CRC generation and checking. The controller can handle up to four drives with no changes in hardware or software. As an option, you can get a software package called FDOS-II, designed for any 8080 or 6800-based system. The software features: named variable-length files, and auto file create, open and close, multiple merge and delete commands.

The FF-36-1 costs $995, and the FF-36-2 costs $1590, both in quantities of 100 or more. Delivery is two or three weeks. Additional power supplies that are required: 5 V at 6 A, − 12 V at 1 A and each drive requires 24 at 2 A.

iCOM Inc., 6741 Variel Ave., Canoga Park, CA 91303. (213) 348-1391. CIRCLE NO. 501

(continued from page 63)

decoder on the motherboard. When one SBC 80/20 desires the use of the bus, it requests service through the external logic on the motherboard. That logic allows bus control depending on the request priority and bus availability. When the requesting unit receives an acknowledge, it takes control of the bus.

Each SBC 80/20 may operate independently of the system bus because each contains 2-k bytes of RAM (twice that of the SBC 80/10) and space for 4-k of ROM/PROM. Like its predecessor, the ROM is assigned to locations starting with 0000, but unlike its forebear, the RAM may be assigned by starting at any page boundary in the full 64-k memory space.

The SBC 80/20 has eight jumper-selected interrupts that are handled by an 8259 programmable-interrupt controller where the SBC 80/10 has six interrupts that must be polled under software control.

Three modes of handling interrupts are allowed: In a traditional manner, the 8259 may be used to interrupt the 8080 and generate a program counter vector corresponding to its highest-priority nonmasked pending request. Or a "rotating priority" scheme may be used to service up to eight devices of equal priority. Or finally, no interrupt may be generated, and the 8259 may be polled by the 8080 to determine the highest-priority nonmasked pending request.

Two of three programmable crystal-controlled timers in the 8253 generate either single pulses, or pulse trains. These timers may be connected to the SBC 80/20 interrupt controller to provide a real-time clock, or may be used to communicate with the outside world.

The timing cycles may be initiated by either software or logic transitions. Pulse durations are program controllable in the 2 μs to 120 ms range in approximately 2 μs steps. The third programmable interval timer is used as a programmable baud rate generator for the RS232C serial I/O port.

A programmable serial communications interface using the 8251 universal synchronous/asynchronous receiver transmitter is contained on the board. The serial interface can be programmed by system software to select the desired mode of operation, data format control character format, parity, and baud rate.

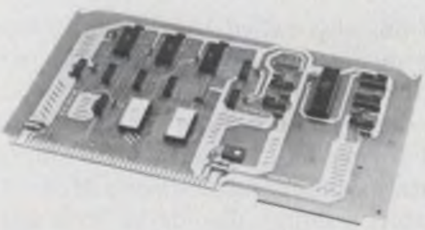
The SBC 80/20 includes only an RS232C compatible interface as contrasted with the SBC 80/10, which also includes a TTY interface on-board. The RS232C interface is brought out to a separate 25-pin edge connector on the board.

The SBC 80/20 contains 48 programmable parallel I/O lines implemented using two 8255 programmable peripheral interfaces. System software is used to configure the I/O lines into several combinations of input/output ports, including two possible eight-bit bidirectional ports, one port more than the SBC 80/10.

Intel Corp., 3065 Bowers Ave., Santa Clara, CA 95051. (408) 246-7501.

CIRCLE NO. 502

Do scientific calculations on numbers in your 8080 system



A plug-in card called the FPU, for "floating point unit," plugs into the Intel MDS systems. The FPU does complex scientific functions on this 8080-based system. Trigonometric functions including the sine, cosine, and tangent, plus the arc and hyperbolic variations can be calculated. In addition, log conversion (both to base e and base 10) and polar to rectangular coordinate conversion can also be done. If these functions sound like things you can do on most of the scientific calculators, guess what? The heart of the FPU is a calculator chip.

All numbers take 17 bytes of memory, consisting of a signed, floating point argument in scientific notation. Up to 64 bytes of RAM will be the maximum required locations. Linkage to the routines is accomplished by loading registers in the 8080 with pointers in program memory and with the code for the desired function.

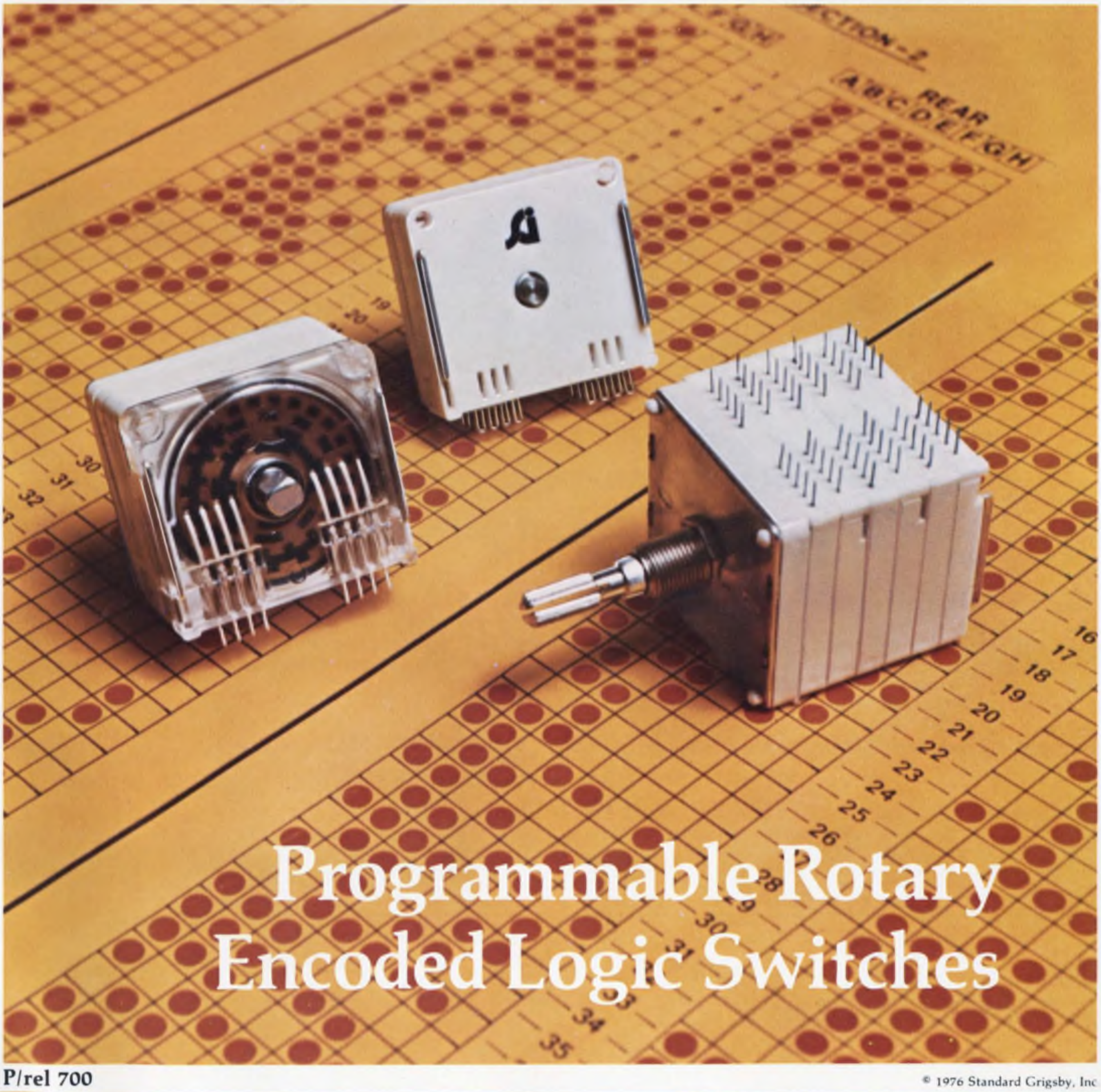
Execution times run rather long—almost as long as equivalent software routines—taking approximately 10 to 25 ms, depending on the function. Total cost for a complete system is $995 (single qty). Two thousand address locations must be reserved for communications with the FPU.

Cybernetic Micro Systems, 2460 EmbarcaderoWay, Palo Alto, CA 94303. (415) 321-0410.

CIRCLE NO. 503

IF YOUR COPY OF STANDARD GRIGSBY INSERT IS MISSING, CIRCLE 236 ▶

Standard Grigsby



Programmable Rotary Encoded Logic Switches

P/rel 700

. . . the industry's first programmable rotary encoded logic switch.

Standard Grigsby introduces the P/rel™ switch—our new Programmable/Rotary encoded logic switch. This switch was developed to economically provide an alternative to conventional rotaries and thumbwheel switches in the manual switching of complex binary codes.

Up to 60 detent positions are achieved with our Dual Flex™ detent (described on p.3). Full programmability is provided by the use of a specially processed printed circuit disc. (see P/rel Disc on p.3)

This switch was designed to lend itself to full automation. Our automation layout includes a 100% program inspection to customer specifications.

Not only is the P/rel™ switch low in cost due to automation, but its installed costs will be reduced by the use of our printed circuit terminals. For those who don't wish to make use of this feature, solder terminals are available.

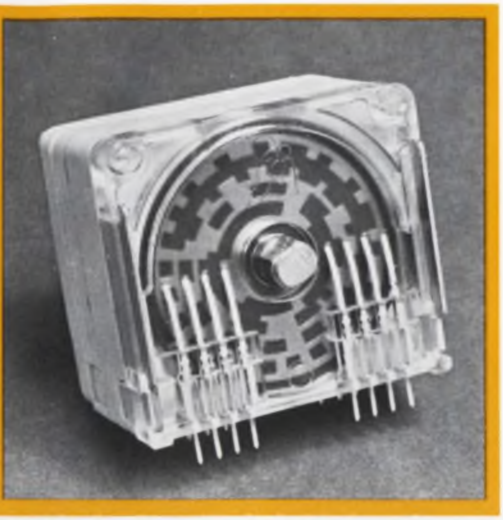
The programmed disc and wiping contacts are protected inside of an enclosed housing which tightly snaps together to prevent contact contamination due to solder flux. In addition, the use of standoffs, which are an integral part of the molded housing, helps prevent solder flux contamination.

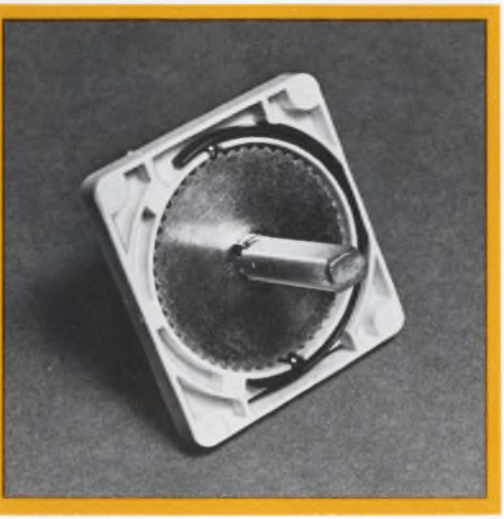
Direct-drive lighted numerical displays can also be accomplished via a single programmable disc. Modular construction allows units to be stacked to whatever number of stators the circuitry requires. Intermodule spacers can be used for special spacing. All printed circuit terminals are .100" center with spacing between rows of .200". The strongest, most reliable materials have been used for all parts. All metal parts are finished to resist corrosion and insure long life. Molded plastic parts are all high temperature 94VO grade.

20 contact terminals provide a large number of programming possibilities for even the most complex codes. And, the use of concentric shafts allows up to 120 detent positions from a single switch!

Other features:

- Low cost via full automation
- Fully programmable to any truth table
- Up to 60 detent positions
- 20 terminals per module
- Dual Flex™ long life detent with tactile feedback adjustment and "tease" resistance
- Printed circuit or solder terminals
- Metal bushing, shaft, stops, locating key
- 100% program disc inspection
- Semi-precious metal contacts
- Soldering standoffs
- Direct drive of LED displays
- Spring alloy terminals to minimize bending or twisting
- Concentric shafts
- Spacers available between modules





P/rel™ Disc *(Upper Left)*

The P/rel™ disc is on a .062" thick printed circuit board which utilizes a special proprietary process for plating and surface preparation. This process results in a very hard surface to minimize wear on both the disc and contact terminals. The code layout for the disc is carefully prepared with dielectric spacings, code addressing, and output termination in mind. Each disc is tested on a mini-computer which has its own storage capability to assure disc to disc and assembly to assembly reliability.

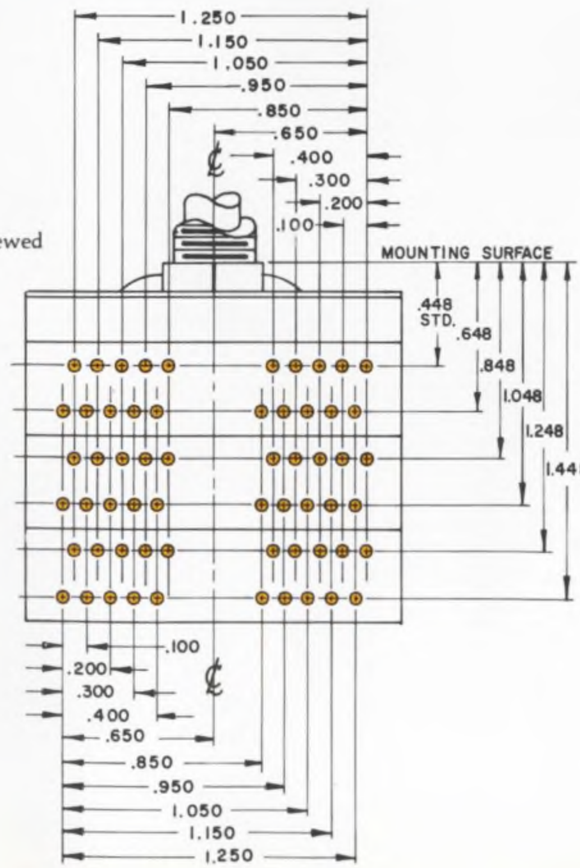
Dual Flex™ Detent *(Lower Left)*

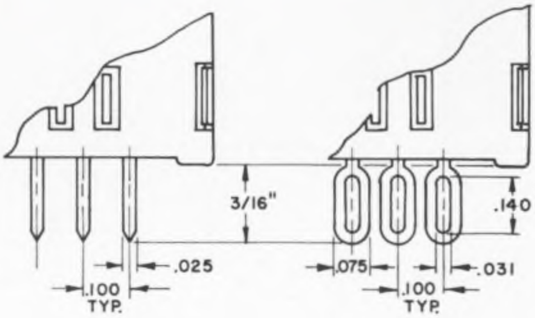
The Dual Flex™ detent was designed for long life, extreme accuracy, tactile feedback and resistance to "teasing." Originally designed for high reliability avionics applications, it features a dual ball, starwheel drive and a single C spring. The totally unique concept of the Dual Flex™ detent is that the C spring is allowed to travel within the molded housing; thus decreasing the amount of spring displacement in a given area and spreading the possibility of spring fatigue over a larger surface area.

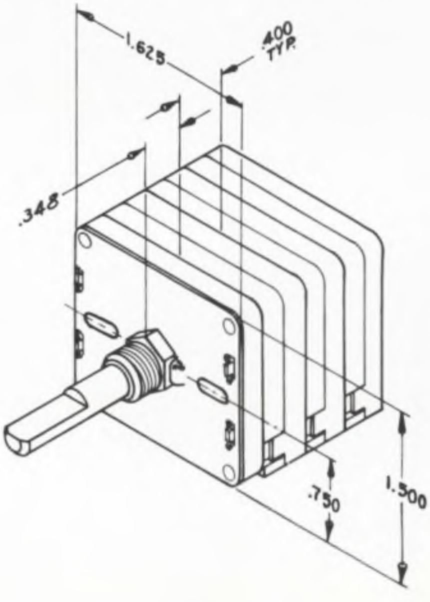
Electrical Ratings:

Current Carrying Capacity	— .25 amp
Resistive Load Switching	— .125 amp @ 115 AC
Contact Resistance	— initial 0.10 ohm maximum
Insulation Resistance	— 100 megohms
Dielectric Strength	— 500 VAC minimum
Contact Life	— 25K cycles of 720° minimum (50K cycles of 360° minimum)
Operating Force	— 14 to 24 inch oz. standard
Temperature Ranges	— -55°C to +85°C
Insulation	— Thermoplastic meets U.L. 94V-O
Programmable Disc	— Plated copper clad laminate
Contacts	— Plated spring tempered material
Front Plate and Shaft	— Cold rolled steel cadmium plated
Bushing	— Brass, aluminum or die cast zinc

Footprint viewed from top of switch.



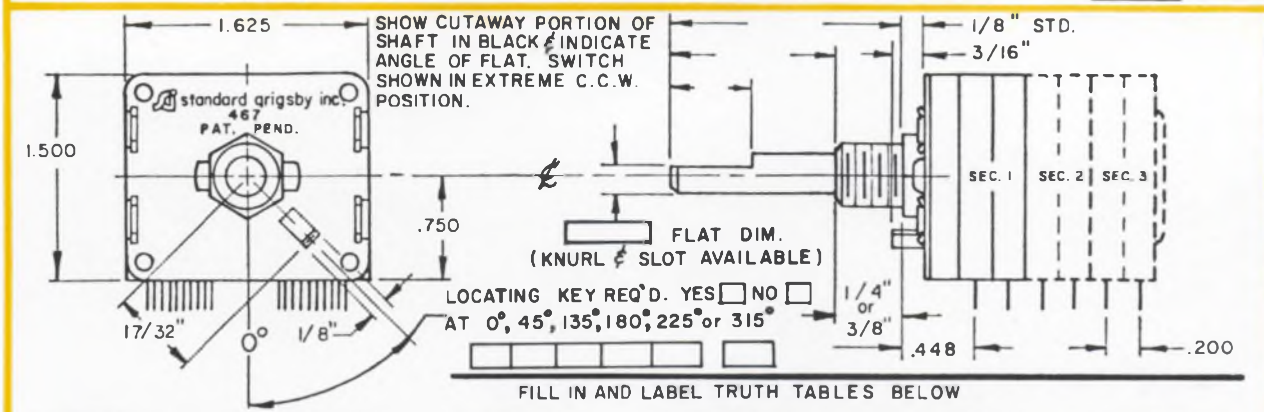




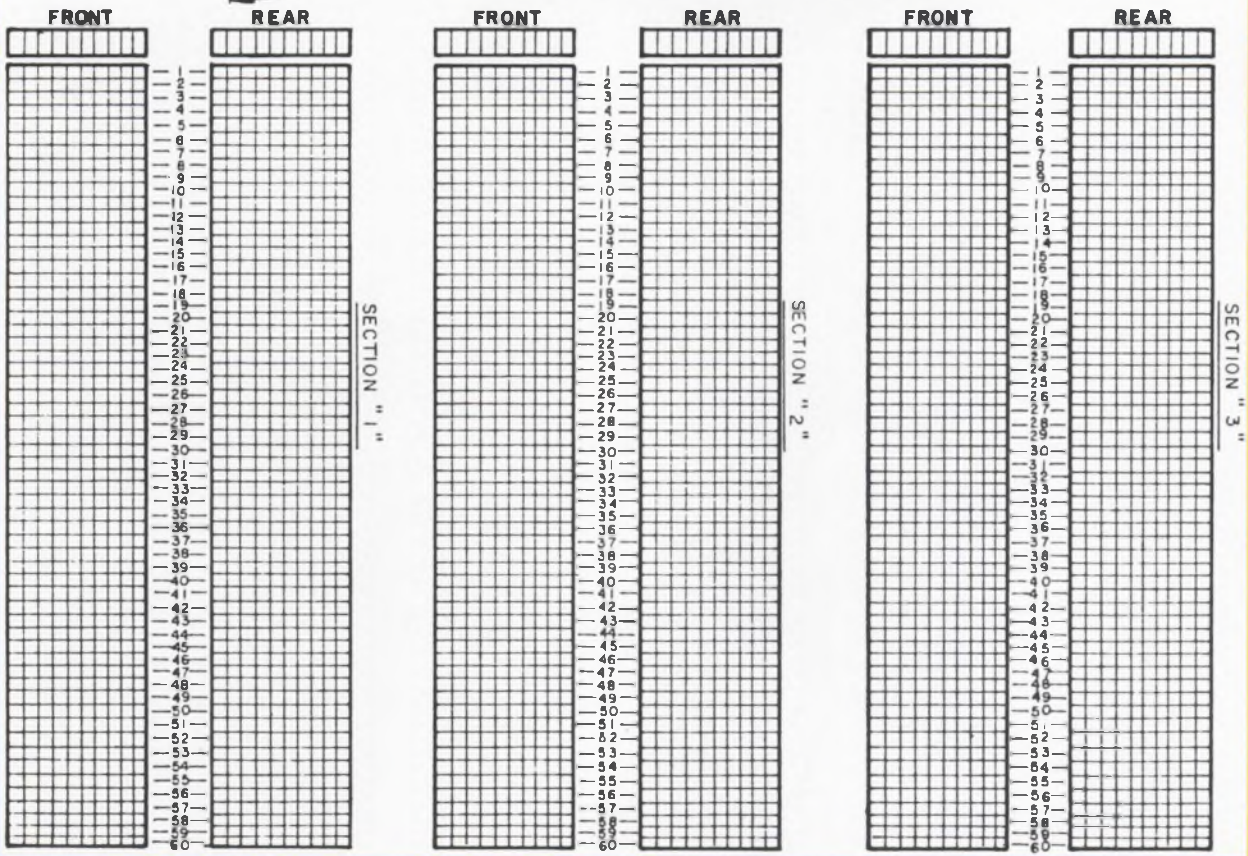
TELEPHONE
312/897-8417

standard grigsby, inc.
920 RATHBONE AVENUE AURORA, ILLINOIS 60507

TYPE P/REL SWITCH
_______ POSITIONS



FILL IN AND LABEL TRUTH TABLES BELOW



CUST. ____________
PART NO. ____________ YES
STAMP NO. ____________ NO

☐ TOTAL NO. OF SECTIONS
☐ NO. OF POSITIONS
☐ SHORTING CONTACTS
☐ NON-SHORTING CONTACTS *
☐ STOPS
☐ CONTINUOUS ROTATION
☐ ANGLE OF THROW
☐ P.C. TERMINAL
☐ SOLDER LUG

* NON-SHORTING POSSIBLE UP TO "24" POSITIONS.

SUPPLY MOUNTING HARDWARE:

☐ YES
☐ NO
☐ ASSEMBLED TO BUSHING
☐ BULK

____ 3/8"-32 NUTS ____ ACROSS FLAT
____ 3/8" INT. TOOTH LOCKWASHER

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TWX 910-232-3138

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6. Rockwell PPS-4/2
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9. Mostek F-8
10. Intel 8008-1
11. Intel 8080 A
12. AMD 8080 A
13. T.I. 8080 A
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15. Siemens 8080 A
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46. Western Digital MCP-1600
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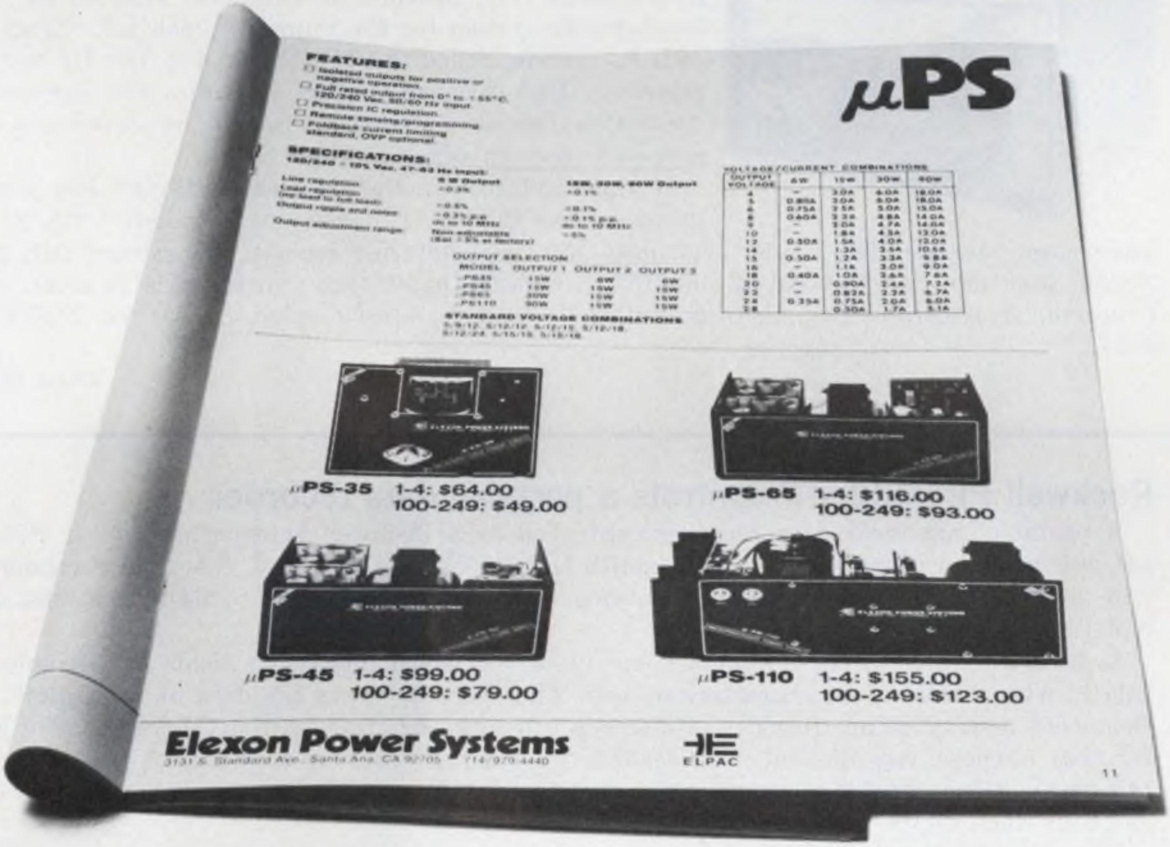

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They've got the right voltages. The right currents. The right specifications.

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CIRCLE NUMBER 40

A CRT display and printer added to Intellec MDS System

An interactive display console and a line printer are now available for Intel's Intellec MDS Microcomputer Development System. The MDS-CRT keyboard display and MDS-PRN printer are said to be more economical than other displays and printers. The display console costs $2240 and the printer $3200 in quantities of 1 to 9, with delivery in 30 days.

The MDS-CRT and MDS-PRN provide all communications normally required during programming, software emulation, prototyping, in-circuit emulation, documentation and production test troubleshooting, and field engineering with the system. A teletypewriter can also be used, if desired, for low speed I/O operations.

The peripherals are compatible with the diskette system that has already been introduced. A program development software aid, called "symbolic debugging," requires a versatile display and display copying. Both of the peripherals are suited to this programming tool.
Intel Corp., 3065 Bowers Ave., Santa Clara, CA 95051. (490) 246-7501.

CIRCLE NO. 504

A development system for the 2650 μP uses paper tape

The μPAL development system, from Processor Applications Ltd., provides a lower cost alternative development system for the Signetics 2650 μP. Signetics sells its system, called the TWIN, for $14,000. Its cost is relatively high because you get a floppy-disc storage that allows larger amounts of data to be stored and accessed than on other storage media.

If you don't require the elegance of floppy-disc storage, however, use the μPAL development system with its paper tape storage. The reader transmits 150 characters per second. The system sells for $5250; less than half the cost of the TWIN, with the paper-tape punch available as an extra.
Processor Applications Ltd., 2801 E. Valley View Ave., West Covina, CA 91792. (213) 965-8865.

CIRCLE NO. 505

Rockwell PPS-4/2 μP controls a portable data recorder

A portable, handheld data recorder controlled by a Rockwell International 4-bit PPS-4/2 μP will soon be introduced by Wordsmith Inc., of Marina Del Rey, CA. The recorder will store 4-bit data words in 4-k locations—optionally expandable to 64-k locations—of NMOS memory.

Data are entered using a standard calculator keyboard into seven fields of variable length, with a total of 24 characters or less. The operator views the data on a 24-digit florescent display before filing it in memory using the separate button that each field has for that purpose. An internal clock records the time of entry of each set of data. Up to 143 transactions per 4-k of memory may be stored, with each transaction containing 24 data and four clock digits.

The recorder is oriented toward such applications as inventory control in stores or for utility meter reading. After a day's data are recorded, the Wordsmith/1 can be hooked to a standard modem via its built-in RS-232-C connector so that the data can be transmitted to a host computer.

An additional feature of the Wordsmith/1 is that it can be connected to a small printer for hard-copy printout in the field. For meter reading, the inspector enters the month's consumption of oil or gas at the customer's home. The Wordsmith/1 calculates the bill, and the printer makes a copy on the spot which is left at the home. Wordsmith/1 will sell for about $1200 in a minimum configuration. It measures 4 × 11 × 2 in. and weighs 2-1/2 lb, including integral battery pack.
Wordsmith Inc., 4316 Via Marina Del Rey, CA 90291. (213) 823-2278.

CIRCLE NO. 506

CIRCLE NUMBER 41

NOW FORTIFIED WITH DCA*!

*DCA means Direct Cursor Addressing. And that's exactly what you'll find added to each and every ADM-3A Dumb Terminal from Lear Siegler. As a basic, standard ingredient.

Now our Dumb Terminal's even more of a snap to use. Because direct addressing lets the operator tell the cursor—quite literally—where to go. Up. Down. Right. Left. Any X and Y location you choose. Even where to home.

Your operators will tell you it's "GRRRREAT!" Not to mention fast and simple. For tracking down typos. Typing in additions. Even for retyping entire passages. Because if the problem's still on the screen, it's open to instant improvement.

What's more, the Dumb Terminal still provides a balanced diet of your favorite standard features. Like a bright 12" diagonal screen. Fifty-nine data entry keys. A 960 character display. Plus 32 positive action switches that let you activate goodies like 1 of 11 different baud rates, an RS232S interface, or a 20mA current-loop. And more. All handsomely packaged in a handy hatchback bonnet.

And if you want to sweeten up the deal by adding switch-selectable options, you've got your pick of plenty. Like a complete upper and lower case USASCII character set, a 1920 character display, or even an "answer-back" capability.

So forget the flaky imitations with their puffed-up, premium prices. (And join the thousands who already start their day, in an LSI kind of way.)

Because what the Dumb Terminal—now fortified with DCA—really delivers, you won't find anywhere else.

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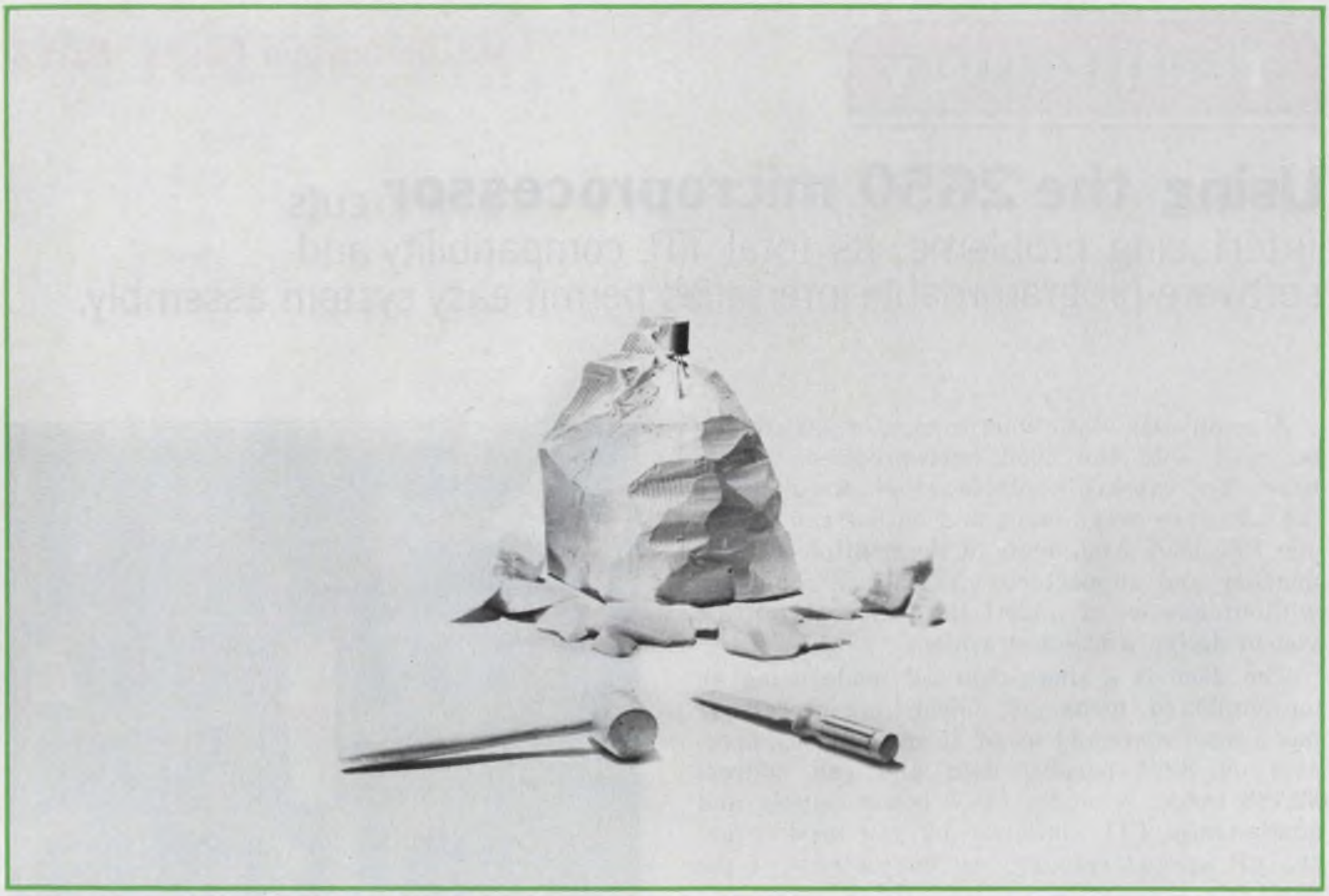
Forget the box tops, for more information contact:
Lear Siegler, Inc./E.I.D., Data Products
714 N. Brookhurst St., Anaheim, CA 92803
Tel. (714) 774-1010

CIRCLE NUMBER 42



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Oh, other suppliers got in the act once we showed them how. But nobody can offer higher FET quality or reliability. And no one can provide more immediate off-the-shelf delivery of FETs to meet your particular needs.

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CIRCLE NUMBER 43

Technology

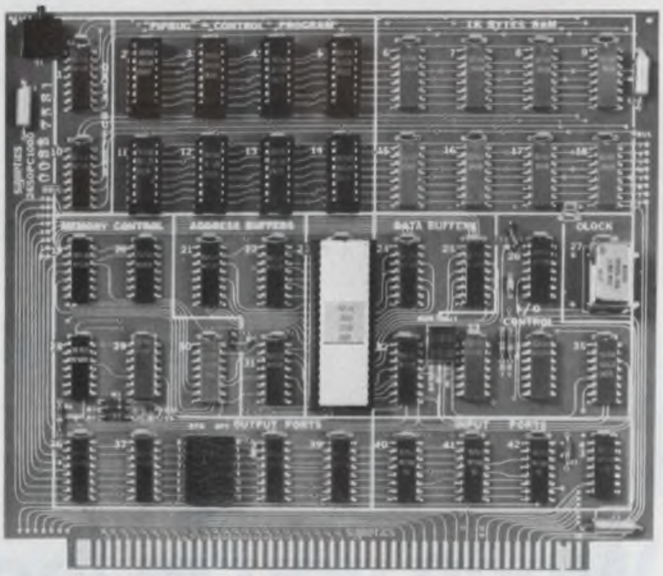
Microprocessor Basics: Part 6

Using the 2650 microprocessor cuts interfacing problems. Its total TTL compatibility and software-programmable interfaces permit easy system assembly.

A completely static microcomputer system can be built with the 2650 microprocessor as its heart. You can easily interface logic circuits with the μP since every input and output can handle one TTL load. And, many of the multiple-sourced memory and support circuits can be connected without any extra interfacing—thus permitting you to design a low cost system.

The 2650 is a single-chip μP made using an ion-implanted, n-channel, silicon-gate process. It has a fixed command set of 75 instructions, operates on 8-bit parallel data and can address 32,768 bytes. A single +5-V power supply and single-phase TTL clock are all you need to get the μP up and running. All bus outputs of the 2650 are three-state and can drive either one 7400-type load, or four 74LS loads.

Both memory and input/output (I/O) lines operate asynchronously at any speed up to the maximum data transfer rate of the memory circuits without additional buffering. No external latching of data is needed.

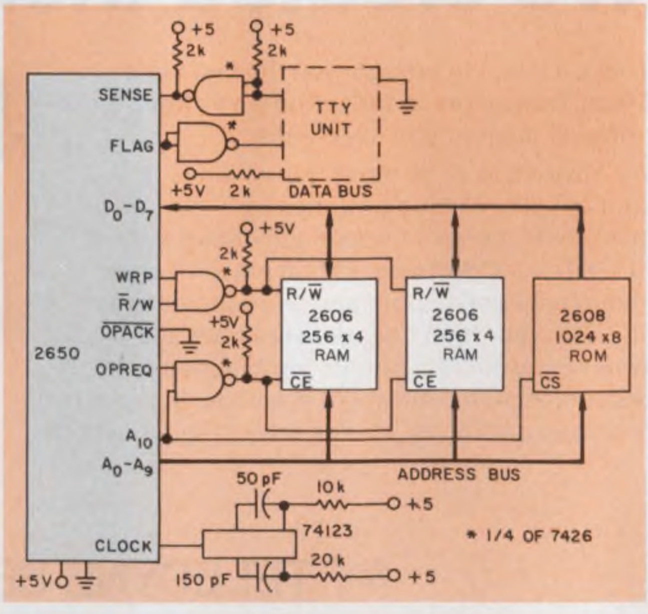


A complete microcomputer on a board, the 2650PC-1000, contains the 2650 μP, a control and R/W memory, an I/O port, a clock and all necessary interface circuits to get a system up and running.

Specialized support circuits cut complexity

Aside from the 40-pin μP IC there are many support circuits and development aids in the 2650 family (Tables 1 and 2). Some of the specialized interface circuits to be introduced include the 2651 programmable communication interface (PCI), which accepts program instructions from the μP and supports almost any serial-data communication mode. Another circuit, the 2655, is a programmable peripheral interface (PPI) that contains three bidirectional 8-bit I/O ports and an 8-bit data bus to communicate with the processor.

The 2650 has a maximum clock frequency of 1.25 MHz, giving a clock period of 800 ns. Each processor cycle requires three clock periods, and an instruction can require two, three or four processor cycles. Since the μP contains static rather than dynamic circuitry, the clock frequency can be dropped to zero without affecting



1. **You can put together a complete microcomputer** with only six ICs. The 2650 offers full TTL compatibility on every input and output line to ease the interface requirements to external circuits.

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Table 1. System components for the 2650

Product	Description	Price (1-24)
2650	8-Bit, N-channel, microprocessor	$26.50
2651	Programmable communication interface	‡
2655	Programmable peripheral interface	‡
2102-1	1024 × 1, N-channel, 500 ns RAM	4.17
2604	4096 × 1, N-channel, 300 ns RAM	22.00
2606	256 × 4, N-channel, 750 ns RAM	5.00
2606-1	256 × 4, N-channel, 500 ns RAM	5.50
2608	1024 × 8, N-channel, 650 ns ROM	*
82S10/11	1024 × 1, Bipolar, 45 ns RAM	24.60
82S23/123	32 × 8, Bipolar, 50 ns PROM	6.45
82S114	256 × 8, Bipolar, 60 ns PROM	39.00
82S115	512 × 8, Bipolar, 60 ns PROM	40.00
82S126/129	256 × 4, Bipolar, 50 ns PROM	8.20
82S130/131	512 × 4, Bipolar, 50 ns PROM	15.05
8T26	Three-state quad bus transceiver	4.29
8T28	Three-state quad bus transceiver	4.29
8T31	8-Bit bidirectional input-output port	13.20
8T34	Quad three-state transceiver	3.63
8T95/96	Hex three-state buffer	2.90
8T97/98	Hex three-state buffer	2.90
2650PC1001	Prototyping card	495.00
2650PC2000	4-k byte memory board	395.00
2650PC3000	Demonstration module	149.00
2650KT9000	Prototyping kit	95.00
2650S2000	Development/demonstration base with power supply	775.00
2650BM1000	Manual set, including update service	40.00
2650AS1000	PIPASM—Fortran IV batch cross assembler (32-Bit)	1250.00
2650AS1100	PIPASM—Fortran IV batch cross assembler (16-Bit)	1250.00
2650SM1000	PIPSIM—Fortran IV batch cross simulator (32-Bit)	750.00
2650SM1100	PIPSIM—Fortran IV batch cross simulator (16-Bit)	750.00
Training	Extensive three day seminar describing	375.00 (West Coast)
	2650 hardware, programming, and applications	425.00 (Other)
	One-day basic microprocessor seminar	40.00
2650KT9500 ABC kit		190.00
2650PC1500 ABC card		275.00

* not available in unit-quantity bracket.
‡ to be announced.

any internal registers. The μP can then be manually stepped through a program for debugging.

A 2650-based microcomputer requires almost no external support circuits, save for a ROM or RAM, a clock and some line drivers (Fig. 1). All the ROMs or RAMs are connected to the data and address busses and up to five other control pins. The entire system is modularized and can be expanded in building-block fashion.

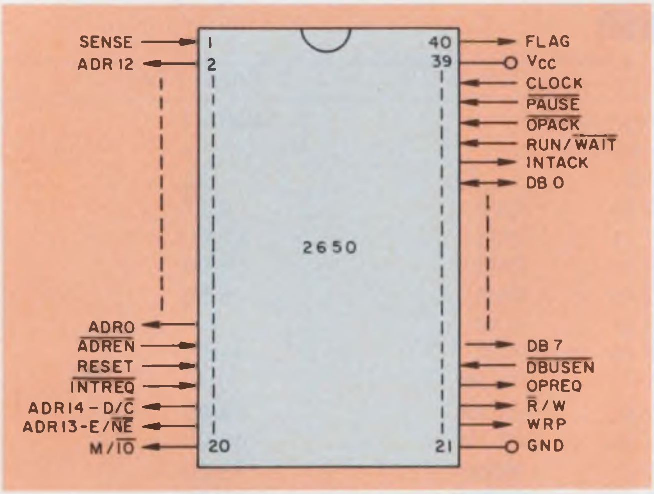
The three main interconnecting busses are the bidirectional data bus, which requires eight lines; the address bus, which requires up to 15 lines; and the memory-control bus, which requires up to five lines. In addition to the 8-bit bidirectional data bus on the 2650, a single-bit-wide I/O port for serial inputs is built into the μP.

Eight-bit wide I/O instructions either are one or two-byte commands. They are designated as nonextended (one byte) or extended (two byte). The nonextended I/O instructions can be directed to one of two I/O devices designated as either data or control. The data or control devices can be accessed from any general purpose register with a single-byte read or write instruction. Extended I/O instructions require two bytes and can be used simultaneously to select a device and transfer data to it.

Assembling a μC is easy

To get a 2650-based system operating, let's first look at all the control and signal pins on the μP (Fig. 2). The SENSE line (pin 1) is a direct input to one of the bits of the Program Status Word register in the 2650 (a special-purpose, 16-bit register that holds status and control bits; its abbreviation is PSW). This pin serves as a serial input port. The bit can be stored or tested by a software instruction.

Pins 2 through 14 represent the lower 13 bits of the address bus and can directly address 8-k bytes of memory. The $\overline{\text{ADREN}}$ (Address Enable)



2. **The different control lines on the 2650** provide handshaking responses to simplify the interface. Two of the memory-address lines serve the dual purpose of cutting the pin count and providing better control.

signal from pin 15 permits external control of the three-state address bus. When pin 15 is HIGH, the address-bus lines appear as high impedances; this permits wired-OR connections with other signal lines.

The RESET line (pin 16) is normally used to start the processor after power-up or to restart a program. When brought HIGH, RESET clears both the Interrupt Inhibit control bit of the PSW and the Internal Interrupt-Waiting signal, then sets the Instruction Address Register to zero.

Pin 17 is the $\overline{\text{INTREQ}}$ input (Interrupt Request) and is normally HIGH. By bringing the line LOW, an external device can change the program flow. When the processor recognizes an $\overline{\text{INTREQ}}$ input, it completes its current instruction, places a ZBSR (Zero Branch to Subroutine Relative) instruction into the instruction register, sets the Interrupt Inhibit bit in the PSW and responds with INTACK (Interrupt Acknowledge) and OPREQ (Operation Request) signals. These signals perform a "handshake" with the peripheral that initiated the interrupt.

Pins 18 and 19, the ADR14 and 13 (D/$\overline{\text{C}}$ and E/$\overline{\text{NE}}$ lines), serve dual functions and are controlled by the next line, pin 20 (the M/$\overline{\text{IO}}$ line). When pin 20 is HIGH (in the M state), pins 18 and 19 act as the higher-order bits of the memory address. However, when pin 20 is LOW, pin 18 is used to discriminate between two types of one-byte I/O instructions. When LOW, pin 18 indicates that either a Read or Write instruction to the I/O device (control) is to be executed; when HIGH, it indicates a Read or Write instruction to the I/O device (data).

The output from pin 19 defines whether a one or two byte I/O operation is being performed. When LOW, the instruction is a one-byte nonextended operation and when HIGH the instruction is a two-byte extended command.

The ground line, pin 21 is connected to the general system ground. The next line, pin 22, is the Write-Pulse output (WRP). It provides a

Table 2. Support hardware and software

Development software	
PIPASM	An assembly-language assembler written in Fortran IV. It operates in a two-pass mode to build a symbol table, issue helpful error messages, produce an easily readable program listing and output a computer readable object module. Two versions are available: The AS1000 for 32-bit machines and the AS1100 for 16-bit machines.
PIPSIM	A Fortran IV program you can use to simulate the execution of your program without using the 2650. PIPSIM maintains its own internal Fortran storage registers to describe the 2650 program, its registers, the ROM/RAM configuration and input data. There are two versions available: The SM1000 for 32-bit machines and the SM1100 for 16-bit units.
PLμS	The Signetics Higher Level Language allows you to program the 2650 in PL-type language and is available for both 16 and 32-bit machines. PLμS is also available from Signetics on mag tape or from NCSS and GE Timeshare Networks.
System development hardware	
TWIN	The Microprocessor Prototype Development System .known as TWIN typically consists of three hardware elements: A prototype development computer (PDC), a floppy-disc storage subsystem and a system console. The PDC includes a MOS and bipolar PROM programmer and an in-circuit emulation/hardware debug facility. System software includes operating system file management, debug software, a text editor and a 2650 resident macro assembler.
ABC	The Adaptable Board Computer prototyping system ABC1500/9500, is a modular microcomputer containing a 2650 μP, memory, I/O ports and support circuitry. Included on the board are 512 bytes of RAM and 1-k byte of ROM, containing PIPBUG (a loader, editor and debug program).
KT9000	A microprocessor protoyping kit that contains a 2650 μP and enough circuits to build a single-board computer system.

Internal architecture of the 2650 microprocessor

The internal structure of the 2650 CPU is centered about the ROM and arithmetic-and-logic unit (ALU). An on-chip ROM contains the control microprograms for the ALU, which does the arithmetic, Boolean and combinatorial shifting functions. The ALU performs 8-bit parallel operations and uses carry-look-ahead logic for fast operation.

A second, small ALU is used to increment the instruction address register and to calculate the operand addresses for the indexed and relative addressing modes. This separate address adder permits complex addressing modes to be used with no increase in instruction execution time.

The general-purpose register stack and the subroutine-return address stack are built from static RAM cells to permit clock rates of the μP to be brought all the way down to dc. The register stack contains seven addressable 8-bit registers and the subroutine return-address stack can hold up to eight 15-bit addresses to permit up to eight subroutine nesting levels.

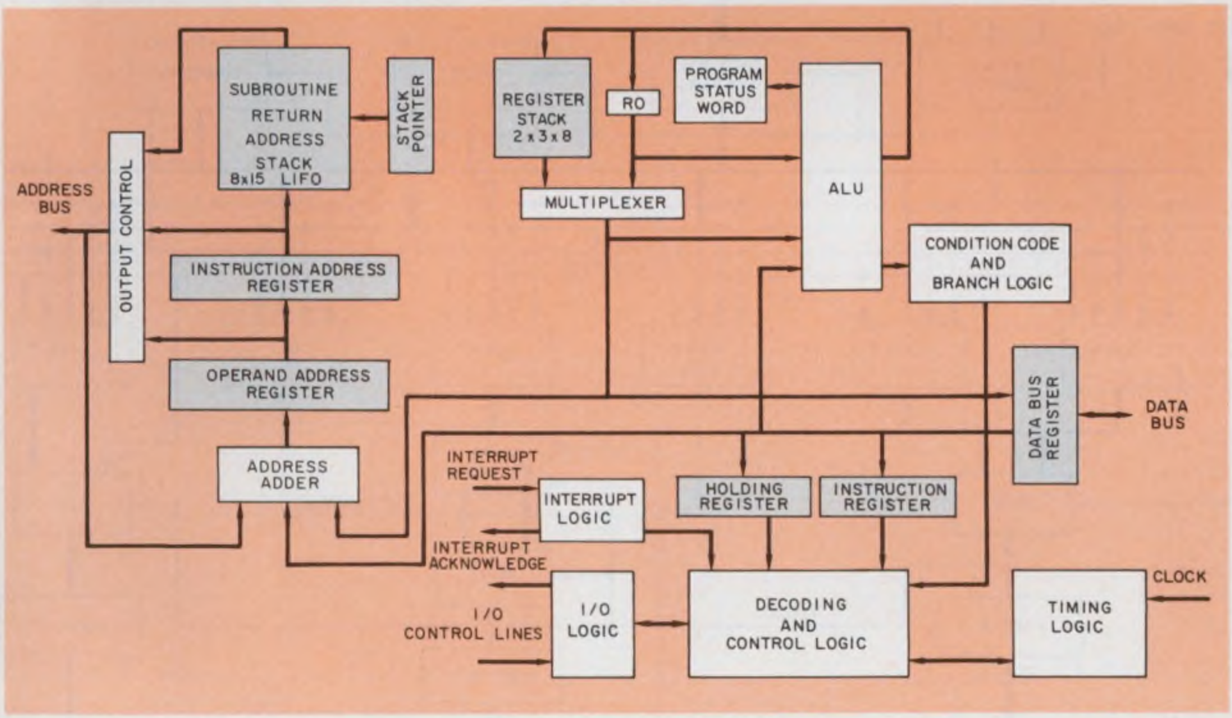
Since the subroutine stack is on the μP chip, very low package-count systems can be built. Separate 15-bit instruction and operand address registers are also included on the chip.

Within the μP is a special-purpose register called the Program Status Word (PSW) that holds the status and control bits of the processor. The PSW can be divided into two parts—an upper and lower half (PSU and PSL). All bits can be tested, loaded, stored, preset or cleared using commands from the fixed instruction set.

The 2650 has only a single level of hardware vectored interrupt. When an interrupt occurs, the μP finishes its current instruction and then sets the interrupt-inhibit bit in the PSW. The processor then executes a Zero Branch to Subroutine Relative instruction (ZBSR) and sends out Interrupt Acknowledge and Operation Request signals. When the interrupting device receives in INTACK signal, it inputs an 8-bit address (the interrupt vector) on the data bus.

The basic instruction cycle for the 2650 requires three clock periods. Direct instructions require from one to three processor cycles. The circuit only requires a single-phase clock that runs at a maximum speed of 1.25 MHz.

The processor is capable of directly addressing 32-k words of memory since there are 15 address lines. Two of the address lines also serve as control lines on a multiplexed basis. Both the ADR13 and ADR14 lines deliver address data when the $M/\overline{IO}$ line is in the M phase. The ADR13 line discriminates between extended or nonextended I/O instruction when $M/\overline{IO}$ is in the I/O phase. The ADR14 line discriminates between data and control I/O when $M/\overline{IO}$ is in the I/O phase. The dual functions of these pins help to keep the pin count to a minimum.

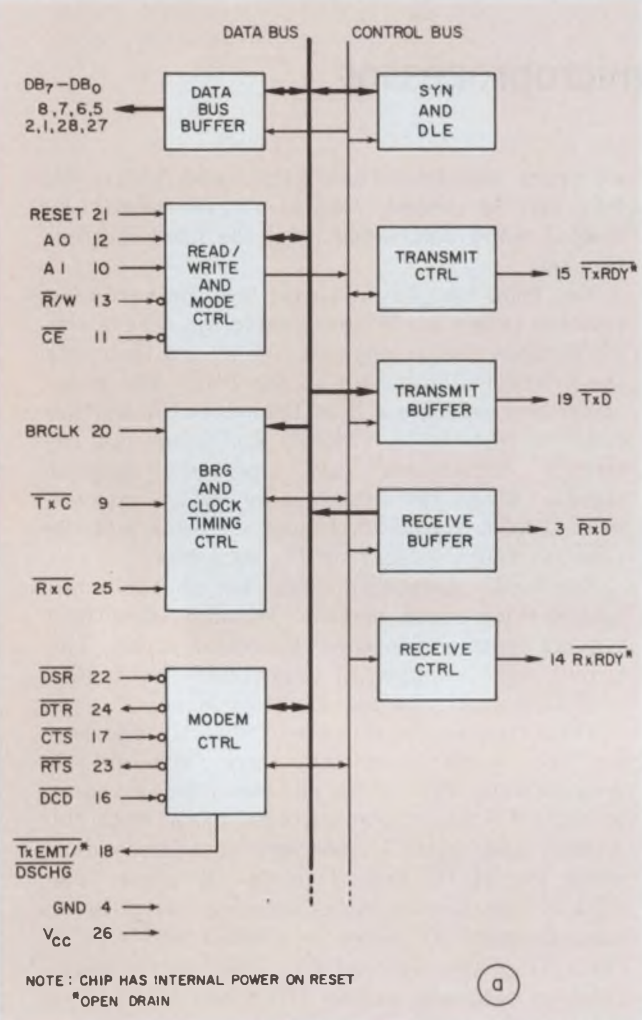


positive-going pulse in the middle of each requested write operation. During read operations the WRP line appears as a high impedance. The WRP line is designed to be used with the company's 2606 RAM to deliver timed Write signals.

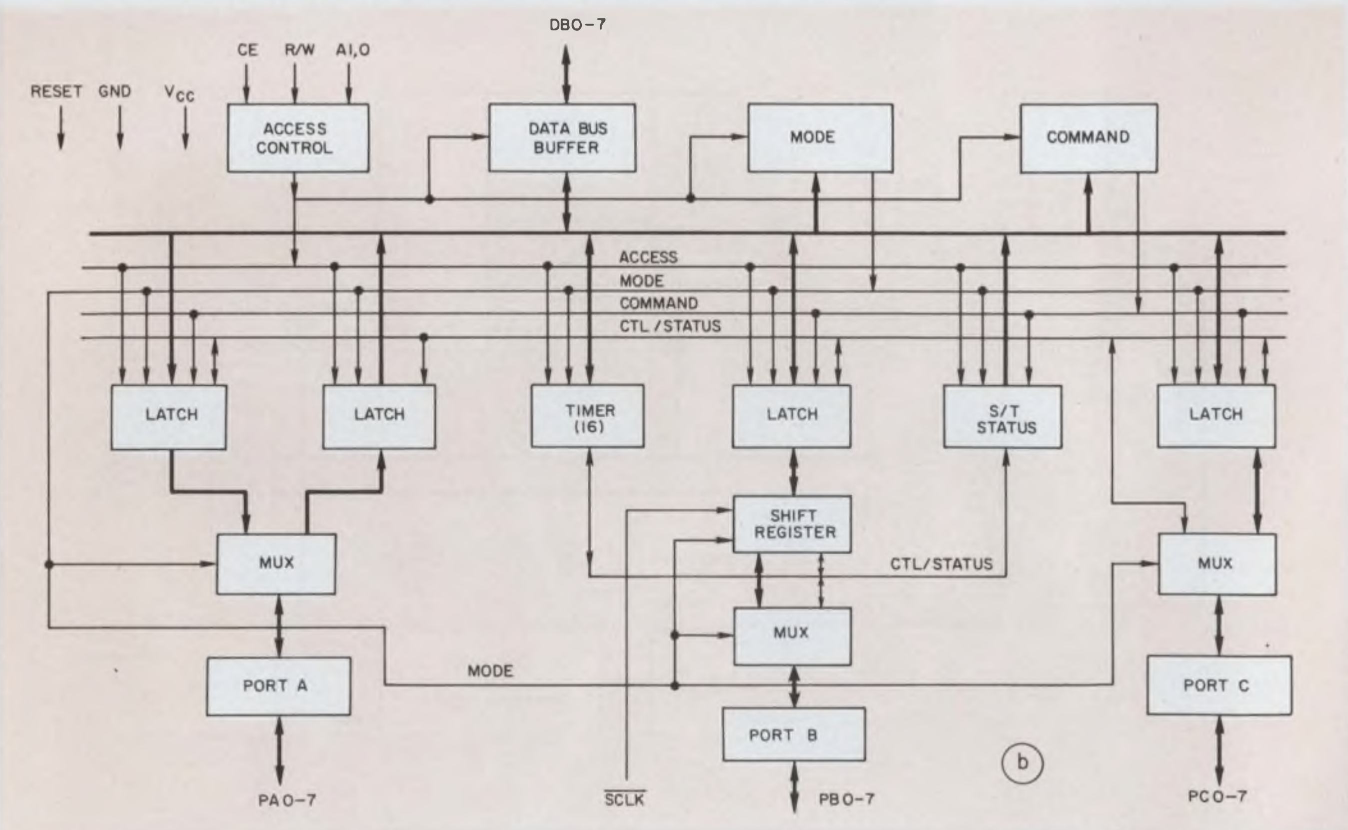
On pin 23, the R/W (Read/Write) output defines whether an operation is Read or Write (HIGH corresponds to Write, LOW to Read). The OPREQ output line (Operation Request), pin 24, coordinates all external operations. When OPREQ is HIGH, the M/$\overline{\text{IO}}$, $\overline{\text{R}}$/W, E/$\overline{\text{NE}}$, D/$\overline{\text{C}}$ and INTACK lines describe the external operation being performed. When LOW, the OPREQ line indicates that the external operation is complete.

The $\overline{\text{DBUSEN}}$ (Data Bus Enable) line, pin 25, permits external control of the three-state data bus. When HIGH, pin 25 causes the data bus to appear as a high impedance; when LOW, the bus operates normally. The next eight pins, 26 to 33, form the 8-bit bidirectional data bus. Pin 23 indicates the flow of data on the bus. From pin 34, the INTACK line, a HIGH output indicates an interrupt request is being handled.

The RUN/$\overline{\text{WAIT}}$ output signal from pin 35 indicates the processor status. When the 2650 is executing an instruction, the line is HIGH (in the RUN state), and when the processor is halted by



3. **By using the programmable serial (a) or parallel** (b) interface circuits you can simplify the over-all circuit design. The serial interface has 16 programmable baud rates and the parallel interface has three 8-bit ports, one of which can also act as a serial port or timer.



a pause instruction the line goes LOW ($\overline{\text{WAIT}}$ state).

Pin 36 is the $\overline{\text{OPACK}}$ (Operation Acknowledge) input line and it accepts inputs in response to the OPREQ signal. It is used to control timing sequences between different speed memories and the processor.

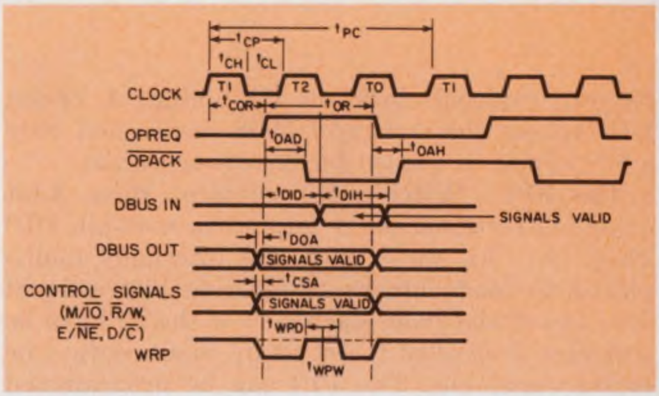
You can temporarily stop the processor with the $\overline{\text{PAUSE}}$ line (pin 36). When the line is driven LOW, the 2650 finishes its current instruction and enters the WAIT state.

The clock input of pin 38 accepts positive-going pulses. Three clock periods make up one processor cycle. Direct instructions are two, three or four processor cycles long and indirect addressing adds two more processor cycles to the direct instruction times.

A simple 5-V supply is all that has to be connected to pin 39. The last pin on the 2650, pin 40, is the FLAG output line. This output indicates the change of state of the FLAG bit in the PSW register.

Support circuitry is simple

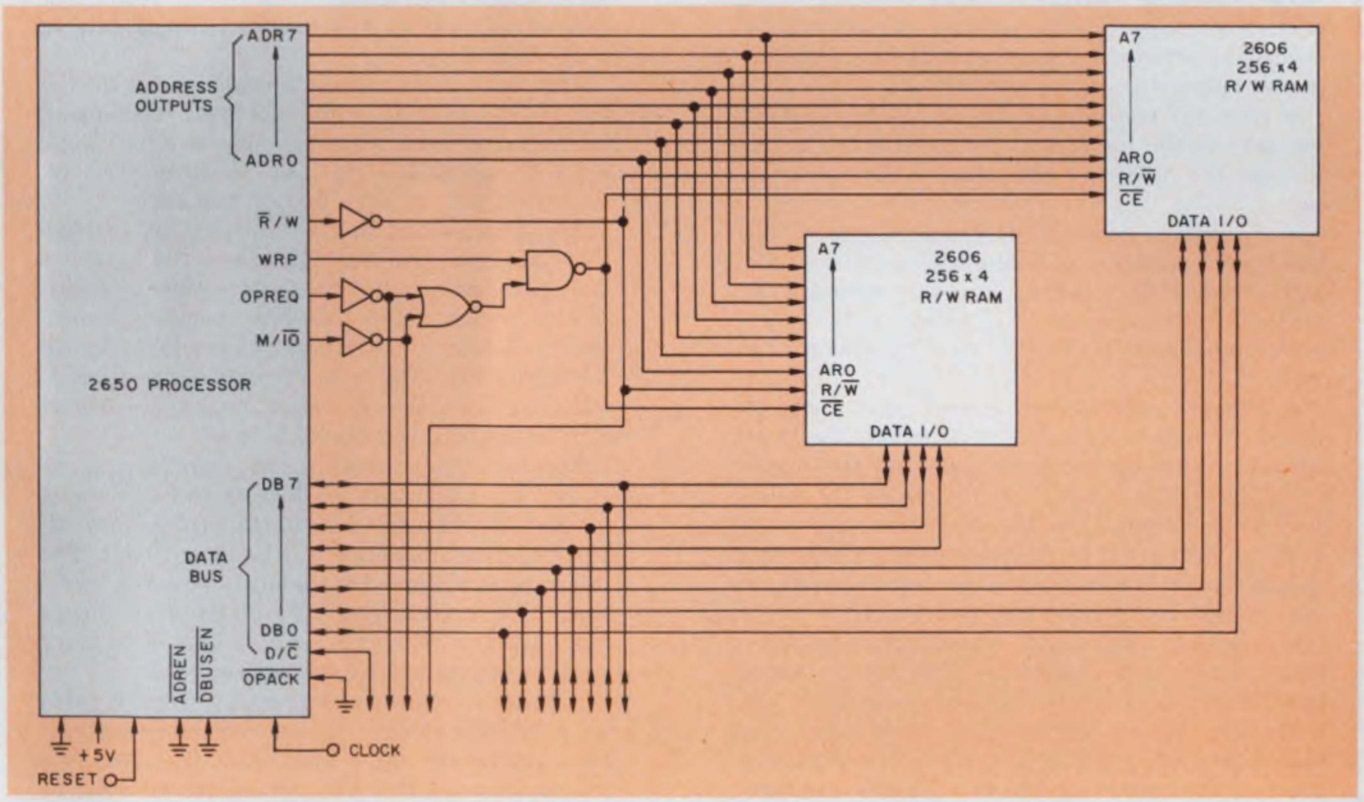
Since all inputs and outputs of the 2650 are TTL compatible, standard logic circuits can be used for all interface requirements. The two specialized interface circuits mentioned earlier—the PCI and PPI—offer interfaces that are software alterable (rather than hardware alterable) for parallel and serial data applications.



4. **There are only half-a-dozen signals** that are used to control the different memory circuits and peripherals that connect to the 2650.

The PCI (Model 2651) is a universal synchronous/asynchronous data-communications controller that supports almost any serial-data communications link in full-duplex or half-duplex modes (Fig. 3a). It accepts serial data from a peripheral and converts it to parallel data for the 2650. Inside the 2651 are a baud-rate generator, a modem controller, data-transmit and receive buffers and support control logic. The baud-rate generator has sixteen commonly used baud rates that are software selectable.

The transmitter and receiver sections of the 2651 can operate simultaneously and the baud-rate generator can accept external clocks or use



5. **Adding memory circuits to the 2650 is simple**—just connect the address and data busses to the circuits and the R/W, M/IO OPREQ and WRP lines; additional memory uses the higher-order address line.

its own internal clock for all timing. A 28-pin DIP houses the n-channel MOS device and only a 5-V supply is needed for circuit operation.

The PPI (Model 2655) contains three 8-bit quasi-bidirectional ports for I/O in a 40-pin DIP (Fig. 3b). All three ports are internally multiplexed to feed onto the 8-bit-wide bidirectional data bus of the 2650. Each port of the PPI can be software controlled to act as an input, output or bidirectional bus. The PPI can be programmed to function in five major I/O operating modes: static, strobed, bidirectional, serial or serial/timer.

One port of the 2655 can act as a serial I/O. A 3-MHz programmable timer or event counter is also available on the serial port to aid in timing external events. All lines are TTL-compatible.

To use either of these circuits, just set up the control words in your program and load the program into the 2650 memory. You can even change the port's function in mid program, depending upon your application. An interrupt request from

Instruction set and addressing schemes

The instruction set of the 2650 contains 75 instructions, about 40% of which are arithmetic. The arithmetic instructions include add, subtract, compare and Boolean operations, each of which can be executed using any one of eight different addressing modes. Another 30% of the instruction set contains branch operators that can be used with six of the addressing modes.

The remaining 30% of the instructions include I/O operations, status-register manipulation commands, a decimal-adjust instruction and a HALT directive.

The multiple addressing modes of the 2650 permit you to reduce the number of instructions needed to perform a desired operation. The different addressing modes include:

- *Register addressing:* In this mode the first two bits of the instruction byte define the register and the other six bits contain the operation code.
- *Immediate addressing:* The first byte of this two-byte instruction contains the operation code and register designation, and the second byte contains the data to be used as one of the operands during execution of the first byte operation code.
- *Relative addressing* (direct and indirect modes): In this two-byte instruction, the first byte contains the operation code and the register address. The second byte contains the relative displacement from the current memory address in a seven-bit two's complement coding. The eighth bit of the second byte defines whether the address is direct or indirect.
- *Absolute addressing* (nonbranch instructions, direct and indirect): This is a three-byte instruction, where the first byte holds the operation code in the six most significant bits and a two-bit Index or Argument register address in the remaining two bits. The second byte is divided into three parts: the highest order bit determines whether direct or indirect addressing is to be used, the next two bits determine how the effective address will be calculated—indexed only, indexed with auto increment/decrement, or nonindexed—and the lower five bits contain the uppermost part of a 13-bit address. The third byte contains the lower eight bits of the 13-bit address.
- *Absolute addressing* (branch instructions, direct and indirect): This instruction is almost identical to the nonbranch instruction, except that there are no index control bits. The second byte contains the single control bit for direct or indirect addressing and the seven upper bits of a 15-bit address.

The fixed instructions permit true indexing and have optional auto increment/decrement. Each instruction requires one, two or three bytes to accomplish its task. However, I/O instructions only require one or two bytes.

The first, second and third bytes of instructions are read into the 2650 from the data bus and are loaded into the instruction register, holding register and data-bus register, respectively. An internal ROM and random logic decode the words. The first byte of each instruction always specifies the operation to be performed and the addressing mode to be used.

Automatic incrementing and decrementing of an index register can be done in the arithmetic indexed instructions. All branch instructions except indexed branching can be conditional. The interrupt is a single-level address-vectored interrupt. This means that the interrupting device can force the 2650 to execute code at a memory location determined by the device.

Register-to-register commands only require a one-byte directive; register-to-memory instructions are two or three bytes long. The two-byte commands use either the immediate or relative addressing modes.

a peripheral is one way to do this.

When an external interrupt occurs on the $\overline{\text{INTREQ}}$ line, the μP branches to any of 128 possible memory locations, as defined by an 8-bit vector supplied by the interrupting device.

Since the interrupting peripheral specifies the interrupt subroutines in a relative-address format, the vector can point to any location that is within +63 or −64 bytes of page zero, byte zero of memory. (Negative relative addresses wrap around the memory, so the address is contiguous.) The peripheral can also specify whether the subroutine address is direct or indirect.

System interconnects are straightforward

Aside from the connections to the data and address busses there are about half a dozen signal lines that make up the control bus (Fig. 4). For instance, during a memory-read operation, the OPREQ and M/$\overline{\text{IO}}$ lines go HIGH and the $\overline{\text{READ}}$/

Mnemonic		Definition
Arithmetic operations		
ADD	Z	Add to register zero w/wo carry
	I	Add immediate w/wo carry
	R	Add relative w/wo carry
	A	Add absolute w/wo carry
SUB	Z	Subtract from register zero w/wo borrow
	I	Subtract immediate w/wo borrow
	R	Subtract relative w/wo borrow
	A	Subtract absolute w/w borrow
DAR		Decimal adjust register
AND	Z	AND to register zero (r ≠ 0)
	I	AND immediate
	R	AND relative
	A	AND absolute
IOR	Z	Inclusive OR to register zero
	I	Inclusive OR immediate
	R	Inclusive OR relative
	A	Inclusive OR absolute
EOR	Z	Exclusive OR to register zero
	I	Exclusive OR immediate
	R	Exclusive OR relative
	A	Exclusive OR absolute
COM	Z	Compare to register zero arithmetic/logical
	I	Compare immediate arithmetic/logical
	R	Compare relative arithmetic/logical
	A	Compare absolute arithmetic/logical
RRR		Rotate register right w/wo carry
RRL		Rotate register left w/wo carry
Branch instructions		
BCT	R	Branch on condition true relative
	A	Branch on condition true absolute
BCF	R	Branch on condition false relative
	A	Branch on condition false absolute
BRN	R	Branch on register nonzero relative
	A	Branch on register nonzero absolute
BIR	R	Branch on incrementing register relative
	A	Branch on incrementing register absolute
BDR	R	Branch on decrementing register relative
	A	Branch on decrementing register absolute
ZBRR		Zero branch relative, unconditional
BXA		Branch indexed absolute, unconditional (see note)
BST	R	Branch to subroutine on condition true, relative
	A	Branch to subroutine on condition true, absolute
BSF	R	Branch to subroutine on condition false, relative
	A	Branch to subroutine on condition false, absolute
BSN	R	Branch to subroutine on nonzero register, relative
	A	Branch to subroutine on nonzero register, absolute
ZBSR		Zero branch to subroutine relative, unconditional
BSXA		Branch to subroutine, indexed absolute unconditional (see note)
RET	C	Return from subroutine, conditional
	E	Return from subroutine and enable interrupt, conditional
I/O, program status and load/store instructions		
WRTD		Write data
REDD		Read data
WRTC		Write control
REDC		Read control
WRTE		Write extended
REDE		Read extended
HALT		Halt, enter wait state
NOP		No operation
TMI		Test under mask immediate
LPS	U	Load program status, upper
	L	Load program status, lower
SPS	U	Store program status, upper
	L	Store program status, lower
CPS	U	Clear program status, upper, masked
	L	Clear program status, lower, masked
PPS	U	Preset program status, upper, masked
	L	Preset program status, lower, masked
TPS	U	Test program status, upper, masked
	L	Test program status, lower, masked
LOD	Z	Load register zero
	I	Load immediate
	R	Load relative
	A	Load absolute
STR	Z	Store register zero (r ≠ 0)
	R	Store relative
	A	Store absolute

Note: Index register must be register 3, or 3'.

WRITE line goes LOW. In return, the $\overline{OPACK}$ line from the memory goes LOW and then the data from the memory appear on the data bus. The OPACK line is a handshaking signal, and must be valid (HIGH) for the data to have meaning.

The FLAG and SENSE lines are I/O ports that can directly output or input one bit of data without any external address decoding or synchronizing signals. The circuit of Fig. 1 shows how these two lines can be used to sense character inputs from a TTY port. The FLAG can be used as a serial output channel, as an extra address bit for wider addressing range, as a switch or toggle output to control external logic or external functions or can be used as a pulse generator for polling applications. The SENSE line, of course, can be used as a serial input channel, a sense switch input, a break signal to a running program, or an input for a yes/no signalling routine from external devices.

The 2650 has a total addressing capability of 32,768 bytes of memory, but in most cases has a direct-addressing instruction range of 8192 bytes —using only the lower 13 bits of the address word. To make it possible to access the full 32-k bytes, a paging scheme is used to break the memory into four 8-k byte pages, where the ADR13 and 14 lines are used to determine the page.

Fig. 5 shows a complete interface between the 2650 and two 2606, 256 × 4 RAMs, organized as a 256 × 8 R/W memory. For a larger memory, the next few address lines can be bussed to the RAM inputs.

Almost any memory can be used

Available memory circuits include the 2602 (1 k × 1) and the 2606 (256 × 4) static RAMs, the 2608 (1-k × 8) ROM and the 82S115/123/129 (512 × 8, 32 × 8 and 256 × 4) PROMs. The RAMs are available with access times ranging from 500 ns to 1 μs, and are housed in 16-pin DIPs. The ROM has a 650 ns access time and comes in a 24-pin DIP. The PROMs, made using Schottky-TTL processing, have access times of 35 ns, typical. They are also available in 16 or 24-pin DIPs. Memories made by other companies can also be used with the 2650, but only memories with access times of less than 800 ns allow the μP to operate at its maximum speed.

The other support circuits include the 8T26 quad transceivers, the 8T31 8-bit bidirectional port and the 8T95, 96, 97 and 98 hex buffers/inverters. All of these support circuits offer pnp inputs and have currents of only 200 μA instead of the 1.6 mA that standard TTL offers. This permits more circuitry to be connected to the 2650 busses without overloading the internal sinks.

To help you with basic system development, Signetics offers several development aids for both hardware and software:

- The 2650PC1001: A microprocessor prototyping card that contains a complete microcomputer on a single printed-circuit card. On the board is the 2650 μP, a control and R/W memory, an I/O port, a clock and all necessary buffering and interface circuits.
- The 2650PC2000: A 4-k byte memory card that is compatible with the 1001. It contains 32, 21L02 1-k × 1 static RAMs. Decoding is provided to select any block of 1-k × 8 and to distinguish cards in a multicard system.
- The 2650DS2000: This is a complete μP demonstration system that can accept one PC1001 and one PC2000. It has a built-in power supply and serial interfaces for RS-232 and TTY inputs.
- The KT9000: This is a microprocessor prototyping kit that contains the 2650 μP and enough support circuits to permit the development of a small system.
- The ABC1500/9500: The adaptable board computer is a modular microcomputer that contains the μP, memory, I/O ports and support circuitry. It also permits user designed circuits to be directly wired on the board. Two forms of the ABC system are available: The 1500 fully assembled version and the 9500 kit.

For software development Signetics has the TWIN microcomputer. It has two central processors so that user-developed programs are kept completely separate from operating programs. This provides a completely "crash-proof" system —no accidental erasing or disruption of operating software can occur as a result of a mistake or accident.

For software support and development debugging several different programs are available:

- Assembler: The 2650 assembly language (PIPASM) is a symbolic language designed to simplify the writing of programs for the 2650. It is written in Fortran IV and is modular—it can be executed in an overlay mode if the processor memory can't handle the entire program. Two passes are used to generate the symbol table, issue error messages, produce a program listing and computer-readable object listing.
- Simulator: The 2650 simulator program (PIPSIM) is a Fortran IV simulation of how the 2650 operates.
- Signetics Higher Level Language (PLμS): A microprocessor programming language which the programmer uses to replace many lines of machine code with a single statement. The PLμS compiler is available in 16 or 32-bit formats and also on GE and NCSS time-sharing services. ■■

Previous articles in this series covered the 8080, F-8 and 6800 microprocessors. The next article will discuss the RCA CDP1802.

INTERFACE ACE

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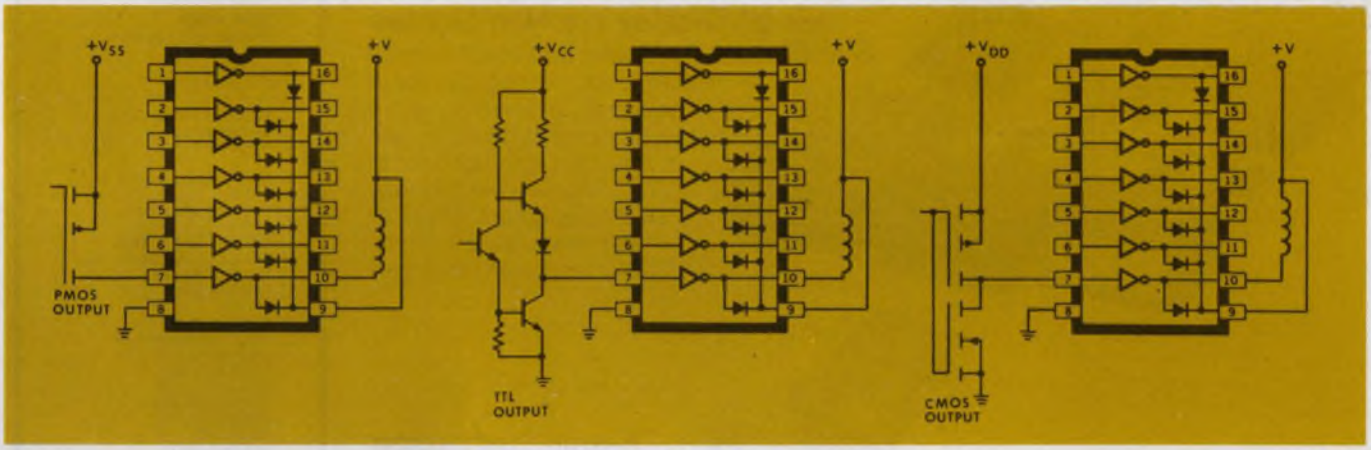

A new exclusive Sprague development, Series 2000 Transistor Arrays are high-voltage, high-current integrated circuits comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. They feature open collector outputs and integral suppression diodes for inductive loads.

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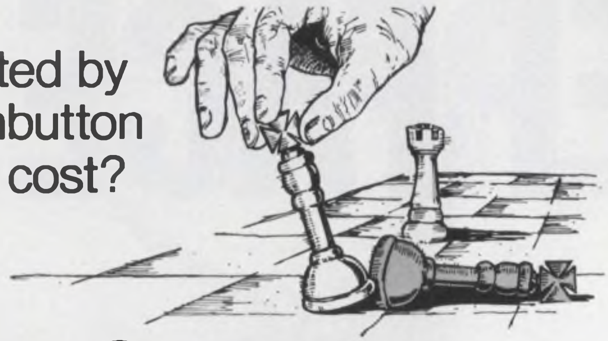

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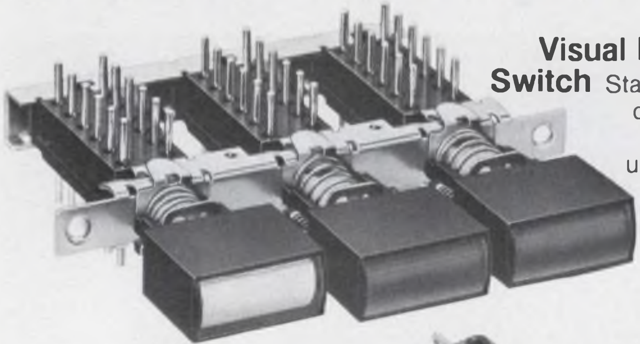

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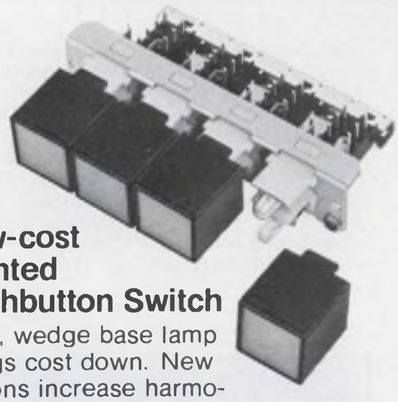

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Design a μP analyzer to handle that 'after-the-design' test problem. With the analyzer, you can capture data and trace both hardware and software.

For a few hundred dollars, you can put together an analyzer that traces the operation of a completed microprocessor-based product.

Although the analyzer is designed to monitor 8080 systems, its concept can be applied to other μPs—the PPS4, for example, a μP as different from the 8080 as you can get.

If you'd like, you can call the analyzer a snapshot test box (STB) since the unit captures, or takes pictures, of the information on the system's address, data, and status busses.

With the STB, you can avoid the use of prototyping equipment for testing. Although widespread, that approach is self defeating because the development equipment performs the CPU and memory functions—the very things that need monitoring in the final product.

Packaging of the STB can range from a bench-console to a portable unit for field-service.

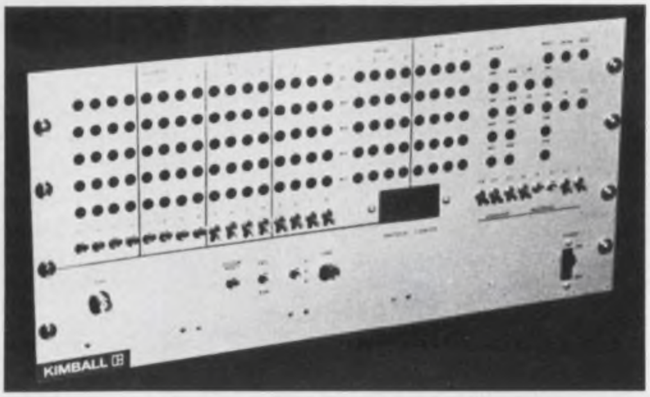
The STB captures information without affecting the operation of the 8080, except for an additional 20-μA/0.8-mA (sink/source) load on each of the bus lines. Displaying the snapshot on the front panel are 140 LEDs arranged in five rows, M_1 to M_5, corresponding to the five-machine-cycle maximum of the 8080's instructions (Fig. 1).

Each row is divided into address-bus, data-bus and status LEDs. Status signals monitored include: hold acknowledge (HLDA), interrupt acknowledge (INTA), memory read (MR), memory write (MW), stack read (SR), stack write (SW), input read (IR) and output write (OW). Because not all 8080 status modes can occur for a given machine cycle, there is no SR LED in rows M_1 and M_5.

Loading the 'camera'

To take a snapshot of any given instruction address, first you set 16 front-panel switches to the address binary number. Another control—called the address-direction switch—provides a snapshot of the instruction executed just before that set on the address switches.

Larry Bruni, Senior Associate Engineer, Kimball Systems, 151 Cortlandt St., Belleville, NJ 07109.



1. **Rows of LEDs display transactions** that occur on a μP's address, data and status busses. The counter shows how many times a given address is executed.

With the direction switch, you can trace backwards through a program and determine the point from which a subroutine was called in the main program loop. Such capability is especially useful when calls are numerous and spread out.

The P setting of the address-direction switch results in a snapshot of the present instruction, and still another position (F) snapshots the following instruction for forward program tracing.

A three-digit decimal counter displays the number of times a snapshot occurs at a given address, up to a number set by the eight binary multiplier switches on the front panel. With the multiplier at zero, each pass through a set instruction is captured and counted. Other multiplier settings determine the number of instruction passes before a snapshot is taken.

When the counter reaches maximum, all decimal points light up, and the counter remains at .9.9.9 until it is zeroed by the STB reset switch.

Note that even though the counter stops incrementing at maximum count, a snapshot still occurs for each pass through the selected address. The reset switch also lights all front-panel indicators as a self test. When you want to capture a previous instruction, the multipliers must be set for a count greater than zero.

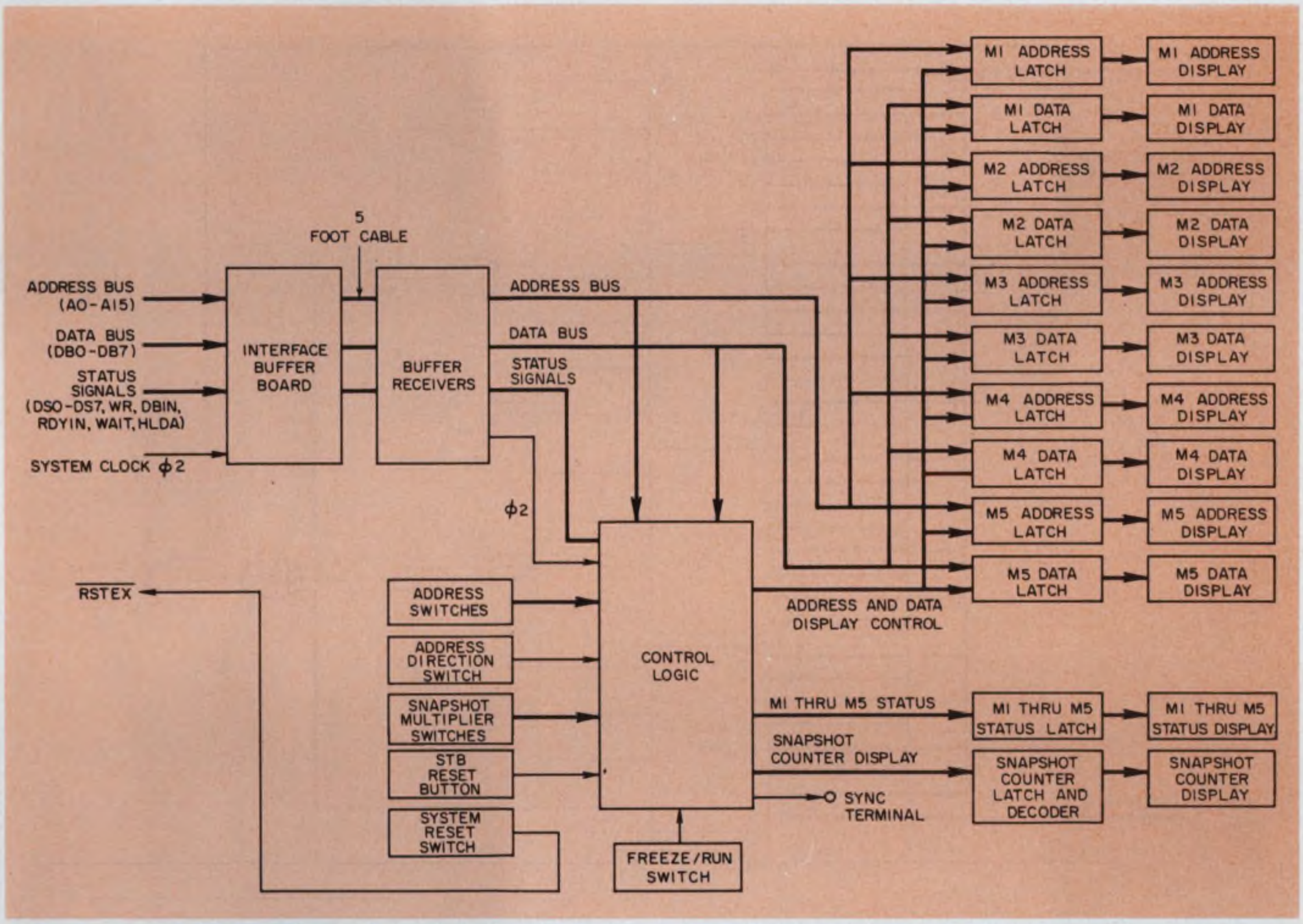
What if you don't know where a program is? Another feature of the STB allows random shots of executed instructions. Set the address direction for "present," the multiplier for "one" and place the freeze/run switch in FRZ position.

The next instruction executed by the μP will be snapped, regardless of the setting of the address switches. Now push the reset button, and you can take random pictures. Set the multiplier to zero, and a snapshot occurs for every instruction fetch.

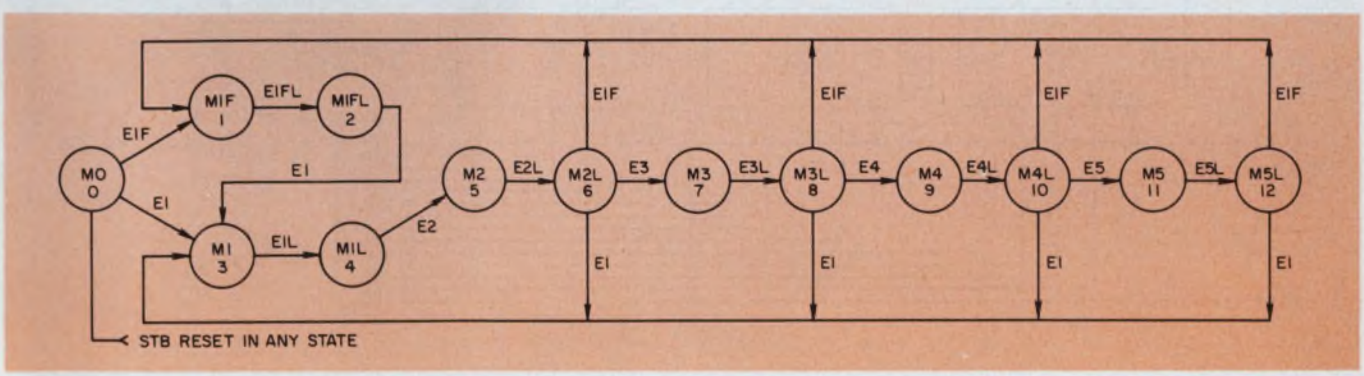
The resulting display on the LEDs is a blur as every instruction runs through. With the "blur," you can spot shorts on bus lines, check if the program range is within limits and immediately know if the μP system is "on the air."

Another useful feature of the STB is a sync pulse that you can use to externally trigger an oscilloscope at the instant a snapshot occurs. You'll find the pulse most helpful when checking I/O operations, especially when you use the multiplier to isolate certain operations in a continuous program loop.

Fig. 2 shows a block diagram of the STB. Note that the system reset signal is the only output



2. **How the test box works:** Routing and logical processing of input signals is the job of the control-logic block, which is built around a state counter. Low-power Schottky is used throughout.



3. **A state counter keeps track** of μP machine cycles. The M numbers shown correspond to internal cycles of the 8080 μP. To isolate the various states, transition states are added between machine cycles.

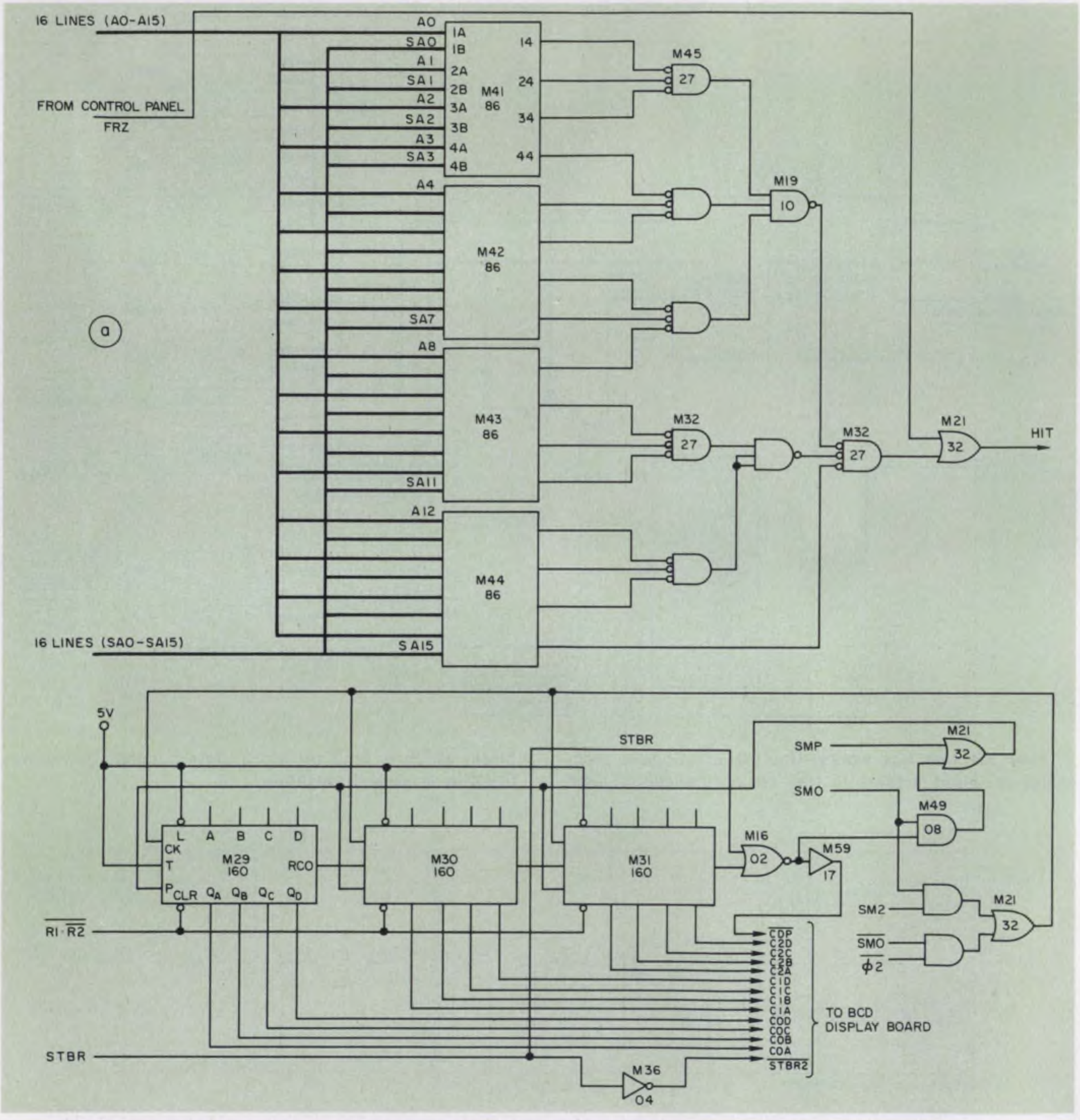
to the μP system under test. Except for the control logic, the electronics of each block are straightforward. Wherever possible, low-power Schottky logic is used (the 74LS prefix is omitted on the schematics).

Watching over machine cycles

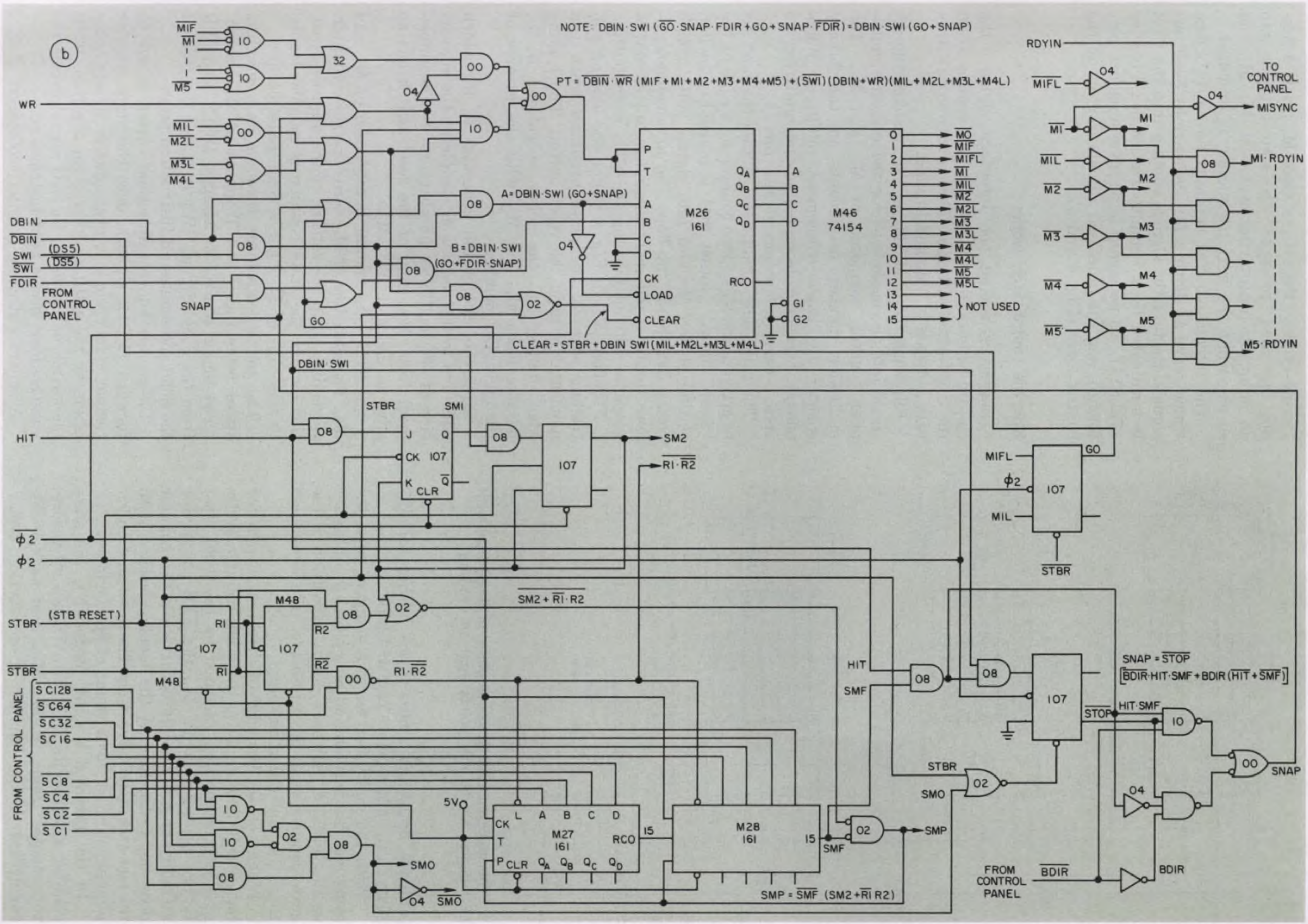
Heart of the control logic is a state counter, with the M numbers of each state corresponding to 8080 machine-cycle numbers (Fig. 3). A transition state (suffix L), added between each machine cycle, isolates one state from the next.

With the address-direction switch in position, P, and the snapshot multiplier set for a count of one or zero, the control logic waits in state M_0 and compares the 8080 address bus with the STB address switches. When the two addresses are identical, a "hit," the counter advances to M_1.

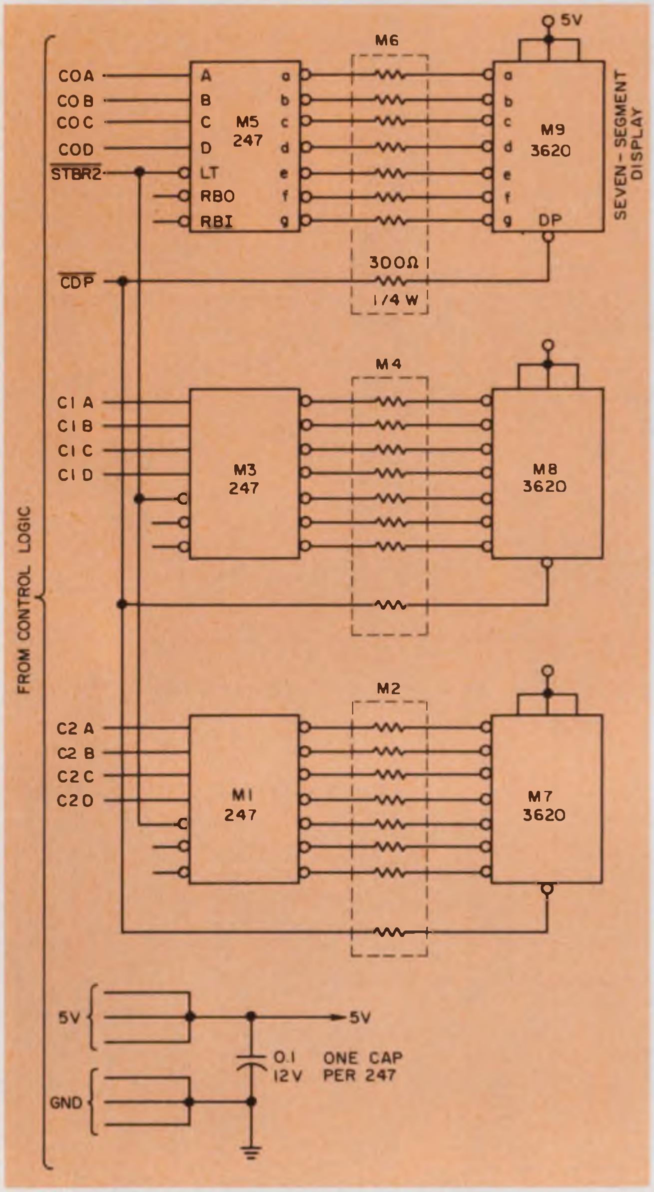
Each subsequent machine cycle taken by the 8080 instruction advances the counter to its next state. If the instruction contains three cycles, the counter traverses M_0-M_1-M_{1L}-M_2-M_{2L}-M_3-M_{3L}-M_0. At counts M_1, M_2, and M_3, the information on the



4. **Control logic forms the various** functional signals of the test box. The "hit" signal indicates an address match (a); and the Snap and Go signals are used to activate and cycle the state counter ("b" on facing page).



b
NOTE: DBIN·SWI (GO̅·SNAP·FDIR + GO + SNAP·FDIR̅) = DBIN·SWI (GO+SNAP)
PT = DBIN̅·WR̅ (MIF + MI + M2 + M3 + M4 + M5) + (SWI̅) (DBIN+WR) (MIL + M2L + M3L + M4L)
A = DBIN·SWI (GO+SNAP)
B = DBIN·SWI (GO + FDIR̅·SNAP)
CLEAR = STBR + DBIN SWI (MIL + M2L + M3L + M4L)
M26 161
M46 74154
NOT USED
WR
DBIN
DBIN̅
SWI (DS5)
SWI̅ (DS5)
FDIR̅
FROM CONTROL PANEL
SNAP
GO
DBIN·SWI
RDYIN
TO CONTROL PANEL
MISYNC
MI·RDYIN
M5·RDYIN
HIT
STBR
SMI
SM2
RI̅·R2̅
MIFL
ϕ2
MIL
STBR̅
ϕ̅2̅
STBR (STB RESET)
M48
SM2 + RI̅·R2
RI̅·R2̅
FROM CONTROL PANEL
SC128 SC64 SC32 SC16 SC8 SC4 SC2 SC1
5V
M27 161
M28 161
SMF
SMP
SMO
SMO̅
SMP = SMF̅ (SM2 + RI̅ R2)
SNAP = STOP̅
[BDIR̅·HIT·SMF + BDIR (HIT̅ + SMF̅)]
HIT·SMF
STOP̅
BDIR̅
BDIR



5. **The snapshot counter** is composed of three 7-segment LED digits. All decimal points light on overflow.

address, data, and status buses latches for display on the appropriate row of LEDs.

With the multiplier set to a count of zero, the state counter activates at every hit. A multiplier setting greater than zero delays activation of the state counter until the number of hits is one less than the multiplier reading.

When you set the address-direction switch for backwards tracing (B), the state counter cycles at every instruction executed by the 8080. Just before cycling through M_1, the STB checks for an address hit. On hit occurrence, the counter does not cycle, leaving the display latched with the last executed instruction. The snap-shot multiplier must be set for a count of one or more.

In the forward tracing mode (F), the state counter again waits for a hit. When a hit occurs, the counter cycles M_0-M_{1F}-M_{1FL} and back to M_0 regardless of the number of instruction cycles. During cycling, the unique state M_{1FL} sets a flip-flop that then "prompts" the state counter into an information-capturing cycle—M_1-M_{1L}-M_2, and so on—when the next instruction is executed.

The interface-buffer contains seven 74LS04s, which serve as drivers for the various 8080 bus signals. Each of the signals coming into the STB is terminated by a Schmitt-trigger hex inverter (74LS14). All necessary logic inversions are performed, and the processed signals then go to the control logic (Fig. 4 and 5).

How the control logic works

Besides receiving the interface signals, the control logic receives all of the lines coming from the front-panel switches. The signals on the lines vary between 5 V dc and ground.

Flip-flops SM_1 and SM_2 in Fig. 4 shape the hit signal into an enable level for the snapshot multiplier counter, composed of M_{27} and M_{28}. The multiplier number decrements in the binary counter by two's-complement addition. When enough hits have decremented the multiplier to zero, a carry-out occurs at M_{28}, pin 15.

The carry-out, signal SMF, allows the next hit to activate the STB state counter by means of the "Snap" signal. Notice that a multiplier switch setting of zero decodes into signal SMO, which resets the "Stop" flip-flop. The arrangement allows the first and each subsequent hit to take a snapshot without pushing the STB reset button.

Flip-flops M_{48} in Fig. 4 define the leading and trailing edges of the pulse produced when you momentarily push the reset button. The leading edge defined by the logic operation, $R_1 \cdot \overline{R_2}$, parallel loads M_{27} and M_{28} with the inverse of the multiplier number.

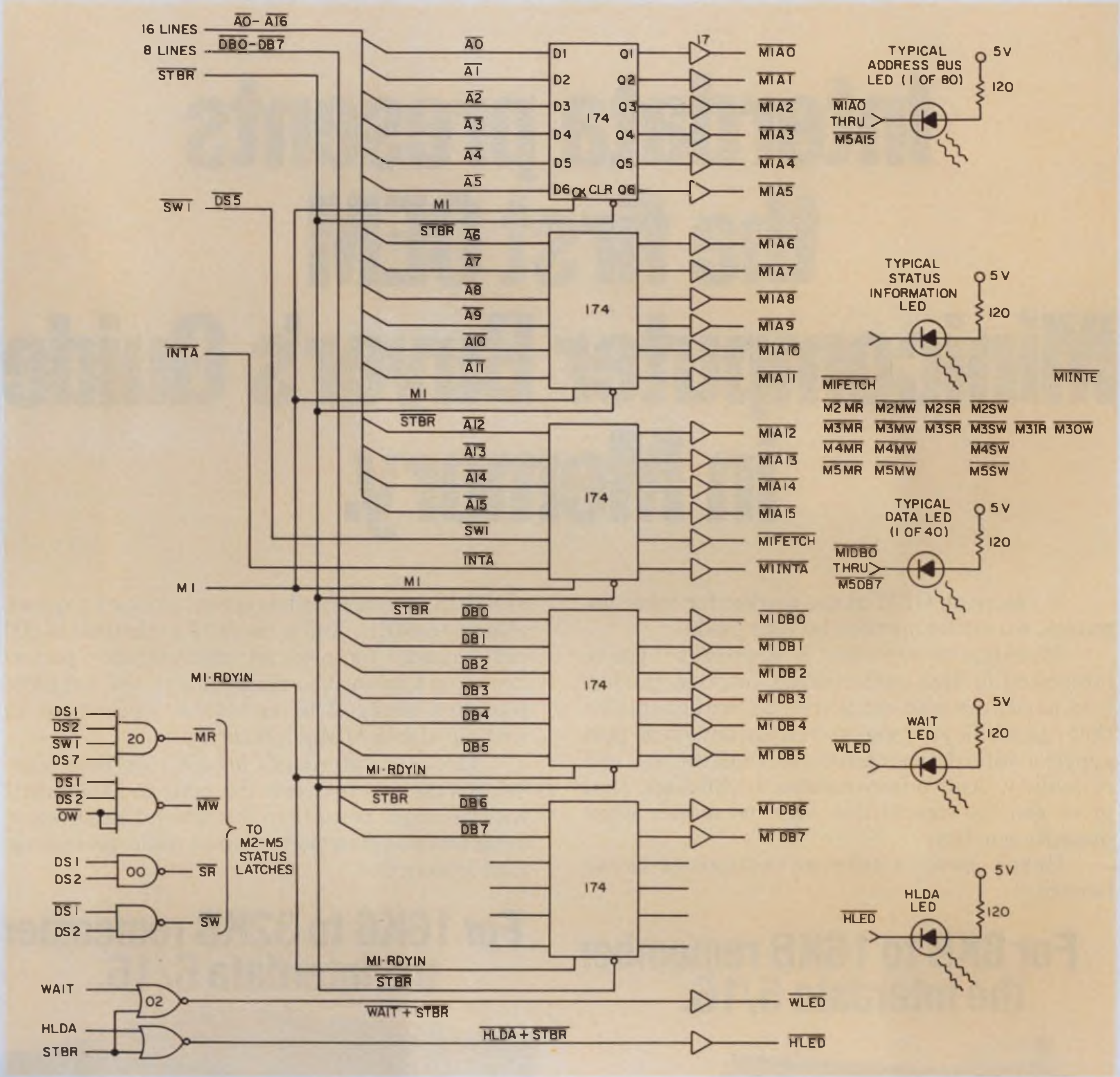
Release of the button generates $\overline{R_1} \cdot R_2$, which adds one to the count and completes the conversion of the multiplier number into two's-complement form. Bouncing of the reset switch has no adverse effect on M_{27}, M_{28}.

The STB state counter is composed of M_{26} and M_{46}. The clear line of M_{26} zeros the state counter. Depending upon the setting of the address-direction switch, the state counter is parallel loaded to state M_{1F} or M_1 when a Snap pulse occurs.

The counter advances through its remaining states when the P and T inputs of M_{26} are enabled under control of signals DB1N and WR from the 8080. Signal SW1 is status bit DS5 of the 8080 and defines an instruction fetch.

Unless the address-direction switch is set to forward (FD1R signal), once the state counter completes its cycle it is prevented from any other action by the setting of the Stop flip-flop. With the switch on forward, the GO signal cycles the state counter on the next instruction.

A separate decimal counter, composed of M_{29},



6. **Latches and drivers for the display** are activated by the state-counter, with a delay to account for system-memory access time. All segments and decimals are lighted to test operation.

M_{30} and M_{31} in Fig. 5, forms the front-panel snapshot-counter display. Two modes of counter operation are possible, depending on the state of signal SMO. When SMO is true (snapshot multiplier set at zero) the counter increments on every SM2 pulse until it overflows.

Overflow disables the counter, keeping the front-panel display at .9.9.9. When you set the snapshot multiplier to a number greater than zero (SMO false), signal SMP increments the counter, and that limits the display to the number at which the single snapshot occurs.

Fig. 5 also shows the address-comparison logic used to produce the hit signal. Notice that the freeze signal, FRZ, from the control panel forces the hit signal to true. This causes an immediate snapshot of the next instruction.

As a test, the STBR signal lights all segments and decimal points on the snapshot counter, a seven-segment, binary-coded decimal display (Fig. 6). In normal operation, the decimal points are lit when the counter overflows.

Latches for the LEDs and drivers are strobed by the appropriate machine-cycle signal from the state counter (Fig. 7). The Ready signal (RDYIN) of the 8080 delays data-bus capture to compensate for the access time of the memory in the system under test. ■■

Interdata presents the first OEM Minicomputer Buyer's Guide in Memory.

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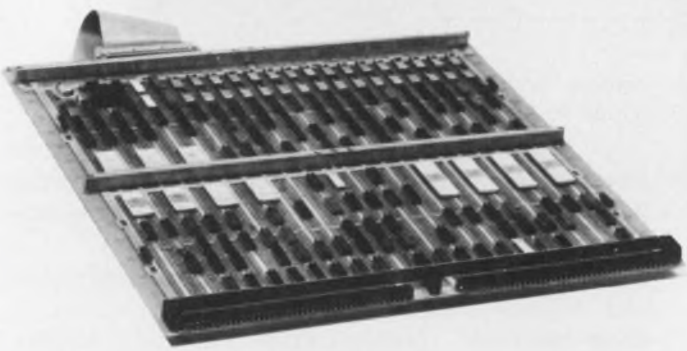

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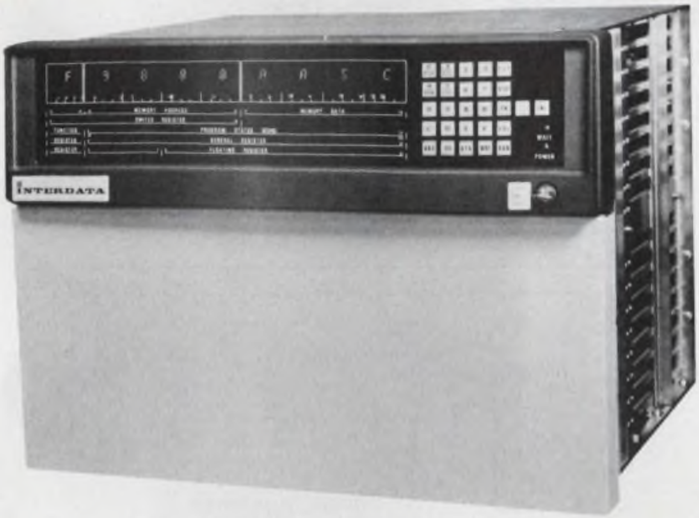

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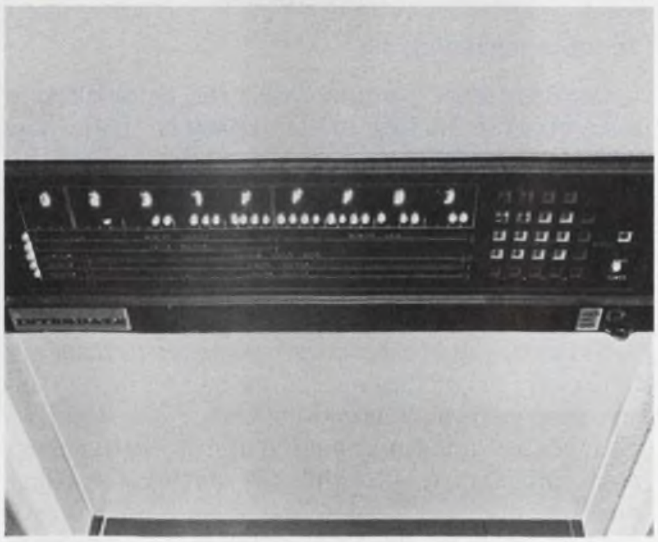

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CIRCLE NUMBER 48

Go from flow chart to hardware.

This approach to the design of complex ROM and PLA logic networks bypasses Boolean equations and truth tables.

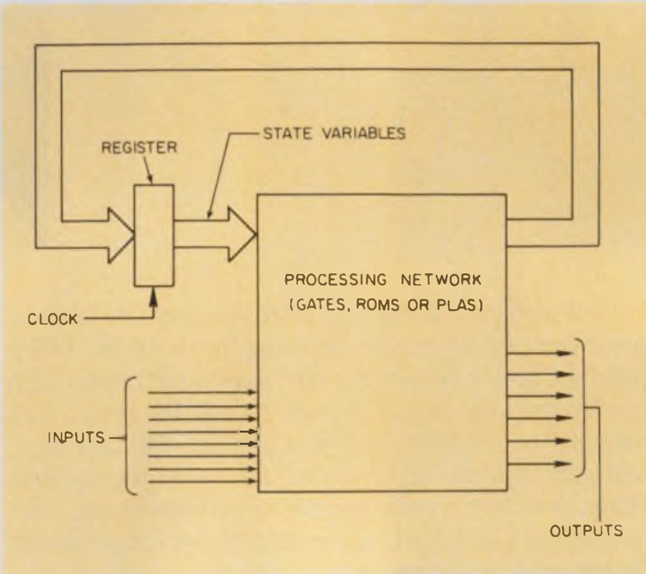
Read-only memories (ROMs) and programmable logic arrays (PLAs) are attractive alternatives to random logic, especially in applications too fast or too simple for a microprocessor. If the design needs only one ROM or PLA, the standard approach using Boolean equations and truth tables is useful, but tedious. For a larger design, some real difficulties arise in partitioning the equations into subsets that "fit" each ROM or PLA, and then somehow interconnecting to generate the correct composite logic.

Why not try a flow chart? Partitioning is easily accomplished right on the chart, and the chart is very effective as a graphic map of the logic and as a minimization tool. You go directly from the chart to hardware implementation without writing a single Boolean equation, and the effect on hardware can be seen immediately if you change the flow chart.

Control logic is the nerve center of most digital designs. A typical construction is shown in Fig. 1. The processing network, consisting of gates, ROMs or PLAs, receives inputs from the rest of the system. State variables, synchronized with the system clock, are also inputs. The network generates new state variables and outputs to control the surrounding logic. To design the network, conventional techniques usually begin with state diagrams from which optimized design equations are derived. These are then implemented with gates and inverters.

Parts count can be reduced by using ROMs or PLAs instead of individual gates. A 4-k ROM (or programmable ROM) configured 512 × 8, will handle up to nine inputs and eight outputs. For up to 16 inputs and state variables, use a PLA or field PLA. Using a PLA instead of a ROM is a little more complicated because there's a limit on the number of product terms a PLA can handle, but these can be minimized by mathematical optimization techniques. Even if more than one ROM or PLA is required, a flow chart can still handle it.

David W. Johnson, Senior Engineer, Communications Development Div., Control Data Corp., Santa Ana, CA 92704.



1. **Digital logic in the processing network** monitors and controls a system based on MSI and LSI devices.

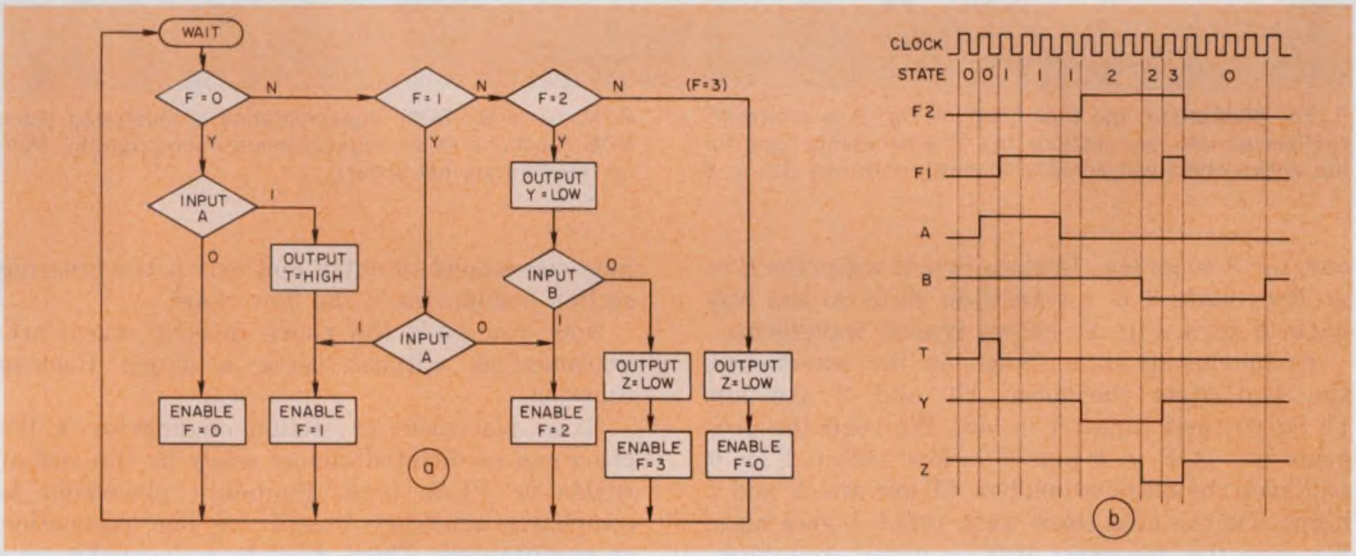
Set up a microprogram

Consider Fig. 1 again. Treat the network as a microprogram instead of combinational logic. The microprogram's basic task is to interrogate inputs and generate outputs (including state variables). Thus, it contains only two kinds of instructions:

1. Jump on input.
2. Activate output.

Further, the instructions are executed instantaneously (asynchronously) rather than one instruction per clock cycle.

By way of analogy, imagine an interactive computer program that begins by waiting for a human operator to type one line of data on a terminal. As soon as the line is typed the program speeds through its steps, examining the data typed, taking into account the values of internally stored parameters (state variables), comput-



2. **Flow chart (a) of a system that has two state variables,** F_1 and F_2; two inputs, A and B; and three outputs, T, Y and Z. Of the outputs, Y and Z are active-low and T is active-high. Typical waveforms are shown (b) as inputs and state variables change. For simplicity, the propagation delays are not shown.

ing new values for these parameters, generating output data, and then waiting for the next line of input data to be typed. This imagined program operates so fast that it has already returned to the "wait" mode before the human operator is ready to enter the next line of data.

The rate of entering new data corresponds to the clock rate of the circuit and its surrounding devices. At the beginning of each clock cycle new state variables and inputs are presented to the microprogram. It then speeds through its instructions, interrogating the inputs and state variables to generate new state variables and outputs before the next clock cycle begins.

The microprogram ("nano-program" is a better description) answers four questions during each clock cycle:

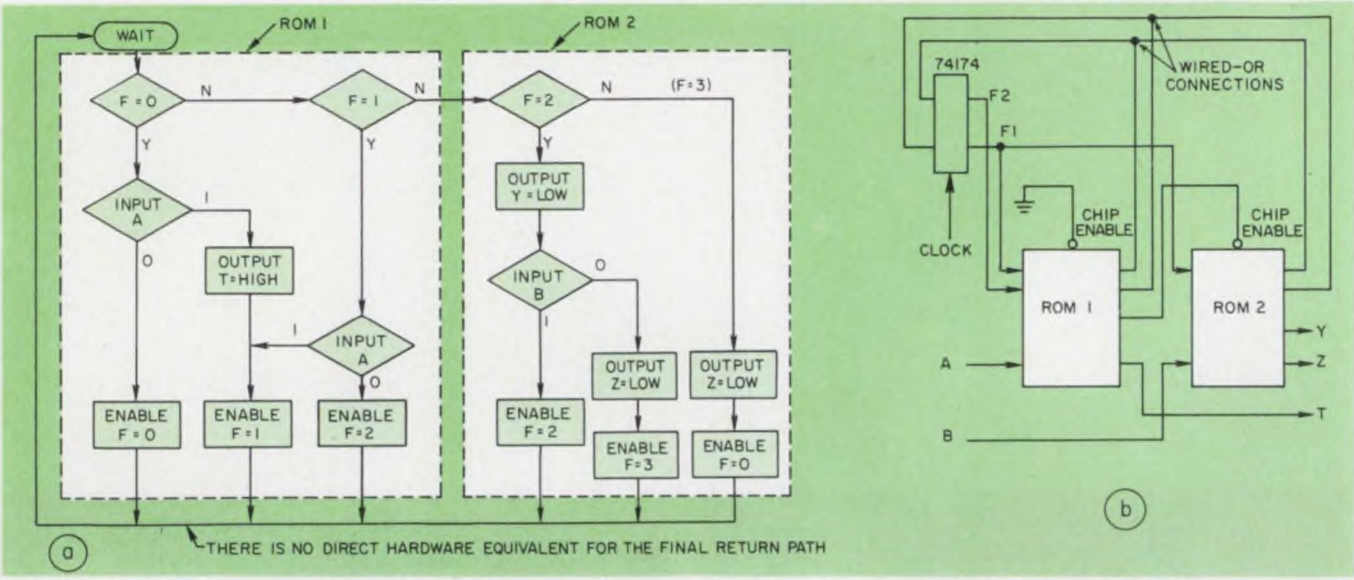
1. What is the circuit's present state, as indicated by the state variables?
2. Which inputs should be looked at in that state?
3. Which outputs should be activated?
4. Into what state should the circuit go on the next clock cycle?

During every succeeding clock cycle, the microprogram answers these four questions again.

Set up a flow chart

The microprogram can be represented by a flow chart (Fig. 2) with the same format as flow charts for actual computer programs. A "decision diamond" is drawn whenever the microprogram should interrogate an input or state variable. Wherever an output should be activated an "action rectangle" is drawn. Outputs not to be activated are omitted, with the understanding that they remain inactive unless explicitly activated. (Outputs may be either active-high or active-low.) Finally, a "wait oval" is drawn when the program should wait for the next clock cycle before proceeding.

Fig. 2 is an example of this kind of flow chart. It has four states, F = 0 through 3; two inputs, A and B; and three outputs, T, Y and Z. In state zero, the program waits for A to go high; in state



3. **For illustration, the flow chart** of Fig. 2 is arbitrarily partitioned into two sections (a). The necessary logic for the entire chart will actually fit easily into one 32 × 8 ROM, but a two-ROM implementation is illustrated. Each ROM functions as an asynchronous microprogram. Pull-up resistors are not shown.

one, for A to go low. In state two, it waits for B to go low; state 3 is a transition state on the way back to zero. Fig. 2b shows typical waveforms.

In the initial state shown on the waveforms, the two state variables, F1 and 2 are low (F = 0), and input A is low. We read the program as: If F = 0 and F is low, retain F = 0 and keep the outputs inactive (T low and Y and Z high). On the next clock state, input A goes high. We read the program: If F = 0 and A is high, turn T to high and shift to state F = 1. The remainder of the program may be read in similar fashion. ("Enable" means that the event does not occur until the next clock cycle.)

The flow chart is similar to an ordinary state diagram, but there is an important difference: state variables are treated as inputs rather than as switching nodes. Thus, the chart could have been drawn with four WAITs instead of four values of F. Each WAIT would then be equivalent to one state, but a flow chart free of embedded WAITs is easier to implement with ROMs or PLAs. When there is only a single WAIT at the beginning the remainder of the chart becomes totally asynchronous and more directly applicable to interconected ROM or PLA networks.

Partition the network

It's easy to partition the chart into actual ROMs or PLAs:

1. Section off the flow chart into ROMs (PLAs).

2. Turn ROMs (PLAs) on or off by other ROMs (PLAs). Use the chip-enable input of each ROM to activate or inhibit.

3. Let the inteconnections of chip-enable inputs correspond to entry and exit paths crossing section boundaries in the flow chart.

Now you have the chart directly hardware-implemented, without using a single Boolean equation.

Exact placement of section boundaries in the chart can be dictated almost solely by the size of ROMs or PLAs used. Boundary placement is completely arbitrary except for one restriction on partitioning: There must be no asynchronous closed loops. Thus, if one ROM controls enabling or addressing of a second ROM, the second ROM must not control enabling or addressing of the first ROM.

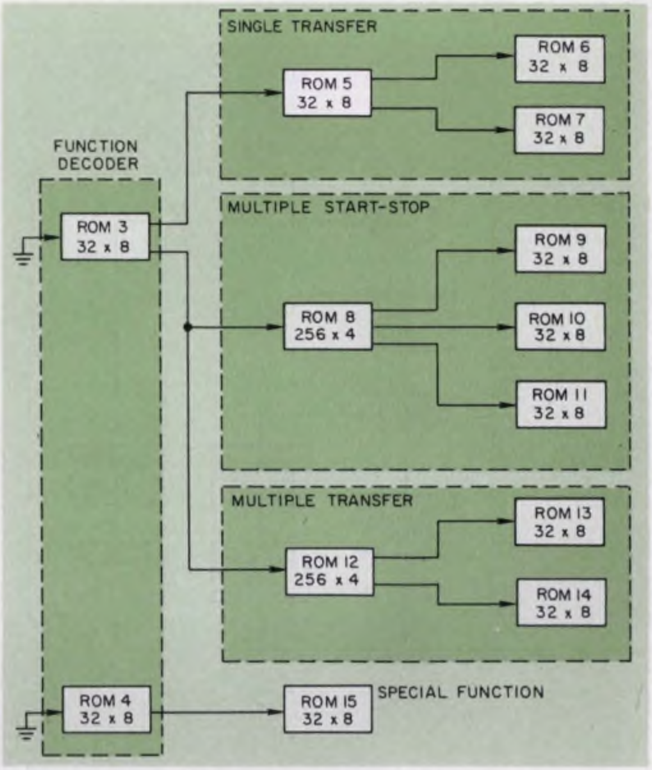
In Fig. 3a, we have partitioned the flow chart of Fig. 2. Fig. 3b shows the hardware implementation with two ROMs. Basically, that's all there is to it. Each ROM or PLA is functionally equivalent to an asynchronous microprogram. Link all the individual microprograms together using chip-enable signals, and you'll have a composite microprogram. If the complexity of the composite flow chart can be reduced, so can the number of ROMs or PLAs needed. If you change the flow chart you'll see the effect on hardware immediately because the correlation between flow-chart sections and individual ROMs and PLAs is one-to-one. If someone else has to take over your design, or diagnose malfunctions, the flow chart is probably far more helpful than equations or truth tables.

A complex network is designed

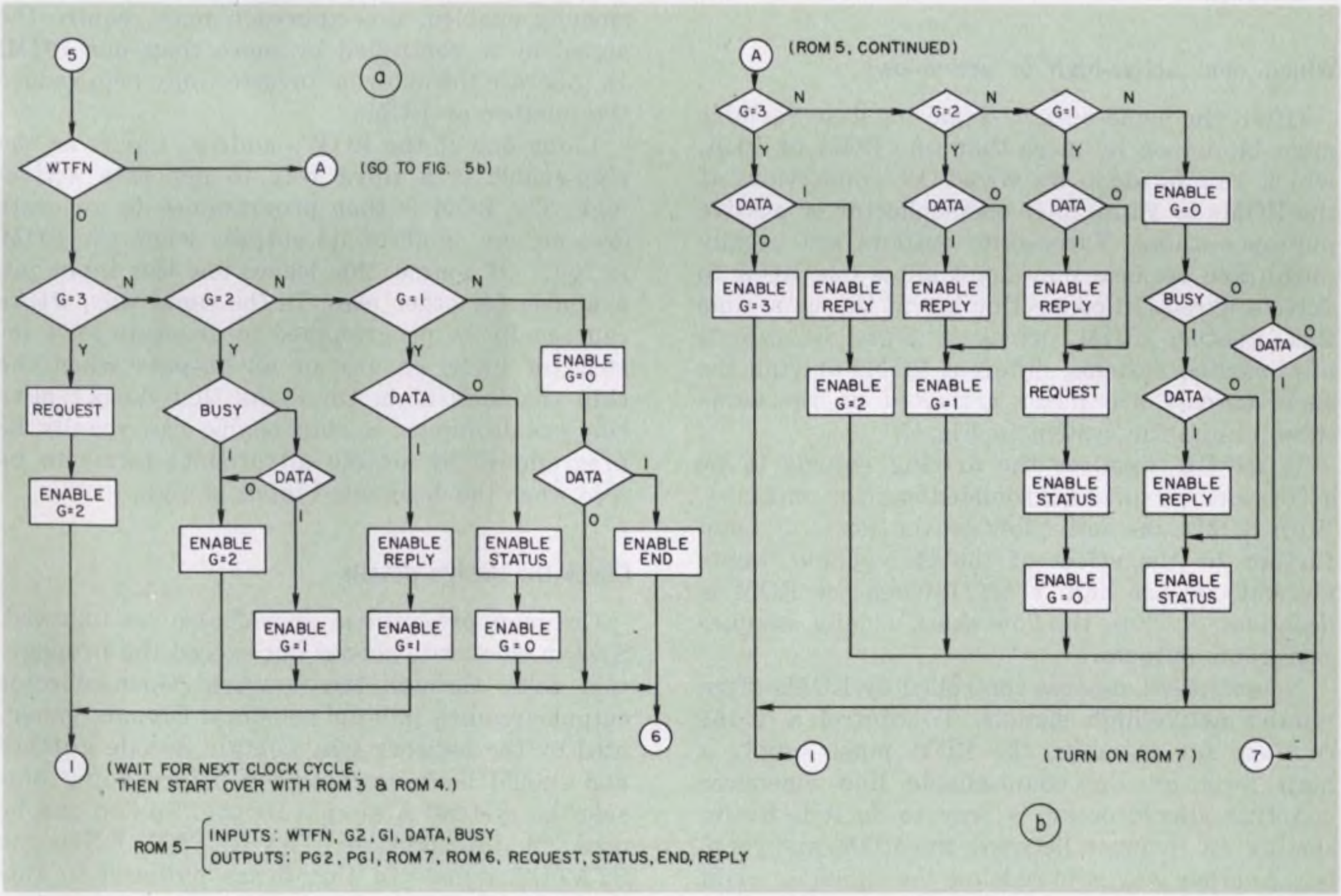
Fig. 4 shows a complex ROM network used in a computer interface coupler regulating information exchange between a central computer and a minicomputer-driven communications system. The function decoder routes input commands to perform these functions: input or output in character format or program format, input or output status or command words, stop, start or clear the minicomputer.

The interconnections in the figure are the chip-enable signals of the ROMs. Each ROM is documented with its own flow chart. The one for ROM_5, for example is shown in Fig. 5. It has two modes, read or write (Fig. 5a and b), determined by the write function signal, WTFN. In each mode there are four states $G = 0$ through 3. The BUSY signal indicates that the data are moving to or from a storage register, and the DATA signal indicates that the central computer is ready to transmit or receive the data word. The entire chart is turned on and off by a signal from the function decoder.

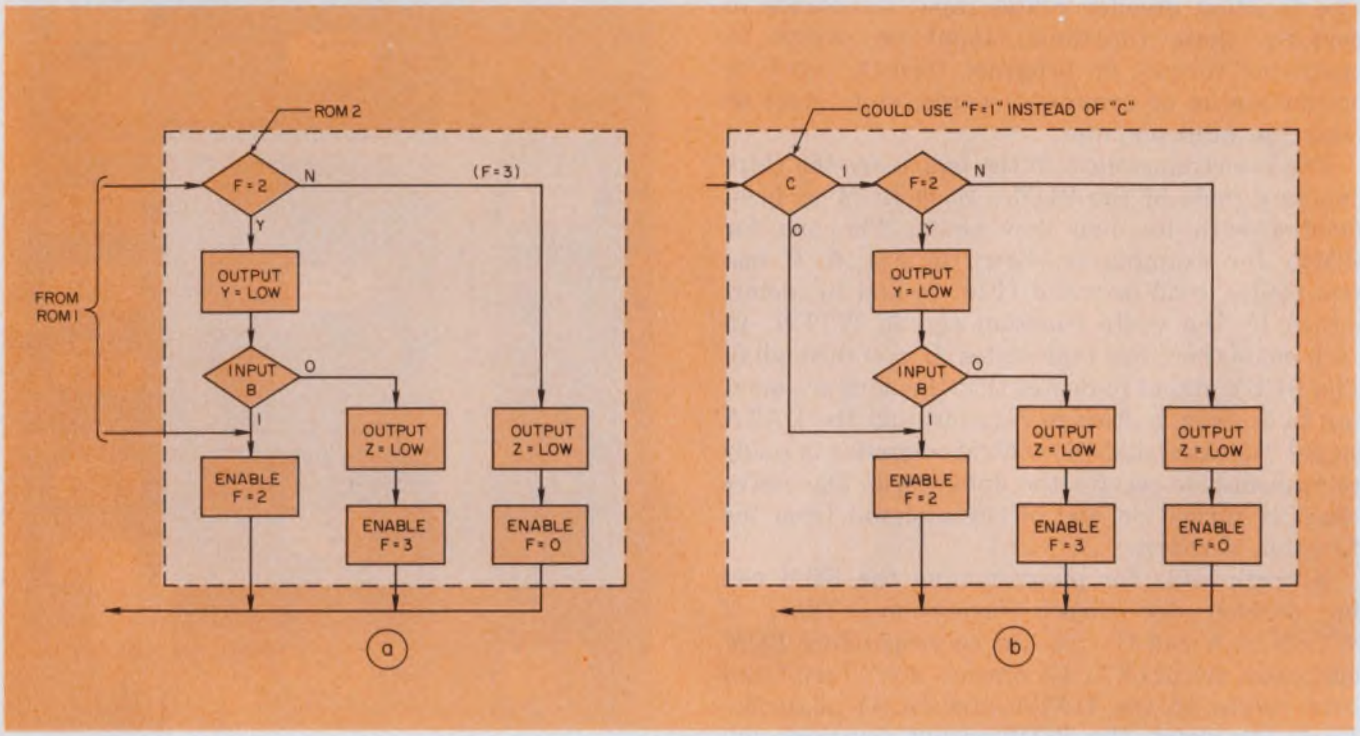
A truth table for programming the ROM can be derived by direct inspection. Thus, if $WTFN = 0$ and $G = 3$, the corresponding ROM addresses are 011XX. (X means "don't care," and here refers to the DATA and BUSY signals.) From the chart, the ROM output for these addresses is 10110111, referring to the eight outputs listed in Fig. 5a in the same order. The remain-



4. **An interface coupling network** regulates information exchange between a central computer and a minicomputer-driven communications system.



5. **Flow chart (a) represents the read logic** in ROM_5, which is part of the single transfer section of the computer communications coupler. The write logic in the same ROM is also shown (b).



6. **There are two entry paths** in this section of the chart (a). A new signal, C, distinguishes between paths (b).

ing ROM addresses can be derived by similar reasoning.

Which one: active-high or active-low?

Often the same output signal or state variable must be driven by more than one ROM or PLA, which can be done by wired-OR connections if the ROMs or PLAs have open-collector or passive pull-up outputs. Three-state outputs are usually unsuitable because they don't allow one ROM to drive a wired-OR connection low at the same time that another ROM drives it high. In typical bus-oriented systems, different ROMs driving the same signals are never activated at the same time, unlike the system in Fig. 4.

Wired-OR requires the driving signals to be active-low (assuming grounded-emitter outputs). With ROMs, the active-low convention is dictated further by the effect of the chip-enable input; i.e., outputs are high ("off") when the ROM is deactivated. Thus, the flow chart usually assumes active-low outputs.

Nevertheless, devices controlled by ROMs often require active-high signals. To control a 74161 counter, for instance, the ROM must supply a high level on the count-enable line whenever counting should occur. A way to do it is by inserting an inverter between the ROM and counter. Another way is to redefine the signal as count inhibit, rather than count enable. The signal is then inherently active low, meaning that counting is inhibited when the signal is low. If the counter is normally inhibited and only occasionally enabled, this approach may require the signal to be controlled by more than one ROM. In this case the external inverter may help reduce the number of ROMs.

Using one of the ROM's address inputs as the chip-enable is a third way to generate active-high. The ROM is then programmed to generate lows on any or all of its outputs when the ROM is "off." Of course, this leaves one less input pin available for other uses. In the same way, PLAs can usually be programmed to generate lows instead of highs on any or all outputs when the chip enable is high. On PLAs that do not have chip-enable inputs, a chip enable can readily be programmed by setting all product terms to be zero when the designated input is high.

Check the design details

Common precautions should also be followed. System clock rate should not exceed the propagation delay through the network. Open-collector outputs require pull-up resistors. Signals generated by the network may contain decode glitches and should be resynchronized before going outside the system. A simple D-type flip-flop can be used for this purpose. The REPLY, END and STATUS signals in Fig. 5 are buffered in this manner. REQUEST is strictly internal and does not require protection against decode glitches.

It's easy to see whether a section of flow chart will fit into one ROM or PLA: just count the number of inputs and outputs required. Obviously every signal requires at least one pin. With a PLA, it's also necessary to estimate the number of product terms needed. This is easily done by counting the number of possible paths through the chart. Each path can be implemented with one product term. In Fig. 2a for instance, since there are seven paths, no more than seven product terms are needed if the entire chart is incorporated into one PLA. This number is a maximum, not a minimum, as can be found by mathematical analysis. The difference isn't important unless the capacity of the PLA is in danger of being exceeded.

Handling multiple entry paths

Frequently a section of flow chart has more than one entry path. In these cases, additional ROM inputs must be used to distinguish between paths. One additional input is needed whenever the number of paths doubles. Thus, three additional inputs are required to distinguish one of 8 possible entry paths. Fig. 6a shows a section of flow chart with two entry paths. In Fig. 6b, signal "C" has been added to take care of the two paths. In this case, an extra output pin on the driving ROM_1 has been allocated. Sometimes an existing signal can be used instead. Comparing Fig. 2a and 6b, for example, shows that "C" will be activated only when $F = 1$. Therefore state variable F2 could be used instead of C to drive ROM_2. Why F_2, not F_1? Because ROM_2 already used F_1 to distinguish between states 2 and 3. Sometimes an entry path can be eliminated entirely. The logic associated with the second entry path in Fig. 6a is so simple it can easily be included in ROM_1, as shown in Fig. 3a.

Given the first cut at partitioning, it can quickly be determined whether further simplification is possible. Count the number of unused pins, the number of times the same signal is connected to more than one pin, and the number of signals used for distinguishing entry paths. If more than one pin per signal is being used there may be a way to reduce the package count by a slight rearrangement of the flow chart. Although it requires trial and error, it may be much more productive than trying to partition several pages of Boolean equations. ■■

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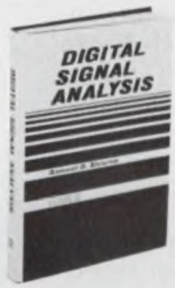

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Patching a program into a ROM may seem impossible. In fact, it is quite possible and can be accomplished with a minimum of extra circuitry.

In developing applications programs for microprocessor-based products, you often find that a desired program is already available in a ROM that also contains one or more unwanted subroutines or program steps. One way around such a problem is to go ahead and use the ROM, adding the minimal circuitry needed to skip over the unwanted sections.

Many times this technique is cheaper than producing a new ROM or more convenient than going through the whole procedure of copying the desired program into read/write memory, modifying it and running it from there. But even with these advantages, the method, naturally, is not intended for use in production volumes where the cost of a new ROM can be justified.

There are programs from many sources, including semiconductor manufacturers, that are widely useful with only slight modification—programs such as monitor routines, debug packages and assemblers.

Another possibility is that a program that has been developed in-house and put into a ROM must be changed in some relatively small way that would be inconvenient to correct by reprogramming a new ROM.

A new program may need more hardware

For either case, the potential user of a ROM program is faced with four alternatives:

(1) He may obtain a modified version of the program from the vendor.

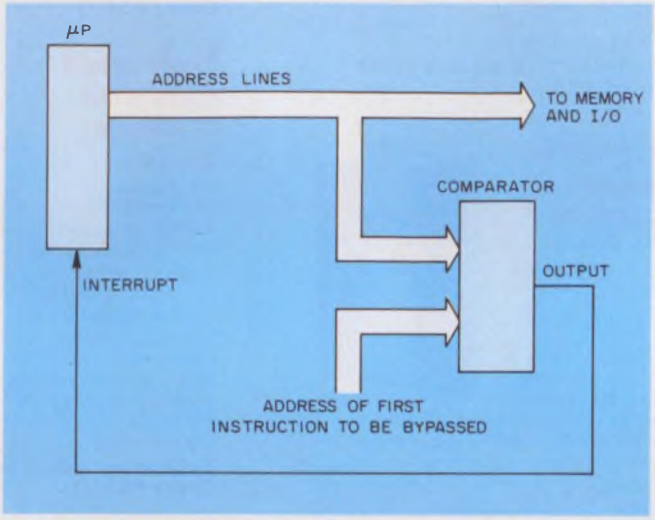
(2) He may modify the program himself and either use it in read/write memory or put it in PROM or ROM form.

(3) He may build a special hardware interface that allows the use of the undesired program.

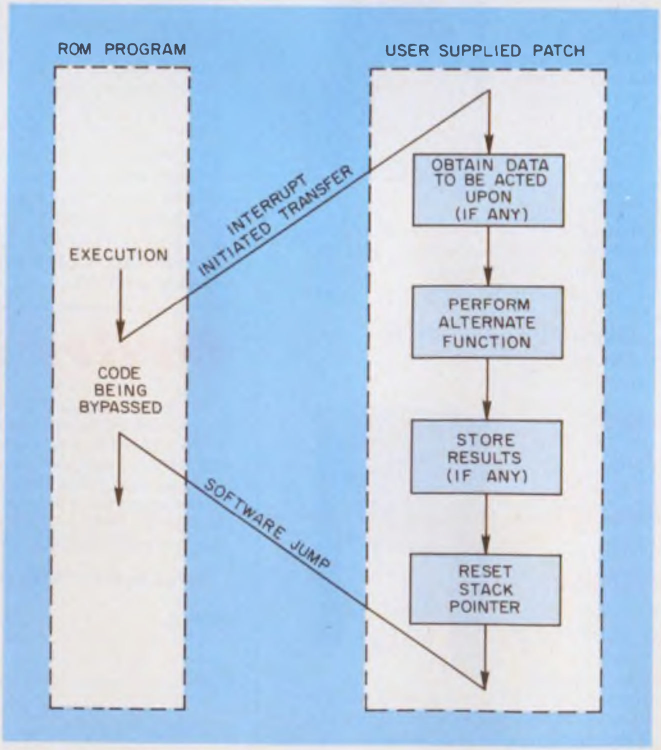
(4) He may transfer control of the microprocessor to another memory when the undesired portion of the ROM is about to be executed.

This last approach is development oriented and can easily be made a permanent part of a μP

Tim Travis, Section Manager, Modeling and Analysis, The Aerospace Corporation, Box 92957, Los Angeles, CA 90009.



1. **The hardware necessary** to skip over undesired programs in a ROM is basically simple. The method uses interrupts generated by the unwanted addresses.



2. **The replacement code** must not allow the microprocessor to jump back to the beginning of the unwanted program. The code resets the stack pointer.

development facility and used whenever the need arises to "patch" a program in ROM.

Patching is done in several steps:

- Determine the starting location of the code to be bypassed.
- Put a digital comparator or other address decoder on the microprocessor address lines and supply one comparator port with the address of the starting location identified above.
- Use the output of the comparator to interrupt the μP when the program begins execution of the code to be bypassed (that is, when the first instruction is fetched and its address appears on the address lines).
- Respond to the interrupt with code that performs the alternate function desired and destroys the linkage back to the bypassed portion.
- Jump (branch) to the remaining code.

A block diagram of the required hardware is shown in Fig. 1. Microprocessors that require an instruction to be placed on the data lines when an interrupt is honored need additional circuitry (usually a jump or branch) to supply that instruction. If the μP program-development facility already has a vectored interrupt capability, it can be used to simplify the added hardware.

```
LOC     CODE          SOURCE         COMMENTS
                      CARD
                      *
                      *              INITIALIZATION CODE
                      *
                      *     SET UP I/O PORT "A" FOR EIGHT INPUT BITS
                      *     AND PORT "B" FOR TWO OUTPUT
                      *     BITS (D0 AND D1) AND THE REMAINING, FOR SIX
                      *     INPUT BITS.
7000    A9 00         START LDA  0     LOAD A WITH ALL ZEROS
7002    8D 01 6E            STA  6E01  STORE IN PORT A CONTROL (Note 1 & 2)
7005    A9 03               LDA  3     LOAD A WITH D0 & D1 = 1 (Note 3)
7007    8D 03 6E            STA  6E03  STORE IN PORT B CONTROL
                                       CONTINUE INITIALIZATION
```

(a)

```
LOC     CODE          SOURCE         COMMENTS
                      CARD
                      *
                      *              SERIAL OUTPUT ROUTINE (PARTIAL)
                      *
                      *     OUTPUTS CHARACTER IN X AND MODIFIES
                      *     CONTENTS OF A
                      *
726E    AD 02 6E      SOUT  LDA  6E02  READ STATUS OF PORT B
                      *
                      *
                      *
[illegible] 60              RTS        RETURN
```

(b)

Notes:

1. The MOS Technology 6502 Microprocessor, like the Motorola 6800, does not use input and output instructions to communicate with peripheral devices as the Intel 8080 does. Instead, such devices are addressed as though they were a part of memory.
2. In this example, I/O port A uses the address 6E00 for its data register and 6E01 for its control register while port B uses addresses 6E02 and 6E03, respectively. When programming one of these ports, a "zero" written into a bit of the control register causes the corresponding bit in the data register to be an input while a "one" bit causes the data-register bit to be an output.
3. D0-D7 refer to the eight bits of the data bus or of a register. D0 is the least significant bit and D7 is the most significant.

3. **The original initialization software** uses two bits programmed for serial data output, and a total of 14 bits bits as input (a). The output routine drives one of the output bits to produce a 6-bit character (b).

The new program must match the original

The program to which the interrupt branches (either in read/write memory or in user-generated ROM) must do a number of things before returning control to the ROM (Fig. 2). First, it must perform the function that replaces the ROM code that is bypassed. Remember, the instruction whose address triggered the interrupt will already have been executed when the interrupt-handling routine gets control. Sometimes the effect of this last instruction is inappropriate and irrecoverable. If that is the case the address-comparator input must be supplied with the address of the instruction that immediately precedes the one bypassed.

Of course, this alternate approach can't be used if the first instruction is called from several other locations, which can happen when the bypassed code is a subroutine used several times in a larger program. Obviously the programmer who is performing the substitution must be familiar enough with the original code to know where that piece of data is located—in an accumulator or other register, in the stack or in read/write memory. Similarly, when the user-supplied patch finishes execution, it must leave its results in the same places as would the original code.

The user-supplied code must also destroy the linkage back to the beginning of the interrupt address, or the undesired program will still be executed. The link—the address of the instruction causing the interrupt—will normally be reserved in the stack and so must be erased.

With normal interrupts this saved information is used as the basis for the return jump that resumes execution where it was originally interrupted, but now it would cause the initially-bypassed code to be executed. Therefore (with the possible exception of certain status data) this information must be removed from the stack as though the return had been executed.

Conveniently, removing data from the stack

Instruction formats and registers for the M6502

6502 instruction formats

1. One byte instructions
   a. First byte = Op code
2. Two byte instructions
   a. First byte = Op code
   b. Second byte = Immediate operand or relative displacement for branch instructions.
3. Three byte instructions
   a. First byte = Op code
   b. Second byte = Low order byte of operand or jump address.
   c. Third byte = High order byte of operand or jump address.

Registers used in the example

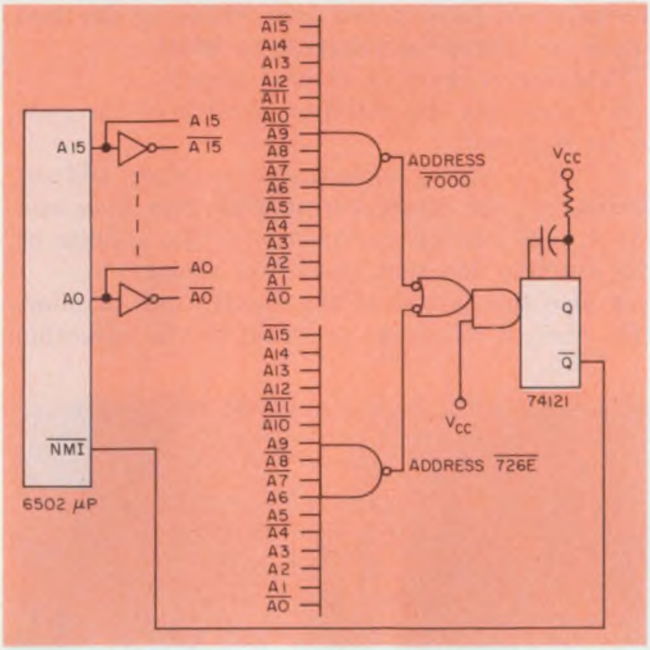
1. A = eight bit accumulator in which all arithmetic and logic operations take place.
2. X = one of two eight-bit index registers.
3. P = eight-bit processor status register.

6502 instructions used in the example

1. AND: Logical product of A register and operand*
2. BEQ: Branch if results of last operation equal zero**
3. BNE: Branch if last result not zero**
4. CMP: Compare operand* with contents of A register
5. JMP: Transfer control to the address specified in second and third bytes
6. LDA: Load A register with operand*
7. ORA: Logical sum of A register contents and operand*
8. PLA: Pull most recent byte from stack and load into the A register
9. PLP: Pull most recent byte from stack and load into status (P) register
10. RTS: Return jump from subroutine—restores program counter from stack
11. STA: Store A register contents in specified address
12. TXA: Transfer X register contents to A register

*Operands may be immediate (the contents of the second byte of a two byte instruction) or the contents of the location pointed to by the second and third bytes of a three-byte instruction.

**The branch if equal (BEQ) and branch if not equal (BNE) instruction,s use relative addressing. Therefore, BEQ—7 indicates that if the previous operation resulted in zero, control will be transferred to the instruction located seven bytes before the first byte of the instruction following the BEQ instruction.



4. The **interrupt-triggering logic** recognizes either of the two addresses that must be skipped. The replacement program differentiates between the two.

only requires that the stack pointer be reset to skip past the no-longer-needed data. Once this is done the patch software will jump to the first instruction following the bypassed code.

If more than one segment of code must be bypassed (e.g., if both input and output routines in a ROM program must be changed) additional comparators must be used and their outputs OR'd together. The comparator triggering the interrupt must then be identified. The interrupt-handling routine examines the last stack address when the comparator generates the interrupt. This address will uniquely identify the code being bypassed, thereby identifying which comparator triggered the interrupt.

Change I/O from serial to parallel

Suppose we modify the input and output routines of a program to change a serial I/O routine to a parallel format. The example is based on the MOS Technology 6502 µP and 6530 Peripheral Interface/Memory Device. The 6530 contains 1024 bytes of mask-programmable ROM, 64 bytes of RAM, two 8-bit I/O ports and a programmable timer.

The manufacturer supplies standard versions of this device with either of two different monitor routines programmed into the ROM portion of the device, or with both. If we can make minor modifications to one of the ROM programs, fewer additional PROMs will be needed, and we won't have to duplicate the RAM, I/O and timer capabilities of the 6530.

The two portions of a hypothetical program, shown in Fig. 3, control communication (via a serial output) to a teletypewriter. The first segment (locations 7000-7009 in hexadecimal) programs the two I/O ports. Port A, whose control-register address is 6E01, is set to all "zeros," thus programming all eight bits to be inputs. Port B is programmed with the two lowest-order bits as outputs and the other bits as inputs.

The second segment of code (location 726E-7291) represents a serial-output subroutine that

```
LOC     CODE        SOURCE                  COMMENTS
                    CARD
                    *
                    *                       PATCH CODE
                    *
                    *        REMOVE PRE-INTERRUPT STATUS AND
                    *        ADDRESS FROM STACK AND DETERMINE
                    *        WHICH ADDRESS TRIGGERED THE
                    *        INTERRUPT
                    *
0200    28          NMINT    PLP            RESTORE STATUS REGISTER
0201    68                   PLA            PULL LOW ORDER ADDRESS BITS
0202    68                   PLA            PULL HIGH ORDER ADDRESS BITS
0203    C9                   CMP   70       COMPARE HIGH ORDER BITS
                                            WITH 70 (HEX) TO CHECK FOR
                                            INITIALIZATION PATCH
0205    D0  0A               BNE   INT2     IF NOT EQUAL, JUMP TO OUTPUT
                                            PATCH
                    *
                    *               INITIALIZATION PATCH
                    *
                    *        INITIALIZE PORT A FOR ALL OUTPUT BITS
                    *        EXCEPT D7 FOR READING STATUS AND
                    *        INITIALIZE PORT B FOR ALL INPUT BITS
                    *
0207    A9  7F      INT1     LDA   7F    LOAD A WITH SEVEN ONES
0209    80  01  6E           STA   6E01  STORE IN PORT A CONTROL
020C    A9  00               LDA   0     LOAD A WITH ALL ZEROS
020E    4C  07  70           JMP   7007  JUMP BACK TO STORE IN
                                         PORT B CONTROL
                    *
                    *                 OUTPUT PATCH
                    *        READ STATUS OF PORT A UNTIL READY AND
                    *        THEN OUTPUT X TO PORT A
                    *
0211    AD  00  6E  INT2     LDA  6E00   READ STATUS OF PORT A
0214    29  80               AND  80     MASK OFF BIT D7
0216    F0  F9               BEQ  -7     IF NOT 1, KEEP TRYING
0218    8A                   TXA         TRANSFER CHARACTER TO A
0219    09                   ORA  40     ADD DATA STROBE BIT (D6)
021A    8D  00  6E           STA  6E00   WRITE CHARACTER TO PORT A
                                         WITH DATA STROBE BIT HIGH
021D    29  BF               AND  BF     MASK OFF DATA STROBE BIT
021F    80  00  6E           STA  6E00   CHANGE DATA STROBE BIT AT
                                         PORT A TO LOW BUT LEAVE DATA
                                         UNCHANGED
0222    60                   RTS         RETURN
```

5. **The interrupt-response software** generates a new output format that contains separate subroutines for both of the substituted ones.

outputs a 6-bit character, one bit at a time, through the low-order bit of port B. Only the first and last instructions are shown here because details of the subroutine are not important to the example.

Now, instead of using a serial-output device, use a parallel device—connected to port A—that requires six data bits and a "data strobe" signal, and that returns a "data ready" signal when ready to accept a new character. This totals seven output bits and one input bit, so we first initialize port A with seven bits that are programmed as outputs and one bit that's programmed as an input.

Since port B no longer is being used for serial output, it is programmed so that all of its bits are inputs. The program in Fig. 3 then requires two modifications:

First, change the initialization sequence—which starts at location 7000—by programming port A as a seven output bits and one input bit, and programming port B as all input bits.

Second, bypass the whole serial-output routine starting at location 726E, and replace it with a parallel-output routine.

The hardware recognizes these two addresses and triggers an interrupt (Fig. 4). The two addresses are detected by ANDing together the appropriate address bits or their complements. (The sixteen-bit NAND gates are combinations of smaller gates). The one shot stretches the result to the two clock periods required by the microprocessor.

The replacement software routine starts at location 0200 (Fig. 5). The program determines which address triggered the interrupt, and destroys the linkage back to the beginning of the unwanted code. The last address saved by the interrupt is pulled from the top of the stack and examined, simultaneously erasing the linkage back to the interrupted code.

After the high-order byte of the return address is pulled from the stack, it is compared with 70 (the high-order byte of the address of the initialization code) to determine whether or not it was the 7000 address that triggered the interrupt. If it was not the interrupt must have been triggered by the 726E address, because in this example those are the only two possibilities.

The return address saved on the stack (7002 or 7271) is the address of the first byte of the instruction following the one interrupted.

If the high-order byte of the return address is 70, the comparison will yield a zero result and the program will not branch at location 0205. Instead, control passes to the initialization patch which starts at location 0207. Next, port A is programmed as one input bit (D7) and seven output bits. A zero is loaded into the A register prior to being stored in the port B control register, and then the A register's contents are stored at 7007 via the jump instruction at location 020E.

If the high-order byte of the return address is not 70, then the branch at location 0205 will be taken, and control will pass to the parallel output routine starting 0211. Since this patch replaces a whole subroutine rather than just a segment of inline code, the patch ends by executing a return (RTS) instruction rather than a jump back to the code being bypassed. ■■

References

1. *MSC6500 Microcomputer Family Hardware Manual,* Publication Number 6500-10, August, 1975, MOS Technology, Inc., Valley Forge, PA.

2. *MSC6500 Microcomputer Family Programming Manual,* Publication Number 6500-50, August, 1975, MOS Technology, Inc., Valley Forge, PA.

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CIRCLE NUMBER 50

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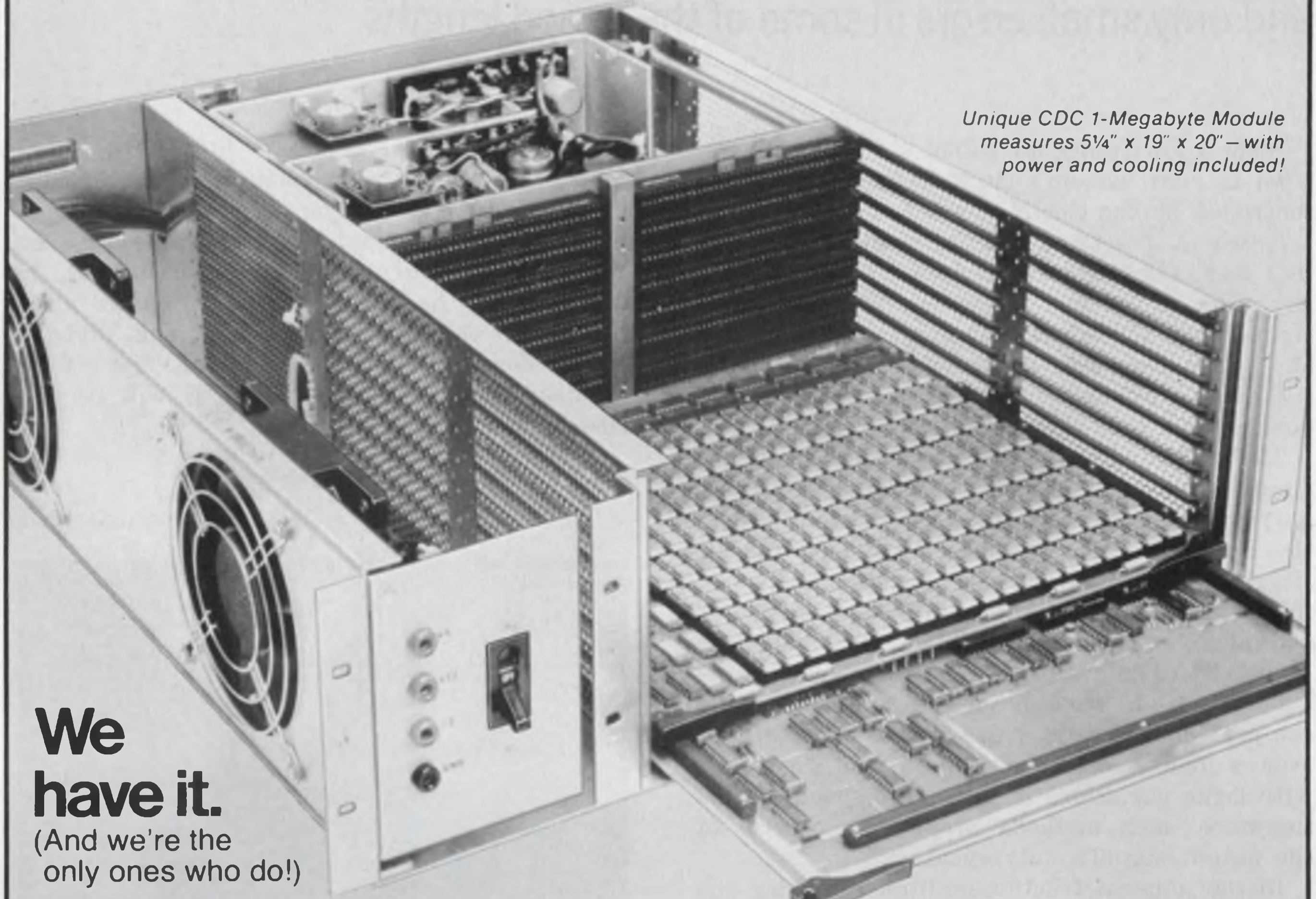

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CIRCLE NUMBER 51

Divide frequencies by nonintegers.

Obtain low frequency signals that have exact average values, and only small errors in some of the period lengths.

Need a low-frequency signal not integrally related to your system's clock frequency, but still controlled by the clock?

Here's a fractional-multiplier/divider circuit that uses only standard counters flip-flops and a minimum of gating. The design procedure is simple and straightforward, and if needed, a 50% duty cycle can be provided. Pulse-to-pulse spacing errors are small, and the average frequency, over only a few cycles, is exact.

The digital division of frequencies by whole numbers is routinely done by many methods: binary counters, decade counters, Johnson counters, etc. But there are few simple techniques for deriving a low-frequency from a high-frequency clock, with the two not integrally related.

Suppose you need 150 Hz, and your base clock is 1 MHz. The ratio of the two frequencies is 6666 2/3 to 1. Though some digital approaches can provide this ratio, pulse periods are averaged over a long sequence of pulses, and generally, with large variations in interpulse spacing. Furthermore, such methods provide no control of the output signal's duty cycle.

In the unusual fraction-multiplier/divider circuit described here, however, period lengths can always be made to differ at most by one period of the high-frequency clock. Thus, the higher the system's clock frequency, and the lower the final output frequency, the smaller is the relative interpulse error.

Designing a three-part divider chain

The techniques of the method can best be explained with the 150-Hz/1-MHz example. Say the 150 Hz signal requires a duty cycle of 50%; the 1 MHz clock's duty cycle can be almost anything.

First, break down the ratio of 150/1,000,000 into a reduced set of prime numbers, as follows:

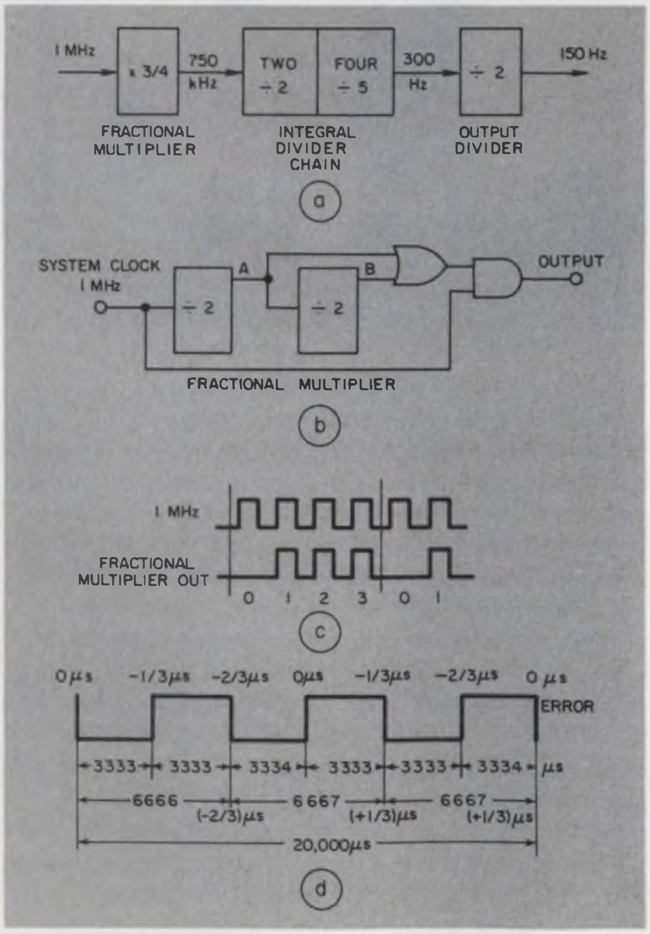
$$\frac{150}{1{,}000{,}000} = \frac{2\cdot 3\cdot 5^2}{2^6\cdot 5^6} = \frac{3}{2^5\cdot 5^4} \qquad (1)$$

Cornelis van Holten, Dept. of Applied Physics, University of Technology, Delft 2208, the Netherlands and **Jan Obdrzalék,** Faculty of Mathematics and Physics, Charles University, 121 16 Prague, Czechoslovakia.

Second, factor the results of Step 1 into three parts, with the last part equal to 1/2 (for a 50% duty cycle). And make the first part, a fractional multiplier, N/D, equal to some value between 1/2 and one. Note that N/D is chosen equal to 3/4 and that the middle factor has only a number one in the numerator so that this division can be done with integral counters. The effects of other possible choices for N/D will be discussed later.

$$\frac{3}{2^5\cdot 5^4} = \left(\frac{3}{4}\right)\left(\frac{1}{2^2\cdot 5^4}\right)\left(\frac{1}{2}\right) \qquad (2)$$

The fraction, N/D = 3/4, is generated by a



1. **To get a 50%-duty-cycle, 150-Hz signal from a 1-MHz clock,** a divider chain (a) consists of three parts: a 3/4 fractional multiplier (b), an integral divider and a final divide-by-twi output. The fractional-multiplier output (c) produces minimum phase errors (d).

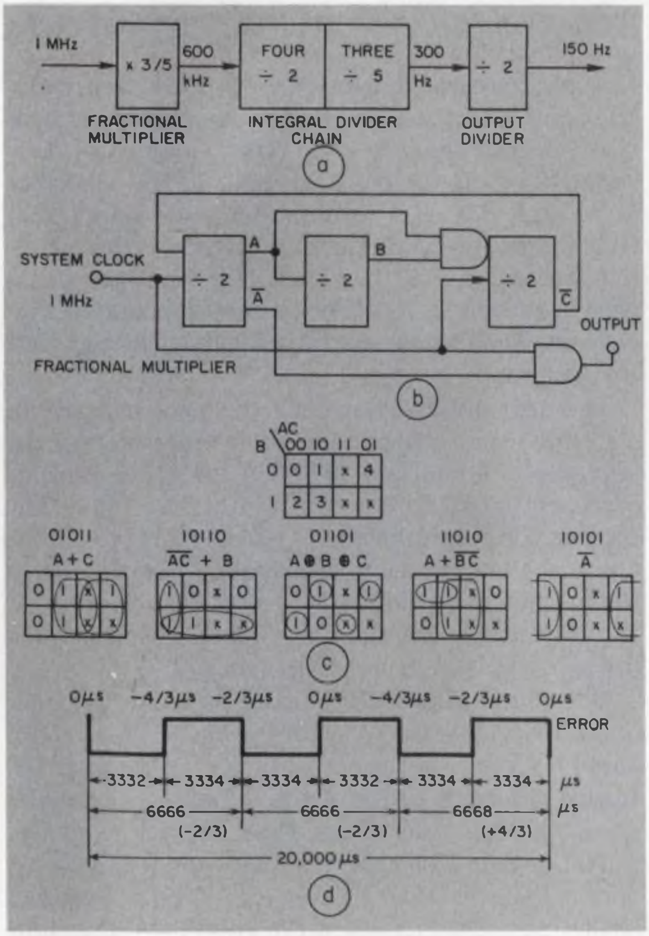
fractional multiplier circuit; the other two factors are easily implemented with standard divide-by-two and divide-by-five chains (Fig. 1a).

The fractional multiplier, if implemented as in Fig. 1b, provides a 0111 output sequence (Fig. 1c). Any decoder gating arrangement that can provide a three-pulse output out of every four pulses can be used—1011, 1101 or 1110—but the circuit in Fig. 1b is the simplest solution.

The order of the dividers in the center chain, of course, may be chosen at will.

The resulting signal has an average frequency of 150 Hz, but the individual period lengths deviate from exact values by $-2/3$ μs or $+1/3$ μs, as shown in Fig. 1d.

The period errors, as would be expected, appear cyclically. The exact single-cycle period of a 150 Hz signal is 6666 2/3 μs. In the circuit of Fig. 1b, one-out-of-three output cycles is short by 2/3 μs and two-out-of-three cycles are wider by 1/3 μs; the sequence 6666, 6667 and 6667 μs is thus obtained. It is true that the exact sequence and magnitude of the errors don't depend upon the order in which the center $\div 2$ and $\div 5$ dividers are arranged. However, there may be an effect from the bit sequence that the fractional



2. **A fractional multiplier that multiplies by 3/5** can also be used. Karnaugh maps (c) may be used to obtain a minimum design for the gating of the fractional multiplier. Larger than minimum errors (d) can result if the "wrong" fractional-multiplier pulse sequence is chosen.

multiplier produces and from the selection of N/D. A chart method described later can provide this information.

An alternate choice of N/D

The fractional multiplier, $N/D = 3/4$, can, instead, be replaced by $N/D = 3/5$ (Fig. 2a). Then the system's three parts split into

$$\left(\frac{3}{5}\right)\left(\frac{1}{2^4 \cdot 5^3}\right)\left(\frac{1}{2}\right) \qquad (3)$$

At that point, the decoder gates of the first—or fractional multiplier—stage must select three-out-of-five pulses. Again, you may choose any one of the possible sequences of three ONEs and two ZEROs. Some of them are better than others. Those with all ONEs adjacent to each other, such as 11100, or 00111 or 01110, don't provide as uniform a distribution of the ONEs as 01011, 10110, 01101, 11010 and 10101.

The idea is to pick a sequence that requires the least possible amount of gating to decode, and one that produces the smallest phase errors.

To find the best sequence, follow Rule 5 (explained in the box): For $N/D = 3/5$, since $N > D + 1$, write down the sequence—

$$\frac{0}{5}, \frac{3}{5}, \frac{6}{5}, \frac{9}{5}, \frac{12}{5}, \frac{15}{5};$$

truncate to whole numbers (6 values)—

0, 0, 1, 1, 2, 3;

determine the differences between these whole numbers (5 values)—

0, 1, 0, 1, 1;

and as mentioned in the box, the sequence may be "rotated," or end-around shifted, to obtain also 10110, 01101, 11010 or 10101.

From the Karnaugh maps of the divide-by-five counter (Figs. 2b and 2c), the sequence 10101 is found to be easiest to implement; it needs only a single AND gate.

The integral divider counters, which make up the middle part of the three-part system (Fig. 2a), are determined by the relationship of Eq. 3. They consist of a chain of four divide-by-two counters in tandem with three divide-by-five counters, and a final divide-by-two flip-flop. This integral divider chain can also be implemented by three divide-by-ten counters and one divide-by-two counter; thus

$$\left(\frac{3}{5}\right)\left(\frac{1}{2 \cdot 10^3}\right)\left(\frac{1}{2}\right) \qquad (4)$$

Again, the sequence order in this center divider chain is arbitrary.

It's interesting to note that the selection of sequence 10101 for implementing the fractional multiplier in Fig. 2b produces the same minimal phase-error distribution as shown in Fig. 1d. However, with a 00111 sequence, the errors are much larger (Fig. 2d). In two-out-of-three cycles, the cycle period is short by 2/3 μs, and in one-

Rules for noninteger frequency-divider design

1. Write down the fraction,
$$\frac{f}{F} = \frac{\text{output frequency}}{\text{clock input frequency}}.$$
2. Factor the numerator and denominator into powers of prime numbers.
3. Simplify the fraction.
4. Separate the result into 3 parts, namely:
   (a) a fraction N/D, such that $1/2 < N/D < 1$ and choose the value closest to one;
   (b) a fraction, 1/2, if a duty cycle of 50% is wanted; if not, this fraction may be deleted;
   (c) a fraction $\left(\frac{1}{f_1 \cdot f_2 \cdot \cdot \cdot \cdot f_n}\right)$. This fraction incorporates all remaining factors of the original denominator, and if no 50% duty cycle is needed, also the 1/2 from 4b.
5. If $N = D + 1$, go to Rule 6.
   If $N > D + 1$, write down a sequence of $D + 1$ fractions: 0/D, N/D, 2N/D · · · DN/D. 1 Truncate (drop fractional parts) the values of this sequence to integers, including 0. Determine the (D) differences between the (D + 1) integers, which deliver a sequence of ONEs and ZEROs. This is the "best" configuration of N out of D pulses. Since this sequence may be "rotated," there are D such possible sequences.
6. Determine the simplest gate configuration using (D) Karnaugh maps to obtain the N out of D pulses. Counter flip-flop states not used in establishing the sequence are don't-care states (X). In this way you have found a sequence with the simplest hardware, and at the same time, the smallest phase-errors.
7. Determine the number and type of the center section integral dividers. By making judicious choices, you may be able to economize in hardware.
8. Select an output divider that gives you the desired output duty-cycle. For a 50% duty-cycle, the final divider is a divide-by-two flip-flop. In practice, small deviations from the 50% duty cycle will occur, since there are small errors in period "half" lengths.
9. Divide the period of the wanted low frequency by the period of the clock. The result, generally a noninteger, can be expressed by an integer followed by a fraction, a/b. The output-signal will have "a" periods with a length somewhat too large and (b—a) with a length somewhat too small. The order and magnitude of these deviations can be determined by the chart method described in the text.
10. If the microsecond errors are too big, choose a higher clock frequency and repeat the process.

out-of-the-three it's long by 4/3 μs.

The pulse sequence needed for minimum errors may not always correspond with the simplest possible decoder-gate configuration, so a hardware/error trade-off may be involved.

Determining the errors

The sequence and magnitudes of the phase errors can best be determined by a simple charting process (Fig. 3). Of course, a set of timing diagrams can also provide this information but the chart is simpler, faster and takes less space.

In the first chart (Fig. 3a), for the system in Fig. 1, the center-section divide-by-two counters are arranged first, and are followed by the divide-by-five circuits. The second chart (Fig. 3b) reverses the order of the counters—divide-by-fives first, then the divide-by-twos—to show that the order of the counters in the center section makes no difference in system performance; the output signal is the same in either case.

The chart merely provides a convenient means for counting input-clock intervals along the divider chain. In Fig. 3a, the first divide-by-two (÷2) column vertically lists three cycles of the three-out-of-four pulse-pattern from the fractional multiplier.

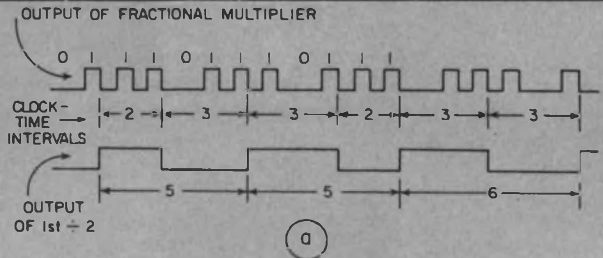
After the first pulse, which is used as a starting point, every sequence of two ONEs (count of two) is marked off, and the number of corresponding input-clock intervals in the sequence is written down. A timing diagram shows this first divide-by-two action simulated by the counting process used in the chart. Note that the clock-time sequence, 2, 3, 3 clock times repeats so that only one such set needs to be derived in the first ÷2 column.

The next divide-by-two circuit also reverses its state for every other input pulse and reverses the sequence of its output "half" cycles with periods of repeating 5, 5, 6 clock-times (Fig. 3a). The process for obtaining the 5 5, 6 sequence becomes quite obvious when you examine the listing in the second ÷2 column. A brief examination of all succeeding columns also clearly reveals the process involved in setting them up.

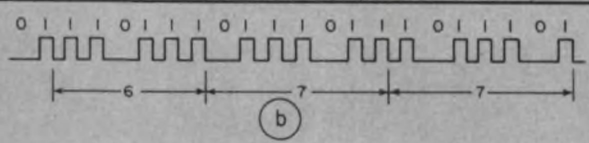
The chart, Fig. 3b, which shows that the order of the dividers in the integral divider chain doesn't matter, is prepared in a similar manner. In this chart the order of the ÷2 and ÷5 circuits are in reverse order from their Fig. 3a sequence.

The next-to-last columns show the sequence of period lengths for successive "half" cycles—3333, 3333, 3334 μs—and the final columns show the output whole-cycle periods—6666, 6667, 6667 μs. Each clock period is 1 μs, because the input clock is 1 MHz. Of course, generally each clock period is $1/f_c$, where f_c is the clock frequency. ■■

Fractional multiplier sequence	Center-section integral dividers						Output divider
	÷ 2	÷ 2	÷ 5	÷ 5	÷ 5	÷ 5	÷ 2
0 1 1 1	0 1 — 1 1 — 2 0 1 1 — 3 1 0 1 — 3 1 1	2 3 — 5 3 2 — 5 3 3 — 6	5 5 6 5 5 — 26 6 5 5 6 5 — 27 5 6 5 5 6 — 27	26 27 27 26 27 — 133 27 26 27 27 26 — 134 27 27 26 27 27 — 134	133 133 134 133 133 — 666 134 133 133 134 133 — 667 133 134 133 133 134 — 667	666 667 667 666 667 — 3333 667 666 667 667 666 — 3333 667 667 666 667 667 — 3334	3333 3333 —— 6666 µs 3334 3333 —— 6667 µs 3333 3334 —— 6667 µs
Sum 4	8	16	80	400	2000	10,000	20,000 µs

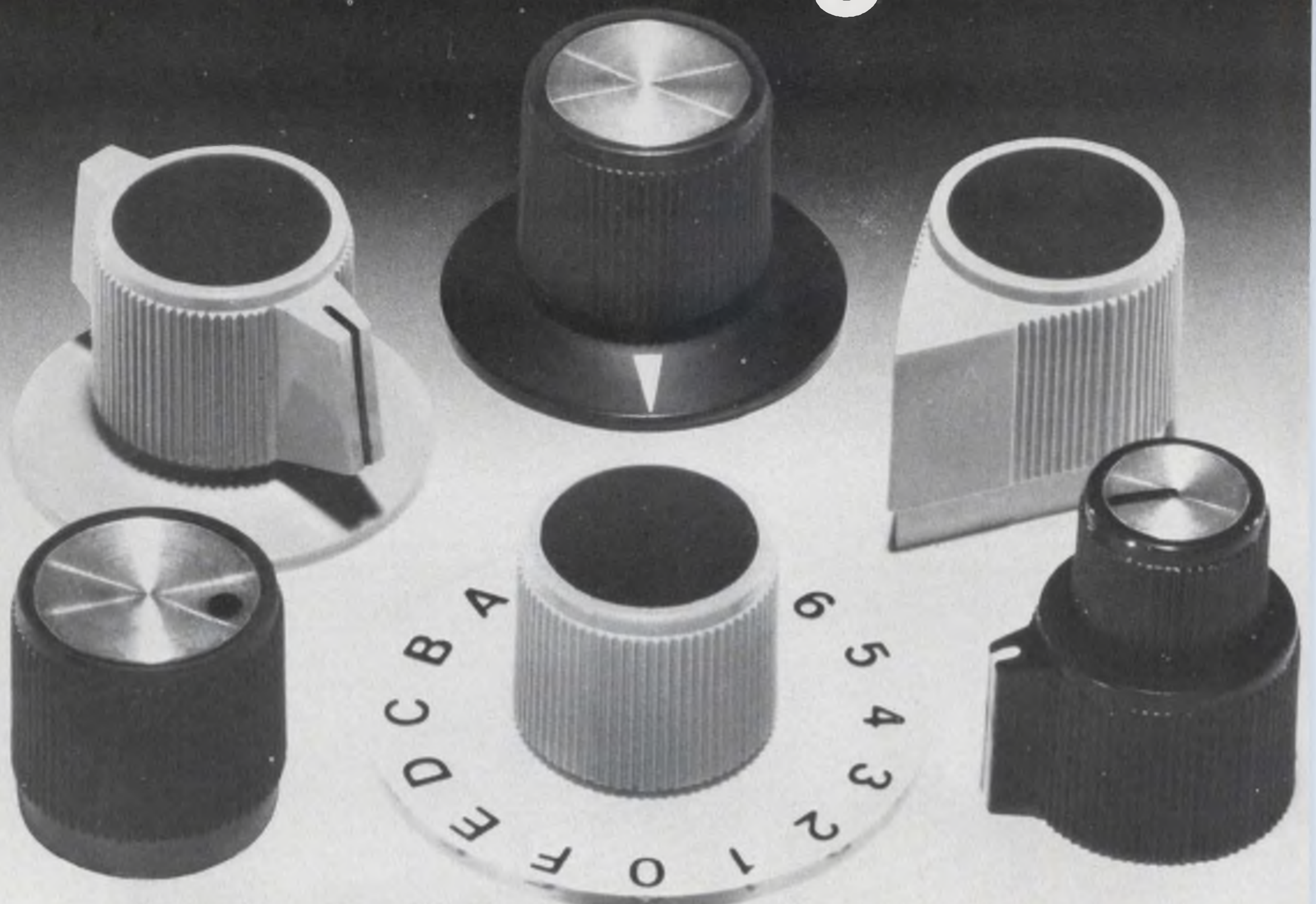


Fractional multiplier sequence	Center-section integral dividers						Output divider
	÷ 5	÷ 5	÷ 5	÷ 5	÷ 2	÷ 2	÷ 2
0 1 1 1	0 1 — 1 1 0 1 1 1 — 6 0 1 1 1 0 1 1 — 7 1 0 1 1 1 0 1 — 7 1 1	6 7 7 6 7 — 33 7 6 7 7 6 — 33 7 7 6 7 7 — 34	33 33 34 33 33 — 166 34 33 33 34 33 — 167 33 34 33 33 34 — 167	166 167 167 166 167 — 833 167 166 167 167 166 — 833 167 167 166 167 167 — 834	833 833 — 1666 834 833 — 1667 833 834 — 1667	1666 1667 —— 3333 1667 1666 —— 3333 1667 1667 —— 3334	3333 3333 —— 6666 µs 3334 3333 —— 6667 µs 3333 3334 —— 6667 µs
Sum 4	20	100	500	2500	5000	10,000	20,000 µs



3. **A chart method** may be used to determine the phase timing of the output signals. When the integral divider chain is arranged as in Fig. 1a, the chart method (a) shows the final sequence of output-phase periods as 6666, 6667 and 6667 µs. Interchanging ÷2 and ÷5 circuits (b) makes no difference.

Front panel components should look good.



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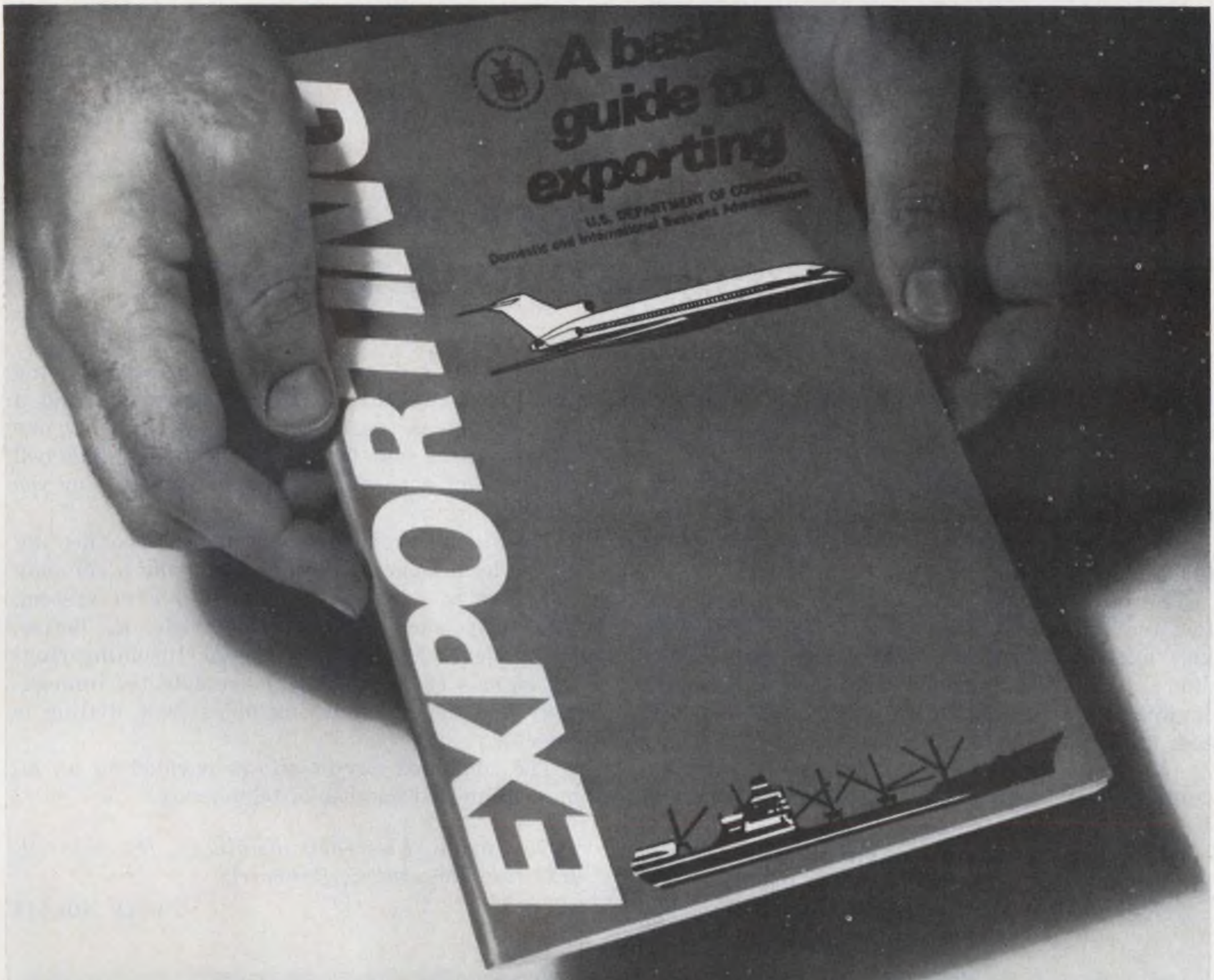
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Give priority to first phone lifted in parallel-connected phone systems

The circuit in the figure takes care of the two well-known problems that occur when telephones are paralleled in the usual manner. The problems are:

1. A telephone set can be "bugged" or "jammed" from another set on the same line.
2. The bell in one set may ring when another set is used for dialing out.

The cure for the first problem is easy: One terminal of each telephone set is provided with an "exclusive switch" built from two 4-layer diodes. The recommended 4EX 581 diodes are commercial versions, but the 4E 30-8 are low-cost trigger diodes with looser specs.

For a 48-V system, the diode's breakdown voltage must be about 33 V. Stable operation requires a maximum holding current of 15 mA, which is easily met in the circuit. The voltage drop across the diodes when ON is 0.8 V.

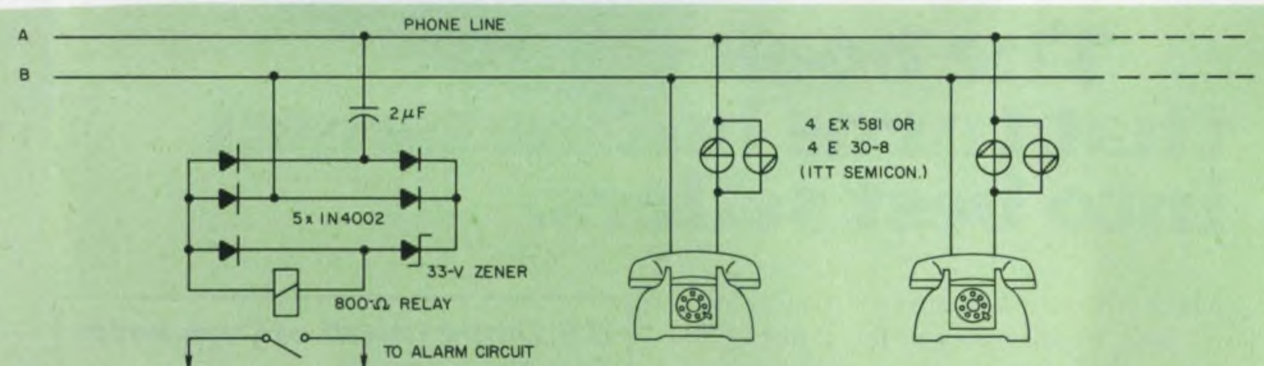
When a call is answered, the line voltage drops to less than 8 V, and all the sets except the one first lifted, are cut off. Changing sets during a conversation is possible, of course, but only one set at a time will be "alive." The dial and bell functions of a normal set are not offected by the switch.

The second problem is solved by disconnecting all the local bells in the sets and using a common call-relay to drive a distributed alarm system. The relay should be time-delayed—or, better, voltage-level dependent as shown. Incoming ringing signals (80 V at 20 Hz) are detected immediately and the commutating noise from dialing is rejected.

The combined circuit allows paralleling an almost unlimited number of telephones.

Ole Baden, Electronic Engineer, Hanehoj 21, DK 2880 Bagsvaerd, Denmark.

CIRCLE NO. 311



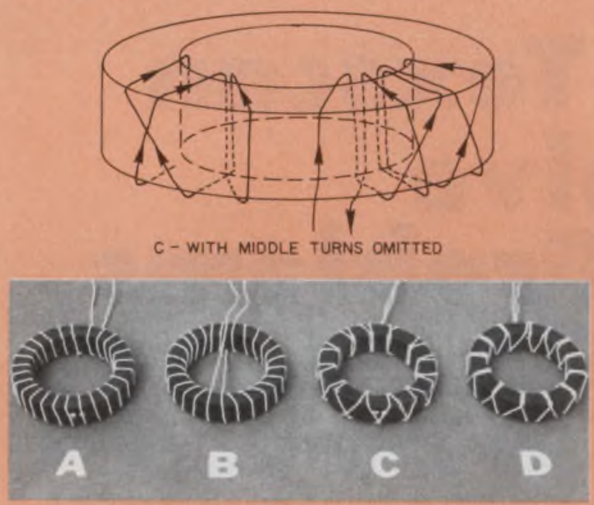
Four-layer diodes give priority to the first phone lifted in a parallel extension-phone system.

Super toroids with 'zero' external field made with regressive windings

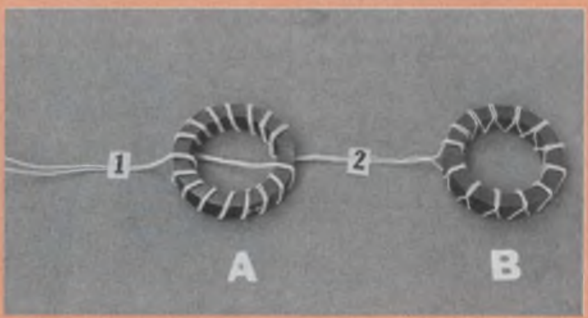
The toroidal coil has long been appreciated for its cancellation of the effects of external magnetic fields. But some uses for toroids demand an extreme degree of rejection of exterior influences.[1]

Simple "super-toroid" techniques can meet these demanding applications.

Fig. 1 shows four toroidal inductors having similar properties except for their radiation and response to external fields. Toroid A is a simple



1. **These four toroidal inductors** with similar low frequency properties have markedly different external field characteristics. The configuration of winding A is in common use, but never should be; B has least capacitance, and less stray coupling than A; both C and D provide extraordinary rejection of external fields.



2. **A super zero-external-field toroid** (B) is driven by a balun (A) so that electrostatic symmetry is obtained even with a grounded signal source on input-pair 1. Baluns provide an unbalanced-to-balanced drive more efficiently than transformers. And they can even couple dc. Though balun balancing properties are lost at low frequencies, the loss is seldom a problem.

360-degree winding. If both an external field and the magnetic properties of the core are uniform, the external magnetic flux will induce equal-but-opposite self-cancelling voltages in uniformly distributed turns located on opposite sides of the torus. However, the coil responds and radiates as a single-turn loop formed by the 360-degree winding as it progresses around the core.

Coil B avoids the single-turn loop by a reversal of the winding progression so that the two half-turn loops buck voltages induced by an external field. Although B is a big improvement over A, it shares with A a sensitivity to external field gradients and a need for a perfectly uniform core.

Most tape cores are not very uniform. If the tape ends are welded, the core properties at the weld are degraded. If not welded, asymmetry in permeance remains because of discontinuity at the tape start and finish. Even with ring stampings, asymmetry persists because of grain anisotropy.

An external field with an appreciable gradient induces a greater volt/turn in the near coil side that isn't cancelled by the far side. Miniaturization of the toroid reduces the effects of the gradient, but a truly zero external field coil must use windings of type C or D.[2]

Differences between C and D are small: Core C is optimized to decouple the winding from noise on a bus encircled by the core; D is used where minimum stray coupling between two stacked toroids is needed.

In both C and D each turn is paired with its complement from the other end of the winding[3] as in a bifilar winding. But unlike the bifilar winding, each turn is series aiding with respect to the core flux. Each pair of turns is self-cancelling to exterior flux. The gradient that may exist across the major dimensions of the torus, and a lack of uniformity in core permeance, has little effect.

These coils are often called regressive windings. They don't radiate, and they also can neutralize exterior electrostatic fields[3] if the two coil terminals are balanced with respect to ground.

A particularly efficient device for achieving balance is a balun[4] (Fig. 2A). The balun forces an ac voltage on the wires of pair number 2 that are to be balanced—even when one of the leads of pair 1 is grounded. Thus, in Fig. 2B no net capacitance current flows between the coil and its surroundings, or electrostatic shield, if any.

The balun employs a winding, as in Fig. 1B, because low distributed capacitance between the wire pairs 1 and 2 is desired. A voltage difference between pairs 1 and 2 is not very harmful, because the difference can be eliminated by the common-mode rejection of coil B.

On the other hand, it is very important that no voltage be induced across the lead pair 2. Thus, close spacing of the paired wires would help. A twisted pair or a coaxial cable is preferable, but not used in the photograph to lessen confusion.

T. A. O. Gross, Consulting Engineer, T. A. O. Gross & Associates, Lincoln, MA 01773.

CIRCLE NO. 312

References

1. Gross, T. A. O., and Sawyer, Paul B., "Measurement of Liquid Conductivity Without Electrodes," *Measurements and Data*, November/December, 1975.

2. Steen, F. L., U.S. Patent #3,449,703, June 10, 1969. 1969.

3. Gross, T. A. O., U.S. Patent #3,806,798, April 23, 1974.

4. Gross, T. A. O., "Baluns for Instruments," *Electronic Products*, September, 1963, pp. 38-39.

Power on or power off, reliable core holds the data. That's why system engineers are taking a new look at Ampex MCM, the Microcomputer Core Memory.

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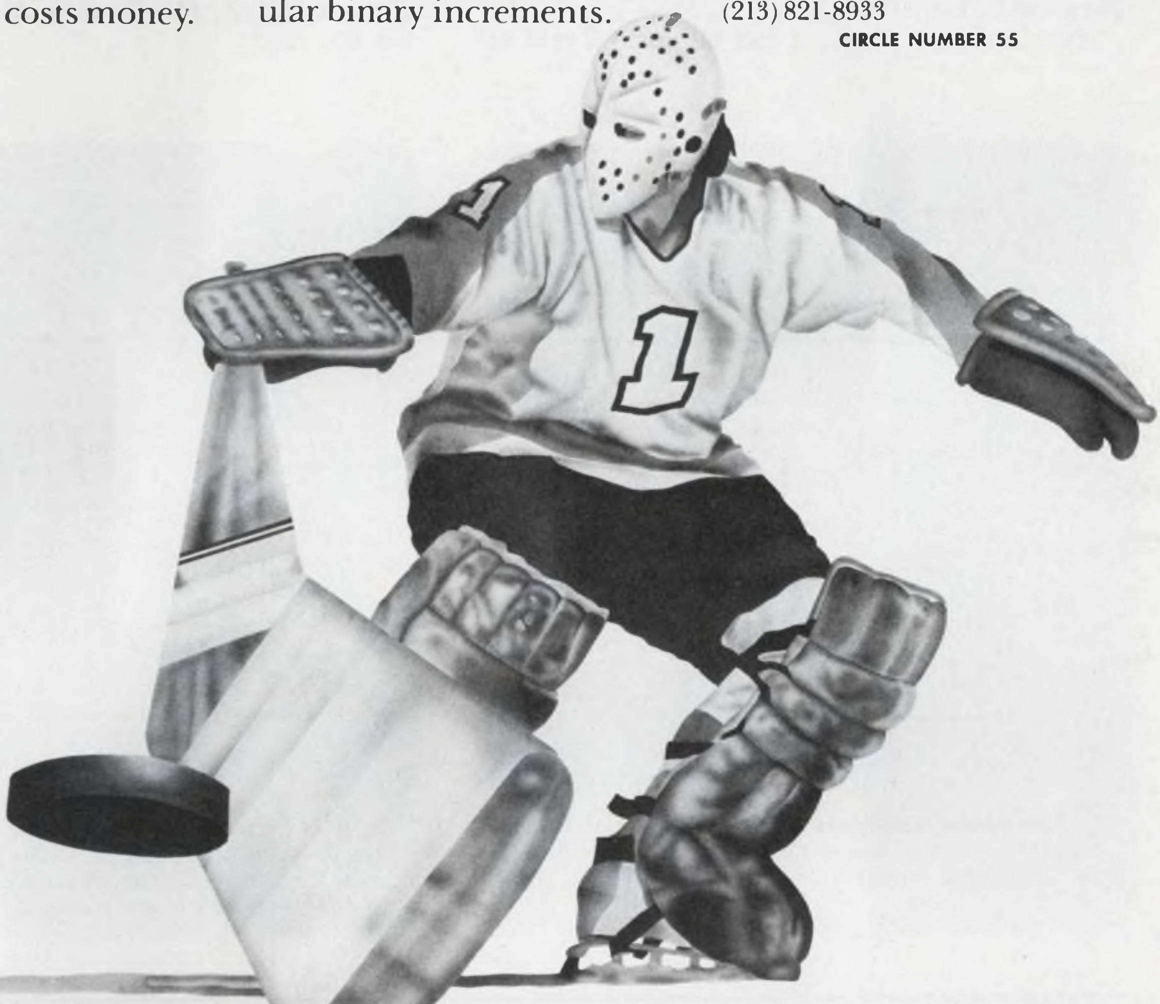
CIRCLE NUMBER 55



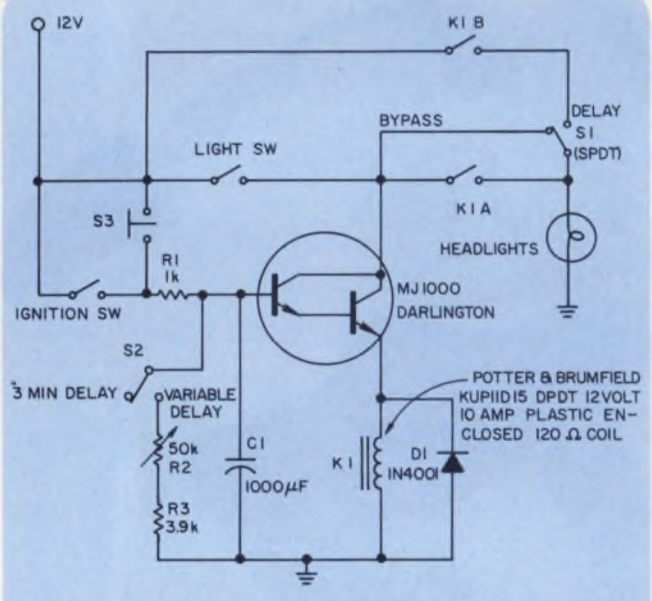
MICROPROCESSOR CORE MEMORY BLOCKS POWER PLAY

Delay circuits keep headlights on when needed; turn them off if you forget

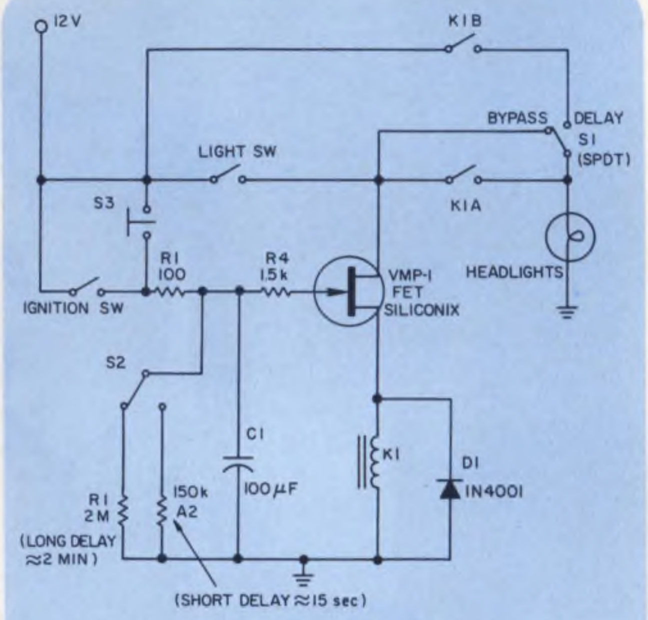
Here's a circuit to keep your automobile's headlights on temporarily as you walk up your driveway and unlock the door. It also will turn the lights off, even if you forget to flip the light switch. The circuit's shut-off delay is actuated only after both the ignition and light switches have been on, and only if the ignition switch is turned off first. If the light switch is turned off first, no delay results. Parking and brake-light operation is not affected.

The maximum time out can be up to 3 min in Fig. 1 and hours with the circuit in Fig. 2, depending on the relay selected and the value of R_2. A switch, S_2, may be used to permit selection of either a short or long delay. Momentary switch S_3 can restart circuit timing before the time-out is completed. A bypass switch, S_1, removes the delay action.

John Okolowicz, Senior Electrical Engineer, Honeywell, Inc., 110 Virginia Dr., Fort Washington, PA 19034. CIRCLE NO. 313



1. **Automobile headlights may be kept on** up to 3 minutes after you leave the car with this Darlington time-delay circuit.



2. **A FET version of the delay circuit** allows the use of a smaller timing capacitor, C_1, for a given delay, and almost instantaneous reset with S_3; the Darlington circuit needs almost 2 s.

IFD Winner for April 26, 1976

Jim Lipman, Member of the Technical Staff, Hewlett-Packard Laboratories, 1501 Page Mill Rd., Palo Alto, CA 94304. His idea "Build a Simple Fire Alarm with Metal-Oxide Temperature Sensors" has been voted the most Valuable of Issue Award.

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Design Decision

'Watchdog' circuit protects sig gen

Signal sources are one-way streets. That is, current is supposed to come out of the source's terminals, and not go into them. If reverse current somehow does flow because of an accidentally applied external voltage, the source's output transistors can be harmed.

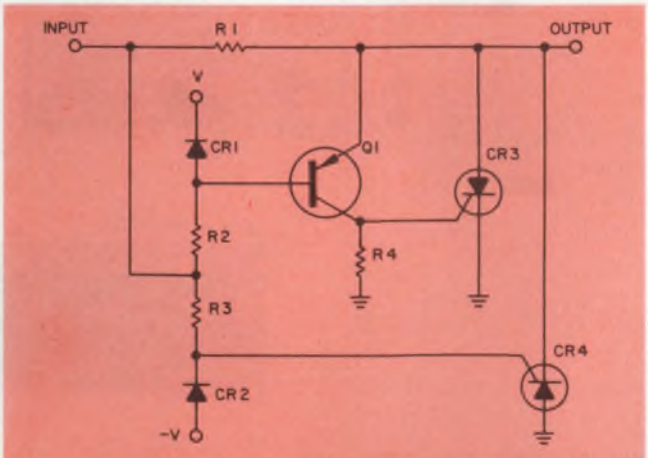
To prevent such damage, Krohn-Hite, Cambridge, MA, protects its function generators with a clever circuit (see figure).

If a voltage is accidentally applied, and if the reverse current is greater than 200 mA, the resulting voltage drop across R_1 will be sufficient to forward bias the gate-cathode junction of one of the two SCRs. Which SCR fires depends on the polarity of the external voltage.

The turned-on SCR presents a short circuit to the load, thereby protecting the generator's output transistors from damage. Rectifier SCR_4 turns on if a negative external voltage is applied. Similarly, SCR_3 turns on if a positive voltage is applied.

Voltage sensing diodes CR_1 and CR_2 further limit the current through the output transistors by clamping the output to the generator's plus or minus power supply whenever the external voltage exceeds the supply value.

The SCRs can handle 1 A continuously, 10 A of repetitive peak current, and 35 A of non-repetitive surge current.



An output-protection circuit for a signal generator connects in series with the generator's main output terminal. One of the two SCRs conducts when 200 mA of current attempts to get into the generator.

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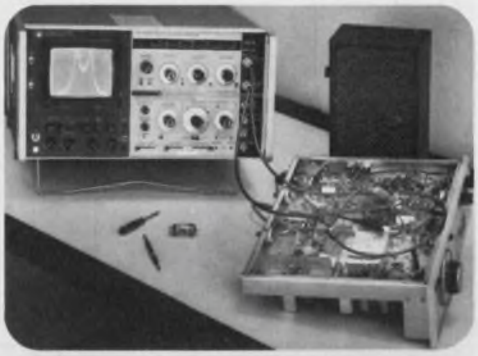
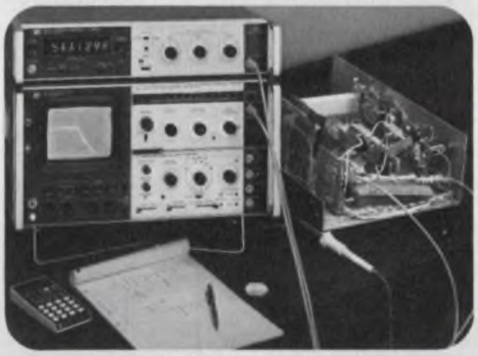


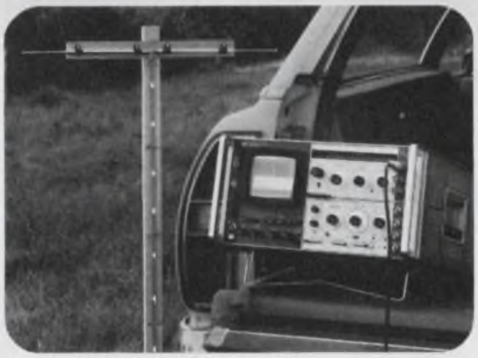
20 Hz to 300 kHz

The 8556A tuner covers 20 Hz to 300 kHz and comes with a built-in tracking generator. It's calibrated for measurements in both 50 and 600 ohm systems, with accuracies better than ±1 dB.



1 kHz to 110 MHz

The 8553B takes you from 1 kHz to 110 MHz with −140 dBm sensitivity. Signals can be measured with ±1¼ dB accuracy. Choose the companion tracking generator/counter for wide dynamic range swept frequency measurements and precise frequency counting.



100 kHz to 1250 MHz

Use the 8554B tuning section to cover the 100 kHz to 1250 MHz range. Measure with ±1¾ dB accuracy. Its companion tracking generator (500 kHz to 1300 MHz) also works with the 8555A tuning section.

10 MHz to 40 GHz

For 10 MHz to 40 GHz, choose the 8555A. Its internal mixer covers to 18 GHz, accessory mixer for 18-40 GHz. Maximum resolution is 100 Hz. Measure with ±1¾ dB accuracy to 6 GHz, ±2¾ dB to 18 GHz. For wide scans free from unwanted response between 10 MHz and 18 GHz, add the automatic preselector.

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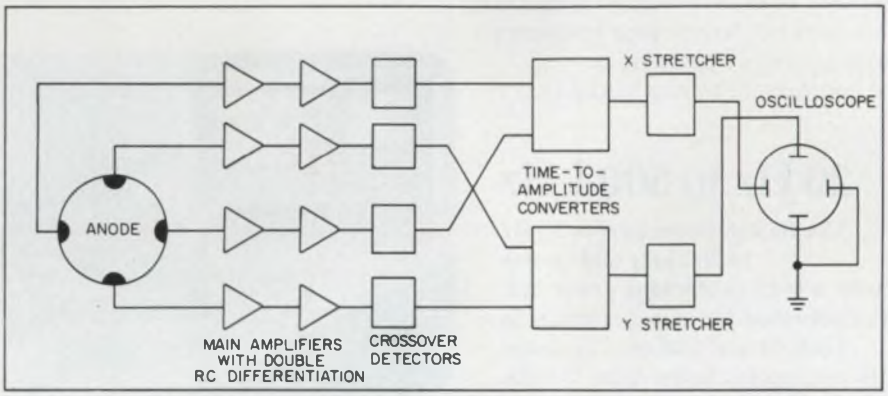
CIRCLE NUMBER 58

Cosmic X-ray detector gives higher resolution

A new position-sensitive detector for mapping cosmic X-ray sources is much simpler than previous two-dimensional detectors and gives a higher spatial resolution. According to its developers at Mullard Space Science Laboratories at University College in London, the parallel-plate, X-ray proportional counter, as it is called, can resolve 0.2 mm of soft X-ray radiation over a circle of few centimeters in diameter.



At present most X-ray detection takes place as a quantum-counting process and uses only energy discrimination to obtain data on the spectral content of the radiation. The position-sensitive detector, however, can form an X-ray image.

The detector consists of an X-ray window, a biasing grid and an anode plate, all parallel to each other. The anode plate is a glass disc coated with resistive material.

These discs, supplied by Philips

Research Labs, are produced by thin-film techniques. They are a few centimeters in diameter and of uniform resistivity over the entire surface. Philips has supplied several discs with resistivity of 1 MΩ per cm².

Four electrodes are deposited on the opposite edges of the resistive disc. The point on the disc where a charged particle has landed may be computed by measuring and comparing electrode voltages. The shape of the voltage pulse at each of the electrodes depends on the relative position at which the charge has hit the anode.

Because there are only four electrodes, the detector readout is relatively simple. Earlier detectors used multiwire resistive anodes that required complex signal-processing electronics.

Three flight models of the position-sensitive detector have been constructed to date. The lightweight version now being produced will be carried in the ESA EXOSAT satellite launch next year.

Single chip FET amp developed by Plessey

A monolithic X-band FET amplifier that has all the input and output matching circuitry on one chip has been produced by Plessey at the Allen Clark Research Center.

The Plessey broadband device is much smaller than travelling wave tubes and needs only a simple DC power supply. The amplifier requires only matching 50-Ω inputs and outputs to fit into a standard X-band system.

The amplifier consists of a broadband input-matching network of lumped elements that are fabricated with the FET on the same gallium-arsenide substrate. Output matching is provided by a wire bond at the drain electrode. The broadband matching network has been optimized, using computer aided-design, to produce minimum-voltage standing-wave ratios on input and output.

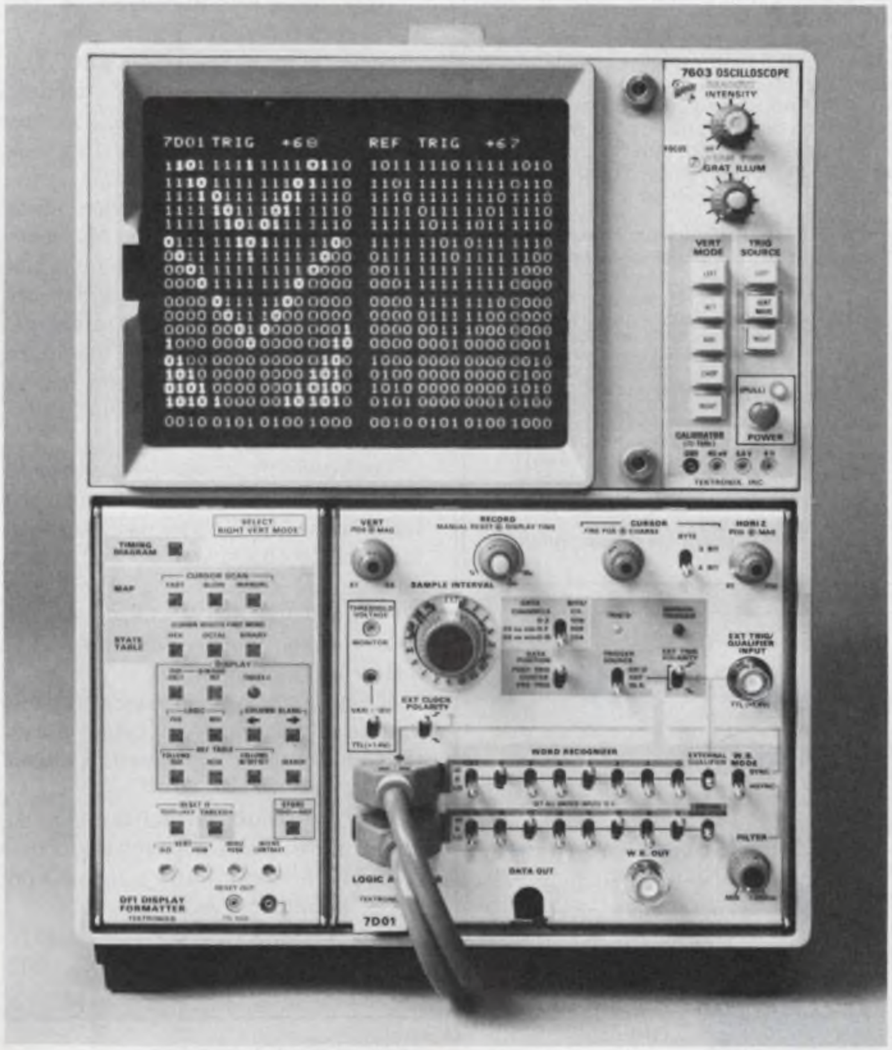
The lumped-element network is made of a gold-germanium alloy on a gallium-arsenide substrate. The FET is made of the same material, but is separated from the network by an epitaxial layer and a buffer layer.

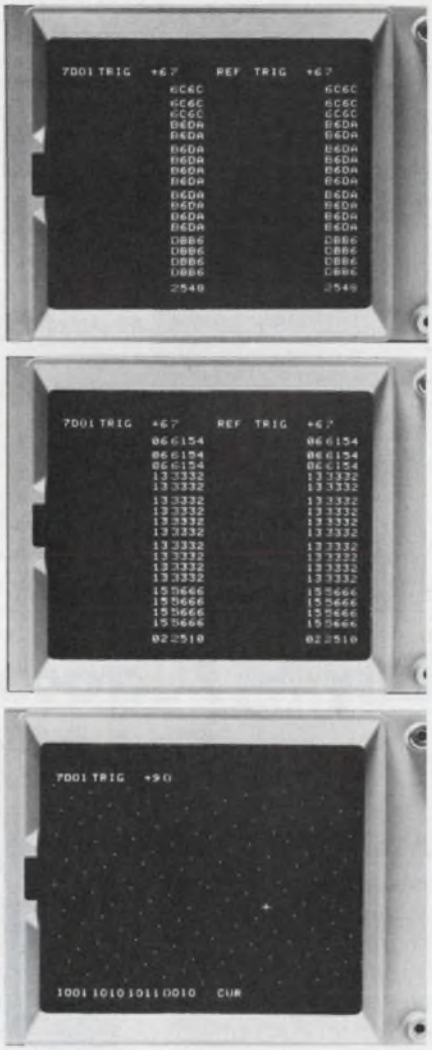
The amplifier is cased in a special cylindrical package that has a very low parasitic reactance and low feedback capacitance. The package diameter is 6 mm.

Frequency ranges of the amplifier are 7 to 11.7 GHz with a center frequency of 9.35 GHz or 6 to 10.7 GHz with a center frequency of 8.35 GHz. Gain is about 4.5 dB but laboratory measurements show a variation of approximately 0.5 dB from one chip to another.

The prototype amplifier has demonstrated noise ratings of 7.3 dB at 10 GHz. The predicted gain of a two-stage, single-ended packaged amplifier, is 9.5 to 10 dB over a 6 to 12 GHz band. A second amplifier chip with an average gain of 4.7 dB from 5.5 to 12.4 GHz has been recently produced. The device was designed under a Ministry of Defense contract.

Display formatter brings new power to logic troubleshooting





Display formats of the DF1 include comparison of two tables in hex (top) or octal (center). Mapping mode assigns each digital word a unique CRT position (bottom).

Tektronix, P.O. Box 500, Beaverton, OR 97077. (503) 644-0161. See text.

Plug the Tektronix DF1 display formatter into any of the company's 7000-series scopes, along with the 7D01 logic analyzer, and you no longer have to worry about which logic display is best. With the DF1, you get any of three presentations: timing diagram, state table and mapping.

The DF1 is the first to give you all three formats, a capability that lets you troubleshoot hardware and software in a variety of analytical modes.

In the timing-diagram mode, the scope CRT shows 16 channels in a square-wave-like display. Logic ONEs and ZEROs are represented by the upper and lower levels of the square wave.

In the state-table mode, the display consists of a table of up to 16 lines of 16-bit words in binary, octal or hexadecimal form.

In the mapping mode, the display resembles a star field, with each 16-bit word occupying a unique position on the CRT in the form of a bright dot.

In all three modes, various alphanumeric readouts add even greater test power. Shown at the top or bottom of the screen are individual words, as selected by a movable cursor, or the number of clock pulses between the triggering word and the word you select with the cursor. Readout can be in binary, octal or hexadecimal, as you prefer.

With the 7D01/DF1's fine and

(continued on page 122)

INSTRUMENTATION

(continued from page 121)

coarse controls, you can advance the display line-by-line or table-by-table for a quick survey of events. Even more important, the DF1 lets you make side-by-side comparisons of two tables—one with new information and the other carrying previously captured data (called the reference).

New data are displayed on the left side of the CRT, while the reference table is on the right. You can compare in several modes: table-by-table, line-by-line, or by use of a blanking feature to check column-by-column.

You can hold reference data steady while you advance the new-data "window" line-by-line or table-by-table to establish an offset between the left and right displays. Another mode lets you compare two sets of data that are offset from each other by a specific number of words.

Looking for a particular word? Go into the search mode and the DF1 scans the 7D01's memory for a match to the key word you select on the reference table. When the DF1 finds what it's looking for, it tells you the word's position in relation to the key word.

Keep hitting the search button and you'll soon have all other words that match the key word, as well as all locations.

The Tektronix formatter can do much more. Send a purchase order for $1195, wait 10 weeks, and check it out for yourself.

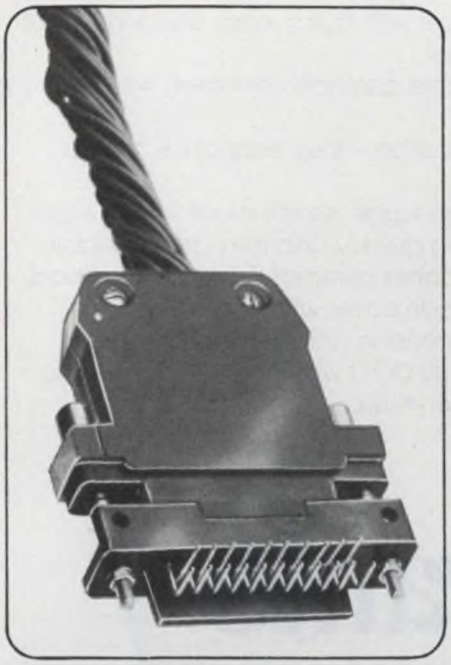
Booth No. 250 to 258; 349 to 357
Circle No. 302

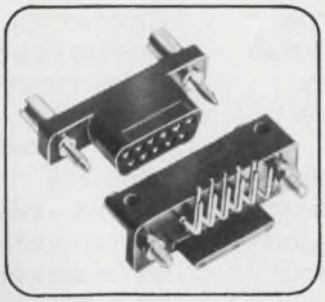
Hand-held DMM gets 'little' brother

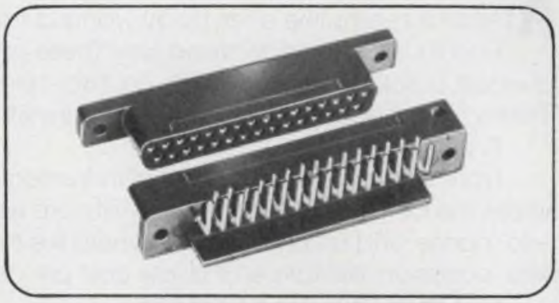
Data Precision, Audubon Rd., Wakefield, MA 01880. (617) 246-1600. $189; stock to 30 days.

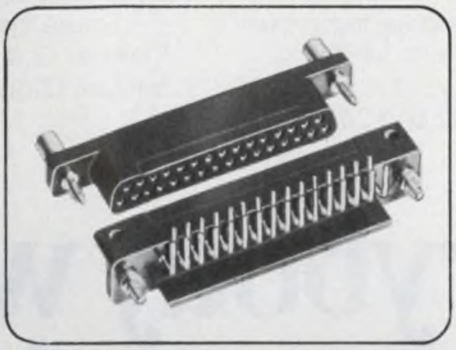
Model 175 3-1/2 digit DMM is a hand-held unit housed in a 1-3/4 × 5-1/2 × 3-1/2-in. case. The 175 is a full function, 32-range, battery and line-operated instrument, with basic sensitivity of 100 μV, both in dc and ac measuring functions. Basic accuracy is 0.1% ±1 LSD—this is a 1-year spec over a ±5-degree temperature range.

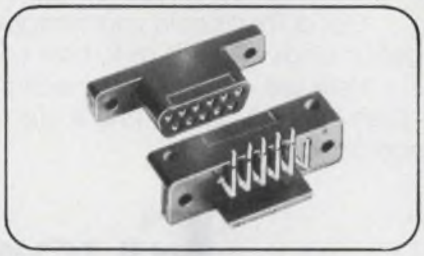
Booth No. 166, 168, 170
Circle No. 306

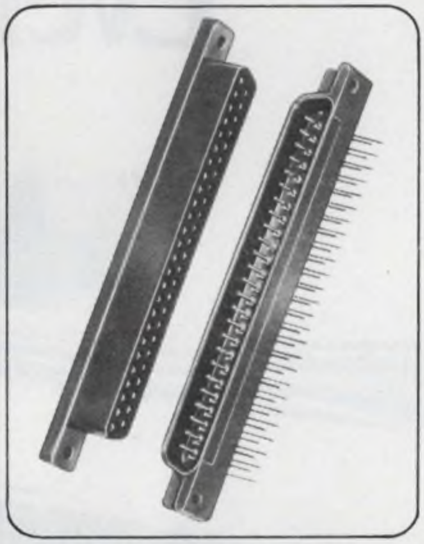












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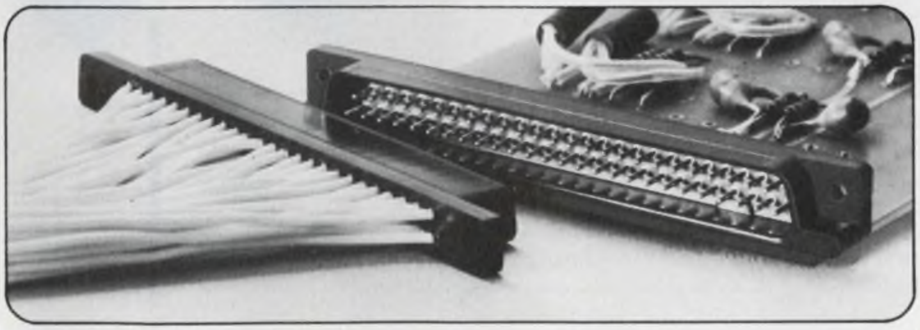

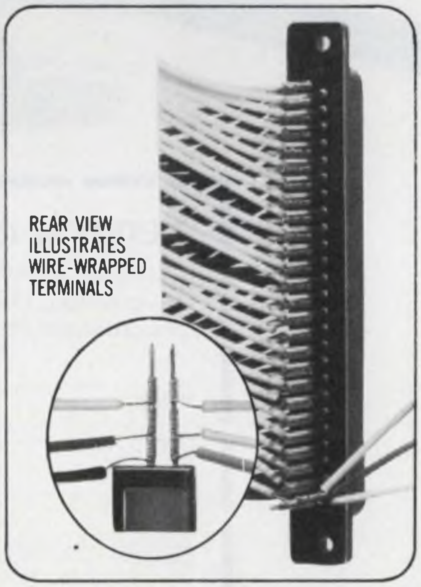

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Viking CONNECTORS

Viking Industries, Inc., 21001 Nordhoff Street
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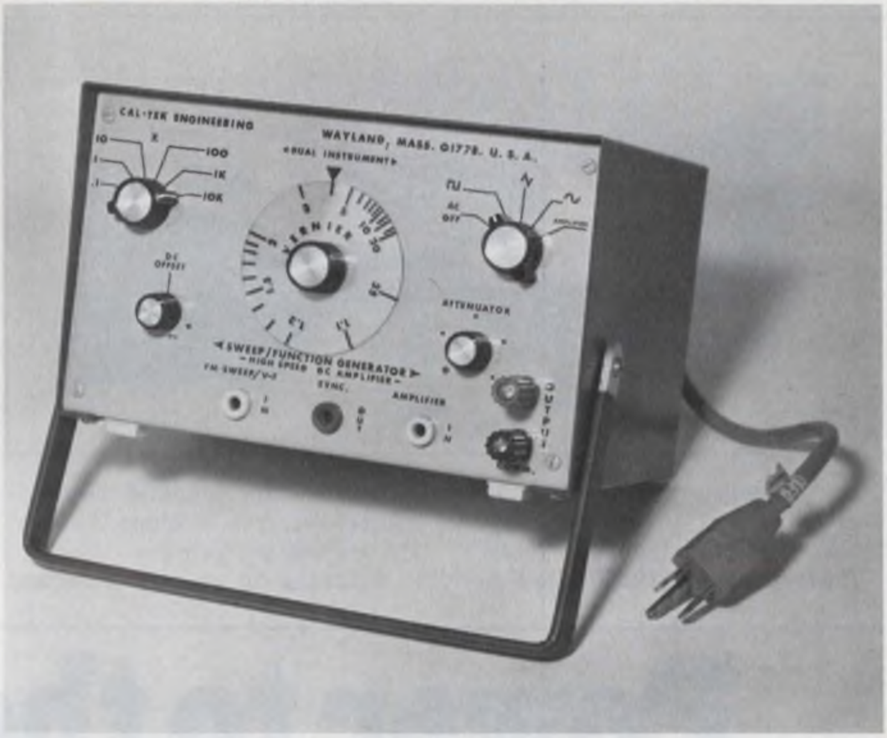
CIRCLE NUMBER 66

Function generator plays dual role as fast amplifier



Cal-Tek Engineering, 29 Pemberton Rd., Wayland, MA 01778. (617) 653-0355. See text.

Cal-Tek Engineering's Model 200 function generator brings a new capability to a class of instrument already known for versatility. The unit not only delivers the familiar sine, square and triangular waveforms, it acts as a fast-slewing, quick-setting dc amplifier.

Output frequencies in the Model 200 span 0.2 Hz to 200 kHz, and the amplifier—a 12-MHz inverter—slews at 70 V/μs and settles within a $\pm 0.1\%$ error band in 800 ns. At the unity-gain crossover point of 12 MHz, the amplifier's phase margin is 60 degrees.

You can couple the function generator and amplifier together or use each independently. All inputs, outputs and controls are located on the front panel, so there's no need to shuffle annoying internal connections.

In the function-generator mode, the output amplitude swings from 0 to 20 V pk-pk into an open circuit or 10 V pk-pk across 600 Ω. A dc-offset control provides ± 5 V of up-and-down motion. Another output provides a 1.4-V pk synchronized square wave.

Use the amplifier summing input and you can modulate amplitude, shift levels or blank a selected waveform.

Still another input lets you frequency modulate, sweep the waveshapes or use the generator as a VCO. Sweep bandwidth is 10 kHz over a 1000:1 range.

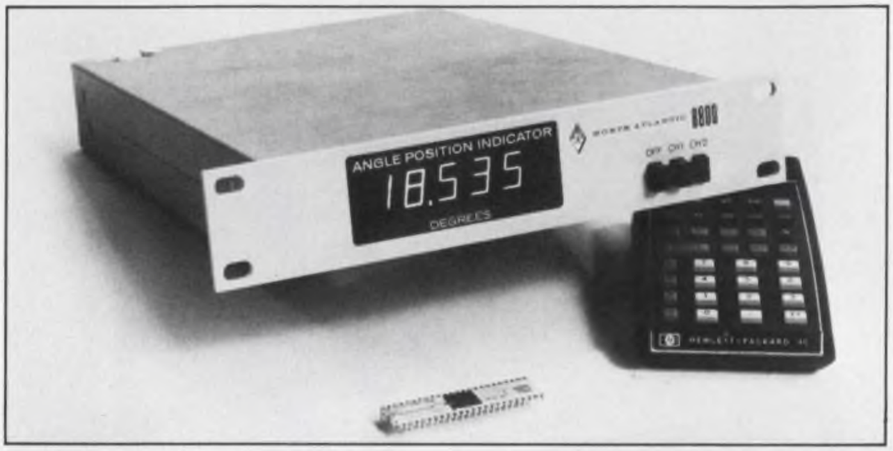
Key specs of the Cal-Tek 200 include a frequency accuracy of $\pm 3\%$ and a maximum tempco of 150 ppm/°C. The linearity of the frequency modulation is $\pm 0.3\%$.

How good are the waveshapes? Sinusoidal distortion stays within $\pm 0.7\%$, triangle nonlinearity is less than 1%, and the square-wave symmetry doesn't go off by more than $\pm 2.5\%$. Transition time of the square wave is 300 ns.

The Model 200 sells for a remarkably low $239, and is shipped from stock.

CIRCLE NO. 303

Angle-position indicator shrinks in size but not performance



North Atlantic Industries, 200 Terminal Dr., Plainview, NY 11803. (516) 681-8600. See text.

North Atlantic's 8800 angle-position indicator is one of the smallest around, yet it offers some of the highest performance.

Weighing in at only 4 lb. and measuring just 1-7/8 × 9 × 12 in., the 5-1/2-digit 8800 resolves 0.005 degrees, with 0.005-degree accuracy. And the diminutive $1875 price includes autoranging so that you can attach 11.8, 26 or 90-V synchros or resolvers without reprogramming.

You needn't worry about phase-shift errors either. The 8800's autophasing circuit compensates for phase shifts up to +30 degrees.

Optimized for ATE use, the North Atlantic unit is pin programmable from the rear and contains all I/O needed for computer or other programming. Pushbuttons at the front select either of two input channels.

Booth No. 495 Circle No. 305

INSTRUMENTATION

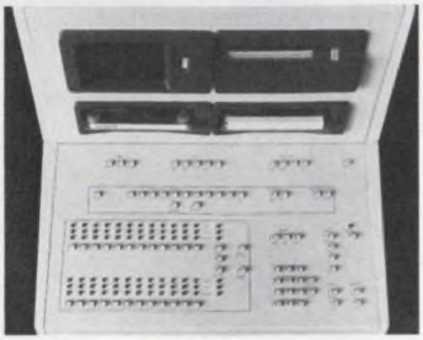
Dual filter falls off at 24-dB/octave rate

Ithaco, 735 W. Clinton St., Ithaca, NY 14850. (607) 272-7640. $665.

Model 4302 dual filter is a general-purpose filter with frequencies selectable from 10 Hz to 1 MHz, with 10 steps per decade. Specs include distortion of 0.005% at 20-V pk-pk output, 25-μV self-noise, 100-dB outband rejection, and 100-dB crosstalk attenuation. Frequency accuracy is 3%.

Booth No. 568 Circle No. 307

IC tester programs from 'cookbook recipes'



Teradyne, 183 Essex St., Boston, MA 02111. (617) 482-2700. $39,000; 20 weeks.

With J401 TTL IC test system, you can communicate directly with a device under test without a programming middle man. The system performs full functional and dc parametric tests, datalogging, plotting, and sorting. It can operate in either a go/no-go or a full-evaluation mode. Key to the software simplicity is a technique called "cookbook programming." Via the CRT, the system interacts with the operator, who uses a dedicated keyboard to fill in blanks, and accept or reject existing test-program "recipes."

Booth No. 434 Circle No. 308

Counter-timer holds readings for 1 year

Kessler-Ellis, Atlantic Highlands, NJ 07716. (201) 291-0500. $120; 3 wks.

This new electronic 4-digit totalizing counter, interchangeable with standard electromechanical counters, combines a liquid-crystal display with 1-year battery standby. The counter operates directly from the built-in battery, which continuously recharges from the power line. On power failure, the counter will hold count and display for up to 1 year. The hooded housing is physically interchangeable with the international 25 × 50-mm panel cutout.

Booth No. 681 Circle No. 309

New from Centralab...

CERBON™ TRIMMER RESISTORS

Affordable Stability... 300% More Stable Than Carbon... at a Carbon Trimmer Price!

Why pay more? With Centralab's new *CERBON* trimmers you get stability approaching cermet and at carbon prices ...As little as 28¢ in distributor 1,000 quantities; as low as 10¢ in high volume orders.

The secret of *CERBON* superior performance? A totally new thick film resistor element, which combines both potentiometer and conventional thick film technologies, *plus* a heat stable ceramic substrate, *plus* a dual-tine contact spring, *plus* "Fluxgard" protection from dust and wave soldering contaminants. In short, a totally balanced electromechanical system.

Look at these benefits:
• TCR less than −400 ppm/°C. • CRV less than 2% of maximum resistance. • Rotational life exceeds 500 cycles. • Adjustability (typical)—0.05% of total voltage. • High overload capability—1 watt at 25°C ambient for 1,000 hours exhibits less than 2% cumulative resistance change. • Maximum stability in humid environment—Resistors exposed to an atmosphere of 40°C at 95% relative humidity for 300 hours return within four hours to +2.5% of their initial readings.

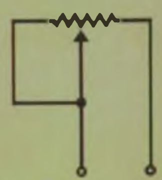
CERBON trimmers are offered in a resistance range of 1 K ohm to 1 megohm with a choice of standard PC terminal configurations. They fit universally accepted circuit board mounting patterns. And they're ready now for fast delivery in any quantity.

Write for complete technical data on Centralab's new *CERBON* trimmer resistors. Or call (915) 779-3961 for a free evaluation sample. Move up to *CERBON* and save!

Knob colors available in white, blue, red and green for ease in assembly operations.

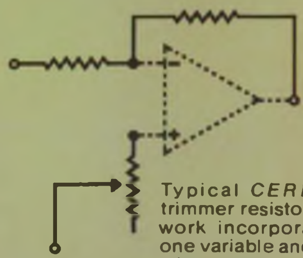
AVAILABLE CIRCUIT OPTIONS

Thanks to their ceramic substrate, Centralab *CERBON* trimmers permit a variety of screen printed circuit options. Here are three typical circuits:



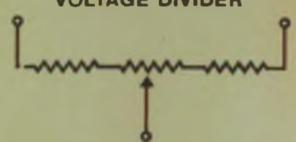
TERMINAL SHORTING
One of five electrical termination options available.

OPERATIONAL AMPLIFIER NETWORK



Typical *CERBON* trimmer resistor network incorporating one variable and two fixed resistors on dual substrate configuration.

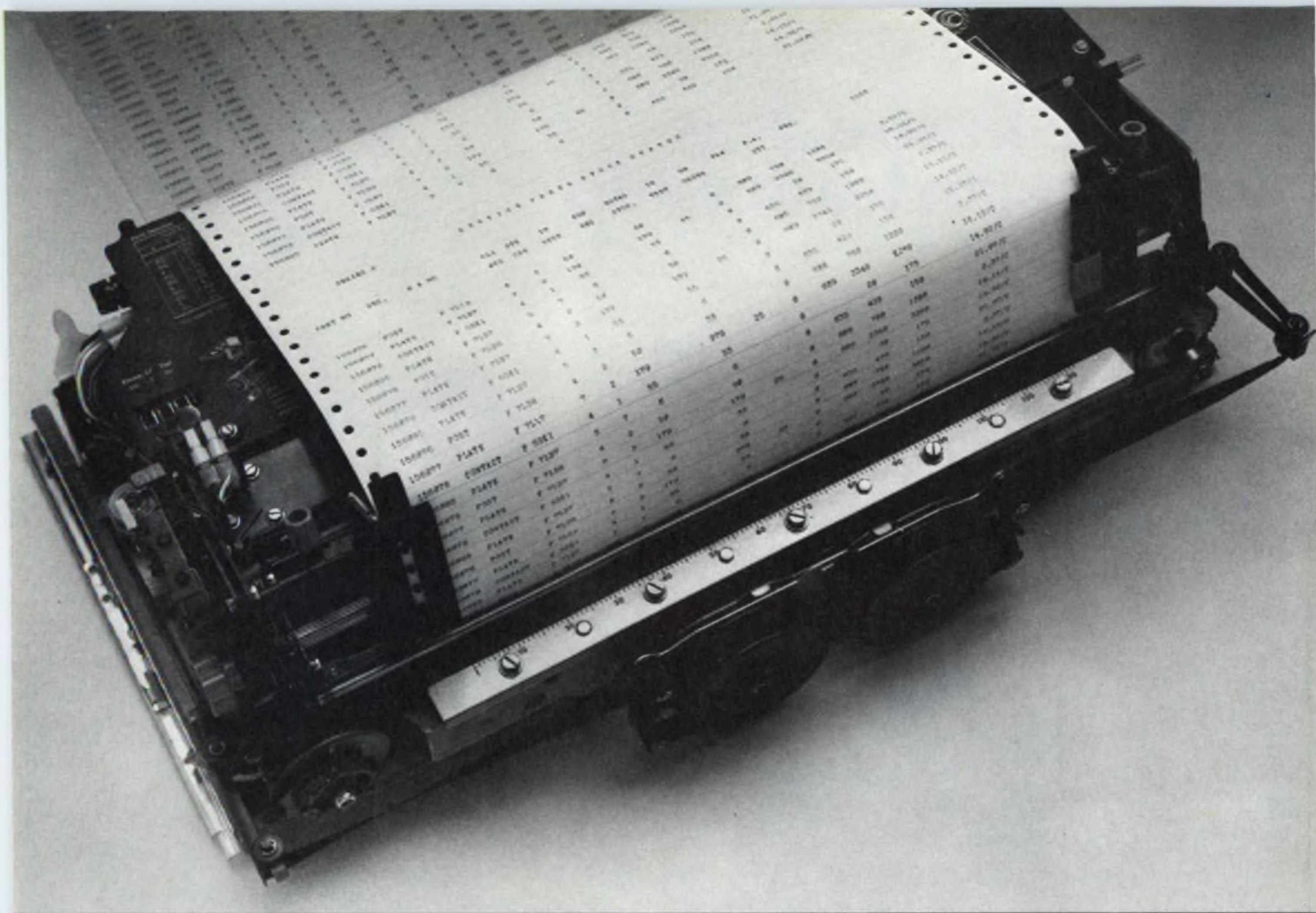
VOLTAGE DIVIDER



Fixed and variable resistors can be ratio matched for precise values and to insure temperature tracking. Eliminates need for costly discrete resistor selection.

CENTRALAB
Electronics Division
GLOBE-UNION INC.
7158 MERCHANT AVENUE
EL PASO, TEXAS 79915

CIRCLE NUMBER 144



The Teletype® model 40 OEM printer. When you look at it from price and performance, you'll find it difficult to look at anything else.

The fact of the matter is simply this:
We don't think any other printer can even come close to the model 40.

And that's no idle boast. Not when you consider the facts.

Consider: Where else can you get a 132-column, heavy-duty impact printer that delivers over 300 lines per minute for less than $2000, or an 80-column printer for under $1400?

The big reason behind the model 40's price/performance advantage is our unique design. Even though it operates at speeds of more than 300 lpm, wear and tear is less than you'd find in a conventional printer operating at considerably slower speed. Fewer moving parts and solid-state components add up to greater reliability and reduced maintenance.

Here's something else to consider: Where else can you get a printer that delivers the kind of flexibility and reliability the model 40 offers?

For complete information, please contact our Sales Headquarters at:
5555 Touhy Ave., Skokie, Ill. 60076. Or call Terminal Central at: (312) 982-2000.

TELETYPE

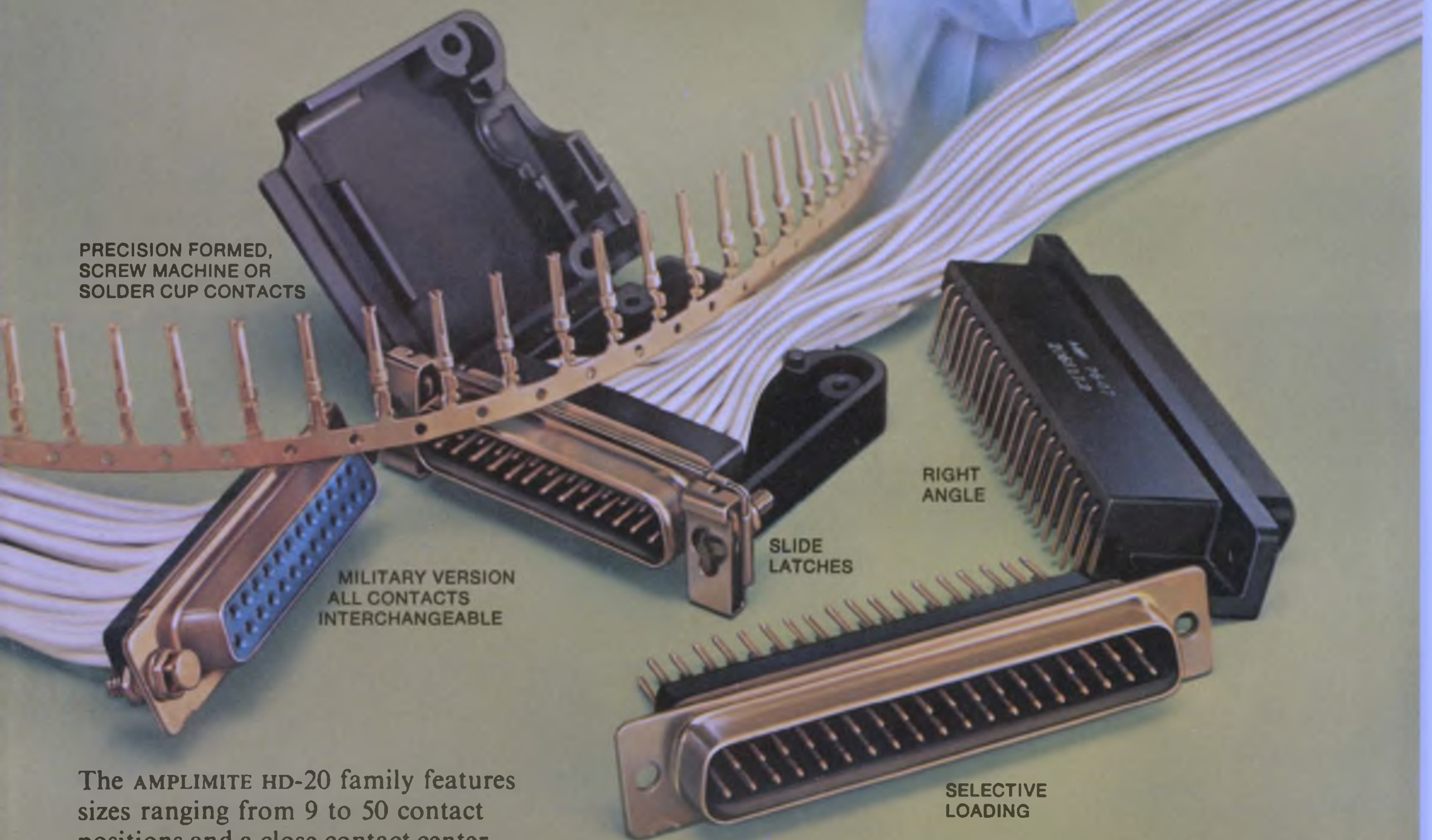
The Teletype model 40 OEM printer. Nothing even comes close.

CIRCLE NUMBER 71

It's the little extras that mean leadership

Both families of AMPLIMITE connectors incorporate exclusive performance features that can help reduce production costs. And with the use of the recently introduced AMP miniature Stripper/Crimper Machine, they can be reduced even further.

Also both families can help you technically. Take the AMPLIMITE HD-22 family, for example. It offers higher density with contacts spaced as close as .090″. Choose from sizes ranging up to 104 positions.



The AMPLIMITE HD-20 family features sizes ranging from 9 to 50 contact positions and a close contact center-line spacing of .109″. Each family is recognized under the component recognition program of Underwriters Laboratories. And the military versions of each (HDM) meet the requirements of MIL-C-24308 and its latest amendments.

For more information on AMPLIMITE miniature connectors just call customer service: (717) 564-0100. Or write AMP Incorporated, Harrisburg, PA 17105.

AMP
INCORPORATED

SEE US AT
BARCELONA SONIMAG SHOW

Logic analyzer zeros in on μP-based systems

Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, CA 94304. (415) 493-1501. $5000; 10 wks.

Hewlett-Packard's 1611A logic analyzer dedicates itself to μP systems and may be the forerunner of the new look in analyzers.

The 1611A hooks right into the μP's socket and, simultaneously, to eight other points. The unit displays read/write or I/O activity directly in the alphanumeric mnemonics of the μP's instruction set.

Gone are the ONEs and ZEROs or mapping displays of previous models. Also gone are the toggle switches used to set the trigger conditions in most analyzers.

At present, the HP instrument "specializes" in systems using either 8080 or 6800 μPs. You can change from one to the other with personality boards or modules—changeover is a 15-min. operation (extra module costs $1000).

Because a keyboard controls what is displayed, as well as other trigger conditions, you may well call the 1611A a selective-trace device.

You can select traces by triggering on a specified address, data word, or—on the eight auxiliary probes—any combination of ONEs, ZEROs and "don't cares." Or you can key-in some combination.

More significantly, instead of selecting a simple break-point trigger, you can choose address ranges. That is, you can set the trigger to be less-than-or-equal-to or more-than-or-equal-to limits on the address magnitude.

You can further modify the triggering by setting in a "pass count" of up to 256 repetitions before triggering occurs. And you can specify enable and disable conditions to set boundaries for a selected window.

Booth No. 449 to 458 Circle No. 304

Modular recorders let you fulfill your needs

Gould Inc., Instrument Systems Div., 3631 Perkins Ave., Cleveland, OH 44114. (216) 361-3315. Start at $2700; 45 days.

The 2000 series of single and multichannel direct-writing recorders are modular in design and incorporate the best features of the company's previous recorders, plus a number of innovations. The modular design allows a user to select the number of channels (1 to 6), channel width (100 or 50 mm) and from a wide range of optional plug-in or external preamplifiers, input power options and portable case or rack mounting.

CIRCLE NO. 413

CIRCLE NUMBER 76

Semiconductor tester works in-circuit

B & K Precision, 6460 W. Cortland Ave., Chicago, IL 60635. (312) 889-8870. $250; stock.

Model 530 semiconductor tester measures transistor cut-off frequency (F_t) up to 1500 MHz. Measurements are made in three ranges and displayed on one large meter. The unit is automatic and allows in-circuit testing and lead identification of diodes, transistors, FETs and SCRs, even in low-impedance circuits. Applied test currents are: collector, 125 mA at 4% duty cycle; base, 250 mA at 4% duty cycle (HI drive) 1 mA, at 4% duty cycle (LO drive). The test repetition rate is 10 times per second.

Booth No. 459-461 Circle No. 310

Calibration standard offers 0.01% accuracy

RFL Industries, Boonton, NJ 07005. (201) 334-3100. $2250; Nov.

Model 82 precision voltage and current standard offers the following features: ac/dc volts from 100 mV to 10 V; ac/dc current from 100 μA to 100 mA; percentage deviation dial and fractional scale division. Frequency range is 50 to 1 kHz internal, to 25 kHz external. Accuracy specifications extend to 0.01% in dc and 0.05% in ac mode.

Booth No. 350 Circle No. 320

Panel counter comes in DIN standard case

Newport Laboratories, 630 E. Young St., Santa Ana, CA 92705. (714) 540-4914. From $250; 30 days.

Digital counter, Model 6130, mounts on a front panel and can be programmed from the rear connector for frequency, frequency ratio, time interval, period, period average, totalize and stop watch. Sixteen selectable gate times are also available from the rear connector. Full-scale count is 99,999 on 1/2-in. LED digits. Parallel BCD outputs are buffered and gated and a/d isolation is 350 V. The case is a DIN standard with a panel cutout requirement of 92 × 45 mm.

Booth No. 582 Circle No. 321

Meter measures volts, amps and watts

Yokogawa Corp. of America, 5 Westchester Plaza, Elmsford, NY 10523. (914) 592-6767. $1307; stock.

A new dc-coupled digital V-A-W meter features an accuracy of ±0.25% for dc, true rms, ac and dc with superimposed ac voltage, current and power. Ranges of the 2514-16 include voltage from 30 to 300 V, current from 0.5 to 10 A and power from 15 W to 3 kW.

Booth No. 274 Circle No. 322

Pocket DMM sneers at 10-foot heights

Sencore, 3200 Sencore Dr., Sioux Falls, SD 57107. (605) 339-0100. $148; stock.

Pocket portable DMM, Model DVM36, features 3-1/2-digit readout, with 0.5% of reading accuracy on dc V in a compact, lightweight (less than 1 lb) drop-proof case. A "push on" switch in the probe turns the entire unit on during a measurement. After the measurement, release the button and the entire unit is off, drawing no current. The Cycolac case is designed to withstand 10 ft drops onto concrete and go right on working.

Booth No. 689, 691 Circle No. 323

Interactive terminal prints and mates with any protocol

LogAbax, U.S. Div., 10889 Wilshire Blvd., Los Angeles, CA 90024. (213) 477-0494. See text.

Selecting an interactive terminal has been simplified with the introduction of the LX1010 printing terminal from LogAbax. The LV1010 is versatile since it is compatible with all computer protocols and can print at rates of up to 180 characters per second.

An internal microprocessor-based controller lets the terminal communicate in ASCII, BCD and Telex codes at speeds from 75 to 4800 baud, either synchronously or asynchronously. Operation in full-duplex, half-duplex and echoplex modes is possible.

The terminal keyboard is totally programmable; you can lay out the standard alphanumeric keys in any sequence on the keyboard. An extra 10-key cluster is also included to ease file creation. You can use either an IBM card or delimiter field entry format. There are also 12 special message keys that can be used to eliminate repetitive typing in certain data entry operations. The special functions are keyboard programmable; just put the terminal into a program mode and enter the instructions.

Inside the LX1010 is an 8008 microprocessor-based controller with 8-k bytes of reprogrammable read-only memory (the first 4-k bytes, though, can be ROMs) and 1-k bytes of random-access memory. The keyboard consists of 53 alphanumeric keys and space bar, a numeric keypad (10 numeric keys plus start, correction, minus and comma keys) and a 12-key function pad with eight indicator lights.

The printing unit is the company's LX180CL printer, which can handle paper widths to 15 in. and prints up to 132 columns at 10 characters per inch. The print mechanism is a nine-needle matrix that permits you to underscore or extend the printing or select an italic or slanted type face.

You can, as an option, order a seven-pin matrix print head if you don't need the print flexibility. The number of lines per inch is also switch-selectable: either six or eight.

Options for the LX1010 terminal include: extended RAM space, up to 7-k bytes in 1-k increments, digital display of eight digits plus sign, a delta digital display of three digits plus sign, print speeds of 140 or 180 char/s, densities of 12 or 16.5 char/in., expandable character set—up to 128 items—and different character fonts.

Prices for the LogAbax LX1010 terminal start at $200/month on a lease contract and about $6000 for outright purchase. Delivery is 30 to 60 days.

CIRCLE NO. 301

Tape-cartridge system connects to CPUs

Qantex, 200 Terminal Dr., Plainview, NY 11803. (516) 681-8600. $2570 w/interface; 30 days.

The Model 2200 cartridge-tape-storage system may be interfaced to DEC's PDP-11, Data General's Novas, the Intel 8080, Rolm computers and others. The system uses the 3M DC300A data cartridge. The tape drive has a read-write speed of 30 in./s, a rewind speed of 90 in./s, and a packing density of 1600 phase encoded bit/in. Either one or two cartridge-tape drives may be used, with a storage capacity of 5.76 Mbyte for a dual drive system. The drives are available with either a 1-track, 2-track or 4-track read-after-write head. Each track is selectable either by computer or by manual control. The interfaces to the PDP-11 and Nova computers are designed to be software compatible with the cassette systems supplied by DEC and Data General. The Model 2200 requires 5.25 in. of rack space.

Booth No. 994 Circle No. 324

PROM programmer also duplicates and tests

Spectrum Dynamics, 11B North Ave., Burlington, MA 01803. (617) 273-1850. $1250; 30 days.

The PR-2 PROM programmer can duplicate patterns and test PROMs without additional equipment. The programmer does basic parametric tests of PROMs as part of the program/verification cycle. The PR-2 tests output leakage and verifies programmed parts with worst-case fanout loads and supply voltages. It also simulates temperature testing. As a programmer, the instrument comes with either a hexadecimal or octal keyboard to input data and address information.

Booth No. 261 Circle No. 325

System emulates ROMs with a plug-in RAM unit

Data I/O Corp., P.O. Box 308, 1297 N.W. Mall, Issaquah, WA 98027. (206) 455-3990. Romulator: $450, Ram-Pak: $150.

A ROM emulator system contains two units, called a Ram-Pak and a Romulator. The Ram-Pak, which is battery powered, contains 1-k × 8 of random access memory. The Ram-Pak is loaded with data from either a programmer or from the Romulator. The Ram-Pak plugs directly into the PROM socket in your circuit. The data in the Ram-Pak are easily altered, as required, until you are satisfied with system operation. When the information is correct it may be transferred directly into a PROM programmer. The Romulator incorporates a hex keypad with supporting address and data displays; it features complete address control. A SET key is used to jump between addresses; CLR is used to erase Ram-Pak data contents.

Booth No. 849, 851 Circle 326

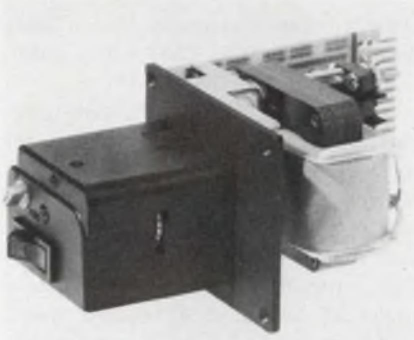
PC card connects LSI-11 to tape storage

Qantex, 200 Terminal Dr., Plainview, NY 11803. (516) 681-8600. See text; 60 days.

Users of DEC's LSI-11 computer can connect it to a Qantex data-storage system using the 3M DC300A data cartridge as the storage medium. Depending on the system, from 22.3 to 180 Mbits may be stored. Data transfer at rates up to 48-k bit/s. The card is plugged into the LSI-11 card cage and then one of the manufacturer's drive systems, Models 2200, 2400 and 2710, is connected. The interface card and the Model 2200 single-drive system sell for $2815 (unit qty).

Booth No. 994 Circle No. 327

Paper-tape reader handles 350 char/s



Addmaster Corp., 416 Junipero Serra Dr., San Gabriel, CA 91776. (213) 285-1121. See text; 2 wks.

A series of paper-tape readers runs at 350 char/s, yet costs as little as $151 for a single unit. Called the 640 "Data Loader" Series, it will read all standard 5, 6, 7 or 8-level tapes. All employ LED light sources and hermetically sealed phototransistors. The motor needs 115 V ac at 10 W, and an additional supply of 5 V dc at 10 to 20 mA is also required. Model 640-1 ($172, 1-49 qty.) uses Schmidt-triggered LS-TTL amplifiers and output drivers. Model 640-2 ($172, 1-49 qty.) uses Schmidt triggered CMOS data amplifiers, and Model 640-3 ($151, 1-49 qty.) just has phototransistors with emitter resistors.

Booth No. 962 Circle No. 328

Electrostatic plotter runs at 1600 line/min

Gould Inc., 3631 Perkins Ave., Cleveland, OH 44114. (216) 361-3315. $7560; 45 days.

An electrostatic printer/plotter, the Model 5005, prints 1600 line/min at 132 char/line. It uses a 64-char set and also plots graphics at a maximum speed of 3.25 in./s. The resolution is 100 dots/in. Computer generated graphics and alphanumerics are produced on 11-in.-wide coated paper in 400-ft reels or on 100-sheet fan-folded paper. The unit has a staggered-stylus writing head, and puts a matrix of dot charges on the paper. On-line, direct memory access interfaces are available for IBM 360/370, PDP-11, HP2100, and Nova computers. Software includes a plot graphics package and specialized application packages.

Booth No. 556 Circle No. 329

Portable data terminal has cassette storage

Micon Industries, 252 Oak St., Oakland, CA 94607. (415) 763-6033. $1995; 30 days.

The Cassetterm contains a built-in mini-cassette recorder, which permits storage and transmission of up to 40-k alphanumeric ASCII characters. The unit also combines, in a single mobile unit, a battery power supply, a full keyboard, 32-character LED display and telephone-handset acoustic coupler. The Cassetterm is battery-powered. Data appear for verification on the alphanumeric LED display prior to storage on the mini-cassette. The data on the mini-cassette can be transmitted over the telephone directly to a central computer at 300 baud, using the built-in Bell-103-compatible modem.

CIRCLE NO. 330

Digital-cassette unit features low cost

Memodyne Corp., 385 Elliot St., Newton Upper Falls, MA 02164. (617) 527-6600. $775 (large qty); 2-4 wks.

Designated the Model 2333, this recorder writes 7-bit ASCII or 8-bit parallel data onto standard cassettes at data rates up to 50 char/s. These data may then be read back on the same recorder or any other 2333 at the same rates. Two tracks are used, in a complementary non-return-to-zero format. Tape motion is controlled by a stepping motor. The 2333 comes in a portable case with simple front panel controls, I/O connectors, and internal power supplies. Data search capabilities are provided along with high-speed rewind.

CIRCLE NO. 331

PROM programmer uses data from hex keyboard

Technitrol, 1952 E. Allegheny Ave., Philadelphia, PA 19134. (215) 426-9105. 1702A version: $935; stock.

The Model 107K can be used to program the following PROMs: the Intel 1702A, 2704/08, and 3601; the NS 5202/03 and 5204; the Signetics 82S23/82S123; the Harris 7602/03, 7610/11, 7620/21, 7642/43/44, and the Fairchild 93436/46. The unit is supplied factory-set for one of these types. The 107K features hex-keyboard entry of data and address, and automatic copying from one PROM to another between selectable minimum and maximum address. It will verify patterns while reading or writing, and stop on a detected error.

Booth No. 1022 Circle No. 332

PB switches offered with snap/wiping action

Dialight Inc., 203 Harrison Pl., Booklyn, NY 11237. (212) 497-7600. $1.65 (1000-up); stock.

Low-cost and of computer-grade, the 554 series are illuminated pushbutton switches. The series includes snap-action switches with either gold or silver contacts, and wiping-action switches with gold contacts. Switch action can be either of the momentary or alternate-switching type. A choice of 200 cap shapes, sizes and colors is available. Rear or snap-in mounting is available in either a direct panel-mount or bezel-mount configuration, with four sizes to choose from. The switches are UL-listed and CSA-approved.

Booth No. 892-894 Circle No. 333

Slide switch's two parts allow easy cleaning

Chicago Switch Inc., 2035 Wabansia, Chicago, IL 60647. (912) 489-5500. $0.52: SPST (1000 up); stock.

Chicago Switch says that it has solved the problem of wave soldering slide switches onto PC boards. "Presently, PC boards and their components, except switches, are wave soldered and cleaned, and only then are the switches hand soldered onto the board. If the switches are wave soldered and cleaned together with the other components, the switches often become contaminated with flux." Chicago Switch's new Mr. Clean switch comes in two pieces. The switch's bare assembly is either machine or hand mounted on the PC board, wave soldered and cleaned together with the other components. Because it's open, it cleans easily. The upper assembly is then snapped over the base. Available in SPST, SPDT, DPDT and form Z circuit configurations, its size compares to the Mini-Mike series of precision miniature slide switches. Samples and illustrative catalog data may be obtained by stating requirements and applications.

Booth No. 943 Circle No. 334

Get servo performance from rugged gearmotors

The Pittman Corp., Sellersville, PA 18960. (215) 257-5117. $13 to $25 (1-9).

Designated Series GM 9413, the new gearmotors provide dc servomotor performance combined with a rugged spur-gear reducer available in five standard ratios from 5.9:1 to 728:1. Motor diameter is 2 in., length, 3.5 in. excluding output shaft extension, and output-shaft speeds extend from 2 to 650 rpm. Gears are made of sintered iron to precision tolerances, and the gearbox's strength limit is 1000 oz-in. The motors feature a skewed armature that provides very low magnetic cogging.

Booth No. 507 Circle No. 335

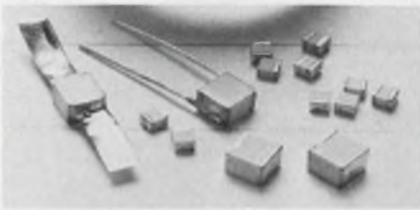
Keyboard provided with plug-on circuitry

Staco Inc., 1139 Baker St., Costa Mesa, CA 92626. (714) 549-3041. $0.44 per station: opaque (1-9); $8 to $14: Adder Board.

The new optional plug-on Adder Boards, containing BCD encoding or other signal-processing circuitry, help reduce design and packaging problems to a single keyboard/adder-board module. A keyboard bezel makes mounting from the front of the panel fast and inexpensive. Connector pins speed installation. The keyboard's life is over 5,000,000 cycles. Keyboards are available with unlighted opaque keybuttons, or with LEDs mounted in transparent colored keybuttons. Key-top markings or decorative decals are color coordinated to the keyboard.

Booth No. 709-711 Circle No. 336

Chip capacitors marked by laser



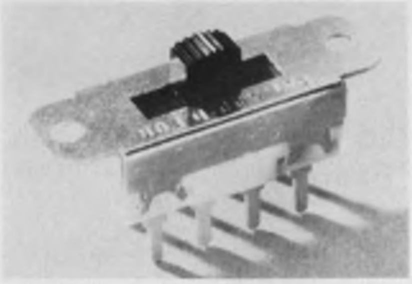
American Technical Ceramics, One Norden Lane, Huntington Station, NY 11746. (516) 271-9600.

High-Q, high-reliability uhf/microwave chip capacitors, in both leaded and unleaded styles, are available in values to 1000 pF with tolerances as tight as ±0.1 pF. They meet or exceed all requirements of MIL-C-11272C. ATC can laser-mark chip capacitors as small as the ATC 55-mil case Size "A" for the positive identification of capacitance values. Verify this for yourself with the Nikon microscope at Wescon and receive a complimentary copy of the revised pocket-sized ATC "RF Capacitor Handbook."

Booth No. 1153 Circle No. 337

COMPONENTS

Slide switch provides two or three positions



Switchcraft, Inc., 5555 N. Elston Ave., Chicago, IL 60630. (312) 792-2700.

New Tini slide switches feature a snap-slide lifting and wiping action and a double-wipe concept in two and three-position units. Terminals are sealed in molded terminal boards to guard against the migration of contaminants through the board to internal contact areas. The housing is cadmium-plated steel; terminals are a silver-plated copper alloy; and the sliders are silver on a copper-alloy bi-metal. Contacts are rated 0.5 A, 125 V ac or dc for a noninductive load. Minimum switch life is 6000 cycles; 10,000 cycles with dry-circuit load.

Booth No. J11-13 Circle No. 338

Pressure transducer uses quartz sensor

Setra Systems Inc., 12 Huron Dr., Natick, MA 01760. (617) 655-4645. $875 to $975 (unit qty).

A barometric pressure transducer, Model 250, achieves high accuracy within 0.05% of full scale by incorporating the new Setraquartz sensor. Self-contained electronics provide a 5-V-dc full-scale output signal. Barometric pressures are accurate to ±0.3 millibars over three months. The transducer also may be used with clean dry gases such as air over ranges to 30 psia or 30 psig with an accurate to ±0.1% of full scale over three months. The sensor is a variable-capacitance quartz capsule that achieves accuracy through its monolithic, symmetrical and homogeneous design. In addition, quartz has the desirable qualities of very-low thermal expansion and super-low hysteresis. The unit draws only 8 mA at 24 V dc.

Booth No. 259 Circle No. 339

Thermistors qualified for use in space

Yellow Springs Instrument Co., Inc., Box 279, Yellow Springs, OH 45387. (513) 767-7241. Stock.

A new series of space-qualified thermistors has been added to the YSI line of precision interchangeable thermistors. Included are 13 units with resistances from 2252 Ω to 1 MΩ at 25 C and interchangeability tolerances of ±0.1 and ±0.2 C. Each thermistor is individually tested and documented per GSFC S-311-P-18/01 for extended space-flight application.

Booth No. 729 Circle No. 340

Linear actuator operates on heat

Thermal Hydraulics Corp., 7045 N. Grand Ave., Glendora, CA 91740. (213) 963-5980.

The TH 750 is an electrically controlled heat motor for linear actuation. It can provide a stroke to 3/4 in. with a force up to 250 lb. The device is compact, consumes little power (30 W), is silent and operates on 24 V ac or dc. The device has a variety of applications including latch releasing, damper operation and valve actuation. It can be operated as an on-off device or modulated for position control.

Booth No. 116 Circle No. 341

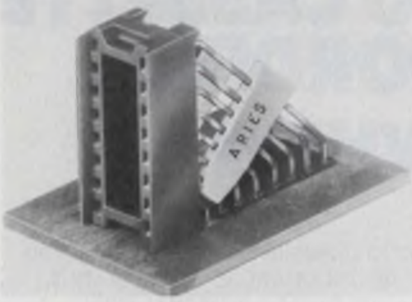
Capacitor standards combine to four figures

Arco Electronics, Community Dr., Great Neck, NY 11022. (516) 487-0500. See text.

A new series of 37 precision standard capacitors, type SS, provides values from 0.0001 to 1 μF with an accuracy of ±0.1% ±0.5 pF at 1000 Hz and 25 C. The units are much smaller and lighter than other designs of comparable accuracy, according to Arco. A kit of 32 units (0.0001 to 0.5 μF) and a four-position adapter jig in a case is priced at $750. The adapter enables you to combine capacitances to obtain desired values to four significant figures.

Booth No. 710 Circle No. 342

DIP LED sockets have several mounting angles



Aries Electronics, Inc., P.O. Box 231, Frenchtown, NJ 08825. (201) 996-4096. 98¢ to $2.85.

A series of 8 to 40-pin sockets for optoelectronic digital display devices, called Vertisockets, features a variety of mounting angles for either vertical, 30, 45, 60, 90 degree, or horizontal applications. Pins come with 0.200, 0.300, or 0.600-in. center-to-center spacing. The design is said to give a firm mounting. The bifurcated pin contacts accept either flat or round leads, and can be gold or tin plated.

Booth No. 235 Circle No. 343

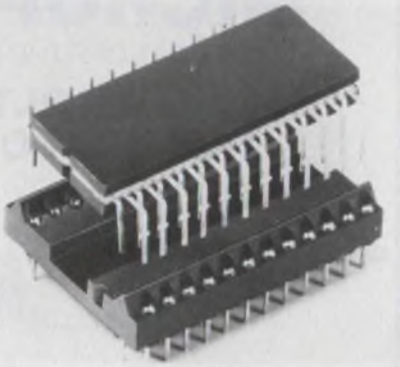
Shipping modules hold 19-in. rack units

W. D. Adam Co., Inc., 630 W. Seventeenth St., Costa Mesa, CA 92627. (714) 646-4488. $6.75 to $9.05 plus inserts; stock.

A line of shipping modules can hold practically all 19-in. rack-mount instruments having a wide range of heights and depths. Six basic sizes of modules, called Cushion-seals, plus a frame-like insert, called Expan-Serts, are available. As many Expan-Serts can be used as needed, to expand case size. Because of their interlocking design, the assembled parts form an integrated package structure. The average weight runs 3 to 4-1/2 lb per package.

Booth No. 211 Circle No. 344

48-pin socket mates with LSI devices



EMC, 96 Mill St., Woonsocket, RI 02895. (401) 769-3800. $2.32 (10 up).

A 48-pin Quil socket mates with the Motorola family—the M10800 series—of bipolar LSI devices. The socket features a design for easy loading and extraction. It has a low profile, and four-finger contacts provide more reliable lead connections and greater resistance to vibration. The socket body is made of high temperature phenolic and will not soften during soldering. The closed-end terminals prevent solder wicking.

CIRCLE NO. 345

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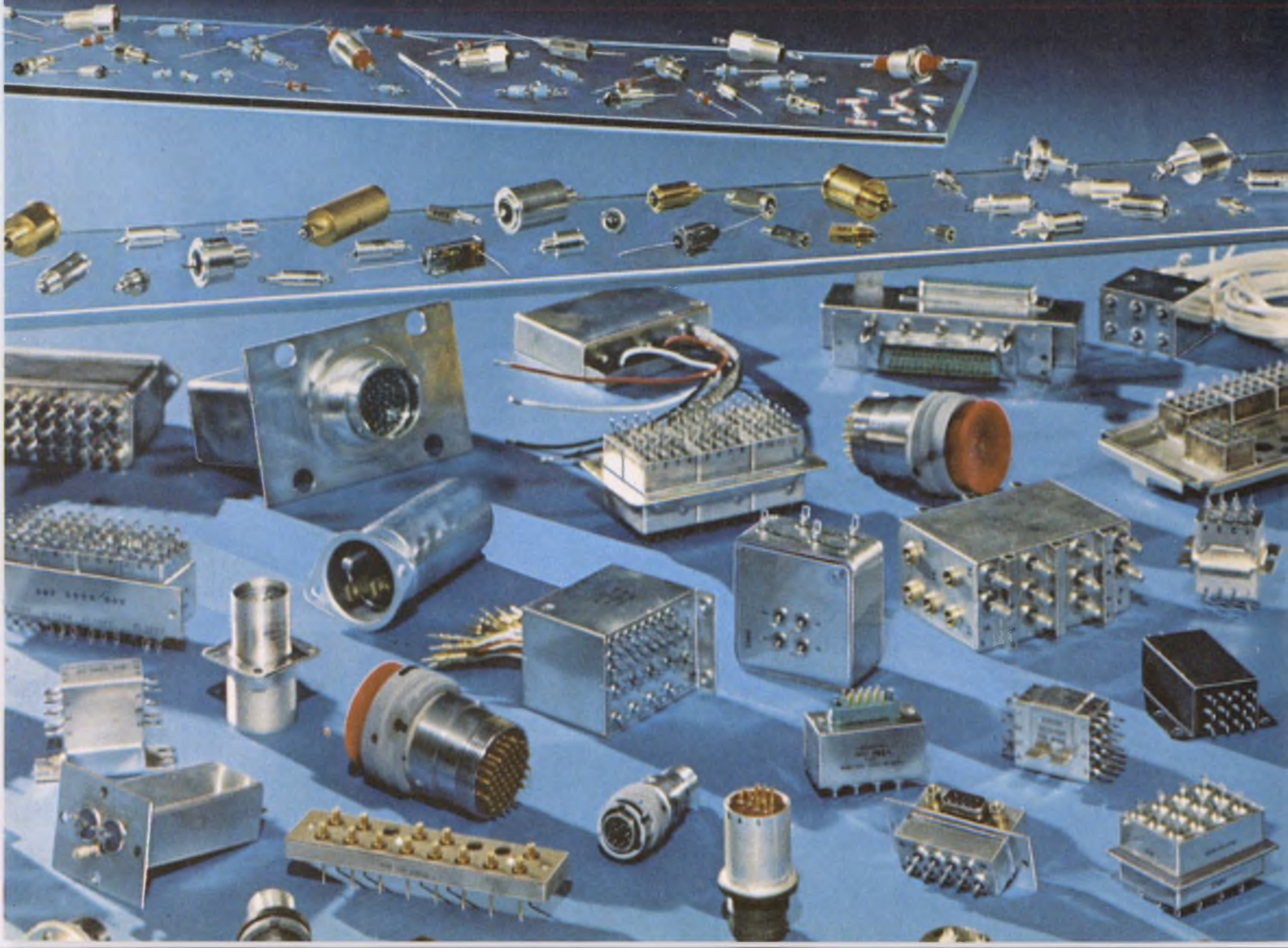


Attach and insulate wires in one operation

General Staple Co., Inc., Autosplice Div., 220 E. 23rd St., N.Y., N.Y. 10010. (212) 674-4369. See text.

A laminated strip system, called Insulsplice, both joins and insulates electrical connections. The system uses an applicator machine and a continuous coil of plastic/metal laminated strip. In use, the operator positions electrical wires or components in the applicator machine. The machine then feeds a length of laminated strip, cuts it, and forms it around the items to be joined in one operation. Insulated connections made with this system eliminate sleeving and taping after a connection is crimped. The laminated strip consists of a plastic dielectric of polyester and brass and comes in standard widths of 3/8, 1/2 and 3/4 inches. The system can join and insulate from two 28-AWG to four 14-AWG wires. Insulated splices made with this system cost from $5 to $9 per thousand connections. Between 1,500 to 2,500 connections may be made per hour.

CIRCLE NO. 346

μP program module runs a test chamber

Tenney Engineering, Inc., 1090 Springfield Rd., Union, NJ 07083. (201) 686-7870. $1475 (single channel).

A programing module called the Digitenn uses a microprocessor in place of mechanical devices to control the company's environmental test chambers. It can be used in place of older cam, two-point, or punched-tape programmers. The Digitenn controls temperature and humidity setpoints, slope rate, dwell time, and secondary functions such as mode selection. It digitally displays the activated modes. With this programmer, there are no cams to cut, tapes to punch, or timers to set. The operator introduces setpoints, times and rates of change, and the time of program completion. The chambers simulate temperature, humidity and altitude.

Booth No. 106 Circle No. 347

◀ CIRCLE NUMBER 93 for DATA
◀ CIRCLE NUMBER 136 for SALESMAN CALL

INTEGRATED CIRCUITS

16-k word ROM has max access time of 550 ns

Mostek, 1215 W. Crosby Rd., Carrolton, TX 75006. (214) 242-0444. $14.85 (1000-up); stock.

A 16-k bit ROM, the MK31000P-3, has a maximum access time of 550 ns even if the single +5 V supply varies by ±10%. The ROM is organized as 2-k × 8 and is a pin-for-pin replacement for the Intel 2316A/8316A and the General Instrument RO-3-8316A. The MK 31000P-3 is TTL compatible, has a maximum power dissipation of 330 mW and is completely static.

CIRCLE NO. 348

Electronic watch circuit has multiple languages

Nortec Electronics, 3697 Tahoe Way, Santa Clara, CA 95051. (408) 732-2204. Under $3 (lge. qty.); stock.

A six-function alphanumeric LED watch chip, the 5055, can be programmed to display the day of the week in any one of 10 foreign languages. The metal-gate CMOS device displays on command hours and minutes, rolling to seconds after 1.5 seconds of display. The presence of one or two colons indicates AM or PM. The chip typically draws 3 μA at 3 V dc but the on-chip segment drivers can deliver 10 mA when activated.

CIRCLE NO. 349

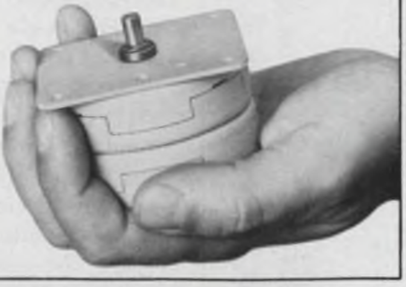
CMOS multiplexers accept 8 or 16 channels

Teledyne Philbrick, Allied Dr. at Rte. 128, Dedham, MA 02026. (617) 329-1600. $28 (lge. qty.); stock.

The 4551, a differential 8-channel multiplexer, and the 4552, a 16-channel single-ended multiplexer, feature overvoltage protection even with power removed. They have break-before-make operation, Schmitt trigger inputs, and CMOS and TTL/DTL compatibility. Both are CMOS and come in 28-pin hermetic DIPs. Break-before-make delay is typically 80 ns, switching time is 500 ns, typical, and input resistance is 1.8 Ω maximum.

CIRCLE NO. 350

Introducing the efficient little 82900 stepper motor



It gives you an edge on compactness, torque and price.

It's new. It's bidirectional. It has a 7.5° step angle. It gives you maximum pull-in/pull-out torque of 23 oz-in @ 200 pps. It's rated at 12.38w @ 5vdc and runs at lower than average temperatures.

The 82900 has a lot to offer, particularly in impact and non-impact printers, small X-Y plotters and computer peripherals. It's powerful, compact and moderately priced. And it's reliable. So reliable — in fact — that it can also be used to control pumps and valves in medical instruments and similar devices. In many applications it can replace larger, bulkier steppers at much lower cost.

Standard construction provides 2-phase operation (requiring simplified, low-cost circuitry), a 7.5° step angle and roller bearings. However, 4-phase operation, a 15° step angle or sleeve bearings can be furnished as options.

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- RFI capabilities

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CIRCLE NUMBER 100

INTEGRATED CIRCUITS

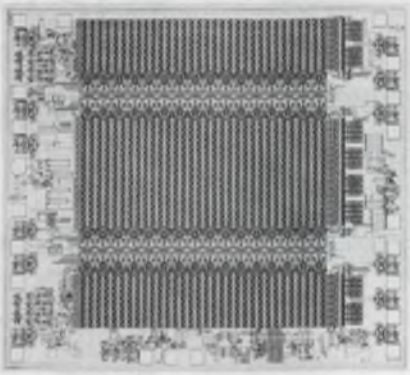
CMOS clock circuits offer seven functions

Synertek, 3050 Coronado Dr., Santa Clara, CA 95051. (408) 241-4300. $10.75 (100-up); stock.

Two CMOS watch circuits, the SY5001 and SY5002, offer seven time functions. The SY5001 is designed to drive 6-digit LCDs giving hours/minutes/seconds/month/date and the day. It also automatically adjusts the calendar function for leap year. The 5001 operates at a maximum of 3 μA average battery current and it can be ordered with either a 12 or 24-hour display option and either European or American format. The second chip, the SY5002, is similar to the 5001, but can drive a LED display. The SY5002 has an average battery current of 10 μA, maximum as well as Euopean date option, automatic calendar update and two optional brightness controls.

CIRCLE NO. 351

4-k MOS RAMs offer access time of 200 ns



Monolithic Memories, 1165 E. Arques Ave., Sunnyvale, CA 94086. (408) 739-3535. From $10 (100-up); stock.

Two 4-kilobit dynamic MOS RAMs, the 2180 and 2180-4, are available housed in 22-pin DIPs. The 2180 has a maximum access time of 200 ns over the full 0-to-70-C temperature range while the 2180-4 offers a 270-ns access time. Both products are compatible with the National 5280 series.

CIRCLE NO. 352

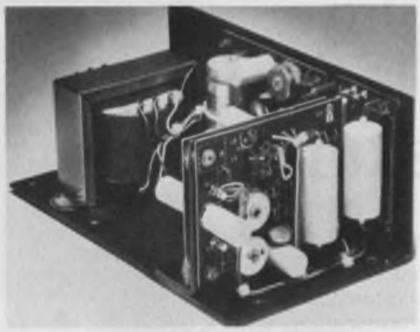
CMOS timebase circuits just need a crystal

Intersil, 10900 North Tantau Ave., Cupertino, CA 95014. (408) 996-5000. $3.05 (100-up); stock.

The ICM7051A and the ICM-7051B CMOS timebase circuits are intended for automobile applications. Each circuit contains the oscillator, dividers, output drivers and over-voltage protection circuitry. An external, 4.19 MHz quartz crystal is needed to drive the oscillator. In the ICM7051A a bridge output provides a 64 Hz square wave for synchronous motor applications. In the ICM7051B a 31.2 ms output pulse at 1 Hz rep rates is available for stepper motor applications. The circuits typically dissipate less than 4 mW at 12 V. Operating voltages range from 4.5 to 22 V at an ambient of 20 C, and from 7 to 17 V over −20 to +85 C. The circuits are available in 8-pin plastic DIPs or as chips.

CIRCLE NO. 353

Single unit powers microprocessor



Standard Power, Inc., 1400 S. Village Way, Santa Ana, CA 92705. (714) 558-8512. $69 up; last quarter 76, stock.

The SMP series dc power supplies are compatible with microprocessors produced by major manufacturers. All are multiple output units offering various combinations of 5, 9 and 12 V dc as required by individual microprocessors. All units regulate to within ±0.1% for both line and load, with typical ripple 0.1% (0.5 to 2 mV rms). Input power of 115 or 230 V ac, 47 to 440 Hz can be used. They have automatic fold-back current-limiting short-circuit protection, adjustable from 20 to 150% of the rated loads; a response time of 50 μs; temperature coefficients of 0.02%/°C; operate over a temperature range of 0 to 50 C; and are built to UL standards. They are available in several wattage ranges from 40 to 160 W.

Booth No. 524 Circle No. 354

Line regulators condition 100-kVA power

Topaz Electronics, 3855 Ruffin Rd., San Diego, CA 92123. (714) 279-0831. $7750 to $14,400; 4 wks.

Ac line regulators rated at 50, 75, and 100 kVA are designed for operating voltages of 120/208 and 277/480-V. The regulators provide ±3.3 to ±7% line regulation, better than 1% load regulation, 98% efficiency, less than 0.1% harmonic distortion and respond in less than 1 cycle. The regulators may be used separately or in combination with the company's line of isolation transformers to provide protection from line noise, line voltage variation, or both.

Booth No. 982, 984 Circle No. 355

Upgraded dc supplies come with lower prices

Adtech Power Inc., 1621 S. Sinclair St., Anaheim, CA 92806. (714) 634-9211. See text.

The EAPS series of dc power supplies is designed to provide improved reliability and performance over former OEM lines. Yet lower prices have been achieved. According to the company, the EAPS series now has these features: all hermetically sealed semiconductor devices; a 100-W output stage; a zener protected regulator in the 12-to-24-V units; a computer-grade, 10-year-life capacitor used on most units; reverse polarity protection and inductive load protection standard on 12-to-24-V units; electrostatically shielded transformer with high-frequency suppression capacitors; automatic-foldback current limiting; no overshoots due to turn-on, turn-off or power failure; and an improved potentiometer. The EAPS series comes in three sizes, rated 15 to 20 W, 30 to 50 W and 50 to 80 W. All units have a regulation of ±0.05% for line, ±0.1% for load, a ripple of 5 mV pk-pk max, and a temperature coefficient of 0.02%/°C. Typical price for the EAPS 5-3, 5 V at 3-A supply is $19.40 in 1000-unit lots.

Booth No. 840 Circle No. 356

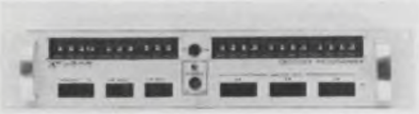
Dc-to-dc converter now unregulated

Bikor Corp., 1228 253 St., Harbor City, CA 90710. (213) 325-2820. $127 to $500 (1-24 qty); stock to 4 wk.

The DDU series dc-to-dc converters is unregulated. Forty-eight models provide inputs and outputs of 12, 24, 48, 110 V dc in power ranges from 48 through 220 W. Ripple is 0.5% max. Series DDR and ADR are regulated converters. DDR with 136 models is dc to dc; ADR, with 34 models, is ac to dc. Both ADR and DDR offer linear or switching regulators with 0.2% regulation and 0.3% ripple. Single through four output models are standard. Inputs are available in 12, 24, 48, 110 V dc and 110 V ac 50 to 400 Hz. Outputs range from 5 through 250 V dc with up to 180 W per output. Overvoltage protection is optional.

Booth No. 182 Circle No. 357

Ac power sources made IEEE-bus compatible



Elgar Corp., 8225 Mercury Court, San Diego, CA 92111. (714) 565-1155. See text; last quarter, 76.

A modified programmable interface to link your computer with Elgar's line of ac power sources offers IEEE-bus compatiblity. The unit, a decoder programmer, can be used with ac power sources that deliver up to 10.5 kVA. The programmable interface was previously available only with simple parallel BCD inputs. The programmer can control frequency, from 45 Hz to 10 kHz, phase voltage and phase angle (for multiphase power). The IEEE-bus interface capability adds from $455 to $2000 to the cost of a typical power system.

Booth No. 491 Circle No. 358

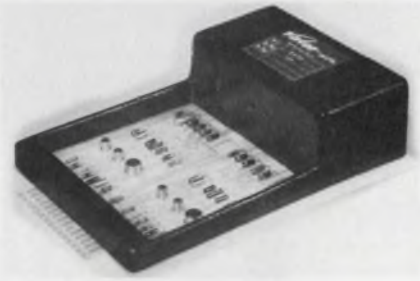
Open-framers keep cool

Faratron Corp., 280 Green St., South Hackensack, NJ 07606. (201) 488-1440. Start at $33 (100); stock.

The OEM-AD-152 Series of dual-output, open-frame supplies is UL recognized and emphasizes thermal design and heat dissipating construction. Operation is said to be up to 50% cooler. These features include a heavy-gauge, anodized aluminum chassis (capable of 3-surface mounting), IC regulators, socket-mounted power transistors, quick-disconnect terminals, and more. All models are adjustable from ±12 to ±15 V dc with full power output supplied at 45 C. Output currents are 0.5, 1 and 3 A.

CIRCLE NO. 359

Dual supply card plugs into your logic rack



Valor Instruments Inc., 1122 Llewellyn, Torrance, CA 90501. (213) 320-5471. $70-$100; 2 wk.

The 6600 series dual dc supplies are mounted on an epoxy glass circuit board. Rails are provided for use in a standard rack using a PC connector or direct wiring. Outputs range from 5 through 28 V, factory set to within 1% of the desired voltage, at 5 W per output. Specifications are: 105 to 125 V ac at 47-to-400-Hz input, output bipolar ±5 to 28 V dc, line and load regulation 0.1%, ripple and noise 1 mV rms max., tracking error 1%, tempco 0.01%/°C.

CIRCLE NO. 360

Supplies list MTBF of 100,000 h

Modular Power, 4818 Ronson Ct., San Diego, CA 92111. (714) 279-1641. From $60; stock-4 wks.

The PSM series of miniature dc power supplies features an MTBF greater than 100,000 h at 25 C. Models are available in single output voltages of 5, 12, 15, 24, 28 and 250 V dc. Output currents range from 0.05 to 1.5 A. Typical regulation is 0.03% line and load, ripple is 500 μV, with 1% preset voltage accuracy. All models are protected against short circuit and overload conditions.

CIRCLE NO. 361

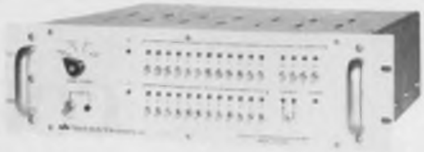
Digital input controls two dc voltages

Systron-Donner, Concord Instrument Div., 10 Systron Dr., Concord, CA 94518. (415) 676-5000. $3500.

The Model DPSD-50 is a digital power source, featuring two independent 0-50 V, 1 A floating-output digitally controlled dc power sources. Both supplies can be controlled via a computer's I/O circuits. This power source is suited for use in automated test systems and process control where fast, accurate settings of dc power outputs are required. Manual settings are also available on the front panel. Addressable memory responds to only a pre-selected one of 32 possible address codes. Inputs are optically isolated to eliminate ground loops. Power supply outputs are floated with respect to the digital inputs and to one another. An IEEE 488 interface is available, as an option, for data programming.

CIRCLE NO. 362

Constant V/I source programs remotely



North Hills Electronics, Glen Cove, NY 11542. (516) 671-5700. $2800; stock-30 days.

Model DCVS-220 digitally programmable constant current/voltage source features bipolar operation with currents of 2.5 μA to 300 mA at ±100-V compliance, and voltages of ±0.025 V to ±100 V in 0.025-V steps at 300 mA. Remote selection of voltage is made though 12 binary bits plus one polarity bit, while current is selectable through 16 bits. Local control is available through the use of front-panel switches. Output regulation of the unit is 25 ppm from no load to full load, 5 ppm for input line ranges, and 15 ppm/°C over a temperature range of 15 to 35 C.

CIRCLE NO. 363

Dc block connectors resist thermal shock

Omni Spectra, 21 Continental Blvd., Merrimack, NH 03054. (603) 424-4111. $15 to $18; 5-8 wks.

Seven new OSM dc block connectors feature patented "shock absorber" construction and are especially resistant to thermal shock and vibration. Five of the new units offer four-hole flange-mount construction. One comes with a two-hole flange. Another is for bulkhead feedthrough. A variety of other flange and feedthrough models and adaptor units are available.

CIRCLE NO. 364

18-GHz switches work in less than 20 ms

Sivers Lab, Box 42018, S-126 12 Stockholm 42, Sweden.

Series PM 7555 and PM 7557 are spdt-switches with SMA connectors. Size is only 30 × 49 × 13 mm, including contacts. Other specs: frequency coverage of dc to 18 GHz, impedance of 50 Ω, insertion loss of 0.2 dB at 4GHz, 70-dB isolation and input VSWR less than 1.10. Power handling is 50 W average, 1-kW peak, and switching time is less than 20 ms.

CIRCLE NO. 365

Crystal detectors show high sensitivity

Narda Microwave, Plainview, L.I., NY 11803. (516) 433-9000. $185; stock.

Models 503 and 4503 miniature crystal detectors operate over the frequency range of 10 to 18 GHz. Extremely low VSWR ($<$ 1.8) and high sensitivity (0.4 mW/μW), with excellent square-law characteristics, make the units ideal for broadband swept measurements. These new SMA and type N detectors have the added advantage of field replaceable diodes.

Booth No. 460-462 Circle No. 366

Spectrum analyzers cover up to 40 GHz

Nelson-Ross, 5 Delaware Dr., Lake Success, NY 11040. (516) 328-1100. 630, $7750; G31, $7100; 632, $5975; 15 wks.

Three compact, solid-state spectrum analyzers for rf, vhf, uhf and microwave applications have frequency spans adjustable up to 2 GHz. Phase-locked narrow spans provide jitter-free spectrum displays with resolution to 300 Hz. A zero-span receiver mode displays modulation waveforms. The new series includes: Model 630 covering 10 MHz to 40 GHz in seven overlapping bands; Model 631, a 10-MHz to 40-GHz unit with six overlapping bands; and Model 632, which covers 500 kHz to 2 GHz in one band.

Booth No. 566 Circle No. 367

Unit checks out radio-relay systems

Scientific Atlanta, 3845 Pleasantdale Rd., Atlanta, GA 30340. (404) 449-2000. $11,825; 10-12 weeks.

Model 4680 radio performance analyzer performs baseband and i-f tests on microwave radio-relay systems. Baseband amplitude response, noise-power ratio, and spurious-tone search tests can be made in less than five minutes. The unit performs the measurements normally made with a combination of a selective-level meter, white-noise test set and i-f spectrum analyzer. Test results are recorded on an X-Y plotter.

CIRCLE NO. 368

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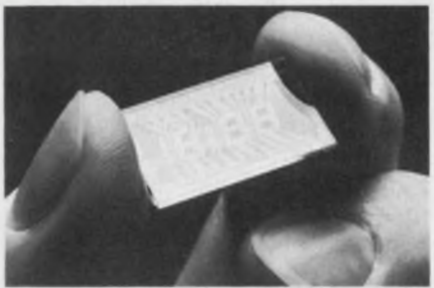
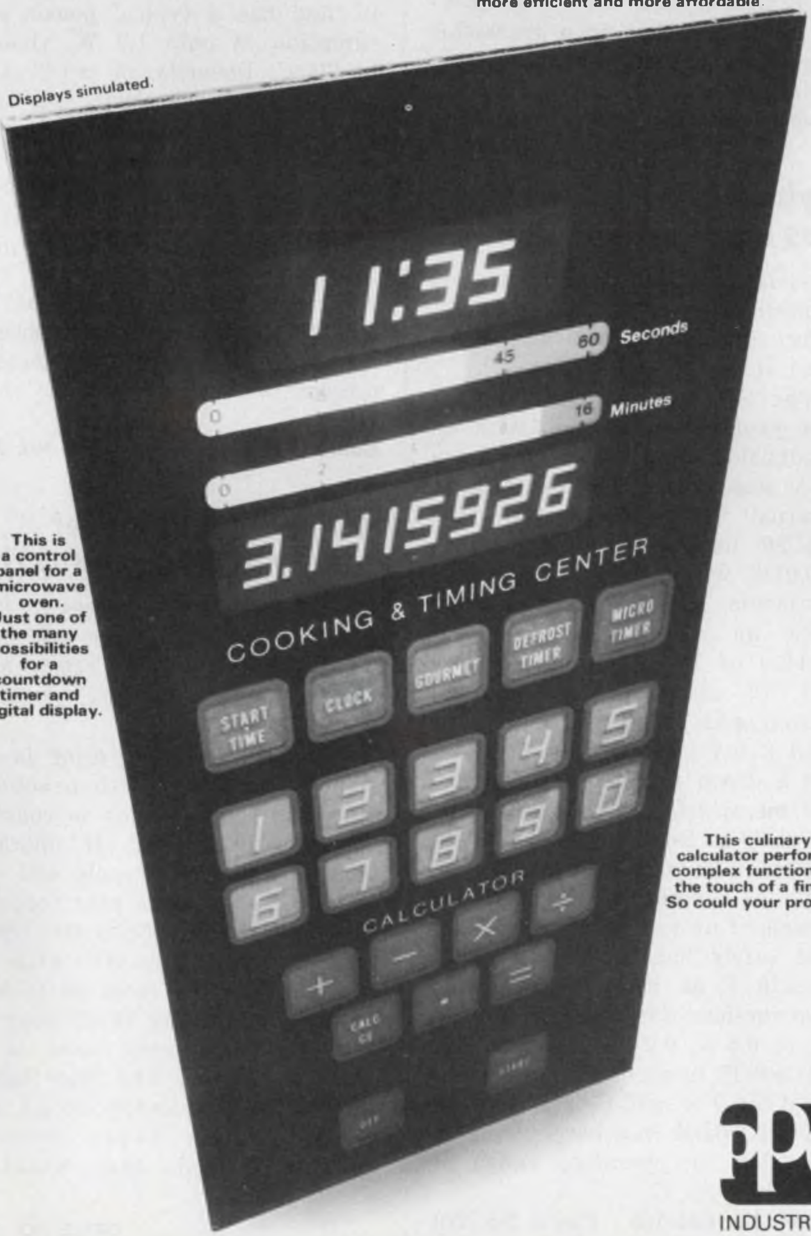
Which means you can literally change the faces of appliances, timepieces, visual displays, and instrumentation of every description.



Digital watches will never be the same. Electronic glass can make them more efficient and more affordable.



Displays simulated.

This is a control panel for a microwave oven. Just one of the many possibilities for a countdown timer and digital display.

This culinary calculator performs complex functions at the touch of a finger. So could your product.

The secret is the permanent conductive metallic-oxide coating on the glass.

It can be made to trigger functions at the mere touch of a finger. Like timing a roast, choosing a station, starting the wash, or even figuring the square root of 34.

In short, if it can be done electronically, it can probably be done a little better with electronic glass.

And, since the coating can be applied to form letters, numbers, or any visual display imaginable, there's almost no end to what you can do.

Digital clocks, wristwatches, speedometers, odometers, oscilloscopes, and radar screens are just a few of the obvious possibilities.

As for its reliability, there's really nothing to go wrong. No moving parts. No knobs, dials, switches, buttons—just glass.

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CIRCLE NUMBER 114

Voltage monitor module senses line trouble

Calex Manufacturing, 3305 Vincent Rd., Pleasant Hill, CA 94523. (415) 932-3911. $49 (unit qty.); stock to 2 wks.

The Model 829 Linesensor is designed to protect equipment against brown-out and overvoltage conditions. It monitors the average voltage of the ac line and provides a positive-logic indication of an out-of-tolerance condition. Also, the unit can sense sudden drops in ac line voltage. Accuracy to set trip points is 0.5 V, rms and response times are 100 ms for a change in average voltage and 16 ms for a line drop-out. The Linesensor comes in two versions: one with a relay output that has a 1-A, 26-V-dc contact rating or a transistor open-collector output that can sink up to 50 mA.

Booth No. 158 Circle No. 369

Hybrid s/h amplifier has holding capacitor

Burr-Brown, International Airport Industrial Park, Tucson, AZ 85734. (602) 294-1431. From $25 (100-up); stock to 4 wks.

The SHC80 sample-hold amplifier provides unity gain with an acquisition time of 10 μs for a 10-V step input. Complete with an internal holding capacitor, the SHC80 has an accuracy within ±0.01% without any external adjustments. The DIP-packaged units have an acquisition time (to 0.01%) of 10 μs for a 10-V step and 12 μs for a 20-V step. Throughput offset voltage is less than 2 mV. At 25 C, the SHC80 has a droop rate of less than 0.5 mV/ms, which increases to 10 mV/ms at 70 C. Input impedance is 10^8 Ω in parallel with 5 pF and the input bias current is 400 nA. Input signals of up to ±15 V can be handled safely but the output range is ±10 V at ±5 mA, maximum. Two versions are available, both in 0.8 × 0.5 × 0.2-in. packages. The SHC80KP, in an epoxy package, is rated for 0 to +70-C operation and the SHC80BM in a hermetic metal case, has an operating range of −25 to +85 C.

Booth No. 503-505 Circle No. 370

Data-acquisition system housed in 32-pin DIP

Micro Networks, 324 Clark St., Worcester, MA 01606. (617) 852-5400. From $140 (100-up); 2 to 4 wks.

Housed in a 32-pin hermetic DIP is a complete 8-channel 8-bit data-acquisition system—the MN-7100. The unit combines the latest MSI and LSI circuits with nichrome, thin-film technology. The system measures only 2.14 × 1.16 in. and has a typical power consumption of only 1.2 W. Over 0 to 70 C, linearity is ±1/2 LSB and absolute accuracy is ±2 LSB. At 25-C absolute accuracy is ±1 LSB. Typical acquisition time of the system is 5 μs, the aperture time, 50 ns and the a/d conversion time 6 μs—adding up to a typical throughput rate of 90,000 conversions per second. Each of the MN7100's eight channels accepts signals in the ±10-V range and presents an input impedance of 10 MΩ.

Booth No. 839 Circle No. 371

Active squelch filter can span 50 to 5000 Hz

KTI Microelectronics, 1999 S. Bascom Ave., Suite 910, P.O. Box 1222, Campbell, CA 95008. (408) 371-5880. From $15 to $25; stock to 4 wks.

The FB-239 active filter is designed for use as both a squelch filter and tone encoder in communications equipment. It operates from a 5 to 15-V supply and can be adjusted over a center frequency range of 50 to 5000 Hz. Filter gain is typically 20 dB ±0.5 dB and Q can range from 40 to 150. Frequency stability is 25 ppm/°C and equivalent input noise is 50 μV rms, typical. The filter has a current drain of under 300 μA and is available in 14-pin hermetic DIPs or in 9-pin edge mounting plastic packages.

CIRCLE NO. 372

Complete 8-bit DACs come in 18-pin DIPs

Micro Networks, 324 Clark St., Worcester, MA 01606. (617) 852-5400. From $16 (100-up); stock.

The MN3013 and MN3014 are complete 8-bit d/a converters housed in hermetically sealed, 18-pin DIPs. Both hybrid units are complete and ready to use without adjustments. The converters have a guaranteed linearity of ±1/2 LSB over the full operating range of 0 to 70 C. Full-scale output settling time to ±1/2 LSB is 23 μs for the MN3013 and 1.5 μs for the MN3014. Four user selectable output ranges of 0 to +10, 0 to −10, ±5, and ±10 V are standard.

Booth No. 839 Circle No. 414

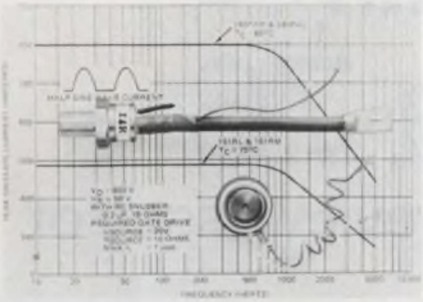
Power dc motor drive has 1000-pps step rate

Superior Electric, 383 Middle St., Bristol, CT 06010. (203) 582-9561. $265 (module only), $410 (with supply); stock.

Designed to provide the correct switching sequence to control bifilar wound dc stepping motors, the PIM151 Slo-Syn preset indexer is available as either a module or complete with power supply. The 5.75 × 11-in. module can completely control the motor speed, direction and distance. An internal oscillator provides stepping rates of up to 1000 pulses per second. Counting circuits assure that the motors are driven the correct number of steps, up to a maximum of 99,999 selected by external BCD switches. Other externally controlled functions include Index, Start, Run, and Jog. A Count Complete signal is issued upon completion of motor motion. The module requires 24 V at 6 A and 5 V at 1 A and operates over 0 to 40 C.

Booth No. 1052-54 Circle No. 415

Fast-switching SCRs rated at 1200 V, 400 A



International Rectifier, 233 Kansas St., El Segundo, CA 90245. (213) 678-6281, $87; 151RM 100, $94.05; 240PAM 100 (10 to 99); stock.

A series of fast-switching SCRs rated for operation to 1200 V and 400 A rms, designated 151RL/RM and 240PAL/PAM, features turn-off times as fast as 25 μs through 1000 V and 30 μs through 1200 V. Model 151RL/RM SCRs are in JEDEC TO-93 stud-mounted cases and offer a current rating of 245 A. Model 240PAL/PAM units are in JEDEC TO-200AB pressure-mounted Hockey-Puk cases and have a current rating of 400 A. Improved dynamic operation of the SCRs is ensured by high rate-of-rise ratings for both turned-on current (di/dt) and off-state voltage (dv/dt). Maximum di/dt is 800 A/μs and reapplied dv/dt is 200 V/μs for all units.

CIRCLE NO. 373

Rf power transistor delivers 175 W on 28 V

Communications Transistor Corp., 301 Industrial Way, San Carlos, CA 94070. (415) 592-9390. $55 (100 to 499); stock.

The S175-28, a rugged rf power transistor—the highest-power 28-V single-sideband unit on the market, according to CTC—offers an output power of 175 W, linearity and a high safe operating area. It's designed especially for the output state of a high-power linear amplifier. Guaranteed minimum intermodulation distortion is −32 dB at full power and minimum gain is 14 dB. The S175-28 is 100% tested for infinite VSWR at all phase angles at full CW output power.

CIRCLE NO. 374

P-i-n diodes switch with low distortion

Unitrode Corp., 580 Pleasant St., Watertown, MA 02172. (617) 926-0404. $1.35 (1000 up); stock.

Low distortion is guaranteed for land-mobile and CB-radio antenna switches using UM9401 p-i-n diodes. Transmit harmonic distortion at 50-W transmitter power is 0.5 μW (80-dB below carrier), which is 20-dB below present FCC requirements. Better performance is available at lower power levels. Intermodulation distortion during the receive state is specified at better than 60-dB below the carrier at +10 dBm (10 mW) input power. Transmitter power greater than 100 W can be handled. Antenna switches incorporating the UM-9401 have reliability and mechanical stability characteristics that are better than electromechanical relays, according to Unitrode.

CIRCLE NO. 375

Electronic Design
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announces a special Oct. 25 preview issue of

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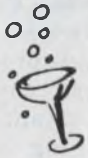

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Design Aids

Guide to CB

A pocket-sized booklet called "A Guide to CB" describes the principles of CB operation and includes charts explaining connectors, and a glossary of CB jargon. Automatic Radio, Melrose, MA

CIRCLE NO. 376

Protection-system tapes

A pocket-sized product guide to resilient protection-system tapes outlines properties of a dozen "Scotchfoam" urethane and vinyl-foam tapes and "Scotch" polyurethane-film tapes. Information is arranged in easy-to-read chart form. 3M.

CIRCLE NO. 377

Bellows calculator

A "slide rule" bellows calculator aids in determining requirements for protective dust bellows. Gagne Associates.

CIRCLE NO. 378

Stationary-battery chart

A battery selection chart that compares number of plates per cell, number of cells, and other pertinent data, is available to aid in selecting the proper battery from Globe-Union.

CIRCLE NO. 379

LED optical-filter chart

The spectral characteristics of optical filters designed for use with the most commonly used LEDs is available. The charts compare the six most popular filters. SGL Homalite.

CIRCLE NO. 380

ASCII code chart

A detailed description of the ASCII code is now available as a wall chart. All 128 ASCII characters, the alphanumeric name, octal, hex and alternate code designations are included. Termiflex Corp.

CIRCLE NO. 381

Bulletin Board

Intersil is now second-sourcing **Harris HA-2500 dielectric isolation op amps.**

CIRCLE NO. 382

Spectrol has added a **bushing-mount option to its 3/4-in. Model 43 trimmers.** The new option is available in any of the three pin configurations.

CIRCLE NO. 383

TRW Power Semiconductors' power Schottky diodes have been "1N" registered and are in qualification for JAN and JANTX versions.

CIRCLE NO. 384

Digital Equipment has announced **software enabling multiple users simultaneously to access a PDP-15 or XVM system** for general-purpose computing. The software is designed for from two to six concurrent users, and will accommodate as many as 16 terminals.

CIRCLE NO. 385

Two new capabilities are available to users of **MRI/STARDYNE software on Control Data's Cybernet data services network.** One, called Constar, is a postprocessing option to prepare contour plots, and the other is an analysis capability for computing loads caused by wave motion.

CIRCLE NO. 386

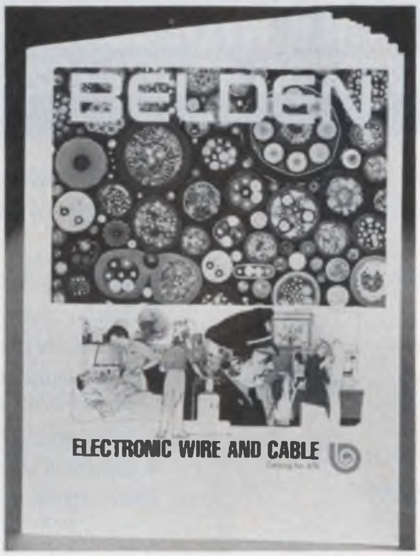
GE Information Services has restructured its **MARK III Foreground Service** pricing. Certain elements will increase approximately 10%.

CIRCLE NO. 387

A powerful Fortran IV compiler from **Computer Automation** supports the company's low-cost Series LSI-3/05 millicomputers and provides the OEM user with a practical tool for implementing applications software.

CIRCLE NO. 388

New Literature



Wire and cable

Electronic wire, cable and cord products are presented in a 100-page catalog. The catalog features expanded identification of UL-listed items, metric equivalents for all physical specifications and application-oriented product designs. Belden, Geneva, IL

CIRCLE NO. 389

Switches

Rotating cam limit switches are described in a catalog. Allen-Bradley, Milwaukee, WI

CIRCLE NO. 390

Crystal products

Key operating characteristics of crystals, precision crystal oscillators, ovens, crystal-clock oscillators, crystal filters and discriminators are covered in a 12-page catalog. CTS Knights, Sandwich, IL

CIRCLE NO. 391

Solid-state relays

A 16-page solid-state relay catalog begins with application data and principles of operation. Included are ac and dc controlled, triac and high frequency, SCR solid-state relays plus solid-state hybrid power relays. Magnecraft, Chicago, IL

CIRCLE NO. 392

Circuit-design aids

From sockets to breadboards, a 26 page catalog contains 180 products—including several complete μP educational systems. E & L Instruments, Derby, CT

CIRCLE NO. 393

Heat-shrinkable tubing

A 32-page catalog describes the company's Voltrex brand tubing. It includes property charts, product-selector guides and application data. SPC Technology, Chicago, IL

CIRCLE NO. 394

Programmable controller

A 24-page color booklet that describes read/write magnetic core memories, I/O addressing, and more sophisticated functions of a programmable calculator is available. Square D Co., Milwaukee, WI line configurations are given. Beckman Instruments, Fullerton, CA

CIRCLE NO. 395

Microwave components

A 4-page quick reference guide to the company's microwave diodes and transistors is available. Hewlett-Packard, Palo Alto, CA

CIRCLE NO. 396

Magnetic shielding

A 48-page magnetic shielding catalog/manual is divided into a 20-page product/facilities section, and a 28-page engineering section. Ad-Vance Magnetics, Rochester, IN

CIRCLE NO. 397

RFI power-line filters

"Everything you always wanted to know about RFI filters" is the title of a new catalog from Corcom, Chicago, IL.

CIRCLE NO. 398

Microwave components

A 36-page catalog covers passive microwave components. Terminations, attenuators, resistors, connectors and DC blocks are included as well as SMA coax, microstrip and stripline developments. The catalog also contains application notes. EMC Technology, Cherry Hill, NJ

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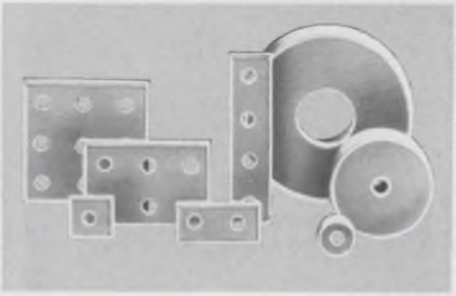

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CIRCLE/MULTI-FEED CAPACITORS 181

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OVENS—INFRARED 187

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POWER SUPPLIES 182

DIGITAL SIGNAL ANALYSIS, S. Stearns. Contains the most recent advances, brand-new design material, and a comparison between continuous and digital systems, making it an ideal master reference to today's signal processing techniques and systems. #5828-4, 288 pages, $18.95. Circle the Info Retrieval Number to order 15-day exam copy. When billed, remit or return book with no obligation. Hayden Book Co., 50 Essex Street, Rochelle Park, N.J. 07662.

DIGITAL SIGNAL ANALYSIS 185

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ELECTRONIC SURPLUS CATALOG 188

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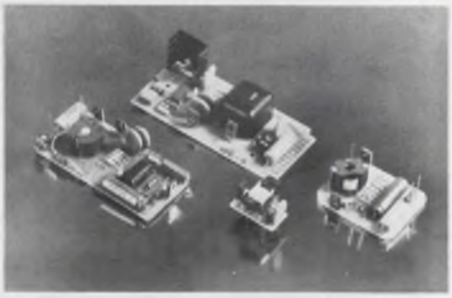
CARD GUIDES - EJECTORS 183



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CUSTOM DESIGNED POWER SUPPLIES 186

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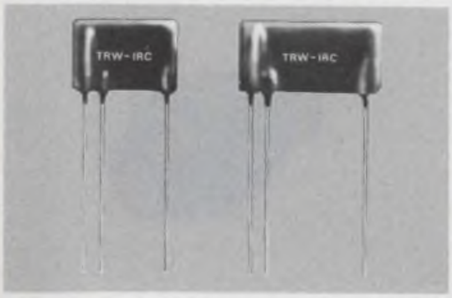
ENCODER **190**



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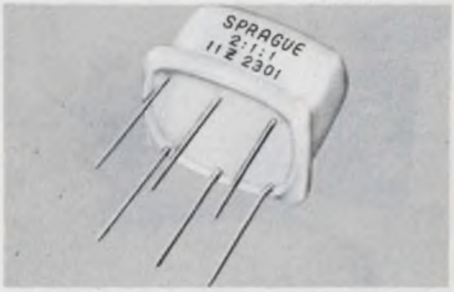
HIGH VOLTAGE RESISTORS **193**



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LED DIGITAL DISPLAYS **191**

Krohn-Hite Model 5800A function generator, budget priced at $245, offers sine, square and triangle waveforms over a range of 0.2 Hz to 2 MHz. Distortion is typically less than 0.3%. Simple 1000:1 frequency tuning dial. Pushbutton controls. 50-ohm output adjustable from 5 mv pk-to-pk to 15 volts. Auxiliary 1-volt pk-to-pk square wave output. Stock delivery. KROHN-HITE, AVON INDUST. PARK, AVON, MA 02322

FUNCTION GENERATOR **194**

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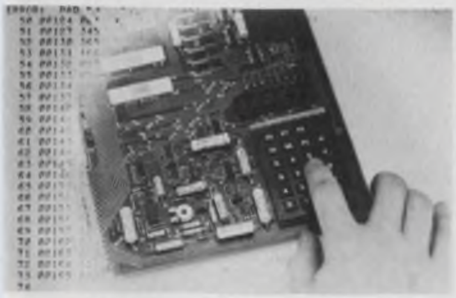
FLEXIBLE CIRCUITS KIT **197**



This **hands-on, laboratory-based** conference, November 15-19, 1976 will enable participants to design microprocessor based systems. Limit of 24. Will use class minicomputer systems and 8 microcomputer based setups with individual teletypes. One session reserved for student problems. Fee is $295. ELECTRICAL ENGINEERING, IOWA STATE UNIVERSITY, Ames, Iowa 50011. (515) 294-3016 or 2663.

MICROCOMPUTER COURSE **192**

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TRAINING TEXT **195**

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TRANSLATOR/GENERATOR **198**

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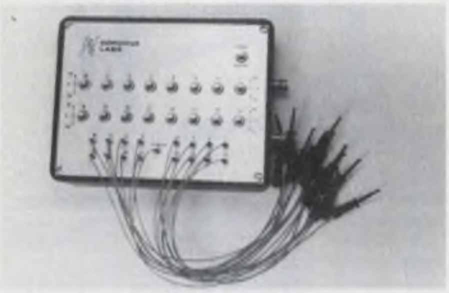

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