VOL. 21 NO.

Electronic Design 11

FOR ENGINEERS AND ENGINEERING MANAGERS

MAY 24, 1973

Micro, mini, maxi computers – They're changing to meet new demands and many engineers are finding it difficult to keep pace. New type architecture, memories, peripheral equipment, software concepts are rapidly evolving. For the latest trends in computer design, specification and use by engineers, turn to page 53.

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INFORMATION RETRIEVAL NUMBER 243

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INFORMATION RETRIEVAL NUMBER 3

VOL. 21 NO.

Electronic Design 11

FOR ENGINEERS AND ENGINEERING MANAGERS

MAY 24, 1973

NEWS

TECHNOLOGY

PRODUCTS

Departments

Cover: Designed by Anthony J. Fischetto, photographed by Steve Grohe, courtesy of Digital Equipment Corp.

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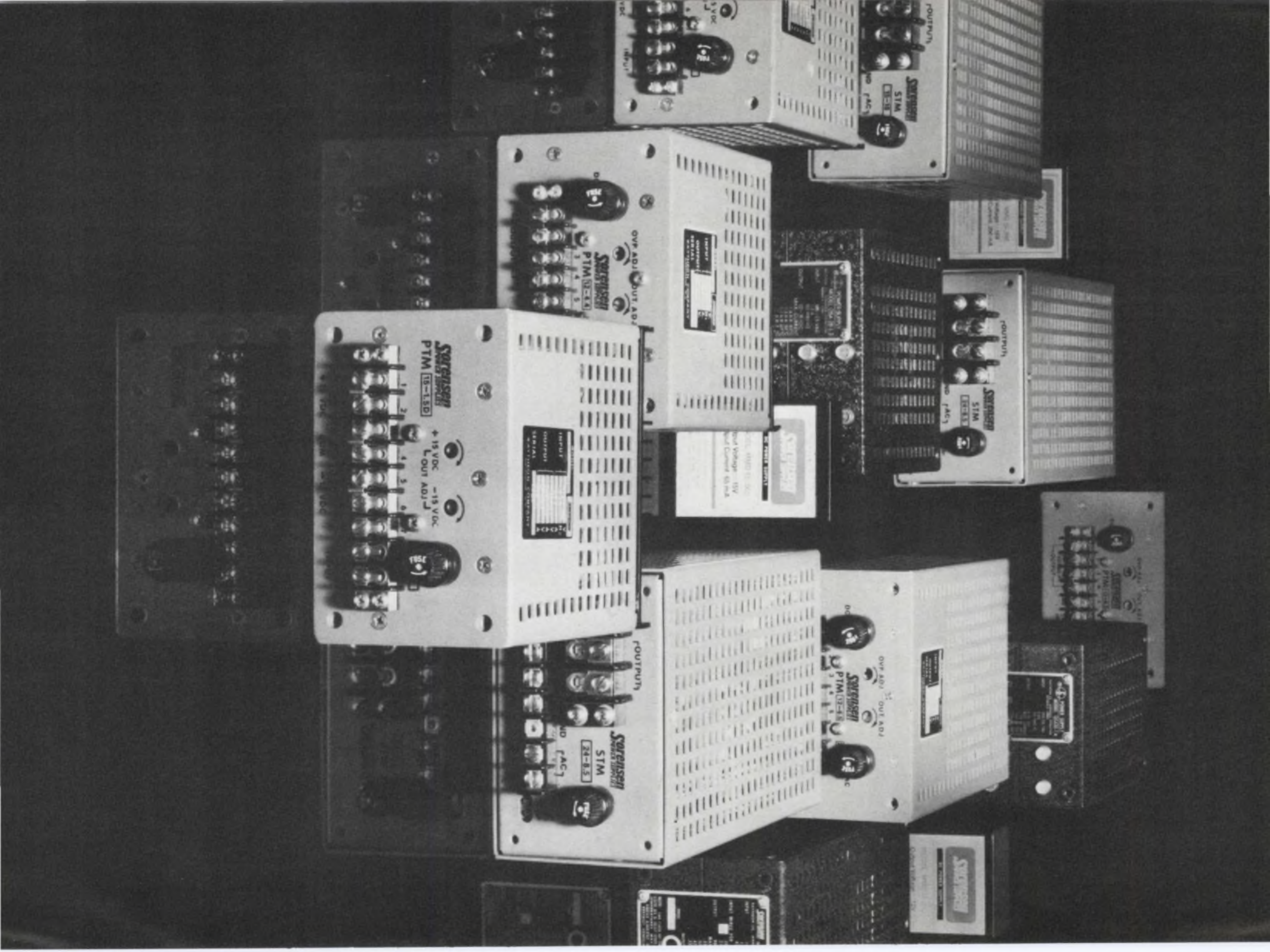

Sorensen
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+15 VDC
-15 VDC
OUT ADJ
STM 24-8.5
OUTPUT
AC

The Sorensen Modulars. A powerful line-up.

Sorensen Modulars give you maximum choice. Plus dependability and efficiency. No matter what your power requirement, count on Sorensen. From the advanced switching-transistor STM series to the miniature encapsulated MMs, there's a Sorensen modular to meet your system specifications and your most rigid performance demands.

Single Output

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PTM Series — 12 models. All solid-state series-pass modulars that achieve state-of-the-art power density; deliver more power per cubic inch than comparable competitive units, at lower cost per watt. Features include built-in overvoltage protection; highest quality components; adjustable automatic current limiting; 0.05% + 5mV voltage regulation; low ripple and noise; six voltage levels to 100 watts.

Dual Output

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Miniature

MM Series — MMS (single) MMD (dual) MMT (triple) — 15 models, 4 package sizes. Designed for maximum reliability in microminiature electronic applications. All MM encapsulated modulars feature built-in overvoltage protection; excellent voltage regulation; single outputs from 5 to 28 Vdc; dual outputs of ±12 or ±15 Vdc.

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SORENSEN CATALOG/73 provides fully detailed specifications for all models of Sorensen modular and lab/systems power supplies. Write for your copy. Sorensen Company, a unit of the Raytheon Company, 676 Island Pond Road, Manchester, N.H. 03103. Tel. (603) 668-4500. Or TWX 710-220-1339.

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across the desk

The manpower crisis: It seems inevitable

In response to the first two letters in your April 1, 1973, issue ("Future for Engineers Seen as Less Than Rosy," ED No. 7, p. 7), I don't think one article, or 20, in a limited-circulation magazine like yours is going to change a three-year enrollment trend away from engineering. Engineers willing to exert an effort to learn—by definition—are seldom obsolete. If you select your job on the basis of a figure of merit equal to the annual return divided by initial learning investment, welfare is the way to go.

I think that the following cycle, seen before, is again appearing:

(a) Job shortage (localized now because engineers won't move to get work).

(b) Bright technician moves up to nondegreed engineer and does the same work for less pay.

(c) Lazy engineers quit learning but get raises with everyone else.

(d) Narrow-minded engineers overspecialize and are overpaid.

(e) Downswing comes along and "c" and "d" above get the ax first and new jobs last.

If you reduce the number of graduates, "b" happens more often. Already 37% of the engineers are nondegreed. If you try to bar nondegreed men, the Government alphabet-soup agencies clobber you.

The problem is a very simple one of supply and demand. Everytime the demand goes up, the increased price tends to expand the supply. And until you get a corner on the market, you're hamstrung. Add to this the fact that engineers are naturally independent and therefore tend to be anti-union, and the result is that anyone attempting to "better the lot" of Mr. Engineer is in for a great deal of frustration and little progress.

To those who are trying to help us, in spite of ourselves: "Gee, thanks fellows, but right now my boss just gave me the most interesting project you ever saw; so I'm busy right now. Let me know if you get anywhere."

Sound familiar?

John M. Mealing Jr.
Engineering Supervisor
General Computer Service, Inc.
444 Executive Center Blvd.
El Paso, Tex. 79902

A clarification on Disco-Vision

In ED No. 3, Feb. 1, 1973, the article on p. 35 ("It's a 40-Billion-Bit ROM, It's a TV Programmer —It's Disco-Vision!") states in the second paragraph that it can record about 40 minutes.

Reading through the article, I get the following:

$$\frac{40{,}000 \text{ grooves}}{1800 \text{ rpm}} = 22 \text{ min.}$$

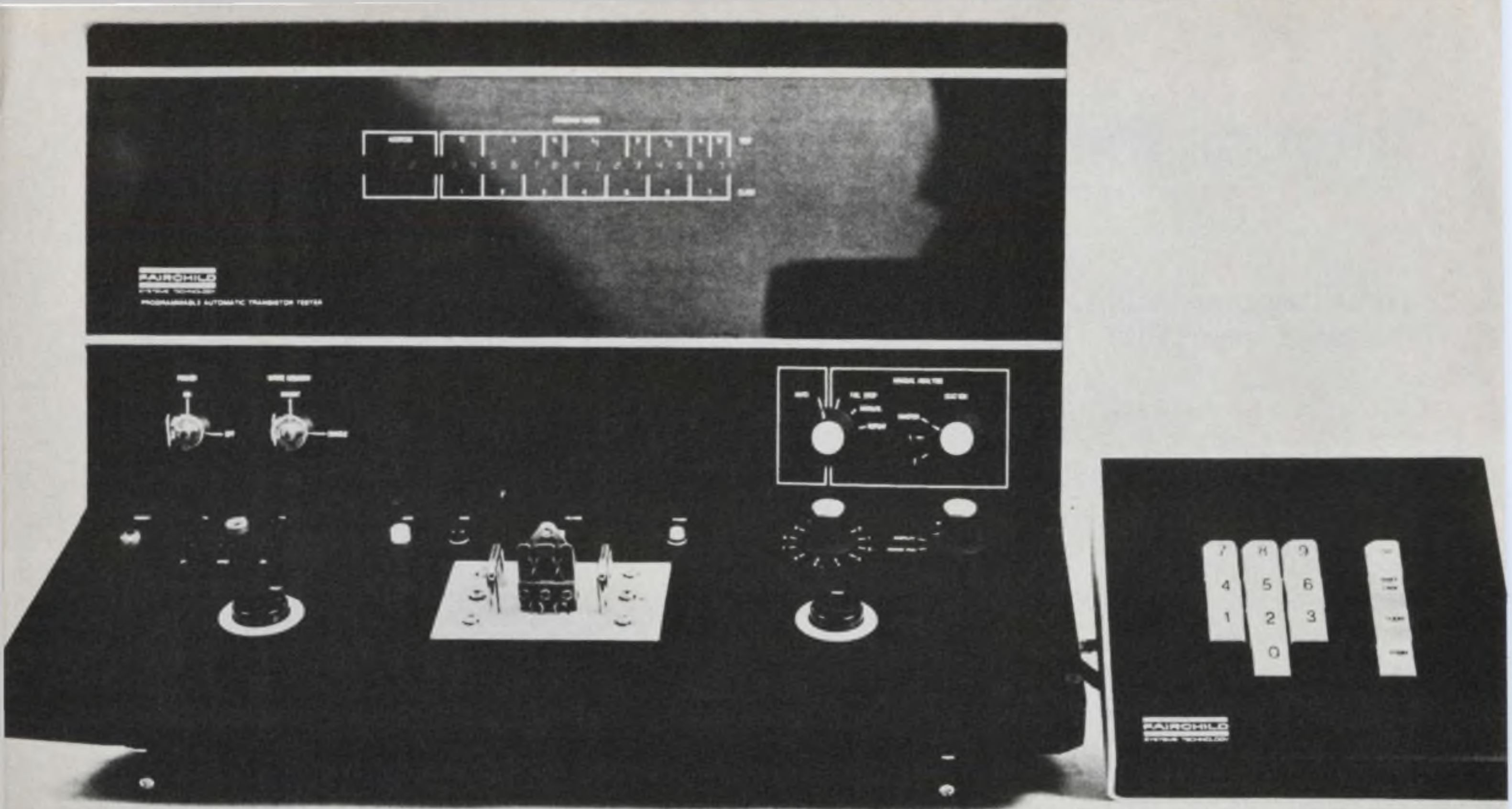
I assumed the 40 minutes was for both sides. But in the Feb. 5 issue of EDN, p. 16, a news write-up on MCA Disco-Vision states that the disc offers 40 minutes of uninterrupted programming (on one side).

Would you please clarify the capability of Disco-Vision?

Anthony J. Nauyokas
Technical Data Supervisor
Cohu, Inc.
Electronics Div.
Box 623
San Diego, Calif. 92112

Ed. Note: Reader Nauyokas is correct. In a 40,000-groove configuration, the disc will hold only 22 minutes of programming. MCA
(continued on page 10)

Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Managing Editor, Electronic Design, 50 Essex St. Rochelle Park, N. J. 07662. Try to keep letters under 200 words. Letters must be signed. Names will be withheld on request.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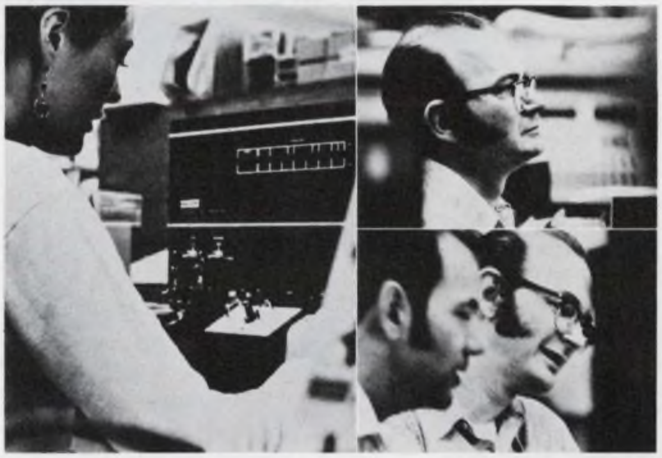
Our sleek, new System 12 Programmable Automatic Test System can offer you the plain, simple, yes or no, pass or fail, answers you need. High speed. Accurate. Reliable. It's a small test system designed to do maximum work while taking up minimum space.

The System 12 will handle incoming inspection, wafer testing, quality control, and die sorting. A 3-station multiplex—each station conducts different tests on different types of polarities at the same time. The solid state MOS memory stores up to 82 tests which can be programmed into Class Plans. Programming is flexible and readily expandable. BV measurements at 600V and currents at 10 amps are standard for power devices.

Among the options for the System 12 are Multiplex option with remote station capabilities, small signal H_{FE}, high throughput, 1KV, SCR parametric expansion, 100 amp DCH_{FE}, 110V or 220V operation, external test capability, memory protect, and digital read-out on the central and remote test stations. The System 12 can be configured to satisfy your requirements today, and expanded as your needs expand...easily and without penalty.

You can order the new System 12 from stock. The price is low. Write for detailed spec sheets, or call collect (415) 493-5011 for demonstrations. Our TWX: 910-373-1204



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ED

Fairchild Systems

Fairchild Systems Technology, a division of Fairchild Camera & Instrument Corporation

ACROSS THE DESK
(continued from page 7)

claims that 40 minutes of programming on one side of the disc will result either from recording two or more frames per groove or from increasing the number of grooves on the disc.

Barking-dog solution prompts a growl

This is in response to the letter suggesting a device to discourage barking dogs—an audio oscillator at 20 kHz, connected to a 10 or 20-W monophonic amplifier that drives a hi-fi tweeter horn (see "How to Outbark a Barking Dog," ED No. 6, March 15, 1973, p. 16C). As an engineer and licensed professional dog handler, I find the solution by that brave soul to the barking dog outright cruelty.

I'm sure if my dogs began to bark unnecessarily that I would propose the following defense: A microphone connected to a saturating amplifier feeding a flip-flop, which drives another speaker. Thus, as long as the dog had his speaker on, he'd get back one-half his medicine.

John W. Fish

MIT/CSDL
68 Albany St.
Cambridge, Mass. 02139.

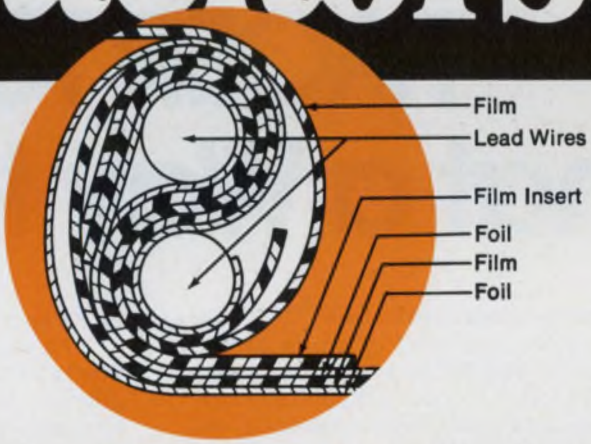
Ed. Note: Yeah, but how do you hang a speaker on your neighbor's dog?

We lose some, we win some

Please throw a dart at the Grumman Grumbler for me ("The Anniversary Issue: A Sampling of Reaction," ED No. 3, Feb. 1, 1973, p. 7). It is precisely this attitude of "I'm not interested in anything that isn't functional" that gives engineers the reputation for being clods, social misfits and despoilers of all that is beautiful in the name of technology. You can replace your loss of his readership with my en-

(continued on page 16)

Newest Idea in film capacitors!



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* Patent No. 3638086
Other Patents Pending

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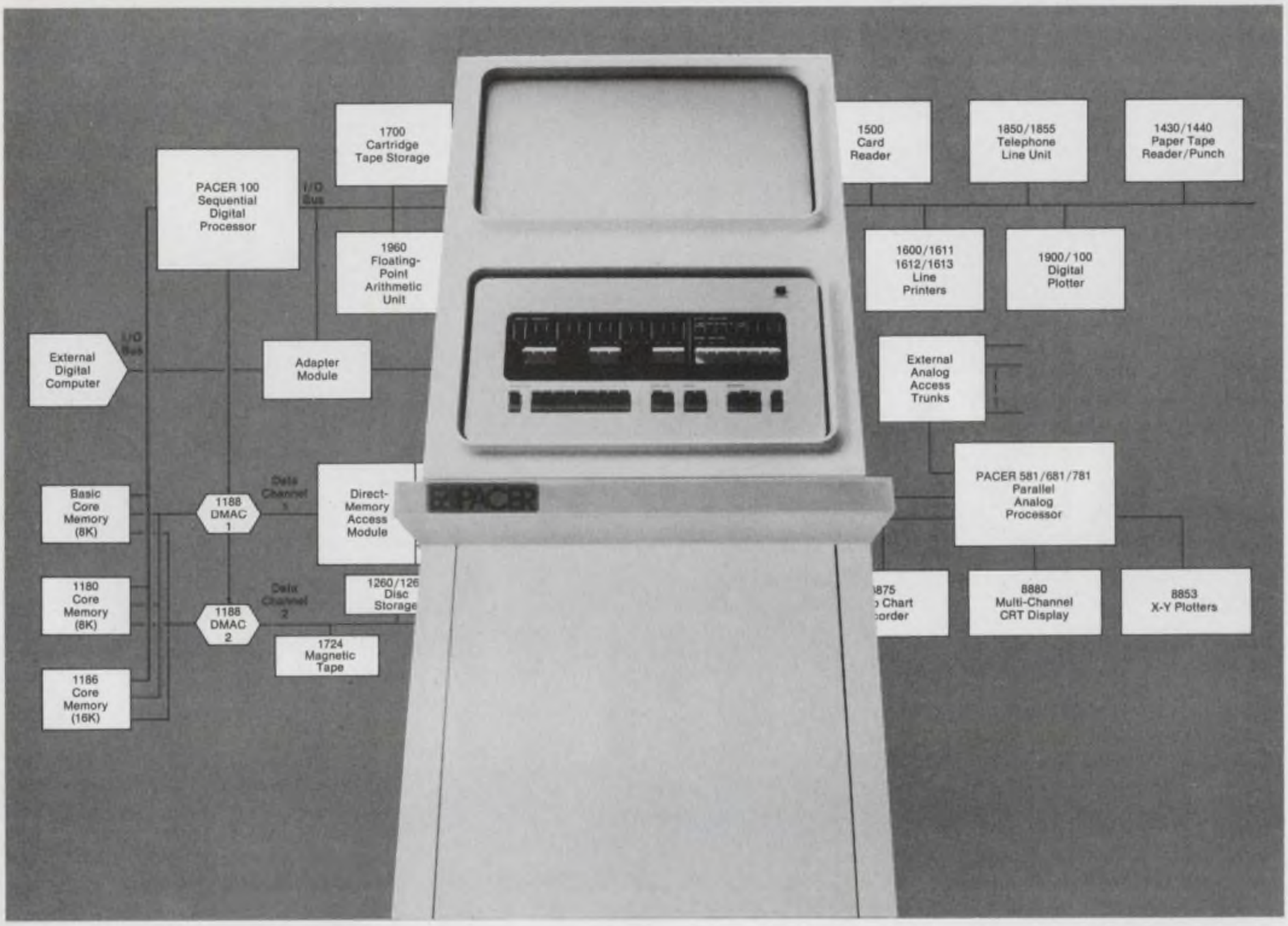

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We put the PACER 100 at the digital corner of three different series of new PACER systems, each larger than the next: PACER 500. PACER 600. PACER 700.

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At each level, your PACER system can deliver far more scientific and engineering design-problem solutions—per day or per dollar—than any other system available.

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Further, we have a huge library of software to help you—including a foreground/background Real-Time Operating System. And we have more than 5,000 case histories of applications to prove our software expertise.

As you can see, we make no ordinary claims. Now, thanks in part to our new digital, we can make one more dramatic assertion: PACER systems can offer you performance/price ratios that run to over 100 times those of conventional digital systems.

That's the sort of efficiency that's worth writing home about or, more to the point, worth writing to us. The faster you do, the sooner we can send you more information to help you start a new growth story of your own.

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INFORMATION RETRIEVAL NUMBER 10

INFORMATION RETRIEVAL NUMBER 11 ►

Licon has added LED's to one LPB switch line . . .
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You always get a great choice with Licon® LPB switches. For example, take just two of our many lines—Types 01-700 and 01-600 single light switches. Our 01-700 line is now available with integral Light Emitting Diodes. That means virtually infinite light life and negligible operating current. And the 01-700's low profile design assures maximum light intensity. Or choose neon or incandescent lamps instead. In either line. Mounting styles? Type 01-600 line features bezel or bezel-barrier, in a single switch or multiple in matrix. Time-saving, snap-in mounting. Switching action? Choose from momentary or alternate—plus a selection of non-lighted switches or non-switching indicator lights in matching styles. But whatever you choose, you also get patented double-break Butterfly switching which offers greater reliability and other advantages not possible with single-break switches. Licon LPB's are easily installed and serviced.
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INFORMATION RETRIEVAL NUMBER 13

ACROSS THE DESK
(continued from page 10)

closed application.

G.J. Colter, Manager
Circuit Design Engineering
Honeywell Information Systems
P.O. Box 6000
Phoenix, Ariz. 85005.

Wrong wine

Our man Harry, covering the Components Show in Paris, almost didn't get back. At one of the great French restaurants, he ordered California wine. After the ensuing explosion, he whimpered, "I was always told the imported was best."

Job survey defended as 'creditable job'

I think the criticism expressed by Dr. T. Reginald Garfield and Mark Smith in your letters columns of April 1 were not entirely fair to author Richard Turmail (see "Future for Engineers Seen as Less Than Rosy," ED No. 7, p. 7).

Dr. Garfield charged that Mr. Turmail's sources had no interest in the economic or social status of the working engineer. If the data obtained by the College Placement Council and the Engineers Joint Council are biased today, when they report an increased demand for engineers, were they equally biased two or three years ago when the college council reported the decline in campus recruiting and the engineers' council urged the Government to curtail immigration because of the reduced demand for engineers in the U.S.? It is easy to dismiss the facts by charging, without proof, that other people have ulterior motives. Your readers will find no such approach in any of the reports published by either the College Placement Council or the Engineers Joint Council.

Mr. Smith feels that the actual unemployment rate is not a valid criterion for judging the comparative severity of engineering unemployment. Actually the rate for en-

(continued on page 23)

The IR/Schottky Power Curve. A new twist that cuts power loss 50%.

Schottky had a good idea. His hot-carrier principle brought unique advantages to users of signal level diodes. So we teamed up to bring the same advantages to the high power league: designers of I/C power supplies and switching regulators in the 50 Amp/20 Volt range. Now it's a whole new ball game.

Check our curve. The dotted line shows the voltage-current characteristics of junction rectifiers. The solid line is the basis for our new pitch. There's quite a difference.

Half The Forward Voltage Drop. Note the forward voltage drop of 0.65 Volt vs. 1.25 Volts for typical rectifiers. At low voltage-low frequency, it means 50% less power loss, for a marked increase in efficiency. Like 10% at 5 Volts/100 Amps. Now you can use fewer rectifiers, smaller transformers, and cut heat-sinks in half. If you design high-frequency circuits, you'll do even better.

More Efficient at High Frequencies. The higher the operating frequency, the greater advantage the Schottky has over junction rectifiers. For example, at 20 KHz, the IR/Schottky gives you 25% more system efficiency. And you can operate at even higher frequencies.

No Reverse Recovery Losses. Unlike junction rectifiers, the IR/Schottky barrier doesn't store minority carrier charges. There are none to be swept out as it is switched to the reverse mode. So time-lag and electrical loss are virtually zero, which accounts for its increased efficiency in high and ultra-high frequency systems.

Reliability/Stability. You can forget about conservative derating. IR proprietary passivation and metallization technology assure long-term stability, extremely low leakage and low sensitivity to temperature. You can count on reliability and optimum life at full ratings.

Try our new curve. Call your IR sales office or distributor today and ask for details on IR/Schottky Power Rectifiers — in either forward or reverse polarities. You'll get everything you need for a whole new ball game.

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WHEN IT COMES TO MATCHING UP CONNECTORS AND CABLE...

IT TAKES TWO TO TANGLE

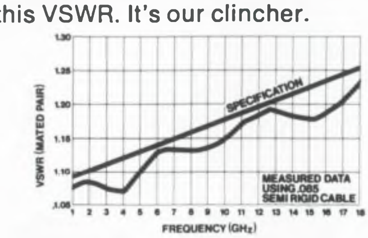
A fact not to forget is that those 3mm SMA connectors you may be specifying were designed for .141 inch cable. Use them with .085 inch diameter and the losses you suffer through a mismatch of connector geometry with cable geometry can be a problem.

In short, it takes two to tangle a signal transmission; the right connector and the wrong cable or the other way around.

That's where Simplicon comes in. They're a remarkable new series of coaxial connectors designed specifically for perfect line match with .085 inch diameter cable, semi-rigid or braided. And, slimmed-down Simplicon connectors will give you the performance equivalent to SMA types without conforming to totally irrelevant requirements that don't make sense in most applications.

If you're faced with the headaches that smaller, higher density packaging can bring, simply specify Simplicon. They're not only made for .085 inch cable but they're small enough to fit where you've never been able to fit a connector before.

Before we ask you to write for our catalog with all the details, check this VSWR. It's our clincher.



Now, will you write for that catalog? Cablewave Systems Inc., 60 Dodge Avenue, North Haven, Connecticut 06473, 203 239-3311.

Cablewave Systems Inc.

A Corporation Owned By Phelps Dodge And Kabelmetal

INFORMATION RETRIEVAL NUMBER 202

Connector or IC panel– we can give you exactly what you need.

Single-, double- or multilayer. Mother/daughter board connectors, IC receptacle packaging, feedthrough posts, low-profile DIP headers, or cable-to-board connectors. Prewired or ready to wire by automatic techniques.

Panels with high reliability, competitive cost and ease of repairability.

We built our reputation for quality and low applied cost in the connector field. And carried it over into back panels—the very heart of modern electronic systems. To give you the kinds of connectors, manufacturing techniques and equipment which ensure reliability, performance and repairability—at a competitive cost.

High reliability.

We eliminate plated through-hole distortion and possible damage caused by force fit insertion. This is done by selectively pre-depositing bands of solder on posts and receptacles before inserting and reflow-soldering them into panels. This process also greatly increases the reliability and performance of our panels by eliminating wicking, bridging, peaks, icicles and board delamination.

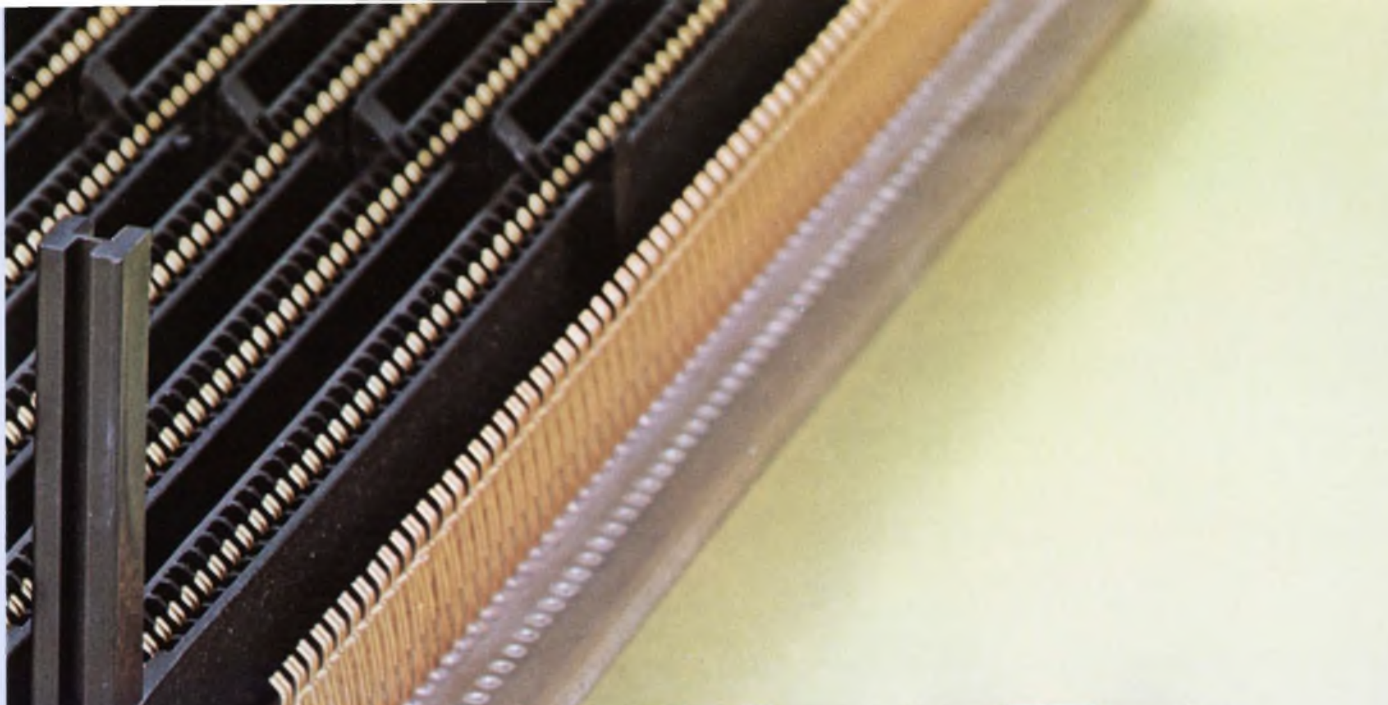
Fillets are more uniform and complete, with full solder top to bottom. And posts are left clean and solder-free for automatic wiring. AMP has also developed connector housings which snap on over the contacts *after* contacts are flow soldered, so there's better use of printed circuit real estate. For information on our panels circle Reader Service Number 150.

Ease of repair.

When snap-on connector housings are used, individual contacts can be exposed for quick, easy removal and replacement, without the need to desolder *all* contacts.

Competitive cost.

There are several important ways in which we keep the cost of our panels competitive. First, by inserting contact posts with high-speed, automated machines. Second, by soldering *all* contacts simultaneously instead of individually. And third, by conducting rigorous electrical and mechanical quality checks on *every single panel* we make, eliminating the cost and burden of incoming inspection for our customers. Additional economies can be achieved by using snap-on housings which do not require time-consuming individual contact loading.



Presoldered contact is inserted into plated panel through-hole.

Solder band is pulled into through-hole with just enough force to retain it during reflow.

Contact is flow soldered in place, producing uniform fillet with full solder, top to bottom, and clean, solder-free posts.

We can design with you or for you.

If you customarily design your own panels, we can assist in optimizing your circuit patterns. Or, we can take your parameters and complete the entire panel-making operation, sparing you considerable investment. Using computer-driven plotters, we "pack" the greatest number of circuit paths into the smallest possible board space, consistent with other design parameters.

We'll set you up to wire or do your wiring for you.

Give us your parameters. We'll give you assembled connector or IC panels, pre-wired or ready for your automatic wiring. If you choose the TERMI-POINT clip system, you'll get highly-reliable, spring-action terminations that are easier to test, maintain and service.

Panel construction is AMP-engineered and manufactured.

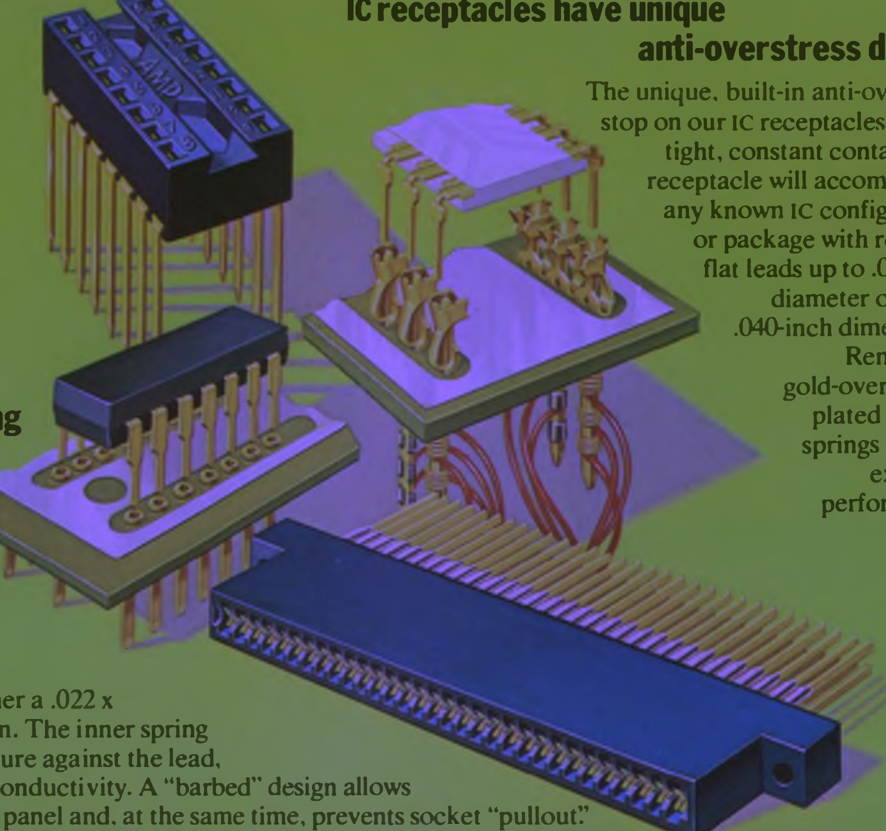
One main reason we can control the quality and cost of our panels so well is the fact that we design, engineer and manufacture literally everything that goes into them.

DIP headers are ideal for low-cost, high-density packaging.

Our low-profile DIP headers provide some of the industry's lowest-cost, highest-density packaging for 14- and 16-lead IC's. Standard headers accept a full range of lead sizes—round, rectangular or both, and are compatible with high-speed, automated wiring methods. Low-profile headers (.150-inch high) accept rectangular leads up to .015 x .030-inch.

IC receptacles have unique anti-overstress design.

The unique, built-in anti-overstress stop on our IC receptacles assures tight, constant contact. The receptacle will accommodate any known IC configuration or package with round or flat leads up to .022-inch diameter or .022 x .040-inch dimensions. Removable gold-over-nickel-plated contact springs provide excellent performance.



Low-profile miniature spring socket offers maximum retention and conductivity.

Designed specifically for electronic and wiring applications that require low profile miniature sockets, this product has an inner spring member and a body with either a .022 x .036-inch or $.025^2$ post configuration. The inner spring member maintains consistent pressure against the lead, providing excellent retention and conductivity. A "barbed" design allows the socket to be self-retained in the panel and, at the same time, prevents socket "pullout."

Posted card connectors offer great versatility in panel design.

Our TERMI-TWIST Connectors are available in a variety of configurations, depending on your requirements for post size, number of positions and center-line spacing. Board area contacts are bifurcated for redundancy. Connectors can all be wired by high-speed, automatic techniques.

Engineering backup...worldwide.

At AMP, nearly 900 application, service and sales engineers are prepared to assist you with every phase of panel-making, connectors and programming systems. At your domestic manufacturing plant, or wherever you use AMP products and machines throughout the world. You'll find AMP manufacturing and service facilities in most major international markets. In the United States, district offices are located in California, Georgia, Illinois, Massachusetts, Michigan, Minnesota, New Jersey, Ohio, Pennsylvania, Texas, and the District of Columbia.

Write for Panel Packaging Folder

Find out how we're able to give you exactly the panel you need. Write on your company letterhead for our Panel Packaging Folder. It contains full documentation of our various processes, with suggestions of how they can work best for you. AMP Industrial Division, Harrisburg, Pa. 17105.

AMP
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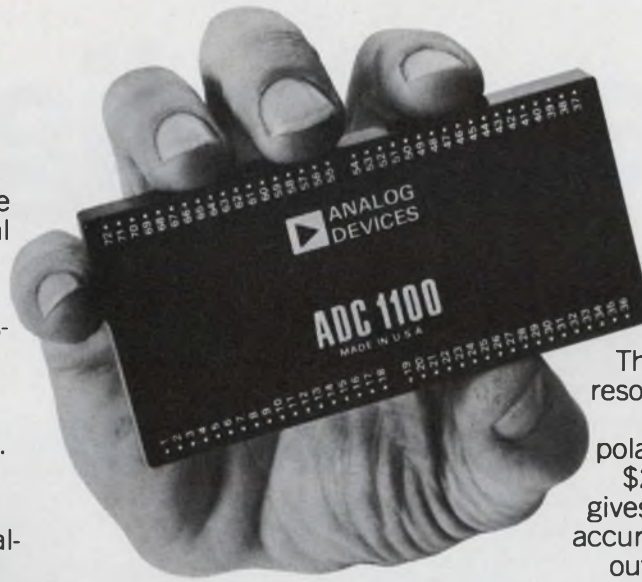
And here's another of our low-cost solutions to your conversion problems.



This 5-volt A/D converter gives you dual-slope noise immunity and BCD-plus-sign output for only $67/100's. The ADC1100.

If you're converting for a remote display, or if you've got a special display requirement, this converter was made for you.

Maybe you're timesharing a display with several data sources. Or rescaling the converter output to display pounds, gallons, rpm, or other engineering units. Or using a special display you designed yourself.

Then meet the ADC1100. A dual-slope converter with a 3½-digit BCD-plus-sign output and automatic zero correction. It'll give you normal mode rejection of 40dB (up to 120dB with a phase lock loop circuit). Plus 5VDC operation and guaranteed monotonicity. And the ADC1100 is equally well suited for feeding a computer.

That's an awful lot for only $67 in 100's. ($99 in singles.)

But after all, we're the people who wrote the book on converters. So you expect a lot from us.

And here's what else you can expect.

Two high-resolution, high-accuracy, A/D converters that can save you time and money. Both with parallel and serial outputs, both with user-selected input ranges. The ADC10Z has 10-bit resolution and accuracy 20 μsec (max) conversion time, for $67 in 100's. The ADC12QZ converts in 40 μsec (max), gives you 12-bit resolution and accuracy—$92 in 100's.

Two low-cost general-purpose D/A converters. The DAC10Z provides 10-bit resolution and accuracy, built-in IC output amplifier, unipolar or bipolar outputs—only $27 in 100's. The DAC12QZ gives you 12-bit resolution and accuracy and five user-selected output ranges for only $47 in 100's.

A low-cost sample and hold amplifier. For $32 in 100's, the SHA 5 will hold your attention, too. The perfect companion to our low-cost converters.

For more information on what you can expect from us, give us a call. We can send you samples, comprehensive data sheets, and, for only $3.95, a 400-page handbook on A-D conversion.

Analog Devices, Inc., Norwood, Mass. 02062

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INFORMATION RETRIEVAL NUMBER 15

Dialight sees a need:

(**Need:** The right switch for the right price.)

See Dialight.

For the switch buyer, choice of function and esthetics, reliability, ease of mounting, and low cost are his prime concerns. He may need a pushbutton switch for panel, sub-panel or snap-in mounting. He may need a choice of bezels with or without barriers in black, gray, dark gray or white. He may need a legend that's positive, negative, or hidden until energized . . . one that's white when "off" and red, green, amber, blue or light yellow when "on" . . . or colored both "on" and "off." He may need a highly reliable switch proven in thousands of installations . . . available in momentary or alternate action . . . N.O., N.C. or two circuit (one N.O., one N.C.) or for low level, low voltage and current applications . . . that accommodates a T-1¾ bulb with midget flanged base, incandescent, in voltages from 6 to 28 V. Matching indicators with same front-of-panel appearance are also available. These are some custom needs he may face, and these switches are some off-the-shelf answers from Dialight.

ACROSS THE DESK
(continued from page 15)

gineers was about 3% during the peak of unemployment in mid-1971. It is now about 1%. The fact that engineering unemployment stayed so much lower than the over-all national average demonstrates very tangibly one of the advantages engineers have obtained in return for their substantial investment in education. Does Mr. Smith think that any engineer would have been better off if he had not obtained an engineering degree, or that the average semiskilled or unskilled worker earns anything approaching the average engineer's salary?

Mr. Turmail did a creditable job of seeking and reporting factual information about the job market.

John D. Alden
Executive Secretary

Engineering Manpower
Commission
Engineers Joint Council
345 East 47th St.
New York, N.Y. 10017

'Cell' engineering viewed as inhibiting

It should be instructive to watch the long-term performance of Autonetics' products, such as the SRAM computer, Micron and Minisins. We may then be able to evaluate the sweaty "cell" approach to engineering of Mort D. Margolis (see "Try Getting It All Together," ED No. 7, April 1, 1973, pp. 58-60), as contrasted with the procedures of other companies in our field. I predict that although the Margolis formula of forced adaptation may squeeze a few extra dollars out of his employees at first, his operation will soon consist of a layer of yes men and a collection of frightened engineers making the quietest technical choices, no matter what their ultimate impact on the success or failure of the product. I doubt that either Rockwell or the taxpayer can really afford the cell approach.

Scott Pearson

8 Lafayette St.
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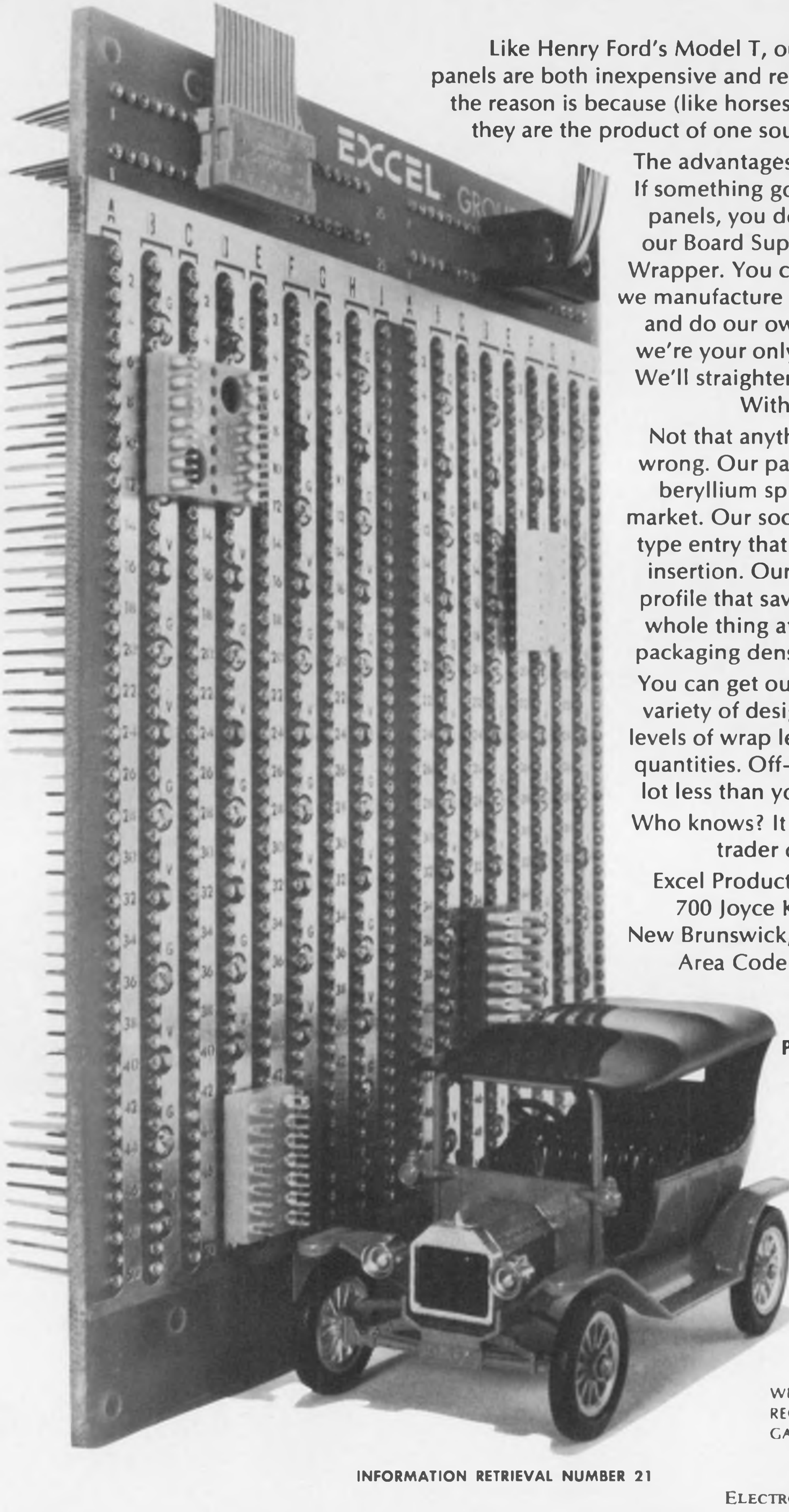
How we harnessed Henry Ford's horse sense to pluggable panels.



Like Henry Ford's Model T, our pluggable panels are both inexpensive and reliable. And part of the reason is because (like horses and Model T's), they are the product of one source of supply.

The advantages are fairly obvious. If something goes wrong with our panels, you don't have to go to our Board Supplier. Or our Wire Wrapper. You come to us. Because we manufacture our own boards and do our own wire wrapping, we're your only source of supply. We'll straighten out the problem. With no fuss.

Not that anything's likely to go wrong. Our panels have the best beryllium spring clips on the market. Our sockets have a funnel-type entry that makes for easy IC insertion. Our pins have a low-profile that saves space. And the whole thing affords the highest packaging density ever achieved.

You can get our panels in a wide variety of designs with 1, 2, or 3 levels of wrap length. In unlimited quantities. Off-the-shelf. All for a lot less than you're paying now.

Who knows? It may make a horse trader of you yet.

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INFORMATION RETRIEVAL NUMBER 23

TV industry views discs as 'breakthrough of '70s'

The video disc—not tape—will be the "breakthrough of the '70s" in television, the Society for Information Display was told at its recent International Symposium and Exhibition in New York City.

"The TV industry is going to change more radically in the next five years than most people realize," said Joseph Markin, manager of display systems for the Zenith Radio Corp., Chicago, and moderator of a panel session on "Whither Television."

"Video recording — particularly video discs—has opened up important new possibilities, primarily because of its low cost. Also, instead of being limited to four, five or seven minutes of color TV playback, the possibility now exists of getting up to 25, 35 or perhaps even 40 minutes of recorded time," Markin went on.

"This ability to increase the amount of information on a disc by one or two orders of magnitude over that of the so-called microgroove record is a real technological breakthrough of the '70s."

Furthermore, Markin noted, since the discs will be embossed or stamped, they can be manufactured at prices now paid for audio records.

C. Bailey Neal, manager of advanced development at Sylvania Entertainment Systems, Batavia, N.Y., a panelist in the same session—agreed that "video disc systems are coming on the line." But he said that the competition among different types of disc systems would—at least for a time—slow the customer acceptance.

Also, he pointed out, the supply of recorded material must be plentiful before the consumer will buy playback equipment.

Other developments foreseen by panelists at the show, which was held May 15-17 in the Statler-Hilton Hotel, included these:

- Bigger and better displays, both for television sets and computers, will result from growth of large-scale semiconductor technology.
- Decreases in the cost of ICs, giving more functions per dollar, will provide an effective weapon for U.S. manufacturers to combat offshore electronics suppliers.

As for "thin panel" screens for color TVs, Zenith's Markin said that "because integrated circuitry is available and prices are decreasing, I look for a display that will be compatible with IC circuitry."

As an example, he pointed to the plasma, or gas-discharge, panel. "Despite some differences in voltage," he explained, "these panels are nevertheless compatible with ICs."

Displays of this type can be made much larger, Markin pointed out. "Now," he said, "you can begin to think of screens that have the same aspect ratio as that of the wide screens, such as Cinerama."

Plasma displays will be highly competitive with CRTs in certain computer terminal applications, according to Dr. D. R. Haring, vice president of Computek, Cambridge, Mass., and a panelist at a session on "The Impact of New Technology on Display System Architecture."

"Plasma displays for alphanumerics, except for the cost, are now here," he said. "But they are still too expensive when compared with CRTs."

Ulf beacon pinpoints site of trapped miners

A new emergency beacon for miners can tell rescuers on the surface the exact location of the men trapped underground.

Developed by Westinghouse Electric's Georesearch Laboratory in Boulder, Colo., under a contract from the Bureau of Mines in Pittsburg, the device uses an ultra-low-frequency radio transmitter that operates off the battery in the miner's lamp cap.

In an emergency, the miner unreels a metal tape stored in his belt to form a loop that has a circumference of 80 feet. He attaches the loop ends to two terminals in his transmitter and transmits a simple electromagnetic signal to the surface. A man on the surface with a portable receiver and 12-inch loop—or someone in a helicopter trailing a loop—picks up the signal and moves toward it until there is a null, indicating he is directly over the center of the loop in the mine.

The Bureau of Mines has tested the prototype from a depth of 1000 feet and believes it will be effective at depths of 2000 feet.

A stationary beacon in the mine could be more sophisticated. A receiver would allow men underground to hear speech transmitted from the surface and permit them to have a transmitter to send back pulses corresponding to "yes," "no" and "don't know." Rescuers could ask questions to determine the number of men at the beacon, their condition and other information.

A battery for the stationary beacon would be constantly charged from the mine's power circuit, and the antenna would be looped around a coal pillar. Bureau of Mines engineers are also considering the possibility of integrating the stationary beacons with the mine's telephone system.

The bureau estimates that the portable beacons would cost about $65 for each miner and the portable surface receivers about $250 each. The stationary beacons would cost about $2000 apiece.

The new system is expected to be more practical than two earlier ones the bureau tested. In one a mine radio system used low-frequency radio waves but was designed primarily for communication rather than position-finding. In the other a seismic system for locating trapped miners (see "Vlf Systems and Geophones Help Rescue Trapped Miners," ED 4, Feb. 18, 1971, p. 30.) required too many geophones on the surface that had to feed their signals into a computer to be understood.

Proposals from a number of companies to build the ulf system are in hand, a Bureau of Mines spokesman says, and a selection will be made before July.

Printers with CRTs speed data handling

By combining a cathode-ray-tube display with a printer, manufacturers are making it easier for computer users to prepare and correct data and to increase transmission speed.

Two companies—American Telephone and Telegraph of New York City and Computer Optics, Inc., of Bethel, Conn.—have each introduced a CRT/printer system.

The AT&T entry, known as Dataspeed 40, contains a CRT display that can show a maximum of 24 lines, each of 80 characters.

AT&T's new data terminal features a combination high-speed printer and cathode-ray-tube display.

Data on the screen can be converted to hard copy with a high-speed belt printer in 4.5 to 6.5 seconds.

Unlike the AT&T device, which has one printer for each CRT display, the system from Computer Optics can share a printer among several CRT displays. Called the CO:77, the system is designed as a plug-to-plug, key-to-key replacement for the IBM 3270. According to Larry Mitchell, vice president of marketing for Computer Optics, the CO:77 is 20 to 30% cheaper on a rental basis and 50% cheaper to buy than the IBM 3270. The reason, he says, is that all the electronics for the displays are in a central control unit.

Roger Fournier, Computer Optics' sales manager, asserts that there is a trend away from hard-copy output. Because of this, he explains, fewer printers per display unit are needed. As many as eight CRT displays can share the same printer, he says, thereby holding down costs and still making hard copy available.

The CO:77 uses an electrostatic printer and, like the AT&T device, it can tranfer a screen full of information in about six seconds.

Unlike the Dataspeed 40, the CO:77 can be used in a polled system—where the computer checks to see if information is ready to be sent before taking it.

When questioned about this, a spokesman for AT&T said that it had plans to introduce a polled version later.

Nickel-cadmium battery takes fast, fast charge

A nickel-cadmium battery has been developed that can be recharged in as little as 15 minutes without damaging the battery or shortening its life—risks now run when trying to shorten the normal four-to-five-hour recharge time of conventional nickel-cadmium batteries.

Called Powerup-15, the fast-charge battery was developed by General Electric's Battery Products Section in Gainesville, Fla. The key to its capability, according to the section manager, D. L. Barney, lies in the design of special cells: They are built to eliminate the need for expensive cell grading and matching—normally needed for fast charge—and they permit the use of a charger with a relatively simple control circuit.

To prevent damaging the battery while it is being charged so quickly—damage that could result from overheating or excessive voltage—a new sensing cutoff automatically terminates the fast-charge current when either the battery voltage or cell temperature reaches a predetermined point.

If the battery is left on "charge" more than 15 minutes, a lower "topping" current continues to flow into the battery without causing cell damage or loss of performance, Barney says. He adds: "The battery can be left on charge for months without causing cell damage or loss of performance." The temperature sensor is either a thermistor or a thermostat buried in the battery pack.

Powerup-15 batteries are designed for use in garden tools, photographic and hobby equipment, small appliances and communications equipment. Batteries are available in ratings from 100 mAh to 3.5 Ah in all the standard GE sealed, cylindrical cell sizes.

PMOS memories turn up in phones

The first application of semiconductor memories to telephones will appear in an automatic number-dialing telephone from Bell Telephone. Known as the Touch-A-Matic, the new phone uses a low-threshold, PMOS shift-register memory.

Developed by Bell Laboratory engineers at Indianapolis and Allentown, Pa., the telephone can store and automatically dial 32 telephone numbers of as many as 15 digits apiece. Each number is stored in a 60-bit shift register.

According to Glen Chaney, supervisor of Bell's digital MOS circuits group at Allentown, the memory requires no decoding. The reason, he notes, is that the telephone user does the decoding by selecting the number to be called. Selection is done by pushing one of 32 selector buttons.

The memory used in the telephone, Chaney says, is a hybrid integrated circuit. Each chip in the hybrid assembly contains four 60-bit shift registers.

The numbers in memory can be changed by the user. He simply pushes a record button and then one of the 32 location buttons. The number to be stored is then entered on a Touch-Tone pad.

Since the memory is volatile, nickel-cadmium batteries are incorporated into the telephone as a source of standby power. If commercial power fails or if the set is disconnected, the batteries prevent the stored numbers from being lost for 24 hours.

From the land of "click, click, click" comes "whirrr."

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Our Cassette Transport has no pinch roller, capstan or servo system to clean, maintain or cause problems. We've shifted the burden of tape speed regulation from mechanics to electronics . . . and you get added reliability at a lot less cost.

A unique electronic ratio detection technique, on a single MOS chip, allows accurate reading and writing regardless of tape speed. Single track, full-width recording, with reading from only the inner 80% of the tape and read after write-checking, minimizes errors due to dirt, tape wear and tape skew, and assures cassette interchangeability from one drive to another.

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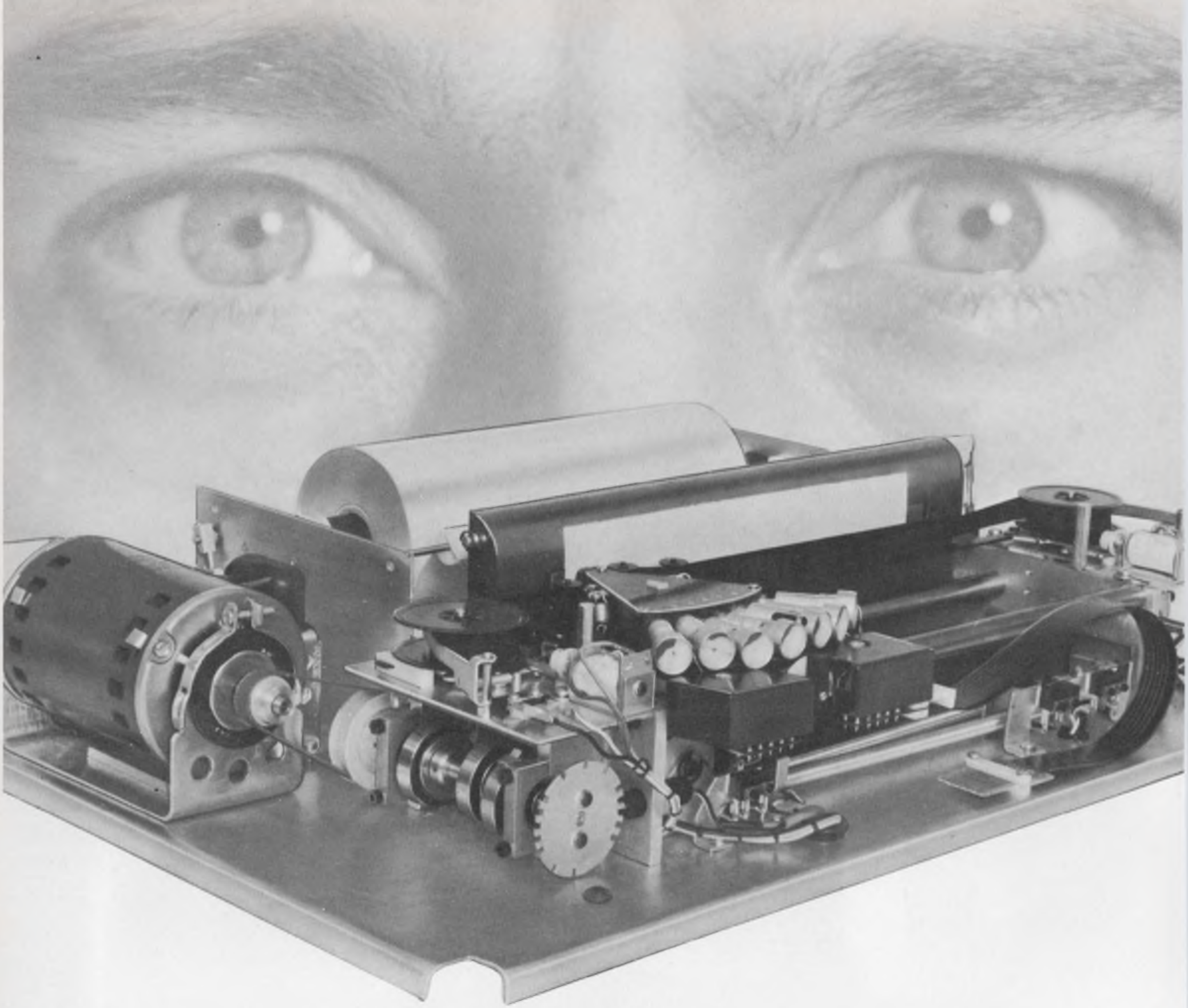

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If there were, our new 30 cps asynchronous printer mechanism wouldn't cost up to 50% less than competitive units or have an MTBF of over 500 *printing* hours. But it does . . . and still gives you the paper handling capability, excellent print quality and low noise level that you want.

For an even closer look, call, write or circle the reader service number for our complete catalog. International Teleprinter Division, The Singer Co. 493 Washington Avenue, Carlstadt, New Jersey 07072 (201) 438-1770 TWX 710-989-0111

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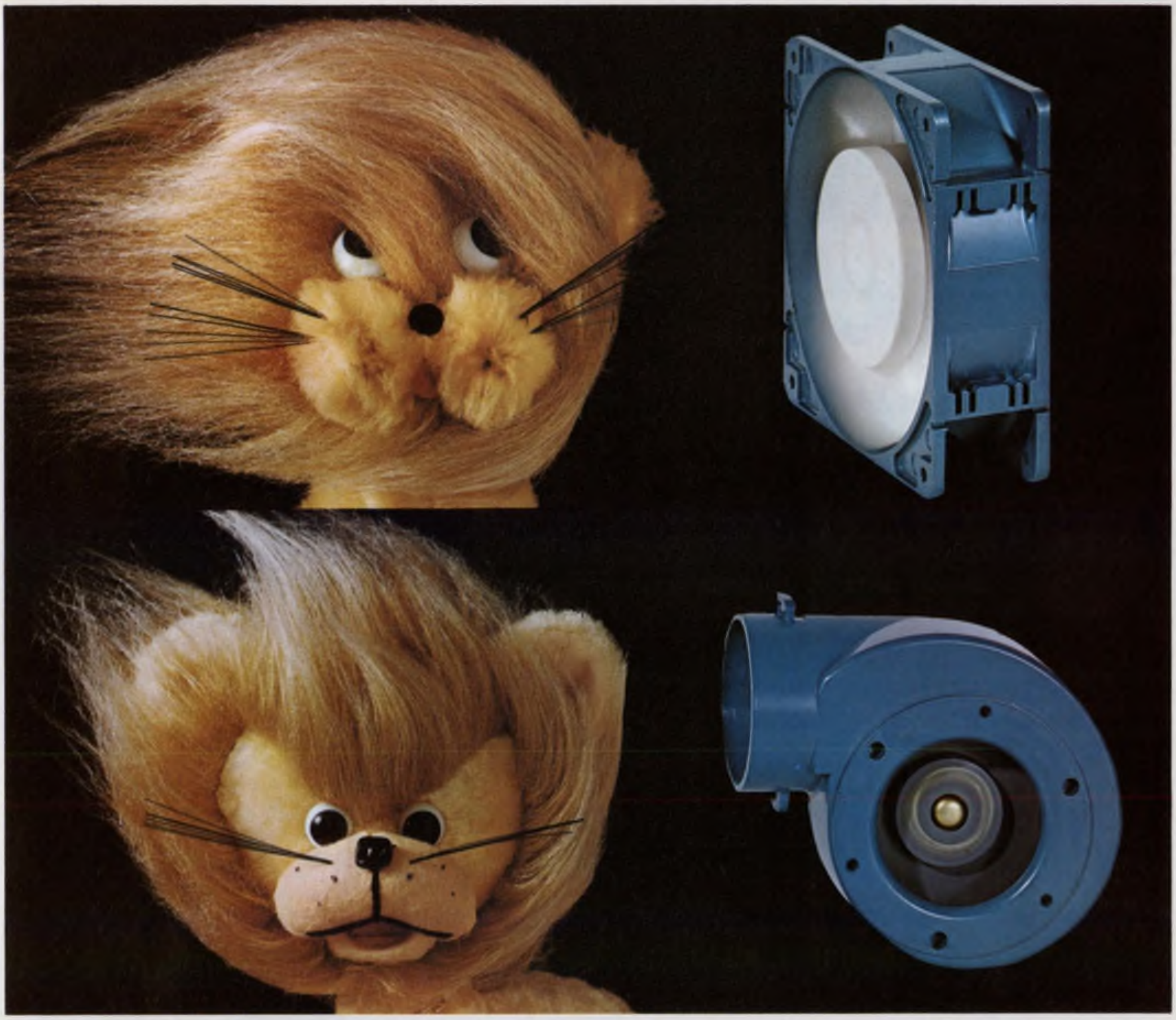

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INFORMATION RETRIEVAL NUMBER 28

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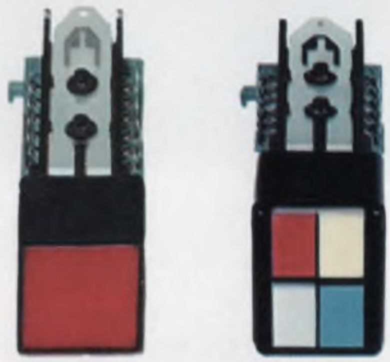

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Colors? Your choice of any one of the following for single-legend switches (or any combination for split-legend switches): lunar white, white, red, green, amber, yellow, orange, blue.

Get the complete details. Write for our Series 300 brochure.

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† Split-legend, four-lamp, normal latch, 2P2T, glass alkyd insulation, no engraving, less lamps. OEM quantities.

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INFORMATION RETRIEVAL NUMBER 29

technology abroad

N-channel, enhancement-mode MOS transistors with an inversion-layer mobility of 770 cm²/Vs and a threshold voltage of 0.8 V have been made by shallow diffusion of germanium into silicon. The operation was performed in a vacuum and also in an open-tube furnace by a team of Israeli scientists. The diffusion, followed by dry oxidation, gave a voltage/capacitance curve shift of about 1 V for a 1000 Å oxide layer. The shift was caused by negative charges in the oxide. Improved control of threshold voltage is obtained with these devices. Poor control has been one of the main disadvantages of n-channel devices, which are potentially much faster than p-channel.

CHECK NO. 441

Investigation of the piezoresistance effect in p and n-channel MOS devices used as Rayleigh surfacewave transducers has been undertaken by Thomson-CSF in France. The sensitivity and dynamic response of the silicon enhancement-mode MOS devices, which have a potential for signal processing of surface waves, have been studied. The n-channel devices, the French researchers say, are better than the p-channel because they have higher response with respect to gauge factor and higher mobility. Both of these factors reduce the dc power required for a given insertion loss. The n-channel device has a gate-control voltage of about 5 V.

CHECK NO. 442

A new technique for growing closely controlled thin films of materials, such as gallium arsenide and other III-V semiconductor compounds, has been developed at Mullard Research Laboratories in England. Epitaxial films of these materials have been grown in an ultra-high-vacuum environment by deposition of the materials from effusion cells onto heated substrates. Use of the modulated molecular-beam technique is required to measure and to provide the requisite precise control of the evaporation rates of gallium and arsenic equilibrium and free-evaporation conditions.

CHECK NO. 443

A low-cost doppler radar module using distributed thin-film microwave circuits has been designed for intruder-warning systems. The system, developed at Mullard Research Laboratories in Surrey, England, contains a Gunn oscillator, a Schottky detector and a circulator that separates the transmitted and received signals and provides local oscillator power at the detector. All of the thin-film circuit elements are incorporated on a 1-cm-square ferrite substrate, together with low-pass filter networks for the dc supply. The Gunn oscillator is varactor-tuned, and the circuit is stabilized by coupling of a resonant line to the oscillator. The output power is 5 to 7 mW. With an antenna of 20 dB gain, the detection range is 20 to 30 m.

CHECK NO. 444

K-187

Dr. Samuel Fok
Siliconix Incorporated
Santa Clara, California

The STEREOSCAN 600 scanning electron microscope plays an important role in process development and quality assurance programs at Siliconix Incorporated. High-reliability semiconductor devices are routinely inspected in process for metallization integrity at windows and steps. Wire bonds and other surface structure are examined on finished devices.

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Features include:

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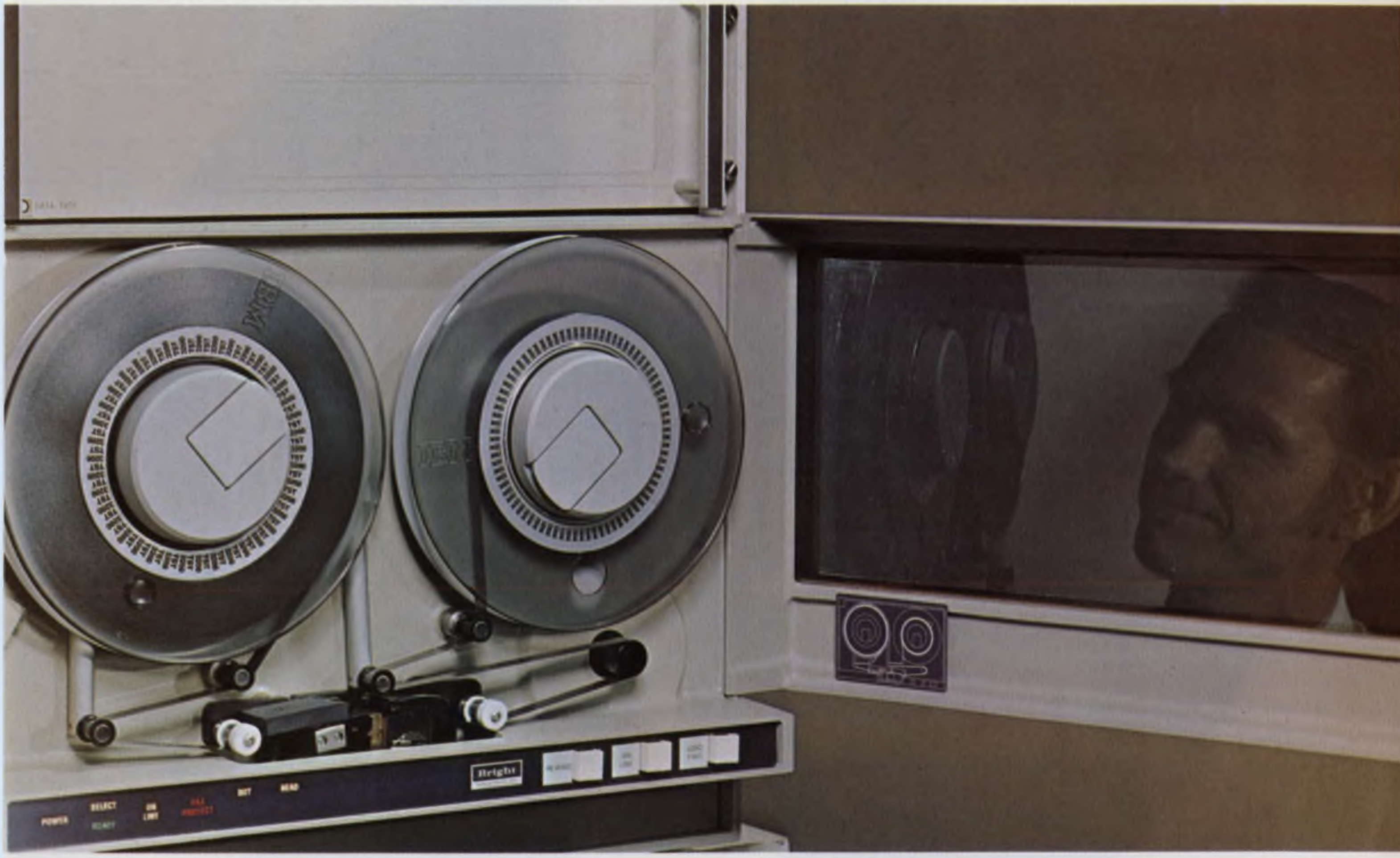
INFORMATION RETRIEVAL NUMBER 32

The moment you open the dust cover, you sense it.



Look closer. The cover frame is cast of solid aluminum. So is the deck panel.

No wonder they fit together perfectly—like the door of a well-made car.

Bright tape decks may be the most solidly built tape decks in the world.

The use of cast aluminum is not frivolous. It provides a perfectly rigid base for the tape guides and the capstan motor. A base that is mounted at only three points so it can't be stressed.

Construction like this means that the tape drive can't come out of alignment—the tape always runs true, and tedious adjustments are simply not necessary.

You can buy Bright tape decks in either 8½ or 10½ inch models configured to suit your needs. Anything from the bare necessities to fully buffered electronics and internal formatting. You can even get an interface.

Tape speed is 12 to 45 ips, bi-directional. Packing density is 200, 556, or 800 bpi on 7 tracks or 800 or 1600 bpi on 9 tracks. Interface is by TTL/DTL logic.

For a tape deck like this, you would expect to pay a premium. And you do, about 10%. But you get what you pay for—a tape deck that is truly impressive in your system.

More information is available. Contact Bright Industries, 686 West Maude Avenue, Sunnyvale, California 94086, (408) 735-9868.

Bright
INDUSTRIES INC.
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See Bright at '73 NCC, Booths 1629, 1631, 1633.

INFORMATION RETRIEVAL NUMBER 33

INFORMATION RETRIEVAL NUMBER 35 ►

washington report

Heather M. David
Washington Bureau

1974 space program off and flying

The fiscal '74 space-program budget has passed its first major Congressional hurdle with ease, but it still faces a major challenge sometime after Memorial Day. The House Science and Astronautics Committee treated NASA like a benevolent uncle, adding $57.5-million to the $3-billion budget request.

The committee, now headed by Rep. Olin Teague (D.-Tex.), added $25-million to the $475-million space shuttle R&D request; $10-million to Skylab, $7-million for a backup ERTS satellite, and $5-million to replace a Convair 990 research aircraft lost in a recent crash. A total of $10-million more was added for nuclear research. Only minor reductions were made by the committee—in the physics and astronomy, lunar and planetary, and tracking areas.

The Senate Aeronautical and Space Sciences Committee also is expected to be generous with NASA's request. However, space lobbyists are watching to see what Sen. William Proxmire (D.-Wis.) and the appropriations subcommittee he heads will do.

Air Force seeks a $10,000 missile

The Defense Dept. is bearing down hard on contractors to design a new air-to-air missile to a specified price. The Air Force, acting as agent for the Navy as well, will issue competitive contracts for the design of a short-range, air-to-air missile that must not cost more than $10,000 per unit. This target price is reported to be far below the cost of most existing missiles and has been thrown as a deliberate challenge to industry designers. Among the key elements that will determine the low cost of the missile, the Air Force says, are the target seeker, guidance and control systems and autopilot. Contractors will perform cost-performance tradeoff studies under three to five-month contracts to see if such a price tag is feasible.

Project Sanguine moving into design phase

Three companies participating in the study phase of the Navy's Project Sanguine extremely-low-frequency (ELS) communications system have been awarded contracts of approximately $3-million each to proceed into the design phase. They are RCA, TRW and GTE Sylvania. The system, which will operate within the frequency band of 30 to 100 Hz—with the most likely carrier frequencies being 45 to 75 Hz—is to consist of a grid of underground antenna. The grid is to be placed in an area of low-conductivity rock.

Defense Secretary Elliot Richardson, in his brief tenure at the Pentagon, reaffirmed an earlier decision by his predecessor, Melvin Laird, that the Sanguine complex will be placed in Texas rather than Wisconsin. The present experimental system is in Wisconsin.

Air Force considering new command-post electronics

The Air Force may start contracting soon for development of advanced communications equipment and remote terminals that will be carried in the second-generation version of the Advanced Airborne Command Post. The service's Electronics Systems Div. has notified contractors that it is considering issuing a request for proposals for development of a prototype system. It would be installed in a Boeing 747 aircraft mockup and undergo stringent electromagnetic-pulse testing. Contractors are already vying hotly for an upcoming contract to integrate existing command-and-control equipment in the first three Advanced Airborne Command Post aircraft. The Pentagon plans four more of the aircraft to carry new-generation equipment.

U.S. widens licensing of its inventions

The General Services Administration has at long last issued new patent licensing regulations in response to a Presidential directive of 1971. It should result in broader licensing of Government-owned patents to American businesses. The National Technical Information Service is computerizing Government patent information and will shortly begin publishing it in abstract form. The new regulations permit exclusive licenses of Government inventions, although nonexclusive licenses are preferred, the GSA says. Meanwhile bills for broad patent reforms have been introduced in the House and Senate, with the Senate Judiciary Committee expected to take the lead in hearings.

Capital Capsules:

The Army's Harry Diamond Laboratories **plans a study of the effect of electromagnetic-pulse phenomena** on circuits. It will use an electron beam, modified to improve the electron energy spectrum, area of illumination and pulse width. . . . **The U.S. will exhibit several lines of computers in Peking** on Sept. 18. A half-dozen computer firms are expected to show their wares to the Chinese, including both scientific and general-purpose equipment. . . . **Two major military electronics procurement offices will be closed** and their activities shifted elsewhere as a result of recent closings of some bases. The Army is shutting its Electronics Command procurement offices in Philadelphia. The Navy is closing the Naval Electronics Supply Office at Great Lakes Naval Base, Ill. . . . Sen. Stuart Symington (D.-Mo.), acting chairman of the Senate Armed Services Committee, **has asked the Controller General to investigate the enormous rise in costs—from $138-million to $250-million—in the Morris-Knudsen Co. contract for construction of Safeguard ABM facilities** at Grand Forks, N.D. . . . An Apollo 13 astronaut, John Swigert, **has been named executive director of the staff of the House of Science and Astronautics Committee** and will start work July 1.

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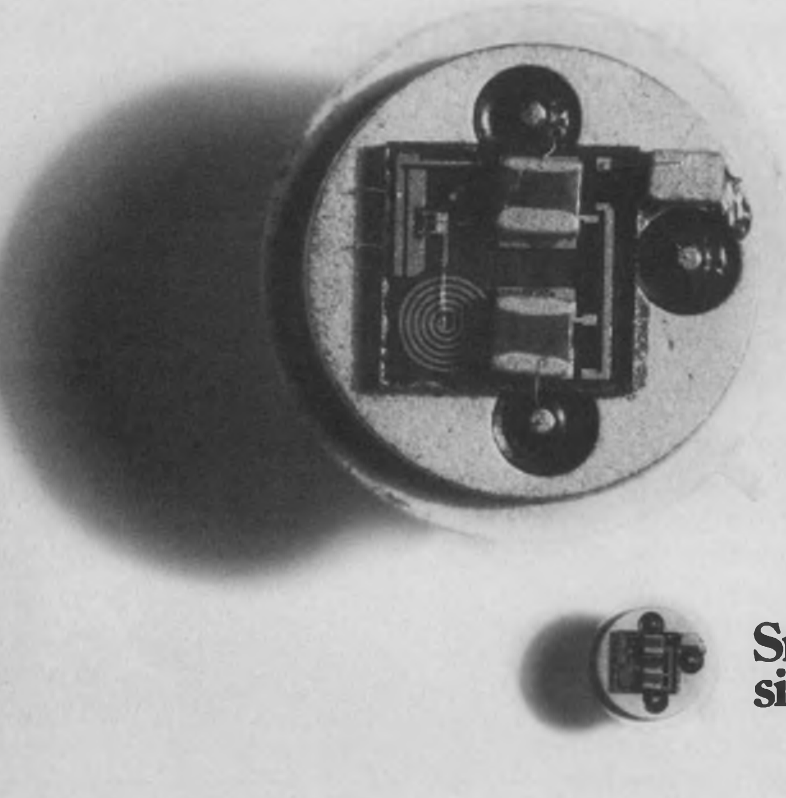

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GPD-461	Same as GPD-401, except three external capacitors are required to establish low frequency roll-off													27
GPD-402	5-400	13	1.0	6.0	−20	+6	+18	2.0	2.0	15	24	−65 to +200	1.0	29
GPD-462	Same as GPD-402, except three external capacitors are required to establish low frequency roll-off													26
GPD-403	5-400	9	1.0	7.5	−20	+15	+26	2.0	2.0	24	65	−65 to +200	1.0	30
GPD-463	Same as GPD-403, except three external capacitors are required to establish low frequency roll-off													27

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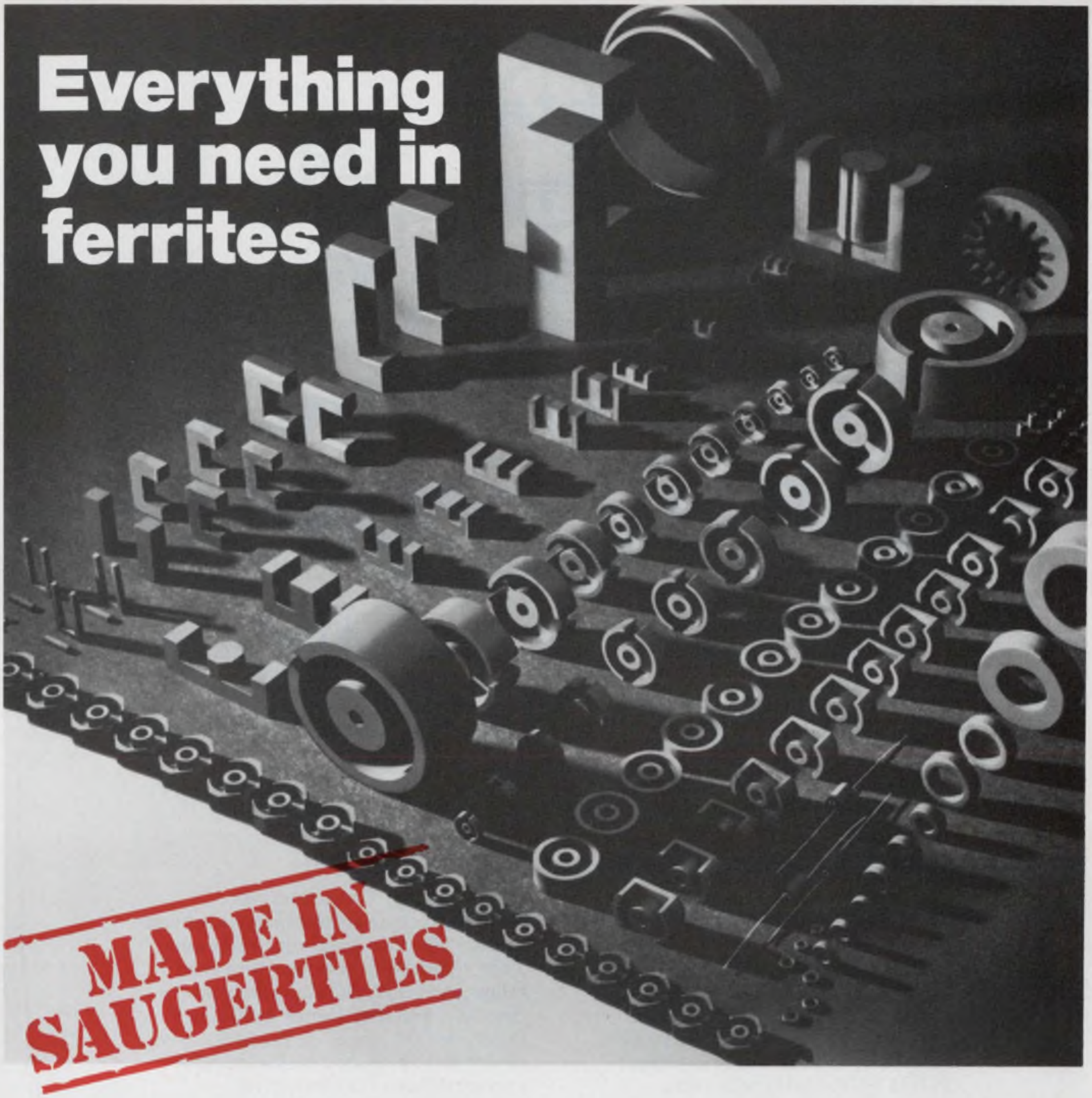

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INFORMATION RETRIEVAL NUMBER 39

editorial

Enter a new computer show – and new hope for the future

The Fall and Spring Joint Computer Conferences are dead. But a new star has risen in their place—the National Computer Conference and Exposition.

For more than 20 years, the traditional fall and spring exhibitions were the key meetings of the computer field. They served the computer industry well during a period of phenomenal growth and technological change.

Their peak year was reached at the 1969 Fall Joint Conference in Las Vegas, where more than 26,000 visited about 1000 booths. Then came the crunch.

The national recession caused potential customers to cancel or delay the purchase of computer systems. Old-time users, instead of upgrading their systems—as they had formerly done almost annually—made do with what they had. At the same time it became apparent that the computer business had become oversold and underutilized.

The effect on the spring and fall conferences was dramatic. Major computer manufacturers dropped out of the shows, and many other companies simply found it too expensive to exhibit in what were essentially regional shows. And, of course, attendance declined.

The result was that the American Federation of Information Processing Societies (AFIPS) decided to replace the two three-day semiannual conferences with a single five-day national computer show. It will open in New York City on June 4.

An AFIPS spokesman describes the new show this way: "The first national gathering of the data-processing community to examine the total picture of computer technology, its application, emerging uses and its impact on user industries and the world economy." If statistics are indicative of success, this show already has it made. More than 700 booths have been sold, representing over 200 companies. AFIPS says it expects over 30,000 visitors. Major mainframe manufacturers—most notably IBM—will exhibit after having previously dropped out. The technical program has been greatly enlarged.

The editors of ELECTRONIC DESIGN share the optimism of the sponsor and exhibitors. We, too, believe in the future of the computer industry. This special Computer '73 issue confirms that belief.

Good luck to the First National Computer Conference and Exposition!

Ralph Dobriner

RALPH DOBRINER
Managing Editor

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We've combined, refined, buffered, and naturally, improved it.

Improving a product like System 8000 is not a simple matter. We saw to that when we designed the industry's first dual density 800/1600 cpi tape system. But we listen to our users. And what you want — you get.

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We've taken our Model NRZI Format Control Unit and our Model 8216 PE Format Control Unit and combined them into one neat box. Model 8217.
It does everything the former two did — controlling up to four transports in a system. These can be Models 8109, 9-track NRZI/PE; Model 8108 NRZI and Model 8107, 7-track triple density. Mix or match.

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Now that the world has flipped over our OEM Model 74, can we make them fast enough?

When we introduced our Model 74 in 1972, we knew we had a great little OEM minicomputer.

We just didn't know how great.

We knew a lot of OEMs would like the hardware multiply/divide, 16 general registers and directly addressable 8KB core – expandable to 64KB. But we didn't know so many OEMs would beat down our door to sign up for it within the first 6 months.

What you need is what you get.

We had an idea that the 80-nanosecond solid-state Read-Only-Memory and the multiplexor providing an I/O system for communicating with up to 255 peripheral-oriented device controllers would turn on a lot of OEMs. But who would've guessed we'd have the big machine tool manufacturers, electronics companies, peripherals houses and controls companies standing in line for it?

The $3600* OEM Model 74.

We were pretty sure a lot of OEMs would appreciate the upward compatibility of the Model 74 and our Mix and Match discount schedule, which gives cumulative credit for all machines bought, regardless of model. But we never even dreamed we'd have to tell our manufacturing people to make them by the bushel to keep our 30-day delivery schedule.

Maybe it's the $3600 price.

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Maybe it's just the way it does so many jobs so well.

Whatever it is, we'll keep making them just as fast as our OEM customers want them.

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INFORMATION RETRIEVAL NUMBER 42

Computer '73
A Special Issue

Cover photo by Jean-Pierre Ragro—Goldust Exchange, courtesy of Data General Corp.

The push for hardware

Symbolic concept of General Electric's Mark III Information Services Network. Outer ring of blocks represents low-speed remote concentrators. Blue colored blocks represent high-speed data concentrators. The third ring depicts preprocessor computers. Next ring performs batch processing. The central circle features "future massive storage devices."

What's new in computers? For today's engineer—whether a designer of computers, a user of them, or both—a more appropriate question might be: What isn't new? Design concepts and applications are changing—radically, in some cases. Not only hardware—software, too—is affected.

In system architecture, there is a continuing demand for better performance at lower cost. The demand is being met by incorporating faster elements—semiconductor logic and memories—in the computer system and splitting the main memory into sections to speed data exchange between the memory, central processing unit and other system elements.

In memories, semiconductors are making headlines with potentially explosive growth, but cores are still a major factor—and expected to remain so for the next decade and possibly beyond. New techniques are lowering the cost of core stringing and core-array fabrication. Manufacturers are also continuing to seek refinements in disc and tape technology. Increases in track density are expected to improve the speed of discs and to lower their cost. Meanwhile more versatile magnetic-tape systems are beginning to emerge,

and software power

The cost of programming today represents nearly 50% of the price of the computer. Efforts are underway to boost programmer productivity by techniques like stack architecture and microprogramming. These are making it possible to provide greater performance with each of the programmer's instructions. Virtual memory is another concept finding increasing use.

including one that employs a transverse recording technique.

Microprocessor chips are beginning to fill the gap between calculator chips and minicomputers. These MOS/LSI processors can be programmed to perform not only arithmetic functions but data processing as well. They have even begun to replace small, dedicated minicomputers in some applications.

Printers and plotters are generating a great deal of excitement in the dynamic world of peripherals. Printers are becoming faster and cheaper. Although current printer outputs range from 10 characters per second to 2000 lines per minute, most of the action is in the speed range of 30 cps to 300 lpm, aimed primarily at the minicomputer market. In this range nonimpact printers are providing a challenge to traditional serial-impact printers.

In software, techniques like stack architecture and microprogramming are increasing programmer productivity.

No single issue of ELECTRONIC DESIGN can hope to cover in full a topic as vast as the computer industry, but in the following pages some of the more important trends are discussed.

Changes in architecture users more computer at

Jim McDermott, Eastern Editor

More performance for less money.

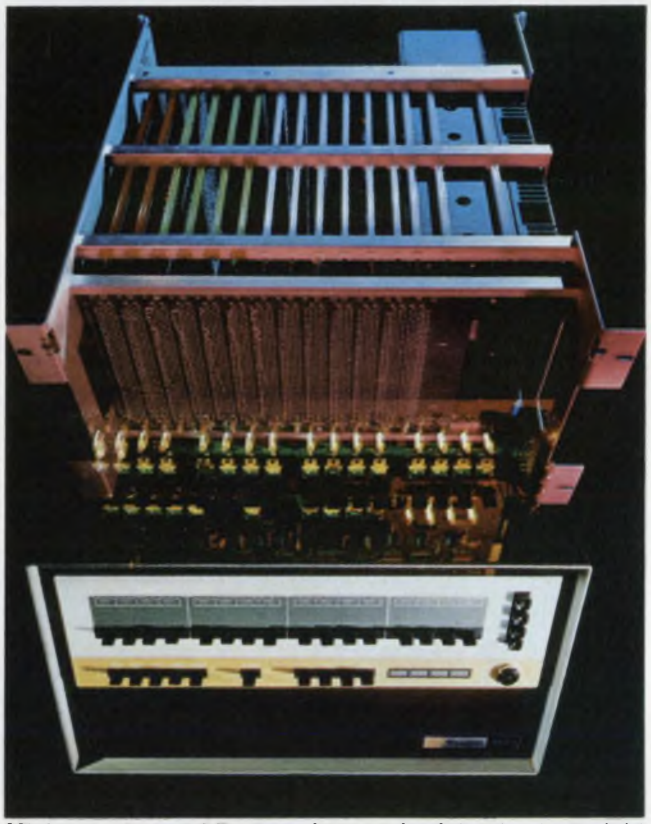
The demand is timeless in the world of business, and computer architecture—the functional elements of the computer system and the subsystems needed to process data—is changing radically to meet it.

The simplest approach has been to incorporate faster system elements, such as semiconductor logic and memories. But a number of other approaches are being used. The designers are doing the following:

- Increasing the speed of data exchange between the memory, central processing unit and other system elements by splitting the main memory into more than one section. Each section is accessed at the same time.
- Making slow main-core memories appear fast to the computer by incorporating rapid semiconductor "cache" memories between the central processor and the main memory.
- Increasing the apparent size of the main memory through the use of "virtual memory" techniques.
- Attacking the software/programmer bottleneck by transforming software routines to hardware. Microprogramming is being used.
- Boosting the capability of the computer by making it a "virtual machine." Nanoprogramming techniques—two levels of microprogramming—are being employed.
- Increasing computing speed by converting long serial operations to parallel concurrent, shorter ones.
- Developing large data-processing systems capable of running more than one program at the same time.
- Building fast supersystems for complex calculations.

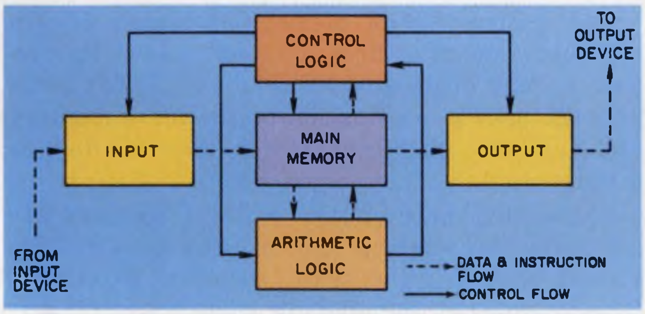
With few exceptions, the basic architecture has been derived from the first stored-program computer, the von Neumann machine (Fig. 1). Modern computers are extensions or permutations of the five basic sections of the von Neumann machine, frequently called a single-processor or unit computer. The five sections are:

1. The input—transmits data and instructions from an input-output device—say, a teletypewriter—into the computer main memory.
2. The main memory—stores the instructions needed for the machine to carry out computations or to process data. Also stores the data and the results of the computer operations on that data,

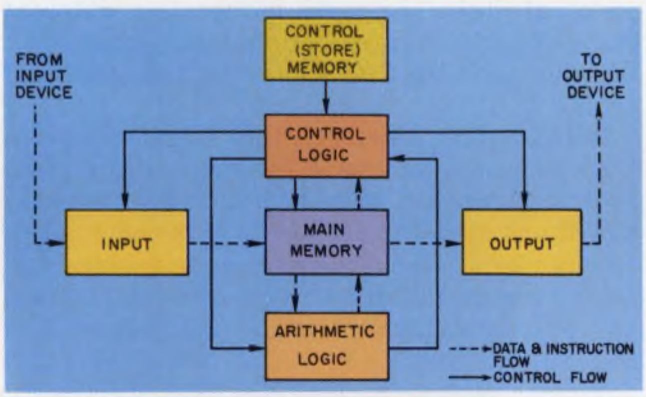


Minicomputer architecture has evolved in the last eight years from a simple single processor to powerful machines, like this Microdata 1600.

are giving less cost



1. **The architecture of the basic single processor** is derived from the configuration of its five elements: the input, the output, control, memory and arithmetic unit.



2. **The microprogrammed computer** uses an additional control memory in which the program elements are stored. These elements carry out the instructions.

both intermediate and final.

3. The arithmetic logic unit—performs both mathematical calculations and logical operations.

4. The control logic—decodes the instructions and then causes the machine to execute them.

5. The output—transmits the completed calculations or data to the input-output device for presentation to the computer user.

Even today, many small computers retain this type of architecture, performing serial operations in executing the instructions for calculation or data processing. But for the larger data processors, where the instructions are complex and may run into the hundreds, waiting for a machine to complete a full serial data-processing cycle would be intolerable. For this reason, the speed of the larger machines has been stepped up not only by using faster computer elements but, more importantly, by performing many of the processing operations concurrently.

Modifications to the machine architecture to obtain this concurrency include overlapping of operations, putting data in and taking data out of the computer simultaneously and providing sufficient memory and computing power to enable the machine to handle more than one problem at the same time.

Overlapping of operations fundamentally depends on the use of architectural variations to modify the serial-operating sequence of the von Neumann machine.

Splitting the memory speeds processing

With some modification of the system, it is possible, for example, to generate during the operating cycle of one instruction the address of the next. This can be accomplished by memory interleaving, or dividing the memory into independent areas so the words corresponding to the consecutive addresses are in different places and thus can be accessed at the same time.

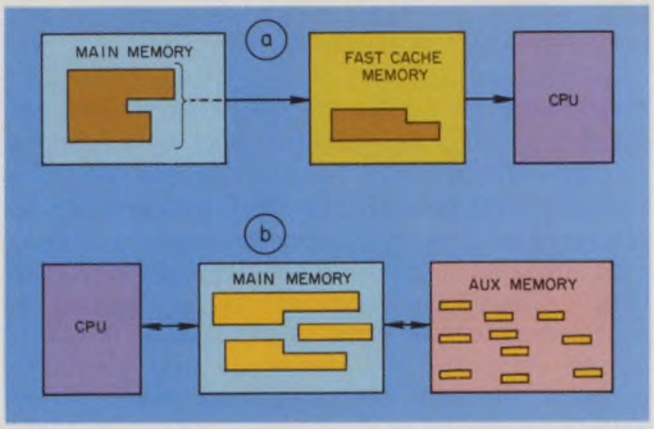
Additional speed is obtained with this arrangement because core-memory access takes longer than arithmetic or logic operations. Splitting the memory into two sections—instruction and operand storage—the way the Univac 1108 does, provides two paths to the central processor unit, in which the control resides. A second word is read during that half cycle while a previously read word is being written back into the memory.

Even further segmenting of the read-write memory cycle is used in the Univac 1100 by division of the main memory storage into independent sections that have their own paths to control. Odd and even addresses are stored in alternate sections of the memory. The central processor is also segmented into twin arithmetic-logic units that provide a simultaneous processing capability.

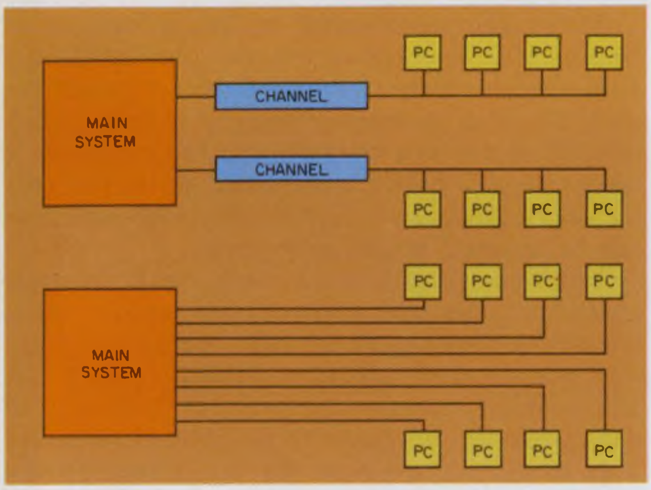
Architecturally, memories are developing into heirarchies of storage.

"A profound change that I see," says Donald M. Edam, director of Univac's development center in Roseville, Minn., "is the increased use of storage. The size of memories is growing because the cost is decreasing. There is also a trend towards multiple levels of memory. We have a bilevel memory in the Univac 1110. The fast main store is plated wire, and the somewhat slower core is extended storage.

"The off-line storage, such as disc or drums,



3. **A main computer memory may appear to be faster or larger than it really is.** A fast semiconductor cache memory between the main memory and the CPU (a) gives the main memory the apparent speed of the cache memory. Keeping track of data and swapping it into and out of the main memory onto an auxiliary memory (b) makes the main memory look substantially larger than it is.



4. **Two methods of controlling the data flow between the peripherals and main computer are** the shared channel (at top) and the floating channel (at bottom). IBM uses the shared-channel system and Burroughs the floating.

is another level in the memory heirarchy, planning and selecting a particular heirarchy involves tradeoffs between cost and performance."

Tricky handling of data

In taking advantage of many of the architectural tricks to speed data processing, designers have made the computer—or elements of it—look faster or more powerful than the hardware actually is. Examples are found in the use of cache memories, virtual memories and even virtual machines.

Several IBM machines use cache memories—small semiconductor memories that are several times faster than the large, lower-cost and slower main memory. The cache memory—IBM calls it a buffer—is situated between the main memory and the central processing unit (Fig. 3). The instructions and data needed for a program in progress are moved ahead of time—in small chunks—from main storage into the faster cache memory. The central processing unit uses this cache data for the actual operation of the machine.

The net effect, from the operating viewpoint, is that of a machine with a large, fast memory. However, additional look-ahead logic is required in the design to anticipate the data and instructions coming up, so they can be transferred to the cache before they are called for by the processor.

Efficiency and throughput improved

The use of virtual memory increases system efficiency and the throughput of data. The virtual memory featured by IBM in the 360/67 and 370/125 uses a combination of the main memory and auxiliary memories, which may be disc or drum.

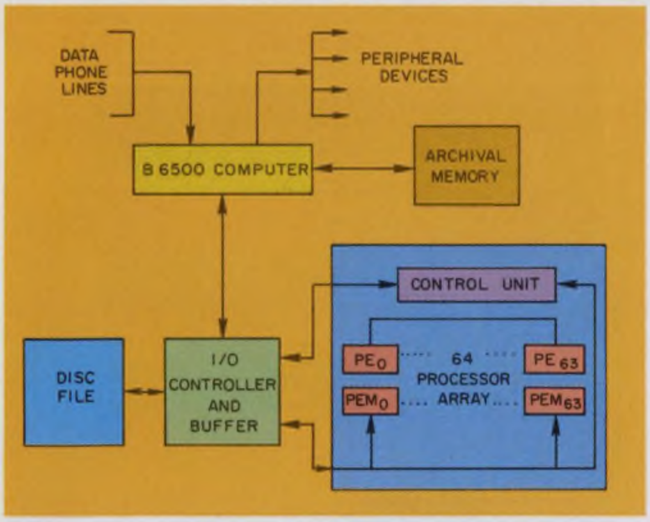
Classically, large chunks of main memory are set aside for each program. But to create a virtual memory, the main memory is divided into a number of segments or small pages of, say, 2-k or 4-k bytes each. Program and other data elements are assigned to these pages. Under operating conditions, the programs and data are scattered about the main memory on different pages. When several programs are processed at the same time, the data appear in these scattered areas.

With virtual memory, the computer keeps track of where each page is stored at any given instant. When any page is not in use, it is removed and stored in an auxiliary memory, to be replaced by a page of a program being executed. Should a page in the auxiliary memory be needed, it is automatically recalled and restored in the main memory.

Virtual storage is used in RCA computers, Honeywell's Multics system, Xerox's Sigma series and Burroughs computers. Burroughs, which has used virtual memory since 1962, transfers segments that vary in size, with the size related to where the programs break. IBM, on the other hand uses segments of arbitrary size.

Honeywell's Multics system achieves the effect of a large, segmented main memory through the use of Honeywell 645 segmentation and paging hardware. A special feature is protection of file data.

Microprogramming—a computer design concept that is more than 20 years old—is now a firmly established building block in the architecture of both minicomputers and large systems. A few years ago microprogramming was found



5. **Parallel processing with an array of 64 independent processors** allows Illiac IV, one of the largest supercomputers, to handle 200 million instructions/sec.

only in some larger systems, including those of IBM, RCA and Honeywell. It wasn't widely used in the smaller machines because the cost of its key element—a read-only, or random access, memory—was excessive. But within the last two years low-cost, high-capacity semiconductor memories have become available, and they are now becoming widely used as special microprogramming control memories (Fig. 2).

A principal present use of microprogramming is in computer emulation—that is, the microprogrammed computer can be tailored, by changing the control-memory contents, to operate as an entirely different machine.

With microprogramming, the instruction routines for many operations are stored in the control memory in a straight-forward sequence. The programmer need only initiate sequences, and the micro-instruction data stored in the control memory carries out the instruction sequence.

Nanoprogramming expands computer power

One of the newer trends in computer architecture is nanoprogramming—in which two levels of microprogramming are used to produce a virtual machine. A virtual computer that is one that can simulate the architecture of a variety of computers. One example of the nanoprogrammed computer is the QM-1 by Nanodata, Inc., Buffalo, N.Y.

John Hale, vice president of Nanodata, who describes the QM-1 as a "general-purpose, special-purpose machine," says: "It is a general-purpose machine that can be configured, through the use of horizontal and vertical levels of microprogramming, to emulate other computers. We see it as directly supporting higher-level languages, such as APL, Fortran and Cobal."

The key feature of the QM-1, Hale explains, is the writeable control stores for both horizontal and vertical levels of microprograms. In operation, the vertical microprogram calls upon micro-instructions in the horizontal program, called the nanoprogram.

"You can change the contents of these memories rapidly, and therefore change the instruction sets that they define," Hale says. "As a result, you can switch between an instruction set that supports one machine architecture and another set that supports another."

A further important feature that Hale points out is the highly parallel structure of the QM-1.

"The QM-1 has 14 buses," he says, "and it has many units that operate in parallel. Therefore you can get a high degree of parallelism for solving special emulation problems.

As to how the QM-1 design affects future machine architecture, Hale predicts that the concept of multiprogramming will be extended down into the microprogram level.

"In four or five years, we'll have what we call a set of virtual machines," Hale says, "all evolving around the one basic multimicroprogrammed system. This future machine will have the ability to switch rapidly between the virtual architecture of a machine that's supporting APL to another machine that's doing process control, to perhaps another machine doing file managing."

The capacity of a computer system to do work depends to a large extent on the capacity of the input/output system and peripherals to feed data in and extract it at speeds consistent with the operating capabilities of the central processing system. In some architectures a peripheral computer is dedicated to the input-output system control. In others, peripherals with buffered stores provide a partial answer.

Most computers incorporate independent access paths or channels. They act as traffic routes, allowing two or more data streams to flow simultaneously into and out of the computer (Fig. 4). However, in channel architecture—such as is used in IBM machines—channels are shared by two or more multiple peripheral controls that limit, to some extent, the transfer of information. One device assigned to a channel may have to wait for other traffic on the channel to clear, even though other channels in the system are free.

A free-channel search can be conducted by means of software, but this may not always be desirable because of a conflict with other jobs running in a multiprogramming mode.

The floating-channel concept, by Burroughs, links the I/O channels to the peripherals through an I/O exchange that is dynamically controlled. With this system, any available I/O channel can service any I/O device. Programmers are not concerned with channel optimization. Instead the system and its control automatically optimizes channel assignments.

As the workload of large systems has approached system capacity, the transfer of information into the processing system from large peripheral files has become a problem. With slower peripheral units, data from a number of peripherals flowing into a single channel are transferred by the multiplexing of bytes. Single bytes or small groups of bytes are fed into preset time slots. The peripherals are polled in sequence to see which has data to transmit.

For disc files and other high-speed peripheral units, data are stored in blocks around tracks. Each block consists of a number of bytes. Like the slower peripherals, the units are polled, and when a channel is open, the blocks are transmitted.

Parallel processing makes a supercomputer

For complex scientific calculations requiring extraordinary and fast calculating power, supercomputers have been developed, structured around parallel or array processing and serial or pipeline.

The ultimate in contemporary multiprocessing—the simultaneous processing of data by 64 parallel units—can be found in the Illiac IV supercomputer (Fig. 5). Capable of handling between 100 million and 200 million instructions per second at an I/O transfer rate of a billion bits per second, the system can conduct 64 computations simultaneously. The full system is under the control of a Burroughs B6700 computer.

The disc-file subsystem of the Illiac IV has intermediate data storage for the array with a capacity of 2.5 billion bits and a storage transfer rate of a billion bits per second. An archival memory, which stores data by burning microscopic holes in a thin film of metal with a laser, has a capacity of more than a trillion bits. It can be accessed at four million bits per second.

Installed at the National Aeronautics and Space Research Center at Moffet Field, Calif., where it is operated for the Advanced Research Projects Agency, Illiac IV has been used for three-dimensional modeling of aircraft, running simulated nuclear-blast tests and worldwide weather modeling.

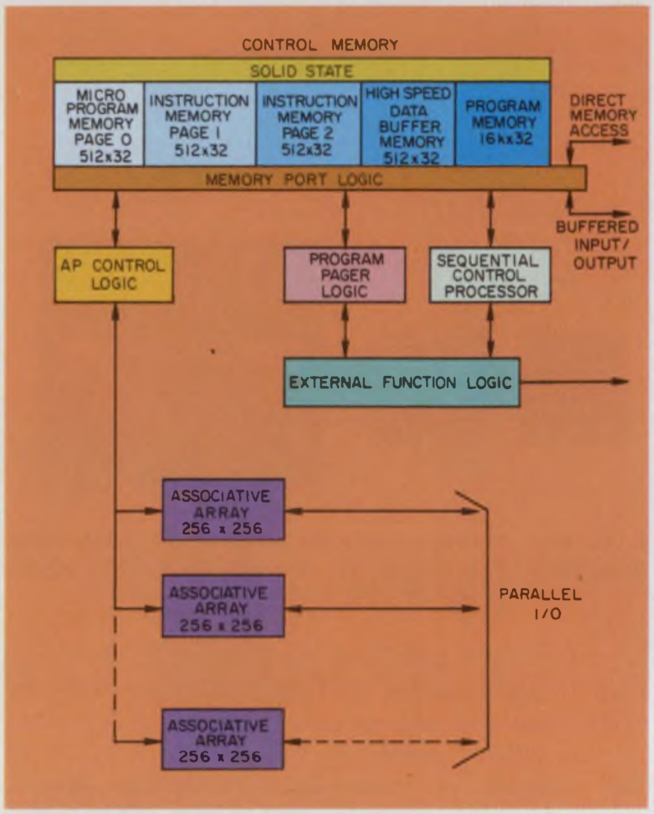
Minicomputers making rapid strides

Minicomputer architecture has evolved rapidly from simple, low-cost versions of larger computers to complex systems with substantial computing power.

"The mini started with limited capacity," says Andrew C. Knowles, vice president of the Digital Equipment Corp. "The first minis had a two-bus structure—an I/O and a memory bus. In most cases they were single-accumulator machines. And the instruction set was minimal.

"We've evolved from that base in the past eight years to quite a level of sophistication. For example, the PDP-11 is now a multiple-register machine. It has memory-stack capability. Its single asynchronous minibus structure has evolved to a multiple bus structure, including a fast memory bus and a fast I/O bus.

"The latest machine has floating-point capability in hardware, whereas in the older version it was in software. The PDP-11 now also has a memory management scheme—verging on virtual memory—that allows 16-bit machines to address up to 124-k bits of memory. Built-in features of memory management permit paging, segmenting and protecting data through memory."



6. **Associative array memories,** which can acquire data from a file without previous knowledge of their location, are used by Goodyear in the Staran computer.

Architectural differences exist between minicomputers and data-processing machines because they are called upon to perform different tasks. Minicomputers, Knowles points out, are real-time oriented. Pure data-processing machines are oriented to batch processing jobs like running off stacks of statistical data from cards and tapes—with high-speed throughput, both from multiplexer channels and high-speed peripherals.

Perhaps the most dramatic change in computer architecture, however, is stemming from the influence of low-cost semiconductor logic and memories. The semiconductor industry is developing ever-larger systems on a single chip.

"The minicomputers—they're usually the computer on a chip type of thing—are starting to be used as machines themselves," says Earl C. Joseph, staff scientist at Sperry Univac Computer Systems, St. Paul, Minn. "I see the microcomputer as the new big architecture for computers, particularly in the next five years. In effect, the microcomputer will relegate the computer to the level of a minor subsystem component."

Joseph explains why.

"If you look at the small, medium and large-scale computers of today," he says, "they're really major system components in terms of dollars. They are major system components in terms of the cost and manpower required to use them.

"But when you integrate the microcomputer into a system, it becomes a minor subsystem—almost like a transistor or IC component—in terms of both cost and usage. And that will be a revolutionary change in the whole computer market.

"First, the microcomputer will move into the minicomputer area. And then it will move into the small and medium computer field, replacing a large number of them simply because many of their applications can be performed by the microsystem—perhaps more than half, as time goes on."

A new computer structured after a distributed-intelligence microcomputer concept was recently delivered by Burroughs to the Avionics Laboratory at Wright-Patterson Air Force Base, Dayton, Ohio. It is a new LSI computer called the Aerospace Multiprocessor. It has many of the architectural advantages forecast by Joseph and others.

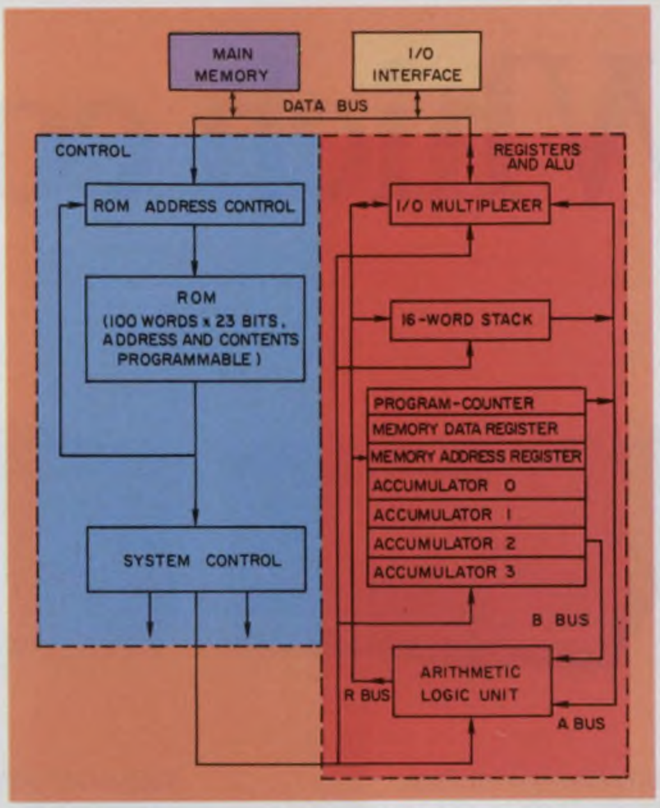
"The system delivered to the Avionics Lab," says William Clark, staff engineer at Burroughs, Paoli, Pa., "is built on LSI chips. It is more sophisticated than the stark microcomputer that people are today putting on chips."

The Air Force computer was built around the Burroughs "interpreter" concept, Clark points out. It is a building-block idea based on the fact that the price of logic is decreasing considerably.

"It therefore no longer makes sense to put together large systems, using a few processors that require software to do elaborate scheduling of computer resources, to achieve a high utilization rate," Clark explains.

"We say, let's use a lot of small processors because they don't cost a lot. It's not important that they be 95% productive, as is usually required. They can be 65% productive and still do a better job than the old systems.

"And not only that. Since we're not so uptight about keeping them 100% utilized, our control



7. **An example of a minicomputer on two chips** is National's CPC/P. It is a four-bit parallel processor with a maximum memory capacity of 65-k words.

software is greatly simplified."

There are five interpreters in the Air Force computer system, Clark indicates, with the logic partitioned to be compatible with a 1000-gate-per-chip LSI device. Because LSI of that density was not available, the unit was built with 500-gate-per-chip devices.

"The function of the interpreters is to perform all the functions that any processing element in any type computer would have to process," Clark points out.

The interpreters are programmed with two levels of microprogramming, similar to that of the QM-1 of Nanosystems. But the interpreter processors are all connected with multibus structures that permit parallelism between all processors.

All of the processors are allowed total access to the shared memory, Clark explains, so it is truly multiprocessing, not a multicomputer.

As a result, the interpreter can perform a wide variety of central-processing functions. It can perform the function of an I/O control module; special functions like matrix arithmetic, file sorting, file merging and file maintenance, and communication control.

The interpreter is versatile, Clark points out, because of its structure and because all of the control is stored in microprogram memories rather than in wired memories. ■■

Which company da

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Model: PDP-8E
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Speed (Cycle Time): 1200ns
Storage Capacity: 32K words
Word Size: 12 bits
DMA (Standard): yes
Input/Output slots: 3

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Price with 4K memory (list): $4,095
Speed (Cycle Time): 900ns
Storage Capacity: 32K words
Word Size: 12 bits
DMA (Standard): yes
Input/Output slots: 7

Digital Equipment Corp.
Model: PDP-11/15
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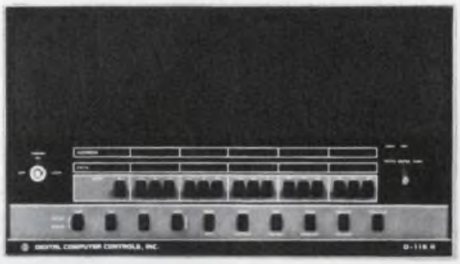

Data General
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Word Size: 16 bits
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Speed (Cycle Time): 960ns
Storage Capacity: 32K words
Word Size: 16 bits
DMA (Standard): yes
Input/Output slots: 7

Hewlett-Packard
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Gene Amdahl competition the machine big, but keep

David N. Kaye, Senior Western Editor

Dr. Gene Myron Amdahl, who has contributed uniquely to computer design in the last 20 years, believes that computers have become too complex and that "the number of logical alternatives at any given point" ought to be "at an absolute minimum." He also feels strongly that a supercomputer is needed for today's business applications—a computer that will be more powerful than such scientific machines as the Illiac IV, Control Data's Star and Texas Instruments' Advanced Scientific Computer.

To fill these seemingly contradictory needs, Amdahl is applying his design philosophy—"Make it as simple as possible"—to building the most powerful computer yet attempted. Called the A System, Amdahl's machine will challenge the top end of IBM's line: the 370/195.

Amdahl, who heads his own company, the Amdahl Corp. in Sunnyvale, Calif., is an apt challenger to International Business Machines. He was manager of architecture at IBM for the 360 series of computers, and, following that, he became an IBM fellow, with free rein to concentrate on advanced systems. He holds a Ph.D. in theoretical physics and belongs to the National Academy of Engineering. Seated in his comfortable office, he expanded recently on his approach to computer design.

Dr. Gene Amdahl, designer of IBM's 360 series, hopes to improve on his original creation.

Flexible and systematic

"The current state of large computer architecture demands too much regularity in the way you solve problems," he said. "What is needed is flexibility. You must be able to build a computer that goes from one task to the next in a way that is determined by the outcome of the preceding task. Upon completion of a task, it must be able to go on to one or several different tasks simultaneously. At times the computer may have to seem like different types of computers in the same box," Amdahl observed.

The computer Amdahl is developing will be smaller and more powerful than IBM's, he says. It will not be a straight parallel machine like the Illiac IV or a vector machine like the Star and the advanced scientific computer. It will be a multiprocessing system with the flexibility to modify its own task priorities, based upon the re-

plan: Make it simple

sults of preceding tasks.

The A-System computer, Amdahl says, will be compatible with current IBM software. The hardwired instruction set will include all IBM 370-series instructions plus several special instructions to enhance system flexibility. LSI technology will abound in the machine.

Logic will be implemented in ECL arrays containing up to 100 gates per chip. The ECL technology will be custom-designed, with propagation delays of about 600 ps. This is faster than any of the current standard families of ECL, Amdahl notes.

At least two types of memory will be used. Bipolar buffer memory will act as a scratch pad for the logic arrays. This memory will have an access time of less than 50 ns. MOS main memory will be used with an access time of less than 200 ns.

"Although we are going with p-channel MOS at the start," Amdahl says, "we are anticipating incorporating 4-k, n-channel MOS RAMs when they become available."

To maximize the computer's speed, two ground rules will be observed in the handling of the data. "The first," Amdahl explains, "is that once you start using a piece of data, it will have a localized high frequency of usage. Secondly, its neighbors will also have a localized high usage."

To maintain flexibility in the architecture, the computer is byte-oriented rather than word-oriented—that is, since different operations or jobs within the machine may call for different word lengths, the computer will process only eight-bit bytes regardless of word length. This is to maintain operational consistency while allowing the correct word length for each job.

Will such a computer sell? Amdahl is confident that it will, even at $3.5-million a throw. "The supercomputer market is not being satisfied by the current computer manufacturers," he says.

The heavy reliance on LSI is risky, some engineering specialists say; the technology is new, and Amdahl has had to create a new family of chips. The fact that the computer will use IBM software could pose further obstacles; if IBM changes the software, Amdahl will have to rework his circuits.

Even before he got his Ph.D. in 1952, Amdahl was an innovator. While working on his thesis at the University of Wisconsin, he helped to design the Wisconsin Integral Synchronized Computer. It was the first computer to use overlapping instructions. This development stimulated thought leading to today's parallel-processing systems.

After receiving his degree, Amdahl went on to IBM, where he was project engineer and chief designer for the IBM 704 and initial planner for the 709 and 7030. During this period his main contributions were the addition of communication channels for the handling of several peripherals in the 709 and the vigorous pushing of an all-solid-state second generation of computers. The 7030 was all-solid-state.

In 1956 Amdahl left computer design for a stint in the defense industry. He returned to IBM in 1960, and spotted potential trouble. "I saw how much hardware had been added to the 7030," he says. "I realized that the computer was too complex, and my design philosophy became, "Make it as simple as possible."

The architecture for the 360 series came out of a design competition between two groups at IBM in the fall of 1961. "Originally," Amdahl recalls, "the goal was to design an upwards compatible line—that is, higher and higher performance could always be added within the framework of the basic architecture. I pushed for an architecture that was compatible both upwards and downwards. Why neglect the high-volume, low-performance segment of the market? I was told that I was crazy, it couldn't be done. We did it."

Amdahl opted for functional design: "Since the 360 line had to accommodate a variety of technology, we tried to specify the architecture functionally. That way the architecture was the same from the bottom of the line to the top."

Several major contributions to computer design came out of the 360 program.

"Microprogramming was a major contribution in the scale that it was applied," Amdahl notes. "It was not an original idea with us. The decision to use read-only memory microprogram control was made because it appeared that we could build the computers cheaper. I'm not sure it worked out that way.

"Another major contribution was the concept that addresses should not be stored with instructions in the instruction stream. We could then build small machines with small addresses and large machines with large addresses." ■■


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INFORMATION RETRIEVAL NUMBER 44

Memories turn to newer but core hangs on as the

Jules H. Gilder, Associate Editor

Like the vacuum tube when transistors first appeared on the scene, core memories are under heavy fire. The semiconductor memory—offering smaller size, higher density, lower power consumption and a big slash in costs—is grabbing headlines. RAMs of 4-k bits are being delivered, and 8-k RAMs are appearing in the laboratory. Are core memories doomed?

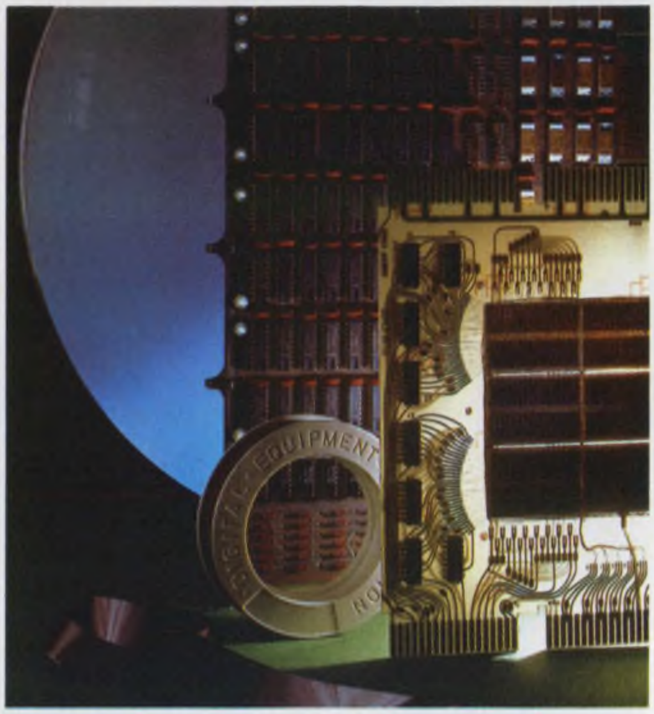
Most computer manufacturers say the answer is yes. But don't look for a fast death, they add. Core is expected to remain a significant factor in computer memories for the next 10 years—and possibly longer, if its demise parallels that of the vacuum tube.

This threat to core's survival follows by only a few years a short-lived challenge by plated wire and magnetic films. Core turned back that thrust and will hang in there even as semis take over, manufacturers say, because it has three major advantages: relatively low cost, versatility and nonvolatility.

Core costs are coming down, notes Dana Moore, department manager for mainframe memories at Honeywell, because of new techniques that lower the cost of core stringing and core-array fabrication. Some manufacturers have started to eliminate manual labor with automatic stringing techniques. This requires use of a two-wire organization instead of three-wire.

This resurrection of two-wire technology, says Robert Savell, manager of memory and power-supply engineering for the Digital Equipment Corp., Maynard, Mass., will also increase the speed of core memories, making them competitive with high-speed bipolar types. Cycle times of less than 500 ns and access times under 100 ns will be possible, he says.

But Honeywell's Moore, noting the trend toward two-wire organization, says these improved characteristics come at a price: The need for additional semiconductor support circuitry.



Key elements of memory technology include MOS semiconductor devices, magnetic ferrite cores, magnetic discs and magnetic tapes.

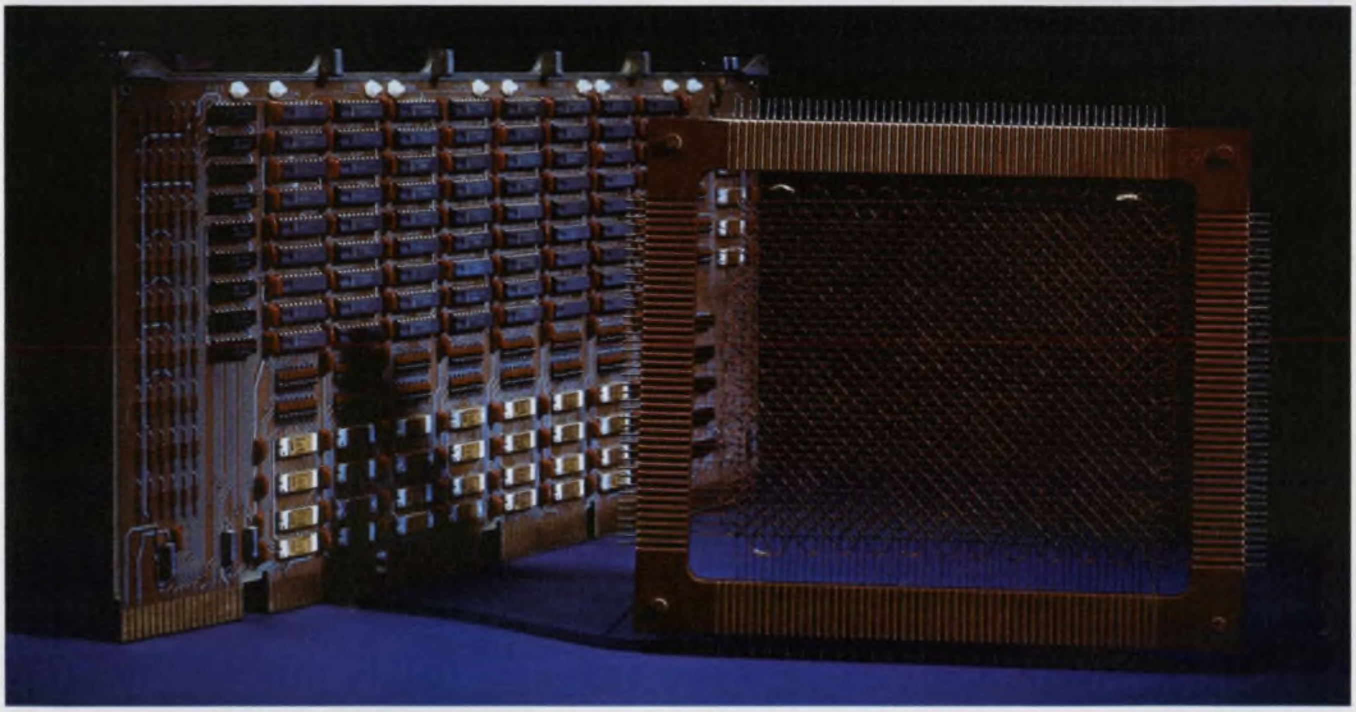
Another factor enabling core manufacturers to keep prices down is continual improvement in mass-production techniques. One of these techniques, says Robert Miller, vice president of marketing for the Data Products Corp., Woodland Hills, Calif., is the roll-cut core process, which consists of punching cores out of a tape of ferrite material instead of pressing each core individually from a mold. The result, Miller points out, is more uniform characteristics from core to core. This is particularly true of small cores, where the powder particles themselves become a significant percentage of the diameter of the core. And with more uniform characteristics, yield at the core level is increased and

materials, old reliable

—known as TIN—can be operated over a temperature range of −25 to +100 C without compensation. Because heat is no longer a critical factor, he says, it is now possible to make denser core planes. And he notes, that Ampex is now producing the largest core plane available, a 1.2-megabit unit.

Ampex is also working on ways to increase switching speed. This can be done by going to smaller cores, Sell notes, but with the trend toward automated stringing, that is undesirable. In fact, automated techniques may result in manufacturers switching from 18-mil cores to the larger 22-mil devices. The bigger hole would make it easier to automate, Sell explains.

Another way to increase switching speed in



MOS semiconductor memory card (left), made by Digital Equipment, can store about 10 times more data than the Honeywell core plane (right). In addition to the increase in storage density, the MOS memory card also contains the peripheral electronics necessary for driving the decoding the memory. The core plane needs external circuitry.

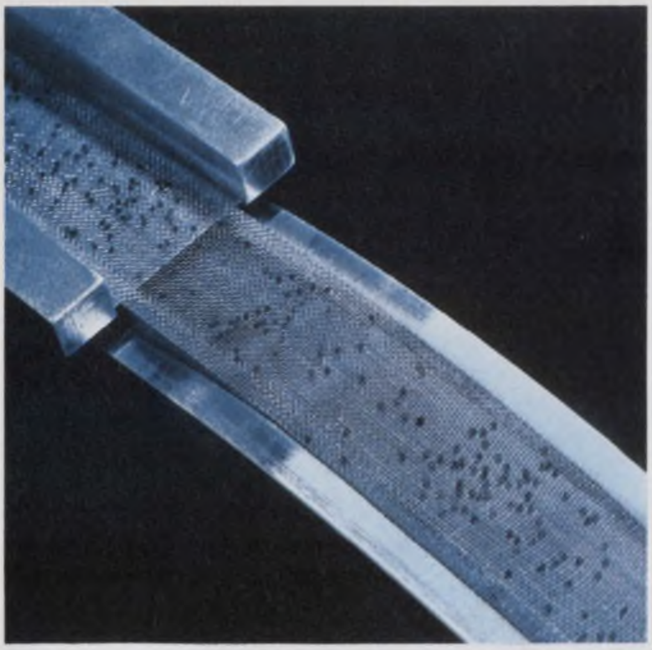
costs are reduced, Miller notes.

Improvements in sensing data are also helping to bring costs down, reports DEC's Savell. Current systems are using one amplifier to sense data from 8 kilobits. Work is currently going on to develop a sense amplifier that will sense data from 16 kilobits, and designers are considering 32-kilobit sense-amplifier systems.

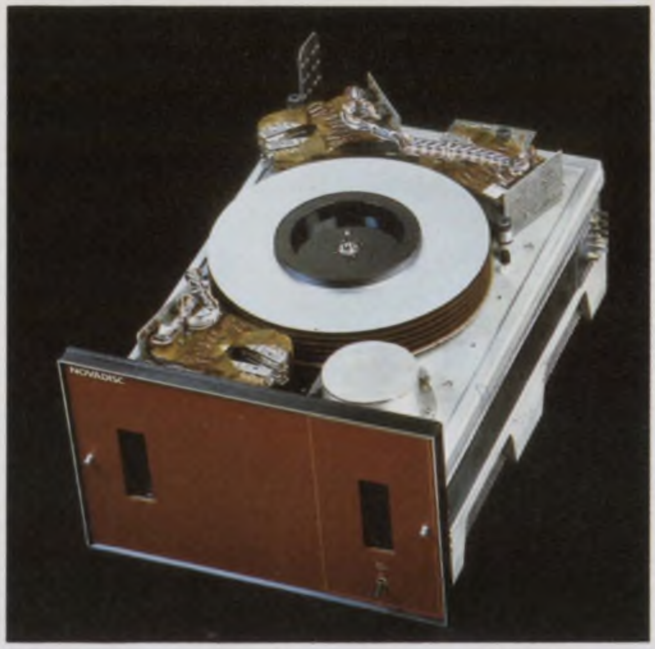
New materials are also being investigated by core manufacturers in an effort to beat back the challenge of the semiconductor memory. The Ampex Corp. of Marina del Rey, Calif., has developed a new temperature-independent ferrite material. According to Victor Sell, senior core product manager for the company, the material

cores, Sell notes, is to use partial flux switching —a technique that uses pulses that are shortened from 250 ns to 150 to switch the core. This has only recently become feasible with the advent of temperature-independent core, Sell explains, because only now is it possible to study the switching mechanism involved without being hindered by variations due to temperature.

Partial flux switching can also be used to produce an "intelligent" core, Sell says. In such a system the core would be divided into equal concentric rings, each of which would represent a different level. The levels, or states, would be determined by the write pulse, with the first state represented by a 40-ns pulse, the second an



These 18-mil cores were produced by a molding process at Data General's new core facility.



Discs should remain the leader in high-performance mass memories for the next decade.

80-ns pulse, the third by a 120 ns pulse, etc.

With an intelligent core system, Sell notes, a designer could use a number system with any base that was convenient, instead of the binary system used in today's computer. For example, binary-to-decimal and decimal-to-binary converters could be eliminated if 10 states are assigned to each core and decimal logic, instead of binary, is used.

Another advantage of a multilevel core system is that hardware could be greatly reduced. As an example, Sell notes that one byte is represented by eight cores, which are capable of being in one of two states for a total of 64 possible combinations. By assigning six states to two cores, you get the same 64 possible combinations, Sell explains, but hardware has been reduced by a factor of four.

Recent work with these cores, he adds, indicates that they can be used to perform logic as well. Sell sees point-of-sale systems as a very good application area.

Plated wire: Down but not out

What happened to plated wire? An admittedly viable technology, it has not been widely accepted by memory manufacturers. Only a few companies have produced wire memories, and, without strong competition, the technology has remained relatively static. The reason seems apparent: Plated wire is a more expensive technology than semiconductor. An indication of this is the recent switch by Univac—a long-time champion of wire memories—to semiconductors.

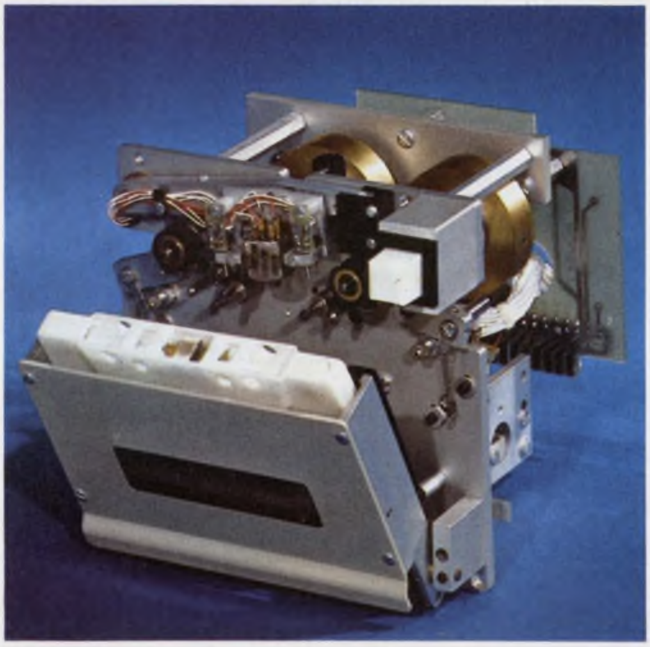
According to Donald Edam, director of Univac's Roosevelt Development Center, Roosevelt, Minn., semiconductor memories now offer superior price/performance advantages. He is quick to point out that this holds true only for certain applications such as commercial mainframe memories. While plated wire is being phased out of mainframe application, Edam says, it is still strong in military computer systems, and he doesn't see any serious challengers to wire in this area at present.

There are also some new applications for which wire memories are being considered, he notes. One is large bulk-storage systems. Edam notes that until semiconductor manufacturers come up with reliable, economical 8-k and 16-k chips, plated wire will give superior price/performance. He doesn't see this happening until around 1976.

Dr. Jerome Sallow, director of special programs for Memory Systems, Inc., Hawthorne, Calif., says that plated wire will also find use in control memories and in minicomputers. It can be used either as a fast RAM or as an alterable ROM for microprogramming. In the microprogramming application, Sallow notes, costs are comparable to those of pROMs, although he concedes that fixed ROMs are cheaper.

Other advantages of plated wire over pROMs include low power operation and increased reliability, Sallow says.

While most people in the industry see wire being used primarily in aerospace and military applications, because of its low power, nondestructive readout and high reliability, Sallow predicts a growing market in commercial applications as well. In the offing, he says, are wires of smaller diameter and systems that are more



Cassette tape systems, such as this Remex unit, are finding increasing use in computer storage.

Ampex's terabit memory system has a capacity of 3 × 10^{12} bits and an access time of 10 s.

compatible with integrated circuits.

Although work continues on advanced technologies that will one day replace disc and tape systems, manufacturers are still seeking improvements in these memories.

Improvements for discs and tapes

James Mordin, vice president of marketing for Caelus Memories, San Jose, Calif., notes that both the cost and speed of discs can be improved by increases in either the linear or track density and reductions in the capacitance per bit. To improve track density, the head must be made smaller and the accuracy of its positioning must be increased. The industry standard for disc systems today, Mordin says, is 100 tracks per inch; however, with improved positioning accuracy, it is possible to achieve 200 tracks per inch. To go beyond that to 400, or even 600, tracks per inch would require a different type of positioning mechanism altogether, because data reliability becomes a problem.

While it would be difficult to get to 600 tracks per inch, Mordin maintains that it is possible. To solve the positioning problem, he poses two possibilities: servoing off the written data, or servoing off prerecorded data.

John Kiernan, director of Univac's Philadelphia Research Center, also believes that better density will be achieved by improving the positioning of the head. "The next generation of devices will have increases in density resulting from absolute positioning off the actual data itself," he says.

Kiernan notes that servoing is being used on IBM's latest entry into the disc market, the IBM 3340, also known as the Winchester. The result is a track density of 300 tracks per inch.

The Winchester disc file, Kiernan says, has set a precedent for the next generation of devices by enclosing the head inside the cartridge.

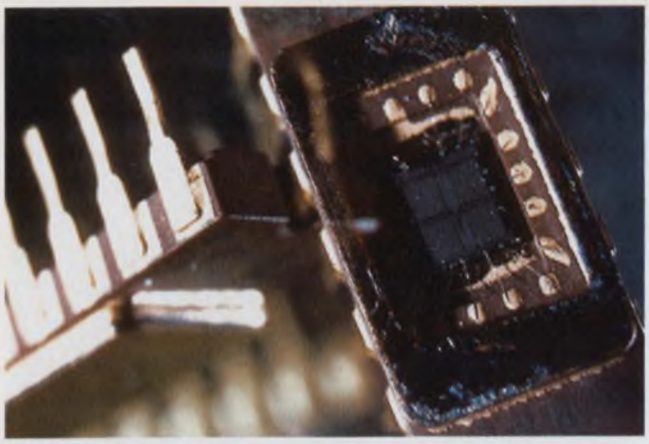
To increase linear density, he says, the heads must fly closer to the recording surface. This, however, poses another problem—surface smoothness. Higher densities require that the head-to-disc distance be less than 30 microinches. This is essentially contact recording, Kiernan notes, and thus the disc surface must be both smooth and durable. As the bit density increases, the available signal gets lower. Therefore stiffer magnetic materials—materials that will give more output per unit area—will be required.

Mordin at Caelus observes that present linear density is 2200 bits per inch and that 4400 can be achieved without too much of a problem. But if density goes much beyond that, he continues, there will be transfer-rate problems. The state of the art in transfer rates today, Mordin says, is 6.5 to 7.5 megabits.

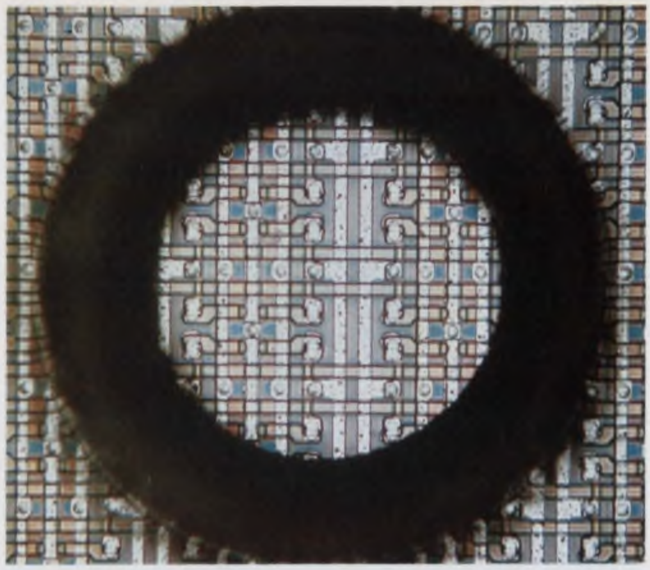
To show that discs are still a long way from reaching their maximum capabilities, Mordin notes that by using the proper coding, linear density could be increased to 10 kilobits per inch. If the disc were rotated at 3600 to 4000 rpm, he continues, the data transfer rate would equal 12 megabits. "There isn't any computer or controller around that could handle that rate," he asserts.

With all the talk about discs replacing tapes, the fact is that a significant amount of money has been invested in tape libraries. According to Kiernan, the shift away from tape will be slow.

"I can't see any big changes with respect to



MOS semiconductor memories, offering smaller size, higher reliability, lower cost and lower power dissipation are replacing ferrite cores in memory applications.



Photos courtesy of Storage Technology Corp.

tape for the foreseeable future," he says. "Magnetic tape represents highly refined technology. You can buy good-quality magnetic tape for about $10 that will store the equivalent of some of the older disc files on it. With this kind of capacity and cost and the investment many people have in large quantities of tape, they're not going to walk away from it so fast."

Recent developments in magnetic-tape systems indicate that more versatile systems are beginning to emerge. An example is Ampex's TBM (tera-bit memory) system. According to Erik Salbu, manager of Ampex's TBM System Dept. at Sunnyvale, Calif., the system uses a transverse recording technique, has a maximum capacity of 3×10^{12} bits and an access time of 10 seconds. The density for the system, Salbu notes, is 1.5 million bits per square inch—the same as IBM's new 3340 disc is offering. However, since a redundant recording scheme is used, the effective density of the Ampex system is only 750 kilobits per square inch.

The TBM can store the same amount of data normally stored on 60 IBM 3300 disc packs or on 2000 computer tape files, Salbu contends. This, he says, makes its possible to put an entire library on-line, thereby greatly increasing the security of the system.

Tape systems are not limited to open-reel systems like the TBM. Cassette and cartridge systems are now being used with minicomputers, and they may play a more significant role in the future, says Univac's Kiernan. There have not been many market applications, he admits, but isolated customers have been using them effectively. An example, he says, is the Masstape system made by Grumman—a large archival storage system that uses the cassette or cartridge for accessing reels under system control.

One of the more significant developments in cartridge systems appear to be the 3M cartridge. While slightly larger and more expensive than a cassette, it has a capacity that is four times that of a cassette and 10 times that of a floppy disc. Interest in the new device is great, and more than a dozen manufacturers are developing tape drives for it.

The promise of semiconductors

The most explosive growth area in memories today is the semiconductor. Even large core manufacturers are hedging their bets by keeping up with—and in some cases even getting into—the semiconductor memory business. An example is Electronic Memories & Magnetics, Hawthorne, Calif., which bought Semiconductor Electronic Memories, Inc., of Phoenix, Ariz.

Although semiconductor memories have been making significant inroads in the market, industry experts generally agree that they won't make a real impact until chips with a capacity of 4 k and up can be produced in quantity with reasonable speed and price. DEC's Savell sees this happening by 1974. In the meantime, he notes, "we're using 1-k RAMs in the PDP-11/45 and we're looking at 2-k chips."

According to David A. Hodges, a memory consultant and an associate professor of electrical engineering and computer sciences at the University of California at Berkeley, the characteristics of today's semiconductor memory components are ideal for any digital memory requirement from 1 bit to 10^6 bits.

Semiconductor memories have had a threefold impact on computer memories, as Hodges sees it: The cost of memory has gone down, performance has improved and the number of bits per system has increased.

Semiconductor memories from IBM are cheaper than core ever was, Hodges reports. To illustrate this Hodges notes that IBM's Model 168 computer contains 8 million bytes of semiconductor memory in the same space that the Model 165 has 3 million bytes of core memory. And the price for the two memories, he points out, is the same. Over the next decade, Hodges predicts, the cost of semiconductor memory will decrease by two orders of magnitude.

Semi memories can be subdivided into two major categories: random-access (RAMs) and read-only (ROMs). The ROMs also include programmable and reprogrammable devices. Work in RAMs and ROMs includes the fabrication of devices with both MOS and bipolar technologies.

Passive isolation techniques, such as the isoplanar and V-ATE processes, are improving memories in both of these technologies. In bipolar devices, the isolation processes are helping to reduce the required silicon chip area. In MOS devices, isolation techniques are increasing performance.

Most of the action in semiconductor RAMs is in MOS technology. The hot item that is capturing a lot of headlines is the 4-k MOS RAM. While the only such device that has made it to the market is one of Microsystems International, Ltd., of Ottawa, Canada, the industry feeling is that by mid-1974 several companies will be offering a 4-k device and that the cost per bit will approach that of the 1-k 1103 device.

At latest count, at least fourteen manufacturers were hoping to capture a portion of the 4-k RAM market: Microsystems International, Standard Microsystems, Intel, Mostek, American Micro-systems, Advanced Memory Systems, National Semiconductor, Electronic Arrays, Signetics, Motorola, Western Digital, Fairchild, Texas Instruments and Intersil.

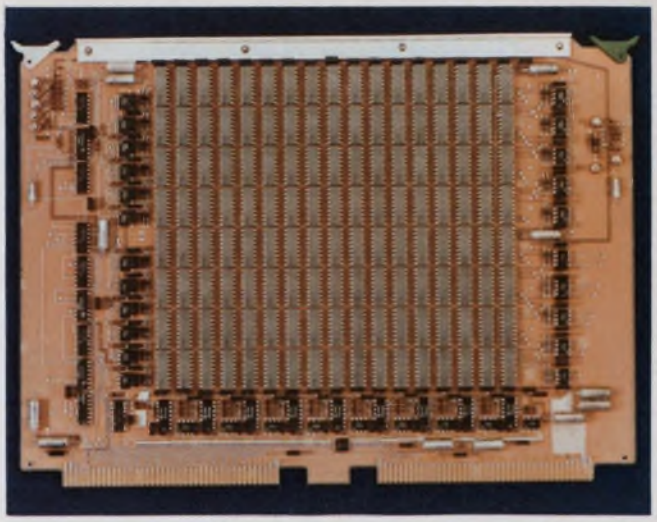
The designs are almost as varied as the number of different manufacturers, and some sort of standardization will probably be needed before the 4-k RAM has the market impact its proponents look for.

Many controversies must be settled before any standard can be agreed upon. Among these is the question of whether to use a one-transistor cell or a three-transistor cell. The single-transistor cell offers smaller geometries and thus higher density. It requires, however, a very sensitive sense amplifier. The three-transistor cell doesn't require this special amplifier, but it does need more chip real estate.

Another problem facing semiconductor memory manufacturers is whether to opt for the high performance and more complex NMOS process or stick to slower, more familiar PMOS. Industry sources indicate that NMOS has the edge.

Two other MOS technologies are being considered for the memory area: complementary MOS and silicon-on-sapphire (SOS).

CMOS devices can provide the high performance of NMOS while using low-power static configurations. Standby power for CMOS can be as low as 1 nW, while dynamic NMOS RAMs require 1 μW. But some of the drawbacks of CMOS for RAMs include the fact that it is a half to a quarter as dense as dynamic NMOS and requires a more complex manufacturing process.



Semiconductor memories for minis, like this one from Texas Instruments, increase computing power.

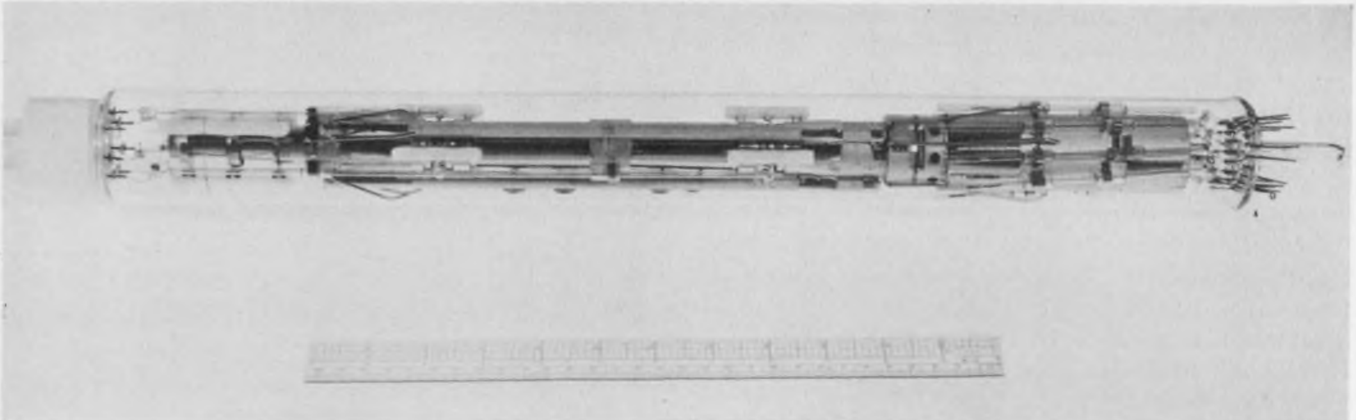
SOS memories, like the 1-k device to be introduced by Rockwell Microelectronics shortly, combine the high speed of bipolar with the low manufacturing costs of MOS. According to James A. Luisi, manager of SOS development for Rockwell, the SOS RAM will be cheaper than its bipolar equivalent and will consume 250 mW, about half the power of bipolar. It is a static device, Luisi notes, has a cycle time of 100 ns and is TTL-compatible on both the inputs and outputs.

Work on random-access memories, however, is not limited to MOS technology. Much research and development is going on in bipolar as well. The primary applications for bipolar memories are in control memories, where high speed is very desirable. And certainly, if the density can be increased and the cost lowered, bipolar memories will be a stiff competitor to MOS devices.

Both IBM and Philips are working on a high-density, static bipolar memory that uses injection-coupled logic. Preliminary results from Dr. S. K. Wiedmann, an IBM researcher in Boeblingen, West Germany, look promising. The projected specs for a 4-k RAM are a cell size of 3.1 mils^2 per bit, an access time of 50 ns, a cycle time of 100 ns and standby power of 0.1 μW per bit. A major drawback of this design, however, is that it requires 5-1/2 contacts per cell.

Wiedmann notes that by use of oxide-isolation technology, along with the injection-coupled memory, cell size can be reduced to 1 mil^2 and that it would be possible to fabricate a 16-kilobit chip on an area 175 by 175 mils^2.

In more conventional bipolar technology, Mo-



The storage tube used in Micro-Bit's beam-addressable storage system can store a million bits of data. Data are stored in a proprietary material. Information is written in and read out by an electron beam.

torola is planning to bring out an ECL RAM that will compete with Fairchild's device by the first quarter of 1974. Fairchild and Motorola are also said to be working on a 4-k ECL RAM.

Semiconductor technology has made possible the development of new forms of memories. One is the programmable read-only type. According to Larry Kessler, memory products marketing manager for Harris Semiconductor, Melbourne, Fla., the pROM is now beginning to replace random logic. In a typical situation, he explains, the Boolean equations for a printed-circuit card containing 50 to 100 gates, flip-flops and other logic devices would be written and an appropriate program would be entered in the pROM.

Logic replacement by pROMs is just becoming practical, Kessler notes, because fast pROMs are being produced. "The majority of random logic runs on a six-to-eight-gate delay," he explains. "That's between 36 and 48 ns. With a fast pROM —Harris has one that will be on the market by mid-year—the propagation delay is between 40 to 45 ns."

Commenting on reprogrammable ROMs, Kessler notes that customers are a bit nervous about them; they want to know what the danger is of their reprogramming when they shouldn't. In some cases this is a real problem, Kessler says. For example, in aircraft and space applications it is almost impossible to use a reprogrammable device with any assurance because of the X-ray and ultraviolet environment.

MNOS devices have a basic problem in that they are not TTL-compatible, says Kessler. As a result, much external support circuitry is needed, and density becomes a problem. If someone can come up with a TTL-compatible MNOS device that is also economical, he'll have a winner, Kessler says. MNOS is reliable, he reports, and it can be reprogrammed, though this is very difficult.

Ron Neale, vice president and general manager of the Read Mostly Memory Div. of Energy Conversion Devices, Troy, Mich., notes that many engineers don't realize that MNOS starts to lose information as soon as it is entered. This poses a problem, because if a device can hold information for 100 hours and there is a power failure after 99 hours, it will be able to hold the stored information for only another hour. This, Neale notes, is contrary to the general impression that MNOS storage life starts when the power fails.

While MNOS is still being developed, the amorphous read-mostly memory has two years of production and reliability experience behind it, Neale stresses.

The read-mostly memory is a bistable device whose characteristics result from an amorphous chalcogenide material that, while capable of exhibiting threshold switching, can also exhibit a reversible bistable phase change.

According to Neale, the RMM is going to have a big impact on the pROM market. One reason for that, he says, is that if you make a mistake when you program a pROM, you have to throw it away, but with the RMM you can erase it and rewrite it.

Another area being actively pursued for the RMM is as a replacement for plated wire. A feature of the RMM that makes this possible, is that it is a radiation-hardened device, Neale notes.

Besides Energy Conversion Devices, IBM is also investigating amorphous memories, according to Sol Triebwasser, IBM's assistant director of applied research.

Exotic approaches explored

Considerable research is being conducted into more exotic memory technologies, such as bubbles, charge-coupled devices and beam-addressable storage. IBM has recently announced the development of a new bubble material, an amorphous film. It is reported easier and less expensive to fabricate than the previously used crystalline films and much more versatile. For example,

A 1980 memory system: No breakthrough is needed

What will the memory system of 1980 look like? David A. Hodges, a memory consultant and associate professor of electrical engineering and computer science at the University of California, Berkeley, says no breakthrough will be required to produce the system. Its design is, in fact, conservative.

The minimum dimension for the chip is a 5-micron line—no step forward over the best practice today, Hodges says. A total of 500 chips could be fabricated into a 50-megabit memory system that would occupy about 1 cubic foot, he predicts.

If a component failure of 10^7 hours is assumed, the mean time between failure for a component in the system would be about two years. With error-correction circuitry, the MTBF could be increased to 20 years. Chances are, however, that someone would cause a failure by physical damage before 20 years, Hodges notes.

The specifications for Hodges' 1980 memory are as follows:

Chip		**50 megabit system**	
Cell: 1 transistor	0.2 mil^2	Bit density	30,000/in^3
Array (may be subdivided)	256 × 512 (128 k)	Power consumption	100 W
Chip size	250 × 250 mil^2	MTBF (component failure)	2 yr
Average power	0.2 W/chip (2 μW/bit)	MTBF with error correction	20 yr
Cycle time	200 ns	System cost to OEM	$20,000
Component MTBF	10^7 hours		(40 millicents/bit)

it can be deposited on almost any kind of surface, including flexible materials like plastics.

Another new development in bubbles was announced last month at the International Magnetics Conference in Washington, D.C.—a 1.15-megabit bubble-memory module. The development, by Bell Laboratories, is the first bubble-memory system designed for computer applications.

The concensus of industry experts is that commercial bubble memories are still five to 10 years away and that the first applications will be as replacements for fixed-head storage systems.

Univac's Kiernan notes that when the bubble size gets down and the density increases, it might be feasible to perform logic with bubbles. At present, however, the bubbles are generally not fast enough to do logic, he declares.

Charge-coupled devices are being investigated by most semiconductor manufacturers, but the general feeling is that they will find their major application in imaging, not in memory. There are, however, several manufacturers investigating memory applications, including Rockwell Microelectronics, Texas Instruments, RCA and Intel.

The main application for bubble and CCD memories, says Energy Conversion's Neale, will be in memories ranging from 10^6 to 10^{10} bits.

The Micro-Bit Corp. of Lexington, Mass., has designed a beam-addressable storage system. Such systems are not new. A number have been proposed in the past, including those that use laser beams or electron beams. The Micro-Bit system is an electron-beam type.

According to Robert White, a member of the company's professional staff, the first system—to be announced later this year—will have a capacity of 10^7 bits and subsequent systems may go as high as 10^{10} bits. The system is block-oriented, White explains, and access to a block of data will require between 5 and 10 μs. Once the block is accessed, he goes on, data can be read out at a 1 to 2-megabyte rate.

The Micro-Bit system is composed of several electron-beam addressable memory tubes, each capable of storing one million bits of data. Each tube is about 1.5 inches in diameter and uses proprietary materials for storage.

The cost of the storage system will be about 0.01 cent per bit initially, and this will drop eventually to 0.005 cent, White says. He sees initial applications as disc and drum replacements. Ultimately, he says, the system will be used in extended memory.

Another approach to beam-addressable storage systems has been taken by the Precision Instrument Co. of Palo Alto, Calif., in its Unicon mass-memory system. This system, being used with the ILLIAC IV computer, consists of a metallized Mylar tape in which holes are punched by a laser. Up to 10^{12} bits can be stored this way. Random access to the 10^{12} bits requires only 10 seconds.

Data are read out when light is reflected off the surface of the tape. A possible disadvantage of the Unicon system is that it is a read only type of memory. If the data must be altered, a new tape must be punched. ■■

Rectifier Product Matrix

RCA Rectifiers	DO-1 						DO-26 				
I_O	0.125A	0.75A	0.75A	1A	1A	2A	0.5A Ava-lanche	0.75A	0.75A Insulated	1A	1A Insulated
I_{FSM}	30A	15A	15A	35A	35A	35A	35A				
$V_{RRM(V)}$ 50			1N536		1N2858A						
100	1N3754	1N4408	1N537		1N2859A	40266					
200	1N3755	1N4418	1N538		1N2860A	40267		1N3193	1N3253	1N5211	1N5215
300		1N4428	1N539		1N2861A						
400	1N3756	1N4438	1N540	1N1763A	1N2862A			1N3194	1N3254	1N5212	1N5216
500		1N4448	1N1095	1N1764A	1N2863A						
600		1N4458	1N547		1N2864A		40808	1N3195	1N3255	1N5213	1N5217
800							40809	1N3196	1N3256	1N5214	1N5218
1000									1N3563		

RCA Rectifiers	DO-15		DO-4 				DO-5 	
I_O	1A	1.5A	5A	6A	10A	12A	20A	40A
I_{FSM}	30A	50A		160A	140A	240A	350A	800A
$V_{RRM(V)}$ 50	44001	1N5391	1N1612	1N1341B	40108	1N1199A	1N248C	1N1183A
100	44002	1N5392	1N1613	1N1342B	40109	1N1200A	1N249C	1N1184A
200	44003	1N5393	1N1614	1N1344B	40110	1N1202A	1N250C	1N1186A
300		1N5394		1N1345B	40111	1N1203A	1N1195A	1N1187A
400	44004	1N5395	1N1615	1N1346B	40112	1N1204A	1N1196A	1N1188A
500		1N5396		1N1347B	40113	1N1205A	1N1197A	1N1189A
600	44005	1N5397	1N1616	1N1348B	40114	1N1206A	1N1198A	1N1190A
800	44006	1N5398			40115			
1000	44007	1N5399						

Fast Recovery Types

RCA Rectifiers	DO-26 	DO-15 	DO-4 		DO-5 	
I_O	1A		6A	12A	20A	40A
I_{FSM}	35A		125A	250A	300A	700A
$V_{RRM(V)}$ 50		44933	43879	43889	43899	40956
100		44934	43880	43890	43900	40957
200	TA7892	44935	43881	43891	43901	40958
300			43982	43892	43902	
400	TA7893	44936	43983	43893	43903	40959
500						
600	TA7894	44937	43984	43894	43904	40960
800	TA7895					
1000						
Reverse Recovery Time trr						
Typ.	200 ns	200 ns	200 ns	200 ns	200 ns	200 ns
Max.	500 ns	250 ns	350 ns	350 ns	350 ns	350 ns

Microprocessors finding between calculator chips

Edward A. Torrero, Associate Editor

A growing number of microprocessor chips are filling the gap between calculator chips and minicomputers. The new chips are emerging in applications that require decentralized cheaper minis as remote, programmable controllers.

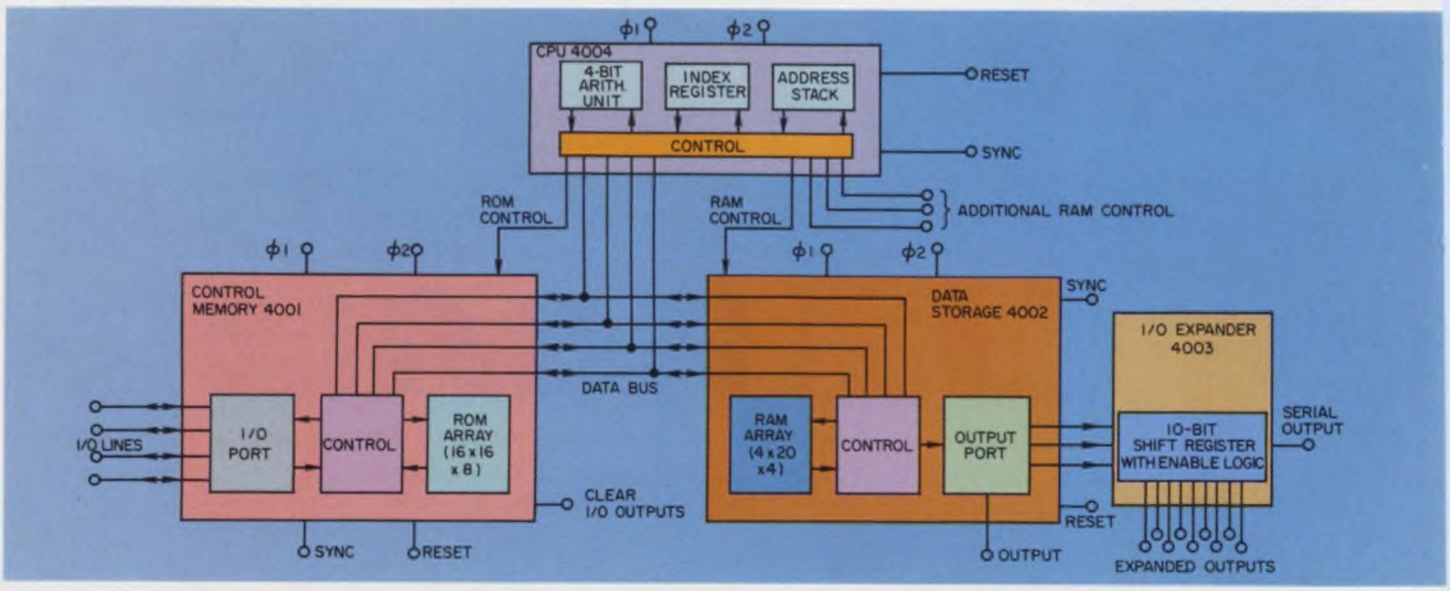
Like the calculator chips from which many of those MOS/LSI processors evolved microprocessors can be programmed to perform arithmetic functions—as in point-to-sale terminals, a leading application area for the processors. But unlike calculators, microprocessors can perform data processing as well: Inventory control, price lookup and credit authorization are some of the additional functions being handled by microprocessors for point-of-sales.

Other uses run the gamut from traffic-control systems to small accounting systems, and from computer terminals to industrial process controllers. In some cases a microprocessor system has replaced a small, dedicated minicomputer.

No processor manufacturer, however, is pushing microprocessors as replacements for minicomputers, especially general-purpose types. Although a few companies are introducing minis built around the LSI chips, the MOS microprocessors operate at speeds that are about an order of magnitude slower than minicomputers with bipolar circuits. And no processor manufacturer can compete with the mini makers when it comes to software backup.

According to Gene Carter, product marketing manager at National Semiconductor, microprocessors are aimed for applications now using hard-wired, or permanent, logic. These are generally inflexible and costly in-house-developed systems. In only about 10% of all cases does Carter see microprocessors replacing minis. And for these, the mini is probably being underutilized, he says.

Henry Smith, manager of minicomputer systems at Intel, believes microprocessors show their



growing role and minis

greatest potential in areas where cost precludes the use of a mini. A basic processor system can be purchased for less than $100. But most minis start at more than a few thousand dollars.

Moreover most microprocessors are being aimed at OEMs rather than the end-users that minicomputers serve. The reason for this, most manufacturers say, is that the market for dedicated processors for custom and random logic is much larger than the market for general-purpose minis.

However, minis and processors can be used together. Michel Ebertin, director of business-machines development at Rockwell Microelectronics, notes that several relatively slow microprocessors—like point-of-sales terminals—can be hooked up to a faster, back-room minicomputer. The mini can process data generated at the terminals and provide main memory storage.

The microprocessors available generally have a parallel organization, like minicomputers. Parallel processors currently handle four, eight and 16 bits, and they can have variable word-length capability for larger words. Typical execution times are as high as 5 μs for four-bit machines.

Among the microprocessors available or expected shortly, the eight-bit word length seems to be the most common. One major reason: Most data-transmission systems operate with words of eight bits or less.

Where control of decision functions outweighs arithmetic operations, the necessary functions generally require the longer word length to allow the handling of standard codes, such as ASCII and EBDIC. The use of standard codes simplifies the interface with text-oriented equipment, like teletypewriters or the more common type of computers.

Microprocessors with words of more than eight bits are available for greater instruction-set power and processor flexibility. However, manufacturers offering smaller word-length machines claim many of the same features can be obtained through the use of the push-down stacks in their machines or latches in the external circuitry.

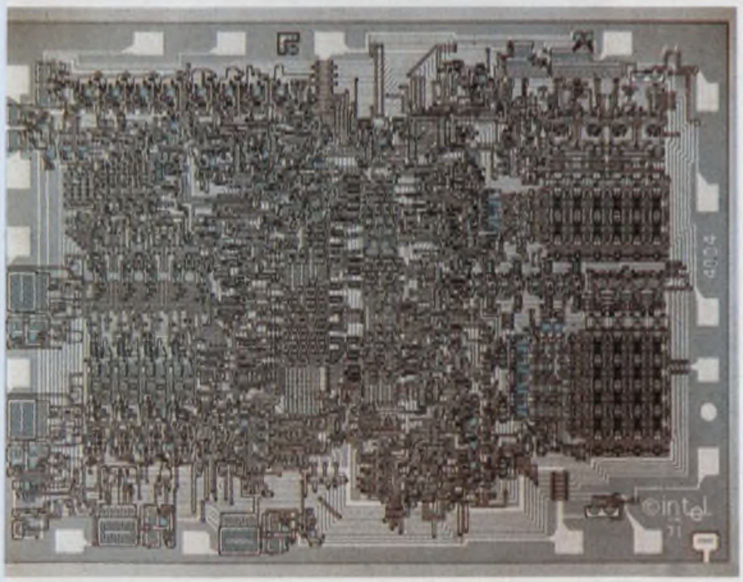
The use of parallel processing, rather than serial operation, provides increased speed by providing multiparallel paths on a data bus for the transfer of data through the system. Fetch and execute cycles, for example, can be performed faster, and the ability to jump from one part of the memory to another is less limited.

In most cases standard p-channel technology is being used to fabricate microprocessors. But for the next generation, the trend could be toward n-channel. By year's end several n-channel processors are expected, with faster execution times and more powerful instruction-set repertoires.

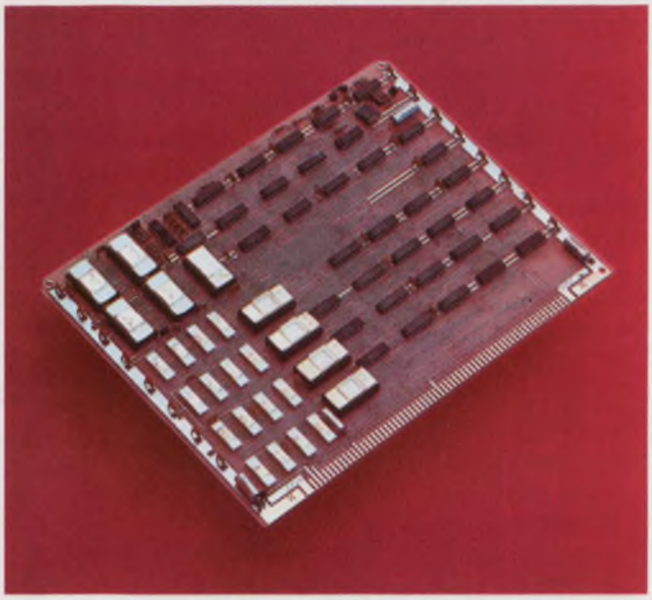
Fixed instruction vs microprogram

The use of microprocessors requires some programming skill. This could emerge as the dominant factor in wide acceptance of the processors, since random-logic designers seeking to upgrade or customize their systems with them must now grapple with the relatively unfamiliar demands of software. Furthermore the designer must choose between a fixed-instruction machine or a microprogrammable one. It's a familiar controversy in computer circles; many of the same arguments were brought out years ago as microprogrammable computers developed.

In a fixed-instruction machine internal instruc-



Intel's MCS-4 system (far left) consists of a four-bit parallel processor chip (left), control ROM, data-storing RAM and I/O expander. The system can perform decimal and binary arithmetic with a basic instruction cycle of 10.8 μs. Two 8-digit numbers can be added in 850 μs. The instruction set includes conditional branching, jump to subroutine and indirect fetching.



National Semiconductor offers a 16-bit microprocessor on a card, the IMP-16C. Included on the card: clock system, I/O bus drivers, 256 words of RAM and provision for 512 words of ROM or pROM. The card has one control ROM that stores the microprogram and provides the logic for four 4-bit register-and-arithmetic-logic units.

tions, or microinstructions, are set by the manufacturer. Accordingly the user must develop software for an application around the instruction-set repertoire. In a microprogrammable machine the internal instructions must be programmed, with the degree of software difficulty depending in part on the complexity of the microprocessor architecture.

For George Reyling, senior project engineer at National Semiconductor—which has the only available fully microprogrammable processor—the microprogramming approach offers a speed advantage, since microinstructions are executed considerably faster than macroinstructions, or external instructions. Microprogramming also offers a more detailed level of control, he says, and this can often be used to reduce hardware by allowing more functions to be controlled by the program.

John Reed of American Micro-systems says the major advantage of microprogramming is that instructions can be tailored to specific requirements. Memory savings are evident, he notes, since some, or all, of the external memory can be eliminated by use of microfirmware, or memory internal to a processor chip.

Both Reed and Reyling agree with Smith of Intel that microprogramming is far more difficult to implement. According to Smith, it calls for a microprogrammer to deal with the specific timing relationships of the processor architecture. And since each application requires a separate microprogram, each has its own instruction set that is generally not transferable to another application.

Smith concedes, however, that with fixed-instruction machines considerable software backup is essential to cover the widely varying applications. With it, Smith believes, only about 5% of the dedicated-processor applications require microprogrammable systems.

Intel probably is offering the largest software package with its microprocessors. The company first introduced these devices in 1971, and it has benefited from this one-to-two year lead over competitors. It is generally regarded as the current leader in microprocessors. And Microsystems International of Canada is alternate-sourcing at least part of the Intel line. Other manufacturers of microprocessors are Fairchild, National Semiconductor and Rockwell Microelectronics. By the end of the year, AMI, Signetics and Western Digital are expected to join the field.

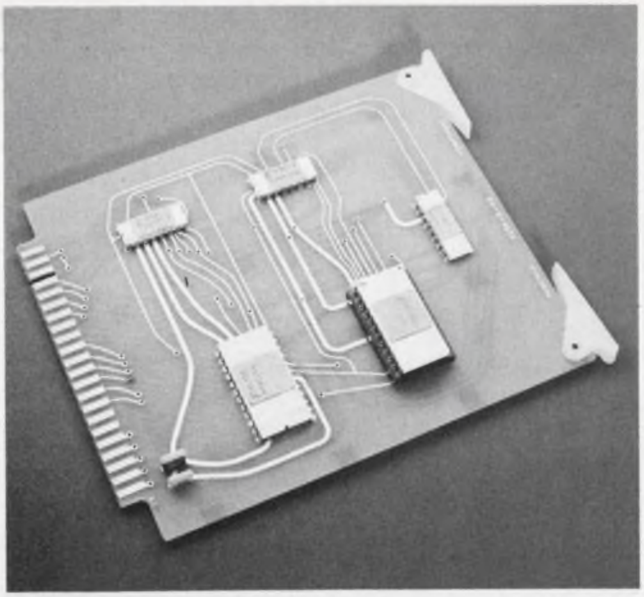
The Intel microprocessors

Intel offers two parallel-processor systems: the four-bit MCS-4 for decimal and binary arithmetic, and the eight-bit MCS-8 for binary arithmetic and logic.

The MCS-4 consists of four basic chips: the processor (4004) with a 45 instruction-set repertoire, a 256-by-8-bit ROM (4001) for control, a 320-bit RAM (4002) for data storage and a 10-bit shift register (4003) for I/O output-line expansion. A single processor can drive up to 16 ROMs for a total storage capacity of 4096 by 8 bits, as well as 16 RAMs for a total of 5120 bits of data. One processor and one ROM—the minimum system—are priced at less than $50 in quantity.

Instructions are executed in either 10.8 μs—eight cycles of a 750-MHz clock—or 21.6 μs—corresponding to 16 cycles. In a typical eight-cycle sequence, the processor fetches data by sending 12 bits of address (in three four-bit bytes on the data bus) to the ROMs in the first three cycles. This address selects a single word from one ROM, which then sends back eight bits of instruction in the next two cycles. The instruction, sent over a four-line data bus in two four-bit bytes, is then interpreted and executed in the final three cycles.

The MCS-8, which requires five timing cycles for one-word instructions, has the 8008 processor with about the same number of instructions as that of the MCS-4 and a typical execution time of 20-μs. However, it also has six eight-bit general-purpose registers, seven-level nesting of subroutines and interrupt capability. Moreover it can operate in an asynchronous mode with the memories, has TTL-compatible inputs and can drive up to 16,000-by-8-bit words of ROM, RAM or shift registers. The minimum system consists



Fairchild's PPS-25 system uses a four-bit parallel processor that responds to 95 instructions, of which 63 can be assigned for I/O control. Interfacing with keyboards and displays is done with standard ICs. The operation time on a register of 16 characters is 62.5 μs. Two groups of 16-digits can be added in 125 μs.

of the processor, one standard ROM and 20 standard TTL circuits. For faster execution times, the 8008-1 offers a typical cycle time of 12.5 μs.

The design support offered by Intel includes a prototyping board that forms an operational processor with erasable pROMs instead of mask-programmable ROMs. The standard board for the MCS-4 can hold up to 8000 bits of pROM and 1280 bits of RAM. In addition FORTRAN IV assemblers and simulators for the MCS-4 enable designers to use any general-purpose computer to develop the processor program and to simulate the microprocessor prior to mask-programming of the ROMs.

For the MCS-8, a bootstrap loader consisting of three pROMs permits data to enter the RAMs from a teletypewriter paper tape or keyboard. The MCS-8 prototyping board holds up to 16,000 bits of pROM and 8000 bits of RAM. And various test programs are available on pROMs that plug into the prototyping board. For both systems, Intel offers a library of programs, which have been contributed by and are free to users.

The PPS-25 for scientific calculators

For arithmetic operations, Intel's MCS-4 generally isn't as fast as Fairchild's four-bit processor. Intended for scientific calculators, control systems and peripheral systems, the Fairchild processor features overlapping instructions for faster numerical calculations.

In the Fairchild system—called the PPS-25—the 3805 arithmetic unit and the 3806 function and timing unit perform all the timing, control and arithmetic functions. The 3810 ROM stores microprograms and data lookup tables. while the 3808/3809 registers provide data storage.

The PPS-25 requires at least one 3810 ROM, which can store 256 program steps, each 12 bits wide. However, up to 26 ROMs can be used for a total read-only memory storage of 6656 words. Similarly up to seven 25-digit registers can be implemented for total data storage of 700 bits of BCD as well as hexadecimal data.

The 3805 and 3806 form a four-bit parallel processing section with a 95-instruction set. The system is organized in 25-digit serial, four-bit parallel format and features a 62.5-μs word time and 2.5-μs bit time, corresponding to a maximum clock rate of 400 kHz (two phase).

The instructions for fetch, data access and operation are overlapping. Hence operations involving data manipulation can be executed in one cycle, independent of the number of bits, or characters. The arithmetic unit, for example, can operate on one group of 25 digits in a single 62.5-μs cycle. Similarly data characters can be transferred directly from the ROM to a data register in one instruction.

Input/output requirements for keyboards and displays can be met with the 3803/3807 keyboard encoder and the 3811 display driver. The 3803/3807 permits direct interfacing with up to 62 key switches and 32-mode switches. The 3811 provides decoded data for displays having up to 16 digits. In the 95-instruction set, 63 I/O commands can be assigned for control.

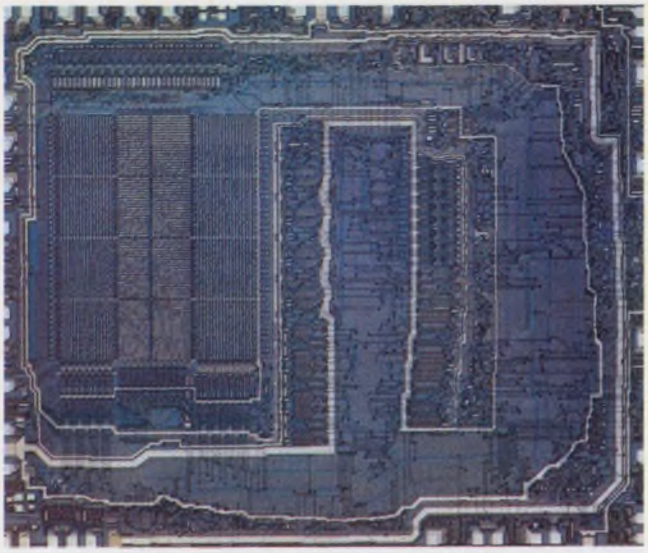
As part of the function and timing chip, two 25-bit status registers can be used to store 25 flags under program control. When the 3803/3807 keyboard encoder is used, the status of 16-mode switches can be stored eight at a time in eight discrete flag bits for each register. And two return addresses for subroutine calls can be stored for each register, for a total of four levels of subroutine testing.

Other features of the PPS-25 system include the following: two and three-way branching; immediate or delayed program-address modification under external control; and conditional external interrupt from a single input line.

As an introductory kit, Fairchild offers the 3025A. The six-part kit allows designs as complex as a 12-digit, one-memory calculator.

The IMP-16C—a microprogrammable system

National Semiconductor's microprocessor system, the IMP-16C is a 16-bit microprogrammable parallel processor on an 8-1/2-by-11-inch PC board. It consists of the processor, clock system, I/O bus drivers, 256 words of RAM and provisions for 512 words of ROM or pROM memory. The IMP-16C uses a standard set of 42 micro-



American Micro-systems' proposed 7200 system consists of a three-chip central processor, including this micro-control chip. Another chip provides registers and an ALU, and the third—a microinstruction chip—contains the microprogram in a 512-word-by-24-bit ROM. All three ICs are ion-implanted, p-channel devices.

instructions, operates on a microcycle of 1.5 μs and can address up to 65,536 words of memory. The single-quantity price is $1380.

The IMP-16C is built with National's GPC/P (general-purpose controller/processor) family of LSI chips. The microprocessor part of the family consists of a register and arithmetic-logic unit (RALU) and a control and read-only memory (CROM). The RALU provides seven general-purpose registers and a 16-word stack. The CROM provides storage for a microprogram and the control logic for up to eight RALUs. The RALU is a four-bit slice, and four are used in the IMP-16C.

The 16-word stack in the RALU, a last-in/first-out or pushdown stack, permits re-entrant subroutine and program interrupt control by preserving the status of the program. The stack becomes essential when the control program is in the ROM and no read/write memory is available to store return addresses.

Between the RALU and the CROM, four different commands are multiplexed over a command bus in each clock cycle. The first two commands specify an operand on the two RALU busses. The third specifies the ALU operation to be performed, and the fourth command specifies the register to be loaded with the result. The RALU uses four nonoverlapping MOS clocks and comes in a 24-pin package, as does the CROM.

The control ROM provides storage for 100 23-bit microinstructions—sufficient to provide a complete internal control program or to implement a macroinstruction set comparable to that of most minicomputers. A typical macroinstruction cycle requires 7 μs.

External to the CROM, a conditional jump multiplexer provides ROM address control, or branching within the microprogram. Branching may be performed on up to 16 or more internal and external conditions. Also external are a group of 16 flag flip-flops, which are controlled by the microprogram.

National also plans to introduce microprocessor boards of larger and smaller capacities, using the four-bit RALU slice to achieve the various word lengths. And the company will offer a complete system consisting of the IMP-16C, a chassis, power supply, console and enclosure.

Fastest four-bit processor: Rockwell's 10660

Among four-bit parallel processors, the fastest is Rockwell Microelectronic's 10660, with an instruction cycle of 5 μs and register-to-register add time of 2.5 μs.

The processor responds to a basic set of 50 instructions and constitutes the basic element in Rockwell's parallel processor system. In addition to the processor, the system generally consists of at least one 1024-by-8-bit ROM (PN A05), one 256-by-4-bit RAM (PN 10432) and an I/O buffer (PN 10696). In quantities of 1000, unit costs are $22 for the 10660, $22 for the ROM, $17 for the RAM and $12 for the buffer.

Up to 16 ROMs and up to 32 RAMs can be handled by the processor through time-shared multiplexing techniques. And up to 16 I/O chips, each with a capacity of 12 input and 12 output lines, can be used with a single 10660 processor for a total of 192 possible inputs and outputs. For smaller applications, Rockwell also offers the PN A08 ROM/RAM combination chip, which includes a 704-by-8-bit ROM and 76-by-4-bit RAM.

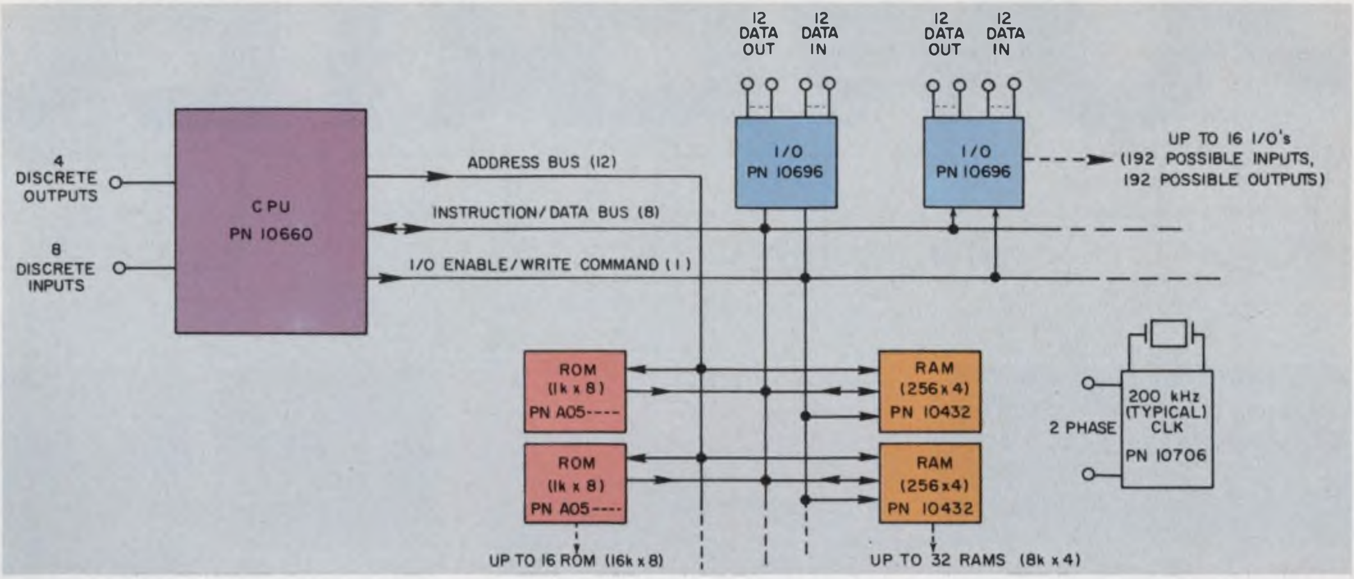
To complete the system, a 200-kHz clock is required. It is offered in a 10-lead TO-100 can. All other chips come in 42-lead flat packs.

The clock generator provides the processor with two synchronized signals. The processor logically divides the signals into four phases, so that internal signals are handled at four times the rate of the external clock.

The parallel-processor-system bus lines transfer data during the second and fourth time interval. In the alternate intervals, the address and data bus lines are automatically cleared to zero. This interface timing scheme permits up to 30 parallel-processor-system devices to share the bus without additional buffering or drive circuitry.

The control logic within the processor allows arithmetic or logic instructions to be carried out in one cycle time. Adding two decimal digits requires six instructions, or six cycle times. Hence for a 5-μs cycle time, two decimal digits can be added or subtracted in 30 μs.

Subroutine nesting uses RAM storage instead



Rockwell Microelectronics' parallel-processing system uses the 10660 central processor, which has a basic instruction cycle of only 5 μs and a 50-instruction set repertoire. Data can be handled internally at four times the rate of the external clock; the processor divides the two-phase clock signal into four phases. Because of time-shared multiplexing techniques, the system may be expanded to include up to 16 ROMs and 32 RAMS. And since subroutine nesting uses RAM storage, a large number of nesting levels is possible.

of the more common push-down register. As a result, the number of nesting levels are limited only by the available RAM storage. Microprocessors using a push-down stack generally have only three or four levels of nesting.

Rockwell also offers an evaluation board for $500 that contains the processor, two RAMs, two I/Os and a clock. The board can be used to set up a basic microprocessor system. In addition assembly and simulator software are expected in FORTRAN on the Tymshare networks.

Next generation of microprocessors

Expected from American Micro-systems is the 7200 three-chip processor. A microprogrammable system, the three chips consist of a microcontroller, microinstruction ROM and a register and ALU chip. The microinstruction ROM can handle 512-by-24-bit words, and a complete 7200 system can operate as an eight-bit or 16-bit parallel machine.

Internally instructions are processed in two 12-bit segments, the first specifying registers to access while the second gives the destination and ALU operation. The last 12 bits of one instruction can be processed while the next 12 are being decoded, for an increase in internal execution speed. The processing time reportedly approaches that of slower bipolar machines.

The 7200 system also features a 32-register push-down stack for program interrupts and subroutines. The stack permits fast subroutine calls executed at microinstruction speeds rather than memory cycle speeds.

The inherent speed advantages of the 7200 are shown in this example provided by American Micro-systems. The contents of a display memory of 2000 characters is to be searched. Each character is to be replaced with an eight-digit character if its MSB is one. The processor signifies completion through a peripheral status register. With the 7200, the problem can be completed in 15 microsteps for a loop execution time of 9 μs (at 600 ns per microstep) and a total problem execution time of only 18 ms.

Speed advantages are also expected this year from NMOS microprocessors. Signetics, Western Digital and Intel have indicated plans for such devices.

Joe Kroeger, MOS applications manager at Signetics, says his company will introduce an eight-bit, fixed-instruction parallel processor with a maximum instruction cycle of 10 μs. The processor, he says, will have capability for indirect and relative addressing, as well as absolute and immediate addressing. The new processor will have in excess of 64 instructions.

From Intel, the 8080 NMOS microprocessor is expected—an eight-bit parallel processor with a 78-instruction set repertoire, including some instructions for double precision. The 8080, the company says, will be able to address 65-k bytes of external memory and have an instruction cycle of 2 μs.

And from Western Digital, William Roberts, vice president of research and development, indicates that his company's NMOS microprocessor —an eight-bit parallel processor—will be comparable in performance to minicomputers. ■■

Proliferous peripherals: fast, slow, versatile and

David N. Kaye, Senior Western Editor

Printers are becoming faster and cheaper. Plotters also are going faster, but paper-tape readers slower. Terminals are getting smarter. Reading capability is being incorporated into card punches.

The world of computer peripherals is dynamic and responsive to the needs of its many markets. And printers and terminals are among the most dynamic devices in this expanding world of peripherals. Present printers put out data at rates ranging from 10 characters per second to 2000 lines per minute.

At the low end of the range—10 cps—is the old, standard teleprinter from the Teletype Corp., Skokie, Ill. At the high end—2000 lpm—is the new 3211 from IBM, Endicott, N.Y. Most activity in printers falls in the speed range of 30 cps to 300 lpm and is aimed primarily at the minicomputer market.

Up to about 100 lpm, most printers use serial printing—that is, they print one character at a time. Sometimes the printing is done by impacting the character against the paper through an inked ribbon; at other times it is of a nonimpact variety.

Nonimpact printing takes on many different forms, the most popular being thermal, electrostatic, electrosensitive and photographic. In each case a special type of paper must be used. In addition the characters are usually formed by a matrix of print elements, and, as a result, the visual quality is not as good as the formed characters used in most impact printers. An additional limitation of the nonimpact printers is that

A variety of peripheral equipment is used in this dual-processor system from Data General. Included in the system are two Nova 1200 computers, three on-line disc memories, four tape drive units, a multiple tape cassette drive, a combination paper-tape reader and punch and a CRT terminal.

They come with 'brains'

usually they make only single copies. Impact printers can make five or six copies.

But nonimpact printers have several things going for them: They are much more quiet than impact printers and therefore good in an office. They are usually less expensive, and they go faster than impact printers in the same price range.

Among the more interesting nonimpact, low-speed printers are units from Texas Instruments in Houston, Teletype, Anderson-Jacobson in Sunnyvale, Calif., National Cash Register in Middletown, Ohio, Elec-trol, Saugus, Calif., and Scope Data, Orlando, Fla. The Model PR1011 from Elec-trol is the most unique.

It uses electrosensitive printing in which an 80-V pulse of energy burns away the top coating of a two-layer paper to expose a dark lower layer. A roll of paper 2.75 inches wide accommodates an 80-column-by-16-line message at 100 cps. The characters are rotated 90 degrees by the printer, and 16 rows of characters (lying on their sides) are printed. After the printer writes 80 lines of these characters, the paper is torn out of the printer and turned on its side. This printer is ideal for printing messages off CRT displays.

Tektronix' 4023 Computer Display Terminal and 4632 Hard Copy Unit provide a low-cost terminal system with upper and lower-case characters and format control.

Of the companies pursuing the low-speed, serial-impact printer market, three have been notably successful: Teletype, Diablo Systems of Hayward, Calif., and the Centronics Data Computer Corp. of Hudson, N.H.

Teletype, which has been big in the 10 and 30-cps markets, plans to introduce a 120-cps, full-character printer at the National Computer Conference next month. Diablo has gone after the 30-cps business with a printer that uses a spinning, plastic, daisy shaped disc. Each petal of the daisy contains a single character. Centronics is king of the fast serial-impact printers, and two are having a major impact in the minicomputer market. The first is a 165-cps, 132-column, dot-matrix printer that sells for just over $4000. The second is the newly introduced Model 306, a 100-cps, 80 column, dot-matrix printer for $1995.

"There is a tremendous need for an impact printer at 100 to 150 cps selling for under $2000," concedes Daniel M. Printz, marketing manager of Teletype. Accordingly, look for Teletype and others to join Centronics at this level.

Hybrids: From 100 to 300 lpm

From 100 to 300 lpm, the waters get a bit muddied. Hybrid printers cover much of this range with serial technology and multiple-print heads. As the number of print heads reaches 25% to 50% of the number of columns being printed, the printer is considered a line printer.

Irving L. Wieselman, vice president of product development of the Data Products Corp. in Woodland Hills, Calif., believes that the characteristics of serial printers and line printers will approach each other to serve the minicomputer market efficiently. He calls these printers "somewhat-serial line printers."

Centronics has demonstrated the capability of redesigning a serial printer to get a somewhat-serial line printer. It added a second print head to the 165-cps printer to achieve 330 cps, or 120 lpm. An experimental model has also been built with four print heads; its rate is 660 cps, or 240 lpm.

Several other companies have moved from a line printer to a somewhat-serial line printer. IBM shares its hammers on the 5203 printer by moving them to four positions while printing with a character chain. The hammers are mounted on flex-pivots, and the mechanism is driven by a cam to achieve printing speeds of 100, 200 or 300 lpm. Control Data Corp. in Rochester, Mich., moves the paper, instead of the hammers, to three positions in the 200-lpm 9322 drum printer. Pertec, in its new P7330, a 300-lpm printer, uses hammers that are as wide as two columns. The hammers impact twice per line, hitting first the odd and then the even characters. In this printer an etched steel band with characters is used instead of the more conventional chains, trains or drums. Data Products, in its 2230, a 300-lpm drum printer, moves the hammer bank to two positions by using flex-pivots and a voice-coil, servo-controlled positioner.

Joel Herbst, manager of Pertec's printer group in Chatsworth, Calif., says: "The trend in low-cost line printers will be to go a little bit faster but a lot lower in price." The Pertec printer is already the least expensive 300-lpm printer at about $4000.

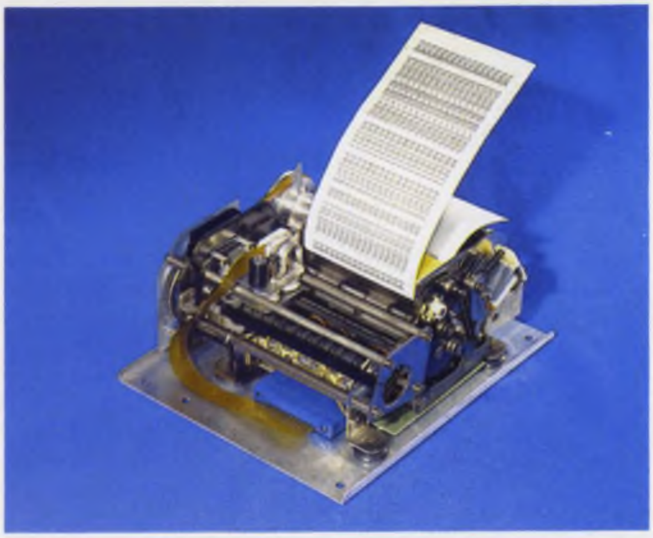
Wieselman of Data Products notes: "The use of shared components will continue in low-to-medium-speed printer designs. As higher-speed electromechanical components become available, the speed of the somewhat-serial line printers will increase, and the costs for the lower-speed printers will be reduced. Servo techniques will become more widely used in more designs. The digital control portion of the printer will take advantage of larger-scale integration, and hence the digital control will only require a few chips."

Other printers at the 300-lpm level are straight-hammer, per-column-line printers. However, none competes in price with the somewhat-serial line printers.

Up, up, up in speed

As the fastest line printer today, the IBM 3211 must be considered the leader in technology. It operates at 2000 lpm and uses a rather unique mechanism. Printing is caused by impacting the characters with hammers, which in turn causes the character to impact the ribbon and paper. This is somewhat similar to the way a conventional typewriter works. In most other line printers the paper is between the hammer and the ribbon with the character on the far side of the ribbon. Then the hammer strikes the paper and pushes it against the ribbon and the character. The speed in the IBM printer results from the use of servo-controlled motors to drive the paper and from a new character-scanning mechanism that employs characters mounted on bars. The bars are attached to a character train slug by pivots.

A prototype version of another new approach to high-speed printing was demonstrated by Data Products at the 1972 Fall Joint Computer Conference in Anaheim, Calif. It is called the Charaband printer. Wieselman describes it this way: "A character band is mounted on a roller-bearing roadbed that carries character print slugs. The band is an endless loop. Each slug has enough mass so that, when impacted by a hammer, a clean impression can be made on the paper."



Called the Sidewriter by Elec-trol, this 100-cps printer uses electrosensitive paper to give an 80-column-by-16-line printout.

Wieselman notes that the Charaband approach eliminates the wear and need for lubrication inherent with train printers and will be capable of speeds in excess of 1500 lpm.

Most unusual of the new high-speed printers on the horizon is one from the Electroprint Corp. of Cupertino, Calif. According to James Sutherland, general manager of the company's Computer Products Div.: "Our printer will go 8000 lpm. It is a nonimpact printer that uses an ion beam focused through a cloud of ink particles, to drive the ink to the paper, instead of a mechanical hammer and ribbon. The printer will sell in the $100,000 category and will be available around the end of 1973."

Joint printing and plotting offered

A class of hard-copy computer output devices that is gaining popularity is the nonimpact, electrostatic printer-plotter, which uses paper coated with a dielectric material. A linear array of conducting styluses is raster-scanned across the paper. The styluses are activated by digital input data, so that wherever they are activated, dots of charge are left on the paper. These dots form the desired image. The paper is then passed through a liquid toner suspension of charged particles of carbon. The toner particles adhere to the paper wherever a charge exists, resulting in a permanent, high-contrast image on the paper. With dyes in the toner, it is possible to do printing in any color.

Most of the units on the market have paper speeds of 1 to 2 in/s. The highest-speed unit moves the paper at 10 in/s. Paper widths are available in various models up to 20 in. Resolution of up to 100 dots/in. is available. The typical plotting accuracy of these units is 0.3%, absolute, with 0.1% repeatability. Most units sell at $7000 to $8000. As printers, they are capable of 1000 to 5000 lpm.

Major manufacturers of electrostatic printer-plotters include Gould in Cleveland, Varian Data Machines, Palo Alto, Calif., and Versatec, Cupertino, Calif.

Sherman Rutherford, manager of engineering at Varian, sees these trends "for the near-term future" for electrostatic printer-plotters: "Paper widths will go wider. Paper costs will come down. A multiple copy capability will be developed. New software will be developed to make the machines move efficiently, and the machines will get smaller. Desk-top models will become common."

Most of these machines are sold with integral controllers for interfacing with a particular computer.

Faster plotters turning up

Plotters, too, are stepping up their speeds. A flatbed type just introduced by Xynetics of Canoga Park, Calif., lays claim to a new record—a maximum pen speed of 60 in/s. The old record, also set by Xynetics, was 42 in/s. The new plotter uses a two-axis linear motor to achieve its speed, along with an accuracy of ±0.005 in. and a repeatability of ±0.001 in.

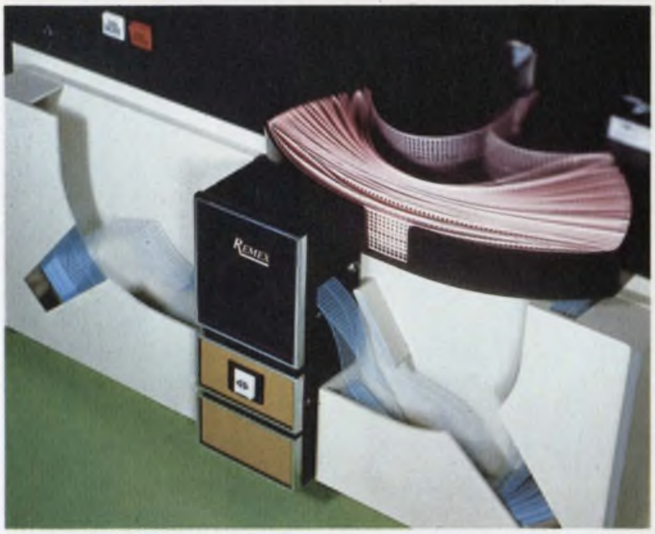
James L. Pyle, assistant to the president of California Computer Products in Anaheim, Calif., notes: "Most flatbed plotters range in size from 30 by 30 in. to 6 by 24 ft. They range in speed from 3 in/s to 60 in/s and have a resolution of as good as ±0.001 in. and a repeatability of up to ±0.003 in."

Pyle notes that flatbed plotters can also plot on a variety of media, including paper, plastics, foil and film.

The other major class of plotter is the drum. On a drum plotter the paper is on a continuous roll 12 to 36 in. wide. The paper moves under a pen to create one axis of motion, and the pen moves back and forth in a direction that is orthogonal to the paper movement, to form the other axis of motion.

Pyle says that the range of speeds for drum plotters is 3 in/s to 10 in/s. Resolution ranges from ±0.01 in. to ±0.001. Repeatibility is better than ±0.003 in.

California Computer Products is the only major manufacturer of drum plotters in this country. Major manufacturers of flatbed plotters include the same company, Xynetics, Gerber Scientific Instruments in Windsor, Conn., Electronics Associates, Inc., West Long Branch, N. J., and Hewlett-Packard, San Diego.



With a fully asynchronous 300-cps reader and a fully asynchronous 75-cps paper-tape punch in the same box, the RAF 6375 from Remex hits the major needs of the industrial-control market.

Dumb, smart and intelligent terminals

Add a keyboard and a communications interface to a computer output device, and you have a computer terminal. Most terminals come with a variety of interface options, the most notable being a selectable transmission data rate.

Terminals are being categorized as "dumb," "smart" or "intelligent." The difference seems to be this: Dumb terminals are like simple teleprinter stations; entered data go right to the computer. Smart terminals accept data and allow manipulation of the input before it is transmitted to the computer; data can be edited, checked for accuracy or checked for format. Intelligent terminals have a built-in legitimate processor and can be programmed to do some actual computations on the data prior to transmission to the computer.

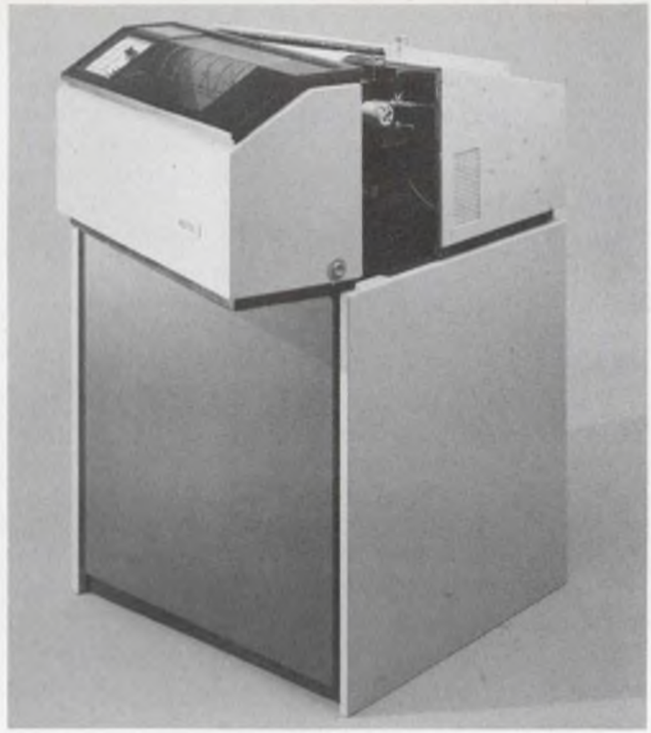
As might be expected, dumb terminals are the least expensive, and they are made by dozens of manufacturers. Among them are Teletype, Hazeltine of Greenlawn, N. Y., and Sanders Associates in Nashua, N. H.

Smart terminals are made by Hazeltine, Courier Terminal Systems of Phoenix, Ariz., Tektronix of Beaverton, Ore., Ann Arbor Terminals of Ann Arbor, Mich., and many others.

Intelligent terminals are made by the Datapoint Corp. of San Antonio, Tex., Sycor of Ann Arbor, Mich., Sanders, IBM, Four-Phase Systems of Cupertino, Calif., and others.

Most of the smart and intelligent terminals are based around a CRT and a keyboard. The CRT is usually a basic alphanumeric display with either 12, 16, 24 or 26 lines of 80-column-wide

Datapoint's 2200 intelligent terminal offers an alphanumeric keyboard for data entry, a CRT for data display and two digital cassette recorders for bulk data storage. The 2200 is programmable and comes with up to 16-k, eight-bit words of storage.



At 300 lines per minute and a cost of $4000, this printer is aimed at the minicomputer user. The printer uses an etched steel character band and offers 132-column printing. The manufacturer is Pertec.

printing capability. The keyboard is either part of the display box or detached. Depending upon the price of the unit, the display may have only upper-case letters and limited number and symbol capability. More expensive units have the full 128-character ASCII display. In some cases a graphics capability is a feature of the terminal. And often the terminal also has a hard-copy facility. Tektronix and the Photophysics Corp. of Mountain View, Calif., make terminals with copiers.

Terminals often are sold as a cluster of several CRT stations with a single controller and communications interface. Most manufacturers sell in this mode. For example, Courier sells a cluster of up to 16 CRT stations around a control station that has two redundant controllers in it.

Most terminals have selectable data rates, the most popular being 1200, 2400 and 4800 baud. Ernest N. Nicely, chief administrator at Courier, expects to see 9600-baud rates in the near future.

Many smart terminals are used in time-sharing systems. According to Robert Wallace, terminal equipment manager at Tymeshare in Cupertino, Calif.: "Most of our users have printing terminals that handle a 132-column business form and print at 30 cps. We have several users on CRT terminals with accessory printers for hard copy when desired."

Printz of Teletype sees a day soon when the CRT display and the printer will be integral parts of the same terminal rather than separate items attached together.

The wave of the future seems to be intelligent terminals. These come in two main types: the processor in the same box with the display, or with the processor in a separate console that controls several terminals.

Lawrence L. Mayhew, manager of the Information Display Products Div. at Tektronix, sees the main advantages of the intelligent terminal as these: "The terminal can be isolated from the main system software. Any software support that the terminal needs can be provided by the internal processor. Finally, the terminal can do some of the local processing that the main computer would otherwise have to be tied up doing."

Mayhew expects to see more and more memory incorporated in these terminals, while Robert R. Green, national sales manager for Datapoint, looks for graphics to be incorporated. Wayne F. Galusha, peripherals marketing manager at the Data General Corp., Southboro, Mass., says intelligent terminals will be shrinking in size.

"I don't see why hand-held calculators could not be used as intelligent terminals," Galusha says. "They have a basic processing capability. So why not tie them to a larger data base?"

Slower, cheaper card punches sought

Until fairly recently, the most popular speed for a paper-tape reader was 300 cps. "Now," says Robert L. Malone, marketing manager at Remex in Santa Ana, Calif., "the market is calling for slower, 150-cps readers. Why? Simply

In the world's first computerized self-service gasoline station at Lawndale, Calif., each pump is connected to a terminal that houses a minicomputer (right). The terminal accepts either money or a credit card. A card that is inserted is automatically checked for the customer's credit rating. If his credit is good, he gets to pump the gas. If he's delinquent in payments, a printout will tell him about it. If it's a stolen credit card, the terminal keeps it. The pump delivers exactly the amount of gas paid for. The gas station is owned by the Atlantic Richfield Oil Co. The terminal is made by the Docutel Corp. of Dallas, Tex.

because it's cheaper by a couple of hundred dollars."

Cost has become such a factor in paper-tape readers that the high-speed capstan drive system is giving way to the cheaper, but very reliable, sprocket drive.

William A. Wiesman, product manager at the Electronic Engineering Co. of California in Santa Ana, agrees with Malone. "Speed is no concern," he says. "Although machines go up to 2000 cps, nobody needs it."

Reader technology seems to be moving towards a separate LED-phototransistor pair for every track on the tape. Most readers, however, still use a single light source, such as a tungsten-halogen lamp, rather than discrete LEDs.

Among the leaders in the paper-tape reader business are such companies as Remex, Digitronics of Southboro, Mass., the Electronic Engineering Co. of California and the Tally Corp. in Kent, Wash.

Paper-tape punches have not progressed much in recent years. Common speeds are 60, 75 and 120 cps. The most often used are the 60 and 75-cps punches. Most of the punch mechanisms sold today are foreign-made. The leading manufacturers in the United States are the Litton Automated Business Systems Div. in Carlstadt, N. J., and Tally.

Malone at Remex points out that one trend in the industry is toward the incorporation of both a reader and a punch in the same box. Both are then offered with either fan-fold or spool tape handling.

"What we really need is a 50-100 card/min card punch that sells for $3000 to $4000," says Theodore H. Sweere, director of systems engineering at Varian Data Machines in Irvine, Calif.

But LeRoy C. Ostrander, vice president of Documentation in Melbourne, Fla., comments on this suggestion: "It's not likely to happen in the near future. The punch mechanism is too expensive."

What is available in punches, according to Ostrander, are speeds of 100 cards/min and up at prices in excess of $10,000. The leading manufacturers of punches include Mohawk Data Sciences in King of Prussia, Pa., Control Data Corp., Valley Forge, Pa., and Data Products, Woodland Hills, Calif.

Documentation is introducing a read-before-punch machine that will handle 100 cards/min.

Punched-card readers on the market are offered in speeds up to 2000 cards/min. The faster ones use a vacuum-assisted card pickup, and the slower ones are strictly mechanical. Optical mark readers are offered with specs that are similar to those for punched-card readers. ■■

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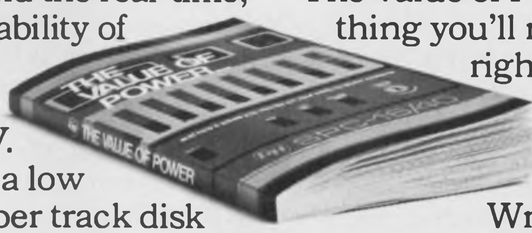

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General Automation

INFORMATION RETRIEVAL NUMBER 47

Portrait of a minicomputer Gordon Bell, engineer in a

John F. Mason, Associate Editor

Can a young dynamic electronics design engineer find fulfillment in a pre-Civil War woolen mill on the banks of the Assabet River in Maynard, Mass.?

C. Gordon Bell has.

Bell, who fathered the minicomputer several years ago, is now vice president of engineering for the Digital Equipment Corp., which occupies the old woolen mill. Bell's quarters could be the office of any successful executive. Except for three shelves of heavy books (heavy in any sense of the word) on such subjects as computer architecture, optical memories and software vs hardware. Bell's workshop, or private think tank, could be the headquarters for a low-profile, but good, textile designer, an architect or the editor of a slick magazine.

A large, blond wooden conference table is surrounded by yellow director's chairs. White end tables match the white brick walls, punctuated here and there by reds, blues and yellow in the form of lamps, coffee cups and ash trays. A color photograph on the wall shows—an asteroid and a distant star? No. It's a jellyfish, Bell explains later, that he photographed while scuba diving.

Sunlight fills the room. A quiet and cheerful oasis of coordinated living color.

The door opens. "Here he is!" the secretary announces with obvious admiration. And the 38-year-old dynamo rushes in. Bell rushes everywhere, people who work with him say. He attends from 15 to 20 meetings a week, interviews prospective employees, administrates and designs.

Clean-cut, an all-American type, young and already the vice president of engineering for a blue-chip computer company who reports only to the company's president, Bell is an inventor, an innovator and an author. He has it made. How did he do it?

Besides the obvious qualification of being very bright, he finds work "a lot of fun"—which, in part, accounts for his enthusiasm. When it stops being fun, he usually moves on, which explains the variety of things he has done—things that due to an unconscious creative organizing force, or to luck, have synergistically buttressed each other to move him up the ladder of success.

Father of the minicomputer, C. Gordon Bell, still manages to design, despite his many other duties as vice president of engineering for Digital Equipment Corp.

For example, after getting a master's degree at the Massachusetts Institute of Technology, Bell went to work at the institute's Lincoln Laboratories. His project was to feed data to a computer by voice.

"It was fun in those days," he recalls. "We were making far more advances in speech analysis and speech synthesis than anyone else had

mastermind: big hurry

made over the previous 10 years."

He left for several reasons.

"I thought the problem was short-term, maybe two years," Bell says. "I'm always getting into two-year projects that last four. But this one, I realized, was a 20-year program. I think engineers tend to get rewarded on shorter-term projects.

"Also, I'm an engineer. I spent my stint with science, and I wanted to build things."

Bell's speech-analysis work prepared him to move into computer design with the Digital Equipment Corp. (DEC). First, he got experience as a user, which he believes is essential. "A good designer must always see the user's point of view," he stresses. "He must be able to empathize with him. Marketing goes hand in hand with good design."

Bell also got computer design experience at Lincoln Labs. "We had a lot of equipment that had to be interfaced with the computer, and we wanted to do this easily and simply," he notes. "We worked with DEC modules—which is how I got involved with DEC—designing these interfaces."

Another aspect of the Lincoln Labs' work that carried over to DEC was a growing awareness that computers needed to operate in real time, or at least close to it. "There were no transistorized machines in 1960 except in the laboratory," he recalls, "and the only input to computers was with cards." So here was a requirement worthy of effort and time—a real-time computer with a faster input, such as a typewriter.

After Bell moved over to DEC, he worked on I/O structures and communications structures. He invented a teletypewriter switching system for the PDP-1. He built the PDP-4, an 18-bit machine. And he specified the PDP-5, "which is the root of the PDP-8 and really what you think of as the minicomputer."

The PDP-11 came in around 1969, still part of the mini family. The PDP-8 is a 12-bit machine, and the PDP-11 a 16-bit machine.

The other DEC machines are considered medium or large machines, and they don't fulfill the essential qualifications for a mini: low cost (under $20,000) and small size.

Bell also developed the PDP-6, a larger machine, which was delivered in 1964.

Work on the PDP-6 resulted in a turning point for DEC, Bell notes.

"In every technological period you've got a different set of mechanical and electrical problems to solve," he explains. "The PDP-1, 4 and 5 were all built with soldered connections. When the bigger PDP-6 came along, I guess I didn't do my homework. A large amount of hand-wiring was required, and the wiring error rate was very high. Something had to be done.

"There weren't enough skilled people to wrap and to check. So we decided to go to a machine-wiring technique. Only IBM was using such a machine at the time. We used the machine to build the PDP-7, 8 and 10. The PDP-8 was the first machine-wire-wrapped system to hit the market.

"All this because we couldn't build the PDP-6. Only 20 PDP-6s were ever built. Companies that didn't switch to machine wrap regretted it later."

Given hindsight, what would Bell have done differently?

"In general," he says, "I'd have argued more strongly about issues as they came up." For example, Bell believes in switching to new technology in the middle of a design. His credo is: "If it's inevitable, do it now!"

How does he feel about doing so much administrative work?

"The most frustrating thing," Bell says, "is knowing that I won't design a machine in detail. I get involved in the allocation of resources, I try to influence how we design—what languages we use, how we do programming, what tools to use and things of that kind. But you can only get so many kicks out of thinking by osmosis of having other people solve your problems."

Where are minis going?

"We're going in two wildly different directions here," Bell answers. "Minis with more capability are being built for the end user to compete with large machines. In the other direction, micro-minis, or microprocessors, are being built for the OEM market. These devices are intended for use as components in control systems, automobiles and instruments."

Does Bell have any strong outside interests?

"I guess I look at computing as having such a wide variety of things associated with it—finance, linguistics, organizational theory and its human parallels—that I don't go too far afield," he replies. "Inherently I think the only thing that pays off is to do things very deeply and follow through. And that takes a lot of time." ■■

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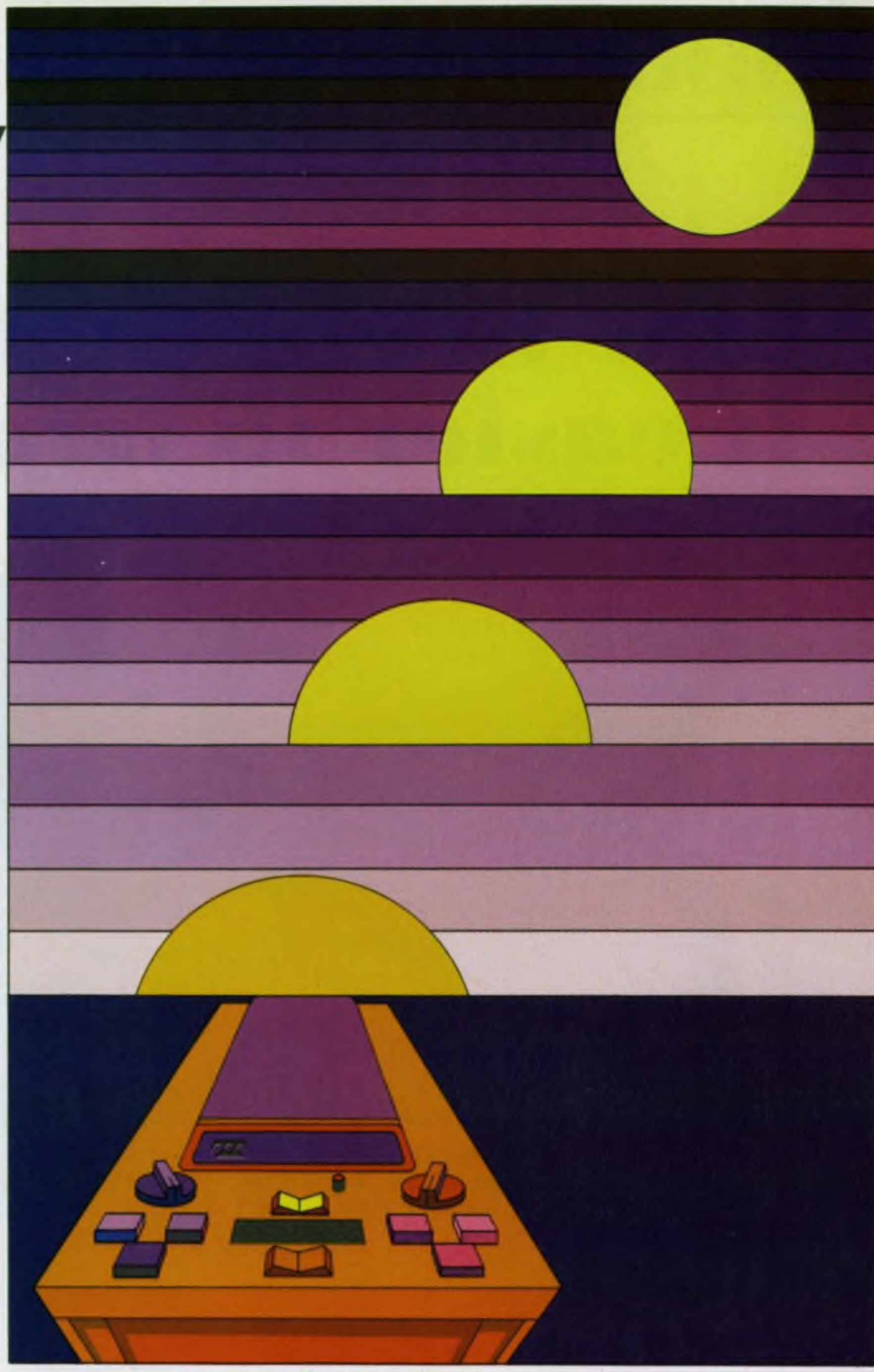

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INFORMATION RETRIEVAL NUMBER 49

New tricks in hardware it easier to improve the

Variable micrologic alters the run-time environment according to the language processed in the Burroughs B1700 series. The system runs Cobol, Fortran, Basic and RPG. All machines in the B1700 series have virtual memory and complete operating system, or Master Control Program in the Burroughs computers.

Seymour T. Levine, Associate Editor

The most vulnerable element of computer power—the programmer—is being strengthened by today's faster, cheaper computer hardware.

Techniques like stack architecture and microprogramming are opening the door to greater computing performance with each of the programmer's instructions. Memory management based on the virtual-memory concept is relieving the programmer of worry about main memory size and letting him concentrate more on the applications at hand.

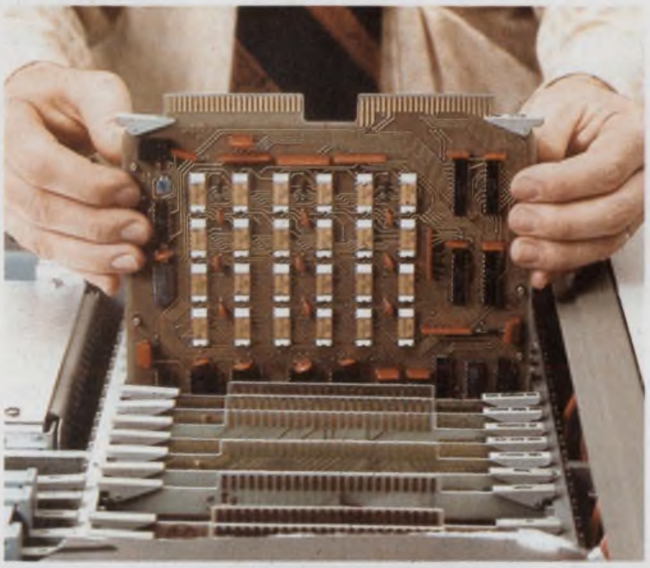
Why such a concentrated effort to boost programmer productivity? There are at least two reasons: For large-scale installations, the cost of programming is almost 50% of the price of the computer. And, secondly, with faster, denser, cheaper hardware—especially semiconductor memories—stack architecture, microprogramming and virtual memory become feasible. The cost tradeoffs alone favor heavier use of the new hardware and less programmer effort.

Microprogramming for instruction power

In a conventional hard-wired computer, user level instructions are fetched from main memory into an instruction register, the individual bits of the instruction set up logic paths in the control section of the computer. The control logic then carries out the instruction.

Instead of wiring-in the logic, the bit pattern of the user level instruction in a microprogrammed machine accesses a series of routines stored in a high-speed memory called a control store. Each instruction in the stored routine, called a microinstruction, orchestrates the control-unit facilities in accordance with the user's wishes rather than a preordained hard-wired pattern.

are making software



Microprogramming users are offered 86 machine-language instructions and 102 microinstructions for use on HP's 2100S computer.

These microinstructions control facilities within the central processing unit, such as inter-register transfers, bit manipulations and most input/output operations.

Two forms of micro-code are used: horizontal and vertical. With horizontal micro-code, each bit represents on-off control over an electrical path. In vertical micro-code, a portion of the microinstruction represents a specific operation to be performed, such as an addition, bit rotation or inter-register transfer.

A high speed ROM or RAM (100 to 200 ns) stores the microprogram. The entries are executed four to eight times faster than the rate for the main memory. In fact, the greater speed of the RAM permits execution of several microinstructions in between fetches from the main memory.

The Interdata Corp. of Oceanport, N.J., reports that a function can be performed three to 10 times faster with control-store programming (firmware) than an implementation with user-level software.

Another important use of firmware is to create a more suitable environment for executing higher-level languages.

With microprogramming, the instruction set of the machine can be geared to speed the execution of higher-level languages, such as Cobol, Fortran and PL/I. In the case of Fortran, the set could contain array-processing commands, floating-point arithmetic and important subroutines, such as sines and cosine. With Cobol the frequent use of the MOVE verb to transfer portions of data records makes firmware instruction a natural choice to perform this operation.

Stack architecture: A compiling aid

A programmer can shuttle data from register to register in machine-level (assembly-level) language to perform a computational task. But the involvement with the machine and the number of instructions required make such programming expensive.

High-level languages perform more with each instruction but the compilers (translators) for these languages do not generate efficient machine code. One reason is that the compiler can only count and sort and therefore ends up making many needless transfers to and from main memory.

But compilers work efficiently with machines that have a "push-down stack" architecture. In fact, stack architecture—together with microprogramming—often achieves efficiencies of 90%, compared with instructions written in machine language.

A push-down stack is a special case of a last-in-first-out buffer. In short, data are retrieved, one item at a time, in the reverse order from which they were entered. As each item is retrieved, the size or depth of the stack decreases by one; conversely, the entry of one item increases the depth by one.

Most compilers translate higher-level statements into pairs of operands, with the operator referring to the operands preceding it.

For example, the expression

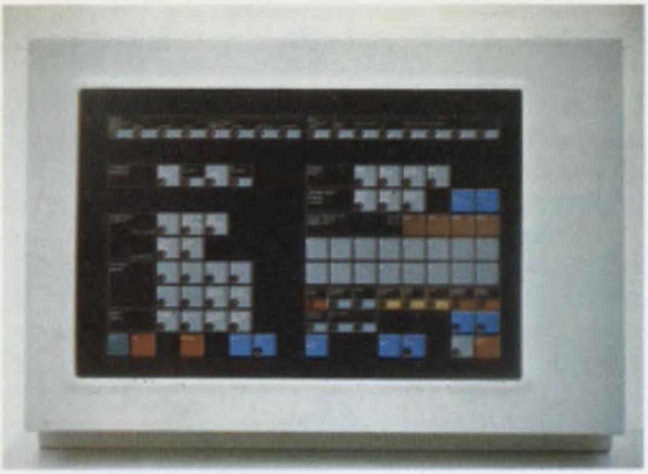
$$U = (E + F) \cdot (Q + M)$$

translates to

$$EF + QM + \cdot U = .$$

This means: "Add F to E (keep result). Add M to Q (keep result), multiply results by one another and store to U."

Without the stack, the compiler would set up temporary registers to hold E + F and Q + M and then divide the two quantities. With a stack, no such register transfers are needed. E and F are entered (depth = 2) and the first addition



Specialized hardware, such as IBM's 370 communications controller, performs the teleprocessing tasks of line control, polling, addressing and code translation, formerly done by mainframe software.

performed (depth = 1; stack contains E + F). Q and M are entered (depth = 3), and the second addition is performed. The stack now contains two entries: E + F and Q + M. The multiplication reduces the depth to one and gives the following product: (E + F) · (Q + M). Finally the "equals" sign delivers the result and empties the stack.

In addition to implementing higher-level languages by means of the stack operations of push (move down) and pop (remove topmost item), stack architecture allocates dynamic parameters (primarily subroutine), dynamic program history and subroutine calls.

Stack architecture also provides a direct assist for re-entrant routines (a subroutine that calls itself or is called by a number of users). Main memory stores the invariant portion of the subroutine code, and the stack holds the computed results and history. As each item in the stack is popped, control is transferred to the prior calling program. There is a twofold gain in efficiency: fewer main-memory references and the elimination of several copies of a compiler or other program to be stored for several users.

Virtual memory fits large programs

Even with microprogramming and stack architecture, there will be jobs that are too large to fit in main memory. Of course, the programmer can break the job into smaller tasks and direct the machine to perform each separately. But a memory-management technique called virtual memory relieves the programmer of this chore.

In a conventional data-processing system (or even one with stack architecture and microprogramming), the processor is directed by a sequence of instructions, or program, to perform arithmetic and logical operations. The entire processor-controlling program is stored in the system's real storage.

But most programs do not reference all their data and logic during any one short interval. So why store the entire program in main memory? In virtual-memory organization only the active portions reside in main memory and the remainder in a direct-access device, such as disc or drum.

To free the programmer of the need to break down the program into portions, addresses are assigned to program statements in terms of virtual storage. These addresses specify locations within the program by segment or page number and then by displacement within the given segment. A hardware-translation facility and system-control program transfer the program segments between main memory and external storage whenever addresses are decoded and the addresses are not in the main memory.

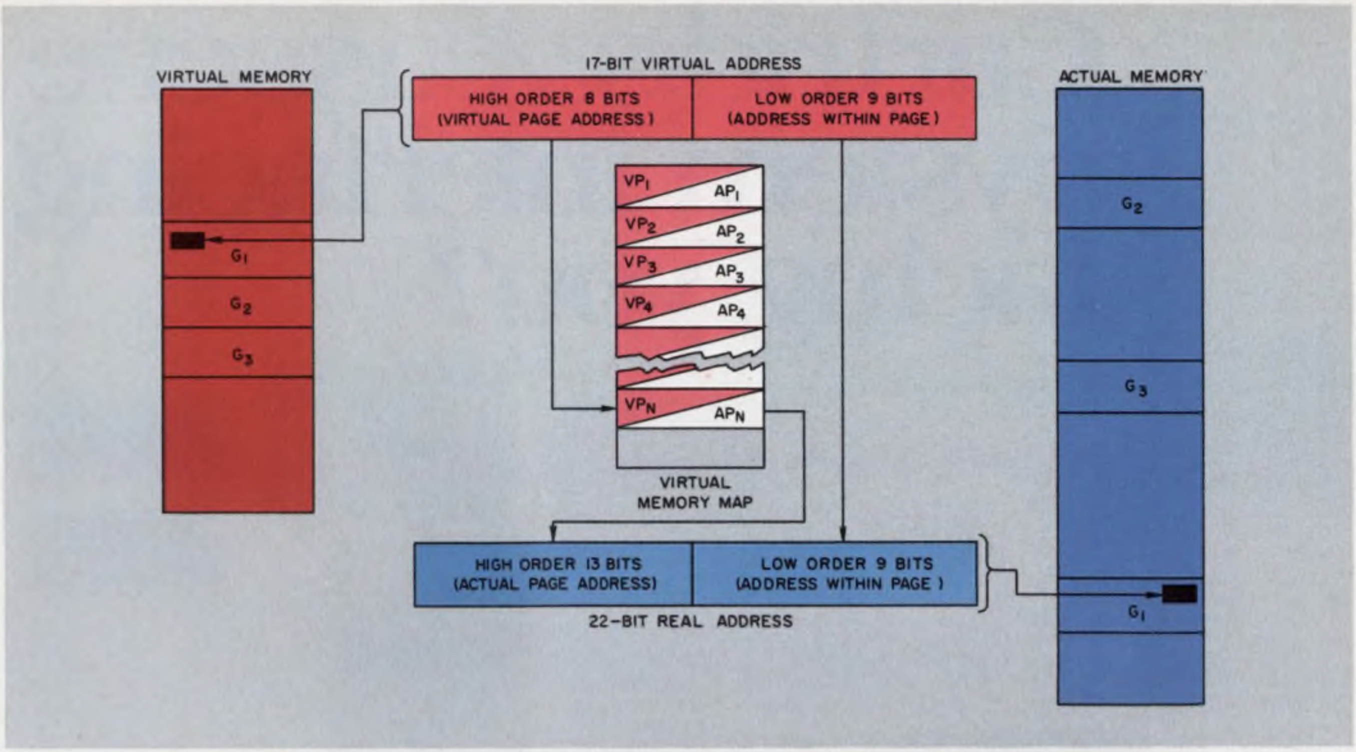
Even though the original program is written as a contiguous whole, the location of program segments in memory is anything but contiguous. Segments are loaded wherever available slots exist in main memory. Software updates the tables to indicate where the page, or segment of program, has been loaded.

Procedures for virtual-memory implementation vary from manufacturer to manufacturer. Burroughs attempts to segment programs at natural break points, such as subroutines or other complete procedures. IBM (370 series) and Xerox (Sigma 6, 7, and 9) segment by block size, or page, with Xerox using small blocks (512-word pages) and IBM 2048 or 4096-byte pages.

Burroughs, IBM and Univac employ virtual storage to relieve the programmer of concern for physical program size. As a fringe benefit, virtual storage provides an economical environment for teleprocessing operations. The memory requirements for these jobs fluctuate by 8:1, but the main memory that the user buys need not accommodate the peak teleprocessing load.

There are some negative aspects to virtual memory, however. If excessive paging—a condition called thrashing—occurs, little useful work will be done. IBM's paging supervisor monitors program paging demands, and if the rate becomes excessive, the supervisor halts some tasks. Burroughs minimizes thrashing by paging the programs in segments that correspond to natural break points. Xerox's Sigma series enters whole programs instead of executable pieces, so paging is not required.

According to Jack Mileski, manager of software marketing planning for Xerox Corporation efficient use of virtual memory, includes full hardware translation and small pages. With reduced I/O requirements, the memory allows operation of five concurrent modes on Xerox's Sigma 6, 7 and



Xerox's virtual-memory system maps virtual program addresses into as many available real memory slots as possible. Tight packing of main memory minimizes the amount of program swapping and enhances multimode operations like time-sharing, data-base inquiry and real-time control.

9 computers with the CP-V operating system. The modes are:

- Multiprogrammed batch.
- Remote batch.
- Time-sharing.
- Transaction processing or interactive information processing.
- Real-time.

Use of hardware features varies

Virtual memory, high-level language and stack architecture have been used in Burroughs machines almost from initial inception. The B5000 had virtual memory in 1961. Since then, all programming on Burrough's computers is based on Algol 60 and an extended version of Algol 60 developed at Burroughs. Yes, there is a machine language, but all compilers and operating systems are written in the extended Algol. Burroughs calls its operating system the Master Control Program (MCP).

The B1700 computer systems released in June, 1972, range from the small-system B1714 and B1712 to the B1726, a medium-scale system. In addition to virtual memory and stack architecture, the B1700 series alters the contents of its writeable microprogram-control store under MCP in accordance with the applications language executed—Cobol, Fortran, Basic and RPG. The latter is a business program language called Report Generator. Burroughs is not alone in using high-level languages to develop systems software. Stack architecture and microprograms are used in such machines as Hewlett-Packard's HP3000 midi, which employs SPL, an Algol-like language, and Microdata's 32/S Mini, which employs MPL, a derivative of PL/I.

In addition microprogramming offers the user complete flexibility in emulating the instructions of a range of machines. Companies such as HP, Microdata and Interdata support user microprogramming with well-defined assemblers and writeable control store. HP offers with its 2100S minicomputer a pROM writer to fuse debugged microprograms into ROM chips. Interdata's Model 85 supports up to 4096 32-bit microprogram words.

A small number of microinstructions can accomplish a great deal: Just 256 24-bit words implement floating-point multiply, divide, add and subtract functions on the HP 2100S.

Computer Automation's new minicomputer, the Naked Mini LSI, announced May 1 has a novel hardware/software tradeoff. The machine's CPU is internally microprogrammed, but not by a ROM or RAM. Three silicon-gate programmed logic arrays, each with 24 input and 20 output lines, replace the ROMs and RAMs. The whole 16-bit mini plus 4-k memory fits on a 15-by-16-in. circuit board.

Both Burroughs and IBM caution that the user should not tamper with the machine's innards. IBM's 370 series has a writeable control store, that can be upset, as does the Burroughs 1700 series. ■■

INFORMATION RETRIEVAL NUMBER 52

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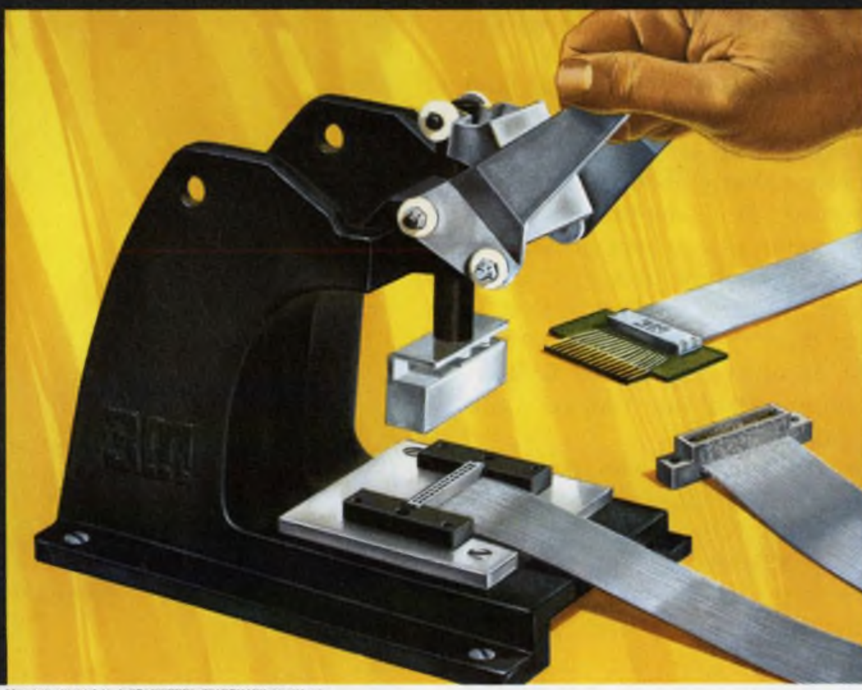

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INFORMATION RETRIEVAL NUMBER 53

Data networks putting the power of computers at fingertips

Morris Grossman, Associate Editor

ONE of the fastest growing areas in the computer industry . . . . the trend that puts access to a computer as close as the nearest phone extension.

Computer data networks are all of that and more.

Banks, airlines, stores and a growing string of other businesses rely heavily on such networks to conduct their business. The computer industry looks to network expansion as a source of soaring profits. Large, on-line computers that link many data terminals have a dollar growth rate that is at least 50% greater than that for the computer industry as a whole, according to James Dobbie, vice president of engineering at Varian Data Machines, Irvine, Calif.

Analog networks are carrying the brunt of data traffic at present, but all-digital systems are on the horizon. Until they arrive in force, modems and auxiliary circuits are playing important roles, correcting distortion and errors and thereby enabling the analog systems to handle digital data.

Plug-in computer power can be purchased from a time-sharing service today almost as easily as a consumer buys electricity from a utility. Recently the Memorex Corp. of Santa Clara, Calif., announced that its Memorex 1280 cassette terminals would be used by Marcoin, Inc., in a nationwide EDP service for gasoline stations. Two-way communications over WATS lines will bring the power of large computers to small stations for as little as $35 a month. The central computer is a Burroughs 3500, based in Falls Church, Va.

With the Memorex terminal, data is entered off-line into the 1280 cassette, which holds 180,000 characters. Thus transmission over the phone line can proceed at its maximum speed of 120 char/s. Receipt of data is also at maximum speed into the cassette unit. Thus the printout

General Electric's Mark III computer network gets a workout in Atlanta's new Omni sports arena. James R. Fincher of Quo-Modo, Inc., operates a terminal that helps design the unusual Ortho-Quad truss structure.

vast power of everyman

494, real-time computer has just gone on-line to handle, eventually, worldwide reservations for Lufthansa-German Airlines. Expansion of the system will continue into 1975.

And then there are the general computer services, offered to the public by approximately two dozen companies. General Electric of Bethesda, Md., for example, offers the Mark III Information Services. It connects 300 cities in Japan, North America and Western Europe. Control Data, University Computing, Computer Sciences, Tymshare, Inc., and many others also offer extensive networks.

The list of companies and the variety of services grows daily, and with it the need for the

Raytheon's PTS-100 data terminals at the Trans Union System Corp. of Chicago operate into a large central computer credit-verification system. Each terminal needs a data link to the computer, and the many links, in turn, need a small computer to control and preprocess the traffic on the network of data links.

need not consume expensive line time. Raw sales and expense data from the average gasoline station is transmitted in about 22 seconds, and computerized payroll, depreciation and other operational analysis can be returned within the same day, as compared with the usual 10-day turnaround from conventional computer services.

Periphonics of Bohemia, N. Y., offers a communications processor aimed at the banking market. Its Bank-Comm 7 equipment includes an audio-response unit with a 2000-word vocabulary. The input terminal uses a Touch-Tone phone. Periphonic's system can be used by itself or as a preprocessor for a centralized computer system. Many peripherals, data sets and CRT terminals can be accommodated.

Sperry-Univac has announced that its Univac expansion of common-carrier data networks to carry the traffic.

Data links are expanding

To carry data from the customer to computer and back, a data link is needed. Not long ago the choice was easy. There was only Ma Bell. Since the 1968 Carterfone decision, more options have become available.

Carterfone Communications, a terminal-equipment manufacturer based in Dallas, Tex., sued to permit the attachment of private phone equipment to AT&T's and that of other dial-up telephone networks. Carterfone won and broke Bell's monopoly.

Besides opening a vast market to phone-terminal equipment makers, this break in Bell's monopoly has led to other Federal Communications Commission decisions, so that now several companies are offering or planning to offer common-carrier services.

Microwave Communications, Inc. (MCI), of Washington, D. C., is one. It is setting up intercity microwave-transmission links, using its own towers and local phone company lines. It is competing with the established carriers—AT&T, Western Union and General Telephone and Electronics—in private-line services. The MCI network includes Chicago, St. Louis, Denver, Kansas City and other cities.

MCI plans to be nationwide by next year. And it has teamed up with Lockheed and Comsat for use of satellite links in 1975-76.

But MCI is a private-line common carrier for point-to-point links only. The Data Transmission Co. (Datran) of Vienna, Va., plans to offer a nationwide switched network, exclusively for data transmission. It hopes to include by 1975 a broadcast capability that will allow a subscriber to send his message simultaneously to many subscribers. In the meantime Datran recently announced that it was ready "to start working with customers" for service to eight cities over leased private lines. The service is to start early next year and cover most of the same cities listed by MCI.

AT&T isn't sitting still either. It plans to establish special digital links between five cities as a first step in its expansion in the 1970s. The data channels will connect Boston, New York, Philadelphia, Washington and Chicago. Service is expected to start by next year.

Meanwhile, Bell of Canada—the Trans-Canada Telephone System—is already offering its Data Route network. Its new, all-digital system will reduce transmission costs by 90%, according to J. C. Carlile, president. "Modularity of the system permits easier installation and expansion as the demand grows," he notes. "And there's greater reliability."

An all-digital system can provide more error-free operation, because digital repeater stations don't merely amplify amplitudes and all the noise picked up along the way as analog systems do, but regenerate and retime the signals. Thus the retransmitted signal is nearly as clean as the original.

The Computer Transmission Corp. of Los Angeles provided much of the equipment and engineering that went into the Canadian network. The company's pulse-mode modulation technique is used for the system's local distribution, and this is where most errors occur in analog systems. Multitran—a time-division multiplexing and switching package—combines these local, slower-speed-signals into 50-kb/s groups for transmission over the network's "spine," or series of high-speed microwave links. And Synctran—a master-clock synchronizer and alarm system—monitors the entire network from a central location.

As with most carriers, the full range of services from a teletypewriter speed of 110 up to 50,000 b/s are offered by the Canadian network.

Problems with analog systems

But in the United States analog systems still carry the data load. And this poses problems. The systems were designed for voice. Modems and auxiliary distortion-correction and error-correction circuits are needed to accommodate the digital traffic.

Some of the problems include these:

- Delay distortion, which varies with frequency, time and different path links.
- Noise—mostly of the impulse type—and phase jitter.
- Narrow bandwidth to about 3000 Hz—adequate for a single voice channel but limiting for high data speeds of about 2400 b/s.
- Frequency offsets between transmitted and received signals, which can be very injurious to data traffic.
- Long turn-around time, which cuts throughput for high data speeds.

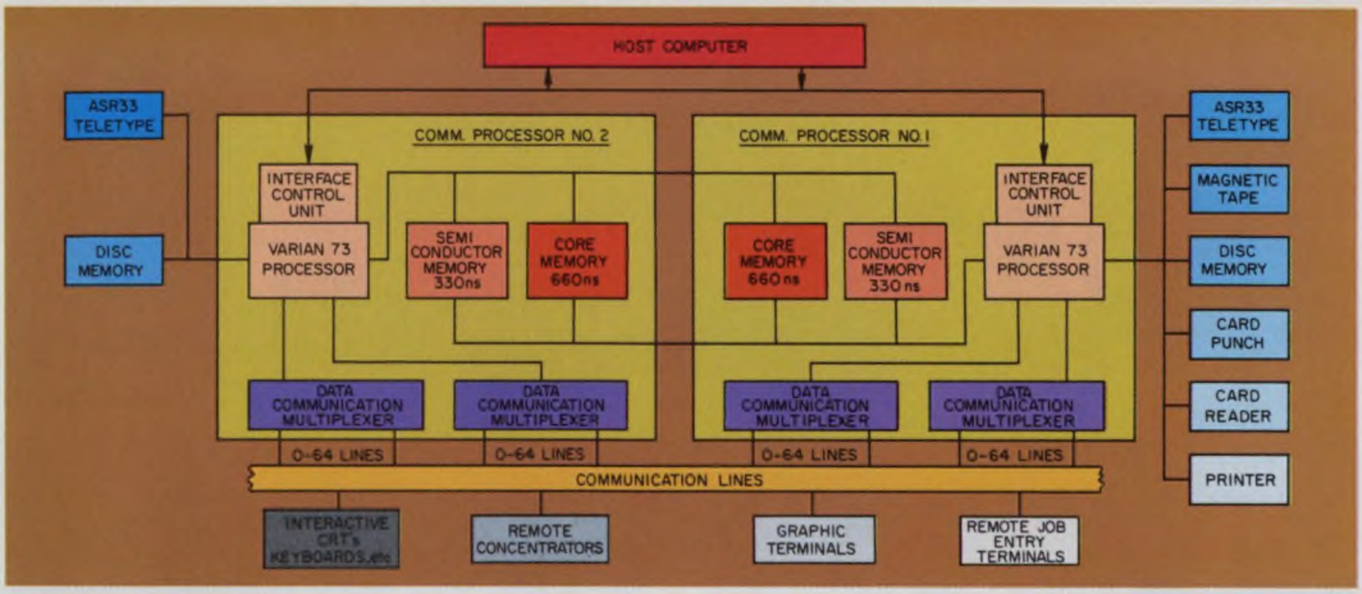
The modems and their compensating circuits correct for these shortcomings.

And, of course, the primary function of the modem at the transmit end is to convert digital-data levels and timing—which, for computers usually conforms to the EIA Standard RS-232—to Bell-compatible analog signals. This function is accomplished via some modulation method, such as amplitude modulation (AM), phase modulation (PM), vestigial-sideband amplitude modulation (VSB/AM) and many others. And at the receive end, the modem must demodulate the signal back to RS-232, computer-compatible data levels. Modems are used on both the switched and leased private lines.

There are many ways of classifying modems. Here is a partial list:

- **Modulation method**—AM, FSK, PM, PAM and many others.
- **Speed**—low speed (to 300 b/s), medium speed (1200 to 2400 b/s), high speed (3600 to 9600 b/s), and very high speed (20,000 to 50,000 b/s).
- **Synchronous or asynchronous.**
- **Error-control features**—adaptive equalization, error-correction codes, ARQ routines and others.
- **Operational features**—simplex, half-duplex or full duplex.

Fortunately the minimum standards for voice



Many minicomputer manufacturers are supplying special packages for control of large communications networks. The Varian-73 preprocessor offers a dual unit that can supply extra reliability through redundancy.

communications are more than adequate for low-speed data transmission, such as the teletypewriter (TTY) speeds. And a veritable flood of companies, many very small, supply modems to handle this speed range, with features and costs so similar that the choice of such a modem often depends most on such intangibles as the company's promotional efforts. Included in this category are the acoustic-coupled modems, modems on a PC board, modems on a chip, voltage-controlled oscillators and, of course, Bell's assortment, which includes that old standard, the low-speed (to 300 b/s) type 103, which uses two-tone FSK.

However, as transmission speeds approach the higher speed categories—2400 b/s and above—the many digital/analog matching problems become more difficult to control. Also, this market is taking longer than some companies expected to become profitable. Thus fewer companies, and those with greater technical and financial resources, are likely to survive to supply the highest speed modems. The recent merger of Rixon, Inc., of Silver Springs, Md., to become a subsidiary of Sangamo, combined the technical resources of Rixon, a pioneering company in the high-speed modem field with the financial resources of Sangamo, which incidentally had its own line of modems.

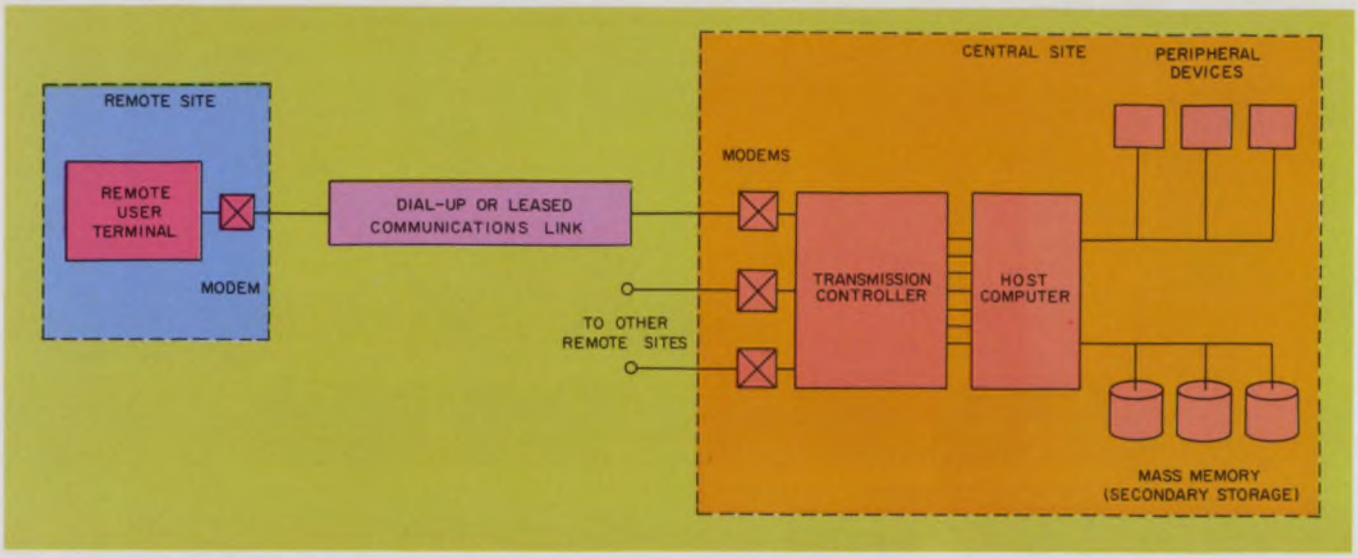
At low speeds most modems are of the asynchronous type, as required by most on-line keyboard type terminals, such as those compatible with TTYs. These modems mostly use an FSK, two-tone modulation system. Asynchronous operation also extends into the low end of the medium-speed range, roughly 1200 to 1800 b/s. But at 2400 b/s and higher, modems usually must use synchronous methods and PM or one of the more sophisticated combinational modulation schemes, such as phase-amplitude modulation (PAM), to attain better use of the available bandwidth.

Also, at high speeds, voice-grade lines require phase and frequency equalization. The more advanced modems provide built-in automatic adaptive equalization, since small changes continuously occur in the transmission lines, and also almost every different dialed-up connection needs a different equalization setting. Paradyne Corp. of Largo, Fla., and Codex Corp. of Newton, Mass., offer automatic equalization, and Codex uses PAM but Paradyne uses a combination PAM/VSB. Many modems have manually adjusted equalizers, and others leave it to the user to provide this facility.

Error control is important

Error control is a major consideration at any data speed, but at high speeds the control of noise, delay distortion and bandwidth limits, among other problems, makes errors particularly difficult to control on voice-grade lines. Error-control methods provide some type of parity check on a message block basis. Should the received signal fail to pass the parity check, a request for retransmission of the message (NAK—not-acknowledged signal) is sent to the data source. An ACK (acknowledge) signal indicates that the block contained no errors and the next block can be sent. Such a scheme is known as an ARQ (acknowledge/return request) routine, and requires line-duplexing ability.

The early Bell 103A could provide full-duplex performance over a two-wire line, but only at 300 b/s. To provide full-duplex operation at medium and high speeds, you need a four-wire



The modem is a basic interface device at both ends of a data link between a central computer and a remote data terminal. And a network of data links requires a computer to act as a transmission controller.

line, which is expensive.

Thus an ARQ routine requires the periodic reversal of the usual two-wire half-duplex voice line. And when compared with the message time, this turn-around time can be substantial and severely limit throughput.

To put this into perspective, a 1000-bit message block at 4800 b/s takes about 200 ms to transmit. But the typical line takes about 300 ms to turn around completely, because echo suppressors on lines must be given enough time to reverse themselves. And each reversal takes about 150 ms.

One way of avoiding channel reversals is to provide a separate, low-speed asynchronous channel for the returning short ACK or NAK signal. But this approach is not often used, because it requires a special interface at the computer or data terminal that is not usually available. However, this is probably the best solution for the near future, according to Steven J. Puchkoff, product manager of Codex Corp.

Another scheme uses special tones to disable the echo suppressors. Then the delay could be only the modem's resynchronization and equalization time. But then you get echoes, and they may take a while to die down. However, best of all is a low error rate to reduce the need for reversing the line.

Modems are here to stay

At the higher data speeds, large areas remain open for technical improvement in error control and throughput. Modem makers, who keep ahead of the pack, will therefore continue supplying new improved data modems, and these will remain as distinct and separate products. However, at the lower speeds the trend is for computer and data-terminal manufacturers to buy stripped-down modems, or modems on PC boards, for incorporation into the terminal or computer. In the short term, low-speed modems will become primarily an OEM market. In the long term, such modems will tend to disappear as separate entities and become part of the terminal manufacturers' equipment, according to Harold Gruen, president of II Communications Corp., Willow Grove, Pa.

This trend is, of course, enhanced by the improved availability of lower-cost MOS/LSI microcircuitry, phase-locked-loop circuits on a chip and other such system building blocks, which makes it easy for the terminal and computer maker to roll his own.

Wideband modems needed for hybrid data systems

Many engineers consider the marriage of data signals and voice oriented lines a shotgun affair. They predict that digital-transmission and switching systems are the choice for the future. And such digital systems would not only carry data but also voice and facsimile. There is a very strong temptation to say, "Let's start from scratch and do it right."

A limited amount of switched, wideband service is available on a trial basis, from AT&T's DataPhone 50. The system offers dial-up 50 kb/s service between New York, Chicago, Los Angeles and Washington, D.C., and the Bell system supplies and maintains all the terminal gear.

But the existent multibillion-dollar investment in current systems cannot be ignored. Therefore, for a long time, analog and digital systems in hybrid combinations must continue to service the data-processing community. Wideband modems provide the vehicle for matching very-high-speed data rates (20,000 to 50,000 b/s and higher) to multichannel spectrums that normally carry 12, 60, 600 or more voice channels in frequency-multiplexed systems. And on the digital side of the modem, time-division multiplexing adds flexibility to the system by accommodating all the needed speeds—from TTY data rates to 9600 b/s, about the maximum that can be packed into a good, well-equalized voice channel. Wideband modems can also link data channels to troposcatter, satellite, microwave or other radio systems, which might form part of a long-haul data link.

Thus analog, voice-channel, dial-up lines feed into frequency-division-multiplexed systems, or time-division-multiplexed data sets are concentrated into broadband radio channels. And also almost every other conceivable combination is found somewhere in one of the data network services offered by such companies as General Electric, General DataComm Industries, University Computing, Control Data, Com-Share and many others.

Computers that service networks

Data-communications systems have grown so complex that computers are needed to control and direct them. These computers, mainly minicomputers, are variously called programmable front-end processors, satellite processors, message switchers or concentrators by different manufacturers. The tasks they perform, though, include similar or identical operations.

Inputs directly from data terminals, frequency and time-division multiplexers or even some low-speed inputs dialed in over telephone lines are combined under the direction of a small computer and fed to a central host computer over one or more wideband lines. The line servicing of these varied inputs involves tasks like terminal identification, polling, link establishment, task scheduling, priority determination and many others. All these tasks take time and need memory capacity. The host computer center is relieved of these tasks by the minicomputer serving the concentrator assembly, and only the essential message data is sent on to the host computer.

Depending upon the installation size, the amount of data sent to the host computer might be reduced to 10 to 20 kilobytes from an incoming level of perhaps 20 to 60. These overhead tasks, among other possible ones, can do the following:

- **Restructure** incoming data and accumulate slow data for more efficient input to the host computer.
- **Recode data** to conform to the host computer needs.
- **Check incoming data** for errors and perform ARQ routines.
- **Switch messages** from one terminal to another.
- **Poll data terminals** to determine whether data is ready for transmission or if the terminal can receive data.
- **Store-and-forward messages** to smooth traffic flow. Messages during peak-load periods can be stored in a suitable memory, and when traffic slows, the messages can be forwarded to their destination—either to another data terminal or to the host computer. This feature can also serve to retain messages for longer periods to provide repeats for messages that are lost.

Several minicomputer manufacturers have entered this communications preprocessor field. Besides supplying the minicomputer, often in a specialized form, these manufacturers also provide a large variety of sub-units and peripherals, such as automatic-dialing units, modems and software to control the system.

Varian Data Machines offers the V73-DC system. It features a dual-processor configuration that can use one of the processors as a hot standby, or both processors can share the processing load. Thus the system can exploit its redundancy for extra reliability in on-line applications, or the dual-port memories can be shared in many ways to control local peripherals or remote I/O units and handle the many diverse line speeds.

Microdata has the Micro 1600/60, which it calls a dual processor, also specifically intended for performing communications tasks, such as data concentration and store-and-forward switching. Its high data capacity (40,000 char/s) permits it to serve up to 256 communications channels. The "dual" part of its name stems from its two independent CPU elements that share a common main core. The first CPU serves the general-purpose data processor functions and uses a microprogram to control the core memory. The second CPU serves the more dedicated functions. Its operations are directed by firmware to control the communications links. An interrupt link allows each CPU to interrupt the other, and the common core memory serves as the transfer channel between the two CPUs.

And Digital Equipment Corp. (DEC) also has an extensive group of building blocks to perform communications tasks, called DecComm 11, which is built around the PDP-11 minicomputer and a special software package called Comtex-11. The building blocks include such items as a 16-line asynchronous multiplexer interface (DM11), an autocalling interface (DN11) and many other units needed to assemble a communications preprocessor station.

Other companies such as Data General Corp., Burroughs, Interdata and Telefile, to mention only a few, also offer such preprocessor minicomputer systems. ■■

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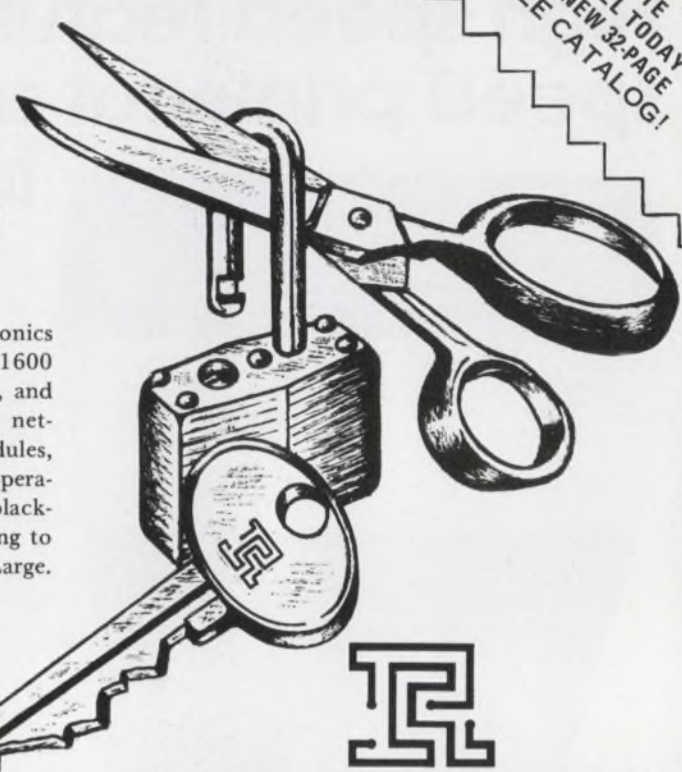

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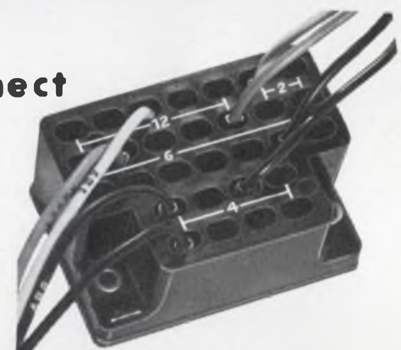

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INFORMATION RETRIEVAL NUMBER 61

World's biggest computer at drawing designers and

Jules H. Gilder and John F. Mason, Associate Editors

By combining the regional Fall and Spring Joint Computer Conferences into one show—the National Computer Conference and Exposition—the organizers hope they have transformed two declining shows into one big winner.

In contrast with the narrow end-user views of the fall and spring meetings, the new exposition examines the total picture of computer technology—both design and end user.

The show is described as the world's largest for the computer industry, with over 200 organizations occupying about 700 booths. A total of 35,000 visitors are expected to attend. This would compare favorably with the biggest year for the fall and spring conferences—1969—when 26,000 visitors and 1000 booths were tallied in the fall and 35,000 visitors and 470 booths in the spring.

Of the more than 100 technical sessions at the new show, 47 are applications-oriented to the end user. The rest are addressed to computer designers.

The quality of the show has apparently impressed some of the bigger companies. IBM, Control Data and one of the divisions of Honeywell have returned as exhibitors after having dropped out of the previous shows.

Intelligent terminals, such as this one from Digital Equipment Corp., contain a minicomputer that can be used to preprocess information for the CPU.

Topics of particular interest at this year's show include computers and the automobile, voice answerback (talking computers), "intelligent" terminals and point-of-sale systems.

Session 13, "Intelligent Terminals," considers terminals according to their "intelligence," or complexity, and then argues the division-of-labor problem. Should the bulk of the workload be put in these terminals or in the central computer?

"The session should be helpful to users, user managers, terminal designers and to systems designers," according to its chairman, Ira Cotton, a staff member of the Institute for

show aims end users

This merchandise ticket reader—the Friden Model 705, built by the Singer Co.—automatically reads and records coded information.

Computer Sciences and Technology in the National Bureau of Standards, Washington, D.C.

Three experts describe the levels of terminal intelligence available today. Presenting the low end of the spectrum—the point-of-sale terminal—is Zane Thornton, deputy director of the Institute for Computer Sciences and Technology of the National Bureau of Standards. "You can't simply replace the cash register with a point-of-sale system and say that you have done something significant," he cautions. "You must look at the whole system in order to take advantage of the technology available, and you must establish some kind of commonality."

The grocery industry has adopted a common code and symbol for use with point-of-sale systems, but there are still gaps in the merchandise industry's code uniformity. Uniformity is necessary, Thornton points out, because "stores are in for very large outlays of money to buy point-of-sale systems, and they must be sure their systems will automate everything they possibly can."

Speaking for the terminal of "average intelligence," such as a text-editing system, is Douglas Englebart, director of the Augmentation Research Center at the Stanford Research Institute, Menlo Park, Calif. He gives examples of entry and feedback techniques for terminals that are tied into large networks of computer "knowledge" centers.

Any system, Englebart points out, must be designed with the assumption that the terminal will be tied in with other computers via digital links.

Describing terminals ranging from "smart" to nearly self-sufficient "genius" machines—one that can draw computer graphics—is a paper by Andries Van Dam, associate professor of computer science, and George Stabler, a graduate student, at Brown University in Providence, R.I.

They tell of a system being planned at Brown and discuss the division of labor between the satellite, or terminal, and the host, or central computer. More last-minute flexibility is needed, the authors say, in deciding how much work the terminal should be asked to do and how much should be assigned to the computer. Van Dam wants to be able to delay such a decision until it's determined how busy the computer is.

The authors describe a technique by which pieces of software can be changed from one machine to the other at run time without having to rewrite any software.

Dividing the work

Session 3, "Point-of-Sale Systems," describes how they are used in grocery and department stores. "The description will, hopefully, help the audience design point-of-sale systems for other kinds of businesses," says Richard K. Hampson, session chairman and president of Data Technology Industries, Inc., Riverdale, Md.

"People in the software business or in systems design might see a way to use point-of-sale systems in the insurance business or in warehouses," Hampson says. "They would simply use a CRT for on-line transaction processing instead of a cash register."

John M. Hunt, vice president and chief of technical offices of Singer Business Machines in San Leandro, Calif., describes department-store point-of-sale systems that use anywhere from one to 150 terminals. Some designers build systems with most of the intelligence in a central computer, he notes. But based on experience gained with 20,000 terminals in the field in the last five years, Hunt is a strong advocate of putting intelligence in the terminal.

"When you look back over the past," he says, "the things that always seem to kill you are things that are inflexible. An intelligent terminal is flexible and can be changed without having to modify a lot of hardware in a central system."

A different tack on this question is taken by W. Riley Daniels, director of food distribution systems for Litton Industries' Sweda International Div., Morristown, N. J. In his paper on point-of-sale in the grocery-store field, he observes that in systems that use a scanning technique, "you're dependent on a system that does a lot of price look-up."

"In that case," he continues, "you want as little intelligence in the terminal as possible. You want it in the big machine in the back room."

On the other hand, Daniels points out, there is also the possibility of having "a 10-minute black-out in the big computer; then you'd want the intelligence back in the terminal."

So, he concludes, it's not an easy question to answer. "We at Sweda, however, lean to the central-computer solution," Daniels says.

The main thrust of his paper considers how new systems should be evaluated. "If a buyer concentrates, as many people do, only on the ringing up and bagging elements," Daniels says, "he misses a very large part of the total checkout process, which includes a lot of irregular things that happen on an infrequent basis."

To take care of all the loose ends, Sweda recommends an intensive work-sampling program as the best way to identify all elements. "This means a solid month with a crew of three to five people," Daniels says.

What codes do you use?

The pros and cons of coding techniques are discussed by E. T. Doddridge, manager of major accounts at National Cash Register, Dayton, Ohio, in his paper, "Mechanics of Technology for all POS Applications."

Doddridge describes black-and-white, magnetic and color-bar codes "trying to remain as unbiased as I can." NCR manufactures the color-bar code, which Doddrige says is the most accurate, consisting of six check points along the way.

"It's a soft checking code," he says, "which means it has no clocking mechanism in the decoding logic. And it is virtually impossible to counterfeit or alter."

Computers and the auto

Four sessions are devoted to computers and the automobile. Session 48 examines the role of computers on the assembly line, Session 75 the computer in the car, Session 60 computers to diagnose malfunctions in cars, and Session 86 two applications: computers used by the FBI to track down automobile thieves, and computers used by car manufacturers to handle customer needs, such as directing complaints to the right place and keeping inventory of spare parts.

Session 48, "Computers in Automotive Design and Manufacturing," is headed by Hans J. Kuschnerus, supervisor of technical and industrial computer systems in the Central Staff Systems Office at the Ford Motor Co., Dearborn, Mich. "I want to show that we're seeing a totally different way of doing business in automotive plants," Kuschnerus says.

Kuschnerus explains how body-design engineers at Ford use a computer-directed scanner to translate the dimensions or clay models into digital reference coordinates. A computer-controlled drafting table is then able to reproduce a comprehensive drawing of the model.

The data obtained by the scanner can also be used to produce visual displays on a CRT, Kuschnerus says. With a light pen, the engineer can adjust the contours and generate smoothed data points, suitable for the production of corrected drawings. With further computer processing, the data can be used in the numerically-controlled machining of tool dies.

With this system, the CRT and light pen also help the engineer design the car's electrical system. A procedure that will allow the engineer to use the CRT and computer to calculate the electrical characteristics of the designed components is under development.

Kuschnerus expects his audience to consist of computer companies and systems houses —"computer systems designers rather than designers of computers"—who would like to know how to design and sell to the automobile manufacturers.

One talk describes how computers can aid the designers of automobiles and the two others how computers can aid on-line manufacturing.

For the designer, General Motors' James E. McDonald's talks on "Design Engineering and Automotive Body Drafting by Computer Graphics." McDonald, who is head of GM's Computer Technology Dept. and a member of the company's design staff, is a user of the computerized system himself. He describes how General Motors engineers progress from clay models of body designs to the design of dies by use of graphics and drafting.

For the users of computerized manufacturing equipment, Dale F. Larson describes the "Use of Computers in Automotive Manufacturing." Larson is supervisor of manufacturing control systems at GE and is involved in advanced planning and the prototype design of computerized manufacturing systems. He tells how computers are used for on-line control and testing, for simulation and for scheduling plant operations.

"Minicomputer—The New Quality Inspector in the Automotive Assembly Plants" is the title of Hriday R. Prasad's paper. Prasad, who is supervisor of process computer systems at Ford, discusses the minicomputer's role in emission tests, electrical tests and the monitoring of torque tools to bolt down chassis components.

Onboard car computers

Session 75, "Onboard Computers for Automobiles," promises to be of high interest to both designers and marketers. Led by H. Blair Tyson, director of transportation systems at General Motors in Warren, Mich., it has seven panelists.

Frank Jaumot, director of research and engineering at the Delco Electronics Div. of General Motors in Kokomo, Ind., describes the achievement of quality and reliability in car electronics. Other panelists are from the Environmental Research Institute of Michigan, Rockwell International Microelectronics, the RCA Solid-State Technology Center, IBM, Bendix and Ford.

"Maybe computers in cars need a special computer language," Tyson says, "and maybe something like this will come out of this session. We hope so."

Session 60, "Off Vehicle Diagnostics," is planned to interest a wide audience of engineers, marketers, manufacturers of automotive test equipment and "Detroit people in general," says Sydney J. Roth, senior product engineer at the Marquette Manufacturing Co., St. Paul, Minn.

Roth presents the first paper in which Marquette's computerized vehicle-diagnostic system is described. Using a DEC PDP-8L, the system detects and pinpoints potential malfunctions.

Electronics for troubleshooting

An Army diagnostic system is described by Harry Young, an electronics engineer, and Daniel Abbas, a research physicist, both of the Army Tank-Automotive Command in Warren, Mich. Three years into development, the system is now in the engineering prototype phase and is to go into the engineering design test phase in the fall.

The Army has recently revised its philosophy and is in the midst of changing the system, Young says. Initially sensors were put on components to test for bad ones. "But that's all the information we got," Young explains. "We found out that certain components were bad."

The new philosophy is to test the vehicle—"we test the power, idle roughness or engine misfires." The system applies these data, using a computer-directed diagnostic approach.

"In some cases the procedure is not completely automatic," Young says. "The computer might direct the mechanic to make the diagnosis."

The new technique has its advantages. It precludes having to connect a lot of transducers to the automobile parts and having to test components unless they are suspicious. And the vehicle does not have to be disassembled during testing.

Eventually the Army would like such systems in its motor pools for the repair of all Army vehicles, including tanks. Tank repairs would also include diagnosing problems with tank weapon systems—infrared sensors and laser rangers.

Besides being brought up to date on American progress with diagnostic systems, the audience of Session 60 will hear Germany's Bosch system described by D. Pohl and an Italian system built by Magneti Morelli discussed by Mario Armand-Pilon.

Audio interface with computers is the subject of Session 2, "Voice Answerback Comes of Age." Since the first developments of the early 1960s, voice answerback in computer systems—the so-called talking computer—has increased sharply in use. According to Tom Fisher, chairman of the session, this reflects advances in both hardware and applications. Vocabularies have grown, he notes, and voice quality is at an acceptable point for the human ear.

The panel members of this session describe a spectrum of uses for talking computers, including telephone messages, the computer instruction of students and banking operations.

Robert Bence, director of planning for Southwestern Bell, St. Louis, describes the telephone applications. In 1965, he notes, the first system, an IBM audio-response unit, was installed to intercept messages and let a person making a phone call know that the number he was dialing had been changed or disconnected. In this application the operator asks the caller the number he's calling, and then keys it into a computer with a Touch Tone pad. From that point on, the computer takes over. It searches its files to determine the status of a phone number and then directs the audio-response unit to form a message to the caller. The message is formed, Bence says, from words and phrases that are 520 ms long and are stored on a magnetic drum.

Voice computers in action

Andrew Benkovich, another member of the panel and supervisor of analysis and programming for Emery Air Freight, Wilton, Conn., discusses the tracking of shipments. Before a voice-answerback system was installed, he says, status information on shipments was requested and received by terminal. With the talking computer, he notes, it is now possible to call the computer from any Touch Tone telephone, key in a shipment number and have the computer describe the status of that shipment. This is particularly useful for customers who wish to track their shipments directly without having to go through an Emery office, Benkovich emphasizes.

Like the system used by Southwestern Bell, the Emery system uses prerecorded phrases, but instead of using a magnetic drum, it uses a special audio disc. The system, made by Para-Phonics Corp., Bohemia, N.Y., can accommodate up to 2000 phrases, Benkovich says. Each phrase has a time factor recorded with it, so that when the phrases are tacked together and played back, the message sounds natural. The message is not choppy, Benkovich notes; it sounds so good, that it can't be discerned easily from a normal voice.

In addition to giving information about shipments, the system instructs a user on how to operate the system. It tells him what information to enter via the Touch Tone pad and when.

Robert H. Rogers, senior vice president of the City National Bank, Bridgeport, Conn., has high praise for talking computers. "It is the cheapest and easiest system to use and makes every telephone a computer terminal," he reports, adding that customers have shown wide acceptance of it.

Voice answerback computer systems are not limited to business. George Schramm, a member of the technical staff at Bell Laboratories, Holmdel, N.J., notes that it can also be used to drill students. In discussing such a system, he notes that a kindergarten class in one Red Bank, N.J., school has been taught reading and vocabulary.

Each student dials in his name. The computer then looks up his file and determines where to start instruction for that student. The computer tells the student to turn to a particular page in a workbook and begins to ask him questions about material on that page. The student answers by pushing buttons on the telephone. When the student reaches a certain level for each drill, he advances to the next drill set.

The system used for this work, Schramm reports, is made by the Cognitronics Corp. of Mount Kisco, N.Y. Audio information is coded and stored on an optical film, which is wound around a drum. The information is read out with a photodiode. The drum holds 200 words and provides a worst-case access time of 1.5 seconds.

As for other work in this field, Schramm notes that Bell Laboratories is also working on a system that would not only output audio information but could also use audio as an input.

Advanced hardware

The influence of hardware on computer architecture is the subject of Session 21, "Advanced Hardware." Of particular interest is a paper by Ronald Brody, a senior programmer for the Burroughs Corp., Paoli, Pa., in which he tells how the performance of computers can be improved.

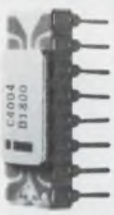
It can be done, Brody notes, by using a machine that can also support a high-level language. In practice, the computer is monitored during operation. A statistical program determines where the computer spends the most time, and the programmer can then go back to the designer and request special microprogram coding to improve the efficiency of the machine.

"By fine-tuning the hardware in this manner, a tenfold increase in throughput is possible," says Brody.

Several other developments and their effects on architecture are discussed by John T. Lynch, director of advanced development for Burroughs and chairman of the session. One of these is the Josephson junction —a very fast, low-power switch that operates at cryogenic temperatures.

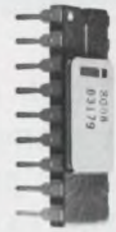
While the application of Josephson devices is still a long way off, Lynch feels they will be used eventually in computers. If this is the case, he continues, the high-speed capability of the Josephson junction will create a trend toward centralization again. ■■

THE MICRO COMPUTERS



Intel's 4004 4-bit central processor typically replaces about 90 TTL MSI and SSI packages. It's the heart of the MCS-4 set of four micro computer devices—which includes a 2048-bit ROM with a 4-bit I/O port, a 320-bit RAM with a 4-bit output port and a 10-port shift register for I/O expansion. They fit together without any interfacing circuitry to make complete systems with 32K bits of ROM and 5K bits of RAM. Using a few simple interfacing devices, you can build much larger systems with up to 96K bits of ROM.

Intel's 8008 8-bit central processor typically replaces about 125 TTL MSI and SSI packages. It's the heart of the MCS-8 micro computer set—which includes standard Intel ROMs, RAMs and shift registers. The central processor can directly address 16,000 8-bit bytes stored in any combination of these memory devices. The processor has interrupt capability, operates asynchronously or synchronously, and can perform as many as seven nesting sub-routines. Systems require some interfacing circuitry.



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INFORMATION RETRIEVAL NUMBER 66

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This snow cat carries a Ruggednova interfaced with two radar systems to help map the Canadian glacial fields.

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INFORMATION RETRIEVAL NUMBER 67

FOCUS on Pulse & word generators

Quick pulses can be elusive. Unless you're used to working with them, they're hard to find and even harder to hold: Fast rise times don't last long in a casual test setup.

Often as elusive as the pulse itself is the information needed to specify a pulse source—information that is either missing completely from a pulse or word-generator spec sheet or, if present, stated ambiguously. Competition spurs manufacturers to write specs that make their units look as good as possible. And no pulse generator is perfect.

Stray capacitance, lead inductance, variation of impedance with frequency and other factors combine to degrade an otherwise perfect pulse of voltage or current—that is, one that possesses perfectly flat upper and lower levels and that attains those levels in zero time.

When you check a spec sheet, you'd like to know what kind of pulse or pulse train you're being offered, just how the pulse departs from perfection. Levels, transition times, pulse widths and repetition rates are the characteristics that rank high in importance, so you'll probably want to check these first.

Maximum rep rate has become an almost universal figure of merit for pulse generators. Consequently when you're looking at a unit, the first question you usually ask is, What's its rep rate? High rep rate is needed in many cases—to verify the maximum toggle rate of IC flip flops, for example. But at 500 MHz, a pulse train can look strangely sinusoidal.

In most applications, however, rise time will be more important than rep rate. You'll be interested, for instance, in transition times when you're measuring propagation delay and the switching times of digital circuits. If you work with ECL or Schottky TTL, you'll be looking for especially fast rise times. And that's when you will run into your first problem.

Of course, it's meaningless to list rise and fall times without stating the points between which they're measured. But many spec sheets do just that. Or the spec sheet lists the rise time (t_r) between nonstandard points so you can't make comparisons. It's generally accepted that t_r should be the time interval for a change from 10 to 90% of the flat-top amplitude.

While a 500-ps rise-time spec is impressive, you may not get that speed across your load. Remember that like the other pulse parameters, t_r is specified at the generator output jack. Your load, and the hookup from generator to load, aren't taken into account. A couple of picofarads of stray capacitance or the inductance of a small length of wire can destroy that subnanosecond rise time or radically alter the waveshape. So know your load and ask: For what load is the t_r specified?

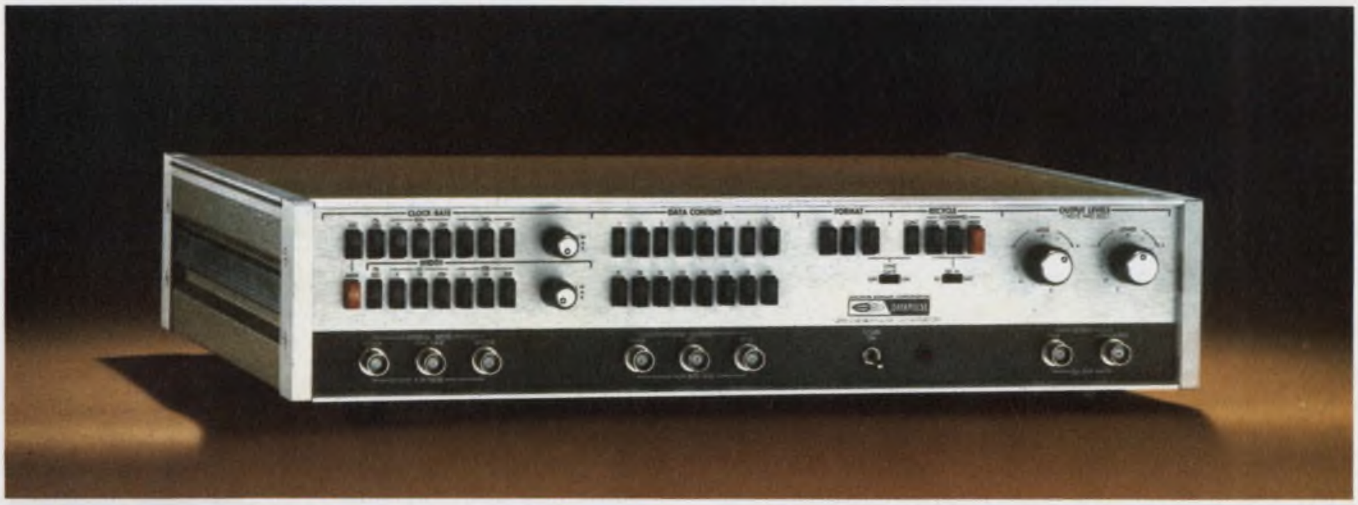
If you're looking at rep rate rather than t_r, make sure the maximum rate given isn't for a double-pulse mode. The double-pulse spec can make the generator appear twice as fast as it really is.

Tradeoffs: 30 V or 1 ns?

Because rise time, amplitude, pulse width and duty cycle are interdependent, you've really got to examine them together. This creates another specifying problem.

Spec sheets often give impressive minimum rise times and maximum amplitudes. What you aren't told, though, is that you can't get both simultaneously. And the same thing happens for other combinations such as pulse width and rise time, amplitude and offset, etc. But there's an

Stanley Runyon
Associate Editor



Datapulse Division's Model 218 operates as both a pulse and data generator at rates to 50 MHz. Output is a 16-bit word in simultaneous, positive true and complement form. The unit costs $925.

important exception: In some cases the minimum t_r can be met only at full output, where the effects of the attenuator are zero. Because these various pairs of specs are mutually limiting, you've got to make tradeoffs—even though the spec sheet "seems" to deny this.

Your first tradeoff is usually amplitude for rise time, duty factor and rep rate. Kilovolt pulses with nanosecond t_r's are available—but at extremely low rep rates and duty cycles. One-GHz pulses are also available—but you'll have to settle for 2 V of amplitude. In between, where most applications lie, are the following: medium to high-speed pulses, with 5-V amplitudes into 50 Ω, t_r's of 1 to 2 ns and rep rates in the area of 100 to 250 MHz, and low rep-rate pulses—to 50 MHz—with 10-V amplitudes and t_r's of about 5 ns.

The amplitude-rise time tradeoff creates problems for engineers working with some types of

The 1900 series is Hewlett-Packard's plug-in pulse/data generator system. A variety of mainframes and plug-ins offer variable functions of pulses to 125 MHz, four-phase outputs and pseudorandom sequences.

MOS. The required combination of high amplitude, moderately fast rep rate and fast rise time—working into a capacitive load—isn't readily available.

When you check a pulse generator's amplitude rating, also check the load for which the rating is valid. When present in the specs—and often it's not—it's usually a purely resistive 50 Ω. When missing, it could be anything up to an open circuit. Check also to see if the voltage varies with changes in rep rate, width, temperature, line voltage or other parameters.

Pulse amplitude also depends on the starting point of the pulse—the baseline. In "fixed-offset" units, the baseline is usually assumed to be zero. But it may not be. It's also assumed that whatever level the baseline is at, it remains constant. This also may not be true. Changes in load, amplitude, duty cycle and other parameters can cause a small but finite baseline shift. Most spec sheets ignore this. Another point: If the generator provides simultaneous positive and negative pulses, see if the pulses start from the same baseline. They may not.

E-H Research Laboratories' Model 137 features a rep rate of 100 MHz, variable rise and fall ramps from 0.5 ns/V to 40 μs/V and variable baseline offset to ±5 V. Delay and width are also variable.

Interaction is unavoidable

In units that offer variable baseline offset, the baseline setting can affect the pulse amplitude (and vice versa), and possibly the pulse shape. This interaction can be important when you want, say, a 200-mV pulse riding on a 10-V offset level. (You'll need a variable baseline for testing TTL, ECL and other transistor circuits.)

The limiting interactions between some pulse generator parameters may not be apparent until you vary one of the parameters. Baseline-amplitude interaction is one example. Rise time-pulse width and rise time-amplitude are others.

Some units offer variable rise and fall times. You'll need this feature to simulate IC-device performance, to optimize pulse shapes so as to minimize ringing and reflections, and in other applications. But when you change a transition time, you automatically change the pulse width. This, of course, is to be expected from the very definition of width. What you don't expect, however, is a change in amplitude. It can happen—even though the spec sheet forgets to mention it, or passes it off as "negligible."

While investigating the effects of varying transition times, don't forget to check the linearity of the transitions. In IC testing, slope linearity may be important in obtaining repeatable, accurate results.

Other controls can interact—such as width, amplitude and rep rate. Variable pulse width is needed, for example, to measure the leakage inductance of pulse transformers. But when you vary width, can the amplitude fall? Does an amplitude change affect the width? The spec sheet should spell this out.

Interaction between pulse width and rep rate usually occurs when you inadvertently set the rep rate above the value that yields the maximum duty cycle (ratio of pulse width to period). What happens then depends on the particular generator. Some units won't allow the "illegal" setting. In others the pulse will collapse in width or amplitude. And in still others, be prepared for a little smoke.

Besides depending on width, the allowable rep rate may also hinge on the amplitude setting and the delay setting. The spec sheet should list all these limitations.

Most generators offer duty cycles up to about 50%. A few go higher—to 90%—at the lower frequency ranges. To determine the duty cycle of a pulse train, divide the pulse width by the train period. This seems easy enough. And it is—right up to the point where you try to determine the pulse width.

With a perfect pulse—a theoretical one, with perfectly vertical sides—there's no doubt as to what the width is. But with an actual pulse—one in which the sides depart from the vertical—the width varies with the measuring points. And, unfortunately, no standard exists for the measuring points.

Most manufacturers measure and specify pulse width between the 50%-of-amplitude points. But you can't assume that this is the case when widths are listed without further qualification: The 90% points may have been used.

Jitter may make you nervous

After you've determined width, don't relax. While the spec sheet may correctly tell you the width at the 50% points, there's something it may not tell—the stability of the width.

When you set a pulse width, you'd like it to keep that width. And when you set a rep rate or delay, you'd like those to remain constant, too. But they may not.

Indequate power-supply regulation, ground loops, triggering difficulties and other factors combine to cause jitter—slight variations in width, period or delay. Some data sheets don't acknowledge the presence of jitter. In others the various types of jitter are lumped together into one spec. And in still others jitter is listed as a percentage. It's left to your imagination to determine just what it's a percentage of.

A spec sheet should list each jitter separately and should state how each is defined and measured. Width jitter is the time variation between the 50% points on the leading and trailing edges. It's usually expressed as a percentage of the width setting and can be measured by triggering a delaying-sweep scope with the leading edge of the pulse and observing the maximum displacement of the trailing edge.

Period jitter refers to the time variation between the 50% points on the leading edges of successive pulses. Also expressed as a percentage of period setting, this jitter can be measured on a delaying-sweep scope by observing the displacement on a pulse downstream from the triggering pulse. Period jitter is usually greatest at maximum width and delay settings for a given rep rate.

Finally delay-time jitter should be determined. This is the variation in the time interval from the 50% point on the leading edge of an internal or external trigger to the 50% point on the leading edge of the output pulse. It's usually expressed as a percentage—but of what? Delay jitter is best measured at its maximum setting, for a given period, on a scope or time-interval meter.

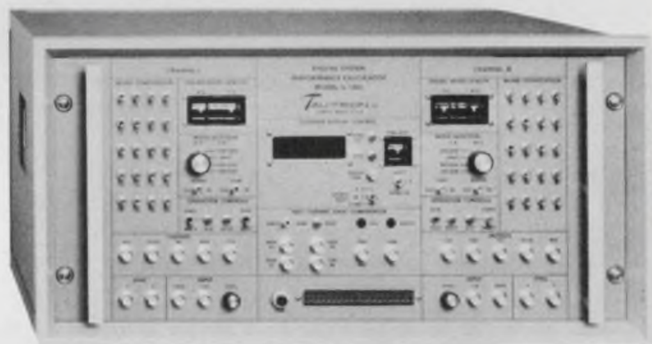
Distortion specs can be distorted

While jitter refers to variations in a pulse's time characteristics, the term "aberration" refers to a pulse's departure from the ideal waveshape. And depart it does, even though manufacturers sometimes don't acknowledge the fact.

The pulse top, for example, is rarely the flat, horizontal line of the ideal pulse. Pulse-generator imperfections combine with stray load capacitance and lead inductance to produce overshoot, ringing, pulse-top tilt (droop), rounding of edges and little excursions called preshoots. In general, the faster the rise time, the greater the possibility of overshoot and ringing. So look for greater distortion at minimum rise times.

Manufacturers tend to specify pulse-top distor-

A peak of 24 kW is obtainable from the 605P, Cober Electronics' high-power pulse generator. Minimum width of the 11-A, 2.2-kV pulse is 50 ns.



Tau-Tron's S-130 calculates the performance of digital systems, ranging from communications to memories to magnetic tapes. The unit offers ten different modes.

A range of generators are offered by Comaltest. From top, are the 610, a 2-phase unit; the 601, a 4-phase unit; and the 801, a 16-channel data generator.

Two new units from Interstate Electronics feature a constant-duty-cycle mode. The P23 has a fixed rise time of 3.5 ns, while the more expensive P25 offers variable rise and fall times down to 5 ns.

tion in various ways—when they bother to specify it at all. Some manufacturers lump the various aberrations into one distortion spec. Others break out the individual contributions from overshoot, ringing and droop. For both the lumped and individual approaches, however, specs that are listed as a percentage—without a reference—are meaningless.

Overshoot—or the first excursion past the pulse flat top—should be specified as a percentage of the flat-top-to-baseline amplitude. So should ringing, the oscillations following the overshoot. But ringing—also called ripple or perturbations—can be specified as rms, peak or peak-to-peak. Only the latter gives the true picture. The other specs, with smaller numbers just make the units look better.

Droop refers to the pulse top's slope, or departure from the horizontal. When given, it's usually expressed as the difference between the leading and trailing-edge amplitudes (top to baseline), as a percentage of either the smaller amplitude or the top's mid-level.

Other pulse aberrations include preshoots and undershoots. For a positive pulse, leading-edge preshoot is a (hopefully) small dip below the baseline that occurs just before the positive excursion. Trailing-edge preshoot, for a positive pulse, is a small positive-going pip that occurs just before the negative-going excursion. Both preshoots are specified as a percentage of the flat amplitude.

Finally, undershoot occurs when the negative-going excursion drops below the baseline and then returns to the baseline, exponentially or accompanied by damped oscillations (ringing). These should be listed as a percentage of trailing-edge amplitude.

Look into the output jack

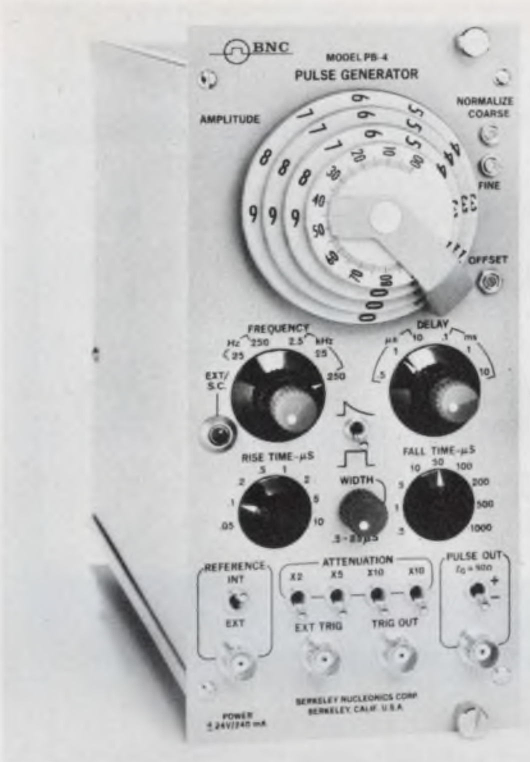
Because load can significantly affect a pulse generator's performance, it's a good idea to check a generator's output characteristics. Source impedance is a good place to start.

You'll run into a few obstacles when you check source impedance. First, it may not be specified. Second, when it is specified, you may wish it weren't.

Lacking universal standards, source impedance may be variously given as "50 Ω shunted by 20 pF, typically" or by "Model XYZ has 50-Ω impedance in attenuator position and a high impedance otherwise." Or you may get this statement: "With 1:1 attenuation, this unit operates as a current source for positive pulses and a voltage source for negative pulses." Or this one: "High-output level supplies 50 mA, low-output level sinks 50 mA."

There are several other ways of specifying source impedance, few of which offer clear, exact source-impedance figures for all modes, rep rates and transition times.

Knowledge of source impedance is important



Berkeley Nucleonics' PB-4 is a precision pulser that provides a highly linear tail or flat-top pulse.

for these reasons: First, a close impedance match between source and load is desirable to avoid reflections that can destroy pulse waveshape. Assuming a 50-Ω load, 50-Ω cables hooking the load to a 50-Ω source will minimize this problem. Many generators therefore have an internal 50-Ω termination, or use backmatching to clean up reflections.

Second, when working with TTL, you'd like to know that a generator's output impedance doesn't prevent necessary current sinking at the logic-ZERO voltage level. Third, if you're mixing the outputs of several generators, or driving devices with an impedance that changes radically during switching, you'll want a low-shunt-capacitance current source, not a 50-Ω source.

Some generators offer a switch-selectable impedance: 50-Ω or high-impedance—whatever "high" means. With these generators, it's wise to check the key specs at each impedance.

Finally, it's also wise to determine what happens when you short—or open—the output jack. Are the outputs protected against these conditions? And what happens when you apply voltage across or pump current into the output: Does a $90 transistor burn out? While you're at it, ask this: Is there some combination of control settings that can damage the instrument? If there is, does the instrument warn or have built-in protection against this possibility?

After you check a generator's key specs, you'll probably look into other capabilities—features that make the unit more versatile or are needed for a specific application. These include various output, gating and triggering modes; programming characteristics; t_r/t_f control and interchangeable plug-in modules.

The extras that enhance versatility

Most general-purpose pulse generators offer a trigger output plus control of pulse timing from either an external or internal trigger. The former is useful for triggering a scope with the generator or for synchronizing several generators.

But to avoid headaches when triggering one generator from a similar one, you'd like the input and output trigger to be identical. So watch for specs that call for an input trigger of 5 V but list an output trigger of 1.5 V. Or for those that have triggers of opposite polarity. Other things to investigate are requirements for trigger transition times, width and rep rate, as well as the amount of delay between input and output.

In a gating mode, pulses are produced only during the interval when an external signal is applied to the input jack. This mode is useful in applications requiring pulse bursts.

Other useful modes include the following: single-cycle, in which one pulse is generated each time a pushbutton is depressed; double-pulse mode, in which closely spaced pulse pairs are emitted; and the simultaneous complementary-output mode, useful for logic testing.

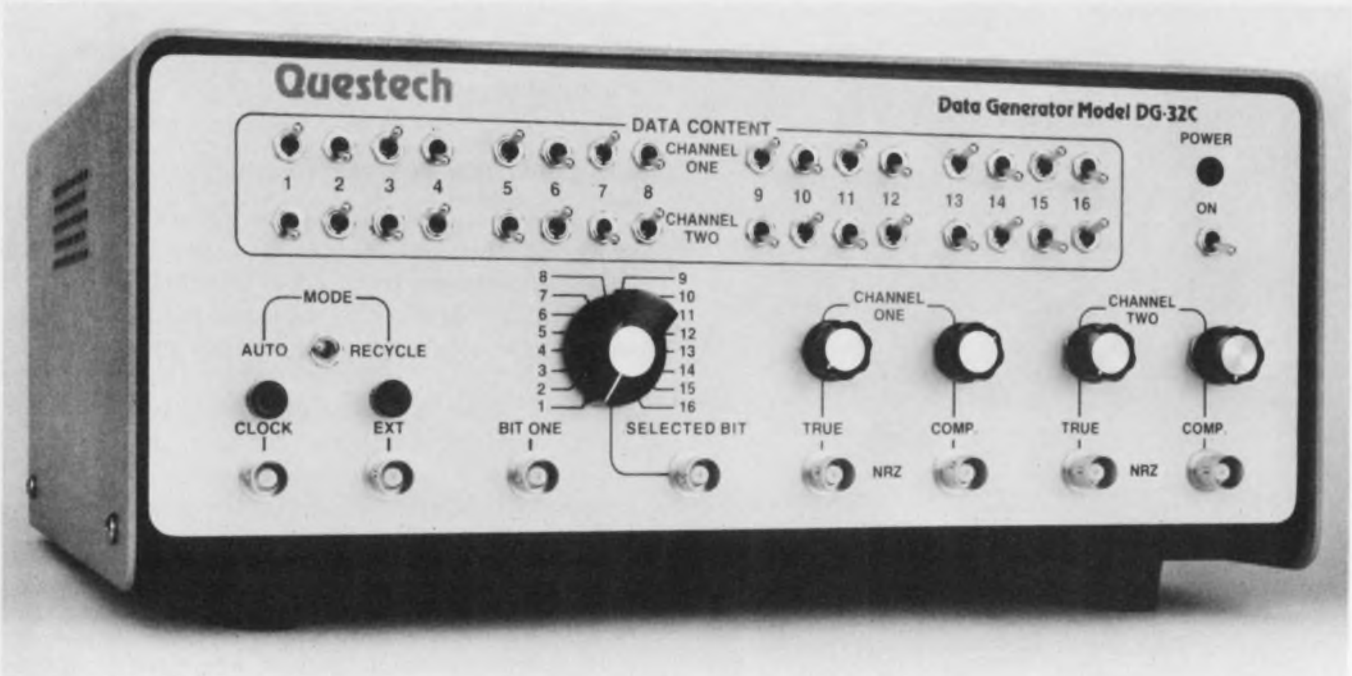
These extra features—plus variable baseline, variable transition times and others—can each cost a few hundred dollars. So check your present—and future—requirements carefully.

If you're working in the growing field of automatic test systems, you'll probably be looking into programmable pulse generators. Many generators with front-panel manual controls also offer programming through rear connectors. Other generators are designed especially for programming and have a blank front panel—except, of course, for a pilot light and power switch.

In addition to the key specs, you'll want to know about those dealing with programming. Some spec sheets skimp on the details.

For example, is the programming format binary or BCD? How many lines are needed to control the generator functions? Which functions are controllable? What about control voltages and drive currents—what levels, transition times and source impedances are required? Are the inputs TTL-compatible, or what? Is positive logic or some other type used?

And that's not all. Some spec sheets forget to tell you that you can't drive the generator directly from your computer—you've got to build an interface first, with buffering, storage, or both. Others may forget to tell you about switching



The DG-32C is Questech's 10-MHz data generator. The unit offers two, 16-bit channels, in both true and complement form. Bits are independently selectable and modes include continuous and single bit or word.

transients and settling times—information you need to determine how fast you can change an output.

Here are other questions to ask: Within what error band can I set the pulse parameters? How closely can I repeat a given setting?

The word generator: A specialized pulser

Although called by other names, many special-purpose instruments are actually pulse generators sharing the same problems as the general-purpose units, as well as having some of their own.

Some examples: Multiphase generators provide up to eight (or more) independent pulse outputs. They're used for testing of dynamic MOS devices. Square-wave generators are pulsers with a fixed duty cycle of 50%. And digital delay generators provide precise delays between an external trigger and the output pulse.

Another class of pulse generator—one that's growing in importance—is the word, pattern or data generator.

Word generators simulate the binary patterns needed to test digital communication systems, computers and other equipment using digital logic or devices.

Unlike traditional pulse generators, which emit a repetitive output, data generators can add or subtract pulses within a repetitive sequence. Some—called pseudorandom generators—produce long, statistically random words. Others are used as character generators or pulse-code modulation (PCM) simulators.

Whether the data generator is general or special purpose, its important specs include clock rate, output format, word length and the number of channels. But when you investigate these, don't forget the specs you'd check on a conventional pulser—specs like rise time, impedance, tempco and aberrations. Indeed, some units are offered as being both data and pulse generators, having simultaneous pulse and data outputs.

Many data generators require an external clock to trigger, time or synchronize the bit patterns. Some offer an internal clock. In either case the rate of the output bit pattern depends on the clock rate. Check for other clock requirements, besides rate: Minimum and maximum widths, source impedance and amplitude are usually important. Check also for delay times between clock input and data output.

Format codes vary, depending on the area of logic design and data shuffling. The most common are the nonreturn-to-zero (NRZ) code, with variations, and the return-to-zero (RZ) code. In the NRZ, a ONE is represented by a high level, while a ZERO is a low level. In the RZ a ONE is represented by a "short" pulse, and a ZERO by no pulse. If RZ is what you need, investigate the minimum and maximum widths of the ONE pulse.

Other format codes exist as well. To capture a larger market, some word generators offer switch-selectable formats, others a fixed format.

Word length is another spec of prime interest. Some generators offer a fixed length of, say, 16 bits, while others provide a variable bit length—three to 10 bits, for example. Some units offer bit expansion capability. In all types the content of a word is usually selected by front-panel switches—one per bit—or, when offered, by programming via a rear connector.

To further increase versatility, multiple, independent channels are offered on some generators, as well as simultaneous true and complementary data. Word outputs can come in serial or parallel form. Also, some of the newer generators are microprogrammable, containing an internal memory that can be altered.

Other available features include repeat or recycle frame formats and output pulses to synchronize the clock, a selected bit or the start and end of a word or frame.

To control the many functions and modes, you'll find a maze of switches, dials, jacks, indicators and possibly even a counter. Look for logical grouping of controls and indicators, so that you don't need an instruction manual each time you use the unit. And, as with any pulse generator, watch for interactions between controls.

Other things to watch for: delays between pulses that are "synchronized" and fixed delays between sequential words—for example, a fixed ZERO between patterns.

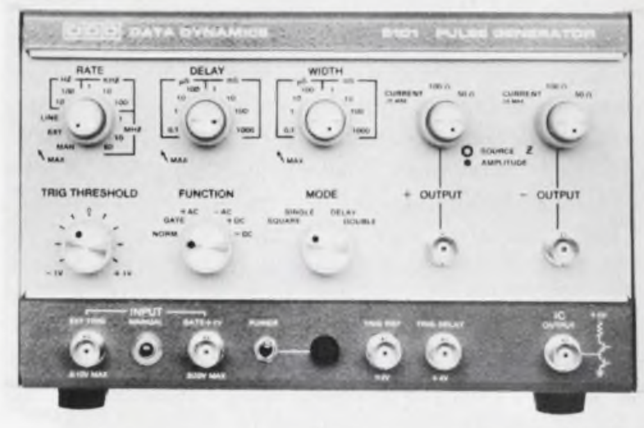
From $165 to $45,000

You can get a pulse generator for as little as $165 or as high as $45,000. Generally, as price goes up, rise time gets faster, rep rate and amplitude go up and waveshape tends to get cleaner. Reliability usually improves, too. But it's always best to get a unit into your lab to check it for performance and workmanship.

Features such as variable rise and fall times, baseline offset, gating and double pulse can cost $200 to $400 each. Higher amplitude can cost up to $1000 extra. But if you don't take the options and you eventually need any of the features in a future application, it'll cost you more to buy a second generator just for those features.

If you use pulses only occasionally, perhaps a function generator will fulfill your need while providing additional waveshapes for other purposes. But, in general, you'll be looking at units that are strictly pulse sources. Let's look at what's available.

The Data Dynamics Div. of Electronic Counters, Inc., offers a number of general-purpose pulse generators. The company's top-of-the-line unit is the 5113, a 50-MHz generator with in-



Outputs of the Data Dynamics' 5101 include positive and negative pulses to 50 MHz, double pulses and a separate output to test TTL, RTL or DTL ICs.

dependently variable rise and fall times ranging from 6 ns to 5 ms. Maximum amplitude of the 5113's simultaneous positive and negative pulses is 10 V into 50 Ω. The baseline is variable from ±2 to ±10 V. The unit sells for $980.

Other Data Dynamics units include the 5101, a 3-ns, 50-MHz unit that goes for $550, and the 5105, a 5-MHz generator with plus-and-minus 20-V outputs, selling for $350.

The Datapulse Div. of Systron-Donner offers close to 20 different pulse generators, more than a dozen data generators and a line of programmable pulse generators. The company's models include the "economy" 88 and 99—20-MHz, 7-ns units that output 5 V maximum into 50 Ω and sell for $395—and the Models 115, 116 and 117—50-MHz units selling for $600, $850 and $750, respectively. The 116 has both variable offset (to ±2.5 V) and transition times (from 5 ns to 0.5 s) while the 117 has variable transition time only.

With Datapulse's PicoPulser concept, a small thin-film hybrid package is placed directly at the load and is driven from an external oscillator/controller. The at-the-load source eliminates long cable runs and other problems, resulting in pulses with 500-ps rise times to 0.5 GHz. The PicoPulser sells for $2750, complete with controller/oscillator.

The company also offers data generators. The 218 is one of Datapulse's economy models. The $925 unit features a clock rate of 50 MHz, 16-bit word length, NRZ or RZ format and continuous, manual or external-command recycle modes.

E-H Research Laboratories' extensive pulse-generator line includes over 20 different models. The latest additions to the line include five models. The 122A is a 250-MHz unit, with rise and fall times of less than 1 ns, a maximum amplitude of ±5 V into 50 Ω, variable offset to ±2.5 V and better than 50% duty cycle. The model sells for $2875.

E-H's Model 129 is one of the fastest available pulsers. Its maximum rep rate is 500 MHz, and its transition times are less than 500 ps. Other features include an output of up to 2 V into 50 Ω, variable baseline offset (−1 to +1 V into 50 Ω) and 50% maximum duty cycle. The price of the Model 129 is $3925.

Variable rise and fall times are offered in E-H's 50-MHz Model 135A and 100-MHz Model 137—the former from 3 ns to 8 ms and the latter from 2 ns to 160 μs. The 135A outputs ±10 V into 50 Ω and has variable offset to ±5 V; it sells for $1595. The 137 outputs ±5 V into 50 Ω, has ±5 V variable offset and costs $1950.

The 1501 is E-H's newest programmable pulse generator. Lacking manual control, the 50-MHz unit provides full control of all pulse parameters by coarse and fine programming through parallel lines. Features include output to 10 V, rise time to 3 ns, variable offset and polarity inversion. The 1501 sells for $3500.

Hewlett-Packard manufactures an extensive line of general-purpose pulse generators, square-wave generators, programmable pulsers and word generators.

You can test digital data communication systems with International Data Sciences' Model 1310. The unit generates pseudorandom start-stop characters.

One of HP's newest developments is the 8007B, a 100-MHz pulser with independently variable rise and fall times from 2 ns to 250 μs. The linearity of the transition slopes is better than 3% above 20 ns. The amplitude can be set to ±5 V and offset to ±4 V (into 50 Ω). The 8007B costs $1750.

HP's 8008A gives two simultaneous, complementary outputs that zip along at up to 200 MHz. Pulse transition times are less than 1.2 ns, and the maximum duty cycle exceeds 50%. Both amplitude and offset can be set, the former to ±4 V into 50 Ω and the latter to ±2 V into 50 Ω. In addition there's a fixed ECL output of −0.9 to −1.7 V. The price: $2700.

The 1900 series is HP's plug-in pulse-generator system. Two mainframes—a high-power ($850) and a medium-power ($565) unit—and at least 16 plug-ins are offered. Two plug-ins are for rate generation, six for timing and word generation and eight for interfacing and output.

Significant specs and features of the system include rep rates to 125 MHz and delays of 15 ns to 10 ms; two to 16-bit words in RZ or NRZ; pseudorandom binary sequences (PRBS) to 50 MHz; and a four-phase clock. Width, transition times, polarity, offset and amplitude are controlled by the particular output module. The outputs of the 1900 range to 50 V t_r's to 350 ps, while prices go from $215 to $1975 for the plug-ins.

The 3760A is HP's latest data generator. Its specs include rates to 150 Mb/s, variable word length to 10 bits and PRBS to $2^{15}-1$ bits. Both true and complementary outputs are given in switch-selectable RZ or NRZ format. The amplitude can be set to 3.2 V, the offset to ±3 V. Transition times of the 3760A are less than 1 ns.

The Interstate Electronics Corp. has recently introduced its Series-20 pulsers, two 50-MHz units that feature a constant-duty-cycle mode. The mode maintains the relationship between pulse width and period regardless of changes in rep rate.

Two units are currently offered by Interstate: The P23, with a fixed rise time of less than 3.5 ns, and the P25 with adjustable t_r and t_f down to 5 ns. Both units have simultaneous positive and negative pulses to 10 V into 50 Ω and complements. The P23 is priced at $625 while the P25 sells for $995.

Tau-Tron, Inc., specializes in high-speed digital-communications test equipment, digital signal sources and semiconductor memory test systems.

The company's DG-7 digital signal generator is both a pulse and data generator. As a data unit, the generator provides 16-bit words in RZ or NRZ format at up to 35-MHz bit rate.

As a pulse generator, the DG-7 offers variable width from 15 ns to 10 ms, variable amplitude to 5 V into 50 Ω and variable offset to ±2 V into 50 Ω. Rise and fall times are fixed at 7 ns maximum. The price of the DG-7 reflects the general trend toward lower costs for data generators—the unit sells for $695, with an internal clock.

Tau-Tron's DG-525 data generator is one of the fastest available—it can shoot out data at over 300 Mb/s. The word length is either 16 or 32 bits, depending on the model, and the format is either RZ or NRZ. An external clock is needed. The 16-bit DG-525L sells for $4365.

To test digital communication systems, Tau-Tron offers its S-130. This 130-MHz unit can function as a pulse generator with variable width and delay; as a variable-length word generator to 20 bits/word; as a bit-error-rate counter; and as a pseudorandom generator. With a single channel and an error counter and display, the S-130 sells for $4950.

Special-purpose units abound

Many companies make just word generators or pulse generators intended for one or a limited number of applications.

For example, Comaltest, Inc., offers its Models 601 and 610—four-phase and two-phase generators, respectively, designed specifically to test and characterize MOS circuits. The company also offers the 801, a 16-channel data generator with bit rates to 12 MHz.

International Data Sciences manufactures the Model 1310 TDM-Modem Test Set, a pseudorandom word generator used to test digital data transmission systems at up to 0.5 Mb/s. The unit sells for $2150.

Questech's DG-32C is a two-channel data generator with a 16-bit word, 10-MHz rep rate, single-bit or word-repeat modes and simultaneous true and complementary NRZ outputs. Each bit can be independently selected. The price is $1975.

Miida Electronics offers the Takeda Riken TR-4200 Series, a unit whose 1-GHz rep rate makes it the fastest available pulse generator and whose $45,000 price makes it perhaps the most expensive on the market. The TR-4200 has a t_r of less than 300 ps, a t_f of less than 200 ps and peak amplitudes of ± 2 V into 50 Ω. Plug-ins are offered to control pulse width, to generate pseudorandom noise sequences and to generate word patterns. The quoted price includes all plug-ins.

Cober Electronics offers a line of high-power pulse generators. The company's Model 605P outputs up to 24-kW peak at 1.5% duty factor. It costs $3990.

The Velonex Div. of Varian manufactures high-power units only. Latest offerings from Velonex include the Model 340, a 5-kW, 1%-duty-factor unit that sells for $1990, and the 370, with 11-kW peak output at 5% duty cycle. The 370 costs $5750.

Other companies offering special-purpose units include Berkeley Nucleonics, a manufacturer of precision digital delay units; Bicron Electronics, with a multipulse delay line tester, and Dranetz Engineering Laboratories, offering a digital gating/timing generator. ■■

Need more information?

The products cited in this report don't represent the manufacturers' full lines. For additional details, check the appropriate information retrieval number:

Adar Associates, Inc., 85 Bolton St., Cambridge, Mass. 02140. (617) 492-7110. (F. J. Bigda) **Check 399**

American Time Products, Bulova Watch, 6120 Woodside Ave., Woodside, N.Y. 11377. (212) 335-6000. (R. Ansell) **Check 400**

Applied Microwave Laboratory, 411 Providence Hwy., Westwood, Mass. 02090. (617) 329-1500. (Herbert Clark) **Check 401**

Berkeley Nucleonics Corp., 1198 10th St., Berkeley, Calif. 94710. (415) 527-1121. (Mel Brown) **Check 402**

Bicron Electronics Co., Box 807, Canaan, Conn. 06018. (203) 824-5125. (John Wallace) **Check 403**

Bowmar/ALI, Inc., 531 Main St., Acton, Mass. 01720. (617) 263-7756. **Check 404**

Chronetics, 500 Nuber Ave., Mount Vernon, N.Y. 10550. (914) 699-4400. (Sid Gordon) **Check 405**

Cober Electronics, Inc., 7 Gleason Ave., Stamford, Conn. 06902. (203) 327-0003. (Bill Zarkower) **Check 406**

Comaltest, Inc., Commerce Drive, Danbury, Conn. 06810. (203) 792-3777. (Peter Quinn) **Check 407**

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Disc Instruments, Inc., 2701 S. Halladay St., Santa Ana, Calif. 92705. (714) 549-0343. (E. L. McElroy) **Check 410**

Dranetz Engineering Laboratories, 2385 S. Clinton Ave., South Plainfield, N.J. 07080. (201) 755-7080. (Abraham I. Dranetz) **Check 411**

EG&G, Inc., 35 Congress St., Salem, Mass. 01970. (617) 745-3200. (S. Rubinovitz) **Check 412**

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Exact Electronics, Inc., Box 160, Hillsboro, Ore. 97123. (503) 648-6661. (Ronald T. Hill) **Check 415**

General Radio Co., 300 Baker Ave., Concord, Mass. 01742. (617) 369-4400. (Karl Alsen) **Check 416**

Gralex Industries, 155 Marine St., Farmingdale, N.Y. 11735. (516) MY-4-3600. (Mike Neidich) **Check 417**

Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, Calif. 94304. (415) 493-1501. **Check 418**

ILC, Inc., 164 Commercial St., Sunnyvale, Calif. 94086. (408) 738-2944. (Harvey Berger) **Check 419**

International Data Sciences, 100 Nashua St., Providence, R.I. 02904. (401) 274-5100. (Raymond B. Sepe) **Check 420**

Interstate Electronics Corp., 1001 East St., Anaheim, Calif. 92803. (714) 772-2811. (Patricia O'Leary) **Check 421**

LVC Industries, Inc., 135-25 37th Ave., Flushing, N.Y., N.Y. 11354. (212) 939-9777. (L. Cartelli) **Check 422**

Linear-Digital Systems, Box 954, Glenwood Springs, Colo. 81601. (305) 945-6122. **Check 423**

Marconi Instruments, 111 Cedar Lane, Englewood, N.J. 07631. (201) 567-0607. (Keith Elkins) **Check 424**

Microwave Control Co., Box 627, Farmingdale, N.J. 07727. (201) 681-7770. (Robert Sepulveda) **Check 425**

Miida Electronics, 2 Hammerskjold Plaza, New York, N.Y. 10017. (212) 973-7152. (Thomas C. Odderstol) **Check 426**

Moxon, Inc., SRC Div., 2222 Michelson Dr., Newport Beach, Calif. 92664. (714) 833-2000. (D. J. Romrell) **Check 427**

Non Linear Systems, Box N, Del Mar, Calif. 92014. (714) 755-1134. (Lou Niemann) **Check 428**

PRD Electronics, 1200 Prospect Ave., Westbury, L.I., N.Y. 11590. (516) 334-7810. (Wally Weisman) **Check 429**

Panametrics, Inc., 221 Crescent St., Waltham, Mass. 02154. (617) 899-2719. (Doug Spooner) **Check 430**

Questech, 385 Putnam Ave., Hamden, Conn. 06514. (203) 288-2591. (Richard M. Ross) **Check 431**

Scientific Measurements, 2945 Central, Wilmette, Ill. 60091. (312) 256-0148. (R. A. Karlin) **Check 432**

Singer Co., Palo Alto Operation, 3176 Porter Dr., Stanford Industrial Park, Palo Alto, Calif. 94304. (415) 493-3231. (Wally Burton) **Check 433**

Systron-Donner, Datapulse Div., 10150 Jefferson Blvd., Culver City, Calif. 90230. (213) 836-6100. (H. W. Mette) **Check 434**

Tau-Tron, Inc., 685 Lawrence St., Lowell, Mass. 01852. (617) 458-6871. (J. J. Slomski) **Check 435**

Tektronix, Inc., P.O. Box 500, Beaverton, Ore. 97005. (503) 644-0161. (Earl Music) **Check 436**

Test & Measuring Instruments Inc., 224 Duffy Ave., Hicksville, N.Y. 11802. (516) 433-8800. (Al Katz) **Check 437**

Vega Precision Laboratories, 800 Follin Lane, Vienna, Va. 22180. (703) 938-6300. (D. M. Kruchko) **Check 438**

Velonex Div. of Varian, 560 Robert Ave., Santa Clara, Calif. 95050. (408) 244-7370. (Elliott Rudee) **Check 439**

Wang Laboratories, Inc., 836 North St., Tewksbury, Mass. 01876. (617) 851-4111. (Roland Boisvert) **Check 440**

INFORMATION RETRIEVAL NUMBER 70

Write a Fortran wire-listing program

that allows easy data entry, error checking and a variety of printouts. Thousands of nodes can be handled.

Computerized wire lists afford two important benefits: lowered labor costs and a minimum of errors. But to achieve these benefits, the designer must pay strict attention to the design of the wire-listing program.

A carefully prepared Fortran program that generates complete wire lists can easily be operated by a single technician and a typist. The type of program described here is modular and provides numerous self-checking features at each step of data preparation.

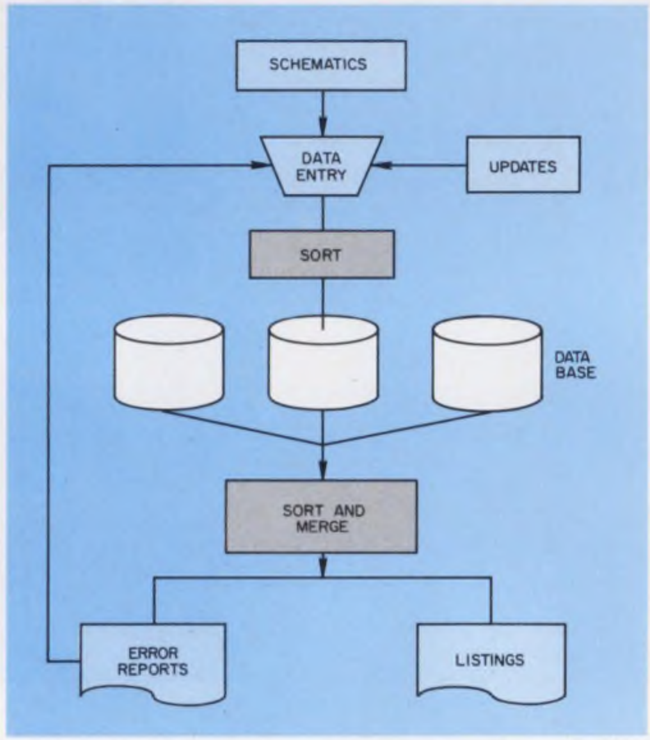
The program employs the idea of a signal chain in which each signal node—terminal, socket pin, etc.—appears once in the central data file, along with the name of its associated signal chain. Sorting, by signal name and node, arranges the data into a form suitable for "from-to" listings. It is assumed that the user's computer system has the necessary equipment and software for alphanumeric sort and merge procedures. Therefore details of the sort and merge programming are not given here.

Organization of input data

As shown in the flow chart of Fig. 1, the program generates error listings and reports from a central data base—usually discs. To assemble the data base, a technician first prepares termination sheets by systematically entering information derived from the electrical schematics (Fig. 2). The typist then transfers the information from the termination sheets to the input file (discs or other storage media). Each line entered into the computer, contains five fields, the first being a sequence number assigned by the typist for later reference.

A given circuit node is identified by a set of data fields, that label the chassis, connector ("conn.") and pin number ("pin no."). The fourth field, "signal name," contains a unique mnemonic to identify the signal chain, and the "notes" field allows for further identifying of data where needed.

J. T. Henderson, Quality Assurance and Reliability Manager, Gulton Industries, Inc., 15000 E. Central Ave., Albuquerque, N. M. 87123.

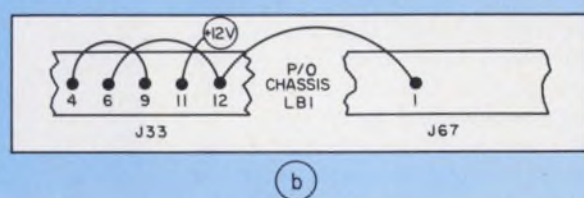


1. **Entries based on the wiring schematics** are sorted and placed in a central data base. Sort and merge operations array the data in requisite report order.

LINE NO	SIGNAL NAME	CHASSIS	CONN.	PIN NO	NOTES
905	J33-9	LB1	J33	4	
906	J33-6	LB1	J33	6	
907	J33-9	LB1	J33	9	
908	+ 12 V	LB1	J33	11	
909	J33-6	LB1	J33	12	
910	J33-6	LB1	J67	1	

NODE IDENTIFICATION OR LOCATION

(a)



(b)

2. **Each circuit node results in** a single entry on the input sheet. Chassis, connector and pin number identify the node (a). All nodes on the same signal path receive a common signal designation (b).

An example of how information is transferred from a schematic is given in Fig. 2a. Chassis, connectors and pins must be identified. It is not necessary to devise special signal names for every signal chain on the schematic. Signals that remain on the same schematic can be assigned an implied, but unique, name. For example, either J33-4 or J33-9 names the signal chain formed by the wire joining pins 4 and 9 of J33. Such is not the case for signals leaving the schematic—for example, the 12-V supply line. Designations for these signals should be circled on the schematic and shown with a name that applies across all schematics.

There are two implied names in the illustration (J33-6 and J33-9) and one given name. The six nodes shown for chassis LB1 result in six entries on the input sheet. In this example the letters FP, BP and LB stand for front panel, back panel and logic bay, respectively.

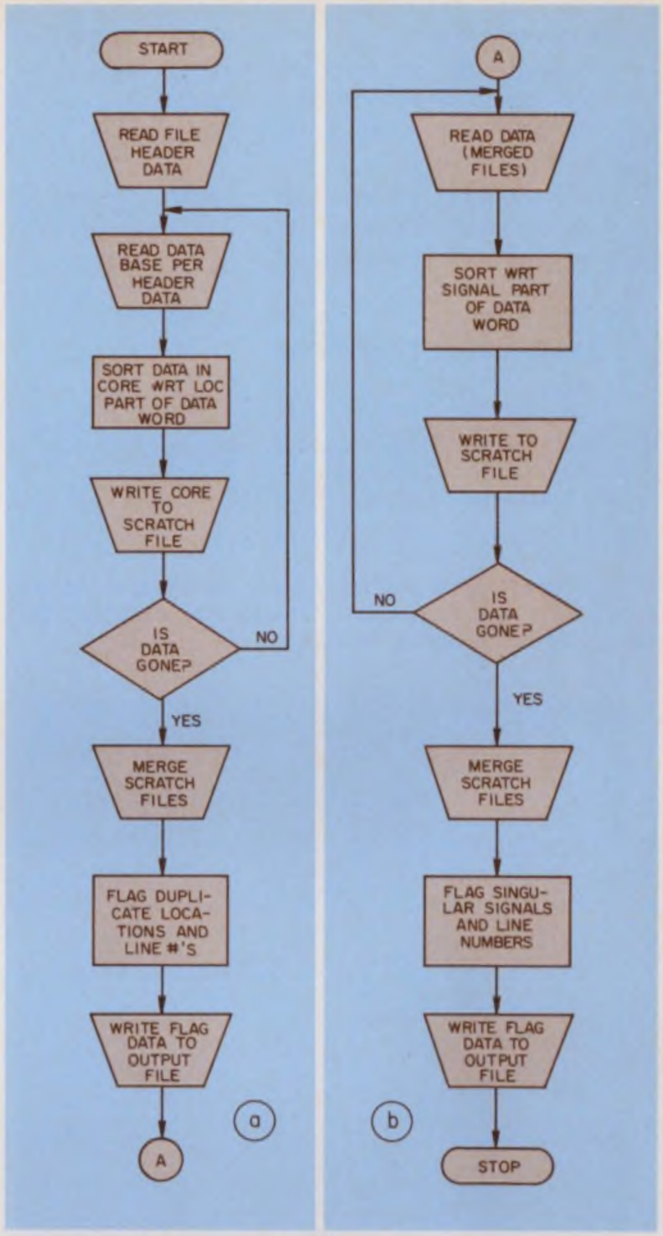
Preparing the data base

After completion of a self-checking routine, data from the input file is merged into the master file. In the checking routine, the data base is first sorted with respect to the node-location fields. Duplicate location assignments, if they exist, will then be adjacent to one another. These duplicates can be flagged and placed in a separate subfile for error listings. The input line number, if carried along with the sort, allows the technician to retrieve the erroneous entry.

A sort with respect to signal name permits flagging of all singular (unwired) nodes. Again, the presence of line numbers permits rapid access to the erroneous entry.

The final data base is stored in multiple files and sorted via several passes through the main memory. Each file can be sorted in main memory. Both error-detection programs (Fig. 3) should be rerun against the corrected data, since the introduction of new errors is possible.

A "header" preamble precedes the node location records in each file of the data base. About 100 records must be reserved for the preamble. A



3. **Sorting by node location** permits detection of multiple assignments to a single terminal (a), whereas a sort by signal name reveals unwired terminals (b). Subfiles are sorted and merged to form the central data base.

Table. Data base header

0001	0204
2	02
3	08
4	FP
5	LB1
6	LB 2
7	BP
8	1
9	2
10	3
11	4

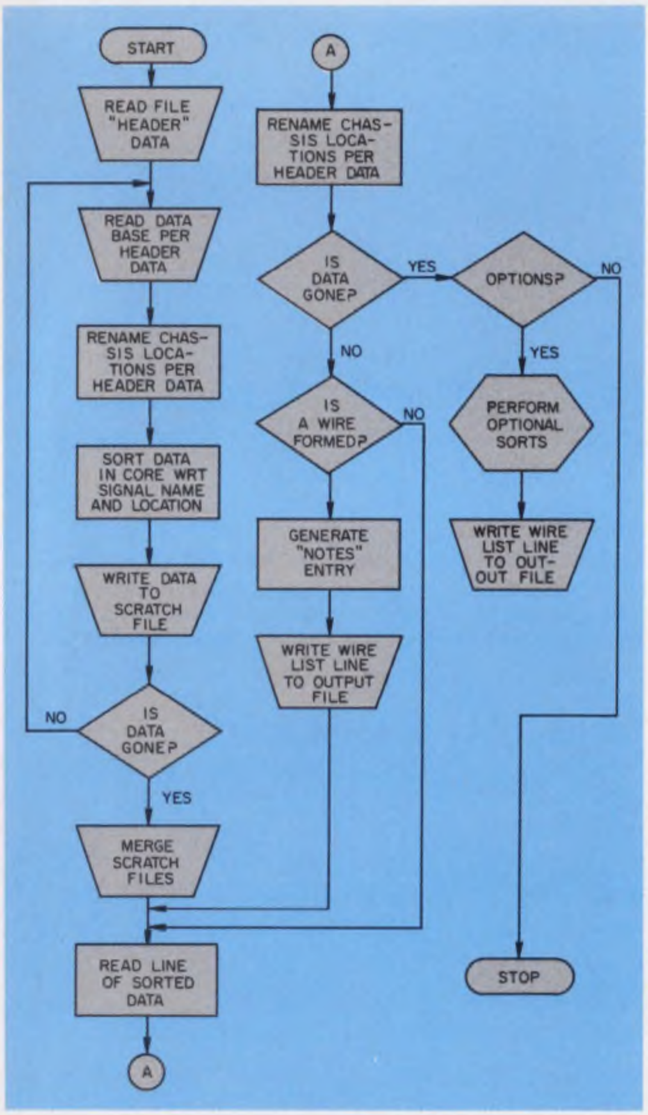
(a)

FROM	TO	NOTES	SIGNAL
FP-X02-003	FP-X04-004	22BLUE	CLK22
FP-X04-004	FP-X06-007	22BLUE	
FP-X06-007	BP-X01-002	22BLUE	
FP-X04-005	BP-X22-010		D12*
FP-X01-002	FP-X04-018	TWIST	E12A
FP-X04-018	BP-X01-003		
FP-X01-001	FP-X07-008		Z06L

(b)

FROM	TO	NOTES
FP-X01-001	FP-X07-008	
FP-X01-001	FP-X04-018	TWIST
FP-X04-018	BP-X01-003	
FP-X02-003	FP-X04-004	22BLUE
FP-X04-004	FP-X06-007	22BLUE
FP-X06-007	BP-X01-002	22BLUE
FP-X04-005	BP-X22-010	

4. **Report by signal order** (a) helps the designer locate a particular signal. However, a report by location order (b) is better for wiring tasks.



5. **A sort merge procedure arrays** the data file in report order. Header data alter the sort order of the location fields to conform with preset priorities. Notes are handled by special procedure.

typical preamble is shown in the accompanying table. Line 1 is obtained by dividing the number of inputs by three and rounding off to the next highest integer—for example, 611 input entries yield the number 204 in the first line of the table. Line 2 specifies the number of files that constitute the data base. Line 3 specifies the number of chassis assignment records to follow. Thus the number 8 tells the computer that four chassis—FP, LB1, LB2 and BP, ranked from 1 to 4—follow. These rankings are used in the reporting system to sort wire runs into the expected order of chassis locations.

Generating the report

Another sort-merge procedure forms the basis for generating the final reports.

Two basic formats prove useful (Fig. 4a and Fig. 4b). The first is based on a major sort by signal name and a minor sort by location. This affords easy access to signal locations for the engineer. But use of the signal name as the major field alters the numerical ordering of signal starting point. A major sort by location, however (Fig. 4b), gives the technician a wire list that is closer to the order in which the actual wiring progresses. To achieve this, the computer temporarily relabels the chassis field with the corresponding rank number, before sorting on location.

An additional feature of the program is "note" processing (Fig. 5). The program sequentially checks adjacent nodes in a signal chain and for each pair, outputs the item in the note field that has the lowest alphabetic rank.

The reports provide a basis for standardizing wire lists. Standardized lists promote assembly efficiency by reducing the number of personalized techniques that the technician must contend with. Also, the program logic minimizes wire lengths, to some degree, by eliminating backtracking.

Evaluate hardware tradeoffs

Most Fortran IV compilers can implement the wire-listing programs. The number of nodes handled varies with the service used. On General Electric's Timeshare Mark III, the program handles about 4000 nodes. Use of the GE Run-Big mode increases the capacity to 8000 nodes. Additional subfiles increase the amount of program logic but also increase the input capacity.

For greatest economy, one should use card files and line printers for wire-list inputs and printouts, respectively. Suitable remote batch services are available with the GE Mark III, or you can use a central computer with its associated card reader and printer. ■■

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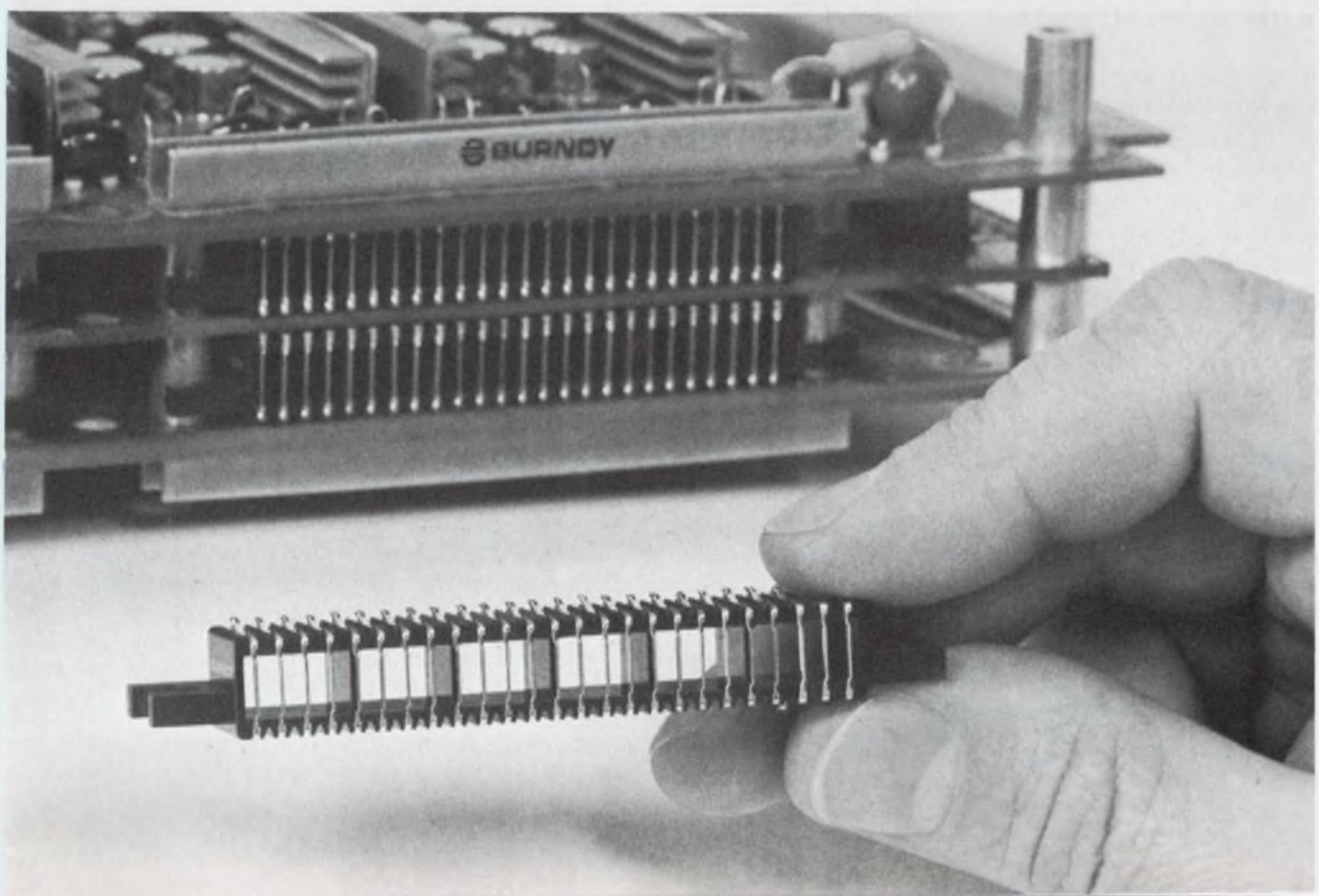

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Consider in-house time-sharing for your engineering computations. You'll get the benefits of interactive use along with 'free' batch time.

Today the design engineer has a wide choice of computer systems for handling his design problems. In a typical situation, the options include batch processing via a large-scale machine, outside time-sharing services, dedicated minicomputers and in-house time-sharing on "midi" computers. Which one should he use?

Batch systems are practical where fast turnaround and user interaction aren't essential. Outside time-sharing is great for beginners—but the costs tend to escalate. In-house time-sharing may well offer the combined benefits at more moderate costs. Minicomputers, of course, offer the cheapest approach, but they can be a big hassle to use.

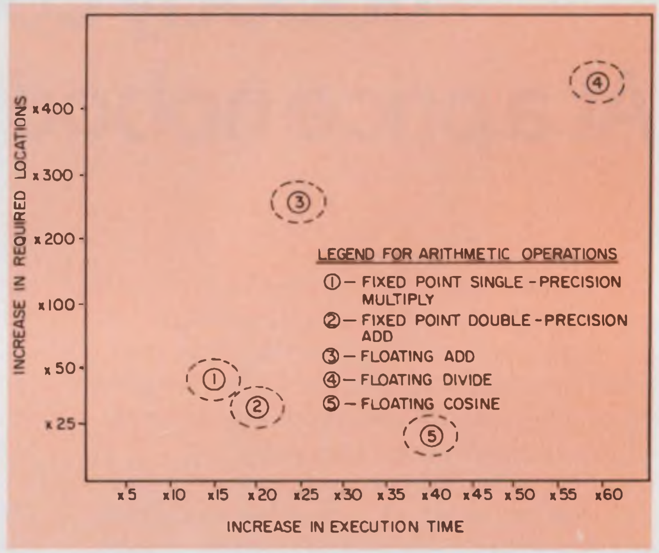
Try starting with a time-sharing service

A beginner in computer programming faces many problems. He will find that generating a simple program may take days—sometimes weeks. Writing, debugging and rewriting is normal. The programs are usually unnecessarily long.

For all practical purposes, an outside time-sharing service provides unlimited memory capacity and other features of a large machine—like the availability of peripheral equipment—to many simultaneous users. For most scientific and engineering problems, an outside service is satisfying for both beginners and experienced programmers.

But the economics of outside time-sharing services must be clearly understood. A typical service bureau charges $10 per connect hour, $6 per CPU minute and $1 per 2 k of disc-pack storage each month. The engineer should remember that a beginner will use a lot of expensive CPU time for program debugging. Despite this, buying an outside service can be quite economical—provided the number of users is relatively small and their programs require little CPU time.

Experience gained with a time-sharing service



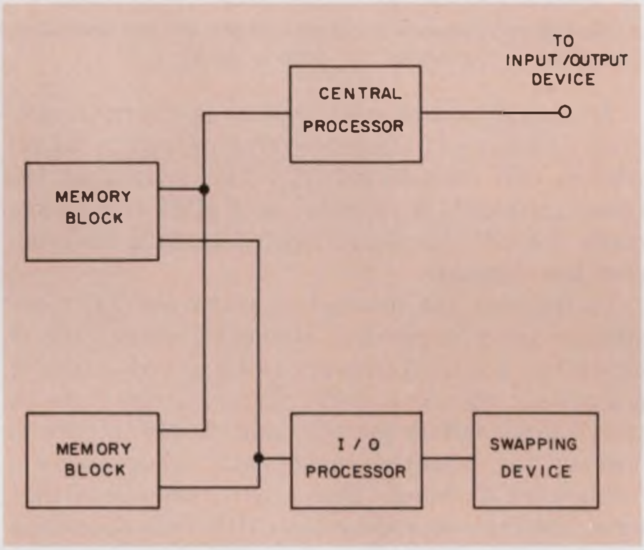
1. **The relative computational power** of a typical large-scale computer and a 12-bit mini with a minimum hardware-instruction set. The required number of instructions and the execution time of the large computer are taken as unity and other data are normalized.

can help an engineer estimate the approximate size and speed of a suitable in-house facility. If modest program size (8-k bytes) and low I/O (few printed pages; small data bases) are usual, a dedicated minicomputer, with its low price tag, becomes attractive.

Minis have their limitations

Remember, however, that the basic cost of a minicomputer usually does not include peripheral equipment. Generally the price of high-performance peripherals is many times that of the mainframe. A typical price for a complete stand-alone, minicomputer-based system is $20,000—four times the price of the basic mini. When you evaluate a minicomputer as a tool for solving engineering and scientific problems, consider not only the price of the system but its ability to solve your specific engineering problems. Because of limited core memory, most minis are used primarily for tasks involving data acquisition and analysis. The availability of high-level languages, such as FOCAL and BASIC, has greatly

Kenneth Klos, Marketing Manager, PDP-11, Digital Equipment Corp., Maynard, Mass. 01754



2. **Independent overlapped operation** is a characteristic of an asynchronous system design. It greatly improves efficiency and processing power by having the CPU execute a program in one memory block while programs are exchanged with the other block.

improved the efficiency of minicomputers for the engineer. But many limitations exist, and these should be carefully evaluated.

A minicomputer will require much greater user involvement than a large-scale system. Three major performance areas should be examined before the decision is made. These are:

- Memory size.
- Arithmetic capability.
- Programming.

The most difficult problem is to estimate memory requirements for a problem. The engineer can't use past experience as a guide if he has been using a large-scale computer. He will be forced to study the instruction routines and be concerned with accuracy (determined by word length) and addressing. These parameters determine the program size and the ability of a machine to do the job.

The arithmetic capability of computers is usually measured in microseconds per addition. In minicomputers this may be misleading, since superficially their cycle times compare favorably with those of larger counterparts.

When you program a mini, the word length and instruction set can have serious effects on both the memory and speed requirements of the system. Word length determines not only the accuracy of computation but also the required memory. For example, with a 12-bit computer, operations would have to be carried out in double precision to obtain accuracy equivalent to that of a 24-bit computer. This means that the 12-bit computer would need much more storage capacity than its larger counterpart.

Floating-point hardware is generally not available to the minicomputer user. He has to choose between fixed-point arithmetic (with its scaling problems) or floating-point software packages. In the first case, programming can become a nightmare. In the second, there are additional memory requirements, along with a tenfold increase in execution time. Fig. 1 shows the relative power of a large-scale computer and a mini. As can be seen, a typical arithmetic feature—floating-point addition—involves a three-hundredfold increase in core storage locations and a twenty-fivefold increase in execution time when a mini is used.

The programming systems currently employed for dedicated and time-shared minicomputers vary in their effectiveness. None, however, fully realize a computer's full potential. The three systems best known today are FORTRAN, BASIC and FOCAL.

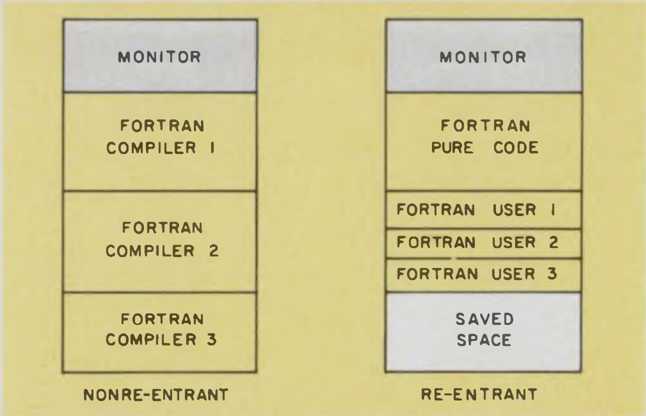
The version of FORTRAN used with minis is just a small subset of FORTRAN II that was originally designed for batch processing. However, batch languages are unsuited for an interactive environment. FORTRAN provides no features for on-line formation and debugging of programs. Consequently an external text editor is needed, and debugging is done off-line.

SINET-BASIC, an interpretive version of FOCAL, provides direct debugging but is limited to the stand-alone configuration.

Use batch processing for routine programs

In applications where fast turnaround time and interactive operations are not essential, batch processing provides the most economical access to a powerful computer at the lowest cost per instruction. Another advantage of batch processing is that it does not monopolize the engineer's time; instead it leaves the job to an operator. In many cases, large companies have their own batch-processing computers as in-house installations, and often these are capable of handling more than one user.

Features such as virtual-memory can eliminate most of the worry about fitting programs into the computer. However, the cost runs about $20,000 a month for a single user—so be sure the expected workload warrants the expense.



3. **Re-entrant software prevents excessive core use** when a program is duplicated for several users.

Reduce costs with in-house time-sharing

As we've seen, when the number of users of an outside time-sharing service increases, the cost can soon become prohibitive. For example, if each terminal is used an average of four hours a day, with a CPU time of about 2.5% of the total running time, the monthly cost for eight terminals would amount to $17,000 a month (assuming 22-day month and 7500-k words of mass storage). At this point buying or leasing an in-house computer system should be seriously considered.

A time-sharing system is not just any computer with additional hardware and software. It is a system designed specifically for sharing a fully implemented computer system among several simultaneous users. A minimum configuration of a time-sharing system includes a CPU, input/output terminals and sufficient core memory to service several users.

The PDP-11/45, for example, allows batch, time-sharing and real-time work to proceed simultaneously. Batch-processing job streams can be entered via local card or tape equipment, or initiated from a remote terminal. A user at a remote terminal can specify batch programs to be run, and he can direct the output to local devices, his own terminal or any other remote station tied to the central computer. The basic system configuration of this time-sharing system and its cost breakdown are as follows:

- PDP-11 (96-k core)—$100,000.
- High-speed printer—$17.000.
- Disc (49 megabytes)—$54,000.
- Tape—$10,000.
- Data communications—$16,000.

The total comes to $197,000.

Each program is assigned a fixed slice of CPU time for execution, and the operation is switched from one program to another in round-robin fashion until all programs are completed. For example, if each user receives a sixtieth of a second and there are 12 users on the system, each will be serviced once every fifth of a second.

The usual time-sharing system performs multiprogramming—it allows several programs to reside in core simultaneously. The switching between programs is initiated by a clock that interrupts the CPU to signal that a certain time period has elapsed.

To increase the number of users served, more storage space is needed. However, since core is expensive, a second memory is employed—usually a magnetic disc or a drum. The programs can be placed in secondary memory and moved into main memory for execution on demand. Programs entering core exchange places with programs that have just been served by the CPU. This operation is called swapping.

The main memory is divided into separate blocks. The secondary memory connects to these blocks through a high-speed input/output processor. This strucure allows the CPU to operate a program in one block of memory while programs are being swapped to and from another block. Independent overlap like this greatly improves efficiency and processing power and is characteristic of an asynchronous system design (Fig. 2).

Round-robin scheduling is effective only if all programs have similar requirements. Very often a system has to handle some programs that require extensive computing time (compute-bound programs) and other programs that stop frequently for input or output (I/O-bound). To serve these two extremes, the scheduling algorithm should provide frequent service to I/O-bound programs and give compute-bound jobs a longer time slice to prevent wasteful swapping. Today's algorithms do this.

To prevent excessive core usage, re-entrant software is usually employed in these systems. The program is written in two parts. One part contains pure code, which is not modified during execution and is used by a number of simultaneous users. The second part belongs strictly to each user and consists of the code and data that are developed during the compiling process. This section is stored in a separate area of core. The two systems are compared in Fig. 3.

Since I/O is handled by a monitor, the input or the output can be transferred even if a program is not in main memory. The monitor also optimizes throughput by keeping all devices busy and executing jobs in the best order. In an efficient time-sharing system, monitor functions (referred to as monitor overhead) take 5 to 10% of central processor time, making 90 to 95% of the time available to the users.

Other modes of operation

Interactive time-sharing provides an excellent method for developing or operating programs where results are needed immediately. In fact, some programs are designed to be interactive—that is, they ask the user questions and formulate results based on his answers. A great number of today's design programs operate in this way.

For other types of programs, batch processing is preferred. Here programs and data are stored on magnetic tape or cards, and the results are used during the day. It is highly advantageous for the computer system to perform several functions simultaneously—batch processing, remote batch and real-time applications. The advantage is not merely one of greater flexibility. The very nature of interactive time-sharing means that only a small percentage of the computer's processing capability is used. This ability to perform other tasks simultaneously enables the user to get more work out of the computer without interfering with the time-sharing users. Thus other work can be performed "free." This is something you don't get from outside services.

The in-house time-sharing system can also serve as a preprocessor of programs being readied for another, business-oriented computer. Users in remote locations can develop, compile and test programs on the time-shared computer, then transfer the completed program via cards or magnetic tape to the business-oriented machine.

A few points to remember

There are several important questions to ask before you consider any proposed computer system, regardless of whether it is an in-house or outside service. The questions include these:

- Does the vendor provide good support for his hardware, software and user training?
- What do these services cost?
- Does the vendor have a good record with other customers and nearby backup facilities?

These are important considerations, both in planning the cost of a time-sharing service and in assuring reliable operation. ■■

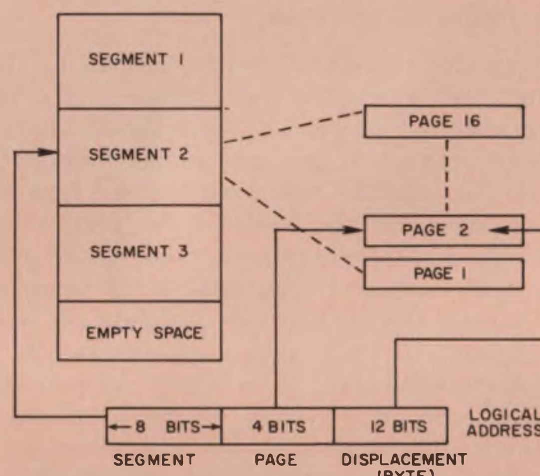
How to increase computer size without making the machine bigger: Use virtual storage. Here is a straightforward explanation of this proved technique.

Have you ever run a program on a small computer and received a diagnostic to the effect that the program size exceeds the memory capacity? What do you do? Ask the company to buy more memory? Redo your program with careful overlays? Redesign the computer?

Suggestion: Try "virtual" memory. It will let you execute programs that exceed main-memory capacity, often without further effort on the part of the programmer.

Virtual storage "expands" the program storage space available to the data-processing system. Programs operate with an imaginary storage facility whose address space is much larger than that of real storage. A hardware-software mapping technique converts the virtual, or imaginary, program address to a real hardware address during execution. Where necessary, temporarily inactive portions of the program reside in auxiliary storage devices, such as discs. But the auxiliary storage is treated as an extension of main storage.

The main storage plus auxiliary storage used equals the size of the virtual memory. For example, System/370, with virtual storage, can address up to 16 million bytes (eight-bits) of virtual storage, compared with four million bytes of real storage.



1. **Virtual memory is divided** into pages and segments. Logical addresses specify a location in virtual memory by segment, then by page number and, finally, by displacement within the page.

Conceiving the virtual memory

In general, a computer program contains and manipulates much information—instructions, constants, work areas, tables, etc.—but it uses only a portion of the information at a time. If the main memory cannot store the entire program, the program can still be executed because only the relevant portion need be present in the main storage at any given time.

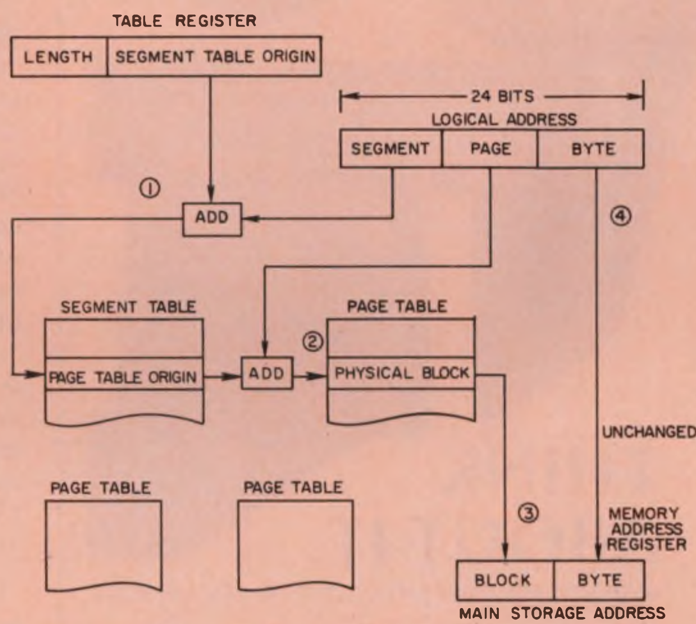
Imagine a virtual storage of some arbitrary size—16 megabytes, say. For the incoming programs, assign each consecutive byte a unique address, and partition this required storage into 4-k bytes—called "pages." Then subdivide the real memory into 4-k byte blocks called "frames," and partition the direct-access storage peripherals into 4-k-byte "slots." Transfer between real memory and peripherals will then occur in 4-k-byte blocks.

A two-level reference to the pages will be used. A given program occupies contiguous segments of virtual memory that contain one or more pages (Fig. 1). Specifying the segment number, page number within that segment and the displacement within the page locates a given program element in virtual storage. We call such an address a "logical address."

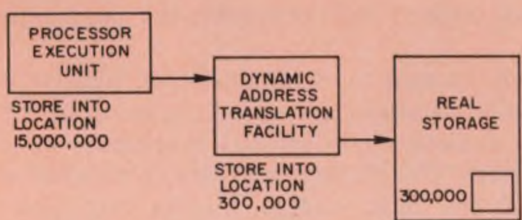
Map to real memory

A hardware/software package links logical addresses to the real ones needed by the CPU to execute the program or programs. The hardware referred to as the "dynamic-address-translation facility" (DAT) intercepts the virtual-storage addresses assigned by the computer to the program and translates them into real-storage addresses (Fig. 2). The DAT actually maps the 16

Stephen C. Kiely, System Development Div., International Business Machines Corp., Neighborhood Rd., Kingston, N. Y. 12401.



3. **Translation of a logical address to a real one** requires a two-level search. The segment table lists locations of corresponding page tables, one for each segment. Each entry in the page table specifies the starting address of the corresponding real storage block.



2. **Real-storage addresses** required by the processor execution unit are derived from the program's logical, or virtual, addresses through the DAT translator.

megabytes of virtual storage into the smaller domain of real storage. Mapping maintenance is done by the software portion of the package—the control program.

For a DAT translation, the control program maintains a segment table and associated page tables (Fig. 3). It also stores the location of the segment table in a special table-origin register. Each entry in the segment table specifies the location in real memory of the corresponding page table. Each page table entry shows the address of the real storage frame containing the virtual page, or indicates that the page is contained in a peripheral slot. The tables reside in real memory during execution of a program.

Here are the steps involved in a DAT translation: (1) The segment number of the logical address added to the segment table origin locates the origin of the page table corresponding to the segment number. (2) Addition of the page table origin to the page number of the logical address gives the location of the page table entry containing the physical block location in main storage (if present). (3) The block location and the byte number (4) complete the memory address to be accessed by the CPU.

Page-in and page-out

Note that the executing program doesn't know or need to know where a particular virtual page is located at any point in time. It may be located in a frame of real storage or in the slot of a peripheral. When the required virtual page is located on a direct-access device (such as a disc), its page-table entry will be flagged to generate an exception condition in the processor. Consequently the control program must find a real storage frame to contain the virtual page. The control program then initiates an I/O operation to transfer the page from the storage device ("page-in") and updates the page table accordingly.

If the amount of virtual storage used by a program exceeds real storage, the control program must make frames available. It selects certain frames and writes the pages for those frames in I/O equipment storage slots. Once the pages are copied out, the frames can be reused to contain other pages. Transfer of pages from frames to slots is called "page-out."

Page replacement can be carried out by randomly selecting pages for page-out, or the control program can determine those pages the program is no longer working with. In the latter case, as in IBM's System/370, the selection of pages can be based on the program's recent history of page usage. The hardware provides the control program with indicators for each frame, and the indicators tell if the page within the frame has been referenced or altered by the program. By periodically resetting these indicators, and at a latter time examining them, the control program builds up a history of the program's storage referencing pattern, thereby providing a factual basis for the page-out selection decision. In fact, the "altered page" indicator allows the control program to shortcut page-out operations. (If a page has not been altered, the page's old image on a direct-access (I/O) slot can be used rather than rewriting the page into the slot.)

Hardware is used to compensate for relatively slow table-translation speeds. A system of at least eight registers (for smaller machines) or a buffer system (for larger machines) retains a number of the most recent translations. Any virtual address matching a previously translated one is converted at hardware speeds.

System usage with virtual storage

With virtual storage, unused portions of programs can be reallocated to permit simultaneous execution of still more programs in main storage.

Real-memory occupancy varies by as much as 8:1 in a 24-hour period in installations that run batch and teleprocessing jobs concurrently. Without virtual memory, the total main-memory requirement equals the peak requirement. With virtual storage, however, less idle main memory is needed; the teleprocessing tasks simply occupy virtual memory. In fact, virtual storage allows the smaller system's user to employ teleprocessing applications in situations that are prohibitive —because of small memory size—for conventional systems.

Virtual storage can aid programmer productivity. The programmer becomes less concerned with splitting up programs to fit the machine. Editing, updating sorting and processing no longer require fragmentation of a complex program. And virtual storage affords the larger space often needed for debugging facilities.

With several segment tables, virtual storage can provide a "virtual machine," composed of a virtual processor and virtual I/O devices. In other words, each user can have his own virtual machine with its own operating system. ■■

Editing problems with your mini?

Avoid them by specifying the right tape transport and by optimizing the timing sequence to prevent loss of data.

The use of minicomputers and magnetic-tape peripherals in data-entry systems is posing problems in selective record updating and fast editing for more and more engineers. A typical minicomputer-based system has neither the additional memory nor the peripherals for complete tape dumping normally required for record updating. And during selective editing of tape records, adjacent data fields can be disturbed.

The solutions involve a tradeoff between the number of permissible updates, the record lengths and the interblock gap (IBG) size.

What causes editing problems

For selective editing, tape-transport deficiencies can cause either of the following:

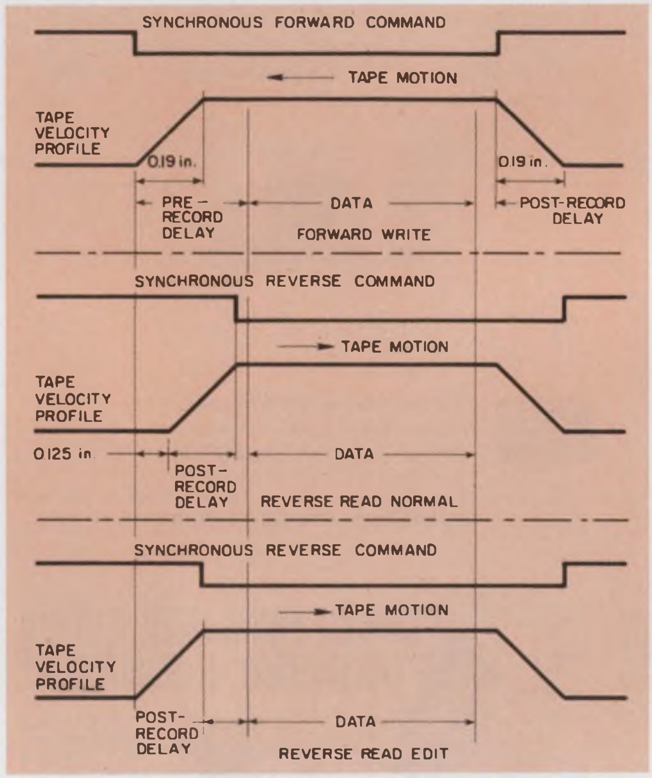
1. Noise transients, or glitches, in the IBG.
2. Inaccurate tape positioning.

A glitch occurs when write and erase currents are turned off. A small area of the tape is affected by the leading pole-tip of the record and erase heads as the magnetic field is collapsing. These flux transients appear as false signals and have 20 to 25% of the normal signal amplitude.

Since this phenomenon is caused by the head design, a logical way to overcome it is by collapsing the magnetic field just before tape comes to a standstill. This can be done by designing proper tape-transport controller delays. Of course, when no editing is required, the transient problem is avoided by leaving write current permanently on until the complete tape is written.

Even if the tape transport has adequate transient suppression, various positioning problems—tolerancing, gapping and erase-head positioning—may still arise.

Tolerances ultimately determine the number of editing retries needed for a given record. The critical factors are controller delays, tape speed and start/stop distances. The tolerance of these parameters can affect the placement of a new data block and, if the block is not positioned



1. **Accurate positioning of a data block** during selective editing of a record on magnetic tape is a function of the interblock gap (IBG). If this gap becomes less than 0.5 inch, successful selective editing becomes impossible.

properly, cause read errors. For example, if the resulting IBG is smaller after an update, the erase head may move into a block of data.

One solution to the tolerancing problem is to increase the IBG to allow for tolerance buildup. But there is a tradeoff. The amount of information stored on a reel decreases with an increase in IBG width. Conversely, if the tape is written with an IBG of less than 0.5 inch, editing is not possible.

Ideally an update/edit system will not only work with tapes originally written on the same transport but will also read/edit tapes written on another system from any IBM-compatible source. Essentially this compatibility depends on the gapping function and accurate control of the gap limits. Nominally the nine-track IBG is 0.6 inch, and this can be allowed to approach a 0.5-

Gerald Lembas, Tape Product Manager, Pertec Corp., Chatsworth, Calif. 91311.

inch minimum. Tapes written on another system can cause the greatest problem for updating. This is particularly true when the IBG, as a result of close tolerancing, is less than 0.5 inch. Then it becomes impossible to shoehorn in additional record information.

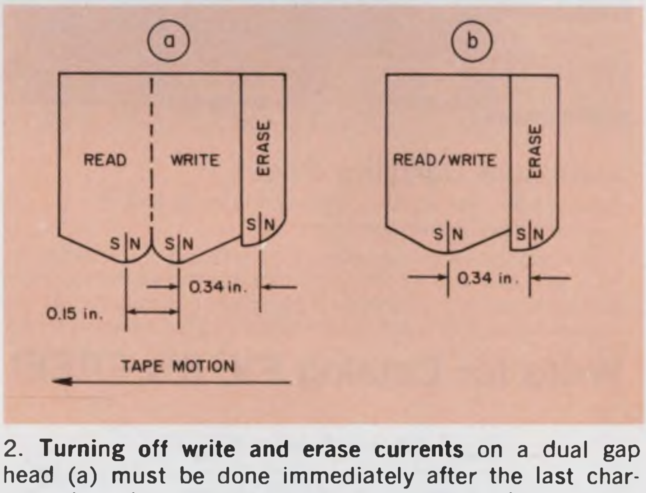
If the designer controls his delays adequately, tape-speed variations and related start/stop distances must still be considered. There are two speed-variation components, short and long-term. Short-term variations are measured in milliseconds, while long-term variations affect tape speeds over longer periods—seconds and minutes. For all practical purposes, the short-term variations average out to zero. Long-term variations, however, often appear as a difference between forward and reverse tape speeds, thus affecting the reverse-stop and forward-start distances. In other words, the reverse-speed tolerance affects the starting point for the writing of new data. An accepted limit on the speed difference between forward and reverse directions for a single-capstan system is 5%.

The number of editing retries then depends on how accurately tape positioning is controlled. Using an IBG of 0.6 inch, we can expect three retries before approaching a marginal condition. A typical IBG timing sequence for forward, write, reverse read and edit is shown in Fig. 1.

Table. Pre-record and post-record delays (at 25 ips*)

Function	Pre-record delay (milliseconds)		Post-record delay (milliseconds)	
	9-track	7-track	9-track	7-track
Write and rewrite delays				
1. WRITE from BOT	226	226	3	3
2. WRITE (normal)				
Single gap	23	28	3	3
Dual gap	17	22	3	3
3. WRITE FILE MARK	150	150	3	3
Read and reread delays				
1. READ from BOT	60	60	0	0
2. READ FORWARD (normal)	12	12	0	0
3. READ REVERSE (normal)	12	12	3	8
4. READ REVERSE (edit)	12	12	8	12

*To calculate the above delays for other tape speeds, scale inversely to tape speed; i.e., WRITE from BOT at 75 ips is (25/75) × 226 = 75.5



2. **Turning off write and erase currents** on a dual gap head (a) must be done immediately after the last character is written because of an additional distance that the tape must travel to reach the read gap. Slower turn-off can be tolerated in a single-gap head (b).

Is the erase head controlled properly?

The erase head is critical for successful editing. To prevent it from interfering with the next record, the erase and write currents must be turned off as soon as the record is completely written. The problem differs slightly, depending on whether dual or single-gap heads are used (Fig. 2). With dual-gap head transports (Fig. 2a), the written data must travel the WRITE-to-READ head distance for verification before the tape stops. Thus the erase head moves further into the next IBG when updating. Consequently current turn-off must be initiated immediately after the last check character is written. With single-gap transports (Fig. 2b), the slow turn-off can be started with the termination of the synchronous forward command (Fig. 1).

When the edit function is implemented, the controller must provide the various switchable time delays that are required. When a block of data is to be updated, the system must first locate it accurately by reading the record in the reverse direction. It is important never to reference the block to be updated from the previous record, since the upcoming IBG is effectively of an unknown length.

Normal READ REVERSE time delays (see table) close the distance between the stop point and the data block that was just read. This avoids backing into the previous record. However, the READ REVERSE edit time delays are chosen to stop the transport at the same reference point from which the record was originally written. Using the delays recommended in the table and stop/start distances given in Fig. 1, we can calculate the resulting IBGs.

Record length is the final consideration in editing. The new block of data should be the same length as the block it is replacing. ■■

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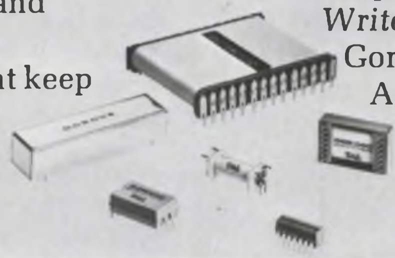

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The world's leader in solid-state power amplifiers.

Cut reference junctions loose in thermocouple scanning systems, and let the computer calculate corrections. You'll eliminate expensive temperature-control hardware.

Conventional thermocouple systems use a reference junction that is maintained at a constant temperature to avoid correction calculations. But there's an easier and cheaper way to establish a reference junction, now that computers are used with most thermocouple data-scanning systems: Allow the reference junction to follow the ambient temperature, measure this temperature with a thermistor and let the computer take it from there (Fig. 1).

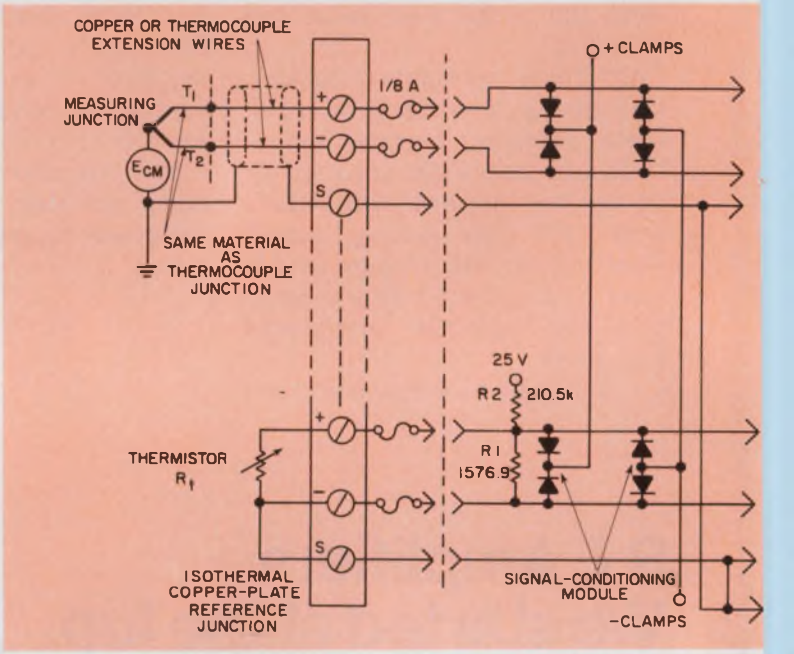
The thermistor output, together with all the thermocouple outputs, are multiplexed at their original low levels to an a/d converter and fed to the computer (Fig. 2). With these inputs, the computer can easily calculate the correct temperatures at the thermocouple measuring junctions.

Thus we eliminate the inconvenience of an ice-water bath or expense of a junction temperature-control system—an expense that is proportionately high if only a few thermocouples are required. Once set up, the computer calculations cost almost nothing.

Also the voltages generated by thermocouples do not vary linearly with temperature. The computer can provide the needed linearization, while conventional systems must resort to calibrated dials or tables for particular combinations of thermocouple metals. And each different reference-junction temperature needs a different table or calibration.

To use a single thermistor to provide ambient-temperature measurements for several thermocouples, the leads from these couples must terminate on an isothermal junction. A typical system handles seven couples with one thermistor.

Both the thermocouple and thermistor terminals are embedded in a copper block that is fastened to a PC board. Printed wiring on the board carries the signal and shield connections to edge connectors, which then lead to a signal conditioning module. In the circuit of Fig. 1, the signal-conditioning module contains a precision-resistor circuit for the thermistor. It also contains clamp circuits for all thermocouples and the thermistor. The module also has noise filters and high-frequency, common-mode rejection circuits (not shown in Fig. 1).



1. **A thermistor monitors the reference-junction's temperature** and the computer uses this information to correct the thermocouple readings. When the temperatures T_1 and T_2 are equal, the extension wires from the thermocouple material to the reference can be made of copper. But special low-cost extension wires, matched to the thermocouple material, should be used when T_1 and T_2 can vary from each other.

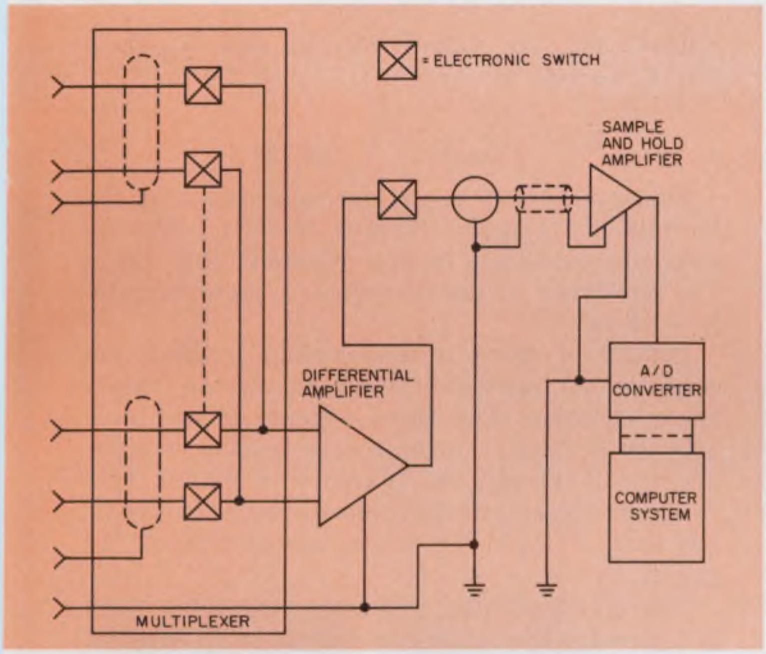
A typical data-gathering system might have, say, 128 multiplexed channels and 16 isothermal reference junctions together with the required signal-conditioning modules in a single multiplexer chassis. For improved accuracy, a separate thermistor assembly measures the temperature of each of the 16 reference junctions.

However, in many applications a single thermistor for each chassis would provide sufficient accuracy, since the adjoining isothermal blocks are at nearly the same temperature. Then, 127 instead of 112 (128 minus 16) channels could be devoted to thermocouples or other transducer inputs. However, in a multiple-chassis system, each chassis should have its own thermistor

Ware Myers, Xerox, 701 S. Aviation Blvd., El Segundo, Calif. 90245.

Thermistor Temperature-EMF Table

Temp °C	Nominal Output (mV)	2-point Linearity Deviations °C	6-point Linearity Deviations °C
0	150.000	−1.44	0
1	148.428	−1.26	0.05
2	146.922	−1.03	0.14
3	145.404	−0.82	0.23
4	143.762	−0.66	0.24
5	142.113	−0.52	0.24
6	140.472	−0.36	0.25
7	138.704	−0.28	0.18
8	136.957	−0.18	0.13
9	135.254	−0.06	0.10
10	133.427	0	0
11	131.667	0.09	0.08
12	129.784	0.12	0.09
13	127.998	0.20	0.16
14	126.093	0.21	0.16
15	124.060	0.16	0.10
16	122.163	0.19	0.10
17	120.147	0.14	0.05
18	118.314	0.20	0.09
19	116.376	0.20	0.07
20	114.324	0.14	0
21	112.147	0.01	−0.09
22	110.229	0.02	−0.05
23	108.207	−0.02	−0.06
24	106.513	0.11	0.10
25	104.286	−0.04	−0.02
26	102.269	−0.09	−0.03
27	100.301	−0.10	−0.01
28	98.290	−0.14	−0.02
29	96.294	−0.17	−0.01
30	94.320	−0.19	0
31	92.317	−0.22	−0.05
32	90.350	−0.24	−0.09
33	88.429	−0.23	−0.10
34	86.498	−0.23	−0.12
35	84.559	−0.23	−0.14
36	82.690	−0.19	−0.12
37	80.827	−0.16	−0.10
38	78.973	−0.11	−0.08
39	77.135	−0.06	−0.04
40	75.316	0	0
41	73.522	0.07	−0.07
42	71.759	0.16	−0.12
43	70.031	0.27	−0.15
44	68.251	0.35	−0.22
45	66.611	0.51	−0.20
46	64.905	0.64	−0.21
47	63.294	0.79	−0.18
48	61.724	0.98	−0.12
49	60.113	1.15	−0.08
50	58.572	1.36	0



2. **A multiplexer can rapidly scan many thermocouples** and reference-junction temperatures at rates far greater than a junction can significantly change its temperature to allow accuracies within the thermistor's capability. Low-level signals obtained from thermocouples and thermistors require careful attention to the details of proper grounding and shielding of the scanning and measuring equipment, especially in electrically noisy environments.

channel, since ambient temperature can vary between chassis.

Experience has shown that a copper-block reference can maintain all the terminals within less than ±0.2 C for an ambient change of up to 10°C/hr in an air movement to 25 ft/min.

Selecting the thermistor

The precision thermistor used in the junction reference (Yellow Springs Instrument Co.—Type 44004) is 2000 Ω at 25 C, and the resistance varies inversely with the temperature. At zero C the resistance increases to 6540 Ω; at 50 C it drops to 720 Ω. Its accuracy is within ±0.3 C from 15 to 35 C, which covers the room temperature range. Accuracy is ±0.6 C from 0 to 15 C and ±0.4 C from 35 to 50 C. Repeatability is ±0.1 C and stability ±0.1 C over 30 days.

Experience with the precision thermistor has shown that in one year of operation the thermistor's resistance is specified to change less than 1% when the temperature shock is less than 10°C/min. The thermistor reaches 63% of its change in resistance in 10 seconds in response to a step change in temperature.

The thermistor resistance, R_t, and the precision resistors, R_1 and R_2, on the signal-conditioning module form a circuit whose output is

$$E_o = \frac{25}{R_2/R_t + R_2/R_1 + 1}.$$

Substituting the values for R_1 and R_2 from Fig. 1, we get

$$E_o = \frac{25}{210{,}500/R_t + 134.489}.$$

This equation is solved for each value of the thermistor resistance from 0 to 50 C. The results are tabulated in the accompanying table. The sensitivity of the thermistor is approximately −1.8 mV/°C.

Instead of using a table-lookup method, the computer can calculate the output voltage from a linear equation. The third column of the table lists the deviations in millivolts from a straight line drawn through the 10 and 40-C points. This two-point linear interpolation produces errors of less than ±0.25 C for temperatures between 10 and 40 C.

The fourth column tabulates deviations from five straight-line segments where each segment covers a 10-C span. This six-point linear interpolation results in errors of less than ±0.14 C between 10 and 40 C.

Thermocouple temperature-emf tables are available from thermocouple manufacturers, the Instrument Society of America or the National Bureau of Standards. A different table serves each different pair of thermocouple metals. Each table also relates to a specific reference-junction temperature, usually zero C. The computer can determine temperature by a table-lookup method or by the use of linear or quadratic approximations. Where the thermocouple table refers to a reference temperature that is different from the actual temperature of the reference, the correction consists merely of adding a voltage corresponding to the actual reference junction temperature to any reading of the thermocouple.

For example, let a Type T (Copper-Constantan) thermocouple produce 16.627 mV, with the reference at 30 C determined by the thermistor. From a thermocouple table that is referenced to zero C, the output for 30 C can be found to be 1.194 mV. Then to correct the thermocouple reading, add the two values:

$$16.627 + 1.194 = 17.821 \text{ mV}.$$

The thermocouple table converts this sum to 350 C. ■■

Putting an engineer in the wrong is a disciplinary action that requires tact, says this manager. But a good swift kick to his pride can help set an engineer right.

Will Durant, the American educator and writer, once said that if you put a man in the wrong, he will hold it against you forever. That's true—but only if you put him in the wrong in the wrong way. And, believe me, it's especially easy for an engineering manager to discipline his people the wrong way. Engineers are professionals, and they want to be disciplined professionally, but the two major mistakes many managers make are to use threats and to issue the criticism in public.

Threats and public criticism are out

It has never done me any good to threaten an engineer with loss of pay or a layoff or the like, because if the engineer didn't like the work environment, he'd simply find another job. So threats are out. I try to reason with engineers and show them my side of the picture. Remember, there's hardly an engineer going who likes to have a thought shoved into his mind without being shown the logic of it first.

I also don't believe that a manager should discipline or criticize engineers in public. Few things can be more degrading. Discuss the complaints in private. And I do think that an occasional disciplinary boot to a man's pride can be very helpful. The engineer should be told where he stands in the organization, even though it may hurt his pride. Having his pride ruffled sometimes can help him develop his potential.

In general, I try to understand the employee's motives and never make light of them; I've always been successful in turning a man's thinking around. Maybe he hasn't always agreed with what I've said, but at least he has understood it enough to go along with it.

Disposing of the visible problems

What constitutes a disciplinary problem often can be a very difficult thing for an engineering manager to determine. How do I know, for instance, when an engineer isn't doing his job? He could be spending long hours at night thinking about the problems of his job, and I might never know about it.

There are disciplinary problems, however, that are more visible, and I concentrate on correcting these obvious ones. Some of the most troublesome are these:

- Lateness.
- Failure to complete paperwork.
- Goofing off.
- Insubordination.
- Uncooperativeness.
- Problem drinking.

Several years ago a night-owling engineering supervisor I knew came in regularly at 9:30 a.m. and left every night at 7 or 8 p.m. No one had ever said anything to him. Suddenly I became his boss. I'd always noticed his lateness, but I'd kept my mouth shut because it was none of my business. But I felt that if he was going to work for me now, the first thing I had to straighten out with him was the matter of getting in on time in the morning.

I told him that his people were there at 8 a.m. and needed his guidance as a supervisor and that it was imperative that he also be there at 8. I told him that the only way he could be sure that his own people were putting in minimal time on the job, and were encouraged to do so, was for him to be there as an example.

This hurt him, because he said he had been working until 8 p.m. My answer to that was that if he chose to leave at 4:30, there was nothing I could do to stop him. If he was able to accomplish all his work in the eight-hour time period, he would have met the letter of the law. But truly successful engineers meet both the letter and the spirit which often times goes beyond the limits of the time clock. He took it pretty hard at the time, but then he reversed himself, and everything worked smoothly after that. He came in at 8 a.m. and never hesitated to put in the extra time. He's now a successful chief engineer.

I think getting engineers to complete their paperwork is one of the most troublesome problems of all. Usually the paperwork falls into three categories:

John P. Brady, Jr., Vice President of Engineering, John Fluke Manufacturing Co., Inc., Seattle, Wash. 98133.

John P. Brady, Jr.

Education: B.S., M.S. in electrical engineering, MIT.

Responsibility: In charge of all engineering.

Experience: Various engineering capacities at Vectron, Inc.; Bell Telephone Labs; Sanborn Co.; and Hewlet-Packard. Credited with several proprietary products, including tape recorders, optical X-Y recorders, photographic time base recorders and standard oscillators. Lectured on the Electrical Engineering Staff at Northeastern University for several years.

Affiliations: WEMA; AMA; Electronics Advisory Committee of Shoreline Community College; MIT Club of Puget Sound (President 1970-1971); Kiwanis; Eta Kappa Nu; Sigma Xi; IEEE; Tau Beta Pi.

Employer: Founded in 1948 in Springdale, Conn., and moved to Seattle in 1952, John Fluke Manufacturing Co., Inc., first produced a VAW® meter which became both a trade name and a generic term for a device that measures voltage, wattage, and amperes. The company also designed and built high-voltage power supplies used in nuclear experimentation. Today Fluke designs and manufactures a broad line of measurement, voltage, and frequency generation and calibration equipment. It approached $14 million in sales in 1971.

1. Routine tests, such as performance appraisals.

2. The filling out of time cards on time, and seeing that their people fill them out on time.

3. Project progress reporting.

To get my engineers to file their reports on time, I bug them. I do it mostly through my secretary and my staff assistant. If the offenders are consistently delinquent, I talk to them myself. We bug them maybe once every two weeks. That's sufficient. The company policy is that if the supervisor wants a raise, he'd better have his performance appraisals up to snuff. I concur.

Straightening out goof-offs

What about the goof-off? This isn't a routine problem. There's no doubt that he's affecting his productivity and that of the organization. Of course, I expect the supervisor to say something to a man if I catch him spending too much of his time gabbing in the hall. If he persists, I request that the supervisor make out an incidence report, which gets into the man's permanent record. If he still persists, he'll be given another incident report and a deadline to either improve or leave. Another way I handle it is to cut the amount of his raises.

I have to consider the engineering worth of the goof-off. A man who's a constant disciplinary problem isn't worth keeping in the long run, no matter how good an engineer he is. His liabilities outweigh his assets. But before he reaches that stage, I talk to the goof-off often and make it very clear where he stands.

Try to counter insubordination

Insubordination. This is a very serious infraction if it's affecting the productivity of the group. Sometimes engineers are fired or choose to leave a company because of personality conflicts that lead to insubordination. That's one thing. But, in general, if I give the responsibility and the authority to a man to have a particular job done, I expect him to do it, and I expect his people to do what is asked of them. I will always back up the supervisor, provided he's not asking the impossible. If, however, the supervisor is having trouble with several of his employees, he's probably being overly demanding, and I'll have to straighten him out, privately.

There's an obvious solution for the problem of the engineer who refuses consistently to cooperate: Get rid of him.

But so often the guy who doesn't cooperate is the genius of the company. Part of the problem is the supervisor's failure to know how to use this kind of talent. I usually try to use such a person on a job where he can work alone. I think that organization charts should be flexible enough to handle the disciplinary anomalies of the different people in the organization, including the engineers who work best in a rigid environment.

When to fire

And then there's the problem drinker. The manager must see that this engineer gets the work out. I don't think he should be the drinker's father confessor, unless there is something that he can do to help. And I don't think that it's the company's obligation to legislate what the employee does on his own time, so long as it doesn't interfere with his output or warp the company reputation. If he fails to produce or if he hurts the company, he's out. It's one of the few good reasons there are for firing a man.

In most cases, the reasons for discharging an employee relate to disciplinary problems that affect productivity. There are other reasons—like industrial espionage, extortion or any other crime punishable by law. And technical incompetence —the engineer who claims he's a technological hot shot and isn't. The incompetent man came in under false pretenses and has no kick when he is let go.

I've known of instances where managers used a layoff as a form of firing. I think that's wrong. I feel that layoffs should never be related to disciplinary problems. If I have a problem employee who should be fired, I'll fire him and not wait for a layoff as a handy excuse to get rid of him.

One other problem I haven't yet mentioned: absenteeism. I've never had much of an absentee problem among my engineers. I suspect it's because a good engineer is a professional in his thinking, and he really needs a good reason to take a day off. I think, too, that he generally likes what he's doing—but, more, I think that it's a mark of the professional. How often does your doctor take a day off? My doctor told me that he thought he was getting old because he was sick a day last year. I think the same is true of engineers. ■■

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INFORMATION RETRIEVAL NUMBER 88

Positive voltage changed into negative, and no transformer is required

A compact, transformerless dc-dc converter derives a negative supply voltage from a positive one. The technique allows dual-supply op amps to operate from a single supply line and still deliver bipolar outputs.

A square wave is generated by the Type 555 timer (Fig. 1) plus four external passive components. The nominal period of the resulting square wave clock signal is given by

$$T = 0.685\ (Ra + 2Rb)\,C.$$

Five additional passive components are required to derive the negative supply from the clock.

The circuit has component values chosen to give a 2-kHz pulse-repetition frequency, with the coupling and filter capacitors selected to minimize ripple under heavy loads. Since the timer is insensitive to variations in supply voltage and has good output drive capability, it makes an excellent system clock. For a specific application, the capacitor values used depend on required clock prf, load and ripple rejection.

With a 500-Ω load, typically equivalent to 10-μA741s, the negative output voltage tracks the positive supply, but its absolute value is always about 3 V lower (Fig. 2a). Output regulation for a constant +10 V input is approximately 10% for a change from no load to a load of 500 Ω. Usable outputs are available with load impedances as low as 50 Ω—which would represent about 70 Type 741 op amps.

As an alternative to this approach, you can derive an artificial ground between the real ground and the positive supply, but this would add complexity and reduce the output capability. Of course, you can also use an external supply, but this would increase cost and size.

Bert Pearl, Research Specialist, Lockheed Missiles and Space Co., Box 504, Sunnyvale, Calif. 94088.

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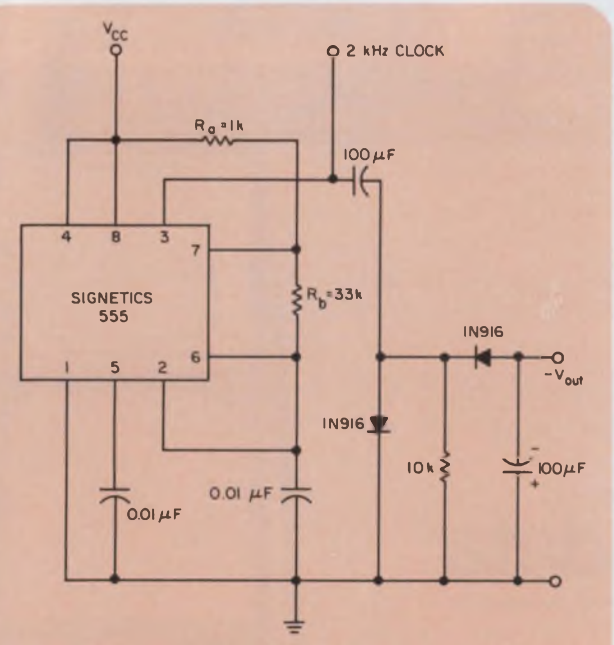
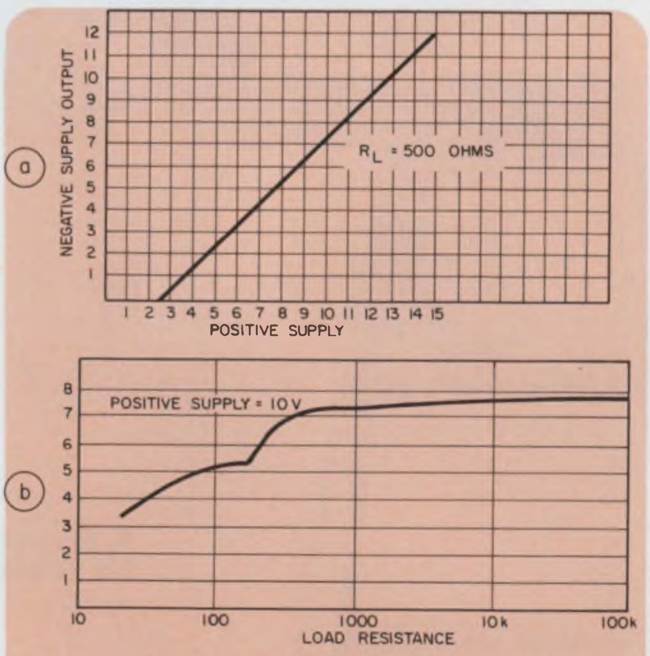
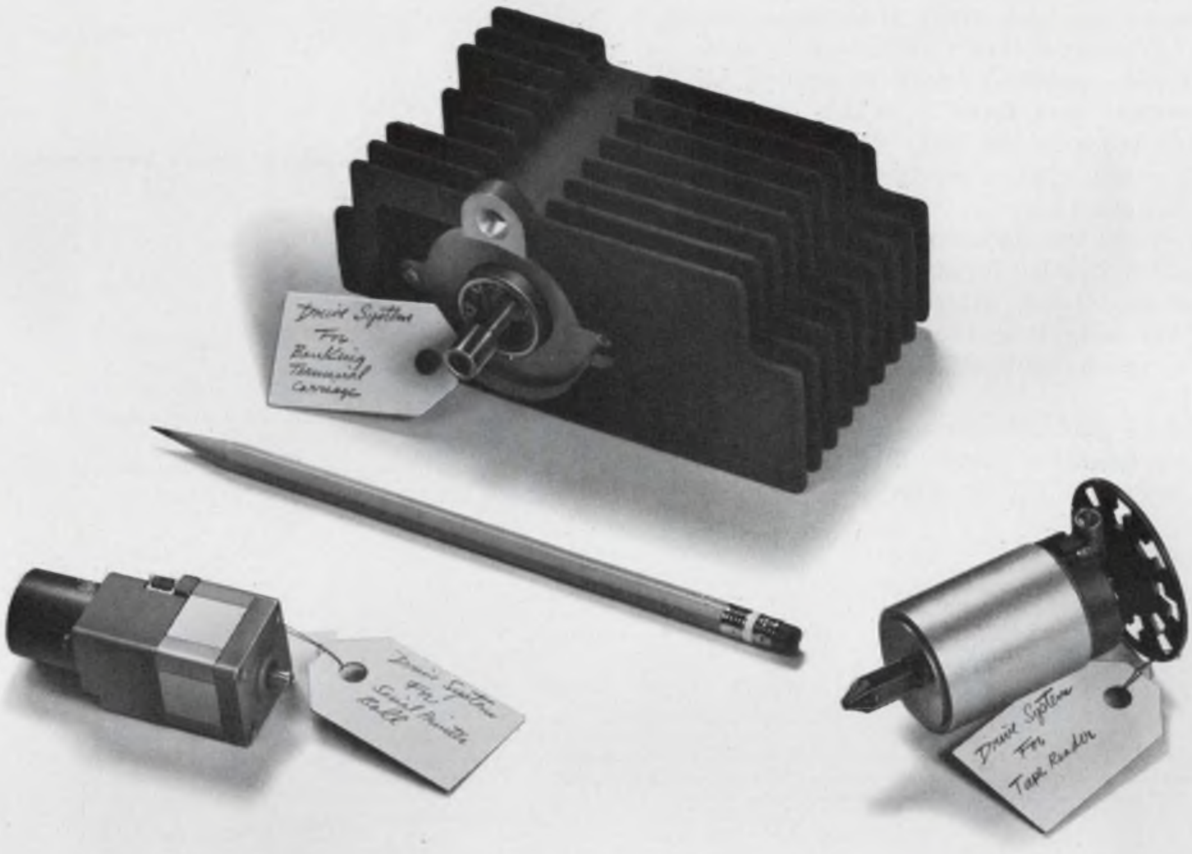


1. **Transformerless dc-dc converter** derives a negative supply voltage from a positive. As a bonus, the circuit also generates a clock signal.



2. **The negative output voltage** tracks the dc input voltage linearly (a), but its magnitude is about 3 V lower. Application of a 500-Ω load (b) causes a 10% change from the no-load value.

Computer builders get more than a motor from TRW/Globe



TRW/Globe customers can achieve a combination of motorized functions in minimum space while eliminating unnecessary assembly operations and simplifying inventory requirements.

They do it by ordering a Globe functional "package" instead of just a motor. For example, take the items above, produced for three of the leading builders of business machines and computers:

The package on the left drives the printing ball on a serial printer and indexes it horizontally, with a DC motor. A DC tach generator provides feedback to the rest of the system. And a hollow motor shaft permits another shaft from a linear solenoid to index the ball vertically.

At the top is a drive for a banking terminal carriage. Globe's integrally cast heat sink permits the high torque motor to operate reliably without burning up and causing costly downtime.

The third package drives a computer tape reader. Widened poles and spiralled armature slots assure smooth motion even though torque changes constantly. The tach wheel is read by an electric eye for feedback, and Globe supplies the drive hub.

When you can't afford the cost of failure, call or write: TRW/Globe Motors, an Electronic Components Division of TRW Inc., Dayton, Ohio 45404 (513-228-3171).

TRW® GLOBE MOTORS

INFORMATION RETRIEVAL NUMBER 82

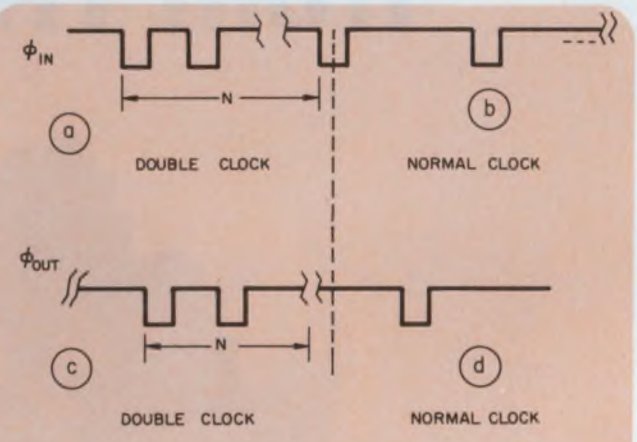
Double clocking cuts off-the-shelf registers to custom sizes

A double clocking technique eliminates unwanted register length in off-the-shelf units by storing input bits twice and reading out each double entry as a single bit. This scheme saves money, since you can avoid ordering a custom register by using a larger off-the-shelf unit.

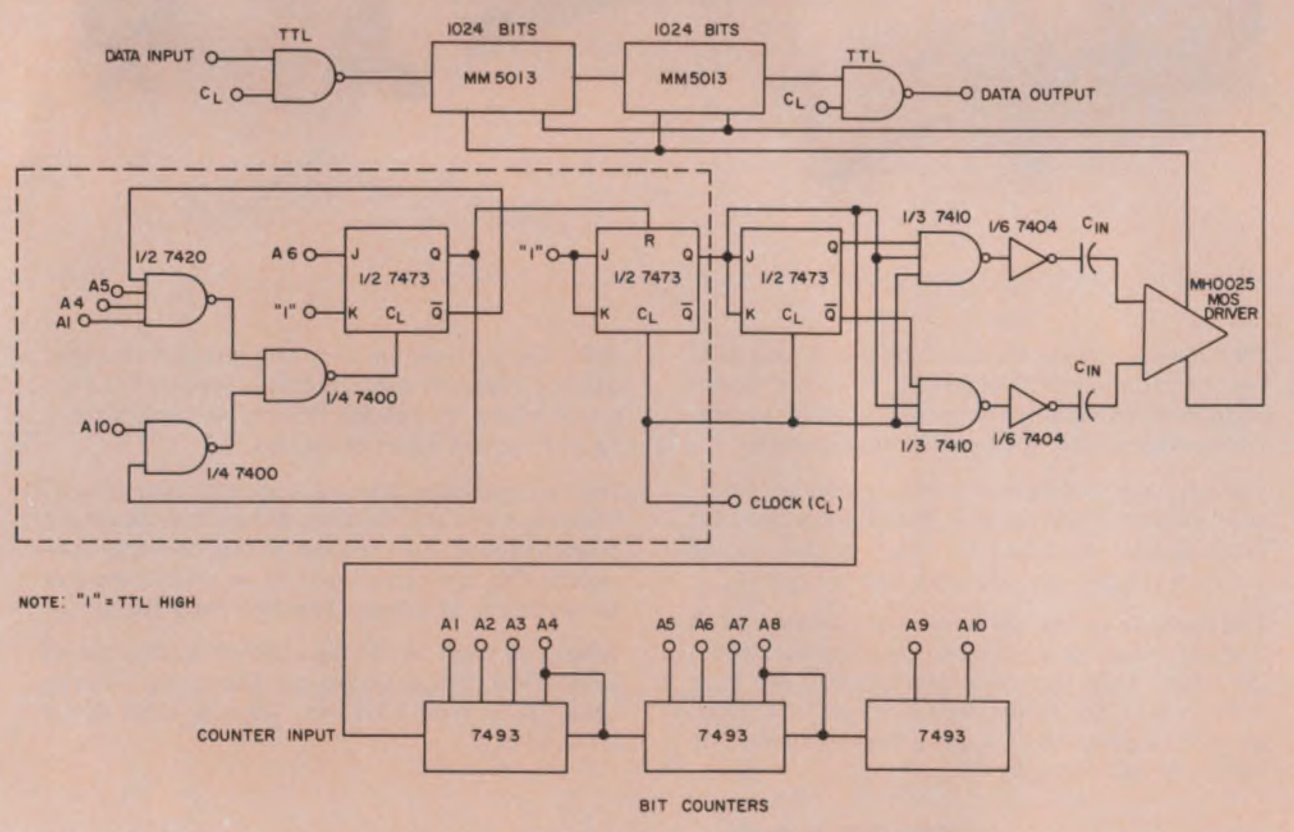
If a double frequency clock is applied for N of the normal data input intervals starting at a fixed point during the total recirculation time, the register will appear shorter by N stages and N clock periods (Fig. 1).

Fig. 2 shows the clock circuit arrangement. If N is equal to 2, a 1-0 input data sequence would be stored as 1-1-0-0. Since these data bits appear at the output at the time the clock frequency is again doubled, the output gate only detects 1-0.

Suppose a parallel array of eight 1991-bit registers is needed to store 1991 eight-bit words. This is shown in Fig. 3. The design of Fig. 2



1. **Doubling the input clock** rate allows artificial shortening of shift registers. The input clock is doubled for N periods (a) and then returns to the normal frequency (b). The output clock (c and d) follows the same patterns.



2. **A 2048-bit register has an apparent length of 1991 bits** when some external TTL control logic is added.

Leading IC manufacturers use it – and they can't afford to take chances in testing. They know that the 8007B delivers the pulses they need. And they know that the \$1,750 price is below competitive models.

Look at the specs of this fast pulse generator: rep rates from 10Hz to 100MHz, variable transition times from 2.0ns to 250μs, ±5V amplitude and ±4V dc offset. It's this kind of capability that you'll need for testing ECL II, ECL 10,000, and other comparable families.

Also note the generator's 50 ohm source impedance – mighty important for minimizing reflections when you're working with fast ECL. Today's testing also calls for a wide span of linear transition times, like the 2.0ns to 250μs of the 8007B. You can really use this when you're measuring propagation delay to a manufacturer's specs (even test linear devices).

In addition to ECL, the 8007B equips you to test most other IC families. You can, for example, measure the sensitivity of a flip-flop; or determine the noise immunity of TTL circuits by adding pulses onto as much as a 4V dc level. These types of tests are made possible because of the continuously variable ±4V offset.

If your test needs call for even higher repetition rates (to 200 MHz) or faster transition time (to 1.2ns), you may also want to look into its companion generator, the 8008A.

For more information on either the 8007B or the 8008A fast pulse generators, contact your HP field engineer.

For standards in pulse generators, think Hewlett-Packard.

083/3

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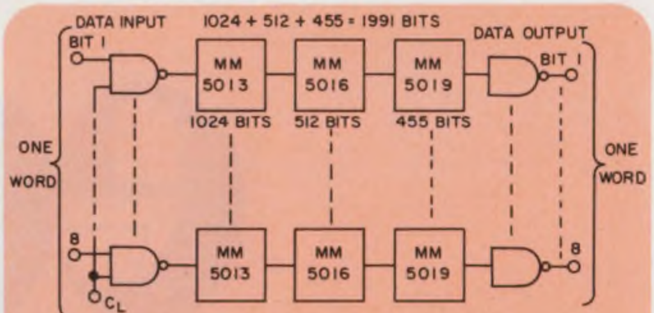
provides the required length with only two registers per bit of the eight-bit word. Therefore, the entire array can be built with 16, instead of 24 packages. The only addition to the overhead logic is the decoder and dual clock generator shown within the dotted lines of Fig. 2.

In this example, N equals 2048 minus 1991, or 57. Therefore the registers of Fig. 2 should be clocked at double frequency for the first 57 standard clock periods of the recirculation cycle. The extra logic decodes the bit-counter output and generates the 114 clock pulses that are needed.

Input capacitors of the clock driver are chosen according to the clock width desired—which depends on clock rate and duty cycle. The pulse width of the MH0025 varies from 100 to 1100 ns at C_{IN} values from 200 to 2200 pF. A nominal 1000-pF capacitor is suitable for a 1 MHz clock rate.

There are, however, some limitations to this technique. The normal clock rate should not be more than half the maximum allowable clock rate for the registers used. Also, if too many bits are subtracted, the clock-drive loading may be affected. The drive-power requirement is proportional to average frequency. For example, if a 2048-bit register is "shortened" to 1991 bits the required drive power will be increased by 57/1991 or 2.8%. In another example, if a 512-bit register is reduced to 397 bits, the increase in drive power is 28%.



3. **Use of the double clocking technique reduces the package count** of an equivalent register from 24 to 16. It also saves the cost of ordering a custom-masked MM5019 register.

Dale Mrazek, National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051.

CHECK NO. 312

Circuit applies power at precise phase angle

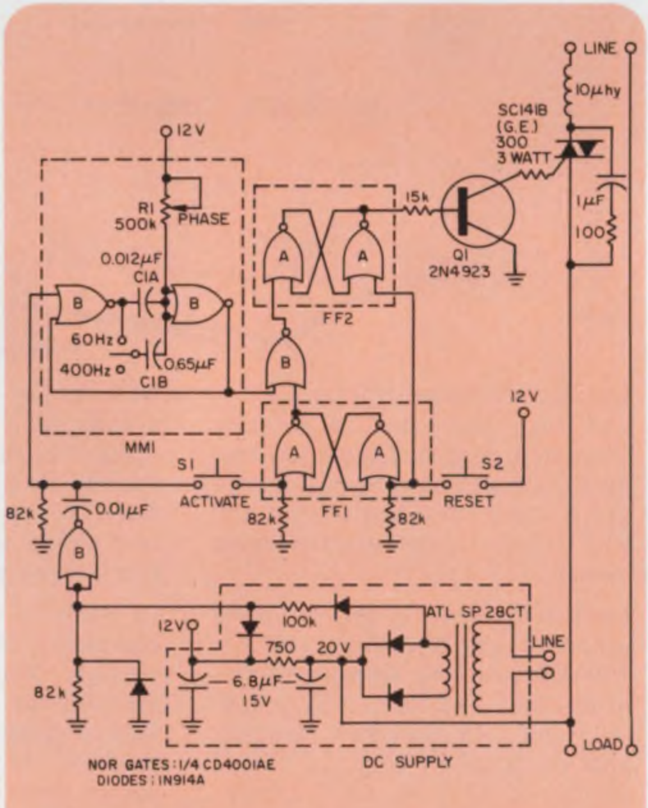
Precise measurements of power-line surges in ac supplies require that the input power be applied with a known initial phase angle. Two CMOS packages and a triac provide a reliable way to do this with either 60 or 400-Hz power lines. And the angle may be varied to determine worst-case conditions.

Pulses generated at the start of the positive half cycle are used as a timing reference. Pressing the Activate switch gates the next reference pulse into latch FF_1. The same pulse train also fires one-shot MM_1. Once FF_1 latches, one of the pulses from MM_1, ANDed by the output of FF_1, sets latch FF_2. The output of FF_2 biases the triac ON. Components R_1 and C_1 determine the pulse-width of MM_1 and hence the point on the ac waveform where turn-on occurs.

If R_1 is calibrated in degrees from 0 to 360, then C_1 may be padded to accommodate the two different power frequencies.

D. Newton and H. Yasothorn, Abbot Transistor Laboratories, Inc., 5200 W. Jefferson Blvd., Los Angeles, Calif. 90016.

CHECK NO. 313

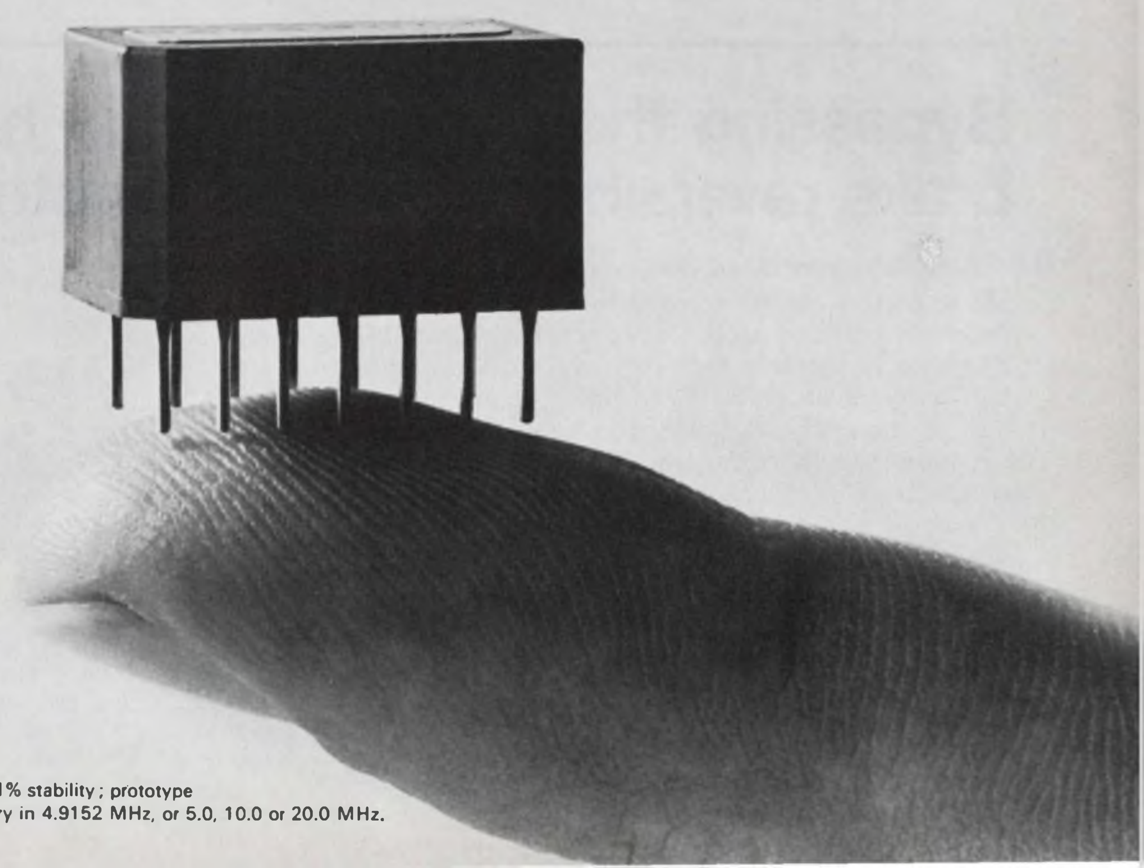


Initiation of load power occurs at a precise point on the ac waveform after depression of S_1. The controllable-pulsewidth of MM_1 (R_1, C_{1A}, C_{1B}) determines the moment FF_2 is latched and the triac gated on.

If you've been looking for a miniature crystal-controlled clock oscillator in a 14 pin DIP package to fit standard PC board sockets, stop looking and start ordering. Get details on model K1091A from Motorola Component Products Dept. 2553 No. Edgington Franklin Park, Ill. 60131

MOTOROLA

INFORMATION RETRIEVAL NUMBER 89



Specifications: 4 to 20 MHz range; 0.01% stability; prototype quantities available for immediate delivery in 4.9152 MHz, or 5.0, 10.0 or 20.0 MHz.

Ferrite toroids in hybrid ICs improve power efficiency and reduce heating

Power that would normally be dissipated in a resistor can be saved if the resistors are replaced by ferrite toroids (shielding beads) on conductors and the power-supply voltage is lowered. Shielding-bead inductors are very lossy—that is, they look resistive at high frequencies and can provide rf decoupling with almost no dc or low-frequency power loss.

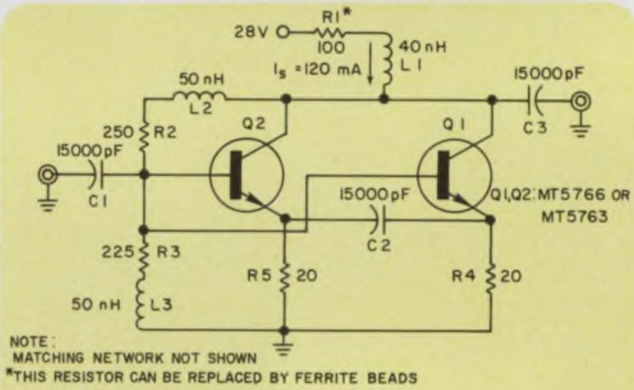
Resistances obtained with ferrite beads range from 30 to 50 Ω in the 50-to-1000-MHz region—typical of Ferroxcube material Type 3B or 4A. Therefore ferrite toroids can be used as rf resistors from about 50 MHz on up, provided the line length through a bead or string of beads is much shorter than a quarter wavelength of the highest frequency.

In the circuit example shown, a thin-film hybrid wideband amplifier provides a power-gain of 6 dB up to 500 MHz and has a thin-film collector resistor, R_1, of 100 Ω. The value of R_1 is selected to optimize ac power transfer and the dc biasing point. The circuit requires 120 mA for operation, and R_1 must pass all the current. The dc power dissipated in R_1 is 1.44 W, and the voltage drop is 12 V.

When R_1 is replaced with a conductor and two beads, the power-supply voltage can be lowered by 12 V—the amount that would otherwise be dropped in R_1. The circuit still sees an ac load of approximately 100 Ω, and there is a power saving of 1.44 W. Because power consumption is reduced, the thermal distribution is improved and efficiency increases.

Petre Sturzu, Hybrid IC Product Engineer, Fairchild-Microwave and Optoelectronics Div., 4001 Miranda Ave., Palo Alto, Calif. 94304.

CHECK NO. 314

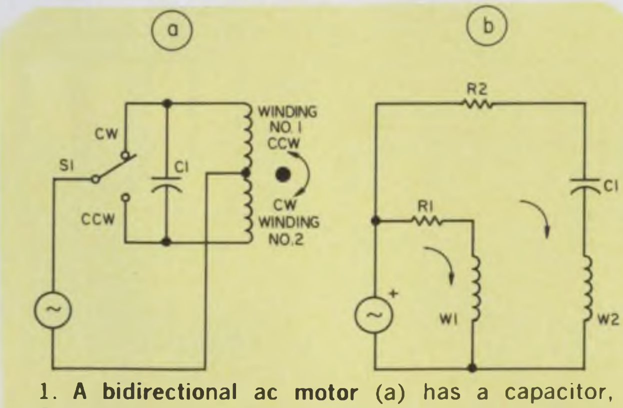


Replacing the 100-Ω resistor with ferrite toroids in this amplifier increases the efficiency. The circuit provides 6-dB power gain from 50 to 500 MHz.

Bypassing the phase capacitor helps brake reversible ac motors electrically

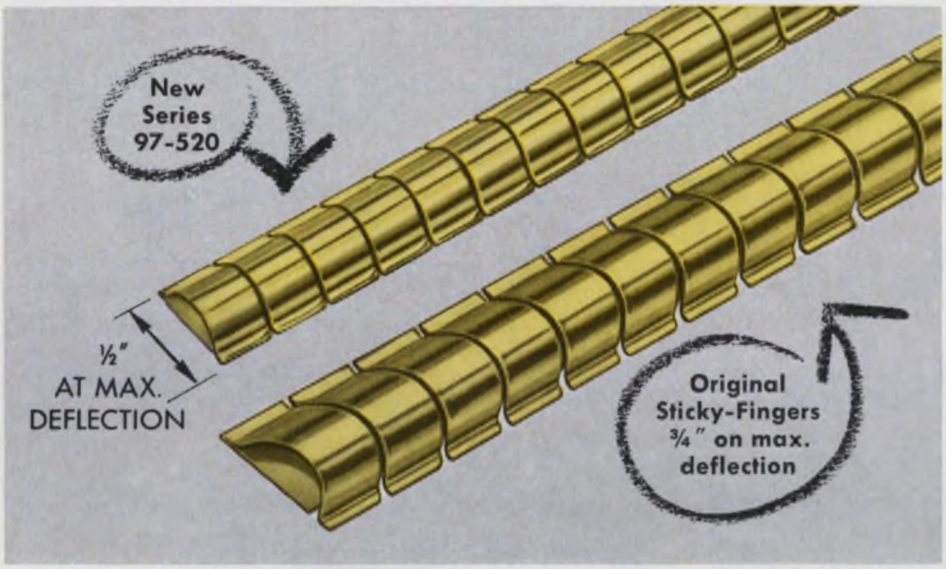
Split-capacitor three-wire or four-wire reversible ac motors do not respond to the conventional magnetic-braking techniques used with unidirectional ac motors. This is because the braking half-wave pulse train or dc flows through only half of the split coil motor. But by electronically bypassing the capacitor, you can brake reversible ac motors electrically.

Fig. 1a is simplified circuit of a typical three-wire, split-capacitor motor, and Fig. 1b is its equivalent circuit. For normal operation, S_1 is set to the cw or ccw position. Capacitor C_1 then creates an out-of-phase current in winding 2 (with respect to winding 1). The phase difference creates a rotating magnetic field that is synchronous with the input frequency and the



1. **A bidirectional ac motor** (a) has a capacitor, C_1, which creates a phase difference between the currents in the two windings, as shown in the equivalent circuit (b). Conventional dc braking won't work with this type of motor.

Greater RFI/EMI shielding in new, narrow-width contact strips from Instrument Specialties



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Series 97-500*—the original ¾" wide Sticky-Fingers. Specify when you require greatest possible shielding and where space permits. Also, supplied as 97-510 with Magnifil® for optimum magnetic shielding.

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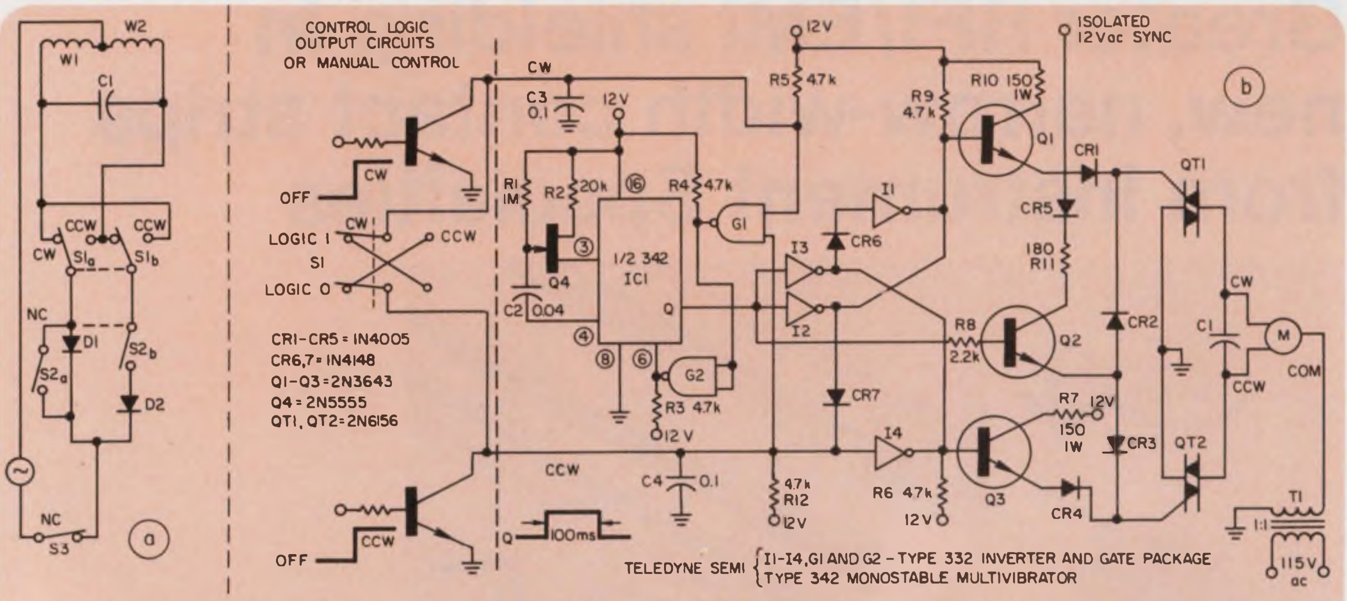
Phone 201-256-3500

*Patented

INFORMATION RETRIEVAL NUMBER 90



2. **Braking can be accomplished** by using a mechanical scheme (a) or electronic switching (b) to bypass C_1 through two triacs. IC_1 provides the necessary timeout to stop the motor.

number of poles. This rotating field establishes a flux linkage (torque) between the rotor and field. If a stationary field is momentarily switched in, the rotor will be subject to a braking torque of many times the original starting torque. Fig. 2a illustrates a manual version of the switching to accomplish braking. As shown in Fig. 2a, switch S_1 controls the direction of rotation, S_2 starts the pulse train (when S_{2a} is opened and S_{2b} is closed), and S_3 stops the pulse train. Diode D_2 helps eliminate the nulling of the stationary field set up in winding 1 by D_1. Therefore it effectively shorts C_1.

The circuit in Fig. 2b uses two triacs, Q_{T1} and Q_{T2}, for shorting C_1 and for determining rotational direction. In the cw mode, constant dc bias is applied to the gate of Q_{T1} via Q_1, CR_1 and I_1. Similarly for the ccw direction, Q_{T2} is held on by Q_3 and CR_4 via I_4. When S_1 is switched to the OFF position, G_1 and G_2 trigger a monostable multivibrator set for a 100-ms (depending on motor) pulse duration. A logic ONE at the Q output turns on Q_2, thus pulsing both triacs through CR_5, CR_2 and CR_3. Inverters I_2 and I_3 disable Q_1 and Q_3 while the monostable multivibrator is timing out. During this period the motor comes to a skidless stop.

Diodes CR_6 and CR_7 prevent simultaneous cw and ccw commands. They may be omitted if this possibility doesn't exist. FET Q_4 buffers the timing components, R_2 and C_2.

In selecting Q_{T1} and Q_{T2}, allow for twice the input voltage to appear across C_1. Therefore use a triac rated for greater than twice V_{in}. The use of dv/dt limiting network may be required with some motors (such as G.E. VP250-10 GE-MOV).

Keith Johnson, Canalco Bio-Med. Inst., Fisher Lane, Rockville, Md. 20852.

CHECK NO. 315

IFD Winner of January 18, 1972

Les Furnanz, Development Engineer, Fairchild Systems Technology, 3500 Deer Creek Rd., Palo Alto, Calif. 94304. His idea "Multiplexer technique solves X-out-of-Y bit pattern-recognition" has been voted the Most Valuable of Issue Award.

Vote for the Best Idea in this issue by checking the number for your selection on the Information Retrieval Card at the back of this issue.

SEND US YOUR IDEAS FOR DESIGN. You may win a grand total of $1050 (cash)! Here's how. Submit your IFD describing a new or important circuit or design technique, the clever use of a new component or test equipment, packaging tips, cost-saving ideas to our Ideas for Design editor. Ideas can only be considered for publication if they are submitted exclusively to ELECTRONIC DESIGN. You will receive $20 for each published idea, $30 more if it is voted best of issue by our readers. The best-of-issue winners become eligible for the Idea of the Year award of $1000.

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makes you an offer you can't resist

It's CTS Series 760 DIP cermet resistor networks, available "off the shelf" from authorized CTS Industrial Distributors. Thirty-five standard 760 series resistor modules (in 2 package styles) make it easy to be a time, space, and money saver. They *eliminate* lead forming, lead trimming, and individual component insertions . . . *eliminate* costly PCB real estate . . . *eliminate* up to 12 separate components.

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CTS CORPORATION
Elkhart, Indiana

A world leader in cermet and variable resistor technology.

Model 760-1

Resistance values 100 ohms thru 22K ohms. Applications: MOS/ROM pull-up/pull-down; open collector pull-up; "wired OR" pull-up; power driver pull-up; high speed parallel pull-up; TTL unused gate pull-up; TTL input pull-down; digital pulse squaring.

Prices (±2% std tolerance):	
1-99	$1.45
100-499	1.24
500-999	.91

Model 760-3

Resistance values 68 ohms thru 22K ohms. Applications: "Wired OR" pull-up; power driver pull-up; power gate pull-up; line termination; long-line impedance balancing; LED current limiting; ECL output pull-down resistors; TTL input pull-down.

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1-99	$1.25
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The complete line of CTS series 760 cermet resistor modules are in stock at:

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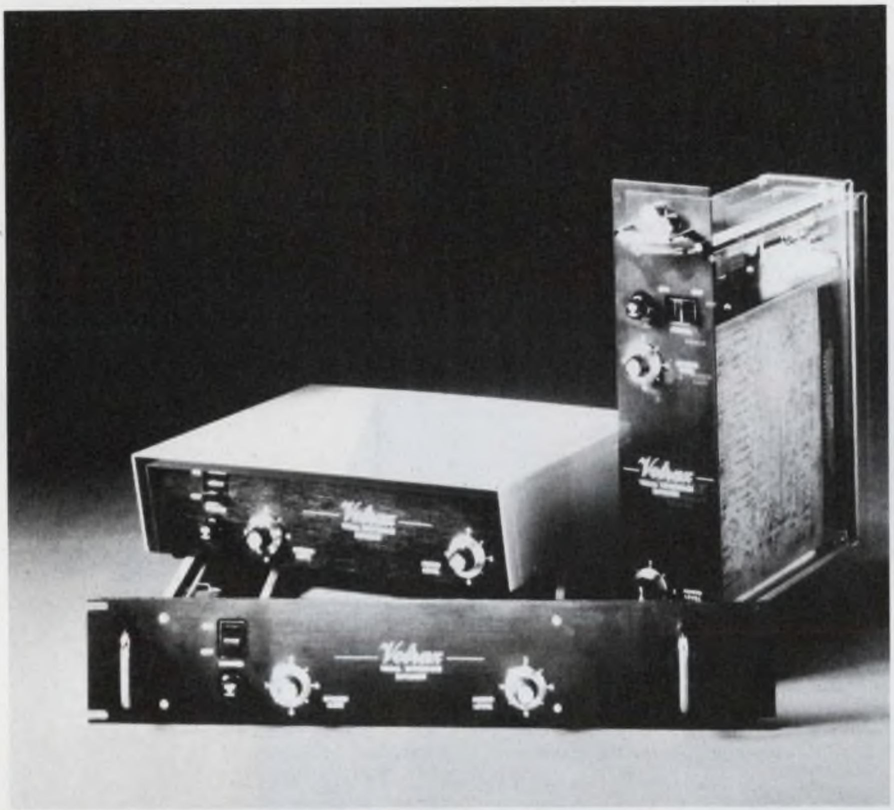
INFORMATION RETRIEVAL NUMBER 96

Computer Conference products

Synthesizer produces speech with 100-bit/s input data



Federal Screw Works, 3401 Martin Ave., Detroit, Mich. 48210. (313) 841-8400. Under $2000 (quan); 60 days.

With just a 100-bit/s input data rate, the VS-V Votrax voice synthesizer will speak in English and other languages. The vocabulary potential is said to be unlimited, as long as the proper sequence of eight-bit digital words are inputted. More conventional instruments require at least 10 times the bit rate of the VS-V Votrax.

The system forms words and sentences by generating the proper phonemes. An analog system comprised of low-frequency function generators and an active filter network generates the sounds. The function generators simulate the phonetic articulation, while the active filter network simulates the vocal tract.

Six bits of the eight-bit digital word specify the desired phoneme (the unit generates 60 phonemes), and the remaining two bits specify the inflection used. On the average, storage of 1000 bytes (eight bits) provides a vocabulary of 200 words (five bytes/word).

The VS-V synthesizer has no moving parts and accepts input data from a variety of sources, such as TTL-logic levels or standand RS-232 communications interface. There is no need to provide storage for a particular vocabulary, but a 500 word vocabulary (or more) can be provided within the unit. The user can develop his own vocabulary via an optional keyboard that provides access to all possible sounds. Or he can use the data patterns for a vocabulary already developed by the manufacturer.

The entire synthesizer is housed in a 12-by-11.25-by-3-in. cabinet containing the three 10-by-10-in. circuit boards that make up the unit—namely, the vocal-tract board, parameter-matrix board and an I/O board.

Booth No. 2000-2004 Check No. 255

Test modems with small hand-held data tester

Tele-Dynamics/Wanlass, 525 Virginia Dr., Fort Washington, Pa. 19034. (215) 643-6161. $495 (1-10).

The 7914A data-set tester is a small hand-held unit that can fully test data sets. The tester works with synchronous or nonsynchronous systems and with the simplex, half-duplex, or full-duplex modes. Data rates may be 150, 300, 1200, or 1800 bit/s in nonsynchronous applications; up to 9600 bit/s for synchronous applications. The 7914A provides a WECO-914B-compatible 63-bit psuedorandom pattern, and mark-hold, space-hold, or dotting patterns for performance evaluation applications. A frame pulse identifies the beginning of each 63-bit word. Bit error count is indicated by a two-digit display and overflow indicator.

Booth No. 2828-2830 Check No. 256

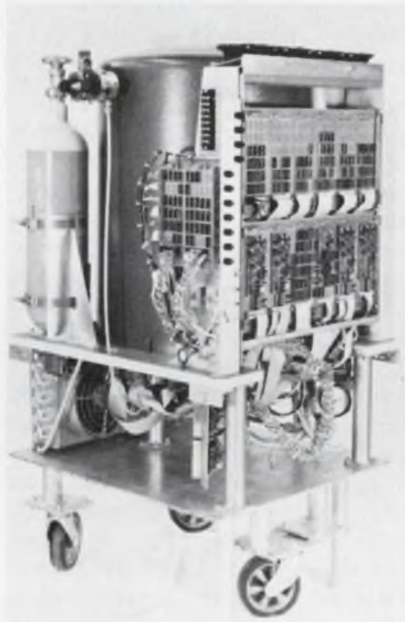
Real-time system supports many tasks

Digital Equipment Corp., 146 Main St., Maynard, Mass. 01754. (617) 897-5111. $5000; stock.

The RSX-11D real-time operating system allows PDP-11/40s and PDP-11/45s to keep many tasks going at any one time. In addition to maintaining critical response times the system provides time to process the collected data. The tasks include on-line data reduction, file updating, interactive program preparation, batch processing and process control. For best memory management, only high-priority tasks with microsecond-level response times have permanent memory allocations. The remainder of main memory is dynamically allocated among tasks that reside on disc. The RSX-11D supports 250 levels of task priority for detailed management of throughput.

Booth No. 2051 Check No. 257

Rugged disc-memory system accesses data in only 5 ms



Digital Development Corp., 5575 Kearny Villa Rd., P.O. Box 23447, San Diego, Calif. 92123. (714) 278-9920. See text; 120 days.

Computer applications like time-sharing or virtual-memory systems require rapid access to stored information—a requirement met by Digital Development Corp.'s 7600-series disc-memory systems. The low average access time of just over 5 ms for this disc drive is competitive with the 5 ms of IBM's Model-2305, Mod 2.

The 7600-series head-per-track disc drives are offered in three models—each capable of recording 75,000 bits/track with 64 tracks/disc surfaces. Models 7611, 7612 and 7613 contain a maximum of two, four or eight discs, respectively, thereby affording maximum storage capacities of 19.2, 38.4 and 76.8 Mbits.

These memory devices are designed to work in adverse industrial environments. They are shock-mounted within a hermetically sealed enclosure filled with dry inert gas. The units can withstand 2g shock and vibration, and they operate at ambient temperatures from 32 to 122 F. According to the manufacturer, the MTBF will range from 15,000 hr for the 64-track units (one disc, one surface) to 9000 hr for the 1024-track units (eight discs).

Within the enclosure, the discs revolve at 5760 rpm (50 to 60 Hz) to provide nominal data-transfer rates of 7.2 MHz. The switching time for changing tracks and read recovery is 25 μs. The combination read/write flying heads are organized into groups of 64. Each group services one disc surface. The heads never touch the recording surface and require no adjustment or calibration. There are also two spare heads in each group. If any of the regular heads, associated hardware or disc tracks fails, the user can reprogram the new address on a replaceable ROM, by means of an optional unit, and the new track is addressed whenever the defunct address is encountered.

In addition to the 7600-series, Digital Development also offers the A7310 (8.5 ms; 6.7 to 107.2 Mbits) and the 9100 (17 ms; 9.6 to 153.6 Mbits). Prices for these series range from $13,100 to $54,100. As with the 7600-series, these head/track memory devices are shock mounted within a hermetically sealed enclosure which is filled with a dry inert gas. The nominal data transfer rates differ from the 7600 series because of the lower rotation rates—4.4 MHz at 1760 rpm for the 9100 series and 6.2 MHz at 3520 rev/min for the A7310 series.

All drives include circuitry for reading, writing, track selection and generation of timing signals. Input and output signals interface at IC logic levels. Controllers are available for all models of DEC's PDP-11 ($4950) and for Data General's Nova 800, Nova 1200 and Super Nova ($2500).

Booth No. 1410 *Check No. 258*

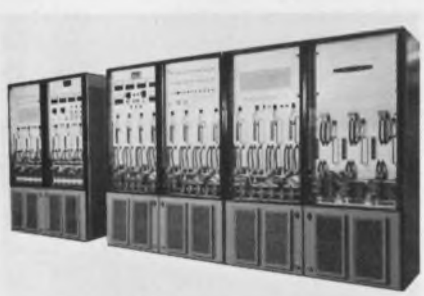
Rack-mounting case holds up to 16 modems

Com Data, 7544 W. Oakton St., Niles, Ill. 60648. (312) 692-6107. $835.

The 330 rack-mounted modem cabinet provides space for up to 16 modems in a 37-by-22-by-22 in. case. It also has a display panel indicating the status of four control and two data functions. The modems interface with data-access arrangements CBT and CBS (for automatic answering applications), the CDT (for manual operation) and private telephone lines (for dedicated applications).

Booth No. 2016 *Check No. 259*

Digitally controlled inverter senses faults



Exide Power Systems, Rising Sun & Adams Ave., Philadelphia, Pa. 19120. (215) 342-8000.

Named the "SuperGuardian," the system uses a digitally controlled stepped wave inverter with sub-cycle current control. The unit is available in ratings of either 200 or 125 kVA at 0.5 to 1 power factor. Its overload capacity is 125% of rated kVA for 10 minutes, to as high as 250% line-to-neutral current for 10 cycles. Transient recovery is accomplished within 50 ms for complete recovery to within ±1%. Either multitubular lead-acid, or pasted plate lead-acid cells may be used for the back-up battery.

Booth No. 1423 *Check No. 260*

Major editing features offered by cassette unit

International Computer Products, Inc., P.O. Box 34484, Dallas, Tex. 75234. (214) 239-5381. $2800.

The 3200 edit TermiCette operates on or off-line and offers the flexibility of two tape transports, with edit and tape-duplication features. All functions are incremental by character during recording, playback and editing. Personnel familiar with paper tape will find TermiCette operations simple and familiar. Control codes allow editing, skip or search operation to be conducted by character word, line or file. Record/play rates are selectable from 110 through 2400 baud and they are serial, asynchronous by character. Bidirectional search speed with automatic index is 350 char/s. A 300-ft. cassette stores in excess of 50,000 characters. Other members of the TermiCette family including a portable unit will also be on display. They offer a variety of operating speeds along with important editing features.

Booth No. 1602, 1604
Check No. 261

Mass tape-memory unit stores up to 10^{12} bits

Grumman Data Systems, 711 Stewart Ave., Garden City, N.Y. 11530. (516) 575-3034. Under $356,000; $11,800/mo., rental.

A mass tape memory, designed for IBM 360 and 370 systems running under OS, has up to 32-device addressability per computer interface. Units can be added as demand increases, with a total storage capability of up to one-trillion bits. Each storage unit holds the equivalent of 5000 conventional tapes. The system speeds information to the computer at data rates up to 14-billion bytes/s.

Booth No. 2427 *Check No. 262*

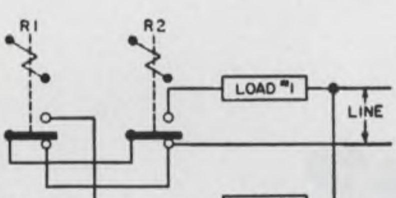
relays revisited

Until we can show you some of the many exciting relay ideas submitted to S-D's 50th Anniversary Contest, let's refresh ourselves with some basic relay circuitry.

"EXCLUSIVE/OR" . . .

A Fancy Name for a Simple Interlock.

A pair of SPDT relays easily connect as shown to prevent power from being applied simultaneously to two loads as in a motor reversing application. When relay R1 is energized and R2 is de-energized, power goes to load #2. Conversely when R2 is energized and R1 is de-energized, power is fed to load #1. When both relays are energized or de-energized, neither load receives power. This circuit works well with reed, sensitive, and other low power relays where mechanical interlocks are impractical.



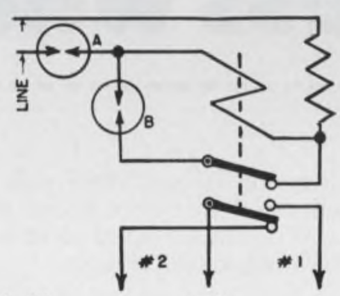
(Fig. I)

CHICKEN OR THE EGG?

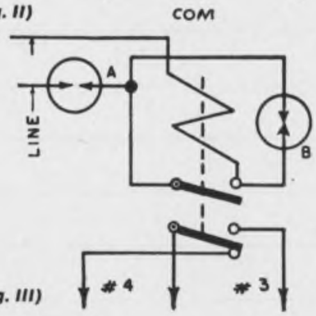
In many process control applications using 2 or more pilot switches it is necessary to insure that the first pilot to operate will dominate subsequent operation of all other pilots. More elegant than a simple interlock, sequence domination circuits come in many forms.

In Fig. II, normally-open Pilot A ordinarily controls the relay unless prevented by prior closure of Pilot B. If A closes first, relay energizes and subsequent closing of B has no effect on relay.

In the modification, Fig. III, normally-open Pilot A operates the relay unless prevented by the opening of normally-closed Pilot B. If B opens before A closes, subsequently closing A will have no effect. However, if A closes before B opens, subsequent opening of B will have no effect on relay.



(Fig. II)



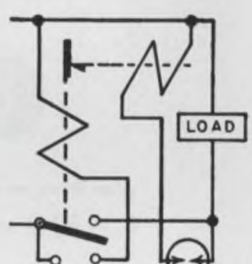
(Fig. III)

TRIP A MITE FANTASTIC!

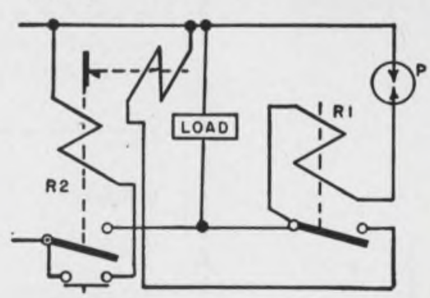
When pilot contacts can stand the moderate load required to operate the release coil of a latch relay, the circuit of Fig. IV shows how to trip the relay's load contacts. Momentarily closing PB will again reclose and mechanically latch the load contacts.

For more delicate pilots, have the pilot contacts operate a sensitive relay (R1) which, in turn, operates the release coil of latch relay R2 as in Fig. V.

For maximum sensitivity and pilot protection, combine sensitive relays and/or op-amps, or select hybrid devices such as Struthers-Dunn models 16-22 Micro-Sensitive dc relays. They'll trip on 1 μA and/or 0.7 volts.



(Fig. IV)



(Fig. V)

150 PAGES OF RELAYS FOR MOST ANY CIRCUIT.
The latest compilation of one of the world's broadest relay lines from the company that has developed an average of 9 new relay designs a month since 1923. Circle reader service card number for your copy.

STRUTHERS-DUNN, INC.

PITMAN, NEW JERSEY 08071

Canada: Struthers-Dunn Relay Div., Renfrew Electric Co., Ltd.

INFORMATION RETRIEVAL NUMBER 100

Fire protection system allows for modification

Fenwal Inc., Ashland, Mass. 01721. (617) 881-2000.

Automatic Halon 1301 fire suppression systems are safe for computer rooms, underfloor areas, tape storage vaults, etc. The automatic systems detect fires at early stages, send alarm signals and discharge extinguishing agents. Halon-1301 is a "safe-for-people" odorless, colorless, noncorrosive and nonconductive extinguishing agent that protects valuable data-processing equipment. A modular concept enables the user to relocate or modify a protection system as required, at minimum cost.

Booth No. 2007-2009 Check No. 263

Channel concentrator handles up to 32 callers

Timeplex, 65 Oak St., Norwood, N.J. 07648. (201) 767-1650. $3250; 60 days.

Data concentrators, such as the C-32, are used where a number of part-time users require random access to a smaller number of system ports. The C-32 is capable of switching up to 32 calling data sources (inputs) to a maximum of 16 called ports (outputs). The unit switches full duplex data and three control signals or clocks. Data to be switched can be synchronous or asynchronous with rates up to 9.6 kilobits/s. Selection of callers is regulated on a first-come, first-served basis in response to a control signal such as Ring Indicator or Carrier Detect.

Booth No. 2815-2817 Check No. 264

Interactive computer system can plot displays

Gerber Scientific Instrument, 83 Gerber Rd., S. Windsor, Conn. 06087. (203) 644-1551.

The Interactive Design System consists of a CPU interfaced to from one to six terminals. Each terminal has a satellite process controller which can support one or more work stations. Each work station has three separate modes: digitizing, editing, and plotting. None of these modes of operation can be used simultaneously, but the operator can switch modes very rapidly. From separate terminals, operations are independent. The basic Interactive Design System software lets the user dynamically construct, store, retrieve, manipulate, associate, edit and reproduce graphic or alphabetic engineering information visually and interactively.

Booth No. 1102 *Check No. 265*

Optical reader handles 650 documents/min

3M Co., P.O. Box 33600, St. Paul, Minn. 55101. (612) 733-1110.

The OCR System 1000 can read high speed printer, imprinter, typewriter fonts and mark-read documents at up to 650 documents/min. The OCR system offers on-line editing and allows flexibility in formatting. Including computer and magnetic-tape output, it is compatible with any data-processing system. An automated self-teaching adaptive recognition scheme allows almost all fonts to be learned without any hardware change. An all-digital scanner with a threshold detection scheme makes the system relatively immune to smears, light strokes and variations in document background. The System 1000 document reader can read up to three lines of print.

Booth No. 1701, 1703, 1705

Check No. 266

Card and key readers allow easy data entry

Addo-X, 437 Madison Ave., N.Y., N.Y. 10022. (212) 758-9171.

The Facit 4020 is capable of reading all kinds of tape material without adjustment, including colored tapes, oiled, Mylar and plastic tapes; also tapes of various thicknesses. Its stepping motor with capstan drive is said to provide gentle tape feed and a low noise level. The maximum speed is 300 char/s in both directions, and the reader tolerates up to 6% spacing error. Also available is the Addo-X KR-107 key reader. With the KR-107, pre-coding of the activating key prevents improper entry, and insures full system security. The 28 information bits are normally arranged to read as a BCD code structure, producing seven decimal digits of information. This configuration can be changed merely by changing bussing jumpers on the assembly.

Booth No. 1623, 1625, 1627

Check No. 267

Printer/plotter delivers 20-in. by 500-ft copies

Versatec, 10100 Bubb Rd., Cupertino, Calif. 95014. $8900 (2000); $10,900 (2000A).

The model-2000 matrix plotter and 2000A printer/plotter use 20-in. wide paper in 500-ft rolls and are designed for operation with computer systems of all types. They plot in an area 18.56-in. wide by any length up to 500 ft. The units are compact in design—28 (w) by 18 (d) by 38 in. (h), and weigh 190 lb. The power required is 115 V ac, 60 Hz; 100 V ac, 50 or 60 Hz; or 230 V ac, 50 Hz. Both units work with parallel, TTL-compatible voltage levels and accept serial RS 232 compatible signal inputs.

Booth No. 1815-1817 Check No. 268

CONFERENCE PRODUCTS

Serial impact printer has 96 character font

Printer Technology, Sixth Rd., Woburn Industrial Pk., Woburn, Mass. 01801. (617) 935-4246. $2800; 60 days.

The Printec 100A serial impact printer uses a 96-character font to provide upper and lower-case printouts. Key features of the new machine include 70 char/sec print rate (equivalent to 26 lines/minute at 132 columns/line), ability to print six-part forms on standard paper, a disposable ink roller instead of conventional ribbon, and the inclusion of a two-channel vertical format unit. Optional extras include buffers, different type fonts, eight-channel VFU, plus a range of interfaces.

Booth No. 1206-1208 Check No. 269

Tape drive can transfer data at 120,000 bytes/s

Wangco, 2400 Broadway, Santa Monica, Calif. 90404. (213) 828-5565. $5500 (OEM).

The Mod 1200 tape drive utilizes the IBM wrap-around cartridge. The Mod 1200 can also use reels without the cartridge—with the same automatic tape threading. The Mod 1200 offers tape speeds from 25 to 75 in./s, with vacuum columns, single capstan drive and IBM-head guide spacing. Transfer rates are to 120,000 bytes/s with data densities to 800 char/in. NRZI, 1600 phase encoded, or in 800/1600 dual-density combination.

Booth No. 2718, 20, 22

Check No. 270

Unit offers versatile data handling

Data 100 Corp., 7725 Washington Ave. S., Edina, Minn. 55435. (612) 941-6500. $61,950.

Statements entered by an operator via a CRT console or card reader define record and block length characteristics of the magnetic tape to the Model 75 Print Utility Station. The station consists of a nine-track 800 or 1600 byte/in tape transport, a 1000 line/min printer, a CRT console and a terminal control unit that contains 12,000 bytes of memory. Stored software also permits the user to control output print format. The current software accepts nine-track tapes from IBM 360 and 370 machines only. The company plans to implement other manufacturer's tape formats at a future date through software update.

Booth No. 2548, 2550, 2551

Check No. 271

CRT terminal affords extensive data editing

Tektronix, P.O. Box 500, Beaverton, Ore. 97005. (503) 292-2611. $2995; July 1.

Major features of the Tektronix 4023 CRT terminal include data formatting, on-screen editing and a full complement of upper and lower-case alphanumerics. Forms capability includes ruling (with optional package), visual effects such as blinking and blanked fields as well as logic formats such as transmit, nontransmit and protected. Editing features include character and line insertion or deletion, erase-to-end and erase page. The model 4023 has a capacity of 1920 characters (24 lines by 80 chars), provides switch-selectable baud rates of 110 to 9600 and is compatible with any system that uses TTYs.

Booth No. 2217 *Check No. 272*

Latest 12-bit DAC shrinks size and price to new lows

Hybrid Systems Corp., 87 Second Ave., Northwest Park, Burlington, Mass. 01803. (617) 272-1522. $35 (1-9); stock to 2 wk.

The Hybrid Systems DAC-373 has a lot going for it; a 12-bit digital-to-analog converter that fits in the space of two side-by-side, 16-pin DIP sockets—and for only $35. It is available in two versions: the I-12, which has a straight binary input, and the I-3-BCD, which accepts three digits of BCD.

The module size of both versions is only 1.1-by-1.7-by-0.385 in., including the current-steering switches, ladder network and reference source. Hybrid believes its closest competitors are the Datel Systems DAC 4912, or 6912, which have output op amps but cost from $4 to $24 more, the Zeltex ZD-433 or 432, which also have internal output op amps but cost from $4 to $14 more, the Cycon CY2635 or 2235 which also include the output of amps but also cost from $4 to $14 more and the Dynamic Measurements models 220 I12QZ, -V12-QZ or -3BCD, which also are more expensive than the Hybrid Systems unit.

The DAC-373 is a current-output unit that delivers 2 mA full-scale but has a voltage compliance of 1.25 V, which can be scaled for any desired output by an external op amp. Settling time is 1 μs to 0.05% of full scale for a major carry of ZERO and all ONEs, or all ONEs, and a LSB ONE input. Linearity is ±0.025%, equivalent to ±1 LSB for 12 bits. The power-supply voltages are ±15 V, and the reference source has a power-supply sensitivity of ±0.05%/%.

Deposited metal thin-film resistors help keep the temperature coefficient to a respectable 20 ppm/°C and help the unit to stay monotonic over the operating temperature range of 0 to 70 C. Hermetically sealed ICs and semiconductors are used throughout to offer high reliability. The digital inputs are TTL/DTL compatible.

Hybrid Systems CHECK NO. 250

Datel CHECK NO. 251

Zeltex CHECK NO. 252

Cycon CHECK NO. 253

Dynamic Measurements CHECK NO. 254

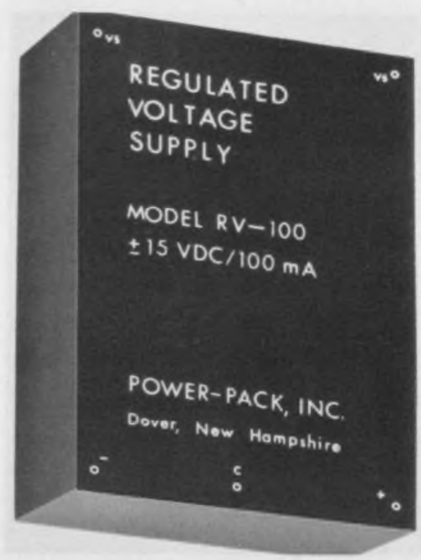
LED reflective scanner blocks ambient light

Skan-A-Matic, P.O. Box S or Rte. 5 W, Elbridge, N.Y. 13060. (315) 689-3986.

The S12001 reflective scanner contains a filter that effectively blocks all visible ambient light. Targets as small as 0.025-in. spaced 0.125-in. apart can be detected with a repeatability of ±0.001 in. White bond paper can be detected as far away as 1.5 in. and retroreflective tape from as far away as 4 in. The LED and phototransistor are matched for optimum performance and are epoxied into a sealed aluminum housing.

CHECK NO. 273

Op amp power supply gives 100 mA for $35



Power Pack, 1 Saint John St., Dover, N.H. 03820. (603) 749-2929. $35 (1-4); stock to 2 wks.

Four op-amp power supplies are the first products of this new company. Models RV-25, RV-60, RV-100 and RV-200 deliver ±15 V dc at 25, 60, 100 and 200 mA, respectively. All units feature 0.1% regulation, dual tracking and 0.5-mV rms ripple, except for RV-25, which has 1-mV rms ripple.

CHECK NO. 274

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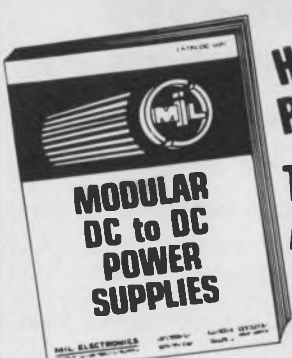

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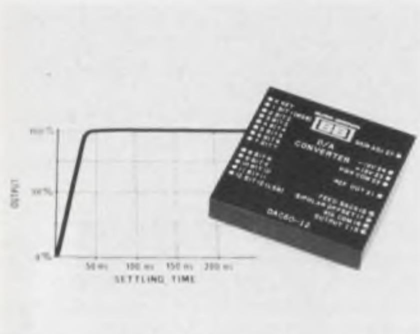
INFORMATION RETRIEVAL NUMBER 111

DAC differential linearity error is only ±1/2 LSB



Burr Brown, International Airport Industrial Pk., Tucson, Ariz. 85706. (602) 794-1431. $110 (10-bit in 1-9), $150 (12-bit in 1-9).

Most d/a converters have an integral linearity error of about ±1 LSB. In addition to that spec, Burr-Brown's DAC60 series specifies a differential linearity error of ±1/2 LSB, maximum. Most graphic-display terminals use d/a converters, and to minimize display distortion, the differential linearity error should be as small as possible.

D/a converters with the differential error unspecified can have a change from 0 to 2 LSB, going from best case to worst case. The DAC60 series has a specified differential error of only ±1/2 LSB, maximum. This error applies for either the 10-bit (DAC60-10) or 12-bit (DAC60-12) models.

Since the DAC60 is intended for use in display systems, the settling time for any LSB change is 25 ns to within 0.05% or 40 ns to 0.0125%, except for a major carry. For worst case (major carry), the settling time is 100 ns to 0.01%. Glitch width and amplitude are 15 ns and 10% of full-scale range (fsr), respectively. The gain error is ±0.1% of fsr, the offset error is ±0.001% of fsr, for unipolar signals and ±0.05% for bipolar signals. Both the gain and offset errors are adjustable to zero by external trimming. Accuracy varies by only 15 ppm/°C for the voltage-output mode and by 30 ppm/°C for the current output.

The power-supply requirements are ±15 V dc at ±50 mA, maximum, and sensitivity to supply variations is ±0.002%. The output range for current outputs is 0 to 5 mA, unipolar, with a 3-V compliance and ±2.5-mA, bipolar, with a 0-V compliance. Output impedance is 650 Ω for unipolar operation and 516 Ω for bipolar. The operating temperature range for monotonicity is 0 to 70 C, which can be extended to −25 to +85 C by relaxing some specifications.

CHECK NO. 275

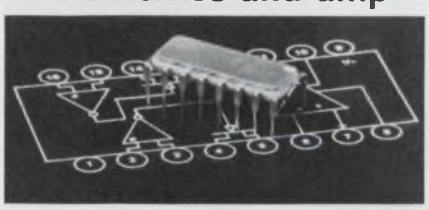
Opto-isolator has 75% current-transfer ratio

Dialight, 60 Stewart St., Brooklyn, N.Y. 11237. (212) 497-7600. $3.01 (1000 up); 2-3 wk.

There are two different versions of the 551-series opto-isolators, (suffixes -0001 and a -0004). The -0001 version has a rated ±4-kV isolation, maximum collector-base voltage of 50 V, maximum collector-emitter (off) voltage of 50 V, and maximum emitter-collector (on) rating of 6 V. Ratings of the -0004 part are slightly lower, but the unit has a current transfer ratio of 75% as compared to 40% for the -0001 unit. Both opto-isolators consist of a GaAs LED and an npn Si phototransistor mounted on four-pin frame and sealed in nonconductive plastic.

CHECK NO. 276

16-pin DIP houses two FET switches and amp

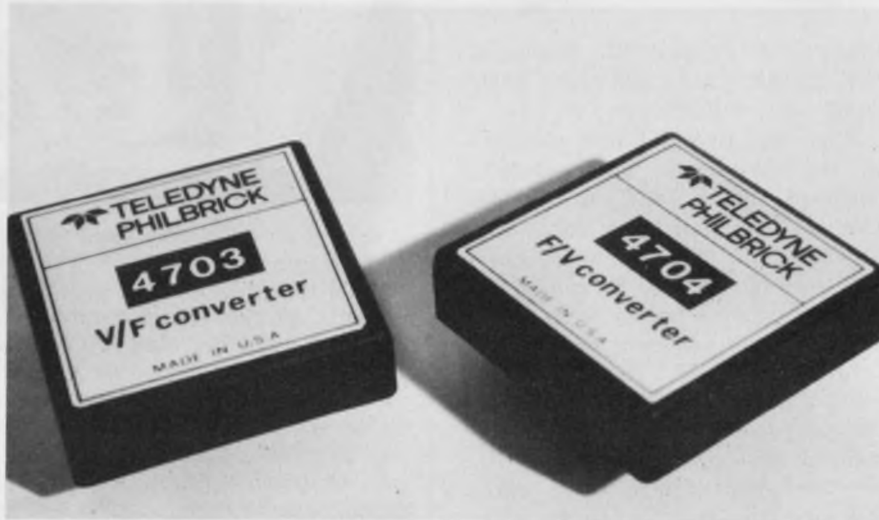


Teledyne Crystalonics, 147 Sherman St., Cambridge, Mass. 02140. (617) 491-1670. $39.75 (military, unit qty.) $29.75 (industrial, unit qty); 1 wk.

The CSH101 is a hybrid microcircuit containing two FET analog switches and a FET-input op-amp. All three sections are uncommitted. The sections can be connected in different ways to meet various applications. For the FET switches, the maximum ON resistance is 60 Ω and the turn-on or turn-off time is 1.2 μs. The amplifier has an open-loop voltage gain of 15,000, minimum. The military version is designated CSH101A and the industrial version is the CSH101B.

CHECK NO. 277

V-F and F-V modules convert signals over 100-kHz range



Teledyne Philbrick, Allied Dr. at Route 128, Dedham, Mass. 02026. (617) 329-1600. $69 (100 up); stock.

When combined, voltage-to-frequency (V-F) and frequency-to-voltage (F-V) modules can form the heart of low-cost data transmission systems. The Teledyne Philbrick 4703 (V-F) and 4704 (F-V) provide digital resolution equivalent to 13 bits at a cost of only $69 a module, in quantities of 100. The manufacturer says these are the lowest-cost V-F and F-V converters having a frequency range of 0-to-100-kHz. Units with a comparable frequency range are known to be available from at least one other manufacturer—Solid State Electronics Corp.—but at a price approximately $25 higher for the same quantity.

Linearity of the 4403 is ±0.015%, typical, and ±0.05%, maximum. The 4704 has a typical linearity of ±0.008% and a maximum of ±0.05%. Both units have an operating temperature range of 0 to 70 C, a power requirement of ±15 V at ±42 mA, a package size of 1.5 in. square by 0.4 in. high and MTBF (calculated according to MIL-Handbook-217A) of greater than 400,000 hours.

The 4703 has TTL-compatible output pulses and an input voltage range from 0 to 10 V. Its full-scale temperature coefficient is ±44 ppm/°C, typical, and ±150 ppm/°C, maximum, with a maximum drift of ±100 ppm of full scale. Settling time to 0.01% for a step input is one to two cycles of the new frequency plus 2 μs, and recovery from an overload takes 10 ms. The allowable capacitive load is 500 pF for rated performance.

The 4704 will output a dc voltage from 0 to 9.9 V ±0.1 V at rated load (adjustable to 10.000 V by use of an external 500-Ω pot) with an input frequency from 0 to 100 kHz. The input voltage can vary to ±15 V maximum without damage to the unit. A minimum voltage pulse width of 2.5 μs is needed to deliver rated accuracy. Output ripple is 50-mV p-p at a frequency of 10 Hz and 70-mV rms at 100 kHz. Output impedance is 0.1 Ω maximum, and a minimum output current of −5 to +20 mA is available. The filter time constant is 0.02 ms but can be increased externally if desired. Stability of the output vs temperature is ±50 μV/°C (±5 ppm/°C) maximum and vs time is ±30 μV/day.

Teledyne Philbrick **CHECK NO. 278**
Solid State Electronics **CHECK NO. 279**

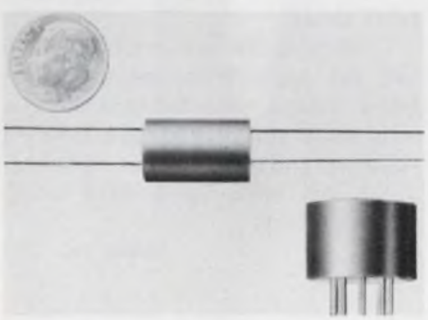
4-3/4-digit DPM has standardized dimensions

Electro-Numerics, 2961 Corvin Dr., Santa Clara, Calif. 95051. (408) 738-1840. $260 (OEM); stock.

A small, self-contained DPM has a resolution of 1/50,000 and an accuracy of ±0.003%. Features include a single-plane Sperry display readable at off-axis angles up to 130°. Model 386 is powered by 115/230 V ac and has standard TTL-level BCD output. Mechanically, the case is interchangeable with meters made by other manufacturers who have standardized on over-all dimensions of 1.8 (H) × 4.05 (W) × 4.56 in. (D). It can be mounted on a panel of any thickness and is front accessible. Overrange accuracy is not specified, but a flashing display provides overrange indication.

CHECK NO. 280

Chopper relay uses FETs for high linearity

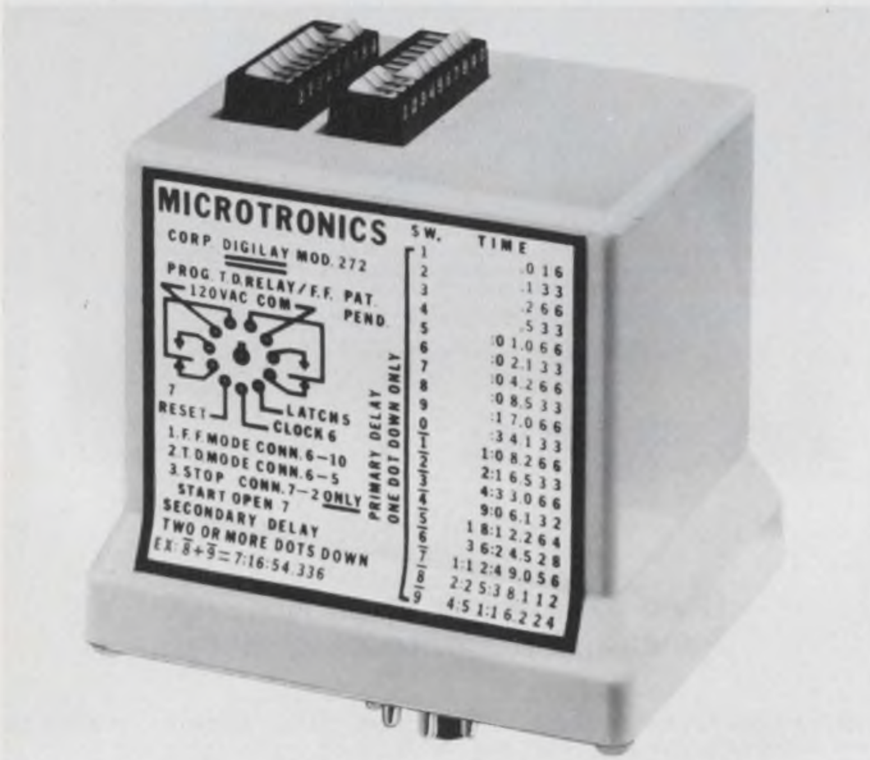


Solid State Electronics, 15321 Rayen St., Sepulveda, Calif. 91343. (213) 994-2271. $29 (100 qty); stock.

Models 33 and 33P FET chopper-relays have a linearity error of only ±0.005% with input frequencies up to 10 MHz. The solid state design has 20-μV dc offset, 50-μV noise, and will accept an input voltage from microvolts to ±5 V dc or 10-V pk-pk ac. The two versions are identical except for package style. Both models have an operating temperature range of −65 to +175 C.

CHECK NO. 300

Time-delay relay repeats cycles to 0.1% or better



Microtronics, 203 Gateway Rd., Bensenville, Ill. 60106. (312) 595-9330. $74 (unit qty); stock to 3 wk.

Most solid-state relays use analog RC networks to produce variable time delays. But Microtronics' M-272 has a proprietary counting scheme that combines MOS, high-threshold logic, 19 rocker switches and a phase-locked loop (PLL) to produce accurate, presettable time delays that range from 16 ms to over 9 hours.

Three modes of operation are possible with the M-272. It can operate as a normal time-delay relay when the desired delays are activated. It can also become a flip-flop: When one switch is depressed, the timer on-off cycle time is determined by the activated switch. Or it can operate as a pulser: When two or more switches are activated, the relay triggers as the sum of the individual delays "times out." The timer will then pulse at a rate determined by the smallest delay for a period equal to the largest. The operational mode is selected when the proper pins are shorted together.

The basic specifications for the unit are as follows:

- Output DPDT contacts are rated at 10 A and 120 V ac.
- Mechanical life is 10^7 operations.
- Timer accuracy follows the accuracy of the line frequency.
- Resolution is 16 ms.
- Repeatability accuracy is 0.1% or better, even at a maximum delay of almost 9-1/2 hr.

The timer is sealed in a standard, UL-approved plastic housing. The storage and operating temperature ranges are 0 to 75 C and 0 to 50 C, respectively.

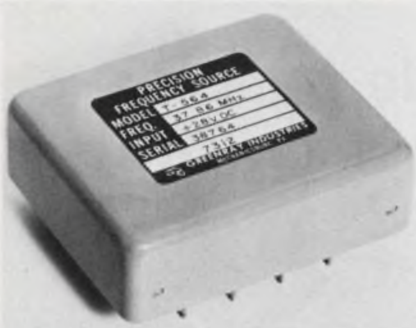
Because it uses a PLL, which locks onto the line frequency, the timer is practically immune to the line noise normally found in industrial environments.

The desired delay is determined by setting one or more case-mounted rocker switches, and by adding the delays assigned to the various switches, you obtain the total delay.

Custom units are available. You can get units with opto-isolation, fixed delays, nonstandard delays, solid-state relays and nonstandard voltages and frequencies upon request. All units come with a 90-day warranty.

CHECK NO. 301

Compensated oscillator doesn't need an oven

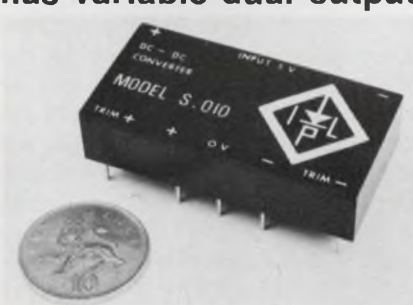


Greenray Industries, 840 W. Church Rd., Mechanicsburg, Pa. 17055. (717) 766-0223.

Temperature compensated crystal oscillators, models T-563 through T-569, provide frequency stabilities from $\pm 5 \times 10^{-7}$ over an ambient range of −40 to +70 C, without the use of an oven. This stability is attained by electronic compensation. Versions are available for frequencies from 3 to 600 MHz, and with sine or square-wave outputs that are compatible with TTL logic up to 100 MHz. Package size is approximately 5 in^3.

CHECK NO. 302

Miniature dc-dc supply has variable dual output

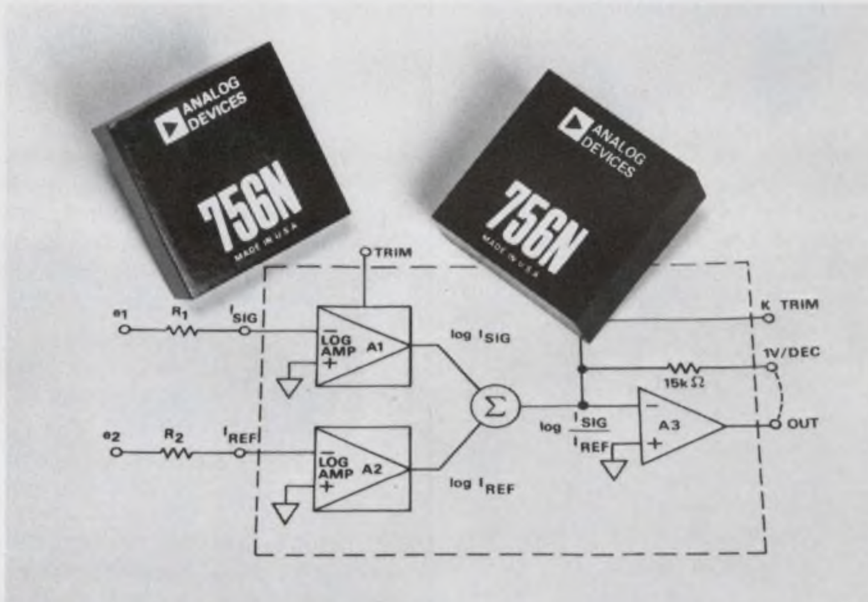


Integrated Photomatrix, The Grove Trading Estate, Dorchester, Dorset, U.K. Telex 41166. $42 (small qty.).

The S.010 dc-dc converter can convert the +5-V bus of TTL circuits into a positive and negative supply for driving op amps. The module features a 5-V-dc input, ±6 to ±15-V independently variable dual outputs, 1-GΩ input-to-output isolation, short-circuit protection, and 10-μs (to 0.1%) transient response. The unit has a 0 to 55 C operating temperature range and a full-load current of 30 to 40 mA for each output. Teknis of Plainville, Mass., is the U.S. distributor for IPL supplies.

CHECK NO. 303

Log-ratio module handles either voltages or currents



Analog Devices, Route 1, Industrial Park, Box 280, Norwood, Mass. 02062. (617) 329-4700. $75 (1-9); $42 (100 up).

To obtain logarithmic current ratios, most suitable function modules require that the inputs be true current sources. Analog Devices' Model 756 claims to be the first log-ratio module that will accept either current or voltage inputs and deliver an output voltage that is proportional to the log ratio of the two inputs. To accept voltage inputs, the 756 needs two external resistors—one in series with each input. This method of voltage-to-current conversion doesn't work with other log-ratio modules, since, unlike the 756, they don't have the required internal summing nodes.

The 756 consists of two signal input channels, one of which is a FET op amp capable of processing four decades of current. The other channel has a range limited to three decades of current.

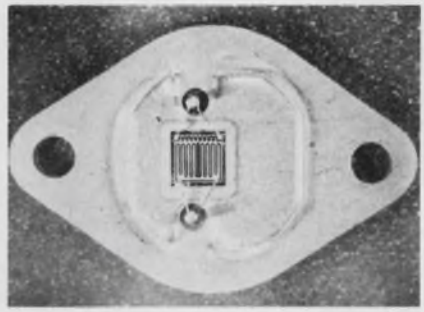
The basic specifications are as follows: the FET-amp's input current ranges from 10 nA to 100 μA (four decades), and the other amp's input current from 0.1 to 100 μA (three decades). The log conformity, or accuracy is $\pm 0.5\%$ over two decades and $\pm 1\%$ for four decades, with constant reference current and the output referenced to the input. The scale factor is 1 V $\pm 1\%$ $\pm 0.04\%/^\circ$C (positive for positive inputs and negative for negative inputs) and can be externally trimmed. Bias current is 10 pA for the FET amp, and it doubles every 10 C; for the other amp it is 10 nA max., $\pm 1\%/^\circ$C. Offset voltages are ± 1 mV with a 25-μV/°C change for the FET amp and 0.5 mV with a 30 μV/°C change for the other amp. The output offset is ± 10 mV with an 85-μV/°C temperature drift.

Power-supply voltages are ± 15 V at a current of 15 mA. Operational bandwidth depends very heavily on input current. The 3-dB bandwidth is 1 kHz at a current of 1 nA and increases to 10 kHz at 10-μA input current. For an increasing input current, the slew rate decreases from 50 to 10 V/μs, and for a decreasing input, it increases from 20 to 200 V/μs.

Aside from the internal summing node, the 756 also has one of the lowest prices for a log-ratio module. Typical prices for competing modules are $95 and higher for units that don't have the same versatility.

CHECK NO. 304

Darlington switches 20 A at 400 V



TRW Semiconductors, 14520 Aviation Blvd., Lawndale, Calif. 90260. (213) 679-4561. SVT6060: $15.54 (100 up); stock.

Monolithic Darlington amplifiers can switch 20 A at 400 V. The new Darlingtons have collector-to-emitter breakdown voltage ratings of 300 V (Type SVT 6060); 350 V (SVT 6061) and 400 V (SVT 6062). The saturation V_{CE} is 2 V, and typical switching time is 300 ns. Units are housed in a standard TO-3 package.

CHECK NO. 305

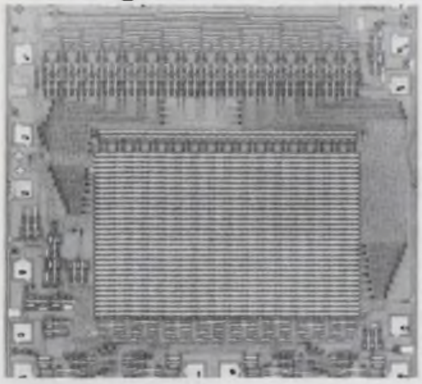
14-pin DIP houses dual zero-crossing detector

Signetics, 811 E. Arques Ave., Sunnyvale, Calif. 94086. (409) 739-7700. $2.15 (unit qty).

The 363 is a monolithic, dual, zero-crossing detector, with a differential-amplifier input and a TTL-compatible output. The input amplifier is referenced to zero volts and employs temperature compensation to ensure stable thresholds. Low-level analog waveforms may be converted to digital signals as long as they exceed ±30 mV. The power requirements are either +5 V, and −6 or −12 V. Manufacturer's instructions must be observed in wiring the −12 or −6 V pins to avoid destroying the internal zener diode.

INQUIRE DIRECT

1024-bit CMOS ROM is the largest available



Motorola, P.O. Box 20912, Phoenix, Ariz. 85036. (602) 273-6900. $24.70 (AL), $13.75 (CL) (100-up); 10 wk.

Desigated the MCM14524AL/CL, the 1024-bit memory is a mask-programmable ROM. The ROM pattern is specified by the user. Organization is a 256 × 4 bit pattern. V_{DD} ranges from 3 to 18 V dc for the A-suffix and 3 to 16 V dc for the C-suffix. Latches at data outputs and full-address decoding are included on the chip. Operational power requirements are around 135 μW at a 10-kHz clock rate. There is no mask programming charge for 500 qty and up. The MC14524AL is rated for operation over −55 to +125 C, while the −CL version is guaranteed over −40 to +85 C. Each type is in a ceramic 16-pin DIP.

CHECK NO. 306

Trim package count by using monolithic SARs

Advanced Micro Devices, 901 Thompson Pl., Sunnyvale, Calif. 94086. (408) 732-2400. From $7.10 (100 up); stock.

The Am25L02/03/04 devices are low-power successive-approximation registers. Circuits in the family are: Am25L02—an eight-bit unit with serial or parallel data output, Am25L03—an eight-bit unit for expandable parallel data output and input enable, Am25L04—a 12-bit unit with both serial and parallel output and input enable. Power dissipation is 110 mW (12-bit version, 150 mW) at typical speeds of 5 MHz. There are two temp ranges available—MIL and commercial, and three package styles—hermetic DIP, molded DIP, and flatpacks.

CHECK NO. 307

Quad OR or NOR gates have 6-ns delay

Signetics, 811 E. Arques Ave., Sunnyvale, Calif. 94086. (408) 739-7700. $3.40 (100-up); stock.

The 82S41 (Schottky clamped TTL) contains four 2-input at Exclusive-OR gates that have a propagation delay of 6 ns. Outputs of the 82S41 are totem-pole structures characteristic of TTL. The 82S42 has four 2 input Exclusive-NOR gates which implement comparison functions. Functional outputs of the 82S42 are bare collector to facilitate implementation of multiple bit comparisons—a four bit comparison is made by connecting the outputs of the four gates together.

INQUIRE DIRECT

INFORMATION RETRIEVAL NUMBER 126

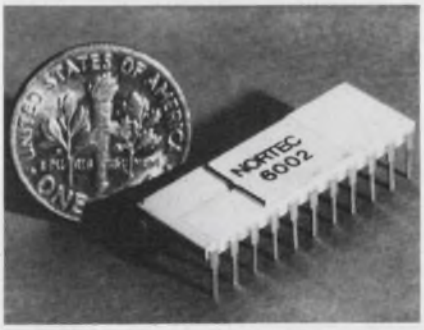
750-mA rectifier diodes offered

Texas Instruments, P.O. Box 5012, M/S 308, Dallas, Tex. 75222. (214) 238-3741. 29¢ to 46¢ (100 up); stock.

A family of six 750-mA silicon-rectifier diodes, types 1N2069-71/A, features double-plug construction and moisture-free stability through hermetic sealing. Peak reverse voltages range from 200 to 600 V. Static reverse current for suffix A versions is 5 μA; for the three 1N2069-71 types, it's 10 μA. Average reverse currents are 50 and 200 μA, respectively.

CHECK NO. 308

1024-bit RAM has 150-ns access



Nortec Electronics, 3697 Tahoe Way, Santa Clara, Calif. 95051. (408) 732-2204. $11.60 (100-999).

A 1024-bit p-channel dynamic random access memory, the NEC-6002, has an access time of 150 ns and a dissipation of only 180 mW. Periodic refreshing is required at 32 cycles every 2 ms. The memory is fully decoded and its differential outputs can be OR-tied.

CHECK NO. 309

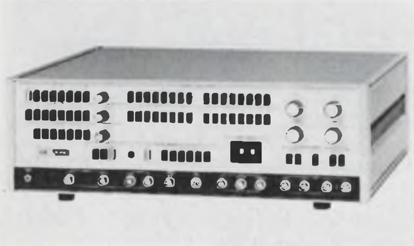
Bipolar/MOS interface fits in TO-100 package

Integrated Microsystems, 16845 Hicks Rd., Los Gatos, Calif. 95050. (408) 268-2410. $9: 7800 (100-up); $6: 8800 (100-up); stock.

Dual-voltage translators in 10-pin, TO-100 packages offer a 31-V max output swing and a power dissipation of 1 mW. Type μIS 7800 is rated for −55 to +125 C; type μIS 8800 operates from 0 to +70 C. Both units are electrically identical. Operation is from a 5-V supply and the dual-channel translators are compatible with all MOS devices.

CHECK NO. 310

Data generator doubles as receiver/comparator



Systron-Donner, Datapulse Div., 10150 W. Jefferson Blvd., Culver City, Calif. 90230. (213) 871-0410. $2025; August.

Here's a data generator that's also a receiver/comparator and pseudorandom transmitter. The Model 229 features dual 16-bit channels, with a combined single-channel capability of 32 bits, and also selected pseudorandom sequences of 15, 63, 511, 2047 and 32,767 bits. A comparator permits a bit-by-bit check of received data, simultaneously with data generation.

Formats include data-content selection from 1 to 32 bits in single-channel operation and 1 to 16 bits in dual channel. One of the channels may be delayed up to 100 ms with respect to the other—in either single or dual-channel mode—to permit simulation of two, skewed bit streams.

The delay in the pseudorandom mode compensates for delays in the received data. Data formats offered are NRZ or RZ, with variable width to 100 ms.

Clock rate is variable from 10 Hz to 10 MHz, and the Model 229 may be externally or manually triggered by pushbutton control. The data stream may be recycled continuously or limited to one data word, triggered by an external-command pulse. A manual reset is provided to return to the first bit at the user's option.

A sync-reset pushbutton is available, which, when used in the pseudorandom mode, permits the receiver to synchronize on the first 32 error-free bits. There is also a sync-lock light as an indication of receiver synchronization to the received data. When errors of roughly more than 40% are detected, the light goes out.

CHECK NO. 320

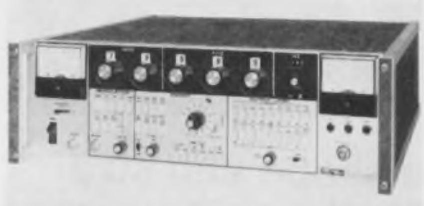
Meter reads picoamps and also megohms

The London Co., 811 Sharon Dr., Cleveland, Ohio 44145. (216) 871-8900. $980; stock.

Model IM6 is two meters in one. It combines a wide-range picoammeter and a stable megohmmeter. The meter display has two scales, a logarithmic one covering nine decades and an expanded scale covering two decades. The expanded scale provides superior resolution, while the single nine-decade scale is useful when the value is unknown or is varying widely. Output includes analog levels of 500 mV per decade for recording and limit sensing purposes. The picoammeter reads from 1 pA to 1 mA, and the megohmmeter measures resistance values between 1 and 10^9 MΩ. A digitally-controlled test voltage supply is incorporated in the megohmmeter which can be set to any value between 1 and 999 V in increments of 1 V by means of thumbwheel switches.

CHECK NO. 321

Synthesized sig gen is programmable

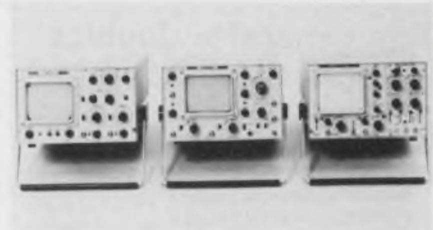


PRD Electronics, 1200 Prospect Ave., Westbury, N.Y. 11590. (516) 334-7810. $3980.

The 7808 sig gen is a solid-state unit that can be used as a digital frequency synthesizer with frequency standard accuracy, as a conventional signal generator, or as a sweep generator. Operation is from 0.05 to 80 MHz, with tuning in 1-kHz steps. The vernier control can be set for frequencies between the 1-kHz steps, with 1-Hz resolution. The unit features remote programming, digital frequency selection, FM/AM, pulse, manual and automatic sweep. Other specs are: 1 part in 10^6/mo. stability; output of 0.1 μV to 10 V rms into 50 Ω; spurious 60-dB down; and harmonics 30-dB down.

CHECK NO. 322

Three new scopes offer 10, 20 and 40-MHz bw



Ballantine Laboratories, P.O. Box 97, Boonton, N.J. 07005. (201) 335-0900. 1040A: $1200; 1066B: $745; 1010A: $495.

The top-of-the-line unit of three new scopes is the Model 1040A, a 40-MHz, dual-channel instrument with delayed and mixed sweeps, a 10-kV, 8 × 10-cm CRT, and a sensitivity of 1 mV/cm on each of its two identical vertical channels. The second scope is the Model 1066B: Replacing the 1066A, it has greater bw (20 MHz vs 15 MHz) and has a larger display (an 8 × 10-cm vs 6 × 10 cm). The third member of the family, the Model 1010A, is an economy model with dual-channels, 10-MHz bw and 5 mV/cm sensitivity.

CHECK NO. 323

Unit converts analog to digital & stores data

General Radio, 300 Baker Ave., Concord, Mass. 01742. (617) 369-4400. $1600.

The 1716 Reference Storage Unit permits automatic frequency-response error updating, rapid comparison measurements, and digital data logging of analog signals. The unit is primarily intended to enhance the performance of the GR 1710 RF Network Analyzer. The 1716 accepts any ±0.5-V analog signal, converts up to 256 points to eight-bit digital data and stores the data in memory. The stored data can then be displayed directly or subtracted from a second signal and displayed as a difference.

CHECK NO. 324

Logic circuit checker emits sounds

Canon Inc., 9.9 Ginza 5 Chome, Chuo-ku, Tokyo 104, Japan. (03) 572-4251. $90 to $105; 30 days.

A new logic circuit (DTL and TTL) checker, called Logictone, weighs only 80 g and can detect and tell by sounds, circuit disconnections, malfunctioning elements and over-loaded circuits. The checker can also measure single pulses to 25 ns and pulse trains to 20 MHz.

CHECK NO. 325

Dual-channel scope weighs just 14 lb.

Dumont, 40 Fairchild Pl., W. Caldwell, N.J. 07006. (201) 575-8666. $1195; 30 days.

The dual-channel 2100G is a portable scope with dc to 10-MHz BW, sensitivity of 10 mV/div, sweep speed of 50 ns/div, 8 × 10 div display with 6.5-kV accelerating potential and delayed sweep. The unit weighs only 14 lb. Integrated circuits assure high reliability: Field proven MTBF exceeds 5000 hours. Included in the 2100G are full auto-triggering single sweep and verniers on vertical and time base controls.

CHECK NO. 326

Sweep generator shows frequency and amplitude

Wavetek, P.O. Box 651, San Diego, Calif. 92112. (714) 279-2200. $1295; 30 days.

Model 147 is said to be the first generator with digital display of frequency and amplitude. A front panel LED display shows the frequency and positive/negative peak voltages of the output signal with 3-digit resolution. Generator output is thus set up without a need for verification with other instruments. The Model 147 is a source of 0.0005-Hz to 10-MHz sine, triangle, square, positive pulse and negative pulse waveforms, each with variable amplitude, dc offset and symmetry. The 147 can be operated in a continuous-output, triggered, gated, continuous-sweeping, triggered-sweep or sweep-and-hold mode.

CHECK NO. 327

Adapter measures ac-current leakage

Triplett Corp., 286 Harmon Rd., Bluffton, Ohio 45817. (419) 358-5015. 60-413: $30; 801: $210; stock.

Ac-current leakage adapter Model 60-413 permits checks of leakage current between patient-connected instruments in hospitals. It also measures leakage current of commercial appliances. The unit plugs into Model 801, V/Ω/mA meter. The adapter, in 8 ranges, measures from 10 μA to 30 mA. Resolution is 0.2 μA on the lowest VOM range. Accuracy is ±4% of full scale. Frequency response approximates C. F. Dalziel's 50 percentile threshold of perception curve, within ±1.0 dB. Input impedance is selectable for medical (500-Ω test load) or commercial appliance (1500-Ω test load) leakage measurements.

CHECK NO. 328

Digital processing scope for complex calculations

Tektronix, P.O. Box 500, Beaverton, Ore. 97005. (503) 644-0161. $5200; see text.

The P7001 digital processor provides a signal interface between a 7704A oscilloscope and a minicomputer. The combination thus formed can do complex computations such as FFTs, signal averaging, convolution, differentiation, integration, rms, multiplication, division, addition, subtraction, squaring, cubing, or any other mathematical transformation you can write a program for. It contains all the required signal-routing circuitry, a/d and d/a converters, 4-k words of core memory (10 bits/word), and an input/output interface to process CRT readouts from the computer.

Without a computer the P7001 can handle only simple digital storage and playback. The following comprises the basic equipment required to use the processor: a PDP-11/05 or Nova minicomputer with 8 or 16-k words of memory, a 7704A oscilloscope, a teletypewriter or input terminal, and the Tektronix APD BASIC-1 or -2 software. (It is assumed that the required plug-ins for the 7704A are available.)

Essentially the system works as follows: Programs are loaded into the minicomputer and operate on the digitized information from the processor. After the data is analyzed, it is stored digitally and displayed on the CRT using a d/a converter and vector generator to give a continuous display (instead of the sampled output that would appear directly out of the d/a converter).

Building the system from scratch, the estimated cost for an elementary system is slightly over $20,000. Many options are available to the user depending on plug-ins, computer size and need.

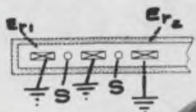
CHECK NO. 329

Ansley

Lowest Crosstalk Yet!

Black Magic™ Cable For Fast Rise Time Pulses

Here is lightweight flexible cable . . . easy to terminate . . . flame retardant (UL listed) outer jacket . . . can be used singly or in layers without crosstalk interference.



We can prove it — too!

Far End Crosstalk on Twisted Pairs (14%)

Far End Crosstalk on Black Magic™ Cable (1.6%)

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INFORMATION RETRIEVAL NUMBER 132

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where accuracy of speed control or high damping is required

PITMO® motor-tachs have a diameter of 1.18″ exclusive of terminal blocks, and a length of 3.66″ exclusive of shaft extension and pilot boss. Standard 12-volt unit provides stall torque of 3.6 oz.-in. and No-load speed of 4,100 rpm.

Separate motor and tachometer-generator armatures are mounted on a single shaft and operate within two different field magnet systems. Tachometer gradient is two volts per 1,000 rpm with typical ripple of 5% peak-to-peak with no filtering.

Other windings are available for both motor and tach. For more information, write today. 113

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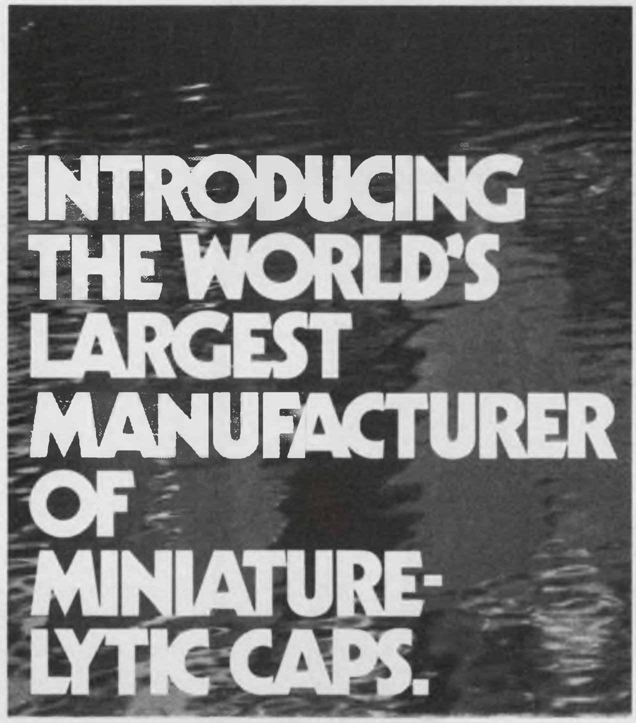
INFORMATION RETRIEVAL NUMBER 133



Now, through United Chemi-Con, everyone can get what it used to take a purchasing agent in Tokyo to get: reliable capacitors at competitive prices from Nippon Chemi-Con.

Our higher level of automation ensures consistent dependability and enables us to produce over 60 million capacitors a month. And now our fully-stocked U.S. warehousing system can give you the fast delivery you're accustomed to.

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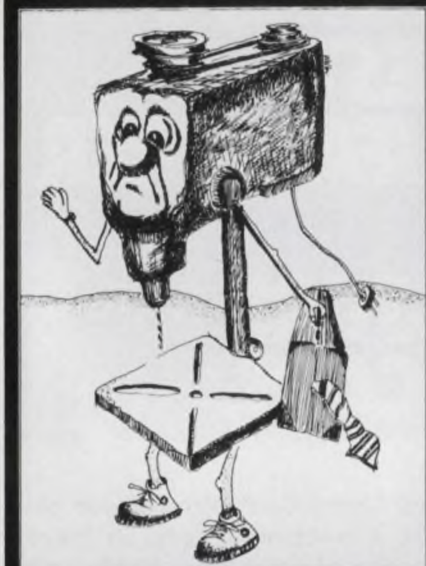
INFORMATION RETRIEVAL NUMBER 134



Inductor chip replaces units 10 times larger

Vanguard Electronics, 930 W. Hyde Park Blvd., Inglewood, Calif. 90302. (213) 678-7161.

Super Q, chip inductors are only ant-sized but replace chokes and coils 10-times larger. The magnetically-shielded, transfer-molded chip inductors measure 0.160 × 0.125 × 0.125 in., have an inductance range from 0.1 to 1000 μH and the Q ranges to 80. A typical Q is 75 min for a 56-μH chip at a 2.5-MHz test frequency. The inductors are not only compatible in size and configuration with conventional chip components, but they are also suitable for reflow soldering and for automatic insertion. The units meet MIL-C-15305 and operate from −55 to 125 C.

CHECK NO. 330

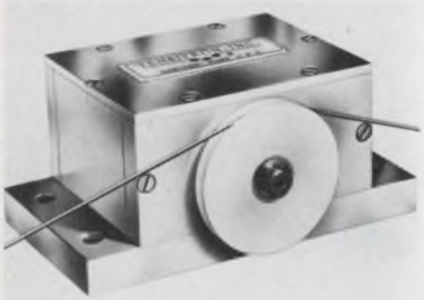
Solid-state relay can sense resistance change

Regent Controls, Inc., Harvard Ave., Stamford, Conn. 06902, (203) 348-7734. $21 (100 up).

The all solid-state relay, SR510, for use in 115-V ac control circuits, can be controlled by a variable resistance or contact, such as: precision positioning electrodes, limit switches, pushbuttons, float switches, reeds or relay contacts in either a NO or NC style. The SR-510V10 unit uses 10 V ac in the control circuit. The SR510V40, with 40 V ac in the control circuit, should be used where control contacts are subject to problems of dirt buildup.

CHECK NO. 331

Load cell has fractional gram sensitivity



Tensitron, 160 Harvard Depot Rd., Harvard, Mass. 01451. (617) 456-3511.

A new low-force load cell is furnished with a rotating pulley or cylinder on ball bearings that can be used for checking the tension on wires, yarns or tapes. Several models provide a range to 10 lb. Fractional-gram sensitivity results from the use of special load columns and standard 350 Ω bonded strain gauges. Excitation voltage is between 5 and 10 V. Output is 2.5 mV/V.

CHECK NO. 332

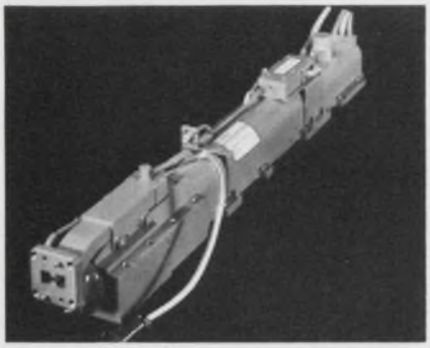
Optical switches come in gain or speed types

Spectronics, 830 E. Arapaho Rd., Richardson, Tex. 75080. (214) 234-4271. 1636: $5.10; 1637: $5.90; (1000 up); stock.

Designated the SPX 1636 and SPX 1637 series, this line of optical switches offers either phototransistors or photo Darlingtons and uses an infrared LED aligned with the photosensor across a gap. Two package sizes are available: in the 1636, the optical gap is 0.2 in.; in the 1637, the gap is 0.375 in. The phototransistor features fast-switching, typically 8 μs. The photo Darlington offers high gain—a minimum of 5-mA photocurrent at a forward current of 30 mA. Both versions are TTL compatible.

CHECK NO. 333

200-W TWT covers 12-to-18-GHz range



Sperry Electronic Tube Div., Dept. 9002, Waldo Rd., Gainesville, Fla. 32601. (904) 372-0411. 60 days (small qty.).

The STU-54313 traveling-wave tube delivers 200 W cw over the frequency range of 12.4 to 18 GHz. Small-signal gain is 38 dB, while gain at rated power is 32 dB. The tube is ppm focused, conduction cooled and it operates with depressed collector. Maximum length is 18-3/4 inches and weight is 8 lb.

CHECK NO. 334

Transistor amplifier operates at 6 GHz

Avantek, 2981 Copper Rd., Santa Clara, Calif. 95051. (408) 739-6170. $4700 (small qty.); 45-60 days.

With microwave transistors and thin-film circuitry on sapphire substrates, the AMT-6005M amplifier achieves a maximum gain variation of ±1.5 dB, minimum gain of 28 dB and maximum noise figure of 10 dB, all over the 4-to-6 GHz frequency range. Maximum input and output VSWR is 2:1. Output power (1-dB gain compression) is a minimum of 10 dBm, and typical intercept point is 20 dBm. The new amplifier operates on 15 V dc and 150 mA, typical.

CHECK NO. 335

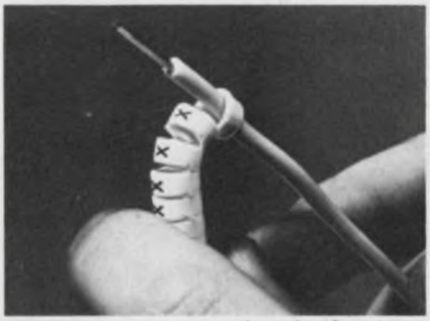
Double-balanced mixer improves tone specs

Watkins-Johnson, 3333 Hillview Ave., Stanford Industrial Park, Palo Alto, Calif. 94304. (415) 493-4141. $299 (1-4).

The M1K double-balanced mixer—a high-intercept, wideband unit—provides improved two-tone characteristics over the frequency range from dc to 4 GHz. With only +23 dBm LO drive level, the mixer has a +28 dBm (typical) input third-order intercept point. With two input tones at 0 dBm, the third-order products are typically 56 dB below the output. The M1K also has a low noise figure of typically 6 dB. And +10 dBm of output power can be obtained.

CHECK NO. 336

Sleeve markers slip onto and grip wires



Electrovert, 86 Hartford Ave., Mount Vernon, N. Y. 10553. (914) MO 4-6090.

Electrovert Z-type markers slip over the wire insulation to provide a nonslip grip on wire or cable. Twelve sizes fit most wire diameters, from 0.045 to 0.460 in. Markings come in individual letters, numerals and symbols. Combinations with up to five markings on one sleeve are also available. A white sleeve with hot-stamped black markings is standard. They are packaged in coils of 50 or 500 snap-off markers.

CHECK NO. 337

Solderless terminals withstand 260 C

Thomas & Betts, 36 Butler St., Elizabeth, N. J. 07307. (201) 354-4321.

Series RTW terminations can take temperatures to 260 C. These solderless ring terminals are insulated with nonburning, nonmelting Kapton. They have a high resistance to solvents, radiation and abrasion. Annular, buttress serrations inside the lead barrel improve electrical contact and increase tensile strength. An insulated sleeve grips the conductor insulation and helps relieve wire strain. Seven sizes handle wires from AWG 26 through 14. And for each wire size there are up to five ring sizes.

CHECK NO. 338

application notes

Transformers

"A u t o-Transformers vs Two-Winding Transformers," a four-page reprint, discusses the pros and cons of utilizing the two types of transformers in low-voltage power distribution systems. Diagrams illustrate cost, weight, efficiency, reliability, safety and maintenance and operation. General Electric, Scotia, N.Y.

CHECK NO. 339

Oscillators

Low-power crystal-controlled oscillator designs for applications with supply voltages of 3 to 15 V dc are described in a bulletin. The bulletin contains a circuit description, schematics, component values, operating parameters, theory and graphs for voltage/current/frequency as well as oscillator phase relationships. Statek Corp., Orange, Calif.

CHECK NO. 340

Spectrum analyzers

"Applications of Modern Tracking Wave and Spectrum Analyzers" includes technical data, block diagrams and application of wave and spectrum amplifiers to various requirements. Topics include transfer function analysis, amplitude response testing, mechanical signal analysis, signal enhancement, phase measurements, cross spectral density, random signal analysis and a brief history of the development of wave and spectrum analyzers. Quan-Tech Div., Whippany, N.J.

CHECK NO. 341

CATV performance testing

How to perform the CATV frequency measurements required by the new FCC system performance regulations is described in an application note. Procedures for measuring all vhf and uhf channel frequencies from Channel 2 through Channel 83 are presented. Singer Instrumentation, Los Angeles, Calif.

CHECK NO. 342

design aids

Symbols handbook

A 22-page, pocket-size handbook illustrates more than 500 symbols commonly used in electronics. Symbols are grouped in 19 general classifications, each listed alphabetically by page reference number in a table of contents. Included is a two-page electronics data guide covering conversion factors and constants, Ohm's Law formulas, resonant frequency, impedance and decibel table and color table. Cleveland Institute of Electronics.

CHECK NO. 343

Electronic reference

A wall chart displays useful optical and electronic terms, definitions, equations and data. Optical Electronics.

CHECK NO. 344

Hi-temp materials

Bulletin 523 describes 33 high-temperature materials. The two-page bulletin lists all of the company's special materials such as machinable ceramics, hi-temp adhesives, coatings, encapsulants and hi-temp tape. The second page of the bulletin folds out into a wall chart in which all the materials are listed including specific data on temperature limits, uses, application procedures and prices on research quantities. Aremco Products, Inc.

CHECK NO. 345

Foldable template

A foldable template in the shape of a projected light beam or cone has been devised for use in designing optical systems in which the light beam is redirected by mirrors. The tool is based on the principle that the true axial length of the light cone is constant, regardless of its geometrical configuration. The light cone can be viewed as folded when it strikes an angled mirror. The triangular template provides a fast visual method of determining mirror and lens sizes and their respective placements. Sandia Laboratories.

CHECK NO. 346

new literature

Integrated packaging

Specifications and dimensions of integrated circuit handling devices, packaging systems, socket, logic and memory panels are given in a 72-page illustrated catalog. Cambridge Thermionic, Cambridge, Mass.

CHECK NO. 347

Instrument publications

An ISA catalog describes 200 instrumentation publications and educational aids. The focus is on state of the art, advances and applications of instrumentation including measurement and automatic control. The catalog contains descriptions, prices and ordering information for proceedings of ISA-sponsored or co-sponsored conferences and symposia, standards and recommended practices, compendia, reference books, periodicals, study guides, motion pictures and tape cassettes. Instrument Society of America, Pittsburgh, Pa.

CHECK NO. 348

Fiberglass polycarbonates

Information on fiberglass-reinforced polycarbonate thermoplastics is given in a four-page brochure. Described are 17 grades including materials with long, intermediate and short fiberglass reinforcement. Fiberfil Div., Dart Industries, Evansville, Ind.

CHECK NO. 349

Interactive graphics system

A four-page brochure describes an interactive graphics system for NC tape preparation and verification. The brochure gives system features, and presents a block diagram of equipment operation, photographs of sample CRT displays and a flow-chart comparison. Systems, Science and Software, La Jolla, Calif.

CHECK NO. 350

Ruby/glass laser systems

Solid-state lasers are described in a six-page brochure. The brochure discusses critical parameters of high-powered ruby and glass laser systems. The problem of how to specify a laser system for a given application is detailed. Apollo Lasers, Los Angeles, Calif.

CHECK NO. 351

Data communications

A synchronous communications controller, synchronous line adaptor, programmed asynchronous multiplexer, asychronous single-line controller, multiprocessor communications adaptor and an IBM 360 interface are described in a 32-page data-communications catalog. Data General, Southboro, Mass.

CHECK NO. 352

Consumer ICs

"Quick Guide to Consumer Entertainment Integrated Circuits" gives a comprehensive roundup of the company's noncustom circuits for use in television, radio and audio applications. Sprague, N. Adams, Mass.

CHECK NO. 353

Disc storage

The series-4500 double-density dual-disc storage systems for minicomputers are described in a four-page brochure. Details on both single and double-platter cartridge disc systems which are said to provide 38-millisecond average access time to five-million words of stored data are provided. System Industries, Sunnyvale, Calif.

CHECK NO. 354

Low-pressure transducers

Low-pressure quartz transducers are described in two bulletins. Photos and dimensional drawings show the small size of these instruments that measure 1.055 in. × 0.433 in. over-all. A specifications table contains capacity and performance data. Kristal Instrument Corp., Grand Island, N.Y.

CHECK NO. 355

Acoustics products

A selection of acoustics products including five sound-level meters is described in a condensed catalog. Pulsar Instruments, Redwood City, Calif.

CHECK NO. 356

Switch assemblies

Three magnetic alarm switch assemblies are described in a bulletin. Specifications, dimensional and installation drawings are provided. North American Philips Controls, Cheshire, Conn.

CHECK NO. 357

Terminal blocks

Dimensions and specifications on terminal blocks, fuse holders, terminals and panel-wiring accessories are given in an eight-page catalog. Maracomm, Wausau, Wis.

CHECK NO. 358

Environmental seals

Clean Fighter environmental seals are detailed in a condensed catalog. The catalog includes Hexseals, one-piece seals which fit all standard toggle, pushbutton and rotary shaft switches; Snapseals, neoprene boots for general commercial applications; and Silikromes, colored filters that mount on clear miniature and automotive lamps and transmit any color required. APM-Hexseal, Englewood, N.J.

CHECK NO. 359

Molded rectifier diodes

Molded rectifier diodes rated for maximum average output of 1, 1.5 and 2 A are described in a data sheet. Complete ratings and specifications, five rating graphs, a dimensioned outline drawing and a photograph of the device are included. International Rectifier Corp., El Segundo, Calif.

CHECK NO. 360

Computer handbooks

A four-book literature series consists of the company's computer-family and communications brochures with their respective design handbooks. The handbooks include chapters on software and hardware products. Modular Computer Systems, Fort Lauderdale, Fla.

CHECK NO. 361

Connectors

Dielectric retention, rear-release, crimp contacts incorporated in a series of electrical connectors are described in a 16-page catalog. The connector series meets the requirements of MIL-C-0026482F and MIL-C-83723. The Bendix Corp., Sidney, N.Y.

CHECK NO. 362

Input formats

"Ways to go with Promemco" is a manual of input formats for pROM programming. Truth-table information is included. Promemco, Inc., Port Washington, N.Y.

CHECK NO. 363

Tech article abstracts

Abstracts of technical articles that have appeared in U.S. electronic engineering publications from October, 1972, to December, 1972, are available in a quarterly publication, Précis. Articles are broken down in the following categories: automatic controls and systems, circuits and components, circuit theory, communications, computers, computer peripherals, design methodology, instrumentation and measurement, manufacturing, microwave, packaging and reliability and maintenance. TIDS, Ridgewood, N.J.

CHECK NO. 364

Beryllia ceramics

Bulletin 724 describes AlSiMag beryllia ceramics. A chart shows the comparison between alumina and beryllia. American Lava Corp., Chattanooga, Tenn.

CHECK NO. 365

Patching, switching systems

A 60-page catalog describes the company's patching devices and switching systems used in such applications as computers, CATV, communications, missile and space, telemetry, nuclear and industrial instrumentation, automatic testing information retrieval and microwave data transmission. Included are an eight-page introductory discussion, "Electronic Systems Wiring & Cable (Problem Areas and Solutions);" a 33-page section covering patch panels, jacks, plugs, networks, connectors and cable; and an 18-page section covering switching matrices and systems. A range of applications are covered from video to 60 MHz, i-f and vhf to 3 GHz. Trompeter Electronics, Chatsworth, Calif.

CHECK NO. 366

Thermal cutoffs

A family of thermal cutoffs for backup protection in electrical and electronic devices is described in a 12-page, illustrated brochure. The booklet describes the capabilities and performance of thermal cutoffs and lists their applications. Photos, schematic drawings, charts and tables are included. 3M, St. Paul. Minn.

CHECK NO. 367

Modular connectors

"PDQ, The New Modular Connector," a four-page brochure, highlights concept and advantages, dimensions, and specifications of connectors. Stanford Applied Engineering, Santa Clara, Calif.

CHECK NO. 368

Battery handbook

"The Gould Battery Handbook" contains engineering data for most types of primary and secondary batteries including comparison of systems and application data. The handbook is over 350 pages, hardbound in two colors and costs $14.-95. Handbook Dept., Gould Inc., P.O. Box 3140, St. Paul, Minn. 55165.

NO/NO_x analyzer

A source-monitoring analyzer employing chemiluminescent technology for the detection of NO/NO_x is featured in a publication. Complete specifications, photographs, charts and outline drawings are provided. Beckman Instruments, Fullerton, Calif.

CHECK NO. 369

Power supplies

A 110-page catalog describes dc modular power supplies, standard dc lab/systems, high-voltage power supplies and an ac voltage-regulator line. Dimensional drawings and domestic list prices are included for the regulators and power supplies. Sorensen Co., Manchester, N.H.

CHECK NO. 370

Tension motors

A data sheet describes the M-100 tension motor. The instrument has been developed to comply with ANSI procedures in measuring cassette-tape winding torque and tension. Information Terminals, Sunnyvale, Calif.

CHECK NO. 371

Microwave pencil tubes

A catalog that describes microwave pencil tubes highlights the small size, lightweight features that have made pencil tubes widely accepted in military, general aviation and other commercial airborne applications. Several new pencil tubes, including integral-cavity amplifiers and oscillators for airborne pulsed service in distance measuring equipment, transponder and interrogator applications, are shown. RCA Commercial Engineering, Harrison, N.J.

CHECK NO. 372

OSHA regulations

A simple and direct outline of the new Federal Occupational Safety and Health Act (OSHA) regulations is now available in the 1973-74 edition of Best's Safety Directory. The 950-page directory includes a digest of applicable OSHA standards and definitions for nearly 4000 products in 80 major categories. Cost of this hard-bound volume is $20 per copy. A. M. Best Co., Safety Div., Park Ave., Morristown, N.J.

bulletin board

Motorola Inc., Semiconductor Products Div., has introduced four more **MECL-10,000 logic blocks.** All parts are specified for operation over the temperature range of −30 C to +85 C. Operation is from a −5.2 V dc power supply. Each device is available off-the-shelf in a 16-pin, black-ceramic, dual-inline package.

CHECK NO. 373

Twenty-one low-power Schottky **TTL ICs** have been introduced by **Texas Instruments.** They are available in plastic and ceramic dual-inline packages.

CHECK NO. 374

Inselek Co. has announced an expansion of its CMOS on sapphire product line to include three new **computer logic circuits.**

CHECK NO. 375

A software package that simplifies the development of applications programs which use the Indexed Sequential Access Method (ISAM) has been announced by **ADL Systems, Inc.** The package, called IP/ISAM, acts as an interface between ISAM system software and the applications programs of the user. Its major function is to add a significant capability for automatic file management and simultaneous file accessing.

CHECK NO. 376

Digital Equipment Corp.'s Laboratory Data Products Group has announced development of a **low-cost, multispeed FORTRAN IV programming system** for scientific calculations. Called OS/8 FORTRAN IV, the ANSI-compatible system is designed for any current PDP-8 minicomputer with a minimum 8-k of core and mass storage. System prices start below $13,000.

CHECK NO. 377

Aerojet Industrial Systems has announced that its line of **electronic controls** for materials handling systems is being marketed independent of its handling equipment.

CHECK NO. 378

Nine more **standard MECL 10,000 logic functions** in addition to the 10 previously announced MECL 10,000 devices are now available from **Motorola Semiconductor Products Div.** These devices are available off-the-shelf and are in hermetic, 16-pin, black-ceramic dual-inline packages (one model comes in a 24-pin ceramic package). They operate over −55 to +125.

CHECK NO. 379

The **digital television picture-processing and enhancement systems** by **Spatial Data Systems** provide a building-block approach to picture analysis. The systems begin with stand-alone, special-purpose instruments and expand to full digital processing and display. The independent systems interface to existing installations.

CHECK NO. 380

Price reductions

Price reductions up to 40% have been announced by the **Dialight Corp.** on its **521 series of LED solid-state lamps.** The 521 series includes LED lamps in four color varieties—red, white, red diffused and clear diffused. All are designed for mounting onto a PC board, a high density package or a front panel via a snap-in technique.

CHECK NO. 381

ACDC Electronics has announced a price reduction on 34 models of its **OEM series power supplies.** Seventeen case-4 models ranging from 5 V at 25 A to 32 V at 5.7 A have been reduced 10% to $149 (10-24). Seventeen case-5 models ranging from 5 V at 35 A to 32 V at 8.1 A have been reduced 5% to $184 (10-24).

CHECK NO. 382

The Electro-Metrics Div. of Fairchild Camera & Instrument Corp. has announced price reductions for its **X-Y plotters.** The EXY-125B (single pen) plotter has been reduced to $1550 from $2350 while the EXY-250 (dual pen) has been reduced to $3950 from $4950.

CHECK NO. 383

Avantek has reduced prices of its **GPD thin-film amplifying devices** by approximately 40%.

CHECK NO. 384

Design Data from Manufacturers

Advertisements of booklets, brochures, catalogs and data sheets. To order use Reader-Service Card
(Advertisement)

New High-Speed FFT Processor Easy to Operate

Conceived from the point of view of the operating engineer rather than the computer programmer, the new Omniferous™ FFT Analyzer *operates like an instrument*, calculates like a computer. This Series OF-400 Analyzer is a universal digital signal analysis system for real-time viewing of changing functions, a complete instrument with all signal conditioning and display calibration built-in. For the first time an operator can observe transfer function, cross-spectra or coherence as the signal is changing without waiting for the analyzer to perform successive laborious calculations.

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The system excels in high dynamic range, ease of use, display flexibility with two simultaneous display outputs, frequency coverage to 100 kHz, and reasonable cost. Designed by the originators of the famous Ubiquitous® family of real-time spectrum analyzers.

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Low-Noise High-Gain Preamplification

Complete specifications of a variable-bandwidth high-gain preamplifier are contained in the P.A.R. data sheet, T-224. Included are typical noise figure contours illustrating the amplifier's exceptionally low noise, which is as low as .05 dB at mid frequencies with a 1 megohm source. Other illustrations include typical plots of the equivalent input noise and common mode rejection, which exceeds 100 dB at 60 Hz at all gain settings. The data contained in the specification sheet will be of interest to all engineers and researchers looking for a preamplifier with calibrated gain and rolloffs from dc to 300 kHz. CIRCLE NO. 172

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Want to contact us? If you have any comments or wish to submit a manuscript or article outline, address your correspondence to:

Editor
ELECTRONIC DESIGN
50 Essex Street
Rochelle Park, N.J. 07662

Electronic Design

Advertising Sales Staff
Tom W. Carr
Sales Manager

Rochelle Park, N.J. 07662
Robert W. Gascoigne
Daniel J. Rowland
50 Essex Street
(201) 843-0550
TWX: 710-990-5071

Philadelphia
Thomas P. Barth
50 Essex Street
Rochelle Park, N. J. 07662
(201) 843-0550

Boston 02116
50 Essex Street
Rochelle Park, N. J. 07662
(201) 843-0550
(617) 482-7989

Chicago 60611
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200 East Ontario
(312) 337-0588

Cleveland
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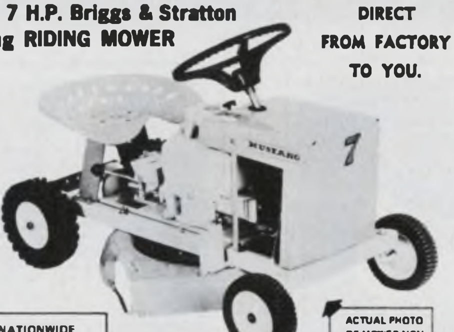

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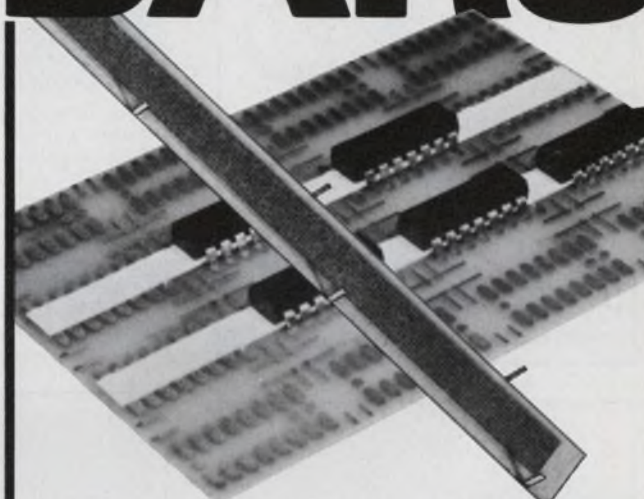
INFORMATION RETRIEVAL NUMBER 902

BUSS BARS



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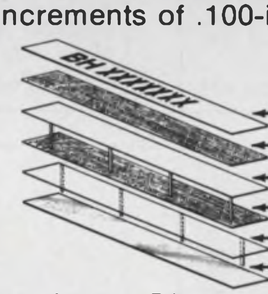
Standard 140 and 160 Series DIP Buss Bars are available for use with 14 and 16-pin DIPs. Conductor tabs share standard board holes with IC's. Custom tab locations can be supplied in spacing increments of .100-inch.



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INFORMATION RETRIEVAL NUMBER 159

quick ads

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INFORMATION RETRIEVAL NUMBER 181

Look what light can do. Unique cadmium sulfide, cadmium selenide light controlled photo potentiometers, photo bridges, photo isolators and selenium cells as well as LED/photo transistor optical switches and a complete line of silicon cells and arrays. Solar Systems, Inc., 8124 N. Central Park, Skokie, Ill. 60076. (312) 676-2040.

INFORMATION RETRIEVAL NUMBER 182

Low cost quartz crystals in TO-5s: For 10 to 250 kHz oscillators, filters, tone generators, timers . . . Rugged—Accurate—High vibration and shock resistance. Prices low as $.95 ea. in 100k qtys. Send your written application. We'll send a sample. Or, write for literature. Statek Corp., 1233 Alvarez Ave., Orange, Calif. 92668. (714) 639-7810.

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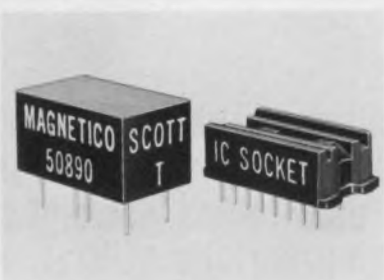

Scott T transformer—dual in line size. In a DIP type size and pin spacing, Scott T No: 50890 converts 400 Hz 11.8V RMS line to line synchro information to 6V RMS Sine and Cosine resolver outputs. Accuracy is 2 arc minutes. Cost is $25.00 in qty. For any Scott T call: Magnetico, Inc., East Northport, N.Y. 11731. Tel: (516) 261-4502.

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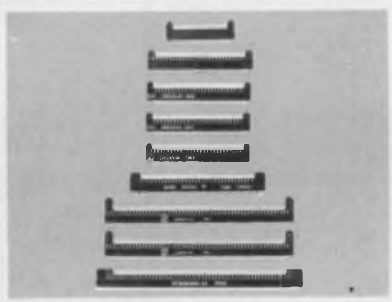

New headers—Here's our new top line of nine right angle molded printed circuit headers for use with 0.100" center wire wrapped plates. One 34-pin model, four 56-pins, one 70-pin and three 112-pins. Your National Connector salesman has all the details. NATIONAL CONNECTOR, 5901 So. County Rd. 18, Mpls., Mn. 55436. (612) 935-0133.

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Coax matrix switch for high frequency test equipment applications, now available in a modular and expandable 19" rack mounted unit. Computer compatible, the switches latch and unlatch with 250 ns TTL pulses. Signals up to 15 MHz with low distortion and crosstalk. ADDS, 830 Linden Av., Rochester, N. Y. 14625. 716/381-2370.

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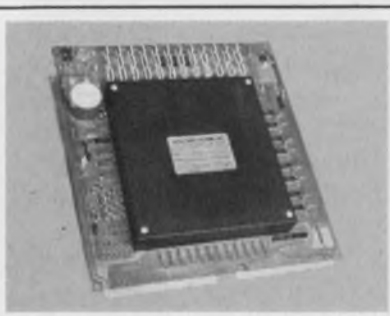

Aztec Data Systems has developed the only single board electrically alterable read-only memory in configurations of either 1K X 16 or 4K X 16 bits on a 15" X 15" PC board. Priced in quantity as low as 5¢ per bit. AZTEC DATA SYSTEMS, INC., 17805 Sky Park Circle, Irvine, Ca. 92707. 714-540-8445.

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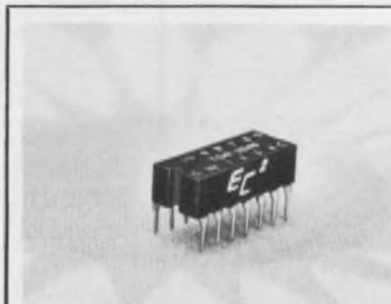

EC²'s "DIP Series" Lumped-Constant Delay Lines are packaged in a low silhouette epoxy encapsulated, 14-pin dual in-line configuration. EC² offers over 200 variations of DIPs, featuring either fixed or tapped delays, from 4 to 150 nanoseconds. Engineered Components Co., 2134 W. Rosecrans Ave., Gardena, Calif. 90249. (213) 321-6565.

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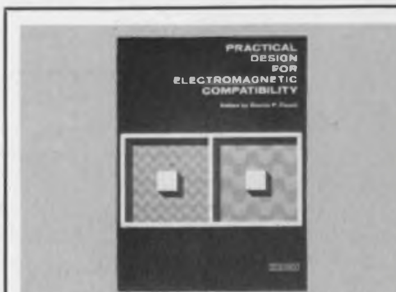


Practical Design for Electromagnetic Compatability, edited by Rocco Ficchi. An -on-the-job manual giving designers practical techniques for analyzing, predicting, controlling, and reducing unwanted signals. 272 pp., 7-1/8 x 9-3/4, illus., cloth, $13.95. Circle number for 15-day examination copy. Hayden Book Company, Rochelle Park, N.J. 07662.

INFORMATION RETRIEVAL NUMBER 191

product index

Information Retrieval Service. New Products, Evaluation Samples (ES), Design Aids (DA), Application Notes (AN), and New Literature (NL) in this issue are listed here with page and Information Retrieval numbers. Reader requests will be promptly processed by computer and mailed to the manufacturer within three days.

new literature

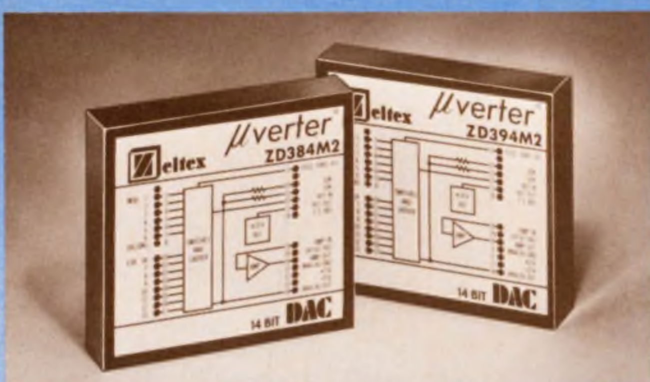
application notes

design aids

NEW!

from ZELTEX...

14-Bit DAC's from $85



LOW COST 14-BIT DAC's—The new ZD300 Series include ten new models that offer excellent linearity, fast settling, current and voltage outputs, bipolar and unipolar coding, slaveable reference, and two quadrant multiplication. Prices range from $85 to $179 in single quantities.

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UNIPOLAR, BIPOLAR OUTPUTS—Unipolar and bipolar operation is specified at 0 to 10V, and ±10V, respectively. Current output models are rated at 0-2 mA. Voltage output models also feature current output capability as well as two-quadrant multiplication-up to 100 kHz.

LINEARITY 0.005%—High performance units feature linearity error of only 0.005% of full scale. Moreover, the extremely low linearity temperature coefficient of only 0.0005%/°C ensures high resolution accuracy.

SMALLEST 14-BIT DAC's—The ZD300 Series modular DAC's measure only 1.96 x 1.76 x 0.40 inches high—less than 1.4 cubic inches in volume. Low profile, DIP pinning compatibility and interchangeability of models make the series highly desirable for OEM usage.

APPLICATIONS—The versatility of the ZD300 Series makes them an excellent choice for use in process-control systems, automated test equipment, servo/synchro/resolver systems, and biomedical instrumentation.

Multiplying capabilities further enhance their use for CRT character generation, digital modulation, and polar-to-rectangular coordinate conversion.

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INFORMATION RETRIEVAL NUMBER 220

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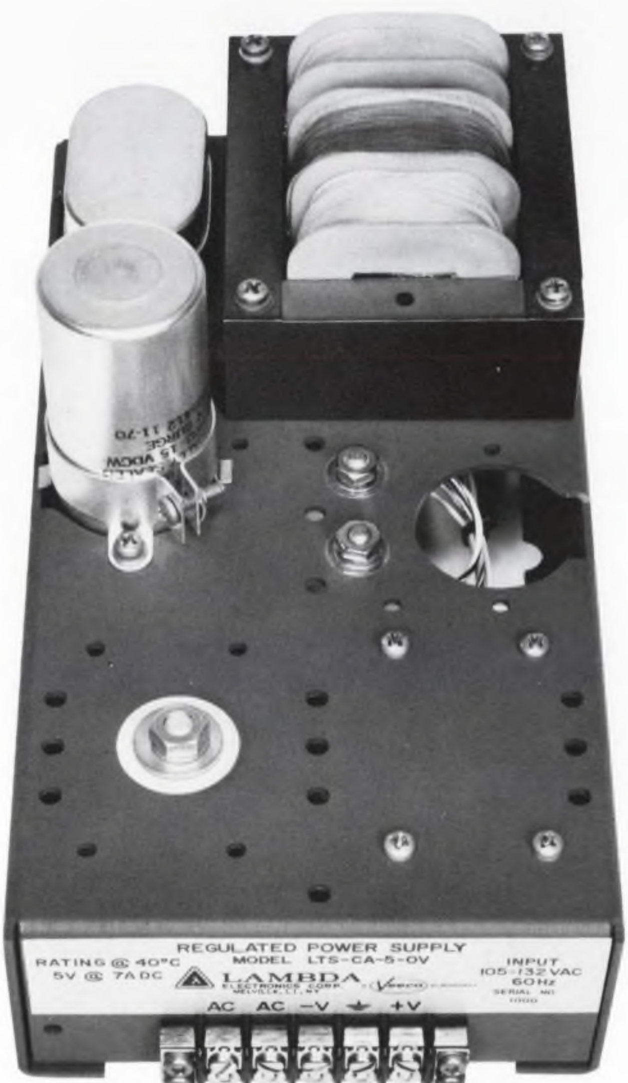

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LTS-CA SINGLE OUTPUT MODELS
$4\frac{29}{32}$" x $4\frac{15}{16}$" x $9\frac{5}{16}$"

MODEL	FIXED VOLT. RANGE VDC	MAX. AMPS AT AMBIENT OF: 40°C	PRICE
LTS-CA5-OV*	5±1%	7.0	$80
LTS-CA-6	6±1%	6.6	80
LTS-CA-12	12±1%	4.4	80
LTS-CA-15	15±1%	4.0	80
LTS-CA-20	20±1%	3.1	80
LTS-CA-24	24±1%	2.6	80
LTS-CA-28	28±1%	2.2	80

*Includes fixed overvoltage protection at 6.8V±10%

LTD-CA DUAL OUTPUT MODEL
$4\frac{29}{32}$" x $4\frac{15}{16}$" x $9\frac{5}{16}$"

MODEL	FIXED VOLT. RANGE VDC	MAX. AMPS AT AMBIENT OF: 40°C	PRICE
LTD-CA-152	±15±1%	2.0	$110
LTD-CA-122	±12±1%	2.0	110

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