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for the Radio-Amateur

Especially Covering VHF,
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VHF communications

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System Measurements using Solar Noise

Two Major Setbacks in the European Space Programme

Two major setbacks in the European Space Programme have had a considerable effect on us VHF/UHF amateurs. The first was the failure of METEOSAT 1, and the second was the unsuccessful launch of the Ariane rocket carrying OSCAR 9 and FIREWHEEL.

continued below Index

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VHF communications

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A Publication for the Radio Amateur
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The failure of METEOSAT was caused by a malfunction in the overvoltage protection circuit. The ESA has tried a number of occassions to bypass this protection circuit but without success. However, two METEOSAT II satellites are now available, and the next launch is planned for either November 1980, or February 1981. We would like to point out that the US geostationary GOES satellite located at 70° W transmits on 1691 MHz, and should be audible for locations west of the 0° meridian.

The loss of OSCAR 9 has a far greater effect on us VHF/UHF amateurs who are impatiently waiting to try this new technology. This must also be a considerable financial blow to the AMSAT organisation who have put in so much research and development into this new satellite, and also so much time and effort. We hope that this will not be too great a setback, and we VHF/UHF amateurs must do all we can to assist them in their future projects.

DJ 0 BQ

Determining the Sensitivity of Receive Systems with the Aid of Solar Noise

by G. Hoch, DL 6 WU

There is a considerable interest amongst radio amateurs in the reception of extra-terrestrial signals. Now that extremely low-noise microwave transistors are available at reasonable prices, a number of possibilities can also be realized by radio amateurs. Examples of this are reception of weather satellites such as METEOSAT, the observation of solar radiation, EME communications, and not to forget the future phase 3 amateur radio satellites (OSCAR 9). The author is to describe a simple method of checking the efficiency of the receive system, and how to optimize it.

1. THE EFFICIENCY OF RECEIVE SYSTEMS

A number of demands of different priorities are placed on a receive system, which is a combination of antenna and receiver. For instance, certain minimum values must be given for the stability and accuracy of frequency and antenna direction, even when this can be partially replaced by patience and experience. However, absolute limits do exist for the sensitivity of the system, that is in its ability to differentiate between signals and noise. A certain minimum value of the signal-to-noise ratio is required for a given mode of transmission.

Whether this minimum signal-to-noise ratio is reached with a given field strength, depends – under ideal conditions – only on two factors: The antenna gain and the receiver noise threshold.

1.1. Antenna Gain

A directional antenna will receive a signal from the selected direction at a higher value than when using a theoretical isotropic radiator; this increase in signal corresponds to its gain factor G_i. The antenna will extract an energy from the field, that is proportional to its aperture F. In the case of horn-antennas and dipole arrays, the aperture will coincide very accurately to the physical dimensions. The gain and aperture can be converted using the following equation:

$$G_i = \frac{4 \pi F}{\lambda^2} \qquad (1a)$$

λ = wavelength

If the energy flux density S of a signal source is known for the receive location, it is possible with the aid of the aperture to determine the energy received by the antenna.

Relatively exact flux values are available for a large number of extraterrestrial sources such as the Sun, Moon, and radio stars.

Unfortunately, an actual antenna will also receive signals from other sources than the required ones; e.g. heat radiation from the ground surface, and the antenna will also have ohmic losses that can also produce noise. In practical work, all these unwanted noise signals are added to the intrinsic noise of the receiver.

1.2. Receiver Noise

This was discussed in detail in (1), and only the most important details are to be repeated here:

1.2.1. Noise factor

The noise factor F is defined as the quotient of the signal-to-noise ratios behind and in front of a four-pole:

$$F = \frac{S_2}{N_2} \div \frac{S_1}{N_1} = \frac{S_2 \times N_1}{S_1 \times N_2} \quad (1b)$$

or as logarithmic noise figure NF:

$$NF = 10 \log \frac{S_2 \times N_1}{S_1 \times N_2} \quad (1c)$$

One often ignores that the given numerical values are only valid for a certain temperature, namely the temperature at which the impedance of the signal source produces noise. This is usually $T_0 = 290$ K. If the signal source is, for instance, an antenna pointing towards a cold portion of space, this will increase the sensitivity of the subsequent receivers more than when measuring the noise factors at a normal ambient temperature. In this case, it is more favorable to compare the additional noise factors F–1, or the noise temperatures which correspond to this.

1.2.2. Noise Temperature

The noise temperature T of a four-pole is dependent on the noise factor (measured at T_0) according to the simple equation:

$$T = (F-1)\, T_0 \quad (1d)$$

(in K)

If the noise components of all portions of a receive system are converted to noise temperature, one will receive the so-called system temperature T_S of the system by simple addition.

1.3. G/T-Ratio

The gain/temperature ratio is used quite commonly in the space communications technology as a measure of the sensitivity of a receive system. This is the quotient from the numerical value of the antenna gain G_i and the system temperature T_S in Kelvin. The value G/T is often given logarithmically:

$$10 \log G/T = 10 \log G_i - 10 \log T_S$$

written as $\frac{dB}{K}$ (1e)

It should be noted that the temperature should also be inserted logarithmically, in other words, also in dB.

The G/T-values of various systems can be compared directly with another. If station A has a G/T of 10 (10 dB/K), and station B one of 5 (7 dB/K), this will mean that station A will receive the same signal twice as strong (+ 3 dB) as station B when using the same bandwidth. It is not necessary to know the noise figure of the receiver or the antenna gain for this.

1.3.1. Determining the G/T-Ratio

A signal of a known magnitude is required for measuring the G/T of a system. This signal must also come from the same direction as is to be used for communications since the received background noise has an effect on the measured value. In the case of systems for the reception of extraterrestrial signals it is not possible to use signal sources on the earth surface. The strongest extraterrestrial source in the VHF, UHF and SHF range is the Sun. Unfortunately, it is also the least accurate, since its radiation fluctuates considerably. However, it is most certainly suitable for amateur measurements if a certain amount of caution is used.

In order to determine G/T, one measures the so-called Y-factor, which is the ratio of the received energy with and without signal source.

$$Y = \frac{S + N}{N} \quad (1f)$$

This is achieved by pointing the antenna alternately to the Sun and to the »cold« part of space. Since the Sun radiates noise energy, the bandwidth is not important

during this measurement. This means that all unwanted noise sources as mentioned in 1.1. are combined in the Y-value measured in this manner. The G/T-value is converted from the Y-value according to the following equation:

$$G/T = \frac{Y-1}{I} \qquad (1g)$$

I is a constant that is given by the wavelength λ, and the flux S of the source used at this wavelength. This can be calculated as follows:

$$I = \frac{A \times S \times \lambda^2}{8\pi K} \qquad (1h)$$

A is a correction factor of approximately 1 (e.g. for absorption losses), which need not be considered during amateur measurements; k is the Boltzmann constant ($k = 1.38 \times 10^{-23}$ Ws x K^{-1}). I has the dimensions of a temperature.

For those interested in the physical relationships, equation (1 g) is obtained as follows:

The gain is given in 1.1. as:

$$G_i = \frac{4\pi F}{\lambda^2}$$

The receiver temperature T_{rx} is measured according to the hot-cold method:

$$T_{rx} = \frac{T_h - Y \times T_c}{Y-1}$$

where T_h is the temperature of the signal source and T_c is the temperature of the cold point in space.

If T_c is assumed to be 0 (cold point in space, residual temperature added to the receiver), the following will be valid:

$$T_{rx} = \frac{T_h}{Y-1}$$

The energy $k \times T_h$ received from the signal source, corresponds to the received radiation energy S x F/2 (this is divided by two since an unpolarized radiation is usually received by the antenna with a certain polarization).

This results in the following

$$\frac{G_i}{T_{rx}} = \frac{4\pi F \times 2k \times (Y-1)}{\lambda^2 \times S \times F} = \frac{Y-1}{I}$$

Table 1: Noise flux of various radio sources (x 10^{-23} Ws/m²) as well as the appropriate values of the constant I

Source	144 MHz [4] Flux	I	432 MHz Flux	I	1296 MHz Flux	I	1700 MHz Flux	I	2800 MHz Flux [5]
Sun 1974	28	3.49 K	220	3.06 K	440	0.68 K	500	0.45 K	700
Sun 1978 [1]	55	6.86 K	300	4.17 K	680	1.05 K	770	0.69 K	1050
Sun 1979 [2]	90	11.2 K	500	6.95 K	1250	1.93 K	1450	1.30 K	1900
Cassiopeia A [3]	15.0	1.87 K	5.55	0.077 K	2.05	0.0032 K			
Cygnus A	10.0	1.25 K	4.00	0.056 K	1.40	0.0022 K			
Taurus A	1.80	0.22 K	1.25	0.017 K	0.29	0.00045 K			

[1]) Autumn 1978
[2]) Autumn 1979
[3]) Values for 1978, decreases by approx. 1 % per year
[4]) Extrapolated values
[5]) These values are identical to the solar flux values. However, the unit is 10^{-22} Ws/m², which means that the numerical value is ten times less. A rough check of the measurements is possible by comparing to the actual flux values.

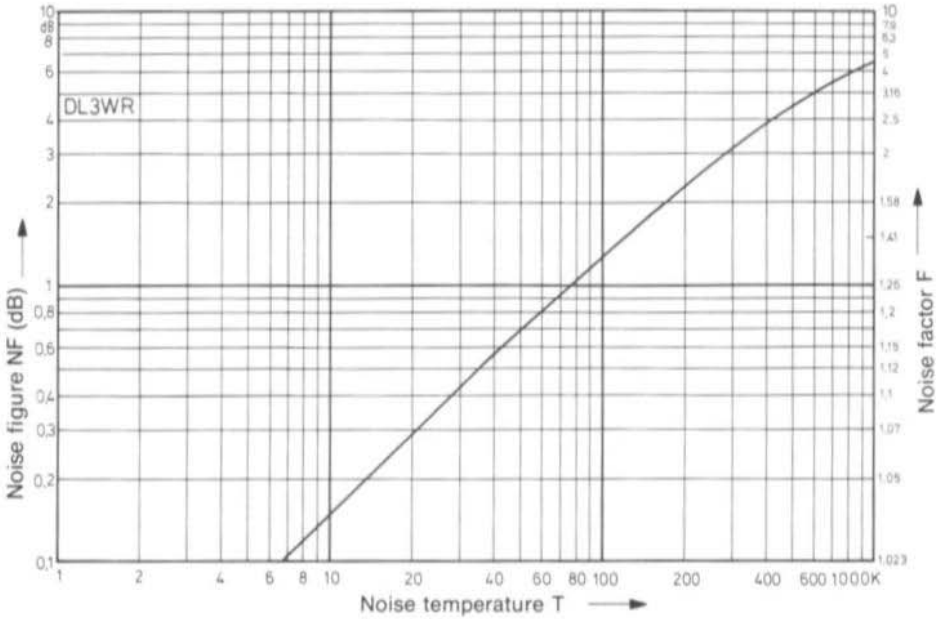

Fig. 1: Diagram for conversion of noise figure / noise factor into noise temperature

If the antenna gain is known, the system temperature can be obtained from the G/T-value. It will be always higher than the noise figure of the input transistor according to the temperature given in Figure 1. If this value is considerably higher, it is necessary for the causes of this to be found. A few typical faults are as follows:

Cable losses between antenna and preamplifier. These losses do not only reduce the effective gain of the antenna, but also produce noise themselves. Noise-matched inputs usually also cause additional losses due to the mismatch characteristics.

Too little preamplification.
The losses of the feeder to the receiver and its noise have an effect on the overall noise figure of the system [see (1)].

Poor unwanted lobe suppression of the antenna.
Other unwanted sources will also be received, for instance radiation from the warm surface of the earth, e.g. when radiating past the edge of a parabolic dish.

2. PRACTICAL MEASUREMENTS

The main prerequisite for the given measurements is to know the noise flux of the signal source to be used. The information given in **Table 1** is based on publications of the NOAA in Boulder, CO/USA (3).

2.1. Solar Noise

Figure 2 gives the flux of the Sun as measured during the periods of minimum sun spots (a) and at maximum activity (b and c).

It is especially at the time of maximum sun spot activity that temporary fluctuations of activity and noise eruptions occur quite often. These can be frequency-selective, and the noise can increase to a hundred or even a thousand times that of the quiet-sun values in the case of lower frequencies (HF to VHF).

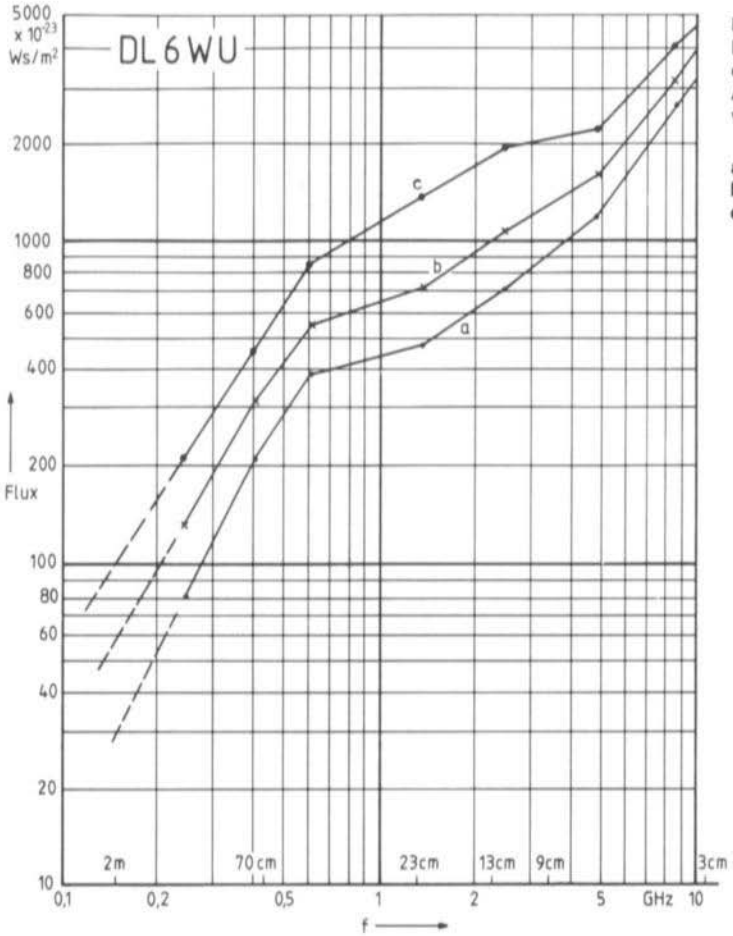

Fig. 2:
Radiation of the Sun: Average flux values on quiet days

a) Sun spot minimum (1974)
b) Transition phase (1978)
c) Sun spot maximum (1979)

If the measurements are repeated over a period of several days, and only the minimum values are used, this will ensure that the greatest errors are avoided.

2.2. Other Radiation Sources

There are a number of other signal sources that generate a flux that is comparable to that of the Sun. A large number of these are to be found in the area of the Milky Way. However, at higher frequencies solar energy will be far higher, as can be seen in the table.

It is especially at 144 MHz where other extraterrestrial sources can cause great errors during the measurements when they are received accidentally at the same time.

2.3. Effect of the Elevation Angle

It is important during determination of the system temperature to know which noise component is contributed by the background during this measurement.

It will only be the space-temperature that is of importance at high elevation angles, as long as a sufficiently good front-to-back ratio is exhibited. Maps are available for the temperature of space (4). It will be seen on studying these and the values given in Table 1 that measurements can only be

influenced noticeably at frequencies below 1 GHz. It should be remembered that the space-temperature is formed from the components of several individual sources. Whereas at 432 MHz the »cold« portions of space in the vicinity of the galactical poles only amount to approximately 15 K, their temperature at 144 MHz would be increased to approximately 180 K. When the antenna is pointed to the center of the Milky Way, the temperature can increase to approximately twenty times these values when using high-gain antennas.

Although it is possible to calculate and determine space-noise, even if with difficulty, any measurements will be very questionable at low elevation angles. In this case, the antenna will also receive heat-radiation from the earth surface, whose magnitude is, however, very dependent on the reflection capabilities of the surface (mirror effect), and will be far greater in the case of built-up areas than in the case of calm sea. The signal can increase by up to 6 dB when the reflected signal is also received by the antenna lobe. The atmosphere also attenuates the signal according to frequency to a differing degree, and also produces noise.

2.4. Measuring Method

Whereas the interpretation of the measured values must be made with considerable caution as already described, the actual measurement can be carried out relatively simply. The measurement is made by determining the ratio of the output (noise) energy with the antenna pointed towards the Sun (or another source) and when pointed to a cold point in space.

The easiest way to do this is when measuring the noise-increase with the aid of a calibrated attenuator in the signal path (for example between converter and receiver). Of course, this must be made at a position where sufficient linearity is available. – Thus not subsequent to an AM-detector (5). The selected attenuator value corresponding to the difference in noise level then represents the Y-value.

If a calibrated S-meter is available, it is possible for the increase in noise to be read off directly. If sufficient linearity is provided (check this with a noise generator !), it is also possible to measure the Y-factor in the SSB-mode by switching off the AGC-circuit and connecting a AF-voltmeter to the output.

2.5. Example

The 70 cm antenna of the author exhibits a gain of approximately 24 dB over an isotropic radiator (6 homemade Yagis of 4 m in length). This is followed by a feeder having approximately 1.5 dB loss, and a preamplifier equipped with a BFT 66 transistor (NF ≈ 2 dB). A noise increase of 5 dB was measured when the antenna was pointed towards the Sun.

When the same preamplifier was connected directly to the antenna, this noise value was increased to 7 dB, and when using a preamplifier equipped with a NE 645 transistor (NF ≈ 1 dB), the noise increase was 9 dB.

The calculation is as follows for the last case:

$$10 \log Y = 9$$

$$Y = 7.94$$

$$I\ (70\ cm;\ sun) = 4.17$$

$$G/T = \frac{Y - 1}{I} = \frac{6.94}{4.17} = 1.66/K\ (2.2\ dB/K)$$

$$G_i = 24\ dB \triangleq 250\ times$$

$$T_S = \frac{250}{1.66} \approx 150\ K$$

Of this, approximately 70 K are from the transistor, approximately 30 K are from the subsequent feeder to the receiver and from the receiver itself. The rest are losses in the feeders to the individual antennas (approx. 0.35 dB ≙ 25 K), the transformation link, as well as the noise components from other sources received by the antenna. It is possible when using this antenna system to hear CW-echos from the stronger EME-stations.

3. FINAL CONSIDERATIONS

The G/T-value provides a useful measure of quality for a receive system, and it can be

determined relatively easily. It represents a clear indication whether any measures bring an improvement or deterioration of the overall system. The bandwidth has no effect on the determination of the G/T-value, as long as no image-noise is measured.

No attempt is made here to discuss the effect of bandwidth on sensitivity, since this is dependent on the transmission mode, and when using the human ear as detector, is even subjective. In principle, the bandwidth can be limited at virtually any position of the signal path.

It is once again to be underlined that the calculation is only valid when using a cold point in space as background. In the case of terrestrial communications, it can be assumed that the signal source will virtually always produce noise at the ambient temperature, and it is therefore not very advisable to attempt to obtain extreme receive sensitivity. In this case, the only way to obtain more signal is usually to increase the size of the antenna !

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A System for Reception and Display of METEOSAT Images

Part 4

by R. Tellert, DC 3 NT

Due to the great deal of interest shown in the FAX-recorder, this unit is to be described after completing the description of the electronic processor. Unfortunately, no construcional data will be available in advance.

The following article is to describe the first two PC-board modules of the image processing modules: Module DC 3 NT 006 comprises the power supply and the output stages for the FAX-motor, and module DC 3 NT 008 provides all the various frequencies required. Further details are given in the block diagram given in Figure 26 of Part 3.

5.2. Module DC 3 NT 006

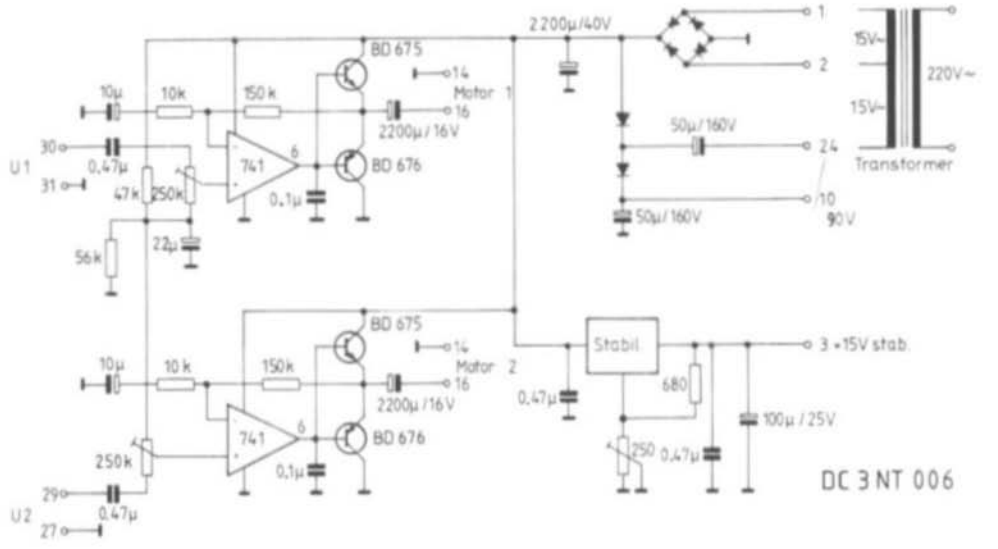
As was mentioned previously, this module contains the power supply and the two output stages for the FAX-motor. **Figure 27** gives the circuit diagram, and the numbers given at the connection points are the pin numbers of a 31-pin connector.

The power supply requires a transformer, which is not accommodated on the board that is able to provide 2 x 15 V at 30 VA. The voltage from one winding is fed to a bridge rectifier to provide a non-stabilized DC-voltage of approximately 19 V which is used for supplying the power amplifier of the FAX-motor. This DC-voltage is also stabilized to 15 V. A fixed voltage stabilizer for 12 V (7812) can be used; the output voltage can be varied between approximately 12 V and 17 V with the aid of the 250 Ω potentiometer. Since this voltage is used as reference voltage for a number of stages, it is advisable for it to be variable. If the voltage stabilizer became defective and had to be exchanged, it would be easily possible to adjust the voltage to the previous value after exchanging this component.

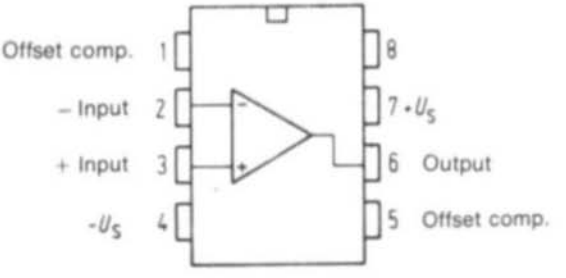
The stylus voltage of the FAX-machine is generated with the aid of both transformer windings and voltage doubling. The output electrolytic of 50 µF will charge itself up to the peak voltage of approximately 80-90 V. Since the stylus current is low, it is not necessary for this voltage to be filtered or stabilized.

The amplifiers for the two phases of the drum motor of the FAX-machine only require an upper cut-off frequency of 100 Hz. They are identical and comprise an operational amplifier with subsequent complementary power amplifier. The transistor types used (BD 675/676) are 40-W-Darlington transistors that are protected against induction voltages from inductive loads with the aid of a built-in protective diode.

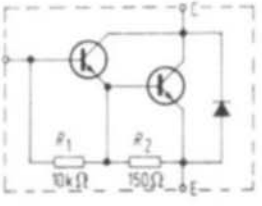
The two output electrolytics of 22 mF should be measured to have approximately the same capacitance values in order to avoid phase-shifts at the lowest frequencies. This can be done by connecting the



TBA 221 B / 741 CN



BD 675 / BD 676



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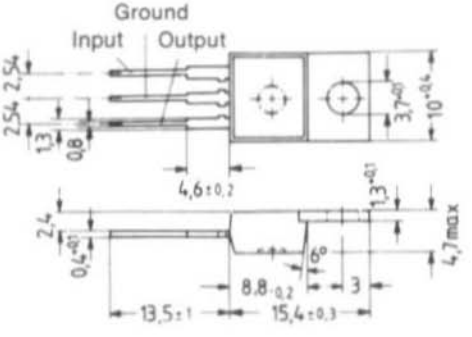


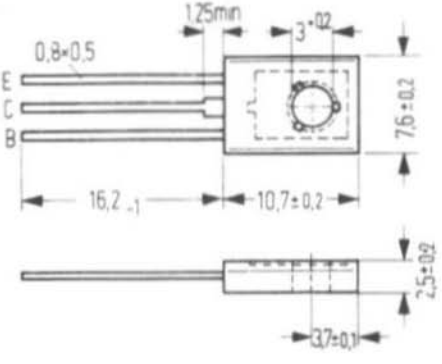


Fig. 27: Circuit of the power supply and output stage of the FAX-motor

electrolytics via a high-impedance resistor to a constant voltage. The voltage is then measured on a high-impedance volt-meter, and the time taken from zero V to a certain value is measured.

The voltage gain is variable between 0 and 15 times; this allows any differences in the drive-amplitudes to be compensated for.

5.2.1. Construction of Module DC 3 NT 006

The PC-board for this module is in the so-called European card size of 160 mm x 100 mm as are all modules of the image processor, and is provided with a 31-pin connector. **Figure 28** shows this single-coated PC-board DC 3 NT 006 together with the component location plan. The four output transistors and the voltage stabilizer should be mounted between PC-board and heat sinks; the photograph given in **Figure 29** shows the author's prototype after removing the heat sinks. The components for this module are given in the following component list and the heat sinks should be drilled and bent as shown in **Figure 30.**

Components of DC 3 NT 006

1 transformer 2 x 15 V, 30 VA
6 rectifier diodes 1 N 4004 or 1 N 4007 or similar
2 BD 675 or BD 677 (Siemens)
2 BD 676 (Siemens)
2 741 or TBA 221 B (Siemens)
1 12 V stabilizer 7812 or similar
2 electrolytics 50 µF / 160 V
1 electrolytic 2.2 mF / 40 V
2 electrolytics 2.2 mF / 25 V
1 electrolytic 100 µF / 25 V
1 electrolytic 22 µF / 25 V
2 electrolytics 10 µF / 25 V (tantalum drops)
4 plastic-foil capacitors, 0.47 µF / 63 V (7.5 mm)
2 plastic-foil capacitors, 0.1 µF / 100 V (7.5 mm)
3 trimmer potentiometers, horizontal mounting, spacing 10/5 mm, with the following values: 2 x 250 kΩ, 1 x 250 Ω
All resistors: carbon layer

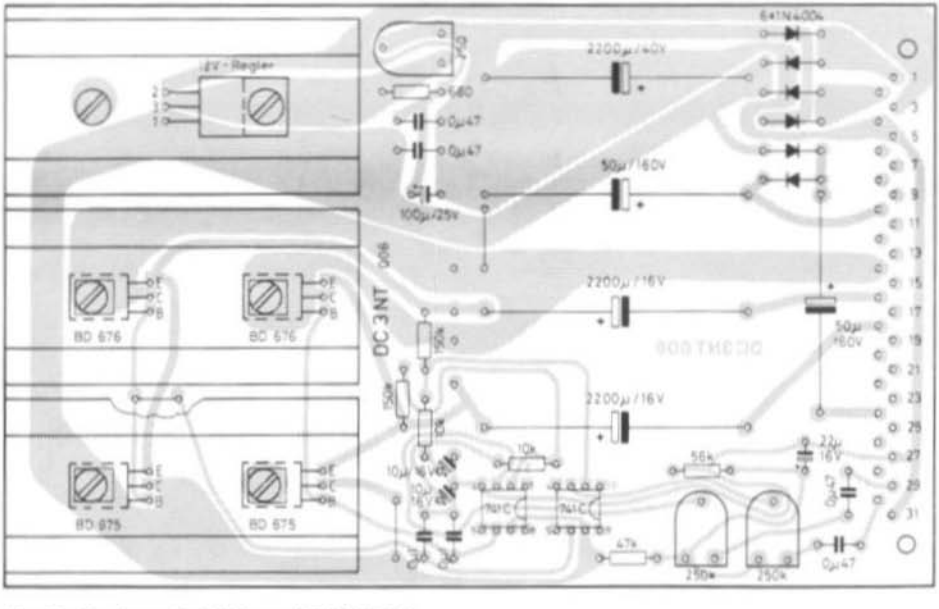


Fig. 28: Single-coated PC-board DC 3 NT 006

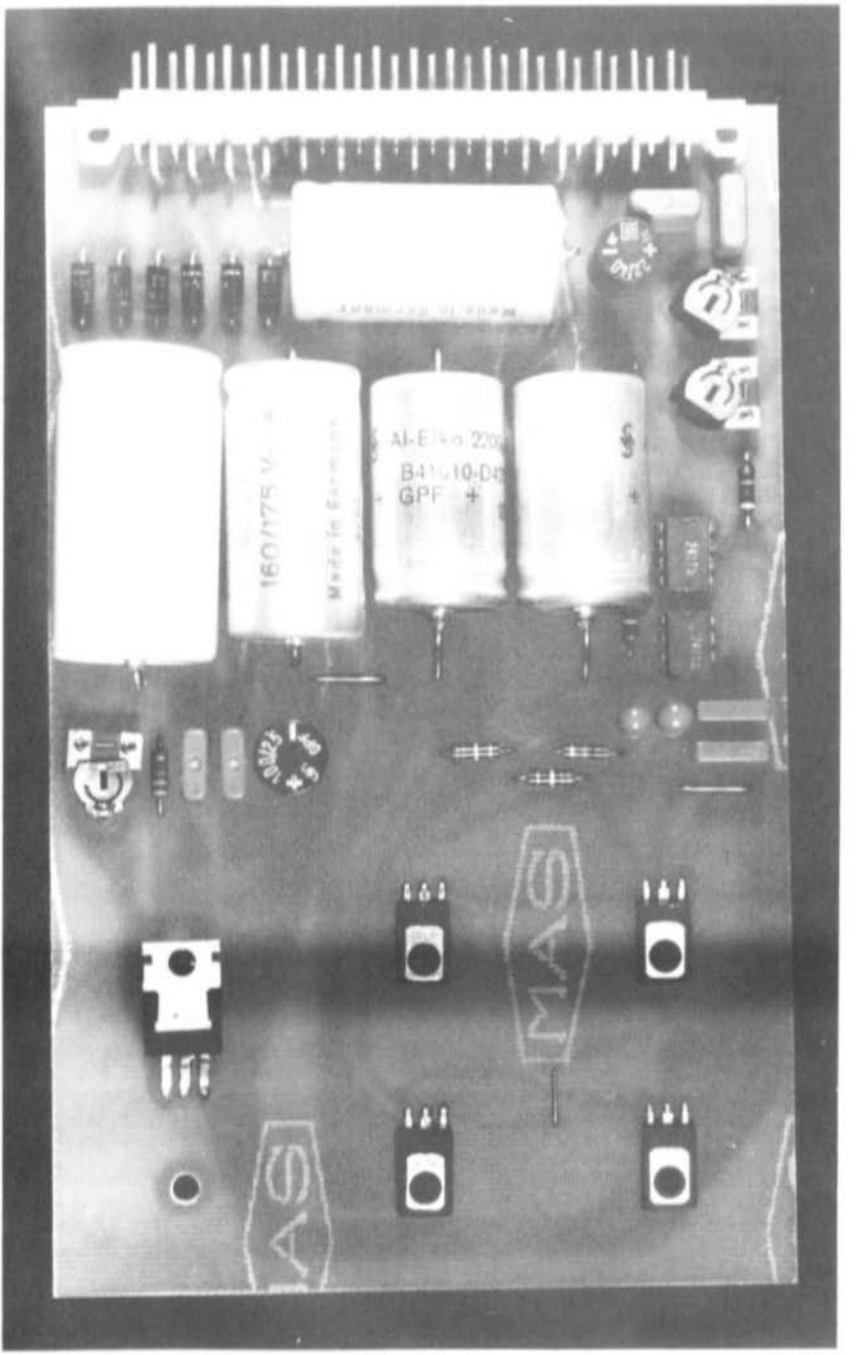


Fig. 29: Photograph of the author's prototype DC 3 NT 006 without heat sink (The five power semiconductors are mounted with the metal surface facing upwards !)

Heat sinks: 3 pcs. 1 mm aluminium plate 60 mm x 80 mm, drilled and bent as shown in Figure 30

Connectors: 31-pin according to DIN 41617 (Siemens)

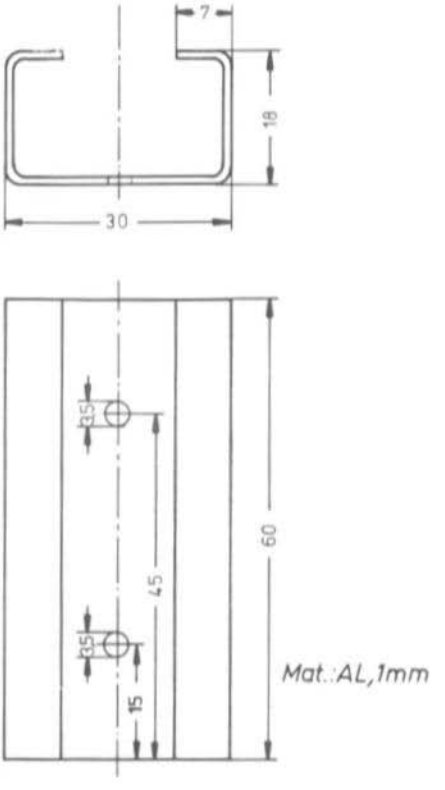


Fig. 30:
Three such heat sinks are required for the module DC 3 NT 006

5.3. DC 3 NT 008

Before discussing the circuit details of this module, one must mention the demands that are placed on this module.

Since the transmitted APT-image is only synchronized at the commencement of the image, high demands are placed on the stability of the deflection frequency. An approximation with the aid of a weather map is to be used to illustrate this:

The last line of the transmitted weather map of 2200 lines, length = 1.2 x width ≙ an index of cooperation of 576, may only be shifted by max. 1 %. This results in a permissible deviation of:

$$\text{Deviation} = \frac{\text{Max. permissible error}}{\text{Number of lines}}$$

$$\text{Permissible deviation} = \frac{0.01}{2200} \approx 0.5 \times 10^{-5}$$

If, on the other hand, a continuous frequency error of 0.5×10^{-3} (= 0.05 %) is present, this will mean that the last line of the image will be shifted by 100 %, which means that a square image will be shifted to an angle of 45°.

This is shown in **Figure 31**. It will be seen that it is necessary for the deflection frequencies to be derived from a crystal-controlled oscillator.

The same problem occurs when recording the sub-carrier using a tape recorder. If the signal was to be recorded and played back without further measures, it would be necessary for the wow-and-flutter and absolute speed deviations (when using different machines for recording and playing back) to be less than 0.5×10^{-5}. In order to avoid this »expensive« demand, it it possible for

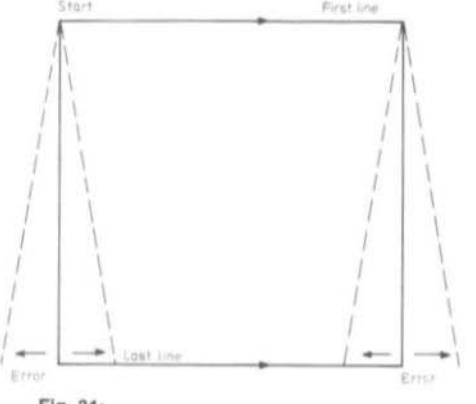


Fig. 31:
Distortion of the image due to speed deviations

a pilot tone derived from the crystal oscillator to be recorded on the second channel of a stereo tape recorder. This signal is then used as reference signal when playing back the recorded image. This method also allows simple, and far less expensive cassette recorders to be used.

Selection of the Required Frequencies

This is based on the requirements of the drum motor of the FAX-machine. The same requirements for the accuracy of the deflection frequency are valid for the speed of the drum motor as for the deflection frequency of the CRT.

Standard synchronous motors are optimized for 50 Hz, and this is why they are to be used as near to this frequency as possible in our application. These motors are mainly 8- pole or 12-pole motors. At 50 Hz, speeds of 375 or 250 rpm result. During the calculation of the required frequencies, a reduction gearing of 3:1 was taken into consideration for the 8-pole motors, or 2:1 in the case of the 12-pole motors.

Both reduction gears are regularly available, so that one can use either an 8-pole or 12-pole motor.

After studying the required speeds for image processing, the lowest common output frequency was examined from which all the motor frequencies should be obtained when using frequency division. The selected frequency is 1440 Hz. The drum speeds given in **Table 1** are all derived from this frequency.

Drum speed per minute	Drive frequency to the motor	Required division ratio
48	19.2 Hz	75
60	24.0 Hz	60
90	36.0 Hz	40
120	48.0 Hz	30
150	60.0 Hz	24
180	72.0 Hz	20
240	96.0 Hz	15

The operating frequency of the motor multiplied by the division ratio will result in a frequency of 1440 Hz. In actual fact, this is based on a frequency which is 60 times higher (86 400 kHz) since the two sinewave voltages phase-shifted by 90° are comprised of 60 pulses per sinewave.

This means that 60 pulses from a 86.4 kHz oscillator would result in a sinewave of 1440 Hz. This is followed by the variable frequency divider and a 90° phase shifter which derives a cosine wave from the sinewave signal. Both signals are then amplified separately and are used to drive the drum motor. Further details regarding the circuit are to be given later.

Now to the selection and generation of the pilot tone required for tape recording the image.

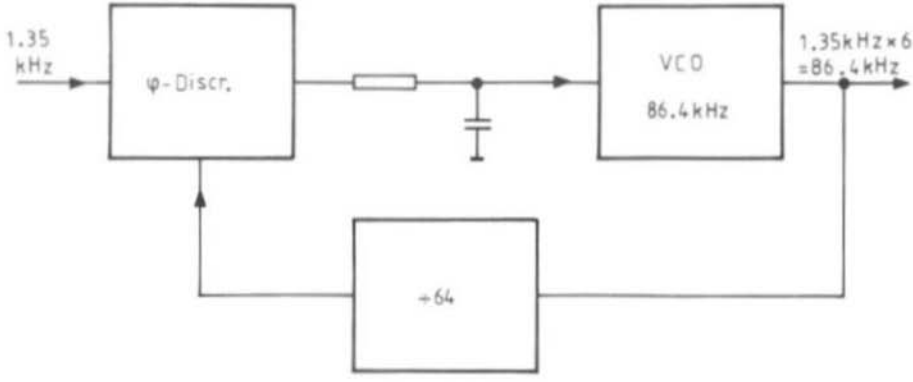


Fig. 32: A PLL-circuit generates the reference frequency of 86.4 kHz, even in the tape recorder mode

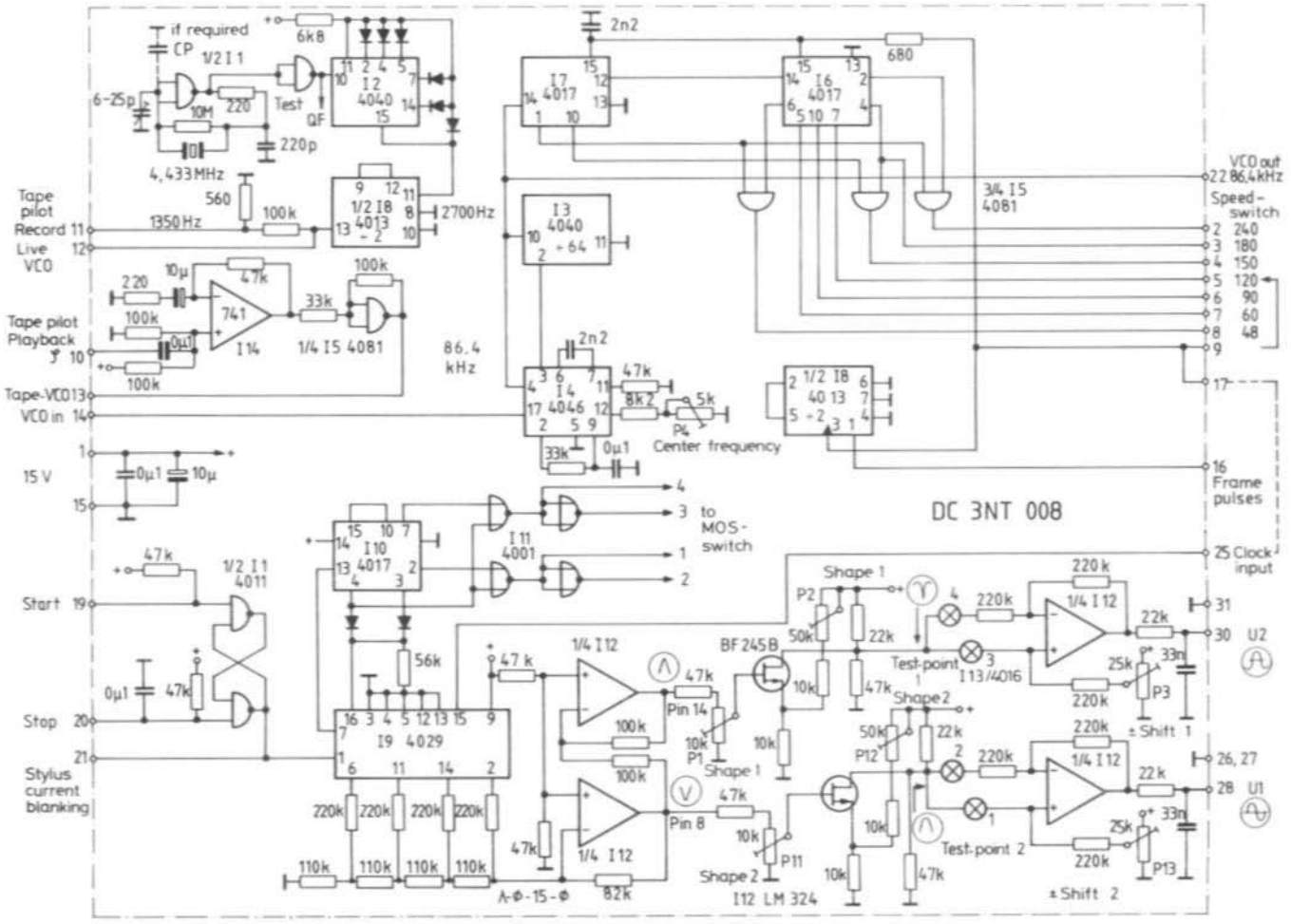


Fig. 33: The above circuit generates all frequencies required for image processing using the CRT, and FAX-machine – all required speeds are provided

A frequency of 86.4 kHz selected for driving the motor is not suitable for tape recording. Instead of this, a frequency of 1.35 kHz is used which can be derived by dividing the 86.4 kHz frequency by 64 (6 binary dividers). In order to ensure that the reference frequency is always available even if there are some faults on the tape such as drop-outs, the recorded frequency is only used to control a phase-control circuit (see **Figure 32**).

When processing directly without tape recorder – computer specialists would call this »on-line-operation« – the whole image processor including FAX-machine is controlled from a crystal-controlled frequency. In the case of tape recorded images («off-line-operation«) on the other hand, the tape recording will also possess this crystal-controlled frequency, however, the image processor will be controlled by the VCO shown in Figure 32, which will follow all fluctuations of the tape speed. This means that the exact time reference is maintained to the recorded image signal since this is also subject to the same speed fluctuations.

In order to consider this with respect to the overall system, it should be mentioned here that the previously mentioned frequency processing is used both for the FAX-machine and deflection when using a CRT. The generation of the deflection sawtooth signal (on board 009) is driven from the pulses of module 008 described here.

If not all image processing possibilities are to be used, a number of simplifications are possible, which are to be discussed in Section 5.3.5.

5.3.1. Circuit Details

The circuit diagram of module DC 3 NT 008 is given in **Figure 33**. As has been previously mentioned, the image processing is controlled from a 86.4 kHz oscillator, which is synchronized with the aid of a phase-control circuit to the reference frequency of 1350 Hz. This reference frequency originates either directly from a crystal oscillator (which is shown in the left upper corner of Figure 33) or via a tape recorder.

A frequency divider that can be programmed with diodes (I 2 = 4040) is used, which has the advantage that virtually any crystal in the frequency range between 2.7648 and 5.52 MHz can be used. The only prerequisite is that its frequency can be pulled to a multiple of 2.7 kHz. A trimmer capacitor and room for a parallel capacitor CP (if required) are provided at the crystal oscillator (2 gates of I 1). In order to program the frequency division ratio, silicon diodes should be soldered into place at I 2 according to the following **Table 2:**

Division ratio	Diode to reset from output/pin	
1	Q 1	9
2	Q 2	7
4	Q 3	6
8	Q 4	5
16	Q 5	3
32	Q 6	2
64	Q 7	4
128	Q 8	13
256	Q 9	12
512	Q 10	14
1024	Q 11	15
2048	Q 12	1

The method is now to be described in the author's example using a PAL-subcarrier crystal of 4.433 MHz:

Firstly, the required division ratio is calculated: 4433.6 kHz : 2.7 = 1642.07.

When rounded down, this results in 1642. This is followed by calculating the frequency to which the crystal oscillator should be tuned:
2.7 kHz x 1642 = 4433.40 kHz.

The frequency division ratio should now be divided into two orders of magnitude:
1642 = 1024 + 512 + 64 + 32 + 8 + 2.

This means that six diodes are required in the manner shown in the circuit diagram. This should be checked according to the table !

For those readers where this method is too complicated or a suitable crystal is not available, it is possible for a bridge to be made from ground to reset (pin 11), and then for a crystal of 2.7 kHz x 1024 = 2764.80 kHz to be used.

The programmable divider is followed by a flipflop (1/2 I 8) which divides the 2700 Hz to 1350 Hz and provides a keying ratio of 1 : 1. A voltage divider is provided for the tape recording mode, whereas the 1350 Hz signal is fed directly to the VCO (I 4) for on-line operation. The signal from the tape recorder is passed via a preamplifier equipped with I 14 and a gate (1/4 I 5). This means the following connections are required via suitable switches:

On-line operations: Pin 12 to pin 14

Tape recorded images:
Pin 11 to tape recorder input
Pin 10 to tape recorder output
Pin 13 to pin 14.

The phase-control circuit given in Figure 32 is realized with the aid of integrated circuits I 3 and I 4. As one can see, the same component is used for the divide-by-64 IC as for the reference frequency divider. If another frequency is required for the pilot tone, it is possible for the circuit of I 3 to be changed according to the previous table.

This is followed by the frequency dividers for the drive voltage of the drum motor. The integrated circuits I 5, I 6 and I 7 are provided for this. The frequencies times 60 listed in Table 1 are fed via a seven-position selector switch to pins 9 and 17, and finally to the clock input (pin 25).

The flipflop I 8 (1/2 4013) divides the selected frequency once again by 2 to provide the so-called frame pulses at connection 16 for generation of the sawtooth signal required for deflection of the CRT.

The following circuits equipped with I 9 to I 13 generate the two 90° phase-shifted voltages for driving the drum motor. For those readers who do not intend to use the FAX-machine but only image processing using the CRT, it is possible for this part to be deleted.

In order to ensure a smooth run of the FAX-machine, it is absolutely necessary to ensure that the two motor voltages are exactly phase-shifted by 90° and are adequately sinewave. Since these demands must be fulfilled at seven different frequencies, a considerable amount of care is required. In our case, the sinewave and cosine voltage are approximated with the aid of digitally generated staircase voltages.

To achieve this, the input pulses from the frequency divider are passed via connection 25 to the input of an up-down counter (I 9), which is followed by a push-pull amplifier that operates as a digital/analog converter. The counter counts 15 steps upwards and then 15 steps downwards, whereby a staircase voltage results with 1/30 of the drive frequency. The subsequent phase-shifting by 180° results in a phase-shift of 90° at the final frequency, since it coincides to half that of the triangular voltage.

The two triangular voltages are shaped in a FET to sine halfwaves, and the operating point and drive can be exactly set with the aid of trimmer potentiometers in order to ensure that the correct slope is used. Finally, this is followed by two switches in each branch (integrated MOS-switches) that are switched every second halfwave thus generating sinewave voltages. The polarity switching represents an alternating connection of the signal to the plus and minus input of the output amplifiers. The joining of one positive and one negative halfwave represents the last halving of the original staircase voltage, and thus results in the required motor frequencies with a phase-shift of 90°.

5.3.2. Component Details

I 1:	4011
I 2, I 3:	4040
I 4:	4046
I 5:	4081
I 6, I 7, I 10:	4017
I 8:	4013
I 9:	4029
I 11:	4001
I 12:	LM 324
I 13:	4016
I 14:	741
T 1, T 2:	BF 245 B

All diodes (8 pcs.): 1 N 4151 or similar

1 crystal 4.433 MHz HC-6/U (see text)

1 plastic-foil trimmer, yellow, spacing 10/5 mm (Philips)

1 styroflex capacitor 220 pF (for I 1)

1 styroflex capacitor 2200 pF (for I 4)

Plastic-foil capacitors for 7.5 mm spacing:
4 x 0.1 µF, 2 x 33 nF

1 ceramic capacitor 2.2 nF

2 tantalum electrolytics: 10 µF

All resistors: for 10 mm spacing

7 helical trimmer potentiometers with 10 or 15 turns for 12.5 / 2.5 mm spacing (see component location plan)

Values: 1 x 5 kΩ
2 x 10 kΩ
2 x 25 kΩ
2 x 50 kΩ

1 31-pin connector (DIN 41617) (Siemens)

5.3.3. Construction of Module DC 3 NT 008

For accommodation of the circuit given in Figure 33, a double-coated PC-board without through-contacts was designed. The designation is DC 3 NT 008 and is given in **Figure 34**. This board has the Europe-card dimensions of 160 mm x 100 mm and is provided with through-contacts at various positions when mounting the components.

This method is, of course somewhat more complicated than when using a PC-board with through-contacts, but is considerably cheaper. Since these through-contacts are made manually by soldering on both sides of the board, only such positions were selected for this that were not covered by components. However, when sockets are to be used for the integrated circuits, these should be types that can also be soldered on the component side of the board.

The circuits for the FAX-machine, which need only be equipped when required, are clearly marked on the PC-board with the aid of a dashed line. For those readers only wishing to operate with the CRT, it is possible for all components accommodated below this line to be deleted.

Finally, it should be noted that this PC-board should not be located where the highest temperatures are to be found within the unit.

5.3.4. Alignment

For alignment, the module should be connected temporarily in the following manner:

Pin 1 to + 15 V, pin 15 to ground; make a bridge from pin 17 to pin 25 and from pin 9 to pin 2. This is the connection for FAX-operation with a speed of 240 lines per minute.

It is now possible for the crystal oscillator to be aligned by connecting a frequency counter to pin 10 of I 2 and aligning the oscillator to the nominal frequency of 4433.4 kHz with the aid of the trimmer (and parallel capacitor if required).

This is followed by alignment of the VCO. The frequency counter is connected to pin 4 of I 4 or to connection 22 of the 31-pin connector. The oscillator is now aligned with the aid of P 4 to 86.4 kHz. If the adjustment range of the helical potentiometer is not sufficient, the dropper resistor should be changed to the next higher or lower standard resistance value.

This is followed by checking the operation of the frequency dividers for the pilot tone by connecting the frequency counter to pin 12 of the 31-pin connector. A frequency of 1350 Hz should be measured at this point.

Direct operation is selected by connecting a bridge from pin 12 to pin 14. In this case, the VCO should be adjusted to exactly 86.400 kHz via its phase-control loop. This is followed by connecting the frequency counter once again to pin 22 of the 31-pin connector. The indication should not vary by more than ± 1 digit (last digit), even when varying the operating voltage by ± 1 V.

Now a tip for fault finding:

Half the operating voltage should be present at pin 2 of the 4046 after the phase-control loop has locked in. However, a high-impedance voltmeter is required for this measurement.

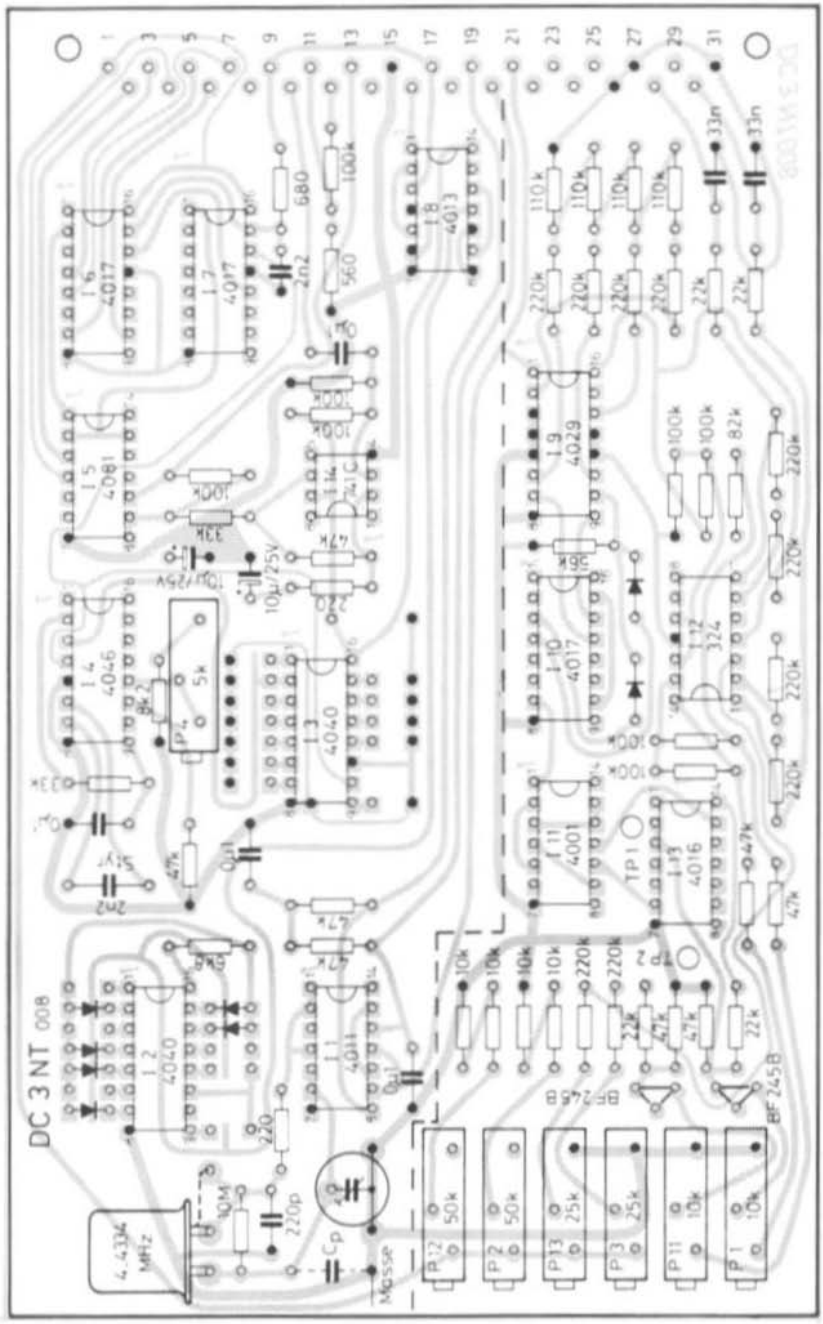
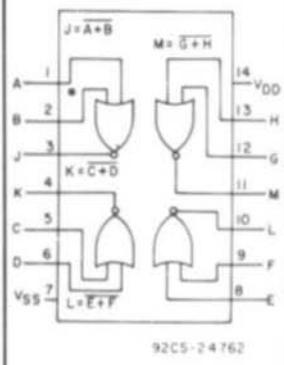
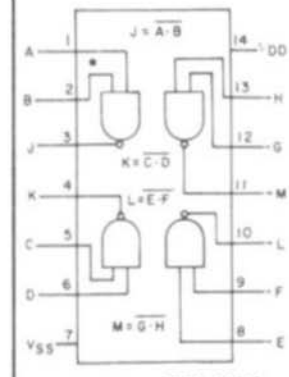


Fig. 34: PC-board DC 3 NT 008 is double-coated, but without through-contacts. If the FAX-machine is not required, the components located below the dashed line can be deleted



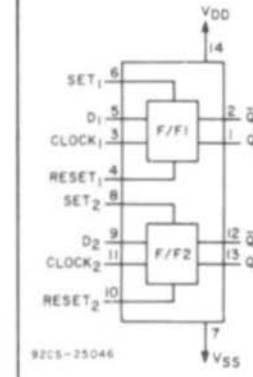
Quad 2-Input NOR Gate

CD4001B (File No. 985)
CD4001UB (File No. 945)



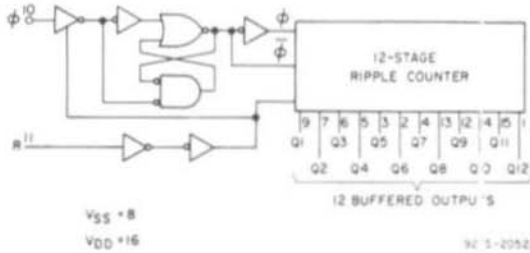
Quad 2-Input NAND Gate

CD4011B (File No. 936)
CD4011UB (File No. 947)



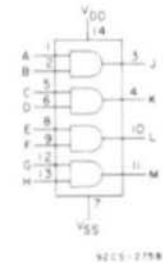
Dual "D" Flip-Flop with Set/Reset Capability

CD4013B (File No. 936)



12-Stage Binary Ripple Counter

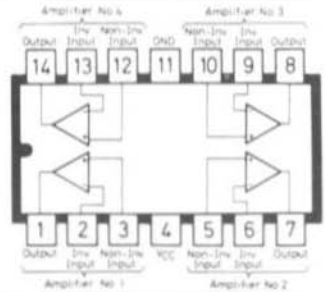
CD40408



Quad 2-Input AND Gate

CD4081B (File No. 806)

LM 324



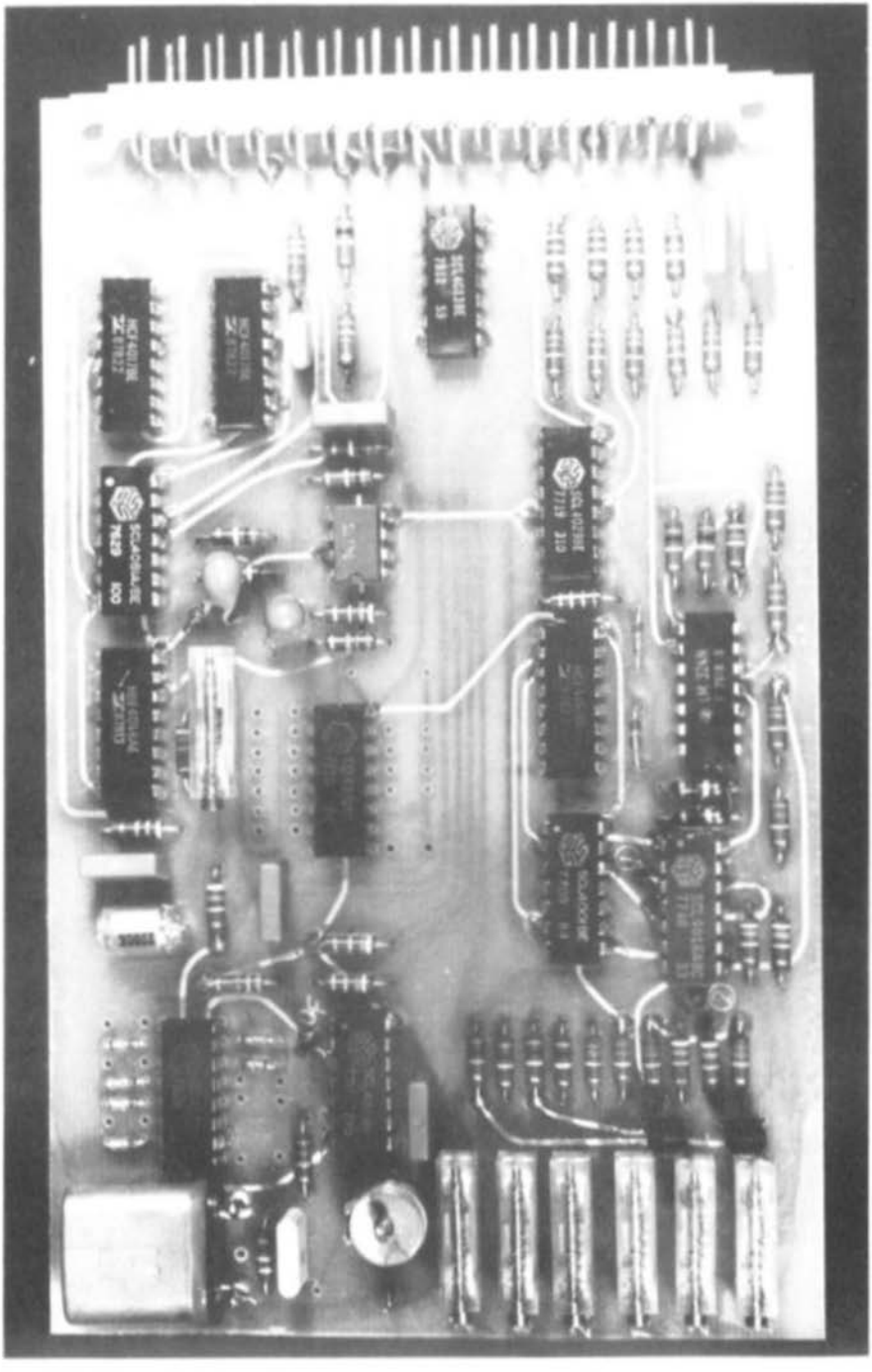
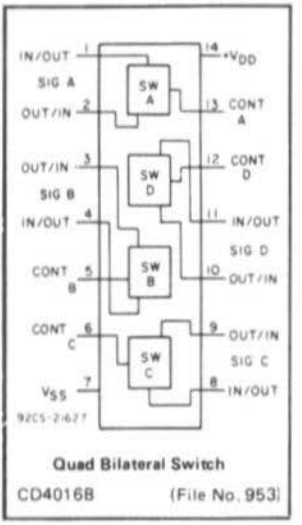
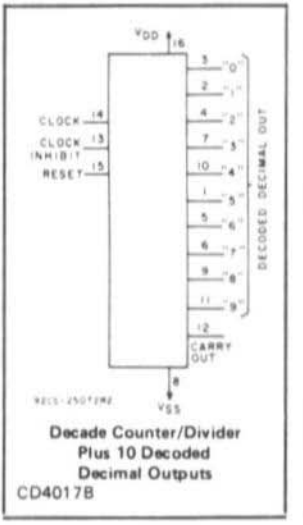


Fig. 35: Photograph of the author's prototype of module DC 3 NT 008



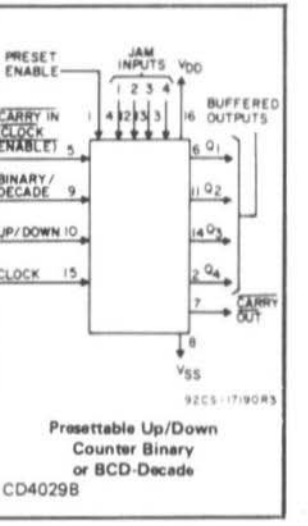
Quad Bilateral Switch

CD4016B (File No. 953)



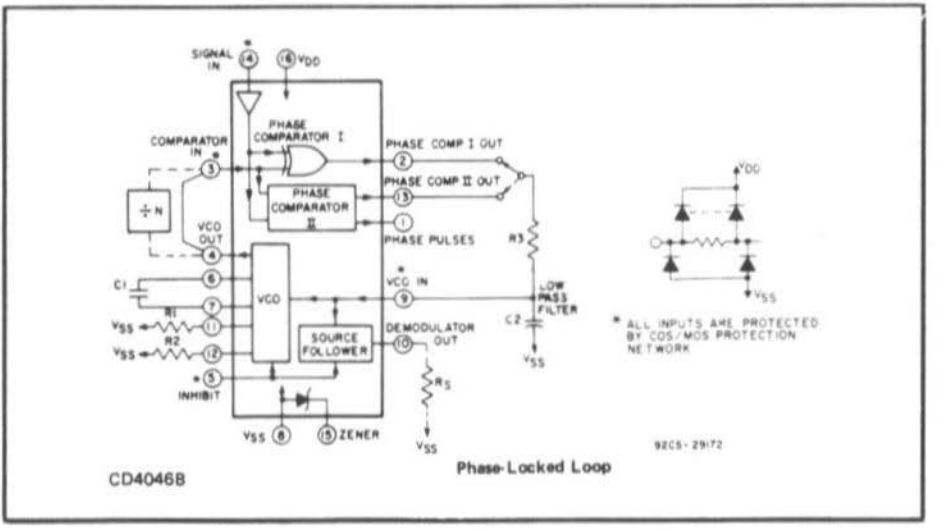
Decade Counter/Divider Plus 10 Decoded Decimal Outputs

CD4017B



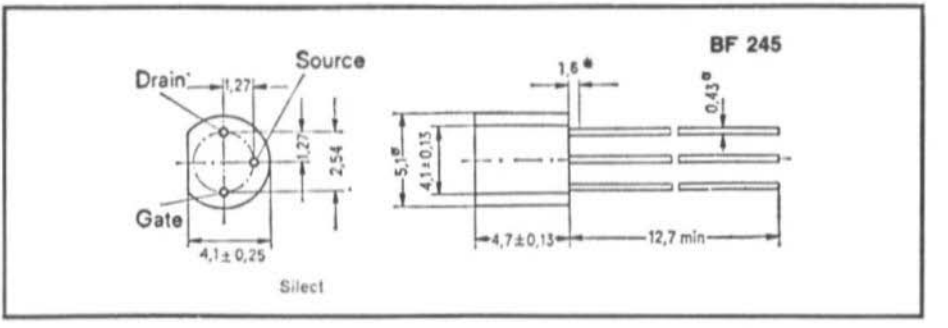
Presettable Up/Down Counter Binary or BCD-Decade

CD4029B



CD40468

Phase-Locked Loop



Silect

It is now the turn of the frequency divider for the various speeds to be measured. If the frequency counter is connected to pin 16 of the 31-pin connector, one will also measure the 2 : 1 divider for the frame pulses. Otherwise, one can measure twice the given frequencies at pin 9. The following frequencies should result on switching, or by connecting a bridge between pin 9 and one of the pins 2 to 8:

Speed	Frequency at pin 16	Bridge from 9 to
240	2880 Hz	2
180	2160 Hz	3
150	1800 Hz	4
120	1440 Hz	5
90	1080 Hz	6
60	720 Hz	7
48	576 Hz	8

Table 3: Frequencies for checking the operation of the frequency divider

The last alignment and measurement is the generation of the two sinewave voltages for the drum motor. To do this, pin 9 is once again connected to pin 2 and the »start«-input should be grounded (bridge from pin 15 to pin 19). It should be possible to see the staircase voltages after connecting an oscilloscope to the outputs of the two first operational amplifiers (pin 14 or pin 8 of I 12). A peak-to-peak staircase voltage of approximately 11 V should be present.

Potentiometers P 1 to P 3 and P 11 to P 13 should be centered and the oscilloscope connected firstly to test point 1. The voltage should be adjusted to best possible dual-path sinewave with the aid of potentiometers P 1 and P 2. The same is then carried out with the other phase by connecting the oscilloscope to TP 2 and adjusting potentiometers P 11 and P 12.

After this, the oscilloscope is connected to pin 30 of the 31-pin connector and the shift in the zero-pass of the sinewave curve is adjusted to minimum with the aid of potentiometer P 3. Finally, the same should be made for the other phase with P 13 with the oscilloscope connected to pin 28.

As a final check, one should subsequently connect outputs 30 and 28 to the X- and Y-inputs of the oscilloscope to see whether a circular figure is visible with the same gain in both channels.

Figure 35 shows a photograph of the author's prototype after completion.

5.3.5. Possible Modifications

As has been mentioned previously, there are two possible simplifications if all image processing possibilities are not to be used.

For those readers who are not interested in driving a FAX-machine, it is only necessary to delete all components located below the dashed line in Figure 34.

A far greater simplification is possible when using the CRT image processor and limiting the speeds to 240 lines/minute for METEOSAT and GOES, and 120 for NOAA and TIROS, as well as deleting the possibilitiy of using a tape recorder. In this case, an extremely simple circuit has been developed which is shown in **Figure 36**.

However, no PC-board or kit has been developed for this.

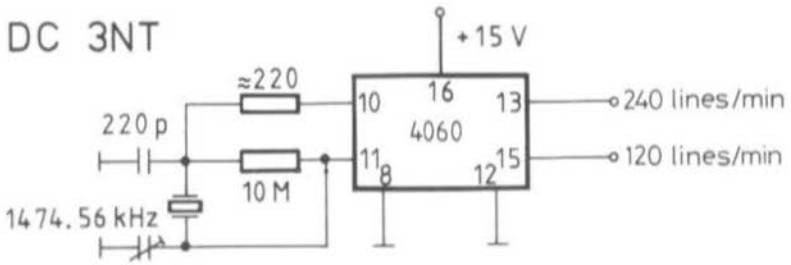


Fig. 36: Simple circuit for operating only in the CRT-mode with only two speeds, and without tape recorder facility

A 29 MHz Transverter for Use with 145 MHz Transceivers

by J. Kestler, DK 1 OF

Many descriptions of UHF and SHF transverters for the 70, 23 and 13 cm bands are designed for use with exciters and receivers operating in the 10 m band between 28 and 30 MHz. Such transceivers are usually not available in the shacks of »VHF-only« amateurs and even if they are available, they usually produce output powers of 100 W and more. This means that it is necessary to either provide large attenuators, or to carry out modifications to the equipment. Furthermore, hardly any of the shortwave transceivers can operate in the FM-mode.

For this reason, the author has developed a frequency transverter which can be used as intermediate module between a 2 m transceiver and UHF-SHF transverters using a 10 m IF; the transverter can handle drive powers of up to approximately 10 W and does not require any transmit/receive switching.

1. CONCEPT

The characteristics of Schottky diode mixers have been discussed in detail in previous publications. In addition to their good large-signal characteristics, this mixer allows one to simply exchange the RF and IF output (input and output); this means that the same mixer and oscillator module can be used both in the transmit and receive mode without switching.

As can be seen in the block diagram given in **Figure 1**, the antenna connector of the VHF transceiver is connected to connection A of the transverter. The voltage divider comprising R 1 and R 2 accepts the full output power of the exciter in the transmit mode and ensures an optimum load impedance of approximately 50-60 Ω for the 2 m transmitter. The subsequent amplifier stage equipped with the bipolar high-current transistor T 1 generates an overall gain for the transverter of approximately + 6 dB including mixer and matching losses; in the transmit mode, T 1 will be driven in the wrong direction and will cause a (desired) signal attenuation to ensure that the ring mixer is not overdriven. A matching link on this and the two other ports of the mixer ensures a correct 50 Ω termination of the ring mixer, which is very important with respect to correct operation.

The converted transmit signal is then fed via a 4-stage lowpass filter to connection B of the transverter; the task of the lowpass filter is to suppress the image frequency as well as any residual components of the input and oscillator frequency. An output power of 1 mW is available in the transmit mode at point B.

The oscillator module of the unit does not offer any special features. The required local oscillator frequency of 116 MHz is obtained using a 38.667 MHz crystal oscillator with subsequent tripler. This is followed by

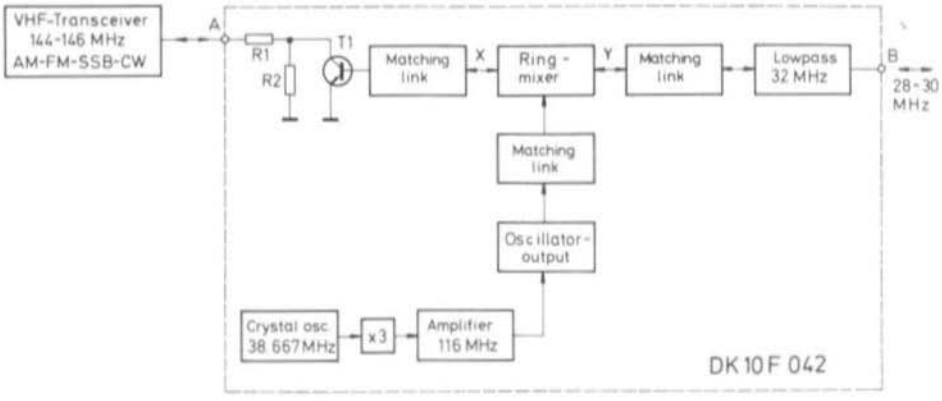


Fig. 1: Block diagram of the transverter 145-29 MHz

a two-stage amplifier which is then able to provide an output power of approximately 10 mW which is the optimum drive level for the ring mixer.

2. CIRCUIT DETAILS

2.1. Input Attenuator and Amplifier T 1

The full circuit diagram of the amplifier stage which is used as attenuator in the transmit mode and as amplifier in the receive mode is shown in **Figure 2**.

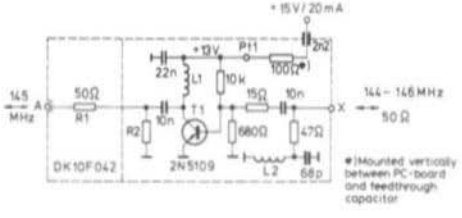


Fig. 2: 145 MHz-module of the transverter

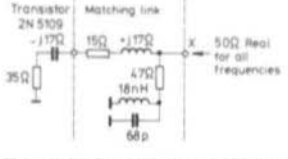


Fig. 3: 50 Ω matching circuit to the input impedance of transistor T 1

A high-current transistor having a high cut-off frequency was selected for transistor T 1. The rating of R 1, as well as the resistance value of R 2 are dependent on the drive power to be fed to point A. Further details regarding this are given in the »Alignment Section«.

Since the input impedance of T 1 possesses a capacitive component, and is also frequency-dependent, it is necessary for a transformation link to be provided for matching it to the ring mixer. **Figure 3** shows the relationships in detail; in practice, the series inductance of + j 17 Ω is formed by the geometric arrangement of the series circuits of the 15 Ω resistor and the 10 nF capacitor (see Figure 2).

The given matching link ensures tha a real terminating resistance of 50 Ω is provided at point X, which is the RF-connection of the ring mixer.

2.2. Oscillator Module

A circuit diagram of the oscillator module is given in **Figure 4**. The crystal-controlled Pierce oscillator (third overtone) can be seen at the left of the circuit. The operating voltage for this transistor is stabilized with the aid of D 1. According to the crystal used, it may be necessary to provide a parallel capacitance C 1 (3-10 pF), in order to pull the crystal to the exact frequency. A fine alignment of approximately ± 2 kHz is

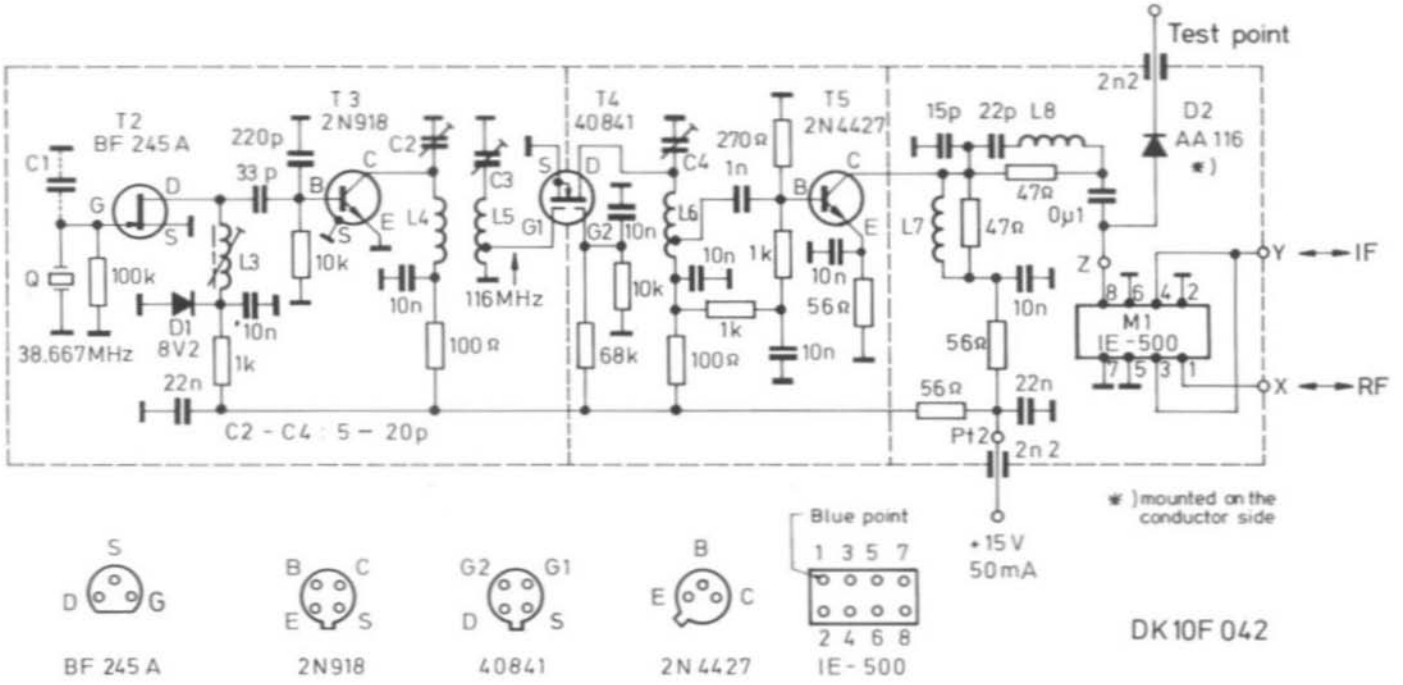


Fig. 4: Circuit diagram of the oscillator

possible with the aid of L 3. The following tripler stage operates in class C and is coupled to transistor T 3 capacitively. A bandpass filter (L 4, L 5) is provided between T 3 and the buffer stage T 4. This filter suppresses any residual components of the fundamental frequency, as well as any unwanted harmonics. The output stage of the oscillator module T 5 operates in class A and is able to provide an output power of approximately 10 mW for driving the ring mixer. Test diode D 2 serves as alignment aid.

The matching link comprising L 7 / L 8 and the adjacent resistances and capacitors seems somewhat complicated. Since this circuit was not discussed in (1), it is to be dealt with in some detail in the appendix.

2.3. IF-Filter

Of course, any mixer will provide a number of unwanted conversion products from harmonics of the input frequencies in addition to the sum and difference of these input frequencies. In order to obtain a clean transmit signal for the UHF/SHF transverter, it is important that the 29 MHz output signal is as clean as possible. For this reason, the author designed a relatively extensive intermediate filter. As can be seen in **Figure 5**, the filter mainly consists of a four-stage lowpass filter comprising L 11 to L 14 and C 7 to C 14, since most of the interfering components are in excess of 30 MHz.

The input and output of the filter are in the form of a bandpass filter link, which is similar to an absorption filter, in contrast to reflection filters which are built up using only purely reactive impedances. When correctly dimensioned, it is possible for the input and output impedance of the circuit to be real (50 Ω) over a wide frequency range (theoretically from 0 to ∞). Since the filter is built up symmetrically, a further ring mixer can be connected to connection B without further measures.

3. CONSTRUCTION

A single-coated PC-board of 120 x 72 mm was designed for accommodation of the described transverter. The designation of the board is DK 1 OF 042. It is possible for the whole module including attenuator resistor R 1, to be accommodated in a 145 x 73 x 28 mm tinplate case. The dashed lines given in the component location plan **(Figure 6)** are the positions of the screening panels that should be soldered into place on the upper and lower side of the board. The spacing should amount to approximately 8 mm on the conductor side of the board. The interconnection Y-Y can be made with the aid of a normal piece of wire, whereas connection X-X should be made with the aid of a thin piece of coaxial cable. A photograph of the author's prototype is given in **Figure 7**.

3.1. Special Components

T 1:	2 N 5109 (RCA)
T 2:	BF 245 A (TI)
T 3:	2 N 918, 2 N 5179 (Motorola, RCA)
T 4:	40841, 40673 (RCA)
T 5:	2 N 4427 (various manufacturers)
M 1:	IE-500 (MCL)
D 1:	BZX 97 C 8 V 2 or similar zener diode
D 2:	AA 116 or similar germanium diode

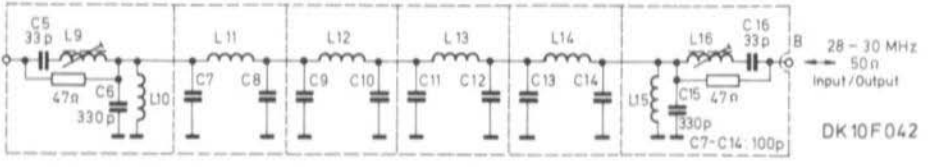


Fig. 5: The 29 MHz filter

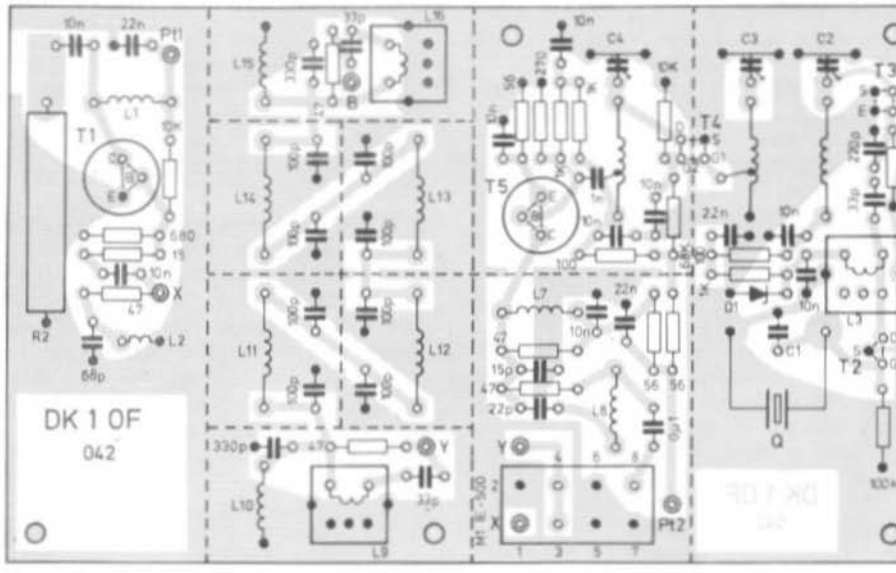


Fig. 6: Component locations on PC-board DK 1 OF 042

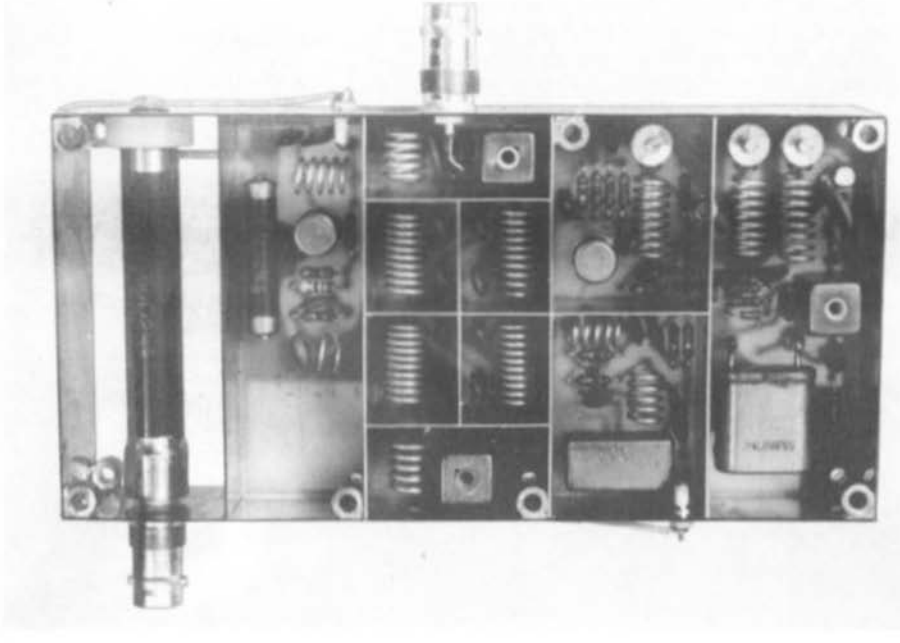


Fig. 7: Photograph of the author's prototype

R 1: 50 Ω carbon resistor without connection leads, rating dependent on drive power of the exciter.

R 2: Carbon resistor, value see Figure 2. Length max. approx. 30 mm

L 1, L 7, L 8, L 10, L 15: 5 turns of 1 mm silver-plated copper wire, wound on a 5 mm former, length 10 mm.

L 2: 2 turns, length 5 mm, otherwise as L 1

L 3: 10 turns of 0.3 mm enamelled copper wire, using special coil set with violet core

L 4: 8 turns, length 15 mm, otherwise as L 1

L 5: as L 4, tap at 2.75 turns from the cold end

L 6: as L 4, tap at 1.75 turns from the cold end

L 9, L 16: 14 turns, otherwise as L 3

L 11, L 12, L 13, L 14: 10 turns, length 15 mm, otherwise as L 1

C 2, C 3, C 4: Plastic-foil trimmer, 22 pF (green), 7.5 mm dia.

All fixed capacitors: Ceramic disk types

Q: Crystal 38.667 MHz, parallel resonance, HC-6/U

Resistors of the type required for R 1 are often quite difficult to obtain. However, it is possible to use a larger number of resistors of a higher resistance value and to connect these in parallel (e.g. 20 resistors 1 kΩ/ 0.5 W) or an available, external attenuator as used with the microwave modules transverter MMT 432/144 (required values: 13 dB attenuation with an input power of 2 W, or 20 dB at 10 W).

4. ALIGNMENT

This is commenced by checking the operation of the crystal oscillator: A voltmeter is connected in parallel with the collector-filter resistor of T 3 and inductance L 3 is aligned to obtain a current maximum of approximately 3 mA (corresponding to 0.3 V across 100 Ω). The voltmeter (≧ 50 kΩ) is then connected between the test point (diode D 2) and ground and trimmer C 2, C 3 and C 4 trimmed alternately several times for maximum reading. A value of approximately 0.6 to 0.9 V should be obtained. In order to ensure that the correct harmonic has been selected, this should be checked by loosely coupling a frequency counter to inductance L 6.

If the oscillating frequency of the crystal is more than 2 kHz too high when inductance L 3 has been aligned for maximum collector current of T 3, this can be corrected with the aid of a parallel capacitance C 1, which must be found experimentally but will be in the order of approx. 3 to 10 pF; the fine alignment is made with L 3. The voltage drop across the emitter resistor of T 5 should be in the order of approximately 1.8 V under drive conditions, and approximately 1 V without signal (crystal short-circuited, or L 3 detuned).

The collector current of transistor T 1 should amount to approximately 15 to 25 mA without 145 MHz drive; if required, the 10 kΩ resistor between the base and Pt 1 can be corrected slightly. For further alignment, connector A of the transverter is connected to the output of a 2 m exciter and connector B either to a 10 m receiver via a suitable attenuator, or to a RF-voltmeter. Inductances L 9 and L 6 (alignment cores), as well L 10 and L 15 (depressing or pulling out) should now be aligned for maximum signal at 29 MHz. The maximum is relatively wide due to the low Q of the input and output of the filter (Q = 3); if necessary, this alignment can be deleted.

The resistance value of R 2 is dependent on the output power of the VHF transceiver, and also on the required drive power of the subsequent UHF/SHF-transverter. For this reason, no concrete details can be given here. It is, however, advisable to commence with low values of R 2 and slowly approach the saturation power; in the SSB-mode, it is advisable to remain at least 3 dB below saturation.

If a suitable oscilloscope is available, it is possible for the envelope curve of the 29 MHz output signal to be checked by observing voice modulation. No visible flat topping of the modulation peaks should be observed.

5. APPENDIX

Bandpass-Link as Matching Circuit for Ring Mixers

This represents an addition to (1). A circuit is to be discussed that allows a ring mixer to be exactly matched to a component having a parallel capacitance (e.g. transistor input).

As can be seen in the circuit diagram given in **Figure 8**, it is possible to combine Ca and Cp, as well as Ra and Rp, since they are connected in parallel. The simplified circuit is given in **Figure 9**. In this case, the following is valid:

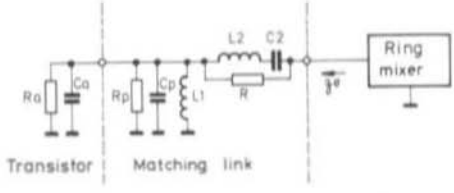


Fig. 8: Bandpass filter link as matching circuit for the ring mixer

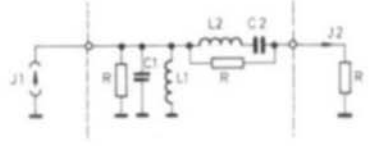


Fig. 9: Simplified circuit

$$C1 = Ca + Cp \text{ and } R = \frac{Ra \times Rp}{Ra + Rp}$$

The input impedance of the circuit as seen from the ring mixer amounts to $\underline{Z}_{in} = R$ when it is assumed that

$$R^2 = \frac{L1}{C2} = \frac{L2}{C1}$$

This means that it is frequency-independent, real and can be determined by selection of R.

$$\frac{L1}{C2} = \frac{L2}{C1} \text{ is the same as}$$

$$L1 \times C1 = L2 \times C2$$

This means that parallel and series resonant circuits are tuned to the same frequency. The following ratio can be selected freely:

$$\frac{C1}{C2} \text{ or } \frac{L2}{C1}$$

This allows the Q and thus the bandwidth Δf to be determined as:

$$Q = \sqrt{\frac{C1}{C2}} = \sqrt{\frac{L2}{L1}}, \quad \Delta f = \frac{f_0}{Q}$$

The center frequency results as:

$$f_0 = \frac{1}{2\pi\sqrt{L1 \times C1}} = \frac{1}{2\pi\sqrt{L2 \times C2}}$$

The attenuation curve of the circuit as a function of frequency is given by the complex attenuation magnitude A:

$$A = \frac{\underline{I}_1}{2\,\underline{I}_2} = 1 + j\,Q\,\eta$$

η is usually defined as the »standardized detuning« and results as:

$$\eta = \frac{f}{f_0} - \frac{f_0}{f}$$

The value of the attenuation is

$$a = |A| = \sqrt{1 + Q^2\eta^2}$$

as numerical value and

$$A = 20 \times \log a$$

in dB.

The attenuation curve as a function of Q x η is given in **Figure 10**, and corresponds to the selectivity curve of a simple resonant circuit.

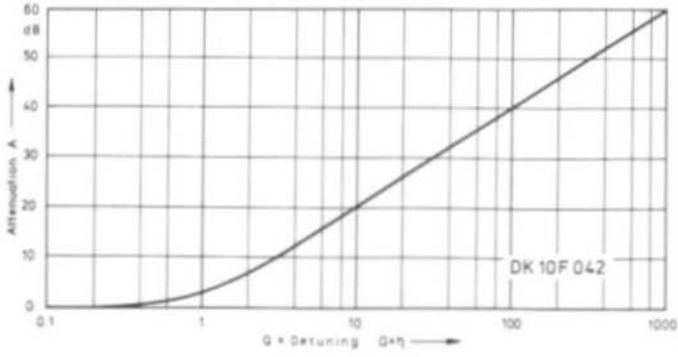


Fig. 10:
Standardized attenuation curve of the circuit given in Fig. 8

After converting the given equations, the following equations are obtained that can be used for designing the required filters:

$$L1 = \frac{R}{2\pi f_0 \times Q} \qquad C1 = \frac{Q}{2\pi \times f_0 \times R}$$

$$L2 = \frac{Q \times R}{2\pi \times f_0} \qquad C2 = \frac{1}{2\pi \times f_0 \times Q \times R}$$

$$Cp = C1 - Ca \qquad Rp = \frac{R \times Ra}{Ra - R}$$

The Q-value should not be higher than necessary (< 10), otherwise component values will result that cannot be realized in practice.

6. REFERENCES

(1) J. Kestler: Matching Networks for Schottky Ring Mixers
VHF COMMUNICATIONS 6, Edition 1/1976, pages 13 - 18

A Noise Blanker for Large-Signal Conditions Suitable for Shortwave and VHF-Receivers Having a Large Dynamic Range

Part 2

by M. Martin, DJ 7 VY

Part 1 of this article discussed the various interference signals and their suppression as well the individual parts of a noise blanker. This part is to discuss construction of such an extensive noise blanker in conjunction with PC-board DJ 7 VY 003, which can be extended up to three different triggering possibilities in the noise blanking mode. Furthermore, some information is to be given regarding the construction of an input stage for shortwave operation.

5. CIRCUIT DESCRIPTION

The overall circuit diagram of the noise blanker system is given in **Figure 10 and 11.** In addition to the HF-triggering given in (7), the author has added AF-triggering and power-line triggering.

5.1. Required-Signal Path

When switched off, the blanker is bypassed in a wideband manner with the aid of two miniature relays. After switching on, all signals will be passed via the first relay and diplexer (C 1, L 4, C 2, L 5) to reach the first directional amplifier T 1 and the preamplifier T 4 for the interference channel receiver. Diodes D 1 and D 2 are provided with the relay energizing current and ensure an improved cross-talk attenuation between input and output of the blanker. Transistor T 1 is followed by the delay crystal filter which can be replaced by a wideband resonant circuit (22 nF from A to C, and R 1, L 8 and Tr 2 can be deleted) in the case of the version with matching input stage. The second directional amplifier T 2 is to be found subsequent to the crystal filter, which is then followed by the actual blanker, a linear gate equipped with diodes D 3 to D 6. The signal is then passed from here via the second miniature relay to the output of the required-signal path.

5.2. Interference Channel Receiver

In order to ensure that the signal-to-noise ratio at the input of T 1 is not deteriorated in the signal-splitting process, a high-impedance preamplifier equipped with T 4 as source follower is used. A resonant circuit tuned to the required receive band is to be found at the output of this transistor, which is then followed by the input transformer Tr 8 of the integrated receiver circuit I 1. The oscillator signal for I 1 is generated externally in transistor T 5 which simplifies the oscillator supply when using various frequency ranges.

The intermediate frequency is 2 MHz, and the bandpass filter comprising L 2 and L 3 should be designed so that it provides a flat top within the passband range. The IF-output voltage will be transformed up due to the tap on L 3 and passed at low impedance via transistor T 6. The impedance

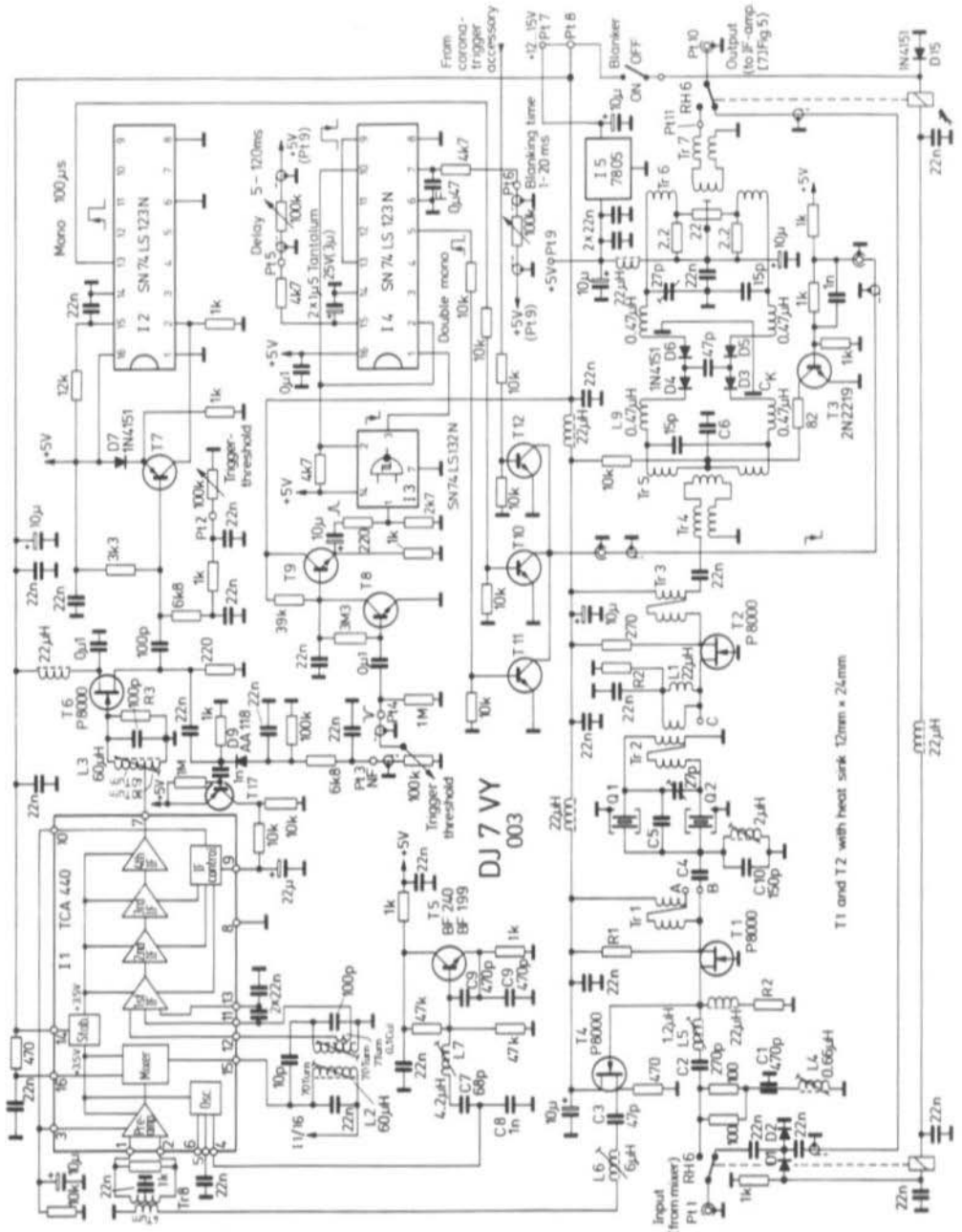


Fig. 10: Large-signal noise blanker for shortwave and VHF-receivers having a large dynamic range

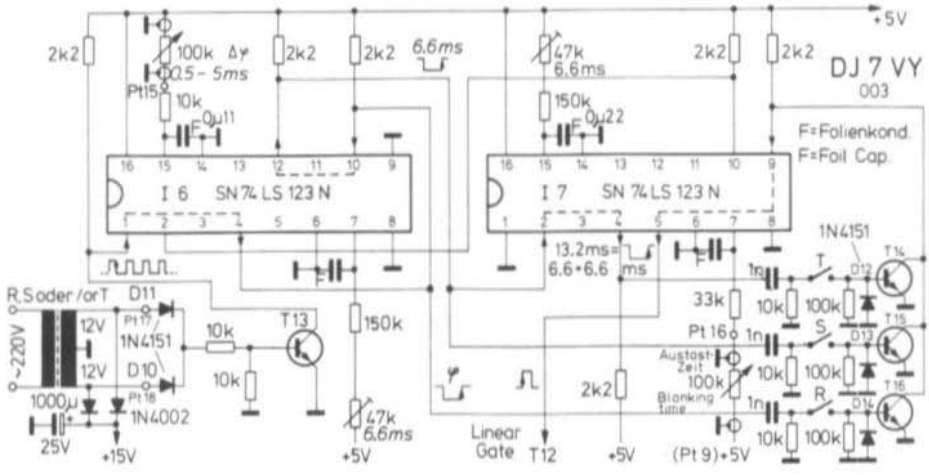


Fig. 11: Corona-trigger accessory

converter drives the RF-trigger circuit, the AF-trigger circuit and the control voltage generator for the control voltage amplifier of the TCA 440 (I 1). The control voltage is amplified by transistor T 17 and by collector rectification so that the IF output voltage is virtually stabilized to 2 V_{pp} + max. 3 dB at input signals between 30 µV and 100 mV. The overall gain between preamplifier input and IF impedance converter output amounts to approximately 100 dB.

According to the spread of the TCA 440 and the Q of inductances L 2 and L 3, it is possible for the gain to be so high that self-oscillation can occur. It is possible using resistor R 3 for the output stage to be dampened to neutralize this tendency. In the case of the author's prototype, R 3 is ∞, even though HIGH-Q coils were used for L 2 and L 3.

During the author's preliminary experiments, it was necessary for R 3 = 18 kΩ to be used, but this was probably because I 1 was mounted in a socket, which no doubts increased its tendency to self-oscillation!

5.3. RF-Triggering

The IF-output signal with a bandwidth of approximately 200 kHz (see winding data for narrower bandwidths) is fed via a capacitor of 100 pF to the base of the PNP transistor T 7 which is biased via diode D 7 (0.7 V). The input current of I 2 produces a voltage drop of 0.4 V across the 1 kΩ resistor, which means that the collector voltage of T 7 amounts to 3.9 V. As soon as the RF-voltage at the base of T 7 exceeds its threshold voltage plus the bias voltage, or if the bias voltage is sufficiently decreased using the RF-trigger threshold potentiometer, the collector voltage of T 7 will increase, the voltage at pin 2 of I 2 will then exceed the TTL-threshold and the retriggerable monoflop I 2 will generate an output pulse. Due to the retrigger characteristics, this impulse will be lengthened in addition to the monotime as long as the RF-interference drives transistor T 7, in other words as long as the trigger threshold is exceeded.

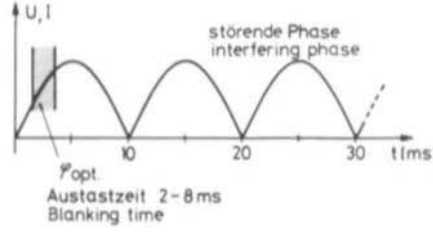


Fig. 11a: Optimum range for the phase position of the blanking time

This means that if the bias voltage is set too low, a continuous triggering of I 2 will

be caused by IF-noise and will cause a permanent blocking of the linear gate !

Transistor T 10 has been inserted between the output of I 2 and the linear gate driver T 3. This transistor together with T 11 and T 12 performes an »OR«-function. Transistor T 3 will be blocked as soon as T 10, T 11, or T 12 switch.

If the RF-interference signal at the output of T 6 is less than the strongest receive signal within the IF-bandwidth, no discrimination of the interference will be possible.

5.4. AF-Triggering

A negative-going AF-signal is generated in the germanium diode D 9. The bandwidth of the AF-signal is limited to 600 Hz in RC-lowpass filter links before the AF-trigger threshold potentiometer, and in the subsequent AF-amplifier comprising T 8 and T 9. The impedance converter T 9 drives I 3 with positive AF-pulses as soon as RF-pulses are present at diode D 9, and when the AF-trigger threshold is sufficiently high.

If the TTL-threshold of 1.6 V is exceeded at pin 1 of I 3, I 3 will start the double-monoflop I 4, whose first half is required for adjustment of the delay time, and its second half for adjustment of the blanking time.

The delay line is designed so that the interfering pulse frequencies between 8 and 200 Hz can be blanked. Other frequency ranges can be included after suitable alteration of the R and C-values. According to the type of interference, the blanking control can be set to an optimum blanking time of between 1 and 20 ms. The scales of both controls can be calibrated linearly with the given values. The output of I 4 drives the »OR« transistor T 11, which in turn blocks T 3, and thus blanks the required-signal path.

5.5. Power Line Triggering

Since a completely integrated power-line network exists in Europe and the phases of all AC-voltages are therefore coherent, it is possible when using power-line triggering to blank any corona-type interference caused by high-tension lines in the short-wave range. However, power line triggering will not be able to compensate for any overlap of the burning times as discussed in section 1. of part 1.

If an anti-phase power-line voltage of between 4 and 25 V is fed to point D and E, transistor T 13 will not produce current during the zero-passes of the voltage which occur at a frequency of 100 Hz. Its collector drives the first half of I 6, which allows a delay time to be set between 0.5 and 5 ms. This allows the blanking threshold to be varied along the rising slope of the sine-wave voltage. The second half of I 6, as well as the first half of I 7 generate the required time delay of 6.6 or 13.2 ms required for the 120° and 240° phase shift in the case of a three-phase network.

This means that needle pulses are present at the output of three monos at the switches R, S and T that are delayed and differentiated with a value of $\Delta\varphi$. After closing the switch, they are able to trigger the second monoflop in I 7 via transistor T 14 to T 16, which allows variable blanking times between 2 and 8 ms to be adjusted. The output of I 7 drives the »OR« transistor T 12, which blocks the linear gate via transistor T 3.

5.6. Signal Delay in the Required-Signal Path

A sufficient signal delay in the required-signal path previous to the linear gate can only be provided by a crystal filter when using the PC-board in the IF-channel of a receiver. This can be achieved as shown in **Figure 7** of part 1. In this case, it may be possible to delete the AF-triggering, since the linear gate will be triggered by the RF-triggering before the pulses appear.

A similar delay line filter using two crystals spaced by ± 8 kHz from the IF was constructed by DL 7 IY for his Atlas 210 X, which exhibited the same characteristics and effects.

It is necessary to change the values of the C 4, C 10, L 8 and Tr 2 when an intermediate frequency of 9 MHz is not used. It is not possible to insert a cable delay line

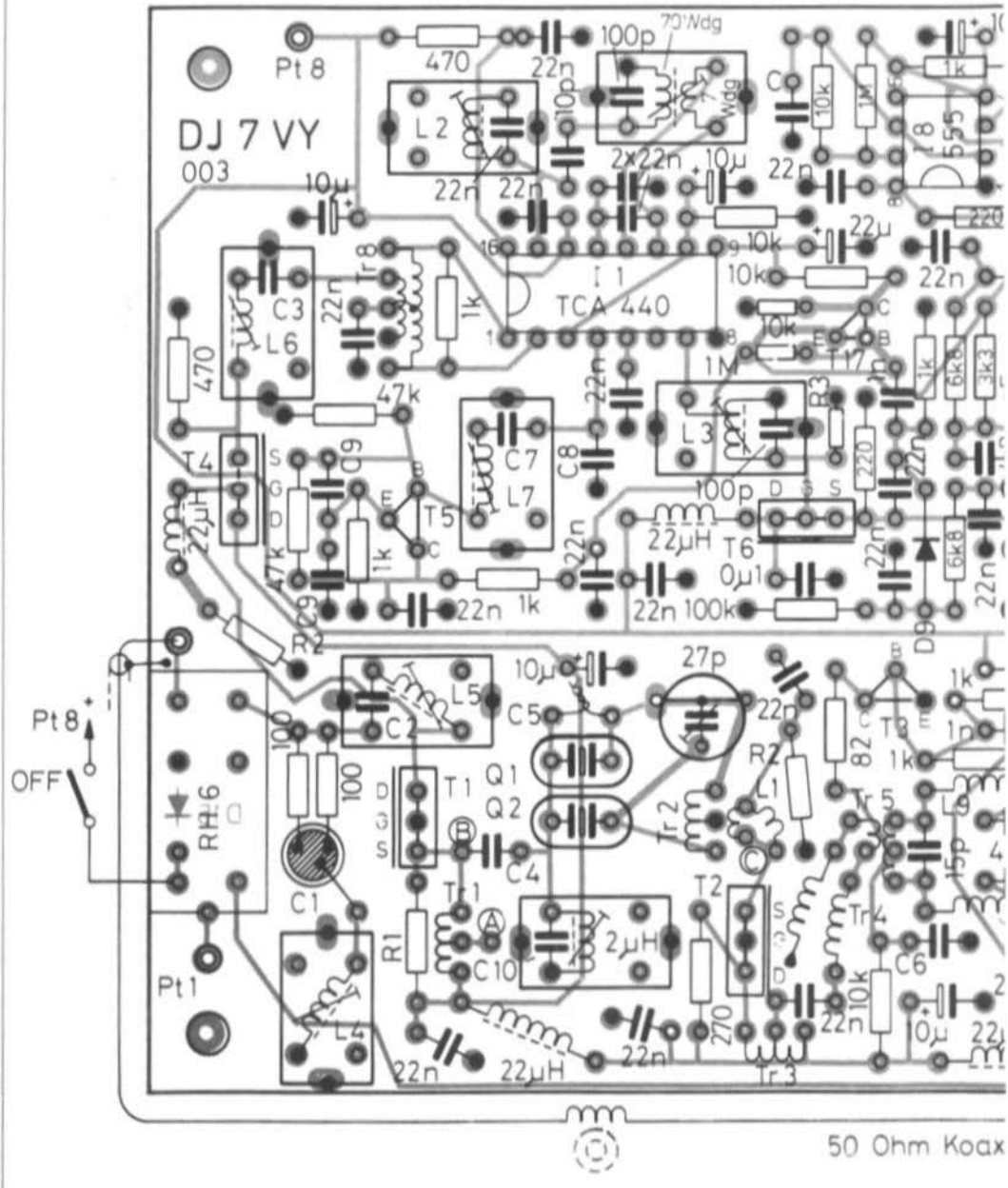
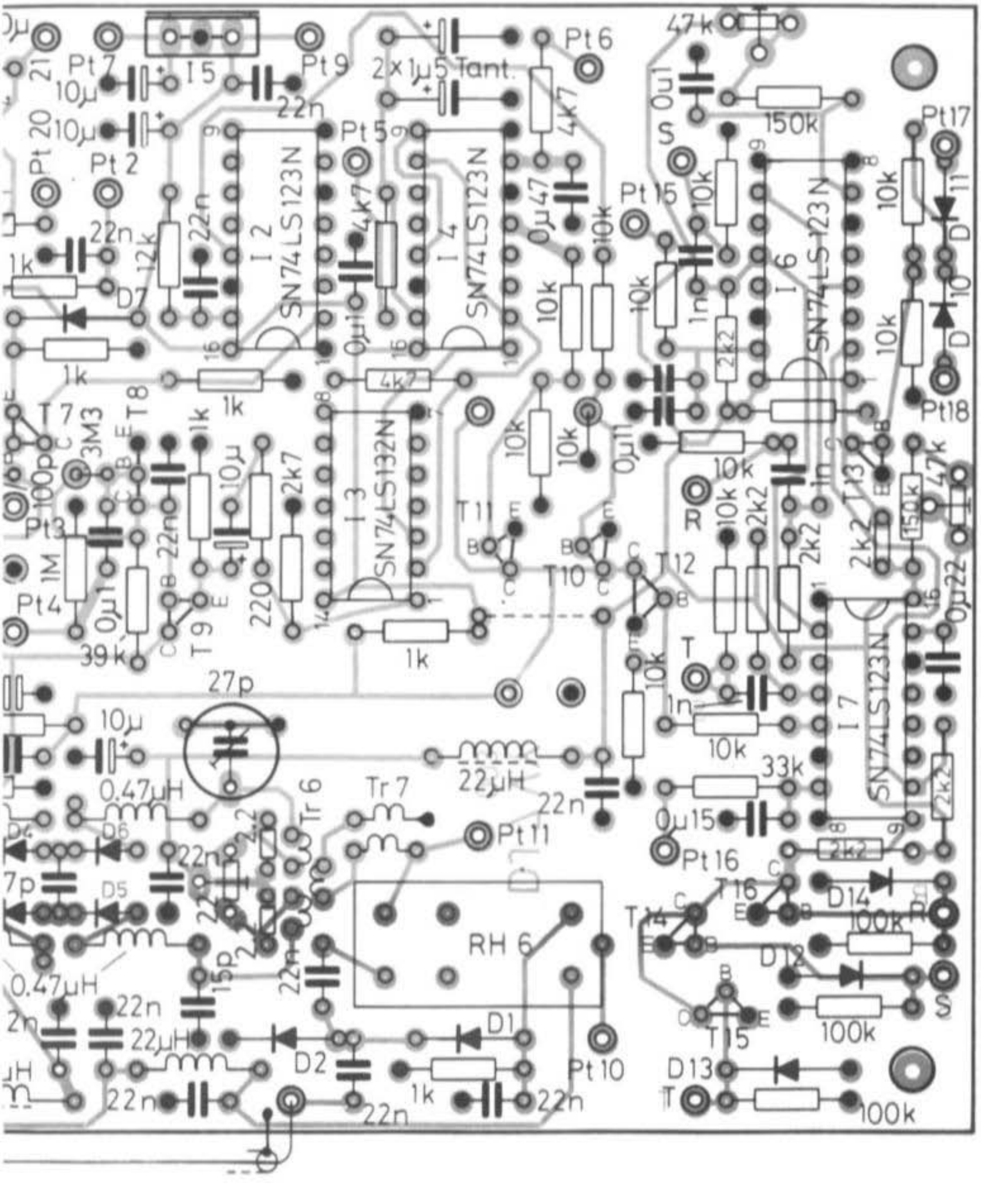


Fig. 12: PC-board DJ 7 VY 003 with through-contacts for accommodation of the noise blanker together with corona-trigger accessory



Pt 7
Pt 9
Pt 6
Pt 20
Pt 2
Pt 5
Pt 15
Pt 17
Pt 18
Pt 3
Pt 4
Pt 11
Pt 16
Pt 10
I 5
I 2
I 4
I 6
I 3
I 7
SN74LS123N
SN74LS132N
2 x 1µ5 Tant.
47k
150k
0µ1
4k7
0µ47
10k
12k
22n
10µ
1k
D7
T 7
T 8
3M3
100p
1M
0µ1
39k
T 9
220
2k7
T 11
T 10
T 12
T 13
0µ11
1n
2k2
0µ22
33k
0µ15
27p
0.47µH
22µH
Tr 6
Tr 7
RH 6
D4
D5
D6
D1
D2
D12
D13
D14
T14
T15
T16
15p
100k
R
S
T

between T 1 and T 2 corresponding to the signal delay in I 1 and I 2, since several kilometers of cable would be required ! The variable delay in I 4 during AF-triggering allows that quasi-periodic interference pulses can be blanked with a phase shift corresponding to its period time.

5.7. Power Supply

If the PC-board is fully equipped, a current of 140 mA will be required at 15 V, and 100 mA at 5 V. This means that the stabilizer 7805 must provide a power dissipation of 10 V x 100 mA = 1 W, and that a suitable heat sink must be provided (rear panel of the case).

6. CONSTRUCTION

A double-coated PC-board DJ 7 VY 003 has been designed for construction of the noise blanker. The dimensions of this board are 90 mm x 120 mm and the component locations are given in **Figure 12**. After manufacturing all inductances and transformers according to the components list and required frequency, the components can be mounted onto the PC-board with the exception of R 2 and C 6. It is important to ensure that the 50 Ω termination at C 1 is soldered into place with short connection leads when the module is to be used as termination for a mixer (Note: The design of a low-noise, varactor-tuned VFO for module DJ 7 VY 002 is under preparation). This termination will not be necessary when used on its own. When used on several bands, it is necessary for the oscillator T 5 and the input filters previous to transistor T 1 and subsequent to T 4 to be made switchable. Since the frequency of the Russian trans-horizon radar is always just below the maximum usable frequency (MUF), this module will mainly be required on the 21 MHz and 14 MHz band.

It is not absolutely necessary for the required-signal or interference signal path to be screened, since sufficient decoupling is provided on the board itself. The cross-talk attenuation amounts to 106 dB in the case of the author's prototype, the blanking attenuation of the linear gate to 88 dB. The insertion loss, when switched off, is 0.12 dB, and the required-signal gain is 4.8 dB (9 MHz, Tr 3 trifilar at 470 Ω).

When using the module as receiver input circuit, it is advisable for it to be constructed together with a power supply in a RF-tight case. The inputs and outputs should be provided with BNC-connectors and measures should be provided on the coaxial cable to block interference currents along the outer conductor of the cable between connector and PC-board.

When using the noise blanking in conjunction with the 144 MHz converter DJ 7 VY 002, a coaxial cable should be fed from the collector of transistor T 11, passed through a toroid core several times for suppression of any RF-current on the sheath of the cable and then connected to the trigger input of the converter. In this case, the components in the signal path of the noise blanker board are deleted. Inductance L 6 of module 002 is connected to Tr 8 of module 003 using a coaxial cable passed several times through a toroid core. Since the converter board does not possess sufficient delay in the signal path, it is mainly AF-triggering that must be used here !

6.1. Special Components

T 1, T 2, T 4, T 6:	P 8000 or P 8002 (TI)
T 3:	2 N 2219 (a) or similar TO 5
T 5:	BF 199, BF 240
T 7, T 17:	BC 415 or similar PNP
T 9 - T 16:	BC 413 or similar NPN
I 1:	TCA 440 (Siemens)
I 2, I 4, I 6, I 7:	74 LS 123 N
I 3:	74 LS 132 N
I 5:	7805
I 8:	NE 555
D 1 - D 7:	1 N 4151
D 9:	AA 118 or similar Germanium diode

Inductances and Filters:

9 MHz crystal filter: 8991.5 kHz (30 pF) and 9008.5 kHz (30 pF) TQ 310312

R 1:	680 Ω
C 4:	68 pF
C 5:	approx. 0.5 pF = 10 mm 0.3 enamelled copper wire wound together

n [turns] = $\sqrt{\frac{L}{0{,}012}}$ (L in µH)

Frequency	C 1 pF	L 4 nH	C 2 pF	L 5 µH	Δf MHz	C 3 pF	L 6 µH	$F_{OSC.}$ MHz	C 7 pF	L 7 µH	C 8 pF	C 9 pF	C 10 pF	L 8 µH	L 9 µH	Turns on L 7
A) When used with converter																
9 MHz	470	665	266	1,2	6,8	47	6	11	68	4,2	1 n	470	150	2	–	19
10,7 MHz	470	470	188	1,2	6,8	39	6	12,7	68	3,2	1 n	470			–	17
14 MHz	470	275	109	1,2	6,8	27	5	16	100	1,5	1 n	470			–	11
29 MHz	470	64	96	1,2	6,8	10	3	31	47	0,9	220	220			0,47	8
B) When used as input circuit																
3,7 MHz	2n2	850	330	5,5		100	19	5,7	33	30	470	470	330	5,5	–	50
7 MHz	1 n	520	100	5,2		47	11	9	100	5	1 n	470	100	5,2	–	25
14 MHz	470	280	68	1,9		22	5,5	16	100	1,5	1 n	470	68	1,9	–	11
21 MHz	330	170	47	1,2		15	3,8	23	100	1	680	220	47	1,2	0,47	8
29 MHz	220	140	33	0,95		10	3	31	47	0,9	220	220	33	0,95	0,47	8

Table 1:
Components for the various operating frequencies
Calculation of inductances using coil sets D 41-2165: A_L approx. 12 nH/w².

When used as an input circuit of a short-wave receiver, it is possible to delete the crystal filter together with R 1 and T 2, L 1 is provided instead of Tr 2, a coupling capacitor of 22 nF is connected from A to C, the value of C 4 will become 22 nF, the value of L 8 and C 10 should be taken from the table.

R 2: for $I_D \approx 35$ mA

C 6: for suppressing the peak, approx. 2.2 nF

L 2: 60 µH = 70 turns 0.15 enamelled copper wire with core in special coil set

L 3: 60 µH = 30 + 40 turns of 0.15 enamelled copper wire + 7 coupling turns at the coil center

The following values are valid for 9 MHz:

L 4: 0.66 µH = 7 turns of 0.3 enamelled copper wire

L 5: 1.2 µH = 10 turns of 0.3 enamelled copper wire

L 6: 6 µH = 24 turns of 0.3 enamelled copper wire

L 7: 4.2 µH = 19 turns of 0.3 enamelled copper wire

L 8: 2 µH = 12 turns of 12 x 0.04 HFL (approximately 5 times the Q of 0.3 mm enamelled copper wire !)

Other operating frequencies are given in the table.

L 9: 0.47 µH = 20 turns of 0.15 enamelled copper wire wound on a 100 kΩ/0.1 W resistor of 2.0 mm dia., coil length 3.5 mm (can be deleted at f < 20 MHz)

Tr 1: 2 x 12 turns of 0.3 mm enamelled copper wire / R 6.3 N 30

Tr 2: 2 x 12 turns of 0.3 mm enamelled copper wire / R 10 K 1 + 3 coupling turns

Tr 3: as Tr 1 (G_p = 2.5 dB) or trifilar 3 x 9 turns/R 6.3 N 30 with R_L 470 Ω (G_p = 4.8 dB)

Tr 4: 6 turns of SM 50 coax. 1 mm dia. on R 6.3 N 30 (or instead of SM 50 it is possible to use 2 x 0.15 enamelled copper wire wound together)

Tr 5: 3 x 9 turns of 0.3 enamelled copper wire / R 6.3 N 30

Tr 6: as Tr 5

Tr 7: as Tr 4

Tr 8: as Tr 1 + 4 coupling turns of 0.3 mm enamelled copper wire

7. ALIGNMENT

An oscilloscope is very advisable for alignment of the noise blanker, but not absolutely necessary. It is only required for the alignment of the delay of I 6 and I 7 (2 times 6.6 ms). A shortwave receiver is suitable for alignment of the linear gate balance. For alignment of the interference channel receiver, one will require a mA-V-meter and a RF-generator, or dipmeter with attenuator. Firstly adjust the quiescent current of T 1 to 35 mA by selection of R 2. This is made by inserting the mA-meter into the drain or source line. Resistor R 2 of T 2 is selected with the aid of the meter so that the quiescent current is in the order of 30 to 45 mA. Inductances L 4, L 5, L 8 and the trimmer of the crystal filter are aligned for maximum S-meter reading on the receiver after injecting an input signal of the required frequency. For aligning the balance of the linear gate, an impulse generator as shown in **Figure 13** is used, which can also be used after completing the board for checking correct operation of the module.

This is followed by connecting pin 3 of I 8 to the collector of T 12 with the aid of a coaxial cable wound several times through a toroid core, and provided with short connections. I 8 should oscillate at a pulse frequency of approximately 100 Hz. This means that the linear gate will be continuously switched on and off and the pulse slopes will be audible in the receiver as clicks.

After providing the switching diodes with silicon heat-conductive paste, so that they possess approximately the same temperature, the receiver noise is adjusted to a minimum with the aid of the 22 Ω and 27 pF trimmers. At lower frequencies, it is better to use an R-alignment, whereas at higher frequencies the C-alignment can be carried out more easily.

After aligning the balance, C 6 is mounted into place after which the remaining »interference« of the receiver is checked. This should only be slightly above the noise threshold of the receiver ! CAUTION: The interference must not be allowed to be fed to the receiver indirectly such as via connections or the power line !

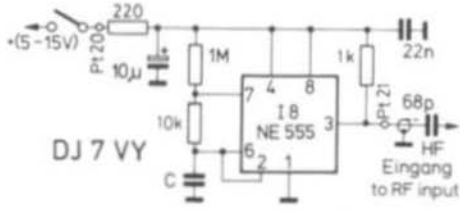


Fig. 13: Interference pulse generator for alignment of the noise blanker

Pulse frequency f	Capacitance C
10 Hz	0.1 µF
100 Hz	10 nF
1 kHz	1 nF

In order to achieve the maximum blanking of the linear gate, a 20 mm long and 0.7 mm thick wire is soldered both to the anode of D 6 and the cathode of D 3 and bent horizontally so that they both run parallel for approximately 15 mm at a spacing of 1 mm.

A 100 mV signal is now injected into the input, whilst observing the S-meter of the receiver. If the base of T 3 is grounded, the output signal should be reduced by approximately 80 dB. It is possible by bending the wires (C ≈ 0.4 to 0.7 pF) to increase the blanking value to more than 90 dB ! Attention must be paid, however, that the generator signal is not able to bypass the linear gate, in other words, both generator and receiver should be RF-tight ! This alignment can also be carried out in conjunction with a strong shortwave-broadcasting signal.

For alignment of the interference channel receiver, a 2 MHz signal is injected to the TCA 440 via a coupling winding on transformer Tr 8. After connecting a voltmeter to pin 9, it is possible for the IF-amplifier with its three resonant circuits to be aligned for maximum reading. The balance of the passband curve is checked by tuning the generator to both sides of the center frequency. After this, the center frequency (9 MHz) is fed to the input of the noise blanker and the oscillator comprising L 7 is aligned at its operating frequeny of 2 MHz above the generator frequency. It is now possible for L 6 to be aligned for maximum control voltage, with the generator signal, if possible, set to < 1 mV.

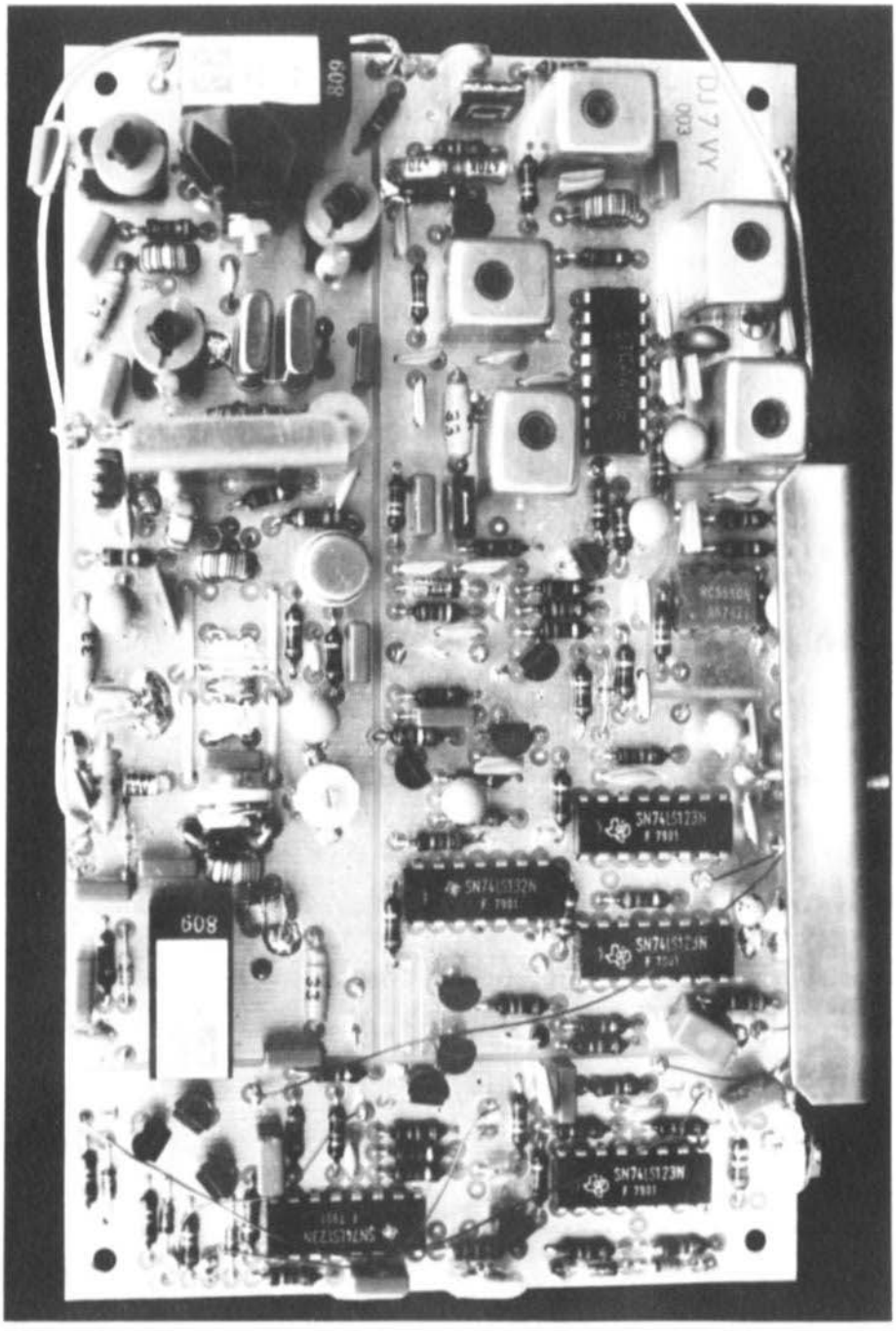


Fig. 14: Author's prototype of the noise blanker including corona-trigger accessory

The alignment of the AF-triggering requires the connection of an oscilloscope to the outputs of I 6 and I 8 and triggering by the previous pulse slope. The output pulses at pin 12 of I 6 and at pin 4 of I 7 should both be aligned to 6.6 ms.

8. OPERATION

For checking operation of the unit, the interference pulse generator with a frequency of approximately 50 Hz is connected via 68 pF to the input of the noise blanker. The capacitor should be directly located at the input socket, and the coaxial cable between it and the NE 555 should be provided with an AF trap (toroid core) and grounded at both ends. In the case of AF-triggering, a complete suppression of the injected interference can be achieved at a delay time of approx. 20 ms and a minimum blanking time of 1 ms. By actuating the RF-trigger threshold, it is also possible to suppress the interference pulses in the IF-version of this module. In the case of very strong interference pulses, an RF-triggering will even occur with the RF-trigger potentiometer turned right down. The triggering point will vary along the pulse slope on actuating the potentiometer (see Fig. 4 d), which allows the residual peak to be reduced. If a radar interference occurs when using the module as an input stage of a shortwave receiver, it is necessary to use AF-triggering without delay filter. In this case, the delay potentiometer should be adjusted to approximately the period of the radar signal, the blanking time to the radar pulse length; in the case of SHF radar interference as shown in Fig. 1 g: to approx. 1.9 ms, and 200 µs. The capacitance values of the monos should be changed correspondingly. It will be seen that the delay time can be set more accurately the lower the blanking time overlaps the interference time. If the overlapping is too great, it can occur easily that too much of the required signal is blanked !

A delay time of approximately 90 ms at a blanking time of 20 ms has been found to be optimum in conjunction with shortwave radar interference. It is possible by making alternate adjustments for the interference pulse length to be established. If only RF-triggering is used, the interference signal will be reduced as shown in Fig. 4 f to a residual amount, which may be sufficient. A complete suppression can be made when the residual pulse length variation caused by altering the threshold shifts the zero positions in the interference spectrum (Fig. 1 g) to the receive frequency, and when the center frequency of the radar is several 100 kHz adjacent to this.

Since all signals that are being blanked are modulated up to 100 % with the blanking frequency, this will mean that AM-stations can only be demodulated with a product detector, otherwise a large degree of distortion will be present. The larger the blanking time, the greater the modulation is made on SSB and CW signals, however, this is acceptable because these signals would otherwise probably be inaudible anyway !

9. IMPROVEMENTS

In order to simplify the adjustment of the AF-triggering, it is possible to use an adapted circuit in order to achieve the time processes automatically (10). The same can also be carried out in a digital manner, if the time between two interference pulses is measured in a counter an decreased by a constant amount of time. This means that when two such circuits were used 180° out of phase, it will be possible to obtain a complete interference suppression even over large interference-pulse repetition frequency ranges. Additionally, it will be possible for the interference pulse length to be digitally measured and for the linear gate to be set automatically to the optimum (minimum) blanking period. However, this would then become somewhat too extensive !

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Automatic Frequency Control and Suppression of Acoustic Feedback in Conjunction with 10 GHz Transceivers

by Dr. Manfred Wieser, OE 7 WMI

Two disadvantages have been found in practical operation of 10 GHz transceivers (1) and (2):

1. THE INFERIOR SHORT-TERM STABILITY OF THE FREE-RUNNING GUNN OSCILLATORS

The frequency drift can be so high that it runs out of the IF-bandwidth of the receiver, especially during bad weather conditions.

2. THE ACOUSTIC FEEDBACK BETWEEN MICROPHONE AND LOUDSPEAKER DURING DUPLEX OPERATION

Duplex operation is one of the major advantages of microwave communications, which means to do without this, or to only use hedsets would be a great disadvantage.

This article is to describe a module that provides both an automatic frequency control for the Gunn oscillator, and a circuit for suppressing acoustic feedback (basically an attenuator).

The circuit operates as follows:

According to (3), the dependence of the oscillator frequency of a Gunn oscillator on the supply voltage amounts to 0 to 20 MHz/V depending on the operating point and on the Q of the resonator. If the operating point is placed on the rising slope of the characteristic **(Fig. 1)**, one will receive a virtual linear frequency variation of ± 5 MHz on varying the operating voltage by ± 0.5 V when using a conventional construction of the Gunn oscillator (1) and (2). If this possibility is used for modulation, it is possible by inducing the AFC voltage from the receiver to form a frequency control loop with a considerably higher short-term stability.

In the duplex mode, it is not only the signal of the partner station that is converted down to IF-level, but also one's own signal. According to whether the signal is above or below the IF-frequency, the demodulated AF-signal will be of identical or opposite phase to one's own modulation. In both

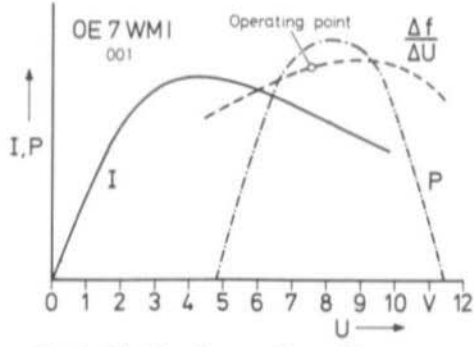

Fig. 1: Selecting the operating point of the Gunn oscillator

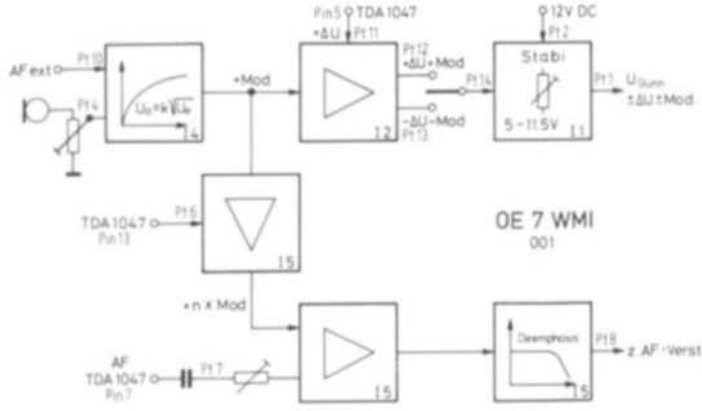

Fig. 2:
Block diagram of the overall system

cases, the (variable) phase-shifts in the acoustic path will cause a feedback between loudspeaker and microphone in both cases (even at low-volume levels) and this will be audible as a pumping or whistling tone.

If, on the other hand, the demodulated AF-signal is mixed with the amplified, anti-phase modulation signal, these signals will theoretically cancel each other out, so that no acoustic feedback can occur. In practice, values of between 25 and 30 dB can be obtained using the described method, especially in the range between 1 and 4 kHz. When varying the conversion from one side to the other, it is necessary for the phase position of the added signal to be also reversed, in the same manner as the AFC-signal must be inverted. For this reason, it seems advisable for the modulation and AFC to be passed through the same signal path (inverting) which is shown in **Figure 2**.

CIRCUIT

The design of the circuit given in **Figure 3** is based on the possibilities offered by the integrated IF amplifier/demodulator TDA 1047. The FET T 4 forms the input stage of the modulator amplifier, and has the advantage that both high and low impedance microphones can be used. The amplified microphone signal is fed to the input of the integrated circuit I 4 that is used as compressor. It is possible at this position for signals from other sources to be added via connection Pt 10.

The compressor has – in contrast to the usual dynamic compressors and clippers used in amateur radio technology – a relationship of: $U_{out} = k \times \sqrt{U_{in}}$ between output and input voltage.

The constant k is determined by resistor R 18 in this circuit, and R 19 will determine the behaviour of the IC at low input voltages. The given values have been found to be most favorable in several experiments. The use of the compressor ensures that no overmodulation will occur even at high sound levels.

A well-proved circuit comprising an integrated circuit type NE 555 was used for calling-tone generator.

The operational amplifiers in the integrated circuit I 2 provide the combination of modulation and AFC, as well as their inversion. The AFC-voltage from pin 5 of the TDA 1047 is connected to connection Pt 11. The AFC-output of the TDA 1047 is a push-pull current output and can be connected to any voltage within the operating voltage range; in our case it is connected to + 5 V from the power supply of the Gunn diode.

Resistors R 7 and R 8 determine the AFC-deviation, and thus the hold range. The value of these two resistors depends on the slope of the characteristic, which was discussed previously. Values of between 10 kΩ and 100 kΩ have been found suitable for various elements.

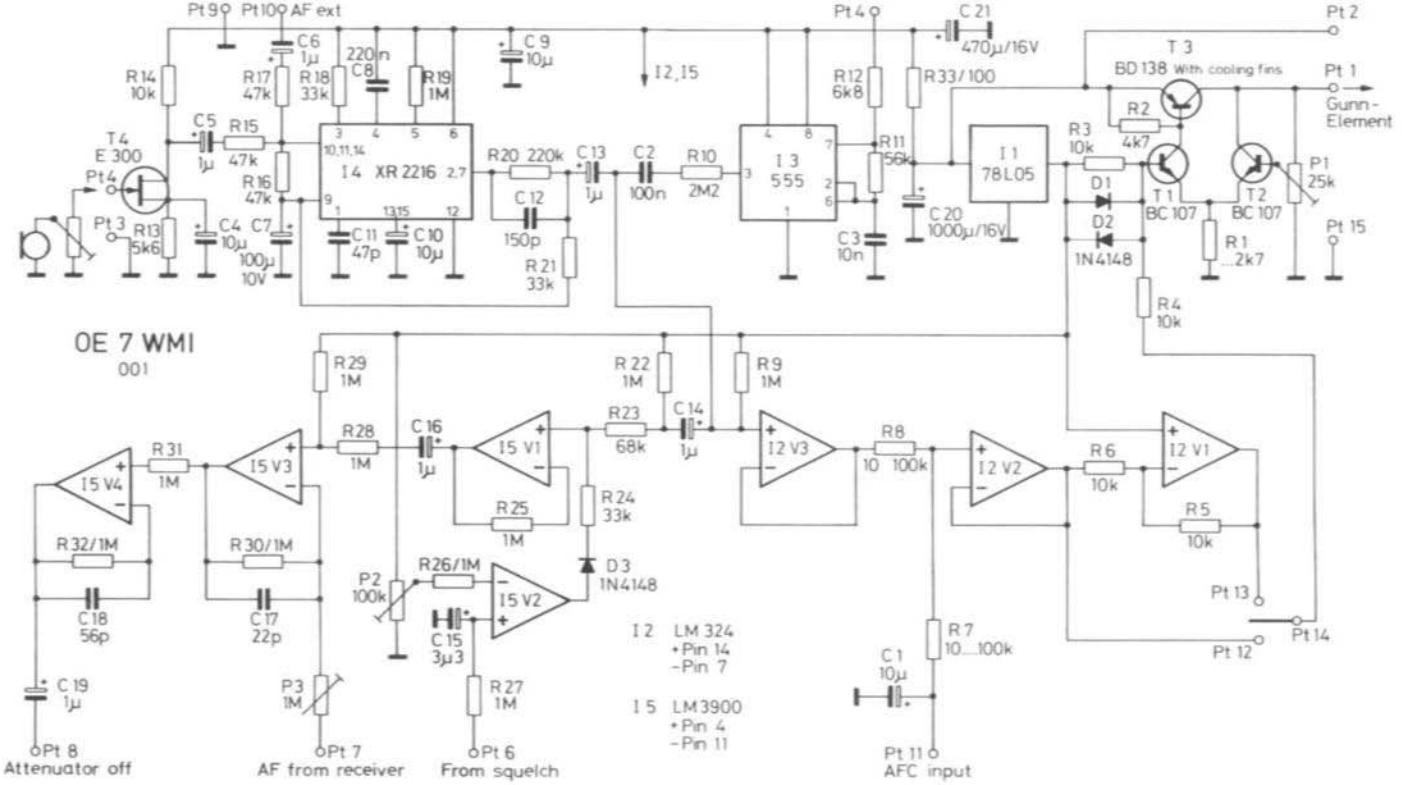

Fig. 3: AFC und suppression of the acoustic feedback in conjunction with Gunn transceivers

The voltage supply of the Gunn diode is a simple circuit equipped with a voltage stabilizer and three transistors. Its advantage is that the lowest possible voltage drop across the pass transistor only amounts to 0.5 V ! The stability of the voltage is less than would be possible with integrated stabilizers (78..), however, the advantage of the AFC is considerable.

A current limiting is provided by resistor R 1. The value is dependent on the current gain of transistors T 1 to T 3.

The four differential current amplifiers of the integrated circuit I 5 form the »attenuator«. The modulation signal is increased in amplifier 1 to approximately the value of the demodulated AF (pin 7 of TDA 1047).

Amplifier 3 forms the subtractor, and potentiometer P 3 can be used to adjust for equal amplitude. Amplifier 4 is used for decoupling and deemphasis.

When not in communication, and thus when one's own modulation signal is not present in the IF-amplifier, feedback would still take place. In order to ensure that this does not happen, amplifier 2 switches off the modulation signal when no signal is present (squelch circuit voltage, pin 13 of the TDA 1047).

A small, single-coated PC-board was designed for accommodation of the circuit given in **Figure 3**. The component locations of the PC-board are given in **Figure 4**. **Figure 5** shows the photograph of the author's prototype.

CONNECTION AND ALIGNMENT

Firstly connect the operating voltage to Pt 2 and Pt 15 (ground). The operating voltage should be adjusted to the correct operating point with the aid of P 1. Resistor R 1 should be adjusted to three to four times the value of the current at the operating point, so that the characteristic is swept quickly.

Check to see whether 5 V is present at Pt 12 and Pt 13, after which the Gunn element can be connected. Connect the microphone to Pt 4 and Pt 5 (galvanic connection is required !); the rest of the alignment is only possible together with a partner station.

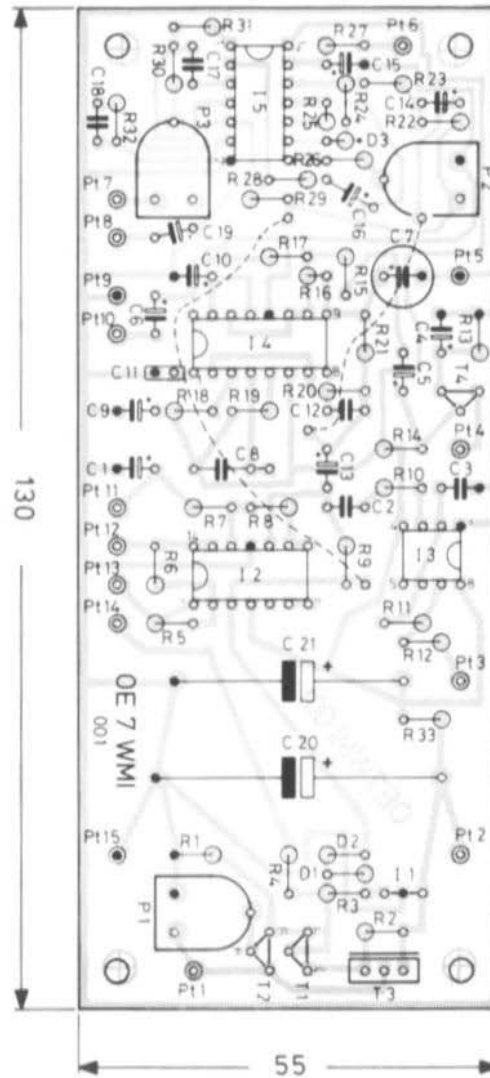

Fig. 4: PC-board OE 7 WMI 001

Connect Pt 3 to the operating voltage after which a calling tone of approximately 1 kHz should be audible. If the frequency deviation of the calling tone is too great, increase the value of R 10. Check to see whether the AFC locks in according to the position of the upper/lower conversion switch with R 7 and R 8 10 kΩ, otherwise increase the values up to a maximum of 100 kΩ. The hold range must always be 10

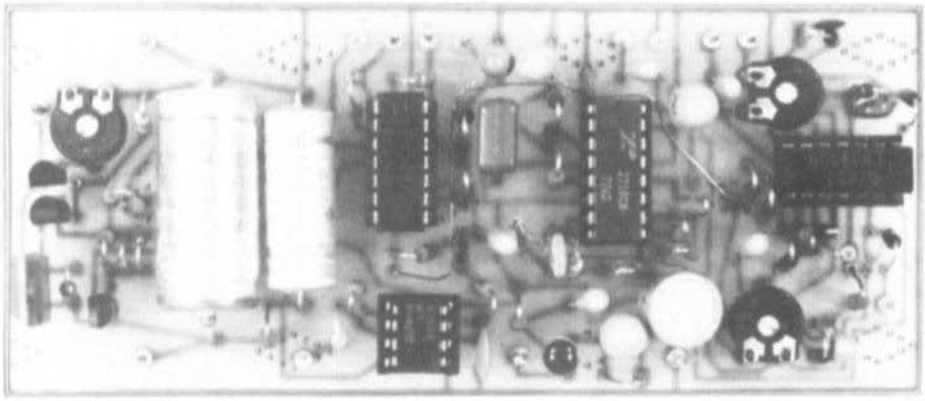

Fig. 5: Photograph of the author's prototype. The single-coated board requires two bridges

to 20 times greater than without AFC ! Place P 2 to maximum (5 V) and feed AF from the IF-amplifier to Pt 7, and from Pt 8 back to the loudspeaker amplifier. CAUTION: Both points carry DC-voltages !

When the AFC is locked in correctly, it is possible by varying potentiometer P 3 to hear a minimum of one's own volume. An exact alignment is possible by using an AF-generator set to 2.5 kHz (Pt 10 and Pt 9) and an AF-millivoltmeter or oscilloscope (Pt 8). It is possible to measure the suppression by comparing the measured values with P 2 open (0 V) and P 2 at 5 V; it should be more than 20 dB. Values of 30 dB were measured with several prototypes !

Finally, connection Pt 6 is connected to the squelch output (pin 13) of the TDA 1047, and the threshold for the attenuator is selected with P 2.

MEASURED VALUES

Current drain of the whole module (only operating voltage connected): 19 mA

AF-generator to Pt 9 and Pt 10:
AC-voltages (RMS):
Input voltage: 215 mV, 1 kHz, sinusoidal

Voltage at Pt 14:	12 mV
Voltage at Pt 1:	15 mV

From IF-module, pin 7:

Voltage at Pt 7:	230 mV

Without attenuator,

Voltage at Pt 8:	260 mV

With attenuator,

Voltage at Pt 8:	13 mV
(difference is 26 dB)	

DC-voltages:

Pt 12, Pt 13 with open AFC-input:	5 V
Pt 1:	5 V up to U_B – 0.5 V
I 4, pin 9:	$U_B/2$
T 4, source:	approx. 2 V
T 4, drain:	approx. 8 V
I 5, V 3 output, V 4 output:	5 V

Calling tone: approx. 1 kHz square wave, 30 mV (peak-to-peak) at Pt 14.

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Radio Society of Great Britain

A Microcomputer for Amateur Applications

Part 2: The Central Processing Unit

by W. Kurz, DK 2 RY

1. CENTRAL PROCESSING UNIT

1.1. Introduction

Part 1 of this article contained a general description of the microcomputer system as well as briefly mentioning the individual modules. Part 2 of this article is to describe the central processing unit (CPU). A CPU type Z 80 manufactured by ZILOG was selected for our application. The reasons for selecting this type are to be mentioned later. It is necessary to describe the CPU before discussing the circuit. For those readers that are not interested in the technicalities, and only wish to construct and operate the system, they can do this by leaving out section 1.2.

1.2. The Central Processing Unit – The »Brain« of the Computer

The central processor takes over a large amount of the given activities and is the actual microprocessor. The technical intelligence is concentrated here. The basic units given in **Figure 2** are required for this, which is shown in the form of a block diagram of the microprocessor Z 80-CPU.

Register Block **(Figure 3)**:
This consists of a number of memory cells into which the intermediate results and other information are filed, and can be fetched by the rest of the processor in the shortest possible time.

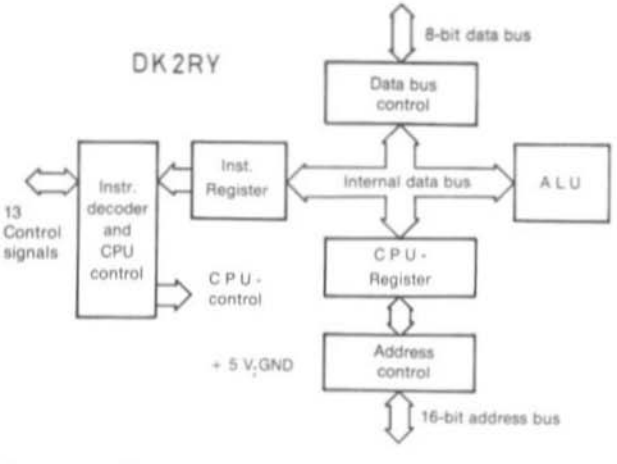


Fig. 2: Block diagram of a 8-bit microprocessor

The user program can also fetch information from a number of these registers, others are reserved exclusively for internal use.

Computer:

This is also called the arithmic/logic unit ALU. This unit executes arithmic (addition and subtraction) and logic (logic AND, OR, EXCLUSIVE OR) operations on which all calculations and decisions of the processor are based. The computer register or registers in which arithmic/logic operations are executed, are called accumulators.

Control Unit:

This is the control center of the central processor. The loaded machine codes are decoded with the aid of a ROM of the integrated hardware of the central processor (so-called microprogram), and thus converted into the actual functions.

This includes the »routing« for the internal data transfer of the processor, the determination of internal processes, the testing of the actual conditions present, which are stored in a special register, the determination of the function to be executed by the computer at that time, and the sequence of the program counter, and the address of the instruction being mapped.

Flag-bits »flags« are used for the previously mentioned condition testing. These are stored in one or more registers. These »flags« are activated by certain instructions and they are set to logic 0 or 1 according to the result of the corresponding order.

This means that a »zero-bit« will result, that will always be logic 1, if the result of the last operation was zero, and logic 0, if the result of the last operation was not zero. The state of these flags thus gives information regarding the results appearing previously in the program, and allows various different activities to be carried out according to the result.

Finally, the CPU requires the two following aids:

- The clock generator, which synchronizes all processes within the computer system. All available microcomputers are »synchronous-machines«, which means that the next activity at gate level will not be commenced by the end of the previous process, but by a certain time sequence determined by the timing of the system.
- The system bus, which comprises the address bus, data bus and control bus.

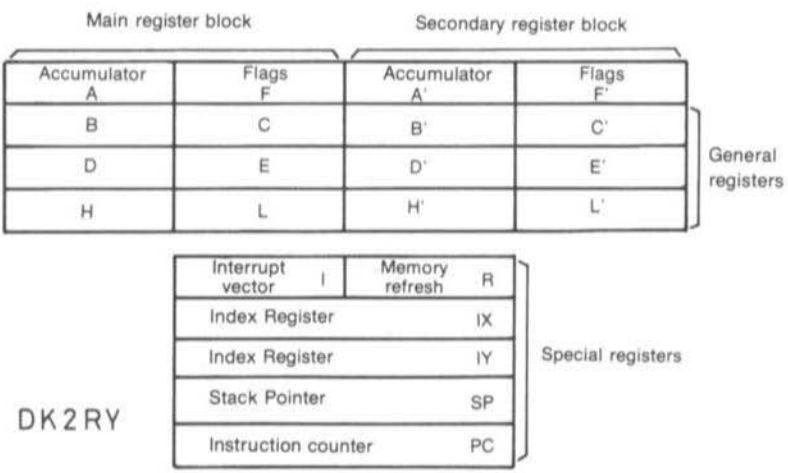


Fig. 3: Schematic display of the register

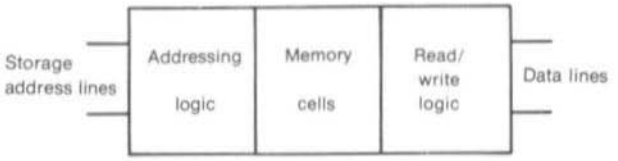


Fig. 4:
Schematic display of the storage (In the case of fixed-value storages only a read-logic is provided instead of the read-write-logic)

The system bus transmits all address and control information to the address and control busses, as well as the machine codes of the orders to be carried out, and the appropriate data to the data bus between microproccesor and the other microcomputer units. These busses are unidirectional, if the information is only to be passed in one direction, or bidirectional, as in the case with the data bus. In this case, the CPU reads information from a write/read memory, or it passes data to it. If such a central processing unit is connected as shown in Figure 2, with the input/output, decoder and driver units, the resulting computer can process a large number of activities that are given in the form of a »user program«, which determine the function of the system.

1.2.1. Order Processing of the Central Processing Unit

The previous section had discussed the basic construction of the central processor. The following is to show how the hardware of the central processor unit processes the orders. A detailed display of the register is given in **Figure 3**; it contains a total of 208 bits accessible to the user, which can be read or written **(Figure 4)**.

Two blocks of these are built up identically, each containing 6 channel registers that allow either 8 or 16-bit operations to be executed. Two accumulators and flag registers are also provided.

The operations of the CPU are run in one of the two register/accumulator blocks; the access to the second register/accumulator block is executed by exchange instructions. This alternative operation allows alternate processing in the main and secondary program without having to transfer the information stored in the register into the memory.

In the program to be used later, the second register is used for the real-time clock.

These registers are the short-time memory of the CPU, whereas the larger amounts of data (and of course also the whole user program) are stored in separate memory units so that it is possible to address both the register and the memory units.

Since all orders are to be found in external memory units, each instruction cycle is made according to the same principle, and in the form shown in **Figure 5**.

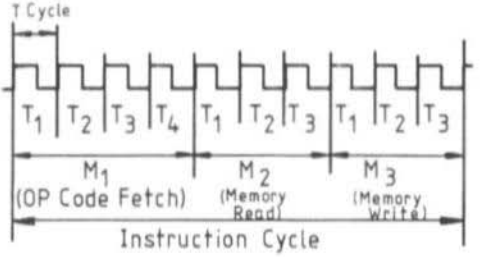


Fig. 5: Display of an instruction cycle

It will be seen that the following sequence exists:

Instruction cycle:

Time required for carrying out an order or instruction; this consists of:

Machine cycles:

The number of machine cycles per order is given by the characteristics of the individual order. Each machine cycle consists, in turn, of several

Clock cycles:

The duration of the clock cycles is given by the frequency of the clock generator. The clock cycle time of the Z 80-CPU amounts to 1.6 µs (≙ 2.5 MHz), and 1 µs (≙ 4 MHz).

The length of a machine cycle amounts to between three and six clock cycles; if the

length of a machine cycle (e.g. of M 1, with which the order code is read out from the program memory) is too short for the memory unit used at the maximum permissible speed, it is possible for it to be extended by inserting an additional clock cycle via the $\overline{\text{WAIT}}$-input of the CPU.

If a machine cycle M 1 takes place, the code of the following order is read into the CPU from the program memory and decoded. Since the individual instructions consist of a differing number of bytes and address fields of different lengths (0 to 2 bytes), this results in a total order length of max. 4 bytes. Since each individual instruction byte must be loaded into the CPU from the memory, this will, of course, also result in different lengths of the M 1-cycle (4 - 6 clock cycles).

It should be noted that not only is the Op-code read during the M 1 cycle, but also the internal decoding within the CPU. During this time, the CPU is not in contact with the busses, which means that other processes such as DMA and refresh can be executed.

Since only $2^8 = 256$ different Op-codes can be handled within one byte = 8 bit, machines with extensive order sets such as the Z 80-CPU (over 600 Op-codes) require 2 bytes for processing the Op-code.

0 byte:	No operator in the address field
1 byte:	8-bit operator in the address field
2 byte:	16-bit operator in the address field

The machine cycles M 2 and M 3 subsequent to M 1 are used for the data transfer between the central processor and the memory or input/output units.

The sequence of an instruction cycle will be seen in **Figure 6**. It will be seen that this results in a certain basic behaviour sequence of the system, but jumps are possible by altering the contents of the order counters.

Which activities that are executed by the central processor after reading in an order (M 2 and M 3) are dependent on the Op-code, or from its decoding by the CPU:

- **Byte transfer instructions**

  Information is transferred between the internal registers of the CPU, or between the registers of the CPU and external memory cells. All these orders contain an origin and destination address; the contents of the origin address is never changed.

  Example: LD C, B copies the contents of register B into register C, without changing the contents of B.

  This includes also direct loading orders that load the constants in a register or in a memory cell, as well as instructions to exchange the contents of two registers.

- **Block transfer instructions**

  A special feature of the Z 80 CPU microprocessor is its capability of transmitting a complete data block of any length after receiving a single order. Since data packets of varying length must be transferred in virtually any application, this type of order saves a considerable amount of storage (at a block length of n-byte, the transfer order does not need to be stored n-times, but only once), and only requires an order processing time in the order of 8.4 µs/byte.

  It is also possible to search for a term in a data block of any length with the aid of one single order.

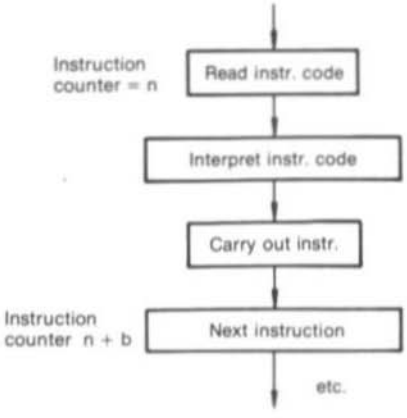


Fig. 6: Flow diagram of an instruction

- **Arithmic/logic instructions:**

  These operate with data words that are loaded into the CPU registers or external memory units. In this case (with the exception of increment and decrement instructions) the result of the operation is taken from the accumulator and set into flags corresponding to the value of the result.

  An example for this is the addition of a memory position to the contents of an accumulator. After addition, the result is loaded into the accumulator. Both 8-bit instructions and 16-bit addition and subtraction instructions belong to this type.

- **Bit manipulation instructions:**

  These instructions allow any Bit in an accumulator, a common register, or a cell of the memory to be set (value = 1), reset (value = 0), or for the contents to be tested, using a single order.

- **Branching instructions:**

  This comprises jumping instructions, instructions for extraction of subprograms and instructions for the return from the subprograms to the main program.

- **Input/Output instructions:**

  These arrange the data transfer between the memory units or CPU-registers. They place the status flags into the appropriate states so that it is not necessary, for instance, to test the parity of its own operations.

  By the way, the Z 80-CPU can carry out block inputs/outputs with a length up to 256 bytes with the aid of a single order.

- **CPU-control instructions:**

  These give the CPU the required operating mode.

STATUS FLAGS

Z 80-CPU possesses two status flag registers that are able to provide information regarding the type of result of the last processor operations. This information is mainly used in order to execute certain jumps, which means that one or another action is executed according to the result of the check. This branching is executed with the aid of so-called jump-orders. These can be either relative or absolute jumps in the case of the Z 80-system.

The position of the individual operating bits within the flag register is given as follows:

7	6	5	4	3	2	1	0
S	Z	X	H	X	P/V	N	C

Where:

C :	Carry Flag
N :	Add/Subtract Flag
P/V :	Parity/Overflow Flag
H :	Half-Carry Flag
Z :	Zero Flag
S :	Sign Flag
X :	not used

The two status bit registers of the Z 80-CPU therefore contain 6-bit status information that are set to 0 or 1 according to the result of the previous CPU activity; the flags in position 3 and 5 of the status flag register remain unused.

Four of the given flags can also be used for checking certain jumps, return instructions, or certain sub-program instructions. These are the flags C, P/V, Z and S. The two flags H and N are used internally for the processing of BCD-operations and cannot be used directly by the programmer. The individual status bits are now to be discussed in more detail.

THE CARRY-FLAG C

The setting or re-setting of the carry-flag is handled differently according to the type of operation to be executed. The carry-flag is set in the case of addition instructions by which an overflow is made, and with subtraction instructions by which no negative overflow is made.

The carry-flag is reset in the case of addition instructions that result in a negative overflow. This aid allows programs to be written easily that are to be made with arithmic operations with word lengths of more than one byte.

In addition to this, the carry-flag is used to show that the conditions for executing the

decimal conversions are given in the case of BCD or 4-bit operations.

In the case of the rotation orders RLA, RRA, RLS, and RRS, the carry-bit is used as intermediate storage for the transfer of the lowest order and highest order bit for any one of the CPU-register or memory positions. With the orders RLCA, RLCs and SLAs, the carry-flag will contain the value of the highest order bit (bit 7) of the register or addressed memory, which has been shifted.

When running a RRCA, RRCs, SRAs and SRLs instruction the carry-bit will receive the last byte from the lowest order bit of the addressed register or memory position.

The carry-flag is always reset in the case of the logic orders ANDs, ORs and XORs.

The carry-flag can be directly set and complemented using the specific orders for this SCF (Set-Carry-Flag) and CCF (Complement-Carry-Flag).

ADDITION AND SUBTRACTION FLAG (N)

This is used on executing the decimal conversion of the accumulator (DAA) to select between addition and subtraction orders. N is reset in the case of all addition orders, whereas 1 is set in the case of subtraction.

PARITY/CARRY-FLAG (P/V)

This flag is used in different ways according to the loaded instruction. When running arithmic operations, this flag will indicate an overflow as soon as the result in the accumulator is greater than the maximum permissible positive number (+ 127), or less than the highest permissible negative number (– 128). It is possible by testing the sign flags of the two operands to establish which of the two mentioned cases is valid:

During addition of operands with differing signs, it is naturally not possible for any overflow to be made. The carry-flag is set as soon as operands of the same sign are added and the result is an opposite sign.

HALF-BYTE CARRY-FLAG (H)

This flag is set or reset according to the carry result between bits 3 and 4 of any 8-bit arithmic operation. This flag is used when an instruction for BCD-conversion (DAA) in the accumulator takes place to correct the result of a packed BCD-addition or subtraction. The H-flag is set, or reset, according to the following table:

H	Addition	Subtraction
1	No carry from bit 3 to bit 4	No negative carry from bit 4
0	No carry from bit 3 to bit 4	A negative carry from bit 4

THE ZERO-FLAG (Z)

The zero-flag is set or reset in the case of a number of instructions corresponding to the result of the operation in question.

In the case of 8-bit arithmic and logic operations, the zero flag is set to 1 if the resulting byte of the accumulator is 0. If the result is not 0, the zero-flag will be set to the value of logic 0.

In the case of comparison and search commands, the zero-flag is set to 1 as soon as the comparison between the value to be found in the accumulator and the storage position that is addressed by the contents of the register pair HL, is positive.

When testing a bit in a register or a storage position, the zero-flag will transfer the complementary value of this bit position.

When transferring a byte between a storage position and an input/output interface (INI, IND, OUTI and OUTD), the zero-flag is set as soon as the value of the counter register (register B) is 0. In addition, the zero-flag is set to 1, when an inputed byte has the valency »0« in the case of order IN_r (C).

SIGN-FLAG

In the case of the sign-flag (S), the highest order bit of the accumulator contents is copied in conjunction with certain instructions. When executing arithmic orders with signed numbers, the binary two-component display is used. A positive number is identified by a »0« in the highest valency bit of a byte (bit 7), and a negative number by a »– 1« in this bit position.

1.2.2. Stack Memory

The contents of the CPU registers are transferred to the stack memory (Stack) when these registers are required for other functions. If, for instance, a subprogram (subroutine) is executed, the last address is transferred to the stack.

After return from the subprogram, this address is copied from the stack and incremented by 1; it is now possible for the main program to continue. The stack is organized in the normal data memory and is addressed using the so-called stack pointer. The stack pointer is a 16-bit register that is integrated in the CPU. After switching on the CPU, this stack pointer is loaded by the initializing program. If a 16-bit information is to be transferred to the stack, this is achieved by firstly loading the highest order part of the 16-bit word to the stack addressed by the stack pointer. After this, the stack pointer is decremented, and the lowest order part loaded correspondingly. The stack pointer is then decremented once again. The extraction of these data from the stack is made in the opposite manner.

1.2.3. The Z 80-CPU

The Z 80-CPU is based on the 8008 and 8080 types and is compatible to type 8085 which is somewhat further developed hardware-wise. However, the Z 80-CPU offers the user software-wise or architectually several considerable advantages. The most important features are to be mentioned briefly:

- 1-chip microprocessor in n-type silicon-gate technology
- The instruction set comprises 158 instructions, including all 78 8080-instructions (the software is fully compatible). In addition to the orders of the 8080, the Z 80 also has a large number of 16, 8, 4, and individual-bit instructions and additional addressing instructions (indicated, relative, and bit addressing)
- 17 internal registers
- 3 interrupt methods and an additional fast, non-maskable interrupt
- Direct connection of dynamic or static standard memory chips without additional components.
- Included refresh-controllers for dynamic memory units
- Instruction processing duration: minimum 1 microsecond
- Only one operating voltage of 5 V is required
- 5 V single-phase clock
- All connections are TTL-compatible

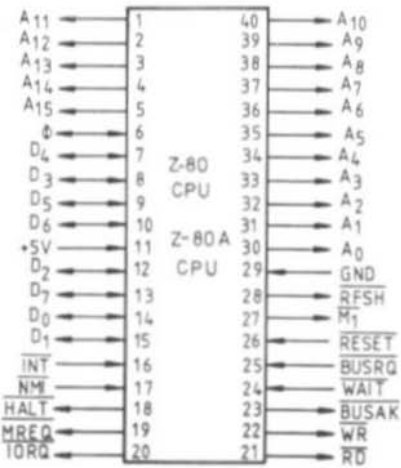


Fig. 7: Pin-connections of the Z 80-CPU

Connections of the CPU

The pin connections of the CPU are given schematically in **Figure 7**. The following is to describe the function of the individual connections:

Pin	Signal	Function	Commentary
1 - 5 30 - 40	A0-A15	Address Bus	Tri-state outputs, high-active. Provides the addresses for the memory (up to 64 kByte) and the input/output units.
7 - 10 12 - 15	D0-D7	Data Bus	Tri-state inputs/outputs (bi-directional), high-active. The data transfer between the CPU and the memory, or CPU and input/output units is made via data bus.
27	$\overline{M1}$	Machine Cycle 1	Output, low-active. M 1 = active means that the momentary machine cycle is the operation code-fetch cycle of the momentary instruction.
19	$\overline{MREQ}$	Memory Request	Tri-state output, low-active. MREQ = active means that the address for an access (read or write) is present on the address bus.
20	$\overline{IOREQ}$	Input/Output Request	Tri-state output, low-active. IOREQ = active means that an address for selection of the input/output port (input or output) is present at the lower valency 8-bits of the address bus. A IOREQ-signal is also generated when an interrupt instruction has been accepted. In this case it is possible for the associated interrupt vector to be placed on the data bus.
21	$\overline{RD}$	Read	Tri-state output, low-active. RD = active means that the CPU will read data from the memory or from an input/output port. The addressed memory or input/output unit interprets the signal as instruction to place data on the data bus.
22	$\overline{WR}$	Write	Tri-state output, low-active. WR = active means that the CPU will write data to the data bus for the storage or input/output unit.
28	$\overline{RFSH}$	Refresh	Output, low-active. RFSH = active means that the lower order 7-bits of the address bus carry a refresh address for dynamic memories and that the valid MREQ-signal for initiating a refresh cycle is to be used for all dynamic storages connected.
18	$\overline{HALT}$	Halt Condition	Output, low-active. HALT = active means that the CPU has executed a (software) HALT order and is waiting for an interrupt signal (non-maskable interrupt or a released maskable interrupt) for further processing of the program. In the HALT state, the CPU issues inactive orders (NOP's) to save the refresh process.
24	$\overline{WAIT}$	Wait	Input, low-active. Low signal at WAIT-input. Indicates to the CPU that the addressed memory or input/output unit is not ready for data transmission. The CPU will run Wait-cycles as long as the input is activated.
16	$\overline{INT}$	Interrupt Request	Input, low-active. The interrupt request signal is generated by a periphery circuit. The request is accepted after executing the running instruction, if the internal software-controlled interrupt release flipflop is set and the BUSRQ-signal is not active.

Pin	Signal	Function	Commentary
17	$\overline{NMI}$	Nonmaskable Interrupt	Input, low-active. An interrupt request at this input has a higher priority than interrupt requests at input INT for maskable interrupts, and is not deactivated by the internal interrupt release flipflop. If a low-signal is fed to the NMI-input, the program processing will be continued at storage address 0066 H corresponding to a RESTART-instruction.
26	$\overline{RESET}$	Reset	Input, low-active. Effects resetting (= 0) of the interrupt release flipflop, order counter, register I and R, and sets the CPU to the 8080 interrupt mode. During the reset process, the data and address busses are at high-impedance, whereas all other outputs are at inactive condition.
25	$\overline{BUSRQ}$	Bus Request	Input, low-active. Places address, data and control bus signals to high impedance, so that external circuits are able to use these lines.
23	$\overline{BUSAK}$	Bus Acknowledgement	Output, low-active. Acknowledges, that address, data and control bus have been brought to their high-impedance condition.

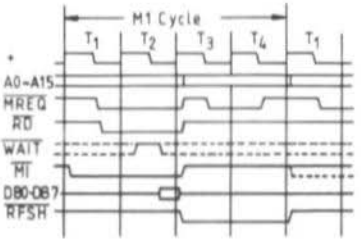


Fig. 8: CPU instruction read cycle

The time sequences of the Z 80-CPU are given in **Figure 8**. The following types of processing cycles are provided:

- **Instruction Op-Code Fetch**

  The contents of the order counter is placed on the address bus at the commencement of the cycle, followed by the $\overline{MREQ}$ active signal 1/2 a clock impulse later, so that the fall slope of the $\overline{MREQ}$ signal can be directly used as release signal (Chip Enable) for the dynamic memories. During $\overline{RD}$ = active, the data from the memory are transmitted to the data bus; these are accepted by the CPU during the rise slope of the clock impulse T 3. Clock impulses T 3 and T 4 of a read cycle are used to source the refresh signal to the dynamic memories during instruction code, decoding and execution in the CPU. $\overline{RFSH}$ releases these refresh signals.

- **Memory Read-or-Write Cycles**

  The $\overline{MREQ}$ and $\overline{RD}$ signals behave in the same way during read or write cycles as during the order cycle **(Figure 9)**. In the write cycle, $\overline{MREQ}$ is active as soon as the information on the address bus is stable, which means that this signal can be used directly as »Chip-Enable«-signal for the dynamic memory.

  $\overline{WR}$ is active as soon as the informations on the data bus are stable which means that it can be used as R/W-signal for all semiconductor memories.

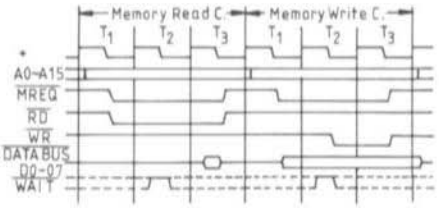


Fig. 9: Memory cycle

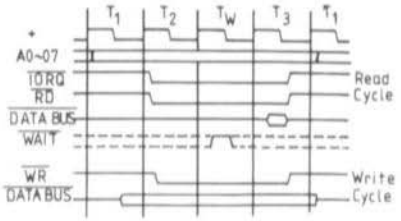


Fig. 10: CPU input/output cycle

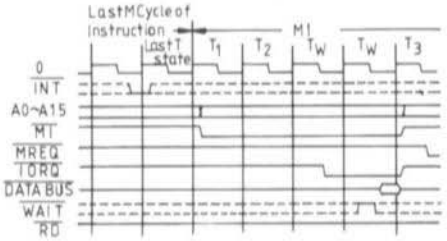


Fig. 11: CPU interrupt cycle

- **Input/Output Cycle**

  A wait cycle (Tw) is inserted during input /output operations in order to allow the input/output port sufficient time for address decoding and may be for activating the $\overline{\text{WAIT}}$-signal **(Figure 10)**.

- **Interrupt Request/Acknowledge Cycle**

  The interrupt input is requested by the CPU during the rise slope of the last clock pulse of each processed order. In the case of an interrupt condition, a special $\overline{\text{M1}}$ cycle is activated, however, $\overline{\text{IORQ}}$ will be active instead of the $\overline{\text{MREQ}}$, as signal for the circuit to be interrupted so that an 8-bit vector is fed to the data bus. Two wait cycles Tw are automatically inserted to allow the priority circuit sufficient time for transmitting the priority signals **(Figure 11)**.

1.2.4. Executing an interrupt by the CPU

Program interruptions allow a running program to be interrupted at any time. They are necessary, for instance, if an unwanted continuous loop is programmed and the operator wishes to cease this from a peripheral unit. However, the main application for this is, when a program is running continuously in the background (e.g. real time clock) and when a main program is running simultaneously, or virtually simultaneously. The Z 80 has a special interrupt mode for this. If a peripheral unit requests an interrupt, the CPU will firstly test if this interrupt is permissible. If an interrupt is allowed, the CPU will check further whether the unit is allowed to request an interrupt at this time (test of highest priority). If the peripheral unit has the highest priority, the CPU will inform the peripheral unit with a special M 1 - cycle **(Figure 11)**. The peripheral unit transmits a previously loaded 8-bit constant (interrupt vector) to the data bus. This interrupt vector is read by the CPU and is interpreted as a 16-bit address together with the contents of the I-register of the CPU (interrupt register). This 16-bit address is a pointer to the interrupt program, and is then loaded into the program counter. Before running the interrupt program, the last program counter state is loaded to the stack. It is now possible for the interrupt program to run (any required program). The return to the main program is possible by providing a RETI-instruction (Return from Interrupt). If the peripheral unit reads a RETI-order, the last contents of the stack, which is the previous address of the program counter, is loaded into the program counter and increased by 1 (incremented). The main program now continues.

1.3. Hexadecimal Code

The hexadecimal code is to be explained for better understanding of the following sections since it is always used during the description of the addresses.

The CPU only knows two conditions: »On« and »Off« (rather: High and Low).

The base of the decimal system is, of course, the number ten (since we have ten fingers). In the decimal system, any number

is given as a sum of the product of a number between 0 and 9 and a power of ten as individual terms.

Arithmetically speaking, this is

$$x = \Sigma\, a_m \times 10^m$$

This sounds very complicated but can be easily described with the aid of an example:

$310.52 = 3 \times 10^2 + 1 \times 10^1 + 0 \times 10^0 + 5 \times 10^{-1} + 2 \times 10^{-2} = 3 \times 100 + 1 \times 10 + 0 \times 1 + 5/10 + 2/100$

It is possible in the same manner for any number to be given in the form of one or two, for instance:

$9.5 = 1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} = 8 + 0 + 0 + 1 + 0.5$

When displayed in a binary manner, the number will then be:

H	L	L	H.H
or			
1	0	0	1.1

Of course, it is very difficult and unfavorable to write down very long binary numbers. In order to simplify this, four sequential numbers are combined. The binary numbers 0000 to 1001 result in the well-known BCD-code; the others are coded with A to F, as is shown in the following table:

0000 = 0	1010 = A
0001 = 1	1011 = B
0010 = 2	1100 = C
0011 = 3	1101 = D
0100 = 4	1110 = E
0101 = 5	1111 = F
0110 = 6	
0111 = 7	
1000 = 8	
1001 = 9	

This means that the binary number 1011/0110/1010/0100 can be reduced to B 6 A 4

In order to show that this is a hexadecimal number, it is provided with a H at the end, which is not defined in the hexadecimal code. This means that the previous number is given as follows:

B 6 A 4 H = 1011011010100100 = 46756 decimal.

A so-called octal-code is also available, but is not to be discussed here.

1.4. Description of the CPU-Circuit

Due to the low fanout (1.6 mA per pin), it is necessary for the output signals from the CPU to be amplified. In the case of the address or control bus, this is achieved using four 6-time bus amplifiers type SN 74 LS 367 N. The data is amplified by two bi-directional bus drivers (8216). It is only the $\overline{\text{BUSAK}}$ (Bus Acknowledgement) that is amplified separately using a SN 74 LS 04, since this signal is required during »Direct Memory Access« of the Z 80 DMA, in order to bring the data and control bus to high impedance.

Integrated circuit I 8 is provided for directional control by programming the actual combinations for directional control. This means that only that part of the 8216 is active in which direction the data flow is occuring, and the other must be at high impedance. In addition to this, the 8216 may only be active when the $\overline{\text{BUSAK}}$ is not active. In other cases, the 8216 must be at high impedance.

The clock frequency is fed via the BUS from a separate clock generator. A separate clock generator is required in order to generate other frequencies required. Several different frequencies are required for the arithmic processor unit (number cruncher), the band rate generator, the real time generator, the monitor-interface and finally for the CPU, and these must be fed via the bus.

1.4.1. Gate Functions of the IM 5610

As previously mentioned, the program in I 8 (IM 5610) sets the data bus buffers to the required direction. The logic table of the 8216 is as follows:

$\overline{\text{CS}}$ Pin 1	$\overline{\text{DIEN}}$ Pin 15	Buffer Direction
1	X	Tristate, high-imp.
0	1	BUS → CPU
0	0	CPU → BUS

X can be 0 or 1.

This means that the IM 5610 must be programmed as follows:

Inputs of					Outputs of		Commentary
$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IOREQ}$	$\overline{M1}$	$\overline{CS}$	$\overline{DIEN}$	
0	1	0	1	1	0	1	Read from memory
1	0	0	1	1	0	0	Write into memory
0	1	1	0	1	0	1	Read from peripheral
1	0	1	0	1	0	0	Write to peripheral
1	1	1	0	0	0	1	Read interrupt vector
All other states					1	0	

1.4.2. Construction of the CPU

The CPU-circuit shown in **Figure 12** is accommodated on the double-coated PC-board DK 2 RY 001 which is equipped with through-contacts. The dimensions of the board are 162 mm x 101.6 mm. Sockets are used for all components, (individual pin sockets for the Z 80-CPU). In the case of the PC-board available from the publishers, normal IC-sockets (e.g. from TI) will be used. This is advisable in order to replace the integrated circuits, e.g. in the case of a fault. The nine sockets and the connector strip should be inserted from the component side which is designated with a »B« after the designation. No alignment of the module is required **(Figure 13)**.

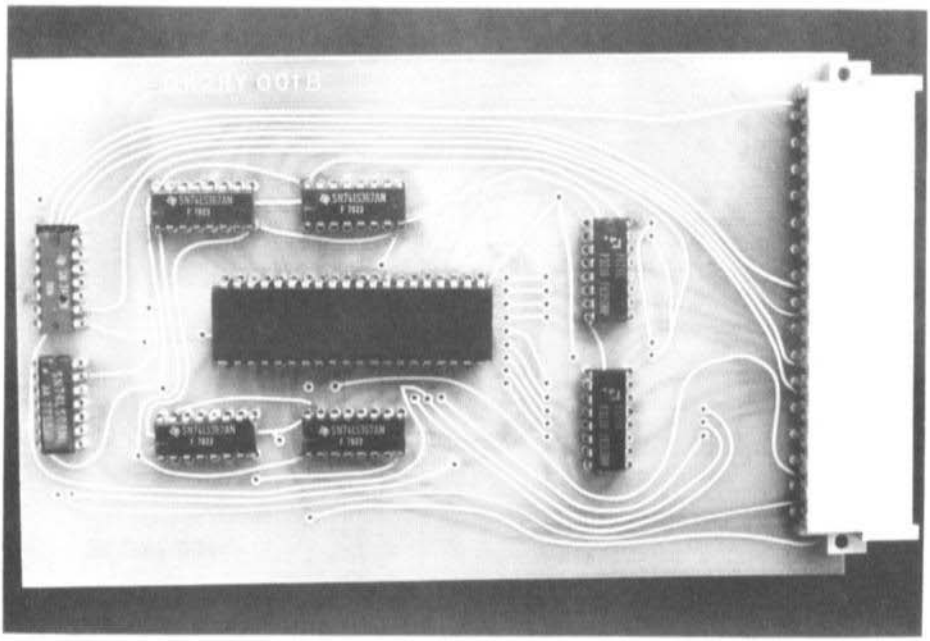


Fig. 12: Photograph of the author's prototype CPU

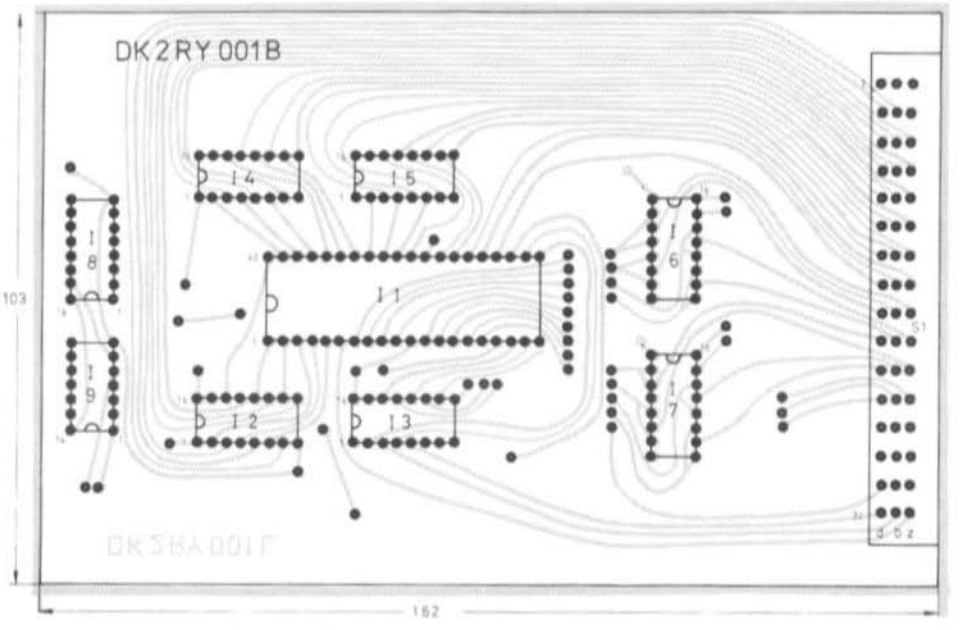


Fig. 13: PC-board DK 2 RY 001 for the CPU

Components

I 1:	Z 80-CPU or Z 80 A-CPU (ZILOG)
I 2 to I 5:	SN 74 LS 367 (Texas Instr.)
I 6, I 7:	8216 (INTEL, Siemens)
I 8:	IM 5610 (Intersil) SN 74 S 288 N (TI)
I 9:	SN 74 LS 04 N (TI)
S 1:	48-pin connector (Siemens C 74334 - A 40 - A 60)

Part 1 of this series was published in:
VHF COMMUNICATIONS 1/80, pages 52-54

Part 3 will describe the following modules:
Fixed program storage (8 kByte)
Write-read storage (4 kByte)
Bus-board with 9 connections

Part 4 will describe the input/output unit.

REFERENCES

Mikrocomputer-Technik
Hofacker-Verlag München

Z 80 Assembler Handbuch
Kontron-Elektronik, Eching

MATERIAL PRICE LIST OF EQUIPMENT
described in Edition 2/1980 of VHF COMMUNICATIONS

DC 3 NT	**WEATHER SATELLITE RECEPTION SYSTEM**		
DC 3 NT 006	**Power Supply and FAX-Motor Driver**		**Ed. 2/1980**
PC-board	DC 3 NT 006	Single-coated with plan	DM 17.—
Semiconductors	DC 3 NT 006	2 op.amps., 4 Darlingtons, 1 stab., 6 diodes	DM 23.50
Minikit	DC 3 NT 006	6 al. and 3 tantalum electrolytics, 6 pl. foil capacitors, 3 trimmer potentiometers, 7 carbon resistors, 1 31-pin connector	DM 39.50
Kit	**DC 3 NT 006**	**complete with above parts**	**DM 80.—**
DC 3 NT 008	**Frequency Generator Module**		**Ed. 2/1980**
PC-board	DC 3 NT 008	Double-coated, undrilled, without plan	DM 32.—
Semiconductors 1	DC 3 NT 008	For CRT-Module: 8 CMOS-ICs, 1 Op.amp., 6 diodes	DM 31.—
Semiconductors 2	DC 3 NT 008	Required in addition for FAX: 4 CMOS-ICs, 1 quad-op.amp., 2 FETs, 2 diodes	DM 19.—
Minikit 1	DC 3 NT 008	1 pl.foil trimmer, 2 styroflex caps., 6 pl.foil caps., 1 ceramic cap., 2 tantalum caps., 1 spindle pot. 5 kΩ, 49 carbon resistors, 1 31-pin connector	DM 33.—
Minikit 2	DC 3 NT 008	Required in addition for FAX: 6 spindle potentiometers	DM 24.—
Crystal	4.433 MHz	HC-18/U	DM 16.—
Kit 1	**DC 3 NT 008**	**complete for operation of the CRT-module**	**DM 110.—**
Kit 2	**DC 3 NT 008**	**complete for all modules w/all above parts**	**DM 149.—**
DK 1 OF 042	**Transmit-Receive Converter 2 m / 10 m**		**Ed. 2/1980**
PC-board	DK 1 OF 042	Single-coated, with plan	DM 13.—
Semiconductors	DK 1 OF 042	5 transistors, 2 diodes, 1 ring mixer IE-500	DM 70.—
Minikit	DK 1 OF 042	3 Neosid coilkits, enamelled copper wire, silver-plated copper wire, 3 pl.foil trimmers, 3 feedthrough caps., 13 bypass caps., 17 ceramic disc caps., 22 carbon resistors, case 145 x 73 x 28 mm inner dimensions	DM 46.—
Crystal	38.6667 MHz	HC-6/U	DM 17.—
Attenuator	MMR 16/10	16 dB / 10 W	DM 45.—
Kit	**DK 1 OF 042**	**complete with above parts**	**DM 189.—**
DJ 7 VY 003	**Large-signal Noise Blanker**		**Ed. 2/1980**
PC-board	DJ 7 VY 003	Double-coated, with thru-contacts	DM 39.50
Minikit	DJ 7 VY 003	8 coil sets D 41-2165, 7 miniature chokes 22 µH, 7 toroids R 6.3 N 30, 1 toroid R 10 K 1, 1 m miniature coax. SM 50, 3 m stranded wire 12 x 0.03 HFL	DM 59.—
Kit	**DJ 7 VY 003**	**with above parts**	**DM 98.—**
OE 7 WMI 001	**AFC-Module with Acoustic Feedback Suppression**		**Ed. 2/1980**
PC-board	OE 7 WMI 001	Single-coated with plan	DM 12.—
Kit	**OE 7 WMI 001**	**on request**	

NEW COAXIAL SPECIALITIES

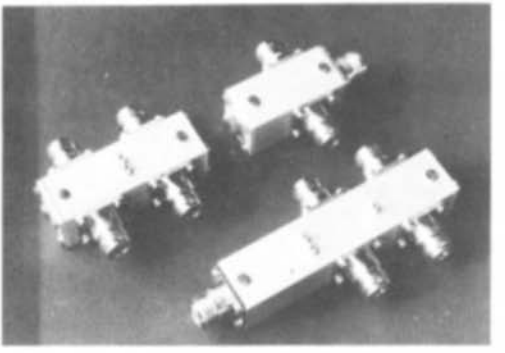


Fig. 1

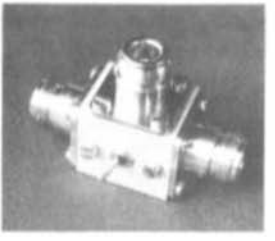


Fig. 2

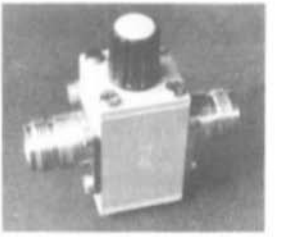


Fig. 3

A completely new programme of coaxial products offering some entirely new possibilities in the HF, VHF and UHF-range:

- **Inexpensive multi-port coaxial relays (Fig. 1)** with 2, 3, or 4 input ports (antennas) to 1 output port (feeder). 50 Ω N-Connectors. Low-loss with good crosstalk rejection (isolation).
- **Multi-port coaxial switches (Figure 2)** with two or five positions. 50 Ω N-connectors. Low-loss and good crosstalk rejection.
- **Multi-port coaxial switch** with 50 Ω cable connections suitable for installation within equipment. RG-58/U.
- **Variable attenuator (Figure 3)** 0-20 dB with 50 Ω N-connectors.
- **Wideband test amplifier** for swept-frequency and spectrum analyzer measurements as well as other applications. Flat passband range upto 1300 MHz. Gain at 800 MHz: 24 dB.
- **Precision detectors** Input N or BNC connectors, output (DC) BNC.
- **Coaxial matching transformers** (power splitters) for 2 or 4 antennas. Available for 145 MHz, 432 MHz, and 1296 MHz. 50 Ω N-connectors.

Full details and prices from your National Representative, or direct from the publishers.

Even Colour ATV-Communications are easy with our ATV-7010 Transmitter

The **ATV-7010** is a complete TV-transmitter for the 70 cm band. It is only necessary to connect a colour or monochrome TV-camera, microphone, antenna, and power-line (220 V / 50 Hz).

The TV-transmitter uses a video-sound spacing according to CCIR. All transmissions can be received on a domestic TV-receiver equipped with a 70 cm converter.

Request full details from your national representative, or from the publishers. ATV-converters and matching antennas are also available.

Specifications:
Frequencies (xtal-controlled): Video 434.250 MHz, sound 439.750 MHz.
Third-order IM: typ. – 30 dB; f_{osc} and f_{image} typ. – 55 dB.
Unmodulated carrier output: typ. 10 W. 3 ICs, 34 transistors, 24 diodes.
Dimensions: 320 mm by 110 mm by 190 mm.
Delivery ex. stock to maximum 8 weeks.

UKWtechnik Hans Dohlus oHG · Jahnstr. 14 · Postfach 80 · D-8523 Baiersdorf
UKWberichte Tel. 09133/855 (Tag und Nacht)

Professional Weather Satellite Reception Systems

We offer a complete system of inexpensive modules for professional applications. These are of special interest for meteological offices at smaller airports, for harbour and similar applications. They are also suitable for instruction at universities, and scientific institutes. A number of image processing systems and receivers are available to suit the application in question. Equipment is available, or under development for:

- The METEOSAT and GOES/GMS satellites in Geostationary orbit, or
- The NOAA and TIROS M satellites in polar orbits (136 - 138 MHz).

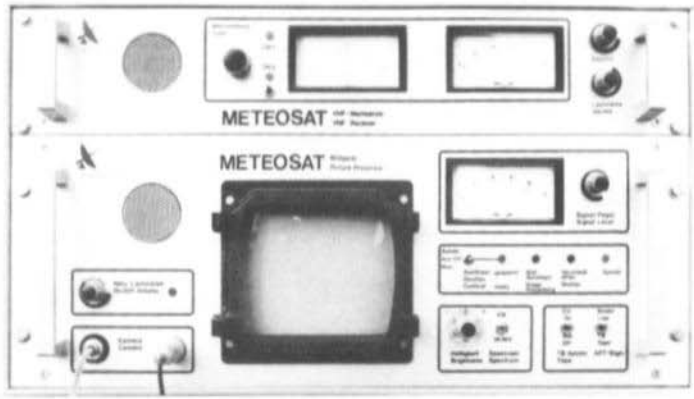
Technical specifications of the basic METEOSAT system:

PARABOLIC ANTENNA:
1.2 m dia., 24 dB gain

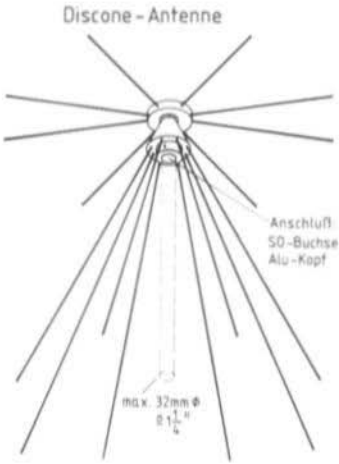
SHF-CONVERTER:
2-stage low-noise preamplifier
with noise figure 3 dB

VHF-RECEIVER:
Noise figure 2 dB
AF-bandwidth:
800 - 4000 Hz
Subcarrier output:
2.4 kHz/1 V

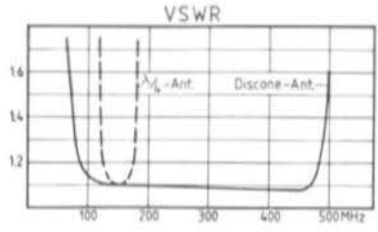
VIDEO PROCESSOR:
Monitor tube and
Polaroid camera

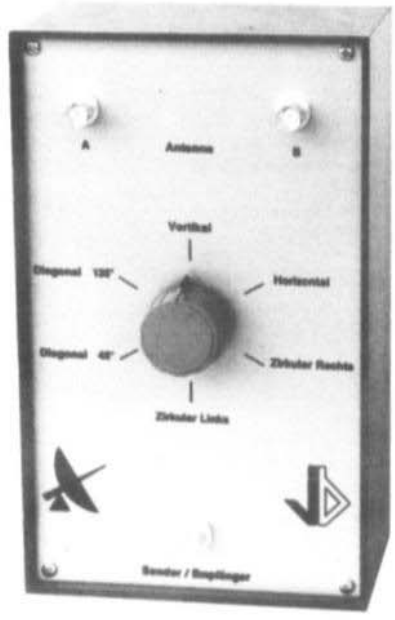


WIDEBAND OMNIDIRECTIONAL DISCONE ANTENNA



- Frequency range: 80 - 480 MHz
- Gain: 3.4 dB / λ/4
- Impedance: 50 Ω
- Power rating: 500 W
- Polarisation: Vertical
- Connection: SO 239 socket in the head
- VSWR: < 1.5 : 1
- Weight: 3 kg
- Dimensions: Height: 1.00 m / Diameter: 1.30 m
- Material: Aluminium
- Mounting: Antenna head is put onto a 32 mm (1¼") dia. mast and secured by a screw.

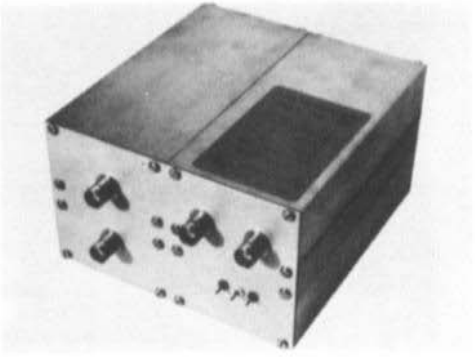




NEW! NEW!
Polarisations Switching Unit for 2 m Crossed Yagis

Ready-to-operate as described in VHF COMMUNICATIONS. Complete in cabinet with three BNC connectors. Especially designed for use with crossed yagis mounted as an »X«, and fed with equal-length feeders. Following six polarisations can be selected: Vertical, horizontal, clockwise circular, anticlockwise circular, slant 45° and slant 135°.

VSWR:	max. 1.2
Power:	100 W carrier
Insertion loss:	0.1 to 0.3 dB
Phase error:	approx. 1°
Dimensions:	216 x 132 x 80 mm



A New Generation of Transverters for 1296 MHz

We would like to introduce our second generation of 23 cm transverters for operation in conjunction with either 10 m or 2 m transceivers.

- Double-conversion both on transmit and receive with the 10 m version to obtain the extremely high image and spurious rejection and clean spectrum.
- Overall noise figure of the receive converter typically 3.9 dB
- Transverters are available in the following versions:

ST 1296/144 A:	2 m IF, output 1 W	**DM 620.—**
ST 1296/144 B:	2 m IF, output 3 W	**DM 786.—**
ST 1296/28:	10 m IF, output 1 W	**DM 770.—**

NEW 23 cm CONVERTER SC 1296/144

Noise figure typ. 3.9 dB, gain typ. 22 dB. Operating voltage 12 V. Contained in aluminium case with BNC-connectors. Similar to ST 1296/144. **Price DM 225.—**

UKWtechnik Hans Dohlus oHG · Jahnstr. 14 · Postfach 80 · D-8523 Baiersdorf
UKWberichte Tel. 09133/855 (Tag und Nacht)

ANTENNA ROTATORS

KR 400, KR 400 RC
KR 600, KR 600 RC

KR 2000

MX 1000

ART 8000

Controllers for above rotators

Our well-known rotators KR 400, KR 600 and KR 2000 are now available with large 360° compass indicators of 105 mm diameter. These models are designated by the suffix »RC«.

Programmable controllers with manual or digital programming are available on request.

Further details are available from your national representatives or from:

KR 400, KR 600, KR 2000

KR 400 RC, KR 600 RC, KR 2000 RC

MX 1000

ART 8000

UKWtechnik Hans Dohlus oHG · Jahnstr. 14 · Postfach 80 · D-8523 Baiersdorf
UKWberichte Tel. 09133/855 (Tag und Nacht)

CRYSTAL FILTERS OSCILLATOR CRYSTALS

SYNONYMOUS FOR QUALITY AND ADVANCED TECHNOLOGY

NEW STANDARD FILTERS

CW-FILTER XF-9NB see table

SWITCHABLE SSB FILTERS

for a fixed carrier frequency of 9.000 MHz

XF-9B 01

8998.5 kHz for LSB

XF-9B 02

9001.5 kHz for USB

See XF-9B for all other specifications
The carrier crystal XF 900 is provided

Filter Type		XF-9A	XF-9B	XF-9C	XF-9D	XF-9E	XF-9NB
Application		SSB Transmit	SSB	AM	AM	FM	CW
Number of crystals		5	8	8	8	8	8
3 dB bandwidth		2.4 kHz	2.3 kHz	3.6 kHz	4.8 kHz	11.5 kHz	0.4 kHz
6 dB bandwidth		2.5 kHz	2.4 kHz	3.75 kHz	5.0 kHz	12.0 kHz	0.5 kHz
Ripple		< 1 dB	< 2 dB	< 2 dB	< 2 dB	< 2 dB	< 0.5 dB
Insertion loss		< 3 dB	< 3.5 dB	< 3.5 dB	< 3.5 dB	< 3.5 dB	< 6.5 dB
Termination	Z_t	500 Ω	500 Ω	500 Ω	500 Ω	1200 Ω	500 Ω
	C_t	30 pF	30 pF	30 pF	30 pF	30 pF	30 pF
Shape factor		(6:50 dB) 1.7	(6:60 dB) 1.8	(6:60 dB) 1.8	(6:60 dB) 1.8	(6:60 dB) 1.8	(6:60 dB) 2.2
			(6:80 dB) 2.2	(6:80 dB) 2.2	(6:80 dB) 2.2	(6:80 dB) 2.2	(6:80 dB) 4.0
Ultimate rejection		> 45 dB	> 100 dB	> 100 dB	> 100 dB	>90 dB	> 90 dB

XF-9A and XF-9B complete with XF 901, XF 902
XF-9NB complete with XF 903

KRISTALLVERARBEITUNG NECKARBISCHOFSHEIM GMBH
D 6924 Neckarbischofsheim · Postfach 7