

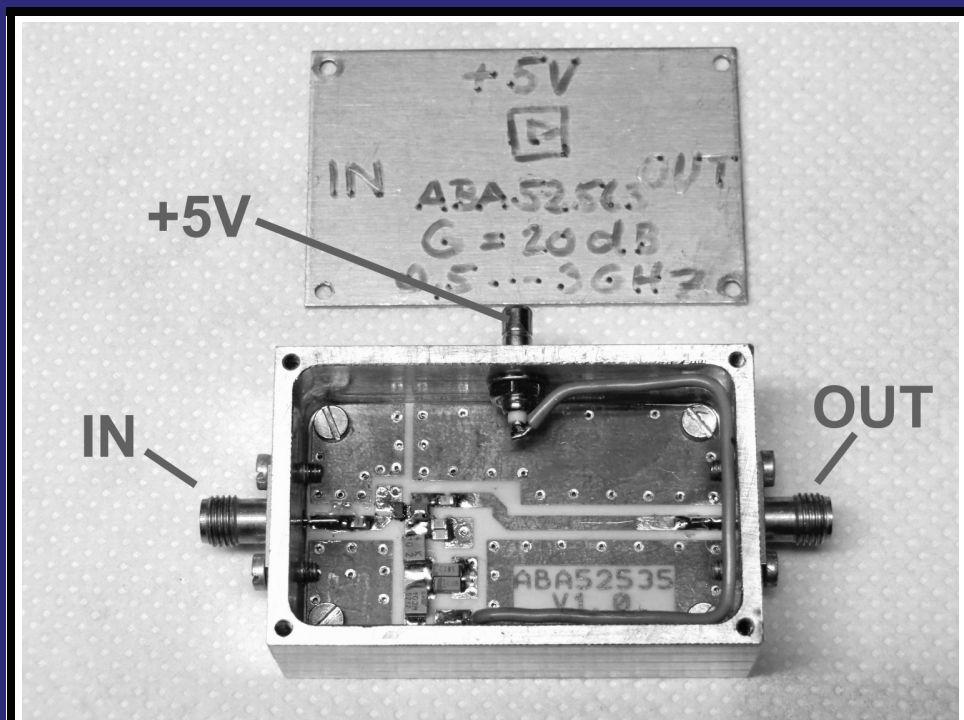


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# VHF COMMUNICATIONS

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**Practical project, Development of a 50MHz to  
2.5GHz wideband MMIC amplifier**

*Gunthard Kraus, DG8GB*

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*I think this will be a difficult year to keep this magazine full of interesting articles. Although the main supply of articles should come from the German magazine UKW Berichte it has republished several articles from VHF Communications magazine subscribers. Because I have already published those articles it cuts down on the material available to fill the pages of this magazine. I will rely more than ever this year on articles submitted by VHF Communications magazine readers. If you have a project that you are working on that you think would be of interest please contact me and I will help to convert it into an interesting article for the magazine..*

73s - Andy



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Gunthard Kraus, DG8GB

# Practical project, Development of a 50MHz to 2.5GHz wideband MMIC amplifier, Part 2

## Continuation from 4/2011

### 2.4. Extension of the simulation circuit

Reason: It is advisable to include the capacitors and micro strip lines at the input and output of the MMICs into the simulation so that there are no bad surprises in later measurements, particularly starting from 1GHz.

#### 2.4.1. Design of strip lines with Ansoft Designer SV

Grounded Coplanar Waveguides are used. These are micro strip lines above a

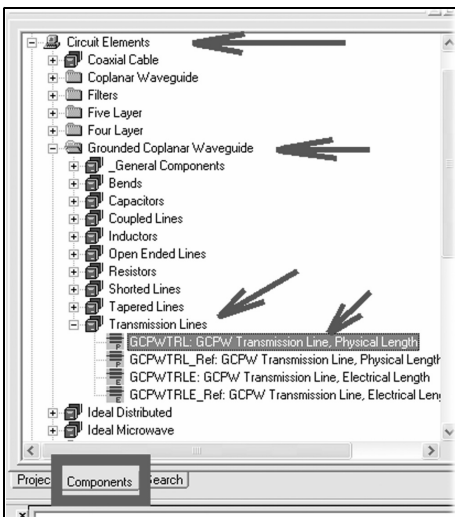
continuous ground surface; the transmission line on the top surface is surrounded with two further ground surfaces on the left and right. Their distance (Gap) to the centre line is only in 0.5mm. Together with the lower ground surface this gives outstanding shielding thus great security against radiation of spurious signals.

Fig 23 shows the path for the changes to “the Components” page (Circuit Elements/Grounded Coplanar Waveguide/Transmission lines), to find the component “GCPW Transmission Line, Physical Length” that is used in the circuit diagram. When the line is selected a menu showing the different levels of the printed circuit board emerges; select “Merge Layers” and then place the line.

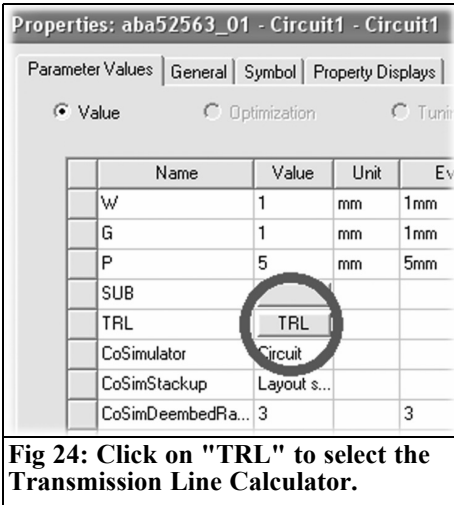
Double left clicking on the circuit symbol of the strip line opens the “Property menu“ (Fig 24) then start the transmission line Calculator (TRL). This produces an interesting screen; first examine the lower left half to make sure the RO4003 data is correct (see chapter 2.3.2.2.). The data for the copper metallisation is controlled in the centre of the screen.

The data required for the transmission line is shown in order in Fig 25:

- 1: Conductor length = 5mm
- 2: Gap (distance of the framing ground surfaces from the conduc-



**Fig 23: This is how to add a "Grounded Coplanar Waveguide".**



**Fig 24: Click on "TRL" to select the Transmission Line Calculator.**

tor) = 0.5mm

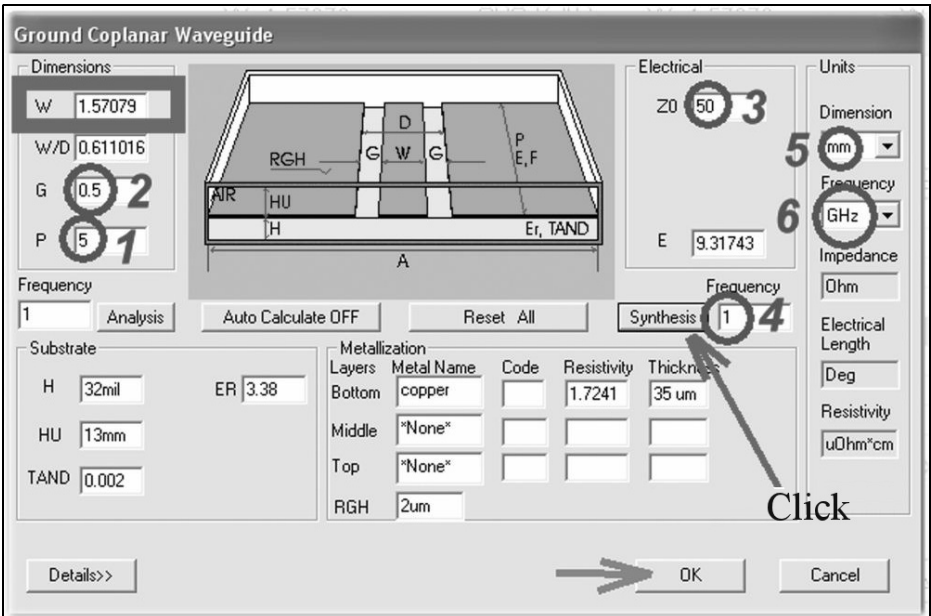
- 3: Characteristic impedance = 50Ω
- 4: and 6: Test frequency = 1GHz
- 5: Mechanical dimensions in "mm"

Once that is created, click "Synthesis" and the conductor width appears in the top left window showing 1.57mm. Clicking "OK" automatically transfers the computation result to the Property Menu of the piece of line already placed; the physical length of 5mm can then be added and all other dimensions checked (conductor width = 1.57mm, Gap = 0.5mm, physical length = 5mm).

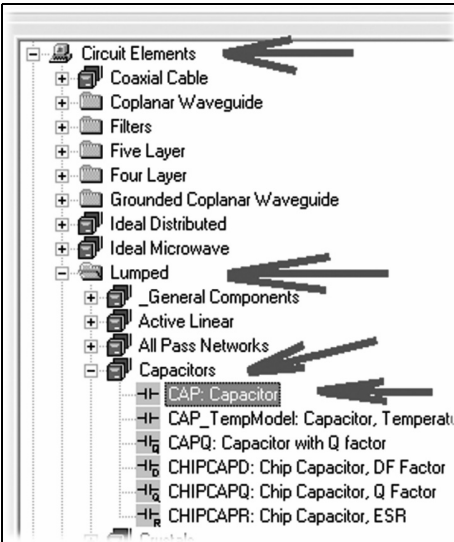
Using Windows cut and paste, the line can be marked and copied to the cut and paste buffer. This should be carried out three times to place the lines required. The last line should be changed in its properties menu from a length of 5mm to 35mm. Now the circuit changes should be made.

**2.4.2. Installation of the pieces of line.**

This continues to with the DC coupling capacitors: these are found on the usual path (Fig 26): Change to the "Components" page, then from the path (Circuit Elements/Lumped/Capacitors) drag the



**Fig 25: Follow steps 1 to 6 carefully then click on "Synthesis" to calculate the width of the strip line (see text).**



**Fig 26: Look for the simple capacitor in the large component library.**

capacitor CAP twice onto the work area. Please do not forget to change back to the project page.

First, delete the connections in the circuit diagram between the ports and the MMIC pins in order to create a place for the strip lines and capacitors to produce the diagram shown in Fig 27.

Please do not forget:

- Every coupling capacitor must have a value of 470pF.
- The piece of line with the largest

length (35mm) must always be attached at the output, because line losses at the input increase the noise figure (Noise Figure) by exactly their value.

**2.4.3. Simulation of the changed circuit**

Starting the simulation gives the result shown in Fig 28.

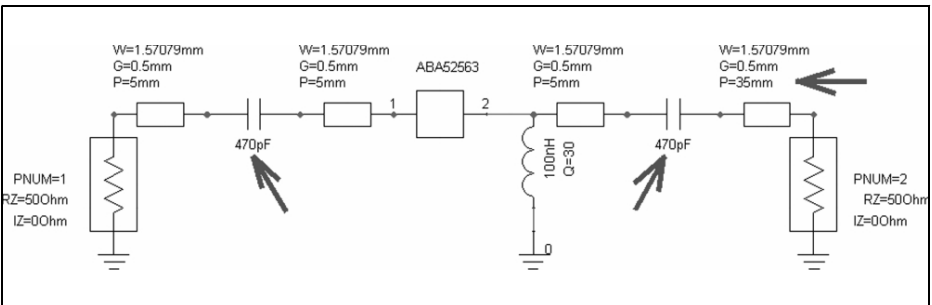
The line losses and the coupling capacitor losses and series inductances of the capacitors become noticeable at the high frequencies and lower the gain and cut off frequency. If lower cut off frequency needs to be reduced, the value of the inductance at the output must be increased. However the self-resonant frequency of this component will then be lower and the high frequency gain will decrease (an SMD inductance behaves like a capacitor above its self-resonance whose resistance becomes smaller with rising frequency).

**2.4.4. Stability control**

This should never be forgotten, which is no problem, if the S parameters are available.

Click on “Results” on the project page with the right mouse button and afterwards on “Create Report” (Fig 29). Check that “Rectangular Plot” is selected on the menu that appears then click OK.

The necessary entries and actions are



**Fig 27: This is the extended simulation diagram with lines and coupling capacitors. Do not forget that the last line is 35mm long (see text).**

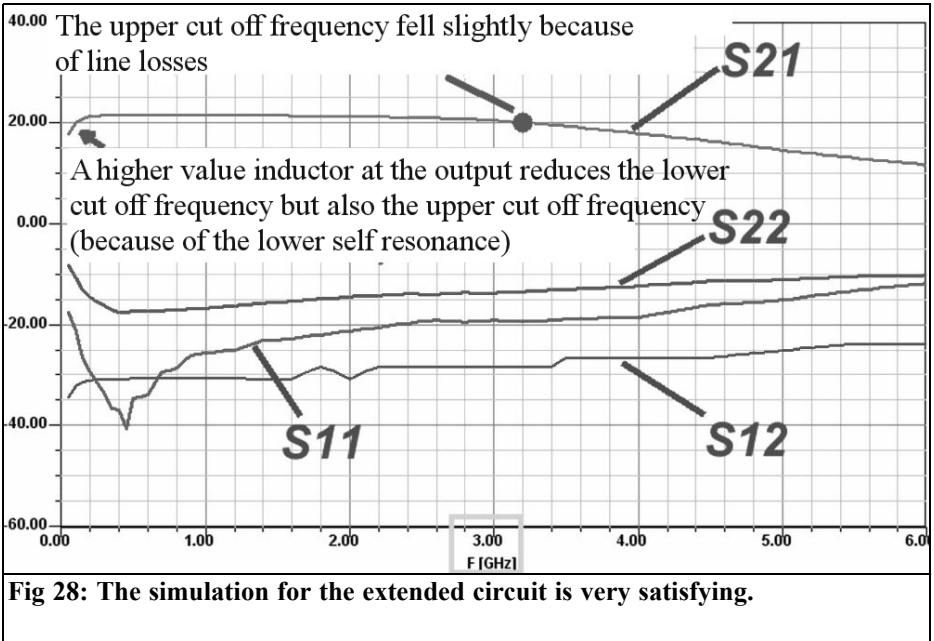


Fig 28: The simulation for the extended circuit is very satisfying.

shown in Fig 30:

- 1: Stability
- 2: Stability factor “k”
- 3: Absolute value of k
- 4: Press "Add Trace" and

5: Finish with "Done"

The expected result is shown in Fig 31, the curve remains, as desired, above the stability limit of  $K = 1$  everywhere.

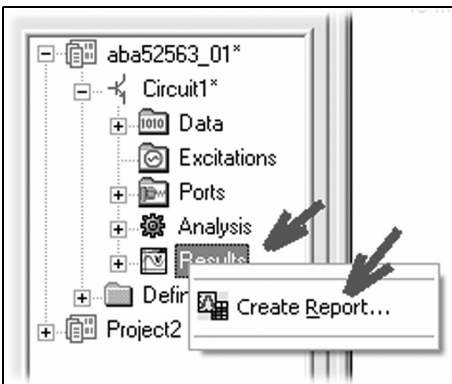


Fig 29: With modern programs the stability can be shown with a new report.

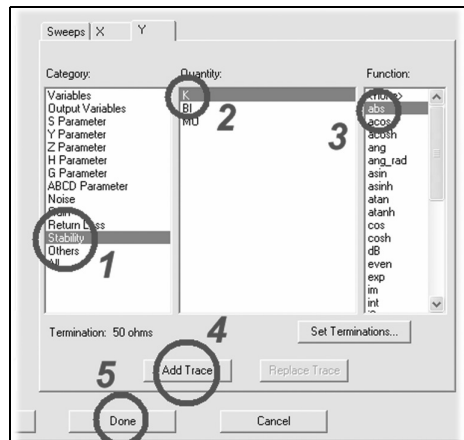
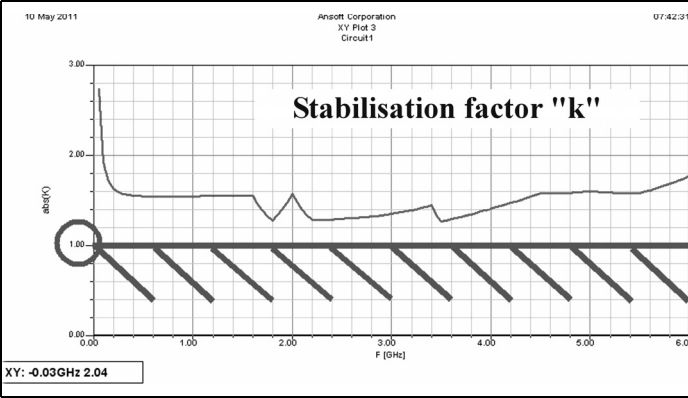


Fig 30: This is how to carefully program the stability report.



**Fig 31: The reassuring result is compensation for the effort to produce the design.**

### 3. The amplifier module in practice

#### 3.1. A view of the printed circuit board

The simple construction principles of a microwave printed circuit board is good to see in Fig 32:

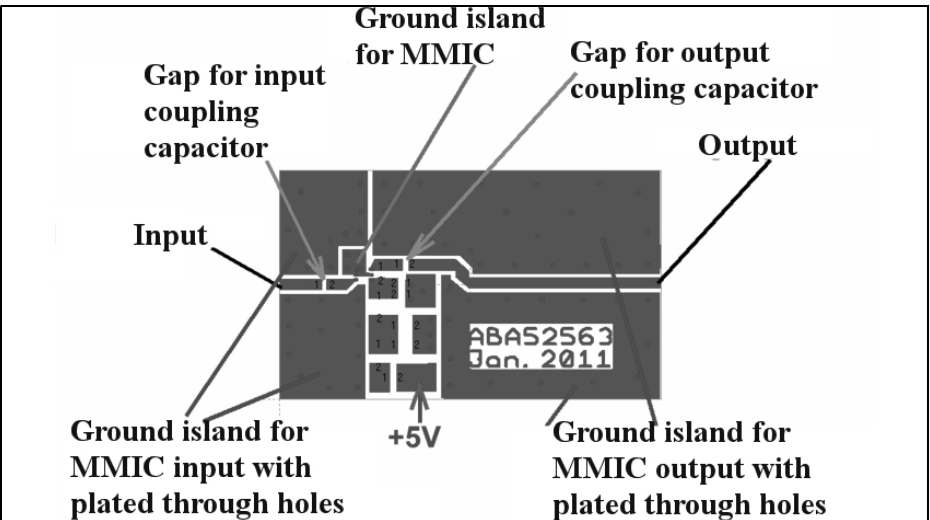
The lower surface of the double-sided

printed circuit board always is a continuous ground surface - it represents the infinite earth plane.

On the top side RF signals are fed on micro strip lines or “Grounded Coplanar Waveguides”. These are interrupted for coupling capacitors or the MMICs by a short gap.

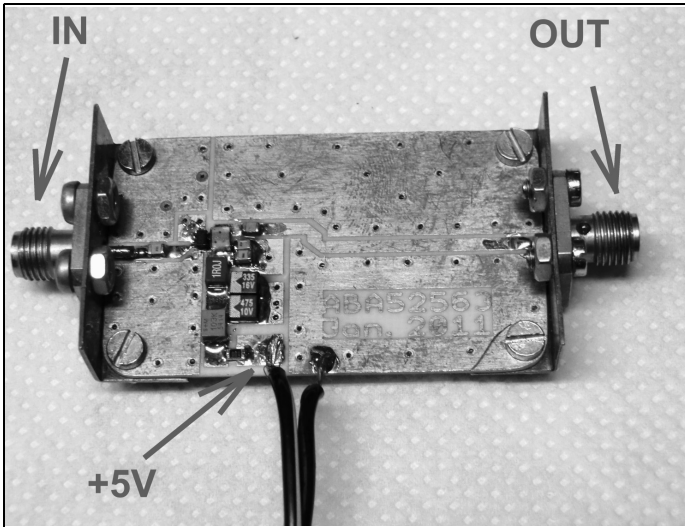
#### Importantly:

Ground islands that are connected to the lower ground plane with plated through holes separate the individual circuit elements.



**Fig 32: A sketch of the printed circuit board.**





**Fig 33: Copper angle fitted to each end of the PCB for the input and output connectors.**

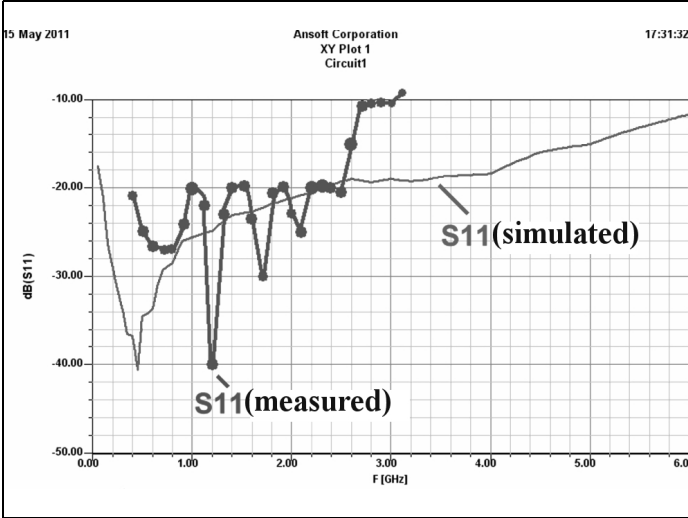
In particular the input ground islands must not be connected with other islands that belong to the output. Solid wires must not be used for the plated-through holes; metallised holes (Vias) must be used. 0.8mm diameter silver-plated hollow copper rivets are recommended as plated-through holes for prototype printed circuit boards. The more plated-through holes the better because the many small inductances that represent the plated-through holes are connected in parallel and the total inductance become smaller. For those who think that not using wire instead of hollow rivets is strange; it is to do with the skin effect. At high frequencies the current only penetrates a few micrometres into an electrical conductor and with a soldered solid wire the direct path down to the ground plane is blocked. The current must flow to the edge of the island surface then on to the lower surface of the copper layer up to the piece of wire. Only from there it goes down to the ground plane, this extended path not only gives additional loss resistance but also additional inductance. That can easily result in instability or give additional dBs of attenuation in the case of very high frequencies (e.g. at several GHz).

The finished printed circuit board prepared for S parameter measurement is shown in Fig 33. Copper angle is screwed on at the left and right as carriers for the SMA sockets for input and output. The centre conductors of these sockets rest flat on the printed circuit board and their ends are filed at 45°. This results in a reflection-poor transition where they are soldered to the strip line. This method is particularly recommended for the first fast test and functioned problem-free to up to 10GHz.

### 3.2. Measurements of the prototype

The hour of the truth: The measurements of the prototype were made with a modern vector network analyser (Rohde and Schwartz, type ZVRE). This equipment is located in the laboratory of the University in Friedrichshafen. Fig 34 shows how good the simulation was; beginning with S11:

Up to 2.5GHz the value is less than -20dB then clearly becomes worse. However the defaults (S11 smaller than -10dB to 2.5 GHz) are achieved. The wild zigzag movements of the curve are caused by the coupling capacitors with their periodic resonances as well as the input reflection of the network analyser.



**Fig 34: The S11 response measured for the amplifier.**

Its data sheet only guarantees a value “smaller than  $-20\text{dB}$ ” over the entire frequency range.

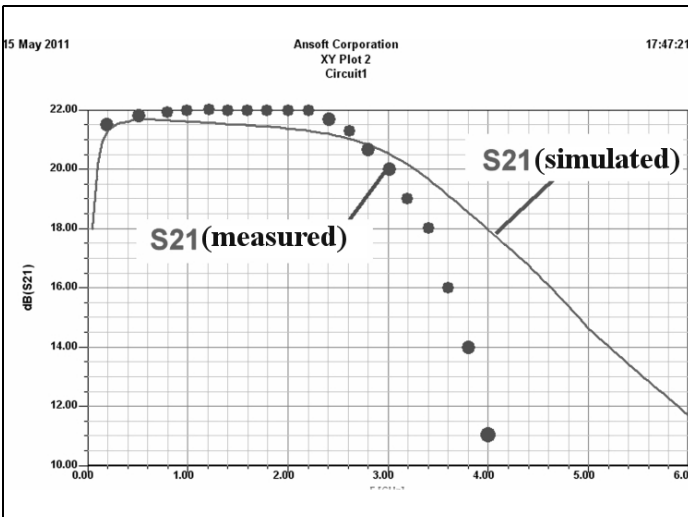
S21 (thus the gain) is shown in Fig 35. The decrease in gain is caused by the self-resonance (approximately 2.2GHz) of the 100nH inductor. If a smaller value had been selected it would have had a lower cut off frequency.

Note: In a separate measurement the lower cut off frequency ( $-3\text{dB}$  frequency)

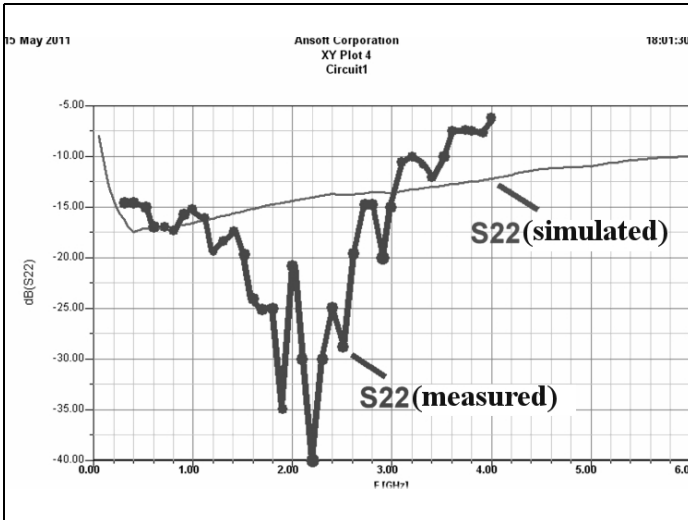
of the amplifier was determined to be 44MHz for this inductance value (100nH).

The output reflection is also of interest, expressed by S22:

From Fig 36 it can be seen that it is even better than the simulation result up to 3GHz. Somewhere about 2.2GHz was the lowest reflection value which is where the self-resonance of the 100nH inductor might lie. That also agrees with



**Fig 35: The S21 response fulfills the requirements (for details see text).**



**Fig 36: The output reflection, S22, is also acceptable.**

the maximum of S21 at this frequency (see previous diagram).

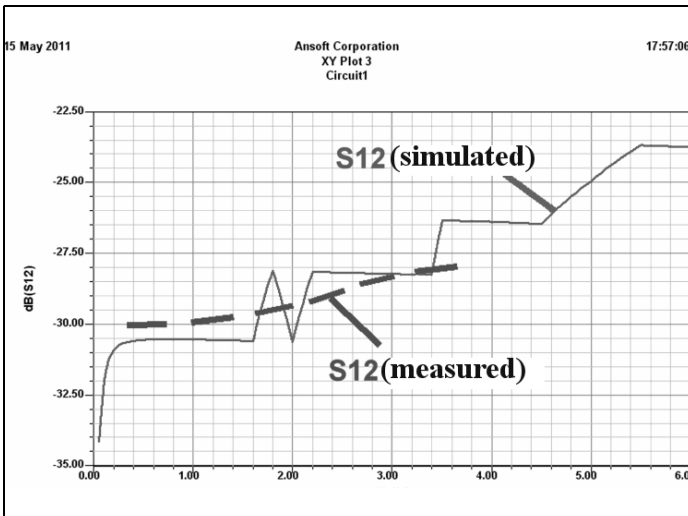
Finally the response from the output to the input (expressed by the parameter S12), shown in Fig 37; it can be seen that it is not a problem.

In principle a prototype PCB can be made and fitted into the milled aluminium housing with a screwed on lid that should not change the performance by much. That will be shown also in the

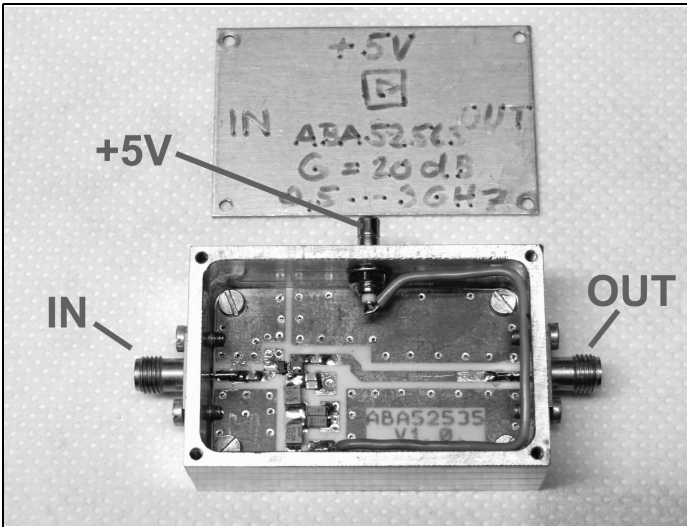
next chapter.

### 3.3. Measurements of the amplifier in the housing

The hour of the truth, part 2: The completion of the overall development and the removal of the last errors took place in my domestic workshop where I have an ancient network analyser (HP 8410 with the S parameter test set for 0.5GHz - 12GHz as well as the HP8690 sweeper).



**Fig 37: The reflections (shown by S12) are low and harmless as expected.**

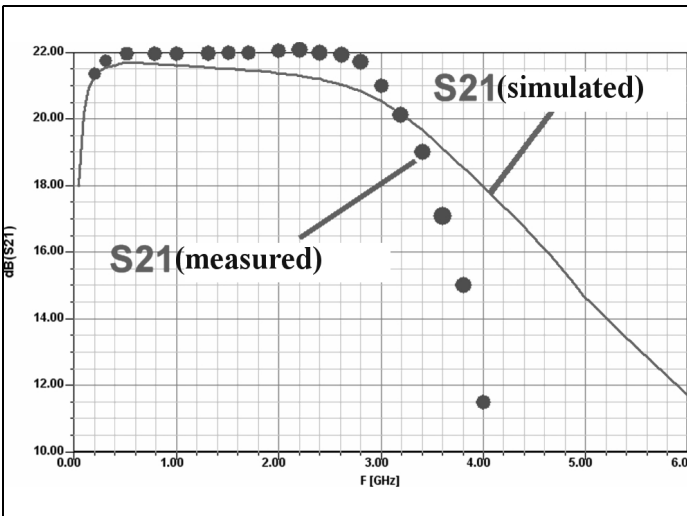


**Fig 38:** This is how the finished product will look. A PCB in a housing with the connectors fitted.

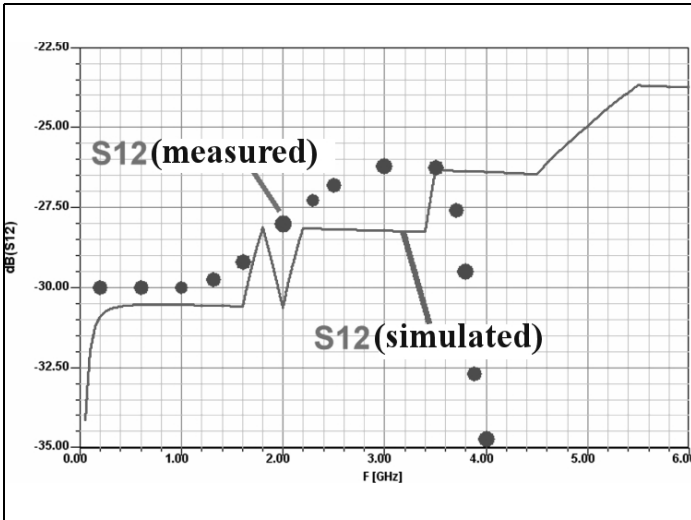
The PCB was bolted into the milled aluminium housing and the SMA sockets for input and output plus the SMB socket supply were fitted. The wire connecting the supply from the SMB socket to the circuit must lie close to the housing running along the housing wall (and close to the cover) past the output. This avoids signal pickup on the supply line from the circuit and the danger of feedback from the output to the input. This is always a problem if the supply voltage is

connected to the top side of the PCB housing but the "supply voltage input pin" on the PCB is arranged at the lower housing side due to the pin sequence of the MMIC. The first attempt in the housing is shown in Fig 38, before the cover was screwed on and measurements taken. This shows the recommended route for the supply wire.

The measurements start with the most interesting curve i.e. with S21 (Fig 39). However some prerequisites are given so



**Fig 39:** The S21 response measured for the complete amplifier using the old network analyser.



**Fig 40: The reflection S21 is not quite the same in the housing.**

that no measuring errors occur with the network analyser.:

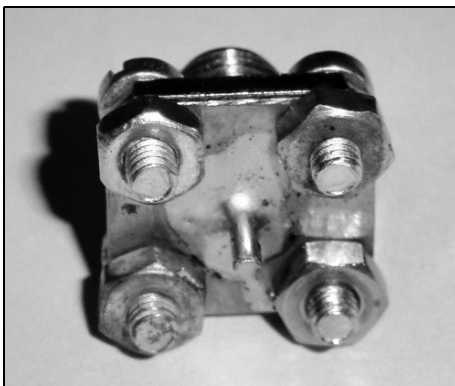
- A 20dB SMA attenuator must be fitted between port 1 of the analyser and the input of the amplifier otherwise the incident wave of the generator will "overdrive" the amplifier input and cause signal compression. Fortunately this can be noticed immediately because some dBs of gain would be missing.
- Before the actual measurement is

made the measuring fixture must be calibrated: The cable connecting port 1 to the attenuator and the signal to port 2 must be as short as possible. The horizontal line on the display is then centred on the zero dB line. The remark about the cable lengths being as short as possible should be taken seriously because when measurements are made up to 4GHz the cable attenuation increases with frequency and suddenly the horizontal line begins to droop downwards.

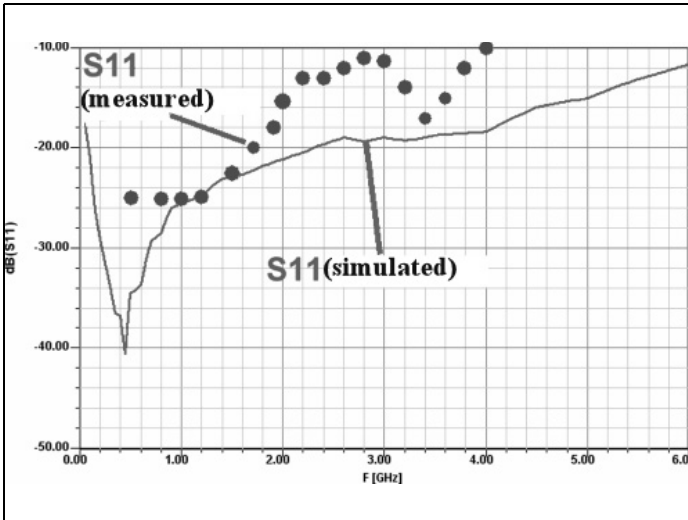
- The network analyser used can only sweep over an octave and therefore has a range synchronisation switch that the user must use correctly. Therefore the measuring procedure is carried out three times, i.e. for 0.5 to 1GHz; 1GHz to 2GHz and 2GHz to 4GHz.

The measurement of S12 does not present problems over the selected frequency range. It is made next using the S12 switch on the measuring bridge. The result in Fig 40 is not at all the same as simulated but it will do the job.

More effort is necessary for the reflection measurements. First for S11 the switch



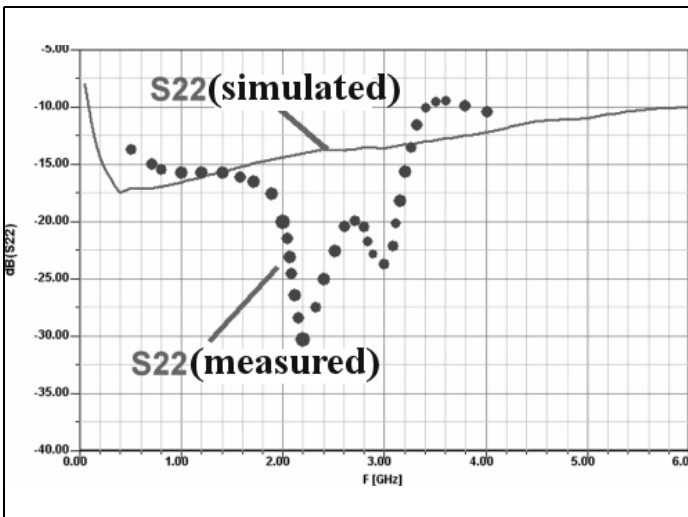
**Fig 41: Another quick design, an SMA short circuit that works perfectly up to 8GHz.**



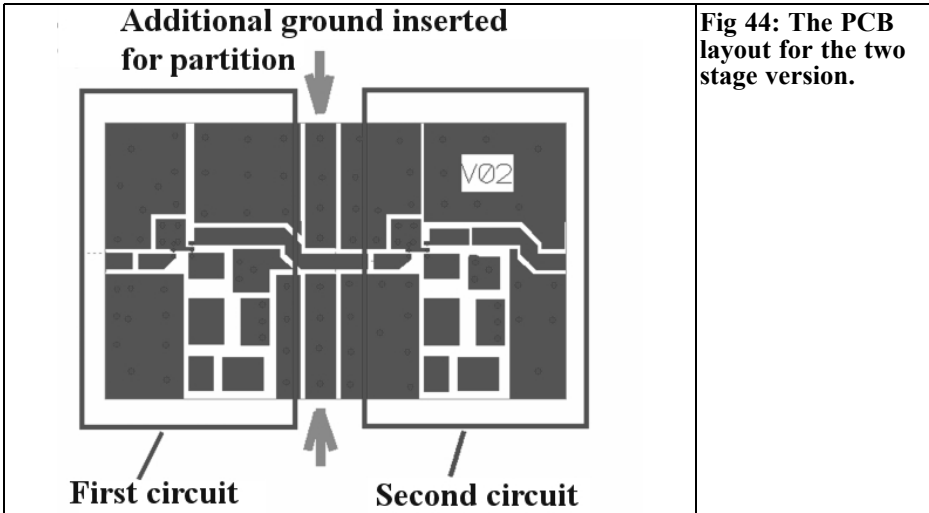
**Fig 42: S11 measured after the measuring fixture had been calibrated.**

on the measuring bridge is activated and port 1 is left "OPEN CIRCUIT". This gives total reflection and the horizontal line for total reflection or S11 is set to 0dB on the screen. For those who want to make it still better then screw on a perfect short-circuit on to port 1 - the line should not change position (the short-circuit can be made as shown in Fig 41 from a 4 hole SMA socket with a small copper plate attached with 4 screws and the centre conductor of the socket sol-

dered to the copper plate, this has been tested up to 8GHz and worked perfectly). Then the short-circuit is removed and replaced by as good an SMA dummy load as possible (the old timers already know that the best ones are the blue painted ones from Watkins Johnson). Now the self-errors of the measuring bridge are displayed on the screen and it is very pleasing, for such old equipment, to see this below -30dB up to 4GHz and even under -25dB up to 8GHz.



**Fig 43: S22 is also satisfactory.**



**Fig 44: The PCB layout for the two stage version.**

Now the measurement can begin: The dummy load is removed and screwed onto the output of the amplifier. The input of the amplifier is connected to port 1 and the S11 measurement read off the screen. The measured S11 curve is shown in Fig 42.

The S22 measurement is now a simple exercise. It is exactly as already described except the amplifier output is connected to port 1 for measurement and the 50Ω SMA dummy load is connected to the input. That produced Fig 43.

If anyone is surprised why this is made such hard work and not done by simply pressing the switches for S11 and S22 that exist on the measuring bridge:

Naturally that works but it can be shown (even with modern equipment) that the reflection factors of both ports on network analysers do not approach the quality of good dummy loads and therefore these kind of the measurements with older equipment are more exact. (for reassurance, modern equipment is not by any means better, but they possess very complex calibration and correction procedures so everything can be done at the push of a button).

## 4.

### Two-stage variant

#### 4.1. A new printed circuit board

After the success of the single-stage version and with sufficient space on the PCB it was obvious to design a further stage. The printed circuit board CAD program copy function is all that is required. After deleting the unnecessary area the space was made free for the second stage (Fig 44). Caution is required because two additional ground islands were planned to decrease the danger of oscillation. And one coupling capacitor was removed because the copy gave one at the output of the first stage as well as the input of the second stage and only one is sufficient for DC isolation.

The microstrip line (Grounded Coplanar Waveguide) is bent through 90° in two places. Therefore the models for these bends must be included in the simulation.

#### 4.2. Ansoft simulation

This is required to guarantee that the “ideal” circuit fulfils the requirements and no instability is caused by internal

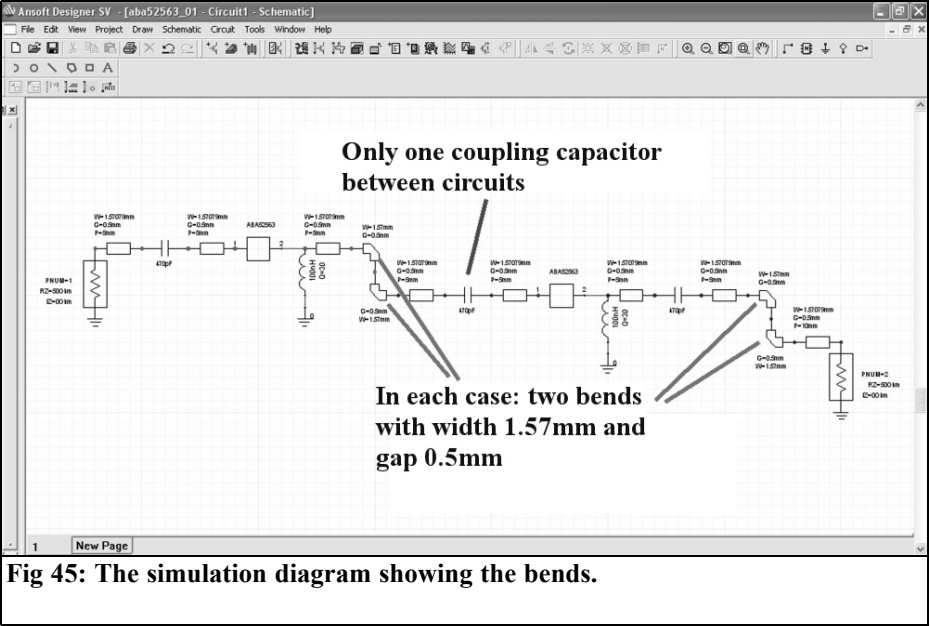


Fig 45: The simulation diagram showing the bends.

reactions between components. If oscillations do occur the problem can be solved with an improved layout, a partitioning screen and pasting attenuating foam on the cover.

The start is the complete circuit for the simulation as shown in Fig 45. The microstrip line bends already mentioned are "Mitred Bends" added from the Components library in the file "Grounded Coplanar Waveguide". Cutting the corner

off (mitring) is done for a simple reason: the current bends around the corner but it does not go into the corner. This gives a piece of copper on the top surface connected to microstrip with a ground surface below it with an insulating medium between them. This can be recognised as an additional capacitor so mitring cuts it off. The S parameter simulation (Fig 46) saves a few surprises. The gain increases to approximately 44dB; the reflections

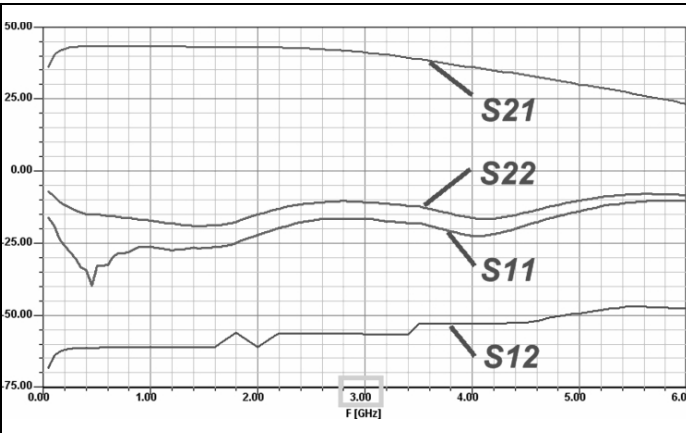
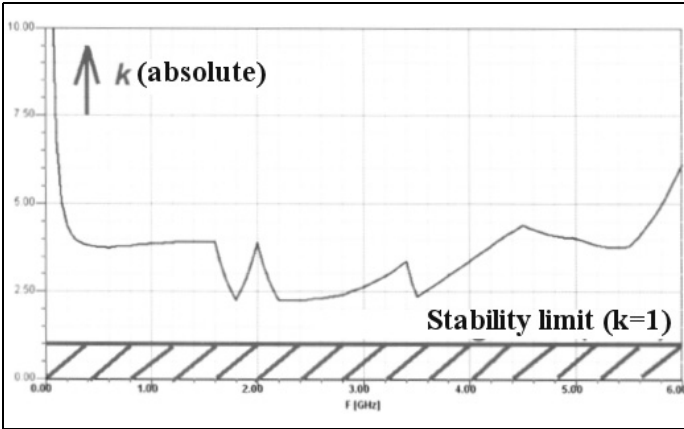


Fig 46: Simulation of the S parameters gives the all clear for further development.





**Fig 47: The stability is not a problem.**

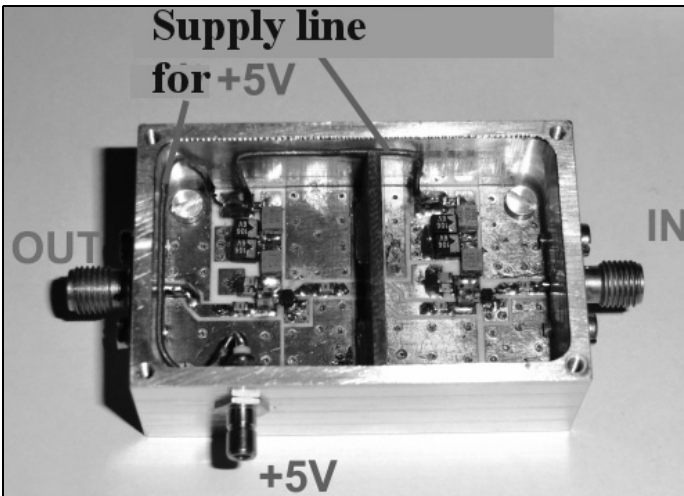
(S11 and S22) remain under  $-10\text{dB}$  and S12 under  $-50\text{dB}$ . Fig 47 shows from the stability factor  $k$  that it will be absolutely stable.

### 4.3. The practical circuit

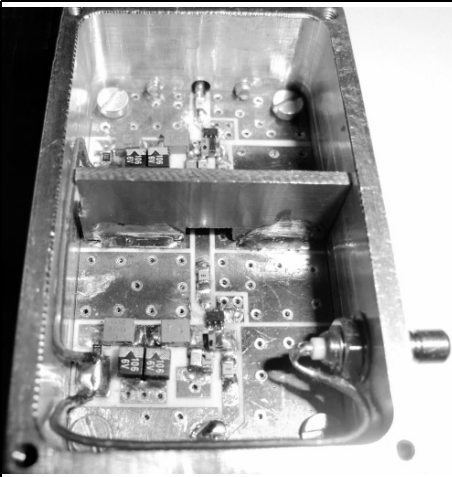
Fig 48 shows the PCB fitted into the housing with a vertical partition soldered onto the PCB. The  $+5\text{V}$  supply wire can be seen connected to the second stage. The wire is fed along the housing wall toward output (above the SMA socket) to the second stage and the on to the first stage in order to give the least opportunity for feedback from the output to the input.

Fig 49 shows how a piece of double sided board has been saw to make the partition and soldered on to the ground island to cover most of the PCB. The cut out was designed for the microstrip (it was then realised that the micro strip line does not run to the second stage in the centre of the PCB. Well; nobody is perfect).

Then the hour of the vector network analyser arrived with the cover not fitted. The S21 result, shown in Fig 46, was as expected so the housing was closed. There was a bad surprise as Fig 50 shows: clearly a breakdown (known as



**Fig 48: The two stage amplifier fitted into the housing.**



**Fig 49: The partition between the two stages was a precautionary measure.**

“Fips” by specialists) appeared at approximately 2.8GHz caused by the closed housing that works like a waveguide or as tuned cavity. If the cover is unscrewed and pushed slowly onto the housing (starting at the output side) the exact moment when the “Fips” occurs is as the cover reaches the area of the partition and it no longer changes if the cover is fully fitted. Fig 51 shows the cause of this effect: the cover forms a gap with the partition because it is lower than the surrounding housing wall. This forms a

marvellous slot antenna that transmits the output signal from the tuned cavity under the cover over the second stage back to the input.

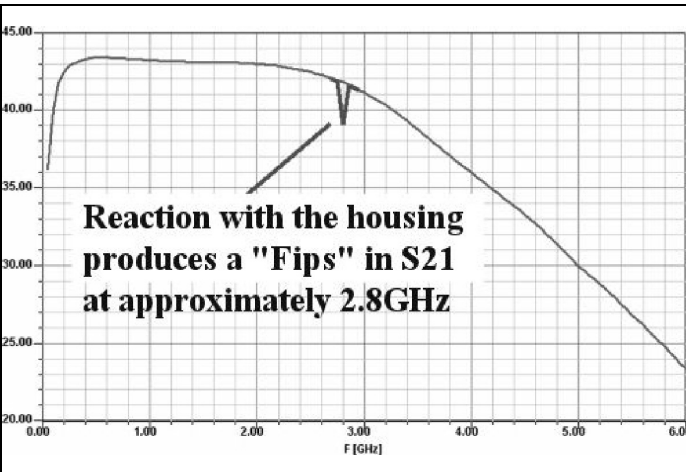
A piece of conducting foam material used to cover the pins of a DIL CMOS IC was cut and used to fill the gap (Fig 52). With this fitted and the cover attached the amplifier was checked with the network analyser. It accurately followed the simulated S21 curve results from Fig 46 without Fips!

In a quite moment the proper solution was found: a piece of this foam material cut accurately and stuck (with Pattex or UHU glue) onto the lower surface of the cover. It squeezes itself onto the partition when the cover is screwed down to reliably remove the unwanted coupling (Fig 53).

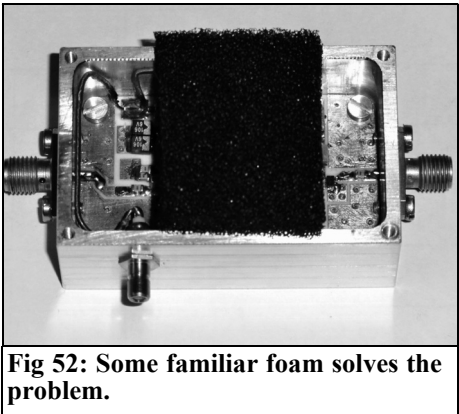
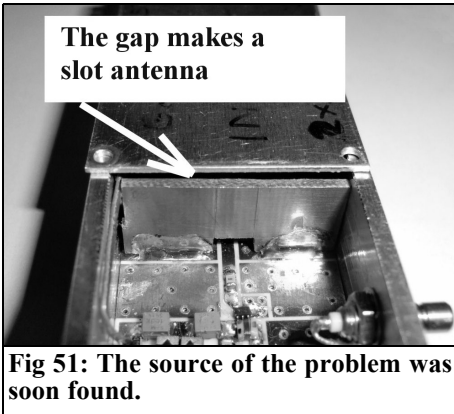
**5.**

**Summary and thanks**

Amplifier development in the GHz range has become uncomplicated and inexpensive today because of the good simulation tools available. For success, training, experience and inspiration in the use of



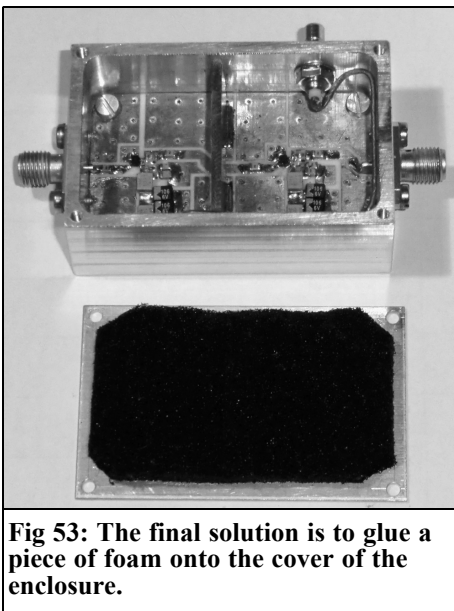
**Fig 50: An annoying problem was quickly found.**



circuit simulation is needed. The strict adherence to the rules to produce a design is an absolute “MUST”. A creative flair plus a good memory for failures and being able to learn from them are also required. The engineering students took part in a discussion following this project. The unanimous opinion being that this project was the best for the conclusion of their communications technology study.

the students who worked with the author and gave him many interesting questions. Thanks also go to the Mauritz Company in Hamburg, they are the German Rogers representatives and generously supplied the RO4003 printed circuit board needed. My colleague Martin Merkel from the electronics school Tettang was the “good guy” who etched the printed circuit boards. My colleague Harry Fimpel, who is a control engineer at the university and not an RF specialist, provided active and invaluable support to the author.

This article cannot end without thanks to



**Fig 53: The final solution is to glue a piece of foam onto the cover of the enclosure.**



Richard A. Formato, Ph.D., WWIRF

# Variable $Z_0$ - A New Antenna Design Paradigm

---

## 1.0

### Introduction

---

This note describes a new, proprietary (patent pending) antenna design and optimisation methodology, *Variable  $Z_0$* .

Traditional design and optimisation methods begin by assuming a fixed value for the feed system characteristic impedance  $Z_0$ , but doing so automatically excludes all antennas whose performance is better with a different value. *Variable  $Z_0$*  addresses this limitation by making  $Z_0$  a true variable quantity whose value is determined by the methodology.

*Variable  $Z_0$*  produces better antennas by introducing another degree of freedom into the design or optimisation space making it easier to meet any set of performance objectives.

As an example of *Variable  $Z_0$* 's effectiveness, an ultra wideband (UWB) meander monopole is optimised using Central Force Optimization (CFO).

---

## 2.0

### UWB Meander Monopole

---

#### 2.1 Optimisation Methodology

CFO is a deterministic optimisation algo-

rithm that has been applied to a variety of antenna problems as well as recognized benchmark functions [1-7]. As an example of applying *Variable  $Z_0$*  to an antenna optimisation problem CFO/ $VZ_0$  was applied to the design of a meander monopole on a PEC (perfectly electrically conducting) ground plane. Other examples employing Yagis and loaded bowties appear in [8-10], which also discuss *Var  $Z_0$*  in greater detail.

One of the major advantages of a deterministic algorithm is that it always returns the same result with the same setup parameters. This attribute makes optimising an antenna much easier, because changes in antenna performance cannot be the result of the optimiser's inherent randomness (for example, a Genetic Algorithm or Particle Swarm Optimisation, both of which are stochastic). Determinism is especially important in defining the "fitness function" against which the antenna is optimised (see [11] for a more detailed discussion of this question).

#### 2.2 MM Fitness Function

The general objective of the meander monopole (MM) optimisation is maximum impedance bandwidth (IBW) with good gain. The MM fitness function therefore was chosen to be the weighted gain-VSWR quotient defined as

$$F = \sum_{i=1}^N \frac{w_g(f_i) \cdot G_{\max}(f_i)}{w_{VSWR}(f_i) \cdot VSWR // Z_0(f_i)}$$



where

$$w_g(f_i) = \frac{(w_g^{\max} - w_g^{\min})(f_U - f_i)}{f_U - f_L} + w_g^{\min}$$

$$w_{VSWR}(f_i) = \frac{(w_{VSWR}^{\max} - w_{VSWR}^{\min})(f_U - f_i)}{f_U - f_L} + w_{VSWR}^{\min}$$

The MM fitness was evaluated at equally spaced frequencies between lower and upper frequency limits  $f_L$  and  $f_U$ . The antenna's performance was evaluated using the Numerical Electromagnetics Code Ver. 4.2 [12-14]. Total power gain (same as directivity in this case) was computed in NEC's standard spherical polar coordinates at 10 degree increments in the polar angle  $\theta$  for two values of the azimuth angle  $\phi$ , broadside ( $\phi=0$ ) and endfire ( $\phi=90^\circ$ ) to the MM (see Fig 1 for geometry).  $G_{\max}$  is the maximum gain over these angles.  $VSWR/Z_0$  is the voltage standing wave ratio relative to the feed system characteristic impedance  $Z_0$ .

The MM gain-VSWR quotient contains frequency-dependent weighting coefficients  $w_g$  for gain and  $w_{VSWR}$  for VSWR. Each of these coefficients decreases linearly with increasing frequency. Of course, the antenna designer is free to choose any form for the fitness function, and changing its form changes the design or, in the case of optimisation, the decision space's topology, so that the antenna(s) meeting the performance objectives or doing so optimally will be different in the different landscapes. In the MM example, the fitness function was chosen empirically for its simplicity, as were the linearly tapered weights.

### 2.3 Variable $Z_0$

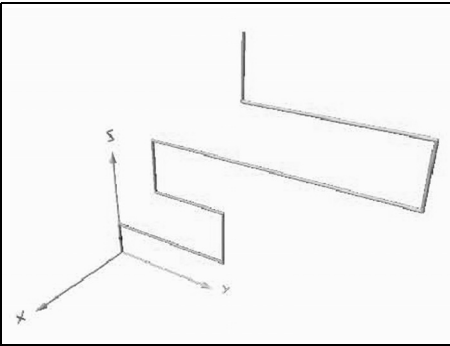
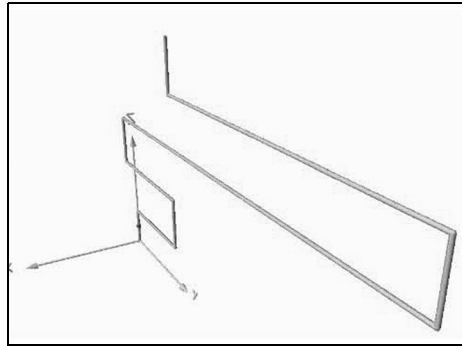
The concept underlying *Variable  $Z_0$*  is extraordinarily simple, and it is rather surprising that it has been overlooked through decades of antenna design and optimisation. All the usual approaches start with an assumed value for  $Z_0$  (even if multiple procedures are employed using different parametric values). Fixing

$Z_0$  inevitably makes it more difficult to meet specific antenna performance goals because that very assumption automatically excludes every better design.

An antenna's performance is determined by its current distribution, which, in turn, determines its input impedance. The objective therefore is discovering a structure whose current distribution meets minimum user-specified performance goals (design) or best meets them (optimisation). The current distribution that meets this objective is entirely independent of the feed system characteristic impedance. By constraining a design or optimisation methodology to produce only current distributions that are matched to  $Z_0$  to the degree possible eliminates all distributions that do a better job of meeting the performance goals.

In contrast, allowing  $Z_0$  to "float" as a true variable quantity places no constraint on allowable current distributions. Once an acceptable distribution or the optimal distribution is discovered, the value of  $Z_0$  is determined automatically by the distribution.

*Variable  $Z_0$*  technology can be applied to any antenna design problem against any fitness function or set of performance goals (although *Var  $Z_0$*  may be especially useful for improving IBW). *V $Z_0$*  moreover is a "product by process" approach that can be used in conjunction with any design or optimisation methodology, deterministic ones like CFO; stochastic algorithms like Particle Swarm, Ant Colony, Group Search Optimisation, Differential Evolution, or Genetic Algorithm; analytic approaches such as extended Wu-King impedance loading [5]; even "seat of the pants" design or optimisation based on experience, intuition, or a "best guess." The specific design or optimisation methodology is entirely irrelevant to the novelty and utility of treating  $Z_0$  as a design *variable* instead of a fixed parameter.

Fig 1a: *Var*  $Z_0$  MM Geometry.Fig 1b: Fixed  $Z_0$  MM Geometry.

## 2.4 Meander Monopole Geometry

In order to demonstrate *Variable*  $Z_0$ 's effectiveness, the MM was CFO-optimised with and without *Var*  $Z_0$ . The *Var*  $Z_0$  run allowed variable  $25 \leq Z_0 \leq 500 \Omega$ , while for the Fixed  $Z_0$  run  $Z_0 = 50 \Omega$ . The antenna was optimised between 2 and 12GHz with a height constraint of a quarter wavelength at 2GHz and maximum width of one half wavelength.

Perspective views of the optimised Meander Monopole geometries visualised using 4NEC2 [15] appear in Fig 1. The corresponding NEC input files defining the geometries appear in Fig 2. The two antennas are quite different, yet the only difference in the optimisation setup is

allowing  $Z_0$  to vary in one case while it was fixed in the other. All CFO parameters were otherwise the same.

The value of  $Z_0$  determined to be optimum by CFO is  $Z_0 = 263.91 \Omega$ . Of course, feeding this MM from a  $Z_0 = 50 \Omega$  feed, which is the most common feed system characteristic impedance, requires a ~5:1 broadband transformer or matching network. Low-loss UWB matching systems are readily available, so that implementing this MM should be straight-forward. But if it happens that the optimised value of  $Z_0$  is unacceptably high or low, then *Var*  $Z_0$  still can be used simply by restricting  $Z_0$ 's range to acceptable values.

```

CM File: MEANDER.NEC
CM MEANDER LINE ON PEC GND PLANE
CM Zo=263.91 ohms
CM Note: All dimensions are in METERS.
CE
GW1,9,0.,0.,0.,0.,0.,0.,006,.00025
GW2,9,0.,0.,0.,006,0.,.022,.006,.00025
GW3,9,0.,.022,.006,0.,.022,.015,.00025
GW4,9,0.,.022,.015,0.,.009,.015,.00025
GW5,9,0.,.009,.015,0.,.009,.024,.00025
GW6,9,0.,.009,.024,0.,.05,.024,.00025
GW7,9,0.,.05,.024,0.,.05,.033,.00025
GW8,9,0.,.05,.033,0.,.025,.033,.00025
GW9,9,0.,.025,.033,0.,.025,.042,.00025
GE1
GN1
EX 0,1,5,1,1,.0.
FR 0,1,0,0,2000,.0.
RP 0,10,2,1001,0.,0.,.10,.90.,100000.
XQ
EN

```

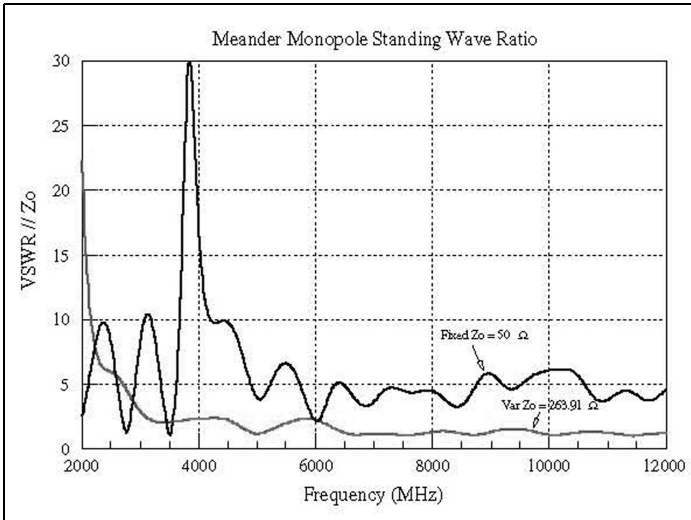
Fig 2a: *Var*  $Z_0$  MM NEC File.

```

CM File: MEANDER.NEC
CM MEANDER LINE ON PEC GND PLANE
CM Zo=50 ohms
CM Note: All dimensions are in METERS.
CE
GW1,9,0.,0.,0.,0.,0.,006,.00025
GW2,9,0.,0.,0.,006,0.,.016,.006,.00025
GW3,9,0.,.016,.006,0.,.016,.014,.00025
GW4,9,0.,.016,.014,0.,-.004,.014,.00025
GW5,9,0.,-.004,.014,0.,-.004,.022,.00025
GW6,9,0.,-.004,.022,0.,.065,.022,.00025
GW7,9,0.,.065,.022,0.,.065,.03,.00025
GW8,9,0.,.065,.03,0.,.016,.03,.00025
GW9,9,0.,.016,.03,0.,.016,.038,.00025
GE1
GN1
EX 0,1,5,1,1,.0.
FR 0,2,0,0,2000.,4.545455
RP 0,19,19,1001,0.,0.,.5,.10.,100000.
XQ
EN

```

Fig 2b: Fixed  $Z_0$  MM NEC File.



**Fig 3: Meander Monopole VSWR.**

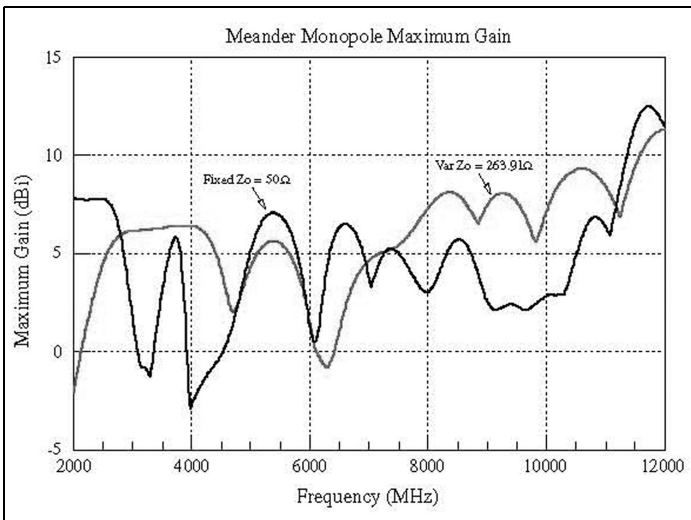
The effect of *Variable Z<sub>0</sub>* methodology is evident in the NEC4.2 MM data. The two parameters of interest, VSWR and maximum gain, are plotted in Figs 3 and 4, respectively. *VZ<sub>0</sub>* performance is plotted in grey, while the Fixed Z<sub>0</sub> curve is black. The *VZ<sub>0</sub>* MM is obviously superior to its Fixed Z<sub>0</sub> counterpart, especially with respect to VSWR, which is much lower and flatter across the entire UWB spectrum (3.1-10.6GHz). Similarly, the maximum gain is generally higher at

most frequencies, and the minima generally are no lower than the Fixed Z<sub>0</sub> antenna's.

### 3.0

## Conclusion

*Variable Z<sub>0</sub>* is a simple and effective methodology for creating antennas de-



**Fig 4: Meander Monopole Max Gain.**



signed or optimised against any set of performance objectives. Its use is straight-forward, and it is universally applicable regardless of the methodology being used. *Variable  $Z_0$*  is a proprietary (patent pending) technology, and *Variable  $Z_0$* , *Var  $Z_0$* , *VZ<sub>0</sub>*, and *“Variable  $Z_0$  Inside”* are trademarks and service marks of *Variable  $Z_0$* , Ltd., P.O. Box 1714, Harwich, MA 02645 USA. Royalty-free licensing is available for experimental and amateur radio use as long as using *Variable  $Z_0$*  is acknowledged by appropriately marking the resulting antenna and including written acknowledgement in any written or published works or materials. Royalty-free licensing requests must include a description of the proposed use. Please email them to [variable\\_z0@yahoo.com](mailto:variable_z0@yahoo.com). Commercial license inquiries should be sent to that address as well.

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## 4.0

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Livermore National Laboratory, Livermore, California, USA.

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## Amateur Television Quarterly

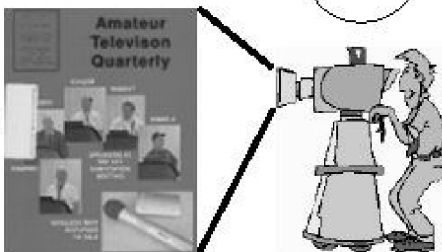
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Andrea Daretti, IZ2OUK and Gianfranco Canale

# A phase meter: a help to synchronize oscillators to GPSDO

## 1.0

### Introduction

The idea was born a long time ago, when, after building the firsts GPS Disciplined Oscillators (GPSDO), we tried to synchronise ours and our friend's quality oscillator, i.e. to tune the oscillators as close as possible to the frequency of the GPSDO.

In general the oscillators to be tested are top class 10MHz oscillators. A simple procedure was tried using a Lissajous figure on an XY scope, by careful fine tuning you can reach a precision of synchronisation in the order of  $10^{-10}$ Hz to the GPSDO.

At these levels the 1PPS GPS signal should be considered with due care. Everybody knows that this signal is very precise, only if averaged on a pretty long time ( see paper of Brooks Shera QST March 1998). In real life the GPS signal is affected by all the disturbances that Mother Nature puts between the satellites and us.

Generally speaking the procedure is as simple as sending both the GPS and our oscillator signal to the X-Y axis of a scope (with BW > 10MHz) and observing the Lissajous figure. When the two frequencies are close, the figure

changes and looks like a circle-ellipses-line-circle rotating at a decreasing speed as the frequency difference decrease; rotation should stops when you get perfect synchronisation. You (almost) never get this.

Even if the two oscillators are of excellent quality/stability, there will almost always be a very small frequency difference (e.g. 0.01Hz) between the two oscillators and that will lead to very slow rotations. On a given (the longer the better) time base the number of rotations gives the frequency difference.

If one full rotation is performed in 100sec, with 10MHz oscillators we are in the order of  $10^{-9}$  frequency difference. Trying to get to  $10^{-10}$  we need to get one full rotation in 1000sec i.e. 17min.

Are you willing to stay in front of a scope for 17 minutes to check the figure rotation, and then make a very small adjustment, and then wait another 17 minutes?

No sexually mature person intends to waste time this way!

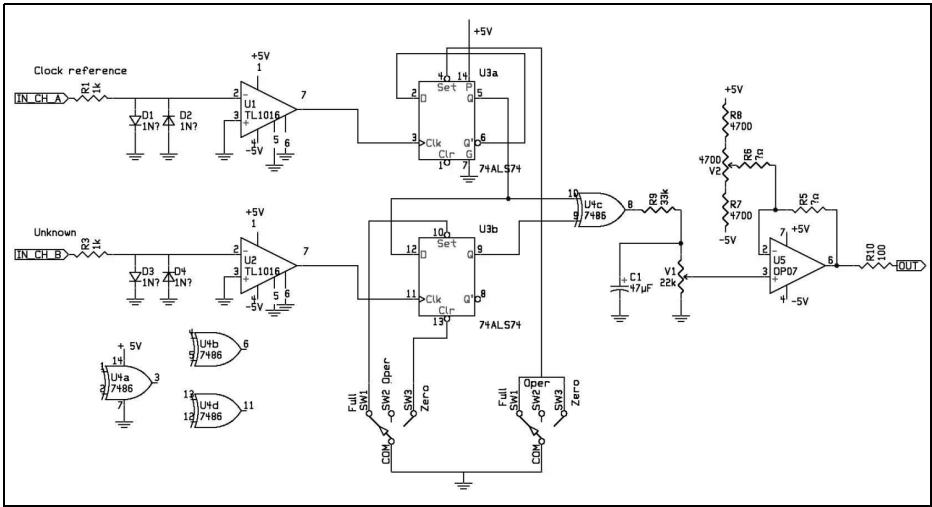
But since

$$f = \frac{d\phi}{dt}$$

$f$  = frequency

$\phi$  = phase

it suggests that a good phase



**Fig 1: Circuit diagram of the phase meter.**

measurement may be easier to measure than frequency. From its variation with the time (speed of rotation), we get to the frequency and there we are.

Typically it happens that with these oscillators the sense of rotation is not unidirectional, but it slowly changes CW (Clock Wise) and CCW (Counter Clock Wise) in an unexpected way, indicating very small frequency increases and decreases. As an example, as soon as you open the window of your lab, and change the room temperature, the frequency will have a small change, and if you are close to synchronisation, probably you'll see a change of sense of rotation.

For this reason you cannot blindly count the number of rotations (on a time base) and infer that this is the difference in frequency (on that specific time base). You should count CW rotation and subtract CCW rotations (or vice versa).

But this clever counting is another story; it is a future project that in our next life (we believe in reincarnation) we intend to solve, maybe using Arduino.

For the time being, we limit our project to the phase measurement and see how it

changes (rotate) to infer frequency difference, still keeping an eye to the next digital step and the above mentioned clever rotation counting.

## 2.0

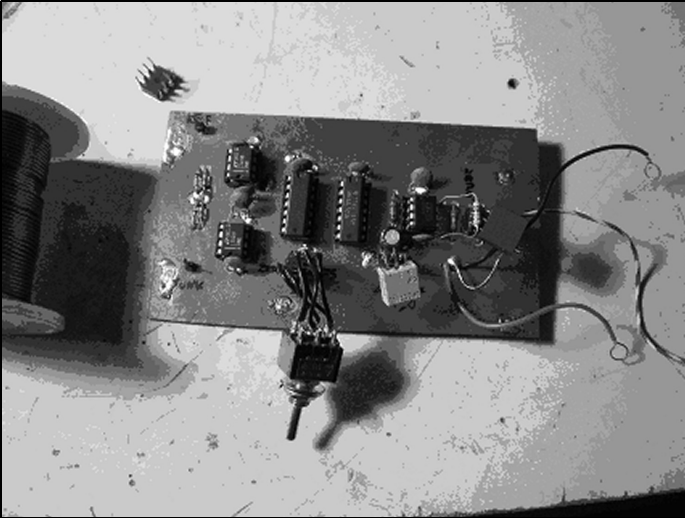
### The project.

A design for a phase meter was published in QEX (Nov/Dec 2010) by Dave Bowker K1FK.

A good project indeed, but with a different target than ours: it was designed mostly to measure phase difference between two cables and limited to 180°.

Beside phase quantisation, our project requires:

- Phase measurement of a signal compared to a reference
- Extend the measurement to 360° phase difference.



**Fig 2: Picture of the component side of the prototype.**

- Have the possibility to record the analogue phase difference signal and, later on, have an option to upgrade to some digital form.

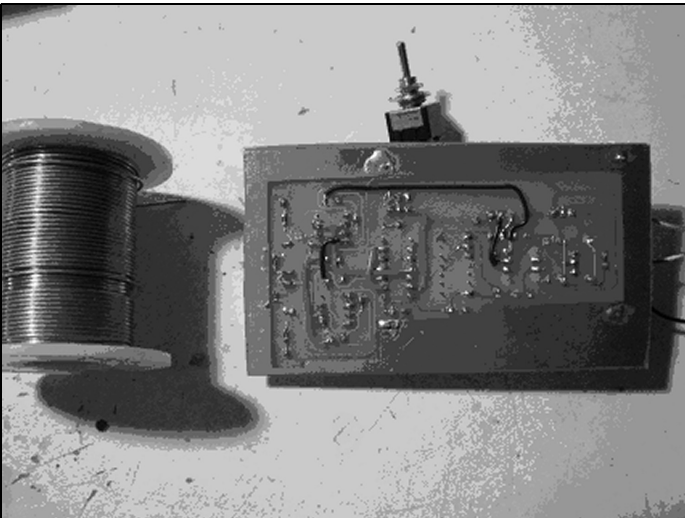
With these targets in mind, we started modifying K1FK's project as follows:

**Reference signal:** We selected one of the two inputs and take it as the reference, and start from this signal for the phase measurement: from the "reference start" until the "unknown signal start" is

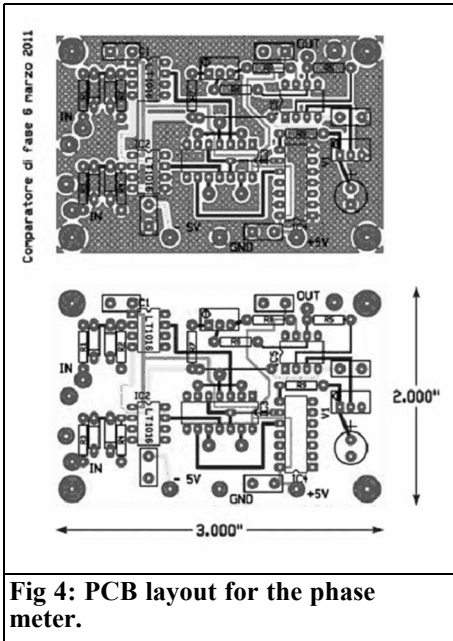
performed by two 74ALS74s. This is why you will see in the circuit the link between U1a "Q" to U1b "D". The circuit diagram is shown in Fig 1.

**To get a 360° range:** the original frequency is divided by two so that 179.9° difference for  $f/2$  is 359.8° for original signals.

A later version will include a digital option, including intelligent "zero crossing" counting, adding CW zero



**Fig 3: Picture of the wiring side of the prototype.**



crossing (phase increase) and subtracting CCW zero crossing (phase decreasing) integrated on a variable time base long enough (hundreds of seconds) to make the measure meaningful.

### 3.0

#### Technical details.

The “Clock reference (IN CH A)” is the reference signal, and the “Unknown (IN CH B)” signal is measured compared to that. Both signals, clipped by two diodes D1-D4, are fed to the two operational amplifiers U1-U2 ( LT1016) fast enough not to loose even small phase differences. The reference signal goes to U3a and sets U3a Q HIGH, which sets HIGH the Output of the “Exclusive OR” U4c that is sent to the following integrator C1/V1 (//R9).

When we get the unknown signal on the Q output of U3b, it close U4C and

creates a pulse with a duration proportional to the phase difference, consequently the integrator gives a DC signal proportional to it. U4 is just a buffer controlling to the zero and scale factor suitable for the output meter.

U3a and U3b divide the input frequency by two allowing the pulse arriving at U4c to be proportional to the phase difference up to 360°; without this division the phase difference will be limited to 180° as on K1FK paper. The prototype is shown in Figs 2 and 3.

### 4.0

#### Component description

U1-U2 are two fast comparators TL1016 that you can find at RS, code 545-4799

U3 is a 74LS74, not critical but should be fast.

U4 is a non critical and a basic 7486

R5 – R6 have a value to be defined by the requirements of the output meter. That value can be easily calculated with formulas you can find in any Op Amp manual and is defined by the full scale voltage required by the output meter / display.

R10 is a simple output protection resistor.

The switch sw1-2-3 is used to set the full-scale indication (sw1) or enable reading (sw2) or zeroing by means of V1 (sw3)

The power supply is dual and doesn't need special care, besides being well stabilised and filtered.

PCB has been designed (Fig 4) with CIRCAD and upon request the file can be e-mailed (ask Gianfranco gf.canale@libero.it).



Geoff Pike, G10GDP

# A Useful Gain Block for the Radio Amateur

## 1.0

### Introduction

A pair of cascaded BGA-616 MMICs from Infineon provides ample gain and power output to 4GHz and beyond. These devices are available from RS at approximately £1 in small quantities.

## 2.0

### Reason for building

I was made aware of these devices from

an article by Chris Bartram.

They are easy to work with and seem very robust. My amplifier data is taken from the Infineon website where both the S-parameters and Spice data are made available. The circuit is shown in Fig 1.

Originally the devices were to be used with pin diodes to produce weak signals at 10GHz, this project did not go well and the PCB was left to one side.

As my HP signal generator was failing in output at >1GHz it was obvious that a small amplifier would restore some of the output, which it did and I don't think I will bother to get inside the HP8657B to fix the doubler.

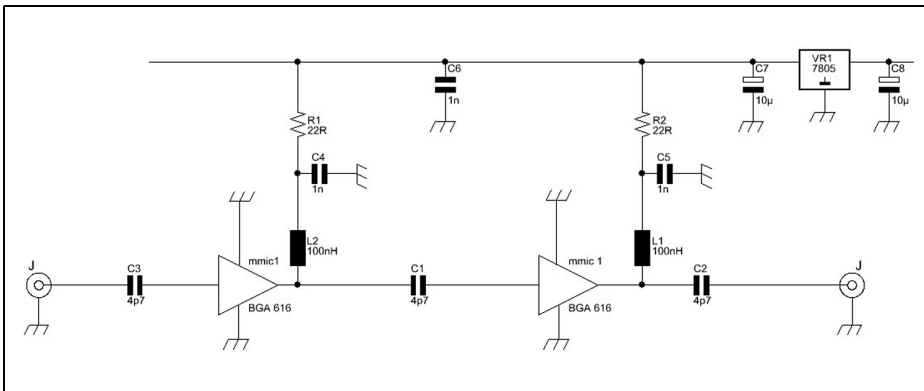
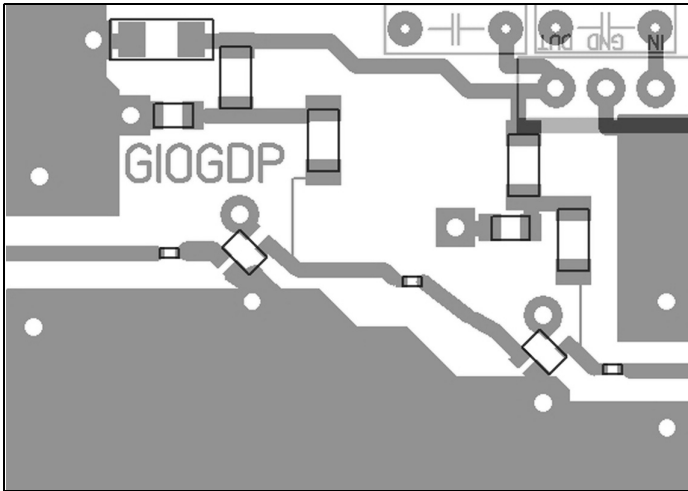


Fig 1: Circuit diagram of the amplifier.



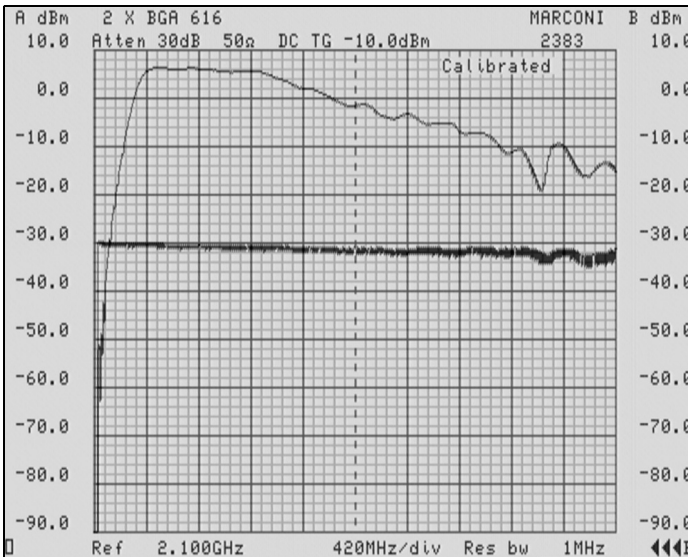
**Fig 2: PCB and component layout for the amplifier.**

### 3.0 Construction

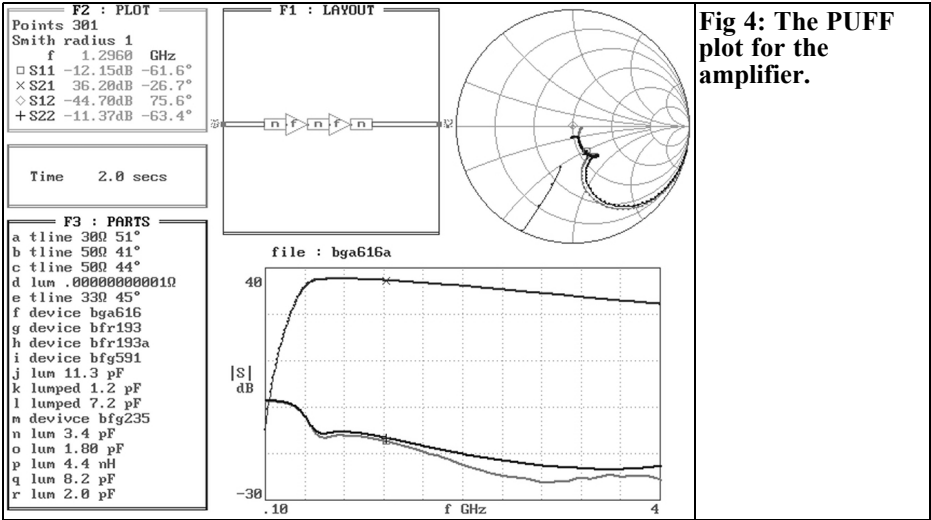
I made up a simple PCB from 0.8mm double-sided FR4 board (Fig 2). I used a 78L05 regulator and reduced the feed resistors from 33Ω to 22Ω.

The PCB chokes are probably of no use;

it was just an artefact from a previous project. In fact to enhance the high end performance the board needs a serious re-think. The 4p7 coupling capacitors produce falling gain at about 350MHz, so if you want to use it 144MHz then these would need changing to say 10pf.



**Fig 3: Measured frequency response of the amplifier.**



**Fig 4: The PUFF plot for the amplifier.**

### 4.0

### Testing

The amplifier is very stable, gain is excellent at 36dB at 1296MHz and saturates at 17dBm and however it's already in gain compression at this point. The gain falls off as expected with frequency (Fig 3), but if you compare the Puff plot (Fig 4) with the analyser then it is obvious that better caps and PCB would improve the situation, and also the PCB lines are not 50Ω

Current draw is about 120mA from a 12v

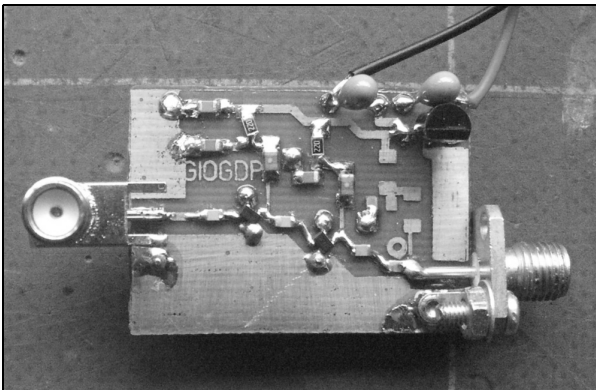
supply. A picture of the amplifier is shown in Fig 5.

### 5.0

### Conclusion

A handy little utility amplifier for signal generators and low level stages in transverters and perhaps LO amplifiers from driving high-level mixers.

Perhaps the noise figure is low enough to be used for early stages in a receiver, the choice is yours.



**Fig 5: A picture of the completed amplifier.**





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2006	Y	Y	Y	Y
2005	Y	Y	Y	Y
2004	Y	Y	Y	Y
2003	Y	Y	Y	Y
2002	Y	Y	Y	Y
2001	Y	Y	Y	Y
2000	Y	Y	Y	Y
1999	Y	Y	Y	P
1998	Y	Y	Y	Y
1997	Y	Y	P	Y
1996	Y	Y	Y	Y
1995	P	Y	Y	Y
1994	Y	Y	Y	Y
1993	Y	P	P	P
1992	Y	Y	Y	Y
1991	P	P	P	P
1990	P	P	P	P
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1987	P	P	P	P
1986	P	Y	Y	Y
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1983	P	P	Y	Y
1982	P	P	P	P
1981	P	L	P	P
1980	P	P	P	P
1979	P	P	P	P
1978	P	P	P	P
1977	P	P	P	P
1976	P	P	P	P
1975	P	P	P	P
1974	L	P	P	P
1973	P	P	P	P
1972	P	P	P	P
1971	P	P	P	P
1970	P	P	P	P
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Ralph Berres, DF6WU

# YIG Filter with calibration memory

## 1.

### Introduction

I have had a Takeda Riken TR4111 spectrum analyser as one of my measuring instruments for some time. This has three frequency ranges 10kHz to 2GHz, 1.5GHz to 3.5GHz and 2.5 to 4.5GHz.

The range 10kHz to 2GHz has a high first IF of 2050MHz and therefore does not have any image frequency products.

The two upper frequency ranges are mixed directly to a second IF of 540MHz and are ambiguous because of the image frequency products. This is not really usable; the remedy is a YIG filter for these two ranges.

An inexpensive 2 pole YIG filter for the

range from 2 to 4GHz was obtained from surplus (Fig 1). Tests resulted showed that it was usable outside this in the range from 1.5GHz to 4.5GHz. The attenuation change was only noticeable at the edges of this range.

The YIG filter gives no improvement by itself. Thus a controller must be developed that generates a frequency related control voltage for the YIG filter from the saw tooth voltage of the internal YIG oscillator.

## 2.

### Preliminary tests

First, a circuit was developed that converts the internal saw tooth voltage from

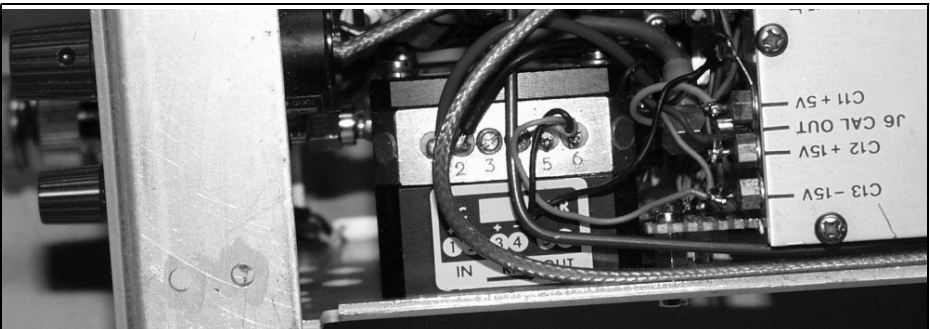


Fig 1: Picture showing the YIG filter.

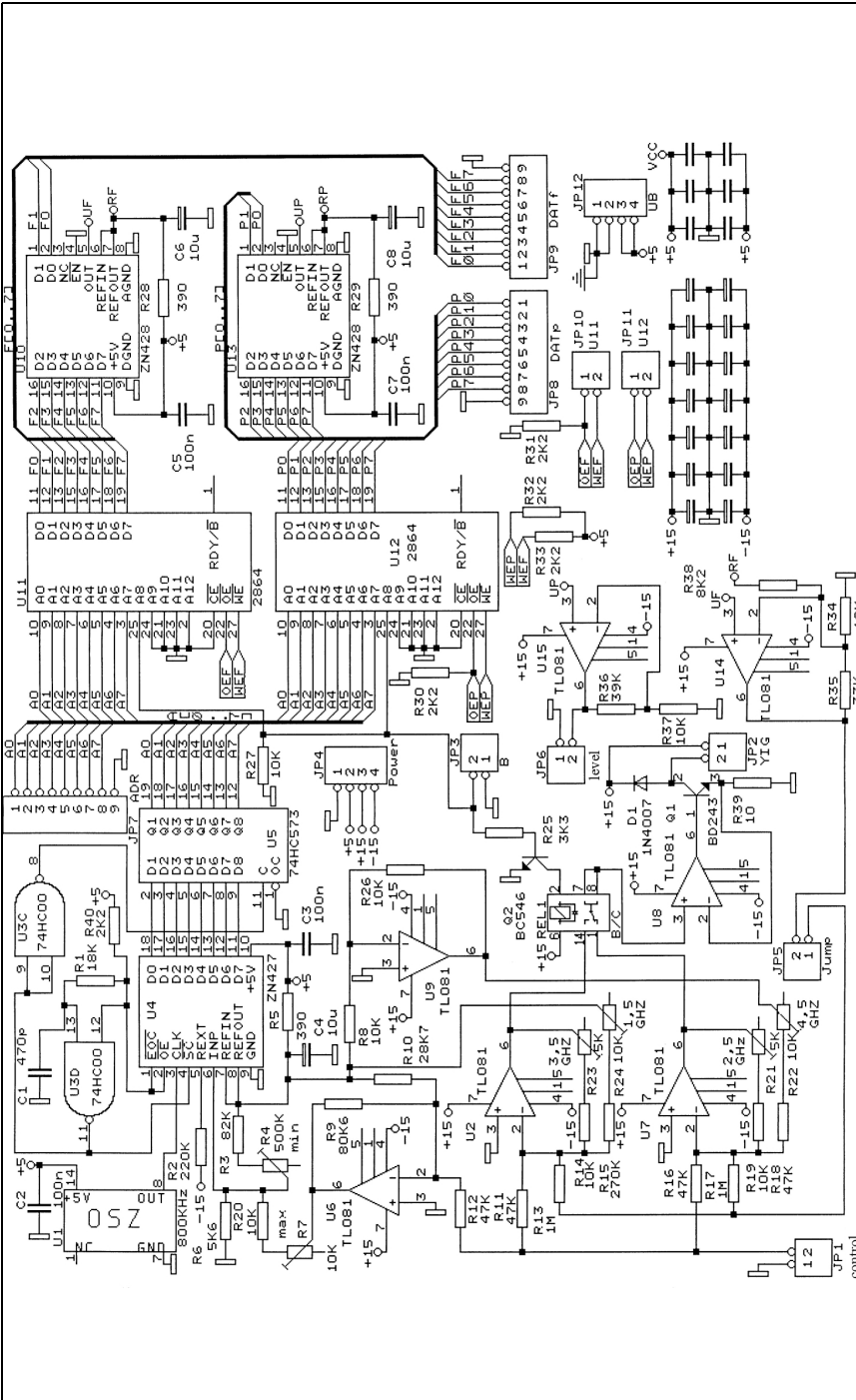
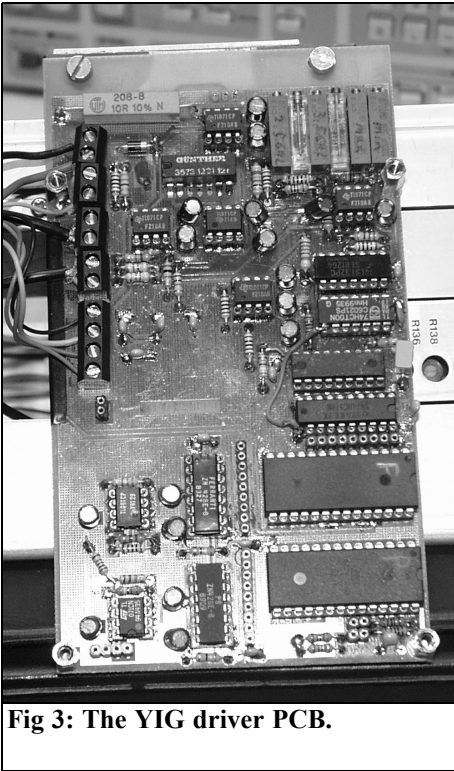


Fig 2: Circuit diagram for the YIG driver PCB.

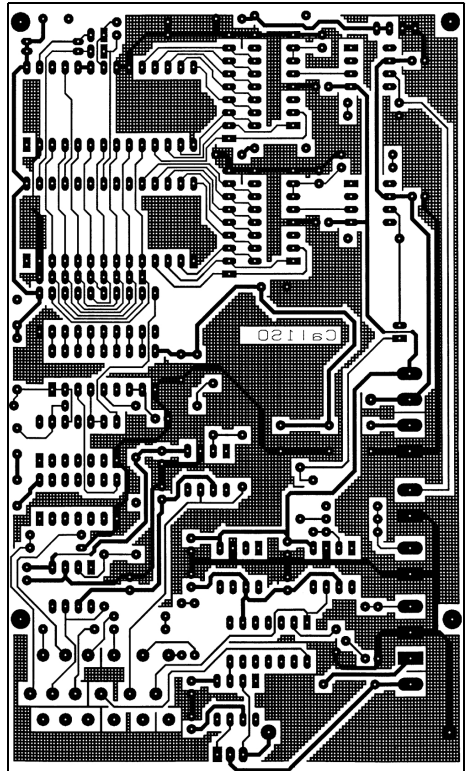


**Fig 3: The YIG driver PCB.**

-4V to -10V into a proportional current for the two upper frequency ranges. For each range the start and end current for the YIG filter can be adjusted separately.

The disillusionment came after the controller was installed into the spectrum analyser and aligned for the frequency ranges. The amplitude response varied by approximately  $\pm 8\text{dB}$  over the frequency range; that is not acceptable. It needed some kind of correction over the frequency range.

This generated the idea of correction values for the attenuation of the YIG filter over both frequency ranges held in an EEPROM.

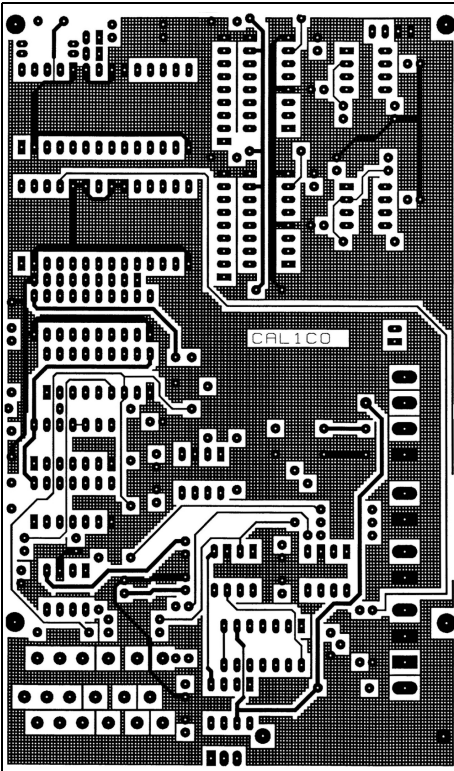


**Fig 4: Lower side PCB layout for the YIG driver (90mm x 160mm).**

### 3.

## Design of the YIG filter driver PCB

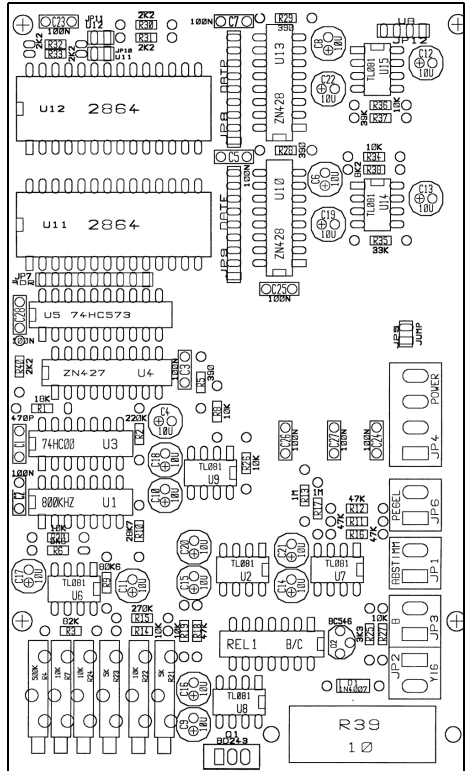
The circuit diagram for the YIG filter driver is shown in Fig 2. The resolution for digitising the saw tooth voltage that drives the YIG filter must first be decided. The scan width for both frequency ranges is approximately 2000MHz. The YIG filter has bandwidth of approximately 8 to 12MHz depending on the frequency.  $2000\text{MHz}/8\text{MHz}$  results in 250 steps. Thus the resolution of an 8-bit A/D converter is sufficient. A ZN427 A/D converter from Ferranti was selected. Trimmers R7 and R4 are used to



**Fig 5: Top side PCB layout for the for the YIG driver (90mm x 160mm).**

adjust the input level range of the A/D converter to the level range of the saw tooth voltage.

The data from the A/D converter is fed directly to the address inputs of the two EEPROMs that store the correction values of frequency and level in each case. The address data is also fed to a connector for the external programming PCB. The data outputs of each EEPROM are connected to a ZN428 D/A converter and to the connector for the external programming PCB. The output voltage for the frequency correction from the D/A converters is fed to the summing amplifier U2 or U7 to control the YIG filter. The relatively high value resistor of 1MΩ ensures that the maximum correction tuning range from the D/A converter is



**Fig 6: Component layout for the YIG driver PCB.**

approximately  $\pm 12\text{MHz}$ . A digital step corresponds to approximately 100kHz.

The correction value from the ZN428 D/A converter is an analogue signal in the range from 0 to 10V. This is fed to a pin diode attenuator at the output of the IF module.

Address line 9 of the EEPROM stores the range 2.5GHz or 4.5GHz.

Input B (JP3) switches both address line 9s of the EEPROMs and a relay that switches between the summing amplifiers U2 and U7. This was necessary in order to be able to adjust both frequency ranges separately for the lower and upper YIG filter frequencies.

28C64 EEPROMs are used because they are readily available. An EEPROM with



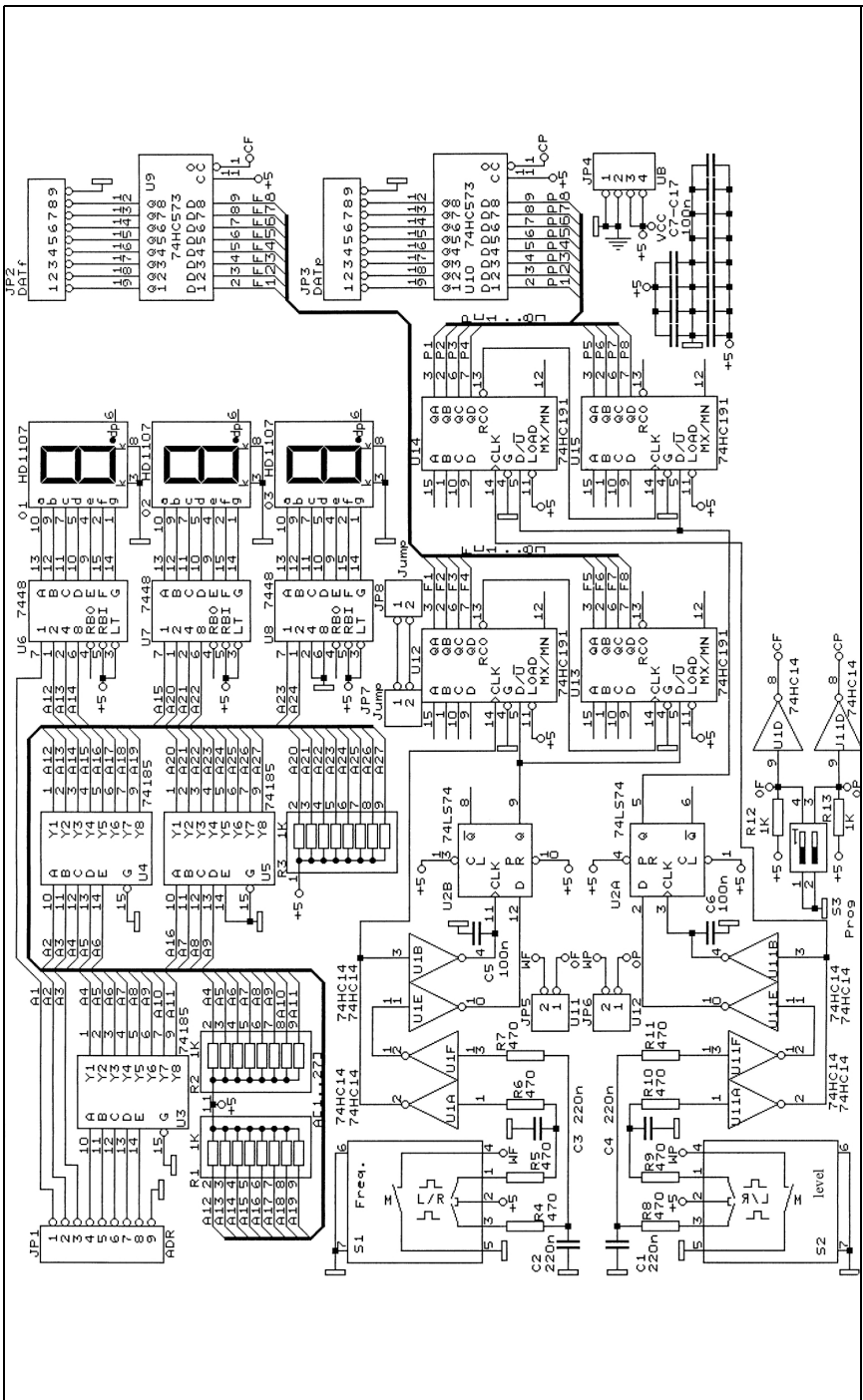
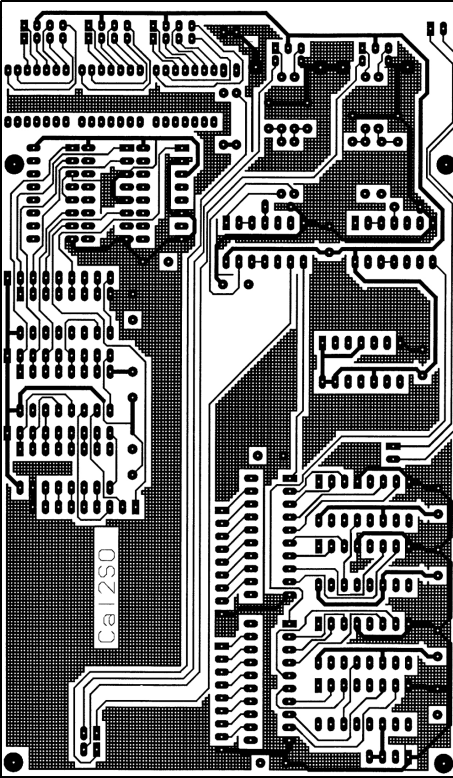


Fig 7: Circuit diagram for the YIG programming PCB.

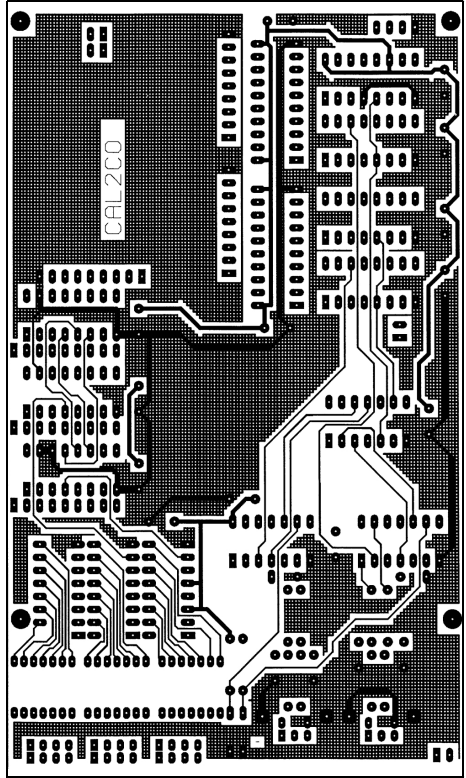


**Fig 8: Lower side PCB layout for the YIG programming PCB (90mm x 160mm)**

parallel data and address lines is clearly an advantage because the complete circuit can operate without a microprocessor.

OP07 operational amplifiers were used for the ramp signal level adjustment by the D/A converter, YIG filter control and pin diode attenuator. In the circuit diagram these are shown as TL081, the OP07 is pin compatible but has a worse drift specification than the TL081.

R39 is a 10 $\Omega$  5W temperature stable resistor; the maximum temperature coefficient must be 10ppm. An Isabellenhütte type PBV-Z R1 10R0 0.05% TK05 resistor was used in the prototype. (A normal ceramic resistor is shown in Fig 3).



**Fig 9: Top side PCB layout for the YIG programming PCB (90mm x 160mm),**

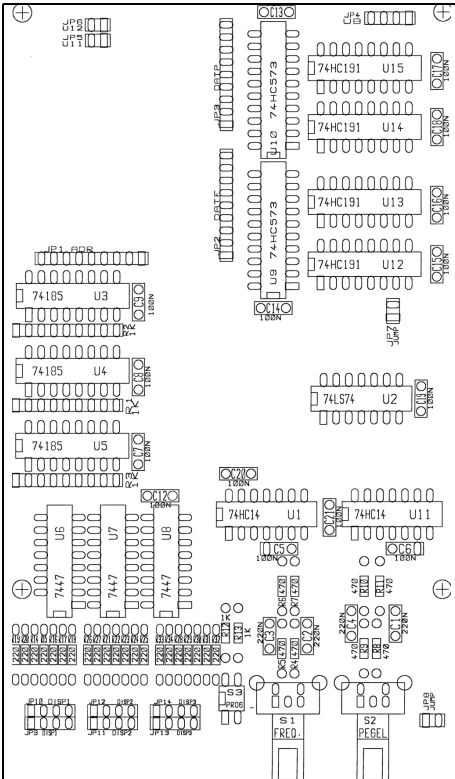
The end frequency of the two frequency ranges is adjusted with the trimmers R21 - 24.

The PCB layout for the YIG filter driver is shown in Figs 4 - 6.

#### 4.

### Design of the programming PCB

Another PCB was required to load data into the EEPROMs that would piggyback onto the driver PCB. The circuit diagram for the programming PCB is shown in

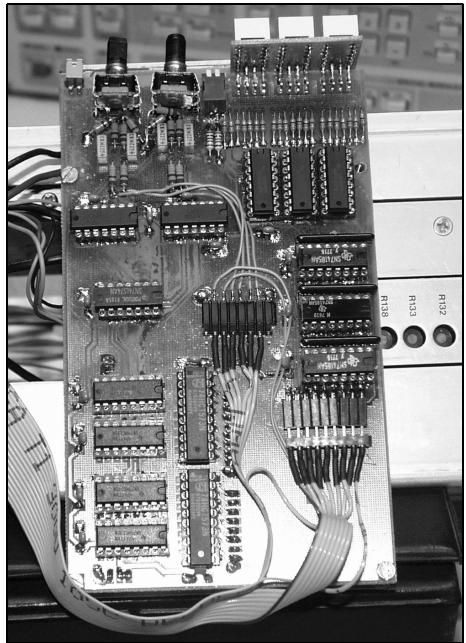


**Fig 10: Component layout for the YIG programming PCB.**

Fig 7. After successful programming it can be removed. It provides the following functions:

- Decoding and display of the EEPROM on a 3 digit display.
- Generate the digital correction values for level and frequency using two rotary encoders.
- Store the correction values into the address while it remains static.

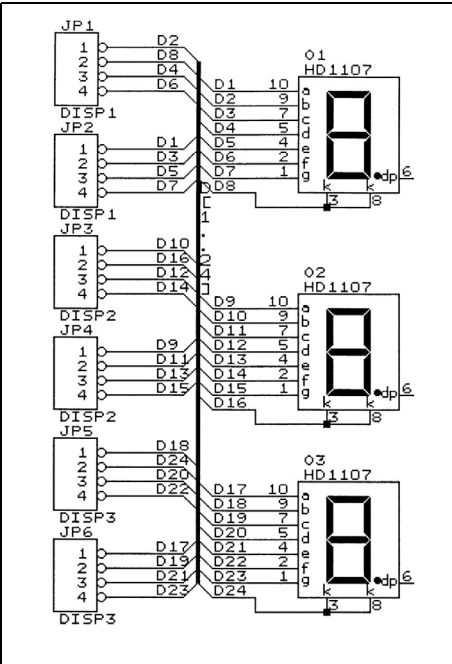
Decoding the address of the EEPROMs is done with three special binary to BCD decoders, type 74185 that are unfortunately difficult to find today. The BCD code is converted with three 7448s into seven segment code for the display. This could all be done with a GAL if necessary.



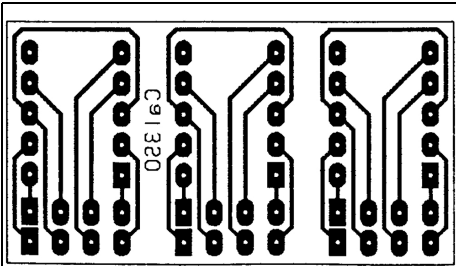
**Fig 11: The YIG programming PCB.**

The pulses from the rotary encoders are digitised with D type flip-flops and some inverters into counting and counting direction pulses that feed data to the EEPROMs via the 74191 binary counters. The 74573 are tri-state drivers for the output. In operating mode the data lines of the EEPROMs are switched to outputs and connected to the inputs of the D/A converters, the outputs of the 74573 are then in high impedance mode. In programming mode the data lines of the EEPROMs are switched to inputs and the outputs of the 74573 are active. The inputs of the D/A converters are connected in parallel.

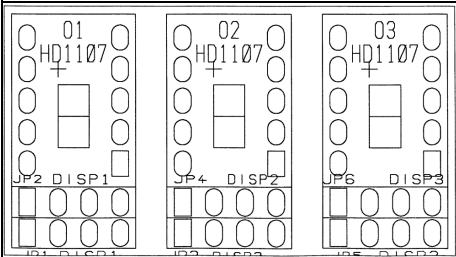
There are two rotary encoders, one for the frequency correction data and the other for the level correction data. The values chosen are stored in the EEPROMs by pressing the rotary encoder knob. Switch S3 can be used to select frequency correction or level correction separately in programming mode.



**Fig 12: Circuit diagram for the display on the YIG programming PCB.**



**Fig 13: PCB layout for the display.**



**Fig 14: Component layout for the display.**

4.7kΩ resistors from pin 1 and pin3 of each rotary encoder to earth are missing from the circuit diagram and PCB. Without them C3 to C4, used to de-bounce the rotary encoders, cannot discharge.

The PCB layout for the programming PCB is shown in Figs 8 – 10 and a picture of the completed PCB is shown in Fig 11. Details of the display board for the programming PCB are shown in Figs 12 – 14.

The possibility to program the system with a PC was added later. The address lines, the inputs of the ICs U1A, U1F, U11A, U11F, and pin 4 of switches S1 and S2 were fed to a connector. The pickup of the frequency adjusting potentiometer on the front panel was also connected to an SMB socket. These changes are still not included in the documentation. But this will be done later.

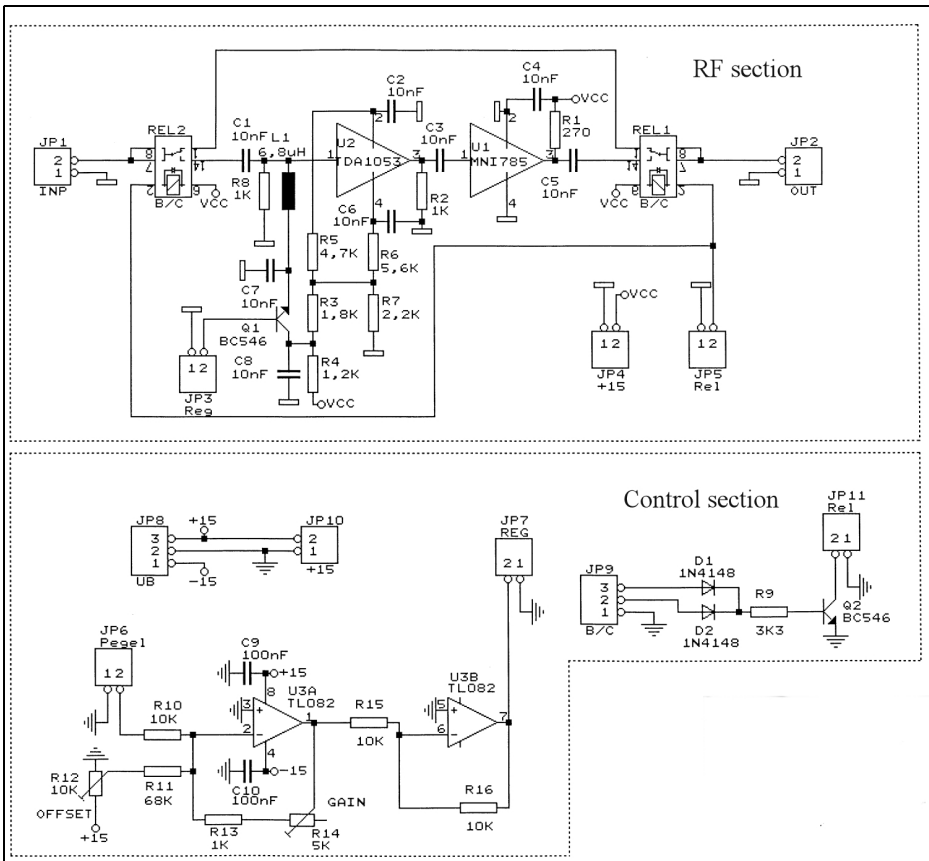
## 5.

### The pin diode attenuator

A method of changing the gain of the spectrum analyser was needed before the level correction data could be used. The manufacturer of the analyser did not foresee this possibility therefore it is not available so a pin diode attenuator had to be developed.

This consists of two piggyback PCBs fitted into the RF section that runs across the rear of the spectrum analyser. The pin diode attenuator is fitted between the IF output of the spectrum analyser and the IF module socket. For this spectrum analyser the IF is at 30MHz.

The circuit diagram for the two PCBs is shown in Fig 15. The TDA1053 pin diode attenuator was used in 1970s TV tuners. It can be replaced by 3 separate pin diodes that are more readily available.



**Fig 15: Circuit diagram of the pin diode attenuator. This is two PCBs, the RF section and the control section.**

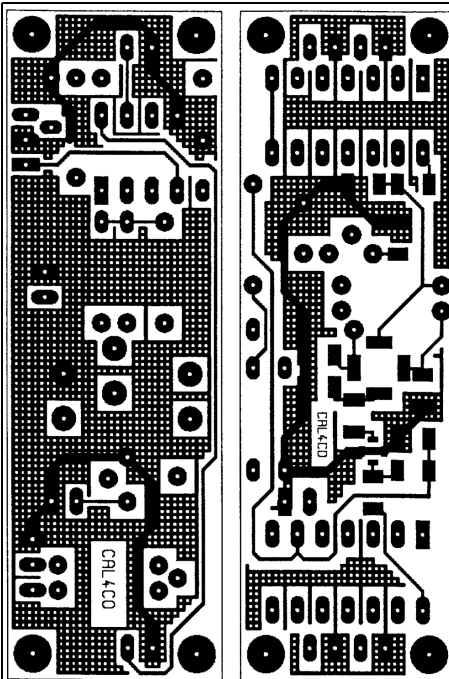
The pin diode attenuator is followed with an amplifier (16 to 20dB). The prototype used an MNI785 but any gain block amplifier with a high IP3 could be used. For the range 10kHz to 2GHz the pin diode attenuator is switched out with two reed relays.

That RF section is on the lower PCB. A circuit to control the adjustment level and the logic to control the reed relays is on the upper PCB. A 0.33μF capacitor was added later in parallel with the level input JP6. This prevents noise (from the address lines) that caused the zero line to increase by approximately 10dB.

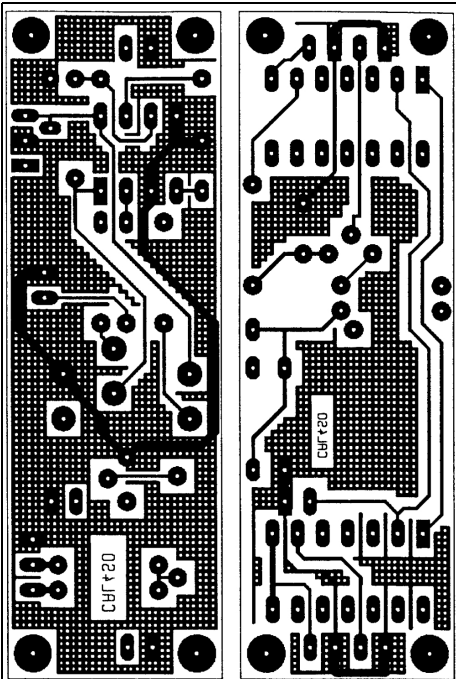
The PCB layouts for the pin attenuator PCBs are shown in Figs 16 – 18.

## 6. Notes

The pin diode attenuator was fitted near the IF output connector. The two other PCBs were located in a suitable space (see Figs 19 and 20). All connections and signals were made with screen cables. The YIG filter has a connection for a



**Fig 16: Lower side PCB layout for the pin diode attenuator PCBs.**



**Fig 17: Top side PCB layout for the pin diode attenuator PCBs.**

heater that can be connected to the supply voltage if necessary. The RF cables used semirigid cables.

## 7.

### Start-up and calibration

The first checks should be made with all plug-on connectors removed and the ICs not fitted so that no components are destroyed. Check the operating voltages are correct (+15V/-15V/+5V) on the IC supply pins.

Now fit the ICs and check the following:

- The reference voltage on the A/D and D/A converters (approximately 2.5V)
- The output of U9 (pin 6) the negative reference voltage

- Clock pulses of IC U4 and IC U5

For the first start-up jumper JP5 is left open.

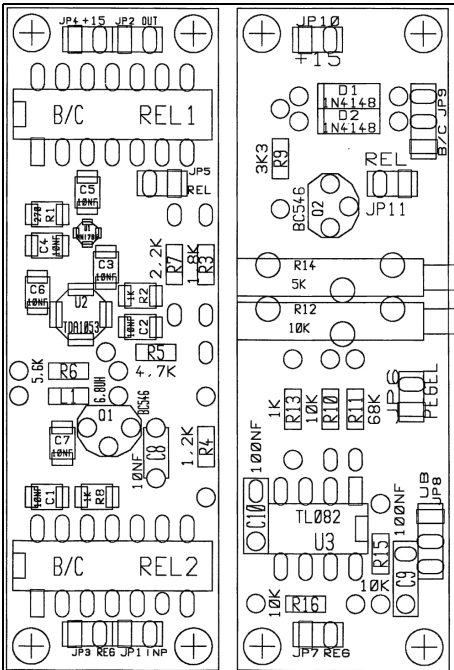
To be able to work around the driver and programming PCBs it is practical to make up 4 and 9 way extension leads.

#### 7.1. Programming

The first job is to set the address range of the A/D converter.

Connect the 9 way address socket on the programming PCB to the 9 way address socket on the driver PCB and the power supply socket of the programming PCB with the driver PCB.

Set the frequency adjuster on the spectrum analyser to the left to give the lowest frequency. Adjust the trimmer R4 so that the display on the programming PCB shows 0 but does not change to 1.



**Fig 18: Component layout for the pin diode attenuator PCBs.**

Set the frequency adjuster to the right and adjust the trimmer R7 to show 255 on the display. Repeat this adjustment several times because the adjustments

interact. Also check that the frequency adjuster on the spectrum analyser changes the address count continuously and evenly up and down from 0 to 255.

Check that the rotary encoders increment up and down perfectly. The capacitors C3 to C6 can be changed to reduce the effects of bouncing.

So far everything is working satisfactorily so the programming PCB can be connected directly to the driver PCB.

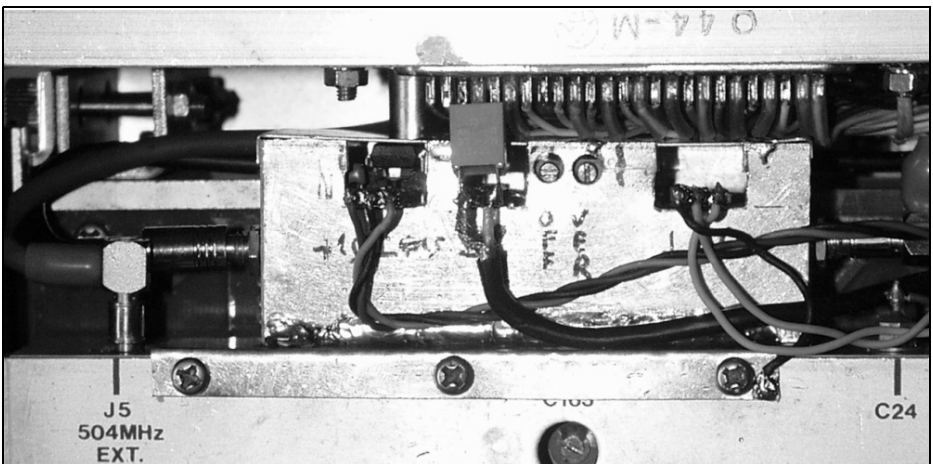
Check that the rotary encoders continuously vary the DC voltage on JP5 pin 2 and JP6 pin 2.

Now the frequency limits of the YIG filter are set as follows:

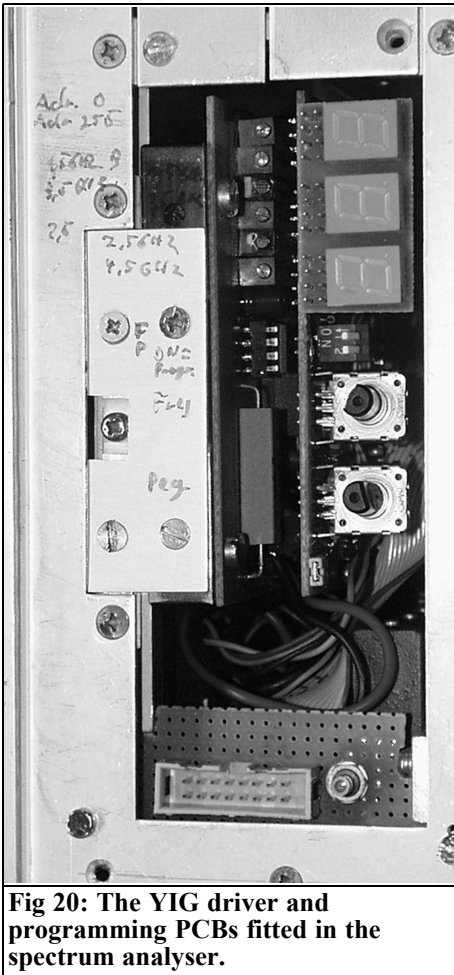
- Leave the spectrum analyser to warm up for at least one hour.
- Set the spectrum analyser to: zero scan, video filters out, range to highest, input attenuator to -20dB, reference line to 0dBm. Do not connect JP9 of the pin diode controller.
- Connect a signal generator to the input of the spectrum analyser and set it to 0dBm.

**Band B adjustment:**

- A) Set the frequency of the spectrum



**Fig 19: The pin diode attenuator fitted in the spectrum analyser.**



**Fig 20: The YIG driver and programming PCBs fitted in the spectrum analyser.**

analyser to minimum with the control on its left hand stop.

- B) Adjust the frequency of the signal generator for the maximum indicated on the spectrum analyser screen.
- C) Adjust the 1.5GHz trimmer R24 for maximum level.
- D) Set the frequency of the spectrum analyser to maximum with the control on its right hand stop.
- E) Adjust the frequency of the signal generator for the maximum indicated on the spectrum analyser screen.
- F) Adjust the 3.5GHz trimmer R25 for

maximum level.

- G) Repeat from step A) until both upper and lower maxima are found.

### **Band C adjustment:**

Repeat steps A) – G) above but adjust the 2.5GHz trimmer R21 and the 4.5GHz trimmer R22.

Following successful alignment, measure the deviation in level over the frequency range with the spectrum analyser adjusted for full scan.

For both ranges (B & C) tune the signal generator in 1MHz steps and note the largest and smallest levels indicated on the spectrum analyser also note the level difference.

- Set switch S3 into programming mode.
- Connect the control port pin 9 on the pin diode attenuator.
- Set the spectrum analyser to zero scan.
- Adjust the band and frequency to the values where the largest level was found. Take care because the half level frequency is only a few MHz and the increment is 100kHz so the spectrum analyser must be trimmed.

Note the minimum and maximum display with the automatic level correction controller the selected band. Using trimmer R14 on the pin diode attenuator the level difference should be a little more than the level difference measured previously in full scan mode. This will mean that the full word length of the correction values can be used for level correction.

- Adjust the band and frequency to the values where the smallest level was found. Look for the greatest possible value set with the level correction rotary encoder. Adjust trimmer R12 on the pin diode attenuator to somewhat more than 0dBm on the display.
- Adjust the band and frequency to the values where the largest level was found. Look for the smallest possible





value set with the level correction rotary encoder. Check that somewhat less than 0dBm is adjustable on the display, if not increase the gain with R14 and repeat the procedure.

If everything ran smoothly, connect the jumper on the driver PCB and begin the actual calibration procedure.

## 7.2. Hand calibration procedure

This is tedious and takes hours of concentrated work. The calibration is identical for band B and band C but they must be done separately.

A signal generator is required that covers the frequency range and supplies a stable output level. Use an RF voltmeter connected to the RF input of the spectrum analyser to measure the level of the signal generator. The output of the signal generator that produces 223mV at both the highest and lowest frequencies of the band should be noted. Divide the difference in level by 20 to indicate how many mV the signal generator must be increased by for the 100MHz steps to keep the spectrum analyser at a constant level of 0dBm.

Set the spectrum analyser on:

- zero scan
- Input attenuator to -20dB
- Reference line to 0dBm
- Range to maximum
- Display to 10dB/div
- Video filters on maximum

Leave the equipment to warm up for 1 hour.

- A) Use the frequency adjustment on the spectrum analyser to set the display on the programming PCB to 0, make certain the address display is centred at 0.
- B) Using 10kHz steps on the signal generator look for the frequency that gives a maximum display on the spectrum analyser.
- C) Search for the YIG filter frequency that gives a maximum using the

rotary encoder. Be careful because it is possibly to get two maxima next to each other, look for the highest.

- D) Press the button on the frequency rotary encoder to store the value found.
- E) Set the level on the spectrum analyser display to as close as possible to 0dBm using the level rotary encoder. After this value has been stored it is possible to use the 2dB/div range on the spectrum analyser to check the setting.
- F) Press the button on the level rotary encoder to store the value found.
- G) Use the frequency adjustment on the spectrum analyser it increases the address by one step (shown by the display on the programming PCB), make certain the address display is centred on the correct value. Repeat the procedure from B). Continue until all 255 addresses are set up.
- H) Set switch S3 on the programming PCB so that programming mode is ended to avoid inadvertently overwriting the EEPROMs.

## 7.3. Calibration procedure with a PC

I wrote a program in HP instrument Basic (only executable using Windows 3.11) to automate the programming. The following are required:

- HP instrument Basic
- HP82335, HP-IB bus card (an ISA card for Win3.11)
- RF generator e.g. SMHU from R&S
- HP34401 voltmeter connected for level measurement to the video output of the spectrum analyser.
- HP33120 DC power supply to produce the 5 - 10V to tune the spectrum analyser.
- A URV5 RF millivoltmeter with NRV-Z1 measuring head.
- A combiner to divide the signal between the spectrum analyser and the RF millivoltmeter. This is used to keep the voltage at the input of the spectrum analyser constant.



- A Fluke 8840 voltmeter to control the voltage of the pin diode attenuator and supply an error message if the range is exceeded.
- An equipment port that can be read and controller over the HP-IB bus. This would be a homemade matrix.
- If required a DC voltage level converter and a shifter to convert the 6 – 10V range to that required by the spectrum analyser. This would be homemade.
- The spectrum analyser must be modified so that the HP33120 DC power supply can control the frequency instead of the adjustment potentiometer. The program must be able to set the centre frequency of the spectrum analyser.

### 7.3.1. The Basic program.

The program is very slow and takes several hours to process the 255 addresses.

Unfortunately neither a sweep generator nor a noise generator was available to document the success of this project. Nevertheless, the frequency response is now smooth at approximately  $\pm 2\text{dB}$  instead of  $\pm 7\text{dB}$ .

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## 8.

### Conclusion

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This article should be read as a suggestion of how it is possible to successfully solve a similar task. It cannot be used as an exact guide to build such equipment partly because some of the components used e.g. ZN427, ZN428, 74185 are difficult to obtain.

Each different spectrum analyser manufactured has different amounts of space available. The saw tooth level will certainly be different for each spectrum analyser. Therefore adjustments would have to be made. Other spectrum analys-

ers have different frequency concepts e.g. scan range 4GHz. Then 255 steps would not be sufficient and 10-bit or 12-bit converters would need to be used. A microprocessor may be suggested but it should be avoided because they produce interference lines in the spectrum that are not easily suppressed.

The program can only be a guide. The available PC program would have to be adapted for more modern systems or the devices available to the reader. Each reader may have different Basic software and HP-IB bus card. Each reader will use different measuring instruments with their own commands for remote control. Each spectrum analyser has different interfaces designed for the specific instrument e.g. the 0dB reference from the Y output. The method of interfacing the BCD data from the A/D converter must be considered. All of this must be adapted in the calibration program.

## Invitation to the 34rd Nordic VHF-UHF-SHF meeting at Aland Island 24-27/5/2012

The Radio Amateur Technology Society in Finland, RATS, invites all VHF-UHF-SHF microwave enthusiasts to the annual Nordic VHF-UHF-SHF meeting to be held at Aland island at 24-27/5/2012. The meeting will take place at the Käringsundsby Resort & Conference centre, where it was held in 2004. The meeting will be organised as a four-day meeting beginning on Thursday, with a possible excursion to a remote location on Friday (still to be confirmed and with allowance for the weather)

The official meeting website - <http://vushf.rats.fi/> - is open for general information, please read and prepare to book your holidays for the best meeting of this summer! Accommodation reservation will be opened soon as the final details are confirmed.



*Henning Christof Weddig, DK5LV*

# AGC test switch

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## 1.

### Introduction

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The reasons for designing the AGC test switch were the “bad surprises” that the author experienced while developing The AGC Module [1, 2, 3]. The AGC module had unexpected response after applying a step of the input signal: it responded with an overshoot of the control voltage thus deafening the receiver. (RF output signal of the signal generator switched on and off).

In order to examine these unwanted regulation characteristics more closely a piece of test equipment was necessary that would give defined level jumps (10 – 60dB) to the module under test. The level change must take place without bouncing and overshoot. This is not achievable with a signal generator.

The test switch is also useful for testing the AGC control characteristics of other (amateur radio) receivers including Software Defined Radios (SDRs).

### 1.1 Design Considerations

The AGC test switch is inserted between the output of a signal generator and the antenna input of a receiver or the input of an IF amplifier chain with automatic gain control capability either on board or as developed by the author as separate boards. With this switch the user can apply two defined levels of the RF signal at user-defined times. The lower level should be selectable in 10dB steps from 10 to about 60dB.

The switching itself between the two

levels should be as fast as possible and free of spikes and bounce. From these two restraints a mechanical relay is not the right choice, an electronic switch must be used instead.

During the on-state the insertion loss should be as low as possible, in the off state the isolation should be as high as possible, minimum about 10 to 20dB higher than the highest attenuation, resulting in an off isolation of 70 to 80dB.

Electronic switches could be built using CMOS-switches like the famous CD4066 or equivalent, GaAs switches, or even the “famous” bus switches FST3126 often used in the H-mode mixer.

The CD4066 has a too high series resistances resulting in a large insertion loss in the “on” state, input capacitances limit the upper usable frequency and off isolations is not sufficient for the above limits.

The FST switches exhibit lower on resistances, but their series resistance varies greatly as a function of the input voltage see Bob Dalley’s (M0RJD) findings in [2]. Also some carrier injection can take place during switching resulting in unwanted spikes.

GaAs switches are widely used as antenna changeover switches in mobile phones. These tiny IC’s could probably be used, but one has to find suitable components for the “very low frequency range (LF to RF). A suitable switch could be an AS176-59 or AS179-59 single pole double throw switch (SPDT) from Skyworks that is specified for a frequency range of DC to 2.5GHz. The frequency range is set by the values of external coupling capacitors. Positive control voltages can control this chip. No infor-



mation is given concerning the charge injection; the off isolation is stated to be typical 50 to 55dB, as two switches are always connected in series, the summed attenuation of the off isolation may be sufficient. To get these high isolation values a careful layout has to be achieved.

A first version of the AGC switch was derived from a circuit developed in the former occupation of the author. This version used two “normal” silicon diodes in series (1N914) but the circuitry did have large spikes during switching. Also the input return loss was only 10dB and frequency range limited to the shortwave bands.

In the book “Experimental Methods in RF Design” [4] a balanced circuit using PIN diodes is described in chapter 7.12 under the title “AGC test switch”

The author made a quick test using this circuit configuration (balanced circuitry) using “ugly style construction” on a metal plate. Signal transformers from Mini Circuits (ADT-1-6T) [9] were used for the unbalanced to balanced conversion of the input, the diodes were BA389 PIN diodes instead of the types shown in [4].

This first test showed good results, i.e. spike free switching (due to the balanced configuration), an off isolation in the range of 80dB and low insertion loss in the on state. This configuration was then used to produce a PCB and refining the circuitry.

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## 2.

### Product requirement specification

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Frequency range: 1 to >100MHz (>150MHz desirably)

- Transmission loss in on state: <1dB
- Input and output matching: better

than –20dB, minimum 10dB (VSWR 1.2... 2)

- Stopband attenuation in the off state  $\geq 80\text{dB}$
- Transmission attenuation in steps: in 10dB steps from 10 – 60dB, minimum attenuation 10dB
- Triggering internal or external either manually or automatically with three different time intervals
- Trigger output (trigger to control an oscilloscope)
- Installed in a metal housing
- BNC sockets for the RF signals
- Power supply by a plug top power supply or an internal power supply

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## 3.

### Description of circuit

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#### 3.1 Overview

The AGC switch is split into two printed circuit boards:

- RF switch module
- Control electronics

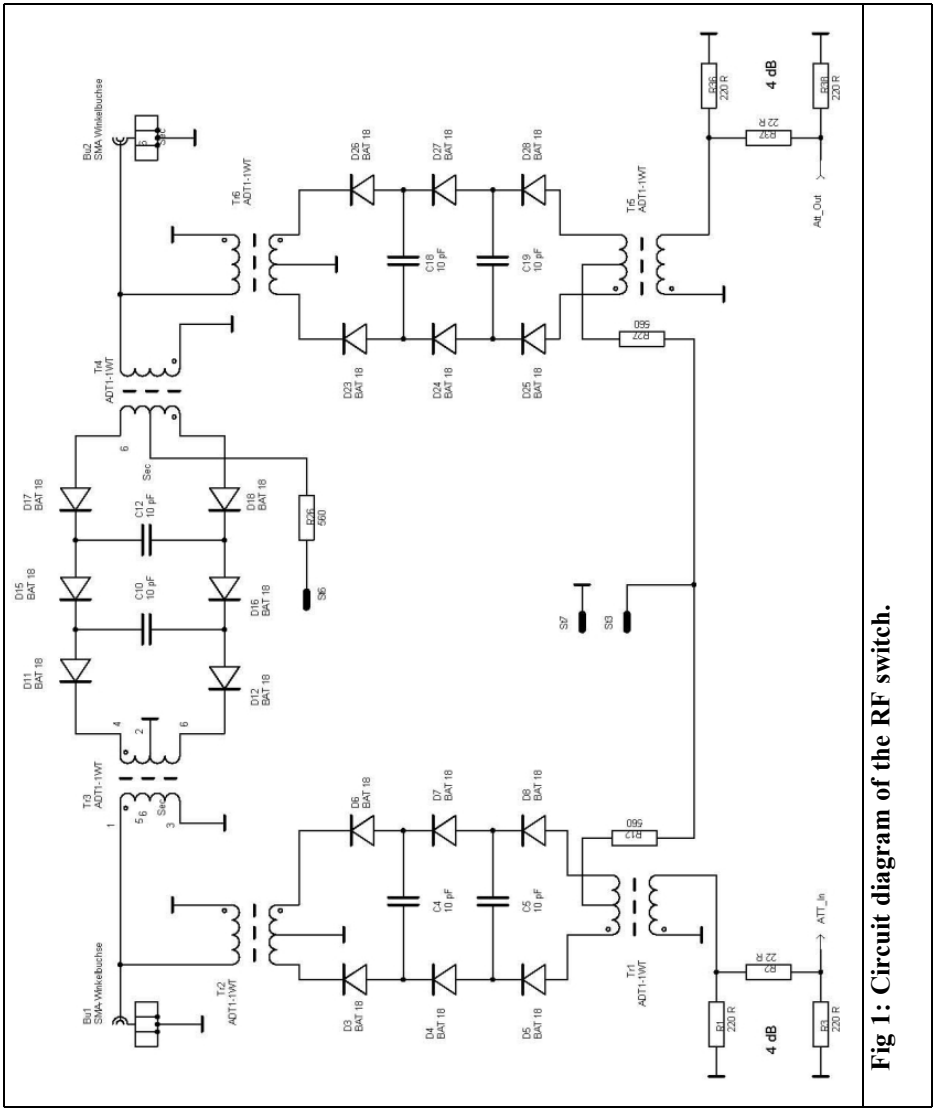
The RF switch and attenuator consists of the following sub-assemblies:

- Change over switch
- Switchable attenuators (one 10dB and two 20dB)
- Fixed attenuator

#### 3.2.1 Switches

The three switches are the same therefore only one switch will be described. Fig 1 shows the circuit diagram of this sub-assembly.

The DC switching voltage is fed to the central tap of the broadband transformer Tr4 (Mini Circuits ADT1-1WT; [9]) via R26 and then via the two windings to the three diodes connected in series (D11, D15, D16; D12, D17 D18). The second centre-tapped transformer, Tr3, connects the two branches of diodes to ground via



**Fig 1: Circuit diagram of the RF switch.**

the centre tap.

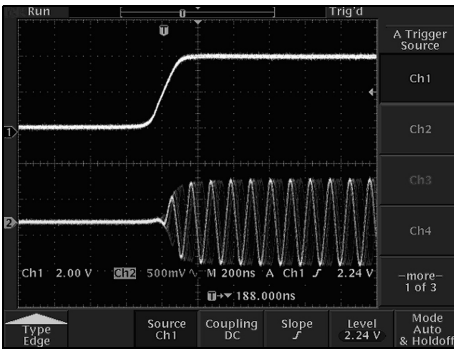
The RF signal is fed from socket Bu1 to the un-tapped coil of transformer TR3 and coupled via the transformers to the un-tapped coil of TR4.

Since the switching signal appears equally on both transformers it is suppressed due to the symmetry of the transformers. The RF signal is switched

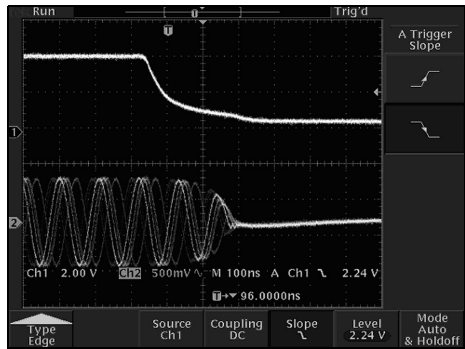
between the two secondary winding by the switching signal.

An examination of the test model using an oscilloscope did not show overshoot or spikes on the switching edges.

Fig 2 shows a 9MHz signal connected to socket Bu1 and terminated with 50Ω as it appears at the output on socket Bu2 on channel 2 of the oscilloscope. Channel 1



**Fig 2: 9MHz signal on Bu1 with RF switch switching on. Channel 1, switching signal. Channel 2, switched RF signal on Bu2**



**Fig 3: 9MHz signal on Bu1 with RF switch switching off. Channel 1, switching signal. Channel 2 switched RF signal on Bu2**

shows the switching signal from the control electronics module. Fig 2 shows the switch on process, Fig 3 shows the switch off process. The long decay time is due to the CMOS components and the discrete transistor driver.

The good stopband attenuation is due to the capacitors C10, C12 that bridge the cathodes of the diodes. This is because of the capacitive voltage divider comprising the reverse bias capacity of the diodes and the bridging capacitors. The bridging capacitors form a low pass filter with the resistance of the diodes when they are turned on. The series connection of three diodes in each branch as well as the capacitors C10, C12 give the desired high stopband attenuation.

Tests showed that applying a negative voltage to turn off the diodes did not give an increase of the stopband attenuation on the prototype.

The centre tap of TR4 should be decoupled to ground with a capacitor so that the RF signal is distributed “well” during both halves of the switching cycle. This would slow the switching speed and tests showed that it works without the capacitor.

In [4] it is pointed out that the diodes heat up with excess input power. For receiver tests a maximum input power of

$<0\text{dBm}$  is often used. With this power no self-switching of the diodes was observed.

If PIN diodes that used as a variable resistor to be used as voltage controlled attenuators their series resistance even under high current conditions is in the range of about  $6\Omega$  and therefore relatively high. This high resistance results in a too high insertion loss when used as a switch

With three BAS16 diodes the insertion loss was measured to be 5dB resulting in a too high insertion loss and mismatch of the input impedance, i.e. the switch showed an input impedance of  $100\Omega$  when terminated with  $50\Omega$  at the output.

Only the use of the special switching diode BAT 18 gave an insertion loss of  $<1\text{dB}$ . According to data sheet [5] this pin diode is intended as switch with low loss for frequencies  $>10\text{MHz}$ . From the data sheet it has the following characteristics:

- Differential resistance ( $f=1200\text{MHz}$ ;  $I=5\text{mA}$ )  $RD = 0.4 - 0.7\Omega$
- Blocking capacity ( $V_R=20\text{V}$   $f=1\text{MHz}$ )  $CT = 0.75 - 1\text{ pF}$
- Series inductance:  $LS=1\text{nH}$

The ADT1-1WT transformers can be used to  $400\text{MHz}$  according to the data

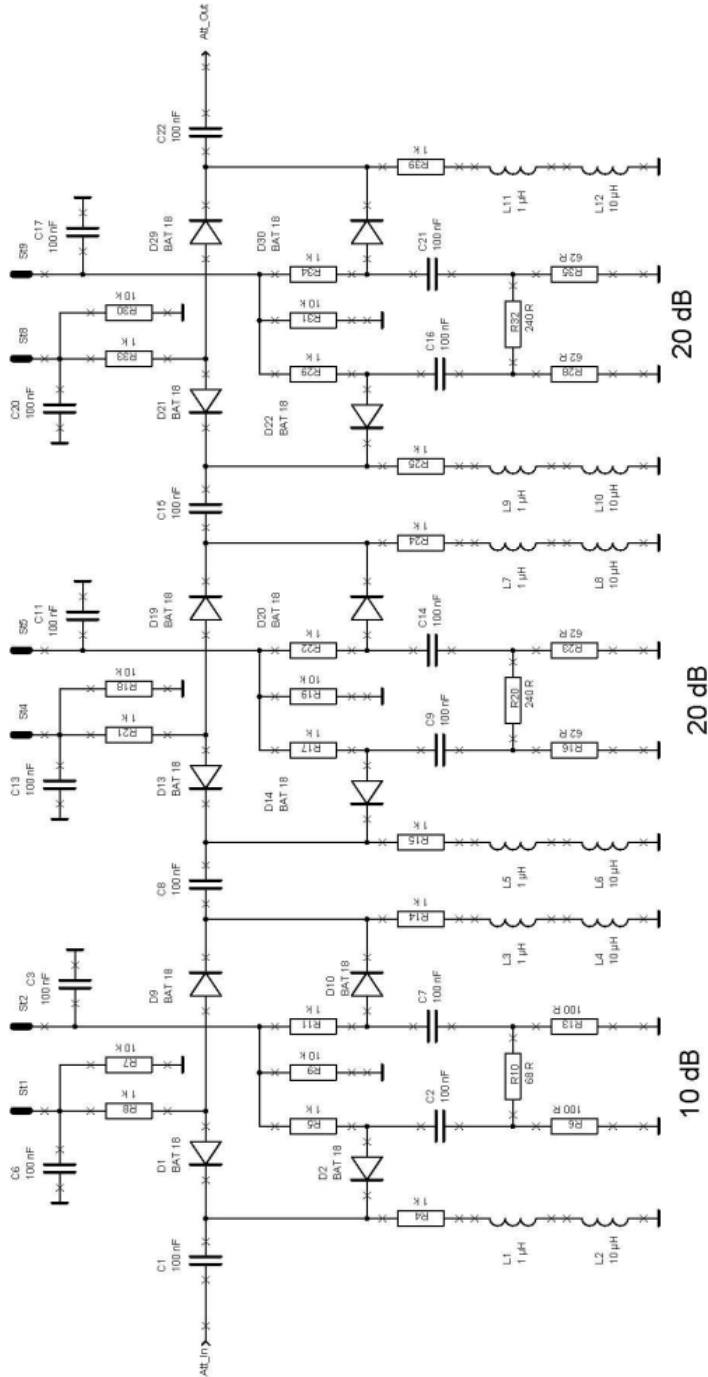


Fig 4: Circuit diagram of the adjustable attenuator.



sheet [9] when used in a  $75\Omega$  system. Nevertheless with a  $50\Omega$  system impedance a good performance was obtained.

The upper usable frequency of the first test model (using ADT1-6T transformers) was  $>150\text{MHz}$  see [9]. The use at these high frequencies was not part of the product requirement specification therefore the ADT1-1WT transformers were used. Unfortunately the connections (central tapping) of both types are not the same so a new PCB layout had to be made.

In the switched off condition the switch is very high impedance. Therefore it is possible to use a similar switch at the input and output ports with a switchable attenuator between them to give a defined attenuation of the input signal.

The two  $\pi$ -circuits (R1, R2, R3; R36, R37, R38) give a pre-attenuation of 4dB each. The fixed attenuators are switched using diodes. In the "through" position all three pairs of diodes (D1, D9, D13, D19, D21, D29) give an extra 2dB insertion loss. Together with the two fixed 4dB attenuators at the secondaries of T1 and T6 the overall loss in the attenuation position is a minimum of 10dB if no adjustable attenuator is selected.

### 3.2.2 Adjustable attenuators

The attenuation values of adjustable attenuators are one 10dB and two 20dB so that the attenuation can be selected in 10dB steps from 10 to 50dB. Together with the basic attenuation of 10dB the maximum adjustable attenuation is 60dB compared to the directly connected through signal.

Originally the switches used for inserting the attenuation into the signal path were normal printed circuit board mounted rocker switches. This technique is often found in the literature on the subject. A version developed by the author did not give the desired results. The return loss (S11) was measured to be -10dB for

frequencies  $>20\text{MHz}$ . According to the specification (see paragraph 2) values of  $<-20\text{dB}$  are required therefore the specification was not met with rocker switches. The frequency response (S21) showed that the attenuation also rose for frequencies  $>20\text{MHz}$  so this did not meet the specification either. The switches have a predominantly inductive component that cannot be neglected, leading to a degradation of the attenuation (and the frequency response). From the authors experience miniature rocker switches are not suitable for use in test equipment.

Because of the good experience with BAT 18 diodes in the main switch they were chosen. A separate printed circuit board was developed for a first test.

Fig 4 shows the circuit diagram of the adjustable attenuator sub-assembly. Two pairs of series connected diodes are used to switch the RF signal either directly through via the  $\pi$ -circuit attenuator using SMD resistors.

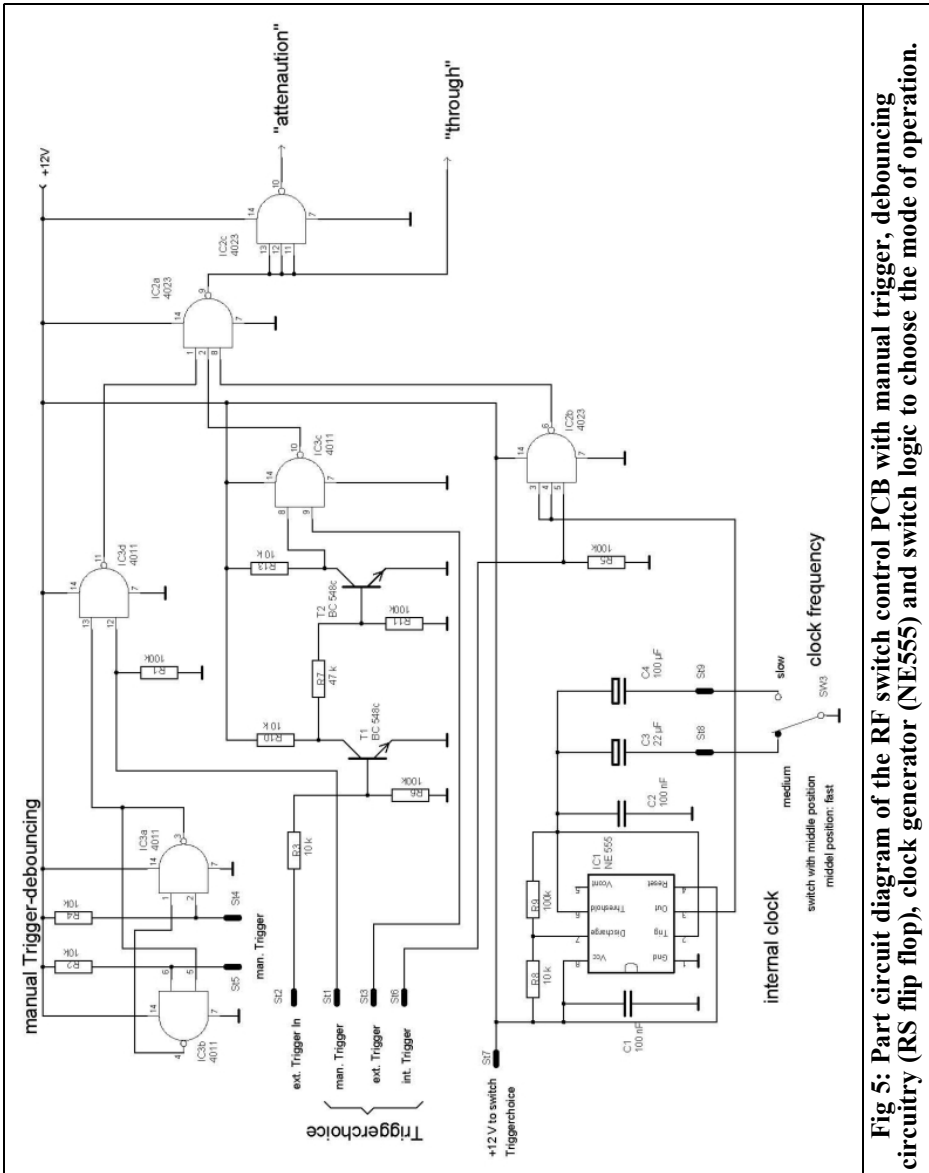
The DC switching voltage is fed via a  $470\Omega$  resistor to the respective pair of diodes and grounded via a  $1\text{k}\Omega$  resistor and two SMD chokes in series [ $1\mu\text{H}$ ,  $10\mu\text{H}$ ]. The  $10\mu\text{H}$  has a self-resonant frequency of 120MHz [8] and the  $1\mu\text{H}$  choke at 450MHz. Above these resonant frequencies the chokes behave like capacitors. The series connection of the chokes minimises the shunt capacitance affect on the RF signal and gives a good high frequency performance.

The 100nF SMD coupling capacitors in the RF path are not ideal because of the self-resonance shown in the data sheet. A capacitor above its self-resonance behaves like an inductance!

Tests with the printed circuit board showed that using single pole rocker switches left one switch input "in the air" giving poor stopband attenuation. Therefore a  $10\text{k}\Omega$  resistor and a 100nF capacitor are used to give an RF short circuit for the open switch connection.

To ensure a good stopband attenuation of





**Fig 5: Part circuit diagram of the RF switch control PCB with manual trigger, debouncing circuitry (RS flip flop), clock generator (NE555) and switch logic to choose the mode of operation.**

the diode switches a double-sided printed circuit board is necessary. A plated-through hole ground surface is particularly important for the ground connections of the chokes.

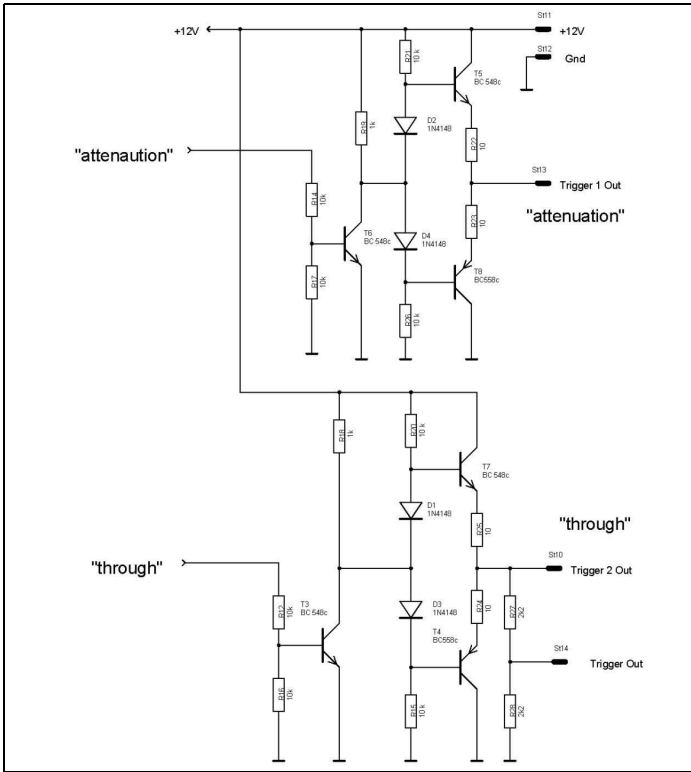
### 3.2.3 Fixed attenuator

The design of the circuit used for the

fixed attenuators (two 20dB and one 10dB) gives strange values for the resistors when they are calculated accurately. It is acceptable to use the next value in the E24 series.

### 3.3 Control circuit

The control circuit consists of two sub-



**Fig 6: Circuit diagram of the driver stages on the control board.**

assemblies, see Fig 5 and 6:

- Bounce buffer for manual change over (R-S flip-flop)
- Pulse shaping of the external trigger signal to logic levels
- Clock generator with external adjustable clock frequency
- Logic for selection of the different trigger sources
- Drivers to control the diode switches
- Trigger output

### 3.3.1 De-bouncing circuit

The R-S flip-flop made from two gates in IC3 de-bounces the manual trigger switch (SW2). The pull up resistors the R2 and R4 give a defined level with SW2 open.

### 3.3.2 Pulse shaping

Pulse shaping of the external trigger

signal uses two discrete component inverter stages, T1 and T2. The output of T2 is fed via a gate in IC3 that is opened if the trigger switch SW1 is in the appropriate position.

### 3.3.3 Clock generator

The internal clock generator uses the familiar NE555 timer IC that is connected as an astable trigger stage. For symmetric pulses the resistor R9 (RB) should be twice the value of R8 (RA), however in the prototype a relationship of 1:10 for the resistors was necessary according to data sheet [7]. Both the IC and the resistors were recycled from an old printed circuit board and the resistors were not checked with an ohmmeter. The values of the two resistors may need adjustment to give a symmetric square wave.

If the external switch (SW3) is in the



central position, only C2 determines the frequency. The capacitor value of 100nF was selected using an oscilloscope to give simple control of the square wave signal. This value can be increased.

The “medium” position of switch SW3 gives a clock pulse of 0.5Hz and in the “slow” position gives a period of approximately 5 seconds.

### 3.3.4 Logic

The logic for selection of the trigger source uses two gates, IC3d and IC3c as well as IC2b, IC2a and IC2c as inverters. The selection of the trigger source is made with the external switch SW1. Resistors the R1 and R5 define a “low” level if the appropriate switch contacts are open.

### 3.3.5 Drivers

Because the CMOS gates cannot supply sufficient current to control the diode switches the drivers using transistors T6, T5, T8 and T3, T7, T4 were designed see Fig 6. The output stage is like an audio amplifier, resistors R22, R23 and R25; R24 give a certain level of protection for the transistors in the event of a short circuit.

### 3.3.6 Trigger output

The trigger output for connection to an oscilloscope uses the voltage divider (resistors R27, R28).

## 3.4 Power supply

Because the power requirement of both printed circuit boards is not very high either a plug top power supply or a small printed circuit board with a transformer, rectifier and voltage regulator can be used. If a plug top power supply is used the problem of magnetic radiation inside the metal housing is avoided. Also issues concerning proper grounding and earthing of the metal case to conform to safety regulations (in Germany VDE) are avoided.

## 4.

## Construction

### 4.1 electronics

The RF switches and control circuits are constructed on two separated double-sided printed circuit boards. Figs 7 to 9 show the component side, track side and component layout of the RF switch board, Figs 10 to 12 show the component side, track side and component layout of the control board. Table 1 and 2 in Part 2 show the parts lists.

The RF switch PCB uses SMD components and the control PCB uses conventional components. The switches SW4 to SW6 for the RF board are connected using short leads to the appropriate pins on the printed circuit board. PCB mounting SMA connectors are used for the RF connections with short RG174 coax cable connections to the BNC sockets on the front panel.

Fig 13 shows a photograph of the component side of the RF switch PCB, Fig 14 shows a photograph of the component side of the control PCB.

To achieve the specified stopband attenuation, the ground surfaces of the RF switch PCB has the upper and lower surfaces connected by through connections in several places. Therefore many via holes are provided. The author uses thin wires from a braid fed through the holes and soldered on both sides. In addition the upper and lower ground surfaces are connected on both long sides and the transverse sides (in the area of the attenuators) by soldering copper foil strips.

Both printed circuit boards should be built into a metal housing in order to avoid stray RF effects. Fig 15 shows a schematic of the electrical inter-connections of both printed circuit boards and the connection to the external controls.

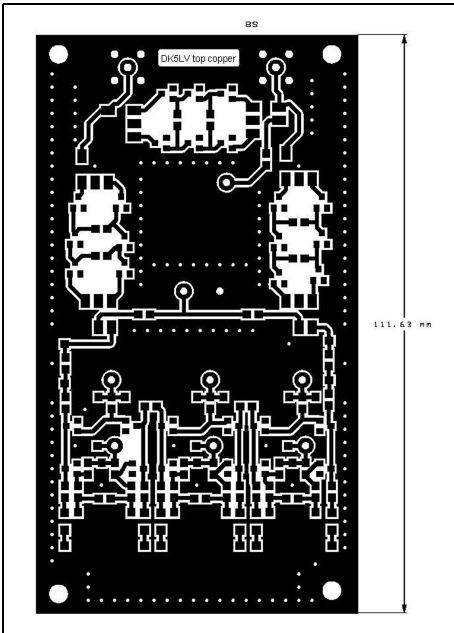


Fig 7: Top side of RF switch PCB (SMD side).

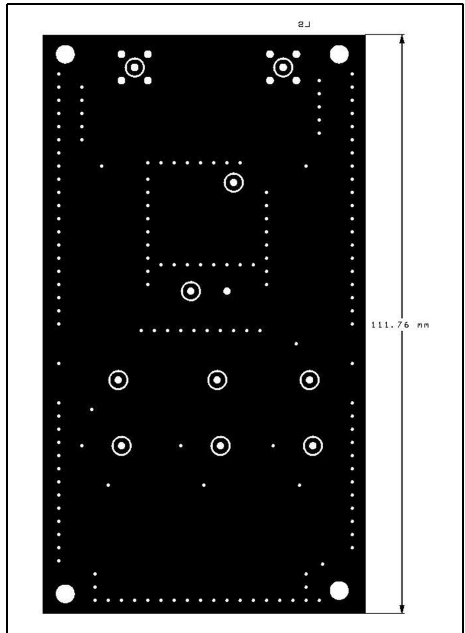


Fig 8: Bottom side of RF switch PCB

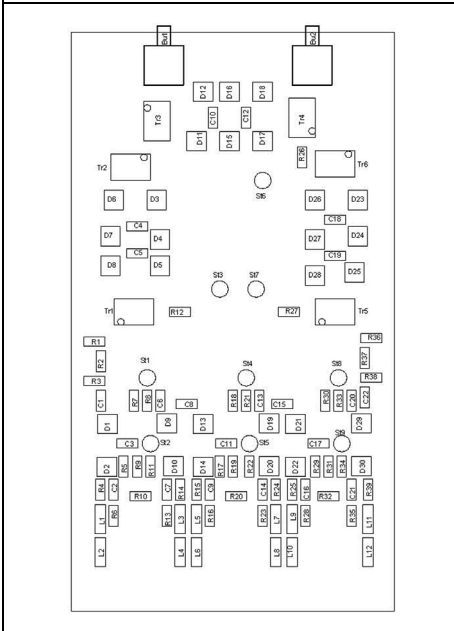
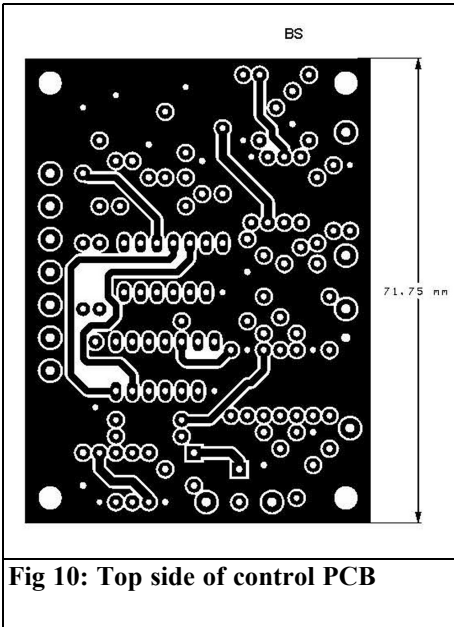


Fig 9: Component layout of RF switch PCB.

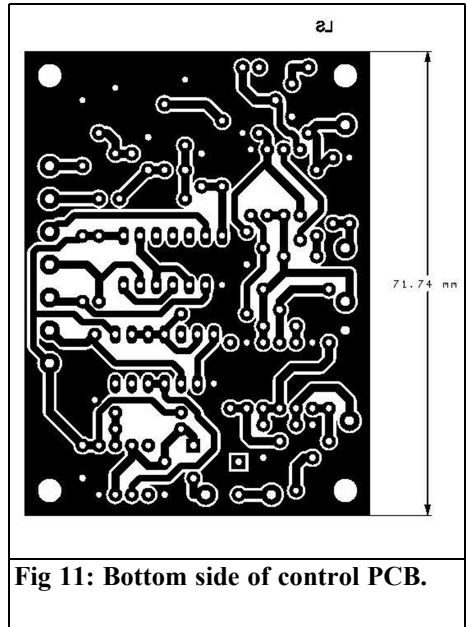
### 4.2 Mechanics

The author built the housing for the AGC switch using many parts from the junk box and from a scrap bin. The housing uses aluminium profiles (from scrapped 19 inch case rescued from a scrap bin) and slide in aluminium panels. The housing is 20 x 15cm and 9cm high. The front panel was a 3 mm thick aluminium front panel from a scrapped 19 inch case. The front panel layout, legends and drilling was done with the help of the CAD program FrontDesigner 30 [11]. This program produces HPGL files for use on a CNC milling machine in the QRL of the author. This milled the contour, drilled the holes and engraved the legends.

Fig 16 shows the front panel and Figs 17 and 18 show photographs of the author's prototype. *[unfortunately there was not enough room to include these in this issue. The article will be continued in issue 2/2012 - Andy]*



**Fig 10: Top side of control PCB**



**Fig 11: Bottom side of control PCB.**

**5.**

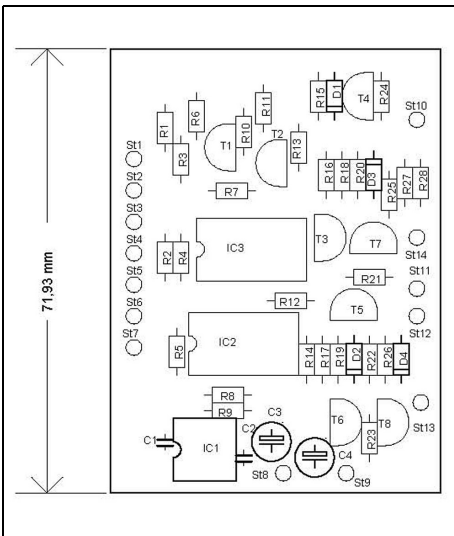
**Conclusion from prototyping process**

The double-sided PCB for the first prototype RF PCB was boded using photographic laquer to give one complete copper side while the other side was etched. A single-sided printed circuit board would not have been sufficient.

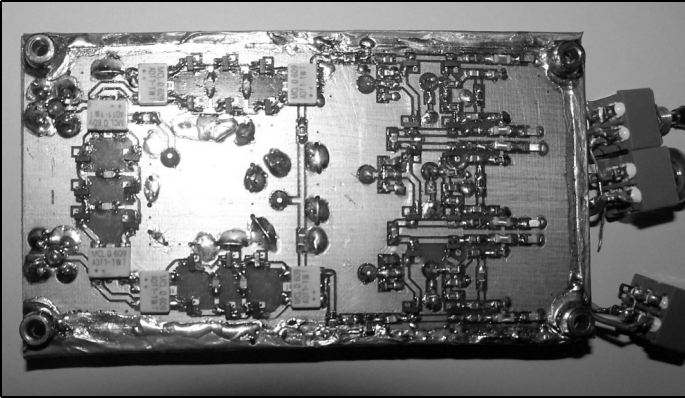
Unfortunately the artwork was used as a mirror image that only affects only the diodes. Pin of 2 at the SOT 23 package is not connected (pin 1 is the anode) so a thin piece of wire could be used between pin 1 and 2.

Only in line switches were used initially. The BAS16 diodes selected resulted in an insertion loss of 5dB that does not meet the specification of the AGC test switch. ADT-6-1T transformers were used.

The feed impedance of 100Ω was measured with an HP 8753B Network Analyser. This input impedance is too



**Fig 12: Component layout for control PCB.**



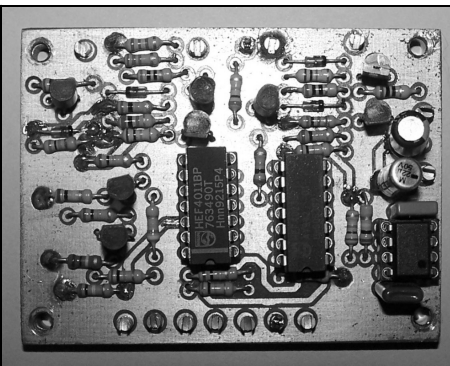
**Fig 13: Picture of the RF switch PCB.**

high that means the series resistance of the diodes chosen was too high with approximately 10mA direct current.

The input impedance could be substantially improved with an internal 100 $\Omega$  SMD resistor connected to ground across Bu1 and Bu2 however the transmission loss was too high at 5dB.

When BAT 18 diodes were used an insertion loss <1dB was reached, the matching was <-20dB in the frequency range up to 100MHz and rose to approximately 14dB at 145MHz. This value does not completely comply with the product requirement specification, however as was judged sufficient. The measured stopband attenuation was sufficient at 80dB in the lower frequency range.

In a second step the two additional RF



**Fig 14: Picture of the control logic PCB.**

switches and attenuators were added. The measurements after this step showed the desired results. When these attenuators were added a maximum stopband attenuation of 40dB was reached for frequencies >10MHz. A “notch” appeared at 160MHz.

These bad results are “food for thought” for experts (and hobby researchers) who have the appropriate measuring equipment at home (or at the QRL).

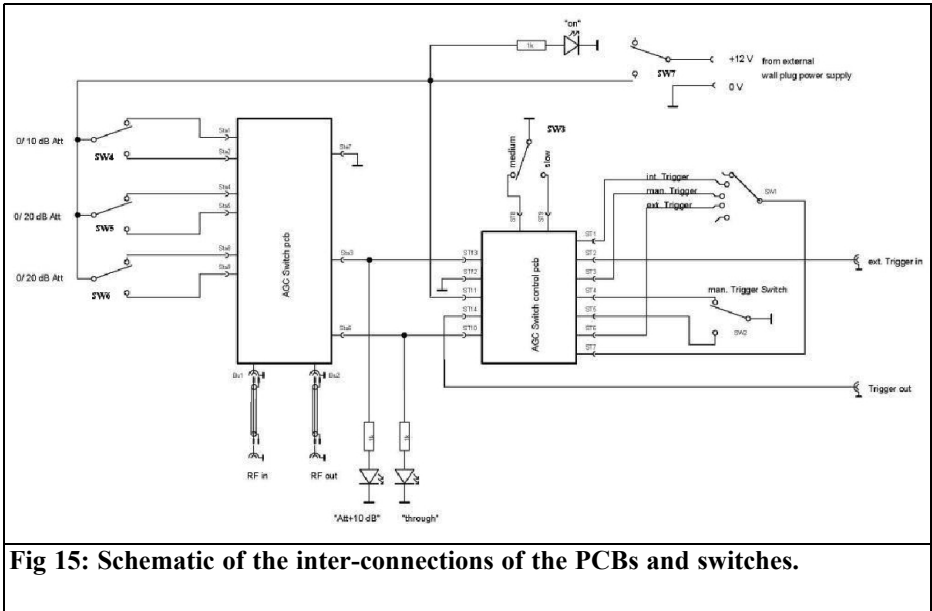
A search of different designs furnish the desired result.

The stopband attenuation could be substantially improved when a piece sheet metal was placed on the top side of the printed circuit board without electrical contact with the ground surface.

Thus a double-sided printed circuit board must be used to eliminate unwanted interconnections.

This double-sided printed circuit board brought an improvement, however the stopband attenuation values at high frequencies was still too bad. Only soldering copper foil strips between the upper and lower surfaces of the printed circuit board edges gave the desired result.

Because the insertion became much worse at frequencies >100MHz a different type of the transformer (ADT1-1WT) was selected. A new PCB had to be made because the pin connections of the ADT1-6 were different.



**Fig 15: Schematic of the inter-connections of the PCBs and switches.**

**6.**

**Literature**

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[2] The AGC module Part 2: continuation from issue 1/2008, Henning Christof Weddig, DK5LV, VHF Communication Magazine 4/2009 pp 242 -250

[3] The AGC module Part 3: continuation from issue 4/2009, Henning Christof Weddig, DK5LV, VHF Communication Magazine 1/2010 pp 54 - 58

[4] Experimental Methods in RF Design, Wes Hayward W7ZOI, Rick Campbell KK7B and Bob Larkin W7PUA, ARRL Chapter 7.12

[5] Bus Switches as Analogue Switches, Bob Dalley M0RJD, <http://www.m0rjd.co.uk/bus-switches.html>

[6] Data sheet BAT 18, Siemens/Infineon

[7] Data sheet LM555, Fairchild Semiconductor

[8] Data sheets wire-wound SMD coils size 1206, Company Stettner (stelco)

[9] Data sheet ADT6-1T, Mini Circuits

[10] Data sheet ADT1-1WT, Mini Circuits

[11] Program FrontDesigner 3.0, <http://www.abacom-online.de/html/frontdesigner.html>

To be continued in issue 2/2012 with the measurement results.



Gunthard Kraus, DG8GB

# Internet Treasure Trove

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## MicroWaves & RF

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The author found this site while carrying out some research on Patch and Vivaldi antennas. There is a lot of information on this site.

Address: <http://mwrf.com/>

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## Antenna-Theory.com

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This is the place for antenna theory. There is more than enough information on this site.

Address:

<http://www.antenna-theory.com/>

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## Telemetering

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They are antennas specialists. The page indicated contains a useful nomogram showing the relationship between antenna height at the transmitter and receiver with the optical and radio horizons.

Address:

[http://www.keytelemetering.com/9600\\_Antenna.htm](http://www.keytelemetering.com/9600_Antenna.htm)

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## Afreet software

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Lots of amateur radio downloads on this site. The page indicated has a voice shaper to process your audio signal be-

fore feeding your transmitter.

Address:

<http://www.dxatlas.com/VShaper/>

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## Pentek

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A familiar name for digital signal processing. This page shows an introduction to a most useful book; the Software Defined Radio Handbook, available free of charge once you have registered.

Address:

<http://www.pentek.com/applications/Applications.cfm#Software%20Radio>

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## Key Telemetering Products

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There is a very interesting article on Spread Spectrum Technology in the Tutorial section of this web site.

Address:

<http://www.keytelemetering.com/>

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## Morse code Trainer

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CW still has a place even in this age of the Internet. This site could be the stimulus you need to learn Morse code. It has some good animated trainers.

Address:

<http://www.ac6v.com/morseprograms.htm>





## Hamuniverse

The title of this web site is not an exaggeration because it is almost unbelievable what has been collected here.

Address:

<http://www.hamuniverse.com/about.html>

Address:

[http://www.minicircuits.com/pages/npa/PMA-545+\\_NPA.pdf](http://www.minicircuits.com/pages/npa/PMA-545+_NPA.pdf)

## High intercept low noise more amplifier with GaAs pHEMT MMIC

It is always interesting to see how other people solve a problem. This complete document shows all the details and is worth a detailed look.

Address:

[www.newsvhf.com/hemt-mmic-wideband-lna.pdf](http://www.newsvhf.com/hemt-mmic-wideband-lna.pdf)

## Ultra Low Noise MMIC Amplifier

If you are looking for an MMIC with a noise figure of 0.8dB, a gain of 20dB, an IP3 of +36dBm, a maximum power output of +20dBm and usable from 50MHz to 6GHz should check this out.

**Download free a copy of CQ-TV 235 magazine**  
<http://www.batc.org.uk/vhfc.html>



# VHF COMMUNICATIONS

*A Publication for the Radio Amateur Worldwide*

*Especially Covering VHF, UHF and Microwaves*

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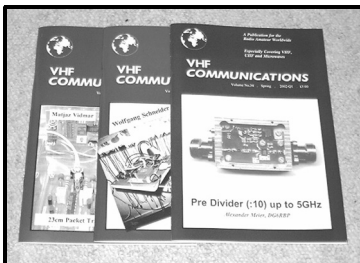
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Tel: (909) 338-6887, email: wa6svt@atvquarterly.com

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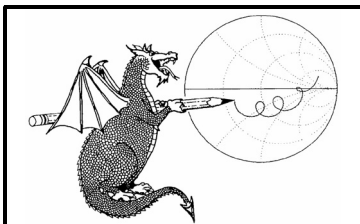
## Back Issues

Available either as photocopies or actual magazines. Issues from 1/1969 to 4/2010 are £1.00 each + postage. Issues from 2011 are £5.35 each or £19.60 for all 4 issues + postage. See web site or page 34 of issue 1/2012 for back issue list. There are two back issue sets that contain the available "real" magazines at a reduced price, see web site for details.



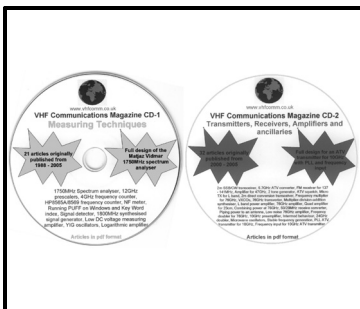
## Blue Binders

A new style binder was introduced in 2010 with an embossed spine. These binders hold 12 issues (3 years) and keep your library of VHF Communications neat and tidy. You will be able to find the issue that you want easily. Binders are £6.50 each + postage. (UK £1.00, Surface mail £2.40, Air mail to Europe £2.50, Air mail outside Europe £4.10)



## PUFF Version 2.1 Microwave CAD Software

This software is used by many authors of articles in VHF Communications. It is supplied on 3.5 inch floppy disc or CD with a full English handbook. PUFF is £20.00 + postage. (UK £0.70, Surface mail £1.45, Air mail to Europe £1.60, Air mail outside Europe £2.60)



## Compilation CDs

Two CDs containing compilations of VHF Communications magazine articles are available. CD-1 contains 21 articles on measuring techniques published in the past few years. CD-2 contains 32 articles on transmitters, receivers, amplifiers and ancillaries published over the past few years. The articles are in pdf format.

Each CD is £10.00 which includes 2<sup>nd</sup> class postage in The UK and surface mail overseas. Air mail postage is £0.60 for Europe and £1.00 outside Europe.



## VHF Communications Web Site [www.vhfcomm.co.uk](http://www.vhfcomm.co.uk)

Visit the web site for more information on previous articles. There is a full index from 1969 to the present issue, it can be searched on line or downloaded to your own PC to search at your leisure. If you want to purchase back issues, kits or PUFF there is a secure order form or full details of how to contact us. The web site also contains a very useful list of site links, and downloads of some previous articles and supporting information.

K M Publications, 503 Northdown Road, Margate, Kent, CT9 3HD, UK

Tel / Fax +44 (0) 1843 220080, Email: [andy@vhfcomm.co.uk](mailto:andy@vhfcomm.co.uk)

# Back Issues on DVD

VHF Communications Magazine has been published since 1969. Up to 2002 it was produced by traditional printing methods. All these back issue have been scanned and converted to pdf files containing images of the A4 sheets that formed the A5 magazine when folded in half. These have been put together on DVD in decade sets.

From 2002 the magazine has been produced electronically therefore pdf files are available of the text and images. These have been used to produce the 2000s decade DVD.

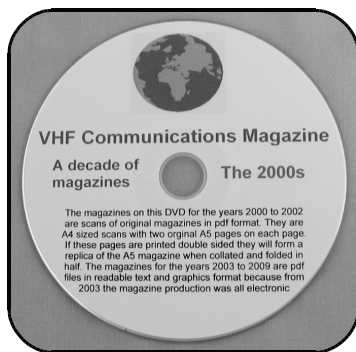


## 1970s - 1980s - 1990s

These three DVDs cover the first 3 decades of the magazine. The 1970s DVD contains all magazines from 1969 to 1979 (44 magazines) the 1980s and 1990s DVDs contain 40 magazines for the decade. The DVDs are £20.00 each

## 2000s

This DVD contains magazines from 1/2000 to 4/2001 in scanned image format and from 1/2002 to 4/2009 in text and image format. This DVD is £35.00



## Bumper 4 decade DVD

This DVD contains all magazines from 1969 to 2009. That is 164 magazines. It also contains the full index for those 41 years in pdf and Excel format so that you can search for that illusive article easily. This DVD is just £85.00 - just 52 pence per magazine.

To order, use one of the following:

- Use the order form on the web site - [www.vhfcomm.co.uk](http://www.vhfcomm.co.uk)
- Send an order by fax or post stating the DVD required (1970s, 1980s, 1990s, 2000s, Bumper)
- Send the correct amount via PayPal - [vhfcomms@aol.com](mailto:vhfcomms@aol.com) - stating the DVD required (1970s, 1980s, 1990s, 2000s, Bumper) and your postal address

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