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Vector analyser VAA 200 for the 0.1 to 220MHz range with graphical display

Bernd Kaa, DG4RBF

Contents

For constructors this is a bumper issue, every article is a great design with all you need to construct something very useful.

Matjaz Vidmar has been working hard on his web site and I have reproduced one of his new designs, a frequency counter. In his usual way this design has some very useful additions to the "standard" offerings. If you like what you see you must take a look at his web site to see the many photographs.

The Vector analyser by Bernd Kaa is a professional piece of test equipment that would be useful in any shack.

The IF amplifier by Henning Christof Wedding is a useful building block, the article contains all of the design decisions made so that those following after Henning will be able to use the AD603 with ease.

Last but not least, Gunthard Kraus has concluded another extremely useful Practical Project, he makes the art of microwave design sound so easy even though we all know that it is far from easy.

Finally, watch out for the new RSGB VHF/UHF Handbook that I spent last winter editing, it has been extensively updated and is due out in October.

73s - Andy

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Matjaz Vidmar, S53MV

A simple RF/Microwave frequency counter

I decided to design a simple, easily reproducible counter around a PIC 16F876A. The basic counter range is extended to at least 180MHz using two 74Fxx devices. A divide-by-64 prescaler is used for higher frequencies up to at least 4.5GHz. All results of the measurement are shown on an inexpensive, 2x16 alphanumeric LCD module with large characters. A block diagram of the counter is shown in Fig 1.

The counter has three front ends: a microwave (prescaled) input, an RF input and a TTL input. The microwave and RF inputs are AC coupled and terminated at low impedance (around 50Ω). The TTL input is DC coupled and has high input impedance. A progress bar indicator is provided on the LCD display for the gate timing.

Both the microwave and RF inputs have an additional feature, usually not found in frequency counters: a simple signal level detector driving a bar indicator on the LCD display. This is very useful to check for the correct input signal level as well as an indicator for circuit tuning or absorption wave meter dip display.

1.

The counter

The whole counter design is based on a 16F876A PIC microcontroller. This includes several peripherals but just a

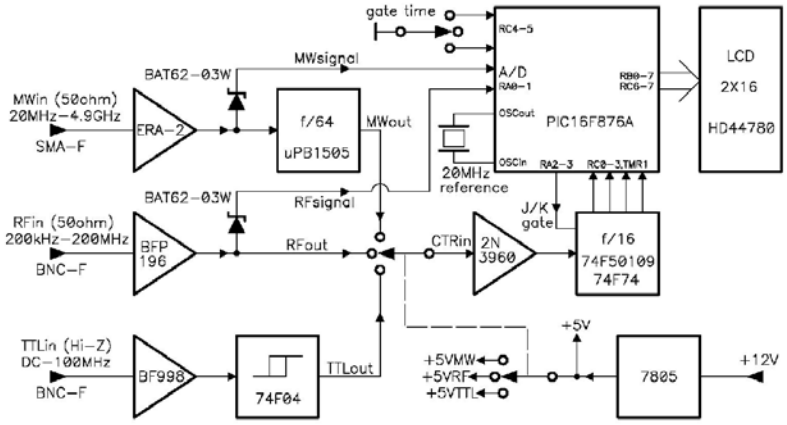


Fig 1: Block diagram of the frequency counter.

few of them are used in this project. The most important in this project are two internal hardware counter/timers called TMR0 and TMR1. The TMR0 timer generates very precise interrupts every 100 microseconds (10kHz) from the 20MHz clock/reference. All required timings for the counter timebase are simply integer multiples of this basic period.

The TMR1 is used as a 16bit (binary) input signal counter. It's maximum counting frequency is just around 16.7MHz. Therefore, the first four flip-flops of the input signal counter chain are added externally as 74Fxxx logic devices. The first two stages use one of the fastest 74Fxxx series devices, the 74F50109 dual J/K flip-flop. The 74F50109 is also specified as metastable immune and is therefore the ideal component for the counter gate. The circuit diagram of the counter is shown in Fig 2.

A more conventional 74F74 dual D flip-flop is used in the third and fourth stages. The TTL flip-flops require pull-up resistors to drive the PIC ports RC0, RC1, RC2 and RC3. RC0 is used as a clock input to the TMR1 at the same time. Replacing the 74F74 with a 74ACT74 could save some current and two pull-up resistors. The 74F50109 has the same pin-out and logical function as the 74F109, but the latter has a lower frequency limit and is not specified metastable free.

The typical frequency limit of the 74F50109 is specified as 150MHz. Driving the 74F50109 with a fast switching transistor 2N3960 (f_t = 1.6GHz) and a schottky diode 1N5712 to prevent saturation, reliable counting can be achieved up to 190 - 200MHz! Unlike conventional AND or OR gates, the J/K gate minimises the jitter of the counting result (wandering of the last digit) regardless of the input signal. Since the /K input of the 74F50109 is inverted, two port pins (RA2 and RA3) of the PIC are required to drive the J and /K inputs with minimal skew.

On the other end, the counter needs to be extended beyond the 4 bits of the 74Fxxx logic and 16 bits of the TMR1 are used adding up to 20 bits of resolution. To avoid disrupting the operation of the main 100µs timer, the TMR1 is not allowed to generate interrupts. The TMR1 overflow (interrupt) flag is checked during every 100µs (TMR0) interrupt. The overflows are counted in two additional 8 bit registers. The overall counter resolution is therefore 36 bits.

These 36 bits are truncated to 32 bits, the upper 4 bits are not used. 32 bits allow counting beyond 400MHz with a resolution of 0.1Hz (gate time 10s). None of these counters is ever reset! The counter value at the beginning of the measurement is stored and subtracted from the end value. Finally, the 32 bit binary result is converted to a 10 digit decimal number and the latter is displayed with the leading zeros blanked, decimal point and units (MHz or kHz).

The basic counter software allows three resolutions (selected with RC4 and RC5): 10Hz, 1Hz and 0.1Hz in direct counting mode (no prescaler), corresponding to gate times of 100ms, 1s and 10s. When used with a divide-by-64 prescaler, the three available resolutions become 1kHz, 100Hz and 10Hz, corresponding to gate times of 64ms, 640ms and 6.4s. All these gate times are obtained by counting the 100µs (10kHz TMR0) interrupts.

The PIC 16F876A drives a standard LCD module with a HD44780 controller and a resolution of two rows of 16 characters each. The HD44780 requires 8 data lines (port B of the 16F876A) and three control signals: Register Select (RC6), Read/Write (GND) and Enable (RC7). Since the data presented on the 8-bit-

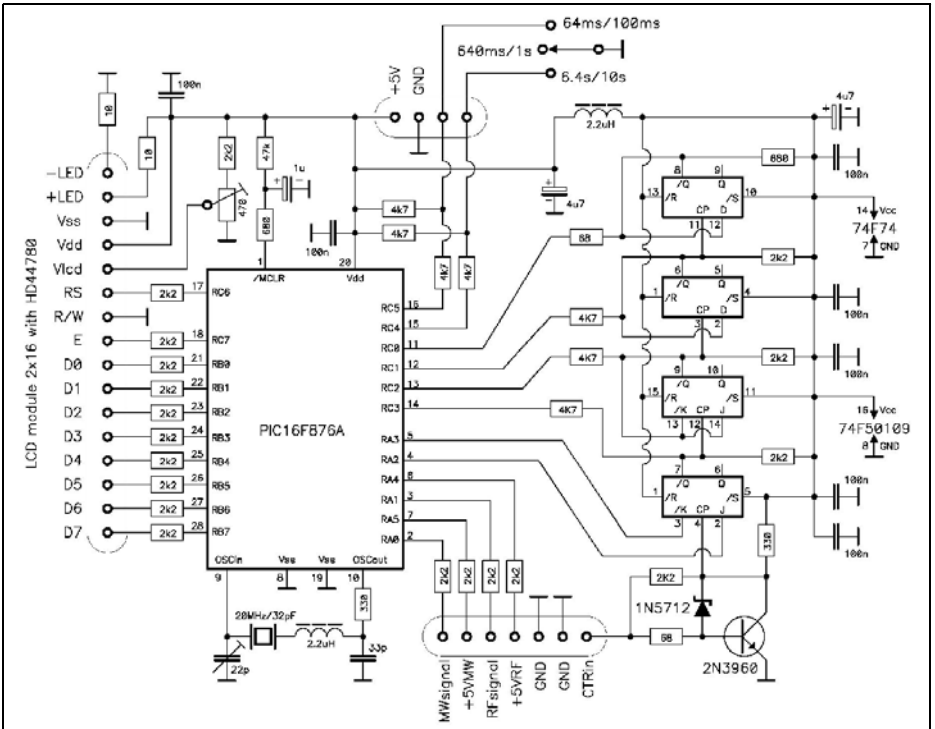


Fig 2: Circuit diagram of the frequency counter.

wide output port RB0-7 is only written to the HD44780, the R/W input is hardwired to ground (/Write). The LCD back light LEDs are supplied through two 10Ω current limiting resistors.

The input signal level is fed to the only

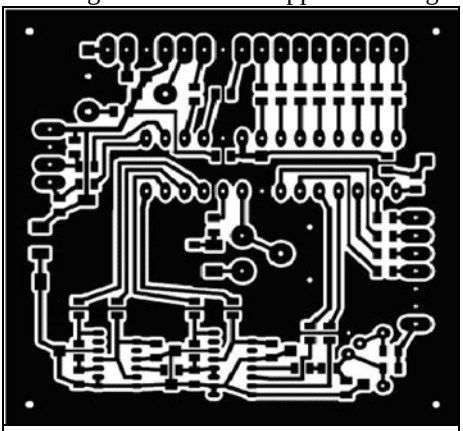


Fig 3: PCB layout for the frequency counter.

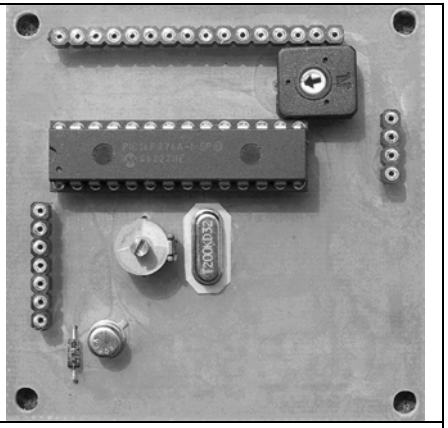


Fig 4: Picture of the component side of the counter PCB.

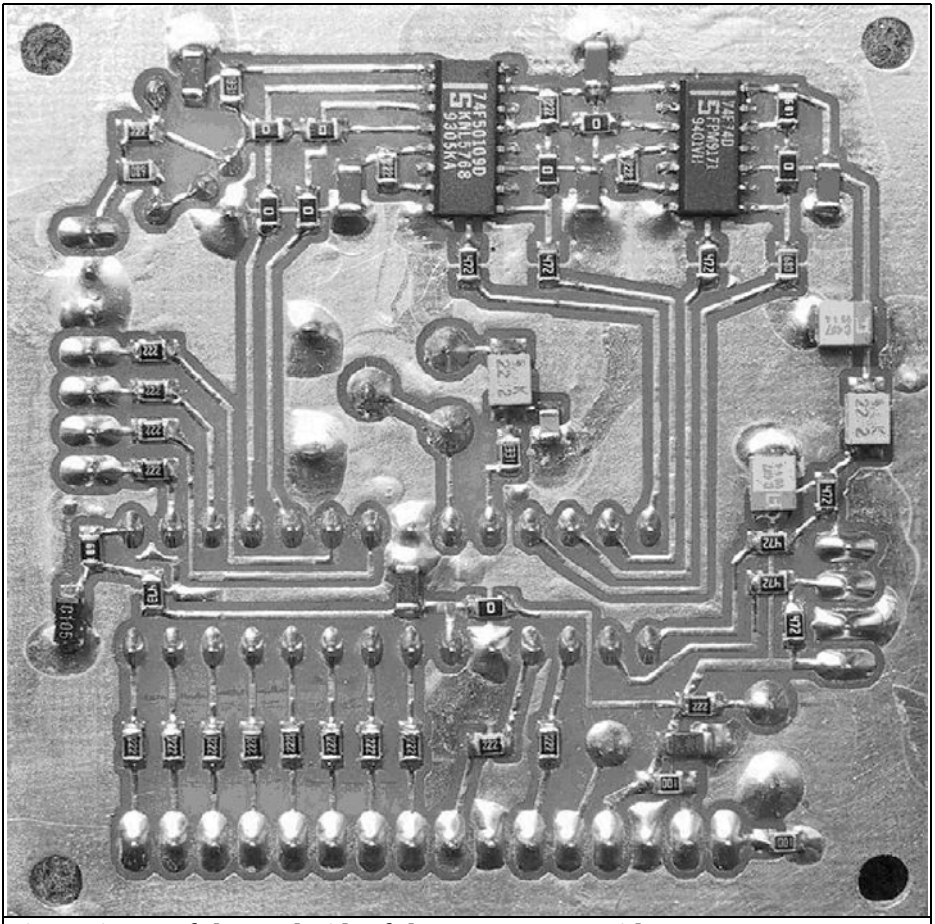


Fig 5: Picture of the track side of the counter PCB with SMD compoenets fitted, note the 0R links.

remaining PIC peripheral used in this project, the A/D converter. The latter has a resolution of 10 bits, but only the most significant 7 bits are used. These drive a bar indicator on the LCD module with 36 segments, corresponding to an input voltage between zero and 1.4V (full scale) on the analogue inputs RA0 (MW mode) or RA1 (RF mode). The operating mode is selected with switches driving the digital inputs RA4 and RA5.

The main counter module is built on a single sided printed circuit board measuring 60mm x 60mm. Good quality IC sockets are used for the PIC 16F876A and as connectors. The PCB layout is shown in Fig 3 and the component layout in Figs 4 and 5.

Most of the components are in SMD packages and are installed on the bottom (solder) side of the printed circuit board. Due to the single sided circuit, many jumpers are required. The PCB is designed for 0805 jumpers shown as 0R on the picture of the completed board Fig 5.

A 20MHz crystal is used both as a clock

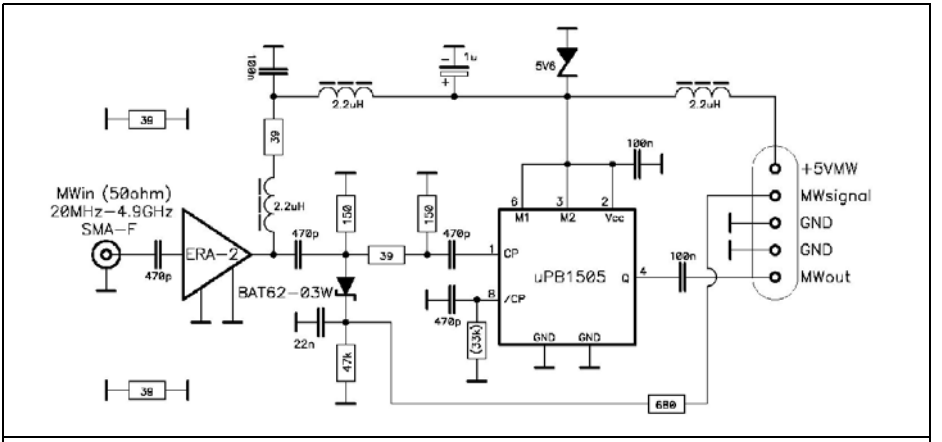


Fig 6: Circuit diagram of the microwave prescaler.

source for the PIC and as a frequency reference for the frequency counter. 20MHz crystals are usually designed either for 20pF - 32pF parallel resonance or series resonance. Since the internal oscillator inside the PIC 16F876A is not able to oscillate on the correct frequency with large capacitors, a series inductor is required to bring the crystal on the exact frequency. The recommended 2.2μH inductor is suitable for 32pF parallel resonance crystals.
Of course, the PIC 16F876A is also able to operate with an external clock source. This has to be connected to pin 9 while pin 10 is left open. If a high quality frequency reference for 5MHz, 10MHz or 100MHz is available, it is recommended to multiply or divide its output to obtain the required 20MHz clock.
Other clock frequencies than 20MHz can be accepted by modifying the software to obtain the 10kHz TMR0 interrupt. The TMR0 time constant allows changing the clock in 80kHz frequency steps (4 clock cycles per instruction and divide-by-2 prescaler for the TMR0). Smaller clock steps of 40kHz can be obtained by inserting NOP instructions in the TMR0 interrupt routine, for example using a high quality (telecom SDH) TCXO for 19.44MHz.

2.

Front ends

The counter is equipped with three different front ends. The front ends are built as separate modules to allow an easy interchange as better components (prescalers) become available or new requirements show up.

2.1 Microwave prescaler

The microwave prescaler front end is designed around the NEC μPB1505 chip, the circuit diagram is shown in Fig 6. This counts up to 4.9GHz and unlike the products from some other manufacturers it is very reliable. An ERA-2 MMIC is used to boost the input sensitivity and provide some protection for the μPB1505. The ERA-2 can accept input signal levels up to +15dBm (30mW). A 6dB attenuator behind the ERA-2 prevents saturating the μPB1505.

A 33kΩ resistor can be used to kill the self oscillation of the μPB1505 around 2.6GHz, but this resistor also adversely affects the sensitivity and the maximum

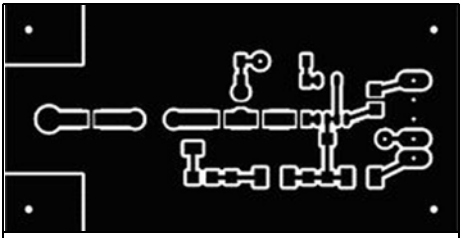


Fig 7: PCB layout for the microwave prescaler.

frequency of the prescaler. A BAT62-03W zero bias schottky diode is used as a signal level detector. The gain of the ERA-2 sets the full scale on the bar indicator to about 0dBm.

The microwave prescaler front end is built on a single sided printed circuit board measuring 30mm x 60mm. The PCB layout is shown in Fig 7 and the component layout in Fig 8. The 50Ω lines are built as coplanar waveguides on a 1.6mm thick FR4 substrate. The input cable is soldered directly to the PCB. To avoid parasitic resonances between the PCB and metal ground plane, two additional 39Ω damping resistors are installed in series with two mounting screws.

2.2 RF front end

The RF front end is designed for a high input sensitivity and low (close to 50Ω) input impedance. The circuit diagram is shown in Fig 9. A high input impedance (as offered in many counters) is actually a disadvantage for RF measurements, last but not least corrupting the measurements due to low frequency (50Hz mains or switching powers supply) interference. The RF front end includes a simple RF amplifier with a BFP196 transistor, an input protection with a 33Ω resistor and a LL4148 diode and a signal level detector using a BAT62-03W zero bias schottky diode.

The RF front end is built on a single sided printed circuit board measuring 20mm x 60mm. The PCB layout is shown in Fig 10 and the component layout in Fig 11

The input cable is soldered directly to the PCB. Since the RF front end does not include any hysteresis, it is not able to operate with sine wave signals at very low frequencies.

2.3 TTL front end

The TTL front end is a high impedance input. DC coupling is necessary to measure pulses with arbitrary duty cycles. The circuit diagram is shown in Fig 12 Further it includes hysteresis for reliable low frequency measurements, regardless of the waveform. The circuit includes a BF998 MOSFET source follower and a 74F04 schmitt trigger. The output of the schmitt trigger is again DC coupled to the 2N3960 in the main counter module.

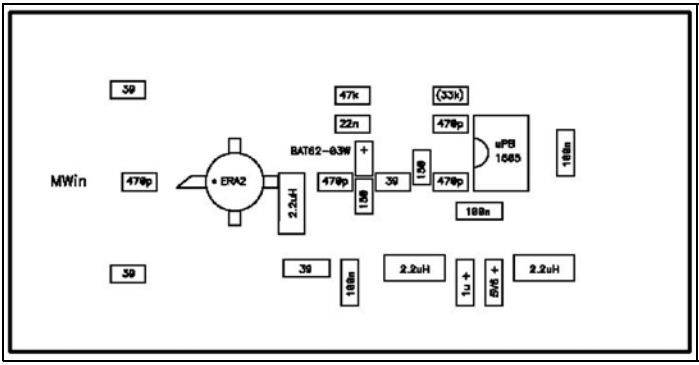


Fig 8: Component layout for the microwave prescaler.

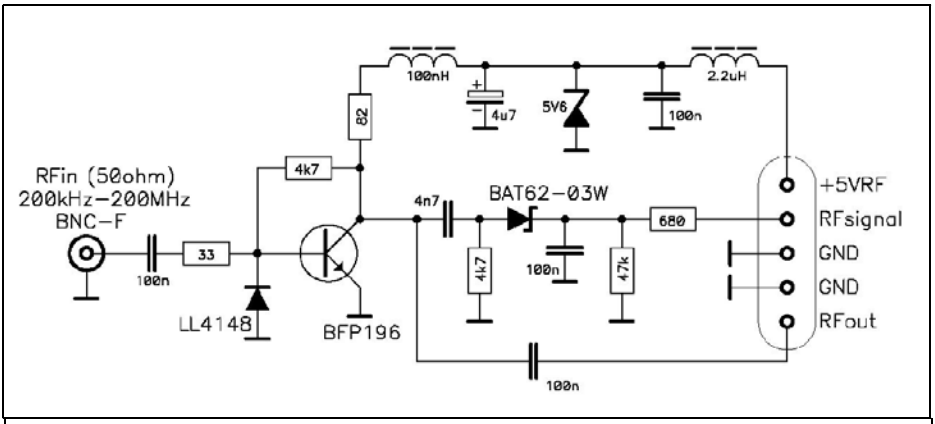


Fig 9: Circuit diagram of the RF front end.

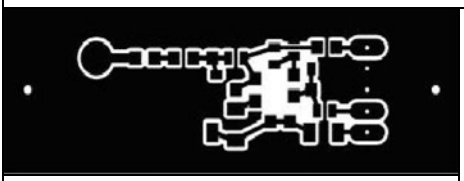


Fig 10: PCB layout for the RF front end.

The TTL front end is built on a single sided printed circuit board measuring 20mm x 60mm. The PCB layout is shown in Fig 13 and the component layout in Fig 14. The input cable is soldered directly to the PCB. Input protection is provided by the 470Ω resistor and the zenner diodes inside the BF998 (breakdown voltage between 8V and 12V). Further protection could be obtained by additional zenner diodes, however the latter may include a large capacitive loading (more than 100pF).

3.

Assembly

All counter modules require a +5V power supply. A 7805 regulator is a simple and efficient solution. Some additional components are required for interference and switching transient suppression. The circuit diagram of the power supply is shown in Fig 15 The 7805 regulator is bolted directly to the rear panel for heat sinking.

Two DPDT switches are used for front end selection. An additional switch is used to select the gate time.

All four printed circuit boards are single sided, etched on 1.6mm thick FR4 laminate (image resolution is 150dpi).

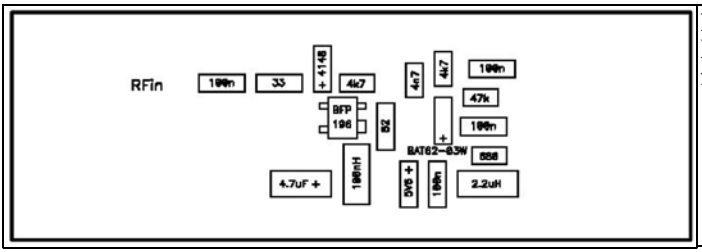


Fig 11: Component layout for the RF front end.

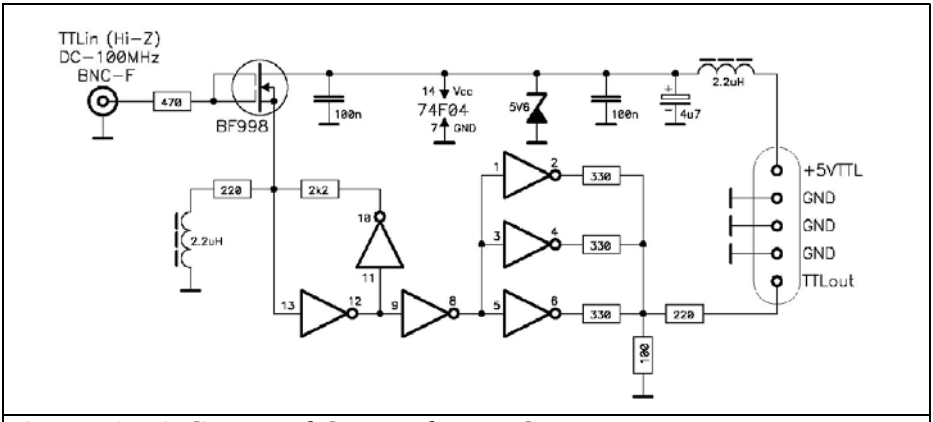


Fig 12: Circuit diagram of the TTL front end.

Fig 13: PCB layout for the TTL front end.

The counter is installed in a box made of aluminium sheet shown in Fig 16. The bottom is made from 1mm thick aluminium sheet, the cover is made from 0.6mm thick aluminium sheet and the LCD is protected by a small piece of plexiglass. The internal width is 200mm, depth 100mm and height 45mm.

The RF connectors, switches and LCD module are installed on the front panel. The power supply connector is installed on the rear panel.

4.

Operation

Immediately after power up, the counter displays the software version/date for about one second.

During normal operation, the leftmost characters of both rows are used as a vertical bar display of the gate progress with 10 horizontal segments. The remaining 15 characters in the top row of the display show the measured frequency. Three characters in the bottom row show the operating mode ("MW", "RF" or "TTL") and the remaining 12 characters are used as a horizontal bar display of the signal strength with 36 vertical segments.

In the microwave mode both prototypes

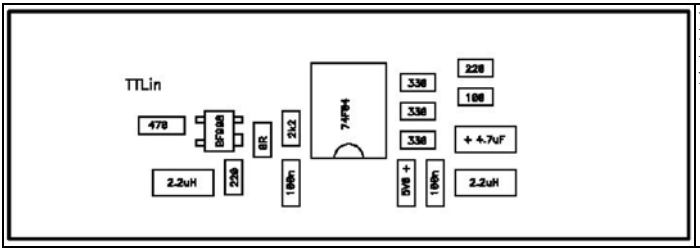


Fig 14: Component layout for the TTL front end.

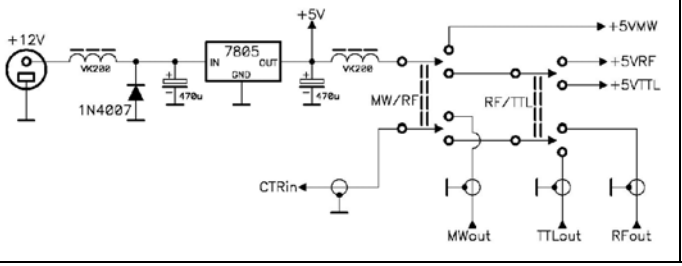


Fig 15: PSU circuit diagram for the frequency counter.

operated reliably up to 4.9GHz with an input signal level of 0dBm (self oscillating μPB1505 without 33kΩ resistor). Below 3GHz the sensitivity improves to -30dBm. The 33kΩ unbalancing resistor to stop self oscillations degrades this sensitivity by more than 10dB! Below 500MHz the sensitivity degrades again: the counter may count odd harmonics with too low signal levels. The minimum usable frequency was found around 12MHz. Fig 17 shows the counter in the microwave mode with a gate time of 640ms corresponding to a resolution of 100Hz.

In the RF mode the 74F50109 allows counting up to about 220MHz. Reliable operation is possible up to 190-200MHz, depending on the internal wiring to the switches, with an input-signal level of 0dBm. The sensitivity improves from -20dBm at 180MHz down to -50dBm at 10MHz. The RF signal-level meter follows a similar increase in its sensitivity. This increase at lower frequencies matches the performance of the described loop probes!

Unfortunately, the 74F50109, manufactured by Signetics (Philips) is not easily available. A 74F109 from the same manufacturer only operated up to about 140MHz. A combination of 74AC109 and 74AC74 (both from National Semiconductor) counted up to about 170MHz. The 74ACxxx logic circuits require a different input DC bias: replace the 2.2kΩ resistor between the input and the collector of the 2N3960 with a 47kΩ resistor. All four pull-up resistors can be omitted with 74ACxxx logic. Finally, the 2N3960 itself does not have many valid replacements. A 2N2369 will decrease the 74F50109 counting rate down to just 165MHz while RF and microwave transistors provide

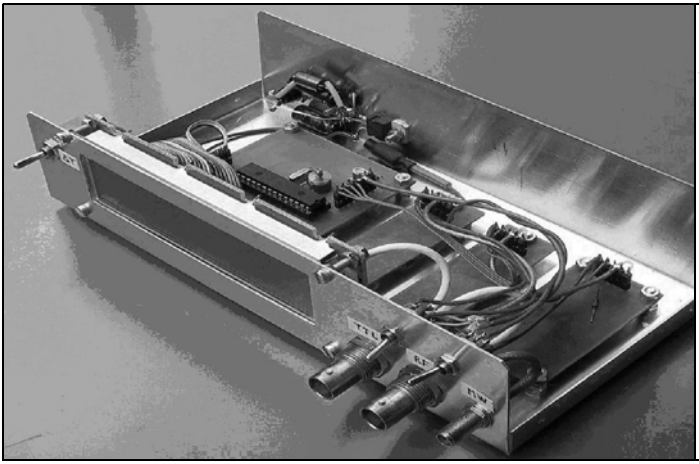


Fig 16: A picture of the completed frequency counter.

Fig 17: The counter in the microwave mode with a gate time of 640ms corresponding to a resolution of 100Hz.

even worse results!

In the TTL mode the prototypes operated reliably beyond 100MHz. This frequency limit is however reduced by the coaxial cable feeding TTL signals and even more when using oscilloscope probes. The input signal level is not indicated in the TTL mode. The built in hysteresis allows reliable counting of very low frequencies, like the 50Hz mains.

The current software version does not detect the mode switching before the end of the gate period. Therefore one may have to wait up to 10 seconds for the gate period to expire and another 10 seconds to get some meaningful reading. The current software also does not make any use of the measured signal level. Therefore it will display the self oscillating frequency of the prescaler with no signal input in the microwave mode or any other invalid data due to low signal levels in the RF or microwave modes.
The software is designed using the same rules as the whole counter: keep this project useful, simple and straightforward. A simple prescaler is therefore used in place of a considerably more complex direct microwave counter. Some simple 74Fxxx logic ensures enough overlap between the prescaled microwave frequency range and the direct RF frequency range. A TTL input with hysteresis is an efficient solution for low frequencies and extreme duty cycles. Finally, an input signal level indicator is an inexpensive but very useful addition to a frequency counter.

Last but not least, all detailed information like PCB files or software source code are available on Matjaz Vidmar's web site [2].

5.

Probes

A very common problem of many frequency counters is that these are supplied to the end user without (any) suitable probes! In fact, most RF/microwave sources cannot be connected directly to a counter input. The conventional oscilloscope probe is not a good solution for most RF/microwave measurements either. Worst of all, most counters are not even designed to be used with some useful probe types.

Any serious RF/microwave engineer has his/her own set of suitable attenuators, circulators, loads and directional couplers to connect spectrum analysers, power meters, counters and other instruments to the circuit under test. A complete set of transitions between different RF connectors is also required. Finally, a number of pigtailed connectors to be soldered directly to the circuit under test is always of great help.

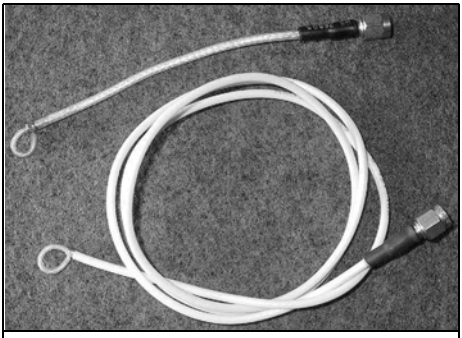


Fig 18: Loop probes.

A very useful probe to be used with RF/microwave counters is a simple inductive pickup or in other words a 5mm diameter loop at the end of a short length of 50Ω coaxial cable. According to my own experience it does not make sense to make this loop much smaller or larger than 5mm. The same loop can be used from a few MHz up to several GHz. A small resistor (around 50Ω) can be installed in series with the loop to suppress any cable resonances.

The loop is simply approached to inductors or resonators in the circuit under test (Fig 18). The undesired loading of the circuit can be minimised by keeping the loop at the maximum distance that still provides a stable reading on the counter. Finally, the loop probe is never affected by low frequency (50Hz mains or similar) interference. Since the coupling to the circuit under test is not very efficient, it is rather unlikely to damage the counter with large RF signal levels.

A standard oscilloscope probe is a practical solution to measure low frequencies, pulsed signals and in some cases even RF signals. In order to use an oscilloscope probe efficiently, the internal operation of the probe has to be understood (Fig 19). Most probes are equipped with a X1/X10 switch. Further there is a series damping resistor (around 500Ω) to avoid cable resonances that could both corrupt the oscilloscope display and severely disturb the circuit under test. Finally, one should understand that although the TTL input of the counter operates in excess of 100MHz, the oscilloscope probe may reduce the upper frequency limit to 50MHz or even less!

6.

References

[1] 13GHz prescaler, Zeljko Bozic, VHF Communications Magazine, 2/2006, pp 89 – 94

[2] Matjaz Vidmar web site for frequency counter http://lea.hamradio.si/~s53mv/counter/history.html

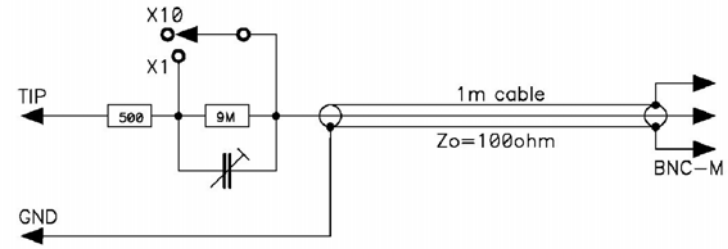


Fig 19: Circuit diagram of a standard oscilloscope probe.

Bernd Kaa, DG4RBF

Vector analyser VAA 200 for the 0.1 to 220MHz range with graphic display

Correct adjustment of individual building blocks or antennas to transmitters is extremely important. The graphic analyser described in this article displays swept values to allow adjustment of the relevant components. It is possible to identify complex adjustment conditions indicated separately and plotted as curve over the frequency range. The phase and impedance as well as the real and imaginary part can be represented for adjustment. It is even possible to determine if the imaginary part is inductive or capacitive and to convert it to the correct value.

Measuring and adjustment analysers are available on the amateur radio market (SWR analysers), most cannot measure the impedance as well as the real and imaginary part. If they are able to measure both the information is represented numerically not graphically. Only a few commercially available analysers offer a graphical display at a reasonable price.

1. Description of the circuit

The heart of the circuit is a modern DDS component, type AD9952, which is specified for a clock frequency up to 400MHz. Because it has an internal

Fig 1: Picture of the vector analyser.

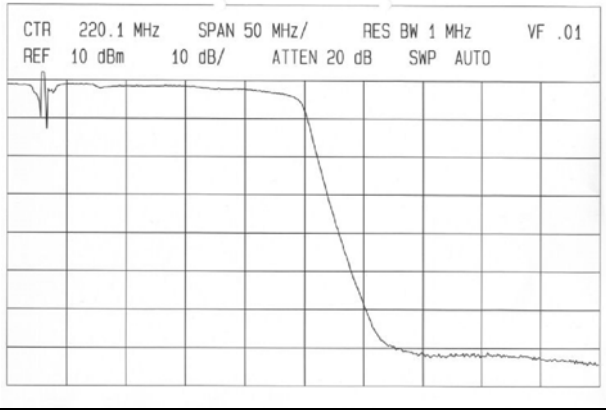


Fig 2: Frequency response of the 15 pole low pass filter.

multiplier, it can simply be fed with a 36MHz TTL oscillator.

Data from the microcontroller is fed to the DDS IC using simple voltage dividers. These voltage dividers are necessary, in order to reduce the 5V TTL signals from the microcontroller to the 1.8V required by the DDS IC. It is important that both outputs (IOUT and IOUT\) are used to produce the output signal so that the unwanted common mode signals developed inside the DDS IC are effectively suppressed. A small centre tapped transformer is used with the centre tap connected to the supply VDD. Two 51Ω resistors are connected from the outputs to the supply to give clean outputs from the DDS IC.

A 15 pole low pass filters with a very steep cutoff ensures that a large frequency range can be used that approaches close to the theoretically usable maximum frequency of F-clock/2. The frequency response of the filter is shown in Fig 2, it has a cutoff frequency of 210MHz. At 220MHz it already has approximately 8dB attenuation. The DDS is operated with 468MHz giving a usable frequency up to 220MHz. Tests of several components showed that this DDS operates well with still higher clock frequencies.

The AD9952 is operated from only 1.8V and has a pleasantly low current consumption. The IC does not warm up much during over clocking so it does not have to be cooled. Soldering the earth surface of the IC to the PCB is sufficient cooling.

A GALI51 (MMIC) with 18dB gain brings the signal up to a level of approximately +5 to +10dBm. A level control is not necessary. Since the AD8302 only evaluates the difference in level of the two input signals, the maximum frequency up to 220MHz can be used.

Measurements are made using a directional coupler (PDC 20-3BD) from Mini Circuits. This is specified for a frequency range from 0.2 to 250MHz and a typical attenuation in the upper range of 30dB. Used with the gain and phase detector AD8302 from Analog Devices it is possible to easily measure the magnitude and phase separately and evaluate them with a microcontroller. The magnitude is a logarithmic output voltage covering the range from +30dB to –30dB. Since +30dB is not used, the resistors R24, R30, R31 shift it to the +10dB to –30dB required. The phase difference is available only within the range of 0 to 180°. The sign is only determined by the microcontroller.

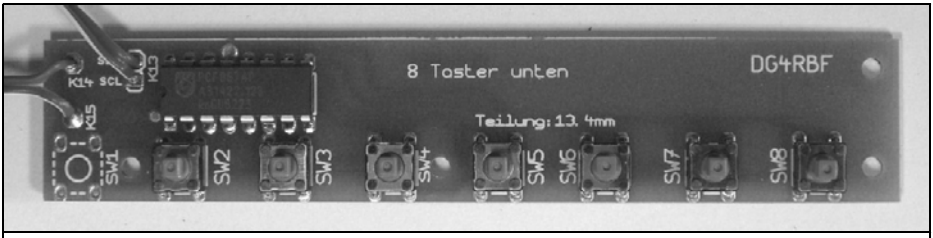


Fig 3: Picture of the switch PCB.

1.1. The microcontroller

The main calculations are performed after measurement by an efficient microcontroller. The AD8302 supplies the raw data in the form of two voltages (MAG and PHS) these are fed to two internal 10 bit analogue to digital converters in the microcontroller to be converted to digital form for further processing.

I had to use mathematics of complex numbers in the microcontroller. For this and for the graphical output a high arithmetic performance is necessary, which the ATMega32 supplies clocked at 20MHz. This microcontroller has a fast processor core and needs no external memory. The system software is programmed directly in the microcontroller. With 32KB of program memory, 2KB internal SRAM and 1KB internal EEPROM it is well suited for this application.

A Lehner Dabitros process card display (YL24012-70) with 240 x 128 pixels is used for the graphical display. It uses the T6963C graphics controller and has a display area of 114.0mm x 64.0mm. The display speed is sufficiently fast in order to be used for alignment work.

The controls are performed using 7 push buttons mounted on a switch board below the display so that legends can be shown on the graphical display. To keep the wiring simple an I^2C bus is used so that only two control lines plus the supply voltage are needed for the switch board. The switch PCB is shown in Fig 3, it is attached to the I^2C bus at K6

1.2. Null of the phase by means of phase line and software nulling

Because the directional coupler, the input connector, as well as the connection cable cause a phase shift, it is necessary to provide for nulling of this phase shift. Two possibilities are available with this equipment:

I. Hardware solution

A phase line, described later, can be used to correct the phase shift.

The phase shift in the forward branch is balanced by a phase line in the return branch. This phase line compensates for the phase shift up to the output connector.

II. Software solution (cable nulling function)

An automatic nulling function is available. If the ZERO key is pressed for approximately 3 seconds, the phase values of the connections are read and stored in the non volatile memory of the microcontroller (EEPROM). If the ZERO function is on during a measurement the stored phase difference is taken into account. The values stored are retained even if the equipment is turned off. For high measuring accuracy the nulling process should be repeated after

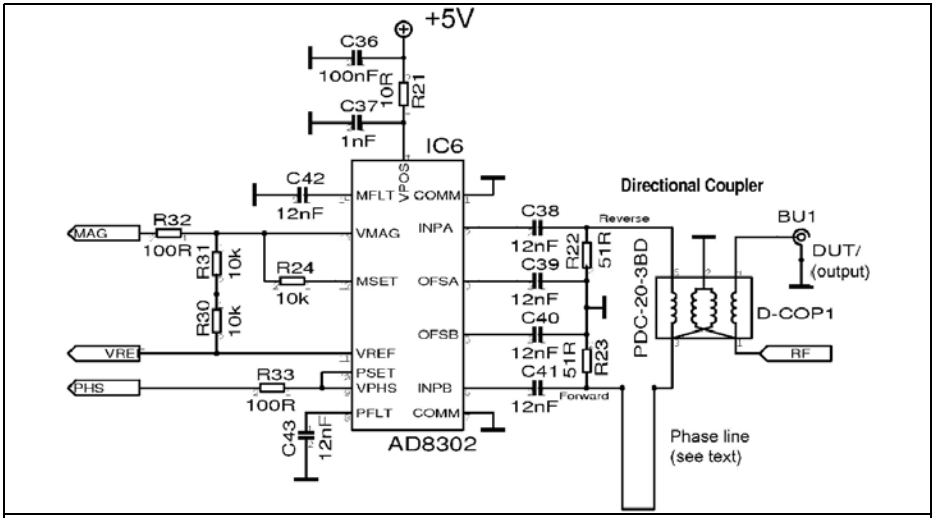
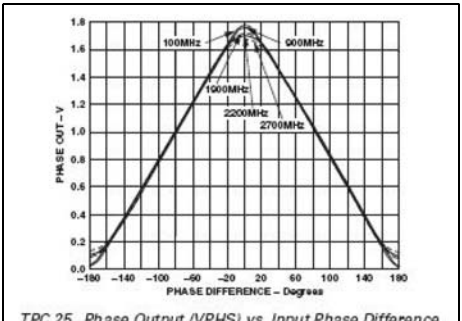


Fig 4: Circuit diagram of the AD8302 log detector with phase and magnitude output.

changing frequency range and the connection cables should be kept as short as possible.

1.3. Gain and phase of detector AD8302

The AD8302 shown in Fig 4 simply evaluates the gain and phase difference between two signals. The gain and phase difference of the reference signal and the reverse signal from the directional coupler are produced as two output voltages. The reference signal does not even have to be level regulated, since only the difference of the two signals is evaluated. This is only possible using the sweep function to 220MHz.



TPC 25. Phase Output (VPHS) vs. Input Phase Difference, Input Levels –30 dBm, Frequencies 100 MHz, 900 MHz, 1900 MHz, 2200 MHz, Supply 5 V, 2700 MHz

Fig 5: Phase difference characteristics of the AD8302.

Unfortunately the low cost of the AD8302 has its price, i.e. in the form of system dependent inadequacies. Like, the phase difference is somewhat inaccurate in the range around 0° and 180°. This is shown in Fig 5 taken from the data sheet. The next problem is that the output is only one voltage, which at the same time represents a phase difference of 0 to 180° and 0 to -180°. That means that it would not be possible to differentiate between the inductive and the capacitive components. Since this is desirable for the vector analyser, a solution was sought to separate the positive phase position from the negative. The safest way would be to use two signals with exactly 90° of phase shift for the evaluation. This would mean a substantial more complicated circuit in the frequency generator. In order to avoid this, the problem was solved by software. The sign is determined by the microcontroller. This way proved as useful alternative.

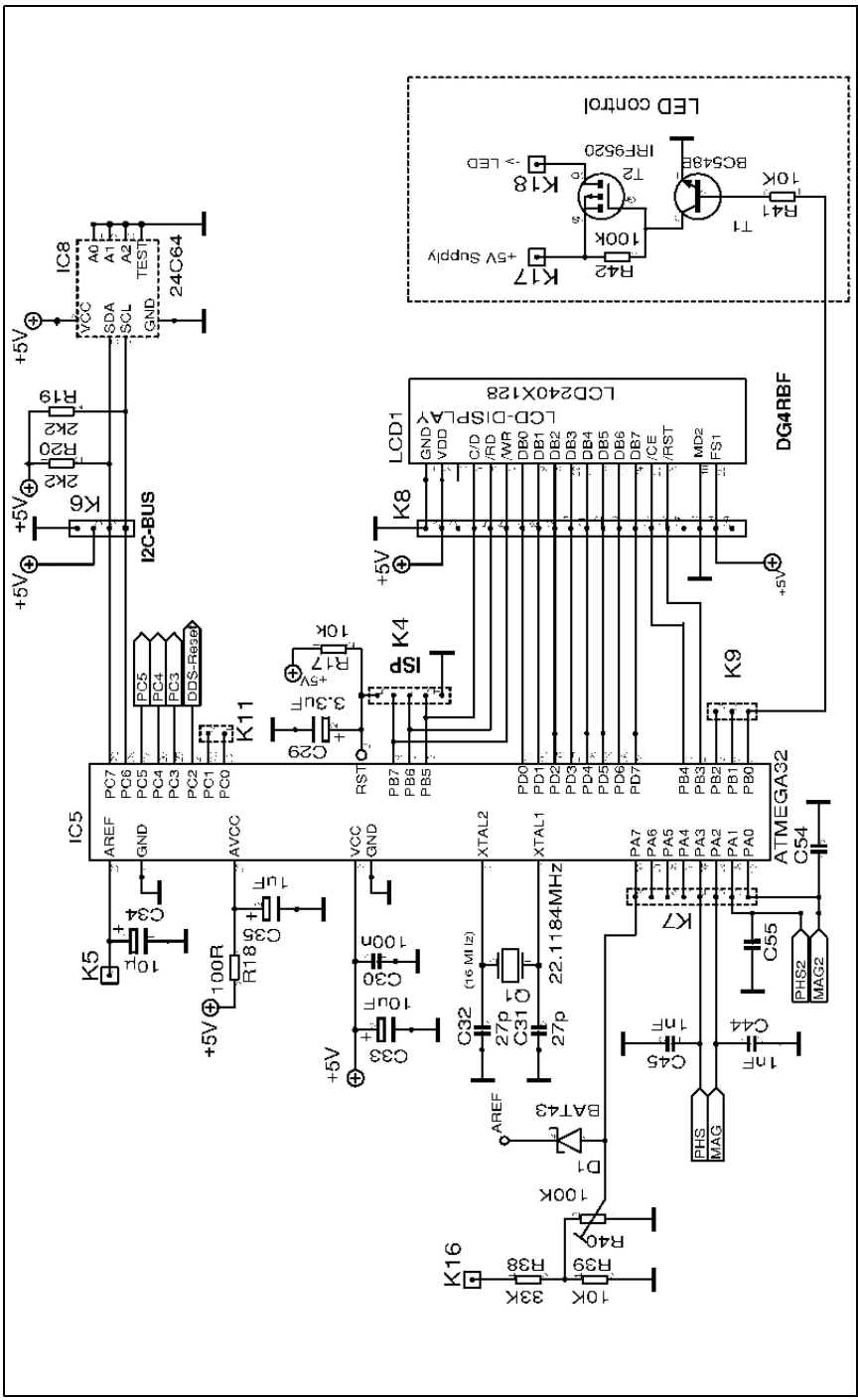


Fig 6: Circuit diagram of the microcontroller section of the analyser.

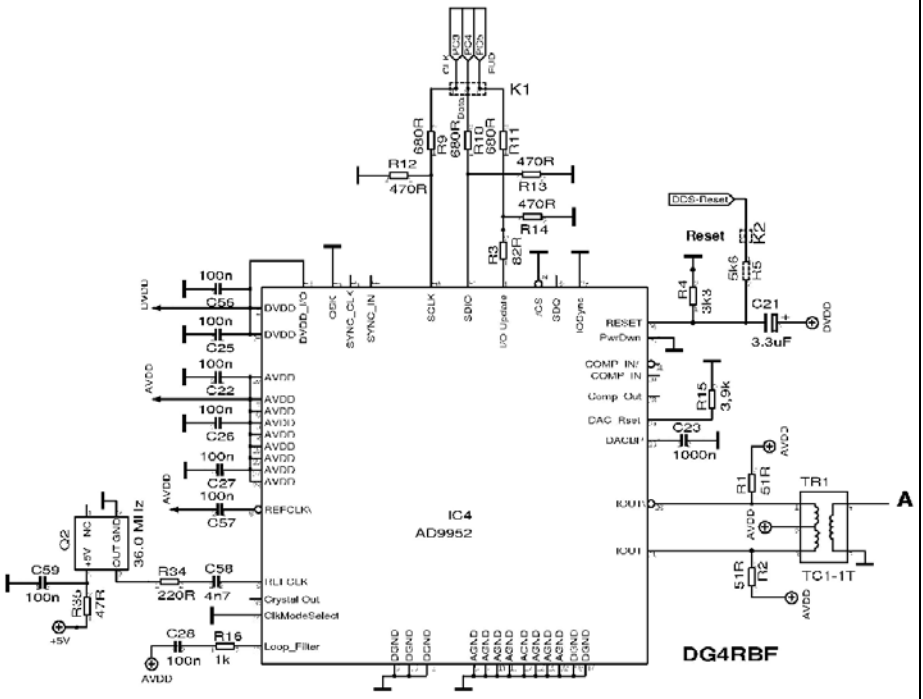


Fig 7: Circuit diagram of the DDS section of the analyser.

1.4. Circuit diagram

The circuit diagram of the microcontroller section is shown in Fig 6. The display is connected to K8 (Pin 1 - Pin20). The connections are shown in Table 2. Since the display backlight requires a high current (approximately 600mA), two transistors T1, T2 controlled by key 7 are used to switch the backlight on and off.

The battery voltage can be measured and indicated in the synthesiser mode. For this the battery is connected to K16 and the indicated voltage adjusted with R40.

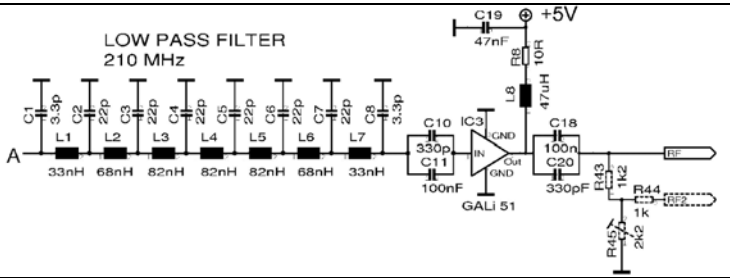


Fig 8: Low pass filter and amplifier for the DDS.

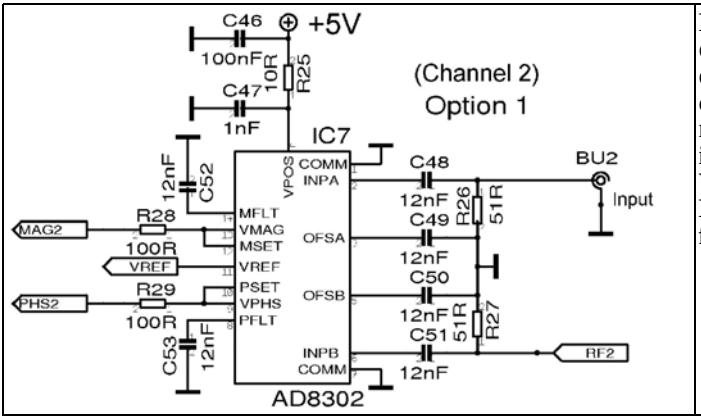


Fig 9: Circuit diagram of the optional second channel. This has not been fully implemented yet. Watch Bernd Kaa's web site [2] for any updates.

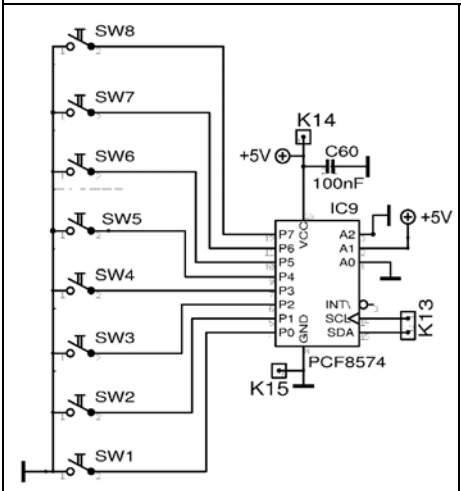


Fig 10: Circuit diagram of the push button controls.

The circuit diagram for the DDS section is shown in Fig 7 and Fig 8. The components in dashes are not fitted nor are the option 1 (second channel) that is still being developed (Fig 9). The remainder of the circuits are shown in Figs 10 and Fig 11.

2.

Everything on one plate

The complete circuit is built on a 72mm x 109mm double sided PCB that can be fitted into a standard tinplate housing. The PCB layout is shown in Fig 12 with the component layout of the SMD side

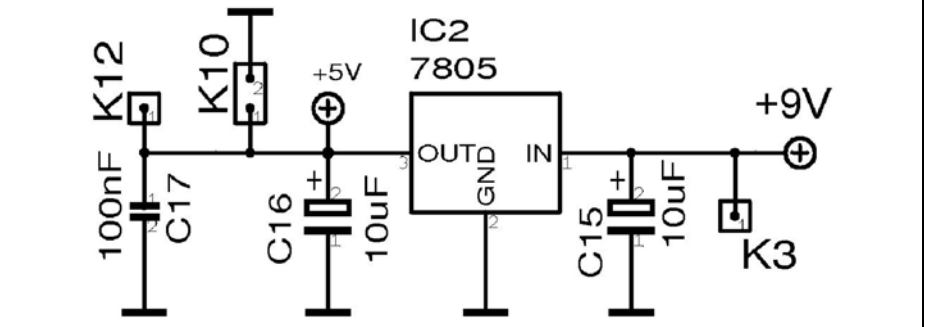


Fig 11: Circuit diagram of the power supply.

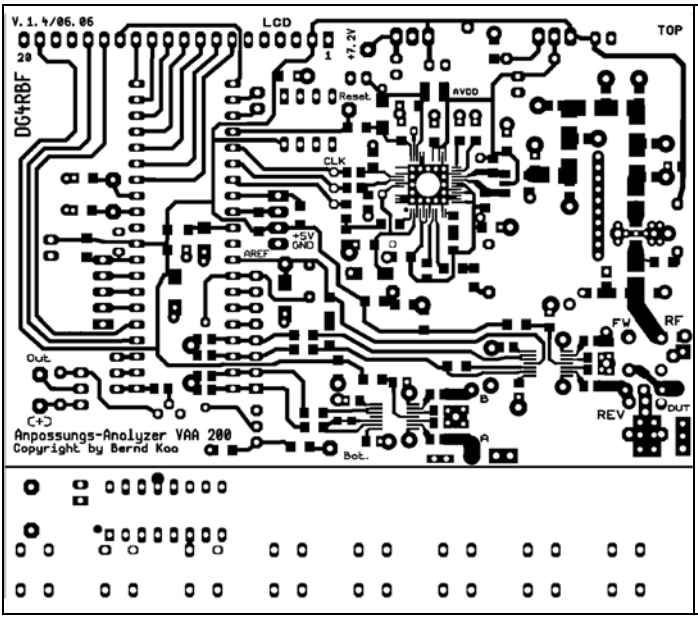


Fig 12: Layout for the track side of the vector analyser PCB.

shown in Fig 13 with a picture of that side of the board with the SMD components mounted in Fig 14. The component layout of the component side is shown in Fig 15 with a picture of that side of the board with the components mounted in Fig 16.

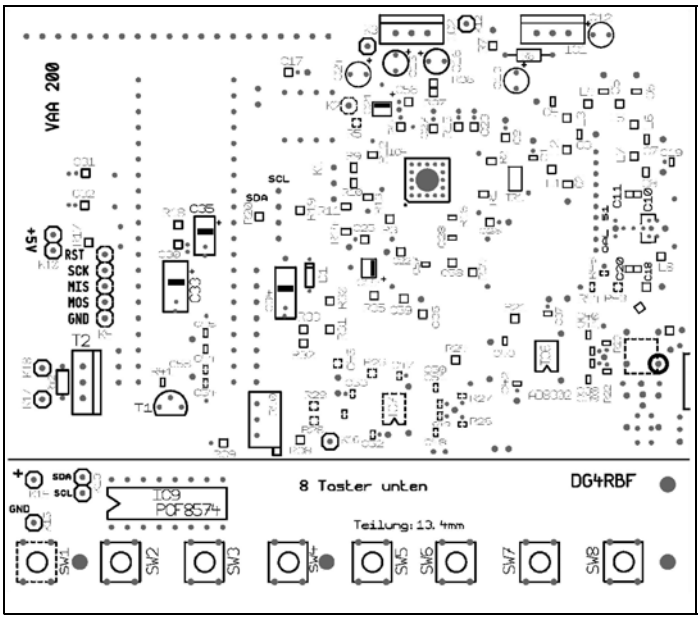


Fig 13: Component layout for the track side of the vector analyser PCB showing the SMD components.

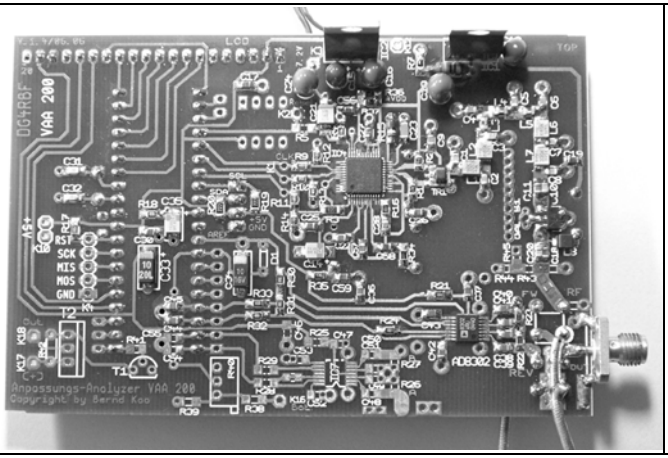


Fig 14: Picture of the track side of the vector analyser PCB showing the SMD components.

3. Construction

At first site, soldering the DDS IC with its close spaced legs looks difficult. If the following method is used, then it is problem free for a practiced amateur constructor. Soldering is assisted because the unused pads are omitted (see Fig 17).

The following soldering procedure worked satisfactorily:

- Tin the pads with a normal soldering iron using a short soldering time so that as much flux as possible stays on the pads. Applying a fluxing agent after tinning is very helpful.
- Position the IC exactly on the pads and solder the corner pins firmly using a soldering iron with an SMD

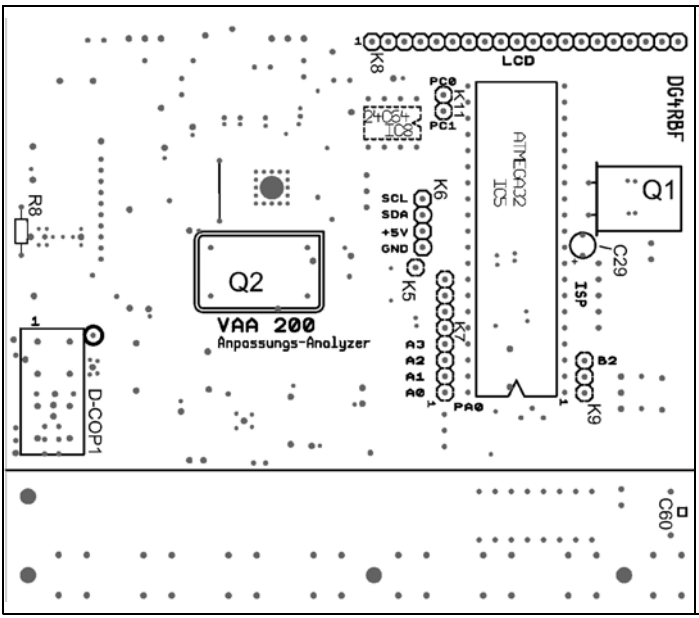


Fig 15: Component layout for the top side of the vector analyser PCB showing the ICs and wired components.

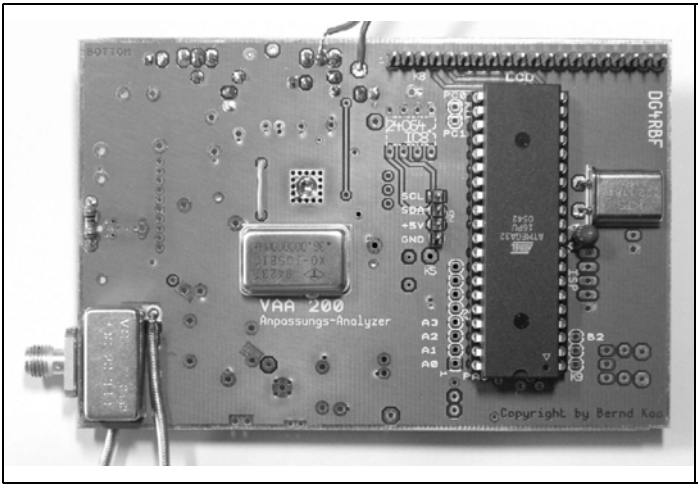


Fig 16: Picture of the top side of the vector analyser PCB showing the ICs and wired components.

tip. A magnifying glass is helpful for this operation. Pressing the hot soldering iron downward is sufficient for the solder and flux on the pads to make a good joint.

- Before soldering the other pins, check the correct positioning of the IC.
- Solder the remaining legs. Short circuits between the legs is prevented because the solder is drawn from the pads.
- After soldering all pins use a magnifying glass to check the joints.
- The lower surface of the IC is an earth surface that must be soldered using the holes in the PCB (see Fig 18). Using a fluxing agent is very helpful. The soldering procedure should not last for a long time so that the IC is not overheated. Use a soldering iron with sufficient power (approximately 60W - 80W) and a 2 – 3mm tip. A damp cloth can be used to cool the IC on the top surface.

Simple and cheap SMD soldering irons have thin needle like tips that are easily bent making them difficult to use. A better choice is a soldering station with a good SMD soldering tip.

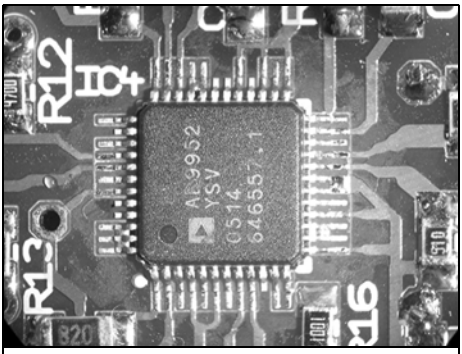


Fig 17: Close up view of the DDS IC.

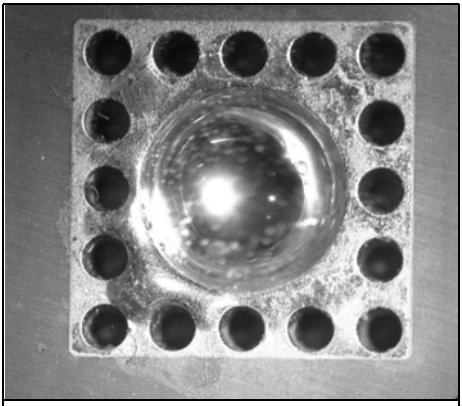


Fig 18: View of the holes used to feed solder to the earth surface in the IC.

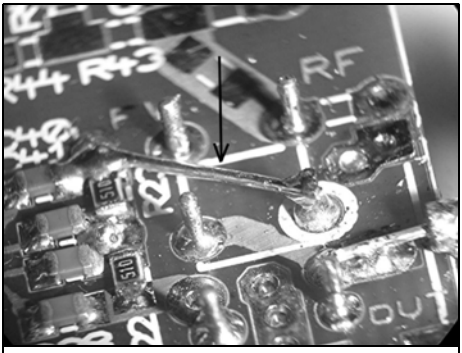


Fig 19: Picture of the phase line.

3.1. Phase line

In the original version of the analyser an external phase line was used to null out the test lead. In the current version an approximately 11mm long piece of jumper wire is soldered on the SMD side of the PCB from Pin 3 of the directional coupler to the input of the AD8203 at C41 as shown in Fig 19. This is suitable for an SMA output connector with a short piece of cable that results in an overall length of approximately 22mm. This also corresponds to an N type socket with a small flange used with a similar length of cable.

This should result is small phase differences at the highest measuring frequency without the software correction. The hardware is adjusted so that no phase shift occurs up to the output connector

3.2. Housing

The analyser was built into a 200mm x 120mm x 57mm case from BOPLA. The prepared case and the front panel are shown in Fig 20.

4.

Measuring examples

Approximately a 72cm length of coaxial cable with 100Ω terminating resistor was used as measuring example. The measurement of the resistor with the real and imaginary part (jX) is shown in Fig 21. The real part [Re], phase and adjustment are shown in Fig 22. These measurements were compared with the same cable tested using an HP (HP8753D) vector network analyser The

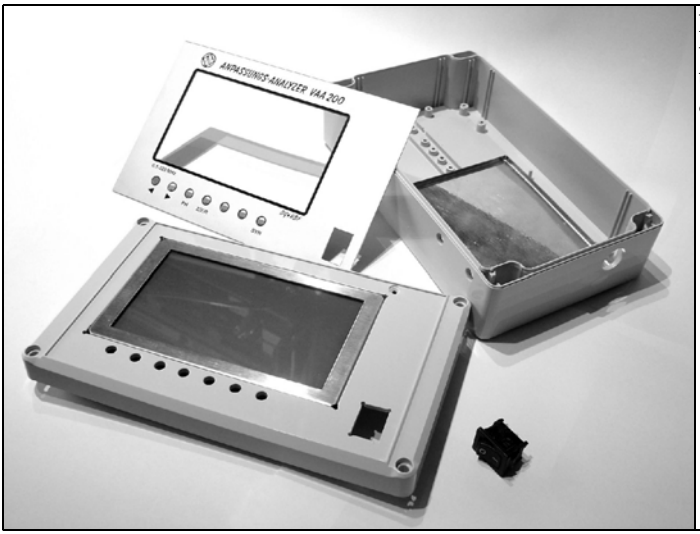


Fig 20: Picture of the plastic case used for the vector analyser.

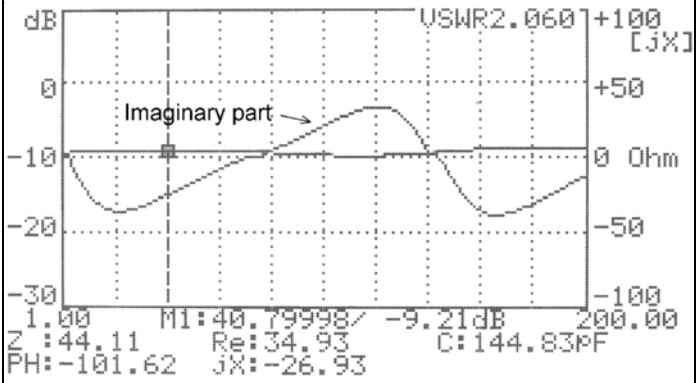


Fig 21:

Marker: 40.79998MHz, Phase: -101.62°

Imaginary part: jX = -26.93Ω, Adjustment: -9.21dB (VSWR: 2.060)

Conversion: 144.83pF

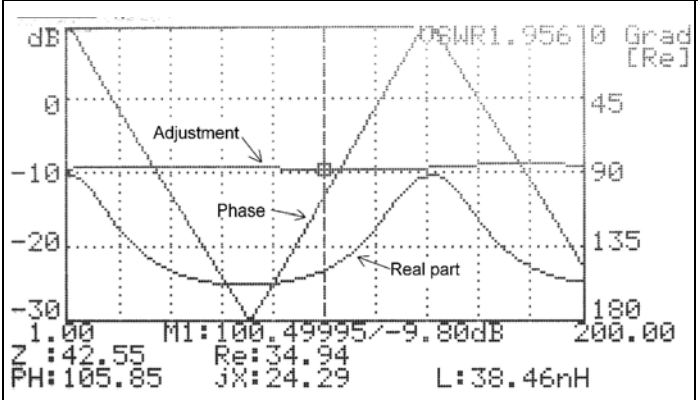


Fig 22:

Marker: 100.4995MHz, Phase +105.85°

Re: 34.94Ω, Adjustment: -9.80dB (VSWR: 1.956)

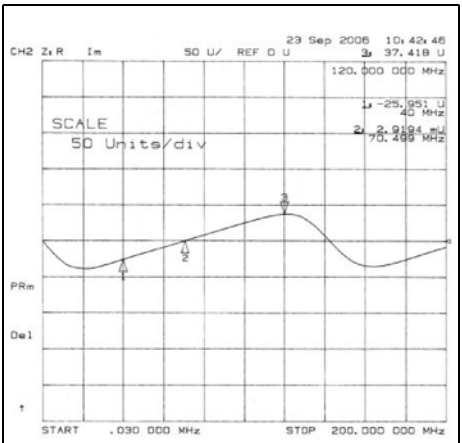


Fig 23: Real part measurement made on an HP VNA.

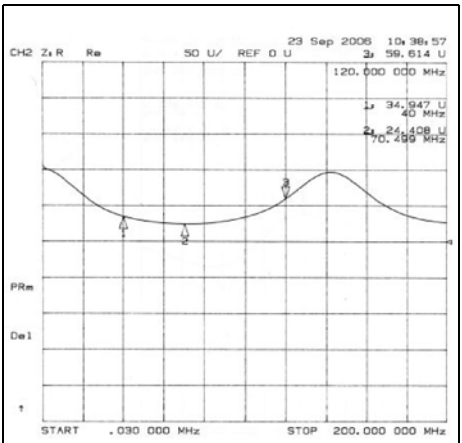


Fig 24: Imaginary part measurement made on an HP VNA.

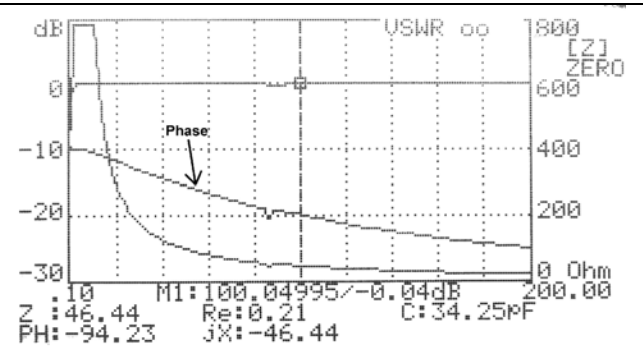


Fig 25: Measurement of cable plus 33pF capacitor on the 800Ω range.

Marker: 100.49995MHz, Phase: -94.23°

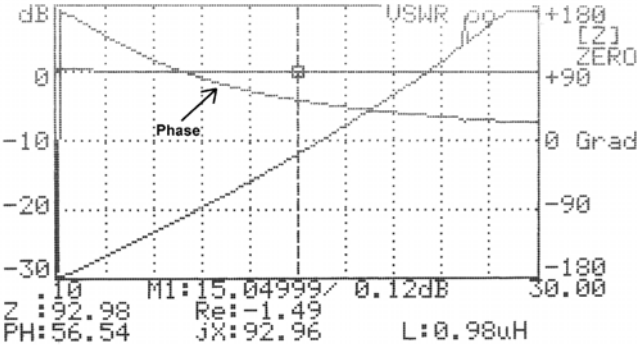


Fig 26: Measurement of cable plus 1µH inductor on the +180°/0°/-180° scale.

Marker: 15.04999MHz, Phase: +54.54°

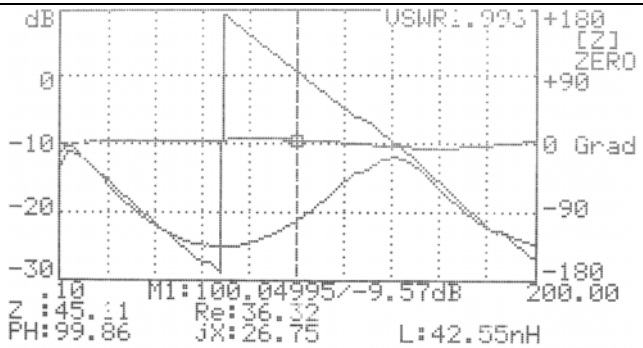


Fig 27: Representation of phase using the ZERO function (+180° to -180°)

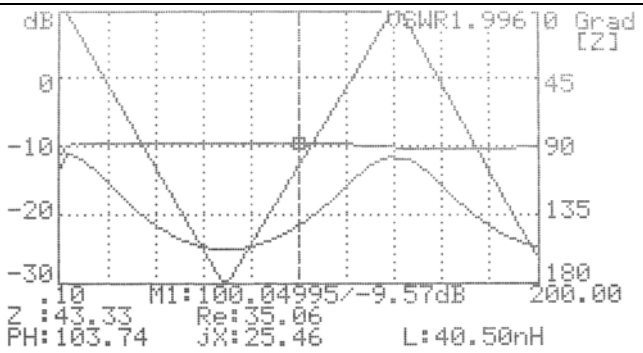


Fig 28: Representation of phase using the ZERO function (0 to 180°)

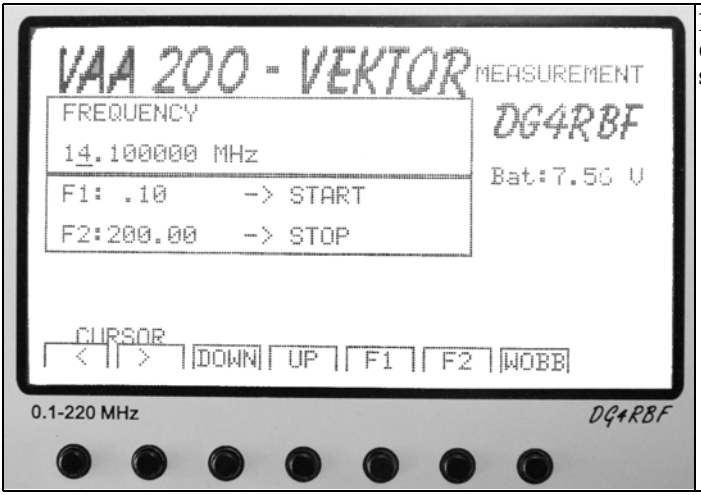


Fig 29: Setup display for the signal generator.

results shown in Figs 23 and 24 show very good agreement. Two more examples are shown in Fig 25 and Fig 26 for a 33pf capacitor and a 1µH coil attached to the cable.

4.1 Display options

Pressing the phase key [pH] toggles the phase measurement on and off. On the left a dB scale is displayed and on the right a scale in degrees or in ohms is displayed depending on whether the phase display is switched on or off.

Key 6 [ohms] switches on a scale from 200Ω to 800Ω even if the phase display is switched on. This gives a more flexible display.

A marker can be moved using the cursor keys, this displays the appropriate data at the selected point.

The nulling option [ZERO] applies the phase adjustment and displays the measured phase from +180° to -180°. Without the [ZERO] function the phase is from 0 to 180° where the upper curve is the "0" (Fig 27 and Fig 28).

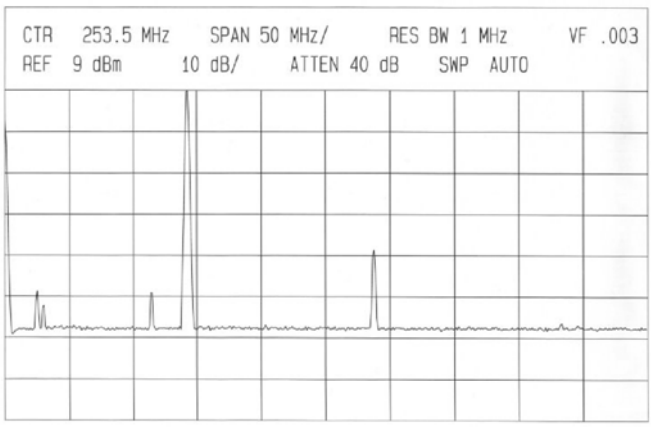


Fig 30: Output spectrum of the signal generator at 145MHz.

Fig 31: Test aids.

5.
Simple signal generator

The VAA 200 can also be used as a simple signal generator. It can generate a frequency from 0.1MHz to 220MHz with a resolution of 1Hz. The signal level drops at 200MHz (max. 210MHz) because of the filter used.

The synthesizer is programmed with software keys. The start and stop frequency for the sweep function (Wobbler) is programmed using [F1] and [F2]. They function like the memory keys on a car radio pressing a key stops the function an accepts the frequency from the input field. This can be seen in Fig 29. The output spectrum measured with an HP 8569A spectrum analyser at 145MHz is shown in Fig 30.

6.
Operation

The analyser is controlled with 7 keys:

***Key 1 and* 2:** [Cursor] Shift the measuring cursor.

***Key* 3** [pH]: Toggles the phase measurement display on and off.

***Key* 4** [Z/X/R]: Toggles between the different measuring curves (impedance, imaginary part and real part)

***Key* 5** [ZERO]: A short press toggles the ZERO function on and off. A longer press (approximately 3 seconds), measures and stores the current phase value used to adjust measurements when the [ZERO] function is switched on.

Key 6 [ohms]: Switches the scaling from 200Ω to 800Ω.

***Key* 7** [SYN]: A short press switches to signal generator mode. A longer pressed (approximately 3 seconds), switches the backlight on and off switched on and/or off.

7.
Set UP functions

There are different set UP functions actuated by holding down an appropriate key when the analyser is switched on.

RESET: If Key 1 is pressed when switching on the analyser is reset.

Frequency Trim: If Key 2 is pressed when switching on a menu is displayed

Table 1: Measured RF output.

Frequency (MHz)	Output (dBm)
0.1.	+7.1
0.2	+10.2
1.0	+11.3
50.0	+11.3
100.0	+10.5
150.0	+8.3
200.0	+5.9
210.0	+3.4
220.0	-5.3

to allow fine adjustment of the clock frequency.

Automatic 0dB calibration: If Key 7 is pressed when switching on the automatic 0dB calibration is carried out and the value is stored.

Manual 0dB alignment: If Key 3 or key 4 are pressed when switching on the corrected 0dB value can be changed up or down.

After normal switch on of the analyser will be in S11 swept frequency measurement mode. The start and stop frequency use are the values stored from signal generator mode.

8.

Testing

The measured RF output is shown in Table 1.

The analyser can be tested when it is complete using a few simple aids. These are made by soldering the following components onto SMA sockets:

- A 1µH coil, a 33pF capacitor, a 100Ω resistor, two 51Ω resistors in parallel to give 25.5Ω and one open circuit socket. This socket is used for the nulling function to eliminate the phase shift of the socket before any measurements are made.

Table 2: Display pin connections.

Display pin	Function	K8 pin
1	GND	1
2	+5V	2
3	NC	3
4	C/C	4
5	/RD	5
6	/WR	6
7 - 14	DB0 - DB7	7 - 14
15	/CE	15
16	/RST	16
17	NC	17
18	MD2 (GND)	18
19	FS1 (+5V)	19
20	NC	20

The test aids are shown in Fig 31. Using the prototype the values shown in Table 3 were measured for the test aids.

9.

Parts list

Active components

D1	BAT42
T1	BC548B
T2	IRF9520
IC1	LM317
IC2	7805

Table 3: Measured values for the test aids.

Device under test	Measured value	Freq. MHz
R 100Ω	Re: 102.1Ω	100
R 25.5Ω	Re: 25.4Ω	100
33pF capacitor	34.25pF	100
1µH coil	0.98µH	15

IC3	GALI51
IC4	AD9952
IC5	ATMEGA32 with software
IC6	AD8302
IC9	PICF8574P
D-COP1	PDC-20-3BD Mini Circuits
TR1	TC1-1T Mini Circuits
Q1	22.1184MHz
Q2	Osc. 36.0 MHz

Resistors

R36	5Ω
R8, 21	10Ω
R35	47Ω
R1, 2, 22, 23, 26, 27	51Ω
R3	83Ω
R18, 32, 33	100Ω
R7	120Ω
R34	220Ω
R6	240Ω
R12, 13, 14	470Ω
R9, 10, 11	680Ω
R16	1kΩ
R19, 20	2.2kΩ
R4	3.3kΩ
R15	3.9kΩ
R17, 24, 30, 31, 39, 41	10kΩ
R38	33kΩ
R40, 42	100kΩ

Capacitors

C1, 8	3.3pF
C2, 3 - 7	22pF
C10, 20	330pF
C37, 44, 45	1nF
C58	4.7nF
C38 - 43	12nF
C31, 32	27nF
C19	47nF
C9, 11, 17, 18, 22, 25 - 28, 30, 36, 56, 57, 59, 60	100nF
C23	1000nF
C14, 35	1µF
C21, 29	3.3µF
C12, 15, 16, 33, 34	10µF
C13, 24	22µF

Inductors

L1, 7	33nH
L8	47µH
L2, 6	68nH
L3 - 5	82nH

Hardware

K3 5	K1X1
K12, 14 - 18	K1X1
K10, 13	K1X2
K6	K1X4
K8	K1X20
SW1 - 8	Push button, Conrad 705349/705115
BU1	SMA or small flange N Type

10.

Latest updates

The author's homepage shows the current information: www.dg4rbf.de. The author can supply a list of current sources of supply for special parts by sending an email to: Info@dg4rbf.de

11.

References

Data sheets:

Analog Devices: AD8302 - http://www.analog.com/en/prod/0%2C2877%2CAD8302%2C00.html

Mini Circuits: PDC 20-3BD - http://www.minicircuits.com/cgi-bin/modelsearch?search_type=info&model=PDC-20-3BD

Note: If there is sufficient demand finished milled and engraved front panels can be manufactured. The front panel design, as well as an auxiliary diagram for the recess in the plastic housing can be downloaded as pdf files from the from author's homepage (www.dg4rbf.de).

Henning Christof Weddig, DK5LV

An IF amplifier with “dB linear” gain control

In Superhet receivers an IF amplifier is used to process amplitude-modulated signals (SSB, CW…). The gain of this IF amplifier has a gain control so that the output signal remains almost independent of the input signal level. If the gain control has a logarithmic relationship to the input level, this can be used to directly display the signal strength on a “dB-linear” signal strength meter. The following article describes such an IF amplifier.

1.

Introduction

In a Superhet receiver an IF amplifier, whose gain is controlled by a gain control in such that the output signal remains independent of the amplitude of the input signal, is needed to process amplitude-modulated signals e.g. in the SSB and CW etc.

The gain control is often used to display the received signal level. Because of the large signal differences that are encountered, a logarithmic relationship between input levels and the gain control is desirable, then the signal strength meter is not an estimate!

A versatile IF amplifier is described in [1], it is a modular system with: switchable crystal filters, demodulators for SSB/CW, FM and AM and a gain control generated from the IF amplifier. In paragraph c) of the article the gain control is described but there is no mention of dB linear control!

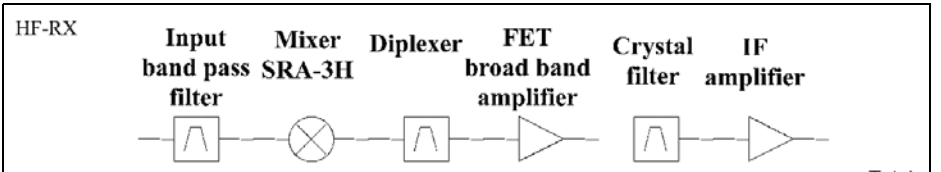
There are several ICs on the market with dB linear gain controls from Analog Devices, National Semiconductors and Texas Instruments. With these ICs linear IF amplifiers for 9 or 10.7MHz can be built which exhibit a true dB linear control curve

An IF amplifier using an AD600 from Analog Devices was described in [2] and in a project called CDG2000 described in [3]. Different versions of an IF amplifier using an AD603 from Analog Devices appeared in [4] and [5]. The AD603 is also used in the “Pic-A Star” project [6] and appeared in a series of articles about IF amplifiers [7].

2.

Background for the specification of the IF amplifier

In order to provide the specifications of the IF amplifier a level plan of a receiver for short wave use and one for VHF use were produced.



							Total
NF (dB)	2.00	6.00	0.20	2.00	3.00	6.00	14.58
Gain (dB)	-2.00	-6.00	-0.20	4.00	-3.00	80.00	72.80
OIP3 (dBm)	100.00	23.00	50.00	30.00	35.00	100.00	97.83
OP1dB (dBm)	100.00	8.00	50.00	21.00	25.00	100.00	88.80
IP3+ (dBm)	0.00	1.27	0.00	0.56	0.08	4.05	
NF+ (dB)		0.78		0.63		3.41	
Po (dBm)	-109.00	-115.00	-115.20	-111.20	-114.20	-34.20	

Input Pwr (dBm)	-107.00	System Temp (K)		290.00		
Modulation: Custom						
System BW (MHz)	0.0024	MDS (dBm)		-125.59	Input IP3 (dBm)	25.03
S/N (dB, Actual)	18.59	S/N (dB, Req'd)		20.00	Output IP3 (dBm)	97.83
Srce Temp (K)	290.00	Sens. Loss (dB)		0.00	OIM3 (dBm)	-298.26
Te Eff. (K)	8042.85	Sensitivity (dBm)		-105.59	ORR3 (dB)	264.06
SFDR3 (dB)	100.41	G/T (dB/K)		-29.21	IRR3 (dB)	88.02

Fig 1: Level plan for a short wave receiver, bandwidth 2.4kHz.

2.1 System simulation of a short wave receiver

The data for a level plan of a short wave receiver (single superhet) was computed with the system simulation program "Syscalc" [8] is shown in Fig 1. The system bandwidth was chosen as 2.4kHz (SSB use). The noise figure of the individual stages, their output intercept point and 1dB compression point are calculated. The input of the IF amplifier has a band filters with a +100dB (unrealistic) intercept point. The intercept point of input band pass filters is difficult to measure. The intercept point of the IF amplifier is unimportant for signals which lie outside of the range of the crystal filter, since these signals do not reach the IF amplifier, therefore the +100dBm is acceptable.

The noise figure of passive devices corresponds to the their insertion loss.

The gain of the individual stages before the crystal filter, that defines the bandwidth, were selected as low as possible to prevent any overloads.

From the simulation the receiver has a total noise figure of 14.58dB. An antenna signal of -107dBm = 1µV gives a signal/(Signal + Noise) ratio of 17.62dB. A signal of -107dBm at the antenna input gives a signal of –114dBm at the input of the IF amplifier. The noise figure of the completed receiver is acceptable because of the high external noise from the antenna, see also [9] and [10]. Because of the low gain of the stages before the IF amplifier it's noise figure still influences the total noise figure. The IF amplifier therefore should have a low noise figure as possible.

2.2 System simulation of a VHF receiver

Fig. 2 shows the level plan of a VHF receiver. Because the external noise coming from the antenna is very much lower in the VHF and UHF range than at HF

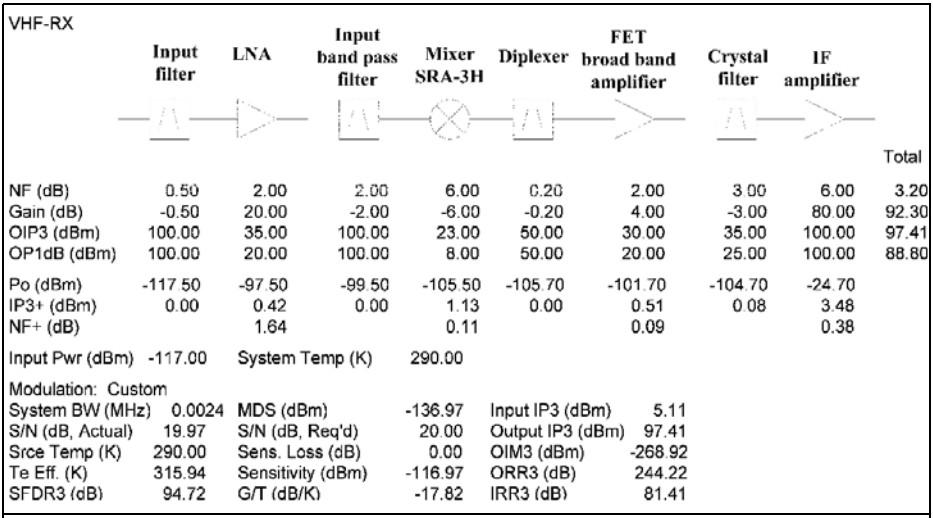


Fig 2: Level plan for a VHF receiver, bandwidth 2.4kHz.

frequencies (approximately 3dB), the receiver sensitivity is increased by an LNA (LNA = low noise amplifier) with a low attenuation filter before the LNA. The LNA has a gain of 20dB. The stages after the LNA are the same as in the short wave receiver.

Using this data a noise figure of the complete receiver is 3.2dB. With an input signal of -117dBm = 0.3µV gives a SINAD of 20dB. The level at the input of the IF amplifier is -104.7dBm which is 10dB more than the IF amplifier of the short wave receiver.

2.3 The signal strength meter problem

2.3.1 Signal strength meter display in the short wave range

At HF the signal level S9 is specified as a voltage at the antenna input of a receiver of 50µV (-73dBm). Each S point is a difference of 6dB. The input voltages for S0 to S9 are shown in Table 1. The signal strength meter reading S0 is equivalent to an input signal of -127dBm, the relationship [signal to (signal + noise) ratio] for SSB is –3dB. Thus the noise floor is higher than the background noise of the receiver! An input signal of -109dBm corresponds to S3. This value is marked in bold on Table 1. With this signal the SINAD is 17dB. At HF the usable sensitivity of the receiver is limited by the external noise at the antenna, see [9] page 168 and [10]. At a frequency of 2MHz (above the 160m band) the external noise has a value of 65dB (electrical noise) and at 30MHz (above the 10m band) it is 25dB (atmospheric noise during the day). At room temperature the thermal noise power is -174dBm

Table 1: Input voltages for S meter values for the short wave range.

S	0	1	2	**3**	4	5	6	7	8	9
V_{in} (µV)	0.1	0.195	0.38	**0.78**	1.56	3.125	6.25	12.5	25	50
P_{in} (dBm)	-127	-121	-115	**-109**	-103	-97	-91	-85	-79	-73

Table 2: Input voltages for S meter values for the VHF range.

S	0	1	2	3	4	5	6	7	8	9
V_{in} (µV)	0.028	0.05	0.079	0.125	0.285	0.5	0.79	1.25	2.85	5
P_{in} (dBm)	-138	-133	-128	-123	-118	-113	-108	-103	-98	-93

measured in a 1Hz bandwidth. For SSB bandwidth (2.4kHz) the noise power rises by 10 log(2400/1) = 34dB which has to be added, resulting in and overall noise power of -140dBm.

For the previous mention frequencies of 2MHz and 30MHz the noise power at the input of the receiver, assuming 50Ω pure resistive antenna input impedance, is:

160m band: P_{noise} = -174dBm + 34dB + 65dB = -75dBm = 39µV. With a good antenna the signal strength meter would indicate an input signal due to the noise of nearly S9!

10m band: P_{noise} = -174dBm + 34dB + 40dB = -115dBm = 0.39µV. At 30MHz the noise is less by about 40dB at -115dBm = 0.39µV, the signal strength meter indicates approximately S2.

2.3.2 Signal strength meter display in the VHF range

At frequencies above 100MHz the external noise drops to approximately 2dB. A low noise amplifier in front of the mixer is meaningful to reduce the total noise figure of the complete receiver by approximately 2 to 3dB. Thus the sensitivity of the receiver described above is increases by 10dB to approximately 3dB. At VHF and UHF the input voltage for S9 is defined as 5µV (-93dBm).

The difference between S points in the VHF range used to be defined as 5dB. At the IARU region 1 conference in Miskolc Tapolca (1978) the difference between S points for frequencies above 144MHz was suggested as 6dB. The IARU region 1 VHF UHF/SHF committee did not accept this suggestion but the reference value for S9 was set as -93dBm from a signal generator (available signal power) at the antenna input of the receiver. With these values the voltages for S0 to S9 are shown in Table 2. For the VHF range the level for S9 is around 20dB lower, the change for each S point from 5dB to 6dB is meaningfully, S0 is around 9dB lower. An input signal of -117dBm is indicated as S4. Note: The noise floor of a receiver (with F = 3dB) and SSB bandwidth (B = 2.4kHz) is -137.2dBm. For CW operation the range can be substantially lowered, with 500Hz bandwidth 6.8dB are gained and with 250Hz approximately 10dB are gained, that is two S points. Speech can be copied with a (S+N)/N from 10dB, better 20dB, CW can be copied with substantially lower values, if the listener is properly trained.

2.3.3 Choice of the start point of the AGC

If the control voltage V_{Agc} is related to the amplitude of the RF signal at the antenna input of the receiver by an accurate logarithmic function then a signal strength meter connected to the control voltage is an accurate signal strength meter. Using the definitions, S0 = -127dBm, with a bandwidth of 2.4kHz the background noise of the receiver is equal to S0. This means that the noise at the output of the receiver is the same as the information. The background noise would be lower than the signal in CW mode because of the smaller bandwidth.

Since the range of control of the IF amplifier is limited, it is sensible to set the point where the control starts at a

signal-to-noise ratio of 20dB (bandwidth = 2.4 kHz; for SSB). The starting point for gain control of the IF amplifier in a short wave receiver would be an antenna input level of -107dBm and a VHF receiver would be -117dBm. Thus the signal strength meter of a short wave receiver would not indicate correct values below S3, and for a VHF receiver below S4.

3.

Specifications for the IF amplifier

a) Noise figure of the IF amplifier

From the data of the input level for the operating sensitivity of the short wave receiver with an antenna signal of -107dBm, for 20dB (S+N) /N on an SSB bandwidth (2.4kHz) and ambient temperature (297ºK), the input level of the IF amplifier from Table 1 is -114dBm. Using this data the noise figure of the IF amplifier can be calculated:

Thermal noise power in a 1Hz:
= -174 dBm

Noise power in SSB bandwidth: = 10 * log 2400Hz/1Hz = 33.8dB

Noise floor in SSB bandwidth:
= -174dBm + 33.8dBm = -140.20dBm

Input signal for 20dB SINAD:
-114dBm

Difference input signal - background noise: 26dB

If theoretically the IF amplifier had no noise figure, a signal of –120dBm would be sufficient to obtain the desired signal-to-noise ratio of 20dB; the difference to -114dBm gives maximum noise figure of the IF amplifier of 6dB. Since the input level is higher for the IF amplifier in the VHF receiver by around 10dB, the noise figure of the IF amplifier could be higher i.e. 16dB.

b) Gain of the IF amplifier

The gain required for the IF amplifier can be determined from the nominal input level of the demodulator. If an SA612 IC is used as a product detector its input level should not exceed -40dBm ($2.24mV_{eff}$ at 50Ω), see [11]. Compression starts with around 10dB higher input level, the intermodulation products (audio signals!) are then only approximately 35dB down.

The good old MC1496 is better, see [12]. Despite it's age it is still available and favoured as a product detector. A meaningful input level for this component is -30dBm.

Under these conditions the IF amplifier must raise the input signal of -114dBm by around 84dB to -30dBm.

c) Overload reserve

Since the gain control does not act instantly if a level RF step occurs, the amplifier must be capable of these overload conditions and must recover quickly. An overload reserve from 20 to 30dB is to be aimed at, i.e. the amplifier must be able to handle outputs from -10 to 0dBm without degradation.

d) Intermodulation

In order that the signal is not badly affected by distortion products of the IF amplifier, the third order intermodulation products should be less than 40dB, relative to the carrier signals over the entire range of control.

e) Start point of the gain control

The start point of the control range

should be adjustable with a trimmer, e.g. 2V, and the gain control range should be larger than 80dB. The slope of the gain vs. control voltage should be true logarithmic in order to have a true "linear" dB relationship.

f) AGC slope

For a simple signal strength meter the AGC slope should be 100mV/10dB.

g) Isolated outputs

The IF amplifier should have one output for the demodulator and one output for the AGC. In SSB/CW mode the BFO signal is fed to the product detector. This signal must not get fed into the AGC circuit because it would produce an unwanted control signal. Therefore both outputs of the IF amplifier should be isolated by at least 20dB. This problem does not exist if the gain control is based on the demodulated audio signal. The technical literature shows that the control speed of an audio based gain control is slower than rectification of the RF signal. Therefore the AGC circuit using a gain control derived from the IF signals is preferred.

h) System impedance

The input and output impedance should be 50Ω which makes simple interconnection possible with other building blocks. The VSWR should not be more than 1.2 (20dB return loss).

3.1. Requirement list

The specifications described above are summarized in the following list.

- Noise figure: < 6dB
- Gain: 74dB (84dB)
- Gain control: > 80dB
- Overload up to output levels: -10 to +0dBm
- Internal Intermodulation over the entire control range of control: >40dB
- Control rate: 100mV/10dB
- Control range start: V_R = 2V
- Linear dB control range
- Input and output impedance: 50Ω, Return loss < -20dB
- Two decoupled outputs (demodulator and AGC), decoupling of the outputs >20dB

4.

Description of the AD603

The data sheet for the AD603 from Analog Devices shows the following characteristics:

- Input impedance 100Ω
- Noise figure 8.8dB (f = 10MHz; maximum gain; R_s = 10Ω)
- 1dB compression -11dBm (f = 10MHz; maximum gain; R_s = 10Ω)
- Distortion (total harmonic distortion) -60dBc (f = 40MHz; V_{out} = $1V_{eff}$)

The AD603 contains a variable attenuator and an amplifier. The attenuator is a multi level R-2R lader network. Each stage of the R-2R network will attenuate the input signal around 6.02dB, intermediate values are achieved by means of an “interpolation circuit”. The output of the attenuator is connected to the input of a low noise amplifier. The inputs of the attenuator are fed out to the ports V_{INP} and COMM. The maximum input voltage (with a supply voltage of ±5 V) is $1V_{eff}$ compared to $1.4V_{ss}$. Input voltages to $2V_{eff}$ do not affect the data concerning

distortion and possible control. The input impedance is laser trimmed during the manufacture of the IC to a nominal 100Ω ± 3%.

The gain can be set by connecting an external resistor between the ports V_{OUT} and FDBK this gives 31dB (3dB range 90MHz) with V_{OUT} and FDBK connected, 41dB with V_{OUT} and FDBK connected with an external 2.48kΩ resistor and 51dB (3dB range 9MHz) with V_{OUT} and FDBK not connected.

Dual supply voltage should be between ±4.75 to ±5.25V, the maximum voltage is ±7.5V. It is possible to use a single supply voltage from 10V to 15V.

The amplifier does not need overload protection because it uses an input attenuator that always provides a smaller input signal to the amplifier. The output of the amplifier can feed loads of 100Ω, with low distortion. For a load of 500Ω in parallel with 5pF and a sinusoidal output voltage of $\pm 1V_{pp}$ at a frequency of 10MHz the distortions is 60dB down on the signal. The maximum output voltage is specified as $\pm 2.5\ V_{pp}$ with a load of 500Ω or ±1V with a load 100Ω. The inputs for gain control; V_{POS} and V_{NEG} are differential opposite to the port COMM. The control voltage is -500mV to +500mV, i.e. 1V.

The gain can be computed with the following formulas as a function of the wiring of the two pins FDBK and V_{OUT}:

$G = 40V_G + 10$ (G = -10… + 31dB): V_{OUT} and FDBK connected

$G = 40V_G + 20$ (G = 0… + 40dB): V_{OUT} and FDBK connected by 2.49kΩ

$G = 40V_G + 30$ (G = +10… + 50 dB): V_{OUT} and FDBK open circuit

The voltage V_G is in volts. If the voltage between V_{POS} and V_{NEG} is 0V the attenuator is in the centre position, thus the input signal is attenuated by around 21.07dB. If a positive voltage is applied to the "G_{POS}" input with the opposite voltage applied to the "G_{NEG}" input the gain is reduced. If these are revered the gain is increased. The gain is reached with the control voltage +500mVs (V_{POS} - V_{NEG}), the minimum gain with -500mVs. If these limits are exceeded, the gain will be -11.07dB (-42.14dB +31.07dB) or 31.07dB (0dB + 31.07dB). The scaling factor is 40dB/V or 25mV/dB. The control voltage may move within the common mode range from –1.2V to +2V relative to a supply voltage of 5V. The data sheet indicates that the control voltage may not fall too much below the lower limit. Experiments showed that in this case the gain rises again. Thus there is no relationship between control voltage and gain under these circumstances.

4.1. Cascading of two AD603s

The maximum gain (31dB) and the range of control of an IC (42dB) is not sufficient for an IF amplifier, that is why two ICs are cascaded. Thus a maximum gain of 62dB as well as a minimum gain of –22dB is achieved if the pins V_{OUT} and FDBK are connected. The upper cutoff frequency is reduced from 90MHz to approximately 70MHz. Other configurations are possible by the external wiring but degrade the upper cutoff frequency (6MHz with G = 22 to 102dB).

To avoid DC offsets the two amplifiers must be AC coupled. In order to keep a high signal/signal-to-noise ratio the second amplifier has it's gain reduced while the first amplifier maintains it's maximum gain. The gain reduction only takes place if the range of control of the second amplifier is exceeded. Naturally the first amplifier must be able to bear the maximum input level that is possible as shown in the level plan of Fig. 1. This kind of the gain control is called sequential mode in the data sheet [13]. The G_{NEG} inputs of both amplifiers are set to a defined DC voltage, (V_{01} = +0.473V for the first amplifier, V_{02} = +0.473V for the second

amplifier). The G_{POS} inputs of both amplifiers are connected together.

For a control voltage of 0V the difference of the G_{NEG} voltages is G_{POS} = -473mVs, the gain of amplifier A1 is:

G (dB) = 40 (-0.473V) + 10 = (-18.92 + 10) dB = -8.92dB

Because V_{02} is 1.526V which is higher than the maximum (1V) but is still within the permissible common mode range, the gain of the second amplifier is thus -42.14dB + 31.07dB = -11.07dB. The total attenuation amounts to –8.92dB + (-11.07dB) = -20dB.

If the control voltage V_G is +1.0V, V_{G1} = 1V - 0.473V = +0.526V, thus the first amplifier is adjusted to its highest gain = +31.07dB. V_{G2} is 1.0V - 1.526V = 0.526V, the second amplifier attenuates the signal by approximately –11.07dB. The overall gain amounts to 31.07dB - 11.07dB = 20.0dB.

If the control voltage V_G is +2.0V, V_{G1} = 2V - 0.473V = +1.526V, thus the first amplifier is adjusted to its highest gain = +31.07dB. V_{G2} is 2.0V - 1.526V = 0.474 V, the second amplifier amplifies the signal by approximately +28.93dB. The overall gain amounts to 31.07dB + 28.93dB = 60.0dB.

4.2. Oscillation tendencies

In the data sheet for the AD603 [13] the amplitude and phase response are shown in *Fig 6* as function of the frequency. It is apparent that the gain rises at high frequencies; the maximum is reached at approximately 60MHz. At this frequency a rapid phase change from -180° to + 180° takes place. This behaviour is an indication of possible oscillations. With the first tests using two AD603s connected by a capacitor as in *Fig 47* of [2], an oscillation could be observed in this frequency range with maximum gain. If a two pole band pass filter for the wanted IF is inserted between the two amplifiers, the oscillation can be suppressed.

5.
IF amplifier circuit description

The circuit diagram of the IF amplifier is shown in Figs 3 - Fig 5.

The IF amplifier comprises of two AD603 ICs and two dual gate MOSFET buffer amplifiers, these increase the overall gain to the 80dB, indicated in the block diagram, and decouple the product detector at the input of the AGC circuit where the high frequency signal is used to produce the control voltage.

5.1. Input stage with FET

The data sheet for the AD603 gives the noise figure of 8.8dB for a source resistance of 10Ω, unfortunately there is no information for higher source resistances. This noise figure is not acceptable for use in a short wave receiver. Therefore two J310 junction FETs are used in common gate at the input of the amplifier.

With a transconductance of 10mmhos (drain current = 10mA) for each transistor amounts to the input impedance approaching 1/transconductance = 1/20mmhos = 50Ω. The gain of this stage is approximately R_{Last}/R_{in} = 100/50 = 2 = 6dB, a power gain of 4. The noise figure for this stage is given as F = 2 (3dB) with the noise figure of the AD603 at 7.78 (8.8dB) results in a total noise figure of:

$$F_{ges} = F_1 + \frac{F_2 - 1}{G1} = 2 + \frac{7.58 - 1}{4} = 3.645 = 5.61dB$$

This fulfils the product specification.

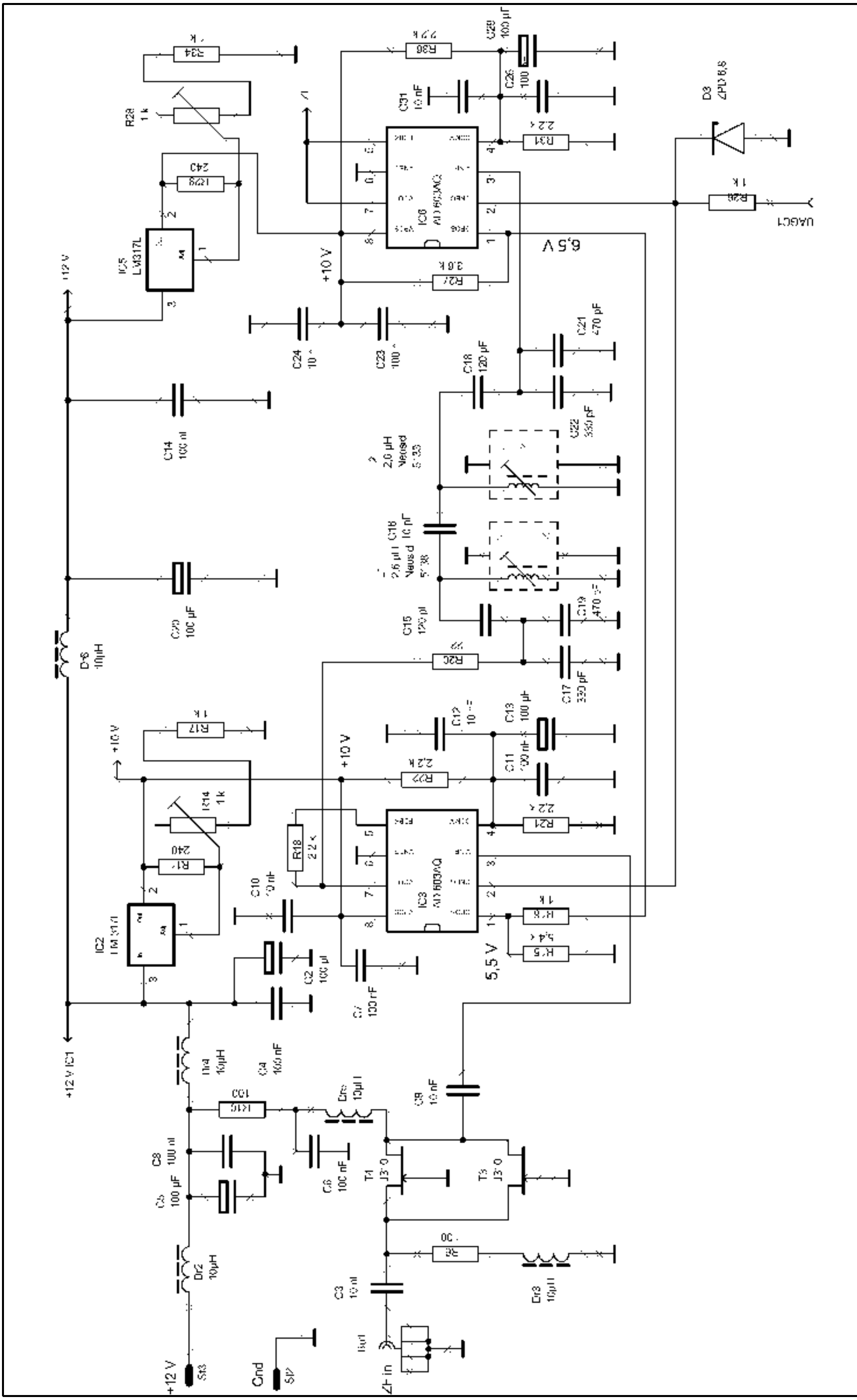


Fig 3: Circuit diagram of the two AD803 ICs in the IF amplifier.

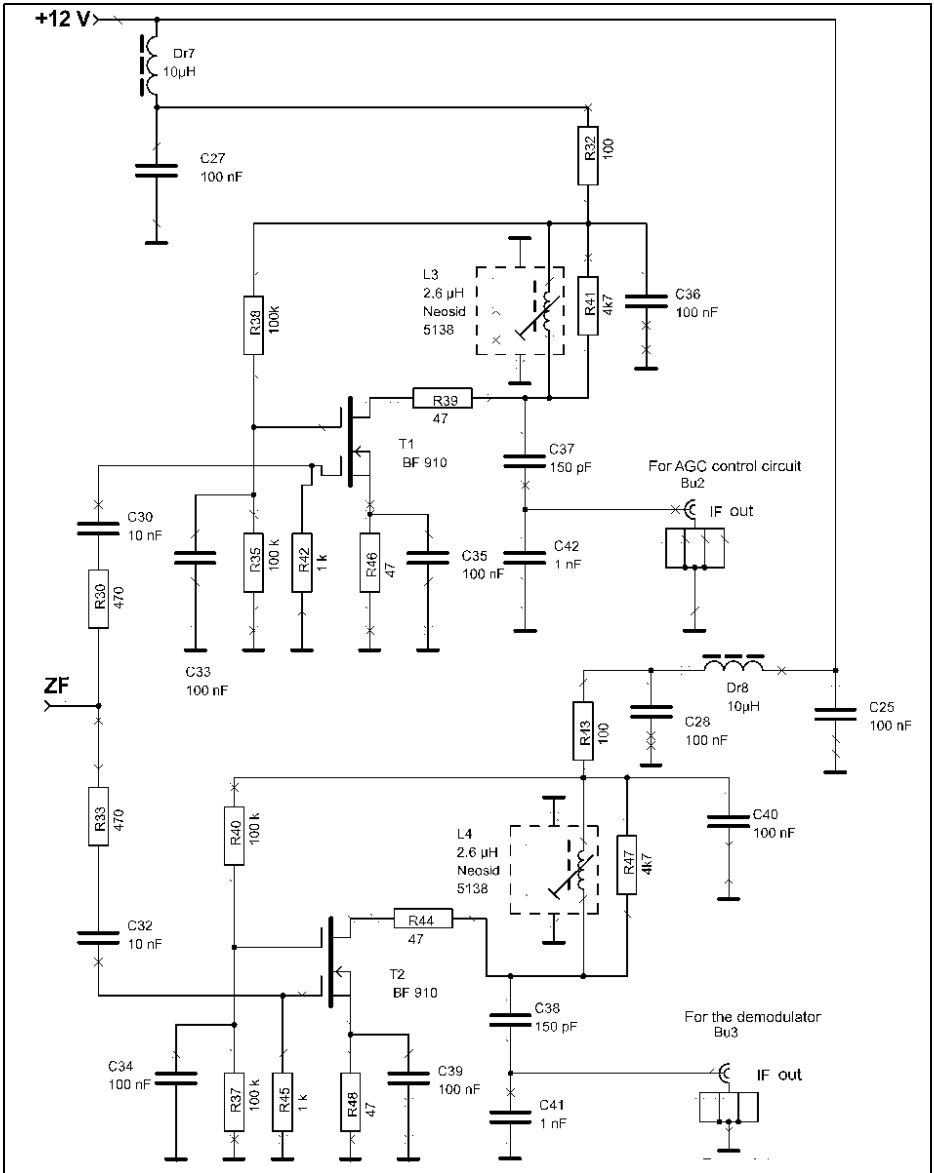


Fig 4: Circuit diagram of the output buffer amplifier of the IF amplifier.

Since the FETs vary, two transistors are selected with the same gate source voltage at a drain current of 10mA if possible. The drain current can be set using resistor R6.

5.2. IF amplifier

Because of the overall gain two AD603 ICs are required, IC3 and IC6. They are operated with a single supply voltage of

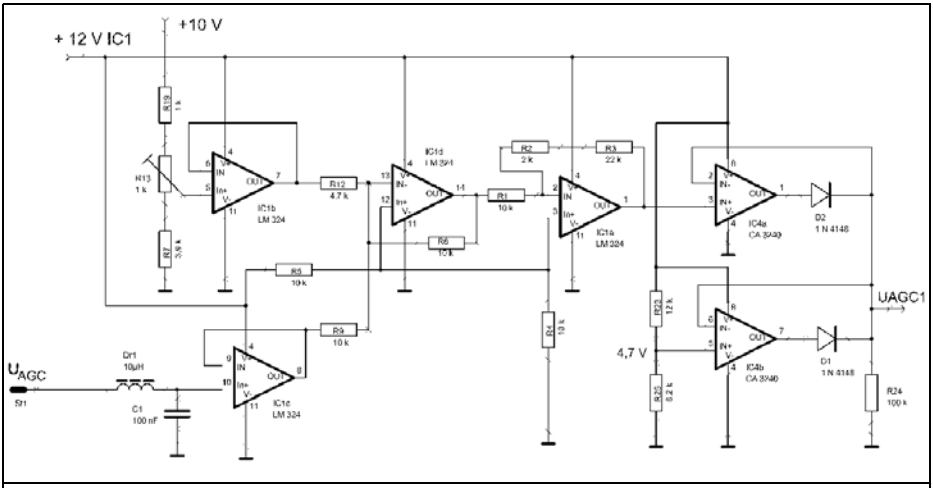


Fig 5: AGC control voltage amplifier for the IF amplifier. AGC range 2 to 3V for gain change G = 84dB, maximum gain at V_{AGC} = 2V.

10V set with the adjustable voltage regulators IC2 and IC5 from the 12V supply voltage and fed to pin 8 (V_{POS}) of IC3 and IC6. Pin 6 (V_{NEG}) of IC3 and IC6 are connected to ground. Both Pin 8s are decoupled to ground with 100nF and 10nF ceramic capacitors.

The voltage of the COMM pin of the two ICs is set to half supply voltage with the resistors R21, R22, R31 and R36. This connection needs a low impedance path to ground achieved with 100µF tantalum capacitors for low frequencies plus 100nF and 10nF ceramic capacitors for higher frequencies.

The control input, G_{NEG}, of both amplifiers are connected together, and the G_{POS} inputs are connected with the resistor chain R15, R16, R27. In the prototype resistor values from the E12 series were used, (R27 = 3.3kΩ, R15 = 5.6kΩ) were used, giving a voltage of 6.7V on pin 1 of IC6 and 4.7V on pin 1 of IC3. With these values the maximum voltage is 100mV higher than indicated in the data sheet over the entire temperature range but it does not exceed the absolute limits. The offset voltage between the G_{POS} inputs of the amplifiers IC3 and IC6 is 1.05V giving (42.14dB * 25mV/dB). The measured offset was only 1V, according to data sheet this deviation should not be critical. The gain increases with increasing control voltage at the G_{POS} inputs. If necessary resistors from the E96 series (with 1% accuracy) can be used: R27 = 3.48kΩ, R16 = 1.05kΩ, R15 = 5.49kΩ. The voltage divider R23/R25 must be changed so that a divided voltage is 4.2V. (***Note from Andy: I have changed the resistor numbers to correspond to the circuit diagrams supplied to me, it seems to make sense!***)

A loosely coupled, two pole band pass filter for 9MHz is inserted between IC3 and IC6, this limits the broadband noise and helps to prevent self oscillation of the amplifier at high frequencies. The coils must be changed if the amplifier is used for other intermediate frequencies. ***(Note from Henning: for 9MHz to 10.7MHz; only the capacitors must be changed the coils can stay the same)***

According to the data sheet the output of the AD603 is very low impedance it states that it is around 2Ω at 10MHz. Trying to match this low impedance to the band pass filter via a capacitive

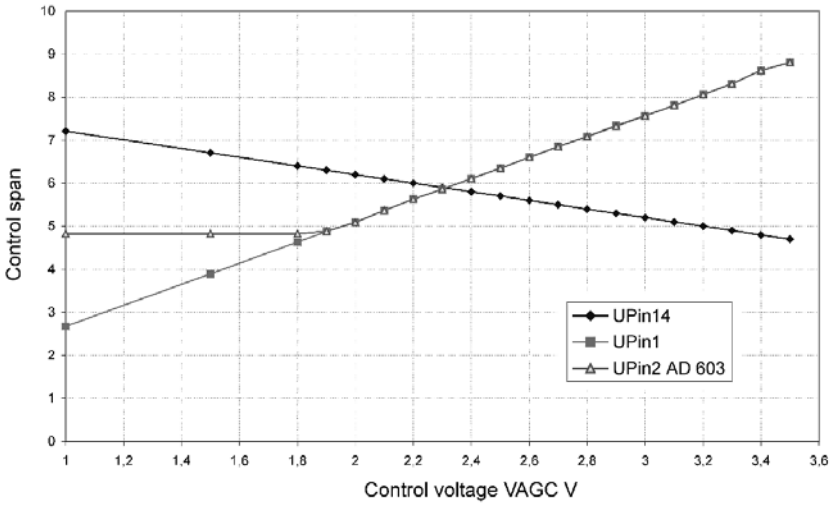


Fig 6: Control voltage and control range at various points of the circuit.

divider or using a small capacitor to the "hot" end of the first resonator failed.

The cure was to add a series resistor (R20) to the capacitive divider of the filter.

Table 3: Voltages for given values of control voltage V_{AGC}.

U_{AGC}	U_{Pin14}	U_{Pin1}	$U_{Pin2\ AD\ 603}$
1	7,21	2,67	4,83
1,5	6,71	3,89	4,83
1,8	6,4	4,63	4,83
1,9	6,3	4,88	4,88
2	6,2	5,09	5,09
2,1	6,1	5,37	5,37
2,2	6	5,63	5,63
2,3	5,9	5,86	5,86
2,4	5,8	6,11	6,11
2,5	5,7	6,35	6,35
2,6	5,6	6,6	6,6
2,7	5,5	6,85	6,85
2,8	5,4	7,08	7,08
2,9	5,3	7,34	7,33
3	5,2	7,57	7,57
3,1	5,1	7,81	7,81
3,2	5	8,06	8,06
3,3	4,9	8,31	8,31
3,4	4,8	8,62	8,62
3,5	4,7	8,81	8,81

5.3. Control voltage

IC1 and IC4 are used to convert the AGC voltage (connected to ST1) in the range 2V to 2.84V to the appropriate DC voltages at the G_{NEG} inputs of the two AD603s. Thus a regulating rate is 100mV/10dB this means 830mV for the range of 82dB. The two IF amplifiers IC3 and IC6 need a control voltage increase of 2V, so that a gain control voltage signal of 2V/0.82V = 2.43 is necessary.

The operational amplifier IC1c is a buffer stage for the control voltage supplied at St1. The voltage set by the trimmer potentiometer R13 is buffered with IC1b, this sets the start point of control. The control voltage and starting voltage are added in the summing amplifier IC1d, its output signal is is then amplified and inverted by IC1a.

From the data sheet for the AD603 [2; Page 3, footnote 4] the control voltage on pins G_{POS} and G_{NEG} can be between $-V_s$ + 4.2V to $+V_s$ -3.4V. In the circuit V_{NEG} = 0V; V_{POS} = +10V, the limit values are therefore 4.2V and 6.6V which caused

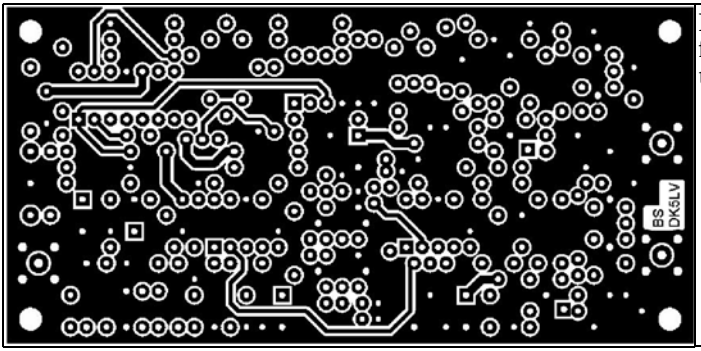


Fig 7: PCB layout for the top side of the IF amplifier.

problems with the prototype. Therefore a clamping circuit was added to IC4, which prevents G_{POS} falling below 4.7V, determined with the voltage divider R23/R25. In order to prevent the control voltage to the AD603 control inputs exceeding their maximum values R26 (1kΩ) and D3 (ZPD6.8) were added. (***Note from Henning: these components were inserted after the layout, R26 is mounted vertically***)

Fig 6 shows the voltages at different pins of IC1 and pin 2 of the two AD603s for control voltages in the range 1 to 3V.

5.4. Buffer stages

There are two separate RF outputs from the IF amplifier to feed a demodulator circuit and an AGC (control voltage) circuit; these must be well decoupled from each other.

The output impedance of the IF amplifier ICs is very low impedance, however according to data sheet the distortion free output voltage rises with increasing load resistance. Therefore dual gate MOSFETs are used for the two buffer stages. Gate 2 is supplied with a constant voltage from a voltage divider; the drain resistor prevents parasitic oscillations. The buffer stages showed signs of self oscillation, which could be prevented by the choice of the resistors R42 and R45 to 1kΩ and a load on the drain resonant circuit of R41 and R47. The resistors R32 and R43 uncouple the buffer stages.

6.

Construction of the IF amplifier

The IF amplifier is built on a 111mm x 55mm double sided PCB that fits into a standard tinplate housing. The PCB layout is shown in Figs 7 and Fig 8. The

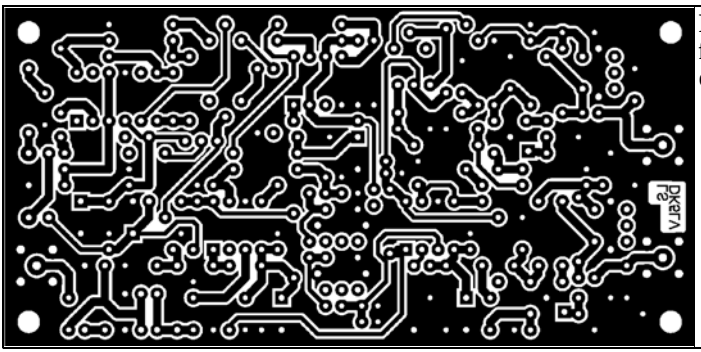


Fig 8: PCB layout for the bottom side of the IF amplifier.

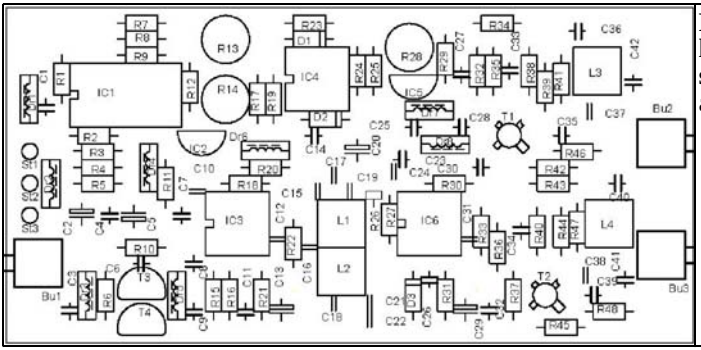


Fig 9: Component layout for the top side of the IF amplifier.

component layouts are shown in Figs 9 and Fig 10. For non-plated through printed circuit boards the ground connections between the two surfaces must be made by soldering links to prevent self oscillations.

Assembly of the printed circuit board begins with the two voltage regulators IC2 and IC5, once fitted set the output voltage using R14 and/or R28 at St3, St2 to 10V with a supply voltage of 12V. Next the components around IC1 and IC4 are fitted. Test these components by feeding an adjustable voltage of 2 to 3V to St1, using a ten turn potentiometer, measure the voltage across R24 and/or pin 1 of IC3 and/or IC6 with a digital voltmeter. This voltage must remain constant for voltages smaller than 2V at St1, rise after the starting point is reached. This start point can be adjusted with R13, it should be adjusted to 2V.

Next the components around IC3 and IC6 are fitted and checked. The voltage at pin 1 of IC6 should be 6.7V and the voltage at pin 1 of IC3 should be 4.7V. The two AD603 ICs can then be fitted, make sure they are from the same batch. Finally the two buffer stages are fitted. Check that the drain currents are between 5 and 10mA by measuring of the voltage drop across the source resistors.

The band pass filter can now be adjusted using an RF signal on Bu1. The two outputs of the IF amplifier are terminated with 50Ω and the output levels set so that there is no overload, the maximum output is 0dBm = $224mV_{eff}$ = $631mV_{ss}$.

6.1. Problems with the prototype

Most problems with the prototype were self oscillation caused at maximum gain. With capacitive coupling of both amplifiers, as intended in the data sheet and [11], the amplifiers oscillated at approximately 70MHz. A double tuned band pass filter between the two AD603 elimi-

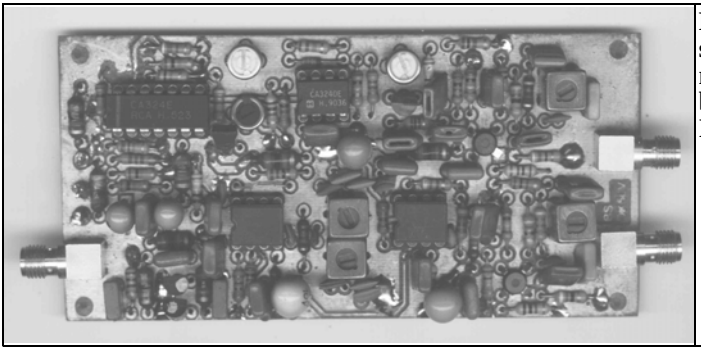


Fig 10: Picture showing component layout for the bottom side of the IF amplifier.

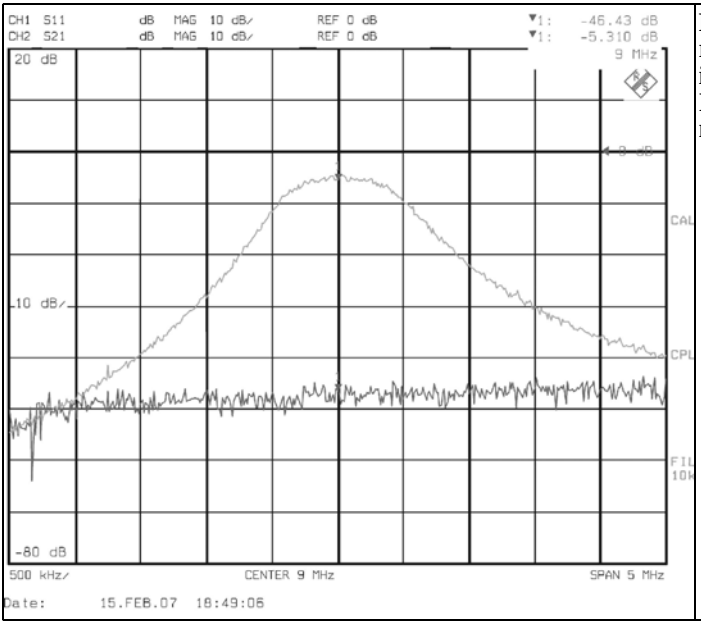


Fig 11: Frequency response and the input match of the IF amplifier for maximum gain.

nated this problem.

The decoupling of pin 4 on each AD603 is critical so several capacitors of different values should be used.

Coupling of the band pass filter to the low impedance output of the AD603 only

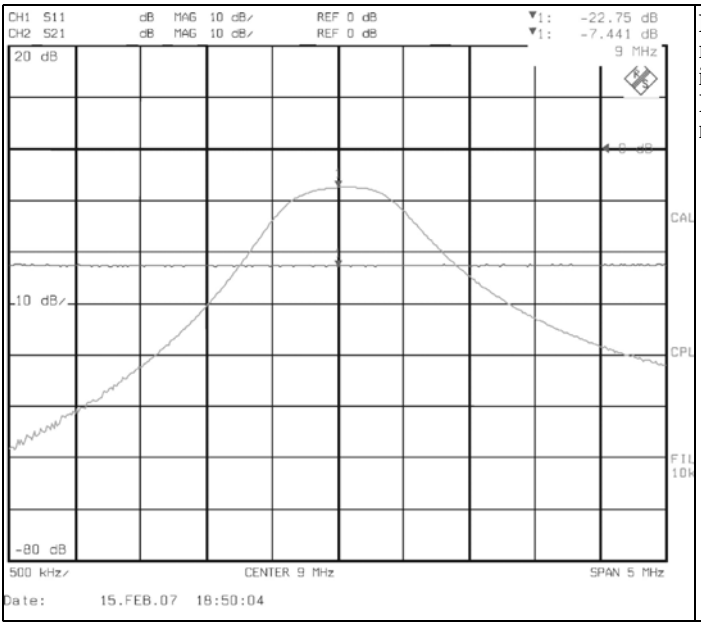


Fig 12: Frequency response and the input match of the IF amplifier for minimum gain.

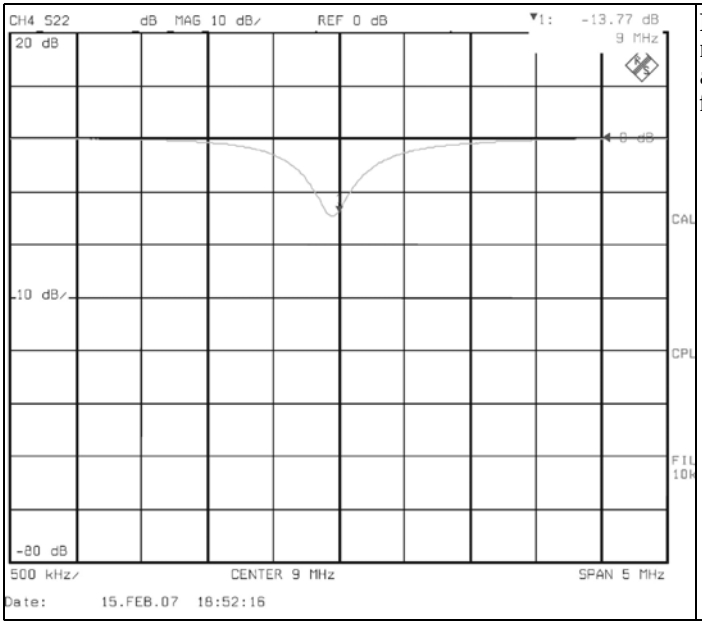


Fig 13: The output matching of the IF amplifier at the first output (Bu2)

succeeded by inserting a series resistor between the output of the AD603 and the capacitive divider of the band pass filter.

The two MOSFET buffer stages gave good isolation of the two outputs but they oscillated very easily. The solution was a 1kΩ resistor from gate 1 to ground, damping the drain circuit with a 4.7kΩ

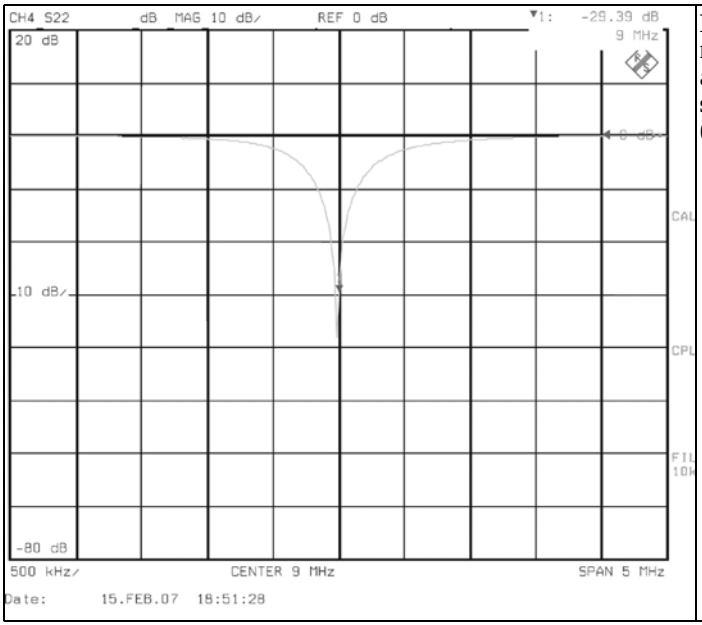


Fig 14: The output matching of the IF amplifier at the second output (Bu3)

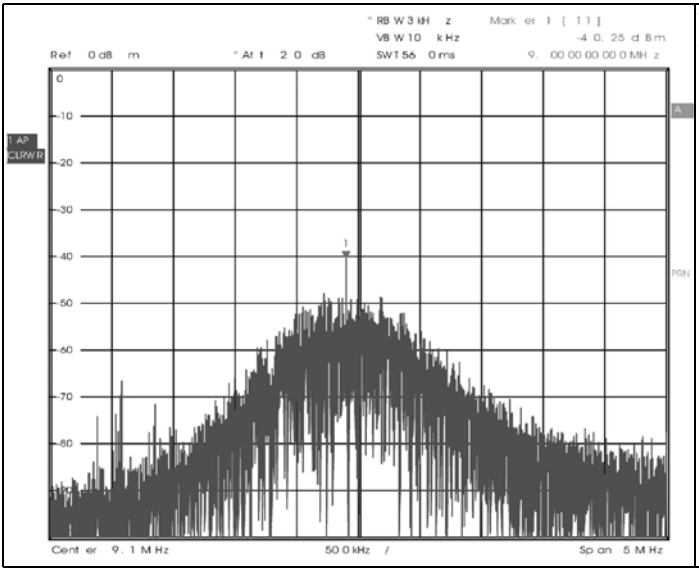


Fig 15: Isolation of the two outputs

resistor and isolating the two RF inputs with 470Ω series resistors.

The choice of MOSFET is important, a BF960 and a BF965 were used initially but using BF910s gave improvements. Both MOSFETs should be operated with a drain current of approximately 10mA.

It would be nice to increase the control range by adding a further AD603 but the problem with self oscillation would be much worse.

6.2. Measurements of prototype

In the prototype AD603 gain setting resistors were replaced by links, the measured values refer to this modification.

Fig. 11 shows the frequency response and the input match of the IF amplifier at maximum gain. Because the network analyser delivered output powers not less than -25dBm at its ports, an attenuator was inserted between the output port of the VNA and the input of the IF amplifier. The resulting good input match is due to these external attenuators!.

The overall gain was 80dB – 5dB = 75dB, thus around 10dB too low for use in a short wave receiver as shown in Fig 1. However if a 2.2kΩ resistor is used for R18 in place of the link, the gain increases by 10dB.

The frequency response and the input match of the IF amplifier for minimum gain is shown in Fig 12. The input match for the prototype is -22dB at minimum gain of the IF amplifier, which was measured without the external 80dB attenuator. It gets worse above 50MHz. These values were with a total value of the current for the two JFETs of 15mA (i.e. voltage drop = 1.5V across R6 =). This could vary with variations in the FETs. Two other FETs gave –15dB.

The output match of the IF amplifier at the first output (Bu2) is shown in Fig 13. The output matching is only -15dB. The transistor has a drain current of 10mA.

Despite same circuit the second output (Bu3) exhibits a substantially better match, see Fig 14, the drain current of this transistor was only 6mA.

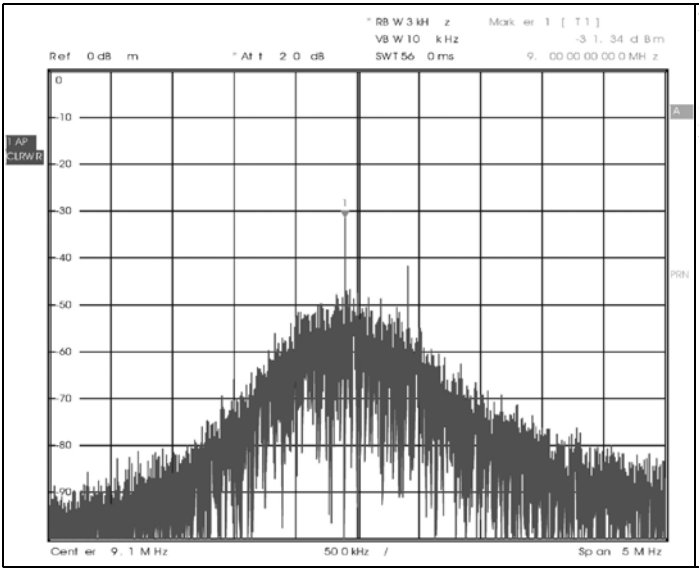


Fig 16: The output spectrum of the IF amplifier with an input signal of -107dBm

The isolation of the two outputs is shown in Fig 15. A 0dBm 9MHz signal was fed into Bu2 that gave a -40dBm signal at Bu3. This means the isolation is 40dB. Checking the result with a network analyser the isolation was measured as -52dB. The isolation is sufficient in each case and exceeds the requirements of the specifications.

The output spectrum of the IF amplifier with an input signal of -107dBm is shown in Fig 16. The spectrum analyser was set to a range of 3kHz. The self-noise can be seen at 20dB below the information signal. With these values the noise figure of the IF amplifier only reaches 13dB, instead of the 6dB required. An exact measurement of the

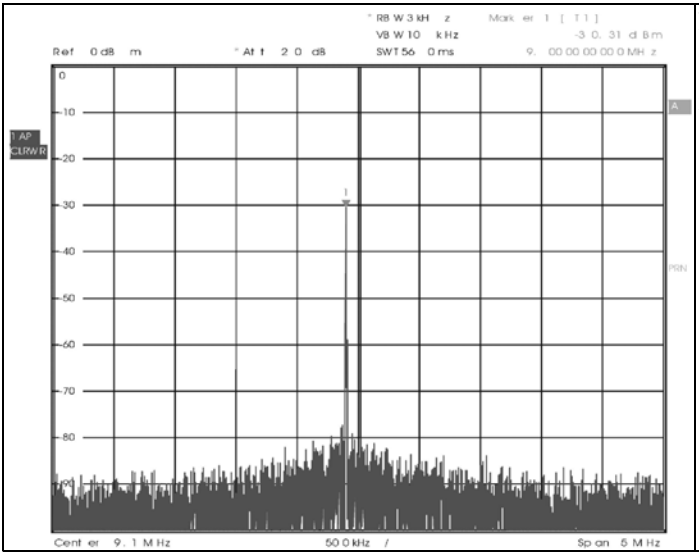


Fig 17: The output spectrum of the IF amplifier with an input signal of -27dBm

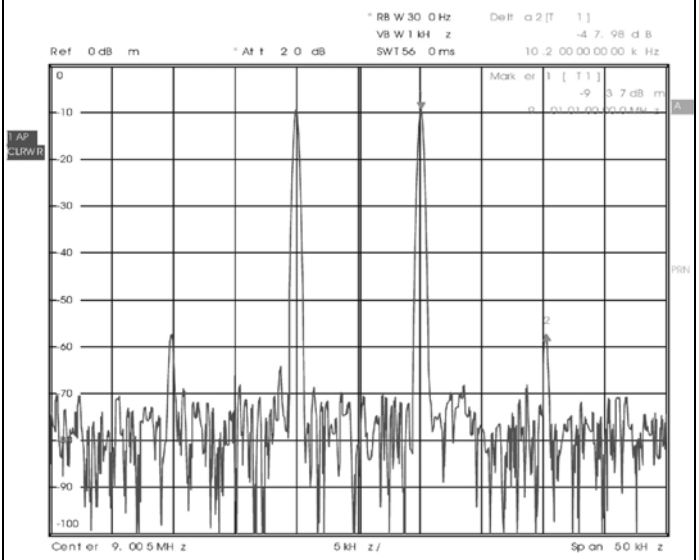


Fig 19 : The output spectrum of the IF amplifier with two input signals, (9 and 9.01MHz)

SINAD was made with a demodulator downstream using a distortion factor meter (Stabilock 4040). 20dB SINAD was measured with an input level of -114dBm.

The output spectrum of the IF amplifier with an input signal of -27dBm is shown in Fig 17. The noise floor noise lowered because the gain of the two amplifiers is changed.

The output spectrum of the IF amplifier with two input signals, (9 and 9.01MHz) and maximum gain is show in Fig 18. Power output is adjusted to around 20dB higher than the nominal level, in order to be able to recognise intermodulation products better, the products are weaker under these conditions by around 47dB in relation to a single tone.

The measurement of the 1dB compres-

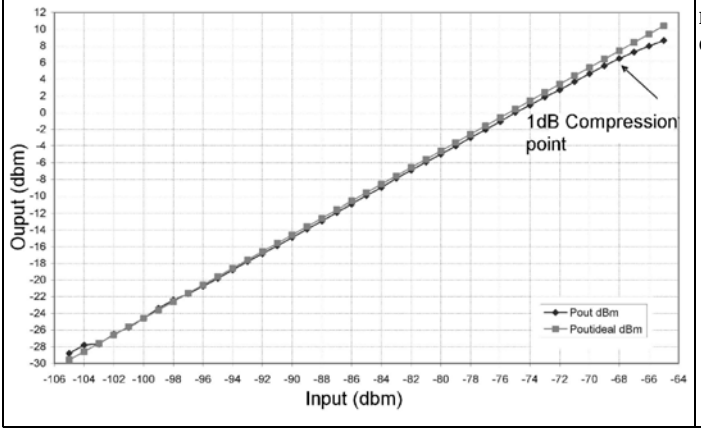


Fig 19: Measurement of the 1dB compression point.

sion point is show in fig 19. In addition the control voltage of the IF amplifier was set for maximum gain. Power output was measured with an HP437 with HP8481 measuring head. The 1db compression point occurred at a power output of +6.2dBm that is higher than required in the specifications.

7.

Conclusion

The control range of "only" 84dB may appear too low 100dB would be better. Experiments with a PCB containing three AD603s were unsuccessful due to self oscillation.

Experiments with an AD605, which contains two individual amplifiers in one housing, with only one supply voltage and an internal low noise preamplifier were unsuccessful. The amplifiers oscillated at maximum gain. A band pass filter between the amplifiers may help but this is still to be examined.

Further circuits have been developed for SSB/CW, an AM demodulator and an AGC circuit generating the control voltage from the high frequency IF signal.

After more testing the amplifier showed AGC voltages >2V without any RF signals. This is due to rectification of the wideband noise of the IF amplifier. A work around is the use of a two pole crystal filter between the output of the AD603 and the two buffer stages. A new PCB has been designed but not tested. There is still a problem with the S meter starting at S0, a solution could be to build a narrow band pass filter to reduce the broadband noise and using a logarithmic rectifier circuit. These modifications will be described in a later article.

8.

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Gunthard Kraus, DG8GB

Practical Project: Durable and reproducible patch antennas for the 2.45GHz WLAN band, Part 2: Continued from issue 1/2007

3.4. Results of measurement and completion of the project

With the antenna manufactured including these changes the SMA socket was soldered to the ground surface and the inner connected to the patch surface. Measurements were taken on the new antenna with an HP8410 network analyser a directional coupler and a frequency counter. Fortunately the results from earlier work were confirmed therefore they can be published and used for future SONNET developments. SONNET Lite simulates the adjustment very accurately, however the results for the resonant frequency are not correct. That means any antenna manufactured has a somewhat low resonant frequency. For the sample antenna the measured minimum reflection factor at resonance was about 1%, which corresponds to an S11 of approximately -40dB. However this was at a frequency of 2383MHz but it should have been 2450MHz that is about 2.5% difference.

For the correction and to finish the development there are three in possibilities:

- Repeat the SONNET Lite simulation using approximately 2,5% higher resonant frequency (accurately, 67MHz).

- Simulate the actual values measured for the antenna and accurately determine the deviations from the ideal then correct the layout using these. With the full version of SONNET that would be easy, but with the limited main memory of the test version and the limited number of cells it is very difficult or nearly impossible.

- Keep your nerves and use a pocket calculator to reduce all dimensions by the factor: 2383MHz/2450MHz = 0.972653 to shift the resonance upward. Using these dimensions a new Patch was made:

  Length = 31.99 mm x 0.972653 = 31.12 mm

  Width = 55.68 mm x 0.972653 = 54.16 mm

  Feed point coordinates 27.08mm/8.09mm

A new antenna was sketched on an 80mm x 60mm printed circuit board and manufactured. This gave the following result:

> The resonant frequency with the minimum S11 (between -34 to –40dB) is now with approximately 2449MHz.

The new result is very satisfying, therefore nothing else needs to be done.

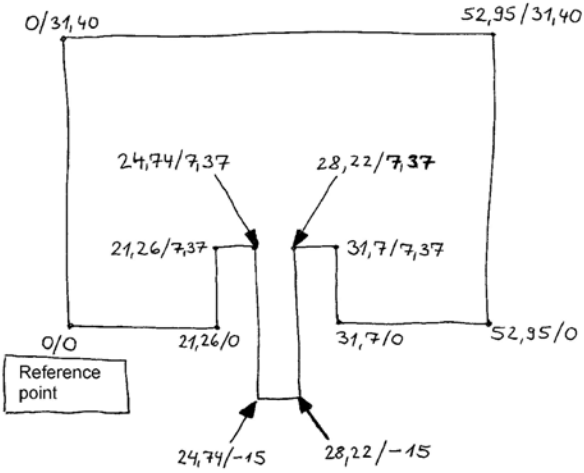

Fig 26: Sketch of the patch antenna ready for SONNET simulation.

4.

Rectangular Patch with an integrated 50Ω microstrip feeder

4.1. Draft

In this version a fascinating fact is that a patch can be fed directly by a 50Ω feeder without using a transformation line (λ/4 line) enabling a plug or semi rigid cable to be connected at the side of the patch. For many applications this is an advantage, in addition it saves space and makes it possible to use the same PCB dimensions as in the previous example. First, an overview of the peculiarities of this design beginning with the simulation from the previous chapter.

The patch dimensions of the last rectangular version with a feed point on the lower surface are:

Length = 31.12mm

Width = 54.16mm

Feed point coordinates
= 27.08mm/8.09mm

With the SONNET editor use these values as precisely as possible. The feed from the lower surface is omitted and instead use a 50Ω stripline (width 3.48mm - see chapter 3.3 in part of 1) from the edge of PCB to the patch face. On the left and on the right of this line leave a space equal to the line width of 3.48mm.

The external dimensions of the PCB are 80mm x 60mm, leaving 15mm at the top and bottom of the patch. Extend the stripline below the bottom edge of the patch by this distance. Fig 26 show a sketch used as a start point for the SONNET simulation.

All the setup parameters remain unchanged, just draw the new structure but use the polygon function instead of the rectangle function from the “Measuring Tools” then the “View” menu.

Note: The end of the feeder has a port instead of a via. The properties of the port must be changed (right mouse click on Properties) to “Autoground” otherwise there will be an unpleasant error message and the simulation will be aborted! The result is shown in Fig 27 with all of the important information. The dimensions are slightly different because of the SONNET defaults, the actual dimensions are:

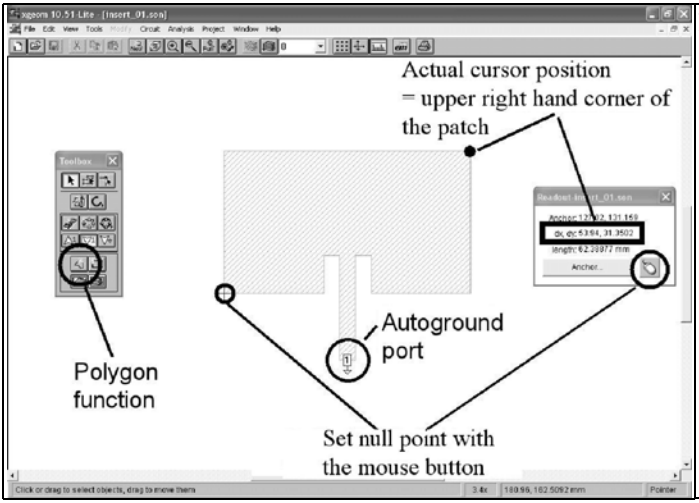

Fig 27: The patch antenna set up in SONNET.

Length x Width = 53.94mm x 31.35mm

Feed point = 8.32mm from the lower edge of the patch

The result of the first simulation can be seen in Fig 28 represented as a Smith chart. The resonant frequency is not correct but there is something more important to consider first:

For this design the feed point is so far into the patch face that it causes the field distribution to lower the feed impedance to below 50Ω and changes the resonant frequency (This information can only be investigated with an EM simulator, an S parameter program such as PUFF is completely useless without suitable models). The necessary re-design gives improvements for each change but it is somewhat annoying, but after some passage of time finally the following data is found:

Length x Width = 31.99mm x 53.94mm

Feed point = 5.76mm from the lower edge of patch

The result using SONNET Lite is shown in Fig 29 so it is the time to make a new sample PCB.

4.2. Measurement of the corrected PCB

The sample PCB gave the following results:

The lowest value of the reflection factor is +13% at a frequency of approximately 2435MHz.

So we have to apply the patch dimension correction factor of 2435/2450MHz = 0.9938775 to increase the frequency and additionally have to move the feed point towards the patch centre in order to decrease the input impedance.

The first problem is the high input impedance.

The patch antenna length (31.99mm) corresponds to about a half wavelength of 32mm at the operating frequency. Each end will have a voltage maximum, but the centre will be a current maximum with the voltage being zero, as with for a dipole (this can be confirmed using the SONNET current distribution simulation with “View Current “).

Thus the feed characteristics can be interpreted as follows by only considering the left half of the patch:

It is a piece of line with the length l = λ/4. The condition at the start of the line

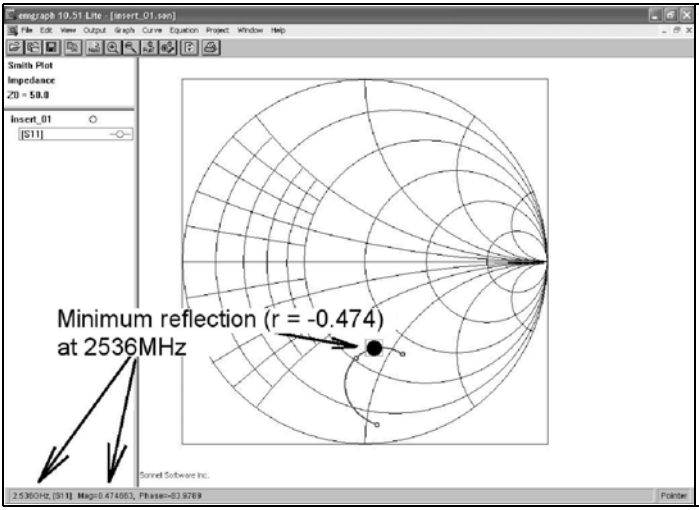

Fig 28: The results of the first simulation.

(patch edge) is the radiation resistance; this means high voltage and low current. At the end of the line (Patch centre) the condition is the same as a short circuit (voltage = zero, current = maximum).

From the patch centre the voltage rises with a sine function towards the left. If the line is tapped at some point it forms a transformer using the following relationship:

The resistance changes as the SQUARE of the voltage along the line AND the voltage changes sinusoidally over the line length. This is shown in Fig 30. For a distance of 5.76mm between radiating patch edge and feed point the PCB manufactured gave a reflection factor of +13%. That results in an input impedance of

$$R_{in} = 50\Omega \cdot \frac{1+0.13}{1-0.13} = 65\Omega$$

The distance of the feed point from the patch centre is about

16mm - 5.76mm = 10.24mm

The rest can be done with a pocket calculator. The new point for an input impedance of 50Ω and its distance from the patch centre is “x” in formula 1:

$$\frac{50\Omega}{65\Omega} = \left[\frac{V_{50\Omega}}{V_{65\Omega}}\right]^2 = \left[\frac{V_{\max}\cdot\sin\left(90°\cdot\frac{x}{16mm}\right)}{V_{\max}\cdot\sin\left(90°\cdot\frac{10.24mm}{16mm}\right)}\right]^2 = \left[\frac{\sin\left(90°\cdot\frac{x}{16mm}\right)}{\sin\left(90°\cdot\frac{10.24mm}{16mm}\right)}\right]^2$$

After rearranging we get formula 2:

$$\sin\left(90°\cdot\frac{x}{16mm}\right) = \sqrt{\frac{50}{65}}\cdot\sin\left(90°\cdot\frac{10.24mm}{16mm}\right) = 0.877\cdot 0.844 = 0.74$$

This is an angle of 47.473 degrees, so it is now very simple to calculate "x"

$$90°\cdot\frac{x}{16mm} = 47.473°$$

The remainder is simple, after rearranging the formula:

x = 8.49mm

Thus a new distance from the patch edge is:

16mm - 8.49mm = 7.51mm.

Note: The measurements of the patch must be changed by a factor of 0.9938775 before the next PCB is made to correct the resonant frequency giving the final result:

Length x Width = 31.79mm x 53.61mm

Feed point = 7.46mm from the lower edge of the patch.

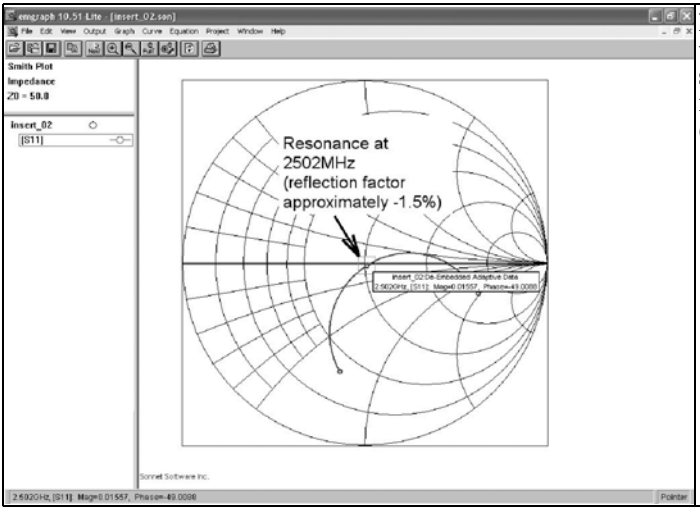

Fig 29: Results of the second simulation with revised patch dimensions.

4.3. The last sample PCB

The third PCB manufactured with these dimensions was tested with the network analyser giving the results:

The resonance was 2420MHz and the reflection factor of approximately 1%, That means:

- The corrections were correct, but…
- by moving the feed point toward patch centre the resonance changed far more than expected. Now all dimensions are changed by the factor:

2420 MHz/2450 MHz = 0.9877551m making the new dimensions:

Length x Width = 31.40mm x 52.95mm

Feed point = 7.37mm from the lower edge of the patch.

Something astonishing was found when this was measured; the new resonant frequency was now nearly 2470MHz and the input impedance amounted to less than 50Ω (reflection factor = 8%). This confirms that this design reacts dramatically when only small changes in dimensions are made. Even the simple reduction of the dimensions gave bad results.

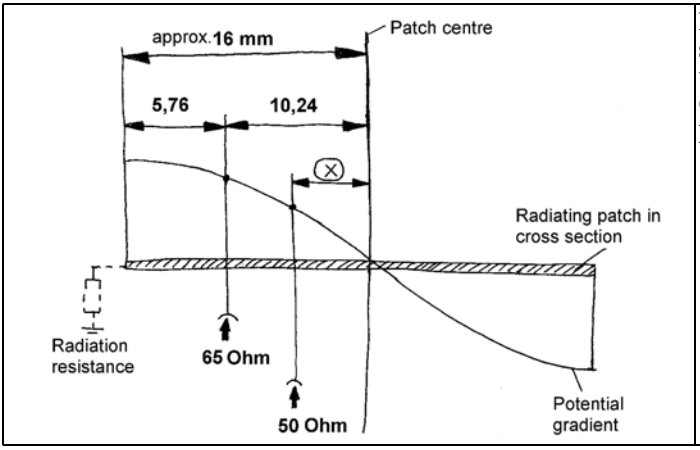

Fig 30: Sketch showing the how the impedance changes with feed point.

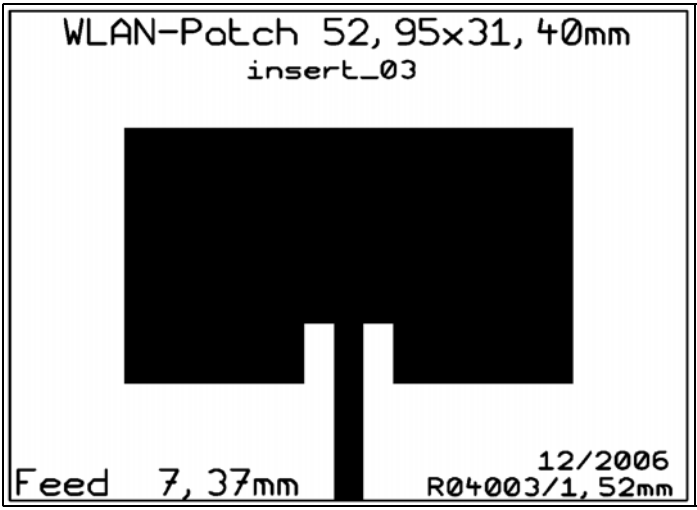

Fig 31: The final PCB layout for the patch antenna. Please remeber to always mark each PCB layout clearly so that you know which version it is!

A more exact investigation showed that the following effects are responsible:

- the reduction pushed the resonant frequency upward as required, but…
- the overall dimensions of the patch antenna are near to the edge of the PCB an it is unfortunate that the conditions for a correct SONNET simulation do not apply (remember: Distance of the patch layout must be at least a half wavelength from the box wall…).
- The PCB was made from a new lot of material and the properties seem to differ within the production process..

Learning from all of this, the final dimensions were set in the centre between version 2 (resonance 2420MHz) and version 3 (resonance 2470MHz). Keep in mind that these lie within the range between -1% and + 1%, and that it is very sensitive.

5.

The round antenna

This is a strange antenna and we have to ask if it can be made to resonate and what are the advantages over the designs used so far. In the long run only easier handling is an advantage with the lack of sharp corners because there are no electrical advantages rather there are disadvantages. This can only be seen by comparing the current distribution for a rectangular patch (Fig 32) with that of a round antenna (fig 33)

The rectangular patch has the same current distribution from left to right. The current is zero along the upper and lower patch edges and a maximum on the centre line (with the voltage zero). This leads to much cleaner linear polarisation conditions, therefore the electrical lines of flux run parallel to the left and right patch edges and are perpendicularly on the lower and upper patch edges. If a square antenna is made two feeders can be used shifted by 90° to produce circular polarisation. This is used in an LNB to separate the vertical and horizontal fields, this can be seen when an LNB cover is removed.

This looks completely different for the round antenna. The current maximum shown in Fig 33 resembles an egg with the current stopping before the edge of antenna giving changed field patterns. It will be less sensitive to alignment and

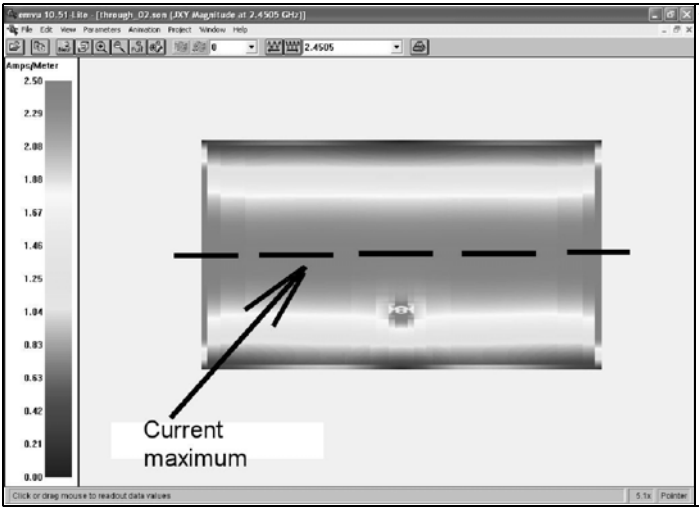

Fig 32: The current distribution of a rectangular patch antenna.

polarisation. Unfortunately the "Farfield Viewer" is not available in SONNET Lite, otherwise this question could be answered by the simulation of the far fields.

Assistance was sought, in the usual way (from radio amateur to radio amateur), from the German SONNET representative (Dr. Volker Mühlhaus in Witten). He was happy to compare the radiation patterns of the rectangular antenna version 1 with the round antenna and the simulation results using the full version of SONNET are shown in Fig 34 and Fig 35.

The round antenna exhibits less gain. But the assumption that is would have worse cross polarisation is given the "all clear"; the effect is there but so small that it plays no role in practice. Therefore both antennas are usable for linear polarisation. So a sample of a round antenna can be made.

5.1. First draft

First there is a bitter pill: the round

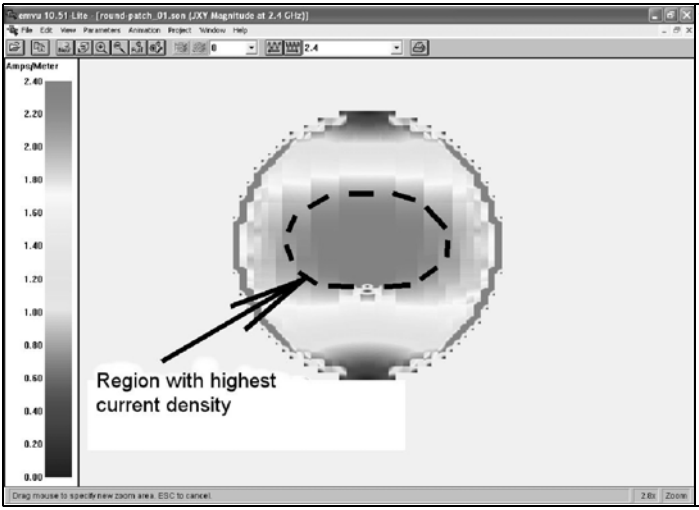

Fig 33: The current distribution of a circular patch antenna.

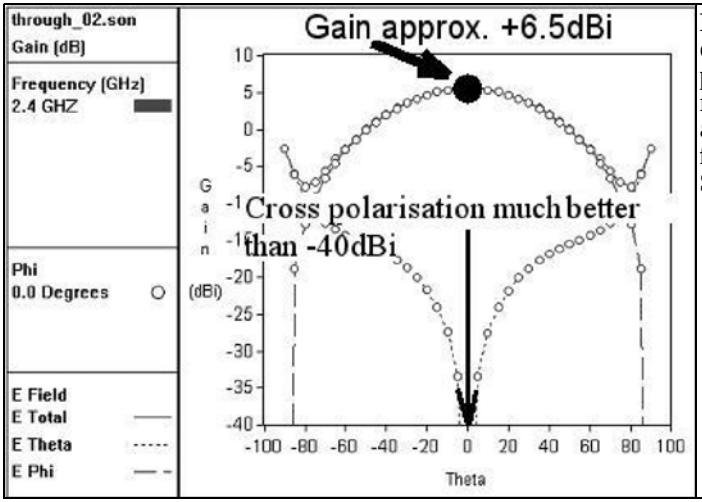

Fig 34: Simulation of the radiation pattern of a rectangular patch antenna using the full version of SONNET.

design clearly requires higher analysis effort, therefore it is easy to exceed the memory limit of 16Mb with the current box attitudes and the simulation is aborted. If a 1mm x 1mm cell size is used, click "Estimate memory" and now you can see that SONNET occupies only 12Mb. Fig 36 shows these details as well as the necessary new box attributes, but an addition comment is necessary; the main memories requirement can only be determined with "Estimate MEMORY" if the complete antenna design is drawn and correctly stored as a project. Some experimentation is inevitable but the following information is required for the design:

- The circular design is drawn with "the Doughnut" function. Fig 37 shows the necessary information to draw filled circles.
- The lowest point of the patch on the screen is the point of reference.
- After some attempts a patch diameter of 38mm (radius = 19mm) and a feed point distance of 13mm (measured

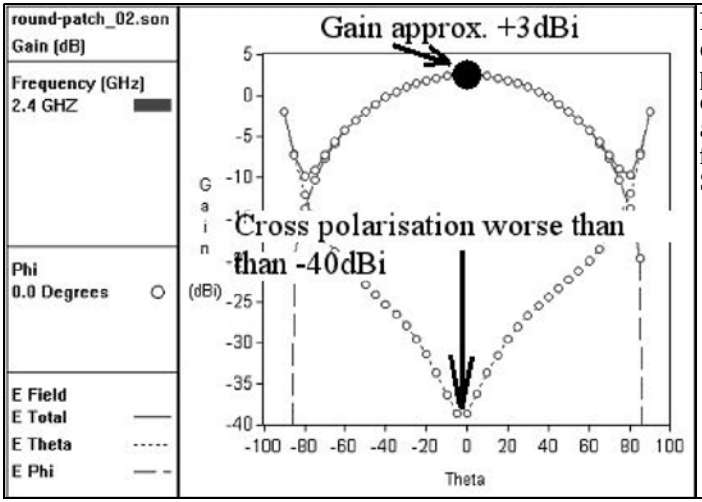

Fig 35: Simulation of the radiation pattern of a circular patch antenna using the full version of SONNET.

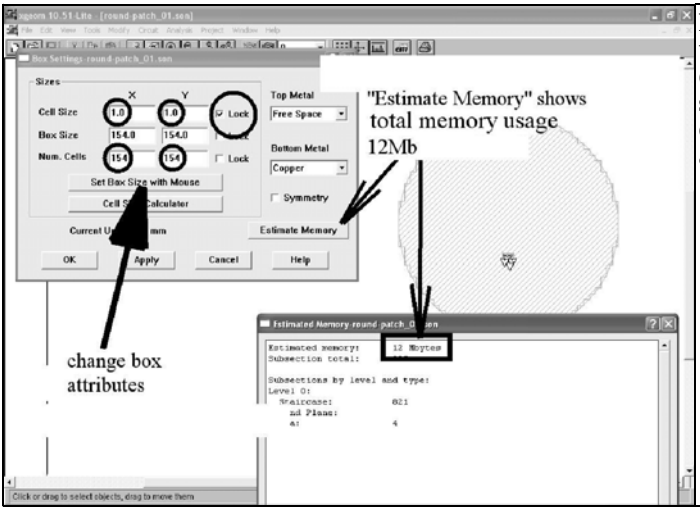

Fig 36: Changing the memory usage of SONNET lite to simulate the circular patch antenna.

from the lower patch edge).

- The feed point must be attached with a "via" with a standard port.

The simulation result shown in Fig 38 shows the best approximation to the given requirements as a compromise because the large jumps due to the cell sizes Dx and Dy of 1mm result in relatively large changes.

The next PCB is shown in Fig 39, it has a diameter of 70mm. The measured result is quite rough and it must be optimised afterwards as in the previous example.

5.2. Finished development with measured results

The network analyser (with polar display and microwave frequency counter) gave the results:

Resonant frequency f = 2374MHz, where the minimum reflection factor r was = +17%.

Do not be alarmed: that is only a frequency deviation of approximately 3% from 2450MHz! It can be optimised again:

Step 1: The measured reflection factor corresponds to an input impedance of

$$R_{in} = 50\Omega \cdot \frac{1+0.17}{1-1.07} = 70.5\Omega$$

and the associated measuring point is

19mm - 13mm = for 6 mm from the centre of the circle.

Step 2: Due to the somewhat strange current and voltage distribution of this patch shape it is difficult to calculate the voltage changes so the changes near to the feed point are regarded as linear from the centre. Applying this to the resistances:

$$\frac{50\Omega}{70.5\Omega} = \left(\frac{x}{6mm}\right)^2$$

Calculating "x" gives the new feed point measured from the centre of the circle.

$$x = 6mm\sqrt{\frac{50\Omega}{70.5\Omega}} = 5.05mm$$

Step 3: Only the correction of the resonant frequency remains using the factor:

$$\frac{2374MHz}{2450MHz} = 0.9689795$$

That results in a new circle radius of

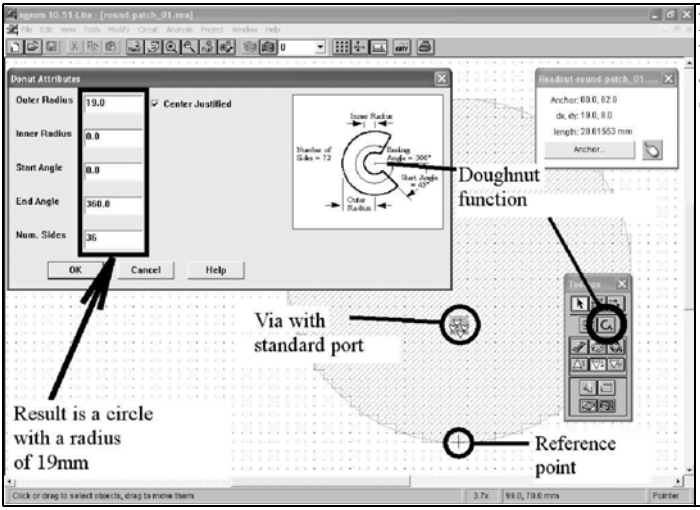

Fig 37: Drawing the circular patch antenna using the doughnut function.

19mmx 0.96989795 = 18.41mm

and a new feed point distance (measured from the centre) of

5.05mmx 0.9689795 = 4.89mm

Step 4: Make a PCB, drill the feed point hole from the earth side and free the hole to avoid short circuit between the ground plane and the central conductor of the SMA socket, solder the SMA socket and then make the measurements with the network analyser. The result: Reflection about +1% at 2465MHz. This is a +0.6% frequency deviation and a further iteration increasing the patch size by around the factor 2465MHz/2450MHz = 1.0061 gives an antenna with the given goal.

6.

Summary

The sample antennas 1 and 3 worked straight away in practical test on WLAN access points of friends, pupils and acquaintances. The only change was to make the SMA socket a reverse polarity SMA.

All users preferred version 1, so a small batch of 12 was manufactured. There was a further small surprise: 10 antennas had a resonant frequency between 2445 and 2450MHz, that is a normal distribution. But with two the resonant frequency was only 2440MHz which cause the designer to wonder!

Nothing visually different, but the cause was found quickly. The two antennas were made from the newest and freshly purchased batch of PCB material. Obviously there are differences between the individual batches, which lies in the permissible tolerance range of the PCB material. Such deviations are the hidden things that catch up on the developer and should be remembered for the next project. In such a case consider raising the resonant frequency again by approximately 4MHz.

It was fun working with free modern simulation and CAD software, a joy and a motivation, which is not influenced by money. Having described the considerations and calculations in this article the author hopes that more people will enjoy such developments.

Special thanks go to the company who made SONNET Lite freely available, and to the help of the specialists Dr.

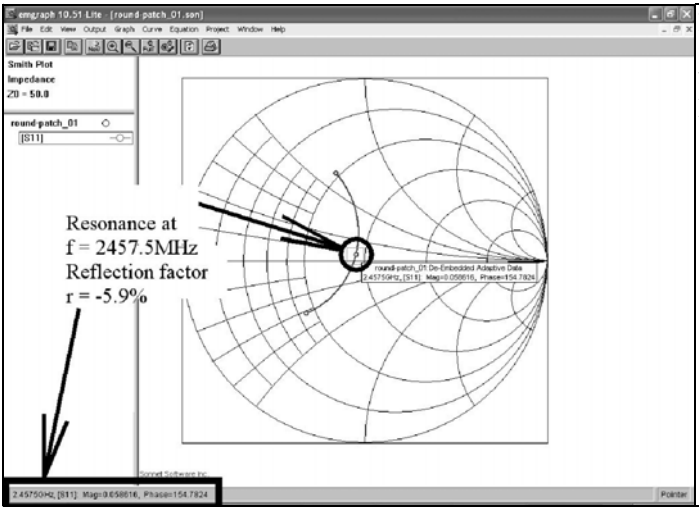

Fig 38: The simulation results for the circular patch antenna.

Mühlhaus (SONNET Germany), who helped with problems by telephone and by discussion with partners to uncovering mistakes. Also to Mr. Schulze Höing from the MAURITZ company in Hamburg who provides the necessary free supply at ROGERS R04003 again and again for PCB development. Finally thanks to my friend, colleague and PCB maker Martin Merkel. Without his infinite patience both the sample as well as the quantity production of the antennas would have been impossible and this article would probably not have seen the light of day.

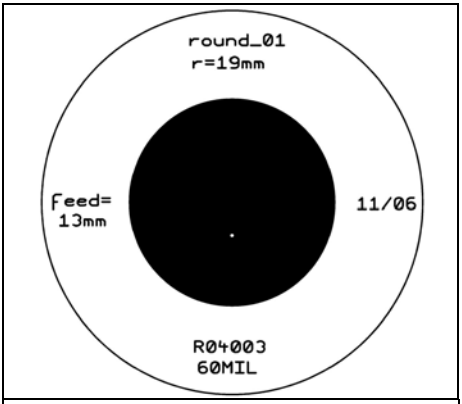

Fig 39: The PCB for the circular patch antenna.

7.

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[3]: Modern patch antenna design Part 1 and Part 2, Gunthard Kraus, DG8GB, VHF Communications Magazine 1/2001, pp 49 – 63 and 2/2001, pp 66 - 86

[4] Practical Project: Durable and reproducible patch antenna for the 2.45GHz WLAN band part 1, Gunthard Kraus, DG8GB, VHF Communications Magazine 1/2007, pp 41 - 55

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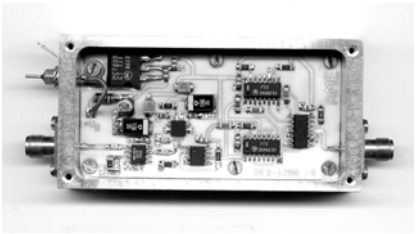

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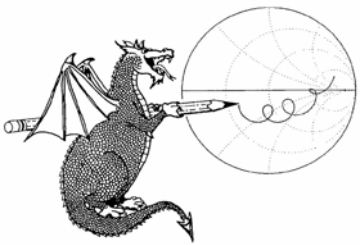

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