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for the Radio-Amateur

Especially Covering VHF,
UHF and Microwaves

VHF communications

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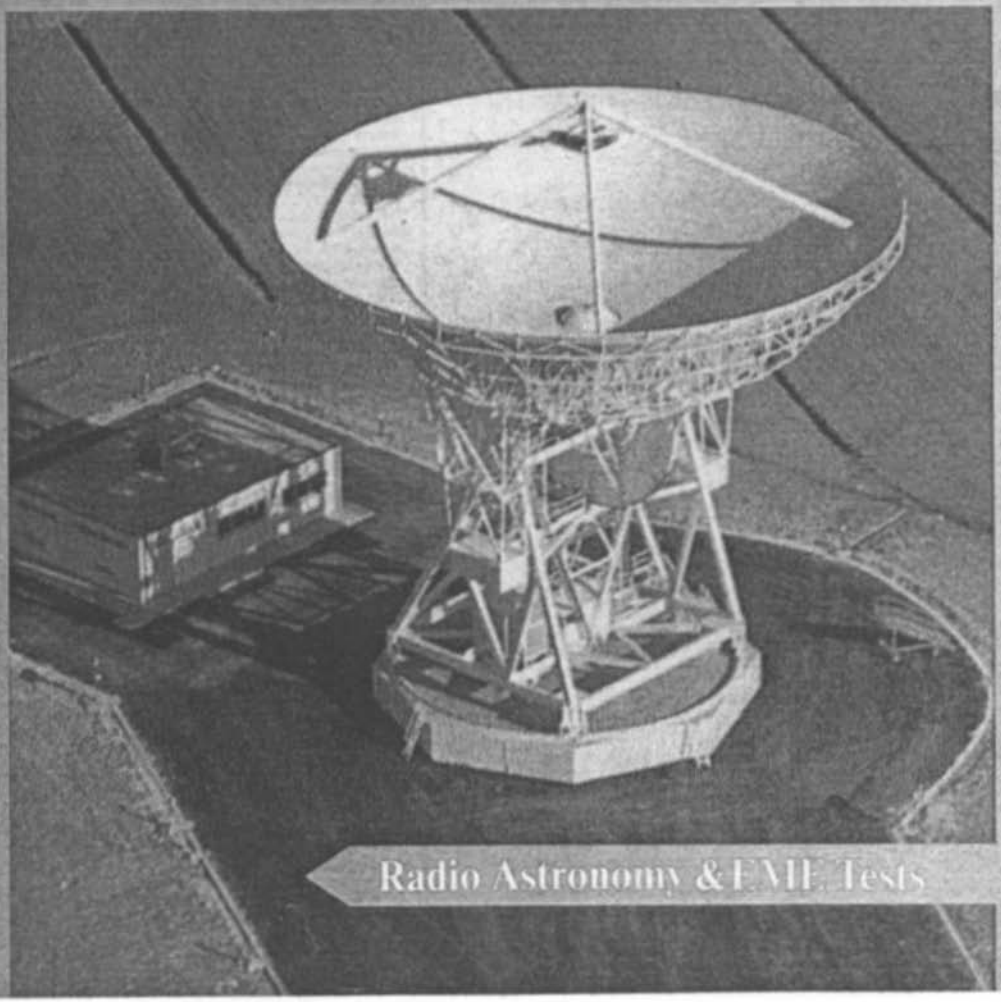

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VHF communications

A Publication for the Radio Amateur
Especially Covering VHF, UHF, and Microwaves

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Matjaž Vidmar, YT 3 MV

Digital Signal Processing Techniques for Radio Amateurs
Part 2: Design of a DSP Computer for Radio-Amateur Applications

As already explained in the theoretical part of the article (VHF COMMUNICATIONS 2/1988), I decided to design a computer with DSP capabilities around a standard 16 bit microprocessor, in particular the Motorola MC 68010. An additional requirement was to design the hardware such that it does not slow down the CPU in any way due to the speed requirements of DSP algorithms.

2.1. GENERAL DESIGN

The practical hardware design of a 16 bit microprocessor imposes many constraints. In comparison to an 8 bit microprocessor system, the number of connections is more than doubled. Further, 16 bit microprocessors have an order of magnitude faster bus than 8 bit microprocessors. Bus ringing and crosstalk, which are seldom a problem in a well-designed 8 bit microcomputer, usually cause troubles in 16 bit designs. Professional computer designers generally solve the problem by using a better printed-circuit-board technology, namely multilayer printed circuit boards. The latter are prohibitively priced if a small quantity is only required and this technology is therefore out of reach for amateur experimental work.

For experimental work a modular design with a common bus board, carrying just several multipole connectors with all the pins connected in parallel, is necessary. After a careful analysis of the MC 68010 bus signals, I found out that a bus with 64 pole connectors could be sufficient. The selection fell on the well-proven and reliable, but easily available and reasonably priced "Eurocard" connectors. A 64 pole "Eurocard" connector has two rows of 32 gold-plated contacts. The required parallel connections can be made all on one side of a double-sided printed circuit board

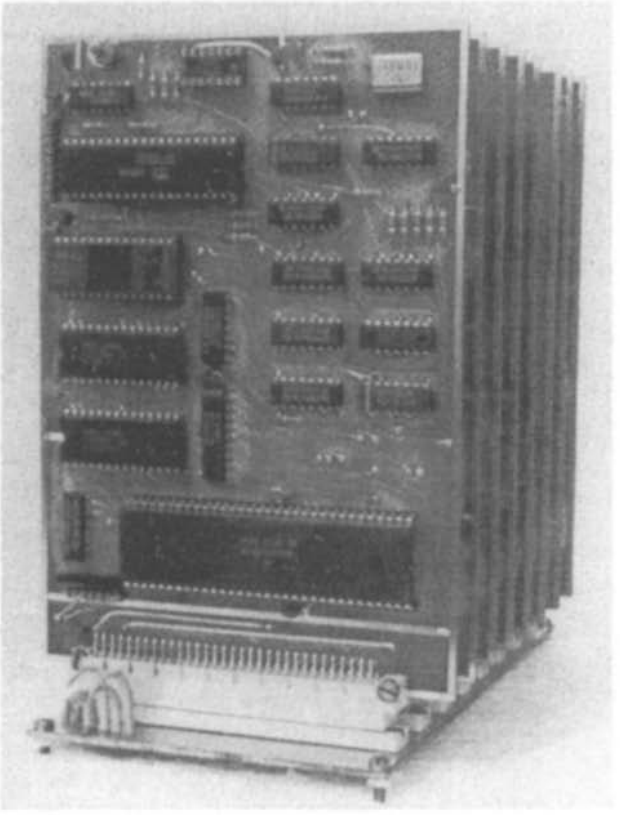

Fig. 2.0.:
The DSP computer with 1 Mbyte SRAM, without power supply unit and housing.

so that the other side can be used as an almost continuous ground plane to significantly reduce crosstalk between the signal lines.

Considering the technology I had available for the printed circuit boards – simple double-sided boards with not too fine line geometry and not too many feedthrough holes – the modules had to be made slightly larger than the standard "Eurocard" format. All the modules developed are 120 mm wide and 170 mm long. The modules represent functional units and all the connections among the modules themselves are made through the computer bus with "Eurocard" connectors (**fig. 2.0.**).

Of course, the hardware design of a computer also depends on the application and software used. Since I decided right from the beginning to use nonvolatile RAM as the main program and data storage, the computer bus also carries a continuous supply voltage obtained from a single NiCd battery in the power supply module. The latter supplies all the computer memory and the real-time-clock circuit. Even more important, a nonvolatile RAM requires a very reliable RESET circuit. The latter should also be able to prevent the destruction of the data during any power-up or power-down sequence by inhibiting the access to the RAM unless the supply voltage is within the specified tolerances. The RESET signal is therefore generated by the power supply module and made available to all computer modules through the bus.

Since I planned little use of magnetic media, I made no special arrangements for quick data

transfer to or from the computer memory. The computer has no DMA capability and the MC 68010 is hardwired to be the bus master all the time. In any case, the MC 68010 is fast enough to handle the data stream to or from a floppy-disk controller on its own, without the aid of a DMA controller. In the case of a DSP application with a typical 10 kHz sampling frequency, not using a DMA controller brings a penalty of only 10 % or less in terms of CPU time. Finally, for memory-to-memory transfers, the MC 68010 loop-mode instructions are almost as fast as a DMA controller.

In a 16 bit microcomputer design it is frequently convenient to use standard 8 bit peripheral devices because they are inexpesive and widely available. Since these are usually too slow to interface directly with a high-speed 16 bit microprocessor bus, additional interface circuits are required. The latter are placed on the peripheral modules where required due to the limited number of conductors available on the computer bus.

2.2. MC 68010 OPERATION

Before describing the various computer modules, a brief description of the MC 68010 CPU operation will be made. This introduction is intended for the reader that has a basic knowledge about the operation of a microcomputer, in particular of an 8 bit microprocessor, but has little or no experience with 16 bit microprocessors.

The MC 68010 has a 16 bit data bus and 32 bit internal registers. All addresses are internally 32 bits long and are referred to 8 bit bytes, corresponding to an addressing range of 2^{32} or 4 terabytes. However, the upper 8 address bits are not available externally (there are not enough pins on the package), and the addressing range is limited to 2^{24} or 16 megabytes. There are only 23 address lines, A1 to A23, since the 16 bit wide bus can access two bytes at a time. In the case of a single byte access, only half of the available data lines are used, either the lower 8 data lines D0 to D7 (odd address) or the upper 8 data lines D8 to D15 (even address).

16 bit data words are always addressed by an even address (LSB = 0). A word access on an odd address (LSB = 1) would require two separate bus cycles. The MC 680xx series of microprocessors do not tolerate word accesses on odd addresses, in contrast with some other 16 bit microprocessors, and a call to the address error handling routine is generated. All MC 68010 instruction codes are either one or an integer number of 16 bit words and the program counter is always incremented in steps of 2, 4, 6 or other even numbers.

A typical memory access (read or write) cycle is shown on **fig. 2.1.** The address lines A1 to A23 are set first, followed by the Address Strobe ($\overline{AS}$) signal going low. Two data strobe lines, Upper Data Strobe ($\overline{UDS}$) and Lower Data Strobe ($\overline{LDS}$) select the byte to be accessed. In the case of a word access, both $\overline{UDS}$ and $\overline{LDS}$ are asserted going low simultaneously. In the case of a write cycle, the Read/Write (R/$\overline{W}$) signal goes low before the data strobes. The microprocessor now waits for the read or write operation to be completed. When the operation is completed, the memory signals this to the microprocessor by pulling the Data Transfer ACKnowledge ($\overline{DTACK}$) line low. If no memory is available at the specified address, an external logic is usually used to activate the Bus ERRor line ($\overline{BERR}$).

The MC 68010 supplies three additional signals, named function codes FC0, FC1 and FC2, to better describe the type of the bus cycle performed: instruction fetch, data read or write in both user and supervisor modes or interrupt acknowledge. Function code signals have to be decoded together with the address lines A1 to A23 to select devices tied on the bus.

The MC 68010 accepts seven different interrupts with differing priorities. The highest priority interrupt is not maskable (NMI) while the other interrupt levels can be inhibited by setting bits in the status register. The seven interrupt requests are decoded from three input lines: $\overline{IPL0}$, $\overline{IPL1}$ and $\overline{IPL2}$, to reduce the number of pins on

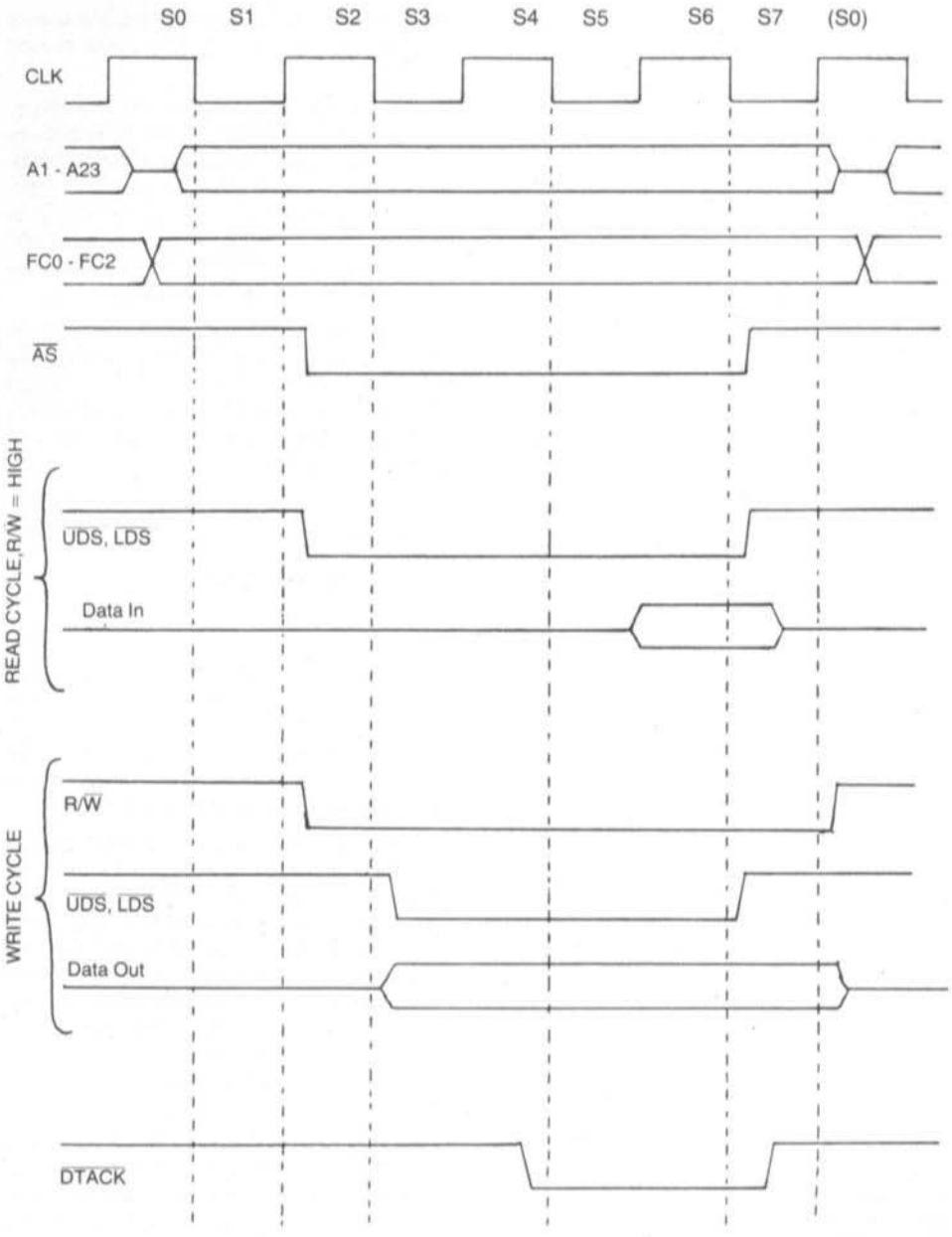

Fig. 2.1.: MC 68010 bus cycle timing

C		A
GND	1	GND
D4	2	D 5
D3	3	D 6
D2	4	D 7
D1	5	D 8
D0	6	D 9
$\overline{AS}$	7	D10
$\overline{UDS}$	8	D11
$\overline{LDS}$	9	D12
R/$\overline{W}$	10	D13
$\overline{DTACK}$	11	D14
D15	12	A23
A22	13	A21
CLK	14	A20
$\overline{HALT}$	15	A19
$\overline{RESET}$	16	A18
A17	17	A16
$\overline{VPA}$	18	A15
FC2	19	A14
FC1	20	A13
FC0	21	A12
A1	22	A11
A2	23	A10
A3	24	A 9
A8	25	A 7
A6	26	A 5
A4	27	$\overline{INT7}$
$\overline{INT6}$	28	$\overline{INT5}$
$\overline{INT4}$	29	$\overline{INT1}$
$\overline{MR}$	30	$\overline{INT2}$
+ CMOS	31	$\overline{INT3}$
+ 5 V	32	+ 5 V

Fig. 2.2.: Bus connections on a Eurocard connector

the microprocessor package. An external priority encoder (usually 74LS148) is required in most applications.

CLOCK is obviously required by the microprocessor itself. $\overline{RESET}$ and $\overline{HALT}$ are both inputs: to reset the microprocessor, and outputs: to reset the peripherals under program control and signal a double bus error. Additional control lines include an interface for the slow 6800 series peripherals ($\overline{VPA}$, E, $\overline{VMA}$) and bus request lines for DMA ($\overline{BR}$, $\overline{BG}$, $\overline{BGACK}$).

Most of the microprocessor signals are brought to the computer bus without using bufffers. The latter are placed on the inputs of the various modules to reduce bus loading. The actual bus connections on a 64 pole "Eurocard" connector are shown in **fig. 2.2.**

2.3. PROCESSOR BOARD

The processor board includes the MC 68010 chip and corresponding support circuitry, up to 32 kbytes of EPROM containing the operating system, 64 kbytes of nonvolatile RAM and the real-time calender/clock. The corresponding circuit diagram is shown in **figs. 2.3. and 2.4.**

The microprocessor support circuits include a clock generator, a bus-error timer, an interrupt-request priority encoder, an interrupt autovector logic, a reset logic and an address decoder for the remaining on-board devices. The clock generator is a simple crystal oscillator built around a CMOS (HC) gate, since there are no special requirements regarding its accuracy. The nominal clock frequency is 10 MHz. Additional HC gates are used to buffer the oscillator output.

The bus-error timer monitors the $\overline{AS}$ signal. In the case of a bus-error no device will answer with a $\overline{DTACK}$ or $\overline{VPA}$ to terminate the bus cycle and the $\overline{AS}$ could remain low indefinitely. However, the $\overline{AS}$ is also used to reset the bus-error timer. If the $\overline{AS}$ remains low for more than 192

clock cycles, the bus-error timeout counter (LS 393) will assert the $\overline{BERR}$ signal commanding the MC 68010 to call the bus-error handling routine.

The interrupt-request priority encoder is simply a LS 148 with pull-up resistors on its active-low inputs, so that more devices requesting the same level interrupt can be simply wired-on. The MC 68010 is used in the autovector mode. The latter is invoked by decoding the interrupt-acknowledge function code (all three FC outputs at logical high) and asserting the $\overline{VPA}$ signal.

The MC 68010 microprocessor is reset when both $\overline{RESET}$ and $\overline{HALT}$ lines are pulled low simultaneously for a sufficiently long period of time – at least 10 clock cycles during normal operation but at least 100 milliseconds after power-up. The reason for this long power-up reset time is easily explained since the MC 68010 is a dynamic NMOS circuit internally. The delay of 100 ms is required for the internal on-chip substrate bias-generator to achieve its full output voltage of about – 3 V. The Main Reset signal ($\overline{MR}$), supplied from the power-supply module, is applied through open-collector gates to both $\overline{RESET}$ and $\overline{HALT}$.

The MC 68010 $\overline{RESET}$ pin can also be an open-drain output, activated when executing the RESET instruction. The latter will not reset the microprocessor but will drive the $\overline{RESET}$ pin low for 124 clock cycles. This signal is made available on the computer bus and is used to reset all peripheral devices.

On the other hand, the $\overline{HALT}$ pin is driven low when a double bus-error is detected after a software crash or hardware failure. A double bus-error blocks the MC 68010 to avoid damaging the memory content allowing subsequent trouble-shooting. After a double bus-error a reset is required to restart the MC 68010.

The address decoder is used to select the on-board memories and peripherals, decoding the most significant address lines and to answer with a $\overline{DTACK}$ or a $\overline{VPA}$ signal. The nonvolatile CMOS RAM requires an additional decoder chip (HC 138) which receives the same battery-backed supply voltage as the RAM itself. The decoder is inhibited by the $\overline{MR}$ signal to protect the RAM content during power-up or power-down.

A single 8 bit wide EPROM is used to store the operating system software. An 8 bit latch (LS 374) and a sequence generator (LS 164) are used to generate a 16 bit data word for the MC 68010. Since this sequential 8 + 8 bit read operation is slow, the software is copied into the on-board system RAM immediately after reset. Once in the RAM, the software can be executed at full speed with no processor wait states.

The lower 16 kbytes of the on-board system RAM are assigned to the stack by the present software. In the case of a software crash it is usual for the stack to grow in an uncontrolled way. Therefore the locations immediately below the stack area are not assigned to any device so that an uncontrolled stack growth ends in a double bus-error safely blocking the MC 68010.

A 71055 parallel I/O port (fast CMOS version of the popular 8255) is used to interface the keyboard and the real-time clock chip. The parallel keyboard output is connected to port A, configured as a strobed input. Port B is a spare output. The remaining bits of port C are used both as inputs and as outputs to interface the 4990 real-time clock chip. The latter has serial inputs and outputs. Clocks and other signals are generated by software.

The 4990 Chip Select (CS) input is driven by the $\overline{MR}$ signal to protect the clock count during power-up or power-down for the same reason as the nonvolatile RAM. The 4990 has an on-chip open-drain interrupt output, while the keyboard interrupt, generated inside the 71055, requires an additional transistor. Current software requires the clock interrupt on $\overline{INT1}$ and the keyboard interrupt on $\overline{INT7}$, selectable through jumpers on the printed circuit board.

2.4. VIDEO BOARD

The video board includes 128 kbytes of special, dual-port video RAM, video D/A converter and

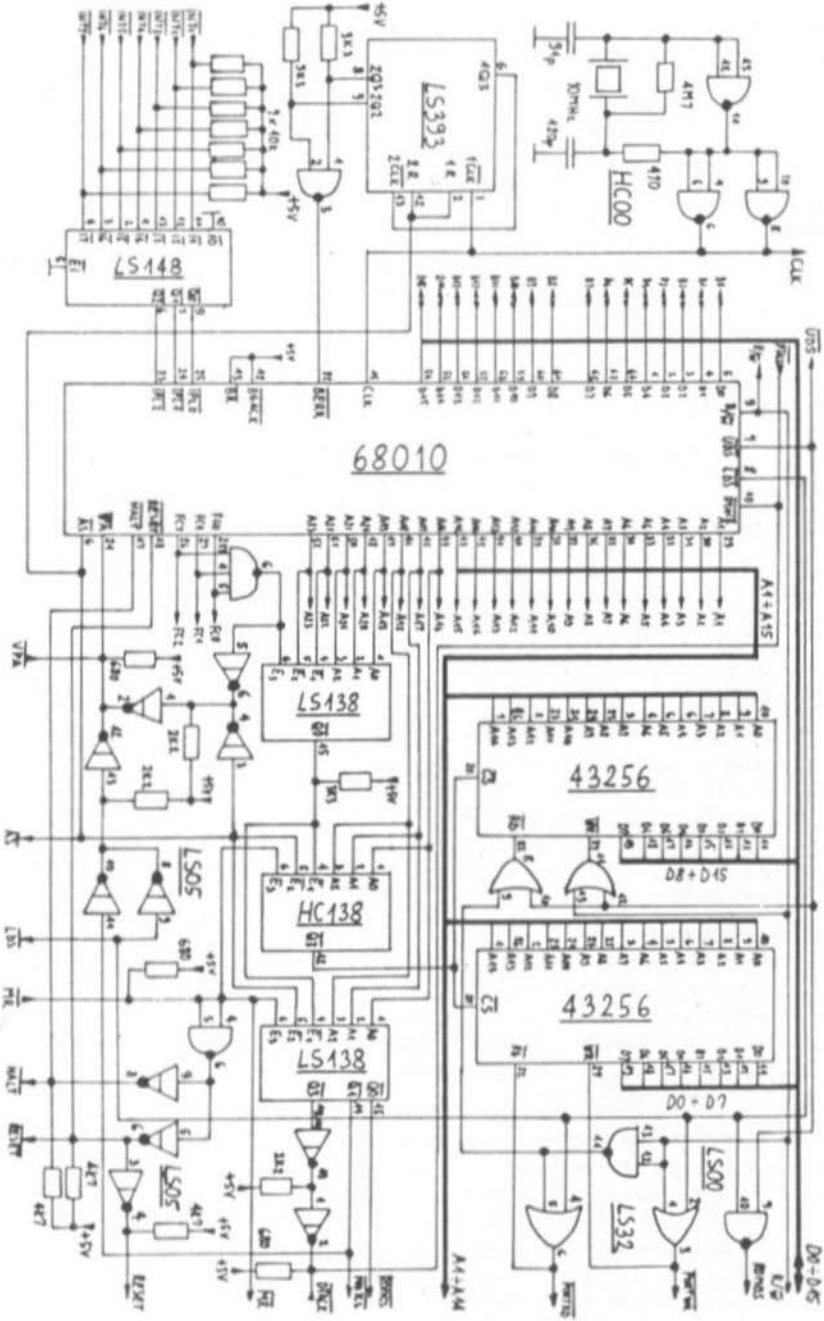

Fig. 2.3.: CPU board circuit diagram (YT 3 MV 004), part 1

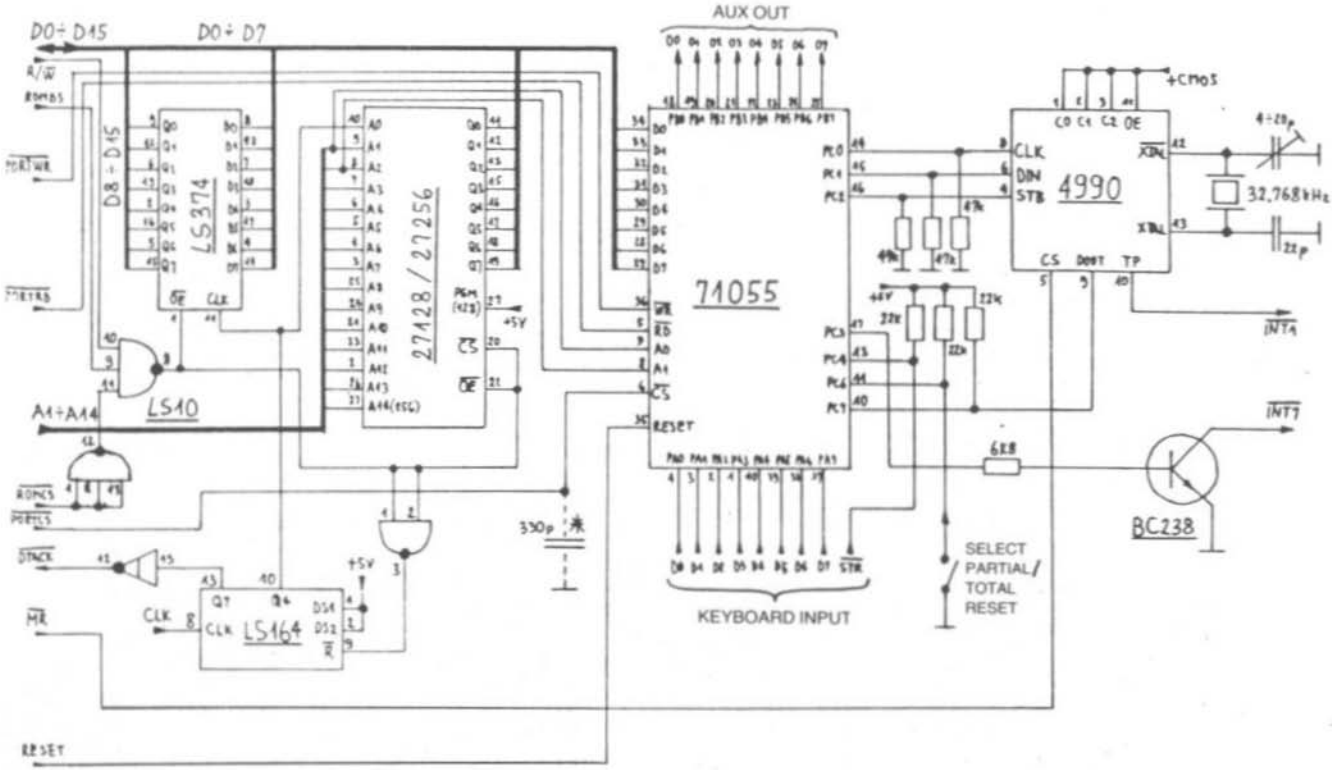

Fig. 2.4.: CPU PC-board YT 3 MV 004, part 2

timing and interface circuits. The circuit diagram of the video board is shown in **figs. 2.5. and 2.6.**

The memory used in a video interface is being read continuously to update the picture displayed on a CRT several times per second. If a microprocessor has to access the same memory, for example to update the picture, it can either wait for the horizontal or vertical retrace period or interrupt the display read operation disturbing the picture. General purpose dynamic or static memories are usually not fast enough to provide data for a high resolution video signal generation and be accessed by a fast 16 bit microprocessor at the same time. On the other hand, true dual-port memories with two completely independent access ports are both difficult to manufacture and expensive.

A few years ago, semiconductor manufacturers invented an alternative solution to increase the data rate from a dynamic memory built using only conventional DRAM chip technology. During any random access read or write operation, inside a dynamic RAM, a whole row of data (1024 bits in a 256 kbit RAM) is transferred from its storage cells to as many refresh amplifiers. This data can not be transferred quickly only because it is completely impractical to build an IC housing with so many pins. However, this data can be transferred to another circuit efficiently if the latter is located on the same semiconductor chip.

Dual-port dynamic memories include on-chip an additional shift register. A whole row of bits can be transferred from the main memory array to the auxiliary shift register in one single operation, called a data-transfer cycle and lasting no more than an ordinary data-access cycle. After such a data-transfer cycle the dynamic memory circuits and the shift register are completely independent: the microprocessor can randomly access the data in the main memory array (with no timing penalties) while other data is shifted out of the auxiliary register to generate the video signal.

Since dual-port video memories are only slightly more expensive than conventional dynamic RAMs, they are very attractive for any new video memory design. A data-transfer cycle usually has to be performed once every television line, i.e. once every 64 microseconds and it takes less than 1 % of this time. The memory is therefore available to the microprocessor for more than 99 % of the total time with no delays or disturbs to the generated video.

The described video board uses four 41264 chips which are organized as 64 k by 4 bits each. From the microprocessor side the video memory is organized as 64 k 16 bit words, from the video side there are 128 k pixels, arranged in 256 lines of 512 pixels each and the intensity of each pixel is described with 8 bits or 256 possible grey levels. Each 41264 chip also has four 256 bit shift registers that are all loaded in a single data-transfer cycle occurring during the horizontal retrace period. During the active scanning period, data is retrived alternately from two shift register groups so that the position of the 512 pixels obtained matches the microprocessor byte address ennumeration, simplifying and speeding-up the software.

All the timing of the generated video signal is derived from an on-board 12 MHz crystal oscillator, which drives a divider chain. The line period matches the standard TV line period (64 μs). One TV line consists of 768 pixels; two thirds (512 pixels) represent the useful scan and the remaining third (256 pixels) is left for the horizontal retrace and black edges at both picture sides. The number of lines in a TV frame is slightly larger than standard – a frame of 320 lines was selected for simplicity. To avoid flicker the scanning is not interlaced.

At the end of each useful scan period the video timing logic issues a request for a data-transfer cycle to obtain the data for the next television line. The request can not be granted immediately since the microprocessor may be using the memory at the same time. All dynamic memories are very sensitive to correct timing – any incorrect timing acces cycle disturbs the refresh operation and destroys immediately at least one whole row of data!

The data-transfer cycle request is therefore passed to an arbitration logic, built around a double JK-FF (LS 112). The arbitration circuit decides who has priority to access the memory, allowing the device currently accessing the

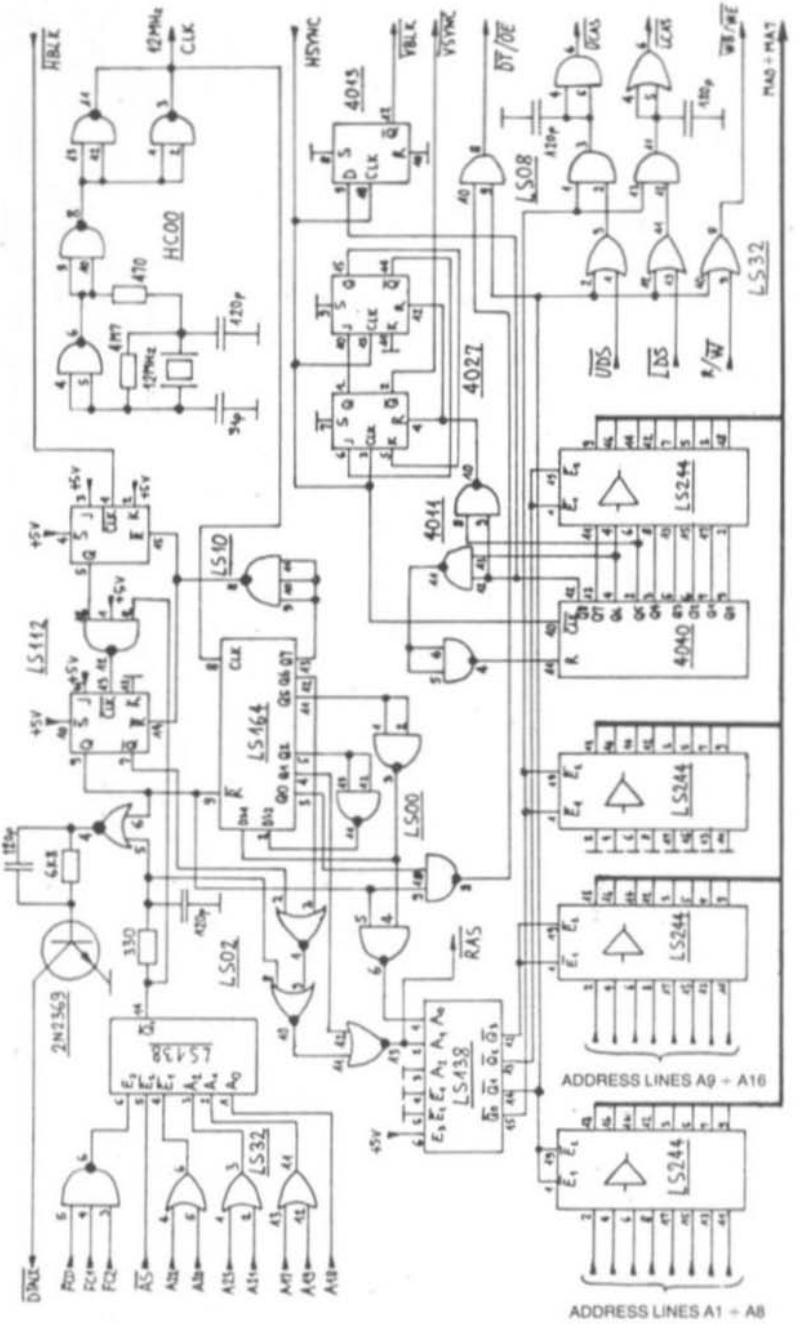

Fig. 2.5.: The video PC-board YT 3 MV 005, part 1

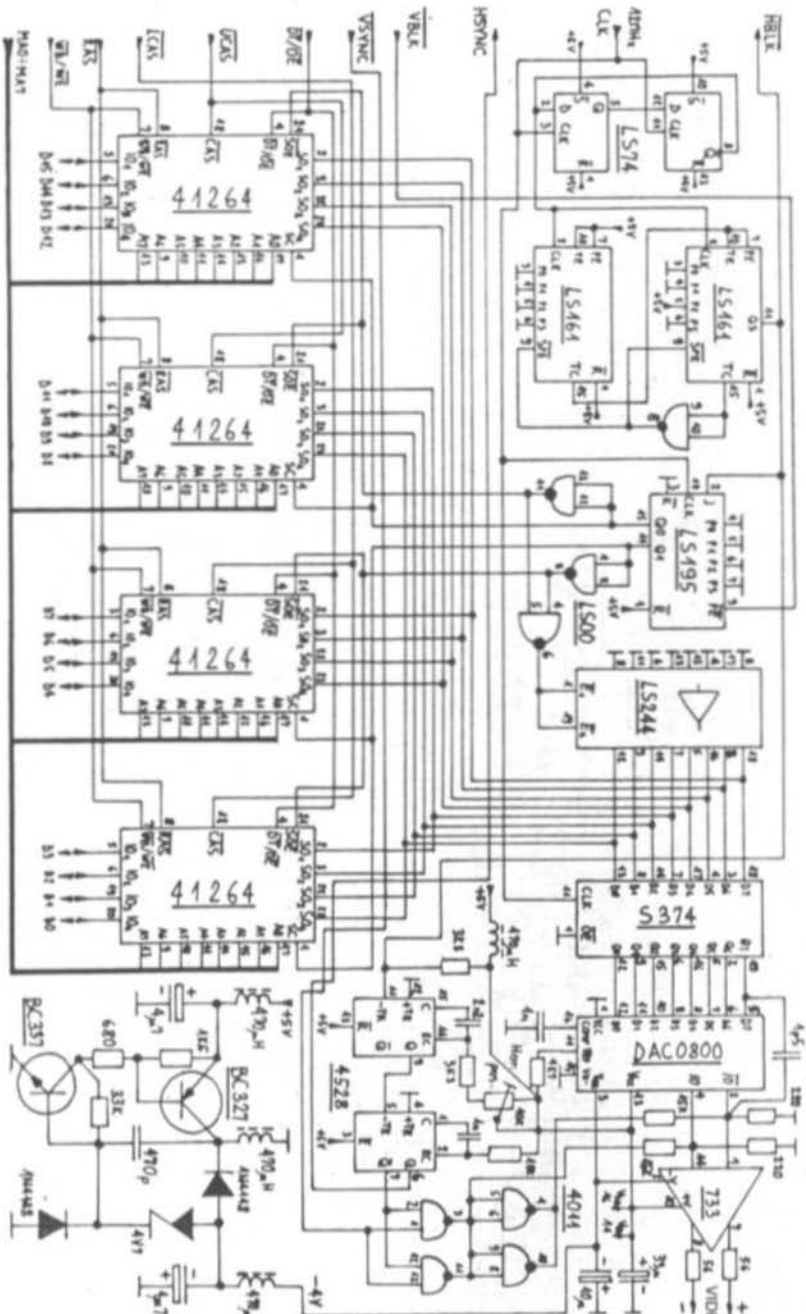

Fig. 2.6.: The video board circuit diagram (YT 3 MV 005), part 2

memory to complete the cycle in a regular way. In the worst case, the microprocessor has to wait for one complete data-transfer cycle or the video timing logic has to wait for one microprocessor bus cycle.

The data-transfer cycle timing is generated by a sequential logic with an 8 bit shift-register (LS 164) and corresponding gates. Like all dynamic memories, the 41264 require $\overline{RAS}$ and $\overline{CAS}$ clocks and address multiplexing. LS 244 tri-state buffers are used for both row and column address multiplexing and for switching the address lines between the microprocessor and the video timing logic. Since the microprocessor may want to access a single byte at a time, separate $\overline{CAS}$ clocks are derived from $\overline{UDS}$ and $\overline{LDS}$.

The 41264 video RAM serial outputs have tri-state capability and are simply tied in parallel for multiplexing. A fast 8 bit D-FF (S374) is however required to "clean" the data in front of the video D/A converter. During both horizontal and vertical retrace periods, all the 8 data lines are held low (black level) by a tri-state buffer (LS 244).

Sync pulses are added to the output of the D/A converter. The horizontal sync pulse is generated by a dual monostable and its position can be adjusted to match the monitor used. The vertical sync pulse is generated by a dual FF, it is two line periods long and occurs 32 lines after the end of the useful picture scan.

A 733 video amp is used to boost the generated video signal level. Both polarities are available to drive any type of standard-scan TV monitor. Both the D/A converter and the video amplifier require a negative supply voltage of about – 4 V that is generated on-board. All supply voltages of the analog part of the circuit are to be well-filtered to avoid disturbs in the video signal.

2.5. MEMORY

For most application programs, especially those handling pictures, the computer requires much more memory than the 64 kbytes provided on the processor board. Out of the MC 68010 16 Mbyte addressing range the current operating system uses the first megabyte for various system functions: start-up ROM, stack, video memory and I/O port addresses. The remaining 15 Mbytes are intended for memory expansion.

The circuit diagram of a 256 kbyte nonvolatile memory board is shown in **fig. 2.7.** The circuit includes eight 256 kbit CMOS RAMs 43256, address and data buffers to decrease the capacitive loading of the computer bus and an address decoder. The start address of the 256 kbyte block can be selected to start anywhere from address 200000H to 3C0000H positioning an on-board jumper.

The 43256 memory chips only have an active-low chip-enable input. To preserve the memory content when the computer is switched off, the chip-enables have to be kept high. This requirement can be met easily using a CMOS (HC) address decoder (HC 138) supplied from the same rail as the memory chips. The address decoder has an active-high input tied to $\overline{MR}$ to protect the memory content.

In a typical system, 4 such memory boards are used for a total 1 Mbyte nonvolatile memory. The latter is enough for most DSP applications and for some simple image processing. Due to bus loading problems it is difficult to connect more than 4 memory boards without sacrifying the operating speed. Of course as soon as higher-density memory chips become available, the described memory boards will be replaced by a higher capacity memory.

2.6. ANALOG I/O

An important part of any DSP computer is its interface to the analog world. As already described in the theoretical part, I decided to use a telephone CODEC IC as the A/D and D/A converter, since its performances match those of voice grade communications receivers and transmitters, including radio-

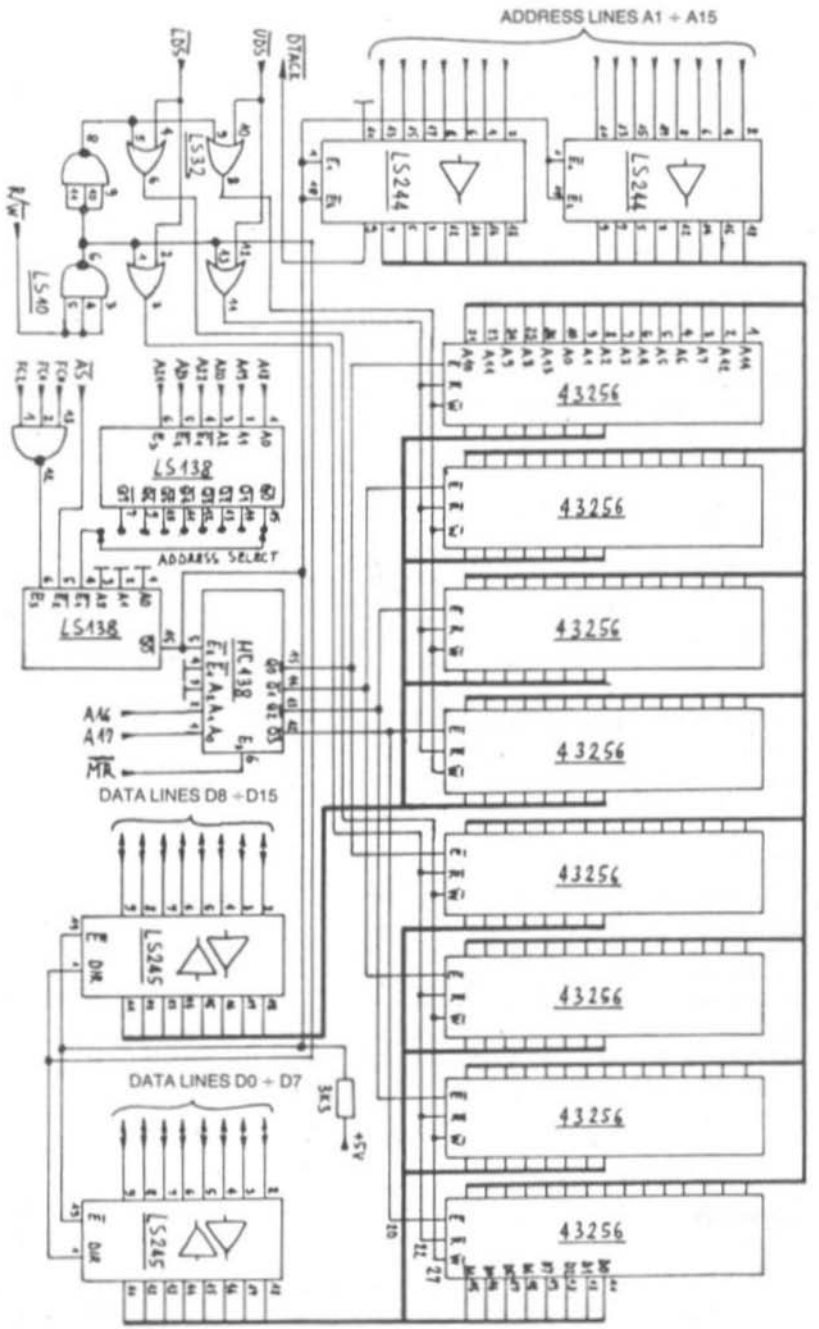

Fig. 2.7.: 256 k CMOS memory PC-board YT 3 MV 006

amateur receivers and transmitters. Since all CODECs have on-chip a serial data interface, a UART is required to interface a CODEC to a microprocessor. Programmable counters are used to generate the A/D and D/A sampling rates.

The analog I/O board also includes an independent RS-232 interface. The circuit diagram is shown in **figs. 2.8. and 2.9.** The RS-232 UART (71051), the programmable counters (71054) and the UART to interface the CODEC (another 71051) are all standard 8 bit microprocessor peripherals. To interface the faster MC 68010 bus, a timing logic built around a 4 bit shift register (LS 195) is required. The logic is started whenever any of the three on-board peripheral chips are selected by the address decoder (two LS 138), generating a longer Read ($\overline{R}$) or Write ($\overline{W}$) pulse and finally terminating the bus cycle by issuing a $\overline{DTACK}$ to the MC 68010. All three peripherals are connected to the lower byte (D0 to D7) of the 16 bit data bus through a bidirectional buffer (LS 245) to reduce the capacitive bus loading.

The RS-232 UART is equipped with a standard RS-232 receiver (75154). A 4053 CMOS multiplexer is used to generate RS-232 compatible transmit signal levels out of the + 5 V and − 5 V supplies available on-board. The RS-232 UART generates both receive (RX buffer full) and transmit (TX buffer empty) interrupts, connected through jumpers to $\overline{INT3}$ and $\overline{INT2}$ respectively. Both RX and TX clocks of the RS-232 UART are connected to a common programmable counter. The TX baud rate therefore can not be programmed different from the RX baud rate.

The CODEC UART has two separate programmable counters to generate the A/D and D/A sampling rates independently. Some additional logic, two 4029 counters and a few gates, are required to interface the MK 5156 CODEC. The A/D generated interrupt (new data available) is connected to $\overline{INT6}$, and the D/A interrupt (new data required) is connected to $\overline{INT5}$.

All the timing is derived from an on-board crystal oscillator at 6144 kHz. Some DSP programs, like the weather-satellite-picture receiving program, require a very accurate sampling frequency. The 6144 kHz clock is used by the UARTs, divided by 3 to obtain 2048 kHz required by the CODEC and switched-capacitor filter, divided by 2 to obtain 3072 kHz for the timing logic and divided by 4 to obtain 1536 kHz as the input to the programmable dividers. The divider-by-3 is a little more complex to obtain a nearly 50 % duty cycle at 2048 kHz.

To interface directly with analog circuits, receivers or transmitters, the CODEC analog input and output are connected to a switched-capacitor filter (TP 3040). The input audio signal is applied to a bandpass filter with a lower cut-off frequency of 300 Hz and an upper cut-off frequency of 3400 Hz before reaching the A/D converter. The D/A output signal is applied to a lowpass with a cut-off frequency of 3400 Hz.

Additional command lines are also provided, one input and two outputs. Their function is software programmable. The input is usually used as a squelch input (high means valid analog signal). The outputs are used as PTT and CW KEY commands to a transmitter. These two outputs are open-collector and active-low as required by most transmitters. The 75452 driver can handle 300 mA and 30 V on each of these outputs.

The CODEC, the switched-capacitor filter and the RS-232 driver require a negative voltage of − 5 V. The latter is obtained on-board with a simple two-transistor flyback inverter similar to that on the video board. The supply voltages of the analog circuits have to be further filtered to avoid any interference from the noisy computer bus + 5 V supply rail or inverter. The CODEC also requires two reference voltages. The positive reference is obtained from a red LED providing a stable voltage drop of about 1.8 V. The negative reference tracks the positive reference to avoid distortion using an op-amp (741).

2.7. FLOPPY DISK DRIVE

Although the operating system developed for my DSP computer does not require a mass memory like magnetic disks for its operation, it is very

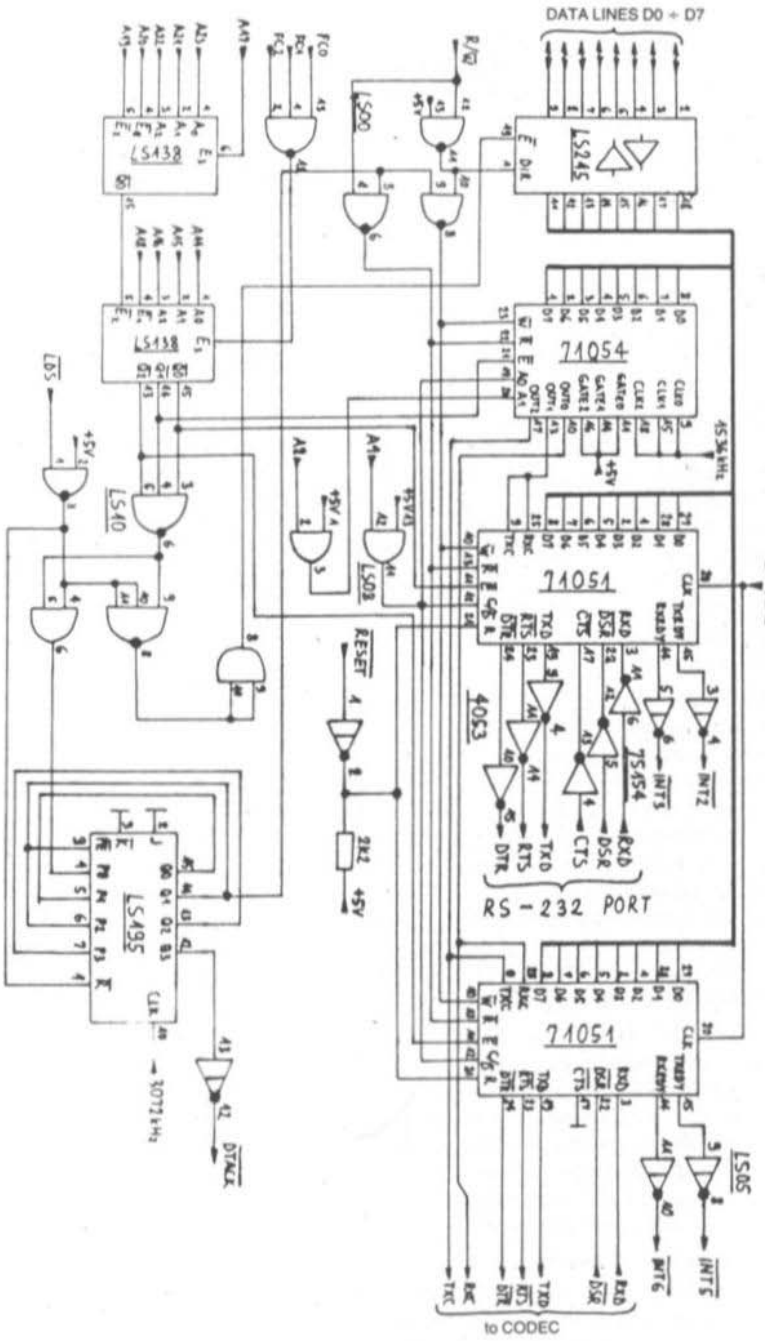

Fig. 2.8.: Analog I/O and RS-232 board circuit diagram (YT 3 MV 007), part 1

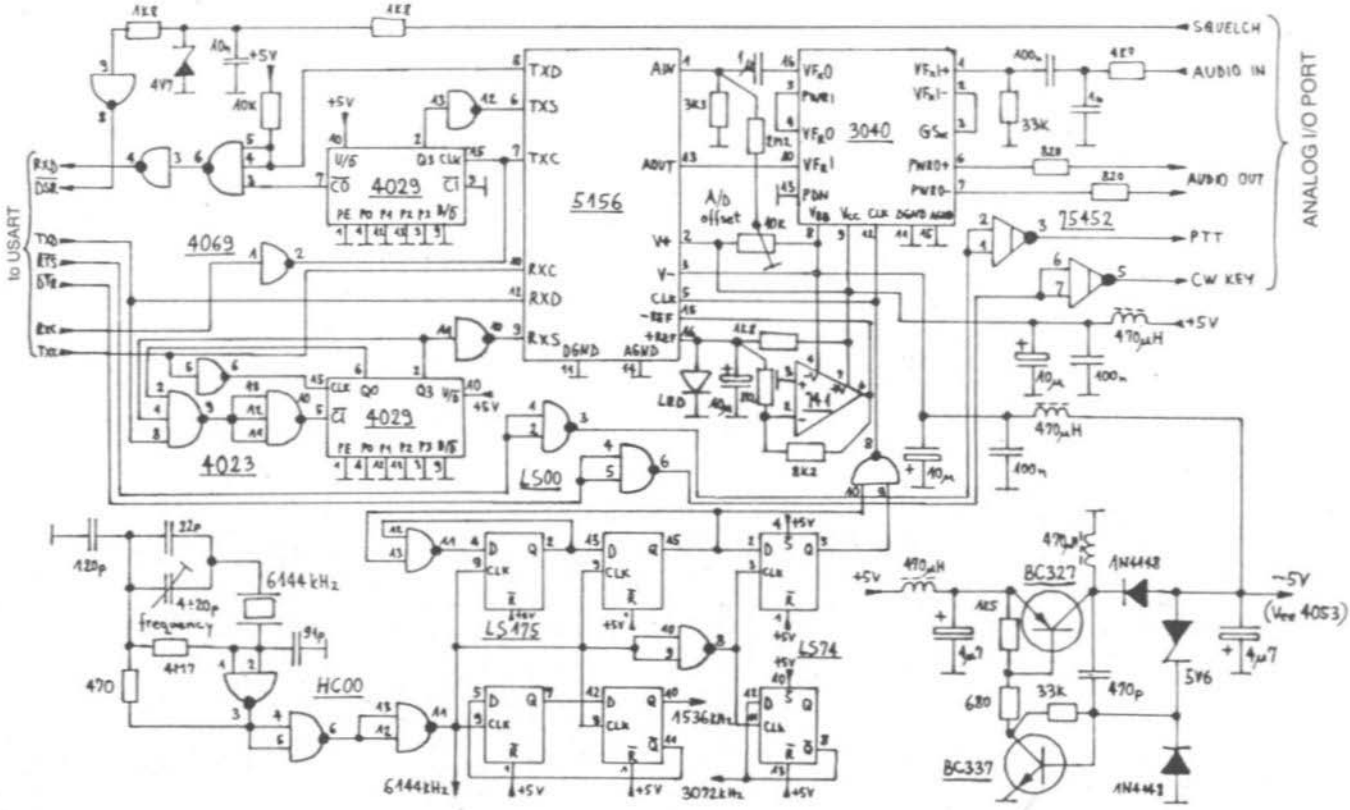

Fig. 2.9.: Analog I/O and RS-232 PC-board YT 3 MV 007, part 2

comfortable to have available a floppy drive. For example, applications programs can be loaded conveniently from a floppy disk for the first time, when initializing the system. Floppy disks are also useful for backup copies and to store large amounts of data for longer periods of time (pictures).

Building the mechanical part of a high-performance floppy drive is probably out-of-reach for an amateur. Available floppy drives come already with some electronics like write and read head amplifiers and motor drivers. Most of the recent floppy drives come with a 34 pole connector carrying TTL level signals in both directions. These signals are standardized. There are also many special purpose chips available, called Floppy Disk Controllers (FDC), to interface the standard "34 pole connector" signals to any microprocessor or DMA controller.

I selected to use 3.5" double-sided floppy disks on a 300 rpm drive at a recording speed of 250 kbps MFM. An 80 track double-sided disk has a raw capacity of 1 Mbyte. Each track has a raw capacity of 6.25 kbytes and the current software formats it into 5 sectors of 1024 bytes each, resulting in a formatted capacity of 800 kbytes per disk.

Floppy disk controllers come either in one chip or as a set of chips. The Western Digital 2797 is a single-chip FDC with an analog data separation PLL. New FDCs have digital PLLs that do not require adjustments, but the 2797 is cheap and easily available. To interface a standard 3.5" floppy drive, it only requires a few open-collector, high-current-sink TTL buffers.

The circuit shown in **figs. 2.10. and 2.11.** also includes some additional logic to make all of the 2797 functions selectable by software. The circuit to interface the slow 2797 to the fast MC 68010 bus is identical to that used on the analog I/O board. A simple high-speed serial interface, based on a 8530 Serial Communications Controller (SCC), is located on the same board.

The timing for the FDC and bus interface logic is derived from a 16 MHz crystal oscillator. Its frequency is divided down to either 1 or 2 MHz to drive the 2797 clock input in the write mode. In the read mode, the 2797 derives its clocks from an on-chip PLL with a VCO running at 4 MHz.

To maintain software compatibility with its predecessors, the designers of the 2797 chip could not implement all of its functions as control register bits. The corresponding selection pins have to be driven by an additional output port, in this case a LS 273 latch. Two outputs of the LS 273 are used to select the floppy drive directly, bypassing the 2797 chip.

3.5" floppy drives do not have a head load solenoid – the read/write heads are loaded immediately after the disk is inserted into the drive. To avoid unnecessary wear of the disk and heads, it is necessary to stop the spindle motor after read or write operations are completed. In the case of the 2797 FDC, its Head LoaD (HLD) signal has to be used as a Motor On (MO) signal for a 3.5" floppy drive. Correspondingly, the READY input of the 2797 can not be used and the READY output from the drive, if available, should be tied to the Head Load Timing of the 2797. The HLD output of the 2797 has an interesting feature: if not disabled by software it will be disabled automatically after 15 disk revolutions (3 seconds) following the last read or write operation. A software crash or a careless programmer will not destroy the disk nor damage the heads!

Some of the connections between the FDC and the 34 pole connector are brought to a jumper plug to adapt for small differences in the connections of different drives. The two 2797 interrupts, DRQ and INTRQ, are also connected through jumpers to $\overline{INT4}$ and $\overline{INT3}$ respectively.

The serial communications controller chip (8530) obtains all its timing from a 6144 kHz crystal oscillator, since this frequency can be divided to obtain standard baud rates. The serial port uses the same signal levels as the floppy drive interface: drivers are open-collector, high-current-sink TTL and receivers are simple TTL inputs with pull-up resistors. $\overline{INT6}$ is assigned to the SCC, again through a jumper, to handle the high data rates expected.

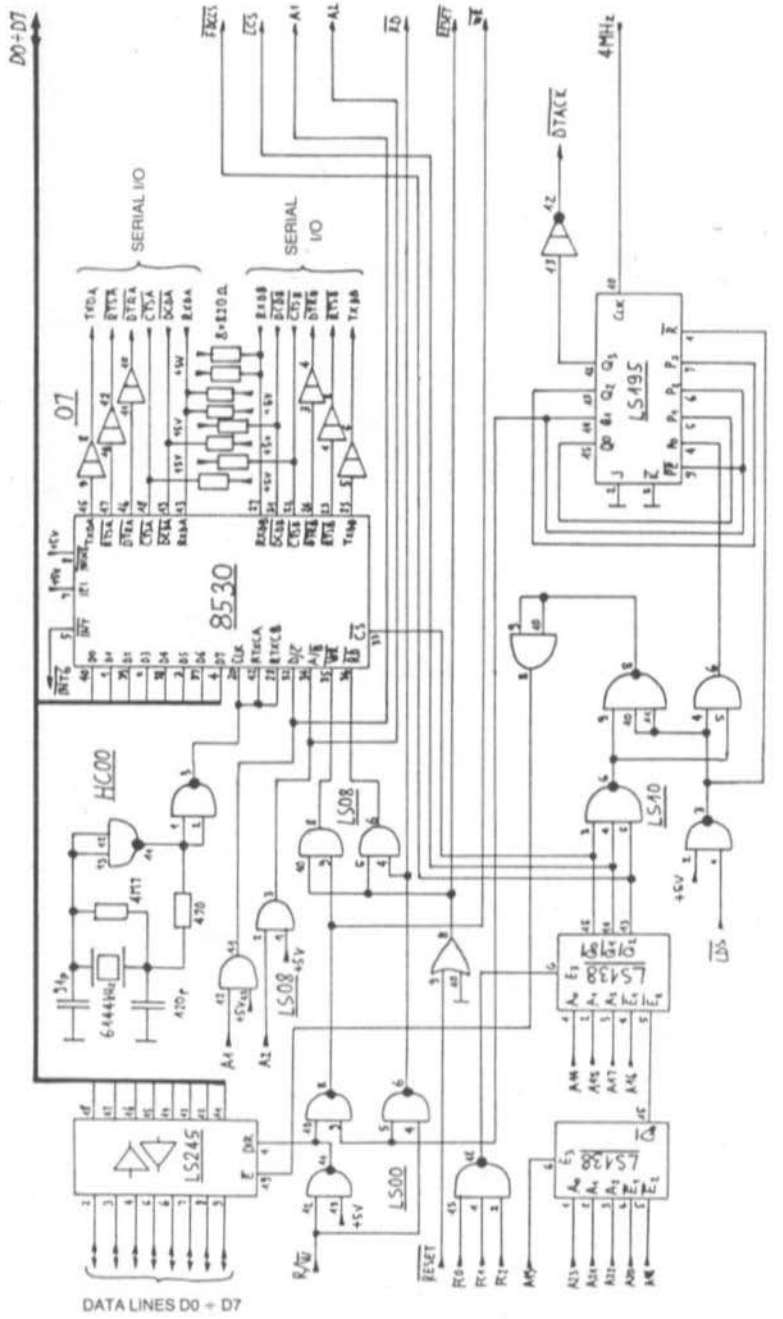

Fig. 2.10.: Serial I/O and floppy interface board circuit diagram (YT 3 MV 008), part 1

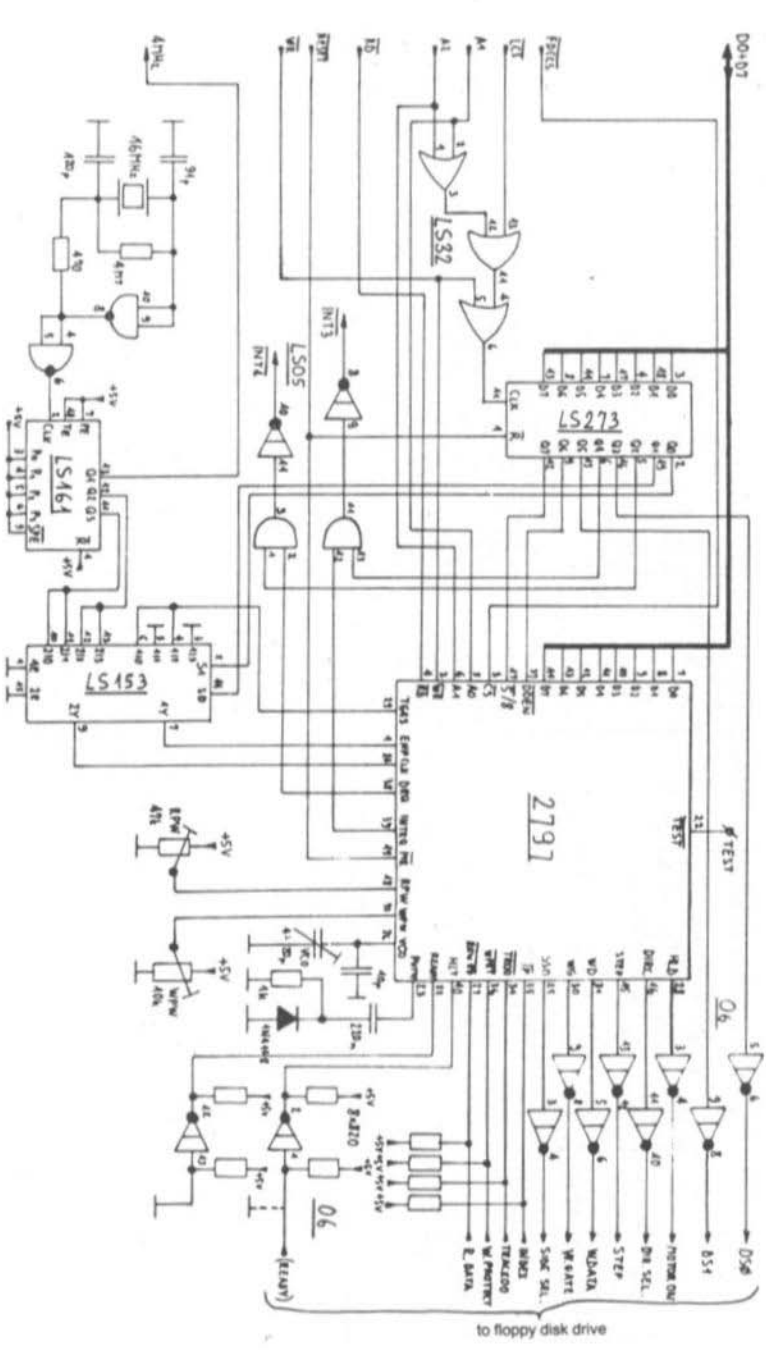

Fig. 2.11.: Serial I/O and floppy interface board circuit diagram (YT 3 MV 008), part 2

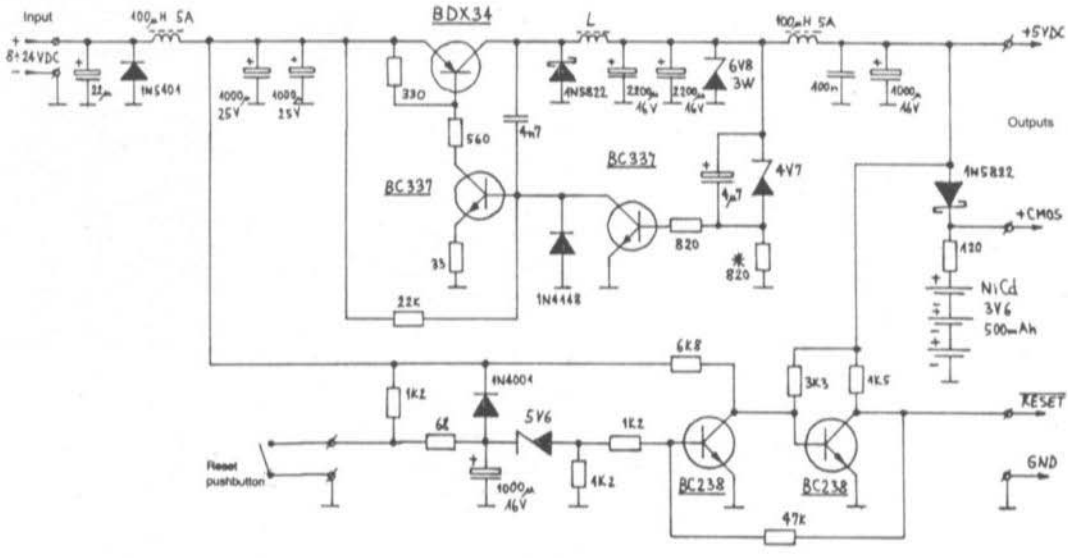

Fig. 2.12.: Power supply board circuit diagram (YT 3 MV 009)

2.8. POWER SUPPLY

Although the design of a power supply is not considered very important by most design engineers, power supplies are usually a major source of troubles in practical electronic circuits, especially computers! Overheating, electrical interferences and unreliable resetting are common problems associated with poorly designed computer power supplies.

A DSP computer is intended to operate together with other analog equipment including sensitive receivers and powerful transmitters. Efficient shielding is a must to avoid interferences in both directions. However, an efficient shielding enclosure is normally very poor from the thermal design point of view since computer chips dissipate most of the heat produced by convection cooling. While it may not be possible to influence the amount of heat produced in the computer chips, other heat sources can be avoided in a careful design. A good efficiency, switching power supply is a must!

The circuit diagram of the recommended power supply for the DSP computer is shown in **fig. 2.12.** The power supply is intended to operate from a non-regulated DC supply of nominally 12 V DC, negative grounded, like most other radio-amateur equipment. The efficiency of the simple series switching regulator is above 80 %. Chokes at both input and output are used to suppress both interferences generated by the computer and by the switching regulator itself.

The power supply module includes a 3.6 V, 500 mAh NiCd battery for clock and memory back-up.

The reset circuit is an integral part of the power supply, since it is very difficult to derive the information to operate a reset circuit just from the + 5 V rail on the computer bus. The $\overline{\text{RESET}}$ signal will be applied immediately after the input voltage falls below about 6.5 V. The series regulator is still operating correctly at this input voltage and the $\overline{\text{RESET}}$ signal will effectively protect the vulnerable content of the non-volatile RAM. If the

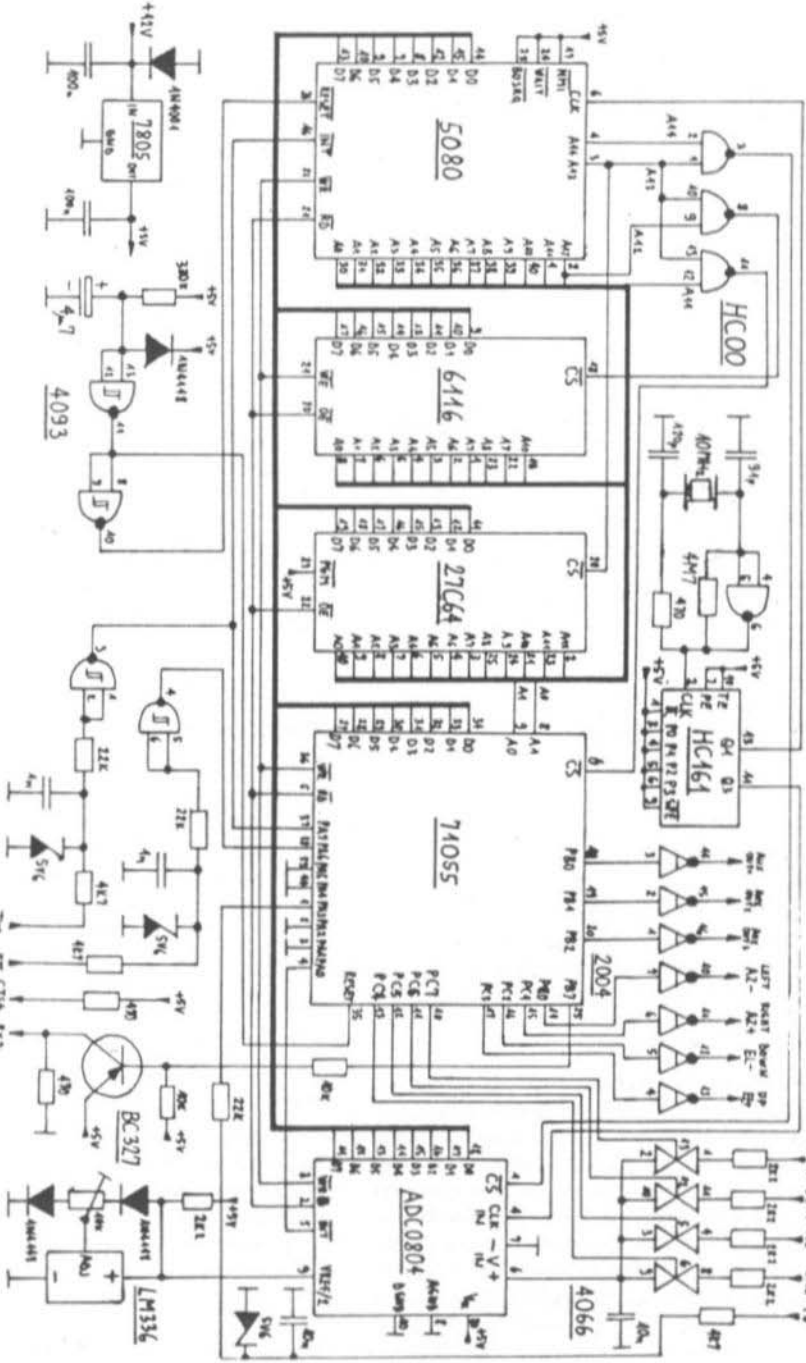

Fig. 2.13.: KR-5600 rotator interface circuit diagram (YT 3 MV 0010)

input voltage falls down to zero, the $\overline{\text{RESET}}$ signal remains active, since it is active-low.

When the input voltage is applied again, the $\overline{\text{RESET}}$ will only be removed after the input voltage goes above about 7 V (hysteresis of about 0.5 V) and after the delay introduced by the 1000 μF/1.2 kΩ time constant. Everyday practical use confirmed that this resetting/protection scheme is failure-proof regardless of the kind of transients on the power line, in severe contrast to what happens with commercial computers, packet-radio TNCs or other equipment using microprocessors!

Since there are just four wires connecting the power supply module to the computer bus: + 5 V, + CMOS, $\overline{\text{MR}}$ and GND, the module is not equipped with an "Eurocard" connector to avoid capacitive loading of the computer bus.

2.9. ANTENNA ROTATOR INTERFACE

Automatic satellite tracking with a steerable antenna system is usually required together with many DSP applications. The described DSP computer is able to generate the required tracking information as a background task to the main DSP task with a minimum additional loading of the CPU. Even in the case of up-dating the antenna pointing direction every second, only about 2 % of the total CPU time is required for the tracking program.

Due to the variety of different antenne rotator systems, I decided not to build any rotator interface inside the computer itself. The rotator interface, shown in fig. 2.13., accepts data from the computer RS-232 port and interfaces to a KR-5600 rotator control unit. It includes an 8 bit microprocessor 5080 (CMOS version of the Z80CPU) with an EPROM (27C64) and a RAM (6116), an A/D converter (ADC0804), darlington relay drivers (2004) and a simplified RS-232 port. Only a very small part of both the EPROM and the RAM are actually used since the software is very simple.

The rotator interface receives the desired antenna azimuth and elevation from the DSP computer. These values are compared with the actual values measured by the position-sensing potentiometers installed on the rotators. The interface microcomputer then decides to activate the motors in the appropriate direction. The software also corrects for the inertia of the rotator and antenna system. The damping coefficients are also up-loaded from the DSP computer. The interface also transmits a complete status report on request from the main computer.

All of the microcomputer components are CMOS versions to keep the current drain low. The overall current consumption of the interface is only about 35 mA. The latter can be derived from the multipole connector on the KR-5600 control unit thus saving the expense of an additional power supply. The interface requires just + 5 V obtained from a three-terminal voltage regulator. The A/D converter has its own 2.5 V reference LM 336. Since the computer memory content is lost after power-down, no special reset circuit is required, an RC network and a Schmitt-trigger gate are sufficient.

The RS-232 serial/parallel and parallel/serial conversions are done in software. Therefore, all the clocks are derived from a single crystal oscillator at 10 MHz – divided by 4 to obtain 2.5 MHz for the CPU and divided by 16 to obtain 625 kHz for the A/D converter.

A parallel I/O port (71055) controls the relay drivers, the analog multiplexer (4066) for the A/D converter and the RS-232 signals. The latter are not completely to the RS-232 specifications, since the output logical-low is only zero volts, but are accepted by most RS-232 receivers. With suitable software the interface could be used with any computer equipped with a RS-232 port.

2.10. FUTURE PLANS

A construction article is planned to follow, discussing also hardware check-out, soft-

ware installation and use of the DSP computer. Some information, like the operating system manual, can not be published since they would take far too much space in the magazine – copies will be made available separately. Software will probably be made available on floppy disks, including source files, their corresponding compiled versions and "manual" files describing how to use them.

There will certainly be many upgrades of both the hardware and especially the software. A very successful upgrade was the replacement of all LS-series TTL integrated circuits with the new HC-series. The HC-series integrated circuits, now available at the same price as the older LSs, offer a much lower current consumption (power dissipation!) and a lower bus loading. In addition, their constant, resistive output impedance efficiently suppresses bus ringing, allowing up to 30 % higher CPU clock frequencies.

The next imminent hardware upgrade is certainly a higher capacity memory board. Other peripherals could be built as well, including "intelligent" ones carrying maybe an even more powerful processor than the MC 68010 or a dedicated DSP chip. On the other hand, future antenna rotators will probably include an RS-232 interface and the described rotator interface board will probably become unnecessary.

Of course, most upgrades can be expected in the software. Several algorithms, including the Fast Fourier Transform, have not even been tried yet, although it is known they are possible on the described hardware.

Wolfgang Schneider, DD 2 EK

FM-ATV in the GHz Range
Part 1: 23 cm Transmitter

Owing to the advancing developments in the field of satellite television techniques, FM-ATV is becoming of increasing importance to the radio amateur. In addition to the use of ready-made industrial units, the modern semi conductors allow the home construction of complete FM-ATV transmitters and receivers, well into the GHz range, with the minimum effort. The following multipart article describes the construction of a transmitter/receiver for FM-ATV in the 23 cm band.

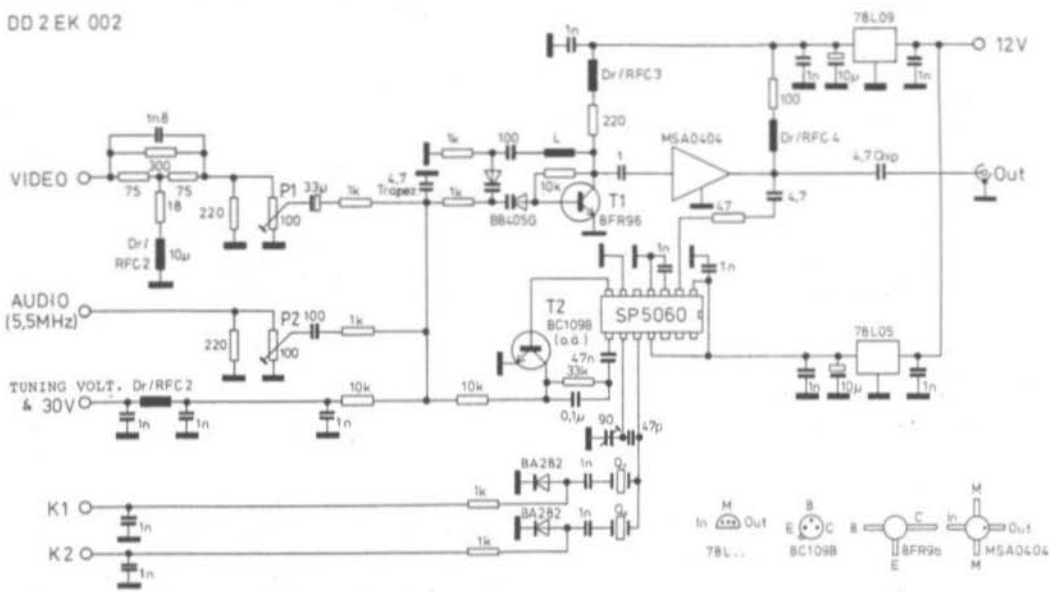

Fig. 1: 23 cm band FM-ATV transmitter

1. CIRCUIT DESCRIPTION

As may be seen from **fig. 1**, the 23 cm ATV transmitter displays no particular peculiarities. As may be expected, the heart of the transmitter may be regarded as the voltage-controlled oscillator (VCO) included in a phase-locked looped (PLL). This will now be examined in detail.

1.1. The Voltage-Controlled Oscillator (VCO)

The VCO (**fig. 2**) was developed using economical, but readily obtainable components. The varicap diodes are normal UHF types and the transistor is also a standard type.

The series resonant circuit comprises an inductor and two varicap diodes (BB405G) connected between the collector and the base of the oscillator transistor. A 100 pF capacitor serves to isolate the varicaps from the DC collector voltage but at the same time its connecting lead forms the series tuning-inductance. Other connections are kept as short as possible in order to prevent the introduction of uncontrolled reactances into the circuit.

The control of the transistor's working point and its quiescent current is achieved by the 10 kΩ resistor between collector and base and the 220 Ω resistor in the collector. A small inductance in series with the collector resistor prevents the tuned circuit from being loaded and ensures complete decoupling from the supply voltage.

The VCO, as described, is capable of working at 2.2 GHz. The inductor formed from the lead of the 100 pF capacitor determines the resonant frequency of this circuit. In the interesting frequency range around 1.2 GHz, a 0 - 24 volt tuning voltage will enable a spectrum of 500 MHz to be covered! An output power of about 12 mW is obtained at 1 GHz and 5 mW at 1.5 GHz (**fig. 3**).

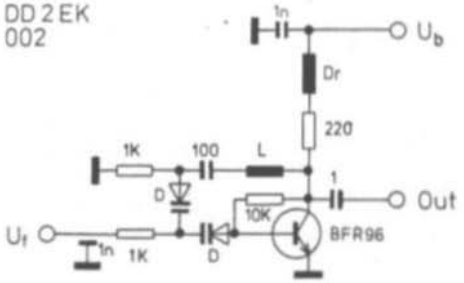

Fig. 2: The voltage-controlled oscillator

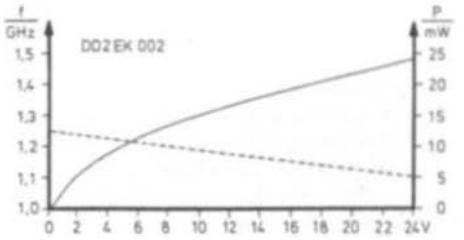

Fig. 3: The VCO frequency and the output power (dotted line) as a function of the tuning voltage

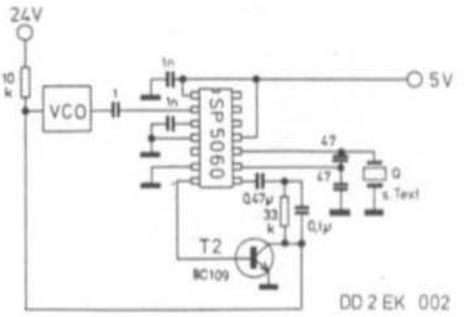

Fig. 4: The phase-locked loop

1.2. The Phase-Locked Loop

The SP 5060 forms, together with the VCO, a complete PLL frequency synthesizer (**fig. 4**) which is usable over the range 300 MHz to 2 GHz. The integrated circuit contains a pre-scaler together with a pre-amplifier and a frequency divider. The latter has a fixed division factor, the ratio between the synthesizer and the reference frequency being 256 : 1.

The phase comparator is supplied with an external, quartz-derived, reference frequency. The output of the comparator controls the varicap diode in the VCO via an external transistor (BC 109 or equiv.).

Owing to the fixed division factor in the SP 5060's divider, the reference frequency is obliged to be exactly a 256th of the synthesizer frequency. This means that for a desired output frequency, say 1270 MHz, a reference frequency of 1270/256 = 4.9609375 MHz is required.

2. CONSTRUCTION

The printed circuit board for the circuit described above, is constructed on a double-sided, 1.5 mm thick, epoxy-glass material and of dimensions 72 x 72 mm (**see fig. 5**). It fits into a proprietary tin-plate box 74 x 74 x 30 mm.

After trimming the board to size, it is cleaned and coated with rub-on silver plating – although this is not absolutely necessary. Then it is drilled. The broadband amplifier is fitted into a suitably cut hole in the board. Also, a slot (1 x 8 mm) is provided, at the appropriate place at the edge of the board, in order to accommodate the BNC socket inner connector spigot.

The board is then drilled for the other components; resistors, capacitors, the crystal etc. Care must then be taken to provide a countersink (using a 2.5 mm drill) around the ungrounded leads on the ground-plane, i.e. component side of the board, in order that the component leads are not inadvertently shorted to earth.

After this work is finished, the board can be treated with flux solution.

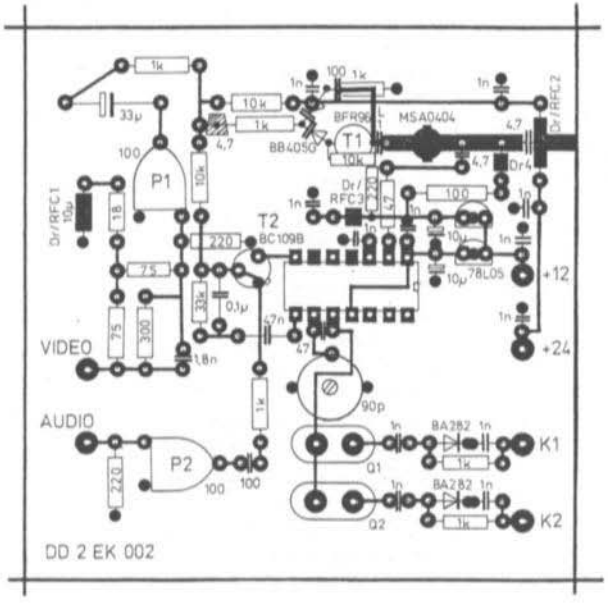

Fig. 5:
The tracks and components of the double-sided PCB DD 2 EK 002 for the circuit diagram of fig. 1

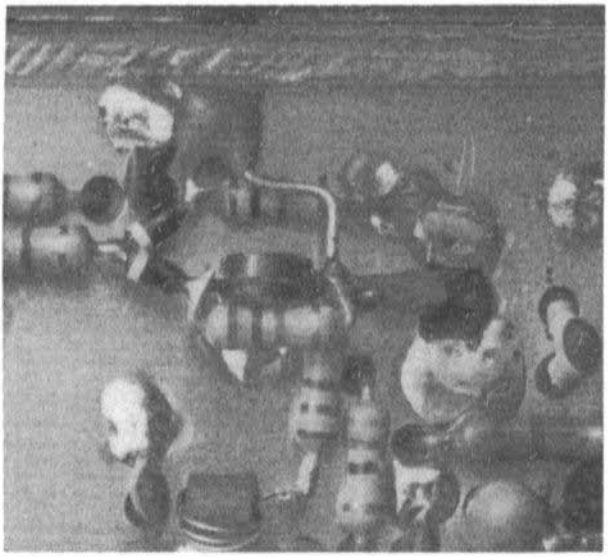

Fig. 6:
The VCO showing the self-supporting-in-air component mounting

When the board is dry, the through-plating contacts can be installed for the broadband amplifier IC. The BNC socket must be installed so that its flange fits to the appropriate place on the frame with its inner spigot in the slot provided on the PCB. The teflon shoulder on the socket may be removed with a sharp knife before mounting. Also, see to it that the module lid is not prevented from fitting when the crystal has been installed (think about this when the board is being soldered into its frame).

Following the correct soldering of the PCB into the box frame, the equipping of the board is carried out. The VCO is wired together "in air" (**see fig. 6**), the component leads being made as short as possible in order to minimize stray inductance effects. The series inductor in the VCO is formed from the collector-side lead of the 100 pF capacitor connected between base and collector of T 1. For the frequency of interest, about 1.2 GHz, this lead is trimmed to 9 mm and bent through 90°. This may be clearly seen in the photograph of fig. 6.

2.1. Components

1 BC109B, BC 413, BC 550 or equiv. low-noise NF types
1 BFR96
1 MSA0404 (Avantek)
1 SP5060 (Plessey)
1 78 L 09
1 78 L 05
2 Diode BB405G
2 Diode BA282
1 RFC 10 μH (Neosid)
1 6-hole ferrite core (Valvo)
2 RFC 4 turns 0.3 mm Cu-lac. wire on 3 mm ferrite bead
1 90 pF foil trimmer (red)
1 4.7 pF trapez. cap.
1 4.7 pF chip cap.
1 0.47 μF cap. (7.5 mm grid)
1 0.1 μF cap. (7.5 mm grid)
1 33 μF/35 V elko. (10 mm grid)
2 10 μF/16 V tant.
2 100 Ω preset pot. (10 mm grid)
1 100 Ω/0.3 W resistor
1 Tin-plate box 74 x 74 x 30 mm

1 BNC panel mounting socket UG290A/U
6 teflon feed-thro insulators

Ceramic disc capacitors (2.5 mm grid)
1 1 pF
1 4.7 pF
1 47 pF
2 100 pF
12 1 nF
1 1.8 nF

Resistors (fixed, 10 mm grid)
1 18 Ω
1 47 Ω
2 75 Ω
1 100 Ω
3 220 Ω
1 300 Ω
6 1 kΩ
3 10 kΩ
1 33 kΩ

Inductors see text.

Crystal
HC-18U or HC-25U (see text)

3. COMMISSIONING

The following test instruments should be available:

- Multi-purpose meter
- Frequency counter (to 1.3 GHz)
- Power meter (to 1.3 GHz)

Following the application of the 12 V supply voltage, the unit should immediately start

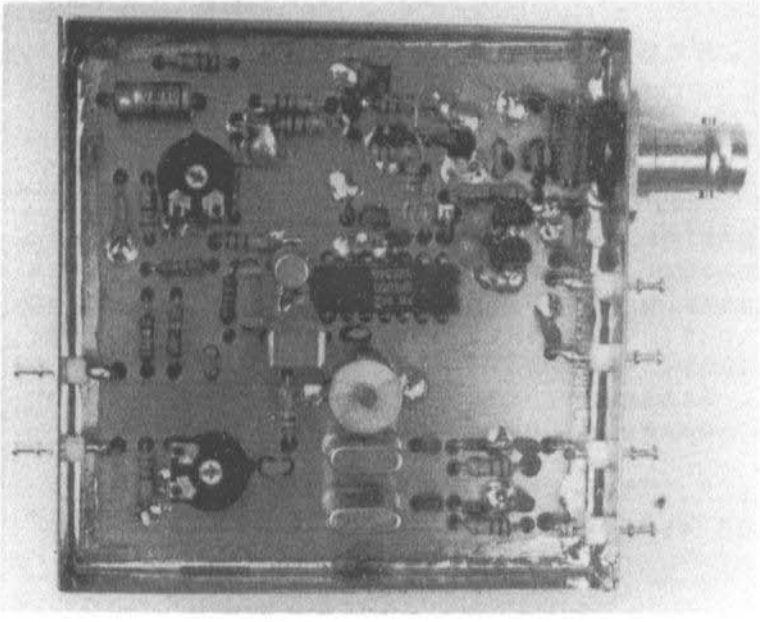

Fig. 7: The completed FM-ATV transmitter module

working, delivering some 20 mW to the power meter. The VCO, however, is not yet locked on to one of the two crystal-determined frequencies but is oscillating at its lowest frequency. The tuning voltage (max. 30 V) is now connected and one of the two crystals put into operation by applying 12 V to the appropriate point. The oscillator is now oscillating, locked at the desired frequency, and if not, it is working outside of the PLL's capture range. This may be corrected either by altering the inductance L or by an adjustment of the control voltage. A small test circuit, which will be described in the second part of the article, will produce an adjustable control voltage from the available 12 V supply voltage.

After the synthesizer has been set-up correctly, the video camera and a frequency-modulated, 5.5 MHz sound carrier can be connected and the unit put into operation. It only remains now to set the frequency deviation with the two preset resistors.

4. LITERATURE

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Andrew Bell, GW 4 JJW

Morse Code Generator for Microwave Applications

This single-sided PCB (fig. 2) generates a morse code modulated tone which can be fed into the modulator of a microwave transmitter. The morse code is stored in an EPROM and it takes about 20 minutes to scan through the entire EPROM at about 15 wpm. When the end is reached, scanning is restarted from the beginning of the EPROM. The theory is that periods of continuous tone or silence may be interspersed with morse code at will. The input to the board is + 12 volt and the output is a low-pass-filtered, morse code modulated audio tone.

1. CIRCUIT DESCRIPTION

I1, a 12-stage CMOS oscillator and divider, is set to oscillate at about 28 kHz by means of C 1 and VR 1 (**fig. 1**). Square wave audio is taken from pin 5 after a division by 32 to yield a frequency of about 880 Hz. After division of the original signal by 8192, the signal is passed on to the I2, a CD 4040, for 12 more stages of division. The results of the last 14 stages of division are taken from the counters and passed to the EPROM on its address lines. The EPROM will then step through about 14 addresses per second which represents a morse code speed of about 15 wpm. At any specific address if a data bit is found to be logical-one, a tone will be generated, otherwise a period of silence will follow. On the prototype (**fig. 3**) only bit-zero was used although provision has been made via a ten-way molex connector, J 1, to select any one of the 8-bits which emerge from the EPROM by means of a switch. The EPROM data bit, which is really a 'tone-enable' signal, is passed to I4, a CD 4011 NAND gate, where it is combined with the square-wave tone signal. The output is audible morse code. This is passed through a two-stage R/C filter to remove many harmonics and glitches caused by the slow propagation time of the counters. It then goes to a common drain JFET amplifier to convert the high output impedance of the filter to a much lower value. The function of R 4 is to reduce the amplitude of the audio signal. Finally VR 2 serves to vary the amplitude of the morse modulated audio signal which is AC-connected to the 4-way molex connector.

A power-on reset comprising R 5 and C 5 ensures that on power-up the EPROM address is set to zero.

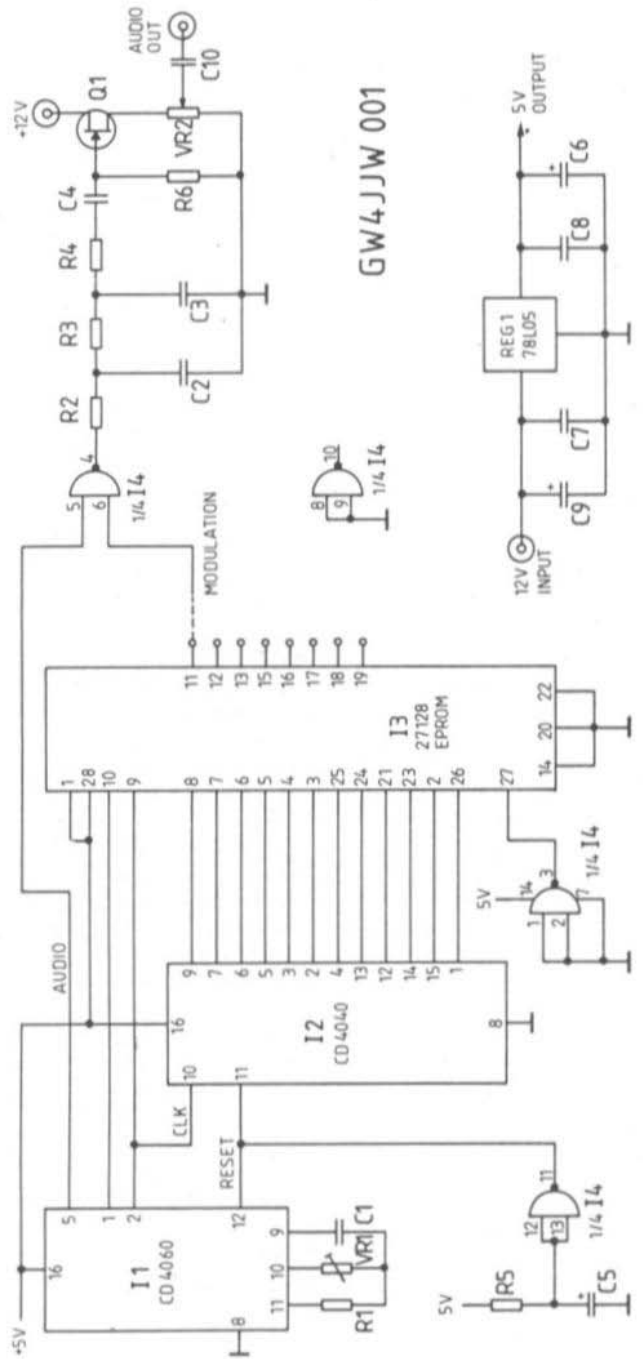

Fig. 1: Beacon circuit diagram

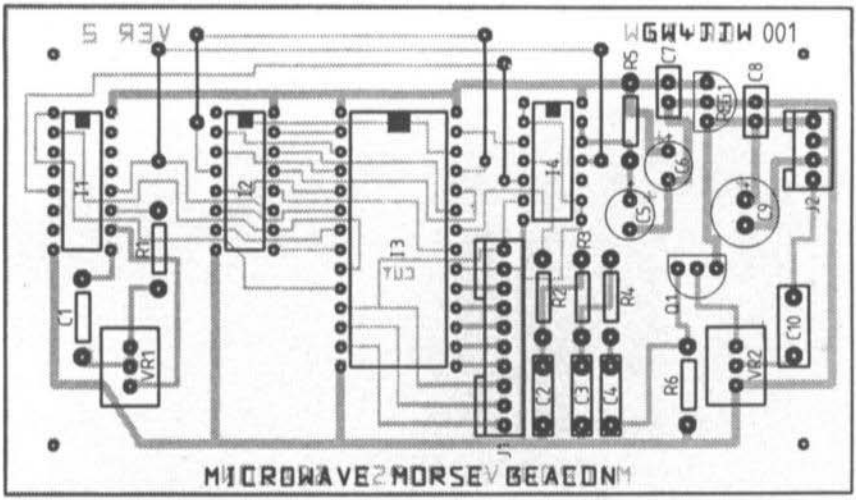

Fig. 2: PC-board GW 4 JJW 001

1.1. Connection

In the prototype the audio output was left continuously connected to the Gunn diode modulator and the 12 V supply was switched on when required. (In this way the EPROM does not consume power when its function is not required.) The morse code speed, and therefore the frequency of the tone, are adjusted by VR 1. The amplitude of the signal is adjusted by VR 2.

1.2. EPROM Programming

The EPROM contains a time image of the morse code to be sent out over the twenty minute period. Every address in the EPROM dictates whether a tone should be output or not. This state lasts for the period of a morse code dot before the EPROM address is incremented.

The author wrote a small BASIC program on a BBC microcomputer which translated ASCII text into morse code *. If a tone was required the byte was set to 255, but otherwise it was set to 254. (The author only used bit-0 and unused bits were set to 1 to speed up programming, but later the program was enhanced and is now able to generate each of the 8-bits of the EPROM separately so that 8 different "messages" may be stored in the EPROM). A morse code 'dash' would therefore be programmed as 3 consecutive addresses set to 255. These results were written to a disc file and later used to program the EPROM. If more than a single bit is used, it may be useful to dedicate one bit to a continuous tone. A ground connection is provided on the ten-way molex plug for 'no tone'.

2. CONCLUSION

The author combined this board with a simple Gunn oscillator and modulator and the resulting 'beacon' has proved most valuable in setting up

* A paper listing of the program will be sent upon request against C.R.I. (coupon-réponse international).

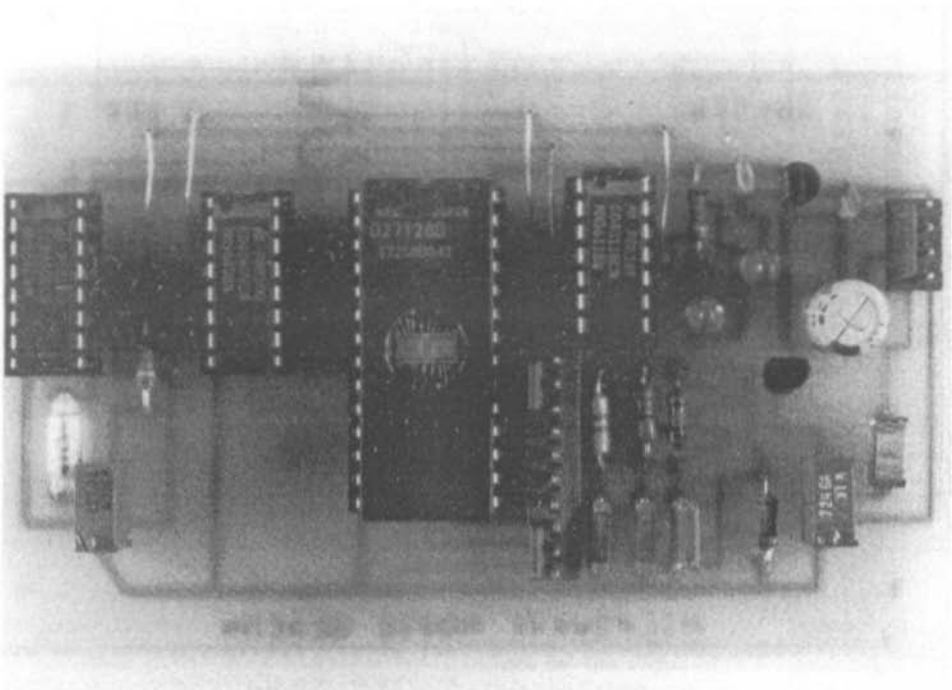

Fig. 3: A completed example of the GW 4 JJW 001 morse code generator

microwave receivers. In particular, one can be sure that the receiver is being aligned on the correct signal and not a spurious one.

3. COMPONENTS

I1	CD 4060
I2	CD 4040
I3	27128 EPROM
I4	CD 4011
REG 1	78L05
Q1	J 310/MPF 102
R 1	100 K
R 2	8 K 2
R 3	68 K
R 4	1 M
R 5	33 K
R 6	100 K
VR 1	100 K (multiturn)
VR 2	1 K (multiturn)
C 1	470 pF polystyrene
C 2	18 nF layer
C 3	2 n 2 layer
C 4	10 nF layer
C 5/C 6	10 μF 16 V tantalum
C 7/C 8	10 nF plate ceramic
C 9	100 μF 25 V can electrolytic
C 10	0.1 μF layer
J 1	10-pin vertical molex (optional)
J 2	4-pin vertical molex

Carsten Vieland, DJ 4 GC

UHF and SHF Broadband Mixers

For frequencies higher than the 70 cm band, the overwhelming majority of amateur mixers are singly-balanced, narrow-band types. However, the positive qualities of symmetrical passive mixers with 50 Ω ports such as, inter-port isolation, suppression of an undesirable mixer product or freedom from self-oscillation tendencies, are available at frequencies above 1 GHz.

The definite qualities of broadband 50 Ω mixers are evident not only in transmit and receive techniques but also in measurement techniques. The low-cost region of industrially manufactured mixers have, in the meantime, reached the 13 cm band (e.g. SRA-11H or LMX-123) and as a result, these mixers have become too expensive for most amateurs. The present technology strives for a band from 2 to 26 GHz.

This article describes broadband mixers which, because of their use of printed circuit boards, are easily and reliably reproducible, demand the use of no expensive components and by means of the well-tried mixer-attenuation, achieves the multi-octave bandwidth of 2 - 11 GHz.

Stimulated by a publication in a German-language, microwave magazine (1), the mixer described here, represents a translation of the published high-tech version into one using readily obtainable materials and components. The astonishing bandwidth specification proved extremely independent of component tolerances and diode characteristics. Practical experiments have shown that despite the use of not so favourably specified diodes or incorrect dimensioning, e.g. of the slotted lines, the characteristics of the mixer circuit are, in the main, well preserved.

1. CONSTRUCTION

The ring mixers which have long been popular e.g. SRA-1, IE-500 or HPF-505, contain two wideband, ferrite transformers and a ring mixer consisting of four Schottky diodes. Ferrite transformers exhibit sharp hysterisis losses above about 3 GHz, thus forming a natural barrier for this technology. Using powdered-iron cores has the disadvantage of narrower bandwidths. In the SHF region therefore, circuits are preferred which utilize the phase relationships of transformer tuned lines, Wilkinson combiners or symmetrical lines to produce the necessary diode phasing. In the following construction, a combination of strip and slotted lines (**fig. 1**) is used in order to achieve symmetry over a wide band.

1.1. PCB Material

The important circuit components are located on a double-sided PCB. As there can be no resonant structures in such a circuit, epoxy-glass base material can be used up to about 3 GHz. RT/Duroid in 0.79 mm thickness and Keene teflon substrate are usable up to about the X-band

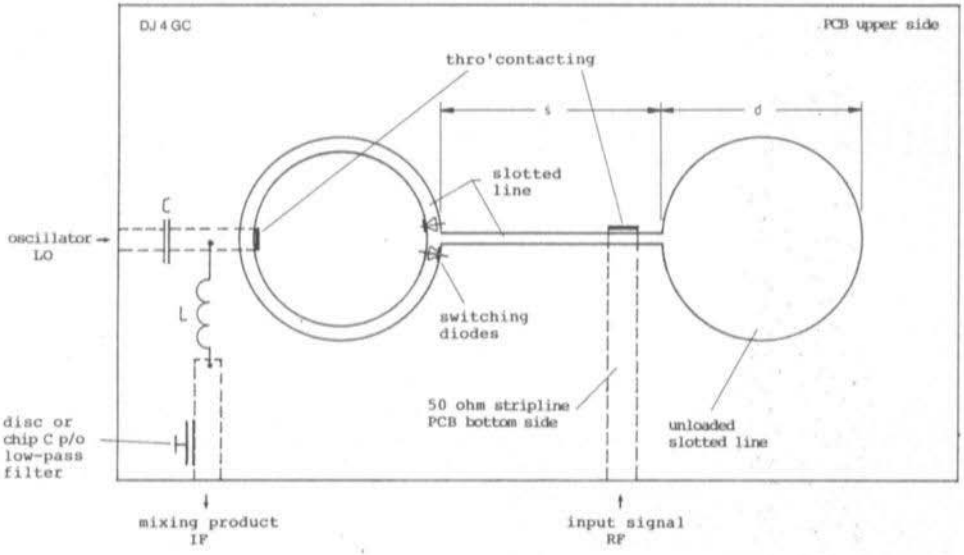

Fig. 1: The constructed details of a wideband, microwave mixer on a two-sided PCB

Mixer	d	s
SHF	5 mm	7 mm
UHF	18 mm	16 mm

(10.3 GHz). Ceramic substrates, owing to their high relative permittivity (9.7) and small loss-angle, appear at first to be ideal candidates. However, the difficulty of obtaining them and also the subtle methods attending the machining of this brittle material at an amateur level, forced higher losses to be tolerated by the use of more pliable and obtainable materials.

Besides that, however, there are new PCB materials appearing in the trade which impregnate the teflon carrier material with pulverized

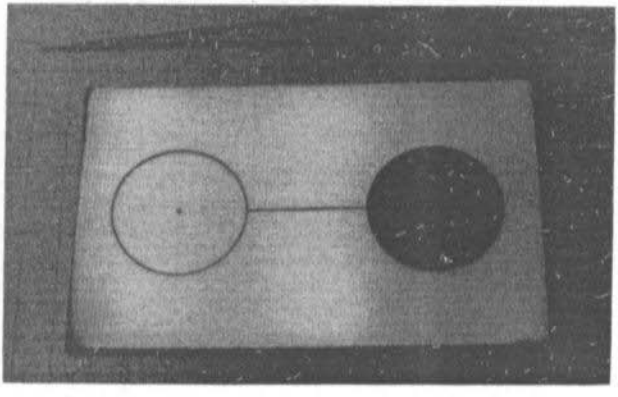

Fig. 2:
Etched mixer board with two BA 481

ceramic (e.g. RT/Duroid 6010 from Mauritz in Hamburg). The consequence of a high permittivity of over 9, is a reduced stripline width for 50 Ω to 0.65 mm (substrate thickness 0.635 mm). The realizable slot width of 0.2 mm results in a better wideband match to the diodes than can be obtained with the "normal" base materials having permittivities of around 2.34. Narrow striplines are therefore to be preferred to wide ones because of the lower energy loss by radiation and the resulting insensitivity to the fitting of covers on the instrument's specifications.

1.2. UHF Mixer

In this construction (**fig. 2**) the local-oscillator signal is fed in from the stripline via a through-contact into a circular formed slotted line. From the feed-in point of view, this arrangement appears like a parallel circuit consisting of two carrier lines. The L.O. signal is fed in-phase to the back-to-back diodes (**fig. 3**). The two diodes will conduct according to the momentary polarity of the oscillator signal. As in all passive mixers, the local oscillator has the function of opening

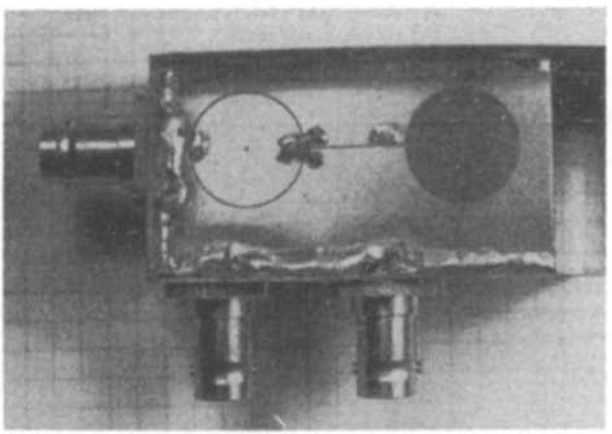

Fig. 3:
A complete UHF mixer in its metal box (slotted-line side)

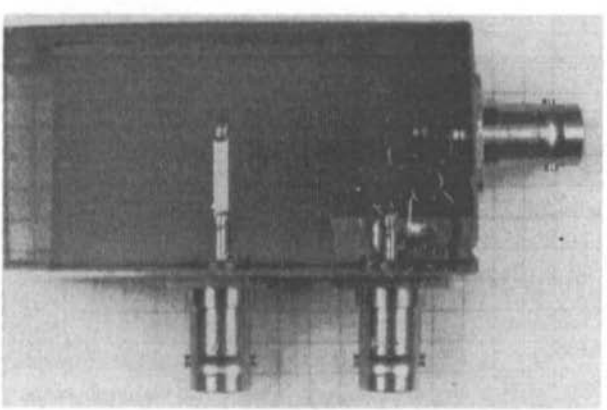

Fig. 4:
Stripline side of the UHF mixer showing the IF low-pass filter, the inductor of which is fashioned from bent wire (grid = 5 mm)

and shutting the diodes at a pre-determined rate. This role could be fulfilled by a relay contact if it were fast enough.

The mixing products are taken from the slotted-line island. The lower difference-signal is selected by a low-pass filter (**fig. 4**) and taken to a coaxial socket. In order to avoid connecting losses, an isolating capacitor (of e.g. 10 pF) is placed in the oscillator's stripline lead-in, which acts as a high-pass filter. As, normally, the IF and the L.O. signals lie very far apart in frequency, no formal diplexer is required for this purpose.

The HF input signal is, either capacitively or via a through-contact, (fig. 4), fed into the slotted line. On the one side, it goes to a circular-formed expansion (unloaded slotted-line) which acts as an impedance discontinuity point. The input signal is reflected from this point and taken to the L.O.-controlled diode switch. From here, and at a clock speed determined by the L.O., energy is transferred to the slotted-line island, first from one diode and then from the other oppositely-phased diode. The multiplexed signal contains both the sum and the difference frequenicies. This arrangement is representative of a simple balanced mixer circuit.

The dimensioning of the slotted line poses many problems. As opposed to striplines, the characteristic impedance of slotted lines is considerably more frequency-dependent. As only the opposite copper edges of the slot are involved in the transport of energy, there is a higher additional loss due to skin-effect which increases with frequency. The various line lengths can never be terminated at every frequency with its nominal impedance. This inevitably, not only leads to both an increasing attenuation with frequency but also to a pronounced ripple across the working band of the mixer.

The prototype used photo-resist PCB material (e.g. RT/Duroid 5870). Both striplines are 2.4 mm wide and are located on the underside of the board. They are made by adhering black strips directly to the photo-resist. Then an exposure is made, followed by developing and etching.

The slotted-line structure can be made quite easily by the use of a pair of divider scribers to scratch a circle in the photo-resist. During the

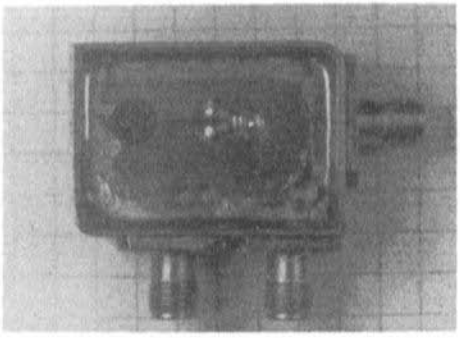

Fig. 5: SHF mixer (slotted-line side) showing both diodes (BAT 14-093). All connectors are SMA (grid = 5 mm)

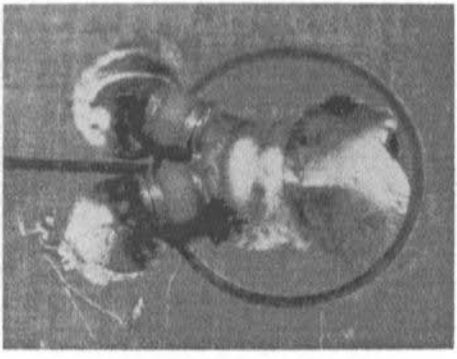

Fig. 5a: Close-up of the mixer diodes

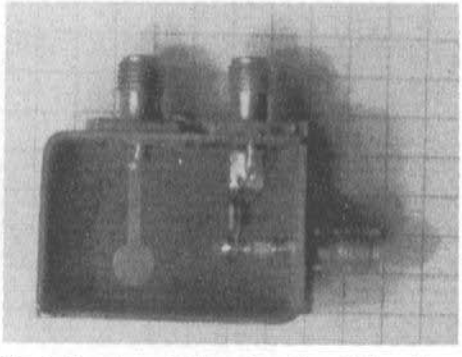

Fig. 6: The mixer of 5 above from the stripline side. The cross-shaped structure is the printed RF input capacitor

following etching process, a 0.25 mm wide slot is formed in the copper-clad surface (fig. 2). The production of a suitable exposure mask is much too time-consuming for a one-off job.

1.3. SHF Mixer

The SHF mixer is shown in **figs. 5 and 6**. The RF input signal is coupled-in capacitively from the stripline to the slotted line by means of a printed structure. In the UHF version, this structure would have been too large, which is why the through-contacting was used. The function is not, however, greatly influenced by the type of input coupling.

The lower limit frequency of this mixer type is reached when the line length of the circular slotted line presents little or no diversion length for the RF signals.

The isolating capacitor in the oscillator branch should be of the "chip" construction (e.g. ATC). Also, the switching diodes (**fig. 5a**) could be chosen in the first instance, according to their form of construction – the smallest form of any particular type being selected. Glass diodes (BA 481) exhibit good characteristics well into the S band. For use in the X band, a microwave diode housing must be employed. The favourably-priced GaAs diodes MGF 3000 can be used in spite of the somewhat large size of their housings. By using a large L.O. input power (+ 13 dBm), the characteristics of these diodes allow a particularly good intercept point (IP) to be achieved.

2. MEASURED RESULTS

The characteristics of mixers are very difficult to assess because two extremely wideband oscillators are required, one of which, must be capable of producing at least 10 mW output power. In order to obtain a sweep display, both test oscillators must be swept so that there is always a constant frequency difference (the IF) between them. As this sort of test equipment is seldom to be found in amateur workshops, a mish-mash of various oscillators, filters, amplifiers, and attenuators must be put together. The general arrangement of the test set-up is shown in **fig. 7**.

To set the level of the HF input signal to 0.5 mW (– 3 dBm), the signal is taken to a thermal power meter via a high-grade change-over switch. A second power meter monitors the power in the IF port at a frequency of, say 145 MHz. Both oscillators must maintain a constant difference

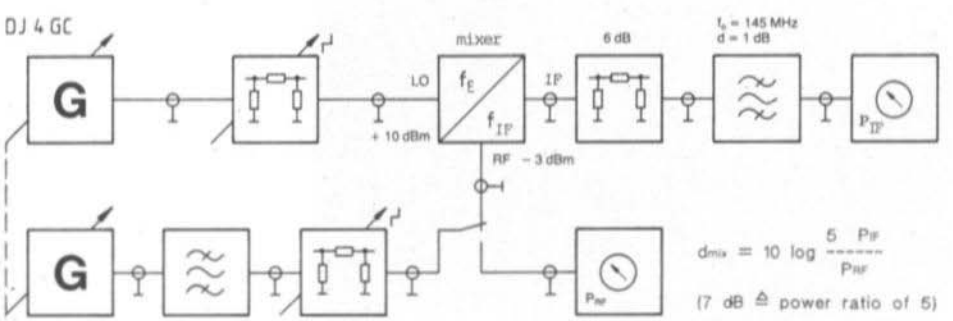

Fig. 7: Test set-up to measure the mixer loss. The attenuator at the IF port is for matching purposes.

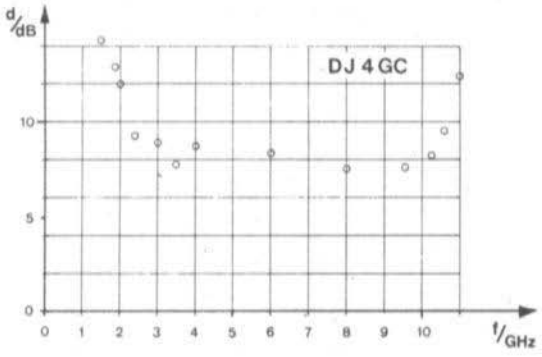

Fig. 8:
Point-by-point depiction of the SHF mixer's mixing loss

of 145 MHz between them at all test frequencies within the range of interest. The oscillator power must always be + 10 dBm.

The RF signal should, in the interests of spectral purity, always be filtered. A harmonic of only − 10 dBc could falsify the measured mixer loss by as much as 0.5 dB. Even after many careful measurements, a measurement tolerance of 0.5 dB should be expected.

The upper frequency limit of the SHF mixer (**fig. 8**) lies in the immediate vicinity of the 10 GHz amateur band (up to 10.4 GHz). To ensure its conclusion, the circular slotted-line structure should be shortened by 0.5 mm to a diameter 4.5 mm. In addition, it would be very interesting to find out whether a reduction of the diameter to 1.6 mm and using beam-lead diodes would allow 24 GHz to be reached?

The IF signal is taken out via a low-pass structure. The required capacitance can be afforded by a chip capacitor or a through-contact could be used. The chosen IF top frequency for the SHF

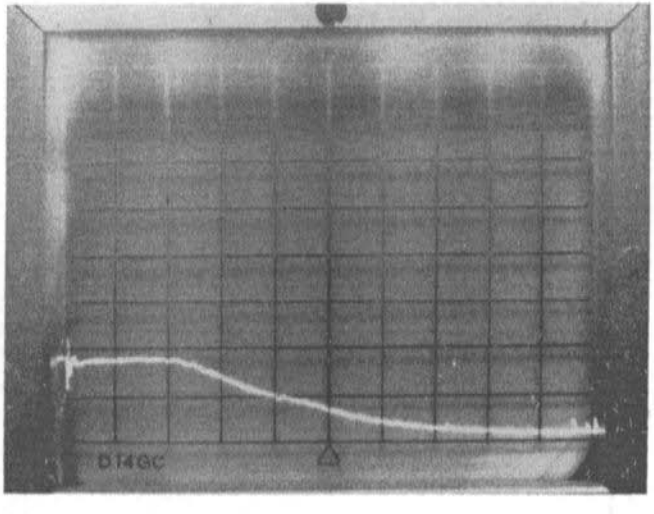

Fig. 9:
Frequency response of the IF port
Centre frequency: 500 MHz
Range: 0 - 1 GHz
Vertical: 10 dB per cm

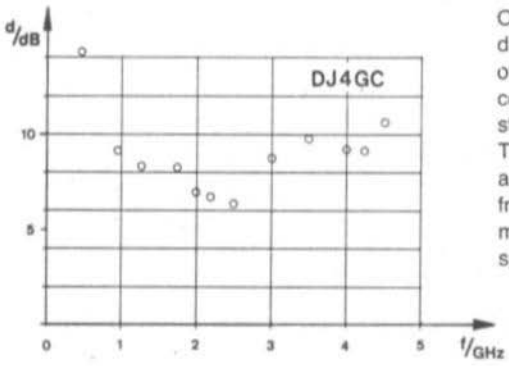

Fig. 10: Point-by-point depiction of the UHF mixer's mixing loss

On the whole, there was not all that much difference in the main, usable characteristics of this home-constructed mixer to those of commercially made mixers. Certainly, the constructional techniques were basically the same. The SHF version was tested in a spectrum analyzer which was expected to take care of a frequency band of 2 to 9 GHz. In the event, only marginal differences could be detected in the spectrum analy's performance.

mixer, 250 MHz, could be seen on the CRT screen by means of a measurement trick. The signal-port generator was replaced by a high-grade, amplified, GHz noise source and the IF monitor oscilloscope, by a spectrum analyzer. The noise spectrum can then be displayed at the IF port as in **fig. 9**.

The UHF mixer has a differently dimensioned low-pass structure which uses an etched capacitor. The 3 dB limit frequency lays around 700 MHz (**fig. 10**). The isolation between the L.O. and RF-input ports lay between 10 dB and 22 dB according to frequency.

The return-loss measurements of mixers is not a subject that manufacturers of mixers like to discuss in detail. Practical measurements yielded a result of 10 dB but that was after optimizing both the power and frequency of the input generators. In this respect, this home-produced effort found itself in quite respectable company.

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Dr. (Eng.) Ralph Oppelt, DB 2 NP

Stabilizing the VCO Frequency by Means of Monostables
Part 2: A Continuously Tunable VCO for the 2 m SSB Band

Part 1 of this article described the principles of the stabilization of VCOs by means of monostable multi-vibrators and also the frequency drift behavior of these oscillators. This second, concluding article, will describe the constructional details of such a VCO which may be employed, for example, with the phasing method of SSB generation described in ref. (1). This would then form the basis for an economical home-constructed, SSB, 2-metre transceiver.

5. CHOICE OF MONOSTABLE

The most convenient integrated monostables are the 4047, 4528 and 4538 from the CMOS 4000 series, also the 74121, 74221, 74122 and 74123 together with their improved, pin-compatible equivalents, the 74422 and 74423 from the 7400 series. The latter series have also meanwhile sprouted a multiplicity of various types in the 74SN..., 74LS..., 74ALS..., 74S..., 74F..., 74HC..., 74HCT...etc. families.

As the ICs are mostly used in battery-supplied equipment, the ones having the lowest power consumption i.e. CMOS or 74HC types, are to be preferred. One thing to be watched, however, is that the minimum duration pulse (T_a) required can be generated in the proposed type to be employed. According to eq. 9 (part 1) the required T_a, for a favourable dimensioning, is about 20 % smaller than the VCOs reciprocal deviation $1/(f_H - f_L)$. For the 2-metre band then, the output pulse duration T_a is about 400 ns – this is able to be reproduced with certainty.

Every real square-wave pulse has, however, finite rise and fall times and mostly has an overshoot or undershoot as well. As **fig. 6** makes clear, it is always important that the monostable output signal u_a (t) has returned to zero before the next trigger pulse. This ensures the linear relationship, indicated in eq. 2, between the monostable frequency $f = 1/T$ and the average value $\hat{u}_a$ of the monostable output signal u_a (t) is valid for any output wave shape. Any departure from the ideal wave shape in u_a (t) will always result in a modification to the relationship given in eq. 2 between $\hat{u}_a$ and f. If u_a (t) has not decayed to zero before the next trigger sequence occurs, a linearity error at the high end of the VCO's band will be the result. It is important that the minimum pulse attainable should be regarded as that occurring from the zero at the leading edge of the pulse, to the instant the wave-form has reached a steady state zero at the trailing edge of the

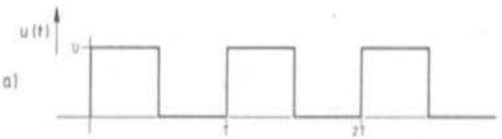


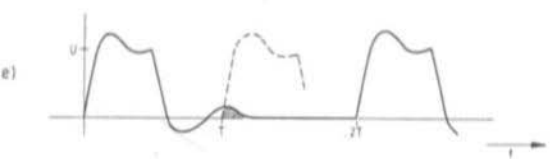
Fig. 6:
Influence of a non-ideal wave shape of a square-wave signal upon its average value $\hat{u}$, i.e. upon the actual frequency of the VCO

a) ideal square-wave, average value $\hat{u}_a = \frac{1}{T}\int_0^T u_a(t)\,dt = U/2$

b) as a) above but non-ideal square-wave, average value $\hat{u}_b = \frac{1}{T}\int_0^T u_b(t)\,dt = c \cdot U/2$ with $c \approx 1$

c) as a) but at half the trigger freq., average value $\hat{u}_c = (U/2 + 0)/2 = U/4 = \hat{u}_a/2$, i.e. exactly half the average value of a)

d) as b) but at half the trigger freq., average value $\hat{u}_d = (\hat{u}_b + 0)/2 = \hat{u}_b/2$, i.e. exactly half the average value of b)



e) Non-ideal square-wave with pronounced overshoot. The trigger frequency $\frac{1}{2T}$ average value

$\hat{u}_e = \frac{1}{2T}\int_0^{2T} u_e(t)\,dt$ (the solid curve is $u_e(t)$)

Triggering at twice the frequency $\frac{1}{T}$ (dotted curve), does not result in twice the average value $2\,\hat{u}_e$, as $\int_0^T u_e(t)\,dt + \int_0^{2T} u_e(t)\,dt$: $u_e(t)$ has, at time T, not reached a stable zero value (see also the hatched part).

pulse. This is the condition which the minimum attainable pulse duration T = 1/f will drive the VCO without any risk of linearity error.

The integrated circuit chosen for this 500 kHz tuning range, SSB VCO is the economical and easily obtainable 4528, in CMOS. This applies also to any VCO which is required to cover the whole of the 2-metre band i.e. 2 MHz. Nevertheless, there is quite a difference in these devices between those of different manufacturers. A good example of the 4528 should be able to produce a minimum pulse of about 120 ns duration with 5 V supply potential and an external load of $R_{min.}$ of 5 kΩ and output capacity of 0 pF.

6. VCO MODULE, CIRCUIT DIAGRAM

The circuit shown in the block diagram of **fig. 7** shows, besides the actual VCO, a crystal oscillator (XO) employed for the generation of a 9 or 10.7 MHz carrier for the mixer which translates the VCO frequency to the transmitting range of 144 to 144.5 MHz. This module may be combined directly with the SSB phasing-method generator described in (1) thus making for a compact single module.

In order that the problem with spurious signal generation, which was discussed in part 1, is avoided, the VCO uses two downward translations (despite what is shown in fig. 1) in order to attain the final local oscillator frequency. In order that things are kept as simple as possible, self-oscillating crystal mixers are used for this operation. An IF of 10.7 MHz was used which means that the VCO must cover from f_L = 133.3 MHz to f_H = 133.8 MHz for transmission on the lower quarter of the 2 m band. Both crystal mixers use cheap computer crystals, 24.576 MHz excited on its 5th over-tone giving an output on 122.96 MHz for the first one, and the second mixer uses a 10.24 or 10.245 MHz fundamental crystal oscillator.

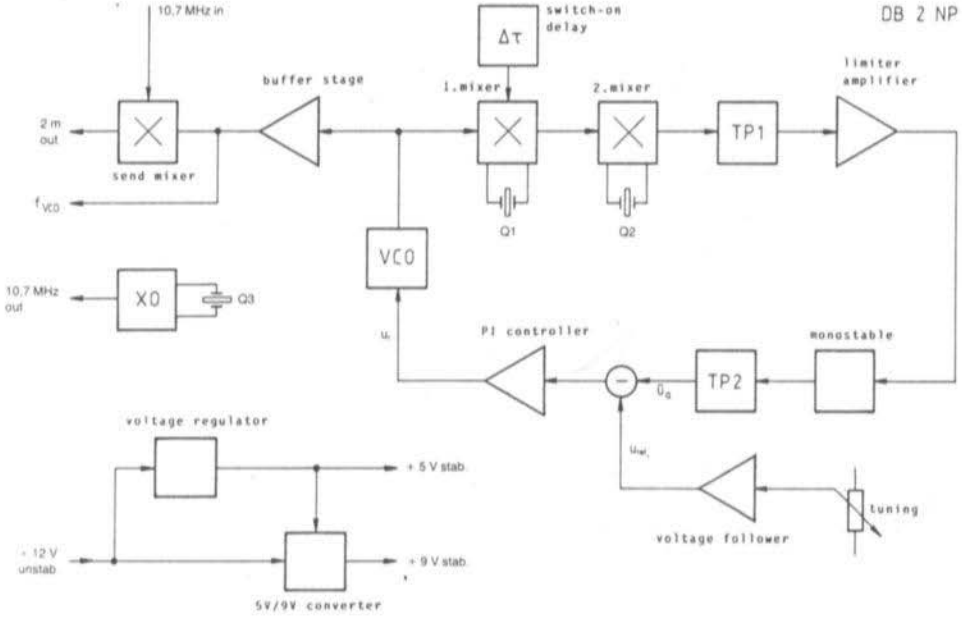


Fig. 7: Block diagram of the VCO for SSB operation in the 2 m band

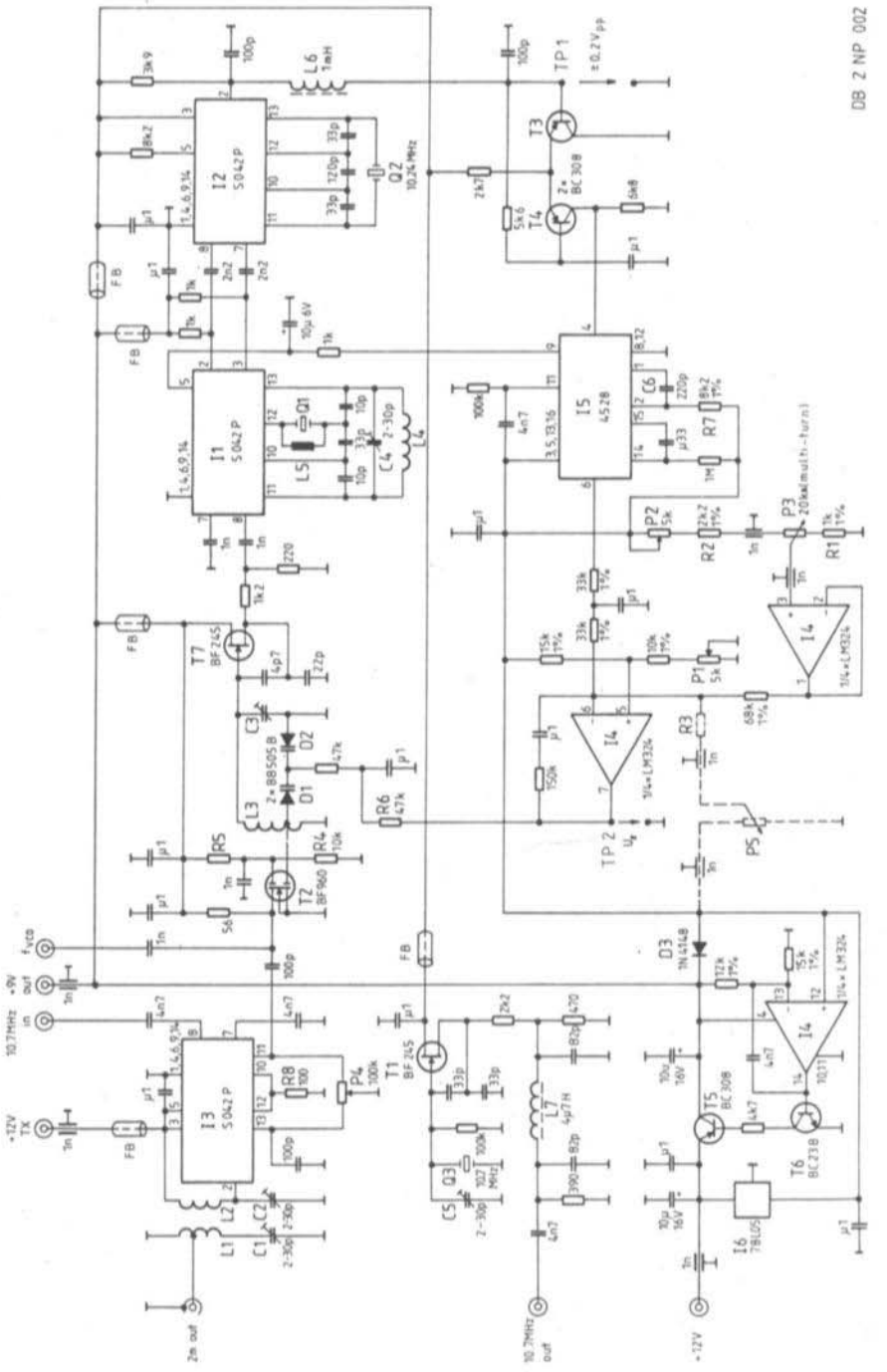


Fig. 8: The circuit schematic of the VCO of fig. 7

The circuit schematic of **fig. 8** shows the whole arrangement in detail. As many standard circuits have been employed, only the peculiarities in this design will be enlarged upon.

It may be observed that the varicap diodes D1 and D2 are not shunted across the complete tuning inductance L3 but only a low-impedance tapping point of it. This measure ensures that a larger tuning voltage increment is required to achieve a given frequency variation. Therefore, a reasonable tuning voltage range of 3 to 7 volts is required to cover the entire VCO range instead of a few millivolts (see part 1, para. 2).

The VCO signal is fed from the source circuit into the PLL control loop. It is then taken to a limiter-preamplifier (2 x BC 308) via the two mixer stages and a 3rd-order, 750 kHz, low-pass filter. It is then presented to the input of the monostable trigger. With the crystals used here, this trigger signal lies in the range of about 100 to 600 kHz. Using other combinations of Q1 and Q2 could result in a higher than intended spectrum resulting in a deterioration of the frequency stability.

The second monostable of the 4528 is disabled for a few milli-seconds following the application of the 12 V supply voltage. This ensures that the control loop trigger signal for the monostable is missing which simulates a "too low" VCO frequency. The control loop voltage U_c and with it the freely oscillating VCO, assumes its maximum possible value. Thereby, when the first mixer is activated via pin 5, the VCO is started up with the correct sideband and a proper PLL lock is ensured.

Frequency tuning is carried out by means of the 10-turn potentiometer P3. Owing to the somewhat coarse winding of this pot'meter, the tuning appears to occur in fine steps making it difficult to adjust to very fine limits. This effect is not pronounced enough to notice when tuning in a station. Should a more continuous tuning be required, it will be necessary to add the dotted-line components P5 and R3 and, depending upon the choice of R3 (MΩ range), it is possible to tune right down to ± 1 kHz or ± 5 kHz. Since the 10-turn pot'meter has a tuning rate of 50 kHz per turn, this alternative is, at the same time, a valuable tuning aid particularly for those whose hand is not too steady.

Of particular importance for the linearity is the resistor R1 on the ground side of P3 as it limits the voltage to be handled by the following voltage-follower IC to a few mV above its negative supply rail (i.e. 0 volts!). As the DC component of the monostable output voltage $\ddot{u}_a$ increases with the VCO frequency, a falling voltage must be provided at the output of the voltage-follower in order that the PI controller has a balanced voltage at its two inputs. When the slider of P3 is set against the connection of R1, the VCO frequency must be at exactly f_H = 133.8 MHz. This adjustment can be precisely adjusted with P1 at the non-inverting input of the PI controller. The setting of P2 is almost irrelevant as it does not affect the voltage set by P3 to any great extent as long as the wiper of P3, as ordained, is turned to the extreme end of its travel to the R1 end. If the wiper is now turned to its other extreme i.e. to the R2 end, the lower band frequency of f_L = 133.3 MHz may be set without affecting the upper frequency setting. This measure avoids the tiresome, iterative adjustments at lower and upper frequency limits so prevalent with other VCO designs.

The stabilized voltage for the monostable IC is provided by the standard three-terminal 78L05. It has proved fully satisfactory for this application but can, of course, be changed for a higher-quality type if required. This stabilized 5 V supply is also used, together with a second IC, type LM324, to provide a stabilized 9 volt for most of the other stages as well as for eventual external employment. Because a pnp type was chosen as the series stabilizer transistor only a 0.3 V voltage difference was necessary. It functions thereby perfectly satisfactory even when the battery voltage has sunk from 12 V to as low as 9.3 V (that is, in any case, long after a change of batteries should have been considered).

The function of diode D3 is of importance. This lies, in the same 9 V stabilized line as the LM324 and ensures that the latter is initially supplied with 4.3 V (i.e. 5 V minus the diode drop) upon switch-on. The circuit is then able to rise automatically to the required 9 V. Diode D3 is then poled in the blocked direction.

7. CONSTRUCTION, COMMISSIONING AND ADJUSTMENTS

Fig. 9 shows the component layout plan of the 72 x 109 mm PCB DB 2 NP 002 which is intended for a tin-plate box of 74 x 111 x 30 mm dimensions. The construction follows closely the procedure mentioned in (1); i.e. first drill all the holes in the tin-plate box, then solder the pre-drilled PCB into the housing – the ground plane to the walls of the box. The tin-plate compartment walls are then fitted and soldered in. The latter are, in fact, not strictly necessary but at least the VCO should be soundly enclosed and fitted with its own lid. The latter should also have a hole drilled in the appropriate place to allow C3 to be adjusted (see the photo of the prototype in **fig. 10**).

The equipping of the board should start with those components which are difficult to get at, or that must be soldered to ground on all sides, or that lie in the vicinity of the wall. It is preferable not to provide an IC holder for the S 042 P. The five pins which are shown connected to ground, are splayed out at right-angles on to the ground plane surface and soldered on to it.

Since the ferrite beads are always placed in the supply line to each individual stage, it is advantageous to include them one by one as the stages are tested.

Upon switching on the completed unit, the stabilized + 5 V and + 9 V supply rails are tested to ensure that they are functioning correctly. The phase loop is then opened by temporarily removing R6 from the PI controller's output and connecting it with the wiper of a test poten-

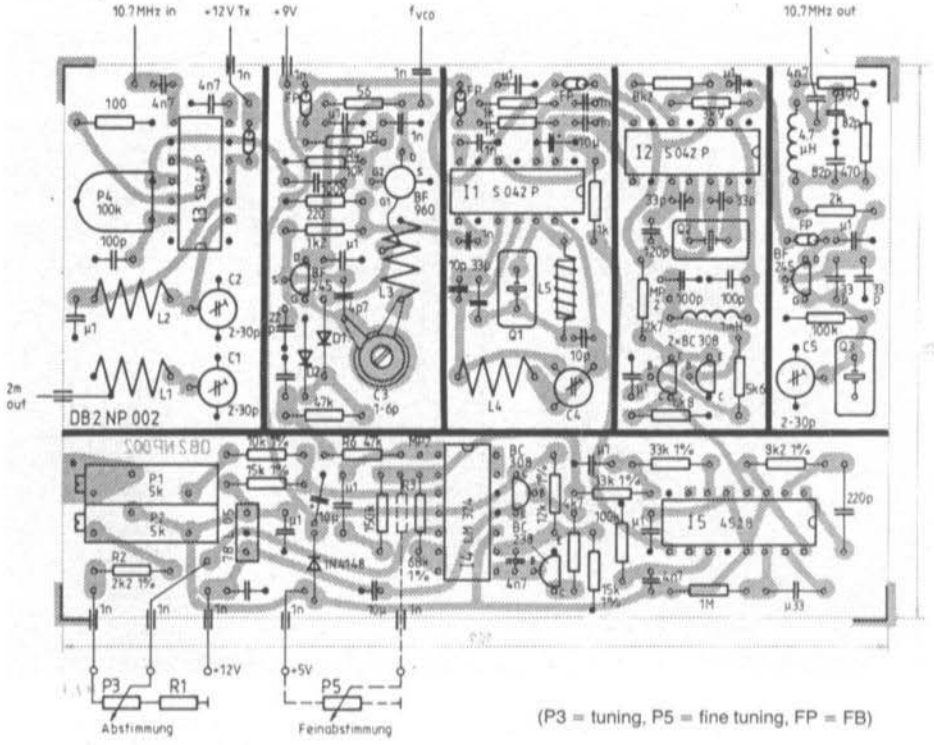


Fig. 9: The component layout for PCB DB 2 NP 002 for the circuit of fig. 8

tiometer, of about 10 to 50 kΩ, which lies across the + 9 V supply.

Now, the VCO output is connected to a frequency counter and both frequency and the voltage at the wiper of the test potentiometer monitored simultaneously. Capacitor C3 is so adjusted that at f_H = 133.8 MHz 7 V (approx.) is obtained. At f_L = 133.3 MHz, the reading should then be 3 V (approx.). If, owing to the tolerances of D1 and D2, this voltage range differs from 4 V, the tapping point of L3 should be shifted towards the cold end of the inductance to reduce the voltage range and towards the hot end to increase it.

Following this preliminary tuning, the VCO is set to 133.5 MHz (approx.). By means of the voltage divider R4/R5, the VCO output voltage can be varied within certain limits. A guide line for this voltage is that provided by the gate-2 potential of the BF960, i.e. 1.8 V which entails a 39 kΩ resistor for R5.

Now, L4 is loosely coupled by an inductive loop to a sensitive frequency counter. By carefully adjusting the capacitor C4, the 5th overtone of the crystal Q1 is excited. It will be immediately apparent from the behavior of the frequency counter if the oscillator is oscillating wildly or

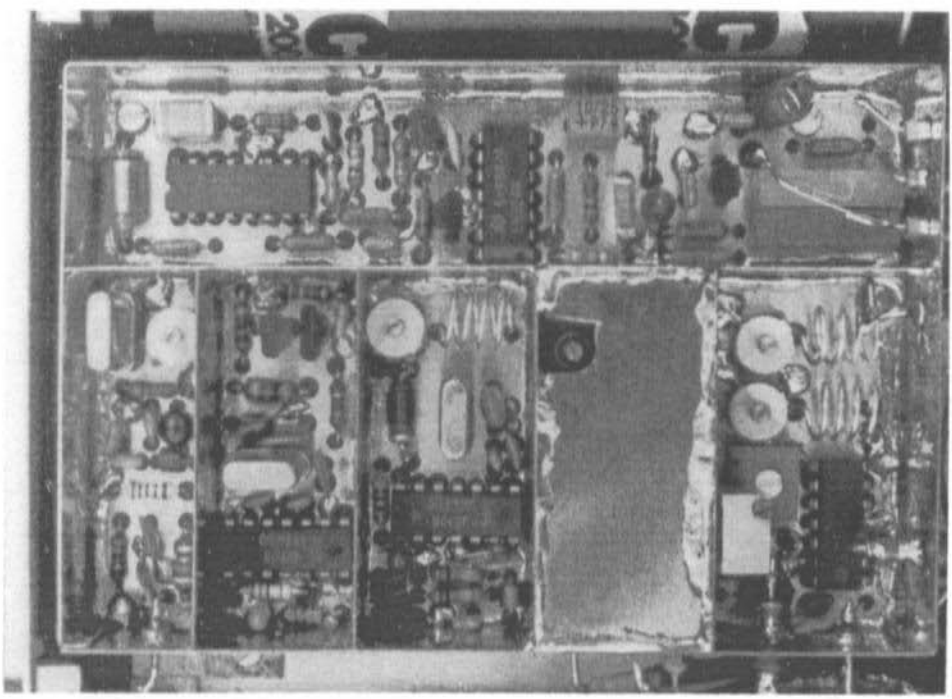


Fig. 10: Prototype of the fully equipped PCB DB 2 NP 002. The oscillator stage is largely hidden away under the soldered-on compartment cover. The trimmer C3 must be accessible. This is achieved by providing a 5 mm hole in the PCB and reversing the trimmer so that its slotted spindle protrudes through the ground-plane.It is then soldered to the track-side.

suddenly locks in to the crystal's overtone frequency. This stage is, in fact, somewhat critical. It may be necessary to match RFC L5, the crystal's capacity compensator, to the crystal in use. Suffice it to say that the stable operation of this stage is absolutely necessary for a stable VCO operation!

The second mixer/oscillator is, on the other hand, without any problems whatsoever. The down-converted VCO, tunable over 200 kHz, can be inspected with an oscilloscope at TP 1. Its amplitude should not be smaller than 0.2 V_{pp}. The amplitude can be maximized by a careful adjustment of C4 which makes the first mixer/oscillator oscillate at full power.

A slightly rounded square-wave signal should now be seen at pin 4 of the 4528 of 4 to 5 V_{pp} amplitude. This triggers the monostable. At its output (pin 6), clean square-wave signals should appear in synchronism with the trigger signal and whose period (1.5 μs) is set by R7 and C7.

The 12 V supply is now disconnected and the PLL loop closed by removing R6 from the test potentiometer and connecting it to the PI controller's output.

After re-applying the 12 V supply, there should be 3 to 7 V at TP 2. If it is only a few mV or nearly 9 V, i.e. at the extremes of the given range, it is an indication that the VCO, for some reason or other, is not phase-locked.

Now, the tuning for f_H = 133.8 MHz and f_L = 133.3 MHz can be carried out with P1 and P2 in exactly the same way as described earlier. At the band extremities it would appear as if the multi-turn pot'meter is non-linear. It may be therefore advisable to set this pot'meter (P3) to the first graduation on the scale and then with P1 set the frequency to 133.35 MHz. In the same manner, P3 is then set to scale graduation 9 and P2 is then adjusted for 133.75 MHz. The extreme frequencies then deviate but slightly from 133.3 and 133.8 MHz but the rest of the scale is much more precise. It should be noted, however, that potentiometers P1 and P2 are not so isolated from each other and this, of course, means more iteration from high to low scale until a satisfactory calibration has been achieved.

In conclusion, the stages which do not belong to the actual VCO are tuned. Capacitor C5 is tuned to obtain exactly 10.70000 MHz from the crystal oscillator Q3. If its output is then, provisionally, fed into the 10.7 MHz input of the transmit mixer, a signal at 144.0 to 144.5 MHz should appear at the mixer's output. Capacitors C1 and C2 should then be set to achieve maximum output power and P4 adjusted for the best possible carrier (133 MHz) suppression. The latter adjustment is carried out by withdrawing crystal Q3 and adjusting P4 for a minimum output. By increasing R8 it is possible to attenuate the 144 MHz output signal and thereby saving on battery supply requirements.

8. OPERATION AND CIRCUIT VARIANTS

The VCO as described was tried by the author in an SSB/AM home-constructed transceiver. After an initial warm-up period of about 3 minutes, it was not necessary to keep re-adjusting the frequency tuning. Components that were toleranced 1 % were, in fact, replaced by 0.1 % tolerance and a thermal drift of ± 50 ppm. A thermal compensation process such as that mentioned in chapter 2, is not, however, absolutely necessary for amateur applications. It would only become unavoidable if, during the course of operation, that large extremes of temperature were encountered and also a large store was laid upon the scale marking being absolutely correct at all times. Such temperature variations are only possible in practice, when the equipment is taken from a warm room into outside air with a temperature of say − 10° C in winter or a summer temperature of + 50° C and operations are immediately commenced. This sort of operational practice will certainly require corrective frequency procedures to allow drift-free operation following switch-over breaks.

A rule of thumb for the optimal dimensioning of the monostable's R7 and C6 to achieve good thermal stability (such as e.g.: 50 Ω NTC in series with R7) cannot be given, as the frequency drift

is dependent upon the inter-relationship between too many components. The correction must be determined individually for each VCO by a series of measurements in a thermally controlled enclosure.

The 10-turn potentiometer has been specified with a ± 0.25 % linearity. As the VCO tuning range covers 500 kHz, an error uncertainty of this magnitude can be expected in the frequency setting due to this cause alone i.e. ± 1.25 kHz. This can be only be circumvented by an individual scale calibration or by a correction scale/table. The author's prototype exhibited a scale error of ± 1 to 2 kHz, the precise error depending upon the frequency setting within the 500 kHz range. A more exact frequency setting could be obtained by the employment of a ± 1 % linearity potentiometer or with a digital frequency read-out. As the VCO signal is downwards translated in any case, only a very slow frequency-counter chip is required, e.g. the 5-digit LCD module EA 6077 which is able to work up to 4 MHz and takes a supply current of only 2 mA (2). To bring it into operation requires only the provision of a buffer stage, e.g. a CMOS inverter stage connected with the monostable's trigger signal. To enable the frequency to be read easily, a specially selected combination of Q1 and Q2 is necessary in order that the exact band edge frequencies, e.g. 100.0...600.0 kHz or better 0...500.0 kHz are produced. The latter then would correspond to a working frequency of 144.0...144.5 MHz.

As the VCO is very easily frequency modulated (see part 1, fig. 1), it would appear a natural reaction to build a circuit variation which will cover the full 2-metre band for use in an FM-transceiver. The required modifications for this application are to be seen in **fig. 11**. The first mixer oscillator is crystal-stabilized at a frequency of 144 MHz minus the IF, i.e. in this case at 133.3 MHz supplied, if necessary, from an external XO. The second mixer oscillator oscillates with the IF, when in the TX mode, i.e. 10.7 MHz. If now, the monostable's time constants are reduced to 400 ns and the limit frequency of the low-pass filter following the 2nd mixer increased to 2.5 MHz, the VCO is able to be tuned to cover a frequency range from 144 to 146 MHz.

The provision of a frequency offset for radio transponder operation is effected by a 10.1 MHz (i.e. 10.7 MHz minus 600 kHz) crystal. In the receive mode (RX), the second mixer oscillator is totally unbalanced and the oscillator part of the circuit suppressed in order that the mixer input signal passes spectrally unaltered to the mixer output. The consequence of this is that the VCO supplies the frequency range 133.3 MHz to 135.3 MHz, i.e. the working frequency minus the IF, to the receive mixer.

As the VCO deviation is multiplied by four times in the process of arriving in the vicinity of the band to be used, the tapping point for the varicap diodes D1 and D2 on the inductor L3 must be made higher up the coil. In addition, a second pair of varicap diodes has the job of providing a large frequency shift, by an amount equal to the IF, during TX/RX switching in order that the PI controller can retain control, within its output voltage limits, over the loop frequency for both TX and RX. Due to the shifting of the VCO spectrum by an amount equal to the IF, an up-conversion mixer for TX is rendered superfluous and therefore obviating the spurious signal problems attending mixer stages.

In SSB equipment, this upward frequency translation is unavoidable as the SSB processing takes place invariably at the IF level. As the monostable trigger signal lies, in both the case of "send" and "receive", in the range 0 to 2 MHz, it is easily retro-fitted with the LCD counter module EA 6077. The working frequency is arrived at by the addition of 144 MHz to the displayed frequency. As the tuning range now is 0 to 2 MHz and not as previously considered, 0 to 500 kHz, the zero is not very exact and could read out at several kHz. The other case entails the coupling and de-coupling capacitors having an excessively high value thus making the VCO unstable in its lower tuning range. (There is also the possibility of a random transition to the other sideband: X-coupled PLL). When tuning the VCO for the indicator translation 0 to ... MHz, the trigger signal lower frequency limit should commence at about 5 kHz for the SSB version and about 25 kHz for the FM version. The lowest working frequency would then be 144.005 MHz (SSB) or 144.025 MHz (FM) and not 144.000 MHz.

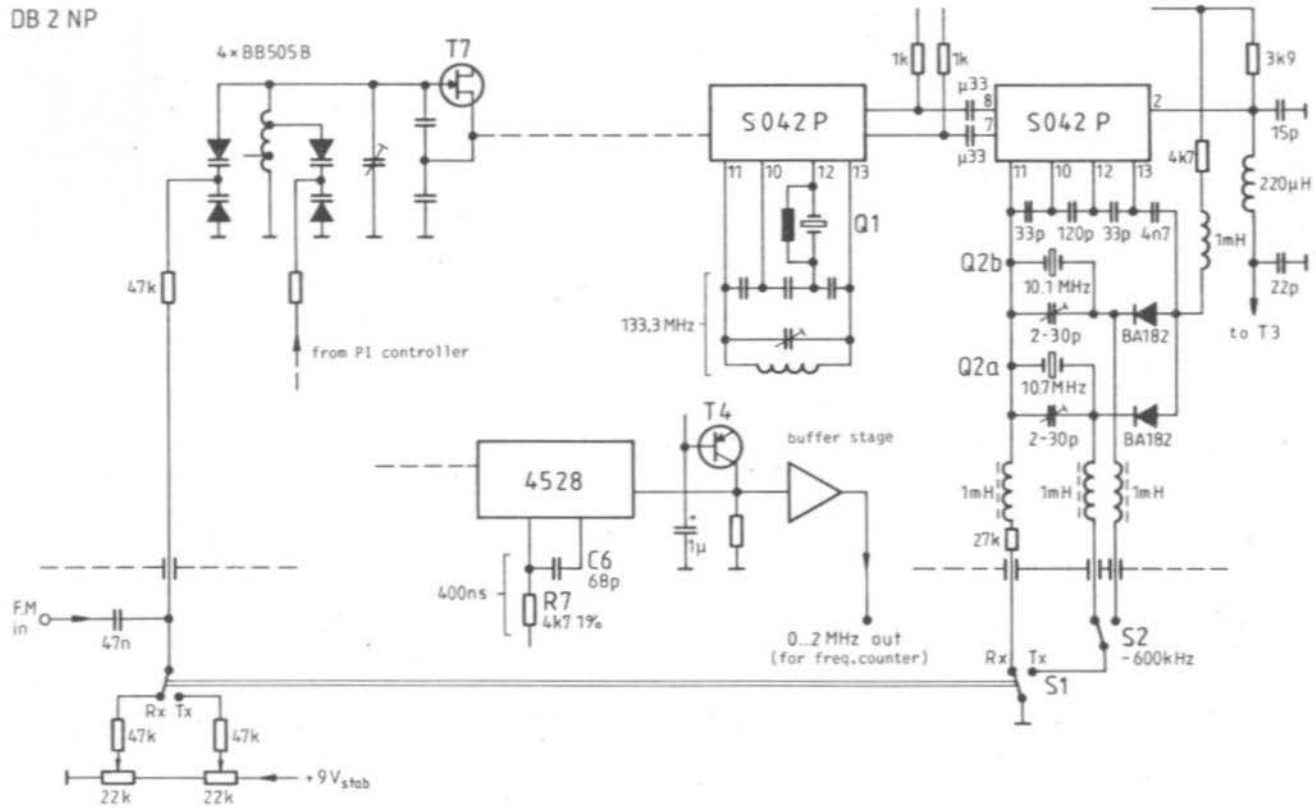


Fig. 11: Modification of the VCO of fig. 8 for an 144 - 146 MHz FM-transceiver having a 0 - 2 MHz output for a frequency counter. Switch S1 is the IF shift for the RX/TX change-over. Switch S2 enables the 600 kHz off-set required on TX for relay operation. The 9 MHz IF version requires Q 2a and Q 2b to be changed to 9 MHz or 8.4 MHz. The up-conversion mixer (IC3) and the carrier oscillator stage (T1) shown in fig. 8 are redundant.

9. COMPONENTS

I1...3:	S 042 P (Siemens)
I4:	LM 324 (various manufacturers)
I5:	4528 (e.g. Fairchild, Valvo)
I6:	78L05 (various manufacturers)
T1, T7:	BF 245
T2:	BF 960
T3...T5:	BC 308 or pnp equiv.
T6:	BC 238 or npn equiv.
D1, D2:	BB 505 B (approx. 2...11 pF)
D3:	1N 4148 or Si. equiv.
C1, C2, C4, C5:	Trimmer 2...30 pF, red, RM 5 mm (Valvo)
C3:	Cer. Trimmer 1...6 pF, multi-turn
C6:	low-loss, styroflex, polypropolane etc.
L1:	4 turns tapped 1.5 turns from cold end
L2:	4 turns
L3:	4 turns tapped 1 turn from cold end
L4:	4 turns

Note: Inductors L1...L4 are to be wound with 0.8 mm silvered wire, L3 ist to be wound on a 6 mm former with 1 mm silvered wire

L5:	10 turns Cu.lacq. 0.3 mm wire wound on 27 kΩ resistor of 3 mm dia.
L6, L7:	Fixed inductor with ferrite core (e.g. Siemens)
FB:	Ferrite bead
Q1:	24.576 MHz fundamental crystal
Q2:	10.24 or 10.245 MHz fundamental crystal
Q3:	10.7 MHz fundamental crystal

Note: For a 9 MHz IF, Q3 should be 9 MHz and Q2 should be either 11.94 or 12.0 MHz

P1, P2:	Preset pot'meter RM 5/7.5/ 2.5 mm
P3:	10-turn potentiometer with panel scale 0...10
P4:	Preset pot'meter, carbon film, RM 10/5 mm (Piher)

Note: All resistors marked 1 % are to be metal-film with TK = 100 ppm/°C, or better 0.1 % with TK = 50 ppm/°C.

All feed-thro' capacitors are approx. 1 nF, solderable.

The 4 feed-thro's are PTFE.

The tin-plate box is 74 x 111 x 30 mm with two covers and is fitted with a compartment divider wall 20 x 109 mm and 4 sub-dividers 20 x 47 mm. An internal cover 22 x 47 mm should also be provided for the VCO stage.

10. REFERENCES TO PART 2

(1) Oppelt, Ralph, DB 2 NP:
The Generation and Demodulation of SSB Signals using the Phasing Method.
VHF COMMUNICATIONS 19 (1987),
Edition 2, Pages 66 - 72
Edition 3, Pages 130 - 140

(2) (not mentioning the author)
4-MHz-Frequenzzähler
Elektor, Edition 6/88, P. 20 - 21

Wolfgang Schneider, DD 2 EK

FM-ATV in the GHz Range
Part 2: Sound-Carrier Circuits and Tuning-Voltage DC Converter

Part 1 of this article about FM-ATV in the GHz range (1) described an FM-ATV transmitter for the 23 cm band. This second, supplementary article, introduces the sound-carrier circuitry and also a DC converter to generate the tuning voltage from a 12 volt source for application to the varicap diodes.

1. THE SOUND-CARRIER CIRCUITS

In order to convey speech information over an ATV link, a frequency-modulated sound carrier at 5.5 MHz is required. This sound subcarrier is modulated together with the video signal in the FM-ATV sender's VCO. The simple circuit suitable for this purpose is shown in **fig. 1**.

1.1. Circuit Description

The sound signal from the microphone is taken via a single-stage pre-amplifier on to a gain-controlled stage using a μA 741 integrated circuit amplifier. At the output of this IC, a portion of the signal is capacitively taken off to a diode rectifier. The DC voltage is then filtered and amplified and is used as the control voltage for the AF amplifier.

The heart of the sound-carrier circuit is the VCO which is a voltage-tuned colpitts oscillator

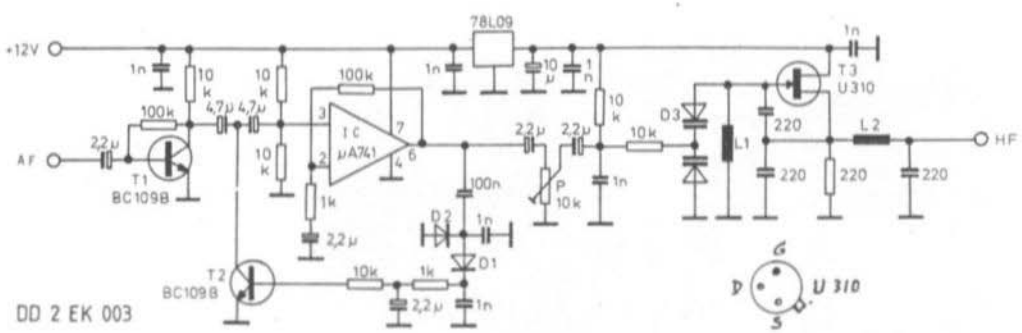


Fig. 1: Circuit schematic of sound carrier

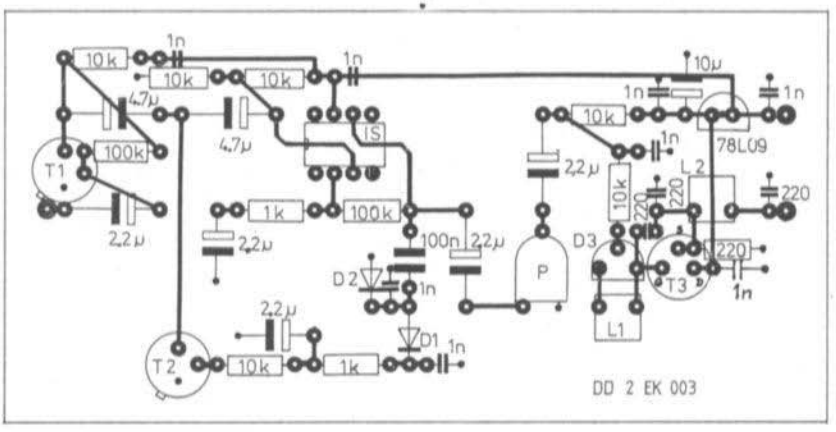


Fig. 2: Component layout of sound-carrier board DD 2 EK 003

working at 5.5 MHz. The frequency-determining parallel tuned-circuit consists of an 8 µH inductor and a double tuning-diode BB 204 B. Owing to the BB 204 B's constructional characteristics (two back-to-back diodes in a single encapsulation), the necessary large capacity variation range is produced and the otherwise capacitive separation of the tuning voltage and the AF signal from the rest of the oscillator circuit, is rendered superfluous.

Both diodes are DC-referenced to a fixed voltage of + 9 V. The amplified signal is applied at this point. The potentiometer serves to adjust the frequency deviation of the ATV sub-carrier sound.

An U 310 is used for the oscillator transistor. At the FET's source the modulated 5.5 MHz signal is taken, via a low-pass filter, to the output at a power of some 3 mW.

1.2. Construction

The printed circuit board DD 2 EK 003 consists of a two-sided 1.5 mm thick epoxy-glass material

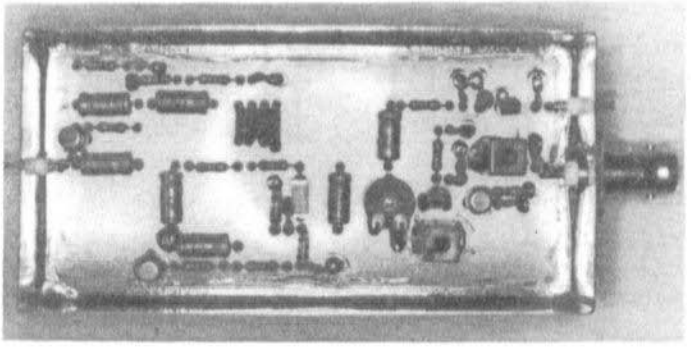


Fig. 3: The completed sound-carrier unit

and of dimensions 53.5 x 108 mm which fits into a proprietary 111 x 55.5 x 30 tin-plate box. After the holes for the small components have been drilled, the component side holes, which are not passing ground leads, are slightly counter-sunk in order that the copper plating is removed from around the circumference of the hole.

When these preparations are ready, the board can be sprayed with anti-corrosion solution. The board is equipped with components only after it has been soldered into the enclosure. **Figure 3** shows the prototype unit.

1.3. Components

T1, T2:	BC 109 B, BC 413, BC 550 or equiv.
T3:	U 310 (Siliconix)
IC:	µA 741
D1, D2:	AA 119 or equiv.
D3:	BB 204 B
L1:	8 µH inductor (Neosid BV 5800, gn/rd)
L2:	1 µH inductor (Neosid BV 5048 ye/gn)
1 x	voltage regulator 78L09
5 x	Elko 2.2 µF/25 V (10 mm grid)
2 x	Elko 4.7 µF/25 V (10 mm grid)
1 x	tantalum pearl cap. 10 µF/25 V
1 x	100 nF (7.5 mm grid)
1 x	10 kΩ preset (10 mm grid)
1 x	tin-plate box 111 x 55.5 x 30
1 x	BNC panel skt. UG-290A/U
2 x	PTFE feed-through

Ceramic disks, 2.5 mm grid:
3 x 220 pF; 7 x 1 nF

Resistors (10 mm grid):
1 x 220 Ω; 2 x 1 kΩ, 6 x 10 kΩ, 2 x 100 kΩ

2. THE DC-DC CONVERTER

2.1. Circuit Description

The circuit in **fig. 4** represents that of a DC-DC converter which supplies the VCO varicap diode with a tuning voltage of about 24 V. The circuit functions with an oscillator frequency of 40 kHz which is determined by the external circuitry to an NE 555. The following high-speed switching transistor drives the storage inductor L1. This inductor has an air-grapped pot-core (A_L = 250) wound with 70 turns of 0.2 mm lacquered copper wire (CuL). The 40 kHz output waveform is rectified and filtered and then applied to a preset potentiometer. The maximum voltage output is limited by the zener diode D1 to 30 V.

2.2. Construction

The DC-DC converter is, as all the other boards in the FM-ATV transmitter, mounted on a two-sided epoxy-glass PCB, DD 2 EK 004, with dimensions 53.5 x 72 x 1.5 mm (**fig. 5**).

The preparation and drilling follows the lines of the sound-carrier board. The board is drilled etc. and then mounted in its housing. The components are then mounted and soldered in. **Fig. 6** shows the prototype of the DC-DC converter.

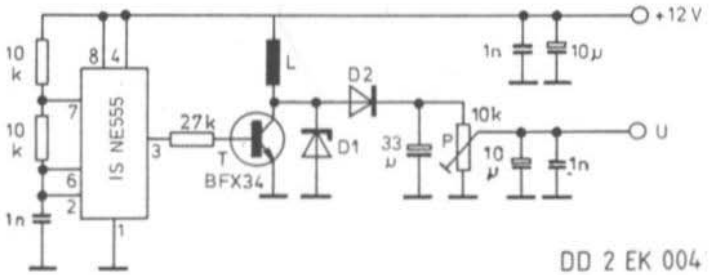


Fig. 4: Circuit schematic of DC-DC converter

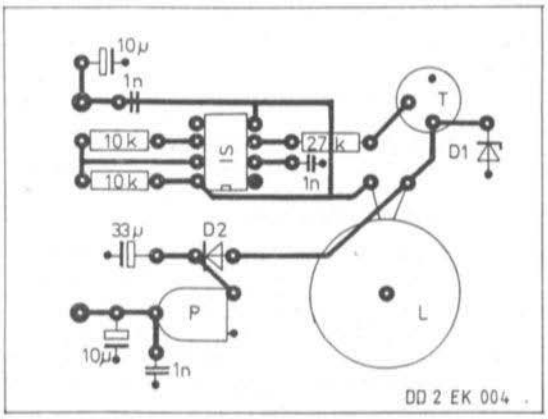


Fig. 5:
Component layout of DC-DC converter DD 2 EK 004

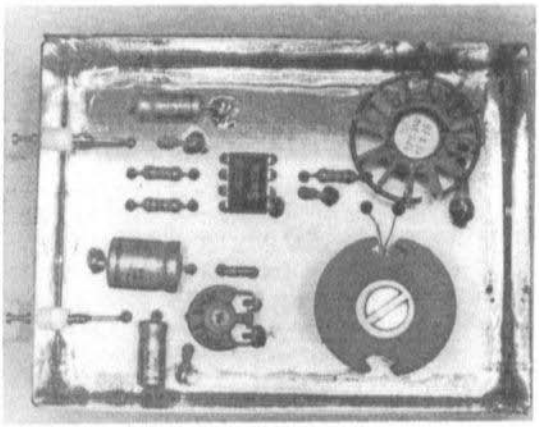


Fig. 6:
The completed DC-DC converter unit

2.3. Components

T1: BFX 34 or equiv.
IC: NE 555
D1: zener diode 30 V/1.3 W
D2: diode 1N 4148
L1: inductor: 70 turns, 0.2 CuL on pot-core 21 Ø x 13 mm (A_L = 250)
1 x Elko 33 µF/40 V (10 mm grid)
2 x Elko 10 µF/40 V (10 mm grid)
1 x preset 10 kΩ (10/5 mm grid)
2 x resistor 10 kΩ (10 mm grid)
1 x resistor 27 kΩ (10 mm grid)
3 x ceramic capacitor 1 nF (2.5 mm grid)
1 x tin-plate box 74 x 55.5 x 30
2 x PTFE feed-through

3. REFERENCES

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FM-ATV in the GHz Range.
Part 1: 23 cm Transmitter
VHF COMMUNICATIONS 21 (1989), ed. 1, p. 25 - 30

MATERIAL PRICE LIST OF EQUIPMENT

described in edition 1/1989 of VHF COMMUNICATIONS

DD2EK 002	**23 cm Band FM-ATV Transmitter (Part 1)**		**Art.Nr.**		**Ed. 1/1989**
PCB	DD2EK 002	two-sided, silvered, drilled	6150		DM 28.–
Components	DD2EK 002	2 transistors, 1 Avantek amp. 1 Plessey IC, 2 volt regs. 4 diodes, 2 RFC's, wire, 1 foil cap., 22 ceramic caps., 3 el. caps., 2 presets, 20 resistors, 1 tin-plate box, 6 PTFE feedthro's, 1 BNC socket.	6151		DM 117.–
Kit	**DD2EK 002**	**without crystal but with all listed parts**	**6152**		**DM 145.–**
Crystals for	DD2EK 002	please give desired frequency!	6153	ea.	DM 46.–
DD2EK 003	**23 cm Band FM-ATV Transmitter (Part 2)**				**Ed. 1/1989**
	Sound carrier				
PCB	DD2EK 003	two-sided, silvered, drilled	6154		DM 24.–
Components	DD2EK 003	2 transistors, 1 IC, 3 diodes, 2 coils, 1 volt. regulator, 8 elkos, 1 ceramic cap., 1 preset, 11 resistors, 1 tin-plate box, 1 BNC socket, 1 PTFE feedthro.	6155		DM 70.–
Kit	**DD2EK 003**	**complete with listed parts**	**6156**		**DM 89.–**
	Voltage converter				
PCB	DD2EK 004	two-sided, silvered, drilled	6157		DM 22.–
Components	DD2EK 004	1 transistor, 1 IC, 2 diodes, 1 pot-core, 5 m CuL wire 0.2 mm, 3 elkos, 3 cer. caps., 1 preset, 3 resistors, 1 tin-plate box, 2 PTFE feedthro's, 1 heat sink	6158		DM 46.–
Kit	**DD2EK 004**	**complete with listed parts**	**6159**		**DM 64.–**
DB2NP 002	**2 m SSB Band VFO**				**Ed. 1/1989**
PCB	DB2NP 002	two-sided, silvered, drilled	6146		DM 29.–
Components	DB2NP 002	6 ICs, 7 transistors, 3 diodes, 1 glass-tube trimmer, 4 foil trimmers, 40 cer. caps., 2 el. caps., silv. wire, 2 RFCs, 5 ferrite beads, 10-turn pot. without scale, 2 multi-turn-, 1 norm. preset pot., 10 MF-, 23 norm. resistors, 4 PTFE feedthro's, 7 feedthro. caps., 1 tin-plate box, 4 sheet metal strips, 3 crystals (for 9 or 10.7 MHz IF)	6147		DM 195.–
Kit	**DB2NP 002**	**with listed parts**			
		for 9 MHz IF	**6149**		**DM 225.–**
		for 10.7 MHz IF	**6148**		**DM 224.–**

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- High-resolution picture transmission on monitor or printer
- Monochrom (black/white), grey-scale or colour representation
- Automatic phasing
- Manual phase readjustment without information loss
- Automatic picture transmission (APT)
- Automatic picture control store and load
- Zoom to different formats
- Inverse scan direction (ISD)
- Installed graphic editor for post processing
- File formats and technical information available

Applications:

- Amateur radio
- Maritime radio
- Press reports
- Professional monitor stations

Hardware configuration:

- ATARI ST or compatible PC with at least 1 Mbyte RAM
- Appropriate SSB-receiver, transceiver, satellite-receiving system
- Standard converter AFUSOFT MPSK equipped for SSTV and other picture modes

Options:
Printer, harddisk and plug-in modules (OPTION BOARDS) which fit into the MPSK.

	Art.No.	Price
PC-RADIOFAX incl. converter MPSK and handbook	5800	DM 950.00
PC-RADIOFAX for ATARI ST, incl. MSPK and handbook	5810	DM 966.00

Ask for our DEMO DISK (DM 20.00).Payment in advance please.

PC/SAT Weather Satellite Reception on a PC/AT

For the First Time!
Reception and processing of weather satellite pictures on any standard PC/AT or a compatible.

HARDWARE

- Antenna for 1.7 GHz (Yagi antenna with dipole or 90 cm offset parabolic antenna).
- Low-noise 1.7 GHz preamplifier (special pre-amplifier with only a 1.2 dB noise figure and a gain of 38 dB).
- Down-converter/receiver for RF translation and demodulation of the satellite's signal.
- PC/SAT interface - slots easily into a free AT/XT expansion-slot.
- PC/AT or compatible with the following basic equipment:
  - 286-processor
  - 640 kbyte and 1 Mbyte (min.) extended memory
  - Hard disk drive with at least 6.5 Mbyte free
  - EGA card or higher
  - EGA monitor

User-friendly SOFTWARE

written in C and Assembler 286

- Automatic reception
- Reception schedule:
  The reception menu contains all METEOSAT transmissions listed with both time and format. Automatic reception by simply "klicking it up".
- Picture format
  All pictures are stored on the hard disk in full format. There are three picture presentation formats:
  - 800 x 800 full resolution
  - 640 x 350 reduced resolution
  - 640 x 350 geographically corrected
- Zoom/histogram
  The pictures may be enlarged up to a factor at x10. A histogram is computed for the selected sector.
- Colour
  A colour table comprising 50 selectable colours is available for various picture spectral ranges.
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We would like to introduce the English edition of the well-known **"UHF-Unterlage"** from **Karl Weiner, DJ 9 HO.**

THE UHF-COMPENDIUM

Interesting for all active and technically minded Radio Amateurs

The book contains sufficient theoretical material to provide the relevant background information and to explain the operation of the equipment described in the building section. Special emphasis has been placed upon the construction of GaAs FET pre-amplifiers and converters as well as power amplifiers and antenna systems for the 70 cm and 23 cm bands. Great attention was paid to diagrams of measuring equipment and tuning aids. Consequently, there are suggestions for the construction of simple alignment tools, power measuring equipment, a fixed frequency generator for receiver alignment, a UHF dipper, a panoramic receiver and a swept frequency generator. Practically all constructional projects have been verified and optimized using present standard test equipment such as generators and spectrum analyzers.

Part 1 and 2	**Art.No. 8054**	**DM 45.00**
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The DB 1 NV Spectrum Analyser

(VHF Communications 3 and 4/1987)

Specifications:

Frequency range:	0 - 500 MHz (1000 - 1500 MHz image)
Sensitivity:	– 100 dBm
IF bandwidth:	1 kHz / 3 kHz / 10 kHz / 50 kHz / 300 kHz
Video bandwidth:	100 Hz / 1 kHz / 10 kHz / 100 kHz
IM-free dynamic range:	≥ 60 dB
Display bandwidth:	10 / 20 / 50 / 100 / 200 kHz / per cm 0.5 / 1 / 2 / 5 / 10 / 20 MHz / per cm also 0 - 500 MHz screen display
Input attenuator (built in):	0...70 dB in 10 dB steps (DC-2 GHz)

Special Features:

The video filter can be automatically switched to accommodate the selected IF bandwidth. When displaying ≤ 200 kHz/cm, PLL stabilization of the 1st local oscillator may be switched in.

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Frequency range	500 kHz – 90 MHz		5 – 30 MHz	8 – 30 MHz	4 – 50 MHz
Adjustment tolerance	± 1 ppm to ± 20 ppm dependant upon model		–	–	Overall tolerance ± 25 ppm to ± 1000 ppm dependant upon model
Pull-in range	–		± 50 ppm (0,25 – 4,75 V)	± 130 ppm (5 V)	–
Temperature stability	±2,5 ppm, 0 ... + 50 °C to ± 50 ppm, – 55 ... + 105 °C dependant upon model		≤ ± 20 ppm at – 40 ... + 90 °C	≤ ± 20 ppm at - 40 ... + 90 °C	0 ... + 70 °C to - 55 ... + 100 °C dependant upon model Tolerance, see above
Current consumption	35 mA (3 – 90 MHz) 60 mA (less than 3 MHz) at 5 V		35 mA max.	10 mA max.	50 mA max.
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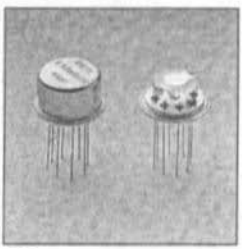

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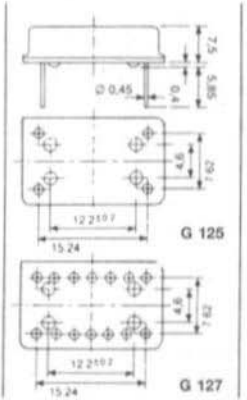

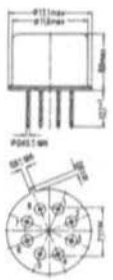

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