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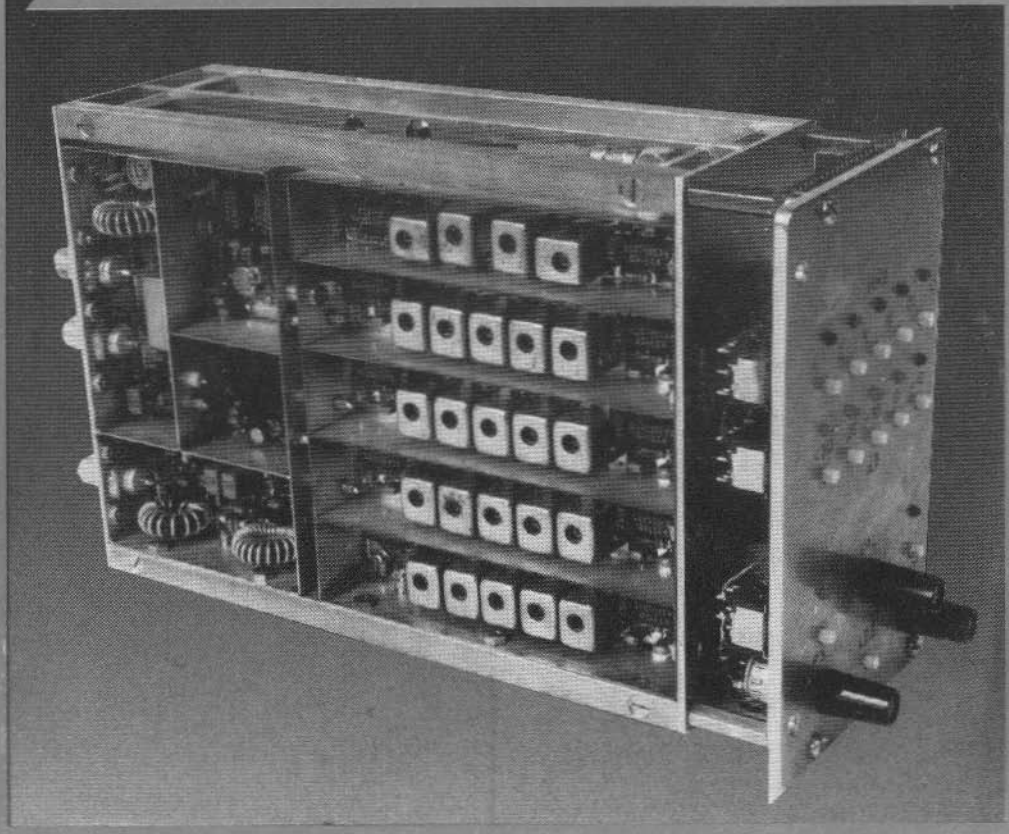
A Publication for the Radio-Amateur

Especially Covering VHF, UHF and Microwaves

VHF communications

Volume No. 19 · Spring · 1/1987 · DM 7.00

Selective Short-Wave Receiver Front-End by DK 1 OF



VHF communications

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Volume No. 19 · Spring · Edition 1/1987

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Contents

Home-Constructed Frequency Counter, Part 2, by D. Schwarzenau and B. Kokot.

Unfortunately, it was not possible to fit the second (concluding) part of this article into this edition as promised but it will definately be included in the summer edition.

With apologies, editor.

UKWberichte Terry D. Bittan · Jahnstr. 14 · Postfach 80 · D-8523 Baiersdorf
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Joachim Kestler, DK 1 OF

PLL Oscillators with Delay Lines
Part 5: Digital Frequency Tuning

The method of tuning originally described for the delay-line oscillator in (1), i. e. manual tuning with a knob, may well be the optimal solution for conventional radio operation. In order to take advantage of the latest communication techniques (under the control of the station computer), it is desirable that receiver operating features such as the mode, bandwidth and frequency etc. should be accessed by a computer. Whilst commercial amateur equipment increasingly employs more standardized interfaces, this aspect has been almost ignored by the home constructed equipments.

As already mentioned many times in the course of this series of articles, this PLL delay-line oscillator (2), (3) is inherently suitable for remote control operation. This present article describes a module which surplants the (expensive) sine / cosine potentiometer in the control of the oscillator DK 1 OF 046 in the following two ways: –

- **Manual tuning up / down, each with four available tuning speeds**
- **A selected frequency (reference value) is compared with the counted oscillator frequency (actual value) with continuous updating of the oscillator tuning.**

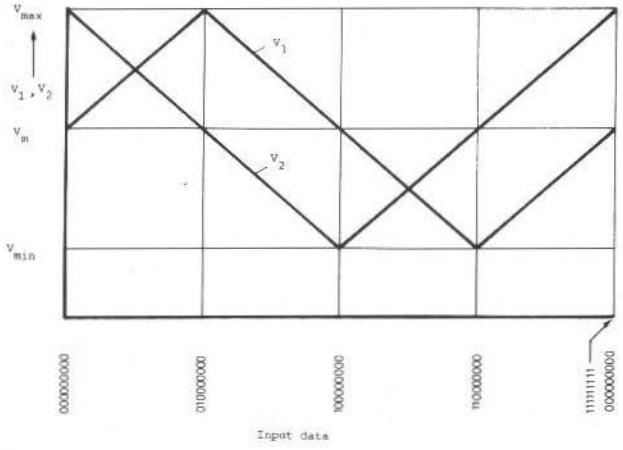

Fig.35:
Control voltages V_1 and V_2 dependent upon input data

7.1. A Little Theory

In part 1, paragraph 1 of this series, it was explained that a full turn of the phase shifter knob amounted to a tuning interval of 1 / 64 μs $\triangleq$ 15.625 kHz (fig. 8 in (1)). If the sine / cosine potentiometer is to be replaced with a digital to analogue converter (DAC), a natural question to ask is, what would be the tuning resolution then? That is, what would the smallest tuning step have to be? A tuning step of 10 Hz would be desirable for both SSB and RTTY and so one revolution of the tuning knob would encompass 1500 steps. Of course, there are suitable fine tune DACs available but they are somewhat specialized and therefore expensive.

If an 8 bit DAC (μP - standard) was used, the tuning intervals would be 15625 Hz divided by 512 steps which yields a resolution of 30.5 Hz. This value seems to be sufficient, moreover, the possibility exists to have in addition, an analogue interpolation (potentiometer P 2 fig. 19 in (2)) carried out with a further DAC, also digitally controlled.

It will have occurred to the attentive reader that 512 steps would be obtained from an 8 bit DAC i. e. $2^8 = 256$. It will be clear, however, from the study of **fig. 35** that the total output voltage range of each DAC will be traversed twice, once with rising values and once with falling values. Therefore, there are, in fact, twice the number of increments available 2 x 256 = 512.

The sine / cosine characteristic of the control voltage depicted in fig. 8 must not necessarily be adhered to, the more natural linear ramp of the DAC can be used instead. The frequency steps, it is true, would not be constant along the tuning curve but the departures amount to a few percent only, which in practice is of no importance. Certainly, a network of diodes and resistors could be used to approximate the sine characteristic, and this was tried, but in my opinion the effort was not justified. Besides, there is a risk that the temperature influence upon the diodes could result in an unnecessary degradation of the oscillator's frequency stability capability.

7.2. Circuit of Frequency Control Unit

First of all, the block diagram is shown in **fig. 36**. The reference frequency is one input and the counter readings representing the oscillator frequency and both being fed to the digital com-

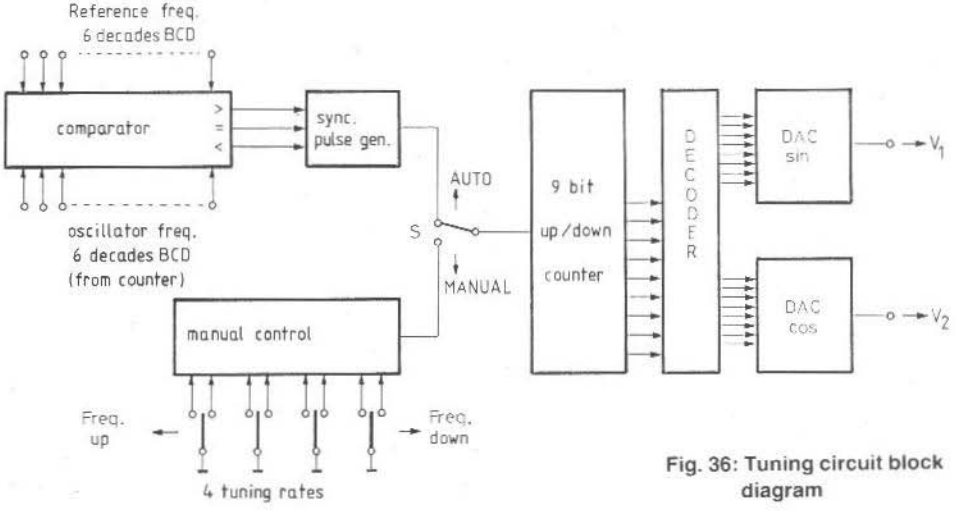

Fig. 36: Tuning circuit block diagram

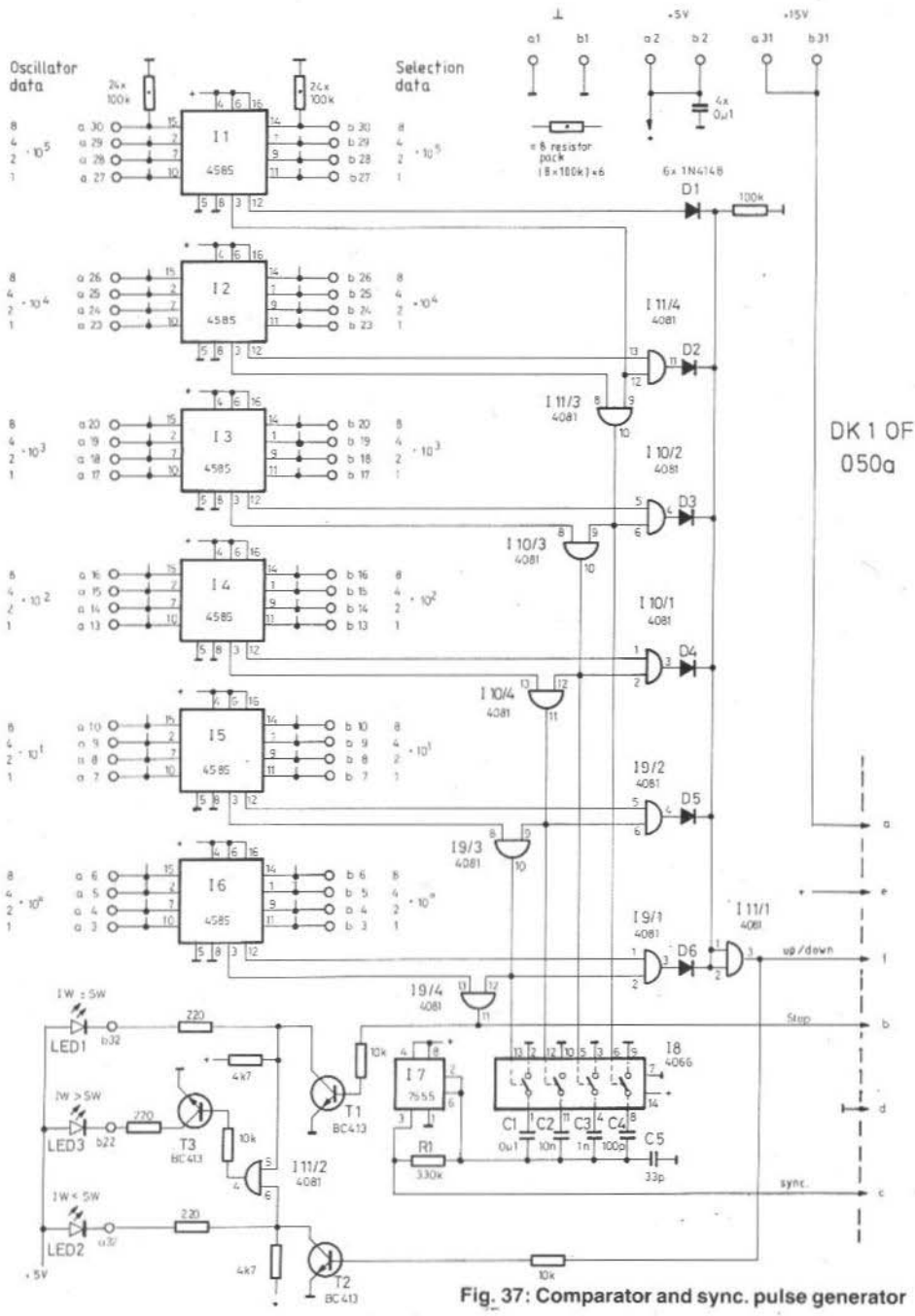

Fig. 37: Comparator and sync. pulse generator

parator in the BCD code. The BCD code was chosen in order that it would be compatible with existing frequency counters. The reference frequency must also be fed in BCD e. g. via character switches or a computer parallel output with 24 bit (6 decades each of 4 BCD bits). The outputs of the comparator (too high – correct – too low) are synchronized with a sync generator which is connected to an up / down 9 bit binary counter via a change-over switch S. The direction of the count depends upon the magnitude of the counter frequency relative to that of the reference frequency. The binary counter outputs are decoded by gate circuits in such a way that the following D / A converter gives voltages V_1 and V_2 in accordance with **fig. 35**.

If the switch S is set to MANUAL the unit is controlled by hand via a push button. The frequency can be adjusted upwards or downwards with four set tuning rates at the operator's disposal.

In order to obtain a better overall view, the detailed circuit diagram was split into three parts. **Fig. 37** shows the digital comparator with its 2 x 24 BCD inputs for frequency and reference (I 1 to I 6) together with the sync. generator I 7. The circuit of I 8 has the task of switching over the sync. frequency, derived from I 7, according to the degree of correspondence at the digital inputs. This accomplishes a fast regulation when the frequency departure from the reference is large. The fine tuning, on the other hand, (differences only in low-weighted decades) must be carried out slowly enough to allow the counter to follow other frequency inputs during the correction process. The circuit would otherwise be unstable i. e. hunt around the correct value.

When all the decades indicate correspondence the output of the gate I 9 / 4 goes high and the binary is stopped via connection b. T 1 then switches on LED 1 which indicates that a regulated condition has been achieved. If correspondence is not achieved either LED 2 or LED 3 is activated according to whether the frequency is smaller or larger than the reference.

Now taking **fig. 38**. Above right is an astable multi vibrator with gates I 13 / 3 and I 13 / 4. It oscillates at about 8 kHz fixed by R 2 and C 6. This frequency is now divided in I 12 by 2^{12} (4096) producing a rectangular 2 Hz pulse at pin 1. All in between values (4, 8, 16, 32 Hz etc.) are available at the "tapping points" of I 12.

Nearby on the left, five RS flip-flops may be recognized. These have been made from the gates of I 15, I 14 and the remaining half of I 13. If, for example, the switch S is momentarily switched up to "AUTO", the top RS FF flips over to its working position, the divider I 12 receives a short reset pulse via D 19 and C 8 and begins to count upwards from zero. After 4096 sync. pulses (i. e. half a second later) a full cycle has been counted and a negative going pulse appears at I 12 pin 1. This flips back the RS flip-flop via C 9 to its original position (if S 1 has already been released). The 9 bit binary counter receives a single synchronizing pulse via I 17 / 3, D 15, I 19 / 3, D 23 and terminal C which knocks it to a further place and with it the oscillator frequency another approx. 30 Hz higher. Accordingly, the same thing occurs when one of the other switches (S 2, S 3 or S 4) is operated. The difference is, however, that not one sync. pulse is released but a whole packet (according to the tapping of I 12's pins determining the frequency) of counting pulses is let out. Using the bridges shown dotted in **fig. 38**, the following values may be obtained:

Switch	No. of counter pulses	Frequency step
S 1	1	30.5 Hz
S 2	16	488 Hz
S 3	256	7.81 kHz
S 4	4096	125 kHz

If a key switch is continuously depressed, the relevant flip-flop will remain in its active condition, the reset pulse being ignored. In this case a stationary square wave pulse will be given at C and the oscillator frequency runs continuously higher.

If the key is switched down, as well as the appropriate flip-flop being set, the lowest flip-flop (I 13 / 1 and I 13 / 2) will be primed in addition. The 8 bit counter receives then the command (via I 19 / 4, D 25 and terminal D) to start counting in the oppo-

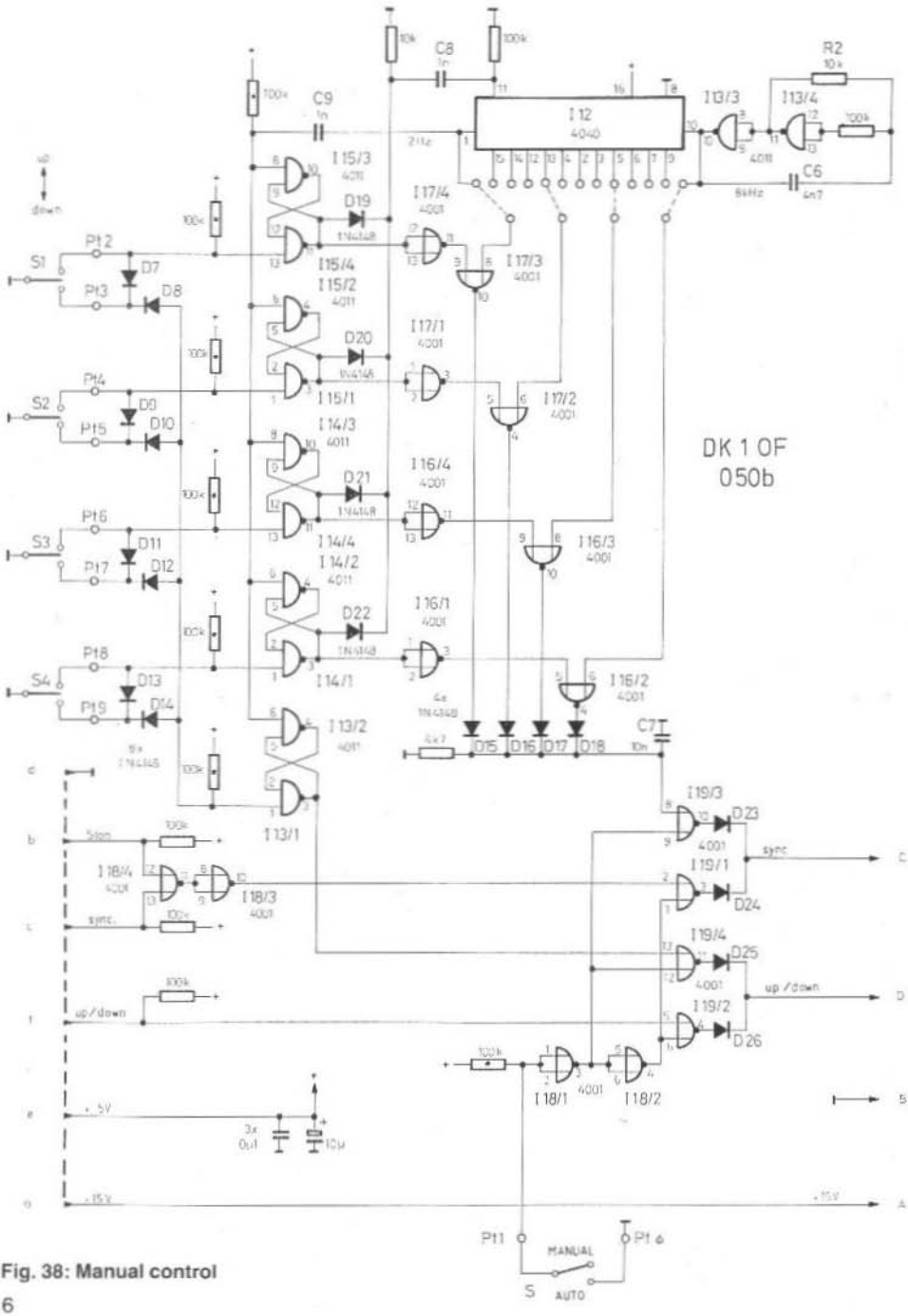

Fig. 38: Manual control

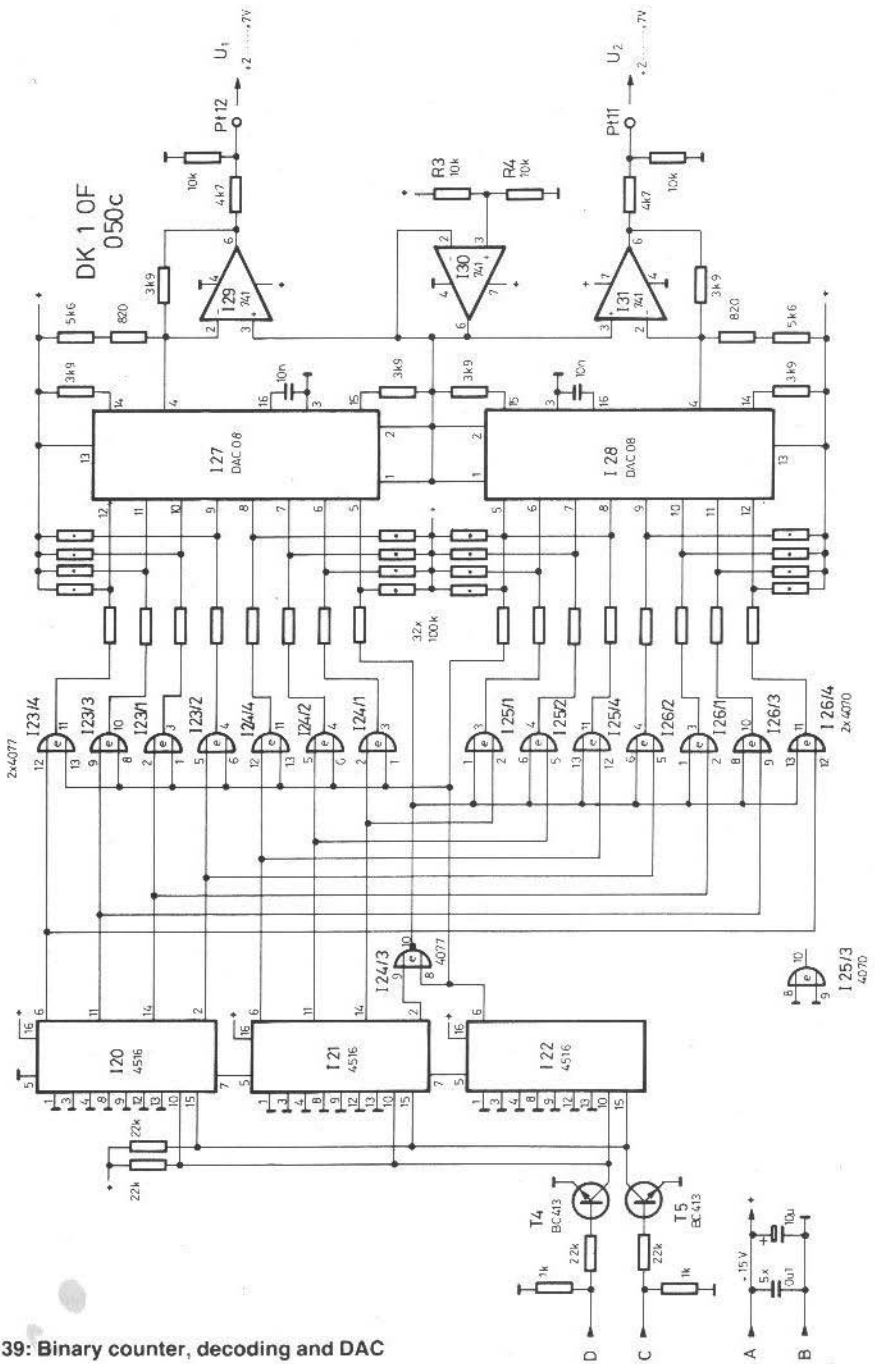

Fig. 39: Binary counter, decoding and DAC

site direction thus sending the oscillator frequency in a downward direction. The capacitor C 7 delays the counting pulses in order that time is given for the counting change of direction. The change-over key MANUAL / AUTO is effected by gates I 19 / 1 to 4 together with I 18 / 1 and 2. The supply voltage to all of the circuits so far described is + 5 V.

The remaining stages of the circuit are shown in **fig. 39**. I 20, I 21, and I 22 form the 9 bit binary counter and this part of the circuit being supplied with + 15 V, T 4 and T 5 taking care of the voltage level change for the sync. and change-over signal. The binary value decoding (to get the DAC data as in **fig. 35**) is carried out by the exclusive-or or exclusive-nor circuits of I 23 to I 26.

The D / A converters (family DAC 08 ...) are usually supplied with a bipolar norm of ± 5 V. As negative voltages are not always available, an artificial mid-point of the ± 15 V supply has been provided by dividers R 3 / R 4 and voltage follower I 30 acting also as ground for I 27 and I 28. The voltage ange for the DAC's data inputs lies therefore between + 7.5 V (L) and + 15 V (H) the necessary level matching being provided by the 16 voltage dividers using 100 kΩ resistors. As the DAC outputs (pin 4) are designed for a current control, a current / voltage converter (I 29 and I 30) is required for each channel and is associated with each of the resistor dividers. The phase shifter's (module DK 1 OF 046) control voltage is available at terminals Pt 11 and Pt 12 at a suitable voltage level.

7.3.Construction

A double-sided, through-contacted printed circuit board, etched on both sides, has been developed for this project. It has the European format of 160 mm x 100 mm and is available from the publishers under the designation DK 1 OF 050. It can be fitted with a 64 pole multi-way plug. The standardized numbering of the plug agrees completely with fig. 37 but terminals Pt 0 to Pt 12 (figs 38 and 39) are not connected via this plug, a separate plug being employed. If only the manual operation is required, the automatic part of the circuit (of fig. 37) may be omitted from the PCB, or simply cut off, in order to save space. **Figure 40** shows the component plan for the circuit in its entirety.

Components

T 1, T 2, T 3, T 4, T 5:	BC 413 or similar
all diodes:	1 N 4148 or similar
I 1, I 2, I 3, I 4, I 5, I 6:	CMOS 4585 B or 40085 B
I 7:	7555 (Intersil, MOS version of 555)
I 8:	CMOS 4066 B
I 9, I 10, I 11:	CMOS 4081 B
I 12:	CMOS 4040 B
I 13, I 14, I 15:	CMOS 4011 B
I 16, I 17, I 18, I 19:	CMOS 4001 B
I 20, I 21, I 22:	CMOS 4516 B
I 23, I 24:	CMOS 4077 B
I 25, I 26:	CMOS 4070 B or 4030 B
I 27, I 28:	DAC 08, DAC 0800 (designation according to manufacturers)
I 29, I 30, I 31:	Op. amp. 741 C, 8 pin DIP housing
Multi-way plug:	Siemens form C, DIN 41612, 64 way e. g. C 42334 - A 191 - A 521
Multi-way skt.:	e. g. C 42334 - A 192 - A 521, Siemens
Electrolytics:	10 µF / 25 V spacing grid 5 mm
Other caps:	Ceramic discs or multilayer, spacing 5 mm
Resistor with spot:	8 x 100 kΩ, 0.1 W spacing 2.54 mm (x 9)
other resistors:	≥ 1 / 8 W spacing 10 mm
Accessories:	
LED 1, LED 2, LED 3:	LEDs
S 1, S 2, S 3, S 4:	4 double or 8 single push buttons
S:	SPST change-over switch

Stabilized supplies of 5 V at 45 mA (without LEDs) and + 15 V at 20 mA are required. The photograph of **fig. 41** shows a completed board.

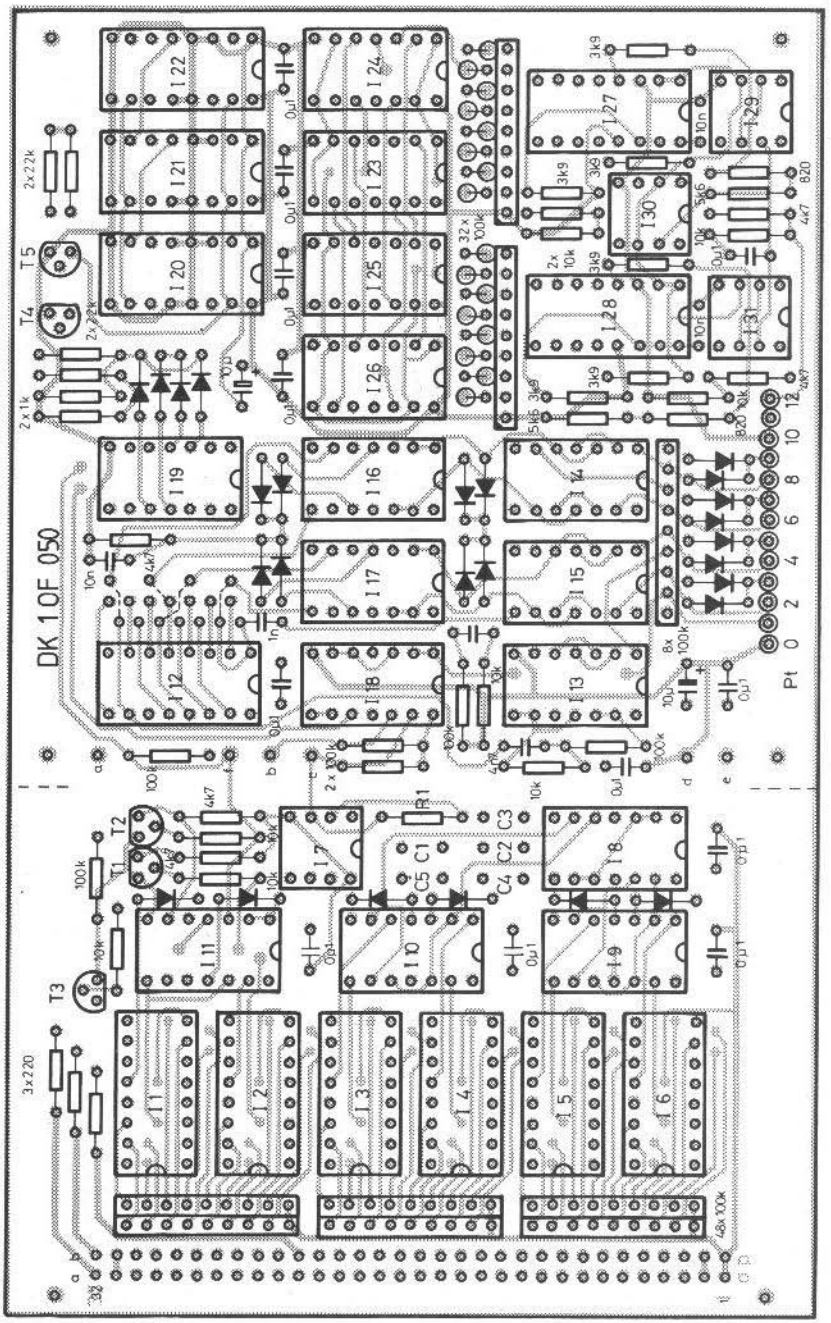

Fig. 40: Component layout plan of PCB DK 1 OF 050

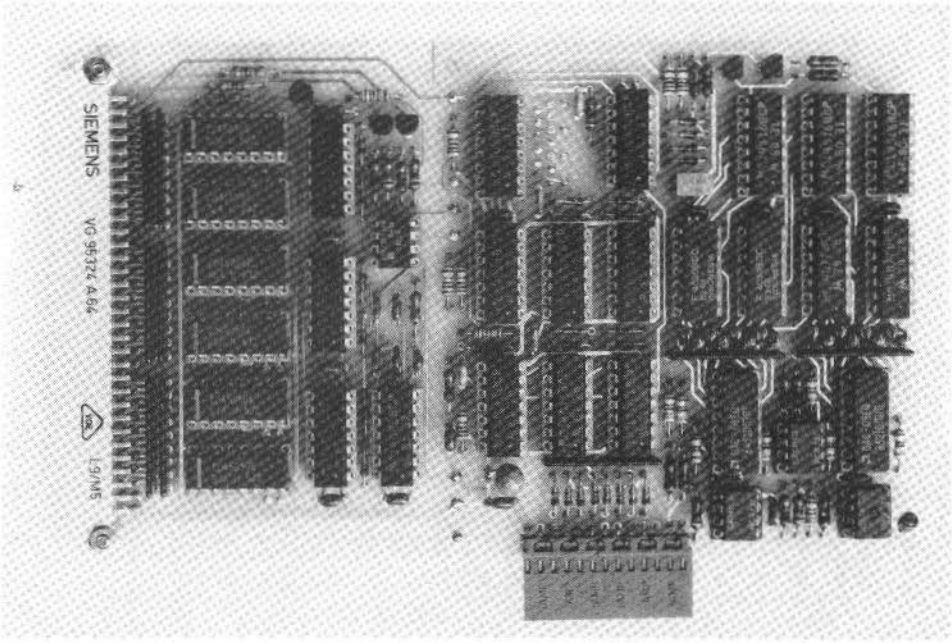

Fig. 41: An example of a completed DK 1 OF 050 board

7.4.Commissioning

Following the connections of the external components, S 1 - S 4, switch S and the three LEDs, the supply potentials can be applied. Switch S should be switched to MANUAL to start with. An oscilloscope connected to pin 10 of I 12 should show a clean square wave signal of 5 Vpp at 8 kHz, the exact frequency being uncritical. The 2 Hz signal at pin 1 can be observed with a voltmeter if an oscilloscope is not available. If now, one of the button switches is depressed, momentarily the "packet of pulses" referred to in paragraph 7.2. will be displayed at point C or at the collector of T 5. A continuous application of the push button will produce a contiuous square wave train. If the switch is now flipped to the other side, the logic level at D (or T 4's collector) will change. Finally, the oscilloscope is connected to Pt 12. Pressing S 4 will result in a triangular waveform trace at about 16 Hz repetition frequency, the voltage maxima is + 7 V and the minima is + 2 V (tolerance ± 0.5 V). The trace must look smooth, each ramp consisting of 256 equal steps. Any kinks or large steps would indicate a fault in the binary counter, the decoder, or in the DAC which must be found and corrected (perhaps a defective chip, solder bridge on the PCB or a forgotten soldered connection etc.) Such a fault would render the oscillator impossible to tune contiuously. This test must also be applied to the second channel (terminal Pt 11).

If an oscilloscope is not available, then all 512 stages must be slowly selected (with S 1) and the voltage steps noted at Pt 11 an Pt 12 with a voltmeter.

Now the outputs of the module can be connected to the terminals Pt 9 and Pt 10 of the oscillator module DK 1 OF 046 and set into operation. Switches S 1 to S 4 should be in operation. Crossing the control lines will result in an inversion of the tuning direction.

Now the switch S is flipped to position AUTO. The data inputs from the actual and reference frequency are open for the time being (this represents no danger for the comparator owing to the pull-down resistors). LED 1 will glow when the actual frequency is equal to the reference frequency and are both zero. If + 5 V is put on the actual frequency data input, LED 3 will glow and the oscillator frequency will run down (if necessary reverse Pt 11 / Pt 12). The tuning rate depends upon which decade has an H (see para 7.1.). If + 5 V is placed on the reference input, LED 2 glows and the oscillator frequency runs upwards.

Finally, the frequency counter is connected, its BCD outputs being wired up (in the correct order) with the actual value inputs of the comparator. The reference value inputs lead to a set of digital switches which are necessary pending the completion of the comparator interface. If then a value within the tuning range of the oscillator is selected, the automatic function now attemps to tune the oscillator to the frequency called up. If this does not occur and instead a hunting around the selected frequency is observed, then the tuning rate of the loop is too high for the capability of the counter. In such a case, increase the value of R 1 until the selection is achieved normally and there are no further signs of hunting. As the gate time of the counter is the deciding parameter, no more exacting explanations can be given. The values given in **fig. 37** for R 1 and C 5 are optimal for a counter having ten counter up dates per second. A reference jump of 1 MHz would require a selection time of 15 seconds requiring a counter resolution (lowest decimal place) of 100 Hz.

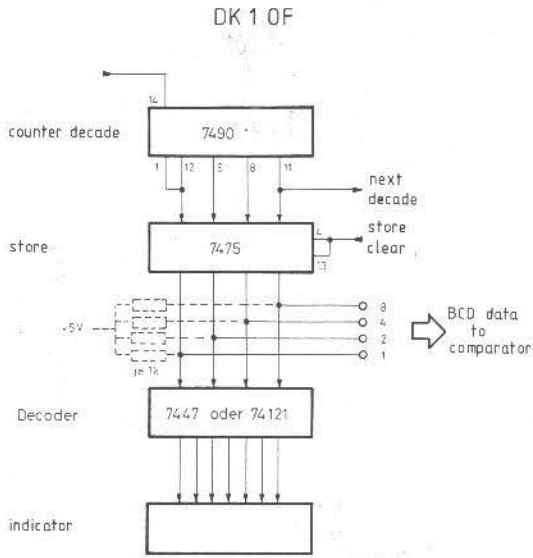

Fig. 42: Extracting the BCD data from the counter

7.5. Suitable Frequency Counters

For the modules described, a suitable counter was designed having a 6 place readout and working to 45 MHz without using a pre-scaler. The printed circuit board is, not as yet, raedy for publication and in any case the publishers of this journal did not want to have yet another frequency counter in their module programme. As will be seen however, it can be done another way.

A suitable discrete component counter is, for example, that of DL 8 TM which uses the old TTL chips. The latch (display store) and the display decoder (for Nixie and seven segment displays) should use separate chips. The block diagram of **figure 42** should clarify the matter. The H level voltage of + 3 to + 4 V offered to the CMOS inputs from the TTL circuits is somewhat too low. It may be just as well, therefore, to connect the TTL outputs with 1 kΩ pull-up resistors which are then tied to the + 5 V rail. This should, in general, be done with all TTL - CMOS transitions.

This practice is also advisable in the case of the latch fitted to the computer counter (5) discussed earlier. **Fig. 43** shows an extract from the circuit, only one indicator circuit is shown but the others are treated likewise. The counter is supplied with + 10 V therefore all the data outputs are supplied with series resistors. These form, together with

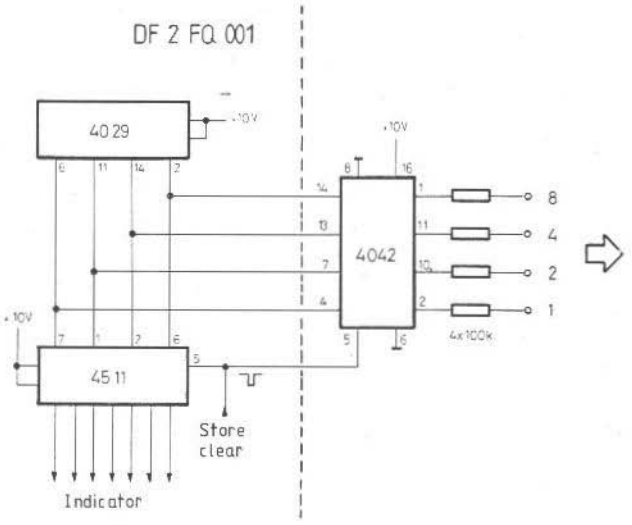

Fig. 43: The BCD outputs from the DF 2 FQ counter

the pull-down resistors at the comparator inputs, a voltage divider which delivers the correct H level of 15 V. The module of DF 2 FQ has a four digit readout which, in general, is sufficient for amateur radio equipments having a resolution of 100 Hz at high frequency and 1 kHz at VHF / UHF. The inputs of both the high value digits remain unswitched.

The counter described in (6) uses an LSI chip which can only be used with extreme difficulty to obtain an output from parallelled BCD data (or the input circuits may be dispensed with). As this has, also, only a four digit readout, it offers no advantage over that described in (5).

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Joachim Kestler, DK 1 OF

A 10 kHz - 30 MHz Receiver Front End Part 1

This article describes a further possibility to use the delay line PLL oscillator of (1) to (5). An associated theme, the single conversion superheterodyne receiver's advantage compared against the double conversion technique of a wideband converter followed by a fixed narrow-range receiver in the context of dynamic range and unwanted spurious signals, was treated in (6).

1. CONCEPT

Professional short wave communications receivers of recent manufacture, without exception, employ an IF which lies well above the highest received frequency – values of 40 to 100 MHz are fairly normal. The single conversion receiver, on account of its large signal handling capabilities, must employ its chief selectivity elements immediately following the mixer. The crystal filter must possess the requisite steep-sided flanks and the minimum bandwidth necessary for the traffic requirements. These filters, on account of their limited production, are only obtainable at comparitively high prices. If four modes of transmission must be optimised in the receiver, for SSB, CW, AM and FM, then the cost threshold may well be exceeded. The use of IF filters intended mainly for VHF, and standardized at frequencies of 9 and 10.7 MHz, does alleviate some of the cost burden but at the expense of another difficulty, namely, the IF lies within the usable range of the receiver. In order to avoid IF breakthrough interference, a rejector circuit must be included before the mixer in order to enhance the insertion loss of the mixer at the intermediate frequency. This creates a ± 100 kHz (approx.) hole in the receiver range capability which is located about the received frequency corresponding to that of the IF.

The low IF, however, does have the advantage that the conversion local oscillator is also working at a low frequency which is favourable for its short-term stability (phase noise).

The block diagram of the receiver front end, using an IF of 10.7 MHz, is shown in **fig. 1**. The switchable input low- and band-pass filter banks ensure that adequate image frequency selectivity is available (image frequency = fr + 2 IF) at 21.4 MHz above the received frequency, whose individual and aggregate power tends to overload the mixer. The actual mixer module has two 35 MHz low-pass filters and a switchable wideband preamplifier located between them. This amplifier may be switched in circuit, for example, when a rod antenna is in use, or out, when using the main station antenna. Directly at the mixer input lies

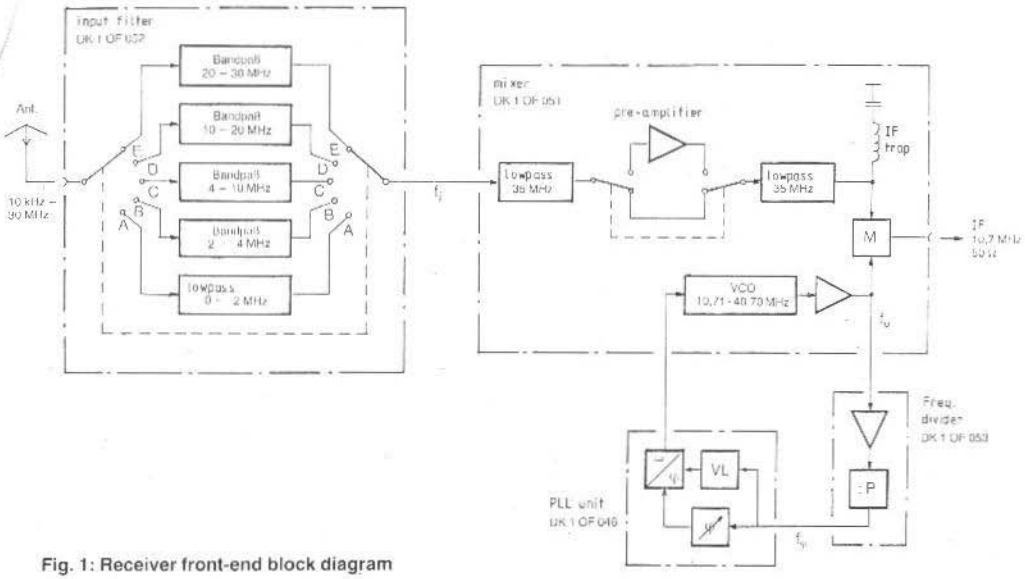

Fig. 1: Receiver front-end block diagram

the IF trap mentioned above. The heterodyne oscillator frequency, always 10.7 MHz above the received frequency, is produced by a voltage-controlled oscillator (VCO) and brought to the correct level to drive a high-level ring mixer by a wideband power amplifier. A small portion of the oscillator power is fed via a buffer stage to a frequency divider where fo is divided by P. The factor P is either 4 or 8 depending on the receiver range switch. See **table 1** below:

Range	fr (MHz)	fo (MHz)	P	fφ (MHz)
A	0 – 2	10.7 – 12.7	4	2.675 – 3.175
B	2 – 4	12.7 – 14.7	4	3.175 – 3.675
C	4 – 10	14.7 – 20.7	4	3.675 – 5.175
D	10 – 20	20.7 – 30.7	8	2.5875 – 3.8375
E	20 – 30	30.7 – 40.7	8	3.8375 – 5.0875

Table 1

Mode	Bandwidth (kHz)	Filter type (KVG)	Terminating impedance (Ω II pF)
CW / RTTY	0.5 at 3 dB	XF – 107 S 172	500 II 30
SSB	2.4 at 3 dB	XF – 107 S 41	200 II 25
SSB	2.5 at 6 dB	XF – 107 S 95	500 II 25
AM	6.0 at 3 dB	XF – 107 S 01	620 II 25
FM	12 at 3 dB	XF – 107 A	820 II 25
FM	15 at 3 dB	XF – 107 B	910 II 25

Table 2

Table 3

Range	fr (MHz)	fo (MHz)	P	fφ (MHz)
B	1.7 – 4	10.7 – 13	4	2.675 – 3.250
C	4 – 12	13 – 21	4	3.250 – 5.250
D	12 – 20	21 – 29	8	2.625 – 3.625
E	20 – 30	29 – 39	8	3.625 – 4.875

The oscillator derived signal f_φ/P is now fed to the separate PLL unit which was extensively described in (2). This unit was designed around a frequency suitable for the delay line employed and therefore the oscillator signal has to be divided down accordingly. Friedrich Krug, DJ 3 RV, has described in (7) to (12) a high-performance 9 MHz IF amplifier which, when fitted with suitable 10.7 MHz filters, could be used with this front end. If the "large" PCB format is used (PCB DJ 3 RV 001 b), then the filter types given in **table 2** should be considered. Unfortunately, there is no monolytic CW crystal filter at 10.7 MHz (for DJ 3 RV 001 a) and the only usable type for SSB (XFM 107 S 60) has only 6 poles, a bandwidth of 2.7 kHz and does not fit exactly into the PCB holes.

If the long and medium wave range is despensed with, however, the front end can be designed for an IF of 9 MHz as shown in **table 3**.

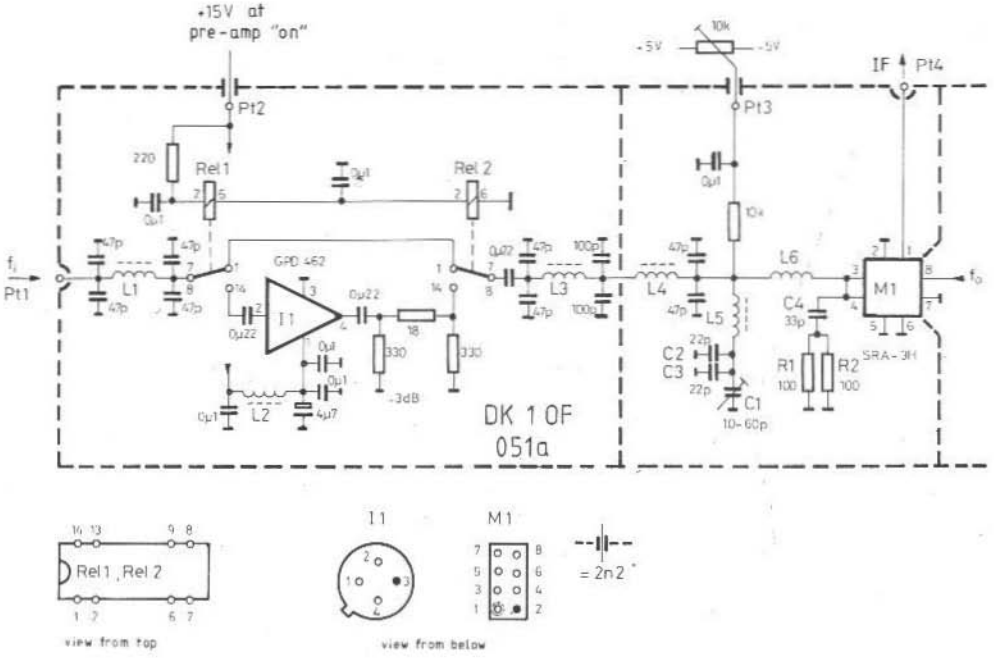

Fig. 2: RF pre-amplifier, IF trap and mixer

2. THE MIXER MODULE

2.1. Circuit Details

The first stage of the mixer module is shown in **fig. 2**. Immediately following the input at (Pt 1) is a π section low pass filter with L 1. The next stage is a GPD 462 (Avantek) integrated circuit broadband pre-amplifier whose data is shown in **table 4**. This amplifier, I 1, may be bypassed by means of the contacts of relays Rel 1 and Rel 2. With reference to the input, the intercept point IP is + 5 dBm and the gain is reduced to 10 dB by the 3 dB pad at I 1's output. The price of this hybrid amplifier is about DM 50.– and obtainable from Telemeter, Donauwoerth (Germany).

As the pre-amplifier is only employed with rod or indoor antennas, in the interest of an improved dynamic range, this pre-amplifier may be dispensed with altogether if operation on the main antenna only is contemplated. A more economical version of this IC amplifier is to be seen in **fig. 3**. This is the NE 5205 EC (Valvo/Signetics, ca. DM 10.–), the data is shown in **table 5**.

Table 4

Frequency range	f = 0 - 400 MHz
Power amplifier	G = 13 dB
Impedance	Z = 50 Ω
Noise figure	F = 6 dB
Output power	P = + 6 dBm (at 1 dB compresssion)
Intercept point	IP 3 = + 18 dBm (w.r.t. output)
Supply	Volts/Amps = + 15 V at 24 mA

Table 5

Frequency range	f = 0 - 450 MHz
Power amplifier	G = 19 dB
Impedance	Z = 50 Ω
Noise figure	F = 6 dB
Output power	P = + 4 dBm (at 1 dB compression)
Intercept point	IP 3 = + 17 dBm (w.r.t. output)
Supply	Volts/Amps = + 6 V at 24 mA

This IC has an IP value of – 2 dBm, again measured with reference to the input, the lower value due to the higher overall gain (19 dB instead

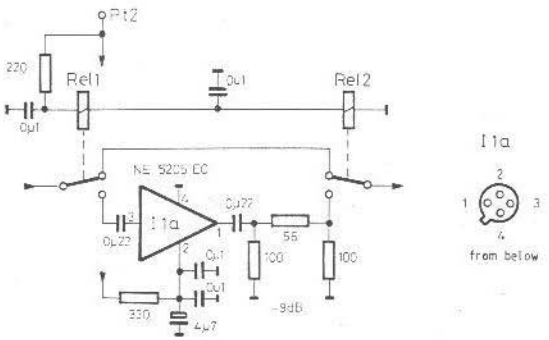

Fig. 3:
Low-cost version of RF pre-amplifier

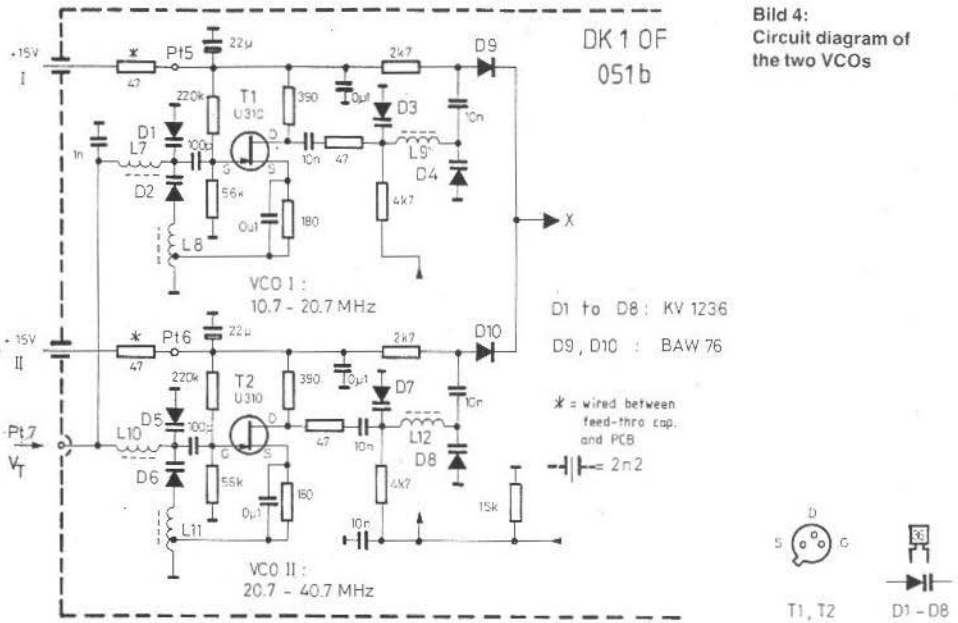

Bild 4:
Circuit diagram of the two VCOs

of 13 dB). The 9 dB attenuator pad can also be omitted but nevertheless the pre-amplifier still determines the total IP as the mixer alone has an IP of + 23 dBm. The signal path (**fig. 2**) is continued on to two further low-pass elements (L 3 and L 4) and the ring mixer, wideband matching network L 6, C 4, R 1, R 2. Such a network is also necessary to terminate the mixer's IF port. The

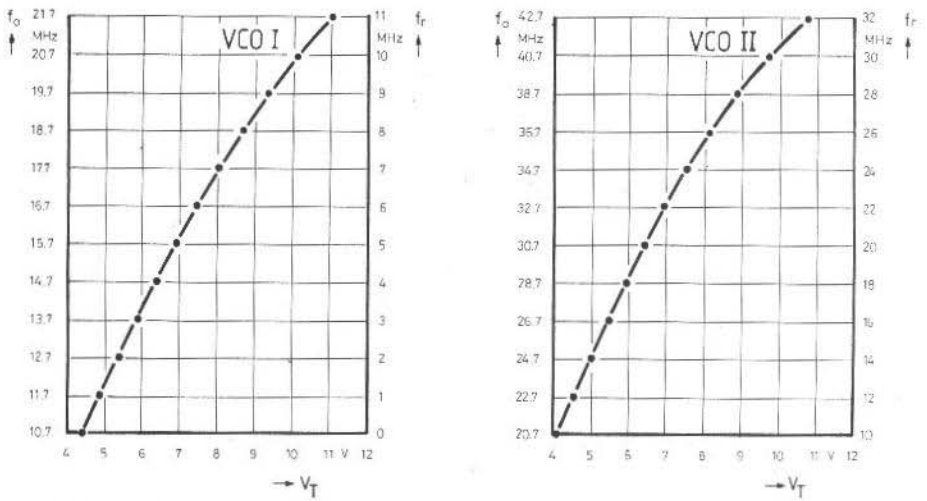

Fig. 5: VCO tuning curves

RF signal input is taken to pin 3, this being the only mixer input which is capable of being used down to very low frequencies. The other ports (oscillator input Pin 8 and IF output Pin 1) use internal transformers which limit the lower unusable frequency to 500 kHz. An external bias may be supplied to port 3 via Pt 3 which can be adjusted to improve the IF suppression of the mixer by some 6 dB to about 60 dB. If this is insufficient then the series circuit L 5, C 1, C 2, C 3 may be installed in order to bring another 30 dB of IF suppression to bear. This assumes a Q for the ring-cored L 5 of 250.

Fig. 4 shows the circuit diagram of the VCO. It may be seen that the necessary frequency range is covered by two oscillators, VCO 1 is supplied via Pt 5 when frequencies of between 10 kHz and 10 MHz are selected and VCO 2 receives a supply via Pt 6 when frequencies from 10 MHz to 30 MHz are received.

The common tuning voltage V_T is fed in via Pt 7. Each oscillator is fitted with an output low-pass filter (D 3, L 9, D 4 and D 7, L 12, D 8) which helps to improve the sinusoidal nature of the output signal. The limit frequency for these filters is influenced by the regulating voltage V_R (and with it the output voltage at X) thus allowing a degree of automatic level control. The tuning characteristics

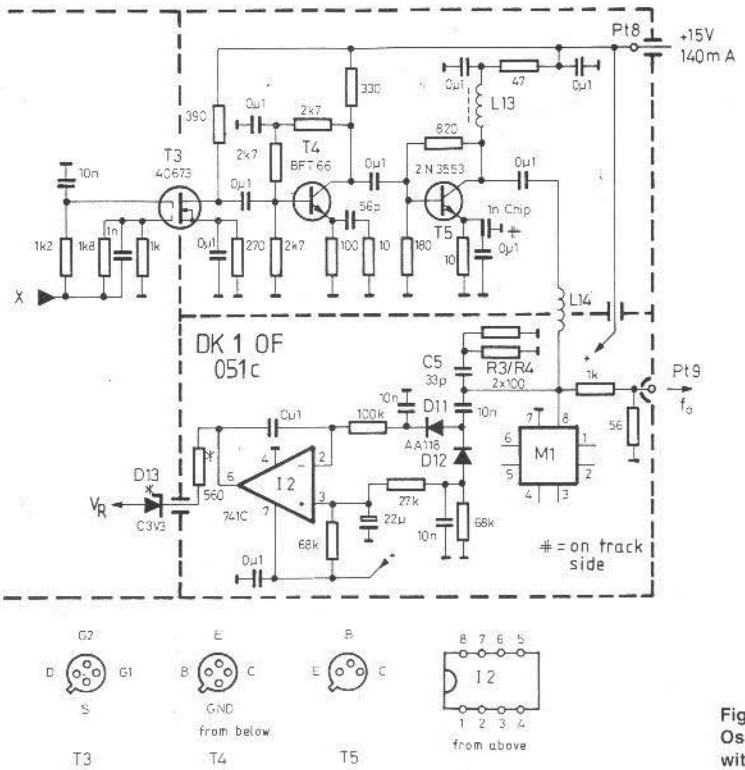

Fig. 6:
Oscillator-amplifier with level control

of both oscillators are depicted in **fig. 5**. Desite the almost full octave covered by the oscillator, the phase noise characteristics, on account of the high-tuned circuit Q, are satisfactory (tuned circuit use ring inductors for L 8 and L 11). The test data will be published at the end of the article.

The other stages of the mixer module are shown in **fig. 6**. The DG-MOSFET T 3 functions as a buffer in order to isolate the VCO. A two stage power amplifier follows, using bipolar transistors T 4 and T 5, which delivers a power of + 17 dBm (50 mW) to the mixer oscillator port. The mixer oscillator port is connected to a matching network L 14, C 5, R 3, R 4 which ensures a wideband 50 Ω termination impedance.

A portion of the local oscillator power is fed out via Pt 9 at a power of − 19 dBm (20 mV/50 Ω) and taken to the PLL portion. Diodes D 11 and D 12 produce a DC level which is proportional to the oscillator amplitude. This DC feeds I 2, the output of which is taken via D 13 to the VCO varicap low-pass filter. The voltage divider resistors on pin 3 of the operational amplifier are dimensioned to allow a power of + 17 dBm to be fed to the mixer. An adjustment for this has been deliberately omitted, as an exact measurement using amateur means is often a perplexing problem. These stages are all fed via Pt 8 with + 15 V at 140 mA.

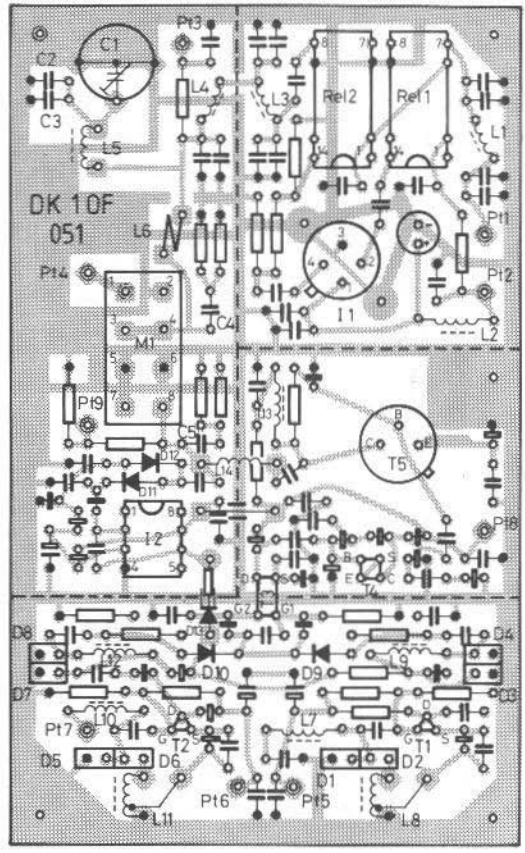

Fig. 7: Mixer card component layout

2.2. Construction

The circuit has been realised on a double-sided, through-contacted printed circuit board. This is 110 mm x 67.5 mm and is designated DK 1 OF 051. A 30 mm high tin-plate (or PCB) wall contains the board. The board is soldered into the container to allow a clearance of about 8 mm from the track side to the bottom of the walls. The HF connections (Pt 1, 4, 7, 9) are made via coaxial sockets or teflon feed-through terminals. the supply lines (Pt 2, 3, 5, 6, 8) are led in via feed-through capacitors. The two integrated circuit types given for I 1 have the same pin-out but the position of the pin locator markers are different. The Avantek type is installed in the component layout plan of **fig. 7**. The dotted lines denote screening walls which divide the board up into several compartments. They are also continued through on the underside of the board. This is shown in the photograph of **fig. 8**.

2.3. Special Components

I 1:	Integrated broadband amplifier, GPD 462 (Avantek) or NE 5205 EC (Valvo, Signetics)
I 2:	Operational amplifier 741 C DIP-8 (various manufactures)
M 1:	Schottky diode ring mixer (LO = 17 dBm) Type SRA-3H, SRA-1 H or TAK-3H (Mini Circuits)

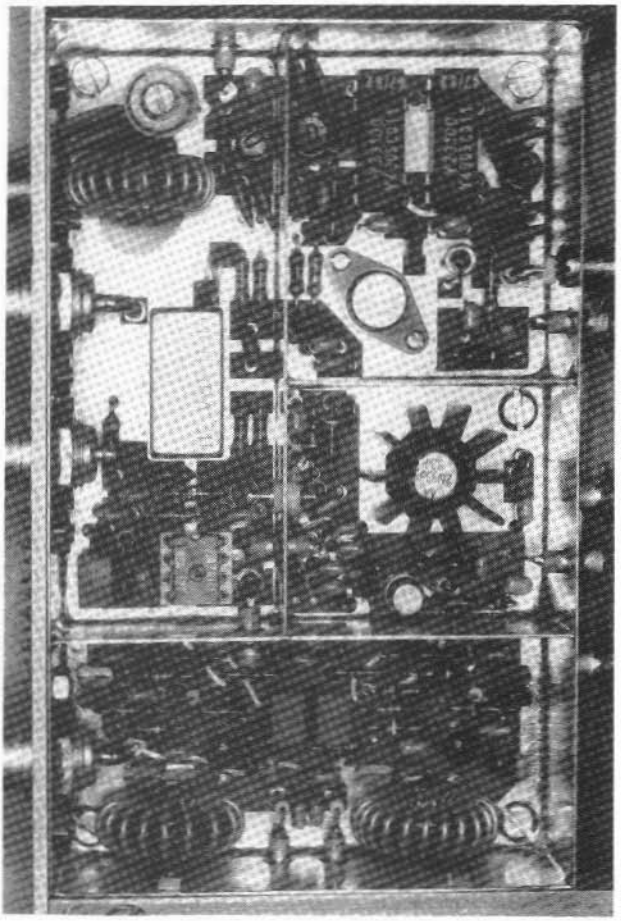

Fig. 8:
Mixer module prototype

Rel 1, 2:	Reed change-over in DIP housing, 5 V/200 Ω (e.g. Siemens V 23100 – V 4305 – C 011)
T 1, T 2:	U 310, E 300 or equiv. junction FET
T 3:	40673, 40841 or equiv. DG-MOSFET
T 4:	BFT 66
T 5:	2 N 3553, 2 N 3866 or equiv., with heatsink
D 1 - D 8:	Varicap diode KV 1236 (Componex, Duesseldorf)
D 9, D 10:	BAW 76, 1 N 4151 or equiv. Si-diode
D 11, D 12:	AA 118 or equiv. Ge diode
D 13:	Z diode 3.3 V
C 1:	Ceramic or foil trimmer ca. 60 pF, 10 mm dia

Note: All capacitors below 1 μF are ceramic, disc or plate NB. If the NE 5205 is used for I 1, choke L 2 (fig. 2) must be exchanged for a 330 Ω resistor (fig. 3)!

2.4. Inductor Data

L 1, L 3, L 4:	Ferrite choke 0.33 µH (e.g. Siemens B 78108-T 3331-M)
L 2, L 9, L 10:	Ferrite choke 10 µH (e.g. Siemens B 78108-T 1103-K)
L 5:	23 turns silvered wire 0.5 mm insul. on Amidon T 68-2 core
L 6:	2 turns silvered wire 0.5 mm, 5 mm dia
L 7, L 13:	Ferrite choke 33 µH (e.g. Siemens B 78108-T 1333-K)
L 8:	23 turns silvered wire 0.5 mm insul. on Amidon T 68-2 rincore. Tapped 2 turns from ground end
L 11:	15 turns silvered wire 0.5 mm insul. on Amidon T 68-10 ringcore. Tapped 3 turns from ground end
L 12:	Ferrite choke 1 µH (e.g. Siemens B 78108-T 1102-K).
L 14:	1 turn silvered wire 0.5 mm, 10 mm dia

Amidon cores: Firm Giessler & Danne, Muenster, Germany. Wire-wrap wire is suitable as it is silvered, highly insulated and obtainable in diameters 0.25 - 0.5 - 0.8 mm.

2.5. Commissioning

The oscillator amplifier is checked first by measuring the currents flowing through T 3, T 4 and T 5 after Pt 8 has been connected to + 15 V (the VCOs remaining unsupplied). This is done by measuring the potential difference across the emitter/source resistor and thereby deriving the current. The following currents should be obtained: –

T 3:	10 mA (6 - 15 mA)
T 4:	20 mA ± 10 %
T 5:	100 mA ± 10 %

Large departures from these values must be investigated and cleared before proceeding further. Note: Before power is applied to Pt 8 for the tests detailed above, a 2.7 kΩ resistor should be temporarily connected from it to the point marked X (fig. 6) in order to provide T 3 with gate bias.

The 15 V supply is now connected to pt 5 and Pt 7 to an adjustable 0 to + 15 V (e.g. from a potentiometer) and a frequency counter is connected to Pt 9. The frequency versus tuning voltage VCO 1 characteristics can now be taken and compared with those of fig. 5. Inductor L 8 may have an adjustment to the number of turns if this is proved to be required. The tuning voltage at Pt 7 is as follows:

at fo = 10.7 MHz not smaller than 3.5 V
at fo = 20.7 MHz not greater than 12 V

VCO 2 is now tested in a similar manner. The frequencies for the given tuning potentials for this voltage range are 20.7 MHz to 40.7 MHz.

The voltage control is now tested by measuring the DC voltage on I 2 pin 6. This must vary between + 3 V and + 12 V when the VCOs are tuned completely through their ranges. The voltage amplitude may be influenced by the inductance of choke L 9/L 12.

If an IF stage is already available, one from a VHF receiver may be employed, it should be connected to Pt 4 and an antenna to Pt 1. Upon tuning the VCO, stations should be heard, although the stability, especially for SSB/CW, will not be very satisfactory to say the least. Nevertheless, tuning-in an AM station should be sufficient to verify that the pre-amp I 1 is functioning correctly.

The IF rejector circuit (L 5) is adjusted to achieve the maximum IF suppression with C 1 and then by adjusting the potential applied to Pt 3 via the preset. This preset is later replaced by a 10-turn version when the whole equipment is completed. When the action of this voltage has been verified, the temporary preset may be removed and Pt 3 connected directly to earth.

3. THE RF INPUT FILTER UNIT

3.1. Circuit Details

The complete circuit diagram of the RF input filter unit is shown in **fig. 9**. Each of the five range

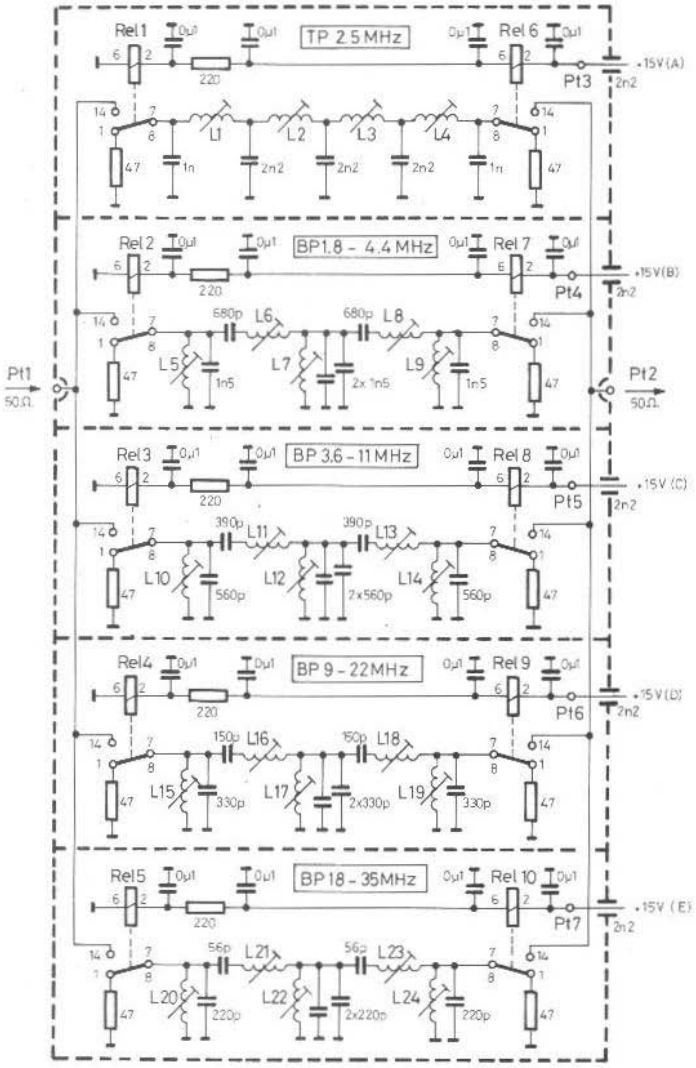

Fig. 9:
RF input filter unit circuit diagram

filters are switched in circuit by means of relays, the unused filters being terminated at both terminals with 47 Ω resistors to ground. The lowest receiver range (0 - 2 MHz) has a four-stage, low-pass filter and the other four have π network band-pass filters. The calculated limit frequencies are also given in fig. 9. The circuit is passive and as the input and output impedances are both normally 50 Ω, Pt 1 can be interchanged with Pt 2.

The photograph of **fig. 10** shows clearly the shape of all filters by means of a multiple expo-

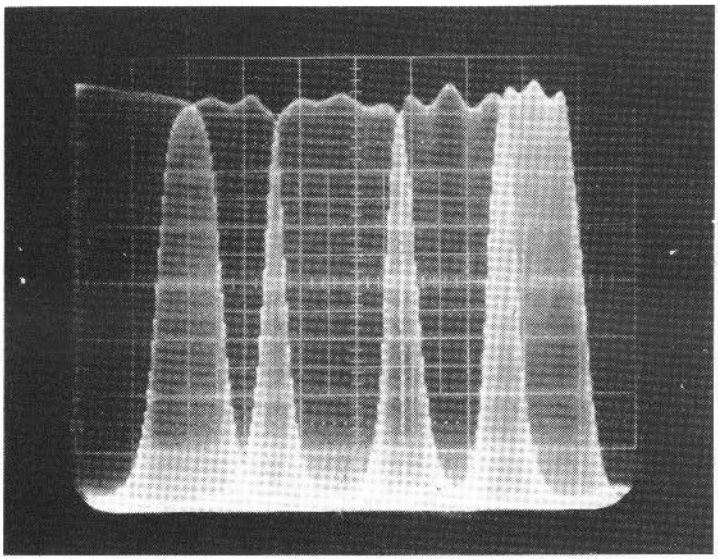

Fig. 10:
Band-pass characteristics of the five input filters

sure film during a swept frequency input. The horizontal X axis (frequency) starts at 1 MHz, finishes at 50 MHz and is logarithmic. The vertical Y axis (amplitude) is linear.

3.2. Construction

A printed circuit board has been prepared for the RF input filter unit which is 110 mm x 102.5 mm large, is double-sided and through-contacted. Its designation is DK 1 OF 052. A similar screening wall, to that of the mixer unit, surrounds the board completely and screening walls are placed between each filter channel. The component layout is shown in **fig. 11** and **fig. 12** shows a plan view of a completed specimen.

3.3. Special Components and Coil Data

Rel 1...Rel 10:	Reed c/o in DIP housing; 5 V, 200 Ω (e.g. Siemens V 23100 - V 4305 - C 011)
All capacitors:	Ceramic disc or layer types, lead spacing 5 mm
All coils:	wound on Vogt coilkit Type 514 - 05
L 1, L 2, L 3, L 4:	22 turns, 0.15 mm CuL S *) L = 5.1 μH, Q = 77 at 1.7 MHz
L 5, L 9:	14 turns, 0.15 mm CuL S, L = 2.1 μH, Q = 72 at 3 MHz
L 6, L 8:	21 turns, 0.15 mm CuL S, L = 4.7 μH, Q = 96 at 3 MHz
L 7:	10 turns, 0.25 mm Cu Ag insul., L = 1.1 μH, Q = 47 at 3 MHz
L 10, L 14:	10 turns, 0.25 mm Cu Ag insul., L = 1.1 μH, Q = 73 at 7 MHz
L 11, L 13:	12 turns, 0.25 mm Cu Ag insul., L = 1.6 μH, Q = 76 at 7 MHz
L 12:	7 turns, 0.25 mm Cu Ag insul., L = 0.57 μH, Q = 74 at 7 MHz
L 15, L 19:	6 turns, 0.25 mm Cu Ag insul., L = 0.39 μH, Q = 95 at 15 MHz
L 16, L 18:	9 turns, 0.25 mm Cu Ag insul., L = 0.86 μH, Q = 100 at 15 MHz
L 17:	4 turns, 0.25 mm Cu Ag insul., L = 0.19 μH, Q = 91 at 15 MHz
L 20, L 24:	4 turns, 0.25 mm Cu Ag insul., L = 0.18 μH, Q = 115 at 25 MHz

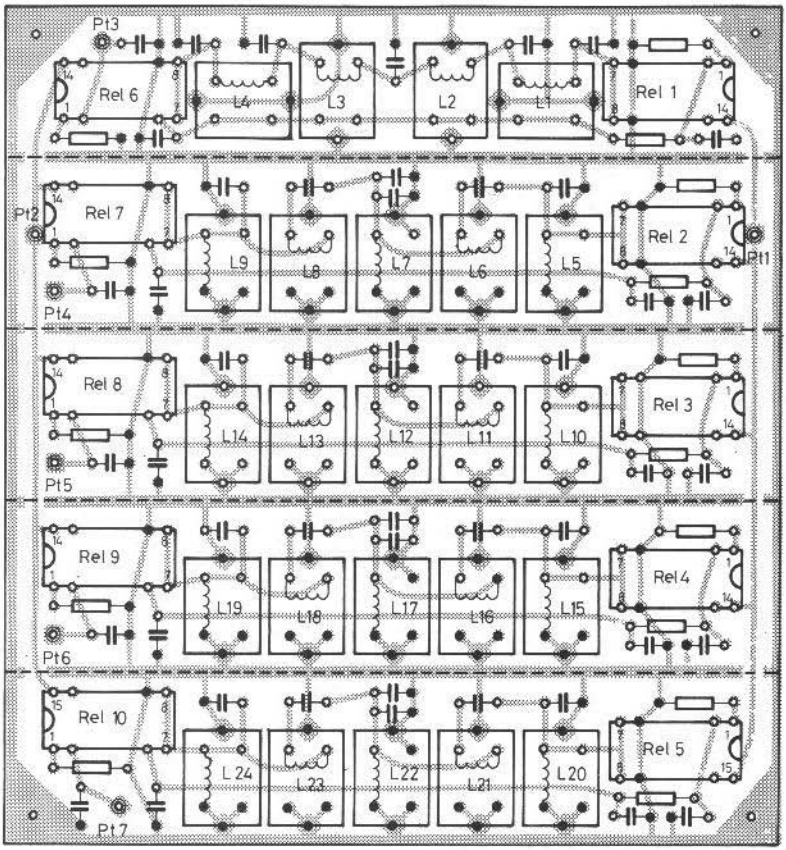

Fig. 11: Filter card component layout

L 21, L 23: 8 turns, 0.25 mm Cu Ag insul., L = 0.70 μH, Q = 140 at 25 MHz

L 22: 3 turns, 0.25 mm Cu Ag insul., L = 0.086 μH, Q = 105 at 25 MHz

*) CuL S = Copper enamelled, silk covered wire

3.4. Alignment

The availability of a sweep generator and oscilloscope would enable the alignment to proceed quickly without any problems. After supplying Pt 3 with + 15 V the range A low-pass can be adjusted so that the − 6 dB point (half voltage) occurs at

Range	+ 15 V to Pt	Middle Frequency (MHz)
B	4	2.8
C	5	6.5
D	6	14.1
E	7	25.1

Table 6

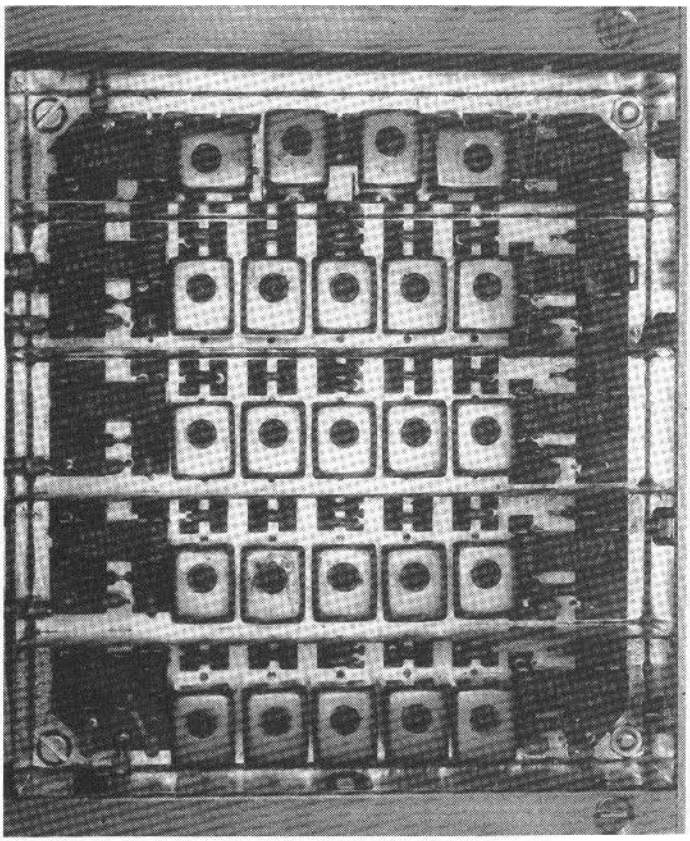

Fig. 12:
RF filter module prototype

2.5 MHz. The level reference being that at a frequency of 1 MHz. It should be noted that the cores of L 1 to L 4 should occupy the same position in the coil form.

Now align the band-pass ranges B to E by aligning them all, each with 5 coils, to the middle of their respective ranges in accordance with **table 6**. If the pass-bands display humps of various amplitudes they can be ironed out with very small tuning adjustments to the cores. The pass-band limit frequencies given in fig. 9 are referenced to – 3 dB rel. centre freq. (i.e. 70 % of midband voltage).

A correctly aligned filter, terminated with a real impedance of 50 Ω (input and output), should exhibit an insertion loss of less than 1.2 dB and pass-band humps of less than 0.5 dB.

The procedure outlined above is also valid for the point-by-point method of alignment using a signal generator and an RF voltmeter but, of course, the whole procedure is much more time consuming and tedious. Should absolutely no test equipment be available, then all cores should be screwed in until they just engage the top of the windings. Results of some kind will be available using this tactic but the pass-bands are liable to 6 to 10 dB variations. However, it is better than nothing!

3.5. Literature

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Wolfgang Borschel, DK 2 DO

Dimensioning Stacked Yagi Antennas using the Superposition Technique

This article describes a technique for the dimensioning of high-gain, stacked Yagi arrays. It employs charts which have a universal application. The article describes further considerations from the work of G. Hoch, DL 6 WU (1) leading to the application of the superposition technique. It gives, in a simple form, the optimum spacing for combined antennas and the gain which can be expected from such a combination.

1. THE SUPERPOSITION PRINCIPLE

Superposition means super (im)position. The superposition principle says, that incompressible potential currents arising from superposition will continue to obtain incompressible potential currents. The superposition occurs arithmetically in general through the addition of the real or complex potentials.

In our case, every individual antenna delivers a received potential. Through the superposition process, two such individual antennas deliver a new received potential and with it, also, a new current. This new potential causes an alteration to the specified size of the beam width and thereby to the gain of the composite antenna. The influencing factors of this new antenna are the stacking distance and the beam width of the individual antennas.

2. GAIN OF A DIRECTIVE ANTENNA

When Yagi antennas are grouped into an array, the beam widths of the individual antennas are decisive factors for their arrangement in the array. This statement invokes the much quoted Kraus formula for the gain of an antenna:

$$G = \frac{4\pi}{\Theta_E \Theta_H}$$

where Θ_E is the beam width in the electric plane and Θ_H is the beam width in the magnetic plane. As it emerges from the formula, the gain and beam width of an antenna have a rigidly fixed relationship with each other.

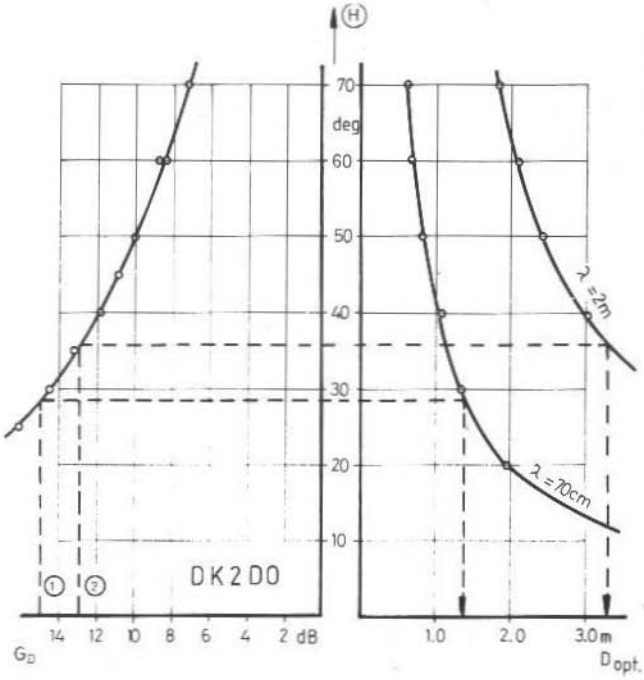

Fig. 1:
Use this diagram for the initial combination of element antennas having an individual gain of 7 – 14 dB_D.

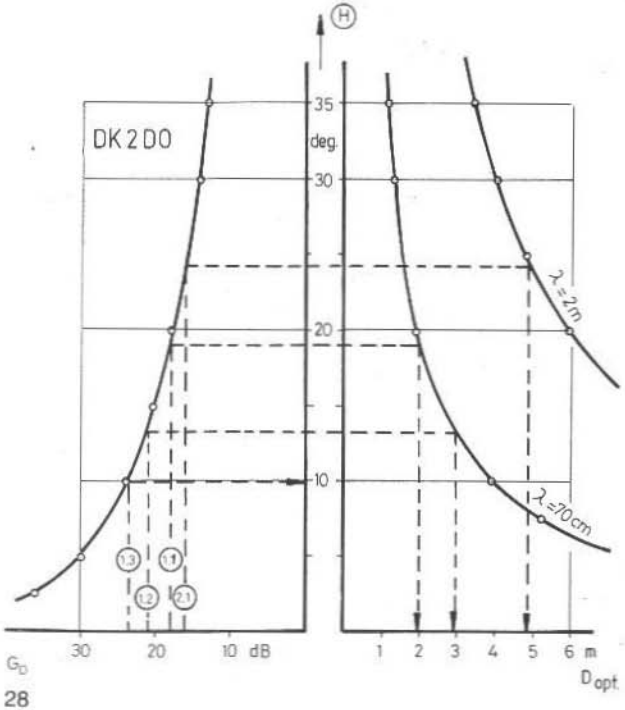

Fig. 2:
Use this diagram for subsequent stacking of combined antennas to form composite arrays having gains of 13 – 35 dB_D.

3. USE OF THE SUPERPOSITION PRINCIPLE IN DIAGRAMATIC FORM

The choice of stacked antennas may well lie in the commercial field but they can come from the ranks of the do-it-yourself brigade. The important thing is, that the characteristics of the individual-element antennas, comprising the stack, are known exactly. The element-antenna's gain is the most important criterion, but often, the manufacturer also specifies the beam width as well. Also, a knowledge of the beam width can be used to obtain a good estimate of the antenna gain.

On account of the form of construction of Yagi antennas, the horizontal and vertical beam widths can never be exactly equal. A departure of a few degrees from parity will always be the case. Using the diagrams of **fig. 1** and **fig. 2** both beam width angles are taken as a geometrical mean, $\Theta = \sqrt{\Theta_E \cdot \Theta_H}$ for the sake of simplicity. The resulting error has been shown, by experiments at UHF, to be negligibly small. In order to ensure this, the first stack is made vertical, the second horizontal, the third vertical, and so on.

In the characteristic of fig.1 and fig. 2, the Kraus formula for the calculated dipole gain is apparent. The right-hand curves of the drawings show the characteristics of the optimal stacking spacing as a function of the beam width. By projecting the "antenna gain" via intersection to the left-hand curve over to the appropriate right-hand curve and down to the optimal spacing (D_{opt}) axis, both the element antenna beam width (before stacking) and optimal spacing may be obtained. It should be noted that the antenna gain G_D of the X-axis is initially taken as being the gain of one of the (identical) element antennas forming the first pair combination of the array. A subsequent pairing of such combinations, to form an array of four elements, will use the "new gain" arising from the element pair. The gain of the element quad is then used for a further combination to form an eight-antenna array, and so on.

It may be seen from **fig. 3** that the optimum spacing yields an increase in gain of 2.8 dB_D over

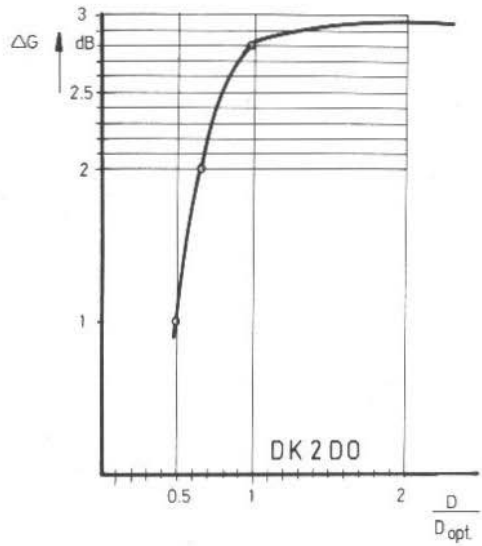

Fig. 3: Stacking gain departures from the gain at the optimum distance. Use this curve to arrive at the shortfall in gain when the optimum spacings cannot be achieved in practice.

one-element antenna (or stack). The following examples will make the procedure clear.

3.1. Example 1

A 70 cm antenna having a gain of 15 dB_D is combined with similar antennas to form an array of eight antennas.

1. What is the total gain to be expected from the stack?
2. What are the required combining and stacking spacings?

Locating the given gain of 15 dB_D on the gain axis (LH) of fig. 1 and projecting the X co-ordinate over to the 70 cm optimum spacing curve (RH), a spacing of 1.40 m is obtained and a beam width of approx. 27°. The two vertically stacked Yagis now have a total gain of 17.8 dB_D (15 dB_D + 2.8 dB_D) at a new beam width of only 19°.

Taking this result over to fig. 2 and following an identical procedure to that given above, two of these combinations stacked in the horizontal

plane must have an optimum spacing of 2 m (follow co-ordinates (1.1)) and a gain of 20.6 dB_D (17.8 dB_D + 2.8 dB_D).

The third combination consisting of two groups of four, this time stacked 3 m vertically apart, have a stacking gain of 23.4 dB_D (20.6 dB_D + 2.8 dB_D). (Follow lines (1.2)). Finally the beam width of the total 8-element array is from the LH gain/beam width curve following lines (1.3) to arrive at a beam width of 10°.

3.2. Example 2

A Yagi for the two-metre band has a gain of 13 dB_D and is to be used in a four-element array.

1. What is the array gain?
2. What are the element-antenna spacings?

Following lines (2) in fig. 1 and using the 2 m curve of the RH graph, a vertical spacing of 3.3 m is arrived at from an element-antenna gain of 13 dB_D in the LH graph. The gain is 15.8 dB_D (13 dB_D + 2.8 dB_D). Tranfering this result over to fig. 2 LH curve and following co-ordinates 2, 1, a horizontal stacking distance of 4.90 m is obtained. The total array gain is then 15.8 dB_D + 2.8 dB_D = 18.6 dB_D. If this distance cannot be achieved in practice, use fig. 3 to determine the gain shortfall to be expected.

3.3. Conclusion

Following the procedure described above, the author has constructed an eight-element array which has been used in numerous EME contacts. It was interesting to use it to determine the total receive installation noise figure as described by the author in (2).

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TV Satellite Receive System Part 2: Indoor Unit

Whilst part 1 of this series (VHF COMMUNICATIONS 4/1986) described the low-noise 11 GHz down-converter, mounted on the antenna and forming the so-called external unit, the present article concentrates upon the indoor equipment located with the television receiver.

This consists of a tunable first IF receiver covering 0.85 to 1.6 GHz and containing a special FM demodulator – which also drives an AM demodulator – a demodulator for speech signals and a power supply for the external unit. This two-part article is thereby concluded.

6. INTRODUCTION OF PART 2

Television signals are usually retransmitted by satellites using the 4 GHz, 11 or 12 GHz frequency bands. Since conventional transmission lines, like coaxial cables, have very high losses at microwave frequencies, the first down-converter should be located rather close to the antenna – usually it is installed directly behind the feed of a parabolic dish antenna.

Although the resulting intermediate frequency may fall at least partially in the frequency range covered by an ordinary TV set, the down-converted satellite signal can not be accepted by an ordinary terrestrial television receiver due to the large differences in the signal format. Terrestrial television broadcasting in the VHF and UHF bands uses amplitude modulation for the video signal and an additional frequency modulated carrier for the corresponding sound information. On the other hand, satellite television transmissions use wideband frequency modulation for the video signal. The corresponding sound can be transmitted in many different ways: usually a frequency modulated subcarrier (between 5 and 8 MHz) is added to the baseband video signal just in front of the main wideband FM modulator, although other systems are being used too, such as a digitally modulated subcarrier or a digital sound-in-sync or as a separate carrier transmitted through a separate satellite transponder.

A separate IF amplifier and FM demodulator is therefore required for satellite TV transmissions. Since most existing TV sets accept only VHF or UHF modulated signals, an AM modulator should be connected to the output of the FM demodulator. A suitable circuit, to demodulate the sound information, should also be included since the sound subcarrier frequency usually differs from the standard 5.5 MHz. All the above circuits are installed together with a power supply for the outdoor microwave front-end in a suitable case and are usually signified as the "indoor unit". Since the outdoor microwave down-converter is usually fixed-tuned (block down-converter), the indoor unit should be tunable across the intermediate

frequency band supplied by the outdoor equipment. Therefore the indoor unit usually includes a second, tunable down-converter to a second, fixed-tuned IF chain.

The first IF band generally ranges from about 900 MHz to 1700 MHz (+/−100 MHz). This frequency choice is simply imposed by the available cables and semiconductors and the need to avoid interference from powerful terrestrial UHF broadcast stations. Note that the instantaneous first IF bandwidth may be as wide as 800 MHz, depending on the actual satellite band being received. The second IF is fixed-tuned and its bandwidth should correspond to the modulation bandwidth of the received signal, which ranges from 25 to 36 MHz. Several second IF values are actually being used – older equipment uses 70 or 134 MHz (center frequencies), while recent IF chains use 400, 480 or 612 MHz due to the ease of filtering out the second conversion image frequency. The indoor unit, described in this article, uses a second IF of 200 MHz, which was chosen as a compromise between the availability of suitable components and circuit complexity. The first IF band ranges from 850 to 1600 MHz with a considerable overlap at both band edges to match the low-noise 11 GHz down-converter, described in (1), and is also compatible with commercially available block down-converters.

7. THRESHOLD EXTENSION DEMODULATORS

Actual satellites can only carry weak transmitters that are up to 40,000 km away from the receiving earth stations. Frequency modulation is being used for the transmission of television signals over satellite transponders since it offers the best performance for a given satellite transmitter output power in comparison with other modulation types. First, the satellite transmitter can operate close to saturation with a high efficiency, second, in the demodulation process, the signal-to-noise ratio can be increased considerably by a fixed amount known as the "FM advantage". Considering the deviation and the pre-emphasis of satellite TV transmissions, the FM advantage amounts up to 30 dB. Of course, this improvement in the signal-to-noise ratio can only be obtained if the signal-to-noise ratio at the input of the FM demodulator is above a certain value, known as the threshold of an FM demodulator. For a conventional FM demodulator including an efficient limiter and a discriminator, the threshold occurs around 10 to 12 dB signal-to-noise ratio at the input. Above threshold, such a demodulator provides a virtually noise-free picture, while below threshold, the output is not usable.

At the output of any FM demodulator, the noise appears in two different forms: as a 'fine-grain' noise and as a 'rough' noise. The 'fine-grain' noise is almost independent on the demodulator threshold. Well above the demodulator threshold, it is the only form of noise present. On a TV picture, this kind of noise causes the familiar 'snow' effect, although much less disturbing than in the case of a conventional AM transmission. Decreasing the signal-to-noise ratio at the input of the FM demodulator, the 'rough' noise starts appearing as random spikes in the signal. The amplitude of these spikes is comparable to the full signal deviation while their duration is determined by the de-emphasis network. Decreasing further the input signal-to-noise ratio, the frequency of these spikes rapidly increases corrupting the useful signal. In the case of television signals, the 'rough' noise appears as random, short black and white lines on the picture, popularly called 'sparklies'.

Since the available RF signal-to-noise ratio is limited by the satellite's Tx power and antenna, receiving antenna size and receiver noise figure, improving the demodulator performance by decreasing its threshold is worth-while the effort. Such improved demodulators are usually called threshold extension demodulators. The operation of any threshold extension demodulator is based on the fact that the instantaneous spectrum width of a frequency modulated signal is usually smaller than the whole available bandwidth. This is especially true when the spectrum of the modulating signal only contains significant, very low fre-

quency components. A tracking filter can be built so that the noise bandwidth is reduced in front of the demodulator increasing the effective signal-to-noise ratio at the input of the demodulator above its threshold. Threshold extension demodulators allow the reception of very weak signals even when the carrier-to-noise ratio is below 0 dB.

Unfortunately, threshold extension demodulators also have a major disadvantage: the tracking filter has difficulties in following fast and wide deviations. Noise induced sparklies will therefore appear at well-defined places in the picture, usually after sharp black/white or white/black transitions. This unwanted side-effect is actually proportional to the amount of threshold extension.

Threshold extension demodulators can be built as either phase-locked-loops or varicap-tuned tracking filter/discriminator combinations. PLL demodulators are widely used, since they are easy to build and align, and the threshold is easily adjustable. On the other hand, the tracking filter/discriminator demodulators provide a slightly better performance but they are more complex and unstable although single-chip demodulators, according to this principle, will probably make them more popular (Plessey SL 1453). In any case, a threshold extension demodulator requires a linear, non limiting IF chain with an accurate AGC and a careful design and construction of the demodulator itself, otherwise the results may be even worse than without threshold extension.

8. BLOCK DIAGRAM OF THE INDOOR UNIT

The block diagram of the TV satellite receive system's indoor unit is shown in **fig. 13** and includes the following modules: a second tunable down-converter, an AGC attenuator, a second IF amplifier and AGC detector, a phase-locked-loop demodulator, an AM video modulator, a sound demodulator and a regulated DC voltage converter. The indoor unit shown in **fig. 13** accepts the broadband IF output of the outdoor antenna-mounted 11 GHz down-converter and supplies the latter with + 12 VDC through the same coaxial cable. After processing the signal, the circuit provides three separate outputs: a baseband video output to feed a TV-monitor, a modulated VHF band 1 signal to feed a conventional TV receiver without a baseband video input and an audio output to drive a loudspeaker. The indoor unit shown does not include de-scramblers to decode scrambled TV transmissions and the sound demodulator is only suitable for conventional frequency-modulated audio subcarriers. If required, these circuits can be added later, but most satellite TV signals over Europe have a clear (unscrambled) video and one or more FM audio subcarriers.

The receiver requires a single supply voltage of + 12 VDC (negative ground) and can be battery-supplied. Of course, it is possible to add a mains transformer, rectifier and a suitable voltage regulator (7812) for mains operation. The regulated DC voltage converter generates from the available + 12 VDC, a stabilized voltage of about + 25 VDC supplying two front panel controls: the channel frequency tuning potentiometer and the audio subcarrier frequency potentiometer, both feeding the corresponding varicap diodes. All the other circuits require only + 12 VDC supply voltage.

The receiver selectivity is given by the tuned circuits in the second tunable down-converter and second IF amplfier. Since the only source of interference is thermal noise, the requirements are not very high. In fact, the PLL threshold extension demodulator itself determines the bandwidth of the receiver. On the other hand, a PLL threshold extension demodulator requires a very stable input signal level since the demodulator transfer function, and in particular its bandwidth, is directly proportional to the input signal level. The signal level can be adjusted by the corresponding potentiometer 'AGC level'. When adjusting the antenna and/or the receiver, it may be useful to switch off the AGC function. In this case the 'AGC level' potentiometer acts as a manual gain control. An automatic frequency control circuit is not included since the stability of both down-converters is sufficient. In any case, the

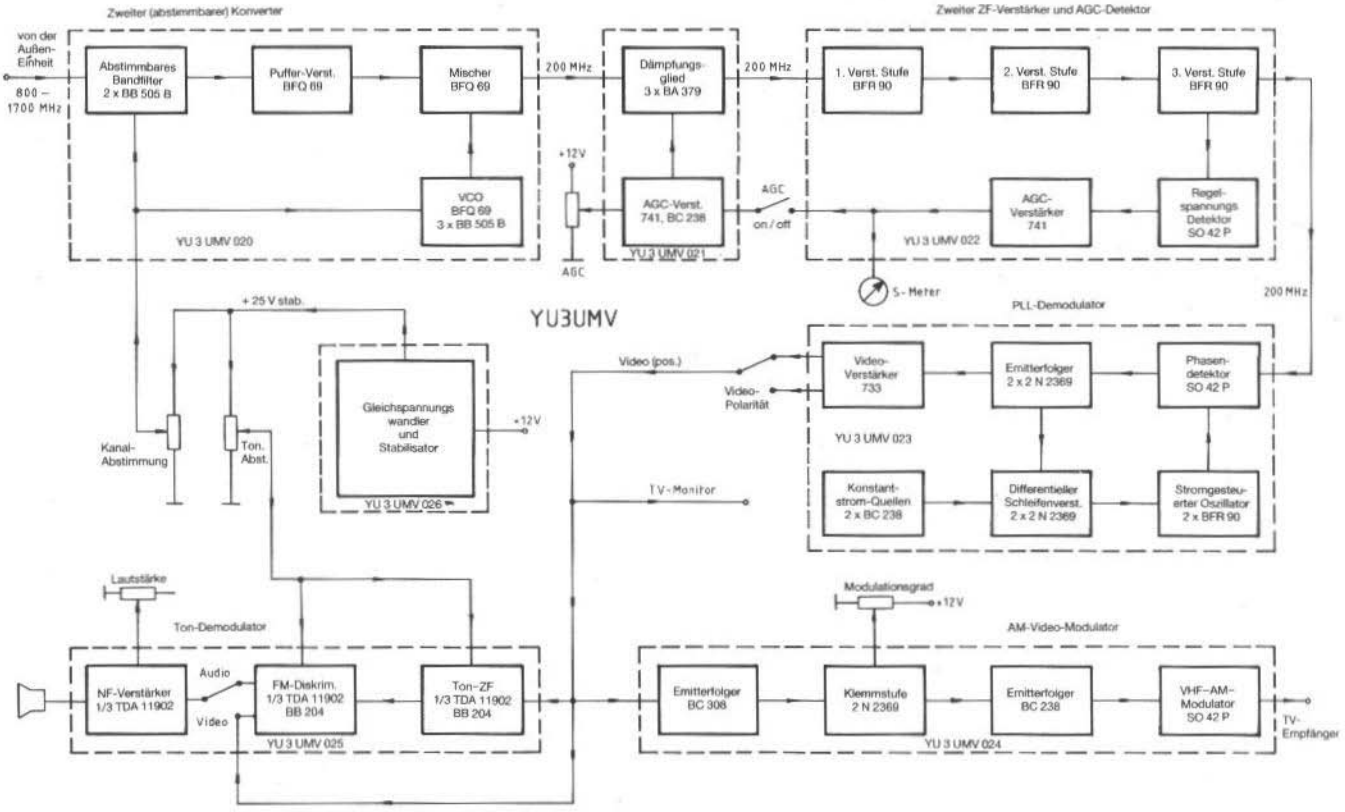

Fig. 13: Blockdiagram of the sat-TV receiver indoor unit

modulating video signal contains a considerable DC component and a conventional average value AFC circuit would detune the receiver with very bright or very dark pictures. A keyed AFC should be required that, as a reference uses the sync level or the re-trace black level.

All satellite TV transmissions include a spectrum dispersion waveform. This is necessary to avoid the concentration of all the transmitter power into a few narrow spectrum lines, especially when transmitting stationary pictures like test patterns, and limit the interference to terrestrial services operating in the same frequency bands. The spectrum dispersion waveform is usually a triangular wave of half the field frequency, the edges of the triangular wave being synchronized with the vertical retrace period to reduce the interference to the TV picture. Such a spectrum dispersion waveform can easily be removed from the video signal by a simple video clamping circuit. This circuit is usually already present in good-quality TV monitors. However, a video clamping stage is required in front of the VHF AM modulator.

Since satellite signals have different deviations and pre-emphasis, the video signal level should be adjusted in front of the modulator. The differences between different pre-emphasis are small and a simple integrator, included in the PLL demodulator module, gives good results for all the available satellite TV signals.

The sound demodulator is very similar to those being used in conventional TV sets, except that all the circuits are tunable using varicap diodes to match the actual audio subcarrier frequency. The input of the audio amplifier can also be switched directly to the output of the PLL demodulator to listen to the video signal. This is very useful when searching for a satellite by adjusting the antenna direction and receiver frequency. The well-known field frequency hum can be heard at signal-to-noise ratios as low as – 20 dB, much before anything can be seen on the TV screen.

8.1. Second Tunable Down-Converter

The second tunable down-converter (**see fig. 14**) includes a two-stage tunable band-pass filter with varicap diodes for image rejection, a buffer RF amplifier stage to overcome the losses in the filter and to provide the mixer with a stable output impedance, a broadband voltage-controlled oscillator (VCO) and a common-base bipolar transistor mixer stage.

Although the block diagram is not much different from a standard UHF TV tuner, the actual design and practical construction is much more demanding, since components with comparable electrical performances are not readily available for higher frequencies. For example, the Q-factor of a readily available UHF varicap diode is only between 10 and 20 at 1.5 GHz depending on the bias voltage. Broadband tunable high-Q filters can obviously not be built with such diodes. Almost all suitable diodes, such as BB 221 or BB 505, have a minimum capacity of about 2 pF. The inductivity required to resonate such a diode in the 1 to 2 GHz range is very small and a printed circuit board made of conventional 1.6 mm thick glass-fiber epoxy can not be used. The performance of the diode is further limited by the diode package parasitic inductivity. Practical experiments have shown that glass-packaged diodes (Do 35), such as BB 221 or BB 505, have a lower parasitic inductivity than earlier plastic-packaged types such as the BB 105.

The input band-pass filter consists of two resonant circuits made of the two BB 505 B varicap diodes and inductors L 3 and L 5 (short air dielectric microstrips). The coupling between the two resonant circuits and to the rest of the circuit is inductive (L 2, L 4 and L 6) since it offers a more constant filter performance across a wide frequency band than capacitive coupling and is easy to implement in practice too. L 1 is not a part of the filter, it is just a $\lambda / 4$ choke to feed the + 12 V supply voltage to the outdoor unit through the coaxial cable. The insertion loss of the filter is about 4 dB per resonant circuit so that the amplifier stage with T 1 (BFQ 69) is just sufficient to recover the overall filter insertion loss. The most important function of T 1 is, however, to provide the mixer and the VCO with a stable output impedance to prevent frequency jumps and other instabilities of the VCO.

The VCO operates 200 MHz above the input frequency for two reasons: first, the required relative

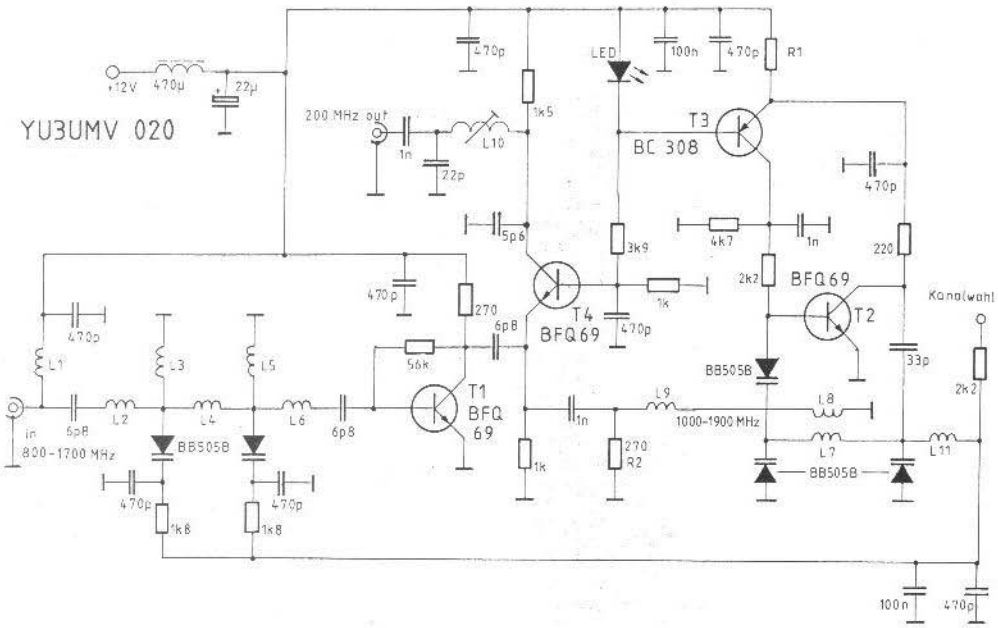

Fig. 14: Circuit diagram of the second tunable down-converter 800 to 1700 MHz/200 MHz (YU 3 UMV 020)

frequency coverage of the VCO is smaller and the tracking between the VCO and the input tuned filter is easier to achieve, second, due to the parasitic inductivity of the varicap diodes in the input filter, their self-series resonance falls almost exactly on the image frequency in a wide frequency range yielding a 40 dB overall image rejection in the band center in spite of the poor diode Q-factor. This is the really rare occasion that the parasitic inductivity of a component turns out to be so useful!

Of course it is not easy to build a broadband oscillator with poor-performance varicap diodes. Generally, an oscillator consists of a phase-shifting network that determines the oscillation frequency and an amplifier to compensate for the losses in the phase-shifting network and supply some power to an external useful load. In the real world, the amplifier has its own phase shift which is also frequency dependent, normally just in the opposite direction of that required to build a broadband VCO. Therefore the phase-shifting network must also compensate the phase shift of the amplifier and this limits the frequency range covered. From the above, it is evident that it is not possible to build a broadband VCO with a single poor - performance tuning element, like either one or more varicap diodes connected as a single variable capacitor. The solution is to split the required phase shift between two or more phase-shifting elements.

The VCO, shown here, uses three varicap diodes connected in a phase-shifting network between the collector and base of the oscillator transistor T 2 (BFQ 69), operating as a common emitter amplifier. L 11 is a $\lambda / 4$ choke feeding the tuning voltage, only L 7 has a role in determining the oscillator frequency. The output is taken through an

inductive link (L 8). Note that the varicap diode, connected to the base, receives a slightly lower bias voltage than the remaining diodes. This is certainly not ideal, but the bias network required, to supply all the diodes with the same voltage, would introduce very high parasitics. A wideband oscillator transistor requires an accurate bias network to obtain the best possible performance. T 3 (BC 308) stabilizes the operating current through the oscillator transistor T 2. The LED diode is a very good 'zener' diode for about 2 V.

In comparison with a real zener diode, it has a lower dynamic resistance, its temperature coefficient subtracts precisely from theT 3 BE junction TC and most important of all, it does not produce noise. As every feedback circuit, the bias network requires a frequency compensation to avoid instability and this is provided by the 1 nF capacitor between the collector of T 3 and ground.

The VCO shown, can (depending on component tolerances and construction) usually cover the frequency range from 800 MHz up to 2000 MHz in a single tuning voltage sweep from 0 V to 35 V. This would allow a theoretical converter input frequency range from 600 MHz up to 1800 MHz. Of course, it is impossible to obtain a good tracking with the input filter across the whole mentioned frequency band. Practically the 800 to 1700 MHz band can be covered with relatively little gain variation. With the outdoor unit, described in (1), the gain variation across the 850 to 1600 MHz frequency range, supplied by the outdoor unit, is in the 10 to 15 dB range with a maximum in the band center and a sharp drop-off at the band edges. This gain variation is, however, mainly caused by the three-stage first IF amplifier of the outdoor unit.

The mixer employs a single transistor T 4 (BFQ 69) in common base configuration. Both the input and oscillator signals are fed to the emitter. L 8, L 9 and the 1 nF capacitor represent a high impedance for the input frequency and at the same time a low-impedance return path for the 200 MHz second intermediate frequency. The nominally 270 Ω resistor from L 9 to ground is used to suppress a parasitic resonance that may cause spurious oscillations of T 4. The Pi filter at the mixer output transforms the high T 4 collector output impedance down to about 50 Ω and filters out the rests of the local oscillator signal. Due to the wide relative bandwidth of the signal at 200 MHz, the output circuit has to be dampened by the 1.5 kΩ resistor.

Other types of mixers were tested also with satisfactory results, in particular a single-ended common emitter BFQ 69 mixer and a balanced Schottky diode mixer. The common base mixer has less gain variation across the frequency band than the common emitter mixer and is much easier to build and cheaper than the Schottky diode mixer.

8.2. AGC Attenuator

The AGC attenuator module (**see fig. 15**) includes an AGC amplifier, a PIN diode driver stage and an electronic Pi attenuator with three PIN diodes. The AGC amplifier I 1 (741) is an operational amplifier connected to compare the AGC voltage, incoming from the AGC detector, with the voltage preset with the 'AGC level' potentiometer. The gain of the amplifier is limited to about 150 with a resistor network. The 330 nF capacitor, connected between the input and the output of the op-amp, determines the AGC time constant. The latter is not critical since the receiver processes a frequency-modulated, constant amplitude signal. It is only necessary to ensure that the AGC feedback loop is stable. When the AGC ON / OFF switch is open, I 1 works as a voltage follower and the 'AGC level' potentiometer allows a manual gain control.

The PIN diode attenuator follows the standard design used in some TV tuners. The PIN diode driver stage supplies the PIN diodes with appropriate currents so that both the input and the output impedances of the attenuator are close to 50 Ω regardless of the actual control voltage. Decoupling capacitors are included at both input and output. L 12 is only a choke for 200 MHz.

8.3. Second IF Amplifier and AGC Detector

The second IF amplifier and AGC detector module (**fig. 16**) includes three, almost identical,

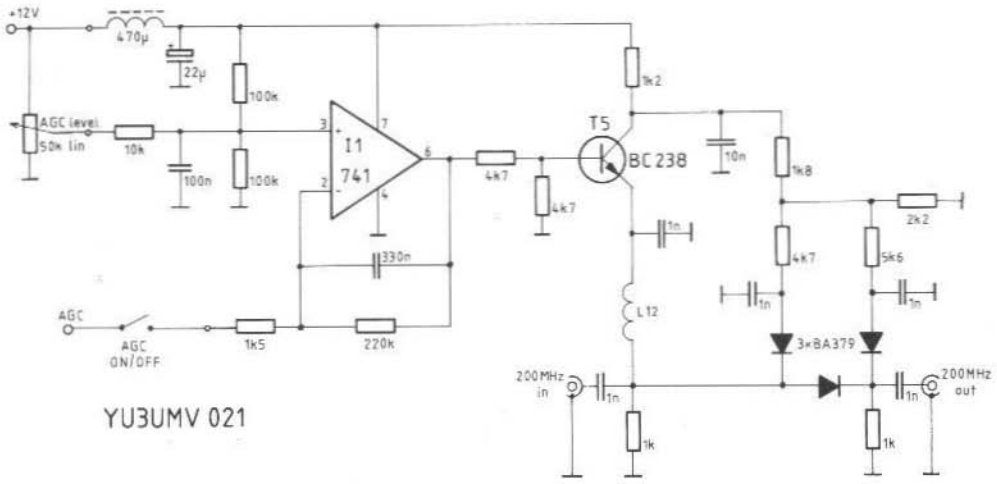

Fig. 15: Circuit diagram of the AGC attenuator YU 3 UMV 021

broadband amplifier stages at 200 MHz, an AGC detector (I 2) and corresponding amplifier (I 3). BFR 90 (or BFR 34 A or similar) bipolar microwave transistors are used in all the three amplifier stages since MOSFETs can not give sufficient bandwidth and usable gain at the same time. Of course, bipolar transistors also have some disadvantages, i. e. they have an extremely high gain at low frequencies and they still have some gain at frequencies much above 200 MHz. To avoid oscillations and overload problems at low frequencies (below 50 MHz), a 1 kΩ / 1 nF feedback network is added to each transistor. The coupling between the amplifier stages is made with series resonant circuits to further limit the gain at very high and very low frequencies and to provide some selectivity. Finally, the high-frequency gain is limited by the small capacitors connected between the base of each transistor and ground. Incidentally, these capacitors improve the matching and the bandwidth at 200 MHz. Although the gain of the transistors is small above 1000 MHz, this frequency range should be rejected to avoid saturating the amplifier with the second local oscillator signal.

The output of the amplifier is fed through a small capacitor to the PLL demodulator since the signal level, required by the latter, is smaller than that required by the AGC detector. The AGC detector I 2 (SO 42 P) is a multiplier / squarer circuit. Since a signal, multiplied by itself, gives also a DC component proportional to the signal power – a squarer circuit is an ideal power detector. The main advantages over conventional diode detectors are that a squarer IC is able to reliably detect RF voltages of only a few millivolts and due to its symmetrical monolithic construction, it does not suffer from thermal instability problems.

The output of I 2 is available as a voltage difference between the two output pins. The operational amplifier I 3 (741) transforms this voltage difference into an AGC voltage referred to ground. The zero signal level can be adjusted with the 10 kΩ trimmer. The polarity of the signal is selected so that the output voltage increases when the RF signal level increases.

The output of I 3 (741) can not reach ground since it operates with a single positive power supply. This does not disturb the operation of the AGC

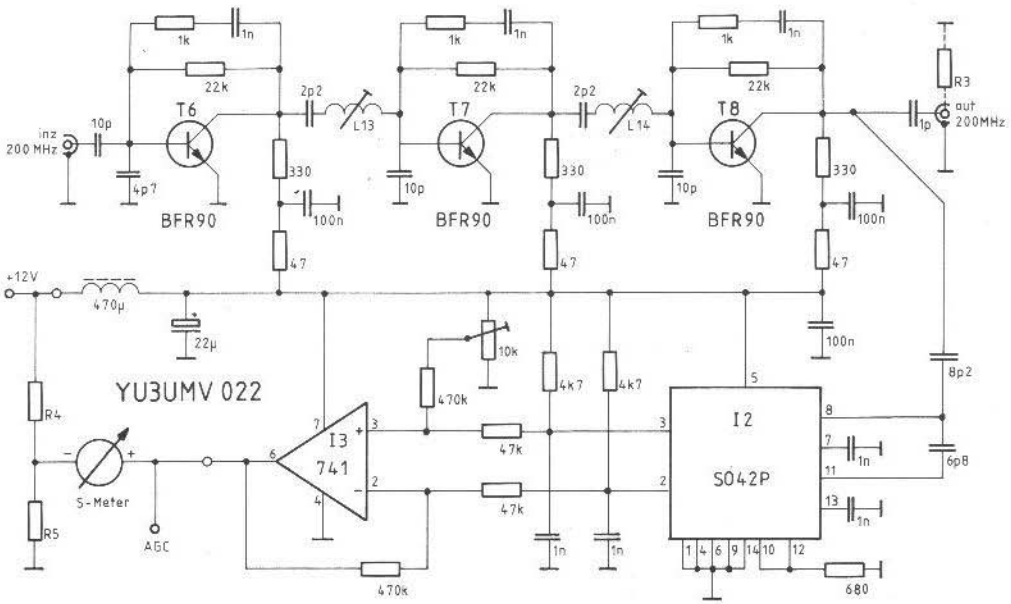

Fig. 16: Circuit diagram of the second IF amplifier and AGC detector YU 3 UMV 022

attenuator module, however, the level indicator's (S-meter's) negative contact should be connected to a resistive divider instead of being grounded.

8.4. PLL Demodulator

The PLL demodulator module (**fig. 17**) includes a PLL circuit with a current-controlled oscillator, a phase detector and a loop amplifier, and a video amplifier including the de-emphasis network. The PLL loop must be fast enough to track the wide and fast deviation of the pre-emphasized video signal frequency-modulated carrier. Phase-locked-loops are not very stable feedback loops. The reason is very simple: a phase detector controls the frequency of an oscillator introducing a 90 degree theoretical phase shift. The delay of all other components has to be kept below 90 degrees to keep the total phase shift below 180 degrees and the feedback loop stable. All the components of a video demodulator phase-locked-loop should therefore not only be able to operate at video frequencies but also to introduce a minimum phase delay up to a few MHz. A monolithic integrated circuit, including all the components of a PLL, is certainly the best solution.

Unfortunately, suitable integrated circuits are not yet easily available and are certainly not cheap. Cheap PLL ICs, such as the NE 560, NE 561 or NE 564 types, can only operate up to 60 - 80 MHz and their performance as wideband video demodulators is marginal at best. A PLL circuit, built from discrete components, was finally chosen: at least the performances of the various stages could be tailored as required.

The phase detector of a threshold extension PLL demodulator must operate in a linear input signal mode. The input signal level directly influences the phase detector gain and as a consequence

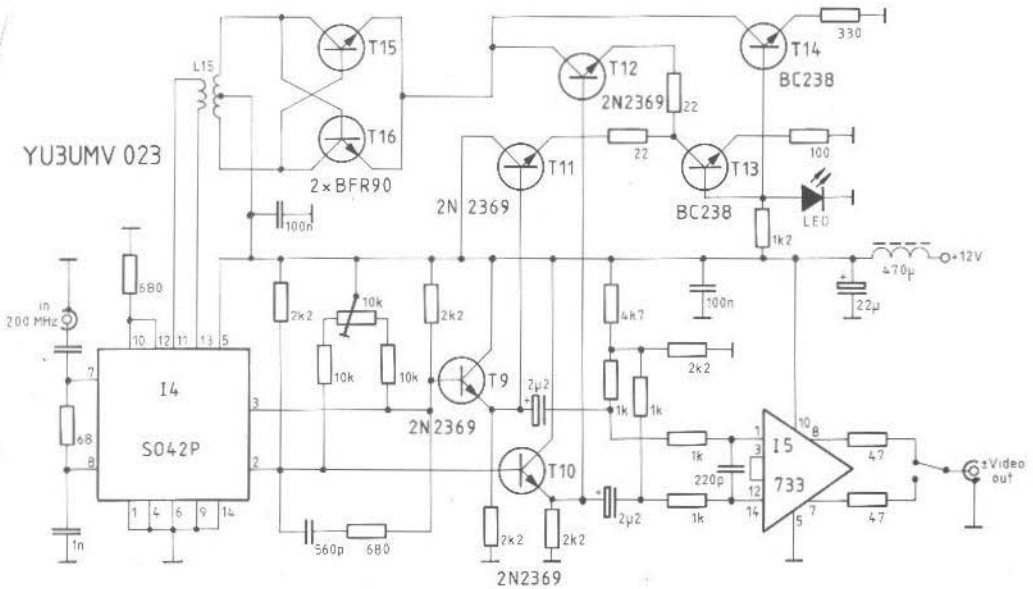

Fig. 17: Circuit diagram of the PLL demodulator YU 3 UMV 023

the loop gain and the demodulator bandwidth. Adjusting the input signal level with the AGC level' controls, the width of the demodulator and the actual amount of threshold extension can be adjusted. Unlike conventional discriminators, a threshold extension PLL demodulator is not affected by out-of-band signals or noise as long as these do not overdrive the phase detector out of its linear range. Since all the signals in the satellite bands are of the same order of magnitude, only a rough selectivity is required in front of the threshold extension PLL demodulator to avoid overload problems while the demodulator itself determines the receiver bandwidth and selectivity. A side advantage of a PLL demodulator is that a complex and / or expensive IF filter can be avoided.

The phase detector is a balanced mixer integrated circuit I 4 (SO 42 P), which has two symmetrical high-impedance outputs. A loop filter network is connected between these outputs to compensate the phase response and improve the loop stability. A symmetry trimmer is added to compensate the tolerances of both the phase detector and the subsequent loop amplifier. T 9 and T 10 (both BC 413) are emitter followers to decrease the phase detector's output impedance feeding the differential loop amplifier and the output video amplifier. A differential circuit is required for the loop amplifier (T 11 and T 12) since it has an excellent DC stability. The differential stage is supplied by a constant current source (T 13). The output of the differential stage is a current to control the oscillator. Another constant current source (T 14) supplies a bias current to the oscillator.

A current-controlled oscillator is used in place of a more common voltage-controlled oscillator since its frequency can be controlled much faster than the voltage across a varicap diode. The current-controlled oscillator is a blocking oscillator, built with two RF transistors T 15 and T 16 (both

BFR 90 or BFR 34 A or similar), acting as a negative resistance and a center tap coil (L 15). The frequency of such an oscillator, neglecting the parasitic effects, is exactly inversely proportional to the DC current flowing through the circuit. Since the dynamic impedance of the circuit is small, it is almost an ideal load for the differential loop amplifier and the phase delay, introduced by the loop amplifier, is very small. The output signal is taken with a link to L 15 to feed the phase detector I 4.

Part of the phase detector output signal is AC-coupled to the input of the video amplifier I 5 (733). Just in front of the video amplifier, a simple de-emphasis network is inserted consisting of a simple RC lowpass cell. The latter was found suitable for all available satellite TV transmissions – in any case, this part of the circuit is not critical at all. After the de - emphasis, the video signal level is very low and a high-gain (34 dB) video amplifier is required to obtain a standard video signal level in the 1 Vpp range. The video amplifier I 5 has two outputs of both polarities. These are fed to a video polarity selector switch. The video polarity of an FM signal may be inverted after a down-conversion, if the local oscillator operates above the input signal frequency. Since outdoor units for the 11 GHz band usually have a local oscillator around 10 GHz while the 4 GHz band outdoor units have a local oscillator around 5 GHz, the demodulated signal from the latter will have its polarity inverted when compared with that obtained from the former. Finally, some stations already transmit with the polarity inverted.

8.5. AM Video Modulator

The AM video modulator module (**fig. 18**) includes a video clamping stage, a VHF AM modulator and two emitter followers for impedance matching. After the first emitter followers stage T 17 (BC 308), the video signal is capacitively coupled to the emitter of the clamping transistor T 18 (BC 413). Since the video signal level is much

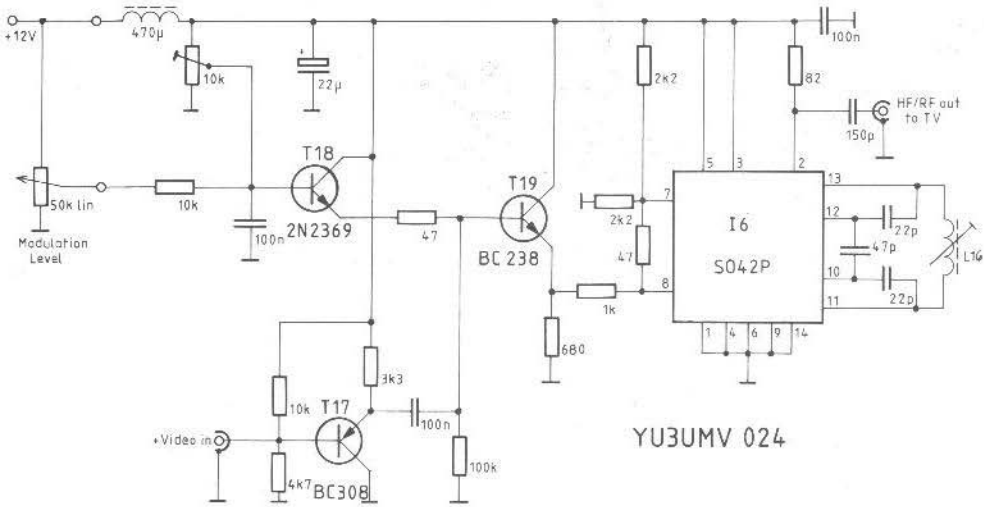

Fig. 18: Circuit diagram of the AM video modulator YU 3 UMV 024

larger than the T 18 BE junction 'knee', T 18 conducts only during the most negative tips of the video signal. The time constant of the circuit, set by the 100 nF coupling capacitor and the 100 kΩ resistor to ground, is set so that T 18 conducts on each horizontal sync pulse, each time resetting the DC level of the video signal applied to the base of T 19 (BC 238). In this way, the video clamping stage restores the DC level of the video signal and rejects all low-frequency disturbances such as the spectrum dispersion waveform. The actual base DC level can be adjusted roughly with the 10 kΩ trimmer, a fine adjustment can be made with the front panel modulation level control potentiometer.

The modulation level control is necessary since not all satellite TV transmissions have the same deviation. An undermodulated TV picture looks rather dark on the TV receiver, but it does not show other defects. An overmodulated TV picture shows defects first on the brightest parts: saturated white and inverted colours in the case of the PAL colour system. Another SO 42 P (I 6) is used as a self-oscillating VHF band 1 AM modulator. The output frequency can be adjusted with L 1 between about 45 MHz and 65 MHz (VHF channels 2, 3 and 4). Of course, a free channel should be selected. Note, however, that the output of I 6 is rich in harmonics so that it should be well-filtered if it is to be combined with other terrestrial broadcast channels in a common antenna installation. In any case, the generated VHF AM signal only contains the original audio subcarrier, which is normally different from the 5.5 MHz terrestrial television standard.

8.6. Sound Demodulator

Although many different systems are being used for the transmissions of the corresponding sound information, the analogue frequency-modulated subcarrier system is the most popular. Satellite TV signals have different sound subcarrier frequencies, however, 6.6 MHz or 6.65 MHz are generally used for the main audio channel. Up to four additional audio subcarriers may be present carrying stereo audio, sound commentry in other languages, independent radio-broadcast sound channels and / or test signals. Sound subcarriers also have widely different pre-emphasis and deviation and some also have the dynamic range companded. Finally, some TELECOM 1 a and 1 b spacecraft transponders are being used exclusively for radio broadcast: the 12.6 GHz carrier is only modulated with the spectrum dispersion waveform and four audio subcarriers carrying two stereo radio broadcast pairs.

The sound demodulator module (**fig. 19**) is suitable for conventional analogue sound subcarriers. It includes an IF amplifier, a discriminator and an audio amplifier. All the active components are included in a single integrated circuit I 7 (TDA 1190 Z), which is a complete sound demodulator for TV receivers. The main difference from the circuit for a conventional TV receiver is that the input filter and the discriminator tuned circuit are tunable from about 5 MHz up to 8 MHz with varicap diodes instead of being fixed-tuned to 5.5 MHz. The input filter, including L 16, L 17 and the two varicap diodes, is designed for narrow-deviation signals and may cause a slight distortion of some widely modulated subcarriers. The coupling between the two resonant circuits is through the 2.2 nF capacitor connected from the BB 204 twin varicap diode common cathode lead to ground. The discriminator circuit (L 18) is tuned with another BB 204 with the two halves connected in parallel.

The TDA 1190 Z is not designed to have a low-level discriminator output nor a separate audio amplifier input, it has only an input (pin 6) for a DC volume control. The volume is at maximum when the DC volume control potentiometer is at minimum. If the volume control pin is left open, the volume is practically cut off. Fortunately the audio amplifier section of the TDA 1190 Z is still operating in this condition and pin 12 can be used as an audio input, for example to monitor the video signal when adjusting the antenna and / or receiver. To select the desired signal, audio or video, a 2 x 2 switch is required as shown in **fig. 19**. This detail is intentionally simplified on the block diagram in fig. 13.

8.7. Regulated DC Voltage Converter

A practical solution to obtain the supply voltage for the varicap diodes is to use a simple regulated voltage converter as shown in **fig. 20**. T 20 (BC

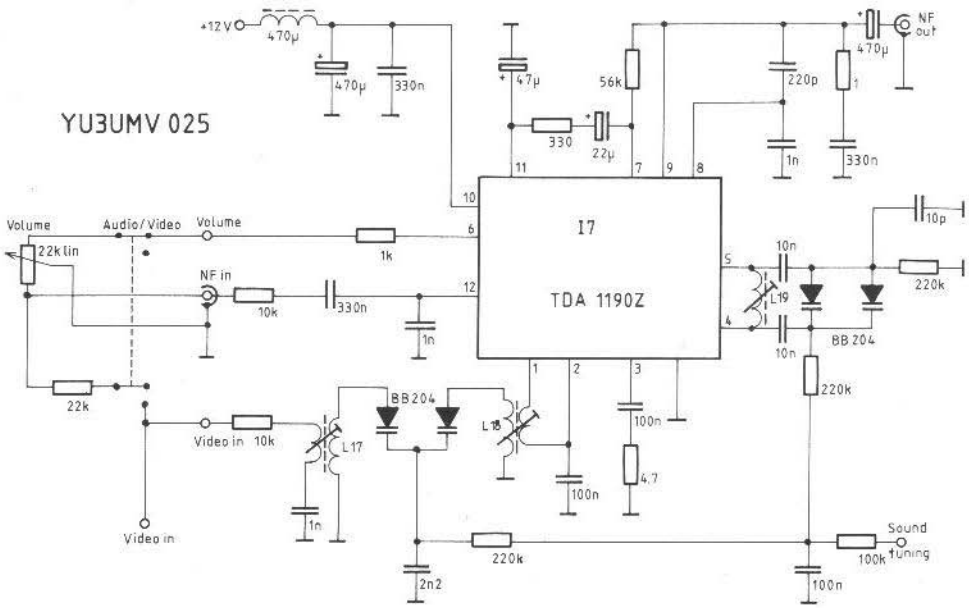

Fig. 19: Circuit diagram of the sound demodulator YU 3 UMV 025

213) and T 21 (2 N 1711) form a blocking oscillator. The energy stored in the 470 μH choke during the conducting phase of T 21 is released as high-voltage spikes which are rectified by the 1 N 4148 diode to charge the 22 μF capacitor. When the voltage across this capacitor reaches a determined value, the 10 V zener diode connected to the resistive divider starts conducting and turns on the regulating transistor T 23 (BC 238). The latter proportionally dampens the oscillations to stabilize the output voltage.

In spite of the simple circuit, the efficiency is good. The output voltage stability mainly depends upon the zener diode used. Of course, both the input and the output of the converter must be well-filtered to avoid disturbing other circuits of the indoor unit. The two tuning potentiometers shown in **fig. 20** only represent the simplest solution. A TV tuner potentiometer keyboard can replace the channel tuning potentiometer. A switch to expand the range of the sound tuning potentiometer around 6.6 MHz is also very convenient. Finally, one of the TV remote control IC sets could be used to control both the channel tuning voltage and the sound tuning voltage.

9. CONSTRUCTION

9.1. Construction of the Second Tunable Down-Converter

The second tunable down-converter cannot be built on a printed circuit board and its construction requires a lot of care to match the results of the prototypes. The components should be installed 'in air' as shown in **fig. 21** using a tinned un-

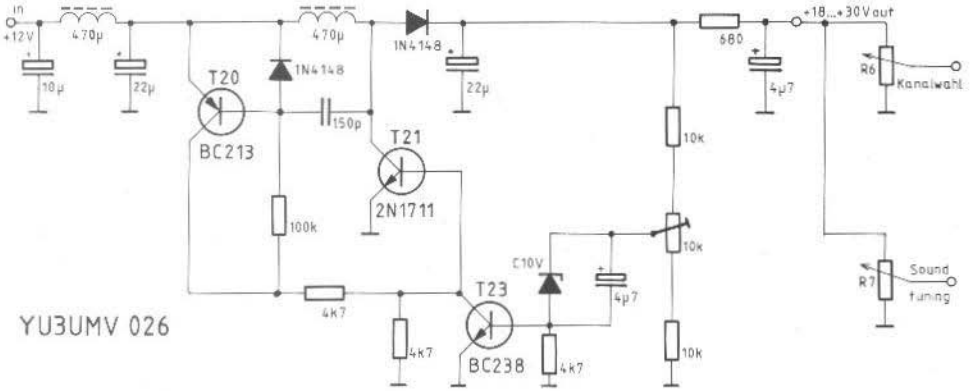

Fig. 20: Circuit diagram of the regulated DC-voltage converter YU 3 UMV 026

etched piece of PCB laminate of about 50 x 120 mm as a support and as a ground plane for the circuit. All the 470 pF capacitors are leadless ceramic discs of 5 mm diameter soldered to the ground plane and used also as supports. The 5.6 pF capacitor (collector of T 4) is a trapezoidal ceramic chip. All the other low-value capacitors are ceramic discs of 5 mm diameter, or smaller, with 0.4 mm diameter wire leads. The resistors are all 1/8 W miniature types. There are also a few supports, made of small rectangles of double-sided, 1.6 mm thick, glassfiber-epoxy PCB lami-

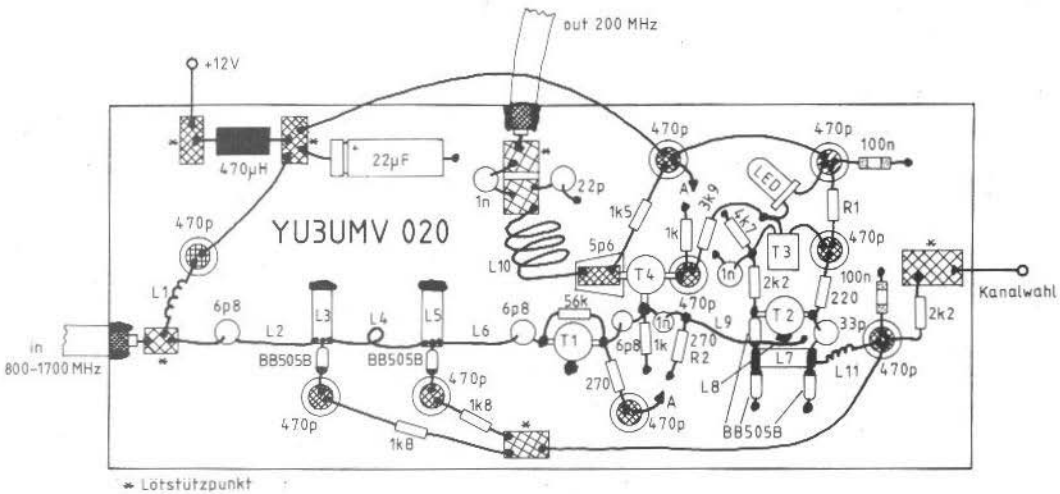

Fig. 21: Construction of the second tunable down-converter YU 3 UMV 020

nate, to improve the mechanical stability of the circuit.

L 1 and L 11 are λ / 4 chokes made of about 6 cm of 0.15 mm thick CuL wire, wound on a 1 mm internal diameter forming a self-supporting coil of 12 - 14 turns. L 3, L 5 and L 7 are made of 3 mm wide strips of 0.1 mm thick copper foil. The length of L 3 and L 5 is 7 mm and they are kept 1.5 mm above the ground surface. The strips, to build L 3 and L 5, are first cut to about 11 mm. Then each strip is bent twice and the remaining 2.5 mm are used to solder the cold end to ground.

L 7 is supported by the varicap diodes and the 33 pF ceramic disc capacitor about 2 mm above the ground plane. The effective length of L 7 is the distance between the two BB 505 B varicap diodes connected to ground. This should be 7 mm and the length of the strip required to build L 7 is about 8 mm.

L 8 should run parallel to L 7 for at least 5 mm at a distance of 0.5 mm. Both L 8 and L 9 are built from one of the leads of the 1 nF capacitor and are kept about 2 mm above the ground surface, their compressed length is about 17 mm.

L 2 and L 6 are also built from the corresponding capacitor leads and are 10 mm long and kept 2 mm above the ground plane.

L 4 is a loop of 4 mm internal diameter made from 0.4 mm diameter wire plus the connecting leads to couple L 3 and L 5, which are spaced by 15 mm. Finally, L 10 has 4 self-supporting turns of 0.7 mm diameter CuL wire with a 5 mm internal diameter.

All the critical frequency determining components should be installed exactly as shown on **fig. 21** with the shortest possible leads. In practice, the leads of the transistors and varicap diodes are first shortened to 1.5 - 2 mm and well-tinned. Note, that not all the BFQ 69 transistors are oriented in the same way.

A power supply jumper is omitted for clarity, it is only marked with the two arrows with the letter "A" on the drawing. The circuit does not require any additional shielding. In any case, the components must be accessible for the alignment.

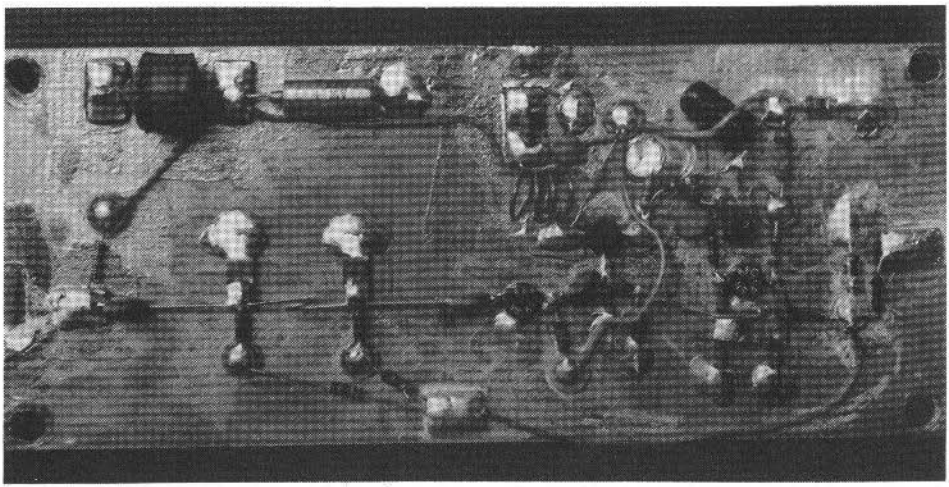

Photo A: Prototype of the PCB YU 3 UMV 020

9.2. Construction of the Remaining Modules

All the remaining modules are built on single-sided printed circuit boards. The comp. loc. plans are shown in **figures 22 to 27**. All the components are installed in the conventional way except the BA 379 PIN diodes and the BFR 90 transistors. The BA 379 diodes are installed below the printed circuit board YU 3 UMV 021 into 4 mm diameter holes drilled at the marked positions. The BFR 90 transistors of PCBs YU 3 UMV 022 / 023 are installed in a similar way into 6 mm diameter holes. The two current-controlled oscillator transistors are both installed in a single hole. The two flat transistors are first soldered together, one over another, and then the combination is put in place on the printed circuit board.

L 12 from the AGC attenuator and L 13 and L 14 from the second IF amplfier are self-supporting coils of 5 turns of 0.7 mm CuL wire wound on a 5 mm internal diameter each. The complex tapped coil L 15 of the current-controlled oscillator is etched on the printed circuit board YU 3 UMV 023 and only requires a few jumpers of 0.4 mm diameter wire (ex-component leads).

L 16 from the AM video modulator should have about 0.7 μH – in practice, 9 turns of 0.15 mm dia CuL wire on a 4 mm dia support with core and ferrite cap used for TV IF transformers.

The coils of the sound demodulator YU 3 UMV 025 are wound on 10.7 MHz IF transformer supports. L 17 and L 18 have 28 turns each of 0.1 mm dia CuL wire and links of 6 turns each of the same wire. L 19 only has a winding of 20 turns of the same wire. The inductance of the resonant windings of L 17 and L 18 should be 18 μH and L 19 should have a nominal inductance of 9 μH.

The completed printed circuit boards should be installed in a metal case about 7 - 9 mm above a metal ground plane. No additional shields are required if the PLL demodulator and VHF AM video modulator modules are sufficiently spaced (10 - 15 cm) from the low-level input modules (second tunable down-converter, AGC attenuator and second IF amplifier),for example installing in the free space in between 'neutral' modules, like the sound demodulator or the De-voltage converter. A mains transformer will also not disturb the circuit if it is at least a few cm away from the printed circuit boards.

10. ALIGNMENT

The most critical part of the second tunable down-converter (**fig. 14**) is the broadband VCO. Firstly, the DC operating current of the VCO transistor T 2 should be checked and corrected if required acting on the 47 - 56 Ω resistor in the emitter of T 3. If the collector current of T 2 is below 18 - 22 mA, there is danger of unstable oscillations and a discontinuous tuning curve. On the other hand, if the current is too high, the maximum frequency can not be reached. The operation of the VCO across the whole band should now be checked. The maximum frequency (tuning voltage 35 V) should be around 2 GHz. This can be adjusted by acting on the distance of L 7 from the ground plane. If the VCO stops oscillating at low-tuning voltages, the distance between L 7 and the ground plane is too small and as a consequence the inductance of L 7 is too small for proper VCO operation. Another possible cause is an improper installation of the varicap diodes or other components, especially if their leads are left too long. Practically it is sufficient that the oscillator operates reliably down to a tuning voltage of 2 - 3 V. The VCO should now be slowly tuned across the whole frequency band checking the output for unstable oscillations and / or frequency jumps. If a spectrum analyzer is not available, the voltage on the collector of T 3 is a good indication of the status of the oscillator. A conventional low-frequency (10 MHz) oscilloscope is sufficient to detect parasitic oscillations or sudden voltage jumps. The T 3 collector voltage must vary smoothly with the tuning voltage if the VCO is oscillating properly. The VCO output level can now be estimated by checking the DC voltage on the emitter of T 4 (through a RF choke). This is around 1.5 V without any VCO signal. Applying the signal, it should increase by a few

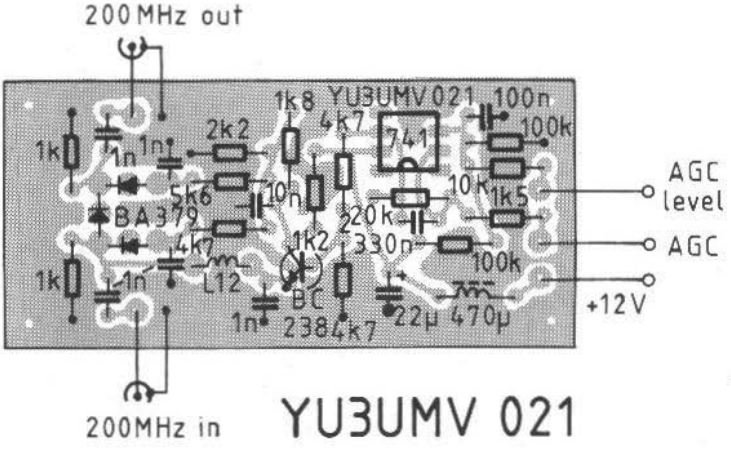

Fig. 22: Component plan of PCB YU 3 UMV 021 (AGC attenuator)

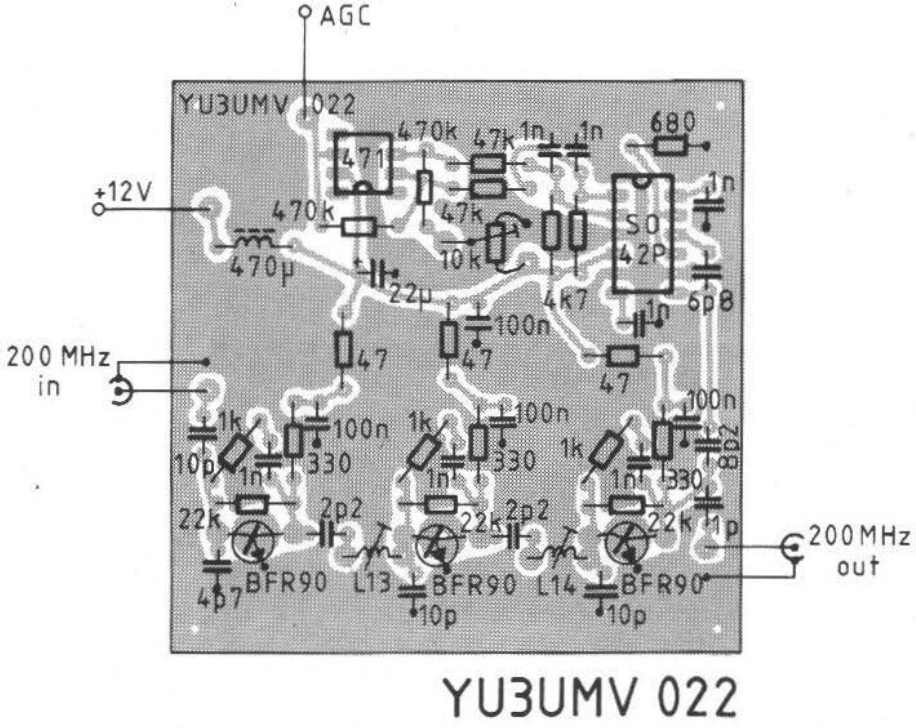

Fig. 23: Component plan of PCB YU 3 UMV 022 (second IF amplifier and AGC detector)

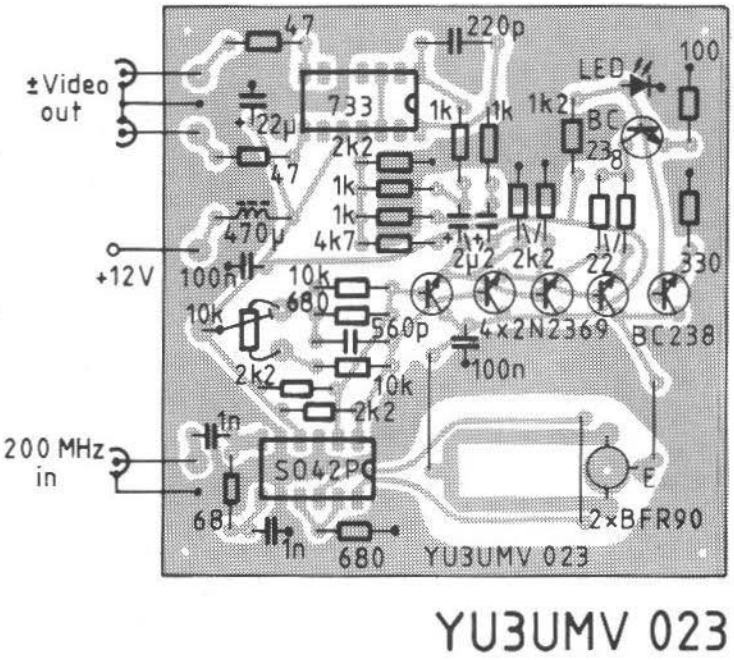

Fig. 24: Component plan of PCB YU 3 UMV (PLL demodulator)

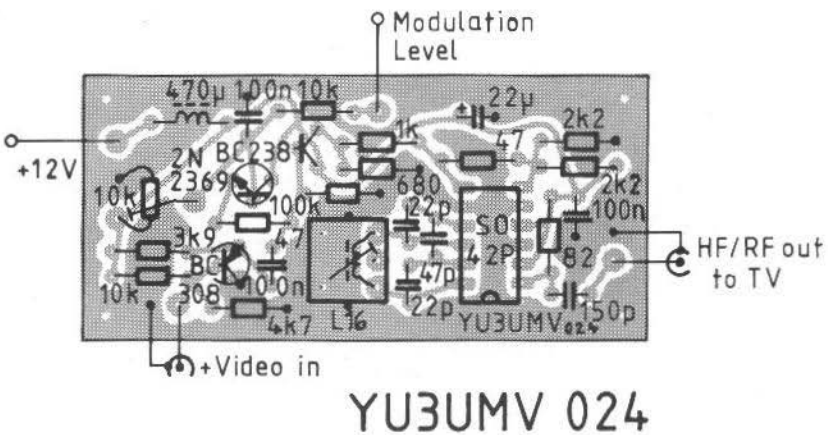

Fig. 25: Component plan of PCB YU 3 UMV 024 (AM video modulator)

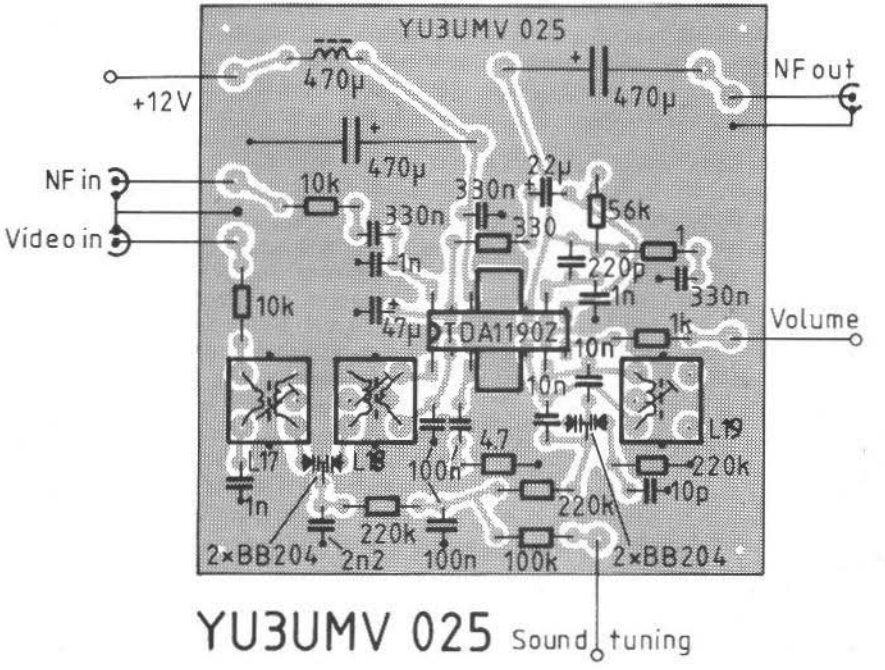

Fig. 26: Component plan of PCB YU 3 UMV 025 (sound demodulator)

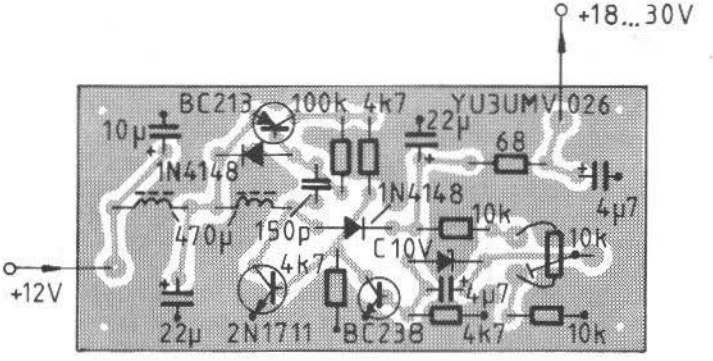

Fig. 27: Component plan of PCB YU 3 UMV 026 (regulated DC-voltage converter)

hundred mV in the band center and less at band edges. The input tunable filter usually does not require any adjustment. In any case, the tracking with the VCO can easily be checked later, when all the receiver modules are operating.

The operation of the AGC attenuator module (**fig. 15**) and the second IF amplifier and AGC detector module (**fig. 16**) can be checked using a noise generator (see part 1) as a signal source. The zero signal level AGC voltage should be adjusted with the corresponding trimmer to 2.5 to 3.5 V. Resistors R 4 and R 5 should be selected so that the full scale deflection of the level indicator corresponds to about 6 V difference of the AGC voltage.

L 13 and L 14 in the second IF amplifier are tuned by adjusting the spacing of the turns to make the gain maximum coincide with the desired band center. This is also valid for L 10 at the output of the second tunable down-converter. These adjustments are not critical at all and if suitable test equipment is not available, the turns of the mentioned coils can simply be spaced to about 6 - 8 mm total coil length.

The phase-locked-loop module should also be first checked alone. The current-controlled oscillator frequency should be 200 MHz +/- 15 MHz and should be adjustable for at least +/- 30 MHz with the 10 kΩ symmetry trimmer. Since the frequency depends on the bias current, it also depends on the LED used in the constant current sources. In the prototypes, red LEDs, producing a voltage fall of about 2 V, were used. Note that some older red LEDs only produce a voltage fall of about 1.6 V since they are based on a different semiconductor, while yellow and green LEDs have an even higher voltage fall. The PLL demodulator is also sensitive on the input termination impedance and in some cases it may lock on its own oscillator signal. To avoid this problem, it is recommended that the cable to the second IF amplifier is 20 - 25 cm long. A resistor across the output of the second IF amplifier (R 3 in fig. 16) of about 150 Ω will also help in solving this problem. Finally, the symmetry trimmer has to be adjusted to prevent this problem (usually close to the center).

The various modules of the indoor unit can now be installed in a suitable case, connected together and checked on a live satellite signal incoming from an operating outdoor unit. To search for a satellite signal, the audio amplifier has to be connected directly to the output of the PLL demodulator. When the characteristic frame frequency hum is heard, a TV monitor can be connected. Only when a reasonable-quality stable image is obtained on the TV monitor, adjusting both the channel frequency and the signal level, the alignment of the VHF AM video modulator can be performed. Finally, the sound tuning voltage is adjusted between 5 and 10 V to detect the (main) sound subcarrier. Then L 17 and L 18 are adjusted for the best signal-to-noise ratio and minimum distortion and L 19 is adjusted for the maximum undistorted audio output. Of course, it is assumed that the selected satellite transmission is an ordinary PAL (or SECAM or NTSC) transmission and that it has an FM sound subcarrier.

11. CONCLUSION

The satellite TV receiver indoor unit described is designed for amateur purposes, operating in 'amateur' conditions with relatively small antennas and poor signal-to-noise ratios. When a strong signal with a good signal-to-noise ratio is available, a conventional demodulator without threshold extension will probably provide better results. The sound demodulator is also designed for poor signal-to-noise ratios sacrifying the audio quality. The IF band used, 200 MHz, is not very standard, however, the second tunable down-converter can easily be modified for 480 MHz replacing the VCO transistor T 2 (BFQ 69) by a better microwave type (BFQ 74) in order to reach the higher frequency. In this way, standard 480 MHz IF components can be used (2). A converter for the audio subcarrier could also be added to feed a standard 5.5 MHz subcarrier to the TV receiver.

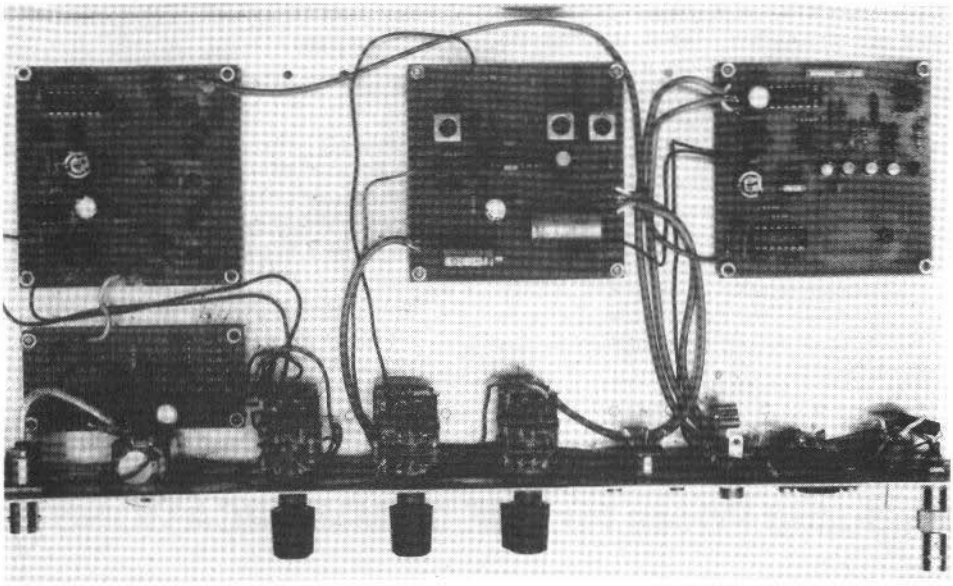

Photo B: One of the older prototypes YU 3 UMV 021 (left down), 022 (left upper), 025 (middle) and 023 (right)

The satellite TV receiver indoor unit, shown in this article, is suitable for conventional wideband FM video with an FM sound subcarrier since most present-day satellite TV transmissions use this system. A few transmissions are scrambled: they are intentionally coded so that they can not be received by unauthorized stations. Due to the narrow available bandwidth and low transmitter power, little scrambling can be done to the video part of the signal – video scrambling therefore only includes video polarity inversion, random line delay (discret scrambling system) or substitution of sync pulses (oak-orion scrambling system). A descrambler (decoder) for the video signal should be inserted between the PLL demodulator and the AM video modulator (or TV monitor). The corresponding sound channel is usually not intentionally scrambled, but other sound systems (especially digital sound-in-sync systems) are considerably more difficult to decode than the simple FM sound subcarrier system.

A new TV transmission system called 'MAC' is slowly being introduced in satellite TV transmissions. The acronym 'MAC' means 'multiplexed analogue components'. In the MAC standard, the colour and sound information is not transmitted as modulated subcarriers. The components of the TV signal, luminance, colour and sound, are first time-compressed and then transmitted sequentially in the time interval occupied by a single TV line. In fact, the sound is first transformed in a digital format. The luminance and the colour are transmitted using wideband frequency modulation, while the synchronization and the sound channels are transmitted as PSK bursts during the horizontal flyback interval. The advantages of the MAC standard are: improved signal-to-noise ratio and increased bandwidth of the video signal and a number (4 or 8) of top-performance sound channels. Unfortunately, the MAC standard also has a major disadvantage: the decoder / demodulator required is very complex and expensive and it is not yet clear whether the complex and fast (20 MHz clock) logic, memories and A / D and D / A converters can be

integrated in a few VLSI chips to decrease the price and improve the reliability. A further disadvantage is, that there are a number of incompatible variants and subvariants of the MAC standard called B-MAC, C-MAC, D-MAC, D 2-MAC ...

The actual sat-receiver design for the MAC standard is the same as for the conventional PAL (or SECAM or NTSC) standard up to the demodulator. In addition to a wideband FM discriminator, a MAC receiver requires a PSK (phase-shift keying) demodulator. The output of a MAC decoder is a RGB signal suitable to feed directly a colour cathode-ray tube.

12. LITERATURE

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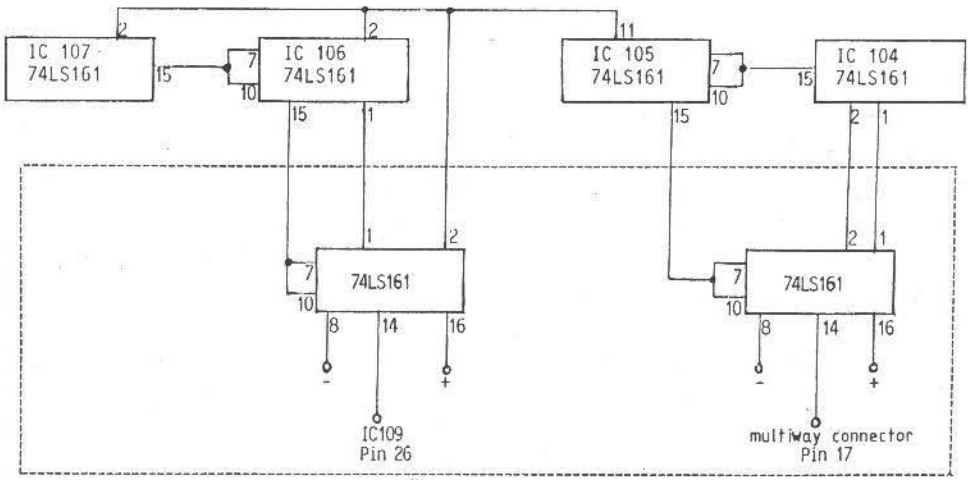
Dirk Petig, DD 1 PE

Colour Test-Image Generator – Improved Resolution

Better resolution / more picture dots (pixels) with the DC 1 BP colour test-image generator (VHF COMMUNICATIONS 4/1984 Pages 194 - 204)

The colour test-image generator is still, on account of its good basic design, being built by amateurs and works very well. The resolution of 128 x 64 pixels, however, leaves much to be desired. Recently, the larger EPROMs are becoming more affordable and it has become worthwhile to modify the generator with an extension comprising two 74 LS 161 chips together with an EPROM 27128 A, in order to improve the resolution. This is accomplished by a picture made up of 256 x 128 pixels, the colours remaining the same. As the circuit now works at a pixel frequency of 9.8 MHz, it is necessary to use a fast EPROM capable of working at speeds of 200 ns maximum otherwise the pulse conditioning circuitry tends to



The part of the circuit within the dotted rectangle is added to the original circuit

Fig. 1: Colour test-image extension DD 1 PE

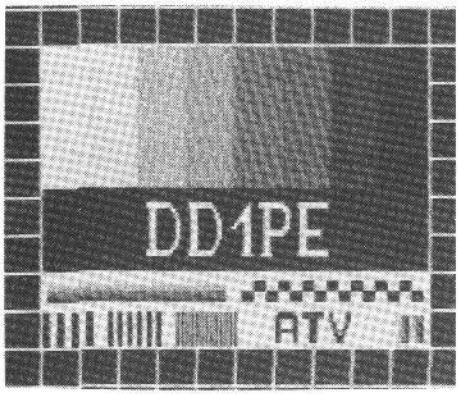


Fig. 2: Original test-image with 256 x 128 pixels following the generator extension

cause some interference. By modifying the circuit, of course, the make-up of the whole picture is changed and not just the number of pixels.

New Picture Card Format

As the pixel frequency is doubled, one gets in the horizontal plane two pictures next to each other. In order, however, that the same picture content is not written into both of them, a change-over to the second 4 bit is made after the middle of the picture. They represented, in the old 2764, the second stored picture which could be manually changed over. This gives, by using the old EPROM, 256 addressable points in 64 lines.

If now in the next step, a 27128 A is used, a doubling of the memory contents is obtained and again a second picture, manually switched, is ready for disposal. The vertical resolution, however, should also be improved. This is achieved by doubling the line frequency thus obtaining two pictures in vertical juxtaposition but containing the same information. The second 8 K of the large EPROM is then switched-in after the picture middle and obtaining thereby 128 effective lines. The whole presentation can still be elevated one step higher just by using the 27256 EPROM. It should, however, be capable of working with 150 ns but that costs a lot of money here, quite apart from the arduous programming effort that such a chip would require – it would take a whole weekend. Nevertheless, one can say that a resolution has been achieved which would render a circle drawn in the test-image to be acceptably reproduced.

Technical Circuit Alterations

For the doubling of the pixel frequency, C 103 will have to be reduced to 33 pF and R 105 adjusted to position the right test-image edge.
Pin 2 of both IC 106 and IC 107 is parted from the existing circuit i. e. the $\overline{\text{BLANK}}$-designated signal is no longer connected to these pins. The switch-over possibility on pin 17/18 of the multiway connector is now redundant.

Pin 2 of IC 106 and IC 107 are both connected together with IC 105 pin 11 (**fig. 1**).

A test-image of my design was realized using 256 x 128 picture elements in the 27128 A (**fig. 2**). In order to simplify the programming, an EPROM will be available from me which has the test-image detail shown but having a white field instead of my callsign. The required callsign may then be programmed-in later.

A PCB was not developed as the modification is not extensive and can be realized on a vero-card.

Practical Modification

IC 101 is, in the interests of reducing the heat loss, separated from the board. In its place, a small vero-board, with the two new ICs, is soldered-in. IC 101 is then placed on a large heat sink.

BRIEFLY SPEAKING...

Observations on "the YUØB Antenna"
VHF COMMUNICATIONS 2/1986

In this article, D. Dobričić, YU 1 AW, indirectly posed the question of whether the given formula (P. 68) for the stacking gain was also valid for antennas with parasitic elements. It would certainly be if through the coupling nothing altered but the radiation resistance. However, the real part of the impedance influences the phase position of currents in the individual elements. (These are predominantly reactive currents), and there can be no question about it, even in the circumstances where the coupling resistance X_{12} has no reactive component.

After compensating the tuning of the 2 λ Yagis, which were spaced at 0.65 λ according to my measurements, a gain of under 1.5 dB is obtained.

The DL 7 KM double-Yagi, which works using practically the same principle as the YUØB antenna, only exhibited a 1 dB gain improvement over a single normal Yagi of the same length.

It is not intended to suggest that an increased gain cannot be achieved by optimising the antenna spacing but only that the gain is not as high as that given in the article.

The recommendation to stack two double-Yagis in the H plane, however, remains unclear. According to fig. 4, the underlying suggestion is that the advantage of the 0.65 λ spacing for the both inner planes are almost compensated by the influence of the opposite outers at 1.3 λ spacing – which one cannot simply forget – whilst for these themselves, the particularly unfavourable spacing is somehow effective. in this case only a stacking gain of 1 dB over the normal can be expected. The closer supposition is, that with four Yagis of length 2 to 2.5 λ the same gain can be achieved as with a 4 x YUØB group and occupying the same space but with very much reduced weight and wind resistance.

A point in favour of the described arrangement is that the unequal power distribution favours the inner plane (approaching binominal distribution). This leads to a very clean radiation diagram – at least in the H plane.

When working at elevated attitudes (EME, MS, Satellites), this can be as decisive as the gain.

Guenter Hoch, DL 6 WU

Digital memory for SSTV, FAX and WEFAX
by ON 6 VD and DK 3 VF in VHF COMMUNICATIONS 1/1986

Walter Ernst, DJ 1 MC has taken the trouble to draw a complete circuit schematic in four parts together with a connection plan for the PCB DK 3 VF 001. He has very kindly put

the five DIN A 3 pages at the disposal of the editor for the benefit of the readers. This set of schematics will in future accompany every ordered printed circuit board. Previous customers for this board can obtain them cost-free by sending in a postcard.

The editor

An A / D - D / A Converter for Video

The firm Intermetall has had, since the end of 1985, an interesting chip available which consists of an 8 bit parallel analog / digital converter and a 10 bit parallel digital / analog converter together on the same chip. This chip, UVC 3100 (or 3101), is housed in a 40 pin housing together with auxiliary circuits such as: two separate reference voltage sources, a wide band buffer amplifier on input and output, a clamping circuit for the input signal and a level converter on the TTL compatible inputs and outputs.

Whilst the UVC 3100 in the DAC has an accuracy of 10 bit, the cheaper UVC 3101 has only an 8 bit accuracy. The supply voltages are + / – 5 volts at 120 mA max. The module is intended for use in satellite TV D 2 MAC decoders and in PAY TV descramblers and allows a maximum sampling frequency of 38 MHz to be employed. As internally, only static logic is used, the converter may be used in the LF range.

The price at 60 DM (approx.) is also interesting allowing the keen amateur experimenter to digitalize video signals. One of our first applications of this chip was for a picture memory in a METEOSAT receiver. This shows that the UVC 3101 is readily and easily put to use and also that completely separate uses of the two converters cause no problems.

Reference: Data sheet UVC 3100 / UVC 3101, ITT - Intermetall

DB 1 NV

Rigid PTFE-Substrate (Teflon)

It has recently become possible for the microwave engineer to utilize and work the rigid ceramic Al_2O_3 or BeO. The ceramic-filled, copper-sided RT/duroid substrate having a dielectric constant of 6 (RT/duroid 6006) or 10.5 (RT/duroid 6010.5) has been stiffened on the underside with a 0.5 - 6.35 mm film which is bonded to the dielectric. It therefore acts not only as a carrier and stiffener but also as a groundplane or heat sink. This rigid version of RT/duroid substrate opens up far-reaching possibilities for its application, such as power amplifiers, microstrip circulators, phase-controlled antennas etc. By means of spot-welding or parallel groove welds, diodes and transistors may also be bonded to the substrate.

The standard board's size is 254 x 254 mm and the maximum format being 508 x 508 mm. The conductor of the microstrip circuit may be etched on the topside in the conventional manner, the underside being covered with etch resist. By means of a special process it is also possible to through-contact the aluminium, stiffened RT/duroid substrate.

Manufactured and supplied in the Federal Republic of Germany by Mauritz GmbH & Co., Postfach 10 43 06,
2000 Hamburg 1,
Tel.: 040 – 24 16 54,
Tlx.: 2 173 816

MATERIAL PRICE LIST OF EQUIPMENT

described in edition 1 / 1987 of VHF COMMUNICATIONS

YU3UMV	**TV Satellite Receive System**	Art. Nr.	**Ed. 4/1986 and 1/1987**
YU3UMV 017 ... 019	Low-Noise 11 GHz Down-Converter (Outdoor Unit) Details of these 3 kits in Ed. 4/1986, Page 254	6981	DM 465.—
YU3UMV 020	**Second (tunable) converter (800 - 1700 / 200 MHz)**		
PCB	YU3UMV 020 unetched PCB material 120 x 50	6164	DM 5.—
Components	YU3UMV 020 4 transistors, 1 LED, 5 varicaps, 1 RFC, 1 piece Cufoil, 2 dia of wire 10 ceramic disc caps (leadless) 1 block cap, 5 ceramic, 5 disc caps, 1 tant. cap., 13 resistors	6165	DM 62.—
Kit	**YU3UMV 020 complete with all above parts**	**6166**	**DM 65.—**
YU3UMV 021	**AGC electronic attenuator**		**Ed. 1/1987**
PCB	YU3UMV 021 drilled, with layout plan	6167	DM 25.—
Components	YU3UMV 021 1 transistor, 1 IC, 3 pin diodes 1 RFC, 1 m CuL wire 0,7 dia, 7 block-caps., 1 tant. cap, 14 resistors,	6168	DM 28.—
Kit	**YU3UMV 021 complete with above parts**	**6169**	**DM 51.—**
YU3UMV 022	**Second IF amplifier and AGC detector**		**Ed. 1/1987**
PCB	YU3UMV 022 drilled, with layout plan	6170	DM 27.—
Components	YU3UMV 022 3 transistors, 2 ICs, 1 RFC, 1 m CuL wire, 0,7 dia, 9 ceramic disc caps, 11 block caps, 1 tant. cap, 1 preset pot, 19 resistors	6171	DM 47.—
Kit	**YU3UMV 022 complete with above parts**	**6172**	**DM 70.—**
YU3UMV 023	**PLL demodulator with adjustable threshold**		**Ed. 1/1987**
PCB	YU3UMV 023 drilled, with layout plan	6173	DM 27.—
Components	YU3UMV 023 8 transistors, 2 ICs, 1 LED, 1 RFC, 2 ceramic disc caps, 4 block caps., 3 tant. caps, 1 preset, 22 resistors	6174	DM 54.—
Kit	**YU3UMV 023 complete, with above parts**	**6175**	**DM 78.—**
YU3UMV 024	**AM Video Modulator (VHF output)**		**Ed. 1/1987**
PCB	YU3UMV 024 drilled, with layout plan	6176	DM 25.—
Components	YU3UMV 024 3 transistors, 1 IC, 1 RFC, 1 m CuL 0.15 mm dia, 1 coil kit, 4 ceramic	6177	DM 31.—

	disc caps, 3 block caps, 1 preset, 1 tant. cap, 12 resistors		
Kit	**YU3UMV 024 complete with above parts**	**6178**	**DM 53.—**
YU3UMV 025	**Tunable sound demodulator**		**Ed. 1/1987**
PCB	YU3UMV 025 drilled, with layout plan	6179	DM 27.—
Components	YU3UMV 025 1 IC, 4 varicaps, 1 RFC, 3 coil kits, 3 m CuL 0.1 mm dia, 3 elkos and 1 tant. cap, 2 ceramic disc caps, 12 block caps, 11 resistors	6180	DM 61.—
Kit	**YU3UMV 025 complete with above parts**	**6181**	**DM 83.—**
YU3UMV 026	**Stabilized DC converter**		**Ed. 1/1987**
PCB	YU3UMV 026 drilled, with layout plan	6182	DM 25.—
Components	YU3UMV 026 3 transistors, 1 Z diode, 2 switching diodes, 2 RFCs, 5 tant. caps, 1 ceramic disc cap, 1 preset, 7 resistors	6183	DM 26.—
Kit	**YU3UMV 026 complete with all above parts**	**6184**	**DM 48.—**
YU3UMV 020 ... 026	**Indoor unit**	**6185**	**DM 425.—**
DK1OF	**Digital Frequency Tuning of PLL Oscillators with Delay Lines**	**Art.No**	**Ed. 1/1987**
PCB	DK1OF 050 through-contacted Euro format	6980	DM 48.—

In-Channel-Select

ICS The FM Power Receiver

Reception improvements through the employment of a super fast electronic tracking ICS filter.

- ★ 6 dB sensitivity improvement
- ★ 20 dB improvement in selectivity
- ★ Automatic or manual bandwidth control
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- ★ Socket on front panel for remote control
- ★ Connection cable to station receiver supplied
- ★ Robust, black lacquer, aluminium housing

Technical Data	ICS
Supply voltage	10 – 16 V from station RX / TR
Supply consumption	100 mA (approx.) at 12 V
IF input impedance	30 kΩ / 10 pF
Bandwidth of ICS filter	1.8 kHz (approx.)
Sensitivity improvement	up to 6 dB
Adjacent channel interference reduction	up to 20 dB
Dimensions (mm)	180 × 90 × 32
Weight	600 g (approx.)
Art.-Nr. 3216	Complete: **Price: DM 495,—**

New · New · New · Now available ex stock

Interface „slave 10“

for the satellite rotator systems
KR 5400 and KR 5600

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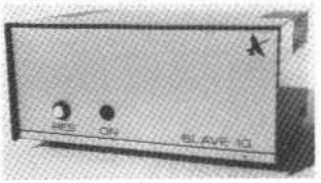
(incl. connection cable)



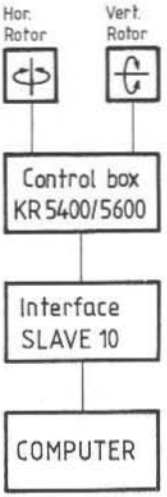
- **fully-automatic antenna tracking system for satellite communications**
- **connection to any computer possible via RS 232**
- **resolution of the dual-channel A / D converter amounts to 10 bits**
- **OSCAR 10 software for the C 64 available**
- **connection to existing rotator systems possible**

Table of commands:

command	response	function
R CR	R CR	rotation clockwise
L CR	L CR	rotation counter clockwise
U CR	U CR	rotation up
D CR	D CR	rotation down
S CR	S CR	all rotators stop
V CR	V CR	rotator stop vert.
H CR	H CR	rotator stop horiz.
G xxxxyyyy CR	G CR	preset position
F CR	F xxxxyyyy CR	interrogation position

xxxx: Vertical position (4 digits)
yyyy: Horizontal position (4 digits)
CR: CARRIAGE RETURN

System's block diagram



Technical data:

Data exchange:	3-wire asynchron. full duplex input and output negative or positive
Data format:	1 start bit 8 data bits 2 stop bits
Baud rate:	1200 B / s
Power supply:	14 V unstab. via control box KR 5400 or KR 5600
Dimensions:	w x h x d = 160 x 80 x 130 mm

Special accessories:

Software on diskette for C 64	Art. nr. 1100	DM 48.—

Satellite rotator systems:

KR 5400	Art. nr. 1013	DM 809.—
KR 5600	Art. nr. 1014	DM 1070.—

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- higher stability than a quartz crystal: less than ± 3 ppm over the temperature range –30 to +60°C. (types B)
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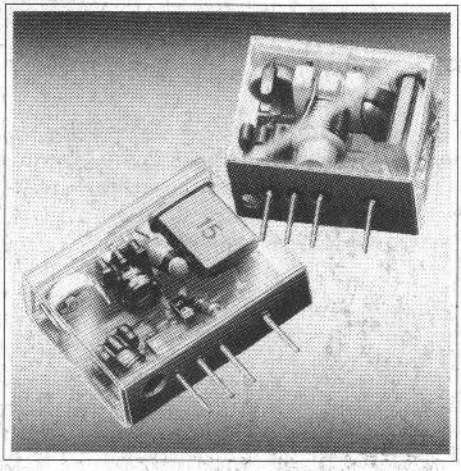
- small outlines: CCO 104 = 2,6 cm³, CCO 102/152 = 3,3 cm³, CCO 103 = 4,0 cm³
- widespread applications e.g. as channel elements or reference oscillators in UHF radios (450 and 900 MHz range)



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Quartz crystal units in the frequency range from 800 kHz to 360 MHz Microprocessor oscillators (TCXO's, VCXO's, OCXO's) crystal components according to customer's specifications

Types	CCO 102			CCO 103			CCO 104		
	A	B	F	A	B	F	A	B	F
Freq. range	10 - 80 MHz			6.4 - 25 MHz			10 - 80 MHz		
stability vs temp. range	–30 to +60°C			–30 to +60°C			–30 to +60°C		
Current consumption	max. 3 mA at UB = +5 V			max. 10 mA at UB = +5 V			max. 10 mA at UB = +5 V		
input signal	–10 dB/50 Ohm			TTL-compatible (Fan-out 2)			0dB/50 Ohm		

CCO 152 A + B
same size as CCO 102 A + B
modulation input:
deviation: typ. 1 kHz/V
mod. frequency: DC to 10 kHz
impedance: 20 k Ohm

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