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A Publication
for the Radio-Amateur

Especially Covering VHF,
UHF and Microwaves

VHF communications

Volume No.16 · Winter · 4/1984 · DM 6.50

EPROM...

STORES
COLOR TEST
IMAGES

VHF communications

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Volume No.16 · Winter · Edition 4/1984

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Contents

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Dieter Meendermann, DC 1 BP

COLOUR TEST-IMAGE GENERATOR FOR AMATEUR TELEVISION APPLICATIONS

The colour test-image generator to be described is used by the author as callsign generator for the ATV-repeater DBØNL in Bentheim, West Germany.The module generates a PAL-standard colour composite video signal, and can be connected to any ATV-transmitter instead of a camera. The number of components has been kept to a minimum. The digital, colour, and power supply circuits are accommodated on a standard Europaboard (100 mm x 160 mm). The image comprises 128 x 64 pixels, and each pixel can be one of eight different colours. The complete images can be stored in the described EPROM, which can then be selected as required.

The circuit diagram of the whole test-image generator is given in **Figure 1**.

1. DIGITAL CIRCUITS

1.1. Clock equipped with the ZNA 234 E.

The integrated circuit ZNA 234 E is manufactured by Ferranti, and contains allrequired dividers and logic stages in order to derive all signals necessary to generate TV-images from a crystal-controlled frequency of 2.5 MHz. The circuit of this integrated circuit is given in **Figure 2**.

The crystal Q 101 is equipped with a pulling capacitor C 108, which is connected between pin 8 and pin 9. It is possible to select the operating mode with the aid of pin 2: +5 V at pin 2 select CCIR-standard with 625 lines, 0 V at pin 2, on the other hand, select EIA-standard with 525 lines. In our application, pin 2 is connected to +5 V.

The whole synchronizing signal is present at pin 3. An oscilloscope can be connected here for checking and alignment. The whole blanking signal is present at pin 4, and the blanking and synchronizing signal are as shown in **Figure 3**. The other outputs are not required for our application and remain unconnected.

1.2. Pixel Oscillator and Pixel Counter

The resolution of the image amounts to 128 pixels in the horizontal direction. In order to be able to address all pixels, one will require a 7-bit counter. This is realized using two synchronous four-bit binary counters type 74LS161 with setting inputs and clock-independent reset inputs. **Figure 4** shows the pin connections of this type of IC.

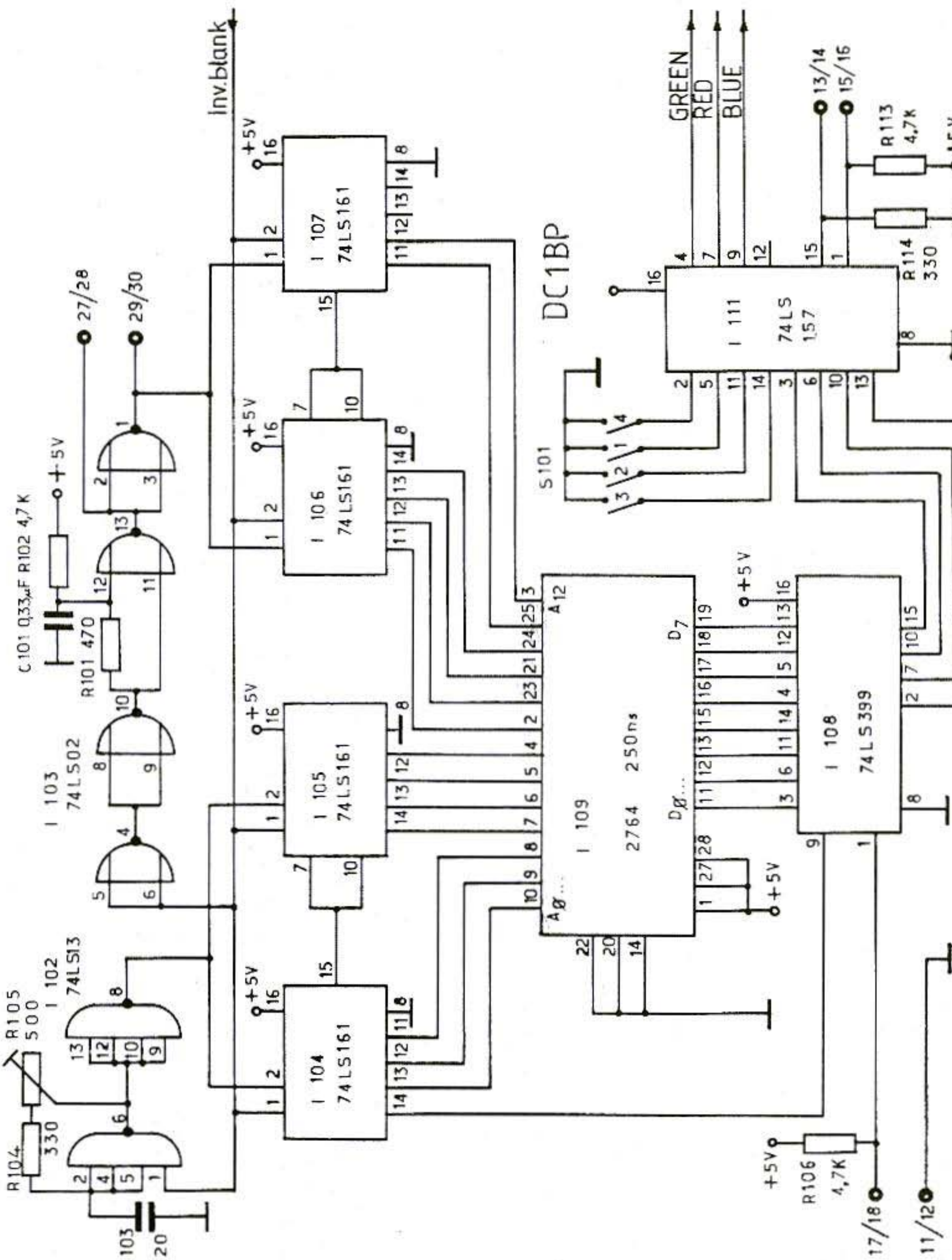

Fig. 1a: Colour test-image generator equipped with a 64 kBit EPROM

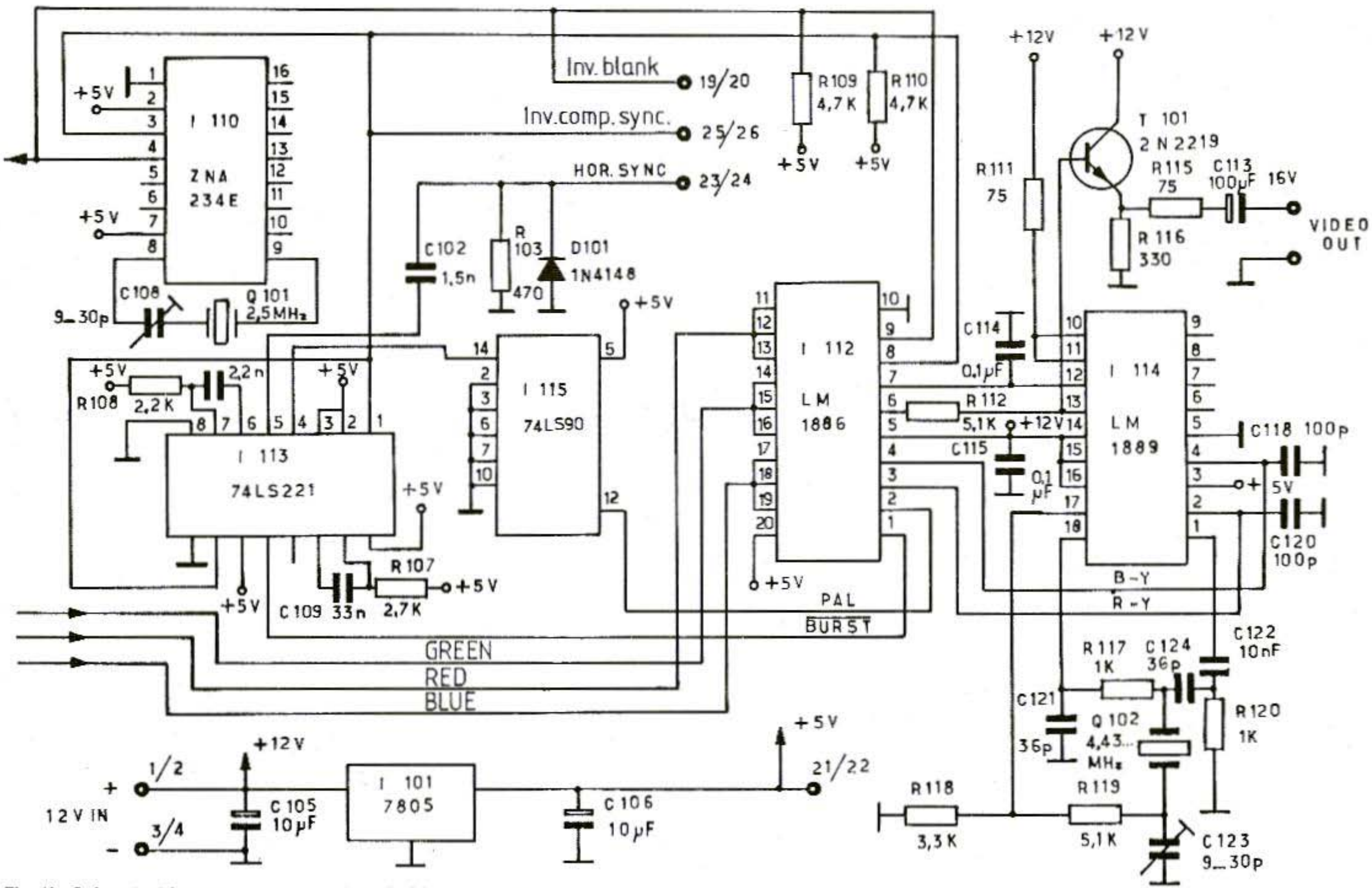

Fig. 1b: Colour test-image generator equipped with a 64 kBit EPROM

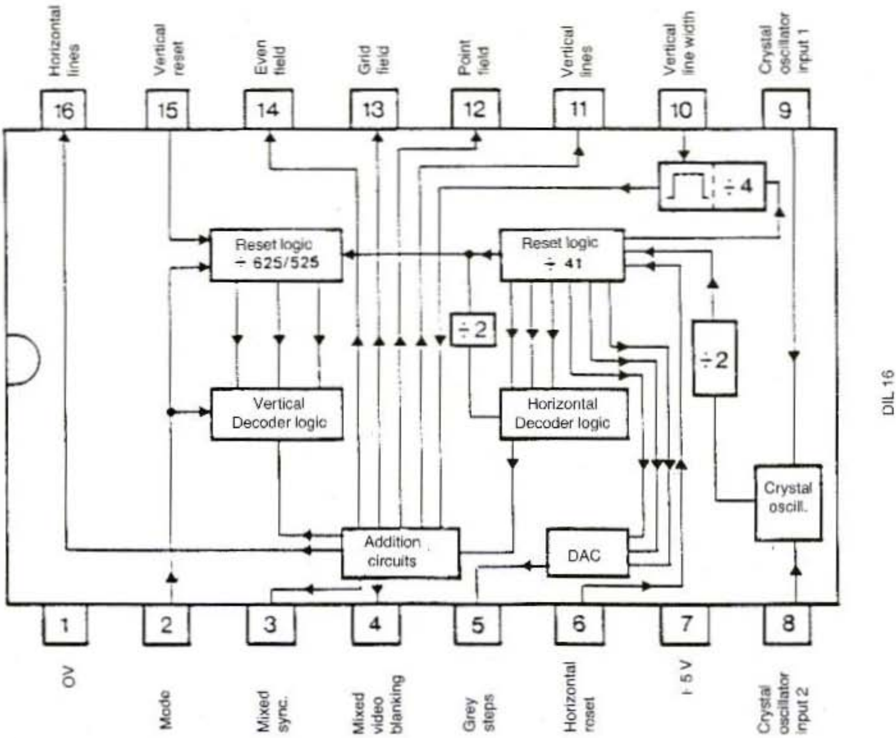

Fig. 2: Block diagram of the ZNA 234 E

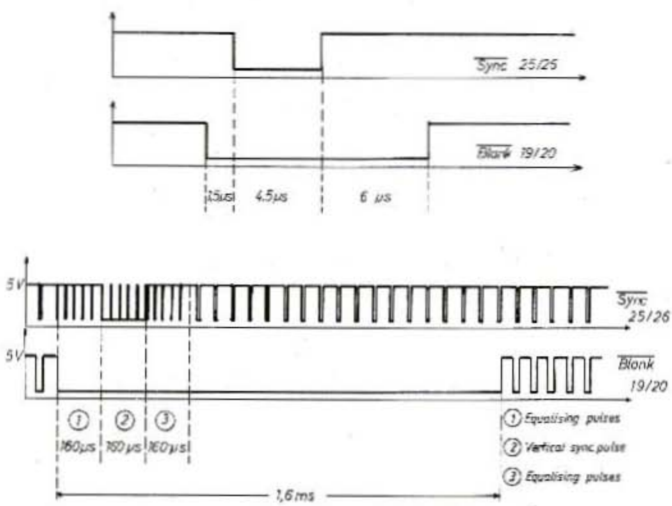

Fig. 3: Diagram of the composite blanking and synchronizing pulses

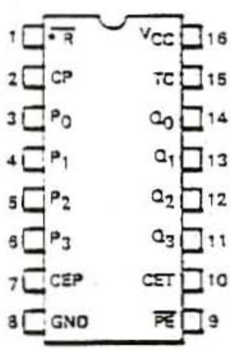

Fig. 4: SN 74LS161 N

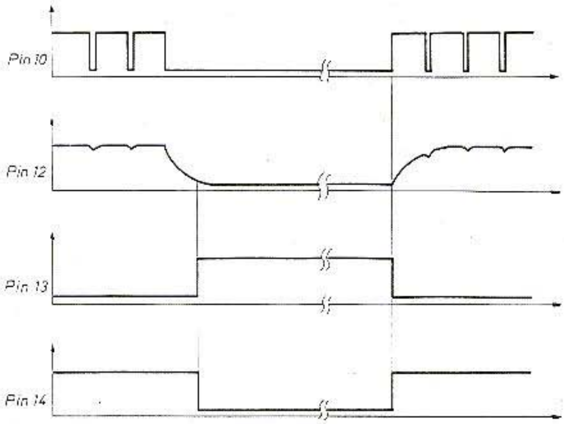

Fig. 5: Generation of the vertical reset pulse

The setting and data inputs are not used here. The control of the subsequent stage is made via the interconnection'transfer' (pin 15/I 104) to 'release' (pin 7 and 10 of I 105).

The counter chain is driven from a free-running start-stoposcillator (I 102). The oscillator is blocked by the blanking signal via pin 1. At the same time, the pixel counter is set to "0". At the commencement of each line, the oscillator and counter are released. At the end of the line, the blanking signal will reset the counter to "0".

The pixel frequency can be set to exactly 4.9 MHz with the aid of R 105. This can be checked at pin 8 of I 102 (74L13). If the frequency is too high, the image will be written several times; if it is too low, only part of the image will be visible. A measurement using a frequency counter is not possible, since the oscillator is blocked during the blanking pulses. The adjustment is therefore made according to the image on the monitor.

1.3. Line Counter

The line counter is only 6 bits in length. In order to obtain a vertical resolution of 64 lines, it is necessary to previously divide the line frequeny of 15 625 kHz by four. Line counter and prescaler are identical to the pixel counter. The two counters are reset at the lower edge of the image with the aid of the vertical reset pulse fed to pin 1.

1.3.1. Vertical Reset Pulse

The vertical reset pulse for the line counter is derived from the overall blanking signal. The 12 μs line blanking pulse and the 1.4 ms vertical blanking pulse are present at point 10 of I 103. The low-pass filter comprising R 101 and C 101 only allow the vertical blanking pulses to pass (see **Figure 5**).

The following NOR-gate generates an exactly defined position for the rear slope of the vertical blanking pulse. This releases the line counter. The vertical blanking signal is available directly (pin 27/28), as well as inverted (pin 29/30) on the 31-pin connector, and can be used for external synchronizing.

1.4. E-PROM

The author has selected an EPROM type 2764 (250 ns) for this application. Line counter and pixel counter are connected to the address inputs.

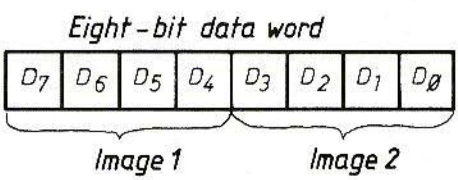

Fig. 6: 8-bit data word

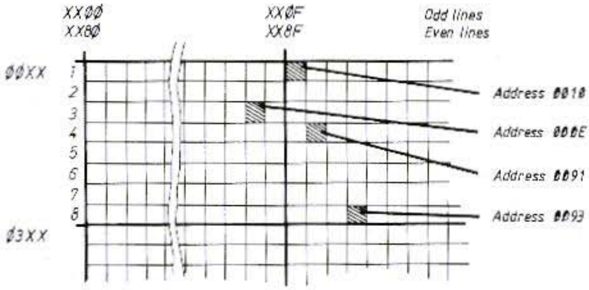

Fig. 7:
Part of a grid for designing the colour TV-image

The resolution of 128 pixels x 64 lines results in 8192 pixels. A data word of 8 bit is available for each pixel. Only 4 bit are required for the colour display. It is possible with the aid of the multiplexer (I 108) for the second 4 bit to be switched to a second TV-image. This is shown in more detail in **Figure 6**.

The colours of the pixels result from the four-bit value as shown in **Table 1**.

Binary	Hex	Colour
Ø Ø Ø 1	–1–	black
Ø Ø 1 1	–3–	blue
Ø 1 Ø 1	–5–	red
Ø 1 1 1	–7–	magenta
1 Ø Ø 1	–9–	green
1 Ø 1 1	–B–	cyan
1 1 Ø 1	–D–	yellow
1 1 1 1	–F–	white

Table 1

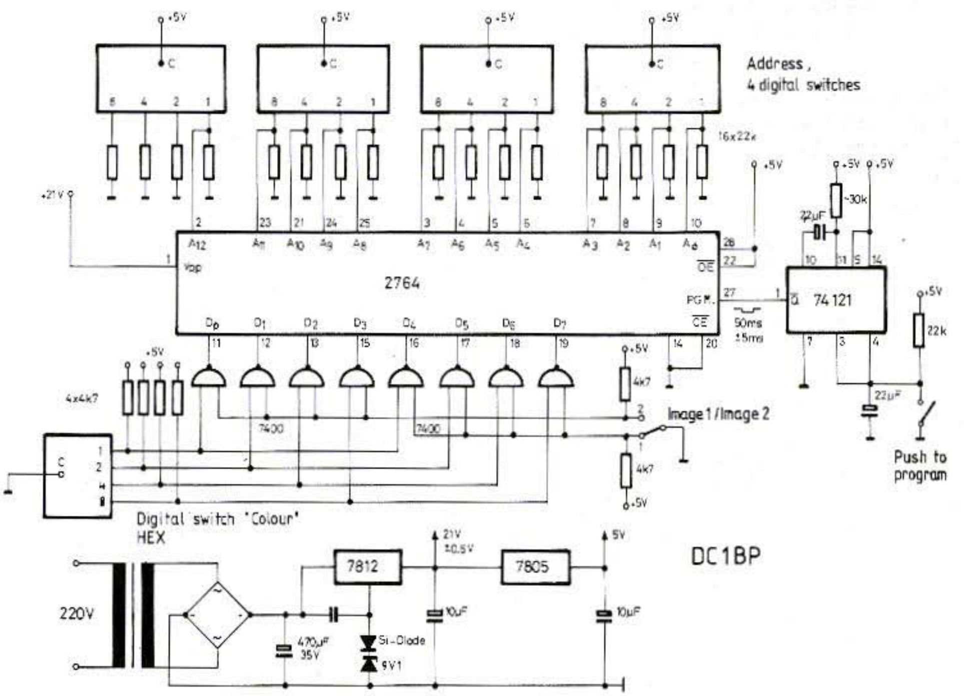

Fig. 8: Simple programming system for EPROMs

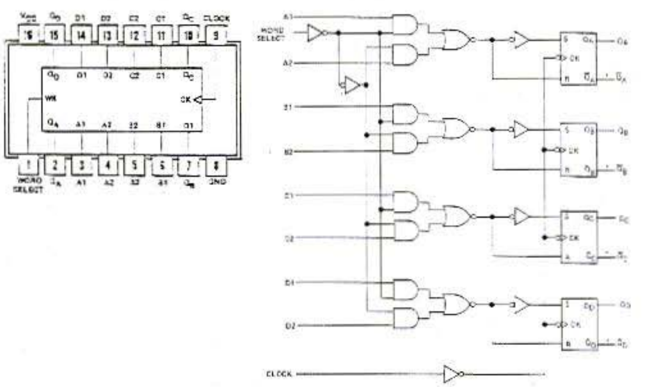

Fig. 9: Image multiplexer

The procedure from the design of the required TV-image up to the finished EPROM is carried out as follows:

The TV-image design is made on, for instance, graph paper (see **Figure 7**). Each square corresponds to one memory address in the EPROM and can be associated with one of the eight possible colours.

There are some limitations: Lines 65 to 72 cannot be freely programmed, but possess the same colours as lines 1 to 8. The memory address of each pixel can be read off on the left and upper edges of the paper.

The programming of the EPROM is very simple if one has access to a computer system (possibly even to a personal computer). Otherwise, it is possible for the EPROM to be programmed using the simple programming circuit for EPROMs shown in **Figure 8**.

It is possible to operate the test-image generator even without EPROM if the following three bridges are made at the socket:

Pin 4 – pin 19, pin 5 – pin 18, pin 6 – pin 17. In this case, one will obtain a colour test pattern. A test-EPROM with sufficient room for subsequently programming your call-sign will be available from the publishers.

1.5. Image Multiplexer

The integrated image multiplexer I 108 is a 74LS399. It selects one of the two 4-bit data sources. **Figure 9** shows the pin connections and a block diagram of this integrated circuit.

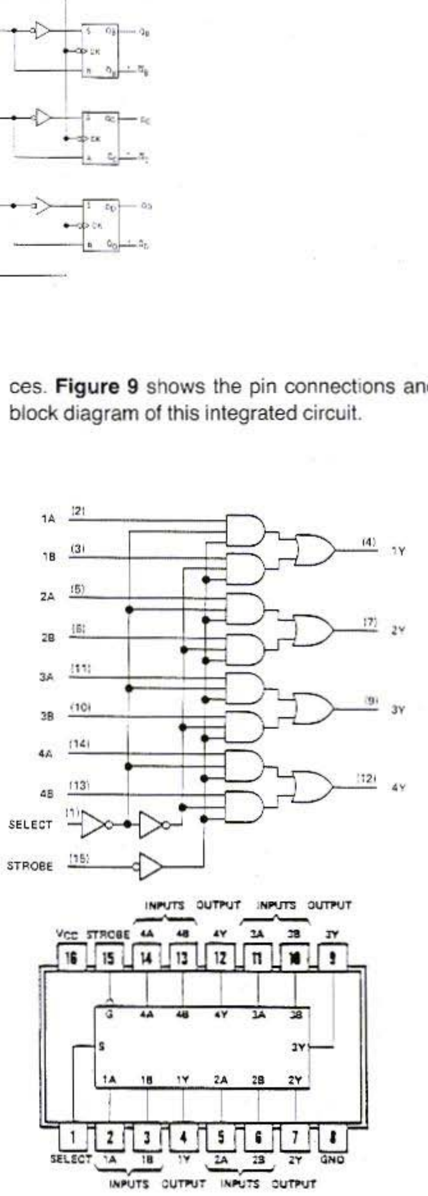

Fig. 10: Multiplexer SN 74LS157 N

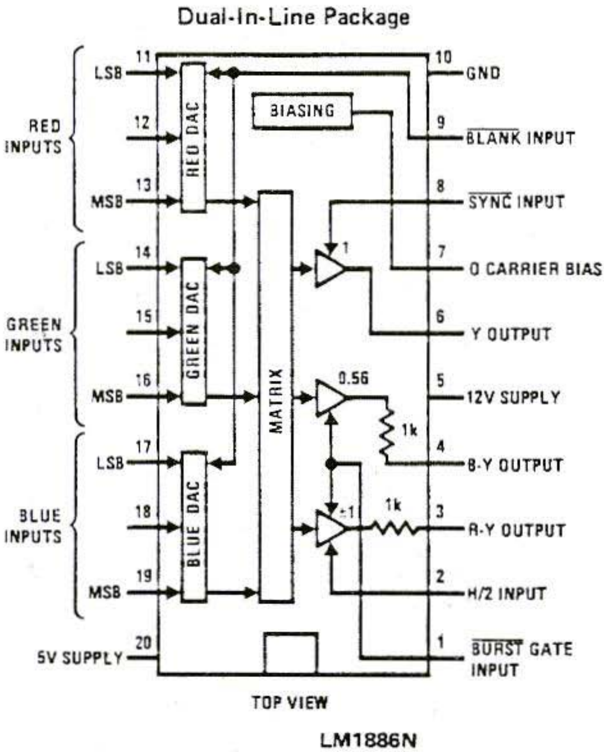

Fig. 11: LM 1886 N, a TV-video digital/analog converter

If the word-select input (pin 1) is low, word 1 (A1, B1, C1, D1) is selected, which means that image 2 will appear on the monitor. Otherwise, word 2 will be selected if pin 1 is high (A2, B2, C2, D2), and image 1 will appear.

The SN74LS399 has one intermediate storage available for each of the four output lines (Q_A, Q_B, Q_C, Q_D). The intermediate storage is necessary since the EPROM itself would have too large tolerances in the readout speed of the individual bits. These tolerances would cause colour edges to the contours.

I 111 (74LS157) is also a multiplexer (see **Figure 10**). It is possible with the aid of pin 1 to switch between the TV-images and a coloured surface. The colour of the surface can be selected with the aid of switch S 101.

A low level at the select input obtains a coloured surface, and high TV-images. The multiplexer can be blocked via the strobe input (pin 15). A high level at the strobe input will cause a black image.

The two non-connected inputs that can be seen in Figure 1 are provided for later applications, such as for injecting moving text into the TV-image.

2. COLOUR CIRCUIT

The LM1886 (I 112) is a digital/analog converter designed for TV-video application. The block diagram and the pin connections of that circuit are shown in **Figure 11**. This circuit generates coded

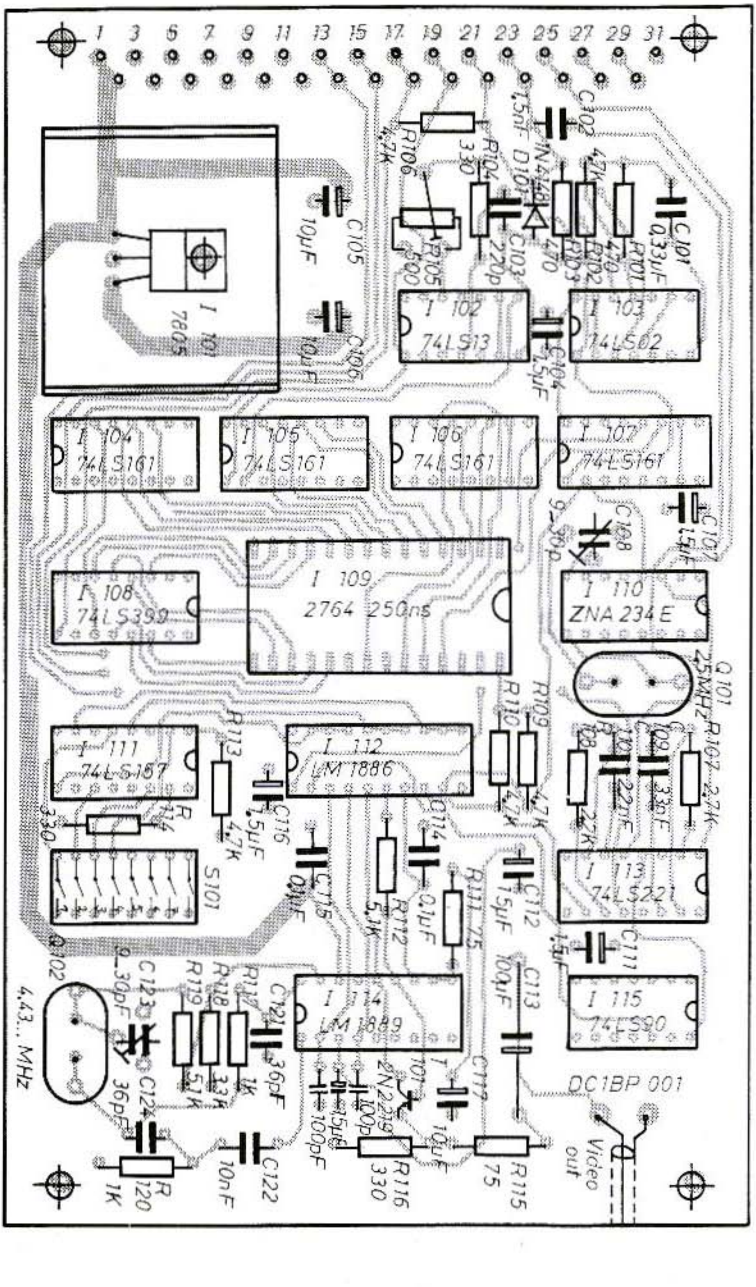

Fig. 12: Through-contacted PC-board DC 1 BP 001 for the colour test-image generator

saturation and colour difference signals from 3-bit red, green, and blue input signals. The polarity of the R-Y signal is switched at the end of each line via input pin 2. A low signal at pin 1 will activate the burst. The output signal corresponds to the PAL-colour TV standard.

Only the quadrature chroma modulator and the chroma oscillator are used in the LM1889 (I 114). The complete colour composite video signal is available at pin 13. T 101 is provided as impedance converter.

3. CONSTRUCTION

The circuit of the colour test-image generator shown in Figure 1 can be accommodated on the double-coated PC-board with through-contacts shown in **Figure 12**. This Europaboard is designated DC1BP 001. The 31-pin DIN connector strip has the following connections:

1 + 2:	+12 V operating voltage
3 + 4:	−12 V operating voltage (ground)
5 + 6:	no connection
7 + 8:	no connection
9 + 10:	no connection
11 + 12:	Ground
13 + 14:	Strobe input (high = black image)
15 + 16:	Colour surface (low = colour selected at S 101)
17 + 18:	TV-image switching (high = image 1, low = image 2)
19 + 20:	Blanking output, inv.
21 + 22:	+5 V output
23 + 24:	Hor. sync. output
25 + 26:	Comp. sync. output, inv.
27 + 28:	Vert. sync. output
29 + 30:	Vert. sync. output, inv.
31:	no connection

Table 2: Pin connections of DC1BP 001

3.1. Component Information

D 101:	Diode 1N 4148, 1N 4151 or similar
T 101:	Transistor 2N 2219 or similar
Q 101:	Crystal 2.5 MHz; HC 18/U or HC 33/U
Q 102:	Crystal 4.43361 MHz; HC 18/U or HC 33/U
S 101:	8-pos. DIL switch
ST 101:	31-pin connector strip DIN 41 617
I 101:	Voltage stabilizer 5 V/1 A, type 7805
I 102:	74LS13
I 103:	74LS02
I 104 – 107:	74LS161
I 108:	74LS399
I 109:	EPROM 2764, 250 ns, with socket
I 110:	ZNA234E, Ferranti
I 111:	74LS157
I 112:	LM1886, National
I 113:	74LS221
I 114:	LM 1889, National
I 115:	74LS90

The resistors are conventional composite carbon resistors, for a spacing of 12.5 mm. The spacings for the 500 Ω trimmer potentiometer are 5/10 mm.

Plastic foil capacitors:

C 101:	0.33 μF, spacing 7.5 mm
C 102:	1.5 nF, spacing 5 mm
C 109:	33 nF, spacing 7.5 mm
C 110:	2.2 nF, spacing 7.5 mm
C 114, C 115:	0.1 μF, spacing 7.5 mm
C 122:	10 nF, spacing 7.5 mm
C 108, C 123:	Plastic foil trimmer 30 pF, Valvo: red

Ceramic disk capacitors:

C 103:	220 pF, spacing 5 mm
C 118, C 120:	100 pF, spacing 5 mm
C 121, C 124:	33 pF, spacing 5 mm

Electrolytic capacitors:

C 104, C 107, C 111, C 112, C 116, C 119:
1.5 μF tantalum, spacing 5 mm
C 105, C 106, C 117:
10 μF tantalum, spacing 5 mm
C 113: 100 μF/25 V aluminium, spacing 20 mm

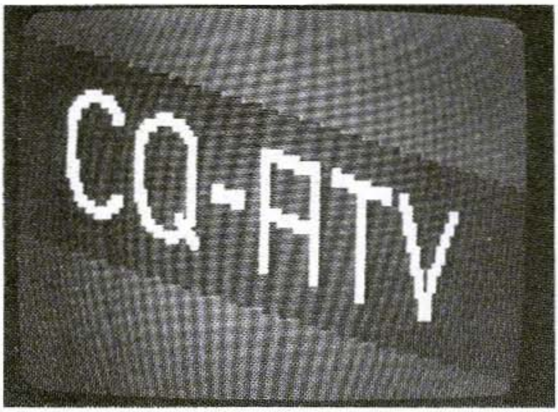

Fig. 13: Image 1

Fig. 14: Image 2

3.2. Examples

Figures 13 and 14 show two examples of colour TV-images, unfortunately only in black and white. The CQ-image comprises yellow letters on a blue background, with red colour surfaces above and below.

The call-sign image gives the call-sign in white letters on a blue background, with various video frequencies below for determining the resolution in black on white, as well as an eight-step colour scale with white on the left and black on the right.

As you can image, there is quite a lot of work involved in programming all 128 x 64 = 8192 individual pixels, and to load these into the EPROM! For this reason, we would like to mention that the publishers offer the possibility of obtaining a programmed EPROM from them. It is programmed as follows:

Image 1: CQ-image with yellow letters on blue background.

Image 2: eight-step colour scale with a white horizontal bar for subsequently adding a call-sign; under the call-sign, the black and white bars are provided for determining the resolution.

Harald Braubach, DL 1 GBH

Directional Couplers – Made to Measure

It was always difficult for radio amateurs to construct wideband directional couplers having a low coupling attenuation. Microstrip couplers are easy to manufacture for those that have such capabilities. However, the minimum coupling attenuation that can be obtained with a reasonable directional characteristic is in the order of 10 dB. On the other hand, it is virtually impossible, using microstrip technology, to design 3 dB power dividers, such as are required when constructing push-pull mixers, or for feeding circular-polarized antennas. It is possible, of course, when using triplate circuits for these values to be achieved, however, the conductor lanes are then so thin that it is hardly possible to use them in conjunction with higher power levels. Most radio amateurs do not have the necessary machines to construct conventional directional couplers mechanically, and do not have enough room for accommodating such large couplers.

A good solution for solving the problem of home-made directional couplers is offered by a product manufactured by Sage Laboratories Inc.: "Wireline" and "Wirepac". It is possible using both these systems to construct directional couplers in the range of 3 to 20 dB coupling attenuation in a frequency range from 50 MHz to 2.4 GHz. Wireline is the cheaper of the two and has a directivity of 20 dB. Wirepac has a directivity of 30 dB, but is considerably more expensive, and is therefore not to be discussed here.

1. FUNDAMENTALS

The Wireline type to be described is a line directional coupler and comprises two coupled lines as shown in **Figure 1**. The coupling attenuation is dependent on frequency and achieves its minimum value at a coupling length of $\lambda/4$ (see **Figure 2**).

Under matched conditions (**Figure 3**), the following is valid:

If a signal with a power P_1 is fed to the input, a power of $P_2 = P_1 - P_1 \times c$ will be present at R_2, and a power of $P_3 = P_1 \times c$ at R_3; where c = coupling factor.

In the case of an ideal directional coupler, R_4 will be powerless, since the diagonally opposite inputs are decoupled from another. In practice, a power will be present that is reduced to the value of the directivity d.

$P_4 = P_1 \times c \times d$ (d = directivity)

accordingly

$P_3 = P_1 \times c - P_1 \times c \times d$

A further characteristic of directional couplers is that the signals of the coupled outputs will have a frequency-independent phase difference of 90°.

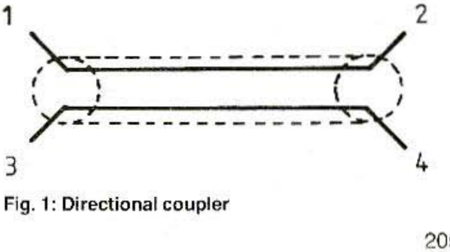

Fig. 1: Directional coupler

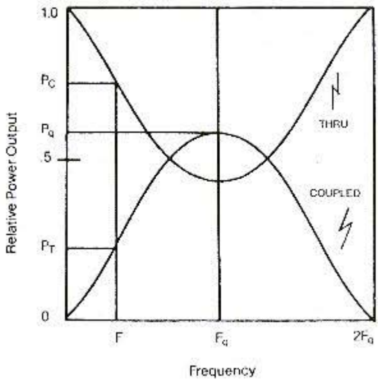

Fig. 2: Coupling attenuation and insertion loss as a function of frequency

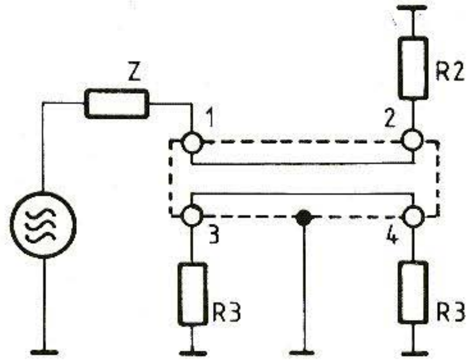

Fig. 3: Matched directional coupler

2. CONSTRUCTION OF WIRELINE

There are five different versions which differ in the type of screening and the maximum power ratings. The internal construction is shown in **Figure 4**. The following **Table 1** shows the most important differences between the individual types.

Due to the coaxial type construction of the coupler, it is possible for the two coupled outputs to be provided on one side as shown in **Figure 5**. This offers several advantages for practical construction.

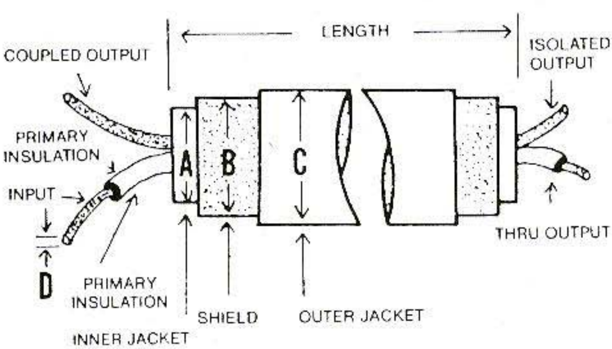

Fig. 4: Construction of Wireline

Typ	H	HB	HC	JB	JC
Schirm	Doublefoil screen	Copper mesh	Copper tube	Copper mesh	Copper tube
P_m/W	100	100	100	200	200
P_s/W	2000	2000	2000	2000	2000

Table 1: Wireline designs
P_m = mean power
P_p = peak value of the power rating

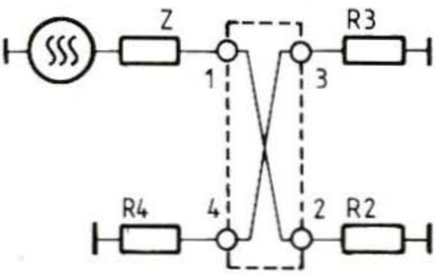

Fig. 5: Coupler showing the coupled outputs on one side

3. CALCULATION OF THE COUPLERS

3.1. Calculation of a Coupler with a certain Coupling Attenuation at a certain Operating Frequency

The following data is required for the calculation:
- Required center frequency f_{op} (e.g. 435 MHz)
- Required coupling attenuation a_c (e.g. 10 dB).

It is firstly necessary to convert the logarithmic value of the coupling attenuation a_c into the linear coupling factor c.

$$c = 10^{-a_c/10} \quad (1)$$

In the case of a 10 dB-coupler, the following results:

$$c_{10dB} = 10^{-10/10} = 10^{-1} = 0{,}1$$

This is followed by calculating the frequency at which a 3 dB coupling is achieved from the operating frequency f_{op} and the coupling factor of the frequency f_c.

$$f_c = \frac{90\ f_{op}}{\arc\sin\sqrt{-\left(\frac{c}{c-1}\right)}} \qquad (2)$$

The following will result at the values of f_{op} = 435 MHz and c = 0.1:

$$f_{c(10\ dB/435)} = \frac{90 \cdot 435\ \text{MHz}}{\arc\sin\sqrt{-\left(\frac{0.1}{0.1-1}\right)}} = 2010.66\ \text{MHz}$$

From this quarterwave frequency (f_c) one then calculates the length l of the coupler as follows:

$$l = \frac{4700\ \text{MHz} \cdot \text{cm}}{f_c\ (\text{MHz})} \qquad (3)$$

This results in the following coupler length in our example:

$$l_{(10\ dB/435)} = \frac{4700\ \text{cm}}{2010{,}66} = 2{,}338\ \text{cm}$$

A 10 dB coupler at 435 MHz would therefore have a length of 23.38 mm.

3.2. Calculation of the Coupling Attenuation of any required Coupler

The following data is required for calculation:
- Length (1) of the coupler in cm (e.g. 10 cm)
- Frequency (f) at which the coupling attenuation is to be calculated (e.g. 435 MHz)

Firstly find the quarterwave frequency (f_c) of the coupler:

$$f_c = \frac{4700\ \text{MHz} \cdot \text{cm}}{l\ (\text{cm})} \qquad (4)$$

In our example:

$$f_{c\ (10\ cm)} = \frac{4700\ \text{MHz}}{10} = 470\ \text{MHz}$$

This is followed by calculating the coupling factor (c):

$$c = \frac{\sin^2\left(90\frac{f}{f_c}\right)}{\sin^2\left(90\frac{f}{f_c}\right) + 1} \qquad (5)$$

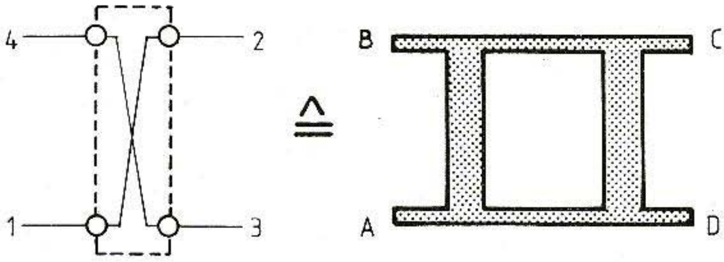

Fig. 6: Comparison between a Wireline coupler and a 4/4 λ hybrid

In our example:

$$c_{(10\text{ cm }435)} = \frac{\sin^2\left(90\,\frac{435}{470}\right)}{\sin^2\left(90\,\frac{435}{470}\right)+1} = 0.4966$$

The coupling attenuation (a_c) is now calculated from the coupling factor:

$$a_c = -10 \log c \quad (6)$$

The following will result in our example:

$$a_{c(10cm435)} = -10 \log 0.4966 = -3.04\text{ dB}$$

4. PRACTICAL APPLICATIONS OF WIRELINE

4.1. Use as a Directional Coupler

Of course, the primary use of Wireline couplers is for determining the VSWR of antennas and other consumers. The construction of VSWR bridges is not to be discussed, since it is well known. **Table 2**, however, provides an aid for designing a directional coupler for frequencies up to 435 MHz.

Table 2: Directional coupler, length l = 50 mm, coupling attenuation as a function of frequency:

$f/_{MHz}$	$a_{c/dB}$
3.5	44.66
7.0	38.64
14.0	32.62
21.0	29.10
28.0	26.61
145.0	12.64
435.0	5.13

4.2. Use as a 3 dB Coupler

This results in a multitude of applications of which the most important are to be mentioned.

4.2.1. Feeding of Circular-Polarized Antennas

Since the coupled outputs always possess a phase shift of 90° (± 1°) to another, it is easily possible to construct a low-loss, wideband feed for circular-polarized antennas (see **Figure 7**).

Directional couplers as shown in Figure 5 have a behaviour as a 4/4 λ hybrid (see **Figure 6**). A RF-voltage fed to 1, or A, will be distributed equally to 2 and 3, or C and D. Connection 4, or B, remains decoupled. A RF-voltage fed to 4, or B, will be distributed equally to 2 and 3, or C and D. In this case, 1, or A will remain decoupled.

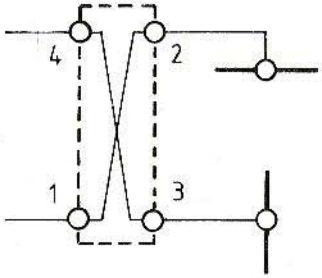

Fig. 7: Directional coupler for feeding circular-polarized antennas

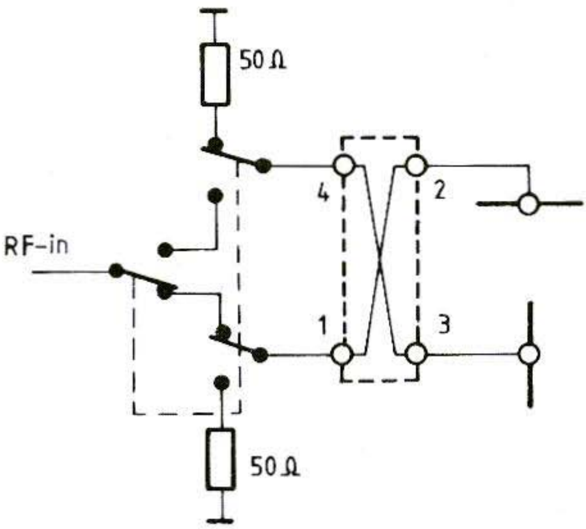

Fig. 8:
Circuit for switching the polarization of circular antennas

Connection 2 and 3, or C and D, have a phase shift of 90° to another (this will only be the case at the center frequency of a 4/4 λ hybrid).

If, for instance, an RF-signal is fed to 1, and 4 is terminated with 50 Ω, anticlockwise, circular polarization will result. If, on the other hand, 4 is fed with the RF-voltage, and 1 is terminated with 50 Ω, clockwise, circular polarization will result. Of course, the actual polarization will also be determined by the phase position of the individual antenna. An anticlockwise circular polarization will be changed to clockwise polarization on rotating the phase position of one of the antennas by 180°.

As can be seen, the polarization switching is nowhere near as critical as when using conventional coaxial delay line methods, and where the switching relay must be taken into consideration in the phase-shift calculation. In the case of the described type of feeding, the relay is placed in front of the phase-shift 3 dB coupler (**Figure 8**). Attention must only be paid that the lengths of the antenna feeders are identical. The terminating resistors should have a rating of one 100th of the transmit power if the antenna matching is good.

4.2.2. Construction of Push-Pull Mixers

A further application of Wireline 3 dB couplers is given in the constuction of push-pull mixers (**Figure 9**). A mixer constructed in this manner will have a bandwidth of one octave (frequency ratio 1:2).

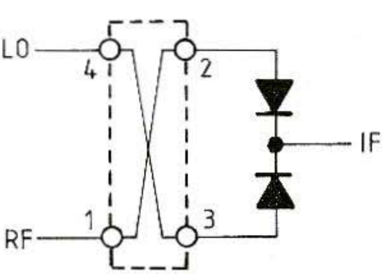

Fig. 9: Push-pull mixer with 3 dB coupler

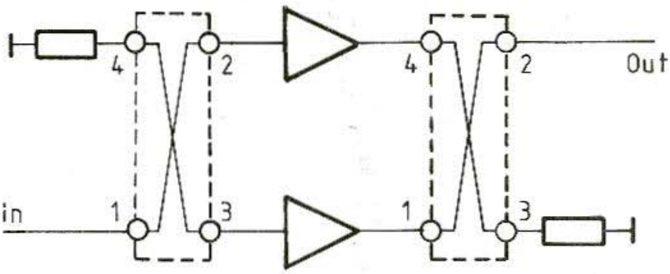

Fig. 10: Wideband amplifier with directional coupler

4.2.3. Construction of Wideband Power Amplifiers

At higher frequencies, it is difficult to connect wideband amplifiers in parallel to achieve higher power levels. In most cases, 4/4 λ hybrids are used. This means that it is possible to use Wireline 3 dB-couplers here, which also have the advantage of being much smaller (**Figure 10**).

4.3. Table of the Most Common Couplers

Table 3:
Coupling length as a function of coupling attenuation and frequency

f/MHz	3 dB	6 dB	10 dB	20 dB
3.5	too long	too long	too long	860 mm
7.0	too long	too long	too long	430 mm
14.0	too long	too long	726 mm	215 mm
21.0	too long	880 mm	484 mm	143 mm
28.0	too long	660 mm	363 mm	107.5 mm
145.0	324 mm	127.5 mm	70.1 mm	20.7 mm
435.0	108 mm	42.5 mm	23.4 mm	too short
1275.0	36.9 mm	too short	too short	too short
2350.0	20.0 mm	too short	too short	too short

5. MANUFACTURER-AVAILABILITY OF WIRELINE AND DESIGN PROGRAMS

Wireline is available from Sage Laboratories Inc. or from Wacker at the address given below.

Since the manufacturers will probably not supply the short lengths required by radio amateurs, the publishers will consider stocking a certain quantity of such Wireline if sufficient interest is shown.

Please, inform us if you would like to purchase such Wireline; the prices are given in the kit price-list.

5.1. Program

A German company has a basic program for the TRS-80 M III for the design of such couplers. We would like to suggest that interested readers contact this company directly. The address is as follows:

Firma Wacker GmbH, Grüneburgweg 85, D 6000 Frankfurt 1/West Germany.

Joachim Kestler, DK 1 OF

PLL Oscillators with Delay Lines

Part 1: Fundamentals

The problem of constructing stable VFOs is as old as amateur radio itself. In the past, one tried to stabilize oscillator circuits equipped with tubes by temperature compensation and by using solid mechanical construction; nowadays, it is mainly digital techniques that are used for frequency stabilization (DAFC, PLL-synthesizers, etc.).

As long as frequency bands are allocated to radio amateurs, and not fixed channels as with other services, there will always be the desire to tune over the band. Of course, as far as repeaters and FM-communications are concerned, certain channels have been agreed for the VHF and UHF amateur bands.

It would seem that an analog tuning system is most favorable to satisfy the desire to tune over the band. Synthesizers are only suitable if they can be switched in sufficiently small steps (max. 10 Hz for SSB/RTTY/CW applications).

An interesting solution of the problem of stable analog frequency tuning was used by the manufacturer Karl Braun in his VHF-transceiver SE-400. In this concept, a PAL-delay line was used as "frequency standard", which then allowed the drift of a varactor-tuned oscillator to be practically eliminated. Such circuits can be easily constructed and designed for virtually all frequency ranges (even for HF); the few special components that are required are available, and are not too expensive.

1. PRINCIPLE OF A PLL-OSCILLATOR EQUIPPED WITH A DELAY LINE

Figure 1 shows the block diagram of a simple PLL-synthesizer, which allows the theory of operation to be seen easily. The varactor-tuned oscillator "VCO" operates in the required output frequency range f_0. This frequency is divided by N in a variable frequency divider and compared to a crystal-controlled reference frequency f_{ref} in a phase comparator circuit. The VCO is tuned via a

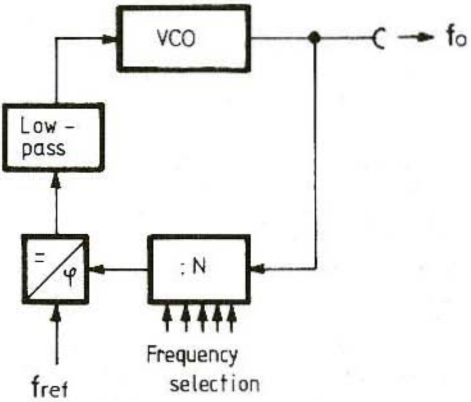

Fig. 1: PLL-synthesizer

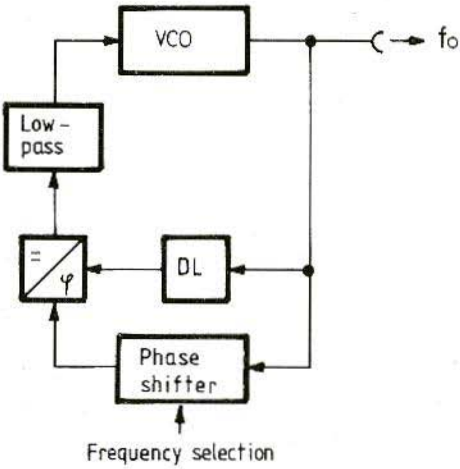

Fig. 2: PLL-oscillator equipped with a delay line

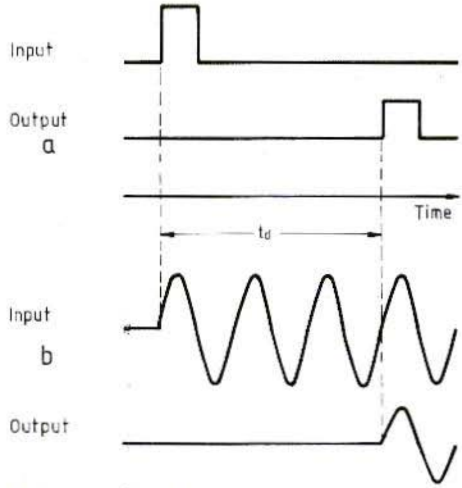

Fig. 3: Operation of the delay line as a function of time

lowpass filter, which is responsible for the stability of the control loop, until $f_0/N = f_{ref}$ is valid. The output frequency of the circuit can be calculated as $f_0 = N \times f_{ref}$.

If one wishes to make small frequency steps, it is necessary for f_{ref} to be a very low frequency, for example 10 Hz, which, on the other hand, is a disadvantage, since the control loop will require a long period to lock in after each frequency change. Secondly, short term frequency variations of the VCO, for instance due to microphonic effects, will not be cancelled. Furthermore, the division factor N will be very large when using a low f_{ref}, which, in turn, will mean that one will require an extensive number of counter components.

If one wishes to operate such a frequency synthesizer with the aid of a rotary tuning control (analog operating technique), one will require additional components such as a slotted disk with two photocell systems and a up/down counter. A further disadvantage of this type of circuit is the presence of low-frequency, steep impulses, whose harmonic spectrum can cause a number of unwanted signals in the receiver, especially when insufficient screening is provided, and lead to spurious transmissions in the case of a transmitter.

The simplest form of delay-line PLL-oscillators is given in **Figure 2**. The required output frequency f_0 is also generated using a varactor-tuned VCO; this frequency is fed firstly via the delay line "DL", and secondly via a variable phase shifter to the phase comparator. The phase shifter is firstly to be considered as a black box with two coaxial connectors for input and output that is equipped with a rotary frequency tuning knob. The phase shift between input and output signal should be selected by rotating the tuning knob. 12 o'clock = = 0°, 3 o'clock = 90°, 6 o'clock = 180°, and 9 o'clock = 270°, and this is independent of the frequency.

Some knowledge of the characteristics of the delay line is now necessary in order to understand the operation of the circuit. If a short impulse is fed to the input (see **Figure 3a**), this will appear at the output delayed to the value of the delay time t_d. This delay time has been fixed by the manufacturer of the delay line, and is very constant, in other words, independent of aging and temperature. In the case of delay lines for PAL-colour TV receivers, this amounts to one period of the line frequency, which is 64 μs. Further details regarding the construction and original application can be studied elsewhere.

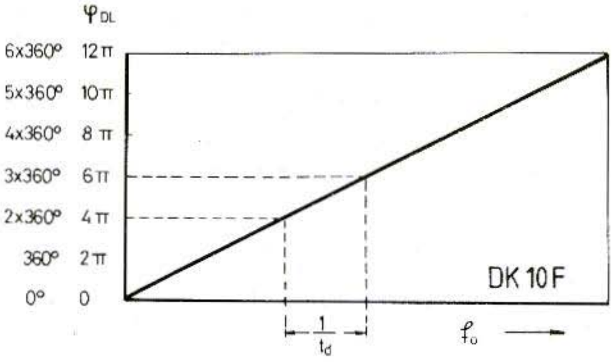

Fig. 4a

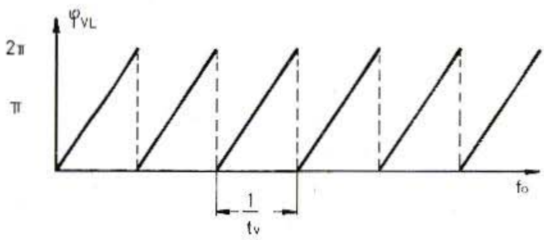

Fig. 4b

Fig. 4: Effect of the delay line as a function of frequency

If a sinewave voltage is fed to the input (see **Figure 3b**), this will be seen at the output also delayed to the value of t_d. The following equation is valid for the phase position between input and output signal:

$$\varphi DL = 360° \times t_d \times f_0 \quad (1)$$

The phase angle is therefore proportional to the frequency, (see **Figure 4a**). Physically speaking, it does not make any difference whether the two oscillations exhibit a phase difference of, for instance, 10° or 370°; one can ignore integer multiples of 360°. The phase response of the delay line can therefore be given as shown in **Figure 4b**.

The phase comparator stage tunes the VCO in the same manner as with a PLL-synthesizer so that the phase difference of the signals is zero at the input. This difference is:

$$\Delta\varphi = \varphi_{DL} - \varphi_d = 360° \times t_d \times f_0 - \varphi_d = 0 \quad (2)$$

where φ_d is the phase selected with the aid of the variable phase shifter.

The following is thus valid for the output frequency:

$$f_0 = \varphi_d/360° \times 1/t_d \quad (3)$$

This means that the tuning is linear to the knob of the phase shifter:
A complete revolution corresponds to a frequency change of 1/64 μs = 15.625 kHz.

The advantage of this concept can now be seen clearly:
A continuous tuning is possible; the only frequency involved is the required frequency itself, which means that no problems are encountered with spurious waves or interfering harmonic spectra; the lowpass filter in the control loop can be designed so that any hum or microphonic effects of the VCO can be controlled easily, and one will not require any gearing for the tuning knob.

Of course, there are some disadvantages, and these should not be ignored:
On switching on, one does not know in advance at which position of the frequency range the circuit will lock in; a total of 64 locking points are possible per MHz, which means that it is advisable to provide a frequency counter as frequency readout. For simple applications, it would be possible to use the tuning voltage of the VCO and to display this on a meter, whose scale has been calibrated in MHz. In the case of a PLL-synthesizer, the

phase comparator is used for frequency comparison. This means that any phase error caused by aging will not cause any variation of the output frequency (rapid variations will cause phase noise, in other words sidebands). In the case of a delay line PLL-oscillator, on the other hand, a phase error will have an effect on the output frequency:

$$\Delta f_n = \Delta\varphi/360° \times 1/t_d \quad (4)$$

Measurements carried out on a few experimental prototypes showed that the transcient drift at an output frequency of 5 MHz was less than 100 Hz in the first ten minutes, after which a value of 10 Hz/hour was measured on a frequency counter synchronized to the frequency standard transmission DCF77.

2. COMPONENTS OF A DELAY LINE PLL OSCILLATOR

2.1. The VCO

The quality of a signal source is mainly dependent on the characteristics of the actual oscillator circuit; in this respect, the delay line oscillator will have a similar behaviour to all PLL-circuits. It is outside the scope of this article to go into complicated fundamentals and special circuitry, however, several important points should be mentioned:

- The most important part of an oscillator circuit is the resonant circuit. The higher the Q-factor, the higher will be the short-term stability (phase noise, FM-sidebands). Attention should be paid that the Q of the circuit is not deteriorated more than necessary by the connected components (FET, varactor diode, output coupling).
- The active elements should not be driven into saturation, since they would then exhibit undefined input and output impedances, which could dampen the resonant circuit. This can be avoided using an automatic level control; furthermore, this also allows one to obtain a clean sinewave output signal.
- The signal level within the oscillator should, however, also not be too low, so that the intrinsic noise of the amplifying components remains low with respect to the required signal. Otherwise, the output signal will possess a noise floor (wideband AM). The use of lowest noise components is very advisable (even in the stages directly subsequent to the oscillator circuit).
- The tuning range of the VCO should not be much greater than absolutely necessary since the inavoidable interference AC-voltage at the tuning input (hum, noise) will generate FM noise spectra that increases on increasing the frequency range to be covered. If such a large frequency range is to be covered, it is advisable for it to be divided over several VCOs – each with a smaller tuning range – in order to solve this problem.

2.2. Delay Line

Only those of the various electrical characteristics of the delay line are to be studied here that are of interest for their use in the delay line PLL-oscillator. The phase relationships between input and output signal were already discussed in the previous section. The amplitude response as a function of frequency is very important for practical applications. A typical passband curve of a delay line is given in **Figure 5**. It will be seen that the component possesses an insertion loss of approx. 10 dB, with a minimum attenuation at approximately 4 MHz (PAL-colour subcarrier:

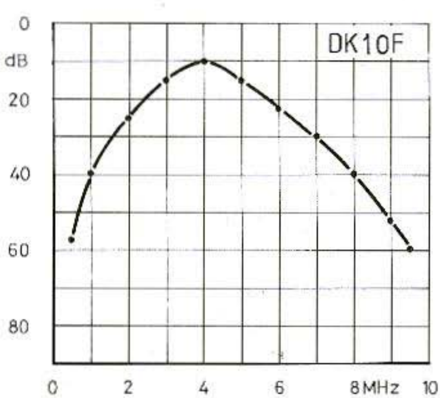

Fig. 5: Insertion loss of a delay line measured with $R_G = R_L = 50$ Ohm; $P_{in} = -13$ dBm

4.43 MHz). The overall loss is less than 30 dB in a frequency range between 2 and 7 MHz. This means that it is only this range that is of interest for the described application. For other frequency ranges, it is necessary to carry out frequency conversion and/or frequency division or multiplication. Further details regarding this are to be given later.

2.3. The Variable Phase Shifter

Such a device was used many years ago for direction-finding applications and was called "Goniometer", which is derived from the Greek word "gonos" = angle. It consisted of a pair of fixed inductances and a further pair that could be rotated through 360°. When using a suitable mechanical construction, it was possible for the phase position of the voltage induced into one pair of coils to be proportional to the angle when compared to the phase of the current fed to the other pair of coils. Such an arrangement would be of use here, but constructional problems would be difficult to solve. This means that a commercially available version would be advisable.

If one studies **Figure 6** in this respect, one will see that a RF-transformer Tr is shown. The input voltage U_{in} is fed to the primary winding of this transformer. The center tap of the secondary winding is grounded so that a voltage is present at the upper end (point **A**) that is in phase with U_{in} ($\varphi = 0°$); the voltage at the other end of the winding (point **B**) is of opposite phase to U_{in} ($\varphi = 180°$).The capacitors and resistors C and R are selected so that a voltage with a phase shift of 90° is present at point D, and one of 270° at point C (when referred to **A**). These four voltages are fed to the stator plates of a variable capacitor (without stops), and the rotor is connected to the output of the circuit. It is now possible by rotating the rotor to select any required phase angle (0° to n x 360°) between input and output voltage.

"Hot" rotors and shafts of variable capacitors are not advisable, since they carry RF-voltages. However, it is possible for the rotor of the variable capacitor to be grounded, if the center tap of the secondary winding of the transformer is used as output of the circuit. The actual operation of the module will not be changed due to this.

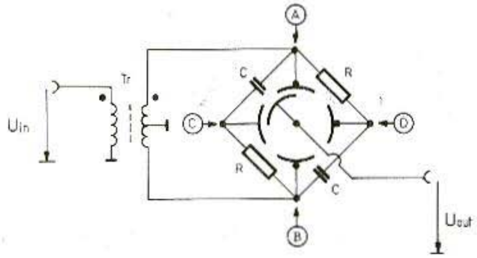

Fig. 6: Variable phase shifter using a variable capacitor

Such variable capacitors are difficult to obtain nowadays and are usually only used in transmitters. **Figure 7** shows how it is possible to replace such variable capacitors as shown in Figure 6 by varactor diodes. As can be seen, the "rotor" (intersection between D 1 and D 2, or D 3 and D 4) is grounded with respect to RF via the bypass capacitors C_A, which is the reason why the output of the circuit is connected to the tap on Tr. Both pairs of diodes D 1 and D 2, or D 3 and D 4, are provided with a common, fixed bias voltage U_b in order to ensure that the **sum** of the tuning voltages is constant for both pairs. It is possible using the control voltages U_1 and U_2 for the **voltage components** of the diode pairs to be varied in the same manner as with the variable capacitor.

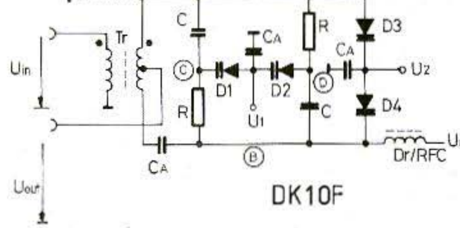

Fig. 7: Variable phase shifter using varactor diodes

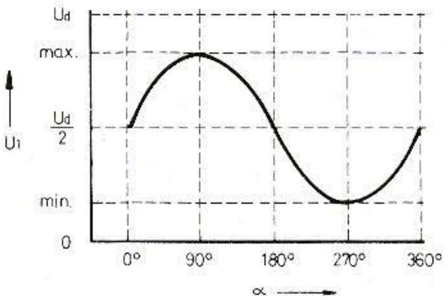

Fig. 8: Bias voltages U_1 and U_2 as a function of angle

Figure 8 shows how these control voltages must be dependent on the angle of the tuning control. One will notice the sinewave characteristic of U_1 and the cosine function of U_2. At first, this seems to be difficult to achieve, fortunately it is not. So-called sine-cosine potentiometers are available on the market, which are used to obtain analog data of rotary movements, in contrast to digital angle-coders using slotted disks and photocells. Required is a potentiometer with two taps which are shifted by 90° to another, and which does not possess stops (**Fig. 9**). The dropper resistors R_d determine the minimum or maximum values of U_1 and U_2. These values are dependent on the varactor diodes used – as is U_d.

As can be seen, it is possible to separate the phase shifter and the control easily when using varactor diodes – this would not be possible when using a variable capacitor. This means that it is possible to locate the phase shifter in a more favorable position RF-wise in the VFO and to provide optimum screening (no tuning shaft is required). The connections to the tuning potentiometer on the front panel only carry DC-voltages and are therefore uncritical.

A further advantage is also to be mentioned: It is possible to obtain the tuning voltages U_1 and U_2 from a digital-analog converter (DAC) instead of from an angle-coder. This, in turn, can be controlled by a computer so that it is possible for certain signals to be identified in programmable frequency ranges, logged, and if necessary answered, without the necessity of an operator.

Later articles in this series are to describe an interface circuit with which a preselected, nominal frequency value can be compared continuously to the actual value provided by a counter, and corrected with the aid of D/A-converters.

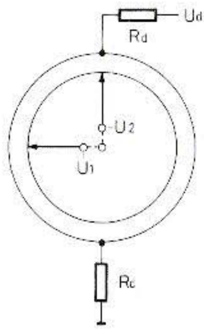

Fig. 9: Sine-cosine potentiometer

2.4. Phase Shifter and Lowpass Filter

These last two modules (see block diagram in Figure 2) are now to be discussed. In the case of a PLL-synthesizer, phase detector circuits are required that operate as frequency discriminators at large deviations between nominal and actual frequency (rapidly changing phase difference), in order to determine the direction of the tuning process (too high/too low). These circuits evaluate the time positions of the zero passes of reference and divided actual frequency (edge-triggered flip-flops). Such circuits are, in principle, sensitive to interference; especially in locked-in condition (phase difference at the input = 0), it will be found that the output magnitude (pulse train) is dependent on statistic processes, that is by chance. This problem is usually reduced by selecting the cutoff frequency of the subsequent lowpass filter to be low enough to average out the "errors" in the time plane. However, this causes the control loop to be sluggish, which means that the VCO can sometimes trip into short-term instability until this is noticed by the control circuit, and it can be slowly controlled back to the nominal frequency. The short-term instability problems (noise characteristics) of such PLL-circuits are sometimes difficult to solve.

In the case of the delay line PLL-oscillator, no such problems are to be expected. Since the frequencies of the two input signals of the phase detector are equal (since they originate from the same source, the VCO), it is possible to use "true" phase discriminators in our application, where the output signal is not dependent on the unreliable time of a switching slope. Such a circuit is, for instance, an analog multiplier, whose output signal is proportional to the input magnitude. In this case, information regarding the voltage behaviour during the whole signal period is processed. Such a system operates continuously, and it is therefore difficult for it to be interfered with by short-term fluctuations (noise).

It is the task of the phase comparator circuit to provide a DC-voltage, whose value is proportional to the phase difference of the input signals. The first input voltage originates from the phase shifter; its phase is adjustable, but is constant in the time plane, and frequency-independent. The second input is provided with a signal from the output of the delay line, whose phase response is proportional to the input frequency f_0 – as previously mentioned. What are the characteristics of the required circuit comprising delay line, phase shifter, and phase detector?

It must be some kind of frequency discriminator, since its input magnitude is a frequency (f_0) and its output signal is a DC-voltage (U_0). As can be seen in **Figure 10**, the output voltage U_0 provides a triangular function as a function of the input frequency f_0. The curve can be shifted in horizontal direction by rotating the tuning knob of the phase shifter. One complete revolution corresponds to a triangular period, thus to 1/64 µs = 15.625 kHz.

Such a circuit would also be suitable as FM-demodulator, but only for very low frequency deviation values, since the whole spectrum (2 x frequency deviation + 2 x max. AF) must be accommdated on one slope (7.8125 kHz).

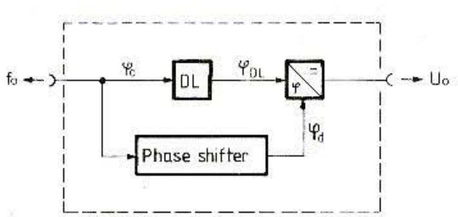

Fig. 10a

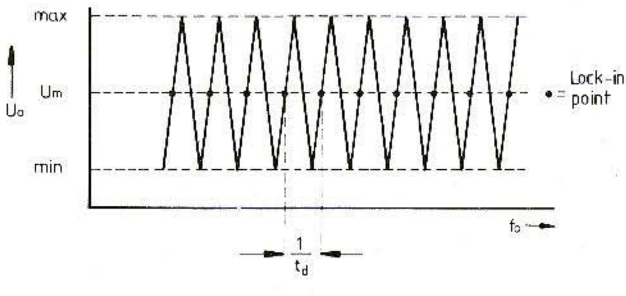

Fig. 10b

Fig. 10: Circuit comprising delay line, phase shifter, phase detector

In order to obtain an optimum design of the overall control loop, it is important to know the dynamic behaviour in addition to the static characteristics of the previously mentioned combination (Fig. 10b); in other words, the periodic variation of the output magnitude according to amplitude and phase for a given variation of the input magnitude. In order to examine this question, let us connect the input of the circuit shown in Figure 10a to the output of a frequency-modulated signal generator. The center frequency is adjusted so that an output voltage of $U_0 = U_m$ results. If the signal generator is modulated with an audio frequency (low deviation, as mentioned above!), the demodulated signal will appear as an alternating voltage at the output of the circuit.

Figure 11 shows the frequency response of the circuit according to amplitude (U_0) and phase (φ) as a function of the modulation frequency f_m, which represents the "variation speed" of the frequency f_0. As one can see, the amplitude is constant at frequencies below approximately 7 kHz, and the phase shift is less than 90°; the maximum possible bandwidth of the phase control circuit is determined by these values. At a frequency of $1/t_d$, and multiples, an attenuation pole $U_0 \rightarrow 0$ will result.

In control technology, one often uses the "jump reply" for characterizing the behaviour of a circuit comprising control, control path, or control link. This is achieved by providing a signal to the input of the circuit to be examined that jumps by a low value at time t_0 (**Figure 12**), and examining the output behaviour of the output magnitude. It will be noticed that the output signal increases linearly with time for 64 µs ($= t_d$) until the "stored" period has been passed, afterwards the relationships are constant again. The voltage variation ΔU_0 is proportional to the value of the frequency jump Δf_0 at the input.

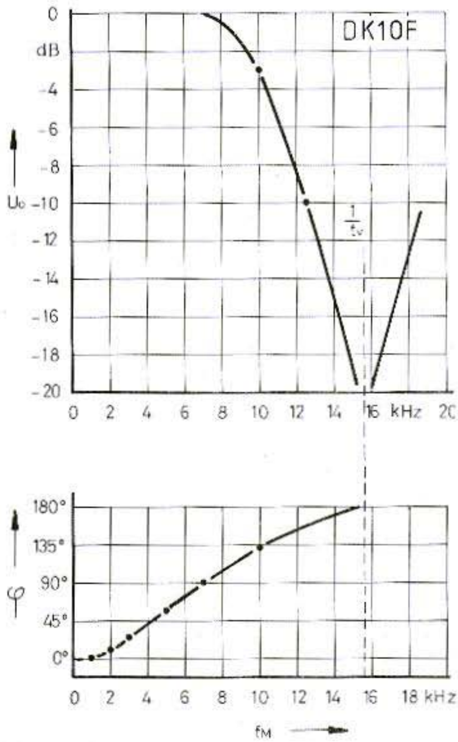

Fig. 11: Transition function according to amplitude and phase

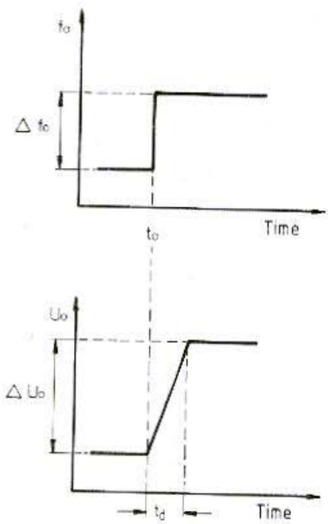

Fig. 12: Jump reply

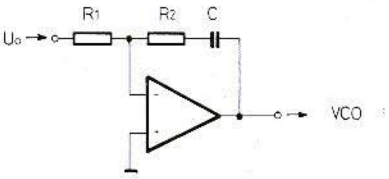

Fig. 13: PI-control as lowpass filter

The lowpass filter given in Figure 2 has the task of stabilizing the control circuit, which means that it should provide an optimum amplitude and phase response over the frequency range. A so-called PI-control as shown in **Figure 13** is suitable. The values of R_1 and C are responsible for the integration time constant ($\tau = R_1 \times C$); the proportional gain $K = R_2/R_1$ ensures that the control can react quickly to small deviations. As is to be shown later, the control loop can be designed so that interference signals of less than approximately 3 kHz (hum, noise, microphonics) can be controlled, whereas the VCO will exclusively determine the quality of the generated signal at higher frequencies.

3. OTHER FREQUENCY RANGES

As previously mentioned, the "original version" of the delay line PLL-oscillator shown in Figure 2 can only be used in the frequency range in which the insertion loss of the delay line remains sufficiently low. If the concept is to be used for higher frequencies, it is possible for frequency division to be used. Semiconductor manufacturers offer suitable ICs, which can operate up into the GHz-range. **Figure 14** shows a principle of construction with the aid of a practical application: An oscillator signal of 100 to 200 MHz is required for a signal generator or receiver. The VCO is able to provide these frequencies; its output signal is divided by factor 32 so that a period of 3.125 to 6.25 MHz results, with which the delay line can operate. A range of 32 x 15.625 kHz = 500 kHz is tuned per revolution of the frequency control. The frequency divider can also be used for driving the required frequency counter.

The block diagram of a receiver for the 2m amateur band is shown in **Figure 15**. The required oscillator signal is generated in a VCO, and fed to the receive mixer. Furthermore, it is also fed to a second mixer where it is mixed with a fixed frequency of 131 MHz (for instance from a crystal oscillator 65.5 MHz and doubler). The resulting difference frequency of 4 to 6 MHz can now be processed as previously described. This shows that it is also possible to increase the range of the delay line PLL-oscillator by frequency conversion.

This series of articles is to be continued in the next editions of VHF COMMUNICATIONS with the following descriptions:

- A VFO from 5 to 6 MHz (original oscillator as shown in Figure 2), as a first step into this technique; the PC-board described there can be used for the other constructional articles.
- Receive mixer for 144–146 MHz with high-level mixer and low-noise oscillator according to DJ7VY.
- Shortwave receiver for 10 kHz – 32 MHz with high-level mixer, and preselector (single-conversion superhet with 10.7 MHz or 9 MHz IF)
- Prescaler module for input frequencies up to 200 MHz (universal application, e.g. for measuring applications).
- Programmable frequency counter (6-digit), constructed using inexpensive CMOS-chips without special components.
- Interface board for digital frequency selection using numerical switches or computer control.

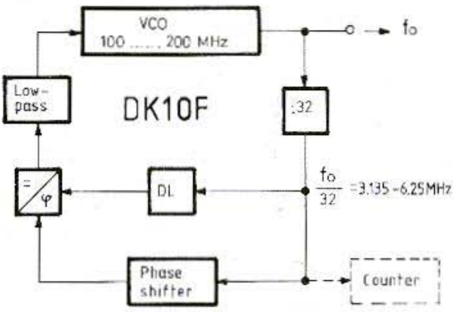

Fig. 14: Extending the frequency range using frequency division

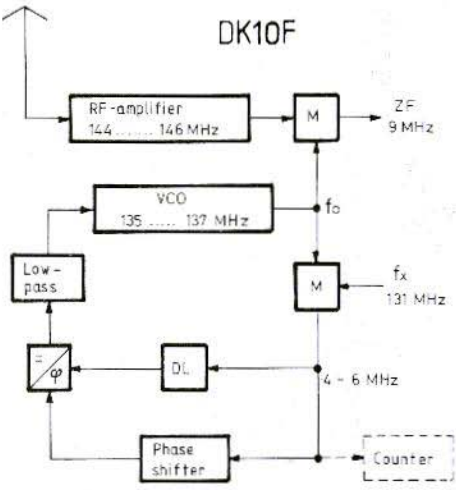

Fig. 15: Extending the frequency range using frequency conversion

Final Note

For many readers, this article describing the fundamentals of this technique may seem to be boring. However, the author would like to underline that he wishes to provide incentives for experimentation, and not only to describe proven designs. This, of course, requires a certain minimum of theoretical background. The practical construction articles are to be commenced in the next edition.

Friedrich Krug, DJ 3 RV

A 10 MHz Timebase Clock for Frequency Counters, complete with a PLL for DCF77

If one attempts to measure the frequency of a RF-signal exactly using a number of different frequency counters, one will experience that a number of different measured values will be obtained due to the fact that the timebase clocks usually differ from the nominal frequency. For this reason, the author developed a 10 MHz standard for testing and aligning the timebase clocks of frequency counters. The frequency is coupled to the 6.2 MHz signal from the DCF77 receiver, described in Edition 2/84 of VHF COMMUNICATIONS (1), with the aid of a phase-locked loop. This provides a sufficiently accurate standard.

The clock oscillator of a digital frequency counter should oscillate exactly at the nominal frequency, and possess a good long-term stability, since any deviation will cause a correspondingly large relative error of the readout. For this reason, a high-quality oscillator is required such as a temperature-compensated crystal oscillator (TCXO), or even better an oven-controlled crystal oscillator (OCXO).

In order to compensate for the long-term drift of the frequency due to aging, it is advisable to use a control circuit that is derived from a standard frequency.

When using the DCF77 receiver described in (1), a reference signal will be available with which such a frequency control can be made with relatively simple means.

The described module uses an available oscillator, i.e. a temperature-compensated 10 MHz crystal oscillator (TCXO), with a capacitive fine frequency alignment. This oscillator represents a good clock even when it is not controlled. This means, that it provides a very accurate frequency standard even if the DCF77 transmitter should go off the air.

The frequency control is made via a phase-locked loop (PLL). Either the 6.2 MHz signal, or the 3.1 MHz signal from the DCF77 receiver is used as reference signal.

Since the module is to be used as a clock for digital circuits, the 10 MHz output signal provided at the output is at TTL-level. It can be divided down to 1 Hz using decade dividers. Any decade frequencies from 10 MHz to 1 Hz, and intermediate values of 5 MHz, 500 kHz, etc. down to 5 Hz are available by using ÷5 and ÷2-dividers. This makes the clock also suitable for other applications.

Due to the possibility of resetting the six lower frequency divider decades, it is easily possible to generate the required switching and control signals for a digital counter.

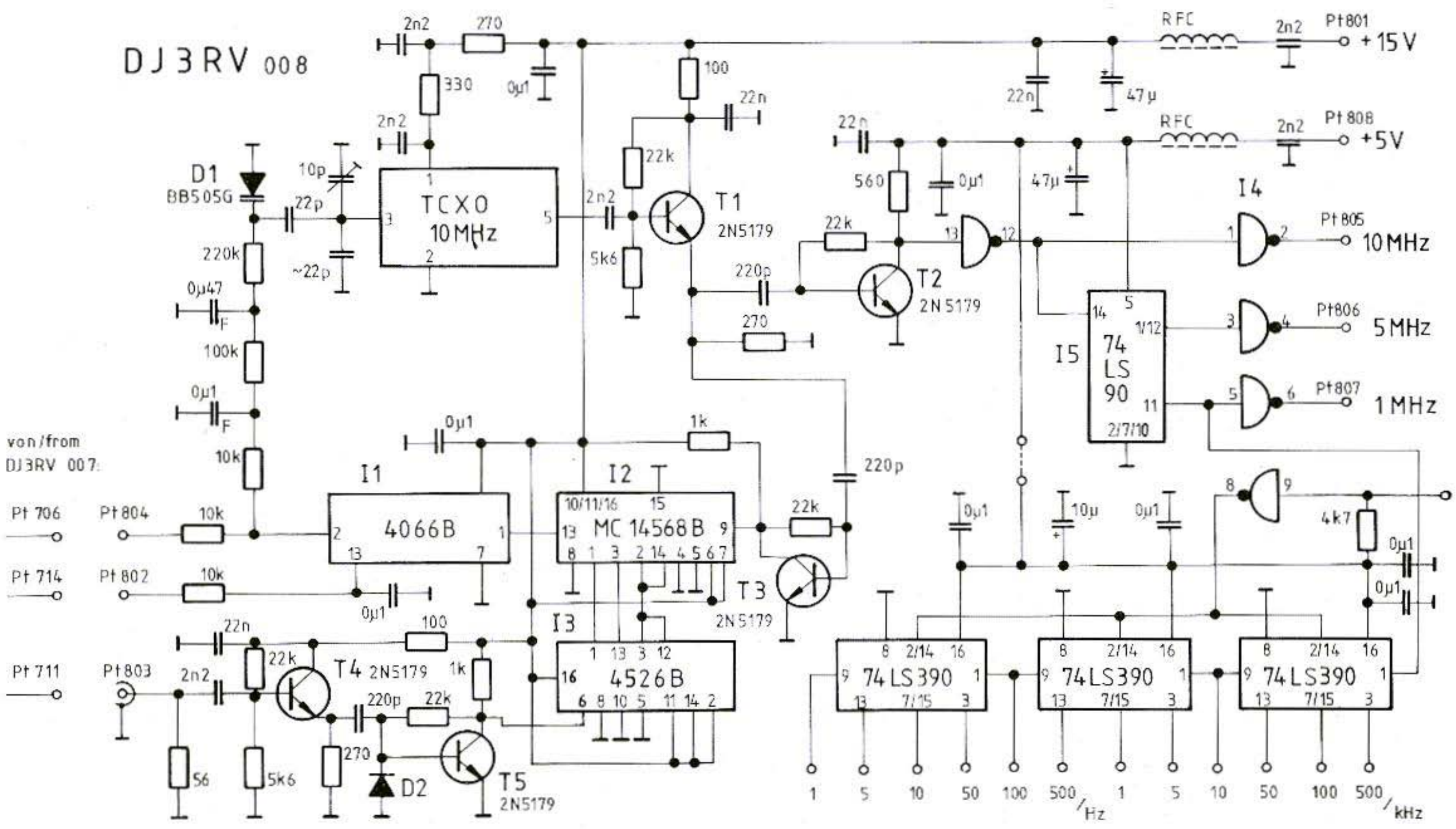

Fig. 1: Circuit diagram of the 10 MHz oscillator module with programming of the divider for a reference signal of 6.2 MHz

1. CIRCUIT DESCRIPTION

As can be seen in the circuit diagram given in **Figure 1**, a temperature-compensated crystal oscillator (TCXO) provides the required 10 MHz-signal whose frequency can be pulled using a variable capacitance. According to the manufacturer, this capacitance of 27 pF comprises a fixed capacitance, a 10 pF-trimmer for fine alignment, and the varactor diode D 1 for frequency control.

The frequency control using the phase comparator I 2 is similar to that used in module DJ3RV 007 (1). The 10 MHz output signal of the TCXO is fed via buffer amplifier T 1 and an impedance converter to level converter T 3 (CMOS-level), and then divided in I 2. The frequency division factor amounts to 100, which is programmed by connecting pins 10 and 11 to "high".

The 6.2 MHz reference signal from module DJ3RV 007 is fed to connection Pt803, and amplified to CMOS-level in T 4 and T 5. Integrated circuit I 3 and the second programmable divider in I 2 divide this signal by 62 and feed it to the phase comparator.

Unfortunately, it was found that not all CMOS-dividers operated well at 6.2 MHz. For this reason, the next section is to study the possibility of injecting a 3.1 MHz signal, and to divide this by 31.

The phase comparator operates at 100 kHz; the control signal is available at the tri-state output I 2/pin 13. With the aid of switch I 1, it is possible for this signal to be switched off when DCF77 is not transmitting. The switching voltage is fed to Pt802, and is also supplied by module DJ3RV 007. In this case, a very stable voltage of 5 V will be present at diode D 1 which is fed to Pt804 also from the DJ3RV 007-module.

The 10 MHz signal is amplified in T 1 and T 2 and is coupled out at TTL-level at Pt805. The divider I 5 divides by 2 and 5 so that a 5 MHz-signal is available at Pt806, and a 1 MHz-signal at Pt807.

A further divider chain is available on the board that comprises six decadic dividers, which means that signals down to 1 Hz are available. This divider chain can be reset, frozen, and started in a defined manner. It is thus possible for the control signals to be generated for a frequency counter.

2. CONSTRUCTION

The circuit is accomodated on a single-coated PC-board (DJ3RV 008), which is enclosed in a metal box of 74 x 148 x 50 mm (see **Figure 2**).

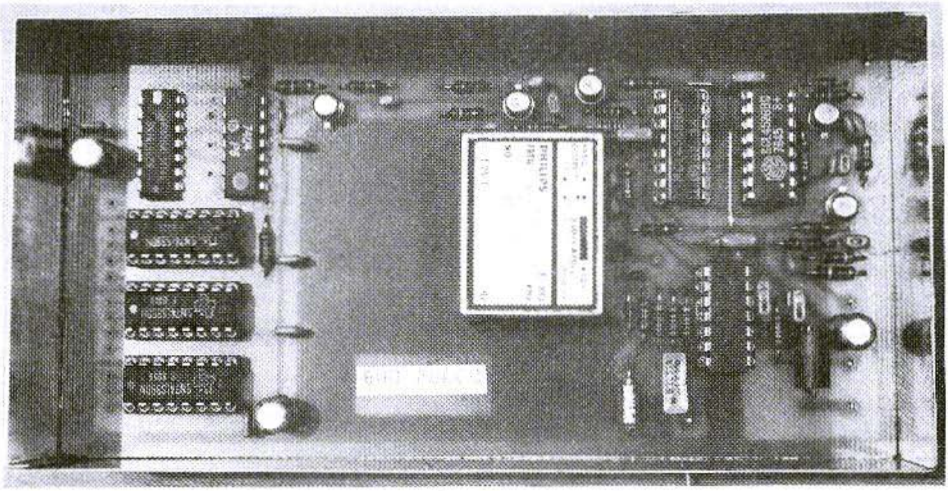

Fig. 2: Photograph of the author's prototype oscillator module DJ 3 RV 008
The ICs in the PLL should be soldered into place.

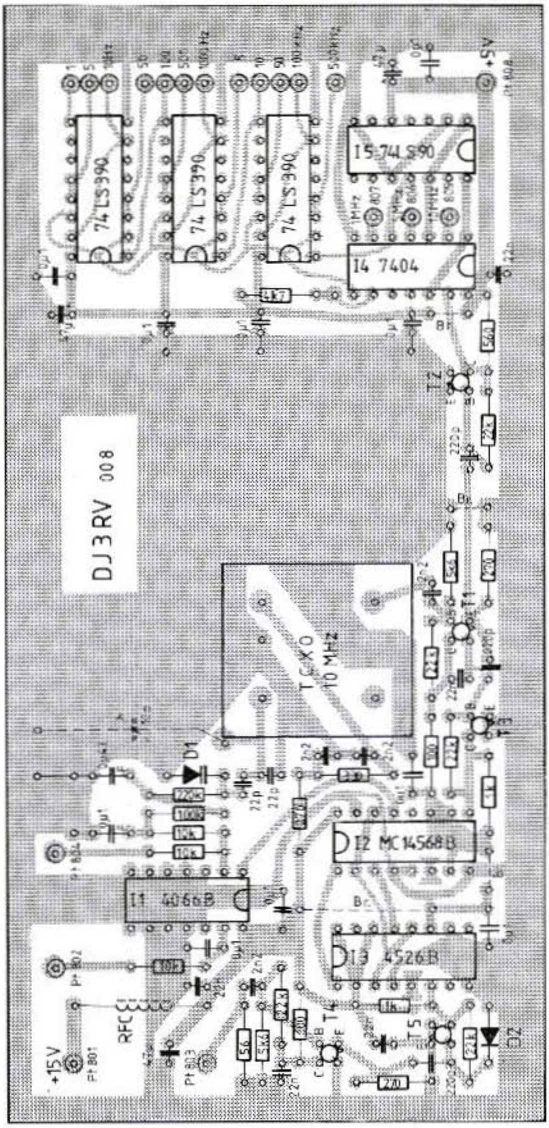

Fig. 3: Component location plan for the single-coated board DJ 3 RV 008

The location of the components can be seen in the component location plan given in **Figure 3**. The special components are given in the following components list:

Components List for DJ3RV 008

T 1 to T 5: 2N5179 (RCA) or similar UHF-transistor, e.g. BFX 89, BFY 90

I 1: 4066 B (RCA etc.)

I 2: MC 14568 B (Motorola)
I 3: MC 14526 B (Motorola etc.)
I 4: 7404 (TI etc.)
I 5: 74LS90 (TI etc.)
I 6 to I 8: 74LS390 (TI etc.)
D 1: BB 505 G (Siemens etc.)
D 2: 1N 4151 or similar
TCXO: Temperature-compensated crystal oscillator TEKO 10.000 kHz, Philips, Order-No. 4322 191 00001
Trimmer: 10 pF air-spaced trimmer, Johanson, type 5200

Some CMOS-circuits I 2 and I 3 will not be able to divide the 6.2 MHz signal by 62, which means that it is necessary to use a reference frequency of 3.1 MHz. In order to do this, it is necessary for diodes D 4 and D 5, as well as the filter comprising L 2 and the capacitor of 100 pF to be removed from the PC-board DJ3RV 007, as shown in **Figure 4a**, and be replaced by a wire bridge. The output signal at Pt 711 is then no longer sinewave, but slightly limited.

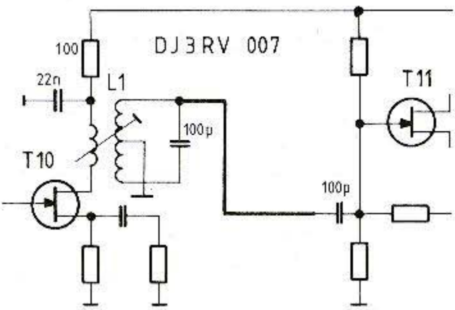

Fig. 4a: Modification of the circuit DJ 3 RV 007 to obtain a 3.1 MHz reference signal

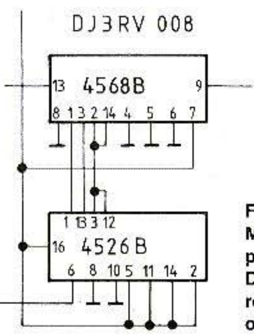

Fig. 4b: Modification of the programming of board DJ3RV 008 for a reference frequency of 3.1 MHz

It is now necessary for the dividers in I 2 and I 3 on PC-board DJ3RV 008 to be programmed to 31, as shown in **Figure 4b**.

The two dividers are connected in series and are binary coded. The lower four bits are set on I 3, and the upper four bits on I 2.

00011111 $\triangleq$ 31
00111110 $\triangleq$ 62

As can be seen with the given binary numbers, only two positions are changed. These are pin 5 of I 3 and pin 6 of I 2. These pins are still not wired on the board and must be programmed using the bridges!

Dividing by 62:
As given in circuit diagram Fig. 1:
Pin 5/I 3 to ground, and pin 6/I 2 to − 15 V

Dividing by 31:
Pin 5/I 3 to + 15 V, and pin 6/I 2 to ground.

In principle, it is possible for the divider circuit to be programmed for other reference frequencies, or division ratios if the conductor lanes on the PC-boards are modified as required. It is important that the reference frequency should be an even multiple of 100 kHz (at least 16 times), otherwise the divider in I 2 cannot be programmed when using the given circuit.

When using the module as a clock for a frequency counter, it is more favorable to increase the loop gain in the frequency control circuit of module DJ3RV 007. The modifications to the circuit are shown in **Figure 5**. Varactor diode D 2 is connec-

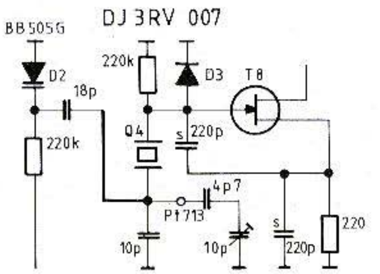

Fig. 5: Increasing the pulling range of the crystal oscillator on DJ3RV 007

ted to the hot end of crystal Q 4 via the 18 pF capacitor, and the series capacitor is reduced to 10 pF. The pulling range of the crystal will then be greater, however, the stability and noise behaviour will be slightly inferior. Holes and lines are provided on the PC-board for this modification.

3. CONNECTION AND ALIGNMENT

Connect the well stabilized operating voltages to Pt 801 and Pt 808. This is followed by connecting a 10 MHz TTL-signal to PT 805. The values given for the current drain are for orientation. With the control circuit switched off (Pt 802 to ground), the frequency of the TCXO should be aligned to exactly 10 MHz with the aid of the 10 pF trimmer. After switching on the control circuit, the frequency should remain phase-locked to the reference signal. The control can be checked at pin 2/I 1, if the frequency of the TCXO is temporarily shifted by touching pin 3.

The transcient behaviour of the control circuit is determined by the time constant of the filter links previous to diode D 1. In practical operation, a capacitor having a value of between 0.22 µF and 2.2 µF has been found suitable. The value of 0.47 µF given in the circuit diagram provides good results.

4. REFERENCES

1) F. Krug, DJ 3 RV
A Receiver for the VLF Time and Frequency Standard Transmissions from DCF 77
VHF COMMUNICATIONS 16, Edition 2/1984, Pages 96–114

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Simple Locus Curves in the Smith Diagram

Impedances of antennas, inputs and outputs of amplifiers, components, etc. are often displayed according to real and reactive components as a function of frequency in one plane as a "locus curve". The "Smith Diagram" is especially suitable for such display. This can be considered to be a "bent" complex plane. The capacitive or inductive behaviour of the test object, return loss, matching range, and standing wave ratio as a function of frequency, and more, can be taken from the position and the frequency-dependent run of the impedance locus curve. It is possible to determine the L, R, and C of the two-pole and to select suitable compensation or matching measures.

Figures 1a and 1b show simple locus curves. In both cases, the standardized impedance Z_{st} is 50 Ω (reference impedance), since this is the standard impedance used in conjunction with most measuring systems in the VHF and UHF

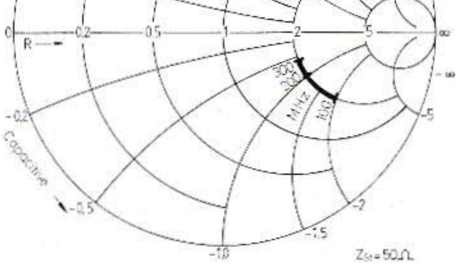


Fig. 1a:
Locus curve of a series-circuit of R and C

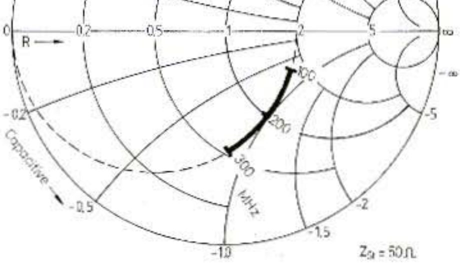


Fig. 1b:
Locus curve of a R/C-parallel circuit

range. According to the locus curve shown in **Figure 1a**, it will be seen that the measured object only represents a **series-circuit** comprising an ohmic resistance and a capacitance:

- The real component (R' = 2) is constant for all frequencies of the locus curve, which is only valid for series circuits; after destandardization: $R = 2 \times 50\ \Omega = 100\ \Omega$.
- The reactive component is reduced on increasing frequency, and seems to be inversely proportional to the frequency, since the spacing is reduced (−2; −1; −0.66), which can only be valid for a capacitance.
- The locus curve is within the negative half of the plane, which is a further indication of a capacitive construction! $X_c'_{100\,MHz} = -2$, or destandardized $X_{c\,100\,MHz} = -2 \times 50\ \Omega = -100\ \Omega$, which corresponds to approx. 16 pF!
  $X_c'_{200\,MHz} = -1$, $X_{c\,200\,MHz} = -1 \times 50\ \Omega =$
  $= -50\ \Omega$. Minus sign means "capacitive".

As can be seen in **Figure 1b**, the locus curve does not possess a simple systematic behaviour between 100 MHz and 300 MHz. Both the real and reactive components of the individual locus-curve points are different! Digital impedance meters would indicate the real and reactive components for the various frequencies according to the table given in **Figure 2** (factor "j" for "reactive component", and sign "−" for "capacitive"). The user will firstly determine from the numerical values that the test object represents a series circuit with a reactive component, whose value is frequency-dependent. This is nothing special.

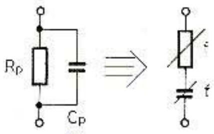
Furthermore, he will determine that the real component is frequency-dependent, and this is rather peculiar when one does not consider the skin effect!

Actually, the test object is a simple, parallel circuit comprising an ohmic resistance (of course with a constant value), and a capacitance. The following is to show how such a locus curve is made. Firstly let us examine why a **parallel connection of R_p and C_p** must be present:

- The curve of the impedance as a function of increasing frequency turns towards the zero-point of the impedance plane; in the case of $f \to \infty$, it seems that the impedance decreases towards zero, which is the case with a parallel capacitance: it will short out the ohmic resistance at higher frequencies!
- It seems on studying the locus curve that a real component remains at very low frequencies, which means that the parallel capacitance C_p is not effective, since the locus curve will exhibit a real component at $f \to 0$, in other words for DC-voltages. In the example shown in Figure 1b this will be the value R' = 2, or destandardized $R_p = 2 \times 50\ \Omega = 100\ \Omega$.

However, a prerequisite of the previous assumptions is that the considered part of the locus curve is **part of a semicircle**, which can be assumed due to the position of the three curve points for 100, 200 and 300 MHz. Only then can one assume a **RC-parallel circuit**!

A **RL-parallel circuit** would also result in a semicircular line in the resistance plane, however, in the upper resistance plane. In this case, the semicircle will be in the direction of the zero point for $f \to 0$ (the inductance will short out the parallel ohmic resistance for DC-voltages, f = 0), and at $f \to \infty$ it will go through R_p (the parallel inductance is high-impedance at higher frequencies, and



f MHz	Real component	Reactive component
100	80 Ω	−j 40 Ω
200	50 Ω	−j 50 Ω
300	30 Ω	−j 46 Ω

Fig. 2: Table of the real and reactive components of the equivalent circuit

therefore does not have any effect on the ohmic impedance).

There are two possibilities to obtain the coordinate values R_s and X_s of the equivalent series-circuit as a function of frequency from a parallel connection of R_p and X_p, in order to display it in a locus curve as shown in Figure 1b: Either with the aid of equations, or by using a graphic method.

The **calculation equations** are:

$$R_s = \frac{1/R_p}{(1/R_p)^2 + (1/X_p)^2},$$

$$X_s = \frac{1/X_p}{(1/R_p)^2 + (1/X_p)^2}.$$

In the case of a parallel capacitance, insert $X_p = -1/\omega C_p$, and with a parallel inductance $X_p = +\omega L_p$. NOTE: The sign "−" of the capacitive, and "+" of the inductive reactive impedance indicates the phase between voltage and current!

Example: The following is assumed:
$R_p = 100\ \Omega$, $C_p \approx 8$ pF. This results in:
$X_p = -1/(2 \times \pi \times 10^8\ \text{Hz} \times 8 \times 10^{-12}\ \text{F}) = -200\ \Omega$.
This is valid for 10^8 Hz ≙ 100 MHz.

The following can be determined from this:

$$R_s = \frac{^1/_{100}}{(^1/_{100})^2 + (^1/_{(-200)})^2}\ \Omega \approx 80\ \Omega,$$

$$X_s = \frac{^1/_{(-200)}}{(^1/_{100})^2 + (^1/_{(-200)})^2}\ \Omega \approx -40\ \Omega.$$

This allows the series values given in the Table in Figure 2 to be checked.

The **graphic method** is more of interest here. This is made as follows:

The real and reactive impedance R_p and X_p are standardized with Z_{st} and from their reciprocal values conductance and susceptance are obtained: G' and B' (the apostroph is used to show that these are standardized values!). These values are now inserted into a separate Smith diagram (**Figure 3, above**) which then serves as "conductance plane". The actual **advantage of such a diagram** is: The coordinates R_s' and X_s' of the equivalent series circuit are symmetrical around the center (≙ 1) of the Smith diagram. This means

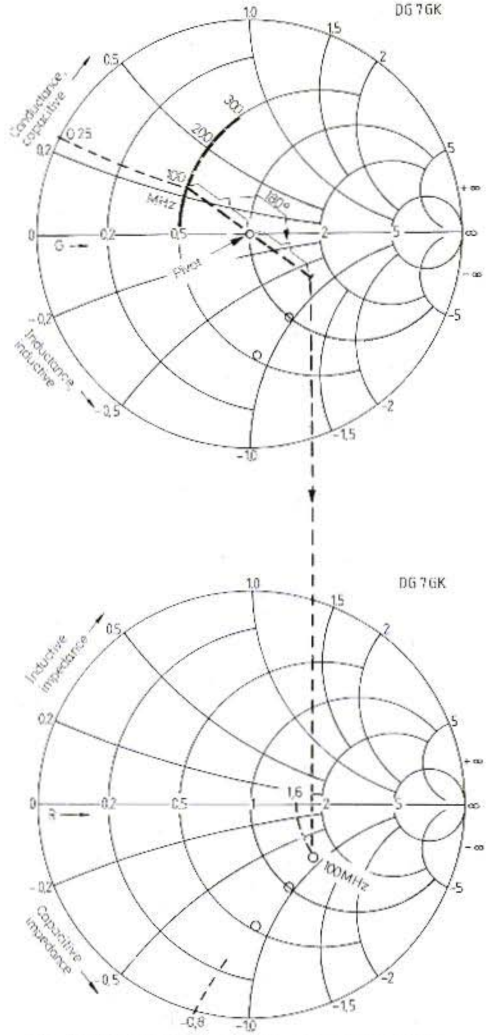


Fig. 3: Smith diagram: above conductance plane, below impedance plane

that if one rotates the point for the conductance value around the center of the diagram by 180° and inserts the new position into a second Smith diagram which is used in the resistance plane (see **Figure 3, below**), the coordinates of the transposed point will directly give the (standardized) real and reactive components of the equivalent circuit without having to use the extensive formulas given in the previous section.

Example: The conductance and susceptance values of a parallel circuit comprising 100 Ω and a capacitance of 8 pF are to be inserted in the conductance plane of a Smith diagram for a frequency of 100 MHz. The coordinates of the real and reactive impedance of the equivalent series circuit are to be obtained from the point transposition! Standardized impedance is $Z_{st} = 50\ \Omega$.

Solution: (also see Figure 3, above and below):
$R_p = 100\ \Omega$, $X_{pc} = -1(2 \times \pi \times 10^8 \times 8 \times 10^{-12})\ \Omega = -200\ \Omega$.
$R_p' = 100\ \Omega / 50\ \Omega = 2$.
$X_{pc}' = -200\ \Omega / 50\ \Omega = -4$.

The standardized conductance values G' are obtained from the reciprocal values of the standardized impedances as follows:

$G' = 1/2 = 0.5$ and $B_c' = -(1/-4) = +0.25$.

NOTE: The change of sign on transposing the reactive impedance to the susceptance, and vice versa is necessary because the sign indicates the angle of the voltage reffered to current with respect to resistance, whereas in the case of conductance values the sign indicates the angle of the current with respect to the voltage. This means that a negative susceptance value B_L will result from a positive, parallel, inductive reactive impedance X_{pL}!

The standardized conductance values, for example 0.5 and +0.25, are now inserted into the conductance Smith diagram as shown in Figure 3, above. The symmetrical line is now drawn through the center point of the diagram to obtain the symmetric reciprocal point. The symmetrical point will have the same spacing to the center of the diagram, since the reflection factor does not change due to this (theoretical) conversion process. It is now necessary for this point to be transferred to a second Smith diagram (Figure 3, below) which is the impedance plane. The coordinates of this point in the impedance plane are the standardized values of R_S and X_S of the equivalent series circuit, and are $R_s' = 1.6$ and $X_s' = -0.8$. After destandardization one will obtain the following impedance values that are given in the Table of Figure 2 for 100 MHz:

$R_s = 1.6 \times 50\ \Omega = 80\ \Omega$, $X_s = -0.8 \times 50\ \Omega = -40\ \Omega$.

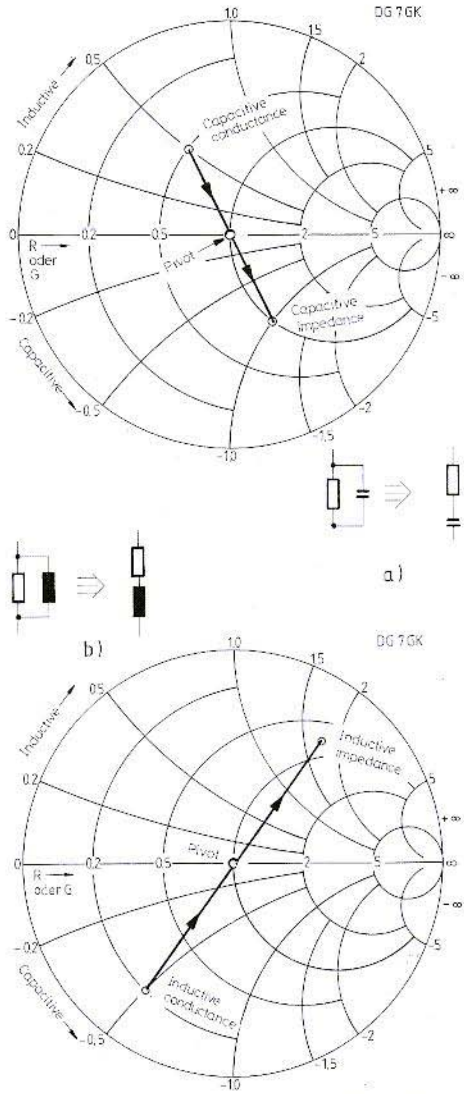


Fig. 4: Conversion (inversion) of a parallel circuit ($G = 1/R_p$; $B = -1/X_p$) into a series-circuit (R_s;X_s)
a) Parallel circuit of R and C
b) Parallel circuit of R and L

It is now possible to insert the values for 200 MHz and 300 MHz into the conductance plane (Smith diagram, Figure 3, above) in a similar manner, and to transpose them into the impedance plane of the Smith diagram by rotating them by 180°. The interconnection of these points results in the locus curve given in Figure 1b, which also shows graphically that the circuit is a parallel connection.

At first, it is recommended that separate Smith diagrams are used for conductance and impedance planes. It can be advantageous to have one of the two in the form of transparent paper or foil. Lateron, after sufficient experience has been gained, it will be possible for the user to insert the standardized conductance values, and read out the standardized impedances using the same diagram, and to interpret the coordinates correctly either as conductance coordinates or as impedance coordinates (see **Figure 4a and 4b**). Figure 4b shows that the same is valid for parallel circuits with an inductive component, as was shown for such with a capacitive component; it is only necessary to exchange the sign of the reactive component.

As has been previously mentioned, it is possible with sufficient knowledge and correct interpretation of the locus curve to find suitable transformation and matching networks. The capacitive component of the circuit shown in Figure 1a, for instance, can be compensated for by using a series-connected inductance (see **Figure 5a**). This results in a series-resonant circuit, and one will see that the compensation is only valid exactly for one frequency on the locus curve, (this frequency is 100 MHz in the case of Figure 5a). In a Smith diagram for impedances, this will mean that the locus-curve point to be compensated is shifted towards the positive plane due to the series-inductance. The new locus curve will, however, remain on the original coordinate of constant real component. In the example given in Figure 1a, this is the standardized real component R' = 2, or destandardized R = 100 Ω. The ohmic component is thus identical after compensation. A matching to another ohmic impedance, for instance 50 Ω, cannot be achieved by series-connection of a further reactive element. This is only possible with the aid of a parallel capacitance in conjunction with a series inductance; however, further details regarding this are not to be discussed here.

In the case of a circuit as shown in Figure 1b and Figure 2, it is possible to achieve not only a compensation of the reactive component, but also a transformation to another real impedance, such as 50 Ω, with the aid of a series-connection of an inductance (see **Figure 5**). This, of course, is also only valid for one discrete frequency, however, the large spacing of the real and reactive components is shifted relatively near to the center of the diagram 1 ≙ 50 Ω, in the vicinity of this frequency, as can be seen in Figure 5b.

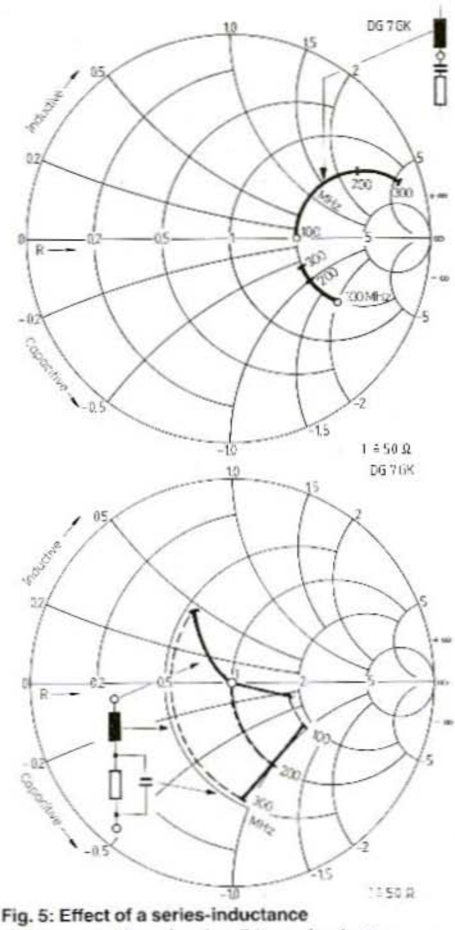


Fig. 5: Effect of a series-inductance
a) Compensation of series-C by series-L at a discrete frequency
b) Matching to 1 ≙ 50 Ω at one frequency using a series-inductance L

The selection of the value of such reactive elements for transformation and compensation networks is not the task of this article.

Manfred Claar, DF 9 EY

A programmable Rotator Control

The described rotator control is able to position an azimuth and elevation rotator simultaneously. The problem of running two rotators with the aid of a common control cable has been solved elegantly by use of a serial port. This has also solved the problem of interference to the receiver from the computer system.

The rotator control system comprises two different modules that are interconnected via a 6-core control cable (**Figure 1**). The first is the microprocessor system that is located in the vicinity of the rotator, and comprises a processor card, a 5 V power supply, and two interface boards.

The other module is the control unit that is located in the operating room. It is provided with a digital

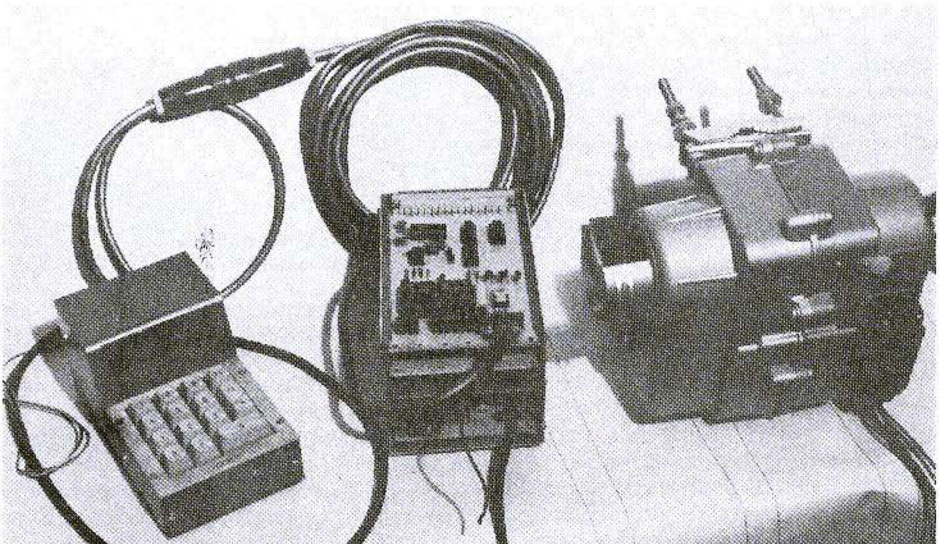


Fig. 1: Photograph of the author's prototype complete with control unit, processor system and elevation rotator KR-500

Fig. 2: Author's prototype control unit showing 27° elevation, manual operation (H), and 197° azimuth

readout that shows the actual position of the antenna. It is also provided with a keyboard for inputting the required angular values (see **Figure 2**).

The software (user program) for the rotator control system can be used on all 6502 or 6504 systems, and can therefore be used without problems, for instance, using the legendary computers KIM-1 or SYM-1. These two systems, as well as better and smaller systems, are well known throughout the world, however, it is not within the scope of this article to give a list of all single-board computer manufacturers using the 6502/04 system.

1. DESCRIPTION

The microprocessor card for the rotator control really only requires three integrated circuits. This minimum configuration should comprise:

1. A CPU-6502 or 6504 (Central Processing Unit)
2. An integrated circuit type RIOT-6532 (RAM, I/0, Timer)
3. A program memory EPROM-2716 (Erasable PROM)

The CPU is the central processing unit that carries out the logic, algebra, transport and jump orders in conjunction with the EPROM.

The RIOT is provided with two bidirectional, programmable 8-bit input/output ports, a programmable clock, and a random access memory (RAM 128 x 8 bit).

The last IC is the program memory. The use of software for the rotator control is accommodated in the 2K-EPROM, and is therefore not lost when disconnecting the power supply.

It should not be difficult to develop such a simple card, or to obtain one suitable for this application. In the following description, we will be using an EMUF (4). The only important things to consider during selection of suitable hardware are the following:

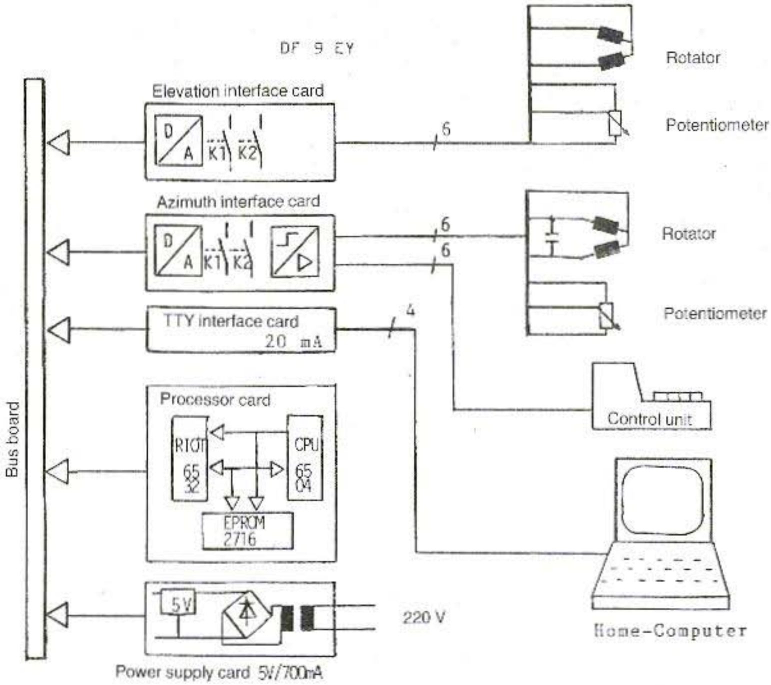


Fig. 3: Overall block diagram of the μP-rotator control system

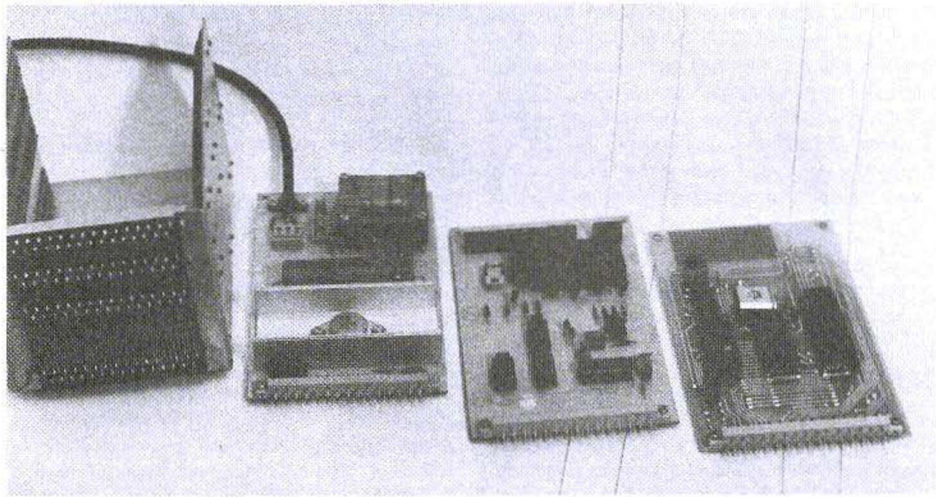


Fig. 4: From left to right: Case with bus-board, power supply card, interface card, and processor card

1.1. The Microprocessor System

The microprocessor system as shown in **Figure 3** is accommodated in a U-shaped aluminium case. It can be slid into the case using plastic rails, and the electric connections are made using a 31-pin connector strip to the buscard; (see **Figure 4**).

1. The EPROM uses the memory range from $ 9800 to $ 9FFF.
2. The RIOT is actuated from $ 9200.

It is, however, also possible to carry out an address change in the user program relatively easily.

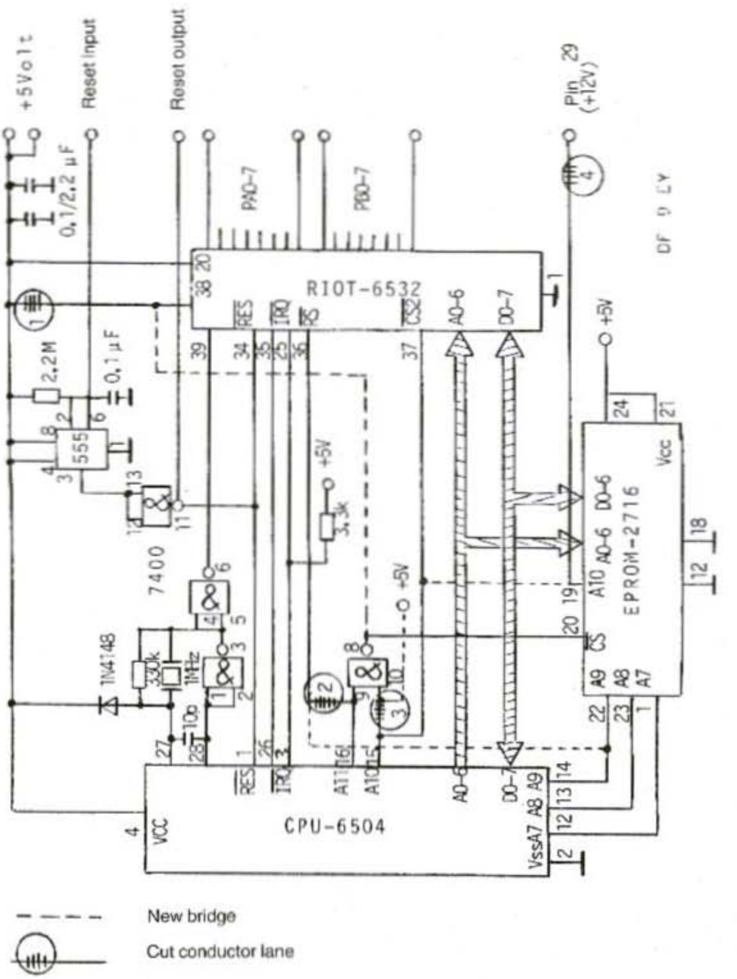


Fig. 5: Block diagram of the EMUF-board extended to have an address memory of 2 kByte

The Processor Card

The single-board microcomputer for universal fixed-program applications (EMUF) was described in (1). This IC is the heart of the rotator control. A complete kit of parts (without EPROM) is available in Germany from several companies.

This mini-system as shown in **Figure 5** comprises only five integrated circuits, which are all accommodated on a Europacard equipped with a 31-pin connector strip. These are the CPU-6504, the program memory 2716, the RIOT 6532 with ports A and B for the inputs and outputs, a timer-IC 555 for actuating the hardware reset, and a TTL, quadruple NAND 7400 for address selection and for generation of the clock frequency of 1 MHz.

The disadvantage of this system is the limited address possibilities. In order to use all of the 2 KByte memory of the 2716, a small modification has to be made. To achieve this, it is necessary to cut the conductor lanes at four positions and to provide four wire bridges. These modifications to obtain extended address capabilities are given in the circuit diagram.

The operation of the card is not critical. If the operating voltage is between 4.8 and 5.2 Volt, the current drain does not exceed approx. 280 mA, and a 1 MHz clock at TTL-level is determined, it is only necessary to check the operation of the reset timer.

The signal at pin 21 of the 31-pin connector strip should jump to +5 V with a delay of approx. 0.3 s on switching on the operating voltage.

Fig. 5a: Connections of the CPU 6504

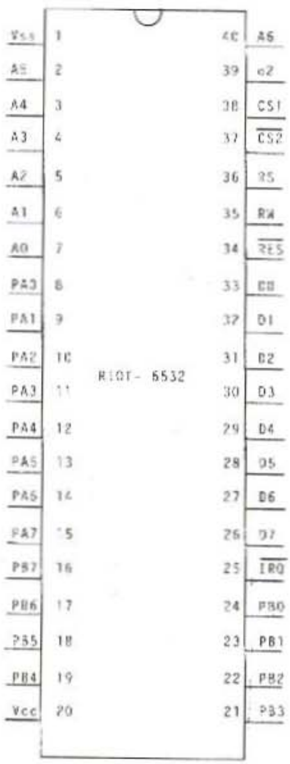


Fig. 5b: Connections of the 6532, which is used as RAM, I/0, and timer array

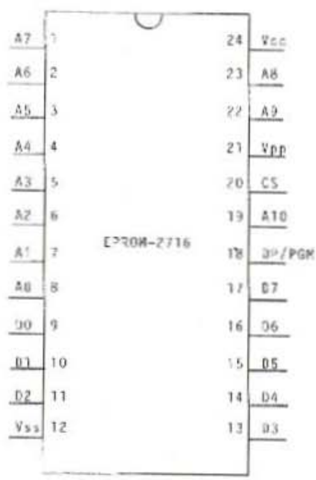


Fig. 5c: Connections of the 2 kByte EPROM 2716

If the processor does not operate, it will be necessary to check the card to see whether there is a short-circuit between conductor lanes, and/or whether one of the integrated circuits must be exchanged.

Connections to Port-A:

PA0 – A/D converter azimuth and elevation
PA1 – A/D converter azimuth and elevation
PA2 – A/D converter azimuth and elevation
PA3 – A/D converter azimuth and elevation
PA4 – A/D converter azimuth and elevation
PA5 – A/D converter azimuth and elevation
PA6 – A/D converter azimuth and elevation
PA7 – A/D converter azimuth and elevation

Connections to Port-B:

PB0 – Azimuth relay, clockwise
PB1 – Azimuth relay, anticlockwise
PB2 – Elevation relay, down
PB3 – Elevation relay, up
PB4 – Clock 1 keyboard
PB5 – Clock 2 readout
PB6 – Data
PB7 – Reply keyboard and ASCII-port

Connections:

Processor Card	Bus-Board
1 Ground	1 Ground
2 Ground	2 Ground
3 N/C	3 N/C
4 IRQ	4 Start serial transmission (ASC II)
5 N/C	5 N/C
6 PA0	6 DA0
7 PA1	7 DA1
8 PA2	8 DA2
9 PA7	9 DA7
10 PA6	10 DA6
11 PA5	11 DA5
12 PA4	12 DA4
13 PA3	13 DA3
14 Ground	14 Ground
15 PB0	15 Relay HR
16 N/C	16 N/C
17 PB1	17 Relay HL
18 PB2	18 Relay VL
19 PB3	19 Relay VH
20 N/C	20 N/C
21 Reset output	21 N/C
22 PB7	22 RM-keyboard
23 PB6	23 Data
24 PB5	24 Clock 2
25 PB4	25 Clock 1
26 Reset input	26 Reset button
27 +5 V	27 +5 V
28 +5 V	28 +5 V
29 N/C	29 N/C
30 Ground	30 Ground
31 Ground	31 Ground

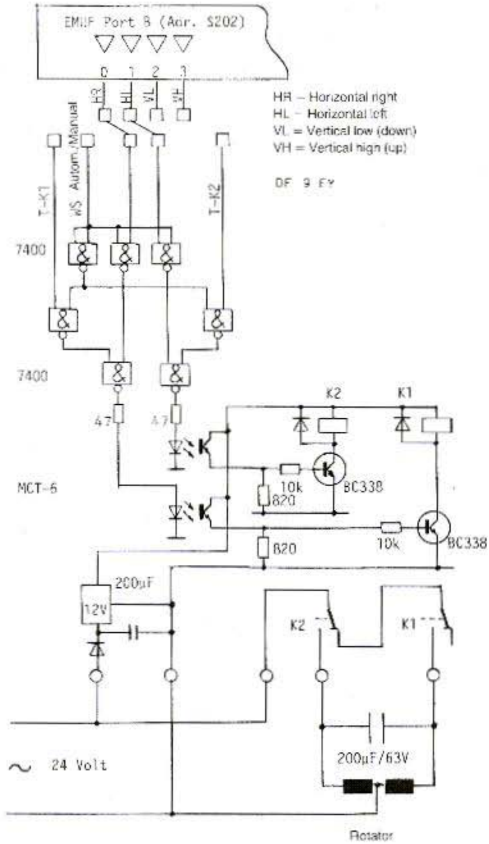


Fig. 6: Parts of the circuit diagram of the interface card: "Relay Drive"

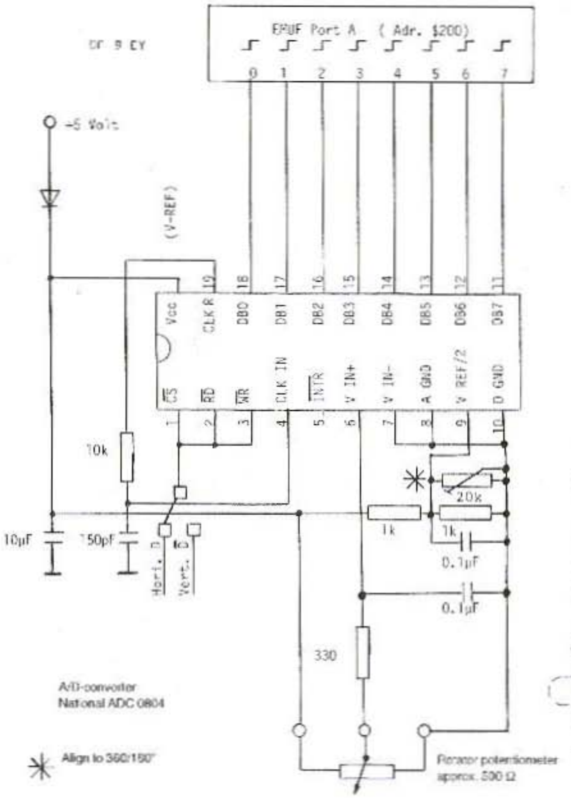


Fig. 7: Part of the circuit diagram of the interface card: "A/D-converter"

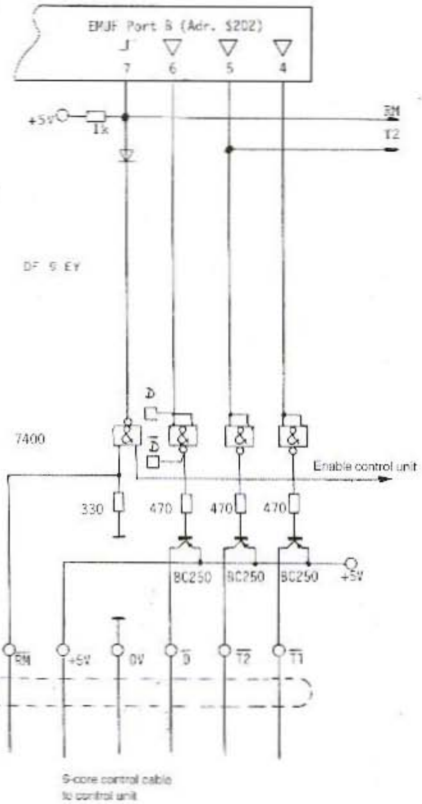


Fig. 8: Part of the circuit diagram of the interface card: "Drive of Control unit"

1.2. The Interface Cards

The two interface cards are identical, and it is therefore worthwile to develop a PC-board for this. Furthermore, the use of a PC-board will increase the reliability of the system considerably.

Each of the two boards accommodates the A/D converter for determining the actual position, two relay outputs, a driver circuit for the operating system, and a connection strip for the connection to the rotator itself (see **Figures 6 – 8**).

An A/D-converter type ADC-0804 manufactured by National Semiconductor is used. It is directly connected to port A via its 8-bit tri-state outputs. Both converters are connected in parallel via the bus board. The selection is made with the aid of the D-line in the case of the azimuth card, and the D̄-line for the elevation card.

The analog signal is provided by the potentiometer in the rotator, and is directly proportional to the pointing angle of the rotator itself. Subsequent to a slope change D/D̄, or D̄/D, and after a certain delay, the digital value is valid for the actual position, and can be interrogated by the program.

A special feature of the relay control is a selector switch for the automatic/manual mode. A keyboard combination for UP/DOWN and LEFT/RIGHT is mounted on the mast. The manual actuation simplifies operational tests on installation, and later maintenance.

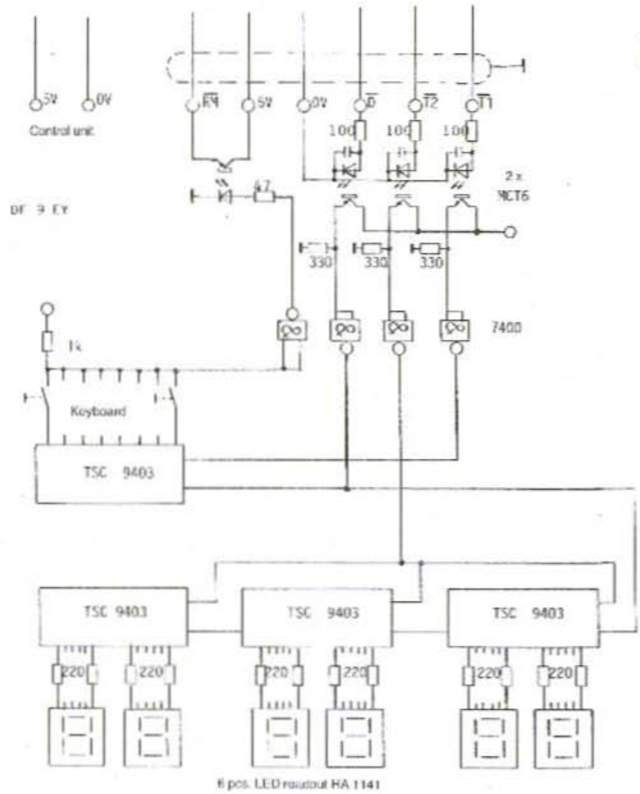


Fig. 9: Circuit diagram of the control unit and readout

1.3. The Control Unit

The control unit is accommodated in a small case, whose dimensions are 40/90 mm high, 100 mm wide, and 170 mm deep. It is provided with a 14-position keyboard, that is driven by a shift register. A 6-digit readout using a 7-segment LED-display is used (**Figure 9**). Three series-connected shift registers are used for driving the individual segments, which in turn require 6 x 8 outputs. The IC "Serial Input/16 Bit Parallel Output Peripheral Driver" type TSC-9403 manufactured by Teledyne Semiconductor has been found suitable and is able to directly drive the readout from its power outputs (60 mA), see **Figure 10**. A further advantage is the simpler overall construction, and the use of only one type of IC (see **Figure 11**).

This hardware structure requires only one data line for driving the A/D-converter and the shift register. The addressing of the keyboard register, or readout register is made via two, separate clock lines. A reply is only to be expected from the keyboard.

All in all, only the following interconnections are required between the control unit and the processor system:

1 data line
1 clock line (keyboard)
1 reply (keyboard)
1 clock line (readout)
1 +5 V and 0 V

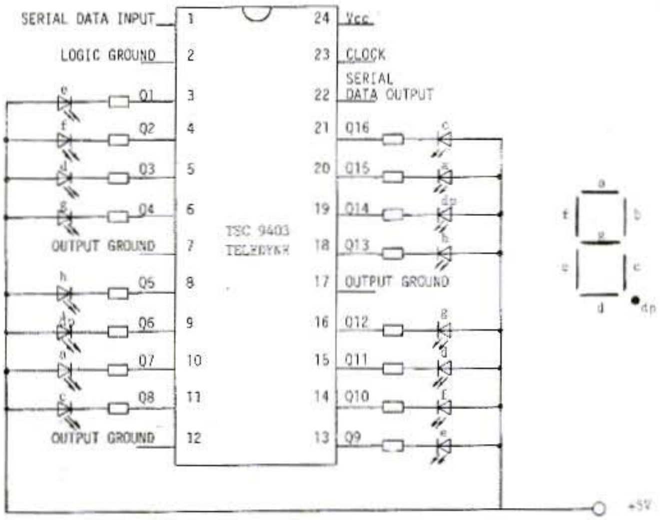


Fig. 10:
Shift register for the readout of the control unit

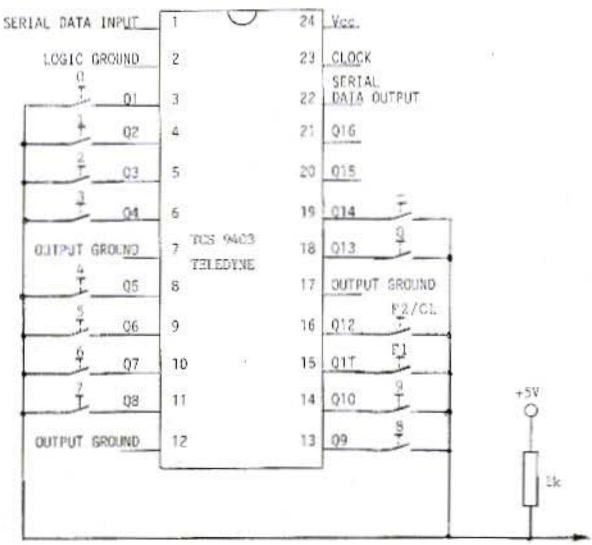


Fig. 11:
Shift register for the keyboard in the control unit

The optocouplers have been especially accommodated in the control unit instead of the interface board. The reason for this is that the high-impedance and very fast (3 MHz) CMOS shift registers must be protected against shortwave transmissions, which are especially present on long, interconnection cables.

The suppression of any interference from the computer to the receive system is not difficult, and only requires one to separate the individual modules. **Figure 12** now shows the interconnection between power supply, interface cards, rotators, and control unit.

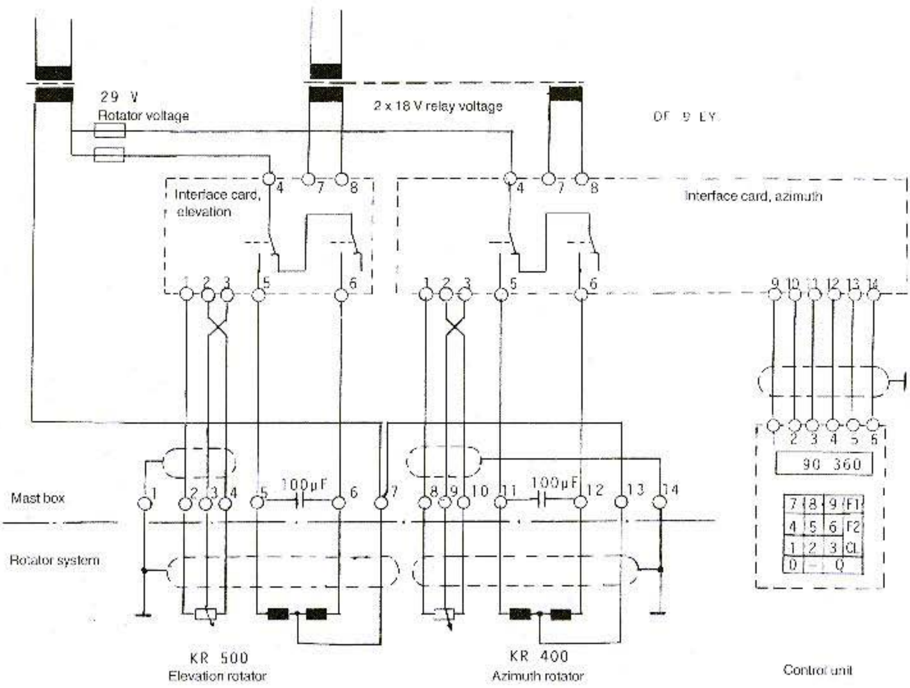


Fig. 12: Interconnection wiring of the programmable rotator control

1.4. The ASCII-Port

It is possible using an ASCII-port as shown in **Figure 13** to directly connect a personal computer that is able to calculate the individual positions and time values. The input of the individual nominal values via the keyboard will then not be required, and operation of the system will become automatic.

The switching to the ASCII-port is made from the control unit by operating the following command:

F1 F1 0 (Band rate) Q
The return to the control unit from the personal computer is made using the ASCII-sign for:
:0<

If the ASCII-mode is selected due to an operating error, and the port is not connected, it will only be possible to switch back to the control unit by providing a hardware reset.

The transmission rate of 300 Bd will be selected automatically after a reset command. If another speed is required, this must be entered. Transmission speeds of 110 Bd to 2400 Bd are permissible. The numerical values for these different Bd-rates are given in the operating instructions (Section 2). Attention should only be paid that a pause is required between the individual ASCII-signs. Otherwise, only the four lowest valuency bits are evaluated, which means that one will obtain various ASCII-signs with the same meaning.

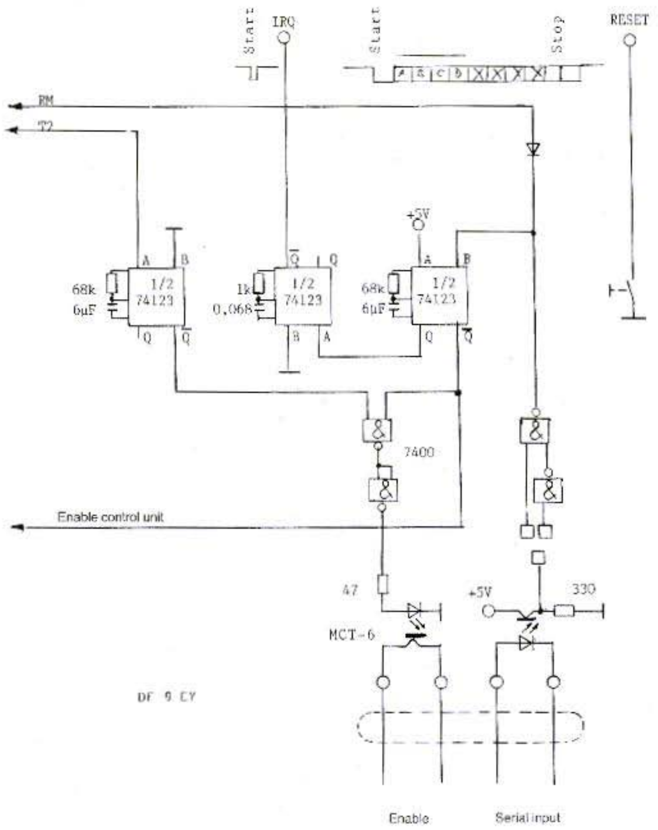


Fig. 13: Circuit diagram of the "ASCII-port 20 mA" card

If the personal computer is controlling the system, all operations can be selected, and it is possible for the nominal values to be inserted.

Example 1:

Required is the setting up of positions 1 to 9 with an azimuth, elevation, and time value:

: : 1 value < value < value <
: : 2 value < value < value <
etc.
: : 9 value < value < value <

Hex. Code	The Home Computer transmits the ASCII sign for:	The rotator control interprets this as actuation of key:
x0	0	0
x1	1	1
x2	2	2
x3	3	3
x4	4	4
x5	5	5
x6	6	6
x7	7	7
x8	8	8
x9	9	9
xA	:	F1
xB	;	F2
xC	<	Q
xD	=	–

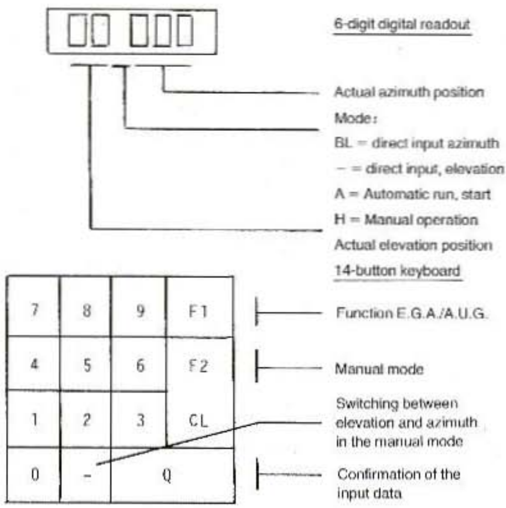


Fig. 14: Functions of readout and keyboard

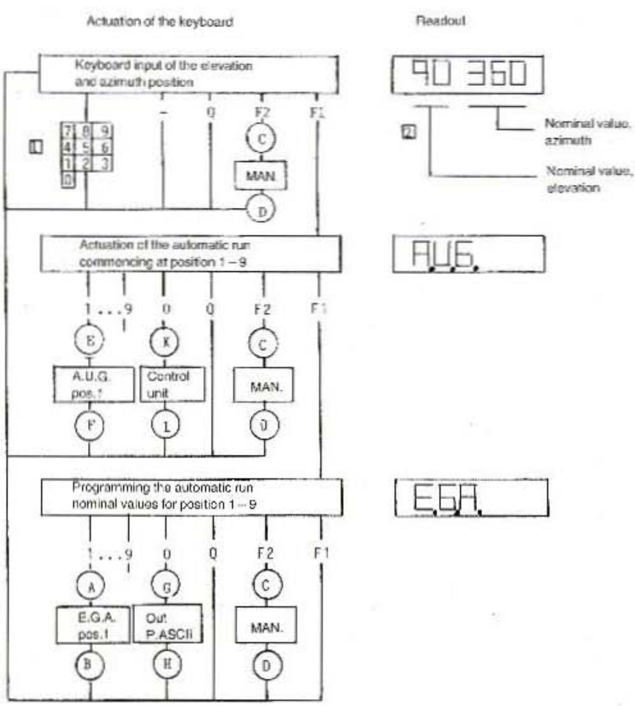


Fig. 15: Flow diagram

Example 2:

Commencement of a run from position 1, 2, or 9:

:1 <
:2 <
etc.
:9 <

2. OPERATING INSTRUCTIONS

Figure 14 shows the relationship between operations and pushbuttons, or readouts. The start and the programming of the run are assissted by a user control from the processor. A run comprises a maximum of nine positions with one azimuth, one elevation and one time value, each.

The numerical value to be inputed should be less than 360° in the azimuth plane and less than 180° in the elevation plane. In the case of the time plane, a maximum delay having a numerical value of 360 is permissible, which corresponds to a time period of 36 minutes.

If larger values are inserted, the remaining amount of the access is used as input.

Figure 15 shows the actuation of the keyboard, and associated readout on actuating the run.

1

If the keyboard is not actuated for a period of 6 seconds, the actual position of the rotators will be indicated on the readout until the keyboard is actuated again. Keyboard operation and the associated readout for the subprogram "Position Insert" is shown in **Figure 16**.

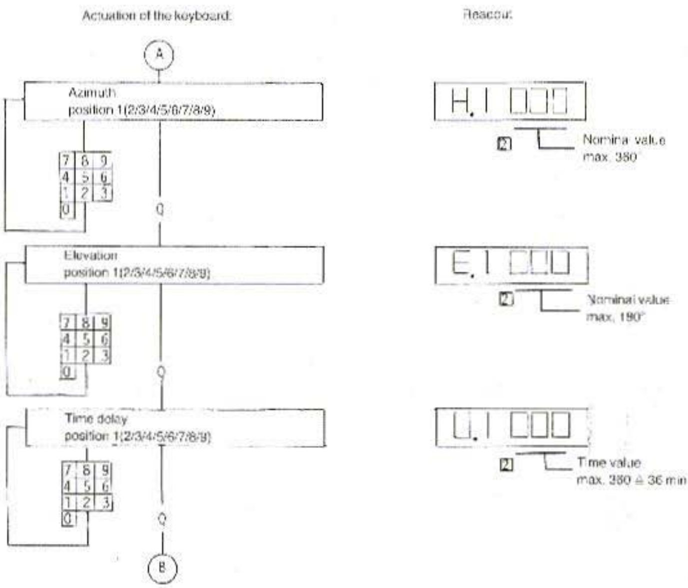


Fig. 16: The subprogram for inserting an antenna pointing angle

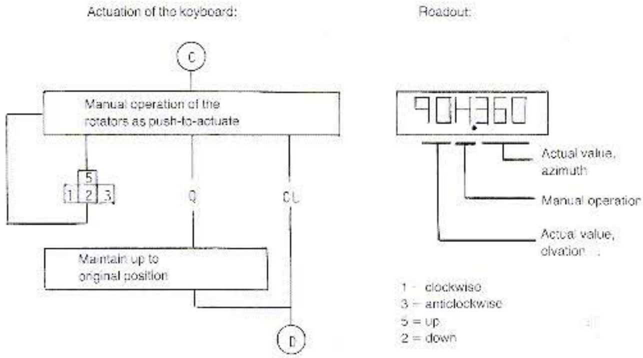


Fig. 17: Subprogram for manual pointing of the antenna

2

On re-entering, the old nominal value is shifted to the left. This means that it is necessary for the zeros to also be inserted when inserting nominal values of 1 or 2 digits.

Figures 17 and 18 describe the operation of the subprograms "Manual Positioning", or "Automatic Run", as well as finally the switching between operating unit/ASCII-port (see **Figure 19**).

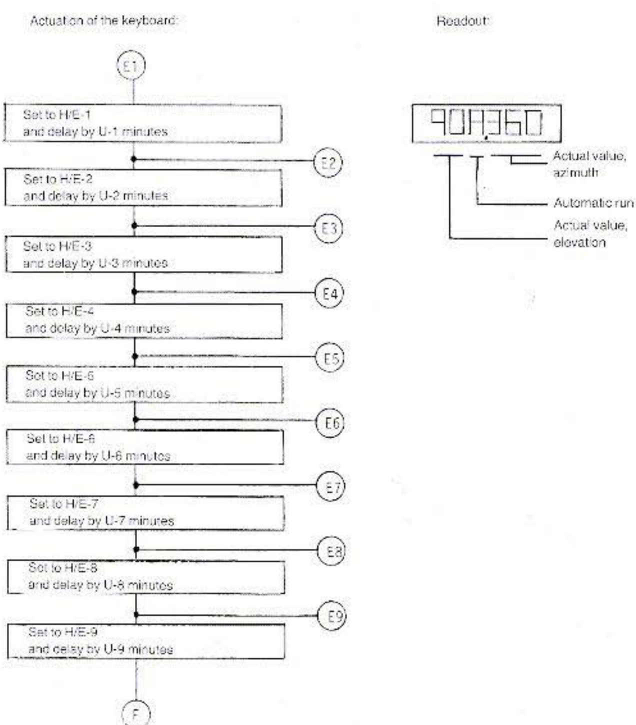


Fig. 18: Subprogram for an automatic run

Finally, the author is willing to provide a 16-page program listing and/or a completely programmed EPROM to interested readers at cost price.

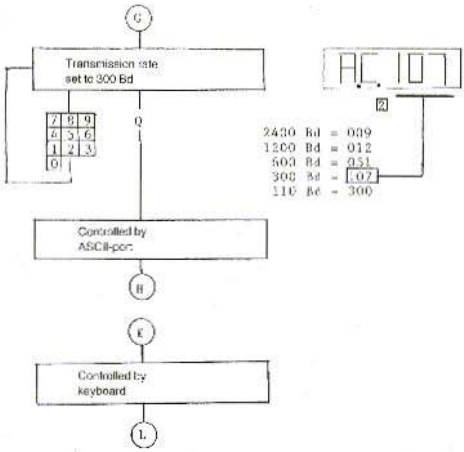


Fig. 19 Switching between control unit and ASCII-port

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Wolfgang Borschel, DK 2 DO

Diagrams that allow one to easily determine the Sensitivity of Receive Systems using Solar Noise

The following article is a follow-up on the previously published articles of Günter Hoch, DL 6 WU (1), and Dragoslav Dobričić, YU 1 AW (2).

It is now always possible to use a galactic noise source to determine the sensitivity of a receive system. Especially in the VHF/UHF range, one seldom has the required minimum antenna gain of 26 dB. This led the author to modify the method described in (1) to allow one to determine the sensivity (in other words the system noise temperature T_s), using noise level measurements of the sun together with the following diagrams.

1. THE SUN AS NOISE SOURCE

It is known that the characteristic of solar noise is that the noise flux increases towards higher frequencies, whereas (all ?) other cosmic noise sources exhibit the opposite behaviour. The sun represents a strong noise source due to its relatively low distance from the earth, however, its noise flux is not constant. Long-term, periodic variations exist over the eleven-year sunspot cycle; the mean values of these variations can be estimated relatively well. Short-term variations of the noise flux can be averaged by evaluating a number of measurements at different times. The following method is based on this principle.

2. MEASURING THE Y-VALUE

It is necessary to measure the Y-value before using the diagrams. The "hot-cold method" as described in (1) and (2) is suitable for this. The author measured the noise level at the output of the receiver (AGC-switched off) with the aid of a simple AF-voltmeter.

2.1. Determining the System Temperature T_s

As given in (1), the following is valid:

$$G/T = \frac{Y - 1}{I}$$

I = noise flux constant.

The system temperature of the receive system results as:

$$\frac{T_S}{K} = \frac{G_i}{G/T}$$

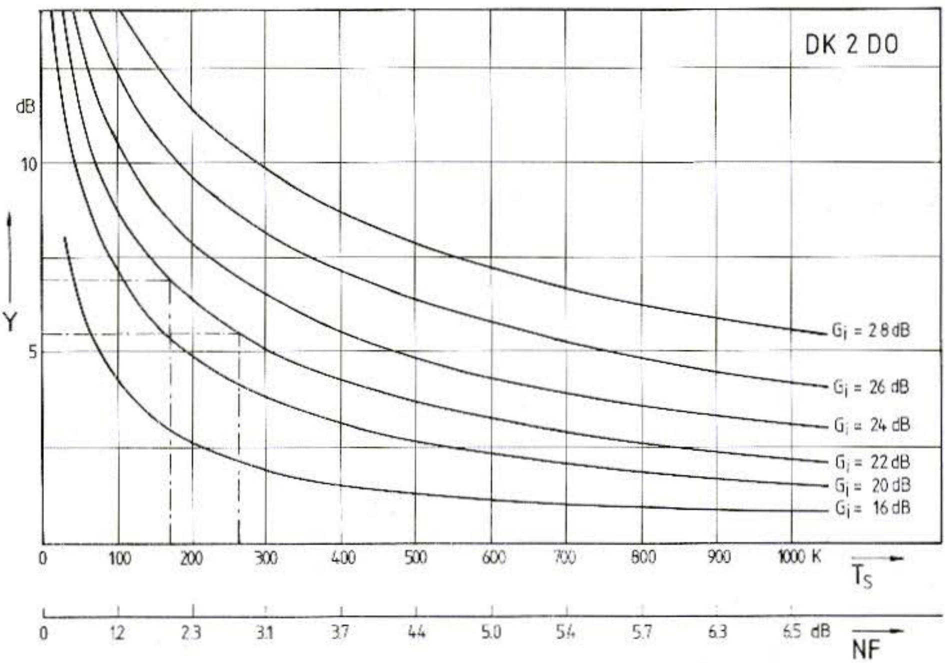


Fig. 1: System temperature T_s or noise figure (NF) of a receiving system determined from the measured Y-value with a known antenna gain G_i for a mean solar noise (flux at 432 MHz: 300 ≙ I = 4.17 K)

This means that:

$$\frac{T_S}{K} = \frac{G_i \times I}{Y-1}$$

whereby both Y and antenna gain G_i should be inserted as a factor. This dependence is given in **Figure 1**. Linear scales simplify the interpolation. In order to simplify the use of the diagram, the value Y is given on the vertical axis directly in dB.

One will obtain a new family of curves for each value of the noise flux constant I. Those given in Figure 1 are valid for a transition value between the two sunspot maximums. **Figure 2a** is valid for maximum sunspot activity, and **Figure 2b** for minimum. Since 1984 is a year of decreasing sunspot activity, Diagram 1 should be valid for the next few years.

3. EXAMPLE

The author measured a noise increase of between 5.5 and 6.9 dB at the output of the receiver (AGC-off) using a 70 cm antenna with a gain of G_i = 22 dB (array of four Longyagi antennas) together with an S 3030 preamplifier directly connected to the antenna. Further check measurements made with the aid of a calibrated attenuator resulted in virtually the same values.

From Figure 1, one can determine the following system temperatures matching these two Y-factors:

Y = 5.5 dB T_s = 265 K
Y = 6.9 dB T_s = 175 K

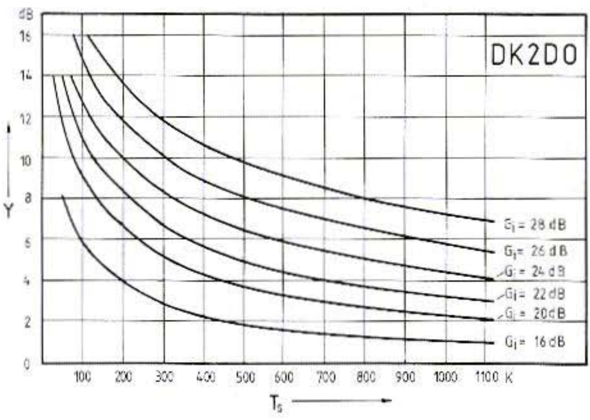


Fig. 2a:
As Fig. 1, but for maximum sunspot activity (flux at 432 MHz: 500 ≙ I = 6.95 K)

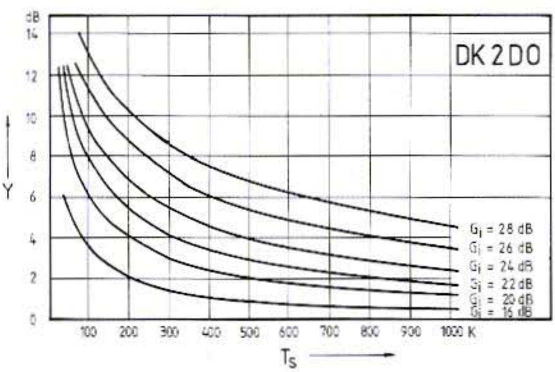


Fig. 2b:
As Fig. 1, but for minimum sunspot activity (flux at 432 MHz: 220 ≙ I = 3.06 K)

The mean arithmetic value of T_s = 220 K corresponds to the system temperature of the author's receiving system. This value would result in a noise increase of 8 dB with maximum sunspot activity (Diagram 2a), and to a value of 5.2 dB with minimum activity (Diagram 2b).

4. CHECKING THE RESULTS

The system temperature determined from Figure 1 was checked in a measuring sequence made in February 1983. The flux values S were obtained, and the solar noise level was measured with the author's receiving system at approximately 16.00 each day. The results of these measurements are given in **Table 1**.

The system temperature was calculated daily from the given solar flux and the measured Y-value. It will be seen that the values for the 4th and 8th of February do not conform to the average values. This is probably due to measuring errors, or irregular solar erruptions. The calculated system temperature values vary between 332 K and 167 K with a mean value of approximately 251 K. If we assume that this value is probably correct, it will be seen that a difference of approximately 15 % is present when comparing it to the values determined in Diagram 1. One must expect such tolerances when using the diagram. The author did not determine whether the family of curves is valid for all ranges.

Febr. 1983	Measured solar flux values from the observatory (1) $10^{-23}\frac{Ws}{m^2}$ (410 MHz)	Noise flux-constant (I) $I = \frac{S \cdot \lambda^2}{8 \pi k}$ [K]	Noise level measured with the author s system		$T_s = \frac{G_i \cdot I}{Y-1}$ [K]
			y [dB]	$Y = 10^{\frac{y}{10}}$	
1	–	–	–	–	–
2	550	7.54	–	–	–
3	370	5.07	6.0	3.98	260
4	600	8.23	6.2	4.16	412*
5	–	–	5.7	3.71	–
6	–	–	5.9	3.89	–
7	–	–	6.5	4.46	–
8	670	9.19	5.9	3.89	503*
9	530	7.27	6.5	4.46	332
10	390	5.35	5.6	3.63	322
11	400	5.49	6.2	4.16	275
12	–	–	5.8	3.80	–
13	310	4.25	6.5	4.46	194
14	290	3.98	5.8	3.80	225
15	300	4.11	6.5	4.46	188
16	300	4.11	5.8	3.80	232
17	290	3.98	5.5	3.54	248
18	300	4,11	6.9	4.89	167
19	320	4.39	6.6	4.57	194
20	320	4.39	6.2	4.16	220
21	300	4.11	6.8	4.78	172
22	320	4.39	5.7	3.71	256
23	320	4.39	6.2	4.16	220
24	310	4.25	6.3	4.26	206
25	350	4.80	6.9	4.89	195
26	340	4.66	6.3	4.26	226
27	410	5.62	5.9	3.89	308
28	310	4.25	5.9	3.89	173

Table 1: * Either a measuring error, or an irregular solar eruption
(1) AGL-Cambridge/Boston: Solar-Geophysical-Data NOAH (Col.) 80 303)303

5. REFERENCES

1) G. Hoch
Determining the Sensitivity of Receive Systems with the Aid of Solar Noise
VHF COMMUNICATIONS 12, Edition 2/1980, Pages 66–72

2) D. Dobričić:
Determining the Parameters of a Receive System in Conjunction with Cosmic Radio Sources
VHF COMMUNICATIONS 16, Ed. 1/1984, Pages 35–50

3) J. Reisert:
Requirements and Recommendations for 70 cm.ham radio magazine, June 1982

Terry Bittan, DJ Ø BQ/G 3 JVQ

Satellite News

FAILURE OF GOES-EAST

Unfortunately, GOES-East failed in orbit about the same time as VHF COMMUNICATIONS 3/1984 went to press. This means that only one of the three GOES satellites is actively able to procure images. For this reason, NOAA decided to shift GOES-West (GOES-6) from its normal position of 135°W to a position of 98°W which is able to provide better images of North, Central, and South America. The new location provides images as shown in **Figures 1 and 2**.

GOES-4 will take over the retransmission of WEFAX images transmitted usually via GOES-W. This satellite is located at 139°W, but is not able to provide image procurement.

Since GOES-6 was to be moved to a position near to that of GOES-Central (GOES-2), it was necessary to move the latter to a new parking position at 113°W.

After failure, several difficulties occured in the retransmission of GOES images via METEOSAT-2. However, such transmissions are now being made from Lannion, France.

METEOSAT Programme

ESA has published the following schedule of weather satellite launches:

METEOSAT 3 (P 2) will be launched in the second half of 1986 on the first test flight of Ariane 4. This satellite is very similar to METEOSAT 1 and 2.

This will be followed by a new generation of METEOSATs with improved image resolution. The launches will be as follows:
MOP 1 in 1987
MOP 2 in 1988
MOP 3 in 1990

Weather Charts via METEOSAT

Many of our readers will not have realized that the ESA transmits weather charts at regular intervals via Channel 2 (1691.0 MHz) of METEOSAT. These charts are provided by the German Weather Service (DWD) from their own and other sources. These prognostic (prog.) charts are as given in table 1.

We are to conclude our series on geostationary weather satellites with a description of the Japanese satellite GMS in one of the following editions of VHF COMMUNICATIONS.

Format	Trans. Time	Diss. Ch.	Content
WEFA 1	0346	2	EUR Prog. 200, 300 hPa for 1200 GMT
WEFA 2	0606	2	Prog. surface for 0000 GMT
WEFA 3	0806	2	Prog. 500 hPa Height, Temperature 24/48 hours for 0000 GMT
WEFA 4	1630	2	EUR Prog. 200, 300 hPa for 0000 GMT
WEFA 5	1930	2	Prog. surface for 1200 GMT
WEFA 6	2006	2	Prog. 500 hPa Height, Temperature, 24/48 hours for 1200 GMT

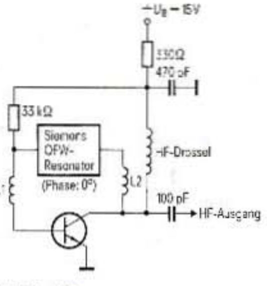
Table 1

BRIEFLY SPEAKING...

SAW Components

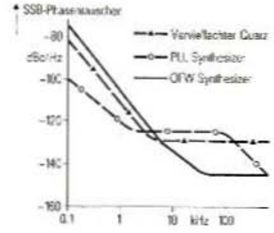
The first application of surface acoustic wave (SAW) components was for IF-filters for TV-receivers and converters in the 38 MHz range. In the meantime, it is possible using micro-structures on piezo-electric substrates to manufacture **precision filters in the frequency range from 10 MHz to over 1 GHz.** The advantages are that they are reproduceable, possess long-term stability and are very compact.

Modern **surface acoustic wave resonators** on quartz are excellent narrow-band filters in the frequency range of 200 to 1250 MHz. The excellent Q-values that are provided by



L1, L2: 3 ... 4 Wdg.

these SAW components are in the order of 8000! Their application is the resonant circuits of oscillators or narrow-band filters.



Abweichung von der Trägerfrequenz →

All electrical parameters have crystal-stable characteristics, in other words, possess a long-term stability and low temperature dependence. In contrast to conventional crystal-oscillator circuits using frequency multiplication, SAW resonators are excited at the fundamental frequency. This means that these compact oscillators have a higher spectral purity, and lower noise adjacent to the signal (≥ 10 kHz).

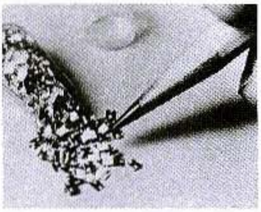
SIEMENS Technical Info No.B4-B3181-X-X-7600 (free of charge)

Chip Attenuators

The dimensions of the new thin-film attenuators of the TS 0500 series are only 1.9 x 1.5 mm^2 and possess 0.64 mm wide connections. They are suitable for operation up to 18 GHz. The attenuation values are between 1 dB and 20 dB with 3, 6 and 10 dB as standard values.

The compact dimensions of these components is only one of the important characteristics of these attenuators: They are accurate to ± 0.25 dB from DC to 18 GHz. In spite of their wide frequency range, they are good value for money.

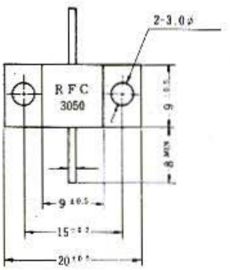
The attenuators can be used in a wide temperature range from − 55 °C to + 125 °C. In contrast to attenuators made up using three or more resistors, these compact components use one common resistance layer having identical thermal behaviour. This ensures exact tracking as a function of temperature and frequency.

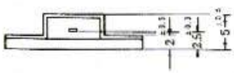


The chips meet or exceed the MIL-E-5400 and MIL-R-55342 specifications. In the frequency range from DC to 4 GHz, they exhibit an VSWR of 1.25 : 1, and 1.35 : 1 from 4 GHz to 8 GHz, and 1.5 : 1 from 8 GHz to 18 GHz. The maximum power dissipation is 0.1 W.
Manufacturer:
EMC TECHNOLOGY, Inc.
Cherry Hill, NJ., U.S.A.

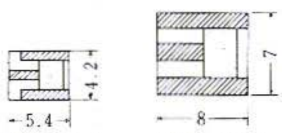
Metal-film resistors from DC to 1000 MHz

The NIKKOHM programme comprises radial, flat MF-resistors on a ceramic substrate (series RP); high-power MF-resistors up to 100 W (series RPL); MF-resistor networks (MP); RC-combinations on ceramic substrates (R-C); attenuators as T-pads for 50 Ω, 75 Ω, and 600 Ω for frequencies





up to 100 MHz (series T); chip attenuators for 50 Ω and 75 Ω from DC to 1000 MHz with 0.5 W rating (series RFA); chip terminating resistors for 50 Ω from DC to 4 GHz with a rating of 0.5 W (RFD-5450); VHF MF-resi-



RFD – 5450
5475

RFD – 8750
8775

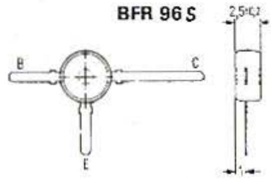
stors from 50 Ω to 2 kΩ with a rating of 10 W (RFD-424); UHF MF-resistors for 50 Ω with ratings of 30 W and 50 W from DC to 1000 MHz (RFC); and finally MF-chip resistors for hybrid circuits (RMC).

Manufacturer: NIKKOHM

BFR 96 S: For wideband amplifiers in the GHz-range

The Siemens BFR96S is a NPN-silicon, planar UHF transistor accommodated in a plastic case 50 B3 (DIN 41867), which is similar to TO-119. The application range is for wideband amplifiers of medium power levels up to the GHz-range. Since the linearity of this transistor is

BFR 96 S



much higher than the basic BFR 96, it is suitable for amateur-TV and SSB-amplifiers in the 70 cm and 23 cm bands.

Brief specifications:
Collector voltage: 15 V, collector current: 100 mA, power dissipation: 0.7 W, transit frequency: 5 GHz, power gain: 11.5 dB and output voltage at 800 MHz: 700 mV.

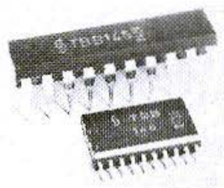
Weather Satellite Receiver DC3NT 003

In some cases self-oscillation in the 137 MHz stages occurs due to unsufficient grounding by the small printed lanes. The following measure will cure this problem: Form two small bridges 3 mm high, approx. 6 mm long made from (silver-plated) wire of at least 1 mm dia.. Solder them across the drain lanes of T 1 and T 2, resp. from ground to ground. That's all! DL3WR

PLL Frequency Synthesizer TBB146

Experience has shown that synthesizers are worthwile where more than five different frequencies are required. With the new Siemens TBB 146, it is possible for the frequency dividers to be set parallel or serial via the address and data line (7 bit), for instance, with the aid of a microcomputer.

The 10 mm² large CMOS chip has an upper frequency limit of 15 MHz, and only requires a quiescent current of 3.2 mA which also makes it suitable for battery operation.



The programmable TBB 146 offers division ratios of 3 to 4095, and the reference frequency can be divided by 1 to 127. Further features are an "anti-backlash" phase detector, and a lock detector to indicate when the PLL is locked-in. This CMOS-IC is compatiable to the MC 145 146 both in operation and pin connections, however, the maximum operating voltage is limited to 6 V, which is completely sufficient for use in conjunction with microprocessors. It is suitable for a large number of applications such as in AM/FM-radios, multichannel professional, amateur and CB communications and for radio navigation. Further ICs for PLL applications are a variable divider (S 89), a PLL (S 187) for 15 V, a programmable diode matrix (S 353) and three FM-receiver circuits (TBB 469/1469/2469).

MATERIAL PRICE LIST OF EQUIPMENT

described in edition 4/1984 of VHF COMMUNICATIONS

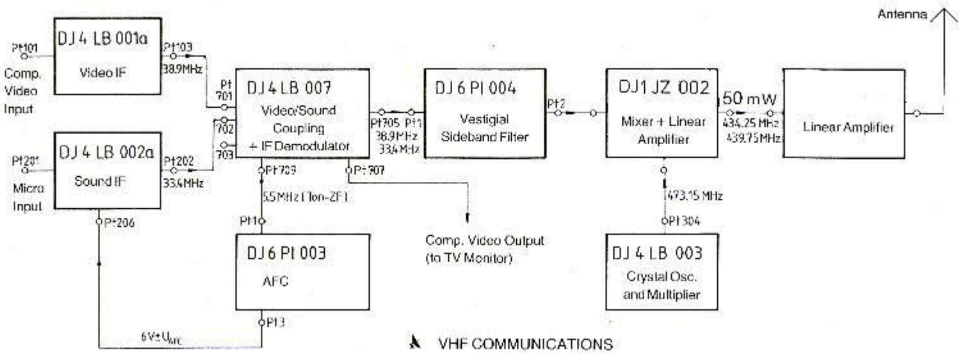
DJ3RV	**10 MHz Time-base with PLL for DCF77**		Art.No.	**Ed.**	**4/1984**
PC-board	DJ3RV 008	single-coated, silver-plated, drilled, with component location plan	6885	DM	34.–
Components	DJ3RV 008	5 transistors, 2 diodes, 3 CMOS- and 5 TTL-ICs, 1 Johanson air-spaced trimmer, 2 ceramic NPO and 19 other ceram. capacitors, 2 foil- and 2 feedthrough capacitors, 3 electrolytic caps., 23 resistors, 2 RF chokes, 5 PTFE feedthroughs, 1 tinned-metal box	6887	DM	160.–
TCXO	DJ3RV 008	10.0 MHz; 12 V DC; fine tuneable	6886	DM	443.–
Kit	**DJ3RV 008**	**complete, with above parts**	**6888**	**DM**	**595.–**
DC1BP	**PAL Colour Test-Image Generator**			**Ed.**	**4/1984**
PC-board	DC1BP 001	European Standard Size, with through-contacts	6889	DM	55.–
EPROM	DC1BP 001	programmed as described in the publication	6890	DM	44.–
Components	DC1BP 001	10 TTL ICs, 3 other ICs, 1 volt.regulator, 1 diode, 1 transistor, 1 DIL-switch, 1 connector pair 31-pole, 5 ceramic, 7 foil capacitors, 2 foil trimmers, 10 electrolytic caps., 1 potentiometer, 19 resistors	6899	DM	215.–
Crystal	2.5 MHz	matched to the ZNA234E	6898	DM	16.–
Crystal	4.433 MHz	PAL crystal	6163	DM	16.–
Kit	**DC1BP 001**	**complete, with above parts**	**6900**	**DM**	**335.–**

DF9EY	**Programmable Rotator Control**	**Ed. 4/1984**	
Single-board computer (without EPROM)		on request	
EPROM	already programmed	on request	
Program listing (16 pages)		DM	10.–

Following a frequent request, we are going to offer a limited number of PC-boards for the Digital Scan Converter, as described by YU3UMV in VHF COMMUNICATIONS editions 4/1982 and 1/1983. They should be available from March 1985 on and prices will be as follows:

PC-board YU3UMV 001, single coated, drilled, with component location plan		**DM 29.–**
PC-board YU3UMV 002, double coated, with through contacts		**DM 69.–**
Both PC-boards together	only	DM 95.–

An Amateur-Television Transmitter for Home Construction



A television transmitter built from modules described in VHF COMMUNICATIONS is shown in the above **block diagram**. Each function is realised on an individual PC-board. Each PC-board is built into its own tinned-metal box, which leads to a very clean operation without unwanted stray coupling and without problems caused by radiation. Each module may be aligned and tested on its own. All this encourages the home constructor since it makes it easy to understand the different functions, and it finally leads to a high-value ATV transmitter to which all possible video sources (black/white or color) may be connected.

For an amplification of the transmit power, a variety of linear amplifiers for the 70 cm band may be used (not FM »linears« !), whereby care should be taken to adjust the drive so that the output power does not exceed half the PEP value of the SSB mode.

The ATV modules listed have been published by three authors. The descriptions are detailed and will enable successful duplication. They are to be found in the following **editions of VHF COMMUNICATIONS:**

A system for Reception and Display of Weather-Satellite Images using a digital scan converter/storage module

A) A complete system as kits

Description	Edition	Kit designation	Art. No.	Price DM
Parabolic antenna, 1.1 m diameter, 12 segments to be screwed or riveted together, 3 plastic supports for radiator, mast-mounting parts with elevation mechanism	3/1979	**Set of 12 segments**	0098	**180.00**
		Riveting machine + rivets	0105	**93.00**
		1.7 GHz Cavity radiator kit	0091	**90.00**
		3 radiator supports	0106	**29.00**
		Mast-mounting parts	0107	**85.00**
Low-noise amplifier for 1.7 GHz	3/1984	**DJ6PI 012**	6867	**175.00**
METEOSAT Converter, consisting of two modules – Output first IF = 137.5 MHz)	4/1981	**DJ1JZ 003**	6705	**189.00**
	1/1982	**DJ1JZ 004**	6714	**185.00**
VHF Receiver, frequency range: 136 – 138 MHz, Output: 2400 Hz sub-carrier	4/1979	**DC3NT 003**	6141	**225.00**
	1/1980	**DC3NT 004**	6145	**80.00**
Digital scan converter (256 × 256 × 6 Bit)	4/1982 1/1983	**YU3UMV 001** **YU3UMV 002**	6736	**675.00**
PAL-Color module with VHF modulator	2/1983	**YU3UMV 003**	6739	**150.00**

B) Aligned ready-to-operate PCB-modules and equipment

Cavity radiator for above parabolic antenna	0092	**150,–**
VHF receiver for 136 – 138 MHz, DC3NT 003	6731	**395,–**
Oscillator for VHF receiver, DC3NT 004	6732	**168,–**
Digital scan converter (256 × 256 × 6 Bit) YU3UMV 001 + 002	6734	**1150,–**
PAL-Color module with VHF oscillator YU3UMV 003	6738	**285,–**

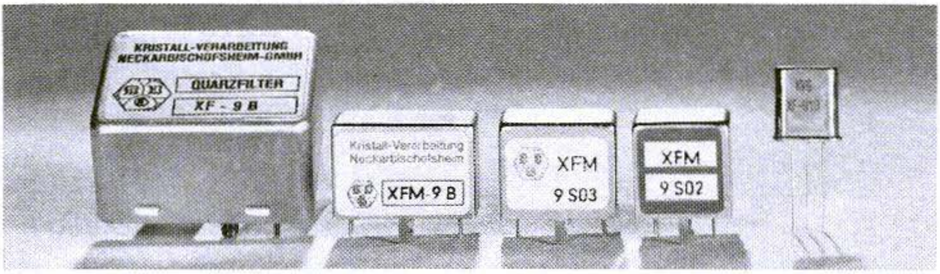
C) A complete system, ready-to-operate in cabinets

Parabolic antenna, 12 segments, riveting machine and rivets, cavity radiator, supports	0108	**510,–**
METEOSAT converter with GaAs-FET preamplifier and mixer, 2 channels, in casing	3026	**692,–**
Antenna for orbiting satellites, DJØBQ-137 (VHF COMMUNICATIONS 4/1981)	0101	**198,–**
Power combiner for above, AT-137	0306	**98,–**
6-channel VHF receiver in cabinet, programmed for: 137,130/137,300/137,400/137,500/137,620/137,850 MHz	3300	**1298,–**
Digital scan converter, 256 × 256 × 6 Bit, with control electronic **and PAL-Color module**/VHF oscillator in cabinet	6735	**1980,–**
Video monitor, black/white, with 31 cm C.R.T.	3301	**550,–**

All 10 editions of VHF COMMUNICATIONS containing information on weather satellite reception	6742	**49,–**
Dissemination Schedule of METEOSAT, incl. surface mail	005D	**3,–**
Audio Compact Cassette with 2 × 30 minutes of selected subcarrier recordings of METEOSAT and NOAA, resp.	6740	**25,80**

UKW**berichte** Terry D. Bittan · Jahnstr. 14 · Postfach 80 · D-8523 Baiersdorf
Tel. West Germany 9133-855. For Representatives see cover page 2

OUR GREATEST now with reduced dimensions !



Case: 1 15 14 13 17

DISCRETE CRYSTAL FILTER	Application	MONOLITHIC EQUIVALENT with impedance transformation			without impedance transformation		
		Type	Termination	Case	Type	Termination	Case
XF-9A	SSB	XFM-9A	500 Ω ‖ 30 pF	15	XFM-9S02	1.8 kΩ ‖ 3 pF	13
XF-9B	SSB	XFM-9B	500 Ω ‖ 30 pF	15	XFM-9S03	1.8 kΩ ‖ 3 pF	14
XF-9C	AM	XFM-9C	500 Ω ‖ 30 pF	15	XFM-9S04	2.7 kΩ ‖ 2 pF	14
XF-9D	AM	XFM-9D	500 Ω ‖ 30 pF	15	XFM-9S01	3.3 kΩ ‖ 2 pF	14
XF-9E	FM	XFM-9E	1.2 kΩ ‖ 30 pF	15	XFM-9S05	8.2 kΩ ‖ 0 pF	14
XF-9B01	LSB	XFM-9B01	500 Ω ‖ 30 pF	15	XFM-9S06	1.8 kΩ ‖ 3 pF	14
XF-9B02	USB	XFM-9B02	500 Ω ‖ 30 pF	15	XFM-9S07	1.8 kΩ ‖ 3 pF	14
XF-9B10*	SSB	—	—	–	XFM-9S08	1.8 kΩ ‖ 3 pF	15

*** New: 10-Pole SSB-filter, shape factor 60 dB : 6 dB 1.5**

Dual (monolithic twopole) **XF-910;** Bandwidth 15 kHz, R_T = 6 kΩ, Case 17
Matched dual pair (four pole) **XF-920;** Bandwidth 15 kHz, R_T = 6 kΩ, Case 2 x 17

DISCRIMINATOR DUALS (see VHF COMMUNICATIONS 1/1979, page 45)

for NBFM	**XF-909**	Peak separation 28 kHz
for FSK/RTTY	**XF-919**	Peak separation 2 kHz

CW-Filters – still in discrete technology:

Type	6 dB Bandwidth	Crystals	Shape-Factor	Termination	Case
XF-9M	500 Hz	4	60 dB : 6 dB 4.4	500 Ω ‖ 30 pF	2
XF-9NB	500 Hz	8	60 dB : 6 dB 2.2	500 Ω ‖ 30 pF	1
XF-9P*	250 Hz	8	60 dB : 6 dB 2.2	500 Ω ‖ 30 pF	1

*** New !**

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