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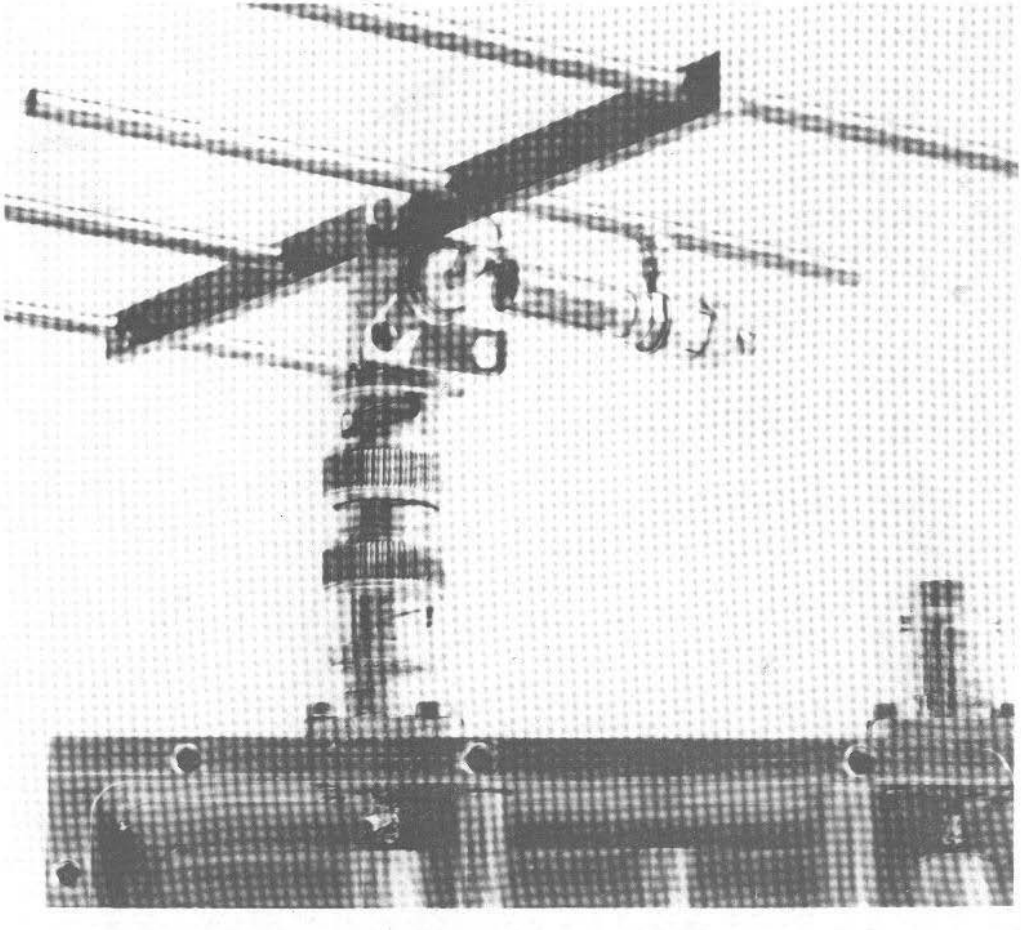

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A 4 ELEMENT YAGI ANTENNA FOR 23 cm

by H. W. Binder, DC 8 XB

The described antenna is, of course, not suitable for earth-moon-earth (EME) or other long distance communications. However, the handy 4-element antenna, which is shown in Figure 1 in true scale is very useful for experiments (e. g. with the 23 cm converter of (1), for demonstration purposes and for local contacts. The antenna is 119.5 mm long which approximately corresponds to a half wave length. According to (2) the maximum gain is approximately 6 dB, referred to a $\lambda/2$ dipole.

The 4-element Yagi antenna for 23 cm is an all-metal construction. The boom is a 129.5 mm long rectangular brass rod of 3 mm x 6 mm. The elements are made from round brass rods of 3 mm diameter. The boom is provided with four 3 mm holes for the elements as well as with a slot for the flange of the angled BNC connector. The boom, the four elements and the socket are soldered together, preferably using hard solder. A ceramic trimmer capacitor (tubular trimmer 4.5 pF (e. g. Philips 2222 802 96067), connects the inner conductor of the socket with the radiator element. The constructional diagram in Figure 1 and the enlarged photograph in Figure 2 show this arrangement which, in principle, represents a gamma match. The trimmer is soldered 28 mm from the end of the radiating element and is adjusted for maximum reading on a field strength meter or for minimum standing wave ratio on a reflectometer.

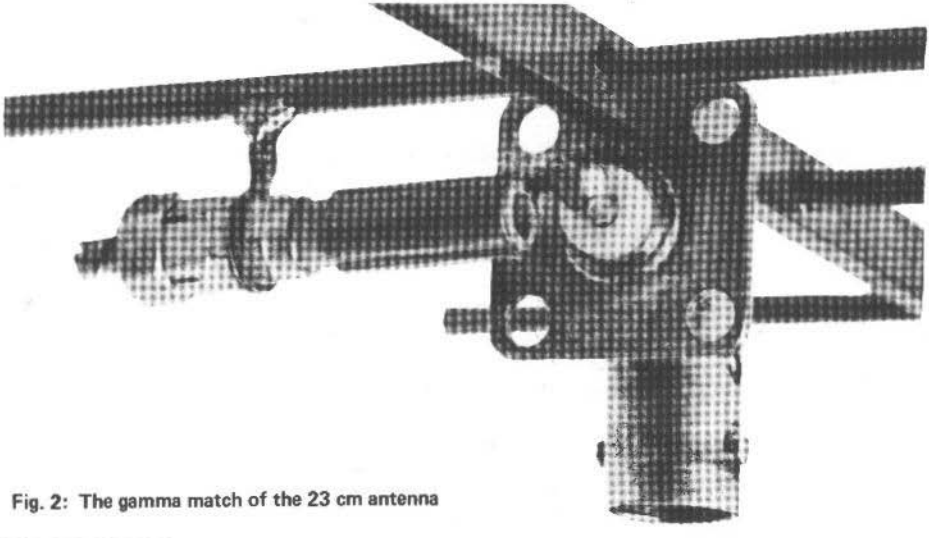

Fig. 2: The gamma match of the 23 cm antenna

REFERENCES

(1) L. Wagner and H. W. Binder: A 23 cm Converter with hot-carrier diode mixer
In this edition of VHF COMMUNICATIONS

(2) K. Rothammel/Antennenbuch
Deutscher Militärverlag Berlin, 7th edition, Page 333
Telekosmos Verlag Stuttgart, 3rd edition, Page 270

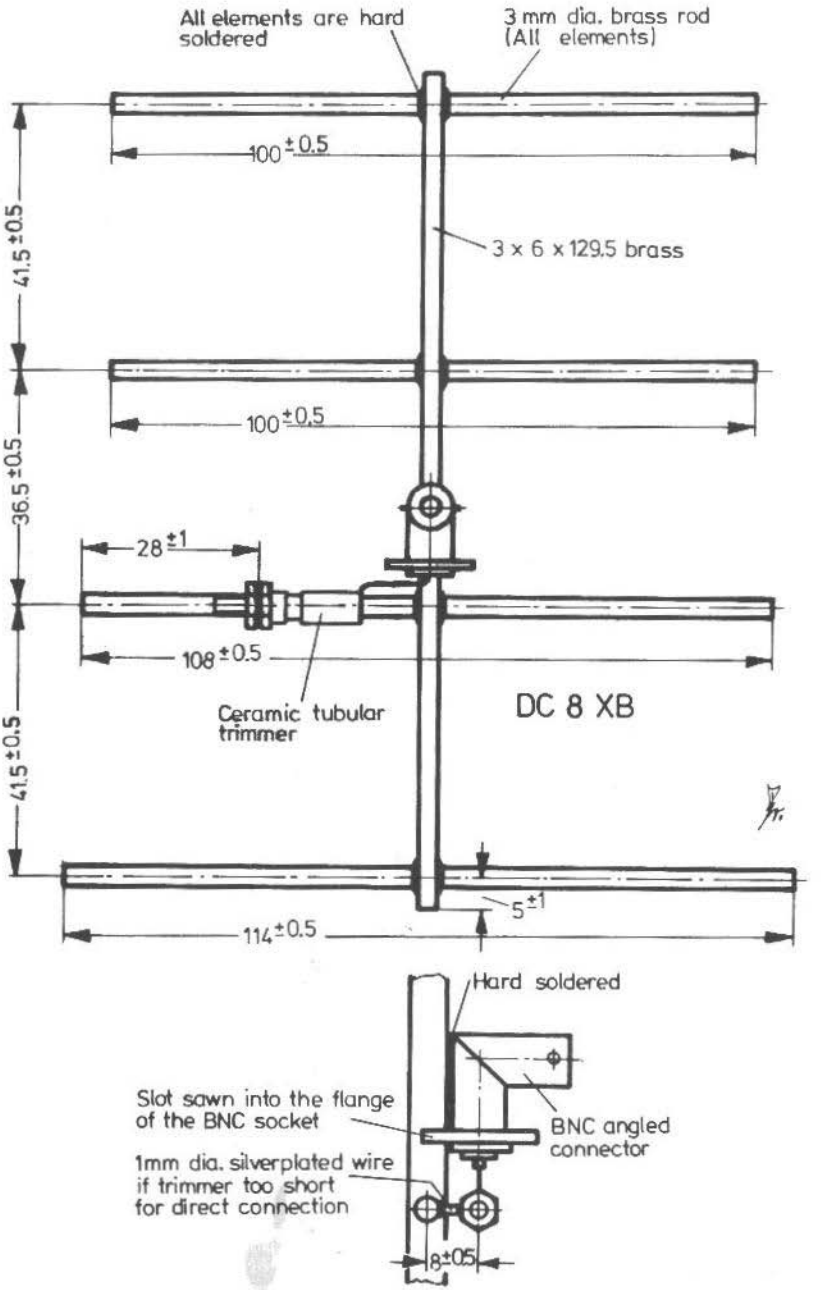

Fig. 1: Dimensions of the 4 element Yagi antenna for 23 cm

A 23 cm CONVERTER WITH HOT-CARRIER DIODE MIXER

by L. Wagner, DL 9 JU and H. W. Binder, DC 8 XB

INTRODUCTION

The following 23 cm converter is equipped with a hot-carrier diode in the input mixer and with silicon transistors in the oscillator and IF-preamplifier. The frequency range of 1296 to 1298 MHz is converted to an intermediate frequency of 144 to 146 MHz. The current requirements are approximately 35 mA at 12 V. The mechanical construction is extremely simple; it is only necessary for the single-coated PC-board material to be cut to size, several holes to be drilled and for a certain amount of soldering to be made. The intermediate frequency in the 2 m band and the weight of only 200 g make this converter extremely suitable for portable operation, e.g. during field days. Figure 1 shows a photograph of the converter.

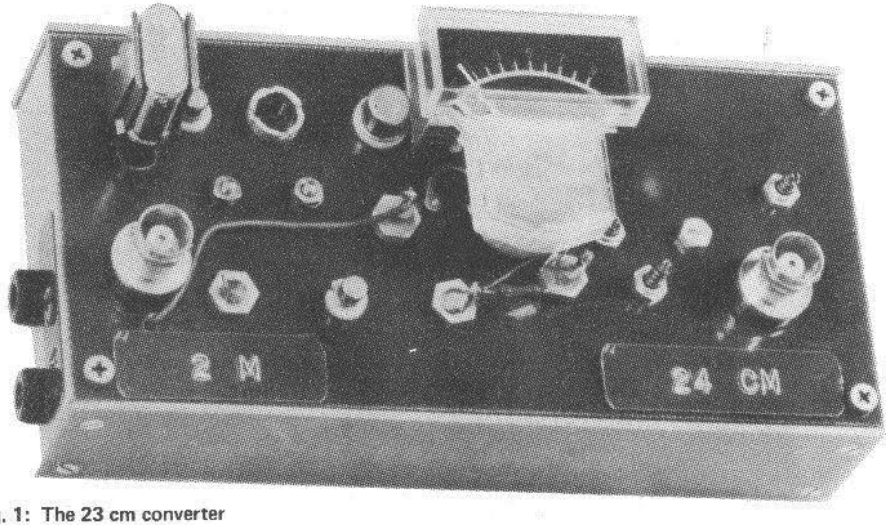

Fig. 1: The 23 cm converter

1. CIRCUIT DESCRIPTION

The converter, whose circuit is shown in Figure 2, consists of three main sections: the oscillator, the UHF portion and the IF-preamplifier.

1.1. OSCILLATOR PORTION

Two different methods can be used to obtain the required frequency processing. Either: 57.6 MHz x 5 = 288 MHz x 4 = 1152 MHz, or: 96.0 MHz x 3 = 288 MHz x 4 = 1152 MHz. Inductance L 1, capacitor C 3 and the input capacitance of transistor T 2 form a resonant circuit for the oscillator frequency of the overtone crystal oscillator equipped with transistor T 1. The resonant circuit comprising inductance L 2 and trimmer C 5 at the collector of the frequency multiplier transistor T 2 is aligned to 288 MHz. Since the subsequent varactor multiplier possesses a very low efficiency, an efficient transistor type must be used for T 2.

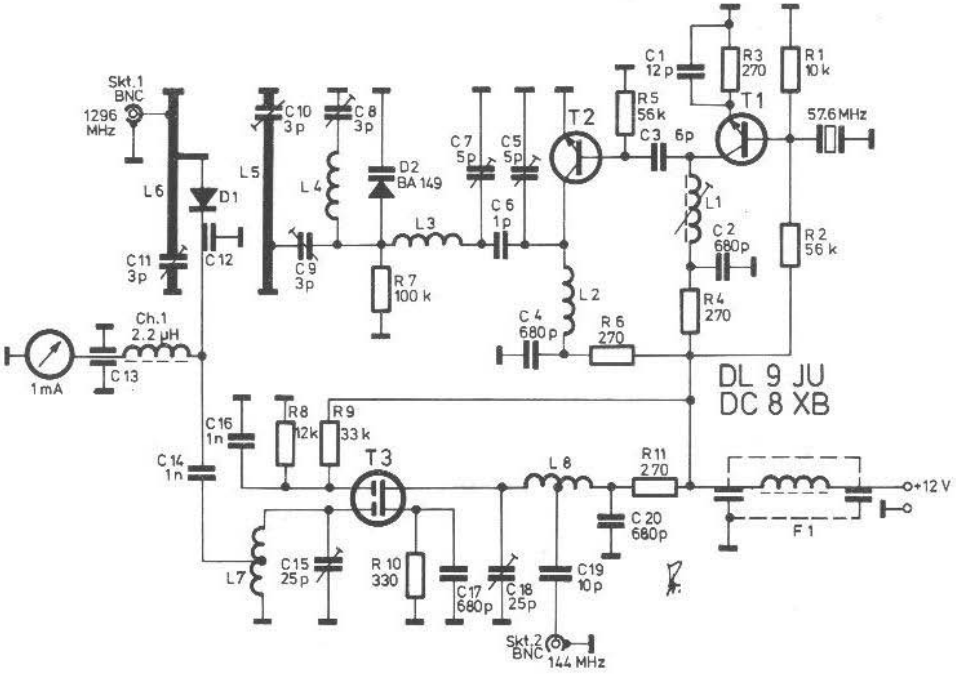

Fig. 2: Circuit of the 1296/144 MHz converter

The varactor diode D 2 receives the 288 MHz drive via a matching network comprising capacitors C 6 and C 7 and inductance L 3 which is also aligned to 288 MHz. The resonant circuit for the multiplied frequency of 1152 MHz comprises a $\lambda/4$ stripline circuit (L 5) shortened with the trimmer capacitor C 10. The varactor diode is coupled to this circuit via trimmer capacitor C 9.

An idler circuit for twice the input frequency (576 MHz) comprising inductance L 4 and trimmer capacitor C 8, as well as resistor R 7 for generation of the bias voltage for the varactor diode, complete the frequency multiplier circuit.

1.2. UHF-PORTION

The stripline circuit L 6, which is shortened with trimmer capacitor C 11, is resonant at the input frequency of 1297 MHz. The input signal is galvanically coupled at low impedance from the antenna socket Pt 1. The mixer diode D 1 is connected to a somewhat high impedance position on the input circuit. The local oscillator frequency of 1152 MHz is inductively coupled on to the coupling link formed by the connection piece and the diode itself. The intermediate frequency voltage is fed via capacitor C 12 to the IF-preamplifier whereas the residual UHF voltages are shorted by C 12. Capacitor C 12 is home-made, and has a capacitance of approximately 10 pF. A meter is provided for indicating the diode current. The full scale deflection is 1 mA. It is connected via choke Ch 1 to the IF line.

A hot-carrier diode type TIXV 305 of Texas Instruments is used as mixer diode. This diode receives so much power from the oscillator circuit that a direct current of between 0.5 and 1 mA will be indicated. Hot-carrier diodes (1), or Schottky barrier diodes as they are sometimes called, possess a metal-semiconductor junction, which makes it virtually impossible for any charge carrier storage to take place, instead of the normal PN junction of normal semiconductor diodes. This mainly results in extremely short switching times. In addition to this, these diodes can handle approximately ten times the input power as the previously used point contact-diodes, of which types 1 N 21 and 1 N 23 are best known. Since only majority carriers are responsible for the conductivity in hot-carrier diodes, their intrinsic noise is somewhat less than that of point contact-diodes. For frequencies in the order of 1300 MHz, the difference is not too important. The converter can therefore also be used with a mixer diode of the 1 N 21 series if the holder is correspondingly altered.

1.3. IF-PREAMPLIFIER

In order to obtain a low noise figure without neutralization, a dual-gate MOSFET is used in the IF-preamplifier. Gate 1 is connected to a resonant circuit comprising L 7 and C 15 which is aligned to 145 MHz. This resonant circuit receives the intermediate frequency from a low-impedance tap on the resonant circuit. Gate 2 is connected to a fixed bias voltage. A 145 MHz resonant circuit is also connected to the drain electrode. This resonant circuit comprises inductance L 8 and trimmer capacitor C 18. The output socket Pt 2 (BNC) is connected to a tap on this resonant circuit.

2. CONSTRUCTION

An idea of the construction is given in the photograph shown in Figure 3. Base plate and side walls are made out of 1.5 mm thick, single-coated epoxy PC-board material. After the base board has been provided with the holes shown in Figure 4, the four side pieces are soldered to the base board. It is also necessary for the corners to be soldered. The cover is later screwed on to four tapped bushings that are screwed to the base plate.

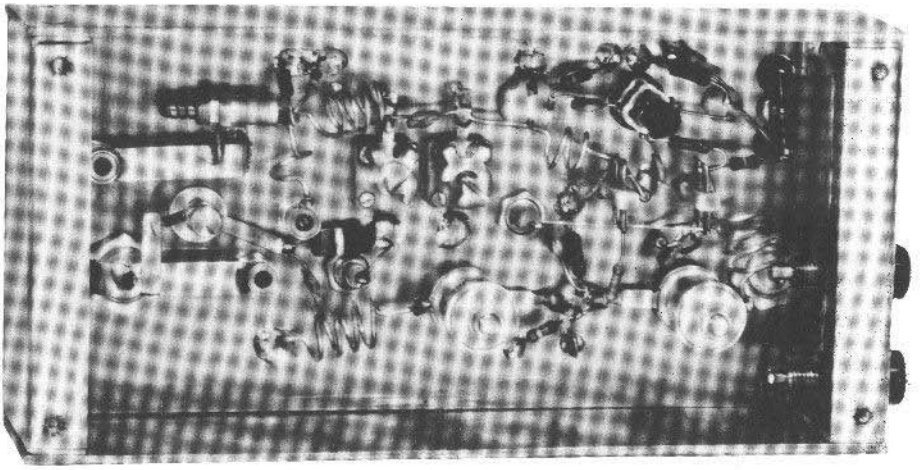

Fig. 3: The converter as seen from below

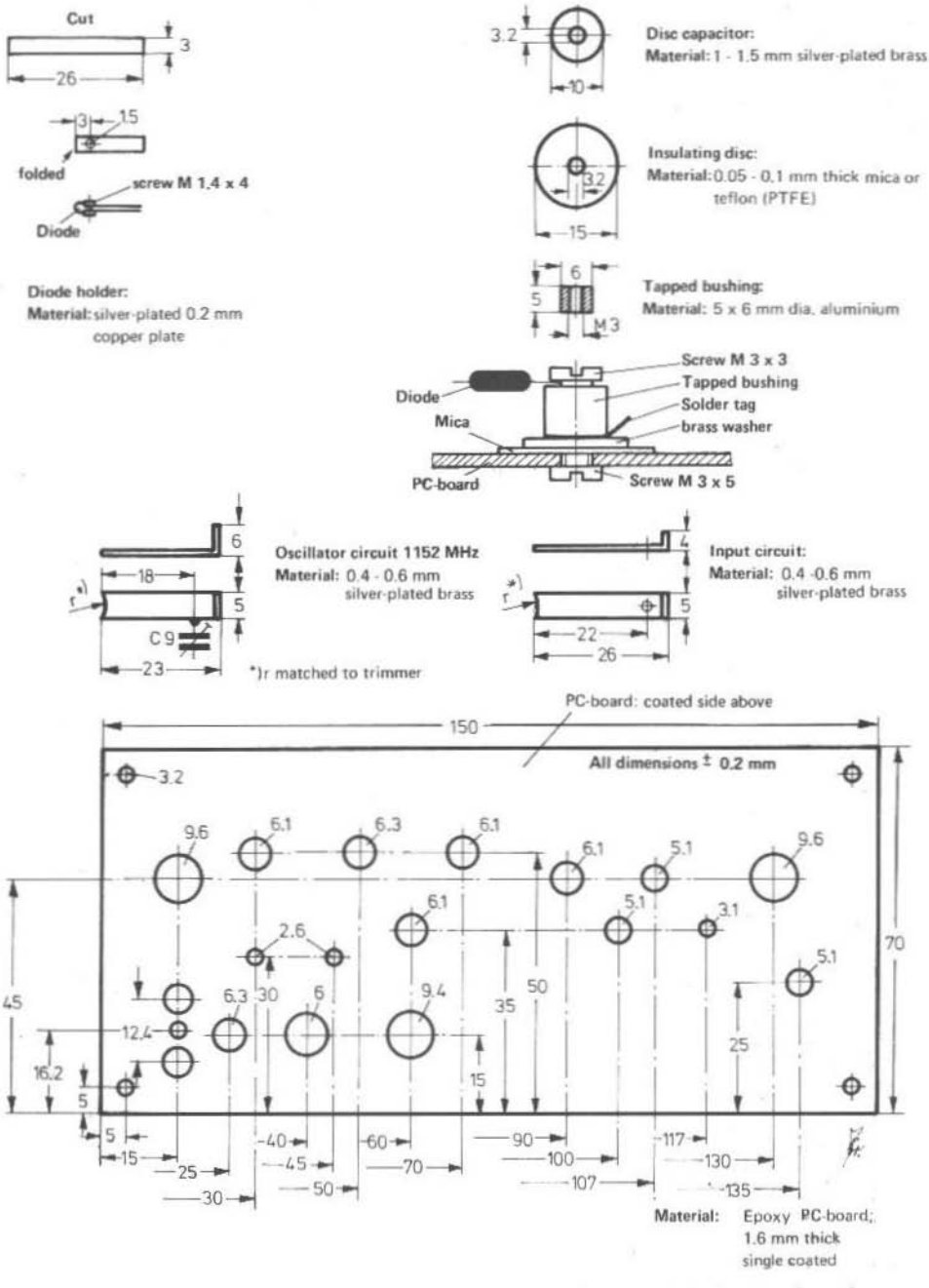

Fig. 4: Dimensions of base plate, stripline circuits and diode holder

After this, the stripline circuits given in Figure 4 are cut. They are provided with a slight rounding at the flat end which is soldered to the stator coating of trimmer capacitors C 10 and C 11. The (somewhat longer) input circuit is also provided with a hole for the inner conductor of the BNC input socket. The two mentioned trimmer capacitors and the input socket are now mounted. The BNC socket is provided with a 4 mm thick intermediate spacing ring on the top of the chassis which can be made of any material. Since sockets are used for single-hole mounting, the ground connection is made via the nut on the coated side of the board. Due to the intermediate ring, the thread of the socket does not protrude beyond the nut.

The input stripline circuit is placed with its hole on the inner conductor of the input socket to which it is soldered. The rounded end is soldered to trimmer capacitor C 11 and the bent end to the nut of the BNC-socket. The 1152 MHz circuit is soldered in the same manner to trimmer capacitor C 10 and to the ground surface (copper coating.).

A 3 mm wide, thin metal strip is used for mounting the diode which is in a glass case with wire connections. The metal strip is folded and the loop formed in this manner clamps one connection of the diode directly adjacent to the glass body. The two ends of the metal strip are soldered to the input circuit 14 mm from the trimmer capacitor. Previous to bending, the metal strip, which is also given in Figure 4, is 26 mm long. The other end of the diode is clamped under the screw of the home-made disc capacitor C 12 also directly adjacent to the glass body. This capacitor (C 12) consists of a metal disc of approximately 10 mm diameter which is fixed to the ground surface by a central screw with an intermediate dielectric formed by a 0.1 mm mica disc (or 0.05 mm of teflon/PTFE). This screw must not come into contact with the ground surface. The copper coating is therefore removed for a greater diameter than that of the screw. The coupling capacitor C 14 and choke Ch 1 can be soldered later to the provided soldering tag. Following this, all transistor sockets, IF output socket (BNC), meter, crystal holder and all other components are mounted. The photographs provide further information as to the construction. Finally, the converter is wired according to the wiring diagram given in Figure 5. Instead of the feedthrough filter F 1, two bypass capacitors of 470 pF each and a ferrite wideband choke or several ferrite beads can be used.

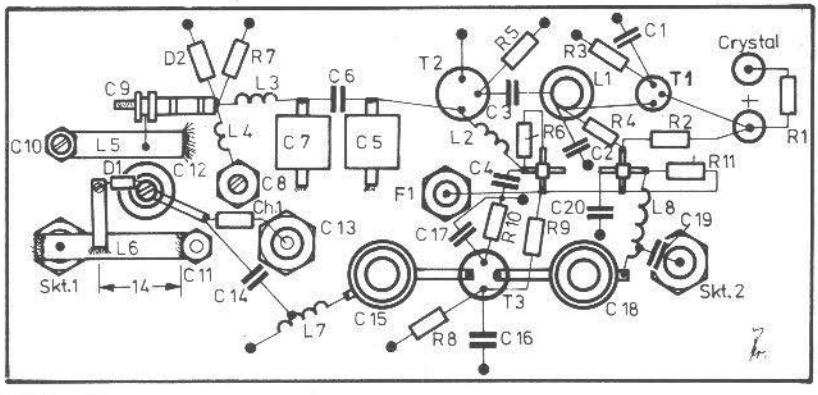

Fig. 5: Wiring diagram

2.1. COMPONENTS

T 1: BF 224 (Texas Instruments Germany)
T 2: 2 N 3866
T 3: 3 N 140 or 40673 or 3 N 187 (RCA)

D 1: TIXV 305 (TI), HP 5082-2817 (Hewlett-Packard)
D 2: BA 149 (AEG-Telefunken) varactor C_T = 6 pF at U_R = 2 V, 1 N 5461 A

L 1: 9 turns of 0.3 mm dia (29 AWG) enamelled copper wire, close wound onto a 6 mm coil former with VHF core. (For 96 MHz crystal: 5 turns)

All other inductances are self-supporting and made from 1 mm dia (18 AWG) silver-plated copper wire.

L 2: 2 turns on a 7 mm former, coil length 6 mm
L 3: 4 turns on a 6 mm former, coil length 12 mm
L 4: 1 turn on a 7 mm former, coil length 8 mm
L 5, L 6: Stripline circuits according to Figure 4
L 7: 4 turns on a 8 mm former, coil length 12 mm, coil tap 1 turn from ground
L 8: 4 turns on 8 mm former, coil length 12 mm, coil tap 1.5 turns from drain end

Ch 1: approx. 2.2 µH, ferrite wideband choke (Delevan)

F 1: Feed-through filter (AEG-Tfk) or as mentioned in the text

C 5, C 7: 1.7 - 6 pF air-spaced trimmers for screw mounting
C 8 - C 11: 0.7 - 3.7 pF ceramic tubular trimmers
(Philips 2222 801 20 005 or 2222 802 20 001)
or 0.8 - 6.8 pF (Philips 2222 801 20 006 or 2222 802 20 002)
C 15, C 18: 3 - 30 pF air-spaced trimmer (Philips 2222 803 20 001)

3. ALIGNMENT

Transistor T 3 is not inserted for the preliminary alignment. The operating voltage is fed to the converter via a mA-meter. A sensitive mA-meter (100 µA) is connected in series with resistor R 7 and transistors T 1 and T 2 are inserted into their sockets.

If the crystal oscillator is not oscillating, a total current of approximately 5 mA will be indicated. The crystal oscillator is then brought into oscillation by trimming the core of inductance L 1. The total current will then rise to approximately 30 to 40 mA. The crystal frequency should be checked, especially when using the crystal frequency of 96 MHz, because it is possible that another harmonic has been aligned. Besides the use of a dip-meter, the 96 MHz signal can be monitored in the FM range of a broadcast receiver.

Next, the 288 MHz circuit should be aligned with trimmer capacitor C 5 and the matching to the varactor diode carried out with trimmer capacitor C 7 for maximum current via resistor R 7 and the µA-meter. When using a 57.6 MHz crystal, it is possible that the fourth harmonic (230.4 MHz) instead of the fifth harmonic is selected. For this reason the frequency should be checked at inductance L 3 with the aid of a dip-meter or Lecher-line. After this, the µA-meter in series with R 7 can be removed.

The μA-meter is now temporarily connected instead of the built-in 1 mA-meter. The trimmer capacitor is adjusted to approximately half its capacitance and the more sensitive meter is brought to full scale deflection by aligning the Idler and 1152 MHz circuit with capacitor C 8 or C 10. After this, the built-in meter is reconnected and the alignment carefully corrected. Since the circuits interact, it is necessary for the alignment to be repeated several times using trimmer capacitors C 5, C 7, C 8 and C 10. The diode current should then be between 0.5 and 1 mA.

If necessary, the capacitance of trimmer capacitor C 9 can be altered in steps after which the alignment is corrected.

The crystal is removed from its holder for the alignment of the IF preamplifier. A 2 m receiver is connected to the output socket and transistor T 3 is inserted into its socket. In order to ensure that the MOSFET is not endangered by static charges, the shorting spring around the connection wires should not be removed until the transistor has been inserted into its socket. The disc capacitor C 12 is now temporarily connected to a 2 m antenna and the 2 m receiver tuned to a signal of approximately 145 MHz. The input and output circuits of the IF-preamplifier are aligned for maximum field strength indication by aligning trimmer capacitors C 15 and C 18. After this, the antenna can be removed and the crystal reinserted into its holder.

Finally, it is necessary for the 1297 MHz input circuit to be aligned. To do this, a 23 cm antenna should be connected and the subsequent receiver tuned to a signal. The harmonics of a 2 m or 70 cm transmitter or the calibration spectrum generator described in (2) can be used as signal source. It is only necessary for trimmer C 11 to be aligned for maximum field strength as indicated on the S-meter.

4. EXPERIENCE

The described converter has been used in the Munich area and constructed by a number of amateurs. B. Helmke, DL 7 HR was awarded the first prize of the 23 cm stations during the Bavarian Mountain Field Day in 1969. Using this converter, he was able to operate a 23 cm contact over a distance of 230 km.

The converter was measured under laboratory conditions by H. -W. Binder, DC 8 XB, and was found to have a noise figure of 8 dB.

5. AVAILABLE PARTS

Various components for the described 23 cm converter are available from the publishers or their national representatives. Please see advertising page.

6. REFERENCES

(1) Hewlett-Packard Application Note AN 907: The Hot Carrier Diode: Theory, Design and Application

(2) K. Eichel: A Simple VHF-UHF Calibration-Spectrum Generator VHF COMMUNICATIONS 2 (1970), Edition 4, Pages 240-243

INTERDIGITAL BANDPASS FILTER FOR 23 cm

by H. J. Franke, DK 1 PN and R. Griek, DK 2 VF

1. INTRODUCTION

Interdigital filters are not too well known to radio amateurs. Interdigital comes from the latin and means "intermediate finger". Such filters usually consist of $\lambda/4$, coupled resonant line circuits whereby the shorted end of one $\lambda/4$ circuit is near the non-loaded end of the next circuit. Passband frequency, coupling and the Q of the circuits and the resulting passband curve are dependent on the mechanical dimensions.

The advantage of interdigital filters over coaxial filters is that they are more easily constructed and require little or no alignment. In spite of this, the good characteristics of these filters such as low passband attenuation and high attenuation outside of the passband can be reproduced without problems after construction. The main reasons for this are that striplines are used which have a predictable behaviour. Prerequisite is, however, that the stripline circuits of the filter are correctly dimensioned with modern calculation methods. This is hardly possible for the amateur and must be left to experts (1) and (2).

2. DESCRIPTION

The described filter possesses three stripline circuits. The arrangement of the circuits, which remind one of interlaced fingers, can be seen clearly in the photograph given in Figure 1. The two (thicker) outer lines are connected to input and output sockets and are used for input and output coupling. The striplines of this filter are round and therefore do not really coincide with the designation. However, one always talks of striplines when the field is concentrated to the spacing between the lines (which are mostly flat) and one, or sometimes even two neighbouring ground surfaces. This is clearly a contrast to coaxial circuits where the field is more or less homogeneously distributed around the inner conductor because it is enclosed by a round or square outer conductor. The described filter is provided with a well-conducting cover which means that the resonant line circuits possess two ground surfaces.

A similar filter and a four-circuit filter for 70 cm were described in (3). In this publication, the narrow sides remained open. However, the base plate, cover and longitudinal walls were extended past the coupling conductors, so that no radiation losses could occur.

3. CONSTRUCTION

Two such filters were constructed by H. J. Franke, DK 1 PN. In order to make the filter completely screened and waterproof (Field Day), the narrow sides of the described filter are closed. The casing is longer than described in (3) so that the coupling lines are not affected by the narrow-side walls.

Figure 2 shows all constructional details of the filter. The case of the filter shown in Figure 1 has been milled from an aluminum block. Normally, the 5 mm thick side, base and cover plates are individually made from metal plate and screwed together. Of course, attention must be paid that a good electrical contact exists between the longitudinal walls and the covers so that the RF currents can flow from cover to cover (e.g. from ground to ground).

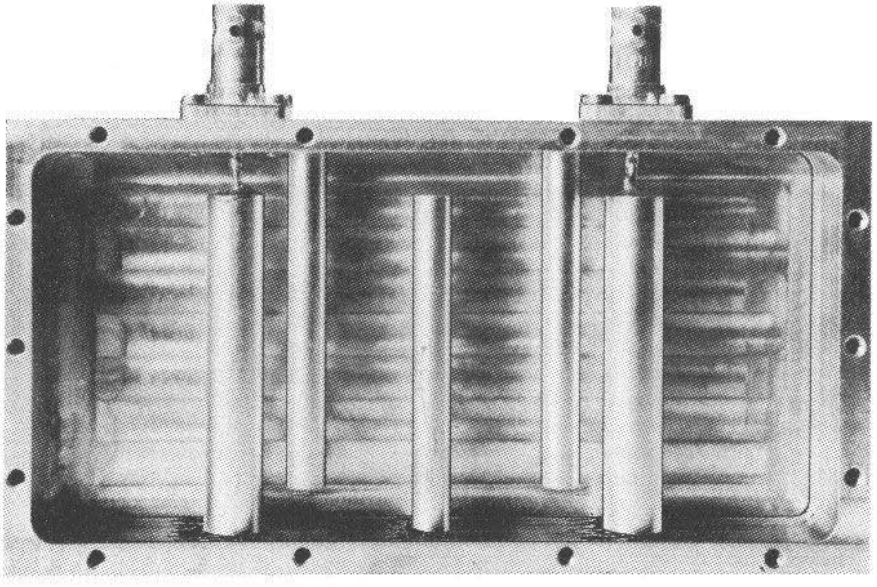

Fig. 1: Three-circuit interdigital filter for 23 cm

The inner conductor diameters are 3/8" and 1/4". If such metal rods are not available it is necessary for them to be made on a lathe. They should be silver-plated, whereas the casing can consist of aluminum. Both BNC or type N sockets can be used. The inner conductors of theBNC sockets just do not reach to the coupling lines which means that a short piece of copper foil of a few millimeter in width must be soldered between them.

4. MEASURED VALUES

The passband curves of two different filter arrangements are shown in Fig. 3. The measurements were made by R. Griek, DK 2 VF. The wider passband curve with the passband sag due to the over-critical coupling was measured in conjunction with a filter that M. Münich, DJ 1 CR made from the original description (3). The narrower passband curve was measured with the filter given in Figure 1. The differences are, as long as only the narrow portion of the 23 cm band is used between 1296 and 1298 MHz, not important. The insertion loss of both filters only amounts to approximately 0.5 dB.

Further examinations by R. Griek have shown that the shape of the passband curve and the value of the insertion loss at the centre frequency remain intact under non-load conditions or with a short-circuit behind an attenuation pad of at least 6 dB.

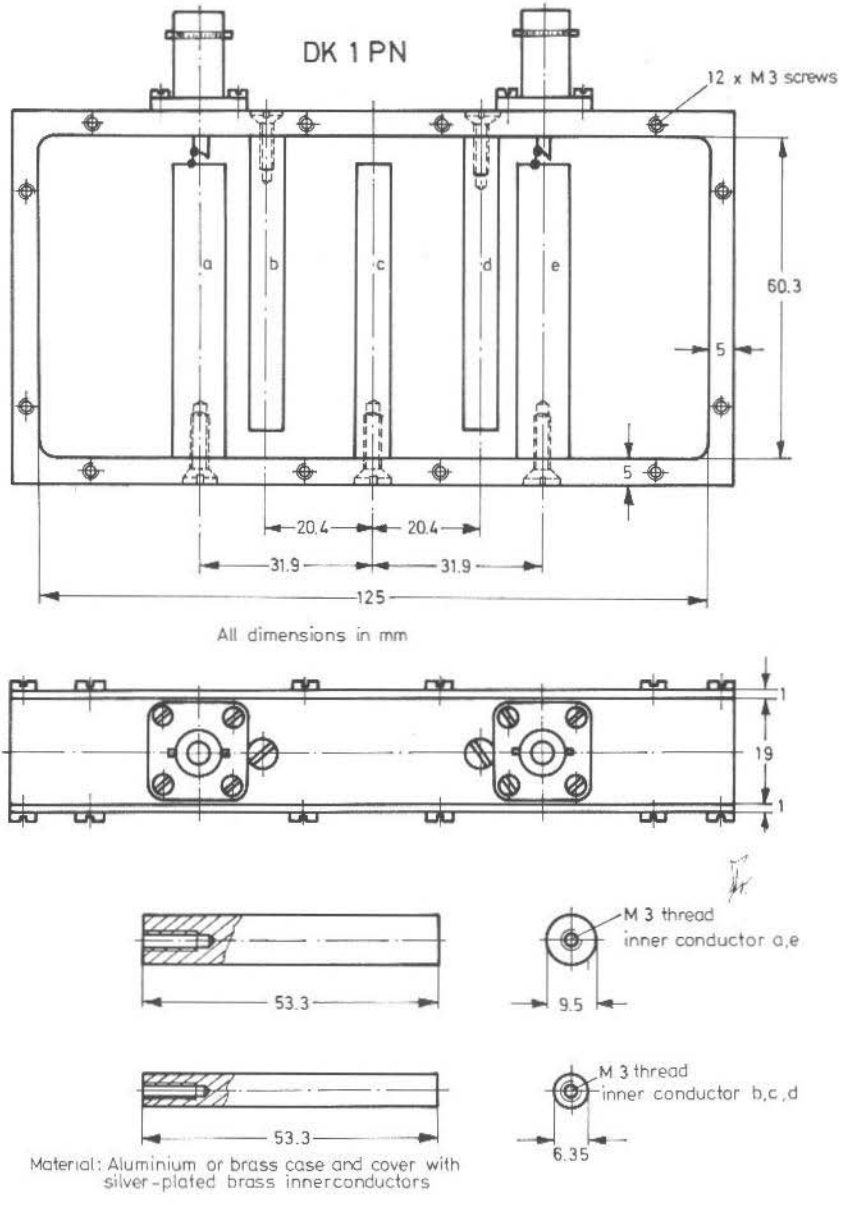

Fig. 2: Interdigital filter for 23 cm

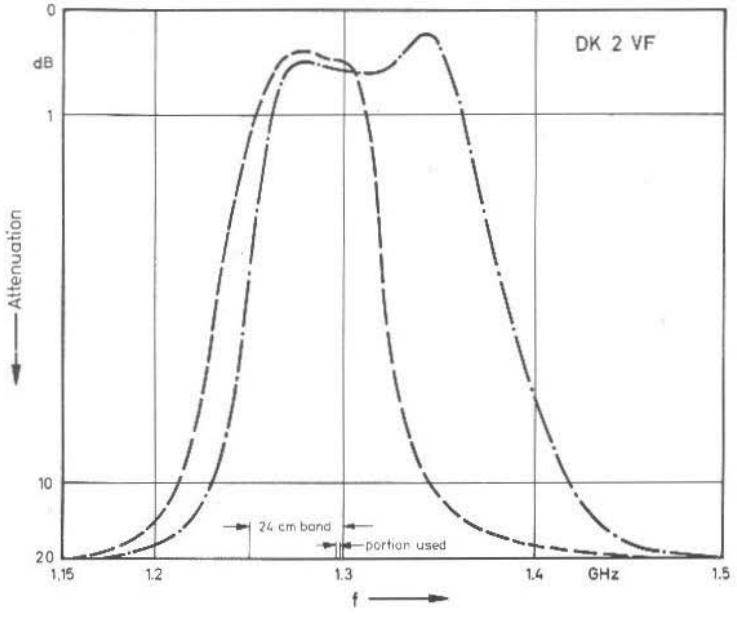

Fig. 3: Passband curves of two different examples of the 23 cm filter

In addition to this, it was found that the spacings between the inner conductors and their length should be maintained as accurately as possible to the values given in Figure 2. Slight constructional tolerances can - if such accurate measuring equipment is available - be compensated for by shortening or lengthening one or more of the inner conductors. The lengthening of such a line can be made by providing a washer. It is possible for a continuous alignment of the circuits to be made when screws are provided in the longitudinal wall opposite to the non-loaded ends of the line circuits. The described filter can, however, be used without having to be measured if the given dimensions are followed with a maximum tolerance of approximately 0.3 mm.

5. AVAILABLE PARTS

A complete filter as well as a kit without connection sockets is available from the publishers or their national representatives. Please see advertising page.

6. REFERENCES

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IRE Trans. on Microwave Theory and Techniques
vol. MTT-10 (Nov. 1962), Pages 479-491

(2) W. S. Metcalf: Graphs Speed Design of Interdigital Filters
Microwaves, Feb. 1967, Pages 91-95

(3) R. E. Fisher: Interdigital Bandpass Filter for Amateur VHF/UHF
Applications, QST March 1968, Pages 32-33

A GROUND STATION FOR SATELLITE COMMUNICATIONS VIA OSCAR 6

by Dr. A. Gschwindt, HA 8 WH

The following article describes the ground station of the Budapest University designed for operation in conjunction with the OSCAR 6 satellite which is planned to be launched by AMSAT' in late 1971.

A transmit-receive ground station is to be described which enables the troublesome frequency variation caused by the Doppler effect to be eliminated. It is planned to have this station operative during the summer of 1971.

Using this system, communications will be just as easy as on the shortwave bands. The stations can work on the same frequency during the pass of the satellite. No frequency variation will occur during communication. If the station is lost due to interference, fading etc., he will be on the same frequency after the interference has ceased.

Unfortunately, very little information was available regarding OSCAR 6 whilst planning this ground station. Even now, it is still not clear what repeaters will be carried or when it will be launched. For this reason, the VHF-Group with HA 8 WH only planned the ground station and Doppler correction system for operation in conjunction with the linear 432/144 MHz repeater of OSCAR 6. In order to carry out tests successfully during the operation of OSCAR 6, it will be necessary for us to find other well-equipped stations to carry out common experiments. Since the expected orbital height will be approximately 1000 km, most of the useful station locations will be within Europe.

1. FREQUENCY VARIATION BETWEEN TWO STATIONS DURING THE SATELLITE PASS

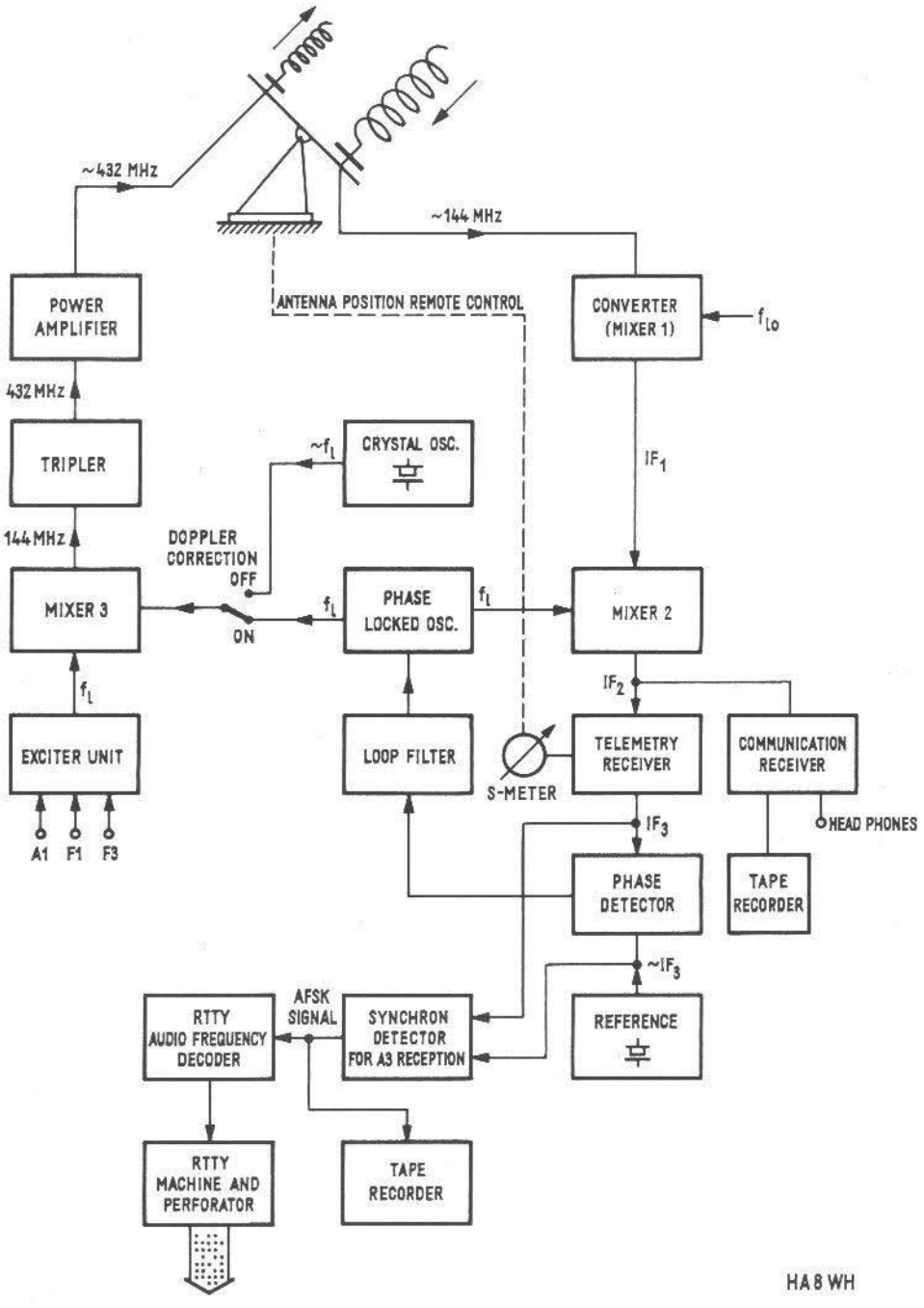
The linear transponder of OSCAR 6 will receive signals from earth on the 432 MHz band, will amplify them and re-transmit them to earth on the 144 MHz band.

The frequency variation caused by the Doppler effect therefore occurs twice: Once on the earth to satellite path (Δf_1) and once from satellite to earth (Δf_2). If the receiver is equipped with an automatic frequency control circuit (AFC), it will be possible to eliminate the frequency variation of both paths as long as the signal remains within the hold range of the AFC circuit and as long as the station transmits continuously. In practice such an AFC circuit would not be able to hold the frequency long enough to allow communication to take place.

A more reliable correction method can be realized using the carrier of the telemetry transmitter onboard the satellite which will be audible throughout the whole satellite pass.

2. BUILD UP OF THE STATION

The block diagram given in Figure 1 shows the principle of the station.


~432 MHz
~144 MHz
ANTENNA POSITION REMOTE CONTROL
POWER AMPLIFIER
CONVERTER (MIXER 1)
f_{Lo}
432 MHz
TRIPLER
$\sim f_L$
CRYSTAL OSC.
IF_1
144 MHz
DOPPLER CORRECTION OFF
ON
MIXER 3
f_L
PHASE LOCKED OSC.
f_L
MIXER 2
IF_2
EXCITER UNIT
f_L
LOOP FILTER
S-METER
TELEMETRY RECEIVER
COMMUNICATION RECEIVER
HEAD PHONES
A1 F1 F3
IF_3
PHASE DETECTOR
TAPE RECORDER
$\sim IF_3$
AFSK SIGNAL
RTTY AUDIO FREQUENCY DECODER
SYNCHRON DETECTOR FOR A3 RECEPTION
REFERENCE
RTTY MACHINE AND PERFORATOR
TAPE RECORDER
HA 8 WH

The frequency correction is made in the following manner: The frequency variation Δf_2 occuring on the satellite to ground path is eliminated by the automatic phase control (APC) circuit of the receiver. The frequency variation Δf_1 required for the transmitter is, of course, three times greater on 432 MHz than on 144 MHz. Also the frequency variation Δf_2 must be opposite to the variation. Δf_2. This means that $\Delta f_1 = -3\Delta f_2$ where the minus sign means opposite and not negative.

Let us now consider the behaviour of the station; the telemetry transmitter is operating in the A3-mode.

The following parameters are available:

f_c = carrier frequency of the telemetry transmitter
IF_1 = first intermediate frequency
IF_2 = second intermediate frequency
IF_3 = third intermediate frequency
f_{lo} = local oscillator frequency of the converter
f_l = phase locked oscillator frequency
f_t = output frequency of the exciter

The incoming signal from the satellite is mixed with the local oscillator frequency of the converter producing the first intermediate frequency IF_1:

$$IF_1 = f_c + \Delta f_1 - f_{lo} \; ; \quad f_{lo} < f_c + \Delta f_1$$

IF_1 is now passed to mixer 2 where it is mixed with the phase-locked frequency f_l to form IF_2. If it is assumed that $f_l > IF_1$, this will mean:

$$IF_2 = f_l - (f_c + \Delta f_1 - f_{lo})$$

The frequency f_l varies together with the incoming signal due to the phase-locked loop.

The output signal of the telemetry receiver (IF_3) feeds one input of the phase detector, the reference signal the other. After phase comparison, the phase (and thus frequency) of the phase-locked frequency f_l is controlled using the error signal.

Frequency f_l will follow the Doppler frequency variation:

$$f_l = IF_2 + f_c + \Delta f_1 - f_{lo}$$

where $f_l > IF\ 2$.

The frequency variation of f_l is inverted in the third mixing process. At the output of mixer 3, the frequency will be:

$$f_t - f_l = f_t - IF_2 - f_c - \Delta f_1 + f_{lo}$$

This frequency will be in the 144 MHz band which is multiplied to the required output frequency in the 432 MHz band.

The frequency tripling provides a Doppler frequency variation that has both the correct magnitude and direction and represents the pre-correction for the earth to satellite path.

The frequency transmitted by the ground station is

$$\underbrace{3\,(f_t - IF_2 - f_c + f_{lo})}_{f_o} - 3\,\Delta f_1 = f_o - 3\,\Delta f_1$$

The frequency f_o remains constant during reception. If the frequencies f_t or f_{lo} or IF_2 vary, this will cause the output frequency to also vary. This means that very stable oscillators must be used to eliminate any unwanted frequency variation of the transmitter.

The transmitter is then tuned by the variation of the frequency f_t of the exciter.

The Doppler correction is switchable; when the correction system is switched off, a crystal oscillator with the frequency f_1 takes over and is introduced into the phase-locked loop.

In our system, we are using a coherent detector for reception of the telemetry signals in order to eliminate the "knee" effect of an envelope detector.

The reception of the communications and other channels in addition to the telemetry signal is obtained by connecting one or more receivers to the second intermediate frequency IF_2.

Of course, it would be possible to tune the transmitter by varying the frequency of IF_2; however, in this case the telemetry and other receivers connected to IF_2 wound also be shifted in frequency.

The tuning range of IF_2 may not be greater than 1/3 of the bandwidth of the channel. For a Channel bandwidth of 50 kHz : 16.6 kHz. If the phase locked loop is operating correctly, the phase-lock of the loop will remain synchronized when tuning slowly. In this case, the exciter frequency f_t would remain constant.

2.1. OPERATIONAL EXAMPLE

Let us assume that the satellite is transmitting on f_c = 145.9 MHz and receives on 432.3 MHz.

The incoming frequency ($f_c + \Delta f_1$) is changed in the converter to 29.9 MHz (IF_1) by mixing it with the local oscillator frequency of 116 MHz (f_{lo}). If a frequency of 7 MHz is chosen for IF_2, a frequency of 36.9 MHz would be required as f_1. The frequency of IF_3 depends on the communications receiver used for reception of the telemetry signal. If it is assumed to be 450 kHz and the phase-locked loop is operating correctly, the reference frequency will also be 450 kHz.

At the output of the third mixer, a signal of 432.3÷3 = 144.1 MHz will be present. This means that the output of the exciter will be
f_t = 144.1 + 36.9 MHz = 181 MHz.

After passing the transmit signal through mixer 3 and the tripler , the required output frequency of 432.3 MHz will be available together with any frequency shift necessary to compensate for the Doppler frequency variation.

2.1.1. ANOTHER VARIANT

It is possible for another frequency plan to be used in conjunction with the previously described station:

Let us assume that the satellite frequency f_c and the frequencies of IF_1 (29.9 MHz), IF_2 (7 MHz) and f_1 (36.9 MHz) remain as in the first example.

If the Doppler frequency variation is inverted in the converter the following will be valid:

$$f_{lo} > f_c + \Delta f_1, \quad \text{thus } IF_1 = f_{lo} - f_c - \Delta f_1$$

The frequency required from the exciter unit will then be 144.1 - 36.9 MHz = 107.2 MHz. This signal is converted in mixer 3 to one third of the output frequency (additive mixing) which is then tripled to the required output frequency. The previous frequency plan would be more useful if high-level mixing is employed in mixer 3.

2.2. SYSTEM ACCURACY

The theoretical accuracy of the Doppler-shift correction system is determined by the ratio of the transmit and receive frequency. If they have a direct harmonic relationship to another, the error will be zero.

In the example described in this article, the relative error will be:

$$\Delta f = \frac{3 \times 145.9}{432.3} = 1.01$$

This means that the error is only in the order of 1%, or an error of 100 Hz in the corrected system for an original error (Doppler shift) of 10 kHz.

3. REFERENCES

(1) AMSAT: OSCAR 6 - Technical Description and Project Status
VHF COMMUNICATIONS 3 (1971), Edition 2, Pages 93-97

4. EDITORIAL NOTES

Dr. Gschwindt would like to cooperate with other groups interested in satellite communications. Would any interested persons contact him under the following address:

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Hungary

BASIC DIGITAL CIRCUITS

by D. E. Schmitzer, DJ 4 BG

Recent articles on electronic keyers, automatic calling systems, frequency counters, RTTY decoders etc. show that more and more digital circuits are being used in amateur radio equipment. This interest is due to the falling prices and inherent reliability of integrated digital circuits.

In order to assist the understanding of digital techniques, some of the basic functions are to be explained that are required repeatedly. Even very complicated digital equipment can be split down to such basic functions.

1. PREREQUISITES

Since the same components occur again and again and the circuit itself is not so important as the function, one usually neglects the actual circuitry of resistors, diodes, transistors etc. This means that one limits oneself to a block diagram indicating the individual digital functions. Several of these symbols are given in Figure 1, and are explained in the following sections. In all cases, a phase reversal is designated by a point at the output (see AND and NAND or OR and NOR). Generally speaking, digital circuits can only differentiate between two conditions, namely "voltage" and "no voltage". These two conditions are used to be associated with the binary numbers ONE and ZERO. In our case the "no voltage" condition has been assigned to the O-condition and "voltage" to the 1-condition. This agreement must be defined further in order to understand available components: In the case of TTL-circuits (Transistor-Transistor-Logic/operating voltage + 5 V), voltage levels of + 0.3 V and approximately 3.5 V appear at the output. The lower voltage level corresponds to the O-condition and the higher, more positive voltage to the 1-condition. This system where the more positive voltage corresponds to 1 is called "positive logic". If the opposite is the case, one will be using "negative logic". In addition to this, different voltages are used for 0 and 1-conditions according to the different circuits. Due to the popularity of the TTL-technology, this article is to devote itself to positive logic at the given voltages.

2. BASIC FUNCTIONS

2.1. INVERTERS

The simplest digital operation is inversion, e.g. when a 0-signal is fed to the input, a 1-signal will be present at the output, and vice versa.

The symbol for this is given in Figure 1a and a detailed circuit of such an inverter in TTL technology is shown in Figure 2. It can be seen that it is a type of series push-pull stage comprising T 3 and T 4 which is driven via transistor T 2. A further transistor (T 1) is connected in an unusual circuit to the input of transistor T 2. If a positive voltage is fed to the emitter of T 1 (logic-1) or if left disconnected, a current will flow from U+ via resistor R 1 and the base-collector path of T 1 to the base of T 2 which is driven. The result of this is that T 3 is blocked and T 4 will conduct so that the voltage at the output will fall to the residual voltage of T 4 which is in the order of 0.1 - 0.4 V (logic-0). If, on the other hand, 0-potential is present at the emitter of T 1, the current from R 1 will be diverted to the input and T 2 will be blocked.

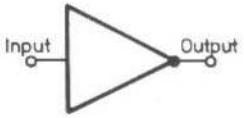

Fig. 1 a: Symbol of an inverter

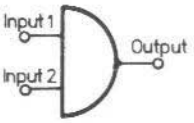

Fig. 1 b: Symbol a two-input AND-gate

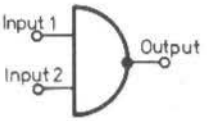

Fig. 1 c: Symbol of a two-input NAND-gate

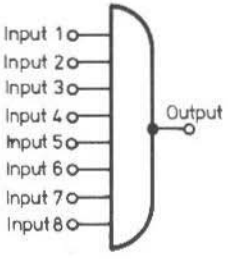

Fig. 1 d: Symbol of a NAND gate with multiple inputs (8)

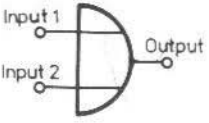

Fig. 1 e: Symbol of an OR-gate

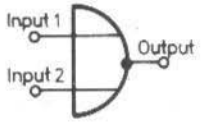

Fig. 1 f: Symbol of a NOR-gate

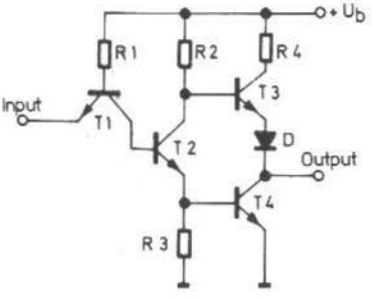

Fig. 2: Basic TTL circuit: inverter ($1/6$ th of an SN 7405)

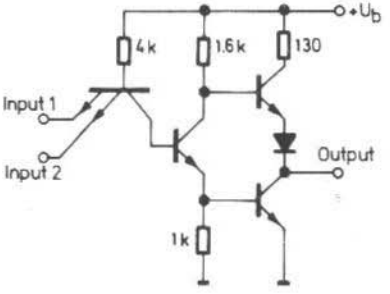

Fig. 3: Basic TTL circuit, NAND-gate with two inputs ($1/4$ of an SN 7400)

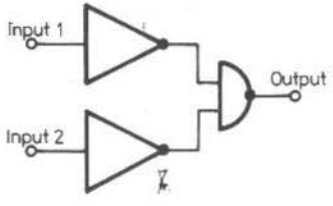

Fig. 4: Combination of an OR-function from two inverters and a NAND-gate

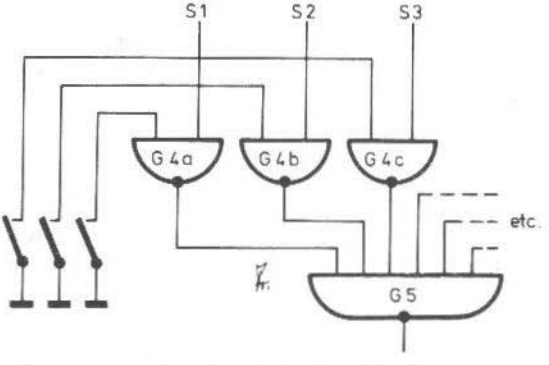

Fig. 5: Extract from the circuit of a calibration spectrum generator for explaining the operation of the NAND-gate G 5

This means that T 4 is also blocked and T 3 will conduct via R 2. A positive voltage is then present at the output which is to the value of the voltage drop across R 4, T 3 and D less than the operating voltage (+ 5 V) and is thus in the order of 3.5 V (logic-1).

2.2. AND GATES

If the input transistor T 1 is provided with more than one emitter, as shown in Figure 3, it will be possible for several signals to be operative. Even if only one of the inputs is at 0-potential, the whole current of R 1 will flow via this input and 1-potential will be present at the output. It is only when all inputs are at 1-potential that the output can change to 0. This circuit therefore behaves as the inverter described in Section 2.1. with the additional condition that all inputs must be of 1-potential to obtain the opposite 0-potential at the output. Such circuits are designated NAND-gates (NOT-AND). The function of such a NAND-gate can be explained and remembered as follows: A 1-potential will only not (N) be present at the output when inputs 1 AND 2 AND 3 etc. are fed with 1-potential. Such gate circuits are available with two, three, four, five and eight inputs which means that circuits can be used where 1-potential must be present at up to eight different inputs before the output potential shifts to 0. This means that up to eight conditions must be fulfilled by a circuit before 0-potential appears at the output to actuate a certain function.

2.3. OR GATES

If an inverter is connected before each input of an AND-gate (Fig. 4), a different type of circuit results: If only one input is at 1-potential, this will cause 1-potential to appear at the output because the inverter before the input converts the 1-potential to 0-potential at the input of the AND-gate breaking the AND-condition where all inputs must be at 1-potential for an output of 0. Such circuits are called OR-gates because the following is valid: when 1-potential is present at input 1 OR 2 etc., 1-potential will be present at the output. This means that it is possible to actuate a certain function when one or more conditions are fulfilled, namely when a 1-potential appears at one input.

The author uses such a circuit in a somewhat extended form in a calibration spectrum generator that is to be described in a later edition of this magazine. In this calibration generator, the individual signals of 100 kHz, 50 kHz etc. are not fed via inverters but via an inverting gate to the AND-gate, as shown in Figure 5. If one input of such a gate is at 0-potential, this will cause 1-potential to appear at the output so that the subsequent gate is not affected. The signal S at another input has therefore no effect on the output signal. Different conditions exist when input 1 is not driven; in this case, the signal at input 2 (an alternating voltage fluctuating between 0 and 1-potential) switches the voltage at the output of the gate and will control gate G 5. The switching process is inverted by gate G 4a or G 4b and the NAND-gate G 5 will operate as an OR-gate.

Since it would be very clumsy to place an inverter in front of an AND-gate to obtain an OR-function, components are available that combine these two functions in one circuit (Fig. 6). An additional inversion occurs with these circuits which are designated NOR-gates (NOT-OR).

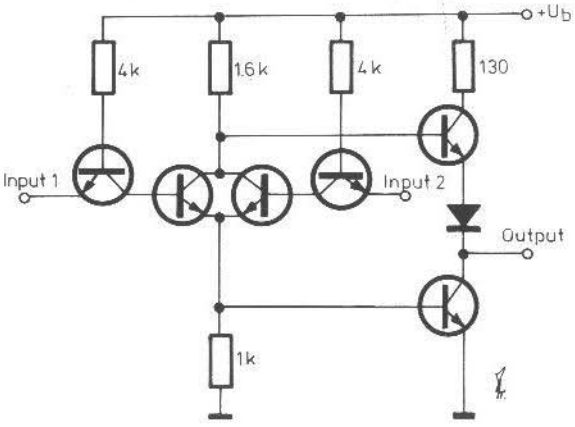

Fig. 6: Basic TTL circuit, NOR-gate with two inputs ($^1/_4$ SN 7402)

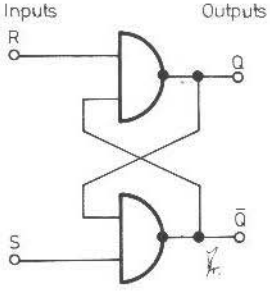

Fig. 7: R-S flip-flop

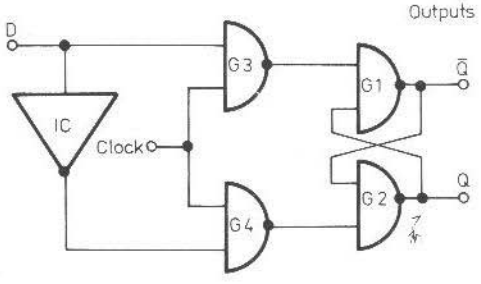

Fig. 8

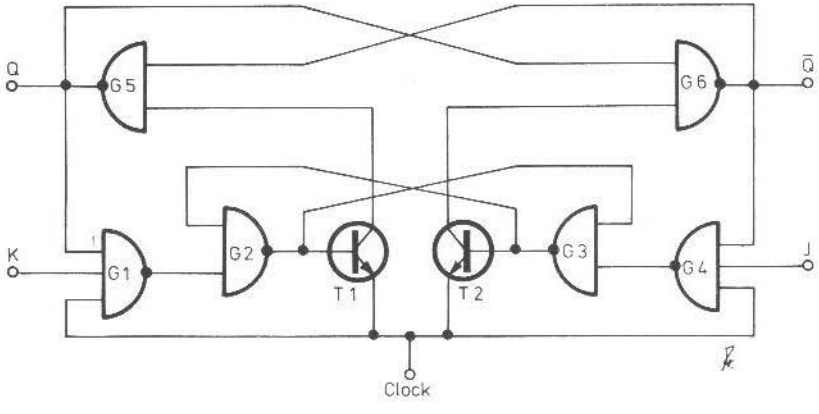

Fig. 9: J-K master-slave flip-flop ($^1/_2$ SN 7473, clear input has been deleted for simplicity)

3. STORES AND COUNTERS

Storage elements also pay an important part in the digital technology. The flip-flop represents one of the simplest storage elements. Several such circuits are to be explained from the extremely large numbers of possibilities that exist.

3.1. R-S FLIP-FLOP

The simplest bistable or flip-flop circuit is obtained when two gates are connected in the form of a cross, as shown in Figure 7. If one of the free inputs, e.g. "R", is momentarily placed at 0-potential, a 1-signal will appear at output "Q". Due to the interconnection of these two gates, this condition will be maintained until input "S" receives 0-potential. This will cause output "Q" to be switched to 1-potential whereas Q returns to 0. It is therefore possible for a certain condition to be selected by feeding a short pulse to the appropriate input; the condition can then be maintained indefinitely.

3.2. CLOCKED FLIP-FLOP

The simple circuit shown in Figure 7 has the disadvantage that one or the other input must be driven according to the required function and that the storage occurs the moment the input signal appears. Any change of the input signal can change the stored state. This can be avoided using the circuit shown in Fig. 8.

By adding an inverter, one can ensure that only one input is fed with the appropriate signal. Using intermediate gates, it is possible to ensure that the input signal is only passed to the actual storage element (the interconnected gates) when a 1-potential is present at the clock input. As soon as the clock input returns to 0, all outputs of the intermediate gates G 3 and G 4 will return to 1-potential and no longer have any influence on the contents of the store. The input voltage at input "D" can vary at will, it will have no effect on the stored information. Only a new 1-signal at the clock input allows the stored information to be altered.

3.3. MASTER-SLAVE FLIP-FLOP

The circuit given in Figure 9 can also only be set via one of its two inputs when a 1-signal is present at the clock input C. Since this circuit consists of two interconnected flip-flops (G 5 and G 6 as well as T 1, T 2, G 2 and G 3), it is able to react in a specific way to the clock-pulses at C when inputs J and K are not driven. A pulse fed to C would, with the present circuit, for instance, switch Q to zero. The condition is stored after the pulse has been ceased at C. The next pulse at C returns Q to 1-potential. This means that two pulses (0-1-0) are required to obtain a 1-0-1 transition at the output. This represents a (frequency) division of 2 : 1. When connected in series, such circuits can therefore be used for frequency division in steps of two. When four circuits are used, a divide-by-sixteen circuit can be formed.

3.4. DIVIDE-BY-TEN CIRCUIT

By suitable interconnection of the stages via the J and K inputs (which have not been used up till now), it is possible for all stages to be reset to zero after the tenth pulse. This means that the output signal will not be 1/16th of the input signal but 1/10th. A frequency division of 10 : 1 is therefore obtained in this manner (see Fig. 10).

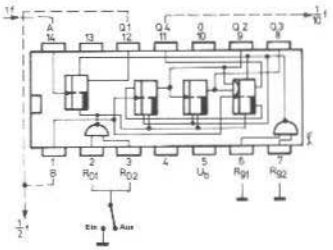

Fig. 10: 10 : 1 frequency divider (SN 7490)

Such a configuration is available as the integrated circuit SN 7490 N where all functions are made on a silicon chip of about one square millimetre. The SN 7490 N comprises more than 50 transistor systems and just as many resistors. In addition to the previously mentioned characteristics, this integrated circuit is provided with reset inputs which allow it to be reset to zero, independent of the state of the division process and pulse, when a 1-signal is present at this input. This allows the frequency divider to be disabled (switched off) without removing the operating voltage. The highest input frequency at which the circuit is able to operate is given as over 10 MHz by all manufacturers.

4. NOTES

This article does not claim to be complete but is designed to at least provide a few basic fundamentals so that one is better able to understand digital circuitry.

5. REFERENCES

(1) Texas Instruments: Data Sheets

A WIDEBAND PREAMPLIFIER FOR FREQUENCY COUNTERS UP TO 60 MHz

by W.-R. Kritter, DL 8 TM

TTL integrated circuits of the SN 74.. series and equivalents require a square-wave drive signal of approximately 2.5 V. This means that a preamplifier and a pulse shaper will be required in a number of applications in order to drive frequency counters equipped with these components. The bandwidth of the pre-amplifier must at least cover the frequency range up to the highest frequency that can be processed by the frequency counter. The output signal of the pre-amplifier must have a square waveform with a rise time less than the maximum permissible rise time of 10 ns for TTL counting decades. Since higher input voltages can be applied, the preamplifier should be provided with some form of attenuator.

1. CIRCUIT DETAILS

A suitable wideband preamplifier is to be described. It was designed for operation in conjunction with a frequency counter having an upper frequency limit of 60 MHz. The gain of the preamplifier allows input voltages of less than 100 mV (typical is 35 mV) to be measured in the subsequent frequency counter. Due to the continuously variable attenuator, the input signals can be as high as 4 V_{rms}. The circuit diagram of this preamplifier is given in Figure 1.

The three-stage amplifier is built up in a similar manner to an integrated TTL NAND-gate. The various stages are directly coupled and are fed from the same stabilized voltage of 5 V as the frequency counter. Since the operating voltage is accurately determined, it is only necessary to adjust the operating point for optimum balance. Two resistors having a tolerance of 5% (R 105, R 107) are required for this.

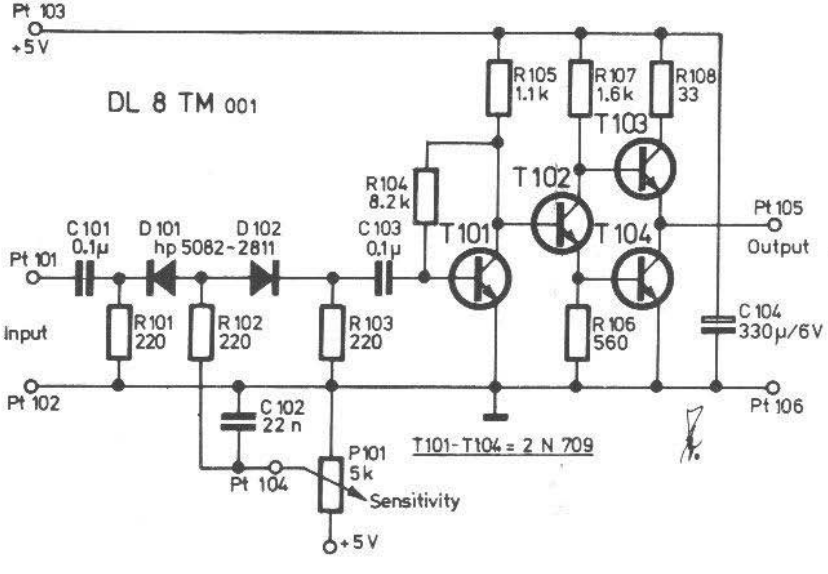

Fig. 1: Circuit diagram of a wideband preamplifier and pulse shaper for frequency counters of up to 60 MHz

If the preamplifier is to provide the required rise time for the pulses even at 60 MHz, only very fast transistors may be used. The transistor type 2 N 709 used here has a storage time t_s of maximum 6 ns. Other switching transistors such as 2 N 706 and 2 N 708 ($t_s \leqq 25$ ns), or 2 N 914 ($t_s \leqq 20$ ns) or 2 N 2368 ($t_s \leqq 10$ ns) have been found to be unsatisfactory.

A two-stage voltage divider with variable attenuation is connected to the input of the preamplifier. Each voltage divider consists of a diode and a resistor. If the diodes are opened by the voltage adjusted at the potentiometer, they will only exhibit a very low forward resistance which means that no voltage division will take place. The input impedance of the preamplifier in this condition virtually consists of the three parallel-connected resistors of 220 Ω and thus amounts to approximately 70 Ω. This means that the input signal can be fed to the preamplifier using a coaxial cable.

If on the other hand both diodes are blocked, a double voltage division occurs across the capacitive resistance of the diodes and the associated 220 Ω resistors. The Schottky (hot carrier) diodes type Hp 5082-2811 possess a capacitance of 1.2 pF which corresponds to a resistance of 2.2 kΩ at 60 MHz. This means that the input signal is divided twice by 10 : 1 at 60 MHz which results in a total attenuation of 100 : 1. At lower frequencies, the capacitive resistance is higher and the voltage division correspondingly greater.

With the diodes blocked, the input impedance of the preamplifier is virtually only given by the resistor R 101 and thus amounts to approximately 220 Ω. This means that the input impedance can vary between 70 Ω and 220 Ω according to the position of the attenuator potentiometer.

2. CONSTRUCTION

The preamplifier as shown in Figure 1 is accommodated on a printed circuit board of 80 mm by 30 mm. The connections have been kept very short; the transistors should be soldered into place so that the bottom of the case is not more than 3 mm from the surface of the PC-board. The printed circuit board, which is designated DL 8 TM 001, is given in Figure 2.

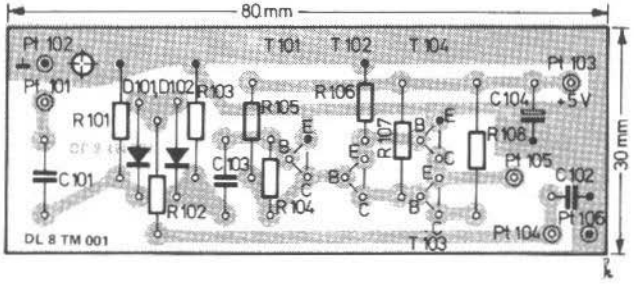

Fig. 2: Printed circuit board DL 8 TM 001

A coaxial cable or socket can be connected to the input Pt 101/Pt 102. The output Pt 105 is connected to the input of the frequency counter with the aid of a thick, short wire. In addition, an equally low-inductive connection must be made from Pt 106 or direct from the ground surface of the preamplifier to the input of the frequency counter. Only DC is present at the potentiometer which means that it can be located anywhere required.

2.1. SPECIAL COMPONENTS

T 101 - T 104: 2 N 709 (Texas Instruments)

D 101, D 102: hp 5082-2811 (Hewlett-Packard) or similar Schottky diodes

All resistors should be suitable for 10 mm spacing.

C 101, C 103: Plastic-foil capacitors for PC-board mounting, spacing 10 mm
C 102: Ceramic disc capacitor of approx. 22 nF
C 104: Tantalium-Electrolytic capacitor of approx. 330 μF/6 V

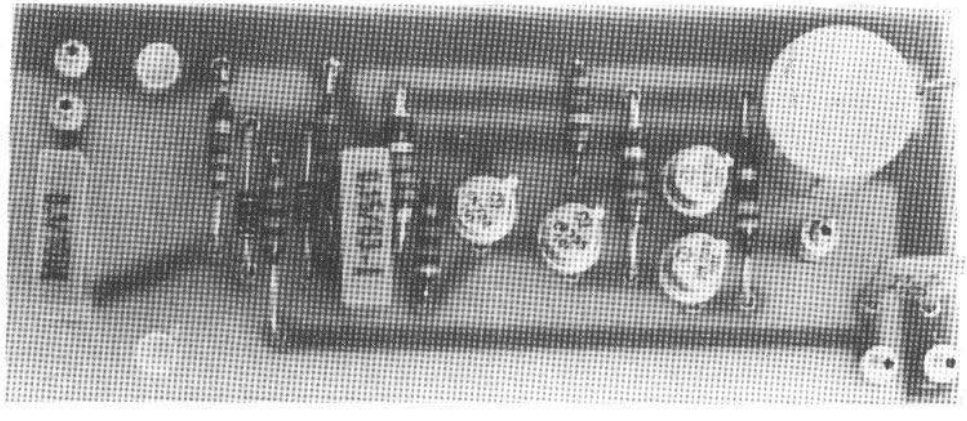

Fig. 3: A photograph of the prototype counter preamplifier

3. CONNECTION TO THE FREQUENCY COUNTER DJ 6 ZZ 003

The described preamplifier is especially well suited to the frequency counter module described in (1). For use in conjunction with this frequency counter, connection Pt 105 of the preamplifier should be connected to Pt 1 of the counter module, the ground connections interconnected and the +5 V connection Pt 103 connected to the +5 V line of the frequency counter. The 1.2 kΩ resistor between the counter input and the +5 V line as well as the simple pulse shaper comprising the transistor BF 224 should be removed.

4. AVAILABLE PARTS

The printed circuit board DL 8 TM 001 and the semiconductors are available from the publishers or their national representatives. Please see advertising pages.

5. REFERENCES

F. Weingärtner: A Four-Digit Frequency Counter Module for up to 30 MHz In this edition of VHF COMMUNICATIONS.

A FOUR DIGIT FREQUENCY COUNTER MODULE FOR FREQUENCIES UP TO 30 MHz

by F. Weingärtner, DJ 6 ZZ

The necessity of knowing the exact frequency is not only important to satisfy the regulations of the amateur radio licence but is a sphere of special interest for a large number of radio amateurs. For many VHF-UHF applications it is imperative to know the frequency exactly: for instance, moonbounce and meteor scatter. This counter can be connected to the VFO or some other point in the exciter or receiver where the frequency multiplication factor is known. This article is designed to at least satisfy the measuring requirements of radio amateurs in the frequency measuring sector. The economic price of this module makes it of interest to a great number of amateurs.

Figure 1 shows a photograph of the frequency counter module which satisfies the requirement of providing an inexpensive counter that can be constructed extremely easily. It comprises 22 digital integrated circuits of the TTL-series SN 74.. N, a 1-MHz crystal, four transistors, four digital Nixie indicator tubes, several capacitors and resistors as well as a double-coated printed circuit board with through-contacts. The latest professional counters use 7-segment numerical indicators that are at present still more than five times more expensive than nixie tubes. They have the advantage that no high-tension supply of about 170 V is required and of a longer life. However, this is of no importance for our applications since the life of 30.000 hours rated for Nixie indicator tubes under normal operating conditions is most certainly sufficient.

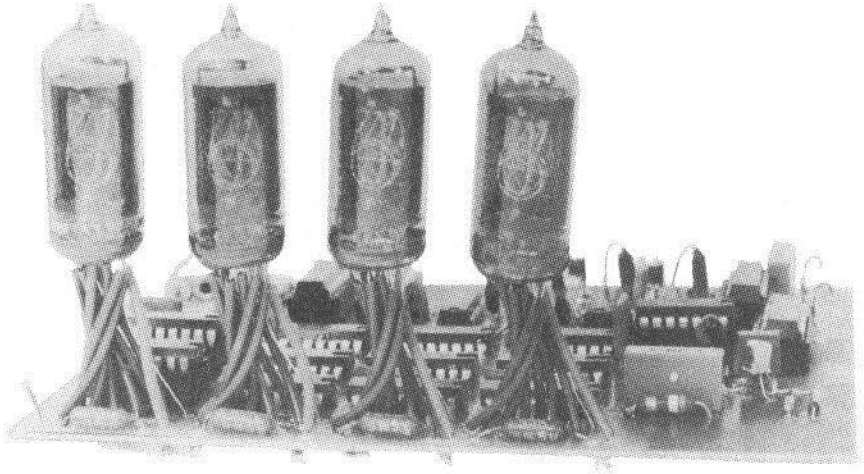

Fig. 1: The four-digit frequency counter module DJ 6 ZZ 003

If a selected integrated circuit SN 7490 N is used as first decade counter, frequencies of up to 30 MHz can be counted. In spite of the fact that the counter is limited to four digits, it is possible by switching the clock to measure down to the 100 Hz position. If a frequency of 12.3456 MHz is assumed, one of the following numerical sequences will be indicated:

12.34 MHz 2.345 MHz 3456 MHz

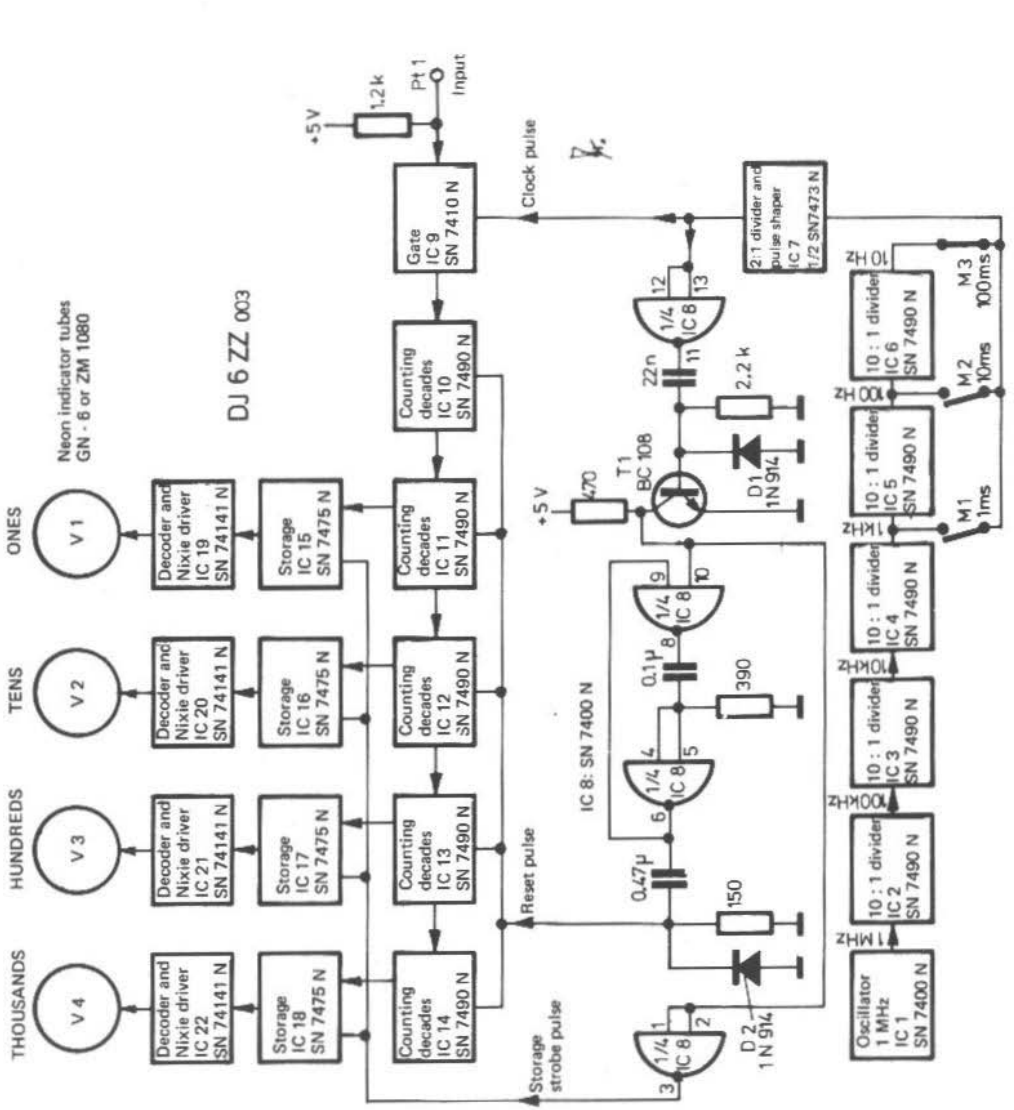

Fig. 2: Block diagram of the frequency counter

The accuracy of the frequency counter is only dependent on the accuracy of the 1-MHz crystal standard which controls the counting intervals via the time base circuit (clock). The crystal can be zero-beated to a frequency standard transmitter with the aid of a trimmer in the same manner as a calibration spectrum generator.

In order to keep the dimensions of the relatively expensive double-coated PC-board with through-contacts to a minimum, a power supply, preamplifier and pulse shaper circuit have not been provided on the main board.

The integrated power supply described in (1) is well suited for this application. A very simple pulse-shaper for the frequency to be measured is to be described in this article. This means that the basic module is able to carry out frequency measurements with input levels of 2 V to 4 V peak-to-peak. A wideband preamplifier suitable for operation with this frequency counter is described in this edition of VHF COMMUNICATIONS (2).

In the form described in this article, the publishers built up and used the counter for measurements on a two metre transistor transmitter by connecting it to the IF-output of a two metre converter. The coupling attenuation of the antenna relay (40 dB) provided sufficient IF-voltage at 28 MHz to operate the frequency counter without preamplifier.

1. PRINCIPLE OF OPERATION

The principle of operation is to be explained in conjunction with the block diagram in Figure 2. An introduction to the operation of digital circuits is given in "Basic Digital Circuits" (3) in this edition of VHF COMMUNICATIONS.

1.1. COUNTING GATE

The input of the frequency counter (Pt 1) is fed with the steep, limited square-wave signal of unknown frequency provided by the pulse shaper.

The counting gate comprising integrated circuit IC 9 allows the pulses to pass to the counter circuit as long as the clock pulse is at 1-potential. If the clock pulse returns to 0, the gate will be blocked, the count is complete and the result will be indicated which means that the counting period corresponds to 1 ms, 10 ms or 100 ms according to which clock time has been selected.

1.2. TIME BASE

The time base circuit comprises the integrated circuits IC 1 to IC 7. The frequency of a 1-MHz crystal oscillator (IC 1) is passed through five frequency divider circuits of 10 : 1 each (IC 2 to IC 6). All frequencies selected by the clock switch M (let us assume 100 ms in the following) consist of an 1 and 0-potential signal. These signals differ in length. Since the clock pulse must be 100 ms of 1-potential, the clock frequency is divided once again by 2 : 1 in the flip-flop circuit comprising IC 7. The exactly shaped clock pulses required are generated in this manner from the previous signal, which in our example consists of a 100 ms 1-signal and a 100 ms 0-signal.

1.3. COUNTER

The pulse counter consists of the five counting decades IC 10 to IC 14. The same digital circuits are used as in the time base. After the first counting decade (IC 10) has received 10 pulses, it will pass an impulse to the next decade and return to zero. After a further 10 pulses, a second pulse will be passed to the second decade (IC 11) and so on until the hundredth pulse which is passed on to the third decade comprising IC 12. This process, which corresponds to a frequency division of 10, continues until the gate is closed.

The contents of the counting decades IC 11 to IC 14 are then available for storage. Since the condition of each counter decade is available in BCD-code, e.g. as a 1 or 0-signal on each of four flip-flops, four connections exist between each decade and the associated buffer storage. After transposing the information into the storage, the counting decades are returned to zero by the reset pulse (1-signal at the reset inputs). They are then prepared for the next counting process.

1.4. STORAGE

The storage configuration consists of four integrated storage components IC 15 to IC 18. Each of these integrated circuits consist of four flip-flops whose inputs are connected to the BCD outputs of the counting decades. The contents of the counters are transposed into the buffer storage during the storage strobe pulses. (1-signal at the special strobe pulse inputs), and are stored until the next strobe pulse is received. This storage ensures that the varying conditions existing during the count are not passed on to the indicator tubes and indicated.

1.5. DECODER AND NIXIE DRIVER

Four integrated decoder and Nixie driver components IC 19 to IC 22 are connected to the output of the storage. The BCD-code is converted in a matrix into the decadic numerical system. This means that they are provided with four inputs and ten outputs. Each output is also provided with a transistor for switching the neon tubes.

1.6. NEON INDICATOR TUBES

The numerical indicator tubes are so called cold cathode types that operate without heater. The 14 mm high digits (0 to 9) are made visible by discharge in a gas environment. Each of the digits can be fired by grounding its cathode. This is achieved with the previously mentioned decoder and Nixie drivers.

The 10 cathodes have a common anode which is connected to a positive operating voltage via a dropper resistor as with other neon tubes. According to the operating voltage, these four dropper resistors must have one of the following values:

U_b (V)	400	300	200
R_d (kΩ)	150	100	33

With most tubes it is possible to operate with an operating voltage of as low as 170 V and a dropper resistor of 27 - 30 kΩ. The anode current per tube is only approximately 1.7 mA, which means that the anode voltage supply of this counter need only be dimensioned for approximately 8 mA.

1.7. RESET AND STORAGE STROBE PULSES

These two 0-1-0 pulses are derived from the clock pulse that controls the whole time base. They must be generated one after the other and in the time between completion and commencement of a count, e.g. whilst the clock signal is 0. The four NAND gates of the integrated circuit IC 8 are used for this. The circuit diagram is included in Fig. 2 since it contains a number of discrete components.

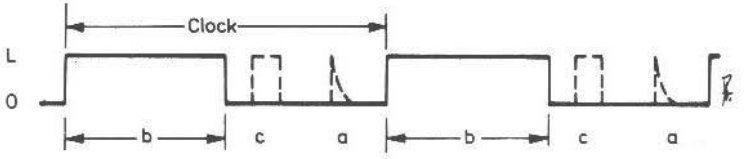

Fig. 3 a: Pulse sequence for controlling the counter

Fig. 3a shows the pulse sequence of the counter in the time scale:
a) Reset pulse
b) Half clock time: Gate open (100 ms, 10 ms or 1 ms)
c) Storage transfer pulse (strobe pulse)
and so on.

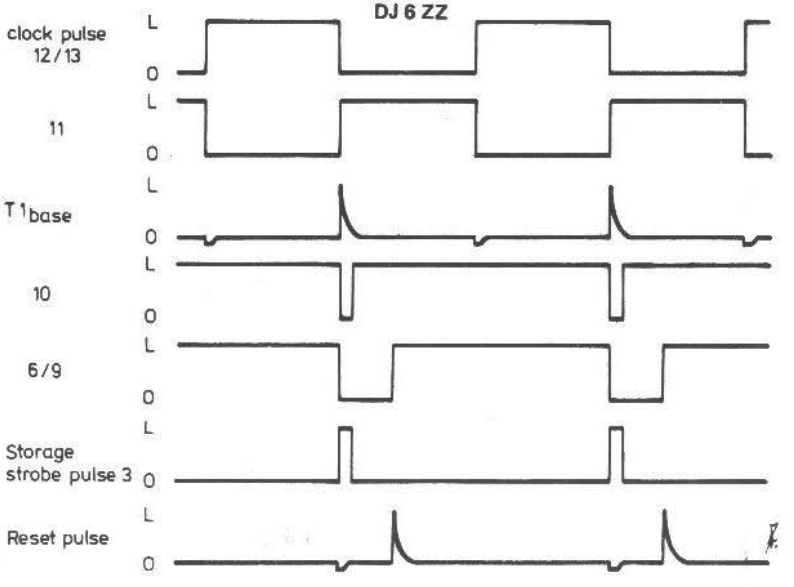

Fig. 3 b: Pulse diagram of the counter control pulses

Fig. 3b shows how the required delayed pulses are gained via several intermediate stages. The number at the commencement of each line indicates the connection pin of integrated circuit IC 8. The 1-0 slope of the clock pulse is changed into a new pulse by differentiating (22 nF; 2.2 kΩ), re-shaping (T 1) and is lengthened in a monoflop (gate 9/10 - 8 and 4/5 - 6). Its differentiated fall

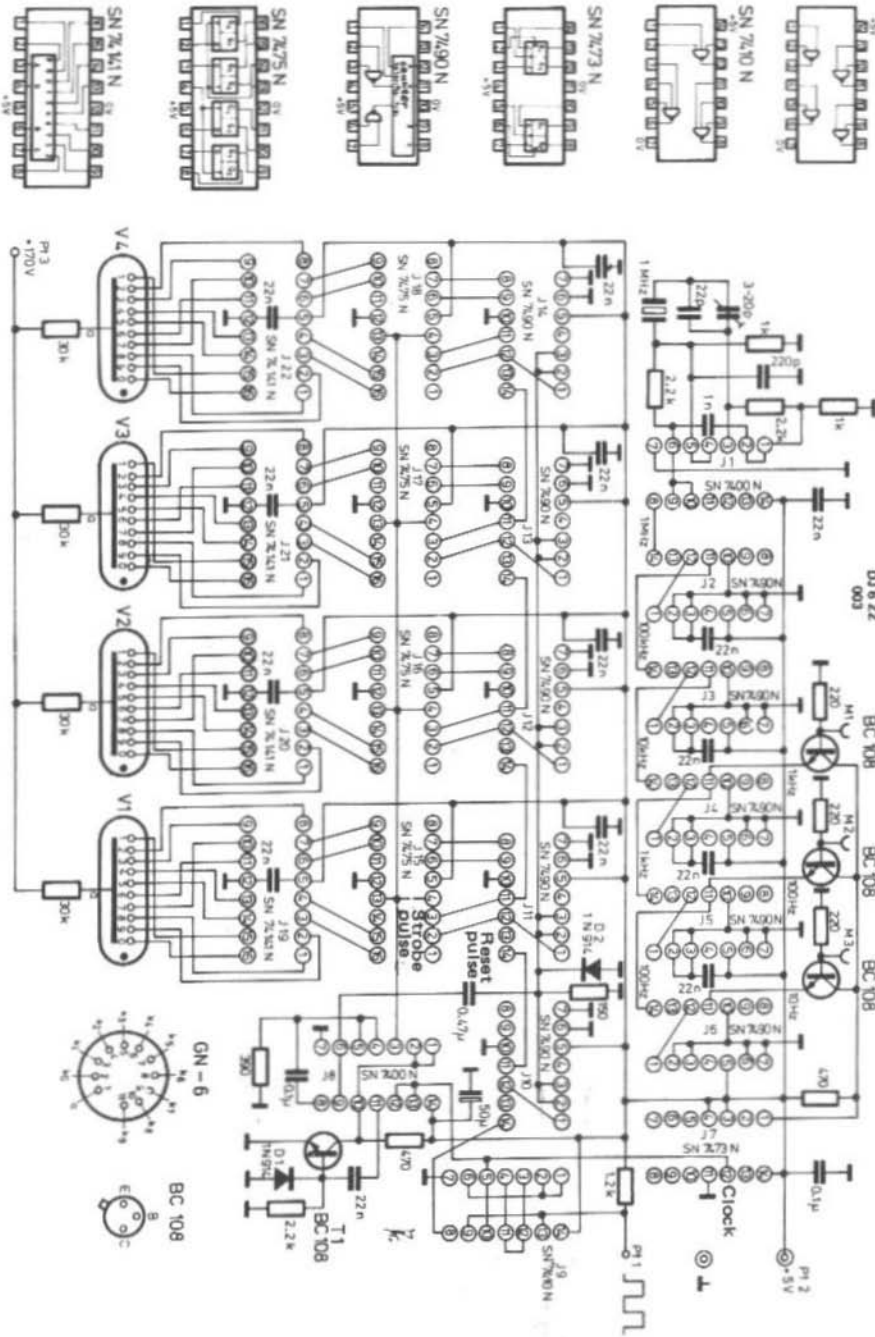

Fig. 4: Circuit diagram of the frequency counter module

slope represents the reset pulse for the counter which appears after the storage strobe pulse with respect to the counting time. The storage strobe pulse therefore appears before the reset pulse because it is taken before the delay monoflop.

2. CIRCUIT OF THE COUNTER MODULE

Due to the use of integrated circuits, the circuit diagram is reduced to a plan of the interconnections as shown in Figure 4. A diagram of the logic functions would have also been too extensive. However, the given logical circuits for the various integrated circuit types allow one to follow the logical functions if required. Figure 4 is especially useful for finding the measuring points on fault finding at a later date if this should be necessary.

2.1. COMPONENT DETAILS

The TTL circuits used in this frequency counter are offered by a large number of manufacturers under different designations. The author and the publishers used integrated circuits manufactured by Texas Instruments for their prototype models. The designations of TI are SN 74.. N. Other companies use the following designations:

AEG-Telefunken:	TL 74.. N	SGS:	TT μL 9...
SESCOSEM:	SFC 4.. E	Siemens:	FL 1 ..
ITT:	ITT 74.. N	Sprague:	US 74 .. A
National Semiconductor:	DM 8 ...	Philips:	FJ ...

IC 1, IC 8:	SN 7400 N
IC 2 - IC 6:	SN 7490 N
IC 7:	SN 7473 N
IC 9:	SN 7410 N
IC 10 - IC 14:	SN 7490 N
IC 15 - IC 18:	SN 7475 N
IC 19 - IC 22:	SN 74141 N (replacement for SN 7441 AN)

T 1 - T 4:	BC 108, 2 N 2926 or similar silicon NPN AF transistor
D 1 - D 2:	1 N 914 or other similar silicon planar diode
V 1 - V 4:	GN-6 (ITT), ZM 1080 (AEG-Telefunken) or similar types
1	standard frequency crystal 1.000 000 MHz, HC-6/U, with holder for horizontal PC-board mounting
1	trimmer capacitor 3-20 pF, 7 mm dia. miniature ceramic disc or foil trimmer
14	bypass capacitors 22 nF (value not critical), 7.5 mm spacing
2	plastic foil capacitors 0.1 μF. Spacing 15 mm
1	miniature disc or tantalium capacitor 0.47 μF. Spacing 7.5 mm (value not critical)
1	tantalium electrolytic capacitor approximately 50 μF; spacing 15 mm
5	DIP 14 sockets
2	DIP 16 sockets

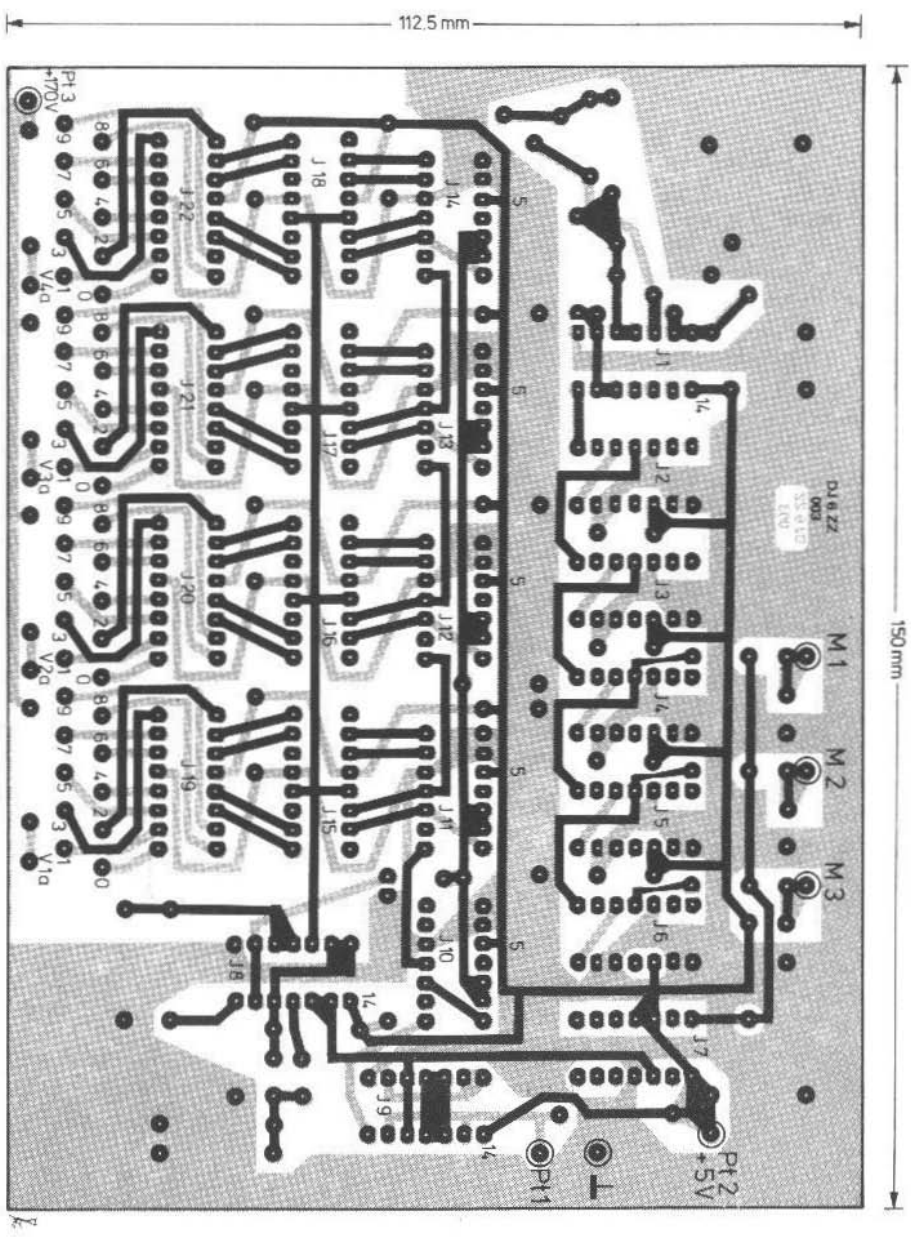

Fig. 5: Printed circuit board DJ 6 ZZ 003, double-coated with through contacts

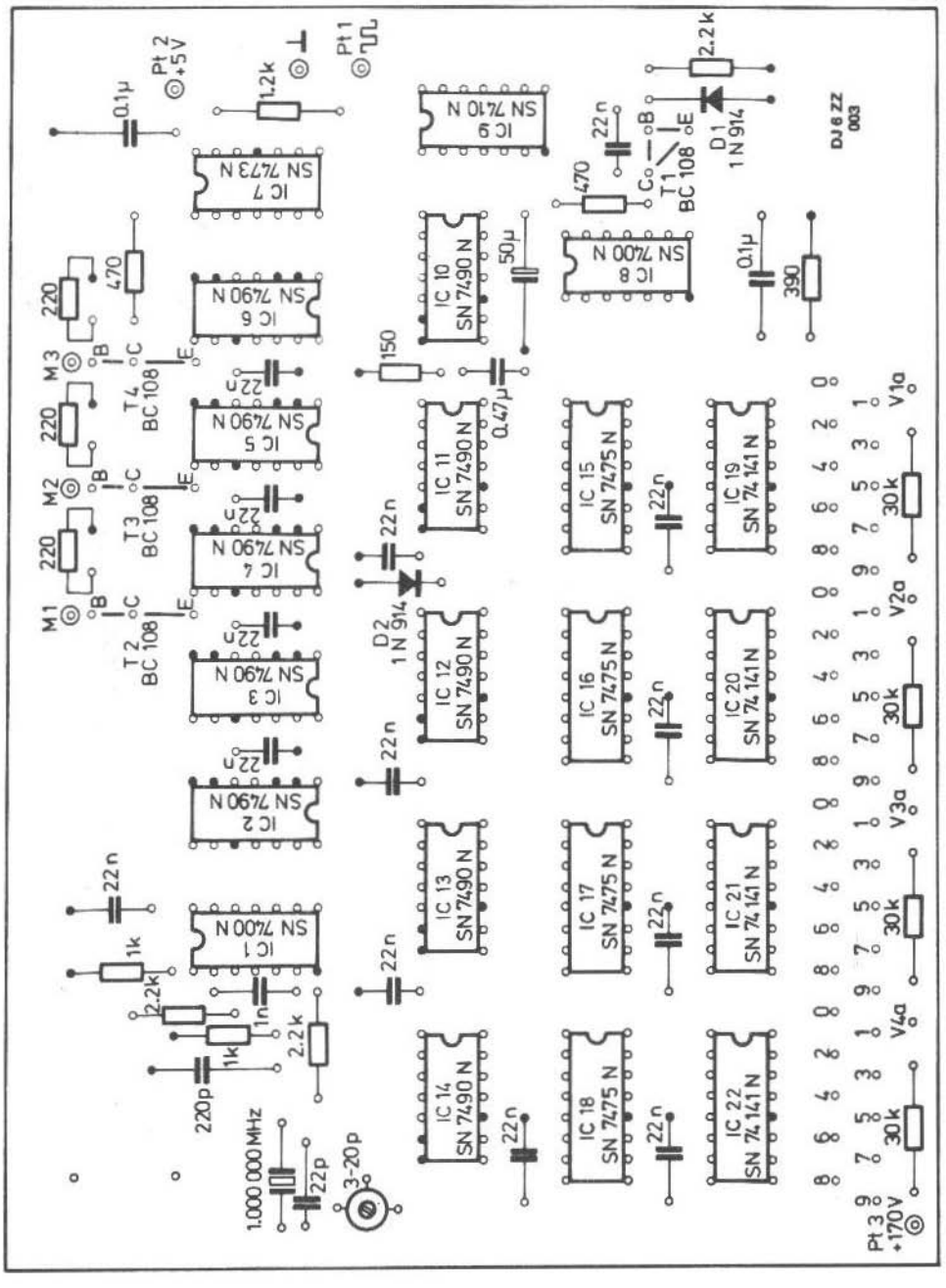

Fig. 6: Component location plan of DJ 6 ZZ 003

3. ASSEMBLY

The frequency counter module is built up on a double-coated printed circuit board with through-contacts having the dimensions 150 mm x 110 mm. The PC-board is designated DJ 6 ZZ 003. Figures 5 and 6 show the PC-board and the position of the components. A photograph of the prototype is given in Figure 7. The soldered connections that can be seen are due to the fact that the prototype board did not have through-contacts. It will also be seen that different bypass capacitors were used. This is not critical as long as a low value is followed by a higher one. If all values are too small, pulses can appear on the operating voltage which can lead to spurious effects.

The indicator tubes were directly connected to the board in the prototype. Of course, they can be connected via relatively long leads since they only handle DC-voltages that are switched at a maximum of 1 kHz.

Finally, it should be mentioned that for each IC-type (and the first counter decade) one was provided with a socket to allow the integrated circuits to be tested before soldering into place. The crystal oscillator (IC 1) is provided with a socket which allows IC 8 also to be tested. This is also true of the first frequency divider IC 2 for testing all the SN 7490 N types. Since the integrated circuit types used for IC 7 and IC 9 only appear once, each is provided with a socket. A socket should also be provided for the SN 7475 N and SN 7414 N types. The last socket is provided for the first counting decade (IC 10), so that one can select the fastest IC if a number of SN 7490 N ICs are available. The switching speed of the first decade determines the upper frequency limit of the whole frequency counter. Since the values fluctuate greatly (typical is 15 to 18 MHz), the selection is very worthwhile. Of course, it can only be carried out after the whole frequency counter is completely ready for operation.

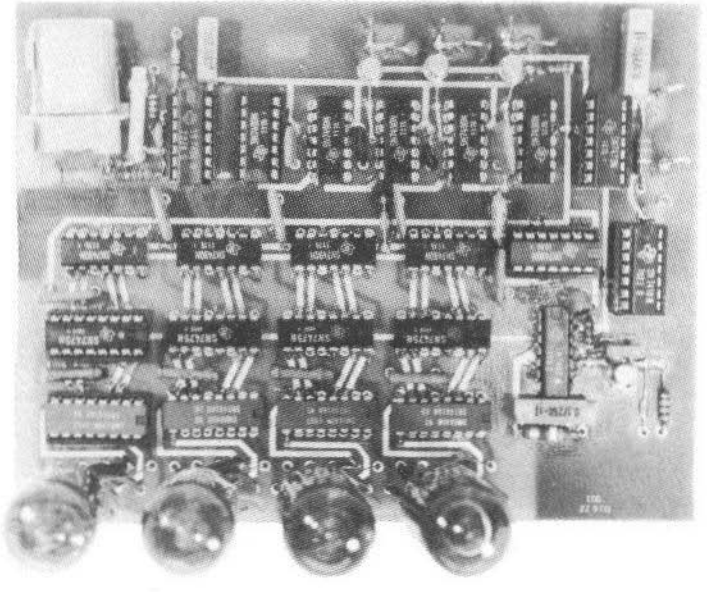

Fig. 7: Prototype of the frequency counter module

The frequency counter module only requires the few external connections shown in Figure 8. The transistor represents a simple limiter to change the more or less sinusoidal voltage of the input signal to steep squarewaves that can be processed by the counter. The diode protects the base-emitter path against overvoltages. The voltage of the signal to be measured is decreased to 2 V - 4 V peak to peak with the aid of the variable dropper resistor. This circuit can be easily built up on a Vero-type board if the connections are kept short. A wideband preamplifier up to 60 MHz with pulse shaper (2) is also described in this edition. If this preamplifier is used, the external pulse shaper shown in Figure 8 will not be required.

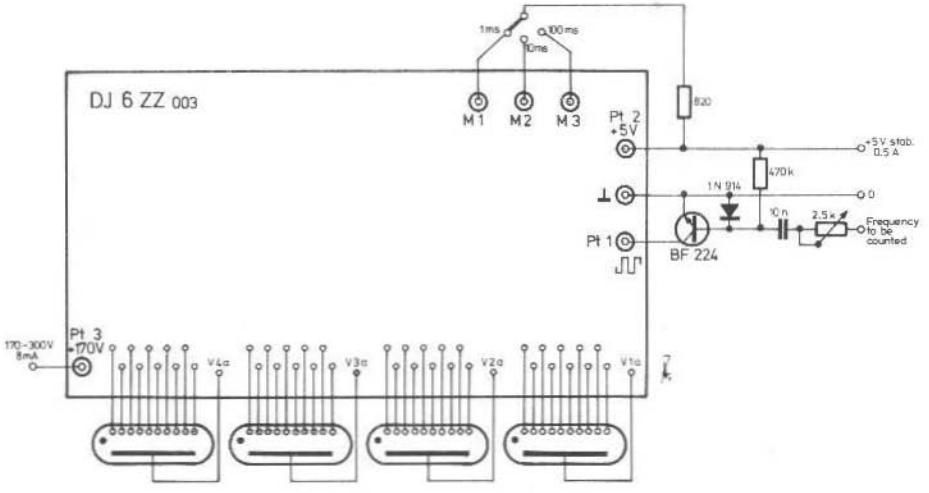

Fig. 8: Circuit diagram of the external connections

4. POWER SUPPLY

The frequency counter requires two operating voltages:

5 V + 0.25 V at 0.5 to 0.6 A
170 V to 300 V at 8 mA

As was previously mentioned, the integrated power supply described in (1) is very suitable. In fact it was developed for such an application. The author used the stabilizer circuit shown in Figure 9. It is not so extensive but the construction represents just as much work as the more extensive printed circuit construction with the integrated voltage stabilizer.

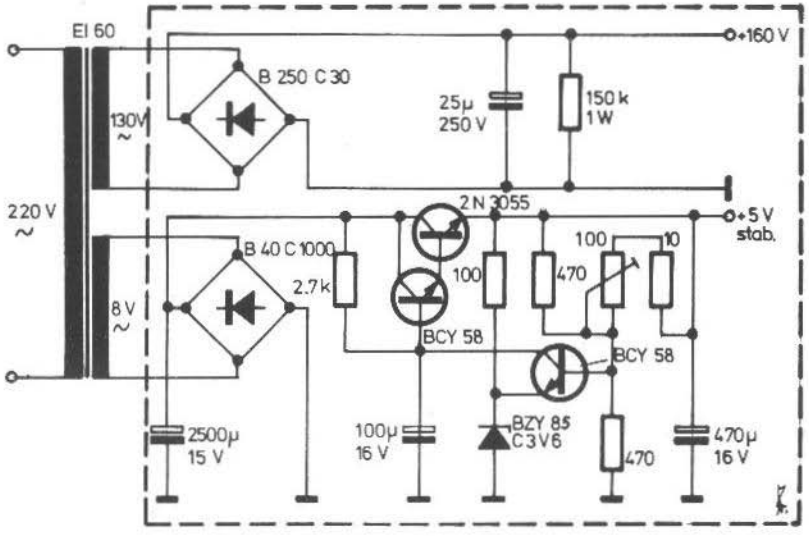

Fig. 9: Power supply circuit used by the author

5. CONNECTION AND OPERATION

Before connecting the frequency counter, the power supply voltages should be measured and adjusted where necessary. The dropper resistors for the neon indicator tubes should be calculated and inserted into the anode circuit of each tube.

The test procedure is commenced with the crystal oscillator which must be audible immediately on a receiver tuned to 1 MHz or a harmonic (e. g. 1 MHz, 7 MHz, 28 MHz or even 144 MHz) when a screwdriver is touching connection 8 of IC 1.

Place a second SN 7400 N into the socket of IC 1 and test. Place a SN 7490 N into the socket of IC 2. A 100 kHz calibration spectrum should now be audible when a screwdriver is touching connection 11 of IC 2.

All SN 7490 N integrated circuits can now be tested one after the other in the socket of IC 2. Solder IC 3, IC 4, IC 5 and IC 6 into place in the given order and observe the calibration spectrum.

The other stages can only be checked with the aid of an oscilloscope which need not be described here. The pulse diagram given in Figure 3 and the circuit diagram in Figure 4 aids the checking process.

The stages provided with sockets are the first that are activated after which all integrated circuits of the same type can be tested. If the components are working correctly, there is no reason why the frequency counter should not operate immediately due to the inherent reliability of the printed circuit board with its through contacts. However, when each stage is checked step by step, one will be better able to understand the operation of the counter.

Finally, a method of obtaining an indication of the decimal point is to be given: Three miniature neon lamps for 110 V are connected via a suitable dropper resistor to the anode voltage and grounded via a second wafer of the clock switch M1 to M3.

The lamps are then mounted between the numerical tubes so that the appropriate decimal lamp lights. However, since the amateur usually knows the frequency to be expected, e.g. the kHz and the 100 Hz when calibrating the scale of a VFO, the provision of a decimal point was not thought to warrant the extra cost.

6. AVAILABLE PARTS

The printed circuit board DJ 6 ZZ 003, the crystal standard, semiconductors (with first decade counter IC selected for 30 MHz), Nixie tubes and a complete kit are available from the publishers or their national representatives. Please see advertising page.

7. REFERENCES

(1) H. J. Franke and H. Kahlert: Universal Power Supply using an Integrated DC-Voltage Stabilizer
VHF COMMUNICATIONS 3 (1971, Edition 2, Pages 121 to 126

(2) W. R. Kritter: Preamplifier for Frequency Counters up to 60 MHz
In this edition of VHF COMMUNICATIONS

(3) D. E. Schmitzer: Basic Digital Circuits
In this edition of VHF COMMUNICATIONS

A NEW METHOD OF FREQUENCY MULTIPLICATION FOR VHF AND UHF SSB

by K. Meinzer, DJ 4 ZC

INTRODUCTION

This article does not represent a constructional description but more an introduction to a new method of frequency multiplying SSB signals. Single sideband operation has been gaining popularity on the VHF and UHF bands especially since amateur satellites and MOONRAY have proposed use of the 70 cm band for space communications.

Unfortunately the normal method of producing SSB signals by frequency conversion and linear amplification becomes increasingly difficult at higher frequencies due to the considerable amount of frequency conversion required and inherent problems of spurious conversion products and intermodulation.

A varactor diode represents a relatively simple and inexpensive means of multiplying CW signals to the UHF region but it is not possible to use this method in conjunction with SSB transmissions due to the inherent non-linearity. Conventional frequency multiplication is also impractical due to the inavoidable distortion of the SSB signal.

To avoid this problem, the author has developed a method of frequency multiplication that allows a varactor diode to be used together with a relatively simple adapter to allow SSB transmissions to be multiplied to 432 and 1296 MHz. This system has been constructed and used on the air with excellent results. It can be used with any exciter that provides a shortwave SSB signal, in our case 9 MHz. The original SSB signal is modified by the adapter in such a manner that after it has been tripled in frequency the output signal will have been restored to a conventional SSB signal.

1. THEORY OF OPERATION

As has already been mentioned, it is known that amplitude modulated signals are distorted greatly by conventional frequency multiplication. Frequency multipliers are usually class C amplifiers which possess a non-linear relationship between the input and output voltages. It is true that the third harmonic of an amateur AM signal will still be readable, although highly distorted. However, the complexity of a single sideband signal will make it unintelligible after conventional frequency multiplication.

To explain the technique let us assume an SSB transmitter with a carrier frequency of 7000 kHz transmitting the upper sideband. If the transmitter is modulated by an audio generator that can be switched between 1 kHz and 3 kHz, the resulting SSB signal will be transmitted on either 7001 kHz or 7003 kHz as shown in Figure 1a.

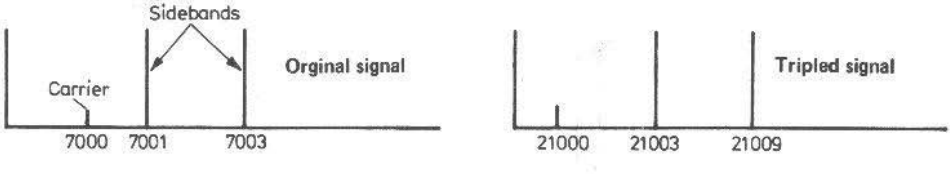

Fig. 1: Effect of frequency multiplication on the sideband frequencies of audio tones

After reinserting the carrier, the 1 kHz or 3 kHz tone is recovered as the heterodyne between the sideband and the reinserted carrier. If this signal is now passed to a frequency tripler, the frequencies will be 21003 kHz or 21009 kHz as shown in Figure 1b. When the carrier is now reinserted heterodyne frequencies of 3 kHz and 9 kHz result. This is because the audio frequencies are also multiplied together with the carrier frequency and the spacing between sideband and carrier will also have been tripled.

If we continue this experiment further by tuning the audio oscillator continuously between 1 kHz and 3 kHz, we will notice that the sideband signal will also change in frequency. This shows that the SSB signal can essentially be considered as an FM signal with a frequency deviation of 2 kHz. If the SSB signal is now passed through a limiter to remove the amplitude components, the result will be a signal only containing FM information which is not the original audio signal but a complex result of the SSB generation process.

If the amplitude variations are demodulated before limiting, the envelope can be used to remodulate the FM signal with the AM components to reform the original SSB signal as shown in Figure 2a.

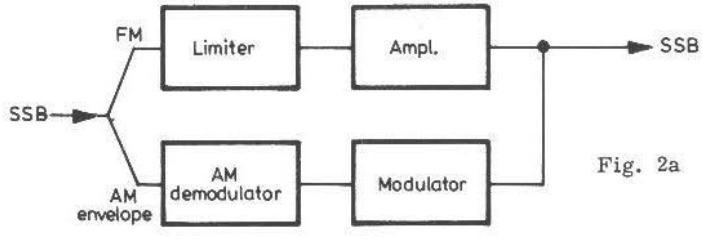

Fig. 2a

Fig. 2: Separation of the SSB signal into its FM and envelope components

The demodulated signal is not the original audio signal but the envelope of the SSB signal, which is the signal heard when listening to a SSB signal on a receiver without BFO. The AM envelope signal contains frequencies between DC and 20 kHz.

It has already been seen that a frequency multiplier also multiplies the frequency deviation of an FM signal, thus destroying the relationships of the original signal. However, if the SSB signal is considered to be a combination of amplitude and frequency modulation, the process shown in Fig. 2b can be utilized. After separating the two components, the FM portion is passed via a frequency divider where both our 9 MHz signal and the frequency deviation are divided by three. The result is a 3 MHz signal whose frequency deviation is one third of that of the original signal. This 3 MHz FM signal is now amplitude modulated with the original envelope signal and passed to a mixer stage where it is converted back to the original frequency of 9 MHz with the aid of a 12 MHz local oscillator frequency. The resulting signal is, of course, not the original 9 MHz signal since the frequency deviation is now only one third of the original value. The output signal is now heterodyned in the conventional manner to one third of the required operating frequency, e. g. to 144 MHz for 70 cm or to 432 MHz for 23 cm operation. The heterodyne frequency is then tripled in a varactor or other frequency multiplier after which an output signal will be provided that can hardly be distinguished from a conventional SSB signal.

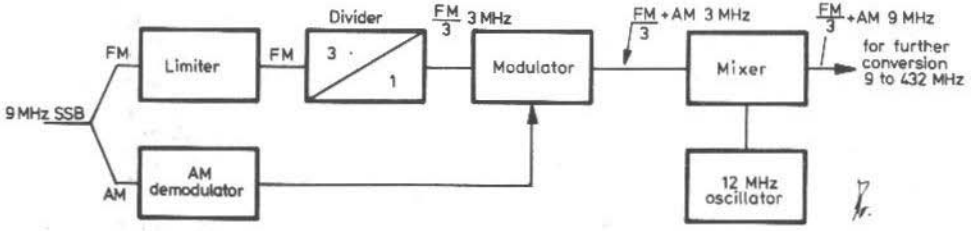

Fig. 2b

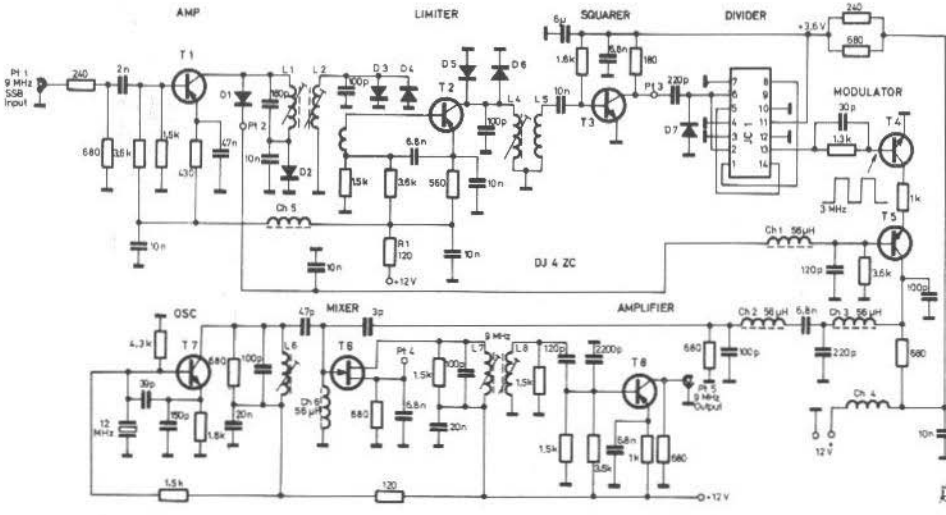

Fig. 3: Practical circuit of the DJ 4 ZC SSB adapter

2. CIRCUIT DETAILS

A practical circuit of such an SSB adapter for use in conjunction with one tripler stage is shown in Fig. 3. A 9 MHz SSB signal is fed at approximately 0.1 V to the input of the adapter (Pt. 1) after which it is amplified in transistor T 1 to roughly 5 V. At this point, the signal is demodulated by diode D 2 to separate the AM-envelope signal; diode D 1 is used to provide a bias voltage for the modulator transistor T 5.

Part of the amplified signal is induced from inductance L 1 to L 2 and limited by diodes D 3 and D 4. After further amplification in transistor T 2, the signal is limited once again by diodes D 5 and D 6. The resulting signal is then passed to transistor T 3 where it is transposed into a square waveform and passed to the integrated circuit IC 1, a dual JK flip-flop that divides the square wave signal by three. Transistor T 4 is an electronic switch controlled by the 3 MHz square wave (FM) signal. The current flowing via transistor T 4 is modulated by the voltage at the base of T 5 which is the envelope component of the original 9 MHz SSB signal.

After this modulation the signal is passed via a low-pass filter in the collector circuit of transistor T 5 to suppress the third harmonic (9 MHz) of the 3 MHz composite signal. The signal is now fed to mixer transistor T 6 where it is heterodyned with the 12 MHz oscillator frequency of T 7 to reobtain the required output frequency of 9 MHz. The signal is amplified in transistor T 8 to the original level of 0.1 V or more. Of course, this signal is still not an intelligible SSB signal until the composite FM/envelope signal is tripled.

3. CONSTRUCTION

As was mentioned in the introduction, this article is not a constructional description. The author built up the described adapter on a chassis made from epoxy PC-board material having the dimensions 57 mm x 140 mm.

3.1. COMPONENTS

D 1 and D 3 to D 7: 1 N 914 or similar
D 2: AA 112 or any germanium video detector diode

T 1, T 2, T 8: Germanium PNP transistor for RF e.g. AF 106, AF 121, AF 139 (AEG-Telefunken); or Motorola HEP-3
T 3, T 4, T 5, T 7: VHF NPN transistor, e.g. 2 N 706, 2 N 708 or similar
T 6: N-channel FET BF 245c (TI Germany) or MPF-102 (Motorola)

IC 1: Dual JK flip-flop (Motorola MC-7908)

Ch 4: Ferrite bead choke (3 beads); Ch 5: Ferrite bead

All coils are 0.3 mm dia. (28 AWG) enamelled copper wire, wound on 1/4" (6.5 mm) coilformers with cores.

L 1: 16 turns
L 2: 22 turns; coupling link two turns
L 3: 22 turns; coupling link four turns
L 4: 16 turns
L 5, L 6: 22 turns

Coil-to-coil spacings: L 1 - L 2 : 5/8"; L 5 - L 6 : 1/2"

4. ALIGNMENT

The alignment procedure is very simple: Connect a voltmeter between Pt. 2 and ground and align inductance L 1 for maximum reading with a low 9 MHz input signal. A voltage of 5 V should not be exceeded at testpoint Pt 2, since this would exceed the linear range of the demodulator. An oscilloscope or valve voltmeter (VTVM) is now connected to testpoint Pt. 3, and the input signal is reduced until the reading is only just readable. Align L 2 and L 4 for maximum indication by reducing the input signal and correcting the alignment until no further increase in gain is obtained. The measuring arrangement is now connected to Pt. 4 and inductance L 6 aligned for maximum indication. With a medium 9 MHz signal at the input, L 7 and L 8 are aligned for maximum 9 MHz signal at the output Pt. 5.

5. RESULTS

The adapter is then ready for operation with a transmitter having one varactor or other frequency tripler stage to restore the original characteristics of the SSB signal. It should be noted that the adapter inverts the sideband so that if

the upper sideband is to be used, the input signal should be lower sideband and vice-versa. The described adapter has been successfully used by the author in conjunction with a 432 MHz SSB transmitter whose output frequency was then tripled to 1296 MHz. The third order distortion of the whole transmitter system was measured to be -25 dB. It was reported that the signal sounded completely normal.

6. EDITORIAL NOTES

This is most certainly not the last that will be written about frequency multiplication of SSB with separated FM and envelope components, especially when one considers even greater division of the FM components. For instance, when dividing by nine, it would be possible to multiply the output signal of a two metre SSB transmitter to 1296 MHz using just two varactor or other triplers. Of course, the principle is not just limited to triplers so that it would be possible to multiply the output signal of a two metre SSB transmitter to 2304 MHz with a few varactor diodes and appropriate division of the FM-components (by 16). The important thing is that the linear amplification is made at frequencies where this can be made efficiently and linearly which is increasingly difficult on the higher UHF bands.

7. REFERENCES

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A TRANSISTORIZED POWER AMPLIFIER FOR TWO METRES USING THE 2 N 3632

by H. J. Brandt, DJ 1 ZB

This article is based on a lecture given by the author at the Weinheim VHF Conference.

1. INTRODUCTION

The first transistor system manufactured in the overlay technology appeared on the market in 1964/65. It was available in three versions: in a TO 60 case as type 2 N 3375, in a TO 39 case as 2 N 3553 and finally with two parallel-connected systems in a TO 60 case as 2 N 3632. Of course, the parallel connection of two transistor systems is the easiest method of increasing the power rating; however, the reliability of such configurations is doubtful since the exact symmetrical current distribution to both systems cannot be guaranteed. It is true that a type with increased reliability, the 2 N 3623 was developed, however, even this type did not receive MIL approval.

This and the fact that overlay transistors are now manufactured by a number of companies have resulted in favourable offers appearing occasionally for radio amateurs. However, power transistors in this range require entirely different circuitry than known for tube amplifiers. This requires a great deal of rethinking, and this is one of the reasons for bringing this article: To explain the different conditions that exist with transistorized power amplifiers. The second part of this article will describe a two-stage power amplifier equipped with a transistor 2 N 3632 in the output stage, as well as modulation and auxiliary circuits.

2. NOTES REGARDING THE SPECIFICATIONS

2.1. LIMITS FOR OPERATING VOLTAGE AND POWER

Modern RF power transistors are designed for operating voltages of either 12 V to 13.5 V or 24 V to 28 V since they were mainly developed for applications in the mobile radio service. Besides this, former types exist with operating voltages in the order of 40 V. Of course, it is easier to achieve higher power levels at higher operating voltages. In addition to this, the gain per stage is greater at these higher voltages. For physical reasons, however, the higher the transit frequency, the lower will be the permissible operating voltage (1). At the moment, 40 V can be considered to be the upper limit for VHF/UHF transistors.

High power levels can therefore only be obtained in conjunction with high current values. This, however, means that the output impedance drops to a few ohms. For several reasons, the maximum power level that can be achieved favourably with a single transistor is in the order of 100 W in the HF/VHF range and 20 to 50 W at UHF. Higher power levels can only be realized by combining several individual, or push-pull amplifiers. Besides the heat dissipation problems arising with such power amplifiers, which can be extremely extensive, further electrical and constructive difficulties are caused because all leads must be kept at an absolute minimum because of the low impedance operation.

In the application in question, a certain similarity to high-energy electrical engineering exists: were high power levels are more favourably obtained by increasing the voltage within certain practical limits. It is therefore not a step in the wrong direction but recognition of the facts when tubes are given priority in this range. A tube also requires a far lower drive power for the same output. The combination of a transistorized exciter and a tube power amplifier has been found to be the best solution by a number of leading companies for the immediate future (2).

2.2. OUTPUT POWER AND POWER DISSIPATION

The maximum output power P_o of a transistor amplifier is given by the following formula:

$$P_o = \frac{U_c - U_{c\,res}}{4} \times I_{c\,peak} \qquad (1)$$

where: U_c is the operating voltage (U_{CE} or U_{CB}), $I_{c\,peak}$ is the peak collector current to which the transistor can be driven at the operating frequency and $U_{c\,res.}$ is the residual collector voltage at this current (including the voltage drop across any emitter resistors).

As can be seen, the power dissipation is not given in the formula; it is only dependent on the efficiency that can be achieved in each mode of the amplifier.

In principle, the same is also valid for tubes. However, the limit values of current and voltage cannot be obtained because the permissible dissipation will be reached beforehand. This means that the output power of tubes can be well estimated from the power dissipation values.

The opposite is true for transistors. The permissible dissipation power cannot be utilized because the voltage and current limits are firstly reached. As a rule, the dissipation power of RF power transistors is usually selected as great as the power input in practice, for reason of breakdown capability.

This is very unfavourable for those countries where the power limits of the radio amateur licence are based on the power dissipation of the final amplifier stage, because higher power levels can be achieved at the same power dissipation values with tubes than with transistors. Even the stipulation of the power dissipation at 70 °C instead of 25 °C does not represent a great improvement. This is the reason why extensive discussions are taking place in a number of countries to find a more favourable means of stipulating the power limit in accordance with modern technology.

2.3. EFFECT OF THE OPERATING LOAD RESISTANCE

The optimum operating load resistance Rc of a transistor amplifier can be determined in two ways:

$$R_c = \frac{2 \times (U_c - U_{c\,res})}{I_{C\,peak}} \qquad (2)$$

$$R_c = \frac{(U_c - U_{c\,res})^2}{2 \times P_o} \qquad (3)$$

According to the data sheet, the transistor 2 N 3632 is designed for a minimum output power of 13.5 W at 175 MHz and an operating voltage of 28 V. A drive power of 3.5 W is required. If a drive power of only 2.5 W, which can be sidered, the following values will result according to formula 1 and 2 assuming a residual voltage of 4 V:

Peak current $I_{c\ peak}$	2 A
Operating load resistance	24 Ω
Operating load resistance of the driver	115 Ω
Real component of the input impedance according to data sheet	5 Ω

Figure 1 provides an idea of the drive conditions of the collector voltage-current characteristics. The collector voltage of 28 V is driven down to the residual voltage of 4 V (accentuated sinusoidal curve) during the conduction period of the drive. In the non-conduction period (class C), it will increase up to a minimum of 52 V (28 V ± 24 V) due to the flywheel effect of the tank circuit. The position of the load line R_c is determined by the operating voltage and the peak current value of 2 A.

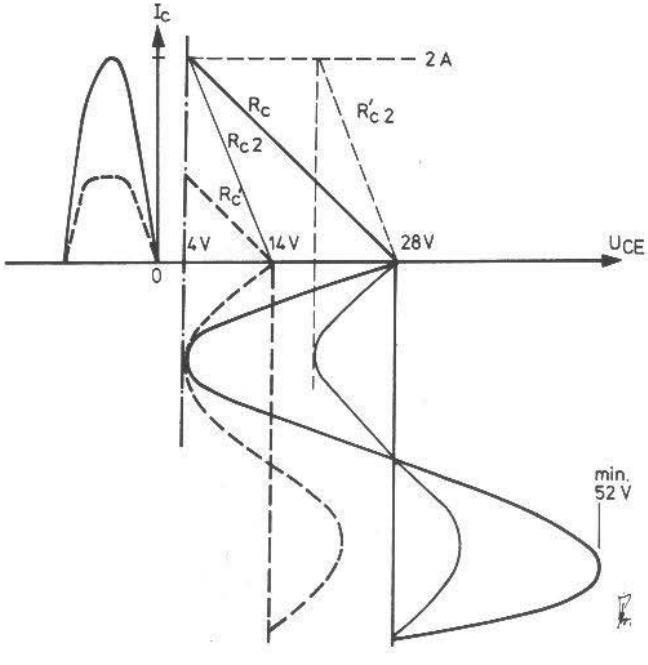

Fig. 1: Diagram of the dynamic characteristics and drive in the I_C/U_{CE} family of curves

If the operating voltage is amplitude modulated at a mean value of 14 V (dashed line), the slope of the load line will be maintained (R_c). This means a depression of the current flow and the alternating voltage at the collector at all voltages lower than 28 V which means that collector voltage modulation can be compared with a limiting process.

If the amplifier stage is aligned for maximum output power at 14 V, the slope of the load line will increase ($R_{C\ 2}$) due to the possibility of a peak current of 2 A. The result of this is a higher carrier power level. Since the slope gradient remains during modulation ($R_{C\ 2}$), no increase of the alternating voltage at the collector will occur on momentarily increasing the DC collector voltage to 28 V and the power will hardly increase above the carrier power level.

This is the reason for the well known negative modulation effect; a second cause is insufficient drive. If the drive is only sufficient for 1 A peak current, it is of course possible to align with a load resistance of $R_C = R_C$ to the correct carrier level at 14 V. However, if the collector voltage is momentarily increased to 28 V during modulation, still no increase of the alternating voltage at the collector will occur because the peak current cannot exceed 1 A.

In order to avoid this source of error during the alignment of stages whose collector-voltage is modulated, it is advisable to align them under modulation whilst observing the envelope. It is also possible to disconnect the modulator and to increase the operating voltage of the stage(s) to be modulated to twice the value. It is then possible for the alignment to be made at the peak carrier level. This problem does not exist if the collector current is modulated instead of the collector voltage. In this case, the alignment is always made at peak carrier level.

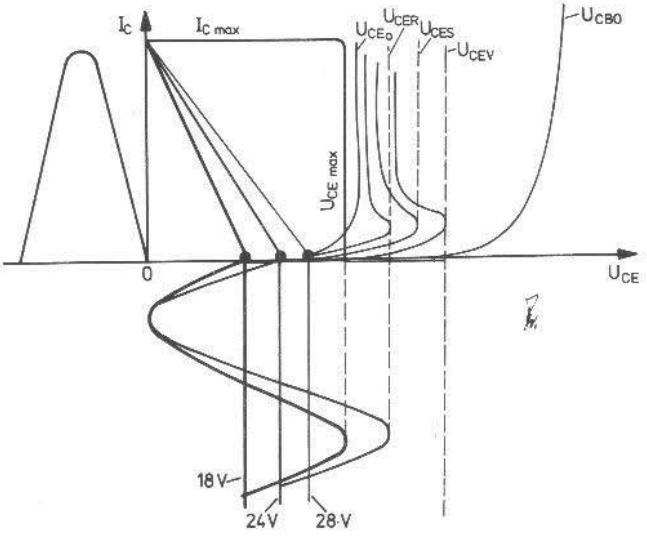

Fig. 2: Breakdown voltage and utilization of the maximum voltage

Figure 2 illustrates the voltage and current utilization of an RF power transistor in comparison with its breakdown characteristics. Fundamentally speaking, the danger of breakdown is greatest at DC and low frequencies (3).

Above a frequency, which is dependent on the construction and the transmit frequency of the transistor, the operating point can take up any position within a rectangular field on the collector voltage-current characteristic without endangering the transistor system. The field is limited by the permissible peak current $I_{C\ max}$ and the breakdown characteristic for U_{CEO}, e.g. at values of 3 A and 40 V for transistor type 2 N 3632. In the shortwave range, this transistor can therefore only be used at an operating voltage of 18 V (accentuated curve) in order to ensure that the breakdown voltage is not exceeded. However, since the breakdown voltage is lower at low current values and since the base is driven in a negative direction whilst the collector has its highest momentary value under correctly aligned conditions, the voltage U_{CER} can be regarded as the breakdown limit.

In this case, the operating voltage may amount to approximately 24 V and it is possible to obtain slightly more output power by carefully trimming. However, this correction could endanger the transistor if it is possible that the collector stage is incorrectly aligned (e.g. by maloperation, disconnection or a short circuit of the antenna). The phase relationship between the alternating voltage at the base and collector is then altered which means that the breakdown characteristic U_{CEO} is valid again. Furthermore, in class C, the operating line will form an area under the curve shaped like a rounded rectangle. At an operating voltage of 24 V, this area exceeds the rectangular field of the operating range and the transistor will be destroyed within milliseconds (4).

There are circuits that react to incorrect alignment and are able to reduce or stop the drive within microseconds so that the transistor system is not destroyed. However, since the power gain achieved by increasing the operating voltage represents only fractions of an S-point, it is simpler to return to an operating voltage of 18 V where the transistor is able to withstand any incorrect alignment even under full-drive conditions.

If RF power transistors are operated in the vicinity of the transit frequency, another effect can be utilized: Namely, the breakdown voltage U_{CEO} increases by the same measure as the reduction in current gain on increasing the frequency occurs. It can reach twice the static value (5). For this reason, it is possible for the transistor 2 N 3632 and similar types to be used in the VHF and UHF range at an operating voltage of 28 V inspite of the relatively low breakdown voltage U_{CEO} However, if the circuit were to break into oscillation at lower frequencies, the transistor would be destroyed instantaneously because a lower breakdown voltage will then be valid. An exact neutralization is therefore not only a matter of suppressing spurious signals but is of fundamental importance with regard to the reliability of the circuit.

3. DIMENSIONING OF THE CIRCUIT

3.1. THE RESONANT CIRCUITS

The resonant circuits in a transmitter must fulfil two demands: They must firstly suppress spurious signals and secondly provide a matching between individual stages, and to a consumer (antenna). As a compromise between selectivity and attenuation, a Q of approximately 10 is selected for tubed equipment, e.g. the values of L and C are chosen so that their reactive impedance is 1/10th of the value of the operating load resistance R_C. The value of R_C is calculated according to formula 2 and 3 (6).

If the same procedure was used with transistorized transmitters, a capacitance of 450 pF and an inductance of 2.5 nH would result at an operating load resistance of 24 Ω for the 2 N 3632 on the two metre band. Since 1 mm of wire already amounts to an inductance of approximately 1 nH, such a parallel circuit is completely impossible. There are also other reasons against the use of such circuits.

Firstly, only impedances of less than 24 Ω can be taken from this circuit, which means that coaxial cables cannot be matched.

Secondly, the voltage-dependent collector-base capacitance of a fully driven transistor will detune the parallel circuit periodically. This means that there is a danger of parametric oscillation (7) that can lead to the production of spurious signals. With amplitude modulated transmitters, additional problems occur from modulation-dependent mismatch as well as unwanted phase modulation.

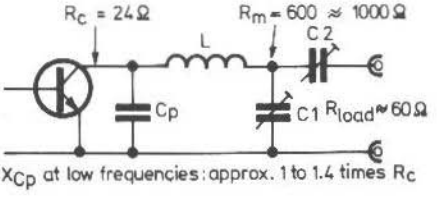

Fig. 3: Output circuit arrangement for RF power transistors

These difficulties can be avoided if the circuit given in Figure 3 is used. In this arrangement, the operating load resistance of the transistor (2 N 3632 = 24 Ω) will be increased by a factor of 25 to 50 to the higher value R_m. R_m is at the "hot" point or highest impedance position of the circuit. Trimmer capacitor C 1 is used for aligning the circuit to resonance. R_m is matched to the load R_L with the aid of the series capacitor C 2; unfortunately, the adjustment of this capacitor shifts the resonance which means that the adjustment must be corrected with capacitor C 1. The inductivity of the connections, which are unavoidable in practical circuits, is included in the total inductance of the circuit and is therefore also aligned during this process.

A capacitance C_p is always present at the output of the transistor. It takes over the current of the resonant circuit during the period when the transistor is blockedby the negative amplitude of the drive signal (class C). If this was not the case, a voltage would be generated across inductance L which is far in excess of twice the operating voltage and could therefore easily destroy the transistor system. The reactive impedance of C_p should be 1 to 1.4 times the operating load resistance R_c of the transistor in question - as given in formula 2 or 3. With such circuit dimensioning, which has proved itself on shortwaves, capacitance variations of the transistor have virtually no effect on the resonance of the circuit.

If the transistor is used in the vicinity of its transit frequency, it is advisable to reduce the value of capacitor C_p experimentally in order to increase the output power and efficiency. Whether C_p can be omitted completely, as is often the case with prototype circuits, must be carefully established experimentally.

Continuous tunability, absence of parametric oscillation, dependence of the alignment on the operating voltage (e.g. the ability to accept modulation), the harmonic suppression, and the stability under misaligned conditions are criteria that pay an important part in the dimensioning of this capacitor.

Peak voltages of three to four times the operating voltage will occur at the collector on reducing the value of C_p (5). This will be permissible due to the high breakdown voltage in this frequency range so that the observations made to Figures 1 and 2 must be extended. This voltage increase is, according to (8), the prerequisite for a high efficiency in the vicinity of the transit frequency.

This is because a low current angle can no longer be assumed since amplification of the harmonics required for this does not take place. According to (8) again, it can be theoretically determined that a high efficiency can be obtained by placing a distorted voltage across a series-resonant circuit. Without C_p, the collector voltage is far from sinusoidal. It is possible in this manner for efficiencies of 70% and more to be attained. The designer of the circuit must decide whether the efficiency is of primary importance, or whether it is more favourable to reduce it to 60% or 50% with a capacitance C_p in order to improve other characteristics.

The operation of the resonant circuit shown in Fig. 3 is based on the principle of a so called reactance transformer (Fig. 4a). A source resistance R_s can be transformed to the greater output resistance R_{out} by suitable selection of the reactive impedances X_L and X_C. The following is valid:

$$\frac{R_{out}}{R_s} = Q^2 + 1 \qquad (4) \qquad Q = \frac{X_L}{R_s} = \frac{R_{out}}{X_c} \qquad (5)$$

Q is therefore the relationship of reactive to actual power in the circuit and also a measure of its selectivity (bandwidth). Usually, it is necessary to increase the selectivity without changing the transformation factor which is dependent on the Q-value. There are two ways of achieving this aim: The easiest is to introduce a series-resonant circuit in series with the inductive, reactive impedance X_L (Fig. 4b). The two inductive components are then combined to form one inductance (Fig. 4c). It should be noted that the highest impedance point, of the circuit is between inductance L and trimmer capacitor C_s which means that it is advisable for the stator connections of the capacitor to be connected to the inductance.

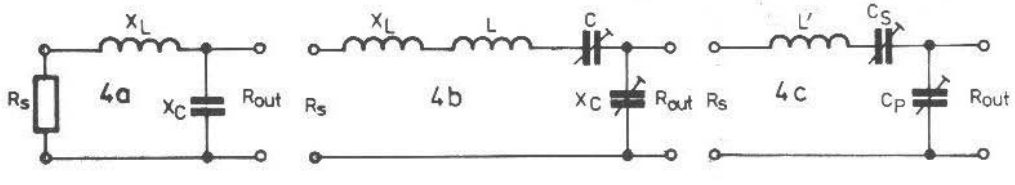

Fig. 4: Operation and dimensioning of the reactance transformer

A second method of increasing the selectivity is by combining two reactance transformers. One value Q_1 is used to transform higher than is actually required. The second portion is provided with such a Q-value (Q 2) that the required output resistance value is obtained. In practice, this would result in a rather unhandy circuit with two inductances (Fig. 5a). The two capacitors in the centre could be replaced by one trimmer capacitor. The circuit is unavoidable if the source resistance R_s and the output resistance R_{out} only differ slightly from another. In this case, the circuit is usually provided with a series or parallel capacitor at the output.

With a reactance transformer, it is possible for the positions of the inductive and capacitive components to be exchanged (Fig. 5b). If R_s is greater than R_{out}, the parallel circuit of X_{C1} and X_{L2} will be inductive and a circuit with two inductances will result (Fig. 5c). If, on the other hand, R_s is smaller than R_{out}, the parallel circuit will be capacitive, and a circuit with one inductance and two capacitors will result. The latter can be used for matching the operating load resistance (Fig. 5d).

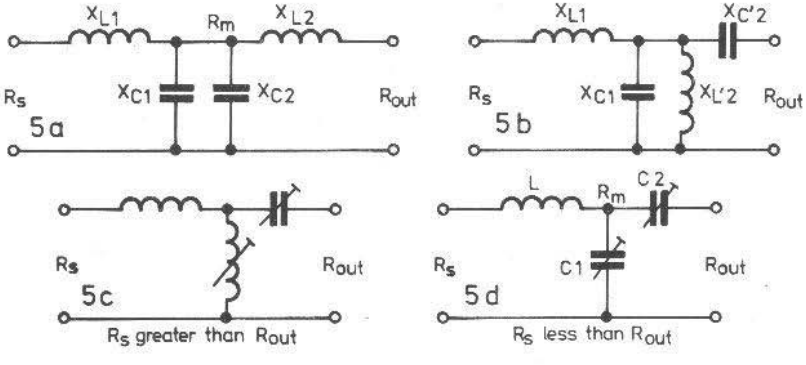

Fig. 5: Two interconnected reactance transformers for increasing the selectivity

The calculation of the circuit components in Fig. 5d is made in the following manner: The values of resistance R_s and R_{out} are, of course, already known. According to the required selectivity, a Q-value for Q 1 is selected - usually in the range of 4 to 10. This means that the medium resistance point R_m (Fig. 3) is already defined according to:

$$R_m = R_s \times (Q_1^2 + 1) \qquad (6)$$

Q 2 for the downward transformation is obtained from the following equation:

$$Q_2 = \sqrt{\frac{R_m}{R_{out}}} - 1 \qquad (7)$$

The reactive resistance of the series capacitor C 2 is then:

$$X_{C2} = R_{out} \times Q_2 \qquad (8)$$

the reactive resistance of the parallel capacitor C 1:

$$X_{C1} = \frac{R_m}{Q_1 - Q_2} \qquad (9)$$

and the reactive resistance of inductance L: $X_L = R_s \times Q_1$ (10)

If the frequency is known, the inductance and capacitance values can be calculated from the reactive resistances determined in formulas 8, 9 and 10. The addition of capacitance C_p, corresponding to the basic circuit shown in Figure 3, results in a slight increase of the adjacent series reactive resistance X_L which however is hardly of importance.

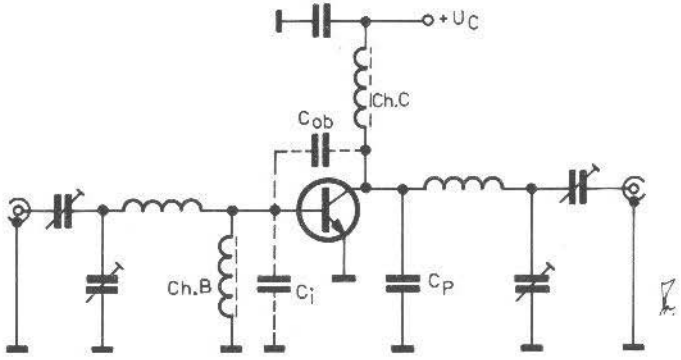

Fig. 6 a: Circuit of a typical transistorized power amplifier

The circuit of a typical transistor power amplifier is given in Figure 6a. The output circuit corresponds to that given in Figure 3. For matching to the input, the arrangement given in Figure 5d is turned around and used because the input resistance of transistors of this power level is lower than the operating load resistance of the driver stage or the impedance of an RF cable. The collector DC voltage is fed via choke Ch C and the base is grounded via Choke Ch B. For VHF/UHF operation, the emitter is directly grounded with a minimum of inductivity. In the shortwave range, some form of current limiting, e.g. in the form of an emitter resistor is usual required due to the increased danger of breakdown. In the VHF/UHF range, and with increasing emitter current, it becomes more and more difficult to realize a sufficiently low-inductive bypassing of the emitter. Modern RF power transistors are therefore provided with integrated emitter resistors so that the external emitter connection can be directly grounded. If an additional bias voltage is to be introduced for class C, this can also be obtained by placing a resistor in the base current circuit (3).

3.2. PARASITIC OSCILLATION

One of the most difficult problems with transistor transmitters is the complete elimination of parasitic oscillations. Even recent descriptions with their complicated alignment procedures show that a satisfactory solution must still be found.

It will be seen from the repeated mentioning of the shortwave bands that the author mainly gained his experience in this frequency range. The "DC" bands possess a greater relative bandwidth than the 2 m band which means that the tuning elements of the transmitter must be accessible externally. This resulted in the necessity that any tendency to parasitic or parametric oscillation be counteracted by suitable circuitry effectively enough for five bands that it is possible to tune easily for maximum meter reading, as is the case with tubed equipment.

If a transmitter is modulated with a voltage that is rich in harmonics (e.g. squarewave or sawtooth), side frequencies will be generated on both sides of the carrier whose distance from another corresponds to the fundamental frequency of the modulation signal. The conditions here are similar to that of a calibration spectrum generator. If such a signal is observed in a panoramic receiver or spectrum analyzer, these signals will be observed as vertical lines on both sides of the carrier, whereby the amplitude of the carrier and neighbouring lines will be greatest. The total bandwidth of the spectrum is dependent on the frequency, on the harmonic contents of the modulating signal and on the selectivity of the subsequent RF circuits. In the VHF range, a bandwidth of 10 MHz and more is possible.

In tubed transmitters, such an effect will only be present when, for instance, the modulator is oscillating at ultrasonic frequencies. With transistor transmitters, however, it can be observed everywhere where the collector capacitance of a transistor can detune the resonant frequency of the connected circuit. Similar difficulties are present with varactor multipliers. With the high voltage drive levels to the transistor that are common in transmitters, parametric oscillations can result. In this case, the resonant circuit jumps between two different frequencies under the effect of the RF voltage fed to it. The change of frequency can be effected by varying the decoupling of the operating voltage or the emitter, however, cannot be completely be avoided. In small-signal stages which still allow parallel resonant circuits, a decoupling resistor of 10 Ω to 100 Ω can be connected between collector and resonant circuit (9). This represents an effective countermeasure. In power amplifier stages, a circuit arrangement as given in Figure 3 has been found to be suitable.

Parasitic or spurious oscillations are more dangerous. In simple cases, similar effects such as the generation of sidelines occur. However, such oscillations can be so great, especially in power amplifier stages, that the transistors can be destroyed within some milliseconds without the operator having a chance of finding the cause.

With common emitter circuits in the VHF/UHF range, these are usually the so called Huth-Kühn oscillations (7). This indicates a disadvantage of the circuits given in Figure 5 (with the exception of Figure 5c), namely that they possess low-pass characteristics which means that frequencies below the resonant frequency are not attenuated. For this reason, they are not suitable for use in the output of frequency-multiplying stages. A parallel circuit is far more suitable to suppress the fundamental wave and unwanted harmonics. However, collector and base chokes can form additional "parasitic" resonant circuits at lower frequencies together with the circuit and transistor capacitance (C_i and C_{ob} in Figure 6a). Both circuits are coupled via the feedback capacitance C_{ob} as in the Huth-Kühn circuit. The fact that this capacitance periodically represents a diode after commencing oscillation and the fact that the transistor capacitances are voltage-dependent, makes it difficult to describe the effect.

If the parasitic circuits have only approximately the same resonant frequency, the circuit will break into oscillation as soon as current flows through the transistor, and completely independent of the fact whether this occurs in the DC mode or by RF drive. Such oscillations are aided by the fact that the current gain is greater at lower frequencies and that the parasitic circuits are not loaded.

The means of avoiding such effects given in (3) by bringing the collector choke together with the output capacitance of the transistor to resonance at the operating frequency and to keep the inductivity of the base choke as small as possible, to damp it or build it up in the form of a wire-wound resistor are designed to shift the parasitic resonances to the highest possible frequency range where the gain of the transistor is lower.

The tuning-out of the transistor output capacitance which varies in step with the operating voltage is, at least in the opinion of the author, very doubtful. In the shortwave range it is not practical. Even the recipe for the base choke is not possible for a multiband transmitter.

On the other hand, it has been found suitable in the shortwave region to place the parasitic resonances as far as possible from another (7). The same principle can also be used for VHF transmitters. For instance, an 1 μH ferrite choke can be used as collector choke. With a base choke of several μH, the circuit will oscillate strongly, even with 30 μH the circuit is not stable. A base choke of 130 μH (the exact value is not critical), allows completely stable operation without damping measures.

Before commencing operation in conjunction with a newly developed circuit it is recommended for the DC test to be made with respect to parasitic oscillations by which the most suitable value for the base choke can be found. Fig. 6b explains the process. With each stage operating in class C (without quiescent current), the cold end of the base choke is isolated from ground and is bypassed with a capacitor that is sufficient even for low frequencies. At this point, base current is introduced from the plus pole via a variable dropper resistor (not a voltage divider). The operating voltage is reduced to 1/3 to 1/4 of the breakdown voltage U_{CEo} of the transistor used, in this case, to 10 to 14 V. The power supply should, if possible, be provided with a variable current limiter. If this is not possible, a resistor of 50 to 100 Ω with a sufficiently high rating should be placed into the plus line.

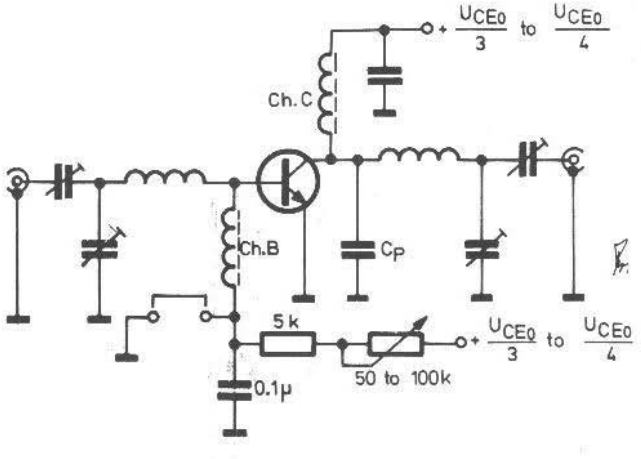

Fig. 6 b: Test circuit for determination of parasitic oscillations without endangering the transistor

Parasitic oscillations will be observed even at a low collector voltage as soon as the collector current exceeds a certain value. An oscilloscope or a valve-voltmeter (VTVM) with a RF probe can be used for indication. If not available, the collector current itself of the stage in question serves as an indicator. The current will be reduced on commencing oscillation whereas the base current determined by the dropper resistor will remain constant. The collector current in a non-oscillating condition can be measured by damping the collector choke with a resistor of 10 Ω to 30 Ω. After selecting a suitable base choke, the collector current of each stage must follow the adjustment of the base current continuously and the damping of the collector chokes must have no influence on the collector current. The operating voltage is increased in steps up to half the breakdown voltage U_{CEo}, in our case to 18 to 20 V, in order to test whether no spurious oscillations occur in this range. How far the collector current can be increased should be estimated because the permissible DC power dissipation of RF power transistors at high collector voltages is lower than in RF operation.

Finally, the trimmers for matching the input and output of the various stages are detuned in order to see whether a tendency to spurious oscillation occurs on altering the resonant frequencies. It is possible during this test that one of the stages, especially the power amplifier stage will break into oscillation in the VHF range. This self-excited oscillation is normally extremely sensitive to any damping. e.g. touching the coil with one's finger, which means that it is not too important. Oscillations at the frequency of operation are not to be expected during practical operation as long as the transit frequency of the transistors is not twenty or more times greater than the operating frequency. Interactions due to an unfavourable construction must, of course, be avoided.

If all stages operate satisfactorily during this test, a low RF drive can be provided and the fundamental operation of the matching links can be tested in class A. Any jump of the current values during alignment indicates instabilities which must be examined further. The (low) output power must vary continuously with the drive. If no irregularities are observed, the stage can be changed to class C (shorting the bypass arrangement of the base choke) and by increasing the operating voltage in steps to the full power level. Once again, no jumps should occur during the alignment and the output power should increase or decrease continuously with the drive and with the operating voltage. If this process has been strictly followed, the circuit can be assembled into its permanent stage, nasty surprises are not to be expected.

3.3. COMMON EMITTER OR COMMON BASE CIRCUIT

Whereas in professional transistorized equipment the common emitter circuit is mainly used, the common base circuit is very often used in amateur circuits. Whether this is the result of past times when the maximum power was squeezed out of transistors such as type 2 N 2218 or whether other reasons exist for this is not known because the authors do not usually give reasons for the selection of a specific circuit.

In comparison, the common base circuit has the advantage that it allows a higher operating voltage and provides a relatively constant gain over a wide frequency range. This means that it is not so liable to destroy itself as the emitter circuit. The problem of parasitic oscillations is also far easier to solve with the common base circuit.

However, the common base circuit possesses several peculiarities which, unfortunately, cannot be avoided by circuit modifications. Every common base circuit with transistors in standard cases represent a "neutralized" oscillator. The collector is directly connected to the case whereas base and emitter are connected via minute wires to the external connections. In a common emitter circuit, emitter connection inductivity merely reduces the gain. The inductivity of the base connection is compensated for; in the common base circuit, on the other hand, the inductivity of the base connection has the effect of a negative input impedance and thus represent a feedback effect. It is this effect that makes the gain in a critical frequency range in the vicinity of the limit frequency seemingly higher than at lower frequencies.

At VHF frequencies, this feedback effect shows itself in several ways. The gain is better than with a common emitter circuit, which may seem very advantageous. However, if a transmitter is, for instance, aligned to 145 MHz, the fall-off of the power at both band limits is not symmetrical and will differ greatly. If the drive is reduced, the output power will fall continuously at first and will then jump to a far lower value after which it will be reduced continuously to zero. On increasing the drive again, it is possible, under certain circumstances, that the previous output power is only achieved after realignment. A reliable AM transmitter cannot be built up with such characteristics.

The common emitter circuit, on the other hand, exhibits a normal symmetric bandwidth and a continuous (naturally, not linear due to class C operation) dependance of the output power on the drive power in the range from zero up to the full value. Since it has been shown that parasitic oscillations can be eliminated with the common emitter circuit, the common base circuit cannot be recommended under normal conditions (4) and (10). However, the common base technology is gaining ground in microwave technology using new types of transistor cases and extremely low inductivities of the base connections (11).

- will be continued -

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AM-DEMODULATORS USING SILICON SEMICONDUCTORS

by D. E. Schmitzer, DJ 4 BG

INTRODUCTION

Although germanium diodes are completely suitable for amateur applications when used in conventional demodulator circuits, it is interesting to try new circuits using silicon semiconductors. Since germanium diodes cannot be just replaced by silicon diodes, a certain amount of additional circuitry is required. However, when using integrated circuits and multiple transistor package, certain characteristics can be achieved that would not be possible with germanium diodes. This article is to describe several such circuits having silicon semiconductor complements.

1. DIODE DEMODULATOR WITH SILICON DIODES

Without any additional measures, a silicon diode is not suitable for the demodulation of amplitude-modulated (AM) signals since its high threshold voltage of approximately 0.5 V would lead to an unpleasant amount of distortion even at high AF (or IF) voltages. The first thought is to forward bias the diode using a voltage divider so that the operating point is brought into class B. However, this is not successful because the slightest temperature variation will cause a shift of the characteristic curve. On reducing the temperature, the diode will be shifted to class C, or to class AB if the temperature is raised. In class AB, low IF voltages will only be demodulated with a high degree of distortion.

However, the threshold voltage of a silicon diode can be made temperature independent by a current of approximately 10 μA. This bias current ensures that the diode is operating in the bend of the characteristic curve, where RF voltages will be demodulated with a low degree of distortion even when below approximately 100 mV. If a positive operating voltage is available, the circuit shown in Fig. 1a can be used. This circuit is not very different from conventional diode rectifiers and supplies a negative DC voltage, in addition to the audio voltage U_{AF}, which can be used as a control voltage. The control voltage is taken previous to the output capacitor and fed to a control voltage amplifier.

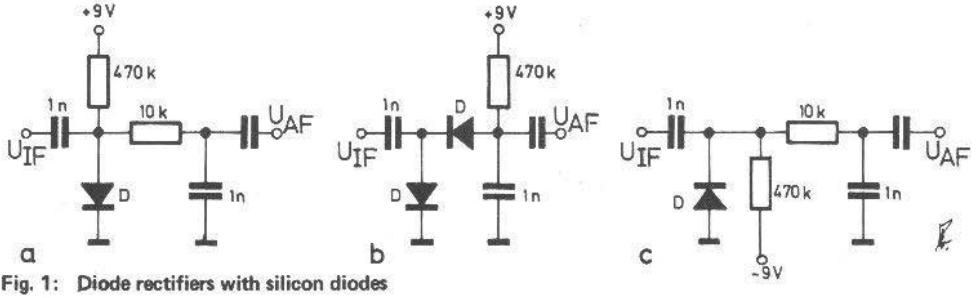

Fig. 1: Diode rectifiers with silicon diodes

A voltage doubler circuit can be built up in the same manner. Such a circuit is shown in Fig. 1b. The demodulation characteristic of this circuit is very linear even with very low IF voltages, whereas a practically perfect linear relationship between input voltage and DC voltage (and thus also audio voltage) exists at higher voltages.

If a positive control voltage is required to feed a control voltage amplifier, it is necessary for a voltage source of negative polarity to be provided for the bias current. Fig. 1c shows the principle of such a circuit.

All low-capacitive, fast silicon switching diodes are suitable for the described circuits. Especially suitable are the inexpensive planar-diodes, of which the 1 N 914 is possibly the most well-known.

2. TRANSISTOR DEMODULATOR WITH TEMPERATURE COMPENSATION

With the following circuits, the demodulation is carried out on the base-emitter path of a silicon transistor. This diode path is biased using a voltage divider so that a collector current of approximately 10 to 50 μA flows (class B). In order to compensate for the shift of the characteristic, as described in section 1, due to temperature variations, the voltage divider is equipped with a silicon diode D. Since the diode has virtually the same temperature response as the base emitter diode path of the transistor, and since the diode is also affected by the same temperature variations, the configuration remains in class B. The quiescent current is adjusted across the dropper resistor R_d (Fig. 2).

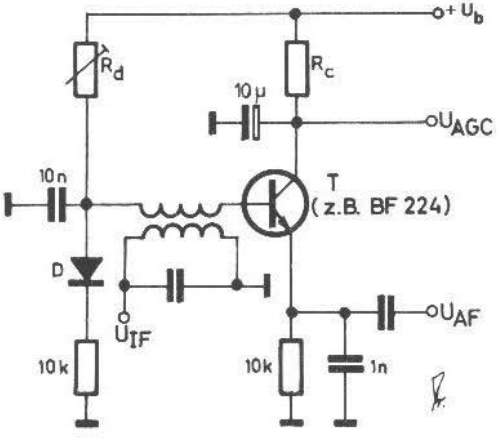

Fig. 2: Transistor demodulator with temperature compensation

At the emitter of the transistor, the AF voltage as well as a positive going DC voltage are available. This DC voltage, which is suitable for automatic gain control, is available from a relatively low-impedance source. Since the collector current of the demodulator transistor increases with the value of the IF voltage, an increasing voltage drop will be present on the collector resistor R_C, which could also be used as a control voltage.

If a transistor having the same characteristics as the demodulator transistor is used in the voltage divider instead of the diode, it is possible to calculate the value of the dropper resistor. The current I flowing through the demodulator transistor is namely of the same value as that flowing through the compensation transistor due to the dropper resistor R_d. This means:

$$I = \frac{U_b - 0.6}{R_d}$$

Measurements and adjustments are thus not required, which means that a fixed resistor can be used instead of the trimmer potentiometer.

Such circuits can be most favourably built up when the transistors are on the same wafer. Such a demodulator circuit using the integrated multiple transistor CA 3018 (RCA) is given in Fig. 3. The type CA 3046 can be used in a similar manner. The two transistors, whose connections are individually fed out from the casing, serve as compensation diode and as demodulator transistor. The Darlington transistor pair is used to amplify the control voltage. The great advantage of this circuit is the very high temperature stability. The dependence of the quiescent current I_O (determined by the dropper resistor of 1 MΩ) as a function of temperature is shown in Fig. 4a. A further advantage is the very high linearity of the demodulator characteristic. This is shown in Fig. 4b, which shows the dependence of the voltage U_E on the IF voltage U_{IF} at the emitter of the demodulator transistor. In addition to this, the characteristic of the (unloaded) control voltage U_{AGC} is also given.

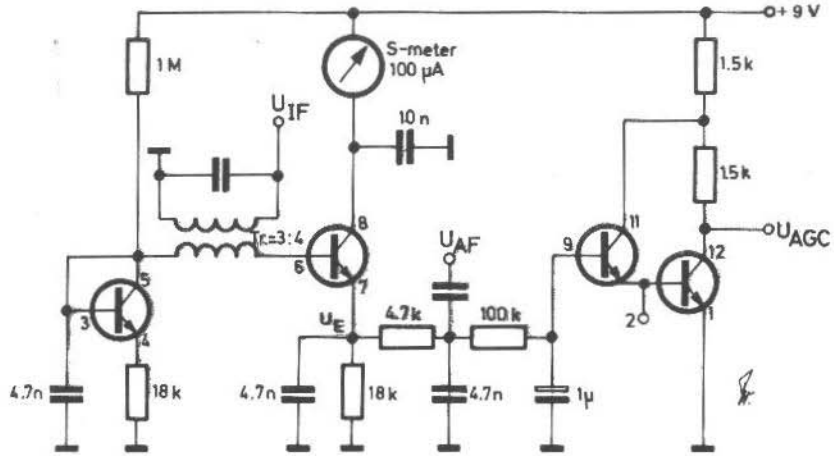

Fig. 3: Temperature-compensated transistor demodulator with AGC amplifier using the integrated multiple transistor CA 3018

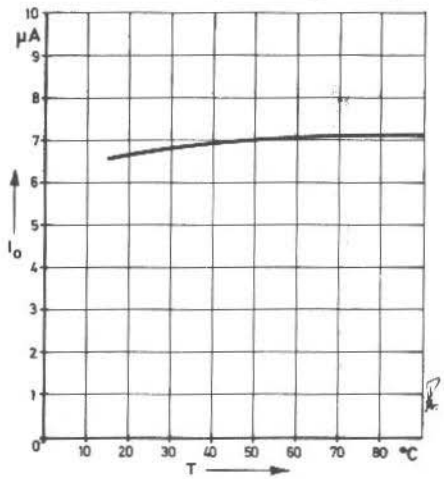

Fig. 4 a: Temperature response of the quiescent current of T 2 in Fig. 3

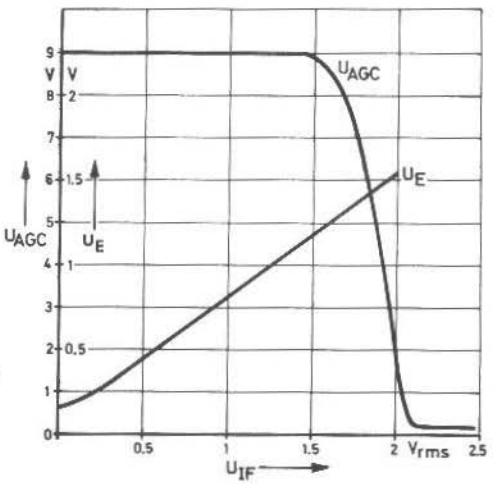

Fig. 4 b: Emitter voltage U_E and voltage U_{AGC} at the control voltage output.

Finally, Fig. 5 shows another variant of the circuit given in Fig. 3 for capacitive injection of the IF voltage. Equal resistors are used in the base circuit of both the compensation and demodulator transistors, which means that a high degree of balance and a good temperature stability are maintained. The rest of the circuit is as given in Fig. 3.

Various integrated circuits require a very high input current for their AGC stage (e.g. CA 3028 A, CA 3053 to point 7). The source impedance of the control voltage circuit given in Fig. 3 is too high for this purpose. It is therefore necessary for a further transistor to be used as emitter follower, whereby the two 1.5 kΩ resistors in the collector circuit of the original control voltage amplifier may both be increased to 33 kΩ. This measure reduces the current of the control stage from approximately 3 mA to about 130 μA (under full control conditions and with U_b = 9 V). This circuit detail, which is shown in Figure 6, is therefore suitable for small battery-driven equipment. All silicon NPN audio transistors such as BC 108, BC 183 or 2 N 2926, are suitable for the emitter follower.

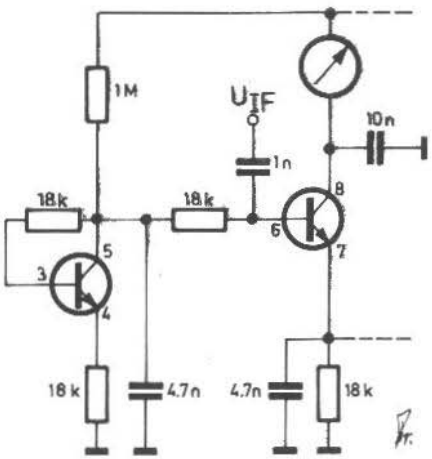

Fig. 5: Modifications to the circuits given in Fig. 3 for capacitive injection of the IF voltage

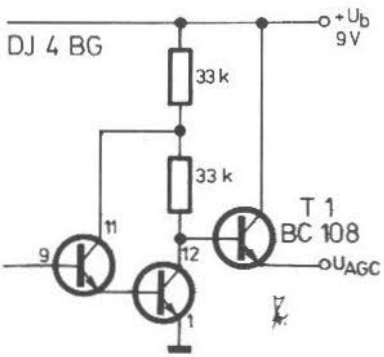

Fig. 6: Extension of the circuit as given in Fig. 3 by an emitter follower for the control voltage

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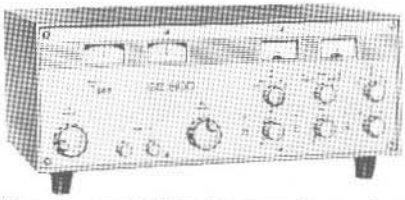

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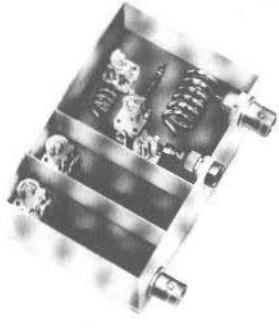

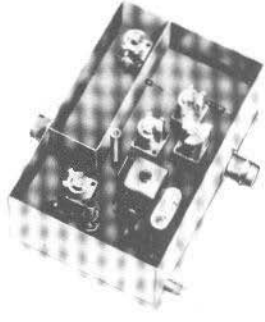

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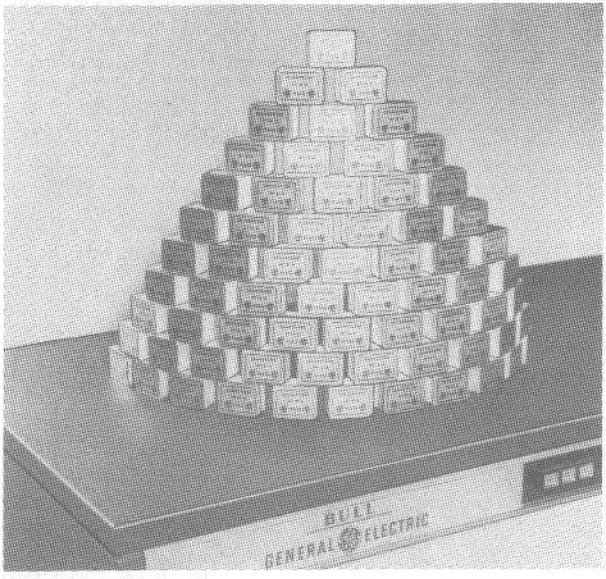

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