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Contents

The design of a high-speed logic system and a Formula 1 racing car have many parallels. In both cases you have a highly-tuned system that's expected to respond instantly to the commands of its controller: microprocessor in one case, driver in the other. And in both cases the designer has to make trade-offs to get ultimate performance: trade-offs of speed versus economy, reliability versus low-cost. With HCMOS logic ICs, however, the analogy ends there. Using proven CMOS processes and tighter (3 μm) layout rules, HCMOS combines the high speed of bipolar logic with the low power consumption of CMOS. Already HCMOS is five times faster than its predecessor, and at the current rate of development, it's expected to double its speed every year. Imagine, if the pace of automobile development had matched that of logic systems over the past few years, we'd now have Formula 1 cars going supersonic!

HCMOS low-power logic ICs that set the standard

HENRI MOLKO

As all logic-system designers know, there's always been a trade-off between the speed at which the ICs in a logic system can operate and the power they consume (Figs.1 and 2). Bipolar ICs can be fast but they are too power hungry and their noise immunity is mediocre compared with that of CMOS ICs. Conventional CMOS is power-sparing but it's slow.

A breakthrough was needed to resolve the dilemma, so our IC development engineers set to work. We didn't want a new untried process and all the teething troubles that go with, it so we re-appraised our well-proven silicon-gate CMOS process, together with the technique we pioneered for the local oxidation of silicon (and have been using for more than ten years to make our HE4000B series of CMOS logic ICs). We tightened the layout rules, built a 3 μm gate structure and thinned the oxide in the gate region. The result – the birth of a new range of high-performance CMOS logic ICs: the 74HC/HCT/HCU high-speed CMOS (HCMOS) family which has all the advantages of LSTTL and CMOS and none of their disadvantages.

The comprehensive HCMOS family encompasses pin-compatible versions of all the popular TTL and CMOS 4000 types. It also includes functions such as phase-locked loop and analog (bilateral) switches, the latter being impossible to implement in bipolar technology. There are 143 IC types in the HCMOS family, all of which are available in 74HC and 74HCT versions in DIL or SO packages.

Circuits with the type number prefix 74HC are fully buffered with CMOS input switching levels (switching threshold 50% of V_{CC}) for high noise immunity, and a supply voltage range of 2 V to 6 V; their main role is as faster CMOS replacements for new logic system designs. There are also unbuffered inverters available (74HCU prefix) for constructing RC or crystal oscillators and other feedback circuits operating in the linear mode.

Circuits with the type number prefix 74HCT are also fully buffered. They have the same features and functions as 74HC types, but have TTL-compatible input switching levels (switching threshold 28% of V_{CC}) and operate from a supply voltage range of 5 V ± 10% (twice the margin of commercial LSTTL). They are pin-compatible with most popular LSTTL ICs which they are intended to replace to reduce the power consumption of existing systems without reducing their speed of operation. We don't view this as an interim measure and believe that there will be a demand for 74HCT ICs in mixed technology systems and to support asymmetrical LSI peripherals far into the future. We therefore developed and patented an HCMOS input structure that allows the entire type range of HCMOS ICs to also be created as 74HCT versions by making a single metal mask change in wafer processing.

Since the low power dissipation of our HCMOS ICs makes them ideal for circuitry on densely packed boards in small enclosures, we didn't overlook the need to make them compatible with the new surface-mounting technology which is being increasingly used to extend automated assembly and achieve significant reduction of the size and weight of electronic equipment. Production quantities of all our HCMOS ICs are available in DIL packages and in SO (small-outline) packages. The dimensions of the latter were originally developed by us and now form the basis of JEDEC standard publication 95 (also published in IEC standard document 191-2, family A76).

Although there are two SO body widths (150 mil = 3,8 mm and 300 mil = 7,6 mm) available for 14-pin and 16-pin ICs, to accommodate different sizes of dies, we have put all our 14-pin HCMOS ICs in the narrower 150 mil (3,8 mm) body SO package. This greatly simplifies pcb layout because it means that the SO body width for HCMOS ICs with 14 or 16 pins is 150 mil (3,8 mm), and for HCMOS ICs with 20, 24 or 28 pins it is 300 mil (7,6 mm).

HCMOS ICs in SO packages are available in tubes or on tape on two sizes of reels: 7 in. or 13 in. diameter: For SO-14 and SO-16 ICs, the tape width is 16 mm and there are about 1000 ICs on a 7 in. reel and about 4000 ICs on a 13 in. reel. For SO-20, 24 and 28 ICs, the tape width is 24 mm and there are about 500 ICs on a 7 in. reel and about 2000 ICs on a 13 in. reel.

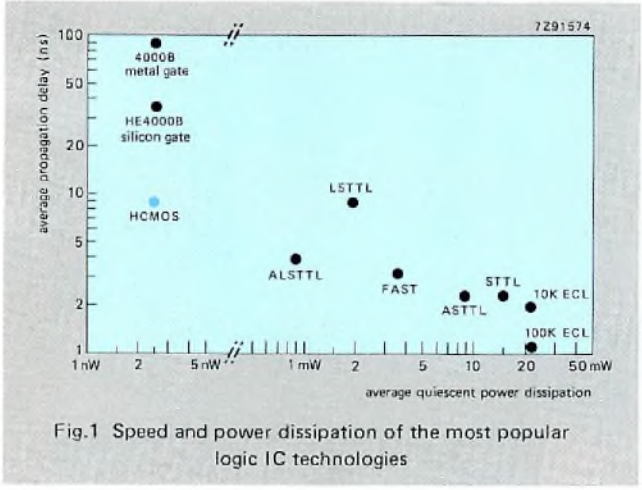


Fig.1 Speed and power dissipation of the most popular logic IC technologies

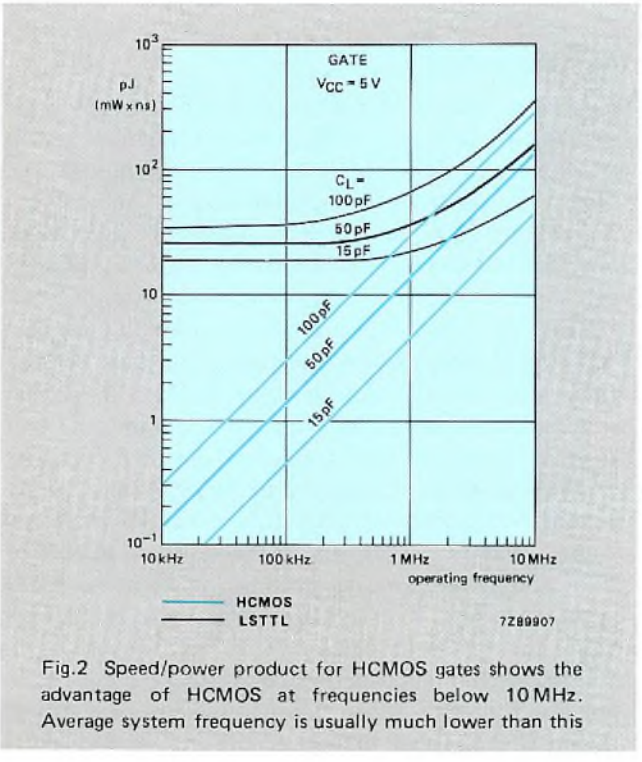


Fig.2 Speed/power product for HCMOS gates shows the advantage of HCMOS at frequencies below 10 MHz. Average system frequency is usually much lower than this

The reliability of our HCMOS ICs is less than 5 FITS at 60% confidence. They are completely latch-up free, and have complete protection against electrostatic discharge (ESD) at their inputs. And remember that, as the largest European source, we can promise continuity of supply when world demand is heavy. Here are 21 reasons why our HCMOS is head and shoulders above the rest.

- A complete type range from simple gates to counters and analog functions.
- Functions and pinning identical to popular LSTTL and CMOS 4000 ICs.
- All types available in 74HC versions (CMOS input levels) and 74HCT versions (TTL input levels). The latter are made from the same mask set as the 74HC versions, so the 74HCT versions are not just an interim measure.
- All types available in SO (small outline) package on tape and reel as well as in DIL, so you can use surface-mounting techniques to increase pcb packing density. All 14 and 16-pin HCMOS ICs in SO packages are available in narrow body versions.
- Wide operating temperature range of −40 °C to +125 °C. Much less limiting than the 0 to 70 °C specified for commercial LSTTL. Our 74HC/HCT/HCU family is tested according to the −40 °C to +125 °C specification so there's no need to invest in 54 prefix types to benefit from a wider operating temperature range
- Completely latch-up free and fully ESD protected at all inputs
- Much more reliable than LSTTL. Life testing reveals a failure rate of only $4{,}3 \times 10^{-9}$/h at 60% confidence level
- Low power consumption. Typical quiescent current per package is only a few nanoamps for gates, flip-flops and MSI. Typical counter operating current with a 5 V supply is 250 nA at 1 MHz and is linear with frequency. This compares with LSTTL operating current of 19 mA which also increases with increasing frequency. So when you use 74HCT types to replace their LSTTL counterparts there are immediate benefits to be gained
- A standard HCMOS output with a 4,5 V supply can drive 10 LSTTL inputs (4 mA) and a bus driver can drive 15 LSTTL inputs (6 mA). That's ten times the fan out of earlier CMOS. HCMOS input current is only 1 μA in the HIGH or LOW state. This is essentially zero compared with the input current of LSTTL which is 400 μA in the LOW state and 20 μA in the HIGH state. The fan-out to other HCMOS ICs is therefore only limited by load-capacitance considerations and not by output-drive capability

- More than three times the noise immunity of LSTTL. Input switching levels for 74HC types are 30% and 70% of V_{CC}. Output swing for all HCMOS ICs is from 0,1 V to V_{CC} – 0,1 V with a load of 20 μA (twenty HCMOS inputs), and from 0,33 V to V_{CC} – 0,66 V with a load of 4 mA (10 LSTTL inputs) or 6 mA (15 LSTTL inputs) for bus drivers
- The input switching threshold level is subject to a variation of only ±60 mV over the entire temperature range. Much less than the ±200 mV specified for LSTTL
- Wider supply voltage range. 74HC versions are specified with a supply from 2 V to 6 V. Battery back-up is no problem and automotive applications are possible. LSTTL-compatible 74HCT versions are specified with a supply of 5 V ± 10%. That's twice the supply-voltage tolerance of commercial LSTTL to allow simpler regulation and cheaper power supplies
- Typical operating frequency up to 60 MHz at 25 °C and f_{max} is simply specified with a 50% duty factor. With a 4,5 V supply, typical propagation delay for a gate is 8 to 11,5 ns for either HIGH-to-LOW or LOW-to-HIGH transitions into capacitive loads of between 15 and 100 pF. This is only one-fifth of the gate delay of earlier silicon-gate CMOS
- Standardized output buffers allow symmetrical output current sourcing and sinking for equal output rise and fall times (7,5 ns for standard outputs and 6 ns for bus driver outputs). This results in simplified design combined with optimum speed and a.c. performance
- Output leakage current of bus drivers with 3-state outputs in the high-impedance state is only a quarter that of similar LSTTL ICs, so the value of bus pull-up/pull-down resistors can be increased to reduce the power they consume
- Unbuffered inverters available for linear applications such as oscillators
- Low current-coupling between adjacent inputs aids application in the noisy environments encountered in vehicles and heavy industry
- All types CECC approved
- All types specified in accordance with JEDEC standards and meet or exceed the JEDEC limits
- Extensive customer support available
- RCA is an alternate source for our HCMOS ICs

COMPARING HCMOS WITH OTHER LOGIC FAMILIES

Supply voltage

HCMOS circuits with the type number prefix 74HC and 74HCU are faster alternatives to earlier CMOS types for new designs. In addition, the HCMOS technology has allowed the lower supply voltage limit to be extended to 2 V, giving an overall range of 2 V to 6 V (Fig.3). This gives an important advantage over earlier CMOS circuits because it will permit the continued use of HCMOS circuits with future generations of memories and microcomputers which may operate from a supply of less than 3 V. The extended supply voltage range also meets the new industry JEDEC standard No. 8 which specifies 3,3 V ± 0,3 V for regulated power supply systems and 2,8 V ± 0,8 V for battery-powered systems. It also facilitates the use of a lithium battery as a back-up supply.

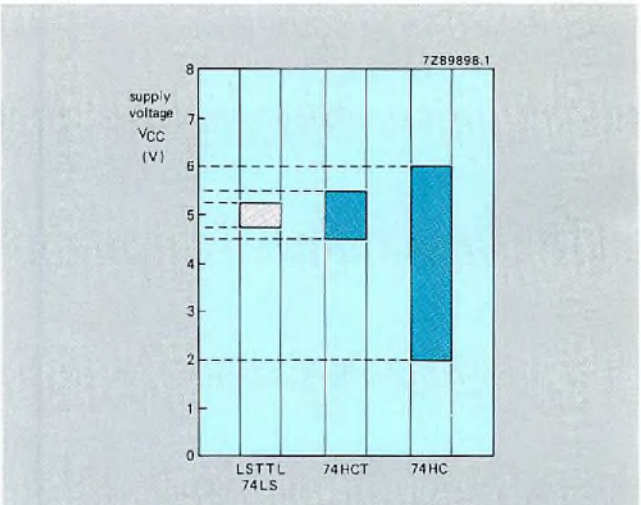


Fig.3 Supply voltage ranges show that 74HCT circuits have twice the margin of commercial LSTTL circuits. And 74HC circuits operate with a supply voltage as low as 2 V

Power dissipation

One of the most important requirements for any logic system is low power dissipation because it minimises system cost, allows higher packing density and results in improved reliability because of lower operating temperature.

Considering quiescent power dissipation first, Fig.4 shows that the quiescent power dissipation of all HCMOS functions is about five orders of magnitude less than that of LSTTL functions. This is because, unlike TTL circuits, CMOS circuits dissipate only negligible power due to leakage currents when they are not switching. Figure 5 shows that the quiescent current per HCMOS package is only 1,3% of that of an equivalent LSTTL package. Figure 6 compares the dynamic power dissipation of HCMOS and LSTTL functions and indicates a wide differential at lower frequencies. This is because the high quiescent current of LSTTL circuits predominates over their transient current at frequencies below about 1 MHz. Conversely, in HCMOS circuits, the quiescent current is so low that the small transient current predominates so that their dynamic power dissipation is directly proportional to switching frequency.

Figure 6 shows that the power cross-over frequency is

Comparison of logic ICs containing four NAND gates

	metal gate CD4000	Si-gate HE4000B	LSTTL	HCMOS
supply voltage range (V_{CC})	3-18 V	3-15 V	5 V ± 5% (com.) 5 V ± 10% (mil.)	2-6 V (HC/HCU) 5 V ± 10% (HCT)
typical quiescent dissipation per gate	2,5 nW	2,5 nW	2 mW	2,5 nW
max. quiescent current per package at 85 °C	7,5 μA	7,5 μA	3 mA*	20 μA
typical power dissipation per gate (V_{CC} = 5 V, C_L = 50 pF)				
at 10 kHz	25 μW	16 μW	2 mW	14 μW
at 100 kHz	250 μW	160 μW	2 mW	140 μW
at 1 MHz	2,5 mW	1,6 mW	2,8 mW	1,4 mW
at 10 MHz	–	–	12,5 mW	14 mW
typical propagation delay				
C_L = 15 pF	90 ns	36 ns	10 ns	9 ns
C_L = 100 pF	175 ns	83 ns	17 ns	11,5 ns
fan-out (TTL loads)	1	1	10	10
max. operating frequency with C_L = 15 pF	3 MHz	5 MHz	25 MHz	25 MHz
worst-case noise margin				
V_{NML} (% V_{CC})	29	29	8	28** 14†
V_{NMH} (% V_{CC})	29	29	14	28** 58†
operating temperature range				
standard (°C)	–40 to +85	–40 to +85	–0 to +70	–40 to +125
extended (°C)	–55 to +125	–55 to +125	–55 to +125	

* 50 % of gates in the HIGH state; ** HC/HCU; † HCT.

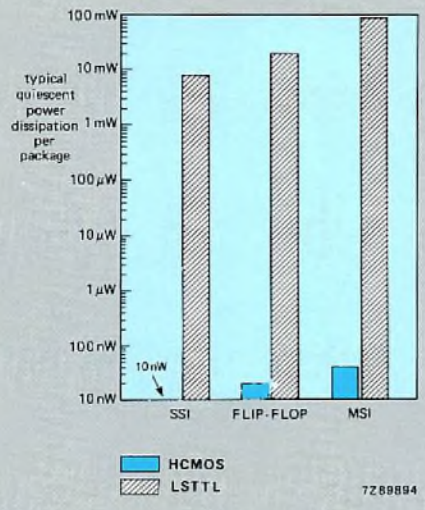


Fig.4 Unlike LSTTL circuits, HCMOS circuits consume negligible power when they are not switching

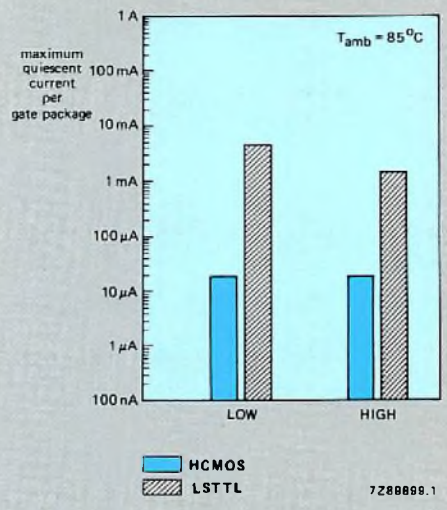


Fig.5 Even a total HCMOS package of four gates under worst-case static conditions consumes more than two orders of magnitude less power than an equivalent LSTTL gate package

about 5 MHz for a gate, and above 10 MHz for a flip-flop. However, in a practical logic system, only a few of the logic elements will operate at the maximum clock frequency, so the average operating frequency is much lower, giving HCMOS ICs an even greater advantage over LSTTL. Figure 7 shows that, in a more complex system comprising a divider chain of ten flip-flops, the power cross-over frequency increases beyond the upper limit of the operating frequency range for HCMOS. It's obvious that HCMOS circuits are far less power hungry than their LSTTL equivalents. They dissipate about the same power as earlier silicon-gate CMOS circuits because their output buffers are made large enough to source and sink LSTTL currents, but they're five times as fast.

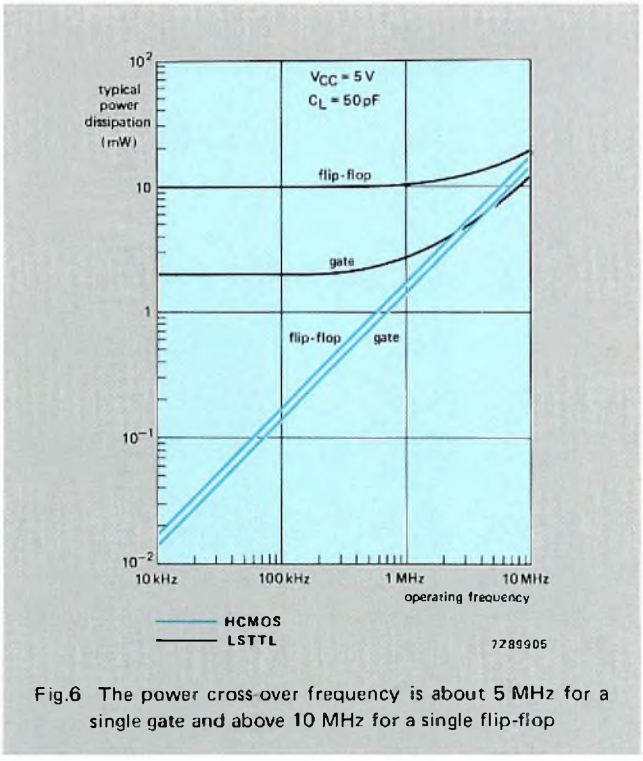


Fig.6 The power cross-over frequency is about 5 MHz for a single gate and above 10 MHz for a single flip-flop

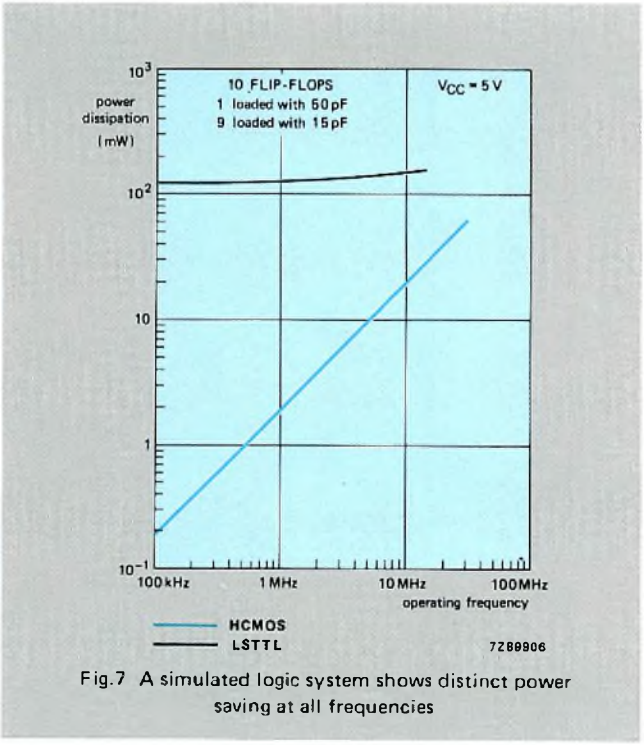


Fig.7 A simulated logic system shows distinct power saving at all frequencies

Propagation delay

As indicated in the Table on page 133 and in Fig.8, the propagation delay for a single HCMOS gate with a 15 pF load is only 8 ns: only one-tenth of the delay of metal-gate CMOS, a quarter that of earlier silicon-gate CMOS and 80% that of LSTTL. Moreover, propagation delay is specified at the lowest system supply voltage (4,5 V) and remains valid over the entire operating temperature range. The a.c. characteristics of HCMOS are further improved by standardized output buffers which allow equal rise and fall times (7,5 ns for standard outputs and 6 ns for bus driver outputs). The typical switching-frequency limit for a flip-flop is 60 MHz, f_{max} being specified with a 50% duty factor so you don't have to tweak with pulse widths as you do with LSTTL. Due to the high drive-current capability of the low-impedance HCMOS outputs, propagation-delay variation for bus drivers is only 3,5 ns over a load-capacitance range of 15 pF to 100 pF. This variation of propagation delay with load capacitance is much less than that of most other logic ICs. The a.c. characteristics of HCMOS ICs are specified over the entire range of supply voltage and temperature, a considerable advantage over LSTTL which is only specified at 5 V and 25 °C.

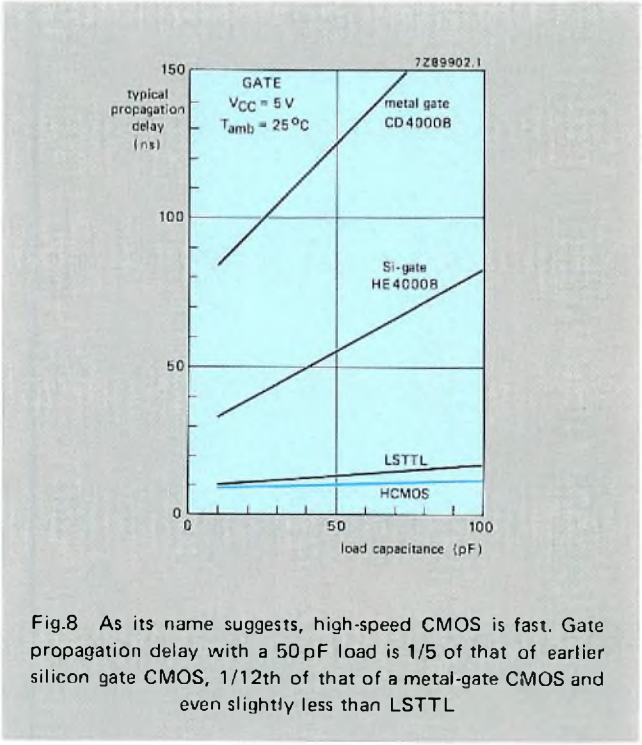


Fig.8 As its name suggests, high-speed CMOS is fast. Gate propagation delay with a 50 pF load is 1/5 of that of earlier silicon gate CMOS, 1/12th of that of a metal-gate CMOS and even slightly less than LSTTL

Noise immunity and input levels

The input switching levels for 74HC/HCU ICs are 30% and 70% of V_{CC}. Output swing is from 0,1 V to V_{CC} – 0,1 V with a load of 20 μA (20 HCMOS inputs). For 74HC/HCU circuits with standard outputs driving 20 HCMOS inputs, the LOW and HIGH level noise immunity with a 4,5 V supply is therefore 28% of V_{CC}. This is a considerable improvement over LSTTL for which the margin in the LOW state is only 8% of V_{CC} and the HIGH-level margin is 14% of V_{CC}.

As shown in Fig.9, the noise margins are even greater for 74HC/HCU ICs with a higher supply voltage 74HCT ICs match the noise immunity of LSTTL at higher operating temperatures (up to 125 °C) and exceed it at 70 °C. HCMOS circuits are therefore ideally suited for use in electrically noisy environments such as those encountered in industry, telephony and automotive applications.

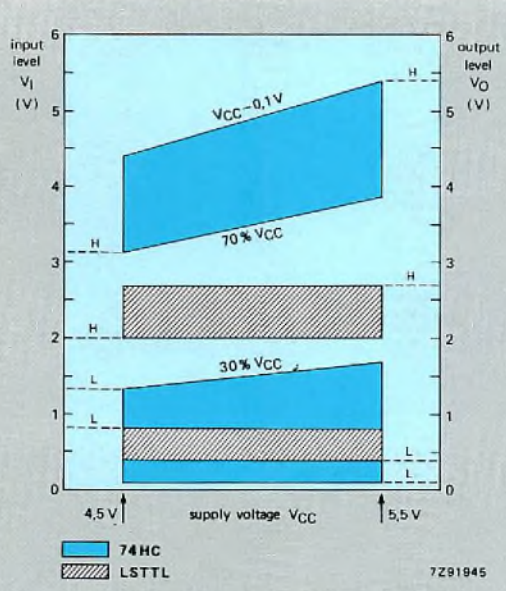


Fig.9 worst-case noise margins for 74HC and LSTTL over the operating supply range 4,5 V to 5,5 V. Valid for wholly 74HC or wholly LSTTL systems

Fan-out

Although the HCMOS family has the low input current which is a characteristic of CMOS circuits, it is capable of providing the same output current levels as LSTTL without sacrifice of noise immunity or switching speed. However, unlike LSTTL circuits, all HCMOS circuits have standardised output buffers which allow symmetrical output current sinking and sourcing to obtain equal rise and fall times. This simplifies design and results in optimum speed and a.c. performance.

As shown in Fig.10, standard HCMOS outputs can source and sink up to 4 mA with a 4,5 V supply. Bus driver outputs can source and sink 50% more current (6 mA) in keeping with their intended application. These drive currents remain valid over the entire operating temperature range. The HCMOS drive capability is thus ten times that of earlier silicon-gate CMOS circuits and, since the required input current for HCMOS circuits is only 1 μA in the HIGH or LOW state (Fig.11), the fan-out when driving other CMOS or HCMOS circuits is only limited by load capacitance considerations and not by the available drive power.

Since the entire type range of HCMOS ICs is also available in 74HCT versions, replacement of LSTTL in existing systems is simply a matter of unplugging the LSTTL ICs and dropping in the 74HCT equivalents. Immediate benefits are considerably reduced power dissipation and wider noise margins. 74HCT versions can also be substituted for, or mixed with ALSTTL, ASTTL or FAST-TTL family ICs in the same system.

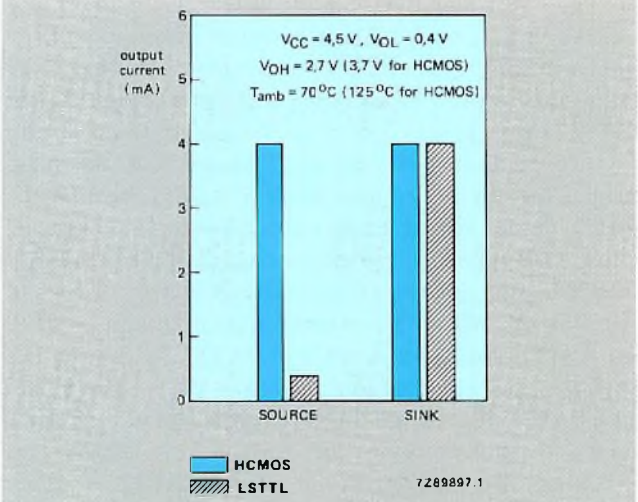


Fig.10 Standard HCMOS outputs can source or sink 4 mA (10 LSTTL loads). Bus driver outputs can source or sink 6 mA (15 LSTTL loads)

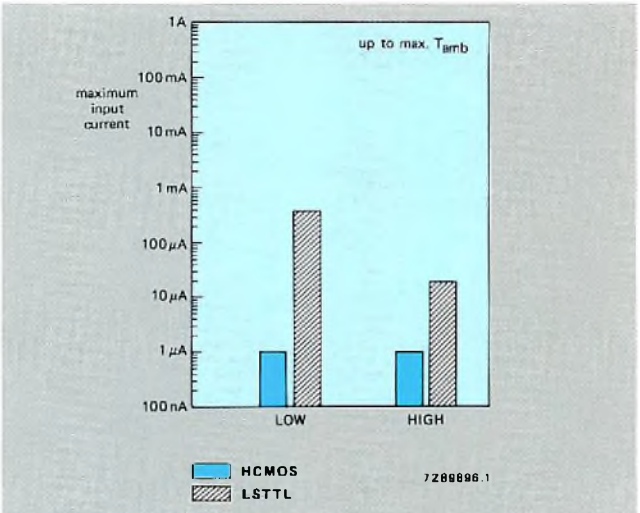


Fig.11 Input current for HCMOS is symmetrical and much lower than that of LSTTL. Theoretically, one HCMOS output can drive nearly a thousand CMOS inputs, but the effect of load capacitance will probably predominate

74HCT – REPLACEMENTS FOR LSTTL

All the advantages previously described for HCMOS ICs naturally also apply to the 74HCT versions. The only differences are that the nominal supply voltage and the input structure of the 74HCT types have been modified to match TTL characteristics. The modified input structure not only adapts to TTL input switching levels, but also reduces power consumption when a minimum TTL HIGH output level of 2,4 V is applied to a 74HCT input. Although the nominal supply voltage for 74HCT ICs is 5 V, just like LSTTL, the supply-voltage tolerance is ±10%, twice the margin of commercial LSTTL, to allow the use of simpler and less expensive power supplies. Unlike 74HC/HCU ICs which have input switching threshold of 50% of V_{CC}, the input switching threshold of 74HCT types is 28% of V_{CC} and input switching levels are the same as LSTTL (V_{ILmax} = 0,8 V, V_{IHmin} = 2 V). The temperature sensitivity of the input switching threshold, however, is only ±60 mV over the entire temperature range compared with ±200 mV for LSTTL, so the noise margins also remain more stable over the temperature range. Figure 12 shows that the noise margins are also wider than those of LSTTL because the 74HCT output voltage swing is much greater. For example, with a 4,5 V supply and an output current of 20 μA (twenty 74HCT inputs), a 74HCT output swings between 0,1 V and V_{CC} – 0,1 V. With the maximum output current of 4 mA (10 LSTTL loads) or 6 mA (15 LSTTL loads) for bus drivers, it swings between 0,33 V and V_{CC} – 0,66 V. So, for a 74HCT IC with a 4,5 V supply driving twenty 74HCT inputs, the noise margins are 53% of V_{CC} (HIGH) and 15,5% of V_{CC} (LOW). For a similar LSTTL IC, they would be only 15% of V_{CC} (HIGH) and 8% of V_{CC} (LOW). Even when a 74HCT IC is driving ten LSTTL inputs, the noise margins are 40% of V_{CC} (HIGH) and 10,4% of V_{CC} (LOW).

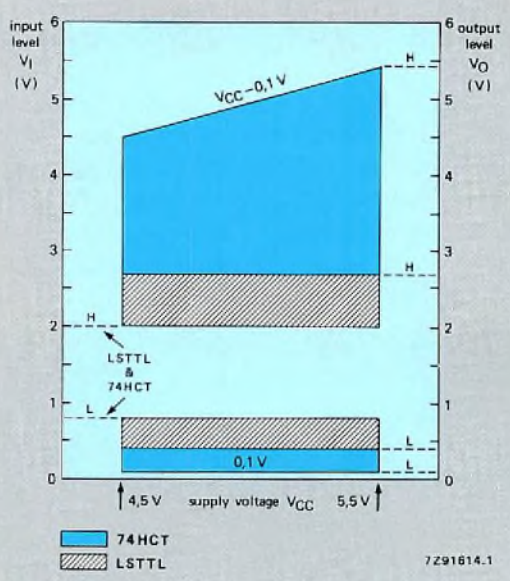


Fig.12 Worst-case noise margins for 74HCT and LSTTL over the operating supply range 4,5 V to 5,5 V. Valid for LSTTL or 74HCT driving 74HCT. For 74HCT driving LSTTL, $V_{OHmin} = V_{CC} - 0{,}66$ V and V_{OLmax} = 0,33 V

Interface requirements

from \ to	HC 5 V supply	HCT 5 V supply	HE4000B 5 V supply	HE4000B 6-15 V supply	TTL* 5 V supply	ECL 10K
HC 5 V supply	direct	direct	direct	4104	direct	10124
HCT 5 V supply	direct	direct	direct	4104	direct	10124
HE4000B 5 V supply	direct	direct	direct	4104	direct	10124
HE4000B 6-15 V supply	4049 or 4050	4049 or 4050	4049 or 4050	direct	4049 or 4050	transistor
TTL* 5 V supply	pull-up resistor	direct	pull-up resistor	4104	direct	10124
ECL 10K	10125	10125	10125	transistor	10124	direct

direct = without interface connections
4104 = LOW-to-HIGH level shifter from the HE4000B family
10124 = TTL to ECL translator from the ECL 10K family
10125 = ECL to TTL translator from the ECL 10K family
4049 or 4050 = HIGH to LOW level shifters from the HE4000B family

* includes LS, S, STD, FAST, ALS and AS.

To summarize, the main advantages of using HCMOS ICs with the prefix 74HCT to replace LSTTL ICs are:

- Direct interface with CMOS 4000 ICs and with TTL ICs including Schottky and low-power Schottky families
- Lower static and dynamic power consumption
- Wider operating-temperature range than commercial LSTTL
- Wider supply-voltage range than commercial LSTTL
- High noise immunity
- Improved stability of input switching threshold voltage
- 1/400th of the input current in the LOW state
- Higher output source current
- Balanced output transitions and delay times
- Lower 3-state (off-state) leakage current
- Maximum clocking frequency is specified for a 50% duty factor so it's not necessary to adjust input pulse widths to obtain maximum speed
- Analog (bilateral) switches and multiplexers available.

INTERNAL STRUCTURE DETERMINES THE HIGH PERFORMANCE OF HCMOS

We got it right first time in the 70's when we used the self-aligning 6 μm (and later 4 μm) polycrystalline silicon-gate CMOS process together with our technique for the local oxidation of silicon (LOCOS) to manufacture the HE4000B family (Fig.13 left). These silicon-gate p-well CMOS circuits were nearly three times as fast as the then available metal-gate CMOS circuits and yet consumed only about 65% of their dynamic power.

Now we've got it right again for the '80s by using the same proven CMOS manufacturing facilities and process, but with tighter layout rules, a 3 μm gate structure and thinner oxide in the gate region for our HCMOS family (Fig.13 right). This enhancement of the CMOS process results in a further fivefold speed increase and a tenfold increase of drive capability without increase of power consumption.

Another reason why the silicon-gate CMOS process is the right choice is that it also allows future evolutionary refinements of the HCMOS family leading to even smaller geometry and consequent increase of switching speed, output drive capability and scale of integration.

The outstanding performance of the HCMOS family is indicated in the family specification at the end at this article and, of course, is fully specified in our HCMOS Data Handbook IC06N. Comprehensive application information for the HCMOS family is given in our newly published HCMOS Designer's Guide.

Excellent ESD protection

The HCMOS input network shown in Fig.14(a) incorporates reverse-biased diodes between the positive rail, input pins and ground to clamp the input voltage. These diodes have typical forward voltage drops of 0,9 V and reverse breakdown voltages of 18 V. In addition, the advanced integration process used for our HCMOS family allows the use of polysilicon current-limiting resistors at all inputs. These slow down fast input transients and dissipate some of their energy. They also ensure that the input impedance never falls below 100 Ω under all biasing conditions, even when V_{CC} is short circuited to ground.

Large inherent diodes formed by the drain surfaces of the output transistors provide output protection and allow discharges greater than 3 kV to be sustained without damage.

The HCMOS input protection network prevents damage to the inputs from ESD of typically greater than ±2,5 kV from the 'human body model' (1,5 kΩ, 100 pF, 13 ns pulse rise time) shown in Fig.14(b). This meets MIL-STD-883C, Method 3015.

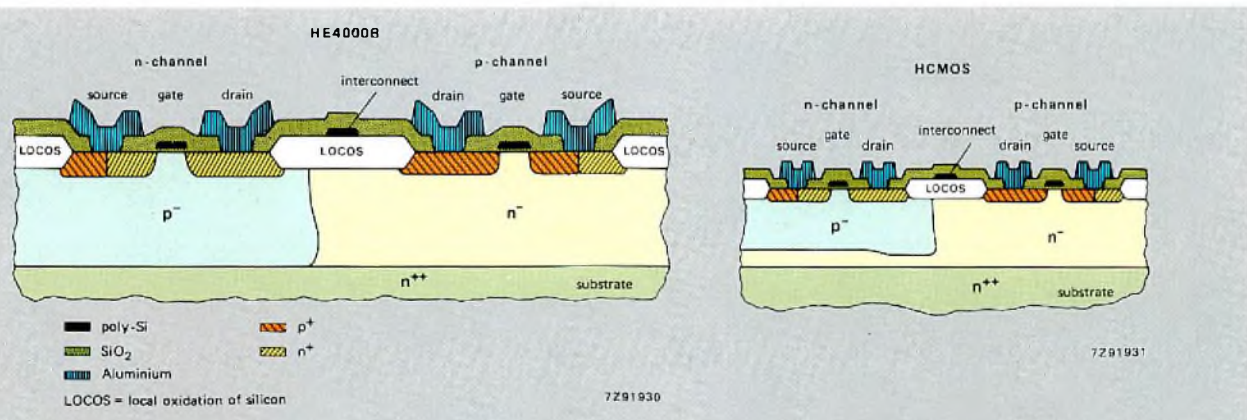


Fig.13 Developed from our 6 μm silicon-gate process as used for the HE4000B family, HCMOS uses the same proven manufacturing facilities and CMOS process, but with tighter layout rules. (left) Basic inverter in HE4000B CMOS, 6 μm gate, and (right) HCMOS inverter, 3 μm gate and thinner oxide in the gate region

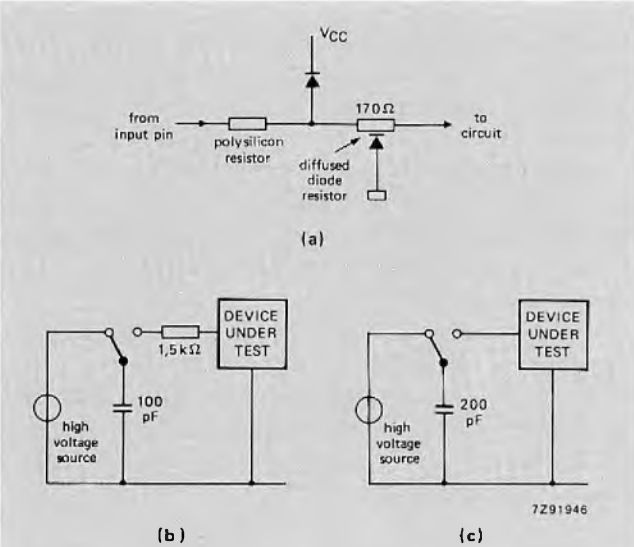


Fig.14 Input protection network for HCMOS ICs. The combination of reverse-biased diodes between the positive rail, input pins and ground, plus polysilicon resistors provides excellent protection against ESD damage. (a) HCMOS input protection network; (b) 'human body model' test arrangement; (c) 'machine model' test arrangement

Most assembly and testing of logic systems is now automatic. This means that the ICs are being handled by robot-like machines which slide them through rails, thus causing the packages to become electrostatically charged. Discharge occurs when an IC package touches a conductive part of the machine. Extensive research and test correlations have resulted in the development of the 'machine model' shown in Fig.14(c) which simulates this. A minimum failure limit of 200 V has now been adopted to determine that devices are not sensitive to ESD from this source. Our HCMOS ICs can typically withstand 320 V in the worst-case test mode.

Latch-up free

Latch-up can be reduced by the use of guard rings, but at the expense of increased chip area. In our HCMOS family, we've completely eliminated latch-up by growing a high resistivity epitaxial layer on the n⁻ substrate.

This prevents lateral current flow through the substrate, dramatically reducing the current gain of the parasitic bipolar transistors that are responsible for latch-up. This, plus proprietary layout rules and process parameters that even further reduce the gain of the parasitic bipolar transistors, means that our HCMOS ICs are completely latch-up free.

We have subjected our HCMOS ICs to latch-up tests with test parameters far exceeding those specified by JEDEC. In no case did latch-up occur. For example, inputs/outputs can withstand currents as high as 100 mA d.c. or 500 mA pulsed. Because of the internal polysilicon resistor at all HCMOS inputs, the voltages necessary to produce these currents are far beyond those that could occur in practice, even in a 6 V system with severe glitches. Inputs can also withstand a discharge from a 200 pF capacitor charged to 370 V (simulated ESD) without latch-up occurring. V_{CC} breakdown for HCMOS ICs doesn't occur until a supply current of 6,8 mA; this requires a supply voltage of more than 21 V. After breakdown, the supply voltage always snaps back to more than 7 V.

HCMOS FAMILY SPECIFICATION

Recommended operating conditions for 74HC/HCT

symbol	parameter	74HC			74HCT			unit	condition
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2,0	5.0	6,0	4.5	5,0	5,5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	–40		+85	–40		+85	°C	see DC and
T_{amb}	operating ambient temperature range	–40		+125	–40		+125	°C	AC CHAR. per device
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs		6,0	1000 500 400		6,0	500	ns	V_{CC} = 2,0 V V_{CC} = 4,5V V_{CC} = 6,0 V

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", 10 V is specified as the maximum operating voltage.

Recommended operating conditions for 74HCU

symbol	parameter	74HCU			unit	conditions
		min.	typ.	max.		
V_{CC}	DC supply voltage	2,0	5,0	6,0	V	
V_I	DC input voltage range	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	–40		+85	°C	see DC and
T_{amb}	operating ambient temperature range	–40		+125	°V	AC CHAR. per device

Ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134)

symbol	parameter	min.	max.	unit	conditions
V_{CC}	DC supply voltage	–0,5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0,5$ or $V_I > V_{CC} + 0,5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0,5$ or $V_O > V_{CC} + 0,5$ V
$\pm I_O$	DC output source or sink current				for $-0,5$ V $< V_O < V_{CC} + 0,5$ V
	– standard outputs		25	mA	
	– bus driver outputs		35	mA	
$\pm I_{CC}$;	DC V_{CC} or GND current for types with:				
$\pm I_{GND}$	– standard outputs		50	mA	
	– bus driver outputs		70	mA	
T_{stg}	storage temperature range	–65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: –40 to +125 °C
	plastic DIL		500	mW	above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", 11 V is specified as the maximum operating voltage. Voltages are referenced to GND (ground = 0 V).

DC characteristics for 74HC

symbol	parameter	T_{amb} (°C) 74HC +25 min.	+25 typ.	+25 max.	−40 to +85 min.	−40 to +85 max.	−40 to +125 min.	−40 to +125 max.	unit	test conditions V_{CC} V	V_I	other
V_{IH}	HIGH level input voltage	1,5	1,2		1,5		1,5		V	2,0		
		3,15	2,4		3,15		3,15			4,5		
		4,2	3,2		4,2		4,2			6,0		
V_{IL}	LOW level input voltage		0,8	0,5		0,5		0,5	V	2,0		
			2,1	1,35		1,35		1,35		4,5		
			2,8	1,8		1,8		1,8		6,0		
V_{OH}	HIGH level output voltage all outputs	1,9	2,0		1,9		1,9		V	2,0	V_{IH} or V_{IL}	$-I_O$ = 20 μA
		4,4	4,5		4,4		4,4			4,5		$-I_O$ = 20 μA
		5,9	6,0		5,9		5,9			6,0		$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage standard outputs	3,98	4,32		3,84		3,7		V	4,5	V_{IH} or V_{IL}	$-I_O$ = 4,0 mA
		5,48	5,81		5,34		5,2			6,0		$-I_O$ = 5,2 mA
V_{OH}	HIGH level output voltage bus driver outputs	3,98	4,32		3,84		3,7		V	4,5	V_{IH} or V_{IL}	$-I_O$ = 6,0 mA
		5,48	5,81		5,34		5,2			6,0		$-I_O$ = 7,8 mA
V_{OL}	LOW level output voltage all outputs		0	0,1		0,1		0,1	V	2,0	V_{IH} or V_{IL}	I_O = 20 μA
			0	0,1		0,1		0,1		4,5		I_O = 20 μA
			0	0,1		0,1		0,1		6,0		I_O = 20 μA
V_{OL}	LOW level output voltage standard outputs		0,15	0,26		0,33		0,4	V	4,5	V_{IH} or V_{IL}	I_O = 4,0 mA
			0,16	0,26		0,33		0,4		6,0		I_O = 5,2 mA
V_{OL}	LOW level output voltage bus driver outputs		0,15	0,26		0,33		0,4	V	4,5	V_{IH} or V_{IL}	I_O = 6,0 mA
			0,16	0,26		0,33		0,4		6,0		I_O = 7,8 mA
$\pm I_I$	input leakage current			0,1		1,0		1,0	μA	6,0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0,5		5,0		10,0	μA	6,0	V_{IH} or V_{IL}	V_O = V_{CC} or GND
	quiescent supply current											
	SSI			2,0		20,0		40,0	μA	6,0	V_{CC}	I_O = 0
I_{CC}	flip-flops			4,0		40,0		80,0	μA	6,0	or	I_O = 0
	MSI			8,0		80,0		160,0	μA	6,0	GND	I_O = 0

Voltages are referenced to GND (ground = 0 V).

DC characteristics for 74HCT

symbol	parameter	T_{amb} (°C) 74HCT +25 min.	+25 typ.	+25 max.	−40 to +85 min.	−40 to +85 max.	−40 to +125 min.	−40 to +125 max.	unit	test conditions V_{CC} V	V_I	other
V_{IH}	HIGH level input voltage	2,0	1,6		2,0		2,0		V	4,5 to 5,5		
V_{IL}	LOW level input voltage		1,2	0,8		0,8		0,8	V	4,5 to 5,5		
V_{OH}	HIGH level output voltage all outputs	4,4	4,5		4,4		4,4		V	4,5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage standard outputs	3,98	4,32		3,84		3,7		V	4,5	V_{IH} or V_{IL}	$-I_O$ = 4,0 mA
V_{OH}	HIGH level output voltage bus driver outputs	3,98	4,32		3,84		3,7		V	4,5	V_{IH} or V_{IL}	$-I_O$ = 6,0 mA
V_{OL}	LOW level output voltage all outputs		0	0,1		0,1		0,1	V	4,5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage standard outputs		0,15	0,26		0,33		0,4	V	4,5	V_{IH} or V_{IL}	I_O = 4,0 mA
V_{OL}	LOW level output voltage bus driver outputs		0,16	0,26		0,33		0,4	V	4,5	V_{IH} or V_{IL}	I_O = 6.0 mA
$\pm I_I$	input leakage current			0,1		1,0		1,0	μA	5,5	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0,5		5,0		10,0	μA	5,5	V_{IH} or V_{IL}	V_O = V_{CC} or GND per input pin; other inputs at V_{CC} or GND; I_O = 0
	quiescent supply current											
	SSI			2,0		20,0		40,0	μA	5,5	V_{CC}	I_O = 0
I_{CC}	flip-flops			4,0		40,0		80,0	μA	5,5	or	I_O = 0
	MSI			8,0		80,0		160,0	μA	5,5	GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4,5 to 5,5	V_{CC} -2,1V	other inputs at V_{CC} or GND; I_O = 0

1. The additional quiescent supply current per input is determined by the ΔI_{CC} unit load, which has to be multiplied by the unit load coefficient as given in the individual data sheets. For dual supply systems the theoretical worst-case (V_I = 2,4 V; V_{CC} = 5,5 V) specification is: ΔI_{CC} = 0,65 mA (typical) and 1,8 mA (maximum) across temperature.

Voltages are referenced to GND (ground = 0 V).

DC characteristics for 74HCU

symbol	parameter	T_{amb} (°C)							unit	test conditions		
		74HCU										
		+25			−40 to +85		−40 to +125			V_{CC}	V_I	other
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1,7	1,4		1,7		1,7		V	2,0		
		3,6	2,6		3,6		3,6			4,5		
		4,8	3,4		4,8		4,8			6,0		
V_{IL}	LOW level input voltage		0,6	0,3		0,3		0,3	V	2,0		
			1,9	0,9		0,9		0,9		4,5		
			2,6	1,2		1,2		1,2		6,0		
V_{OH}	HIGH level output voltage	1,8	2,0		1,8		1,8		V	2,0	V_{IH} or V_{IL}	$-I_O$ = 20 μA
		4,0	4,5		4,0		4,0			4,5		$-I_O$ = 20 μA
		5,5	6,0		5,5		5,5			6,0		$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3,98	4,32		3,84		3,7		V	4,5	V_{CC} or GND	$-I_O$ = 4,0 mA
		5,48	5,81		5,34		5,2			6,0		$-I_O$ = 5,2 mA
V_{OL}	LOW level output voltage		0	0,2		0,2		0,2	V	2,0	V_{IH} or V_{IL}	I_O = 20 μA
			0	0,5		0,5		0,5		4,5		I_O = 20 μA
			0	0,5		0,5		0,5		6,0		I_O = 20 μA
V_{OL}	LOW level output voltage		0,15	0,26		0,33		0,4	V	4,5	V_{CC} or GND	I_O = 4,0 mA
			0,16	0,26		0,33		0,4		6,0		I_O = 5,2 mA
$\pm I_I$	input leakage current			0,1		1,0		1,0	μA	6,0	V_{CC} or GND	
I_{CC}	quiescent supply current SSI			2,0		20,0		40,0	μA	6,0	V_{CC} or GND	I_O = 0

Voltages are referenced to GND (ground = 0 V).

AC characteristics for 74HC

symbol	parameter	T_{amb} (°C) 74HC +25 min.	typ.	max.	−40 to +85 min.	max.	−40 to +125 min.	max.	unit	V_{CC} V
t_{THL}/t_{TLH}	output transition time standard outputs		19	75		95		110	ns	2,0
			7	15		19		22		4,5
			6	13		16		19		6,0
t_{THL}/t_{TLH}	output transition time bus driver outputs		14	60		75		90	ns	2,0
			5	12		15		18		4,5
			4	10		13		15		6,0

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

AC characteristics for 74HCU

symbol	parameter	T_{amb} (°C) 74HCU +25 min.	typ.	max.	−40 to +85 min.	max.	−40 to +125 min.	max.	unit	V_{CC} V
t_{THL}/t_{TLH}	output transition line		19	75		95		110	ns	2,0
			7	15		19		22		4,5
			6	13		16		19		6,0

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

AC characteristics for 74HCT

symbol	parameter	T_{amb} (°C) 74HCT +25 min.	typ.	max.	−40 to +85 min.	max.	−40 to +125 min.	max.	unit	V_{CC} V
t_{THL}/t_{TLH}	output transition time standard outputs		7	15		19		22	ns	4,5
t_{THL}/t_{TLH}	output transition time bus driver outputs		5	12		15		18	ns	4,5

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

HCMOS Schmitt-trigger applications

JAN EXALTO

Digital systems often receive input signals that have long rise and fall times, for example filter output signals, data-link signals, transducer output signals and signals derived from oscillators or transformers. Theoretically, the high gain between the input and output of integrated logic elements results in a rectangular output pulse regardless of the rise and fall times of the input signal. However, when a slowly rising edge of an input signal reaches the switching threshold level of the IC, it starts to switch, and charge-dumping shifts the V_{CC} and ground levels slightly. This pulls the circuit back into the pre-switching state, thereby causing a jittering output. Also, as the input signal passes slowly through the switching threshold, the power dissipation increases due to the through current in the input stage. The rise and fall times of input signals to logic systems must therefore be kept short. Furthermore, if it is necessary to construct an RC oscillator from integrated logic inverters or inverting gates, two gates or inverters (4 signal pins) must be used. To overcome these problems, the 74HC/HCT/HCU family of HCMOS logic ICs includes two ICs with Schmitt trigger inputs. They are:

- 74HC/HCT14 Hex inverting Schmitt trigger
- 74HC/HCT132 Quad two-input NAND Schmitt trigger.

The advantages of using these two ICs for waveshaping and timing are:

- in common with all HCMOS ICs, they dissipate little power and have high input impedance. The latter allows a wide range of time-constants to be used without resorting to the use of expensive high-value capacitors which would also increase power dissipation
- they have high gain, so the output is a square wave regardless of the slope of the input, but unlike with integrated gates and inverters, glitches during the transition of the input signal through the switching threshold don't cause spurious oscillations, even with the parasitic capacitance between pins
- an RC oscillator built from a Schmitt trigger requires only two pins of the IC for the signal lines. RC oscillators using gates or inverters require four signal pins
- frequency and duty factor of Schmitt trigger oscillators are largely independent of temperature because the temperature sensitivity of the trigger thresholds is only ±60 mV over the temperature range −55 °C to +125 °C
- the additional NAND function of the 74HC/HCT132 is particularly useful for enabling/disabling clock-controlled-oscillators or timing circuits.

INTERNAL CIRCUITRY AND CHARACTERISTICS

Figures 1 and 2 are the logic diagrams of the HC/HCT14 and HC/HCT132. Each input has it own Schmitt trigger that switches independently, and the inputs and outputs are buffered. The inputs also have the standard HCMOS input circuitry for protecting the inputs against ESD as illustrated in Fig.3. The HCMOS family specifications for 74HC/HCT ICs also apply to the Schmitt trigger ICs unless specified differently in the individual data sheets.

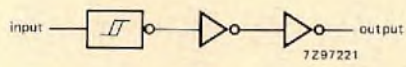


Fig.1 74HCT/HCT14 logic diagram

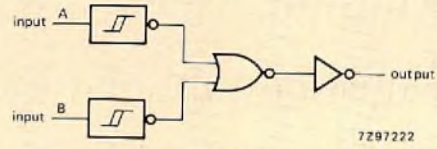


Fig.2 74HC/HCT132 logic diagram

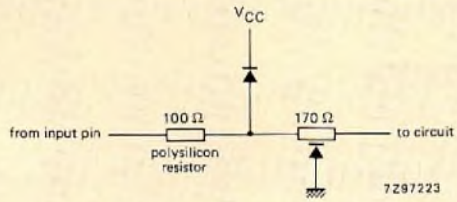


Fig.3 HCMOS input protection network

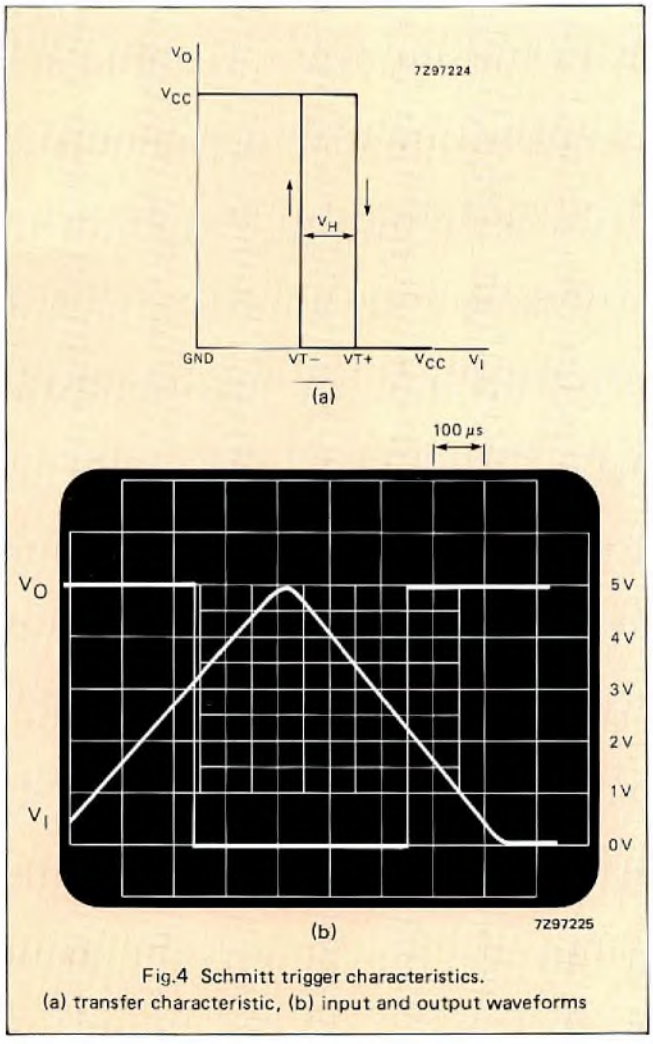


Fig.4 Schmitt trigger characteristics.
(a) transfer characteristic, (b) input and output waveforms

Figure 4(a) shows the transfer characteristic of a Schmitt trigger. The general shape of the characteristic is valid for all permissible values of V_{CC}, but the guaranteed maximum and minimum values of threshold voltages V_{T+} and V_{T-} are functions of V_{CC} as shown in the data sheets.

Figure 4(b) shows input and output waveforms illustrating the transfer characteristic of a 74HC132 Schmitt trigger with a 5 V supply and a triangular wave input. As the input voltage (V_I) increases from ground, the output remains HIGH until V_I reaches V_{T+}. At this point, the output goes LOW and remains LOW while V_I rises to V_{CC}. As V_I decreases from V_{CC}, the output remains LOW until V_I reaches V_{T-}. At this point, the output goes HIGH. By definition, the hysteresis is the difference between the HIGH tripping level (V_{T+}) and the LOW tripping level (V_{T-}).

In this example, it can be seen that V_{T+} is 3,25 V and V_{T-} is 2,25 V, giving hysteresis of 1 V. For a 74HCT Schmitt trigger, the trigger levels are lower and the minimum specified V_{T-} is 0,5 V which is less than the family specification figure of $V_{IL\,max}$ = 0,8 V for other 74HCT ICs. If a design is made with respect to the worst-case TTL-compatible input levels for 74HCT ICs ($V_{IL\,max}$ = 0,8 V and $V_{IH\,min}$ = 2,0 V), a 74HCT Schmitt trigger has less noise immunity than a 74HC type.

APPLICATIONS

Most of the applications described in this article use the 74HC/HCT132, but in circuits where both inputs are connected together, or one input is connected to V_{CC}, the 74HC/HCT14 can be used.

Waveshaping

One of the most common waveshaping applications for Schmitt triggers is in sine-to-square-wave converters like the one shown in Fig.5. The capacitive coupling removes any d.c. component from the input sine wave. The voltage divider provides a d.c. bias of $V_{CC}/2$ to allow maximum swing of the sine wave without clipping.

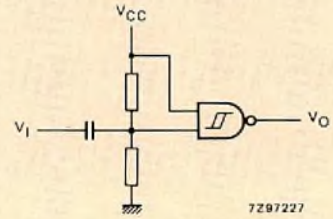


Fig.5 Sine to square-wave converter

Timing and delay

Signal delay is often provided by simple discrete RC networks. Unfortunately, if a high capacitance is used, the rise and fall-times of the delayed signal are increased considerably, causing jittering and synchronization problems. Schmitt trigger delay circuits overcome these problems since their high input-impedance allows a high-value resistor, and hence a low-value inexpensive capacitor, to be used in the RC network.

The simplest way to delay a pulse is shown in Fig.6(a). The input's leading edge is delayed by:

$$t_{d+} = RC \ln \frac{V_{CC}}{V_{CC} - V_{T+}}.$$

Its trailing edge is delayed by:

$$t_{d-} = RC \ln \frac{V_{CC}}{V_{T-}}.$$

Unfortunately, in this simple circuit, the same RC network delays both edges of the input signal (see Fig.6(b)). In many applications, only one edge has to be delayed or the edges have to be delayed by different amounts. Figure 7 shows a circuit that can delay the positive-going edge by the longest RC time and negative-going edge by the shortest RC time.

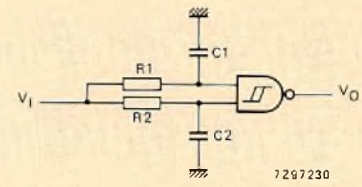


Fig.7 Circuit for delaying the positive-going and negative-going edges of an input by different amounts

If only one edge need be delayed, then the circuit shown in Fig.8 can be used to delay the positive-going edge. If the negative-going edge must be delayed, the signal must first be inverted.

Pulse generation

In digital systems, it is often necessary to generate an edge-triggered pulse. A circuit commonly used for this is given in Fig.9. Unfortunately, this circuit is sensitive to noise on the power-supply. If there is a spike on the supply line while the input is HIGH, a pulse with the same duration as the spike is transmitted from the output of the previous stage via the input capacitor. So, it's better to use the circuit shown in Fig.10 which, although more complex, has higher noise-immunity.

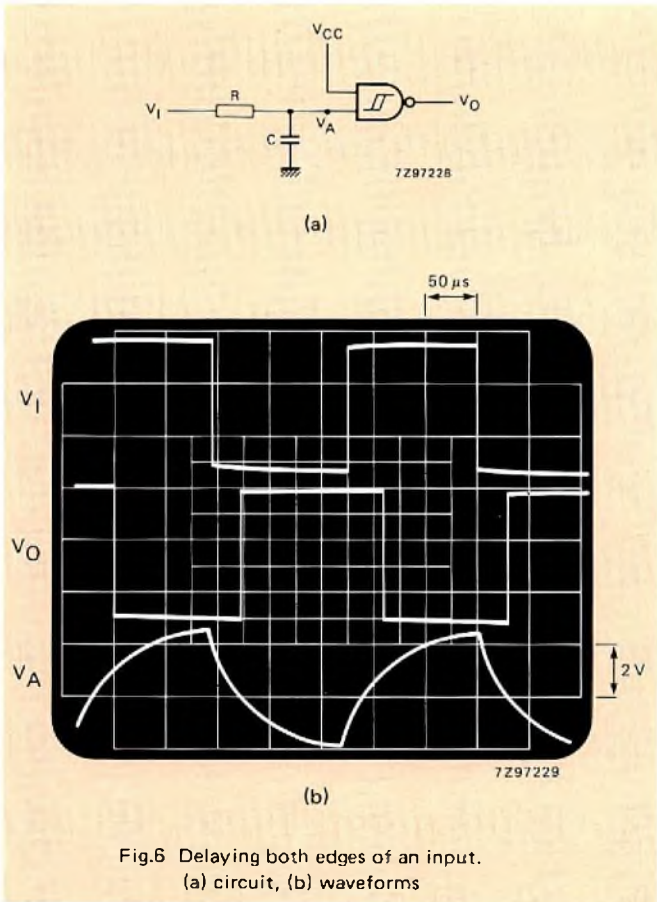


Fig.6 Delaying both edges of an input. (a) circuit, (b) waveforms

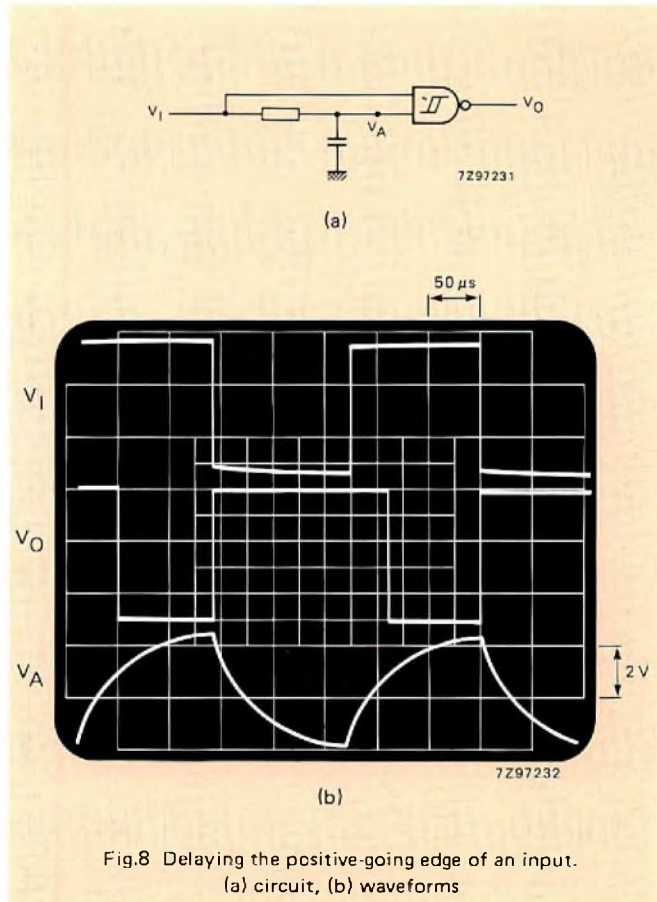


Fig.8 Delaying the positive-going edge of an input. (a) circuit, (b) waveforms

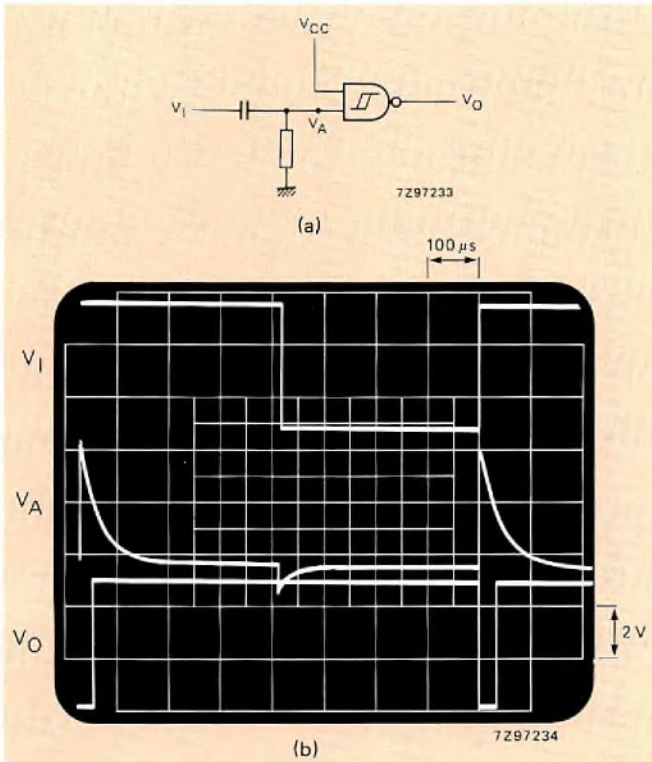


Fig.9 Generating a pulse coincident with positive-going edge of the input signal. (a) circuit, (b) waveforms

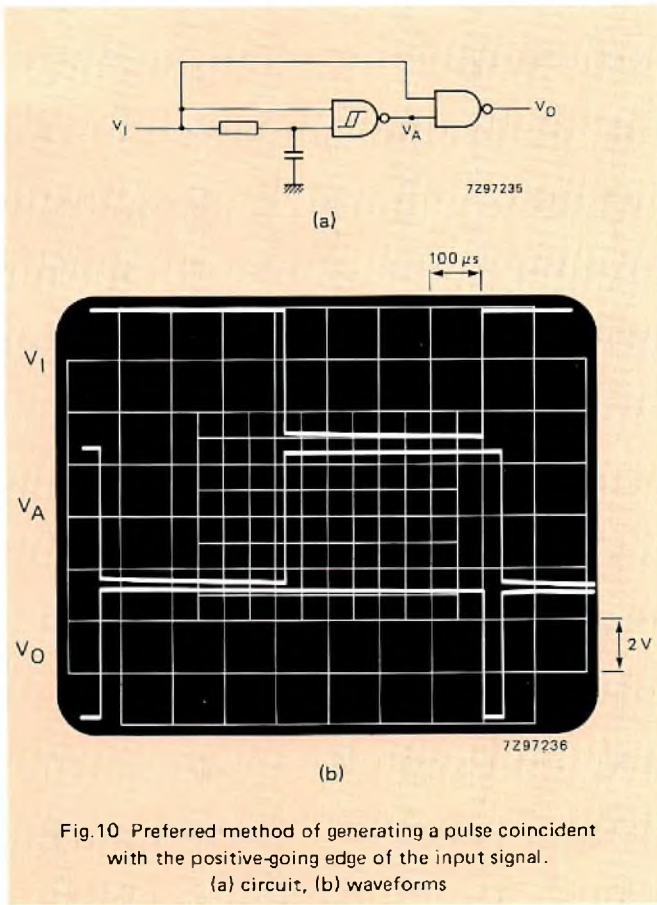


Fig.10 Preferred method of generating a pulse coincident with the positive-going edge of the input signal. (a) circuit, (b) waveforms

Oscillators

The circuit of a simple relaxation oscillator is given in Fig.11. The second input of the 2-input NAND Schmitt trigger HC/HCT132 can be used as an enable/disable for the oscillator. This is often required in battery-powered equipment to set an oscillator to the 'standby' mode to reduce power consumption.

The HIGH and LOW periods (t_1 and t_2) for the oscillator are:

$$t_1 = RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}$$

$$t_2 = RC \ln \frac{V_{T+}}{V_{T-}}$$

$$t_1 + t_2 = RC \ln \frac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})}.$$

These expressions are only valid if the value of the resistor is high-enough to ensure that the output voltage drop is negligible. This must be checked against the family specification.

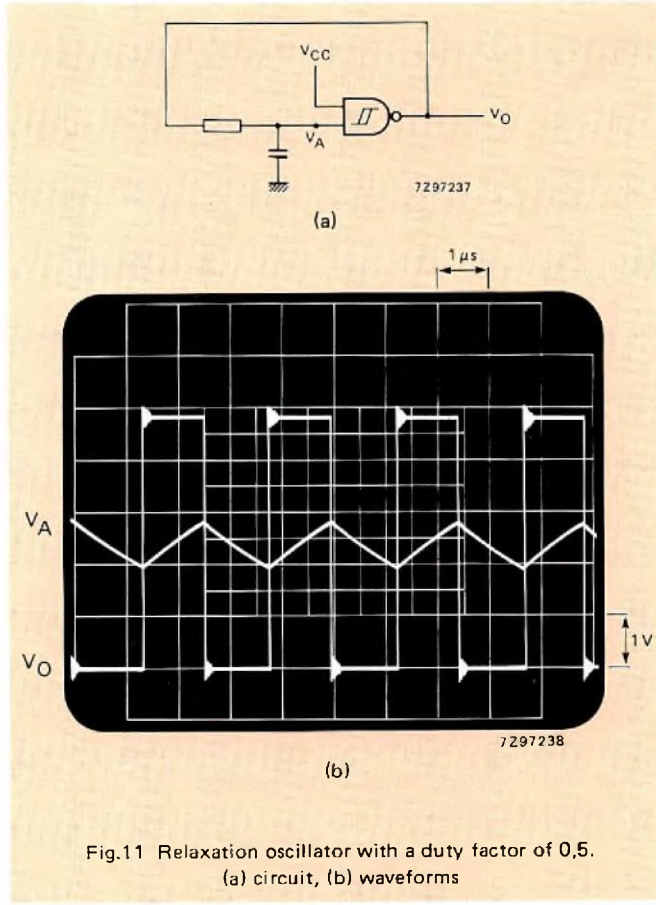


Fig.11 Relaxation oscillator with a duty factor of 0,5. (a) circuit, (b) waveforms

TABLE 1
Power dissipation due to average through current during switching

type	V_{CC} (V)	power dissipation (mW)	average through-current (μA)
74HC14	2	0,096	48
	4.5	2,16	480
	6,0	5,3	880
74HC132	2.0	0.08	40
	4,5	1,85	410
	6,0	4,44	740

As the Schmitt-trigger input swings between V_{T+} and V_{T-} (the linear region of operation), the through-current I_{CC} in the input stage is maximum. The average through current and its power dissipation are indicated in Table 1. Although this power dissipation during switching is usually higher than that of an RC oscillator using HCMOS gates or inverters, this circuit does have the important advantage of requiring only two pins for the signal connections.

The frequency and duty factor of this oscillator depend on the ratio V_{T+}/V_{T-}. Since this ratio remains almost constant with supply voltage variations, these have little influence on the duty factor or frequency. However, since the ratio V_{T+}/V_{T-} varies with switching level spreads between ICs, the influence of these on the duty factor and frequency can be considerable. The resistor in the RC network should therefore be made adjustable to compensate for switching level spreads between individual ICs.

The frequency of the oscillator as a function of supply voltage with RC time as a parameter is shown in Fig.12.

The duty factor is 0,5 when the tripping levels (V_{T+} and V_{T-}) are symmetrical about $V_{CC}/2$. The waveforms in Fig.11 illustrate that, in this example, the duty factor is almost 0,5. To obtain a duty factor of exactly 0,5, the oscillator can be run at twice the frequency and its output divided by a flip-flop.

Another way to alter the duty factor is to use the circuit in Fig.13(a). With this arrangement, the LOW and HIGH periods are individually set by resistors R_1 and R_2 respectively. In Fig.13(b), the HIGH period is much longer than the LOW period ($R_2 > R_1$), and in Fig.13(c), the LOW period is much longer than the HIGH period ($R_1 > R_2$). A controlled Schmitt-trigger oscillator can also be designed as shown in Fig.14. Note that the first LOW period is considerably longer than subsequent LOW periods. This is because the capacitor's initial charge is higher. The duration of the first LOW period is:

$$t = RC \ln \frac{V_{CC}}{V_{T-}}.$$

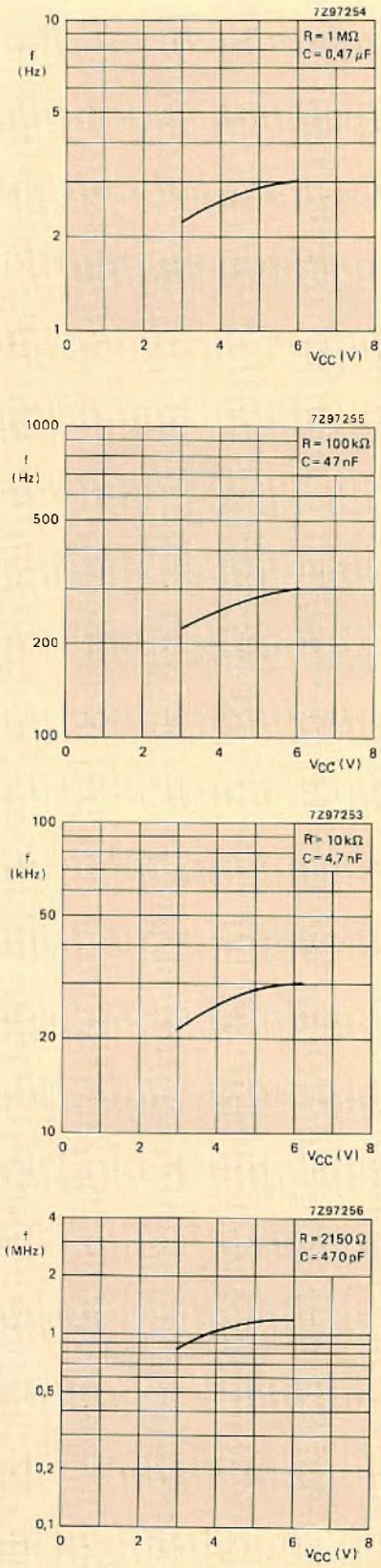


Fig.12 Frequency as a function of supply voltage with time-constant as a parameter for Schmitt trigger RC oscillators according to the circuit of Fig.11

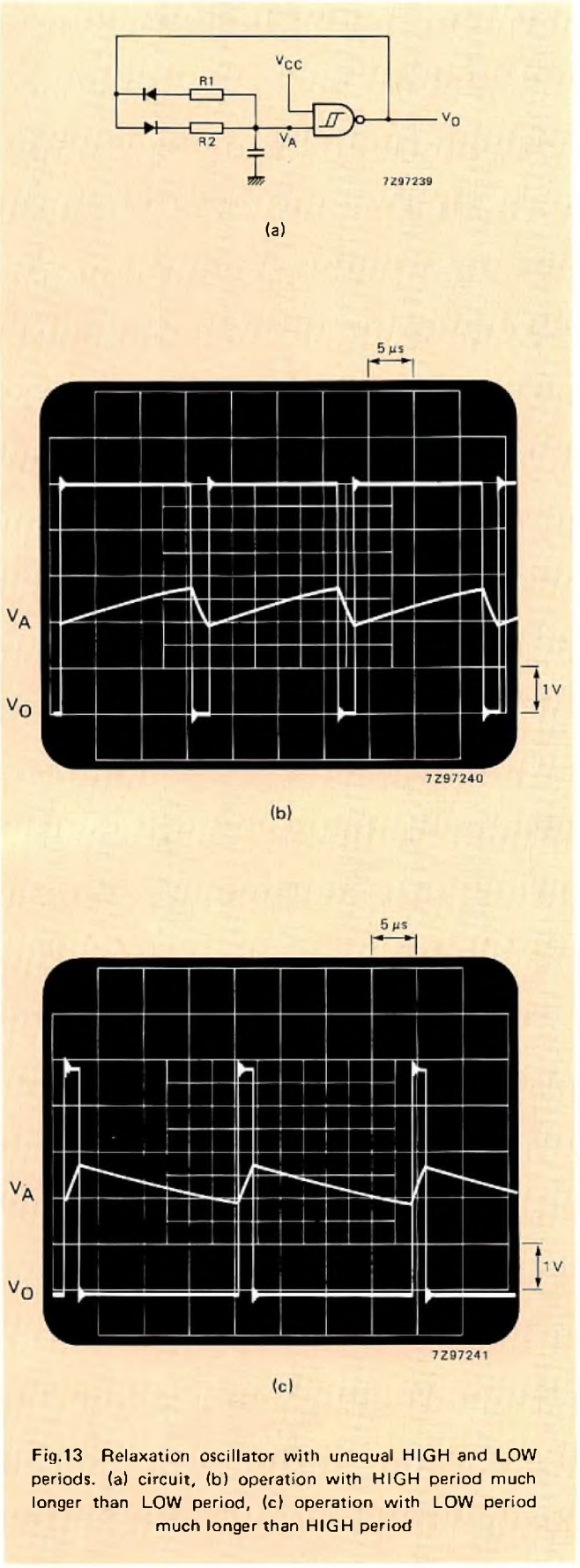


Fig.13 Relaxation oscillator with unequal HIGH and LOW periods. (a) circuit, (b) operation with HIGH period much longer than LOW period, (c) operation with LOW period much longer than HIGH period

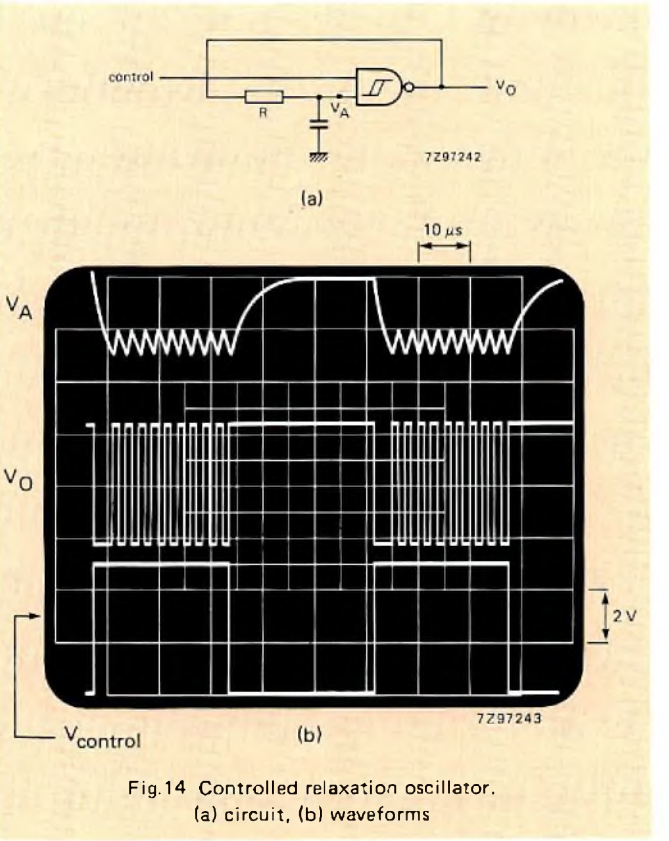


Fig.14 Controlled relaxation oscillator. (a) circuit, (b) waveforms

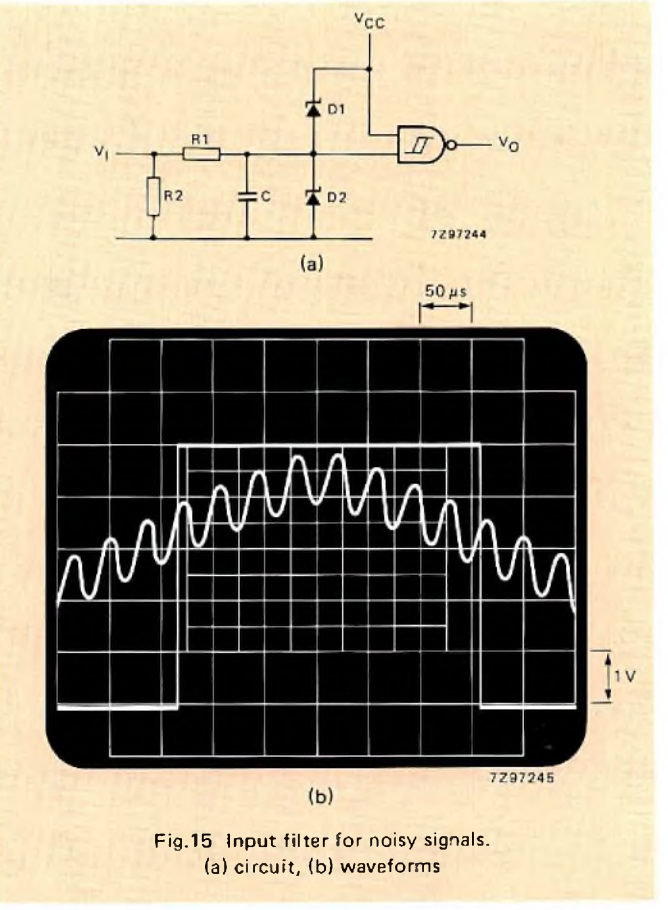


Fig.15 Input filter for noisy signals. (a) circuit, (b) waveforms

Input filtering

Input signals to digital systems are often very noisy. This problem can be solved with an input filter made with a Schmitt trigger as shown in Fig.15.

Resistor R_2 can also be a pull-up resistor connected to V_{CC} if this suits the system better. The time-constant chosen depends on the amount of noise and on the permissible speed reduction. The two diodes should be Schottky types (e.g. BAT85). They ensure that the current through the internal input protection diodes does not exceed the maximum rating. Figure 15(b) illustrates the effectiveness of this filter by comparing its output with its input.

CIRCUIT DESIGN CRITERIA

Family specification

All circuit calculations must be based on the guaranteed parameters given in the 74HC/HCT/HCU family specification. However, no specific parameters are given for oscillators. This is because external components define the performance of the oscillator. The values of these components must therefore be calculated from the data in the family specification to ensure that input/output currents and maximum dissipation are not exceeded.

Value limits for timing resistors

For predictable operation, the minimum values for timing resistors are dictated by the output drive available. For the 74HC132 with a supply voltage of 4,5 V, V_{OL} max and V_{OH} min are 0,4 and 3,7 V respectively, with an output current of 4 mA. Also, V_{T+} max is 3,15 V and V_{T-} min is 0,9 V. The minimum value for the timing resistor when the output is LOW is:

$$R_{min} = \frac{V_{T+\,max} - V_{OL\,max}}{I_{OL}} = \frac{3{,}15 - 0{,}4}{0{,}004} = 688\ \Omega.$$

When the output is HIGH, the minimum value for the timing resistor is:

$$R_{min} = \frac{V_{OH\,min} - V_{T-\,min}}{I_{OH}} = \frac{3{,}7 - 0{,}9}{0{,}004} = 700\ \Omega.$$

For this example, R_{min} at V_{CC} = 4,5 V is therefore 700 Ω. To keep the voltage drop due to leakage current low, the maximum value for timing resistors is 1 MΩ.

Power dissipation due to through-current in the input stage

Figure 16 shows the typical power dissipation ($V_{CC}I_{CC}$) due to through current in the first stage for the 74HC14 and 74HC132 Schmitt triggers as a function of supply voltage. The power dissipation is almost frequency-independent up to 25 kHz, but above this frequency there is a slight increase. By 2 MHz the power dissipation has doubled.

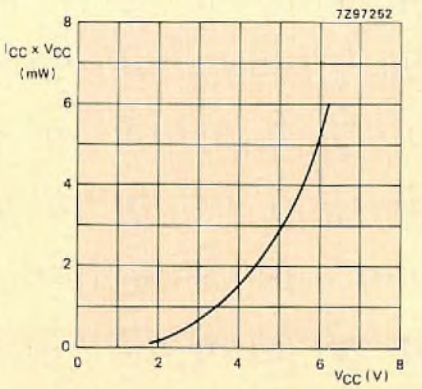


Fig.16 Typical power dissipation due to through-current in the first stage for the 74HC/HCT14 and 74HC/HCT132 Schmitt trigger as a function of supply voltage

Total power dissipation

The total power dissipation consists of:

$$P_{osc} = fC_tV_H^2 + fV_{CC}^2(C_{PD} + C_L) + V_{CC}I_{CC}$$

where:

V_H = hysteresis ($V_{T+} - V_{T-}$)

f = frequency

V_{CC} = supply voltage

C_t = the timing capacitance

C_{PD} = the equivalent device power dissipation capacitance given in the data sheets

C_L = the output load capacitance

I_{CC} = the average through current when the input swings between V_{T+} and V_{T-}. It is proportional to $(0{,}5V_{CC} - 0{,}7\ V)^2$. The average through currents for the 74HC14 and 74HC132 used as RC oscillators are shown in Table 1 and Fig.16.

Maximum oscillator frequency

To avoid propagation delay effects, the frequency of oscillators should be kept well below:

$$f_{osc\,max} = \frac{1}{t_{PHL} + t_{PLH}}$$

where:

t_{PHL} = the propagation delay for a HIGH to LOW transition

t_{PLH} = the propagation delay for a LOW to HIGH transition.

Using 74HCT HCMOS to replace LSTTL and drive transmission lines

ROB VOLGERS

Before the introduction of our 74HC/HCT/HCU high-speed CMOS (HCMOS) family of logic ICs, designers of high-speed logic systems were restricted to the use of power-hungry bipolar ICs such as LSTTL. Since the logic ICs of the HCMOS family can operate as fast as LSSTL but consume much less average power, and since they can operate over a wider supply voltage range, using them to replace LSTTL results in considerable system economies for both new and existing logic system designs. HCMOS ICs with the suffix 74HCT are purpose-designed for the latter application. Not only are they pin- and function-compatible with their LSTTL counterparts, they also have TTL-compatible input voltage levels and the same fanout as LSTTL (10 LSTTL loads). They can therefore be simply inserted in place of bipolar LSTTL logic ICs of the same type without the need for any redesign to achieve wider noise margins. What's more, they dissipate much less power, are more reliable and allow the use of simpler power supplies and cooling arrangements than those required for LSTTL. This article compares the input/output structures and performance of LSTTL and 74HCT logic ICs and discusses interfacing and low-power techniques for driving terminated data transmission lines with 74HCT ICs.

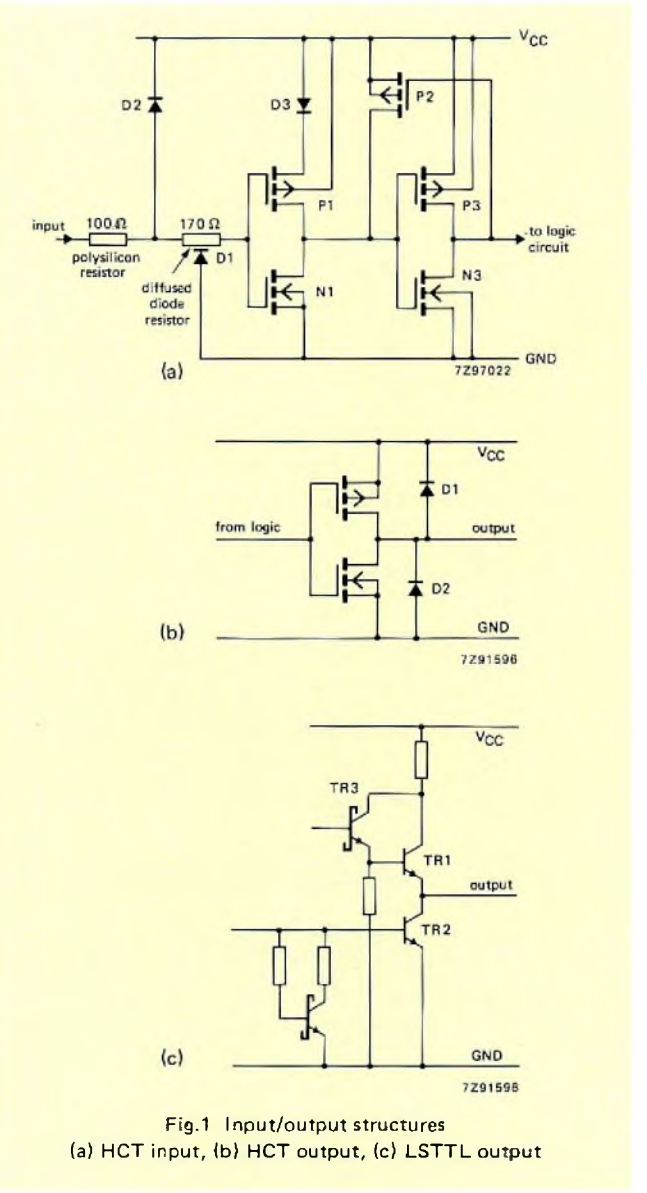


Fig.1 Input/output structures
(a) HCT input, (b) HCT output, (c) LSTTL output

INPUT/OUTPUT CHARACTERISTICS OF LSTTL AND 74HCT ICs

Input characteristics

The input structure of 74HCT ICs is shown in Fig.1(a). The resistor/diode network protects the input against electrostatic discharge by clamping input voltages which exceed the supply rails to V_{CC} or ground. Under normal operating conditions, the input voltage should swing within the supply voltage limits (V_{CC} and ground) to prevent current flow through diodes D_1 and D_2. The maximum permitted d.c. through these diodes is 20 mA.

If MOS transistors P1 and N1 were identical they would have a switching threshold of $V_{CC}/2$ (as in 74HC ICs). A minimum HIGH level derived from an LSTTL output (2,7 V), although being recognized as a logic "1" would then allow both input transistors to partially conduct, causing a flow-through current between V_{CC} and ground and increasing power dissipation. To prevent this, N1 is enlarged in 74HCT ICs and level shifting diode D3 is incorporated between the drain of P1 and V_{CC}. The effect of D3, combined with N1 having higher gain than N2, is to reduce the input switching threshold to 1,4 V typical which matches that of LSTTL. Unlike LSTTL inputs however, 74HCT inputs present a purely capacitive load to a driving IC and therefore draw only a small leakage current when quiescent. The maximum leakage current into 74HCT inputs held in the HIGH or LOW state is only 1 μA. This is essentially zero when compared with the input current of LSTTL which is 400 μA in the LOW state and 20 μA in the HIGH state.

The main consequence of 74HCT inputs having a much higher impedance than LSTTL inputs is, of course, a considerable reduction of power dissipation which simplifies power supplies, cooling arrangements and battery back-up. A drawback however is that a 74HCT input creates a high impedance termination for a transmission line. This will cause reflections and consequent corruption of data unless the line is terminated with its characteristic impedance formed by a discrete termination network. This is explained in more detail in the Appendix.

Output characteristics

The output structure of a 74HCT IC is shown in Fig.1(b). With an output current of 20 μA, the LOW to HIGH output level swing is from 0,1 V to V_{CC} – 0,1 V. With an output current of 4 mA (6 mA for bus drivers) V_{OH} min is 0,66 V below V_{CC}, and V_{OL} max is 0,33 V. Figure 2 shows that, when a 74HCT output is at worst-case LSTTL output levels (V_{OH} = 2,7 V min. and V_{OL} = 0,5 V max.), it can source 8 mA (12 mA for bus drivers) and sink 6 mA (9 mA for bus drivers) with a 4,5 V supply.

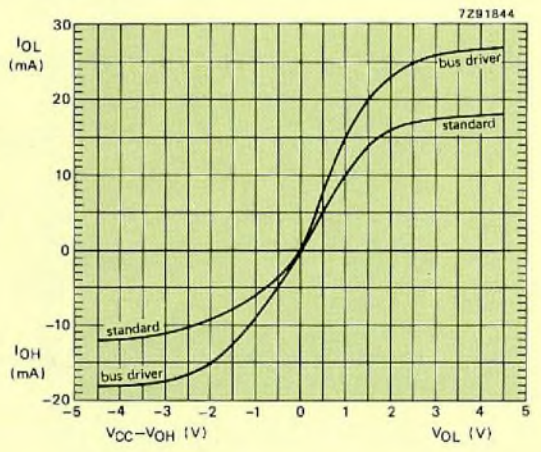


Fig.2 Minimum output drive characteristics for 74HCT ICs (V_{CC} = 4,5 V, T_{amb} = 85 °C)

In contrast, the HIGH output level for the LSTTL output structure shown in Fig.1(c) is limited by the V_{BE} of TR_1 and TR_3 and the voltage drop across the collector resistor. Over the full temperature range, V_{OH} can therefore be as low as 2,7 V at I_{OH} max with the minimum supply voltage (4,75 V). The LOW output level for LSTTL is the saturation V_{CE} of TR_2. Even if a source current flows out of the output, V_{OL} will not exceed 0,5 V.

The main consequence of 74HCT ICs having a wider output voltage swing than LSTTL ICs is that the noise immunity of a 74HCT logic system is much greater than that of a comparable LSTTL system.

PERFORMANCE COMPARISON

Of paramount importance for the replacement of LSTTL ICs with 74HCT types is the identical input voltage specifications and nominal operating voltage for the two technologies. The maximum LOW input level is 0,8 V; the minimum HIGH input level is 2 V; the nominal operating voltage is 5 V.

The Table compares all applications-related parameters of 74HCT and LSTTL ICs. The following comparisons which are based on the figures in the Table show that 74HCT ICs not only easily replace LSTTL ICs, they also enhance system performance in many respects.

Quiescent power dissipation

The quiescent power dissipation of 74HCT ICs is due only to small leakage currents flowing between V_{CC} and ground and is essentially zero compared with that of LSTTL ICs. However, when a 74HCT input is driven by a TTL minimum HIGH level of (V_{CC} – 2,1 V), a small current is drawn from V_{CC}. This current is called additional quiescent supply current (ΔI_{CC}) and is specified on a per input basis in the d.c. characteristics for HCT ICs. Since all LSTTL ICs (except some bus drivers) have a higher minimum HIGH level (2,7 V) than TTL ICs, the published figures for the additional quiescent supply current can be halved when 74HCT ICs are driven by LSTTL.

Dynamic power dissipation

Unlike the dynamic power dissipation of LSTTL, the dynamic power dissipation of 74HCT ICs is due to the charge and discharge of capacitive loads and is therefore frequency-dependent. It is only comparable to that of LSTTL ICs at high operating frequencies. Generally, it is much lower because average data transmission rates are less than 1 MHz. A full discussion on 74HC/HCT power dissipation and how to calculate it is given in the section Power Dissipation.

Comparison of characteristics of 74HCT and LSTTL circuits (V_{CC} = 5 V unless stated otherwise)

characteristic	74HCTXXX			74LSXXX	
max. quiescent power dissipation over temp. range at V_{CC} max					
per gate (mW)	0,027			6	
per flip-flop (mW)	0,11			22	
per 4-stage counter (mW)	0,44			175	
per transceiver/buffer (mW)	0,055			60	
max. dynamic power dissipation (C_L = 50 pF)					
at f_i (MHz)	*0,1*	*1*	*10*	*0,1 to 1*	*10*
per gate (mW)	0,25	2,25	22	6	22
per flip-flop (mW)	0,35	2,5	24	22	27
per 4-stage counter (mW)	0,70	3	27	175	200
per buffer/transceiver (mW)	0,30	2,5	24	60	90
operating supply voltage (V)	4,5 to 5,5			4,75 to 5,25	
operating temperature range (°C)	−40 to +85 −40 to +125			0 to +70	
max. noise margin (H/L in V)	2,9/0,7			0,7/0,4	
input switching voltage stability over temp. range	±60 mV			±200 mV	
min. output drive current at T_{max} and $V_{CC\ min}$ (mA) source current (V_{OH} = 2,7 V)*					
standard logic	− 8			−0,4	
bus logic	−12			−2,6	
sink current					
standard logic (V_{OL} = 0,4 V)	4			4	
standard logic (V_{OL} = 0,5 V)	6			8	
bus logic (V_{OL} = 0,4 V)	8			12	
bus logic (V_{OL} = 0,5 V)	9			24	
typ. output transition time (ns) (C_L = 15 pF) standard logic					
t_{TLH}	6			15	
t_{THL}	6			6	
bus logic					
t_{TLH}	4			15	
t_{THL}	4			6	
typ. propagation delay (ns) (C_L = 15 pF)**					
gate t_{PHL}/t_{PLH}	8/8			8/11	
flip-flop t_{PLH}	14			15	
flip-flop t_{PHL}	14			22	
typ. clock rate of a flip-flop (MHz)	50			33	
max. input current (μA)					
I_{IL}	−1			−400 to −800	
I_{IH}	1			40	
3-state output leakage current (μA)	±5			±20	

* V_{OH} for a few LSTTL bus outputs is specified as 2,4 V.
** Refer to data sheets for the effect of capacitive loading.

Supply voltage

74HCT ICs need much less voltage regulation than LSTTL ICs. They operate from a nominal supply of 5 V, the same as LSTTL. The permitted supply voltage deviation from the nominal value for 74HCT (±10%) is twice as much as that for LSTTL (±5%).

Operating temperature range

The operating temperature range for 74HCT ICs is −40 °C to +125 °C. This is less limiting than the 0 °C to +70 °C specified for 74LSTTL.

Noise immunity

Replacing LSTTL with 74HCT can considerably increase the noise immunity of a logic system. For a totally 74HCT system with a 4.5 V supply, the noise margins are 53% of V_{CC} (HIGH) and 14% of V_{CC} (LOW) with one 74HCT output driving 20 74HCT inputs. For an LSTTL system with a 4.75 V supply they are 15% of V_{CC} (HIGH) and 8% of V_{CC} (LOW). However, if the full drive capability of 74HCT bus logic is exploited (driving a d.c. terminated transmission line for example), the 74HCT output levels will be the same as those for LSTTL and the noise immunity will also be the same.

Stability of input switching threshold

The switching threshold of the input pair of CMOS transistors in 74HCT ICs (1.4 V) is the same as that of LSTTL but it is less temperature dependent than that of the diode input circuitry of LSTTL. The noise margin of 74HCT ICs therefore remains more stable over the operating temperature range. RC astable multivibrators are also less susceptible to temperature variations.

Timing

The sizes of the p-channel/n-channel MOS transistors in the push-pull output stages of 74HCT ICs are adjusted to obtain saturation currents which result in equal output transition times ($t_{TLH} = t_{THL}$). The sizes of the p-channel/n-channel MOS transistors in all the symmetrical logic circuitry stages are adjusted to obtain equal propagation delays ($t_{PHL} = t_{PLH}$).

Maximum clock frequency

The maximum clock frequencies of 74HCT ICs are comparable to those of equivalent LSTTL ICs.

Input current

An important difference between systems using LSTTL and 74HCT ICs is the relatively high constant direct current that flows in LSTTL interconnect wiring. In comparison, the current flowing into 74HCT inputs is essentially zero. Typically, only a few pA of reverse current flows in the input diodes. This results in better buffering and a wider frequency range for RC oscillators and time delay circuits constructed from 74HCT ICs.

Leakage current of 3-state outputs

Since the leakage current of the 3-state outputs of 74HCT bus drivers in the high-impedance state is only a quarter that of LSTTL circuits, the values of pull-up/pull-down resistors for bus drivers with 3-state outputs can be increased to reduce power dissipation.

Output drive current

The guaranteed minimum source current for HCT ICs is much higher than that of LSTTL and is matched to the sink current to achieve balanced L/H and H/L transition times. The sink current of 74HCT ICs is lower than that of LSTTL ICs to minimize current spiking and electromagnetic radiation, but is sufficient for LSTTL interfacing requirements. This article discusses the influence of the lower sink current and higher input impedance of 74HCT ICs on line terminations; the only area of logic system design which may be affected when replacing LSTTL ICs with 74HCT equivalents.

LSTTL/HCT INTERFACING

The following worst-case figures are based on systems with a single nominal 5 V supply and using standard logic with each output driving ten inputs.

Driving 74HCT from LSTTL

The LSTTL output/74HCT input levels for a worst-case single supply voltage (4.75 V) are:

LSTTL	*74HCT*
$V_{OL\,max} = 0.4$ V	$V_{IL\,max} = 0.8$ V
$V_{OH\,min} = 2.7$ V	$V_{IH\,min} = 2$ V.

This allows direct interfacing. The maximum current flowing into each 74HCT input is only 1 μA. This means that the 74HCT input structure presents a true CMOS type d.c. load resulting in a high fanout. The HIGH and LOW noise margins will be the same as those for an all LSTTL system.

Driving LSTTL from 74HCT

The 74HCT output/LSTTL input levels for a worst-case single supply voltage (4,75 V) are:

74HCT	*LSTTL*
V_{OL} max = 0,33 V	V_{IL} max = 0,8 V
V_{OH} min = 4,1 V	V_{IH} min = 2 V.

This again allows direct interfacing. The LOW level noise margin will be 70 mV greater than that for an all LSTTL system, and the HIGH level noise margin will be 1,4 V greater.

Driving 74HCT from 74HCT

The 74HCT output/input levels for a worst-case single supply voltage (4,5 V) are:

74HCT output	*74HCT input*
V_{OL} max = 0,1 V	V_{IL} max = 0,8 V
V_{OH} min = 4,4 V	V_{IH} min = 2 V.

The LOW level noise margin will be 0,3 V greater than that with LSTTL, and the HIGH level noise margin will be 1,7 V greater.

74HCT to 74HCT drive capability is expressed as minimum guaranteed source/sink current at a specified output voltage as shown in Fig.2. Since a quiescent 74HCT input draws a maximum of 1 μA, the unit-load (UL) concept as used for LSTTL doesn't apply. Instead, consideration must be given to charging/discharging capacitive loads. With a specified LOW output level of 0,33 V, a standard logic 74HCT output can sink 4 mA which is equivalent to driving 4000 74HCT inputs. Even with a specified low output level of 0,1 V, a standard output can still sink 20 μA which means that it can drive twenty 74HCT inputs.

TERMINATION OF UNUSED INPUTS

Termination of unused LSTTL inputs is not absolutely necessary because all inputs have an internal pull-up of 2200 Ω. However, if good design practice has been followed, all unused inputs of LSTTL ICs will be terminated to prevent any possibility of linear operation of the input circuitry, which would considerably increase power consumption. Unlike LSTTL inputs, the impedance of 74HCT inputs is very high and, if unused, they must be terminated to prevent the input circuitry floating into the linear mode of operation, which would cause extra supply current flow or oscillation. Unused 74HCT inputs can be terminated by connecting them to V_{CC} or ground, either directly, or via resistors of between 1 kΩ and 1 MΩ. Since the value of terminating resistors for unused inputs of LSTTL ICs is usually between 220 Ω and 1,2 kΩ, it will often be possible to directly replace LSTTL circuits with their 74HCT counterparts.

SUPPLY DECOUPLING

General requirements for power supply decoupling are discussed in the User Guide section of the Data Handbook or the Designer's Guide. In any circuitry for driving terminated lines, the supply to each IC must be decoupled to ground by a ceramic capacitor of at least 10 nF. The capacitor should be as close as possible to the ground pin of the IC to minimize inductance, which could cause ringing in the ground of the IC. If ringing persists when a 74HCT IC is driving a terminated line, and this ringing or noise is above or near the input switching threshold (1,4 V), the receiving IC should be replaced by an HC type which has a higher input switching threshold ($V_{CC}/2$) than 74HCT or LSTTL ICs.

In critical applications where hardly any noise can be tolerated, the supply to the circuit board or card can be decoupled by a low-pass RC filter consisting of a 10 Ω or lower value resistor of adequate power rating in series with the supply to the ICs and a 33 μF or higher value capacitor in parallel with the supply input. This filter should be at the point where the supply voltage enters the board or card.

DRIVING DATA LINES

Printed circuit-board tracks or striplines are used to carry data on circuit-boards, but twisted pairs of wires and coaxial cables are often used to carry data over longer distances in a system or in a large backplane. The lines are considered to be electrically long and will behave as transmission lines if the time taken for a transition to travel the length of the line and return exceeds the rise or fall time of the transition. If an electrically long line is not terminated with its characteristic impedance (for example, with the inputs of 74HCT ICs, which have a much higher impedance than those of LSTTL ICs), reflections will occur and cause ringing which can corrupt high speed data. This is explained in more detail in the Appendix.

Driving a pcb track multi-transistor data bus

One of the major uses of logic ICs is in computer and microprocessor-based systems incorporating transceivers, octal latches, and line drivers with 3-state outputs connected to a data bus consisting of a pcb track. The 3-state outputs allow several driver ICs to be connected to the same bus because they remain in the high-impedance state when inactive.

Even if a 3-state 74HCT bus isn't long enough to act as a transmission line, it must be terminated with a pull-up/pull-down resistor to prevent noise pick-up if it remains in the high-impedance state for more than 100 μs. However, it is good practice to always terminate a 3-state bus in case the system stops momentarily in the high impedance state or there is noise in the system due to crosstalk. Choice of

either a pull-up or pull-down resistor will depend on whether a HIGH or LOW state is required on the bus during the high impedance state. Choice of the resistor value is a compromise between power dissipation and bus speed. A higher resistance will reduce power dissipation but will increase the time-constant in conjunction with the bus capacitance and increase the time needed for pull-up/pull-down. A lower resistance will speed up the bus but will dissipate more power. Typical values of pull-up resistors are 220 Ω to 1,2 kΩ for LSTTL and 750 Ω to 1 MΩ for 74HCT. Typical values of pull-down resistors are 680 Ω to 1 kΩ for LSTTL and 1 kΩ to 1 MΩ for 74HCT. Pull-up/pull-down resistors should be positioned as far as possible from the bus drivers. Multiple terminating resistors can be distributed along the bus, but their individual values must then be high enough to ensure that the total parallel pull-up or pull-down resistance is not less than the values previously mentioned.

Driving a stripline multi-transmitter data bus

The propagation delay along a stripline on a glass-epoxy pcb is 7,2 ns/m. With rise and fall times of 4 ns, the bus is considered to be electrically long if it exceeds 28 cm. In the unlikely event of a 3-state pcb wiring bus with multiple drivers being much longer than this, it must consist of a stripline terminated at both ends by its characteristic impedance to prevent reflections corrupting the transmitted data (see Appendix). Such a stripline usually consists of a 0,6 mm track on one side of a 1,6 mm thick glass-epoxy pcb, and a groundplane on the other. This has a characteristic impedance of 120 Ω. An arrangement for terminating this type of bus for LSTTL circuits is shown in Fig.3. The output of the LSTTL driver has to sink 47 mA at a V_{OL} of 0,5 V, and the total power dissipated by the driving IC and the terminating network in the LOW state is more than 250 mW.

74HCT bus drivers cannot be used to replace LSTTL ICs driving a 120 Ω stripline more than 28 cm long in the arrangement of Fig.3 because:

– the required sink current (47 mA) far exceeds the guaranteed minimum sink current of 10 mA specified at V_{OL} = 0,5 V for a 74HCT bus driver

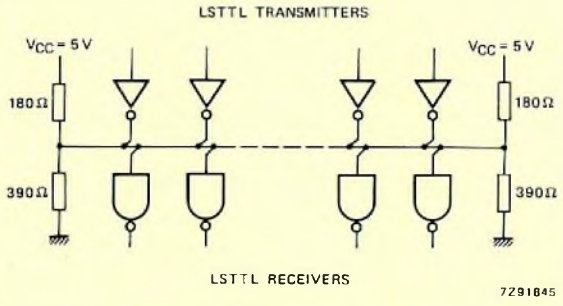
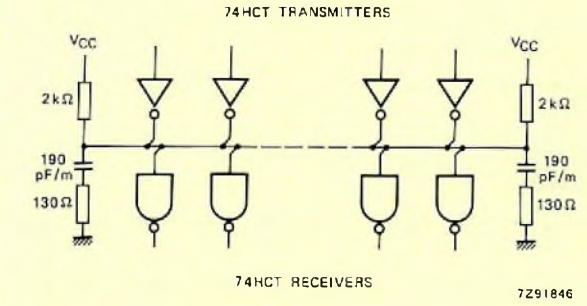
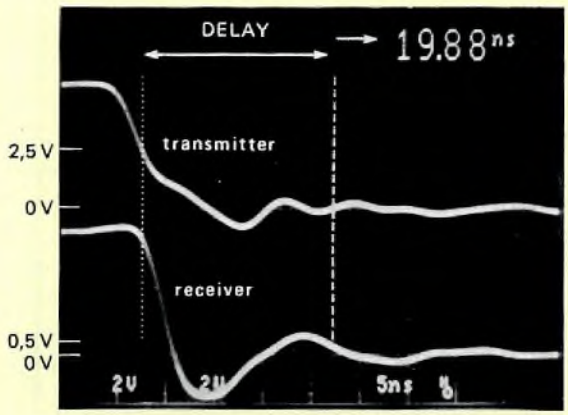


Fig.3 A d.c. termination for a stripline data bus with several 3-state LSTTL drivers





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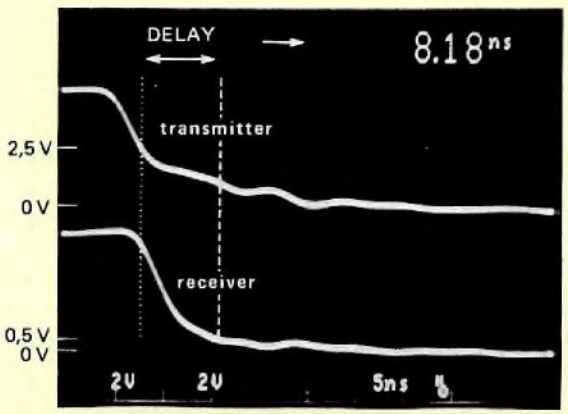

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Fig.4 An a.c. termination with pull-up for a stripline data bus with several 3-state 74HCT drivers

- total power dissipation of more than 250 mW per driver (including dissipation in the termination network) is contrary to the principle of replacing LSTTL ICs with 74HCT types to reduce power dissipation
- with a supply of 4,5 V, a V_{OL} of 0,5 V, $I_{OL\,max}$ = 9 mA, a terminating arrangement like the one shown in Fig.3 and the same ratio of resistor values (2:1), the lowest impedance line terminated at both ends that can be driven by a 74HCT bus driver is about 500 Ω (two 500 Ω terminations in parallel = 250 Ω effective load). A characteristic impedance of 500 Ω is impractical for a stripline.

However, resistive (d.c.) termination of an electrically long stripline multi-transmitter data bus is not essential because, as shown in the Appendix, the line can instead be terminated with its characteristic impedance (120 Ω) consisting of a series RC network (HCT bus drivers can deliver up to 70 mA during switching). A suitable low-power termination for a 3-state bus is shown in Fig.4. The maximum d.c. power dissipation of this arrangement when the bus in the LOW state is only 21 mW. The network shown provides a pull-up facility when the bus in the high-impedance state.

Driving twisted wire lines

Another type of line that must often be driven in logic systems consists of a pair of 0,38 mm (28 SWG) pvc-insulated wires twisted together. One of the wires is grounded and the characteristic impedance of the line is 110 Ω. The propagation delay along a twisted wire line is 6,2 ns/m. With rise and fall times of 4 ns, the line is considered to be electrically long if it exceeds 32 cm. Since it can only be end-driven, termination is only required at the receiving end of the line.

A twisted wire line driven by a 74HCT driver cannot be terminated with a 2:1 resistive potential divider with an effective parallel resistance of 110 Ω without exceeding the minimum guaranteed sink and source currents. By changing the potential divider ratio to 3:2, however, a 140 Ω termination can be made as shown in Fig.5. The total d.c. power dissipation (driver output plus termination network) in the LOW state is 42 mW.

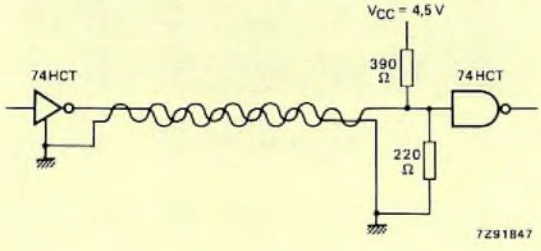
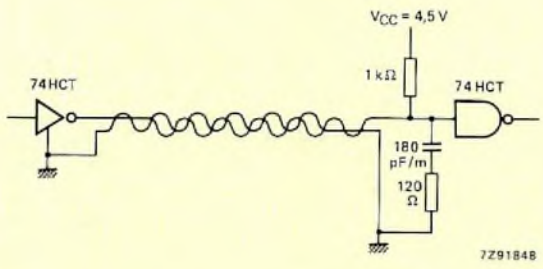
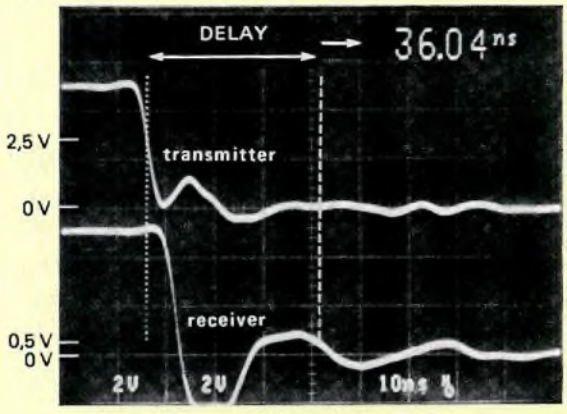


Fig.5 A d.c. termination for a twisted-pair line between 74HCT ICs.





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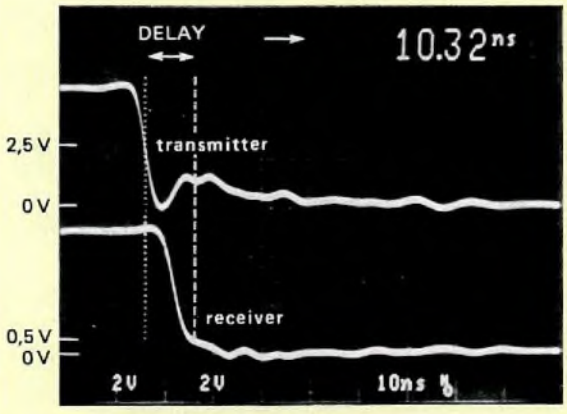

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Fig.6 A low-power a.c. termination for a twisted-pair line between 74HCT ICs.

A low-power 110 Ω a.c. termination suitable for the receiving end of a twisted wire line which requires pull-up/pull-down is shown in Fig.6. The capacitor has a low impedance to reflections and its value is calculated from the information in the Appendix. The total d.c. power dissipation of this arrangement in the LOW state is 17 mW. If a pull-up/pull-down facility is not required (2-state line), the 1 kΩ resistor can be omitted and the value of the remaining resistor reduced to 100 Ω. The d.c. power dissipation will then be reduced to zero.

Driving coaxial cables

Another type of data link is coaxial cable. There are various types of coaxial and triaxial cable available, but the most commonly used is RG-59B/U which has a characteristic impedance of 75 Ω and a propagation speed of 5 ns/m. With rise and fall times of 4 ns, the cable is considered to be electrically long if it exceeds 40 cm. One of the most common terminations used when driving a long coaxial cable with an LSTTL IC is shown in Fig.7. Since this termination provides a poor impedance match, requires a current sinking capability of about 20 mA and dissipates 100 mW in the LOW state, a 74HCT bus driver can't be used to drive it without exceeding its minimum guaranteed sink current. If pull-up/pull-down is required, it is therefore necessary to use an a.c. line termination with pull-up as shown in Fig.8. If pull-up/pull-down is not required (2-state line), the low-power a.c. termination shown in Fig.9 can be used. The coaxial cable should be terminated with its characteristic impedance at both ends for cable runs of more than 15 metres.

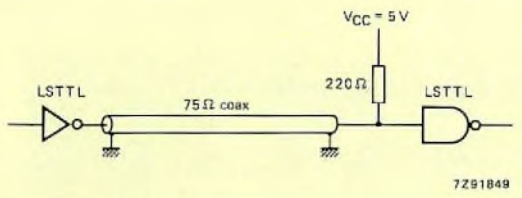


Fig.7 Termination of a 75 Ω coaxial cable interconnecting LSTTL ICs.

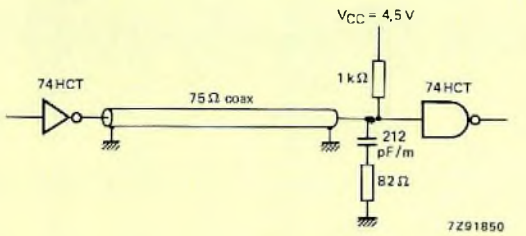
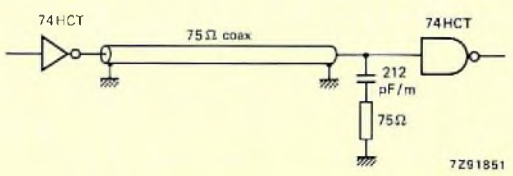
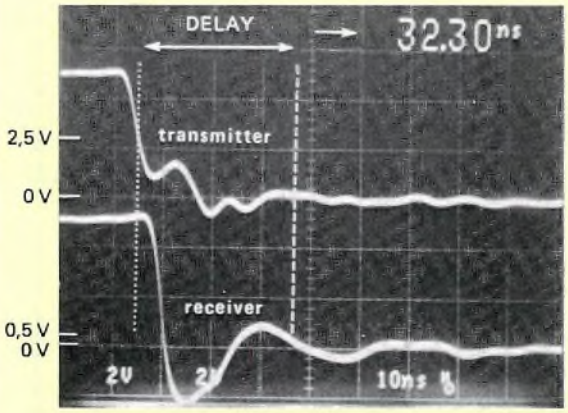


Fig.8 An a.c. termination with pull-up for a 75 Ω coaxial cable between 74HCT ICs.





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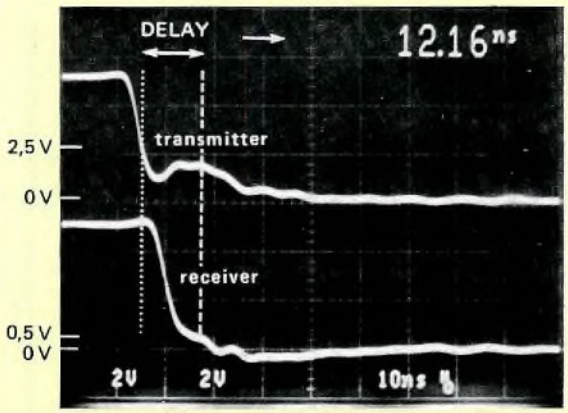

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Fig.9 A low-power a.c. termination for a 75 Ω coaxial cable.

Driving ribbon cable

The risk of crosstalk between the high impedance 74HCT inputs due to capacitive and inductive coupling is an additional factor restricting the length of unterminated ribbon cable that can be connected between 74HCT ICs. When the connections act as transmission lines the problem becomes even more critical. Since it is extremely difficult to calculate the combined effects of crosstalk and reflections in ribbon cable, the length restrictions are best determined empirically.

The length of an unterminated ribbon cable with a signal on each wire should not exceed 60 cm. If each alternate wire in the ribbon is grounded as shown in Fig.10, the unterminated length limit increases to 1,8 m.

A 74HCT IC can drive a longer ribbon cable if each signal wire is terminated with a pull-up resistor, pull-down resistor or one of the twisted-pair terminations previously described. With a 1 kΩ pull-up resistor per wire and no alternate ground wires, the maximum length that can be driven without crosstalk causing problems is 120 cm. The same arrangement but with alternate wires grounded as shown in Fig.11 increases the maximum permitted length to 2 m. When using a twisted-wire line a.c. termination with a Thevenin impedance of 170 Ω, but not using an alternate ground scheme (Fig.12), the maximum length that can be driven is 2 m. By adding the alternate grounded wires, the maximum length is extended to 5 m. The maximum length of ribbon cable that can be driven can be extended beyond 5 m by using 170 Ω terminations at both ends of the cable. The main point to bear in mind is that the maximum guaranteed sink current as specified for 74HCT ICs in the Table at the beginning of this article must never be exceeded.

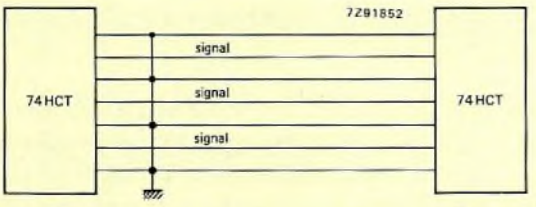


Fig.10 Unterminated ribbon cable with alternate ground wires

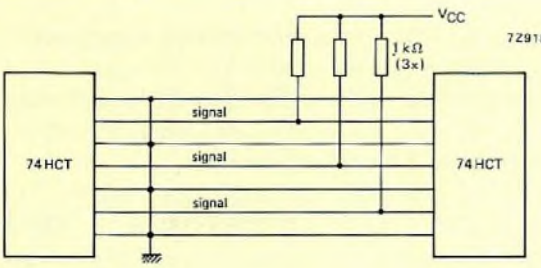
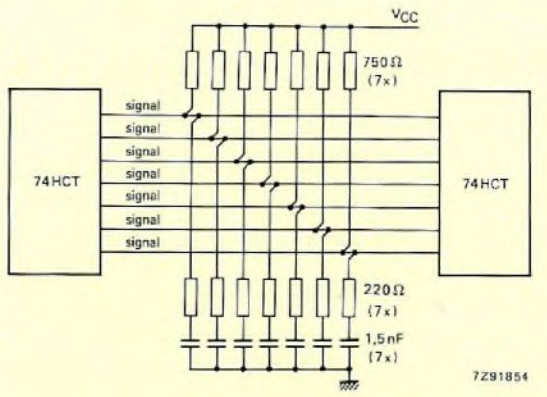
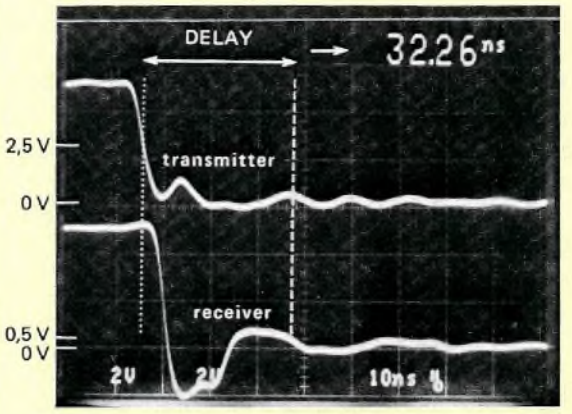


Fig.11 Ribbon cable with alternate ground wires and pull-up resistors





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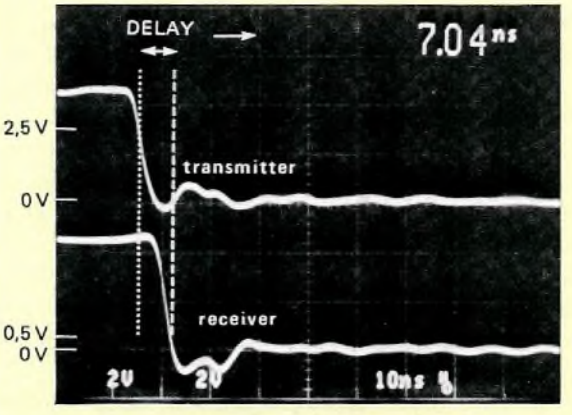

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Fig.12 Ribbon cable terminated with an impedance of 170 Ω.

APPENDIX

TRANSMISSION LINE REFLECTIONS AND TERMINATIONS

In digital systems, an interconnection is considered to be electrically long when the time taken for a transition to propagate down the line and return exceeds the rise or fall time of the transition. Such a line cannot be regarded as a short-circuit between the points it connects (with stray capacitance to ground), but must be regarded as a transmission line with characteristic impedance Z_O. A fast switching edge transmitted along an incorrectly terminated transmission line will be reflected by the line termination, possibly several times, before a steady state is reached. These reflections can degrade system performance by introducing delays and causing spurious switching.

If the input impedance of the line receiver and the output impedance of the line driver at $(V_{OH} - V_{OL})/2$ are both higher than the characteristic impedance of the line, a transition will reflect back and forth along the line several times, and its amplitude at the receiving end will progressively approach its final value in staircase fashion as shown in Fig.A1. The degree of mismatch between the driver output-impedance/receiver input-impedance and the characteristic impedance of the line determines the amplitude and number of staircase steps. This phenomenon limits the transmission speed because it introduces a delay before the amplitude of the received transition falls below the specified maximum V_{IL} for a H/L transition, or rises above the specified minimum V_{OH} of the receiver for a L/H transition.

Alternatively, if the input impedance of the line receiver is higher than that of the line, and the output impedance of the line driver at $(V_{OH} - V_{OL})/2$ is lower than that of the line, the amplitude of each reflection will alternately overshoot and undershoot its final value. The degree of mismatch between the driver output-impedance/receiver input-impedance and the characteristic impedance of the line determines the amplitude and duration of the ringing. As shown in Fig.A2, there may be a considerable delay before the amplitude of the received signal ceases to fall below $V_{IH\,min}$ or rise above $V_{IL\,max}$ of the receiver. Apart from introducing a delay and limiting the transmission speed, the ringing can also reduce the dynamic noise margin and cause erroneous switching.

For 74HCT outputs (standard and bus logic) with the minimum specified output current at 85 °C driving unterminated lines with a characteristic impedance of between 75 Ω and 150 Ω, the situation depicted in Fig.A1 occurs for L/H and H/L transitions. For 74HCT ICs with the maximum specified output current at 25 °C, the situation depicted in Fig.A2 occurs for L/H and H/L transitions.

A Bergeron diagram can be used to determine the amplitude of the reflections at both ends of the transmission line.

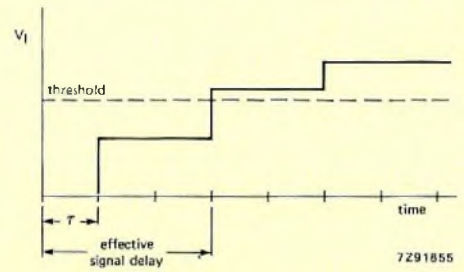


Fig.A1 A L/H transition at an unterminated receiver input when the output impedance of the driver is higher than that of the line

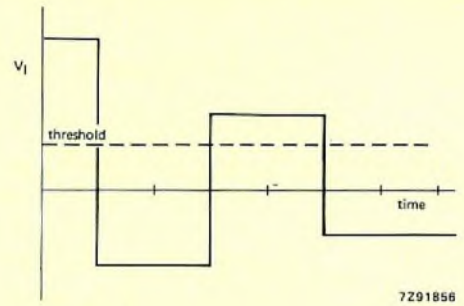


Fig.A2 A H/L transition at a receiver input when the output impedance of the driver is lower than that of the line

It shows the characteristic impedance of a transmission line as a series of load lines on the input and output characteristics of the line driver and receiver. The method of constructing it is to draw a load line for each input and output situation. Each load line originates from the previous quiescent point where the previous load line intersects the appropriate input/output characteristic. The slope of the load lines is equal to the characteristic impedance of the line but alternate load lines have opposite signs representing the change of current flow direction. The points where the load lines intersect the input/output characteristics indicate the amplitudes of the reflections.

A Bergeron diagram for analysing reflections during a H/L transition from $V_{CC} = 5$ V to 0 V for a 74HCT bus driver is illustrated in Fig.A3. To ensure a worst-case calculation, a H/L transition is selected because the LOW noise margin is always less than the HIGH one. For the same reason, the lowest practical transmission line impe-

dance (75 Ω coaxial cable) is assumed and the 74HCT bus driver output characteristics in Fig.A3 represent the maximum output drive current. The input characteristic is the maximum input resistance when V_{IN} is within the limits of the supply rails. The input resistance when V_{IN} exceeds the limits of the supply rails is the input voltage divided by the current flow through the input polysilicon resistors and conducting diodes of the HCMOS input protection network. The resistance shown is maximum.

In Fig.A3, the first load line originates from the maximum HIGH level (5 V = point 1), has a slope of $-1/75\ \Omega = -13{,}3$ mA/V, and is extended to intersect the NMOS output characteristic at point 2. The next load line has a slope of $+1/75\ \Omega$ and extends to intersect the input characteristic at point 3. This procedure continues, alternately intersecting the output and input characteristics until the 0 V/0 mA point is reached. Note that the effect of the input protection network on the input characteristic reduces the amplitude of the reflections from point 3 onwards. The voltage amplitudes at points 1 to 7 are plotted in Fig.A3(b) to show the effect of the ringing. It can be seen from Fig.A3(b) that the frequency of the ringing is $\frac{1}{4\tau}$ where τ is the propagation delay of the line. Propagation delays of various types of line and the associated ringing frequencies are given in Table A1.

It can be seen from Fig.A3 that, if the line is terminated with its characteristic impedance at the receiving end, the line from point 2 will intersect a much lower impedance input characteristic and point 4 will be zero volts. In the interests of low quiescent power dissipation, it is desirable to use an a.c. termination consisting of a series RC network between the receiver input and ground as explained elsewhere in this article. All that remains is to calculate the value of the components for the RC network.

If a criterion of the frequency dependent component of the termination impedance being 20% of the total is assumed,

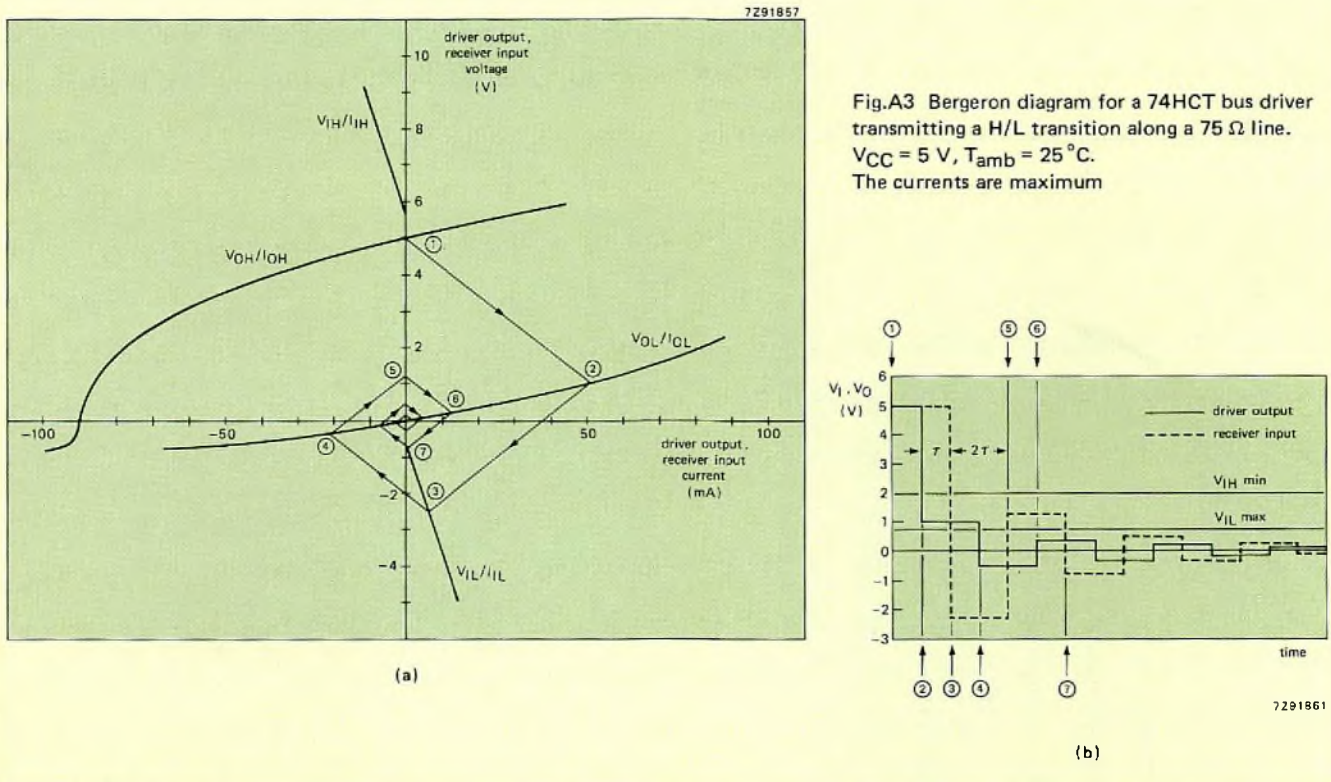


Fig.A3 Bergeron diagram for a 74HCT bus driver transmitting a H/L transition along a 75 Ω line. V_{CC} = 5 V, T_{amb} = 25 °C. The currents are maximum

TABLE A1
Characteristics of transmission lines

type of line	Z_O (Ω)	τ(per m)	f_{ring}
stripline on 1,6 mm glass-epoxy pcb: 0,6 mm track over groundplane	120	7,2 ns	34,7 MHz/line length (m)
two 0,38 mm (28 SWG) pvc insulated wires twisted together	100	6,2 ns	40,3 MHz/line length (m)
coaxial cable RG-59B/U	75	5 ns	50 MHz/line length (m)

the value of the resistor is $0{,}98\,Z_0$ and the value of the capacitor is:

$$C = \frac{1}{2\pi f_{ring} \times 0{,}2\,Z_0}.$$

Using the values of f_{ring} and Z_0 from Table A1 for a coaxial cable gives:

$$R = 75\,\Omega,\ C = 212\,\text{pF per metre.}$$

Similarly, for a twisted pair:

$$R = 110\,\Omega,\ C = 180\,\text{pF per metre.}$$

And for a stripline:

$$R = 120\,\Omega,\ C = 190\,\text{pF per metre.}$$

An interesting feature of the a.c. termination is that, if it is used on a 3-state bus, it will maintain the bus at the last existing logic state if the bus goes to the high-impedance state for a short period ($<100\,\mu s$).

To allow worst-case and best-case Bergeron diagrams to be constructed for all types of HCMOS logic elements, the maximum output current characteristics for 74HCT standard logic are shown in Fig.A4. The minimum output current characteristics for standard and bus driver 74HCT logic are shown in Fig.2.

For the sake of completeness, Fig.A5 is a Bergeron diagram for a L/H transition from a 74HCT bus driver with the minimum specified output current at 85 °C. This gives a practical illustration of the staircase effect shown in Fig.A1.

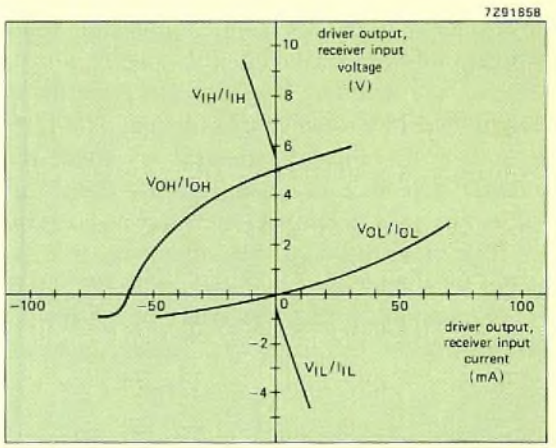
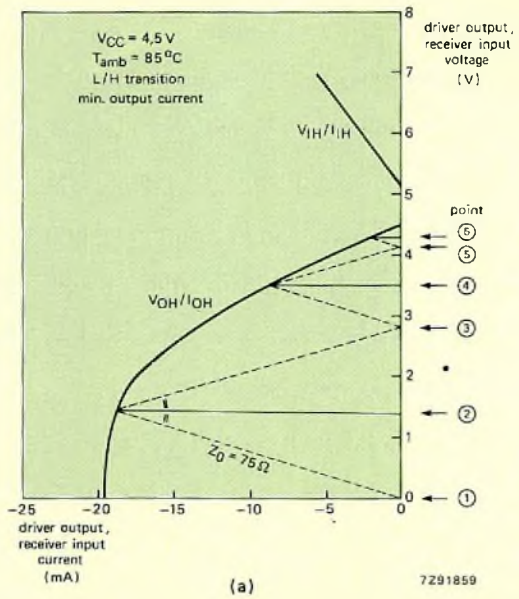


Fig.A4 Maximum V/I characteristics for standard 74HCT logic. V_{CC} = 5 V, T_{amb} = 25 °C



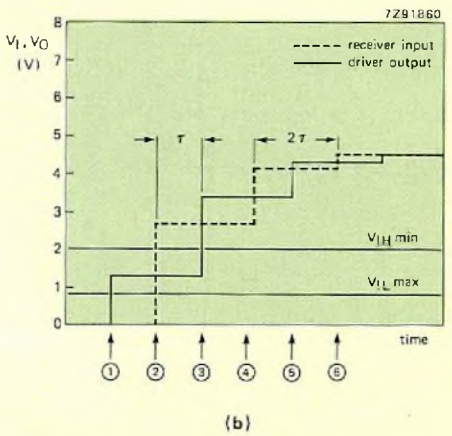


Fig.A5 Bergeron diagram for a 74HCT bus driver transmitting a L/H transition along a 75 Ω line. V_{CC} = 4,5 V, T_{amb} = 85 °C. The currents are minimum

Protection of HCMOS logic ICs in the automotive environment

JAN EXALTO and HENK KLOEN

With the exception of car radio components, the first electronic components to be used for automotive applications appeared about twenty years ago in voltage regulators. New functions which could be performed by electronic components appeared in the mid-seventies but, unfortunately, these had not been anticipated by electronic component manufacturers who, at that time, had insufficient knowledge of the characteristics of the automotive environment in which their components would have to operate. Today, the situation is much different and electronic components and assemblies are being used, or being developed, for a multitude of automotive functions such as engine management, displays, single-cable switch-units and all manner of accessories.

One thing that hasn't changed is the harsh environment in which electronic components for the automotive industry must work. However, much research has been done to fully characterize the automotive environment so that it is now possible to make real worst-case designs instead of following the rather haphazard approach of twenty years ago. Furthermore, more suitable electronic components such as high-speed CMOS (HCMOS) logic ICs of the 74HC/HCT/HCU family are now available for these applications. Special features that make HCMOS ICs attractive for automotive applications are:

- high noise immunity
- 5 V logic retains speed when battery is almost flat
- input current up to 20 mA d.c. permitted
- low power consumption
- output short-circuit proof
- very low d.c. coupling between adjacent inputs
- latch-up free
- operating temperature range –40 °C to +125 °C
- all types available in 74HCT versions with TTL switching levels
- all types available in DIL or space-saving SO (small outline) packages

This article first discusses the automotive environment, and then outlines logic system design practices for protecting the power supply inputs, and signal inputs/outputs of HCMOS logic ICs against it.

THE AUTOMOTIVE ENVIRONMENT

Extensive studies have been made by electronic component manufacturers and the automotive industry to characterize the climatic and electrical environment which exists in motor vehicles. The results of these studies have been published by the Society of Automotive Engineers (SAE) and the International Standardization Organization (ISO). This information is supplemented by numerous methods of testing electronic components published by most motor-vehicles manufacturers. However, these test methods have many similarities because they are all modelled on the results of the previously mentioned environmental studies. The data on electrical disturbances presented in this article are based on information published by the ISO.

Thermal conditions

From the point of view of temperature, the automotive environment is divided into two main areas: the passenger compartment and the engine compartment. In the passenger compartment of a vehicle in Europe, the temperature can vary from −40 °C on a cold winter morning in Scandinavia to 75 °C on a hot summer afternoon in Spain. In most places in the engine compartment, the temperature will only reach 125 °C (including automatic gearbox, engine block etc.), but care must be taken to avoid mounting electronic assemblies close to very hot items such as exhaust pipes.

The foregoing thermal conditions regularly lead to temperature cycling at a rate of 40 °C/minute and a need for an IC operating temperature range of −40 °C to +85 °C in the passenger compartment, and −40 °C to +125 °C in the engine compartment. The 74HC/HCT/HCU family of HCMOS ICs are specified for both of these temperature ranges and are therefore suitable for use in all automotive applications.

Vibration

In general, the vibration present in the engine compartment of a motor vehicle prohibits the use of ICs in sockets. Even in the passenger compartment, IC sockets should only be used for ICs that have to be interchangeable to suit various applications, for example, PROMs. Remember that all HCMOS ICs are also available in SO (small outline) packages which generate lower acceleration forces than ICs in DIL packages because of their significantly lower mass.

Contaminants

The engine compartment of a motor-vehicle is an especially dirty environment due to the presence of salt spray, oil, hydraulic fluid, petrol, dust, sulphuric acid, water and anti-freeze. Special care must therefore be taken when designing housings, connectors, coatings and wiring for electronic equipment to be located in an engine compartment. This subject is adequately covered in many other publications and will not be discussed further here.

Electrical disturbances

During normal running, the voltage available from a 12 V motor-vehicle electrical system will be between 11 V and 16 V. There are, however, some conditions during which the supply voltage will be subject to transient disturbances. The characteristics of many of these disturbances have been specified by the ISO. The ISO test pulses which simulate them should be connected to the system under test via the artificial battery supply network shown in Fig.1.

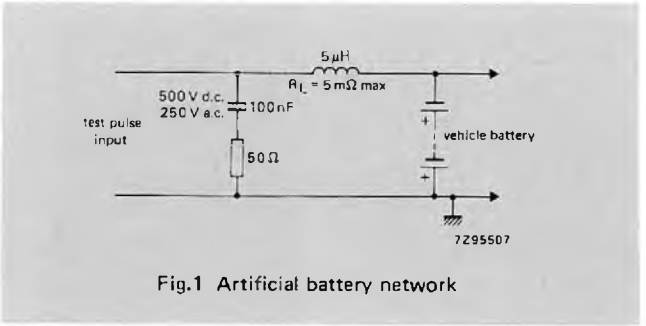


Fig.1 Artificial battery network

Static overvoltage. If a battery is flat after long-distance transport of a new vehicle, it will sometimes be disconnected and an external 24 V battery connected to the system. Electronic equipment must be able to withstand the extra voltage for five minutes if the equipment is connected directly to the battery terminals, or for fifteen seconds if it's connected to the battery via the ignition switch. In some cases, it may also be necessary for electronic equipment to function correctly during these periods.

Static reverse voltage. A battery may be inadvertently reverse connected to a motor-vehicle's electrical system during battery replacement or emergency starting. Electronic equipment must be able to withstand this reverse voltage for at least one minute (all other conditions worst-case). It is not necessary for electronic equipment to function correctly during this period.

Transients due to disconnection of parallel load. If an item of electronic equipment remains connected in parallel with a highly inductive component (e.g. starter motor, solenoid, air-conditioning system, fuel pump, relay or horn) after the latter is disconnected from the battery, the electronic equipment supply input will be subjected to a negative-going voltage transient of up to −100 V. The characteristics of this transient, as published by the ISO, are shown in Fig.2.

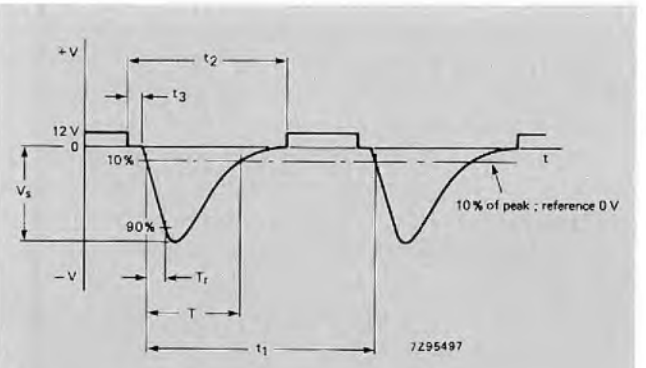


Fig.2 Pulse due to disconnection of an inductive load in parallel with electronic equipment (ISO test pulse 1). V_s = −100 V, R_i = 10 Ω, T = 2 ms, T_r is given in Table 1, t_1 = 0,5 to 5 s, t_2 = 0,2 s, t_3 < 100 μs (the shortest possible time between disconnection of the supply source and application of the pulse)

Transients due to disconnection of series load. If an item of electronic equipment is connected in series with a highly inductive component which is suddenly switched off, the electronic equipment supply input will be subjected to a positive-going voltage transient of up to 100 V. The ISO has published the characteristics of this transient as shown in Fig.3. Electronic equipment must be able to withstand several thousand repetitions of the transient which occur at a repetition rate of between twice per second and twelve times per minute.

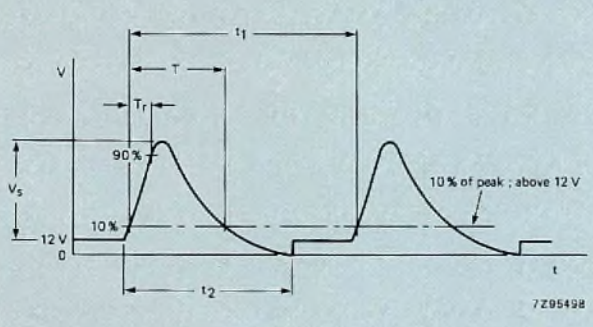


Fig.3 Pulse due to disconnection of an inductive load in series with electronic equipment (ISO test pulse 2). V_s = + 100 V, R_i = 10 Ω, T = 0,05 ms to 0,2 ms, T_r is given in Table 1, t_1 = 0,5 to 5 s, t_2 = 200 ms

Switching spikes. Switching spikes with peak levels up to 100 V can be superimposed on a motor-vehicle's 12 V supply due to the distributed capacitance and inductance of the wiring harness. The characteristics of negative-going and positive-going spikes as published by the ISO are given in Fig.4 and Fig.5 respectively.

TABLE 1
Rise time as a function of duration for ISO test pulses in Fig.2 to Fig.5

pulse duration (T)	rise time (T_r)
100 ns	6 ns
1 μs	20 ns
10 μs	70 ns
50 μs	150 ns
100 μs	200 ns
200 μs	300 ns
1 ms	800 ns
2 ms	1 μs

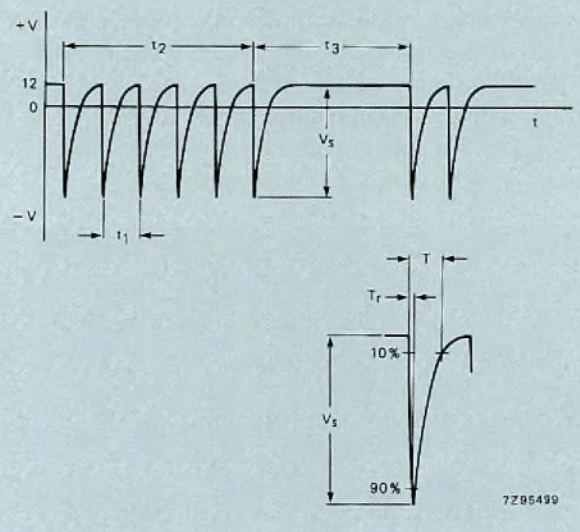


Fig.4 Negative-going switching spikes (ISO test pulse 3a). V_s = −150 V, R_i = 50 Ω, T = 0,1 μs, T_r is given in Table 1, t_1 = 100 μs, t_2 = 10 ms, t_3 = 90 ms

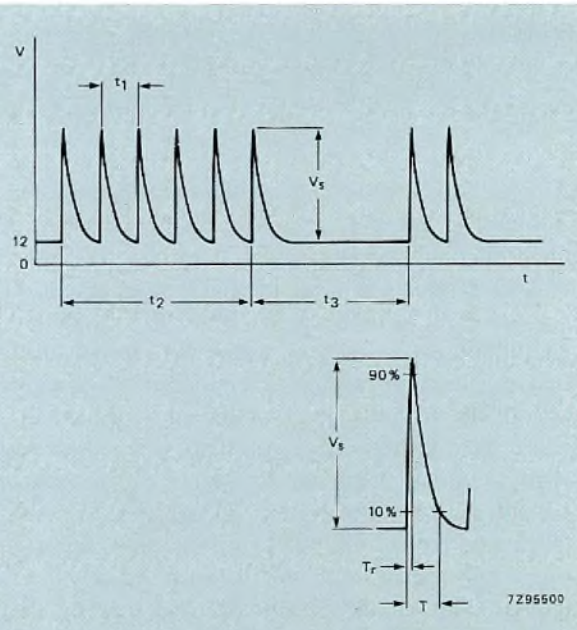


Fig.5 Positive-going switching spikes (ISO test pulse 3b). V_s = +150 V, R_i = 50 Ω, T = 0,1 μs, T_r is given in Table 1, t_1 = 100 μs, t_2 = 10 ms, t_3 = 90 ms

Low-voltage noise transients. Transient reductions of the nominal 12 V supply to around 5 V occur during engine starting due to the varying load imposed by the starter motor as it rotates the crankshaft. Since the viscosity of sump oil increases at lower temperatures, the amplitude of these transients increases with decreasing temperature. The ISO test waveform for this condition is given in Fig.6. The test should be repeated several times. All electronic components should remain undamaged by the test and any component associated with engine management must remain operational throughout the test.

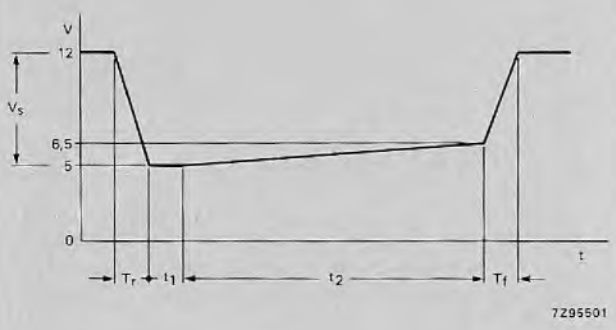


Fig.6 Starter motor engagement interference (ISO test pulse 4)
V_s = 7 V, R_i = 0,01 Ω, T = 130 ms, T_r = 10 ms, t_1 = 10 ms, t_2 = 100 ms, T_f = 10 ms

Load dump. A positive-going transient is superimposed on the nominal 12 V supply if a large load or flat battery is disconnected from the electrical system of a vehicle whilst the engine is running at high speed. The peak amplitude of the transient will be between 10 V and 120 V depending on the level of alternator field excitation at the instant the load or battery is disconnected, and its duration will be between 40 ms and 400 ms depending on the time-constant of the alternator field excitation circuit. This is the most severe transient to which electronic equipment can be subjected in the automotive environment. Although several vehicle manufacturers are currently working on central suppression of load dump transients it must be assumed, for the time being, that there is still a possibility that they will occur. The test pulse specified by the ISO for load dump transients is shown in Fig.7.

Transient due to ignition coil interruption. If the ignition coil is interrupted, a negative-going impulse with a peak amplitude of up to −300 V will occur on the electrical system supply line. The test pulse specified by the ISO for this condition is shown in Fig.8.

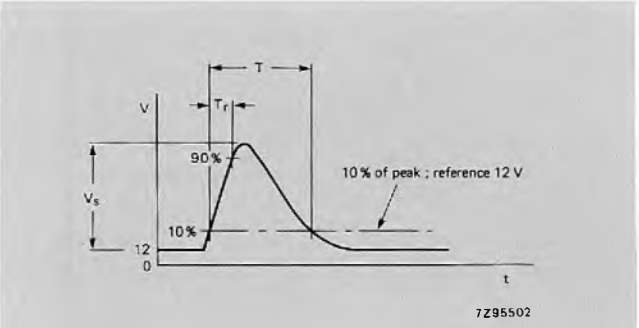


Fig.7 Pulse due to load dump (ISO test pulse 5).
V_s = 10 V to 120 V, R_i = 0,5 to 4 Ω, T = 40 to 400 ms, T_r = 5 to 10 ms

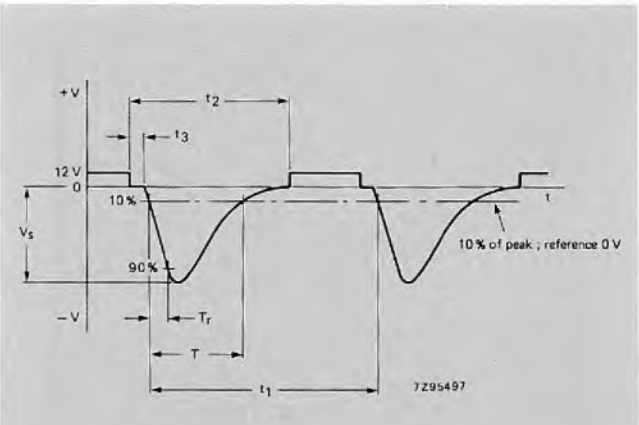


Fig.8 Pulse due to interruption of ignition coil circuit (ISO test pulse 6).
V_s = −300 V, R_i = 30 Ω, T = 300 μs, T_r = 60 μs, t_1 = 15 s, t_2 = 1 s, t_3 < 100 μs (the shortest possible time between disconnection of the supply source and application of the pulse)

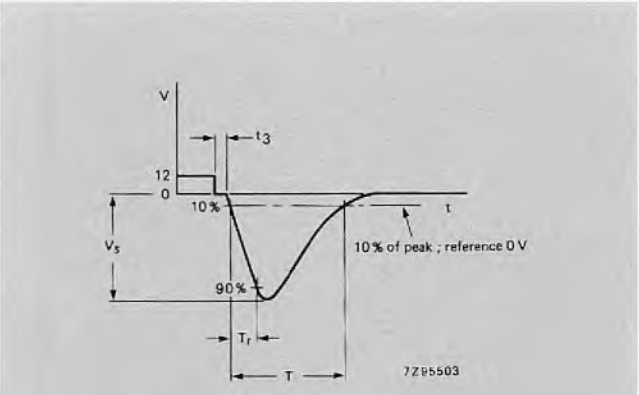


Fig.9 Pulse due to alternator field decay (ISO test pulse 7).
V_s = −80 V, R_i = 10 Ω, T = 100 ms, T_r = 0,5 to 10 ms, t_3 < 100 μs (the shortest possible time between disconnection of the supply source and application of the pulse)

Transient due to alternator field decay at ignition switch-off. When the ignition of a motor vehicle is switched off, the field windings of the alternator lose their energy and cause a negative-going transient with a peak amplitude of up to −80 V on the electrical system supply line. The test pulse specified by the ISO for this condition is shown in Fig.9.

Arc-over transient. An arc-over transient occurs if a sparking plug lead or high-tension lead from the ignition coil accidentally falls close to an electronic assembly, or if a spark is intentionally drawn from the h.t. distribution system of a motor-vehicle during servicing. There is no ISO test pulse for this condition but electronic assemblies must be able to withstand h.t. sparks to the case and to all supply and ground connections (not to signal inputs or outputs).

Electrostatic discharge. The terminals of an electronic unit can be subjected to electrostatic discharges during vehicle assembly or during repair or replacement of the unit. Any electronic equipment with driver-operated controls may also be subjected to repeated electrostatic discharge via the driver's body throughout the life of the vehicle. A method commonly used to simulate these electrostatic discharges is to charge a 100 pF capacitor to ±10 kV and then discharge it, via a resistor (560 Ω specified by ISO but the industry standard is 1,5 kΩ) and the pin(s) or lead(s) of the electronic component or assembly under test.

PROTECTING ELECTRONIC SYSTEMS FROM THE AUTOMOTIVE ENVIRONMENT

The power supply line, housing, signal inputs and signal outputs of HCMOS electronic systems for automotive applications must all be protected from the harsh operating environment encountered in all types of motor-vehicle. Although it is not possible to devise a universally-applicable protection scheme, the remainder of this article will be devoted to recommendations for protecting electronic systems which contain high-speed logic ICs of the 74HC/HCT/HCU family.

Type of housing

Because of the risk of arc-over from the h.t. leads, electronic equipment in the engine compartment should be in a metal case connected to the bodywork or chassis of the vehicle. Electronic equipment in the passenger compartment is not exposed to this hazard and can therefore be housed in a case made from any material.

HCMOS IC supply line protection

Electronic equipment supply lines in vehicles must be protected against all the previously discussed electrical disturbances. In addition, they must be able to continue to supply items such as engine management systems and trip computers with sufficient energy to allow them to operate normally during the low-voltage noise transients that occur during operation of the starter motor.

The previously discussed ISO requirements are so diverse that the only method of completely meeting them for CMOS logic ICs would be to incorporate on-chip integrated zenering; indeed, this method is commonly used for custom ICs. However, the high power handling requirements would lead to the use of too large an area of silicon to justify the use of this method for standard ranges of logic ICs. Furthermore, many of today's applications use multiple IC technologies in which a multitude of unforeseen interactions can occur. All these factors indicate that the best solution to the problem of operation of electronic systems in the harsh automotive environment is to have a central stepped-down (5 V) stabilized power supply which also incorporates decoupling and noise filtering. However, since vehicle manufacturers have not yet universally accepted this philosophy, additional precautions must be taken to protect the supply units of electronic systems containing HCMOS ICs.

For low current applications (up to 20 mA), the supply line protection circuit given in Fig.10 can be used. The component values which allow continued operation during 10 seconds of starter motor operation are given in Table 2.

If continued operation during engine starting is not required, D_1 can be omitted (the zener diode also absorbs negative-going transients) and the value of C_1 can be decreased to 22 μF.

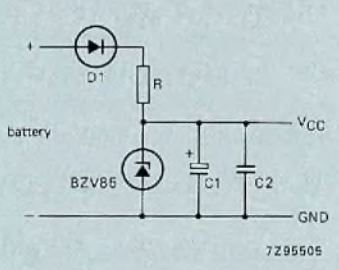


Fig.10 Protection for a low current power supply

TABLE 2
Component values for the circuit of Fig.10

supply current	R	C1
5 mA	560 Ω	60 mF
10 mA	330 Ω	80 mF
20 mA	220 Ω	220 mF

If it's necessary to supply more than 20 mA, the use of a zener diode is not recommended because its power dissipation would be too high. It's better to use the arrangement shown in Fig.11 which incorporates one of the voltage regulators specially designed for automotive applications. These regulators have a very low forward voltage drop (0,2 V at 150 mA and 0,4 V at 400 mA) combined with adequate protection against all the electrical disturbances encountered in a motor-vehicle. The low forward voltage drop of the regulator ensures that HCMOS logic ICs will remain operational during starter motor operation without the need to use the extremely high values of electrolytic capacitor (C_1) specified in Table 2 for the circuit in Fig.10.

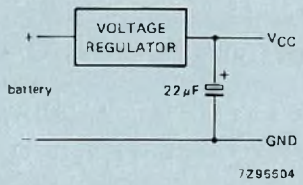


Fig.11 Protection for a higher current power supply

HCMOS IC input protection

Having taken precautions to protect the supply line, it may seem that the ICs are now fully protected against the automotive environment, but there are still two important points that need attention. Firstly, the 2-rail power supply system puts the burden of sequencing on the electronic equipment designer. Secondly, the input device (sensor, actuator) is still in a harsh environment. Taking a simple door contact as an example, the following requirements must be met:

- the contact must pass at least 20 mA to ensure self-cleaning
- since the signal lines are still subject to 150 V transients, additional resistance must be added in series with HCMOS inputs to reduce forward current through the input protection network to a safe level. The graph in Fig.12 shows safe levels of input current as a function of pulse duration
- radio-frequency interference from within the vehicle (e.g. ignition) or from external sources such as strong CB transmissions can easily swamp input signals from an input sensor. It is good practice to bypass r.f.i. to ground with a capacitor immediately after the input connector to the electronic equipment
- the point at which a simple mechanical contact makes or breaks is often poorly defined. Debouncing is therefore essential and the resulting signal should also be conditioned by a Schmitt trigger.

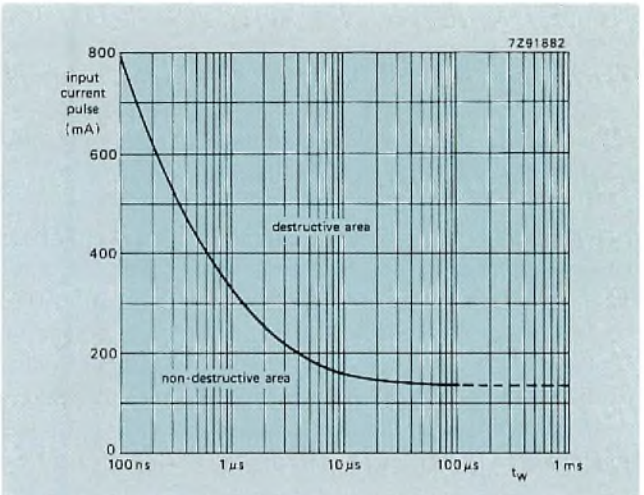


Fig.12 HCMOS input current as a function of pulse duration

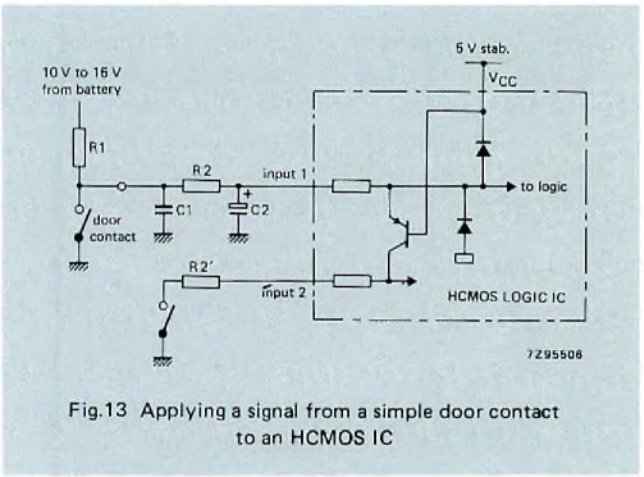


Fig.13 Applying a signal from a simple door contact to an HCMOS IC

The circuitry shown in Fig.13 conforms to the foregoing requirements. Resistor R_1 ensures that at least 20 mA flows through the contact. Capacitor C_1 should have a value of 22 nF to 100 nF to decouple r.f.i. immediately after the electronic equipment connector.

In most cases, the input signals from several sensors are received by a single CMOS IC. There is then a possibility of interaction between adjacent inputs via the parasitic bipolar transistor shown in Fig.13. Current injected into the substrate at one input is partially diverted to an adjacent input where it manifests itself as a 'leakage' current. This phenomenon is described in more detail under the heading 'coupling of adjacent inputs' in the User Guide section of the Data Handbook or Designer's Guide. If the contact at the adjacent input is closed, the 'leakage' current causes a voltage to be developed across R_2, which may exceed V_{ILmax}. HCMOS ICs have two guaranteed parameters which prevent this from happening:

- the h_{FE} of the parasitic bipolar transistor is 0,05 max.
- the worst-case LOW input level is 30%V_{CC} compared with 20%V_{CC} for standard CMOS logic.

In a 5 V HCMOS-based electronic system in a vehicle, the maximum allowable input current to prevent degradation of a LOW level at an adjacent input is:

$$\frac{V_{IL\,max}}{h_{FE}\,R_2'} = \frac{0{,}3 \times 5}{0{,}05 \times R_2'} = \frac{30}{R_2'}. \qquad (1)$$

The current into the input can also be described as:

$$\frac{V_{bat} - V_{CC}}{R_1 + R_2} = \frac{16 - 5}{R_1 + R_2} = \frac{11}{560 + R_2}. \qquad (2)$$

Since equations (1) and (2) are equal, and assuming $R_2 = R_2'$:

$$\frac{30}{R_2} = \frac{11}{560 + R_2}$$

which expressed in terms of R_2 gives:

$$R_2 = -\frac{16800}{19} = -884\,\Omega.$$

Since the resulting value of R_2 is negative, the calculation proves that interaction between inputs which causes a problem with conventional 4000 series CMOS logic is no longer a problem with HCMOS logic. The value of R_2 can therefore be chosen solely for limiting the input current to the maximum HCMOS rating. For positive input current into HCMOS inputs, this is 20 mA for one input or 50 mA total for all inputs of a package. For negative current, it is 14 mA for one input, 9 mA for two inputs, 6 mA for three inputs, 5 mA for four inputs, 4 mA for five inputs and 3 mA per input for more than five inputs. Assuming a worst-case pulse amplitude of 150 V and a maximum input current of 10 mA, the value of R_2 would be 15 kΩ. However, a designer might elect to increase this value to obtain the debouncing time-constant in conjunction with C_2 (high value resistors are cheaper than high value capacitors!). A time-constant of at least 200 ms should be used for simple contacts which are often manufactured to achieve a compromise between mechanical rigidity and price.

HCMOS IC output protection

According to the HCMOS family specification, it's not permissible to short-circuit the output of HCMOS ICs. Nevertheless, this sometimes happens. For example, a breakdown mechanic could inadvertently short an injection-coil signal-line to the bodywork, or an engineer servicing an electronic module could short an output to GND with a probe (printed-circuit boards are very densely packed nowadays). Our development engineers have anticipated this and designed the aluminium tracks to HCMOS outputs to be able to carry short-circuit current. Laboratory experiments have confirmed that HCMOS ICs are indeed short-circuit proof.

A potential hazard for all CMOS ICs is the possibility of latch-up being initiated by excess input/output current or supply overvoltage. This is a real possibility in a motor-vehicle where the ICs are often supplied by the unfiltered voltage from the battery which is usually at least a metre away. Also, the nanosecond rise and fall times of IC signals can be reflected by actuator inputs and, due to voltage-doubling at the end of the cable, travel back and cause overshoots or undershoots at IC outputs. If an IC is driving a power npn transistor, the base pin of which becomes shorted to the collector for some reason, 12 V will be applied directly to the IC output. A resistor must therefore be connected in series with the IC output. Its value must be chosen not only to allow sufficient base drive for the power transistor, but also to limit the output current of the IC to a level that doesn't cause latch-up, even during fault conditions. The latch-up phenomenon has been fully discussed in the article "Standardizing latch-up immunity tests" which explains why, unlike many other CMOS ICs, HCMOS ICs are absolutely latch-up free.

SUITABILITY OF HCMOS ICs FOR MIXED TECHNOLOGY SYSTEMS

The automotive electronics industry selects its components to achieve an optimum balance between price and performance. For example:

- NMOS microprocessors which have LSTTL input/output compatibility are still widely used. All HCMOS ICs are available in 74HCT versions which are TTL-compatible
- many bipolar P(ROMs) which were originally designed in TTL technology are still used for look-up tables etc. 74HCT input levels are compatible with the 0,4 V/2,4 V output swings of these devices
- analog comparators are in widespread use. The output levels from these are the saturation voltages of bipolar transistors (0,4 V or V_{CC} – 0,4 V). 74HC ICs are ideal for this input voltage swing.

AUTOMATIC ASSEMBLY OF AUTOMOTIVE ELECTRONICS

To aid their drive toward more automated production lines and further miniaturization, manufacturers of electronic equipment for vehicles will appreciate the fact that HCMOS ICs are not only available in DIL plastic packages. All types are also available in SO (small outline) packages; ideal for automated surface mounting.

Modifying LSTTL test programs to test HCMOS logic ICs

HENK KLOEN

For many years, LSTTL logic has been the established technology for interconnecting more complex VLSI circuits such as ALU, RAM and ROM. Consequently, circuit designers are familiar with it. However, the 74HC/HCT/HCU high-speed CMOS (HCMOS) family is establishing itself in the market as the natural successor to LSTTL in the role of interconnecting logic. Because of its low power dissipation and high speed, HCMOS is an alternative to LSTTL that drastically reduces power consumption without sacrificing system speed.

Furthermore, the LSTTL pin- and function-compatible 74HCT versions allow designers to replace LSTTL ICs in existing circuits. Interfacing with other logic families presents few problems as HCMOS is perhaps the most interface-flexible logic family available.

But the switch from LSTTL to HCMOS also makes it necessary for test personnel to change from testing LSTTL logic to testing HCMOS logic. This article outlines the basic criteria for converting test programs, takes an in-depth look at modifying the popular Teradyne J283 system for testing HCMOS, and briefly examines the possibilities of using other test systems.

WHY CONVERT?

If conversion of test programs from LSTTL to HCMOS involved replacing all test hardware and software, the high investment required could deter many potential users. But with the major test systems in use, replacement is not necessary. Converting test hardware and software involves minimal investment, of both capital and time.

The following test systems are in common use:

By manufacturers

- Teradyne J283 (particularly versions with both d.c. and functional test capabilities).
- Teradyne J325HV (used for CMOS testing, frequently by manufacturers who have never produced LSTTL).
- Manufacturers' custom-designed systems (Texas Instruments' LSTTL testers, and our CMOS systems, for example).
- MCT2000 tester (d.c. and a.c. parameters).

By users

- Gen Rad GR1732.
- Hewlett Packard HP5046.

(both widely used for incoming inspection).

The following characterization and qualification systems are used by both manufacturers and users:

- Sentry VII, Fairchild Series 20, and the GR16. These all have the flexibility needed for full functional/d.c. + a.c. evaluation. Auto-calibration routines improve "absolute accuracy" tests.

Conversion cost

As an introduction to converting test programs, conversion for the 74HC00 (quad 2-input NAND gate) will be sufficient to gain familiarity with the techniques involved, but it is only after a test conversion for, say an octal circuit, that a reliable estimate of the time required for converting all test programs can be made. The 8 buffer-outputs switching at one time will also reveal the a.c. response of the test-fixture and handler-interface. After establishing to what

degree the test programs need to be altered, and the manpower available, a consistent and scheduled conversion strategy may considerably reduce the time needed for each circuit.

Assuming that a high-level programming language is to be used, the conversion, compiling and hardware debugging should take no more than two to three man-hours per IC. Depending on how comprehensive your master program is, conditional compiling can also produce high and low temperature test programs at the same time.

COMPARING LSTTL AND HCMOS

Most modifications to the test programs result from the following fundamental differences between LSTTL and HCMOS:

- LSTTL is current-controlled whereas HCMOS is voltage-controlled.
- Static HCMOS gates have built-in redundancy. Either the p-channel pull-up transistor or the n-channel pull-down transistor is enough to perform the logic function. Test vectors applied in LSTTL testing may therefore be inadequate to weed-out all open-circuit failures in HCMOS.

Open-circuit testing

As LSTTL ICs are current-controlled, truth-table testing will detect all short- and open-circuit faults, because internally charged nodes have insufficient residual charge to latch the preceding test vector. However, HCMOS ICs are voltage-controlled, so stored charge on internal nodes can be sufficient to latch the preceding state, thus the test programs could overlook open-source or open-drain connections to parallel p-channel (NAND) or n-channel (NOR) transistors.

To illustrate this, we will examine a basic NAND gate as shown in Fig.1. With inputs A and B both LOW, P_1 and P_2 conduct and output Q is HIGH. If input B is made HIGH, P_2 ceases to conduct but output Q remains HIGH as P_1 is still conducting. If, however, there was an open-circuit in the drain of P_1, output Q could still appear to be HIGH due to the stored charge on this circuit node.

It is therefore necessary to make output Q LOW (by making both inputs A and B HIGH) between these two test stages to guarantee that it is the action of P_1 that produces the HIGH output.

For this reason, truth-table testing must be extended. For the two-input NAND and NOR gates they become:

NAND GATE			NOR GATE		
inputs		output	inputs		output
A	B	Q	A	B	Q
0	0	1	0	0	1
[1	1	0]	0	1	0
0	1	1	[0	0	1]
[1	1	0]	1	0	0
1	0	1	[0	0	1]
1	1	0	1	1	0

[ ] indicates an additional line in the function table required for testing open-circuit drain or source connections.

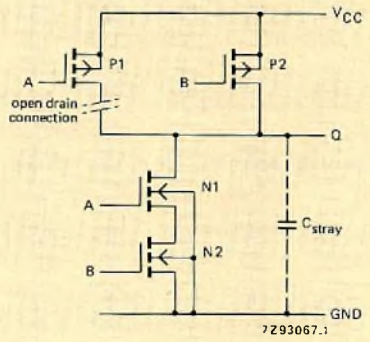


Fig.1 A basic NAND gate

As HCMOS ICs are voltage-controlled (energy-less), a similar problem occurs when detecting open feedback connections in flip-flops. Once the flip-flop is in the desired state, parasitic capacitances stay sufficiently charged to keep the flip-flop in that static state for several minutes, despite a missing feedback connection (to make it a static device). This situation is avoided by following this sequence:

1. At V_{CC} = 2 V, preset the IC.
2. Return logic inputs to LOW, leaving the output comparators of the tester connected.
3. Increase V_{CC} to 6 V.
4. If a flip-flop was non-static (due to open-circuit feedback), the outputs will now have flipped back to the opposite states; internal capacitances charged to 2 V (HIGH when V_{CC} = 2 V), will now be seen as LOW levels.
5. Repeat the sequence, but this time with opposite presets to the ICs.

Supply current

Although average system power consumption is lower for HCMOS than it is for LSTTL, testing of HCMOS imposes two new items:

Static mode test. HCMOS leakage current in any logic state should be low (in the region of nA). In LSTTL, a link has been found between faults in the IC and high I_{CC}. This is even more pronounced in HCMOS as excessive leakage current may load internal nodes, thus reducing the noise margins. Testing I_{CC} for every logic state combination takes a prohibitively long time (full A/D conversion), unless the test system has an analog comparison facility (for example, custom-built systems or as a special option on Teradyne J325HV). An acceptable solution is to test I_{CC} at enough logic states to ensure that all inputs and outputs have been both HIGH and LOW at least once.

Dynamic behaviour during static mode testing. In LSTTL, switching from one logic state to the next does not produce high di/dt (current switched from one internal node to another is barely detectable at the V_{CC} pin). In HCMOS however, heavy currents are drawn from V_{CC} during such transitions (several tens of mA because of the high di/dt from charging and discharging internal and external capacitances very rapidly). Therefore, an additional test for these transition currents is required. More stringent requirements are also placed on V_{CC} decoupling, and chip capacitors close to the V_{CC} pin are necessary. This, however, is contradictory to the static mode test where parasitic leakage must be minimized. So, if relays are to be used to isolate the capacitors for the static mode test, they should be low-inductance reed relays.

Clock requirements

As long as the input drivers of the test system are able to drive inputs faster than 500 ns, there is no problem. Input rise and fall-times, however, should be linear since a staircase shape can cause false triggering. Overshoots and ringing should be kept within 0,5 V of the supply rail voltage. All our 74HC/HCT ICs, however, are free from input and output induced latch-up so any overshoot will not lead to self destruction due to latch-up.

Input current

LSTTL has asymmetric characteristics at both inputs and outputs. In the HIGH state, LSTTL has a rather high impedance, drawing leakage current in the order of only tens of μA. But in the LOW state, there is active current of several mA.

On the other hand, HCMOS inputs impose only a capacitive load, drawing a few nA in both HIGH and LOW states (tested at 6 V and 0 V respectively). This can give problems in low-temperature testing because a leakage current of a few microamps (due to the formation of condensation) can be ignored in LSTTL but not in HCMOS, which should only draw a few nA. Flushing the loadboard and test socket with dry nitrogen overcomes this problem.

Output tests

Since in HCMOS, n- and p-channel transistors are laid-out to make them electrically identical, normal output load voltage tests can be applied with the following provisions:

- Force the current and measure the voltage. Otherwise, typical output currents at specified V_{OL} and V_{OH} may sometimes exceed the rated output currents.
- The output voltage HIGH for HCMOS is much higher than that for LSTTL. To obtain more accurate readings, a differential measurement between V_{CC} and the output should be made.

LSTTL CHARACTERISTICS THAT NEED NOT BE CHECKED FOR HCMOS

Output short-circuit current (I_{OS})

I_{OS} is not specified for HCMOS. Originally, I_{OS} was measured to reassure the TTL user that the circuit would withstand accidental output short-circuit to GND, and then in propagation delay calculation, to define the ability of a circuit to charge the line capacitance. In HCMOS, however, there is no need to check I_{OS} because the purely capacitive loads allow extrapolation of a.c. parameters over the whole loading range.

DC input diode current (I_{IK})

As there are no Schottky-clamps on HCMOS inputs, it is unnecessary to check I_{IK}. ESD protection networks are integrated on-chip and inputs enter the circuit via a true (polysilicon) resistor. A test program should check only for diode-clamps (at a low current, about 100 μA, to eliminate the effect of the resistor from the measurement).

Note: specialized HCMOS ICs (HIGH-to-LOW logic converters) don't have an input protection diode connected to V_{CC}.

HCMOS CHARACTERISTICS THAT NEED SPECIAL TESTING

Noise margin

As HCMOS ICs are fast-switching and have high voltage gain between input and output, oscillation problems may be encountered (as with testing ALSTTL and FAST ICs). For ALSTTL and FAST, some manufacturers advise that noise margin tests should be omitted.

Since oscillation is an interaction between the IC characteristics and the hardware response of the test system, you should first try to improve the dynamic response of the supply to the device-under-test (DUT), by using groundplanes and high-frequency decoupling.

If the oscillation problem is still not solved, you can either skip the noise margin test or check the analog characteristic of the input stage. By measuring the I_{CC} current for 2 selected input voltages (see Fig.2), you can ensure that the noise margin specification is met, as follows:

1. Measure I_{CC} at specified V_{IL} (or V_{IH}).
2. Measure I_{CC} at specified V_{IL} + 50 mV (or V_{IH} – 50 mV); the current should be higher than during measurement 1.

Indirectly, you're sure to be on the correct side of the actual switching point of the input stage. The operation of subsequent stages, already at near full-swing (V_{CC} or GND) has already been checked by functional testing.

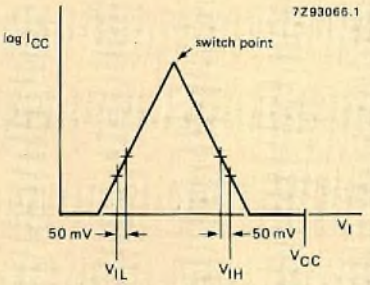


Fig.2 Measuring I_{CC} during noise margin test

V_{OL}/V_{OH} unloaded (20 μA load, 100 mV difference is allowed across the supply rails)

Having determined that the DUT is leakage-free for output HIGH and LOW, there is no need to perform unloaded output voltage tests, since the on-resistance of outputs is less than 100 Ω (0,4 V/4 mA min.). Even if all I_{CC} leakage were concentrated in one output stage, the total current drawn (160 μA for MSI + 20 μA external, for example) multiplied by R_{on} (<100 Ω) is 18 mV max., well within the 100 mV limit.

Resistance to latch-up

Good latch-up immunity can be obtained with a good lay-out (p^+-plugs closer to p-well than any n^+-diffusion) or by using epitaxial-wafers. These techniques have been combined to make HCMOS completely immune to latch-up.

Although bench testing (either d.c.-triggered or through-ramped V_{CC}-voltage tests) is likely to be more accurate for product characterization purposes, you can write an algorithm for your test system to compare the latch-up immunity of ICs from different manufacturers by following this procedure:

1. Supply the IC with 6 V. The power supply current clamp to be set to 200 mA.
2. Pulse (preferably 1 ms) the input or output under test with +10 mA (HIGH output) or –10 mA (LOW output).
3. Measure V_{CC}. If latch-up has occurred, the resulting hold-voltage will be much lower than 6 V.
4. Increase the pulse-current and go back to step 2.

For a comprehensive discussion on latch-up, see the article "Standardizing latch-up immunity tests".

AC characteristics

Experience in testing LSTTL, ALSTTL or FAST logic will have outlined the pitfalls which can be met when using test fixtures. Commercial load-boards and pin electronics are commonly laid-out as 50 Ω striplines, and while this is acceptable for ECL testing, and for simulating LSTTL resistive loads, with HCMOS it creates problems. Consider the following:

- HCMOS is specified with a 50 pF load. The lumped capacitance at the end of the stripline may not be seen by the IC output due to the substantial delay of the line compared with the transition time.
- Switching all 8 outputs of an octal IC simultaneously (each loaded with 50 pF), results in a massive load dump on the V_{CC} decoupling or groundplane, and ringing and overshoots are likely to occur. Switching outputs on at a time will relieve the problem.
- HCMOS reference levels are set at 50% of the transition. If reflection occurs in the system, the 50% point is right in the reflected area (see Fig.3). If you can't improve your test fixture, it might be more reliable to test at the 90% (t_{PHL}) or 10% (t_{PLH}) points. Correlated limits should be set to the specification value minus 50% of typical-specification transition times.
- True "absolute accuracy" characterization calls for dedicated test fixtures. The more flexibility you built-in, the more concessions you have to make on accuracy.

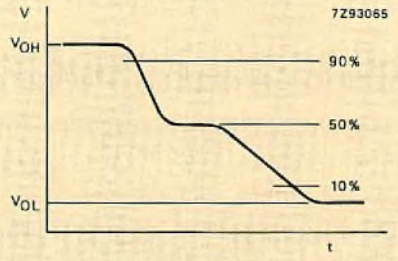


Fig.3 Output with reflection

TEST SYSTEM CONSIDERATIONS

Pin count (input only, output only, 3-state or multiplexed input/output)

For the HCMOS standard-range alone, a SSI/MSI tester may be adequate. More and more users, however, are changing to dedicated HCMOS ICs which integrate their system onto a single Gate- or Cell-Array chip. This secures copyright on the IC and gives a more reliable, simpler system. To match this trend, your test system should be able to handle configurations with more than 64 pins even if this means partitioning the load-board into dedicated input and output pins.

Pin electronic (load-board) considerations

As detailed later under "Future options", a logarithmic scale for each I_{CC} test-vector may be valuable. Having loads connected to every output will substantially reduce the test duration.

Clock speed

For specialized ICs, maximum clock frequency testing may be necessary. Although abnormalities within the IC may often be revealed by I_{CC}/pattern testing, it could be necessary to test for full clock-frequency response in certain cases. As an option, MCT2000 gives you the opportunity to test 200 MHz functional response.

Pattern generation capability

For enhanced fault grading, software tools should be used to adapt the test vectors to HCMOS. Furthermore, the functional pattern your fault-grader generates must be easily downloadable into your test system.

Parametric measurement capability

- current range: 1 pA to 100 mA.
- voltage range: 10 mV to 30 V.

PROGRAMMING CONSIDERATIONS

High-level languages are recommended for HCMOS testing

Because input and output configurations are the same for every HCMOS IC, a high-level language (giving you the framework for the family through conditional compiling) is recommended. Together with the utility-programs already available in the "Master Operating Program", efficient data reduction may help you to grade different IC manufacturers and optimize the "fitness for use" in your application.

Throughput – reducing the test time

Depending on the preferences and prejudices of your manufacturers, you can skip certain parameter tests. PPM data (assuming full exchange of test information between user and manufacturer, avoiding test duplication) based on an open manufacturer-user relationship is helpful to optimize complete testing.

MODIFYING TERADYNE J283 TEST PROGRAMS FOR HCMOS

Modifying an existing LSTTL test program for the Teradyne J283 system is relatively straightforward. Following the guidelines previously given, adaptation of the patterns and parametric tests is possible. The level of fault-grading attainable is comparable with that for LSTTL testing.

The parameter tests that must be modified for use with HCMOS ICs can be divided into the following two categories:

1. Those tests that must be modified to obtain a "PASS" for HCMOS circuits. For these tests, it is only necessary to modify the settings that cause problems. This results in a test that confirms the ability of the HCMOS ICs to perform the LSTTL function.
2. Those tests that must be modified to test the IC to the HCMOS specification if the user wishes to take advantage of the additional features of HCMOS.

Category 1 tests

Input current at $V_I = 7$ V. Due to the input protection network of HCMOS ICs shown in Fig.4(b), input current will flow if the input voltage exceeds V_{CC} by 0,5 V or more. To prevent a "FAIL", the input voltage must be reduced from 7 V to V_{CC}. To test the exact input leakage current, the setting must be modified according to the d.c. characteristics for 74HCT circuits given in Appendix 2.

Input clamp voltage. The protection network for each HCMOS IC input incorporates a series resistor that will cause the input clamp voltage with an input current of −18 mA to be much lower than the −1,5 V specified for LSTTL. Since the input clamp voltage is not specified for HCMOS circuits, this test could be omitted, or changed to have a conservative limit of −5 V. This assumes −3,6 V across a 200 Ω polysilicon input resistor plus −1,5 V across the input protection diode to GND.

Output short-circuit current HIGH. As shown in Appendix 1, LSTTL has an output short-circuit current (I_{OS}) of −20 mA to −100 mA. However, due to the symmetrical output structure of HCMOS ICs as shown in Fig.4(b), the LSTTL collector output resistor is not present. Since I_{OS} is not specified for HCMOS ICs, this test may be omitted.

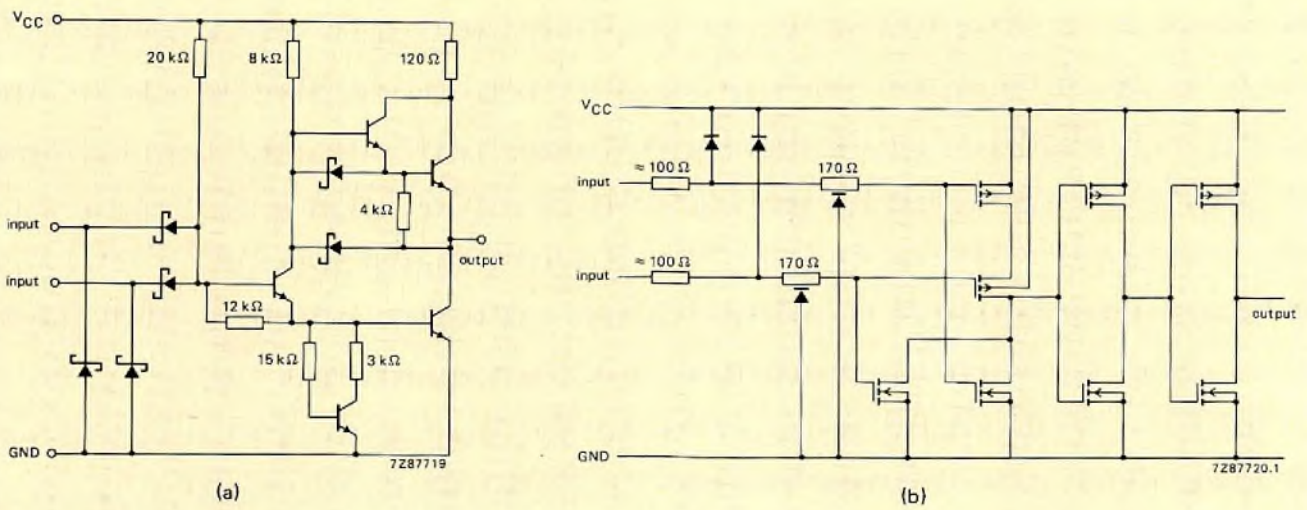


Fig.4 Comparison of LSTTL and HCMOS circuit structures.
(a) 2-input LSTTL NAND gate with totem-pole outputs (¼ 54/74LS00). For other structures, refer to published data;
(b) 2-input HCMOS NOR gate

Hysteresis (bus driver ICs). Many LSTTL bus driver ICs undergo a test for hysteresis using a 0,2 V minimum limit. HCMOS bus drivers don't have input hysteresis, so this test may be omitted, or the minimum hysteresis limit changed to 0 V.

Output voltage LOW at I_O = 12 mA (bus drivers types). Many LSTTL bus drivers have two specifications for V_{OL} test current that must be altered as shown below for HCMOS:

LSTTL		HCMOS	
V_{OL} max	I_{OL}	V_{OL} max	I_{OL}
0,4 V	12 mA	0,33 V	6 mA
0,5 V	24 mA	0,5 V	9 mA

These figures seem to indicate that the HCMOS LOW-level output current is less than that of LSTTL. The output t_{THL} of HCMOS, however, is similar to that of LSTTL. The real significance of the I_{OL} = 24 mA for LSTTL is the ability of its bus drivers to drive a d.c. terminated bus (see Fig.5(a)). However, this output current causes power dissipation of 250 mW per output (2 W per octal IC). For much lower power dissipation with an HCMOS IC, an a.c. termination as shown in Fig.5(b) is used.

Continuity. With some settings used for continuity testing, the input protection polysilicon resistor of HCMOS ICs could cause a "FAIL". This must be borne in mind when test engineers select their individual settings for this test. Therefore, it is important to keep input current to ±20 mA during continuity testing. With this current, the test voltage is ±5,5 V maximum.

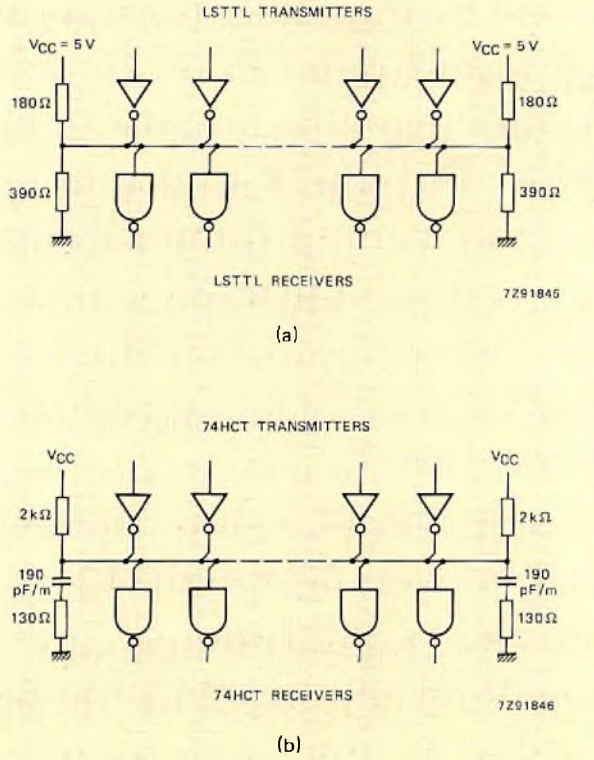


Fig.5 Termination of a 120 Ω stripline bus
(a) d.c. termination for LSTTL
(b) low-power a.c. termination for HCMOS

Category 2 tests

Quiescent supply current. Setting supply current I_{CC} for the output LOW condition for HCMOS ICs will not cause problems, but setting the output HIGH condition is more complex. In the Teradyne J283, there is a comparator connected to each of the outputs under test. These comparators cause an extra load current of about 7 μA per output, the precise current depending on the specific tester. The extra load currents are negligible compared with the I_{CC} of LSTTL ICs and can be ignored. When testing HCMOS circuits, however, they can be very significant in comparison with the total I_{CC} and must be taken into account. A solution to this problem is to connect the HIGH outputs to V_{CC} so that they are excluded from the I_{CC} measuring path. This can be done with the statement:

MTEST V_{CC} 1 A B C (A, B, C are HIGH outputs in this test).

Output voltage LOW. The lower output voltages of HCMOS can be tested without any complications (4 mA for standard outputs, 6 mA for bus driver outputs).

Output voltage HIGH. The higher output voltages of HCMOS can be tested without any complications.

High impedance (OFF-state) output current for types having three-state outputs with $V_O = V_{CC}$ or GND. The high-impedance (OFF-state) leakage current (I_{OZ}) for HCMOS ICs can be tested without any complications, but with much tighter limits, as follows:

	LSTTL	HCMOS
I_{OZ}	20 μA	5 μA

Input leakage current (all HCMOS types). Input leakage current LSTTL tests can be run for HCMOS, but with much tighter limits, as follows:

	LSTTL	HCMOS
I_{IL}	−400 or −800 μA	−1 μA
I_{IH}	+20 or +40 μA	+1 μA

Function testing. This test can remain relatively unchanged because HCMOS and LSTTL ICs with the same type numbers have identical truth-tables. However, the requirement discussed for detecting open-drain or open-source connections (see "Comparing LSTTL and HCMOS – Open-circuit testing") must be met, and truth-table function tests modified accordingly.

USING OTHER TEST SYSTEMS FOR HCMOS

With the Teradyne J325HV, program changes are straightforward. The VDIF feature can be fully exploited to test for V_{OL}/V_{OH} loaded (as well as unloaded; see also "Supply current – Static mode test").

Our MCT2000 was originally set-up to test propagation delays and transition times. Practical experience, however, has shown that it is suitable for a full data sheet check of d.c. parameters and function. As with the J283, output comparators cannot be fully isolated from the output-pins (solid-state switched, μA leakages are reported) and instead of I_{CC}, the leakage has to be measured in the GND line if one or more outputs are HIGH.

Another way of minimizing the leakage current drawn by the output comparators is to set them in parametric mode and program the forced current to 0 nA.

The auto-calibration library contains the leakage current value per pin-card, and programming the current to zero will compensate for the remaining leakage current down to tens of nA.

For incoming inspection testing using the GR1732 or HP5045, in addition to existing machine limitations (e.g. inability to test for low leakages), care should be taken to ensure that the load board or its pin electronics don't influence the a.c. performance of the device under test.

Improving tester hardware/software for HCMOS testing

Teradyne's TTL testers are less appropriate for testing long counters (e.g. 2^{14} for 74HC/HCT4020 and 74HC/HCT4060, or 2^{12} for 74HC/HCT4040). While compiling the symbolic language into machine code, at least two computer words (2 × 10 μs) will be sent out and therefore $2^{14} \times 20\,\mu s = 330$ ms are needed for one functional pass. If you wire your clock input to the "word-one" pin cards, you can bypass the compiler by directly programming the "W1" in machine code, and since "W2" stays the same, you can halve the time for a functional pass.

On the J325, there is also the "burst" option which allows you to send out a high-speed burst of clock pulses in one functional pattern. During the burst, it is impossible to check the IC response but the logic state can be verified after the burst. Another helpful option on the J325 is the "I_{CC}-test per functional pattern". The buffered analog output of either VTEST (current monitor in V_{CC}) or MTEST (device supply from the parametric measurement unit PMU) is now connected to a square channel-card and can be monitored during each test vector with the digital comparators already built-in.

Future options

A logarithmic scale (as available on our custom-built testers) has proved to be essential for I_{CC} testing. Within a batch to be tested, I_{CC} ranges from pA to μA, so scale-compression at the high end (μA range) is required.

System specifications should be extended "up to and including" the handler-connectors. This requires interface standardization but it means that manufacturers and users will be working to the same standard. Currently, only MCT can comply with this requirement (being able to supply both tester and handler).

APPENDIX 1 DC characteristics for the 74HCT circuits

Voltages are referenced to GND (ground = 0 V)

parameter	V_{CC} (V)	symbol	T_{amb} (°C)							unit	conditions	
			+25			−40 to +85		−40 to +125			V_I	others
			min.	typ.	max.	min.	max.	min.	max.			
HIGH level input voltage	4,5 to 5,5	V_{IH}	2,0	1,6	–	2,0	–	2,0	–	V		
LOW level input voltage	4,5 to 5,5	V_{IL}	–	1,2	0,8	–	0,8	–	0,8	V		
HIGH level output voltage all outputs	4,5	V_{OH}	4,4	4,5	–	4,4	–	4,4	–	V	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
HIGH level output voltage standard outputs	4,5	V_{OH}	3,98	4,32	–	3,84	–	3,7	–	V	V_{IH} or V_{IL}	$-I_O = 4,0$ mA
HIGH level output voltage bus driver outputs	4,5	V_{OH}	3,98	4,32	–	3,84	–	3,7	–	V	V_{IH} or V_{IL}	$-I_O = 6,0$ mA
LOW level output voltage all outputs	4,5	V_{OL}	–	0	0,1	–	0,1	–	0,1	V	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
LOW level output voltage standard outputs	4,5	V_{OL}	–	0,15	0,26	–	0,33	–	0,4	V	V_{IH} or V_{IL}	$I_O = 4,0$ mA
LOW level output voltage bus driver outputs	4,5	V_{OL}	–	0,16	0,26	–	0,33	–	0,4	V	V_{IH} or V_{IL}	$I_O = 6,0$ mA
Input leakage current	5,5	$\pm I_I$	–	–	0,1	–	1,0	–	1,0	μA	V_{CC} or GND	
3-state output OFF-state current	5,5	$\pm I_{OZ}$	–	–	0,5	–	5,0	–	10,0	μA	V_{IH} or V_{IL}	*
quiescent supply current												
SSI	5,5	I_{CC}	–	–	2,0	–	20,0	–	40,0	μA	V_{CC}	$I_O = 0$
flip-flops	5,5	I_{CC}	–	–	4,0	–	40,0	–	80,0	μA	or	$I_O = 0$
MSI	5,5	I_{CC}	–	–	8,0	–	80,0	–	160,0	μA	GND	$I_O = 0$

* $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$.

APPENDIX 2 DC characteristics for LSTTL circuits

These figures are for positive NAND gates and inverters with totem-pole outputs.
For the characteristics of other types, refer to published data for LSTTL circuits.

Voltage are referenced to GND (ground = 0 V)

			54LS			74LS				
parameter	V_{CC}	symbol	min.	typ.	max.	min.	typ.	max.	unit	conditions
operating temperature	*	T_{amb}	−55	–	+125	0	–	+70	°C	
HIGH level input voltage	*	V_{IH}	2	–	–	2	–	–	V	
LOW level input voltage	*	V_{IL}	–	–	0,7	–	–	0,8	V	
input clamp voltage	min.	V_{IK}	–	–	−1,5	–	–	−1,5	V	I_I = −18 mA
HIGH level output voltage	min.	V_{OH}	2,5	3,4	–	2,7	3,4	–	V	V_{IL} = max., I_{OH} = −400 µA
LOW level output voltage	min.	V_{OL}	–	–	–	–	0,25	0,4	V	V_{IH} = 2 V, I_{OL} = 4 mA
LOW level output voltage	min.	V_{OL}	–	0,25	0,4	–	0,35	0,5	V	V_{IH} = 2 V, I_{OL} = max.
input current at V_I = 7 V	max.	I_I	–	–	0,1	–	–	0,1	mA	
HIGH level input current	max.	I_{IH}	–	–	20	–	–	20	µA	V_{IH} = 2,7 V
LOW level input current	max.	I_{IL}	–	–	−0,4	–	–	−0,4	mA	V_{IL} = 0,4 V
short-circuit output current	max.	I_{OS}	−20	–	−100	−20	–	−100	mA	

For 54 LS, V_{CC} = 4,5 V to 5,5 V; for 74LS, V_{CC} = 4,75 V to 5,25 V.
All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
For short-circuit output current, only one output must be shorted, and for not more than one second.

* over V_{CC} range.

Battery backup of HCMOS logic ICs

ROB CROES

HCMOS logic ICs, in contrast to other logic families, can easily be provided with battery backup in the event of failure of the normal power supply. Two of the main reasons for this are their very low quiescent power consumption (quiescent currents typically in the low nA region compared with around 2 mA for LSTTL ICs), and their fast transition times, which minimize the time they spend in the linear region and hence the power they consume during switching. Added to these is the fact that HCMOS ICs operate quite happily at supply voltages significantly lower than their nominal supply voltage (say as low as 2 V compared with a minimum of 4,75 V for LSTTL), so except for a reduction in speed, a 2 V battery supply voltage is no hindrance to efficient operation.

For long periods of battery operation, however, there are a number of simple guidelines you should follow. None are essential, but if you stick to them you will at least minimize power consumption and assure maximum battery life.

MINIMIZING POWER CONSUMPTION IN BATTERY-BACKUP SYSTEMS

Don't use non-CMOS circuitry

Avoid using non-CMOS circuits in your design, this includes microprocessors and memories, otherwise you'll incur the inevitable penalty of higher power consumption. Remember, non-CMOS circuits draw quiescent supply currents that are often too high for battery operation. And although you can provide non-CMOS sections of your circuits with facilities for reduced-power (and hence slower) operation or for a completely idle power-down mode (for data retention only), in both these cases you'll find that operation of battery-backed up sections is likely to suffer severely in the event of a power failure. With all-CMOS circuitry, you won't have these problems at all.

Aim at low-frequency operation

Aim at low-frequency operation or switch logic ICs to the idle state if operation is not required. In CMOS systems, the dynamic power dissipation P_D is one of the greatest sources of power loss (static supply current drawn by CMOS circuits being almost negligible) and this is related to the input and output frequencies f_i and f_o by:

$$P_D = C_{PD}V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o) \qquad (1)$$

in which V_{CC} is the supply voltage, C_{PD} is the power-dissipation capacitance per device (obtainable from the data sheets) and C_L is the output load capacitance. P_D therefore varies directly with operating frequency.

An example should illustrate this. A typical MSI circuit with two outputs loaded with 50 pF will have a total load capacitance ($C_{PD} + 2C_L$) of 150 pF. Even with an operating frequency as low as 15 kHz, this will result in a dynamic supply current of 14 μA (with a 5 V supply), almost double the maximum quiescent supply current of 8 μA. And since operating frequencies may often be several orders of magnitude greater than this, you can appreciate how significant dynamic power dissipation can be, and how important it is to keep your operating frequency as low as possible.

The alternative is to add extra circuitry such as multiplexers to reduce overall power consumption. Multiplexers direct the information bit streams only to sections where they are needed, and allow all unused logic to be switched to the idle state in which it dissipates (negligible) leakage current only.

Use low-value capacitors to minimize charging losses

From the above discussion you can see that dynamic power dissipation is also proportional to load capacitance, so if capacitors are needed, make sure their values are as low as possible to minimize charging energy losses. High value load capacitance also increase transition times and hence the time the inputs spend in the linear region (see next item).

Make sure transitions are fast

The longer the voltage level of an input waveform is maintained between the undefined logic region of the MOS transistors (the linear region), the longer both the n-and p-channel input transistors remain conducting and the greater the power dissipation. Maximum current through the transistors (through-current) occurs at 50% of V_{CC} for 74HC ICs and at 28% of V_{CC} for 74HCT ICs, but there will also be significant current throughout the linear region, i.e. for V_I between $V_{IL\,max}$ and $V_{CC} - V_{IH\,min}$, which for a V_{CC} of 4,5 V means V_I between 1,35 V and 3,15 V. So you can see that input waveforms play a significant role in determining power loss.

Usually output rise/fall times and hence input rise/fall times of 20 ns at 5 V or 60 ns at 3 V are satisfactory to minimize power loss due to through-current.

When an output is heavily loaded capacitively and/or its signal is distributed to many inputs, the waveform can be squared-up (i.e. the capacitance reduced) by splitting the line at the output into several sections and driving these sections with independent drivers.

Finally, there's a common misconception that Schmitt triggers draw little through-current in the linear region. Whilst it's certainly true that the output transitions of a Schmitt trigger are fast, there's no guarantee that the input transitions will be. Indeed, since Schmitt triggers are generally used to square-up slow waveforms, there's a very good chance that input transitions will be slow and that heavy through currents will be drawn. The data sheets give you the through-currents drawn by Schmitt triggers.

You can get a rough idea of the through-current drawn by a 74HC IC for a given input voltage by looking at the unit load coefficient of its 74HCT counterpart. The unit load coefficient of a 74HCT IC is an indication of the size of the input transistors and hence of the current they consume during transitions. A type with a unit load coefficient of say 0,3, will draw only 0,3 times the through-current of a type with a unit load coefficient of one. So you can calculate the through-current drawn by a 74HCT IC for a given input voltage by multiplying its unit load coefficient by the current given in the through-current graph (Fig.1). And since nearly all 74HC and their 74HCT counterparts are produced by similar aluminium interconnect masks, this will give you an indication of which 74HC types draw the lowest through-current for the input voltage you want to operate at.

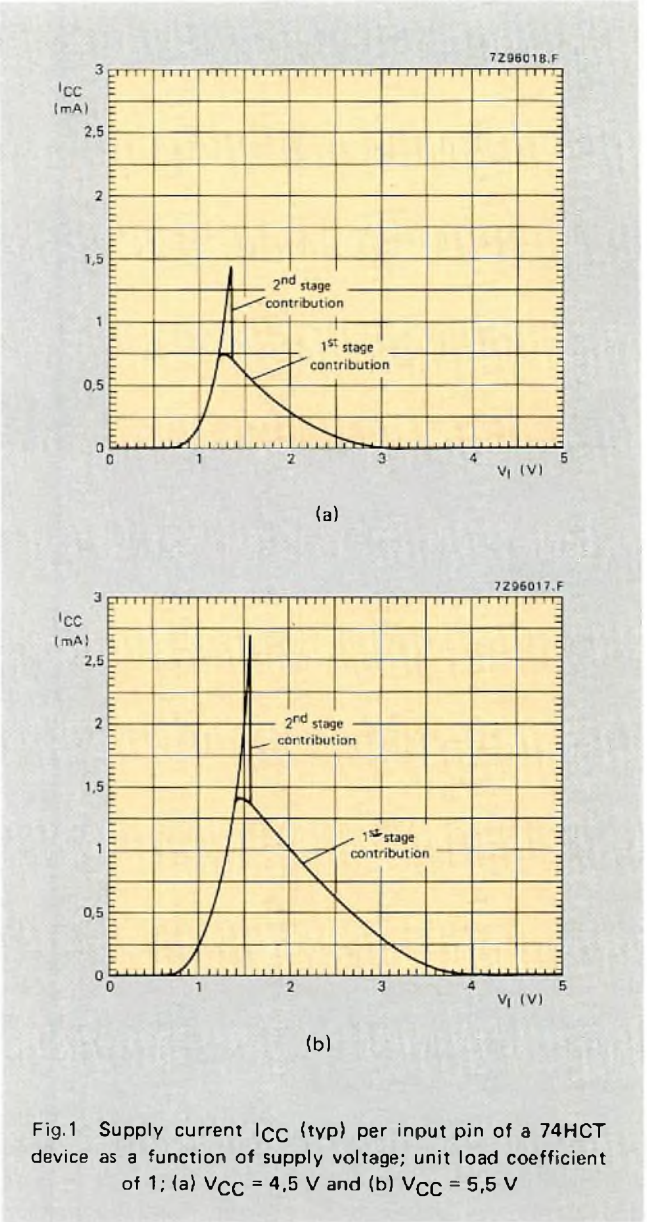


Fig.1 Supply current I_{CC} (typ) per input pin of a 74HCT device as a function of supply voltage; unit load coefficient of 1; (a) V_{CC} = 4,5 V and (b) V_{CC} = 5,5 V

Avoid the use of pull-up resistors

Don't use input or output pull-up resistors at the interface between the high-power (mains) fed section and the battery-fed section, since they can lead to sneak current paths when the normal power supply fails.

Although any pull-up or pull-down resistor disspates power, an input pull-up resistor that's returned to the V_{CC} rail of the battery-fed section will create a current sneak path when the high-power section fails (Fig.2). If resistors are necessary, use the highest values possible e.g. 1 MΩ.

If you look at Fig.2, you'll see that the sneak current path travels through the pull-up resistor R_{PU}, back along the signal path to the higher power logic, and forward-biases the input or output CMOS protection diodes (or the protection diodes in TTL), and supplies current to the high-power logic, severely draining the back-up battery.

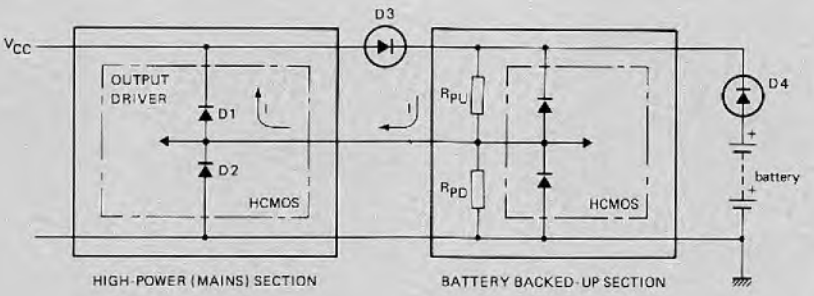


Fig.2 Pull-up resistors at the interface between high-power (mains) fed sections and the battery-fed section can lead to a sneak currents (I) when the normal power supply fails. This current passes through the pull-up resistor R_{PU}, back along the signal path to the high-power logic, severely draining the back-up battery

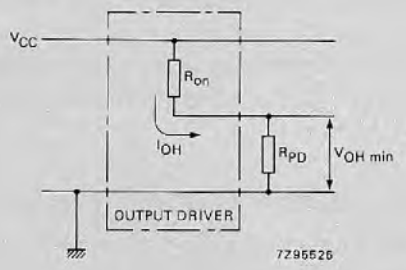


Fig.3 Pull-down resistors avoid the problems of sneak current paths. The minimum value of the pull-down resistance R_{PD} must be selected to guarantee that the HIGH output level of the driver doesn't fall below the $V_{OH\,min}$ for the $I_{OH\,min}$ being sourced. R_{on} represents the on resistance of the p-channel transistor of the driver IC

Figure 3 shows how you can instead select a pull-down resistor (R_{PD}) that avoids this problem.

The minimum value of R_{PD} is selected to guarantee that the HIGH output level of the driver doesn't fall below the $V_{OH\,min}$ for the $I_{OH\,min}$ being sourced. In Fig.3, resistor R_{on} represents the "on" resistance of the p-channel transistor of the driver IC. Its value is given by:

$$R_{on} = \frac{V_{CC} - V_{OH}}{I_{OH}}$$

and the value of $R_{PD\,min}$ is given by:

$$R_{PD\,min} = \frac{V_{OH\,min}}{I_{OH\,min}}$$

Example:

For $V_{CC} = 4{,}5$ V, $V_{OH\,min} = 3{,}98$ V at $I_{OH\,min} = 4$ mA and:

$$R_{PD\,min} = 3{,}98/(4 \times 10^{-3}) \cong 1\ \text{k}\Omega.$$

The maximum value of R_{PD} is set by the maximum allowable leakage current that will still allow the logic to reach its required level. For supply voltages lower than 4,5 V, use the output curves in the User Guide to determine the output current available.

Pull-up resistors should also be avoided on buses at the interface between battery backed-up sections and high-power sections, and you should design the system with active-HIGH signals at the bus. Then when power fails, the outputs of the high-power section will be set to their initial state. If instead you opted for active-LOW signals at the bus, you would again get a current sneak path through the protection diodes of the high-power section (Fig.4), severely draining the back-up battery.

Use the minimum supply voltage for your needs

From expression (1), you can see that dynamic power dissipation is also proportional to the square of the supply voltage. So for the battery-fed section, at least, it's essential to keep the supply voltage low. You should, in fact, choose a supply voltage just high enough to fulfil your speed requirements.

It's worth mentioning here the new low-voltage Jedec Standard 8 for battery operated systems. This standard was established to allow for future scaling-down of design rules without the problems caused by high electric-field stresses that would inevitably occur if the supply were to remain at 5 V. The Standard recognizes the need to maintain compatability with existing 5 V TTL circuitry, and accordingly, recommends somewhat higher operating voltages than would be expected purely on the basis of directly scaling down of design rules.

The recommended voltages are $3{,}3\ \text{V} \pm 0{,}3\ \text{V}$ for the normal power supply and $2{,}8\ \text{V} \pm 0{,}8\ \text{V}$ for unregulated LVBO (low-voltage battery operation). These are, of course, ideal for HCMOS, but designers must be able to contend with the nearly ±30% voltage fluctuation the

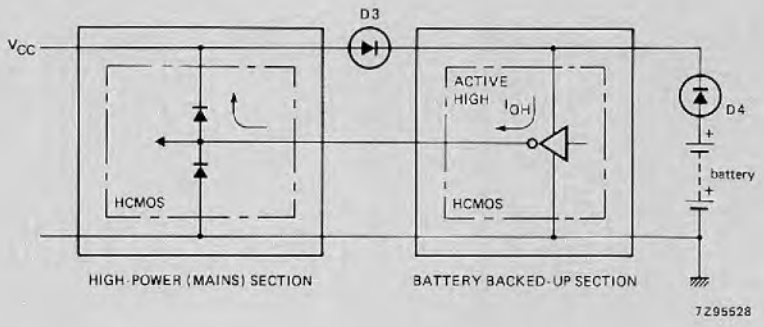


Fig.4 Systems should be designed with active-HIGH signals at buses interfacing battery backed-up sections and high-power sections. This again avoids current sneak paths and sets outputs of the high-power sections to their initial state when power fails

standard allows for battery powered systems (which provides a 2 V lower limit covering the end-of-discharge levels of lead-acid cells and two series-connected nickel-cadmium cells, as well as of lithium-based cells). Standard 8 also specifies the d.c. interface parameters that provide for inter-system compatability between the LVBO HCMOS and TTL.

Use only low-power LCDs

If you are using LCDs, make sure they are low-power ones. And remember, since no quiescent current flows in an LCD, make sure you also use low-capacitance versions.

Power-down microprocessors and memories when not in use

Power-down microprocessors and memories when not in use and switch logic to its idle state when operation is not required.

Here, you will probably have to devise software or hardware-controlled stand-by facilities to yield power savings when (long) battery operation is required. Remember that systems generally spend most of their time waiting for external events to occur or for specified intervals to elapse, so design your software to take advantage of this fact. Remember also that memories spend most of their time in the quiescent mode, so you should use memory ICs that consume minimum power in this mode. Here, of course, you'll find CMOS systems ideal. Finally, minimize switching by basing your designs on algorithms that reduce the number of gates which have to switch to perform a particular function. Silencing unused logic is another way to eliminate unnecessary gate switching.

Terminate unused inputs

Terminate all unused inputs, either to V_{CC} or to GND (via resistors of between 1 kΩ and 1 MΩ), otherwise you might find some inputs floating into the linear region. This is, of course, good practice anytime, not just for battery operation. Where no GND or V_{CC} is readily available, it's often tempting to connect the unused pin to a well-defined switching pin. However, this isn't recommended with battery-powered systems owing to the redundant circuitry that is then switched.

Use crystal oscillators for low-power consumption

Most oscillators based on logic ICs operate mainly in the linear region so they draw quite significant through-currents. Schmitt-trigger oscillators are the worst offenders in this respect, followed by RC oscillators and then by crystal oscillators.

Power consumption of Schmitt-trigger and RC oscillators is relatively independent of frequency, which means that you derive no advantage from operating them at low frequency, and that their quiescent power consumption is high. Crystal oscillators, on the other hand, have a power consumption that's directly proportional to frequency, so you can operate them at lower frequency to reduce power consumption. For these oscillators, a good choice of operating frequency is 32 kHz because crystals for this frequency are readily available, and the frequency is low enough to give reasonably low power consumption.

Use economical bus structures to save power

In this respect, the non-proprietary CMOS STD Bus (produced by more than eighty manufacturers worldwide) definitely has the edge over the C44 Bus structure. The CMOS STD Bus, developed to match the characteristics of CMOS microprocessors, is a modified and upgraded version of the STD Bus and includes a battery stand-by facility. Major features in its favour are its average current drain and operation time, both of which are about 1/500th that of the C44 Bus.

PRACTICAL CIRCUITS FOR PROVIDING BATTERY BACKUP

HCMOS ICs, like all other CMOS families, have an input structure that provides excellent protection against ESD. This input structure does, however, mean that you must ensure the supply voltage of the driving system is never more than one diode drop above the driven circuit supply voltage. If it is, current will flow through the input protection diode to V_{CC}, and this will not only cause quiescent power dissipation, it could also damage the diode if it greatly exceeds the diode's maximum d.c. rating I_{IK} (20 mA).

In practice, however, power fed from the normal supply via an output and then via an input protection diode is not totally lost since it does provide power for the battery-powered section. And the diode will be completely safe provided the current to V_{CC} doesn't exceed 20 mA continuously for one input, or 50 mA for several inputs biased simultaneously (if types with bus-driver outputs are used, this latter figure can go as high as 70 mA). What's more, since HCMOS is completely latch-up free, there's no danger of latch-up being caused by any input currents triggering parasitic bipolar structures. If these currents are very large, however, say between 120 and 150 mA, the polysilicon resistors in the diode input circuitry path will burn out.

In the example of Fig.5, HIGH-to-LOW level-shifters 74HC4049 or 74HC4050 are used to prevent the flow of positive input currents into the system due to input voltage levels being greater than one diode drop above V_{CC}. The level shifters simply reduce the input voltages to a level below this value to prevent current flowing through the input protection diode. If the circuit is such that input voltages can still exceed V_{CC} even with level shifters, then external resistors should be included to limit the input currents to 20 mA. External resistors may also be necessary in the output circuits where, if the output voltage can be pulled above V_{CC} or below GND, the currents should be limited to 20 mA. These currents are due to inherent V_{CC}-to-GND diodes that are present at all outputs (including three-state outputs).

To avoid input diode current in the receiving part of Fig.4, the same HIGH-to-LOW level shifters can be used to replace the inverter.

Figure 6 shows a very simple circuit for providing battery back-up using a dry battery, or a rechargeable battery if a trickle-charge resistor is used. Diode D_1 is included to ensure that, in normal operation, the main supply voltage never exceeds the voltage of the backed-up supply. If Schottky diodes (V_f = 0,2 V) are used, however, D_1 can be omitted.

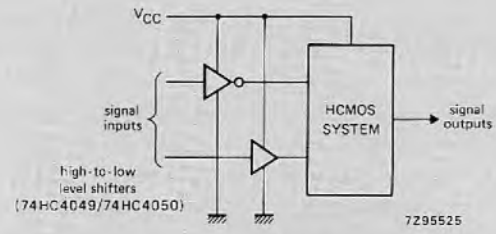


Fig.5 HIGH-to-LOW level-shifters 74HC4049 or 74HC4050 prevent the flow of positive input currents into the system due to input voltage levels being greater than one diode drop above V_{CC}. The level shifters simply reduce the input voltage to a level below this value to prevent current flowing through the input protection diode

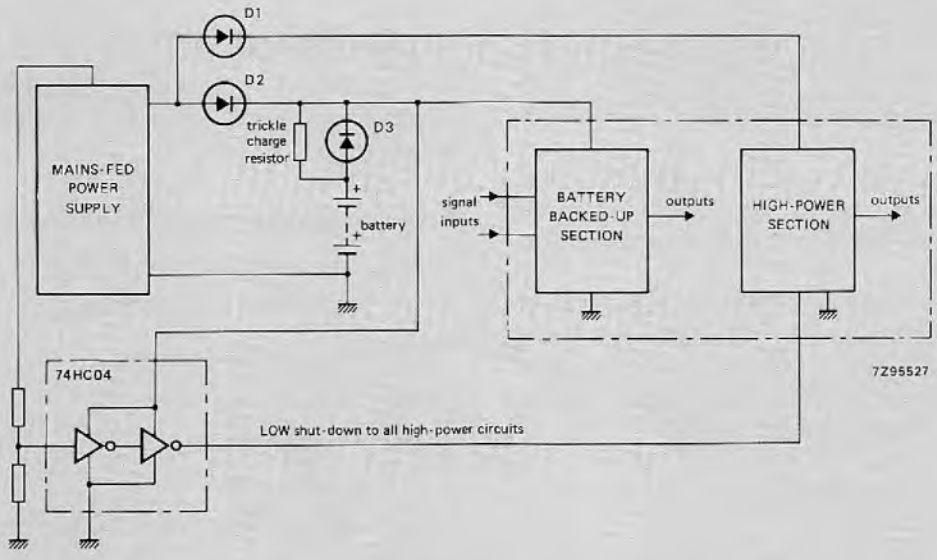


Fig.6 A simple circuit for providing battery back-up using a dry battery, or a rechargeable battery if a trickle-charge resistor is used

Many designers like to include some kind of regulation circuitry in their battery supply to provide the system with a constant voltage even while the battery voltage decreases during discharge. CMOS circuits, however, can operate directly from batteries despite the voltage decrease with discharge. If, however, the system is designed to run at maximum speed at V_{CC} = 5 V and the battery voltage falls to say 3,5 V, a reduced operating frequency will have to be accepted.

Figure 6 provides a power-down failure signal by means of a 74HC04 driven from a higher-voltage (unregulated) supply. If power goes down, the input to the 74HC04 (normally about 5 V) goes to zero, giving an active-LOW shut-down signal.

POWER MANAGEMENT IN BATTERY-POWERED SYSTEMS

Battery backed-up systems should be designed to use very little stand-by power, so your first aim should be to get as good an estimate as possible of the stand-by power P_S in your system. In HCMOS systems, the best estimate of stand-by power can be got by taking all the worst-case I_{CC} quiescent currents for each individual IC and adding them to any termination currents. Table 1 gives you the worst case I_{CC} values for different IC classes of complexity (SSI, FF, MSI).

TABLE 1
Max. quiescent supply current per device category

device complexity	I_{CC} at V_{CC} max		
	25 °C	85 °C	125 °C
SSI	2 μA	20 μA	40 μA
FF	4 μA	40 μA	80 μA
MSI	8 μA	80 μA	160 μA

The I_{CC} used is determined by the temperature range over which the system will operate. For example, a 74HC00 operating from −40 to +85 °C will have a worst-case I_{CC} of 20 μA.

The total dynamic power dissipation P_D of an HCMOS system was given by expression (1) earlier. The total power P_T of the system will then be the sum of the stand-by power P_S and dynamic power P_D, and the average current delivered by a battery with a voltage V will be:

$$I_{AV} = \frac{\delta P_T}{V}$$

in which δ is the duty factor of the back-up system (estimated power-down time as a fraction of the total operating time).

The lifetime of the battery will then be:

$$\text{battery lifetime} = \frac{\text{ampere-hour rating of battery}}{I_{AV}}$$

BATTERIES

Depending on the application, you can provide battery back-up with either rechargeable batteries or dry batteries.

Rechargeable batteries

For applications in which power interruptions may be frequent and of fairly long duration (for example during transport), you should use rechargeable batteries. Here the best choice is still the nickel cadmium battery. This is available in several sizes and can be soldered to a printed circuit board as a discrete component.

Nickel cadmium batteries present very few problem in use, and provided you treat them properly, particularly when charging them, they should have a long and trouble-free life. The best way of keeping them fully charged is to incorporate a trickle-charging circuit that provides a low, continuous current (roughly 0,03 x cell capacity). Expect a nominal operating voltage of 1,25 V per cell, and a minimum voltage of about 1 V per cell.

The alternative to the nickel-cadmium battery: the sealed lead-acid battery has a nominal voltage per cell of of about 2 V and a lower limit of 1,8 V. Like the nickel-cadmium battery it requires no maintenance. It's best used where charging may be infrequent, say after several hours of operation. Its shelf discharge rate is lower than that of a nickel-cadmium battery and when fully charged, it will have a shelf life of about two years.

Dry batteries (non rechargeable)

You can use dry batteries in applications where power interruptions are likely to be seldom and short. Six options are available:

Leclanché batteries possess the following advantages:

- they can be bought almost anywhere
- and they fit into standard fittings

and the following disadvantages:

- their life is relatively short
- their power is relatively low
- they're rather bulky
- and even with intermittent loading, their discharge rate is high.

Their nominal operating voltage is around 1,5 V per cell down to a minimum of around 1 V per cell.

Alkaline batteries possess the same advantages as Leclanché batteries. And they have the additional advantages of being able to provide greater power (especially for loads with heavy and continuous current drain), and of being able to operate at lower temperature (down to −30 °C).

Zinc-Mercury batteries posses the following advantages:

- they're compact
- they have a fairly flat discharge characteristic
- and they provide relatively high power

and the following disadvantages:

- they're not easy to acquire (normally only available from specialist suppliers)
- their life is relatively short
- they're not suitable for delivering high currents
- they don't operate well at low temperature
- and they can't be used in standard fittings.

Their nominal voltage is around 1,35 V per cell.

Zinc-silver batteries have about the same advantages and disadvantages as zinc-mercury batteries and a nominal voltage of 1,5 V.

Zinc-air batteries have the same advantage and disadvantages as zinc-mercury and zinc-silver batteries and like zinc-silver batteries they have a nominal voltage of 1,4 V per cell. They also have an operating life almost double that of the other two types.

Lithium batteries possess the following advantages:

- they have a high voltage per cell (say a minimum of 2 V)
- they have a long shelf life (greater than 10 years)
- they're compact (often disc-shaped so they can be easily soldered to a print board)
- they have a very flat discharge characteristic (see Fig.7)
- their wide operating temperature range matches perfectly that of HCMOS
- and finally, they offer you the highest energy density of all batteries

and the following disadvantages:

- like mercury batteries they're not always easy to find
- and they can't be used in standard fittings.

So, wherever power interruptions are likely to be seldom and short, your best choice is undoubtedly the lithium battery, the characteristics of which are given in Table 2.

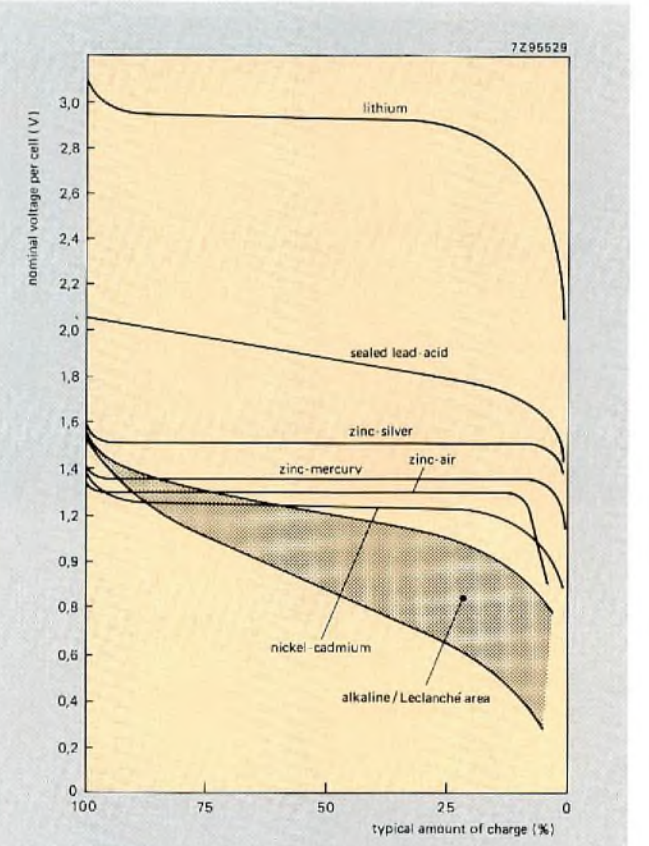


Fig.7 Cell voltage as a function of charge for various batteries

TABLE 2
Characteristics of lithium batteries

cathode material	operating voltage (V)	energy density (Wh/kg)	discharge rate	seal type	operating temp. (°C)	size
iodine	2,8	140	low to 0,5 Ah	hermetic	−55 to +125	small
carbon mono-fluoride	2,7	280	medium to 1 Ah	plastic crimp	−20 to +55	large
manganese dioxide	3	270	medium to 1 Ah	plastic crimp	−20 to +55	large
copper oxide	1,7	300	medium to 1 Ah	plastic crimp	−55 to +125	large
sulphur dioxide	2,8	330	1 Ah and more	hermetic vented	−55 to +75	

The disadvantage of not being able to use it with standard fittings will be of little importance since in normal applications you'll only need to renew the battery once every 10 years so it can be soldered into the circuit.

Finally, to help choose the best battery for your application, we've included Table 3 which shows the major parameters of various types of battery.

TABLE 3
Major specifications of various batteries

	nominal voltage (V)	typical capacity (Ah)	operational power (W/kg)	operational energy density (Wh/kg)	operational energy density (Wh/cm³)	temperature range storage (°C)	temperature range operating (°C)	shelf life to 80% capacity (months)
Dry batteries (non-rechargeable)								
Lechlanché								
– ammonium chloride	1,5	0,05 - 30	1,0	45	0,12	–40 to 50	– 6 to 50	6 - 24
– zinc chloride	1,5	0,1 - 9	1,5	88	0,18	–40 to 70	–17 to 70	30
alkaline	1,5	0,1 - 20	2,0	92	0,22	–40 to 50	–30 to 55	30
zinc-mercury	1,35 - 1,4	0,02 - 28		120	0,39	–40 to 60	0 to 55	30
zinc-silver (monovalent)	1,5	0,04 - 0,3		120	0,48	–40 to 60	0 to 55	18
zinc-air	1,4	0,2 - 0,3		500	1,45	–40 to 60	– 8 to 55	30
lithium	3,0	1,1 - 10		330	0,53	–50 to 70	–40 to 70	60
Rechargeable batteries								**charge cycles**
lead acid (sealed)	2,0	0,03 - 25	3,5	30	0,1	–40 to 60	–40 to 60	100 - 500
nickel-cadmium (sealed)	1,2	0,02 - 5	35	35	0,09	–40 to 60	–20 to 45	300 - 2000

Courtesy of Philips Lighting Division.

Standardizing latch-up immunity tests for HCMOS logic ICs

ROB CROES and PETER HENDRIKS

Like all other integrated CMOS logic circuits, the 74HC/HCT/HCU family of HCMOS logic ICs contain a number of parasitic 4-layer bipolar structures (SCRs) which may be triggered by current transients caused by high-level voltage transients at the input, output or supply pins. Once one or more of these parasitic structures has been triggered, a low-impedance path exists between the internal supply rails. This pulls the supply voltage down to a low level causing a flow of supply current (several hundred mA) which exceeds $I_{CC\,max}$ and causes excessive or destructive power dissipation. If the low-impedance path between the supply rails persists after the transient has passed (quiescent I_{CC} exceeds the maximum specified value), the IC is said to be in latch-up.

This article discusses the parasitic bipolar structures within HCMOS ICs, and describes the precautions that have been taken during the manufacturing process to minimize their effect. It also describes four test methods which effectively evaluate the input/output currents and the supply overvoltage which are necessary to induce latch-up.

The four tests are:

1. Continuous current (2 ms to 5 s) into inputs/outputs with the supply voltage applied either before or after the input/output current has been established. The 5 s current duration can only be used if the power dissipation is below 500 mW. This test can be performed with automatic test equipment.
2. Pulsed currents into inputs/outputs (<2 ms). A less severe worst-case type of test (less heat generation and delay storage effect allows higher currents before latch-up occurs) that creates a more realistic simulation of transients and also allows the test to be automated.
3. Capacitor discharge into inputs to simulate electrostatic discharge.
4. Supply overvoltage.

Extensive application of these tests to several different brands of high-speed CMOS ICs has shown that tests 1 and 4 alone are sufficient to evaluate the sensitivity of any IC to all four types of latch-up stimulus. Since test 2 allows higher test currents to be applied before latch-up occurs, especially when the pulses are very brief (<1 μs) test 1 will indicate the worst-case (lowest) currents required to initiate latch-up.

All latch-up tests published so far lack essential information and require a dedicated test set-up. We therefore propose tests 1 and 4 for use as a standard for evaluating latch-up immunity of high-speed CMOS ICs.

It is also possible to use a transistor curve tracer (Tektronix 576 or similar) to perform tests 1 and 4 to very quickly evaluate the latch-up immunity of HCMOS ICs. The tests performed with a transistor curve tracer have the added advantage of being non-destructive and clearly indicating the V/I relationship after latch-up to indicate the severity of the phenomenon. They also show the 'snap back' voltage (sustaining voltage) after V_{CC} breakdown and the minimum holding current. This gives a good indication of the maximum supply voltage that can be used without parasitic SCRs being triggered. Because bipolar transistor current gain (h_{FE}) and the value of resistors increase with increasing temperature, high ambient temperature or localized die heating results in reduced latch-up immunity.

The JEDEC standard test being developed for latch-up specifies that the input/output current should be equal to

the maximum rating (±20 mA), and that V_{CC} should also be not more than twice $V_{CC\ max.}$ (14 V) for testing latch-up immunity with excess supply voltage. HCMOS ICs have been extensively subjected to the previously described tests with test parameters far exceeding those quoted by JEDEC. In no case did latch-up occur. For example, it has been determined that an HCMOS input can typically withstand continuous current (5 s on, 15 s off) of 100 mA to 120 mA, or 1 μs pulses of 300 mA with a duty factor of 0,001. An input can also withstand a discharge from a 200 pF capacitor charged to 330 V. An HCMOS output can withstand continuous current (5 s on, 15 s off) of 200 mA to 300 mA, or 1 μs pulses of 400 mA with a duty factor of 0,001. However, because there is an internal polysilicon 100 Ω resistor in series with all HCMOS inputs, the input voltages required to achieve these current levels are so high ($V_I = V_{CC} + 0{,}7\ V + 100I_I$) that it is unlikely that they could occur in practice, even in a 6 V system with severe glitches. Moreover, beyond these current levels, excessive heating occurs or aluminium tracks or bond wires break-down. It is therefore reasonable to conclude that HCMOS logic ICs are completely latch-up free.

THE LATCH-UP PHENOMENON

Output current triggered latch-up

A CMOS structure in which latch-up can occur is shown in Fig.1(a); the equivalent circuit formed by parasitic diodes of the n-channel MOS transistors with adjoining n^+ and p^+ regions is shown in Fig.1(b). The resistors represent resistance to lateral current flow and their values depend on circuit geometry and doping.

Application of a negative voltage to the output results in a current (I) which, in turn, gives rise to a current $I+(I/h_{FE})$ in the collector of TR_2. If this current causes sufficient voltage drop across r_c, TR_3 conducts. Since the h_{FE} of TR_2 is fairly high, hardly any of the collector current of TR_3 flows into the base of TR_2. Most of the collector current of TR_3 therefore flows through $r_{bb'1}$ and $r_{bb'2}$. If sufficient voltage is dropped across $r_{bb'1}$, TR_1 turns on. Since the collector current of TR_1 then further increases the base drive of TR_3, thyristor (SCR) TR_1/TR_3 is latched and current I, due to the negative voltage on the output pin, is no longer necessary to sustain the low impedance path between V_{CC} and ground. In principle, the current through SCR TR_1/TR_3 is only limited by the source resistance of the power supply.

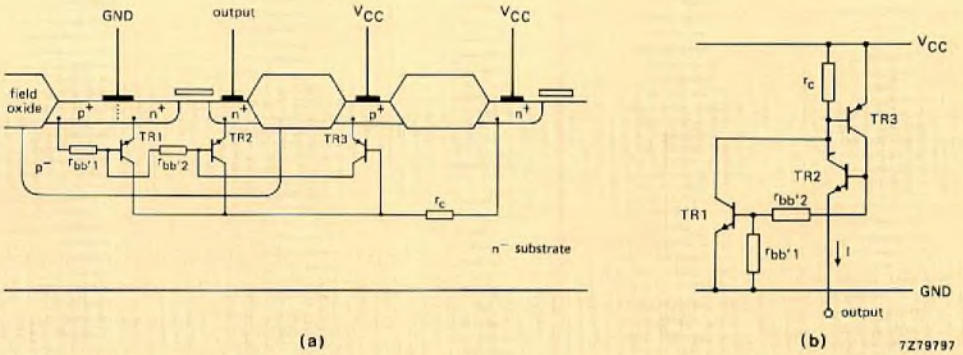


Fig.1 (a) Section through a CMOS IC showing how parasitic components are formed, (b) equivalent circuit of the parasitic components

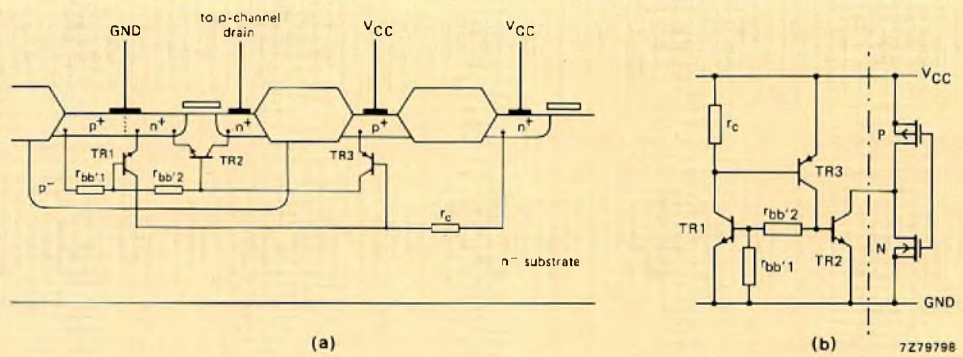


Fig.2 (a) The structure of Fig.1, but with TR_2 now formed laterally, (b) equivalent circuit incorporating lateral transistor TR_2

Latch-up triggered by excessive supply voltage

Latch-up can also be initiated via the supply line. Figure 2(a) shows a similar circuit structure to that in Fig.1(a) but now TR_2 is lateral, formed by the source and drain junction of the associated n-channel MOS transistor forming part of a complementary inverter stage. Its p-channel complement (not shown), when conducting, connects the n-channel drain and the collector of TR_2 to V_{CC}. The equivalent circuit of this arrangement is in Fig.2(b).

Excessive supply voltage when the p-channel MOS transistor is conducting (output HIGH) can break-down the collector-base junction of TR_2. SCR TR_1/TR_3 will then be triggered if the resulting current-flow through $r_{bb'1}$ is sufficient to turn on TR_1. Although the breakdown current through TR_2 is limited by the on-state resistance of the p-channel MOS transistor, the current through SCR TR_1/TR_3 is limited only by power supply resistance.

It can be seen from Fig.2(b) that a fast positive-going transient on the supply line can also trigger SCR TR_1/TR_3 because it will cause current through $r_{bb'1}$ via the capacitance of the collector-base junction of TR_2.

Input current triggered latch-up

As shown in Fig.3, all HCMOS ICs have an intentional input diode/resistor network to protect the thin oxide gate area of the logic against electrostatic discharges. If input voltages exceed V_{CC} by one V_{BE}, or go negative by more than one V_{BE}, current flows through the input diodes which, together with neighbouring diffusions on the die, can act as parts of parasitic bipolar structures such as transistors or 4-layer devices (SCRs).

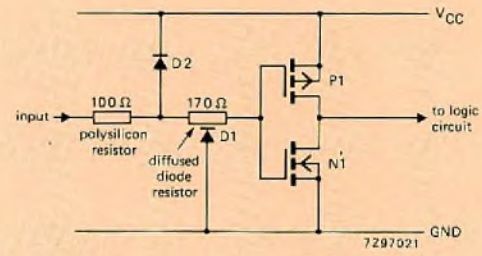


Fig.3 HCMOS input structure

WHY HCMOS LOGIC ICs ARE NOT LATCH-UP PRONE

It can be seen from Fig.1 and 2 that both the values of $r_{bb'1}$ and r_c, and the topologies of the p^+ and n^+ diffusions into the n-substrate are important factors influencing the susceptibility of a CMOS logic IC to thyristor latch-up. The latch-up immunity of HCMOS ICs has been considerably improved by careful design of the source-to-pocket contacts of the n-channel MOS transistors and the interchange of the p^+ and n^+ diffusions into the substrate as shown in Fig.4. The value of r_c could be reduced by arranging the n^+ diffusion as a guard ring around the n-channel MOS transistor but this would considerably increase the area of the device. As shown in Fig.5, the problem has been solved by preventing lateral current flow in the n^- substrate by growing an epitaxial layer on a very low resistivity substrate. Also important for improving latch-up immunity are the established HCMOS layout rules and process parameters that minimize the current gain of the parasitic bipolar transistors.

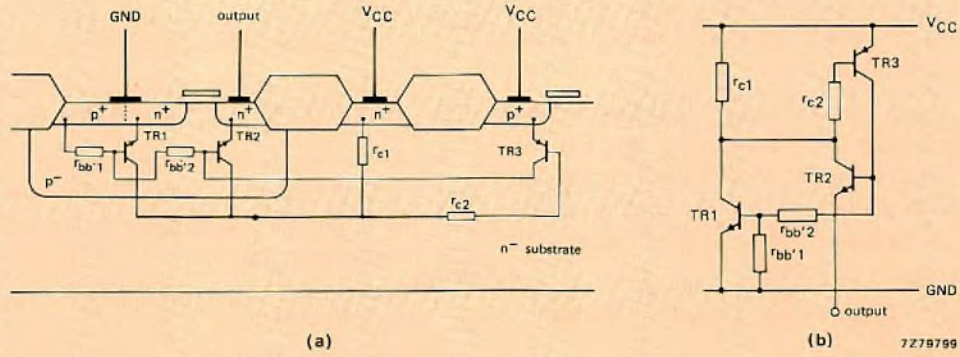


Fig.4 (a) Rearrangement of the structure of Fig.2 greatly increases latch-up immunity by incorporating base resistance r_{c2} (b) equivalent circuit

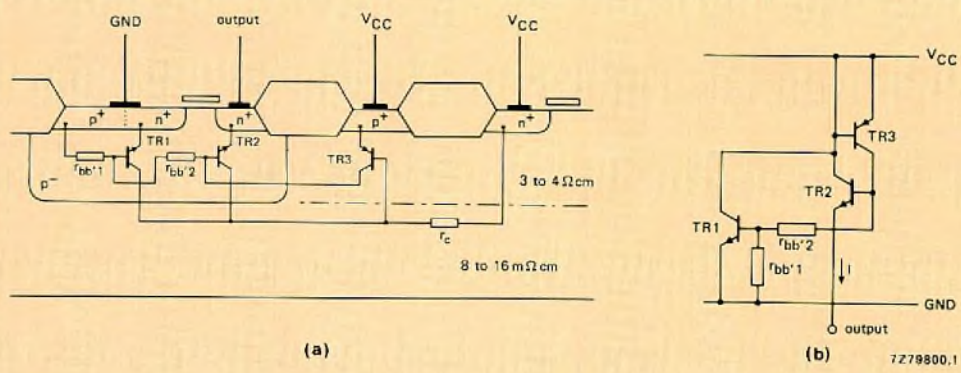


Fig.5 (a) By growing an epitaxial layer on a very low resistivity substrate, the lateral current flow responsible for latch-up is very largely eliminated, (b) equivalent circuit

LATCH-UP IMMUNITY TESTS

It should be noted that, when an HCMOS IC is subjected to a test to evaluate its immunity to latch-up, the applied currents and voltages will exceed the absolute maximum ratings of the IC to such an extent that they will almost certainly degrade its performance and may even destroy it. Latch-up immunity tests are therefore only intended for characterization purposes and should never form part of production tests. Any IC that has been subjected to latch-up immunity tests should be discarded so that it cannot be used for design or production purposes.

Test conditions and limits

When testing the immunity of HCMOS ICs to latch-up, the following limits and conditions must be observed:

- If $\pm I_I$ or $\pm I_O$ exceed the maximum ratings (±20 mA), the tests may be damaging or even destructive. For d.c. testing with higher currents, the trigger current should therefore only be applied for short periods (e.g. 5 s) followed by a cooling period of three times this duration. Alternatively, automatic tests with low duty-factor pulsed current can be used.
- The minimum trigger current duration is 2 ms over the entire temperature range. The maximum trigger current duration is 5 s. The rise and fall times are not critical but to avoid correlation problems, suitable limits are 50 μs to 1 ms measured between the 10% and 90% amplitude points. A timing diagram is shown in Fig.8.
- The supply current (I_{CC}) must be limited to 200 mA to avoid excessive heating.
- Ambient temperature should be high (85 °C to 125 °C).
- To confirm that latch-up was the true cause of the quiescent supply current exceeding the maximum specified value after a latch-up immunity test, the IC must be checked electrically and functionally to verify that no damage has occurred.

Applying continuous (2 ms to 5 s) input/output current to test latch-up immunity

Since the parasitic SCRs are current triggered, it is possible to trigger them by forcing current through the input protection diodes or through the parasitic bipolar structures at the output. The test circuit shown in Fig.6(a) forces current through the diode between an input/output pin and V_{CC}; the test circuit in Fig.6(b) forces current through the diode between an input/output pin and GND. The supply pin (V_{CC}) is at ground potential in Fig.6(a) because otherwise, the source of supply voltage would have to sink current and there would be danger of this causing the supply voltage to increase.

There are two methods of performing this test, the timing requirements for which are given in Fig.8. The first is to apply V_{CC} before forcing the current into the input/output. This simulates the application of an input/output voltage which exceeds the supply voltage. The test procedure is:

1. Connect all unused inputs of the IC under test to VCC or GND.
2. Set the current source to zero.
3. Connect a current limited (200 mA max.) 7 V supply between the V_{CC} and GND pins of the IC under test.
4. Either ramp-up the current source or set it to the test level. If testing an output, make sure that the state of the IC inputs is such that the output is HIGH for positive-going trigger current, or LOW for negative-going trigger current. A 3-state output should be in the high impedance state.
5. Set the current source to zero and ensure that the input being tested is at V_{CC} or GND. If an output is being tested, check that it is open (current source disconnected).
6. Check the supply current (I_{CC}). If latch-up has occurred, it will be about 200 mA. If it is, verify that the input/output circuitry has not been damaged. This should not happen unless very high test currents have been used. If

latch-up hasn't occurred (I_{CC} below max. specified value), test for continuity to determine whether the IC has been destroyed.

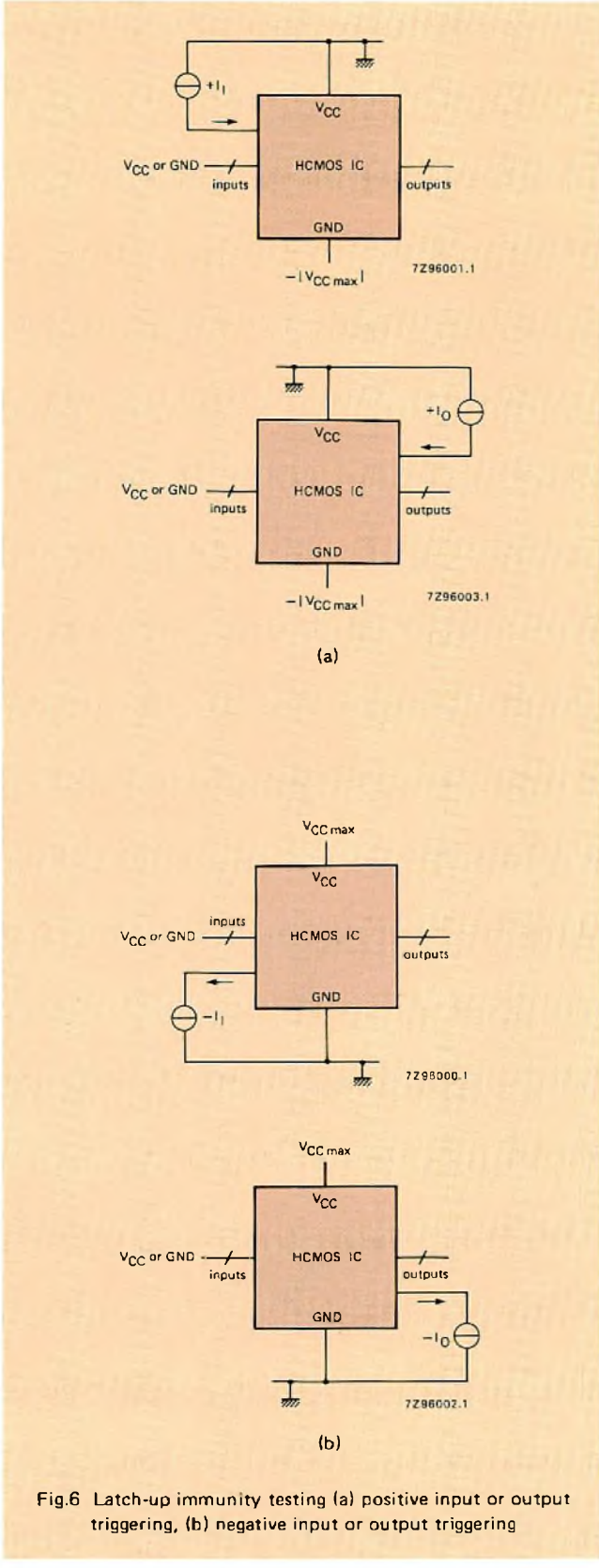


Fig.6 Latch-up immunity testing (a) positive input or output triggering, (b) negative input or output triggering

The second version of this test involves forcing the input/output currents before applying the supply voltage. This version therefore simulates a condition in which one section of a logic system is powered-down whilst its inputs remain active, and is then powered-up again. This could be caused by partial power failure or the plugging-in of boards without first switching-off (service engineers don't always follow the rules!). The test procedure is:

1. Connect all unused inputs to V_{CC} or GND.
2. Set the current source connected to the pin being tested to the test level. If testing an output, make sure that the state of the inputs is such that the output will be HIGH for positive-going trigger current, or LOW for negative-going trigger current. A 3-state output should be in the high-impedance state when the supply is connected.
3. Connect a current limited (200 mA max.) 7 V supply between the V_{CC} and GND pins of the IC under test.
4. Set the current source to zero and ensure that the input being tested is at V_{CC} or GND. If an output is being tested, check that it is open (current source disconnected).
5. Check the supply current (I_{CC}) at $V_{CC} = 6$ V. If latch-up occurred, it will be about 200 mA. If it is, verify that the input/output circuitry has not been damaged. This should not happen unless very high test currents have been used. If latch-up hasn't occurred (I_{CC} below max. specified value), test for continuity to determine whether the IC has been destroyed.

We adopt this second version of the test as standard because we consider that it is more severe than the previous one. This is because, in the first test, the trigger current could be bypassed by the output circuitry when an output is being tested. Furthermore, the second version allows bench characterization using a curve tracer in the continuous writing mode so that the complete behaviour of the IC is displayed on the screen. For the first version of the test, the curve tracer would have to be in the d.c. mode and only dots would be displayed on its screen. Both versions of the test can be performed with automatic test equipment. Testing with a curve tracer is described in the Appendix.

Input voltage considerations

Although the parasitic SCRs in HCMOS ICs are current-triggered, the input/output voltage required to achieve the trigger current must also be considered.

As previously explained, all HCMOS ICs incorporate an input protection network which includes a 100 Ω poly-silicon resistor in series with the input to limit current caused by excess input voltage (see Fig.3). This could occur due to ESD or failure of part of a power supply. Latch-up in a CMOS system is also an energy phenomenon because it can be caused by input signal overshoots or undershoots caused by crosstalk or flashes. The level of input current

caused by this induced energy depends on the input voltage level. Since the polysilicon resistor in HCMOS IC inputs limits the input current, it is also necessary to consider the level of input voltage required to induce latch-up.

To force an input current of 100 mA through one of the input diodes via the polysilicon series resistor requires an input voltage of 100I + 0,7 V = 10,7 V beyond the limits V_{CC} and GND. Forcing such a high current into an HCMOS input to induce latch-up is therefore an unnecessarily severe test because the associated high input voltage is unlikely to occur in practice, even in a 6 V system with severe glitches or overshoots. Furthermore, as shown in Fig.7, forcing very high level currents into HCMOS inputs can destroy the input resistors. It should be noted that the energy (I^2Rt) in an input resistor increases fourfold each time the input current is doubled.

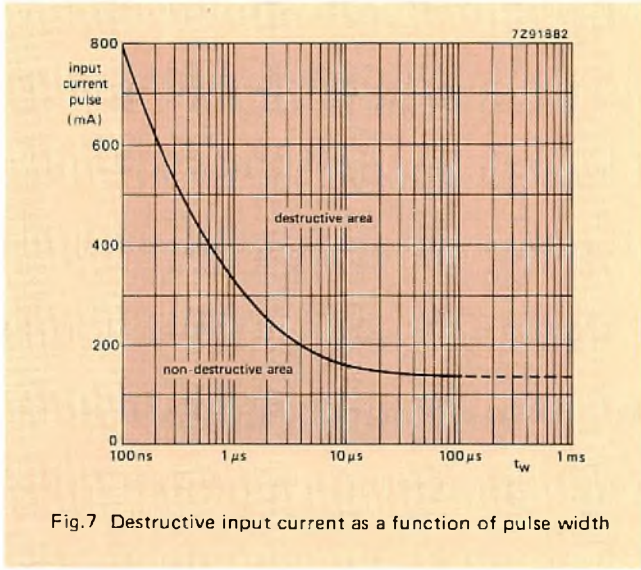


Fig.7 Destructive input current as a function of pulse width

Automatic testing of latch-up immunity

The previously described "continuous" current tests with timing as shown in Fig.8 are also suitable for automatic testing since most automatic testers incorporate current sources. Pulsed current testing with pulse widths much less than 2 ms has advantages over using longer duration pulses. For example:

- It more closely simulates glitches which are usually short-duration spikes.
- Less localized heating of the input structure allows the use of higher test currents. This is important because the ICs are less sensitive to lower currents. Latch-up is a bipolar phenomenon and requires the building up of storage effects. This effectively delays the start of SCR conduction so that higher current must be applied before latch-up occurs.

So, the main point to note is that, since the current is only applied for a short duration during an automatic test, the duration of the trigger current, and the interval between its removal and the measurement of V_{CC}, must be sufficient for latch-up, if any, to be established.

Figure 8(a) shows the timing for an automatic latch-up immunity test in which V_{CC} is applied before the input current. Figure 8(b) shows the timing for an automatic latch-up test in which V_{CC} is applied after the input current has been established.

As with other modes of latch-up immunity testing, automatic testing can also damage the input structure if the test current exceeds the limits shown in Fig.7.

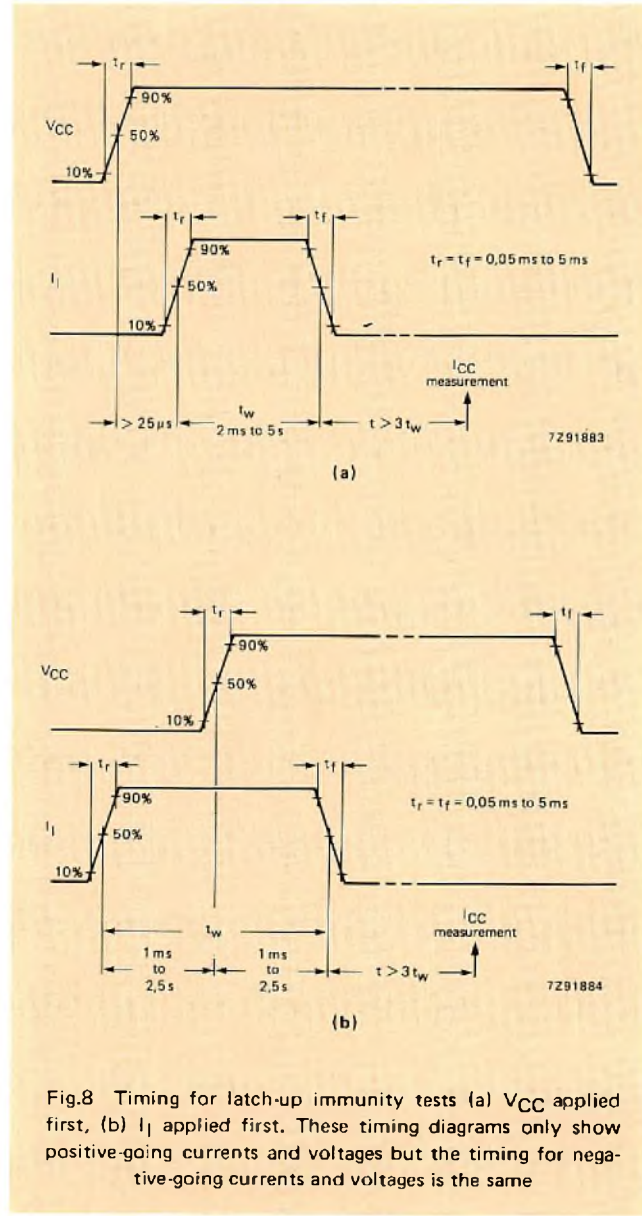


Fig.8 Timing for latch-up immunity tests (a) V_{CC} applied first, (b) I_I applied first. These timing diagrams only show positive-going currents and voltages but the timing for negative-going currents and voltages is the same

Testing latch-up immunity with simulated ESD at an input

It is also possible to initiate latch-up in a CMOS logic IC by inadvertantly applying a high-voltage electrostatic discharge (ESD) to its input (zapping). This can happen, for example, if an IC input is terminated with a connector or other

fixture which is exposed to human touch. Such a situation can be simulated by discharging a pre-charged capacitor into the input using the test circuit in Fig.9(a) for a negative-going discharge, or the test circuit in Fig.9(b) for a positive-going discharge. The 1 MΩ resistors in the test circuits terminate the test input so that it doesn't float and cause erroneous results. The test procedure is:

1. Connect a 7 V supply (200 mA current limited) between the V_{CC} and GND pins of the IC under test.
2. Set the switch to charge the capacitor to the test voltage.
3. Switch the capacitor to the input.
4. After a few seconds, measure I_{CC}. If it is greater than the maximum quiescent value quoted in the HCMOS family specification, latch-up has occurred.
5. Verify that any abnormal I_{CC} flow is not due to damage caused by the test.

Testing latch-up immunity with excess supply voltage

Latch-up can also occur if the supply voltage to an HCMOS logic IC increases beyond the absolute maximum rating to a level that causes the parasitic diode between the V_{CC} and GND rails to break down (20 V typical). Figure 10 shows that, if the supply current is limited to 100 mA, the supply voltage will then 'snap-back' to one of two holding voltages.

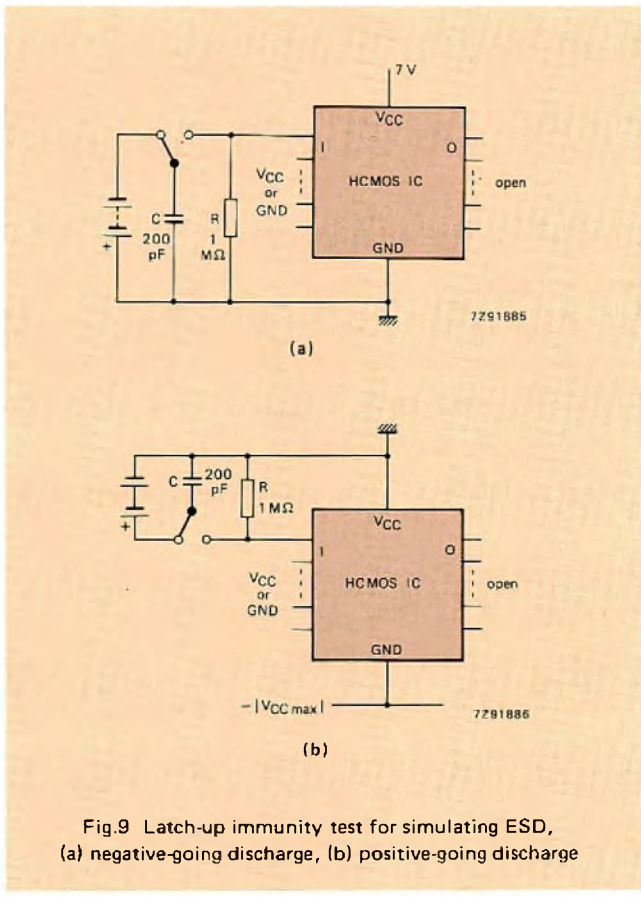


Fig.9 Latch-up immunity test for simulating ESD, (a) negative-going discharge, (b) positive-going discharge

If this voltage is above 7 V, the IC is immune to latch-up caused by excess supply voltage. If the holding voltage is below 7 V latch-up will have occurred. If excess supply voltage is applied to the IC for too long, the IC will be destroyed because the maximum power dissipated by it during the test will be as high as 2 W which is four times the maximum rating. The test procedure is:

1. Connect the test circuit as shown in Fig.11 with the supply current limited to 100 mA.
2. Increase V_{CC} until supply current flows.
3. Measure V_{CC}. If it is less than 7 V, latch-up has occurred.

This test can also be performed very rapidly by automatic testers or with a transistor curve tracer as described in the Appendix.

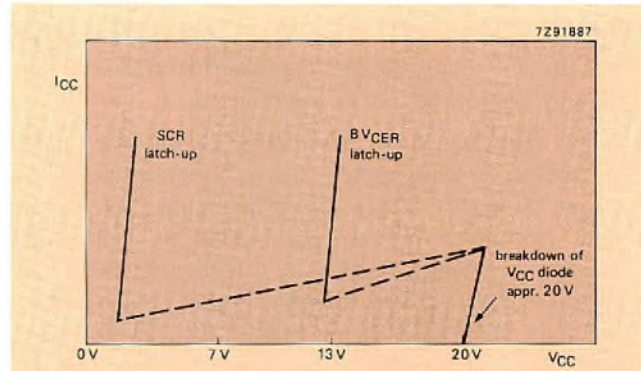


Fig.10 Sustaining voltages after testing for latch-up due to excess supply voltage

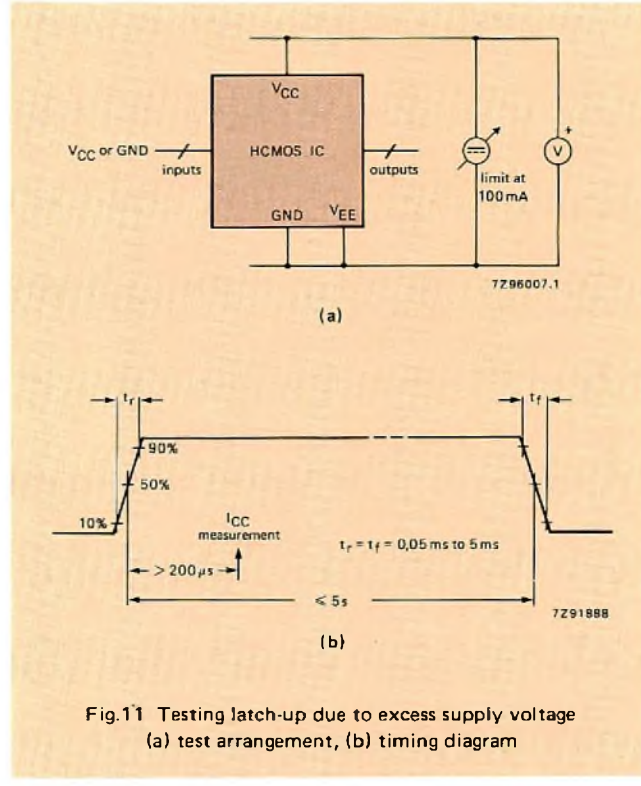


Fig.11 Testing latch-up due to excess supply voltage (a) test arrangement, (b) timing diagram

APPENDIX

LATCH-UP IMMUNITY TESTS USING A TRANSISTOR CURVE TRACER

The immunity of HCMOS ICs to latch-up caused by high input/output current or excessive supply voltage can also be evaluated with a transistor characteristic curve tracer such as the Tektronix 576. Using a curve tracer provides a quick and simple method of displaying the behaviour of the IC under test on a screen. If the correct value of collector resistor is selected in the curve tracer, the tests will be non-destructive and a wide range of currents can be used to stimulate latch-up. Any high supply current caused by input/output current can easily be observed. The collector resistor in the curve tracer influences the latch-up immunity tests in two ways:

1. It limits the supply current that can flow after latch-up, thereby making the tests non-destructive.
2. It has the undesirable effect of decreasing the supply voltage (V_{CC}) when supply current (I_{CC}) is flowing. To ensure minimum supply voltage reduction, the chosen value of collector resistor should therefore be as low as possible. However, to play safe, it is recommended that a fairly high value is selected for the collector resistor at the start of a test. The value can then be decreased whilst the effects of the tests are being observed on the screen of the curve tracer.

An important advantage of using a curve tracer is that it allows direct determination of any input current contribution to the supply current. Heating effects are also reduced because the collector voltage from the curve tracer is a continuous series of half sinewaves giving an average power dissipation of $(2/\pi)^2 V_{CC} I_{CC} = 0{,}4\ V_{CC} I_{CC}$). When testing latch-up immunity with excess supply voltage, the V_{CC} diode breakdown voltage, secondary breakdown and the SCR effect can all be evaluated.

It is important to note that, to allow the latch-up phenomenon to be shown, all the curve tracer oscillograms presented in this Appendix show the results of tests on specially manufactured ICs which are much more prone to latch-up than the ICs of the 74HC/HCT/HCU family.

CURVE TRACER CHARACTERISTICS

Figure A1 shows the voltages and currents at the collector and base terminals of a transistor characteristic curve tracer. It can be seen that there is a continuous stepped current flow from the base terminal of the curve tracer into or out of the IC being tested. Since the level of the steps changes when the voltage at the collector terminal is zero, this is in accordance with the latch-up immunity test which calls for the input/output trigger current to be established before the supply voltage is applied. This is therefore a more severe form of test than one with a static supply voltage.

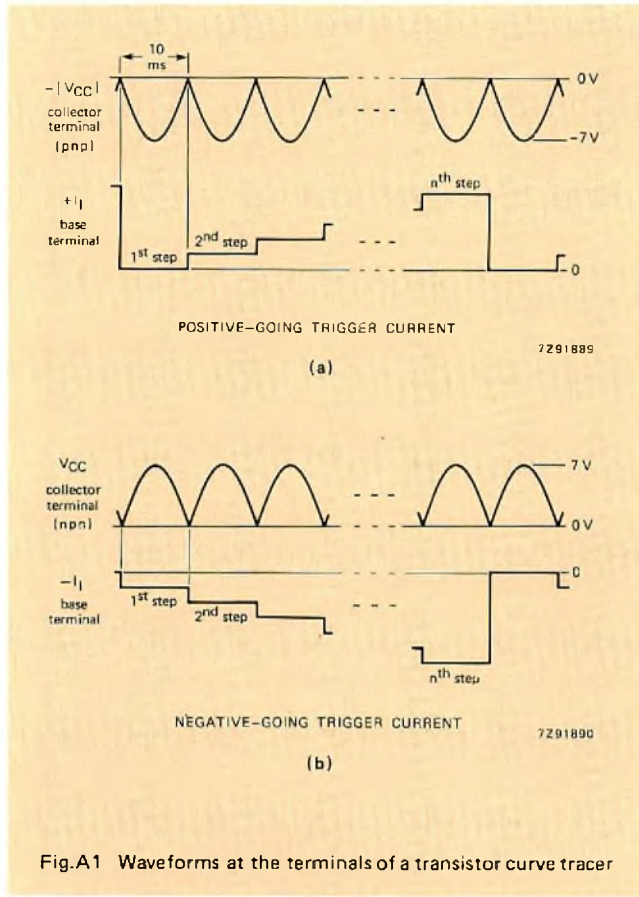


Fig.A1 Waveforms at the terminals of a transistor curve tracer

LATCH-UP IMMUNITY TESTS

Positive current into an input

The test arrangement is shown in Fig.6(a). The IC being tested should be connected to the curve tracer as follows:

- GND pin to the collector terminal.
- V_{CC} pin to the emitter terminal.
- Input pin to the base terminal (all unused inputs to GND or V_{CC}).

The controls of the curve tracer should be set as follows:

- Collector voltage: 15 V, pnp, normal mode.
- Collector series resistor: at least 140 Ω.
- Base current: 1 mA per step. Polarity: inverted.

The results of this test on a special IC used to demonstrate the latch-up phenomenon are shown in Fig.A2. The base line (top of oscillogram), being the zero current step, shows the leakage current ($-I_{GND}$) without input current. The increase of $-I_{GND}$ on the zero current step could be due to

breakdown of a parasitic bipolar junction or the onset of a field-effect leakage mechanism. According to the HCMOS specification, no supply current should flow with supply voltages up to 6 V. With higher supply voltage (even up to 15 V), 'leakage' increase can be observed by studying the zero current step trace. Because there is little parasitic bipolar action during the first three input current steps, there is very little $-I_{GND}$ flowing. The third current step (3 mA) results in $-I_{GND}$ of about 1 mA. This means that there is a bipolar transistor with a current gain of about 0,33 resulting in attenuation of about 3 in this testing mode. This will cause any positive input current to be attenuated about 3 times rather than being amplified. The fourth step (4 mA) results in the supply voltage falling to about 0,4 V due to SCR latch-up. The collector series resistor limits the supply current to about 45 mA (outside the picture). Any increase of current with V_{CC} greater than 7 V will be meaningless because the maximum V_{CC} rating for HCMOS ICs is 7 V. However, it does give an indication of how the IC will behave under severe stress or during high level V_{CC} transients.

This test can be varied by changing the combination of unused input connections and observing the screen to see if latch-up or early breakdown occurs. In particular, the input pins can be connected alternately to V_{CC} and GND or an input combination can be applied such that as many as possible of the outputs are in the same logic state.

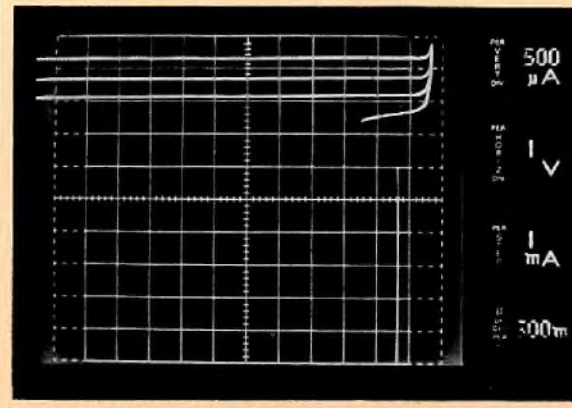


Fig.A2 Latch-up due to positive input current

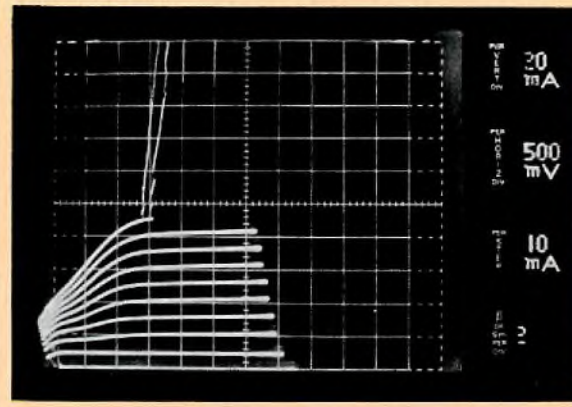


Fig.A3 Latch-up due to negative input current

Negative current drawn from an input

The test arrangement is shown in Fig.6(b). The IC being tested should be connected to the curve tracer as follows:

- GND pin to the emitter terminal.
- V_{CC} pin to the collector terminal.
- Input pin to the base terminal (all unused inputs to V_{CC} or GND).

The controls of the curve tracer should be set as follows:

- Collector voltage: 15 V, npn, normal mode.
- Collector series resistor: at least 6,5 Ω.
- Base current: 10 mA per step. Polarity: inverted.

The results of this test on a special IC used to demonstrate the latch-up phenomenon are shown in Fig.A3. If only the input protection diode between the input pin and GND were forward biased, there would only be a current flow out of the GND pin. However, there is obviously also a parasitic npn transistor with its emitter connected to the input, its base connected to GND and its collector connected to V_{CC}. This diverts the input current to the V_{CC} pin. As can be seen, the first current step (10 mA) is completely diverted to the V_{CC} pin which means that the current gain between the input and V_{CC} pins is unity. A current at the V_{CC} pin which is much higher than that being drawn from the input pin would be undesirable because the excessive supply current could destroy the IC. The maximum acceptable current gain is 2 because 40 mA of input current would then cause a power dissipation of 240 mW at V_{CC} = 6 V. Latch-up occurs on the ninth input current step (90 mA).

Positive current into an output

The IC being tested should be connected to the curve tracer as follows:

- GND pin to the collector terminal.
- V_{CC} pin to the emitter terminal.
- Output pin to the base terminal (inputs set to cause HIGH output state or high impedance state for 3-state outputs).

The controls of the curve tracer should be set as follows:

- Collector voltage: 15 V, pnp, normal mode.
- Collector series resistor: at least 650 Ω.
- Base current: 5 mA per step. Polarity: inverted.

The results of this test on a special IC used to demonstrate the latch-up phenomenon are shown in Fig.A4. In this test the inherent pn output diode is forward biased. Forward-biasing the output diode before the supply voltage is applied is the most severe test because, if V_{CC} is present, the p-channel MOS output transistor will bypass the trigger current. The decrease of $-I_{GND}$ during the increase of V_{CC} in Fig.A4 is due to the conduction of the p-channel MOS output transistor as V_{CC} increases. Latch-up occurs on the sixth output current step (30 mA).

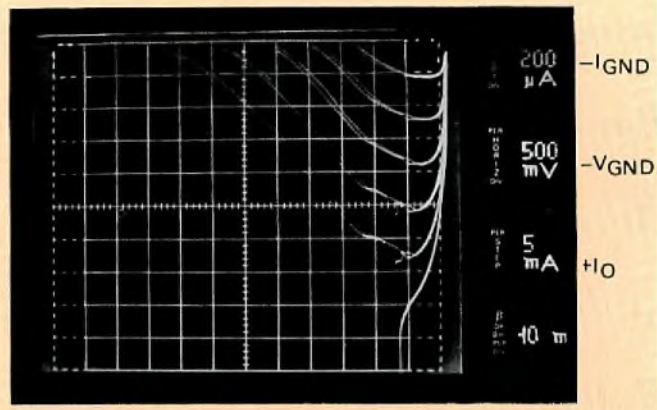


Fig.A4 Latch-up due to positive output current

Negative current drawn from an output

The IC being tested should be connected to the curve tracer as follows:

- GND pin to the emitter terminal.
- V_{CC} pin to the collector terminal.
- Output pin to the base terminal (inputs set to cause LOW output state or high impedance state for 3-state outputs).

The controls of the curve tracer should be set as follows:

- Collector voltage: 15 V, npn, normal mode.
- Collector series resistor: at least 140 Ω.
- Base current: 10 mA per step. Polarity: inverted.

The results of this test on a special IC used to demonstrate the latch-up phenomenon are shown in Fig.A5. The inherent np output diode is forward biased and latch-up occurs on the third output current step (30 mA). Figure A5 also shows that negative output current causes current at the V_{CC} pin. If there is gain between the output and V_{CC} pins, undershoot at the output in will lead to additional supply current.

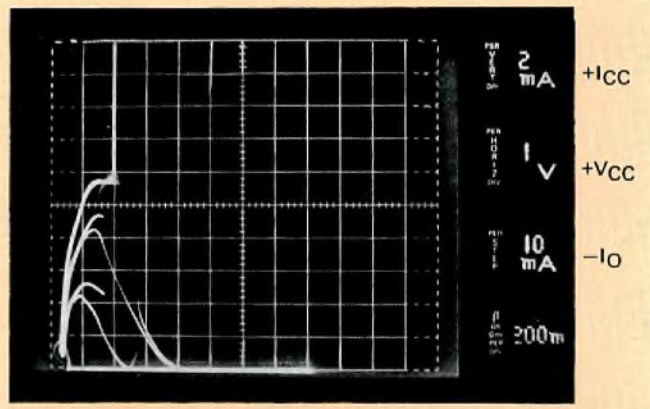


Fig.A5 Latch-up due to negative output current

Excess supply voltage

This is a very simple test set-up which only uses the output from the collector terminal of the curve tracer. The IC being tested should be connected to the curve tracer as follows:

- GND pin to the emitter terminal.
- V_{CC} pin to the collector terminal
- All input pins alternately to V_{CC} and GND.

The controls of the curve tracer should be set as follows:

- Collector voltage: 75 V, npn, normal mode.
- Collector series resistor: at least 650 Ω.

The results of this test on a special IC used to demonstrate the latch-up phenomenon are shown in Fig.A6. It can be seen that SCR latch-up occurs with only 750 µA of supply current (I_{CC}) flowing. The sustaining voltage is as low as 1,5 V so the impedance between the supply pins is nearly zero.

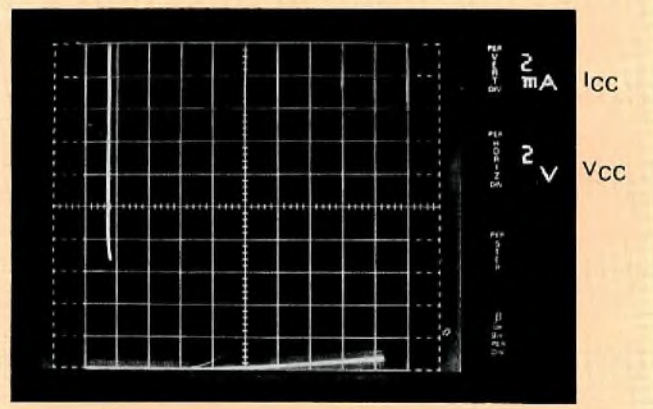


Fig.A6 Latch-up due to excess supply voltage

RESULTS OF LATCH-UP IMMUNITY ON HCMOS ICs USING A CURVE TRACER

The latch-up tests using a curve tracer have been extensively applied to 74HC/HCT/HCU logic ICs. In no case did latch-up occur. The input/output trigger tests were performed over the entire temperature range and used trigger currents up to ±100 mA continuous, and ±400 mA with a 100 ns pulse and a duty factor of 0,01. During the 100 mA continuous current test, excessive heating occurred, so the test time was restricted to a few seconds. During the test for latch-up with excess supply voltage, a breakdown current of 6,8 mA was necessary and the supply voltage snapped back to 12 V as shown in Fig.A7 in most cases. In no case was the sustain voltage less than 7 V.

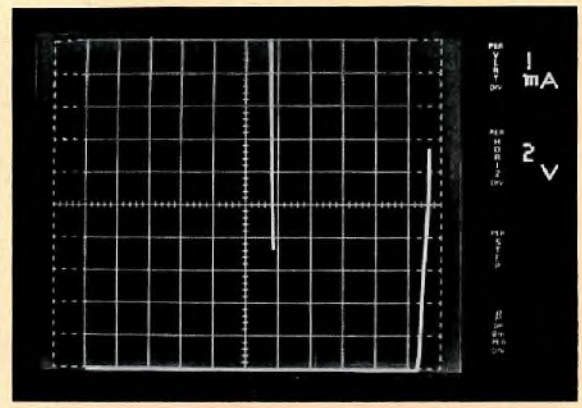


Fig.A7 Typical V_{CC} breakdown for HCMOS ICs occurs at V_{CC} = 21 V, I_{CC} = 6,8 mA.
The supply voltage then snaps back to 12 V

Abstracts

HCMOS Schmitt trigger applications

Theoretically, the high gain of integrated logic elements results in a rectangular output pulse regardless of the rise and fall times of the input signal. However, input signals with slow edges can cause the output pulses to jitter and can increase power consumption. The 74HC/HCT high-speed CMOS logic family includes two ICs with Schmitt trigger inputs to overcome these problems. This article describes how these two ICs can be used to solve all manner of waveshaping problems and to construct RC oscillators which only require two pins to be used for the signal lines.

Using 74HCT HCMOS ICs to replace LSTTL and drive transmission lines

Before the introduction of our HCMOS family of logic ICs, designers of high speed logic systems were restricted to the use of power-hungry bipolar ICs such as LSTTL. Since the logic ICs of the HCMOS family can operate as fast as LSTTL and consume much less average power, and since they can operate over a wider supply-voltage range, using them to replace LSTTL results in considerable system economies. HCMOS ICs with the prefix 74HCT are purpose-designed for replacing LSTTL or for use in mixed-technology systems. This article compares the input/output structures and performance of LSTTL and 74HCT logic ICs and discusses interfacing and low-power techniques for driving terminated data transmission lines with 74HCT ICs.

Protection of HCMOS logic ICs in the automotive environment

The harsh climatic and electrical environment in motor vehicles makes it difficult for electronic equipment to operate reliably throughout the lifetime of the vehicle. Moreover, many electronic engineers are unaware of the true character of the conditions which exist in the engine and passenger compartments of vehicles. This article fully describes the automotive environment and explains how to protect HCMOS logic ICs so that their outstanding characteristics can be fully exploited in automotive electronics applications.

Modifying LSTTL test programs to test HCMOS logic

Manufacturers switching from LSTTL logic to HCMOS will need to convert their test facilities accordingly. This article outlines how existing test software and hardware can be modified for HCMOS testing, at a minimal investment of both capital and time. The article compares characteristics, and gives guidelines for additional test parameters necessary for HCMOS testing, and for LSTTL tests that can be omitted. It also takes an in-depth look at modifying the popular Teradyne J283 system for testing HCMOS.

Battery backup of HCMOS logic ICs

With their very low quiescent power consumption and fast transition times, HCMOS logic ICs can easily be provided with battery backup if the normal power supply should fail. For long periods of battery operation, however, a number of simple guidelines should be followed to at least minimize power consumption and assure maximum battery life. This article discusses these guidelines, gives some practical circuits for providing battery backup and reviews the various batteries that are best suited for use with HCMOS.

Standardizing latch-up immunity tests for high-speed CMOS logic ICs

Latch-up is the thyristor action experienced by all conventional CMOS logic ICs. In the 74HC/HCU/HCT family of HCMOS logic ICs, latch-up has been completely eliminated by growing a high resistivity epitaxial layer on the n^- substrate to prevent lateral current flow through the substrate. This, plus proprietary layout rules and process parameters means that 74HC/HCU/HCT ICs are completely latch-up free. This article discusses these methods of eliminating latch-up and describes four tests that effectively evaluate the input/output currents and the supply overvoltage that are necessary to induce latch-up.

Anwendungen von HCMOS-Schaltungen mit Schmitt-Trigger-Funktion

Die hohe Verstärkung bei integrierten Logik-Schaltungen führt, theoretisch gesehen, ungeachtet der Anstiegs- bzw. Abfallzeiten des Eingangssignals zu rechteckförmigen Impulsen am Ausgang. Eingangssignale mit langsamen Flanken können jedoch ausgangsseitig einen Impuls-Jitter hervorrufen und dadurch eine erhöhte Leistungsaufnahme bewirken. In der HCMOS Logik-Familie sind zwei ICs mit Schmitt-Trigger-Eingängen, um diese Schwierigkeiten zu umgehen. Der Artikel beschreibt, wie diese beiden ICs eingesetzt werden können, um alle Arten von Problemen mit Signalformen zu lösen und um RC-Ozillatoren mit lediglich zwei Anschlüssen zum Betreiben der Signalleitungen zu konstruieren.

Ersatz von LSTTL-Schaltungen und Treiben von Übertragungsleitungen mit HCMOS-ICs

Vor der Einführung unserer HCMOS-Logikreihe waren die Entwickler beim Entwurf von Hochgeschwindigkeits-Logiksystemen gezwungen, leistungsverzehrende bipolare Schaltungen zu verwenden, wie z.B. LSTTL. Da die Logik-Schaltungen der HCMOS-Familie genauso schnell wie LSTTL-ICs arbeiten, dabei aber eine weitaus geringere mittlere Leistung aufnehmen und zudem über einen grösseren Bereich der Versorgungsspannung betrieben werden können, führt ihr Einsatz im Vergleich zu LSTTL zu beträchtlichen Einsparungen von Systemkosten. HCMOS-ICs mit der Bezeichnung 74HCT wurden speziell für den Einsatz von LSTTL-Schaltungen und den Einsatz in Systemen mit gemischter Technologie entworfen. Dieser Beitrag vergleicht den Aufbau der Ein- bzw. Ausgangsstufen und die Leistungsfähigkeit von LSTTL und 74HCT-Logikschaltungen miteinander; es werden Techniken der Schnittstelle und der Leistungsminimierung beim Treiben von abgeschlossenen Übertragungsleitungen mit 74HCT-Bausteinen diskutiert.

Schutz von HCMOS Logik-ICs vor Umwelteinflüssen in Automobilen

Das rauhe klimatische und elektrische Umfeld in Automobilen erschwert den zuverlässigen Betrieb von elektronischer Ausrüstung während der Lebensdauer des Fahrzeugs. Darüber hinaus sind viele Elektronik-Ingenieure in Unkenntnis über die wirkliche Natur der Umweltbedingungen, die im Motor- und Fahrgastraum herrschen. Dieser Beitrag beschreibt in umfassender Weise das Umfeld in Kraftfahrzeugen und erklärt, wie HCMOS Logik-ICs zu schützen sind, damit ihre herausragenden Eigenschaften bei Einsatz im Automobil voll ausgeschöpft werden können.

Umstellen der Testprogramme von LSTTL auf HCMOS-Logik

Anwender, die von LSTTL-Logik auf HCMOS wechseln, werden ihre Testgeräte entsprechend umrüsten müssen. Dieser Artikel gibt Übersicht darüber, wie bereits vorhandene TTL-Soft- und Hardware bei Testern ökonomisch auf HCMOS-Logik umgestellt werden kann. Der Beitrag vergleicht Charakteristiken und gibt Richtlinien für zusätzliche Parameter zum Testen von HCMOS-Schaltungen sowie für LSTTL-Tests, die entfallen können. Er befasst sich ausserdem eingehend mit dem Umstellen des bekannten Systems Teradyne J283 zum Testen von HCMOS.

Batterie-Notversorgung von HCMOS-Logik-ICs

Wegen ihrer niedrigen Ruheströme und geringen Schaltzeiten können HCMOS Logik-ICs leicht aus einer Batterie-Notversorgung gespeist werden, falls die Netzteilversorgung ausfallen sollte. Für längere Zeiträume des Batteriebetriebs sollte jedoch eine Reihe von einfachen Massnahmen beachtet werden, um wenigstens die Leistungsaufnahme zu minimieren und um eine möglichst grosse Batterielebensdauer zu gewährleisten. Der Beitrag diskutiert diese Massnahmen, stellt einige praktische Schaltungen zur Notversorgung vor und gibt eine Übersicht über die verschiedenen Batterien, die für den Einsatz in HCMOS-Schaltungen am besten geeignet sind.

Vereinheitlichung der Tests zur Latch-up-Festigkeit von HCMOS Logik-ICs

Der Latch-up-Effekt bezeichnet das Thyristor-Verhalten, das alle konventionellen CMOS Logik-Schaltungen aufweisen. In der HCMOS-Logikreihe (74HC/HCU/HCT . . .) wurde der Latch-up-Effekt vollständig beseitigt, indem man auf das n^--Substrat eine hochohmige epitaktische Schicht aufwachsen liess, um einen lateralen Stromfluss durch das Substrat zu verhindern. Diese Massnahme, in Verbindung mit eigens entwickelten Design-Regeln und Prozessparametern, bedeutet, dass die ICs der HCMOS-Reihe vollkommen frei von Latch-up-Effekten sind. Dieser Beitrag diskutiert die Methoden zur Beseitigung von Latch-up-Effekten und beschreibt vier Tests zur effektiven Berechnung der Eingangs/Ausgangsströme und der Versorgungsüberspannung, die zum Auslösen des Latch-up-Effekts nötig ist.

Applications de la HCMOS en trigger de Schmitt

En théorie, le gain élevé des éléments logiques intégrés se traduit pas une impulsion de sortie rectangulaire, quels que soient les temps de montée et de descente du signal d'entrée. Toutefois, les signaux d'entrée à fronts lents peuvent entraîner la fluctuation parasite des impulsions de sortie et accroître la consommation de courant. La famille logique CMOS à grande vitesse 74HC/HCT comporte deux circuits à deux entrées trigger de Schmitt pour éviter ces inconvénients. L'article décrit comment ces deux circuits intégrés peuvent être utilisés pour résoudre de nombreux problèmes de formes d'ondes, et pour réaliser des oscillateurs RC ne nécessitant que deux broches pour les lignes de signal.

Remplacement des lignes de transmission de commande et de la TTL-LS par les circuits intégrés HCMOS 74HCT

Avant l'introduction de notre famille HCMOS de circuits intégrés logiques, les concepteurs de systèmes logiques à grande vitesse étaient limités à l'utilisation de circuits intégrés bipolaires grands consommateurs de courant, tels que la TTL-LS. Les circuits intégrés logiques HCMOS sont aussi rapides que la TTL-LS avec une consommation en courant moindre, et ils peuvent fonctionner sur une plage de tension d'alimentation considérablement plus grande. Leur utilisation à la place des TTL-LS aboutit à des économies de systèmes considérables. Les circuits intégrés HCMOS portant le préfixe 74HCT sont conçus spécialement pour remplacer les TTL-LS ou pour l'utilisation dans des systèmes à technologie mixte. Cet article compare les structures entrée/sortie et les performances des TTL-LS, et des circuits intégrés logiques 74HCT. Il présente les méthodes d'interface et les techniques à basse puissance permettant de commander des lignes de transmission de données à l'aide des circuits intégrés 74HCT.

Protection des circuits intégrés logiques HCMOS dans les automobiles

Soumis aux rigueurs climatiques et aux fluctuations électriques, les équipements électroniques fonctionnent difficilement de façon fiable dans un véhicle, tout au long de la durée de vie de celui-ci. En outre, de nombreux électroniciens ne connaissent pas bien les véritables conditions régnant autour du moteur et dans l'habitable. Cet article décrit l'environnement dans un véhicle et explique comment protéger les circuits intégrés logiques HCMOS, afin que leurs caractéristiques remarquables puissent être pleinement exploitées dans les applications automobiles.

Modification des programmes de tests TTL-LS pour la logique HCMOS

Les fabricants qui passent de la logique TTL-LS à la logique HCMOS auront besoin de modifier leurs bancs d'essai en conséquence. Le présent article décrit la façon de modifier les matériels et logiciels d'essai pour les tests HCMOS, pour un investissement minimal en coût et en temps. L'article compare les caractéristiques et fournit des directives concernant les paramètres d'essai supplémentaires nécessaires aux tests HCMOS, tout en abordant les tests TTL-LS, qui peuvent être omis. Cet article décrit également en détail la modification du système classique Teradyne J283 pour les tests HCMOS.

Alimentation de secours par piles pour les circuits intégrés logiques HCMOS

Du fait de leur très faible consommation de courant au repos et des temps de transition rapides, les circuits intégrés logiques HCMOS peuvent aisément être dotés d'une alimentation de secours par piles pour palier à tout défaut de l'alimentation normale. Toutefois, en cas d'emploi prolongé sur piles, il convient de suivre quelques recommandations fort simples, afin de réduire encore la consommation de courant et assurer aux piles une durée de vie maximale. Cet article décrit ces recommandations, donne quelques circuits pratiques pour réaliser une alimentation de secours par piles, et présente les différents types de piles les mieux adaptés aux circuits HCMOS.

Normalisation des tests d'immunité au blocage pour les circuits intégrés CMOS à grande vitesse

Le latch-up provient du fonctionnement thyristor que subissent tous les circuits intégrés logiques CMOS classiques. Dans la famille 74HC/HCU/HCT des circuits intégrés logiques HCMOS, le latch-up a été totalement éliminé par l'implantation d'une couche épitaxiale à forte résistivité sur le substrat N, afin que celui-ci ne soit pas traversé par un flux de courant latéral. Compte tenu également des règles de conception et des paramètres du procédé, ceci signifie que les circuits intégrés 74HC/HCU/HCT sont entièrement insensibles au latch-up. Cet article présente les méthodes de suppression du latch-up et décrit quatre tests où l'on peut évaluer efficacement les courants d'entrée/sortie et la surtension d'alimentation propres à engendrer le latch-up.

Aplicaciones del disparador de Schmitt HCMOS

En teoría, la elevada ganancia de los elementos lógicos integrados producen impulsos de salida rectangulares independiéntemente de los tiempos de subida y bajada de la señal de entrada. No obstante, las señales de entrada de flancos lentos pueden hacer que los impulsos de salida trepiden y que aumente el consumo. La gama de circuitos lógicos CMOS de gran velocidad 74HC/HCT incluye dos circuitos integrados con entradas de disparador de Schmitt para superar estos problemas. Este artículo describe como se pueden emplear los mencionados circuitos integrados para solucionar todo tipo de dificultades de formas de onda y para construir osciladores RC que sólo necesitan utilizar dos terminales para las líneas de señal.

Uso de los circuitos integrados HCMOS 74HCT para sustituir a los LSTTL y excitar lineas de transmisión

Con anterioridad a la introducción de nuestra gama de circuitos integrados lógicos de estructura HCMOS, los diseñadores de sistemas lógicos de gran velocidad se limitaban a emplear circuitos integrados bipolares de gran consumo energético, como los LSTTL. Como los circuitos HCMOS funcionan con igual velocidad que los LSTTL, pero consumen por término medio menos energía, a la vez que pueden trabajar en un margen más amplio de tensiones de alimentación, su empleo se traduce en un ahorro considerable. Los circuitos integrados HCMOS que llevan el prefijo 74HCT están diseñados especificamente para substituir a los LSTTL, o para su empleo en técnicas mixtas. En este artículo se comparan las estructuras de E/S y el rendimiento de los LSTTL y de los circuitos integrados lógicos 74HCT, tratándose las técnicas de conexión y de baja potencia para excitar líneas de transmisión de datos terminadas con circuitos integrados 74HCT.

Protección de los circuitos integrados logicos HCMOS en el automovil

Las adversas condiciones climáticas y eléctricas de los vehículos motorizados dificultan el functionamiento normal de los dispositivos electrónicos durante toda la vida útil del vehículo. Por si fuera poco, son muchos los ingenieros electrónicos que desconocen la auténtica naturaleza de las condiciones que prevalecen en el compartimiento del motor y en el de los pasajeros. En este artículo se describen detenídamente las susodichas condiciones y se explican los métodos para la protección de estos circuitos, de modo que se aprovechen plenamente sus extraordinarias propiedades en aplicaciones electrónicas del automóvil.

Modificacion de los programas de prueba de los LSTTL para probar los circuitos integrados logicos HCMOS

Los fabricantes que cambien de LSTTL a HCMOS deberán transformar consecuéntemente sus instalaciones de prueba. Este artículo describe a rasgos generales las modificaciones pertinentes de los programas y de la circuiteria existentes para probar los HCMOS invirtiendo un mínimo de tiempo y dinero. Se comparan las características y se dan las directrices para los parámetros adicionales de prueba de los HCMOS, que pueden omitirse para las pruebas de los LSTTL. También revisa minuciosamente el método de modificación del famoso sistema Teradyne J283 para probar los HCMOS.

Pilas de reserva para circuitos integrados logicos HCMOS

El reducido consumo en reposo y la rapidez de transición de estos circuitos facilitan la adición de pilas de reserva para casos de falla de la alimentación normal. Sin embargo, para periodos largos de funcionamiento con pilas, deben seguirse varias reglas sencillas para reducir el consumo al mínimo y garantizar la máxima duración de la pila. Este artículo describe dichas reglas, presenta varios circuitos prácticos para la instalación de las pilas de reserva y hace una revisión de los tipos de pila más adecuados para su empleo con HCMOS.

Normalización de los ensayos de antibloqueo de los circuitos integrados lógicos CMOS de gran velocidad

Bloqueo es el efecto de tiristor que experimentan todos los circuitos integrados lógicos de estructura CMOS convencional. En la gama 74HC/HCU/HCT de circuitos integrados lógicos de estructura HCMOS, el bloqueo se ha eliminado completamente al añadir una capa epitaxial de gran resistividad al material de base "n" para evitar el paso de las corrientes laterales por dicho material, lo cual, unido a las reglas de diseño exclusivas y a los paràmetres de proceso, eliminan totalmente el bloqueo de los circuitos integrados 74HC/HCU/HCT. Este artículo trata dichos métodos y describe cuatro ensayos para la evaluación eficaz de las corrientes de entrada y salida y de la sobretensión de alimentación que son necesarias para provocar el bloqueo.

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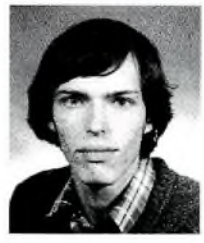

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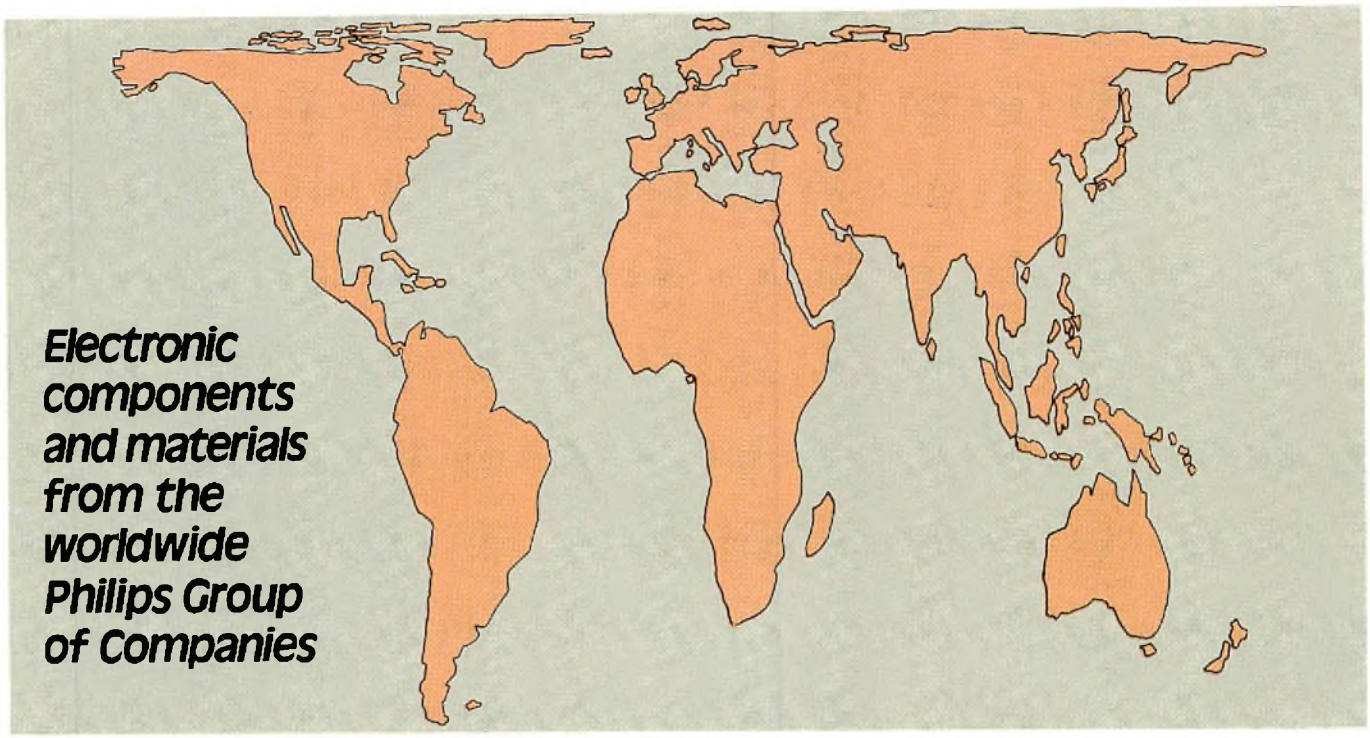

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