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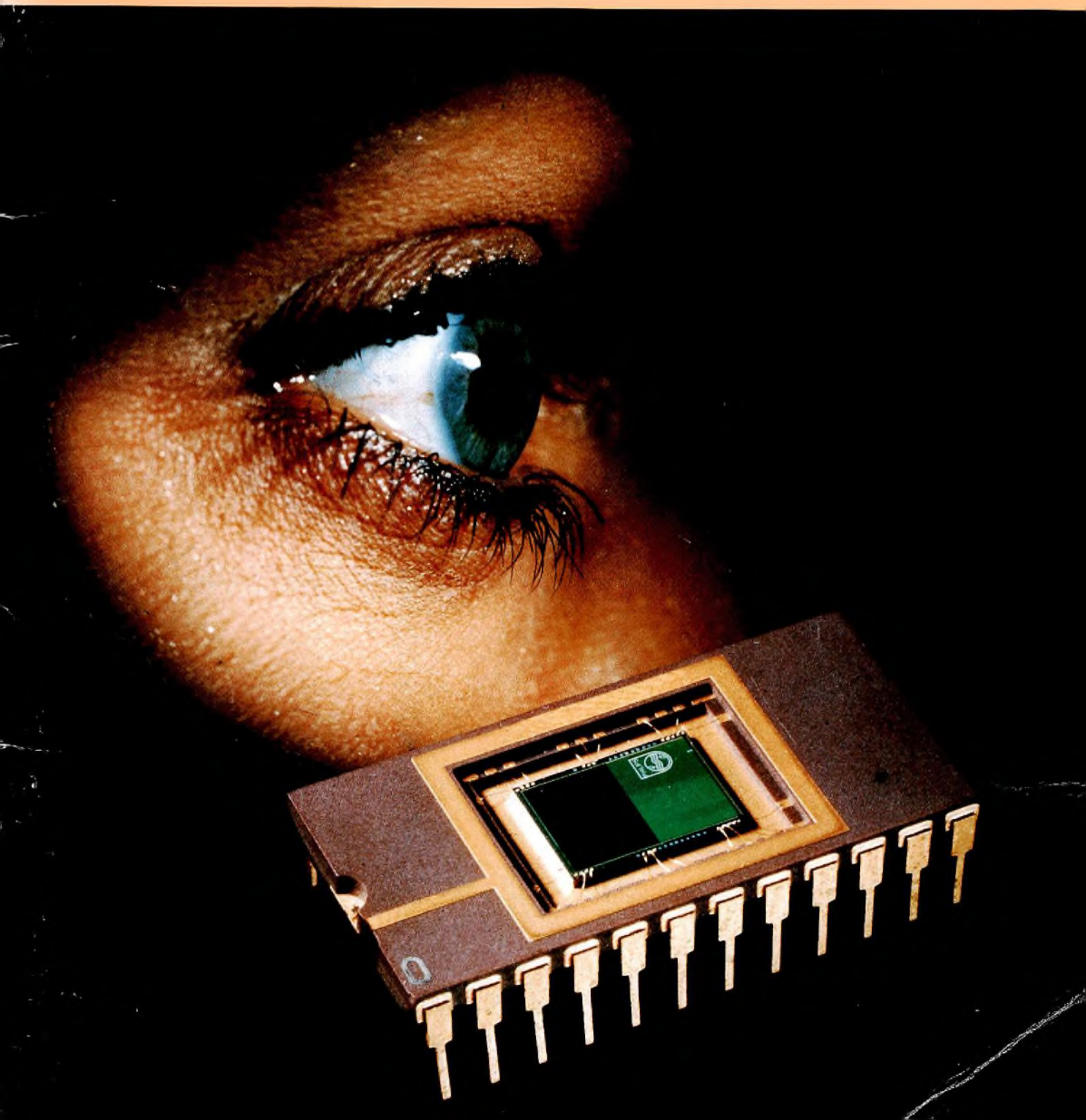

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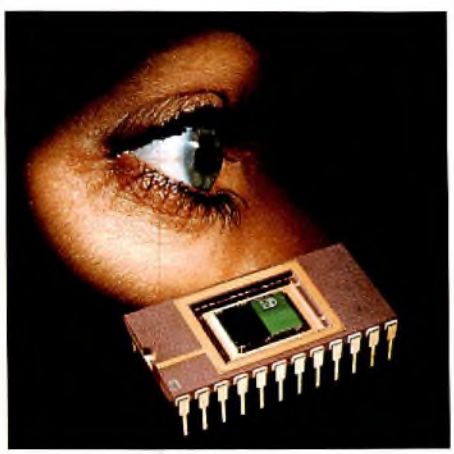


Not so long ago the solid-state imager was regarded as little more than a curiosity, something for the research labs to play with, but no real competition for the tv camera tube. In just a few short years, however, those early imagers have grown into something really big. Already we find two-dimensional imagers, such the NXA1010/1020 frame-transfer sensors featured in this issue, replacing vidicons in CCTV and home video systems, and it won't be long before they hit the broadcasting market in the latest ENG tv cameras. But their real future lies in areas where camera tubes have hardly penetrated, such as character-recognition systems and home security systems, and in the more distant future, videophones, robot-vision systems and electronic still-picture cameras. With such a bright future, the solid-state imager is certainly worth keeping an eye on.

Contents

Disk controller supports both rigid and floppy drives

GUY THOMSEN

Many designers are developing systems that use hard disks for on-line mass storage and some other medium to back up the disks. Because it's compact, portable and inexpensive, the floppy disk has been a popular back-up choice, but until now, its use has meant that you had to develop two separate controllers – one for each drive type.

Using a new 2-chip set, however, you can design a single controller to service both rigid and floppy disks. The two ICs are the SCN68454, an intelligent multiple-disk controller (IMDC), and the SCB68459, a phase-locked loop for the disk drives (DPLL). You can use the pair of chips to control as many as four rigid or floppy disks in any combination. The ICs can work with any drive that has a Shugart SA850, SA1000 or Seagate ST506 interface. (For more details on the controller and phase-locked loop, see panel).

If you want to employ these chips, though, the controller will affect your overall system design, especially its memory usage and the software drivers that control data transfers. On the other hand, adding the hardware to your system is an easy process, and once you understand the hardware, the controller's operation and its effect on your software becomes clear. So it's best to begin with a hardware implementation that can serve as a model for understanding the controller's unique way of operating.

SIMPLE CONTROLLER HARDWARE

The use of the IMDC and DPLL hardware in the design of a controller is rather straightforward. As Fig.1 shows, you need only a few ICs – some octal buffers, an address decoder, a multiplexer, and a couple of delay lines and voltage-controlled oscillators (VCOs) – in addition to the IMDC and two DPLLs. With conventional ICs, you'd need more than 90 devices to provide the same features found in the IMDC/DPLL-implemented design.

The controller's interface to the 68000-based host system's bus consists of five octal buffers: three 74LS373s for address and function codes and two 74LS245s for data. Address lines A_1 and A_2 and all other control lines can be tied directly to the system bus. Once the host has activated the IMDC by sending the IMDC's address to the address decoder (which activates the IMDC's chip-select ($\overline{CS}$) line), lines A_1 and A_2 directly address the IMDC's internal registers.

Tied to the controller side of these five buffers is a 16-bit bus, called the local bus, which is controlled by the IMDC. When the IMDC wants to send an address to the host, it first puts the high-order addresses A_{19} to A_{23} and function codes FC_0 to FC_2 on bus lines D_8 to D_{15} and asserts the upper address strobe (UAS). IC_5 retains the data after UAS returns LOW.

Next, the IMDC puts the lower-order address codes A_3 to A_{18} on the bus and asserts the lower address strobe (LAS). When LAS is driven LOW, IC_3 and IC_4 retain the address. Finally, the IMDC puts the remaining address bits on lines A_1 and A_2 and sends the address through a normal 68000-bus cycle using the address strobe, $\overline{AS}$, and the data strobes, $\overline{UDS}$ and $\overline{LDS}$. If during a consecutive addressing operation, the higher-order address lines remain unchanged, the IMDC doesn't reload the upper address lines.

The local bus also transfers data to and from the host system. When the IMDC uses DMA to read data from host memory, for example, it first latches that data into IC_1 and IC_2; the state of the data-direction (DDIR) line determines which port of these bidirectional buffers will accept the data for buffering, and the LOCAL line enables the buffers.

Then, using the local bus, the IMDC moves the data to temporary storage in its 128 byte first-in, first-out (FIFO) buffer before transferring the data to a disk. A write operation is just the opposite: data from the disk is sent to the FIFO, then to the bidirectional buffers, and then to the host memory.

The local bus also carries control information between the IMDC and the disk units. With EN_0 HIGH, data is latched into IC_6 and IC_7. With EN_1 LOW, buffer IC_8 passes information back to the IMDC.

Data is written to or read from a drive by means of the DPLL. In Fig.1, two DPLLs are used: one for a slow read/write data path (floppy-disk drive), and the other for a fast read/write data path (rigid-disk drive). The example uses two parts because different drives can require different read-data rates and associated voltage-controlled-oscillator

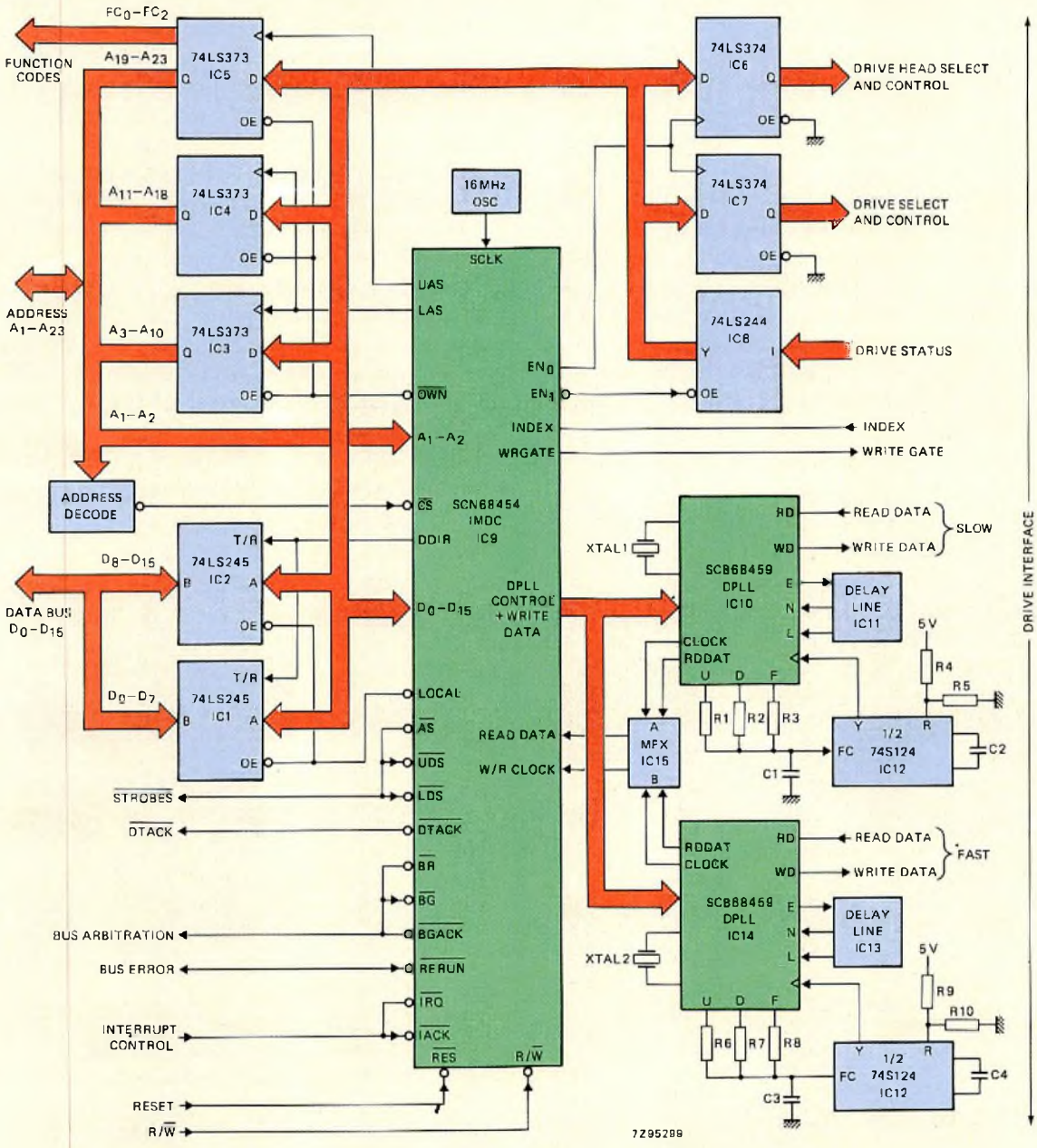


Fig.1 This 2-drive controller uses few ICs because its controller chip set is made up of an Intelligent Multiple Disk Controller (IMDC) and two Disk Phase-Locked Loop (DPLL) ICs

(VCO) timing, and because the two write clocks require different crystals. If the data rates for both types of drive attached to the IMDC were the same, then the circuit would only require one DPLL. In any case, you only require one IMDC to control four disk units.

In this case, each DPLL uses a separate VCO, ½ of a 74S124. You attach the VCO to the DPLL via three resistors and a capacitor. The resistors attach to the pump-up, pump-down and frequency-pump pins of the DPLL. The voltages that the DPLL pumps across these resistors are summed by the capacitor. The sum point of the four passive devices attaches to the VCO's frequency-control pin.

In addition to the four passive devices used for frequency control, passive elements control other VCO parameters. Two resistors (you could use one trim pot instead) set the frequency range, and a capacitor sets the range's centre frequency.

The final part that the DPLL requires is the crystal. This crystal must have a frequency that is twice the data rate of the disk drive or drives attached to the DPLL. The DPLL function requires only three ICs and eight passive components. Many other designs would require amplifiers and a lot of components to accompish the same function.

You need the multiplexer, IC_{15}, when you incorporate two or more DPLLs into a design. IC_{15} selects the Read Data and Read/Write Clock from the DPLL for the drive chosen. The other control signals can go directly to each DPLL.

INITIALIZATION

Before the IMDC performs any operation, three areas must be initialized: one in the controller and two in the host system. These areas are the IMDC's internal registers and two special areas of the host memory – the event control area (ECA) blocks and the ECA pointer table. These three areas are critical to the controller's unique way of performing. By writing to the IMDC's registers, the host system tells the controller what operations to perform, and by looking at the ECA pointer table and the ECA blocks, the IMDC knows how to perform them.

There are seven addressable registers in the IMDC (Fig.2). To initialize them, the host must load the first four registers – the ECA registers – with the address of the ECA pointer table. It then loads the fifth register – the Interrupt Vector register – with the vector-priority number assigned to the IMDC. The last two registers are initialized just prior to actual operation; before initializing them, the ECA pointer table and the ECAs themselves must be initialized.

The ECA pointer table contains the addresses of the ECA blocks, there can be as many as four – one for each of four drives. The block addresses are arranged by drive number in ascending order. The ECA block addresses need not be contiguous; the only requirement is that the IMDC should be able to address them.

The ECA blocks must also be initialized. That is, each block must contain the drive parameters that the IMDC

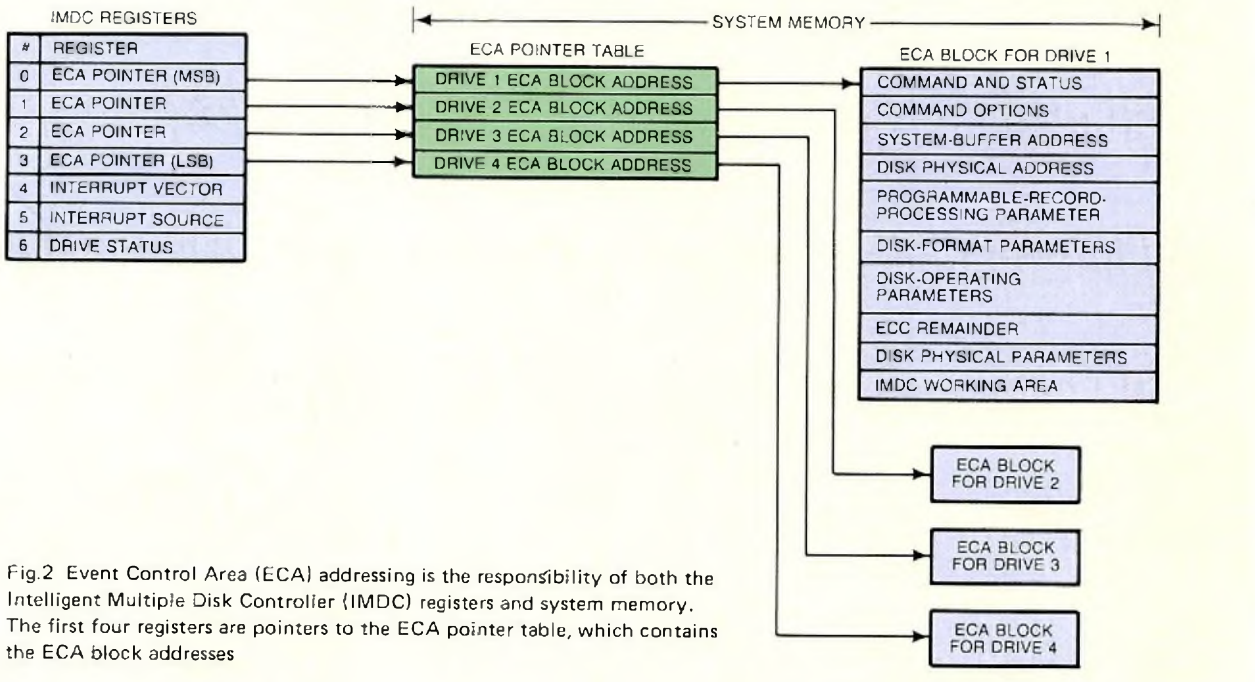


Fig.2 Event Control Area (ECA) addressing is the responsibility of both the Intelligent Multiple Disk Controller (IMDC) registers and system memory. The first four registers are pointers to the ECA pointer table, which contains the ECA block addresses

needs in order to determine whether the drive is rigid or floppy. Normally, once you set up these areas, you shouldn't need to change them.

While there is normally a separate ECA block for each drive, you can use an ECA block for more than one disk unit if you take proper care. If there are common parameters in ECA blocks, save those parameters separately from the unique parameters that are associated with a particular disk's physical address. After you access the unique parameters, branch to the common parameters.

Within the ECA block, eleven IMDC commands provide read and write data transfers (Table 1). Status gets updated at the completion of each requested operation. The status consists of two areas: a main status and an extended status. For each command completion, it is necessary to check only the main status to determine whether an error is posted. If there is no error, the extended status provides additional information about the operation.

The System Buffer Address and Disk Physical Address define where to transfer data from and to during a read or write. The remainder of the ECA block defines special parameters for each command and drive type. The IMDC uses these bytes to determine whether the disk unit is rigid or floppy, and the extent of storage capabilities. Included are the parameters that define step rate, head load time (if required) and other physical features.

In the IMDC, there are only two registers that the system software uses during disk operations: the Interrupt Source and Drive Status registers. To request an IMDC operation, the host software must set one of four bits in the Drive Status register. Each bit corresponds to one of the four drives. Setting a bit flags the IMDC to use the ECA pointer register plus an appropriate offset to get the ECA block address. The IMDC then uses this address to obtain the what, where and how for the current request.

TABLE 1
IMDC commands

command mnemonics	HEX code	description
WRMS	00	write multiple sector
WRDD	01	write with deleted data flag
VER	10	verify sector data
REMS	11	read multiple sector
PRP	12	programmable record processing
TSR	13	transparent sector read
RETD	20	read identifier
FORM	40	format track
CALB	41	recalibrate to track zero
CORR	81	correct data with ECC remainder
DIAG	80	diagnostic

When the IMDC completes the posted command, it sets the appropriate bit in the Interrupt Status register and asserts the interrupt line to the host processor. The system software then reads the ECA status to determine proper command completion, and the cycle continues as necessary. You can set each of the bits in the Drive Status register independently of the others. Resetting a bit before an operation is complete aborts the request and sets an interrupt. Figure 3 shows a sample flowchart. Figure 4 contains an interrupt service routine for the IMDC written in 68000 microprocessor assembly language.

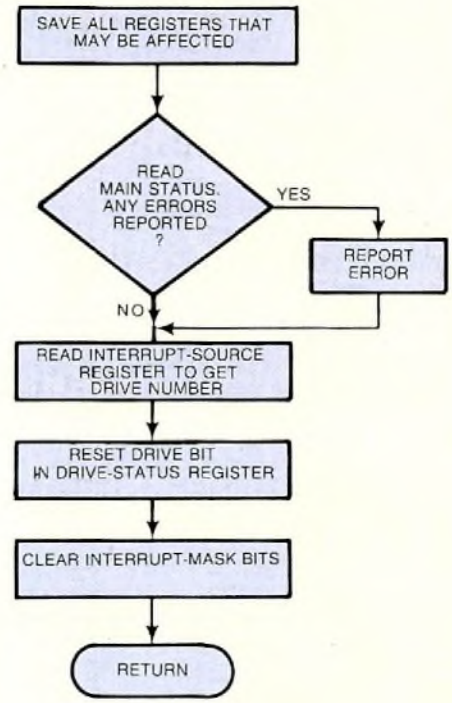


Fig.3 This flowchart contains all the interrupt handling for a simple disk-controller system

```
;*****************************************************************
;                INTERRUPT SERVICE ROUTINE FOR IMDC              *
;*****************************************************************
;
IMDC.INTR   MOVE.L   D0,-(SP)          ;SAVE REGISTER
            MOVE.B   MAIN.STATUS,D0    ;GET MAIN STATUS BITS
            BEQ.S    INTR.CONT         ;SKIP ERROR REPORT IF OK
;
            BSR.L    ERROR.REPORT      ;GO TO ERROR REPORTING ROUTINE
;
INTR.CONT   MOVE.B   INTR.SOURCE,D0    ;GET THE FINISHED DRIVE NUMBER
            EOR.B    D0,DRIVE.STATUS   ;CLEAR DRIVE-BUSY BIT
;
            MOVE     SR,D0             ;GET 68000 STATUS BITS
            AND.W    #INTR.MASK,D0     ;CLEAR INTERRUPT-MASK BITS
            MOVE     D0,SR             ;RETURN STATUS BITS TO 68000
;
            MOVE.L   (SP)+,D0          ;RETURN SAVED REGISTER
;
            RTR                        ;RETURN FROM INTERRUPT
```

Fig.4 This interrupt service routine for the Intelligent Multiple Disk Controller is written in 68000 assembly-language code

A CLOSER LOOK AT THE CHIP SET

The SCN68454 Intelligent Multiple-Disk Controller (IMDC) illustrated in Fig.A is a microprogrammed disk-control subsystem that employs a memory-to-memory architecture. Bus compatible with the 68000 microprocessor family and its vectored interrupt structure, the IMDC has 31 address lines for the DMA transfer, a 128-byte first-in, first-out (FIFO) buffer, a 31-bit address counter and user-specified data transfers of either 8 or 16 bits to the host data bus. Housed in a standard 48-pin DIP, the IMDC needs only a single 5 V power supply.

The IMDC is the interface to both the host system and the disk units. The IMDC and host system use the IMDC's seven internal registers for communication about the task to be performed. After the IMDC accepts a command from the host, an on-chip direct-memory-access (DMA) controller takes charge of all transfers between system memory and IMDC. The IMDC uses its on-chip FIFO buffer to provide temporary storage during data transfers.

The IMDC's disk-interface section contains the read and write logic, the serial/deserial register, the error check and correction (ECC) register, and the disk input/output (I/O) control logic. The table shows the input and output lines.

Complementing the IMDC is the SCB68459 Disk Phase-Locked Loop (DPLL), a 20-pin bipolar IC. Like the IMDC, it requires only a single 5 V power supply. The block diagram (Fig.B) shows the DPLL's internal architecture.

The DPLL uses an external voltage-controlled oscillator to provide a variable clock rate to track the read data from the disk unit. The on-board crystal oscillator also generates the write clock. The DPLL operates with a composite data rate of 100 kHz to 10 MHz for precision management of the bit stream flowing between the disk drive(s) and the host system. Precompensation logic is built into the chip; designers can use this precompensation to write-compensate the modified-frequency-modulation (MFM) data to the disk unit.

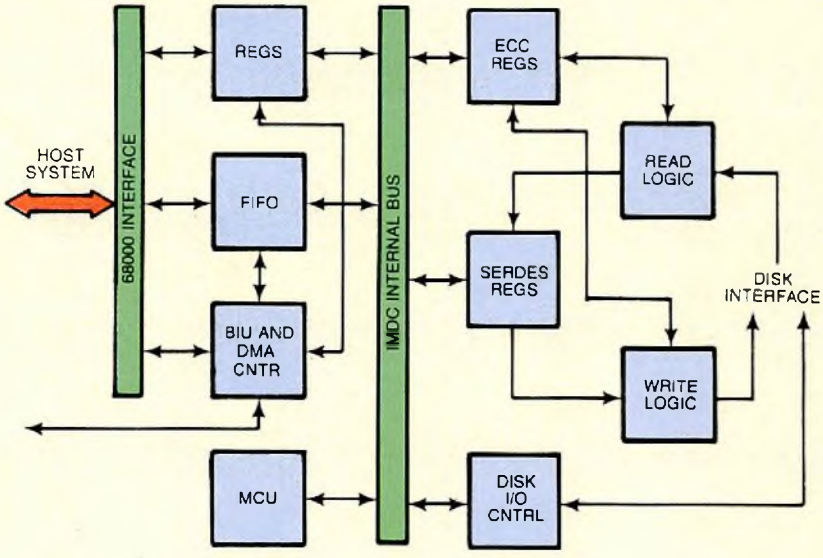
However, the devices are not limited in scope to use with the 68000 microprocessor family. Designers can integrate the IMDC and DPLL for use with any microprocessor architecture that employs either an 8- or 16-bit data bus. In any system design, expect a relatively low component count. The 2-chip set integrates the equivalent functions of 90 or more ICs. Because of this high level of integration, the chips reduce PC-board space by as much as 90%. Correspondingly, manufacturing costs are reduced and reliability increased.

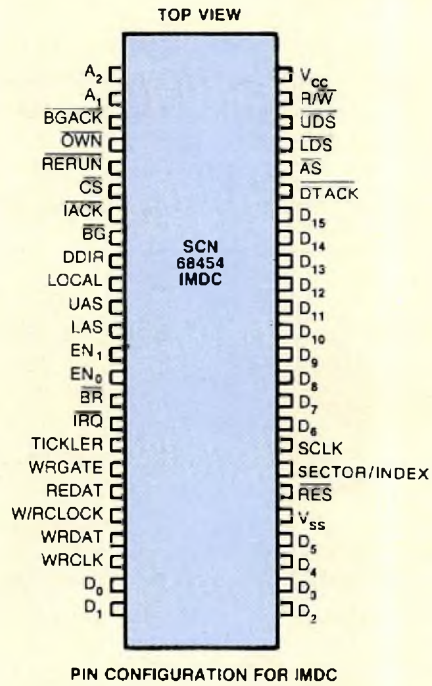
The ability to detect and correct data errors is an important feature of any disk controller. The IMDC and DPLL support multiple-sector read/write with implied seek and automatic bad-sector handling. The IMDC can correct data errors by using either 32- or 40-bit user-specified ECC polynomials or with the CRC-CCITT (cyclic redundancy check) polynomial.

One powerful IMDC feature is real-time record processing, which allows the user to specify the search criteria on a character-by-character basis and to specify the action that is to occur on completion of the search.

The IMDC supports the IBM 3740 and System 34 media formats as well as soft- or hard-sector formats. The device handles both frequency-modulation (FM) and modified-frequency-modulation (MFM) data formats with data rates as high as 2 million bits/sec for FM and 10 million bits/sec for MFM-regardless of the host processor's operating speed.

The introductory version of the chip set controls as many as four rigid and/or floppy drives. At present, these drives must have Shugart SA850, SA1000 or Seagate ST560 standard interfaces. Future changes in the IMDC's mask-programmable microcode will let you use the chip with other interfaces, such as ESDI, ANSI and SMD.





PIN CONFIGURATION FOR IMDC

Fig.A The Intelligent Multiple Disk Controller provides an interface between the host system and the disk units

PORT DEFINITIONS

input			output	
bus line	signal name	definition	signal name	definition
D0	INDEX	rigid-disk index signal	HEAD1	head select 2^0
D1	READY	disk ready	HEAD2	head select 2^1
D2	SEEKC	seek complete	HEAD4	head select 2^2
D3	TR0A	track-zero first signal	HEAD8	head select 2^3
D4	TR1A	track-zero second signal	HEAD16	head select 2^4
D5	WFA	floppy write-protect	not used	
D6	WFB	write fault	STEP	head step pulse
D7	not used		DIR	direction of head
D8	not used		LWC	low write current
D9	not used		MOT	motor on
D10	not used		PRECOM	precompensation enable
D11	not used		HDL	head load for floppies
D12	not used		SEL0	drive 0 select
D13	not used		SEL1	drive 1 select
D14	not used		SEL2	drive 2 select
D15	not used		SEL3	drive 3 select

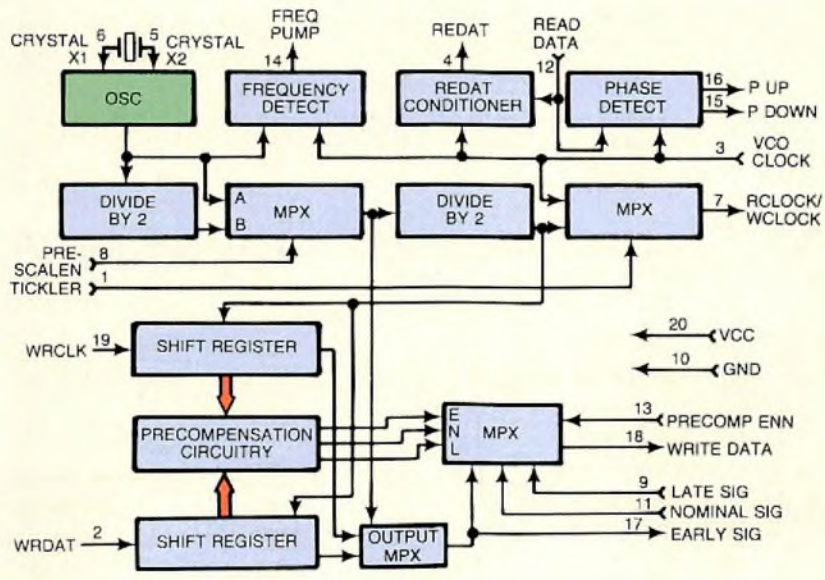


Fig.8 The Disk Phase-Locked Loop (DPLL) uses an external voltage-controlled oscillator for the variable clock rate which tracks the read data from the disk unit

FORMATTING DIFFERENT DRIVE TYPES

The IMDC lets you format disks to several different standards. The device supports both the IBM single-density (IBM 3740) and double-density (IBM System 34) formats, and it can format both hard- and soft-sectored disks. The user can also specify either a 1- or 2-byte cylinder field within the sector header. This accommodates the next generation of rigid disk units which may have more than 256 cylinders.

Each of the format options has a fixed number of bytes that are repeated within each sector; the IMDC automatically writes those bytes. The IMDC fetches from a table in memory the bytes that vary, such as the cylinder number, head and sector number. The System Buffer Address in the ECA table points to this table.

For each sector on each track of a floppy disk, the software driver first puts into ECA memory the cylinder number, side, sector number and record length. Using DMAs, the IMDC then puts the information into the FIFOs during the format operation. Because the user places the information into the ECA, he or she can specify the sector mapping on the track. This can take place in any order the user wants, and it links together as many consecutive sectors as the system software requires. The IMDC can read consecutively numbered sectors over the total track length.

The information for a rigid-disk format is the same as for the floppy-disk format, except that there is no sector length placed in the sector header. With a rigid disk, formatting takes place one track at a time. This allows the user to perform other disk operations without waiting for the whole disk to be formatted. For some drives, the formatting time is several minutes.

HANDLING BAD SECTORS

The IMDC provides the user with a bad-sector feature. If, after formatting a track, tests show that an area has an unreliable sector, the IMDC provides a bad-sector flag, along with an alternative physical address. During a read or write to that sector, the IMDC finds the flag, reads the alternative sector address and goes to that sector. The IMDC then moves the drive head to that sector, performs a seek operation (if one is required by a read-operation), and completes the transfer operation to that location in the normal way. The IMDC then returns to the track with the bad sector and continues the read operation at the next sector.

The IMDC's ability to select alternative sectors is especially useful during multiple-sector data transfers, the user is not aware of any interruptions in the actual data transfer. It also relieves the system software of the responsibility of maintaining an alternative-sector map on the disk and performing the extra operations required during the data transfers.

An unusual feature built into the disk controller is its ability to search for a character string and then perform an operation. With this feature (the Programmable Record Processing (PRP) command), you can instruct the IMDC to locate a specific string of characters within a logical data block on a disk. After the match, the IMDC can read the logical data block, process a pointer within the data block or locate all blocks that satisfy some search criteria.

You specify the PRP functions by filling the Scan Control Word Table (SCWT) with the string and instruction parameters. The SCWT is part of the system memory, and its address is placed into the ECA table in the PRP parameters area. Each word of the SCWT consists of two parts, one data and the other an instruction; each part is eight bits long. The IMDC divides the FIFO memory into two parts for the PRP command; one part is dedicated to the character string and instructions, and the other is to be used during the disk data transfers. The FIFO memory receives the PRP commands and character string before the operation begins.

The physical sector address and a byte-count offset specify the start of the first byte to be scanned. You can specify the end of the record for which you are looking in terms of either a fixed record length or an end-of-record character.

You can transfer either the records for which you are searching or their locations to the system memory. In either case, you begin by reading records on the disk sequentially. When a record meets the search criteria, you can either immediately transfer the record's data into the system memory, or you can tell the IMDC to log the location of the record match and return the logged location to system memory.

You can write a software driver for the IMDC in two levels: entry level – for cold-start (power-on) entry to the drives, or normal level – for access to the drives during normal operation. Both levels can be part of the same driver, with flags and tests to route the program to the correct procedures.

As previously noted, the IMDC registers, ECA pointer table and ECA blocks must be initialized before any operation is performed. At power up, a typical operating system would put into the ECA pointer table the address of each ECA block and fill the ECA block with the parameters that define the disk types. Although these parameters would not usually change during normal operation, a diagnostic routine might call for such a change. Table 2 shows the ECA block parameters used by each command.

During successive disk operations, the parameters most likely to change from one operation to the other, are the Command Code, Buffer Address and the Physical Disk Address (cylinder, head and sector), which define the

nature, location and quantity of the requested transfer. Therefore, the operating system should, at least, pass these parameters to the normal-level software driver. In some cases, the buffer length will differ from the sector length, so it, too, should be updated with each command. For example, a read (REMS) operation without any data transfer becomes a seek command.

The last thing the driver must know is what drive to activate. This unit's number becomes the busy bit set in register 7 of the IMDC, reflecting the fact that it is the selected drive. As it is possible to request more than one operation at a time, the driver must be sure that it does not permit a previously requested drive's bit to be overwritten.

TABLE 2
ECA parameters used by each command

	command mnemonics										
ECA parameter used	WRMS	WRDD	VER	REMS	PRP	TSR	RETD	FORM	CALB	CORR	DIAG
COMMAND CODE	•	•	•	•	•	•	•	•	•	•	•
STATUS BYTES	•	•	•	•	•	•	•	•	•	•	•
MAX NUMBER OF RETRIES	•	•	•	•	•	•	•	•	•		
DMA COUNT	•	•	•	•	•	•	•	•		•	
COMMAND OPTIONS	•	•	•	•	•	•	•	•		•	
BUFFER ADDRESS	•	•	•	•	•	•	•	•		•	
BUFFER LENGTH REQUEST	•	•	•	•	•	•	•	•		•	
CYLINDER NUMBER	•	•	•	•	•	•	•	•	•		
HEAD NUMBER	•	•	•	•	•	•	•	•			
SECTOR NUMBER	•	•	•	•	•	•					
PRP COMMAND CONTROL WORD					•						
PRP PARAMETERS					•						
N0 – PRE INDEX GAP								•			
N1 – POST INDEX GAP								•			
N2 – SYNC BYTE COUNT	•	•						•			
N3 – POST-ID GAP	•	•						•			
N4 – POST-DATA GAP								•			
N5 – ADDRESS MARK CONTROL	•	•	•	•	•	•	•	•			
ECC MASK	•	•	•	•	•	•	•	•		•	
MOTOR-ON DELAY	F	F	F	F	F	F	F	F	F		
NUMBER OF HEADS	•	•	•	•	•	•	•	•			
ENDING SECTOR NUMBER	•	•	•	•	•	•	•	•			
STEPPING RATE	•	•	•	•	•	•	•	•	•		
HEAD SETTLING TIME	•	•	•	•	•	•	•	•	•		
HEAD LOAD TIME	F	F	F	F	F	F	F	F			
SEEK TYPE	•	•	•	•	•	•	•	•	•		
LOW WRITE CURRENT BOUNDARY TRACK	•	•	•	•	•	•	•	•			
PRECOMP BOUNDARY TRACK	•	•	•	•	•	•	•	•			
MAX NUMBER CYLINDERS/TRACKS	•	•	•	•	•	•	•	•			
SECTOR LENGTH/LAST SECTOR NUMBER	•	•	•	•	•	•	•	•			
FLAG BYTE			•	•		•	•				
B-TREE POINTER					•						

F = floppy only.

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Liquid-crystal displays for automotive applications

E. LOWARD and P. STREIT

The LCD is no stranger to the car dashboard. These days you'll find it in displays for the clock, for the radio and for the trip computer (Figs.1 to 3), as well as for many other auxiliary functions that are rapidly becoming regarded as essential features of the modern car. You don't have to look far to find the reasons for this current popularity. Low operating voltage and power consumption are probably the principal ones, and you can also add its small size, low cost and outstanding design flexibility, all of which make it extremely attractive to the dashboard designer. And provided some simple operating rules are adhered to, legibility is extremely good. Finally, there's its straightforward drive circuitry which is fully compatible with the digital output signals generated by the auxiliary functions within the dashboard.

At present, small displays for auxiliary functions in the car are generally designed for positive contrast viewing mode, i.e. with black segments on a bright background. These are mounted so that they can operate by reflection during bright daylight, and they have rear illumination (operating in what's known as the transflective mode) or indirect front lighting for low-light-level and night-time viewing.

A car cockpit, however, is a rather special environment in which both ergonomics and styling play important roles (Fig.4). In the latter respect, there's little doubt that current styling is strongly influenced by the conventional 'mechanical' dashboard, so to gain acceptance, a modern 'electronic' dashboard must exhibit its information with bright, partly-coloured symbols on a dark background. For the LCD this means operating in what's known as the transmissive mode in reverse contrast with permanent backlighting and intermediate colour filters. We'll refer to this mode as the 'quasi-active' mode since it leads to an appearance directly comparable to that of active displays like the LED, VFD (vacuum fluorescent display) or ELD (electro-luminiscent display).

Fig.1 Philips car radio model AC930 with Videlec LCD

Fig.2 Trip computer (Bosch) with Videlec LCD (Opel)

Fig.3 Clock module (Borg) with Videlec LCD (BMW4 series)

Fig.4 Display module from RT-Philips for radio/clock/temperature (Renault R25) with Videlec LCD

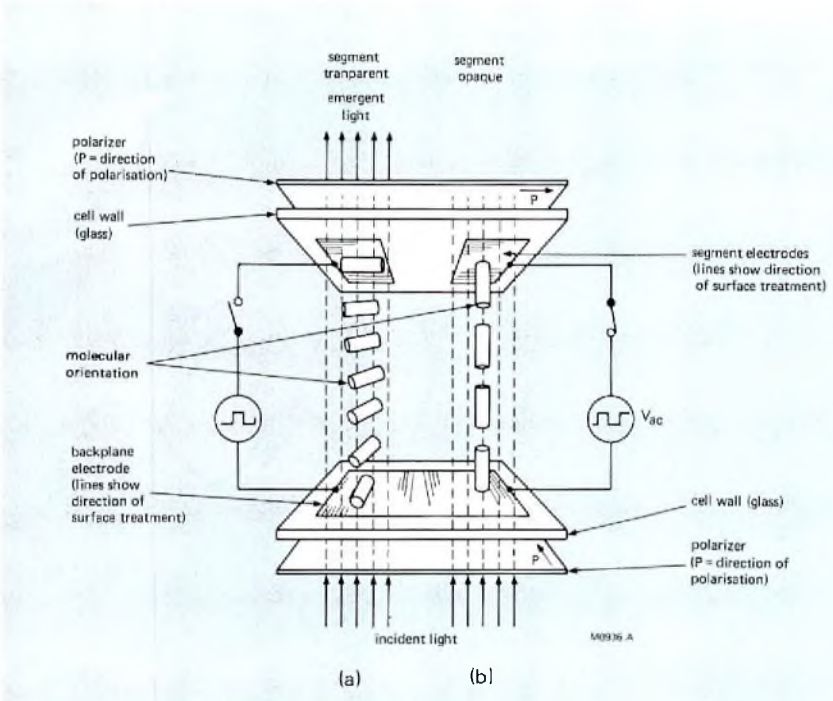


Fig.5 Principle of operation of TN-LCD (positive contrast mode). In the OFF-state (a), the plane of polarization is rotated 90°. In the ON-state (b), the plane of polarization is not rotated.

OPTIMIZING THE LCD FOR QUASI-ACTIVE OPERATION

By far the most commonly used liquid-crystal technology and the most promising for today's automotive industry is the twisted nematic (TN) type (Ref.1). The optical property of the liquid-crystal layer of such a display can be roughly characterized by the property that in the OFF state, the plane of polarization of linearly polarized light is rotated by 90°, whereas in the ON state (i.e. with an electric field applied normal to the liquid-crystal layer), the plane of polarization is not rotated (Fig.5). With the liquid-crystal layer between two polarizers rotated 90° to each other, the non-energized zones will be transparent and the energized one will be dark. If the polarizers are aligned, the picture will be reversed, showing transparent segments on a dark background (Fig.6).

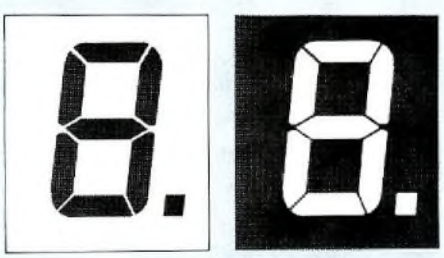


Fig.6 Positive and reverse contrast mode

So at first sight, it would appear to be a simple matter to transform a standard positive TN-LCD into a reverse-contrast one – simply rotate one polarizer through 90° and you'll get complete reversal of the display. Unfortunately it's not that simple and some important factors have to be considered when operating in reverse-contrast mode.

To understand this, it's necessary to introduce a basic figure of merit for displays: the *contrast ratio* C_r, defined as the ratio of light intensity between light and dark areas, i.e. $C_r = (I_{bright})/(I_{dark})$.

For good legibility, i.e. high C_r, I_{bright} must be very much greater than I_{dark}. C_r will then, of course, be much more sensitive to variations of I_{dark} than to variations of I_{bright} (Fig.7), so it's very important to know how I_{dark} varies with cell homogeneity, driving conditions and polarizer quality.

For a standard TN-LCD with crossed polarizers and dark information on a light background, I_{dark} is the residual transmission of the energized segments, and its value is determined principally by the drive voltage and by the polarizer efficiency. For optimum contrast with standard TN-LCDs, you need a drive voltage close to saturation and good polarizers.

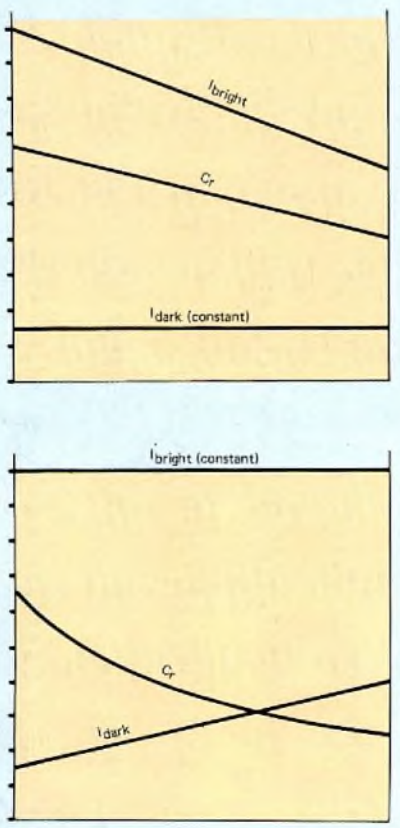


Fig.7 Contrast ratio dependence on light intensities (I_{bright}/I_{dark})

For a TN-LCD with reversed contrast, I_{dark} is the residual transmission of the background in its quiescent (inactive) state. This is independent of driving conditions and is influenced mainly by the optical quality of the cell and by its rotational characteristics, i.e. the way it transmits polarized light.

Specifically, the anisotropic nature of the liquid-crystal material means that any liquid-crystal cell of finite thickness will turn linearly-polarized light into elliptically-polarized light. The degree of ellipticity depends on the wavelength λ, cell thickness d and birefingence Δn of the liquid-crystal material. The quantity $d\Delta n$ is known as the optical thickness of the display, and for any given wavelength, certain discrete values of $d\Delta n$ lead to zero ellipticity (Fig.8). For white light there's no perfect solution and ellipticity essentially decreases with increasing $d\Delta n$. This shows itself as light leakage in the dark zones of the display and hence reduced contrast.

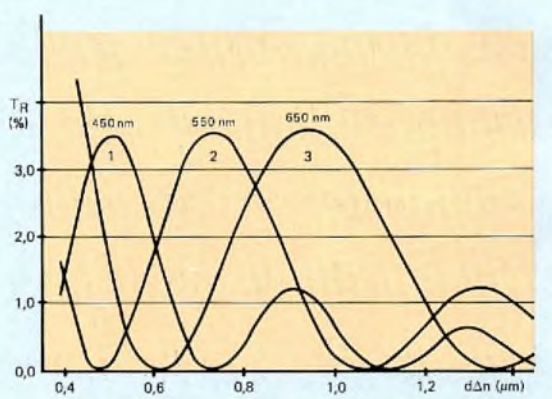


Fig.8 Transmittance behaviour of the dark state in a TN-LCD with reverse contrast and ideal polarizers

There are various ways of reducing this light leakage (see Ref.2). You can, for instance, increase d or Δn, or reduce the angle of twist of the cell. None of these methods, however, are without drawbacks. A far better solution, and one which we use in our displays, is the use of *pleochroic dyes*.

Using pleochroic dyes to reduce light leakage

A pleochroic dye consists of rod like molecules that align with the liquid-crystal molecules. The dye essentially has no effect on light propagating parallel to its molecular axis, but it will strongly absorb light of a given wavelength propagating perpendicular to the molecular axis if this axis also lies in the plane of polarization. So when the liquid-crystal cell is in the ON state, the liquid-crystal and dye molecules are aligned parallel to the propagation direction (right side of Fig.9) and the dye has practically no effect.

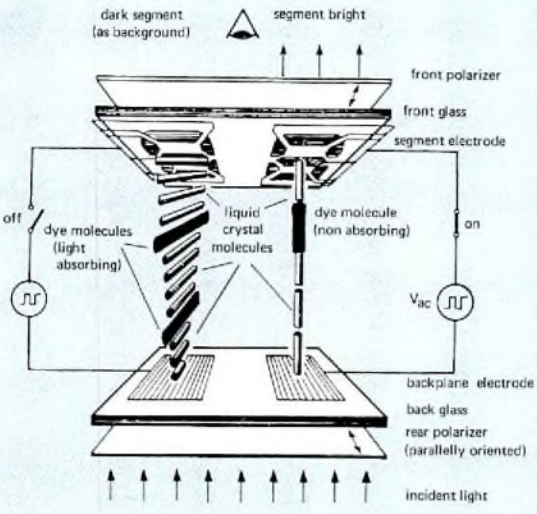


Fig.9 Reverse contrast TN-LCD with dye admixture: principle of operation

When the cell is in the OFF state, the liquid-crystal and dye molecules are aligned perpendicular to the propagation direction (left side of Fig.9) and the dye effectively forms a supplementary absorption system.

So by choosing the appropriate dye, the light leakage in the dark zones (which is wavelength dependent) can be suppressed. The dye can also be used to suppress disturbing rainbow effects caused by variations in light leakage due to small differences in cell thickness.

A further problem with reverse-contrast TN-LCDs is that the choice of operating voltage is far more critical than it is for positive contrast displays, and to avoid OFF-segment visibility (at least for low multiplex rates), it should be between 200 and 500 mV lower. However, it's safe to say that all measures taken to reduce leakage into the dark zones of a reverse-contrast TN-LCD will also reduce OFF-segment visibility.

So the above approach, using optimized liquid-crystal materials with pleochroic dyes has led to reverse-contrast quasi-active LCDs with high contrast ratio and extremely low leakage, permitting the use of LCD panels with uniform appearance without need of a black mask.

COLOURED TN DISPLAYS

Colour can be introduced into TN-LCDs in three ways: with colour-selective polarizers, colour filters or coloured back-lighting. Colour-selective polarizers produce coloured segments on a bright background (or vice versa). Colour filters and coloured backlighting are basically the same, each being used to best advantage with reverse-contrast LCDs.

We expect the second (i.e. colour filters) to become the most popular with reverse-contrast LCDs. This will probably be realized either by separate mechanical filters behind the display, or better still, by printing translucent colours on the display itself.

Figure 10 shows a prototype reverse-contrast LCD with printed coloured segments. To guarantee good legibility for all illumination levels from darkness to direct sunlight, new transflector materials will have to be developed with a higher transmission coefficient than those of current materials (which are optimized for operation in the reflective mode only).

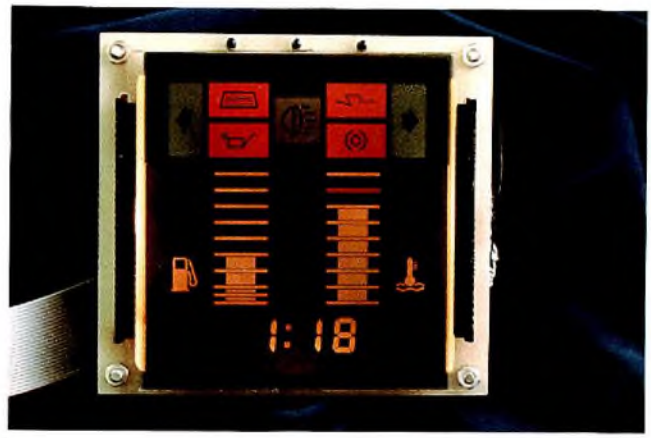


Fig.10 Reverse contrast prototype LCD with printed colour fields

DRIVING MODE – CONNECTIONS AND DRIVER INTEGRATION

For multiplexed LCDs, the OFF-segment visibility imposes constraints on operating voltage, reducing the viewing angle and changing the viewing cone symmetry. In a car, however, the main requirement is for a wide horizontal viewing angle (the vertical viewing angle being relatively unimportant), and a multiplex ratio of 1:2 is generally considered quite satisfactory. For auxiliary features, however, in driver information systems, for example, higher multiplex ratios will be necessary. It's advisable to incline the cell normal slightly relative to the principal viewing direction (Fig.11), say around $\pm 15^{\circ}$.

For optimum contrast and to keep the OFF segments invisible, the operating voltage V_{op} must be chosen so that the OFF voltage is just below the threshold voltage V_{th} (the voltage at which contrast first appears). Too high an operating voltage causes the OFF segments to become visible, too low a voltage reduces contrast. Figure 12 shows the recommended voltage area for a multiplex ratio of 1:2.

Since the threshold voltage has a negative temperature coefficient, compensation will probably be necessary to allow operation over the wide temperature ranges likely to be encountered in motor vehicles. For this, specialized integrated circuits are becoming available.

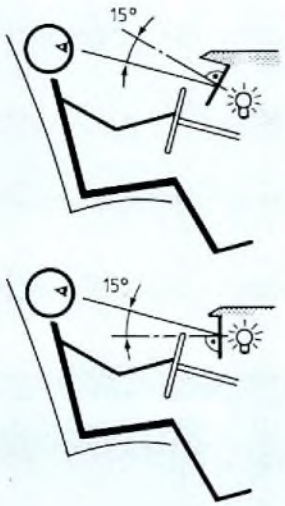
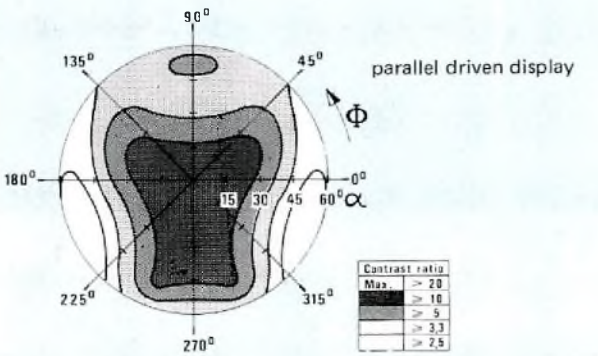
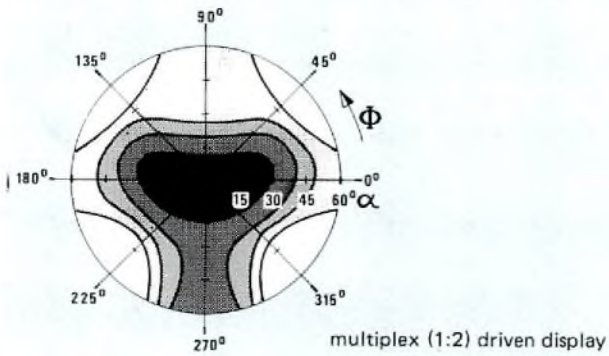


Fig.11(a) Preferred viewing directions of displays driven in a 1:2 multiplex ratio





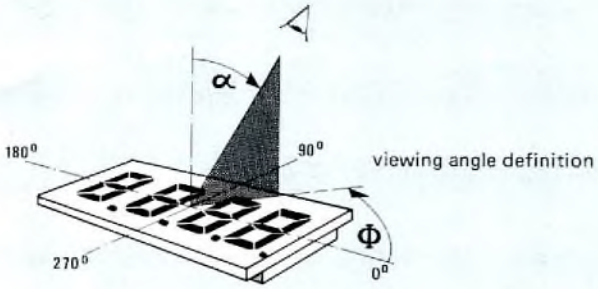


Fig.11(b) Isocontrast diagram for TN-LCD

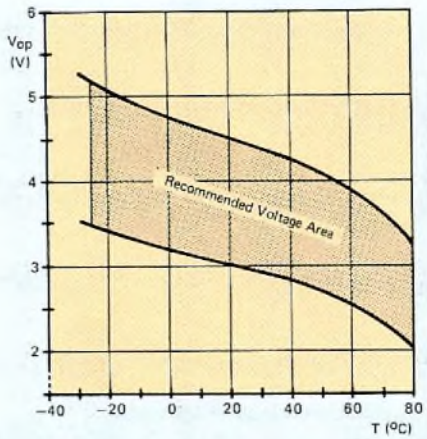


Fig.12 Recommended voltage for driving a MUX 1:2 TN LCD. Off segments visible at $\alpha > 40°$ and $\phi = 270°$. Typical contrast ratio $< 2{,}5$ at $\alpha = 0°$

VIDELEC INTEGRATED DISPLAY (VID)®

An important benefit of the 1:2 multiplex mode is that it almost halves the number of connections to the display (compared with a directly-driven display) – important for system reliability. However, for large dashboard display systems with quite high information density, contacting still remains a major problem, and the best solution will undoubtedly be to integrate the driver onto the glass.

For this, Videlec now has available a new chip-on-glass technology in which the driver IC is bonded directly to the glass of the LCD. Only general-purpose drivers are integrated onto the glass to allow the display system to interface directly with an external controller (Fig.13). The driver is bonded in what's known as 'flip-chip geometry' (with the chip face down on the contact pads, Figs 14 and 15) requiring the smallest amount of extra glass for the hybrid section.

Fig.13 Prototype Videlec integrated display (VID) with chip-on-glass and printed translucent colours, the LCD is driven in a multiplex 1:2 mode

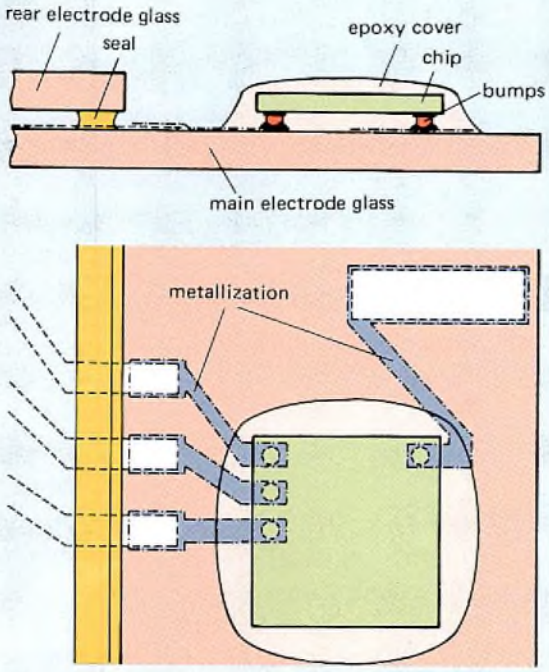


Fig.14 Schematic view of the hybrid section of a cell with integrated driver IC

The manufacturing process fits well into standard LCD technology and is partly implemented in batch production (Refs 4 and 5). Some of the advantages offered by this new chip-on-glass technology are:

- shorter connections between segments and driver output
- lower stresses induced in the glass during bonding

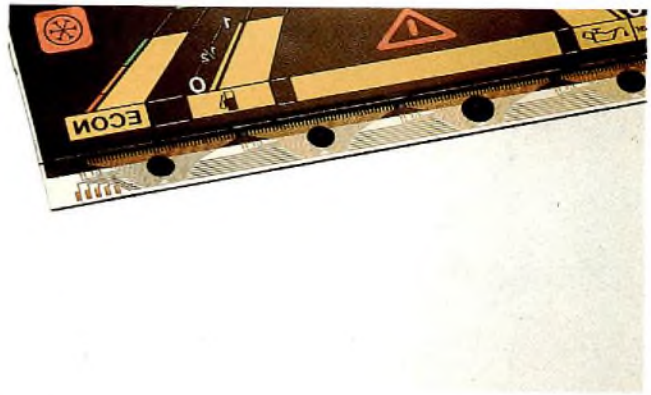


Fig.15 Detail of custom-designed Videlec integrated display (VID) showing the cascade of driver ICs (PCF8576)

- compact bond geometry for good thermal matching, giving high immunity to thermal cycling and thermal shocks
- excellent humidity resistance and complete immunity to light penetration.

The principal constraint of this new technology is that it's limited to single-plane wiring configurations and chip layouts. This presents no problem, however, with Videlec's new general-purpose PCF8576 driver IC (see the Table and Fig.16) which allows for chip cascading in single-plane configurations. The PCF8576 is equipped with a standard serial-bus (I^2C) interface and hardware sub-addressing. It's programmable in driving mode from direct to multiplex 1:4, and it can handle complicated display systems with up to 16 chips on the bus (with five external contacts on each display element).

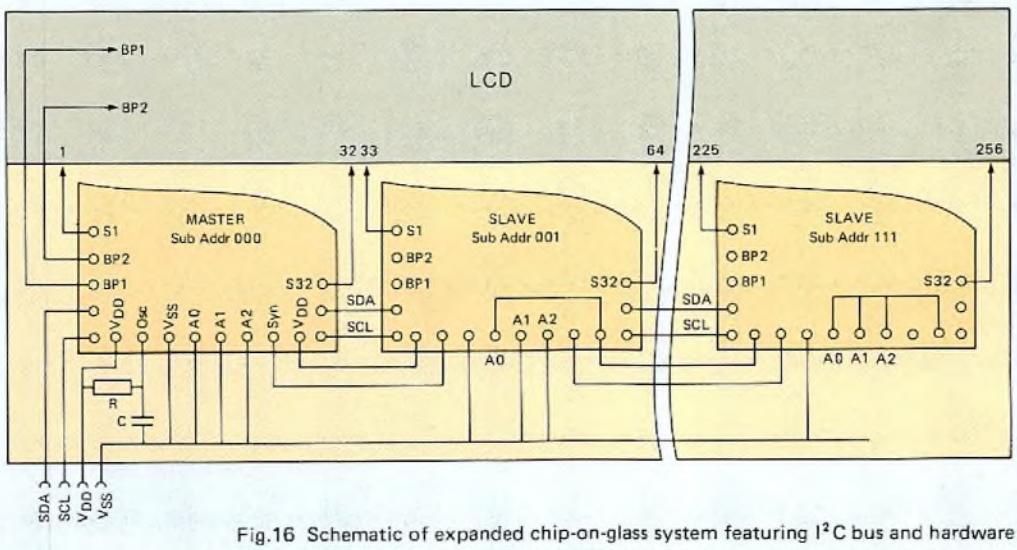


Fig.16 Schematic of expanded chip-on-glass system featuring I^2C bus and hardware subaddressing in single plane wiring configuration

Fig.17 Example (work prototype) of a dashboard combination

Features – PCF8576 universal LCD driver for low multiplex rates

- Single chip controller/driver
- Selectable drive configuration: direct, MUX 1:2, 1:3, 1:4
- Selectable driving method: 2-, 3-, 4-level
- 40 segment lines (up to 160 elements)
- I^2C bus interface, compatible with any 4-, 8-, 16-bit microprocessor
- 2 V to 9 V power supply range
- Separate LCD and logic supplies possible
- Power saving mode available
- 40 X 4 bit RAM for display data storage
- Auto-increment addressing and hardware subaddressing
- Versatile blinking capabilities (selected segments or whole display)
- Cascadable with up to 16 drivers (max. 2560 elements)
- Optimized for single plane wiring
- Compatible with Videlec chip-on-glass technology
- Very low external component count (at most one resistor)
- Space-saving 56 lead VSO-56 package

Finally, 5 to 8 contacts for supply lines and serial bus will still be necessary, but in a dashboard, there'll be more than enough space for a plug or clip-on arrangement. And since only one small connector will then provide access to the display system, mounting of the display will be independent of its electrical connections, an evident advantage in an environment subject to considerable vibration.

ACKNOWLEDGEMENT

The authors are indebted to Dr. M. de Zwart for his help in preparing this article.

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An integrated approach to CD players

Part 1: The optical pick-up

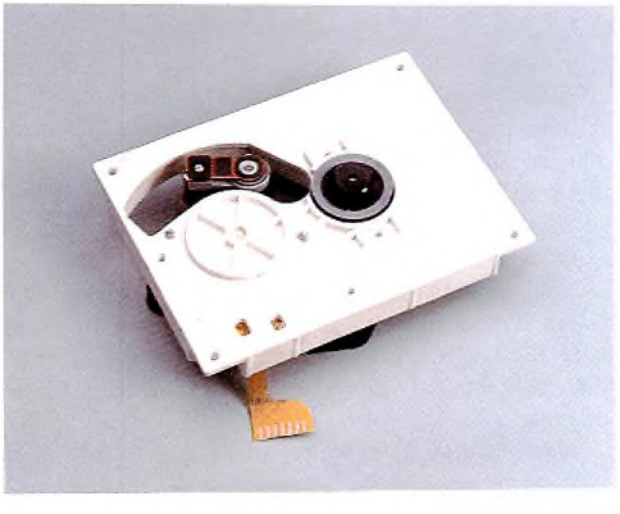
J. NIJHOF

A much-publicised advantage of the Compact Disc (CD) system is its high level of immunity to dust, fingerprints and scratches on the compact discs. To this list can be added its immunity to (within-specification) disc defects such as pin-holes and track eccentricity introduced by the pressing equipment. Less-publicised, but even more important, are the marked differences in the ability of individual players to handle these defects and, in addition, the knocks, vibration and g-forces experienced in cars.

This article and Part 2 will describe some of the novel aspects of our new ICs and optical pick-up that can be used to manufacture players that will play mishandled discs under adverse conditions without producing any detectable sound colouration. Benefits for the player manufacturer include

- simple designs (few ICs with virtually no external components),
- flexible designs owing to the use of a standardized inter-IC digital audio bus,
- designs that can be upgraded to accommodate future trends in digital signal processing.

A full-performance player using the new ICs is shown in Fig.1. All player functions are integrated in the new chip set, reducing the cost of a player's electronics significantly. Furthermore, no factory adjustment of players is necessary. Two servo ICs, with automatic gain and offset correction, control the pick-up, and a single decoder chip incorporates the demodulator PLL and VCO, error corrector and a basic concealment function for uncorrectable audio data. For full-performance players, an additional chip containing a digital oversampling filter and an enhanced concealment function is available. The chip set is completed by a dual 16-bit DAC for maximum fidelity and an integrated analog filter with outputs for an audio amplifier and for a headphone.



The new CD mechanism (CDM2) comprising pick-up, swing arm and disc drive motor. Just 30 mm high and with an operating temperature range of −30 to +75 °C, the mechanism is suitable for home, car and portable players. The size reduction has been achieved, without the need to resort to folded optics, by using a new optical arrangement that requires only four components.

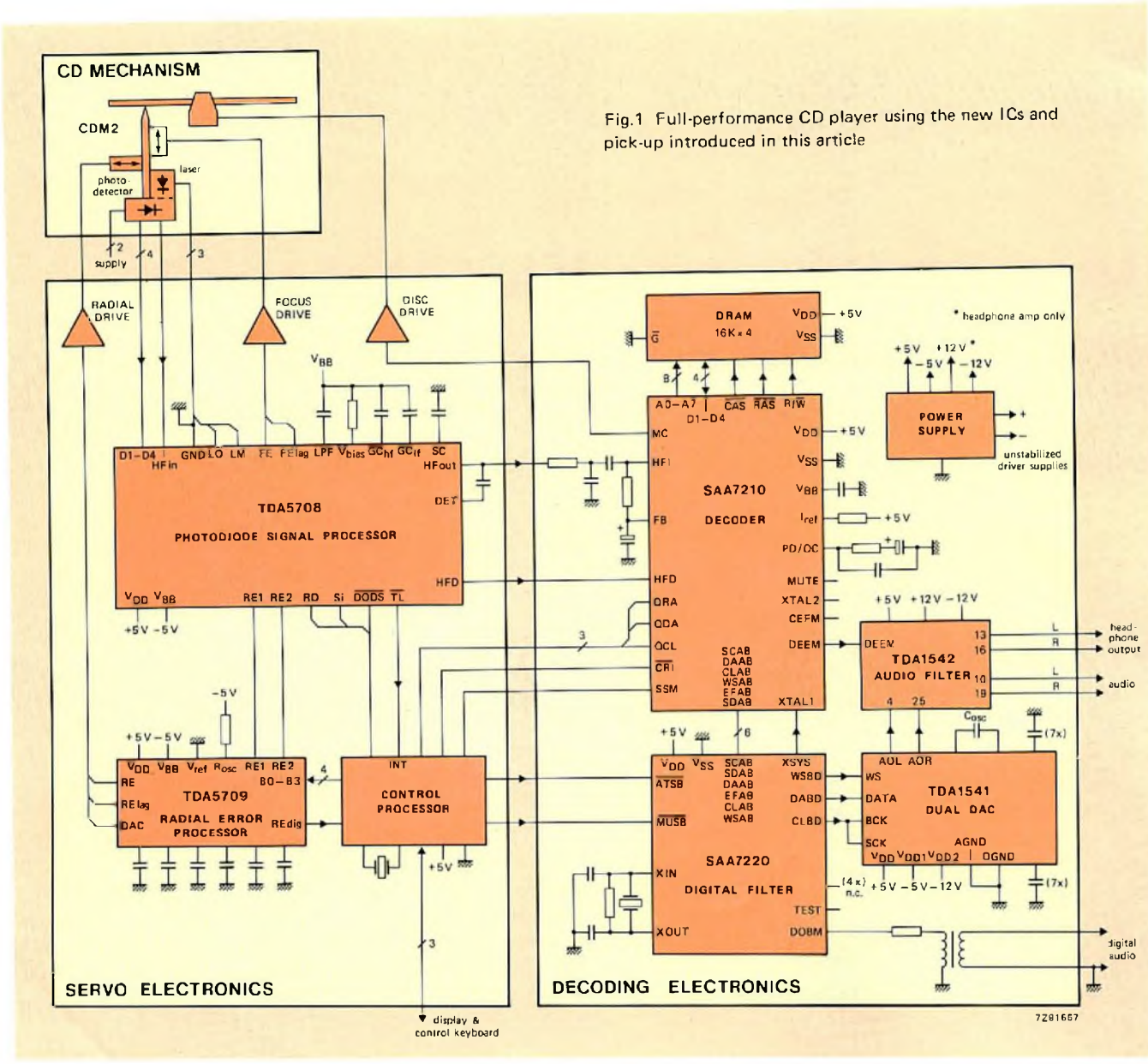


Fig.1 Full-performance CD player using the new ICs and pick-up introduced in this article

CD OPTICAL PICK-UPS

Before we describe the CDM2 pick-up*, it will be useful to summarize the stringent requirements to be met by a pick-up servo-system, and to review the pick-ups in current use.

The function of the optical pick-up of a CD player is to generate a high-quality r.f. signal (eye pattern) for the player's demodulator from a disc's pit/land transitions which contain the audio data, track number, title, etc. To generate an eye pattern from which all the data on the disc can be retrieved, the laser spot should follow the centre of the 0,6 μm wide track to within about ±0,1 μm, with no interference from adjacent tracks *just 1,6 μm away*. Since the track on the disc may be slightly eccentric due to tolerances in disc pressing equipment, and to handle the effects of vibration, the servo should furthermore be able to accommodate a maximum side-to-side track swing of about 300 μm. The radial tracking servo system capable of meeting these, already demanding, requirements should in addition be able to absorb the effects of knocks to the player and external vibration.

The requirements for the focusing servo are equally severe. For adequate read-out, the focusing servo has to keep the laser beam focused on the reflecting layer of the disc to within ±0,5 μm, even with a maximum disc warp of 1 mm.

Manufacturers use a variety of techniques (with varying success) to generate the error signals for the tracking and focusing servos.

* a product of Philips Consumer Electronics Division.

CD2 – SECOND GENERATION CD SYSTEM

CD2 is the first all-integrated system for CD players. CD2 means improved performance for the listener, and simpler more flexible designs for the manufacturer. This additional flexibility stems from a single-chip decoder concept which can be expanded for full-performance designs by adding a digital oversampling filter IC. An analog filter IC can be used to make either a low-order analog filter for a full-performance player or a high-order filter for a low-cost player. Two bipolar ICs provide all the control servo functions for a single-beam swing arm pick-up. A full-performance player is shown in Fig.1. This player which requires *no factory adjustment* comprises:

CD mechanism

CDM2: a smaller version of our swing arm mechanism CDM1 in a tough plastic surround. Height of the CDM2 is 30 mm. Operating temperature range is −30 °C to +75 °C. These features and a very short arm with low moment of inertia make CDM2 suitable for use in portable and car CD players.

Servo electronics

TDA5708: bipolar photodiode signal processor

- photodiode signal preamplifiers with separate r.f. and d.c. a.g.c.s for optimum generation of the r.f. data signal and the focusing/tracking error signals
- tracking error signal amplifier
- focusing error signal processor with focus normalising and start-up circuit
- data equalizer
- r.f. level and track-loss detectors
- regulated supply for the reading laser diode
- low current consumption: 15 mA (8 V – 14 V).

TDA5709: bipolar radial error processor

- tracking error processor with automatic asymmetry control
- a.g.c. circuitry with automatic start-up and wobble generator
- tracking control for fast forward/reverse scan, search, repeat and pause functions
- low current consumption: 10 mA (8 V – 14 V).

Decoding electronics

The decoder comprises three ICs compared with the six ICs of our previous decoder. In addition, an IC is avajlable for constructing a variety of low-pass analog filters.

SAA7220: NMOS digital filter with enhanced concealment of uncorrectable errors

- two identical phase-linear digital FIR filters with 120 filter coefficients
- four times oversampling
- linear interpolation of up to 8 consecutive erroneous samples
- I^2S data I/O for compatibility with future sound processors
- integrated digital audio output according to the Philips-Sony proposal
- soft mute of audio when starting, stopping or pausing
- 12 dB attenuated audio facility when scanning.

TDA1541: bipolar dual 16-bit DAC

- two separate DACS on one chip (no multiplexing, so no delay between the stereo channels)
- operates at bit rates up to 6 Mbits/s for use with four times oversampled data in the CD system
- programmable for offset binary or two's complement signals
- I^2S input format
- 1 μs (typ.) settling time to ± 1 LSB.

TDA1542: bipolar dual analog output IC

- can be used to make a low-order analog filter for a full-performance player with digital filtering, or a high-order filter for a low-cost player using a single-chip (SAA7210) decoder
- two identical circuits for stereo applications
- incorporates de-emphasis switch and silent switch-on/off circuitry
- headphone output.

SAA7210: NMOS single-chip decoder

- comprises all decoding functions:
  - demodulator with adaptive data slicer
  - fully-integrated demodulator PLL
  - subcoding data processor
  - error corrector with adaptive error-correction strategy
  - basic interpolation and sample-and-hold circuit
- improved error correction – of up to a 15-frame burst error
- large (64-frame) FIFO storage for portable and car player applications
- I^2S (inter-IC signal) data output.

Tracking

Four basic techniques are available for generating a radial tracking error signal:

- single-beam push-pull tracking
- single-beam differential phase detection (DPD) or heterodyne tracking
- single-beam h.f. wobble tracking
- three-beam tracking (using two auxiliary beams to generate the error signal).

Focusing

Three basic techniques are available for generating a focus signal:

- astigmatic (cylindrical lens) focusing
- Foucault (knife edge) focusing
- critical angle focusing.

The three most popular tracking-focusing combinations found in CD pick-ups are:

- single-beam push-pull tracking with Foucault focusing (a design of Philips Audio Division)
- three-beam tracking with astigmatic focusing
- DPD with critical angle focusing.

The first two are in common use and are shown in Fig.2. CDM2 uses a version of the first combination with a low-frequency wobble injected onto the radial error signal for optimum tracking. The pick-up is mounted in a swing arm which describes an arc across the disc during playback. In contrast, a three-beam pick-up is usually mounted in a sled capable of movement along a disc radius. A single-beam pick-up can also be mounted in a sled-driven system; a 3-beam pick-up on the other hand won't work in the swing arm since the three beams have to be aligned and maintained in a fixed position relative to the track. Table 1 shows the relative merits of CDM2 and a typical three-beam pick-up. Table 2 gives brief data on CDM2.

TABLE 1
Comparison of the CDM2 single-beam/swing arm pick-up and a three-beam/sled pick-up

	CDM2	typical three-beam pick-up
mechanics	simple – just one moving part	complex, two-stage radial movement using a lead screw. A moveable mirror is often used to deflect the reading beam quickly over small distances to handle track eccentricity
optics	4 components: objective (single aspherical lens) collimator, wedge, fixed semi-transparent mirror	at least 5 components: objective, collimator, grating (with adjustment) cylindrical lens beam splitter
	only one adjustment needed during player assembly – horizontal position of the photodetector	several critical alignments needed during player assembly including the alignment of the beams used to generate the radial error signal
focusing	Foucault; objective moved by a coil/magnet combination	astigmatic; objective moved by a coil/magnet combination
interference in the radial error signal	virtually none – all signals derived from a single spot on the disc	the l.f. components of the eight-to-fourteen modulation used in the CD system create interference with a 3-beam pick up. Not relevant when playing video discs there being no l.f. components in the modulation (Philips Laservision players have a 3-beam pick-up)
shock tolerance	good[1])	good
electronics	depends on the playability required[2])	depends on the playability required[2])

[1]) a swing arm is more immune to the translational forces associated with everyday bumps.

[2]) playability is the ability of a CD player to reproduce the original recorded sound under adverse playing conditions (scratched discs, moving player etc.) without interrupting the audio output, see panel.

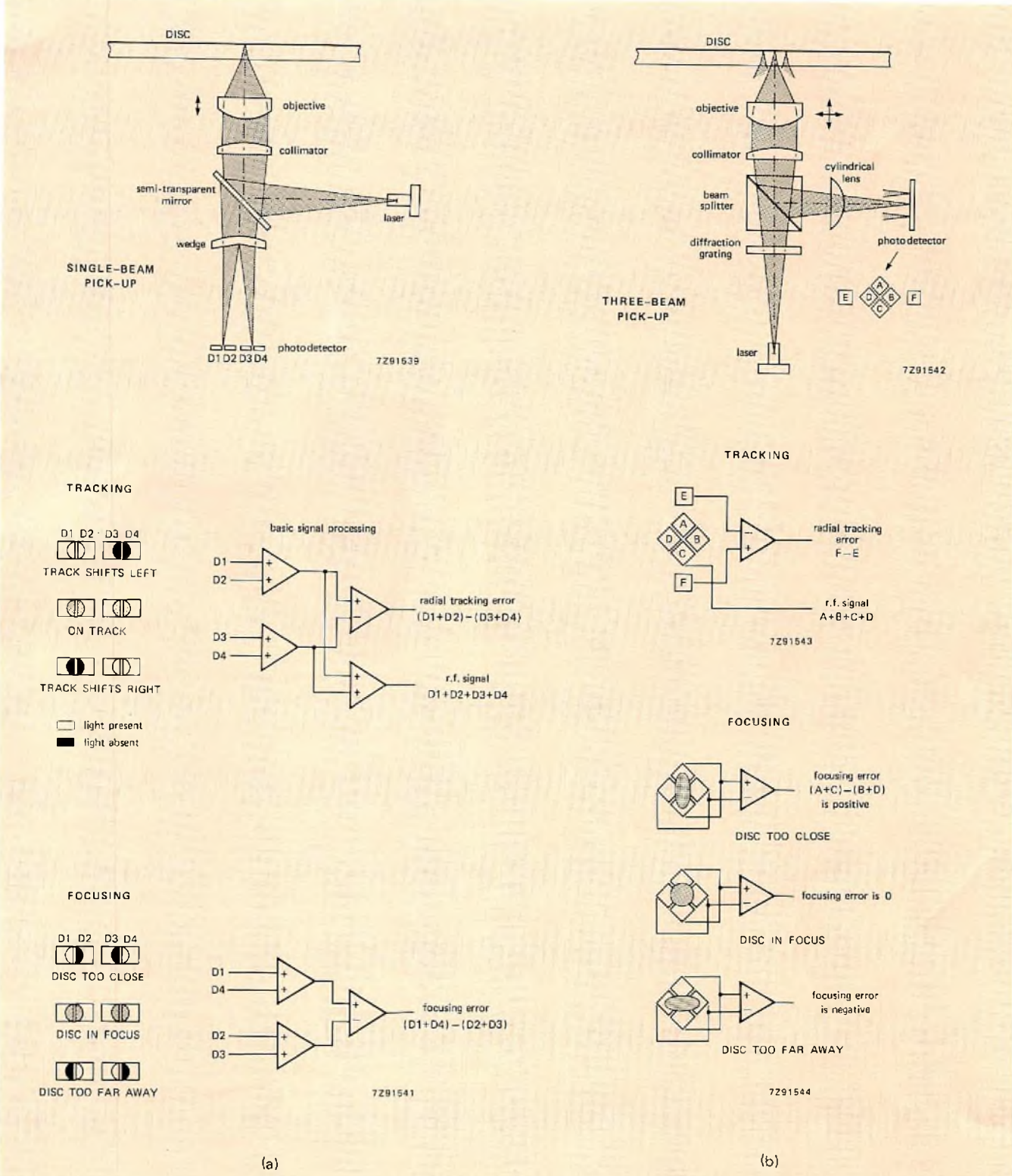


Fig.2 (a) A single-beam pick-up such as CDM2. Servo ICs TDA5708 and TDA5709 obviate the critical alignment and precision mechanics needed with a three-beam pick-up shown in (b)

PLAYABILITY

Standard test discs are available to all licensees and distributors of the Compact Disc digital audio system. These discs readily expose weaknesses in the design of a CD player by testing a player's ability to tolerate small defects in a disc without producing audible clicks or pauses in the reproduced sound (playability).

On the surface of each disc are a series of opaque dots which represents dust and dirt, a simulated fingerprint, and gaps in the recorded track which simulate minor imperfections in the pit pattern. A player's ability to handle these artifical defects is a good measure of its ability to cope with real production defects such as air bubbles, pin-holes, enclosures and scratches.

Test disc '4A'

test	details	requirement of the CD system specification
fingerprint	a simulated fingerprint that reduces the light reflected onto the photodiodes in the pick-up	should produce no audible distortion
stain	a series of opaque dots with diameters of 300, 500, 600 and 800 μm	the 300 μm dot should produce no audible distortion
wedge	400 μm to 900 μm gaps in the recorded pit pattern	the 400 μm gap should produce no audible distortion

TABLE 2
Brief data on the CDM2 mechanism

length	130 mm
width	100 mm
height	30 mm
weight	325 g
operating temperature range	−30 to +75 °C
supplies	
laser	55 mA typ
radial drive	30 mA typ
focus drive	25 mA typ
disc drive	30 mA typ
objective	
numerical aperture	0,46

CDM2 PICK-UP

Mechanics

The pick-up is mounted at the end of a low-inertia balanced arm pivoted at its centre. A coil housed in the arm, see photo, and a permanent magnet attached to the chassis form a linear motor used both to track and to fast-feed the pick-up across the disc. When the motor is energised, the pick-up can be directed quickly to any track (<1 s from inner to outer track), and can follow the centre of the track accurately to within 0,1 μm. Large track eccentricities can be followed because there is no vignetting (the whole pick-up moves, not only an objective as in a three-beam pick-up). Since there is only one moving part (the arm pivot), the mechanism is extremely reliable and wear is minimal.

Close-up of the optical pick-up and swing arm of the new CD mechanism

For comparison, it will be useful to say a few additional words about a three-beam pick-up. A three-beam pick-up needs a linear movement. A disc is tracked by moving the pick-up objective along a radius of the disc. Often, a moveable mirror is inserted in the optical path to deflect the laser beam quickly over small distances, to handle track eccentricity for example. Two auxiliary beams are used to generate a tracking error signal. Alignment of these beams is critical, and the sled carrying the pick-up and the lead screw and guide all have to be precision components. Any misalignment of the auxiliary beams during the life of the player will impair tracking. Fast-feeding is done by moving the complete optical assembly radially across the disc, for example, by means of a lead screw. The thread of the lead-screw is always a compromise between the fine thread required for normal tracking during playback (35 mm per hour to take up the tracking movement) and the coarse thread required for fast feed (35 mm in 1 second, say).

Optics

A feature of the CDM2 pick-up is its simple diffraction-limited optics. The laser point source is focused on the information layer of the disc by two lenses: a spherical

glass objective with a plastic aspherical skin, and a sperical glass collimator (most CD pick-ups, including our own CDM1, use a three-element objective and a two-element collimator). The thin plastic skin of the objective is attached using a proprietary process (Ref.1). Owing to the glass body, the objective is stable in humid conditions and temperatures up to 85 °C, while the aspherical skin provides the desired aberration-free optical performance.

The low-profile optics of CDM2 has been obtained by interchanging the positions of the laser and photodetector used in our previous pick-up (Fig.2(a) and Ref.2). Furthermore, an inexpensive semi-transparent mirror is used instead of a beam-splitter cube. Astigmatism introduced into the reflected beam by the mirror is corrected by a plastic component (the wedge, in Fig.2(a)) which also dissects the beam into the two halves from which the tracking and focusing error signals are generated.

One could ask, why not use the reflected astigmatic beam to generate the error signals directly (i.e. astigmatic focusing in combination with push–pull tracking)? Our experience indicates that the error signals generated in this way are noisier than with Foucault focusing/push-pull tracking.

Virtually no interference in the radial error signal

The CDM2 pick-up derives the tracking error, the focusing error and the audio signals from one spot on the disc. Compared with a three-beam pick-up, this has two advantages:

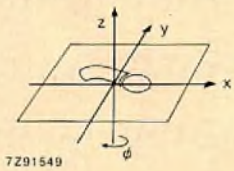
- virtually no interference from the r.f. signal in the radial error signal
- allows lower mechanical tolerances in the pick-up, giving long-term optimum tracking with no adjustment of the radial error signals needed.

Shock tolerance

The tracking servo-system for CDM2 is optimised to handle disc defects and the effects of vibration. The latter can be reduced further by mounting the CDM2 mechanism in a well-designed floating suspension. This suspension should have the characteristics given in Table 3 with progressive damping for large-amplitude shocks.

TABLE 3
Recommended characteristics of a suspension for CDM2

Resonant frequency	
x axis	25 ± 4 Hz
y axis	25 ± 4 Hz
z axis	25 ± 4 Hz
ϕ	45 ± 4 Hz
Q damping	5



Electronics

Some aspects of the decoding electronics are described in Part 2.

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ACKNOWLEDGEMENTS

1. This article is based on an article that appeared in Japanese in the December 1984 issue of Audio, Video, Electronics and Record, Tokyo, Japan; permission to publish is gratefully acknowledged.
2. The author wishes to acknowledge the assistance given while preparing this article. Particular thanks are due to colleagues at the Compact Disc Laboratory, Philips Consumer Electronics Division and at Philips Research Laboratories, Eindhoven.

An integrated approach to CD players

Part 2: The decoding electronics

J. NIJHOF

In Part 1, we introduced a new single-beam optical pick-up and servo ICs for Compact Disc (CD) players, the advanced designs of which allow the manufacture of small players that can handle disc defects such as scratches, pin holes and track eccentricity, as well as the knocks, vibration and g-forces encountered in portable systems. Hand in hand with this advance come exciting developments in the signal-processing circuitry. Developments that, among other things, allow full advantage to be taken of the error-correction capability of the CD system, to produce high-performance players with no detectable sound colouration.

This article describes some of these new developments, in particular the integrated CD decoder. The decoder requires no adjustment and is suitable for all CD players – those with a single-beam pick-up and those with a three-beam pick-up. Besides the audio application, the decoder can be used in many other applications requiring a high-performance high-reliability Reed-Solomon decoder, e.g. CD ROM.

Supporting the decoder IC, several circuits have been developed to facilitate the manufacture of players with:

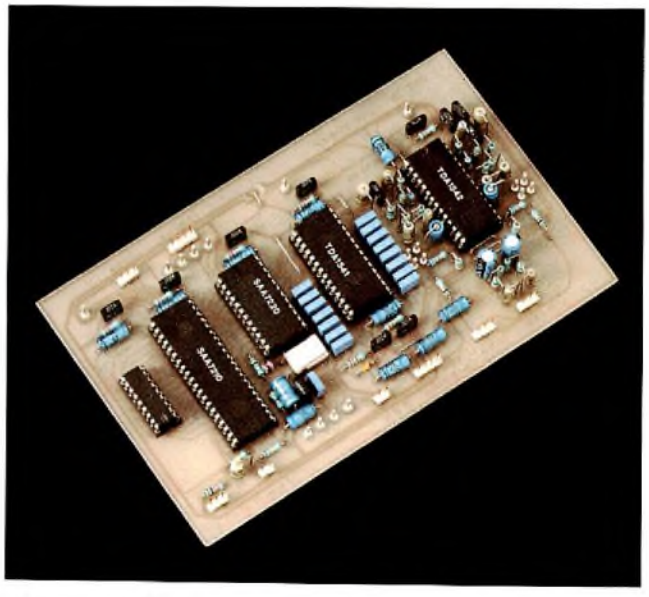
- fewer ICs and fewer peripheral components
- greater design flexibility
- improved sound reproduction.

Such a player is shown in Fig.1.

Figure 2 shows the new decoding electronics and the six ICs (shaded) it replaces (Ref.1). The SAA7210 decoder IC incorporates the functions of demodulation, error correction and basic interpolation. The SAA7220 digital filter IC incorporates enhanced interpolation circuitry and a phase-linear digital FIR filter. A dual 16-bit DAC TDA1541 (operating at 176,4 kHz) followed by a stereo analog output IC TDA1542 replaces two DACs and two discrete analog filters.

The data format between the SAA7210, the SAA7220 and the TDA1541 is according to the I^2S (inter-IC signal) specification*, giving the player manufacturer maximum design flexibility. This would allow the SAA7220 to be omitted in Fig.2, for low-cost players, leaving the manufacturer free to design his own low-pass filter.

* Inter-IC signal (I^2S) communication is a communication format for digital audio. The I^2S bus is a three-line bus comprising: clock, serial data line, and a control line used to select left and right channel words.



Laboratory model of the new high-performance decoding electronics for CD players

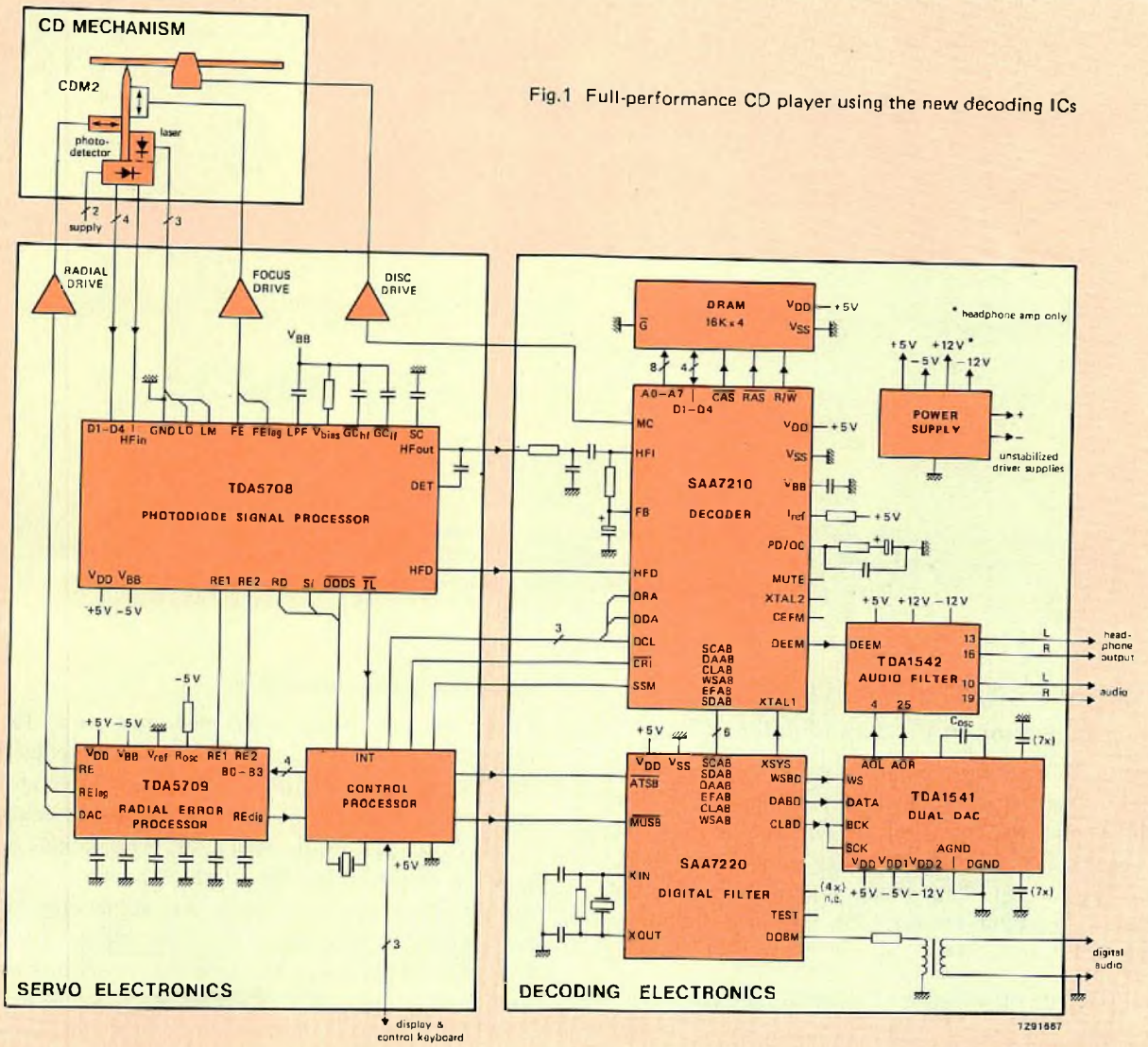


Fig.1 Full-performance CD player using the new decoding ICs

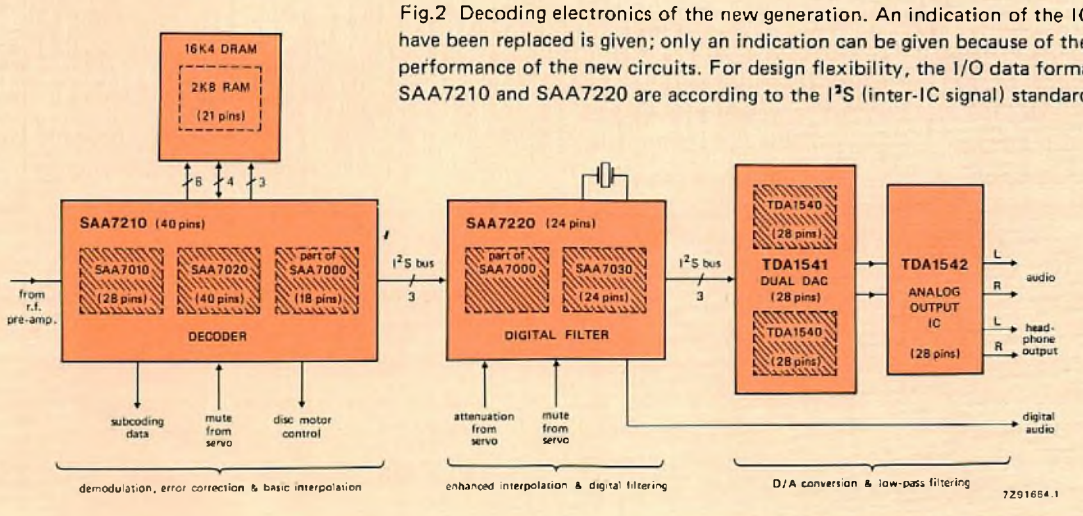


Fig.2 Decoding electronics of the new generation. An indication of the ICs that have been replaced is given; only an indication can be given because of the superior performance of the new circuits. For design flexibility, the I/O data formats of the SAA7210 and SAA7220 are according to the I²S (inter-IC signal) standard.

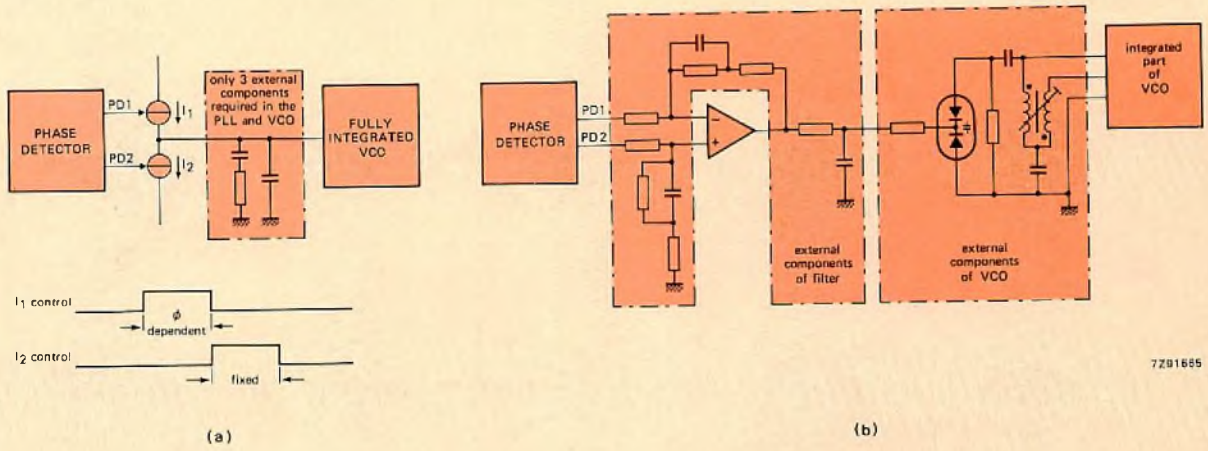


Fig.3 (a) In the SAA7210, an integrated charge pump design is used in the differential filter of the demodulator PLL. This filter is self-balanced and consists of only three external components; the VCO is fully integrated. (b) Previous arrangement requiring a balanced differential filter, varicap diode, coil, resistors and capacitors

FEATURES OF THE NEW DECODER

Further integration of the demodulator PLL

A feature of the SAA7210's demodulator PLL is that it requires virtually no peripheral components. The VCO is a fully-integrated RC oscillator; it requires no peripheral components. The differential filtering circuitry of the PLL uses a self-balancing charge pump design that requires only one filter comprising just three low-tolerance components (Fig.3).

More efficient processing of subcoding data

Besides the audio information recorded on a compact disc, information representing track numbers, playing times, titles and composers is recorded so that tracks can be played in any desired sequence and titles and elapsed playing times etc. can be displayed. This information, termed Q-channel subcoding data, is derived continually in the SAA7210 from the demodulated r.f. signal. A new handshaking protocol between the SAA7210 and control processor reduces the time the control processor spends handling subcoding data. When the processor wants data, a request is sent (via QRA, see Fig.1) to the SAA7210 which, when a full Q-channel frame is ready, acknowledges the request and enables the serial data output QDA. The processor sends a clock signal (QCL) to shift the data out of the SAA7210.

The first negative-going edge of the clock signal resets the acknowledge signal thereby releasing the request line. If the processor doesn't require all the subcoding data, say only the number of a track (contained in the first sixteen bits), it can reset the request line after these bits have been received, thereby disabling the QDA output of the SAA7210 which resumes collecting new subcoding data.

Adaptive error-correction

Until now, no CD player has made full use of the error-correcting capability of the CD system's Cross-Interleaved Reed-Solomon Code (CIRC). This code enables up to four erroneous symbols* (in a 32-symbol block) to be corrected if the CIRC decoder is given prior information about the position of the errors. This type of correction, where the position of an error is known, is called an erasure correction. When the positions of errors are unknown, up to two erroneous symbols can be corrected. A decoder with the maximum error-correction capability (like that of the SAA7210) can make the corrections shown in Table 1.

For optimum error-correction, only the following corrections of Table 1 are relevant:

t = 2	look for and correct two errors, positions unknown
e = 1, t = 1	make one erasure correction, and look for and correct one additional error
e = 2, t = 1	make two erasure corrections, and look for and correct one additional error
e = 3	make three erasure corrections
e = 4	make four erasure corrections.

A new approach to error-correction in the SAA7210 known as adaptive error-correction discriminates between the errors found on a compact disc. This discrimination:

- enables more corrections to be made (e.g. longer burst errors)
- makes the corrections more reliable.

* 14 bits.

TABLE 1
Error-correction possibilities of the CIRC decoder of the SAA7210

t \ e	0	1	2	3	4
0	•	•	•	•	•
1	•	•	•		
2	•				

t = detect and correct an error
e = erasure correction.

As shown in Fig.4, these improvements are achieved by using additional error flags generated by the EFM decoder (using the bit run-length criteria to flag symbols likely to be in error) and by using multi-level error flags generated by the C1 and C2 corrector*.

With the error flags, several error-correction strategies are available, the strategy chosen depending on the type and number of error flags which are set by the defects on a disc.

To determine the typical defects to be found on a disc, and therefore the strategy for correcting them, special test discs with known data patterns were manufactured on normal production equipment. These discs enabled typical manufacturing defects to be identified. Normal handling defects such as scratches and fingerprints were then introduced on each disc. Extensive testing with these discs demonstrated that the error-correction was significantly improved by using multi-level flags to signal symbols in error, three flags (two bits) being sufficient:

- hard error-flag (most reliable flag)
- medium error-flag
- soft error-flag (least reliable flag).

A no-error flag is indicated by setting both bits to zero.

With these flags, the best correction strategy is selected by a flag processor, see Fig.4. For example, when two symbols in a block of thirty-two are flagged with soft error-flags, it is best to attempt a $t = 2$ correction (rather than an $e = 1$ and a $t = 1$, or an $e = 2$, $t = 1$ correction). When two symbols are flagged with hard flags, it is usually better to attempt an $e = 2$ correction and to look for and correct another symbol in error with the remaining $t = 1$ capability. After a correction, the input flags are compared with the new flags produced by the corrector to update (harden) the flags for the next stage of processing. Flag hardening progressively improves the reliability of all flags, so that very reliable $e = 3$ and $e = 4$ corrections can also be made.

Adaptive error-correction (with about 60 routes* to the correction possibilities in Table 1) is significantly better than the present correction which, owing to the use of single-level flags, has a somewhat limited correction capability.

* Two Reed-Solomon codes C1 and C2 are used to correct erroneous audio samples, C1 being used to correct small errors in adjoining symbols, C2 to correct burst errors.

All the error-correction routes for the CD audio application system are programmed in ROM in the SAA7210. They can be altered for non-audio CD storage applications.

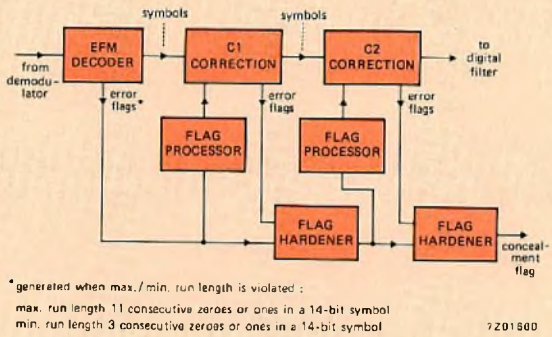


Fig.4 Symbols that violate the run length criterion are flagged 'likely to be in error' by the EFM (Eight-to-Fourteen Modulation) decoder. With this advance information, the C1 corrector can correct up to four erasures (symbols in error whose position is known) compared with the two in current designs. Although shown here as two correctors, C1 and C2 is a single corrector using sequential processing with the FIFO memory as buffer for de-interleaving 32-symbol blocks of data

Large FIFO memory for car players and portables

Part of the memory used to de-interleave the error-correction data is used as a FIFO memory to remove variations in the demodulated-data rate due to, amongst other causes, the g-forces on car players and portables. In addition, this FIFO can be used to increase the allowable mechanical tolerances for the disc drive of a player. The SAA7210 is designed to operate with a 16K x 4 DRAM which can accommodate up to 64 frames compared with the 4-frame FIFO of first-generation players. This larger FIFO is also used to store the increased number of error flags used in adaptive error-correction.

8-sample interpolation

In low-cost players, the SAA7210 can be used as a single-chip decoder, requiring only D/A conversion and low-pass filtering. The SAA7210 contains an audio hold function and single-sample interpolation as found in most other decoders on the market. Full-performance players can be made by adding the digital filter circuit SAA7220 which contains an 8-sample interpolator (Fig.5) that can conceal large burst errors. When more than eight consecutive samples are in error, a hold function operates before the interpolation.

Figure 6 shows the combined effect of improved error-correction and interpolation.

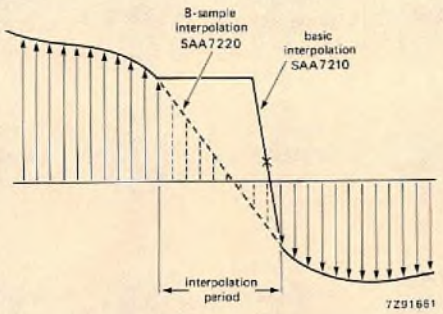


Fig.5 The SAA7220 can make an 8-sample linear interpolation, the SAA7210 a hold and single-sample interpolation. Unlike the previous design, there is no attenuation of the audio signal prior to or immediately after interpolation. When interpolating more than 8 samples, a hold function operates in the SAA7220 before the interpolation

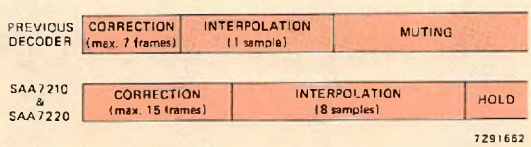
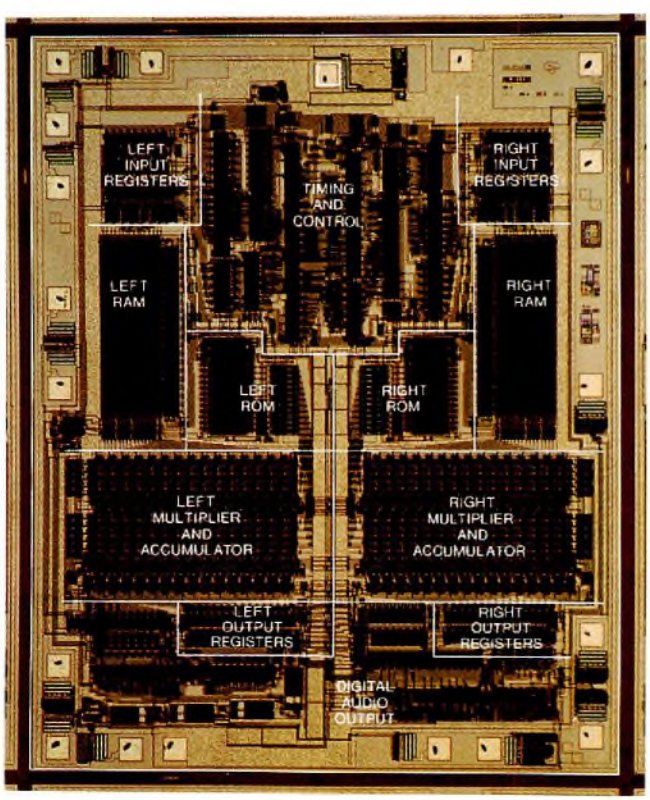


Fig.6 Improved tolerance to burst errors is a feature of the full-performance decoder comprising the SAA7210 and SAA7220. This figure shows the maximum burst error that can be corrected and the improved interpolation



Photomicrograph of the SAA7220 digital filter IC. Actual size 4,5 x 3,6 mm

REQUIREMENTS FOR THE LOW-PASS FILTER OF A CD PLAYER

There are several schools of thought for the low-pass filter of a CD player – all-analog, partly digital and predominantly digital – which has, to date, left the audio critics somewhat divided in their preferences. Our preference is for predominantly digital filtering followed by low-order analog filtering, a preference determined, not least, by the following considerations:

Pass-band ripple

Experiments (Ref.2) have shown that a discerning listener can detect a ripple of ±0,2 dB in the pass-band, so the maximum allowable ripple should be less than 0,2 dB. When designing our digital filter, we set out to produce a flat pass-band response with the pass-band extending beyond the audible frequencies, falling thereafter with a gentle roll-off around the Nyquist frequency (22,05 kHz).

Phase response

Most people can hear phase distortion (group delay variation) in an audio system as a change in the stereo 'picture'. This effect is worse when any phase distortion is accompanied by ripple in the pass-band. It is notoriously difficult, however, to correlate ripple and phase response to audibility thresholds. Experiments (see Ref.2) suggest that any audible effects are due, not to the ripple amplitude itself (many high-quality audio systems used to have ripple figures exceeding ±0,5 dB), but to the large number of ripples in the pass-band of a filter with steep roll-off.

Stop-band rejection

Many CD players have low-pass filters with out-of-band attenuation as high as 90 dB. Such high values are based more on the methods used to measure the performance of a player*, than on the stop-band rejection required. A more realistic attenuation figure, taking into account the peculiarities of audio equipment and the intermodulation distortion of audio amplifiers and tape decks, would be closer to 50 dB. Furthermore, extremely high stop-band rejection means a narrow transition band with steep roll-off which produces more ripples in the pass-band and makes the filter ring. The audible manifestation of steep roll-off, pass-band ripple and non-linear phase response are pre-echoes and post-echoes which can be readily observed on test burst sine waves**

To meet the foregoing requirements for pass-band ripple, phase response and stop-band of the low-pass filter, both an analog and a digital filter could suffice. However, the requirement for linear phase response would make the analog filter more expensive, and digital filters are renowned for their excellent impulse response. Add low thermal noise and long-term stability over a wide temperature range to the requirements, and the filter can best be digital and then with four-times oversampling (to shift any sidebands far beyond the audio band). Figure A compares the main types of low-pass filter in current use and Fig.B shows the noise levels in each.

* Popular audio magazines commonly publish *broadband* measurements taken on CD players. Owing to the presence of upper sidebands in PCM audio systems, it would be more meaningful to measure noise and distortion *over a 20 kHz bandwidth.*

** 400 Hz test signal acc. to Institut für Rundfunktechnik, Munich, Germany.

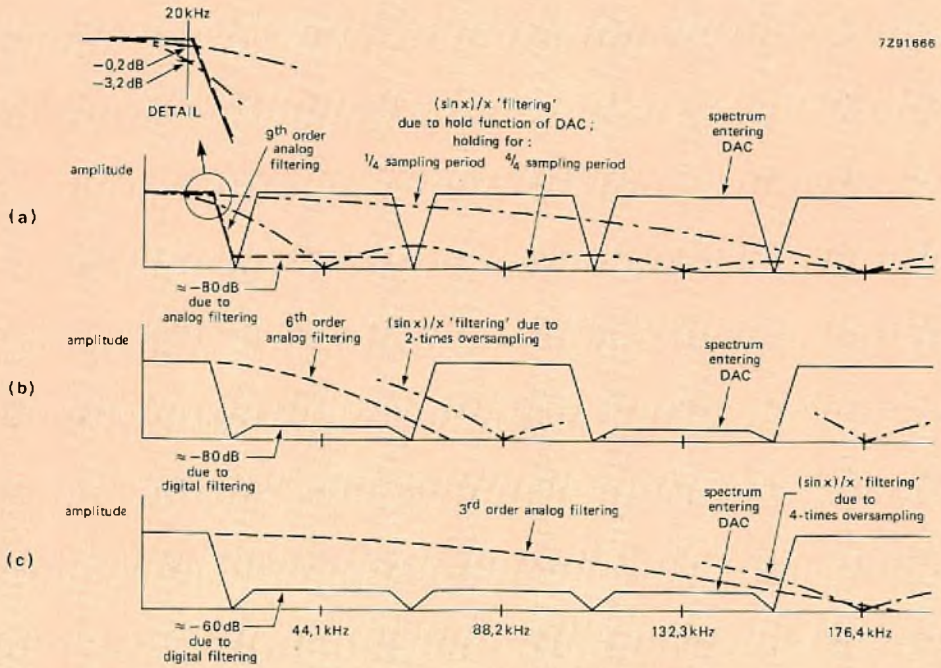
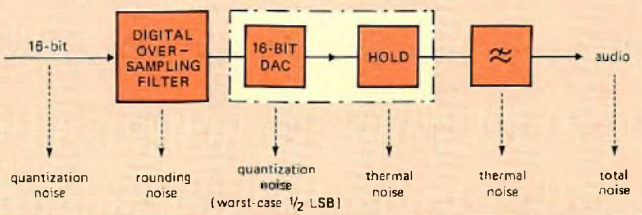


Fig.A Comparison of low-pass filtering in digital audio. (a) No oversampling, wholly analog filtering. To suppress the sidebands, a combination of a steep filter and the hold function of the DAC is used. To reduce the fall-off of frequency response at the top of the audio band, the hold function of the DAC operates for only ¼ the sampling period. Digital oversampling filters don't suffer from this effect. (b) Two-times oversampling, partly digital, partly analog filtering. (c) Four-times oversampling with predominantly digital filtering and simple analog filtering



WHOLLY ANALOG FILTERING	−98dB	n.a.	−98dB	<−110dB	−90dB to −100dB	−88,5dB to −93,8dB
PARTLY DIGITAL FILTERING, 2-TIMES OVERSAMPLING	−98dB	−101dB	−101dB	<−110dB	−100dB	−93,8dB
MOSTLY DIGITAL FILTERING, 4-TIMES OVERSAMPLING	−98dB	−104dB*	−104dB	<−110dB	−110dB	−95,6dB

* even lower values are possible with noise shaping

7291663

Fig.B Noise (theoretical values) in the D/A section of a CD player

LOW-PASS FILTERING

The low-pass filter of a CD player should attenuate any high frequency components while preserving the audio band intact. Any intermodulation products should be too weak for perception, and possibly even for measurement, see Table 2.

TABLE 2
Requirements for a low-pass filter for a CD player

pass-band	0 to 20 kHz
pass-band ripple	< ± 0.02 dB
transition band	20 to 24.3 kHz
stop-band rejection	>60 dB
linear phase response	
low thermal noise	
no ageing effects	
no adjustments	

The choice of low-pass filter in a CD player is very important, a choice that explains, in part, the difference in the sound reproduction of different players. Designs ranging from wholly analog to predominantly digital, with either two-times or four-times oversampling, can be found in current players, see panel. We favour predominantly digital filtering with four times oversampling followed by a low-order analog filter. This arrangement gives:

- linear phase response (at a much lower cost than with all-analog designs, and with no component adjustments necessary)
- flat pass-band
- optimum roll-off for excellent impulse response
- low noise
- long-term stability (no component ageing effects)
- smaller filter than discrete analog designs.

Digital filtering is probably the best-known feature of our approach to creating true high-fidelity sound. Our new digital filter circuit SAA7220 followed by a low-order analog filter produces no detectable sound colouration.

The digital filter is a (stereo) phase-linear four-times oversampling FIR filter with 120 filter coefficients. The (stereo) analog filter is an active simple third-order Bessel filter constructed with the TDA1542. Connected between the two is a 16-bit dual DAC TDA1541 operating at 176,4 kHz, see Fig.1. This DAC introduces no delay between the stereo channels – highly desirable for the listener of normal stereo sound, and essential when mixing audio signals, for example, to generate 4-channel audio or spatial stereo sound.

D/A CONVERSION

The TDA1541 dual DAC, located after the digital filter, uses a method of current division called *dynamic element matching* for high-accuracy binary-weighted currents with long-term stability. In addition, for the chip manufacturer, dynamic element matching eliminates resistor trimming. Bit switching is performed with a diode-transistor configuration for fast and accurate switching without the need for external deglitching circuitry.

The TDA1541 has been designed to also meet future trends in digital audio. For example, it is generally acknowledged that digital signal processing such as digital tone control and equalization increases the requirements for the dynamic range of the output signal. Eighteen-bit resolution can be achieved using the TDA1541 with four-times oversampling and noise shaping, because oversampling and noise shaping shift the quantization noise to above the audio band. As a result, a digital tone control using the TDA1541 can produce a frequency boost of about 12 dB while maintaining a 16-bit dynamic range over the whole audio band.

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The frame-transfer sensor

an attractive alternative to the tv camera tube

U. FEDDERN and S. ZUR VERTH

With the tremendous advances in semiconductor technology over the past few years, it was only a matter of time before the solid-state image sensor (SSIS) proved itself the equal of the venerable tv camera tube. Hardly surprising when you consider its intrinsic advantages.

It causes absolutely no picture geometry distortion for a start, and it has no burn-in or lag. It's also completely unaffected by magnetic fields, and highly resistant to knocks and vibration. Add to these qualities its highly stable characteristics, its low power consumption and operating voltage, its long life and its extremely light, compact construction, and you see why many tv-camera manufacturers are beginning to look on the SSIS as an attractive alternative to the camera tube.

Currently, it's use is limited to consumer, industrial and low-end broadcast applications: home video cameras, CCTV installations, industrial inspection equipment and ENG tv cameras. Rough treatment, adverse operating conditions and poor lighting are the norm in these applications, and it's here that the outstanding qualities of the SSIS really show up.

Two SSIS devices that offer exciting possibilities for the future are the new NXA1010 and NXA1020 frame-transfer sensors (Fig.1).

As their name suggests, these sensors operate on the frame-transfer (FT) principle, according to which each field of the complete picture frame is separately integrated within a photosensitive imaging region, transferred by CCD shift registers into a storage region during vertical blanking, and then clocked out serially to form the video signal during the subsequent field integration period.

The NAX1010 is the black/white version. The NXA1020 is essentially the same device with cyan, green and yellow stripe filters to allow its use in single-sensor colour tv cameras.

Outstanding features of these sensors are:

- *good blue sensitivity* since the polysilicon gate electrodes used for clocking the CCD registers cover only about 70% of the photosensitive area
- *high tolerance to overexposure* which allows the devices to be used in systems where highlights are likely to be encountered, for example, surveillance installations, pipe inspection systems and ENG colour cameras (with prismatic colour-separation and three B/W sensors).

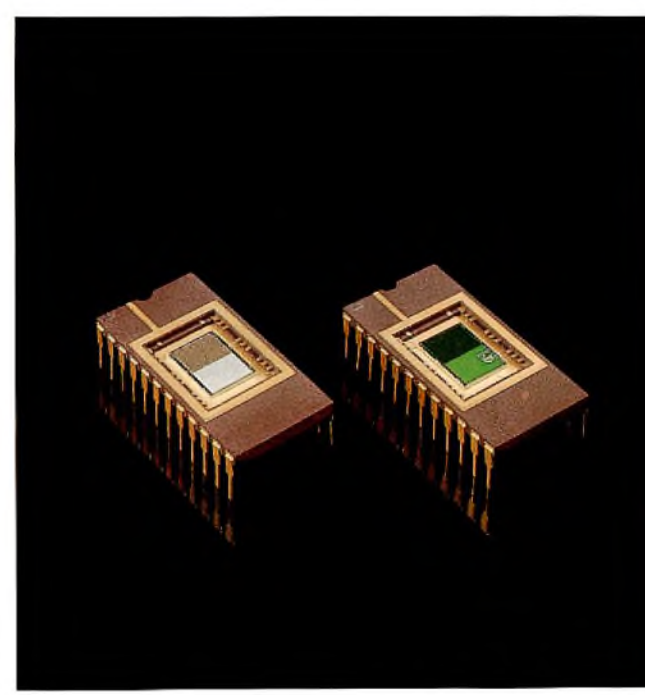

Fig.1 NXA1020 and NXA1010 frame-transfer sensors. The NXA1010 is the black/white version and the NXA1020 incorporates stripe filters for use in single-sensor colour tv cameras

ADVANCED MOS TECHNIQUES GIVE EXTRA HIGH PIXEL DENSITY

The NXA1010 takes advantage of the latest MOS techniques that have recently provided such spectacular advances in microprocessors, memories and other complex VLSI systems. In a super-8 picture format (½-inch camera tube) with an image diagonal of no more than 7,5 mm, the device can boast a total of 294 lines, each containing 604 pixels. With the CCIR standard of 576 lines (two interlaced fields each of 288 lines), this means effectively a total of 347904 pixels (each 10 μm x 15,6 μm) available exclusively for imaging.

What's more, thanks to the well established production techniques now available to manufacturers of MOS devices, we can form these pixels with a uniformity hitherto undreamed of.

Figure 2 shows the FT structure of the NXA1010. It's made up of a photosensitive imaging region next to a storage region and connected to it by 604 parallel CCD shift registers. These registers are separated by stop diffusions and their width defines the pixel width.

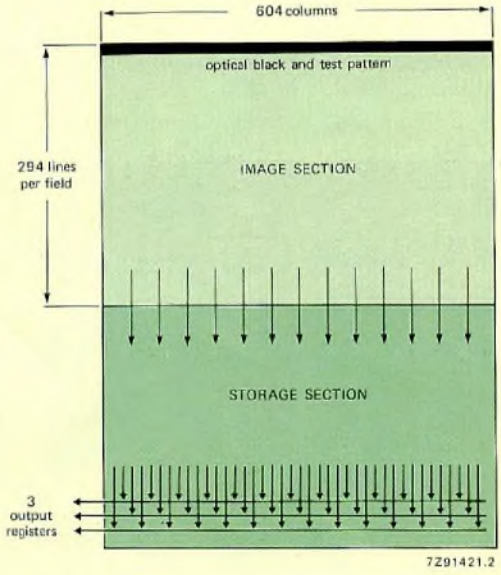

Fig.2 The NXA1010 frame-transfer structure comprises a photosensitive imaging region located next to a storage region and connected to it by parallel shift registers

A two-dimensional charge pattern representative of the image to be televised is integrated in the imaging region over the duration of a field and transferred to the storage region during the vertical blanking period.

Figure 3 shows the FT structure in more detail. The imaging and storage regions are practically identical, both being based on four-phase CCD shift registers (phases ϕ_1, ϕ_2, ϕ_3, and ϕ_4, subscript A in the imaging region and B in the storage region).

Charges generated by incident light in the imaging region collect beneath the gate electrodes with high potential. A low-potential electrode repels them, thus forming a boundary between charge packets to produce the individual pixels.

Figure 3 also shows the horizontal read-out structure. This comprises three 3-phase horizontal CCD shift registers controlled by gate electrodes ϕ_{1C}, ϕ_{2C} and ϕ_{3C}. The pixels in each line are read out in groups of three as indicated in Fig.3, selection being controlled by three transfer gates TG_1, TG_2, TG_3.

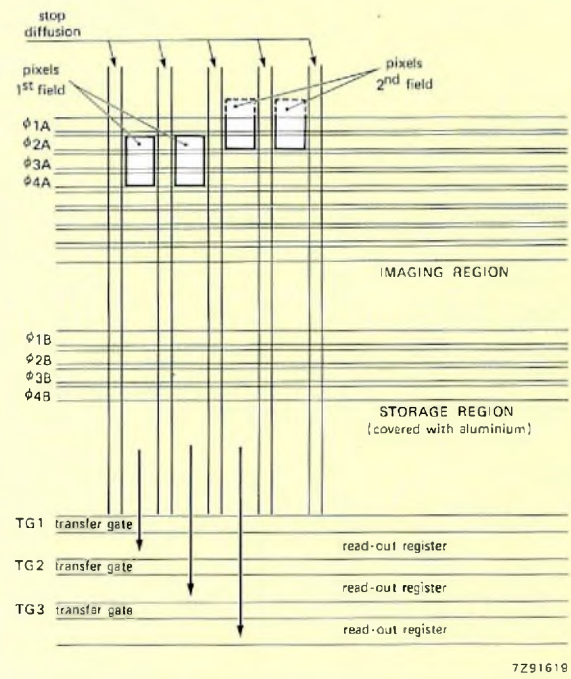

Fig.3 The imaging and storage regions are almost identical. Both incorporate four-phase CCD shift registers for vertical field transfer. Charge distribution into the three-phase horizontal readout registers is controlled by three transfer gates TG_1, TG_2 and TG_3

This provides two advantages. First, it allows a much higher horizontal pixel density than would a single read-out register, in which the finite width of the gate electrodes limits the minimum horizontal spacing between charge packets. With three shift registers, this spacing is effectively reduced threefold. Second, it allows selective separation of charge packets within each line and thus, with stripe filters over the imaging region, it allows the device to be used as a colour image sensor (NXA1020).

The first field is generated when the phases ϕ_2, ϕ_3 and ϕ_4 are high and ϕ_1 is low, Fig.4(a). ϕ_1 effectively forms a potential barrier separating the pixels in the first field. The charges generated by incident light then integrate beneath ϕ_2 to ϕ_4, centred on ϕ_3. So each pixel extends vertically over roughly three gate electrodes.

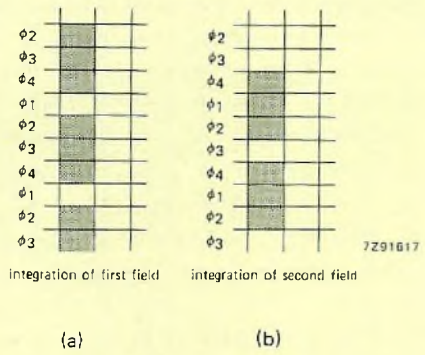

Fig.4 (a) For integration of the first field ϕ_2 to ϕ_4 are high, ϕ_1 is low forming a barrier between charge packets; (b) for integration of the second field, ϕ_4 to ϕ_1 are high, ϕ_3 is low

The potential distribution of the second field, and hence its position relative to the first field is shown in Fig.4(b). The second field is always displaced by two gate electrodes relative to the first field, with its charge patterns centred on ϕ_1, and with ϕ_3 forming the barrier between pixels, thus providing a perfectly interlaced frame structure.

FIELD TRANSFER

Figure 5 shows the transport process in the imaging and storage regions. At time t_0, the start of the first-field read-out from the imaging region, ϕ_1 is low and the charge is concentrated beneath ϕ_2 to ϕ_4 (as described above). At t_1, ϕ_2 goes low and the charge in each pixel concentrates beneath ϕ_3 and ϕ_4. At t_2, ϕ_1 goes high and the charge packets advance one gate electrode, spreading out beneath ϕ_3, ϕ_4 and the following electrode ϕ_1. In the next step, at t_3, ϕ_3 goes low compressing the charge packets beneath ϕ_4 and ϕ_1, and at t_4, ϕ_2 goes high allowing the charge packets to again advance one gate electrode.

This process continues in both the imaging and storage regions until all the charge packets have transferred to the storage region.

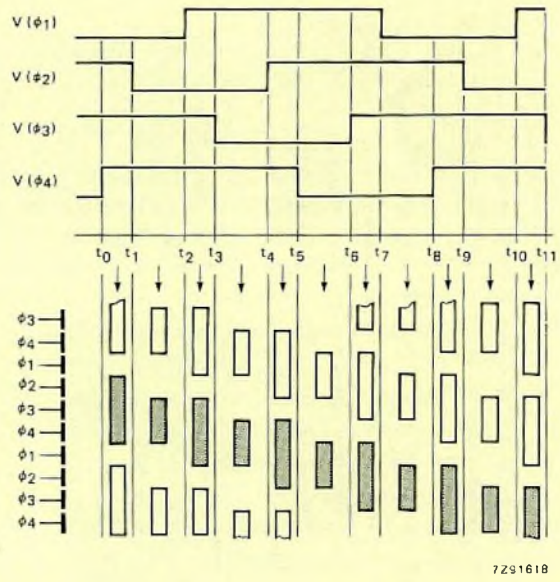

Fig.5 Transport process in the imaging and storage regions

HORIZONTAL READ-OUT

The storage region is read out line-by-line while integration is taking place in the imaging region. During successive horizontal-blanking periods, the vertical shift-registers in the storage region advance the stored image one line, so that at the end of the blanking period, the next line is ready to be transferred to the horizontal read-out registers via the three transfer gates.

The read-out registers are provided with an output stage (source follower) with a sensitivity of 3,5 μV per electron.

PULSE SEQUENCES FOR THE NXA1010/1020

Figure 6 shows the drive-pulse sequence and line numbering for field-transfer in the NXA1010/1020 (for the PAL/CCIR tv standard). To show both fields in the same figure, the second field is shown below the first with the appropriate tv line numbering above it. As the figure shows, the field-transfer process occupies about 30% of the tv-standard vertical blanking period.

The CCD lines used for image recording are distinguished in the figure by hatching and by the letter 'V' above them.

The read-out time for the first field extends from tv lines 23 to 310, and for the second field from tv lines 335 to 623. Lines 624 to 3, and lines 311 to 315 are all shifted out but not transmitted. Lines 314 and 2 serve as black-level reference lines, and lines 312, 624 and 625 are all reserved for testing the sensor during production.

Figure 7 shows the field-transfer pulses in greater detail, as well as the transfer-gate pulses and the horizontal read-out pulses ϕ_{1C}, ϕ_{2C} and ϕ_{3C}. Transfer gates TG_2 and TG_3 are connected electrically, so only the former's pulse sequence is shown.

Since the first field is shifted relative to the second by half a line, to bring it into the correct position for transfer into the storage region, half a clock period must be added at the start and end of its ϕ_A pulses (Fig.7(a)).

Transfer gate TG_1 is closed during the waiting period, i.e. the period between transfer of a field into the storage region and the start of readout of that field (see Figs 6 and 8).

The last gate electrode in the storage region is ϕ_{3B}, and this is followed by TG_1 which controls transfer of the signal charge from the storage region into the upper horizontal read-out register. During the horizontal blanking period, pulses ϕ_{3B}, TG_1, TG_2, in combination with ϕ_{1C} to ϕ_{3C} (Fig.9) sort the signal charge into the three horizontal read-out registers.

At the end of each field read-out, all residual charge in the storage region must be removed before the next field is entered. This is done by keeping TG_1 open after the field has been clocked out and continuing to clock the horizontal registers (phases ϕ_C) until the next field is ready to be read out.

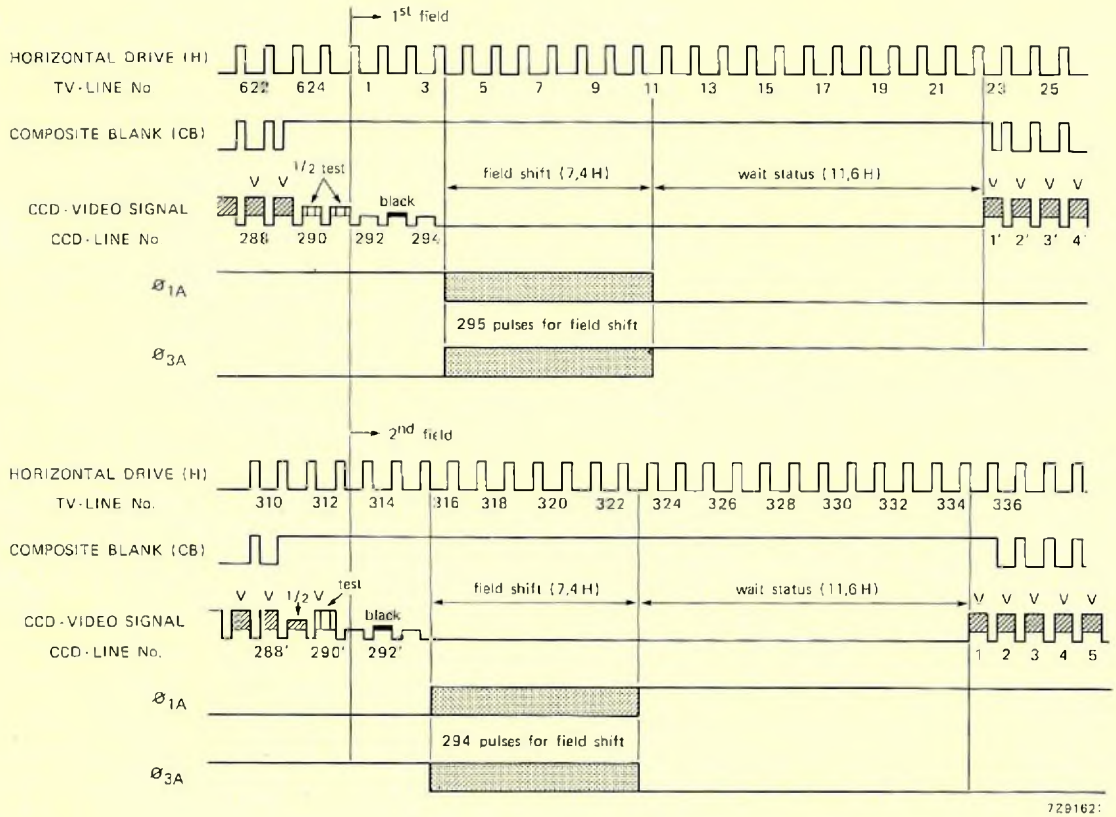

Fig.6 Drive-pulse sequence and line numbering for field transfer (PAL/CCIR tv standard). Of the ϕ_A pulses, only ϕ_{1A} and ϕ_{3A} are shown since these pulses change sign between the first and second fields. The actual details of the ϕ_A pulses can be found in Fig.5

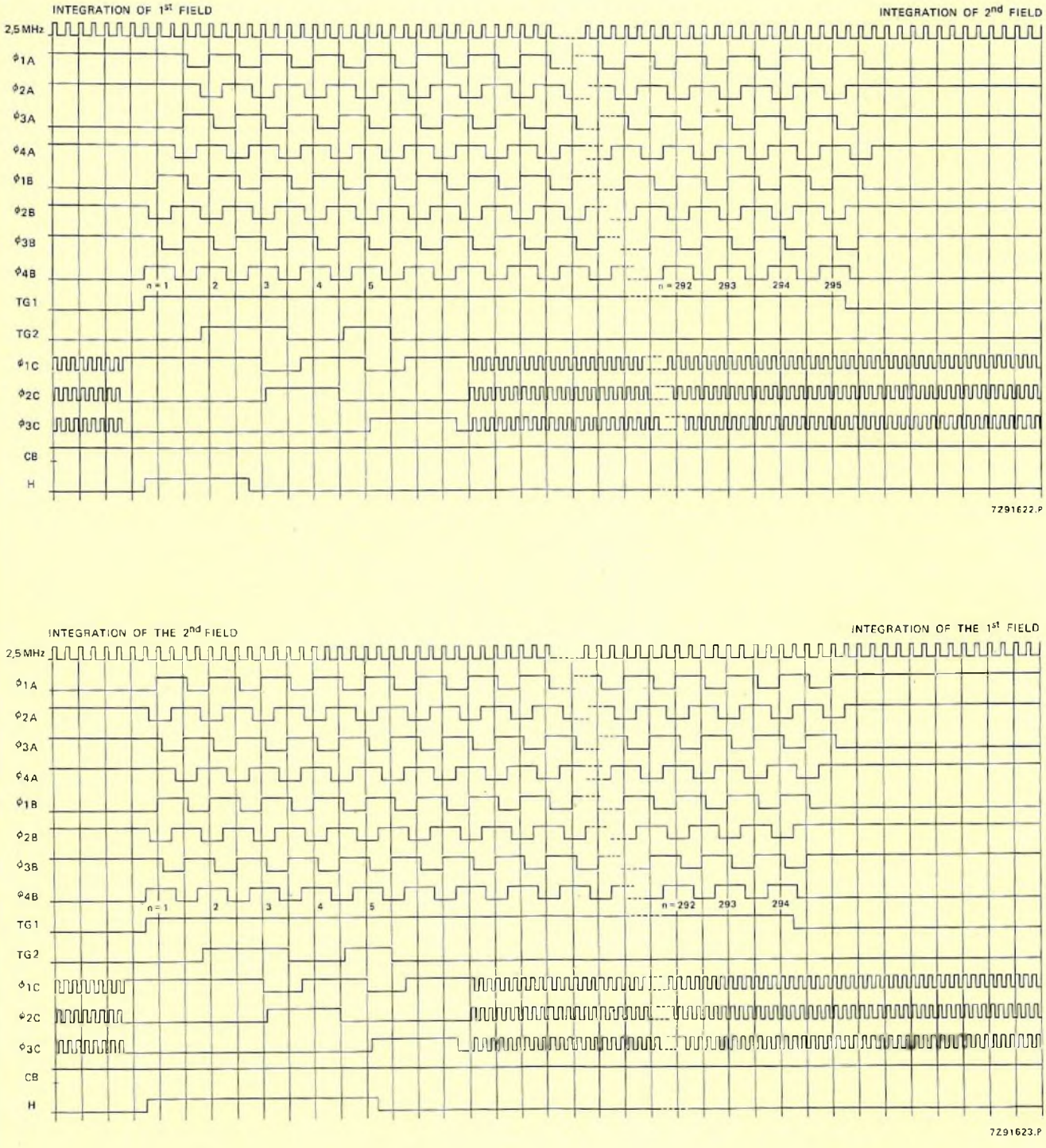

Fig.7 Field-transfer pulses, transfer-gate pulses and horizontal read-out pulses $\phi 1C$, $\phi 2C$ and $\phi 3C$. Transfer gates TG_2 and TG_3 are connected electrically, so only the former's pulse sequence is shown

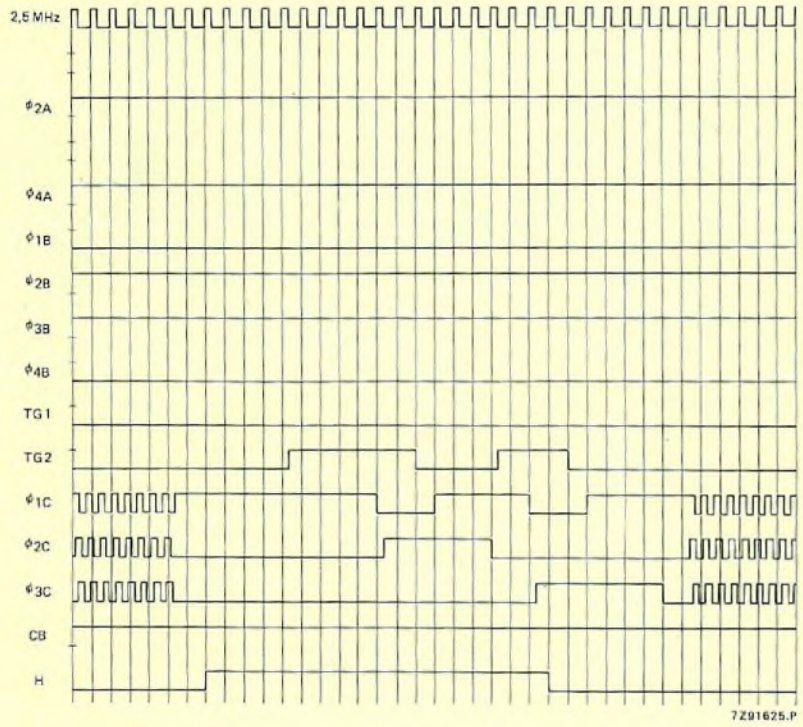

Fig.8 Transfer gate TG_1 is closed during the waiting period, i.e. the period between field transfer into the storage region and the start of readout of that field

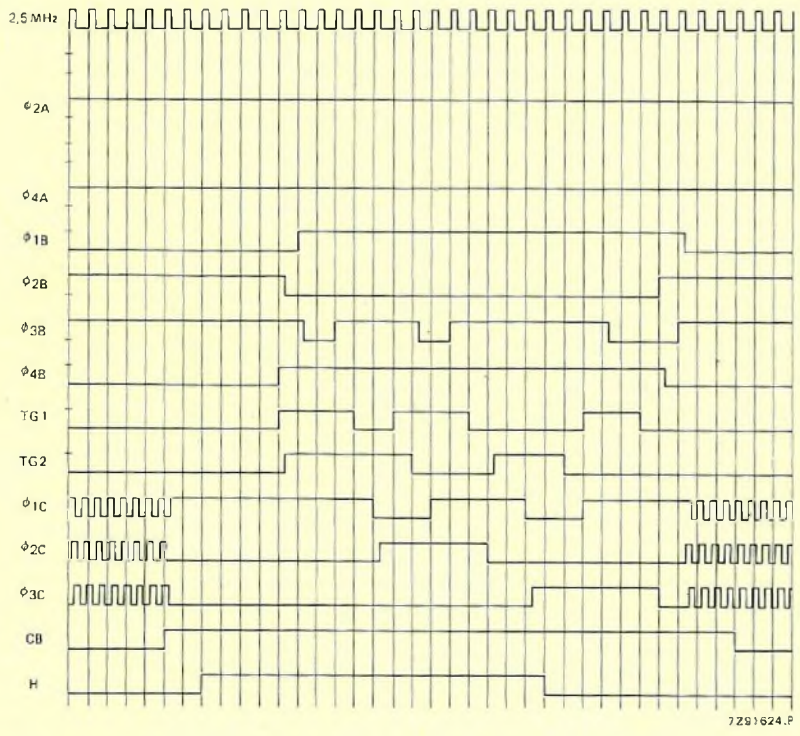

Fig.9 During the horizontal blanking period, pulses ϕ_{3B}, TG_1, TG_2 and ϕ_{1C} to ϕ_{3C} sort the signal charge into the three horizontal read-out registers

DRIVE CIRCUIT FOR THE NXA1010/1020

Figure 10 shows a circuit for providing the pulse sequences needed to drive the NXA1010/1020.

An SAA1043 sync-pulse generator, provides pulses for the three tv standards, namely PAL, SECAM and NTSC. These include vertical and horizontal blanking, and black-level clamping. It also provides other signals essential for tv camera operation, and can be triggered externally for operation with, for example, a VCR or computer.

The sync-pulse generator drives an SAD1007 pulse-pattern generator, developed specifically for the NXA1010/1020. It provides all the clock signals except the pulses for the horizontal read-out registers, and its use avoids the need to develop complex circuitry for driving the NXA1010/1020.

Fast clock pulses for the three horizontal read-out registers are generated by a 'pixel oscillator', a TDA4302 square-wave oscillator delivering three 3,9 MHz pulse trains with a 120° phase difference between them.

The output levels from the pulse-pattern generator and from the pixel oscillator are too low to drive the shift registers directly. Extra driver ICs are therefore needed to boost the signals: for the pixel oscillator – one TDA4305, and for the pulse-pattern generator – two TDA4301 ICs (one for the ϕ_A pulses, one for the ϕ_B pulses). The TDA4301 ICs are also used to boost the transfer-gate pulses.

During horizontal blanking, the pixel oscillator is inhibited, and slower pulses derived from the pulse-pattern generator are applied to the pixel-oscillator output, and hence, via the TDA4305, to the transfer gates and horizontal gate electrodes to sort the charge packets into the three horizontal read-out registers.

Finally, the d.c. offset for the drive pulses can be provided by a circuit using discrete components, or better still, by a TDA4304 d.c. control IC.

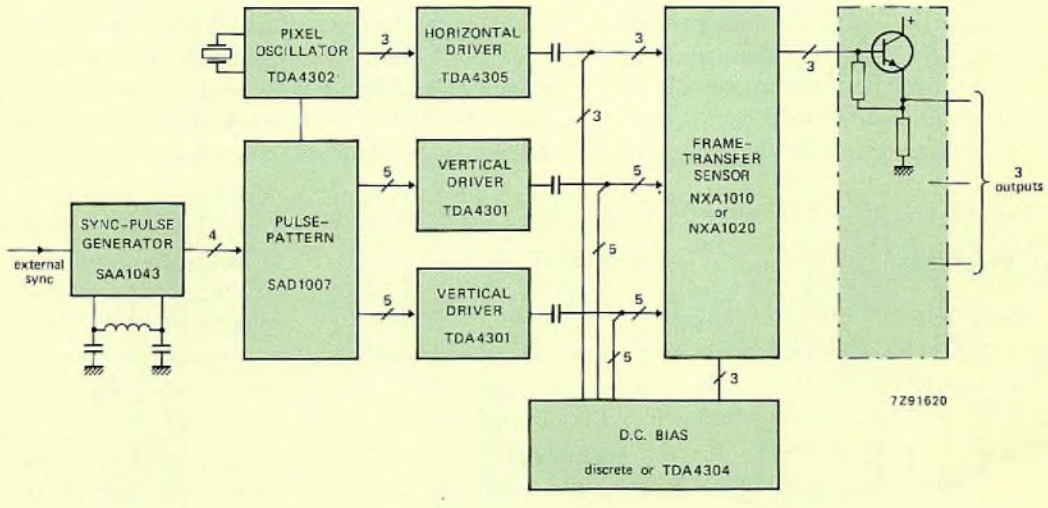

Fig.10 Control circuitry for driving the NXA1010/1020 frame-transfer sensors

DMA Interface for 68000 systems

GUY THOMSEN and BART VERNOOIJ

Direct memory access (DMA) is often used to improve I/O operations and increase system throughput in applications requiring frequent transfers of blocks of data between system memory and peripherals. DMA eliminates the restriction placed on system operation that would occur if the CPU itself had to carry out these transfers.

A major requirement of DMA controllers is speed, since a slow controller will inevitably slow down system operation and reduce efficiency – particularly important in 68000-based systems which already operate at speeds in excess of 12 MHz. This requirement led to the development of the SCB 68430, a high-speed single-channel DMA interface (DMAI, Fig.1) that's completely compatible with the 68000's architecture and bus structure.

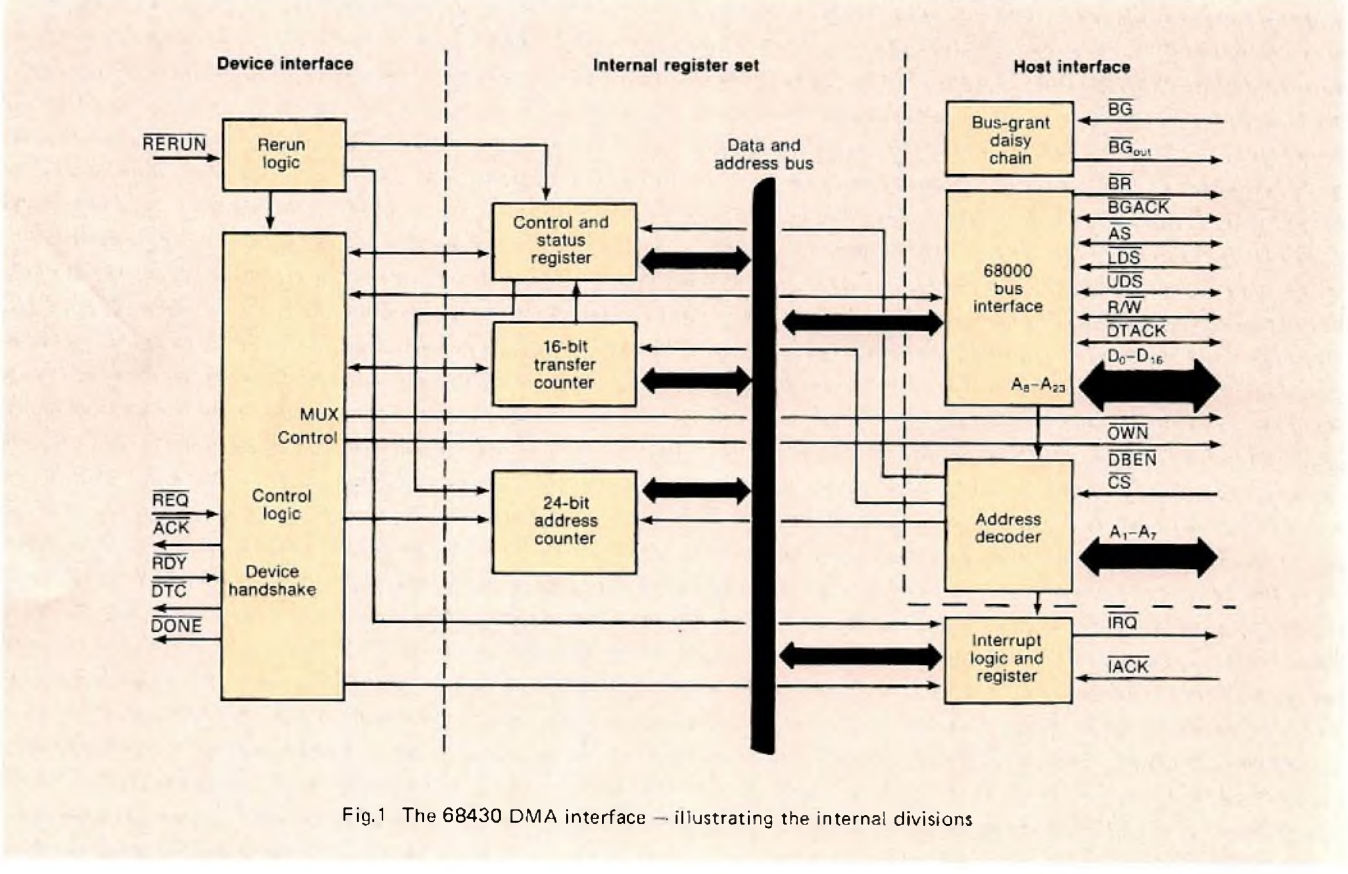

Fig.1 The 68430 DMA interface – illustrating the internal divisions

TABLE 1
Transfer rates for the SCB68430

clock frequency (MHz)	mode	from memory to device (Mbytes/s)	mode	to memory from device (Mbytes/s)	read 32-bit word over VMEbus (Mbytes/s)	write 32-bit word over VMEbus (Mbytes/s)
10	bytes	2.5	byte	2	10	8
10	word	5	word	4	10	8
10	long word	5	long word	4	10	8
12.5	byte	3.125	byte	2.5	12.5	10
12.5	word	6.25	word	5	12.5	10
12.5	long word	6.25	long word	5	12.5	10

TABLE 2
Address map for the SCB8430

address bits								register		mode	affected by reset
7	6	5	4	3	2	1	0	name	acronym		
d	d	0	0	0	0	0	0	channel status register	CSR	R/W	yes
d	d	0	0	0	0	0	1	channel error register	CER	R	yes
d	d	0	0	0	0	1	0	reserved			
d	d	0	0	0	0	1	1	reserved			
d	d	0	0	0	1	0	0	device control register	DCR	R/W	yes
d	d	0	0	0	1	0	1	operation control register	OCR	R/W	yes
d	d	0	0	0	1	1	0	sequence control register	SCR	R/W	yes
d	d	0	0	0	1	1	1	channel control register	CCR	R/W	yes
d	d	0	0	1	0	0	0	reserved			
d	d	0	0	1	0	0	1	reserved			
d	d	0	0	1	0	1	0	memory transfer counter high	MTCH	R/W	no
d	d	0	0	1	0	1	1	memory transfer counter low	MTCL	R/W	no
d	d	0	0	1	1	0	0	memory address counter high	MACH	R/W	no
d	d	0	0	1	1	0	1	memory address counter middle high	MACMH	R/W	no
d	d	0	0	1	1	1	0	memory address counter middle low	MACML	R/W	no
d	d	0	0	1	1	1	1	memory address counter low	MACL	R/W	no
d	d	0	1	d	d	d	d	reserved			
d	d	1	0	0	0	d	d	reserved			
d	d	1	0	0	1	0	0	reserved			
d	d	1	0	0	1	0	1	interrupt vector register	IVR	R/W	yes
d	d	1	0	0	1	1	0	reserved			
d	d	1	0	0	1	1	1	interrupt vector register	IVR	R/W	yes
d	d	1	0	1	0	d	d	reserved			
d	d	1	0	1	1	0	0	reserved			
d	d	1	0	1	1	0	1	channel priority register	CPR	R/W	no
d	d	1	0	1	1	1	0	reserved			
d	d	1	0	1	1	1	1	reserved			
d	d	1	1	d	d	d	d	reserved			

To attain high speed, initial DMAI fabrication was in ISL (integrated Schottky logic). But now it's manufactured in even faster I^2L (integrated injection logic), making it the fastest DMA controller while still maintaining software compatibility with other DMA controllers (68440 and 68450) in the 68000 family.

This article describes the operation of the 68430 DMAI and gives an application example with the 68681 DUART (Dual Universal Asynchronous Receiver/Transmitter).

The main function of the DMAI is to transfer data in 8, 16 or 32-bit units between system memory and a peripheral. Users can choose to transfer data either in single-cycle (cycle-stealing) mode, allowing the system CPU to continue with other tasks, or in burst mode, which allows up to 64 Kbytes to be transferred in one block. Table 1 lists typical data transfer rates for the DMAI as a function of clock frequency. Note that at any clock frequency, 32-bit data transfer is at least twice as fast over the VMEbus than over the 68000 bus. Whatever the operating speed and whichever bus is used, the DMAI helps eliminate the memory-to-I/O bottlenecks that occur frequently in conventional memory-handling systems.

THE INTERNAL REGISTER SET

Contained within the internal register set are the control and status registers, two programmable counters (memory address counter and memory transfer counter) and an interrupt vector register (Fig.2). Inactive registers (sequence control and channel priority registers), have been added for compatiblity with the other 68000 DMA controllers. Also for compatibility, the control and status bits are mapped into positions equivalent to those in the other DMA controller register sets. Each register can be accessed with an 8-bit address. Furthermore, the registers are arranged in groups each of which can be accessed using a single word or long-word address.

Registers used in data transfer

Device control register

The External Request Mode bit of the *device control register* is used to select burst or cycle-stealing mode operation. In burst mode a peripheral may request a multiple-data-operand transfer over consecutive bus cycles. Operand transfer in cycle-stealing mode, however, is requested by generating a falling-edge signal on $\overline{\text{REQ}}$. The controller services a transfer request by arbitrating for the bus, obtaining it, and notifying the peripheral by asserting the $\overline{\text{ACK}}$ output.

Operation control register

Transfer direction and operand size are defined using the *operation control register*. Bidirectional transfers can be made between system memory and peripheral, with the bits defining the operand size determining which data strobes ($\overline{\text{UDS}}$ and $\overline{\text{LDS}}$ – upper and lower data strobes) are required to increment the memory address counter correctly after each transfer. A DMAI operand can be a byte, a 16-bit word, a long word (32-bit transfer) or a double word (two separate word transfers).

Channel control register

The *channel control register* contains the Start Operation, Software Abort and Interrupt Enable bits. The controller starts to operate when the Start Operation bit is set and stops when the Software Abort bit is set, placing the controller in the idle state. If the Channel Operation Complete (COC) bit is set in the channel status register, the Enable Interrupt will generate an Interrupt Request. When an operation ends, the COC bit is always set, regardless of whether the operation was successful or not and it must be cleared before the next channel operation can start.

Channel status register

Controller status is indicated by the *channel status register*. The COC bit as well as the Normal Device Terminate (NDT), and Error (ERR) bits are cleared by writing a logic 1 to the appropriate bit positions. Writing a logic 0 to these bit positions will have no effect.

When a peripheral initiates a channel operation, the Channel Active bit is set and remains set until the operation ends, at which point the NDT bit is set. Using the $\overline{\text{ACK}}$ signal, the DMAI indicates completion of the operation to the peripheral. If the peripheral no longer requires use of the DMAI, it asserts the $\overline{\text{DONE}}$ (bidirectional active-LOW) signal while the acknowledge is still active.

As with the COC bit, the NDT bit must be cleared before another operation can begin. Reading the Ready Input State (RIS) bit will give the state of the $\overline{\text{RDY}}$ (ready) input, a logic 0 if $\overline{\text{RDY}}$ is LOW and a logic 1 if it is HIGH. Write and reset operations will have no effect on RIS.

Channel error register

If operation is terminated by an error then the ERR bit indicates this fact while the contents of the *channel error register* define its source. For example, 00000 indicates that there has been no error and 01001 indicates that there was a bus error in the last bus cycle generated by the controller. Clearing bit 12 of the status register clears the channel error register contents.

DEVICE CONTROL REGISTER (DCR)

	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT09	BIT08
DCR	EXTERNAL REQUEST MODE 0 = BURST 1 = CYCLE STEAL	NOT USED (0)	NOT USED (1)	NOT USED (1)	NOT USED (*)	NOT USED (0)	NOT USED (0)	NOT USED (0)

* Should be programmed as '0' for SIZE (OCR[5:4]) = 00 and as '1' otherwise. When read, the value of this bit is OCR[5]. OR. OCR[4].

OPERATION CONTROL REGISTER (OCR)

	BIT07	BIT06	BIT05	BIT04	BIT03	BIT02	BIT01	BIT00
OCR	DIRECTION 0 = MEM TO DEV 1 = DEV TO MEM	NOT USED (0)	OPERAND SIZE 00 = BYTE 01 = WORD (16 BIT) 10 = LONG WORD 11 = WORD (32 BIT) *		NOT USED (0)	NOT USED (0)	NOT USED (1)	NOT USED (0)

* Long word and 32 bit word modes are not supported by 68440. 32 bit word mode is not supported by 68450.

SEQUENCE CONTROL REGISTER (SCR)

	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT09	BIT08
SCR	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (1)	NOT USED (0)	NOT USED (0)

CHANNEL CONTROL REGISTER (CCR)

	BIT07	BIT06	BIT05	BIT04	BIT03	BIT02	BIT01	BIT00
CCR	START 0 = NO 1 = YES	NOT USED (0)	NOT USED (0)	SOFTWARE ABORT 0 = NO 1 = YES	INTERRUPT ENABLE 0 = NO 1 = YES	NOT USED (0)	NOT USED (0)	NOT USED (0)

CHANNEL STATUS REGISTER (CSR)

	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT09	BIT08
CSR	CHANNEL OPERATION COMPLETE 0 = NO 1 = YES	NOT USED (0)	NORMAL DEVICE TERMINATE 0 = NO 1 = YES	ERROR 0 = NO 1 = YES	CHANNEL ACTIVE 0 = NO 1 = YES	NOT USED (0)	NOT USED (0)	READY INPUT STATE 0 = LOW 1 = HIGH

CHANNEL ERROR REGISTER (CER)

	BIT07	BIT06	BIT05	BIT04	BIT03	BIT02	BIT01	BIT00
CER	NOT USED (0)	NOT USED (0)	NOT USED (0)	ERROR CODE 00000 = NO ERROR 01001 = BUS ERROR 10001 = SOFTWARE ABORT				

CHANNEL PRIORITY REGISTER (CPR)

	BIT07	BIT06	BIT05	BIT04	BIT03	BIT02	BIT01	BIT00
CPR	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)

MEMORY ADDRESS COUNTER (MAC)

MAC	MACH	MACMH	MACML	MACL

MEMORY TRANSFER COUNTER (MTC)

MTC	MTCH	MTCL

INTERRUPT VECTOR REGISTER (IVR)

IVR								

7Z95300

Fig.2 The register set

Memory address counter

Depending on the direction of transfer, a 32-bit *memory address counter* specifies either the memory location of the first operand to be transferred or the memory location to which it has to be transferred. This counter must first be initialized so that when transferring data it will increment correctly, according to the operand length. Only the least significant 24 bits are implemented in the controller with MACH (the most significant byte of the memory address counter) just to provide compatibility with the other 68000 family DMA controllers. Reading MACH gives HEX '00' while writing to MACH has no effect on chip operation.

Memory transfer counter

The programmer defines the number of operands to be transferred using the 16-bit *memory transfer counter*. Before starting a data-block transfer, the counter must be initialized and will then decrement automatically. Upon reaching zero, channel operation is terminated and the COC bit in the channel status register is asserted.

Interrupt vector register

The *interrupt vector register* contains the memory location to be put on the data bus in the event of an interrupt acknowledge from the controlling microprocessor. Register contents are initialized to HEX '0F' by Reset, and this value is fixed until the register is programmed by the controlling processor. The DMAI uses the most significant 7 bits of this programmed value. If operation terminates normally, the LSB will be a logic 0 and if it terminates because of an error, the LSB will be a logic 1.

For compatibility with other DMA controllers in the 68000 family, the interrupt vector register has two addresses – one for normal termination and the other for when an error occurs. If program compatibility with the other DMA controllers is required, the value written to the normal address must have a logic 0 as its LSB, and the value for the error address is the same except for the logic 1 in the LSB position.

GAINING CONTROL OF THE SYSTEM BUS

When a valid data transfer request is received from a peripheral, the DMAI arbitrates for and acquires control of the system bus. It does this by asserting its Bus Request ($\overline{BR}$) line, which tells the processor that an external device requires use of the bus. Since the processor has lower priority than the external devices, it relinquishes control of the bus after completing the last bus cycle it started. The processor then puts the bus up for external arbitration by asserting its own Bus Grant output. This signal can be routed through the daisy chain provided by the DMAI or through any other priority-encoded network.

The Bus Grant signal then enables the $\overline{BG}$ input of the DMAI which becomes the next bus master. The DMAI first waits until the Address Strobe ($\overline{AS}$), Data Transfer Ackowledge ($\overline{DTACK}$), and the Bus Grant Acknowledge ($\overline{BGACK}$) signals become inactive before assuming acquisition of the bus by asserting its own $\overline{BGACK}$ line. Then after de-activating its $\overline{BG}$ line, the DMAI commences data transfer. Finally, upon completion of data transfer, the DMAI releases the bus by de-activating its $\overline{BGACK}$ line.

In burst-mode transfer, an active-LOW request detected by the DMAI after it has begun operation initiates the bus arbitration cycle. But if a peripheral de-activates its $\overline{REQ}$ line at least one clock cycle before the DMAI asserts $\overline{BGACK}$, the DMAI de-activates its Bus Request line and will therefore not try to become the bus master.

The Interrupt Enable bit (bit 3 in the channel control register) determines whether interrupts are generated by the DMAI. When the bit is set, an Interrupt Request ($\overline{IRQ}$) is generated if the COC bit is set. With an interrupt request pending and the Interrupt Acknowledge ($\overline{IACK}$) asserted, the DMAI returns an interrupt vector on the data bus.

TRANSFERRING DATA

A peripheral requests service by asserting its Request line. The DMAI can then service the peripheral in either the burst or cycle-stealing mode depending on the state of the External Request Mode bit.

Data is transferred between the memory and peripheral during the data transfer phase as shown in Fig.3. All transfers are single-cycle except for long-word operands which are moved as two 16-bit words, and therefore take two cycles. A single address protocol is used in data transfer: the DMAI addresses memory via the bus address lines, and the peripheral is addressed implicity via the Acknowledge ($\overline{ACK}$) line.

When a Request is generated, the DMAI acquires the bus and asserts its $\overline{ACK}$ output to inform the peripheral that a transfer is about to begin. It also asserts all 68000 bus control signals required for the transfer (Fig.4) and holds them until the peripheral responds with $\overline{RDY}$ – an active-LOW input that indicates that the data has been stored or transmitted on the bus. If the peripheral connected is fast enough, $\overline{RDY}$ can be tied LOW which would indicate that the peripheral is always ready.

During transfers to a peripheral, data is valid when $\overline{DTACK}$ is asserted and remains valid until the data strobes are de-activated. For transfers in the opposite direction, the data must be valid on the bus before the DMAI asserts the required data strobes. The peripheral indicates that the data is valid by asserting its $\overline{RDY}$ line. Then the DMAI

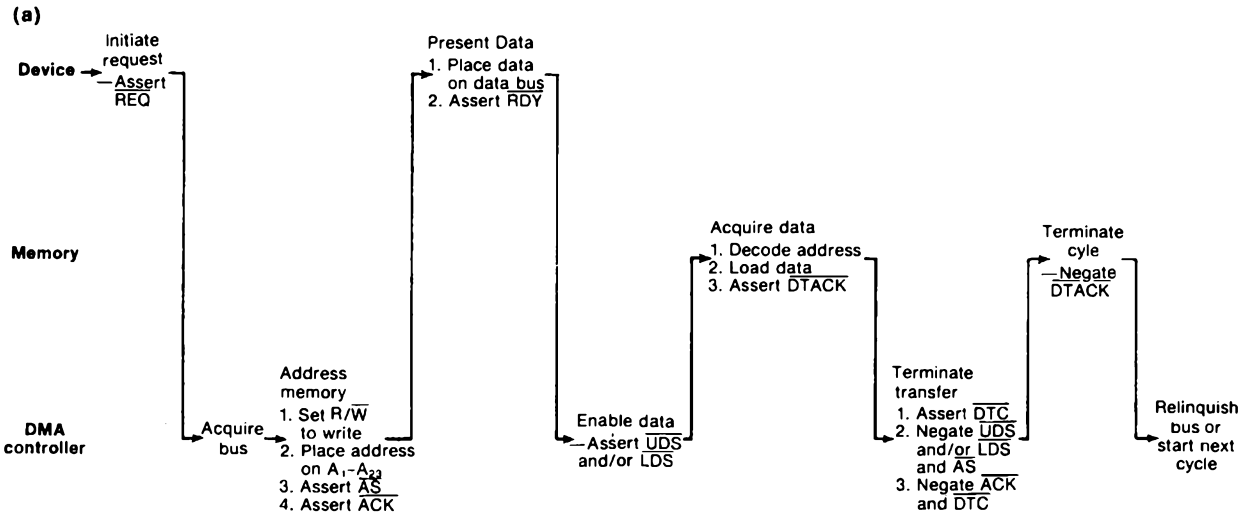

Fig.3 Data transfer between memory and peripheral

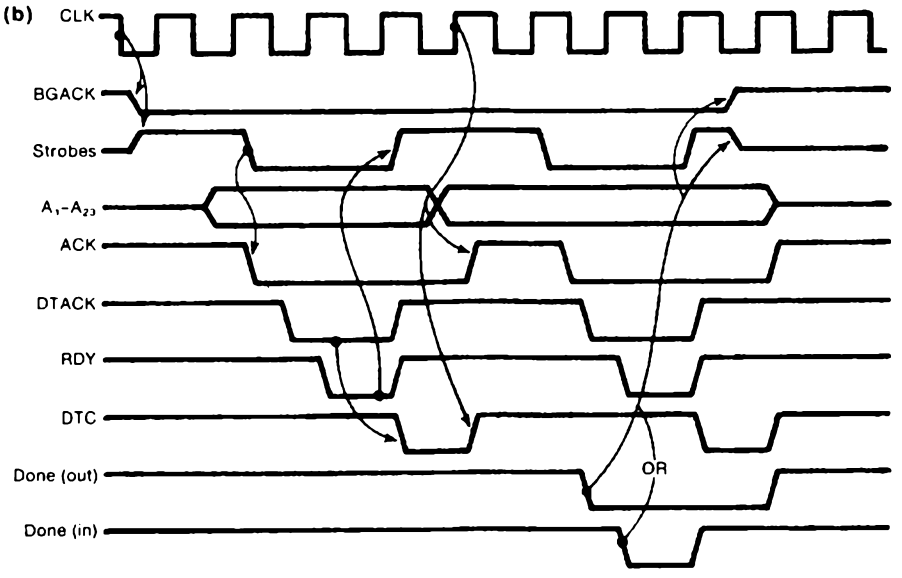

Fig.4 Bus control signals during memory-to-peripheral transfer

asserts the strobes and holds them until the memory accepts the data, indicated on $\overline{\text{DTACK}}$. The DMAI then deactivates the data strobes by asserting $\overline{\text{DTC}}$. This is an active-LOW output that the DMAI asserts to indicate that the requested data transfer is complete. In a peripheral-to-memory transfer, it indicates that the data supplied by the peripheral has been stored.

During transfers from a peripheral, $\overline{\text{DTC}}$ informs the peripheral that data is present on the bus and should be latched. $\overline{\text{DTC}}$ is not asserted if the $\overline{\text{RERUN}}$ input terminates the transfer. To indicate to the peripheral that as a result of the transfer the DMAI's operation is complete, it asserts and negates the $\overline{\text{DONE}}$ signal in synchronization with the acknowledge output of the last operand.

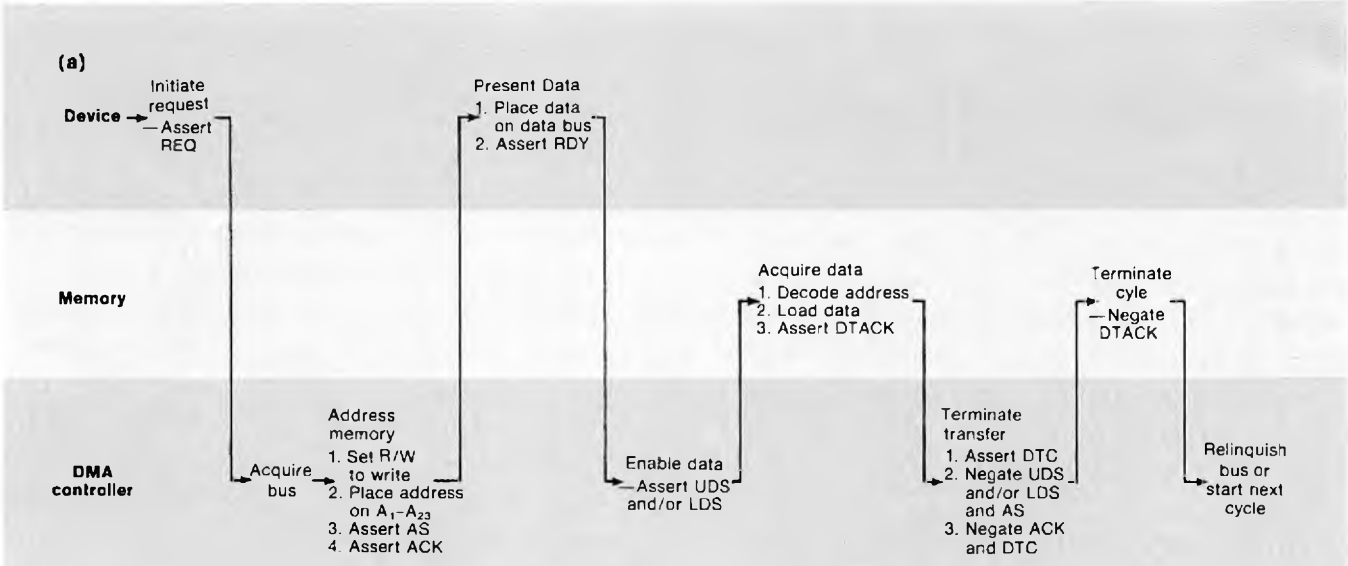

Fig.5 Data transfer from peripheral to memory

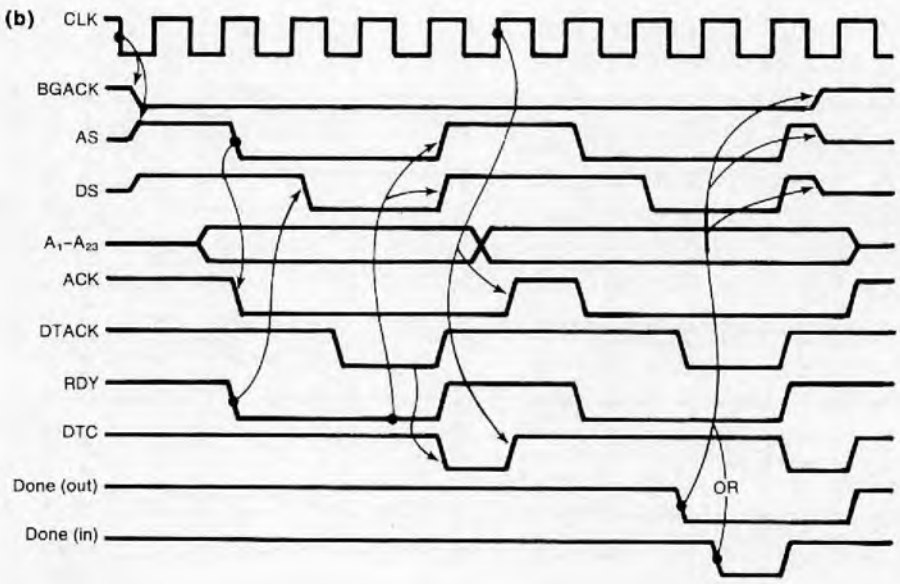

Fig.6 Bus control signals during peripheral to memory transfer

Direct memory access for dual UART

In communication applications, the DMAI can provide direct memory access for the 68681 dual universal asynchronous receiver-transmitter (DUART), a single chip with two fully independent channels for communication.

The DMAI has all the necessary signals to interface with the DUART as both system master and peripheral (Fig.5). U_1 to U_5 are required for address and data line demultiplexing, even though the DMAI drives the 68000 bus directly. U_1 is an output buffer for the register address and together with U_2 and U_3, drives memory address signals during DMA operation. In a register read/write cycle, octal bus transmitter/receivers U_4 and U_5 act as bidirectional data buffers.

All the other circuitry shown in Fig.5 is used in interfacing with the DUART. Address lines to it come from multiplexer U_6 and the output is selected by the $\overline{OWN}$ signal from the DMAI, asserted during transfers.

Making a path to the UART

During system and DMA accesses, multiplexer U_{10} is used to gate the DUART's $\overline{CS}$ and R/$\overline{W}$ data path control signals. ANDed signals from U_8 and U_9 also enable the correct transmitter/receiver buffer for data to or f· ·n the DUART through U_{10}. With DMAI operation, the R/$\overline{W}$ is inverted for the DUART, since a read from the memory is a write to the receiver/transmitter. For host access, the system requires the $\overline{DTACK}$ signal to be generated at the correct time for gating onto the bus by U_8 and U_9.

The DUART's interrupt line ($\overline{INTR}$) is used to request DMA operation via the interface's $\overline{REQ}$ input. Before the DUART or the DMAI can transfer data, both must be initialized. For the DUART, this involves setting the communication parameters (see Table 3). In this application, the DMAI's interrupt vector register is also loaded during initialization. Channel A is primarily an output port to a display, and channel B is an input port from a microcontroller. Information is transferred along both channels in block format. When a DMA transfer is in progress, the $\overline{DTACK}$ signal from the $\overline{DUART}$ is used as the $\overline{RDY}$ signal for the interface.

When information has to be transferred, the system software sets a bit in memory and calls the driver (see Table 4). The driver reads the bit to determine which channel to use. It will then either set or reset the MSB of the DUART's address (flip-flop U_7). A simple software driver can be used to load the interface because of its straightforward register-set arrangement. For example, the transfer driver needs only three instructions to set the operand transfer length and the system buffer address, and then to load the transfer type and the start bit. The three variables required for that sequence can be locations in the system memory that can be updated or changed as necessary by the supervisory program.

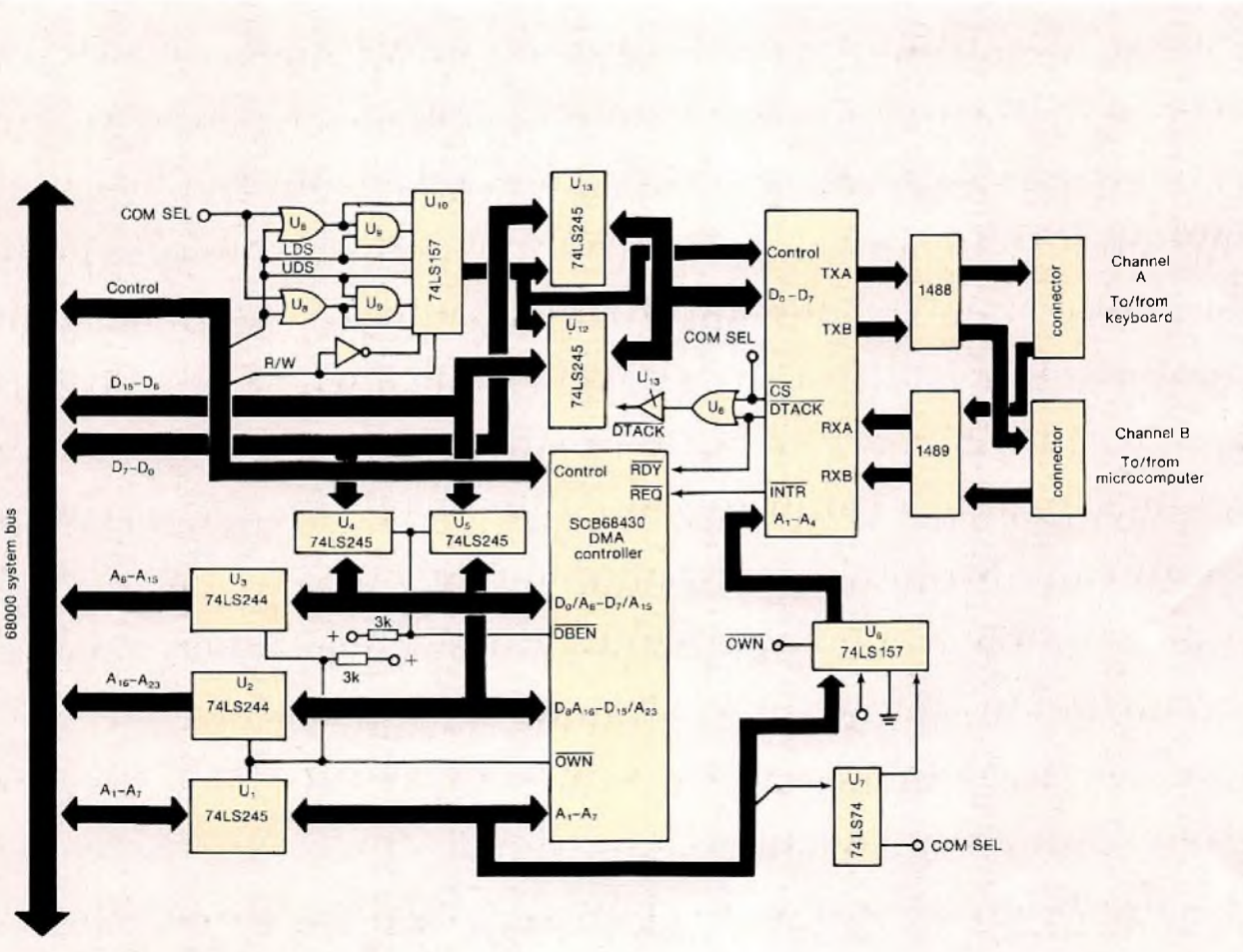

Fig.7 DMA compatibility for UART via the 68000 bus

TABLE 3
Initialization routine

```
COMINIT  MOVE.B #$10, CRA ; RESET POINTER
         MOVE.B #$02, MR1A ; 7 BITS, EVEN PARITY
         MOVE.B #$37, MR2A ; ENABLE RTS, CTS
         MOVE.B  #$44, CSRA  ; SET 300 BAUD RATE
         MOVE.B  #$30, CRA   ; RESET.TRANSMITTER-RECEIVER
         MOVE.B  #$20, CRA   ; NOW ENABLE BOTH
         MOVE.B  #$05, CRA   ; NOW ENABLE BOTH

         MOVE.B  #$10, CRB   ; RESET POINTER
         MOVE.B  #$02, MR1B  ; 7 BITS, EVEN PARITY
         MOVE.B  #$37, MR2B  ; ENABLE RTS, CTS
         MOVE.B  #$44, CSRB  ; SET 300 BAUD RATE
         MOVE.B  #$30, CRB   ; RESET TRANSMITTER-RECEIVER
         MOVE.B  #$20, CRB   ;
         MOVE.B  #$05, CRB   ; NOW ENABLE BOTH

         MOVE.B  #$33, ISR   ; SET INTERRUPT CONDITIONS

         MOVE.B  #$72, IVR   ; SET INTERRUPT TO VECTOR POINT

         RTS                 ; WE ARE DONE
```

Note: Channel A is the monitor and channel B the microprocessor.

TABLE 4
A simple driver

```
TRANSFER MOVE.B  DO,CSRA    ; RESET A3 AT FLIP-FLOP U7
         BTST.B  #00,CHAN   ; CHANNEL _ _ IS TO BE ACTIVE
         BEQ     ONWARD     ; SKIP SETTING OF BIT IF
                              CHANNEL A

         MOVE.B  DO,CSRB    ; SET A3 AT THE FLIP-FLOP U7

ONWARD   MOVE.W  LENGTH,    ; SET THE TRANSFER LENGTH
                  MTCH
         MOVE.L  BUFFER,    ; LOAD THE BUFFER ADDRESS
                  MACH
         MOVE.L  TPXFER,    ; SET THE TRANSFER MODE,
                  DCR         DIRECTION, AND START BIT

         OPERATION NOW STARTED, SO RETURN TO MAIN
         PROGRAM

         RTS                ; GOOD-BYE
```

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Interfacing HCMOS with other logic families

J. P. EXALTO

Demands for higher speed, greater complexity and lower power dissipation in logic systems are being met by interfacing different logic technologies in the same system. These mixed technology systems must also be able to communicate with the outside world. As the input voltage requirements of conventional CMOS circuits are incompatible with TTL output levels, it's often necessary to sacrific noise margins, speed and quiescent power dissipation to achieve these interfaces between families. However, with our PC54/74HC/HCT family of high-speed CMOS (HCMOS), this is no longer so.

The HCMOS ICs are available in two versions: circuits with type number suffix HC operating with CMOS input switching levels from a 2 to 6 V supply (intended primarily as faster CMOS ICs in new designs), and devices with suffix HCT, switching at TTL input levels from a supply of 5 V ±10%. All types are fully buffered and pin- and function-compatible with most popular LSTTL ICs.

Additionally, unbuffered inverters (suffix HCU) are available for oscillators, and other feedback circuits operating in linear mode, but it's with the HC and HCT types and their interfacing with other logic families that this article is concerned. Furthermore, it will discuss the quiescent and dynamic noise immunity characteristics of HCMOS devices and compare them with those of LSTTL ICs.

HC/HCT INTERFACING TECHNIQUES

It's necessary to consider two groups of interfaces for the HC/HCT devices: interfacing with other logic families; and interfacing with non-standard peripheral levels and directly driven loads.

Due to the comparable operating speeds of HCMOS and LSTTL logic, it's the interface between these two families that will be most common, so we'll discuss these considerations at greater length. However, interfaces with other families, including the HE4000B series CMOS and ECL 10K, are also simply implemented. Table 1 summarises the solutions for the various types.

HCMOS and TTL output configurations

The typical output structure of an HCMOS IC is shown in Fig.1(a). When the output is HIGH or LOW (V_{OH} or V_{OL}), its level is very close to V_{CC} or GND respectively.

In contrast, the HIGH level output voltage for the standard TTL circuit shown in Fig.1(b) is limited by the V_{BE} of TR_1 plus the voltage drop across D_1, resulting in a maximum V_{OH} of 3,5 V at V_{CC} = 5 V. Further, if a collector current is flowing, R_1 will cause an additional voltage drop and the worst case V_{OHmin} specified for TTL is 2,4 V (at I_{OHmax}), over the full temperature and power supply range.

The LOW level output voltage for TTL is the collector/emitter saturation voltage of TR_2 (excess of base current) and so even when a source current flows from the loaded output, V_{OLmax} will not exceed 0.5 V.

Looking at the output structure for LSTTL devices in Fig.1(c), the V_{OH} is now limited by the V_{BE} of both TR_1 and TR_3 (the diode does not feature in the LSTTL output structure) and is typically 3,4 V. LSTTL specifications quote V_{OHmin} as 2,7 V over the full temperature range with V_{CCmin} = 4.75 V.

TABLE 1
Interfacing HCMOS to other logic families

		TO					
		HC 5 V supply	**HCT** 5 V supply	**HE4000B** 5 V supply	**HE4000B** 6 – 15 V supply	**TTL*** 5 V supply	**ECL 10K**
FROM	**HC** 5 V supply	direct	direct	direct	4104	direct	10124
	HCT 5 V supply	direct	direct	direct	4104	direct	10124
	HE4000B 5 V supply	direct	direct	direct	4104	direct	10124
	HE4000B 6 – 15 V supply	4049 or 4050	4049 or 4050	4049 or 4050	direct	4049 or 4050	ansistor
	TTL* 5 V supply	pull-up resistor	direct	pull-up resistor	4104	direct	10124
	ECL 10K	10125	10125	10125	transistor	10124	direct

* Includes LS, S, STD, FAST, ALS and AS.

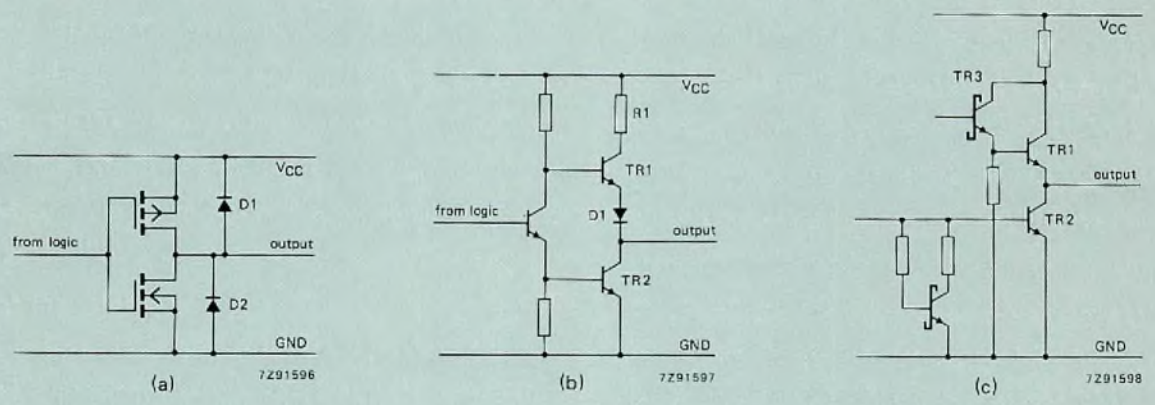

Fig.1 Typical output configurations of: (a) HC/HCT devices – D1 and D2 are the inherent diodes of the p-drain and the n-drain respectively, (b) standard TTL, and (c) low-power Schottky TTL (LSTTL)

HCMOS input structures

The input structure for HC devices is given in Fig.2(a). Under normal operating conditions, the input voltage should swing within the supply voltage limits V_{CC} and GND, since exceeding these limits can cause a current to flow through the input protection diodes, D_1 and D_2. The maximum d.c. current permitted through these diodes is 20 mA and if this rating is exceeded, the function of the circuit may be impaired. As the MOS transistors TR_1 and TR_2 are electrically identical, the typical logic switching of the device is $V_{CC}/2$.

The input configuration for HCT devices is basically identical to that for HC circuits but with the addition of a level shifting diode (D_3) between PMOS transistor TR_1 and V_{CC}. This is shown in Fig.2(b). The effect of D_3, combined with NMOS transistor TR_2 having a higher gain than PMOS transistor TR_1, is to reduce the input switching level typically to 1,4 V.

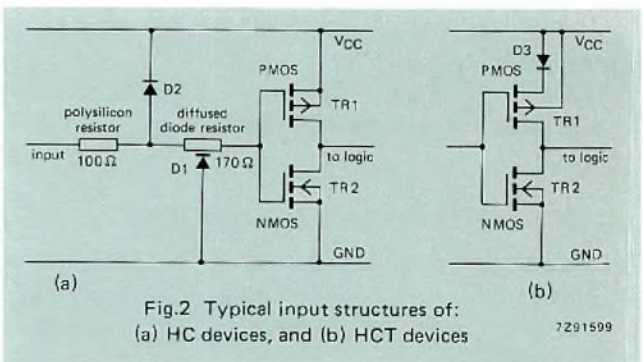

Fig.2 Typical input structures of: (a) HC devices, and (b) HCT devices

The advantage of diode D_3 is that it reduces power dissipation when a HIGH input from a TTL output is applied. This HIGH level can be as low as 2,4 V, and although it will be recognised as a logic "1", the PMOS transistor TR_1 would not be fully cut-off allowing a flow-through current between V_{CC} and GND. D_3, and the influence of the back-gate (substrate) connection of TR_1 to V_{CC}, dramatically reduces the flow-through current, and therefore the power dissipation, in the input stage whilst yielding input switching levels compatible with LSTTL.

Interfacing LSTTL with HC/HCT

When HCT and LSTTL devices operate from the same supply, the quiescent flow-through current I_C at V_{IH} = 2,4 V and V_{CC} = 4,5 V, is close to zero. This means that the HCT input structure gives true CMOS type power dissipation, even when driven from TTL. If V_{CC} is increased to 5,5 V, the minimum HIGH level output voltage also rises 1 V to 3,4 V.

For interfacing LSTTL with HC/HCT in a dual supply voltage system, the following worst case conditions supply:

V_{OHmin} for TTL = 2,4 V

V_{OHmin} for LSTTL = 2,7 V

and

V_{IHmin} for HC devices = 3,85 V (70% of V_{CC})

V_{IHmin} for HCT devices = 2 V

(where V_{CC} = 4,75 V for TTL and 5,5 V for HCMOS, over total temperature range).

From the above figures, it's clear that the worst-case TTL HIGH level output voltage is less than the minimum HIGH level input voltage for HC devices and an interface is required. A solution is provided in the circuit in Fig.5(a), where pull-up resistor R_1 will pull the output voltage of the LSTTL against V_{CC}. However, we don't favour this technique because the time-constant formed by the pull-up resistor and the stray capacitance (C_S) plus the load capacitance (C_L) will increase the propagation delay.

Furthermore, with this set-up the propagation time is less predictable because it relies on both active and passive RC time-constants. Although a low value for R_1 will reduce the propagation delay, it consumes extra power and reduces the noise margin LOW (due to an active load) and this conflicts with the purpose of using HCMOS. The pull-up resistor also requires board space and insertion time thus increasing production costs.

Therefore, the pull-up resistor interface should only be used if unavoidable and the practical solution is to use HCT devices (all types in the PC54/74 family are available in both HC and HCT versions). The LSTTL and HCT ICs interface directly as shown in Fig.3(b).

Driving LSTTL from HCMOS

Since the output of HCMOS devices swing between V_{CC} and GND, they are TTL input compatible and the interface is a direct connection (also shown in Fig.3(b)).

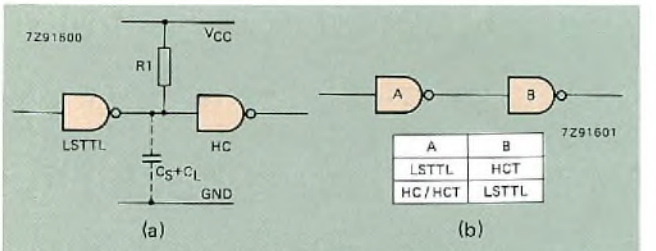

Fig.3 Techniques for interfacing: (a) LSTTL with HC devices, and (b) LSTTL with HCT devices, and HC/HCT with LSTTL devices

When an HCT device is the driving source, the speed can be accurately predicted because the LSTTL logic switching threshold of 1,4 V is also used for HCT ICs. For HC driving sources, the speed difference introduced by the HC logic switching threshold of $V_{CC}/2$ can be calculated from the specified output transition times (from the data sheets).

Table 2 gives the driving capability (fan-out) of HC/HCT for the various TTL families.

TABLE 2
Maximum fan-out for HC/HCT driving TTL

receiving input	standard output	bus driver output
TTL	2	3
LSTTL	10	15
STTL	2	3
FAST	6	10

Interfacing HC/HCT with HE4000B series CMOS

HC/HCT devices can be coupled directly to standard HE4000B series CMOS ICs if they operate from the same supply voltage. However, if the circuits have different supply voltages, level shifting is necessary. The configuration shown in Fig.4(a) illustrates this for the HC/HCT to HE4000B interfaces using the HEF4104B LOW-to-HIGH level-shifter. Note that this IC is exclusively a LOW-to-HIGH level-shifter and care should be taken to ensure that V_{CC1} never exceeds V_{CC2} by more than one V_{BE}.

Figure 4(b) shows how to interface the HE4000B family with HC/HCT using the HEF4049B/4050B or PC74 HC4049/4050 buffer ICs. These buffers don't have an input clamping diode to V_{CC} and this means that the maximum input level is 15 V. The logic level switching threshold remains referenced to V_{CC2}, so the noise margin LOW will be as for the 5 V specification.

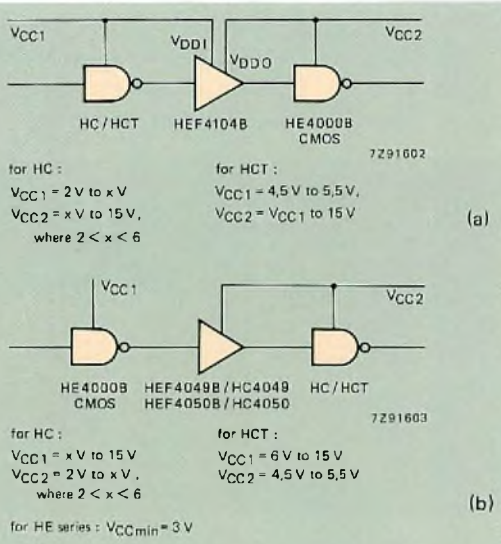

Fig.4 Techniques for interfacing: (a) HC/HCT devices with HE4000B series CMOS, and (b) HE4000B series CMOS with HC/HCT devices

For interfacing HC/HCT devices with NMOS devices (microprocessors, memories, etc.). the rules for TTL apply since NMOS ICs generally have TTL-compatible inputs and outputs. Exceptions are NMOS ICs with open-drain outputs where a pull-up resistor must be used to load the output.

Interfacing HC/HCT with ECL 10K

To interface with ECL 10K series logic, the 10124 TTL-to-ECL and the 10125 ECL-to-TTL translator ICs (for HC/HCT-to-ECL and ECL-to-HC/HCT interfaces respectively) are used. Note that these devices operate at TTL levels. When using the 10125 for interfacing HC circuits, the pull-up resistor R_1 must be used in accordance with the instructions for driving HC devices from TTL. The circuit configurations are shown in Figs.5(a) and 5(b).

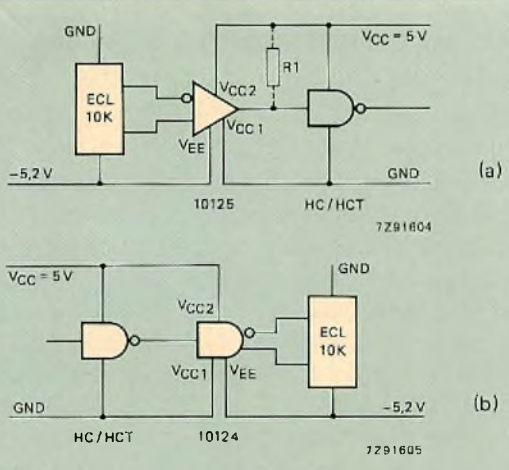

Fig.5 Techniques for interfacing: (a) ECL 10K logic with HC/HCT circuits — R1 is only required when driving HC types, and (b) HC/HCT devices with ECL 10K logic

Interfaces with terminated buses

Buses are used chiefly in industrial applications and unfortunately, this environment imposes several restraints on microprocessor-based systems, electrical noise and battery back-up requirement being two such examples. CMOS technology provides the ideal solution to these problems, and the HC devices offer superior noise immunity, similar operating speed and lower power dissipation over a wider temperature and supply range than comparable LSTTL ICs. For the HCT range, the noise immunity is the same as for LSTTL.

Therefore, development of a new bus standard for CMOS systems should be based on the performance of the devices available with bus driver outputs, for example, the PC74/54HC245 transceiver. Figs.6(a) and 6(b) show examples of TTL and HC/HCT bus terminations respectively.

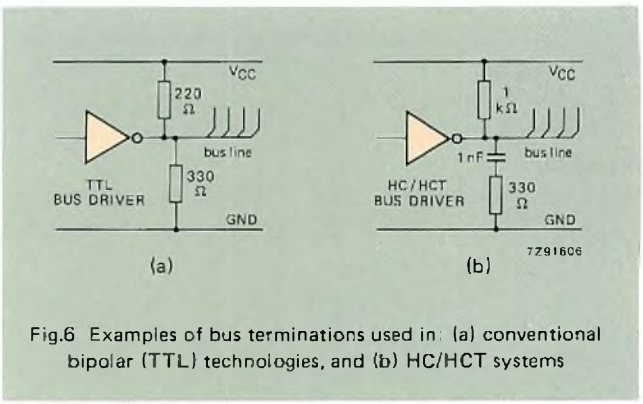

Fig.6 Examples of bus terminations used in: (a) conventional bipolar (TTL) technologies, and (b) HC/HCT systems

Conventional buses are heavily d.c. loaded so within existing bus standards, HC/HCT bus drivers are unable to drive these loaded buses as they can only deliver an output current of 6 mA. Under these circumstances, the interface should be implemented with a suitable bus driver.

HC/HCT devices do not generally have input hysteresis so Schmitt trigger circuits should be used if slow, noisy bus rise and fall voltages call for hysteresis in the receiver. The PC54/74HC/HCT14 and 132 are two such ICs for noise tolerant systems and five devices in the flip-flop series (PC54/74HC/HCT73, 74, 107, 109 and 112) also have Schmitt triggers in the clock input.

Interfacing with non-standard levels

In many applications, PC54/74 high-speed CMOS ICs will need to interface with non-standard input and output levels, for example, with industrial or automotive systems operating from a 12 to 24 V supply. The circuits in Figs.7(a) and 7(b) show the basic design rules for these interfaces. Figure 7(c) illustrates an example of a user edge input circuit for interfacing with input levels greater than V_{CC}. The configuration for HC/HCT devices driving loads from an external power supply is given in Fig.8(a), and Figs.8(b) and 8(c) show HC/HCT devices driving loads (for example, a relay) on the same supply voltage.

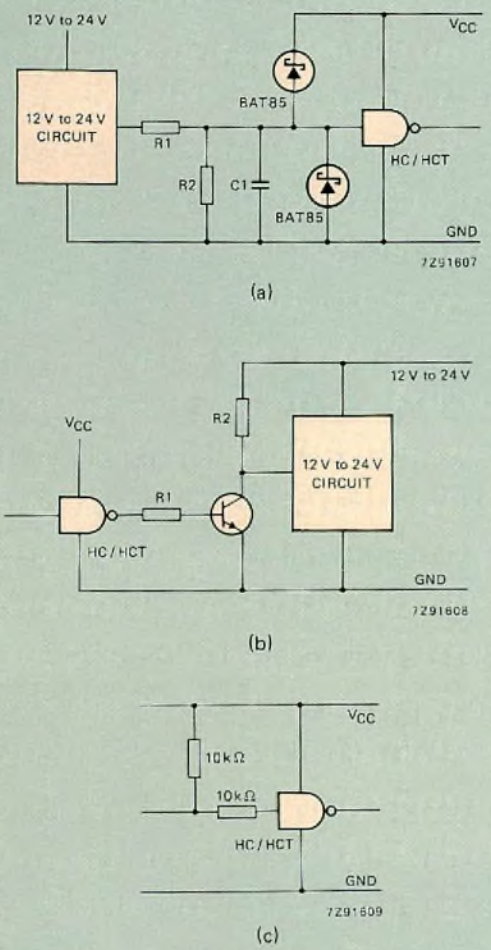

Fig.7 Techniques for interfacing: (a) non-standard logic levels with HC/HCT circuits – values of R1 and R2 depend on the output voltage of the driving circuit and C1 depends on the noise and speed, and (b) HC/HCT devices with non-standard logic levels – values of R1 and R2 depend on supply voltage and transistor type. (c) shows a user-edge input circuit configuration for interfacing with input voltages greater than V_{CC}

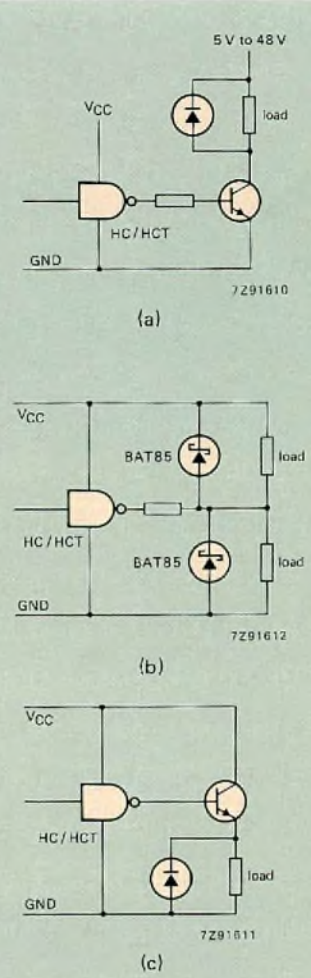

Fig.8 Interfacing HC/HCT devices with a load on: (a) an external power supply via a transistor, and (b) the same power supply via a transistor. (c) shows interfacing HC/HCT directly with loads on the same power supply

NOISE IMMUNITY IN HC/HCTMOS

The noise immunity characteristics for logic devices can be divided into two categories: static and dynamic noise immunity. If we first examine the static noise immunity, this can also be divided into two further categories as follows:

- static noise immunity LOW – this is the difference between the V_{ILmax} of the receiving circuit and the V_{OLmax} from the driving circuit
- and static noise immunity HIGH – this is the difference between the V_{OHmin} from the driving circuit and the V_{IHmin} of the receiving circuit.

If we compare the guaranteed static noise immunity characteristics for LSTTL, and HC/HCTMOS, the result is as shown in Table 3.

TABLE 3
Static noise margins for LSTTL at V_{CC} = 4,75 V and HC/HCT systems at V_{CC} = 4,5 V

	LSTTL	HC	HCT
V_{OHmin}	2,7 V	4,4 V	4,4 V
V_{IHmin}	2,0 V	3,15 V	2,0 V
noise margin HIGH	0,7 V	1,25 V	2,4 V
V_{ILmax}	0,8 V	0,9 V	0,8 V
V_{OLmax}	0,4 V	0,1 V	0,1 V
noise margin LOW	0,4 V	0,8 V	0,7 V

TABLE 4
Ratio of static noise margins, LSTTL to HC/HCT

	LSTTL	HC	HCT
noise margin HIGH	1	1,75	3,4
noise margin LOW	1	2	1,75
ambient temperature range T_{amb}	0 to +70 °C	−40 to +85 °C	−40 to +85 °C
supply voltage V_{CC}	4,75 V	4,5 V	4,5 V

If we now take the static noise margins for LSTTL to be unity, (for both the HIGH and LOW states) a direct comparison can be made by taking the ratio of LSTTL to HC/HCT static noise margins as shown in Table 4. These results are particularly impressive when considering the extended ambient temperature range of the HC/HCT and the lower supply voltage.

The graph in Fig.9(a) compares the static noise margins for HC devices with those for LSTTL. This illustrates that whilst HC circuits can drive LSTTL (as V_{OHmin} for HC $>$ V_{IHmin} for LSTTL), the converse is not true (since V_{OHmin} for LSTTL $<$ V_{OHmin} for HC – there is no overlap on the noise margin HIGH regions). Therefore, the noise margin HIGH for LSTTL driving HC devices is said to be negative which explains the reason for the pull-up resistor interface described in Fig.3(a).

In a mixed technology system with fully loaded HCT outputs driving LSTTL inputs, the static noise margin LOW is equal for both families, and the HCT devices exhibit an excellent static noise margin HIGH that encompasses that displayed by LSTTL. This is illustrated by the graph in Fig.9(b) and shows that HCT and LSTTL devices are fully interchangeable.

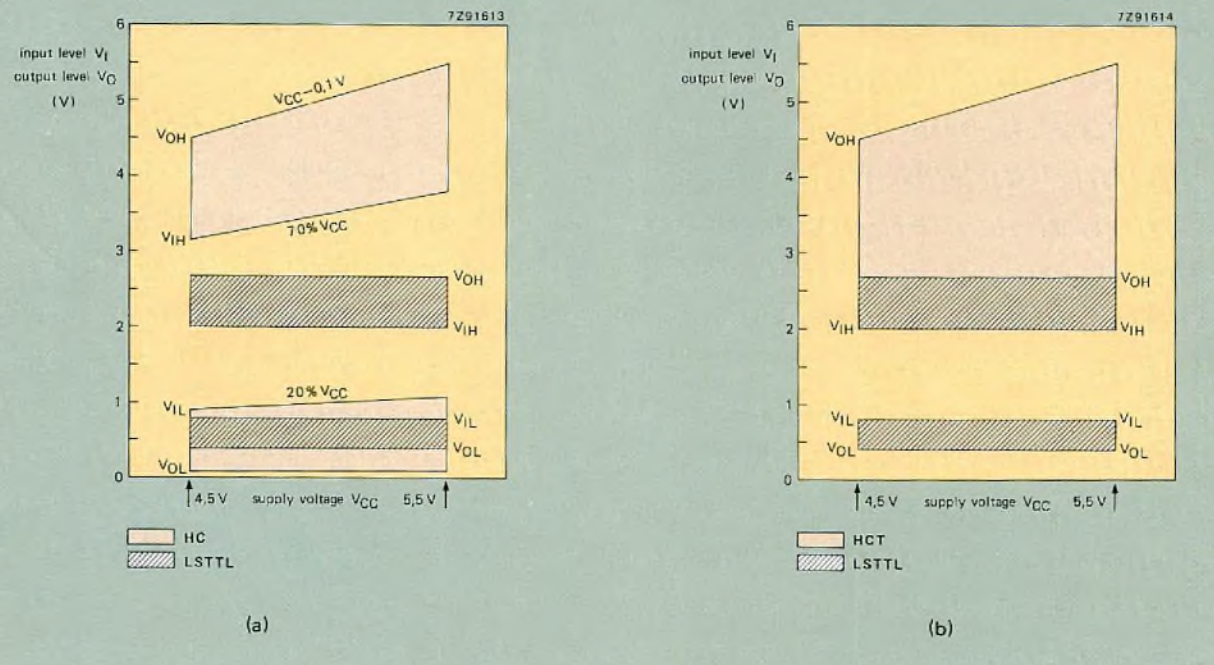

Fig.9 Static noise margins for: (a) HC devices compared with LSTTL, and (b) HCT devices compared with LSTTL in a mixed technology system

DYNAMIC NOISE IMMUNITY

As for static noise immunity, dynamic noise immunity for HC/HCT circuits falls into two catagories, HIGH and LOW. The dynamic noise margin LOW is again the smaller of the two, so it is this parameter that we'll consider here.

To plot the dynamic noise immunity LOW for HC/HCT devices, a pulse of known magnitude V_p is applied to the input of a device and its width (t_W) is increased until the device just begins to switch. The input level on which V_p is based is equal to the switching voltage minus the worst-case static noise margin LOW. Pulse width (t_W) is measured at half pulse height ($V_p/2$) and the rise and fall times (t_r and t_f) are 0,6 ns.

The V_p is then reduced in increments and the t_W for each new value assertained. The test is repeated over a series of varying supply voltages, V_{CC} (between 2 and 6 V for HC and at 5 V for HCT), and output current, I_O.

The resulting graphs in Figs.10(a) and 10(b) illustrate the dynamic noise immunity characteristics of HC and HCT circuits respectively. Note that increasing I_O, lowers the curve and therefore reduces the dynamic noise immunity. As these curves illustrate the worst-case conditions with fully loaded HC/HCT devices, a system of only HC or HCT circuits will demonstrate an increase in dynamic noise immunity, shifting the curves up 0,3 V.

Derived from the typical input switching threshold levels of 1,3 V and 2,5 V for HC and HCT respectively, the noise immunity characteristics will show a typical improvement of 0,8 V in HCT systems and 1,2 V in HC systems.

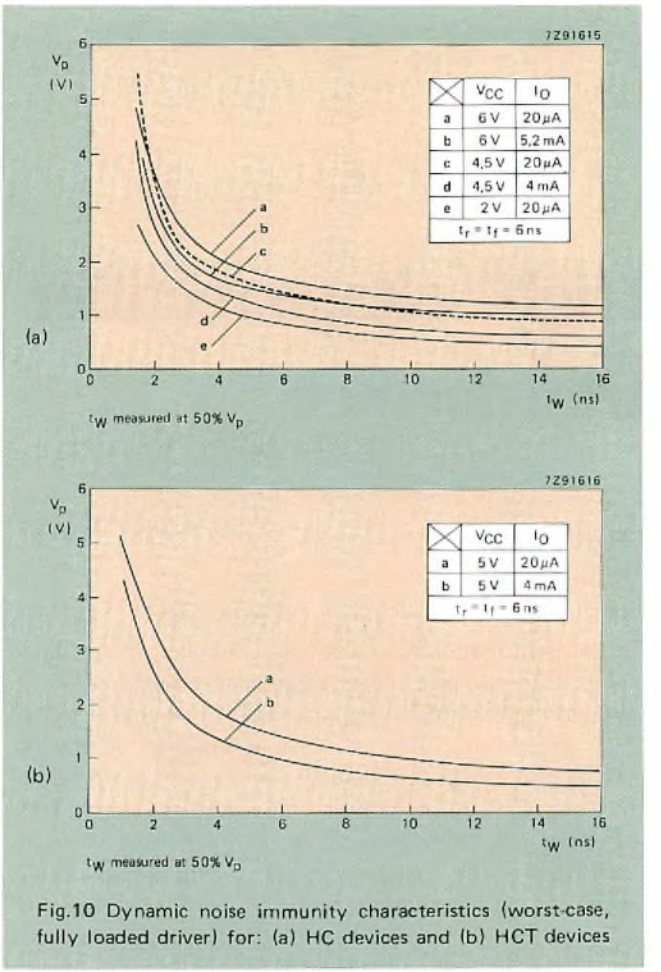

Fig.10 Dynamic noise immunity characteristics (worst-case, fully loaded driver) for: (a) HC devices and (b) HCT devices

High-voltage rectifier stacks for diode-split transformer

GRAHAM HINE

First widely used in television e.h.t. supplies, silicon-diode high-voltage rectifier stacks have since established themselves in a host of other applications. To name just a few: X-ray generators, often working at upwards of 100 kV; military and civil radar; night viewers, in which a few kilovolts may have to be derived from a portable, low-voltage battery supply; and, closer to home, microwave ovens. As the list has grown, so has our mastery of the manufacturing technology and our ability to tailor the characteristics of our high-voltage rectifier stacks to the requirements of specific applications.

Table 1 lists our current range of high-voltage rectifier stacks and summarizes their principal data in the following terms:

V_{RW}, working reverse voltage

V_{RRM}, repetitive peak reverse voltage

V_F, forward voltage drop at T_j = 120 °C and I_F = 100 mA (except as otherwise noted)

$I_{F(AV)}$, average forward current

I_R, reverse current at T_j = 120 °C and $V_R = V_{RW}$

Q_S, stored charge

t_{rr}, reverse recovery time.

The abbreviations VM and DST in the 'applications' column indicate whether a type is more suitable for use in conventional voltage multipliers or in the diode-split transformers now widely used in television and monitor applications.

MANUFACTURE

Figure 1 illustrates the construction common to all our high-voltage rectifier stacks, and Fig.2 a selection from the present range.

Manufacture begins with sawing the silicon ingot into slices. Phosphorus (n^+) and boron (p^+) are diffused simultaneously from opposite sides of each slice. Next, platinum carrier-lifetime killer is diffused to a concentration that depends on the specified operating frequency of the rectifier; diffusion temperature and time control the concentration.

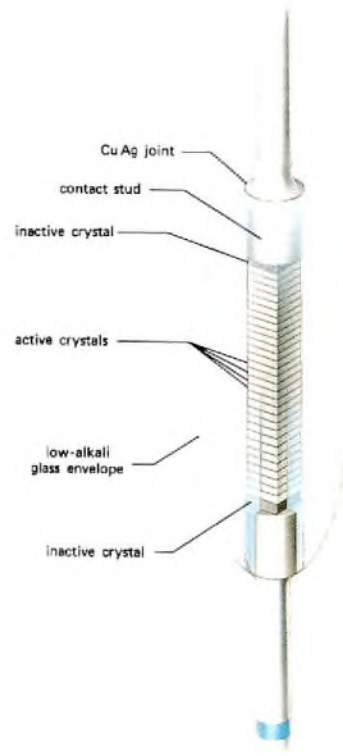

Fig.1 High-voltage rectifier stack construction

TABLE 1
Principal characteristics and applications of our current range of high-voltage rectifier stacks

type	V_{RW} max. (kV)	V_{RRM} max. (kV)	V_F (V)	$I_{F(AV)}$ max. (mA)	I_R (μA)	Q_S (nC)	t_{rr} (μs)	applications
BY584	1,5	1.8	< 8.5	85	<3	<1	0,2	V_{g2} supply in colour tv
BY505	2	2.2	< 8.5	85	<3	<1	0.2	VM
BY614	2	2,2	< 9	50	<3		<0,3	VM, miniature stack for night viewers
BY509	11,5	15	<43	4	<3	<1	0,2	VM, e.g. triplers
BY609	12	15	<50	4	<3	<1	0.2	DST, e.g. layer wound
BY610	12	17	<50	4	<3	<1	0,2	DST, e.g. layer wound
BY619	12	15	<75	4	<3	<0,4	0,1	DST, e.g. layer wound, up to 128 kHz
BY620	12	17	<75	4	<3	<0,4	0.1	DST, e.g. layer wound, up to 128 kHz
BY707	8	9	<52	4	<3	<1	0,2	VM
BY708	10	12	<52	4	<3	<1	0,2	VM, e.g. triplers
BY709	12	14	<52	4	<3	<1	0,2	VM
BY710	14	17	<70	3	<3	<1	0,2	DST, e.g. slot wound
BY711	16	19	<70	3	<3	<1	0,2	DST, e.g. slot wound, in small-screen b/w tv
BY712	18	22	<76*	3	<3	<1	0,2	half-wave e.h.t. rectifiers e.g. for B/W tv
BY713	20	24	<76*	3	<3	<1	0,2	
BY714	24	30	<76*	3	<3	<1	0,2	
BYX90G	6	7.5	<14.5**	550	<50		<0,35	VM, X-ray, radar, microwave ovens

* at I_F = 50 mA ** at I_F = 2 A.

Aluminized on both sides by electron-beam vacuum evaporation, the slices are stacked and bonded together by silicon-aluminium eutectic. Depending on the specified reverse voltage, a stack may contain up to 30 active slices. Inactive, heavily doped, low-ohmic slices are included at the top and bottom for mechanical protection and to make ohmic contact with the terminal studs. The stacks are wire sawn into square rods whose cross-sectional size depends on the specified rectifier forward current.

The rods are etched clean and alloyed to terminal studs whose thermal expansion coefficient closely matches that of silicon. The copper leads, brazed to the studs with high-conductivity, corrosion-resistant, silver-copper alloy, are iron-cored to facilitate magnetic handling.

The assembly is etched and the terminal studs oxidized to provide a suitable surface for adhesion; then it is coated with a frit of low-alkali zinc-borate-silicate glass which is fired to a smooth, impervious envelope that ensures hermeticity and protection from aggressive chemicals. The glass also passivates the diode junctions, ensuring low, stable leakage currents even at high junction temperatures. Its expansion coefficient closely matches the expansion coefficients of silicon and the terminal studs.

Completed stacks are subjected to 100% final inspection of main electrical characteristics before being bandoleered, spooled and packed in polyethylene bags with dessicant.

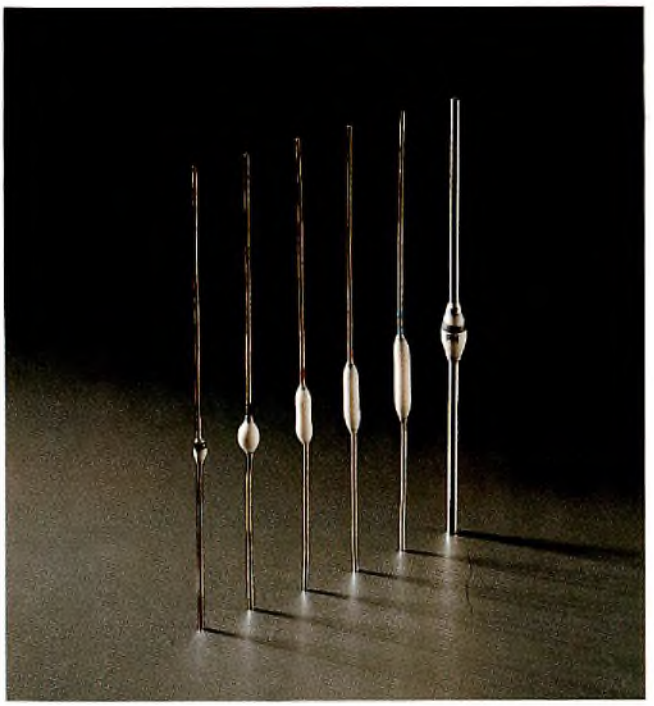

Fig.2 A selection from our current range of high-voltage rectifier stacks

QUALITY

Development of high-voltage rectifier stacks follows the same lines as those described in a previous article on glass-bead diodes (see Ref.). This establishes the foundations of quality: design, materials, and processes. Once full-scale production begins, measures are taken to safeguard those foundations. Process control is highly mechanized; the production equipment is to a large extent self-checking and is regularly calibrated against standards. Operators and staff undergo continual training. Acceptance tests, inspections, and quality assessments enter into the production flow at the same points as for glass-bead diodes (see Ref.). Engineering and production departments, in collaboration with the quality department, continually propose and implement quality improvement programmes. At the end of the production line a 100% inspection is performed according to the type specification. In addition, the quality department takes weekly samples from production for assessment of electrical characteristics, dimensions, appearance, robustness of terminals, solderability, operating endurance, and high and low-temperature storability. Table 2 lists the applicable AQLs and inspection levels.

TABLE 2
Sample inspection criteria, AQLs, and inspection levels for high-voltage rectifier stacks

inspection criteria	AQLs individual	AQLs combined	inspection level
mechanical/visual			
major dimensions	0,65%		S2
other dimensions	6,5%		S2
visual	0,6%	2,5%	II
electrical characteristics			
major	0,4%	0,65%	II
other	2,5%		S2
inoperatives			
mechanical	0,1%		
electrical	0,1%		II

The operating endurance tests are done at maximum rated conditions and are designed to promote failures for analysis. High-temperature reverse-bias tests at maximum rated d.c. voltage and maximum rated junction temperature are made on random production samples.

The quality measured is reported in terms of

- conformity, expressed in p.p.m. (parts per million)
- reliability, expressed as Failure Rate per million device hours at an upper confidence level of 60% (FR_{60}).

Conformity

The process average reject level as measured at the end of the production line is less than 10 p.p.m. During acceptance inspection of the type families BY509/609 and BY708/714 in 1983 and 1984 no electrical failures occurred.

Experience of customers with whom we cooperate in a p.p.m. policy has shown a net line fall-off rate for BY509/609 stacks of less than 10 p.p.m.

Reliability

For type BY708/711/713 stacks, endurance tests under maximum rated conditions and high-temperature reverse-bias tests during 1982-84 gave the following results:

type	failures	device hours	FR_{60}
BY708/711/713	0	450 000	$2,0 \times 10^{-6}$/h

Similar tests on the type BY509 and BY609/610 stacks spanning a longer period gave the results:

types	failures	device hours	FR_{60}
BY509	0	920 000	$1,0 \times 10^{-6}$/hr
BY609/610	0	605 000	$1,5 \times 10^{-6}$/hr

Combining these results on the basis of the structural and technological similarities of the products gives:

types	failures	device hours	FR_{60}
BY509 BY609/610 BY708/711/713	0	1 975 000	$0,5 \times 10^{-6}$/hr

Note that this failure rate applies under maximum rated conditions. Assuming the cause of failure to be reverse instability, which has an activation energy of 1,4 eV to 2,0 eV, one can apply the same failure rate multiplication factor as a function of temperature as for glass-bead diodes (see Ref.). Under normal operating conditions, in a tv set for instance, this would result in a failure rate at least a hundred times smaller than that tabulated above; i.e. about 5×10^{-9}/h (5 FITS).

DESIGN AND APPLICATION OF STACKS

Designing a stack for a specific application entails compromises and trade-offs. By way of illustration, we shall consider one aspect of the design of a stack for use in a diode-split transformer television e.h.t. supply (Fig.3). The aspect on which we shall focus is dissipation; specifically, optimizing the dissipation throughout the operating range.

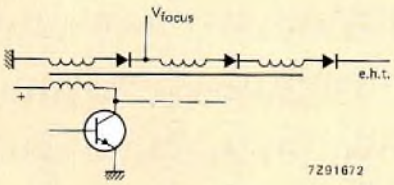

Fig.3 Diode-split transformer circuit

In a diode-split transformer the e.h.t. is obtained by rectifying and adding together the voltage pulses developed across several secondary windings during flyback. Two types of transformer are used: layer-wound (Fig.4(a)), with the secondaries wound one on top of another; and slot-wound (Fig.4(b)), with secondaries wound side-by-side in separate slots. Although, unlike a doubler or tripler, neither uses discrete capacitors, both have interwinding capacitances which significantly affect their performance. In particular, the rate of rise of the reverse voltage (dV_R/dt) is generally higher in layer-wound than in slot-wound transformers and, as a result, the reverse switching dissipation is larger. In respect of total dissipation, therefore, layer-wound transformers are the more critical and are the type on which we shall concentrate here.

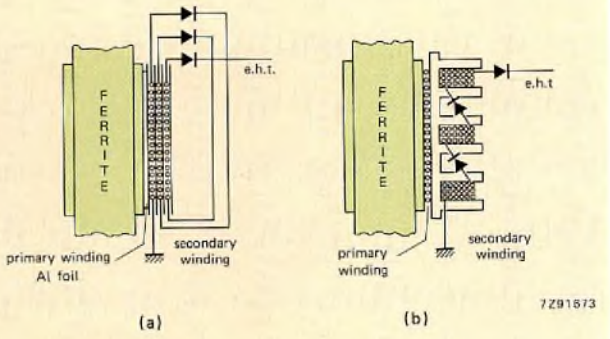

Fig.4 Diode-split transformer construction: (a) layer wound; (b) slot-wound

Dissipation components

The dissipation in a rectifier diode has three components:

- the forward dissipation P_F
- the reverse dissipation P_R
- the switching dissipation P_S.

Measures can be taken to minimize each of these, but not independently of each other.

Forward dissipation

Forward dissipation is the product of the average forward current $I_{F(AV)}$ and the forward voltage drop V_F at $a^2 I_{F(AV)}$, where a is the form factor of the forward current waveform ($a = I_{F(RMS)}/I_{F(AV)}$).

In a tv set $I_{F(AV)}$, the sum of the beam current, the focus current and any bleeder resistor current, may be as much as 2 mA. Depending on the design of the transformer, however, a^2 may be as large as 40, so the forward dissipation will be a function of the forward voltage drop at 40 x 2 mA = 80 mA. A low forward voltage drop at low current is therefore no guarantee of low forward dissipation; that is why, in our data sheets, we specify V_F at 100 mA or 200 mA and give curves of its maximum values at $T_j = 25\,^{\circ}C$ and $T_{j\,max}$ (Fig.5).

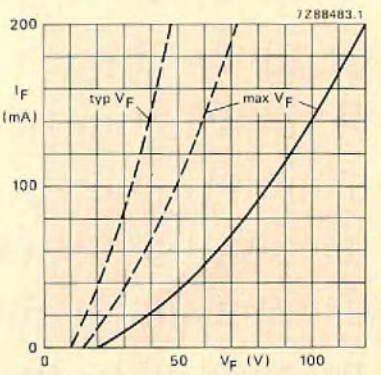

Fig.5 Typical curves of forward voltage drop V_F as a function of forward current I_F at junction temperature of 25 °C and 120 °C, as presented in the data sheets of high-voltage rectifier stacks. The curves shown are for the type BY609 and BY610

Reverse leakage dissipation

The dissipation due to the reverse leakage current I_R is $P_R = V_R I_R \delta$, where V_R is the amplitude of the reverse voltage waveform and δ its duty factor.

At maximum junction temperature the diode must remain thermally stable. That is, the power supplied to it per degree must not exceed the amount of heat removed per degree; otherwise, the resulting temperature rise will be destructive. As the reverse leakage dissipation has a positive temperature coefficient, roughly doubling for every 10 K to 15 K rise, it sets the following condition for thermal stability:

$$P_R\, c\, R_{th\,j\text{-}a} \leqslant 1$$

Here, $R_{th\,j\text{-}a}$ is the junction-to-ambient thermal resistance of the diode, and c the temperature coefficient of P_R in the equation

$$P_R = P_0 \exp c\,(T_j - T_0)$$

where P_0 is the reverse leakage dissipation at a reference junction temperature T_0.

A doubling of P_R per 10 K corresponds to a temperature coefficient of $c = 0{,}069$, and under normal mounting and potting conditions in a layer-wound transformer $R_{th\,j\text{-}a} \approx 120$ K/W. Therefore, the condition for thermal stability is

$$P_R \times 0{,}069 \times 120 \leqslant 1$$

$$P_R \leqslant 0{,}120\ \text{W}.$$

At $V_R = 10$ kV and $\delta = 0{,}83$, this corresponds to a reverse leakage current $I_R \approx 15\ \mu$A.

Thanks to the use of platinum lifetime killer, and the excellence of the glass passivation, we are able to guarantee a leakage current at maximum junction temperature of no more than $3\ \mu$A. In a layer-wound transformer this affords a safety factor of 5 against thermal instability due to reverse leakage dissipation.

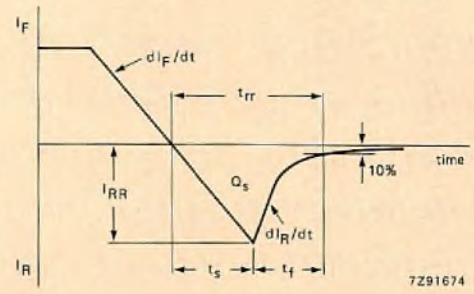

Fig.6 Current waveform in a high-voltage rectifier switching from forward conduction to reverse blocking, showing the division of the reverse-recovery time t_{rr} into storage time t_s and fall time t_f. Q_s is the charge stored in the junction during switching (also called reverse recovery charge)

Switching dissipation

Switching dissipation has two components, forward and reverse. In a diode-split transformer the forward component can usually be disregarded.

The reverse component depends on the reverse recovery characteristic of the diode (Fig.6), the operating frequency, and the rate of rise of reverse voltage, dV_R/dt. The reverse recovery time of the diode, t_{rr}, can be divided into two parts: the storage time t_s, at the end of which the reverse current reaches its maximum value I_{RR}; and the fall time t_f during which the reverse current falls to its steady-state value and the reverse voltage starts to rise. The larger the values of I_{RR}, dV_R/dt and t_f, the larger the dissipation.

The rate of rise of reverse voltage, dV_R/dt, is determined not by the diode but the circuit, and in a layer-wound transformer can be as high as 6 to 8 kV/μs. It is therefore essential to use diodes with both a small I_{RR} and a short t_f. As shown by Fig.7, a small I_{RR} alone gives no guarantee of small switching dissipation; although the diode of Fig.7(a) has by far the smallest I_{RR}, its dissipation is the largest because its fall time is the longest.

The importance of a small t_f might seem to argue for the use of snap-off diodes (Fig.8(a)), but because of the interference and 'spook' phenomena these might cause they are not practical in a tv set. All our high voltage stacks use soft-recovery diodes, guaranteed minimum values of t_f, as well as maximum values of stored charge Q_S, being specified in the data sheets.

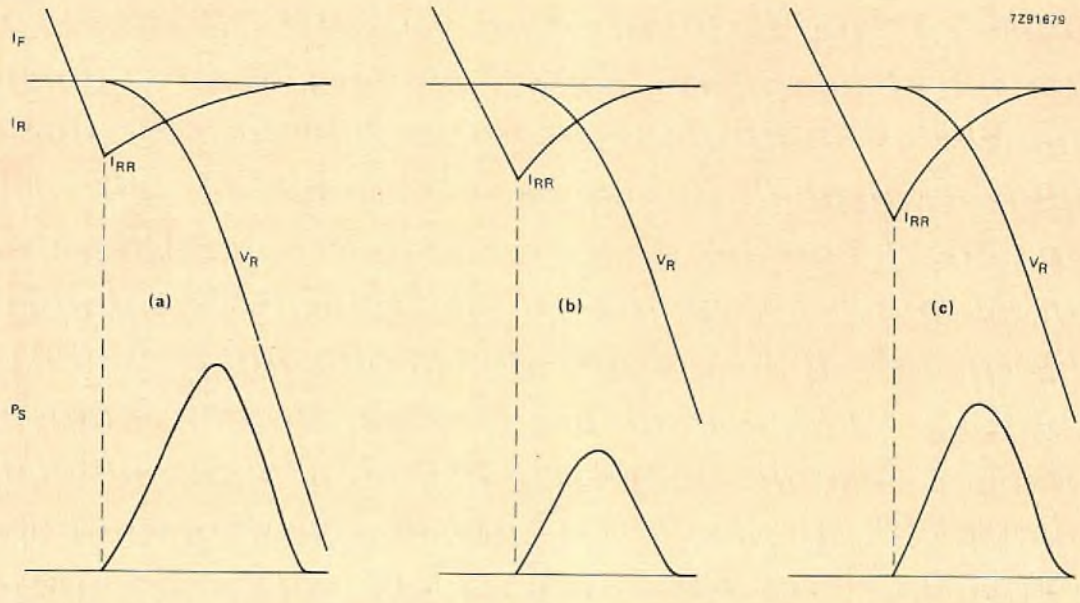

Fig.7 Switching dissipation P_S depends on both I_{RR} and t_{rr}. Given the same rate of rise of V_{RR}, diodes (b) and (c) have smaller dissipation than (a) because their recovery times are shorter, even though they both have larger I_{RR}

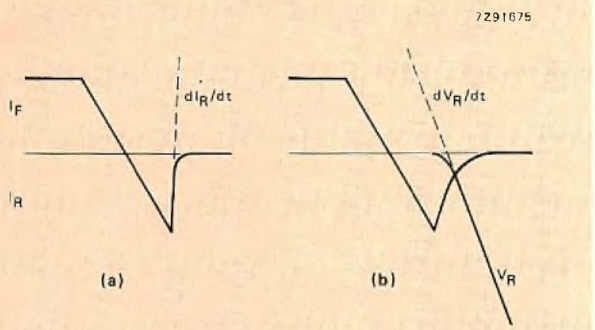

Fig.8 (a) Snap-off recovery, unsuitable for use in tv sets because of interference risk due to high dI_R/dt. (b) Soft recovery, also showing the reverse voltage V_R which, together with reverse current I_R, determines the switching dissipation; the circuit, not the rectifier, determines the rate of rise of V_R

Finding the optimum compromise

At the frequencies at which diode-split transformers commonly operate (upwards of 15 kHz), the switching dissipation due to the relatively long reverse-recovery time of silicon would be unacceptable. The time can be shortened either by irradiation or diffusing into the silicon a carrier-lifetime killer. Irradiation, though, is not practical for crystals that are to be glass encapsulated; moreover, irradiated crystals deteriorate rapidly at temperatures above 125 °C. Therefore, diffusion is necessary. Of the two possible lifetime killers, platinum and gold, the former is preferable on several counts:

- it gives lower reverse leakage current, with correspondingly lower reverse dissipation and higher permissible operating temperature at comparable switching speeds
- within limits it is possible to increase the platinum concentration to shorten the recovery time without increasing the leakage current. Increasing gold concentration to shorten recovery time increases the leakage current proportionately
- platinum hardly affects the forward recovery voltage and time. Gold increases both in proportion to its concentration, and forward switching dissipation cannot then be disregarded.

An apparent disadvantage of platinum is that at room temperature it gives a larger forward voltage drop than gold; at normal operating temperatures, however, the difference becomes less significant.

Platinum killing reduces the stored charge Q_S and the reverse recovery time t_{rr}. Figure 9 shows how the total dissipation and its three components vary as functions of these. The left side of each graph shows the effect of a high platinum concentration, and the right side the effect of a low concentration. The high forward dissipation at high concentration shown in Fig.9(a) is due to the effect of platinum on the forward voltage drop.

Figure 9 is for a given set of forward and reverse operating conditions ($I_{F(AV)}$, a, V_R, δ, dV_R/dt, and frequency). Thus the optimum indicated in Fig.9(d) applies only at those conditions, and only at a certain ambient temperature. Figure 10(a) illustrates the decrease of forward dissipation due to the negative temperature coefficient of the forward voltage drop. Figures 10(b) and (c) show how the other two dissipation components both increase with temperature, resulting in a total dissipation curve as shown in Fig.10(d).

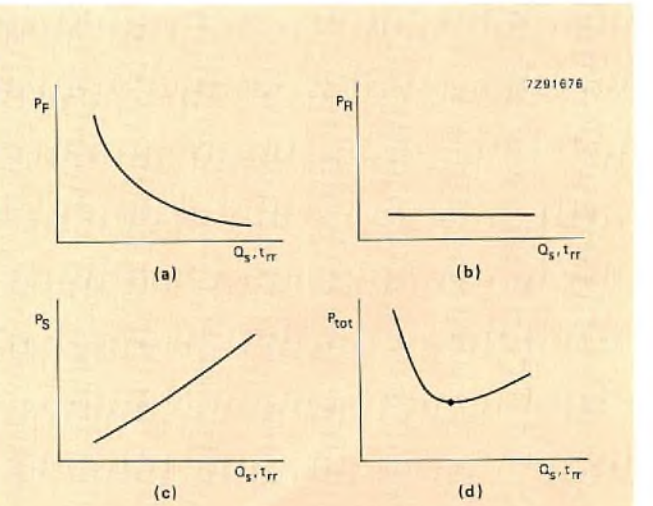

Fig.9 Dissipation as a function of stored charge Q_S and reverse-recovery time t_{rr} in a platinum-killed rectifier diode, at constant temperature. (a) Forward dissipation, (b) reverse dissipation, (c) switching dissipation, (d) total dissipation. Q_S and t_{rr} both vary inversely as the platinum concentration

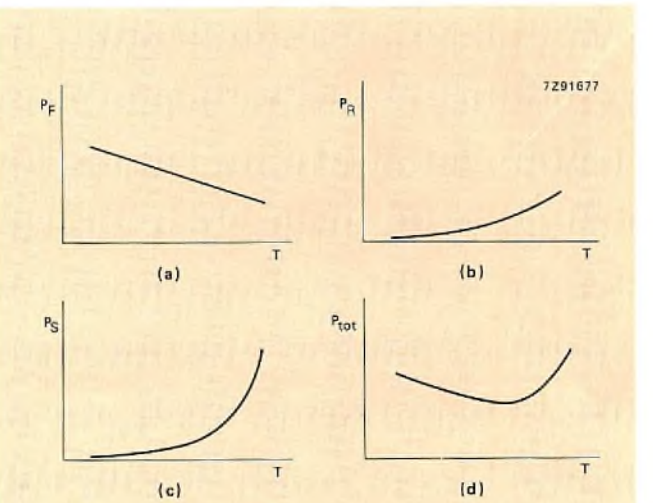

Fig.10 Diode dissipation as a function of temperature at a given platinum concentration (Q_S and t_{rr} constant). (a), (b), (c) and (d) as in Fig.9

The point of departure in optimizing dissipation is therefore a detailed specification of the operating conditions, including ambient temperature range. In-circuit measurement of prototypes designed on this basis provide information for subsequent improvement. Figure 11, which compares the performance of two stacks in a layer-wound transformer, illustrates the benefit to be gained. Curve A is for a stack commonly used in diode-split transformers; curve B is for a stack specially developed for that application. The design operating conditions were

V_{eht} = 25 kV

I_{load} = 2 mA

f = 16 kHz

T_{amb} = 25 – 140 °C

and the significant characteristics of the two stacks were:

	curve A	curve B	
V_F	130 V	60 V	at 100 mA, 25 °C
Q_S	0,3 nC	0,6 nC	when switched from I_F = 200 mA to V_R at dI_F/dt = 200 mA/μs.

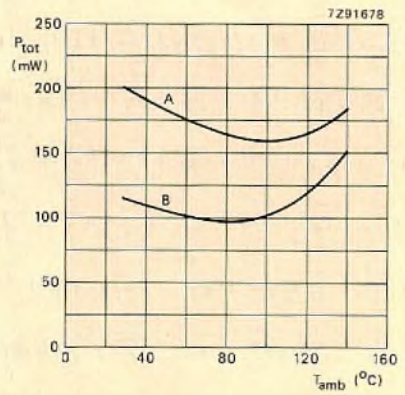

Fig.11 Comparison of total dissipation as a function of ambient temperature for two high-voltage rectifier stacks in a layer-wound diode-split transformer. Curve B illustrates the results of design optimization

Both curves show the total dissipation as a function of the ambient temperature; the operating junction temperature is 15 K to 30 K higher, depending on the total dissipation.

In curve B the negative temperature coefficient of P_F predominates over the positive temperature coefficients of P_R and P_S up to about 85 °C; the steeper rise of curve B between 100 °C and 140 °C reflects larger switching dissipation due mainly to the larger stored charge. Nevertheless, there is no threat of thermal instability, and throughout the 25 – 140 °C design temperature range curve B remains significantly below curve A. Moreover, in the practically important range from 25 – 80 °C, curve B is more nearly constant than curve A.

Curve B is for type BY609/610 rectifier stacks for use in tv sets; similar stacks for use in display terminals at up to 128 kHz are the BY619 and BY620.

Conclusion

Selective though the foregoing treatment is in its focus on dissipation alone, it serves to illustrate how analytical and empirical methods complement each other in the development process. High-voltage rectifier stacks can be similarly optimized in respect of other performance aspects as well, such as the ability to withstand transients due to picture-tube flashover. In combination with modern manufacturing techniques and our 'zero defects' quality philosophy, this enables us to supply high-voltage rectifiers to meet virtually the full spectrum of today's e.h.t. requirements. The continuity of our research activity and the breadth of our application experience amply support the confidence that we shall be equally well prepared to meet the challenge of tomorrow's.

REFERENCE

HINE, G., 'Quality of small-signal, low and medium power diodes', Electronic Components and Applications, Vol. 6 No. 2, 1984, pp. 112 to 124.

ACKNOWLEDGEMENT

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Abstracts

Disk controller supports both rigid and floppy drives

Two ICs: an SCN68454 intelligent multiple disk controller, and an SCB68459 phase-locked loop for the disk drives, allow you to build a disk controller that supports as many as four rigid- and/or floppy-disk drives, and lets you select from a number of different disk and drive-interface formats.

Liquid-crystal displays for automotive applications

LCDs have been successfully used for auxiliary functions in the car, and should now be used in the dashboard. This article presents the latest developments of Videlec for this application, in particular optimizing contrast and reducing light leakage in transmissive reverse-contrast LCDs, and driver integration onto the display.

An integrated approach to CD players

Part 1: The optical pick-up

A much-publicised advantage of the Compact Disc (CD) system is its high level of immunity to dust, fingerprints, and scratches on the compact discs. To this list can be added its immunity to disc defects such as pin-holes and track eccentricity introduced by the pressing equipment. Less-publicised, but even more important, are the marked differences in the ability of individual players to handle these defects and, in addition, the knocks, vibration and g-forces experienced in cars. This article introduces a new range of ICs and an optical pick-up that can be used to manufacture players that will play discs with defects without producing any detectable sound colouration.

An integrated approach to CD players

Part 2: The decoding electronics

Until now, no CD player has made full use of the error-correcting capability of the CD system's Cross-Interleaved Reed-Solomon Code (CIRC). In this article, a decoder that can make the maximum four erasure corrections of this code is introduced. For errors that cannot be corrected by the CIRC, the decoder performs a basic interpolation. For full-performance players, a circuit that has an 8-sample interpolator and a new FIR digital filter with four times over-sampling is available. In combination with a low-order analog filter, this digital filter produces no detectable sound colouration of the audio.

The frame-transfer sensor – an attractive alternative to the tv camera tube

The NXA1010 and NXA1020 are two solid-state image sensors (black/white and colour respectively) operating on the frame-transfer (FT) principle, according to which each field of a complete picture frame is separately integrated within a photosensitive imaging region during vertical blanking, and then clocked out serially to form the video signal during the subsequent field integration period. Outstanding features of these sensors are good blue sensitivity and high tolerance to overexposure.

DMA Interface for 68000 systems

DMA is often used to improve I/O operations and increase system throughput in applications requiring frequent transfer of large blocks of data between system memory and peripherals. This article describes the operation of the fastest DMA controller in the 68000 family – the 68430 DMAI. It then goes on to show a typical application providing DMA capability for the 68681 dual universal asynchronous receiver/transmitter (DUART).

Interfacing HCMOS with other logic families

When designing systems with our high-speed, low-power HCMOS family of logic ICs, it's invariably necessary to interface these ICs with other logic families, the most common being LSTTL (for which, in most cases, HCMOS is pin compatible), others being ECL, other CMOS families and automotive or industrial ICs. This article discusses the techniques involved and the device used to implement these interfaces whilst still maintaining high operational speed.

High-voltage rectifier stacks for diode-split transformer

The technological refinements of today's solid-state rectifiers make them suitable for most e.h.t. supplies, even including those delivering more than 100 kV. The present range includes types tailored for use in conventional voltage multipliers as well as in the diode-split transformers that are finding increasing application in tv and high-frequency monitors. To illustrate the options available with current technology, this article describes how diode parameters can be adjusted to minimize dissipation in one type of e.h.t. supply.

Disk-Controller unterstützt sowohl Festplatten- als auch Floppy Disk-Laufwerke

Zwei integrierte Schaltungen, SCN68454 IMDC (Intelligent Multiple Disk Controller) und SCB68459 DPLL (Disk Phase-Locked Loop), erlauben den Aufbau von intelligenten Disk-Controllern für maximal vier Festplatten- und Floppy Disk-Laufwerke in gemischter Konfiguration, wobei zum einen unterschiedliche Laufwerk-Schnittstellen unterstützt werden, zum anderen unterschiedliche Aufzeichnungsformate selektierbar sind.

Flüssigkristall-Displays für Kraftfahrzeuganwendungen

LCDs sind erfolgreich in Kraftfahrzeugen zur Anzeige verschiedener Funktionen eingesetzt worden. Sie sollten nun auch ihren Platz im Armaturenbrett finden. Dieser Artikel behandelt die neuesten Entwicklungen von Videlec für diesen Anwendungsbereich. Besonders eingegangen wird auf die Optimierung des Kontrasts, die Verringerung von Lichtverlusten in Durchlicht-ICs mit negativem Kontrast sowie die Integration der Treiber auf dem Display.

Eine integrierte Lösung für CD-Spieler

Teil 1: Die optische Abtasteinheit

Ein oft genannter Vorteil des Compact Disc-(CD-)Systems ist seine weitgehende Unempfindlichkeit gegenüber Staub, Fingerabdrücken und Kratzern auf der Plattenoberfläche. Die Liste der Disc-Fehler, die das CD-System zu verkraften imstande ist, lässt sich ergänzen um Stiftlöcher- und Spurexzentrizität, die durch die Pressvorrichtungen verursacht werden können. Weniger bekannt, aber noch wichtiger sind die markanten Unterschiede im Leistungsvermögen der einzelnen CD-Spieler, diese Fehler auszugleichen, ausserdem auch zusätzliche Beanspruchungen, die beim bevorstehenden Einsatz im Automobil zu berücksichtigen sind, z.B. Stösse, Vibrationen und Beschleunigungskräfte. Dieser Beitrag stellt ein neues IC-Paket und eine optische Abtasteinheit vor, die den Aufbau von CD-Spielern mit einwandfreier Wiedergabe ohne erkennbare Tonverfärbungen ermöglichen.

Eine integrierte Lösung für CD-Spieler

Teil 2: Die Decodierelektronik

Bislang wurden die Fehlerkorrektur-Möglichkeiten, die der Cross-Interleaved Reed-Salomon Code (CIRC) des CD-Systems bietet, von keinem CD-Spieler vollständig ausgenutzt. In diesem Beitrag wird ein Decoder vorgestellt, der die auf der Basis dieses Codes möglichen, maximal vier Fehler- bzw. Aussetzer-Korrekturen ausführen kann. Bei Fehlern, die sich über CIRC nicht korrigieren lassen, führt der Decoder eine lineare Interpolation aus. Für CD-Spieler der Spitzenklasse steht eine Schaltung mit einem 8-Sample-Interpolierer und einem neuen Digitalfilter (FIR) zur Verfügung, das mit vierfacher Überabtastung arbeitet. In Kombination mit einem analogen Nachfilter niedriger Ordnung liefert dieses digitale Filter eine hohe Klangqualität ohne feststellbare Tonverfärbungen des Stereo-Audiosignals.

Der Frame-Transfer-Sensor – eine attraktive Alternative zur Fernseh-Kameraröhre

NXA1010 (SW-Sensor) und NXA1020 (Farbsensor) sind zwei Halbleiterbildaufnehmer, die nach dem Frame-Transfer-Prinzip arbeiten: Jedes Halbbild eines vollständigen Bildes wird in dem fotoempfindlichen Bildbereich integriert, während der Speicherbereich ausgelesen wird. Die Information zum Bilden des Videosignals wird seriell ausgegeben; währenddessen wird das nächste Halbbild integriert. Herausragende Merkmale dieser Sensoren sind: gute Blauempfindlichkeit und Widerstandsfähigkeit gegen Überstrahlung in einem grossen Bereich.

DMA Interface für 68000-Systeme

DMA wird oft verwendet, um E/A-Operationen zu vereinfachen und den Datendurchsatz in Systemen zu erhöhen, bei denen häufig lange Datenblöcke zwischen dem Systemspeicher und peripheren Einheiten übertragen werden müssen. Dieser Artikel beschreibt die Arbeitsweise des schnellsten DMA-Controllers der 68000-Familie, des 68430 DMAI. Ausserdem wird eine typische Anordnung vorgestellt, bei der DMA-Operationen im Zusammenhang mit dem 68681 (DUART) erforderlich sind.

Anpassung von HMOS-Schaltungen an die ICs anderer Logik-Familien

Beim Entwurf von Systemen mit unseren sehr schnellen, wenig Leistung verbrauchenden Logik-ICs der HMOS-Familie ist es unverändert notwendig, diese an die ICs anderer Logik-Familien anzupassen. Häufig handelt es sich um LSTTL-Schaltungen (meistens anschlusskompatibel mit HCMOS-Schaltungen) sowie um ECL-Schaltungen, andere CMOS-Familien und um ICs für den Kraftfahrzeug- und Industriesektor. Dieser Artikel behandelt die damit verbundenen Techniken und die Bauelemente, die man benötigt, um die Anpassungen bei Erhaltung der hohen Arbeitsgeschwindigkeit zu verwirklichen.

Hochspannungs-Gleichrichtergruppen für Diodensplittransformatoren

Die technische Verfeinerung heutiger Halbleitergleichrichter befähigt diese Bauelemente, die Vakuumgleichrichterdiode in vielen Hochspannungsanwendungen zu ersetzen, sogar in solchen, die mehr als 100 kV liefern. Das laufende Gleichrichterprogramm enthält Typen sowohl für konventionelle Spannungsverstärkung als auch für Diodensplittransformatoren, die allgemein in Fernsehgeräten und Hochfrequenzmonitoren eingesetzt werden. Um den heutigen Stand der Technik zu illustrieren, beschreibt dieser Artikel, wie die Diodenparameter gezielt ausgelegt werden können, um eine Minimierung der Verluste in einer gegebenen Hochspannungsanwendung zu erreichen.

Un contrôleur pour unités de disques durs ou de disques souples

Deux circuits intégrés: un contrôleur multi-disques intelligent SCN68454, et une boucle à verrouillage de phase SCB68459 pour unités de disques, vous permettant de réaliser un contrôleur supportant jusqu'à quatre unités de disques durs et/ou souples et vous laissant le choix entre plusieurs formats différents de disque et d'interface.

Afficheurs à cristaux liquides pour applications à l'automobile

Des afficheurs à cristaux liquides ont été utilisés avec succès dans des fonctions auxiliaires en automobile; on envisage maintenant de les employer sur les tableaux de bord. Cet article présente les développements les plus récents de Videlec en vue de cette application, en particulier l'optimisation du contraste et la réduction des fuites de lumière dans les afficheurs transmissifs à contraste inversé, ainsi que l'intégration de l'étage de commande à l'afficheur (puce sur verre).

Une approche globale des lecteurs de Compact Disc

Première partie: le capteur optique

Un avantage du système Compact Disc, dont il est fait beaucoup état, est son degré élevé d'insensibilité à la poussière, aux traces de doigts et aux rayures sur les disques. On peut ajouter à cette liste son insensibilité aux défauts du disque, tels qui piqûres et excentricité du sillon, provenant des appareils de pressage. Moins connues, mais tout aussi importantes, sont les différences marquées que présentent les lecteurs individuels dans leur aptitude à corriger ces défauts, ainsi que les chocs, les vibrations et les efforts d'accélération subis dans les automobiles. Cet article présente une nouvelle gamme de circuits intégrés et un capteur optique permettant de construire des appareils capables de lire des disques présentant des défauts sans produire de coloration perceptible du son.

Une approche globale des lecteurs de Compact Disc

Deuxième partie: les circuits électroniques de décodage

Jusqu'à présent, aucun lecteur de Compact Disc n'a encore exploité toutes les possibilités de correction d'erreurs du CRSEC (Code Reed-Solomon Entrelacé et Cascadé) de ce système. Le présent article présente un décodeur capable d'effectuer les corrections par calcul de ce code, quatre au maximum. Pour les erreurs qui ne peuvent être corrigées par le CRSEC, le décodeur effectue une interpolation de base. Un circuit équipé de l'interpolateur à 8 échantillons et d'un nouveau filtre numérique FIR assurant l'échantillonnage quadruple est prévu pour les lecteurs hautement performants. Associé à un filtre analogique d'ordre inférieur, ce filtre numérique ne produit pas de coloration perceptible du son.

L'analyseur d'image à transfert de charges – intéressante solution de rechange au tube de caméra de télévision.

Le NXA1010 et le NXA1020 sont deux capteurs d'image état solide (respectivement noir et blanc, et couleur) fonctionnant suivant le principe du transfert de trame (frame-transfer ou FT). Chaque trame d'une image complète est intégrée séparément dans une zone de visualisation photosensible et transférée dans une zone mémoire pendant la suppression verticale, puis sortie séquentiellement pour constituer le signal vidéo au cours de la période suivante d'intégration de trame. Les caractéristiques les plus remarquables de ces capteurs sont une bonne sensibilité au bleu et un degré élevé de tolérance aux surexpositions.

Interface d'accès direct mémoire pour microprocesseur 68000

L'accès direct mémoire est fréquemment employé pour améliorer les opérations d'entrée/sortie et accroître le débit dans les applications qui nécessitent de fréquents transferts d'importants blocs de données entre la mémoire du microprocesseur et les périphériques. Cet article décrit le fonctionnement du contrôleur d'accès direct mémoire le plus rapide de la famille 68000 – le DMAI 68430. Il décrit ensuite une application type dans laquelle le double émetteur/récepteur asynchrone universal (DUART) 68681 est doté de l'accès direct mémoire.

Interfaçage de circuits HCMOS avec d'autres familles logiques

L'introduction dans des ensembles de nos circuits intégrés logiques, ultra-rapides, à faible consommation de la famille HCMOS, a conduit à les interfacer avec des circuits intégrés d'autres familles logiques, essentiellement des TTL-LS (avec lesquels les HCMOS sont généralement compatibles broche à broche), et aussi des ECL, des circuits d'autres familles CMOS et des circuits pour applications automobiles ou industrielles. L'article expose les techniques mises en oeuvre et les dispositifs utilisés pour réaliser ces interfaces tout en conservant une rapidité de fonctionnement élevée.

Groupes redresseurs à haute tension pour transformateurs à enroulements fractionnés

Le perfectionnement technologique des redresseurs à semiconducteurs actuels leur a permis de remplacer les diodes à tubes à vide dans la plupart des alimentations à très haute tension, même celles qui fournissent plus de 100 kV. La gamme actuelle comprend des modèles conçus pour les multiplicateurs classiques de tension ainsi que pour les transformateurs à enroulements fractionnés de plus en plus employés dans les moniteurs de télévision et les moniteurs à haute définition. En vue d'illustrer les options qu'offre la technologie actuelle, l'article décrit comment déterminer les paramètres de diode en vue d'une dissipation minimale dans un type particulier d'alimentation à très haute tension.

Controlador de disco que soporta lectores de discos rígidos y flexibles

Dos circuitos integrados: un controlador intelligente de múltiples discos SCN68454, y un bucle enclavado en fase para lectores de disco SCB68459, permiten construir un controlador de disco que soporta unos cuatro discos flexibles y/o rígidos, y permite elegir entre varios formatos diferentes de disco e interconexiones de lector.

Visualizadores de cristal líquido para aplicaciones en el automóvil

Los visualizadores de cristal líquido (LCD) se han utilizado con éxito para funciones auxiliares del automóvil, y ahora se pueden utilizar en el tablero de instrumentos. Este artículo presenta los últimos desarrollos de Videlec para esta aplicación, optimizando en particular el contraste y reduciendo las fugas de luz en visualizadores de cristal líquido transmisivos de contraste inverso, y la integración del excitador en el visualizador.

Circuitos integrados para reproductores de disco compacto

Parte1: El lector óptico

Una ventaja muy divulgada del sistema de disco compacto es su alto nivel de inmunidad a polvo, huellas y rayaduras en los discos compactos. A esta lista hay que añadir su inmunidad a defectos del disco tales como pequeños orificios y excentricidad del surco introducidos por el equipo de prensado. Menos divulgadas, pero aún más importantes, son las marcadas diferencias en la capacidad de cada reproductor para manejar estos defectos y, además, los golpes, vibración y fuerzas g experimentadas en los automóviles. Este artículo introduce una nueva gama de circuitos integrados y un lector óptico que pueden utilizarse para la fabricación de reproductores que reproducirán discos con defectos sin producir ninguna variación de sonido detectable.

Circuitos integrados para reproductores de disco compacto

Parte 2: La decodificación electrónica

Hasta ahora, el reproductor de disco compacto no había hecho uso completo de la capacidad de corrección de error del "Cross-Interleaved Reed-Solomon Code" (CIRC) del sistema de disco compacto. En este artículo, se introduce un decodificador que puede hacer las cuatro máximas correcciones de borrado de este código. Para errores que no pueden corregirse mediante el CIRC, el decodificador realiza una interpolación básica. Para reproducciones con todas las prestaciones, está disponible un circuito que tiene un interpolador de 8 muestras y un nuevo filtro digital FIR con cuatro sobremuestras en combinación con un filtro analógico de orden bajo, este filtro digital produce una coloración del sonido de audio no detectable.

Sensor de área – una atractiva alternativa al tubo de cámara de TV

El NXA1010 y el NXA1020 son dos sensores de imagen de estado sólido (blanco/negro y color respectivamente) que operan según el principio de transferencia de cuadro (frame-transfer (FT), de acuerdo con el cual cada campo de un cuadro de imagen completo está integrado separado dentro de la región fotosensible del conformador de imagen durante el borrado vertical, y después sincronizado externamente en serie para formar la señal de video durante el siguiente periodo de integración de campo. Las características más importantes de estos sensores son una buena sensibilidad al azuly y alta tolerancia a sobreexposiciones.

Interconexión DMA para sistemas 68000

A veces se utiliza el DMA para mejorar las operaciones E/S y aumentar el rendimiento del sistema en aplicaciones que requieren transferencias frecuentes de grandes bloques de datos entre la memoria del sistema y los periféricos. Este artículo describe el funcionamiento del controlador DMA más rápido de la familia 68000- el DMAI 68430. Se da también una aplicación típica que proporciona capacidad DMA para el doble receptor/transmisor universal asíncrono 68681 (DUART).

Interconexión HCMOS con otras familias lógicas

Al diseñar sistemas con nuestra familia de circuitos integrados lógicos HCMOS de alta velocidad y baja potencia es invariablemente necesario interconectar estos circuitos integrados con otras familias lógicas, la más común es la LSTTL (con la cual, en muchos casos, la familia HCMOS tiene los terminales compatibles), otras son las ECL, CMOS y circuitos integrados industriales o del automóvil. Este artículo estudia las técnicas y los dispositivos utilizados para implementar estas interconexiones manteniendo mientras la alta velocidad operacional.

Pilas rectificadoras de alta tensión para transformador de diodos divididos

Los refinamientos tecnológicos de los rectificadores de estado sólido actuales han permitido desplazar a los diodos de vacio en la mayoria de fuentes de M.A.T., incluso en las que dan más de 10 kV. La gama actual incluye tipos diseñados para usarlos en multiplicadores de tensión convencionales así como en los transformadores de diodos divididos que están encontrando cada vez más aplicaciones en TV y monitores de alta frecuencia. Para ilustrar las opciones disponibles con tecnología normal, este articulo describe la forma de ajustar los parámetros del diodo para minimizar la disipación en un tipo de alimentación de M.A.T.

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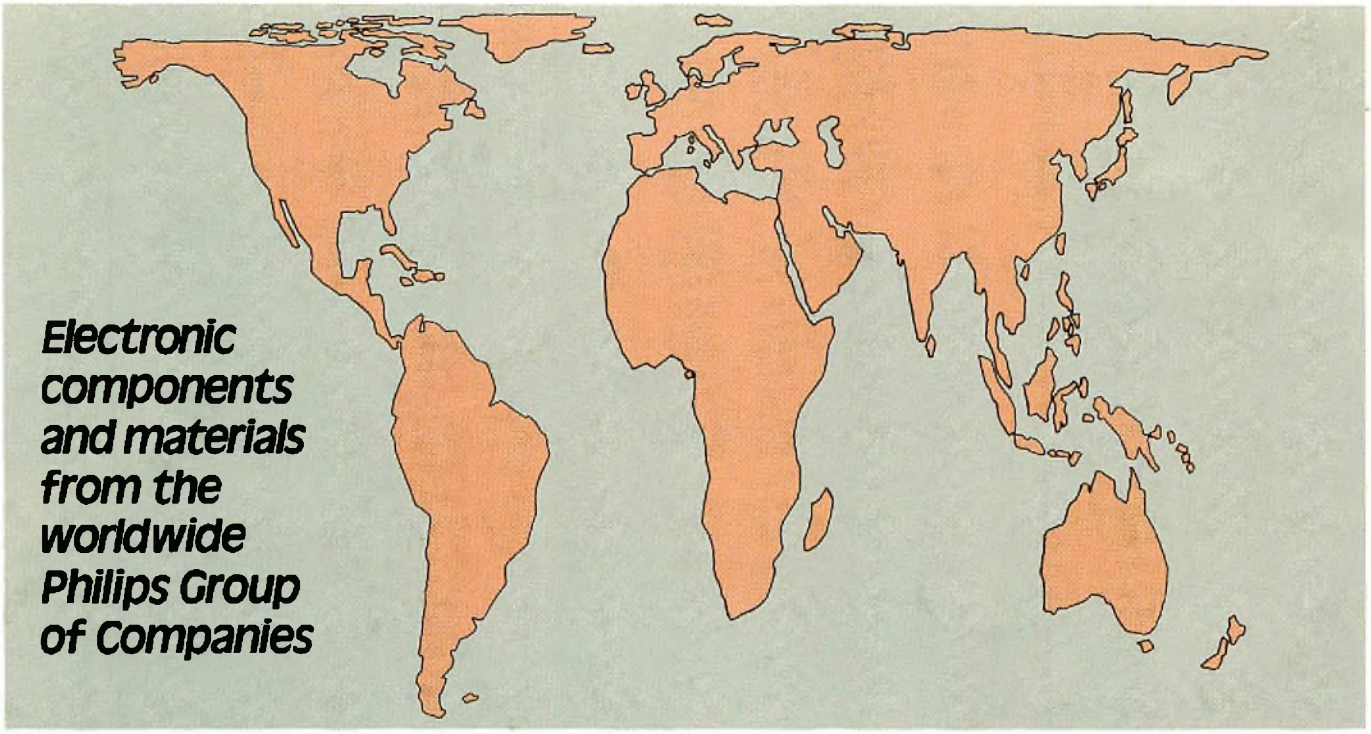

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