Electronic components & applications

Vol. 6, No 1
1984

ISSN 0141 – 6219

Electronic components & applications

Volume 6, No. 1 1984

The radio telescope at Westerbork in the Dutch province of Drenthe, one of the largest astronomical instruments in the world and a dramatic example of how computerized signal processing with advanced electronic components and techniques enables us to overcome otherwise insuperable physical barriers. Fourteen parabolic antennas, each measuring 25 metres in diameter, are equally spaced along a 3 kilometre east-west line; assembled by computer into a single composite, their combined signals provide an image whose resolution is equal to that of a single parabolic reflector 3 kilometres in diameter.

Keeping watch on cosmic radio emissions at the 21 cm 'hydrogen' wavelength, as well as 6 cm and 50 cm wavelengths, the telescope supplies a wealth of information about the physical processes in stars and galaxies that cannot be gained from optical telescopes.

Contents

This article originally appeared in the February issue (Vol. 11 No. 2) of Communications International, copyright 1984, International Thomson Publishing Ltd.

Versatile speech/transmission ICs suit all telephone architectures

P. SIJBERS

The speech and transmission functions which form the heart of a subscriber telephone set are undoubtedly the most difficult to implement in an integrated circuit. To begin with, such an IC must be adaptable to the diverse transmission requirements of the various telephone authorities. Furthermore, it must provide an interface between the line and either a pulse or DTMF dialling circuit. And finally, the amplifiers must be flexible enough to work in conjunction with many different types of microphones and earpieces. Two versatile new ICs that meet these requirements are the TEA1060 and TEA1061; using either of them, subscriber sets can be designed that fully satisfy BSI requirements.

The TEA1060 and TEA1061 are powered by the telephone line current and perform all the interface functions between a telephone line and the microphone, earpiece and dialling circuits of a subscriber set. An outstanding feature of the new ICs is that they are suitable for use with a wide range of microphone types. The TEA1060 provides up to 60 dB of gain for a low-sensitivity dynamic or magnetic microphone. The TEA1061 provides up to 46 dB of gain for a high-impedance microphone such as a piezo-electric type, an electret type with a source-follower preamplifier or buffer-amplifier, or a sensitive dynamic or magnetic type. They can also accommodate a wide variety of earpieces including piezo-electric types. Both ICs can provide click-free electronic switching between dialling and speech modes of operation. They also incorporate a power-down function to facilitate pulse dialling or for incorporating a flash feature in sets with DTMF dialling. Moreover, they have a supply point for peripheral circuits such as diallers, they can provide a confidence tone in the earpiece during DTMF dialling, and they have a very high (9 dBm) maximum transmission level.

SUBSCRIBER SET ARCHITECTURES

There are two basic types of architecture for electronic telephone subscriber sets. In one type, the speech and dialling circuits are connected to the line by the same interface. In the other type, the speech and dialling circuits are separated and connected to the line by individual interfaces.

Sets with a common line interface are for electronic telephone sets in which the speech circuit need not be a two-wire replacement for a conventional speech section comprising a hybrid transformer and a carbon microphone. In this approach, all of the line current flows into the circuit which requires only one voltage regulator and one transmitting stage to apply either speech or dialling signals to the line. Switch-over from the dialling mode to the speech mode is electronic.

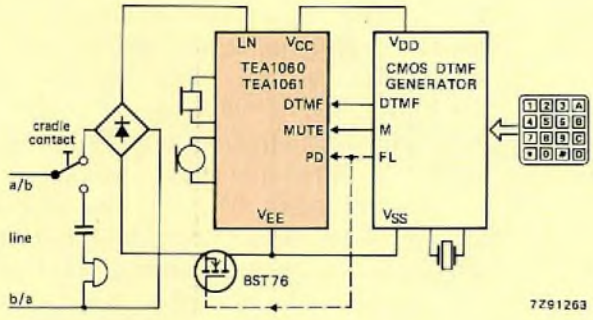
Separated speech and dialling circuits are used when the speech circuit must be a direct two-wire replacement for the conventional speech section of a subscriber set. In this case, the switch-over from the dialling to the speech mode can be either electronic or by a common contact on the keyboard.

Sets with a common line interface

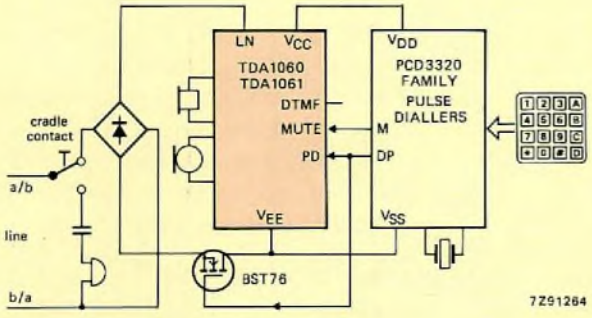
The versatility of the TEA1060 and TEA1061 allows them to be used in the three main types of subscriber set with common line interface shown in Fig.1. Figure 1(a) and (b) show two basic sets with pulse or DTMF dialling. All the advantages of the ICs can be fully exploited in a microcomputer-controlled "feature phone" as shown in Fig.1(c).

The advantage of a common line interface architecture are:

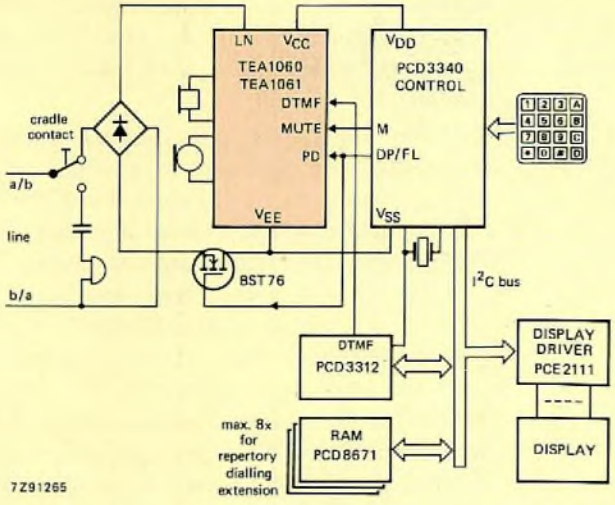
- well defined interface (supply, common, mute, power-down and interrupter) between speech functions, dialling functions and control functions
- switch over from dialling to speech mode is virtually click-free because of the mute function in the TEA1060 and TEA1061
- the line interface is not duplicated
- it is possible to have a conficence tone in the earpiece during DTMF dialling
- no additional peripheral components are needed for switching over from dialling to speech mode
- this modular approach results in considerable flexibility with regard to dialling features.



(a) Basic set with DTMF dialling and an optional flash feature



(b) Basic set with pulse dialling

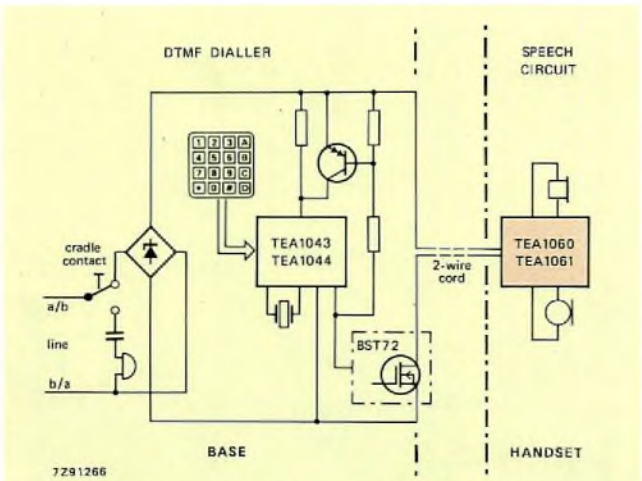


(c) A feature phone with pulse and DTMF dialling

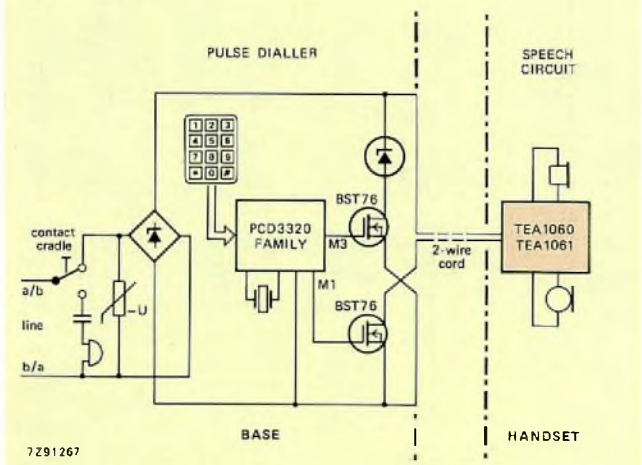
Fig.1 Subscriber telephone sets with a common line interface

Sets with a separated speech and dialling circuit

The TEA1060 and TEA1061 can also be used in subscriber sets with separated speech and dialling circuits so that the speech IC can be installed in the handset with only a two-wire connection to the base of the instrument. This type of architecture is shown for sets with DTMF or pulse dialling in Fig.2(a) and (b). When using this type of architecture, it is necessary to duplicate the line interface functions. Since the speech and dialling circuits are alternately connected to the line, it is not possible to have a confidence tone during DTMF dialling or to have click-free switch-over from the dialling mode to the speech mode. However, this type of architecture does allow the TEA1060 or TEA1061 to be used as a direct two-wire replacement for the conventional speech part of a telephone. Also, since the wires between the microphone capsule and the speech IC will be very short, there will be high immunity to r.f. interference.



(a) Basic set with DTMF dialling



(b) Basic set with pulse dialling

Fig.2 Subscriber telephone sets with separated speech and dialling functions

FUNCTIONS OF THE TEA1060 AND TEA1061

The following description is based on the block diagram of the TEA1060 and TEA1061 shown in Fig.3.

The line voltage is applied to a temperature-compensated voltage regulator which has adjustable static internal resistance. This regulates the voltage across the circuit to between 4,15 V and 6 V for line currents from 5 mA to 100 mA. The voltage variation with temperature is only −2 mV/K with a line current of 15 mA.

A supply (V_{CC}) is provided for peripheral circuits such as an electret microphone with source-follower or pre-amplifier, a pulse dialler, a DTMF dialler or a microcomputer. The available supply in the mute state is dependent on line current. With a line current of 15 mA it is 2,2 V at a maximum current of 2,6 mA and 3 V at a maximum current of 1,2 mA. With higher line currents the available voltage and current increase. They can also be increased by the addition of an inductor or gyrator in parallel with the 620 Ω resistor connected between pins LN and V_{CC} (Fig.4).

A gain controlled microphone amplifier provides a gain of 44 dB to 60 dB (depending on the value of a resistor connected between pins GAS 1 and GAS 2) between the microphone inputs and the line. The amplifier has high frequency roll-off, the corner frequency of which is adjustable. The gain control is a function of line current (proportional to line length) and has a range of 0 to −6 dB for line current limits which are set by selection of the value of a resistor connected to pin AGC. The value of the resistor is dependent on the exchange supply voltage and the resistance of the feeding bridge. The microphone amplifier in the TEA1060 has a low impedance (4 Ω) symmetrical input and is intended for use with a dynamic or magnetic microphone capsule. The microphone amplifier in the TEA1061 is preceded by a 14 dB attenuator so that it has a reduced maximum overall gain of 30 dB to 46 dB and a high input impedance (20 kΩ). The TEA1061 is suitable for use with a symmetrically connected piezo-electric microphone or an asymmetrically connected electret microphone with a FET source-follower or pre-amplifier.

During dialling, the tones from a DTMF dialling circuit are applied to an attenuator with two outputs. One output feeds a confidence tone amplifier and the other feeds a DTMF amplifier which provides an overall gain of 18 dB to 34 dB between the DTMF input and the line.

A transmitting output stage applies outgoing DTMF tones or microphone signals to the line.

Incoming signals from the line are applied to a gain-controlled receiving amplifier with an input impedance of 20 kΩ. The gain control characteristic of this amplifier is the same as that for the previously described microphone amplifier. Its gain is adjustable by selection of the value of a resistor connected between pins GAR and QR+. The gain range is 17 dB to 33 dB if the earpiece is driven single-ended, or 23 dB to 39 dB if the earpiece is driven differentially.

The amplifier receives the signals from the line after they have been attenuated by about 32 dB by an external anti-sidetone network connected between the line at LN, pin SLPE and the receiving amplifier input (IR). The anti-sidetone network uses the anti-phase microphone signal at SLPE to cancel the microphone signal content of the line signals at the input to the receiving amplifier.

The earpiece is driven by an output stage with adjustable cut-off frequency and complementary outputs. Single-ended drive (output impedance 4 Ω) is used for a low-impedance (<450 Ω) dynamic or magnetic earpiece. Differential drive is used for a high-impedance (>450 Ω) dynamic, magnetic or piezo-electric earpiece.

An active-HIGH (>1,5 V) mute input is used to achieve virtually click-free switch-over from the speech mode to the dialling mode. During dialling, this input is activated to inhibit the receiving and microphone amplifiers. The DTMF signal is then passed to the transmitting output stage and a low-level confidence tone is passed, via the confidence tone amplifier, to the earpiece output stage. During dialling, the gain between the DTMF input and the earpiece output is 43 dB less than the gain between the receiving amplifier input and the earpiece output in the speech mode.

A power-down input can be used to reduce the current drawn by the IC to 50 μA during line current interruptions caused by pulse dialling or register recall. The IC then derives its supply current from the charge on a smoothing capacitor connected to the V_{CC} pin. Whilst the power-down input is activated, the external capacitor connected to the REG pin is disconnected from the voltage regulator. This inhibits the voltage regulator to prevent it distorting the pulses of line current which are generated during pulse dialling.

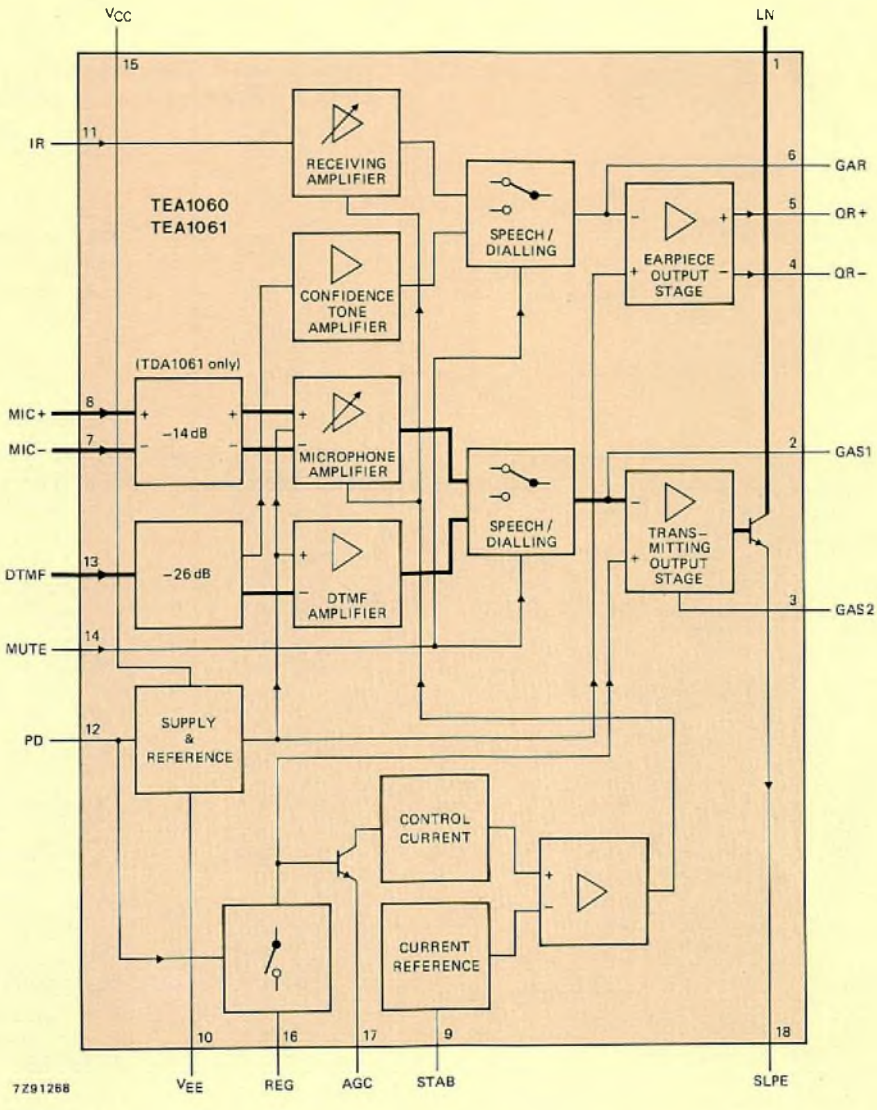


Fig.3 Block diagram of the TEA1060 and TEA1061

PRACTICAL CIRCUITS FOR THE TEA1060 AND TEA1061 IN SUBSCRIBER SETS

The complete circuit diagram of the TEA1060 or TEA1061 in a telephone subscriber set with a common line interface and DTMF dialling is shown in Fig.4. If pulse dialling or register recall is used with this circuit, the voltage limiting level of the protection circuit must be changed. The circuit diagram of the TEA1060 or TEA1061 installed as a speech circuit in the handset of a telephone subscriber set with separated speech and dialling functions is shown in Fig.5. The circuit is connected to the base of the subscriber set by a single pair of wires.

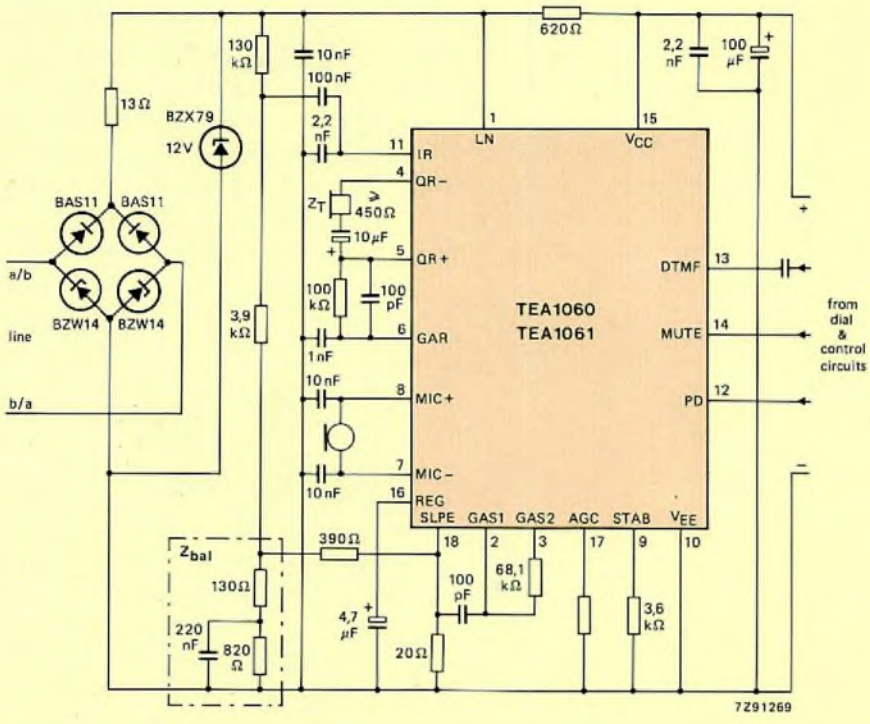


Fig.4 Complete circuit diagram of a subscriber telephone set with a common line interface

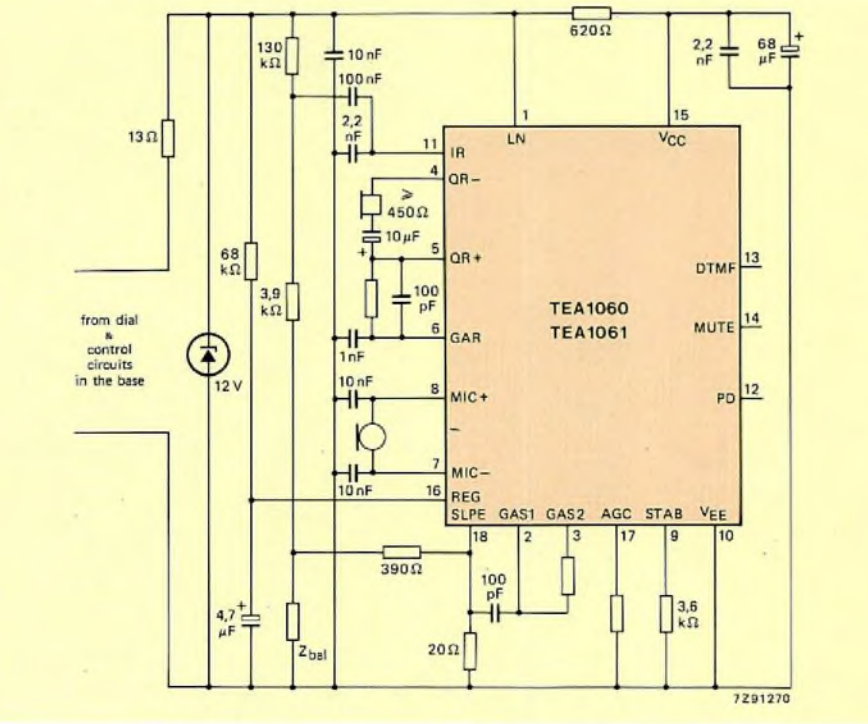


Fig.5 Circuit diagram of the handset of a subscriber telephone set with separated speech and dialling functions

Fault-tolerant software in real-time single-chip microcontroller systems

N. Q. BURNHAM and C. F. COWLING

Microcontrollers store their programs in on-chip ROM, and because of the tight linking of the program store and the CPU, it is generally assumed that the program is secure and unaffected by the operational environment. Furthermore, the use of microcontrollers normally results in a greatly reduced component count and often eliminates the need for mechanical components which are subject to wear. Much greater reliability can therefore be expected from equipment using microcontrollers, and in general such high reliability is realized.

However, microcontrollers are now moving into areas where only the very lowest fault levels can be tolerated, and where the consequences of system malfunction can be costly and even dangerous. Applications such as the control of large mechanical or electrical systems, vehicle control, and telephone exchanges are typical examples.

In such applications, secure, uncorrupted and bug-free programs cannot be assumed, and the designer must take measures to ensure that transient program or data errors, or deeply hidden software bugs, do not result in system failure.

This article discusses some of the techniques that can be advantageously used in designing highly fault-tolerant software for microcontroller-based systems. As an example, the design of software for a sophisticated PABX telephone exchange junction using MAB8400 series 8-bit microcontrollers is described. Tests on the system under extreme noise conditions showed that with conventional software, significant unrecoverable errors occurred, whereas the same system operating with the fault-tolerant software proved extremely rugged.

The general techniques outlined are applicable to any microcontroller-based system and should be considered for any system where software failure might prove hazardous.

GENERAL CONSIDERATIONS

Microcontroller-based systems are fragile because for correct performance they rely on a software 'edifice' whose structure can only be maintained by the supply of valid machine code instructions to the CPU. The corruption of just one byte can result in incorrect interpretation, leading to a temporary or even permanent collapse into random logic execution, and the destruction of RAM data. The effect on the system of such a collapse is unpredictable and its severity depends on the application.

The design of fault-tolerant software for interfacing this TBX3000 digital PABX with a public exchange junction illustrates the principles discussed here

As an illustration of potential software fragility, consider a microcontroller-based system executing some 10^5 bytes of machine code per second in normal operation. To perform without failure over a five year period of continuous operation, say, the system must successfully execute about 1.6×10^{14} sequential bytes. It seems unreasonable to assume that such a long string of machine code operations could be performed without failure, particularly in view of error sources such as noise, program faults, memory faults, or marginal faults in the CPU and associated circuitry.

The difficulties in correcting for such errors are enhanced by the use of variable byte-length instructions, and by the lack of memory error correction. Problems also arise because the microcontroller cannot discern the significance of the machine code being executed (that is, data or instruction code). Therefore, at the most important and fundamental level, there is no mechanism for failure detection. This situation may be alleviated to a significant extent by adopting the design techniques outlined later in this article. However, before discussing methods of achieving fault tolerance, it is worth considering error sources in more detail to obtain an appreciation of their contribution to possible system failure.

Error sources

Program faults

It is generally accepted that bug-free software is a difficult, if not impossible, target. It must be assumed, then, that any software above a trivial level of complexity has resident bugs. Moreover, it is usually impossible in practical and economic terms to subject a system to the full combinatorial range of stimuli in a laboratory environment. Even after field trials, there are usually some faults of a subtle nature left unexposed.

Noise

Noise transients, produced for example by lightning, electromagnetic components in a control system, and heavy duty equipment on the same mains circuit, tend to be underrated as error sources. They give rise to 'apparent software failure' and their effects include:

- corruption of memory Reads, resulting in changed data or incorrect instruction code
- corruption of memory Writes, giving incorrect data at one or more RAM addresses
- initiation of hardware-driven CPU functions such as reset, false-interrupt generation, or processor halt
- interruption of the clock supply; this is rare but possible and will cause indeterminate effects in dynamic processors.

Most of these effects can lead to serious software failure and, because of their transient nature, are difficult to identify. In all systems, it is important that well-proven procedures for circuit decoupling are adhered to.

Memory faults

Strictly, these are hardware failures, and they result in data or instruction code corruption. If they occur in little-used routines, they may give transient-like errors.

Effects of transient errors

In a hardware system, transient errors are unlikely to cause permanent catastrophic failure since the physical integrity of the system (that is, interconnections, chip functions, etc.) is unaltered. This is not the case in a software system where, by analogy, the interconnections and circuit functions are represented by sequences of machine-code instructions and data which, even if embedded in ROM, may be interpreted by the CPU as meaningless (from a system function point-of-view) strings of code. It is as if, in a hardware system, the interconnections and circuit functions were being randomly and repetitively re-arranged. Transient errors can result in:

- random logic execution of indefinite but potentially infinite duration
- looping without return to normal sequence
- initiation of halt conditions.

The effect on external devices being controlled by such random processing is clearly unpredictable.

SOFTWARE FAULT TOLERANCE

Implementing hardware functions in software significantly reduces the incidence of trivial system failure. However, the probability of catastrophic failure may increase and the effect on the system can be more severe. Nonetheless, the very real advantages of software-based microcontroller systems (greater flexibility, smaller physical volume, broader application, and lower cost) still outweigh the penalties incurred (more memeory required, less available processing time) provided the fault tolerance of the software is maximized. A reasonable minimum objective for fault tolerance in a software-based system can be stated as follows: *The response of the system to transient failure should be no worse than that of the hardware system it replaces, even though performance and flexibility are improved.*

Improvement in fault tolerance and reliability implies a degree of redundancy and extra processing, resulting in greater memory usage and lower processor availability for

prime tasks. This, however, would seem to be contrary to the aims of most system designers, who would reasonably be seeking minimum memory utilization and short program execution times. However, reliability has to be paid for, and experience suggests that an overhead in program code for diagnostic routines of 5% to 15% will give a significant improvement (except where exceptional security is required). The additional code that this implies is, of course, system dependent.

Because the CPU cannot differentiate between valid and invalid strings of code, it is not possible to prevent misoperation occurring. It is possible, however, to detect misoperation once it has occurred. Fault tolerance ultimately depends on the effectiveness of the diagnostic and recovery procedures employed. The following points are recommended for serious consideration.

- Consider the diagnostic check and recovery procedures as an inherent part of the design; do not add recovery mechanisms as an afterthought.
- Determine the effect of potential failure in the operational environment; this defines the degree of security and the sophistication of the recovery procedures required. It also determines whether duplication of software is necessary.
- Aim for simplicity in software, data, and supervisory structures. In practice, complex software requires complex recovery mechanisms.
- Ensure that there is at least one restart address to which software execution can be forced by external means. This guarantees escape from random logic execution.
- Minimize the sub-routine nesting depth to simplify the recovery methods. If possible, keep to a single level (that is, for interrupt handling). Accept the resultant increase in program code as a reasonable trade-off for ease of recovery.
- Provide back-up in RAM for that data which is essential for software supervision. This will permit 'intelligent' restart.
- Fill every vacant memory location with single-byte instructions and provide a jump to a 'safe' destination at the end of each infill area. This 'traps' invalid jumps into vacant memory since it provides a secure exit mechanism.
- Determine the smallest real-time period within which recovery must be achieved. This defines the required frequency for diagnostic checks and the response time for recovery.
- Examine the effects of an invalid reset (caused, for instance, by noise). For example, if power-on reset initialization would be catastrophic should it occur at any other time, then the reset invoked during recovery must omit the initialization procedure. In this case, a latch can be used to determine that power-on reset has already occurred.
- Keep in mind the technology and architecture of the processor to be used. For example, compared with dynamic processors, static types are less affected by an interruption in the clock supply. Note also that processors operating with three-byte instructions are more likely to enter into random logic execution than two-byte instruction devices. A benchmark comparison indicates that systems using two-byte instruction devices are two to three time more secure against crashes due to program fetch errors than those using three-byte types.

Error prevention

In the initial design phase, action should be taken aimed at preventing incorrect operation by, for example, 'tying down' unused interrupt vectors and 'padding out' branch tables with defined exits. For example, interrupt vector locations should always be filled so that if incorrect arrival at the vector occurs, the program will be directed to a safe destination. Similarly, branch tables not completely filled should be padded out with default values to safe destinations.

Maintenance of integrity

It is essential that vital control variables such as RAM pointers and table indices are kept within valid bounds. (For example, index registers used with branch tables of length, say, 16, should be checked for values not greater than 16.) Such containment can, under fault conditions, prevent an excursion into uncontrolled random logic execution although it will not necessarily prevent some illogical function sequences.

Data preservation

Variable data is repetitively set up, in contrast to a once-only operation, thus providing a continuous data recovery facility without the need for specific administration and diagnostic procedures. For example, an instruction issued to a critical I/O device cannot be assumed to be indefinitely valid; it should be reinforced periodically.

FAULT-TOLERANT SOFTWARE IN A PRACTICAL APPLICATION

As an example, the design of fault-tolerant software for a U.K. public exchange junction interfacing with a TBX3000 digital PABX is described (Fig.1). To keep component count and cost to a minimum, the system is implemented using MAB8400 microcontrollers with external EPROMs, each time-shared over four circuits (Fig.2 and 3). Maximum use is made of software in realizing circuit functions such as the detection of telephone ringing waveforms and contact debounce. Although the design is inexpensive and reliable, it is vital that the system runs for long periods without catastrophic failure. Malfunction on just one junction card can result in the loss of four external lines.

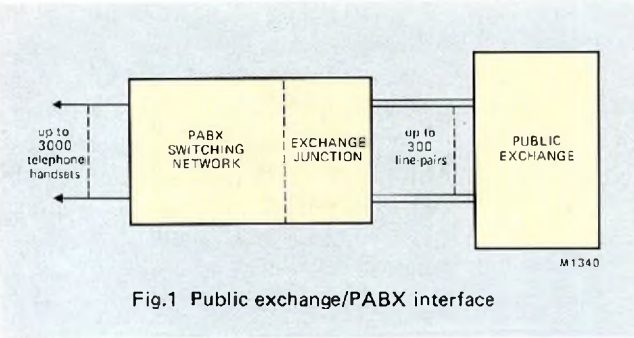


Fig.1 Public exchange/PABX interface

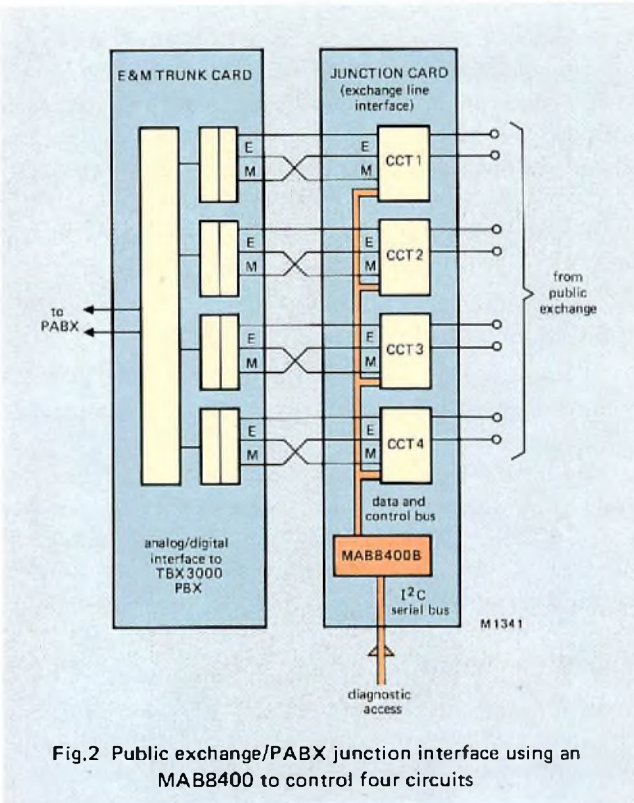


Fig.2 Public exchange/PABX junction interface using an MAB8400 to control four circuits

The traffic handled on a PABX/public-exchange junction is usually heavy in the 'busy' hour. The loss of even a small number of circuits during this period, with the consequent increase in traffic on the remainder, can lead to an objectionable increase in route blocking, particularly in small systems. Even a trivial processing error, if not recovered, can have a disproportionate effect on system operation since it is likely to lead to looping or random logic execution. Two serious effects of this are:

- Permanent 'lock-out' of the four circuits. This need not necessarily render the circuits busy to new calls; the circuits may accept calls but not switch. This can be particularly aggravating in certain types of business (e.g. mail order).
- Generation of spurious line signals. This leads to intermittent seizure of the public exchange and false indication of incoming calls at the PABX.

In the system described, the MAB8400 junction processor has no communication with the TBX3000 CPU and is therefore totally reliant on autonomous measures for recovery in the event of a fault condition. Furthermore, the junction design does not include a hardware watchdog timer, and therefore recovery must be achieved entirely by software means.

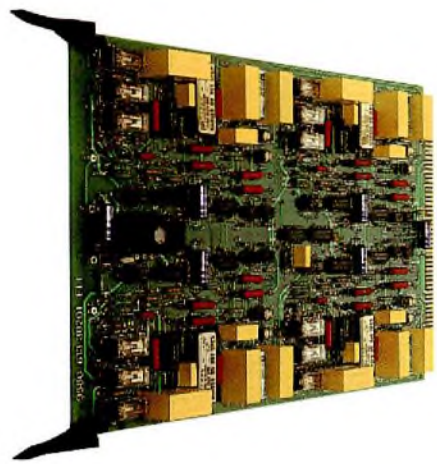


Fig.3 Junction card

Software structure

The software is partitioned into two distinct sections: Real-Time Software (RTS) and State Processing Software (SPS) (see Fig.4).

The Real-Time Software is interrupt-driven from the internal timer at 5,5 ms intervals and controls all I/O functions, input signal integration, digit regeneration, impulsing (10 impulses per second), ringing waveform analysis, circuit selection and scanning, and timer interval updating.

The State Processing Software controls the telephony functions on a state-driven basis. State transitions are handled by a supervisory program (part of the SPS).

A detailed diagram of the software structure is shown in Fig.5.

Reliability measures

The term 'catastrophic failure' in this application does not imply any hazard. An occasional call failure can be tolerated, and consequently duplication in software or special measures to guard the reset condition are not necessary. The real-time telephony environment will allow a slip of two 5,5 ms system real-time periods for diagnostic and recovery action before any significant degradation of performance occurs. Recovery requires restart of internal timer, initialization of the sub-routine stack level, and restart of the State Processing Software to continue execution of the current system state.

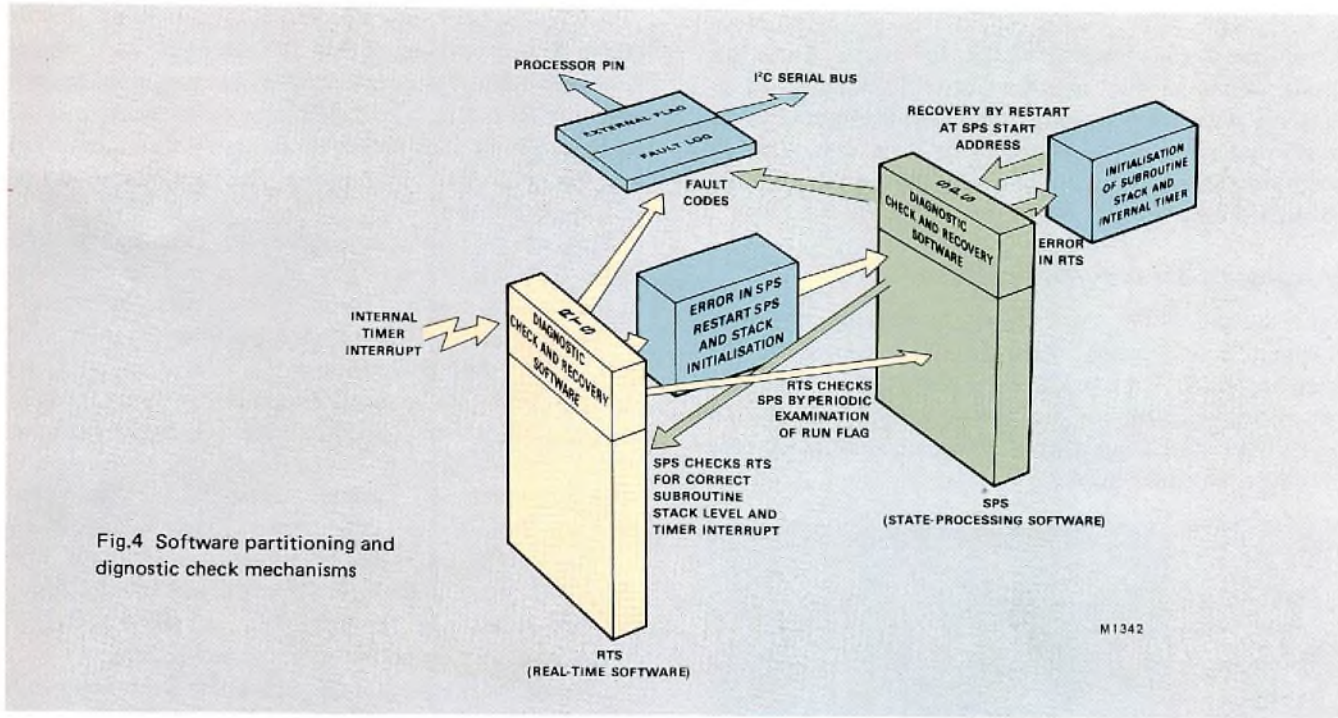


Fig.4 Software partitioning and dignostic check mechanisms

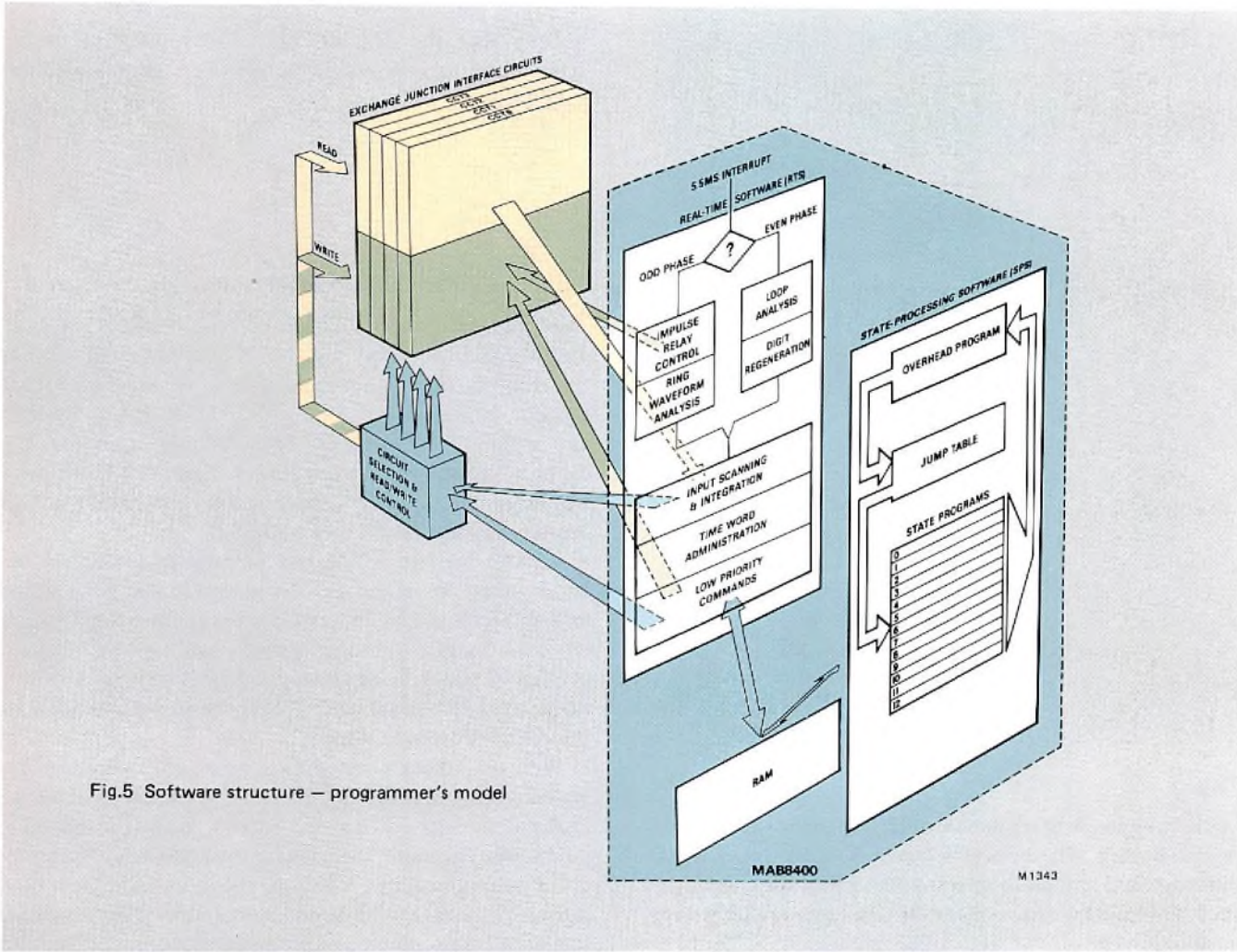


Fig.5 Software structure — programmer's model

RAM data is not backed up in this application since dependence on historical RAM data is minimal. There is a strong likelihood that, in the event of RAM-data corruption, the system will reprocess the current telephony input signals and arrive at the correct state, or at a state which will maintain transmission between the two parties involved in a call.

Microcontroller sub-routine level

Since the sub-routine stack is open to corruption, its level is limited to one; that is, there is only one sub-routine, the complete RTS. The stack level is zero during state processing. Since there are no nested sub-routines, the recovery procedure is greatly simplified, albeit at the expense of some additional PROM.

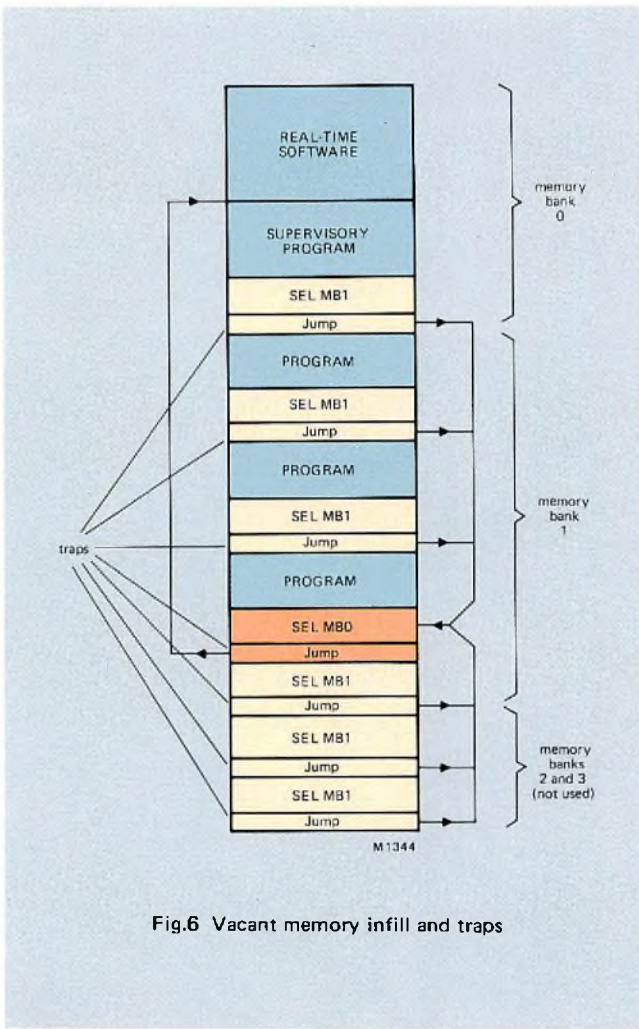


Fig.6 Vacant memory infill and traps

Traps

In this system, a timer/counter (T/C) interrupt is the only valid interrupt. The effects of false external or serial I/O interrupts are limited by placing RETR (return from interrupt sub-routine) instructions at the appropriate vector locations.

A T/C interrupt, invoking the RTS, should only occur during SPS execution. Should the interrupt occur during RTS execution, it is a fault and will be recognized as such when the RUN flag in the state program is checked. If the RUN flag is invalid, the RTS returns to the start of the supervisory program by 'forcing' the start address in the return address stack.

Program modules are mapped for linking, with gaps deliberately left between them so as to avoid the possibility of overrunning page and memory boundaries. One result of this is that sections of memory between programs, and between the last program and the end of memory, are vacant. This vacant memory is used in the system to 'trap' improper jumps; see Fig.6. An unconditional jump instruction is inserted prior to each program and at the end of memory. Remaining vacant areas are filled with 'Select Memory Bank 1' (SEL MB1) instructions. Should an improper jump be made into an unused memory area, then the jump instructions return control to the supervisory program located in Memory Bank 0, via intermediate SEL MB0 and an unconditional jump instruction.

The vacant memory infill bytes represent *single-byte* instructions and therefore guarantee sequential program execution until the next trap jump is required.

Note that the SEL MB instructions preselect the required bank and are only effective when an unconditional jump is executed.

OPERATIONAL RESULTS

The vulnerability of the system to fault conditons was observed under laboratory conditions both with and without the recovery mechanism in operation. With the prototype junction card installed in a TBX3000 laboratory system, and without the recovery mechanism in operation, occasional catastrophic failures were observed. These were significant, particularly in view of the electrically-benign conditions under which they occurred.

A large increase in the rate of catastrohpic failure occurred when the junction card was used to verify the design of a production junction card tester. The increased failure rate was found to be due to noise, produced by 'unquenched' reed relays, being transmitted back via a +12 V power supply into the mains, and from there via a +5 V supply to the MAB8400 supply pins.

With the recovery mechanism again not operating, the system was subjected to 30 ms, 3 V peak-to-peak noise bursts at the rate of 10 bursts/second, applied to the +5 V power rail. The noise was generated by a T51 relay operating via a self-interrupting contact; the noise spectrum was similar to that of the production tester. Failure modes similar to those observed previously occurred and analysis

showed them to be either random logic execution, internal timer disablement, or reset. (The occurrence of reset was relatively rare compared to the other fault conditions.)

Under the above conditions but with the recovery mechanism now operating, no catastrophic failures were observed. Subsequent monitoring of fault recovery flags indicated that failures were indeed occurring but that the recovery mechanism was entirely effective.

It was concluded from these results that the degree of fault tolerance designed into the system is sufficient to meet operational field requirements. This conclusion was reinforced by further trials in which software execution was started at 'random' memory addresses (even in the middle of multi-byte instructions) in an attempt to induce catastrophic failure; no failures were observed. (The latter tests were carried out using a microcontroller development system in debug/ICE mode.)

FURTHER MEASURES

In some systems, further integrity may be desirable; the techniques described above can be enhanced as follows.

System logic breakdown

The software described here is based on the state transition method, and it is possible to validate state changes by reference to a table of permissible state transitions (current and previous transitions are recorded). Depending on the required design sophistication, system logic breakdown can be handled either by exiting to specific fault handling states, or by recursion to the previous state. In applications where the response of the external environments is slow compared with the recovery time (as is so in telephony), recursive handling is obviously the simplest procedure to adopt.

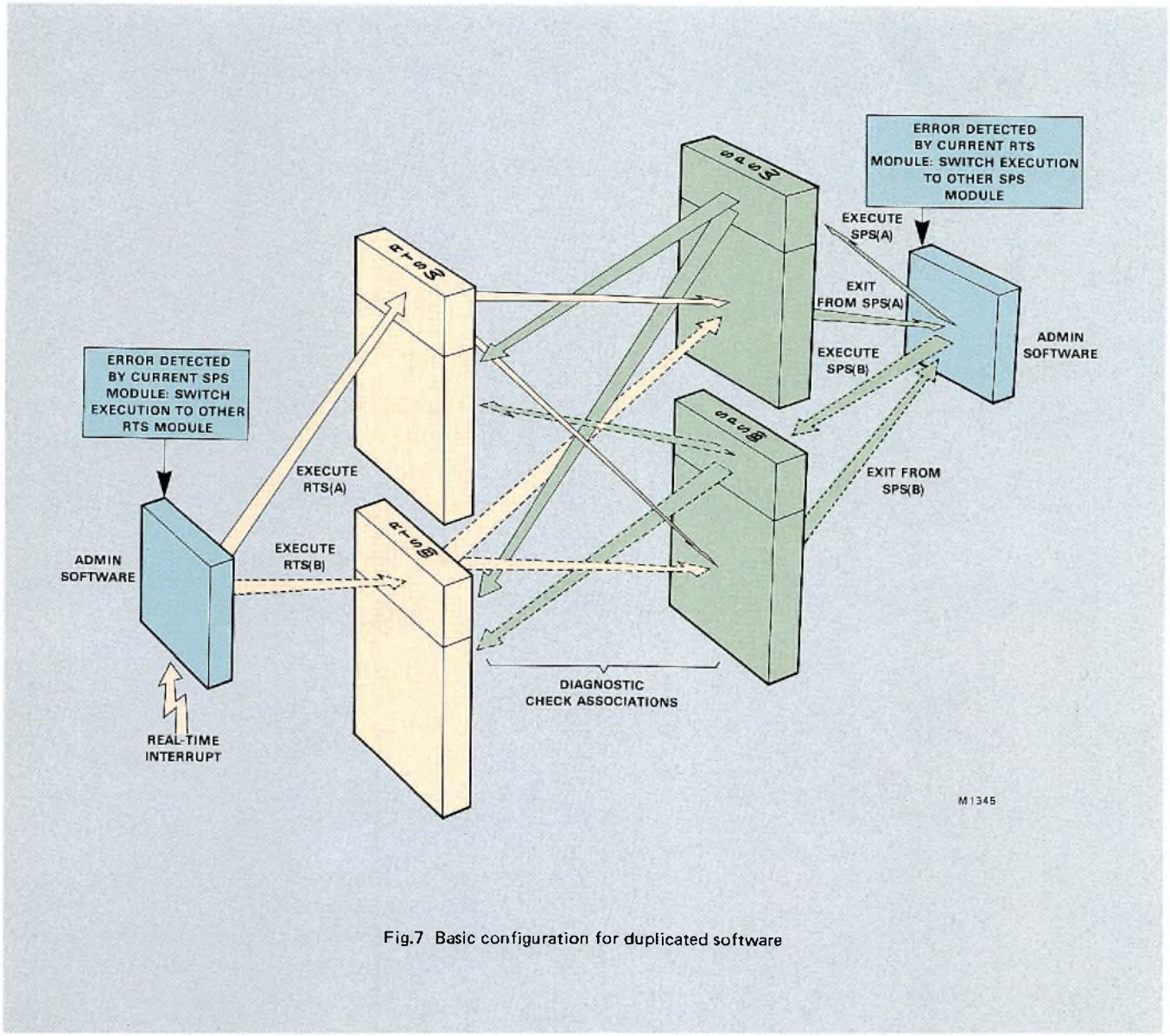


Fig.7 Basic configuration for duplicated software

Memory failure

In some microcontrollers, extensive memory expansion is possible. Although failures in this memory are strictly hardware failures, in operational terms, the effects are identical to those caused by other factors; that is, the outcome is an apparent software failure with all the potential effects outlined earlier.

The normal method of overcoming this problem is to perform periodic tests on RAM and checks on the validity of program memory, further processing being aborted under fault conditions. Whilst this is a fail-safe procedure, it is not fault tolerant.

To achieve fault tolerance in program memory, redundancy must be incorporated in the system either in the form of error correction or direct duplication of program. For the design described here, the latter is the only option. Thus both real-time and state-processing software modules are duplicated (see Fig.7).

Any of the four operating combinations are permissible. During recovery, RTS/SPS combinations are reassigned. If, for instance, a failure is detected by an RTS module in an SPS module, the restart is switched to the supervisory program of the second SPS module. The procedure is identical for a failure detected during SPS execution.

At the cost of a small increase in diagnostic intelligence, discrimination can be made between permanent failure and transient failure. This leads to the interesting possibility that, in the event of recording a permanent failure in both modules in one half of the system, the failure is likely to be due to pure software error since permanent memory faults are unlikely to occur in both modules simultaneously.

Computer controlled teletext

J. R. KINGHORN

During the last few years, teletext has firmly established itself in the domestic tv market. A major factor in this rapid expansion has been the proven performance of the first-generation teletext decoders. As the price of the decoder board falls and its features improve, the size of the market is expected to rise still further. The next generation of decoders, known as Computer Controlled Teletext, CCT, offers a range of improved facilities and is now available.

The UK teletext signal conforming to the original BBC/IBA/BREMA specification of 1976 is known as Level 1 teletext. This is the first in a series of downward-compatible teletext Levels from 1 to 5. Each level has improved features in relation to the preceding level; for example, pastel colours and more advanced graphics. To obtain downward compatibility, "ghost rows" (invisible to first-generation teletext decoders) will be transmitted in association with the normal data. The ghost rows will contain the extra information required for the higher teletext levels (Ref.1).

There are two basic categories of functions performed in a teletext decoder. Firstly, there are the standard functions fixed by the broadcast specifications which are always performed in the same way; for example, data slicing and sync generation. The second category consists of functions that are liable to differ significantly between different customers and applications, for example the displayed language.

The second-generation decoder distinguishes between these two basic categories to allow, in a very cost-effective manner, much more flexibility in the facilities offered. The fixed functions are performed by dedicated circuitry in the ICs. The variable functions are performed in software by an associated control microcomputer. This controls the European computer-controlled teletext chip, type SAA5240, referred to as the EURO CCT. (EURO, European, indicates that this IC is for 625-line operation).

The EURO CCT based decoder is shown in Fig.1. This example has storage for eight pages. It makes use of the rapid advances in fabrication technology made since the first-generation teletext decoders were designed. It combines the functions and improves on the performance of several chips used in the original decoders. A new Video Input Processor (VIP2, SAA5230) improves the performance of the decoder under poor signal conditions. The control microprocessor with associated memory uses the I^2C (Inter-IC) serial data transfer bus (Ref.2).

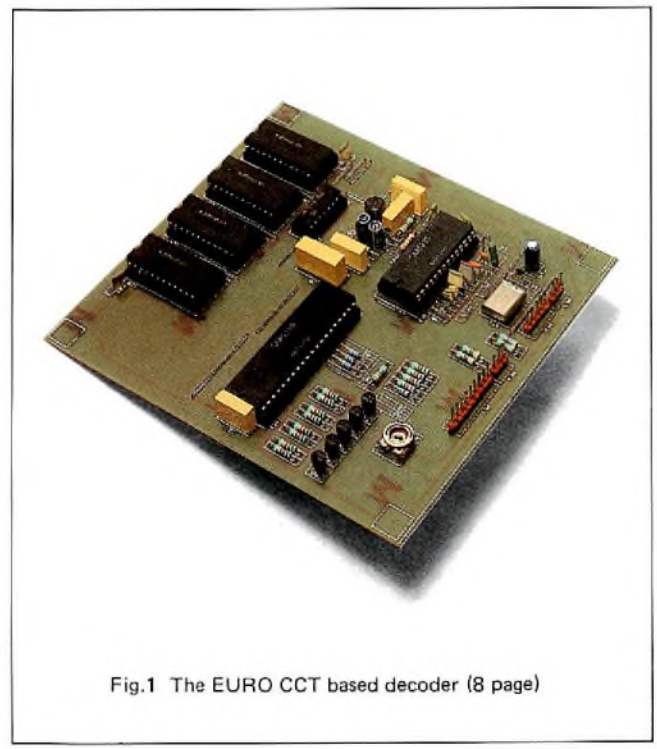


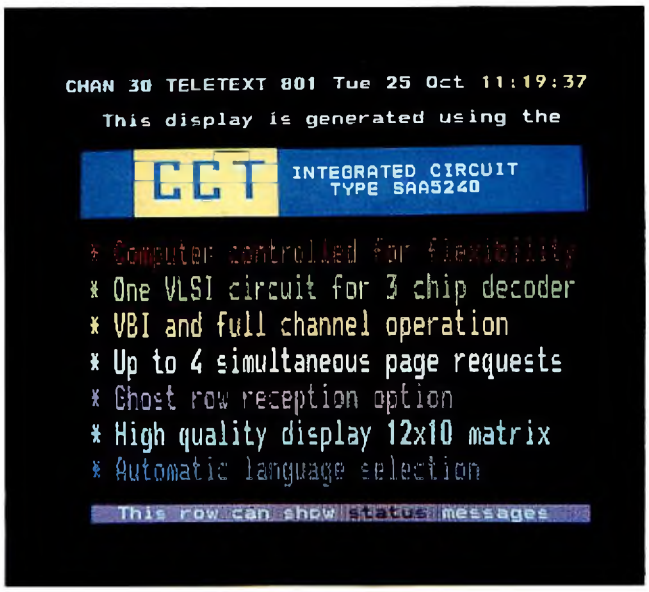
Fig.1 The EURO CCT based decoder (8 page)

The system has improved display characteristics, providing a non-interlaced display from an interlaced tv transmission to reduce flicker. Also, a major improvement in character shape is achieved by using a 12 x 10 dot resolution ROM in place of the original 5 x 9 type.

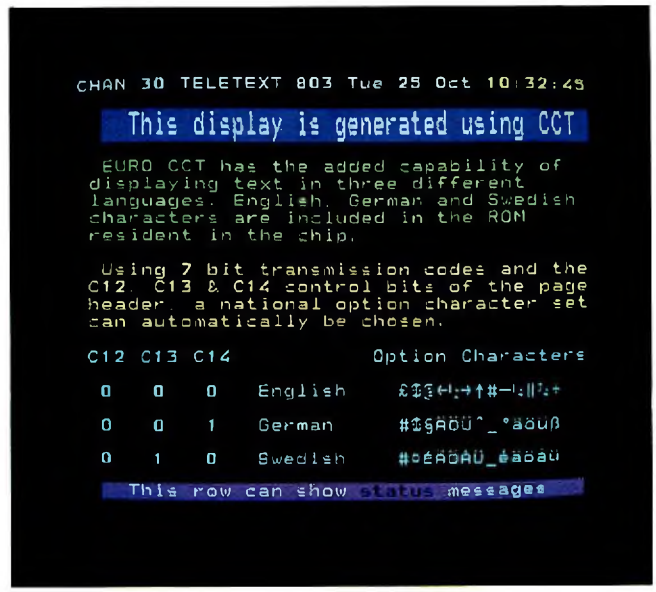
The EURO CCT is basically a Level 1 decoder with some enhanced features. One of these features is the ability to capture the data required for all the planned levels, although in its standard form it cannot display the extra information. It does permit, however, facilities like linked pages, automatic display language switching, programme service rows and telesoftware to be used when sufficient additional resources are built into the decoder. This usually means extra software in the control microcomputer.

Another feature of this type of second-generation decoder which may become important is the ability to capture data in full-channel mode, that is with teletext data on all tv lines. This allows a high data transfer rate, (approximately 600 pages/second) on a dedicated channel such as satellite or cable tv or even on simple data distribution networks.

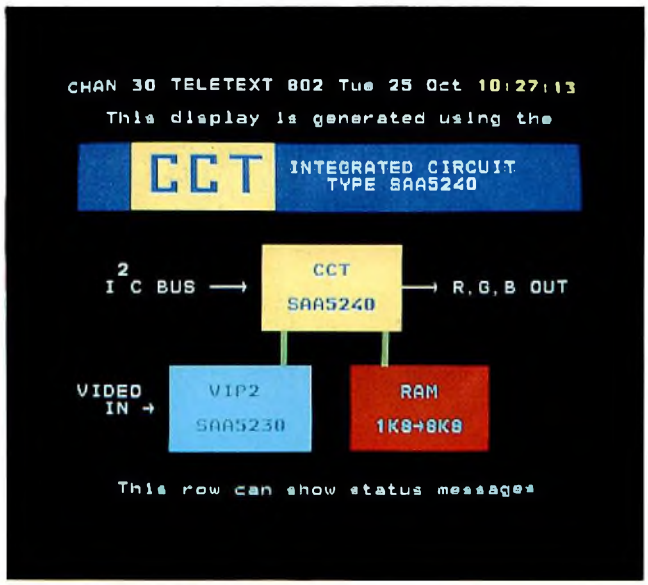
From the user's point of view, access time to the required page is of prime importance; in this respect the ability of the EURO CCT to search for up to four pages simultaneously is a real advantage. Also, helpful status messages can be



(a) General text display



(c) Multiple language options



(b) EURO CCT block diagram

(d) Multiple language options

Fig.2 Sample EURO CCT generated telext page

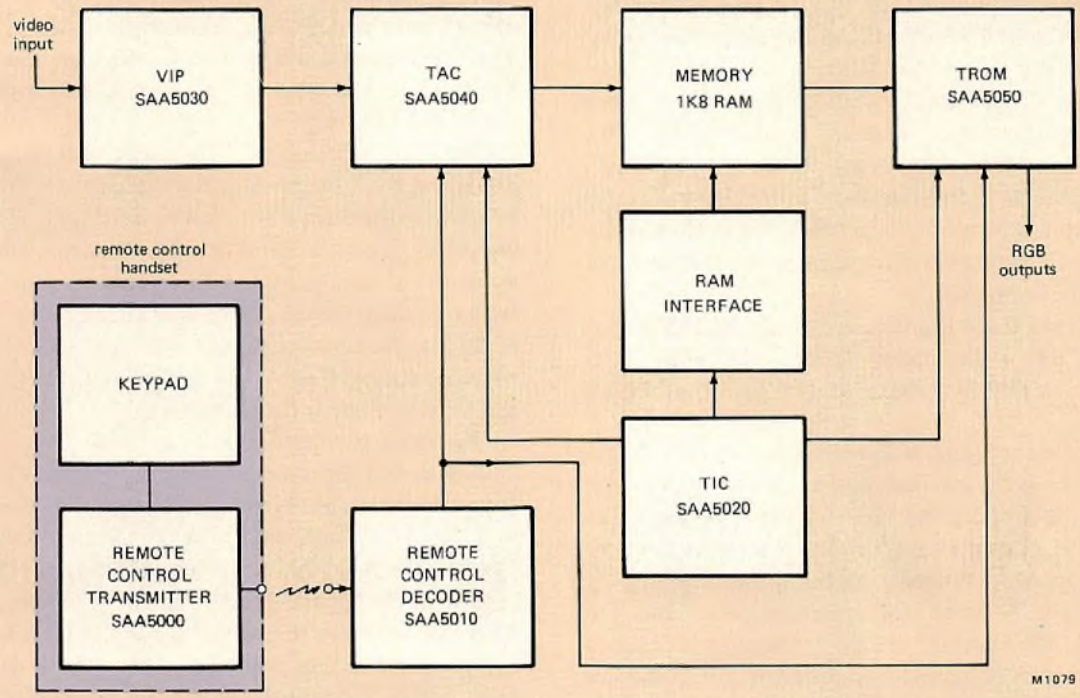


Fig.3 First-generation LSI teletext decoder

generated locally and displayed on a separate row either above or below the main text.

Some of the EURO CCT features are illustrated in Fig.2 which shows four simulated pages displayed on a domestic receiver. In Fig.2(a), the major advantages of the system are listed in double-height characters using the standard high-resolution dot display. The status row is available for locally generated messages and is shown beneath the main text. Figure 2(b) shows a basic block diagram of the EURO CCT based decoder. Figure 2(c) illustrates the fact that up to three different languages can be displayed using the same EURO CCT chip (previously a change of TROM was necessary to change language). In this case English, German, and Swedish are shown. However, a mask programmed device variant can be used to provide any three Latin-based languages. The language is normally automatically selected by the control bits in the page header. More than one language can be displayed on a single page, however, using ghost row transmissions, as shown in Fig.2(d).

A EURO CCT based teletext decoder can be built on a single-sided printed circuit board, and indeed many set-makers may decide to incorporate the decoder into the main tv board to reduce costs. EURO CCT allows more complex and sophisticated systems to be custom built by adding extra resources (hardware and software) while maintaining a low cost for the simple basic decoder.

FIRST-GENERATION LSI TELETEXT DECODER

The block diagram of the first-generation LSI teletext decoder with remote-control handset is shown in Fig.3. It consists of 12 ICs including two for the infrared user-control link normally positioned separately from the main decoder board. The basic decoder functions are performed by:

- VIP (Video Input Processor) SAA5030 – a bipolar linear device which provides serial data and clock derived from the incoming video signal. It also arranges timing synchronization for the rest of the decoder.
- TAC (Teletext data Acquisition and Control) SAA5040 – a digital NMOS device which arranges the capture of the requested page into memory. It is also concerned with the overall decoder control and writing user status into memory.
- RAM–1K8 bytes of memory for page storage with standard LSTTL circuits to provide an interface.
- TROM (Teletext Read Only Memory) SAA5050 – an NMOS device containing a ROM for generating characters from a dot matrix and other control functions.
- TIC (TIming Chain) SAA5020 – an NMOS device providing timing and addressing signals for the whole decoder.

These components are mounted on a single decoder board.

EUROPEAN COMPUTER-CONTROLLED TELETEXT (EURO CCT) BASED DECODER

A block diagram of the EURO CCT based decoder is shown in Fig.4. The video processing functions are performed by the VIP2, basically an updated VIP1, although the two are not compatible. The EURO CCT effectively replaces seven ICs in the first-generation teletext decoder (TAC, TIC, TROM, and four TTL interfaces). It does not include, though, the remote-control command processing and status functions, formerly carried out in TAC. These are now required to be programmable and are therefore performed in the control microcomputer.

Standard static RAM is connected to the EURO CCT as page memory. For a single-page decoder 1K8 bytes are required but up to 8K8 bytes may be used giving up to eight stored pages.

The control microcomputer is used to decode the remote-control pulses from the infrared receiver. It also controls the operation of the decoder and provides status messages. Depending on the particular application, the microcomputer may also control other tv functions, for example tuning.

The interface between the microcomputer and the EURO CCT is the standard I^2C bus. Although most data flow is from the microcomputer to the EURO CCT, the bus is bidirectional so that, for example, data in the page memory may be read by the microcomputer.

Video input processor VIP2, SAA5230

The bipolar linear IC VIP2, type SAA5230, performs most of the functions of the VIP1, type SAA5030, as shown in Fig.5. However, each function has been redesigned to improve performance and build on the operating experience gained with VIP1. In particular, the data extraction function has been designed to avoid the use of any critical components and it can be easily adapted to operate at different data rates. There are two VIP1 functions, field sync integrator and signal quality detector, which are not included in VIP2. These functions are now performed digitally inside the EURO CCT chip.

The data detector of VIP2 finds the slicing level for extracting the teletext data and compares it with the video to obtain sliced data. The slicing level can adapt itself to variations in data amplitude and to low-frequency disturbances such as co-channel interference, while remaining relatively unaffected by echoes, data content, or noise. An additional feature is that high-frequency losses in the signal are compensated if necessary to obtain a greater eye opening and to ensure better data reception.

The clock regenerator takes in sliced data and generates a clock in synchronism. It uses a continuous clock, derived from a free-running crystal oscillator, whose phase is shifted in a feedback loop until it is at the optimum point for latching the data. A PLL is not used as it would take too long to lock up; the present circuit will find the correct clock phase before the end of the run-in. This type of regenerator achieves less jitter than a tuned coil, with no critically adjusted components and no possibility of missed clock cycles causing a loss of bit synchronization.

The VIP2 contains a 6 MHz VCO which is the clock for the character display. This clock is part of a PLL required to synchronize the characters to the video; the PLL has been designed to allow the display to be locked to a VCR for status messages, etc. The chip includes a wide range adaptive sync separator for this PLL. The separated sync is also taken to the EURO CCT to perform field synchronization of the display.

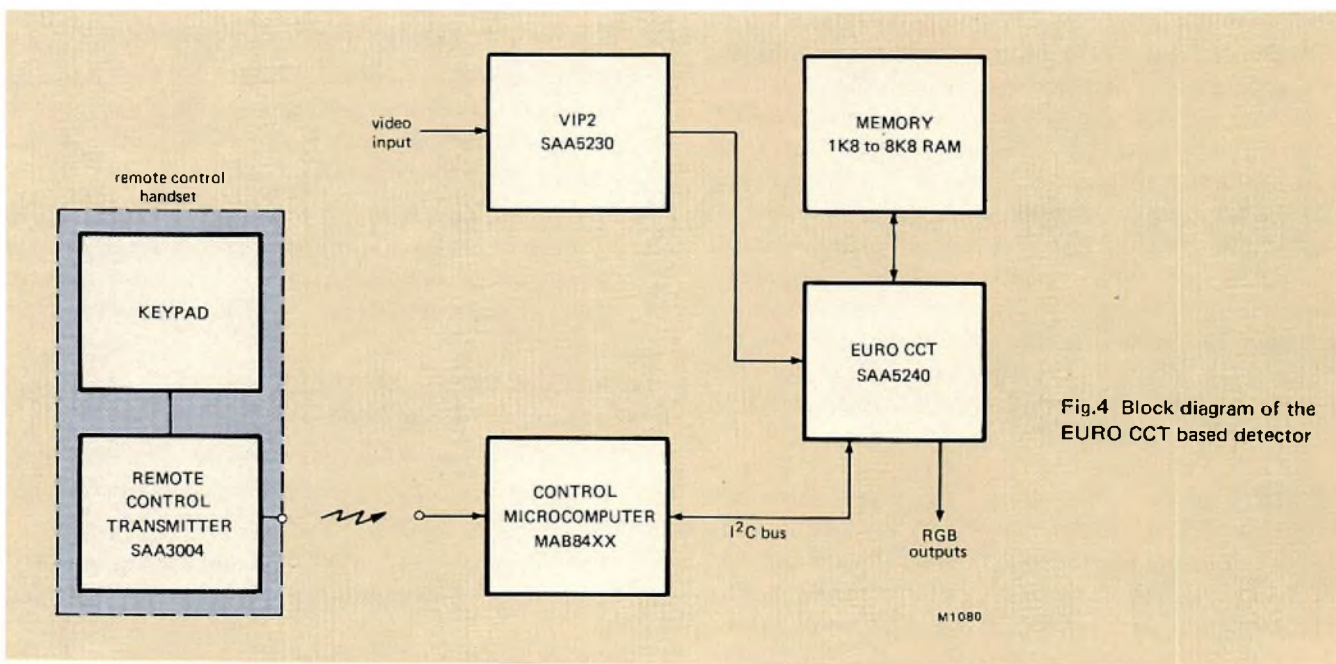


Fig.4 Block diagram of the EURO CCT based detector

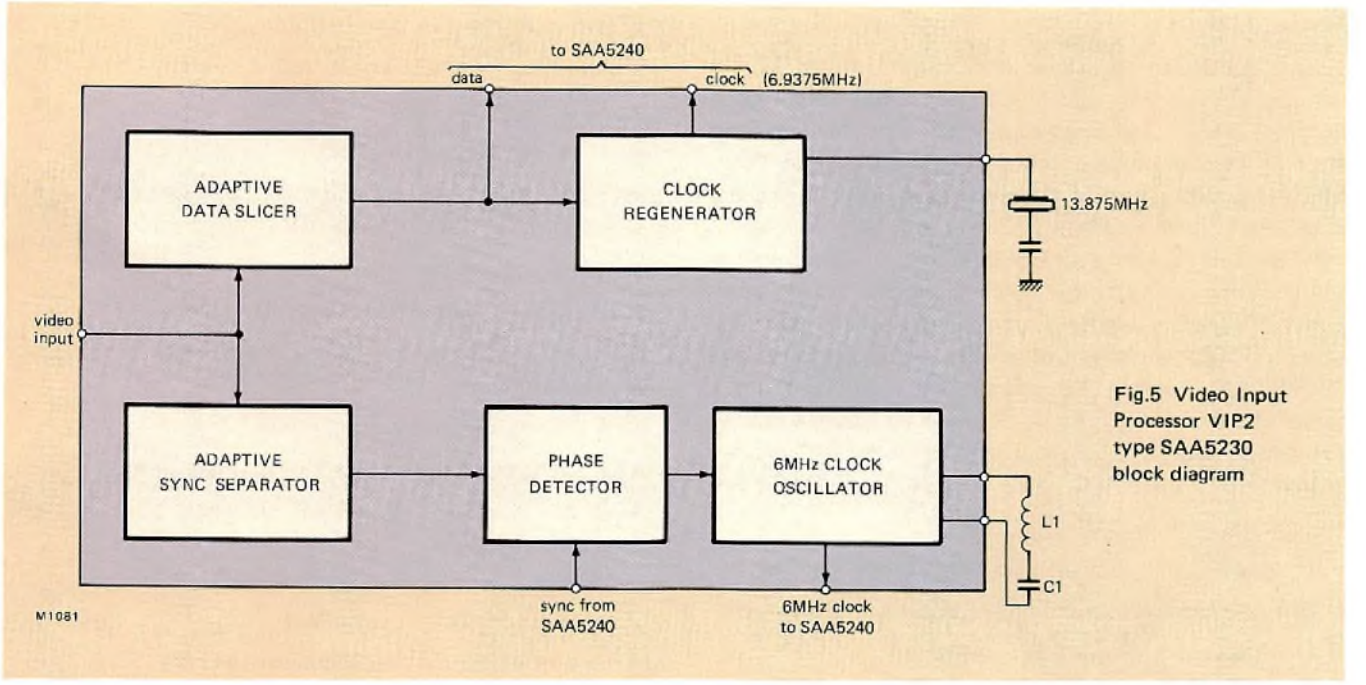


Fig.5 Video Input Processor VIP2 type SAA5230 block diagram

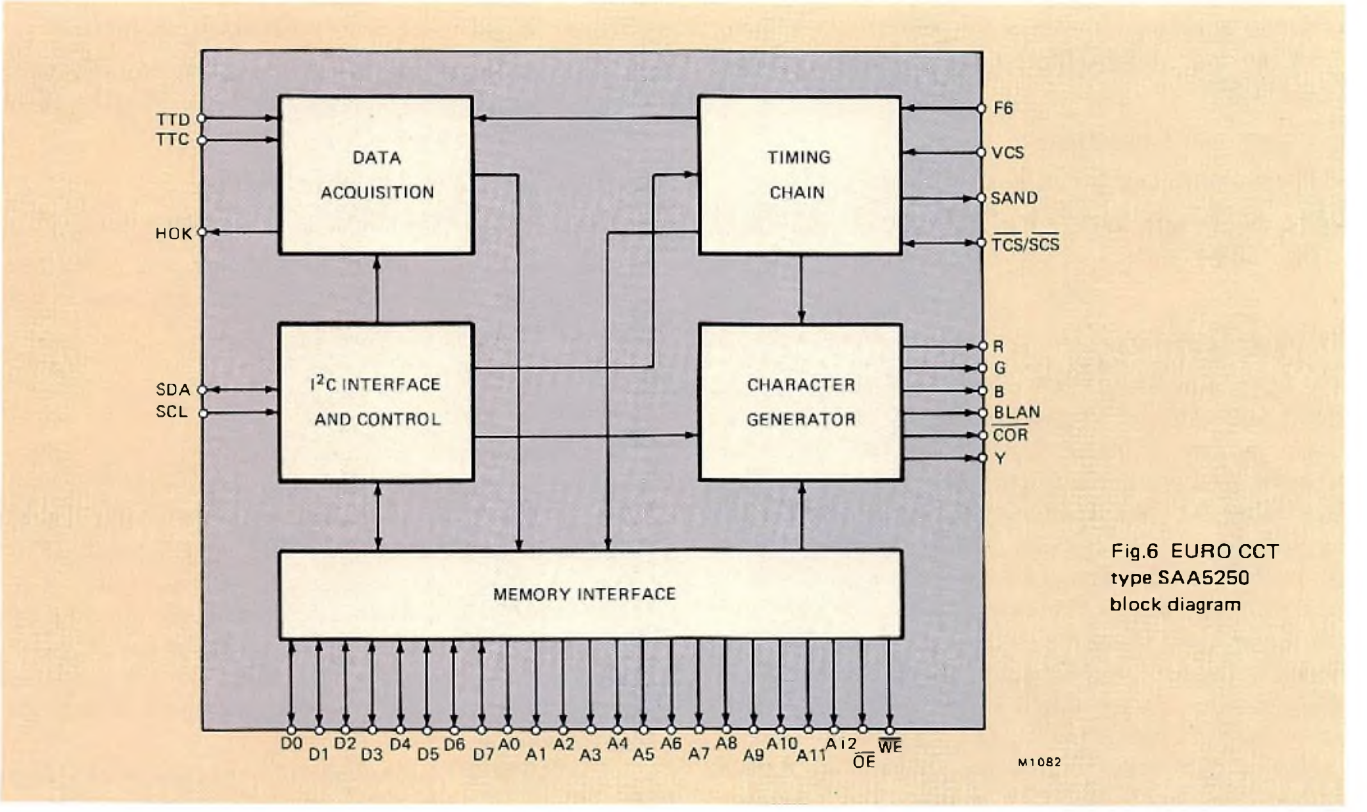


Fig.6 EURO CCT type SAA5250 block diagram

EURO CCT IC, SAA5240

A simplified block diagram of the 40-pin EURO CCT IC is shown in Fig.6. It contains five major functions: timing chain, character generator, data acquisition, memory interface, and I^2C interface and control.

Serial data and clock signals from VIP2 are input through the TTD and TTC pins, and the appropriate data is captured by the data acquisition function. It is then passed to the RAM via the memory interface and supplied to the character generator, which in turn provides RGB drive outputs for the video stages of the receiver or monitor. Outputs are also provided for blanking and contrast reduction of the tv picture (BLAN and $\overline{COR}$), together with a monochrome text signal for driving a printer (Y).

Timing chain

Timing signals for the whole circuit are provided by the timing chain function, which operates from a 6 MHz clock F6 from VIP2. Line synchronization with the incoming signal is performed by a phase-locked oscillator in VIP2, which is provided with a reference signal SAND from the EURO CCT. A composite sync waveform, VCS from VIP2, provides field synchronisation for the acquisition timing and also the display timing when interlaced display is selected. The display timing circuit generates a composite sync waveform, $\overline{\text{TCS}}$, which is used to drive the display timebases via VIP2; alternatively this pin can act as an input for a composite sync waveform to "slave" the display timing circuits. In summary, the main features of the timing chain include:

- Operates from external clock, VIP.
- Display format – 625 lines/25 rows/10 lines per row.
- Can generate interlaced or non-interlaced composite sync.
- User-selected double-height is available.
- Line counter for acquisition is independent of display.
- Software control of data entry period; that is either normal field flyback (lines 6 to 22), or all lines (full channel).
- Internal field sync integrator.
- Internal signal quality detector.
- Interfaces with VIP2 (SAA5230) but not VIP1 (SAA5030).

Character generator

The ROM in the EURO CCT contains 128 characters, each stored as a matrix of 12 dots horizontally and 10 dots vertically, leading to better display appearance and greater legibility than was previously the case. The 128 characters are selected by character address decoding and the ten lines by ROM line address decoding. The ROM is accessed once per microsecond providing 12 outputs corresponding to the 12 dots in each line of a character. A 64 μs rate signal from the timing chain clocks the lines per row counter, which normally divides by ten (except when double-height is selected). The counter output is used to select the appropriate line of 12 dots in the ROM.

The outputs from the character generator are R, G, B, BLAN, $\overline{\text{COR}}$, and Y, as shown in Fig.6. The Y output is active for the character foreground only, regardless of colours, and does not contain the flashing function. Blanking signals for the tv picture are supplied through the BLAN pin being combined dot, box, and full-screen blanking. All the character generator output pins have the open-drain configuration, making many different interfacing arrangements possible.

The main features of the character generator are:

- Display is based in 12 x 10 dot matrix.
- Interlaced or non-interlaced under software control.
- Serial attributes only.
- 128 alphanumeric characters.
- 3 national character sets (initially English, German, and Swedish; see Figs.2(c) and (d).
- 6 location auxiliary character set.
- RGB and Y outputs open-drain (true polarity).
- BLAN (blanking) and $\overline{\text{COR}}$ (contrast reduction) outputs are open-drain.
- Y output foreground colour only.
- Flashing is inhibited from Y output (for printers).
- BLAN output is combined character, box, and full-screen blanking.
- $\overline{\text{COR}}$ output allows contrast reduction for superimpose or boxes (software controlled).
- Double-height characters inhibited in row 23.
- User-selected double-height under software control. Large characters are then displayed quadruple-height.
- Separate status row, always available for software-generated messages. This may be displayed at the top or bottom of the screen, (under software control).
- Status row is always in single height.
- Decoding for black foreground colour is provided.
- Internal cursor inverts background and foreground colours. It may be made to flash using a software loop in the control microcomputer.

Data acquisition

The data acquisition section is enabled by a signal from the timing chain during lines 6 to 22 inclusive in field flyback mode or all lines in full channel mode. Serial data from the VIP2, type SAA5230, at 6,9375 MHz is applied to the TTD (Tele Text Data) pin via an external coupling capacitor. TTC (Tele Text Clock) is used to shift the teletext data into the EURO CCT from the VIP2. The serial data stream is converted to 8-bit wide parallel data bytes, and a byte counter keeps track of the incoming data and allocates it to the correct function.

The EURO CCT acquisition section is capable of searching for, storing in memory and constantly updating four pages simultaneously. In general the system operates as if there were four entirely different acquisition circuits. In non-ghost row mode, up to eight pages may be stored although only four at a time may be kept updated.

With first-generation teletext decoders there are two methods of requesting a page – normal and timed. The former requires three digits and ignores the sub-code whilst the latter requires all seven digits to be specified. The

EURO CCT includes a much more flexible option – the "don't care" facility. This method allows pages to be acquired when the full numbering allocation and transmission sequence is not known in advance.

The major features of the acquisition section are:

- Accepts UK standard teletext transmission.
- Automatic switching of character sets by C12, C13 and C14 bits of the page header (see Figs.2(c) and 7).
- Ghost rows can be accepted for processing by the microcomputer (up to 24 rows per page). 2K8 bytes of memory are used per page, hence there is a maximum of 4 pages in this mode.
- All transmitted control bits and addresses can be read by the microcomputer (after hardware Hamming checks), for any stored page.
- Up to 4 simultaneous page requests are allowed in either field-flyback or full-channel mode.
- Software selection of field-flyback or full-channel data operation.
- "Don't care" facility is available on magazine, page and sub-code digits.
- In field-flyback mode, automatic clearing of old page on first reception and clearing when page header bit C4 is set.
- In full-channel mode, the clear functions are not available so pages should be transmitted non-row-adaptively.
- Central part of the page header rolls, in green, when the page in the display chapter is being looked for.
- Broadcast (rolling) time is always directed to the display memory.
- 8-bit data reception option on all rows (for example, telesoftware), or normal 7-bits plus parity (under software control).
- Output indicating valid data line (for echo equaliser interface).
- Acquisition function may be switched off under software control.

Memory interface

The memory interface has 8 parallel data input/outputs (D0 to D7) and 13 address outputs (A0 to A12) which interface up to 8K bytes of static RAM. Control signals $\overline{OE}$ (Output Enable) and $\overline{WE}$ (Write Enable) are also provided. The RAM cycle is 500 ns, with in general one write and one read cycle every microsecond. In summary, the major features of the memory interface include:

- Interfaces up to 8K RAM providing up to 8 stored pages in normal mode or 4 stored pages in ghost row mode.
- 500 ns memory cycle time.
- Timings for static RAMs only, 200 ns access time is sufficient.
- I^2C bus can address any RAM location for reading and writing.
- Address converter from row or clumn to 10 bits is included and addresses all 1024 locations.
- All memory automatically cleared to "space" on power-on.
- Separate address counters for display, data acquisition, and I^2C bus. I^2C bus address counters allow incrementing and presetting.
- RAM locations not used for display or data acquisition purposes are available for use by the control microcomputer.
- All RAM accesses (display, acquisition and I^2C bus) are synchronous with system clock.
- All pages can be cleared, one at a time, under software control.

I^2C bus interface and control

The I^2C bus and control section provides the means of controlling the variable functions of the EURO CCT, either directly using mode-register bits or indirectly via the memory devices. The I^2C bus slave transceiver accepts commands from the microcomputer via the SDA and SCL (serial data and clock) pins. The main features are:

- Standard I^2C bus slave transceiver.
- Operates from 0 to 100 kHz.
- Acknowledge function is performed.
- Position registers auto-increment after certain commands or may be directly addressed.
- Auto-increment between certain command registers as well as direct addressing.
- All RAM locations are accessible via the I^2C bus for reading and writing.

EUROCCT memory organization and register maps

Figure 7 shows the organization of a page memory. The EURO CCT provides an additional row compared with first-generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

The first 10 bytes of row 25 contain control data relating to the received page and this is detailed in the expanded section at the bottom of Fig.7. Seven digits are used to identify a page: magazine (page hundreds), page tens, page units, hours tens, hours units, minutes tens, and minutes units. (The names of the last four digits are from an obsolete application as time coded information.) Bits C4 to C14 are used to control various display facilities; see Fig.2(c) for an example.

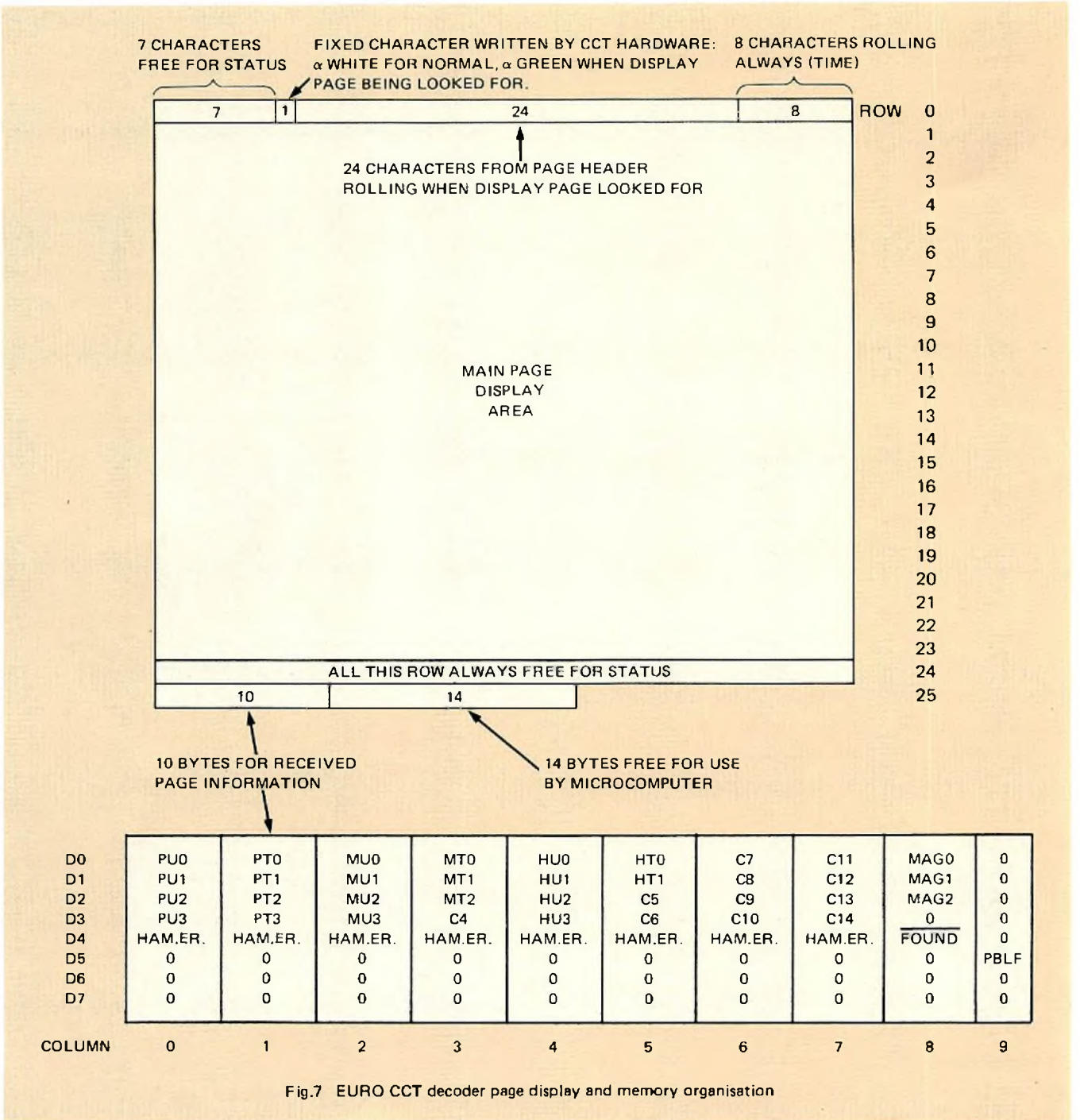


Fig.7 EURO CCT decoder page display and memory organisation

The abbreviations are:

MAG	magazine	page number
PU	page units	
PT	page tens	
MU	minutes units	page sub-code
MT	minutes tens	
HU	hours units	
HT	hours tens	
$\overline{\text{FOUND}}$	LOW for page has been found	
PBLF	page is being looked for	
HAM.ER.	Hamming error in corresponding byte	

The remaining 14 bytes in row 24 are unused and are free for use by the microcomputer, if required.

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alpha-numerics white or green control character, written automatically by EURO CCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Figure 8 shows the mode registers in the EURO CCT, R1 to R11; Register R11, for accessing external memory, can be written or read; all the others can only be written. Some of the following abbreviations are used:

(R1) Mode

T0, T1	interlace/non interlace 312/313 line control
TCS ON	text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	field-flyback or full-channel mode
$\overline{7+P}$/8 bit	7 bits with parity checking or 8-bit mode

(R2) Page request address

start column	column for acquisition data
ACQ CCT	which of 4 page requests
bank select	one of two banks of 4 page requests (one at a time)

(R4) Display chapter

determines which of 8 pages is displayed

(R5, R6) Display control for normal and newsflash/subtitle

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

(R7) Display mode

BOX ON 0	boxing function allowed on row 0 etc.
STATUS ROW	Row 25 displayed below or above
$\overline{\text{BTM}}$/TOP	main text
(R8 to R11)	Active chapter, row, column, and data information written to or read from page memory via the I^2C bus.

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C transmission byte.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
T_A	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{\text{ON}}$/OFF	GHOST ROW ENABLE	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T_1	T_0	R1 MODE
–	BANK SELECT A_2	ACQ. CCT A_1	ACQ. CCT A_0	T_B	START COLUMN SC_2	START COLUMN SC_1	START COLUMN SC_0	R2 PAGE REQUEST ADDRESS
–	–	–	PRD_4	PRD_3	PRD_2	PRD_1	PRD_0	R3 PAGE REQUEST DATA
–	–	–	–	–	A_2	A_1	A_0	R4 DISPLAY CHAPTER
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5 DISPLAY CONTROL (NORMAL)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6 DISPLAY CONTROL (NEWSFLASH/ SUBTITLE)
STATUS ROW $\overline{\text{BTM}}$/TOP	CURSOR ON	$\overline{\text{CONCEAL}}$/ REVEAL	$\overline{\text{TOP}}$/ BOTTOM	$\overline{\text{SINGLE}}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7 DISPLAY MODE
–	–	–	–	CLEAR MEMORY	A_2	A_1	A_0	R8 ACTIVE CHAPTER
–	–	–	R_4	R_3	R_2	R_1	R_0	R9 ACTIVE ROW
–	–	C_5	C_4	C_3	C_2	C_1	C_0	R10 ACTIVE COLUMN
D_7 (R/W)	D_6 (R/W)	D_5 (R/W)	D_4 (R/W)	D_3 (R/W)	D_2 (R/W)	D_1 (R/W)	D_0 (R/W)	R11 ACTIVE DATA

– bit does not exist.

T_A and T_B must be 0 for normal operation.
All registers are write only, except R11 (Read/Write). All bits in registers R1 to R10 are cleared to 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to 1.

All memory is cleared to 'space' (00100000) on power-up, except row 0 column 1 chapter 0, which is 'alpha white' (0000011) as the acquisition circuit is on.

Fig.8 EURO CCT register map

Register R3 (for page requests) is shown in detail in Fig.9. Abbreviations are as in Fig.7 except for DO CARE bits. When the DO CARE bit is set to 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to zero the digit is ignored. This allows, for example, "normal" or "timed page" selection.

If HOLD is set LOW, the page is held and not updated.

There are four groups of data shown in Fig.9, one for each acquisition circuit (four simultaneous page requests). Columns auto-increment on successive I^2C transmission bytes.

COLUMN	D_4	D_3	D_2	D_1	D_0
0	DO CARE MAG	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	DO CARE PAGE TENS	PT3	PT2	PT1	PT0
2	DO CARE PAGE UNITS	PU3	PU2	PU1	PU0
3	DO CARE HOURS TENS	X	X	HT1	HT0
4	DO CARE HOURS UNITS	HU3	HU2	HU1	HU0
5	DO CARE MINUTES TENS	X	MT2	MT1	MT0
6	DO CARE MINUTES UNITS	MU3	MU2	MU1	MU0

X bit not used

Fig.9 EURO CCT page requests register (R3) map

SYSTEM CONFIGURATIONS

Single-page CCT decoder

The single-page CCT decoder, shown in Fig.10, is designed to work with the TDA3560 PAL decoder circuit but is typical of the system configuration. (The components for the remote-control link are not shown).

The video input from the receiver demodulator is coupled to the CV (Composite Video) pin on VIP2. The data slicing function in VIP2 generates serial data TTD and data clock TTC which are passed to EURO CCT. The composite sync part of CV is output as VCS, and its line component is compared with SAND to provide the phase-locked 6 MHz system clock, F6. The $\overline{\text{TCS}}$ output from EURO CCT is passed through VIP2 to the STTV pin, which provides the sync signal to the tv receiver timebases. Positive or negative sync may be chosen depending on the connection of the load resistor. The $\overline{\text{TCS}}$ output of EURO CCT may be switched off under I^2C bus command; when this happens VIP2 automatically provides composite video output on the STTV pin for synchronizing a normal tv picture.

Interfacing of the EURO CCT to the page memory is straightforward. A single-page display requires 1K byte of memory so only ten address lines (A0 to A9) are required. Eight data lines (D0 to D7) and two control lines (output enable $\overline{\text{OE}}$, and write enable $\overline{\text{WE}}$) complete the interface.

The output red, green, and blue signals (R,G,B) from EURO CCT are buffered by emitter-followers, and the upper voltage levels are clamped by the diodes to a value which depends on the contrast control of the tv receiver. This allows text amplitude to follow picture contrast under a common control.

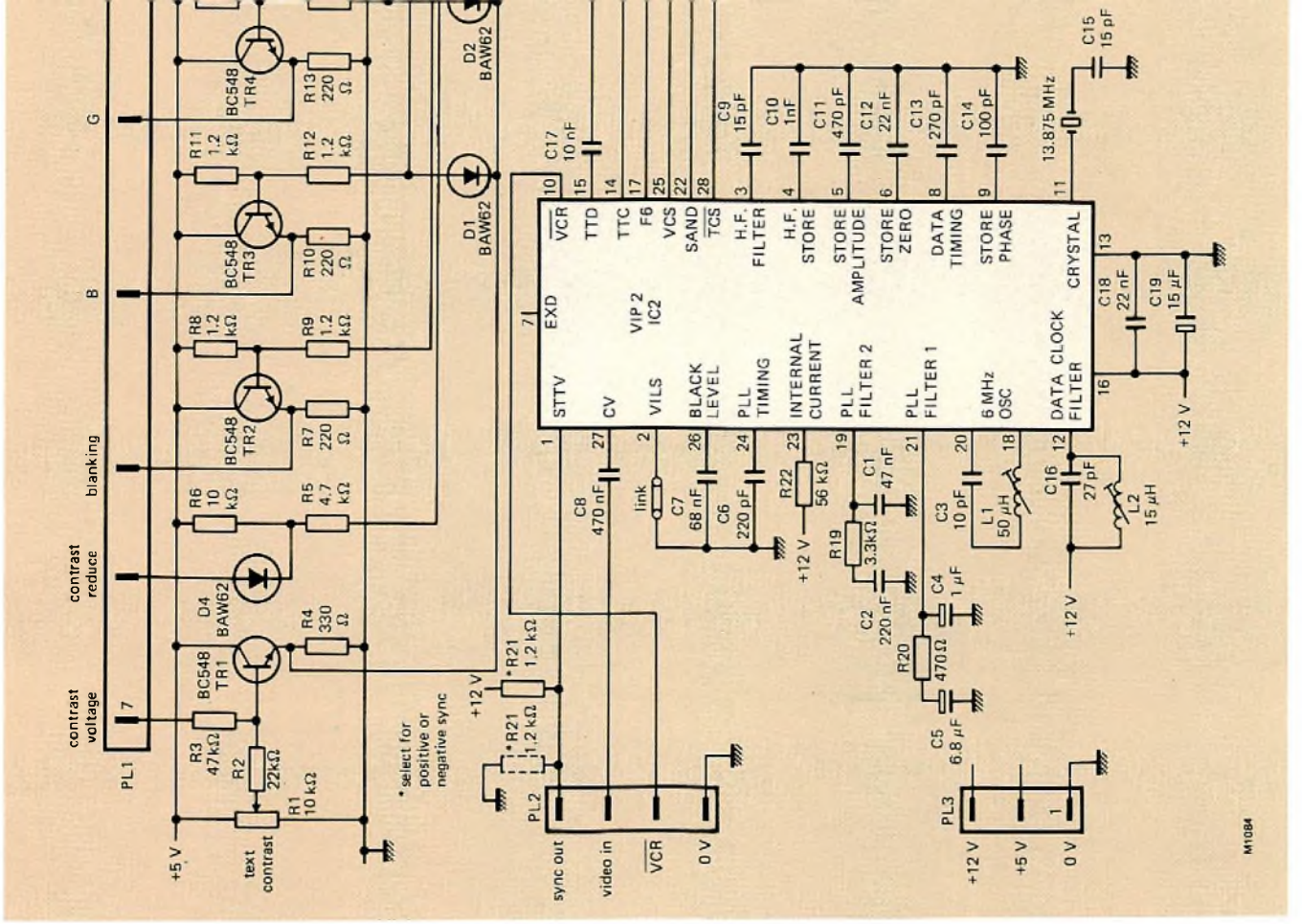
The blanking output (BLAN) is similarly buffered to give a switching signal for picture video. The BLAN pin of EURO CCT provides full screen, box, and dot blanking combined, so there is no need for the external OR-ing arrangements required in first-generation LSI decoders.

When the contrast-reduce function is activated, the $\overline{\text{COR}}$ pin goes LOW. A suitable potential divider and diode arrangement can reduce the contrast voltage in the receiver by a preset amount. This can be used for more readable mixed displays or subtitles in reduced-contrast boxes, for example.

Suitable decoupling capacitors complete the single-page EURO CCT decoder shown in Fig.10. The system may be realised on a single-sided printed circuit board, about 100mm square.

In the decoder shown in Fig.10, the control microcomputer and software will depend on the facilities required and the type of remote control to be used. As an example, consider a decoder required to work with the first-generation remote control (SAA5000/SAA5010 series), to give similar performance to the first-generation decoders. This could be provided by an MAB8420 microcomputer using the 2K bytes of ROM provided on-chip.

This example assumes that the software is written in a modular form for ease of understanding and flexibility of use. Some extra facilities can be provided within the available 2K bytes of software; for example status messages on arrival of a page, hold and update, don't care digit page requests, toggled height commands, etc. If the software modules are not required to be general, to be used for a particular model only as opposed to a range of decoders, software more dedicated to the application can be written. In this case it would probably be more economic in ROM utilisation, allowing more facilities to be provided with the same microcomputer.


contrast voltage
contrast reduce
blanking
PL1
R1 10 kΩ
R2 22kΩ
R3 47kΩ
BC548 TR1
D4 BAW62
R4 330 Ω
R5 4.7 kΩ
R6 10 kΩ
BC548 TR2
R7 220 Ω
R8 1.2 kΩ
BC548 TR3
R9 1.2 kΩ
R10 220 Ω
R11 1.2 kΩ
BC548 TR4
R12 1.2 kΩ
R13 220 Ω
D1 BAW62
D2 BAW62
+5 V
text contrast
* select for positive or negative sync
+12 V
*R21 1.2 kΩ
PL2
sync out
video in
VCR
0 V
71
STTV
EXD
CV
VILS
VIP 2 IC2
BLACK LEVEL
PLL TIMING
INTERNAL CURRENT
PLL FILTER 2
PLL FILTER 1
6 MHz OSC
DATA CLOCK FILTER
CRYSTAL
VCR
TTD
TTC
F6
VCS
SAND
TCS
H.F. FILTER
H.F. STORE
STORE AMPLITUDE
STORE ZERO
DATA TIMING
STORE PHASE
C1 47 nF
C2 220 nF
C3 10 pF
C4 1 µF
C5 6.8 µF
C6 220 pF
C7 68 nF
C8 470 nF
C9 15 pF
C10 1nF
C11 470 pF
C12 22 nF
C13 270 pF
C14 100 pF
C15 15 pF
C16 27 pF
C17 10 nF
C18 22 nF
C19 15 µF
R19 3.3kΩ
R20 470Ω
R21 1.2 kΩ
R22 56 kΩ
L1 50 µH
L2 15 µH
link
13.875 MHz
PL3
+12 V
+5 V
0 V
M1084

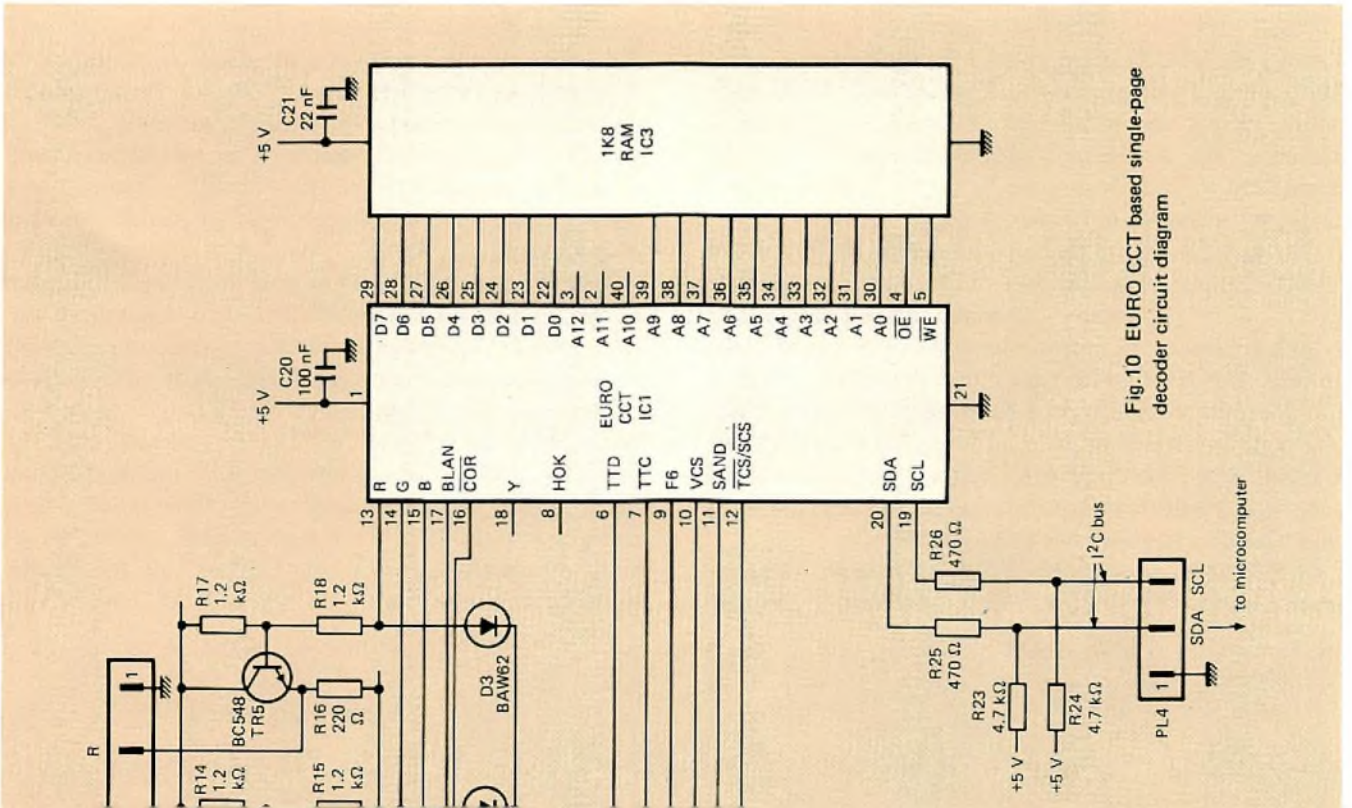


Fig.10 EURO CCT based single-page decoder circuit diagram

General control variation

Various EURO CCT based control configurations are possible; one of the simpler ones is shown in Fig.11(a). In addition to performing its normal CCT functions, the single microcomputer is used to decode user commands from the remote-control unit. It can also be used to control directly all display analogues and receiver tuning.

The examples shown are based on the MAB8400 series of microcomputers. Available in a range of program-memory sizes, they are particularly convenient to use in this kind of system because of the hardware serial bus interface provided on-chip. This greatly facilitates interfacing with the I^2C bus and the microcomputer can be programmed to act as a master or slave transmitter or receiver. The I^2C bus itself is a sophisticated interface which can support bi-directional data flow, multi-transmitter operation, and data acknowledge with data transfer rates up to 100 kHz.

In Fig.11(b), a modular structure is used, with one microcomputer to perform the remote-control decoding and tuning system drive functions and a second microcomputer dedicated to teletext decoder control. The system can be extended to provide, for example, viewdata, VCR, or cable decoding functions, simply by connecting extra hardware to the common I^2C bus (provided the existing system has sufficient resources, for example an adequate number of spare keys).

Generally, the I^2C bus allows great flexibility in the design of systems and is convenient where sub-systems are physically some distance apart. In addition, an increasing number of special-purpose devices are being made with I^2C bus interface on-chip. Examples are the PCD8571 128 x 8 bit static CMOS RAM, the PCB8573 clock/calendar chip, the SAB3035 (CITAC) tuning and analogue control chip, and the SAA1300 tuner switching circuit. Using these components it is possible to build sophisticated systems for all kinds of applications up to the limit of cost and the designer's imagination.

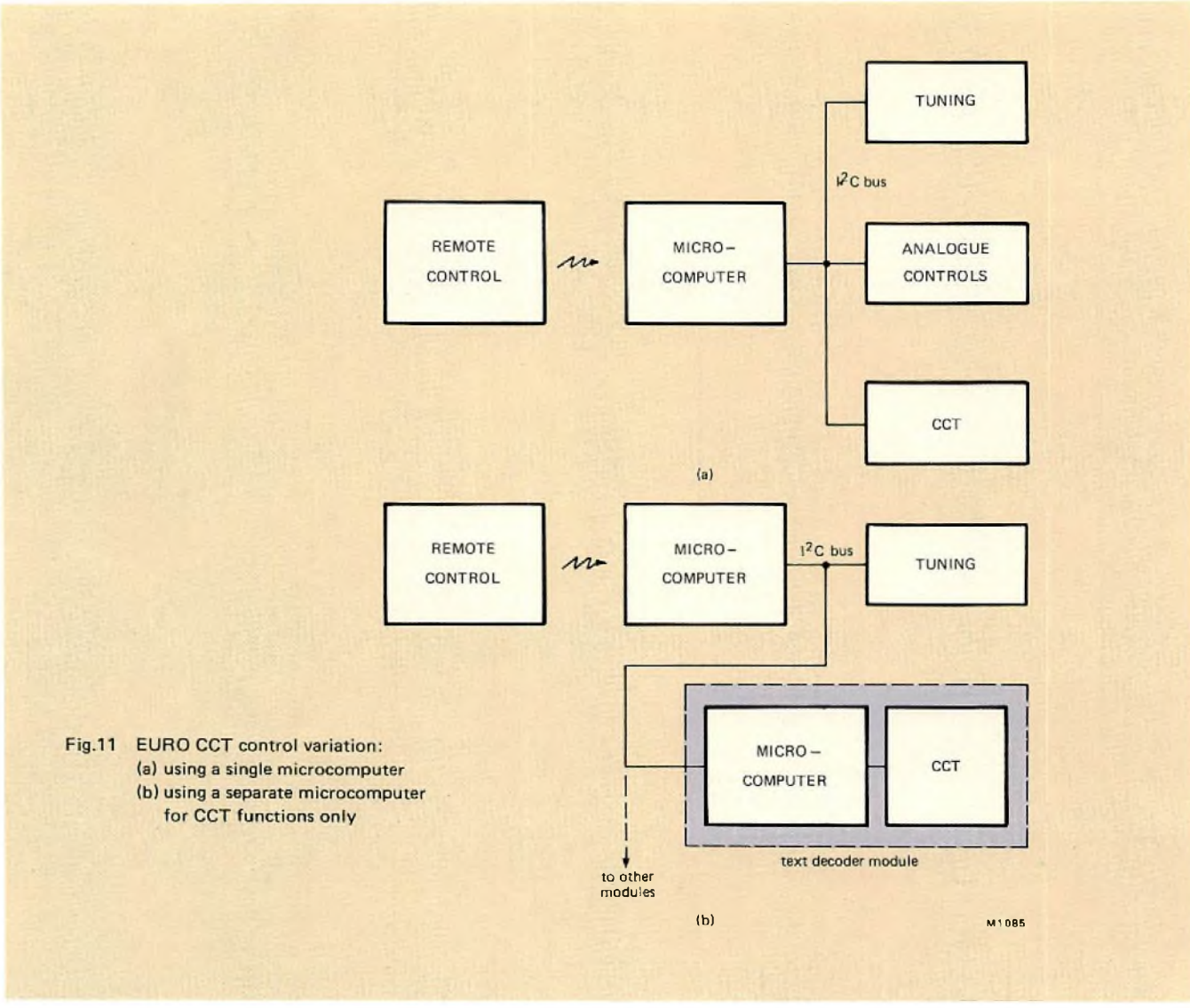


Fig.11 EURO CCT control variation:
(a) using a single microcomputer
(b) using a separate microcomputer for CCT functions only

Multipage decoders

Almost all teletext decoders that have been manufactured so far have been for single page use. The EURO CCT based decoder is capable of searching for and storing up to four pages simultaneously (including ghost rows). Extra software as well as more memory space (1K byte per page for normal use, 2K bytes per page in ghost-row mode) is required to deal with multipage requests. In fact, the circuit diagram is almost identical to that for single-page acquisition (Fig.10). The only addition required is that some or all of the three unused EURO CCT address lines (A10, A11 and A12) need to be connected to the enlarged memory. Up to 8K bytes of memory may be used.

By using a software command it is possible to switch the EURO CCT based decoder into ghost-row mode. This mode allows for greater "user-friendliness" especially with the linked pages facility. The linked pages are transmitted in row 27. There can be up to four row 27s, each containing six page numbers (including sub-code). Thus, each teletext page can have associated with it up to 24 other pages. There are two main ways in which these numbers can be used: indexing and chaining. With indexing, an index page contains the page numbers referred to in associated row 27s, allowing some form of short code dialling to select them (for example 4th page instead of page number 117). When chaining, each page has a ghost row indicating the next page, previous page, and index. This permits simple "step-forward" and "step-backward" buttons to be provided for the user with no need for three-digit page dialling. The order of page access is then predetermined by the broadcasters, but the pages are displayed when required by the user, giving a simple "browsing" facility. Of course, combinations and extensions of these methods can be used and with agreement on codes of practice by the broadcasting authorities they can give simple user controls.

Full-channel decoders

The EURO CCT has the ability to handle teletext on all tv lines, for use with cable transmissions. This full-channel decoder is achieved by software command, the hardware being the same as that required for normal field-flyback mode. However, page clearing has to be handled in a slightly different manner.

When a page is first received, the EURO CCT usually arranges for the old data in memory to be cleared. There is no problem in field-flyback mode as most of the field period is available for the clear function. However, in full-channel mode wanted data may be coming in at the same time, thus inhibiting the clearing function. There are two ways around this difficulty.

Firstly, the database can be arranged to transmit non-row-adaptively, so that blank rows are always transmitted. There is then no need to clear the page as new data will overwrite the old. Alernatively, the page can be cleared by a command from the control software when a new page is requested, so that new data is received into an already blank memory. If the database is very large, it is possible to arrange a second page of memory to display the old page until the new one has been received, thus avoiding a blank screen for the transmission cycle time.

Viewdata

The display standards of wired text systems are currently in transition to a higher level than Level 1 teletext, with more sophisticated graphics, pastel colours, etc. However, the Level 1 display available since the inception of the UK Prestel service is adequate for many applications at the lower cost end of the market and for these users the EURO CCT is an ideal display device.

For most viewdata systems the data rate is relatively low (for example 1200 baud) and this is easily transferred down the I^2C bus into the EURO CCT. In this way interfacing complexity is minimized. The EURO CCT also contains features which facilitate the handling of the information, for example page clear command, automatic address increment, and cursor display.

A viewdata-only decoder is shown in Fig.12. This consists of an MAB8440 microcomputer performing the decoding, connected to the SAA5070 (LUCY) IC and a line terminating unit (LTU) which interface with the telephone line. The PCD8571 remembers the required numbers for the autodialler and autoidentification.

It is possible to have both teletext and viewdata decoders in the same receiver. The modular receiver architecture of Fig.11(b) is very suitable for this application.

Telesoftware

The basic concept of telesoftware – transmitting computer programs via teletext – embraces a large variety of equipment and system configurations. If the application involves simple processing of alphanumeric data, for example financial calculations, then the EURO CCT display facilities and transfer of data via the I^2C bus would be adequate. This type of system could be built into a tv receiver as a more complex type of teletext decoder with an additional microcomputer and perhaps more memory. Telesoftware protocols use the linked-page facility to handle long programs and so the EURO CCT would be operated in ghost-row mode. If the remote-control keypad buttons were sufficient for the application, a telesoftware add-on unit could be constructed for use with the modular tv system of Fig.11(b).

For some applications a more sophisticated graphics display may be required. In these situations the EURO CCT would be used as the telesoftware acquisition system, with a suitable form of interface to transfer the data to, for example, a home computer. It is also possible to use EURO CCT in "8-bit" mode (that is with normal parity checking

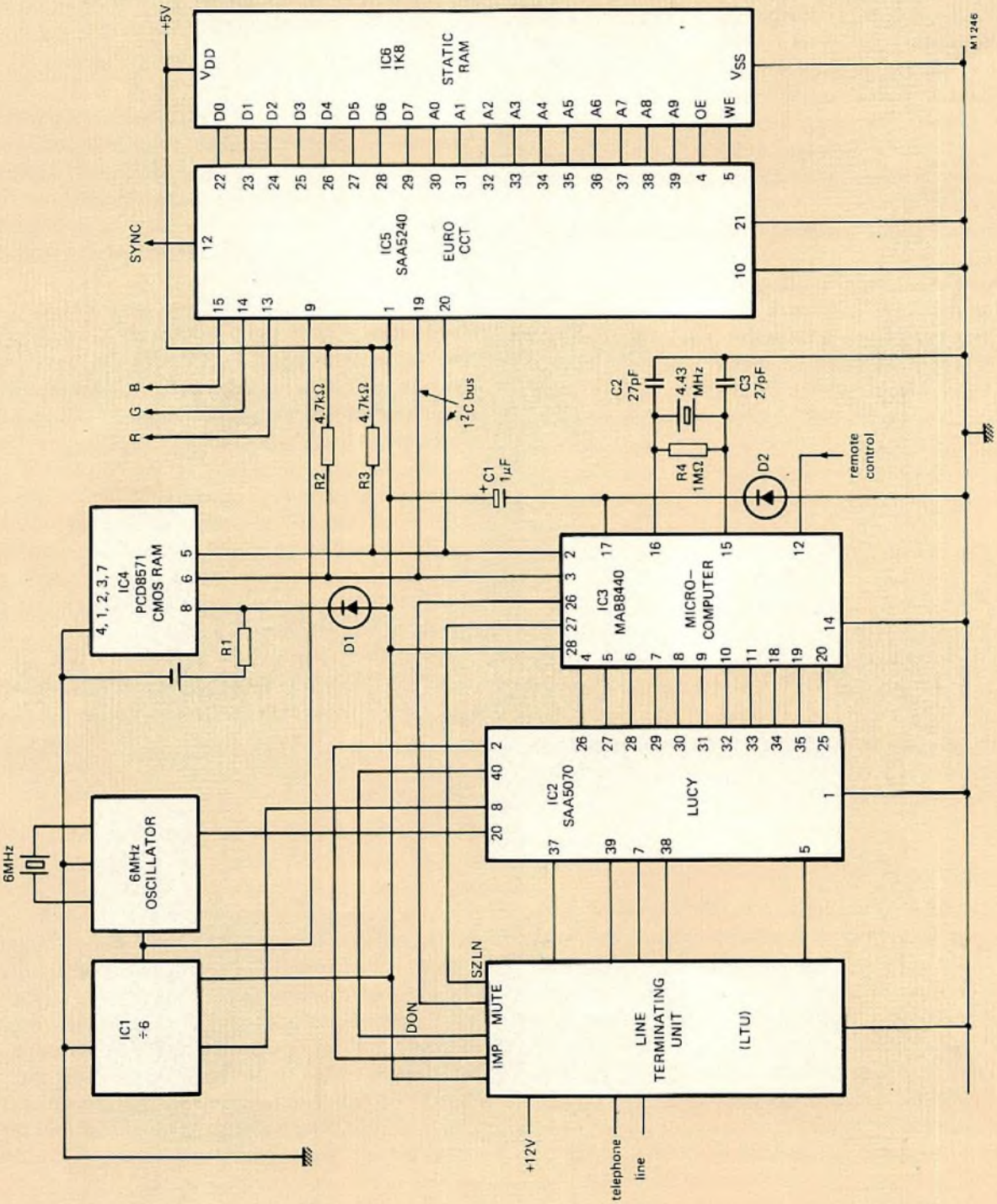


Fig.12 Viewdata decoder circuit diagram. (RGB and telephone line interconnection components not shown)

disabled), allowing sophisticated error-correctable or scrambled-data streams to be dealt with for special applications.

The telesoftware technique could also be applied to page selection methods in sophisticated teletext decoders. This would allow a pseudo-interactive viewdata-like control scheme, by making the displayed page number depend on YES/NO questions or selections. In view of the database size, this would be most applicable to full-channel data systems.

Other telesoftware applications may not need an alphanumeric display, for example a credit card verifier, with invalid card numbers transmitted by teletext. For these applications, the EURO CCT could still be a suitable acquisition-only device in view of its multipage and ghost-row capabilities.

It is also possible with the EURO CCT to request pages in hexadecimal, not just BCD digits. This is necessary for the acquisition of telesoftware and higher levels of teletext. Using the full hexadecimal range there are 4 194 304 combinations of page and sub-code numbers.

Other configurations

Although it is anticipated that the great majority of EURO CCT applications will have the device built into the same equipment as the display, it is also possible to use add-on units plugged into the standard tv aerial socket. Tuner, i.f., and demodulator stages are required for the dcoder input, together with a colour encoder and modulator for the output.

A printer for hard copies of the teletext pages may be included in a sophisticated receiver or connected separately as a decoder peripheral. There are two main ways of interfacing a printer. The first is to provide a real-time scanning dot stream from the Y output of the EURO CCT with a suitable interface buffer in the printer itself. Alternatively, character data can be read out of the display memory via the I^2C bus and transferred to the printer, which in this case must have its own character generation system.

The same technique of reading character data through the I^2C bus can also be applied to bulk storage of data, for example using a tape recorder. The I^2C bus data is processed (and compressed if necessary) by a microcomputer which drives a suitable modem function, for example part of LUCY SAA5070.

The configurations briefly mentioned here are examples of the very many arrangements made possible by this extremely versatile device.

REFERENCES

1. "Characteristics of Teletext Systems", C.C.I.R. XV Plenary Session, Geneva, Vol. 11, Report 957, 1982.
2. "I^2C Bus in Consumer Applications", Philips Technical Publication 110, Mullard Technical Publication M83-0196, 1983.

Fast co-processor meets factory's real-time needs

J. K. CHAY

Numerically controlled (NC) tools, robots and so on have become a familiar part of manufacturing. However in some environments a definite trend can be seen toward Integrated-Computer-Aided-Manufacturing (ICAM, see page 35).

With ICAM we step aside from the system whereby each operation in a factory leads an isolated life. The trend is toward an integrated approach. One in which each operation is informed (insofar as is necessary) of other operations taking place. Where CAD is tied direct to manufacturing, and manufacturing direct to quality control and inventory control – and almost as directly to profit and loss control. Central to such a system is task allocation and control.

Task allocation usually implies distributed intelligence whereby microcomputers or microcontrollers are chosen for their ability to perform specific tasks (process or robot control; inventory analysis; information access or display, etc.) plus an ability to communicate at specific levels.

Communication calls for bus structure specifications, for communication protocols, for communication compatibility. Here the right to say is no less important than the right to know. Hierarchies and priorities must be specified, distinction must be made between real-time and machine time. A real-time operation cannot wait until the profit and loss account has been balanced. Real-time has priority. Nevertheless the speed of current microcomputers is such that real-time operations need only be minor interruptions in their machine-time world.

Such is the burden of this article. The addition of a co-processor allows a fast microcontroller to carry out its machine-time functions while only occasionally being interrupted to perform a real-time operation.

Factory control

The need for distributed intelligence and real-time response in the automated factory demands a powerful input and output system. In robotics, for example, designers often depend on several processors to implement a multitude of separate I/O functions, such as motion and manipulation control, vision and speech recognition, and several levels of data communications. The job of coordinating such a multiprocessor system is a difficult one. Indeed, the data communication task alone is complex enough to send designers back to their books looking for solutions.

One way to reduce the complexity of real-time I/O design is to use a very fast bipolar controller directed by an interrupt-driven co-processor. The co-processor momentarily interrupts the controller's non-real-time task to let it perform a real-time operation before returning to its main task. In this way it interfaces the fast controller with an often very much slower real-time world.

The 8X310 interrupt control co-processor – together with its companion 8X305 8-bit bipolar controller – satisfies the need for manageable, responsive local control in the factory, particularly in robotics.

Interrupt drive

In operation, the controller executes its main program until called upon by the interrupt co-processor to service an I/O request (Fig.1). After it executes the interrupt service routine, which is stored in main memory, the controller can take advantage of delays in the I/O to continue executing the main program. Because its 16-bit instruction word needs just 200 ns for execution, the controller can quickly return to the main program, thereby maintaining the efficiency of the system's overall throughput (Fig.2). What's more, the co-processor gives the controller the ability to execute up to four levels of subroutines, thus adding to the combination's I/O agility.

An interrupt cycle begins at the end of any controller instruction during which a process forces one of the co-processor's three interrupt lines to a logic high. In response, the co-processor halts the controller via the Halt timer,

takes over the instruction bus, and "pushes" (stores) the next address that would normally be fetched (in the main program) into a 4-address-deep last-in, first-out (LIFO) stack, a structure that sets the co-processor apart from conventional interrupt-handling chips, which require external stacks (Fig.3).

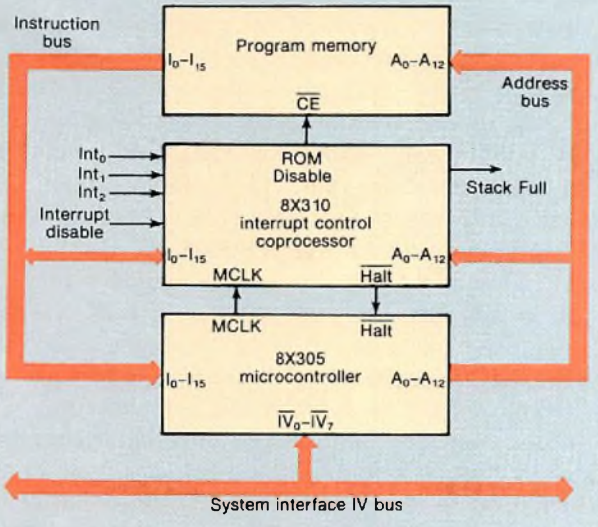


Fig.1 The 8X310 interrupt co-processor chip gives the 8X305 microcontroller the power to process three priority levels of interrupts and adds the ability to nest up to four levels of subroutines. The result is a powerful team of two fast chips for managing real-time input and output

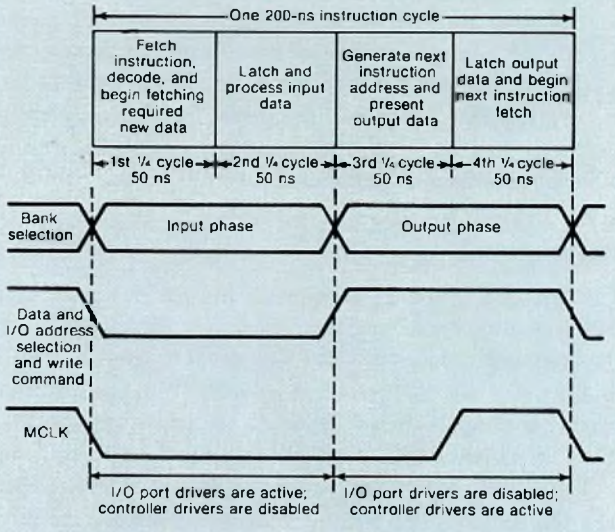


Fig.2 The microcontroller's 200 ns instruction cycle is divided into input and output phases. As a result, data can be read, modified, and sent out in a single cycle. What's more, eight basic instructions (Add, AND, XOR, Move, XMIT, NZT, XEC and JMP), whose variations form 95 possible commands, stress bit-manipulation and serve well for robotics

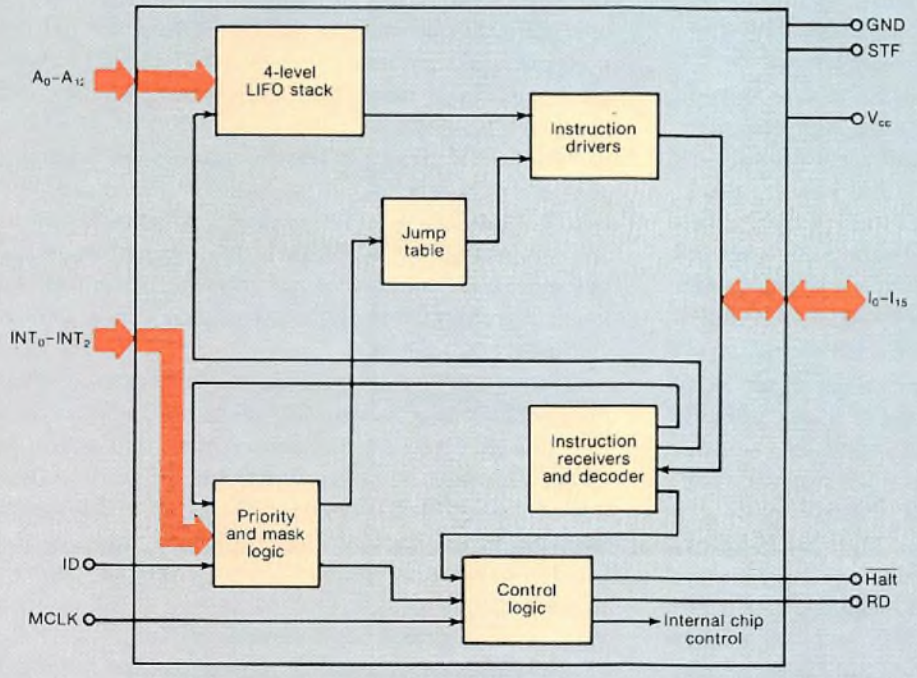


Fig.3 The interrupt co-processor's operation centres on its 4-address-deep last-in, first-out stack. When the chip gets an interrupt request on one of its three lines, the stack stores the controller's next address and forces the controller to jump to one of three memory locations, from which it begins to execute an interrupt service routine. The routine's last instruction, a Return, pops the stack and returns the controller to the stored address.

Next, the co-processor releases the Halt line and forces the controller to jump to one of three fixed locations – address 4, 5, or 6 – in main memory, depending on which of the three interrupt's (IN_0, INT_1, and INT_2) occurred.

Normally, each fixed address to which the controller jumps also contains a Jump instruction, one that directs the controller to an interrupt service routine written by the designer. The controller executes the routine, communicating to the outside world when necessary through its interface vector (IV) bus, one of three buses forming its Harvard (separate data and instruction buses and memory) rather than von Neumann architecture.

Return to main program

The last instruction of the service routine, a Return command, is intercepted by the co-processor, which again halts the controller and returns it to its pre-interrupted state by "popping" (taking) the stored address from its stack and placing a jump to that address on the controller's instruction bus, allowing it to continue executing the main program.

Each "Push" and "Pop" of the co-processor takes 200 ns, and the forced Jump instruction (in response to the interrupt) takes another 200 ns. Thus, within 400 ns of an interrupt the controller starts executing a service routine. On completion, another 400 ns gets the controller back to its main program.

The co-processor always responds to an interrupt, unless the interrupt mask is set, and provided that the interrupt's priority is higher than any in progress. The interrupt mask is set automatically (when an interrupt is started) or by the programmer executing a Set Mask command, one of the co-processor's five instructions for managing its interrupt and subroutine capabilities. (The other four instructions are Clear Mask, Return, Push and Clear Interrupt.)

As for the controller, it can perform a complete function – instruction fetching, data input, rotation, ALU operation, bit-string masking, and data output – within a single 200 ns instruction cycle. Besides its 8-bit IV bus, which is shared by the working (RAM) storage and a variety of I/O peripherals, the controller uses a 13-bit program address bus and a 16-bit instruction bus. The instruction and address busses connect directly to program memory (ROM or PROM).

For fast I/O transfer rates – up to 5 Mbytes/s – two control signals, Left Bank (LB) and Right Bank (RB), divide all I/O devices into two groups of 256 single-byte locations. In this way, the controller can pass data between any two devices on opposite banks in a single machine cycle. In a typical system design, one bank addresses up to 256 bytes of RAM and the other addresses up to 256 I/O devices.

What's more, using latched ports, memory buffers larger than 256 bytes can be interfaced with the controller. For example, two ports can latch the high and low address bytes of a 64-Kbyte memory, while a third port handles RAM control signals and a fourth transfers the data between the controller and the memory.

Robot control

Because robotics implies controlling devices such as stepper motors and servo-mechanisms and sensing the status of input detectors and switches – tasks that are intensely bit-oriented – the controller has extensive bit manipulation capabilities. These are implemented using a variable bit-shifter, a special multiplexer, and dedicated bit manipulation logic operating in the data path of an ALU.

Among the other strengths of the controller is its high-level language instructions for controlling the ALU (Add, AND, XOR), moving data (Move, XMIT), and jumping and conditional branching (XEC, NZT, JMP). In fact, the different variations of these eight instructions form a total of 95 real-time, industrial control operations.

As an example of the power of the controller's instructions, an Add instruction can select an external data field of from one to eight contiguous bits, add to it the accumulator's contents, and write the results back to the same or a different external location within one instruction cycle.

What's more, the controller's fast I/O can be made even faster by adding microcoded-program memory to extend the width of the instruction word. Thus each instruction would carry additional data bits to provide system control functions, status information, or whatever is needed to avoid a separate, time-consuming address-selection cycle. Extending the instruction word in this way speeds up, for example, critical timing loops that transfer data between several different ports.

Fast bit shifting

In addition, it is easy to program commonly used ALU operations, like subtraction, inclusive-ORing, and left rotation, although they are not included in the basic instruction set. For example, subtraction is performed within 1 μs using the two's complement method; an OR operation is performed in 800 ns with a few commands; and rotating the contents of a general-purpose register three places to the left, for instance, that of register R4, takes 200 ns with one instruction, MOVE R4(5), R4. Operations such as multiplication and division can also be performed, using longer algorithms, but still fast enough for most industrial controller applications.

To perform table look-ups or multiple conditional branches based on an operand's value, programmers can use the XEC (Execute) instruction in conjunction with a series of Move, XMIT, or JMP instructions. XEC causes a single instruction to be executed out of sequence without altering the controller's program counter. Such an operation is useful, for example, when an I/O port contains a value indicating the status of an external operation and a succeeding programming task depends on the value.

A plausible architecture for a multipurpose robot is one in which the hardware executes multiple real-time tasks and the software gives the robot flexibility to meet changing

roles in the factory. This architecture can be implemented with a host CPU supervising tasks and front-end microcontrollers interfacing with the specific task-oriented hardware. In this way, the microcontrollers off-load the host by performing bit manipulation and control-oriented tasks, leaving the host free to supervise the system.

Integrated drive saves controller time

Robots vary in their degrees of mechanical freedom. A robot's typical articulation can include base sweep, shoulder swivel, elbow extensions, and wrist pitch, roll, and yaw; each demanding a controller's attention. To minimize the time the host processor is idle, each of these axes is interrupt-driven, affording real-time responses using stepper motor controls.

In one installation each of two stepper motors has four driving coils (Fig.4). Energizing and de-energizing the coils causes the motor shaft to change position, the direction being determined by the sequence in which the coils are excited. Since the current through each coil is either on or off, the stepper motion is directly and precisely controlled by digital outputs from the microcontroller.

The controller issues a set of four parallel pulses to rotate the shaft one step. There is a delay as the motor starts, moves, and returns to rest ready for the next step. On average, this delay which depends on the characteristics of the motor, is about 1 to 1.5 ms – about 5000 machine cycles for the controller. Time enough for it to return to its main program or handle other interrupts. The controller, however, must be available to deliver the next set of pulses when the stepper is ready to respond. To let the controller know when to transmit the next set of pulses, a timer is attached to one of the interrupt lines on the co-processor.

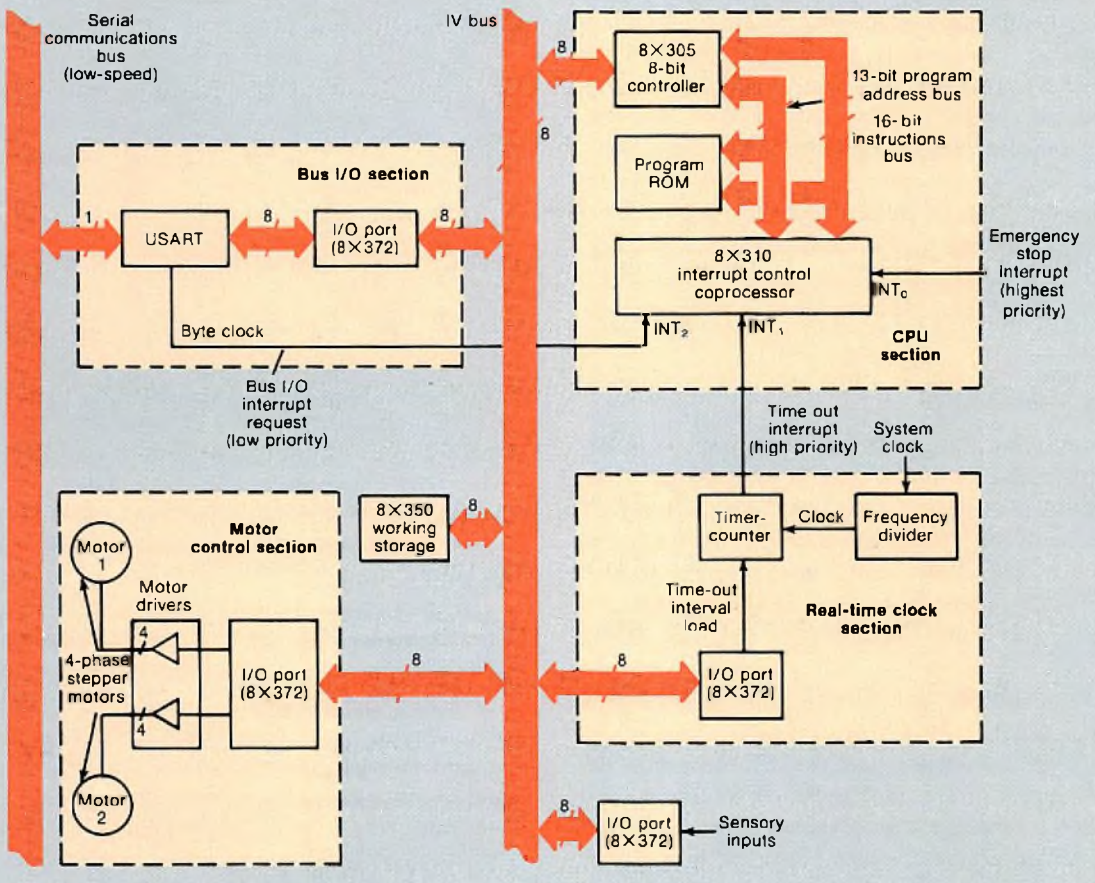


Fig.4. In a typical multifunction robot application the controller and interrupt processor manage a pair of stepper motors. Once the controller sends a step pulse to the motor, it is free to continue executing its main program until the motor actually moves far enough to take the next step. At that time, a real-time counter interrupts the controller to tell it that the motor needs its next pulse

One driver, two motors

To interface the controller with the stepper motor, addressable I/O ports control a set of driver circuits, which in turn produce the current required by the motor coils. Four bits are required to control the four coils of each stepper motor; thus an 8-bit I/O port can accommodate two stepper motors. By changing each 4-bit output pattern according to the proper bit manipulation sequence, the microcontroller has complete command over the rate of each motor's rotation and is able to track the exact number of steps each motor has travelled.

In controlling a stepper motor, the microcontroller must change its pattern at a rate that leaves time for the motor's shaft to overcome the system's mechanical inertia. If the controller sends out pulses too quickly, the motor could not physically keep up. Thus, for the best performance in a robot, the microcontroller should adjust its stepper motor pulses according to the acceleration curve characteristics of each of several motors. Here, the controller and interrupt co-processor use an acceleration-curve look-up table stored in memory, to optimally drive the stepper motor. In the event that a new robot with different mechanical characteristics is installed, the designer can easily reprogram the controller with a factory-floor data entry terminal.

Stepper-motor control is only one area where the controller and co-processor team up to simplify the job of automating a factory. Another place is in handling serial data transfers between factory elements. Two types of serial data communications are specified in an automated factory: device-to-device communication carried over a backplane and station-to-station communication via a local network.

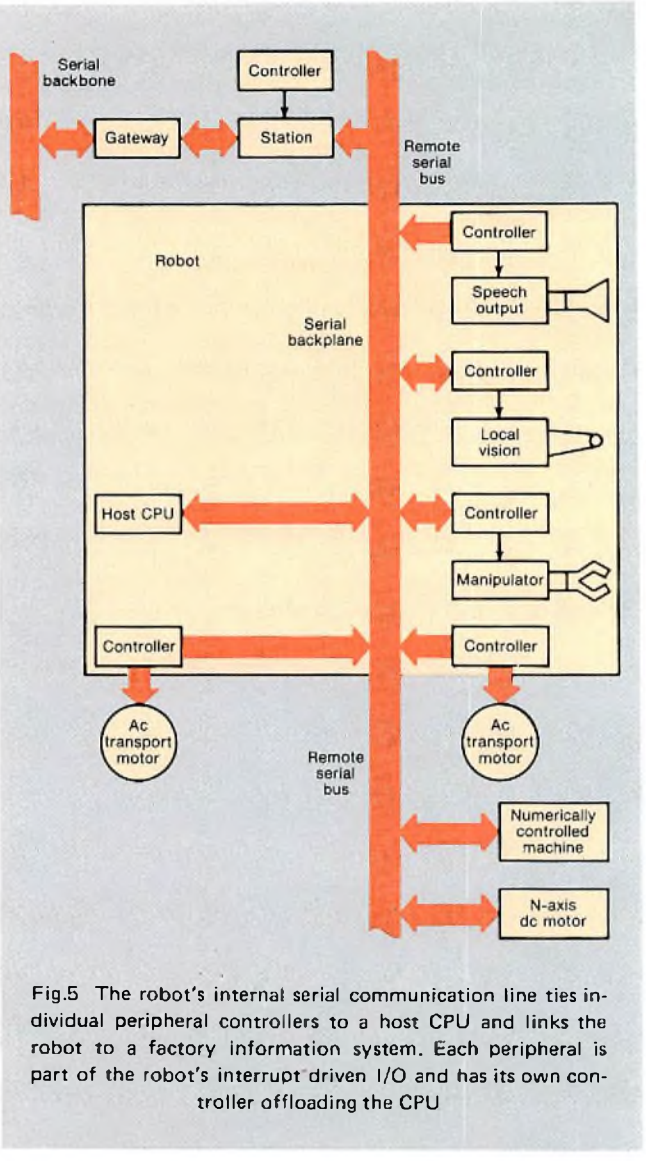


Fig.5 The robot's internal serial communication line ties individual peripheral controllers to a host CPU and links the robot to a factory information system. Each peripheral is part of the robot's interrupt driven I/O and has its own controller offloading the CPU

Communication control

A robot's internal data link along a serial backplane – easier to build and more economical than a parallel bus – can employ a bit-oriented protocol (such as the High-level Data Link Control) with error checking and correction to improve the reliability of the received data. In this case, a general-purpose USART (universal synchronous/asynchronous receiver-transmitter) links various I/O devices within a robot.

A typical example is a robotic I/O manipulation section consisting of multiple stepper motors under control of the robot's host central processing unit (Fig.5). When required, the CPU broadcasts an interrupt packet to all internal I/O devices along the serial backplane. Once the message is sent out, each device de-serializes and decodes its address, and if an I/O device address matches the one broadcast, that device generates an interrupt requesting a communication link. The co-processor senses the interrupt, allowing the controller to transfer its data byte through an I/O port. As part of the system, a 256-by-8-bit RAM buffers any short messages and maintains important system data. Once the serial data link is established, the controller executes its communication routines and serializes data in order to send a response packet back to the host CPU over the serial backplane.

When multiple robot stations require communication with each other through a factory's backbone network, a local network can increase the overall real-time system throughput by distributing intelligence among robot stations that do not require constant supervision by a master computer (Fig.6). The data rate of a local network that is based on a token-access scheme using the high-speed microcontroller ranges from 1 to 10 Mbits/s. However, since the controller transfers at rates of up to 5 Mbytes/s (on the IV bus), it requires data buffering to directly manage the bus's serial data stream.

The two modes of operation for which the controller manages the network interface are reception and transmission. The receiver's physical layer interface is accomplished by a modem control input for demodulating the incoming token carrier. Here, start-delimiter detection logic

ICAM: a factory model

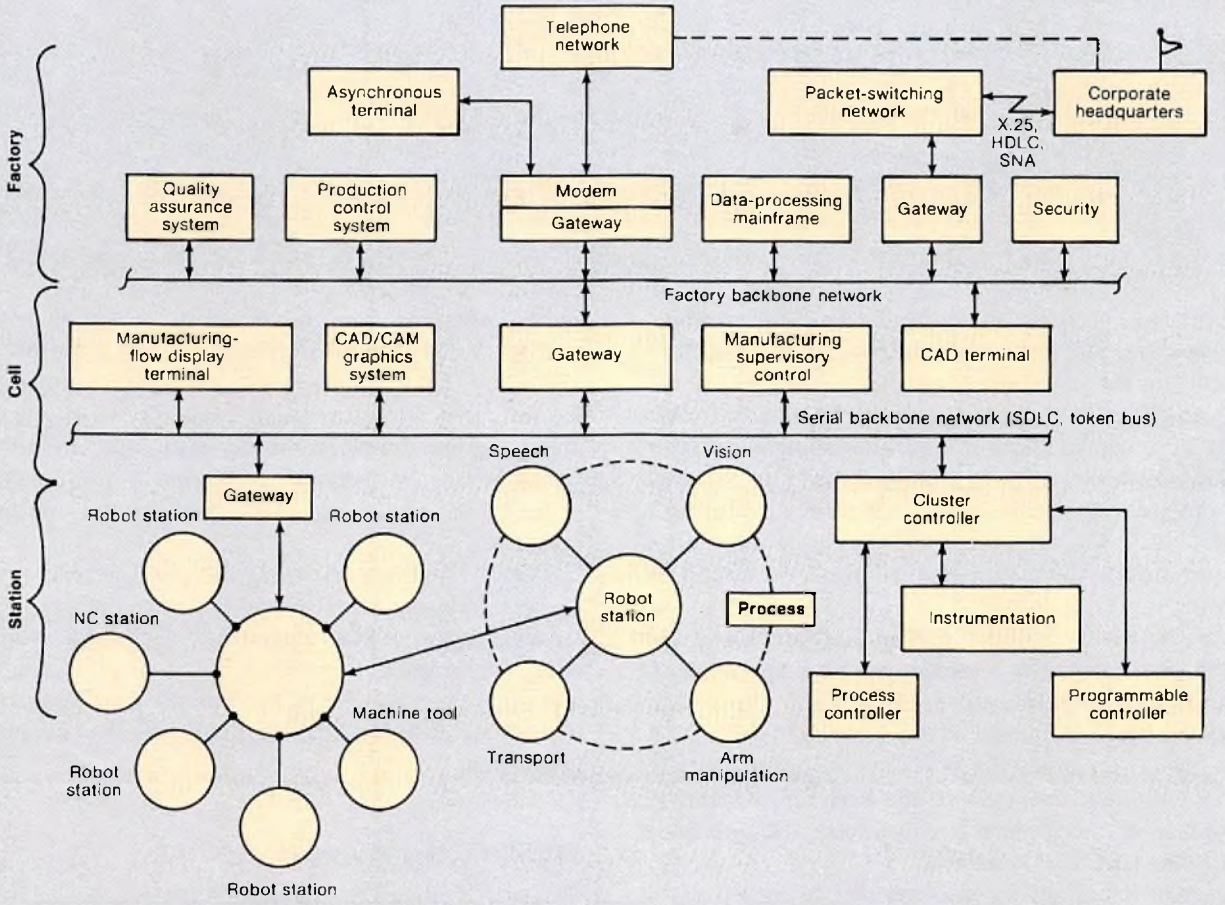
The integrated computer-aided manufacturing (ICAM) model is used by various industries to conceptualize the levels of activity in an automated factory. It incorporates data communications over local networks, process controllers, CAD/CAM graphics systems, numerical control machines, and robotic systems, and is made up of factory, cell, station, and process segments (see the figure).

The factory segment supplies information on the manufacturing process and its management, including data on sales, finance, production control, quality assurance, CAD, and factory security. It also provides communications at two levels; throughout a single factory location via a factory "backbone" network and among plants and other facilities over a global-area network such as existing X.25 packet-switching systems. As a result, the factory level can furnish a data base for an office automation system through a gateway controller.

The communications link among multiple stations is coordinated and controlled at the cell level, which typically consists of a serial backbone network (a bus using CSMA/CD or token passing). Indeed, it is through the cell level that station-level robots can tap into the factory backbone network.

Station-level equipment, in turn accesses the cell level through either a cluster network controller or a gateway. Thus, when a segment of multiple robots needs to communicate with another segment, that link is coordinated through the cell level. At station level there is interstation communication via some form of serial net (a token-passing ring or bus). At this level, a real-time local network is a very desirable approach to building a distributed intelligence system, since it guarantees that responses to communication and commands occur within a specified time.

Finally, the process level defines the internal operation of a robotic system. It covers the control and articulation of real-time devices and sensors, such as those needed for a robot's arm manipulation, vision, transport, and speech input recognition. A remote supervisory microcontroller may be responsible for particular task operations. Accordingly, the process level enables each device to communicate with all of the others, while being centrally supervised by a station-level host CPU. Communication is via a serial backplane according to CSMA/CD, SDLC, or an asynchronous protocol.



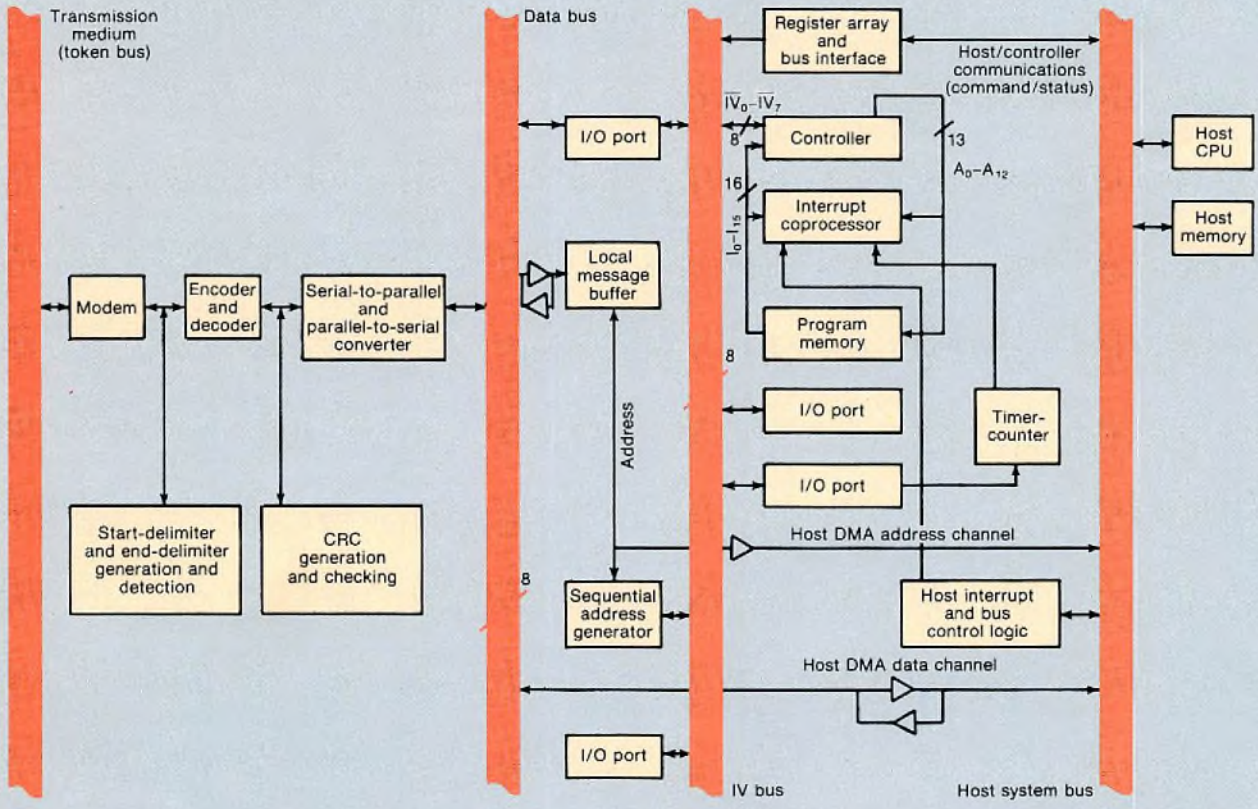


Fig.6 Reliable high-speed communication is achievable between sections in an automated factory with distributed intelligence. With the controller and interrupt chips at its heart, a token-based local network can transfer data at a maximum rate of 10 Mbits/s

interrupts the controller at the beginning of an incoming message packet. The destination address field is de-serialized and sent to the controller through an I/O port. If the address matches that of the receiving device, the controller, assisted by a combination of sequential address generator and DMA controller chip transfers the data into the local RAM and enables the CRC (cyclic redundancy check) error detection logic. On the other hand, if the device address does not match the destination address, the packet is discarded.

Once the packet is stored in the local buffer and any errors are corrected, the controller can interrupt the host, if needed, to transfer the data out of the RAM. The transfer is accomplished with the aid of the address generator DMA device, which generates the sequential addresses that are used to write the message into the host CPU's memory. The controller then interrupts the host, acknowledging that the data transfer is complete.

It is very important for the controller to keep track of real time, since in token-passing a station controls the medium for a given interval, passing the token to the next station when its time expires. Also, a station needs to measure a delay time before it can transfer the token to make sure that the next station is operating properly and has not been removed. Real-time delays are also required during system initialization. In each case, an interrupt function can be accomplished with a real-time clock operating in conjunction with the interrupt control co-processor.

Finally, the network controller also transmits message packets from the host by way of the local network in a sequence more or less the reverse of that for reception. After the transfer is completed the network controller interrupts the host CPU as an acknowledgment, waits until it receives the token, and then transmits the packet to its destination.

Publisher's acknowledgement

This article originally appeared in the January 12 issue of Electronic Design, copyright 1984, Hayden Publishing Co.; permission to reprint is gratefully acknowledged.

New techniques for accurately tuning a.m. and f.m. radios

J. W. BEUNDERS and A. GARSKAMP

In microcomputer-controlled radios, the correct tuning points for f.m. stations, or the stopping points for search tuning, are usually established by a window detector which locates the zero crossing of the S-curve output from the frequency discriminator. The main disadvantages of this tuning system are its need for alignment and its sensitivity to d.c. shifts caused by temperature variations. Furthermore, even when the radio is accurately tuned to a strong f.m. station, there will be audible distortion if the signal is received from more than one direction on the same frequency (multipath reception) due to reflections. This is most likely to occur during car radio reception in mountainous regions. Most conventional search tuning systems are unable to reject stations with multipath distortion.

To solve these problems, we have developed the TEA6000 which is an f.m. i.f. system and microcomputer-based tuning interface. This 18-pin DIL IC performs the functions of a conventional f.m. i.f. amplifier for driving a ratio detector (e.g. our integrated f.m. i.f. system TEA5560), and also generates digital data representing the correct tuning point, the field-strength of the received signal, and the level of any multipath distortion. The TEA6000 uses a unique approach to establish the correct tuning point. This is done with a digital frequency counter which can measure the i.f. with an accuracy of ±3,2 kHz or ±6,4 kHz in the range 10 MHz to 11 MHz for f.m., the accuracy being dependent on the required measuring speed. There is also a separate input for an a.m. radio i.f. signal which can be measured with an accuracy of ±125 Hz or ±250 Hz within the range 428 kHz to 492 kHz. This facility makes it possible to construct an a.m./f.m. radio by simply adding an integrated a.m. receiver such as our TEA5550. Fig.1 is a block diagram of a typical a.m./f.m. stereo car radio using the TEA6000.

The TEA6000 also detects the level (field strength) of the selected i.f. signal and incorporates an operational amplifier which can be used as an active filter to separate any a.m. (multipath distortion) from the output of the level detector during f.m. reception. The field-strength and multipath level signals thus derived are multiplexed, A to D converted, and passed, together with the measured i.f., to the radio's microcomputer via the simple 2-wire bidirectional I^2C bus. The power supply lines for the analogue and digital signal processing sections of the TEA6000 are completely isolated to prevent crosstalk between the two sections.

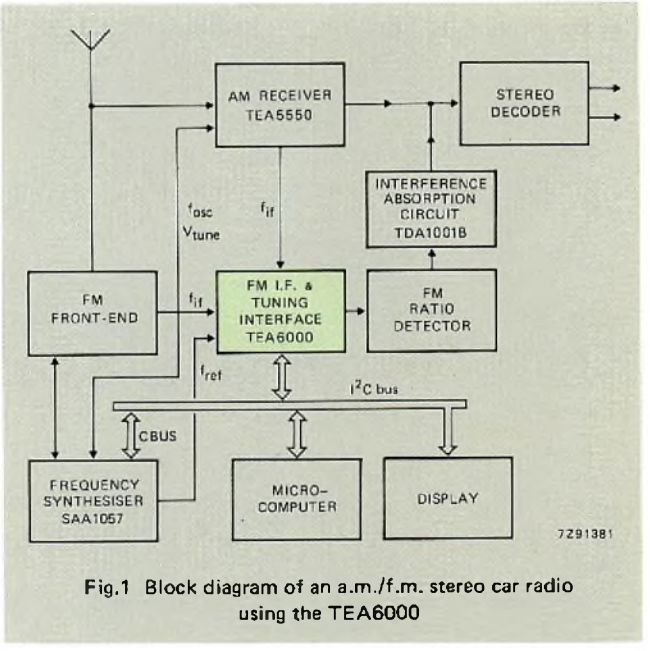


Fig.1 Block diagram of an a.m./f.m. stereo car radio using the TEA6000

ANALOGUE SIGNAL PROCESSING

The following descriptions are based on Fig.2 which is a block diagram of the TEA6000 with its peripheral components.

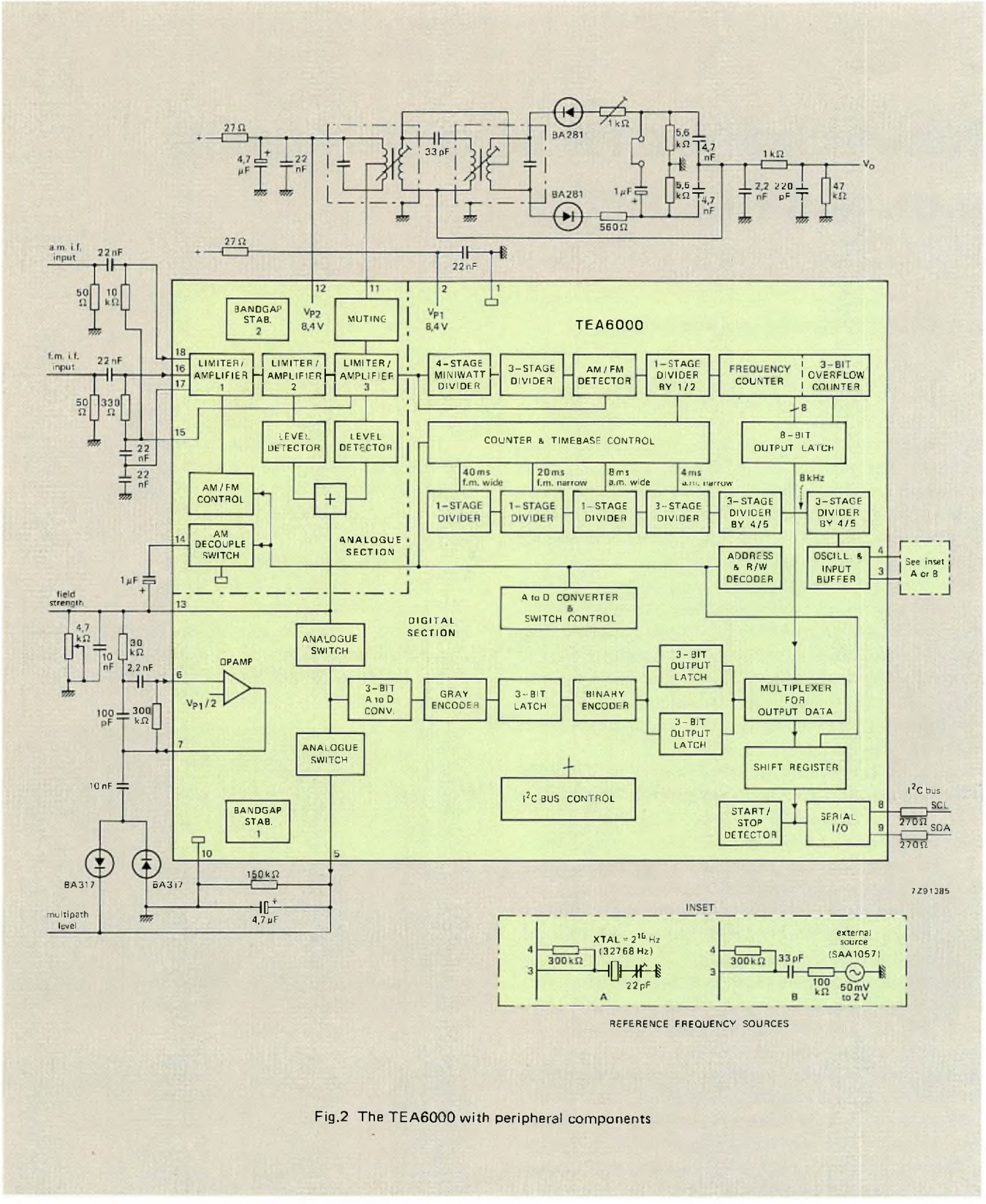


Fig.2 The TEA6000 with peripheral components

I.F. amplifiers and muting

The i.f. section of the TEA6000 incorporates three direct-coupled wideband differential i.f. limiting amplifiers which have separate software-selected inputs for a.m. and f.m. signals, and require very few external components. The input sensitivity for 3 dB below limiting at the f.m. input is 150 μV. The final i.f. amplification stage has two outputs. One is internally applied to a frequency counter. The other is applied, via a muting stage, to pin 11 from where it can be applied to the input of an external f.m. ratio detector. The muting stage reduces interstation noise during tuning by about 15 dB and the ratio detector is damped during a.m. reception to prevent spurious noise output.

Level detectors

The final two i.f. amplification stages also drive a two-stage level detector with a high-level field-strength dependent direct-current output at pin 13. This current output can be converted into the desired voltage level by an external resistor and used to derive an a.g.c. signal. It can also be used for smooth field-strength dependent control of stereo/mono switching (stereo channel separation), and for control of the high-frequency audio response at the stereo decoder. To increase the versatility of the TEA6000, the level detector output at pin 13 can be switched off under software control; pin 13 can then be used as an input. A low value external smoothing capacitor between pin 13 and the common return will ensure fast response of the field-strength signal during f.m. reception and will not smooth out any a.m. due to multipath reception. During a.m. reception however, more smoothing is required to ensure that the field strength signal is not influenced by the amplitude modulation. Since pin 14 is connected to the common return in the a.m. mode, this additional smoothing can be obtained by connecting a higher value capacitor between pin 13 and pin 14.

During f.m. reception, with the level detector switched on, the output at pin 13 will be amplitude modulated if multipath distortion is present. This a.m. can be separated from the i.f. carrier by an active filter constructed around the internal operational amplifier between pins 6 and 7. After external rectification and smoothing, the multipath level signal can be reinserted at pin 5. Software control also allows the internal reset signal of the frequency counter to be routed to pin 5 for testing purposes. This facility can, however, also be used to ensure that the external smoothing capacitor for the multipath distortion signal is rapidly discharged when changing from one station to another.

The field-strength and multipath-distortion level signals at pins 13 and 5 are multiplexed by two internal analogue switches and applied to an A to D converter.

The A to D converter receives the multipath signals from the analogue switches and converts them into a 3-bit binary code representing one of eight quantization levels referenced to the output from a bandgap stabilizer. The converter can be software-programmed to have low or high sensitivity to the field-strength and multipath distortion signals at pins 13 and 5. In the low sensitivity mode, the eight quantization levels cover the range 0 V to 6 V. In the high sensitivity mode, they cover the range 0 V to 3 V. To ensure glitch-free data from the A to D converter, its 3-bit binary output is first converted into a Gray code (in which only one bit changes for each level increment), latched, and then reconverted into binary form and latched before being transmitted on the I^2C bus.

DIGITAL SIGNAL PROCESSING

Frequency counter

The frequency counter is an 11-bit ripple counter with reset and preset. The 3 MSBs of the counter have an overflow function and can be switched off under software control for test purposes. The remaining eight bits represent an intermediate frequency in the range 10 MHz to 11 MHz for f.m., or in the range 428 kHz to 492 kHz for a.m. To increase the flexibility of the system, the counter is preceded by a single stage divider which can be switched on or off under software control. This allows a trade-off to be made between the speed of counting and its accuracy by effectively changing the length of the counter. With the divider off, the counting accuracy is ±1 bit (±6,4 kHz for f.m. or ±250 Hz for a.m.) and a short window is selected in the measuring window control circuit. With the divider on, the counting accuracy is ±½ bit (3,2 kHz for f.m. or 125 Hz for a.m.) and a long window is selected.

Measuring window control

The measuring window for the TEA6000 frequency measuring system is derived from a 40 kHz or 32 kHz reference signal which passes through a chain of frequency dividers. The first three-stage divider is software-programmed to divide by four for a reference frequency of 32 kHz or to divide by five for a reference frequency of 40 kHz, thereby obtaining a frequency of 8 kHz. The second three-stage divider is software-programmed to divide by four for a.m., or to divide by five for f.m. Following a third three-stage divider are three single-stage dividers which are software-controlled to set the measuring windows to 20 ms (1/50 Hz) or 40 ms (1/25 Hz) for f.m., and 4 ms (1/250 Hz) or 8 ms (1/125 Hz) for a.m. The duration of the long window for f.m. (40 ms) is not less than one complete period of the lowest f.m. audio frequency (25 Hz) so that symmetrical frequency shifts due to modulation do not disturb the counter.

A microcomputer-controlled radio is usually tuned by a frequency synthesizer. If our SAA1057 is used for this purpose, a 32 kHz or 40 kHz reference frequency to synchronize the internal oscillator of the TEA6000 can be made available under software control from pin 18 of

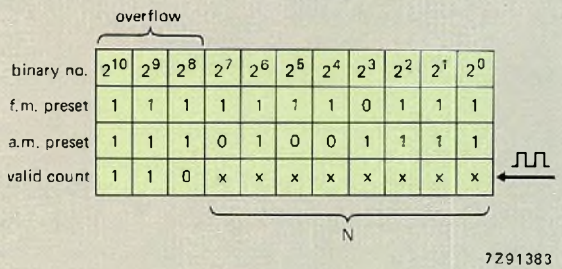
HOW THE FREQUENCY COUNTER WORKS

At the start of a counting period, the 11-bit counter is preset to binary 1871 for a.m., or binary 2039 for f.m. The number of pulses required to fill the counter, and then set it to zero, is $2^{11} - 1871 = 177$ for a.m., and $2^{11} - 2039 = 9$ for f.m. The counting continues, and the 8 LSBs become valid after the overflow contents has reached $110 = 2^{10} + 2^9 = 1536$. The counting is stopped at the end of the counting period. The total pulse count is then:

counts to zero + overflow contents + contents of 8 LBSs (N)

For a.m. this is: $177 + 1536 + N = 1713 + N$

and for f.m. $9 + 1536 + N = 1545 + N$



7Z91383

The relationship between the measured frequency and the pulse count (N) is:

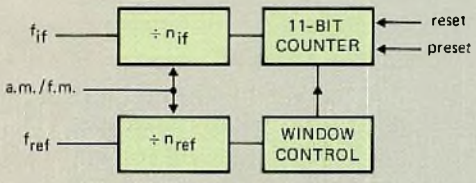
for a.m. (frequencies in kHz)

$f_{if} = (n_{if} f_{ref}/n_{ref})(1713 + N) = 428{,}25 + 0{,}25N$

for f.m. (frequencies in kHz)

$f_{if} = (n_{if} f_{ref}/n_{ref})(1545 + N) = 9888 + 6{,}4\,N$

These values are calculated for $f_{ref} = 32$ or 40 kHz and for $f_{ref} = 32{,}768$ kHz in the tables at the end of this article.



7Z91382

	f_{ref}	n_{ref}	n_{if}	$(n_{if} f_{ref})/n_{ref}$*
a.m. (wide window)	32 kHz	256	2	0,25
a.m. (narrow window)	32 kHz	128	1	0,25
a.m. (wide window)	40 kHz	320	2	0,25
a.m. (narrow window)	40 kHz	160	1	0,25
f.m. (wide window)	32 kHz	1280	256	6,4
f.m. (narrow window)	32 kHz	640	128	6,4
f.m. (wide window)	40 kHz	1600	256	6,4
f.m. (narrow window)	40 kHz	800	128	6,4

* f_{ref} in kHz.

the SAA1057. Alternatively, if this source of reference frequency is not available, the internal oscillator of the TEA6000 can be synchronized by an inexpensive 32,768 kHz watch crystal. In this case however, the previously mentioned measuring accuracies will be reduced by about 2,4%. The external components connected between pins 1, 3 and 4 of the TEA6000 must be selected so that the free-running frequency of the internal oscillator (astable multivibrator) is close to the reference frequency to which it is synchronized.

A special feature of the frequency measuring system of the TEA6000 is that the measuring cycle is synchronized with the transmission from the I^2C bus so that it is reset immediately after a valid instruction (READ or WRITE) has been terminated. This means that data can be read out on the I^2C bus after one measuring cycle.

DATA FORMATS

The general specification for the I^2C bus is in our Data Handbook IC2. The data formats for the I^2C bus transceiver in the TEA6000 are as shown in Fig.3.

Write mode

The TEA6000 is initialized and the frequency counter reset when it receives its address (1100001) followed by a write bit (0) and an 8-bit data byte. The functions of each of the data bits are:

bit 1 matches the reference frequency divider chain to the frequency at pins 3 and 4
1 = 40 kHz
0 = 32 kHz

bits 2 and 3 determine the sensitivity of the A to D converter to the analogue inputs at pins 5 (bit 2) and 13 (bit 3)
1 = high sensitivity (3 V full-scale)
0 = low sensitivity (6 V full-scale)

bit 4 switches the level detector output
1 = on
0 = off

bit 5 sets the divider chains and selects the correct input for f.m. or a.m. operation
1 = f.m.
0 = a.m.

bit 6 switches the 3-bit overflow function of the frequency counter on for normal operation, or off for test purposes
1 = on
0 = off

bit 7 sets the duration of the measuring window
1 = wide window (40 ms for f.m., 8 ms for a.m.)
0 = narrow window (20 ms for f.m. 4 ms for a.m.)

bit 8 routes the reset signal of the frequency counter to pin 5 or specifies pin 5 as an analogue level input
1 = reset signal output at pin 5
0 = pin 5 is an analogue level input

Read mode

The results of the measurements of intermediate frequency, field-strength and multipath distortion level are transmitted to the microcomputer when the TEA6000 receives its address code followed by a read bit (1). The information is transmitted as two 8-bit words. The first byte contains the field strength and multipath distortion level data. The second byte contains the measured intermediate frequency code. The transmission can be aborted after the first byte by omitting the acknowledge bit that normally follows it. The relationship between the measured frequency code (in hexadecimal) and the actual intermediate frequency is given in Tables 1 and 2.

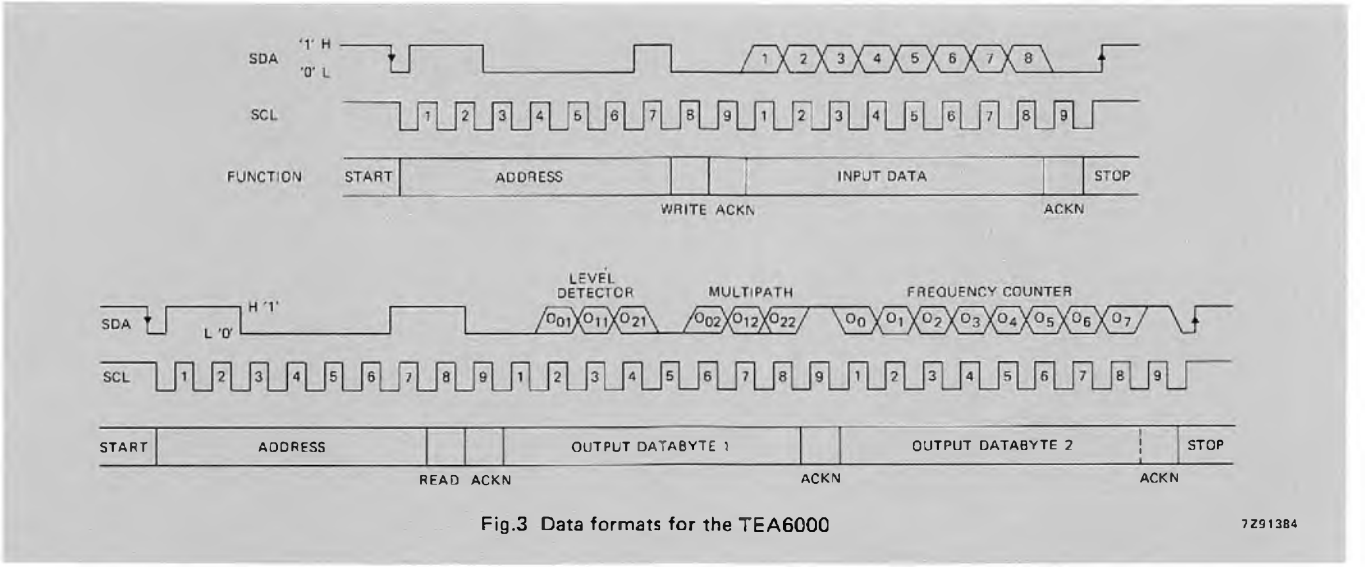


Fig.3 Data formats for the TEA6000

7Z91384

Table 1 Conversion table for 32/40 kHz reference input

AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)
428.25	'00'	9.888	441	'33'	10.214	453.75	'66'	10.541	466.5	'99'	10.867	479.25	'CC'	11.194
428.5	'01'	9.894	441.25	'34'	10.221	454	'67'	10.547	466.75	'9A'	10.874	479.5	'CD'	11.2
428.75	'02'	9.901	441.5	'35'	10.227	454.25	'68'	10.554	467	'9B'	10.88	479.75	'CE'	11.206
429	'03'	9.907	441.75	'36'	10.234	454.5	'69'	10.56	467.25	'9C'	10.886	480	'CF'	11.213
429.25	'04'	9.914	442	'37'	10.24	454.75	'6A'	10.566	467.5	'9D'	10.893	480.25	'D0'	11.219
429.5	'05'	9.92	442.25	'38'	10.246	455	'6B'	10.573	467.75	'9E'	10.899	480.5	'D1'	11.226
429.75	'06'	9.926	442.5	'39'	10.253	455.25	'6C'	10.579	468	'9F'	10.906	480.75	'D2'	11.232
430	'07'	9.933	442.75	'3A'	10.259	455.5	'6D'	10.586	468.25	'A0'	10.912	481	'D3'	11.238
430.25	'08'	9.939	443	'3B'	10.266	455.75	'6E'	10.592	468.5	'A1'	10.918	481.25	'D4'	11.245
430.5	'09'	9.946	443.25	'3C'	10.272	456	'6F'	10.598	468.75	'A2'	10.925	481.5	'D5'	11.251
430.75	'0A'	9.952	443.5	'3D'	10.278	456.25	'70'	10.605	469	'A3'	10.931	481.75	'D6'	11.258
431	'0B'	9.958	443.75	'3E'	10.285	456.5	'71'	10.611	469.25	'A4'	10.938	482	'D7'	11.264
431.25	'0C'	9.965	444	'3F'	10.291	456.75	'72'	10.618	469.5	'A5'	10.944	482.25	'D8'	11.27
431.5	'0D'	9.971	444.25	'40'	10.298	457	'73'	10.624	469.75	'A6'	10.95	482.5	'D9'	11.277
431.75	'0E'	9.978	444.5	'41'	10.304	457.25	'74'	10.63	470	'A7'	10.957	482.75	'DA'	11.283
432	'0F'	9.984	444.75	'42'	10.31	457.5	'75'	10.637	470.25	'A8'	10.963	483	'DB'	11.29
432.25	'10'	9.99	445	'43'	10.317	457.75	'76'	10.643	470.5	'A9'	10.97	483.25	'DC'	11.296
432.5	'11'	9.997	445.25	'44'	10.323	458	'77'	10.65	470.75	'AA'	10.976	483.5	'DD'	11.302
432.75	'12'	10.003	445.5	'45'	10.33	458.25	'78'	10.656	471	'AB'	10.982	483.75	'DE'	11.309
433	'13'	10.01	445.75	'46'	10.336	458.5	'79'	10.662	471.25	'AC'	10.989	484	'DF'	11.315
433.25	'14'	10.016	446	'47'	10.342	458.75	'7A'	10.669	471.5	'AD'	10.995	484.25	'E0'	11.322
433.5	'15'	10.022	446.25	'48'	10.349	459	'7B'	10.675	471.75	'AE'	11.002	484.5	'E1'	11.328
433.75	'16'	10.029	446.5	'49'	10.355	459.25	'7C'	10.682	472	'AF'	11.008	484.75	'E2'	11.334
434	'17'	10.035	446.75	'4A'	10.362	459.5	'7D'	10.688	472.25	'B0'	11.014	485	'E3'	11.341
434.25	'18'	10.042	447	'4B'	10.368	459.75	'7E'	10.694	472.5	'B1'	11.021	485.25	'E4'	11.347
434.5	'19'	10.048	447.25	'4C'	10.374	460	'7F'	10.701	472.75	'B2'	11.027	485.5	'E5'	11.354
434.75	'1A'	10.054	447.5	'4D'	10.381	460.25	'80'	10.707	473	'B3'	11.034	485.75	'E6'	11.36
435	'1B'	10.061	447.75	'4E'	10.387	460.5	'81'	10.714	473.25	'B4'	11.04	486	'E7'	11.366
435.25	'1C'	10.067	448	'4F'	10.394	460.75	'82'	10.72	473.5	'B5'	11.046	486.25	'E8'	11.373
435.5	'1D'	10.074	448.25	'50'	10.4	461	'83'	10.726	473.75	'B6'	11.053	486.5	'E9'	11.379
435.75	'1E'	10.08	448.5	'51'	10.406	461.25	'84'	10.733	474	'B7'	11.059	486.75	'EA'	11.386
436	'1F'	10.086	448.75	'52'	10.413	461.5	'85'	10.739	474.25	'B8'	11.066	487	'EB'	11.392
436.25	'20'	10.093	449	'53'	10.419	461.75	'86'	10.746	474.5	'B9'	11.072	487.25	'EC'	11.398
436.5	'21'	10.099	449.25	'54'	10.426	462	'87'	10.752	474.75	'BA'	11.078	487.5	'ED'	11.405
436.75	'22'	10.106	449.5	'55'	10.432	462.25	'88'	10.758	475	'BB'	11.085	487.75	'EE'	11.411
437	'23'	10.112	449.75	'56'	10.438	462.5	'89'	10.765	475.25	'BC'	11.091	488	'EF'	11.418
437.25	'24'	10.118	450	'57'	10.445	462.75	'8A'	10.771	475.5	'BD'	11.098	488.25	'F0'	11.424
437.5	'25'	10.125	450.25	'58'	10.451	463	'8B'	10.778	475.75	'BE'	11.104	488.5	'F1'	11.43
437.75	'26'	10.131	450.5	'59'	10.458	463.25	'8C'	10.784	476	'BF'	11.11	488.75	'F2'	11.437
438	'27'	10.138	450.75	'5A'	10.464	463.5	'8D'	10.79	476.25	'C0'	11.117	489	'F3'	11.443
438.25	'28'	10.144	451	'5B'	10.47	463.75	'8E'	10.797	476.5	'C1'	11.123	489.25	'F4'	11.45
438.5	'29'	10.15	451.25	'5C'	10.477	464	'8F'	10.803	476.75	'C2'	11.13	489.5	'F5'	11.456
438.75	'2A'	10.157	451.5	'5D'	10.483	464.25	'90'	10.81	477	'C3'	11.136	489.75	'F6'	11.462
439	'2B'	10.163	451.75	'5E'	10.49	464.5	'91'	10.816	477.25	'C4'	11.142	490	'F7'	11.469
439.25	'2C'	10.17	452	'5F'	10.496	464.75	'92'	10.822	477.5	'C5'	11.149	490.25	'F8'	11.475
439.5	'2D'	10.176	452.25	'60'	10.502	465	'93'	10.829	477.75	'C6'	11.155	490.5	'F9'	11.482
439.75	'2E'	10.182	452.5	'61'	10.509	465.25	'94'	10.835	478	'C7'	11.162	490.75	'FA'	11.488
440	'2F'	10.189	452.75	'62'	10.515	465.5	'95'	10.842	478.25	'C8'	11.168	491	'FB'	11.494
440.25	'30'	10.195	453	'63'	10.522	465.75	'96'	10.848	478.5	'C9'	11.174	491.25	'FC'	11.501
440.5	'31'	10.202	453.25	'64'	10.528	466	'97'	10.854	478.75	'CA'	11.181	491.5	'FD'	11.507
440.75	'32'	10.208	453.5	'65'	10.534	466.25	'98'	10.861	479	'CB'	11.187	491.75	'FE'	11.514

Table 2 Conversion table for 32.768 kHz reference input

AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)
438.53	'00'	10.125	451.58	'33'	10.46	464.64	'66'	10.794	477.7	'99'	11.128	490.75	'CC'	11.462
438.78	'01'	10.132	451.84	'34'	10.466	464.9	'67'	10.8	477.95	'9A'	11.135	491.01	'CD'	11.469
439.04	'02'	10.138	452.1	'35'	10.473	465.15	'68'	10.807	478.21	'9B'	11.141	491.26	'CE'	11.475
439.3	'03'	10.145	452.35	'36'	10.479	465.41	'69'	10.813	478.46	'9C'	11.148	491.52	'CF'	11.482
439.55	'04'	10.152	452.61	'37'	10.486	465.66	'6A'	10.82	478.72	'9D'	11.154	491.78	'D0'	11.488
439.81	'05'	10.158	452.86	'38'	10.492	465.92	'6B'	10.827	478.98	'9E'	11.161	492.03	'D1'	11.495
440.06	'06'	10.165	453.12	'39'	10.499	466.18	'6C'	10.833	479.23	'9F'	11.167	492.29	'D2'	11.502
440.32	'07'	10.171	453.38	'3A'	10.505	466.43	'6D'	10.84	479.49	'A0'	11.174	492.54	'D3'	11.508
440.58	'08'	10.178	453.63	'3B'	10.512	466.69	'6E'	10.846	479.74	'A1'	11.18	492.8	'D4'	11.515
440.83	'09'	10.184	453.89	'3C'	10.519	466.94	'6F'	10.853	480	'A2'	11.187	493.06	'D5'	11.521
441.09	'0A'	10.191	454.14	'3D'	10.525	467.2	'70'	10.859	480.26	'A3'	11.194	493.31	'D6'	11.528
441.34	'0B'	10.197	454.4	'3E'	10.532	467.46	'71'	10.866	480.51	'A4'	11.2	493.57	'D7'	11.534
441.6	'0C'	10.204	454.66	'3F'	10.538	467.71	'72'	10.872	480.77	'A5'	11.207	493.82	'D8'	11.541
441.86	'0D'	10.211	454.91	'40'	10.545	467.97	'73'	10.879	481.02	'A6'	11.213	494.08	'D9'	11.547
442.11	'0E'	10.217	455.17	'41'	10.551	468.22	'74'	10.886	481.28	'A7'	11.22	494.34	'DA'	11.554
442.37	'0F'	10.224	455.42	'42'	10.558	468.48	'75'	10.892	481.54	'A8'	11.226	494.59	'DB'	11.561
442.62	'10'	10.23	455.68	'43'	10.564	468.74	'76'	10.899	481.79	'A9'	11.233	494.85	'DC'	11.567
442.88	'11'	10.237	455.94	'44'	10.571	468.99	'77'	10.905	482.05	'AA'	11.239	495.1	'DD'	11.574
443.14	'12'	10.243	456.19	'45'	10.578	469.25	'78'	10.912	482.3	'AB'	11.246	495.36	'DE'	11.58
443.39	'13'	10.25	456.45	'46'	10.584	469.5	'79'	10.918	482.56	'AC'	11.253	495.62	'DF'	11.587
443.65	'14'	10.256	456.7	'47'	10.591	469.76	'7A'	10.925	482.82	'AD'	11.259	495.87	'E0'	11.593
443.9	'15'	10.263	456.96	'48'	10.597	470.02	'7B'	10.931	483.07	'AE'	11.266	496.13	'E1'	11.6
444.16	'16'	10.269	457.22	'49'	10.604	470.27	'7C'	10.938	483.33	'AF'	11.272	496.38	'E2'	11.606
444.42	'17'	10.276	457.47	'4A'	10.61	470.53	'7D'	10.945	483.58	'B0'	11.279	496.64	'E3'	11.613
444.67	'18'	10.283	457.73	'4B'	10.617	470.78	'7E'	10.951	483.84	'B1'	11.285	496.9	'E4'	11.62
444.93	'19'	10.289	457.98	'4C'	10.623	471.04	'7F'	10.958	484.1	'B2'	11.292	497.15	'E5'	11.626
445.18	'1A'	10.296	458.24	'4D'	10.63	471.3	'80'	10.964	484.35	'B3'	11.298	497.41	'E6'	11.633
445.44	'1B'	10.302	458.5	'4E'	10.636	471.55	'81'	10.971	484.61	'B4'	11.305	497.66	'E7'	11.639
445.7	'1C'	10.309	458.75	'4F'	10.643	471.81	'82'	10.977	484.86	'B5'	11.312	497.92	'E8'	11.646
445.95	'1D'	10.315	459.01	'50'	10.65	472.06	'83'	10.984	485.12	'B6'	11.318	498.18	'E9'	11.652
446.21	'1E'	10.322	459.26	'51'	10.656	472.32	'84'	10.99	485.38	'B7'	11.325	498.43	'EA'	11.659
446.46	'1F'	10.328	459.52	'52'	10.663	472.58	'85'	10.997	485.63	'B8'	11.331	498.69	'EB'	11.665
446.72	'20'	10.335	459.78	'53'	10.669	472.83	'86'	11.003	485.89	'B9'	11.338	498.94	'EC'	11.672
446.98	'21'	10.342	460.03	'54'	10.676	473.09	'87'	11.01	486.14	'BA'	11.344	499.2	'ED'	11.679
447.23	'22'	10.348	460.29	'55'	10.682	473.34	'88'	11.017	486.4	'BB'	11.351	499.46	'EE'	11.685
447.49	'23'	10.355	460.54	'56'	10.689	473.6	'89'	11.023	486.66	'BC'	11.357	499.71	'EF'	11.692
447.74	'24'	10.361	460.8	'57'	10.695	473.86	'8A'	11.03	486.91	'BD'	11.364	499.97	'F0'	11.698
448	'25'	10.368	461.06	'58'	10.702	474.11	'8B'	11.036	487.17	'BE'	11.37	500.22	'F1'	11.705
448.26	'26'	10.374	461.31	'59'	10.709	474.37	'8C'	11.043	487.42	'BF'	11.377	500.48	'F2'	11.711
448.51	'27'	10.381	461.57	'5A'	10.715	474.62	'8D'	11.049	487.68	'C0'	11.384	500.74	'F3'	11.718
448.77	'28'	10.387	461.82	'5B'	10.722	474.88	'8E'	11.056	487.94	'C1'	11.39	500.99	'F4'	11.724
449.02	'29'	10.394	462.08	'5C'	10.728	475.14	'8F'	11.062	488.19	'C2'	11.397	501.25	'F5'	11.731
449.28	'2A'	10.401	462.34	'5D'	10.735	475.39	'90'	11.069	488.45	'C3'	11.403	501.5	'F6'	11.737
449.54	'2B'	10.407	462.59	'5E'	10.741	475.65	'91'	11.076	488.7	'C4'	11.41	501.76	'F7'	11.744
449.79	'2C'	10.414	462.85	'5F'	10.748	475.9	'92'	11.082	488.96	'C5'	11.416	502.02	'F8'	11.751
450.05	'2D'	10.42	463.1	'60'	10.754	476.16	'93'	11.089	489.22	'C6'	11.423	502.27	'F9'	11.757
450.3	'2E'	10.427	463.36	'61'	10.761	476.42	'94'	11.095	489.47	'C7'	11.429	502.53	'FA'	11.764
450.56	'2F'	10.433	463.62	'62'	10.768	476.67	'95'	11.102	489.73	'C8'	11.436	502.78	'FB'	11.77
450.82	'30'	10.44	463.87	'63'	10.774	476.93	'96'	11.108	489.98	'C9'	11.443	503.04	'FC'	11.777
451.07	'31'	10.446	464.13	'64'	10.781	477.18	'97'	11.115	490.24	'CA'	11.449	503.3	'FD'	11.783
451.33	'32'	10.453	464.38	'65'	10.787	477.44	'98'	11.121	490.5	'CB'	11.456	503.55	'FE'	11.79

Critics may fault the current growth of information technology for increasing society's already voracious appetite for paper, but it can work the other way too. Certainly one of today's most extravagant consumers of paper is the familiar telephone directory — printed in the millions, reissued regularly, and never quite up to date. Now, however, it is at the threshold of extinction — a victim of information technology. In France, it is soon to be replaced by MINITEL, a continually updated, nationwide directory that will be accessible to subscribers via terminals in their homes and offices. What's more, MINITEL is a multi-function videotext system with which it is planned to give users access to other information and data services as well. The French Telecommunications Administration chose a wide range of our products — picture tubes, ICs, and other components — to realize this innovative approach to subscriber services.

Although a video display terminal may seem an expensive substitute for a mundane telephone book, the French Telecommunications Administration expects to recoup the investment within a very few years through savings of printing, paper, and distribution costs. Not to mention the convenience to subscribers of having a directory that is always up to date!

Modifying Teradyne 283 programs to test high-speed CMOS logic ICs

J. EXALTO and H. KERN

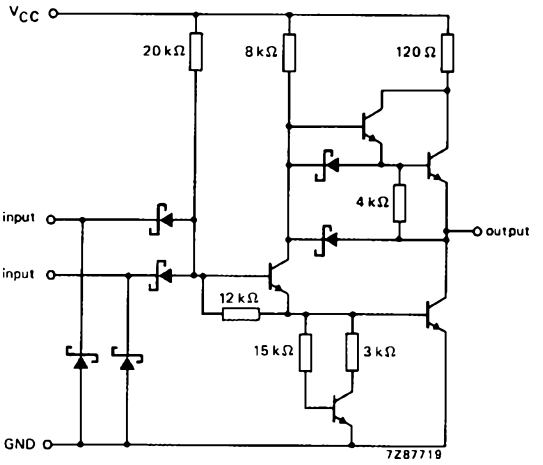
The PC54/74 HC/HCU/HCT family of high-speed CMOS (HCMOS) logic ICs has the low power consumption, high input noise immunity and wide operating temperature range of earlier silicon-gate CMOS, combined with the high speed and drive capability previously only attainable with bipolar LSTTL. Circuits with the type number suffix HCT have the additional advantages of TTL input switching levels, operation from a supply voltage range of 5 V ±10% and pin compatibility with most popular LSTTL circuits. These advantages, will result in PC54/74 HCT circuits being used to replace their LSTTL counterparts in many existing logic systems. This will lower the overall power consumption of the systems without reducing their operating speed, but it will no longer be possible to use the same test programs to test the HCMOS circuits on the equipment which is normally used to test the bipolar LSTTL circuits. Since the Teradyne 283 is one of the most widely used logic testers, we shall show how its programs can easily be modified for testing PC54/74HCT logic ICs.

Using an existing LSTTL test program, without modification, to test an HCMOS circuit will result in a "FAIL". Analysis of this "FAIL" will reveal that only two or three of the parameter tests have failed and the remainder have passed. The parameter test failures occur because the input and output structures of HCMOS and LSTTL circuits as shown in Fig.1 are not the same. The failures don't indicate that the HCMOS circuits are unsuitable as LSTTL replacements, but the test program must be modified to obtain a "PASS" for the HCMOS circuits when they are tested on the Teradyne 283 tester.

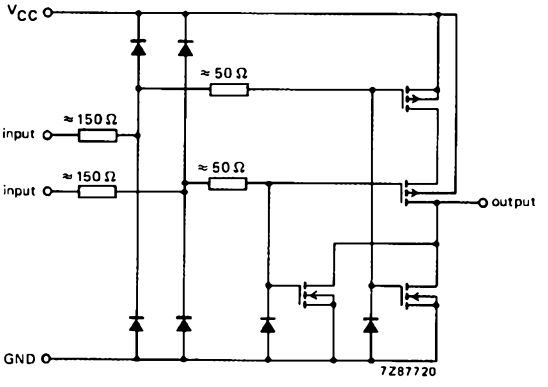
The parameter tests which must be modified for use with HCMOS circuits can be divided into the following two categories:

1. Those tests that must be modified to obtain a "PASS" for the HCMOS circuits. For these tests, it is only necessary to modify the settings that cause problems. This will result in a test that confirms the ability of the HCMOS circuit to perform the LSTTL function

2. Those tests that must be modified to test the circuit to the HCMOS specification if the user wishes to take advantage of the additional HCMOS features.



(a) 2-input LSTTL NAND gate with totem-pole outputs (¼ 54/74LS00). For other structures, refer to published data



(b) 2-input HCMOS NOR gate (¼ PC54/74HCT02)

Fig.1 Comparison of LSTTL and HCMOS circuit structures

CATEGORY 1 TESTS

Input current at V_I = 7 V

Due to the input protection network of HCMOS circuits shown in Fig.1(b), input current will flow if the input voltage exceeds V_{CC} by 0,5 V or more. To prevent a "FAIL", the input voltage must be reduced to V_{CC}. To test the exact input leakage current, the setting must be modified according to the d.c. characteristics for PC54/74HCT circuits given in Appendix 2.

Input clamp voltage

The protection network for each HCMOS circuit input incorporates a series resistor that will cause the input clamp voltage with an input current of −18 mA to be much lower than the −1,5 V specified for LSTTL. Since the input clamp voltage is not specified for HCMOS circuits, this test must be omitted.

Output short-circuit current HIGH

Due to the symmetrical output structure of HCMOS circuits as shown in Fig.1(b), the LSTTL collector output resistor is not present. HCMOS circuits will therefore draw a much higher short-circuit output current than their LSTTL equivalents. Since the output short-circuit current is not specified for HCMOS circuits, this test must be omitted.

Hysteresis

The octal buffer/line drivers in the PC54/74HCT range do not have input hysteresis. This test must therefore be omitted.

Output voltage LOW at I_O = 12 mA (buffers)

The LOW level output voltage for HCMOS bus drivers is specified for an output current of 6 mA. The current setting must therefore be reduced to 6 mA.

Output voltage LOW at I_O = 8 mA

The LOW level output voltage is not specified at this output current level for HCMOS circuits. This test must therefore be omitted.

Continuity

With some settings used for continuity testing, the input resistor of HCMOS circuits could cause a "FAIL". This must therefore be borne in mind when test engineers select their individual settings for this test.

CATEGORY 2 TEST

Quiescent supply current

Setting supply current I_{CC} for the output LOW condition for HCMOS circuits will not cause problems, but setting it for the output HIGH condition is more complicated. If the Teradyne 283 doesn't have a hardware CMOS modification, there is a comparator connected to each of the outputs of the circuit under test. These comparators cause an extra load current of about 7 μA per output, the precise current depending on the specific tester. The extra load currents are negligible compared with the I_{CC} of LSTTL circuits and can be ignored. When measuring HCMOS circuits however, they can be very significant compared with the total I_{CC} and must be taken into account. A solution to this problem is to connect the HIGH outputs to V_{CC} so that they are excluded from the I_{CC} measuring path. This can be done with the statement MTEST VCC1 A B C D, where A, B, C, and D are the outputs in the HIGH state.

Output voltage LOW at I_O = 4 mA

The lower output voltages of HCMOS circuits can be tested without any complications.

Output voltage HIGH

The higher output voltages of HCMOS circuits can be tested without any complications.

Short-circuit output current with V_O = 0,5 V

Although this parameter is not specified for HCMOS circuits, they will meet the same requirements as LSTTL circuits. This test, however, can be omitted.

OFF-state output current for 3-state outputs with $V_O = V_{CC}$ or GND

The lower leakage current for HCMOS circuits can be tested without any complications.

Input leakage current with V_I HIGH or LOW

The much lower input leakage currents of HCMOS circuits can be tested without any complications.

Function

This test can remain unchanged.

APPENDIX 1 DC characteristics for LSTTL circuits

These figures are for positive NAND gates and inverters with totem-pole outputs.
For the characteristics of other types, refer to published data for LSTLL circuits.

Voltages are referenced to GND (ground = 0 V).

parameter	V_{CC}	symbol	54LS			74LS			unit	conditions
			min	typ	max	min	typ	max		
Operating temperature	*	T_{amb}	−55	–	125	0	–	70	°C	
HIGH level input voltage	*	V_{IH}	2	–	–	2	–	–	V	
LOW level input voltage	*	V_{IL}	–	–	0,7	–	–	0,8	V	
Input clamp voltage	min	V_{IK}	–	–	−1,5	–	–	−1,5	V	I_I = −18 mA
HIGH level output voltage	min	V_{OH}	2,5	3,4	–	2,7	3,4	–	V	V_{IL} = max, I_{OH} = −400 µA
LOW level output voltage	min	V_{OL}	–	0,25	0,4	–	–	0,4	V	V_{IH} = 2 V, I_{OL} = 4 mA
LOW level output voltage	min	V_{OL}	–	–	–	–	0,25	0,5	V	V_{IH} = 2 V, I_{OL} = 8 mA
Input current at V_I = 7 V	max	I_I	–	–	0,1	–	–	0,1	mA	
HIGH level input current	max	I_{IH}	–	–	20	–	–	20	µA	V_{IH} = 2,7 V
LOW level input current	max	I_{IL}	–	–	−0,4	–	–	−0,4	mA	V_{IL} = 0,4 V
Short-circuit output current	max	I_{OS}	−20	–	−100	−20	–	−100	mA	

For 54 LS, V_{CC} = 4,5 V to 5,5 V; for 74LS, V_{CC} = 4,75 V to 5,25 V.
All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
For short-circuit output current, only one output must be shorted, and for not more than one second.
* over V_{CC} range.

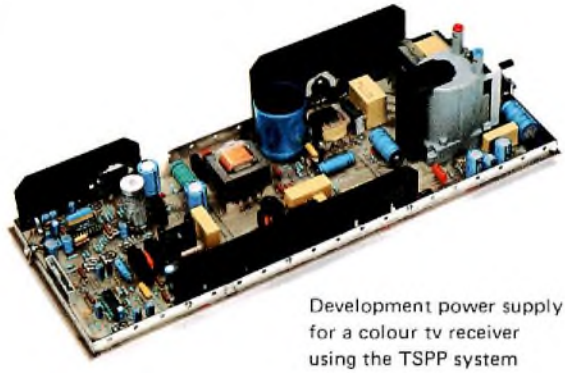
APPENDIX 2 DC characteristics for the PC54/74HCT family of circuits

Voltages are referenced to GND (ground = 0 V).

parameter	V_{CC} V	symbol	T_{amb} (°C)							unit	conditions	
			PC54HCT/PC74HCT +25			PC74HCT −40 to +85		PC54HCT −55 to +125			V_I	others
			min.	typ.	max.	min.	max.	min.	max.			
HIGH level input voltage	4,5 to 5,5	V_{IH}	2,0	–	–	2,0	–	2,0	–	V		
LOW level input voltage	4,5 to 5,5	V_{IL}	–	–	0,8	–	0,8	–	0,8	V		
HIGH level output voltage all outputs	4,5	V_{OH}	4,4	4,5	–	4,4	–	4,4	–	V	V_{IH} or V_{IL}	$-I_O$ = 20 µA
HIGH level output voltage standard outputs	4,5	V_{OH}	3,98	–	–	3,84	–	3,7	–	V	V_{IH} or V_{IL}	$-I_O$ = 4,0 mA
HIGH level output voltage bus driver outputs	4,5	V_{OH}	3,98	–	–	3,84	–	3,7	–	V	V_{IH} or V_{IL}	$-I_O$ = 6,0 mA
LOW level output voltage all outputs	4,5	V_{OL}	–	0	0,1	–	0,1	–	0,1	V	V_{IH} or V_{IL}	I_O = 20 µA
LOW level output voltage standard outputs	4,5	V_{OL}	–	–	0,26	–	0,33	–	0,4	V	V_{IH} or V_{IL}	I_O = 4,0 mA
LOW level output voltage bus driver outputs	4,5	V_{OL}	–	–	0,26	–	0,33	–	0,4	V	V_{IH} or V_{IL}	I_O = 6,0 mA
Input leakage current	5,5	$\pm I_I$	–	–	0,1	–	1,0	–	1,0	µA	V_{IH} or V_{IL}	
Analog switch OFF-state current per channel	5,5	$\pm I_S$	–	–	0,1	–	1,0	–	1,0	µA	V_{IH} ot V_{IL}	$\|V_S\| = V_{CC}$
3-state output OFF-state current	5,5	$\pm I_{OZ}$	–	–	0,5	–	5,0	–	10,0	µA	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; I_O = 0
Quiescent supply current												
SSI	5,5	I_{CC}	–	–	2,0	–	20,0	–	40,0	µA	V_{CC} or	I_O = 0
flip-flops	5,5	I_{CC}	–	–	4,0	–	40,0	–	80,0	µA	GND	I_O = 0
MSI	5,5	I_{CC}	–	–	8,0	–	80,0	–	160,0	µA		I_O = 0

Twin-switch power pack for 110° colour tv

C. H. J. BERGMANS



Development power supply for a colour tv receiver using the TSPP system

The new diode-split transformer used in the TSPP system

Present deflection and supply circuits for 90° raster-correction-free display systems and 110° systems are incompatible and require different chassis. Furthermore, the output transformer in our synchronized power pack for 110° systems (Ref.1) is by today's standards rather bulky. Therefore, we are introducing a new television supply system known as the twin-switch power pack (TSPP). The TSPP (Fig.1) is a combined mains-isolated horizontal-deflection circuit and power supply for 110° display systems. Like its predecessor, the synchronized power pack, it uses a power supply synchronized with the horizontal scan to generate all the needed d.c. supply voltages, including the e.h.t., and to drive the horizontal deflection output transistor. The switch in the power pack part of the TSPP is a BU505, the deflection switch is a BU508A.

The twin-switch power pack uses a new diode-split transformer, the AT2077/82. This transformer, smaller and cheaper than existing types but with the same high conversion efficiency, can be supplied with almost identical pinning for single-switch power packs for raster-correction-free (r.c.f.) systems. Consequently, one chassis can be used to accommodate the power supply of both 90° r.c.f. and 110° systems.

To meet present trends in tv sound reproduction, the TSPP can also supply audio amplifiers rated at 2 x 15 W without distorting picture width or height. The audio supply is taken from a secondary winding of the input choke.* The TSPP can operate from mains voltages between 180 V and 265 V.

* Since it has more than one winding, this component is depicted by the symbol for a transformer on circuit diagrams. Throughout this article it will nevertheless be referred to as a choke in accordance with its main function.

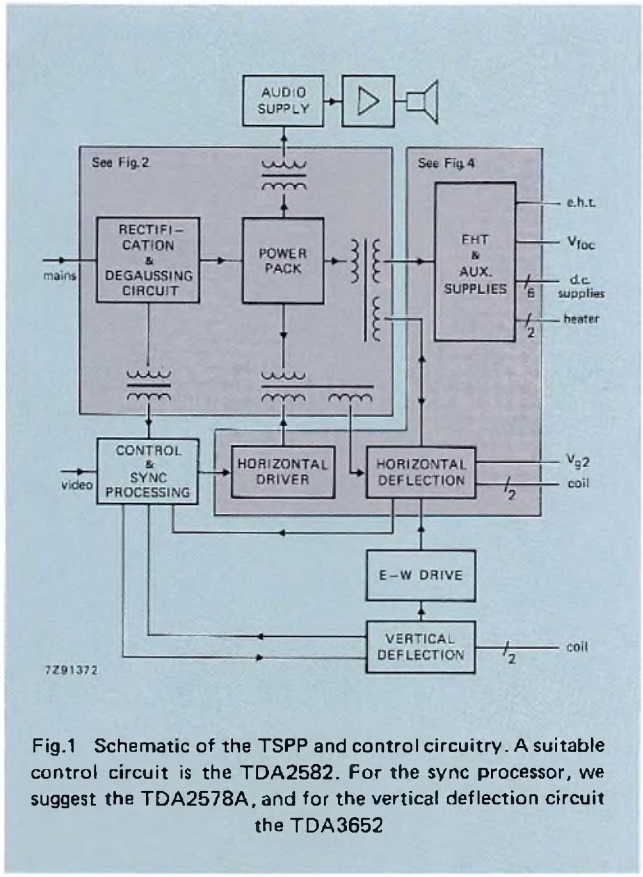


Fig.1 Schematic of the TSPP and control circuitry. A suitable control circuit is the TDA2582. For the sync processor, we suggest the TDA2578A, and for the vertical deflection circuit the TDA3652

MAINS RECTIFICATION AND DEGAUSSING CIRCUIT

The mains voltage is full-wave rectified and smoothed to produce a d.c. supply voltage V_1 for the SMPS, see Fig.2. A 3,3 Ω resistor limits the in-rush current. The filter AT4043/55 reduces mains-injected interference. The degaussing circuit comprises a dual PTC thermistor and two series-connected degaussing coils. A small mains transformer TS561/2 is used to supply the starting voltage for the horizontal driver and for the control circuit. This transformer can also supply the stand-by voltage for a remote-control reciver.

POWER SUPPLY

The input choke T_1, D_1, D_2, TR_1, C_1 and T_2 form a power supply that delivers all the voltages needed by the set. The voltage across C_1, which is the supply voltage for the rest of the TSPP circuit, is stabilized at 100 V by controlling the duty cycle of TR_1. During scan, C_1 maintains a constant potential across the primary of T_2; during flyback, negative-going flyback pulses appear across the primary of T_2. Rectification of a secondary winding voltage from T_2 during the scan period provides low-voltage supplies for the receiver circuits. Rectification of a separate secondary winding voltage from T_2 during the flyback period provides the e.h.t. and focus supply.

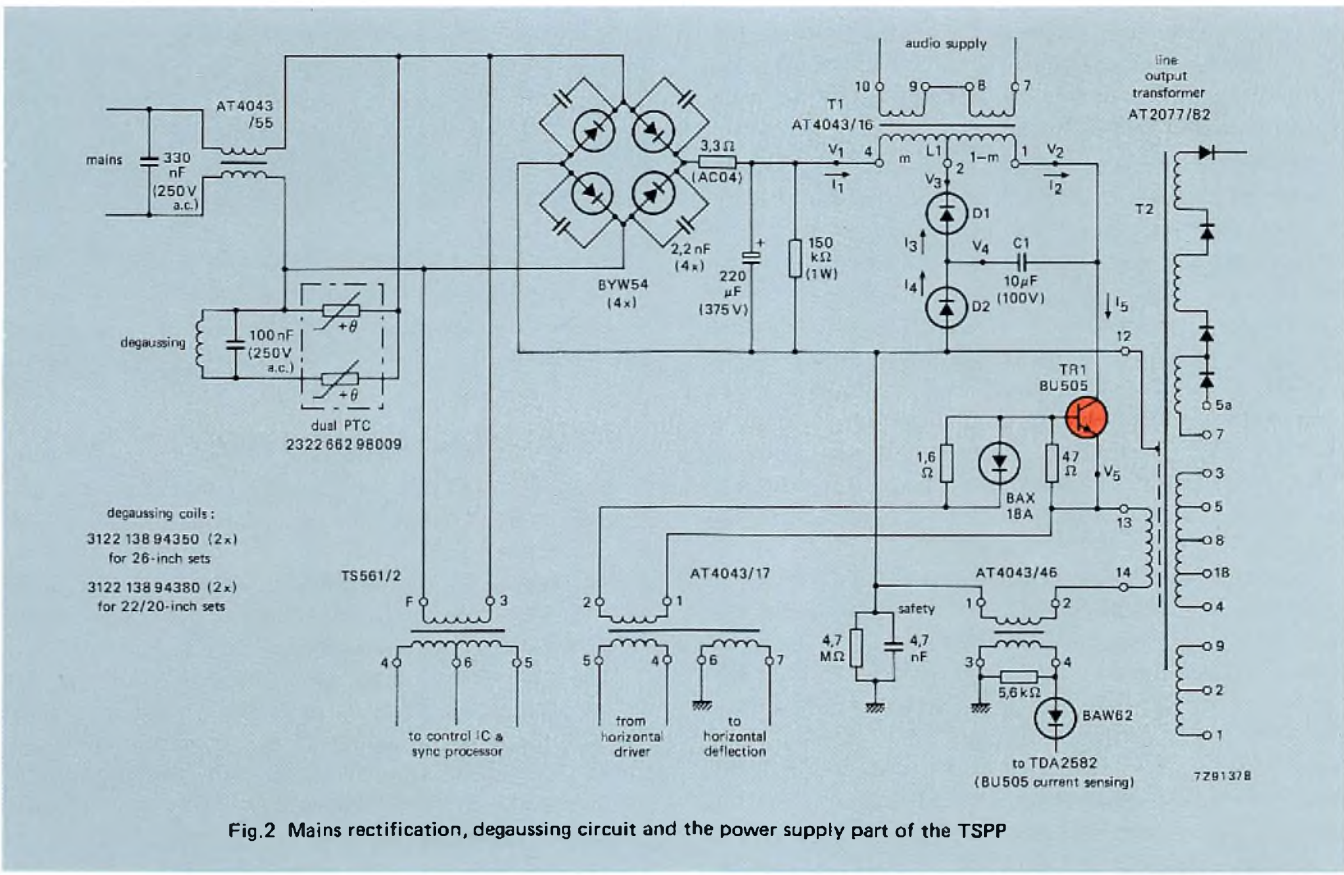


Fig.2 Mains rectification, degaussing circuit and the power supply part of the TSPP

The voltage across C_1 is:

$$V_{C1} = \frac{m\delta}{1 - \delta(1 - m)} V_1 \qquad \text{(Refs.2 and 3)}$$

where:

m is the tap on the input choke (0,4 for TSPP)
δ is the duty cycle of TR_1
V_1 is the rectified mains voltage.

The tap on the input choke is chosen so that the power supply operates over the mains voltage range 180 V to 265 V, with V_{C1} chosen as high as possible to keept the current in TR_1 and T_2 low. For the aforementioned mains voltages, the duty cycle of TR_1 varies between 0,62 and 0,47 to keep the supply capacitor C_1 charged to 100 V.

The voltage across TR_1 is the sum of a square-wave voltage and a flyback voltage transformed from the line part of T_2, see Fig.3. For 220 V mains and nominal beam current, the peak voltage across TR_1 is 1260 V.

During horizontal scan, the voltage on the secondary of the diode-split transformer is rectified by the second power switch (the horizontal deflection transistor TR_2), or by the diodes connected across it, see Fig.4. This rectified output voltage is 150 V and is on pin 9. When transformed to the primary side, this "d.c. voltage" corresponds to a capacitor charged to 100 V, i.e. corresponds to the charged supply capacitor C_1. When TR_1 is turned on, the primary winding is connected across C_1 (via TR_1 and D_2), so any loading on the 150 V output will discharge C_1 on the primary side. C_1 is recharged by controlling the duty cycle of TR_1, the energy stored in the input choke T_1 being transferred to C_1 when TR_1 is switched off.

During flyback, the flyback pulse on the secondary winding of the diode-split transformer is transformed to the primary. However, since the primary has no flyback capacitor, unlike the single-switch power pack circuit, turning-off TR_1 and TR_2 isn't critical provided TR_1 switches off first. When TR_1 is switched off while TR_2 is conducting, the magnetizing current of about 1,2 A flowing in the primary of the diode-split transformer has to be handled temporarily by TR_2. For a turns ratio (primary:secondary) of 1:1,5, TR_2 will have an additional collector current of 0,8 A at the end of scan, making a total of about 3,8 A at the end of scan. This is well within the current rating of the BU508A.

Note that an increase in beam current will produce an increase in V_{C1}, owing to the stabilized 150 V on pin 9 of the transformer. An increased V_{C1} means an increased flyback voltage for part of the flyback time. For a 220 V mains and 1,5 mA beam current, the maximum voltage across the BU505 of the SMPS is 1290 V (450 V square-wave voltage plus 840 V flyback voltage). For a 265 V mains, the square-wave voltage is $45\sqrt{2}$ higher, 515 V, and the maximum voltage will then be 1365 V. For the BU505 which has a V_{CESM} of 1500 V, the flyback voltage may then be up to 1500 − 515 = 985 V. This is 17,3% above nominal and will allow for increased flyback voltage due to component tolerances.

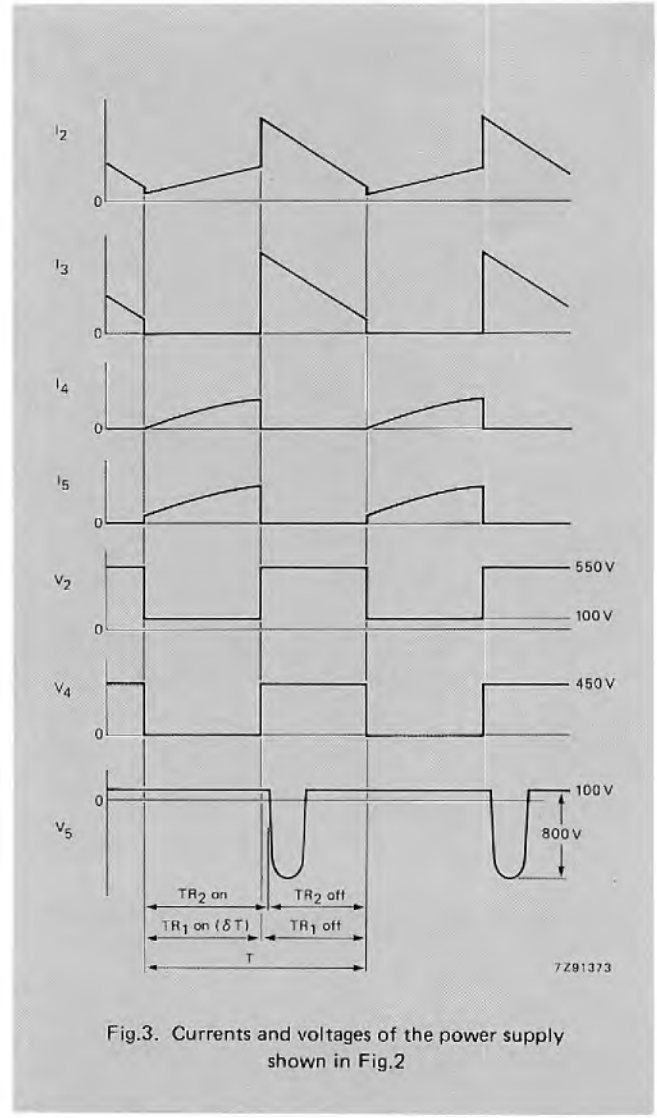


Fig.3. Currents and voltages of the power supply shown in Fig.2

EHT AND AUXILIARY SUPPLIES

Table 1 gives brief data on the new diode-split transformer. Typical power consumption in a complete CTV receiver would be about 65 W.

The supply for the picture-tube heater is across pins 4 and 18. To reduce the heater voltage to 6,3 V, a resistor of 2,7 Ω should be connected in series with pin 4.

The V_{g2} voltage can be taken from pin 7. However, if it is, measures should be taken to prevent possible damage to the phosphors in the middle of the screen should the deflection circuit fail, since the e.h.t., V_{foc}, and V_{g2} will still be present. Much better is to take V_{g2} from the horizontal deflection circuit, see Fig.4. With this arrangement, V_{g2} is interrupted when horizontal deflection stops.

Fig.4 Horizontal deflection circuitry and derivation of the auxiliary and e.h.t. supplies from the new diode-split transformer of the TSPP

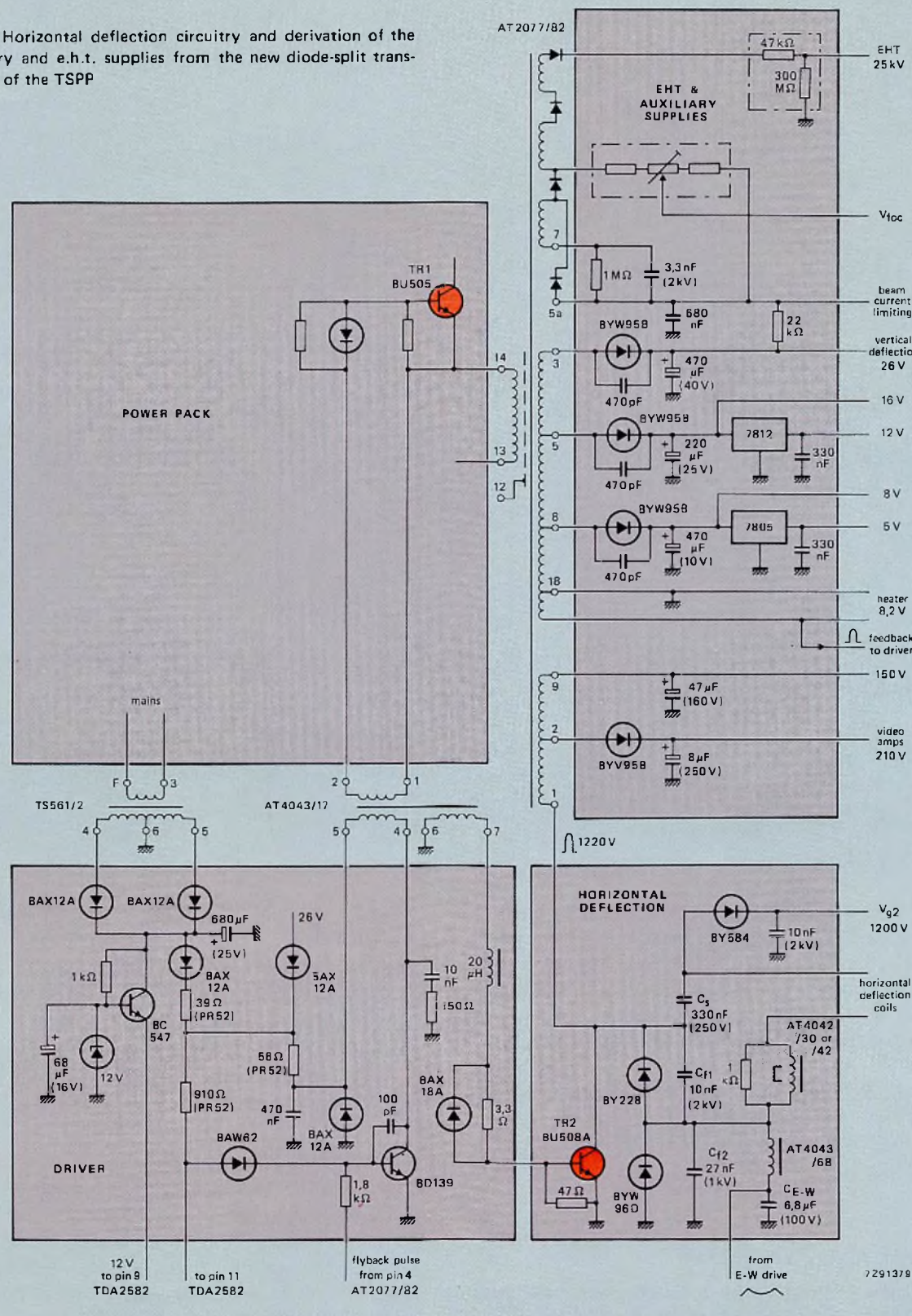


TABLE 1
AT2077/82 diode-split transformer

	beam current	mA	0	1	1,5
e.h.t. supply	I_{eht}*	mA	0,08	1,08	1,58
	e.h.t	kV	25	24,1	23,65
	V_{focus}	kV	5,6 to 9,1		
	R_{int}	MΩ		0,9	
power supply	V_{CE} of TR_1, with 220 V mains	V	1260	1270	1290
	I_C of TR_1	A	1,7	2,1	2,15
	V_{C1}	V	100	101	101,5
	$V_{pin\ 9}$	V	150	150	150
deflection	flyback time	µs	11,5	11,5	11,5
	V_{CE} of TR_2	V	1220	1230	1235
	I_C of TR_2	A	3,45	3,65	3,8
	deflection current	A	5,3	5,25	5,2
	overscan	%	6	6	6

auxiliary supplies		after rectification	remarks
Pin 1	+1220 V p-p		flyback voltage
Pin 2	+87 V p-p plus 139 V d.c.	210 V	video amplifier
Pin 3	−218 V p-p	26 V	vert. deflection
Pin 4	+29 V p-p	8,2 V r.m.s.	heater voltage
Pin 5	−129 V p-p	16 V	12 V after regulation
Pin 7	1120 to 1145 V d.c.		V_{g2} (optional)
Pin 8	−74 V p-p	8 V	5 V after regulation
Pin 9	150 V d.c.	150 V	line deflection

the +/− signs indicate the winding polarities.
* with 300 MΩ bleeder to earth.

In some receiver designs, the load on the auxiliary supplies could cause the absolute maximum current rating of the BU505 to be exceeded. In these cases a suitable replacement would be the BU508A as used for the deflection switch. If this modification is made, the 1,6 Ω resistor in the base of the transistor should be replaced by a 3,3 Ω resistor.

The mains interference screen (pin 12) should be earthed on the mains side of the circuit. To prevent a build-up of static charge, the transformer core should be earthed on the secondary side.

CONTROL AND SYNC CIRCUITS

Suitable integrated circuits for controlling the power pack and for sync processing are the well-known TDA2578A and TDA2582. The operation of each is summarized below.

TDA2578A: Sync circuit with vertical oscillator and driver

The TDA2578A derives the horizontal and vertical sync pulses from the composite video signal and feeds the sync pulses to internal horizontal and vertical oscillators. The vertical output signal is fed to the vertical output amplifier e.g. the TDA3652. The TDA2578A also controls the phase of the output pulse using the video signal as reference.

TDA2582: Control circuit

The TDA2582 delivers duty-cycle-controlled pulses to the line driver stage where, via the AT4043/17, they are used to regulate the duty cycle of the power supply. The 150 V supply from the secondary of the diode-split transformer is used as a feedback signal to control the duty cycle of the pulses. The oscillator of the TDA2582 is synchronized with the video signal via the sync. separator in the TDA2578A.

When the circuit is first connected to the mains, the internal slow-start circuitry is activated. This slowly increases the duty cycle of the output pulses from zero until the feedback voltage reaches its correct value.

A small current-sensing transformer AT4043/46 is used to monitor the collector current of the BU505, the transformed voltage being fed to the input of the overvoltage protection circuit of the TDA2582. Part of the flyback voltage, is fed to the same input. When either voltage exceeds a preset level, the output of the TDA2582 is turned off and the slow-start procedure activated.

The supply voltage for the TDA2582 and for the output stage of the sync circuit is from a small mains transformer TS561/2. The rectified secondary voltage of this transformer is about 24 V d.c. This voltage is also used to supply the line driver stage during start-up. The 12 V supply voltage for the ICs is derived from this voltage by a stabilizer comprising a zener diode and a BC547 transistor.

LINE DRIVER

The duty cycle controlled pulses from the TDA2582 are fed to the base of the BD139 driver transistor. The two power switches are driven by a transformer AT4043/17 having two secondary windings. The leakage inductance from the secondary winding for TR_1 is about 10 μH and that for TR_2 about 4 μH, the difference being due to the mains-isolation. A 20 μH coil connected in the base of TR_2 ensures that TR_1 switches off before TR_2. To prevent the power switches being forward driven during flyback (e.g. at maximum duty cycle), a flyback pulse from pin 4 of the diode-split transformer is fed to the base of the driver transistor.

HORIZONTAL DEFLECTION

The supply voltage for the horizontal deflection circuit is a scan rectified secondary voltage of the diode-split transformer (150 V). The deflection circuit is the well-known one, with diode modulator. The flyback pulses on the collector of TR_2 are fed direct to the diode-split transformer on pin 1 and used to generate the e.h.t. supply in the usual way. The e.h.t. supply has a low (0,9 MΩ) internal impedance, owing to very tight coupling between the secondary winding and the e.h.t. winding. It has already been mentioned that the V_{g2} voltage can be obtained from the horizontal deflection circuit by rectification of the collector voltage of the BU508A.

E-W DRIVE

The frame-frequency parabolic voltage applied to the diode modulator in the horizontal deflection circuit to correct E-W pin cushion distortion can be generated in the usual way by integration of the sawtooth voltage across the feedback resistor in the vertical deflection circuit. A suitable E-W drive circuit is described in Ref.4.

VERTICAL DEFLECTION

The TDA3652 (Ref.5) produces a vertical deflection current of up to 3 A (p-p) from the driver signal from the TDA2578A. It also generates a feedback signal for that IC. A flyback generator incorporated in the TDA3652 is used to keep the flyback time short when the supply voltage is low.

AUDIO SUPPLY

The TSPP provides the power for any audio amplifier not requiring a completely stabilized supply voltage. Continuous output power can be up to 2 x 15 W or 1 x 30 W with peak powers up to 50 W. A feature of the audio power supply is that operation of the horizontal and vertical deflection circuits is unaffected by large currents drawn by the audio amplifiers.

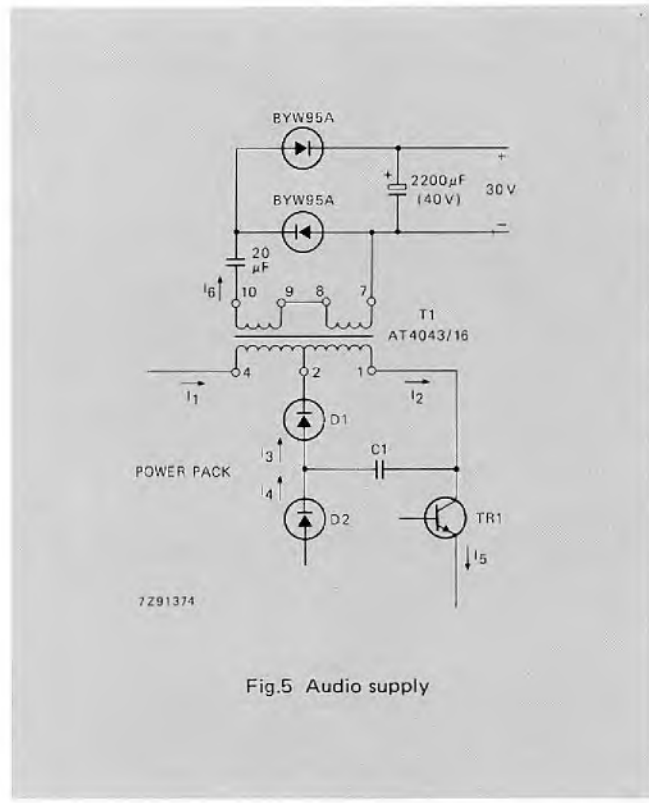


Fig.5 Audio supply

The audio supply is taken from a secondary winding of the input choke AT4043/16, see Fig.5. The secondary voltage is rectified by a resonant peak-to-peak rectifier. Although the source impedance is quite low, the output voltage is only partly stabilized against mains voltage variations. However, this won't give problems with class-B amplifiers having adequate supply rejection.

Figure 6 shows the equivalent circuit of the audio supply. The input voltage V_{in} is a square wave transformed from the primary side of the input choke. L_2 is the leakage inductance of the choke. C_2 and L_2 form a series resonant circuit. Diodes D_3 and D_4 form a peak-to-peak rectifier. C_3 is a smoothing capacitor. R_L represents an audio load.

Under no-load conditions, C_2 charges to V_6 during the negative excursions of V_{in}, and C_3 is charged to $|V_6 + V_7|$.

With R_L connected, C_3 discharges a little but is recharged when V_{in} is positive by a current flowing through L_2, C_2 and D_4. The amplitude of this charging current is determined by the load, the duration by the resonant frequency of the circuit. Charging C_3 discharges C_2 a little, but C_2 is recharged to V_6 via D_3, C_2 and L_2 when V_{in} is negative. The charging currents for C_2 and C_3 are identical since the resonant circuit is the same in each case. Figure 7 shows the sequence of events in more detail.

At t_0:
Capacitor C_2 has been discharged by ΔV_{C2} in the previous period owing to the load. V_{in} changes from a positive voltage to a negative one (V_6), producing a voltage across L_2 of:

$$V_{L2} = V_6 - (V_6 - \Delta V_{C2}) = +\Delta V_{C2}.$$

This voltage causes a current in the resonant circuit which charges C_2.

At t_1:

$V_{L2} = 0$ and $V_{C2} = V_6$,

and the charging current is a maximum. Between t_1 and t_2, the charging current falls to zero.

At t_2:
C_2 has charged to $V_6 + \Delta V_{C2}$. No current flows since there is no stored energy in L_2. Since D_3 is blocked, the voltage at point y changes to that of V_{in}, i.e. to V_6. The voltages at points y and z rise by ΔV_{C2}. From t_2 to t_3 there are no currents so nothing changes.

At t_3:
V_{in} changes from V_6 to V_7. The voltage across L_2 is:

$$V_{L2} = (V_6 + V_7) - (V_6 + \Delta V_{C2}) - V_7 = -\Delta V_{C2}.$$

This voltage causes a current through L_2, C_2, D_4 and C_3 identical to the current during t_0 to t_1, but in the opposite direction, since the sign of V_{L2} has reversed. Since the resonant circuit is the same, the current pulses will be identical for $C_3 \gg C_2$.

At t_4:
The supply current is a maximum. $V_y = V_7$ and $V_{C2} = V_6$.

At t_5, the supply curreht reaches zero and V_y and V_z fall by ΔV_{C2}.

From t_5 to t_0 nothing changes and at t_0 the cycle starts again. The current pulses in the choke secondary are transformed to the primary, but have no effect on the average current flowing in the input choke and have almost no effect on the storage time of TR_1, see Fig.8.

During the first current pulse I, the transformed current is subtracted from the current flowing in part m of the input choke. The second pulse II is added to this current. Therefore, the total average current flowing in the input choke is unaffected by the "audio currents" and so the d.c. voltage on the supply capacitor for the SMPS, C_1, in unaffected. The peak collector current of the switch is not influenced by the "audio" currents, so the storage time of this switch will hardly be affected. The maximum "audio" current is determined by the peak value of I_3.

The maximum width of the current pulses is set by the duty cycle of the SMPS and the audio supply current has to be zero when TR_1 is switched on.

In the case of a maximum duty cycle of 0,62 (180 V mains), the maximum duration of the audio supply pulses will be $T - \delta T = 64 - (0{,}62 \times 64) \approx 24\ \mu s$.

To reduce the cost of the audio supply circuit, C_3 can be replaced by a capacitor of 3,3 μF in series with a 12 μH choke. This will increase ΔV_{C2} without altering the resonant frequency of the circuit or changing the internal impedance of the audio supply.

TABLE 2
Key components of the TSPP system

diode-split line output transformer	AT2077/82	
linearity control	AT4042/30 or AT4042/08	
input choke	AT4043/16	
line driver transformer	AT4043/17	
current sensing transformer	AT4043/46	
bridge coil	AT4043/68	
stand-by supply transformer	TS561/2	
supply capacitor C_1	10 μF, 100 V	2222 344 90206
audio capacitor C_2	3,3 μF, 100 V	2322 344 21335
E-W capacitor (Fig.4)	6,8 μF, 100 V	2222 344 21685
flyback capacitor (Fig.4)	10 nF, 1500 V	2222 357 82103
flyback capacitor (Fig.4)	27 nF, 1000 V	2222 357 72273
S-correction capacitor (Fig.4)	330 nF, 250 V	2222 357 51334
resistor (inrush limiter)	3,3 Ω AC04	
resistor (start up supply)	39 Ω PR52	
resistor (line driver)	56 Ω PR52	
resistor (line driver)	910 Ω PR52	
power transistor TR_1	BU505	
power transistor TR_2	BU508A	
control IC	TDA2582	
sync processor IC	TDA2578A	
vertical deflection IC	TDA3652	

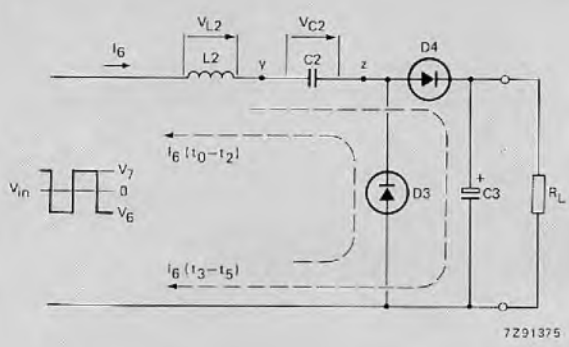


Fig.6 Equivalent circuit of the audio supply

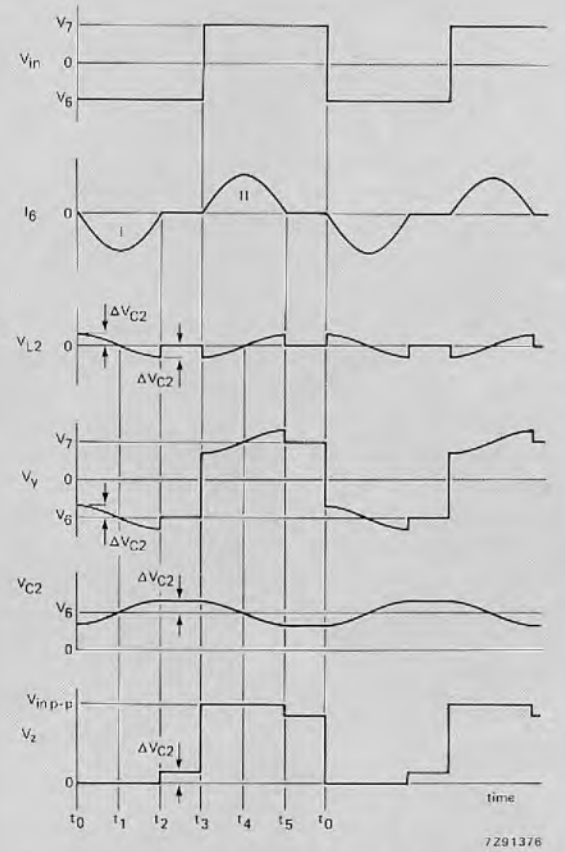


Fig.7 Currents and voltages shown in the circuit of Fig.6

REFERENCES

1. "Synchronized power pack (SPP) for colour TV receivers", Philips Technical Note 137, ordering code 9398 013 70011.
2. "Simplified synchronous power pack with diode-split transformer for colour TV", Philips Technical Publication 006, ordering code 9398 017 40011.
3. "Single-switch power pack system for television receivers with BU508A", Central Application Laboratory report EDS8105, Oct. 1981.
4. "East-west drive circuit for colour TV", Philips Technical Note 079, ordering code 9399 110 07901.
5. HAENEN, G. H., "Vertical deflection with the integrated power output circuit TDA3652", Central Application Laboratory report EDS8303, March 1983.

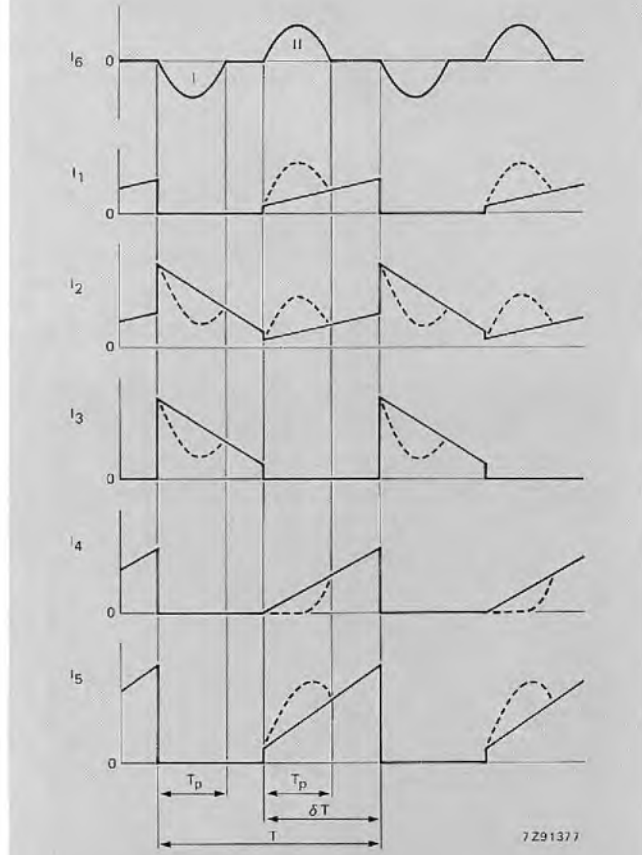


Fig.8 Effect of audio loads on the SMPS part of the TSPP, see Fig.5. ——— without audio load; – – – – with audio load

Wideband i.f. amplifier for satellite tv receiving systems

P. MOORS and T. H. UITTENBOGAARD

Hot on the heels of the direct tv Broadcast Satellite (DBS), scheduled for regular service in Europe by 1986, comes a host of advances in receiving systems, with major developments in dish antennas, 12-to-1 GHz downconverters, tuners, demodulators and decoders.

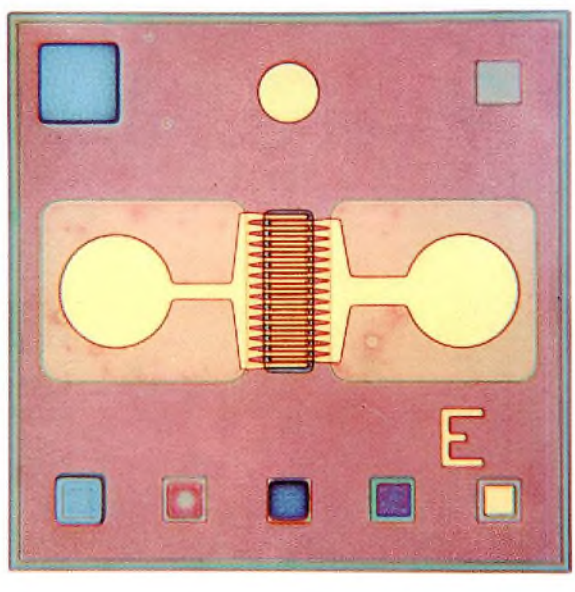


Fig.1 The BFG65 chip uses an extra-fine interdigitated electrode structure (2,5 μm base-emitter finger pitch, 0,75 μm emitter-finger width) which minimizes noise and increases gain by minimizing collector/base area. The chip also has extremely high f_T (typically 7,5 GHz) thanks to the use of shallow ion-implanted base and emitter regions and of very thin epitaxial layers (1,2 μm compared with 3 to 4 μm in equivalent devices)

A major factor dictating the speed with which these new systems gain popularity will be their cost. It's currently estimated that a complete receiving system (excluding tv receiver) should cost no more than a few hundred US dollars if it's to be of interest to the domestic-tv user. This means that there will be strong competition in all areas, and that products formerly the exclusive preserve of the professional market will have to be tailored to satisfy the far more cost-conscious consumer market.

This article describes one of these new developments – a wideband (950 to 1750 MHz) amplifier for the 1 GHz downconverter i.f. stage, and for the line extension stages in community systems (i.e. systems in which a single dish antenna serves several receivers). The amplifier is made up of discrete components and uses a new purpose-designed wideband npn transistor, the BFG65 (Fig.1), whose specifications are given in Table 1.

TABLE 1
BFG65 specifications

power gain (at 2 GHz)*	typically 11 dB
d.c. current gain (at I_C = 15 mA, V_{CE} = 5 V)	typically 100
transition frequency (at 500 MHz)*	typically 7,5 GHz
total power dissipation (up to T_{amb} = 60 °C)	<300 mW
max. junction temperature	150 °C
noise figure (at 2 GHz)*	typically 3 dB
feedback capacitance	typically 0,5 pF
encapsulation	SOT-103**

* I_C = 15 mA, V_{CE} = 8 V, T_{amb} = 25 °C.

** same chip also available as BFQ66 (SOT-173), BFQ65 (SOT-37) and BFQ67 (SOT-23).

This new transistor is closely related to our well established BFR/BFQ range of wideband transistors, and possesses many of their advanced features, including:

- *high f_T* thanks to the use of shallow ion-implanted base and emitter fingers and of very thin epitaxial layers (1,2 μm compared with 3 to 4 μm in equivalent devices) which help to minimize carrier transit time within the collector
- *low noise* thanks to high f_T combined with low base resistance, the latter coming from an extra-fine interdigitated electrode structure (2,5 μm base-emitter finger pitch, 0,75 μm emitter-finger width)
- *high gain* thanks to high f_T and low feedback capacitance, itself a result of the fine electrode structure which minimizes collector/base area
- *titanium/platinum/gold metallization* – comprising a gold conducting layer, and a platinum/titanium barrier layer (to prevent gold-silicon alloy formation); the titanium, moreover, acts as an adhesive and provides excellent ohmic contact
- *nitride sealing* of the whole active area to provide maximum environmental protection.

Besides its advanced design, one of the most outstanding features of the BFG65 is its low cost. Current alternatives to the BFG65 can be found only in the range of professional microwave transistors, which cost far more. So with this new transistor, it's possible to make significant reductions in the cost of line extenders and downconverter i.f. stages. And this is a big step in bringing these products into the price range of the consumer market.

NEW PRODUCTION METHODS GIVE EXTRA-FINE GEOMETRY

The die of the BFG65 is manufactured using a modified form of the now familiar planar epitaxial process. In this an n-type epitaxial layer is first formed on an n^+ silicon substrate, after which the (p-type) base and (n-type) emitter regions are formed by ion implantation.

The conventional process involves:

– depositing a first oxide layer on the silicon substrate and opening windows in this layer for implanting the p^+ base-contact fingers (boron)

– removing the oxide layer from between and around the contact fingers and implanting a shallow boron layer to form the p-type base region

– depositing a second oxide layer and opening windows in this layer for implanting the n^+ emitter fingers (arsenic)

– re-opening the base-contact windows in preparation for metallization

– Ti-Pt-Au metallization to produce the base and emitter contacts.

This process needs two masks for producing the base fingers, one for the p^+ implantation, one for the metallization. For accurate base geometry, these masks must be perfectly aligned, a difficult task with the extra-fine geometry (2,5 μm pitch) of the BFG65.

Instead, we use a modified process (Fig.2) in which the p^+ base-contact fingers are implanted after the n^+ emitter fingers. Base-contact implantation then takes place just before metallization, and uses the same window geometry in the oxide layer. So this process needs only one mask to produce the base regions and completely eliminates alignment problems. The result is probably the finest electrode structure available with current manufacturing techniques. And the higher yield, coming from the elimination of one process step, means a drastic reduction in manufacturing costs.

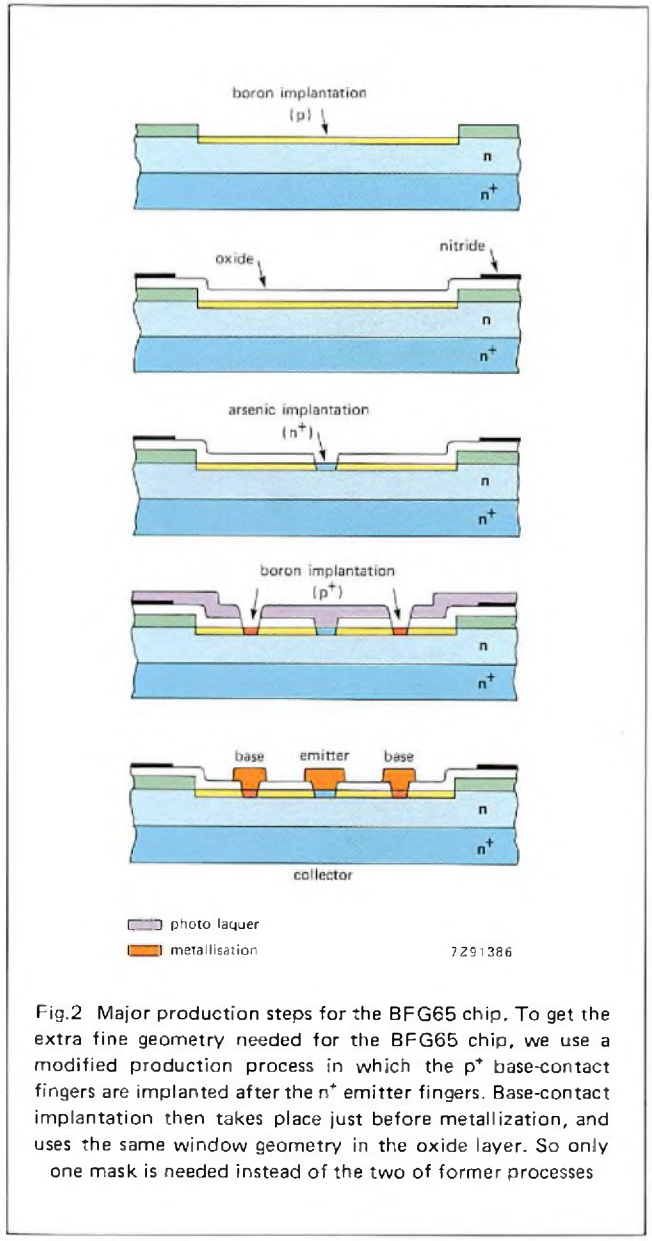


Fig.2 Major production steps for the BFG65 chip. To get the extra fine geometry needed for the BFG65 chip, we use a modified production process in which the p^+ base-contact fingers are implanted after the n^+ emitter fingers. Base-contact implantation then takes place just before metallization, and uses the same window geometry in the oxide layer. So only one mask is needed instead of the two of former processes

WIDEBAND AMPLIFIER WITH THE BFG65

Figure 3 gives the amplifier circuit and Fig.4 gives the print board and component layout. With the high gain of the BFG65 (Table 1), only two amplification stages are needed to produce a power gain greater than 20 dB, and a single series resistor (10 Ω) is all that's needed to match the input of the first stage to the 75 Ω antenna circuit.

To reduce parasitic inductances (which may introduce dispersion effects), chip capacitors are used for input and output coupling.

The collector-emitter voltage of each stage is set at around 7 V, and the emitter current of the second-stage is set at around 15 mA, corresponding to I_E at f_{Tmax}. Since the first stage operates at lower power, its emitter current can be set lower at around 9 mA to minimize noise. The exceptionally low noise of the BFG65 means that, even with a 10 Ω matching resistor, the circuit's noise figure is better than 4 dB.

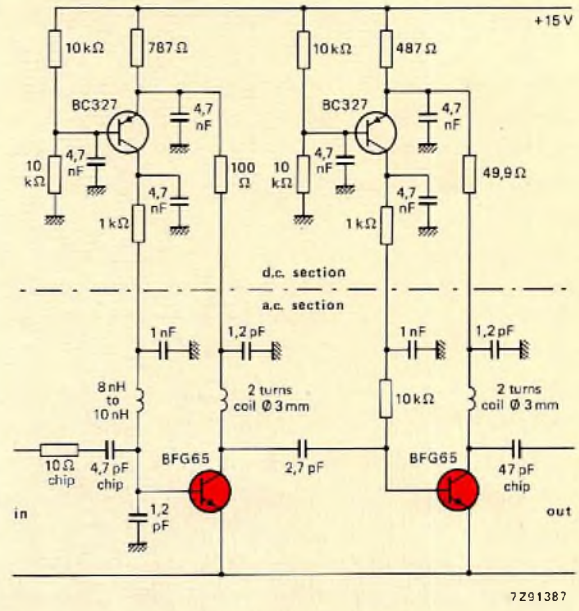


Fig.3 Two-stage wideband amplifier using BFG65 transistors

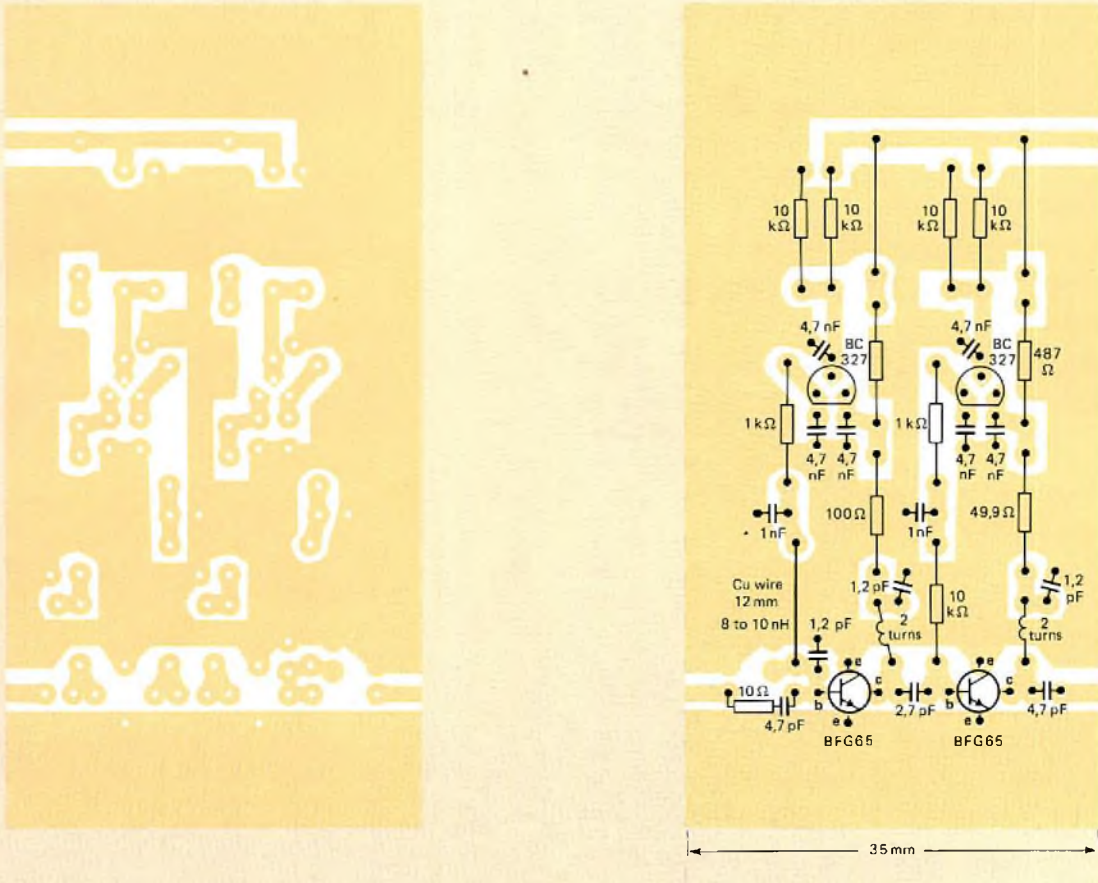


Fig.4 Print board and component layout

AMPLIFIER PERFORMANCE

Table 2 gives a brief performance specification of the amplifier. A better indication of its performance, however, is given in Fig.5, which shows the amplifier's frequency response, as well as its noise figure and return losses as functions of frequency.

TABLE 2
Amplifier performance

frequency range	950 to 1750 MHz
response ripple (over frequency range)	$\leqslant \pm 1$ dB
power gain	$\geqslant 20$ dB
noise figure	$\leqslant 4$ dB
vswr (input and output)	$\leqslant 2{,}0$

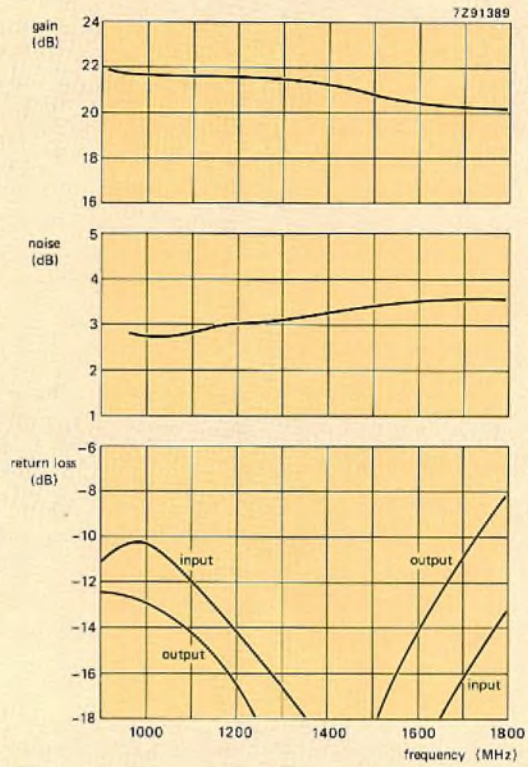


Fig.5 Gain, noise and return losses of a prototype amplifier as functions of frequency

Recent publications

MEA8000 voice synthesizer: principles and interfacing,
Technical Publication 101, 16 pages
(ordering code 9398 041 80011)

The development of speech synthesis techniques has dramatically reduced the bit rate and memory required for digital speech synthesis so that it is now economically feasible to open a wideband voice channel between machine and man. Such a channel is provided by our totally digital integrated voice synthesizer MEA8000. A 4-page leaflet describing the components and editing system supporting the MEA8000 speech synthesizer is also available.
(ordering code 9398 319 40011)

70-90 W hi-fi audio amplifiers with the BDV66 and BDV67,
Technical Publication 113, 8 pages
(ordering code 9398 043 20011)

This publication describes two high-fidelity audio amplifiers using complementary Darlington power transistors BDV66 (pnp) and BDV67 (npn) in the output stage. Features of these transistors are economy, improved SOAR and high reliability.

A low-cost monochrome data and graphics display unit (C6T),
Technical Publication 114, 4 pages
(ordering code 9398 043 30011)

The C6T is a minimum circuitry VDU based on circuit design techniques that have been well-proven by extensive tv usage. It is ideal for alphanumeric and graphic display applications such as computer terminals, small business computers and video games.

A versatile high-resolution monochrome data and graphics display unit (C64),
Technical Publication 115, 6 pages
(ordering code 9398 043 40011)

The C64 is a high resolution VDU which can be adapted to operate over a wide range of line and field frequencies and can operate in either landscape or portrait orientation. It therefore allows many different dedicated display units to be built from one basic design.

EUROM – A display IC for CEPT Videotex, 6 pages
(ordering code 9398 317 90011)

A brochure describing the EUROM IC, an NMOS CRT controller chip that covers all presentation level aspects of the CEPT Videotex standard.

Simple rules for GTO circuit design,
Technical Publication 116, 20 pages
(ordering code 9398 043 50011)

Some of the terms and characteristics in the published data for GTOs may be unfamiliar to those circuit designers who are more accustomed to using transistors and thyristors. This publication describes the characteristics and performance of the GTO and discusses the design of GTO circuits.

Miniature ceramic capacitors, 16 pages
(ordering code 9398 313 90011)

A brochure describing the manufacture and quality control procedures for our flanged miniature ceramic plate capacitors.

Microwave oscillators, 12 pages
(ordering code 9398 315 70011)

A survey of microwave oscillators for high-quality telecommunications, satellite tv, radar beacons, test equipment and electronic guidance systems. Products described range from ultra-stable low-noise cavity-stabilized oscillators in the 11 to 19 GHz band to economy-class X-band devices.

On-line semi custom logic, 20 pages
(ordering code 9398 317 80011)

A brochure describing our semi-custom ICs including CMOS, ACE and ISL gate arrays, IFL programmable arrays and CMOS and TTL cell libraries.

High-speed CMOS, PC54/74 family, 26 pages
(ordering code 9398 317 30011)

A survey of the HCMOS products including performance data and a cross-refererence guide to 54/74 series TTL and 4000 series CMOS circuits.

CATV amplifier modules, 12 pages
(ordering code 9398 311 40011)

A survey of our BGY series of hybrid wideband amplifier modules designed specifically for tv applications.

Microwave transistors, 20 pages
(ordering code 9398 317 70011)

A survey of our bipolar silicon transistors and GaAs FETs for operation at frequencies from 1 GHz to 16 GHz.

Copies of these publications can be ordered from any of the companies whose addresses are listed on the back cover; subscribers in the U.S.A. are requested to address their orders to the Editor, Electronic Components and Applications, Building BA, Philips Elcoma Division, MD 5600 EINDHOVEN, The Netherlands. When ordering, please quote the twelve-digit ordering code number.

Abstracts

Versatile speech/transmission ICs suit all telephone architectures

If a feature phone has modular architecture, it can be tailored to specific customer's requirements. A condition for modularity is the availability of a supply point through which the microcontroller and some peripherals can be powered from the telephone line. A convenient place to provide this is in the transmission circuit. The transmission circuit should also be suitable for use with either pulse dialling or DTMF dialling and should preferably have a power down to minimise its supply current during line current interruptions. All these conditions are fulfilled with the new speech/transmission IC TEA1060/61.

Fault-tolerant software in real-time single-chip microcontroller systems

Techniques that can be used in designing fault-tolerant software for microcontroller-based systems are discussed. As an example, the design of software for a sophisticated PABX telephone exchange junction using MAB8400-series 8-bit microcontrollers is described. Tests under extreme noise conditions show that with conventional software significant unrecoverable errors occur which can be avoided with fault-tolerant software.

Computer-controlled teletext

During the last few years, teletext has firmly established itself in the domestic tv market. A major factor in this rapid expansion has been the proven performance of the first generation of teletext decoders. As the price of the decoder board falls and its features improve, the size of the market is expected to increase still further. This article describes the next generation of decoders which is now available and is known as Computer Controlled Teletext (CCT).

Fast co-processor meets factory's real-time needs

Integrated Computer-Aided Manufacturing (ICAM) calls for a combination of high speed operation, as in communications and data handling, and low speed real-time operation, as in process or robot control. This article describes the use of an 8X305 high-speed microcontroller together with an 8X310 interrupt-driven co-processor to accommodate these differences in operational speed. Examples taken are of multi-axis robot control and of communications control.

FM/IF system and microcomputer-based search tuning interface

We have now packed a complete f.m. i.f. system as well as a microcomputer-controlled search tuning interface onto a single chip. This IC, the TEA6000, is intended for use in digitally-controlled car and hi-fi radios which have a ratio detector for f.m. Manufacturers will benefit from the high replacement value of the new IC, and users will benefit from its highly accurate tuning. The latter is achieved by using a high-resolution frequency counter instead of the usual method of detecting the zero crossing of the f.m. demodulator S-curve. The circuit can be used in conjunction with most available integrated a.m. receivers to construct an all-band radio.

Modifying Teradyne 283 programs to test high-speed CMOS LOGIC ICs

Some high-speed CMOS logic ICs from the PC54/74 family have a type number suffix HCT. Many of these circuits are pin and function compatible with the 54/74 series of LSTTL circuits and have the same input switching levels and supply voltage range. Their main role is replacing LSTTL circuits to reduce power consumption without reducing operating speed. Standard TTL test programs cannot, however, be used to test the CMOS circuits because they have a different input and output structure than LSTTL circuits. This article shows how the TTL test programs for one of the most widely used logic testers, the Teradyne 283, can easily be modified to test high-speed CMOS logic ICs.

Twin-switch power pack for 110° colour TV

The twin-switch power pack (TSPP) is a combined mains-isolated horizontal-deflection circuit and power supply for 110° display systems. The power supply is synchronized with the horizontal scan and can generate all the d.c. supply voltages including the e.h.t. and up to 50 W for the audio amplifiers without distorting the picture. The TSPP uses a new diode-split line output transformer incorporating the focus potentiometer. This transformer, smaller and cheaper than the one in the current 110° synchronous power pack, is also available, with almost identical pinning, for single-switch power packs for raster-correction-free systems. Consequently, one power supply layout can be used for either an r.c.f. or 110° system.

Wideband i.f. amplifier for satellite-tv receiving systems

The new BFG65 wideband transistor has been designed for use in the i.f. amplifier stage of satellite-tv reception systems. The transistor has an extra-fine (2,5 μm) interdigitated electrode structure, and a thin (1 μm) epitaxial layer, giving it high f_T, high gain and low noise. With the BFG65, only two amplification stages are needed to produce an i.f. amplifier with over 20 dB gain, and with a noise figure better than 4 dB.

Aktive Sprechschaltung passt für alle Telefon-Systeme

Komfort-Telefone besitzen einen modularen Aufbau und können Kundenwünschen entsprechend ausgestattet werden. Voraussetzung für die Modul-Technik ist das Vorhandensein eines Speisepunktes, der Mikrocontroller und Peripherie aus dem Linienstrom versorgen kann. Ein solcher Punkt liegt zweckmässigerweise in der Sprechschaltung. Sie sollte ausserdem sowohl für Impuls- als auch für Mehrfrequenz-Wahl geeignet sein und müsste während der Schleifenstromunterbrechungen auf einen Betrieb mit minimaler Stromaufnahme umschaltbar sein (power down mode). Alle diese Bedingungen erfüllt die aktive Sprechschaltung TEA1060/61.

Fehlertolerante Software in Echtzeit-Mikrocontroller-Systemen

Mögliche Methoden für die Entwicklung fehlertoleranter Software werden diskutiert. Als Beispiel wird ein Verfahren für eine komplexe Nebenstellenanlage mit 8 bit-Mikrocontrollern der HAB8400-Serie beschrieben. Tests unter extremen Störbedingungen zeigen, dass konventionelle Software zu nicht korrigierbaren Fehlern führt, die mit fehlertoleranter Software vermieden werden können.

Computer Controlled Teletext

In den vergangenen Jahren hat sich Videotext auf dem hiesigen TV-Markt einen festen Platz erobert. Ein wichtiger Faktor für die schnelle Verbreitung waren und sind dabei die bewährten Leistungsmerkmale der ersten Videotextdecoder-Generation. Da der Preis für die Decoderplatine bei gleichzeitiger Verbesserung der Eigenschaften im Fallen begriffen ist, kann man von einer weiter steigenden Nachfrage auf dem Markt ausgehen. Dieser Beitrag beschreibt die nächste Decoder-Generation, die jetzt verfügbar ist und den Namen "Computer Controlled Teletext" (CCT) trägt.

Schneller Coprozessor erfüllt industrielle Echtzeitanforderungen

Integrierte, computergestützte Fertigung (Integrated Computer-Aided Manufacturing, ICAM), erfordert eine Kombination von Hochgeschwindigkeits-Operationen, z.B. für die Datenverarbeitung und -übertragung, mit langsamen Echtzeit-Operationen, zB. für die Prozess- und Robotersteuerung. Dieser Beitrag beschreibt den Einsatz des schnellen Mikrocontrollers 8X305 in Kombination mit einem interruptgesteuerten Coprozessor 8X310, um derartige Unterschiede in der erforderlichen Arbeitsgeschwindigkeit zu bewältigen. Die ausgewählten Applikationsbeispiele beziehen sich auf mehrachsige Robotersteuerung und Datenübertragungssteuerung.

FM-ZF-System und mikrocomputergesteuertes Suchlauf-Abstimm-interface

In diesem Artikel wird die integrierte Schaltung TEA6000 beschrieben, in der ein vollständiges FM-ZF-System und ein mikrocomputergesteuertes Suchlauf-Abstimminterface auf einem einzigen Silizium-Kristall untergebracht sind. Diese Schaltung is vorgesehen für den Einsatz in Auto- und Hifi-Radios, deren Funktionen digital gesteuert werden. Für die Hersteller von Rundfunkempfängern wird der hohe Ersetzungsgrad der neuen integrierten Schaltung von Nutzen sein, während für den Gerätebenutzer die hohe Abstimmgenauigkeit vorteilhaft ist. Letztere wird erreicht durch den Einsatz eines hochauflösenden Frequenzzählers anstelle der sonst üblichen Methode, der Nulldurchgang der FM-Demodulatorkurve als Abstimmkriterium zu verwenden. Mit der Schaltung TEA6000 lässt sich in Kombination mit den meisten verfügbaren integrierten AM-Empfängerschaltungen ein Allband-Rundfunkempfänger aufbauen.

Modifizierung von Teradyn 283–Programmen zur Prüfung von sehr schnellen CMOS-Logik-ICs

Einige sehr schnelle CMOS-Logik-ICs der PC54/74-Familie haben bei der Typenbezeichnung den Zusatz HCT. Viele dieser Schaltungen sind Pin- und Funktionskompatibel mit der 54/74-Serie der LSTTL-Schaltungen. Sie haben auch die gleiche Eingangsschaltschwelle und den gleichen Versorgungsspannungsbereich. Ihre Hauptaufgabe ist es, LSTTL-Schaltungen zu ersetzen, um die Leistungsaufnahme ohne Herabsetzung der Schaltzeiten zu vermindern. Standard-TTL-Programme können jedoch zum Prüfen der HCMOS-Schaltungen nicht verwendet werden, da sie eine andere Ein- und Ausgangskonfiguration als LSTTL-Schaltungen haben. Dieser Artikel zeigt, wie die TTL-Prüfprogramme für eines der am meisten verwendeten Prüfgeräte, Teradyn 283, so modifiziert werden können, dass die Prüfung sehr schneller CMOS-Schaltungen möglich ist.

Twin-Switch Power Pack für 110° Farbfernsehgeräte und -Monitore

Das TSPP (Twin-Switch Power Pack) ist eine Kombination von netzgetrennter Horizontal-Ablenkschaltung und Versorgungsschaltung für 110°-Bildröhren-Systeme. Die Versorgungsschaltung arbeitet synchron mit der horizontalen Ablenkung und liefert alle Versorgungsgleichspannungen, auch für die Erzeugung der Hochspannung, sowie die Versorgungsleistung für die Tonverstärkung bis 50 W ohne Störbeeinflussung des Bildes. Das TSPP benützt eine neuen Diodensplittransformator für die Horizontalablenkung mit eingebautem Fokuspotentiometer. Der Transformator ist kleiner und preisgünstiger als in synchronen 110°-Versorgungschaltungen übliche Transformatoren. Er kann auch bei weitgehend gleicher Pinbelegung, im SSPP (Single-Switch Power Pack) von rasterkorrekturfreien (r.k.f.) Systemen eingesetzt werden. Folglich kann man das gleiche Layout sowohl für r.k.f.-Systeme als auch für 110°-Ablenksysteme verwenden.

Breitband-ZF-Verstärker für Satelliten-FS-Empfangssysteme

Die neue Breitband-Transistor BFG65 ist für ZF-Verstärkerstufen von Satelliten-FS-Empfangssystemen entwickelt worden. Der Transistor ist mit einer sehr feinen (2,5 μm) interdigitalen Elektrodenstruktur sowie einer dünnen (1 μm) Epitaxialschicht ausgestattet. Diese ermöglichen eine hohe Transitfrequenz f_T, hohe Verstärkung und ein günstiges Rauschverhalten. Zum Aufbau eines ZF-Verstärkers mit mehr als 20 dB Verstärkung und einem niedrigeren Rauschmass als 4 dB werden nur zwei Stufen mit dem neuen Transistor BFG65 benötigt.

Des circuits intégrés pour la transmission téléphonique adaptables à toutes les architectures

Un poste téléphonique doté d'une architecture modulaire, peut être adapté aux impératifs particuliers du client. Une des conditions de la modularité est la nécessité de disposer d'une source d'alimentation auxiliaire dans le circuit de transmission afin d'alimenter les circuits périphériques. Ce circuit de transmission doit également être prévu pour un usage dans un système utilisant la numérotation soit décimale, soit DTMF, et donc posséder un mode d'attente caractérisé par une basse consommation pour supporter les interruption du courant de ligne. Toutes ces conditions se trouvent réunies avec le nouveau circuit intégré de transmission TEA1060/61.

Un logiciel tolérant l'erreur pour les circuits intégrés microcontrôleurs à puce unique, fonctionnant en temps réel

L'article présente les techniques applicables à la conception d'un logiciel tolérant les erreurs pour les systèmes à base de microcontrôleur. L'exemple donné décrit la conception d'un logiciel pour une liaison de central téléphonique PABX sophistiqué utilisant des microcontrôleurs à 8 bits de la famille MAB8400. Des essais menés dans des conditions de bruit extrême montrent qu'avec le logiciel classique, d'importantes erreurs irrécupérables se produisent, qui pourraient être évitées avec un logiciel tolérant l'erreur.

Télétexte commandé par ordinateur

Ces dernières années, le télétexte s'est fermement implanté dans le marché de la télévision grand public. L'un des principaux facteurs de cette expansion rapide réside dans l'amélioration prouvée du rendement des décodeurs télétexte de la première génération. A mesure que le prix du décodeur diminue et que ses possibilités augmentent, on s'attend à ce que le marché poursuive encore sa croissance. Cet article décrit la prochaine génération de décodeur qui est d'ores et déjà disponible, sous le nom de Télétexte Commandé par Ordinateur (Computer Controlled Teletext = CCT).

Un co-processeur rapide satisfait les impératifs de temps réel des usines

La Fabrication Assistée par Ordinateur Intégré (Integrated Computer-Aided Manufacturing = ICAM) exige que soient combinés le fonctionnement à grande vitesse, comme dans les communications et le traitements des données, et le fonctionnement en temps réel à faible vitesse, comme dans la commande des processus ou par robot. Cet article décrit l'utilisation d'un micro-contrôleur à grande vitesse 8X305 en conjonction avec un co-processeur régi par interruptions 8X310, afin de pallier cette différence de vitesses de fonctionnement. Les exemples cités concernent à la commande de robot sur plusieurs axes et la commande des communications.

Système FM/FI interface d'accord commandée par microcontrôleur

Nous avons réuni sur un seul cristal un système FM/FI complet ainsi qu'une interface d'accord commandée par microcontrôleur. Ce circuit intégré appelé TEA6000, est destiné aux autoradios à commande numérique et aux récepteurs radio haute fidélité, équipés d'un détecteur de rapport pour la F.M. Les fabricants bénéficieront de la grande valeur de remplacement du nouveau circuit intégré, et les utilisateurs de son accord extrêmement précis. Celui-ci est obtenu en utilisant un compteur de fréquence à grand pouvoir séparateur, au lieu de la méthode habituelle consistant à détecter le recoupement zéro de la courbe S du démodulateur F.M. Le circuit peut être associé à la plupart des circuits récepteurs à modulation d'amplitude existants, pour réaliser un récepteur radio toutes bandes.

Modification des programmes Teradyne 283 pour le test des circuits intégrés logiques CMOS à grande vitesse

Certains circuits intégrés logiques CMOS à grande vitesse de la famille PC54/74 ont le suffixe HCT dans leur numéro de type. Un grand nombre de ces circuits sont compatibles, du point de vue brochage et fonctions, avec la série 54/74 des circuits TTL/LS; ils présentent en outre les mêmes niveaux de commutation d'entrée et les mêmes gammes de tension d'alimentation. Ils sont destinés à remplacer les circuits TTL/LS afin de réduire la consommation de courant, sans diminuer la vitesse de fonctionnement. Cependant, les programmes de test de la TTL standard ne peuvent pas être appliqués aux circuits CMOS, car la structure d'entrée et de sortie des circuits CMOS diffère de celle des circuits TTL/LS. L'article montre

comment les programmes d'essai TTL pour l'un des matériels de test logiques les plus couramment utilisés, Teradyne 283, peuvent aisément être modifiés pour permettre l'essai des circuits intégrés logiques CMOS à grande vitesse.

Unité d'alimentation à commutation double pour moniteurs et récepteurs de télévision couleur à tube de 110°

L'unité d'alimentation à commutateur double (Twin-Switch Power Pack = "TSPP") comporte un bloc d'alimentation et un circuit combiné de déviation horizontale isolée du secteur, pour les tubes-image 110°. L'alimentation est synchronisée avec le balayage horizontal et fournit toutes les tensions d'alimentation en courant continu, y compris la très haute tension, et l'alimentation des amplificateurs audio fréquences, jusqu'à 50 W, sans perturber l'image. L'unité "TSPP" utilise un transformateur de sortie de lignes à division par diode, d'un nouveau genre, auquel est incorporé le potentiomètre de focalisation. Plus petit et meilleur marché que celui que l'on trouve couramment dans les unités d'alimentation synchrone 110°, ce transformateur est également disponible – avec un brochage pratiquement identique – pour les unités d'alimentation à commutation simple destinées au système d'analyse totale d'image sans correction. Par conséquent, cet agencement d'alimentation peut être utilisé aussi bien pour un système d'analyse totale d'images sans correction que pour un système 110°.

Amplificateur à fréquence intermédiaire en bande large, pour les systèmes récepteurs de télévision par satellite

Le nouveau transistor à bande large BFG65 a été conçu pour l'utilisation dans l'étage d'amplification de fréquence intermédiaire des systèmes récepteurs de télévision par satellite. Ce transistor possède une structure d'électrodes interdigitées extrêmemet fines (2,5 μm), et une mince couche épitaxiale (1 μm), procurant une valeur f_T élevée, un grand gain et un faible bruit. Avec le BFG65, il suffit de deux étages d'amplification pour produire un amplificateur de fréquence intermédiaire, avec un gain de plus de 20 dB et un facteur de bruit meilleur que 4 dB.

Circuitos integrados de voz/transmisión adecuados a todas las arquitecturas telefónicas

Si un equipo telefónico tiene arquitectura modular, puede confeccionarse según los requisitos específicos del cliente. Una condición para la modularidad es la disponibilidad de un punto de alimentación a través del cual el microcontrolador y algunos periféricos pueden alimentarse a partir de la línea telefónica. Un lugar conveniente para este punto es en el circuito de transmisión. La transmisión también puede ser adecuada para utilizarla tanto con discado de impulsos como discado DTMF, y sería preferible tener un modo bajo de potencia para minimizar su corriente de alimentación durante las interrupciones de la corriente de línea. Todas estas condiciones se cumplen con el circuito integrado de voz/transmisión TEA1060/61.

Software tolerante a fallos en sistemas de microcontrolador monochip de tiempo real

Se explican las técnicas que se pueden utilizar en el diseño de software tolerante a fallos para sistemas basados en microcontrolador. Como ejemplo se describe el diseño de software para una sofisticada central telefónica PABX que se usa con microcontroladores de 8 bits de la serie MAB8400. Las pruebas bajo condiciones extremas de ruido muestran que con software convecional se presentan importantes errores no recuperables, los cuales se pueden evitar con software tolerante a errores.

Teletexto controlado por ordenador

Durante los últimos años, el teletexto se ha establecido firmemente en el mercado de la TV doméstica. Un factor importante en esta rápida expansión han sido las prestaciones resultantes de la primera generación de decodificadores de teletexto. Como el precio de la placa decodificadora baja y sus características mejoran, se espera que el tamaño del mercado aumente aún más. Este artículo describe la próxima generación de decodificadores que está disponible ahora y que se conoce como teletexto controlado por ordenador (CCT, Computer-Controlled Teletext).

Co-procesador rápido que cumple las necesidades de tiempo real de las factorías

La fabricación ayudada por ordenador integrada necesita una combinación de funcionamiento a alta velocidad, como en comunicaciones y manejo de datos, y de funcionamiento en tiempo real de baja velocidad, como en control de procesos o robot. Este artículo describe el uso de un micro-controlador de alta velocidad, 8X305, junto con un co-procesador de excitación interrumpida, 8X310, para acomodar estas diferencias en velocidad operacional. Los ejemplos tomados son de control de robot multi-eje y control de comunicaciones.

Sistema FM/FI y acoplamiento para sintonía por ordenador

Recientemente hemos encapsulado en un chip un sistema FM/FI completo así como un acoplamiento para búsqueda de sintonía controlada por microordenador. Este circuito integrado, TEA6000, está diseñado para utilizarlo en radios de Hi-Fi y auto-radios controladas digitalmente, las cuales tienen un detector de relación para que los fabricantes de sistemas de FM se beneficien del alto valor de sustitución del nuevo circuito integrado, y los usuarios se beneficien de su sintonía altamente precisa. Esto último se consigue utilizando un contador de frecuencia de alta resolución en lugar del método usual de detectar el cruce por cero de la curva S del demodulador de F.M. Este circuito se puede utilizar junto con la mayoría de receptores A.M. integrados disponibles para construir una radio toda banda.

Modificacion de los programas del Teradyne 283 para probar circuitos integrados lógicos CMOS de alta velocidad

Algunos circuitos integrados lógicos CMOS de alta velocidad de la familia PC54/74 tienen un sufijo HCT en el número de tipo. Estos circuitos son compatibles, tanto en terminales como funcionalmente, con la serie 54/74 de circuitos LSTTL y tienen los mismos niveles de conmutación de entrada y margen de tensión de alimentación. Su principal papel consiste en reemplazar circuitos LSTTL para reducir el consumo de potencia sin reducir la velocidad de funcionamiento. Sin embargo, los programas de prueba TTL estándar no se pueden utilizar para probar los circuitos CMOS debido a que tienen una estructura de entrada y salida diferente de los circuitos LSTTL. Este artículo muestra cómo se pueden modificar fácilmente los programas de prueba TTL para uno de los comprobadores lógicos más ampliamente utilizados, el Teradyne 283, con el fin de probar circuitos integrados lógicos CMOS de alta velocidad.

Sistema compacto de potencia de conmutacion doble para monitores y receptores de TVC de 110°

El sistema compacto de potencia de conmutación doble (TSPP, Twin-Switch Power Pack) es una combinación de fuente de alimentación y circuitos de desviación horizontal aislados de red para sistemas de visualización de 110°. La fuente de alimentación está sincronizada con el barrido horizontal y puede generar todas las tensiones continuas de alimentación incluyendo la tensión de M.A.T. y hasta 50 W para los amplificadores de audio sin distorsionar la imagen. La TSPP utiliza un nuevo transformador de salida de líneas de diodos divididos, el cual incorpora el potenciómetro de foco. Este transformador, más pequeño y barato que el del usual sistema compacto de potencia síncrono de 110°, está disponible también, con casi idéntica configuración de terminales para sistemas compactos de potencia de conmutación sencilla para sistemas sin corrección de trama. Consecuentemente, se puede utilizar un circuito de alimentación para cada R.C.F. o sistema de 110°.

Amplificadir de F.I. de banda ancha para sistemas de recepcion de TV por satélite

El nuevo transistor de banda ancha BFG65 ha sido diseñado para ser utilizado en la etapa amplificadora de F.I. de sistemas de recepción de TV por satélite. El transistor tiena una estructura de electrodos interdigital extrafino (2,5 μm), y una capa epitaxial delgada (1 μm), lo que le da un alto f_T, alta ganancia y bajo ruido. Con el BFG65 sólo se necesitan dos etapas amplificadoras para realizar un amplicador de F.I. con una frecuencia por encima de 20 dB con un factor de ruido mejor que 4 dB.

Authors

Jan Exalto, born at Eindhoven in 1942, graduated from Eindhoven Polytechnic in 1964. After military service he joined the Central Applications Laboratory of Philips Electronic Components and Materials Division in 1966. Since then he has been principally engaged in digital electronics and is at present responsible for applications of standard and customized CMOS.

Arnold Garskamp was born in Rotterdam, The Netherlands in 1936 and graduated in electrical and radio engineering in 1967. After military service, he joined the Central Application Laboratory of Philips Electronic Components and Materials Divison where he was involved in the application of semiconductors in radio and audio circuits. For the past eight years, he has concentrated on design techniques for radio circuits intended for subsequent integration.

Chris Bergmans joined the Central Application Laboratory of Philips Electronic Components and Materials Division in 1966. He has worked on a variety of projects including hardware process controllers and control systems for arc welding equipment. For the last nine years, he has been a member of the Deflection and Supply Group for colour tv receivers.

Helmut Kern was born in 1949 in Ludwisburg and graduated as Dipl. Ing. from the Technical University of Stuttgart in 1975. He joined Signetics G.m.b.H. in 1977 as Product Engineer for Logic Integrated Circuits and later became supervisor of that group. After the takeover of Signetics G.m.b.H. by the newly founded SES Electronics Vertriebs G.m.b.H. he transferred to the Distribution Department as technical adviser for components, systems and testers.

J. W. Beunders, born at Wassenaar, The Netherlands, in 1949, studied electronics at The Hague. Immediately after his graduation in 1974 he joined Philips Electronic Components and Materials Division as a member of the radio and telecommunications group. He is currently engaged in development of digital control and display systems for radio and audio equipment.

John Kinghorn, received his degree in electronics from the University of Sussex in 1971. He then joined the Mullard Application Laboratory, working initially on switched-mode power supplies and digital systems. Since 1973 he has been involved in the development of text systems and is currently project leader for teletext.

N. Q. Burnham was born in Caterham, Surrey in 1935. He studied telecommunications and electronic engineering at South London College. After periods with Short Brothers and Harland and ICT, he joined MEL at Crawley where he worked on the development of circuit modules. He later moved to Mullard Mitcham where he served as Product Engineer for ferrite memory core systems. He is currently Field Application Engineer, IC Division, Mullard House.

P. Moors was born in Grave, the Netherlands, in 1935 and graduated in electrical engineering from 's Hertogenbosch Polytechnic, in 1957. The same year, he joined Philips Electronic Components and Materials Division, Nijmegen, and since 1972, he has headed the development group for high-frequency transistors for MATV, CATV, tuners and transmitters.

Jonees K. Chay, born in Seoul, Korea, in 1955, graduated in electrical engineering at Pennsylvania State University. After working for Intel Corporation, where he was engaged in microprocessor marketing, he joined Signetics where he is now applications manager for standard bipolar LSI products. For the past several years he has been active in factory automation applications, including robotics, LANs, CAD/CAM graphics, and DSP.

Peter J. M. Sijbers joined Philips Electronic Components and Materials Division after graduating in electronic engineering at the Venlo Polytechnic. As a member of the Central Application Laboratory he has worked on television tuners and i.f. integrated circuits and is now concerned with the design and application of ICs for telephone equipment.

C. F. Cowling was born in Coventry in 1943. He began his career in telecommunications with the British Post Office in 1960, and studied at Coventry Technical College. Since 1966, he has spent much of his time in the development of PABX (Private Automatic Branch Exchange) equipment, initially with GEC, and from 1970 onward with TMC Ltd (formerly Pye TMC Ltd.). He is at present principal engineer responsible for the Quality Assurance of delivered software.

T. H. Uittenbogaard was born in Wageningen, the Netherlands, in 1942. He joined Philips Electronic Components and Materials Division in 1961, initially working in the quality laboratory, electron tubes, and from 1963, at the u.h.f. tubes laboratory. Since 1965 he has been a member of the tv tuner group of the application laboratory at Nijmegen.

Philips Electronic Components & Materials

Elcoma - Philips Electronic Components and Materials Division - embraces a world-wide group of companies operating under the following names:

IBRAPE **PHILIPS**
MBLE RTC
Miniwatt signetics
Mullard VALVO

Elcoma offers you a technological partnership in developing your systems to the full. A partnership to which we can bring

- *world-wide production and marketing*
- *know-how*
- *systems approach*
- *continuity*
- *broad product line*
- *fundamental research*
- *leading technologies*
- *applications support*
- *quality*

DISPLAY SYSTEMS

B & W tv display systems
Colour tv display systems
Data graphic display systems

INTEGRATED CIRCUITS

Bipolar analogue
Consumer circuits
- *video & radio/audio circuits*

Industrial circuits
- *opamps* • *voltage regulators*
- *comparators* • *D/A & A/D converters*
- *amplifiers* • *interface circuits*

Bipolar digital
Standard logic families
- *TTL/STTL* • *ECL 10K/100K*

LSI circuits
- *gate arrays* • *interface circuits*

8-bit Microprocessors

Memories
- *RAMs/PROMs* • *Fuse logic*

NMOS
8 and 16-bit Microprocessors & peripherals

Logic systems
- *video & radio/audio circuits*
- *text decoders*

ROM memories

CMOS
Standard logic families

LSI circuits
- *gate arrays* • *clock circuits*

8-bit Microprocessors

Hybrid integrated circuits
LF, VHF, UHF & microwave circuits
D/A converters
Proximity switches
Custom-designed circuits

ELECTRO-OPTICAL DEVICES

Image intensifier devices
Infra-red image detectors
Camera tubes
Imaging devices

SEMICONDUCTORS

Small-signal diodes
Medium and high-power diodes
Controlled rectifiers
LF & HF small-signal transistors
LF & HF power transistors
Microwave semiconductors
Opto-electronic semiconductors
Semiconductors for hybrid ICs
Semiconductor sensors

PROFESSIONAL TUBES

Industrial cathode-ray tubes
Photomultiplier tubes
Geiger Müller tubes
Transmitting tubes
Microwave devices
Reed switches

MATERIALS

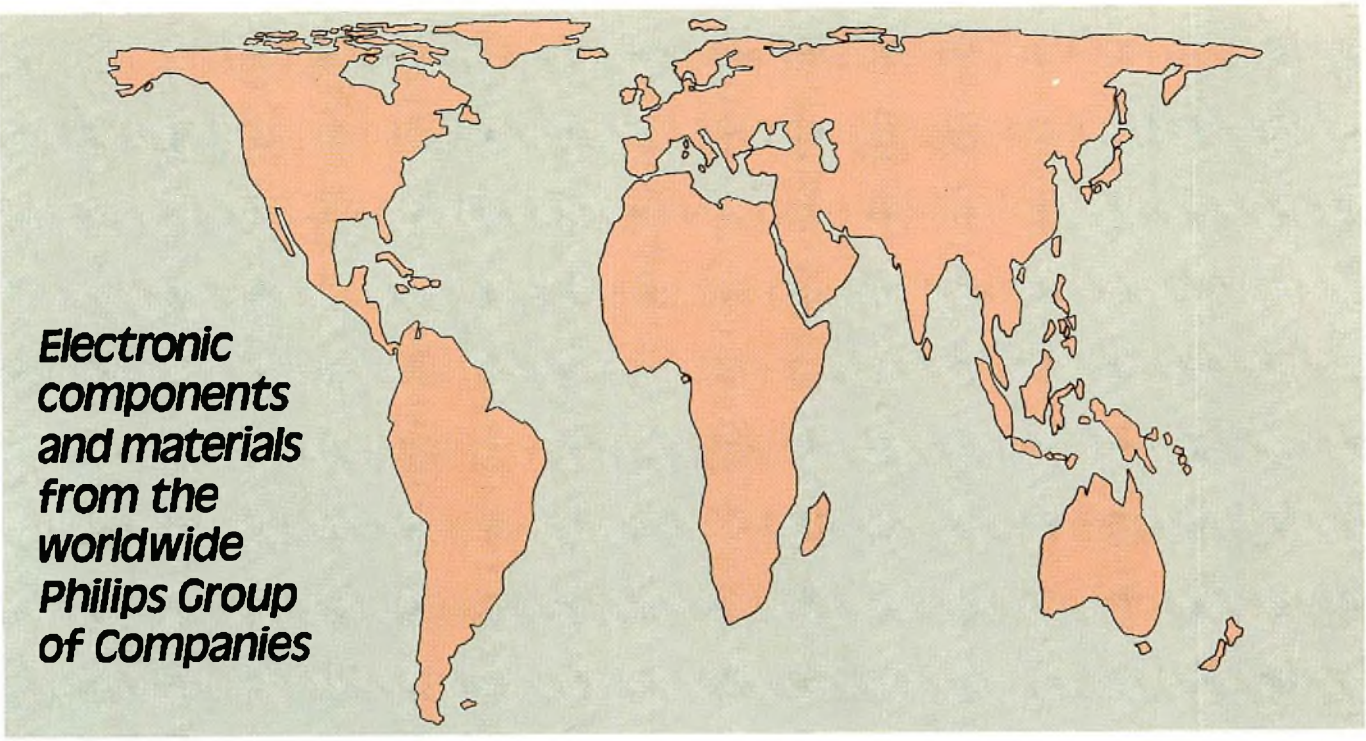
Ferroxcube products
Permanent magnets
Piezoelectric products
White ceramic products

PASSIVE COMPONENTS

Ceramic, film and foil capacitors
Electrolytic capacitors
Fixed resistors
Variable capacitors
Potentiometers and resistor trimmers
Non-linear resistors
Delay lines
Piezoelectric quartz devices

ASSEMBLIES

Electric motors
Loudspeakers
Tuners
Printed circuit boards
Variable transformers
Thumbwheel switches
Industrial microcomputer systems
Microwave sub-assemblies



Electronic components and materials from the worldwide Philips Group of Companies

Argentina: PHILIPS ARGENTINA S.A., Div. Elcoma, Vedia 3892, 1430 BUENOS AIRES, Tel. 541-7141/7242/7343/7444/7545.
Australia: PHILIPS INDUSTRIES HOLDINGS LTD., Elcoma Division, 67 Mars Road, LANE COVE, 2066, N.S.W., Tel. 4270888.
Austria: ÖSTERREICHISCHE PHILIPS BAUELEMENTE Industrie G.m.b.H., Triester Str. 64, A-1101 WIEN, Tel. 62911.
Belgium: N.V. PHILIPS & MBLE ASSOCIATED, 9 rue du Pavillon, B-1030 BRUXELLES, Tel. (02) 2427400.
Brazil: IBRAPE, Caixa Postal 7383, Av. Brigadeiro Faria Lima, 1735 SAO PAULO, SP, Tel. (011) 211-2600.
Canada: PHILIPS ELECTRONICS LTD., Electron Devices Div., 601 Milner Ave., SCARBOROUGH, Ontario, M1B 1M8. Tel. 292-5161.
Chile: PHILIPS CHILENA S.A., Av. Santa Maria 0760, SANTIAGO, Tel. 39-4001.
Colombia: SADAPE S.A., P.O. Box 9805, Calle 13, No.51 + 39, BOGOTA D.E. 1., Tel. 600600.
Denmark: MINIWATT A/S, Strandlodsvej 2, P.O. Box 1919, DK 2300 COPENHAGEN S, Tel. (01) 541133.
Finland: OY PHILIPS AB, Elcoma Division, Kaivokatu 8, SF-00100 HELSINKI 10, Tel. 17271.
France: R.T.C. LA RADIOTECHNIQUE-COMPELEC, 130 Avenue Ledru Rollin, F-75540 PARIS 11, Tel. 355-44-99.
Germany: VALVO, UB Bauelemente der Philips G.m.b.H., Valvo Haus, Burchardstrasse 19, D-2 HAMBURG 1, Tel. (040) 3296-0.
Greece: PHILIPS S.A. HELLENIQUE, Elcoma Division, 52, Av. Syngrou, ATHENS, Tel. 9215111.
Hong Kong: PHILIPS HONG KONG LTD., Elcoma Div., 15/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, Tel. (0)-245121.
India: PEICO ELECTRONICS & ELECTRICALS LTD., Elcoma Div., Ramon House, 169 Backbay Reclamation, BOMBAY 400020, Tel. 221012.
Indonesia: P.T. PHILIPS-RALIN ELECTRONICS, Elcoma Div., Panim Bank Building, 2nd Fl., Jl. Jend. Sudirman, P.O. Box 223, JAKARTA, Tel. 716131.
Ireland: PHILIPS ELECTRICAL (IRELAND) LTD., Newstead, Clonskeagh, DUBLIN 14, Tel. 693355.
Italy: PHILIPS S.p.A., Sezione Elcoma, Piazza IV Novembre 3, I-20124 MILANO, Tel. 2-6752.1
Japan: NIHON PHILIPS CORP., Shuwa Shinagawa Bldg., 26-33 Takanawa 3-chome, Minato-ku, TOKYO (108), Tel. 448-5611.
(IC Products) SIGNETICS JAPAN LTD., 8-7 Sanbancho Chiyoda-ku, TOKYO 102, Tel. (03) 230-1521.
Korea: PHILIPS ELECTRONICS (KOREA) LTD., Elcoma Div., Philips House, 260-199 Itaewon-dong, Yongsan-ku, C.P.O. Box 3680, SEOUL, Tel. 794-4202.
Malaysia: PHILIPS MALAYSIA SDN. BERHAD, No. 4 Persiaran Barat, Petaling Jaya, P.O.B. 2163, KUALA LUMPUR, Selangor, Tel. 774411.
Mexico: ELECTRONICA, S.A de C.V., Carr. Mexico-Toluca km. 62.5, TOLUCA, Edo. de Mexico 50140, Tel. Toluca 91 (721) 613-00
Netherlands: PHILIPS NEDERLAND, Marktgroep Elonco, Postbus 90050, 5600 PB EINDHOVEN, Tel. (040) 793333.
New Zealand: PHILIPS ELECTRICAL IND. LTD., Elcoma Division, 110 Mt. Eden Road, C.P.O. Box 1041, AUCKLAND, Tel. 605-914.
Norway: NORSK A/S PHILIPS, Electronica Dept., Sandstuveien 70, OSLO 6, Tel. 680200.
Peru: CADESA, Av. Alfonso Ugarte 1268, LIMA 5, Tel. 326070.
Philippines: PHILIPS INDUSTRIAL DEV. INC., 2246 Pasong Tamo, P.O. Box 911, Makati Comm. Centre, MAKATI-RIZAL 3116, Tel. 86-89-51 to 59.
Portugal: PHILIPS PORTUGESA S.A.R.L., Av. Eng. Duarte Pacheco 6, 1009 LISBOA Codex, Tel. 683121.
Singapore: PHILIPS PROJECT DEV. (Singapore) PTE LTD., Elcoma Div., Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. 2538811.
South Africa: EDAC (Pty.) Ltd., 3rd Floor Rainer House, Upper Railway Rd. & Ove St., New Doornfontein, JOHANNESBURG 2001, Tel. 614-2362/9.
Spain: MINIWATT S.A., Balmes 22, BARCELONA 7, Tel. 3016312.
Sweden: PHILIPS KOMPONENTER A.B., Lidingövägen 50, S-11584 STOCKHOLM 27, Tel. 08/7821000.
Switzerland: PHILIPS A.G., Elcoma Dept., Allmendstrasse 140-142, CH-8027 ZÜRICH, Tel. 01-4882211.
Taiwan: PHILIPS TAIWAN LTD., 3rd Fl., San Min Building, 57-1, Chung Shan N. Rd, Section 2, P.O. Box 22978, TAIPEI, Tel. (02)-5631717.
Thailand: PHILIPS ELECTRICAL CO. OF THAILAND LTD., 283 Silom Road, P.O. Box 961, BANGKOK, Tel. 233-6330-9.
Turkey: TÜRK PHILIPS TICARET A.S., EMET Department, Inonu Cad. No. 78-80, ISTANBUL, Tel. 435910.
United Kingdom: MULLARD LTD., Mullard House, Torrington Place, LONDON WC1E 7HD, Tel. 01-5806633.
United States: (Active Devices & Materials) AMPEREX SALES CORP., Providence Pike, SLATERSVILLE, R.I. 02876, Tel. (401) 762-9000.
(Passive Devices) MEPCO/ELECTRA INC., Columbia Rd., MORRISTOWN, N.J. 07960, Tel. (201) 539-2000.
(Passive Devices & Electromechanical Devices) CENTRALAB INC., 5855 N. Glen Park Rd., MILWAUKEE, WI 53201, Tel. (414)228-7380.
(IC Products) SIGNETICS CORPORATION, 811 East Arques Avenue, SUNNYVALE, California 94086, Tel. (408) 739-7700.
Uruguay: LUZILECTRON S.A., Avda Uruguay 1287, P.O. Box 907, MONTEVIDEO, Tel. 914321.
Venezuela: IND. VENEZOLANAS PHILIPS S.A., Elcoma Dept., A. Ppal de los Ruices, Edif. Centro Colgate, CARACAS, Tel. 360511

For all other countries apply to: Philips Electronic Components and Materials Division, International Business Relations, Building BAE-3, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Tel. +31 40 72 33 04, Telex 35000 phtc nl/nl be vec.

A37

Printed in The Netherlands

9398 704 00011