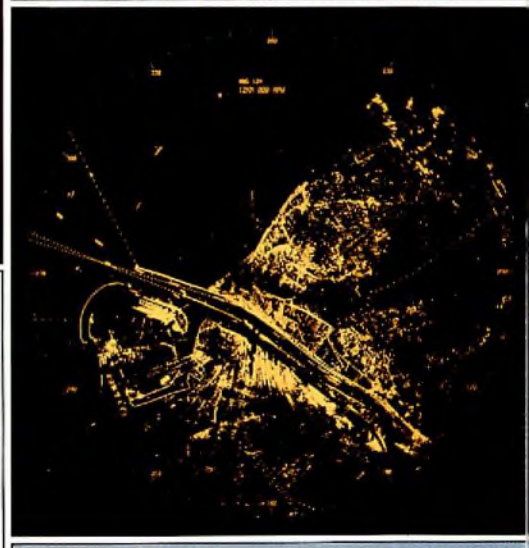
Electronic components & applications

Vol. 5, No 4
September 1983



ISSN 0141 – 6219

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Most important gateway to continental Europe, Rotterdam handles well over 30 000 ships a year – and with a safety record second to none. Nevertheless, the Vessel Traffic Management System which helps maintain this safety record is to be renewed. Work has already started on a new Traffic Centre, three of which will manage a new 26 station shore-based radar chain due for completion in 1986. Such very advanced projects, that must watch over the safety of ships and men and must protect the environment from many hazardous cargoes, call for reliability standards analogous to those of the aerospace industry. As major electronic component supplier, Elcoma has a proud record in meeting such standards.

Contents

Cobalt rare-earth high energy permanent magnets

N. A. ANDERSON

Rare-earth cobalt is the cheapest of the super-performance permanent-magnet materials currently available. Its very high stored energy, combined with high coercivity and low temperature coefficient, results in permanent magnets with the small size and high performance needed to complement the increasing miniaturisation of electronic components.

Since their introduction some 15 years ago, rare-earth cobalt materials have opened new applications for permanent magnets, solving problems for which older materials proved unsuitable. Moreover, their unique characteristics have altered the design of many traditional transducers, reducing volume and increasing efficiency. The high coercivity of these materials allows for very short magnetic lengths, whereas their high remanence often makes the use of mild-steel pole pieces for flux concentration unnecessary.

COMPOSITION AND MANUFACTURE

Rare-earth cobalt materials now available under the designation RES are intermetallic compounds of cobalt and the rare-earth element samarium. Three versions are currently available: RES 160, RES 190 and RES 220. RES magnets are made by pressing and sintering, a process similar to that used for Ferroxdure hard ferrites.

A powder of the alloy is first compacted in a die. At this stage, the magnetic properties in the final magnetising direction are enhanced by aligning the material particles by means of an external magnetic field. The compacts are then sintered in a controlled-atmosphere furnace. After sintering, the magnets are heat-treated to optimise their properties.

During sintering, RES magnets shrink. The amount of shrinkage depends on, amongst other things, their size and shape. Some variation in dimensions results, so, for close tolerances, important surfaces are ground.

TABLE 1
Principal properties of RES rare-earth cobalt permanent magnet materials (typical values)

property	symbol	RES160	RES190	RES220*	unit
remanence	B_r	810	890	950	mT
coercivity	H_{cB}	600	670	710	kA/m
polarization coercivity	H_{cJ}	>1100	>1100	>1100	kA/m
maximum BH product	$(BH)_{max}$	128	154	176	kJ/m³

* only for certain shapes.

PROPERTIES

Magnetic characteristics

The B-H characteristics of all grades of RES materials are substantially linear in the second quadrant of the hysteresis loop, as shown in Fig.1. This property, combined with a recoil permeability of around 1.05 and very high polarisation coercivities, makes for stable operation and gives the designer considerable freedom.

RES 160, RES 190 and RES 220 differ only in their guaranteed B_r and $(BH)_{max}$ values.

Effect of temperature

The principal effect of increasing temperature on the performance of RES is a decrease of useful flux at the working point. Depending on the thermal history of the magnet, the loss may be reversible or irreversible.

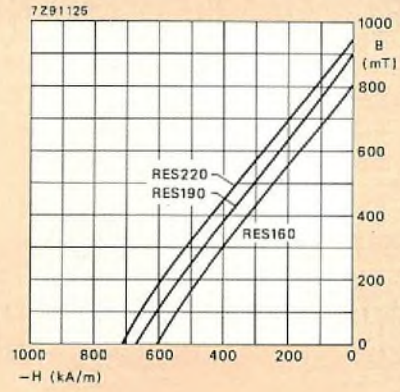


Fig.1 Second (demagnetising) quadrant of the hysteresis loops of RES rare-earth cobalt permanent magnet materials

Reversible losses, caused by the effect of temperature on the saturation polarisation, are expressed in terms of the temperature coefficient of remanence which, for RES magnets, is very much lower than for hard ferrites. In fact, as Table 2 shows, the thermal stability of RES materials, <0.1%/K, approaches that of Ticonal alloys; it can be further improved by suitable treatment.

Irreversible losses can be divided into those that are recoverable by remagnetisation and those that are not; however, this distinction is usually academic, since remagnetisation is rarely practicable.

TABLE 2
Temperature coefficient of remanence for various permanent magnet materials

material	temperature coefficient of remanence (%/K)
Ferroxdure hard ferrites	−0.2
Ticonal alloys	−0.02
RES materials	−0.05

Irreversible losses that are recoverable by remagnetisation are caused by elemental parts of the magnet becoming demagnetised by thermal agitation. The extent to which this occurs depends upon the magnetic working point (the demagnetising field strength), the time elapsed, and the temperature, so the data given for the material relates to losses at a specified working point. The lower the working point (that is, the higher the demagnetising field), the higher the loss. This loss also increases with temperature. The effect of time is logarithmic: the majority of the loss occurs in the first four hours after magnetisation. The loss quoted is a maximum, extrapolated to infinity. Irreversible losses that cannot be recovered by remagnetisation are caused by metallurgical changes within the magnet (such as oxidation). Improvements in production technology have reduced that problem significantly for normal working conditions. The maximum recommended operating temperature should, however, not be exceeded.

The superior temperature stability needed in some applications can be obtained by ageing the magnets (at the relevant working point) for several hours at a temperature slightly higher than the expected maximum operating temperature.

Magnetising requirements

The high coercivity of RES materials is due both to the difficult nucleation of reverse domains and the pinning of domain walls at grain boundaries. Following the final manufacturing heat treatment the material is composed of many densely packed grains, each containing several magnetic domains. (A domain can be considered as being composed of a group of atoms whose magnetic moments are oriented in the same direction.) In this unmagnetised state the domains will be oriented with respect to each other so that the magnetic energy in the material is minimised.

When an external field is applied, domains which are oriented in the direction of the field become enlarged at the expense of domains oriented in other directions. The growth of these domains by the realignment of neighbouring atomic moments is relatively easy within the grains. The growth of favourably oriented domains results in a net magnetisation which approaches the maximum level at quite low applied fields, Fig.2.

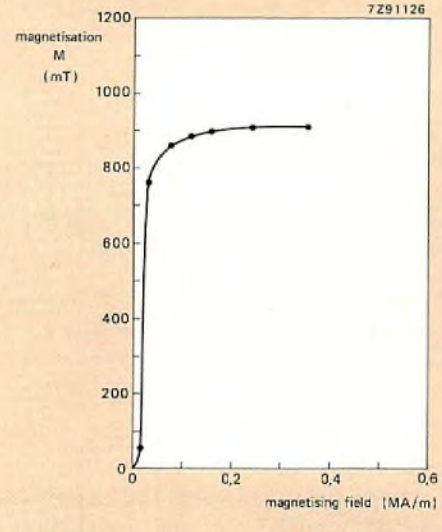


Fig.2 Initial magnetisation curve for a thermally-demagnetised RES 190 magnet. The magnetisation increases rapidly to saturation at fairly low applied field strengths

However, if the applied field is now reversed there is also little resistance to the reduction in size of the previously enlarged domain and the magnet is easily demagnetised. Thus, the coercivity developed by this mechanism is not large.

If the initial applied field is increased beyond the comparatively low levels necessary to approach maximum magnetisation, the coercivity of the material is substantially increased, Fig.3. This is thought to be due to interactions between the domain boundaries (called walls) and the grain boundaries. This interaction results in the domain walls being pinned or locked at the grain boundaries. To create this pinning effect a higher energy is necessary than that required to move domain walls through the grains. However, once a domain wall has been pinned at the grain boundary, very much higher energies are necessary to break the pinning, so the coercivity of the material becomes large.

Since the grains are not completely homogeneous, the applied field necessary to create pinning, or the larger field necessary to break it, are not constant throughout a magnet, which accounts for the behaviour illustrated by Fig.3. This also implies that, once pinning has occurred, a given large demagnetising field may be sufficient to break most of the pinning points and to produce pinned domains in the reverse direction. The result would be a magnet with reversed, but lower, net magnetisation due to the proportion of domains still pinned in the original direction.

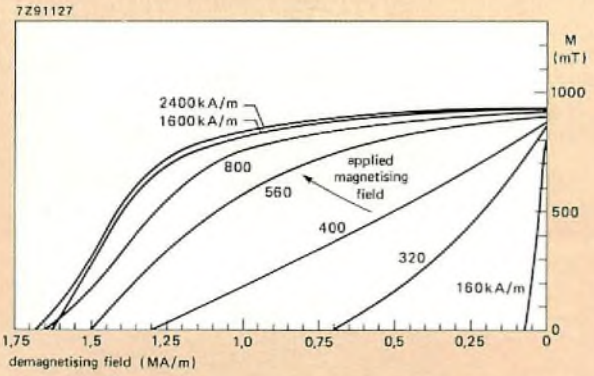


Fig.3 Failure to achieve near saturation of RES materials degrades performance. This is illustrated here by second quadrant curves of an RES 190 magnet resulting from the application of various magnetising fields

With an applied field of around 150 kA/m a high magnetisation can be obtained, but the magnet can still be easily demagnetised or reversed. As the applied field is increased above 300 kA/m the coercivity rapidly increases and the magnet becomes difficult to demagnetise and to remagnetise in another direction.

As indicated, demagnetising and remagnetising with applied magnetic fields is not a straightforward procedure: the results depend on the strength of the initial magnetising field. If this is above 800 kA/m and the magnets are demagnetised by applying fields equal in strength to their intrinsic coercivity, the magnets should be remagnetised with fields around 2.5 MA/m in the same direction as the initial magnetisation, Fig.4.

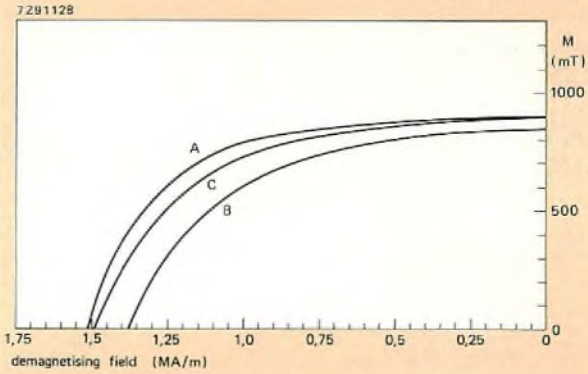


Fig.4 Remagnetisation of RES magnets requires much higher applied fields. This is shown here for an RES 190 magnet. Curve A was obtained after initial magnetisation at 2.5 MA/m; reverse magnetisation at the same field yielded curve B; subsequent remagnetisation in the original direction yielded curve C

RES MAGNET DESIGNS

The principal characteristic of magnetic circuit designs using RES materials can be deduced from their characteristics relative to other, established, magnet materials. Consider a magnetic circuit that requires a magnet capable of supplying 1.6 kA of magnetomotive force and 217 μWb of flux. If the magnet can operate at its $(BH)_{max}$ point for maximum energy and, thus, minimum volume, the areas and magnetic lengths required are:

	length	area
FXD 330	0.88 cm	12.1 cm²
Ticonal 550	2 cm	4 cm²
RES 190	0.46 cm	4.9 cm²

Although RES 190 requires a slightly larger area than Ticonal 550, it requires little more than half the length of the FXD 330 magnet. The relative volume of the system is of paramount importance in many applications; here, the RES magnet has a clear advantage:

	magnet volume
FXD 330	10.6 cm³
Ticonal 550	8 cm³
RES 190	2.25 cm³

The higher working flux density of RES magnets often makes flux-concentrating pole-pieces unnecessary. This results in lower leakage and magnetomotive-force drop and, consequently, less magnet material. In dynamic applications, such as motors, the magnets are exposed to external demagnetising fields. Since recoil takes place along the main BH curve, the reduced allowance for demagnetisation results in less magnetic length.

APPLICATIONS OF RES MAGNETS

When describing the advantages of a new product, there is always the temptation to suggest as wide a range of applications as possible. Here, this temptation has been resisted; only those applications in production, or nearing completion of development are described.

Miniaturising motors

Motors using RES magnets may have an order of magnitude greater power output for the same frame size. Figure 5 compares wound field, ceramic and RES magnet motor designs for the same armature diameter and speed/torque characteristic. The advantage of the RES design is apparent.

Because of cost reductions due to increased production and improved manufacturing methods these advantages are no longer limited to military and aerospace applications.

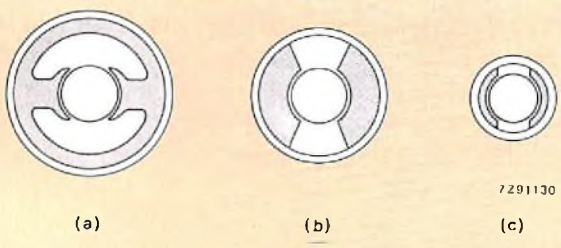


Fig.5 Cross section through motors of identical armature diameter and speed-torque characteristics. The progressive size reduction from the wound-field design (a) achievable with Ferroxdure ceramic stator magnets (b) and RES stator magnets (c)

Permanent-magnet motors using RES magnets are now finding widespread use, especially as

- miniature motors in battery-operated equipment
- miniature stepper motors for clocks and watches
- high-efficiency compact servomotors with power ratings up to 15 kW
- actuating motors for automatic cameras
- drive motors in miniature cassette players
- industrial stepper motors.

Audio-frequency transducers

RES magnets are widely used in microphones, moving-coil pick-ups for record players, earphones, and loudspeakers. Figure 6 compares three loudspeaker magnet-system designs using Ticonal, Ferroxdure and RES. Besides being by far the smallest and lightest, the RES design has the advantage that the magnet is the most closely screened, largely eliminating stray field problems. Figure 7 shows the construction of a miniature loudspeaker using a RES 190 magnet.

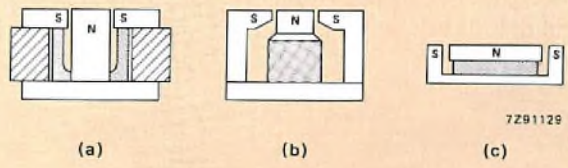


Fig.6 Relative size of loudspeaker magnet systems using (a) FXD 330 ferrite, (b) Ticonal 550 alloy, (c) RES 160 rare-earth cobalt. The last is not only very compact, but completely screened, making it very suitable for miniature equipment

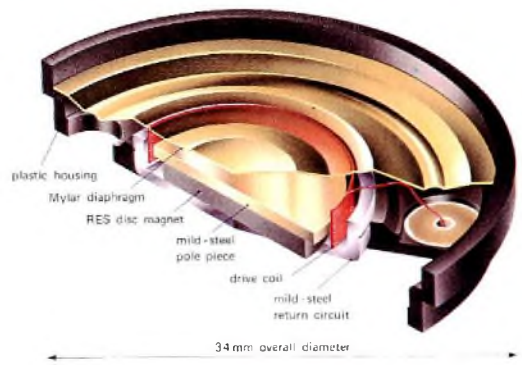


Fig.7 Section through a miniature loudspeaker showing the simple magnetic system design made possible by RES magnets

Position transducers

The high energy per unit volume, and the high, stable, operating flux density possible with RES magnets makes them ideal for applications in moving-coil instruments and other position transducers. A good example is a linear voltage transducer shown in Fig.8, which was developed for the focusing control of the Compact Disc player. Another application from the Compact Disc player is the oscillatory actuator shown in Fig.9.

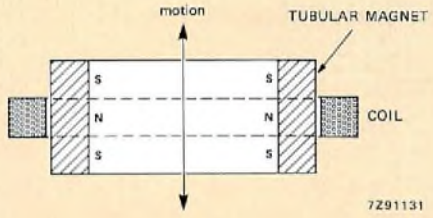


Fig.8 Elements of a linear voltage transducer used in the automatic focusing control of the Compact-Disc player. The transducer produces a force of 100 mN at a current of 25 ampere-turns in the coil; its displacement of 1 mm in each direction is essentially linear with voltage

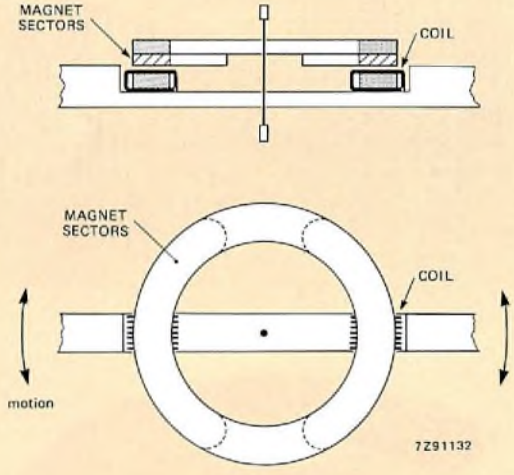


Fig.9 Outline and cross-section of an oscillatory actuator using RES magnets, also developed for the Compact Disc player

More compact portable equipment

The higher energy and flux density due to RES magnets results not only in more compact loudspeakers, motors and other actuators but in considerable increases in their efficiency. This, in turn, reduces the power requirements for the equipment, resulting in further size reduction. For this reason, RES magnets are finding widespread use in miniature, portable audio equipment, Compact Disc players and dictating machines.

Microwave devices

An early application of rare earth-cobalt materials was the construction of periodic-focusing magnets for travelling wave tubes, where considerable reduction in size and weight has been obtained. RES magnets are also used to reduce the weight of magnetrons, isolators and circulators in portable radar.

And almost everything else . . .

Other examples of applications which have been made more practical by RES magnet materials include

- Hall-effect keyboards
- tachometer sensors
- miniature synchronous motors
- high-speed printers.

Compact servo motors using RES magnets are now in service in 'fly-by-wire' military aircraft and are expected to replace much of the conventional hydraulic equipment in the next generation of transport aircraft. These motors ease the problem of interfacing the automatic pilot to the control surfaces.

In fact, it is apparent that, as their cost comes down, so RES magnets will find an increasing number of applications where their small size and low weight are of great advantage. A typical example is in the design of magnetic bearings, where their high resistance to demagnetisation, high stored energy and high stability are of vital importance.

The RES family of permanent-magnet materials complements the improvements made possible by integrated circuit techniques. Compact electronics can now be mated with efficient, miniature mechanical transducers based on these materials, thus enabling full advantage to be taken of the reduced power consumption, and weight, and volume made possible by integrated-circuit technology.

PERMANENT MAGNETS

For most applications, permanent magnets should be made from a material that provides adequate magnetic flux, stores a useful amount of energy per unit volume, and is resistant to demagnetisation. Such a material is described as magnetically hard, and is characterised by its full hysteresis loop.

After magnetisation to saturation, B_s, removal of the external field causes the magnet flux density to fall back beyond remanence, B_r, to an extent that depends on the shape of the magnet. The magnet then 'works' at a point (B_w, H_w) corresponding to the effect of self-demagnetising by the magnet. This point lies in the second quadrant (+B, −H) of the hysteresis loop; it is this part of the loop which usually defines the usefulness of the magnet in a given application. The product ($B_w H_w$) gives the energy outside the magnet. At some point on the curve, ($B_w H_w$) reaches a maximum value $(BH)_{max}$; this is a major criterion for comparing permanent magnet materials, it determines the size of magnet required to provide a given value of field in a given air gap.

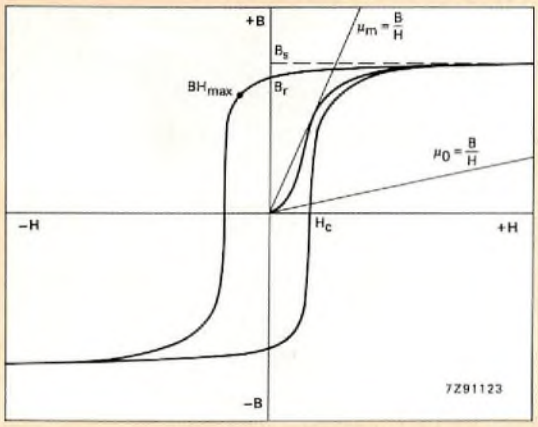


Fig.A. Hysteresis (B versus H) loop of a permanent-magnet material. The performance of a magnet is determined by the shape of the second quadrant (+B, −H) of the loop. Flux density B sets the area of the magnet; demagnetising field H_c sets the length of the magnet; and, finally, maximum energy-product $(BH)_{max}$ sets the overall volume of material required

EVOLUTION OF PERMANENT-MAGNET MATERIALS

Apart from the naturally-occuring oxide or iron known as lodestone, which was the first permanent magnet material to find widespread use, the earliest manufactured magnets were made from hard steels. Those first magnet steels were hardened by their high carbon content. Progressive improvements in performance were made with additions of tungsten, nickel and cobalt. The best magnet steels of the 1930s contained 35% cobalt.

During the period 1925 to 1950, Philips' Research Laboratories developed the Ticonal series of titanium, cobalt, nickel, aluminium iron alloys whose performance was greatly superior to the best cobalt steels. Those alloys greatly aided the development of moving-coil meters, loudspeakers and radar devices.

The scarcity of nickel which was becoming apparent at the beginning of the 1950s, stimulated the search for other permanent-magnet materials. The result of this search was the development (also in Philips' Research Laboratories) of Ferroxdure ceramic magnet materials. These consist mainly of iron oxide with various additions according to the properties required.

Many other combinations of both magnetic and non-magnetic elements have been known for a long time to give useful properties as permanent magnets. Some, such as Silmanal (Ag-Mn-Al) and platinum-cobalt, are too expensive to find widespread use. Others, such as manganese-aluminium, are difficult to form or have poor mechanical properties. The potential of rare-earth elements, especially samarium, as bases for permanent-magnet materials has been known since about 1905, but not commercially exploited until fairly recently.

An evolutionary tree of commercially-important permanent-magnet materials looks very much like this. The two main branches of development are apparent: ceramics, culminating with Ferroxdure, and metal alloys, of which RES materials are the most advanced.

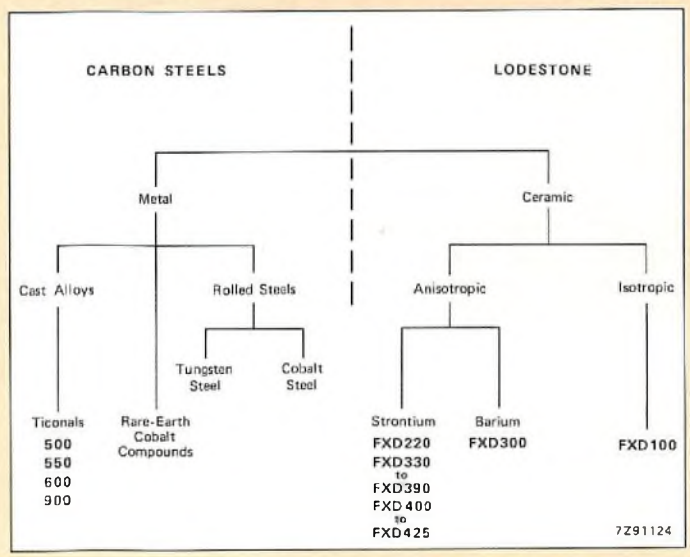


Fig.B. The evolution of permanent-magnet materials has proceeded in two main branches: metallic and ceramic materials

Multiple loudspeaker arrays using Bessel coefficients

W. J. W. KITZEN

Stereo aside, if you want to fill an auditorium with high-fidelity sound, you have a choice: one large loudspeaker or an array of smaller ones. Single loudspeakers capable of radiating 200 W or more are usually expensive and cumbersome. An array of smaller ones is usually easier to install and cheaper. However, such arrays do have certain drawbacks – at least in the form they have generally taken until now.

An array of N loudspeakers connected in parallel and in phase can radiate N^2 times as much power as a single loudspeaker at very low frequencies, but only N times as much at high frequencies. The power response of the array is therefore quite different from that of the single loudspeakers that compose it. This is due to the increased directivity of the array; whereas the radiation pattern of a single loudspeaker is reasonably omnidirectional, usually up to at least a few kilohertz, that of an array is so only at low frequencies. At high frequencies it becomes much more directive; moreover, the directivity varies considerably with frequency. Audience members seated away from the axis of the array therefore perceive a quite different tonal balance from those seated on-axis.

These shortcomings can be remedied, at some expense to power radiation, by correctly proportioning the drive to the individual speakers of the array. The required proportioning coefficients are based on Bessel functions.

BESSEL COEFFICIENTS

Consider an array of 2N+1 speakers equidistantly spaced in a straight line (Fig.1) and driven by a common signal multiplied by coefficients $(a_{-N}, a_{-N+1}, \ldots a_0, \ldots a_{N-1}, a_N)$ peculiar to each speaker. Assume that

- the point of observation P is in the far-field region of each speaker
- the radiation of each speaker is not influenced by the others
- all speakers have the same frequency and directional response $A(\omega, \theta)$.

The sound pressure at P is then given by

$$p(\omega, \theta) = A(\omega, \theta) \sum_{n=-N}^{N} a_n \exp(jnx)$$

where

$x = \dfrac{\omega l \sin \theta}{v}$

ω = radial frequency of the sound

v = velocity of sound

l = distance between speakers.

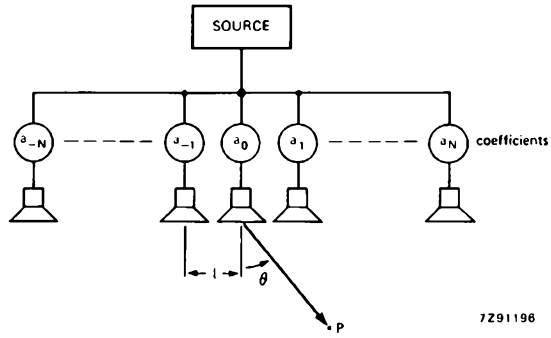


Fig.1 Linear array of 2N–1 uniformly spaced loudspeakers driven from a common signal source via individual proportioning coefficients

If, for example, N = 2 and all the coefficients $a_n = 1$ (i.e. 5 loudspeakers identically driven),

$$p(\omega, \theta) = A(\omega, \theta)\,[1 + 2\cos x + 2\cos 2x]$$

which is very dependent on both frequency and direction (Fig.2).

However, if we choose drive coefficients of the form $a_n = J_n(z)$, where $J_n(z)$ is a Bessel function of the first kind of order n,

$$J_n(z) = \left(\frac{z}{2}\right)^n \sum_{k=0}^{\infty} \frac{(-z^2/4)^k}{k!\,(n+k)!}$$

the sound pressure at P then becomes

$$p(\omega, \theta) = A(\omega, \theta) \sum_{n=-N}^{N} J_n(z) \exp(jnx)$$

$$= A(\omega, \theta) \exp(jz \sin x) \qquad \text{if } N \to \infty$$

Therefore, $|p(\omega, \theta)| = |A(\omega, \theta)|$ if z is real. That is, the dependence of |p| on direction and frequency is the same for the array as for a single speaker.

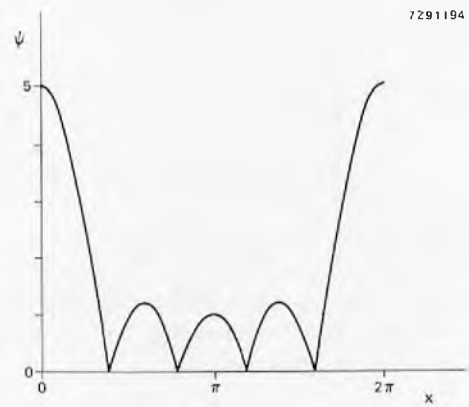


Fig.2 Frequency and direction dependence of a 5-speaker parallel-driven, in-phase array, normalised with respect to that of a single speaker

$\psi = 1 + 2\cos x + 2\cos 2x \qquad x = (\omega l \sin\theta)/v$

PRACTICAL NETWORKS

If integer values of z are chosen, the resulting values of $J_n(z)$ do not lend themselves to realisation by simple networks (see Table 1). However, the choice is not limited to integer values. For a practical loudspeaker array, the thing to do is to look for values of z which yield values of $J_n(z)$ that stand in simple ratios to each other. Moreover, since Bessel functions always satisfy the relation $J_{-n}(z) = (-1)^n J_n(z)$, it becomes possible to realise the corresponding drive coefficients by appropriately connecting the loudspeakers in series or parallel, in phase or antiphase.

TABLE 1
Bessel coefficients $a_n = J_n(z)$ for integer values of z, for arrays with 2N + 1 loudspeakers

N	z	a_0	a_1	a_2	a_3	a_4
2	1	0.7652	0.4401	0.1149		
3	2	0.2239	0.5767	0.3528	0.1289	
4	3	−0.2601	0.3391	0.4861	0.3091	0.132

For a 5-speaker array a good choice is z = 1.5, giving

$$J_2 : J_1 : J_0 : J_{-1} : J_{-2} = 0.23 : 0.56 : 0.51 : -0.56 : 0.23$$

the ratio of which can be approximated by the integral coefficients

$$a_2 : a_1 : a_0 : a_{-1} : a_{-2} = 1 : 2 : 2 : -2 : 1$$

These coefficients can be realised by connecting the loudspeakers in either of the ways shown in Fig.3.

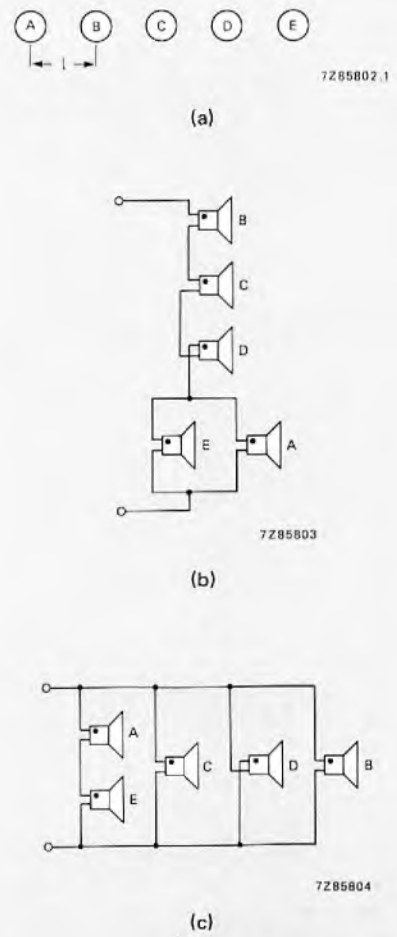


Fig.3 Five-speaker Bessel array, layout and wiring alternative

For a 7-speaker array, the choice z = 2,6 gives

$$J_3:J_2:J_1:J_0:J_{-1}:J_{-2}:J_{-3} = 0.24:0.46:0.47:-0.1:-0.47:0.46:-0.24$$

the ratio of which can be approximated by

$$a_3:a_2:a_1:a_0:a_{-1}:a_{-2}:a_{-3} = 1:2:2:0:-2:2:-1$$

which in fact requires only six speakers (Fig.4), since the middle one, whose coefficient is 0, can be omitted.

For a 9-speaker array, the choice z = 3.8 gives

$$J_4:J_3:J_2:J_1:J_0:J_{-1}:J_{-2}:J_{-3}:J_{-4} = 0.25:0.42:0.41:0.01:-0.4:-0.01:0.41:-0.42:0.25$$

corresponding to coefficients

$$a_4:a_3:a_2:a_1:a_0:a_{-1}:a_{-2}:a_{-3}:a_{-4} = 1:2:2:0:-2:0:2:-2:1$$

In this case two speakers can be omitted. Note, though, that to preserve the geometry on which the principle of the Bessel coefficients is based, in this as well as the preceding example the spacing must be the same as it would be if the omitted speakers were actually present.

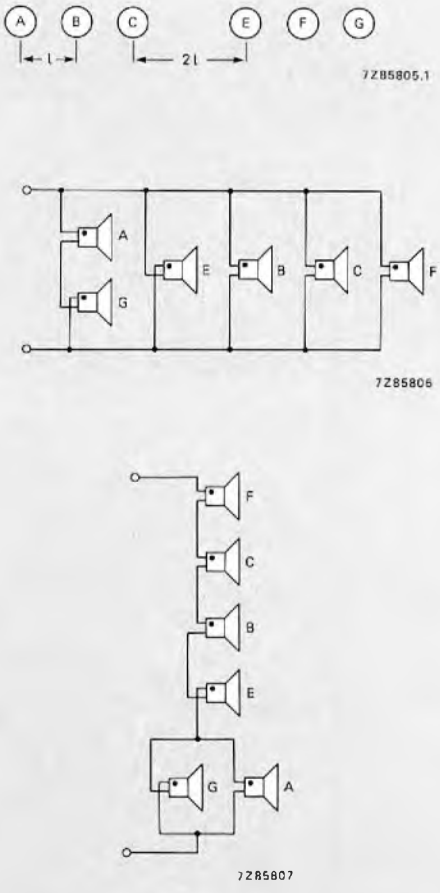


Fig.4 Seven-speaker Bessel array. As the driving coefficient of the centre speaker is 0, that speaker can be omitted but normal space for it must be allowed for it in the baffle layout nevertheless

Other sets of practical coefficients can be found by calculation for larger arrays. The size of the spacing unit l between speakers (including notional ones with drive coefficient zero) is not critical. However, the smaller the spacing the smaller the complete array and the shorter the distance for which the far-field approximation is valid; so, for best results, the spacing should be as small as the structure and material of the baffle allows.

GAIN AND RIPPLE

The gain of an array of n speakers can be defined as

$$G = 10 \log \frac{P_n}{P_1}$$

where P_n is the maximum power that can be radiated by the array, and P_1 the maximum power that can be radiated by a single speaker. For a Bessel array P_n is not so large as for a plain parallel-driven array of the same nominal size. It is, however, much more uniform throughout the frequency spectrum. Thus, the sound pressure radiated by a Bessel array is not nearly so dependent on frequency and direction as that of a parallel-driven array. A measure of this dependence is the ripple factor R:

$$R = 20 \log \frac{|p(\omega,\theta)|_{max}}{|p(\omega,\theta)|_{min}}$$

Table 2 compares the calculated low and high-frequency gains and the ripple factors of 5, 7 and 9-speaker Bessel and parallel-driven arrays. The polar diagrams in Fig.5, which reflect measurements on otherwise identical Bessel and parallel-driven arrays using 5 Philips squawkers, further illustrate the comparative frequency and directional independence of the Bessel array.

TABLE 2
Gain and ripple factor comparison of parallel-driven and Bessel loudspeaker arrays

type	number of speakers	driving coefficients	G low freq. (dB)	G high freq. (dB)	R (dB)
parallel	5	1:1:1:1:1	14	7	∞
Bessel	5	1:2:2:−2:1	6	5.4	1.2
parallel	7	1:1:1:1:1:1:1	16.9	8.5	∞
Bessel	7(6)	1:2:2:0:−2:2:−1	6	6.5	1
parallel	9	1:1:1:1:1:1:1:1:1	19	9.5	∞
Bessel	9(7)	1:2:2:0:−2:0:2:−2:1	6	7.4	3.6

Numbers in parenthesis denote actual number of speakers required when one or more of the driving coefficients is 0.

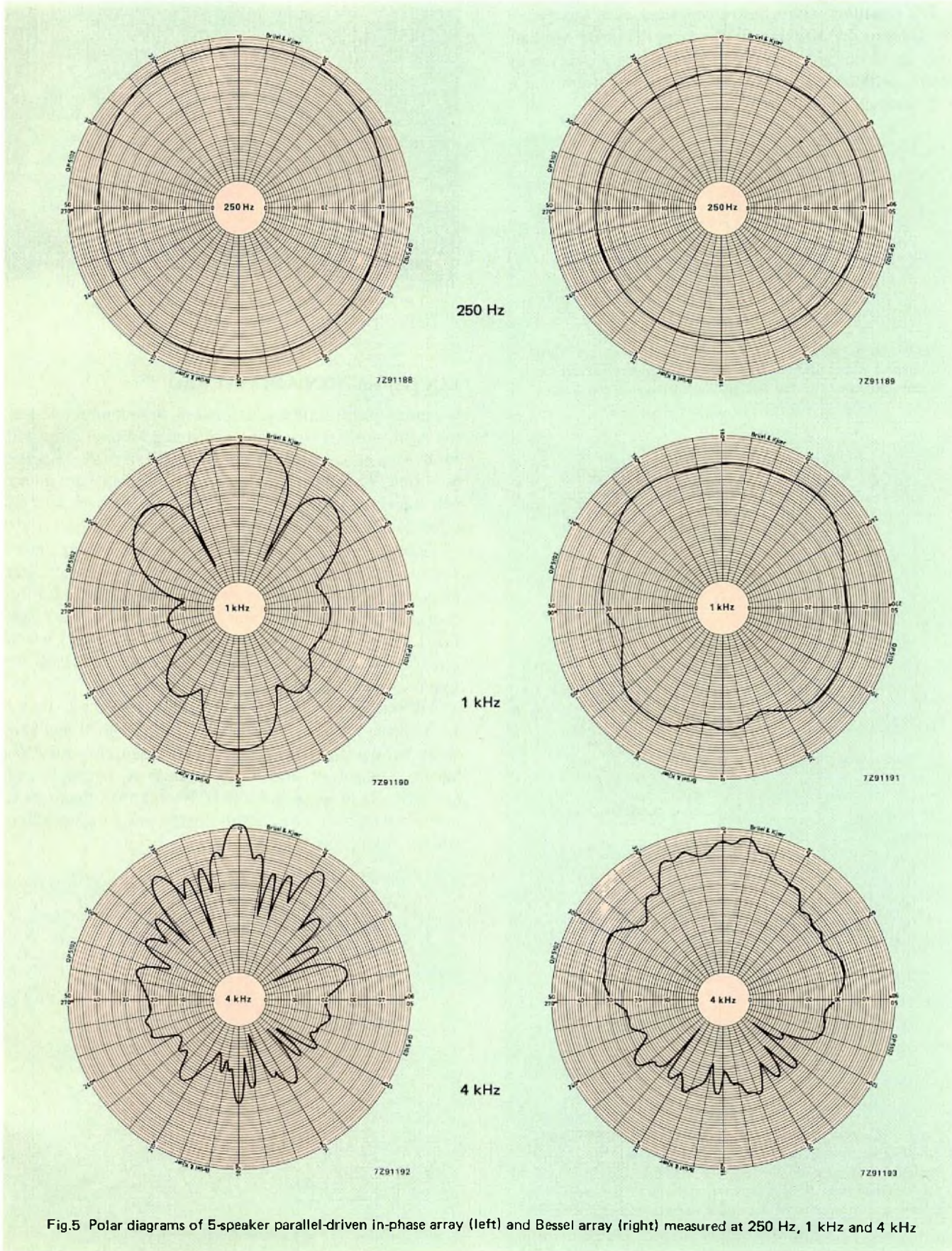
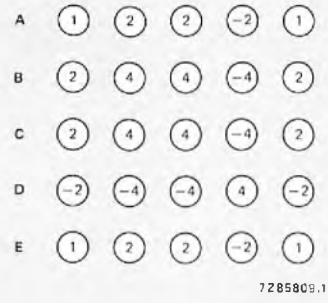


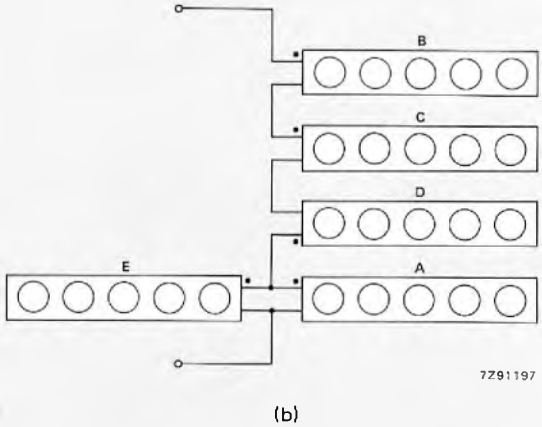
Fig.5 Polar diagrams of 5-speaker parallel-driven in-phase array (left) and Bessel array (right) measured at 250 Hz, 1 kHz and 4 kHz

The radiation pattern can be concentrated at the level of the speakers by stacking similar arrays (Fig.6). A square array in which both the rows and columns are driven by Bessel coefficients (Fig.7) gives a radiation pattern that is both vertically and horizontally omnidirectional.

Fig.6 Stacked Bessel arrays. When the three panels are driven in parallel their radiation is omnidirectional in the horizontal plane but concentrated vertically at the level of the arrays



(a)



(b)

Fig.7 (a) Layout and driving coefficients of a 25-speaker Bessel array for hemispherical sound distribution; each horizontal row of speakers is connected as shown at (c) in Fig.3. (b) Interconnection of the horizontal rows to obtain the driving coefficients given in (a); the impedance of the array is equal to that of a single speaker

Model arrays of the type illustrated in Fig.7

LOCALISATION AND STEREO

Owing to phase differences between the sound arriving at the right and left ear, a listener facing a Bessel array will localise the sound somewhat to the right of centre. For the 5, 7 and 9-speaker arrays described, the apparent source will coincide with the speaker driven by coefficient a_1. This effect can be used to obtain stereo from a single Bessel array.

Figure 8 shows a 5-speaker Bessel array wired for stereo. Tested with Philips squawkers mounted 15 cm apart, this array gave a good stereo image at a distance of 3 m for frequencies up to about 6 kHz; at higher frequencies the image faded. (Note: the frequency response of the speaker, which is intended as a squawker in 3-way systems, dips 9 dB between 6 kHz and 8 kHz.)

The stereo image can be varied by taking the L+R and L−R signals of Fig.8 to a balance control before applying them to the junctions indicated. The outputs from the balance control are k(L+R) to speakers A, C and E, and (1−k)(L−R) to speakers B and D. When k = 0.5 the result is normal stereo; when $k < 0.5$ the stereo image expands, and when $k > 0.5$ it shrinks.

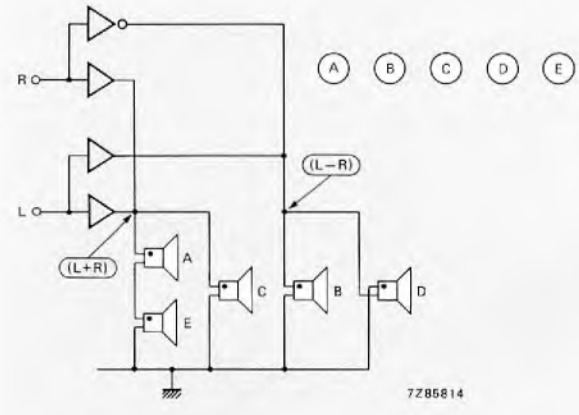


Fig.8 Stereo Bessel array

OTHER APPLICATIONS

Bessel coefficients can also be applied to microphone arrays and artificial reverberation systems. Figure 9 shows an element of a reverberation system in which signals taken from a delay line tapped at equal intervals are added together after being multiplied by Bessel coefficients to give a flat amplitude response.

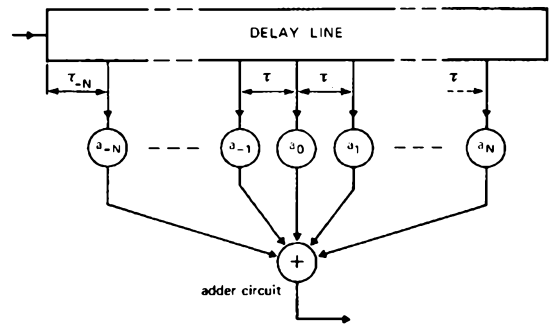


Fig.9 Echo simulator using Bessel coefficients for flat response

ACKNOWLEDGEMENT

This article is based on the work of the late N. V. Franssen of Philips' Research Laboratories.

Silicon temperature sensors

A. PETERSEN

Over the past few years, the increasing use of integrated circuits in control systems has stimulated a demand for electronic temperature sensors that are both accurate and reliable. The KTY81/83/84 series of silicon temperature sensors are well placed to meet this demand. Developed to provide an alternative to more conventional sensors using NTC or PTC thermistors, these new devices make use of the temperature dependence of resistivity exhibited by silicon.

Figure 1 shows this dependence for n-type silicon at several doping levels. As the figure indicates, the temperature coefficient of resistance of doped silicon is initially positive and becomes negative at higher temperatures (when the intrinsic semiconductor properties predominate). The KTY81/83/84 series operate in the positive region. They use n-type silicon with a doping level between 10^{14} and $10^{15}/cm^3$, providing a nominal resistance of about 1000 Ω. (Note, however, that two variants of the KTY81 series exist, the KTY81/2 and KTY81/5 series, with nominal resistances of 2000 Ω and 5000 Ω respectively).

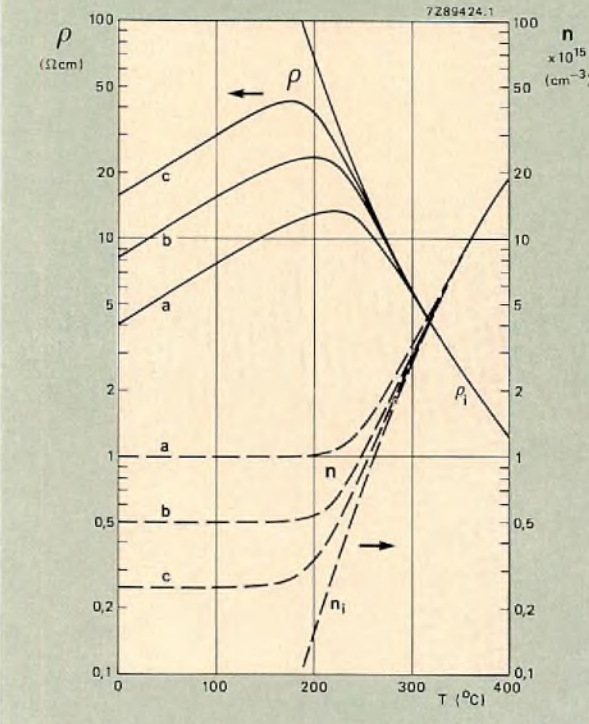


Fig.1 Resistivity ρ of n-type silicon versus temperature for various doping levels (a, b, c). The initial rise in resistivity is caused by the fall in free charge-carrier mobility with rising temperature, and over this region, silicon exhibits a positive temperature coefficient of resistance. At higher temperature, the number n of free charge carriers,increases (due to increase in the number n_i of spontaneously-generated charge carriers) and the intrinsic semiconductor properties of silicon predominate. Resistivity then falls with increasing temperature

CONSTRUCTION AND MANUFACTURE

Figure 2(a) shows the basic sensor, the approximate size of which is 500 μm x 500 μm x 240 μm. The entire bottom plane is metallized, and the upper plane is provided with a circular gold contact of about 20 μm diameter. This arrangement provides a conical current distribution through the crystal, which significantly reduces the dependence of sensor resistance upon manufacturing tolerances. An n^+ region, diffused into the crystal beneath the metallization, reduces barrier-layer effects at the metal/semiconductor junctions.

Figure 2(b) shows a second arrangement consisting effectively of two single sensors connected in series but with opposite polarity. This *twin-sensor* arrangement has the advantage of providing a resistance that is independent of

current direction, in contrast to the *single-sensor* arrangement of Fig.2(a), which, for larger currents at least, gives a resistance that varies slightly with current direction.

The devices are manufactured using the now familiar *planar* technique that has proved its reliability in the manufacture of many other semiconductor devices. A layer of silicon nitride protects the crystal surface, and to provide additional protection, the entire crystal is coated with phosphor glass.

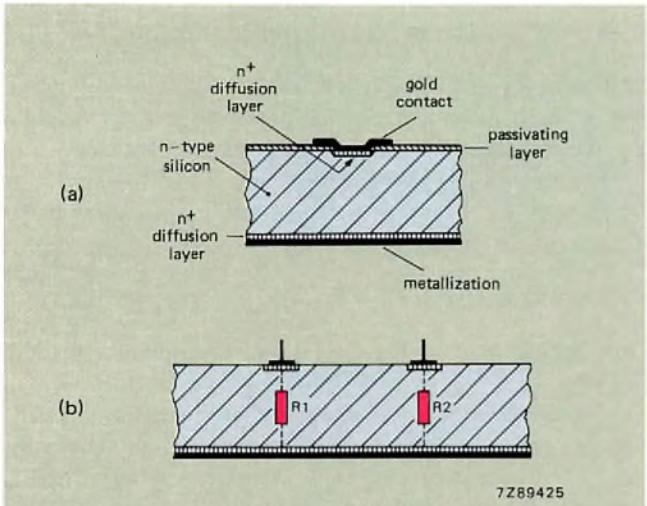


Fig.2 (a) Section through the crystal showing the electrode arrangement. The entire bottom plane is metallized, and the top plane is provided with a circular gold contact; (b) setup consisting of two single sensors connected in series but with opposite polarity

PRACTICAL DEVICES

Both arrangements shown in Fig.2 are used in practical devices. The KTY81 series uses the twin-sensor arrangement. These sensors, in SOD-70 encapsulation (Fig.3(a)), are therefore polarity independent.

The KTY83/84 series use the more basic single-sensor arrangement. The simplicity of this arrangement allows the sensors to be produced in compact DO-34 encapsulation (Fig.3(b)) – marked to indicate polarity.

Besides simplicity, the single-sensor device has another important advantage – the potential for operation at temperatures up to 300 °C.

The normal temperature sensor has a temperature limit of around 150 °C, imposed by the intrinsic semiconductor properties of silicon (Fig.1). If, however, the single-sensor device is biased with its gold contact positive, the onset of intrinsic-semiconductor behaviour is shifted to higher temperature. This stems from the fact that a positive voltage on the gold contact severely depletes the hole concentration in the upper n^+ diffusion layer, and so effectively isolates holes spontaneously generated within the body of the crystal (due to its intrinsic nature) – preventing them from contributing to the total current, and hence from affecting the resistance.

The intrinsic semiconductor properties of the crystal will, of course, ultimately predominate, but at a higher temperature than for the normal sensor. The effect is current sensitive, the temperature of transition from extrinsic to intrinsic behaviour increasing with increasing operating current. At zero current the effect is entirely absent and the sensor behaves in the conventional way.

The KTY84 series makes use of this property – being designed specifically for operation at temperature up to 300 °C.

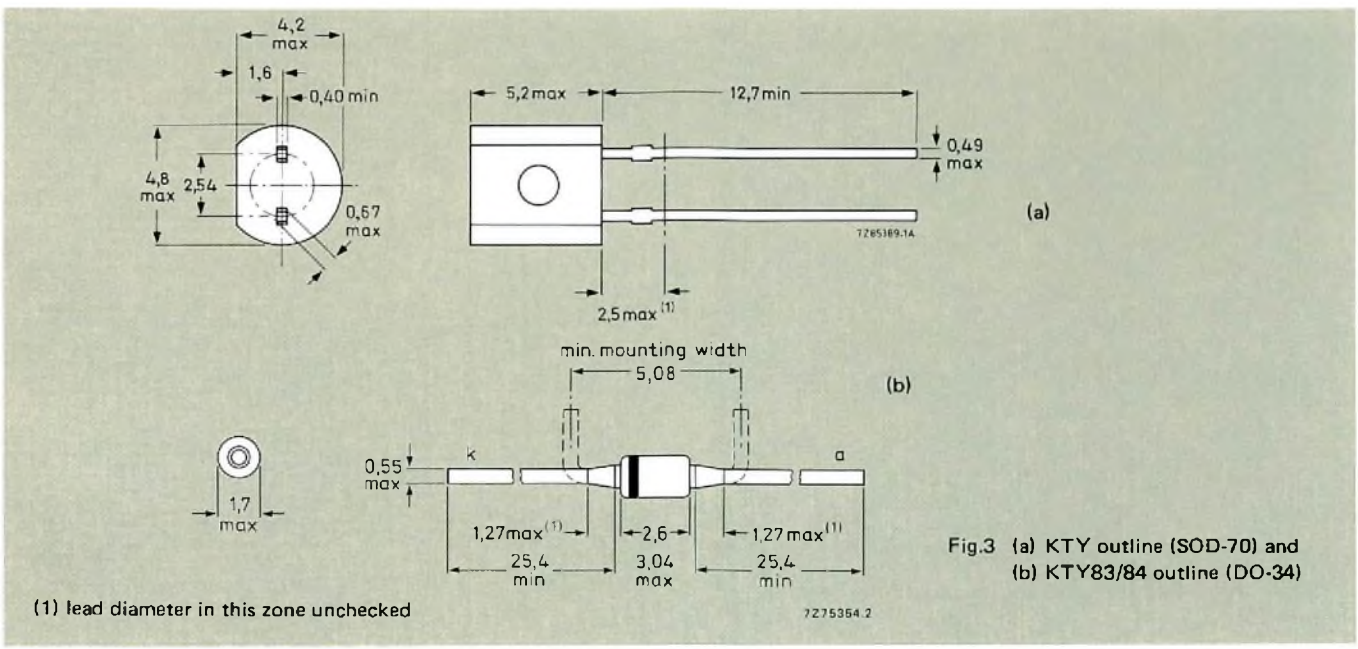
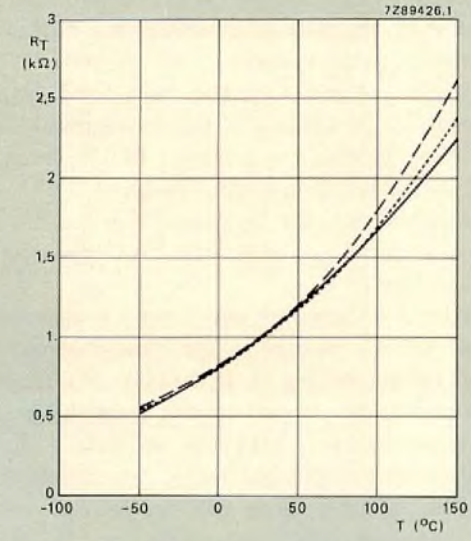
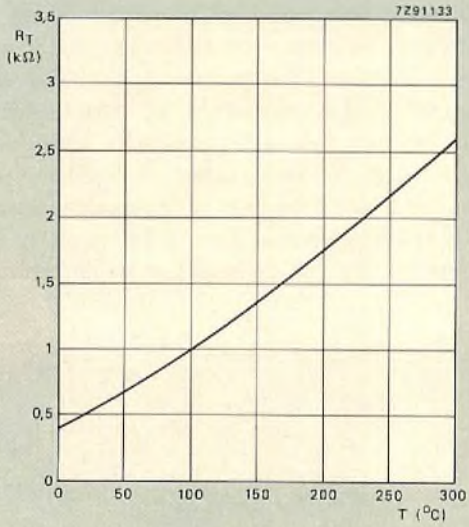


Fig.3 (a) KTY outline (SOD-70) and (b) KTY83/84 outline (DO-34)

(1) lead diameter in this zone unchecked



(a)



(b)

Fig.4 (a) Variation of KTY81 resistance with temperature

———— experimental curve

– – – – – – $R_T = R_{amb} \exp [\alpha(T - T_{amb})]$ with $\alpha = 0{,}75\%/K$

..... $R_T = R_{amb} \exp [\alpha(T - T_{amb})]$ with $\alpha = 0{,}82\%/K$ for $T \leqslant T_{amb}$, and $\alpha = 0{,}7\%/K$ for $T > T_{amb}$

(b) Variation of KTY84 resistance with temperature

PERFORMANCE

The table overleaf gives the electrical and mechanical specifications of the KTY/81/83/84 series.

Temperature dependence

Figures 4(a) (solid line) and 4(b) show respectively the resistance/temperature characteristics of the KTY81 and KTY84. The dependence is non-linear, and can be approximated by

$$R_T = R_{amb} [1 + \alpha(T - T_{amb}) + \beta(T - T_{amb})^2] \qquad (1)$$

in which, R_T and R_{amb} are the resistances at temperature T and at ambient temperature T_{amb} respectively, and α and β are the sensor's temperature coefficients of resistance.

For the KTY81, $\alpha = 0{,}75\%/K$ and $\beta = 0{,}00185\%/K^2$ at $T_{amb} = 25\,^{\circ}C$. So for most practical purposes β can be neglected and relation (1) becomes

$$R_T = R_{amb} \exp [\alpha(T - T_{amb})]$$

The broken line in Fig.4(a) shows this relation for the KTY81.

The above expression assumes that α remains constant over a range of temperatures. In reality, α itself varies with temperature as shown in Fig.5. A better approximation is thus obtained by taking two values for α: 0,82%/K for $T \leqslant T_{amb}$, and 0,7%/K for $T > T_{amb}$. Substitution of these values into the above expression yields the dotted line in Fig.4(a), which is quite close to the true curve.

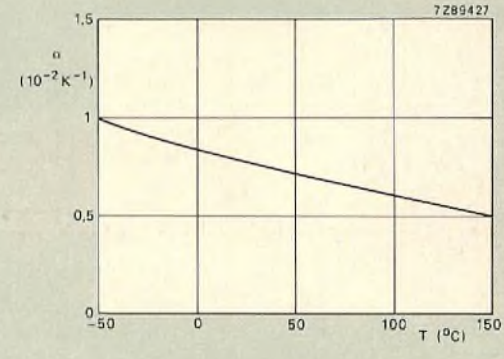


Fig.5 Variation of α with temperature (KTY81).

Electrical and mechanical specifications of the KTY81/83/84 series

	KTY81	KTY83	KTY84
resistance at T_{amb}	1000 Ω ± 1%[1][3]	1000 Ω ± 1%[1]	1000 Ω ± 2%[2]
temperature coefficient of resistance	typ 0,75%/K[1]	typ 0,75%/K[1]	typ 0,6%/K[2]
measuring temperature range	−55 to 150 °C	−55 to 175 °C	0 to 300 °C
max load current			
at T_{amb} = 25 °C	10 mA	10 mA	10 mA[4]
at T_{amb} = 150 °C	1 mA	1 mA	–
at T_{amb} = 300 °C	–	–	2 mA[4]
thermal time constant			
in still air	85 s	40 s	40 s
in flowing liquid	3 s	0,5 s	0,5 s
in still liquid	5 s	1 s	1 s
encapsulation	SOD-70	DO-34	DO-34

[1]) T_{amb} = 25 °C.
[2]) T_{amb} = 100 °C.
[3]) variants of the KTY81 are available: the KTY81/2 and KTY81/5 with resistances of 2000 Ω and 5000 Ω respectively.
[4]) for high-temperature measurements the KTY84 needs a minimum load current of about 2 mA.

Operating current

Figure 6 shows how the resistance of a typical KTY81 sensor varies with operating current. Up to about 1 mA, the resistance is substantially independent of operating current, so this figure should be regarded as the upper limit if current fluctuations are to have minimal effect upon resistance.

Note: for the KTY84 series, operating currents in excess of 2 mA must be used to permit operation up to the specified 300 °C.

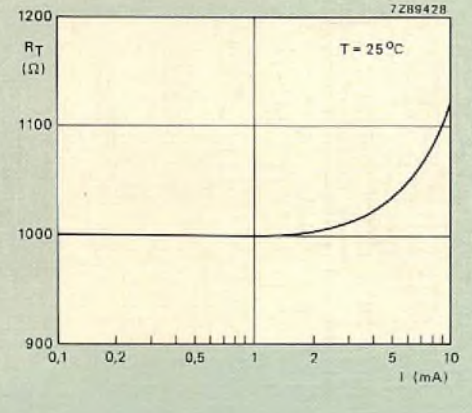


Fig.6 Dependence of sensor resistance on operating current. Below about 1 mA the resistance is substantially independent of temperature

Linearization

The non-linear resistance/temperature characteristic of the silicon temperature sensor is not normally a handicap if the device is properly calibrated. It's only in control systems requiring high accuracy that linearization of the sensor becomes necessary.

A simple way of linearizing the resistance/temperature characteristic of the sensor is to shunt it with a fixed resistor R. The resistance $RR_T/(R + R_T)$ of the parallel combination then effectively becomes a linear function of temperature, and the output voltage V_T of the linearizing circuit can be used to regulate the control system.

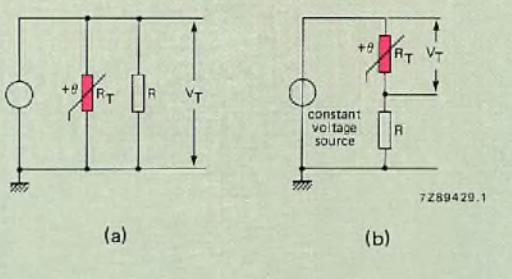


Fig.7 Linearization of sensor characteristics (a) with a resistor R shunted across the sensor; (b) with a resistor R in series with the sensor and the system powered by a constant-voltage source

If the system is powered by a constant-voltage source, a resistor can be connected in series with the sensor, the voltage across the sensor and across the resistor will then again be approximately linear functions of temperature.

The value of the series or parallel resistor depends on the required operating-temperature range of the sensor. A method for finding this resistance will now be described that gives zero temperature error at three equidistant points T_a, T_b and T_c say.

Take the parallel arrangement first. If the resistance of the sensor at the three points is R_a, R_b and R_c, and the corresponding resistance of the parallel arrangement R_{pa}, R_{pb} and R_{pc}, the requirement for linearity at the three points is

$$R_{pa} - R_{pb} = R_{pb} - R_{pc}$$

i.e.

$$\frac{RR_a}{R + R_a} - \frac{RR_b}{R + R_b} = \frac{RR_b}{R + R_b} - \frac{RR_c}{R + R_c}$$

So

$$R = \frac{R_b (R_a + R_c) - 2R_aR_c}{R_a + R_c - 2R_b} \qquad (2)$$

For the series arrangement with a constant voltage source V, and with voltages V_a, V_b and V_c across the sensor at the three points, the requirement for linearity is

$$V_a - V_b = V_b - V_c$$

i.e.

$$\frac{VR_a}{R + R_a} - \frac{VR_b}{R + R_b} = \frac{VR_b}{R + R_c} - \frac{VR_c}{R + R_c}$$

This reduces to relation (2) above, which means that the same resistor is suitable for both the series and parallel arrangements.

So with a knowledge of the required operating temperature range, R can be calculated from relation (2) using the resistance/temperature curves (Fig.4) to determine the sensor resistance at the three points.

As an example, Fig.8 shows the deviation from linearity to be expected from a nominal KTY81 sensor linearized over the temperature range 0 to 100 °C with a linearizing resistance of 2870 Ω.

Note: because the KTY84 is chiefly intended for use at higher temperatures, say above 100 °C, its almost linear characteristic at these temperatures means that linearization is often unnecessary.

MANUFACTURING TOLERANCES AND THEIR EFFECT UPON SENSOR CHARACTERISTICS

As stated above, the electrode arrangement in the KTY81/83/84 series has the advantage of minimizing the effects of manufacturing tolerances. Fig.9 shows the variation of resistance with thickness D of the crystal.

After a sharp rise for small values of D (<50 μm say), the resistance levels off and thereafter remains relatively insensitive to further increase of D. So any spread in the values of D incurred during manufacture, will have little effect upon the final characteristics. Far more important, in fact, is the diameter d of the gold contact (see Fig.9) and the thickness x of the n^+ diffusion layer. Fig.10 shows the effect of this latter parameter on the resistance. The heavy dependence on x, far from being a disadvantage, provides a useful means of offsetting the effects of spread in the values of d and of the doping level.

As a result of the above considerations, silicon temperature sensors are normally produced to quite fine tolerances – ΔR and Δα in the region of ±1%. These compare favourably with typical values quoted for NTC thermistors (ΔR = ±10% and Δα = ±5%).

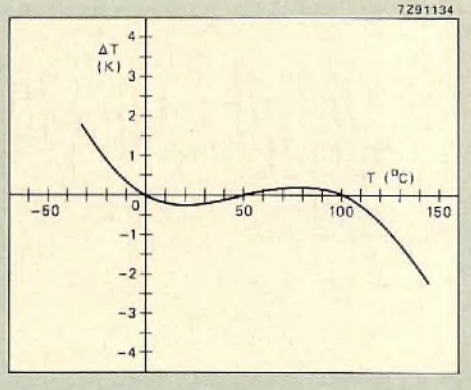


Fig.8 Temperature error ΔT to be expected from a nominal KTY81 sensor linearized over the temperature range 0 to 100 °C (linearizing resistance 2870 Ω)

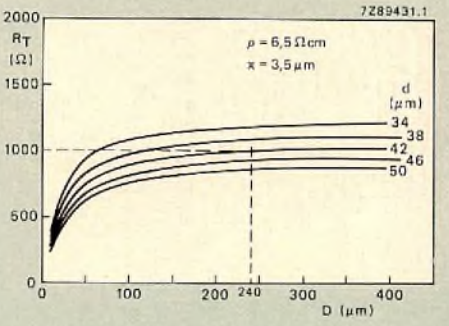


Fig.9 Variation of sensor resistance R_T with the thickness D of the crystal. After an initial rise, the resistance thereafter remains relatively insensitive to further increase of D. The resistance is, in fact, far more sensitive to variations in the diameter d of the gold contact

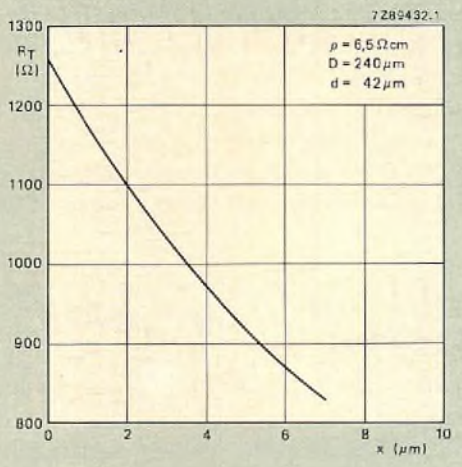


Fig.10 Sensor resistance R_T as a function of the thickness x of the n^- diffusion layer. The heavy dependence of resistance on x provides a useful means of offsetting the effects of spread in the value of d and in the doping level

Figure 11 shows the absolute temperature error ΔT of a silicon temperature sensor with reference temperature (i.e. the temperature at which α is defined) of 25 °C. The minimum error occurs at 25 °C, since at this temperature the only contribution to ΔT comes from ΔR. Away from this temperature, the influence of $\Delta\alpha$ becomes ever more important and ΔT increases.

Figure 12 shows the combined effect of manufacturing-tolerances and linearization errors for the KTY81 sensor linearized over the temperature range 0 to 100 °C. Calibration of the subsequent circuitry (opamps, control circuitry etc.) can reduce this error significantly. Figure 13(a) shows the temperature error of the system with (linear) output circuitry calibrated at 50 °C and Fig.13(b) shows the error of the same system calibrated at 0 and 100 °C.

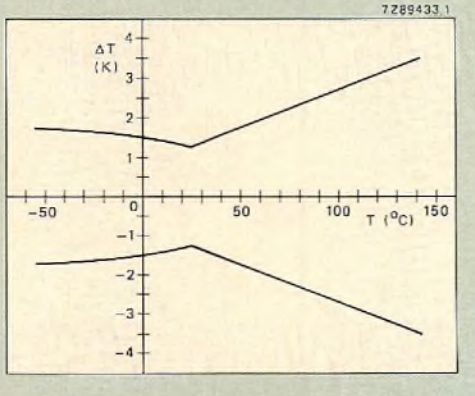


Fig.11 Absolute error ΔT expected of a silicon temperature sensor

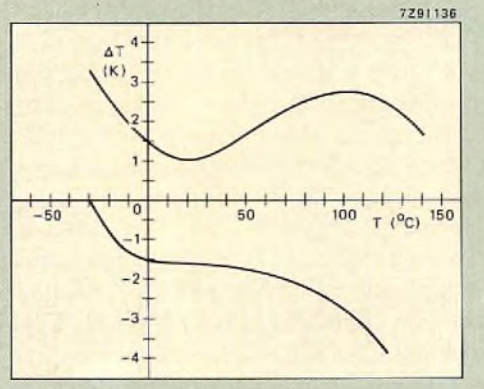
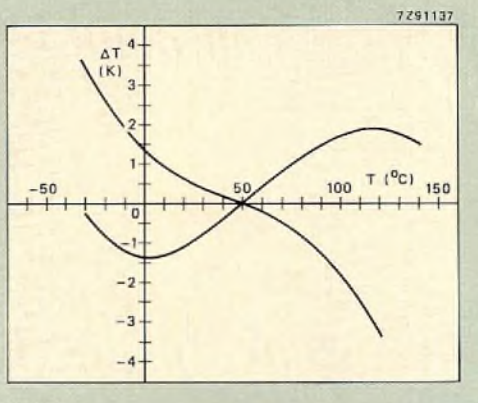
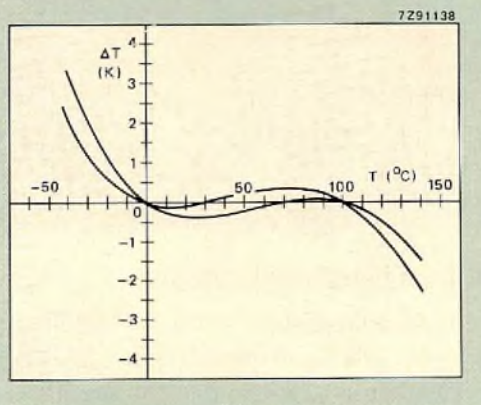


Fig.12 Combined effect of manufacturing-tolerance and linearization errors for the KTY81 sensor



(a)



(b)

Fig.13 (a) temperature error of system with linear output circuitry calibrated at 50 °C; (b) error of the same system calibrated at 0 and 100 °C

CIRCUITRY

Simple bridge circuit

Figure 14 shows a simple circuit for giving a temperature dependent signal within the temperature range 0 °C to 100 °C. The silicon sensor forms part of a bridge network across which a stabilized voltage derived from a zener diode is applied. A potential divider formed by R_2, R_3 and R_4 sets this voltage at about 2,5 V. The circuit employs an NE532 opamp, one half of which (A_1) acts as an impedance transformer, and the other half (A_2) exclusively as an amplifier. The output ranges from 0 to 5 V, i.e. 50 mV/K.

The circuit is calibrated at the extreme ends of its range, first by adjusting R_9 to give 0 V output at 0 °C, and then by adjusting R_4 to give 5 V at 100 °C. When properly calibrated, the error of this circuit, including the effects of the saturation voltage of the output stage A_2, can be kept within ±0,2 °C.

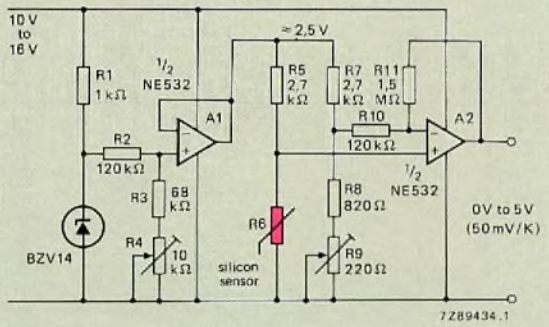


Fig.14 Simple bridge network for giving a temperature dependent signal between 0 V and 5 V within the temperature range 0 °C and 100 °C. Properly calibrated this setup can measure temperature with less than ±0,02 °C error

Circuit for a liquid crystal display

Figure 15 (overleaf) shows a system for indicating temperature by means of a liquid crystal display. The range of the system extends from −28 °C to +99 °C in increments of 0,1 K.

The circuit uses three BCD decade counters HEF4029B, each connected to a 7 segment LCD driver HEF4543B. The clock frequency for the counters (100 kHz) is produced by three inverters of an HEF4069UB inverter IC. The circuit includes an LM339 voltage comparator which is used to provide a pulse with a duration that depends on temperature.

Power for the circuit comes from a constant voltage source (4,2 V) via a switching transistor Tr_1. The latter is controlled by a 1 Hz pulse derived from an HEF4040B binary counter (128 Hz). This pulse also activates the counters, ensuring that power is delivered to the circuitry for only a brief period every second. This arrangement limits the total current drain to about 200 μA, permitting the equipment to be operated using only four 1,5 V penlight batteries.

Circuit operation

At the start of each 1 Hz pulse, counting begins and capacitor C charges via transistor Tr_2. A temperature dependent voltage V_T (derived from the silicon temperature sensor) is applied to pin 4 of the LM339, and a constant reference voltage V_g (greater than V_T) is applied to pin 7. As C charges, the voltage on pins 5 and 6 rises as shown in Fig.16(a), and produces (at pins 1 and 2) the pulses shown in Figs16(b) and 16(c) – and hence at point P, the pulse shown in Fig.16(d). The duration of this final pulse, which is proportional to temperature, is evaluated by the counters and displayed.

The counters are preset to −28 °C at the beginning of each measuring period (i.e. at the start of each 1 Hz pulse) and count backwards to 0 °C, after which they change over to forward counting. At the end of the measuring period, the count is displayed on the LCDs, a two segment display before the reading indicating whether the temperature is positive or negative. The display itself is driven by a 64 Hz signal derived from the HEF4040B binary counter.

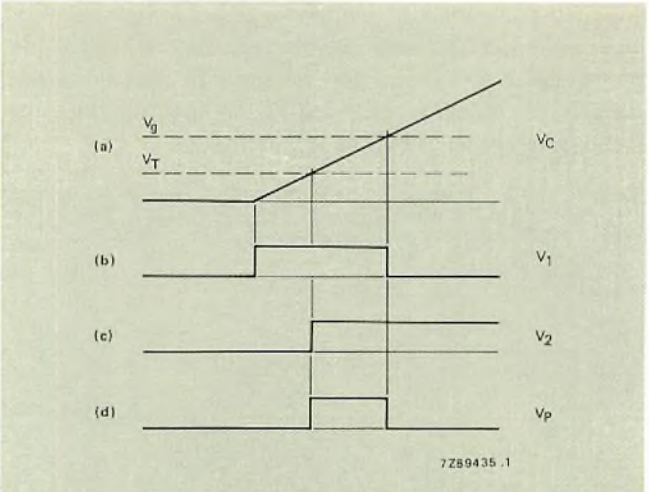


Fig.16 Pulse sequence set up in the circuit of Fig.15. The final pulse (Vp) has a duration proportional to the temperature. The HEF4029B decade counters are activated only over the duration of this pulse, so the count displayed by the LCDs provides a direct reading of the temperature

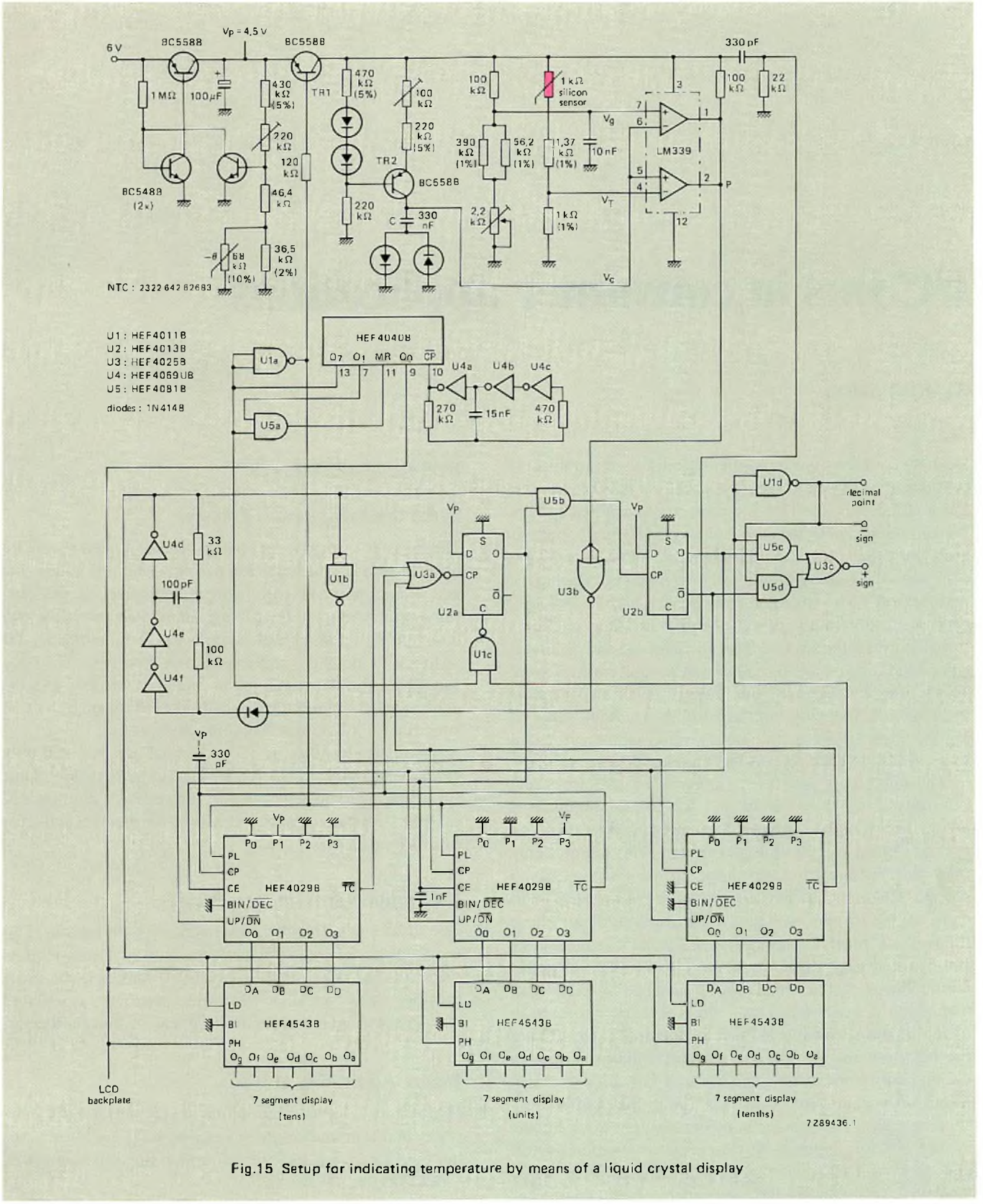


Fig.15 Setup for indicating temperature by means of a liquid crystal display

Note: a computer program to calculate the effects of tolerances and to ease linearization calculations can be made available on request.

I²C bus in consumer applications

A. MOELANDS

Much of today's consumer-oriented electronic equipment contains at least one controller, usually a microcomputer, and a number of standard and dedicated integrated circuits for storing and displaying data, and for performing digital and analogue circuit functions. There are, of course, many ways of linking the internal circuit assemblies and interfacing the peripheral ICs with the microcomputer(s), but it's obviously of great benefit to equipment designers and manufacturers if the control interface is simple, standardised and facilitates equipment upgrading or conversion to unit construction. This is why we developed our Inter IC (I^2C) bus and have included the hardware interface for it in a wide range of ICs for applications such as tv sets, video equipment, audio units, radios, telephones and automotive electronics.

The I^2C bus is structured for economy, efficiency and versatility. Since data throughput for control functions is low, it transfers the control data serially in either direction at a rate of up to 100 kbits per second. This requires only two wires; one for the data and one for the system clock, so few IC pins and only simple print-board wiring and inter-board connectors are needed. Consequently, it doesn't limit the scale of integration per IC package and it reduces costs and board space. Furthermore, the I^2C bus is a true multi-master bus so that control can be assumed by more than one of the ICs connected to it. To avoid loss or corruption of information, a unique address is allocated to each IC and the bus protocol incorporates an arbitration procedure to decide control priorities. When ICs with fast clocks communicate with others with slow ones, the protocol effectively synchronises the system clock by defining the clock source.

The I^2C bus supports a wide range of microcomputers and peripheral ICs manufactured in many different semiconductor technologies and, since engineers and equipment manufacturers find it a powerful tool for system design and product development, it's fast becoming accepted as an industry standard.

BUS REQUIREMENTS

Serial Bus Information Transfer

The transfer of digital data within the equipment should be by way of a 2-wire serial bus which consists of a data line and a clock line. This decreases interconnection costs because printed-circuit boards are simplified and only two interconnection wires are required where functions are far apart as in modular equipment. For example, when the tuning function in a tv set is on the main pcb, and the control function and display is on the front panel. Connector costs for inter-board links are also reduced.

Another advantage of a 2-wire serial bus is that it only requires two pins on the IC. This leaves more pins available for achieving a greater degree of integration within each IC or allows package costs to be reduced by permitting the use of smaller packages.

Bidirectional Information Transfer

The serial bus must permit bidirectional data transfer. This requirement follows directly from the functional requirements of the system. For example, in a tv set, a non-volatile memory which contains the channel numbers or preferred analogue settings must be both read and written via the bus.

Binary Addressing of ICs

Modules or ICs must each have a unique binary address because there is no enable line in a two-wire system. This leaves more I/O available on the controller for other purposes.

Acknowledgement of Reception

The bus system must allow the receiving device to acknowledge reception of a message. This enables checks to be

made on the transfer of data and allows a master controller to determine the configuration of the system under control.

Multi-master Operation

It is essential for the bus system to allow multi-master operation. A master device is one that can initiate a data transfer. Multi-master operation allows more than one device to assume control of the bus to start a transfer. However, an arbitration system must be incorporated to ensure that information is not lost or corrupted when more than one master tries to simultaneously control the bus.

With multi-master operation there is no need for a central master (usually a microcomputer) to control all the functions. This means that incorporation of additional features or conversion of the system to a modular form will not affect the original system. The extra controls and software are contained within an additional master-controller which is simply clipped onto the bus.

Whereas with single-master operation the central controller has to transmit data continually, the controllers in a multi-master system need only transfer data of mutual importance. This reduces the data carried on the bus and allows the bus to be used more efficiently. In a multi-master system, with its inherent distributed intelligence, real-time interrupts can be handled locally and therefore, interrupts need not affect the whole system.

Multi-master operation also simplifies diagnostic procedures during which an additional master can be temporarily connected to the bus to implement programming or alignment routines.

Low-priced Slave Interface Implementation

Another important requirement is that the bus system must allow inexpensive hardware implementation of a slave interface. A slave is a device controlled by the current master.

The cost of the hardware interface to the bus is of paramount importance because it applies to each IC connected to the bus. For example, the interface should not require an internal oscillator in the slave because it would be redundant for many functions.

Standardised Protocol

The bus protocol must be standardised to allow a modular build-up of software.

THE I²C BUS

Definition of I²C bus terminology

Transmitter – The device which sends data to the bus

Receiver – The device which receives data from the bus

Master – The device which initiates a transfer, generates clock signals and terminates a transfer

Slave – The device addressed by a master

Multi-master – More than one master can attempt to control the bus at the same time without corrupting the message

Arbitration – Procedure to ensure that if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.

The I²C bus meets all the previously described requirements:

- It is a 2-wire serial bus consisting of a clock and a data line.
- It allows bidirectional data transfer.
- It is a real multi-master bus which means that more than one device capable of controlling the bus can be connected to it. Each master generates its own clock.
- Each IC has a unique 7-bit address and can operate as a receiver or transmitter.
- ICs can be considered as masters or slaves when performing data transfers.
- An arbitration procedure prevents corruption or loss of data when masters are competing for use of the bus.
- The first byte of a transfer contains the 7-bit slave address. The least significant bit of this byte is a direction bit.
- Every byte transferred is acknowledged by the receiver.
- The slave interface implementation is simple and inexpensive.
- The protocol is standardised.

Another feature of the I²C bus is that any master can operate the bus at its own speed as long as it does not exceed 100 kbits/s. Consequently the data transfers are asynchronous and the clock is only generated by each master as long as it is in control of the bus. If more than one master attempts to gain control of the bus simultaneously, a system clock signal is derived from the clocks of the active masters.

The input levels of the I²C bus have been designed with a view to protecting the ICs against line transients. For example, in a tv set, series resistors of up to 300 Ω can be used to protect the ICs against high voltage spikes on the data and clock lines due to flash-over of a television picture tube.

The maximum number of devices which can be driven from the bus is only limited by the maximum bus capacitance of 400 pF. The bus can therefore be up to 3 or 4 metres long.

General Characteristics

The serial data (SDA) and serial clock (SCL) lines are both bidirectional. Each is connected to a positive supply voltage via a pull-up resistor (see Fig. 1). When the bus is free, both lines are HIGH. The output stages of ICs connected to the bus must have an open-drain or open-collector to perform the wired-AND function. The number of ICs than can be connected to the bus, and its length, are solely limited by the maximum bus capacitance of 400 pF.

Due to the variety of different technology devices (CMOS, NMOS, bipolar) which can be connected to the I²C bus, the levels of the logical '0' (LOW) and '1' (HIGH) are not fixed but depend on the supply voltage of the ICs (see ELECTRICAL SPECIFICATIONS OF INPUT AND OUTPUTS OF I²C DEVICES). One clock pulse is generated for each data bit transferred. Data can be transferred at up to 100 kbits/s.

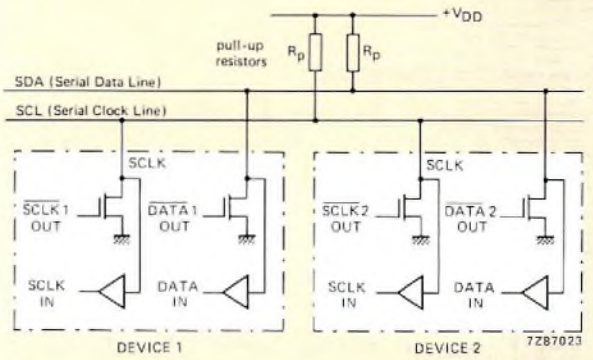


Fig.1 Connection of devices to the I²C bus

Data Validity

As shown in Fig.2, the data on the SDA line must be stable during the HIGH period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW (Fig. 2).

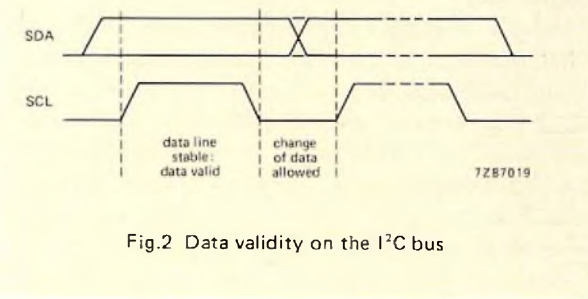


Fig.2 Data validity on the I²C bus

Start and Stop Conditions

As shown in Fig.3, a HIGH to LOW transition of the SDA line while SCL is HIGH indicates a start condition. A LOW to HIGH transition of the SDA line while SCL is HIGH is a stop condition. Start and stop conditions are always generated by the master. The bus is considered to be busy after the start condition. The bus is considered to be free again a certain time after the stop condition. This bus free situation will be described later in detail.

Devices connected to the bus can easily detect start and stop conditions if they possess the necessary interfacing hardware. However, microcomputers with no such interface have to sample the SDA line at least twice per clock period to sense the transitions.

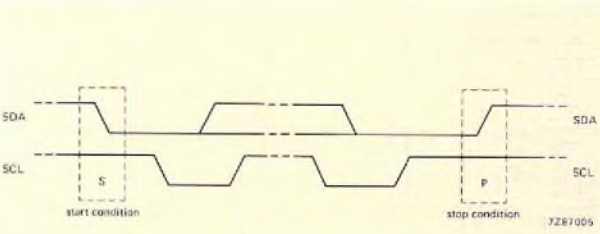


Fig.3 Start and stop conditions

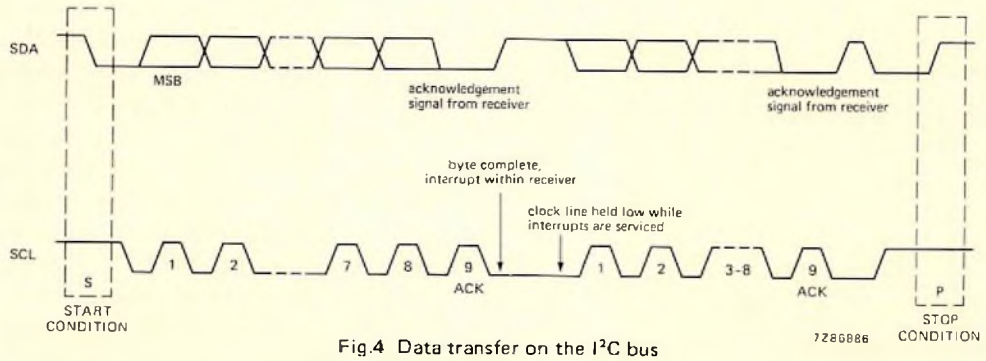


Fig.4 Data transfer on the I²C bus

Transferring Data

Byte Format. Every byte transferred on the SDA line must contain 8-bits. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge bit. As shown in Fig. 4, the most significant bit (MSB) is transferred first. If a receiving device cannot receive another complete byte of data until it has performed some other function, for example, serviced an internal interrupt, it can hold clock line SCL LOW to force the transmitter into a wait state. Transfer then continues when the receiver is ready for another byte and releases clock line SCL.

Acknowledge. The acknowledge-related clock pulse is generated by the current master. The transmitting device releases the SDA line (HIGH) during the acknowledge clock pulse. The receiving device must pull down the SDA line (LOW) during the acknowledge clock pulse so that the SDA line is stable LOW during this clock pulse (Fig. 5). Of course, set-up and hold times must also be taken into account. A receiver which has been addressed is usually obliged to generate an acknowledge after each byte has been received. When a slave receiver does not acknowledge its address, for example if it is not able to receive because it is performing some real-time function, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer.

If a slave receiver acknowledges its slave address, but some time later in the transfer cannot receive further data bytes, the master must again abort the transfer. This is indicated by the slave not acknowledging a data byte by leaving the data line HIGH. The master then generates the STOP condition.

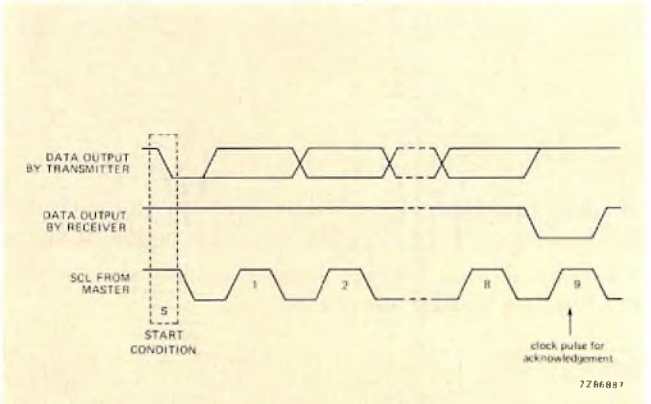


Fig.5 Acknowledgement on the I²C bus

If a master receiver is involved in a transfer, it must signal an end of data to the slave transmitter by not acknowledging the last byte from the slave transmitter. The slave transmitter must then release the data line to allow the master receiver to generate the stop condition.

Clock Generation and Arbitration

Synchronisation. All masters generate their own clock on the SCL line during transfer of data. Data is only valid during the clock HIGH period. A defined clock is therefore needed to allow the bit-by-bit arbitration procedure to take place. Clock synchronisation is performed using the wired-AND connection of devices to the SCL LINE. As shown in Fig. 6, a HIGH to LOW transistion on the SCL line causes all competing devices to count off their LOW periods and the SCL line is held low until the device with the longest LOW period finishes its count. Devices with shorter LOW periods remain in a HIGH wait state during this time. When all devices concerned have counted off their LOW periods, the clock line is released and goes HIGH. There is then no difference between the state of the device clocks and the state of the SCL line, and all devices start counting their HIGH periods. The first device to complete its HIGH period count pulls the SCL line LOW. In this way, a synchronised SCL clock is generated, the LOW period of which is determined by the device with the longest clock LOW period and the HIGH period of which is determined by the device with the shortest clock HIGH period.

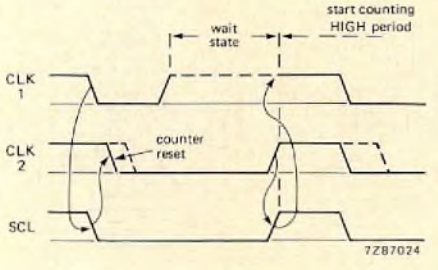


Fig.6 Clock synchronisation during the arbitration procedure

Arbitration. Arbitration ensures that a master which transmits a HIGH level on the SDA line while another master transmits a LOW level, will switch off its DATA output stage because the level on the bus does not correspond to its own level. Arbitration can continue during many bits. The first stage of arbitration is the comparison of the address bits. If the masters are addressing the same device, arbitration compares the data bits. Because address and data information is used for the arbitration, it does not delay the transfer of information.

A master which loses the arbitration can generate clock pulses until the end of the byte in which it lost the arbitration. If a master loses arbitration during the addressing procedure, it is possible that the winning master is trying to

address it. The losing master must therefore switch over immediately to its slave receiver mode.

Figure 7 shows the arbitration procedure for two masters. Of course more masters may be involved. As soon as the master generating DATA 1 generates an internal HIGH level whilst the data on the SDA line is LOW, it switches its output off so that the master generating DATA 2 wins the arbitration and its output continues to be transferred on the SDA line. Since arbitrations are decided solely on the basis of addresses and data transmitted by competing masters, there is no central master, or any order of priority on the bus.

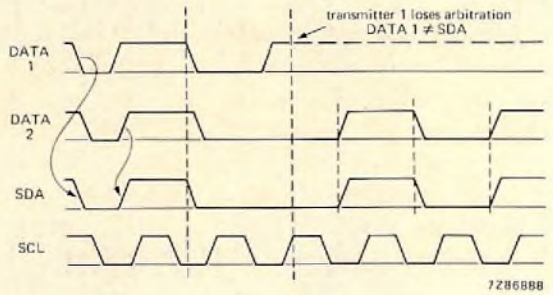


Fig.7 Arbitration procedure for two masters

Use of the Clock Synchronising Mechanism as a Handshake. In addition to being used during the arbitration procedure, the clock synchronisation mechanism can be used to enable receiving devices to cope with fast data transfers, either on a byte or bit level.

On the byte level, a device may be able to receive data bytes at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slave devices can then hold the SCL line LOW, after reception and acknowledgement of a byte, to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure.

On the bit level, a device such as a microcomputer without a hardware I²C interface on-chip can slow down the bus clock by extending each clock LOW period. In this way, the speed of any master is adapted to the internal operating rate of this device.

Formats

The data transfer format is shown in Fig. 8. After the start condition, a 7-bit slave address is transmitted and followed by a data direction bit ($R/\overline{W}$); a '0' indicates WRITE, a '1' indicates READ. A data transfer is always terminated by a stop condition generated by the master. However, if a master still wishes to communicate on the bus, it can generate another start condition, and address another slave without first generating a stop condition. Various combinations of read/write formats are then possible within such a transfer. Possible data transfer formats are:

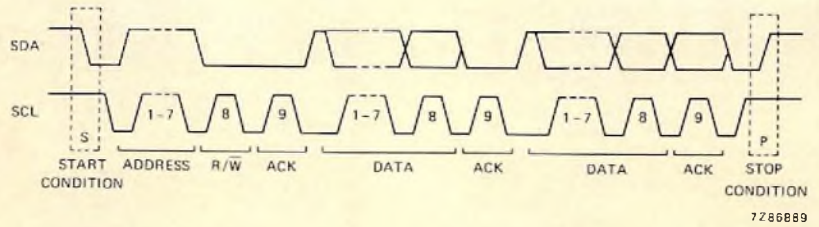
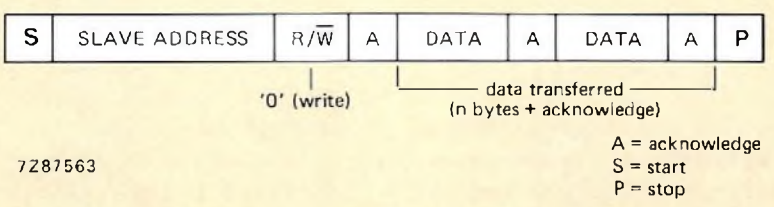
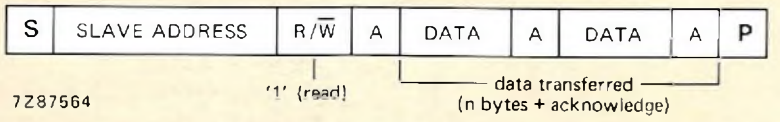


Fig.8 A complete data transfer

(a) Master transmitter transmits to slave receiver. Direction is not changed.

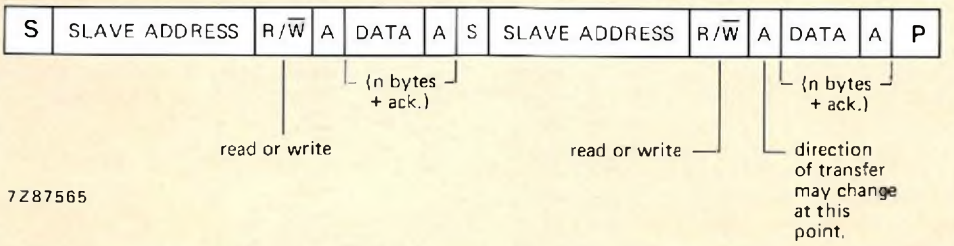


(b) Master reads slave immediately after first byte.



At the moment of the first acknowledge, the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter. This acknowledge is still generated by the slave. The stop condition is generated by the master.

(c) Combined formats.



During a change of direction within a transfer, the start condition and the slave address are both repeated, but with the R/$\overline{W}$ bit reversed.

Notes:

1) Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the start condition is repeated, data can be transferred.
2) All decisions on auto-increment or decrement of previously accessed memory locations etc. are made by the designer of the device.
3) Each byte is followed by an acknowledge as indicated by the A blocks in the sequence.
4) I²C devices have to reset their bus logic on receipt of a start condition such that they all anticipate the sending of a slave address.

Addressing

The addressing procedure for the I²C bus is such that the first byte after the start condition determines which slave will be selected by the master. Usually, this first byte follows that start condition. The exception is the 'general call' address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge, although devices can be made to ignore this address. The second byte of the general call address then defines the action to be taken.

Definition of Bits in the First Byte. The first seven bits of this byte are the slave address (Fig.9). The eighth bit (LSB – least significant bit) determines the direction of the message. A '0' in the least significant position of the first byte means that the master will write information to a selected slave; a '1' in this position means that the master will read information from the slave.

When the address is sent, each device connected to the bus compares the first 7 bits after the start condition with its own address; if there is a match, the device considers itself addressed by the master as a slave receiver or slave transmitter, depending on the R/$\overline{W}$ bit.

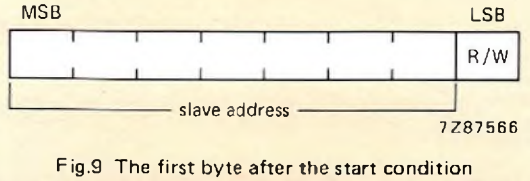


Fig.9 The first byte after the start condition

Since identical ICs may be used more than once in a system the slave address can be made up of a fixed part and a programmable part. The number of programmable address bits depends on the number of pins available. For example, if a device has 4 fixed and 3 programmable address bits, a total of eight identical devices can be connected to the same bus.

General call address. The general call address is used to address every device connected to the I²C bus. However, if a device does not need any of the data supplied within the general call structure, it can ignore this address. If a device does require data from a general call address, it will behave as a slave receiver. The second and following bytes will be acknowledged by every slave receiver capable of handling this data. A slave which cannot process one of these bytes must ignore it by not acknowledging. The meaning of the general call address is always specified in the second byte (Fig. 10).

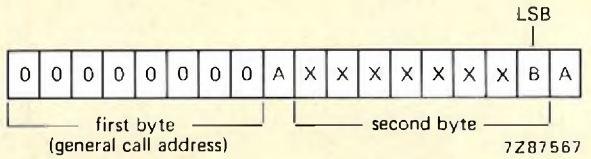


Fig.10 Generall call address format

ELECTRICAL SPECIFICATIONS OF INPUTS AND OUTPUTS OF I²C DEVICES

The I²C bus allows communication between devices made in different technologies which might also use different supply voltages. For devices operating on a supply voltage of 5 V ± 10%, the input levels are:

V_{ILmax} = 1,5 V (maximum input LOW voltage)
V_{IHmin} = 3,0 V (minimum input HIGH voltage)

Devices operating on a supply voltage different from 5 V (e.g. bipolar), must also have these input levels.

For devices operating over a wide range of supply voltages (e.g. CMOS), the input levels are:

V_{ILmax} = 0,3 V_{DD} (maximum input LOW voltage)
V_{IHmin} = 0,7 V_{DD} (minimum input HIGH voltage)

For both groups of devices, the maximum output LOW level is:

V_{OLmax} = 0,4 V (maximum output LOW voltage at 3 mA sink current).

Devices with fixed input levels can each have their own power supply of 5 V ± 10%. Pull-up resistors can be connected to any supply as shown in Fig. 11. However, the devices with input levels related to V_{DD} must have one common supply line to which the pull-up resistor is also connected (Fig. 12).

When devices with fixed input levels are mixed with devices with V_{DD} related levels, the latter devices must be connected to one common supply line of 5 V ± 10% along with the pull-up resistors (Fig. 13).

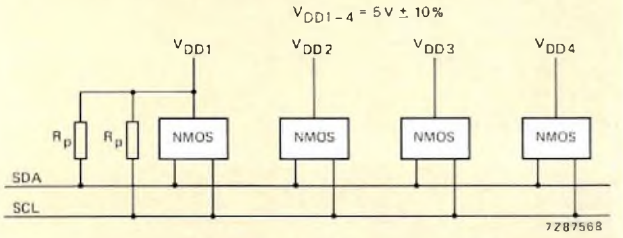


Fig.11 Connection of fixed input level devices to the I²C bus

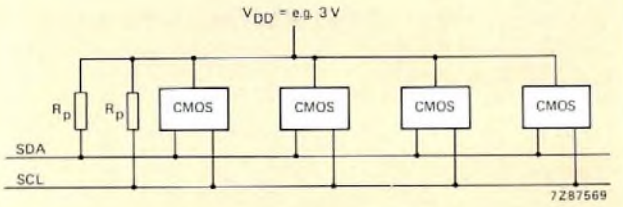


Fig.12 Connection of devices with a wide supply voltage range to the I²C bus

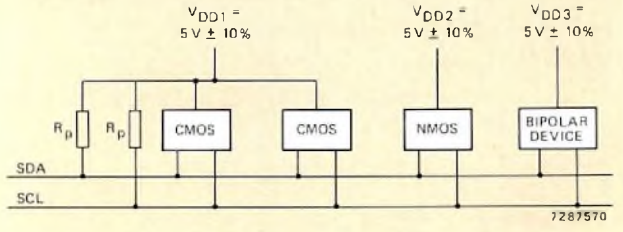
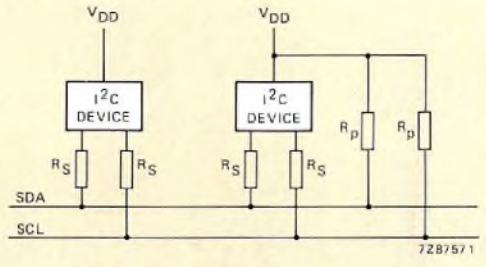


Fig.13 Connection of a mixture of devices with fixed input levels and devices with supply voltage related input levels to the I²C bus

Input levels are defined in such a way that:

- The noise margin on the LOW level is 0,1 V_{DD}.
- The noise margin on the HIGH level is 0,2 V_{DD}.
- Series resistors (R_S) up to 300Ω can be used for protection against high voltage spikes on the SDA and SCL line due, for example, to flash-over of a tv picture tube (Fig.14).

The maximum bus capacitance per wire is 400 pF. This includes the capacitance of the wire itself and the capacitance at the pins connected to it.



•Fig.14 Series resistors for protecting ICs against high-voltage transients

TIMING

The clock on the I^2C bus has a minimum LOW period of 4,7 μs and a minimum HIGH period of 4 μs. Masters can generate a bus clock with a frequency up to 100 kHz.

All devices connected to the bus must be able to follow transfers with frequencies up to 100 kHz, either by being able to transmit or receive at that speed or by applying the clock synchronisation procedure which will force the master into a wait state and stretch the LOW periods. Of course, in the latter case the frequency is reduced.

FURTHER INFORMATION

Further information is available in the I^2C bus specification, ordering code 9398 615 00011.

High-voltage power transistor quality

J. DIJK

Our range of high-voltage power transistors has been developed to cover all the major areas of application: switched-mode power supplies, TV and VDU deflection, electronic ignition, mains inverters and electronic motor control. Rigorous Quality Control and the most advanced fabrication technologies achieve the high built-in quality essential if modern requirements are to be met.

Here we give the results of over 10 million device-hours testing of our high-voltage power transistors, carried out as part of routine Quality Control over a three-year period. This includes over 12 million device-cycles of thermal-fatigue testing (power cycling). The results obtained indicate a maximum failure rate at maximum ratings of about 10^{-6}/h with 60% confidence.

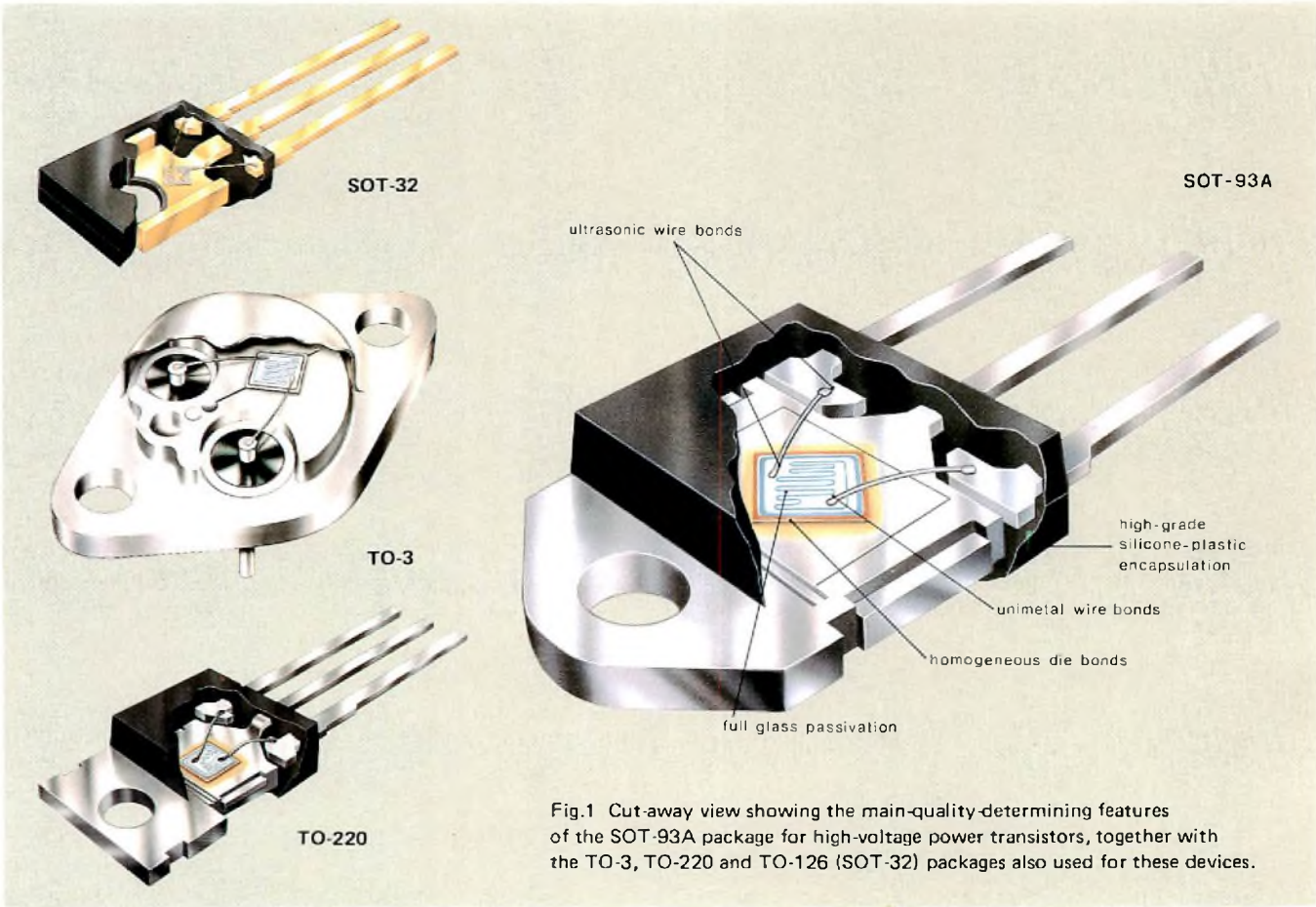


Fig.1 Cut-away view showing the main-quality-determining features of the SOT-93A package for high-voltage power transistors, together with the TO-3, TO-220 and TO-126 (SOT-32) packages also used for these devices.

This publication gives quality data, both conformity and reliability, for the range of high-voltage power transistors in Table 1. Symbols for quantities used are those in our Data Handbook and are based on the recommendations of IEC Publication 148. Ratings are defined in accordance with IEC Publication 134; reliability definitions are those of IEC Publication 271.

TABLE 1
High-voltage power transistor types discussed in this note

type no.	package	V_{CEO} max (V)	P_{tot} max (W)	h_{FE}
BU426	SOT-93	375	70	30 (typ.)
BUX80*	TO-3	400	100	30 (typ.)
BUS11/11A	TO-3	400/450	100	17 (typ.)
BUS12/12A	TO-3	400/450	125	17 (typ.)
BUS13/13A	TO-3	400/450	175	17 (typ.)
BUS14/14A	TO-3	400/450	250	17 (typ.)
BU508A	SOT-93A	700	125	>2,5
BU208A*	TO-3	700	80	>2,5

* Maintenance types.

FOUNDATIONS OF QUALITY

Specifying quality

Quality is the fitness for use of a product and so has two essential attributes: fitness for use initially, conformance to specification, or conformity; fitness for use for a period of time, reliability. The practical measure of conformity can be either AQL (in %) or reject level (in ppm – parts per million). Reliability is generally expressed in terms of failure rate. The usual unit is failures per million device-hours testing.

Both conformity and reliability data for batches of new devices are necessarily predictions, based on measurements carried out on samples, reinforced by experience of identical production. Such quality data, to be realistic, need to be supported by a confidence level: a statement of the probability that the data will apply to the bulk production from which the samples were taken. For AQLs, the confidence level depends on the inspection level. For ppm reject levels, the confidence level depends on the number of devices involved. Observed failure rates are adjusted (increased) so that a predetermined confidence level applies, usually 60%.

Applying quality

Quality experienced by an OEM (Original Equipment Manufacturer) in equipment production and service depends on the proper application of high-quality components. With specialized devices like high-voltage transistors this is especially important. Manufacturer's recommendations for operating conditions should be followed closely, particularly with regard to heatsinking, SOAR and, especially, base-drive conditions. Cooperation between device manufacturer and OEM on device specification and application usually results in improved quality experienced in finished equipment.

Testing is not enough

Testing alone cannot ensure high product quality. The maintenance of high quality, or the progressive improvement in quality that circumstances now demand, requires that the results of testing and the analysis of rejects are fed back so that corrective action can be taken to eliminate design faults and deviations in processing conditions. Ideally, OEM and service experience of the product should be included in this feedback loop so that quality optimization is application oriented.

Quality must be built in

In order to achieve high quality in our high-voltage power transistors, we involve the Quality Department at the earliest possible stage in the development of a new device. Process technology and materials are selected to provide the maximum quality in the intended application. Evaluation of preproduction samples by the Quality Department ensures that design quality requirements are met before full-scale production is approved.

Once in production, zero-defect-oriented line inspection and quality-control gating ensure that only good devices pass for further processing. Our new glass-passivation technology for high-voltage transistors allows on-slice testing: a valuable aid to line inspection.

Following the 100% final electrical test – which includes a fast thermal-resistance measurement to check die-bond integrity and, thus, SOAR performance – all batches are routed to the Quality Department for Acceptance Testing. Samples are taken and subjected to a wide variety of tests that monitor all aspects of device quality. Parameter checks reinforce and prove the final electrical tests. Mechanical and climatic tests explore the structural integrity of the devices and their resistance to environmental conditions. Finally, endurance tests carried out under Absolute-Maximum Rating conditions probe device reliability.

Normal endurance test durations are 168 h, to measure early-failure level, and 1000 h. Some tests are prolonged for up to 10 000 h to check the validity of the shorter-test results. It is the accumulated information from three years Acceptance Testing that forms the basis of this publication.

DEVICE TECHNOLOGIES

Die attach is by alloy bonding; controls during manufacture, and the 100% fast thermal-resistance measurement, ensure that bond uniformity is good. A stable, homogeneous bond is essential for reliable SOAR performance. As will be seen, reliability of these devices during thermal fatigue (power cycling) testing is excellent.

Devices such as the BU508A in the SOT-93A package shown in Fig.1 incorporate a fully glass-passivated chip. The same technique is used for all high voltage devices, both in plastic and metal envelopes. The two constructions are shown in Fig.2.

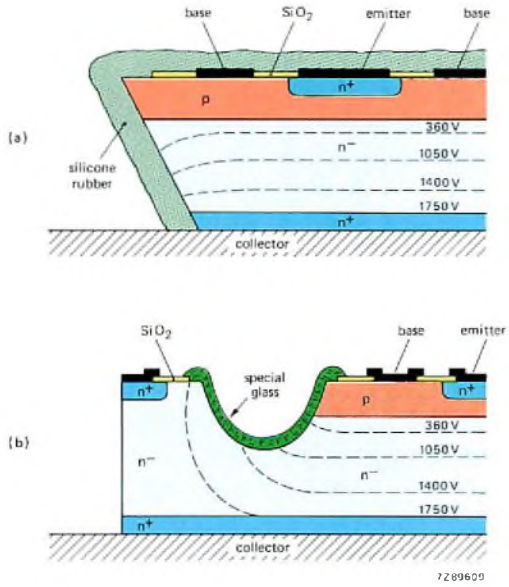


Fig.2 Two technologies employed in our range of high-voltage power transistors: (a) the older bevelled die with silicone-rubber coating; (b) the new glass-passivated construction.

AQL

During Acceptance Testing, samples are measured to establish that conformity is within the set AQLs. The process-average reject level of our high-voltage power transistors is, actually, well below economically-determinable AQLs, and we use AQL mainly as an internal quality threshold. However, devices are, of course, available to these AQLs, which are given in Table 2.

Spreads

Quality Control Acceptance Testing also includes the measurement of all published device parameters. These measurements both check the final electrical test itself, and indicate the accuracy of processing conditions. Where trends or discrepancies are observed, details are fed back to production so that corrective action can be taken.

Spreads of $V_{CE\,sat}$, $V_{(BR)CES}$, t_f, h_{FE} and $R_{th\,j\text{-}mb}$ measured during Acceptance Testing are given in the Appendix.

TABLE 2
Our standard AQLs for high-voltage power transistors

Note: definitions and methods are those of MIL-STD-105D and IEC Publication No. 410.

inspection criterion	AQLs (%)		inspection level
	individual	combined	
mechanical/visual			
major dimensions	0,65		S2
other dimensions	6,5		S2
appearance		2,5	II
marking	2,5		
electrical characteristics			
major	0,4	0,65	II
other	1		II
inoperatives			
electrical + visual	0,1		II
wrong marking	0,1		II
illegible marking	0,25		II

STRUCTURAL INTEGRITY

Device structural integrity is probed by the Quality Department during Acceptance Testing by means of a series of mechanical and environmental tests. These tests are designed to explore all aspects of the mechanical construction and workmanship of our high-voltage power transistors. Where defects are revealed, information is fed back to the manufacturing units for corrective action.

Test methods

Hermetic (metal, TO-3) devices are subjected to the following test sequence.

- Visual inspection.
- Hermeticity: devices are immersed in alcohol for 16 h at a pressure of 500 kPa (5 atmospheres).
- Soldering heat: device leads are immersed in a solder bath at 300 °C to within 1 mm of the body for 10 s.
- Temperature cycling: 30 minutes at −65 °C followed by 30 minutes at $T_{j\,max}$ with a transition time less than 2 minutes; 5 cycles.
- Electrical measurement according to type.

Plastic-encapsulated devices (SOT-32, TO-220, SOT-93 and SOT-93A packages) are subjected to the following test sequence.

- Visual inspection.
- Soldering heat: device leads are immersed in a solder bath at 300 °C to within 5 mm of the body for 11 s.
- Moisture resistance: 10 cycles in which relative humidity and temperature vary from 95% at 25 °C to 55% at 65 °C over 24 h.
- Temperature cycling: 15 minutes at −65 °C followed by 15 minutes at +150 °C; 10 and 100 cycles.
- Drop test: devices are dropped 75 cm onto a hard surface 3 times.
- Electrical measurement according to type.

Table 3 gives the failure criteria for Complete failures as defined in IEC Publication No. 271, for our range of high-voltage power transistors in this test sequence.

TABLE 3

Definitions of complete failure for high-voltage power transistors measured during and after mechanical and environmental testing and endurance testing

characteristic	complete failure limit
$V_{CE\,sat}$, V_{EBO}, V_{CBO}	twice published limit or flutter
I_{CBO}, I_{CEX}	ten times published limit at $V_{CB\,max}$ and high temperature, or, if less, a value less than that which could cause thermal runaway
I_{EBO}	ten times published limit at $V_{EB\,max}$ and high temperature
$R_{th\,j\text{-}mb}$	twice published limit
mechanical	broken leads, cracks in envelope and, for metal envelopes, lack of hermeticity.

Test results

Table 5 (Appendix) gives the Complete failures detected during Mechanical and Environmental Acceptance Testing of our high-voltage power transistors for the period 1980 to 1982.

ACKNOWLEDGEMENT

The author wishes to acknowledge the assistance of his colleagues F. Geertsen, A. D. Tuinhof (Nijmegen), S. Bruneteau D. Henri (Caen) and M. Shu (Hong Kong) in compiling the information for this article.

TABLE 4

Analysis of early-failure and failure-rate data from Tables 7 and 8

Note: all data corrected to a confidence level of 60%.

device type	early failures at maximum ratings	failure rates at maximum ratings	
		(1000 h tests)	(> 1000 h tests)
BU208A*	<0,1%	$1{,}3 \times 10^{-6}$	$0{,}7 \times 10^{-6}$
BU426A	0,63%	$2{,}2 \times 10^{-6}$	$8{,}2 \times 10^{-6}$
BUX80*	<0,1%	$3{,}6 \times 10^{-6}$	$3{,}5 \times 10^{-6}$
BUS 11 to 14	0,14%	$3{,}75 \times 10^{-6}$	new types:
BU508A	0,3%	$1{,}7 \times 10^{-6}$	no data

* maintenance types.

TABLE 5

Results of mechanical and environmental tests performed on our high-voltage power transistors by Quality Control during the period 1980 to 1982

type	1980		1981		1982	
	sample	failure	sample	failure	sample	failure
BU208A*	360	0	250	0		
BU426	900	1	900	2	440	1
BUX80*	360	0	120	0	400	0
BUS11 to 14	180	2	300	1	260	0
BU508A	–	–	300	1	400	0

* maintenance types.

Note: failures are complete failures as defined in Table 3.

RELIABILITY

The reliability of our high-voltage power transistors is monitored during Acceptance Testing by endurance tests of 168 h and 1000 h duration, supplemented by further tests of duration up to 10 000 h. These tests are generally conducted at Absolute Maximum ratings, as defined in IEC Publication No. 134 and given in our Data Handbook.

The tests programme is designed to expose weakness in device design or construction. Failures are analysed and data fed back for corrective action. Failures observed at 168 h are predominantly early failures, due to faulty construction. The period 168 h to 1000 h is the beginning of the constant-failure period and yields results that are a suitable basis for reliability prediction. Where possible, results from endurance testing are compared with and supplemented by field experience for reliability-prediction purposes.

TABLE 6
Endurance test conditions for our range of high-voltage transistors

test description	parameter	type							
		BU208A	BU508A	BU426	BUX80	BUS11/11A	BUS12/12A	BUS13/13A	BUS14/14A
dissipation	P_{tot}	8 w	20 W	50 W	60 W	36 W	46 W	56 W	66 W
	I_E	80 mA	2 A	2 A	2 A	2 A	2 A	2 A	2 A
	T_{mb}	25 °C	25 °C	70 °C	60 °C	90 °C	90 °C	90 °C	90 °C
thermal fatigue	I_E	6 A	6 A	6 A	10 A	5 A	8 A	12 A	24 A
	P_{tot}	10 W	10 W	10 W	15 W	10 W	15 W	20 W	40 W
	T_{amb}	25 °C	25 °C	25 °C	25 °C	25 °C	25 °C	25 °C	25 °C
	t_{on}	2 min	2 min	2 min	2 min	2 min	2 min	2 min	2 min
	t_{off}	4 min	4 min	4 min	4 min	4 min	4 min	4 min	4 min
d.c. cut-off	V_{CB}	750 V	750 V	500 V	400 V	400 V	400 V	400 V	400 V
	T_{mb}	100 °C	125 °C	125 °C	125 °C	150 °C	150 °C	150 °C	150 °C
a.c. cut-off	V_{CBM}	1500 V	1500 V	800 V	800 V	800 V	800 V	800 V	800 V
½ cycle a.c. 50 Hz	T_{amb}	100 °C	125 °C	125 °C	125 °C	150 °C	150 °C	150 °C	150 °C
tropical d.c. cut-off	V_{CE}		500 V	49 V	–	–	–	–	–
	V_{EB}		1 V	1 V					
	T_{amb}		55 °C	55 °C					
	RH		95%	95%					
forward current	I_E	7 A		6 A	15 A	combined with thermal fatique			
	T_{MB}				80 °C				
high temperature storage	T_{amb}	115 °C	150 °C	125 °C	125 °C	200 °C	200 °C	200 °C	200 °C
low temperature storage	T_{amb}	−65 °C	−65 °C	−65 °C	−65 °C	−65 °C	−65 °C	−65 °C	−65 °C
practical circuit	V_{CEM}	1350 V	–	–	–	–	–	–	–
	I_{CM}	4,5 A							
f = 15625 Hz	T_{amb}	55 °C							
d.c. cut-off	V_{EB}	5 V	5 V	7 V	7 V	7 V	7 V	7 V	7 V
	T_{amb}	125 °C	125 °C	125 °C	125 °C	125 °C	125 °C	125 °C	125 °C

TABLE 7

Results from 168 h and 1000 h endurance tests on our high-voltage power transistors during the period 1980 to 1982

test per device type	1980				1981				1982			
	168 h		1000 h		168 h		1000 h		168 h		1000 h	
	N	CF	N	CF	N	CF	N	CF	N	CF	N	CF
BU426												
dissipation	–	–	–	–	–	–	20	0	–	–	30	0
thermal fatigue	460	1	60	1	100	0	–	–	40	0	270	0*
d.c. cut-off	460	4	80	0	400	0	190	2	–	–	390	0
a.c. cut-off	460	10	80	0	390	0	180	0	10	0	140	0
high themperature storage	–	–	70	0	–	–	70	0	–	–	20	0
low temperature storage	20	0	20	0	20	0	20	0	–	–	30	0
tropical cut-off	20	0	20	0	20	0	20	0	–	–	40	0
cut off V_{EB} (DC)	–	–	–	–	–	–	80	0	–	–	40	0
BU508A												
dissipation					–	–	70	0	–	–	20	0
thermal fatigue					20	0	30	1	50	1	60	0*
											30	0
d.c. cut-off					120	0	120	0	10	0	170	0
a.c. cut-off					100	0	180	0	20	0	170	0
high temperature storage					–	–	50	0	–	–	20	0
low temperature storage					–	–	50	0	–	–	20	0
tropical cut-off							20	0	–	–	70	0
cut off V_{EB}(DC)							20	0	–	–	20	0
BUS11 to 14												
dissipation	–	–	10	0	–	–	70	0	–	–	30	–
thermal fatigue	10	0	–	–	100	1	–	–	110	1	–	–
d.c. cut-off	140	0	50	0	310	0	120	0	110	0	90	0
a.c. cut-off	150	0	40	0	310	0	130	1	100	0	100	1
high temperature storage	10	0	10	0	–	–	70	1	–	–	80	0
low temperature storage	–	–	20	0	–	–	70	0	–	–	70	0
cut off V_{EB}	–	–	–	–	–	–	120	0	–	–	40	0
BU208A												
dissipation	–	–	–	–	–	–	20	0				
thermal fatigue	–	–	20	–	–	–	70	0				
d.c. cut-off	420	0	80	0	290	0	30	0				
a.c. cut-off	400	0	100	0	290	0	50	0				
high temperature storage	20	0	20	0	20	0	20	0				
low temperature storage	20	0	20	0	10	0	10	0				
practical circuit	70	0	70	0	60	0	60	0				
cut off V_{EB} (DC)	–	–	–	–	–	–	80	0				
BUX80												
dissipation	–	–	–	–	–	–	–	–				
thermal fatigue	–	–	–	–	–	–	–	–				
d.c. cut-off	180	0	80	0	70	0	30	0				
a.c. cut-off	180	0	50	0	70	0	30	0				
high temperature storage	20	0	20	0	10	0	10	0				
low temperature storage	20	0	20	0	10	0	10	0				
cut off V_{EB}												

* 3 week test duration.

Endurance tests

Table 6 (Appendix) gives the endurance-test conditions for our high-voltage power transistors. In each set of conditions, there is generally at least one that corresponds to an Absolute Maximum Rating for the device in question. Operation at stress levels that correspond to Maximum Rated conditions not only minimizes the test duration (without introducing the complications associated with over-stressed accelerated testing) but also ensures that any failure mechanisms associated with the device technology within its design operating conditions are exposed.

Thus, each test is designed to explore a specific aspect of device construction. Thermal-fatigue testing exposes any weak dice, or die and wire bonds. Operation at cut-off reveals potential instabilities of die surface or passivation. Tropical cut-off explores the tendency to corrosion of plastic-encapsulated devices. Dissipation checks other high-temperature tests, and indicates failure rate at maximum power operation. High temperature storage checks bond and encapsulation stability.

Test durations are generally 168 h (1 week) and 1000 h (6 weeks). Most early failures occur within the first week of operation under maximum-rated conditions: the period 168 h to 1000 h thus corresponds to the beginning of the constant-failure period. Tests are occasionally prolonged for up to 10 000 h to check these assumptions, and to establish the validity of data from the shorter tests.

Endurance test results

Table 7 (Appendix) gives the results obtained from endurance tests performed as part of Quality Department Acceptance Testing of our high-voltage power transistors during the period 1980 to 1982; test durations are 168 h and 1000 h. Both yearly and total results are given. Although only complete failures are given in Table 7 (Appendix), three lower categories of failure are recognized and recorded during endurance testing: Major and Minor Partial failures, and Stability failures. These not only allow for a greater insight into the long-term behaviour of devices in service, but also provide an early warning of potential problems in production.

The results given are those from all batches submitted for Acceptance Testing, including some batches which were not cleared for delivery. Thus, the early failure proportion and failure rates derived from these results are rather less favourable than those to be expected from delivered batches.

The way in which routine endurance testing can lead to process improvements is well illustrated by the test results for the BU426 in Table 7. The 1980, 168 h, results for both a.c. and d.c. cut off tests show a number of failures. From 1981 onwards these failures disappear. This is due to the introduction of a production-line leakage-current test performed at 400 V. Not only are far fewer leakage-prone devices produced, but data from this testing has been used to improve the passivation.

Early failures and failure rates

Table 4 gives the early-failure percentage for the 168 h tests, and the overall failure rates from the 1000 h tests reported in Table 7; failure rates derived from the longer-duration tests reported in Table 8 are included for comparison.

Overall, the failure rates are comparable with those for low-voltage power transistors at Absolute Maximum Rating operation as reported in Ref. 1 and 2. Detailed examination of Tables 7 and 8 shows that plastic-encapsulated devices with gold-silicon eutectic die bonds showed no failures after between 1.2 and 2 million device-cycles testing. Moreover, the tight process controls applied to the alloy die bonds resulted in instances of zero failures in up to 1.4 million device-cycles testing.

TABLE 8

Results of endurance tests of greater than 1000 h duration on our high-voltage power transistors during the period 1977 to 1981

test	BU208A		BU426		BUX80	
	Nt*	CF	Nt	CF	Nt	CF
dissipation I	120	0			80	0
dissipation II					80	0
thermal fatigue	80	0	80	2	60	1
	90	15*				
cut off d.c.	120	0	240	1	20	0
cut off a.c.	120	0	240	3	20	0
tropical d.c.			100	0		
forward current	60	0			80	0
high temperature storage	530	0	240	0	230	0
practical circuit	160	0				

* test extended to end of useful life (various failures).

Not counted in failure rate calculations.

Reliability in service

The conditions under which our high-voltage power transistors are tested are such that the results obtained can be used as the basis for the prediction of reliability under normal service conditions. In essence, the method of prediction is to correct the failure rate obtained from endurance testing by factors that reflect the difference in stress levels between test and service conditions.

In practice, a number of derating factors are used, depending on the type of application and service environment. A system of failure-rate determination using a large number of these factors is given in MIL-HDBK-217C. A good insight into the probable failure rate in normal industrial or consumer applications can be obtained by considering temperature and operating voltage only. Temperature determines the rate at which failure mechanisms develop, according to Arrhenius' Law; operating voltage accelerates the development of die surface instabilities or the migration of any ionic impurities trapped in the passivation.

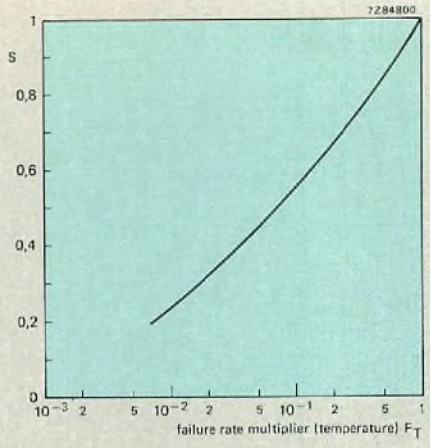


Fig.3 Temperature failure-rate multiplier F_T as a function of stress level $S = (T_j - 25)/(T_{j\,max} - 25)$ for our high-voltage power transistors

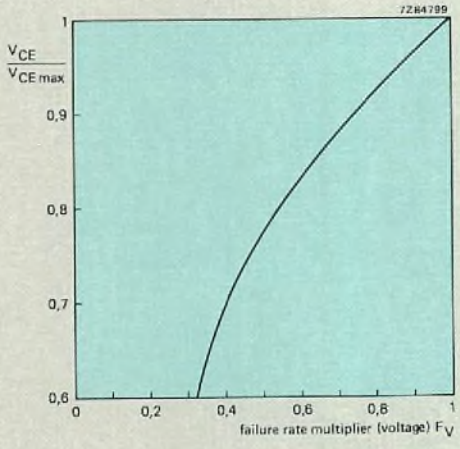


Fig.4 Operating voltage failure-rate multiplier F_V as a function of $V_{CE}/V_{CE\,max}$, where V_{CE} is the operating voltage and $V_{CE\,max}$ the rated voltage

Figure 3 shows temperature failure-rate factor F_T as a function of stress level

$$S = (T_j - 25)/(T_{j\,max} - 25).$$

This curve has been derived from laboratory measurements and field experience, and corresponds broadly to a failure-rate activation energy of 0,7 eV for devices of maximum operating junction temperature $T_{j\,max}$ in the region 100 °C to 150 °C.

Figure 4 gives voltage failure-rate factor F_V as a function of operating V_{CE} divided by rated V_{CE}. The curve gives results similar to MIL-HDBK-217C, Table 2.2.1-5.

High-voltage power transistors are generally operated fairly close to their maximum ratings. For example, the BUX80, $V_{CEO\,max} = 400$ V, is generally used in switched-mode power supply applications operating from rectified 220 V a.c. mains with an applied V_{CE} of about 310 V. The rated junction temperature is 150 °C, and operation at junction temperatures of 115 °C is common.

From these data,

$$S = 90/125 = 0{,}72$$

and $V_{CE}/V_{CEO\,max} = 310/400 = 0{,}775$. Figures 3 and 4 give $F_T \approx 0{,}2$ and $F_V \approx 0{,}5$, an overall failure rate multiplying factor of 0,1 for the application. Since the failure rate from the 1000 h endurance tests was $3{,}6 \times 10^{-6}$/h at 60% confidence, Table 8, a failure of about $0{,}36 \times 10^{-6}$/h (at 60% confidence) can be expected in the application quoted.

REALIZING QUALITY POTENTIAL

Two aspects of quality most concern the OEM: the reject rate in new equipment, which affects the fall-off rate; and the failure rate during the guarantee period, which affects the call rate. The level of quality of our high-voltage power transistors is now such that the major factor determining the quality realized in finished equipment is more a function of the application conditions than the devices themselves.

Due to both their complex structure and high operating stresses, high-voltage power transistors are more sensitive to application conditions than the majority of discrete semiconductors. It is thus essential, if maximum quality is to be experienced with them, that

- operation under worst probable conditions remains both electrically and thermally within the manufacturer's specified limits
- regard must be had for the effect of surges and transients on operating conditions, and that the effect of failure of adjacent components should be considered
- where doubt exists, the device manufacturer should be consulted about the suitability of the device for a specific application.

Consultation between device manufacturer and OEM at all stages in the design and production of equipment containing high-voltage transistors will almost certainly improve real quality and so reduce production costs.

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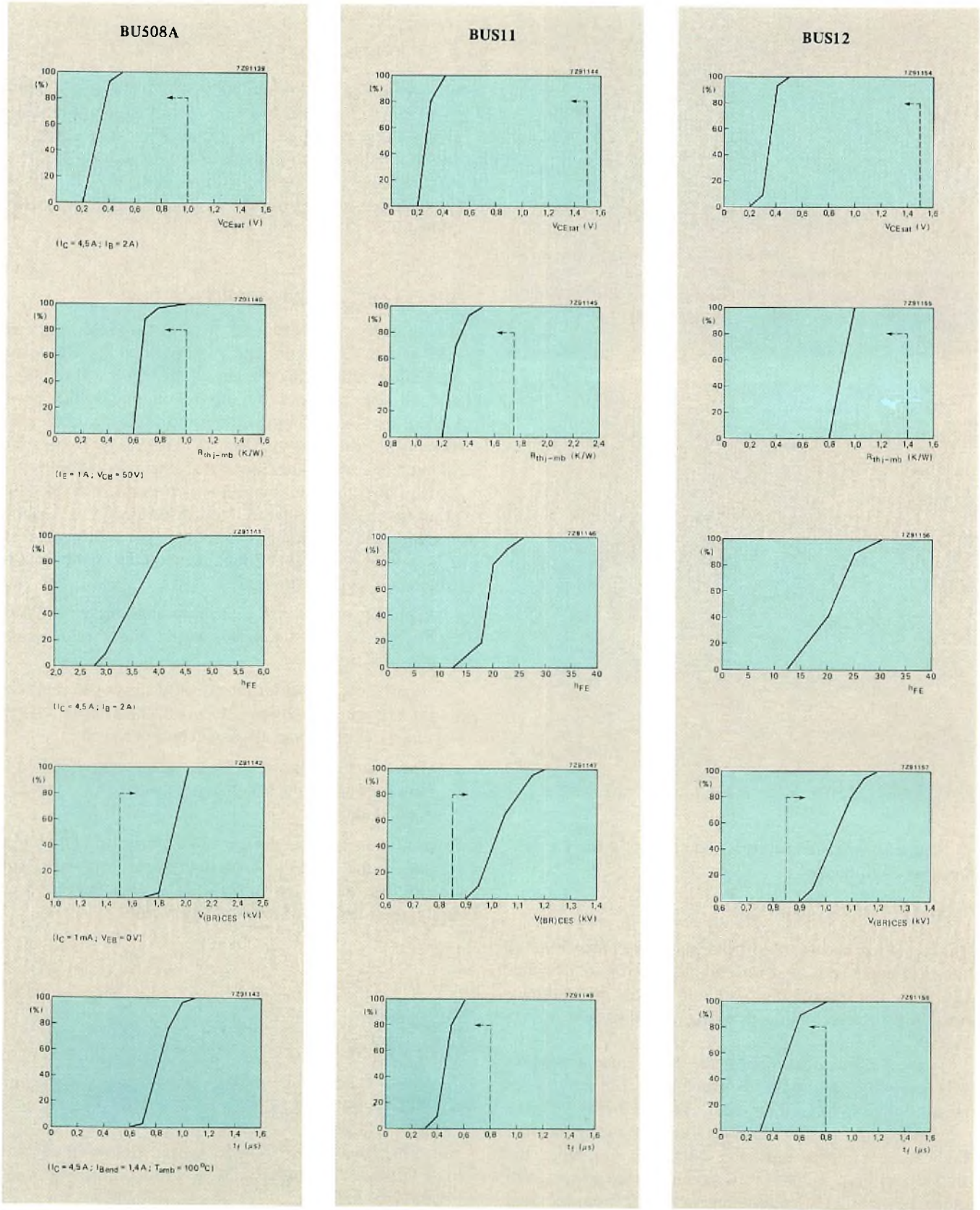
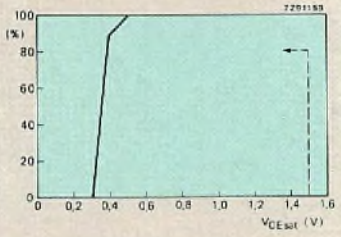
1. 1979. Quality of SOT-32 plastic power transistors. Philips' ELCOMA Technical Note 110, ordering code: 9398 011 00011.
2. 1979. Quality of TO-220 power transistors. Philips' ELCOMA Technical Note 133, ordering code: 9398 013 30011.

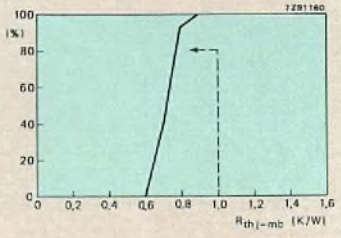
APPENDIX

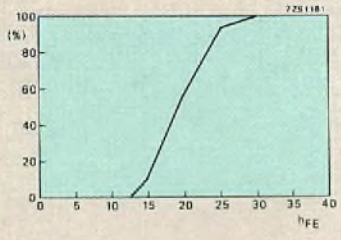
Typical parameter spreads recorded during routine checks on our high-voltage transistors

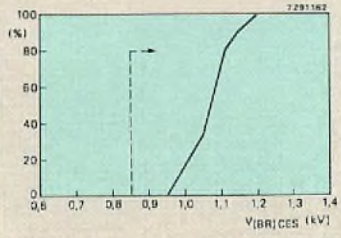


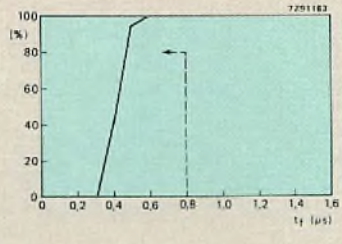
BUS13











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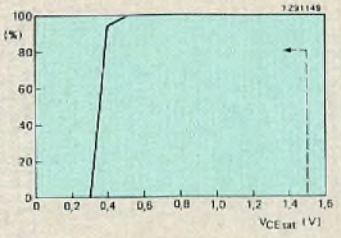

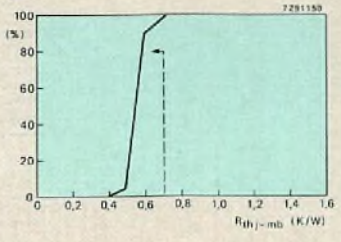

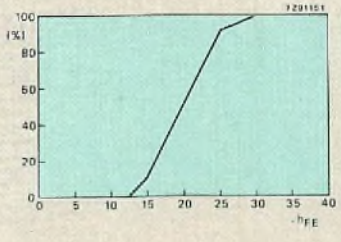

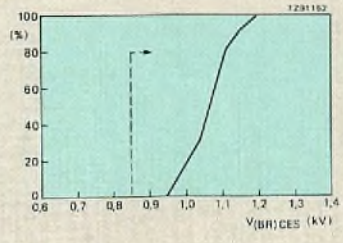

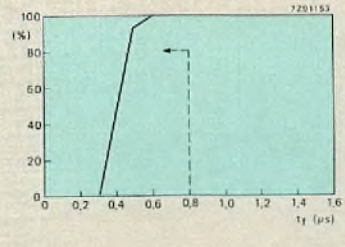

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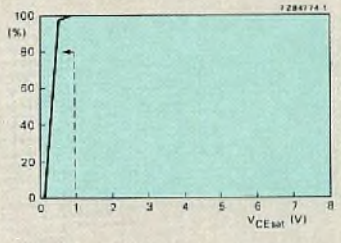

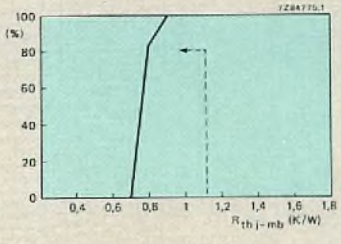

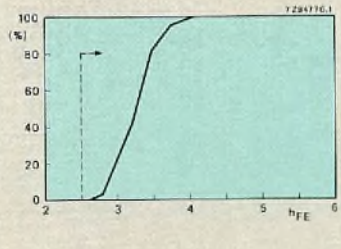

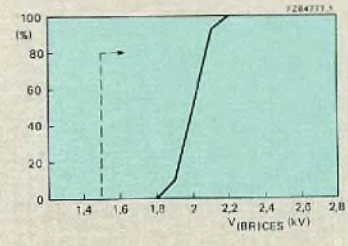

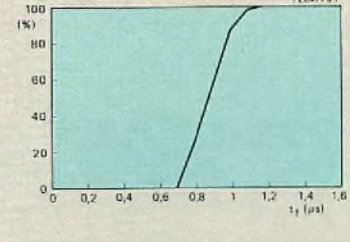

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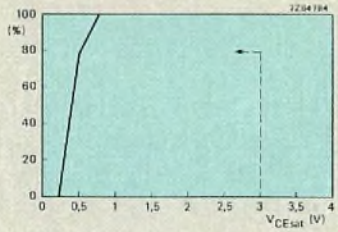

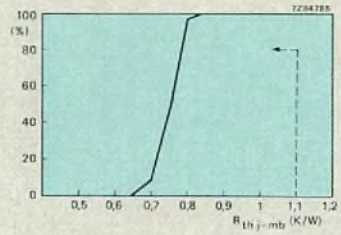

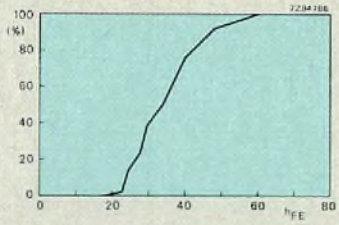

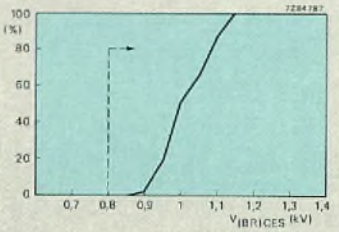

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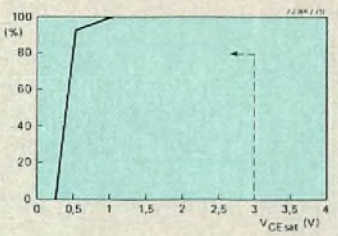

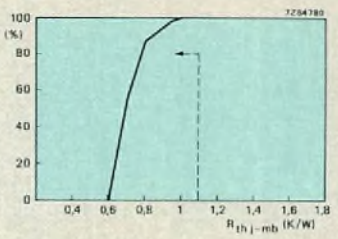

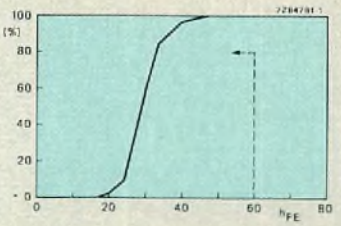

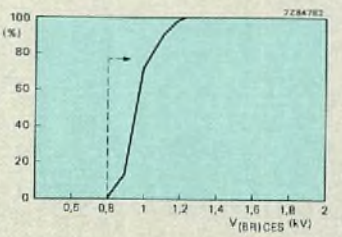

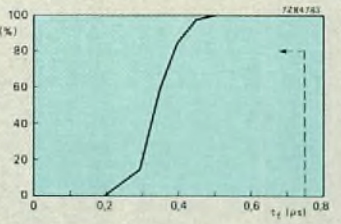

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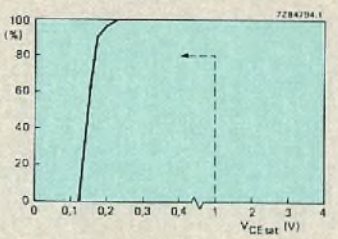
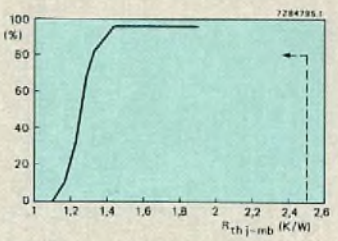
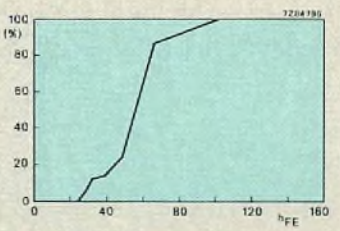
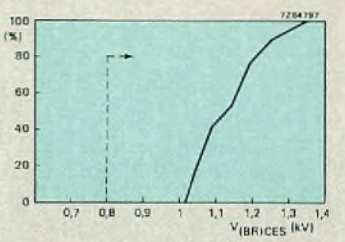
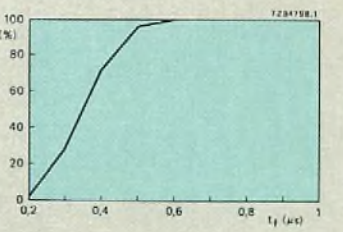










Liquid crystal displays

A. D. SCHELLING

Liquid crystal displays (LCDs) are passive displays. Unlike active displays*, which convert electrical energy into light, LCDs modify incident light – either transmitted or reflected.

LCDs use little power and operate from low voltages, thus making them ideal for battery-powered applications. The displays are highly legible, even in bright sunlight and are easy to illuminate for night use.

LIQUID CRYSTALS

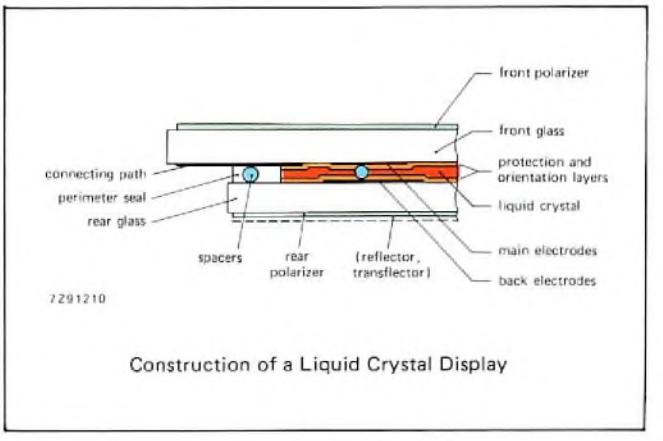
Liquid crystals are certain organic materials whose optical properties can be influenced by electric fields. They are called liquid crystals because, like liquids, their molecules are free to move but, like the molecules of solid crystals, they group together in an ordered manner.

In the class known as nematic liquid crystals, the class mostly used for displays, the rod-shaped molecules are more or less aligned in one direction.

TWISTED NEMATIC DISPLAYS

In an LCD the liquid crystal occupies a space of a few microns between two parallel glass plates. The inner surfaces of the plate have transparent conductive coatings (electrodes) that define the symbols, characters, or other pattern to be displayed. The surfaces in contact with the liquid are treated to induce the molecules to align in one direction parallel to the plate.

* Such as light emitting diodes (LEDs), incandescent lamps, etc.



Construction of a Liquid Crystal Display

In twisted nematic (TN) LCDs the induced direction at one plate is at right angles to the other. The liquid crystal structure twists through 90°, therefore, between one plate and the other. This rotates the plane of polarisation of transmitted light through 90°. A suitable voltage between two opposite electrodes breaks this twisted structure as the molecules align themselves parallel to the electric field.

Provided no voltage is applied, when the liquid crystal cell is placed between two crossed polarising filters, light passes through the display following the helix of the liquid crystal. The pattern defined by the electrodes is invisible (Fig.1(a)). When a voltage is applied, the helix structure is broken between the electrodes and the plane of polarisation is no longer rotated. The pattern defined by the electrodes appears dark against a bright background (Fig.1(b)). If one polariser is rotated 90°, the pattern appears bright on a dark background.

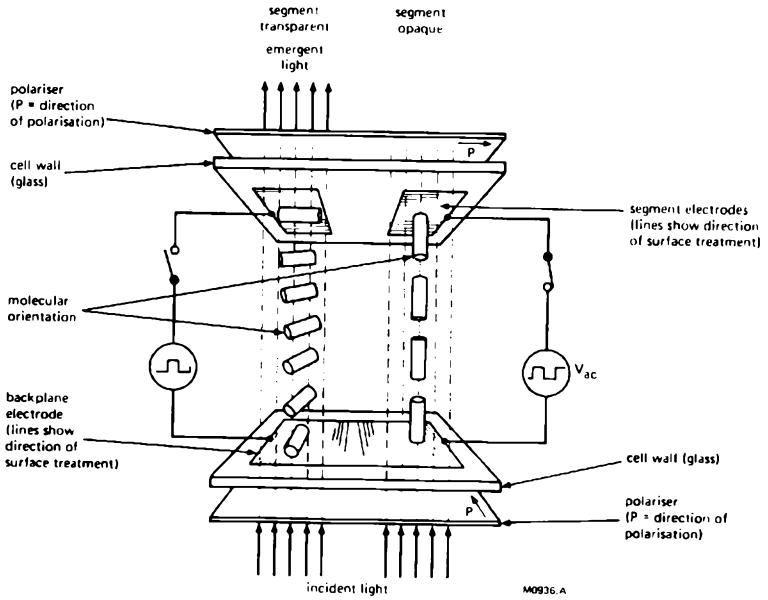


Fig.1 (a) The polarisation plane of light entering an un-energised part of an LCD is turned 90° by the twisted nematic crystal and so passes through the front polariser. (b) In an energised part, the polarisation plane is unaffected by the realigned crystal, so the light is blocked by the front polariser. The thickness of the liquid crystal layer is 6-10 μm

VIEWING MODES

LCDs can be used in three modes:

transmission mode in which the display is lit from behind (Fig.2(a)). Artificial light sources are usually used but uniform illumination is essential. Negative display (bright segments on a dark ground) is best suited to this mode. Transmissive LCD displays can also be projected, like slides.

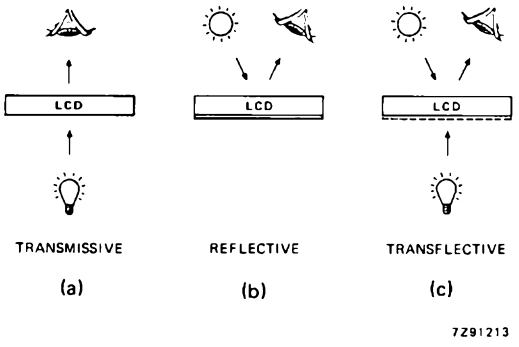


Fig.2 The three LCD viewing modes

reflective mode in which the LCD is backed by a diffuse reflector, such as brushed aluminium foil, that reflects ambient light through the display (Fig.2(b)). This mode exhibits high contrast and is most suited to use where ambient light is always available. Because no energy is needed for a light source, LCDs operating in this mode are especially suited to battery operated equipment.

transflective displays, a compromise between the other two, are used where the display is to be viewed under all lighting conditions (Fig.2(c)). The transflector, a partially transmissive reflector, reflects ambient light as well as diffusing back-lighting for night use.

COLOURED TN DISPLAYS

Colour can be introduced into a TN display in three basic ways: colour selective polarisers, coloured filters and coloured back-lighting. Colour selective polarisers produce coloured segments on a bright background, or vice versa. Videlec* has approved red, green and blue colours for applications in standard and extended temperature ranges.

Coloured filters may either be of foil or printed on the display. Coloured filters work better with back-lighting and, as with coloured back-lighting, are best used with transmissive, negative image LCDs (light segments on a dark ground). Unenergised, the segments appear dark like the background. Switched on, the active area becomes a window through which the coloured light shines.

*See page 242

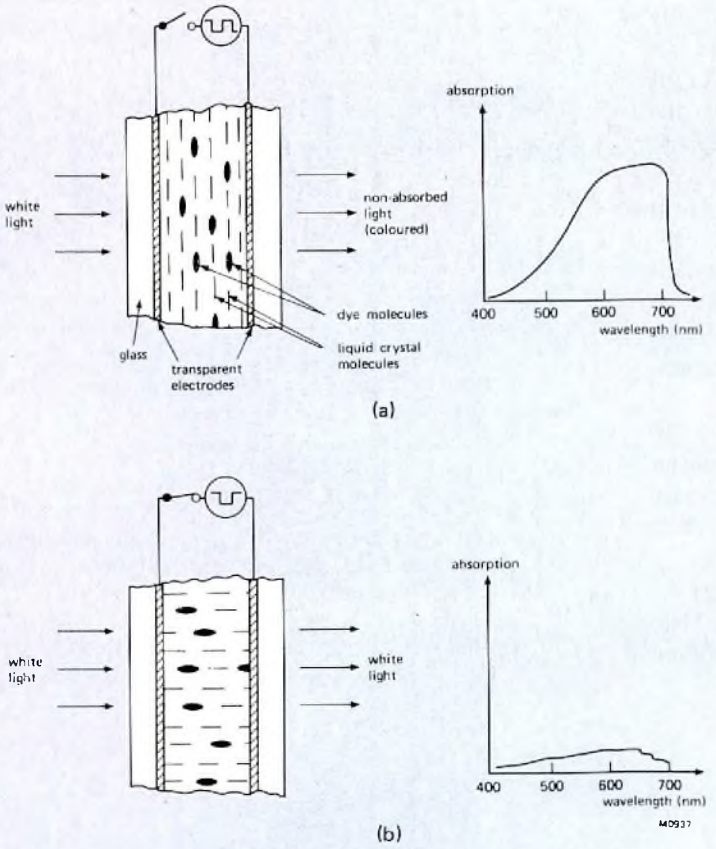


Fig.3 Operation of a guest-host display.
(a) In unenergised parts of the display, host liquid crystal molecules align the guest dye molecules parallel to the glass so that they absorb an important part of the incident light.
(b) In energised parts, the molecules are perpendicular to the glass and absorb little incident light

GUEST-HOST DISPLAYS

A relatively new kind of LCD is the guest-host display (GHD) in which molecules of a dichroic dye (guest) dispersed in a liquid crystal (host) align themselves with the long axis of the liquid crystal molecules. Where the molecules are parallel to the display surface (typically the non-energised parts, Fig.3(a)) a part of the incident light is absorbed and the display appears coloured. Where the molecules are perpendicular to the surface (energised parts, Fig.3(b)), the light passes unaffected through the display so that these parts are clear. Typically, guest-host displays have bright segments on a coloured background. They are now available in various colours.

Videlec offers two types of guest-host display: the 'Heilmeier' type with one polariser for higher contrast in the transmissive mode, and the 'White and Taylor' type (no polarisers) with very bright segments in the reflective mode.

The advantages of GHDs include brighter displays, wider viewing angle and less parallax distortion. Present disadvantages are lower contrast (but high legibility owing to higher brightness), higher operating voltages and inferior multiplexability; development is being directed toward overcoming these.

A selection of Videlec coloured LCDs: left, with colour selective polarisers; right, guest-host displays (White and Taylor type)

CONTRAST AND BRIGHTNESS

Liquid crystal displays don't generate light but modify incident light by controlled absorption and reflection. The brightness B of an LCD is expressed as the luminance L_{LCD} of the reflected or transmitted light in relation to the luminance L_{in} of the incident light (for reflective displays, measured on a MgO surface).

The legibility of an LCD depends largely on the contrast ratio $C_r = B_l/B_d$ where B_l is the brightness of the light parts of the display and B_d is the brightness of the dark parts. For TN displays the maximum contrast ratio is typically between 5 and 50. The limit of legibility in good light is a ratio of about 2, and in bad light about 3. For comparison, the contrast ratio of a newspaper is about 7.

The ratio $C = (B_l - B_d)/B_l = 1 - 1/C_r$, which can be between 0 and 1, is called simply contrast. The ratio of the actual contrast of a display to the maximum contrast obtainable from the display under given conditions is called relative contrast, D; it is usually expressed in percent.

Brightness and contrast both depend on the type of polariseres used. Those with a high polarising ratio give high contrast but low brightness in the light parts; those with a low polarising ratio have the opposite effect.

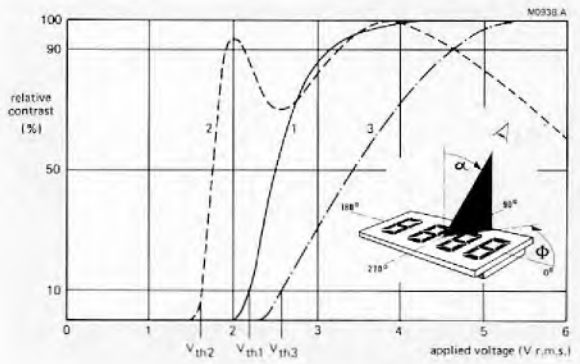


Fig.4 Relative contrast D as a function of applied voltage, measured at three viewing angles α (see inset).

Curve 1: $\alpha = 0°$ (view normal to surface)

Curve 2: $\alpha \approx 50°$, $\Phi = 270°$

Curve 3: $\alpha \approx 40°$, $\Phi = 90°$

The liquid crystal molecules at the front and back surfaces are oriented at 45°/225° and 135°/315°

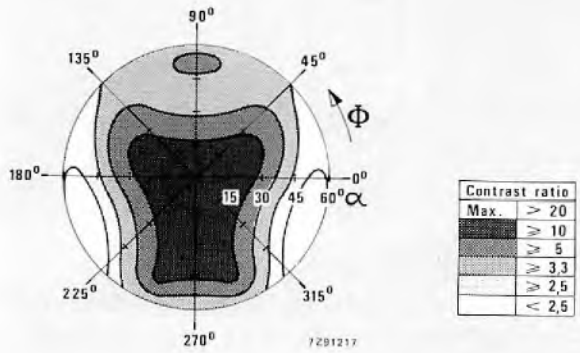


Fig.5 Typical isocontrast diagram for a direct-driven, reflective LCD, showing the variation of contrast as a function of the two components α and Φ of the viewing angle. The liquid crystal surface molecule orientations are 45°/135° and 135°/315°

ELECTRO-OPTICAL CHARACTERISTICS OF LCDs

Contrast/voltage and contrast/viewing-angle characteristic

The contrast of a twisted nematic LCD depends on both the applied voltage and the viewing angle. The voltage at which contrast first appears is called the threshold voltage, V_{th}. As voltage increases the relative contrast D also increases, more or less steeply, toward its maximum; the voltage at which D = 90% is called the saturation voltage, V_{sat}. Both V_{th} and V_{sat} as well as the shape of the curve joining them, vary considerably with viewing angle (Fig.4).

Contrast also varies with viewing angle. LCD data sheets therefore give isocontrast diagrams, like that of Fig.5, showing the contrast/viewing-angle characteristics under various drive conditions.

The contrast/voltage characteristic is temperature dependent, with a negative coefficient. That is, the threshold voltage declines as temperature rises. Typical values of dV_{th}/dT are −3 to −10 mV/K.

The On and Off response times (Fig.6) are also temperature dependent (Fig.7). Because of the increasing viscosity of the liquid crystal, both increase as temperature decreases.

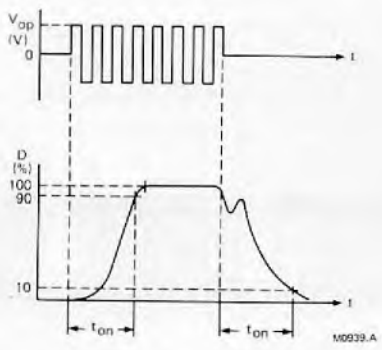


Fig.6 On and Off response of an LCD in relation to the alternating drive voltage V_{op}

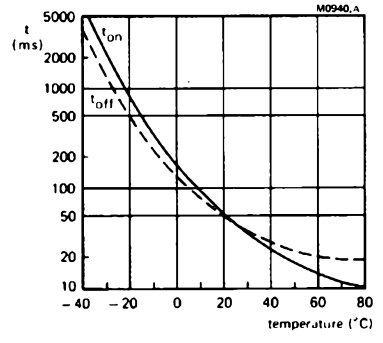


Fig.7 Response times of an extended temperature range LCD as functions of temperature. V_{op} = 4.5 V at 100 Hz. Direct drive

USING LCDs

Equivalent circuit

Figure 8 is a simplified equivalent circuit of an LCD. To avoid electrochemical reactions that shorten the life of the display, the drive voltage must be an alternating one whose effective amplitude is not much greater than the saturation voltage V_{sat}; the maximum permissible d.c. component is 100 mV.

The lower frequency limit of the drive voltage is set by the onset of flicker at about 30 Hz. Between 30 Hz and 1 kHz an LCD can be regarded as a capacitive load. At 30 Hz and a drive voltage of 4.5 V r.m.s., the current consumption is about 1.5 μA per square centimetre of activated area; this increases linearly with frequency. The current consumption sets a practical upper frequency limit of about 200 Hz.

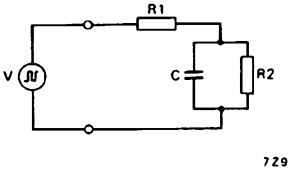


Fig.8 Simplified equivalent circuit of an LCD. R_1 is the series resistance of the electrodes, R_2 the series resistance of the liquid crystal and C the interelectrode capacitance. Typical values are R_1 = 10 kΩ, R_2 = 1 MΩ/cm², C = 1.5 nF/cm²

Direct drive

In direct drive the back-plane electrode is common and each display segment is connected directly to a corresponding terminal of the driving electronics. Figure 9 illustrates a phase-switching arrangement commonly used with direct drive. Here, a square-wave is applied to the back-plane electrode and to one input of each of the exclusive-OR gates controlling the individual segments. The control voltage at the other input of each gate determines whether the gate output is in phase or antiphase with the back-plane voltage. If the control voltage is high, the gate output is in antiphase with the back-plane voltage and the segment is On; if it is low, the output is in phase with the back-plane voltage and the segment is Off.

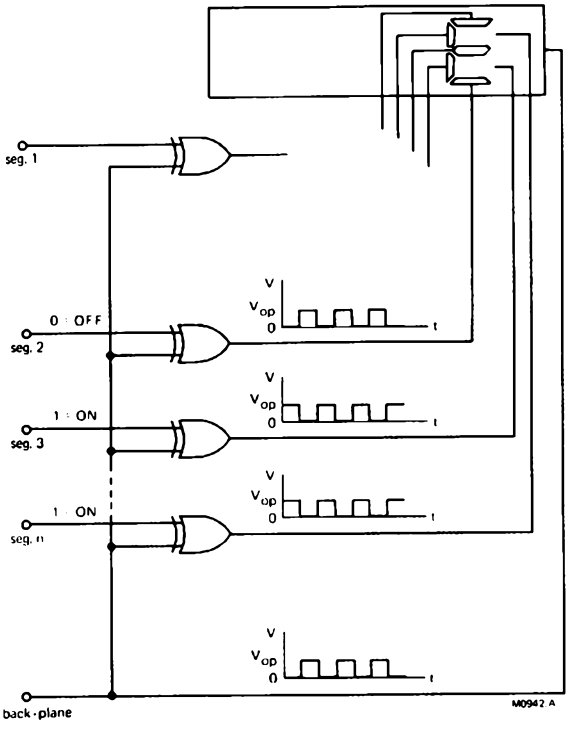


Fig.9 Phase-switching circuit for direct drive

Direct drive affords the most freedom with regard to drive voltage, operating temperature range, and viewing angle. However, it also requires the most contatcs, driving circuits, and connections.

Multiplex drive

Direct drive of an LCD with very many segments is impractical because of the large number of connections and driving circuits required. Both can be reduced by multiplexing: connecting segments together in groups and addressing them sequentially via multiple back-plane electrodes (Fig.10). The number of back-plane electrodes or segments per group determines the multiplex ratio.

Figure 11 shows the drive voltage waveforms of a 1:4 multiplexed LCD. The back-plane electrodes are activated sequentially and the segment groups are switched on or off simultaneously in accordance with the characters to be displayed. The repetition frequency of the drive waveforms must be at least $N \cdot f_f$, where N is the reciprocal of the multiplex ratio and f_f the flicker-onset frequency for direct drive (30 Hz).

Because the liquid crystal responds to the r.m.s. value of the voltage across it, the Off voltage of a multiplexed LCD is not zero, as in direct drive, but some fraction of the On voltage. The ratio of the On to the Off voltage (called discrimination) depends on the multiplex ratio and the number of voltage levels involved (see Table, p. 239).

What makes multiplex operation possible is the non-linearity of the contrast/voltage characteristic of the LCD.

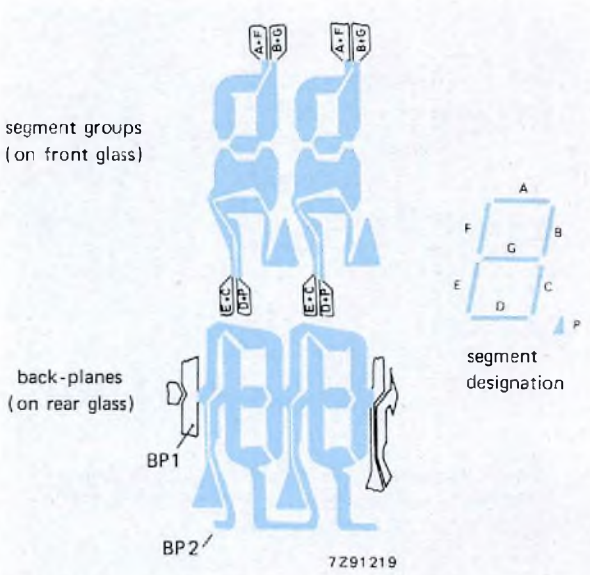


Fig.10 Segment grouping and back-plane electrodes of a two-digit, 7-segment LCD for 1:2 multiplex drive. The segments are grouped in pairs and the back-plane electrode is divided into two parts

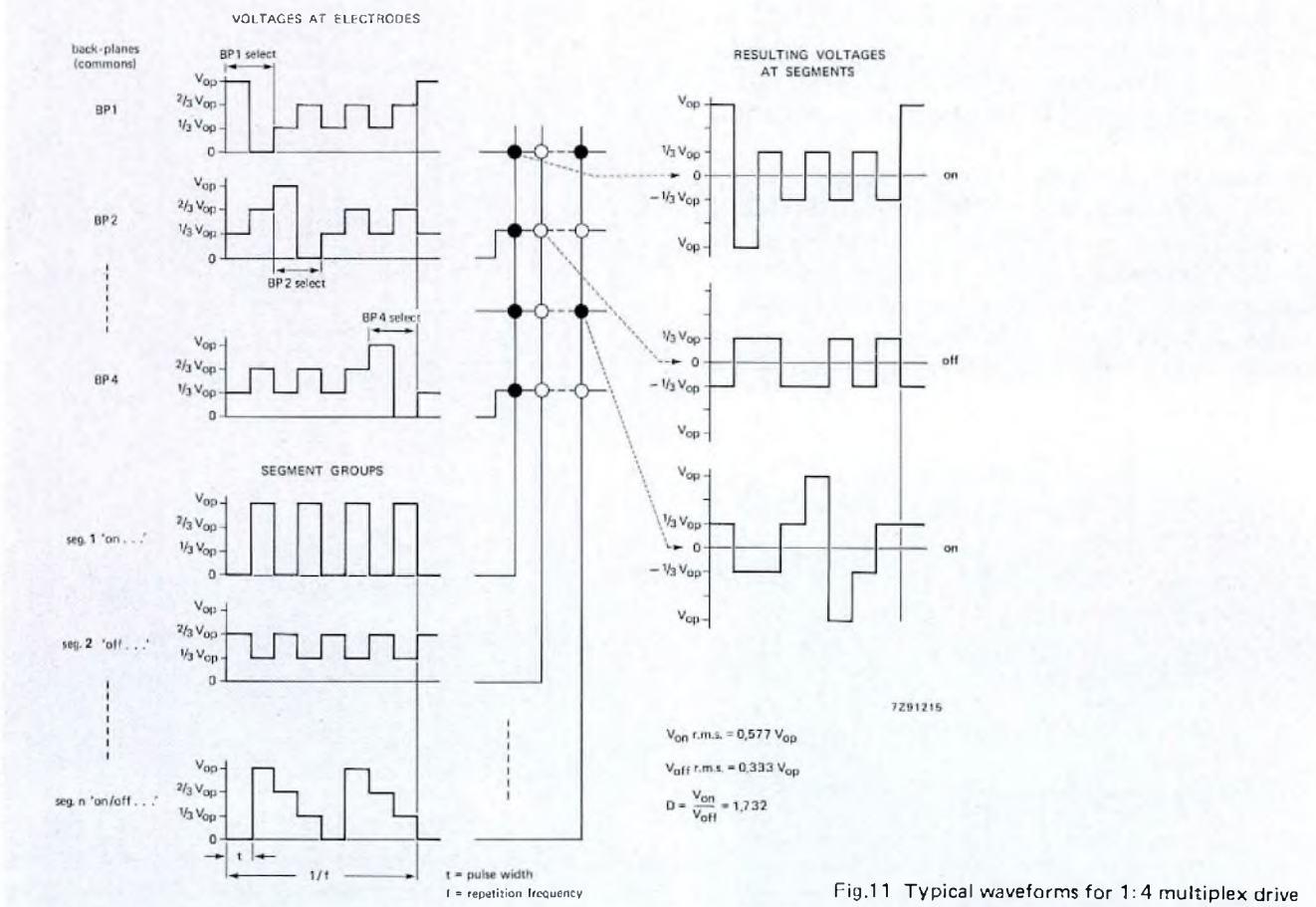


Fig.11 Typical waveforms for 1:4 multiplex drive

Operating voltage ratios, required discrimination, and number of display connections for various multiplex ratios

multiplex ratio, 1:	1	2	3	4	8	16
V_{off} (r.m.s.)/V_{op}	0	0.35	0.33	0.33	0.30	0.24
V_{on} (r.m.s.)/V_{op}	1	0.79	0.64	0.57	0.43	0.32
discrimination, V_{on}/V_{off} (r.m.s.)	∞	2.24	1.92	1.73	1.45	1.29
number of connections required for sixteen 16-segment characters	257	130	89	68	40	32

Based on 3-level method for 1:2, 4-level method for 1:3 and 1:4, and 6-level method for 1:8 and 1:16 multiplex ratios.

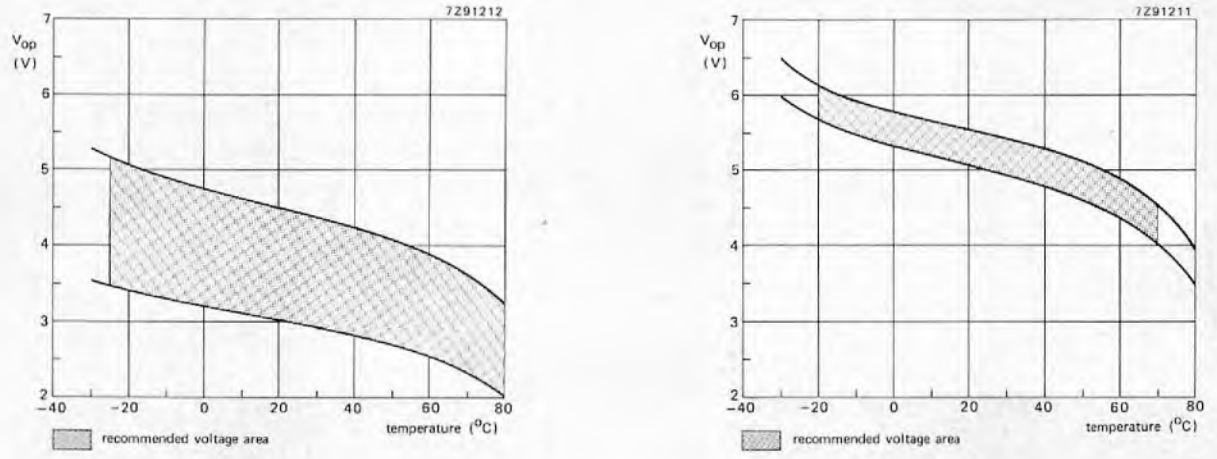


Fig.12 Typical recommended voltage areas for 1:2 (left) and 1:8 (right) multiplex drive. At the upper boundary of each area the Off segments become faintly visible at a viewing angle $\alpha = 40°$, $\Phi = 270°$; at the lower boundary $C_r < 2.5$ at $\alpha = 10°$, $\Phi = 270°$ for Mux 1:8 and $\alpha = 0°$ for Mux 1:2

To obtain optimum contrast and keep the Off segments invisible, the operating voltage V_{op} has to be chosen so that the Off voltage is just below the threshold voltage V_{th}. The On voltage, and hence the contrast, is then a function of the steepness of the characteristic (which depends on the liquid crystal) and the discrimination (which depends on the multiplex method). With too high a voltage the Off segments become visible, and with too low a voltage contrast is lacking. Figure 12 shows typical recommended voltage areas for multiplex ratios of 1:2 and 1:8; the larger the ratio, the smaller the recommended voltage area.

At low multiplex ratios, satisfactory operation over a wide temperature range can be obtained with a fixed value of V_{op}. To obtain a constant viewing cone throughout the same temperature range at high multiplex ratios, however, V_{op} has to be temperature compensated to allow for the negative temperature coefficient of the threshold voltage.

The slope of the contrast/voltage curve, as well as other characteristics of twisted nematic LCDs, sets a practical limit to the multiplex ratio. Besides its effects on operating voltage and temperature range, multiplexing also narrows the viewing angle (Fig.13). The highest ratio recommended at present ia about 1:16, but new liquid crystals that will allow ratios of 1:100 or more are being developed.

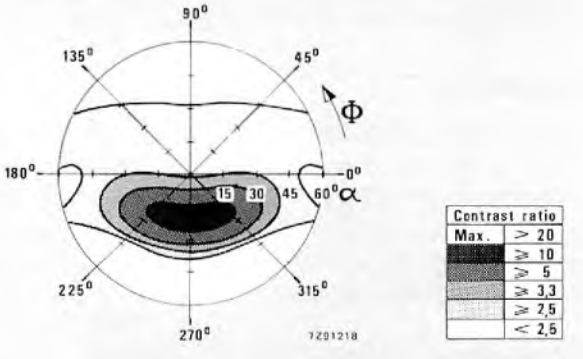


Fig.13 Typical isocontrast diagram for a 1:8 multiplex display (compare Fig.5)

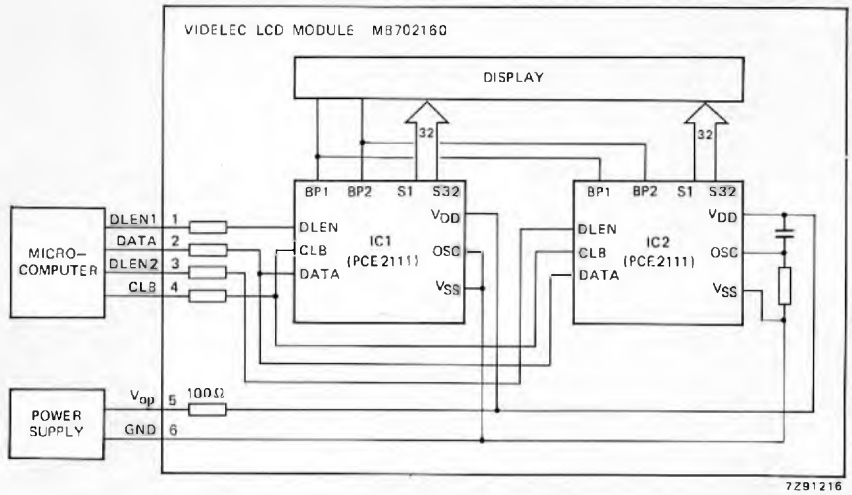


Fig.14 Videlec 16-character, serial data input LCD module MB 7020160 with built-in PCE2111 drivers

LCD modules

Besides being available by themselves, some LCDs are also available in modules complete with driving circuitry, frame or housing, mounting board, and connectors (Fig.14). Being compatible with microprocessor-based systems, such modules relieve the equipment designer of having to concern himself with problems specific to the display.

Chip-on-glass (Videlec integrated display)

A recent Videlec innovation is chip-on-glass technology, in which the driver IC chip is bonded direct to the glass of the LCD. The number of external contacts is drastically reduced to only five or six (for power supply and for a serial data bus that is directly controllable by most microcomputers). The example shown in Fig.15 is an element for displaying one character in a large information panel. Being driven at a multiplex ratio of 1:2, the display has a wide viewing angle and wide operating temperature range. Without chip-on-glass technology, the same display would require 34 external contacts.

Chip-on-glass displays are conveniently slim, require no PC board and are easy to mount, connect, illuminate and drive.

Lighting and mounting

Reflective and transflective displays should be mounted as close as possible to the front surface of the equipment to gain maximum illumination from ambient light. In choosing a mounting position, take account of the viewing angle and the isocontrast diagrams published in the LCD data. Auxiliary front lighting for a reflective display should be at an angle close to the viewing direction to minimise reflection

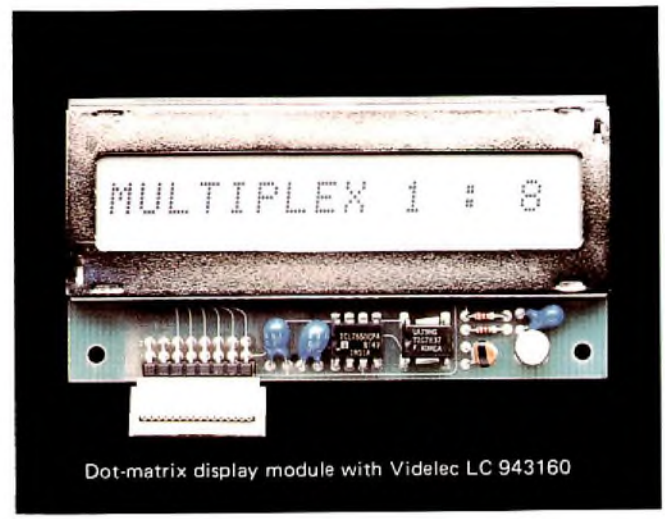
and shadow effects. Back lighting for transmissive and transflective displays must be diffuse and as uniform as possible; suitable sources are electroluminescent panels, or incandescent lamps or LEDs in combination with light pipes. The casing of the equipment can be designed to provide a mounting for the LCD with a suitable aperture through which to view the display.

Apply mounting pressure symmetrically and as evenly as possible; avoid pressure on the seal or within the viewing area. To protect front polarisers from scratches and humidity, use glass or a non-birefringent plastic.

Connecting

The two commonly used means of connecting LCDs are: 2.54 mm pitch dual-in-line pins which can be soldered into a printed wiring board or plugged into a socket; and zebra strips.

Zebra strips are elastomer strips with alternating conductive and insulating sections that support the LCD and connect it to its wiring board (Fig.16). The electrode of LCDs designed for zebra-strip connection are brought out to overhanging edges on the underside of the front glass; the conductive sections of the zebra strips connect these with corresponding contacts on the wiring board. A mounting bezel or clamp ensures uniform contact pressure. The pitch of the zebra strips should be at least four times as fine as that of the contacts; strips with as many as eight conductive sections per millimetre are available. Zebra strips are particularly suitable for making connections to LCDs that are to be mounted in slim cases.



Dot-matrix display module with Videlec LC 943160

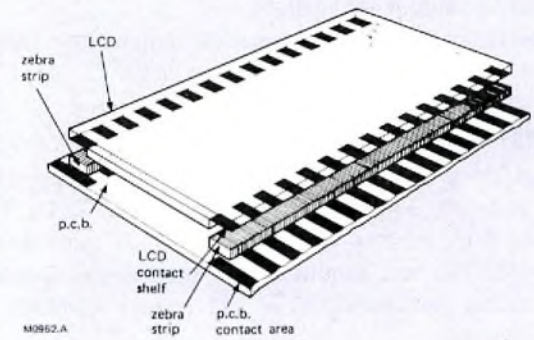


Fig.16 LCD connection using zebra strips

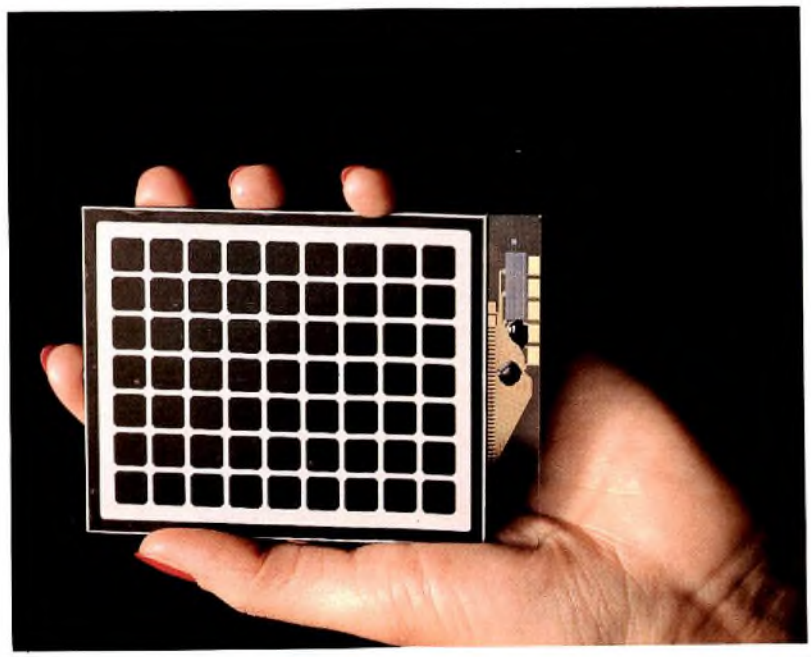


Fig.15 Videlec HX10607600 chip-on-glass 7 x 9 character matrix; the character height is 80 mm

ENVIRONMENTAL CONDITIONS

Operating temperature range

The operating temperature range of a twisted nematic LCD is bounded by the temperature limits of the nematic phase of the liquid crystal. The upper limit is the clearing point, the temperature at which molecular alignment disappears and the material becomes isotropic. The theoretical lower limit is the melting point, which is difficult to determine because all currently used liquid crystals can be supercooled very easily. The practical lower limit depends on how slow a response can be tolerated.

Videlec LCDs are classified in two operating temperature ranges. The normal range, –10 °C to +60 °C, is suitable for most interior applications where there is some control of temperature and humidity. The extended range, –25 °C to +80 °C, is for use in less controlled settings such as automobiles or outdoor applications.

Operation outside the specified temperature range is unsatisfactory but does no permanent harm.

Storage temperature range

Storage limits are –25 °C to +70 °C for normal temperature range and –40 °C to +90 °C for extended range LCDs. These are absolute minima and maxima which must not be exceeded. The best conditions for long-term storage are a temperature not above 30 °C and relative humidity not exceeding 60%.

Humidity

Short-term exposure to high humidity does not harm an LCD as long as there is no condensation on it. However, permanent operation at high temperature and humidity reduces the life of both the liquid crystal cell and the polarisers.

QUALITY CONTROL AND RELIABILITY

Quality control

Quality control of Videlec LCDs includes incoming inspections,fabrication controls, functional and final inspections, and reliability tests.

- Incoming inspection covers all materials, tools, and production aids.
- Fabrication controls include supervision of the production equipment and control of key process steps.
- 100% of the LCDs produced are checked for leaks, visual and dimensional defects, and electrical operation.
- Before any production lot is released for delivery, random samples taken from it must pass accelerated reliability tests under extremes of voltage, temperature, and humidity.
- Samples taken regularly from all production lots are subjected to various combinations of operating and environmental stress to gain information about life and reliability.

Results of all these tests are fed back to the departments and activities concerned to ensure that quality is built-in, not inspected out.

Guaranteed AQLs are monitored by sampling. Two classes of failures are inspected for:

- Mechanical/optical defects, including imperfect or inoperative segments, lack of contrast, restricted viewing angle, scratches on the polarisers, and glass cracks.
- Electrical/optical defects, including excess power consumption and response time, low d.c. resistance, high capacitance, black spots, contrast variations between segments, etc.

The reject criteria for standard quality are an AQL of 1.5% for mechanical/optical and 1% for electrical/optical defects. AQLs are calculated from inspections carried out according to MIL-STD-105D, Inspection Level 2, or DIN4080.

Reliability

Under normal operating conditions the failure rates of LCDs are of the order of 10^{-7}/h, comparable to those of discrete semiconductors. The expected service life is more than 10^5 h (more than 11 years).

Operating stresses that may increase the failure rate are d.c. voltage, excess operating (a.c.) voltage, extreme temperatures, and high humidity. Voltage stresses can be avoided by correct design of the driving circuits. Where high temperature or humidity is unavoidable, LCDs specially designed for such conditions should be used. Developments in materials and technologies are continually extending the practical environmental limits.

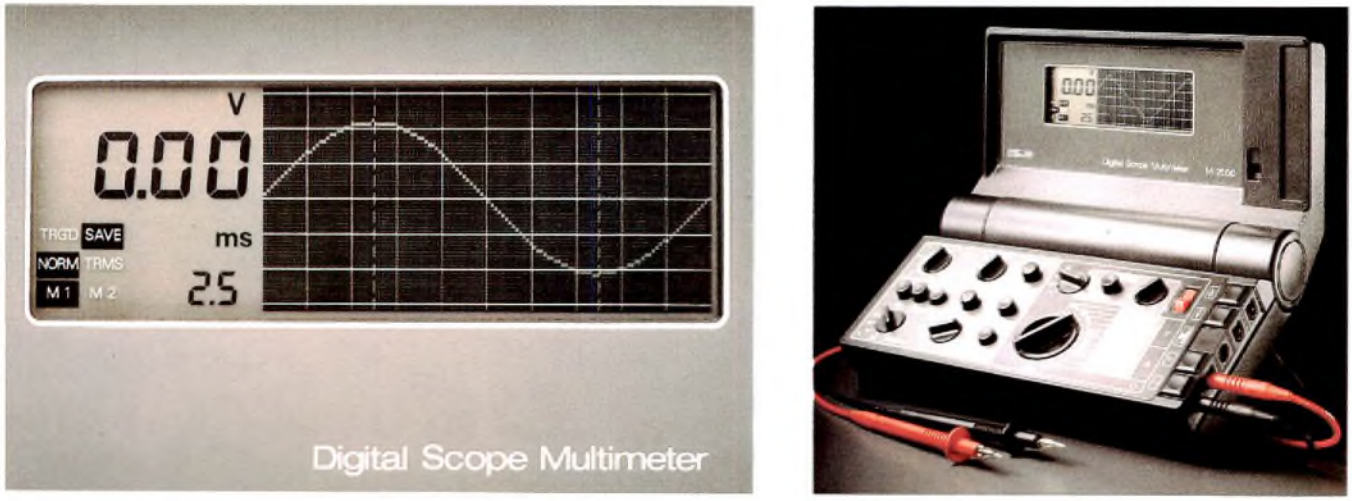
Standard LCDs and recommended driver ICs

Videlec type number	overall size (l x h) (mm)	character height (mm)	drive	no and type of connections*	driver ICs	description of display
LC 241440-101	23.9 x 14.0	6.8	direct	32 E	PCF2112	4 digits, 3 points (p)
LC 283020-300	27.9 x 30.4	12.7	direct	18 E	PCF2112 or SAA1062	2 digits, 2 p
LC 283020-301	27.9 x 30.4	12.7	direct	18 DIP	PCF2112 or SAA1062	2 digits, 2 p
LC 382040-401	38.0 x 20.3	8.0	direct	37 E	PCF2112 or SAA1062 (x2)	4 digits, 3p, colon, ±, B,
LC 382080-411	38.0 x 20.3	6.0	Mux 1:2	38 E	PCE2111	8 digits, 8p, 2 pointers
LC 382232-700	38.1 x 21.6	8.5	direct	26 E	PCF2112	3½ digits, 1 colon
LC 512332-300	50.8 x 22.9	8.9	direct	29 E	PCF2112	3½ digits. 1 colon, AM/PM, bell
LC 513000-300	50.8 x 30.4	3.7 bar width	direct	44 E	PCF2112 (x2)	dual bar graph
LC 513031-300	50.8 x 30.4	12.7	direct	32 DIP	PCF2112	3½ dig., 3p, 1 colon, ±, BAT, ~, ▲
LC 513031-309	50.8 x 30.4	12.7	direct	32 E	PCF2112	3½ dig., 3p, 1 colon, ±, BAT, ~, ▲
LC 513031-302	50.8 x 30.4	12.7	direct	31 DIP	PCF2112	3½ dig., 3p, 1 colon, ±, LO BAT
LC 513031-303	50.8 x 30.4	12.7	direct	31 E	PCF2112	3½ dig., 3p, 1 colon, ±, LO BAT
LC 513031-307	50.8 x 30.4	12.7	direct	38 E	PCF2112 (x2) or SAA1062 (x2)	3½ dig., 3p, –, 8 signs for DMM
LC 513040-301	50.8 x 30.4	12.7	direct	35 DIP	PCF2112 (x2) or SAA1062 (x2)	4 dig., 3p, 1 colon
LC 513040-303	50.8 x 30.4	12.7	direct	35 E	PCF2112 (x2) or SAA1062 (x2)	4 dig., 3p, 1 colon
LC 513041-300	50.8 x 30.4	10.0	direct	39 DIP	PCF2112 (x2) or SAA2062 (x2)	4½ dig., 4p, 2 colon, ±, LO BAT
LC 513041-301	50.8 x 30.4	10.0	direct	39 E	PCF2112 (x2) or SAA2062 (x2)	4½ dig., 4p, 2 colon, ±, LO BAT
LC 513041-320	50.8 x 30.4	11.0	Mux 1:3	15 E	–	4½ dig., 4p, –, LO BAT, cont.
LC 513050-300	50.8 x 30.4	10.0	direct	40 DIP	PCF2112 (x2) or SAA1062 (x2)	5 digits, 4 p
LC 522232-300	52.0 x 22.0	10.0	direct	30 E	PCF2112 or SAA1062 (x2)	3½ dig., 1 colon, AM/PM, S, bell
LC 554731-412	46.8 x 54.8	5.6	Mux 1:2	78 E	OKI MSM 5015	analog + digital clock
LC 7020160-412	69.8 x 20.3	6.0	Mux 1:2	68 E	PCE2111 (x2)	16 digits, 16 p
LC 7020160-430	69.8 x 20.3	6.0	Mux 1:4	32 E	–	16 digits. 16 p
LC 703000-300	69.8 x 30.4	5.0 bar width	direct	46 DIP	PCF2112 (x2)	dual bar graph
LC 703060-301	69.8 x 30.4	12.7	direct	50 DIP	PCF2112 (x2)	6 digits, 5 p, 2 colon
LC 703831-300	69.8 x 30.4	17.8	direct	32 DIP	PCF2112 or SAA1062 (x2)	3½ dig., 3p, 1 colon, ±, BAT, ~, ▲
LC 703840-300	69.8 x 30.4	17.7	direct	33 DIP	PCF2112 or SAA1062 (x2)	4 digits, 3 p, 1 colon
LC 07610110-300	76.2 x 101.6	76.0	direct	9 DIP	PCF2112 or SAA1062	1 digit, 1 p
LC 943080-301	93.8 x 30.4	12.7	direct	67 DIP	PCF2112 (x3)	8 digits, 7 p, 3 colon
LC 9430160-344	93.8 x 30.4	7.5 (5.8)	Mux 1:8	88 E		16-character dot-matrix
LC 11402600-310	26.0 x 104.0	5.0 bar width	Mux 1:2	107 E	PCF2111 (x4)	dual bar graph
LC 11404650-301	114,0 x 46.0	25.0	direct	50 DIP	PCF2112 (x2)	5 dig., 4p, 4 commas, 4 sale signs
MB 7020160	92.5 x 25.0	6.0	Mux 1:2	16 digit numeric LCD module with serial data input		
HX 10607600-380	76.2 x 106.2	79.8	Mux 1:2	7 x 9 dot matrix with on-glass integrated driver PCE2111		
HX 845800-380	58.3 x 83.9	60.3	Mux 1:2	7 x 9 dot matrix with on-glass integrated driver PCE2111		

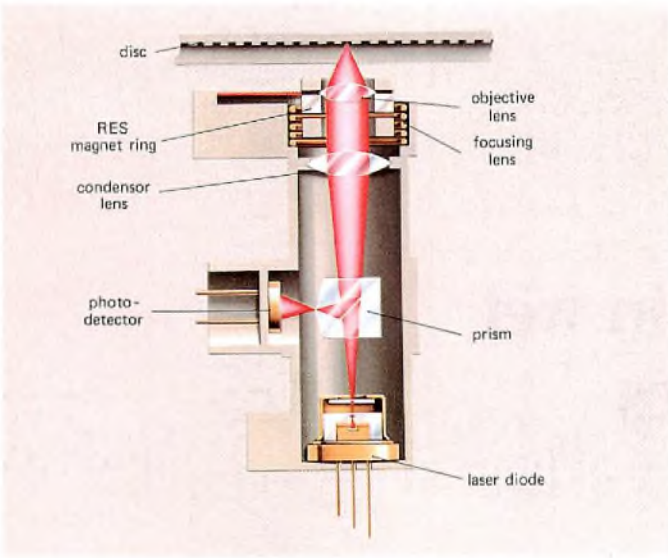
* *E (elastomer) = zebra strip.*

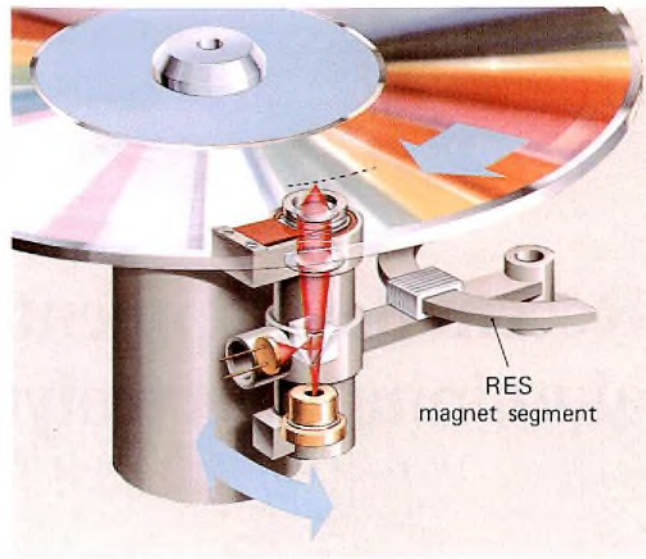
Applications of Liquid Crystal Displays

- Measuring and controlling equipment
  - multimeters
  - panel meters
  - scales
  - oscilloscopes
  - thermometers
- Clock and watches
  - digital and analog
- Telephony
  - telephone sets
  - tariff counters
  - telephone directory
  - telex machines
  - switch boards
- Cars
  - clocks
  - trip computers
  - dashboards
  - car radios
- Entertainment electronics
  - portable radios
  - HiFi equipment
  - Video equipment
  - cameras
  - games and toys
- Domestic appliances
  - heating controllers
  - cookers
  - irons
  - freezers
- Public information
  - large scale information boards
  - station indicators in buses, trains
  - aircraft
- Data processing
  - data terminals
  - typewriters
  - cash registers
  - calculators



Digital oscilloscope/multimeter with LCD data display (photo courtesy of BBC Metrawatt)





pictures above

Application of RES magnets (see article on page 194) in Philips Compact Disc Player: focusing the laser beam (left) and controlling the player arm (right).

picture left

Reducing the depth of small loudspeakers: with Ticonal magnet system (left), depth 15 mm and with RES magnet system (right), depth 8 mm.

Recent developments in wet aluminium electrolytics

A. OTTEN, H. SCHMICKL and J. SLAKHORST

It is generally accepted that, if you want a high value capacitor with a high rated voltage and you don't want to pay too much for it, a wet electrolytic is the answer. Outdated opinion has it, however, that although a feature of electrolytics is their high CV/unit volume, such a capacitor must be quite large, cannot withstand much ripple current, and will fail prematurely if operated at the upper extremity of its voltage or temperature rating. Furthermore, there is a belief that the leakage current of any wet electrolytic will increase dramatically if the component is stored for a long time at high temperature.

This article shows that our continuing progress in wet aluminium electrolytic capacitor development during the last two decades has resulted in the creation of new foils, electrolytes and construction techniques which overcome all these disadvantages. Wet electrolytics are no longer components which can only be considered for the less stringent requirements of the consumer market. Ours can now also perform important roles in professional and industrial applications such as high-speed data systems and fast switching power supplies operating at high power levels.

PHYSICAL PROPERTIES OF WET ALUMINIUM ELECTROLYTICS

Understanding how the new developments improve the performance of our wet aluminium electrolytics, requires knowledge of how the physical properties of an electrolytic influence its electrical characteristics. A schematic cross-section of a wet aluminium electrolytic and its equivalent circuit are given in Fig.1 and 2.

Anode

The anode is a strip of high-purity aluminium foil. Since a large effective surface area for the anode increases capacitance to volume ratio, the foil is electrochemically etched to increase its surface area (by about 50 times for most conventional foils).

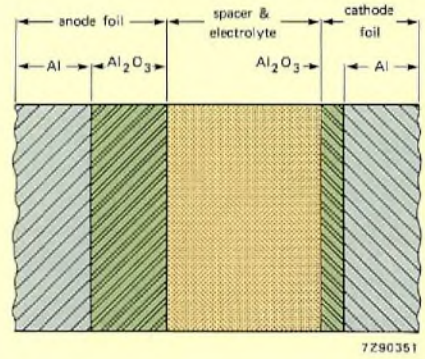


Fig.1 Schematic cross-section of a wet aluminium electrolytic

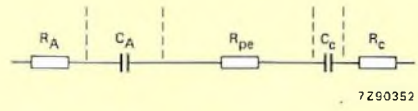


Fig.2 Simplified equivalent circuit of a wet aluminium electrolytic

Dielectric

The dielectric is formed by anodising the anode foil (also known as forming) to convert its surface to aluminium oxide (AL_2O_3). The forming voltage is at least 20% higher than the rated voltage of the electrolytic (U_R) and forms a 1.4 nm thick layer of a aluminium oxide for each volt (thickness constant $= 1.4 \times 10^{-9}$ m/V). This dielectric strength approaches the upper limit predicted by the ionic theory of crystals. The dielectric has a relative permittivity (ϵ_r) of about 8.

Cathode

The cathode is a low-resistivity, non-corrosive liquid electrolyte which ensures effective and uniform contact with the spongy aluminium oxide dielectric on the anode foil. Electrical contact is made to the cathode (electrolyte) via a 20-60 μm thick strip of etched aluminium foil which has a 2 nm layer of stabilised aluminium oxide dielectric on its surface. The voltage drop across the cathode will therefore be about 1.5 V. The thin dielectric, together with the large effective surface area of the etched cathode foil, results in a stored charge (CV product) at the cathode which is equal to the CV product at the anode. This improves the charge/discharge properties of the capacitor. One or two ≈ 50 μm thick absorbent paper strips on each side of the cathode foil act as a reservoir for the electrolyte and also form a spacer between the anode and cathode foils after the capacitor has been wound into cylindrical form.

Winding and connections

The anode/paper/cathode/paper sandwich is rolled up as shown in Fig.3 on a winding machine to form the characteristic compact cylindrical shape of an electrolytic capacitor. In certain types of electrolytic, the resistance of the aluminium foils is minimised by making multiple connections to the anode and cathode terminals.

Fig.3 The electrolytic cell of a wet electrolytic

IMPROVING THE PERFORMANCE OF WET ELECTROLYTICS

Increasing volumetric efficiency

The capacitance of a basic parallel plate capacitor is:

$$C = \epsilon_0 \epsilon_r A/t$$

where ϵ_0 is the permittivity of a vacuum, ϵ_r is the relative permittivity (dielectric constant) of the dielectric, A is the surface area of the electrodes and t is the thickness of the dielectric.

Incorporating the factor by which the etching increases the surface area of the electrodes (etching factor f_e), and the thickness constant of the aluminium oxide dielectric (1.4 nm/V) gives the expression for the anodic capacitance (C_A):

$$C_A = \epsilon_0 \epsilon_r f_e A/(1{,}4\ V \times 10^{-9}) \text{ or,}$$

$$C_A V = K f_e A$$

where constant $K = \epsilon_0 \epsilon_r/(1.4 \times 10^{-9})$.

Since the cathode foil has a much thinner dielectric layer than the anode foil, the cathodic capacitance is very much greater than the anodic capacitance and the two capacitances are connected in series (Fig.2). The anodic capacitance therefore predominates and the cathodic capacitance can be ignored for the purpose of this analysis.

The volume of the anode/paper/cathode/paper sandwich of the electrolytic cell is:

$$vol = A(t_a + t_c + 2t_p)$$

where t_a = anode foil thickness

t_c = cathode foil thickness

t_p = paper spacer thickness.

The volumetric efficiency of the electrolytic cell is therefore:

$$CV/vol = K f_e/(t_a + t_c + 2t_p).$$

Since K is a constant, the following methods are available to increase the volumetric efficiency of an electrolytic capacitor:

1. decrease the thickness of the anode foil (t_a)
2. decrease the thickness of the cathode foil (t_c)
3. decrease the thickness of the paper spacers (t_p)
4. increase the foil etching factor (f_e).

Since the cathode foil must be etched, this sets a limit to its minimum thickness. The conventional thicknesses of 20-60 μm cannot be further reduced. The paper spacer must act as a reservoir for the electrolytic and must also protect the anodised surface of the anode foil. Paper thinner than 40-90 μm is not suitable. Since decreasing the

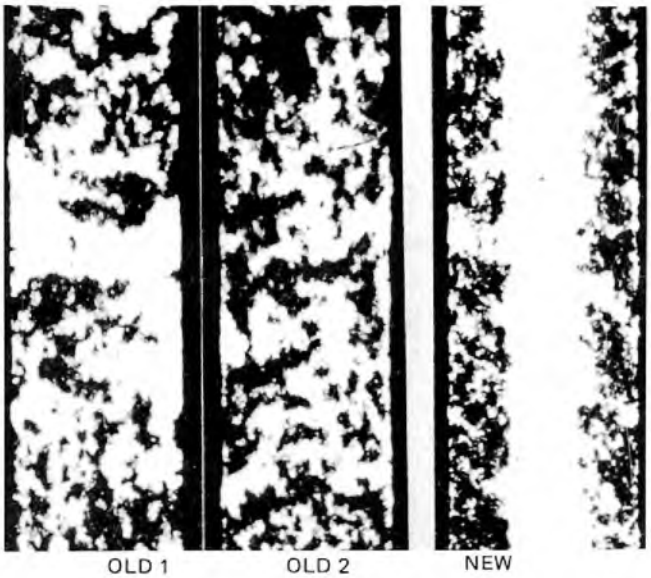


Fig.4 Comparison of anode foil etching

thickness of the anode foil for a given etching factor is not very effective due to the large influence of $t_c + 2t_p$, the only effective method of increasing the volumetric efficiency of an electrolytic is to increase the etching factor for the foil without increasing its thickness.

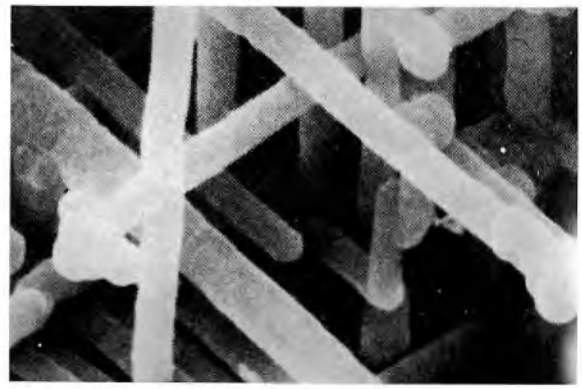
We have recently developed a new process for etching much more densely packed pores in aluminium. This results in an etching factor of about 100 for low voltage foils instead of the etching factor of 50 obtained with conventional etching. Figure 4 compares cross-sections of foils etched by the conventional process and by the new process. Figure 5 shows electron-micrographs of the etch structure and of the oxide in an etched pore.

(a) Scanning electron-micrograph of a replica of the etched structure of anode foil (1 cm = 1 μm)

(b) Transmission electron-micrograph of the oxide layer on the wall of an etched pore (1 cm = 5 X 10^{-3} μm)

Fig.5 Structure of etching and forming by the new process

(a) Scanning electron-micrograph of a replica of etched pores in the anode foil of a low voltage wet electrolytic



(b) Scanning electron-micrograph of a replica of etched pores in the anode foil of a high voltage wet electrolytic

Fig.6 Anode foil structures

The new etching process allows the size of the pores to be controlled so that they can accommodate the required thickness of oxide as dictated by a wide range of rated voltages. Figure 6 shows photo-micrographs of the etch structure for a low-voltage foil and for a high-voltage foil.

Since the etching factor (f_e) is doubled, the volumetric efficiency is doubled and the size of the electrolytics in several of our ranges has been halved. Some examples are shown in Fig.7.

Fig.7 Some examples of increased volumetric efficiency for wet electrolytics

Reducing equivalent series resistance

The equivalent series resistance (ESR) of an electrolytic (and tan δ and impedance which are closely related to it) is a dominant characteristic for many applications. In an SMPS for example, the impedance of the electrolytics becomes increasingly important as the switching frequency is increased. The ESR is determined by the total resistance of the anode and cathode foils (R_f) and the resistance of the paper/electrolyte combination (R_{pe}). Since the paper strips at each side of the cathode foil are connected in parallel, the total ESR of the electrolytic cell is:

$$ESR = R_f + 0.5R_{pe}.$$

A general expression for the resistance of both foils is:

$$R_{a/c} = (\rho_{Al}A)/(0.3w^2t_{a/c})$$

where ρ_{Al} = resistivity of aluminium

A = geometrical foil surface area

0.3 = unetched portion of foil cross-section (see Fig.4(b))

w = foil width

$t_{a/c}$ = thickness of anode/cathode foil.

The resistance of the paper/electrolyte combination is:

$$R_{pe} = (f_R\rho_{el}t_p)/A$$

where f_R = factor by which resistance is increased due to paper density

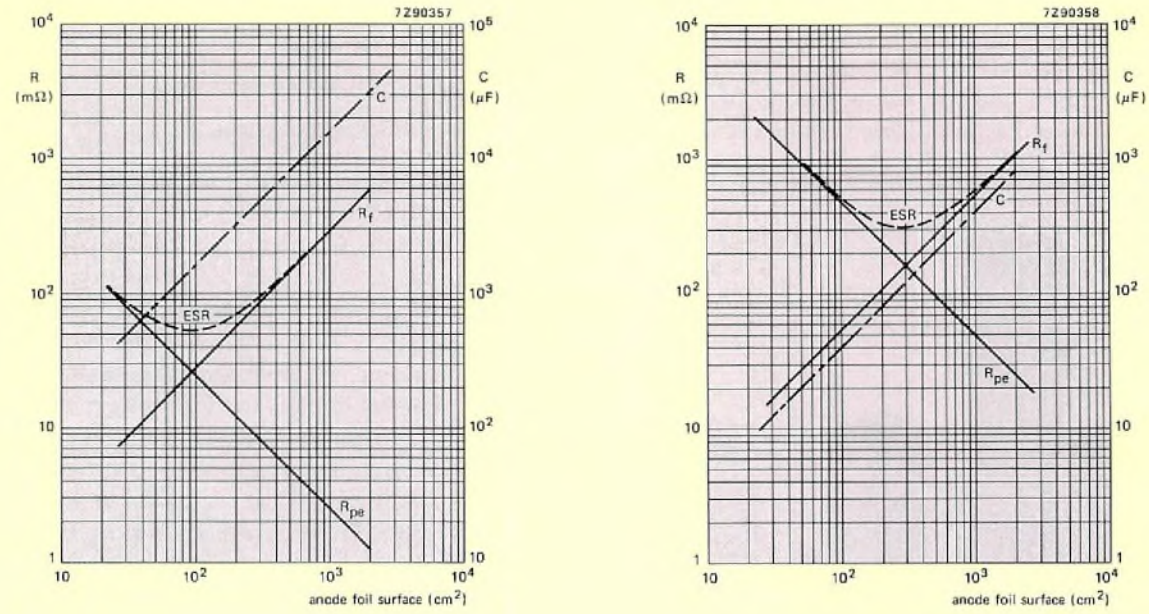
ρ_{el} = resistivity of electrolyte

t_p = thickness of paper.

It was previously shown that, when the volumetric efficiency of an electrolytic is increased by increasing the foil etching factor, the geometrical surface area of foil (A) for a given capacitance is reduced. From the expression for foil resistance ($R_{a/c}$) and resistance of the paper/electrolyte (R_{pe}), it is apparent that, when A is reduced, R_f is reduced and R_{pe} increased. Figure 8 shows the ESR, R_f, R_{pe} and capacitance of low-voltage and high-voltage electrolytics as functions of foil surface area. The illustration shows that, for high CV electrolytics with their long foils, the ESR is mainly foil resistance which decreases as surface area is decreased. ESR is further reduced in some types by using multiple connections to the anode and cathode foils as shown in Fig.3. Figure 8 shows that, for very low CV electrolytics with their shorter foils, and for high-voltage electrolytics with their denser papers and higher resistivity electrolytes, the ESR is mainly electrolyte and paper resistance and increases as surface area A is reduced for a given capacitance. We have eliminated this undesirable effect by introducing new low-resistivity solvent-type electrolytes which have very low water content and are based on dimethyl acetamide (DMA) and dimethyl formamide (DMF). The Table shows that our electrolytics with the new foils and electrolytes (051 and 021 series) have about the same ESR as their predecessors (050 and 032/033 series) despite the fact that their volumetric efficiency has been doubled.

Comparison of volumetric efficiency and ESR for 40 V wet electrolytics

series	value (μF)	CV/vol (μc/cm³)	ESR max (mΩ)
050	4700	4342	48
051	4700	8511	50
032/033	1000	5240	190
021	1000	10863	190



(a) typical low-voltage capacitor

(b) typical high-voltage capacitor

Fig.8 ESR, foil resistance, paper/electrolyte resistance and capacitance as functions of foil surface area

RIPPLE CURRENT CONSIDERATIONS

Effect of increased volumetric efficiency on permissible ripple current

For some applications, the maximum permitted ripple current for an electrolytic is the most important characteristic. Since ripple current causes a temperature rise which reduces life, it is important to understand the relationship between ripple current and temperature rise so that the life expectancy of the electrolytic can be calculated under the actual working conditions.

When ripple current is applied to an electrolytic, the power dissipated in the electrolytic cell is:

$$P = I^2ESR$$

where I = r.m.s. value of ripple current

ESR = equivalent series resistance. Data handbook C14 gives ESR values for 100 Hz sinusoidal ripple currents. For other frequencies and/or waveforms, correction factors must be applied.

Thermal equilibrium occurs when the power dissipated by the electrolytic cell equals the thermal power radiated by the case and convected directly to ambient. The following condition is then fulfilled:

$$I^2ESR = \alpha S \Delta T$$

where α = coefficient of heat transfer for the Al case (about 15 W/m^2K)

S = surface area of the case

ΔT = temperature difference between the surface of the case and ambient.

For our aluminium electrolytics the temperature difference between the core of the electrolytic cell and the case is about the same as that between the case and ambient. The temperature of the electrolytic cell is therefore:

$$T_C = (2I^2ESR)/(\alpha S) + T_a$$

where T_a = ambient temperature.

From this expression it is apparent that if the volumetric efficiency of an electrolytic is increased, its size reduces so that S reduces, and the permissible ripple current for a given T_C is reduced, even if the ESR remains unchanged.

Effect of ripple current on life expectancy

The specified typical life expectancy ($t_{l\ typ}$) of our electrolytics assumes application of the rated voltage and maximum permissible ripple current. Under these conditions, the maximum temperature of the electrolytic cell (T_{max}) is $T_{amb\ max} + 10\ ^{\circ}C$. If the temperature of the electrolytic cell is reduced by 10 °C, the life expectancy of the capacitor (t_l) is doubled. This can be expressed as:

$$t_l = t_{l\ typ}\, 2^{[(T_{max} - I^2K - T_a)/10]}$$

where $k = (2ESR)/(\alpha S)$

Figure 9 shows this expression plotted for equivalent electrolytics from our 050 series (original types) and 051 series (new types).

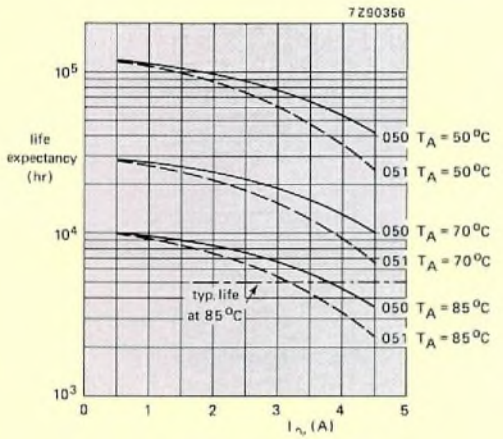


Fig.9 Life expectancy as a function of ripple current with capacitor type and temperature as parameters. The 050 series are original types. The 051 series are new types

ADVANTAGES OF OUR NEW ELECTROLYTES

The water-glycol electrolyte of old-fashioned wet electrolytics is aggressive to the oxide dielectric and causes a high level of leakage current during operation especially after storage. Since, during operation, the high leakage current causes the formation of new oxide to self-heal the eroded dielectric, gas is generated and there is a pressure build-up inside the case. This leads to premature failure.

It is well known that the life expectancy of old-fashioned wet electrolytics is extended if they are operated at well below their rated voltages. There are two main reasons for this:

- the ratio of forming voltage to operating voltage is increased so that there is a greater reserve of oxide dielectric. This allows more time before gas pressure starts to build up after the aggressive electrolyte has reduced the thickness of the oxide dielectric below the level that can withstand the operating voltage
- a bigger capacitor is used for a given capacitance. This results in a reserve of electrolyte and more space to store the gas which is generated during the forming that occurs to self-heal the dielectric as it is eroded by the electrolyte.

It is often believed that electrolytics cannot be stored because the electrolyte is aggressive to the oxide dielectric. This remains valid for old-fashioned wet electrolytics which are still available with aggressive water-glycol electrolytes. It is certainly not valid however for our wet electrolytics with their modern non-aggressive solvent-type electrolytes based on DMA and DMF. These new electrolytes incorporate gas absorbing constituents, have low water content and low resistivity.

Voltage derating not necessary

The electrolyte of our wet electrolytics has very high oxide forming efficiency and incorporates gas absorbing constituents. The anode forming voltage creates a sufficiently thick oxide layer on the anode foil to withstand voltages of at least 20% above the rated voltage. This additional thickness of dielectric is sufficient to maintain a very low level of leakage current which remains low throughout the life of the electrolytic because the electrolyte is non-aggressive. Figure 10 shows the increase of leakage current as the applied voltage is gradually increased. The curve illustrates clearly that operating the capacitor below its rated voltage does not significantly reduce the leakage current.

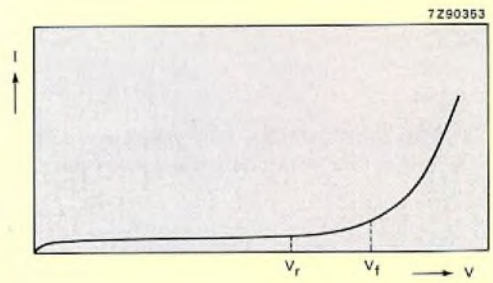


Fig.10 Leakage current as a function of applied voltage

Characteristics remain stable during storage

It is of the utmost importance to the user that an electrolytic capacitor functions correctly immediately following a prolonged period of storage under extreme conditions. The main problem during storage of old-fashioned electrolytics is erosion of the oxide dielectric by the electrolyte which contains more than 10% water that reacts with Al_2O_3 to create $2Al(OH)_3$ or hydrated oxides. Consequently, their leakage current increases considerably after they have been stored. Figure 11 shows that the leakage current increase after storage for two years at ambient temperature is much greater for electrolytics with 30% water-glycol electrolytes than it is for our wet electrolytics with their low water content DMA/DMF electrolytes. Figure 11 also shows that capacitors with electrolytes containing a lot of water take several hours (during which a lot of gas is generated) to reach the low level of leakage current obtained after one minute with our wet electrolytics.

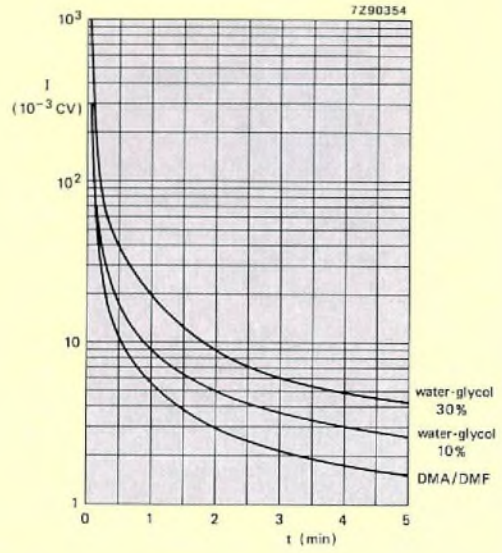


Fig.11 Leakage current at room temperature as a function of time with type of electrolyte as a parameter

RELIABILITY

All our capacitors are the result of an extensive programme of development and testing. An important contributory factor to their reliability is the fact that we manufacture their most important parts and materials ourselves. These include not only the sealing discs and cases, but also (and even more important), the electrolytes, cathode contact foil and, most important of all, the anode foil. In common with all other electronic components, however, some of our wet electrolytics will fail during operation. The failure rate is time-related as shown by the well-known bath-tub curve in Fig.12. The three periods of the curve are:

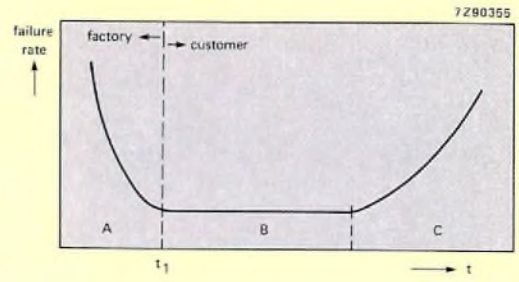


Fig.12 Reliability curve

A: *infant mortality period.* Failures during this period are eliminated during the post-forming procedure which also acts as a burn-in period. Electrolytics are therefore delivered to our customers when they have a failure rate corresponding to instant t_1

B: *service life.* The typical failure rate during this period is 10^{-7}/hr at 40 °C and with the rated voltage applied. It is clear from the previous sections of this article that variations of temperature and voltage within the specified limits will have little influence on the failure rate

C: *wear-out period.* This period is the end of the useful life of the capacitors during which the failure rate gradually increases. The main wear-out mechanism for our wet electrolytics is drying out due to diffusion of the electrolyte. This causes a reduction of capacitance and an increase of ESR above the specified maximum value. For capacitors operated under worst-case conditions, the start of the wear-out period typically occurs after 5 to 10 thousand hours of service.

FUTURE TRENDS

In the future, the upper category temperature of wet electrolytics will be increased to as much 150 °C, and they will be made smaller without increasing the present low levels of ESR. The main high temperature applications for wet electrolytics are military electronics and automotive uses. However, a high upper category temperature is also very desirable for switched mode power supplies and other power electronics applications because it allows a much higher level of ripple current to be tolerated. For example, with an ambient temperature of 70 °C, an electrolytic with an upper category temperature of 125 °C would have a temperature margin of 55 °C. An extra 55 °C temperature rise due to power dissipation caused by additional ripple current could then be tolerated.

Another advantage of an increased upper category temperature is that it results in a considerable increase of life expectancy at lower temperatures. It also allows endurance tests to be accelerated.

The future size reduction of wet electrolytics will allow a much wider capacitance range to be made available on tape for use in automatic placement machines.

Abstracts

Rare-earth cobalt magnets

The high specific energy of super-performance rare-earth cobalt (RES) permanent magnets complements the miniaturization gained with IC technology, resulting in more compact and efficient equipment designs. RES magnets are becoming extensively used in consumer and professional applications in high-efficiency motors, loudspeakers, transducers and actuators.

Multiple loudspeaker arrays using Bessel coefficients

Replacing one large loudspeaker by an array of small ones with the same total power-handling capacity normally results in an altered power response and a highly directional radiation pattern at certain frequencies. These disadvantages can be overcome by proportioning the drive to individual speakers in accordance with coefficients derived from Bessel functions. The coefficients can be chosen in such a way that they are easily realized by connecting the speakers in series and parallel, phase and antiphase combinations.

Silicon temperature sensors

The KTY81/82/83 series of silicon temperature sensors make use of the temperature dependence of resistivity exhibited by silicon. The devices use n-type silicon with a doping level between 10^{14} and $10^{15}/cm^3$. The electrode arrangement – metallized lower plane and circular gold contacts on the upper plane – produces a conical current distribution through the crystal, which significantly reduces the dependence of sensor resistance upon manufacturing tolerances. Operating temperature range extends from −55 to 150 °C for the KTY81, −55 to 175 °C for the KTY83 and 0 to 300 °C for the KTY84.

I^2C bus in consumer applications

Much of today's consumer-oriented electronic equipment contains at least one controller, usually a microcomputer, and a number of ICs performing analogue and digital functions. This article shows how our two-wire bidirectional I^2C bus is the ideal cost-effective interconnection medium. Full details are given of the principles of operation and protocol for the bus.

Quality of high-voltage power transistors

The results from over 10^6 device hours testing of high-voltage power transistors, coupled with field results, indicate a maximum service failure rate of about 10^{-6}/hr. Transistor types tested cover all major areas of application: TV and VDU deflection, electronic ignition, mains inverters, switched-mode power supplies and electronic motor control.

Liquid crystal displays

Thanks to their versatility and low current consumption, LCDs are now the preferred type of display for a wide range of consumer and industrial applications. This article explains the relations between driving voltages, response times, viewing angles, and ambient temperature that govern their operation. Used within the limitations that these imply, they can be expected to give upwards of 100000 hours of service. New types of LCD now coming into use will open still more areas of application.

Recent developments in wet aluminium electrolytics

This article describes how revolutionary manufacturing processes and materials have allowed us to improve the performance of wet aluminium electrolytics. Most of the well-known shortcomings of wet aluminium electrolytics have now been eliminated. The new components are no longer only suitable for the less stringent requirements of the consumer market. They can also perform important roles in professional and industrial applications such as high-speed data systems and fast switching power supplies operating at high power levels.

Seltenerd-Kobalt-Magnete

Die hohe Energiedichte der Hochleistungs-Seltenerd-Kobalt–Permanentmagnete (RES) führt in gleicher Weise zur Miniaturisierung wie IC-Technologien. Mit RES-Permanentmagneten lassen sich äusserst kompakte und leistungsstarke Geräte entwickeln. Daher werden diese Magnete immer mehr sowohl für konsumorientierte als auch für professionelle Applikationen verwendet, z.B. für Motoren mit hohem Wirkungsgrad, Lautsprecher, Wandler und Aktuatoren.

Entwurf vom Mehrfachlautsprecheranordnungen auf der Basis von Bessel-Koeffizienten

Wird ein grosser Lautsprecher durch eine Anordnung von mehreren kleinen Lautsprechern mit gleicher Gesamt-Nennbelastbarkeit ersetzt, dann ergibt sich normalerweise ein geänderter Frequenzgang und bei bestimmten Frequenzen ein stark gerichtetes Strahlungsfeld. Diese Nachteile können beseitigt werden durch geeignete Aufteilung der Ansteuerleistung auf die einzelnen Lautsprechersysteme gemäss der sich aus Besselfunktionen ergebenden Koeffizienten. Die Wahl dieser Koeffizienten kann so erfolgen, dass die benötigte Aufteilung leicht durch Serien- und Parallelschalten der Lautsprechersysteme in Gleich- und Gegenphasenerregung erreichbar ist.

Silizium-Temperatur-Sensoren

Die Silizium-Temperatur-Sensoren der Serie KTY81/83/84 machen von der Widerstandsabhängigkeit des Siliziums von der Temperatur gebrauch. Es wird N-Silizium mit einer Dotierungskonzentration von 10^{14} bis 10^{15} cm^{-3} verwendet. Die Anordnung der Elektroden – untere Fläche metallisiert, obere Fläche mit ringförmigen Goldelektroden versehen – bewirkt im Kristall eine konische Stromverteilung, welche die Abhängigkeit des Sensorwiderstands von Fertigungstoleranzen wesentlich herabsetzt. Die Arbeitstemperaturbereiche sind: −55 bis 150 °C für KTY81, −55 bis 175 °C für KTY83 und 0 bis 300 °C für KTY84.

I^2C-Bus in Konsumgeräte-Applikationen

Viele der heutigen konsumorientierten elektronischen Geräte enthalten mindestens eine Steuerschaltung, meist in Form eines Mikrocomputers, ausserdem eine Anzahl integrierter Schaltungen zur Ausführung analoger und digitaler Funktionen. Dieser Beitrag macht deutlich, dass unser bidirektionaler 2-Draht-I^2C-Bus die ideale, kosteneffektive Verbindungslösung darstellt. Die Arbeitsprinzipien und die zugehörigen Bus-Protokolle werden im Detail beschrieben.

Qualität von Hochvolt-Leistungstransistoren

Die Prüfergebnisse der Hochvolt-Leistungstransistoren aus über 10^6 Bauelementestunden liefern für den praktischen Einsatz eine maximale Ausfallrate von 10^{-6}/h. Die geprüften Transistoren überdecken alle wichtigen Anwendungsbereiche: Fernseh- und Monitorröhrenablenkung, elektronische Schalter, Wechselrichter, Schaltnetzteile und elektronische Motorsteuerung.

Flüssigkristall – Displays

Dank ihrer Vielseitigkeit und ihres niedriegen Stromverbrauchs stellen LCDs für viele Konsumer- und Industrie-Anwendungen die verbreitetste Art von Displays dar. Dieser Artikel erklärt die Zusammenhänge zwischen Ansteuerspannung, Abklingzeit, Ablesewinkel und Umgebungstemperatur, Grössen, die den Einsatz der Displays bestimmen. Betreibt man die Displays innerhalb der vorgegebenen Grenzen, kann man mit über 100 000 Betriebsstunden rechnen. Die neu zum Einsatz kommenden LCD-Typen werden noch mehr Einsatzgebiete eröffnen.

Neue Entwicklungen bei Elektrolytkondensatoren mit nassem Elektrolyten

Dieser Artikel beschreibt, wie durch revolutionäre Änderungen des Fertigungsprozesses und der verwendeten Materialien eine Verbesserung der Eigenschaften von Elektrolytkondensatoren mit nassem Elektrolyten erzielt wurde. Die meisten der diesen Kondensatoren bisher anhaftenden Unzulänglichkeiten konnten beseitigt werden. Die neuentwickelten Kondensatoren sind nicht mehr nur für die weniger strengen Anforderungen im Konsumer-Bereich geeignet. Sie sind jetzt auch in der Lage, eine bedeutende Rolle bei professionellen und industriellen Anwendungen zu übernehmen, wie z.B. bei schnellen Datenübertragungs-Systemen und bei Schaltnetzteilen mit hoher Betriebsfrequenz.

Aimants terre rare/cobalt

L'énergie spécifique élevée des aimants permanents super-performants terre rare/cobalt (RES) permet une miniaturisation des produits développés, rendant ainsi possible la conception de matériels plus compacts et plus efficients. L'emploi des aimants est de plus en plus fréquent dans des moteurs de haut rendement, des haut-parleurs, des transducteurs et actuateurs pour applications professionnelles et Grand Public.

Ensembles de haut-parleurs basés sur les coefficients de Bessel

Le remplacement d'un haut-parleur de grandes dimensions par un ensemble de haut-parleurs de petites dimensions possédant la même puissance globale a normalement pour résultat une altération de la réponse en puissance et une répartition fortement directionnelle du rayonnement à certaines fréquences. Il est possible de remédier à ces inconvénients en appliquant à chaque haut-parleur une excitation des pondérée suivant des coefficients issus des fonctions de Bessel. On peut choisir les coefficients de telle manière qu'ils soient aisés à obtenir en connectant les haut-parleurs suivant des combinaisons série-parallèle, phase – opposition de phase.

Capteurs de température au silicium

Les capteurs de température au silicium de la série KTY81/83/84 sont basés sur la variation de la résistivité du silicium en fonction de la température. On utilise le silicium type *n* à niveau de dopage compris entre 10^{14} et $10^{15}/cm^3$. La disposition des électrodes – plan inférieur métallisé et contacts dorés circulaires sur le plan supérieur – produit une répartition conique du courant qui traverse le cristal, ce qui réduit sensiblement l'influence des tolérances de fabrication sur la résistance du capteur. La gamme des températures d'utilisation va de −55 à 150 °C pour le KTY81, −55 à 175 °C pour le KTY83 et 0 à 300 °C pour le KTY84.

Bus I²C dans applications Grand Public

Les appareils électroniques Grand Public actuels contiennent au moins une unité de commande, généralement un micro-ordinateur, et un certain nombre de circuits intégrés remplissant des fonctions analogiques et digitales. Il est montré dans cet article que notre BUS bifilaire et bidirectionnel I²C est l'interconnexion idéale du point de vue coût-efficacité. Le principe de fonctionnement et le protocole du BUS sont expliqués en détail.

Qualité des transistors pour alimentation haute tension

Cette publication est consacrée à une étude de la qualité des transistors pour alimentation haute tension Philips effectuée en 1980, 1981 et 1982. Compte tenu des résultats de plus de 10^6 heures d'essai et d'utilisation pratique, le taux de panne en service est d'environ 10^{-6}/heure.

Affichage à cristaux liquides

Grâce à leur souplesse d'utilisation et à leur faible consommation de courant, les cristaux liquides sont maintenant le mode d'affichage le plus courant dans une large variété d'applications industrielles et Grand Public. Cet article explique les relations entre les divers paramètres: tension d'excitation, temps de réponse, angle d'observation et température ambiante, qui régissent leur fonctionnement. Employés dans les limites que ces paramètres impliquent, leur durée de vie peut dépasser 100 000 heures. Les nouveaux types de cristaux liquides récemment apparus ouvriront de nouveaux domaines d'application.

Développements récents dans les condensateurs électrolytiques

L'article décrit comment des procédés de fabrication et de traitement des matériaux ont permis d'améliorer les performances des condensateurs électrolytiques. La nouvelle technologie permets dès maintenant de produire des composants dont les caractéristiques répondent non seulement aux exigences du marché Grand Public, mais aussi à celles des marchés professionnells et industriells, notamment les matériels informatiques et les alimentations à découpage.

Imanes de cobalto de tierras raras

La alta energía específica de los imanes permanentes con superprestaciones en cobalto de tierras raras complementa la miniaturización ganada con la tecnología de los circuitos integrados, dando lugar a diseños de equipos eficientes y más compactos. Los imanes de cobalto de tierras raras están siendo muy utilizados en aplicaciones profesionales y de consumo: motores de alto rendimiento, altavoces, transductores, y actuadores.

Redes múltiples de altavoces que utilizan los coeficientes de Bessel

Reemplazando un altavoz grande por una red de altavoces pequeños con la misma capacidad total de manejo de potencia se obtiene una diferente respuesta en frecuencia y un diagrama de radiación altamente direccional a ciertas frecuencias. Estas desventajas se pueden superar proporcionando una excitación a los altavoces individuales de acuerdo con los coeficientes obtenidos de las funciones de Bessel. Se pueden elegir los coeficientes de forma que sea fácil de realizar conectando los altavoces en serie y en paralelo, y combinaciones en fase y contrafase.

Sensores de temperatura de silicio

La serie KTY81/84 de sensores de temperatura de silicio hace uso de la dependencia de la temperatura de la resistividad presentada por el silicio. Los dispositivos utilizan silicio tipo N con un nivel de dopado entre 10^{14} y $10^{15}/cm^3$. La disposición de los electrodos – plano inferior metalizado y contactos de oro circulares en el plano superior – produce una distribución de corriente cónica a través del cristal, lo que reduce significativamente la dependencia de la resistencia del sensor en las tolerancias de fabricación. El margen de temperaturas de funcionamiento se amplía desde − 55 a 150 °C para el KTY81, de −55 a 175 °C para el KTY83 y de 0 a 300 °C para el KTY84.

Bus I²C en aplicaciones de consumo

Muchos de los equipos electrónicos actuales orientados a consumo contienen como mínimo un controlador, usualmente un microordenador, y algunos circuitos integrados que realizan funciones analógicas y digitales. Este artículo muestra como nuestro bus bidireccional de dos hilos I²C es el medio de interconexión ideal y con un coste efectivo. Se dan todos los detalles de los principios de funcionamiento y protocolos para el bus.

Calidad de los transistores de potencia de alta tensión

Esta publicación estudia la calidad de los transistores de potencia de alta tensión medida durante 1980, 1981 y 1982. Los resultados de nuestras pruebas de 10^6 horas-dispositivo, junto con los resultados de campo, indican una tasa de fallos en funcionamiento de 10^{-6}/hora.

Visualizadores de cristal líquido

Gracias a su versatilidad y bajo consumo de corriente, los visualizadores de cristal líquido son actualmente el tipo de visualizador preferido para una amplia gama de aplicaciones industriales y de consumo. Este artículo explica las relaciones entre las tensiones de excitación, tiempos de respuesta, ángulos de visión, y temperatura ambiente, que gobiernan su funcionamiento. Utilizados dentro de las limitaciones que éstas implican, puede esperarse más de 100.000 horas de servicio. Los nuevos tipos de visualizadores de cristal líquido (LCD) tendrán cada vez más areas de aplicación.

Ultimos desarrollos en condensadores electrolíticos húmedos de aluminio

Este artículo describe como se han logrado unos materiales y procesos de fabricación revolucionarios para mejorar las prestaciones de los condensadores electrolíticos húmedos de aluminio. Se ha eliminado la mayoría de los conocidos defectos de los condensadores electrolíticos húmedos de aluminio. Los nuevos componentes no son más largos, adecuados únicamente para los requisitos menos severos del mercado de consumo; también pueden realizar papeles importantes en aplicaciones industriales y profesionales tales como sistemas de datos de alta velocidad y fuentes de alimentación de conmutación rápida que trabajan con altos niveles de potencia.

Authors

August Petersen, was born near Flensburg, Germany, in 1937, and graduated in phyiscs from the University of Kiel in 1964. The same year he joined Valvo Application Laboratory, Hamburg, initially working on applications of passive components, especially piezo-electric ceramics. As a member of the Industrial Electronics Group, he is currently responsible for developing sensor control circuitry.

Andreas D. Schelling was born in Dussnang, Switzerland in 1953. He received an MSc in electrical engineering from the Federal Institute of Technology, Zurich, after which he worked for a time at Nippon Telephone and Telegraph, Japan. In 1982 he joined Videlec – a joint Philips/Brown Boveri venture in Lentzburg, Switzerland, and is currently responsible for technical sales support of liquid crystal displays.

J. Dijk was born in Zuidlaren, The Netherlands in 1946. He studied electronics at Groningen, completing his studies in 1967. In 1970 he joined Philips' Quality Laboratory for Semiconductors, Stadskanaal, and is currently working in the area of power transistors.

Helfried Schmickl studied mechanical and electrical engineering and took his doctorate at the University of Technology, Graz, Austria, in 1970. After working on capacitor development for Siemens G.m.b.H., Deutschlandberg, he joined Philips in 1973 and since 1977 has been in charge of electrolytic capacitor development, first at Klagenfurt and, since 1979, as development chief at Zwolle. He is a reader in television engineering at the University of Technology, Graz.

Wil J. W. Kitzen was born in Grevenbicht, The Netherlands in 1955. He studied electrical engineering at Eindhoven University of Technology, receiving his MSc in 1979. The same year he joined Philips Research Laboratories, Eindhoven, initially working on loudspeaker arrays, dummy-head stereophony and room acoustics. Since 1980 he has worked on digital signal processing techniques in the field of electro-acoustics.

Just W. H. Slakhorst received his degree in materials science from Twente University of Technology in 1973, and his doctorate from the Dutch Foundation for Fundamental Research of Matter, in 1977. The same year he also received the Brandoma Award for his work on recrystallization textures. He joined Philips Elcoma Division, Zwolle in 1978, and is currently responsible for development of wet electrolytic capacitors and for production of capacitor foils.

A. P. M. Moelands was born at Breda, The Netherlands, in 1951. After graduating in electrical engineering at the University of Technology, Eindhoven, in 1976, he joined Philips Electronic Components and Materials Division where he was instrumental in the development of the 8400 serial I/O. He is now a member of the product marketing group *MOS microprocessors*.

Ad M. M. Otten joined Philips Research Laboratories, Geldrop, The Netherlands in 1964, after completing his studies at Eindhoven Polytechnic. Initially he worked on electron and ion optics. In 1978 he moved to Philips Elcoma Division, and since that time he has been responsible for marketing electrolytic capacitors.

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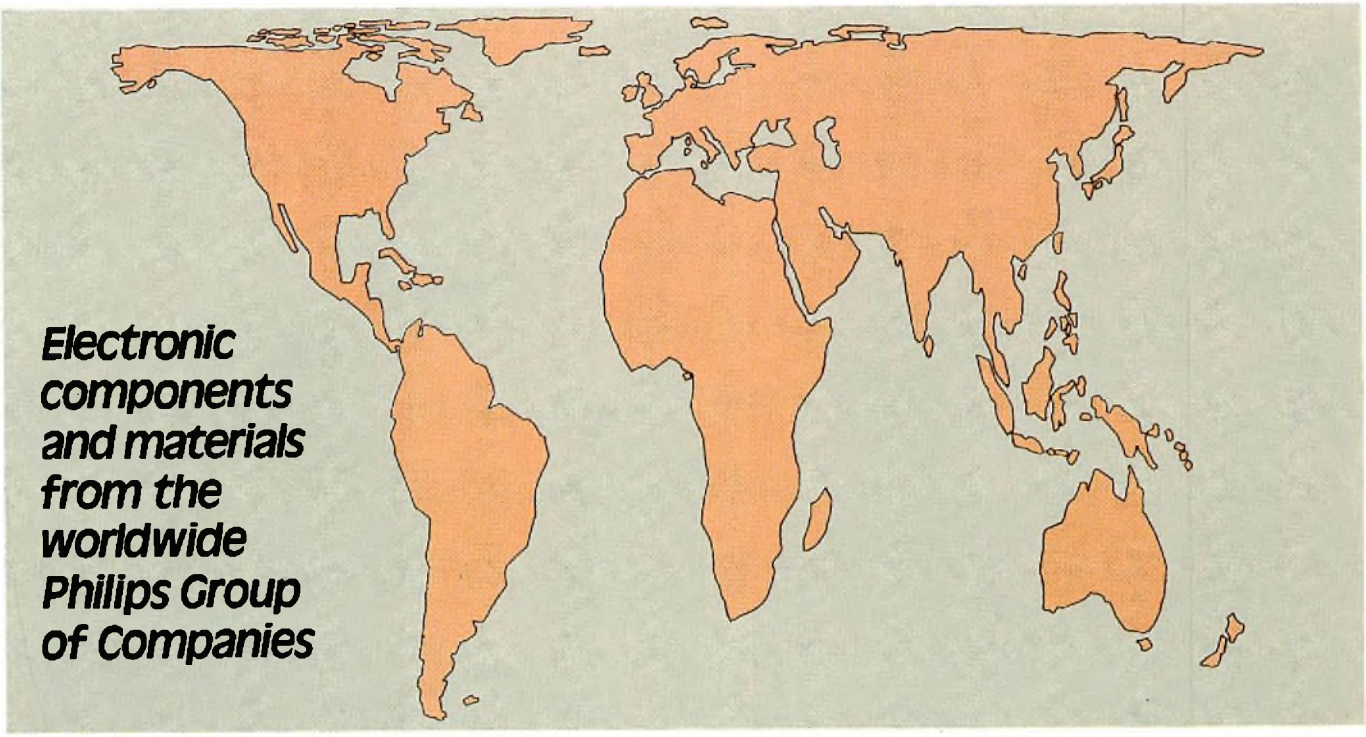

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