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Theory, technology, and demand seldom go forward hand in hand. Symbolic of the sort of pivotal development likely to occur when they do come together is the jumbo jet pictured on the cover of this issue. Less striking visually but no less to the point is the gate turn-off switch described in the article starting on page 194. The theory underlying its structure and operation was well-known a decade ago, only to await the manufacturing technology. Recent advances in ion implantation, neutron doping, and fine-line photolithography supplied that. Now the need to make more efficient use of costlier energy is generating a demand that promises to make the gate turn-off switch as commonplace in the world of power control as the jumbo jet has become in air transport.
(Photo courtesy of Luchthaven Schiphol)

Contents

Gate turn-off switch

F. BURGUM, E. B. G. NIJHOF, and A. WOODWORTH

The gate turn-off switch* is one of the most versatile switching devices yet developed, incorporating the advantages of both the thyristor and the high-voltage switching transistor. It is a fast three-terminal four-layer pnpn device similar in construction to the conventional thyristor. Like the thyristor and the ASCR, the gate turn-off switch (or GTO) can be turned *on* by positive gate drive; but like the transistor it can also be turned *off* by negative gate drive. It combines the inherently *high blocking voltage* and *high overcurrent capability* of the thyristor with the *ease of gate drive* and *fast switching* associated with bipolar transistors and darlingtons. The GTO also operates with low gate currents and offers outstanding static and dynamic dV/dt performance.

Based on new concepts and using new materials and techniques, GTOs can now be mass-produced with properties suitable for a very wide range of applications. This article describes the GTO, what it is, how it works, and how it compares with other fast switches. Methods of drive are considered and some simple application ideas are outlined.

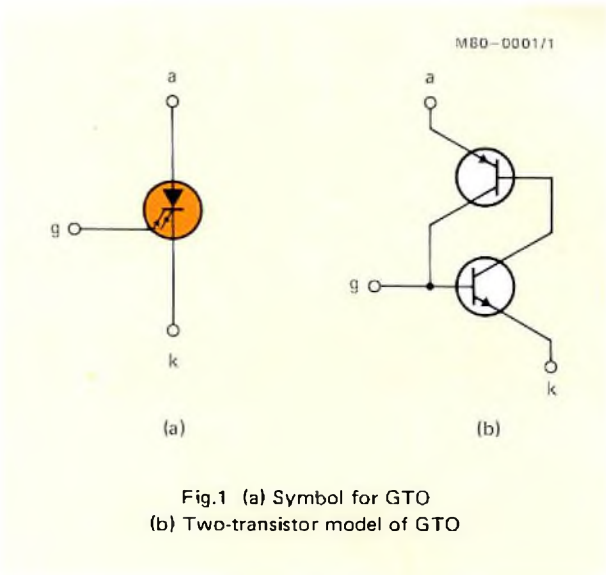


Fig.1 (a) Symbol for GTO
(b) Two-transistor model of GTO

OPERATION

Like the thyristor, the operation of a GTO can be considered in terms of a simplified two-transistor model (Fig.1). When positive gate drive is applied to the base of the npn transistor, the transistor turns on, and its collector, which is also the base of the pnp transistor, is driven low. The pnp transistor then turns on and its collector current flows into the base of the npn transistor, setting up regenerative conditions. If the main current I_a is sufficient for the sum of the transistor gains to exceed unity ($\alpha_{npn} + \alpha_{pnp} \geqslant 1$), the device will latch; that is, remain on. Unlike the thyristor, the GTO is designed so that negative gate drive can be used to interrupt regeneration and turn off the device. This is achieved by making α_{npn} relatively large and α_{pnp} small. In practice, α_{npn} is maximised by careful control of the diffusion profiles, and α_{pnp} is minimised by making the base wide, by controlling the carrier lifetime, and by controlled shorting of the emitter. Such control is only possible with the latest ion implantation, neutron doping, photolithographic, and process control techniques

*Sometimes referred to as a latching transistor or gate-controlled switch (GCS).

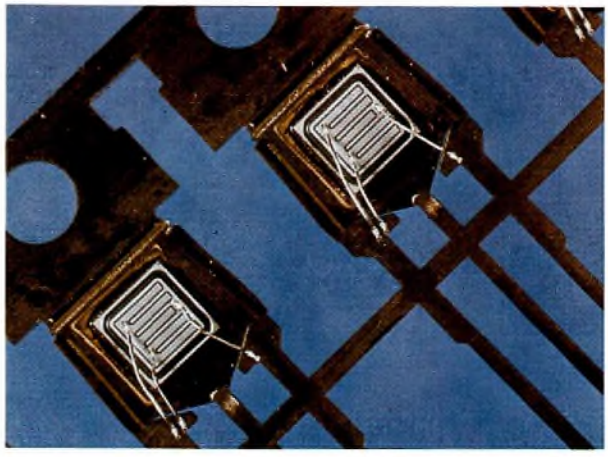


Fig.2 BTW58 GTO

utilised in the manufacture of GTOs. Figure 2 shows the structure of a BTW58 GTO; the gate and cathode are interdigitated to achieve the required low gate resistance.

The four-layer structure of the GTO gives it several advantages over three-layer switches such as transistors and darlingtons. The most obvious of these is that a four-layer device has an inherently higher stand-off voltage. A second advantage is that in a four-layer device, the latching action is provided by a built-in gain; this means that the higher the current, the more the GTO saturates, unlike the transistor which comes out of saturation at higher currents. Thus a smaller chip can be used. The GTO also has a higher overload capability than a transistor and can be protected by a fuse.

In the BTW58, gold doping is used to obtain a lower storage time and a faster, cleaner turn-off (less than 0.5 μs) compared with high-voltage bipolar devices or thyristors. The permissible rate of rise of reapplied off-state voltage, 1000 V/μs, is also far superior to present-day bipolar switches.

In any switch, a low drive current requirement is advantageous. However, in a GTO a low gate drive ($\simeq$10 mA) would necessitate a high internal gain which in turn would make the device difficult to turn off. A compromise is therefore necessary between gate drive and turn-off performance.

The BTW58 requires only about 100 mA to switch on 5 A, while fast switch-off ($<$0.5 μs) is achieved by applying a negative gate voltage of $\geqslant$5 V.

COMPARISON WITH OTHER POWER SWITCHES

Table 1 summarises how the GTO compares with a number of other power switches. Figure 3 indicates areas of operation in terms of voltage and frequency for the

TABLE 1

Comparison of power switches

Device	On-state dissipation	Ease of turn-on	Ease of turn-off	Switching frequency	Overcurrent capability	Chip area
GTO	Moderate	Moderate (regenerative)	Good	Good	Good (10 to 15×)	Small
Thyristor (conventional)	Low	Good (regenerative)	Very poor (external commutating devices required)	Very poor	Very good (20×)	Small
ASCR	Low	Good (regenerative)		Moderate	Very good (20×)	Small
Darlington with speed-up	Moderate	Moderate (non-regenerative)	Moderate	Good	Poor	Moderate
Bipolar transistor	Low	Poor (non-regenerative)	Moderate	Good	Poor	Moderate
VMOS	High	Very good but capacitive (non-regenerative)	Very good	Very good	Moderate	Large

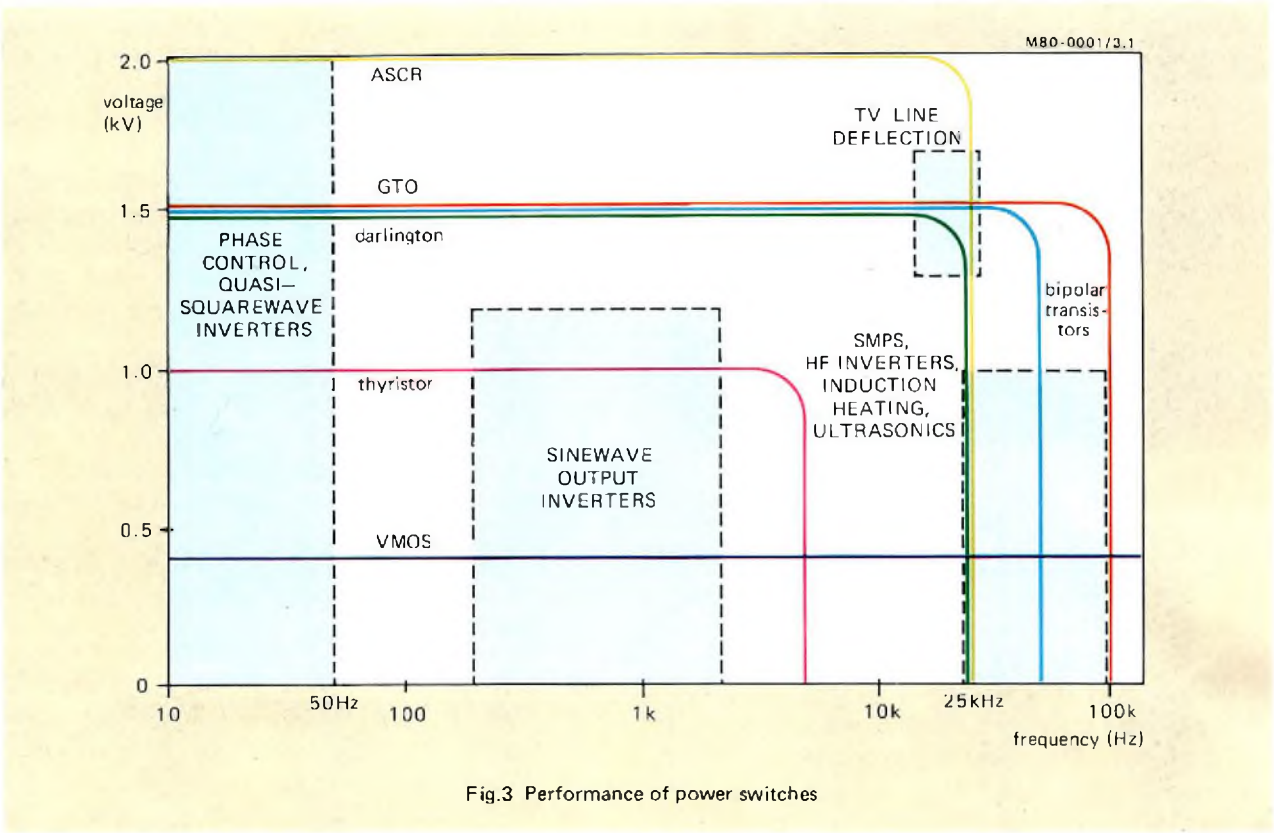


Fig.3 Performance of power switches

various switching devices in Table 1. It also shows typical areas of application for comparison.

DRIVE CIRCUITS

The GTO operates with very short switching times for both turn-on and turn-off, less than 0.5 μs for the BTW58. However, to achieve this performance in practice, it is essential that the device is driven correctly. Figure 4 shows the basic method of drive.

To turn the GTO on, a positive current must be injected into the gate for the duration of the time necessary for turn-on. This continuous drive reduces the forward voltage drop at low anode currents (below about 2 A for a BTW58) and thus minimises losses.

Turn-off is achieved by drawing from the gate a current pulse of between 20 and 100% of the anode current for a few hundred nanoseconds. This is done by applying a negative voltage of between −5 and −10 V directly between gate and cathode.

If the impedance of the gate turn-off circuit is sufficiently low, unity turn-off gain is achieved. Under these conditions, all the anode current is diverted into the gate, turning off the cathode before the anode voltage has started to rise. With unity turn-off gain, the slow-rise circuit indicated in Fig.4 is not required and circuit dissipation is reduced.

Three practical drive circuits for the BTW58, based

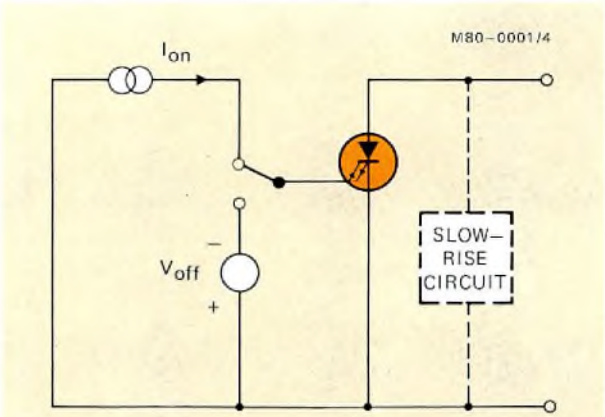


Fig.4 Basic drive circuit

on the turn-off circuit in Fig.4, are shown in Figs.5, 6, and 7. In all three, the negative turn-off voltage is switched from a capacitor charged during the on-time of GTO to a level set by a voltage regulator diode.

Figure 5 shows a simple direct gate-drive circuit. With TR_2 turned off, positive gate drive current flows from the d.c. supply rail to the GTO via the emitter follower TR_1. When TR_2 is turned on, TR_1 turns off and a negative voltage of about 10 V, set by D_2, is applied to the gate of the GTO. As long as TR_2 is on, the gate voltage will remain negative because the reverse gate resistance

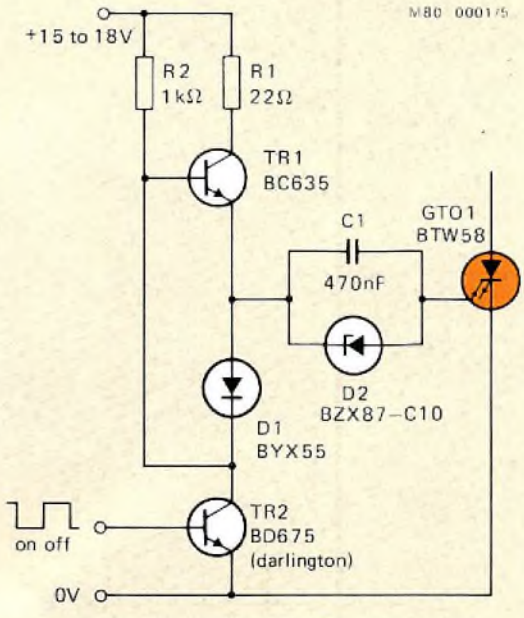


Fig.5 Simple direct gate drive circuit

of the GTO in the non-conducting state is high and C_1 will therefore only discharge slowly. A GTO anode current of up to about 10 A can be turned off with this circuit; for lower currents, a lower value voltage regulator diode can be used.

The main drawback of this simple circuit is that the positive turn-on current is dependent on the supply voltage. A modified circuit in which this dependency is reduced is shown in Fig.6. In this circuit, TR_1 is a current source which gives the required positive gate drive. Diode D_1 in Fig.5 is now omitted and consequently the impedance in the negative gate current path is reduced, making the circuit better suited to operation with unity turn-off gain.

If the anode dI/dt is high, capacitor C_2 should be included to ensure that the initial gate current is large, hence reducing turn-on loss.

An isolated GTO drive circuit is given in Fig.7. When a positive signal is applied to the base of TR_1, the transformed current in the secondary flows as positive gate current into the GTO. Diode D_4 conducts and TR_2 turns off. As in the other circuits, C_1 charges to the zener voltage of D_5 during the GTO on-time. When TR_1 is turned off, TR_2 turns on and the voltage on C_1 is applied to the gate of the GTO, turning it off. The combination R_1 D_3 limits the peak primary voltage caused by magnetisation current.

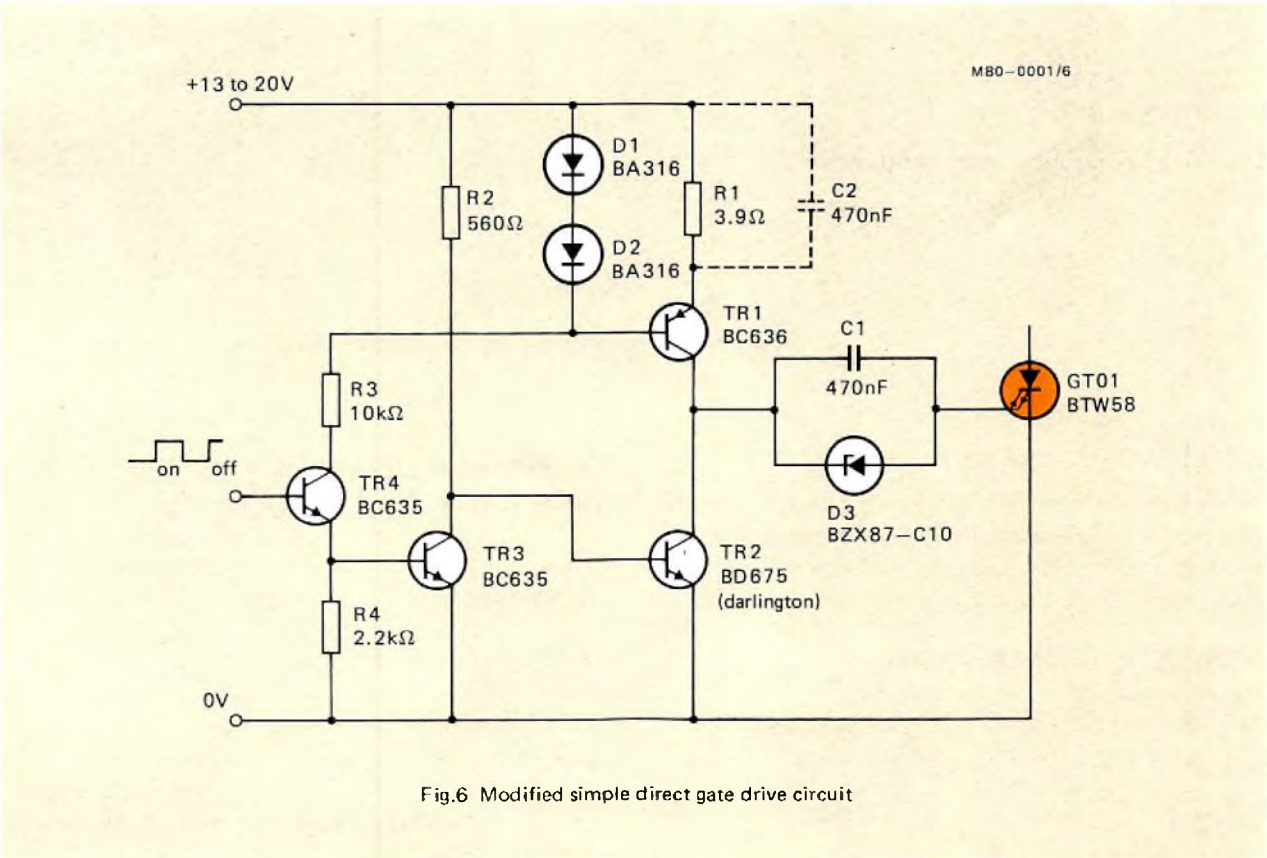


Fig.6 Modified simple direct gate drive circuit

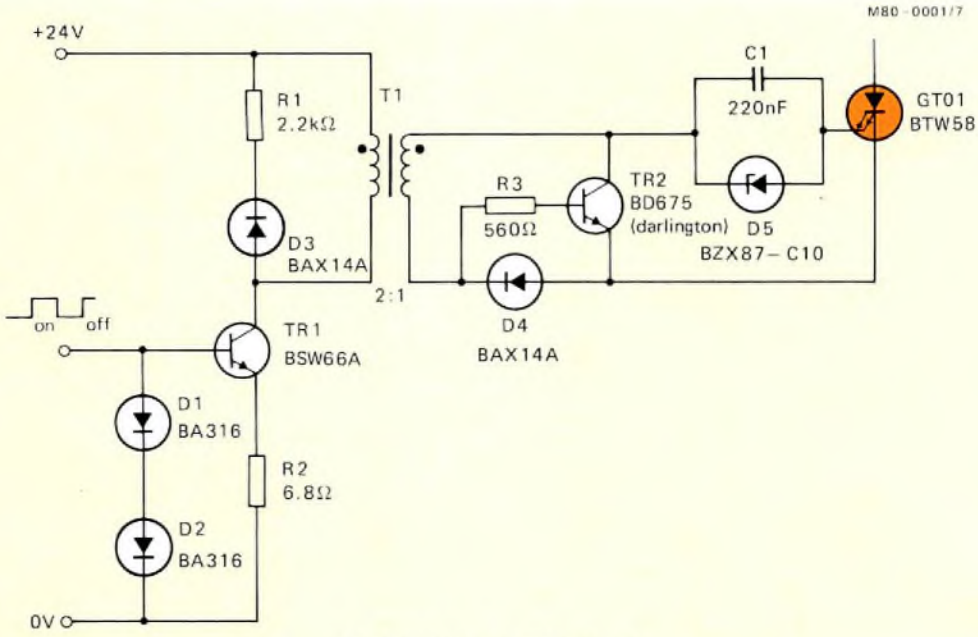


Fig.7 Isolated gate drive circuit

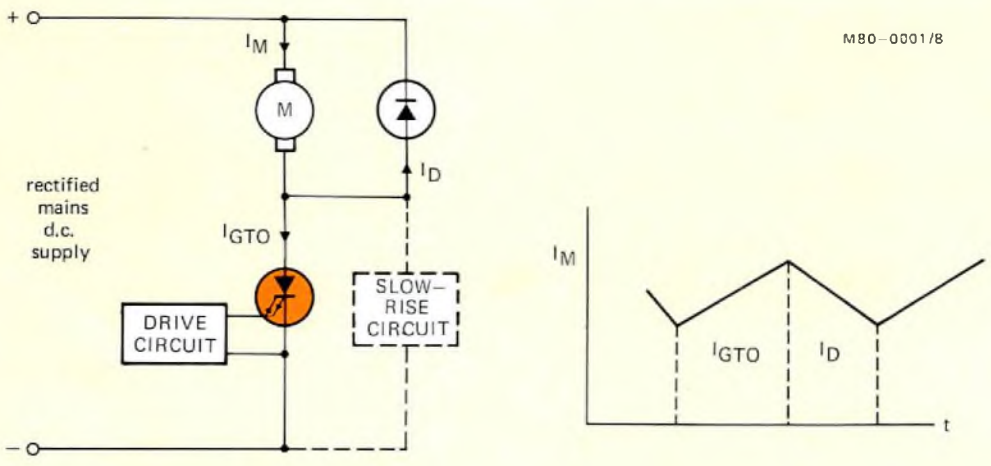


Fig.8 D.C. motor chopper control

APPLICATION AREAS

As mentioned earlier, the high forward blocking voltage, ease of drive, and fast switching capability of the GTO make it eminently suitable for use in a vast range of applications. These include:

- **INDUSTRIAL APPLICATIONS**

Power supplies	–	general
A.C. inverters	–	a.c. motor control
		induction heating
		ultrasonic cleaning
Lighting	–	starters; ballast
Automobiles	–	ignition

- **DOMESTIC APPLIANCES**

Motor control	–	white goods
		small appliances
Power control	–	microwave cookers
Ignition systems	–	gas

- **TELEVISION**

Power supplies
E.H.T. regulation
Line deflection

A few of these applications are outlined briefly in the following pages

D.C. motor control

Figure 8 shows the basic configuration for the PWM control of a d.c. motor; no commutation circuit is required. The switching frequency is chosen so that the switching period is much less than the L/R time-constant of the motor to ensure that the motor current is continuous. The slow-rise circuit may not always be needed, depending on the drive circuit used.

Figure 9 shows a d.c. motor controller which uses a second GTO and allows regenerative braking. When GTO2 is turned on for a short time, the back e.m.f. of the motor transfers energy into the motor inductance. When GTO2 is tuned off, this energy is returned to the supply.

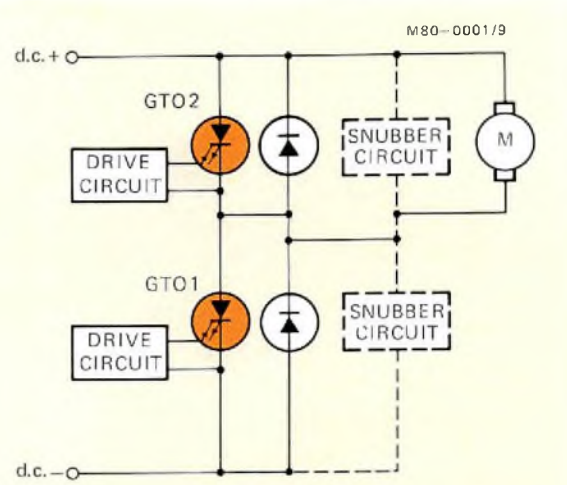


Fig.9 D.C. motor chopper control with regenerative braking

A.C. motor control

A basic configuration for a variable-speed three-phase a.c. motor controller is shown in Fig.10. The circuit is much simpler than that of a similar controller using thyristors because no commutation circuits are needed. The GTO is more able to withstand high peak voltages (1000 V) than a transistor and its high surge current capability enables it to be protected by fuses.

Full-wave a.c. controller

Figure 11 shows a simple a.c. mains chopper by means of which any part of the waveform can be applied to the load. This can be used to give a better power factor and reduced harmonic pollution compared with conventional

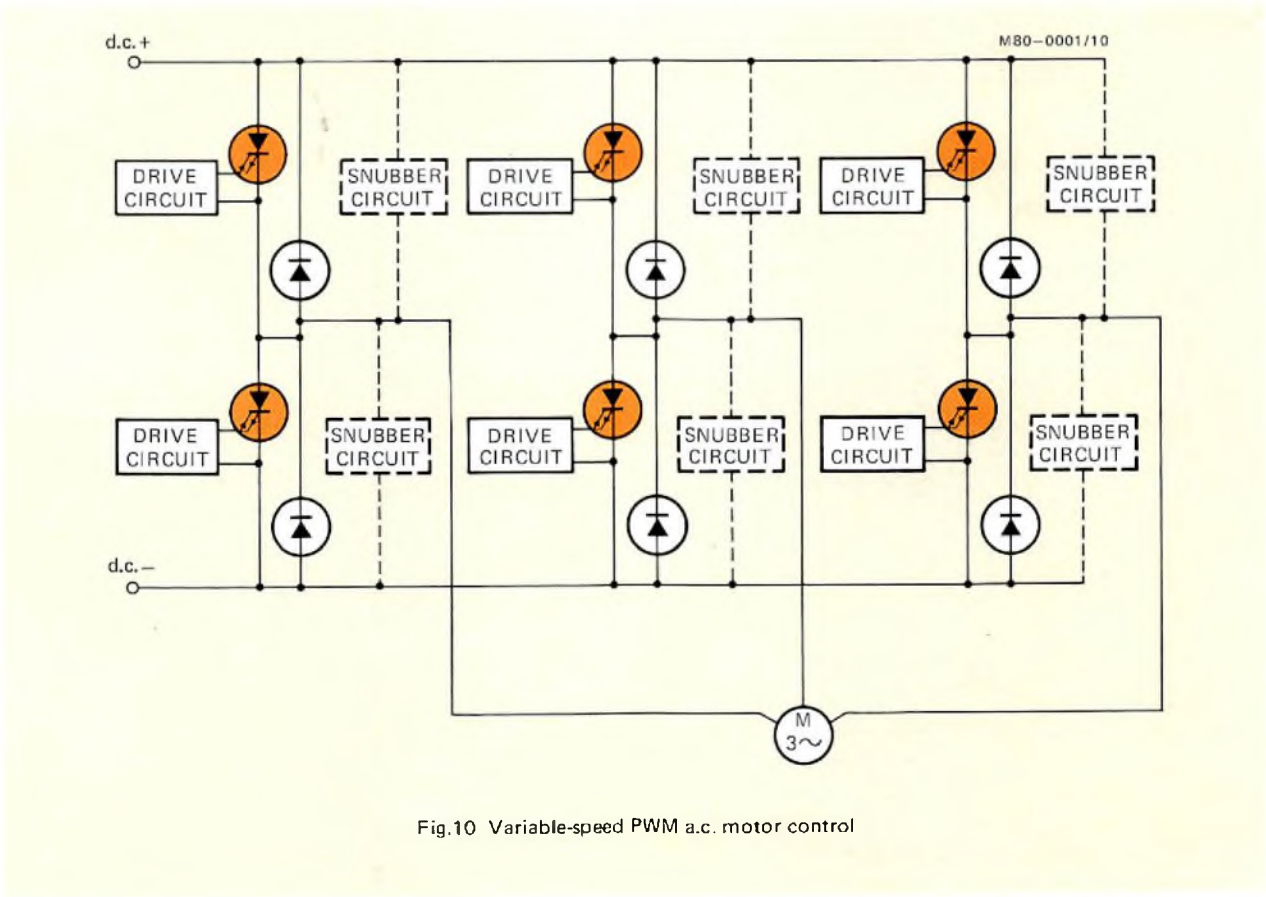


Fig.10 Variable-speed PWM a.c. motor control

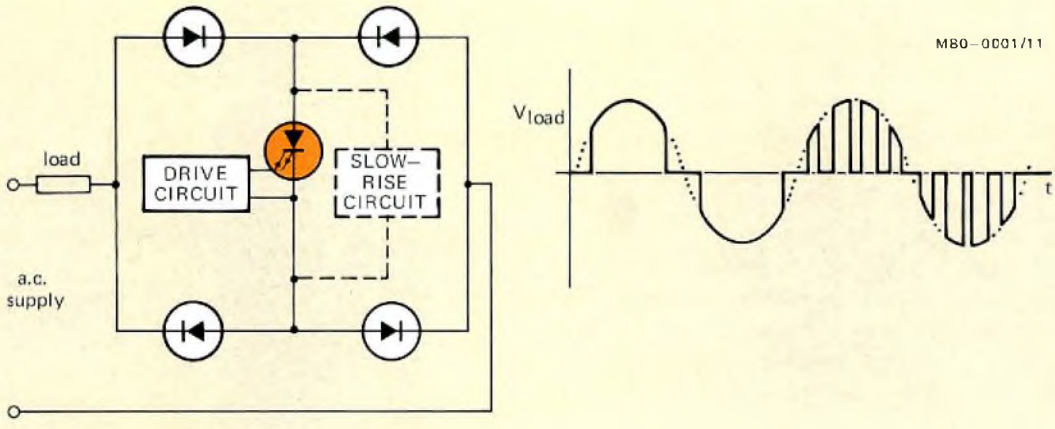


Fig.11 Full-wave a.c. mains chopper controller

thyristor phase-control circuits. The circuit also has good overload properties in that the load voltage can be turned off on demand, whereas with a thyristor, a delay of up to 10 ms is required.

Switched-mode power supplies

When used in switched-mode power supplies, the GTO is more rugged than a transistor which is limited by its SOAR characteristic. The output stage of an isolated flyback converter is shown in Fig.12.

Series-resonant converter

The GTO is well suited for use in series-resonant circuit switched-mode power supplies (SRPS), where the reduced dI/dt may lead to less r.f.i. and lower switching losses (increased efficiency) compared with conventional switched-mode circuits (Fig.13).

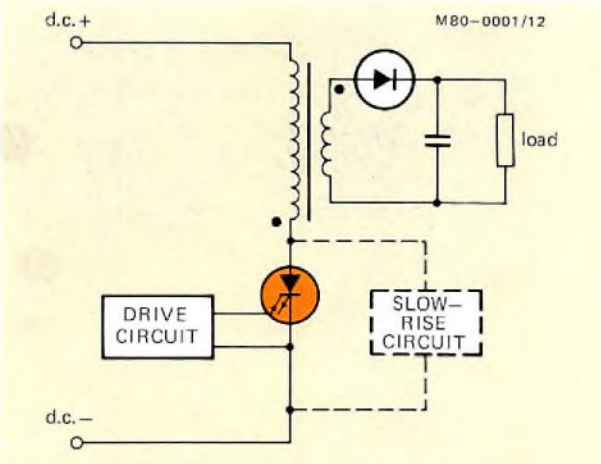


Fig.12 Isolated flyback switched-mode power supply

TV deflection

The use of a GTO in tv deflection circuits offers a high peak voltage capability and a high surge current rating. A basic circuit is given in Fig.14.

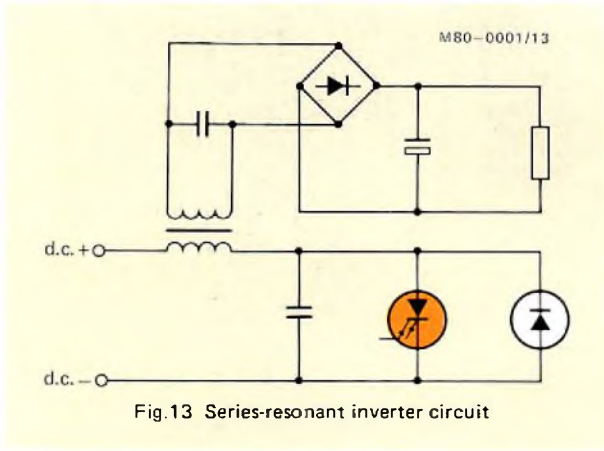


Fig.13 Series-resonant inverter circuit

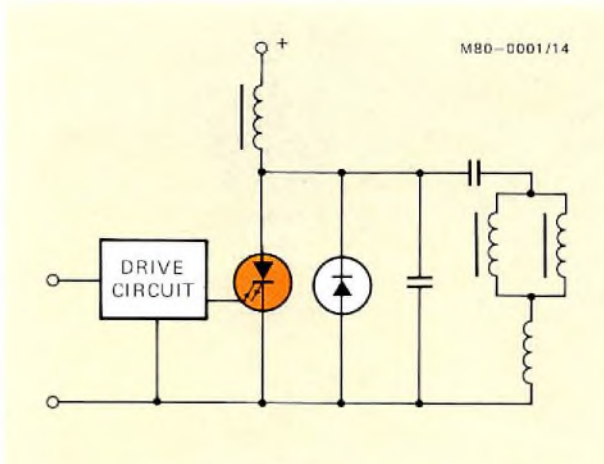
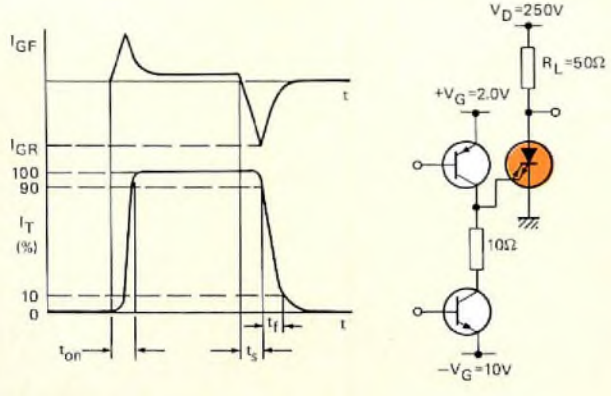


Fig.14 TV line deflection circuit

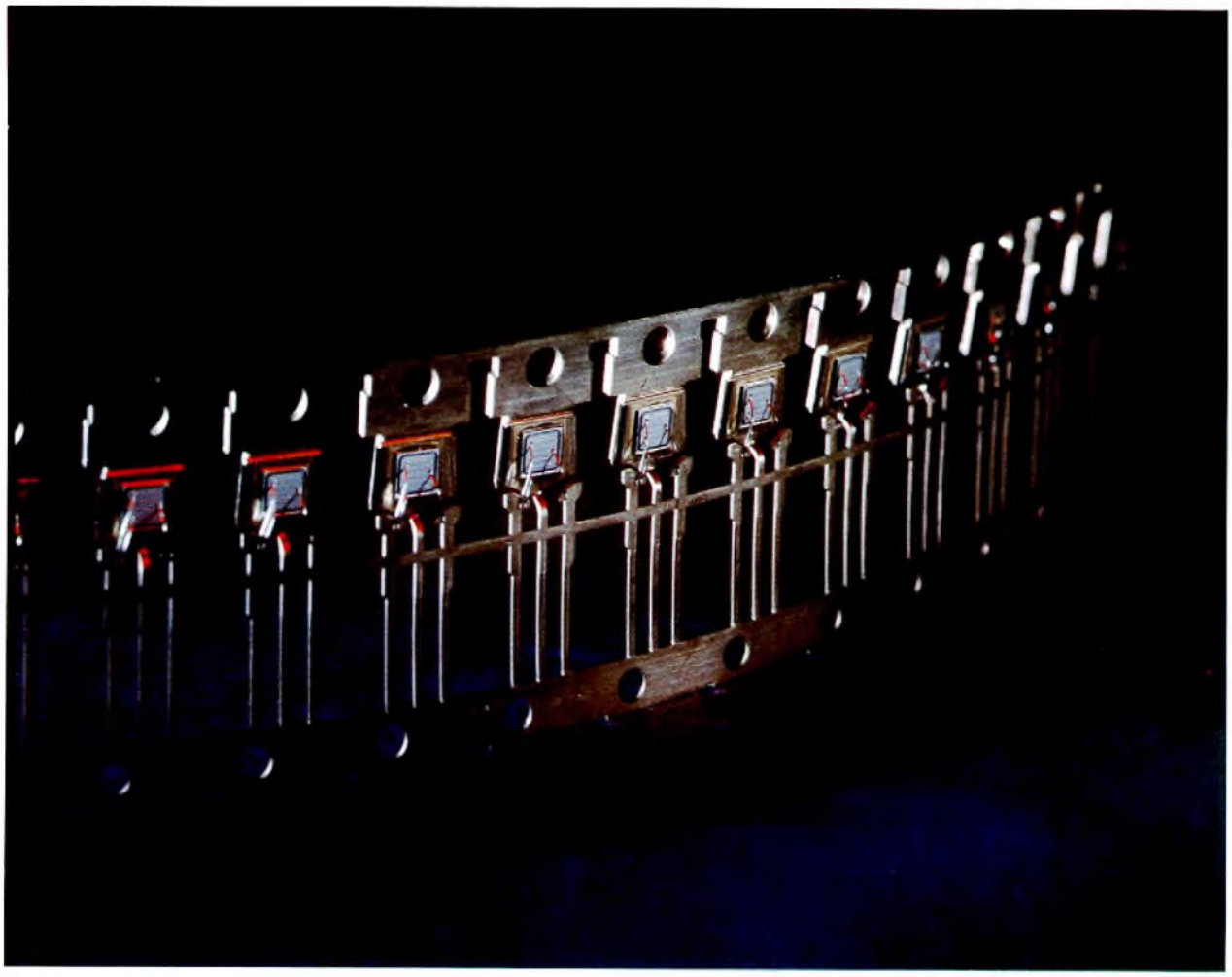
BRIEF DATA FOR BTW58 GTO

		BTW58-1500R	-1300R	-1000R	
Ratings					
Repetitive peak off-state voltage	$V_{DRM\ max}$	1500	1300	1000	V
Working peak forward current	$I_{TWM\ max}$		6.5		A
On-state current (d.c.)	$I_{T\ max}$		5		A
Controllable anode current	$I_{TCM\ max}$		25		A
I^2t for fusing; t = 10 ms	I^2t max		12.5		A^2s
Total power dissipation up to $T_{mb} = 25°C$	$P_{tot\ max}$		65		W
Operating junction temperature	$T_{j\ max}$		120		°C
Characteristics					
On-state voltage $I_T = 5$ A, $I_G = 0.12$ A, $T_j = 120°C$	V_T		<3.0		V
Rate of rise of off-state voltage that will not trigger any off-state device; exponential method $V_D = 2/3\ V_{D\ max}$, $-V_{GK} \geqslant 5$ V, $T_j = 120°C$	dV_D/dt		<10		kV/μs
Rate of rise of off-state voltage that will not trigger any device following conduction; linear method $I_T = 5$ A, $V_D = V_{D\ max}$, $-V_{GK} = 5$ V, $T_j = 120°C$	dV_D/dt		<1		kV/μs
Gate current that will trigger all devices $V_D = 12$ V, $T_j = 25°C$ BTW58-1500R,-1300R	I_{GT}		>120		mA
BTW58-1000R	I_{GT}		>300		mA
Turn-off when switched from $I_T = 5$ A to $V_D = 250$ V with $-V_G = 10$ V, $dI_G/dt = 5$ A/μs					
fall time: $T_j = 25°C$	t_f		<0.5		μs
$T_j = 120°C$	t_f		<1.0		μs
storage time $T_j = 25°C$	t_s		<0.5		μs
$T_j = 120°C$	t_s		<1.0		μs



Switching characteristics: waveform and test circuit

Thermal resistance					
From junction to mounting base	$R_{th\ j\text{-}mb}$		1.5		°C/W



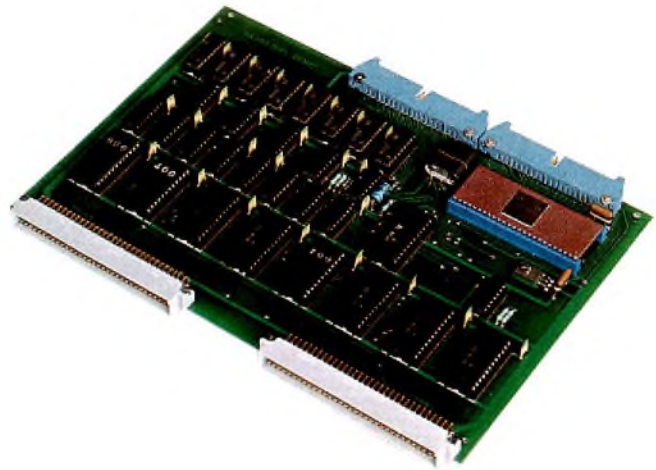
Although the GTO is not a new device, it is only recently with advances in ion implantation, neutron doping, fine-line photolithography, and process control, that its transfer from the laboratory to large-scale production has been made possible. Excellent yields are now being achieved and the manufacture of GTOs with characteristics suitable for a wide range of applications is now feasible. In many respects, the GTO out-performs both the conventional thyristor and the bipolar transistor. The BTW58 (shown before encapsulation, above) has a blocking voltage of up to 1500 V, a surge current rating of 50 A, dV/dt capabilities of 10 kV/μs static and 1 kV/μs dynamic, and very fast switching times of less than 0.5 μs

Development of digital filters using the 8X300 microprocessor

J. A. A. DEN OUDEN

Digital filters are succeeding their analogue counterparts wherever signal filtering is needed. Unlike analogue filters, they can be exhaustively analysed, can be of any required accuracy, can have extremely high Qs, and their parameters do not change with temperature. In a PCM codec, digital filters can simplify the precision analogue input and output filters. In radar, for performing Fast Fourier Transforms where multiple filtering is used, and in storage techniques for image enhancement in television systems digital filters are invaluable.

This third article on the 8X300 microprocessor and system support (Refs. 1, 2) describes a digital filter development system using the 8X300 Development and Monitoring System (DMS). The DMS facilitates fast and economical development of the filter program. After development, the fully-proven program held in the DMS RAM can be transferred to the 8X300 system PROM and the DMS can be disconnected.



The 8X300-DMS-2KMC microcomputer board — heart of the digital filter system

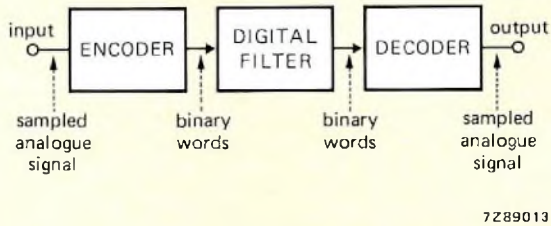


Fig.1 A digital filter processes signal samples as encoded words

A digital filter operates on the same principle as a sampled-data filter; it processes signal samples. The difference between the two is that the digital filter processes the signal samples as encoded (usually binary) words, see Fig.1. Since a digital filter mainly performs addition and multiplication of delayed signal samples by constant coefficients, its hardware includes binary adders and multipliers. The basic delay unit is a shift register which stores a binary word until it is needed for processing at the next sampling time.

The system described performs a double-byte multiplication, addition and shift in 4.25 μs.

8X300 DIGITAL FILTER SYSTEM

Figure 2 shows the block diagram of an 8X300 digital filter system. The heart of the system is an 8X300-DMS-2KMC microcomputer board. This is connected to the DMS which is used to develop the filter program.

The microprocessor also interfaces with a dedicated parallel multiplier which saves microprocessor time and requires far fewer instructions than would be required using the microprocessor's ALU. Multiplication of two 16-bit words takes just 7 clock cycles (1.75 μs). Filter coefficients and delayed signal samples are stored in a 64-word x 16-bit memory, in the multiplier subsystem.

Internally, signals are processed as 16-bit words, allowing a 12-bit ADC and DAC to be used. Analogue input and output signals are band-limited using simple low-pass filters. The cut-off frequency of the filters should be less than half the sampling frequency, to prevent aliasing. The sampling frequency is controlled by a timer which is polled by the 8X300.

8X300-DMS-2KMC board

As shown in Fig.3, the 8X300-DMS-2KMC board comprises:

- an 8X300 microprocessor,
- sockets for PROMs (2K words of program),
- 256 bytes working storage on the right bank,
- 8 I/O ports on the left bank,
- connections for I/O expansion,
- connections for the DMS.

During development, the filter program is stored in the DMS program storage (RAMs). The debugged program is then punched into paper tape in a reloadable or PROM programmer format. If the contents of the DMS RAMs are transferred to PROM, the DMS can be removed.

If a TWIN system is available, the 8X300 cross-assembler can be used and 8X300 object code can be loaded directly from diskette.

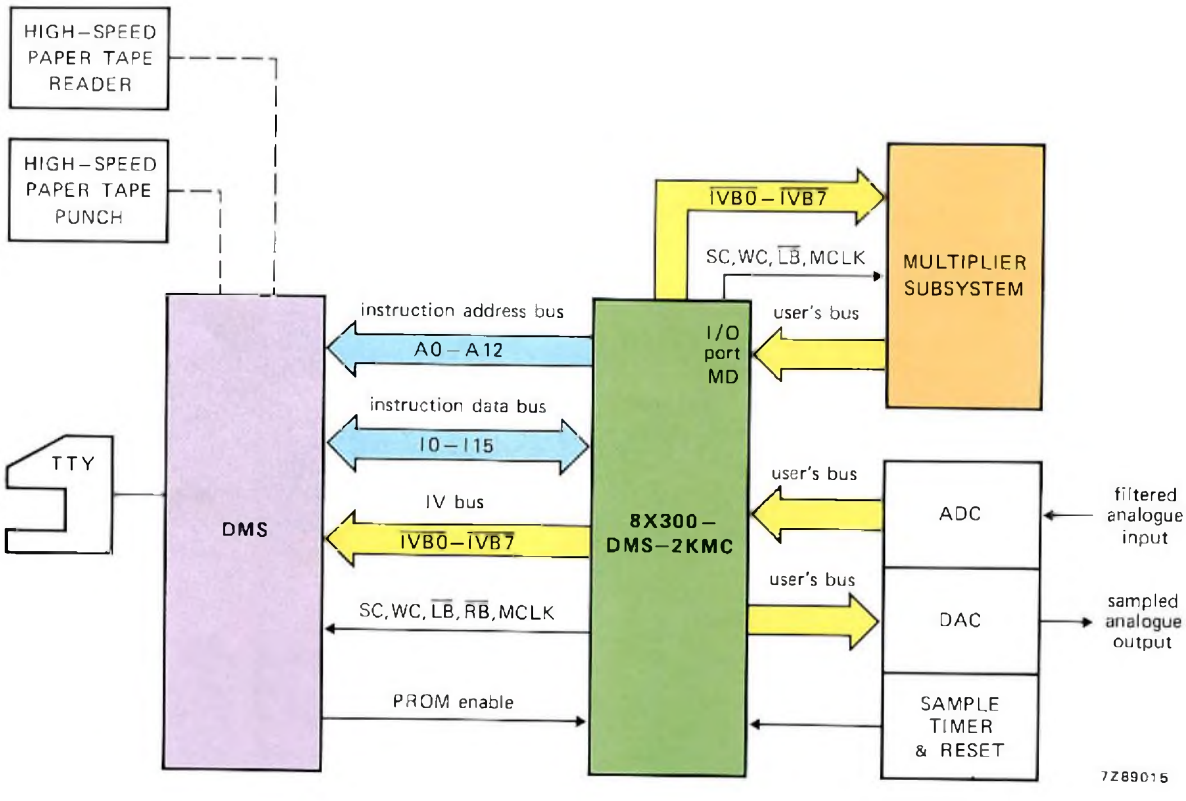


Fig.2 Block diagram of an 8X300 digital filter and connection to filter development tools

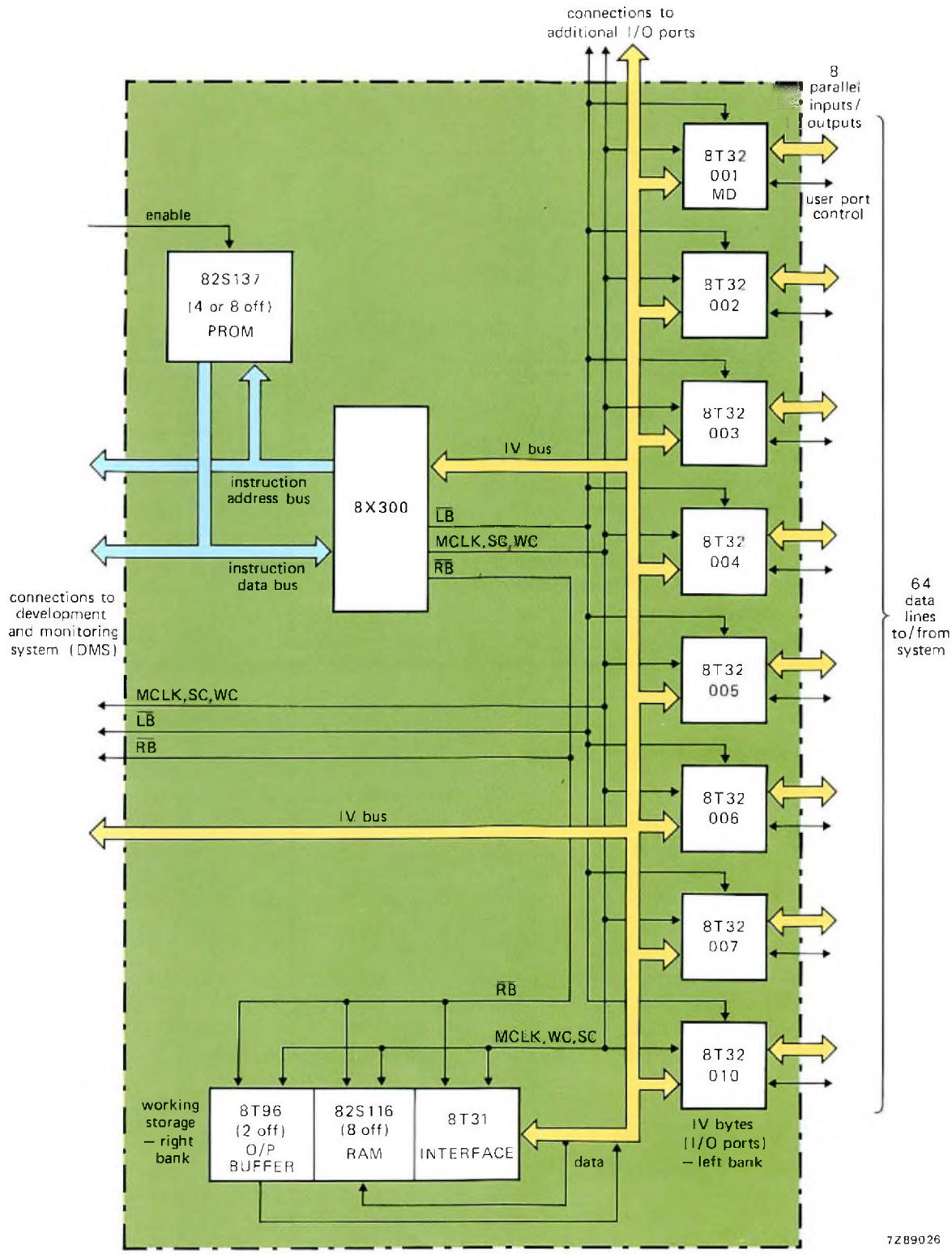


Fig.3 Block diagram of the 8X300-DMS-2KMC microcomputer board

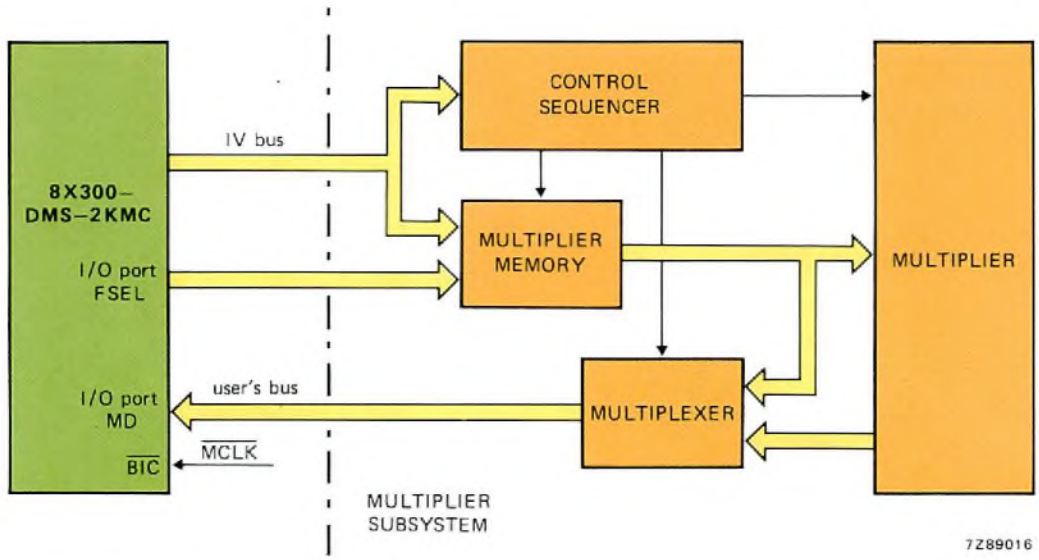


Fig.4 Block diagram of the multiplier subsystem and connection to the 8X300-DMS-2KMC. Figure 15 shows the detail

Multiplier subsystem

The 16-bit x 16-bit multiplier subsystem (Fig.4) comprises:

- control sequencer,
- multiplier memory, 64 words of 16 bits,
- multiplier,
- output multiplexer.

The multiplier memory stores filter variables and constants. The memory address includes control bits which indicate the type of action to be executed (read/write or multiply) and the format of the output. Part of the address comes from the filter bank select (FSEL) I/O port.

Control sequencer

The control sequencer is built around an FPLA. The sequencer generates control signals for:

- the multiplier,
- the multiplier memory,
- the output multiplexer.

The FPLA program table appears on p. 213. Four of the FPLA outputs (F4 – F7) are clocked with $\overline{MCLK}$ into D-type flip-flops. The outputs of the flip-flops (SQ0 – SQ3) indicate the sequencer status and are fed back to the FPLA.

There are three sequences: multiplier memory access (read/write) and two multiplication sequences. A sequence starts when the FPLA detects a LB (left bank) address with the MSB = 1 (i.e. an address greater than 200H), and the first state (A) is clocked into the status flip-flops. Subsequent states, and hence the sequence followed, depend upon bits 1 and 2 in the control address; bit 1 = IVB1 = $\overline{MEM}$, bit 2 = IVB2 = FMD.

Memory access is selected if IVB1 = 0, and the sequence will be (A)→(3)→(2)→(3)→(2) . . . see Fig.5.

Multiplication is selected if IVB1 = 1, and IVB2 (= FMD) indicates the sequence:

FMD = 0 denotes the 2-byte sequence:
(A)→(2)→(3)→(4)→(5)→(4)→(5) . . . ,

FMD = 1 denotes the 4-byte sequence:
(A)→(2)→(3)→(6)→(7)→(4)→(5)→(6)→(7)→(4)→(5) . . ,

see Fig.6.

In state (A) of the memory read access sequence and in state (2) of the multiplication sequences, the I/O port MD = L001 is selected to enable data routeing to the 8X300. Any select address (LB or RB) at a later stage will stop the sequence.

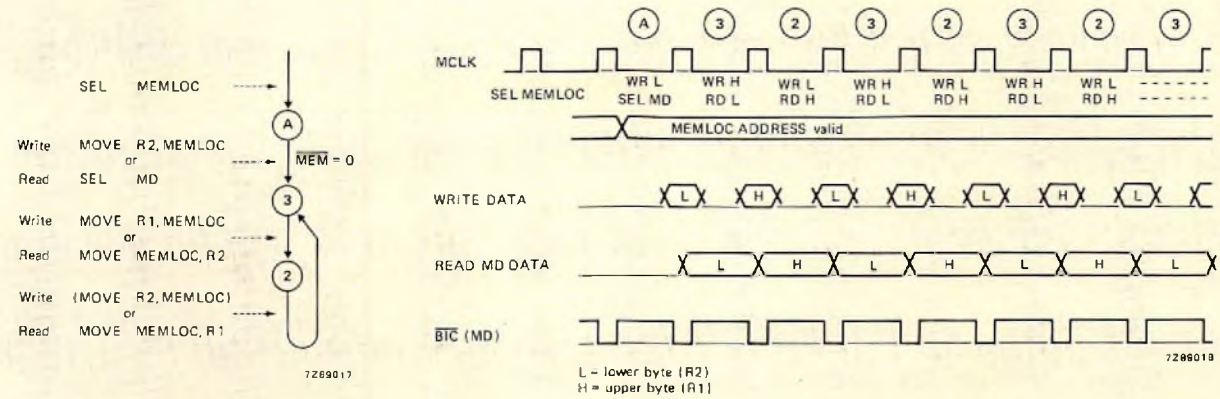


Fig.5 Multiplier memory access sequence and timing diagram

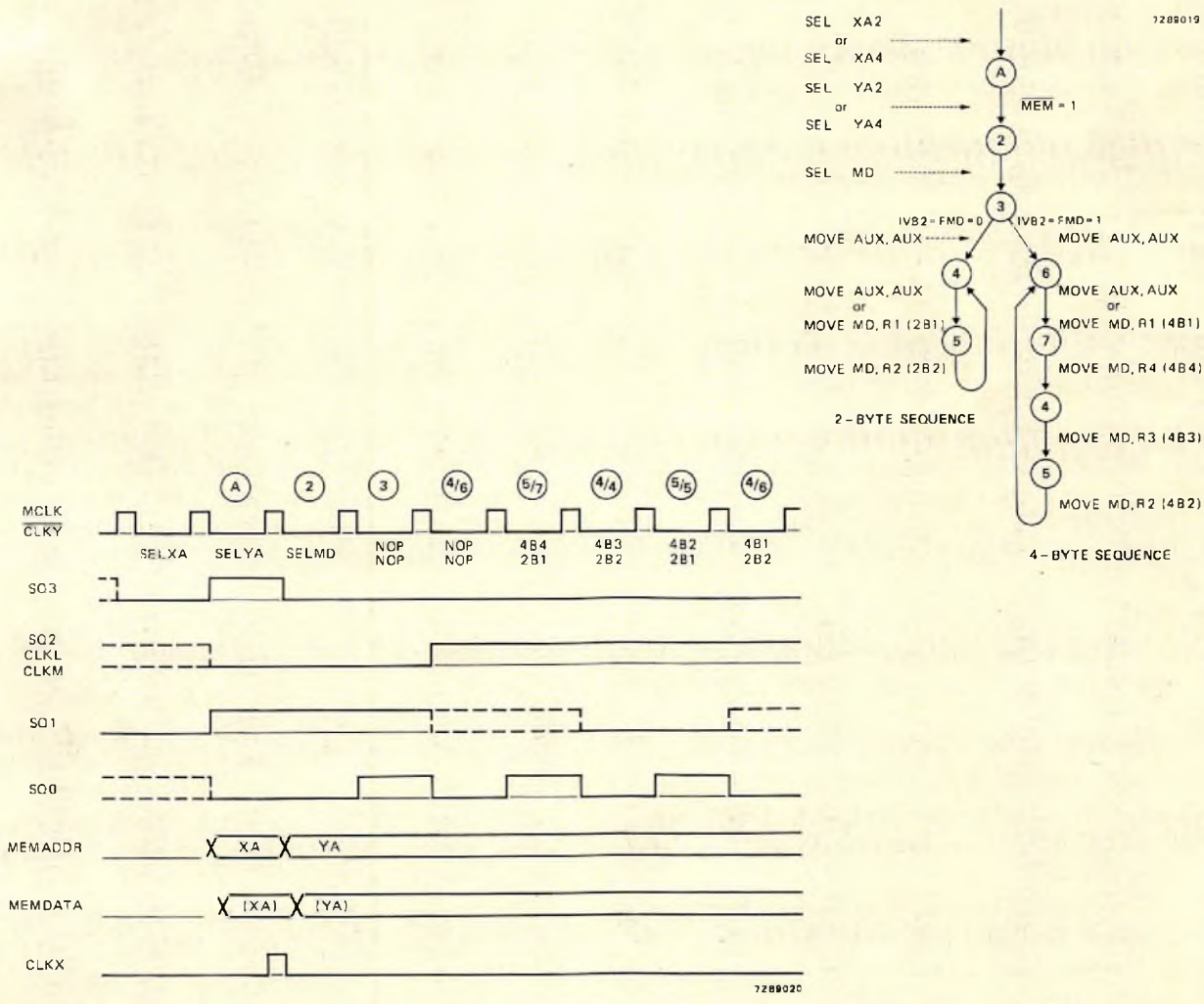


Fig.6 Multiplication sequences and timing diagram

Multiplier memory

The 64-word memory is arranged in 8 banks of 8 words each, by means of a memory address supplied in two parts. An I/O port on the 2KMC board provides 3 address bits (filter select) which select the filter bank; three other bits which select the word arrive via the latches of the control sequencer.

The filter select has to be set to the correct bank before a memory read/write instruction or data transfer from memory to the multiplier:

```
SEL     FSEL
XMIT    001H, FSEL      SELECT FILTER BANK 1
```

For multiplication, the operands must be in the same filter bank.

A sequence is started by sending a LB address (including control bits) with the MSB = 1; for memory access IVL = 10XXXAAA. A 16-bit word can then be *written* into the memory in two clock periods:

```
SEL     MEMLOC
MOVE    R2, MEMLOC      WRITE LOWER BYTE
MOVE    R1, MEMLOC      WRITE UPPER BYTE
```

Data is *read* from the memory via the multiplexer and an I/O port. The I/O port must be selected before reading commences:

```
SEL     MEMLOC
SEL     MD              MPY-MEM DATA PORT
MOVE    MD, R2          READ LOWER BYTE
MOVE    MD, R1          READ UPPER BYTE
```

After a select MEMLOC (and MD) instruction, the chosen memory location remains selected until a new LB address is sent to the control sequencer.

Multiplier

This is a 16-bit x 16-bit parallel two's complement multiplier with double precision output (TRW MPY-16AJ; Fig.7).

The two 16-bit words to be multiplied are clocked into the input registers X and Y with the clock inputs CLKX and CLKY respectively. The CLKX signal, generated by the FPLA, is derived from the MCLK; CLKY is derived from $\overline{\text{MCLK}}$.

The 32-bit product is available to be clocked into the output registers MSP and LSP within 200 ns from the time the Y-operand was loaded into the Y register. The MSP register stores the Most Significant Part of the product, the LSP the Least Significant Part. The output register clock lines CLKM and CLKL are connected to

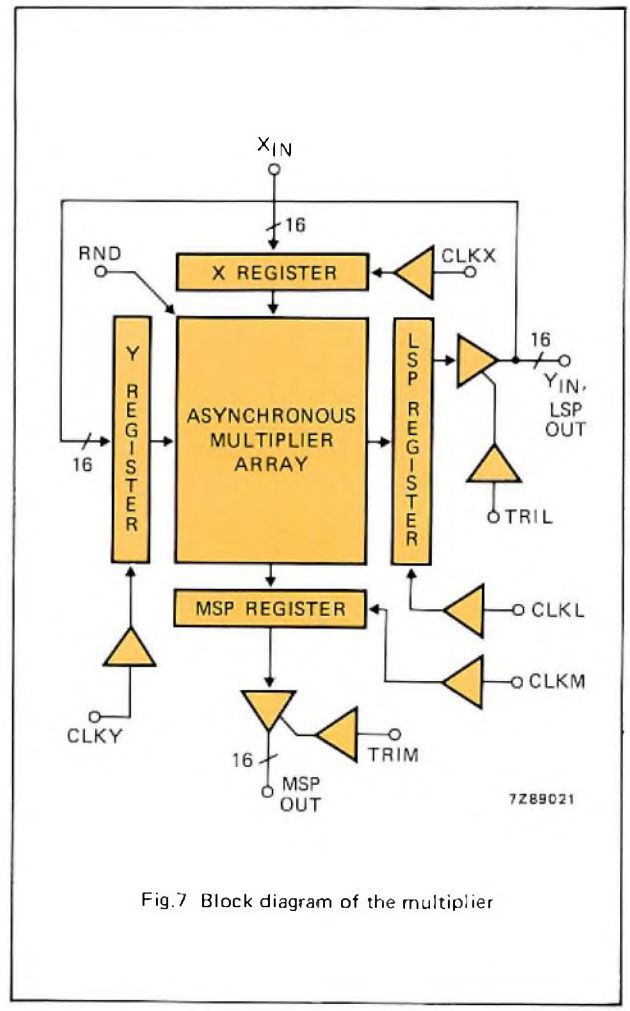


Fig.7 Block diagram of the multiplier

the output of the sequencer flip-flop SQ2; the product from the multiplier array being clocked into the output registers on the rising edge of SQ2, see Fig.6.

The contents of the output registers are then routed to the multiplexer using the TRIL and TRIM three-state controls. For TRIL and TRIM, the inverse of SQ2 is used; while true SQ2 disables the multiplier memory output.

Output multiplexer and data formats

The output multiplexer routes data from the multiplier memory or from the multiplier output registers to the 8X300 I/O port MD. The inputs of the multiplexer are connected in such a way that the products from the multiplier are transmitted in a format suitable for further calculations by the 8X300. There are two data formats: 2-byte and 4-byte, see Fig.8.

In the 4-byte format, the binary point is situated after the first bit of 4B1. Thus, the range -1.0000_{10} to $+0.9999_{10}$ can be represented; the first bit indicates the sign. In the output format of the multiplier, the sign bit of the LSP of the product is omitted and a zero is placed in the LSB.

In the 2-byte format, the binary point is situated after the third bit of 2B1. Thus, the range

-4.000_{10}
(100.0000000000000_2)

to

$+3.999_{10}$
(011.1111111111111_2)

can be represented. Note, multiplication of two 16-bit words produces a product with six bits before the point. To obtain the correct format, three of these bits must be removed; the multiplier removes one bit, and the multiplexer the other two.

Table 1 shows the multiplexer input and control table.

TABLE 1
Multiplexer input and control table

SELECT			DATA	MUX	TO I/O PORT MD							
S2	S1	S0	BYTE	INP	UD0	UD1	UD2	UD3	UD4	UD5	UD6	UD7
0	0	0	2B1	I0	PR02	PR03	PR04	PR05	PR06	PR07	PR08	PR09
0	0	1	2B2	I1	PR10	PR11	PR12	PR13	PR14	PR15	PR16	PR17
0	1	0	M1	I2	PRS	PR16	PR17	PR18	PR19	PR20	PR21	PR22
0	1	1	M2	I3	PR23	PR24	PR25	PR26	PR27	PR28	PR29	PR30
1	0	0	4B1	I4	PRS	PR01	PR02	PR03	PR04	PR05	PR06	PR07
1	0	1	4B2	I5	PR08	PR09	PR10	PR11	PR12	PR13	PR14	PR15
1	1	0	4B3	I6	PR16	PR17	PR18	PR19	PR20	PR21	PR22	PR23
1	1	1	4B4	I7	PR24	PR25	PR26	PR27	PR28	PR29	PR30	0

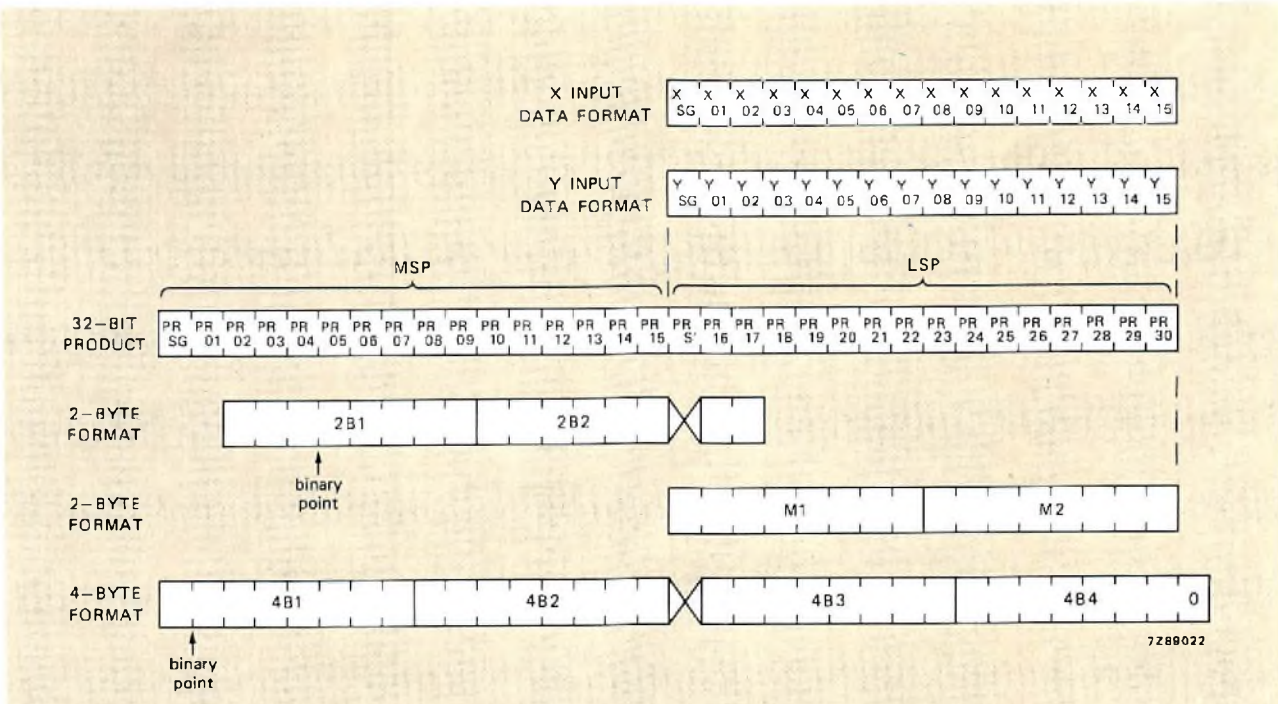


Fig.8 Output data formats of the multiplier subsystem. The 2-byte format M1 and M2, is for memory access (read); the other 2-byte format and the 4-byte format are for multiplier products. The input data formats are shown for reference

FILTER EXAMPLE

We shall now outline a second-order recursive digital filter developed using the 8X300. Figure 9 shows the block diagram of the system.

Analogue signals are band-limited by a simple low-pass filter, sampled at 8 kHz and then encoded by a 10-bit ADC. The digital signals are processed by the 8X300 and multiplier and reconverted to analogue by an 8-bit DAC. The unwanted sidebands of the reconstituted analogue signals are removed by another low-pass filter similar to the input filter. A programmable timer sets the sampling frequency.

Figure 10 shows the filter and Fig.11 the flow chart of the filter program. The filter centre frequency f_0, and the bandwidth b_w can be adjusted separately: f_0 with F, b_w with B.

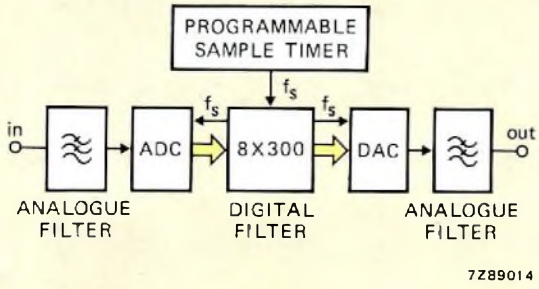


Fig.9 Block diagram of the 8X300 filter system

The filter program is available on request. Certain aspects of the program using the 2-byte format are now described.

Data range and clamping

The output Y(nT) must be clamped between 000.111$\mathcal{1}$ ($+0.999_{10}$) and 111.000$\emptyset$ (-0.999_{10}) to prevent overflow.

Clamping is done by testing the three MSBs of the output for sign and overflow. If the MSB = 1, the output is negative and the following two bits should also be 1s (111.XXXXX). If the MSB = 0, the output is positive and the following two bits should also be 0s (000.XXXXX). If overflow is detected, Y(nT) is set to its maximum positive or negative value.

Round off

In the 2-byte format the bits of the lower bytes (bits 18 to 30) of the 32-bit product are ignored. For 2s-complement numbers this decreases the magnitude of a positive product and increases the magnitude of a negative product. Therefore, a value is added to negative products such that ignoring the lower bits always decreases the magnitude of the original 32-bit product by the same small amount.

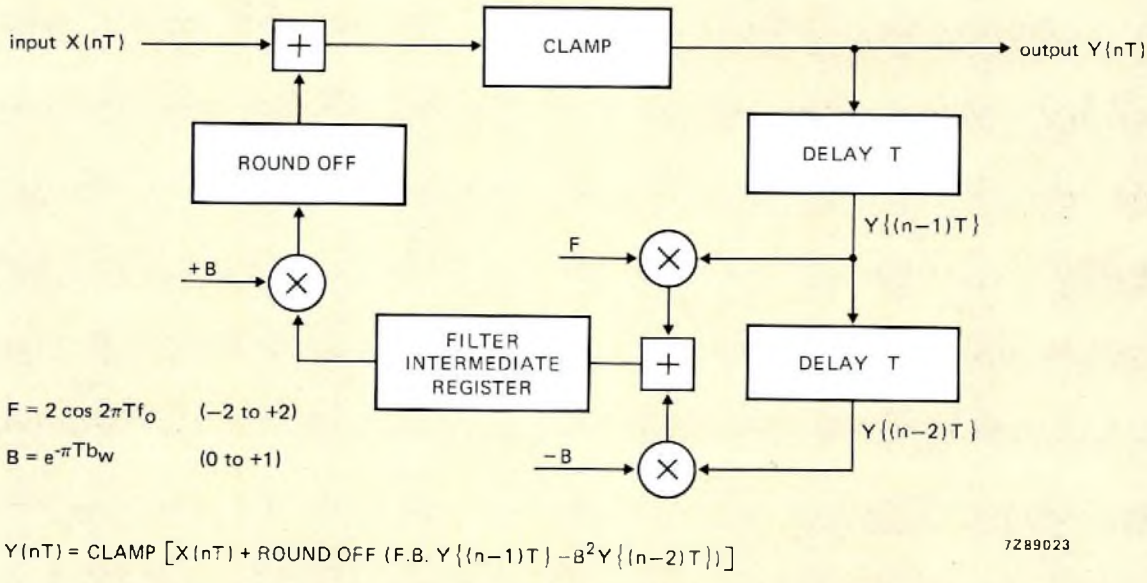


Fig.10 Functional diagram of the second-order recursive digital filter

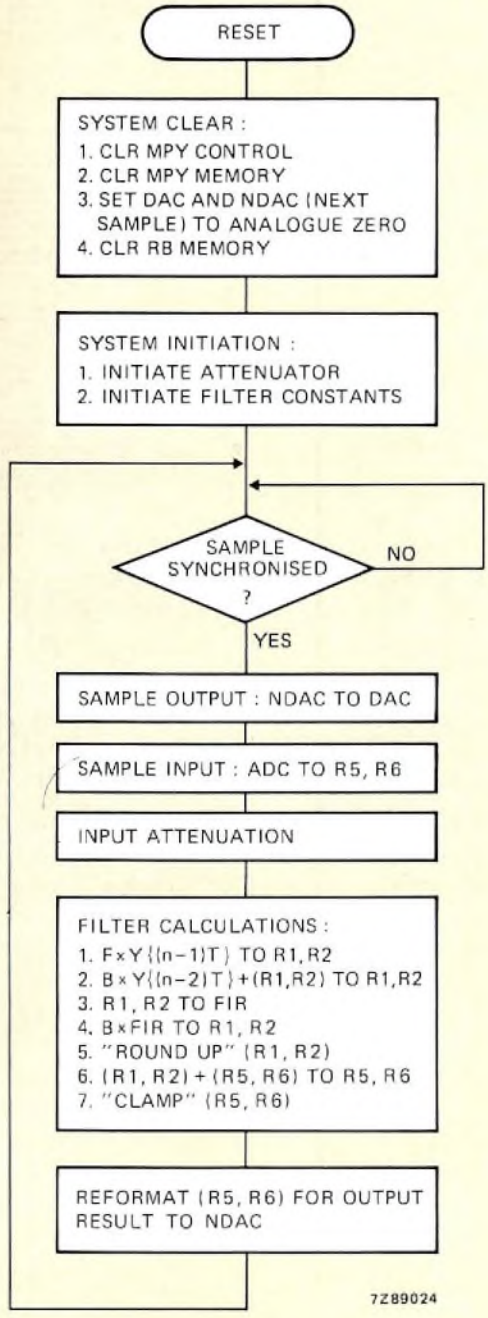


Fig.11 Flow chart of the filter program

Processing software overhead

At a sampling frequency of 8 kHz, there are 500 processor cycles between samples. The filter loop including sample synchronisation and I/O takes a maximum of 89 cycles, leaving 411 cycles in which overhead can be processed. Seven more filter stages could also be added, resulting in a 16th-order digital filter.

Auxiliary routines

Data in the multiplier memory can be examined and changed throughout the development of the filter program, using two copy auxiliary routines in 8X300 program. One routine transfers data from the multiplier memory to the RB working storage on the 2KMC board. This data can be displayed using a DR aaa aaa (display RB data) command and changed using an AR aaa (alter RB data) command. The other routine restores the RB data into the multiplier memory. These routines are started with a GT command. They should be considered as temporary program; the DMS is the main debugging tool.

Analogue to digital conversion

The output data of the ADC has to be reformatted for use in the filter calculations. Reformatting is partly done by the hardware itself, the MSB (B10) being propagated two bits. Four bits of the lower byte are insignificant and must be cleared (set to zero).

The output data of the ADC is always a positive (binary) number, whereas the input signal can vary from −5 V to +5 V. This output offset is removed by subtracting from the output data a value equal to half the input range.

Figure 12 shows the arrangement of the reformatted data.

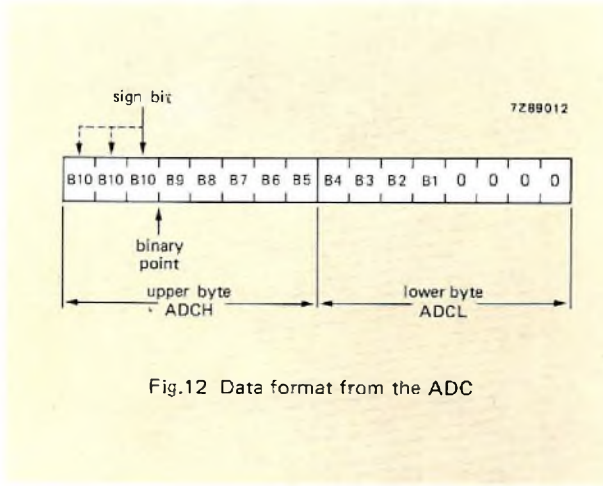


Fig.12 Data format from the ADC

Digital to analogue conversion

The DAC, like the ADC, operates with unsigned binary, whereas the analogue output range must be from −5 V to +5 V. Therefore, the data format used by the 8X300 has to be altered before the data is output to the DAC, by adding a value equal to half the analogue range. In addition, because the filter output data is clamped between 000.111*1* and 111.0000, the first three bits which indicate sign are always alike. Hence, two bits can be removed before data is output to the DAC.

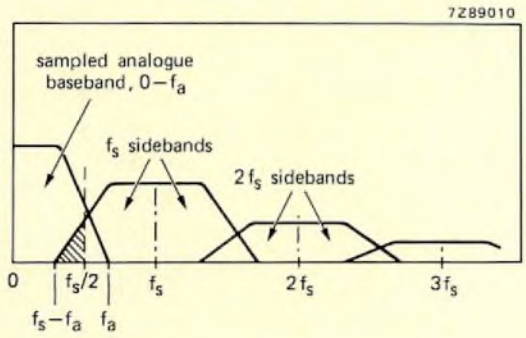
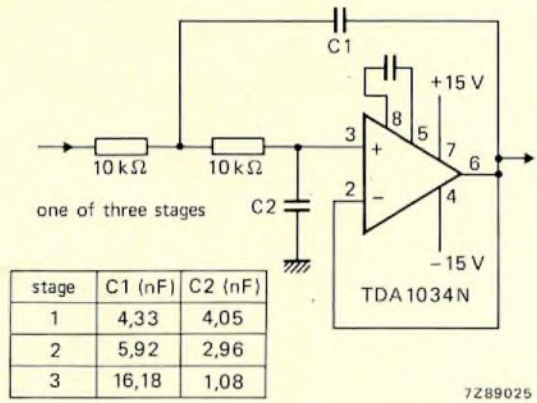
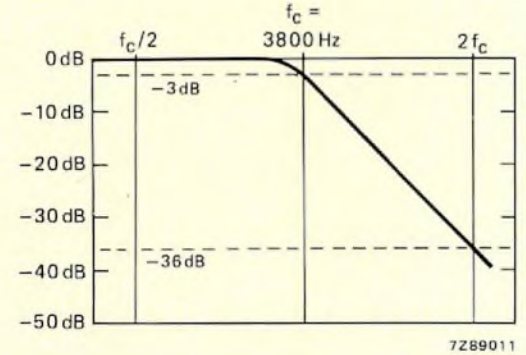


Fig.13 Aliasing due to the analogue signal spectrum containing frequencies higher than the sampling frequency f_s



stage	C1 (nF)	C2 (nF)
1	4,33	4,05
2	5,92	2,96
3	16,18	1,08

(a)



(b)

Fig.14 Six-pole Butterworth input and output filters:
(a) circuit diagram
(b) transmission curve

Analogue low-pass input and output filters

Sampling an analogue signal at a rate f_s can be considered as a kind of mixing or multiplying of the analogue spectrum with f_s. As well as the wanted spectrum in the digital signal, sidebands are produced at f_s and multiples thereof. If the analogue signal contains frequencies $f_a > f_s/2$, the lower sideband around f_s penetrates the spectrum of the sampled analogue signal that is to be processed, see Fig.13. This overlapping effect is called aliasing. Aliasing is prevented by suppressing the analogue input frequencies greater than $f_s/2$.

The output of the DAC is a sampled analogue signal too. Its spectrum contains frequencies up to f_a and sidebands around the multiples of f_s like the sampled input. These sidebands are removed with the same type of filter used at the input – a 6-pole Butterworth, see Fig.14. Better performance can be obtained by using 8 or even 10-pole filters.

Note that the total analogue input noise level with a 12-bit ADC should be less than the ADC quantization noise (72 dB), for a 16-bit ADC less than 84 dB.

Sample timer

This is a 16-bit programmable divide-by-N counter built from four 4-bit binary counters which run from a 4 MHz clock. The timer is programmed by setting the parallel load data on DIP switches.

Sampling pulses come from the output of one of the counters. The 8X300 polls for the falling edge of a sampling pulse. When one is detected the 8X300 proceeds to output data to the DAC, input data from the ADC and begin filter calculations. Polling for a falling edge gives more accurate timing because only one microprocessor cycle is necessary, as opposed to two cycles to detect a rising edge.

ADDITIONAL INFORMATION

Additional information on the 8X300 software and hardware can be found in:

- The 8X300 System Design Manual
- The 8X300 DMS user's manual
- The 8X300-DMS-2KMC instruction manual

product term	inputs										
	$\overline{MCLK}$ I15	$\overline{LB}$ I14	WC I13	SC I12	IVO I11	MEM I9	FMD I8	SQ3 I3	SQ2 I2	SQ1 I1	SQ0 I0
0	–	L	L	H	H	–	–	L	–	–	–
1	–	–	–	–	–	H	–	H	L	H	L
2	–	–	–	L	–	H	–	L	L	H	H
3	–	–	–	L	–	H	–	L	L	H	L
4	–	L	H	L	–	H	–	H	L	H	L
5	–	L	H	L	–	H	–	L	L	H	–
6	L	–	–	–	–	L	–	H	L	H	L
7	–	–	–	–	–	L	–	H	L	H	L
8	–	–	–	–	–	L	–	L	L	H	L
9	–	–	–	–	–	L	H	L	L	H	H
10	–	–	–	L	–	L	H	L	H	L	L
11	–	–	–	L	–	L	H	L	H	L	H
12	–	–	–	–	–	L	L	L	L	H	H
13	–	–	–	L	–	L	L	L	H	H	L
14	–	–	–	L	–	L	L	L	H	H	H
15	–	–	–	L	–	L	L	L	H	L	L
16	–	–	–	L	–	L	L	L	H	L	H

All inputs and outputs are active HIGH

A = product term present

· = product term *not* present

– = don't care

Inputs I4 – I7 and I10, and output F0 are not used.

outputs							sequencer status	
SD3 F7	SD2 F6	SD1 F5	SD0 F4	MWE F3	CLKX F2	S2 F1		
A	•	A	•	•	•	•	?→(A)	sequence start
•	•	A	A	•	•	•	(A)→(3)	memory access sequence
•	•	A	•	•	•	◦	(3)→(2)	
•	•	A	A	•	•	•	(2)→(3)	
•	•	•	•	A	•	•	(A)	WRITE pulse generation
•	•	•	•	A	•	•	(2) or (3)	
•	•	•	•	•	A	•	(A)	CLKX generation
•	•	A	•	•	•	•	(A)→(2)	multiply sequences
•	•	A	A	•	◦	•	(2)→(3)	
•	A	•	•	•	•	•	(3)→(4)	
•	A	•	A	•	•	•	(4)→(5)	
•	A	•	•	•	•	•	(5)→(4)	
•	A	A	•	•	•	A	(3)→(6)	
•	A	A	A	•	◦	A	(6)→(7)	
•	A	•	•	•	•	A	(7)→(4)	
•	A	•	A	•	•	A	(4)→(5)	
•	A	A	•	•	•	A	(5)→(6)	

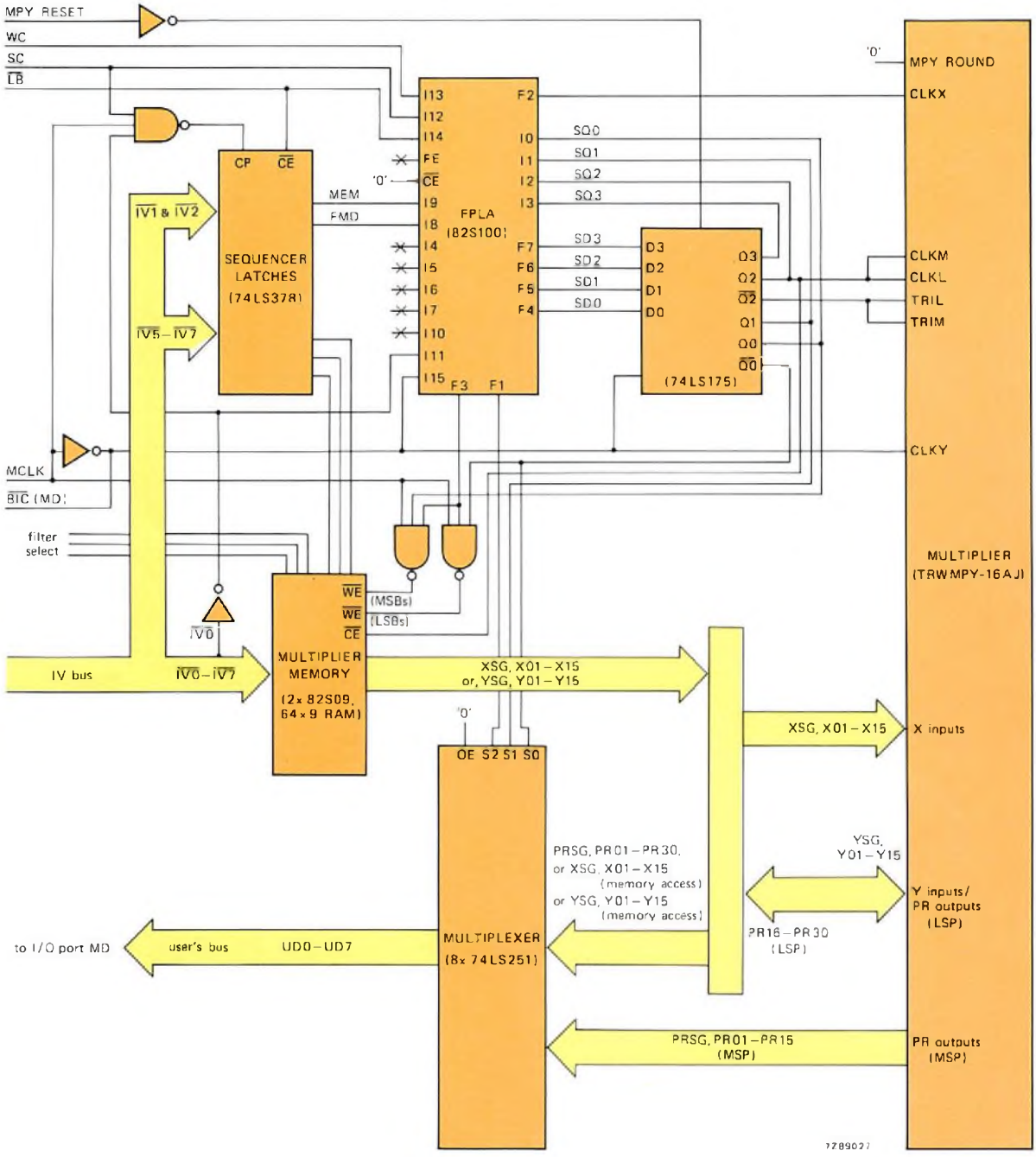


Fig.15 Multiplier subsystem. The X and Y inputs to the multiplier and the LSP outputs are interconnected; the connection between the Y inputs and the LSP outputs is an internal connection of the multiplier. The MSP outputs are routed directly to the multiplexer

REFERENCES

1. VAN VELDHUIZEN, E. D., 'The 8X300 – a high-speed control-oriented microprocessor', Electronic Components and Applications, Vol. 1, No. 2, Feb. 1979, pp. 91-101.

2. VAN VELDHUIZEN, E. D., 'The 8X300 development and monitoring system (DMS)', Electronic Components and Applications, Vol. 1, No. 4, August 1979, pp. 249-257.

Interference suppression for FM radios

D. J. VAN DER WAL

The high-quality reception capability of f.m. radios is often marred by the intrusion of h.f. interference radiated by vehicle ignition systems, neon signs and atmospherics. This type of interference is characterised by brief pulses with steep flanks and a repetition rate dependent on the nature of the source. Although such interference can be minimised by accurate i.f. alignment, precise tuning and a well-balanced demodulator, it cannot be entirely eliminated by these means. We therefore developed our well-known interference absorption integrated circuit TDA1001 for incorporation between the demodulator and audio output stages of an f.m. radio without the need for circuit modification. Since its introduction, the TDA1001 has been setting the industry standard for noise absorption in f.m. radios, and several other manufacturers have now produced ICs with identical circuitry.

In accordance with our policy of constantly reviewing the performance required from our components in the light of our customers' experience, we have now considerably improved the circuit and allocated it the new type number TDA1001A. The differences between the TDA1001A and its predecessor are:

- The relationship between the trigger sensitivity and the noise at the input of the TDA1001 is subject to a rather wide spread due to the tolerance of internal components. The influence of the spread of values of internal components has been eliminated in the TDA1001A.
- Interference pulses are unable to trigger the TDA1001 in the presence of high-level noise because the noise-operated gain control circuit continues to reduce the trigger sensitivity as the noise level increases. In the TDA1001A the trigger sensitivity remains constant if the noise level exceeds a predetermined threshold.
- The active filters in the TDA1001 have an open-loop gain of 60 dB and their stability is defined by a phase margin of about 45° and a gain margin of about 6 dB. In the TDA1001A, the open-loop gain of the active filters has been reduced to about 40 dB resulting in improved stability defined by a phase margin of about 70° and a gain margin of about 20 dB.

Although the TDA1001A can be incorporated in all types of f.m. radio, this article concentrates on its use in car radios where it can also eliminate the expense of suppressing interference radiated by the electrical circuits of the car and by tyre static. The main features of the TDA1001A are:

- Operates from a supply of 8 V to 15 V d.c.
- Can function in ambient temperature between −30 °C and +80 °C.
- After interference absorption, the peak-to-peak amplitude of the residual pulse on the audio signal waveform is less than 4 mV.
- The typical overall gain of 0.8 dB allows simple incorporation of the IC in existing radio circuits.
- Continues to absorb interference spikes during extremely high level noise at the input.
- Prevents degradation of the audio signal during the suppression of intensive (high repetition-rate) interference by limiting the maximum interference absorption rate.
- Includes a facility for regenerating the 19 kHz stereo pilot tone whilst interference is being absorbed.

- The very high trigger sensitivity of the circuit can be fully exploited in radios with low-noise demodulators (e.g. ratio detectors), or can be reduced by selection of the value of an external resistor for quadrature detectors.

OPERATING PRINCIPLES

The simple principles on which the TDA1001A operates are depicted in Fig.1. The signal from the demodulator in the radio is first split into two paths; an audio signal path that carries both the audio signal and the interference, and an interference path that carries only the interference. To do this, differentiation must first be made between the wanted audio signal and the spurious interference spikes. For high-quality stereo reception, the 3 dB bandwidth of the signal path must not be less than the bandwidth of the stereo sub-carrier (38 kHz) plus the width of the upper sideband (15 kHz). Any signal with a slope that exceeds that of a 53 kHz sinewave can therefore be considered to be interference and can be passed along the interference path. The interference path therefore incorporates a 53 kHz high-pass filter which separates the interference signals from the audio signals. The separated interference spikes drive a one-shot circuit to close a gate in the signal path for the duration of the interference pulse, thereby preventing it from reaching the output. An RC network connected to the gate circuit maintains the instantaneous level of the audio signal during the interference elimination process.

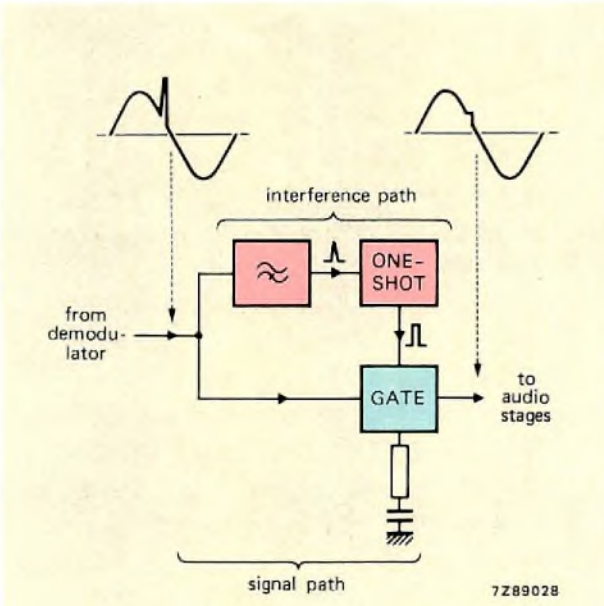


Fig.1 Basic principle of interference absorption

THE PRACTICAL INTERFERENCE ABSORPTION CIRCUIT

A practical circuit incorporating the TDA1001A is given in Fig.2.

The interference path

After buffering, the input signal at pin 1 is passed through an active 4th-order high-pass Chebyshev filter which provides attenuation of −3 dB at 91 kHz and −40 dB at 60 kHz. This filter only permits the passage of components of the input signal which have rise times shorter than the rise time of a 53 kHz sinewave (≈5 μs). The separated interference and noise signals are then passed to a gain-controlled pulse amplifier. The sensitivity of the pulse amplifier, and therefore the triggering sensitivity of the absorption circuit, is adjusted by an external resistor connected to pin 13. This allows a high sensitivity for low-noise ratio detectors or a lower sensitivity for quadrature detectors.

The pulse amplifier is followed by a pulse converter which ensures that the circuit responds to both positive-going and negative-going interference pulses. The output from the pulse converter triggers a one-shot circuit which produces a fixed duration positive-going pulse for driving the gate in the audio signal path. The duration of the one-shot pulse is determined by the RC network connected to pin 11. With the values shown in Fig.2, the pulse duration is 30 μs. Changing the value of the capacitor to 4.7 nF or 10 nF results in a pulse duration of 47 μs or 78 μs respectively.

A gain control circuit driven by negative-going pulses from the one-shot, together with the integrating network connected to pin 12 ensures that the absorption of interference pulses with a high repetition rate does not cause too long an interruption of the audio signal and thereby introduce audible distortion. This is achieved by limiting the maximum duty factor of the pulses from the one-shot circuit. The values of the resistors in the integrating circuit connected to pin 12 are given by:

$$R_2 = 700/\delta \text{ and } R_1 = 10R_2$$

where δ is the maximum duty factor for the one-shot pulses. Subjective tests have shown that audible distortion is avoided if the duty factor is limited to 0.5. The preferred resistor values are then $R_2 = 1.5\,k\Omega$ and $R_1 = 15\,k\Omega$.

In the presence of noise, the triggering sensitivity of the circuit is reduced due to the build up of a regulating voltage across the capacitor connected to pin 12. Unless precautions were taken, this would result in the circuit being unable to suppress interference spikes during periods of high-level noise. An internal circuit has therefore been incorporated to prevent further reduction of

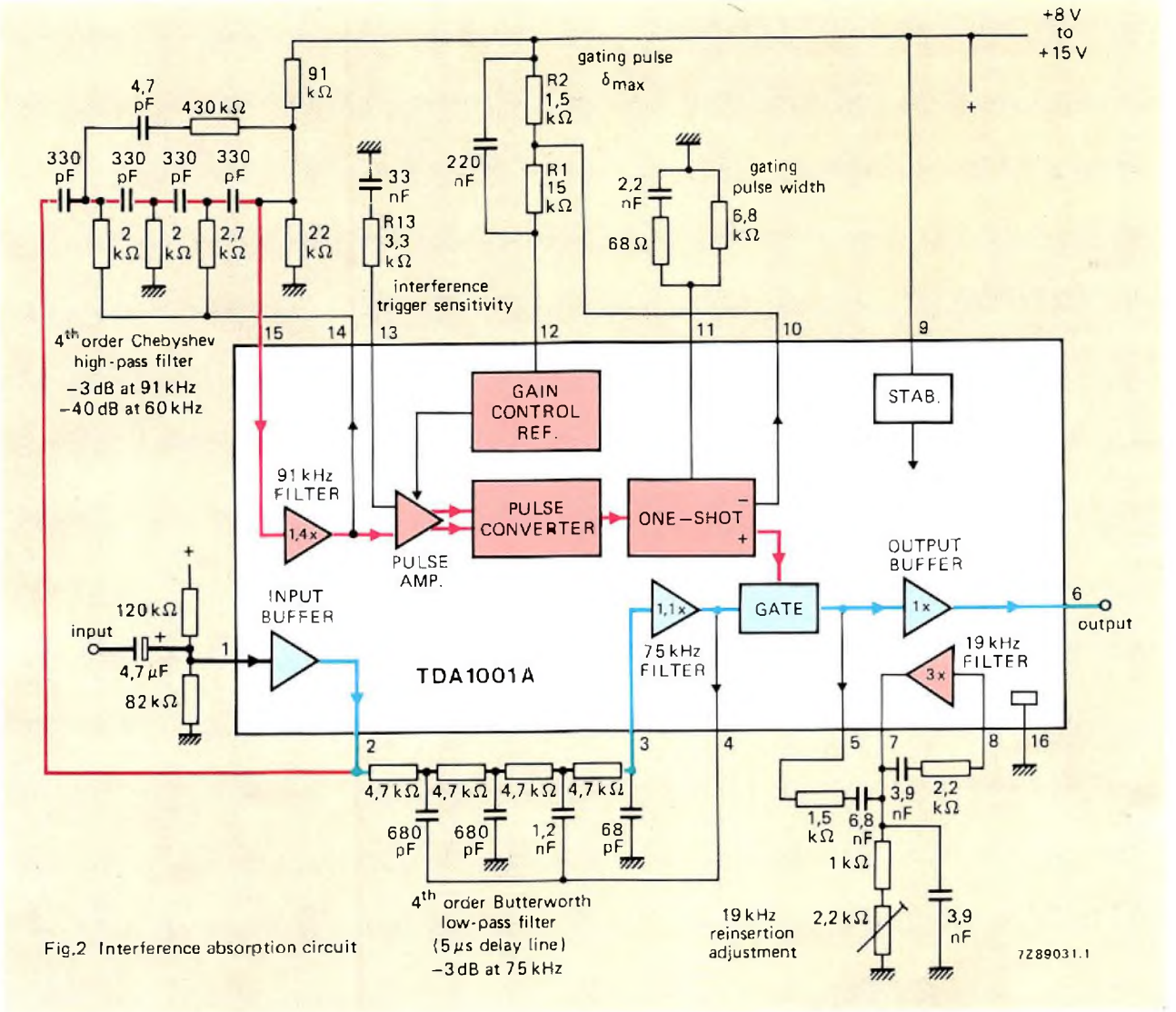


Fig.2 Interference absorption circuit

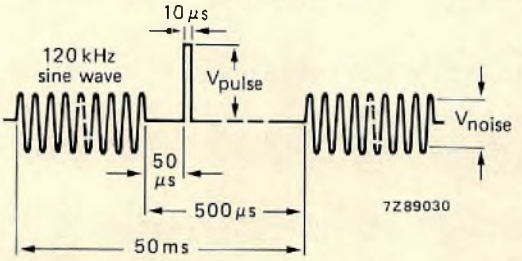
Performance of the circuit

Supply voltage range	$V_P = V_{9-16}$		8 to 15 V
Ambient temperature	T_{amb}	typ.	25 °C
Supply voltage	V_P	nom.	12 V
Total quiescent current	I_{tot}	typ.	15 mA
A.F. input signal handling (peak-to-peak value)			
$d_{tot} < 1\%$; f = 1 kHz	$V_{1-16(p-p)}$	<	1.5 V
Input impedance at f = 40 kHz (pin 1)	$\lvert Z_i \rvert$	>	30 kΩ
Audio voltage gain	$\frac{V_{6-16}}{V_{1-16}}$	typ.	0.8 dB
Total distortion			
f = 1 kHz; $V_{i(rms)} \leq 0.5$ V	d_{tot}	typ.	0.35%
Residual gate pulse in output signal (pin 6) (peak-to-peak value)	$V_{r6-16(p-p)}$	<	4 mV
Interference trigger sensitivity peak value			
R13 = 3.3 kΩ	V_{1-16}	typ.	50 mV
R13 = 2.5 kΩ	V_{1-16}	typ.	42 mV
Suppression pulse duration (pin 10)	t_s		20 to 35 µs

the trigger sensitivity when the noise at pin 1 reaches a predetermined level. This allows the interference absorption to continue until the noise level is high enough to itself cause triggering. The triggering sensitivity of the circuit is shown as a function of noise level, with the value of R_{13} as a parameter, in Fig. 3.

The audio signal path

The audio signal path starts with a low-pass active filter which provides a delay of about 5 μs to compensate delays in the interference path circuits. The output from the filter passes through a gate which is controlled by the one-shot circuit in the interference path. When the gate is closed during a pulse from the one-shot, the instantaneous level of the audio signal prior to the gate closing is maintained by the RC network connected to pin 5. The 19 kHz stereo pilot tone is regenerated during this period by the high-Q 19 kHz resonant circuit connected to pin 5. The oscillogram in Fig.4 shows the circuit absorbing two 10 μs interference spikes on the peak of a 1 kHz sinewave.



Testsignal applied to pin 1

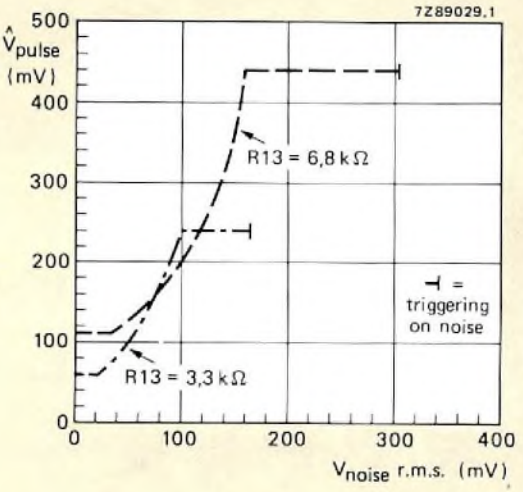
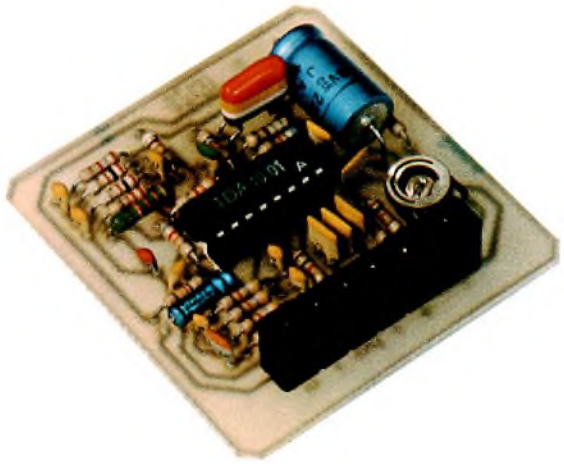


Fig.3 Typical triggering sensitivity as a function of noise level with the value of R_{13} as a parameter



Circuit evaluation board for the TDA1001A

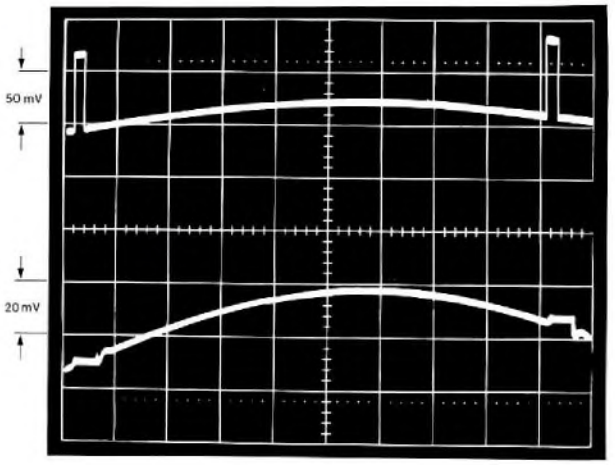


Fig.4 Two 75 mV interference pulses being removed from the crest of a 1 kHz sinewave

LSI circuit for AC motor speed control

B.G. STARR and J.C.F. van LOON

In the past, sinusoidal Pulse-Width Modulation (PWM) speed control systems for three-phase a.c. motors have been produced in a number of different forms. However, no single system has been completely satisfactory. High costs, circuit complexity, output variation with temperature, etc. have all prevented the widespread application of this potentially attractive method of a.c. motor speed control. This article describes a purpose-designed LSI circuit, type HEF4752V, which has been developed specifically for signal generation in such systems, and overcomes all the previous disadvantages. The IC is manufactured using locally-oxidised complementary MOS technology (LOCMOS) and is mounted in a standard 28-pin dual-in-line package.

This is the third in a series of articles all devoted to our a.c. motor speed control system. A general introduction to this subject is given in Refs.1 and 2, and a description of an inverter circuit developed specifically for the system is given in Ref.3.

PWM CONTROL OF A.C. MOTORS

A block diagram of our PWM speed control system is shown in Fig.1. In this system, the output waveforms from the three phases Red (R), Yellow (Y), and Blue (B) of a six-element inverter consist of sinusoidally modulated trains of carrier pulses, both edges of each pulse being modulated to give an average voltage difference between any two of the output phases which varies sinusoidally. This is illustrated in Fig.2 for a carrier wave having 15 pulses for each cycle of the inverter output.

Figure 2a shows the 15-fold carrier, Fig.2b the double-edge modulated R-phase, and Figs.2c and 2d show the double-edge modulated Y and B phases. The line-to-line voltage obtained by subtracting the Y-phase from the R-phase is shown in Fig.2e.

A detail of the double-edge modulation of a carrier wave is shown in Fig.3. Each edge of the carrier wave is modulated by a variable time δ, where δ is proportional to $\sin\alpha$, and α is the angular displacement of the unmodulated edge. The modulation of a 15-fold carrier requires a total of 30 δ values.

The modulation of the output waveforms is achieved by opening and closing the upper and lower switching elements (transistors or thyristors) in each phase of the inverter. Closing the upper element gives a high output voltage, and closing the lower element gives a low output voltage. The basic function of the PWM IC is to provide three complementary pairs of output drive waveforms which, when applied to the six-element inverter, open and close the switching elements in the appropriate sequence to produce a symmetrical three-phase output. The drive waveforms are supplied to the inverter via buffer amplifiers with isolation where necessary. The integrated circuit is completely digital, so that the repetition frequency of the PWM signal (switching frequency) is always an exact multiple of the inverter output frequency. This results in excellent phase and voltage balance and consequent low motor losses.

A 15-fold carrier multiple is used only for the highest motor speed range. To improve the pulse distribution at lower motor speeds the switching frequency is derived from higher multiples of the inverter output frequency. A hysteresis between the switching points is included to avoid jitter when operating in these regions. Typical

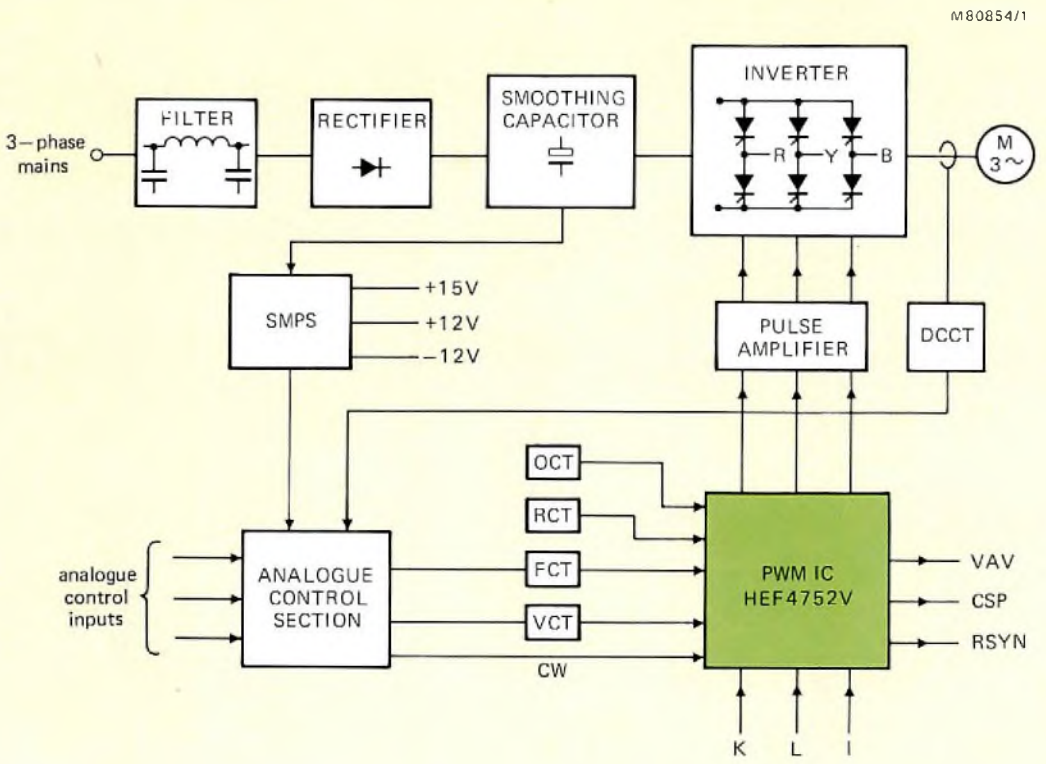


Fig.1 PWM motor control system using HEF4752V

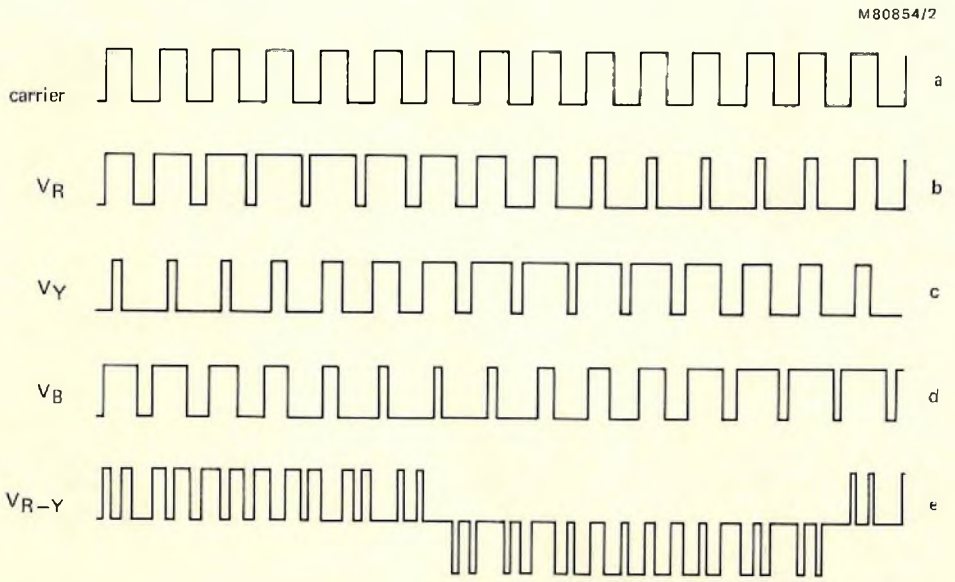


Fig.2 15-pulse sinusoidal PWM waveforms

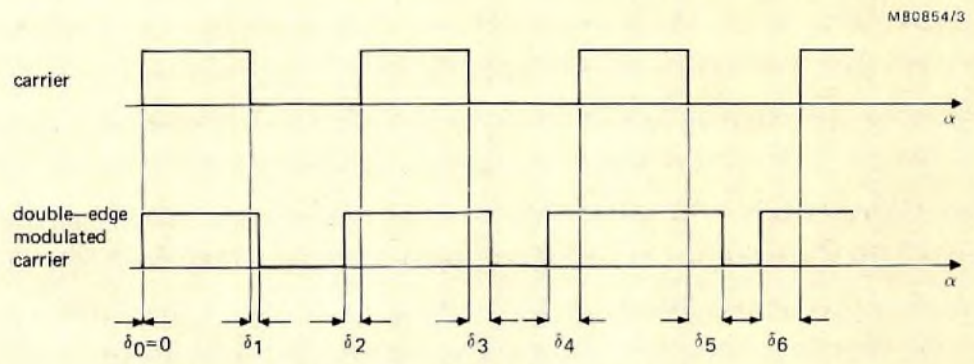


Fig.3 Detail of double-edge modulation

values of the carrier multiple and the output frequency are given in Table 1. It should be noted that this table applies only for a particular set of input conditions. The selection of input conditions is discussed later in this article.

For the values shown in Table 1, the IC has full control of the inverter switching frequency for output frequencies in the range 4.0 to 71.3 Hz. For output frequencies greater than 71.3 Hz, the switching frequency will increase beyond 1070 Hz until over-modulation is reached. Over-modulation implies a merging of adjacent pulses, with a corresponding reduction in switching frequency, until eventually a quasi-square output waveform is obtained. The point at which over-modulation occurs is determined by two of the clock inputs of the IC: VCT and FCT. This is covered in detail under the discussion of the VCT clock input. The practical upper limit on the output frequency is determined by the rating of the motor under control, the design of the inverter, and the performance of the IC. Detailed advice on the recommended maximum output frequency is also given under the discussion of the VCT clock input.

TABLE 1

Variation of carrier multiple with output frequency

Output frequency range Hz	Carrier multiple	Switching frequency Hz
0 to 4.0	168	0 to 675
4.0 to 6.4	168	675 to 1070
5.7 to 8.9	120	675 to 1070
8.1 to 12.8	84	675 to 1070
11.2 to 17.9	60	675 to 1070
16.3 to 25.5	42	675 to 1070
22.3 to 35.7	30	675 to 1070
32.5 to 51	21	675 to 1070
44.6 to 71.3	15	675 to 1070
71.3 +	15	See text

HEF4752V INTERNAL ORGANISATION

A block diagram indicating the internal organisation of the IC is shown in Fig.4. The circuit comprises three counters, one decoder, three output stages, and a test circuit. The test circuit is used primarily for testing the IC during manufacture, and is not discussed in this article. The operation of the IC is now considered in outline, and this is followed by a detailed discussion of the various input/output functions.

The three output stages (Fig.4) correspond to the R, Y, and B phases of the inverter. Each output stage has four outputs: two main outputs which control the upper and lower switching elements in each phase of the inverter, and two auxiliary outputs used to trigger commutation thyristors in 12-thyristor inverter systems. As explained above, the essential function of the IC is to provide the output waveforms which open and close the upper and lower inverter switching elements in the appropriate sequence. This is achieved by alternately switching between the upper and lower main outputs in each output stage. To ensure that the main outputs cannot be on simultaneously, an interlock delay period is used to separate the on condition of the upper and lower outputs. The interlock delay period is determined by inputs OCT and K, while the switch between the main outputs is controlled by an internally-generated control signal. A change in the level of this control signal causes the HIGH main drive output to switch off, and then after the interlock delay period, causes the LOW main drive output to switch on. With the interlock delay period fixed, variations in motor speed are produced by changes in the control signal, and a description of the production of this signal provides a basic understanding of the operation of the IC.

The control signal is derived from the carrier wave modulated by the appropriate δ values. Production of the control signal therefore requires the determination of the correct carrier frequency, and the corresponding δ modulations. The carrier frequency, which is equal to the product of the output frequency and the carrier multiple, is set by the FCT counter and the RCT counter. Dividing the clock input of the FCT counter by 3360 gives the output frequency, while the correct carrier multiple is determined by gating RCT clock pulses into the RCT counter, with a gating time equal to a fixed number of FCT clock pulses. For a given frequency of the RCT clock, the number of pulses counted in the gating time will fall as the frequency of the FCT clock increases, and this is used to derive a correspondingly lower value of the carrier multiple.

For each value of the carrier multiple, the decoder holds a corresponding set of δ values. Each δ value is

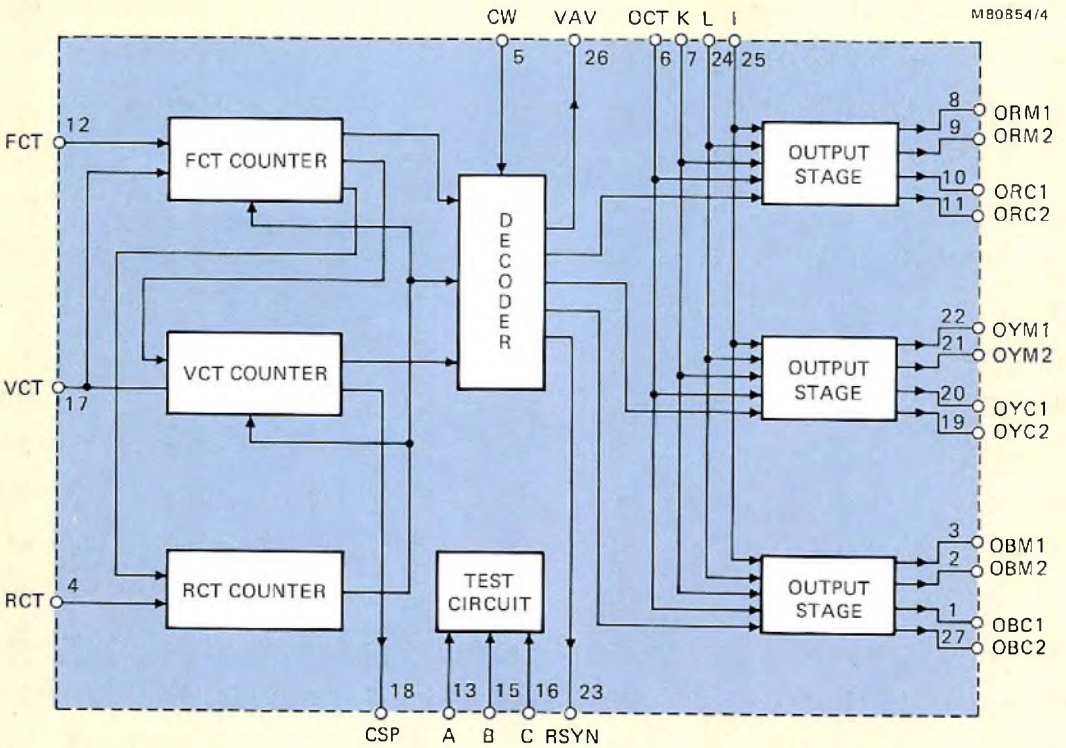


Fig.4 Block diagram of HEF4752V

stored as a number, and the width of the corresponding modulation is determined by the rate at which this number is counted. The counting frequency used is the VCT clock input, and the modulation depth is therefore inversely proportional to the frequency of the VCT clock input.

From the carrier frequency, and the δ modulations, the decoder finally assembles the control signal. A total of three control signals is produced by the decoder, one for each output stage, with a phase difference of 120° between each signal.

INPUT/OUTPUT FUNCTIONS OF THE HEF4752V

A pinning diagram of the HEF4752V IC is shown in Fig.5. The IC has 12 inverter drive outputs, three control outputs, four clock inputs, and seven data inputs.

Inverter drive signals

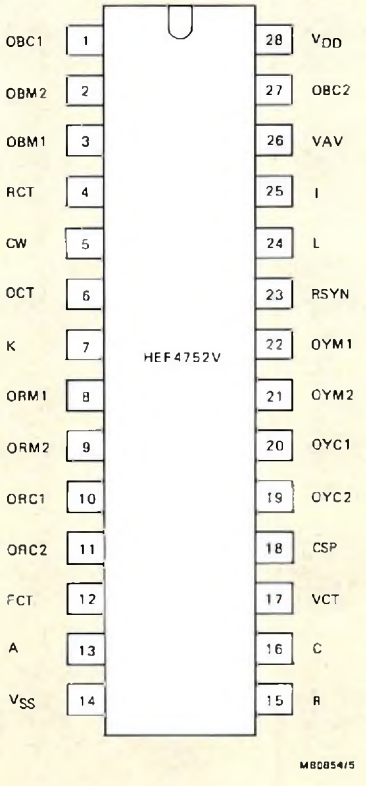
There are six main drive outputs which are arranged in complementary pairs. The pins are coded as follows.

First letter	O (output)
Second letter	R, Y, or B (phase indication)
Third letter	M (main)
Number	1 for output of upper switching element, or 2 for lower switching element

For example, ORM2 is the main drive waveform for the Red phase lower switching element.

Associated with each main output is the auxiliary output used to trigger the commutation thyristor in 12-thyristor inverter systems. These outputs are identified by a C as the third letter of the pin code, so that ORC2 is the commutation trigger pulse output associated with ORM2.

The inverter drive signals can be obtained in two



PINNING

Inverter drive signals		
8	ORM1	R-phase main
9	ORM2	R-phase main
10	ORC1	R-phase commutation
11	ORC2	R-phase commutation
22	OYM1	Y-phase main
21	OYM2	Y-phase main
20	OYC1	Y-phase commutation
19	OYC2	Y-phase commutation
3	OBM1	B-phase main
2	OBM2	B-phase main
1	OBC1	B-phase commutation
27	OBC2	B-phase commutation
Data inputs		
24	L	data
25	I	data
7	K	data
5	CW	data
13	A	data
15	B	data
16	C	data
Clock inputs		
12	FCT	frequency clock
17	VCT	voltage clock
4	RCT	reference clock
6	OCT	output delay clock
Control outputs		
23	RSYN	R-phase synchronisation
26	VAV	average voltage
18	CSP	current sampling pulses

Fig.5 Pinning diagram

forms, one mode for driving transistor inverters, the other for thyristor inverters. The form produced by the IC is determined by the logic level applied to the data input I.

Data inputs

Data inputs I, K, and L

As explained above, input I determines whether the inverter drive signals are in the thyristor or transistor mode. Input I LOW corresponds to the transistor mode; input I HIGH corresponds to the thyristor mode. In the transistor mode the main upper and lower switching elements in the inverter are switched HIGH alternately, with an interlock delay period (both switches LOW) at each changeover. During the delay period the commutation output associated with the off-going main output is set HIGH. The data input K, in association with the clock input OCT, is used to adjust the length of the interlock delay period. The details of this adjustment are described under the discussion of clock input OCT.

Input L provides a stop/start facility. In the transistor mode, with L LOW, all main and commutation signals are inhibited, and with L HIGH, the normal modulated block pulses continue. The action of L inhibits the actual output circuits only, so that while L is LOW the internal circuits generating the output signals continue to operate. Typical output waveforms for the transistor mode are shown in Fig.6. Figures 6a to 6d show the normal inverter drive outputs, and Fig.6e shows the internally-generated control signal which effects the transition between the upper and lower main drive outputs. Figures 6g to 6j illustrate the influence of changes in the level of input L (Fig.6f) on the inverter drive outputs.

With input I HIGH, thyristor mode, the main outputs become pulse trains with a mark-space ratio of 1:3, and the commutation outputs become a single pulse lasting for the first quarter of the interlock delay period. This is used to facilitiate the use of trigger transformers for isolation purposes. The interlock delay period is set in the same way as that used in the transistor mode, but in this case the logic level at input K and the frequency of OCT also control the frequency of the main output pulse trains, which in turn will affect the choice of trigger transformer. The delay period is selected to allow time for the commutation circuit to operate and reset in the 12-thyristor circuit, or to set the minimum pulse width for the six-thyristor self-commutated circuit. In this mode, with L LOW, the three lower switching elements in the inverter are triggered continuously, the upper elements being inhibited. Typical output waveforms for the thyristor mode are shown in Fig.7.

Data input CW

The phase sequence input CW is used to control the direction of rotation of the motor by altering the phase sequence. This is illustrated in Table 2. The phase sequences shown in Table 2 represent the order in which the phases pass through zero voltage in a positive direction.

TABLE 2

Phase sequence input CW

Input CW	Phase sequence
LOW	R, B, Y
HIGH	R, Y, B

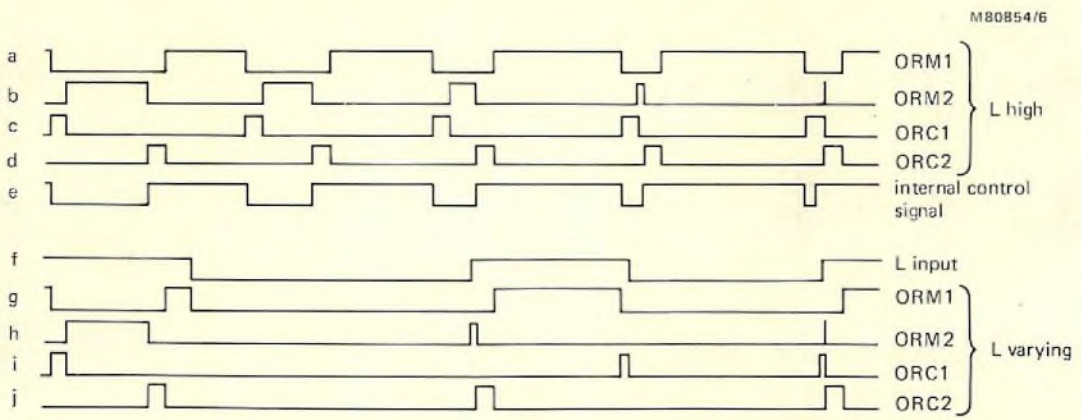


Fig.6 Typical output waveforms for transistor mode

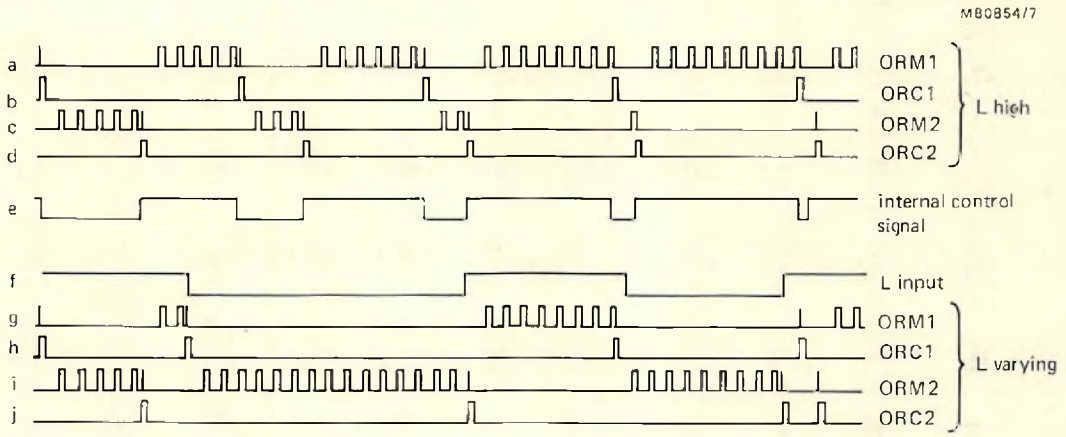


Fig.7 Typical output waveforms for thyristor mode

Data inputs A, B, and C

The three inputs A, B, and C are provided for use during production testing. They are not used during normal operation, when they must be connected to V_{ss} (0 V). Input A HIGH initiallises all the IC circuits, and can be used for reset. The use of input A is considered in detail below under the discussion of switch-on conditions.

Clock inputs

There are four clock inputs which are used to control the output waveforms. The following sections give a guide to selecting the frequency, or range of frequencies, for each clock.

Frequency control clock FCT

The clock input FCT controls the inverter output frequency f_{out}, and therefore the motor speed. The clock frequency f_{FCT} is related to f_{out} by the following equation:

$$f_{FCT} = 3360 \times f_{out}.$$

It is permissible to stop the FCT clock during system operation, the effect being to switch the outputs to either all M1 or all M2 outputs, and this occurs irrespective of the state of input I.

Voltage control clock VCT

An induction motor is governed by the general expression:

$$V = N\frac{d\Phi}{dt},$$

so that to maintain constant motor flux, the voltage-time product Vt must be kept constant. The IC automatically satisfies this requirement by making the output voltage directly proportional to the output frequency. The level of the average inverter output voltage, at a given output frequency, is controlled by the VCT clock input, changes in output voltage being achieved by varying the modulation depth of the carrier. Increasing f_{VCT} reduces the modulation depth, and hence the output voltage, while decreasing f_{VCT} has the opposite effect.

The maximum undistorted sinusoidal output voltage, which is obtainable in a given system, is determined by the voltage of the d.c. link, V_{link}; the maximum r.m.s. value of the fundamental component is given by $0.624 \times V_{link}$. This voltage occurs at 100% modulation of the carrier; that is, when some adjacent pulses are just about to merge. The output frequency at which this condition can apply in a given system is determined by the Vt product of the motor. The frequency at 100% modulation, $f_{out(m)}$, can be determined by relating the maximum r.m.s. inverter output voltage to the motor ratings as follows:

$$f_{out(m)} = f_N \times \frac{0.624 V_{link}}{V_N},$$

where f_N is the motor rated frequency and V_N the motor rated r.m.s. voltage.

Once $f_{out(m)}$ has been established, a value of f_{VCT} can be determined which will set the Vt product correctly throughout the frequency range of the motor to be controlled. This nominal value of f_{VCT} is denoted by $f_{VCT(nom)}$, and is related to $f_{out(m)}$ by:

$$f_{VCT(nom)} = 6720 \times f_{out(m)}.$$

With f_{VCT} fixed at $f_{VCT(nom)}$, the output voltage will be a linear function of the output frequency up to $f_{out(m)}$. Any required variation in this linear relation-

ship is obtained by changing f_{VCT}. For example, to double the output voltage at low frequencies, as a possible compensation for 'IR' losses, f_{VCT} is made equal to 0.5 $f_{VCT(nom)}$.

The frequency ratio f_{FCT}/f_{VCT} is important in system design. At 100% modulation it will have a value given by:

$$\frac{f_{FCT}}{f_{VCT(nom)}} = \frac{3360 \times f_{out(m)}}{6720 \times f_{out(m)}},$$

$$= 0.5.$$

Below 0.5 the modulation is sinusoidal, while above 0.5 the phase waveform approaches a squarewave, giving a quasi-squarewave line-to-line voltage. At approximately 2.5, the full squarewave is obtained. Above 3.0, the waveform becomes unstable as the internal synchronising circuits cannot function correctly, and 3.0 is therefore the recommended limit.

Reference clock RCT

RCT is a fixed clock which is used to set the maximum inverter switching frequency $f_{s(max)}$. The clock frequency, f_{RCT}, is related to $f_{s(max)}$ by the following equation:

$$f_{RCT} = 280 \times f_{s(max)}.$$

The absolute minimum value of the inverter switching frequency, $f_{s(min)}$, is set by the IC at 0.6 $f_{s(max)}$. These figures apply provided f_{FCT} is within the range 0.043 f_{RCT} to 0.8 f_{RCT}, and f_{FCT}/f_{VCT} is less than 0.5.

Figures 8 and 9 show the variation of inverter switching frequency plotted against output frequency with f_{RCT} = 280 kHz, and $f_{s(max)}$ = 1 kHz. To obtain the equivalent figures for different values of $f_{s(max)}$, both scales and f_{RCT} should be multiplied by the required value of $f_{s(max)}$ in kHz. For example, with $f_{s(max)}$ = 2 kHz, $f_{RCT} = 2 \times 280 = 560$ kHz, and referring to Fig.9, the value of f_s for f_{out} = 50 Hz (2 X 25) will be 1.5 kHz (2 X 0.75) at a pulse rate of 30 pulses per output cycle. Referring to Figs.8 and 9, it can be seen that the range of f_{out} that will keep f_s in the band 2 to 1.2 kHz will be 7.1 Hz (2 X 3.55) to 133 Hz (2 X 66.5), provided the ratio f_{FCT}/f_{VCT} is less than 0.5.

Output delay clock OCT

The OCT clock input, operating in conjunction with the data input K, is used to set the interlock delay period which is required at the changeover between the complementary outputs of each phase. For a thyristor inverter, where the output thyristors are triggered by a train of pulses (mark-space ratio 1:3), OCT and K have the additional function of determining the frequency of the pulse train.

The operation of OCT and K is shown in Table 3. Whenever possible input K should be HIGH as this keeps the jitter caused by lack of synchronisation between FCT and OCT to a minimum. In many cases a design economy can be obtained by using the same clock for both RCT and OCT.

Control outputs

Oscilloscope synchronisation RSYN

This is a pulse output of frequency f_{out} and pulse width identical to the VCT clock pulse. It is timed to occur just before the positive-going zero transition of the R-phase voltage. It therefore provides a stable reference for triggering an oscilloscope.

Output voltage simulation VAV

VAV is a digital waveform which simulates the average value of the expected line-to-line voltage of the inverter output; however, it excludes the effect of the interlock

TABLE 3

Operation of clock input OCT* and data input K

K	Interlock delay period ms	Trigger pulse frequency kHz	Trigger pulse width ms
LOW	$8/f_{OCT}$	$f_{OCT}/8$	$2/f_{OCT}$
HIGH	$16/f_{OCT}$	$f_{OCT}/16$	$4/f_{OCT}$

*f_{OCT} in kHz

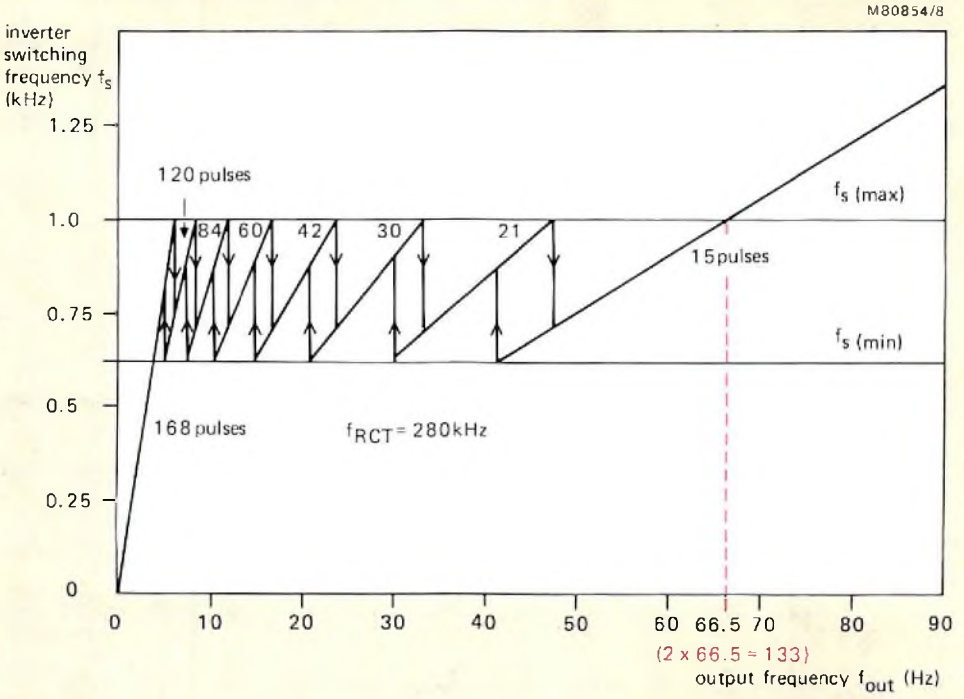


Fig.8 Inverter switching frequency against output frequency (full range)

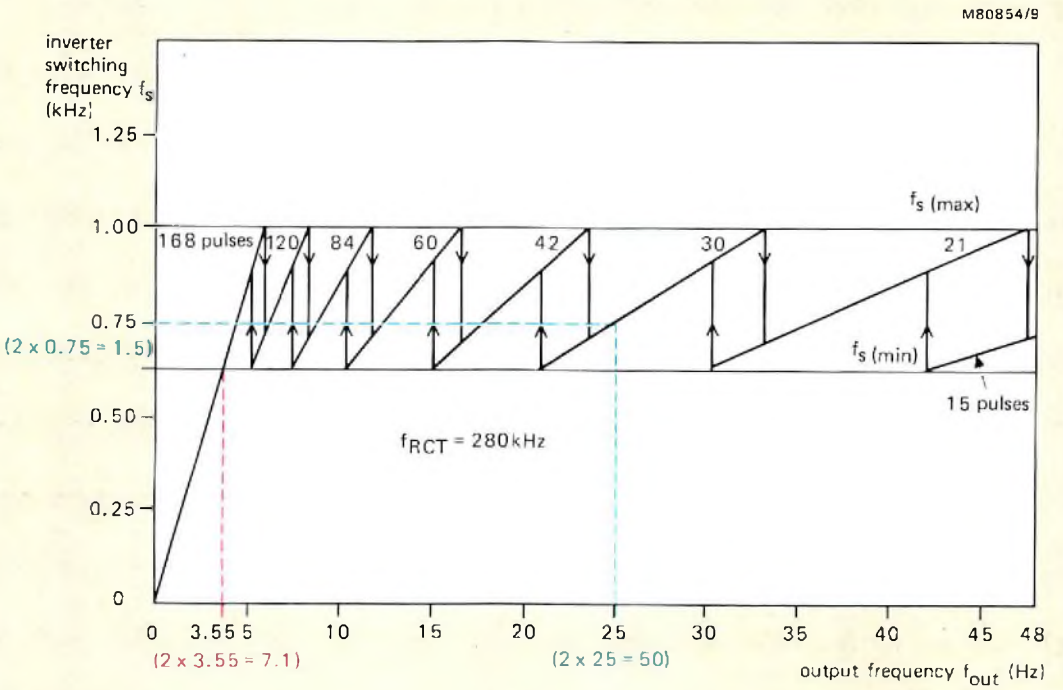


Fig.9 Inverter switching frequency against output frequency (expanded scale for low frequencies)

delay set by the K and OCT inputs, and is present irrespective of the L input state. The VAV signal has a frequency equal to the inverter switching frequency f_{out}, and a modulation given by $6f_{out}$.

VAV is useful for closed-loop control of f_{VCT} to obtain some improvement in the linearity of voltage with frequency when the frequency ratio f_{FCT}/f_{VCT} is greater than 0.5. The variation of VAV with frequency ratio is shown in Fig.10.

Inverter switching output CSP

The output CSP is a pulse train at twice the inverter switching frequency. The falling edge of each pulse occurs at the point of zero modulation of the main outputs. When f_{FCT}/f_{VCT} exceeds 0.5, CSP represents the theoretical inverter frequency; however, because of the merging of pulses from over-modulation, the actual switching frequency will be less. As with the VAV output, CSP is unaffected by the state of input L.

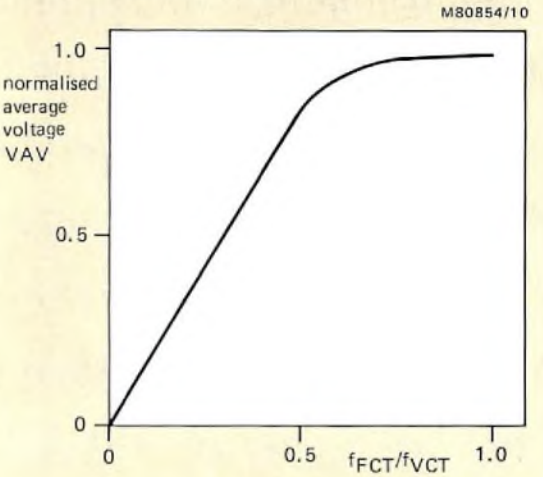


Fig.10 VAV against f_{FCT}/f_{VCT}

APPLICATION ADVICE

Proper operation of the IC requires limitations on the frequency ratio f_{FCT}/f_{VCT}, and on the range of f_{FCT}. These limitations have already been described under the discussion of the clock inputs VCT and RCT. Three additional conditions for ensuring satisfactory performance are now considered.

Start/stop input L

If input L is used in the thyristor mode, care must be taken to ensure that the switching edges are clean. For example, if some switch bounce occurs when switching to the LOW condition, then this can result in one or more of the M1 outputs being on instead of all the M2 outputs. A simple circuit to overcome this problem, together with the corresponding output waveform, is shown in Fig.11.

Switch-on conditions

For safe operation an initial switch-on period is required, during which the thyristor trigger circuits or transistor drive circuits are inhibited, and the correct clock and input conditions are established. During the first half of the switch-on period, the internal IC circuit should be reset. This can be done by either applying a HIGH signal to input A, or running the FCT clock for at least 3360 FCT pulses.

The required input states on all inputs must be established during the second half of this period. If FCT is to

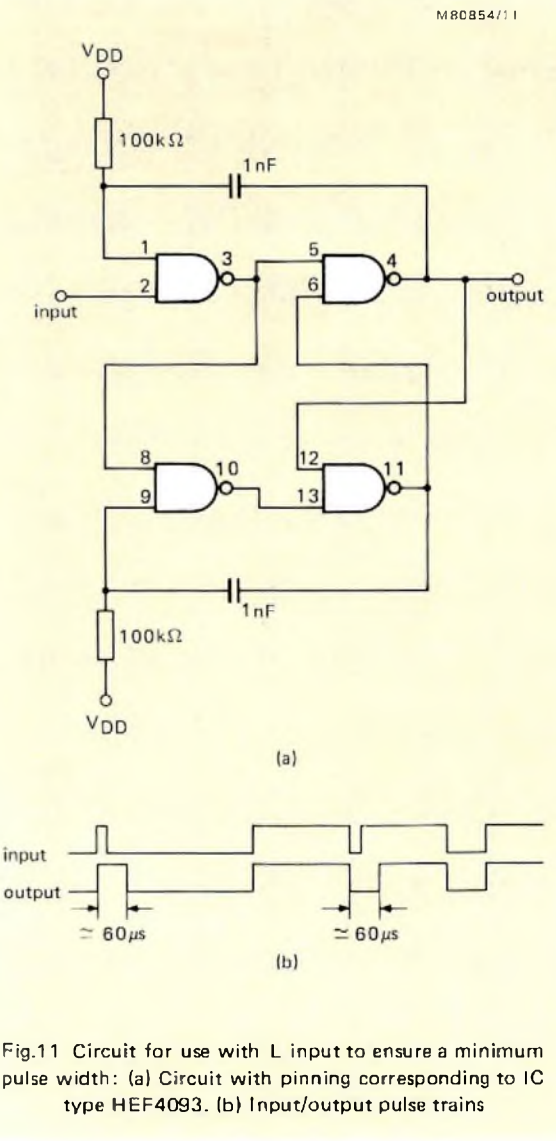


Fig.11 Circuit for use with L input to ensure a minimum pulse width: (a) Circuit with pinning corresponding to IC type HEF4093. (b) Input/output pulse trains

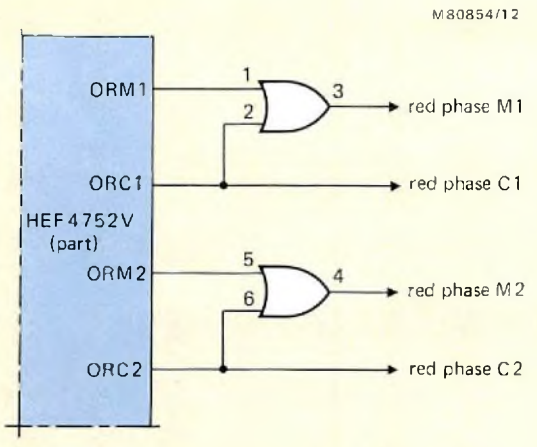


Fig.12 Circuit for producing a full length trigger pulse under minimum pulse width conditions. Pinning corresponds to IC type HEF4071

be started from zero during normal operation, it is advisable to run the FCT clock at about 0.04 f_{RCT} during the second half of the switch-on period for at least 3360 pulses, otherwise the output circuits will be set at 15 pulses per cycle for the first few pulses, instead of 168, which could result in damage to the inverter.

Minimum pulse width

From Figs.6 and 7 it can be seen that once the control signal (waveforms 6e and 7e) produces a pulse width equal to, or less than, the interlock delay, the appropriate main output is reduced to a narrow pulse. The width of this pulse is $1/f_{OCT}$ and it is always followed by a full-width commutation pulse. In the transistor mode, this narrow pulse will normally have little or no effect on the inverter. However, in the thyristor mode the correct triggering of the main thyristor may require the connection of the commutation pulse to the main pulse via an OR-function. A circuit to achieve this result is shown in Fig.12.

The next article in this series will describe the analogue control section.

REFERENCES

1. HOULDSWORTH, J.A. and ROSINK, W.B., 'Introduction to PWM speed control system for 3-phase AC motors', Electronic Components and Applications, Vol.2, No.2, February 1980, pp.66 to 79.
2. HOULDSWORTH, J.A. and BURGUM, F.J., 'Induction motor drive using new digital sinewave PWM system', IEE Conference on Electrical Variable-Speed Drives, London, September 1979.
3. BURGUM, F. and NIJHOF, E.B.G., 'Inverter circuit for PWM motor speed control system', Electronic Components and Applications, Vol.2, No.3, May 1980, pp.130 to 142.

ERRATA

E.C. and A., Vol. 2 No. 3, May 1980. The article 'Electret microphone for telephony' should have included the following acknowledgement:

The author gratefully acknowledge the research and cooperation of Dr. Ir. J. van Turnhout and his associates at the TNO Central Laboratory in Delft, many of whose publications are pertinent to the topic of this article.

Quality line

Quality-oriented designs and processes

Modern, complex, electronic equipment can be successful only if proper use is made of high-quality components. Economic production requires low fall-off and call rates, which, in turn, requires high quality in components, design and assembly. There is no acceptable level of quality: equipment complexity and rectification and repair costs are continually increasing. We know from our broad-based involvement in the industry that, as component suppliers, we shall always be asked for improved quality.

However, the very high quality demanded today can be achieved only if supplier and user cooperate to ensure that both are fully informed about component capabilities on the one hand and the special requirements of the application on the other. Only then can quality be optimised. This column will regularly report the steps we are taking to achieve this and the results we obtain.

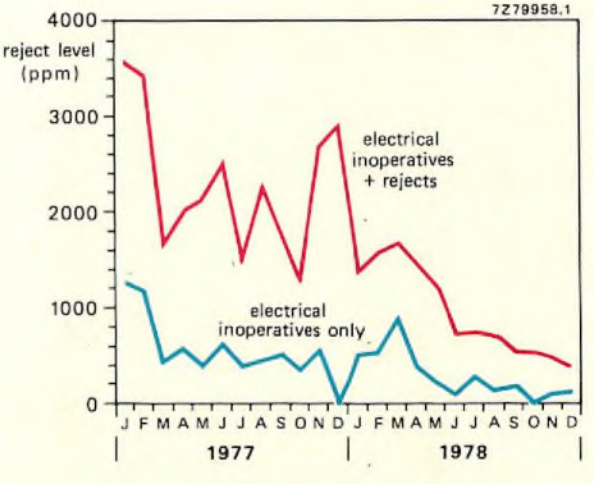
CONTINUING IMPROVEMENT IN CONSUMER-BIPOLAR IC QUALITY

Increased mechanisation and detail process improvements during 1977 and 1978 are reflected in an improvement in the reject level of new devices. This fell by nearly an order of magnitude over that period. The process-average reject levels from one IC factory for

(1) electrical inoperatives
and
(2) electrical inoperatives and limit rejects combined

are shown in the graph.

Reliability results from both laboratory testing and field experience indicate a failure rate of 0.7×10^{-6}/h after 5000 h operation, with a confidence level of 60%.



Process average from acceptance testing of our consumer-bipolar ICs during 1977 and 1978. Note the continually falling reject level resulting from improved overall quality

LOCMOS FAILURE RATES APPROACH 10^{-9}/h IN CERDIP

Owing to their greater complexity and finer structure, integrated circuits demand far more intricate quality control than discrete semiconductors. The basic principles, however, are the same. Quality in a finished product is achieved only by quality-oriented design and development, both of the products themselves and the processes by which they are made.

These were the guiding principles in our development of LOCMOS. Each of the quality-limiting factors of conventional CMOS was examined, and a solution package developed that not only allows a substantial improvement in device performance and reliability, but also permits a reduction in gate area that allows the use of fully-buffered circuitry. Gate dissipation, switching times, and device spreads are all reduced.

Reproducibility

Low spreads indicate that the good workmanship essential to high reliability is consisently achieved. LOCMOS processing reduces spreads: local oxidation of the die provides self-aligning masks; the polysilicon gates of individual MOSTs are inherently self aligned. Thus, channel lengths are uniform and spreads negligible.

Reliability

Two protection features are unique to LOCMOS: all inputs are protected by polysilicon resistors of well defined value; where this method is unpractical, a specially-developed network affords the same degree of protection.

Latch up

The features of the LOCMOS process enable precautions in die geometry to be taken that virtually eliminate latch up. Use of a substrate with an epitaxial surface layer avoids lateral current flow in the substrate itself and reduces the associated voltage drops. The greater diffusion accuracy possible allows careful design of the p^+ and n^+ pockets.

Moisture-level control in cerdip

A highly developed method of package-cavity dew-point measurement enables us to limit the moisture levels in packages, with a consequent improvement in long-term reliability.

Measured failure rates

Both static and dynamic life tests are performed on LOCMOS devices sampled from regular production at temperatures of 125 °C, 150 °C and, for hermetic devices only, at 175 °C. In addition, we use plastic-packaged LOCMOS devices in our own automatic test equipment; this operates 24 h per day.

Failure rate for plastic-packaged LOCMOS, normalised to a die temperature of 50 °C, is 19.54 x 10^{-9}/h, or 21 x 10^{-9}/h with a confidence level of 60%. For cerdip-packaged LOCMOS the failure rate, normalised to a die temperature of 50 °C, is 2.2 x 10^{-9}/h, or 4.5 x 10^{-9}/h with a confidence level of 60%.

For cerdip-packaged LOCMOS, the failure rate, normalized to a die temperature of 50 °C, is 2,2 x 10^{-9}/h, or 4,5 x 10^{-9}/h with a confidence level of 60%.

IMPROVED RECTIFIER RELIABILITY FROM GLASS-BEAD DIODES

Glass-bead diode construction is shown in the cut-away drawing. A bevelled, double-diffused die is alloyed to two molybdenum studs to which are brazed the axial leads. This arrangement makes for excellent heat transfer. A bead of void-free glass of matching temperature

Cut-away view of a SOD-57 glass-bead diode package as used for the BYW54 family showing the robust, hermetic construction used

coefficient both protects the junction and provides the mechanical strength of the assembly. Finally, leads and studs are tinned for good solderability.

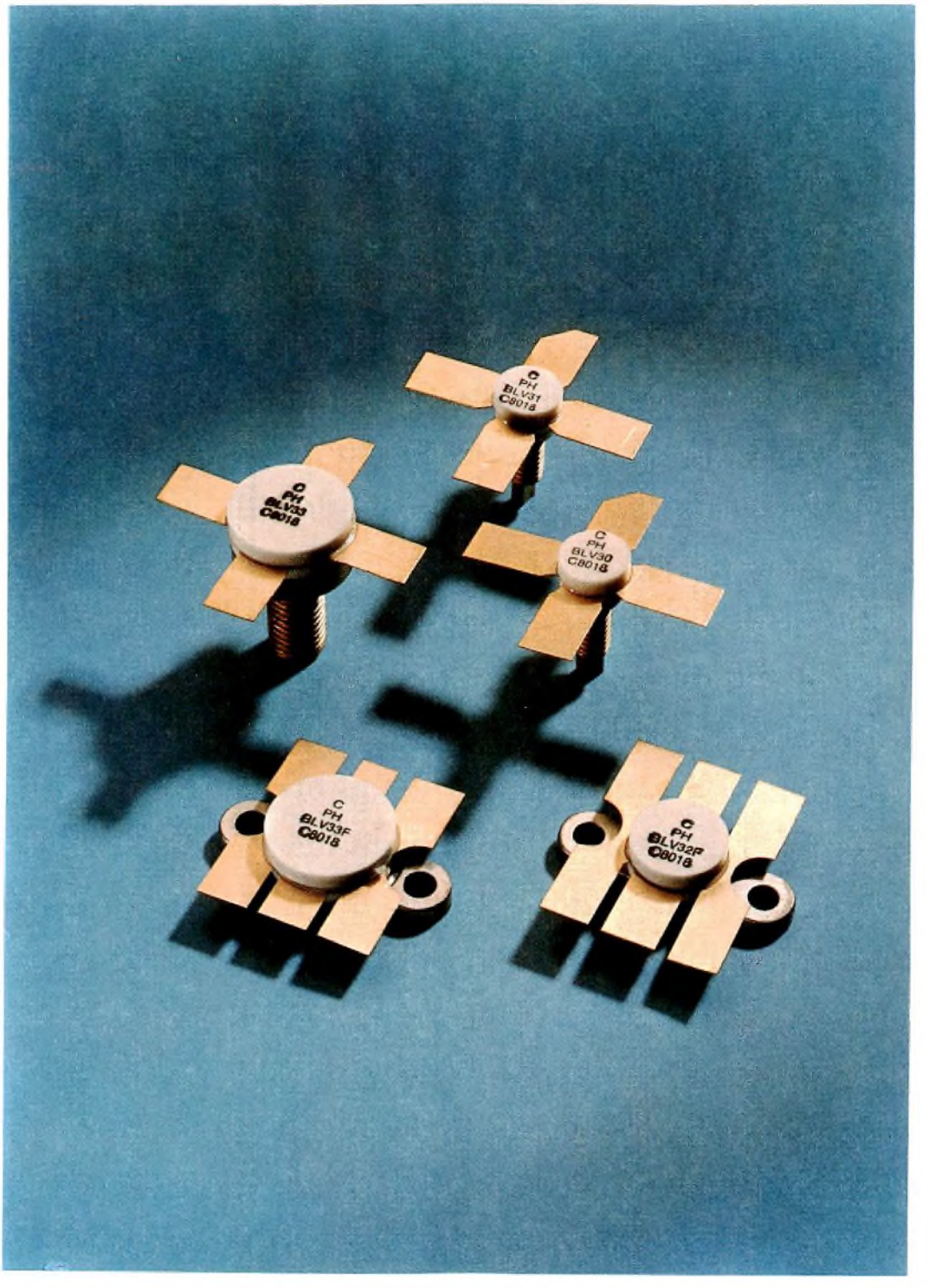
Glass-bead diodes like the BYW54 family have been developed to overcome the weakness of plastic encapsulated rectifiers. Epitaxial diodes (BYV27/28) and fast recovery diodes (BYV95/96) are also available in the same envelope. Since 1977 production has been carried out in a CECC-approved factory and the diodes themselves are available to CECC 50008-015. The principal characteristics of the BYW54 family are given in Table 1. Table 2 gives the failure rates during the constant-failure-rate period of glass-bead diodes and comparable 1 A/1000 V plastic-encapsulated diodes. Despite their more severe test conditions, glass-bead diodes show better stability and reliability.

TABLE 1
Principal characteristics of the BYW54 family of glass-bead rectifier diodes

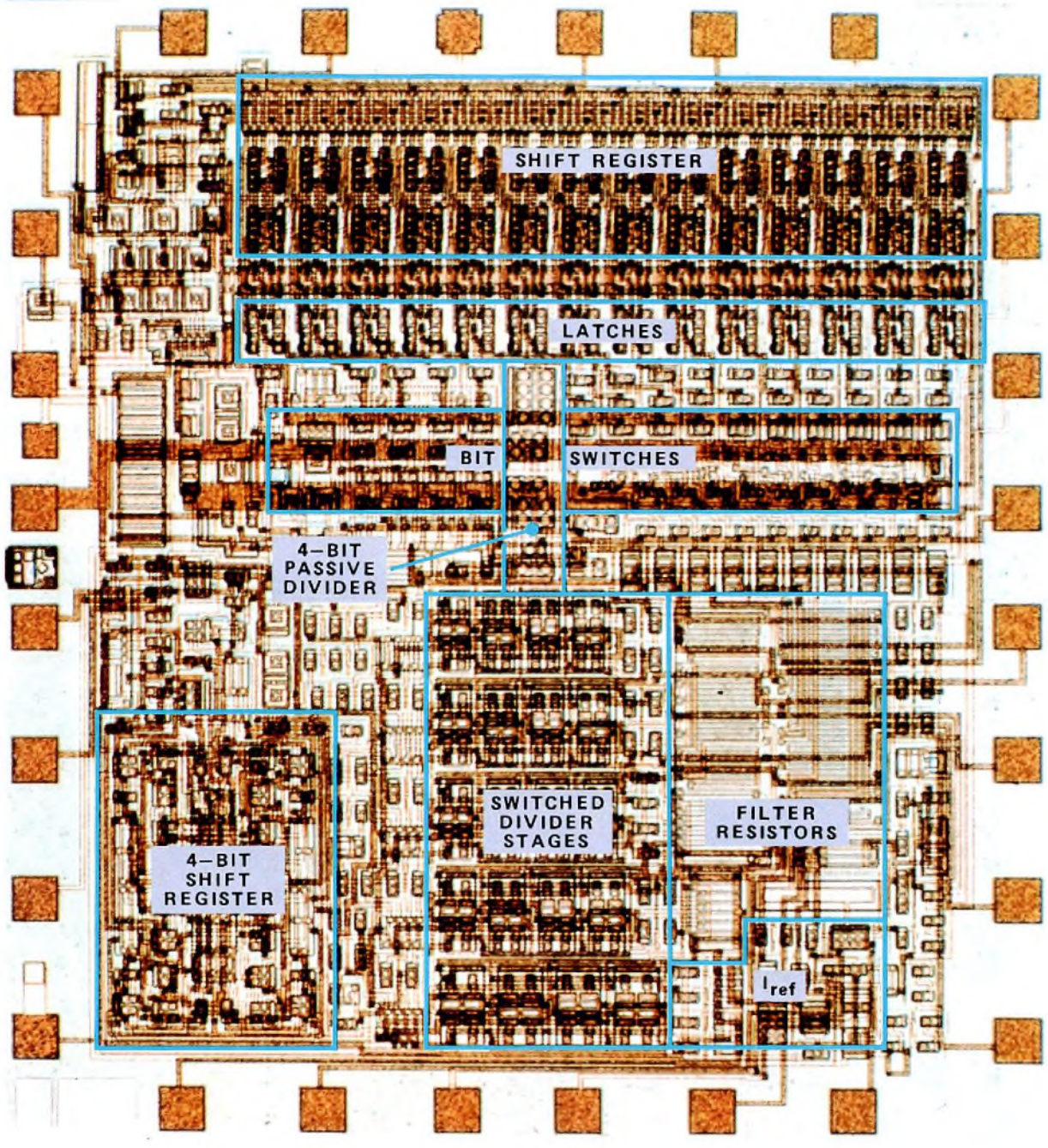
	BYW54	BYW55	BYW56
maximum crest working voltage	600 V	800 V	1000 V
reverse avalanche breakdown voltage	>650 V <1000 V	>900 V <1300 V	>1100 V <1600 V
maximum average forward current	2 A	2 A	2 A
maximum non-repetitive peak forward current	50 A	50 A	50 A
maximum non-repetitive peak reverse power dissipation	1 kW	1 kW	1 kW
maximum junction temperature	165 °C	165 °C	165 °C

TABLE 2
Comparison of failure rates during constant-failure-rate period of glass-bead diodes and comparable plastic-encapsulated rectifier diodes

test	package	conditions	failure rate (60% confidence level)
d.c. reverse voltage	plastic	800 V reverse, 100 °C ambient	45×10^{-6}/h
	glass-bead	800 V reverse, 150 °C ambient	12.9×10^{-6}/h
RC load	plastic	800 V peak reverse, 60 °C ambient, 0.55 A average	23×10^{-6}/h
	glass-bead	1000 V peak reverse, 60 °C ambient 0.7 A average	9.8×10^{-6}/h
thermal fatigue (on and off times: 90 s)	plastic	1.5 A, 25 °C ambient, 100 °C junction swing	2.5×10^{-6}/cycle
	glass-bead	1.8 A, 25 °C ambient, 140 °C junction swing	0.25×10^{-6}/cycle



Reliable unattended operation for extended periods is essential for linear wideband r.f. power amplifiers and drivers in band III television transmitters and transposers. Our new BLV30 series of npn silicon planar epitaxial r.f. power transistors have been specifically developed for this purpose. Gold-sandwich metallisation ensures the long life of the transistors by minimising electromigration. Multiple base and emitter geometry, together with a shallow diffusion, ensures high gain and good linearity. Diffused emitter ballast resistors give even current distribution. The first five transistors of the new series are now available. They provide minimum peak sync power outputs of 1.5 W to 19 W (class A) 80 W to 100 W (class AB) at a vision carrier frequency of 224.25 MHz with a heatsink temperature of 70 °C. Under these conditions, the 3-tone intermodulation distortion remains below −55 dB. Application information and data are available on request



Layout of the 3.0 x 3.4 mm TDA1540 chip

Monolithic 14-bit DAC with 85 dB S/N ratio

R. J. v. d. PLASSCHE

The introduction of digital signal processing in sound recording and reproduction systems imposes stringent requirements on the performance of digital-to-analogue converters (DACs). Many of these systems demand converters with up to 16-bit resolution to obtain sufficiently high signal-to-noise ratio and good linearity.

The TDA1540 is the first monolithic bipolar 14-bit DAC with a signal-to-noise ratio of 85 dB (typ) for audio signals, sampled at 44 kHz. It uses a new method of current division, called dynamic element matching, to achieve high-accuracy binary-weighted currents, with long-term stability. Dynamic element matching combines passive division with a time division concept which eliminates resistor trimming.

In addition, the TDA1540 features:

- on-chip serial-to-parallel shift register and data latches,
- on-chip current reference,
- inherent monotonicity from −25 to +70 °C,
- TTL compatible input,
- serial data input (offset binary) which reduces feed-through and correlated noise,
- improved bit switching – no deglitching circuit required.

Table 1 gives further data on the TDA1540.

STANDARD DIGITAL-TO-ANALOGUE CONVERSION TECHNIQUES

Monolithic DACs widely use an R-2R resistive ladder network with multiple-emitter terminating transistors to generate binary-weighted currents. These currents are switched by digitally-controlled switches (bit switches) to a summing point; thereby digital-to-analogue signal conversion is performed. Figure 1 shows a DAC of this type.

There are two problems in the design of an R-2R DAC: the weighting accuracy of the binary currents which is set by the tolerance of the resistors and transistors, and the switching of the accurately weighted binary currents without glitches which determines the dynamic performance. Regarding the problem of accuracy, Table 2 shows that it is straightforward to integrate DACs having up to 10 bits; a 10-bit converter requires a 512:1 current division, i.e. requires resistor tolerance better than 0.05%. Twelve-bit converters usually need laser trimming of thin-film resistors, or trimming of the binary-weighted currents using Zener zapping to achieve 12-bit accuracy.

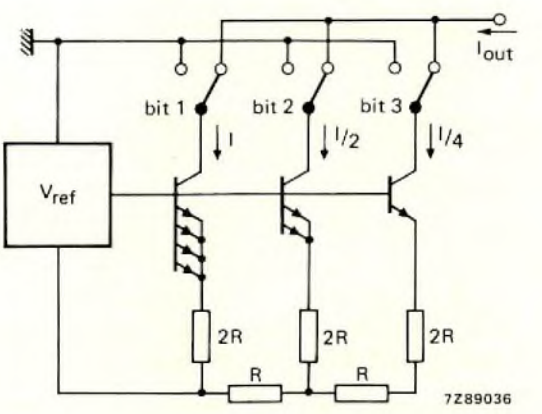


Fig.1 3-bit binary-weighted R-2R digital-to-analogue converter

TABLE 1
TDA1540 data

Resolution	14 bits
Signal-to-noise ratio* (typ.)	85 dB
Linearity (typ.)	±¼LSB at T_{amb} = 25 °C
	±½LSB −20 °C < T_{amb} < +70 °C
Full-scale current (typ.)	4 mA
Settling time to +½LSB (for a full-scale change)	typ. 1 μs
Maximum input bit rate	12 Mbit/s
Power dissipation	350 mW
Supply voltages	+5 V, −5 V and −17 V
Encapsulation	28-pin ceramic DIL

* measured between 31.5 Hz and 20 kHz at a sampling frequency of 44 kHz.

TABLE 2
Matching tolerance of different types of resistor

fabrication process	matching tolerance			
	σ(%)		mean (%)	
	10 μm	40 μm	10 μm	40 μm
Diffusion	0.44	0.23	−0.1	0.07
Thin-film	0.24	0.11	−0.1	−0.06
Ion implantation	0.34	0.12	−0.04	0.05

Resistor linewidth 10 μm and 40 μm.

It is questionable how successfully trimming can be applied to 14 or 16-bit converters. Mounting the chip after trimming can change the resistances; trimming after mounting can be expensive. Long-term stability may be a problem too. Furthermore, the cost of laser trimming in large-volume production can be significant.

In the TDA1540 trimming has been eliminated by dynamic element matching.

DYNAMIC ELEMENT MATCHING

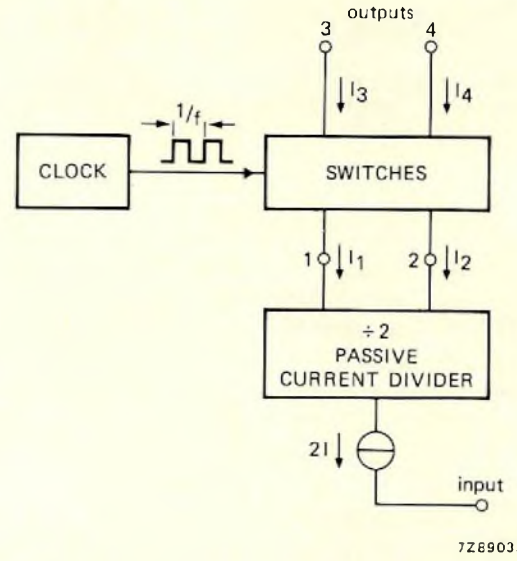
Basic current divider

Figure 2(a) shows the block diagram of the divider. It consists of a passive current divider and a set of switches driven at a frequency f by a clock pulse generator.

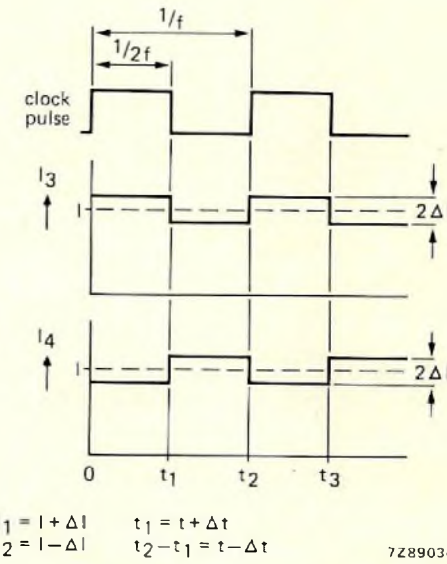
The input current 2I is divided into two nearly equal parts: $I_1 = I + \Delta I$ and $I_2 = I - \Delta I$. Then, I_1 and I_2 are interchanged with respect to the output terminals 3 and 4 *for equal times* by means of the switches. The average current at each output terminal is then exactly equal and has a value I, see Fig.2(b).

There is a small ripple current 2ΔI (p-to-p) of frequency f on the output currents. This ripple is proportional to the accuracy of current division by the passive divider. By using a simple low-pass filter to suppress the ripple an exact current ratio of 2:1 (input-to-output) is obtained.

If the time that I_1 and I_2 are switched to each output differs by Δt, see Fig.2(b), there will be an error in their 1:1 current ratio of $(\Delta t/t)(\Delta I/I)$. For $\Delta I/I \approx 1\%$ and $\Delta t/t \approx 0.1\%$, this error is ≈0.001%.



(a) Basic current divider using dynamic element matching



(b) Output currents I_3 and I_4

Fig.2

By cascading divider stages an accurate binary-weighted current network is formed. However, in a practical circuit, each stage requires a minimum supply voltage of ≈2 V. This leads to an impractically large supply voltage for a 14-bit current network. Therefore, an improved divider is used which gives more weighted currents in one current interchange.

Improved divider

In the improved divider, a current 4I is divided into four nearly equal parts: $I + \Delta_1 I$, $I + \Delta_2 I$, $I + \Delta_3 I$ and $I + \Delta_4 I$, see Fig.3(a). Note that $\Delta_1 + \Delta_2 + \Delta_3 + \Delta_4 = 0$.

These currents are fed into a switching network which interchanges all the currents with respect to the output terminals for equal times. The switches are controlled by signals from a 4-bit shift register.

At the output of the switching network, two currents are combined; thus, the output currents have average values of 2I, I and I, Fig.3(b). All currents have a ripple of frequency f/4 (the time for one complete interchange of the four currents being 4/f). Timing errors in the current switching have the same effect on accuracy as for the basic divider.

Figure 4 shows the circuit diagram of a practical current divider. Transistors TR1, TR2, TR3 and TR4, with the resistors R divide the current 4I into four nearly equal currents. These currents are fed into the switching network which consists of Darlington transistor switches to minimise base current loss. Two currents are summed directly giving an output current of 2I (av.). A 4-bit shift register controls the transistor switches which for accurate current division must have high current gain.

BINARY-WEIGHTED CURRENT NETWORK

By cascading divider stages, a binary-weighted current network is formed, see Fig.5. In the first stage the on-chip reference current source I_{ref} and a current amplifier form an accurate current mirror. The reference current is used as the most significant bit current, which eliminates filtering.

To obtain 14-bit accuracy, a choice can be made between the number of switched and unswitched current dividers. The minimum supply voltage decreases as the number of unswitched dividers increases. However, the number of unswitched dividers is limited by circuit yield. Five switched dividers followed by a 4-bit passive divider using emitter scaling represents the best compromise between supply voltage and circuit yield.

FILTERS AND BIT SWITCHES

Figure 6 shows how the output currents of a switched divider stage are filtered and switched to the output. R1C1 and R2C2 form first-order filters (the capacitors are connected externally). Darlington transistors TR3, TR4 and TR5, TR6 isolate the filters from the switching of the binary-weighted currents to the output (bit switching). Bit switching is performed with a diode-transistor configuration TR1, D1 and TR2, D2, enabling fast and accurate switching with no loss of base currents.

Individual filtering of bit currents minimises the noise of the TDA1540 output current, and makes the conversion time solely dependent upon the speed of the bit switches.

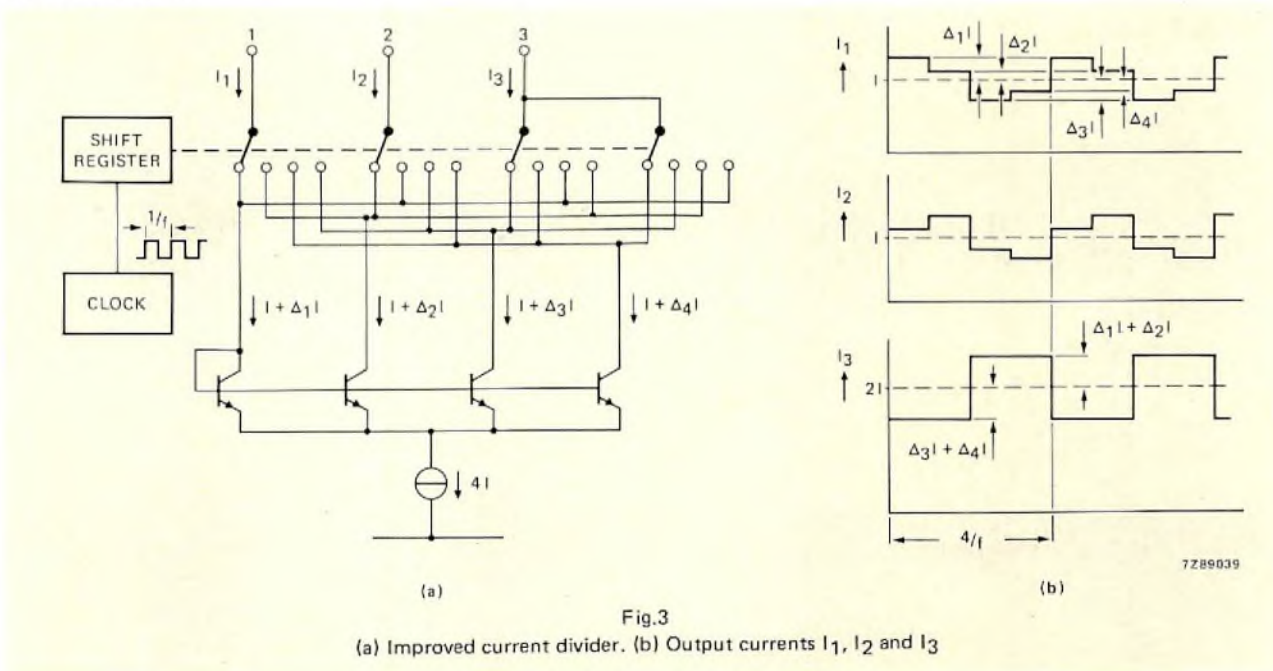


Fig.3
(a) Improved current divider. (b) Output currents I_1, I_2 and I_3.

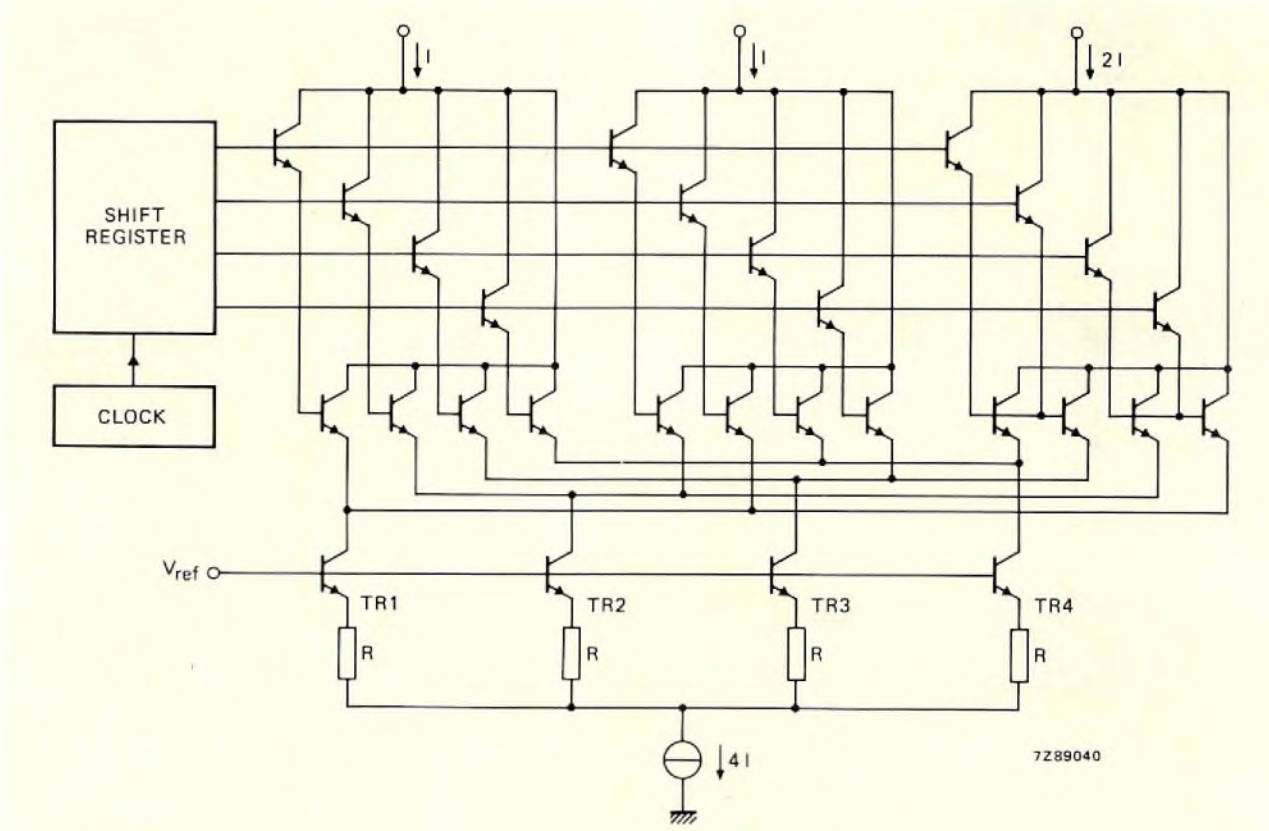


Fig.4 Circuit diagram of the practical current divider

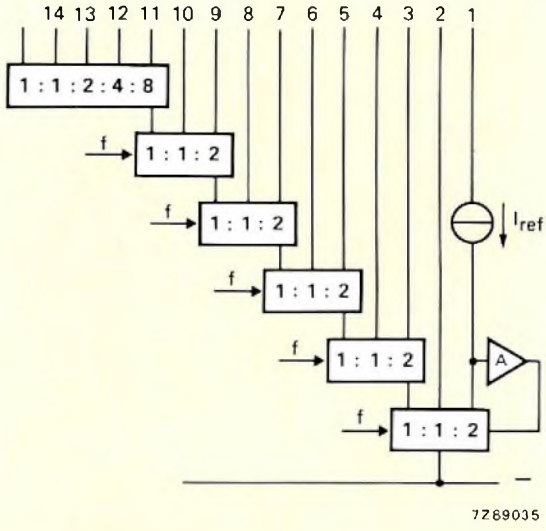


Fig.5 Binary-weighted current network

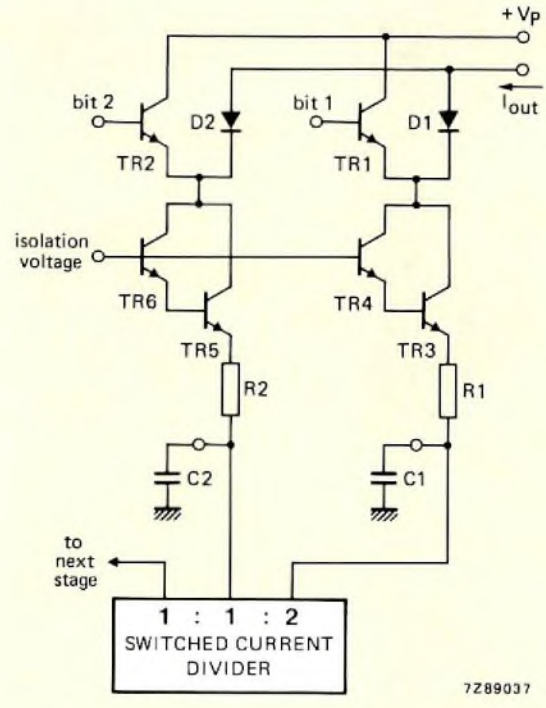


Fig.6 Filtering and switching the binary-weighted currents to the output

COMPLETE 14-BIT DAC

Figure 7 is the block diagram of the complete DAC. It shows the 14-bit binary-weighted current network, the reference current source, individual bit-current filters and the bit switches. The shift register that controls the Darlington transistor switches is at the bottom of the figure.

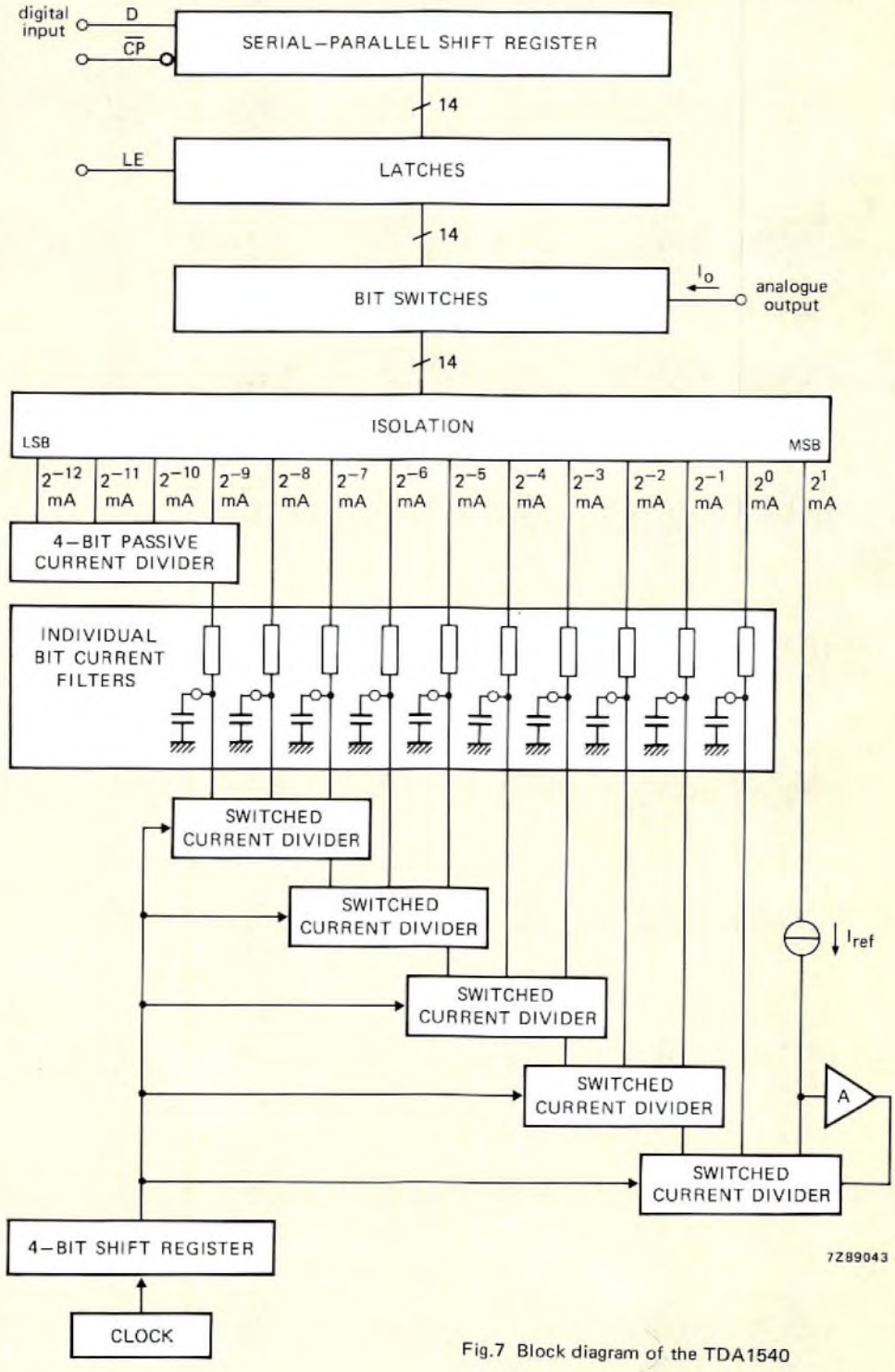


Fig.7 Block diagram of the TDA1540

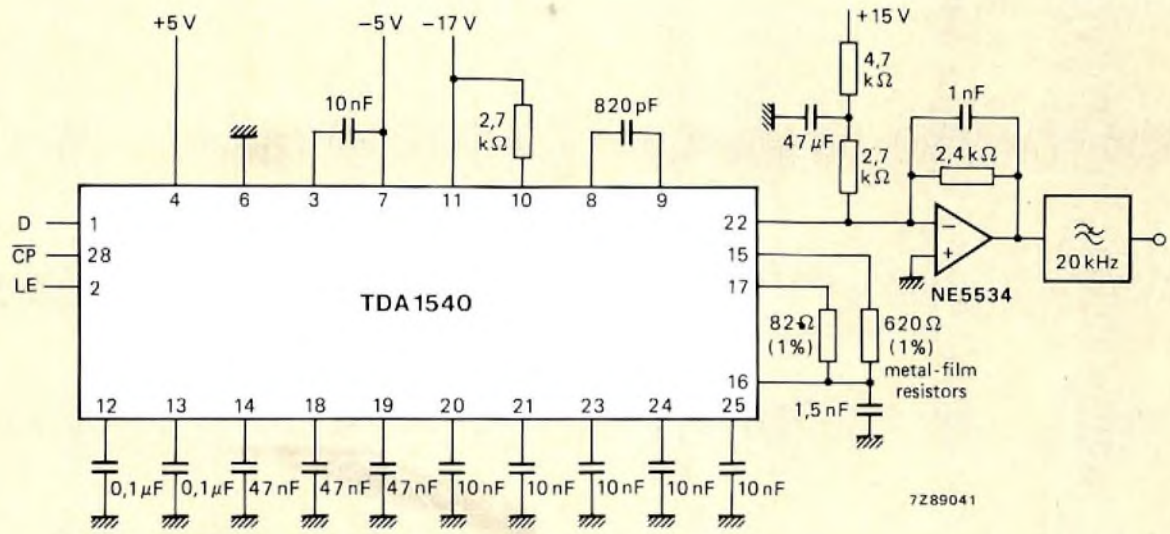


Fig.8 Circuit diagram of a voltage-output digital-to-analogue converter using the TDA1540

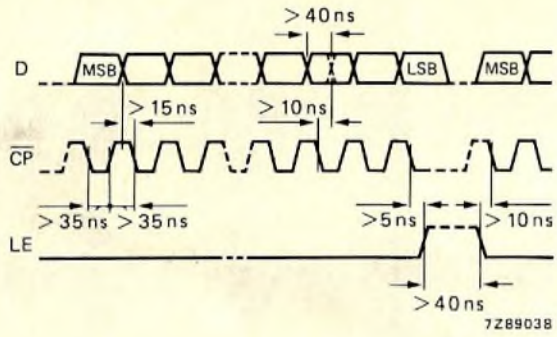


Fig.9 TDA1540 timing diagram

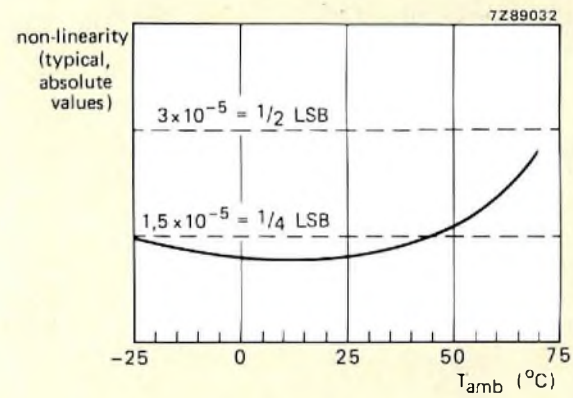


Fig.10 Non-linearity of the TDA1540 as a function of temperature

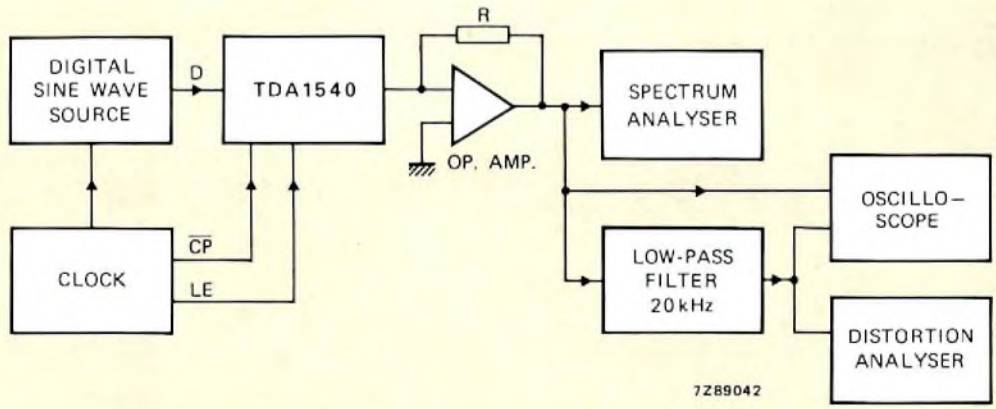


Fig.11 Arrangement for measuring dynamic performance

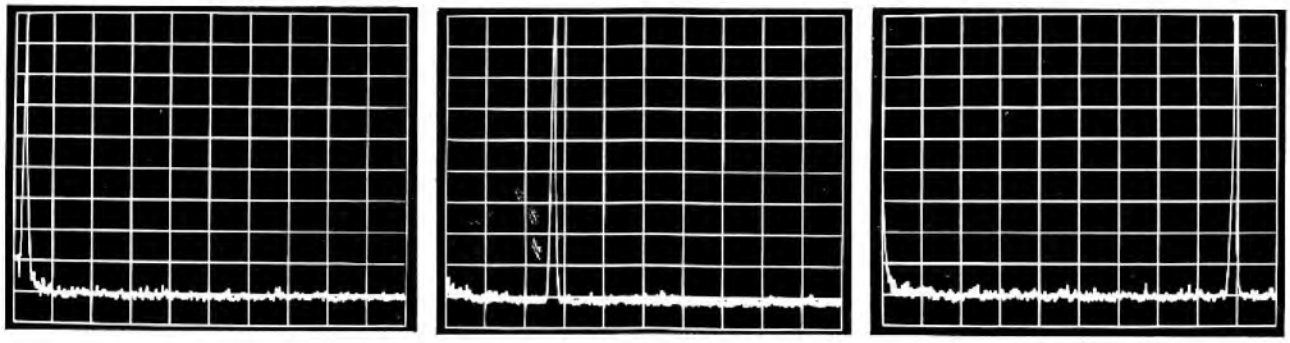


Fig.12 Distortion of an output sinewave of frequency 600 Hz, 5.5 kHz and 18 kHz, respectively. Vertical scale 10 dB/div., horizontal scale 2 kHz/div. Bandwidth 30 Hz

Figure 8 shows how to obtain a voltage output using the TDA1540 with an operational amplifier.
Figure 9 shows the input data format D, and the corresponding timing signals $\overline{CP}$ (clock input) and LE (latch enable).

PERFORMANCE

Linearity

A DAC is monotonic if the non-linearity is less than ±½ LSB. Figure 10 shows that the non-linearity of the TDA1540 is typically less than ½LSB (3×10^{-5}) over the temperature range −20 to +70 °C.

Dynamic performance

Figure 11 shows the arrangement used to measure dynamic performance. A digital sine wave source produces 14-bit words which are latched at 44 kHz. The outputs of the latches drive directly the bit switches of the converter. A high-speed operational amplifier with feedback resistor R converts the output current of the converter into a voltage suitable for examination by spectrum analyser and oscilloscope, or distortion analyser.

Figure 12 shows the results of spectrum analysis. For sine waves of 600 Hz, 5.5 kHz and 18 kHz, distortion is about −90 dB with respect to the maximum sine wave output. Note, −90 dB is the limit of resolution of the spectrum analyser.

Figure 13 shows oscillograms of the filtered and unfiltered output signals. The low-pass filter introduces a delay in the output signal.

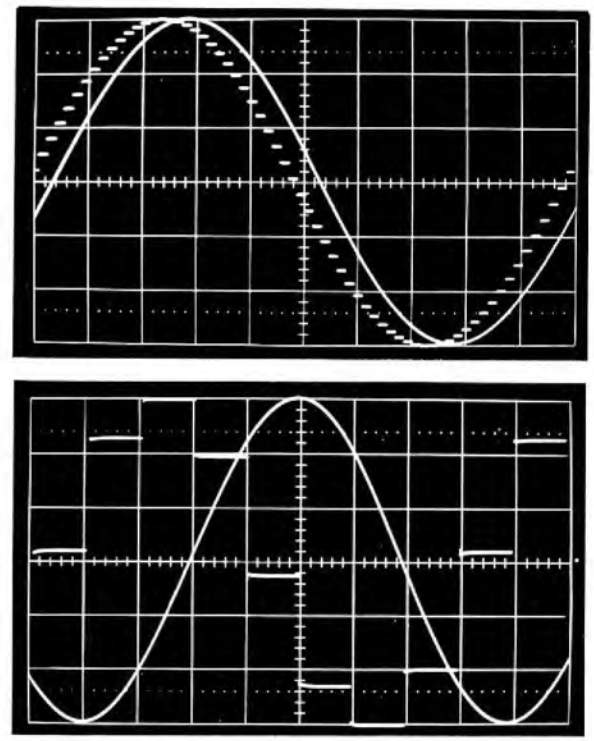


Fig.13 Filtered and unfiltered output signals: above, 1 kHz; below, 6.3 kHz. Vertical scale 0.33 volt/div.

APPLICATIONS

Dynamic element matching is a simple, accurate and reliable method of current division for high-accuracy monolithic DACs; the resulting dynamic performance of the TDA1540 makes it ideal for sound reproduction and recording systems.

Its 15-bit linearity also makes it suitable for applications that do not require 14-bit resolution, but demand high linearity to improve relative accuracy. Such applications include graphic display systems, electron-beam recording and nuclear instrumentation.

The TDA1540 easily fulfills the requirements of a 12-bit DAC for telephony. For instrument manufacturers, the TDA1540 can extend present limits of performance of distortion meters, spectrum analysers, sine wave and other signal generators.

The use of over-sampling techniques with the TDA1540 further improves the S/N ratio in audio applications and simplifies output analogue filters.

PCM codec with on-chip digital filters

D. J. G. JANSSEN and L. v. d. MEEBERG

In EC&A Vol. 2, No. 1 we gave a brief description of a new approach to the design of an integrated PCM codec for telephony. It was explained that one of the major difficulties in designing a monolithic PCM codec, together with its filters, is obtaining sufficient accuracy and long-term stability for the 3.4 kHz low-pass analog filters. Although the comparatively long time-constants required can be achieved with integrated switched capacitor ladders, this technique has yet to be proved as far as its long-term (up to 20 years) stability is concerned. A second obstacle to codec integration is the additional process control required for integrating the weighted current-sources or ladder networks of resistors which define the quantising levels in the encoder and decoder. Finally, if the integrated codec incorporates precision analog circuitry, the testing procedures are time consuming and costly.

In our new single-channel PCM codec, the need for high-resolution quantising has been eliminated and the transfer function requirements for the anti-aliasing analog filters have been simplified. The need for accurate quantising is overcome by using Sigma-Delta modulation as an intermediate pulse code. The high sampling rate then allows the use of low-performance analog filters. Digital code converters recode the Sigma-Delta bit-stream into standard PCM and vice-versa. The steep band-limiting function at 3.4 kHz is performed by non-recursive digital filters.

The new design allows the precision analog circuitry and associated high-performance filters of a conventional codec to be replaced by digital circuitry. The circuit fully meets the technical requirements of the telephone industry and allows rapid 100% testing of the integrated circuitry by a special scan-test method.

DESIGN PHILOSOPHY

Since the voice signals in telephony PCM systems are sampled at 8 kHz, a vital part of a conventional PCM encoder is an analog filter which limits the bandwidth of the input signal to 4 kHz. This filter must meet the CCITT requirements for small ripple in the passband and sharp cut-off. At the output of a conventional PCM decoder, the out-of-band components of the reconstituted analog signal are suppressed by a sharp cut-off analog filter similar to the one preceeding the encoder. In a typical encoder circuit, the band-limited analog signal is sampled at 8 kHz and converted into digital form by a companding A to D converter. The decoding process takes place in the reverse sequence.

The most popular technique for A to D and D to A conversion in PCM codecs is successive approximation in which the quantising levels are defined by weighted current-sources or resistors. The required signal-to-noise ratio demands that the converters have a resolution of twelve bits. The filtering, A to D conversion and D to A conversion require precision analog circuitry on the chip. It is desirable to minimise this precision circuitry to achieve the necessary long-term stability and facilitate rapid testing.

Much of the information contained in this article is derived from a paper presented by Mr. v. d. Meeberg on June 10th, 1980 at the IEEE sponsored International Conference on Communications (ICC'80) in Seattle, Washington, USA.

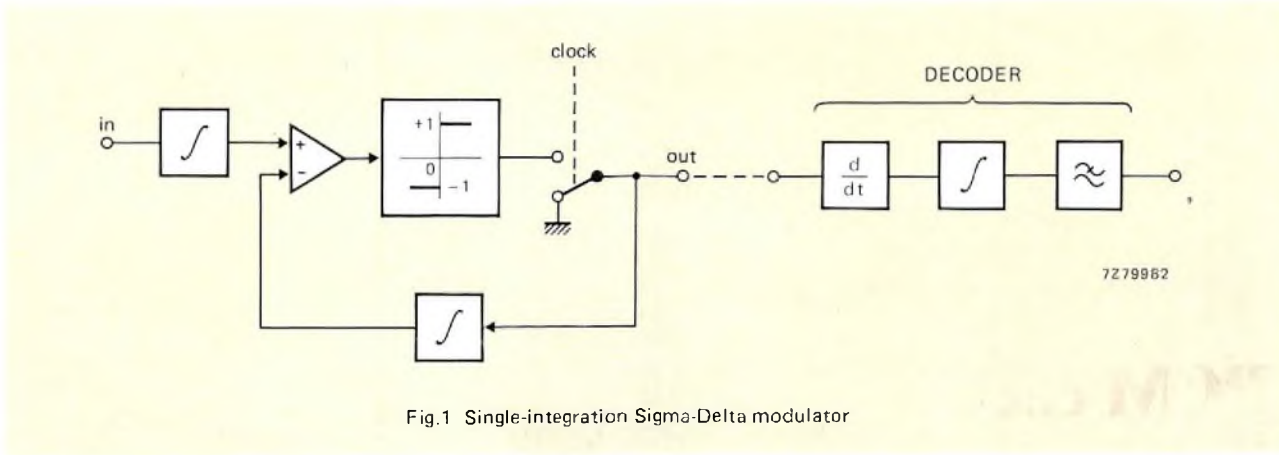


Fig.1 Single-integration Sigma-Delta modulator

It has been shown by Goodman, Candy and others (Ref. 1, 2 and 3) that analog circuit complexity and accuracy can be traded-off against digital circuit complexity and speed. Our new codec therefore uses digital filters for the band-limiting function and easily-implemented Sigma-Delta modulators for the A to D and D to A conversion. A uniform Sigma-Delta modulator is especially suitable for the encoder because the 1-bit samples can be easily processed in a non-recursive digital filter. The use of integrated digital filters also results in the following additional advantages.

- The digital filters can be exhaustively analysed by a scan-test (Ref. 4) which may be applied either during production or after installation.
- Any required accuracy can be achieved. The only limitations are speed and required chip area.
- The parameters of the digital filters do not vary during production or change with temperature variations or ageing.
- The integrated circuit process does not require any precision control.
- The cost is potentially low because the chip area occupied by digital circuits will be reduced more rapidly than the area occupied by analog circuits.
- The filter coefficients can be altered to suit specific requirements by modifying only one mask.
- The power consumption can be very low when using CMOS or dynamic NMOS.

THE ENCODER

The Sigma-Delta modulator

The signal-to-noise ratio and the overload characteristic of the well-known uniform, single-integration Delta modulator (Ref. 5 and 6) is inversely proportional to the frequency of the input signal. It can be made constant within the signal frequency range by inserting an integrator into the input signal path. The resulting circuit is a Sigma-Delta modulator (Ref. 7) as shown in Fig.1. The corresponding decoder has to be extended with a differentiator to compensate for the extra integrator in the encoder. However, since the differentiator and the integrator in the decoder are complementary, they can be removed so that the decoder then consists solely of a low-pass filter.

Since integration and subtraction are both linear operations, their functional sequence can be interchanged. This results in a Sigma-Delta modulator with only one integrator.

It is well-known that the signal-to-in-band-noise ratio can be increased by replacing the single integrator with a double integrator (Ref. 5). The performance can be yet further improved by using a higher order low-pass filter. Increasing the stop-band attenuation however, leads to a larger phase shift which results in a less stable feedback system and degrades the performance again.

Optimisation of the performance by careful filter design has been thoroughly studied (Ref. 8). It has been shown that a good compromise between analog circuit complexity and sampling rate is obtained with a third-order filter and a sampling rate of 256 kHz. This results in a signal-to-in-band-noise ratio of 38 dB for a signal level of −40 dB.

The transfer function of the filter largely determines the spectrum of the quantising noise. If we denote the spectra of the signals given in Fig.2 by X(z), D(z) and Q(z), it is easy to see that

$$D(z) = [X(z) - Q(z)]\,H(z) \qquad (1)$$

where H(z) is the transfer function of the (time discrete) loop filter. Q(z) can be described as the spectrum of the amplified decision signal Ad(n) to which a quantising error spectrum E(z) is added. This can be expressed as

$$Q(z) = AD(z) + E(z) \qquad (2)$$

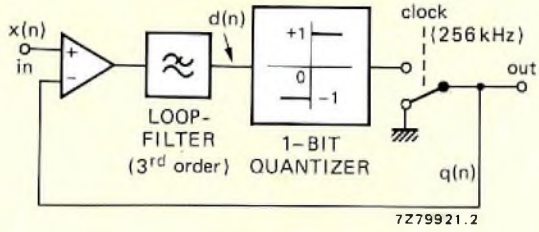


Fig.2 Sigma-Delta modulator with third-order loop filter

Combining equations (1) and (2) and solving for Q(z) gives

$$Q(z) = X(z)\frac{AH(z)}{1 + AH(z)} + E(z)\frac{1}{1 + AH(z)} \qquad (3)$$

Ref. 8 shows that the spectrum E(z) can be made flat over a wide range so that, for AH(z) much greater than unity, the quantising noise spectrum (the right-hand term in eq. (3)) is approximately the reciprocal of H(z). A typical spectrum of Q(z) for a small input signal is shown in Fig.3. Although the total noise power is constant, the filter shapes the quantising noise spectrum so that the noise power in the voice band is minimised. Moreover, the noise power spectrum is independent of the signal frequency. Eq. (3) also shows that the signal transfer function Q(z)/X(z) is approximately flat in the voice band if AH(z) is much greater than unity.

The 256 kHz sampling frequency sufficiently exceeds the upper frequency limit of the voice band to allow a very simple first-order analog anti-aliasing filter to suppress spurious input signals above 252 kHz. Another advantage of Sigma-Delta modulation is the simple convolution of the 1-bit samples with the coefficients of the subsequent digital filter.

The digital signal processor

The filter following the Sigma-Delta modulator must not only limit the bandwidth of the signal but must also suppress the out-of-band noise generated by the Sigma-Delta modulator. After filtering, the signal is subsampled at 8 kHz, compressed to eight bits and then loaded into a parallel to serial converter. An 8 kHz synchronisation pulse assigns a time-slot during which the burst of eight bits appears at the encoder output at a rate of 2.048 Mbits/s. This allows up to thirty-two channels to be multiplexed onto one PCM bus. An offset control circuit compensates any eventual offset in the Sigma-Delta modulator. All of the signal processing functions, together with the digital part of the Sigma-Delta modulator, are included in one LSI circuit.

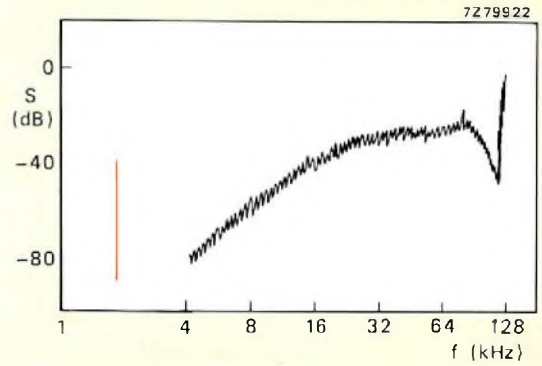


Fig.3 Typical output spectrum of Sigma-Delta modulator for sinewave input signal of −40 dBm

Operating principles

A filter with a symmetrical impulse response is easy to implement because it is only necessary to store the coefficients which define one half of the impulse response. Because of this, such a filter which also has a linear phase characteristic has been used. A length of 320 is necessary to meet the transfer function requirements. The 160 filter coefficients are divided into five sets as shown in Fig.4. The coefficient sets which define the smaller outer lobes of the impulse response require fewer bits than those which define the main lobe. This allows the ROM capacity to be minimised.

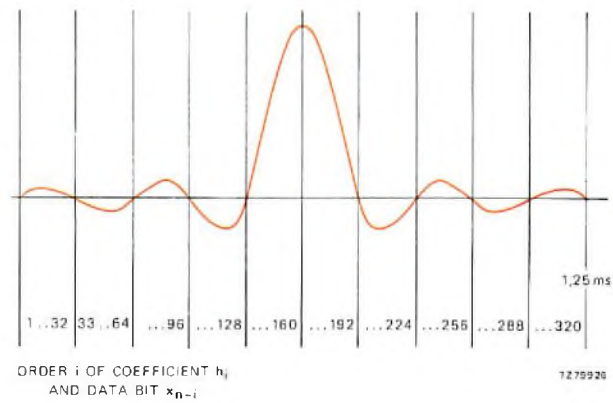


Fig.4 Symmetrical impulse response of decimating digital filter

The implementation of the filter is shown in Fig.5. The Sigma-Delta modulation bits are stored in nine 32-bit shift registers. The fifth (middle) register is arranged to reverse the data in the four subsequent registers so that they correspond with the second half of the impulse response (Ref.9). We will index the filter coefficients h_1 to h_{320} while $h_i = h_{321-i}$ ($i = 1$ to 160). During a given time slot $(n - 32)T$, the output from the left-hand data adder will be $x_{n-32} + x_{n-289}$. During the same time slot, coefficient h_{32} is selected from the ROM and multiplied by $x_{n-32} + x_{n-289}$. Similar products are produced by the other four multipliers and the accumulator then contains:

$$\sum_{j=1}^{5} (x_{n-32j} + x_{n-321+32j})\, h_{32j}$$

During the next time slot, a new data bit is presented the filter input, the left-hand multiplier produces $(x_{n-31} + x_{n-290})\, h_{31}$, and the accumulator then contains:

$$\sum_{k=0}^{1} \sum_{j=1}^{5} (x_{n-32j+k} + x_{n-321+32j-k})\, h_{32j-k}$$

During the 32nd time slot, data bit x_{n-1} is presented at the filter input and the accumulated sum will then be:

$$\sum_{k=0}^{31} \sum_{j=1}^{5} (x_{n-32j+k} + x_{n-321+32j-k})\, h_{32j-k}$$

or $$\sum_{j=1}^{160} (x_{n-i} + x_{n-321+i})\, h_i$$

Since $h_j = h_{321-i}$, this is equal to the convolution sum:

$$\sum_{i=1}^{320} (x_{n-i}\, h_i)$$

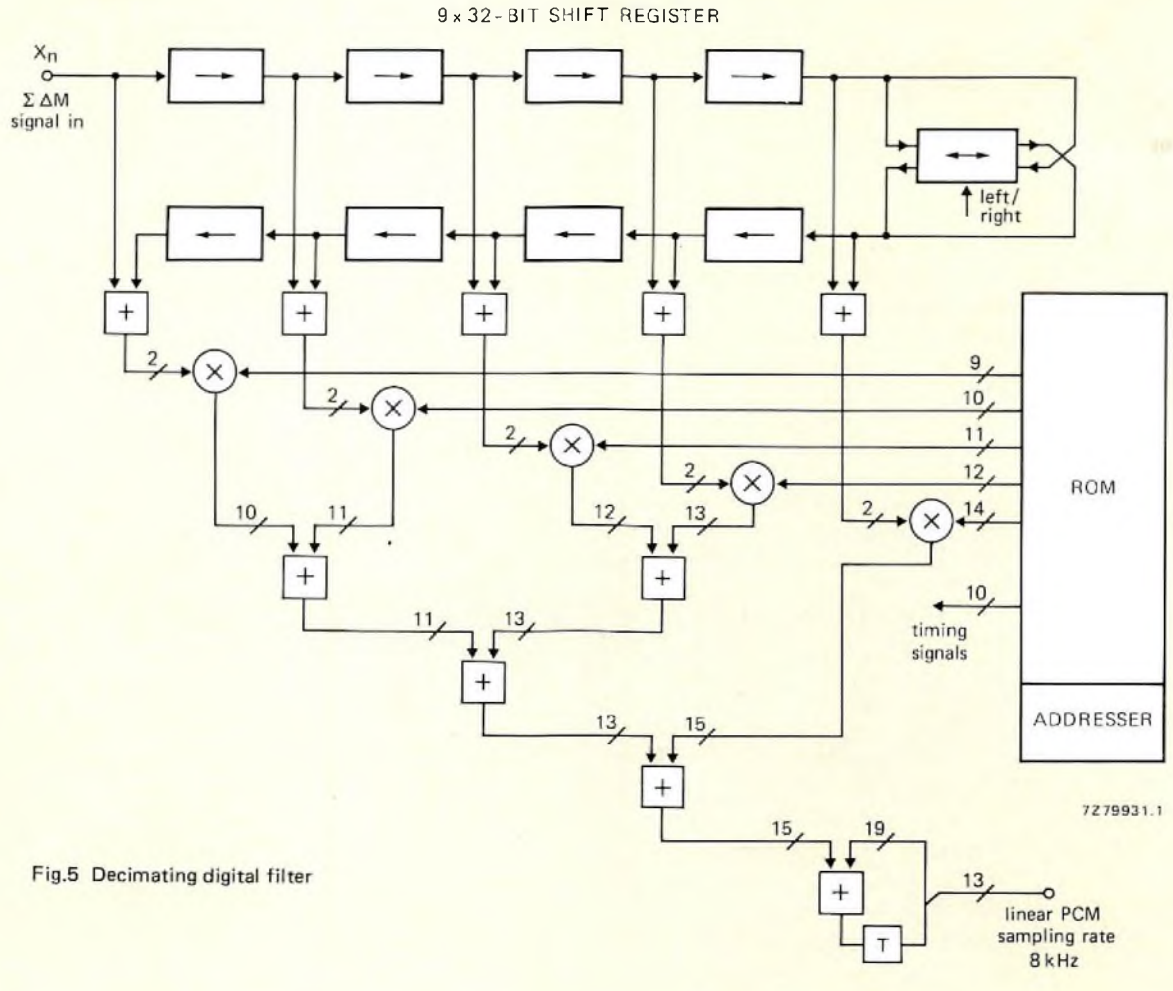


Fig.5 Decimating digital filter

The next data bit, x_n, is the first bit of the next 8 kHz cycle. The accumulator is reset after its rounded contents have been transferred to the compressor circuit formed by a simple combinatorial network followed by an 8-bit buffer. The sequential ROM addresser then selects h_{32}, h_{64}, h_{96}, h_{128} and h_{160} again.

A block diagram of the encoder is given in Fig.6.

THE DECODER

The digital filter

The 8 kHz PCM signal is expanded and convolved with an impulse response of length 40 at a sampling rate of 32 kHz so that all of the spectrum lobes of the input signal, except those that occur at multiples of 32 kHz, are suppressed. The sharp bandwidth limiting function is thus performed digitally and the remaining spurious components in the output signal only occur at frequencies above 28 kHz. These are suppressed by a simple second-order analog filter after the D to A conversion. All of the signal processing functions are included in one integrated digital circuit.

Operating principles

Ten compressed PCM samples are stored in eight recirculating 10-bit shift registers. The samples must be expanded and successively multiplied by four sets of ten coefficients to produce four samples in one 8 kHz cycle. A-law expansion and multiplication are performed simultaneously by using a data-shift and add technique described by Eggermont (Ref.10 and 11) and shown in Fig.7.

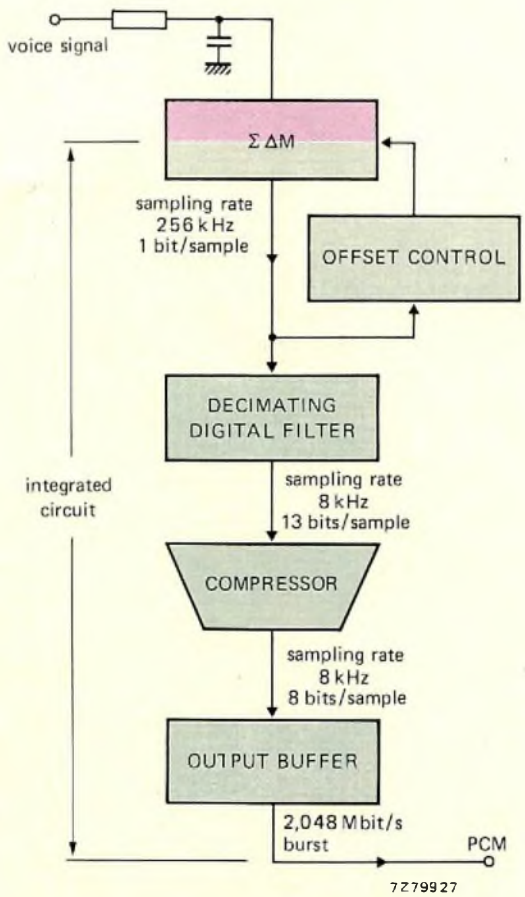


Fig.6 Block diagram of PCM encoder

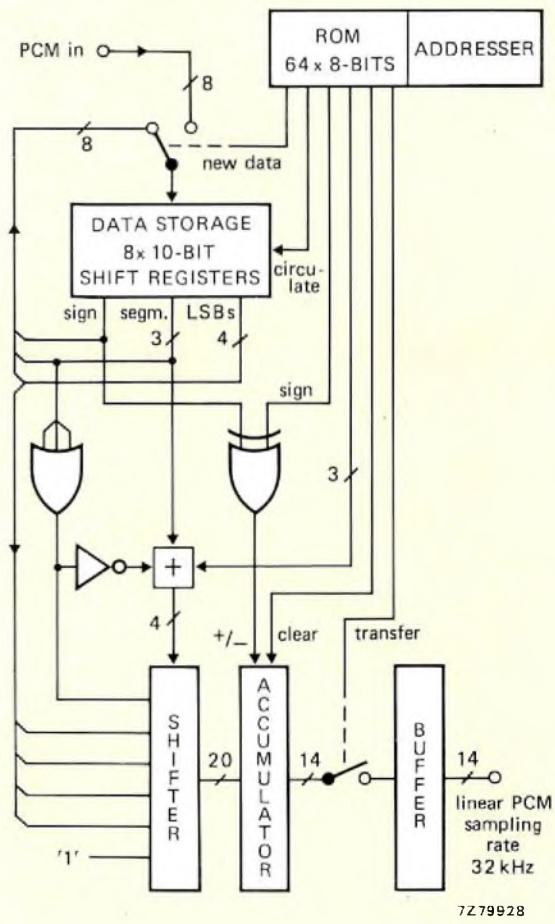


Fig.7 Expanding and interpolating digital filter

To perform the expansion (Fig.8), the four LSBs of the PCM data, preceeded by the OR-function of the three segment bits and followed by a '1', are shifted by the number of bit positions indicated by the segment bits.

Multiplication of the data by the filter coefficient is performed in a similar way (see Fig.9). The data is first shifted to the left by the number of bit positions corresponding to the position of the least-significant '1' in the coefficient. The resulting partial product is added to a second partial product obtained by shifting the data to the left by the number of bit positions corresponding to the position of the next '1' in the coefficient. This procedure is repeated to obtain the sum of the partial products for each '1' in the coefficient, i.e. the product of the data and the filter coefficient. As an example, if the data is to be multiplied by coefficient 101000, the first partial product is obtained by shifting the data three positions to the left. The second partial product is obtained by shifting the data five places to the left.

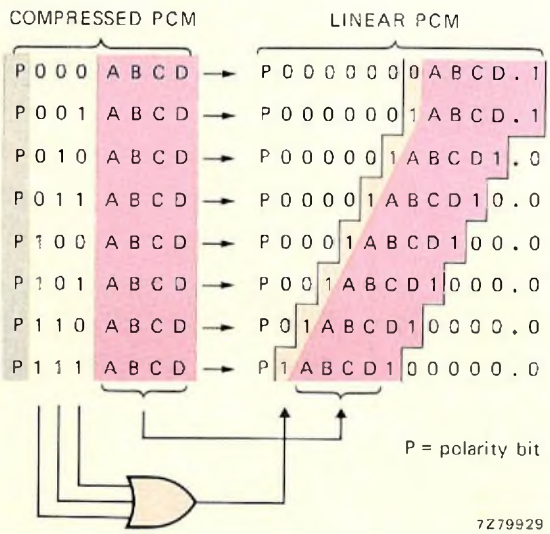


Fig.8 A-law expansion

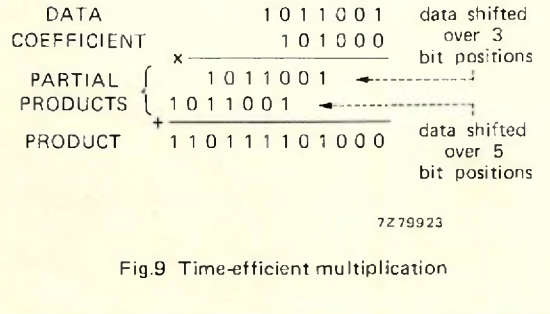


Fig.9 Time-efficient multiplication

These two partial products are then summed to obtain the product of the data and the filter coefficient. To perform this multiplication, the actual filter coefficient need not be stored. It is only necessary to store shift commands consisting of the binary-coded bit position of each '1' in the coefficient. In the previous example of a filter coefficient with a '1' in the third and fifth position, the binary-coded shift commands 3 and 5 would be stored. The sign bits of the data and the coefficient are modulo-2 added to determine the sign of the product. Simultaneous multiplication and expansion is achieved by simply adding the shift command to the three segment bits (except in the 000 case where the sum is increased by one).

To minimise the filter arithmetic, it is important that the filter coefficient set contains as few 1s as possible. We have succeeded in defining the required filter characteristic with a set of forty coefficients which contain a total of sixty-three 1s. The associated sixty-three shift commands, data circulate commands, accumulator clear and transfer signals are stored in a sequentially addressed ROM.

The D to A conversion via Sigma-Delta modulation

The objective is to convert the 32 kHz linear PCM signal back into a voice signal in such a way that a second-order analog post-filter is sufficient to suppress spurious out-of-band signals. It is not possible to use a digital version of the 256 kHz uniform Sigma-Delta modulator, as in the encoder, because its noise spectrum increases with a slope of 18 dB/octave above 4 kHz. Adequate suppression of this noise would require at least a fourth-order filter, which is just what we are trying to avoid. The only type of Sigma-Delta modulator which can be used to solve the problem is the single-integration type.

With a sampling rate of 512 kHz (the internal clock frequency of the integrated circuit), a single-integration Sigma-Delta modulator achieves a signal-to-in-band-noise ratio of approximately 55 dB (Ref.5 and 6).

For a second-order post-filter to have a linear response in the voice band, it must have a cut-off frequency of about 8 kHz. This increased noise bandwidth results in the maximum signal-to-noise ratio being reduced to about 45 dB.

We have combined a single integration Sigma-Delta modulator with a 7-bit linear DAC so that relatively low-resolution circuitry (Fig.10) can be used to obtain a high enough signal-to-noise ratio over the entire signal level range. The DAC comprises 128 equal value resistors connected as a stepping potentiometer with two taps bridging one of the resistors at each step. The stepping of the potentiometer is controlled by the seven MSBs of the linear PCM signal. The carry output from an accumu-

lator which integrates the seven LSBs of the linear PCM signal controls the duty cycle of a switch that selects one of the two taps. This duty cycle control signal can be considered to be the output of a digital Sigma-Delta modulator (Ref.12). This is explained as follows.

In the circuit of Fig.2, the loop-filter is replaced by a single integrator. Substituting the circuit elements with equivalent digital elements results in the encoder shown in Fig.11 for processing the N least significant bits of the linear PCM signal. Its action is described by:

$$d(n) = x(n) - q(n-1) + d(n-1)$$

The single-bit quantiser rounds the signal $d(n-1)$ to zero or 2^N because $x(n)$ ranges between zero and $2^N - 1$. In two's complement or offset binary notation, this can be done by simply taking the MSB of the signal $d(n-1)$.

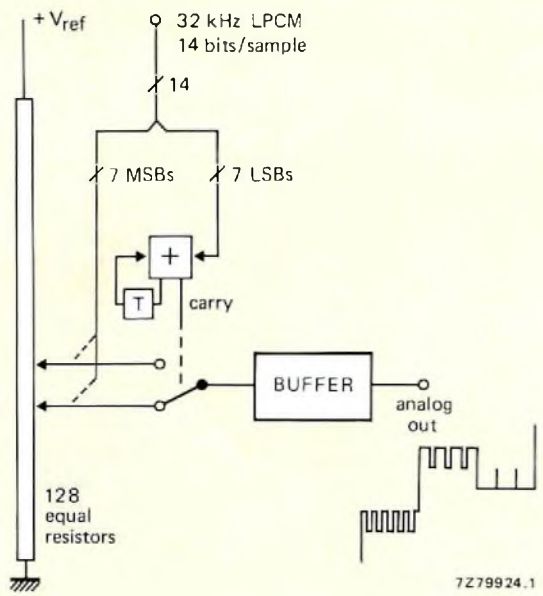


Fig.10 Sigma-Delta PCM coder and D to A converter

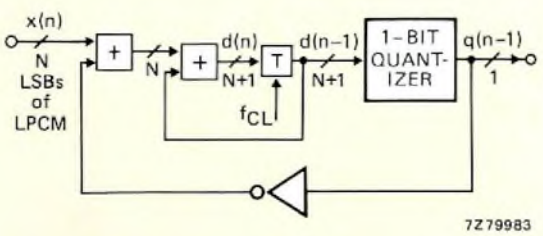


Fig.11 Digital single-integration Sigma-Delta modulator

Signal $d - q$ is then formed by the N least significant bits of signal d. Thus, q(n) is obtained by taking the MSB of the sum d(n) formed by the addition of x(n) and $d(n-1) - q(n-1)$. In the resulting circuit shown in Fig.12, output signal q(n) is the carry of the N-bit full adder. The selected quantising method results in an offset of $2^{N-1} - 2^{-1}$ but this can be eliminated in the DAC buffer.

With the combination of a straightforward linear DAC and a Sigma-Delta modulator, only the middle two quantising levels on the resistor chain are used for small signals. Only two of the DAC resistors need therefore be close tolerance types. For larger signals, more quantising levels are used but, since the signal-to-noise ratio requirements for these larger signals are less stringent, resistor matching is not so critical.

The spectrum of the reconstituted analog signal is shown in Fig.13. The hold effect (sin x/x) considerably decreases the 32 kHz spectrum lobe so that a second-order post-filter is sufficient to eliminate the remaining spurious signals and the out-of-band noise that increases with a slope of 6 dB/octave. The influence of the hold effect on the in-band ripple is compensated by the digital filter. A block diagram of the complete PCM decoder is given in Fig.14.

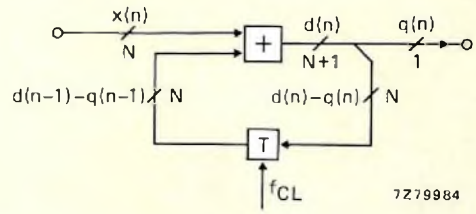


Fig.12 Rearrangement of the digital single-integration Sigma-Delta modulator

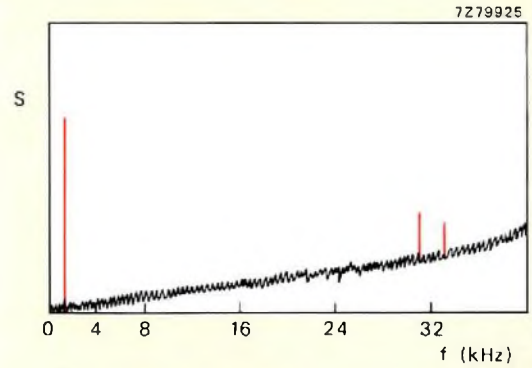


Fig.13 Spectrum at the output of the D to A converter for a 1 kHz sinewave

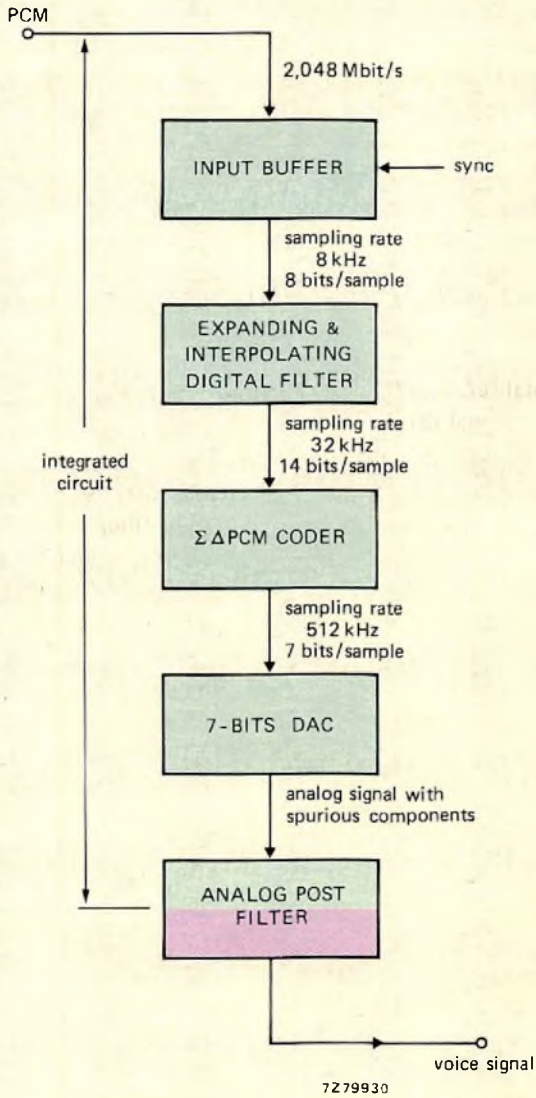


Fig.14 Block diagram of PCM decoder

BRIEF SPECIFICATION OF THE NEW CODEC

- CCITT G712 compatible, A-law compansion.
- Even-order bit inversion (ADI) included.
- PCM rate: 64 kbits/s or 2.048 Mbits/s burst.
- Linear-phase filters on-chip. The next version will have a choice of linear-phase or minimum-phase filters.
- Linear conversion output available from encoder.
- Power supplies ±5 V, ±5%, +12 V, ±5%.
- Power consumption: 200 mW max.
- Power-down option (10 mW max).
- Reference voltage: +5 V.
- Packaging: Cerdip or ceramic, 2 x 24 pins.
- Technology: NMOS.
- 4-phase dynamic design technique.
- 100% tested by special scan-test method.

TECHNOLOGY AND FUTURE DEVELOPMENTS

Most of the digital circuits of the codec such as data shift registers, ROMs, accumulators and D to A converter are repetitive structures that make the design eminently suitable for LSI. The present codec is implemented as two separate integrated circuits; an encoder and a decoder. Inexpensive NMOS technology has been used to achieve low cost. A 4-phase dynamic design technique minimises the power consumption. As soon as available technology allows, the entire codec with its associated filters will be integrated on a single chip. In the next version of the integrated codec, the linear-phase filter in the encoder will be replaced by a minimum phase filter. The filter in the decoder can be changed from linear-phase to minimum-phase by simply changing the ROM programming mask. Most of the present off-chip components, i.e. the comparator and the loop filter of the Sigma-Delta modulator in the encoder, and the analog post-filter of the decoder, will be integrated in a future generation of the codec.

ACKNOWLEDGEMENTS

The authors wish to thank their colleagues from the Philips Research Laboratory, particularly Mr. M. H. H. Höfelt on whose work this article is based. The assistance of Mr. L. F. Gee and his integrated circuit development group at Mullard in Southampton is also acknowledged.

REFERENCES

1. GOODMAN, D. J.: 'The application of Delta modulation to analog-to-PCM encoding', BSTJ, Vol. 48, 1969, pp. 321–343.
2. CANDY, J. C. and WOOLEY, B. A.: 'An A/D converter with segmented companding', Proc. Nat. Telecomms. Conf., Dec. 1974, pp. 388–391.
3. CANDY, J. C., CHING, Y. C. and ALEXANDER, D. S.: 'Using triangularly weighted interpolation to get 13-bit PCM from a Sigma-Delta modulator', IEEE Transactions on Communications, Nov. 1976, pp. 1268–1275.
4. MULDER, C., NIESSEN, C. and WIJNHOVEN, R. M. G.: Layout and Test Design of Synchronous LSI Circuits, ISSCC 1979 conference records, pp. 248–249.
5. de JAGER, F.: 'Delta modulation – a method of PCM transmission using the 1-unit code', Philips Research Report 7, 1952, pp. 442–466.
6. STEELE, R.: 'Delta modulation systems', Pentech Press, London 1975.
7. INOSE, H. and YASUDA, Y.: 'A unity-bit coding method by negative feedback', Proceedings IEEE, Vol. 51, Nov. 1963, pp. 1524–1535.
8. HÖFELT, M. H. H.: 'On the stability of a 1-bit quantized feedback system', ICASSP 1979 conference records, pp. 844–848.
9. JANSSEN, D. J. G. and v. d. MEEBERG, L.: 'Decimating linear phase digital FIR filter', Dutch patent application 7905332, 9th July 1979.
10. EGGERMONT, L. D. J.: 'Digital filter device for processing binary-coded signal samples', USA patent 3,988,606, October 26th, 1976.
11. EGGERMONT, L. D. J.: 'Arrangement for filtering of compressed pulse-code modulated signals', Dutch patent application 7800406, 13th, January 1978.
12. FLANAGAN, J. L.: 'Digital conversion from one PCM format to another', USA patent 3,772,682, November 13th, 1973.

Research news

UNCONVENTIONAL CUTS FOR QUARTZ RESONATORS

Quartz crystal resonators of many types are employed in electronic systems to provide and select desired stable frequencies. Uses range from clocks and counters, through communication systems and computers, to satellite and other navigation systems. Relatively simple devices are capable of accuracies of better than a few ppm which, for clocks, is equivalent to about one second in a week.

Work at the Philips Research Laboratories at Redhill in the UK and Cathodeon Crystals Ltd. (part of Cambridge Electronic Industries Ltd.) has shown that the stability of quartz resonators can be much improved by the use of plates cut from the quartz crystal at an orientation different from the one conventionally used.

The most important improvement obtained is the superior temperature stability of the new SC (strain compensated) cut compared with the AT cut normally used (Fig.1). A lower sensitivity to thermal and mechanical shock is also obtained. Two unexpected bonuses were found in further investigation of the properties of the SC cut: the new devices aged much more slowly and showed much higher Q values. A comparison of SC-cut properties with those of the AT-cut plates is given in Table 1. The penalties to be paid for this improved performance are only minor: it is harder to cut the

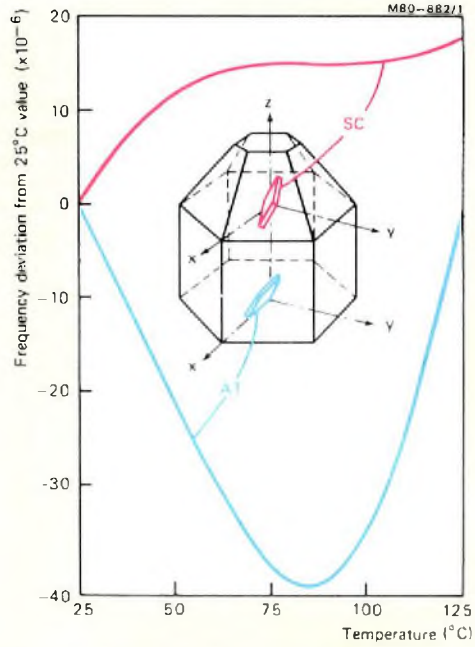


Fig.1 Frequency deviation from the 25°C value as a function of temperature for conventional AT-cut quartz crystals and the new SC device optimised to work at 85°C. For an SC device, any temperature between 75 and 95°C will give a frequency temperature coefficient between $\pm 0.02 \times 10^{-6}/°C$

TABLE 1

Comparison of SC-cut frequency stabiliser quartz plates with conventional AT-cut plates

	SC-cut	AT-cut
Frequency change with temperature in the range 70 to 100°C	$\pm 0.2 \times 10^{-6}$	$\pm 2 \times 10^{-6}$
Sensitivity to bending forces equivalent to 100 times the plate weight	0.02×10^{-6}	0.25×10^{-6}
Sensitivity to 0.2°C temperature pulses	0.01×10^{-6}	0.2×10^{-6}
Ageing	0.002×10^{-6}/day	0.005×10^{-6}/day
Q factor	0.4×10^{6}	0.2×10^{6}

quartz at the correct angles, and marginally more-complex circuits are needed to suppress an unwanted vibration mode at a frequency 11% above that of the temperature-stable one.

The results described here have been obtained in investigations partly funded by the British Government.

IMPROVEMENTS IN MOBILE RADIO COMMUNICATION

The increase in the use of mobile radio has caused considerable crowding in the frequency allocation given to radio communication, and there is a constant search for equipment that would use the available bandwidth more efficiently. Three recent developments from the Philips Research Laboratories, Redhill, UK, have all contributed to this objective. The developments include a single-sideband modulation system for mobile radio at v.h.f. frequencies, a frequency synthesiser circuit, and an investigation of channel congestion in trunked radio systems. The single-sideband and trunking systems can be used separately or together, but both require the synthesiser.

Single-sideband for v.h.f.

The new system is a development of the 'Pilot Signal' technique, originally used in h.f. single-sideband radio for frequency stabilisation, and uses a pilot carrier of less than one-tenth the peak speech power. This pilot carrier is used both as a frequency reference, to recover the audio signal from the radio signal, and as a constant-strength reference to compensate for variations in signal strength. The use of single-sideband for v.h.f. and u.h.f. mobile radios has reduced the required bandwidth per communication channel from 25 or 12.5 kHz to 5 kHz, thus more than doubling the number of channels potentially available.

Universal frequency synthesiser

The high frequency stability, and multi-channel operation, needed for single-sideband mobile radio at v.h.f. is easily and economically achieved by the universal frequency synthesiser circuit, also developed at Redhill (see Ref.1). In this system, the output frequency of a voltage controlled oscillator is divided by a variable number in a divider circuit. The output of this divider circuit is compared with a reference frequency from a fixed quartz-stabilised oscillator using a phase comparator, and the d.c. error signal from the phase comparator is then used to control the original oscillator. A lowpass filter is needed to avoid frequency modulation of the

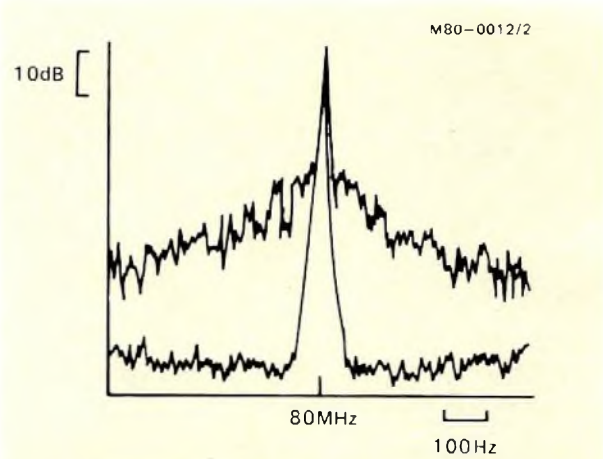


Fig.2 Frequency spectra for synthesiser circuits incorporating new (lower trace) and conventional (upper trace) phase comparators

oscillator by spurious signals from the phase comparator, and to be effective, the cut-off frequency of this filter must normally be about a hundred times lower than the reference frequency. This can result in reaction times of the order of seconds. However, the Philips Laboratories have now designed a new phase comparator which allows less stringent filtering, as well as a considerable reduction of noise in the feedback loop. This results in a fast-response circuit, with excellent frequency purity and stability (see Fig.2).

Channel sharing

The trunking of radio channels, for sharing by many users, is a further development made possible by the frequency synthesiser. Such systems are likely to become essential in the near future.

A trunked radio system differs from a telephone network in that the number of users will be smaller and the amount of traffic generated by each user more variable. An analysis of such 'unbalanced' systems made at Redhill shows that the unbalance results in a system operating more efficiently than predicted by the telephone theory for balanced systems. For the same waiting time, the difference in efficiency can be up to 50%. The first experimental model of the trunking scheme is currently being developed at Redhill, and is due to come into operation during 1980.

REFERENCE

1. GILES, T.G., 'Versatile LSI frequency synthesiser circuit', Electronic Components and Applications, Vol.2, No.2, February 1980, pp.91 to 105.

Publications news

Solid aluminium capacitors

This 20-page publication describes the results of the various reliability and stability tests carried out on samples from our 121 range of solid-state aluminium capacitors over the period 1971 to 1977. The structure of the 121 range is briefly described, and some definitions used in quality control are listed. The results of the tests are presented, and it is shown that in life tests totalling 77.4 million component hours, only one catastrophic and one degradation failure were observed.

Integrated AM radio TDA1072

This 6-page Technical Note describes the TDA1072, an IC designed to perform all the active functions between the aerial and the audio power amplifier of an a.m. radio. The main features of the IC are listed, and the peripheral circuit required for the i.f. and audio sections described. Circuits are given showing the use of the TDA1072 in a permeability-tuned medium-wave car radio, a variable-capacitor tuned medium-wave domestic radio, and a medium-wave domestic radio tuned by variable-capacitance diodes.

Industrial Microcomputer System

A 16-page guide to our Industrial Microcomputer System (IMS). This system has been developed specifically to simplify the problems of implementing microcomputer systems and is based on the Signetics 2650 microprocessor. The complete system consists of a number of separate functional modules, each on a single (160 × 100 mm) Eurocard. To facilitate software development, IMS has a low-cost microcomputer development system called MODEST, which formed the starting point of the IMS design. The guide lists the features of each of the modules, and gives a full description of the MODEST software facilities.

Hi-Bri colour picture tube with pigmented phosphors

The phosphor-keyed filtering of reflected light improves the performance of the Hi-Bri picture tube. Contrast is increased by 20%, colour rendition is enhanced, and the albedo of the screen is reduced. This 2-page Technical Note outlines the principles of pigmented Hi-Bri, and compares the performance of the pigment enhanced Hi-Bri tube with a conventional tube, and the Hi-Bri tube without pigment enhancement.

Whiskerless diodes – quality control and reliability

A revised guide giving the latest quality and reliability results for our range of whiskerless diodes. The structure of the diode is briefly described, together with the various stages of product development and testing. The 26-page publication gives diode parameter spreads derived from quality control tests carried out between 1971 and 1978, and environmental and life test results for the period 1974 to 1978. The maximum failure rate observed in over 4.5×10^{10} device-hours of diode operation was 0.6×10^{-9}/h.

Low-cost remote sensing radiometer using the RPY89 infrared detector

This 8-page Technical Note describes a remote sensing radiometer which is ideal for monitoring temperature over a relatively large area. Temperature control in microwave ovens would be a typical application. It is a low-cost design which does not need expensive optical components or detector elements. The radiometer uses a null technique in which radiation from a defined area of the target is balanced against an internal reference source. The operation and design of the system are described in detail, and the note concludes with a full description of the performance of the system.

Copies of the publications mentioned can be obtained upon written application either to the publications department of one of the companies listed on the back cover or to the Editor, stating the nature of the applicant's interest.

Abstracts

Gate turn-off switch

The gate turn-off switch (GTO) combines the high blocking voltage and high switching current of the thyristor with the ease of gate drive and speed of the transistor. This article describes the BTW58 series GTO and compares it with other fast switches. A number of possible application areas are suggested.

Development of digital filters using the 8X300 microprocessor

Digital filters are an attractive alternative to their analogue counterparts. They can be exhaustively analysed and changes can be easily made to filter parameters. This article describes a digital filter development system using the 8X300 microprocessor with the 8X300 Development and Monitoring System. Filter coefficients and data are stored in a 64-word X 16-bit memory. Reading/writing, multiplication and addition of coefficients are described. The article concludes with a simple filter example.

LSI circuit for AC motor speed control

The disadvantages of Pulse Width Modulation (PWM) speed control systems for a.c. motors have now been overcome by the development of a purpose-designed LSI circuit for signal generation. This article describes the internal organisation of the circuit. There is a full description of the various input/output facilities, and detailed user advice is given. The article is the third in a series describing our PWM speed control system.

Monolithic 14-bit digital-to-analogue converter with 85 dB S/N ratio

Sound recording and reproduction systems that use digital signal processing impose stringent requirements on the performance of the digital-to-analogue converters (DACs). Many of these systems demand 16-bit converters to obtain acceptable S/N ratio and linearity. A new method of current division called dynamic element matching is used in the TDA1540 DAC to achieve a S/N ratio of 85 dB for audio signals, sampled at 44 kHz, in a 14-bit converter. Dynamic element matching eliminates trimming. The TDA1540 is monotonic over the temperature range −25 to +70 °C and requires no deglitching circuit.

PCM codec with on-chip digital filters

A new approach to the design of a single-channel PCM codec eliminates the need for high-resolution quantising and simplifies the transfer function requirements for the anti-aliasing analogue filters. The need for accurate quantising is overcome by using Sigma-Delta modulation as an intermediate code. The high sampling rate then allows low-performance anti-aliasing analogue filters to be used. Digital code converters recode the Sigma-Delta bit-stream into standard PCM and vice-versa. The sharp band-limiting function at 3.4 kHz is performed by non-recursive digital filters which have well-proved long-term stability and can be more easily tested than complex (sampled) analogue filters.

Abschaltthyristoren

Der über die Steuerelektrode abschaltbare Thyristor vereinigt die hohe Spannungsfestigkeit und Strombelastbarkeit des Thyristors mit der einfachen Steuerbarkeit und hohen Schaltgeschwindigkeit des Transistors. Dieser Artikel beschreibt die Abschaltthyristoren der Reihe BTW58 und vergleicht sie mit anderen schnellen Schaltern. Eine Anzahl möglicher Anwendungsbereiche wird vorgeschlagen.

Entwicklung von digitalen Filtern mit dem Mikroprozessor 8X300

Digitale Filter sind eine attraktive Alternative zu ihren analogen Gegenstücken: sie lassen sich erschöpfend analysieren, und Filterparameter können leicht geändert werden. Dieser Beitrag beschreibt ein System zur entwicklung digitaler Filter, das den Mikroprozessor 8X300 in Verbindung mit dem 8X300-Entwicklungssystem DMS benutzt. Filterkoeffizienten und Daten werden dabei in einem 64 Worte X 16 bit-Speicher aufbewahrt. Lesen/Schreiben, Multiplikation und Addition von Koeffizienten werden beschrieben. Der Beitrag schliesst mit einem einfachen Filterbeispiel ab.

LSI – Schaltung für Drehzahlregelung von Wechselstrommotoren

Die Nachteile der Drehzahlregelung von Wechselstrommotoren durch Pulsbreiten-Modulation sind jetzt durch die Entwicklung einer speziellen LSI-Schaltung zur Signalerzeugung überwunden worden. Der Artikel beschäftigt sich mit dem Aufbau dieser Schaltung. Die Ein- und Ausgabeeinheiten der Schaltung werden vollständig beschrieben und ausführliche Hinweise für den Anwender gegeben. Dieser Artikel ist der dritte in einer Serie, die Drehzahlregelung durch Pulsbreiten-Modulation behandelt.

Monolithischer 14 bit-Digital/Analog-Konverter mit 85 dB Rauschabstand (S/N)

Ton-Aufnahme-und Wiedergabesysteme, die digitale Signal-verarbeitung verwenden, stellen strenge Anforderungen an die Eigenschaften von Digital/Analog-Konvertern. Viele dieser Systeme benötigen 16 bit-Konverter, um einen akzeptablen Rauschabstand und genügend hohe Linearität zu erzielen. In der integrierten Schaltung TDA1540 wird eine neue Methode der Stromteilung angewandt, die als "dynamic element matching" bezeichnet wird. Hiermit wird bei Tonsignalen, die mit 44 kHz abgetastet werden in einem 14 bit-Konverter ein Rauschabstand (S/N) von 85 dB erreicht. Die neue Stromteilungsmethode ermöglicht es, ohne jeden Abgleich auszukommen. Die Schaltung TDA1540 verhält sich im Temperaturbereich von −25 bis +70 °C monoton und benötigt keine Schaltung zur Unterdrückung laufzeitbedingter Störimpulse.

PCM-Codern/Decodern mit digitalen Filtern auf dem Chip

Mit einer neuen Methode ist es beim Entwurf von Einkanal-PCM-Codern/Decodern jetzt möglich, eine hochauflösende Quantisierung zu vermeiden und die Anforderungen an die Übertragungsfunktion des Analogfilters herabzusetzen. Die Notwendigkeit einer hochauflösenden Quantisierung wird dabei durch Verwendung einer Sigma-Delta-Modulation als Zwischencode beseitigt und die hohe Abtastrate ermöglicht dann den Einsatz von einfachen Analogfiltern. Digitale Code-Konverter setzen den Sigma-Delta-Bitstrom in ein Standard PCM-Signal um und umgekehrt. Die scharfe Bandbegrenzung bei 3,4 kHz wird durch nichtrecursive Digitalfilter erreicht, die eine gute Langzeitstabilität besitzen und leichter als komplizierte getastete Analogfilter geprüft werden können.

Commutateur à grille de contrôle à semiconducteurs

Ce commutateur à grille de contrôle (GTO) associe la haute tension de blocage et le courant de commutation élevé du thyristor à la commodité de commande de grille et à la rapidité du transistor. Cet article décrit le commutateur à grille de contrôle de la séries BTW58 et le compare à d'autres commutateurs rapides. Diverses applications possibles sont suggérées.

Développement de filtres digitaux à l'aide du microprocesseur 8X300

Les filtres digitaux sont susceptibles de remplacer avantageusement leurs homologues analogiques. Ils peuvent être analysés complèment et leurs paramètres peuvent être aisément modifiés. Cet article décrit un système de développement de filtre digital à l'aide du microprocesseur 8X300 et du Système de Développement et de Surveillance 8X300. Les coefficients et les données du filtre sont enregistrés dans une mémoire de 64 mots X 16 bits. Les processus de lecture/écriture, multiplication et addition de coefficients sont décrits. L'article se termine par l'exemple d'un filtre simple.

Circuit LSI pour régulation de vitesse de moteurs alternatifs

Les inconvénients des dispositifs de régulation de vitesse des moteurs alternatifs à modulation par impulsions de durée variable (PWM) viennent d'être surmontés par la mise au point d'un circuit LSI spécial pour la génération de signaux. L'article décrit l'organisation interne du circuit. Il contient une description complète des divers dispositifs d'entrée/sortie et donne des recommandations détaillées à l'intention de l'utilisateur. C'est le troisième d'une série consacrée à notre dispositif de régulation de vitesse PWM.

Convertisseur digital-analogique monolithique 14 bits à rapport signal/bruit de 85 dB.

Les systèmes d'enregistrement et de reproduction du son qui font appel au traitement digital de signaux exigent des convertisseurs digitaux-analogiques des performances particulièrement élevées. Nombre de ces dispositifs nécessitent l'emploi de convertisseurs 16 bits pour obtenir un rapport signal/bruit et une linéarité acceptables. Une nouvelle méthode de division du courant, appelée "dynamic element matching", est utilisée dans le convertisseur digital-analogique TDA1540 pour obtenir un rapport signal/bruit de 85 dB pour les signaux audio, échantillonnés à 44 kHz, dans un convertisseur 14 bits. Le "Dynamic element matching" rend inutile le réglage de capacité. Le TDA1540 est monotonique dans la gamme de température −25 à +70 °C et n'a pas besoin de circuit anti-parasites.

Codeur décodeur à modulation par impulsion codées avec filtres digitaux sur microplaquette unique.

Une nouvelle méthode d'étude d'un codeur décodeur monovoie á modulation par impulsions codées évite la nécessité d'une quantification à haute résolution et simplifie les spécifications de la fonction de transfert pour les filtres analogiques anti-erreurs d'identification ("aliasing"). La nécessité d'une quantification précise est évitée par l'emploi de la modulation Sigma-Delta comme code intermédiaire. La fréquence d'échantillonnage élevée permet alors l'emploi de filtres analogiques anti-erreurs d'identification à basses performances. Des convertisseurs de code digital recodent le flot de bits Sigma-Delta en modulation par impulsions codées standard et vice-versa. La fonction de limitation de bande à 3,4 kHz est assurée par des filtres digitaux non-récursifs, qui ont une stabilité à long terme éprouvée et peuvent être testés plus facilement que des filtres analogiques (échantillonnés) complexes.

Conmutador de semiconductor controlado por puerta

El conmutador controlado por puerta (GTO) combina la elevada tensión de bloqueo y la elevada corriente de conmutación del tiristor con la facilidad de control por puerta y rapidez de conmutación del transistor. Este breve artículo describe el conmutador controlado por puerta de la serie BTW58 y lo compara con otros conmutadores rápidos. Se sugieren algunas de las áreas de aplicación posibles.

Desarrollo de filtros digitales con el microprocesador 8X300

Los filtros digitales son una atractiva alternativa con respecto a sus contrapartidas analógicas. Estos pueden ser analizados exhaustivamente y se pueden realizar fácilmente cambios en los parámetros del filtro. Este artículo describe un sistema de desarrollo de filtro digital que utiliza el microprocesador 8X300. Los coeficientes del filtro y los datos son almacenados en una memoria de 64 palabras X 16 bits. Se describen las operaciones de lectura/escritura, multiplicación y suma de coeficientes. El artículo concluye con un ejemplo sencillo de filtro.

Circuito LSI para control de velocidad de motores de C.A.

Las desventajas de los sistemas de control de velocidad por modulación de anchura de impulsos (PWM) para motores de corriente alterna han sido eliminadas ahora con el desarrollo de un circuito LSI diseñado a propósito para generación de señal. Este artículo describe la organización del circuito. Se dá una descripción detallada de las diversas posibilidades de entrada/salida y algunos consejos detallados al usuario. Este artículo es el tercero de una serie que describe nuestro sistema de control de velocidad por modulación de anchura de impulsos.

Convertidor digital-analógico monolitico de 14 bits con una relación señal/ruido de 85 dB

Los sistemas de grabación y reproducción de sonido que utilizan un proceso digital de señal, imponen severas exigencias a las características de los convertidores digital-analógico (CDA). Muchos de estos sistemas necesitan convertidores de 16 bits para obtener una linealidad y una relación señal-sonido aceptables. En el convertidor digital-analógico TDA1540 se utiliza un nuevo método de división de corriente, llamado adaptación dinámica del elemento, con lo que se consigue una relación señal/ruido de 85 dB para señales de audio, muestreada a 44 KHz, en un convertidor de 14 bits. La adaptación dinámica del elemento elimina el ajuste. El TDA1540 es monotónico en el margen de temperatura de 25 a 70 ° C y no necesita circuito de supresión de áleas.

Codigo PCM con filtro digital

Una nueva aproximación al diseño de un sistema de codificación PCM de un canal elimina la necesidad de cuotificación de alta resolución y simplifica los requisitos de la función de transferencia de filtros analógicos. La necesidad de una cuantificación precisa se evita utilizando modulación sigma - delta como código intermedio. La elevada velocidad de muestreo permite por lo tanto el uso de filtros analógicos sencillos. Los convertidores digitales de código pasan el grupo de bits codificado en sigma - delta a un código estandar PCM y viceversa. La limitación de banda con una brusca caida a 3.4 MHz se realiza mediante filtros digitales no recursivos que tienen buena estabilidad a largo plazo y se pueden probar más facilmente que los filtros analógicos complejos.

Authors

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