Electronic components & applications

Vol. 2, No. 2
February 1980

incorporating Philips Electronic Applications Bulletin and Mullard Technical Communications

ISSN 0141–6219

Electronic components & applications

Volume 2, No. 2 February 1980

Contents

Electrical safety requirements in hazardous environments such as this off-shore oil rig are particularly severe. The advent of electronic speed control systems for asynchronous motors, as described in the article beginning on page 66, not only provides a prime mover setting new standards of safety, it also contributes to more efficient use of our diminishing energy resources.

Photo courtesy Smit International Rotterdam

Introduction to PWM speed control system for 3-phase AC motors

J. A. HOULDSWORTH and W. B. ROSINK

The majority of industrial drives use electric motors, since they are controllable and readily available. In practice, most of these drives are based on a.c. induction motors because such motors are rugged, reliable, and relatively inexpensive.

To control the speed of a drive many methods have been developed, ranging from mechanical and hydraulic systems to electrical and electronic systems using, for example, d.c. shunt-wound motors whose speed can be controlled directly. However, it has been the desire of drive system manufacturers to vary the speed of the standard three-phase induction (asynchronous) motor by electrical means. This aim has been technically possible for some years, and with recent advances in power electronic components and integrated circuits it is now achievable with both cost and quality comparable to that of alternative systems.

This article begins by considering the development of the most common currently available electronic systems by examining two approaches to the control of d.c. motors: phase (or line) control, and chopper (switched mode) control. Then, the characteristics of the three-phase induction motor are discussed, establishing the dependence of motor speed on frequency, and the need to control both frequency and voltage for a proper method of control. This is achieved by using a three-phase inverter to convert the mains frequency to a variable frequency and voltage supply to the motor. The main features of the various types of inverter currently available are then considered. These systems have certain shortcomings, and in this article we describe a new improved system using Pulse-Width Modulation (PWM) techniques. We have developed a purpose-designed Large Scale Integrated (LSI) circuit specifically for this application.

GENERAL INTRODUCTION TO MOTOR SPEED CONTROL

Traditionally, d.c. motor control using Ward-Leonard sets required the use of three electrical machines: a three-phase induction motor, a d.c. generator, and a d.c. motor. This can now be replaced by a double six-thyristor bridge employing only one electric machine, the d.c. motor. Changing from electromechanical control systems to electronic control systems generally provides a reduction in complexity, savings in cost, space, and response time, and gains in efficiency.

Phase control of d.c. motors

Figure 1 shows a typical d.c. motor controller using a bridge circuit of six thyristors fed from the three-phase mains supply. Motor voltage control is achieved by varying the phase angle at which the thyristors are fired relative to the incoming mains voltage supply waveform. This provides an output voltage ranging from zero to a value equal to that provided by a full-wave diode rectifying bridge. Such a circuit is typically used in the control of d.c. shunt motors (d.c. motors with separate field excitation).

Phase controlled rectifier circuits, like that shown in Fig.1, are the simplest form of electronic motor control because the thyristors are naturally "mains-commutated" or "line-commutated" from the three-phase a.c. source. In this case, the commutation process consists of a cyclic transfer of current from one pair of conducting thyristors to the next. The three thyristors in the upper group (Th_1, Th_3, and Th_5) have a common cathode terminal, and conduction is via the thyristor with the most positive anode voltage. The other two thyristors are reverse-biased relative to the common cathode terminal. Similarly, the

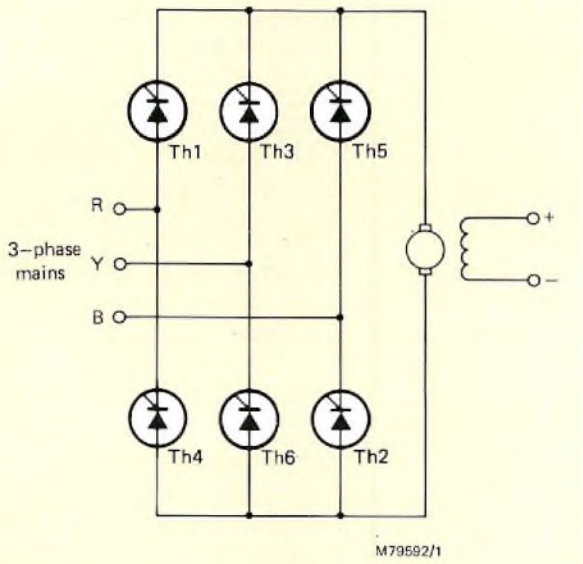


Fig.1 Basic 6-thyristor phase-control circuit for d.c. motor

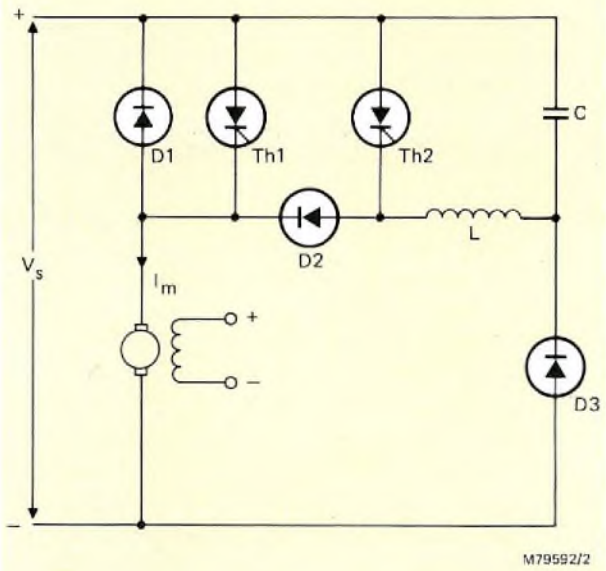


Fig.2 Basic chopper circuit for d.c. motor

thyristors in the lower group (Th_4, Th_6, and Th_2) have a common anode connection, and conduction is via the thyristor with the most negative cathode. For a phase sequence R, Y, B, the thyristors conduct in pairs: Th_1 and Th_2; Th_2 and Th_3; Th_3 and Th_4; Th_4 and Th_5; Th_5 and Th_6; they are consequently numbered in their correct firing sequence in Fig.1.

All phase control systems use line commutation which imposes a controller bandwidth limited by the mains supply frequency, and for improved performance other systems are required.

Chopper control of d.c. motor

The limitations of phase control may be overcome by using chopper control. The principle of chopper control can be illustrated by considering the speed control of a d.c. shunt motor from a rectified a.c. supply or d.c. supply source. The motor average voltage is controlled by varying the on-to-off time ratio for which the d.c. supply voltage is applied to the load, and thyristor turn-off is now achieved by forced commutation. Forced commutation, as the name implies, "forces" the thyristor to turn-off by using an auxiliary circuit (the commutation circuit) consisting for example of an auxiliary or commutation thyristor and a series resonant LC circuit.

The mechanism of varying the on-off time by "chopping" the input voltage into discrete pulses gives this type of control its name. Thus, by varying the width of the pulses, or the repetition frequency of the switching period, the average value of the d.c. output voltage can be varied from a very small value to almost the voltage of the supply source.

An example of a basic chopper circuit is shown in Fig.2. The motor current is labelled I_m. Thyristor Th_1 is the main thyristor and Th_2 the commutation thyristor which is used to turn off the main thyristor Th_1 with the aid of the series-resonant LC circuit. When Th_1 is switched off, the motor current I_m can flow via the diode D_3, the inductance L, and the diode D_2. The diode D_3 is therefore known as the 'flywheel diode'. The operation of the commutation circuit is described in detail later in this article.

The a.c. motor

The majority of industrial drives are powered by three-phase a.c. induction motors. The wide application of these motors is a direct consequence of their inherent advantages when compared with other types. These advantages include:

- High reliability with low maintenance costs.
- Low cost: for a given output power a d.c. motor can cost several times as much as its a.c. equivalent.
- High output power to volume and weight ratios.
- The speed is relatively independent of the load for a given supply frequency.
- Brushless construction: this makes it particularly suitable for use in hazardous environments such as mining and petrochemical industries.
- Standard versions are readily available from stock.

The standard three-phase induction motor is essentially a single-speed machine when supplied from mains of

fixed voltage and fixed frequency. If f is the frequency of the mains supply and p is the number of pole-pairs in the stator, then the speed of rotation of the stator field (the synchronous speed) is given by:

$$N_s = \frac{f}{p} \times 60 \text{ rev/min.}$$

By changing the number of pole-pairs of the motor, the motor can be made to operate at a number of fixed speeds. For continuously variable speed control, however, the supply frequency must be varied; the applied voltage must also be varied in linear proportion to the supply frequency to maintain constant motor flux. At low frequencies, where the motor inductive reactance is low, boosted voltage may be used to compensate for the stator 'IR' voltage drop. Thus control of both frequency and voltage is necessary for proper variable-speed operation. Under normal operating conditions, the rotor (motor shaft) speed is a few per cent less than the synchronous speed. The difference between the two speeds is called slip.

Figure 3 illustrates the induction motor torque-speed characteristics under nominal rated voltage V_1 and reduced voltage V_2 together with typical fan and industrial machine tool loads (superimposed). It can be shown that smooth speed control depends on the slope of both the motor torque curve and the speed torque curve. Thus constant-frequency variable-voltage operation is suitable only for "square law" loads such as fans or pumps to ensure proper starting and stable running conditions. Systems using speed control by variable voltage are not suitable for use with constant-torque loads, and, when used with fan or pump loads, efficiency is poor. To overcome these limitations it is necessary to provide a variable-frequency variable-voltage supply to the motor, and this requires the use of some type of inverter circuit.

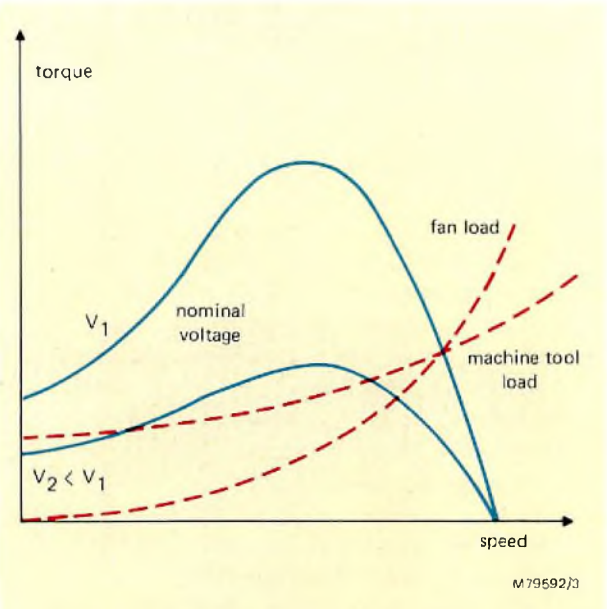


Fig.3 Induction motor torque-speed characteristics

INVERTERS FOR A.C. MOTORS

There are two basic types of inverter for use with variable-frequency and variable-voltage speed control systems for three-phase a.c. motors: the current-source type and the voltage-source type.

The current-source inverter

A block diagram of a current-source inverter is shown in Fig.4. It consists of either a phase-controlled rectifier circuit, or rectifier-chopper circuit, followed by a choke to provide a constant-current source for the inverter. The inverter thyristors are force-commutated to transfer the current between phases. Since the inverter is supplied from a current source, it is protected from transient current surges arising from rapid load variations.

In theory, the current-source inverter makes possible an economical inverter design in which the thyristors are fully utilised during normal operation. However, it cannot be used for the control of two or more motors in parallel, and motors exhibit pulsating torques at low frequencies. Because of these restrictions, current-source inverters are therefore only of limited application.

The voltage-source inverter

Because of the limitations of the current-source inverter, the voltage-source inverter is the most commonly used type. The simplest form of this is the quasi-square-wave inverter, or 'six-pulse inverter'.

Quasi-square-wave control of a.c. motors

In the quasi-square-wave inverter system, each of the three inverter outputs is switched every half-period between the plus and minus terminal of the fixed d.c. supply source as in Fig.5. This produces the output waveforms of Fig.6. The half-period average line output voltage is given by $V_{(R-Y)av} = V_s \times 2/3$, where V_s equals the d.c. supply voltage. However, the a.c. motor requires an average voltage proportional to frequency, and this variation of the output voltage with frequency requires the use of an additional chopper circuit.

Pulsed quasi-square-wave source inverter

The need for this extra circuitry can be overcome by the pulsed quasi-square-wave system. The output of this system is shown in Fig.7. Each of the three inverter outputs supply the motor with n output pulses, ampli-

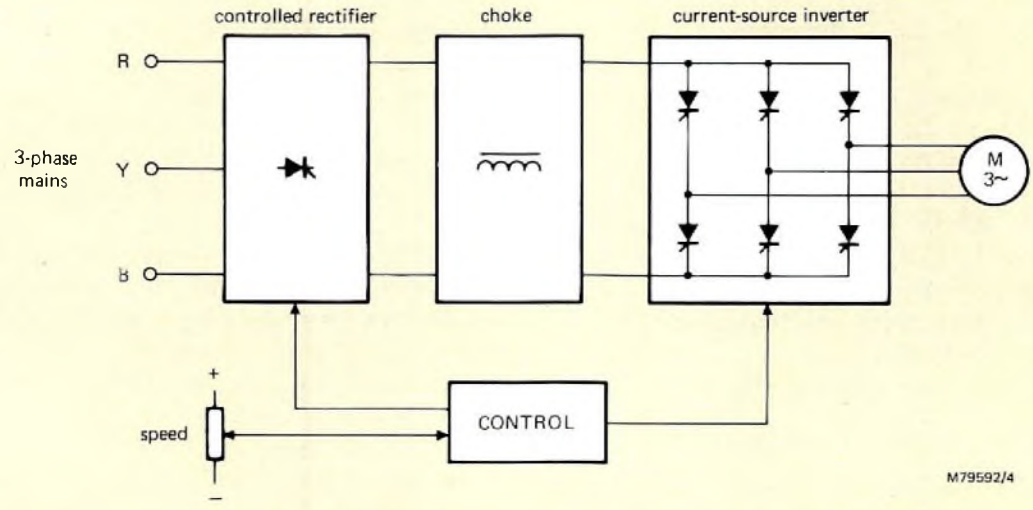


Fig.4 Variable-frequency current-source inverter system

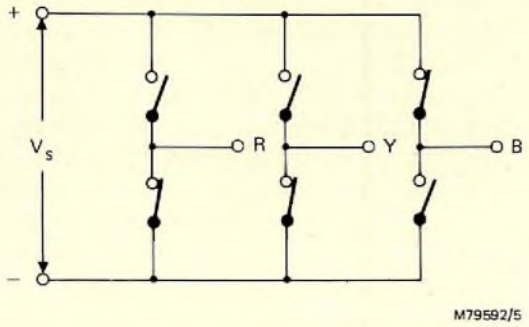


Fig.5 Voltage-source inverter

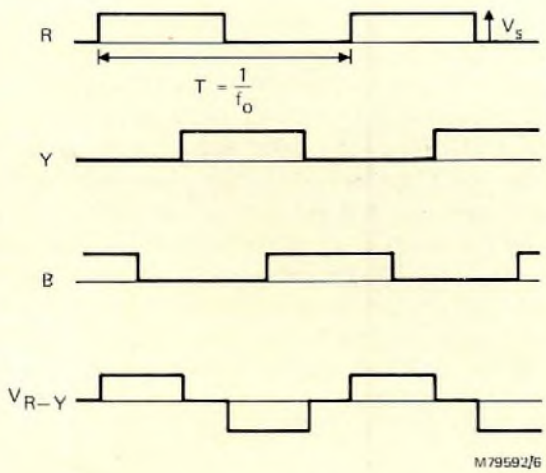


Fig.6 Quasi-square waveforms

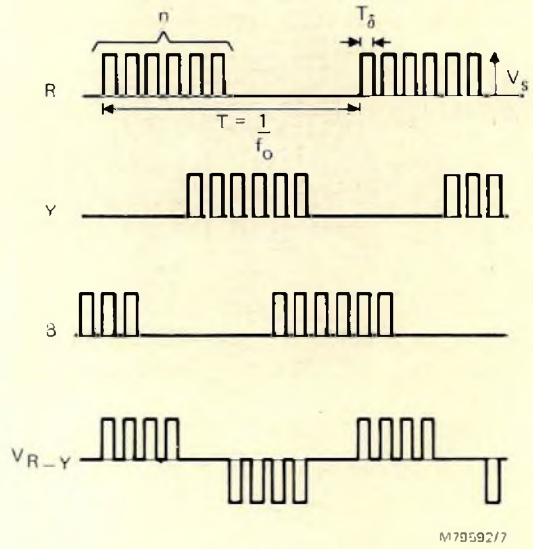


Fig.7 Pulsed quasi-square waveforms

tude V_s, pulse-width T_δ, during each half-period.

The average line output voltage for half a period is given by:

$$V_{(R-Y)av} = V_s \times n \times \frac{2}{3} \times T_\delta \times \frac{2}{T},$$

$$= V_s \times \frac{4n}{3} \times T_\delta \times f_o.$$

The output voltage $V_{(R-Y)av}$ is therefore proportional to the motor drive frequency f_o, assuming V_s, n, and T_δ are fixed, and so the induction over the whole speed range is constant. However, for a fixed number of pulses per cycle, system performance is limited at high speeds

by the high inverter switching frequency required, and at low speeds by the pulsating torques produced.

The performance of the pulsed quasi-square-wave system can be considerably improved by increasing the number of pulses per half-period as the motor speed decreases. The pulse-width T_δ has to be decreased at the same time so that the total half-period voltage-time product remains constant. This increase in pulse number reduces the level of the harmonics in the motor current to a level comparable with the simple quasi-square-waveforms. However, the harmonic spectra associated with the quasi-square-waveforms (Fig.8a) give rise to significant motor losses requiring derating of the motor.

PWM control of a.c. motors using an LSI circuit

The motor performance obtained using the quasi-square inverter system can be improved by using the technique of sinewave-modulated pulse-width modulation (PWM). Many types of sinusoidal PWM systems have been developed in the past, but each system has had its own shortcomings, such as circuit complexity, cost, and output variation with temperature, etc. Our approach overcomes all of these problems by using a purpose-designed LSI circuit type HEF4752V for signal generation. This IC uses a totally digital approach and is fabricated using the LOCMOS process. A block diagram of the system is shown in Fig.9, and the PWM section, the most important part of this diagram, is described below.

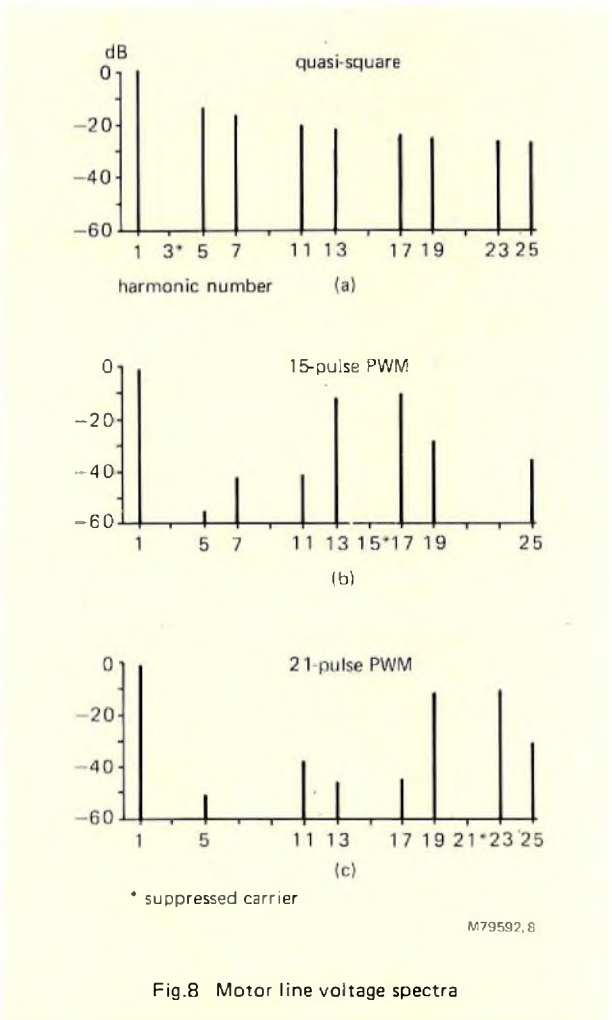


Fig.8 Motor line voltage spectra

The IC provides three complementary pairs of output drive waveforms which, when applied to a three-phase bridge inverter, produce a symmetrical three-phase (120°) output. Data inputs for reversing, start/stop, and interlock delay selection are provided. Twelve PWM outputs, together with monitoring and synchronising signals, are available for user control.

The output waveforms are pulse-width modulated using double-edged modulation such that the average voltage difference between any two of the three output phases varies sinusoidally, and this is illustrated in Fig.10 using a nine-pulse waveform for clarity. Figure 10a shows the unmodulated inverter output, 10b shows the double-edge modulated R-phase, 10c and 10d show the double-edge-modulated Y and B phases. The line-to-line voltage obtained by subtracting the R and Y phases is shown in Fig.10e. Double-edged modulation combined with odd multiple-of-three values for pulse number or frequency ratio n would give perfect line-to-line voltage waveform symmetry as illustrated in Fig.10e. The term n is defined as the ratio of switching frequency to motor drive frequency. In practice, the following eight pulse numbers (n) were chosen:

$$n = 15, 21, 30, 42, 60, 84, 120, 168.$$

Figure 8 compares the harmonic spectra of a quasi-square-waveform to the PWM waveforms with n = 15 and n = 21. The information in Fig.8 is also given in Table 1. These PWM harmonic patterns together with the variable pulse number operation produce low motor losses and smooth starting performance.

The relationship between the motor drive voltage and frequency is inherently linear, but separate control of voltage and frequency is possible if required. Double-edged modulation has the advantage of giving twice the number of line voltage pulses for any given switching frequency, resulting in substantially lower values for motor current ripple compared with single-edged modulation systems. The system has a built-in over-modulation capability which permits the PWM waveform to become a quasi-square waveform in the limit condition. This facility is useful in retro-fit applications where a standard induction motor is fitted to machinery and variable speed operation up to the same top speed is required.

The integrated circuit has four clock inputs which define motor frequency, motor Hz/volt, bridge switching

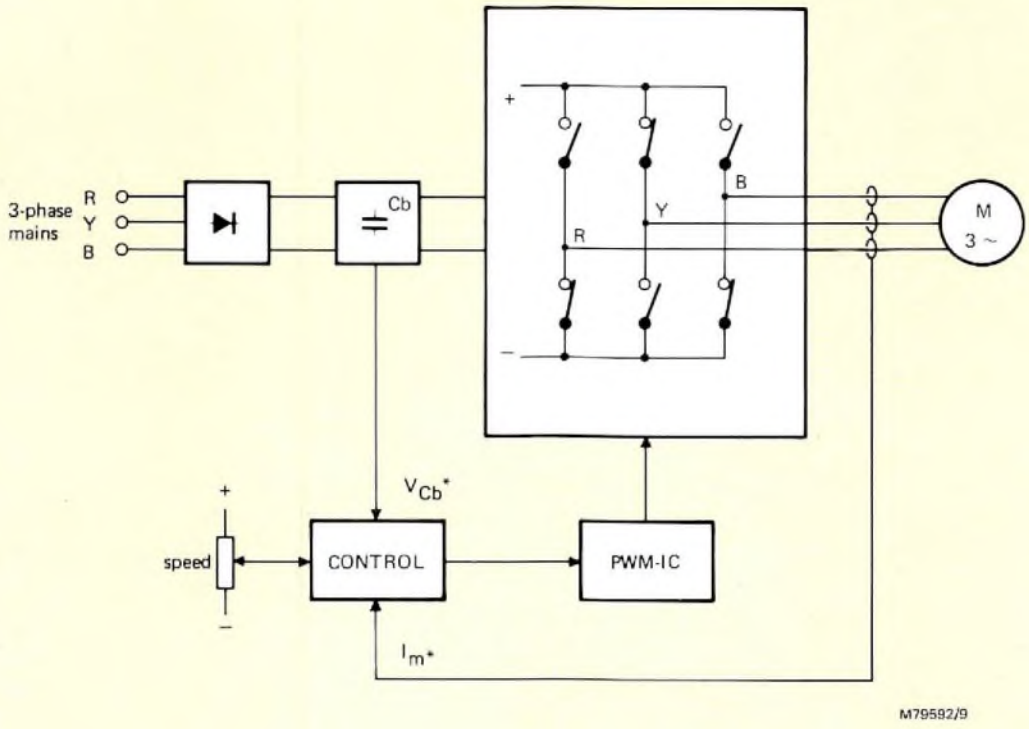


Fig.9 Voltage-source PWM inverter system

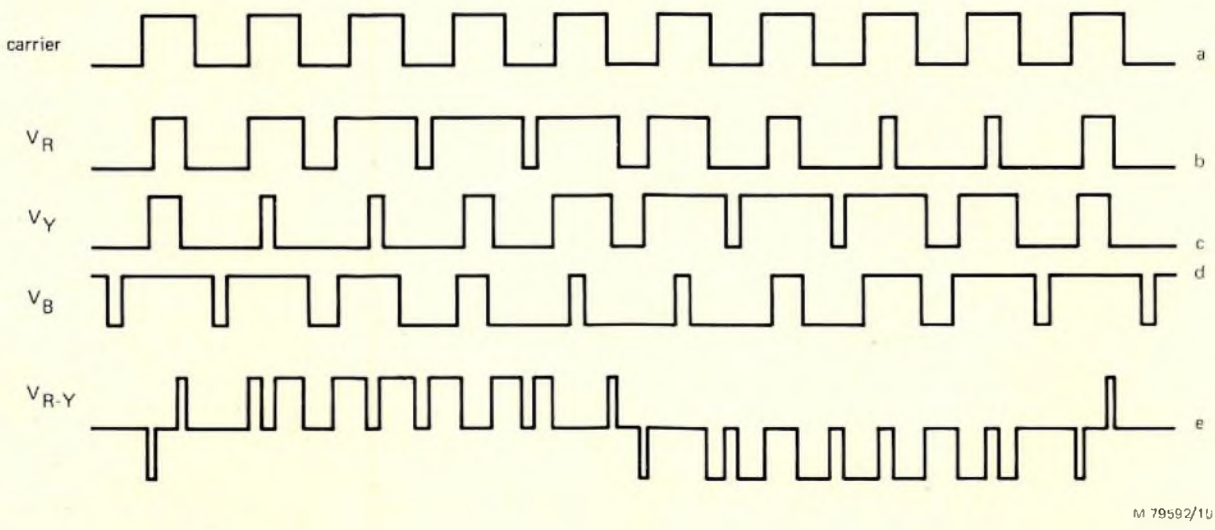


Fig.10 9-pulse sinusoidal PWM waveforms

TABLE 1

Harmonic contents for quasi-square, 15-pulse, and 21-pulse waveforms

Harmonic number	A_1	A_5	A_7	A_{11}	A_{13}	A_{17}	A_{19}	A_{23}	A_{25}
Quasi-square wave	1.103	0.221	0.157	0.100	0.085	0.065	0.058	0.048	0.044
15-pulse waveform*	0.881	0.002	0.007	0.009	0.248	0.305	0.038	0.001	0.016
21-pulse waveform*	0.881	0.003	0.001	0.014	0.005	0.006	0.257	0.295	0.031

*At 100% modulation

All tabulated values are referenced to the a.c. supply voltage source.

frequency, and minimum pulse width. The inverter switching frequency f_s is an integral multiple of the motor drive frequency f_o, that is:

$$f_s = nf_o.$$

Figure 11 shows typical operation with the maximum switching frequency set to 1 kHz. A small amount of hysteresis is included at the pulse number change points to ensure that jitter is avoided when operating in these regions. The minimum switching frequency is set internally by the LSI circuit to:

$$f_{s\,(min)} \simeq 0.6\, f_{s\,(max)}.$$

The frequency of the motor line-current ripple is held

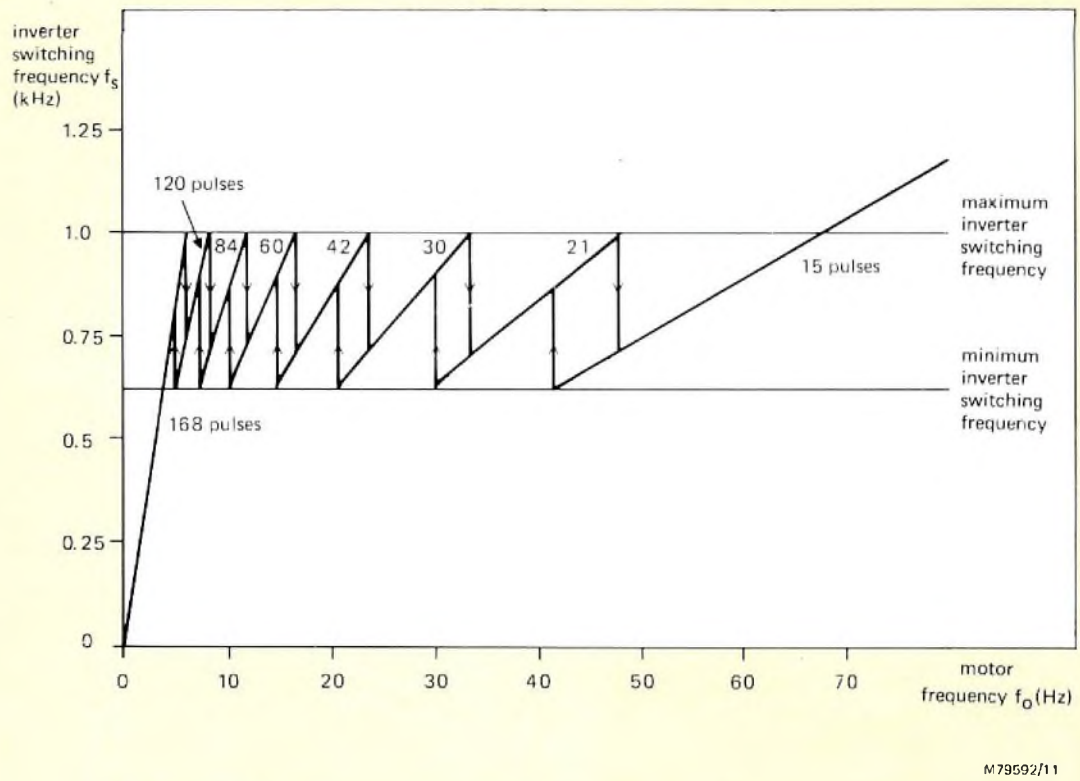
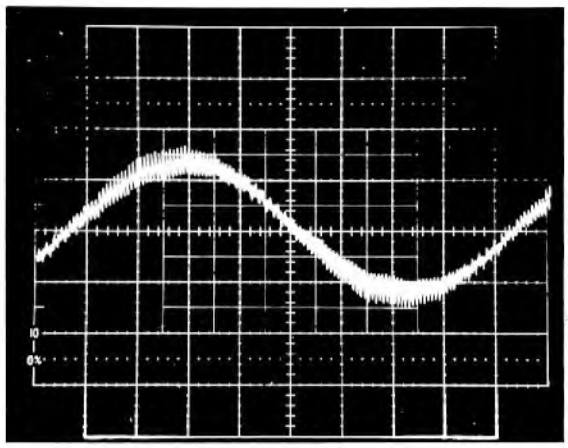
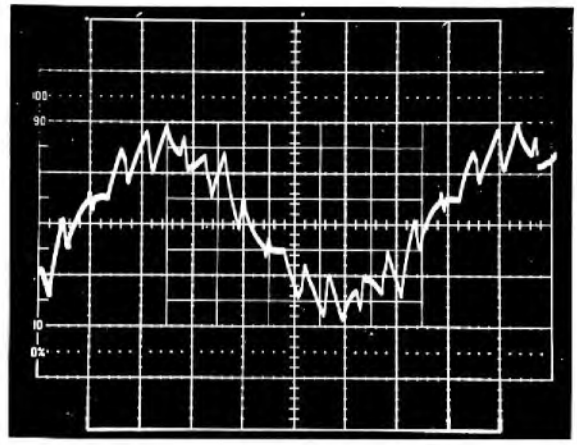


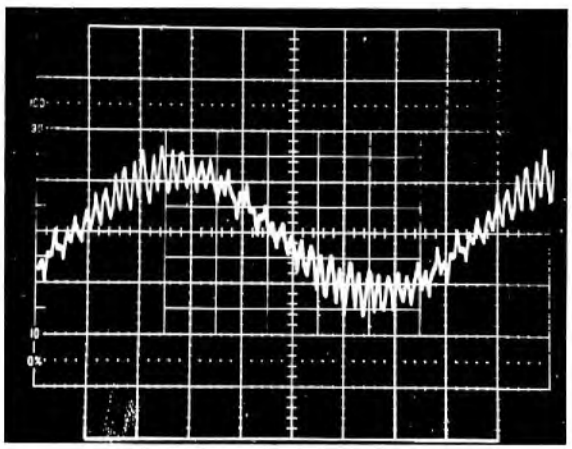
Fig.11 Inverter switching frequency versus motor drive frequency with pulse number as a parameter



(a)



(c)



(b)

Fig.12 Line current waveforms at various motor drive frequencies:
(a) motor drive frequency = 10 Hz
pulse number = 60
(b) motor drive frequency = 25 Hz
pulse number = 21
(c) motor drive frequency = 50 Hz
pulse number = 9

within a band of constant width over an operating motor drive frequency range of greater than 18.5:1.

Figure 12 shows the resultant line currents at various frequencies for a 2.2 kW motor system using a maximum switching frequency of 1 kHz.

Single section of three-phase inverter

The inverter circuit design required for PWM using the LSI circuit type HEF4752V is composed of three completely independent choppers, one for each of the phases R, Y, and B. A circuit diagram of a section of such an inverter is shown in Fig.13.

The circuit contains four thyristors: two main thyristors Th_1 and Th_2 which chop the rectified mains, and two commutation thyristors Th_3 and Th_4 which force-commutate Th_1 and Th_2. The trigger pulses for the thyristors are supplied via pulse amplifiers and trigger pulse transformers. The motor current I_m is conducted alternatively via Th_1 and the flywheel diode D_2, or via Th_2 and D_1. The commutation circuit for Th_1 is composed of the elements Th_3, D_3, L_2, and C_1, and flywheel diode D_1.

The anti-parallel connection of the main thyristor-diode combination (for example Th_1 and D_1) avoids the need to use reverse voltage commutation which is particularly important since it permits the use of modern high-speed asymmetric thyristor types having only a few volts reverse blocking capability.

The operating principle of the commutation circuit can be understood with reference to Fig.14 which shows only the basic elements of the commutation circuit associated with main thyristor Th_1. It is assumed that the capacitor C_1 is charged to the supply voltage with the polarity marked 'a' and Th_1 is conducting the load current I_m and is required to be turned off. Commutation is initiated by triggering the auxiliary thyristor Th_3. This action causes a sinusoidal resonant current to flow via Th_3, L_2, and C_1 in the direction indicated by the arrow marked 'A'. At the end of the half-cycle of sinusoidal

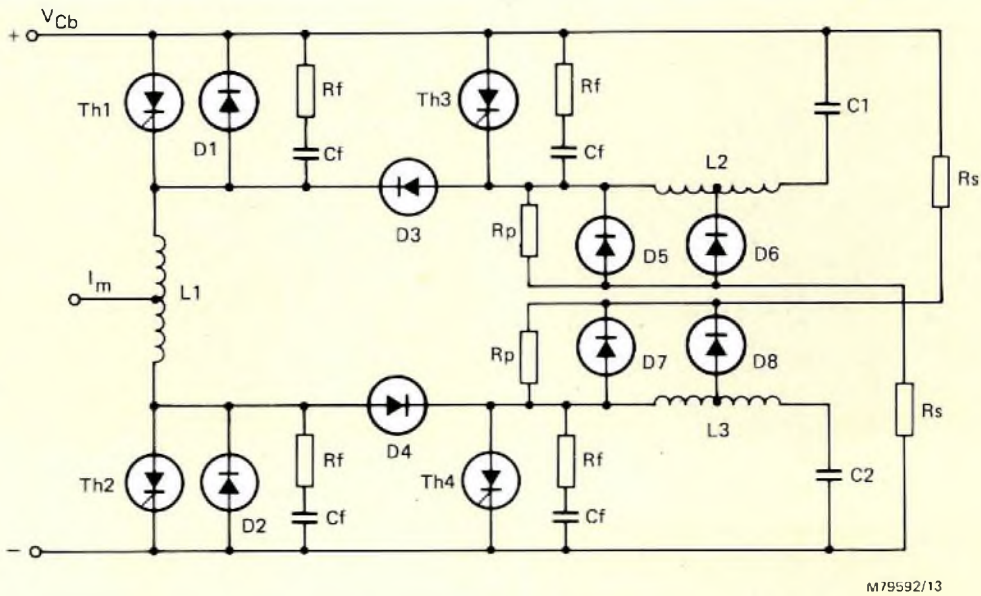


Fig.13 One phase of three-phase PWM inverter

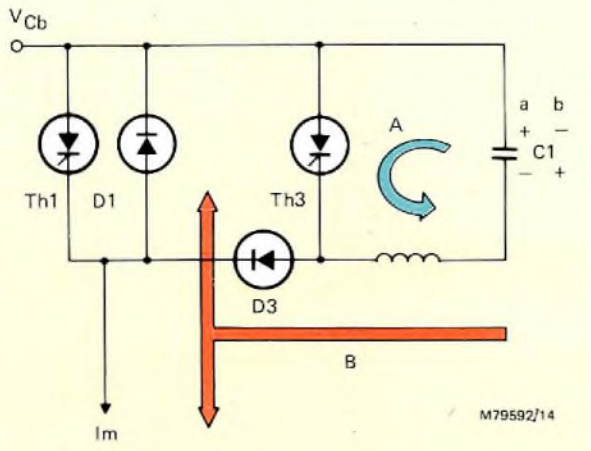


Fig.14 Principle of auxiliary commutation

current the voltage polarity of C_1 is now reversed (marked 'b'), the current through Th_3 is zero and Th_3 turns off. The direction of capacitor current now reverses, and the second half-cycle of sinusoidal resonant current begins to flow in the directions indicated by the arrow marked 'B'. As the current through D_3 increases during the resonant half-cycle, so the load current I_m is increasingly supplied from the resonant circuit. A point is reached when no current is supplied through Th_1 and the thyristor turns off. Any excess current flows through D_1, and the duration of conduction of D_1 provides the turn-off interval. During the fourth quarter-cycle when the current in D_3 is again reduced to the load current I_m, forward voltage is then reapplied to both thyristors Th_1 and Th_3, and the capacitor voltage polarity is now restored to the initial condition marked 'a' and commutation of Th_1 is complete.

The second half-sinewave of current which commutates-off Th_1 has an amplitude I_{cp} and a period T_{cp} given approximately by:

$$I_{cp} = V_{Cb}\sqrt{(C_1/L_1)},$$

$$T_{cp} = \pi\sqrt{(L_2C_1)},$$

where C_1 = commutation capacitance and L_2 = commutation inductance.

The values of C_1 and L_2 must be chosen so that the commutation current in L_2 exceeds the maximum peak load current I_m for the commutation turn-off, 't_q value' of the thyristor Th_1.

In the inverter section shown in Fig.13, the values of L_2 and C_1 required are determined by the maximum motor peak current, the minimum d.c. voltage $V_{Cb(min)}$, and the required turn-off time t_q of Th_1, as given in the following equations:

$$L_2 \geq \frac{0.4\ V_{Cb(min)} \times t_q}{I_{m(pk)}},$$

$$C_1 \geq \frac{t_q \times I_{m(pk)}}{V_{Cb(min)}}.$$

An RC filter is connected across each thyristor to ensure that, after commutation the rate of rise of reapplied voltage dV/dt does not exceed the thyristor rating. Diodes D_6 and D_8 with the resistors R_s provide critical

damping of the L_2C_1 and L_3C_2 circuits at the end of a commutation cycle. Diodes D_5 and D_7 limit the maximum peak voltages across the thyristors to slightly more than the d.c. supply voltage.

For good performance, smooth operation at low speeds, and high electrical efficiency, it is necessary to operate the inverter at a relatively high PWM switching frequency. This requires the use of thyristors with short t_q times and high reapplied dV/dt ratings together with correspondingly fast diodes. Suitable thyristors and fast diodes are available from our range.

A.C. MOTOR SPEED CONTROL SYSTEM USING HEF4752V

An example of a practical drive system has been designed round our fast thyristors and the PWM IC type HEF4752V (see Fig.15). The type of thyristors, and the design of the power section, are determined by the power rating of the motor which is to be controlled.

System specification

The specification of the described system includes:

- Mains input: standard three-phase, 380 to 415 V, 50 Hz
- Fast dynamic speed response (accelerating and decelerating)
- Output frequency: 0 to 100 Hz (bidirectional speed control)
- Output voltage: up to 415 V r.m.s. (line-to-line) for 415 V r.m.s. line voltage input
- Fast dynamic braking

Control system

The control system provides the following facilities.

- Adjustment of motor speed, from zero up to twice nominal speed. Remote control is possible by an externally supplied control voltage.
- Adjustment of maximum motor current up to about 150% of the nominal value.
- Adjustment of the acceleration and deceleration time during motor speed variation.

Fig.15 2,2 kW PWM a.c. motor control system

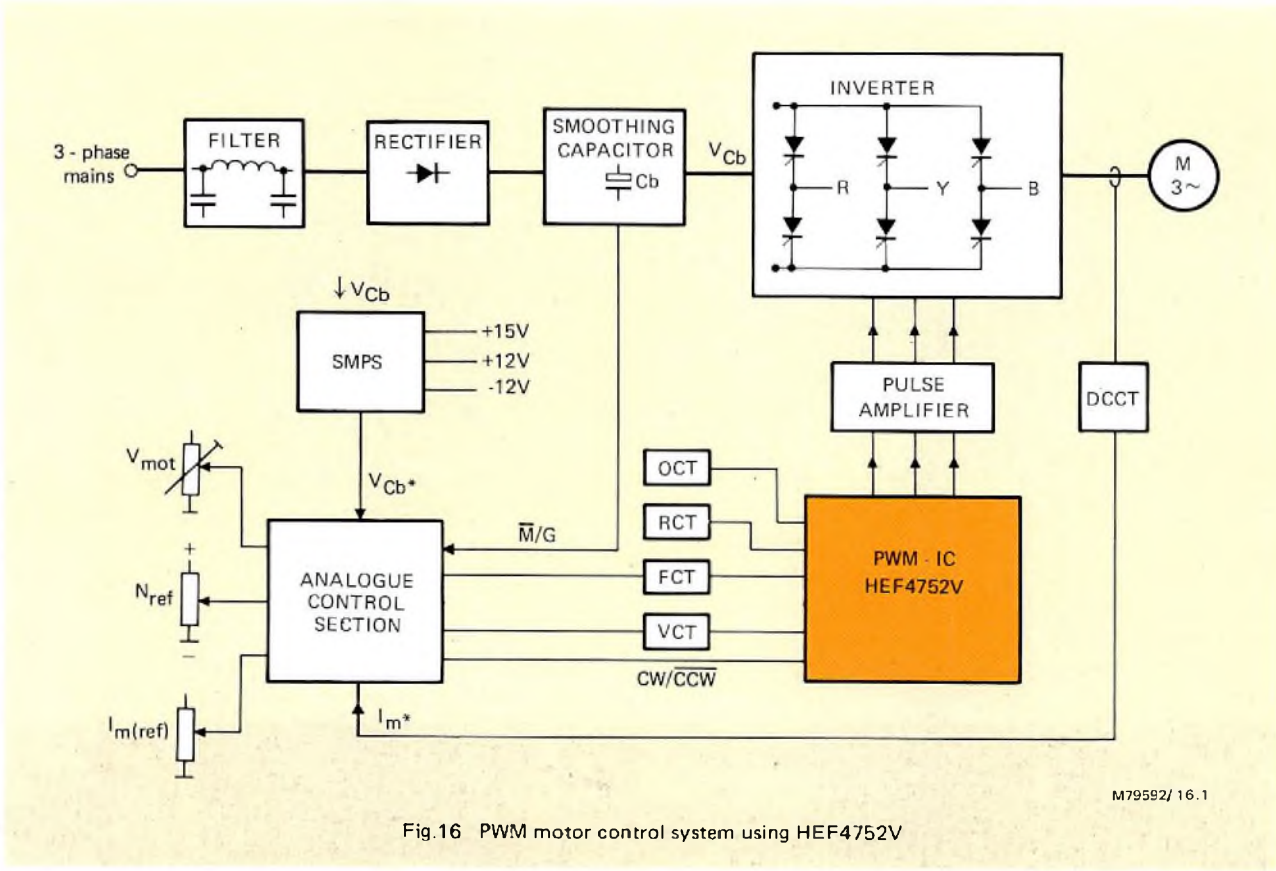


Fig.16 PWM motor control system using HEF4752V

- Limitation of power regenerated during speed deceleration to protect the inverter against overvoltage.
- Adjustable slip correction to improve speed regulation with load variation.
- Adjustable 'IR' compensation to increase the starting torque.

The basic speed control system is shown in Fig.16. The mains input is connected to the rectifier via an interference filter which ensures that mains pollution caused by the inverter remains below CISPR and VDE limits. The d.c. voltage V_{Cb} is smoothed by a smoothing capacitor and then applied to the inverter. The inverter delivers the three-phase output voltages for the a.c. motor. The d.c. supply voltage is also connected to an SMPS, which provides the low-voltage supply for the control section.

To limit motor current and V_{Cb} during overload or braking conditions, the following three feedback signals are supplied to the control section.

- A voltage V_{Cb}*, from the SMPS: this signal is proportional to the d.c. voltage across the smoothing capacitor. Without some form of voltage limitation, the d.c. voltage across the smoothing capacitor can become excessive under uncontrolled braking conditions. V_{Cb}* is also used to provide safe operating conditions during switch-on and switch-off.
- A signal M/G: this signal is also derived from the smoothing capacitor voltage, and indicates the direction of power flow in the drive system (motor mode or generator mode).
- The motor current signal I_m*: this is sensed by a D.C. Current Transformer (DCCT) in the motor current lines.

The twelve thyristors of the inverter section are triggered by the PWM IC, the HEF4752V, via pulse amplifiers and trigger transformers. The HEF4752V generates the sinusoidal pulse-width modulated signals. The following four clock inputs VCT, FCT, RCT, OCT define the operating conditions of the IC.

- VCT (Voltage Clock Trigger). This determines the output frequency/voltage ratio (Hz/V).
- FCT (Frequency Clock Trigger). This determines the motor supply frequency, thereby controlling the motor speed.
- RCT (Reference Clock Trigger). This sets the inverter maximum switching frequency.
- OCT (Output Clock Trigger): This sets the minimum pulse-width allowable.

The CW input to the HEF4752V determines the direction of motor rotation. The motor can only be reversed when the FCT clock is stopped. Both FCT and

VCT are generated in the control section. Motor speed, maximum motor current, and motor voltage are adjustable by potentiometer settings N_{ref}, $I_{m(ref)}$, and V_{mot}. However, under overload and regenerative conditions, the motor speed is also controlled by the motor current and the d.c. voltage across the smoothing capacitor. The analogue control section provides the required start and stop signals to ensure safe switching on and off of the power section.

Speed reference circuit

The speed reference circuit provides the voltage control signal for the FCT clock pulse generator. The input speed reference signal can be adjusted by potentiometer, N_{ref} from −10 V to +10 V, varying the motor speed from maximum clockwise to maximum counter clockwise. A functional diagram of the circuit is given in Fig.17. The circuit rectifies the input signal. The output signal can be expressed as $V_N = -k|N_{ref}|$. The required direction of rotation is given by the digital CW/$\overline{\text{CCW}}$ output signal.

The output V_N is derived from the signal N_{ref} via a comparator (1) and an integrator (2). A stepwise variation of N_{ref} results in a linear increase or decrease of the output signal V_N. The rate of variation of V_N can be adjusted via the accelerate/decelerate limiting potentiometers A and D, as shown in the waveforms of Fig.18. This control of maximum speed variation protects the drive system, and is useful for achieving special speed change characteristics. Inverter protection against excessive motor currents and against excessive voltage across the smoothing capacitor during a regenerative mode is given by the I_{lim} signal, obtained from the current voltage control circuit (see next section). A motor current which exceeds the preset current limit under motoring conditions (such as a stalled motor), will result in a negative signal of I_{lim}. The negative value of V_N will be

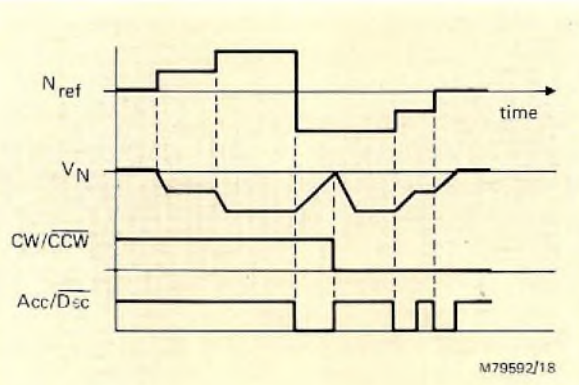


Fig.18 Performance of speed reference control system

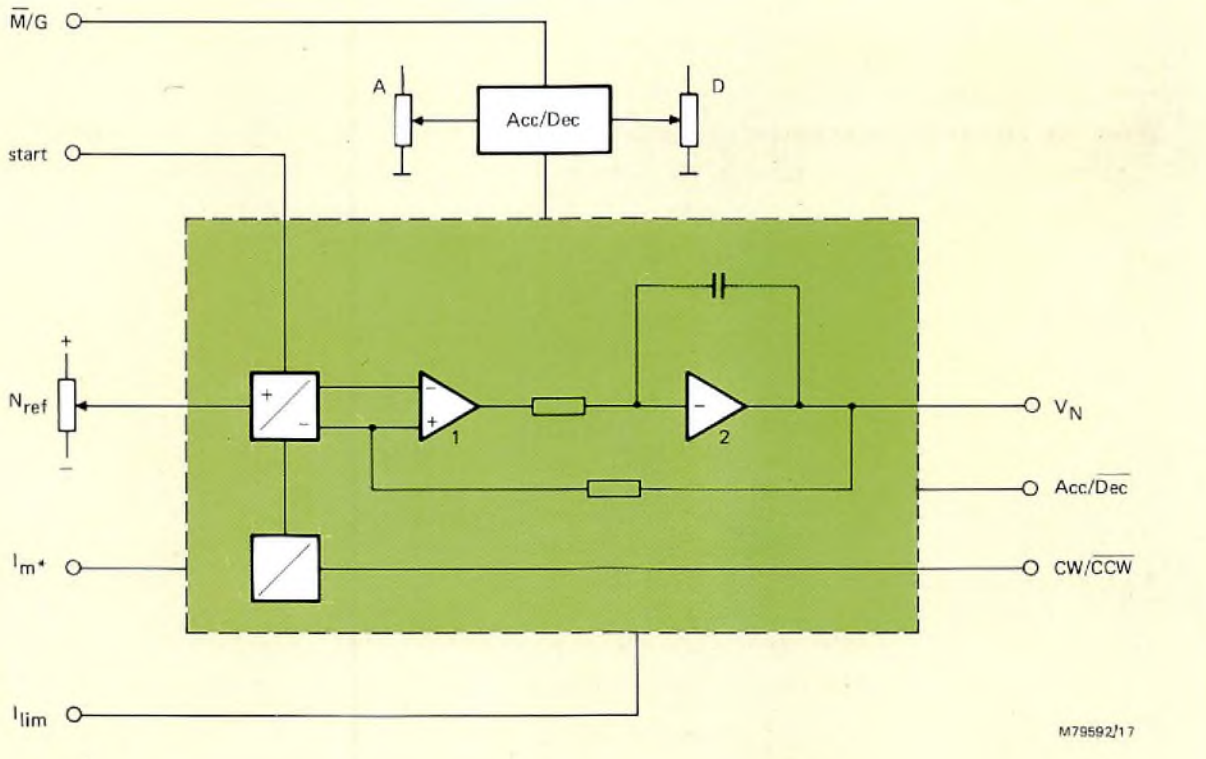


Fig.17 Speed reference control system

decreased, resulting in a lower output frequency of the inverter, thereby reducing the slip and the motor current.

Under regenerative conditions, I_{lim} will be positive if the preset limits for current or voltage across the smoothing capacitor are exceeded. This action increases the value of $-V_N$, and thus increases the output frequency. In this way the frequency difference between inverter and rotor (slip frequency) is decreased, thereby reducing the braking torque of the motor.

For correct current control, the $\overline{M}/G$ signal is also supplied to the accelerate/decelerate limiting circuit. Motor acceleration is prevented as long as the $\overline{M}/G$ signal indicates the generator mode. A second digital input is provided by the start signal which releases the output V_N after the start procedure. To improve the motor speed stability, a signal I_m* can be applied to the input of the first comparator (1). This signal increases the inverter output frequency when the motor torque is high (slip correction).

Current/voltage limitation

As mentioned in the previous section, the inverter should be protected against excessive current and voltage. The current and voltage control loops that provide this protection are shown in Fig.19.

The motor current is measured by three d.c. current transformers connected between the inverter output and motor. If the motor current exceeds the value set by the potentiometer $I_{m(ref)}$, I_{lim} becomes negative, resulting in reduction of the inverter output frequency and hence the motor torque.

During braking, when power is regenerated to the d.c. supply source, the voltage across the smoothing capacitor V_{Cb} rises above its normal value. This increase results in an activation of the $\overline{M}/G$ signal from the mains supply section, and the lower control section of Fig.19 becomes operative. As soon as the braking current signal I_m* exceeds the value of $I_{G(ref)}$, a positive voltage is generated at the I_{lim} output. The inverter output frequency is therefore increased and the braking torque reduced. If the voltage across the smoothing capacitor exceeds the preset maximum level $V_{Cb(ref)}$, the comparator (3) reduces the reference value $I_{G(ref)}$ of the current comparator (4). The braking torque will then be reduced to a level where the regenerated power is just compensated by power losses of the inverter, the SMPS, and the motor. As a result of this control principle, the maximum braking action is always available.

Motor voltage control

To improve the low-speed torque of the motor, required for such load conditions as compressors and vehicle drive systems requiring a high starting torque, it is necessary

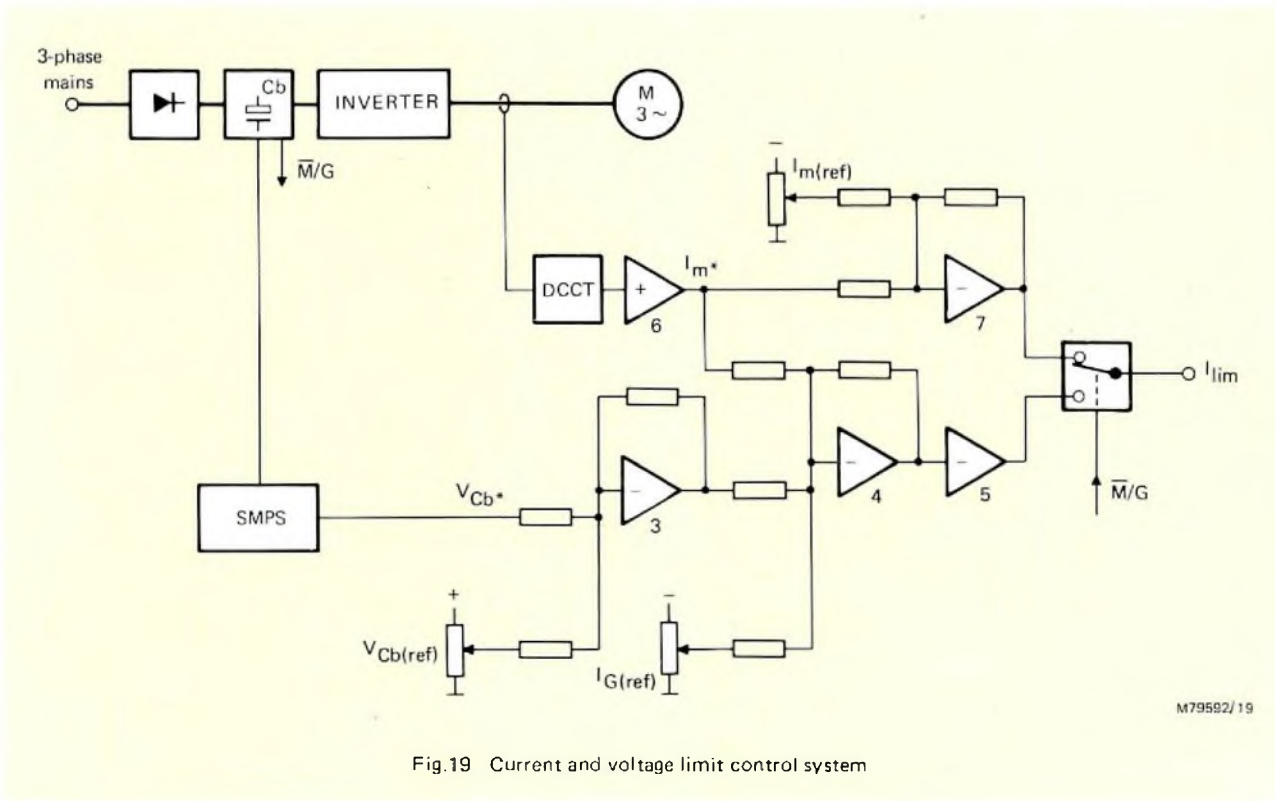


Fig.19 Current and voltage limit control system

to increase the motor voltage at low speed. This function, which compensates for the relatively high 'IR' losses at low speed, is obtained by decreasing the frequency of the VCT clock at the low end of the speed range. The circuit can be adjusted with three potentiometers giving control over the following conditions:

1) the motor voltage at nominal speed,
2) the speed range for 'IR' compensation,
3) the maximum 'IR' compensation at zero speed.

APPLICATIONS

The stage of technological evolution has now been reached where it is cost-effective to manufacture general-purpose high-quality industrial variable-speed drives using three-phase induction motors. This has been made possible by recent advances in power semiconductors and the introduction of a purpose-designed LSI circuit for signal generation.

The system described in this article illustrates one method of producing a high-performance variable-speed drive for a three-phase induction motor, using the most advanced power semiconductors and LSI technology now available. Typical applications of variable-frequency a.c. inverters include:

- textile manufacturing,
- chemical processing,
- glass manufacture,
- machine tools,
- polymer forming,
- food processing,
- material handling and packaging,
- printing and paper making,
- grinders,
- pumps.

In these and many other applications, the electronic motor control system described in this article provides improved efficiency, compactness, and control flexibility.

REFERENCE

1. NIJHOF, E.B.G.'Een Spannings/Frequentieomvormer Voor Draaistroommotorregelingen', Polytechnisch Tijdschrift, Elektrotechniek Electronica, Jaargang 33, November 1978, pp.651 to 663.

Application note

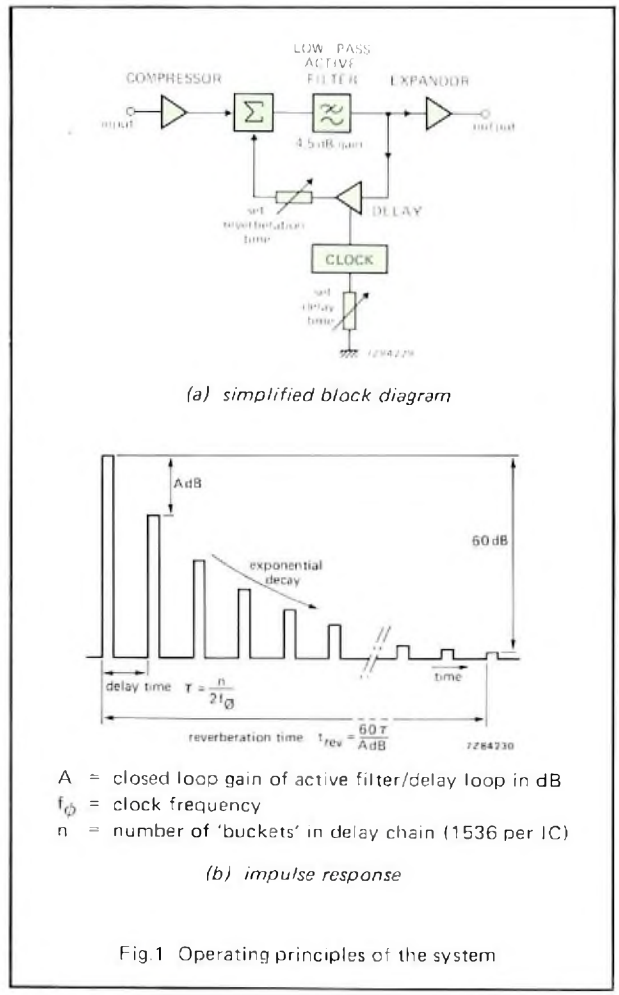
Bucket-brigade delay-line enhances sound reproduction

In the reproduction of recorded music, one thing is conspicuously missing: no matter how good the recordings or reproduction equipment, the true ambience of 'live' music still cannot be re-created in the home. This is because the original sound would have reached our ears in two ways; direct sound from the instruments and indirect sound reflected from the walls and ceiling of the auditorium. Since the indirect sound travels much further than the direct sound in a large hall, it is considerably delayed and, furthermore, it is reflected many times, each reflection being weaker than its predecessor. In other words, the indirect sound reverberates.

To re-create this effect in the comparatively small home listening room, at least one other loudspeaker must be added and fed with a muted, delayed and slowly decaying version of the signals fed to the main loudspeakers. Until recently, achievement of the necessary initial delay (up to 300 ms) by inexpensive and purely electronic means posed a problem. That problem was solved by the development of integrated charge-transfer devices cascaded to form a 'bucket brigade' delay line. One of the first of these was the TDA1022 (Ref.1) with 512 'buckets', delay up to 25 ms and insertion loss of only 4 dB. This circuit is mainly intended for creating sound effects for electronic musical instruments.

We have now developed the TDA1097 with 1536 'buckets', delay up to 75 ms and zero insertion loss. Four of these circuits in cascade form the heart of an add-on listening room expansion system that can bring a new dimension to high-fidelity sound reproduction.

The operating principles of the 'bucket brigade' are



(a) simplified block diagram

(b) impulse response

A = closed loop gain of active filter/delay loop in dB
f_ϕ = clock frequency
n = number of 'buckets' in delay chain (1536 per IC)

Fig.1 Operating principles of the system

This note is based on a laboratory report. Requests for additional data should mention the title of the note, the issue of E.C.&A. in which it appeared, and the nature of the applicant's interest.

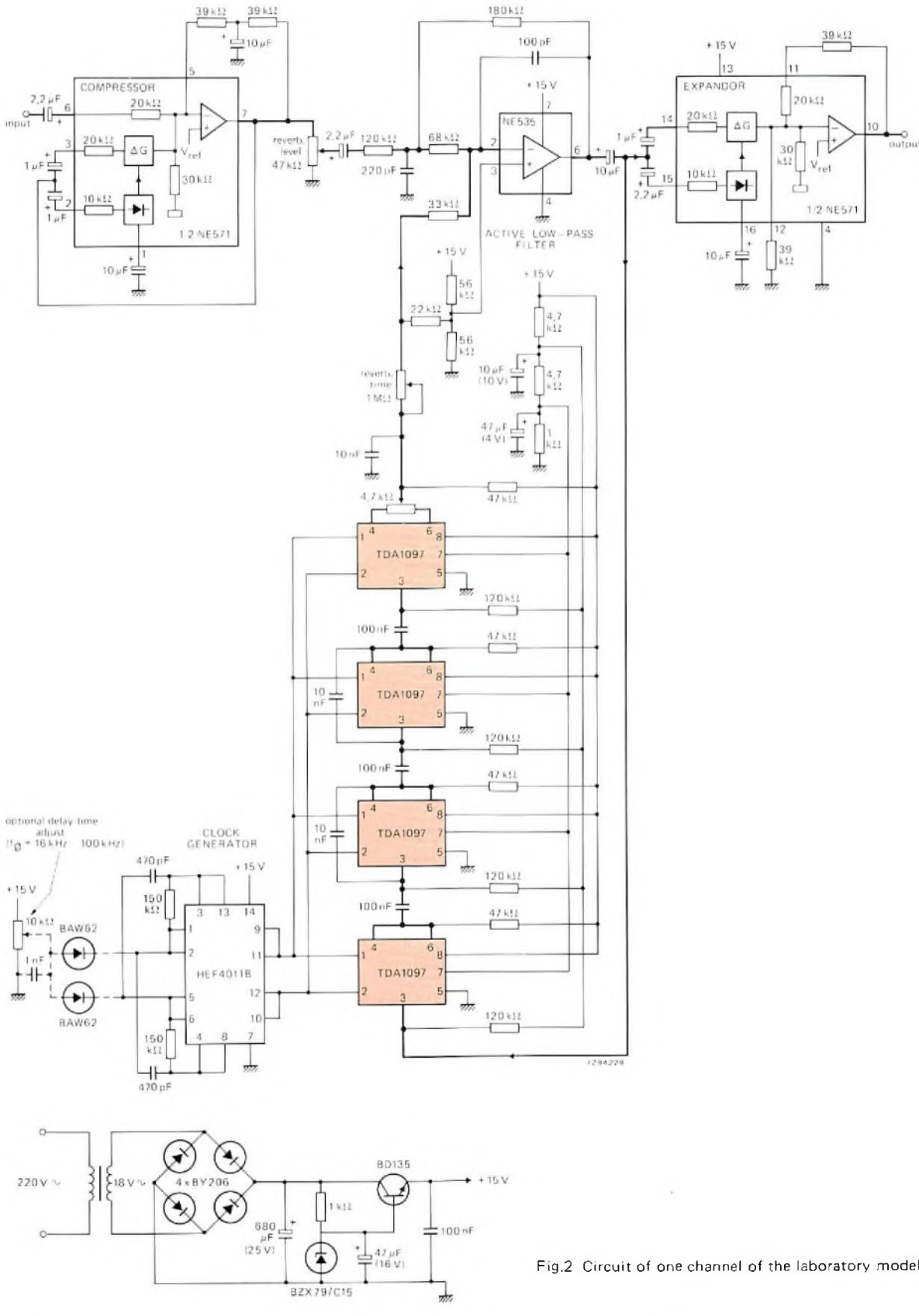


Fig.2 Circuit of one channel of the laboratory model

Performance of the circuit in Fig.2

Clock frequency	10 kHz	16 kHz	100 kHz
Delay time	307 ms	192 ms	31 ms
Maximum reverberation time	6 s	3.8 s	620 ms
Delay bandwidth (−3 dB)	3 kHz	5.3 kHz	25 kHz
S/N ratio referred to V_O = 1 V r.m.s.		>60 dB	
THD at V_O = 1 V r.m.s.		<1%	
Minimum input voltage		70 mV r.m.s.	
Maximum output voltage		1 V r.m.s.	
Input impedance		20 kΩ	
Output impedance		<1 kΩ	
Current consumption with V_S = 15 V, V_O = 1 V r.m.s.		<100 mA	

fully explained in Ref.1 and will not be repeated here. The principles of operation of a laboratory model of a listening room expansion system are shown in Fig.1. From the block diagram it can be seen that, if an impulse is applied to the input of the system, it will pass around the delay loop once for each delay period and will be attenuated each time by the closed-loop gain (−3 dB or less). Since the delay time τ is equal to $n/2f_\phi$ it can be varied by adjusting the clock frequency. The reverberation time (decay time) is inversely proportional to the closed-loop gain and can be varied by adjusting the amount of delayed feedback.

If the fundamental or a harmonic frequency of the incoming signal approaches half the clock frequency, it will be sampled less than twice per cycle and an erroneous lower frequency (alias frequency) signal will appear at the output. It is therefore necessary to restrict the high-frequency response of the reverberation system to not more than half the clock frequency. In practice, it is restricted to one-third of the clock frequency by a low-pass, second-order active filter which also provides about 4.5 dB of gain. This bandwidth restriction is of little consequence to the audible results since the higher frequencies in a 'live' listening environment are quickly absorbed and do not therefore reverberate.

To allow the circuit to handle a wide dynamic range without degrading the signal-to-noise ratio, a compressor/expandor (compandor) is added to the system. This circuit is fully explained in Ref.2.

A system such as that described would normally exhibit a frequency response like that of a comb filter instead of the desirable all-pass characteristic. This would impart a hollow, reedy or metallic quality to the reverberated sound. The required all-pass characteristic is simulated by applying an additional feedback loop around some of the delay circuits.

The full circuit diagram of one channel of the system is given in Fig.2 and its performance, is given in the table.

There are many ways of adding this variable reverberation system to an existing sound installation. As an example, the system could be entirely separate with its own stereo amplifier and loudspeakers. The level of the reverberated sound should be about half of that from the main system, and the loudspeakers, which need not have an extended frequency response, should be positioned so that they cannot be heard as identifiable sound sources. The reverberated signals can also of course be applied to the main amplifier and mixed with the normal signals. In this case, separate loudspeakers and amplifier are not necessary.

REFERENCES

1. TDA1022: an integrated bucket-brigade delay line for audio signal processing, Technical Information 038. N.V. Philips Gloeilampenfabrieken, Elcoma Marketing Communications, Eindhoven, The Netherlands, 1977.
2. Analogue compandor, Technical Note 031. N.V. Philips Gloeilampenfabrieken, Elcoma Marketing Communications, Eindhoven, The Netherlands. 1976.

Mains pollution caused by domestic appliances

Part 2 - Harmonic distortion

H. W. EVERS

In this article we shall concentrate on the problem of harmonic distortion. This problem is not new since for many years fluorescent lamps, transformers and appliances employing bridge rectifier circuits have produced harmonic distortion in the mains supply. However, recent years have seen such a dramatic increase in the use of electronically controlled domestic appliances that harmonic distortion is now approaching intolerable levels.

The situation is not helped by the current popularity of phase control as a means of power regulation. Employing such devices as thyristors and triacs, phase control can introduce severe distortion into the supply. The problem can be alleviated to some extent by limiting the power of equipment employing phase control. This approach has been adopted by CENELEC (European Committee for Electrotechnical Standardization) and is embodied in its Standard EN 50 006.

The real solution to the problem, however, lies not solely in power limitation, but in an overall rethink of our design philosophies. Only in this way can we hope to produce future equipment that provides minimum interaction with the supply.

This article is a first attempt at providing a basis for such a rethink. We cannot hope to cover all the problems that will present themselves to the designer. Our object is simply to bring to the designer an awareness of the problems, and to provide him with guidelines on appropriate circuit design.

We shall begin by considering some aspects of phase control, since this is potentially a major cause of harmonic distortion, and is accordingly the subject of much debate on the CENELEC Committee.

POWER REGULATION BY PHASE CONTROL AND ITS EFFECT UPON HARMONIC CONTENT

Phase control, by which is meant the controlled conduction of current over a selected part of the mains cycle, is becoming increasingly popular as a means of power regulation. Devices employing it include light dimmers and motor control units used in portable tools, vacuum cleaners etc. At present its use is limited in cooking and heating appliances. Such control can be effected either by a triac (symmetrical control) or by a thyristor (asymmetrical control). In both cases the output signal shows substantial departure from pure sinusoidal and the harmonic content is high.

Symmetrically controlled loads

Symmetrical phase control generates odd harmonics only, their amplitudes being governed by the firing angle α. This is illustrated for a purely resistive load in Fig.1, which shows normalized harmonic amplitudes together with the power factor $\cos \phi$ as functions of α.

The harmonics generated by inductive loads (combined inductive and resistive) are of lesser magnitude than those generated by pure resistive loads. This is illustrated in Table 1 which shows the effect of symmetrical phase control operating on a combined inductive/resistive load. An obvious consequence of this is that for the same harmonic content, the phase controlled power is higher for inductive loads than for resistive loads. Figure 2 gives the relation between third harmonic and firing angle α for a symmetrically controlled inductive load.

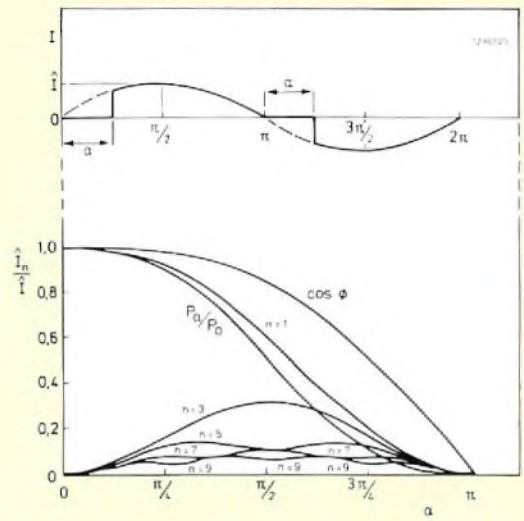


Fig.1 Harmonic content (normalised amplitudes) produced by a symmetrically controlled resistive load. Also shown are the power factor cos ϕ and the fractional power P_α/P_0 as functions of α

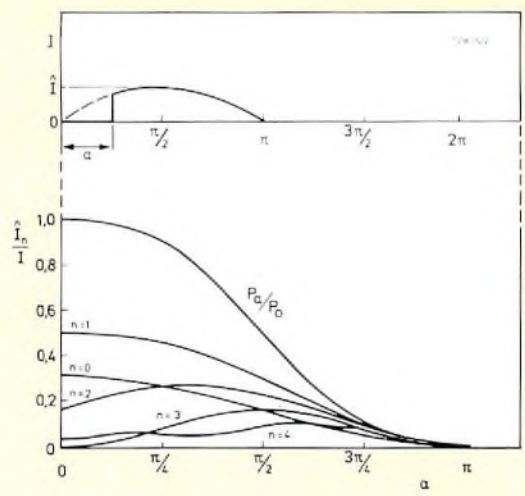


Fig.3 Harmonic content (normalised amplitudes) produced by an asymmetrically controlled resistive load. Also shown is the fractional power P_α/P_0 as a function of α

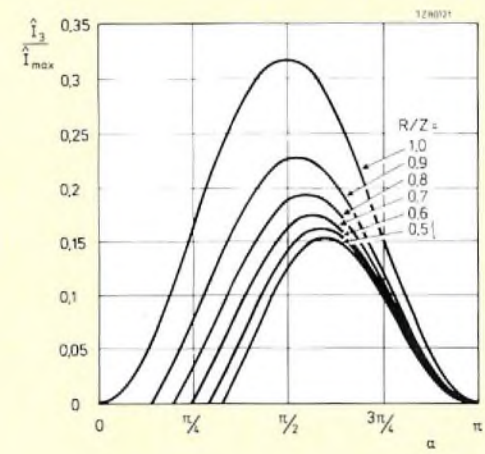


Fig.2 Third harmonic content (normalised amplitudes) produced by a symmetrically controlled combined inductive/resistive load

TABLE 1

Peak amplitudes (normalised values) of the current harmonics produced by a symmetrically controlled combined inductive/resistive load

n	R/Z					
	1	0,9	0,8	0,7	0,6	0,5
3	0.318	0.227	0.193	0.174	0.161	0.153
5	0.138	0.078	0.067	0.061	0.058	0.055
7	0.106	0.041	0.032	0.030	0.029	0.028
9	0.076	0.026	0.020	0.018	0.017	0.016
11	0.064	0.016	0.014	0.012	0.011	0.011
13	0.052	0.012	0.010	0.009	0.008	0.008
15	0.046	0.009	0.007	0.006	0.006	0.006

Asymmetrically controlled loads

In asymmetrically controlled loads, both odd and even harmonics are generated, as well as a d.c. component. At a given power the harmonic content produced by asymmetrical control is significantly higher than that produced by symmetrical control. Figure 3 gives the normalized amplitudes of the harmonics as functions of α, for a purely resistive load. The figure also shows the variation of fractional power with α (i.e. P_α/P_0 where P_α is the power at firing angle α).

PROBLEMS ASSOCIATED WITH HARMONIC DISTORTION OF THE MAINS SUPPLY

Current harmonics generated in the 220/250 V line by consumer appliances will inevitably transfer to the H.T. supply system (commonly 10 or 25 kV). Here they produce disturbances that eventually feed back to the consumer, adversely affecting the performance of all mains connected appliances. Some of the important effects are listed below:

- Voltage harmonics. Current harmonics in the H.T. system give rise to corresponding voltage harmonics. These distort the sinusoidal voltage of the H.T. system itself, leading to inferior performance of both supplier and consumer equipment. Another effect of voltage harmonics in the H.T. system is the premature actuation of remote control devices of the supply network operating between about 200 and 400 Hz.
- Resonance in the H.T. system. The H.T. system comprises many resonant circuits formed by the combination of cable capacitance, load impedance and transformer inductance, as well as the capacitive networks included to correct for phase shifts. Current overloads may occur in these circuits if the harmonics happen to excite them at their resonant frequencies. These overloads can cause severe damage, particularly to the phase correction capacitors.
- Voltage drop in the low tension system. Current harmonics in the low tension system produce a voltage drop which reduces the efficiency of all mains connected appliances. This voltage drop depends on the length and composition of the supply cables, and on the magnitude and order of the current harmonics.
- Losses in the mains network. Phase control introduces phase shifts into the mains network. These can result in significant losses, particularly during peak periods.
- D.C. biasing of the mains. Asymmetrical phase control besides generating both odd and even harmonics, also produces a d.c. component (n = 0 in Fig.3). Hence, if used extensively, this type of control can cause a voltage bias on the mains network, thus increasing the chance of mains transformer saturation.

Harmonic distortion produced by a given source is directly related to the impedance of the mains, which in turn depends on the complexity of the mains network. Moreover, the mains impedance is generally frequency dependent in all but the simplest networks, so that a knowledge of this dependence is essential for assessing the effects of harmonic distortion in a real system. Fig.4 shows the H.T. mains impedance as a function of frequency for three networks exhibiting varying degrees of complexity.

For the purposes of rationalization in its recommendations of maximum permitted harmonic content, CENELEC has assumed a typical mains impedance on the low tension side (220/240 V single phase) of $Z = (0.4 + 0.25j)\Omega$ at 50 Hz. In most modern networks, however, the impedance will be lower than this.

THE CENELEC RECOMMENDATIONS

The CENELEC Standard EN 50 006 applies to all household electrical appliances supplied from a low tension network, that can be purchased directly by the consumer, and that are equipped with regulating means employing burst firing or phase control. This covers electric cooking and heating appliances, portable tools, light dimmers, etc. It does not cover television and radio receivers, and other such devices.

The recommendations regarding maximum harmonic content are given in Table 2, and apply to a device driven from the nominal mains voltage at 50 Hz. Devices may be subject to test by the supply authorities to ensure that they meet these recommendations.

Studies carried out by some supply authorities indicate that phase control, operating over long periods

TABLE 2

Maximum harmonic content permitted by the CENELEC recommendations, for an appliance driven from the nominal mains voltage at 50 Hz

	harmonic order (n)	maximum harmonic content %
odd harmonics		
	3	0.85
	5	0.65
	7	0.60
	9	0.40
	11	0.40
	13	0.30
	15	0.25
	⋮	⋮
	39	0.25
even harmonics		
(a) symmetrical control	2	0.20
	4	0.20
	⋮	⋮
	40	0.20
(b) asymmetrical control	2	0.30
	4	0.20
	⋮	⋮
	40	0.20

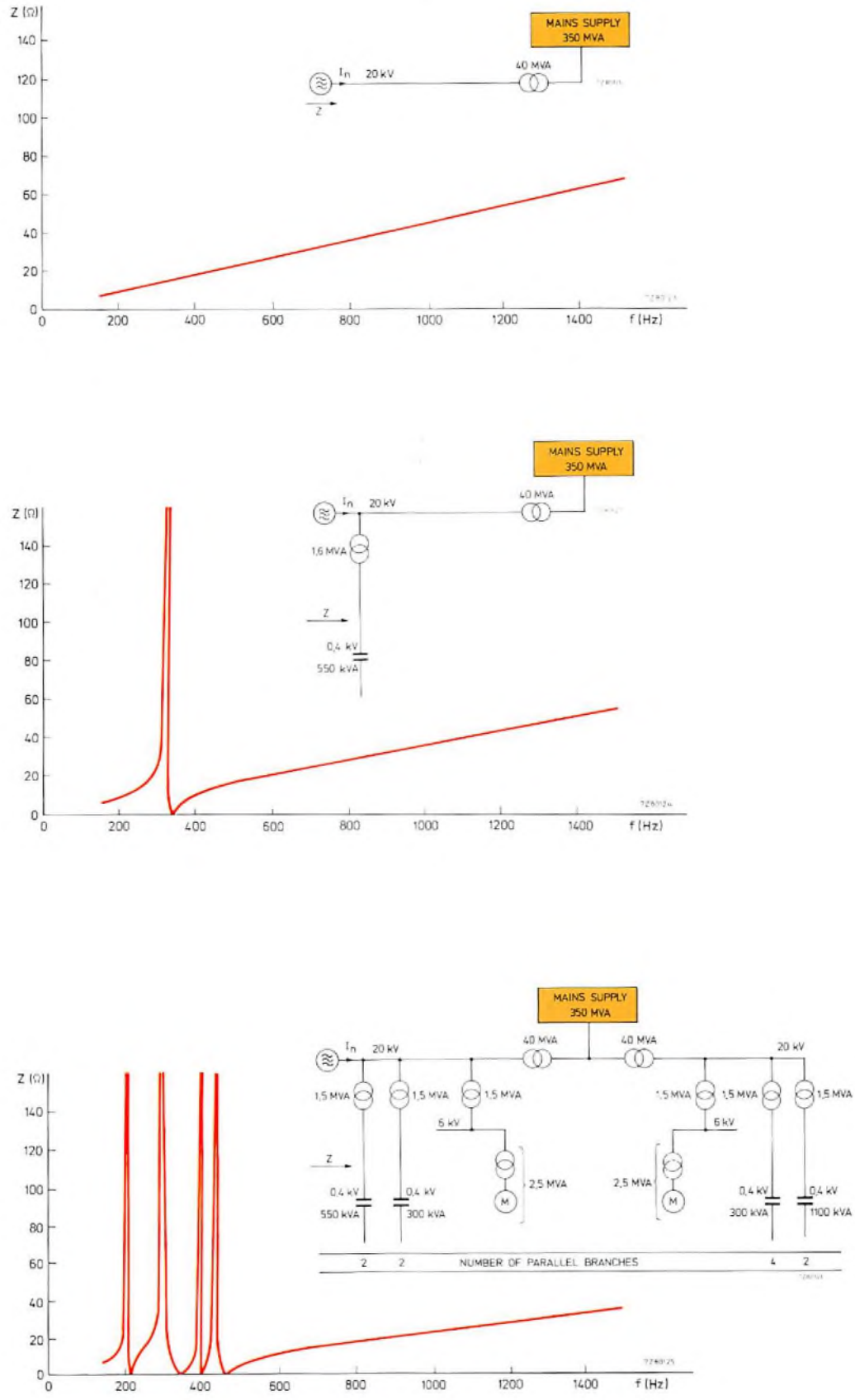


Fig.4 Some characteristic impedances of the HT (20 kV) network

and with a high degree of occurrence, should be restricted to reduce the harmonic content and the additional losses introduced into the mains network, and to save the extra capital investment that would be necessary to boost the mains capacity.

Partially as a consequence of these investigations, CENELEC has recommended the prohibition of phase control for all thermal appliances in the domestic field having a power greater than 200 W. (Note: in this context light dimmers are not regarded as thermal appliances.)

The CENELEC recommendations are supported by the supply authorities of most European countries and it is thus advisable for manufacturers to comply with them.

ASPECTS OF EQUIPMENT DESIGN CONCERNED WITH REDUCING HARMONIC DISTORTION

Reducing harmonic distortion is generally a matter of initial design. In the case of phase control devices, however, very little can be done in this respect, and the future is likely to see regulations so severe that other means of power control will become preferable. Moreover, future regulations, particularly those being prepared by the IEC (International Electrotechnical Commission), will undoubtedly cover equipment unaffected by the present regulations, e.g. television receivers and hi-fi equipment.

Designers would therefore be wise to anticipate such regulations now, and to make every effort to reduce the harmonic distortion produced by their equipment. To this end we offer the following guidelines, which we hope will provide a basis for future design. We must emphasise that the circuits given below are still under development, and serve merely to illustrate a worthwhile approach to the problems.

We shall divide our discussion into two parts, namely power levels up to 150 W and, power levels up to 1000 W.

Power levels up to 150 W

Power levels of 150 W are typical of those used in the power supplies of colour television receivers, hi-fi equipment, video recorders etc. A simplified circuit of such a power supply (incorporating a bridge rectifier) is shown in Fig.5.

A significant reduction in harmonic content of the mains current I_m can only be attained by increase of the opening time t_o (i.e. the time within one half cycle during which the rectified mains current is non-zero). This can be achieved by using a larger input choke L_I. Table 3 shows the relation between harmonic content and opening time for various values of total inductance L_t. It is evident from the table that harmonic content is suppressed significantly by increase of choke inductance, although in the case of the third harmonic relatively high inductance values are needed.

Note: reducing the bridge capacitance may also effect some reduction of harmonic content, but in reality the improvement is negligible and is more than offset by the effects of increased ripple.

In applications where cost and space are important considerations, large input chokes are not always practical. A possible alternative would then be to make use of an inverter, and to ensure by appropriate control of the supply that the inverter presents a constant impedance to the mains.

TABLE 3

Calculated harmonic content produced by the bridge rectifier circuit of Fig.5. L_t comprises 0.8 mH mains inductance, the inductance of the input choke L_I and the inductance of the r.f.i. coil.

L_t (mH)	1.5	3	6	12	24	48	96
$\hat{I}_m$ (A)	3.48	3.25	2.86	2.46	2.06	1.65	1.42
t_o (s)	2.34	2.55	2.92	3.41	4.04	4.78	5.63
V_{min} (V)	285	285	285	282	276	267	255
P_o (W)	148	148	148	147	143	136	126
H_3 (%)	0.24	0.24	0.23	0.21	0.19	0.16	0.13
H_5 (%)	0.31	0.29	0.26	0.21	0.16	0.10	0.05
H_7 (%)	0.31	0.27	0.22	0.14	0.08	0.04	0.04
H_9 (%)	0.24	0.20	0.12	0.06	0.05	0.05	0.03
H_{11} (%)	0.14	0.09	0.05	0.06	0.05	0.03	0.02
H_{13} (%)	0.03	0.03	0.07	0.06	0.03	0.03	0.03
H_{15} (%)	0.05	0.07	0.07	0.04	0.04	0.02	0.02

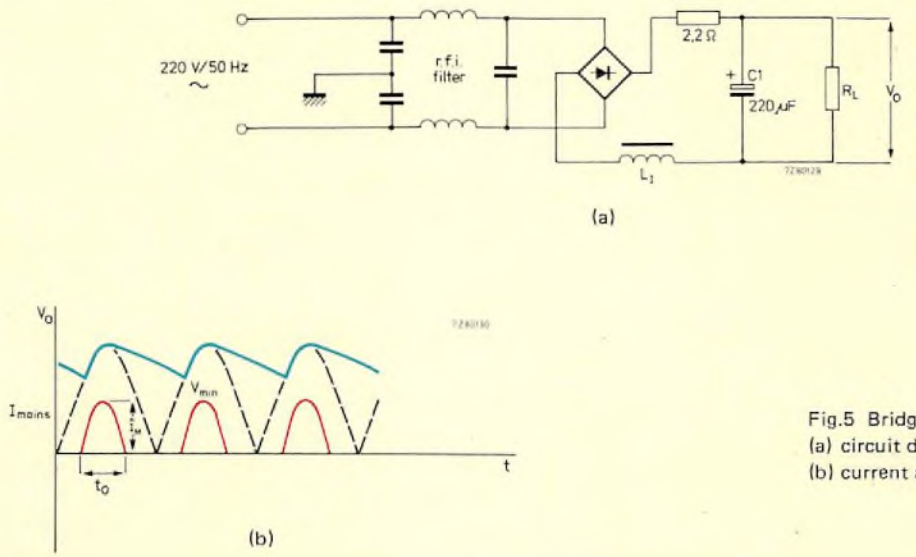


Fig.5 Bridge rectifier with r.f.i. filter;
(a) circuit diagram,
(b) current and voltage waveforms

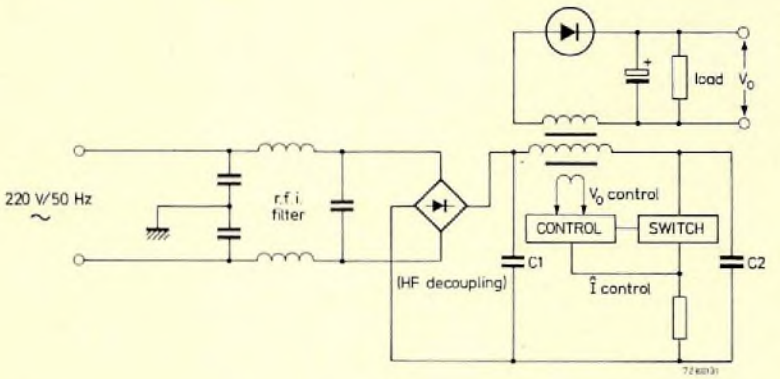


Fig.6 Basic circuit of an h.f.-converter which presents a constant impedance to the mains. Use is made of the transformer leakage inductance in combination with C_2 to produce a tuned flyback circuit which is able to withstand open or short circuit output conditions without radical change of characteristics

Power levels up to 1000 W

Power levels of 1000 W are typical of those employed in the supply of HF-converters, used, for example, in electronically controlled microwave ovens, inductive heating appliances and some small industrial appliances. In the case of bridge rectifier inputs incorporating buffer capacitors, the recommendations of CENELEC can be met only if the power does not exceed 500 W. This power can be increased to about 600 W by insertion of a choke-input filter.

The problem of harmonic distortion in HF-converters is overcome to a great extent by appropriate design of the converter to ensure that it presents a constant

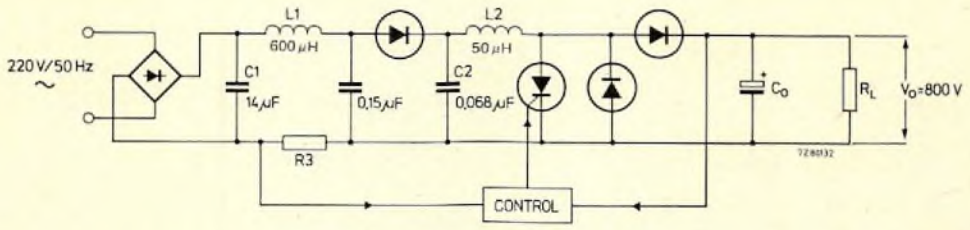


Fig.7 Simplified circuit diagram of an experimental up-converter. The thyristor/diode combination operates in a pulse mode. During the conduction phase, input energy is stored in L_1. This stored energy then serves to augment the input energy that transfers directly to the output during the non-conduction phase of the thrystor/diode combination

impedance to the mains. A simplified circuit for such a converter is shown in Fig.6. If smoothing of the 100 Hz output ripple is necessary, an extra electronic buffer stage must be incorporated. However, in the case of heating or motor control, i.e. loads with high time constants, smoothing is unnecessary.

Another way of reducing harmonic distortion under high power conditions is by using an up-converter, a circuit diagram of which is shown in Fig.7. This circuit is also ideally suited to serve as an electronic buffer stage (see above).

If L_1 (see Fig.7) is provided with secondary windings, the output can be isolated from the mains supply, and additional output levels can be obtained.

The mains current waveform produced by an experimental up-converter is shown in Fig.8 for an effective output power of 1000 W.

A major part of the current modulation is caused by the h.f. decoupling capacitor C_1 which is excited by the disturbed input voltage. C_1 should accordingly be as small as possible to minimise distortion of the mains current waveform. However, C_1 also induces h.f. voltage variations in the mains supply, which increase as the capacitance is reduced. Thus, although these voltage variations can be attenuated by an r.f.i. filter, they do place a lower limit on C_1 so that its value must always be a compromise.

The effect of the decoupling capacitor on the disturbed mains is shown more clearly in Fig.9 where the up-converter is replaced by a pure resistive load for an output power of 500 W (p. 90).

In Fig.10 mains harmonic distortion produced by an up-converter employing an r.f.i. filter is compared with that produced by a pure resistive load. The differences are very small and in both cases the harmonic content lies well below the CENELEC recommendations.

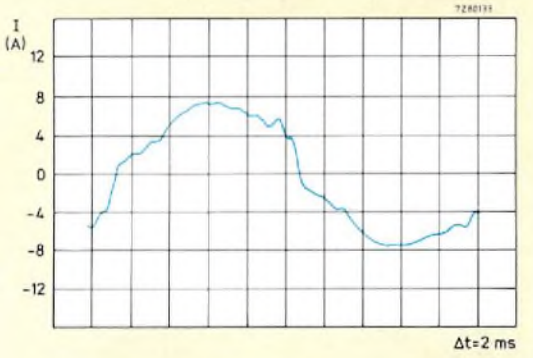
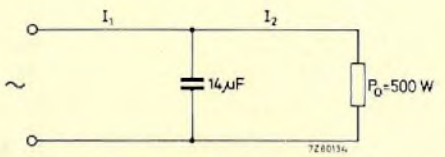


Fig.8 Mains current waveform produced by an experimental up-converter with an effective output power of 1000 W

CONCLUSIONS

As we have indicated, judicious design of electronic circuitry can go a long way towards reducing harmonic distortion of the mains supply. The solutions given here are in no way definitive, and must be regarded merely as a basis for future effort. By anticipating the problems the designer can seek to minimise them before his equipment is made available to the consumer. In this way harmonic distortion may be maintained at tolerable levels, to the obvious benefit of consumer and supplier alike.



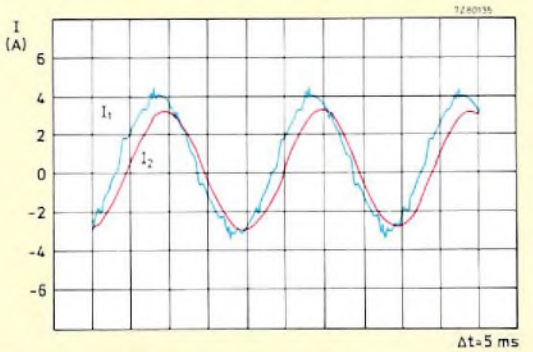
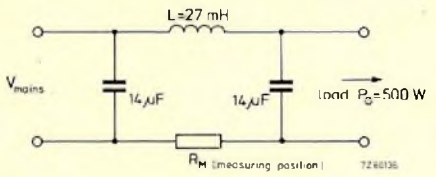


Fig.9 Extra currents induced in the mains by a disturbed input mains voltage acting on a pure resistive load with decoupling capacitor



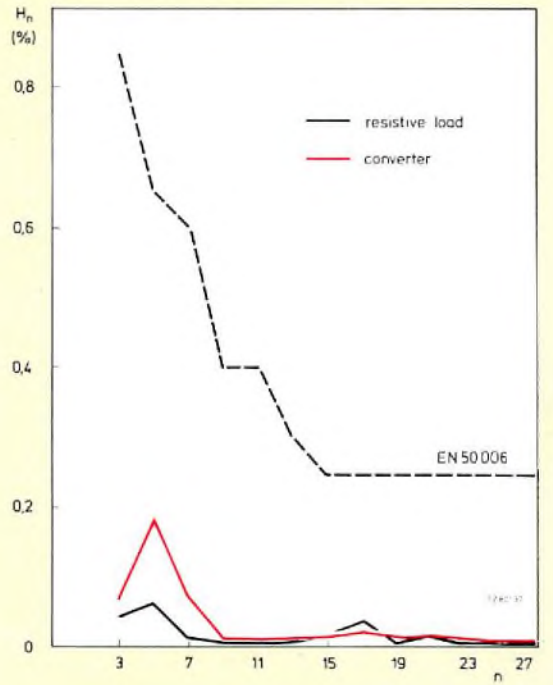


Fig.10 Comparison between the harmonic content of the mains produced by an up-converter and that produced by a pure resistive load

Versatile LSI frequency synthesiser system

T. G. GILES

INTRODUCTION

Frequency synthesisers have now been used for a number of years for the generation and stabilisation of operating frequencies in h.f. and military radio communications equipment. In such relatively expensive systems, the high cost of the conventional frequency synthesiser is not prohibitive. At the low-cost end of the communications market (v.h.f. mobile radios for instance), quartz crystals have traditionally been used for frequency stabilisation. The quartz crystal offers simplicity, reliability, a clean output, and high stability, but there are a number of disadvantages. First, two crystals are needed per channel (which leads to a large number of crystals in a multi-channel set). Second, each frequency needs its own unique crystal (causing major problems of stock control and delays in fitting new channels in a transceiver). Finally, there are many tuning operations required during the production of a transceiver built in this way and, in recent years, the cost of crystals has risen sharply.

The HEF4750 and HEF4751* ICs described here form the basis for a simply constructed "universal", single-loop phase-locked frequency synthesiser suitable for professional and military equipment. Moreover, the ICs replace the large number of SSI and MSI devices currently used in frequency synthesisers, and therefore now make the use of frequency synthesisers in low-cost equipment a realistic proposition. The two ICs enable mobile radio manufacturers to design transceivers which can work on one or any number of channels in a given band, using a single common reference crystal, thus dispensing with the cost and delays in ordering individual crystals for each frequency.

Historically, the design of a synthesiser to meet the stringent CEPT specifications has been complicated and has required a great deal of expensive screening and decoupling to keep down spurious outputs. The two new ICs simplify the design of high-performance synthesisers by putting all the critical parts of the circuit, both analogue and digital, within the packages. The ICs offer considerable flexibility: the synthesiser is programmable, compatible with microprocessor-based and other digital systems, and suitable for remotely-controlled transmitters, scanner receivers, frequency-agile systems, etc. This flexibility also means that the synthesiser does not have to be built for a specific system; a single design can be programmed to suit most applications. An additional benefit, derived from the use of LOCMOS in the ICs, is the low current consumption which can be an important factor in some applications.

A summary of the performance of a typical frequency synthesiser suitable for use in a mobile radio is given in Table 1.

THE SINGLE-LOOP PHASE-LOCKED FREQUENCY SYNTHESISER

From the point of view of simplicity, cost, and purity of output signal, the most attractive type of frequency synthesiser is the single-loop phase-locked design shown

*The type numbers HEF4750 and HEF4751 are now assigned to the frequency synthesiser ICs which were previously allocated development type numbers LN123 and LN124 respectively.

TABLE 1

Typical performance of a high-band v.h.f. synthesiser (155 MHz, 12.5 kHz steps)

Parameter	Measurements
In-band residual f.m. (300 Hz to 3 kHz)	<3 Hz
Noise at ±12.5 kHz in 1 Hz bandwidth	≈ −120 dBC
Discrete spurious signals at ±12.5 kHz	−95 dBC
Switching time for 1 MHz change	<4 ms
Modulation bandwidth for 3 kHz deviation	50 Hz to 4 kHz ±1 dB
Modulation distortion for 3 kHz deviation	<2%
Current consumption	36 mA

as a block diagram in Fig.1. The output signal at frequency f_o from the voltage-controlled oscillator (VCO) is phase-compared with a stable fixed reference frequency f_r after being divided by a programmable ratio N. Any frequency or phase error detected in the phase comparator corrects the VCO frequency until a stable phase-locked condition is achieved. We then have the condition:

$$f_o = Nf_r.$$

Figure 2 is a simplified block diagram of the HEF4750/4751 system. A further programmable divider is added; this increases the flexibility of the system because it enables reference to be obtained from a range of crystal frequencies. The reference frequency is now defined as:

$$f_r = \frac{f_{crystal}}{M}.$$

The dividers are programmed to the correct division ratio via the digital inputs so the synthesiser is compatible with microprocessor-based or other simple digital control systems. The reference divider is normally used for determining step size (usually channel spacing, 12.5 kHz for instance) and the output frequency is set by a suitable value of N. The division ratio N is usually an integer but under certain circumstances, discussed later, it is useful for N to contain a fraction.

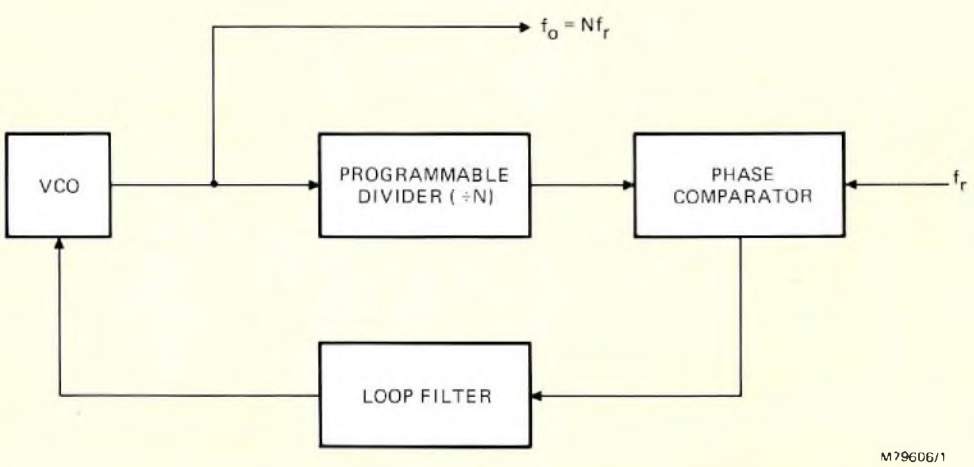


Fig.1 Basic single-loop phase-locked frequency synthesiser

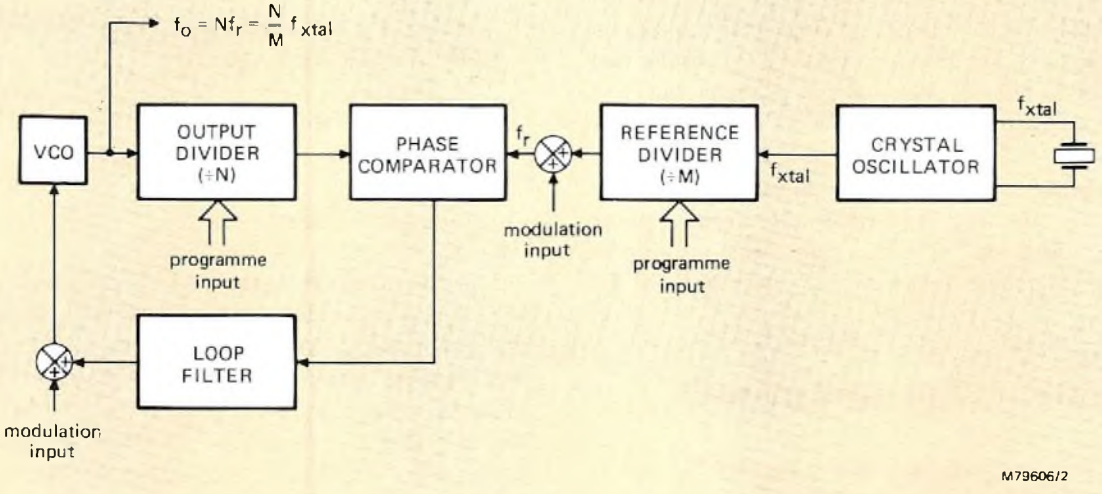


Fig.2 Basic frequency synthesiser with added programmable reference divider

The advantages of the single-loop type of frequency synthesiser are briefly:

- simplicity
- low cost
- any frequency can be obtained without altering the basic circuit
- it is potentially the purest type of frequency synthesiser
- only one crystal is required and its frequency is not dictated by the output frequency.

The reason that the single-loop synthesiser is potentially the purest type of synthesiser is because it has the smallest number of possible spurious frequencies present. Unfortunately it suffers from the disadvantage that the large division ratio (typically 10 000 for a v.h.f. mobile radio) reduces a phase error at the VCO output to a very small value by the time it reaches the phase comparator. To achieve satisfactory control, it is necessary to have a high gain after the phase comparator. This means that any noise generated in the comparator will be amplified and applied to the VCO, producing a noisy output signal. One way to remove these unwanted signals is to use a very narrow bandwidth in the control loop but this leads to slow synthesiser operation, long settling times when changing frequency, and no protection against VCO microphony.

It is possible, however, to design a single-loop synthesiser to overcome these difficulties and provide a good dynamic performance over a wide frequency range (Ref.1). The HEF4750 and HEF4751 employ a special high-gain phase comparator which has an effective gain of about 3 kV/cycle (compared with about 10 V/cycle for conventional phase comparators). The gain in the loop can then be reduced, or an attenuator can be used, to achieve a high loop bandwidth. The phase comparator is a low-noise circuit and, because it works on a sample-and-hold principle, it has a low level of spurious output. This, combined with the low-loop-gain requirements, makes low noise, low spurious output synthesisers easy to construct. Other features have been incorporated to give rapid switching between channels for frequency-agile systems.

The HEF4751 universal divider IC is a versatile programmable divider for use with or without external prescalers. It incorporates facilities for providing decimal and fractional channel selection, transmit/receive frequency offsets, optional half-channel offset, and rapid switching between channels. Programming is performed by a self-addressing multiplex technique which is compatible with PROM, diode matrix, or BCD-coded switch inputs.

Cost and selection of components

At the present time the true cost of active electronic components such as ICs is steadily dropping, but mechanical assemblies like screening boxes are becoming more expensive and more difficult to include as equipment gets smaller.

The choice of components for use in a frequency synthesiser has to be very carefully considered in terms of their electromagnetic compatibility (EMC) both within the phase-locked loop and with the other components in the equipment. Two types of logic, ECL and LOCMOS, offer potentially the simplest configuration and are

likely to have the best EMC. They are both symmetrical logic (when one transistor switches on, a similar transistor switches off), and so there are no large current pulses on their supply lines. The extremely low power consumption of LOCMOS reduces electromagnetic radiation and makes decoupling easier. The HEF4750/4751 synthesiser system is therefore based on LOCMOS LSI for as much of the circuitry as possible, and small ECL prescalers are used where required. A further advantage of using LOCMOS technology is that it has been possible to combine high-quality linear circuitry with logic in the same IC.

The HEF4750/4751 frequency synthesiser system

Figure 3 is a block diagram of the two ICs in a v.h.f. frequency synthesiser system. The ICs can be used for digital frequency synthesisers in all communications, instrumentation, tv and broadcast applications, and the general circuit shown in Fig.3 offers the following advantages.

- A wide choice of reference frequency using a single crystal.
- A high-performance phase comparator with low phase noise and low spurious signal level.
- System operation to over 1 GHz.
- Assured 18 MHz input at 10 V (HEF4751VD-1 version).
- Flexible programming with frequency offset and fractional channel capability.
- A programme range of 6½ decades including up to 3 decades of prescaler control.
- Division range extension by cascading.
- A built-in phase modulator.
- A fast-lock feature.
- A foolproof out-of-lock indication.
- Non-critical mechanical and electrical layout.
- Low power dissipation and high noise immunity.

The out-of-lock indication can be used to mute transmission when the reference crystal or either divider fails, or when the loop loses lock as happens temporarily, for instance, when switching from one frequency to another. This is important because of statutory regulations which require that off-frequency signals are not radiated from a transmitter.

THE HEF4750 FREQUENCY SYNTHESISER IC

Figure 4 shows the internal configuration of the HEF4750. The device contains five main circuit blocks: phase comparator PC1, phase comparator PC2, phase modulator, reference divider, and reference oscillator.

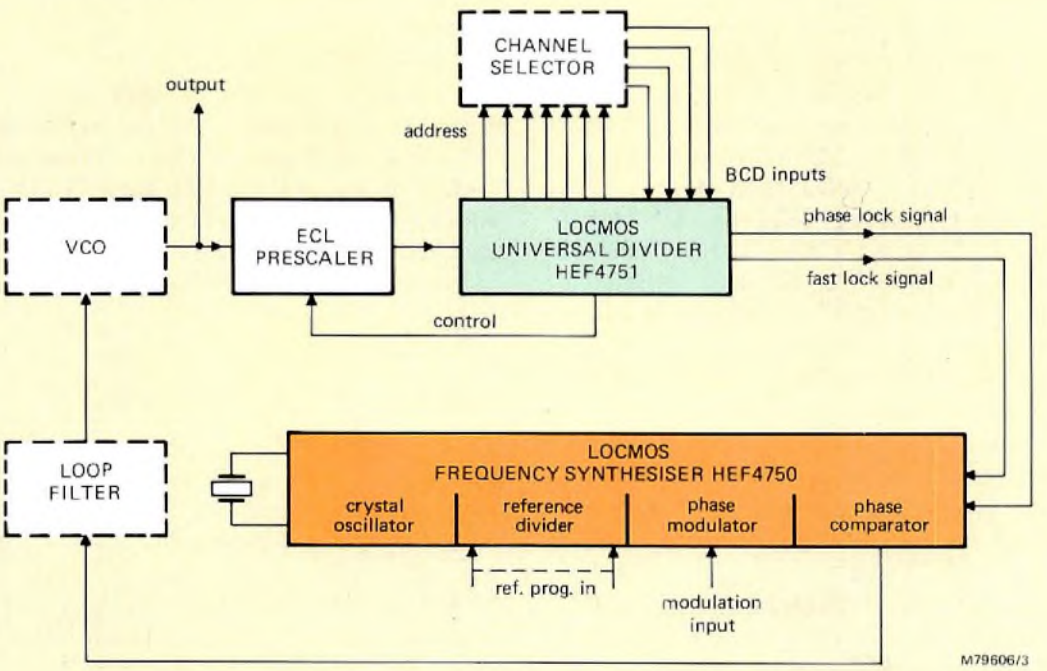


Fig.3 HEF4750/4751 frequency synthesiser system

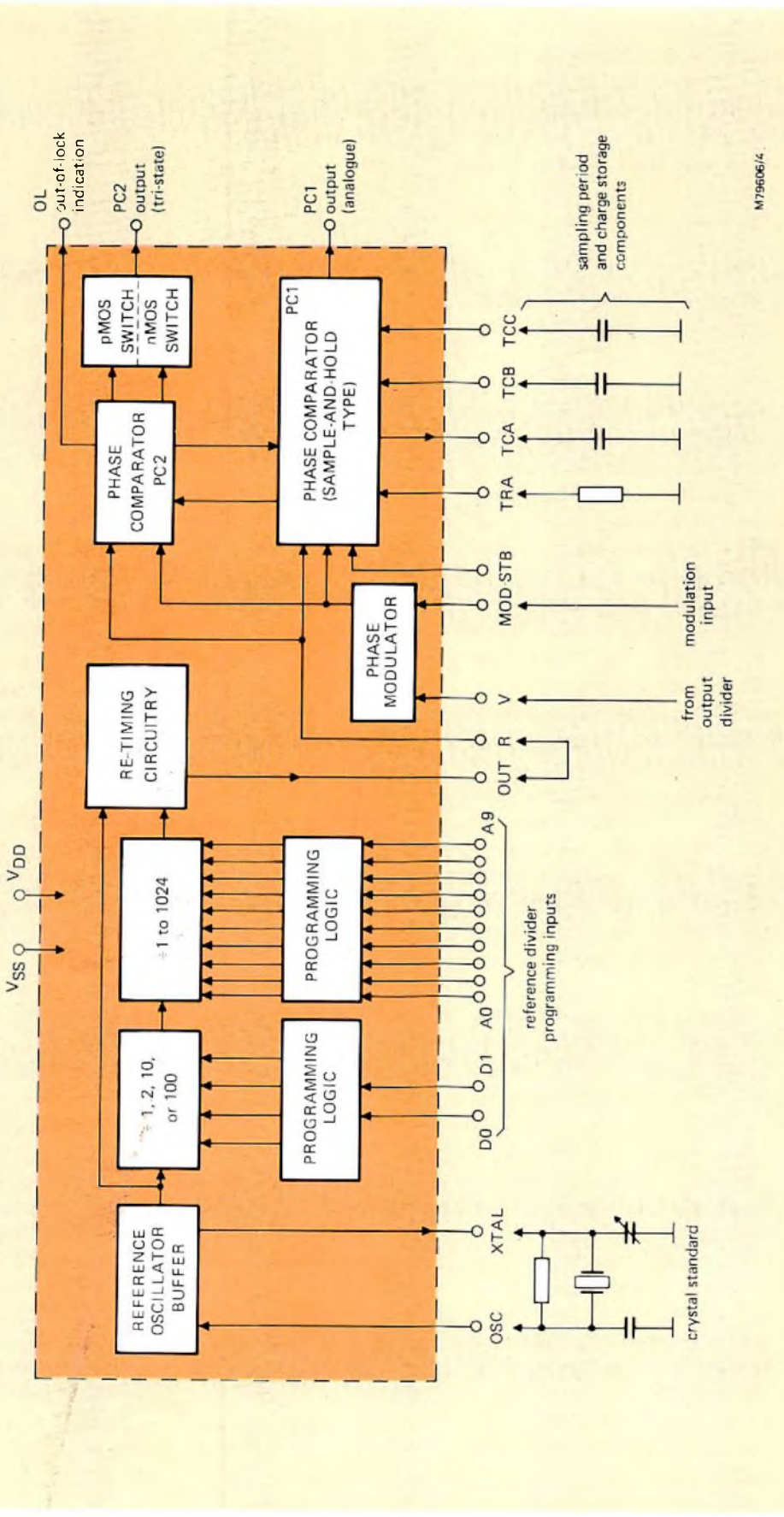


Fig.4 Organisation of the HEF4750 frequency synthesiser IC

Phase comparators

The in-band noise output from a frequency synthesiser is proportional to $N/K_pF(S)$, where K_p is the phase comparator gain constant and F(S) is the transfer function of the loop filter. In a v.h.f. or u.h.f. single-loop frequency synthesiser, the division ratio N is very large, typically 10 000, and so gives rise to a great deal of noise on the output signal. There are two obvious ways of reducing this noise:

1) reduce N by using a mixer or multiple loop system,
2) reduce the loop bandwidth by increasing the filtering effect of F(S).

The first solution is costly because it means a more complex system and probably more components. It is also less flexible; that is, different designs will be needed for different frequency ranges. Reducing the loop bandwidth, on the other hand, gives poor loop performance characteristics such as long settling time and inadequate protection against VCO microphony, etc.

An alternative solution to the problem has been provided by Dr M.J. Underhill and his team at Philips Research Laboratory at Redhill, U.K. They have developed a phase comparator with a very high gain K_p, reducing the in-band noise without the disadvantages of solutions (1) and (2). This patent phase comparator has been incorporated into the HEF4750 (PC1 in Fig.4) and can be set to any value of gain required. A typical value is 3 kV/cycle (477 V/radian). The phase comparator works on the sample-and-hold principle with double sampling and therefore is not only a low-noise circuit but also has a very low level of reference breakthrough and other spurious outputs. The low noise and high gain enable a wide loop bandwidth to be used without a reduction in division ratio N.

A second, more conventional, digital phase/frequency comparator (PC2 in Fig.4) has been included to provide very rapid switching between channels. This is done by summing the PC2 output into the loop filter integrator at a very high gain. When the VCO is off-frequency, this will rapidly bring the system to within a few degrees of phase lock, at which point the PC2 output is inhibited by the P-MOS N-MOS switch, and the loop is locked in by the main high-performance comparator PC1. Noise and spurious signals from PC2 are not important because this circuit is inhibited under steady-state conditions.

Phase comparator PC2 produces positive-going or negative-going output pulses of variable width, depending on the phase relationships of the two inputs. These pulses are integrated in the loop filter to produce a ramp between about 0 and 10 V for $\pm 360^\circ$ phase difference at the inputs. The gap in the characteristic of PC2 in which only PC1 operates is caused by the tristate output of PC2 being switched to the high-impedance condition.

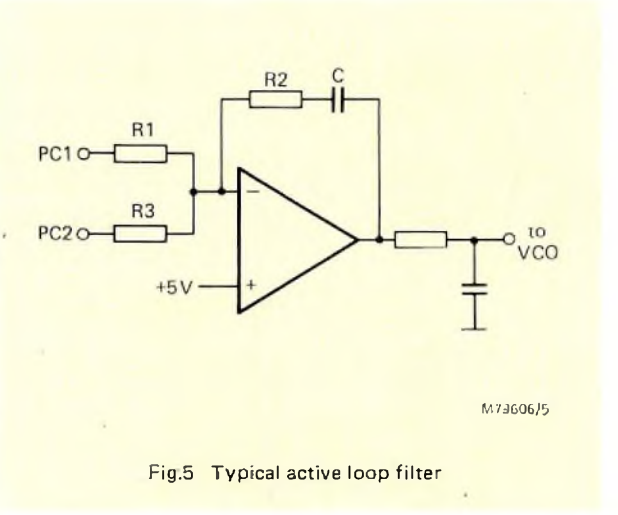


Fig.5 Typical active loop filter

This facility, with the connections shown in Fig.5, provides the high loop-locking speed of the IC. The loop filter constants, including R_1, are calculated for normal (PC1) operation. Resistor R_3 should be chosen to be much smaller than R_1 to pass a large amount of current to or from the integrator during the initial rapid locking-in period. A value of R_3 between 1 and 10% of R_1 gives satisfactory performance, but if the value of R_3 is too small the system can become oscillatory and not settle on to the region where only PC1 operates.

Both phase comparators increase their output voltages as the signal from the output divider V leads the input from the reference divider R. The loop filter shown in Fig.5 inverts the input from the phase comparators which ensures correct operation of the loop in the normal case where the VCO increases in frequency with increasing control voltage. Where a passive loop filter is used, the phase of the comparators can be reversed by interchanging the R and V inputs to the IC.

The main phase comparator PC1 is based on a sample-and-hold technique and uses both linear and digital circuitry. The gain of the phase comparator is controlled by a resistor TRA and capacitor TCA external to the IC (Fig.4). A gain of about 3 kV/cycle is suitable for most applications. Capacitor TCB provides an internal delay and the modulator ramp. Its value is not critical but is typically half that of TCA. Capacitor TCC is the hold capacitor for the sample-and-hold circuit. Again its value is not critical, and in most systems it will be within the range 1 to 100 nF. It must be a low-leakage type, but the important consideration is that when combined with the driving impedance of about 400 Ω it does not cause excessive phase shift which could lead to loop instability. Normally, no difficulties should be experienced if the time-constant is less than 10% of the slow reference frequency period.

The strobe input (STB in Fig.4) is driven by the slow reference frequency FS from the HEF4751, but in the case where the counter C_3 in the HEF4751 is set to 1, the V and STB inputs are at the same frequency. Note that the R, V, and STB inputs are all negative-edge triggered. If the phase comparators are driven from a divider other than the HEF4751 IC, care must be taken to ensure that the negative-going edges have no phase jitter.

An out-of-lock indication is provided as a transmitter mute or fault indicator. In addition to its function as an out-of-lock indicator, this signal also indicates if the phase error at the comparator is more than a preset number of degrees, or if the reference oscillator/divider, prescaler, or main programmable dividers have failed.

Reference oscillator

The crystal oscillator maintaining circuit built into the IC needs an external bias resistor of between 10 kΩ and 10 MΩ connected between the the XTAL and OSC pins. The reference crystal, connected between the same pins, can be any parallel resonant fundamental mode crystal in the range 10 kHz to 15 MHz. Two external loading capacitors are also required, connected as shown in Fig.6.

The power limiting resistor, also shown in Fig.6, is provided to prevent the oscillator from overdriving the crystal which would otherwise happen in certain circumstances. (The resistor should not exceed 2.7 kΩ for reliable operation.) Crystal overdrive can cause the crystal dissipation to increase and lead to drift and excessive radiation from the oscillator to the rest of the synthesiser.

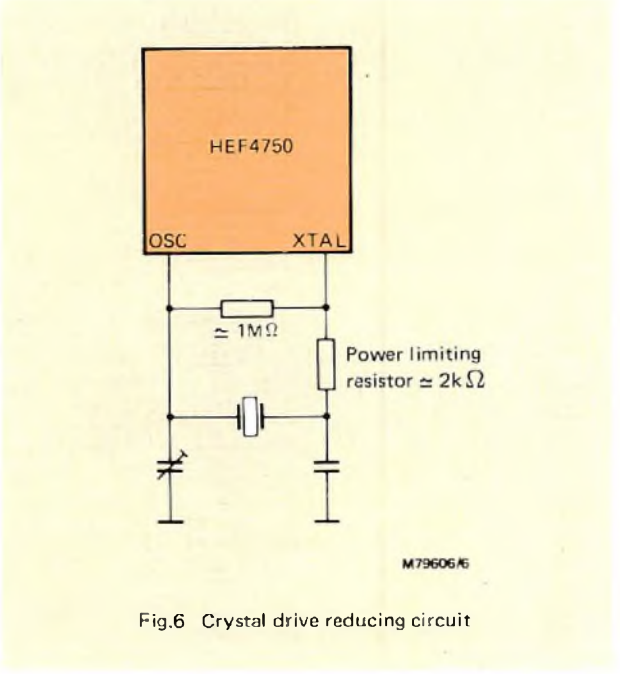


Fig.6 Crystal drive reducing circuit

An independent external reference frequency can be used by the synthesiser IC if a suitable signal is available. In this case, the oscillator maintaining circuit in the IC is connected as a buffer amplifier; only the bias resistor is needed and the reference signal can be a.c.-coupled to pin OSC. A signal of 500 mV rms should ensure sufficient drive to the reference divider. If a logic-level reference signal is available, the bias resistor and coupling capacitor are not required. The maximum external reference frequency is 20 MHz.

Reference divider

The reference divider consists of a binary divider with a programmable division ratio of 1 to 1024 and a prescaler with selectable ratios of 1, 2, 10, and 100. In this way, suitable comparison frequencies can be obtained from a range of crystal frequencies. The divider can also be used as a "stand-alone" programmable divider.

The division ratio of the programmable divider is set by the binary code on pins A_0 (LSB) to A_9 (MSB) so that if, for instance, all ten pins were linked to the positive supply rail (V_{DD}, +10 V) the divider would be set to divide by 1023. The zero input condition (all pins connected to 0 V) sets the counter to 1024. The prescaler ratio is set as shown in Table 2.

TABLE 2

Prescaler control

Input pins D1	Input pins D0	Prescaler ratio
0	0	1
0	1	2
1	0	10
1	1	100

1 = V_{DD} (+10 V) 0 = V_{SS} (0 V)

Phase modulator

A time delay phase modulator in the IC enables either frequency or phase modulation to be obtained with a minimum of external components. Its gain and other characteristics can be set by an external capacitor.

The modulating signal is typically applied to both the VCO loop and the on-chip modulator (two-point modulation, as shown in Fig.2). This gives essentially constant modulation sensitivity, irrespective of loop

bandwidth, and practically eliminates the spurious signals often associated with synthesiser modulation. The loop bandwidth may then be chosen to suit other requirements. The application of two-point modulation to phase-locked loop frequency synthesisers is discussed in Ref.2.

Retiming circuit

The frequency synthesiser circuits are edge-controlled and thus it is important that there is no jitter. The retiming circuit synchronises the divided-down reference signal with the oscillator output.

THE HEF4751 UNIVERSAL DIVIDER IC

The HEF4751 is a novel programmable divider and control IC with an input frequency of 9 MHz at 10 V supply voltage (18 MHz for the HEF4751VD-1). The system can provide a maximum of 6½ decades up to an input frequency of 4.5 GHz (9 GHz for the HEF4751VD-1) with suitable external prescalers.

Multiple feedback division

The HEF4751 is based on a multiple feedback dividing principle which is a development of the conventional swallow counting technique. It enables a combination of internal and external prescalers to be cascaded to form a divider of any size. Decimal and fractional division can be used in the same counter.

A block diagram of the basic divider is shown in Fig.7.

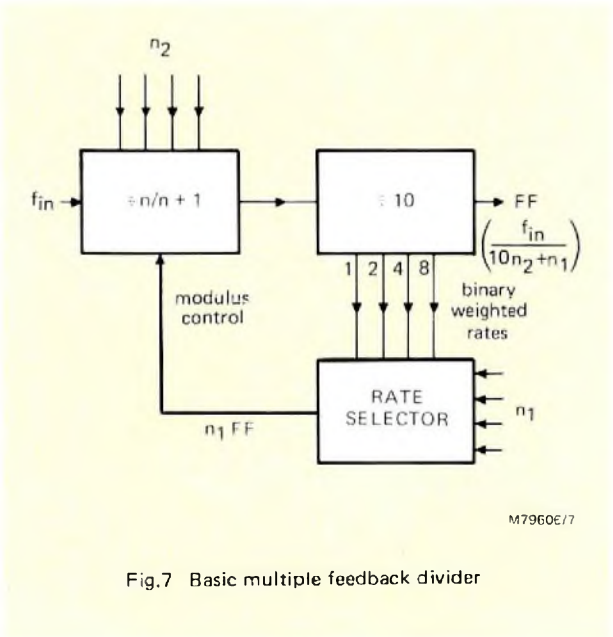


Fig.7 Basic multiple feedback divider

It consists of three stages. The first is a fully programmable 4-bit counter which can be set to any number from 1 to 9; its division ratio is increased by 1 when a pulse is applied to a control input. The second stage is a fixed divide-by-ten counter that has four binary weighted rate outputs. These provide 1, 2, 4, or 8 pulses for each cycle of the counter output FF. The pulse streams do not have an even mark-to-space ratio but are designed to be non-overlapping. The third block is a rate selector which is a series of gates that will assemble a pulse stream made up of selected rate inputs. The frequency of the pulse stream at the rate selector output will be n_1FF, where n_1 is a number programmed into the selector to determine the selection of the rate inputs. The divide-by-ten circuit and the rate selector form a decimal rate multiplier.

Operation of the complete circuit is as follows. The n/(n+1) counter is programmed to divide by n_2 but will divide by n_2+1 for n_1 of the 10 states of the fixed counter. It will divide by n_2 for the remaining 10-n_1 cycles. Therefore, the total division ratio is given by:

$$N = (n_2+1)n_1 + n_2(10-n_1),$$

$$= 10n_2 + n_1.$$

The circuit is therefore a two-digit programmable divider where n_2 has the significance of tens and n_1 of units.

An alternative way of considering the multiple feedback divider is to regard the ÷n/(n+1) stage as a fixed ÷n stage preceded by a pulse swallow circuit, as shown in Fig.8. Each time a pulse is generated by the rate selector, one pulse in the input stream is swallowed, which is the same as increasing the division ratio by one. The frequency at the output of the divider is FF and so at the input of the ÷10 stage it must be 10FF. At the input to the ÷n stage, it will be 10FFn_2, and at the pulse swallower it will be 10FFn_2 plus the frequency n_1FF from the rate selector. Thus the input frequency is $(10n_2+n_1)$FF.

Operation of the universal divider IC

The multiple division technique can be extended by using the IC with any necessary external prescalers as shown in Figs.9 and 10. Fig.9 shows the internal configuration of the HEF4751, and Fig.10 is a pulse flow diagram of the HEF4751 connected with one external prescaler. Comparing Fig.10 with Fig.7, counter C_1 corresponds to the ÷n/(n+1) stage of Fig.7. Counter C_2 corresponds to the ÷10 stage, and rate selector RS_3 corresponds to the rate selector of Fig.7. Further stages C_{-1}, C_{0b}, and C_3 provide a cascaded divider with a division ratio f_{in}/FF of $(n_0/m) + n_1 + 10n_2 + 100n_3 + 1000n_4$ where n_0 to n_4 and m are programmable constants. The cascade can be extended in either direction by further external prescalers or HEF4751 ICs. The

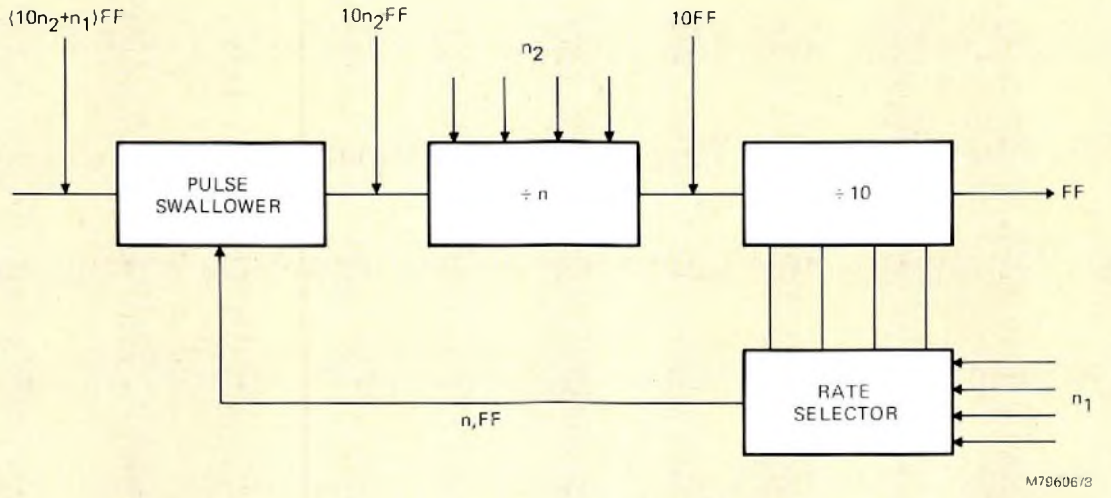


Fig.8 Alternative way of considering multiple feedback division

principles of operation remain the same and the operation of the circuit in Fig.10 is outlined below.

Counters C_{-1} to C_3 are cascaded to form the main programmable divider chain of the system. Counter C_{-1} is a fast ÷(10/11) prescaler external to the IC and counter C_{0b} is an internal (÷ 1, 2, 5, 10/11) counter programmed to work as a ÷(10/11) circuit (the programming is explained later). Counter C_1 is a fully-programmable 4-bit counter. Counter C_3 can be programmed to any value from 1 to 16. The output from the rate selector RS_0 is added to the rate from RS_1 to give a total division ratio which contains a fractional term n_0/m. The fractional term is very useful for simplifying the operation of the frequency synthesiser in some circumstances. For example, if a synthesiser with 12.5 kHz steps is required, FF can be set at 100 kHz and m at 8. Rate selection constant n_1 will then have the significance of hundreds of kilohertz, n_2 megahertz, n_3 tens of megahertz, and n_4 hundreds of megahertz. The rate selection constant n_0 will set the multiple of 12.5 kHz and thus will have the range 0 to 7 to select 12.5 kHz, 25 kHz, 37.5 kHz, etc. Alternatively, if m is set to 5, n_0 will give 20 kHz steps.

The fractional term n_0/m implies a phase jitter at FF. This can be removed either by the averaging effect of the loop, or by connecting the FS output to the strobe (STB) input of the HEF4750 IC.

Half-channel offset

A further extension, called half-channel offset, is provided by the 1-bit counter C_4 and the rate selector $RS_{½}$, shown in Fig.9. The circuit is inoperative when C_4 is set to 1, but when it is set to divide-by-two it supplies a timing signal to the 1-bit rate selector $RS_{½}$. The $RS_{½}$ output is summed into RS_0, as shown in Fig.9.

To illustrate the use of half-channel offset, take the condition where m is 10, C_4 is set to divide-by-two, and $RS_{½}$ is set to 1. From Figs.9 and 10, it can be seen that the overall division ratio from system input to output FF is given by the expression:

$$N = 2(½ + n_0 + 10n_1 + 10^2n_2 + 10^3n_3 + 10^4n_4).$$

The half-channel offset facility is used principally where radio channel allocation conforms to the expression;

$$f_o = f_{ch}(N + ½),$$

where f_o is the channel frequency, f_{ch} is the channel spacing, and N is an integer. In this case the frequency at output FS is $f_{ch}/2$, $RS_{½}$ supplies the half-channel term, and numbers n_0 to n_4 control the value of N in decimal form.

Programming

Programming is performed in a BCD parallel-bit serial decade format. To accommodate fixed or variable frequency offsets, two numbers are input in parallel, one being subtracted from the other in the IC to produce an internal programme. The decade selection address is generated by an internal programme counter which may be run continuously, or on demand, or may be synchronised to the HEF4751 output.

Figure 9 shows ten programmable blocks, four of which (C_{0b}, C_3, C_4 and $RS_{½}$) are concerned with the mode of counting. These four are programmed by a single number n_6 which is explained later. The other circuit

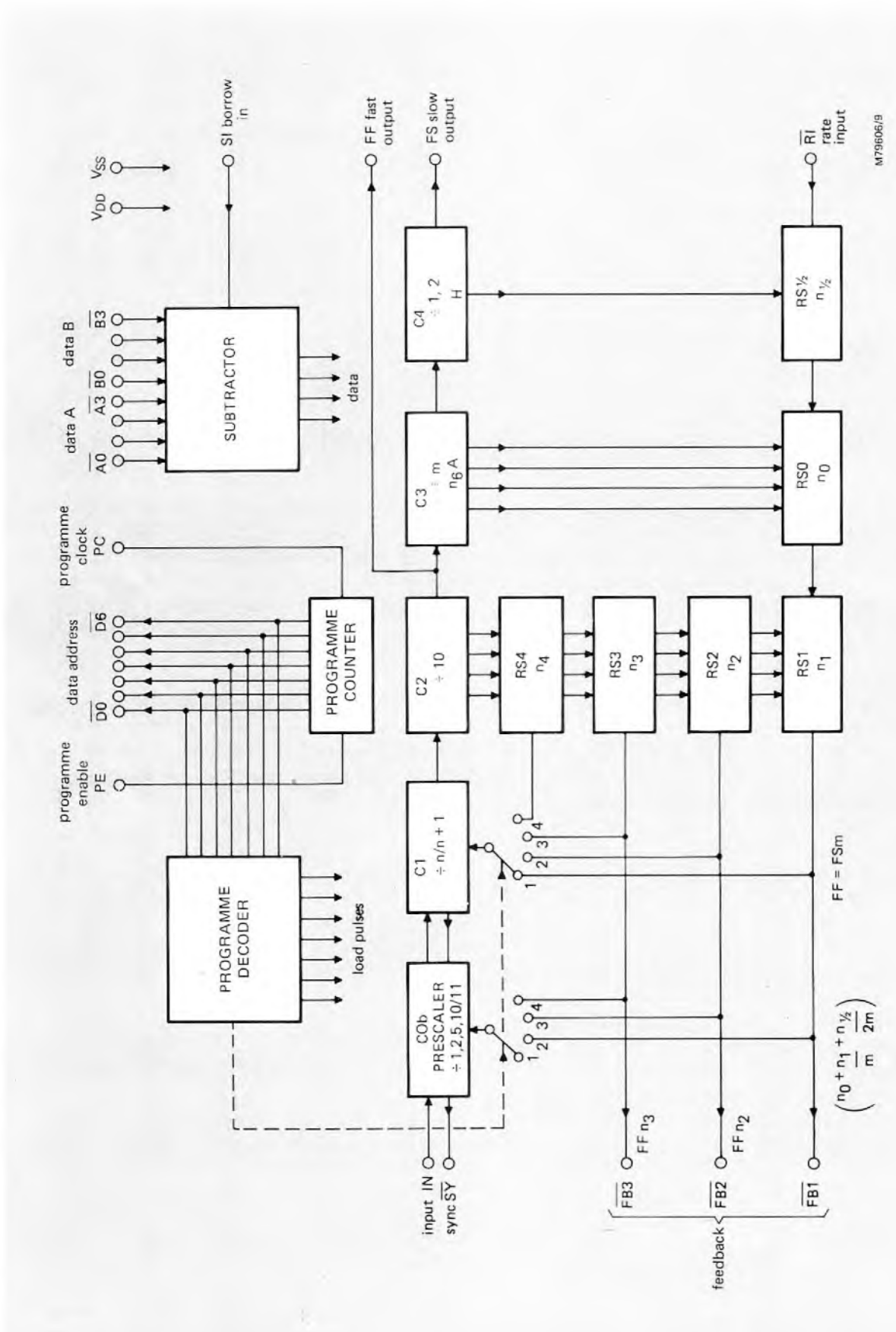


Fig.9 Organisation of the HEF4751 universal divider IC

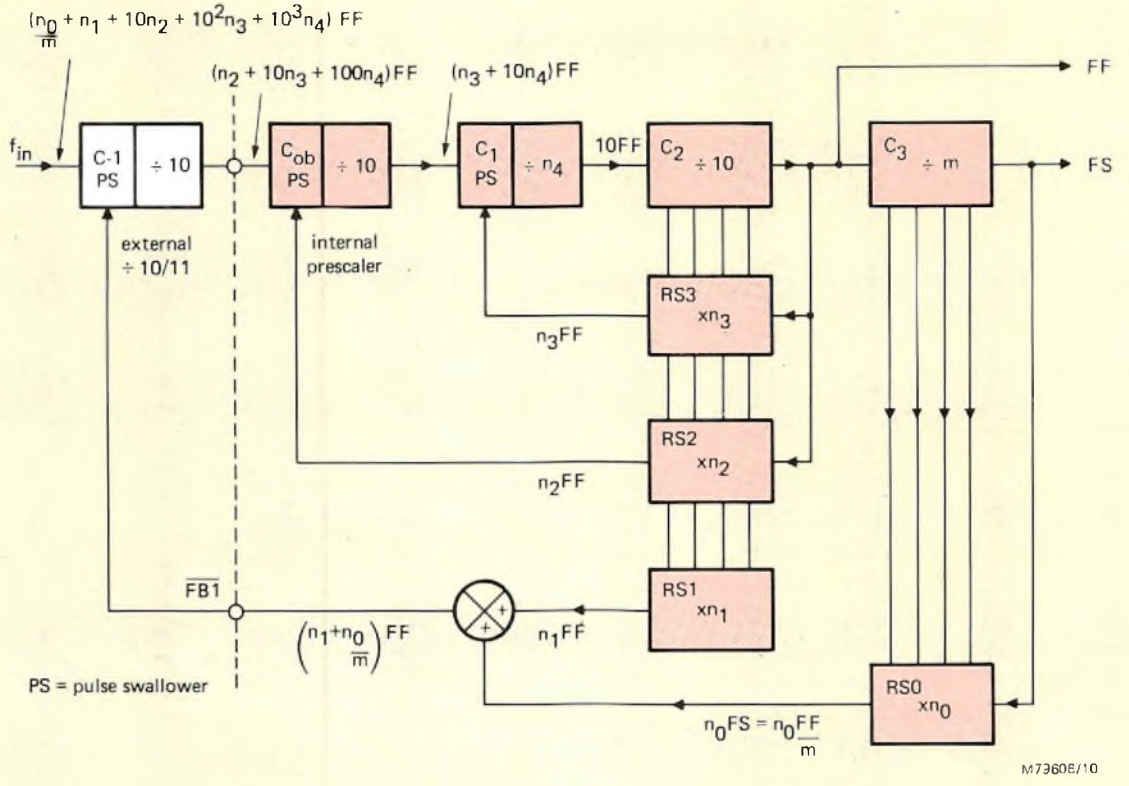


Fig.10 Pulse flow diagram of HEF4751 with one external prescaler

blocks (RS_0 to RS_4 and C_1) are programmed by six 4-bit numbers, generated internally from programme input n_0 to n_5. These represent a single number P which gives the overall division ratio (ignoring half-channel offset) of:

$$P = n_0 + m(n_1 + 10n_2 + 10^2n_3 + 10^3n_4 + 10^4n_5).$$

The complete division ratio from system input to FS is:

$$N = H(P + \tfrac{1}{2}).$$

The programme input consists of data applied to the Data A and Data B input pins of the IC. The programme assembled in the IC to set up the dividers has three components: Data A and Data B, each comprising six 4-bit numbers n_{0A} to n_{5A} and n_{0B} to n_{5B}, and a subtract input SI which is used when HEF4751 ICs are connected in cascade. These components are combined within the IC so that:

$$P - 10^5 b_{out}\, m = A - B - b_{in},$$

where:

$$A = n_{0A} + m(n_{1A} + 10n_{2A} + 10^2n_{3A} + 10^3n_{4A} + 10^4n_{5A}),$$

$$B = n_{0B} + m(n_{1B} + 10n_{2B} + 10^2n_{3B} + 10^3n_{4B} + 10^4n_{5B}),$$

b_{out} = borrow out (not used),

b_{in} = borrow in (at pin SI).

Data A and Data B numbers are entered sequentially into the two sets of four input pins $\overline{A0}$ to $\overline{A3}$ and $\overline{B0}$ to $\overline{B3}$.

The HEF4751 generates its own timing signals for this process which are output on pins $\overline{D0}$ to $\overline{D5}$. Pin $\overline{D0}$ goes LOW to signify the load time for n_{A0} and n_{0B}, $\overline{D1}$ goes LOW to indicate the load time for n_{1A} and n_{1B}, and so on.

As the internal numbers are generated, they are stored and applied to the appropriate circuit block as shown in Table 3. The numbers n_0 to n_4 are applied to the rate selectors RS_0 to RS_4 respectively. The programme number for C_1 does not have a fixed position in the internal programme, the most significant non-zero internal number is selected as programme input to C_1. A leading zero detector identifies this number, which may be any of the internal numbers n_2 to n_5, and at the same

TABLE 3

HEF4751 programme loading

	n_5	n_4	n_3	n_2	n_1	n_0
Data A	0	7	6	1	1	8
Data B	0	0	0	8	5	6
	↓	↓	↓ ↙	↓ ↙	↓	↓
Internal programme	0	7	5	2	6	2
		↓	↓	↓	↓	↓
Destination		C_1	RS_3	RS_2	RS_1	RS_0

↙ borrow

time sets the rate selector output switching circuits, shown in Fig.9, to give the optimum configuration for the universal divider. This involves ensuring that the second most significant number is used as feedback for C_1, and the next most significant as the feedback to C_{0b}. If several external prescalers are being used, FB1 must be connected to the first one, FB2 to the second (if present), and FB3 to the third (if present). Table 3 is an example of the assembling of the internal programme. This example would set the configuration shown in Fig.10: RS_3 output enables C_1, RS_2 output controls C_{0b}, and RS_1 and RS_0 outputs control a prescaler via $\overline{FB1}$.

The other programmable circuit blocks in the IC are programmed by the 8-bit control number n_6, read in when $\overline{D6}$ goes LOW. The four bits entered at the Data A inputs $\overline{A0}$ to $\overline{A3}$ are interpreted as the division ratio m for counter C_3. The inputs are interpreted in active LOW binary code except that a zero input ($\overline{A0}$ to $\overline{A3}$ HIGH) sets m to 16. The Data B bits have the following significance:

$\overline{B0}$ enables C_4,

$\overline{B1}$ controls $RS_{½}$,

$\overline{B2}$ and $\overline{B3}$ are the control inputs for C_{0b}.

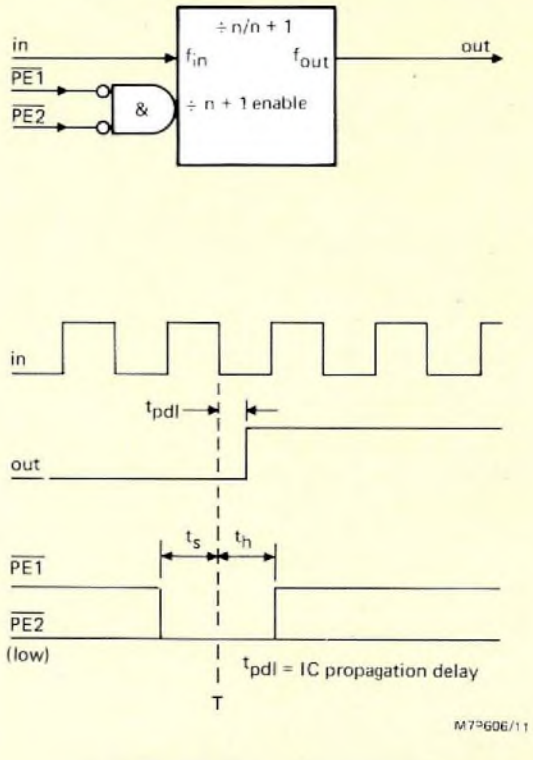


Fig.11 Typical dual modulus prescaler

INTERCONNECTIONS

Fast prescalers

A fast dual-modulus counter is shown preceding the HEF4751 IC in Fig.10. The swallow action is controlled by signals generated within the IC. Since the speed of the IC is limited, care is needed in the timing of the control signals.

Consider the typical dual-modulus counter shown in Fig.11. The counter normally divides by n, but when the control $\overline{PE}$ is LOW the counter divides by n+1. The signal $\overline{PE}$ is the OR function of $\overline{PE1}$ and $\overline{PE2}$. The timing rules for $\overline{PE1}$ and $\overline{PE2}$ are identical. In the timing diagram shown in Fig.11, $\overline{PE2}$ is permanently LOW; therefore, the swallow action is enabled when $\overline{PE1}$ is LOW. The value of $\overline{PE1}$ must then be correct for a time t_s (set-up time) before, and t_h (hold time), after, time T. The propagation delay time t_{pdl} of the counter is also shown.

Since the set-up time and propagation delay are small

compared with an output period, most of the output period is available for making a decision on the next value of $\overline{PE1}$. For correct operation the output period must be greater than the sum of t_s and t_d, the latter being the decision time.

The decision is made within the IC, and the result is output as two separate signals both of which are referred to a basic timing period consisting of the period between outputs of counter C_3. The first signal is generated on pin $\overline{SY}$ (sync). This is a LOW pulse with a duration of one period of the input at pin IN of the IC. This signal is always present, regardless of the divider program. Its purpose is to time the $\overline{PE}$ input of the prescaler, and the delay from IN to $\overline{SY}$ is therefore minimised. The other signal is output at one of the feedback pins $\overline{FB1}$, $\overline{FB2}$, or $\overline{FB3}$. Each produces a signal which is LOW for a whole basic timing period. The fastest external counter is connected to $\overline{FB1}$, the next (if present) to $\overline{FB2}$, and so on. The timing of $\overline{FB1}$, $\overline{FB2}$, $\overline{FB3}$, and $\overline{SY}$ for use with a ÷(10/11) prescaler is shown in Fig.12.

If a single prescaler is used, the $\overline{FB1}$ and $\overline{SY}$ signals from the IC can be connected to the two $\overline{PE}$ inputs of the prescaler. A suitable interface is needed if the prescaler used is an ECL IC; an example is shown in Fig.13. If two prescalers are used, it is necessary to regenerate the $\overline{SY}$ signal by gating the $\overline{SY}$ signal with an output from the prescaler connected to the HEF4751 IN terminal. Similarly, if three prescalers are used, the $\overline{SY}$ input to the fastest prescaler is an AND function of the $\overline{SY}$ input to the second prescaler and one output of that prescaler.

A prescaler is currently being developed which includes the regenerating logic for $\overline{SY}$ that is necessary when more than one prescaler is used.

Phase comparator

The slow output from the HEF4751, FS, takes the form of evenly-spaced logic LOW pulses. This output is normally connected to the phase comparator section of the HEF4750 at pin STB. Accurate phase information is conveyed by each of the negative-going edges.

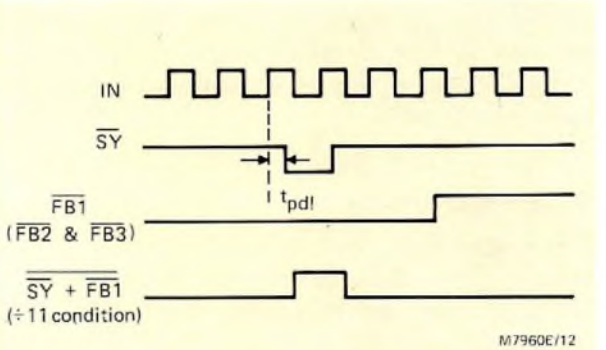


Fig.12 Timing of signals $\overline{FB1}$, $\overline{FB2}$, $\overline{FB3}$, and $\overline{SY}$

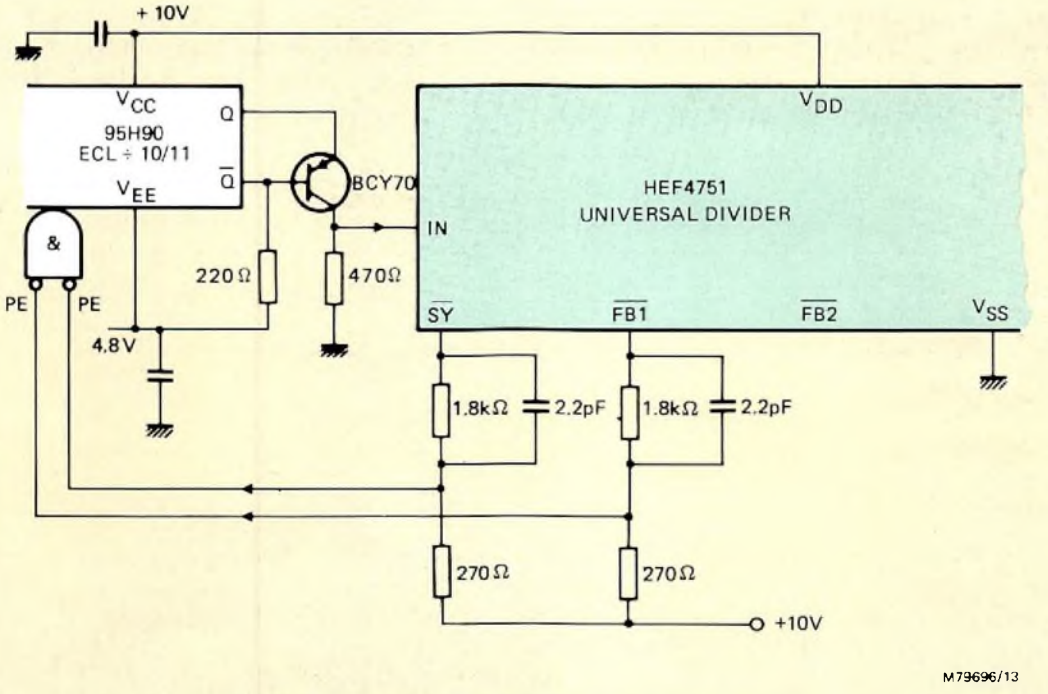


Fig.13 Connection of the HEF4751 to a fast ECL prescaler

The phase sample rate is thus equal to the pulse rate at FS. There are applications where this sample rate allows an adequate phase-lock loop bandwidth but is not fast enough to give a good frequency acquisition time. The fast output pin FF is provided to remedy this and should be connected to pin V of the HEF4750. The waveform at FF is related to that at FS by the ratios of the C_3 and C_4 counters but, because of the feedback from RS_0 and $RS_{½}$, there is some phase jitter. The maximum jitter time is ±1 period at the system input and will be removed by the strobe action of the main phase comparator PC_1 if:

$$\tau_i < \frac{TRA \times TCA}{4},$$

where τ_i is the period at the system input, and components TRA and TCA are the resistor and capacitor at pins TRA and TCA of HEF4750.

The R input to the phase comparator must be at frequency FF (mFS).

Programme memory

The programming process is timed and controlled by signals at input pins PC and PE of the IC, as is illustrated in Fig.14. When the Programme Enable input PE is HIGH, the positive-going edges of the programme clock (PC) signal step the internal programme counter through a sequence of eight states. The first seven states define fetch periods, each indicated by a LOW signal at one of the Data Address pins D0 to D6. The eighth state is not used.

The seven active-LOW Data Address signals are used, externally to the IC, to fetch the appropriate 8-bit bytes from the programme source. The programme source may consist of any combination of PROM, ROM, diode matrix, or BCD switches. Frequency selection, channel selection, transmit/receive, and offset control signals control the programme source.

The data from the programme source is applied to A0 to A3 and B0 to B3. The programme counter is advanced on the positive-going edge of PC. While PC is HIGH the external memory has a chance to settle, and the data is latched internally when PC goes LOW. The scanning action of the programme counter is controlled by the Programme Enable (PE) input. If PE is HIGH, the scanner will run continuously; when the PE goes LOW, the scanner will jump to the D6 state and stop. This facility can be used to synchronise the scanner to a microprocessor, or to enable single-shot programming. Signal PC can be any frequency up to 1 MHz and can be provided by the programme source, but it is more usual for the R output of the HEF4750 to be used for simplicity.

Cascading HEF4751 ICs

For applications such as SSB radio where the frequency must be selected in small steps, extra counters and rate selectors may be used. To simplify programming and interconnection, a "slave" mode is incorporated in the HEF4751 to allow it to perform the function of two extra stages.

In the slave mode the following changes occur compared to normal operation.

- C_{0b} and C_1 are disabled so that IN connects directly to C_2.
- $\overline{FB3}$ is converted to a borrow output signal, which is valid after the fetch 5 period. It represents the borrow signal from the programme subtractor after n_0 and n_1 have been programmed.

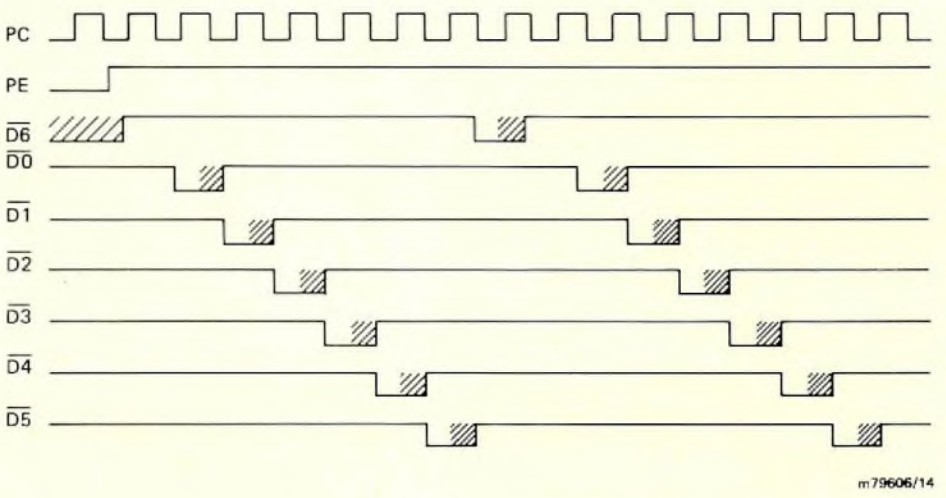


Fig.14 Programme, clock, and Data Address timing

TABLE 4

HEF4751 programme for slave mode

	n_6	n_5	n_4	n_3	n_2	n_1	n_0
Data A	X	0	0	0	11	X	X
Data B	X	0	0	0	10	X	X

X is normal programme data

The HEF4751 is put into the slave mode by the programme shown in Table 4. The necessary interconnections are shown in Table 5.

The FS output of the slave IC is always to the STB of the phase comparator. There is then a choice of three signals to connect to the V_{input} of the HEF4750, namely FF and FS of the master IC, and FF of the slave.

TABLE 5

Connections for cascaded HEF4751 divider IC

Master IC		Slave IC
FS	to	IN
SI	to	$\overline{FB3}$
$\overline{RI}$	to	$\overline{FB1}$

Unused inputs

All inputs to LOCMOS devices must be connected to an output or to one or other of the supply lines. Table 6 indicates the levels to which each input should be set to be inactive.

PRACTICAL SYNTHESISER

A detailed description of a practical synthesiser using the HEF4750 and HEF4751 will be published later.

REFERENCES

1. Underhill, M.J., "Wide range Frequency Synthesisers with Improved Dynamic Performance", IERE Conference on Land Mobile Radio, Lancaster (U.K.), September 1979.
2. Scott, R.I.H. and Underhill, M.J., "Wideband Frequency Synthesisers", IERE Conference on Land Mobile Radio, Lancaster (U.K.), September 1979.

Inactive input levels

HEF4750 input	Inactive state	HEF4751 input	Inactive state
D0 and D1	LOW	SI	LOW
A0 to A9	LOW	$\overline{RI}$	HIGH
MOD	HIGH	$\overline{A0}$ to $\overline{A3}$	HIGH
TRA	HIGH (PC_1 disabled)	$\overline{B0}$ to $\overline{B3}$	HIGH

Logic LOW = V_{SS} = 0 V Logic HIGH = V_{DD} = +10 V

Integrated Schottky logic gate array

S. Y. LAU

While the concept of logic gate arrays is not new, earlier designs used I^2L and MOS technology which gave a high gate density and low power consumption, but which could only operate at moderate or low speeds. Now, the speed of low power Schottky TTL and the inherently high packing density of I^2L have been combined in a new technology called Integrated Schottky Logic (ISL) used in the 8A1200 gate array.

Intended for semi-customised applications, the array comprises 1144 ISL gates, 52 Schottky buffers for high fan-out and 36 I/O cells. Each I/O cell can be programmed as an input, output or bidirectional transceiver. Eleven I/O cell configurations are available.

To design with the ISL array, logic equivalents of the ISL gates must be developed. For example, a two input NOR gate is implemented by three ISL gates. However, of most significance is the one-to-one correspondence between a NAND logic diagram and an ISL schematic.

Various circuits such as shift registers, flip-flops and counters, as well as logic gates, can be constructed on the same array. As a replacement for MSI and SSI TTL, the 8A1200 can replace up to 50 logic packages in a typical system.

Also known as uncommitted logic or masterslice, the 8A1200 gate array is a simpler, faster, less expensive means of producing a custom LSI logic circuit compared with conventional custom techniques.

INTRODUCTION TO ISL TECHNOLOGY

Each gate has two transistors – a normal downward npn (Q_1) which is clamped by a parasitic vertical pnp (Q_2), see Fig.1. The parasitic pnp is enhanced without enlarging the npn device. This is done in two ways:

- a shorter buried layer than usual is applied for the npn device, giving the vertical pnp more area;
- a shallow p-ring diffusion which overlaps the isolation diffusion, is added around the base of the npn to create a lateral pnp (Q_3) that actually parallels the vertical one.

Thus, the pnp transistor formed from Q_2 and Q_3 is an integral part of the ISL gate structure, producing a minimal-size gate geometry.

Although the normal downward configuration of Q_1 places a parasitic pnp transistor just where it is needed, it creates a problem.

ISL like I^2L requires a current source. This is a resistor fabricated as a pnp transistor and connected between V_{BB} and the base of Q_1. With Q_1 in normal downward configuration (as opposed to the inverted npn of I^2L), the current source cannot be merged with the npn device. Therefore, the 'resistor' must occupy its own island on the chip. This is why ISL occupies an area slightly larger than I^2L.

An ISL gate has one input and multiple outputs. Gate outputs are formed by Schottky metallisation made to the collector diffusion of Q_1. Each Schottky diode forms an independent output. The gate input is a single connection made to the base of Q_1.

8A1200 ARRAY ORGANISATION

The array consists of LSI gates, Schottky buffers, I/O cells and local and main supply rails (Fig.2).

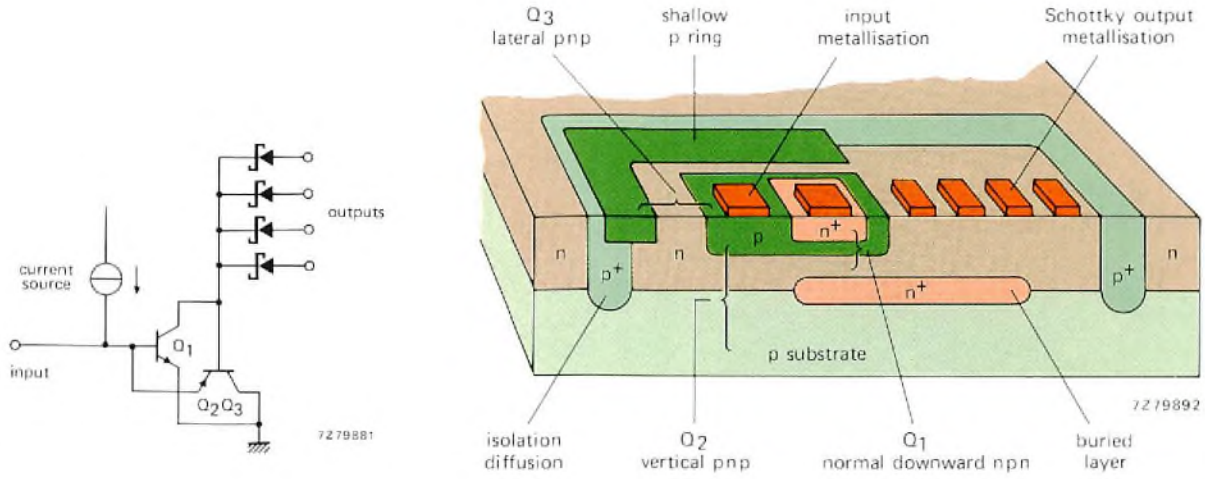


Fig.1 ISL gate structure and circuit diagram

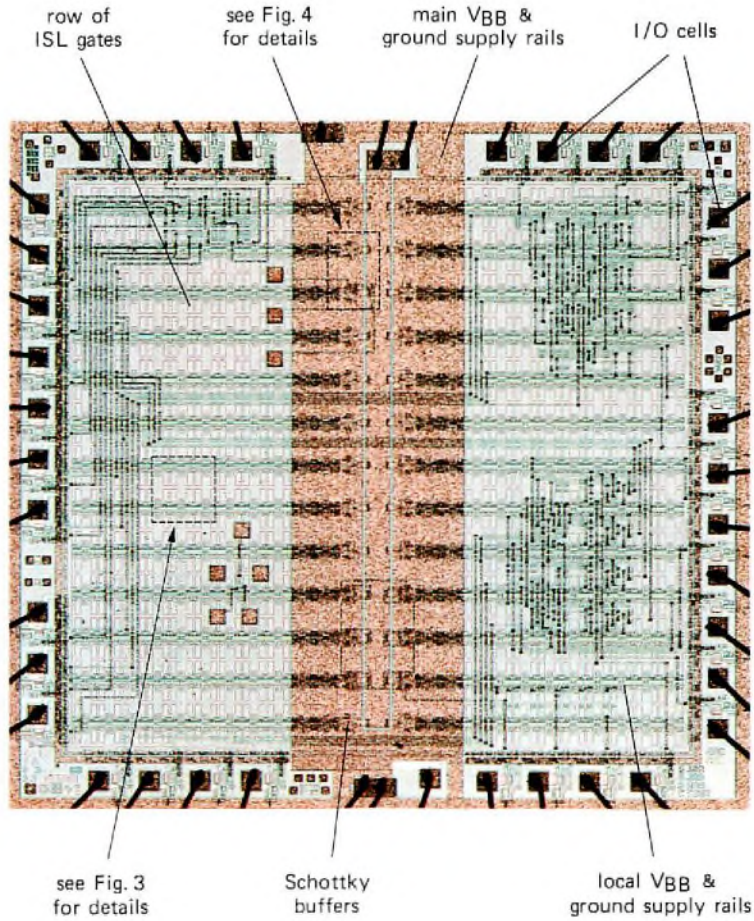


Fig.2 8A1200 ISL array layout

The gates are in 26 rows of 44 each. Figure 3, which is based on the mylar sheet used to specify gate interconnections, shows part of a row. The portion of each gate lettered L-R is a possible connection to a Schottky output. A,B,C,E,F,G,J,N,P,T,U and Y are direct connection points to a gate input. H,M,S and W are connection points to an input incorporating a series resistor to prevent current hogging.

The main supply rails divide the array in half. Between the two halves there are 52 Schottky buffers. Four Schottky buffers are shown in Fig.4. Here, points AA and CC are the direct connection points to a buffer input. Points BB and JJ are connection points to a buffer input which include a series decoupling resistor.

Around the periphery of the array, there are 36 I/O cells; 10 on each side and 8 at the top and bottom.

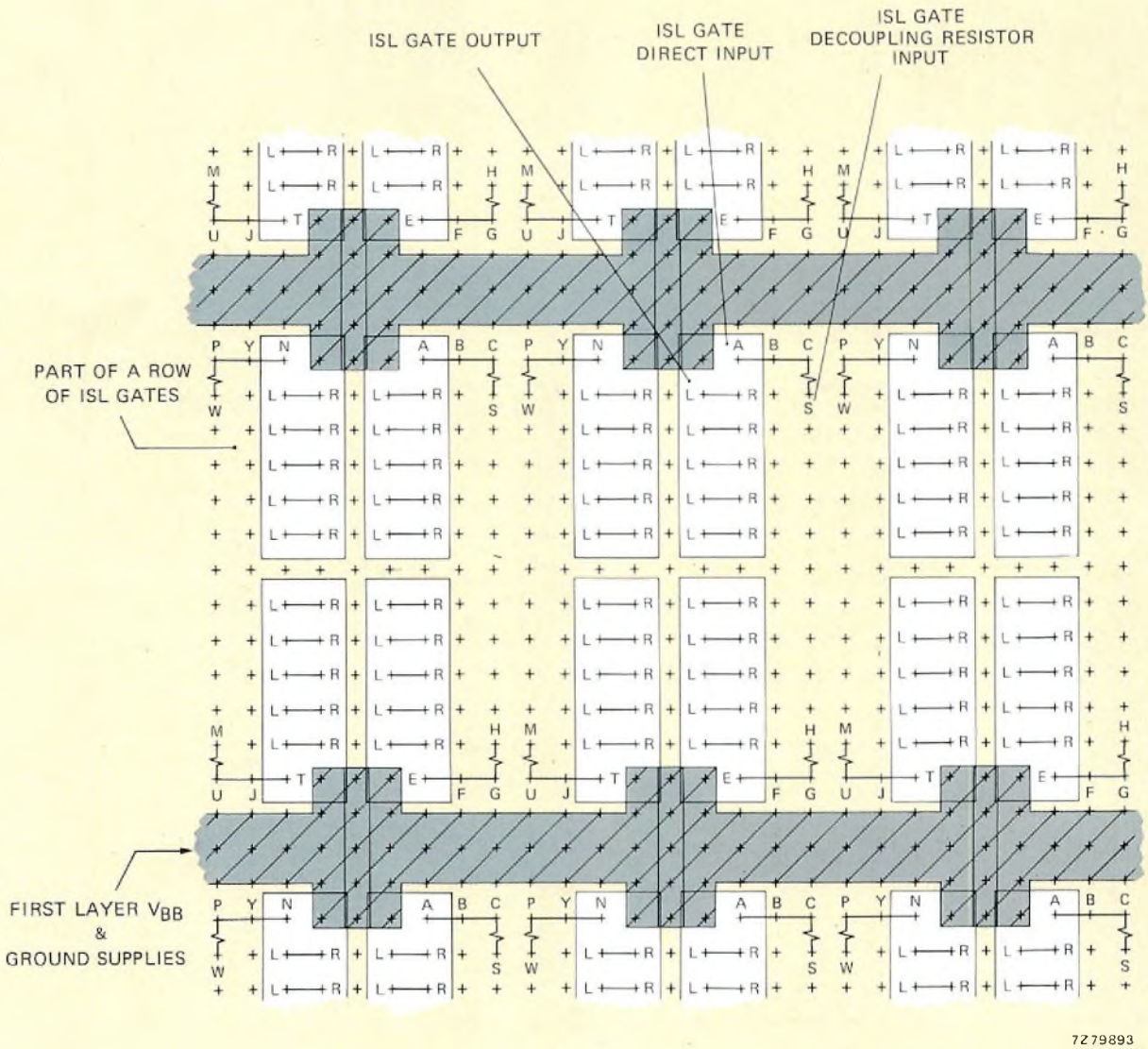


Fig.3 Layout of ISL gates in the 8A1200

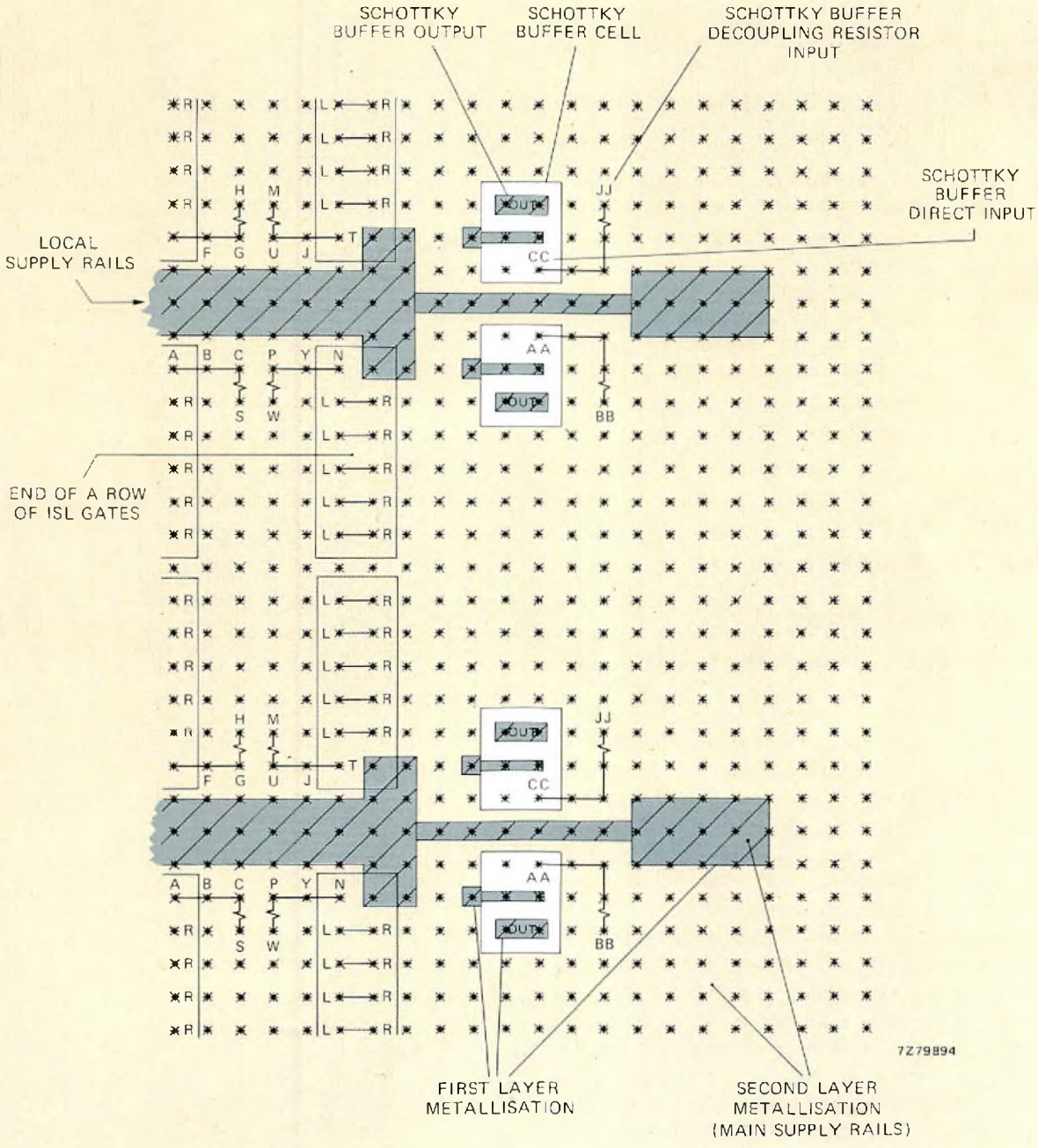


Fig.4 Layout of Schottky buffers in the 8A1200

ISL CHARACTERISTICS

Gates

Each gate occupies approximately 0.008 mm^2. The speed-power product per gate is typically 0.9 pJ, and the average gate propagation time is 3.5 ns (typical). Power consumption is 250 μW with a bias current of 150 μA.

Figure 5 shows the circuit diagram of an ISL gate, and Fig.6 the simplified symbol used in subsequent diagrams. The ISL gate functions as a logic inverter. It has one input and four outputs. These four outputs (actually five are provided for improved routing of which only four may be used) can each drive one load. Thus, each gate has essentially a fan-out of four.

Only one of the two possible connections to a gate input is used, depending on the sourcing device. For example, if the sourcing device is another ISL gate, the direct input is used. If the sourcing device is an I/O cell or a Schottky buffer (which normally has multiple loads) then the resistor input is used.

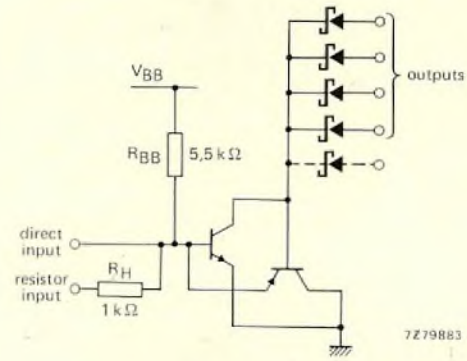


Fig.5 Circuit diagram of an ISL gate

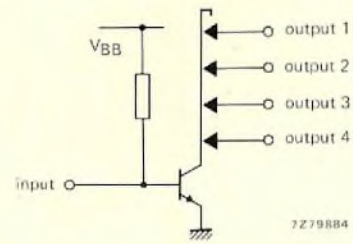


Fig.6 Symbol for an ISL gate

CURRENT HOGGING

Current-hogging conditions

When implementing shift registers, synchronous counters, decoders and similar circuits in ISL, some signals must be distributed to a large number of gates. This is most conveniently done by connecting together the inputs of those gates that require such a signal and then driving the common line from one gate. This approach reduces the number of gates that are necessary to achieve the required fan-out. However, it can also cause current-hogging. The current-hogging condition and its prevention are illustrated in the following example.

Suppose two gates A and B have their inputs connected to the output of a Schottky buffer, and suppose that the gates are in different locations on the array (Fig.7). When the drive transistor is off, current is fed into the common node through the two bias resistors R_{BB} of gates A and B. Ideally, the current divides equally between the gates and both transistors are on. However, gates A and B are not at the same ground potential because of voltage drops in the ground rail (the gates are in different parts of the array). This difference in potential is represented by the voltage source V_G. Only a few tens of millivolts difference in ground potential can cause one gate to hog the current from both bias sources, causing the transistor of the other gate to turn off. To prevent this, decoupling resistors R_H are connected in series with each gate input, as shown in Fig.8. This decouples the gates and does not significantly alter signal distribution.

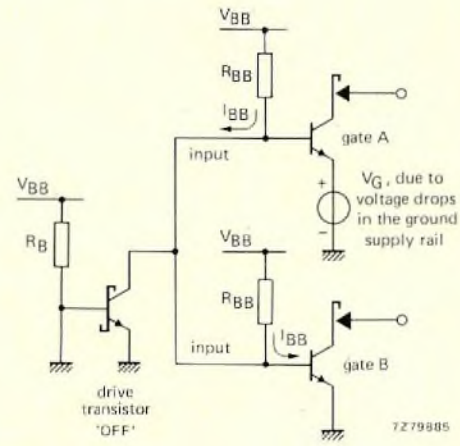


Fig.7 Condition for current-hogging to occur

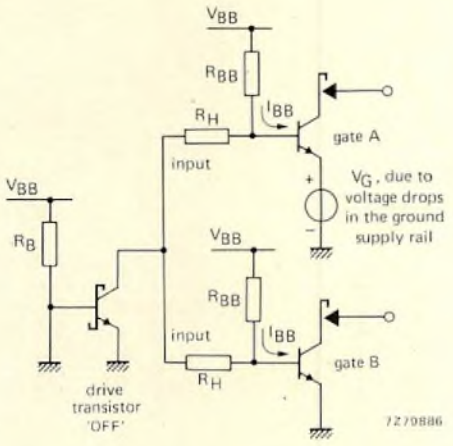


Fig.8 Use of decoupling resistors to prevent current-hogging

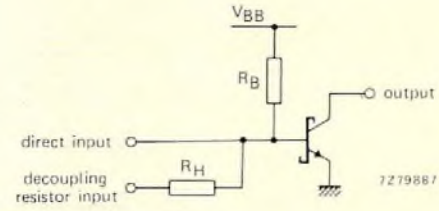


Fig.9 The Schottky buffer

Schottky buffer characteristics

Each collector output of an ISL gate has a fan-out of one. To provide a higher fan-out, Schottky buffers are used.

The Schottky buffer (Fig.9) has one open collector output which can drive up to 10 ISL gates. The direct input of the Schottky buffer can be driven by an ISL gate output. Schottky buffers themselves may have their inputs connected together to further increase the fan-out. In this case alone, the resistor input is used.

One Schottky buffer or input gate (an I/O cell programmed as an input gate) may drive up to 10 Schottky buffers with interconnected inputs. A Schottky buffer input and an ISL gate input may not be connected together to form a mixed fan-out configuration. Nor may two or more Schottky buffer inputs connected together be driven by one ISL output. However, a single ISL gate may drive up to four Schottky buffers (one buffer per collector).

I/O cell characteristics

All signal interfaces with the package pins are made through I/O cells. Each cell may be programmed as an input, output or bidirectional transceiver. There are four possible connection points to an I/O cell. Only the type of cell required, and the connection to or from the array, or both, need be specified. The cell options are summarised in Table 1.

All I/O cells are TTL compatible. These are basically no restrictions on the mixture or the number and type of I/O cells.

TABLE 1
I/O cell options

Mnemonic*	Function
AP	Standard low power Schottky output buffer with totem pole active pull-up.
OC	Standard low power Schottky output buffer with open collector output.
EOC	Enabled open collector output buffer. This is a standard low power Schottky buffer with open collector output enabled from the three-state enable bus.
TS	Standard three-state low power Schottky output.
EOCD	Input cell with output driver for driving the three-state enable of three-state output cells.
IOCD	As EOCD, except input is designed to interface with ISL gates. This cell is used internally and does not interface to an external pin.
INB	Low power Schottky input buffer with low current pnp input transistor.
TTS	Three-state transceiver. This is a back-to-back configuration of an input buffer and a three-state output in one I/O cell (INB + TS).
TOC	Open collector transceiver. This is a back-to-back configuration of an input buffer and an open collector output buffer (INB + OC).
TEOC	Enabled open collector transceiver. This is a back-to-back configuration of an input buffer and an enabled open collector output buffer (INB + EOC).
IOD	Input with three-state driver. This is a back-to-back configuration of an input buffer and an internal three-state driver (INB + IOCD).

* The mnemonics are used for programming the array.

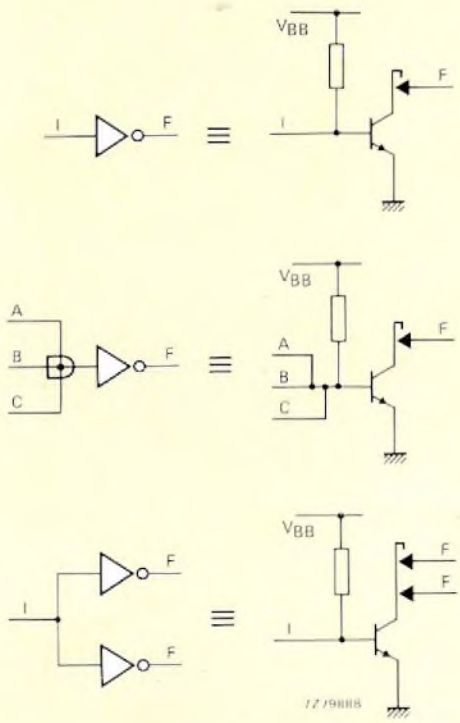


Fig.10 Representation of ISL circuits in conventional logic

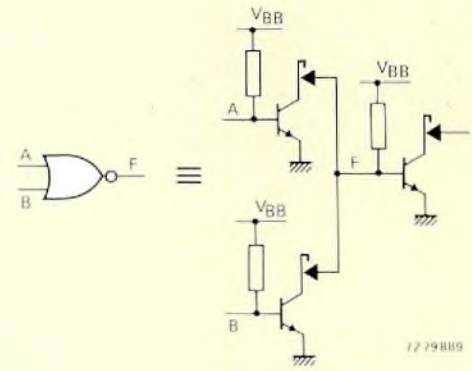


Fig.11 Representation of a NOR gate in ISL

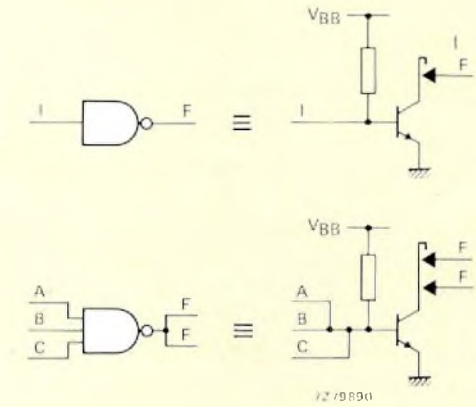


Fig.12 Representation of a NAND gate in ISL

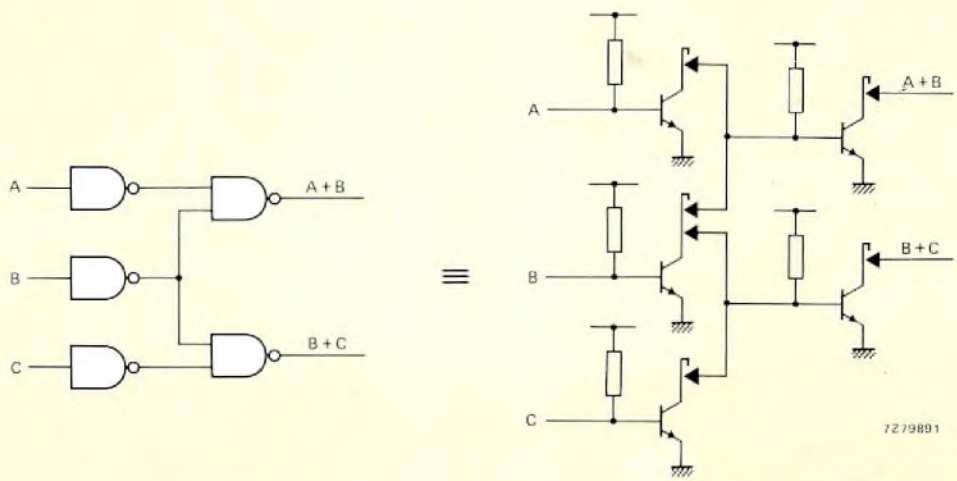


Fig.13 Representation of a simple logic circuit in NAND and ISL notation

DESIGNING WITH THE 8A1200

Logic to ISL transformation

The ISL gate behaves like a multiple-output single-input inverter. An ISL circuit can be represented directly using wired-AND gates and inverters, see Fig.10 for examples.

For convenience in system design, it would be advantageous to represent ISL circuits in NOR or NAND logic.

NOR representation

The logic and ISL circuit representation of a 2-input NOR gate are shown in Fig.11. The advantage of this approach is that, when trouble-shooting, signals can be checked directly at the transistor bases. However, there is one major disadvantage – the NOR gate is physically spread over three ISL gates.

NAND representation

Here, there is a one-to-one correspondence between a NAND logic diagram and an ISL schematic. Figures 12 and 13 illustrate this point. This physical equivalence means that signal names remain the same; inputs of the NAND logic diagram are inputs of the ISL gates. Similarly, outputs in one representation are outputs in the other.

An additional benefit is that NAND logic (the sum-of-products) is generally acknowledged to be easier to use than NOR logic (the product-of-sums).

Design aids

Computer simulation and computerised testing are used throughout the design of a customised ISL array (Fig.14). This gives a short development time and ensures a high first-time success rate in the first prototypes.

A library of logic functions is available on computer in TEGAS* format, for simulating the ISL circuit. It contains the following fully characterised functions:

- logic gates
- latches and flip-flops
- multiplexers
- decoders/encoders
- adders/comparators
- counters
- shift registers.

* TEGAS is a trademark of Comprehensive Computing Systems and Services Inc.

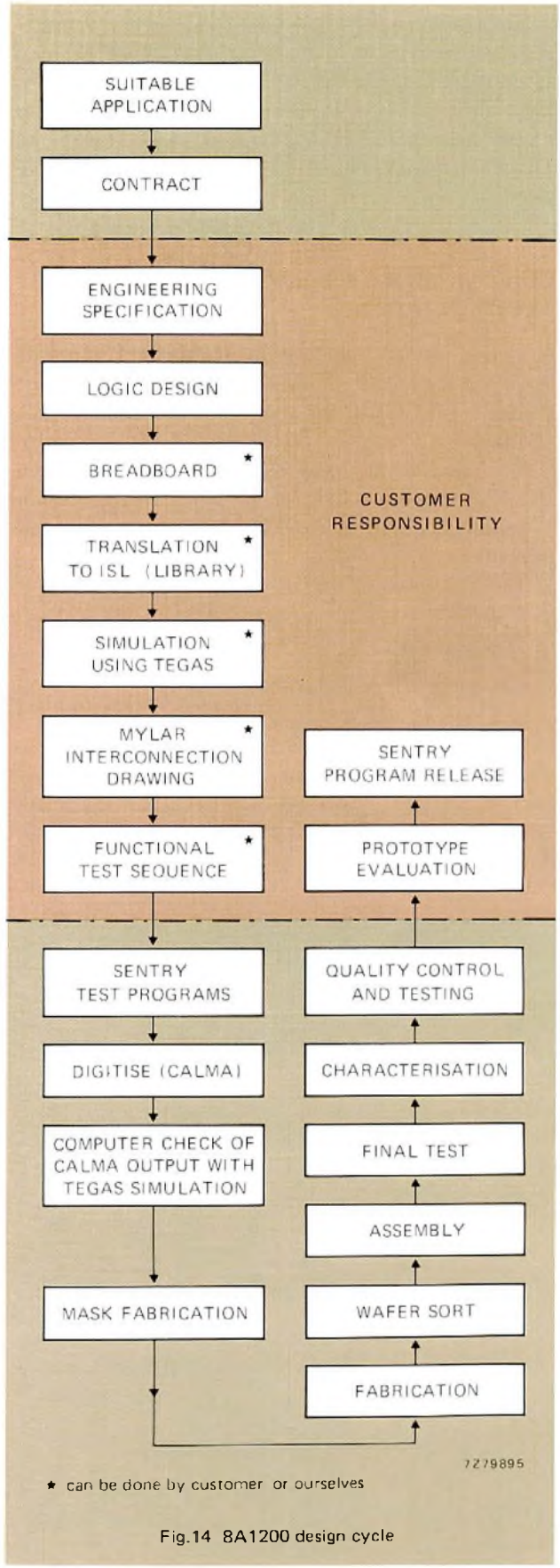


Fig.14 8A1200 design cycle

After simulation has verified the logic design, the buffer and gate connections that will be needed on the array are indicated on a mylar sheet. The information on the mylar sheet is then digitised on the CALMA graphic data system and the CALMA output is checked with the TEGAS simulation before fabrication of the array commences.

COMPARISON OF ISL WITH OTHER TECHNOLOGIES

Compared with I^2L and LS technologies, ISL has the best speed-power product (Table 2). Its packing density is of the same order as I^2L and about nine times greater than LS (Table 3).

The 8A1200 gate array makes it practical to design and produce custom LSI logic circuits at less cost and in a fraction of the time required using conventional LSI techniques.

The high speed of the 8A1200 makes it attractive for such applications as:

- EDP equipment
- data and telecommunication controllers
- magnetic disc controllers
- military equipment.

As a replacement for SSI and MSI TTL, the 8A1200 can typically replace up to 50 logic packages. In this application, the 8A1200 is more suitable than other types of programmable logic arrays (e.g. FPLA) because of its ability to implement a mixture of sub-systems, as well as logic gates, on one IC.

As a means to implement new system architecture, the 8A1200 offers a degree of flexibility unmatched by standard bit-slice microprocessors.

TABLE 2
Speed-power comparison of ISL with I^2L and LS. All values are typical

	ISL	I^2L	LS	units
Gate speed	3.5	15	9.5	ns
Power	250	250	2000	μW
Speed-power product	0.8	3.75	19.0	pJ

TABLE 3
Area in $mm^2 \times 10^{-2}$ occupied by various logic functions implemented in ISL, I^2L and LS

Function	ISL	I^2L	LS
NAND	1.16	0.71	9.23
NOR	1.87	1.42	25.81
D Flip-flop	5.81	4.26	47.42
4 to 1 MUX	9.35	7.10	85.67

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Digital control of radio and audio equipment

Part 6 - Voltage-controlled tuning of AM radios

B. P. BAHNSEN

The trend in radios and tuners is toward all-band, fully-electronic operation in which both the tuning and station presetting/selection are voltage-controlled. There is also an increasing demand for digital tuning and remote control. The space available for the radio circuits however is becoming smaller, especially in car radios with cassette playing facilities and in home radios in the new mini format. For these reasons, it has become essential to use variable-capacitance diode tuning not only for f.m., but also for a.m. stations in the long, medium and short-wavebands. Diodes for the a.m. frequencies must meet the following performance requirements:

- The normally used part of the tuning voltage/capacitance characteristic of the diode must be exponential to minimise non-linear distortion of signals applied to the tuned circuit. Furthermore, some form of signal limiting must be used to prevent high-level aerial signals shifting the tuned frequency and thereby causing the reception of spurious signals and increased distortion.
- For car radios, the required tuning voltage must always be less than 10 V. Since the permissible level of the aerial signal decreases with a low tuning voltage the previous problem is aggravated.
- The maximum capacitance and max/min capacitance ratio must tune the required frequency band.
- The capacitance/tuning voltage characteristics of the diodes in the aerial and oscillator tuned circuits must be accurately matched to provide good tracking.
- The diode capacitance must have a low-value, easily compensated temperature coefficient.
- The diode must have a low leakage current which is largely independent of temperature and tuning voltage.
- The diode must have low series resistance to prevent damping of the tuned circuits.
- Since the diode must be inexpensive, it must be capable of being mass-produced.

Even with such a high-performance variable-capacitance diode, the following precautions must be taken when designing voltage-tuned radios:

- The tuning voltage must be stabilised against temperature and supply voltage variations. This is especially critical in car radio applications. Typical stability requirements are ±0.1% for ±1 kHz tuning stability on medium wave.
- External circuits must cause minimum parasitic capacitance in parallel with the diode.
- The local-oscillator signal must have a constant low level.
- The tuning voltage must be adequately decoupled at signal frequencies.
- The resistor in series with the tuning voltage must be correctly chosen with regard to acceptable voltage drop and desired Q.

The newly developed controlled-growth profiled epitaxial process has allowed the manufacture of the a.m. variable-capacitance diode pair BB212 to meet the requirements of voltage tuned a.m. radios. These two closely matched diodes in one TO-92 variant require a tuning voltage of between 0.5 V and 8 V. Each has a maximum capacitance of 500 pF at 0.5 V and a max/min capacitance

ratio of at least 23. Since the tuning voltage/capacitance characteristic of the diodes is virtually exponential, they cause very little non-linear distortion.

This article shows how awareness of a few specific requirements and observation of a number of simple design rules leads to the construction of high-performance home and car radios in which diode pairs type BB212 control the selectivity.

NON-LINEAR DISTORTION

Since the capacitance of a variable-capacitance diode is a function of the applied voltage, the following signal handling problems arise when the component is used in a radio tuned circuit:

- Since the relationship between applied voltage and diode capacitance is non-linear, spurious non-linearity effects can cause modulation distortion of the applied signal. This distortion increases with increase of signal level and capacitance range and decreases with increasing tuning voltage. It cannot be eliminated by adding selectivity later in the circuit.
- If the signal level is not small relative to the tuning voltage, detuning can occur. This detuning increases non-linear distortion. The maximum distortion occurs when the tuned circuit is detuned to the 3 dB points of its original bandpass characteristic. Detuning also increases the effects of cross-modulation.

The foregoing non-linearity effects can be minimised by using a diode with the correct voltage/capacitance characteristic and by ensuring that the signal amplitude does not exceed a pre-determined level.

Voltage/capacitance characteristic

Figure 1 shows a number of possible/capacitance characteristics for variable capacitance diodes plotted on a log/linear scale. It can be calculated that the non-linearity factor (Ψ) of signals applied to diodes with these characteristic is as given in Table 1. The figures in Table 1 were calculated for a max/min capacitance ratio of 25 and a maximum tuning voltage of 8 V.

Table 1 shows that a characteristic as shown in Fig.1(c) is most appropriate since, in this case, the non-linearity factor is zero. This however is only valid for a test component which is not connected in a practical tuned circuit.

When the variable-capacitance diode is connected into a practical tuned circuit, there is inevitably some parallel parasitic capacitance (C_p) which modifies the diode capacitance (C_D) and thereby changes the shape of the

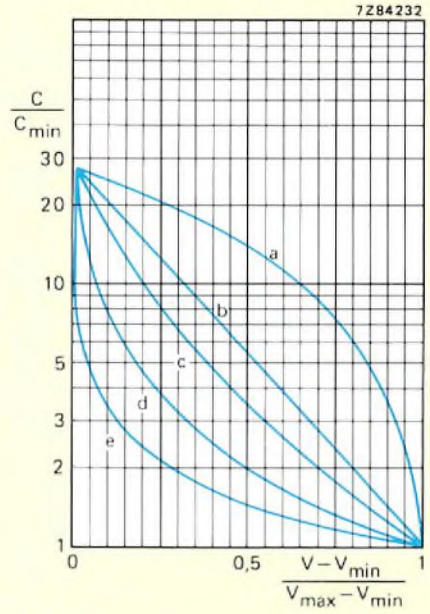


Fig.1 Voltage/capacitance characteristics for variable capacitance diode plotted on a log/linear scale. Curve (a) follows a linear law, curve (b) is exponential, curves (c) to (e) follow a law according to the expression $c = A/V + B)^n$ where n = 3,1 and 0.5 respectively

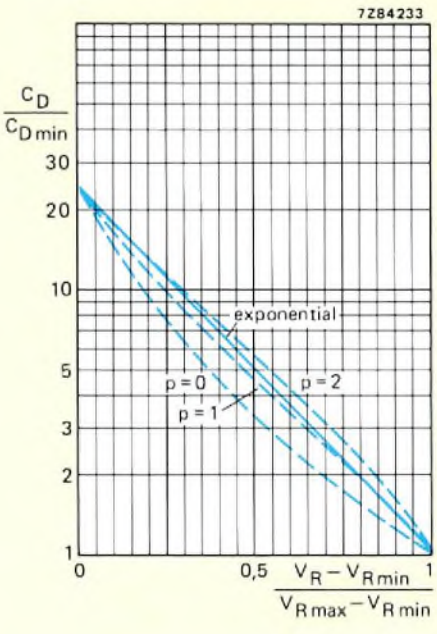


Fig.2 Voltage/capacitance characteristics for minimum non-linearity when parasitic capacitance (C_p) is connected in parallel with the diode; $p = C_p/C_{D\,min}$. The p = 0 curve corresponds with curve (c) in Fig.1, the exponential curve corresponds with line (b) in Fig.1

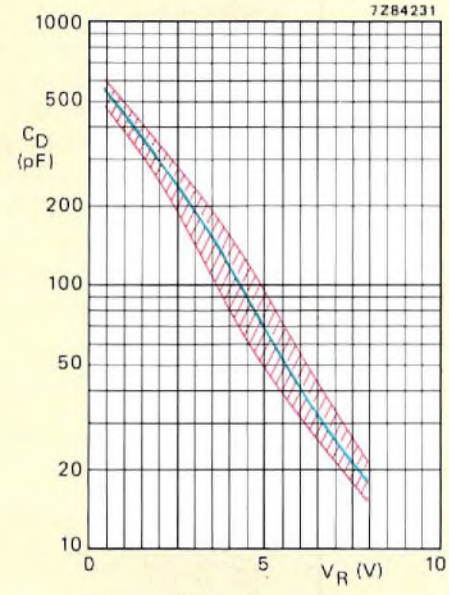


Fig.3 Typical voltage/capacitance characteristic for variable capacitance diode pair BB212. The shaded area indicates the characteristic spread for 98% of all components dispatched from the factory

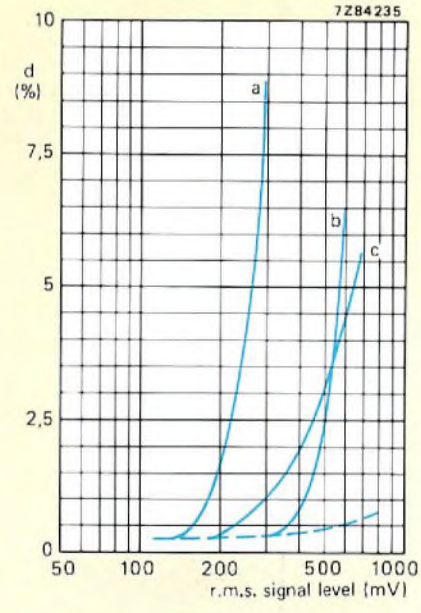


Fig.4 Distortion as a function of signal level with tuning voltage as a parameter. Curve (a) is for a tuning voltage of 0.5 V (f = 504 kHz). Curve (b) is for a tuning voltage of 8 V (f = 1627 kHz). Curve (c) is for a tuning voltage of 1 V (f = 562 kHz). The dashed curve applies for a conventional variable capacitor

TABLE 1
Non-linearity factors for the V/C characteristics in Fig.1

Fig.1 characteristic	non-linearity factor k_{max}
a	1.5
b	6.75×10^{-3}
c	317
d	0.75
e	0

voltage/capacitance characteristic. Figure 2 shows the ideal voltage/capacitance characteristics when various amounts of parasitic capacitance are taken into account. This illustration shows that, with a parasitic capacitance of between $C_{D\,min}$ and $2C_{D\,min}$, an approximately exponential voltage/capacitance characteristic causes least non-linear distortion. Since $C_{D\,min} < 22$ pF for the BB212, this assumes parasitic capacitance of between 20 pF and 40 pF which are realistic values for a practical circuit. The typical voltage/capacitance characteristic for the BB212 is given in Fig.3. Since this curve very closely approximates a straight line on the log/linear presentation, it is very close to the ideal exponential form which results in the lowest possible non-linearity factor.

Since the capacitance ratio required to tune the local-oscillator of a radio is different to that required to tune the aerial circuits, it is necessary to add some padding capacitance which increases the effective parasitic capacitance (C_p). The exponential voltage/capacitance characteristic is therefore not ideal for tuning the local-oscillator. In this case however, a low level oscillator signal will minimise both the non-linear distortion and the radiation.

Effect of signal amplitude on non-linearity

As previously stated, the non-linear distortion caused by the variable-capacitance diode increases with applied signal amplitude. To determine the extent of this distortion, a radio tuned circuit incorporating a BB212 was tuned to a signal modulated to 80% with a 400 Hz tone. After demodulation, the a.f. distortion was measured as a function of signal level with tuning voltages of 0.5 V, 1 V and 8 V. The results of these measurements are plotted in Fig.4. This diagram shows that the distortion can be restricted to 1.5% if the signal level is limited to 200 mV r.m.s. at the lowest tuned frequency. At the highest tuned frequency (highest tuning voltage, lowest capacitance), the signal level could rise to 450 mV r.m.s. without increased distortion.

The curves in Fig.4 are only valid if the circuit is correctly tuned. In practice, some unavoidable padding errors occur and cause slight mistuning at some frequencies, thereby increasing the distortion. Figure 5 shows the distortion variation caused by padding errors.

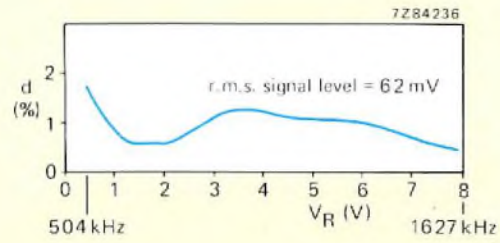


Fig.5 Non-linear distortion variation caused by padding errors in the aerial stage of a receiver. The signal voltage across the diode was maintained at 62 mV r.m.s. by varying the input signal. The circuit was first correctly aligned at three frequencies within the range 504 kHz – 1627 kHz

The application examples at the end of this article show how aerial signal limiting circuits can be used to limit the signal voltage across the aerial circuit tuning diode to 100 mV r.m.s. and thereby ensure a.f. distortion of less than 2% for aerial signals of up to 1 V r.m.s.

MAXIMUM CAPACITANCE AND CAPACITANCE RATIO

The resonant frequency of an LC tuned circuit is:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

Assuming a fixed-value inductor, the capacitance ratio required to tune the circuit across a frequency range f_1 to f_2 is:

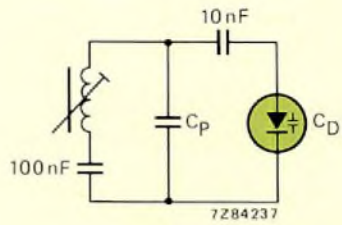
$$\frac{C_{D\,max}}{C_{D\,min}} = \left(\frac{f_2}{f_1}\right)^2$$

This relationship only holds true for an ideal circuit without parasitic capacitance. If parasitic capacitance with a fixed value C_p is taken into account, the expression becomes:

$$\frac{C_{D\,max} + C_p}{C_{D\,min} + C_p} = \left(\frac{f_2}{f_1}\right)^2$$

From this equation, expressions can be derived for the capacitance ratio C_{Dmax}/C_{Dmin} and for C_p for any frequency range. In the local-oscillator circuit, the effects of padding capacitors also have to be taken into account and complicate the calculations. The curves in Fig.6 have been plotted for $f_2/f_1 \approx 3$ which represents the typical frequency coverage of the medium-waveband (510 kHz to 1620 kHz). The diagram shows that, assuming a typical parasitic capacitance of 25 pF and C_{Dmax} = 500 pF, the required capacitance ratio is 20. The BB212 exceeds these requirements with a maximum capacitance of at least 500 pF and a capacitance ratio of at least 23.

The assumed frequency ratio of 3:1 is also more than sufficient for long-wave tuning because here, the required frequency coverage is less than that required for the medium-wave. Since the short-wave is normally divided into a number of bands to facilitate tuning of the closely spaced stations, each band can have a maximum/minimum frequency ratio of not more than 3:1 (e.g. 6 MHz to 18 MHz ≈ 49 metres to 16 metres).



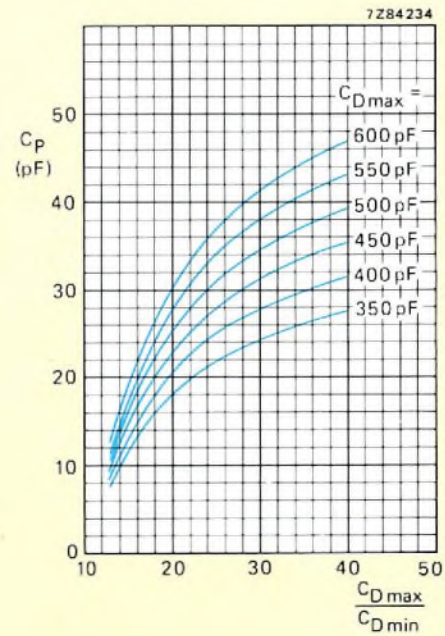


Fig.6 Capacitance ratio as a function of parasitic capacitance with $C_{D\,max}$ as a parameter. These curves are plotted for a 3:1 frequency ratio (510 kHz to 1620 kHz)

THE TUNING VOLTAGE AND TUNING STABILITY CONSIDERATIONS

For a given diode capacitance ratio, non-linear distortion of the applied signal will decrease with increasing tuning voltage. For example, it is fairly simple to achieve low non-linear distortion if the tuning voltage range can be as high as 20 V to 30 V. Although such a high tuning voltage range would be acceptable for some mains-powered radios, it could not be obtained from the battery in mobile applications such as car radios. It would therefore be necessary to derive it from a d.c. to d.c. converter which would increase cost, size and interference generation. These disadvantages are eliminated if the maximum tuning voltage is less than 10 V. As previously explained, if the diode has the ideal exponential voltage/capacitance characteristic and the optimum amount of parasitic capacitance is present, non-linear distortion is reduced to within acceptable limits even if the maximum tuning voltage does not exceed 8 V. The minimum tuning voltage is directly related to the maximum obtainable capacitance and must therefore be as low as possible in the interests of wide frequency coverage for the tuning system.

The BB212 is eminently suitable for both mobile (12 V) and home (mains-powered) applications since it has a nearly exponential voltage/capacitance characteristic, a maximum tuning voltage of 8 V and a capacitance of at least 500 pF with a tuning voltage of 0.5 V (see Fig.3).

To ensure tuning stability under all operating conditions, the tuning voltage must be compensated for supply voltage and temperature variations. For example, when using the BB212, the tuning drift on the medium waveband will be restricted to 1 kHz in a radio without a.f.c. if the tuning voltage drift does not exceed 0.1%. In radios with a.f.c., the tuning voltage drift can be 0.3% for the same tuning drift. Although this order of voltage stability can be easily achieved with temperature compensated voltage regulator diodes or integrated voltage stabilisers, it must be remembered that the overall tuning stability of the radio will also depend on the temperature coefficients of the variable capacitance diode, the tuning potentiometer and the coils and capacitors used in the tuned circuits. The exponential voltage/capacitance characteristic of the BB212 results in a very constant, low, and therefore easily compensated, temperature coefficient of capacitance. At temperatures within the range 25 °C to 60 °C, the typical temperature coefficients are 0.05%/°C with a tuning voltage of 8 V and 0.054%/°C with a tuning voltage of 0.5 V.

DECOUPLING THE TUNING VOLTAGE AND THE EFFECTS OF LEAKAGE CURRENT

The coil connected in parallel with the variable-capacitance diode in a tuned circuit must not short-circuit the tuning voltage source. A series capacitance C_S must therefore be included in the circuit as shown in Fig.7(a). In the aerial circuit, the value of series capacitance must be much larger than the maximum diode capacitance. In the oscillator stage, it should be of the same order or smaller than the maximum diode capacitance.

The tuning voltage is applied to the diode via series resistor R_V to prevent the tuned circuit being short-circuited by the tuning voltage source. The value of R_V in Fig.7(a) must be fairly high because it has a considerable damping effect on the tuned circuit. However, it must have a low enough value to prevent significant reduction of the tuning voltage due to the passage of the diode leakage current. If the maximum permissible voltage variation is known, the maximum value for R_V can be calculated from:

$$R_{V\,max} = \frac{\Delta V_R}{\Delta I_{R(T)}}$$

When the circuit in Fig.7(b) or (c) is used and $C_S \gg C_D$, the value of R_V can be lower than that required for fig.7(a) because the damping effect on the tuned circuit is negligible.

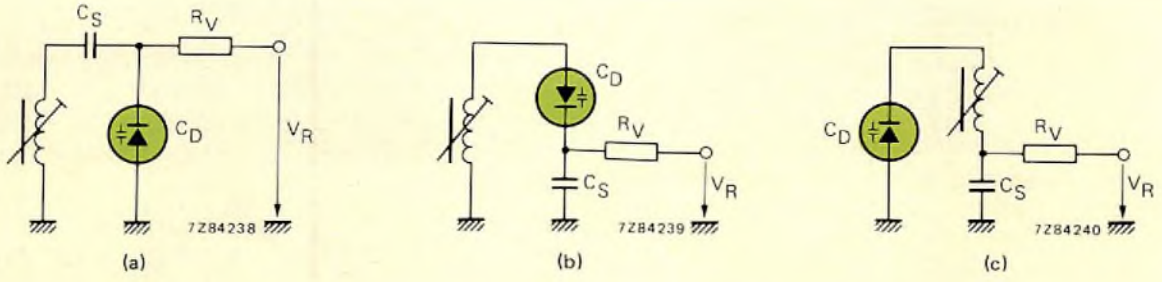


Fig.7 Various methods of connecting the tuning voltage to the variable capacitance diode and decoupling the tuning voltage supply line

The specified leakage current for the BB212 at $T_j = 60°C$ and $V_R = 10\,V$ is 0.3 nA typical, 200 nA maximum. The worst-case change of leakage current over the temperature range 25 °C to 60 °C is therefore 200 nA. The tuning error due to the effects of leakage current is more significant in the oscillator circuit than it is in the aerial circuit. This is because the oscillator frequency determines the i.f. and its bandpass characteristic is narrower.

EFFECT OF DIODE SERIES RESISTANCE ON CIRCUIT DAMPING

The simplified equivalent circuit of a variable-capacitance diode consists of a series-connected capacitance (C_D) and resistance (r_D). The series resistance comprises two parts; one part, which is not voltage dependent, consists of the metal-oxide junction, the substrate resistance and the dielectric loss resistance. The remaining part, the profile resistance, varies with applied voltage at frequencies above a few megahertz but remains constant at lower frequencies.

The quality factor of the variable-capacitance diode is:

$$Q_D = \frac{X_{CD}}{r_D} = \frac{1}{\omega_0 C_D r_D} \qquad (1)$$

In a tuned circuit where

$$C_p \ll C_D$$

$$C_s \gg C_D$$

and Q_0 is the quality factor ignoring the diode series resistance,

$$Q = \frac{1}{1/Q_0 + 1/Q_D} \qquad (2)$$

Inserting equation (1) into equation (2) in place of Q_D and solving for r_D gives:

$$r_D = \frac{Q_0 - Q}{QQ_0\omega_0 C_D} \qquad (3)$$

In a typical radio tuned circuit where the required bandwidth is 10 kHz at the lowest medium-wave frequency (530 kHz) the required quality factor is:

$$Q = \frac{f_0}{BW} = \frac{530}{10} = 53$$

If the quality factor ignoring the diode series resistance (Q_0) is 80, the permissible series resistance for the diode from equation (3) is:

$$r_D = \frac{80 - 53}{53 \times 80 \times 6.28 \times 530 \times 10^3 \times 500 \times 10^{-12}} = 3.8\,\Omega$$

For the short-wave ($f_0 = 6$ MHz, $C_D = 500$ pF), this value becomes 0.34 Ω. From the foregoing, it can be seen that, since the maximum series resistance of the BB212 is 2.5 Ω, it will not cause too much damping in long and medium-wave tuned circuits where the series capacitance is much greater than the diode capacitance. For the short-wave, the damping appears to be excessive. However, if the short-wave band does not extend below a frequency of about 6 MHz (49 metres), the series capacitance can be reduced, thereby considerably reducing the damping.

MATCHING THE CAPACITANCE OF THE DIODE PAIR BB212

In the ideal case the capacitance of the variable-capacitance diodes in an aerial and oscillator circuit of a radio should be the same at any tuning voltage. In practice, this is not the case because there is always some spread of capacitance during the manufacturing process. This tolerance cannot be corrected with additional circuit components because it varies with the tuning voltage applied to the diode. It is therefore normal to publish a tolerance field for capacitance variation as a function of tuning voltage. Either of the following methods can be used to keep the published tolerance field within acceptable limits:

- Post-production selection of diodes with capacitance values that fall within the published tolerance field.
- Development of a technology and manufacturing process that yields sufficient diodes with capacitance values that fall within the acceptable tolerance field. The few diodes that have capacitance values outside the tolerance field are then rejected during production.

The latter method is used for the BB212 diode pair. The two diodes of the pair remain adjacent to each other on the crystal throughout the manufacturing process so that differences (especially in the relationship between tuning voltage and capacitance) are minimised.

The spread between the capacitances of the two diodes is given by:

$$\frac{\Delta C}{C_2} = \frac{C_1 - C_2}{C_2}$$

Since the higher capacitance values can be kept within closer tolerances than the lower ones, the capacitance spread increases with increasing tuning voltage (decreasing capacitance) and can be expressed at any tuning voltage as:

$$s(V_R) = \left.\frac{C_1 - C_2}{C_2}\right|_{V_R} \qquad (4)$$

Since the tolerance (s) is dependent on tuning voltage, it cannot be compensated with additional components in

the tuned circuit and must therefore be allowed for when determining worst-case component values.

The tolerance field for any single BB212 diode is shown in Fig.8. However, the tolerance for any specific diode will always remain either positive or negative regardless of tuning voltage within the range 0.5 V to 8 V. The capacitance of one diode of the pair relative to the capacitance of the other, as a function of tuning voltage, can therefore always be plotted within a field with limits of twice those shown in Fig.8 but which is totally above or below the nominal capacitance line. This field is shown for diode pairs with positive or negative tolerances in Fig.9. Contained within the field are curves of the measured capacitance difference between the two diodes of six typical diode pairs BB212. It can be seen from these curves that, within the normally used tuning voltage range (0.5 V to 8 V), the curves never cross the nominal capacitance line. This means that one of the diodes of each pair has a higher capacitance than the other at all tuning voltages. If it is known which of the two diodes has the higher capacitance, that capacitance can be denoted C_I and equation (4) will then always yield a positive result. Only one half of the symmetrical tolerance field of Fig.9 is then applicable as shown in Fig.10.

The diode with the highest capacitance (measured at $V_R = 3$ V) in each diode pair BB212 is therefore identified with a coloured dot adjacent to its anode lead and the published tolerance field is as shown in Fig.10.

As shown in Fig.10, the maximum capacitance tolerance for the BB212 increases linearly from 2% at a tuning voltage of 0.5 V to 7% at a tuning voltage of 5.5 V and then remains constant up to the maximum tuning voltage of 8 V. The average value of the tolerance is shown by the dashed line drawn between s = 1% at 0.5 V and s = 3.5% at 8 V. The average tolerance can be expressed as:

$$s_{av}\,\% = \frac{s_{max} - s_{min}}{2}\left(\frac{V_R - V_{R\,min}}{V_{R\,max} - V_{R\,min}}\right) + \frac{s_{min}}{2}$$

Inserting values from Fig.10 gives:

$$s_{av}\,\% = 0.33\,(V_R - 0.5\,V) + 1 \qquad (5)$$

To verify the validity of equation (5), two radios were built; one with the tuned circuit component values calculated according to the worst-case capacitance values from Fig.8, and one allowing for the average capacitance tolerance calculated from equation (5). The difference between the resulting component values was never more than 3.5%. Tracking errors were greater at the higher frequencies when the tolerances from Fig.8 were used. The tracking errors were greatest at the lower frequencies when equation (5) was used.

Since the capacitance tolerance increases with increasing tuning voltage (decreasing capacitance), the lowest capacitance diode usuallu has the highest capacitance ratio C_{max}/C_{min}.

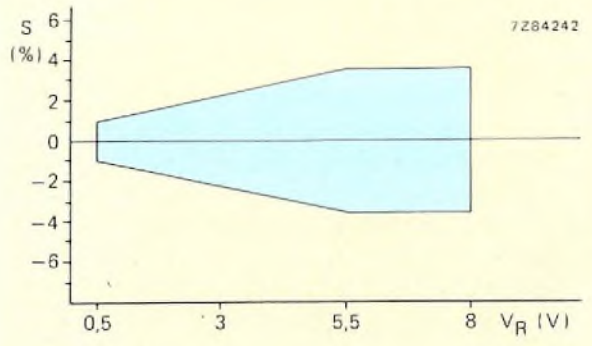


Fig.8 Capacitance tolerance field for a single diode of a BB212 pair

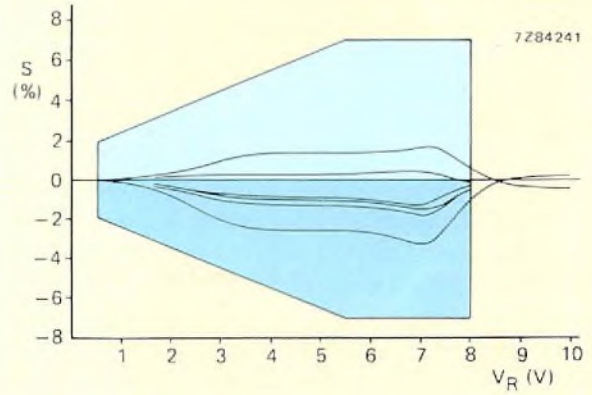


Fig.9 Tolerance field for the relative capacitance of the two diodes of a BB212 pair with plots for six typical devices

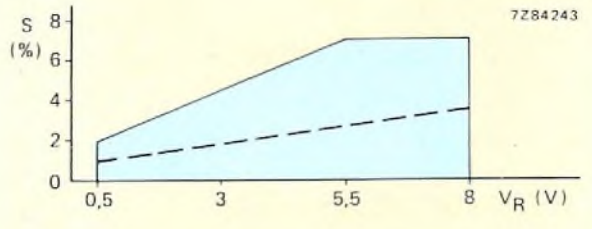


Fig.10 Tolerance field for the relative capacitance of the two diodes of a BB212 pair when the diode with the highest capacitance is identified

THE BB212 IN PRACTICAL RADIO CIRCUITS

Medium-wave car radio

Figure 11 is the circuit diagram of a typical medium-wave car radio using the BB212 variable-capacitance diode pair. The circuit is powered by a 9 V d.c. stabilised supply and incorporates the integrated a.m. receiver circuit TDA1072.

As explained earlier in this article, it is necessary to limit the amplitude of both the aerial and local-oscillator signals to minimise non-linear distortion when using variable-capacitance diode tuning. For a maximum a.f. distortion of 2%, the aerial signal must be limited to 100 mV r.m.s. The local-oscillator signal must not exceed 350 mV r.m.s.

The TDA1072 incorporates an amplitude-controlled local-oscillator which maintains the output at pin 12 constant at a typical level of 140 mV r.m.s. (200 mV r.m.s. max).

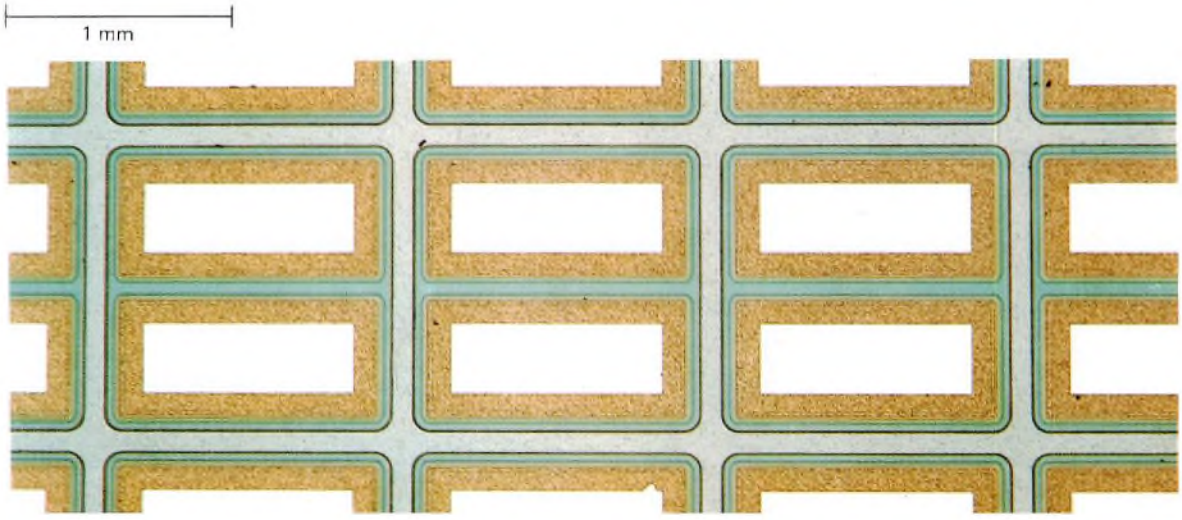
In the circuit of Fig.11, the aerial signal is applied to the gate of a BF410D FET to obtain amplification and impedance conversion with a high signal-to-noise ratio. The signal is then passed through a π-filter tuned by a variable-capacitance diode at its output. This filter suppresses high-frequency signals to prevent spurious product frequencies. The resistor at the input and output of the filter provide damping to reduce unwanted resonances. They also help to achieve a constant signal transfer ratio between the aerial and the r.f. input to the TDA1072. Limitation of the amplitude of the signal at the anode of the aerial circuit tuning diode is achieved by a feed-forward control loop between this point and the aerial input. The signal at the anode of the aerial circuit tuning diode is fed, via a low noise FET impedance converter, to a BF494 transistor connected as a diode rectifier. The rectified signal is smoothed by a low-pass filter and applied to the base of a BF450 transistor connected in the source circuit of a BSV78 FET. The amplification provided by the BSV78 is thus controlled in proportion to signal strength. Since the signal at the drain of the BSV78 is antiphase to the aerial signal, the sum of the signals at the gate of the BF410D input FET is inversely proportional to the aerial signal amplitude. The aerial signal amplitude at which the gain control commences is set by the potentiometer in the base circuit of the BF494 rectifier. This potentiometer should be adjusted so that the gain control circuit is inoperative with an aerial signal of 100 μV r.m.s., and is fully operational when the amplitude of the signal across the aerial circuit tuning diode reaches 100 mV r.m.s.

Performance of the circuit

With a 1 V r.m.s. aerial signal, the total a.f. distortion is less than 1.5%. The 3 dB bandwidth of the h.f. stages is 12 kHz at a tuned frequency of 600 kHz, and is 16 kHz at a tuned frequency of 1600 kHz. The required aerial signal levels for S/N ratios of 6 dB and 26 dB are given in Table2.

TABLE 2
Noise performance of a.m. car radio

tuned frequency	required r.m.s. aerial signal for (S + N)/N =	
	6 dB	26 dB
600 kHz	7.8 μV	78 μV
1 MHz	5.5 μV	59 μV
1.5 MHz	5.5 μV	55 μV



Photomicrograph of BB212 diode pairs on the silicon slice

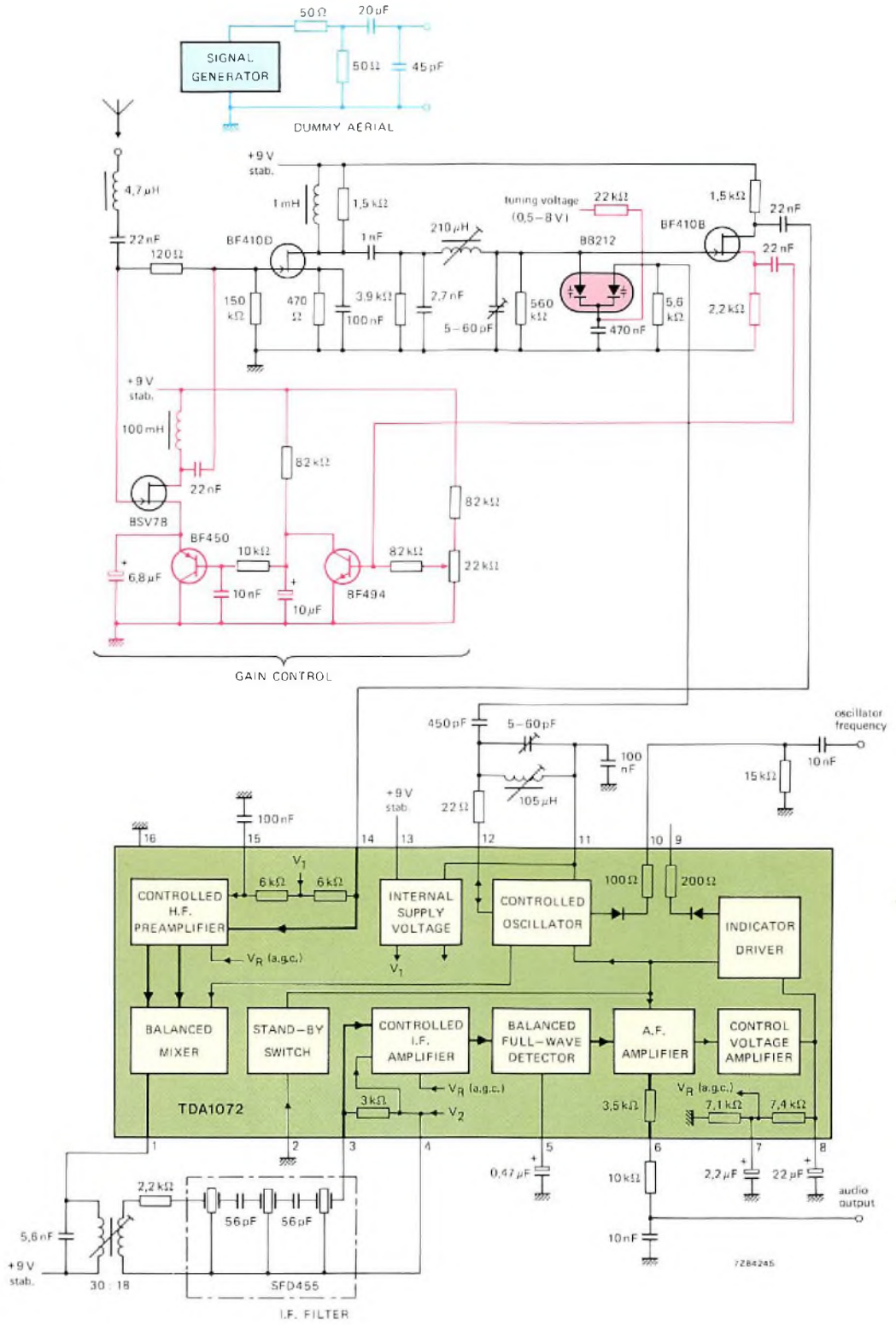


Fig.11 Medium-wave car radio using tuning diode-pair BB212

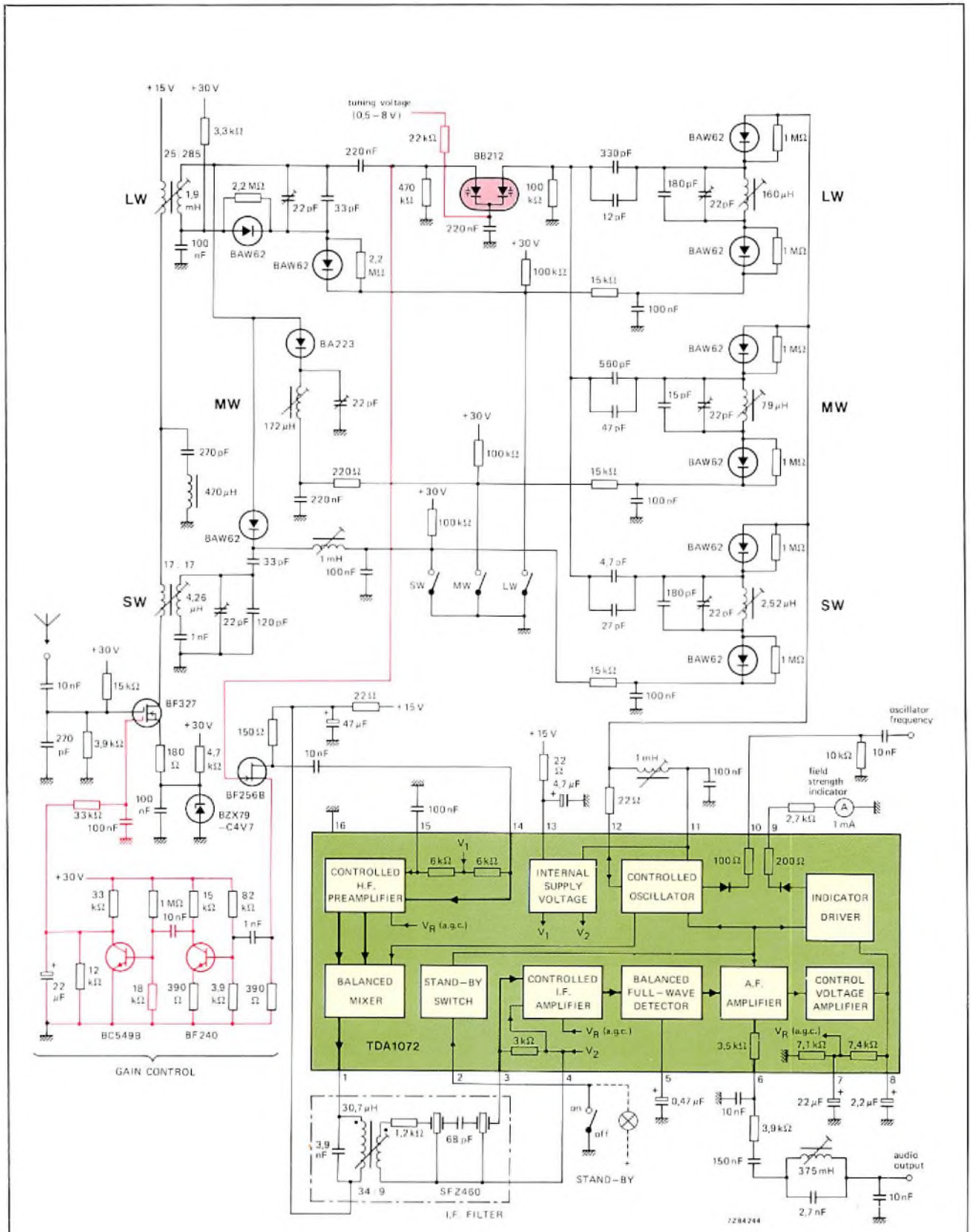


Fig.12 All-band a.m. mains-powered radio using tuning diode-pair BB212

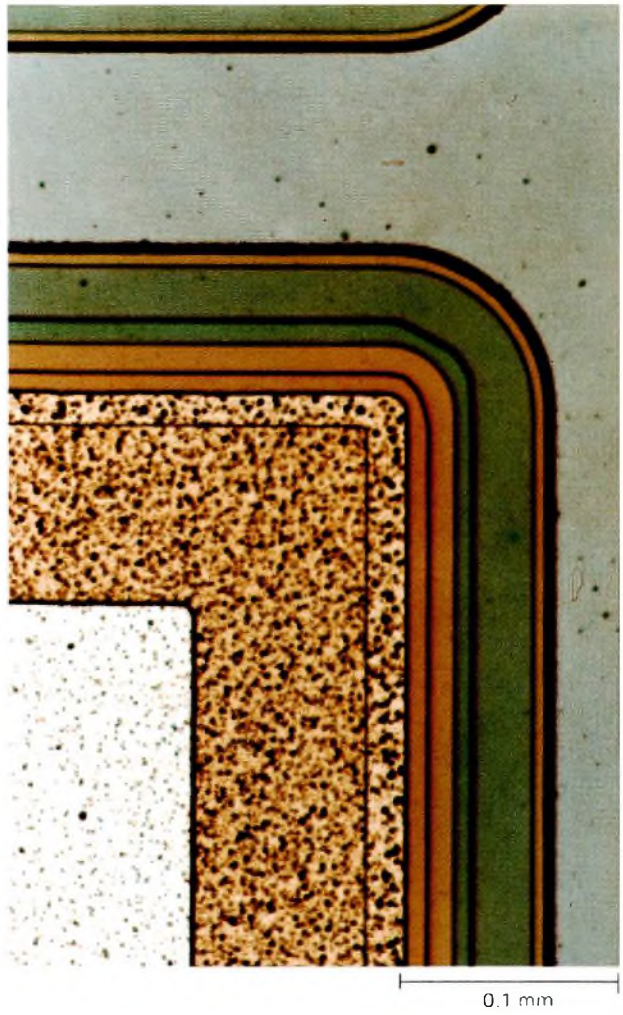
All-band a.m. mains-powered radio

The diagram of a typical mains-powered all-band a.m. radio circuit using the BB212 variable-capacitance diode pair is given in Fig.12. Like the previously described car radio, it includes the TDA1072 integrated a.m. receiver circuit which incorporates an amplitude-controlled local-oscillator. Limitation of the signal amplitude at the anode of the aerial circuit tuning diode is achieved by a FET aerial input stage with controlled amplification. The signal at the anode of the aerial circuit tuning diode is fed, via a low noise FET impedance converter and BF240 transistor connected as a diode rectifier. The rectified signal is smoothed by a low-pass filter and applied to one gate of the dual-gate input FET BF327. If the aerial signal level exceeds about 10 mV r.m.s., the gain control voltage at the gate of the BF327 starts to decrease, thereby decreasing the source-drain current and reducing the gain. If the level of the aerial signal reaches 1 V r.m.s., the signal level at the anode of the aerial circuit tuning diode is limited to 100 mV r.m.s.

A low impedance (3.9 kΩ in parallel with 270 pF) between the aerial input gate of the BF327 and the common rail reduces the noise current input and also, in conjuction with the aerial impedance, provides aerial voltage division to reduce the level of aerial signal applied to the gate. Linear signal transfer for the input stage is achieved by applying negative feedback by not de-coupling the 180 Ω source resistor. The voltage regulator diode in the source circuit provides an accurate and stable bias voltage for the input stage.

The circuit uses diode waveband switching. Because the switching diode in the medium-wave aerial circuit must pass the h.f. signal, the low-resistance BA223 is used at this position. The inexpensive BAW62 is used at all other positions.

Since the 5 kHz station spacing on short-wave can cause whistles, a low-pass filter with an attenuation of 60 dB at 5 kHz is incorporated in the audio output circuit. An i.f. trap is formed by the series-connected 270 pF capacitor and 470 μH inductor connected between the short-wave and long-wave aerial coils. To facilitate frequency counting for digital displays, the local-oscillator signal (I_0 2 mA_{max}, R_0 = 150 Ω) is available at a level of 200 mV peak at pin 10 of the TDA1072.



Detail of the photograph on page 122

TABLE 3
Noise performance of all-band a.m. radio

tuned frequency	required r.m.s. aerial signal for (S + N)/N =		
	6 dB	26 dB	46 dB
long-wave, 200 kHz	17 μV	200 μV	2.7 mV
medium-wave, 1 MHz	7.3 μV	90 μV	1.3 mV
short-wave, 6.1 MHz	8 μV	100 μV	1.3 mV

PERFORMANCE OF THE CIRCUIT

With a 1 $V_{r.m.s.}$ aerial signal, the total a.f. distortion is less than 2%. The 3 dB bandwidth of the h.f. stages is 12 kHz at a tuned frequency of 600 kHz and is 36 kHz at a tuned frequency of 1600 kHz. The required aerial signal levels for S/N ratios of 6 dB, 26 dB and 46 dB are given in Table 3.

ACKNOWLEDGEMENT

The author wishes to thank A.C.Smaal and J.M.A. Spoorenberg of the Elcoma Central Application Laboratory, Eindhoven, for their contributions to the circuit designs and information contained in this article.

Abstracts

Introduction to PWM speed control system for 3-phase AC motors.

The described speed control system uses the variable frequency principle, high performance and efficiency being obtained by a sinusoidal modulation of the width of the pulses supplied to the motor. A purpose-designed LSI circuit has been developed for signal generation. The analogue control system provides for the correct operation and protection of all functions. A fast dynamic response is obtained even under braking conditions.

Mains pollution caused by domestic appliances

Part 2 — Harmonic distortion

The current popularity of phase control as a means of power regulation in domestic appliances, has led to a sharp increase in harmonic distortion of the mains supply. Future regulations (particularly those being prepared by the IEC) are likely to place severe constraints on the use of phase control devices and other devices not covered by the present CENELEC Standard EN 50 006. This article discusses the major causes of harmonic distortion, and shows by way of example how it can be reduced significantly by judicious circuit design.

A flexible LSI frequency synthesiser system

Two LOCMOS LSI integrated circuits can be used to produce a flexible, low-cost, frequency synthesiser with a professional performance. The ICs contain all the critical circuits, both analogue and digital, to enable a programmable phase-locked-loop frequency synthesiser to be built easily and compactly. This article describes the ICs, their connection as a frequency synthesiser system, and the method used to overcome noise problems usually associated with phase-locked-loop frequency synthesisers. The novel technique for simplifying high speed frequency division (multiple feedback division) is also described.

Integrated Schottky Logic gate array

In the 8A1200 gate array, a new circuit technology called Integrated Schottky Logic (ISL) has been used, which combines the speed of Low Power Schottky and the high packing density of I^2L technology. The array comprises 1144 ISL gates, 52 Schottky buffers and 36 I/O cells. Logic equivalence indicates that the ISL array can replace up to 50 MSI and SSI TTL circuits in a typical system.

Digital control of radio and audio equipment

Part 6 — Voltage-controlled tuning of all-band a.m. radios

The need to reduce the space occupied by radio circuits, especially in car radios, and to make them compatible with digital control, has created an urgent requirement for a variable-capacitance tuning diode for tuning the long, medium and short-waves. The a.m. variable-capacitance diode pair BB212 meets the requirement. The article shows how awareness of a few specific requirements and observation of a number of simple design rules leads to the construction of high-performance home and car radios with diode tuning.

Beschreibung eines Systems zur Steuerung und Regelung der Drehzahl von Asynchronmotoren

Das behandelte Antriebssystem arbeitet mit einer Speisespannung, deren Frequenz geändert wird, wobei man einen hohen Wirkungsgrad dadurch erhält, dass man die Breite der dem Motor zugeführten Spannungsimpulse sinusförmig variiert. Für die Signalerzeugung wird eine speziell hierfür entwickelte LSI-Schaltung verwendet. Die analog arbeitende Schaltung, die auch im Bremsbetrieb schnell reagiert, erfüllt zuverlässig alle an sie gestellten Anforderungen.

Beeinflussungen des Versorgungsnetzes durch Haushaltgeräte

Teil 2 — Verzerrungen

Die gegenwärtige Verbreitung der Phasenanschnittsteuerung als Mittel zur Leistungssteuerung in Haushaltsgeräten hat zu einem starken Ansteigen der Verzerrungen der Versorgungsspannung geführt. Künftige Vorschriften (besonders die von IEC in Vorbereitung befindlichen) werden wahrscheinlich zu schwerwiegenden Auflagen führen bezüglich des Einsatzes von Bauelementen für Phasenanschnittsteuerungen sowie anderer durch den CENELEC Standard EN 50006 nicht erfasster Bauelemente. In diesem Artikel werden die Hauptursachen der Verzerrungen diskutiert und wird an Beispielen gezeigt, wie diese Verzerrungen durch eine wohldurchdachte Schaltungsauslegung wesentlich reduziert werden können.

Ein flexibeles LSI-Frequenzsynthesizer-System

Zwei LSI-Schaltungen in LOCMOS-Technik werden vorgestellt, mit denen sich ein flexibeler, preiswerter Frequenzsynthesizer mit professionellen Eigenschaften aufbauen lässt. Die integrierten Schaltungen enthalten sowohl die analogen als auch die digitalen Schaltkreise, die zum Aufbau eines kompakten, programmierbaren Frequenzsynthesizers mit Phasenregelschleife (PLL) erforderlich sind. Der Artikel beschreibt die beiden integrierten Schaltungen, das Zusammenschalten der IC's zu einem Frequenzsynthesizer-System und eine Methode, mit der die Rauschprobleme, die bei einem PLL-Frequenzsynthesizer auftreten, gelöst werden. Ebenfalls wird die auf der Grundlage von Mehrfachrückkopplungen beruhende neue Technik zur schnellen Frequenzteilung behandelt.

Ein Gate Array in ISL-Technik

Beim Gate Array 8A1200 wird eine neue Schaltungstechnologie verwendet, die den Namen Integrierte Schottky-Logik (ISL) trägt und die hohe Geschwindigkeit der Low-Power Schottky-Technik mit der hohen Packungsdichte der I^2L-Technik verbindet. Die Schaltung enthält 1144 ISL-Gatter, 52 Schottky-Puffer und 36 Ein-/Ausgabe-Zellen. Mit seinen Logikfunktionen kann das ISL-Gate Array in einem typischen System bis zu 50 MSI- und SSI-TTL Schaltungen ersetzen.

Digitale Steuerung von Rundfunk- und NF-Geräten

Teil 6 — Spannungsgesteuerte Abstimmung von Allband-AM-Rundfunkempfängern

Der Wunsch, das Volumen von Rundfunkempfängern, insbesondere Autoradios, zu reduzieren und die Empfängerabstimmung digital vornehmen zu können, hat zum Bedarf von Abstimmdioden geführt, die sich zur Abstimmung im Lang-, Mittel- und Kurzwellen-AM-Bereiches eignen. Das Abstimmdiodenpaar BB212 erfüllt die für die Abstimmung in den AM-Rundfunkbereichen erforderlichen Bedingungen. Der Artikel zeigt, wie die Kenntnis einiger spezieller Voraussetzungen und die Beachtung einiger einfacher Entwurfsregeln zur Konstruktion eines hochwertigen Heim- oder Autoradios mit Diodenabstimmung führt.

Présentation d'un système de commande à modulation à largeur d'impulsion pour les moteurs à courant alternatif

Le système de commande de vitesse décrit a recours au principe de la fréquence variable; les hautes performances et l'efficacité sont obtenues grâce à une modulation sinusoïdale de la largeur des impulsions fournies au moteur. Un circuit LSI spécialement conçu à cet effet assure la production du signal. Le système de commande analogique favorise le fonctionnement correct et la protection de toutes les fonctions. Une réponse dynamique rapide est obtenue, même dans les conditions de freinage.

Pollution du secteur causée par les appareils domestiques

2ème partie – Distorsion harmonique

La popularité actuelle de la commande de phase comme moyen de régulation de puissance dans les appareils domestiques se traduit par un net accroissement de la distorsion harmonique de l'alimentation secteur. Les règlements futurs (en particulier ceux que la CEI prépare actuellement) imposeront vraisemblablement de sévères restrictions sur l'emploi des dispositifs à commande de phase et d'autres dispositifs non couverts par la norme CENELEC EN 50 006 actuelle. Le présent article expose les causes principales de distorsion harmonique et montre à titre d'exemple comment on peut la réduire sensiblement par une conception judicieuse des circuits.

Un système synthétiseur de fréquence à LSI, très diversifié

Deux circuits intégrés LOCMOS LSI peuvent être utilisés pour constituer un synthétiseur de fréquence, peu coûteux et diversifié dans ses applications, offrant des performances de niveau professionnel. Les circuits imprimés suffisent à assurer toutes les fonctions critiques, aussi bien analogiques que numériques, de manière à permettre la construction simple et compacte d'un synthétiseur de fréquence à boucle d'asservissement de phase programmable. Le présent article décrit les circuits intégrés, ainsi que leur connexion dans un système synthétiseur de fréquence et la méthode utilisée pour résoudre les problèmes de bruit souvent inévitables avec les synthétiseurs de fréquence à boucle d'asservissement de phase. La nouvelle technique adoptée pour simplifier la division de fréquence à grande vitesse (division à contreréaction multiple) est également décrite.

Dispositif de porte ISL

Dans le dispositif de porte 8A1200, une nouvelle technologie de circuit a été utilisée. Il s'agit de la logique Schottky intégrée (ISL = Integrated Schottky Logic), alliant la vitesse de la technologie Schottky basse puissance et la grande densité utilisable inhérente à la technologie I^2L. Le dispositif comprend 1144 portes ISL, 52 tampons Schottky et 36 cellules entrée/sortie. L'équivalence logique indique que le dispositif ISL est capable de remplacer jusqu'à 50 circuits MSI et SSI TTL dans un système typique.

Commande digitale d'équipements radio et audio

6ième partie – Accord à commande de tension pour toutes les gammes radio en modulation d'amplitude

La tendance va vers une réduction toujours plus poussée de l'espace occupé par les circuits radio, surtout pour les équipements auto, et aussi pour les rendre compatibles avec la commande digitale. Ceci a suscité un besoin urgent envers une diode d'accord à capacité variable pour la recherche des stations dans les gammes d'ondes grandes, moyennes et courtes. La paire de diodes à capacité variable en modulation d'amplitude BB212 satisfait ces conditions. L'article montre comment l'observation de quelques impératifs spécifiques et le respect de quelques règles simples de conception ont abouti à la construction de récepteurs radio pour la maison et pour la voiture, avec accord par diode.

Introducción al sistema de control por modulación de anchura de impulso para motores de C.A.

El sistema de control de velocidad descrito emplea el principio de frecuencia variable, obteniendo elevado rendimiento y eficiencia mediante una modulación sinusoidad de la anchura de los impulsos suministrados al motor. Se ha desarrollado un circuito LSI especialmente diseñado para generación de señal. El sistema de control analógico proporciona el correcto funcionamiento y protección de todas las funciones. Se obtiene una respuesta dinámica rápida incluso en condiciones de frenado.

Polución de la red causada por aplicaciones domésticas

Parte 2 – Distorsión armónica

La popularidad del control de fase como medio de regulación de potencia en aplicaciones domésticas, ha conducido a un fuerte aumento en distorsión armónica de la alimentación de red. Regulaciones futuras (especialmente las que está preparando IEC) probablemente establecerán severas limitaciones sobre la utilización de dispositivos de control de fase y de otros dispositivos no abarcados por la actual norma CENELEC EN 50 006. Este artículo analiza las principales causas de distorsión armónica y muestra a manera de ejemplo como pueden ser reducidas significativamente mediante cuidadoso diseño del circuito.

Sistema sintetizador de frecuencia LSI flexible

Pueden utilizarse dos circuitos integrados LSI LOCMOS para obtener un sintetizador de frecuencia flexible y de bajo coste con unas características profesionales. Los circuitos integrados contienen todos los circuitos críticos, tanto analógicos como digitales, para que pueda construirse de modo fácil y compacto un sintetizador de frecuencia PLL (phase-locked-loop) programable. Este artículo describe los circuitos integrados, su conexión como sistema sintetizador de frecuencia y el método empleado para superar los problemas de ruido normalmente asociados con los sintetizadores de frecuencia PLL. También se describe la nueva técnica para simplificar la división de frecuencia de alta velocidad (división por realimentación múltiple).

Red de puertas ISL (Integrated Schottky Logic)

En la red de puertas 8A1200 se ha empleado una nueva technología llamada Lógica Schottky Integrada (ISL, Integrated Schottky Logic), que combina la velocidad de la tecnología Schottky de baja potencia y la elevada densidad de empaquetado de la tecnología I^2L. La red comprende 1144 puertas ISL, 52 buffer Schottky y 36 células entrada/salida. La equivalencia lógica indica que la red ISL puede reemplazar hasta 50 circuitos TTL de pequeña y mediana escala de integración (SSI y MSI) en un sistema típico.

Control digital de equipo de radio y audio

Parte 6 – Sintonía controlada por tensión en receptores de radio A.M. toda banda

La necesidad de reducir el espacio ocupado por los circuitos de radio, especialmente en autorradios, y hacerlos compatibles con control digital, ha creado el urgente requerimiento de un diodo de sintonía de capacidad variable para sintonizar ondas largas, medias y cortas. La pareja de diodos de capacidad variable BB212 satisface este requerimiento. El artículo muestra como el cumplimiento de algunos requisitos específicos y la observancia de cierto número de reglas de diseño conduce a la construcción de receptores de radio de elevadas características para hogar y automóvil con sintonía por diodo.

Authors

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Stephen Y. Lau received his Bachelor of Science degree in electrical engineering from Michigan State University and his Master of Business Administration degree from the University of Santa Clara. He joined the Bipolar LSI Division of Signetics Corporation in 1975 and specialised in the applications of bit-slice microprocessors and custom LSI; he is now product-line Marketing Manager for Custom LSI products.

Wim Rosink was born in Delden, the Netherlands, in September 1939. He studied electronic engineering at Enschede Polytechnic and received his Ing. degree there in 1959. After military service he joined the Central Application Laboratory of Elcoma, where he was at first involved in the design of wideband amplifiers. In 1967 he became engaged in application work on devices for power control, especially for speed control of d.c. and a.c. motors. As a market application engineer he is now responsible for contacts with numerous European customers concerned with power control.

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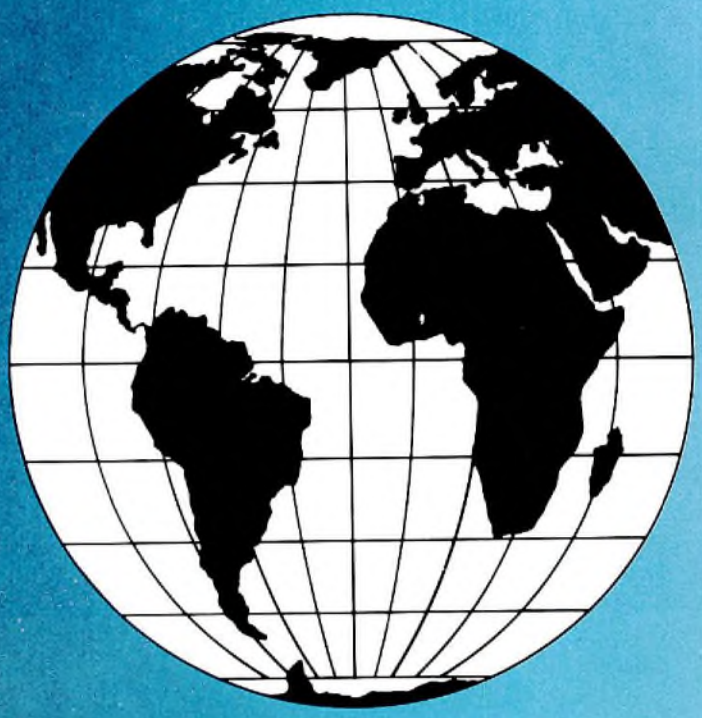

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