ELECTRONIC COMPONENTS & APPLICATIONS

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In 1927, the lady in this photograph was already benefiting from Philips' innovative approach to electronics. Since then, Philips has continued to be a major force in electronics, not only by manufacturing end-user equipment but also by making important contributions to technology, research and the development of components to meet the needs of set manufacturers world-wide. In the past we've seen important Philips innovations in TV, radio, cassette recorders, video-disc and compact-disc players. Today there are components from Philips Semiconductors in 100 Hz improved-definition TV sets, Laser Disc Players, portable VCR/TV combinations and personal compact-disc players. The near future will see the introduction of Radio Data Systems for programme/station identification, high-definition TV broadcasts via satellite, digital tape recording and interactive compact disc. Perhaps if the lady in the picture had turned her head to the right and seen the picture on the wall, she could have visualized the flat solid-state TV screen of the future.

Contents

Picture quality improvements in bus-controlled TV receivers

AXEL LENTZER

Although television is passing through a phase of rapid technological change, the definition of TV pictures is still limited by the restrictions imposed by the PAL, SECAM and NTSC transmission standards. Despite these restrictions, Philips have always fully exploited the latest advances in IC technology to develop signal processing ICs that offer TV set manufacturers the means to eliminate or reduce many of the effects that degrade the quality of TV picture. These effects include large-area flicker, edge flicker, line instability, line structure, crosstalk between the luminance and chrominance signals, and noise.

As a first step toward improved picture quality, we introduced large-area flicker reduction by 50 Hz/60 Hz to 100 Hz/120 Hz scan conversion using a field store of nine 256 K memories with gate arrays at the inputs and outputs.

The second step was the introduction of an economy large-area flicker reduction system using the SAA9088 memory controller and four 1-Mbit VDRAMs. This system used three ADCs at the input and three DACs at the output. It also included an analog picture signal improvement IC TDA4670 for colour transient improvement (CTI) and luminance peaking.

We have now taken a giant step along the road to picture quality improvement by developing a field/frame memory-based chip-set which can eliminate or reduce nearly all the effects that degrade TV picture quality. Moreover, it's also completely future-proof because it's compatible with the 16:9 picture format that will eventually be required for EDTV and HDTV (1250 lines, f_H = 32 kHz).

The heart of the new chip-set is a second-generation memory controller SAA4950 and an SAA7158 for line-flicker reduction (LFR) processing and D to A conversion. The new chip-set extends the picture quality improvements to include line flicker reduction, thereby providing the first truly flicker-free TV picture. The SAA7158 also includes improved Digital Colour Transient Improvement (DCTI), luminance peaking, and three DACs for the YUV signals. There is also an SAA4940 for noise/cross-colour reduction.

ARCHITECTURE OF THE VIDEO/ DEFLECTION SIGNAL PROCESSING CIRCUITRY

The aims of Philips in designing picture quality improvement ICs have always been to achieve the highest feasible level of integration, and to strike an ideal balance between flexibility, cost-effectiveness and performance. This automatically led to the use of analog colour decoding and the definition of a YUV/sync interface between the colour decoder and the video/deflection signal processing stages where an Improved Picture Quality (IPQ) module could be inserted to provide the required digitally-processed picture quality improvements. This arrangement is shown in Fig.1. For set manufacturers who prefer to use a digital colour decoder, an 8-bit device that fits into the IPQ architecture will soon be available.

The IPQ module is controlled via the I²C-bus[1] and a microcontroller with an on-chip I²C and UART interface (e.g. a PCB83C652). This modular architecture is not only cost-effective, but also offers set manufacturers considerable flexibility of design because it is not only independent of the transmission standard being received, but also allows the picture quality improvements to be added step-by-step.

[1] Purchase of Philips I²C components conveys a license under the Philips I²C patent to use the components in the I²C system, provided the system conforms to the I²C specifications defined by Philips.

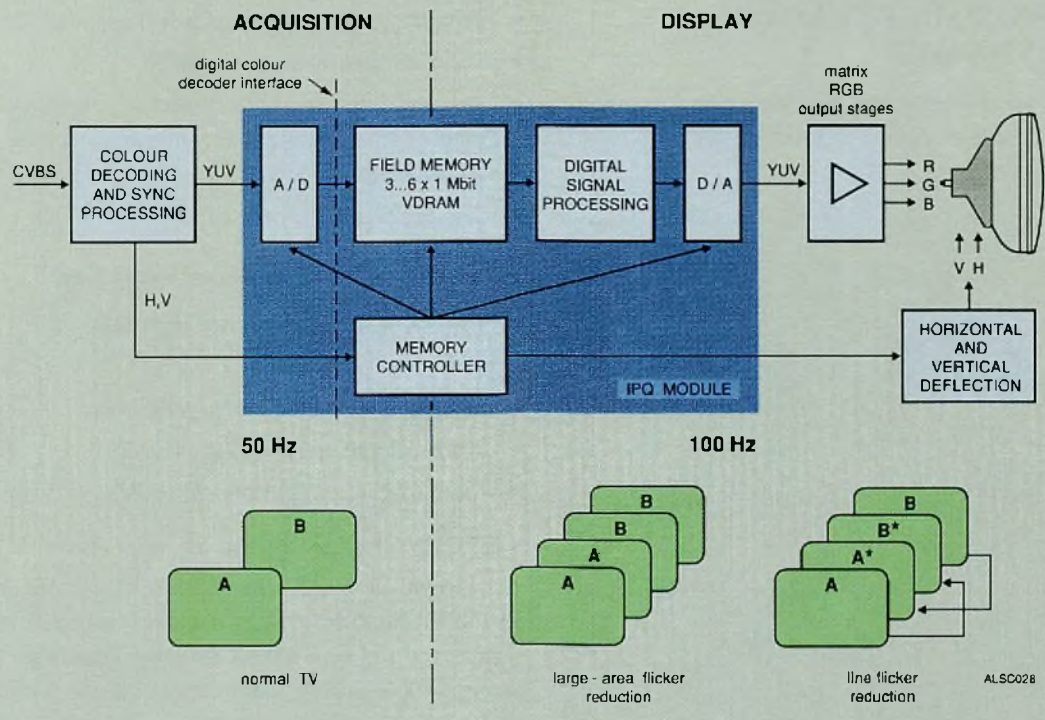

Fig.1 Architecture of the video/deflection signal processing section of a TV receiver with picture quality improvement

The picture quality improvements obtained with a particular IPQ module depend on the type of signal processing ICs it contains and the capacity of the VDRAM(s). For example, a full-options IPQ module with a YUV sampling ratio of 4:1:1 contains two 3-Mbit VDRAM memories for storing two picture fields, an SAA4950 third-generation bus-controlled memory controller, an SAA4940 for noise/cross-colour reduction, and an SAA7158 LFR processor and DAC circuit. The full-options IPQ module fully exploits the separated acquisition and display control capabilities of the memory controller. It allows simultaneous 50/60 Hz to 60/120 Hz scan conversion and line flicker reduction by an adaptive mix of field/frame repetition rate doubling. For frame rate doubling, the information for the extra fields is calculated by non-linear interpolation using median filtering of the luminance signal in the SAA7158. The SAA7158 also provides luminance peaking, improved Digital Colour Transient Improvement (DCTI) and high-speed D to A conversion (9/8/8 bits) of the YUV signals. Other features available with the full-options module include 4:3 to 16:9 aspect ratio conversion, still picture, strobe/cine mode and Multi Picture-In-Picture (MPIP) in conjunction with an SAB9070 Picture-In-Picture (PIP) processor. There is also a zoom facility for "letter box" expansion to allow full display of 4:3 wide-screen films on a 16:9 picture tube.

In an extended IPQ module there is only one 3-Mbit field memory and the SAA7158 is replaced by an SAA9065 video enhancement and DAC circuit. The SAA9065 is similar to the SAA7158 of the full-options module but without the adaptive line flicker reduction circuitry. This module therefore has no facility for line flicker reduction or zoom, but retains noise/cross-colour reduction and performs large-area flicker reduction by displaying each field twice to increase the field repetition rate from 50 Hz/60 Hz to 100 Hz/120 Hz.

An economy IPQ module can operate with a field memory comprising a 3-Mbit VDRAM (YUV sampling ratio 4:1:1) or a 4-Mbit DRAM (YUV sampling ratio 4:2:2). It is similar to an extended module, but has no facility for noise/cross-colour reduction.

The chip-set also includes a choice of multistandard colour decoder/sync systems, a Picture-In-Picture (PIP) processor with fast YUV multiplexers, and two video processors with automatic alignment of RGB cut-off (TDA4680 and TDA4686) and white-point (TDA4680 only). There is also an advanced deflection controller which features computer-controlled alignment of the raster geometry, and a teletext decoder for operation in the 100 Hz domain.

COLOUR DECODING/SYNC PROCESSING USING COLOUR DECODER TDA4650

Figure 2 shows an analog system for dual colour decoding/sync processing for the normal picture and for Picture-In-Picture (PIP) processing.

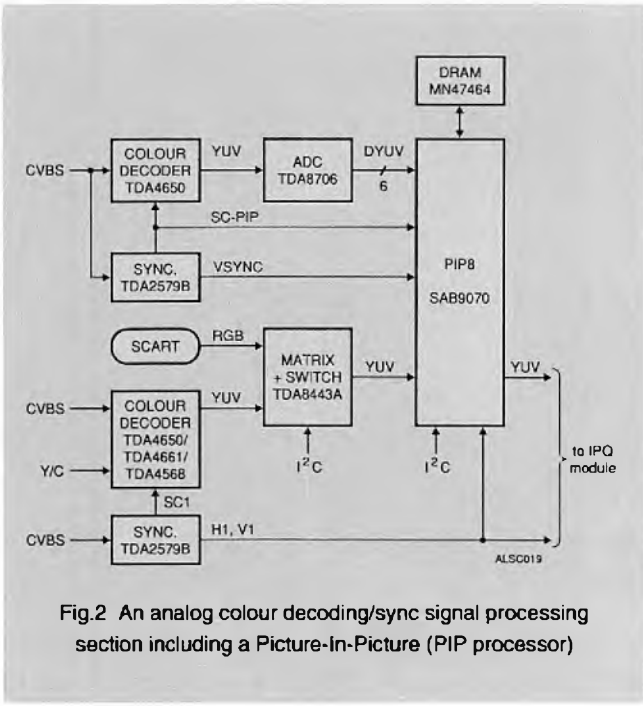

Fig.2 An analog colour decoding/sync signal processing section including a Picture-In-Picture (PIP processor)

The CVBS signal from the vision IF stage, or separate chrominance (C) and luminance (Y) signals in S-VHS format from a VCR, are decoded by the TDA4650 multistandard colour decoder. TDA4661 is an alignment-free CMOS switched-capacitor baseband delay line for the colour-difference signals. TDA4568 is the luminance delay line. The H and V sync signals are generated by synchronization circuit TDA2579B. External wideband RGB signals from the SCART connector are fed to the TDA8443A source switch/matrix IC to obtain the luminance and colour-difference signals Y, U and V.

Features of the main ICs are as follows:

TDA4650 – analog multistandard colour decoder

- reliable, automatic transmission standard control and scanning sequence
- decodes PAL, NTSC and SECAM
- two crystal inputs with internal selection
- only one external SECAM reference circuit; two adjustments
- only one SECAM signal demodulator; no diaphotie (colour carrier crosstalk)
- four control outputs for external filter selection
- separate external de-emphasis capacitors for SECAM
- DC hue control input for NTSC
- standard-independent amplitudes at colour-difference outputs (in combination with the TDA4661 CMOS baseband delay line)
- few peripheral components.

TDA4661 – CMOS baseband delay line

- CMOS switched-capacitor technique
- alignment-free
- on-chip line-locked clock generation
- cross-colour reduction for NTSC
- low power consumption (35 mW).

SAB9070 – Picture-In-Picture processor

As shown in Fig.2, the CVBS signal for inserting a Picture-In-Picture (PIP) is decoded, and the YUV output signals are fed to a TDA8706 which contains a clamping stage, a triple analog multiplexer and one 6-bit ADC. The digitized YUV signals are processed by the SAB9070 PIP processor. Features of the SAB9070 are:

- multistandard (PAL/SECAM/NTSC) input
- can be used with different colour decoders
- built-in PAL delay line
- I^2C-bus control
- PIP size of 1/3
- PIP with horizontal resolution (YUV) of 192/32/32 pixels
- PIP vertical resolution (50/60 Hz) of 80/66 lines
- 6-bit quantization for Y, U and V signals
- requires 64K × 4-bit VDRAM
- seven horizontal, and nine vertical positions for the PIP
- single/double/large PIP modes
- 256 border colours
- on-chip PLL
- integrated analog YUV multiplexer for fast PIP insertion
- user-adjustable DACs for contrast and saturation
- multi-picture-in-picture (MPIP) in combination with an IPQ module
- special effects: luma key, mosaic and solarization.

The analog YUV outputs from the SAB9070, and the H and V sync signals from the main picture sync processor are fed to the Improved Picture Quality (IPQ) module.

COLOUR DECODING/SYNC PROCESSING USING ALIGNMENT-FREE COLOUR DECODER TDA9140

Figure 3 shows a more highly-integrated colour decoding/sync processing system in which the alignment-free colour decoder TDA9140 also performs the sync processing and RGB/YUV matrix functions. This system therefore requires only two ICs (a colour decoder and a baseband delay line) for colour decoding the main picture, plus a second colour decoder for PIP decoding. Features of the TDA4661 CMOS baseband delay line and the PIP processor have already been given.

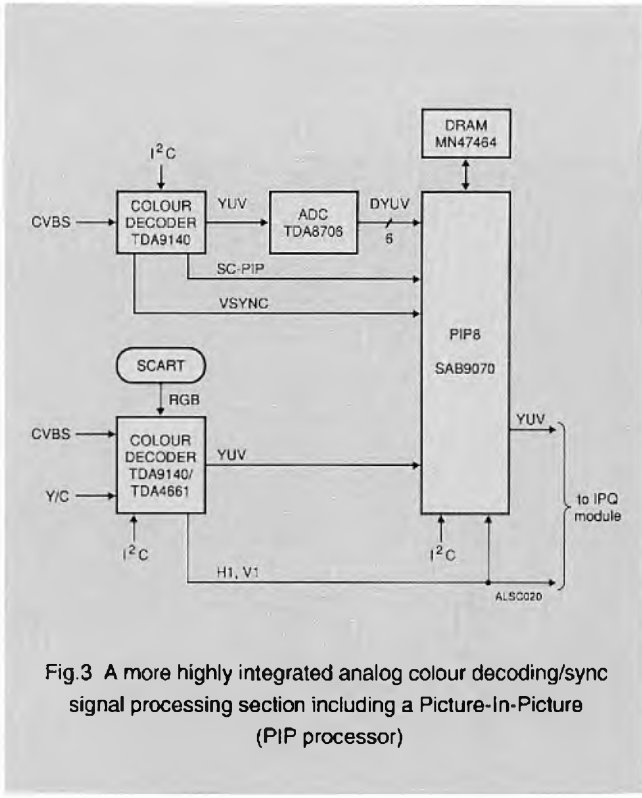

Fig.3 A more highly integrated analog colour decoding/sync signal processing section including a Picture-In-Picture (PIP processor)

TDA9140 – alignment-free colour decoder

Features of this multistandard colour decoder are:

- on-chip Y/C filtering
- reliable, automatic transmission standard control and scanning sequence
- decodes PAL, NTSC and SECAM
- I²C-bus controlled
- two crystal inputs with internal selection
- only one SECAM signal demodulator; no diaphotie (colour carrier crosstalk)
- two CVBS inputs
- RGB inputs with fast switch
- RGB/YUV matrix
- Y/C input
- Y/C input signal detection
- TXT output
- sync. separation and processing
- vertical divider system
- digital H and V line-locked clock outputs.

IMPROVED PICTURE QUALITY (IPQ) MODULES

There are three IPQ modules; a full-options version (Fig.4), an extended version (Fig.6) and an economy version (Fig.7).

After passing through anti-aliasing low-pass filters, the analog YUV signals are passed through individual 8-bit A to D converters. The luminance (Y) data consists of 8 data bits on 8 data lines. Depending on whether the YUV sampling ratio is 4:1:1, 4:2:2 or 4:4:4, the colour-difference (UV) data is organized in a sequential data format of 2 × 8 data bits on four, eight or sixteen bus lines respectively. For systems with a sampling ratio of 4:1:1 or 4:4:4, the correct data format is established by formatting logic after the A to D converters. If formatting logic is used, a luminance delay is incorporated to compensate for the colour-difference data delay.

Field memory

The IPQ modules use field memories consisting of VDRAMs operating as dynamic shift registers (FIFOs) with two independent clocks for write and read access. Double clock operation is a vital necessity for accommodating different transmission standards (e.g. PAL, D2-MAC) and different picture tube aspect ratios (4:3, 16:9). It also improves the stability of the display during VCR playback. As shown in Table I, the memory capacity required depends on the relative bandwidth (sampling ratio) of the YUV signals.

Field memory controller

The field memory is controlled by an SAA4950 memory controller. This IC controls the A to D and D to A conversion, and the memory read/write sequence so that the read and write picture data sequences don't overlap.

The VCOs associated with the SAA4950 can provide clock signals for operating the memory with several different input/output sampling rates. The standard input/output sampling rates for transmissions and picture tubes which both have a 4:3 picture aspect ratio are 13.5/27 MSPS (Mega Samples Per Second). For 4:3 pictures displayed on 16:9 picture tubes an input/output sampling rate of 12/32 MSPS or 13.5/36 MSPS is available, the higher rates being for use with fast VDRAMs. Some applications may require higher resolution than that recommended by CCIR 601. For this purpose, clocks for input/output sampling rates of 16/32 MSPS and 18/36 MSPS are available. As before, the higher rates are for fast VDRAMs.

The SAA4950 memory controller also provides a 27 MHz clock for a deflection processor and a teletext decoder.

Features of the IPQ modules

All IPQ modules have the following features:

- large area flicker reduction by 50/60 Hz to 100/120 Hz scan conversion
- 4:3 to 16:9 aspect ratio conversion
- improved digital CTI
- luminance peaking
- still/strobe/cine mode
- multi PIP (in conjunction with PIP controller SAB9070)
- drive clock for text and deflection controller
- fully I^2C-bus controlled.

Additional specific features for each IPQ module are given in Table 1.

TABLE 1 Specific features of IPQ Modules

	IPQ module				
	Full-options		Extended	Economy	
sampling ratio (YUV)	4:1:1	4:4:4	4:1:1	4:1:1	4:2:2
data word length (bits)	12	24	12	12	16
memory capacity (Mbits)	2 × 3	6	3	3	4
requires formatting logic	yes	yes	yes	yes	no
Signal processing ICs used					
TDA8709: ADC	3		3	3	3
SAA4950: memory controller	1		1	1	1
SAA9065: video enhancement and DAC circuit			1	1	1
SAA4940: noise/cross-colour reduction	1		1		
SAA7158: LFR processor and DAC circuit	1				
PCB83C652: microcontroller	1		1	1	1
Features					
line flicker reduction	yes	no	no	no	no
suitable for processing RGB signals	yes	yes	yes	yes	yes
noise/cross-colour reduction	yes	no	yes	no	no
zoom 1 ("letter box" expansion)	yes	no	no	no	no
zoom 2 (× 2 expansion)	yes	no	no	no	no

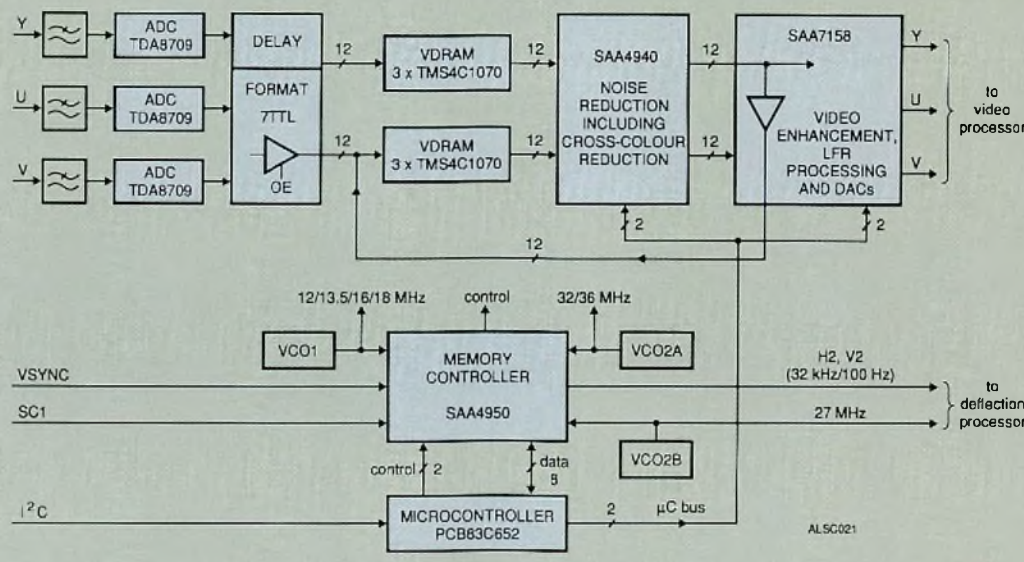

Fig.4 Block diagram of a full-options IPQ module

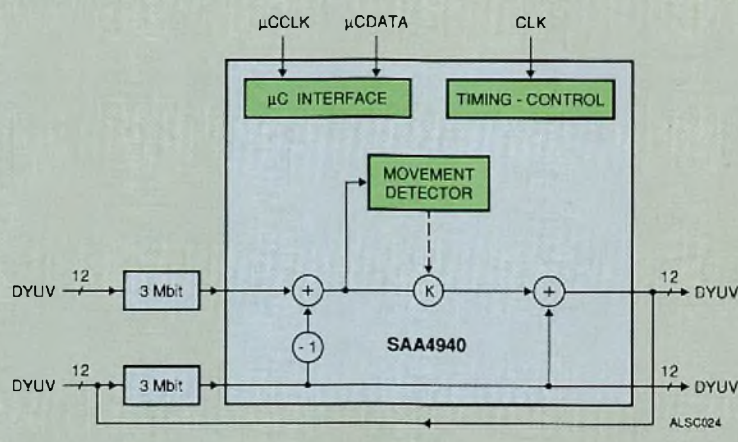

Fig.5 Simplified block diagram of the SAA4940 noise reduction IC

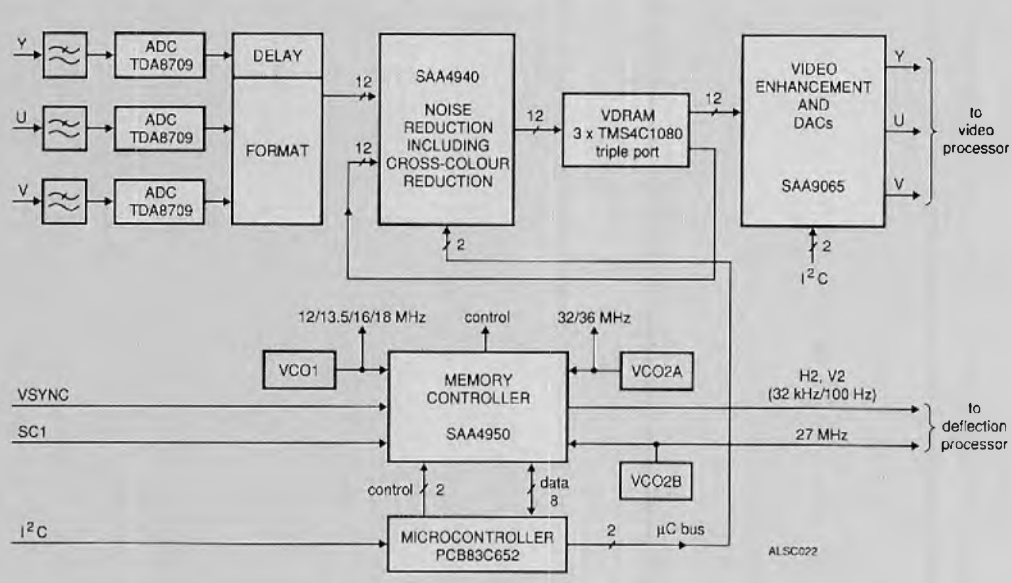

Fig.6 Block diagram of an extended IPQ module

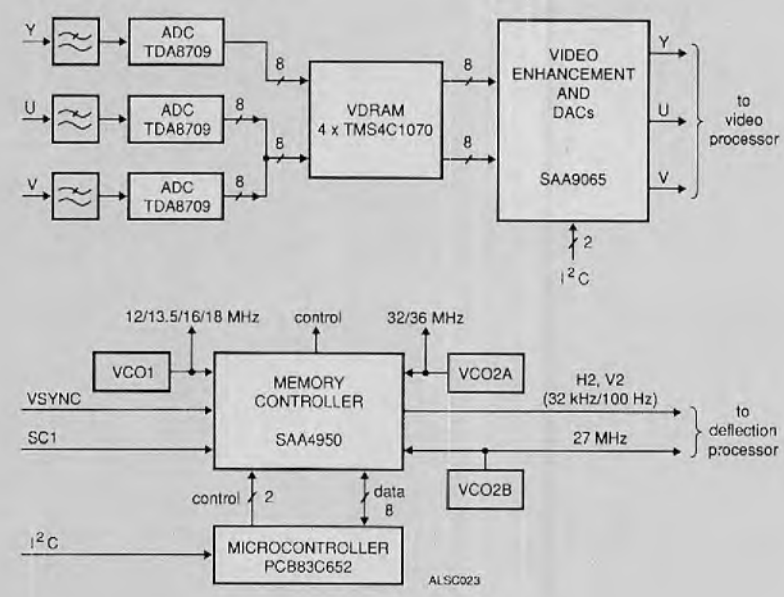

Fig.7 Block diagram of an economy IPQ module

Full-options IPQ module

With large-area flicker reduction by storing YUV data for each picture field in a memory and reading it out twice at double the write clock frequency (linear interpolation), there remains a problem in large stationary areas of the picture. Temporal vertical interlace combined with mainly temporal alias components causes residual flicker on thin horizontal lines or sharp edges. Adding a second field memory to allow frame repetition eliminates flicker in stationary areas of the picture. Furthermore, due to the full 100 Hz interlace of 1:2, even the line structure and line crawl becomes invisible.

The full-options IPQ module shown in Fig.4 uses two 3-Mbit field memories and an SAA7158 LFR processor and DAC circuit at the output. This allows an adaptive combination of picture field and frame display rate doubling to be implemented to achieve 50/60-Hz to 100/120 Hz scan conversion and simultaneous elimination of line flicker.

The full-options IPQ module also incorporates an SAA4940 noise reduction IC which reduces noise and cross-colour interference by recursive filtering using the field memory as the delay element as shown in Fig.5. The k-factor can be constant (non-adaptive noise reduction) or can be controlled in eight steps between 0 and 1 by a movement detector via the fast microcontroller bus (movement-adaptive noise reduction). Other features available with the SAA4940 include:

- colour generation for side panels, box or border
- pixel repetition for side panels
- split-screen noise reduction inside or outside box for demonstration purposes
- solarization
- 4:4:4 throughput

The SAA7158 contains the circuitry for implementing the line flicker reduction by an adaptive mix of field repetition (linear interpolation) and frame repetition (non-linear interpolation by 3-point median filtering). A more detailed description of this function is given in the Appendix.

The SAA7158 also performs colour-difference signal re-formatting, Digital Colour Transient Improvement (DCTI), Y-signal peaking and high-speed D to A conversion of the YUV signals.

In some applications involving film transmissions (e.g. saving a photo-finish sequence or serving a video printer) a kind of flicker reduction can be obtained by using one of the memories as an active field memory, and the other as a background memory. For this purpose, the SAA7158 includes a feature called "movie phase" detection. For a cinemascope film transmission, the "movie phase" detector identifies a first and second field with the same video content. This may force the IPQ module to switch to "cine mode" under control of the I^2C-bus which would result in four lines with the same video content and interlace (a perfect image free from line or field flicker).

For a full-options IPQ module operating in the 4:1:1 mode, the SAA7158 provides two additional features called zoom 1 and zoom 2. Zoom 1 provides vertical expansion of the video. This allows 4:3 aspect ratio "letter box" transmissions to be displayed as a full-screen picture on a picture tube with a 16:9 screen. Zoom 2 provides × 2 magnification of the video both horizontally and vertically.

For operation with RGB signals, full Y and U,V bandwidth can be obtained by operating a full-options IPQ module in the 4:4:4 mode. However, in this mode it is no longer possible to benefit from the noise reduction, line flicker reduction, or either of the zoom facilities. We therefore recommend that the 4:4:4 mode should only be used for signals from perfect RGB sources. For less perfect RGB signals, we recommend that the 4:1:1 mode still be used so that the full range of picture improvements remain available.

Extended IPQ module

Figure 6 is a block diagram of the extended IPQ module. Its main purpose is to eliminate large-area flicker by converting the field repetition rate from 50/60 Hz to 100/120 Hz. This is achieved by storing YUV data for each picture field in a 3-Mbit VDRAM field memory and reading it out twice at double the write data clock frequency. It also has noise and cross-colour reduction with the SAA4940 as previously described

The final IC in the extended IPQ module is the SAA9065 Video Enhancement and DAC circuit which replaces the SAA7158 used in the full-options IPQ module. The CMOS SAA9065 operates at a data rate of 13.5 MHz to provide colour-difference signal re-formatting horizontal peaking for the digital luminance signal, and Digital Colour Transient Improvement (DCTI) for the chrominance signals. One of the features of the DCTI is that the luminance and chrominance signals remain time-related, regardless of the steepness of the transient. The SAA9065 also contains the three high-speed D to A converters (9/8/8 bits) for the YUV signals.

Economy IPQ module

Figure 7 is a block diagram of the economy IPQ module. It performs the same functions as the extended IPQ module except noise/cross-colour reduction. The least expensive version of this IPQ module has a YUV sampling ratio of 4:1:1 and a 3 Mbit memory. However, with a YUV

sampling ratio of 4:2:2 as shown in Fig.7, the chrominance bandwidth is increased and it is not necessary to use formatting logic between the ADCs and the 4-Mbit field memory.

I²C-bus control

All the functions of the IPQ modules are controlled via the I²C-bus which sends control signals, via the microcontroller, the memory controller and a fast microcontroller bus. The functions that can be controlled include the k-factor in the noise reduction IC, CTI steepness, Y peaking, and line flicker reduction on/off in the SAA7158. The functions of the Video Enhancement and DAC circuit SAA9065 in the simpler IPQ modules are controlled directly via the I²C-bus.

VIDEO OUTPUT/TELETEXT/ DEFLECTION SIGNAL PROCESSING

Figure 8 is a block diagram of the video output, teletext and deflection signal processing section of an TV receiver with picture quality improvement.

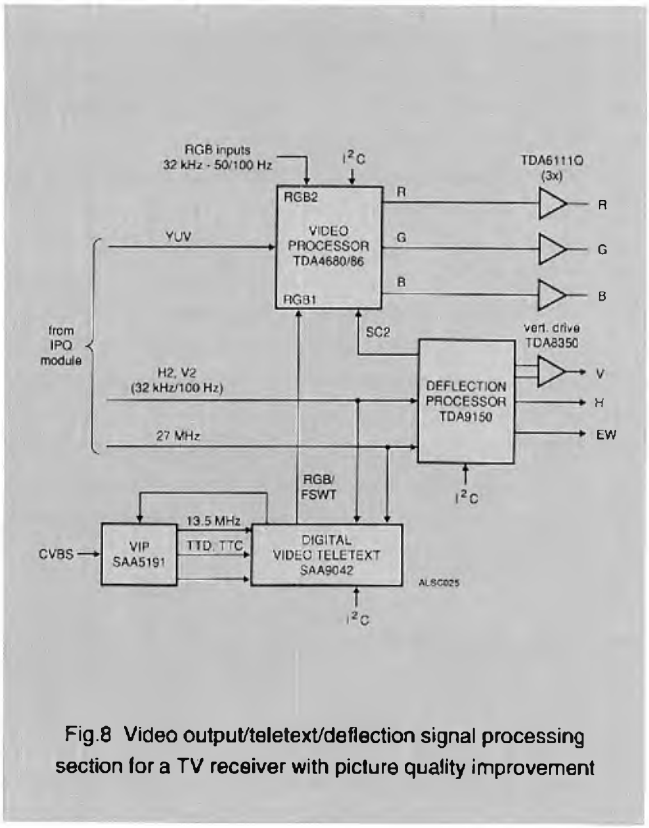

Fig.8 Video output/teletext/deflection signal processing section for a TV receiver with picture quality improvement

Video output signal processing with the TDA4680/86

The analog, standard-independent baseband YUV signals from the IPQ module are fed to the TDA4680 video control combination which automatically controls RGB cut-off and white-balance. The TDA4680 matrixes the YUV signals to RGB in a PAL/SECAM or NTSC matrix. Two other sets of RGB input signals (e.g. videotext or SCART inputs) can be selected via switching pins associated with the signal source, or via the I²C bus. The contrast, brightness, and even the saturation adjustment acts on the YUV and RGB signals.

Measuring periods are provided for automatic RGB cut-off adjustment with picture tube leakage current compensation and white-point adjustment. The RGB cut-off adjustment is repeated for each field and the control values are stored in capacitors. The white-point setting can be stored in a non-volatile memory in the I²C-bus controlled microcontroller so that the measuring line (field sequential) can be switched-off if not required. The currents measured during one "white" line are compared with the reference value for the optimum white-point (stored as a code in a non-volatile memory in the I²C-bus controlled microcontroller). The result of the comparison can be read-out via the I²C-bus and a correction made by the microcontroller. This ensures that the white-point remains correct throughout the life of the TV set.

The bandwidth of the video and RGB channels has been chosen to accommodate broad-band applications like double line and field frequencies. The RGB signals are amplified to a nominal peak-to-peak level of 2 V and their DC levels are shifted in accordance with the cut-off control. The output signals are suitable for driving integrated wide-band video amplifiers (e.g. TDA6111Q).

The TDA4686 video control combination is similar to the TDA4680 but without automatic white-point adjustment.

Features common to the TDA4680/86 are:

- I²C-bus control
- brightness, contrast and saturation control of the luminance and colour-difference signals
- hue control for the multistandard colour decoder
- two sets of switchable inputs for analog RGB signals from external sources
- selection of PAL/NTSC matrix
- white-point control
- two- or three-level sandcastle pulse reception
- selectable automatic RGB cut-off control or RGB output clamping

- compensation for leakage current of the picture tube if automatic RGB cut-off control is selected
- signal limiting by contrast control
- two switch-on delays for run-in without discolouration.

Additional features of the TDA4680 are:

- memory registers for RGB cut-off and white-point reference data
- white-point comparators
- automatic white-point adjustment via the I²C-bus
- white measuring lines within selectable blanking periods
- saturation control for external RGB signals
- I²C-bus transceiver
- line counter for measuring line position control via the I²C-bus
- typical bandwidth: ≥12 MHz/3 dB.

Additional features of the TDA4686 are:

- I²C-bus receiver only
- start of measuring lines with V-pulse in the sandcastle or with an extra vertical flyback pulse
- typical bandwidth: ≥20 MHz/3 dB.

Teletext decoding with the SAA9042

The SAA9042 is an I²C-bus controlled Digital Video Teletext (DVT) IC which acquires, decodes and displays 625-line and 525-line World System Teletext. It is used with an SAA5191 teletext Video Input Processor (VIP) and a single-chip 64 K × 4-bit or 256 K × 4-bit DRAM page memory.

Features of the SAA9042 are:

General

- directly interfaces up to 1 Mbit of DRAM
- fully-independent acquisition and display timing
- three display modes:
  - normal
  - 32 kHz (progressive scan)
  - 100 Hz/120 Hz (field doubling)
- single +5 V power supply.

Acquisition

- simultaneous update of up to 8 pages
- up to 100-page memory capability
- software selectable 625/525-line operation
- VBI and full-channel operation.

Display

- stable display by slaving from scan-related timing signals
- automatic selection of up to seven different languages
- software controlled RGB level eliminates the need for hardware adjustment
- up to 27 display rows; 0 to 24 plus 1 or 2 status rows.

Features of the SAA5191 (VIP) are:

- high-performance adaptive data slicer
- data clock regenerator
- 13.5 MHz character display clock derived from a PLL including an adaptive sync separator; the design of the PLL allows the display to be locked to the TV line scan for stable status messages.

Deflection signal processing with the TDA9150

The final IC in the chip-set is the advanced BICMOS TDA9150 deflection processor which requires only one resistor in its functional peripheral circuitry. This IC, which is designed for optimum operation in the 16 kHz/50 Hz or 32 kHz/100 Hz environment, automatically aligns the geometry of the raster under control of the I²C-bus and contains the output stages for E-W correction as required for 110° picture tubes. Since the internal offsets and linearity errors of the TDA9150 are very low, it can provide vertical drive within the frequency range 23 Hz to 132 Hz for a DC-coupled TDA8350 vertical deflection output IC.

Advantages of directly-driven vertical deflection compared to conventional AC-coupled drive are:

- avoids the disturbing effects caused by the long settling time of an AC-coupled loop ('bouncing')
- eliminates the need for linearity adjustment
- eliminates costly coupling capacitors.

The TDA9150 requires a clock frequency of 6.75 MHz/13.5 MHz for 16 kHz line deflection, or 13.5 MHz/27 MHz for 32 kHz line deflection. In the application described, it receives a clock frequency of 27 MHz from the SAA4950 memory controller in the IPQ module.

Parameters that can be controlled via the I²C-bus are:

vertical scan

- amplitude
- S-correction
- shift
- EHT compensation
- interlace/non-interlace
- deflection start.

horizontal scan

- phase
- shift
- clamping pulse shift.

E/W raster geometry correction

- width
- parabola
- corner
- trapezium
- EHT compensation.

Features of the TDA9150 are:

- peripheral circuitry consists of only one resistor
- vertical frequency range 23 Hz to 132 Hz
- horizontal frequency 16 kHz/32 kHz
- clock controlled (432/864 clocks/line)
- H-pulse control (t_p = 0 to 55%)
- differential vertical drive output for TDA8350 vertical output IC
- the vertical placement of the spot on the screen is clearly defined by a sawtooth output voltage with 14-bit resolution
- allows fully computerized raster geometry adjustment during set manufacture
- on-chip protection circuit
- clock input 6.25/13.5/27 MHz (pin-controlled)
- full raster geometry correction.

TV PICTURE IMPROVEMENT – A CONTINUING QUEST

There are still several years to wait for High Definition TV (HDTV) broadcasting of wide-screen (16:9 aspect ratio) pictures with 1250 lines. The first step toward HDTV will be Extended Definition TV (EDTV) to provide wide-screen pictures from satellite broadcasts using the D(2)-MAC transmission standard or from terrestrial broadcasts using the PAL PLUS standard.

Meanwhile, Philips keeps TV set manufacturers abreast of the latest picture quality improvement techniques by offering advanced signal processing ICs to increase the customer appeal of their existing designs.

APPENDIX – PRINCIPLES OF ADAPTIVE LINE FLICKER REDUCTION

In a full-options IPQ module (Fig.4), one field memory acts as a 50 Hz to 100 Hz display rate converter (13.5 MHz write clock, 27 MHz read clock). The other field memory (both clocks 27 MHz) provides fast storage of another field for data processing.

Adaptive line flicker reduction with the SAA7158 effectively combines the advantages of field and frame repetition rate doubling to simultaneously create a 100 Hz display and reduce line flicker without adding visible defects.

As shown in Fig.A1, the basic field sequence of a 100 Hz flicker-free display is A A* B* B in which A and B are the fields of the 50 Hz sequence with new fields A* and B* inserted between them. The 4-field frame of this 100 Hz display scheme offers three advantages with regard to fields A and B:

- fields A and B are correctly positioned in the 100 Hz interlace raster
- fields A and B are not in the wrong temporal position
- the contents of fields A and B are not affected or degraded by signal interpolation.

The remaining problem is the insertion of new fields A* and B*. As mentioned in the main text, linear interpolation alone gives unsatisfactory results. Instead, to maintain the correct temporal sequence for moving scenes, it is necessary to use an adaptive method of flicker reduction which automatically switches between a "moving scene" mode and a "stationary scene" mode. In the "moving scene" mode, field A* is filled with the contents of field A, and field B* is filled with the contents of field B (field repetition). In the "stationary scene" mode, field A* is replaced with field B, and field B* is replaced with field A (frame repetition).

Adaptive switching between the two modes is commonly controlled by complex motion detectors or edge detectors. Neither of these is needed with the SAA7158 LFR processor and DAC circuit because it uses non-linear interpolation by a vertical median filter to act as an adaptive switch between field and frame repetition.

One of the most attractive properties of median filtering is the invariance of the step response which means that edges are not blurred as with linear interpolation. The 100 Hz field sequence is generated as follows:

for field A:

$$\{a_{x,y}\} = \{a_{x,y}\}$$

for field A:*

$$\{a^*_{x,y}\} = \{\mathrm{med}(a_{x,y}, a_{x,y+1}, b_{x,y})\}$$

for field B:*

$$\{b^*_{x,y}\} = \{\text{med}(b_{x,y},\ b_{x,y+1},\ a_{x,y+1})\}$$

for field B:

$$\{b_{x,y}\} = \{b_{x,y}\}$$

In these equations, "a" is the actual field, "b" is the previous field, "x" is the horizontal axis of the display, and "y" is the vertical axis.

For natural scenes, this signal processing results in a good quality picture, but distortion due to the non-linearity of the median filter become visible with test pictures. Although vertical signal components at 1/3 of the vertical sampling frequency are suppressed, the 3rd-order harmonic gives rise to alias components. These cause distortion that must be regarded as the penalty for line flicker reduction in most other types of picture. With one exception, they can be neglected.

At the intersection of f_{hor} = 1/3 and f_{vert} = 1/3 in the spatial frequency domain, there is a fairly visible "centre" of alias. Because of the 13.5 MHz sampling clock, residual components of the PAL colour subcarrier may occasionally cause annoying distortion. These defects are eliminated in the SAA7158 by × 2 up-sampling the luminance median operation to an invisible frequency range while the colour-difference signals are averaged over two lines.

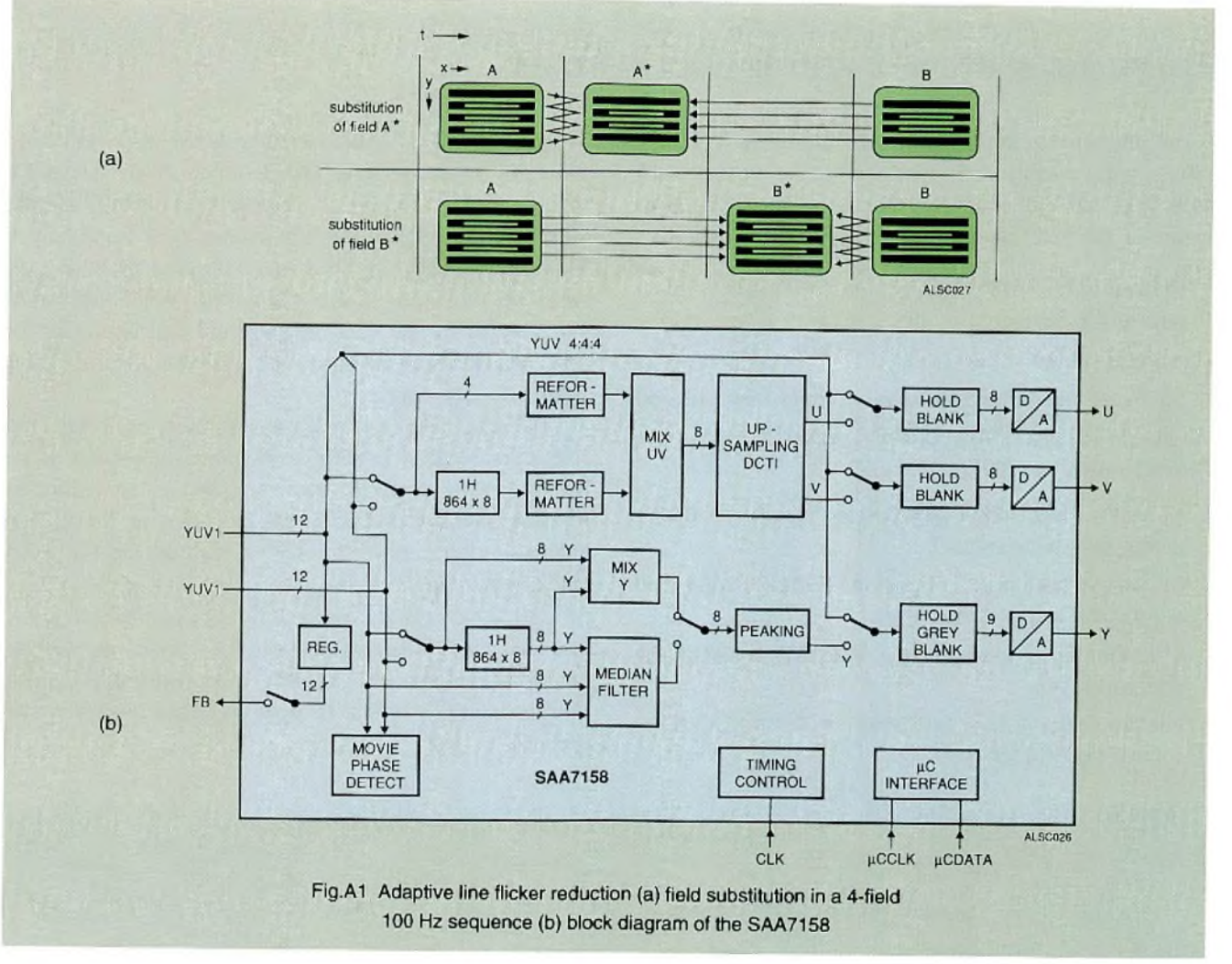

Fig.A1 Adaptive line flicker reduction (a) field substitution in a 4-field 100 Hz sequence (b) block diagram of the SAA7158

REFERENCE

B. Laue, G. Müller and J.Wohlerdt "100 Hz flicker-free feature module with memory controller SAA9088" Philips Semiconductors Laboratory Report No. HTV9002; ordering code: 9398 077 10011.

A Frame Grabbing Application using the 66470 and 68070

WOLFGANG SCHWARTZ AND JEAN-CLAUDE SIX

Frame grabbing is the procedure of digitizing a picture from a video source and storing it in the system/video memory of the Video and System Controller (VSC). This feature of the VSC can be used in applications such as:

- desk-top publishing
- remote surveillance
- machine vision
- digitizing e.g. either TV, VCR or Video Disk pictures.

As shown in Fig.1, the following main functions are required around the SCC66470 VSC:

- an analog video source (e.g. a video camera) to deliver a composite video signal
- an analog-to-digital conversion (ADC) section to digitize the analog video input
- a system/video memory (e.g. DRAM) to store the digitized image
- a microcontroller (e.g. SCC68070 or SCC90CXXX) to control the SCC66470 VSC.

The SCC66470 is synchronized with the video source in Slave TV mode or Slave DUAL mode. In the Slave TV mode, the VSC receives a vertical sync signal from the video source and generates a horizontal sync signal output. This latter signal is synchronized with the horizontal sync signal in the video source via a PLL which delivers a clock signal to the VSC. In the Slave DUAL mode, the VSC receives both the horizontal and vertical sync signals from the video source.

The VSC grabs the video image frame by frame. The frame grabbing bit in the display command register is set by software to invoke the frame grabbing action at the start of each frame, and reset at the end of each frame. The analog-to-digital conversion section includes the TDA8703 and external latches.

Different hardware configurations can be used to allow grabbing of 8 bit/pixel monochrome images as well as colour images. It is also possible to use two VSCs to attain double resolution so that 16 bit/pixel colour images can be grabbed.

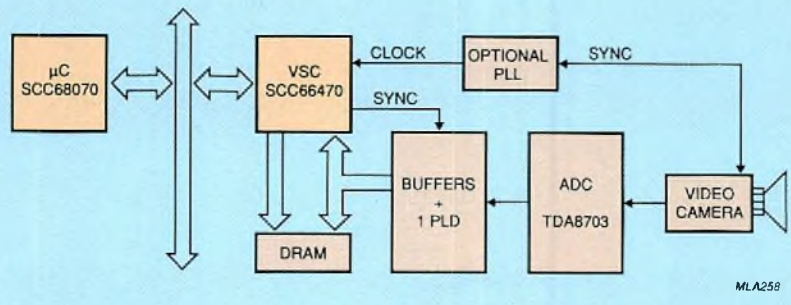

Fig 1. VSC in Frame grabbing application

Integration and performance

The high integration of advanced ICs such as the SCC68070 32-bit microprocessor and the SCC66470 (VSC) has greatly reduced the cost of graphics-based interfaces.

The SCC66470 VSC is for applications where integration and performance are key criteria. It incorporates a dynamic RAM controller for video or system memory, display control logic, a pixel accelerator for fast image manipulation and an interface for an optional graphics co-processor. The SCC68070 is a general purpose 68000 code-compatible processor with advanced features (memory management unit, direct memory access controller).

The VSC approach is a cost-effective solution. The 66470 also opens up new markets for graphics-based displays in novel areas like process control systems, motor vehicle dashboards, test equipment, and small office equipment such as state-of-the-art photocopiers.

THE 66470 VSC, THE 68070 MICROPROCESSOR AND THE MICROCORE EVALUATION BOARD

General

The 66470 is a video and system controller in CMOS technology and is compatible with the data bus of the 68000 family. Operating with the 68070 microcontroller, and a video controller of this "bit map" type, they perform a number of functions that minimize the logical "glue" required for building small systems.

The two circuits are ideal for applications involving user-friendly man/machine interfaces. They combine high integration, superior performance and low costs.

Philips Semiconductors Markets an evaluation board for these two circuits under the name "Microcore". Using this board we have been able to develop and examine the video acquisition possibilities of the VSC. Before considering the different functions of the VSC it is necessary first to give a brief description of its "preferred companion", the 68070.

The 68070 microprocessor

The 68070 is compatible at bus level with the 68000 family and includes a central unit with a 68000 compatible instruction set, thus allowing easy transcription of the logic developed for this processor.

What makes this product original is that most of the functions required by high-performance systems are integrated in one unit. A single chip integrates in either 84-pin PLCC or QFP120 packaging:

- A 32-bit central unit with 68000 compatible architecture
- A memory management unit
- Two completely independent DMA channels, (up to 3 Megatransfers/second)
- A serial asynchronous communication interface (up to 38000 baud)
- Three programmable delay counters compatible with a minimum resolution of 5.5 µs
- One I^2C bus, controller allowing transfer at up to 100 kbits per second (the integral bus controller can be configured as either "master" or "slave" and can address up to 128 peripherals). This allows, for example, the connection of a diskette controller and, in DMA mode, to transfer an image from a magnetic carrier to the video memory.

Video controller function

The VSC has a "bit map" controller that can function with either 4 bits or 8 bits per pixel, thus permitting the creation of images with 16 or 256 grey levels or in colour.

The image format can be programmed in several modes between 224×210 pixels and 768×560 pixels, the resolution attainable being dependent on the selected number of bits per pixel. The pixels are extracted by a serialization register (shifter) operating at up to 15 MHz. This register extracts the data via the internal bus of the VSC. It is possible to decode images stored in memory in the formats: *bit map, Run Length*, or *mosaic*. The pixels, after decoding and serialization, are transferred to the video port. Depending on the operating mode selected, these are either in the 4 bits/pixel or 8 bits/pixel format. They can then be processed by a DAC or a colour circuit. The simplest device for digital conversion is a resistive network.

The VSC can be programmed for 50 or 60 Hz. Display can conform to TV standards or be compatible with dual-frequency monitors, other frequencies being possible as a function of the crystal frequency used for the oscillator and the display mode chosen. Scanning can be programmed as interlaced, non-interlaced or repetitive.

The synchronization signals, line, raster and composite video signals are available together with the blanking signal (active while line and raster are suppressed). Synchronization of the VSC with an external video source or another VSC is possible. It is thus possible to arrange several VSCs in parallel so that the number of bits affecting each pixel can be increased. The frequency of the quartz oscillator is selectable between 20 and 30 MHz as required by the application. e.g. 24 MHz for a videotext application, 30 MHz for an application requiring full resolution.

The starting address for an image is programmable anywhere within the first megabyte of the DRAM (so long as the complete image remains within this memory space) thus allowing progressive displacements of the image in the horizontal and vertical directions.

Two sizes of screen are possible, either a reduced screen surrounded by a border in a programmable colour, or a full screen of the TV type.

Two modes of memory configuration are available:

- Physically organized: The memory space occupied by one video line corresponds exactly to the number of pixels on this line (in bytes or ½ bytes, depending on the pixel format)
- Logically organized: Since the memory space occupied by one video line is constant and equal to 512 bytes, the visualized portion of this line is shorter. Such an organization facilitates a horizontal shift of an image of n lines.

While horizontal and vertical suppression is active, the VSC can read information in memory. This may be useful for reloading some of its registers or for transmitting information to a colour circuit or another postprocessor. This principle can be used to generate subscreens. Two mechanisms are possible, one being active during the vertical return (ICA) and the other during the horizontal return (DCA).

At the start of each scan, the VSC reads the address 400H, the value of the DCA pointer designating the memory location of the instructions to be executed. When these have been completed and immediately before the start of the display, it restores the contents of the register pointer to the start of the VSR image and then displays the first line of the latter. At the end of each line the VSC "jumps" to the DCA instruction block and executes it if necessary. It then goes on to the next line and repeats the process until the end of the image.

The VSC can also acquire, in real time, an image from an external video source (Fig.2). A relatively simple interface is required for digitization and loading the pixels into memory.

Two principles of synchronizing the source and the VSC are possible:

(a) The VSC is synchronized by the external video source (video tape for example) which requires the use of a phase coupler.

(b) The source can be synchronized by the composite synchronization signal delivered by the VSC, eliminating the necessity for a phase coupler; this can be the case with certain cameras.

Rapid treatment of groups of pixels (PIXAC)

The PIXAC (Pixel Acceleration Unit) is a logic unit that allows rapid manipulation of pixels stored in memory by means of the CPU or a microprocessor. PIXAC operations are performed on 16-bit data representing 2 or 4 pixels and take less than 500 ns.

PIXAC can be used for:

- aligning source information with destination information
- comparing the value of one pixel with a reference
- modifying destination words in accordance with test results
- applying a mask to protect pixels not being manipulated
- applying a mask with the object of modifying certain bits of a pixel
- applying a logic function to the final result.

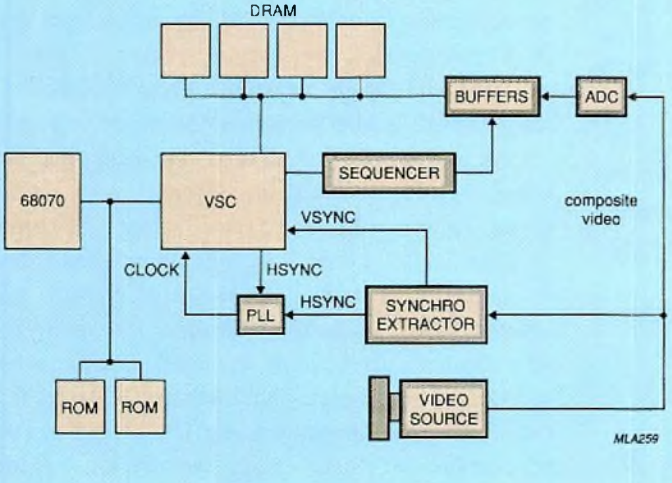

Fig 2. The VSC can also acquire, in real time, an image from an external source

The final result can also be compressed or expanded by a factor of 2; or a bit-pixel or pixel-bit transformation can be performed, when displaying characters for example.

The Microcore board: a system requiring minimum development

The Microcore board uses only 9 circuits on a double-sided board of normal Euro format, to provide a bit map image management system, an RS232 interface for connection to a host computer or a terminal, and a storage monitor and ROM, the whole constituting a system requiring minimum development.

OPERATING VIDEO ACQUISITION MODE

Video acquisition function of the 66470

The bit map video controller of the 66470 can both visualize a bit map image and control the storage of a digitized video image in RAM. Acquisition of a complete image is performed in one scan, or two scans in the case of an interlaced scan. All the functions dedicated to controlling storage are also available in the video acquisition mode ("frame grabbing"). It is therefore possible to program:

- the number of bits per pixel (4 or 8 bits/pixel)
- the horizontal resolution, with a minimum of 768 pixels per line, each pixel being coded with 4 bits
- the vertical definition, from 210 to 280 lines (or twice as many in the case of interlaced scan)
- the scan frequency, 50 or 60 Hz
- the type of scan: interlaced, non-interlaced, scan frequency or dual frequency
- the screen size: full or reduced
- the organization of the image in memory: physical or logical.

The VSC has three lines for the synchronization functions:

- line CSYNCN (pin 55): output for composite synchronization
- line HSYNCN (pin 83): input/output for horizontal synchronization
- line VSYNCN (pin 82): input/output for vertical synchronization.

These three lines are supplemented by:

- an input for selecting the mode of synchronization M/SN (master/slave pin 58) and two outputs for storage control signals
- a suppression signal BLANKN (pin 81)
- an active storage signal DA (pin 56).

The VSC can operate in several synchronization modes: "master" mode, "lave" mode, "dual slave" mode. These modes are programmable as a function of the levels applied at the input M/SN and on line CSYNCN, see Table 1.

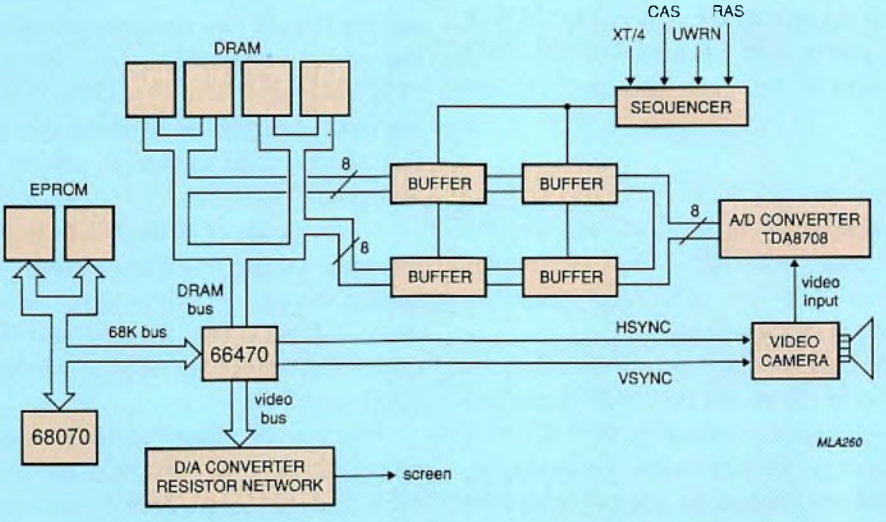

Fig.3 Video acquisition functions and modes

Table 1

MODE VSYNCN	M/SN	SYNCN DE = 0	SYNCN DE = 1	HSYNCN	
master	1	X	output SYNCN	output	output
slave	0	1 not earthed	output HSYNCN = 50%	output	input
dual slave	1	0 earthed	output phase difference	input	input

"Master" mode

In this mode of synchronization, the VSC generates the three signals VSYNCN, HSYNCN, DSYNCN. The VSC clock signal is supplied by the built-in oscillator by connecting the appropriate crystal (30 MHz for maximum horizontal resolution) across pins XTAL1 (119) and XTAL2 (2).

"Slave" mode

In this mode, the VSC generates the horizontal synchronization signal HSYNCN and receives the vertical synchronization signal supplied by a master source (TV, camera, video recorder, master VSC). Line CSYNCN is used as an output and delivers a signal with the same period and phase as the signal HSYNCN but with a cyclic ratio of 50%.

This signal is intended to be applied to the comparator of an external phase coupler. In fact, in this synchronization mode, the VSC must be supplied with a clock signal in phase with the horizontal synchronization signal originating from the master source. The output of a voltage controlled oscillator (VCO), is controlled by the signal HSYNCN and applied to the VSC input XTAL1 (119) of the circuit (the central frequency of this VCO must be identical to that of the crystal used to obtain the required frequency).

"Dual slave" mode

In this mode of synchronization, the VSC receives the signals HSYNCN and VSYNCN from a master synchronizing device. The line CSYNCN must be connected to earth via a 10 kΩ resistor.

The signal present at this output thus corresponds to the phase difference between the master HSYNCN signal and the HSYNCN signal internally generated by the VSC. This mode of synchronization is intended mainly for connecting several VSCs in parallel to increase the number of bits per pixel. One of these VSCs is configured as the master and supplies the horizontal and vertical synchronization signals to the remaining VSCs in the dual slave mode.

Configuration of the VSC for the "frame grabbing" mode

The VSC is provided with a software storage register. Within the 16 bits of this register, bit number 7 (FG) is concerned with the acquisition command. Setting the "frame grabbing" bit (FG) to 1 authorizes writing of the data presented on the bus (MD0 to MD15) to the image memory, starting at the memory address flagged by the register as the start of the VSR image. A complete image is acquired in one scan, or two scans in the case of the interlaced mode.

When register bit FG has been set to 1, video acquisition begins, immediately after the trailing edge of the first vertical synchronization pulse. During the *Grabbing* period of acquisition, the write signals of the upper and lower bytes of the DRAM bus controlled by the VSC are kept at logic level 1, thus allowing DRAM access by the system bus during the CPU window. It should be noted that in the interlaced mode acquisition always begins with the even scan.

When video acquisition has been completed the software register bit (7) FG automatically returns to 0. This bit can be read by the CPU which is thus able to detect the end of the acquisition phase. The data to be stored in memory during the acquisition phase must be obtained from a device external to the VSC. This must be capable of delivering to the DRAM data bus the digitized values resulting from sampling and the quantification of the composite video signal delivered by the source (camera, TV etc).

Logic interface

The logic interface is between the analog-to-digital converter which is used for sampling and quantification, and the DRAM bus which is controlled by the VSC. The memory incorporated on the Microcore board "TSC514256P10" can be addressed in page mode. Using this mode it is possible to access two words of 16 bits: the first addresses the column N (even), the second column N+1 (odd).

For this mode of addressing there is a fast page address sequence. During this sequence two words are written to DRAM during two consecutive Column Address Strobe (active LOW) CASN signals, each Row Address Strobe (active LOW) RASN display window is equal to two CASN windows.

When in the video acquisition mode software register bit (1) FG, the CPU window of each memory management cycle can be used. During this storage window it is necessary to insert synchronously at the memory inputs generated by the VSC, two 16 bit words representing 4 or 8 pixels in accordance with the bits/pixel ratio selected.

Synchronization function

We have seen that, among the three possible synchronization modes of the VSC, the modes "Slave" and "Dual Slave" require the extraction of synchronization signals for line and frame as well as the control of the VSC clock frequency.

In "Master" mode, the video source synchronizes itself using the Composite Synchronization Signal (CSYNCN) generated by the VSC.

Extraction of the synchronization signals

This function can be easily handled by a horizontal combination IC like the TDA2595. This IC has the necessary functions to extract the synchronization signals and generate the necessary signals for the horizontal and vertical synchronization of for example a TV set. This component has the advantage of being able to recognise synchronization pulses as low as 50 mV. The TDA2595 receives the composite video signal and outputs the composite synchronization signal.

The extraction of the synchronization signals for frame and line are done using a Phase Locked Loop circuit. The heart of circuit can be an NE564. It integrates a voltage controlled oscillator, an amplitude limiter and phase comparator.

Synthesis of the logic interface for the 8 bits/pixel format

The function of this interface is to convert the stream of 4- or 8-bit data leaving the ADC into words of 16 bits, i.e. the format required by the data bus DRAM. Moreover, two 16-bit words must be fed to the bus for each activated acquisition cycle.

Each of these words must be fed to the bus in such a manner that it can be written to memory following the trailing edge of the signal CASN. For that purpose, the set-up time and the hold time for the memory used must be taken into consideration. In the present case, the set-up time is 5 ns and the hold time 15 ns. If we need to view the image this is done on the leading edge of the signal CASN during the acquisition phase, and this also ensures the image is readable on the data bus by the pixel serializer. Once again, a set-up time of 5 ns and a hold time of 15 ns must be respected.

The buffer register

This is a pipeline register analogous to a two level, 16-bit FIFO register, the input stage of which can be used for writing two bytes in parallel. Input/output operations for such a register take place in the following manner: the two 8-bit bytes are applied to the input positions of the FIFO register and input when the FIFO is addressed, and output from the FIFO pipeline register by applying a clock pulse.

With a format of 8 bits/pixel we can acquire 384 pixels during the 51.2 microseconds active period of a video line. This leads to the adoption of a sampling frequency of 7.5 MHz, i.e. the clock signal XT4 which can serve as the sampling signal. The pixels are sampled at the leading edge of the XT4 signal and stored at the trailing edge of the same signal, which allows a maximum conversion time of 66 ns.

APPLICATION EXAMPLE

The following application is an example of a remote surveillance system and an associated algorithm of image compression.

Thanks to the large possibilities offered by the Microcore board and its associated frame grabbing card, it is quite simple to develop a cost effective remote surveillance system. Using the Philips monochrome camera 56474, it offers the possibility of synchronizing the camera with an external signal, so allowing the VSC to work in the "Master" mode.

The communication of the images and related information can be performed via a normal telephone line, running at 9600 baud, or lower, or via a ISDN line (see Fig.4).

After a frame is grabbed, and before the image is seen, the 68070 can be used to compress the image, and compute the number of bytes to send. The reception of the image will be made using the RS232 port of the Microcore board. This will take care of the decoding and the display of the image on for example a monitor.

With the availability of the I^2C-bus, ICs like I/O ports for the man-machine interface, clock/calender etc can easily be added to the system.

Methods of image compression

Various techniques exist for image compression, but in general there are two different methods:

Exact methods

They allow you to recover exactly the sampling of the original digital image: run length, supported by the VSC is one.

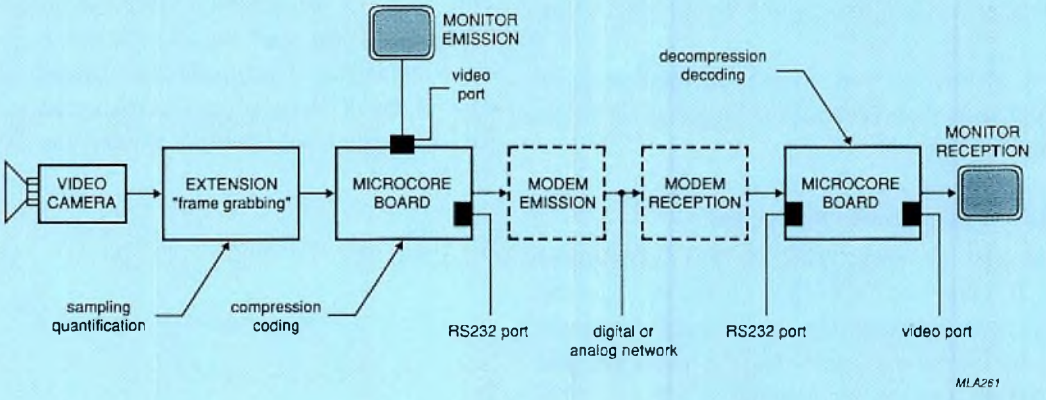

Fig 4. Camera surveillance application

Psycovisual methods

These methods bring some distortion to the reconstructed images exploiting the properties of the eye, so any distortions introduced are not visible.

Among the various methods, the "Block Truncation Coding" or (BTC) is one of the most powerful. This method gives very low distortion of the reconstituted image together with a very good image compression factor. The algorithm to be implemented can be easily handled by the 68070 cpu.

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Colour monitor tubes with ARAS coatings

JOS RIJNDERS AND ANDRE VAN DER VOORT

Philips 14" HiRes+ and 21" (51FS) colour monitor tubes are available with an advanced anti-reflection/antistatic screen coating that provides maximum operator comfort and excellent visibility in even the harshest ambient light conditions.

The coating is one of the most effective anti-reflection/ antistatic screen treatments currently available. Known commercially as ARAS (for Anti-Reflection AntiStatic), it comprises a multilayer structure of transparent dielectric material that suppresses specular reflections by broadband interference effects at the screen surface. The antistatic properties are provided by a single conductive layer within the multilayer structure.

ARAS is standard on our 51FS monitor tube and available as an option in our 14" HiRes+ range.

With ARAS, the intensity of reflected light is reduced from around 4.5% of the incident light (the reflectivity of uncoated screens) to *less than 0.5%*. It also has a major advantage over other screen treatments in that it doesn't diffuse or scatter the reflected light, so picture contrast and sharpness remain completely unimpaired. ARAS is also easy to clean and is tough enough to withstand all commercially available cleaning agents.

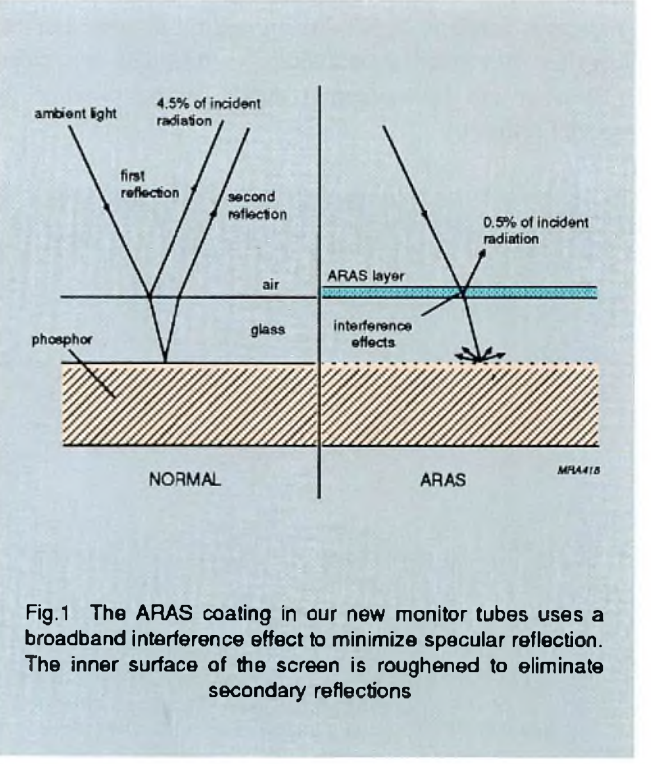


Fig.1 The ARAS coating in our new monitor tubes uses a broadband interference effect to minimize specular reflection. The inner surface of the screen is roughened to eliminate secondary reflections

DIRECT DEPOSITION

ARAS is normally deposited by electron-beam evaporation onto glass panels that are then glued to the screen. In the 51FS and in our HiRes+ range, however, we deposit the ARAS coating *directly* onto the screen, giving the tubes the advantages of:

- better picture quality with no glass panel to introduce distortion
- higher screen transmission since ARAS also reduces back reflection of light emitted by the phosphor
- harder, more scratch resistant coating since the ARAS layer after deposition undergoes the sintering effects that occur during frit sealing and subsequent tube production processes. (*Meets MIL-C-675A standard for hardness.*)

Because ARAS reduces specular reflections so dramatically, secondary reflections i.e. internal reflections from the inner surface of the screen could become a serious problem (since they are then the major contributor to reflected light). We eliminate these by roughening the inner surface of the screen to create a diffusing reflective surface.

REST-COLOUR OPTIONS

Figure 2 shows the reflected intensity as a function of wavelength for our current range of ARAS screens. These screens have a *rest colour* (a mean reflected spectrum) in the blue region of the visible spectrum so that the residual reflected ambient light appears blue. If, for aesthetic reasons, customers should prefer a different rest colour (green or red for example) these can be provided by special request.

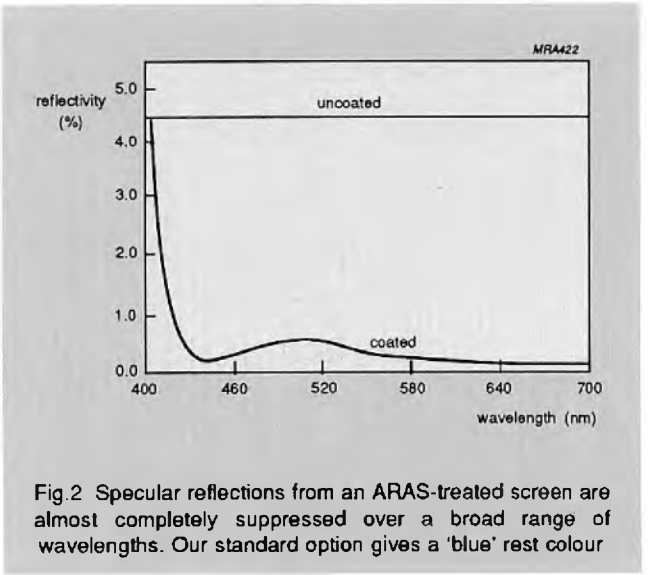


Fig.2 Specular reflections from an ARAS-treated screen are almost completely suppressed over a broad range of wavelengths. Our standard option gives a 'blue' rest colour

PERFORMANCE IMPROVEMENTS WITH ARAS

Black level

For any monitor screen, the black level, i.e. the brightness of the unexcited phosphor areas, provides a limit on contrast. In a bright working environment, these areas will reflect more light and the difference in brightness between excited and unexcited areas (and hence the contrast) will be reduced. As Fig.3 shows, it's under these conditions that the performance of an ARAS-treated screen really comes into its own.

The figure relates to the light intensity variations of a 14" monitor tube displaying a typical test signal, i.e. a vertical bar pattern producing intensity excursions from black level to peak white. The relative black level measurements were taken with the screen subjected to direct illumination of 160 lux from a non-diffuse (specular) source.

Under these conditions, the relative black level exhibited by the uncoated screen is around 93% of peak white which means that the test signal would be only just visible on the screen. Any increase in ambient lighting conditions (sunlight passing through a window for example) would then cause the pattern to be completely obscured.

Contrast that with the performance of the ARAS-coated screen. Even with 160 lux illumination, the relative black level is only around 30% of peak white, leaving around 70% available to provide contrast and accommodate signal variations and increases in ambient lighting conditions.

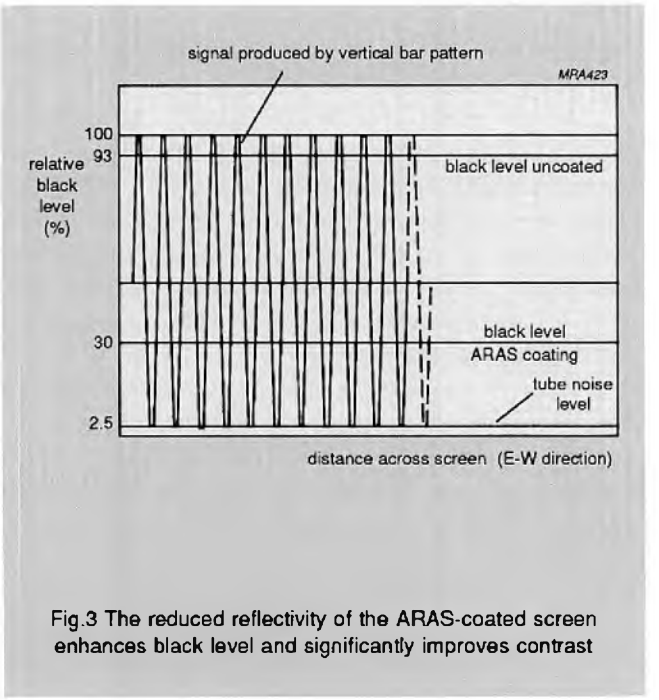


Fig.3 The reduced reflectivity of the ARAS-coated screen enhances black level and significantly improves contrast

Subjective contrast improvement

Black-level and contrast-ratio measurements give a good objective assessment of the performance to be expected from an ARAS-coated screen, but such measurements make little allowance for the observer's visual perception. To take this into account, Fig.4 compares the radiant energy reflected from the screen with the *eye curve* (the spectral sensitivity of the average eye). As with the curves of Fig.2, both the uncoated (high gloss) and ARAS screens (with blue rest colour) are shown.

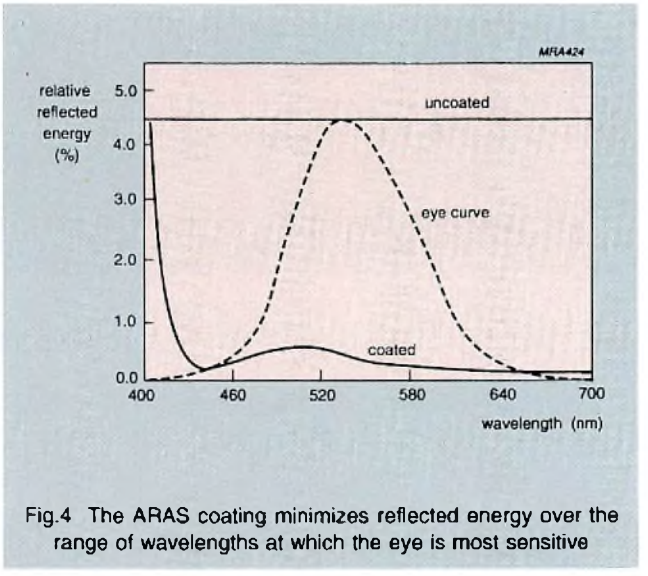


Fig.4 The ARAS coating minimizes reflected energy over the range of wavelengths at which the eye is most sensitive

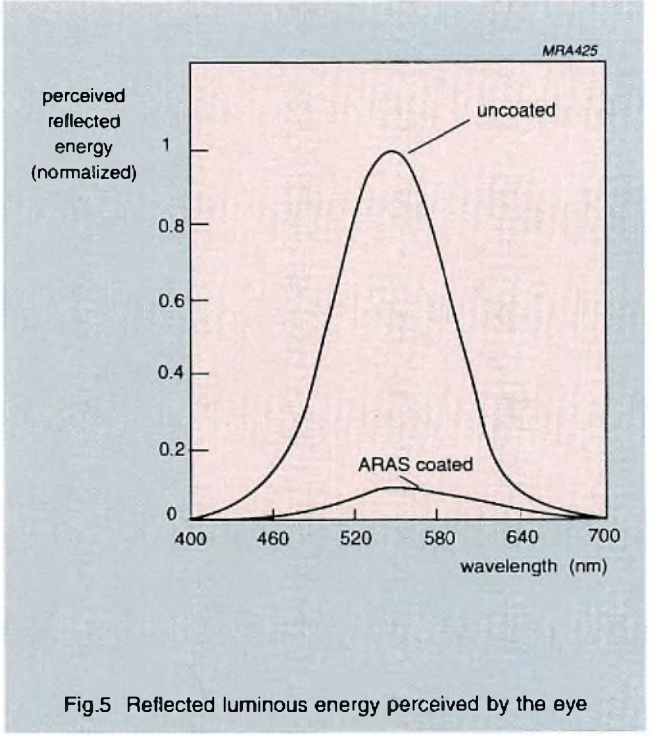


Fig.5 Reflected luminous energy perceived by the eye

At each wavelength, the product of the reflected intensity level and the corresponding eye curve level is an indication of the radiant energy that can be perceived by the eye at that wavelength. Figure 5 gives this *perceived* energy as a function of wavelength for both the coated and uncoated screens. The area under each curve gives the total reflected energy (normalized) that can be perceived by the eye and from the figure it can easily be demonstrated that the drop in reflectivity from 4.5% to 0.5% by applying an ARAS coating leads to a *twenty-fold* reduction in this perceived reflected energy.

Screen brightness

An important quality of the ARAS coating is that it is bi-directional, i.e. it suppresses not only specular reflection of ambient light falling on the screen, but also internal reflection of radiation emitted by the screen phosphor. This property, which is not exhibited by other commercially available screen coatings nor by direct-etch screens, reduces reflective losses compared with these other screen finishes and gives an approximate 3% improvement in light output.

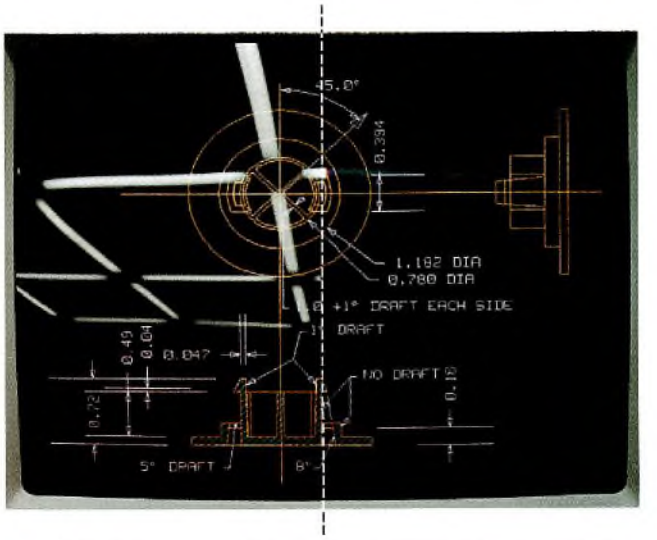


Fig.6 Split screen – high gloss left, ARAS right. The ARAS screen is much more comfortable to work with

ANTI-STATIC PROPERTIES OF ARAS

The advantages of anti-reflecting monitor screens are rather obvious: easier working in bright surroundings, better visibility and hence less operator eye-strain. The advantages of antistatic coatings are somewhat less obvious but are primarily directed towards reduced chance of electrostatic discharge effects (such as the tingling sensation that comes when a hand approaches the screen) and reduced deposits of dust (and other aerosol materials) on the screen. Specific criteria for antistatic behaviour are all embodied in the MPRII requirements (see Ref.)

The ARAS coating on our monitor tubes is provided with an indium-tin oxide (ITO) conductive layer to eliminate electrostatic build-up on the screen. The ITO layer is capable of continuously discharging electrostatic voltages on the screen up to 20 kV and meets the most stringent Nordic requirements (including those of MPRII).

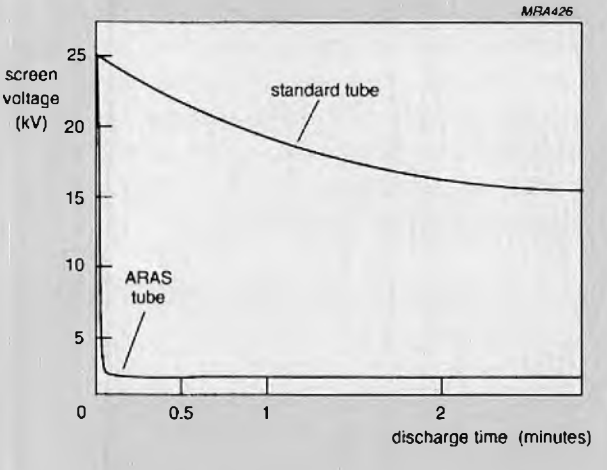


Fig.7 An ARAS treated screen will discharge from 25 kV to under 3 kV in less than a second from switch-on

Antistatic properties of ARAS-treated screens

	uncoated	ARAS
surface resistance	10^{12} Ω/□	= 10^{6} Ω/□
discharge time (voltage from 25 kV to 3 kV)	>10 min	<1 s

REFERENCE

MPR 1990:10 'Test methods for physical display units'; Swedish Board for Technical Accreditation (SWEDAC)

THE ¼ λ PRINCIPLE

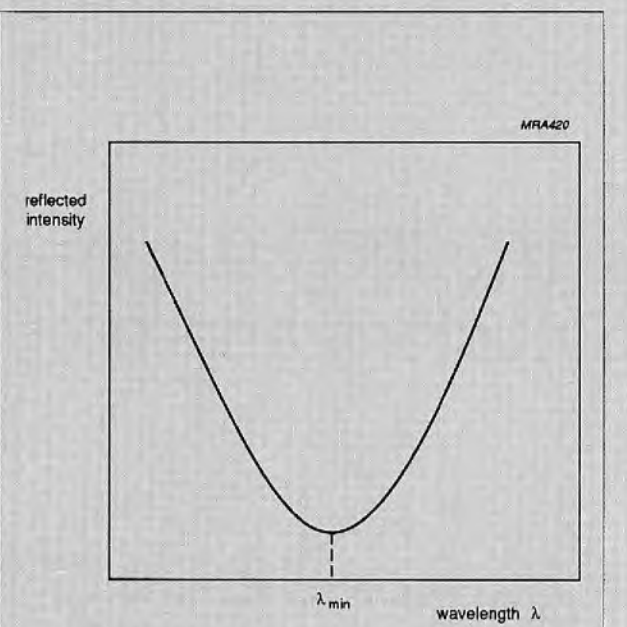
The principle of anti-reflection coatings using non-reflecting thin films has been known for a very long time. It's been used extensively in the optical industry, for example, to reduce reflection losses in multiple lens systems (in cine cameras and TV cameras for instance). Lenses that are treated in this way are said to be *bloomed*.

In its simplest form – *a single dielectric film* deposited on a glass substrate – radiation reflected from the front of the film (primary reflections) interferes destructively with radiation internally reflected from the back (secondary reflections) to produce an intensity minimum.

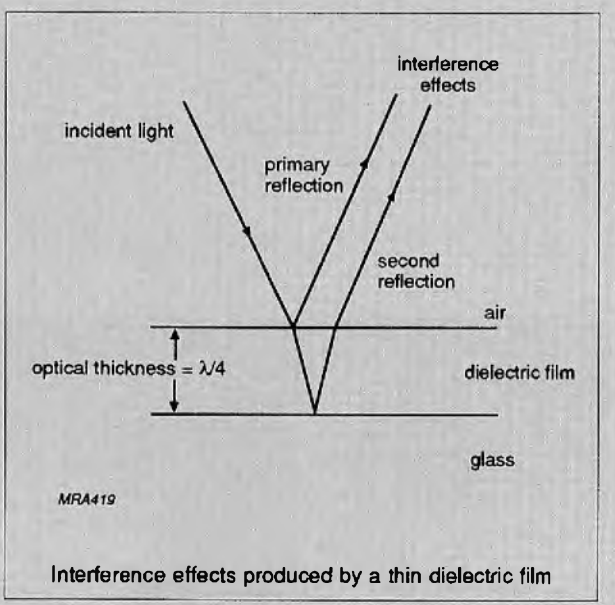
For zero reflected intensity at a particular wavelength λ, the refractive indices of the glass substrate n_g and of the thin dielectric film n_f must be related by $n_f = \sqrt{n_g}$ and the optical path difference between the primary and secondary reflected radiation must be an odd number of half wavelengths.

The first condition, which in effect says that the primary and secondary reflected radiation must of equal amplitude, is usually impossible to realize in practice (because of the limited choice of dielectrics available) and this means that the reflected intensity will never truly be zero. The second condition is satisfied by making the optical thickness of the film ($n_f t$) equal to a ¼λ*.

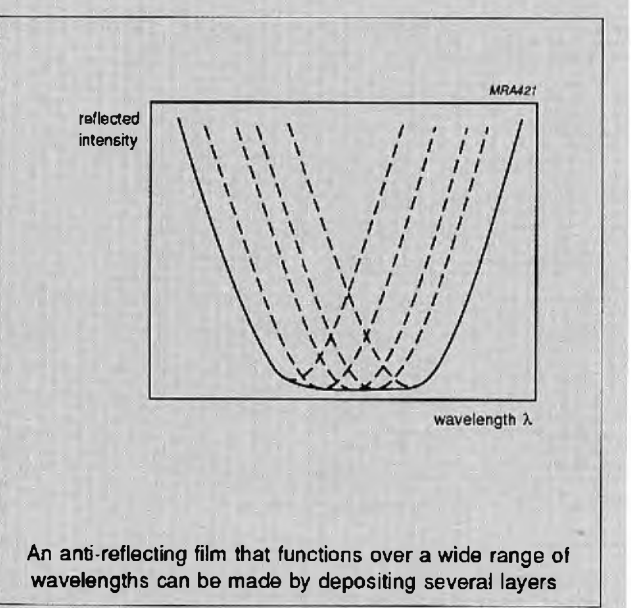
A single thin film gives an intensity minimum at one wavelength only. It's possible, however, to produce anti-reflecting films that function over a wide range of wavelengths by depositing several layers whose refractive indices decrease progressively from the glass towards the air. This is the principle of the ARAS coating.



Specular reflections from a thin film reach a minimum at a single wavelength λ_{min} equal to 4 × the optical thickness of the film



Interference effects produced by a thin dielectric film



An anti-reflecting film that functions over a wide range of wavelengths can be made by depositing several layers

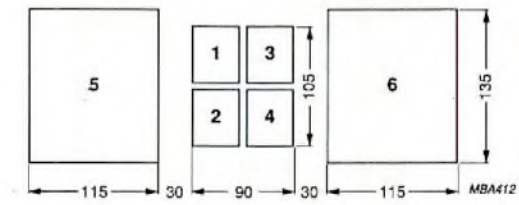
* In theory any odd number of quarter wavelengths will do provided the optical path difference between the primary and secondary radiation doesn't exceed the coherence length of the incident radiation

TSA9000T – monolithic photo-detectors and preamplifiers (PDP)

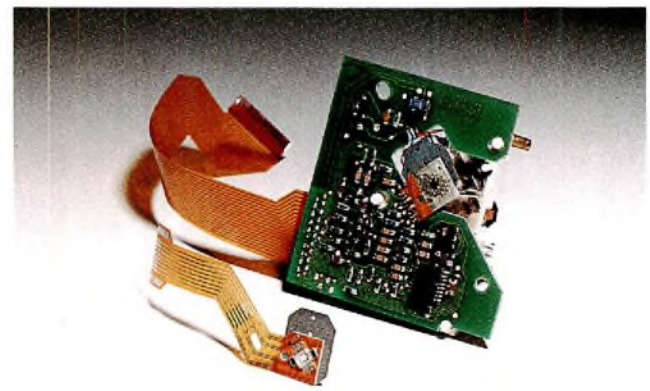
For optimum interference-free coupling between the optical and electronic systems of Laser Disc (LD) and Compact Disc (CD) players, the sensitive photo-diodes, their associated low-noise wideband RF data preamplifier and the low-offset focus and tracking error servo amplifiers should be implemented as a monolithic IC structure. Unfortunately, all attempts so far to achieve this high level of integration have resulted in a 5 dB reduction of the RF preamplifier signal-to-noise ratio and significant servo amplifier offset. This is caused largely by interaction between the photo diode AC coupling capacitors and the parasitic parallel capacitance at the input to the RF data preamplifier.

Philips have now overcome this problem, and minimized cost without compromising performance, by using an innovative architecture for their highly-integrated Photo-Detector/ Preamplifier (PDP) TSA9000T. This IC contains a four-quadrant main spot photo-detector which is optimized for λ = 780 nm and DC coupled to a wideband RF data preamplifier. The IC also includes two satellite spot detectors and six class-B (virtually offset-free) servo amplifiers for generating the focus and tracking error signals. For beam landing correction and gain compensation of the tracking error in a 3-spot pick-up, normalizing functions are incorporated in the focus error and tracking error signal processing part. Also included are dropout concealment of the normalizer circuit and test functions which simplify the mechanical and optical alignment of the system.

The TSA9000T is in a transparent 10-pin VSO package that can be surface-mounted, together with the three peripheral passive components required, directly onto the end of the flexible PCB wiring to the optical pick-up. Since a rigid PCB is no longer necessary, the weight and size of the pick-up sled is much reduced. Also, because the RF data stream is transferred at a reasonably high level from the PDP to the processing circuitry elsewhere in the player, it is less susceptible to corruption by radiated interference and shielding is not required.



Dimensions in µm of the photo diodes in the TSA9000T



The TSA9000T compared with a hybrid optical pick-up with integrated photo diodes, a discrete component RF data preamplifier and a normalizer IC

QUICK REFERENCE DATA

The TSA9000T can operate over an ambient temperature range of −30 °C to +85 °C. All the figures quoted are typical values, measured with a supply of +5 V (V_{dd}) and −5 V (V_{ss}), P_{CS} = 20 µW, I_{REF} = 50 µA.

Sensitivity

data detector-amp V_{RF}/P_{CS}: 30 mV/µW
(within 3 dB, DC coupled for f_{in} = 0 to 15 MHz)

central sum I_{CS}/P_{CS}: 5 µA/µW
(for f_{in} = 0 to 1 MHz)

track sum I_{TS}/P_{TS}: 10 µA/µW
(for f_{in} = 0 to 1 MHz)

Normalizer reference current

I_{NREF}: 50 µA

Summary of terms

CS: central sum output signal

FEN: normalized focus error output signal, diagonal direction four-quadrant photo detector

I_{CS}: output current from pin CS

I_{FEN}: output current from pin FEN

$$I_{FEN} = I_{NREF} \times \left(\frac{P1 - P2}{P1 + P2} + \frac{P4 - P3}{P4 + P3} \right)$$

I_{REF}: reference current

I_{TENa}: output current from pin TENa

$$I_{TENa} = I_{NREF} \times 2 \frac{P6}{P5 + P6}$$

I_{TENb}: output current from pin TENb

$$I_{TENb} = I_{NREF} \times 2 \frac{P5}{P5 + P6}$$

I_{TS}: output current from pin TS

P1 to P6: light power detected by photo diodes

P_{CS}: sum of the light power detected by photo diodes 1 to 4

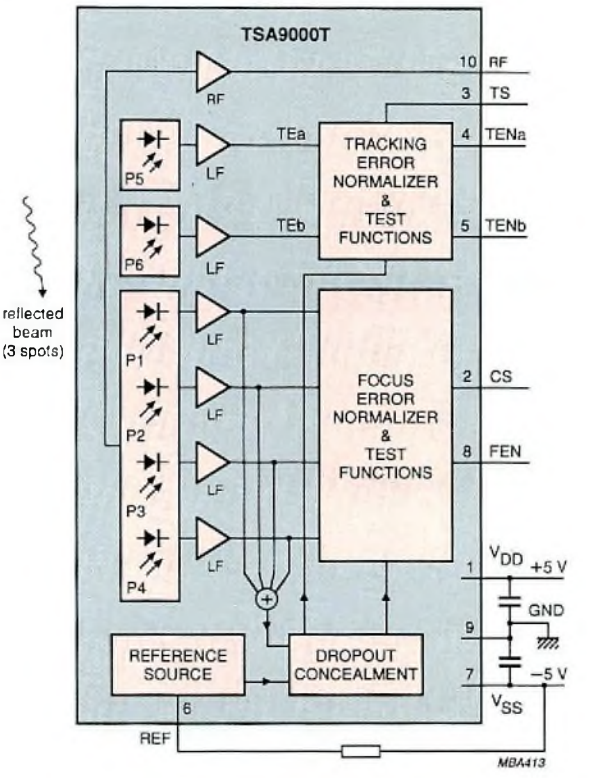
P_{TS}: sum of the light power detected by photo diodes 5 and 6

RF: data signal output

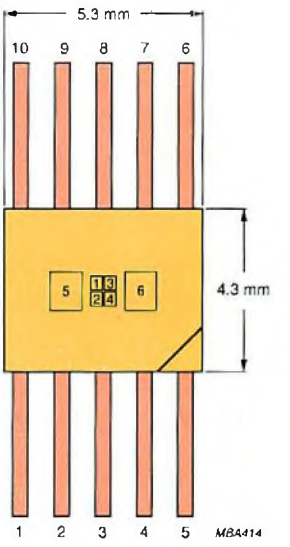
TENa: normalized tracking error output signal

TENb: normalized tracking error output signal

TS: track sum output signal



Block diagram of the TSA9000T



10-pin transparent VSO package of the TSA9000T

Advanced BiCMOS – the solution to bus interface logic

TINUS VAN DE WOUW

The new QUBiC process, recently developed by Philips Components, is a major step forward in processing technology. It's a no-compromise process, combining the best of Philips' superior CMOS and bipolar technologies. This process is the cornerstone of a new BiCMOS bus interface logic family – the ABT series (Advanced BiCMOS with TTL switching levels) which consists primarily of high-speed octal buffers, latches and transceivers.

The ABT series opens up exciting possibilities for new design. Its advantages include:

- the best switching properties of any standard interface family
- nearly twice as fast as current bipolar logic
- extremely low ground bounce
- excellent drive capabilities
- very low dissipation
- ease of drive.

The ABT interface range is simply the best available today for applications where high speed and a high output current are required.

QUBiC: THE NEW TECHNOLOGY

Whereas competitor BiCMOS processes are basically modifications of existing bipolar or CMOS processes, QUBiC is a a true blending of both technologies – a no-compromise process, with the complete integration of bipolar and micron CMOS presenting exciting possibilities in design.

In the QUBiC process, the following circuit elements can be made:

- N-channel MOS transistor
- P-channel MOS transistor
- NPN transistor
- lateral PNP transistor
- Schottky, standard and zener diodes
- fuses
- resistors.

The available elements allow CMOS, TTL and ECL signal levels all to be present on the same chip, providing new design options in mixed-signal environments.

The QUBiC process is not only suitable for ABT logic devices; its versatility and unique properties make it an ideal choice for advanced products such as PLDs, gate arrays, ASICs and memories, and for devices for FutureBus+ applications.

The 1 μm process generates extremely fast MOS transistors and provides a very high packing density. Large parts of each logic circuit are made in CMOS technology for low power consumption.

The very-narrow-base NPN transistor has a transistion frequency of 13 GHz – incredibly fast for an integrated transistor. It also has excellent drive capability, for driving highly capacitive loads.

The PNP transistor that can be made is relatively slow owing to its lateral fabrication, so wherever possible, the other circuit elements are used instead.

The QUBiC Schottky diodes allow bipolar devices comparable to those of other Schottky families to be made.

Together, these circuit elements give the ABT range superb characteristics combining the best of FAST* with the best of Advanced CMOS. However, because twenty-two process steps are required to manufacture ABT, we limited the number of ABT devices to those where the combination of speed and drive is really required – primarily in fast bus applications. Simple gates are not cost-effective to make using the QUBiC process.

CIRCUIT ELEMENT FABRICATION

Figure 1 is a cross-section through part of an ABT device showing the forementioned NMOS, PMOS, and NPN transistors.

Transistors

Owing to its very narrow base, the NPN transistor has a very high transition frequency of 13 GHz, which gives switching times of less than a nanosecond; competing processes have transition frequencies of less than 8 GHz. In addition, its current-handling is excellent, providing high output drive.

The NMOS and PMOS transistors have very narrow channel lengths, effectively 0.85 μm. This too yields sub-nanosecond switching times.

Together, the NPN transistor and the CMOS elements make ABT logic the fastest on the market.

Resistor

There are two ways of making a resistor, as can be seen in Fig.1 – with or without doped polysilicon – producing two values of resistivity with two temperature coefficients, one positive, one negative. This gives a wide choice in resistances and enables resistors to be made with zero temperature dependency.

* FAST is a trademark of Fairchild Instrument and Camera Corp.

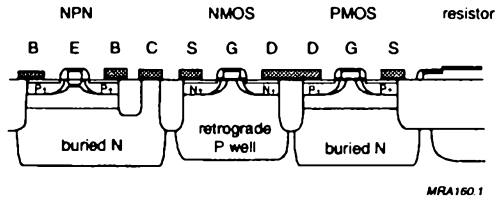


Fig.1 Cross-section through an ABT device showing the main elements that can be fabricated using the QuBiC process

Diode

Not shown in Fig.1 is a Schottky diode which is used, for example, to speed up the NPN transistor even further by minimizing hole storage.

BICMOS RANGE

Current range and future plans

The relatively large number of process steps makes QUBiC more suited to the fabrication of complex circuits than simple gates. And its high output drive capability and fast speed strongly favours fabrication of fast bus driver interface circuits. Therefore, it's unlikely that simpler circuits will be incorporated in the ABT range.

However, for other fast applications where speed is important and high output drive is not, Philips' ACL family (with centre pin supply) is available, offering high speed with low ground bounce and very low power dissipation. And a full range of SSI/MSI standard logic functions is available. Together, ACL and ABT provide an unequalled range of logic products.

A survey of ABT products that are released or due to be released in the near future is given in the Appendix. All of the circuits are basically ABT versions of existing products and have the same outline and pinning. For example, the 74ABT244 is functionally identical to the 74HCT244 or its FAST version the 74F244. The electrical performance, however, is significantly better.

To simplify designing with ABT products, the data sheets include graphs not usually featured in the data sheets of other logic families such as:

- AC specifications vs. V_{CC}, temperature, capacitive load and the number of outputs switching
- ground bounce and undershoot vs. temperature and capacitive load (all outputs switching)
- V_{CC} bounce and undershoot vs. temperature and capacitive load (all outputs switching)
- output current vs. voltage.

Technology comparison

The ABT family compares favourably with other logic families on speed, drive and power dissipation. As Table 1 illustrates, Philips ABT is the right choice for all logic applications requiring a high drive current and high speed. Furthermore, ACL complements the ABT range for all applications where drive is not a prime concern and for all simpler functions such as gates, Schmitt-triggers, flip-flops, multiplexers and counters.

TABLE 1
Comparison of various logic families
(the popular '245' function of octal transceiver is used for comparison)

	Philips' products			competitor products				unit
	ABT	FAST	ACL	BCT	FCTA	FACT	FCT	
ground bounce	**<1**	1	<1	<1	2-3	2	2.5	V
speed[1]	**0.7**	1	1	~1	0.7	1	~1	
output drive[2]	**64**	64	24	64	64	24	64	mA
I_{DD} static	**0 to 30**	100	0	~45	1.5	0	1.5	mA
P_D at 50 MHz[1]	**0.3**	1	0.5	0.6	0.6	0.5	0.6	mW
temperature range	**−40 to +85**	0 to 70	−40 to +85	0 to 70	0 to 70	−40 to +85	0 to 70	°C

[1] FAST is taken as reference: FAST=1;
T-versions of ACL products are about 20% slower than the standard versions.
Competitors' BCT enable and disable times are relatively slow.
[2] Higher output drive is not always better: due to higher internal capacitances, propagation delays tend to increase for higher output current devices.

BASIC TRI-STATE CELL

Here, we describe the design of the 'basic cell' generally used in all ABT tri-state bus driver circuits. The other parts of an ABT circuit are usually simpler, and can be easily described once the basic cell is understood.

Figure 2 is the circuit diagram showing the signal input (IN), the enable inputs (E and $\overline{E}$) and the output (OUT).

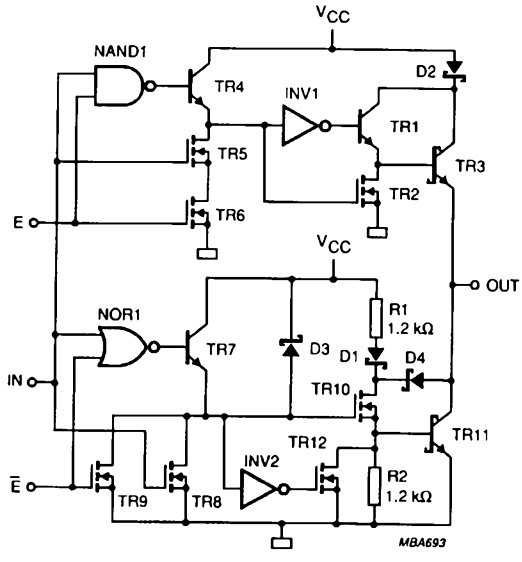


Fig.2 ABT basic cell

Basic inverter circuit

First look at the three elements INV1, TR1 and TR2. This trio functions as an inverter. The NMOS transistor TR2 functions as in normal CMOS, and INV1 consists of a small NMOS-PMOS pair again as in standard CMOS. Together, INV1 and the NPN transistor TR1 function as the PMOS transistor normally present in standard CMOS. The main advantage of this new configuration is that the size of the transistors in the inverter INV1 can be minimized, making the internal capacitances low. This minimizes internal losses because of the smaller charging/discharging currents. In addition, it reduces the propagation delay (which is already short due to the advanced QUBiC technology) further to about 0.2 ns.

A similar design (CMOS inverting element, NPN transistor and NMOS transistor) is recognizable around NAND1 and NOR1 which both function as optimized extremely-fast NAND and NOR gates.

Main signal flow

Suppose that the enable input E is HIGH (and $\overline{E}$ is LOW). A positive signal on the IN input follows a path via NAND1/TR4/TR5, INV1 to TR1 which drives the Schottky output transistor TR3. A LOW input signal goes via NOR1, TR7 and TR10, driving output Schottky transistor TR11. The required base drive for TR11 comes via the base resistor R1. Clearly, this base current is only required when the output is forced LOW; if the output is HIGH, no base current flows. This implies that using bipolar transistors incurs a slight penalty because a base current (of 2 to 3 mA per output) should be provided when outputs are pulled down.

Tri-state operation

When the enable input E is HIGH (and $\overline{E}$ is LOW) the signal flow is as described above. When the reverse is true, the LOW E input always keeps the output of NAND1 HIGH so that TR3 is always off. And the HIGH $\overline{E}$ input keeps TR10 and hence TR11 off.

The enable/disable input shuts down operation from the earliest point on, so that, even while an input signal is present, there is no internal dissipation.

Additional circuit characteristics

Besides the major elements of the basic cell, some other elements are also important.

Firstly, diode D4 provides a high base current when initially turning on TR11, effectively 'kicking on' TR11 while the output is still HIGH.

The combination of INV2 and TR12 ensures that the hole charge stored in TR11 is extracted quickly during turn-off, for a faster turn-off. This 'break-before-make' output push-pull circuit reduces power consumption during transitions and minimizes ground bounce.

Should V_{CC} become zero, diode D1 prevents current flowing from the output to ground, while D3 ensures that TR10 and hence TR11 are off.

Finally, diode D2 provides an extra voltage drop in the output to ensure a TTL-level output swing. And together with a series resistor (not-shown), it limits the source output current as well as preventing current flowing from the output load to V_{CC} during device power-down.

PROPERTIES OF THE NEW RANGE

Key electrical characteristics

The main electrical characteristics of a 74ABT245 are given in Table 2.

Dependence of speed on V_{CC} and temperature

The propagation delays depend on both V_{CC} and temperature, see Fig.3. The slight variation in delay at different V_{CC} is normal – as V_{CC} increases, the drive improves, lowering internal resistances which makes operation faster. The temperature stability of ABT devices is excellent – a by-product of the process technology, with the temperature dependences of the bipolar and CMOS transistors compensating each other.

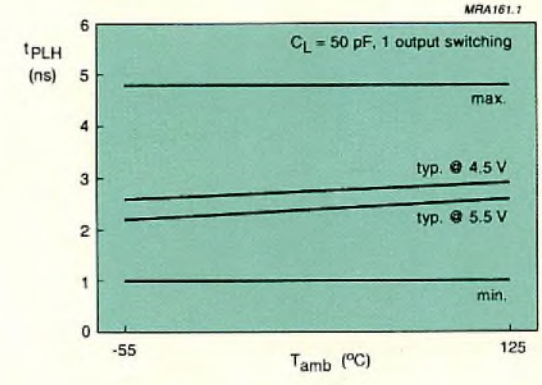


Fig.3 Propagation delay t_{PLH} as a function of temperature with V_{CC} as a parameter

Effect of load capacitance

Figure 4 shows how the propagation delay changes with the load. Obviously, for ABT bus driver ICs which can handle relatively high output currents, it makes sense to specify propagation delays at load capacitances higher than the standard 50 pF. Graphs such as Fig.4 are therefore included in the data sheet of every ABT product.

TABLE 2
Main electrical characteristics of a 74ABT245 octal transceiver

symbol	parameter	conditions (T_{amb} = 25 °C; GND = 0 V)	value
t_{PHL}/t_{PLH}	propagation delay	C_L = 50 pF; V_{CC} = 5 V, R_L = 500 Ω	typ. 2.9 ns
C_{DIR}	input capacitance	V_i = 0 V or V_{CC}	4 pF
$C_{I/O}$	I/O pin capacitance	V_i = 0 V or V_{CC}	7 pF
I_{CCH}	quiescent supply current	outputs HIGH; V_{CC} = 5.5 V; V_i = 0 V or V_{CC}	<50 µA
I_{CCL}	"	outputs LOW; V_{CC} = 5.5 V; V_i = 0 V or V_{CC}	<30 mA
I_{CCZ}	"	outputs 3-state; V_{CC} = 5.5 V; V_i = 0 V or V_{CC}	<50 µA
ΔI_{CC}	additional I_{CC} per input pin	outputs enabled, one V_i = 3.4 V; others are 0 V or 5 V	<1.5 mA

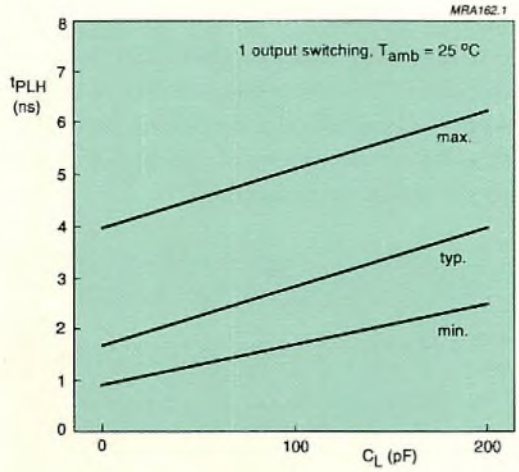


Fig.4 Propagation delay, t_{PLH}, as a function of load capacitance

Number of outputs switching

Usually, propagation delays are specified for only one output switching. However, when more outputs are switching simultaneously, the switching times tend to increase. This is due to the fast dI/dt generating a voltage in the ground wire which decreases the drive voltage for the devices inside the IC, thus slowing them down. This is valid in general for all digital circuits.

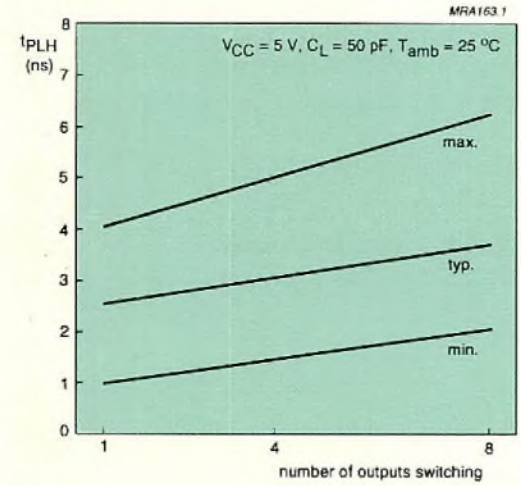


Fig.5 Propagation delay, t_{PLH}, as a function of the number of outputs switching simultaneously

Since the ground inductance also plays an important role in ground bounce (see next section), there is generally a good correlation between this effect and ground bounce.

All ABT data sheets contain graphs such as Fig.5 showing the effect of the number of outputs switching simultaneously on propagation delay.

Ground bounce

In today's fast switching environments, ground bounce would be a designer's nightmare, with the generated voltage spikes causing false triggering, introducing wait states or other effects all slowing down the system.

In the new ABT range, you don't have to worry about noise. Ground bounce is kept to a minimum in several ways. First, the output devices are bipolar transistors which have inherently better ground bounce performance than MOS transistors. The break-before-make output helps too. In addition, there is some slight output edge control, reducing the instantaneous current spike present during a transition, without any sacrifice in speed. Finally, the output voltage swing has been kept at TTL levels, reducing ground bounce even further. As a result, ABT circuits outperform all other logic families, see Fig.6.

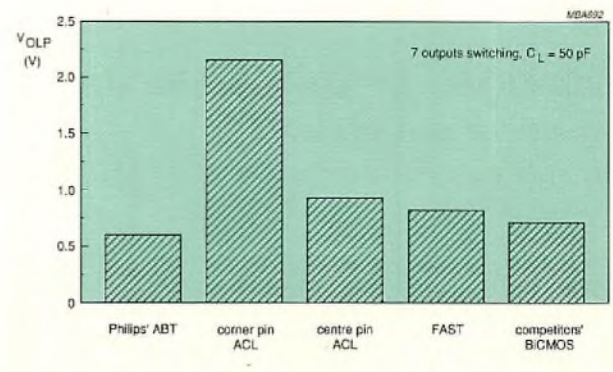


Fig.6 V_{OLP} (ground bounce) for several logic families

Centre supply-pinning as used for ACL was not necessary for ABT, but for future designs with higher current drive, faster speeds or more outputs (such as MULTIBYTE™), it increases performance further.

™ MULTIBYTE is a trademark of NAPC.

Supply current as a function of frequency

Figure 7 shows how I_{CC} varies with operating frequency for several logic families. At zero frequency, the supply current equals the specified I_{CCZ} (tri-state quiescent current). Then I_{CC} increases due to internal switching losses which are proportional to the frequency.

Advanced bipolar logic such as FAST has the biggest I_{CCZ}, which is significantly larger than that of the other logic families. Advanced CMOS (ACL) has the lowest I_{CCZ}, but I_{CC} increases more steeply than for the bipolar and BiCMOS families.

Below 20 MHz, ACL has the edge over the other families; above 20 MHz, Philips' ABT is the best logic family.

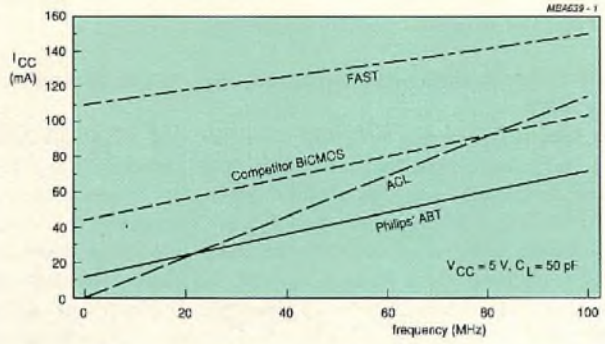


Fig.7 I_{CC} as a function of frequency for several logic families

APPENDIX

ABT product survey

type number 74ABT...	pins	description
125	14	quad buffer, 3-state
126	14	quad buffer, 3-state
240	20	octal buffer, inverting, 3-state
241	20	octal buffer, 3-state
244	20	octal buffer, 3-state
245	20	octal transceiver, 3-state
273	20	octal D flip-flop, asynchronous reset
373	20	octal latch, 3-state
374	20	octal D flip-flop, 3-state
377	20	octal D flip-flop, enable
534	20	octal D flip-flop, inverting, 3-state
540	20	octal buffer, inverting, 3-state
541	20	octal buffer, 3-state
543	24	octal latched transceiver, 3-state
544	24	octal latched transceiver, inverting, 3-state
573	20	octal latch, 3-state
574	20	octal D flip-flop, 3-state
620	20	octal transceiver, inverting, 3-state
623	20	octal transceiver, 3-state
640	20	octal transceiver, inverting, 3-state
646	24	octal registered transceiver, 3-state
648	24	octal registered transceiver, inverting, 3-state
651	24	octal registered transceiver, inverting, 3-state
652	24	octal registered transceiver, 3-state
657	24	octal transceiver, 8-bit parity, 3-state
821	24	10-bit D flip-flop, 3-state
823	24	9-bit D flip-flop, 3-state
827	24	10-bit buffer, 3-state
833	24	octal transceiver, 9-bit parity, error flip-flop, 3-state
834	24	octal transceiver, 9-bit parity, error flip-flop, inverting, 3-state
841	24	10-bit latch, 3-state
843	24	9-bit latch, 3-state
845	24	octal latch, 3-state
853	24	octal transceiver, 9-bit parity, error latch, 3-state
854	24	octal transceiver, 9-bit parity, error latch, inverting, 3-state
861	24	10 bit transceiver, 3-state
863	24	9-bit transceiver, 3-state
2952	24	octal registered transceiver, 3-state
2953	24	octal registered transceiver, inverting, 3-state

all types are available in DIP and SO packages

Abstracts

Picture quality improvements in bus-controlled TV receivers
The article gives an overview of Philips' latest IC developments for adding an Improved Picture Quality (IPQ) module to a TV set to introduce memory-based improvements such as adaptive line flicker reduction, noise/cross-colour reduction and zoom. The article also describes two bus-controlled receiver architectures and three IPQ modules (economy, extended and full options).

A frame grabbing application using the SCC66470 and SCC68070
With a system based on the Philips 68070 (CPU) and the SCC66470 (VSC), it is easy to digitize video images or grab natural images. Frame grabbing is the procedure of digitizing a picture from a video source and storing it in the system/video memory of the Video and System Controller (VSC). This feature of the VSC can be used in applications like desk-top publishing, remote surveillance, machina vision and digitizing TV, VCR or Video Disk pictures.

Colour monitor tubes with ARAS coatings
Philips colour monitor tubes are available with an advanced anti-reflection/antistatic (ARAS) screen coating that provides maximum operator comfort and excellent visibility in even the harshest ambient light conditions. One of the most effective screen treatments currently available, ARAS comprises a multilayer structure of transparent dielectric material that suppresses specular reflections by broadband interference at the screen surface. The antistatic properties come from a single conductive layer within the multilayer structure. With ARAS, the intensity of reflected light is reduced to less than 0.5% of the incident light. ARAS also doesn't diffuse or scatter the reflected light, so picture contrast and sharpness remain completely unimpaired.

Advanced BiCMOS – the solution to bus interface logic
As processor cycle times continue to decrease, designers need the fastest bus interface logic products available. Philips' new advanced BiCMOS family has the best switching properties of any standard family today. It's fabricated using Philips' 1 µm QUBiC process, which combines the best of FAST with the best of advanced CMOS. QUBiC is suitable for fabricating logic devices and circuits for Futurebus+ applications, PLDs, gate arrays and memories. The new BiCMOS products have extremely low ground bounce, excellent RFI performance and 64 mA output drive.

Verbesserung der Bildqualität bei bus-gesteuerten Fernsehgeräten
Dieser Artikel enthält eine Übersicht über die neuesten Entwicklungen von ICs bei Philips zur Erweiterung eines Fernsehgeräts mit einem Modul zur Verbesserung der Bildqualität (sogenanntes IPQ-Modul von Improved Picture Quality). Mit einem solchen Modul lassen sich speichergestützte Verbesserungen, wie z.B. adaptive Verringerung des Zeilenflimmerns, Herabsetzung der Rausch- und Cross-Colour-Störungen sowie Zoomfunktionen, durchführen. In diesem Beitrag werden ferner zwei busgesteuerte Empfängerarchitekturen und drei IPQ-Module (eine Spar-, eine erweiterte und eine voll ausgebaute Version) beschrieben.

Eine Frame-Grabbing-Anwendung mit dem SCC66470 und dem SCC68070
Mit Hilfe eines auf dem SCC68070 (CPU) und dem SCC66470 (VSC) von Philips basierenden Systems lassen sich auf einfache Weise Videobilder digitalisieren oder Originalbilder abtasten. Mit "Frame Grabbing" wird die Digitalisierung eines Bildes einer Videoquelle und dessen Speicherung im System-/Bildspeicher des Video- und System-Controllers (VSC) bezeichnet. Diese Funktion des VSC läßt sich bei Anwendungen wie Desktop Publishing, Fernüberwachung, optische Maschinensteuerung und Digitalisierung von Fernseh-, Video- oder Bildplattenbildern einsetzen.

Bildröhren für Farbmonitore mit ARAS-Beschichtung
Die Philips Bildröhren für Farbmonitore sind mit einer wirkungsvoll entspiegelnden, antistatischen (ARAS) Bildröhrenbeschichtung versehen, die ausgezeichnete Sicht, auch bei extrem ungünstigem Umgebungslicht ermöglicht und damit ein Maximum an Komfort für den Benutzer ergibt. ARAS, zur Zeit eine der wirkungsvollsten Bildschirmbeschichtungen, besteht aus einer mehrschichtigen Struktur transparenten dielektrischen Materials, das mit Hilfe von Breitbandinterferenz Reflexionen an der Bildschirmoberfläche verhindert. Die antistatischen Eigenschaften ergeben sich aus einer einzelnen leitenden Schicht innerhalb der Mehrschichtstruktur. Durch ARAS wird die Intensität reflektierten Lichts unter 0,5 % des auffallenden Lichts reduziert. ARAS verursacht keine Diffusion oder Streuung des reflektierten Lichts, wodurch Kontrast und Bildschärfe vollkommen unbeeinträchtigt bleiben.

Hochentwickelter BiCMOS-Prozeß - die Lösung für Bus-Interface-Logik
Da die Zykluszeiten bei Prozessoren immer weiter reduziert werden, benötigen Entwickler stets die schnellsten der auf dem Markt verfügbaren Logikbausteine für Bus-Schnittstellen, die zur Verfügung stehen. Die neue Advanced BiCMOS-Familie von Philips weist gegenüber allen anderen derzeit erhältlichen Standardserien die besten Schalteigenschaften auf. Sie wird mit dem 1 µm-QUBiC-Prozeß von Philips gefertigt, der die Vorteile von FAST und Advanced CMOS miteinander verbindet. QUBiC eignet sich für die Herstellung von Logikbausteinen und Schaltungen für Futurebus+-Anwendungen, PLDs, Gate-Arrays und Speicherbausteinen. Die neuen BiCMOS-Produkte zeichnen sich durch extrem niedriges NF-Rauschen, hervorragenden Hochfrequenzstörabstand sowie einen Treiber-Ausgangsstrom von 64 mA aus.

Amélioration de la qualité des images sur les récepteurs de télévision à pilotage par bus
L'article donne un aperçu des derniers développements sur le plan des circuits intégrés, permettant d'adjoindre un module IPQ (rehaussant la qualité des images) à un téléviseur, dans le but d'apporter des améliorations sur base de mémoire, comme par exemple la réduction du papillotement de ligne adaptatif, la réduction du bruit et des influences mutuelles des couleurs, ainsi que celle des effets de zoom. On y décrit également deux architectures de récepteur à pilotage par bus et trois modules IPQ (économique, étendu et toutes options).

Application Frame Grabbing (saisie d'image) à l'aide des SCC66470 et SCC68070
Avec un système basé sur les 68070 (processeur central) et SCC66470 (contrôleur vidéo et système) de Philips, on peut aisément numériser des images vidéo ou saisir des images naturelles. La saisie des images est une procédure consistant à numériser une image à partir d'une source vidéo et à l'emmagasiner dans la mémoire système/vidéo du Contrôleur Vidéo et Système. Les propriétés de ce dernier peuvent être mises à profit dans des applications telles que la micro-édition, la télé-surveillance, la vision 'machine' et la numérisation d'images de télévision, de magnétoscopes à cassettes ou de vidéo-disques.

Tubes-images couleurs avec revêtements ARAS
Les tubes pour moniteurs couleurs Philips sont disponibles avec un revêtement d'écran ARAS (advanced antireflection/antistatic = antireflet et antistatique évolué) procurant un maximum de confort aux opérateurs et une excellente visibilité, même dans les pires conditions d'éclairage ambiant. Le traitement ARAS, l'un des plus efficaces actuellement disponibles pour les écrans, comprend une structure multicouches de matériau diélectrique transparent qui supprime les reflets spéculaires dues à des interférences en bande large sur la surface de l'écran. Les propriétés antistatiques proviennent d'une couche conductrice unique au sein de la structure multicouches. Avec ARAS, l'intensité de la lumière réfléchie est ramenée à moins de 0,5 % de la lumière incidente. De surcroît, ARAS ne diffuse ni disperse la lumière réfléchie, de sorte que le contraste et la netteté de l'image restent absolument intacts.

BiCMOS évolué - la solution en matière de logique d'interface de bus
Les temps de cycle des processeurs diminuent sans cesse. De ce fait, les concepteurs ont besoin des produits de logiques d'interface de bus les plus rapides qui soient. La nouvelle famille de BiCMOS évolués de Philips possède les meilleures propriétés de commutation parmi tous les ensembles standard actuels. La fabrication a lieu à l'aide du processus QUBiC 1 µm de Philips, réunissant les plus grands avantages de FAST et ceux des CMOS évolués. Le processus QUBiC convient pour la fabrication de circuits et dispositifs logiques destinés aux applications Futurebus+, PLD, circuits prédiffusés et mémoires. Les nouveaux produits BiCMOS présentent des rebonds de terre extrêmement faibles, d'excellentes performances en matière de lutte contre les parasites RF et une unité de sortie 64 Ma.

Mejoras de calidad de imagen en televisores controlados por Bus
Este artículo ofrece una panorámica de los últimos desarrollos de circuitos integrados Philips para incorporar un módulo de mejoramiento de calidad de imagen (IPQ) en los televisores, con el fin de lograr mejoras basadas en memoria, tales como la reducción adaptativa de parpadeo de línea, reducción de ruido e interferencia en el color y zoom. El artículo también describe dos arquitecturas de receptor controladas por bus y tres módulos IPQ (económica, ampliada y completa).

Aplicación para la fijación de imagen utilizando en SCC66470 y el SCC68070
Con un sistema basado en la unidad central de proceso (CPU) 6870 Philips y el SCC66470 (VSC), es fácil digitalizar imágenes de vídeo o fijar imágenes naturales. La fijación de imagen es un procedimiento para digitalizar una imagen de una fuente de vídeo almacenándola en la memoria de vídeo/sistema del controlador de vídeo y sistema (VSC). Esta función del VSC puede ser utilizada en aplicaciones tales como autoedición, inspección remota, máquina-visión y digitalización de imágenes de TV vídeo y videodisco.

Tubos en color para monitores con recubrimientos ARAS
Los tubos en color Philips para monitores se sirven con un recubrimiento de pantalla antirreflectante y antiestático avanzado (ARAS), que ofrece la máxima comodidad al operador y una excelente visibilidad incluso en las más adversas condiciones de luz ambiental. ARAS, uno de los tratamientos más efectivos de pantallas actualmente disponibles, incluye una estructura de capas múltiples de un material dieléctrico transparente, que elimina reflejos por interferencia de banda ancha sobre la superficie de la pantalla. Las propiedades antiestáticas las ofrece una sola capa conductora dentro de la estructura de capas múltiples. Con ARAS, la intensidad de la luz reflejada se reduce a menos del 0,5 % de la luz incidente. ARAS tampoco difunde o dispersa la luz reflejada, por lo que el contraste y la nitidez de la imagen no se ven afectadas lo más mínimo.

BiCMOS avanzado - La solución para los circuitos lógicos de interfaz de "bus"
En vista de que los tiempos de los ciclos de los procesadores siguen reduciéndose, los diseñadores necesitan los circuitos lógicos de interfaz de bus más rápidos existentes en el mercado. La nueva gama BiCMOS avanzada de Philips presenta las mejores propiedades de conmutación de cualquier generación estándar hoy por hoy. Se fabrica utilizando el proceso de 1µm QUBiC de Philips, que combina lo mejor de FAST con lo mejor de CMOS avanzada. QUBIC es apropiada para la fabricación de dispositivos y circuitos lógicos para aplicaciones de Futurebus+, Dispositivos Lógicos Programables (PLDs), matrices de compuertas y memorias. Los nuevos productos BiCMOS tienen un nivel de tierra sumamente estable, un funcionamiento excelente en RFI y una corriente de salida de 64 mA.

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