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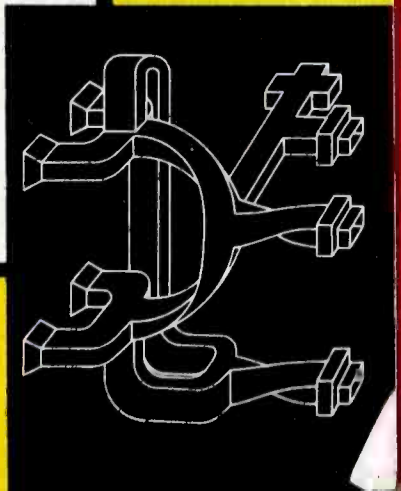
IN THIS ISSUE...



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Editorial

by John E. Remich
Manager, Technical Department

SINGLE SIDEBAND COMMUNICATIONS

The Air Force Strategic Air Command has for some time been using single sideband techniques for radio communications, and the recent announcement by the Navy that it has adopted single sideband and plans to convert to this mode of communication merely highlights the tremendous efforts which are being put forth to alleviate the over-crowding of the radio-frequency spectrum and to achieve the ultimate in reliable transfer of information.

The adoption of single sideband by the Air Force and the Navy is the result of carefully planned and executed evaluation programs, each encompassing features designed to evaluate the equipment in the light of requirements peculiar to the particular service. The Navy program, in which a team of Philco Tech-Rep Field Engineers played an important role, lasted for more than a year. During this time, many circuits and components were tested under severe environmental conditions.

The end result of these programs has been the development of circuits, components, and equipments which will become commonplace in the near future. Features of the equipments now in limited use and soon to be completely integrated into the Armed Forces include: a frequency stability of better than one part in 10 million (this means a drift of less than 10 cycles at a frequency of 100 megacycles), transfer of information at 400 words per minute or more, almost complete suppression of undesired signals, and reliable operation between —90 degrees and +125 degrees at values of relative humidity as high as 95%.

Although adoption of the single sideband techniques and equipments does not mean that all other equipments immediately become obsolete, it does point the way to a change. Many field engineers have already encountered single sideband equipments, and it is expected that many more will encounter such sets in the near future. To all communications engineers who are not familiar with SSB — now is the time to prepare for the future.

WANTED — BULLETIN CONTRIBUTORS

Since its inception in 1951, the Philco TechRep Division BULLETIN has been serving Philco TechRep Field Engineers and many others as a printed medium for the exchange of technical information. A steady flow of material, however, is necessary for the BULLETIN'S existence. The purpose of this brief discussion is to invite greater participation in the BULLETIN.

Although there is no hard and fast classification for BULLETIN articles, they may usually be divided into three broad categories. The first category includes articles devoted to an explanation of the theory underlying a device, equipment, component, or circuit. An excellent example of this type is the "Theory of Monopulse Radar," by Harry L. Martin, which appears in this issue. Included also in this category are articles of general interest, such as the articles on the earth satellites which appeared late last year.

The second broad category includes articles devoted to electronic tests, test equipment, and simulation equipment which are general in nature and applicable to many equipments. This category includes such articles as "Sun-Strobe Techniques," by Bud M. Compton, which was presented in the previous issue.

The third category includes articles devoted to a specific equipment, such as "Dependable Operation of the A-F-C Circuits in the FPS-3," by Fred F. Thomas.

These are only a few of the many excellent articles which have appeared in the BULLETIN. You no doubt know many interesting topics and devices which need only to be written about. We'd like to hear about them in BULLETIN articles. In this way, new techniques and new "how-to" information can be made available to a large number of people who would benefit.

Here are a few hints in preparing manuscripts. First, the manuscript should be typed, if possible, with double spacing between the lines, and the pages numbered. As insurance against possible loss, it is advisable to retain at least one carbon copy. Second, schematics, drawings, and other art work should be prepared on separate pages, with each figure numbered and "called out" in the text of the article. It is desirable to use photographs, wherever applicable, and these should preferably be in the form of glossy prints. Third, the first page should include the author's name, exactly as it should appear in print. This hint may seem unnecessary, but it is surprising how many manuscripts do not include the author's name, except as the signature on the covering letter.

Literary style and polished grammar are not necessary — the technical content is. The editors will make the necessary changes to ensure that the final copy is readable and conforms to the BULLETIN style. Manuscripts should be mailed to the address which appears on the reverse side of the BULLETIN front cover.

If your article is accepted and printed, you will gain the prestige and recognition accruing to an author of technical material. As an added incentive, you will receive a gratuity for each accepted article of 500 words or more.

One final note — contributions are not restricted to Philco TechRep Division personnel. This discussion applies to any and all who read the BULLETIN or are interested in writing for it. Keep your material coming in.

The Editors

THEORY OF MONOPULSE RADAR

By Harry L. Martin
Philco TechRep Field Engineer

The high accuracy and high-speed response required of tracking radars by the introduction of high-speed aircraft and missiles have resulted in the development of monopulse radar. This article discusses the principles of monopulse radar and explains the theory of the r-f section used with it.

WITH THE DEVELOPMENT of extremely high-speed aircraft and even faster missiles, it has been necessary to increase the accuracy and response of tracking radars to furnish exact information to anti-aircraft and anti-missile batteries. One new type of system employs an r-f section called *monopulse* and a three-channel receiver. This system derives target information from each returned signal, instead of using several pulses as is necessary in lobing-type radars.

The r-f system, shown in figure 1, is a complex arrangement of hybrid junctions[1] terminated by four feedhorns as the antennas. During transmission, the magnetron energy enters the E arm of T1 and divides into the collinear arms, the two signals being equal in amplitude and 180 degrees out of phase. No energy leaves the H arm. The signals from T1 enter T2 and T3, in the H arms, in phase because of reverse 90-degree twists in each arm. The signals in each of these junctions divide equally, in phase, and pass through the forked collinear arms into the four feedhorns. Energy does not pass to T4

[1] For hybrid junction review, refer to the BULLETIN, Volume 5, No. 5.

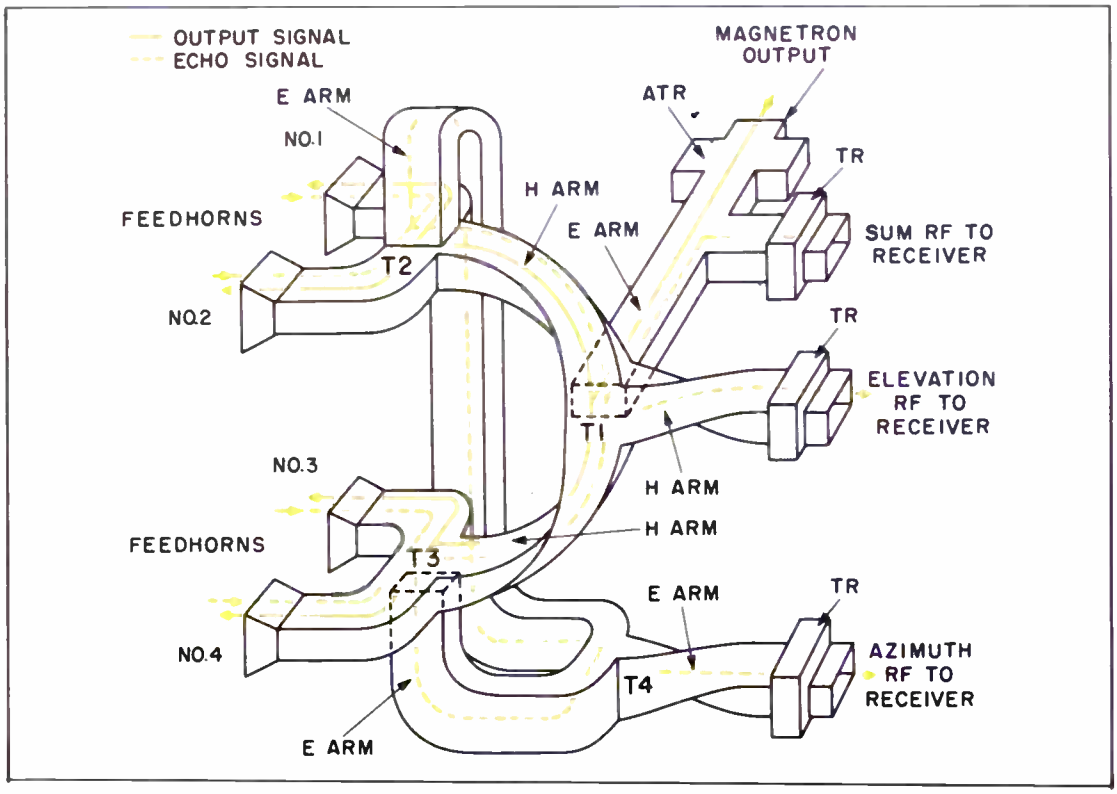


Figure 1. R-F System of a Monopulse Radar

because of cancellation at the E arms of T2 and T3. Therefore, the magnetron signals leaving the feedhorns are in phase and of equal amplitude, and they combine to form a single transmitted wavefront. This transmitted signal is focused into a narrow, pencil-type beam by a lens assembly[2] for greater accuracy.

The returned echo signal is focused into the four feedhorns by the lens assembly. The focusing action of the lens plays an important part in the determination of pointing error. If the antenna is pointed directly at the target, the signal is focused so that in-phase signals of equal amplitude are introduced into the feedhorns. These signals enter the collinear arms of T2 and T3 and add in the H arms of each. There is no output to T4 because of cancellation at the E arms of T2 and T3. The signals leaving the H arms of T2 and T3 pass through the 90-degree twists to T1, where they enter the collinear arms 180 degrees out of phase, and equal in amplitude. These signals cancel at the H arm and add at the E arm. The resultant signal is channeled into the receiver by ATR tube action, and is called the *sum rf* because it is proportional to the sum of the energy in all four feedhorns. This signal is produced whenever an echo signal is received even if there is a pointing error at the antenna. It is used for automatic ranging and as a reference to determine the pointing error.

Because of the focusing action of the lens, if the antenna is pointed below the target, the echo signal is strongest in the upper feedhorns (No. 1 and No. 2); if pointed above, it is the strongest in the lower feedhorns (No. 3 and No. 4); if pointed to the right, it is strongest in the feedhorns on the right (No. 2 and No. 4); if pointed to the left, it is strongest in the feedhorns on the left (No. 1 and No. 3). If the antenna is pointed above and to the right of the target at exactly 45 degrees, as illustrated in figure 2, feedhorn No. 4 receives the strongest signal, feedhorns No. 2 and No. 3 receive medium-strength, equal-amplitude signals, and feedhorn No. 1 receives the weakest signal.

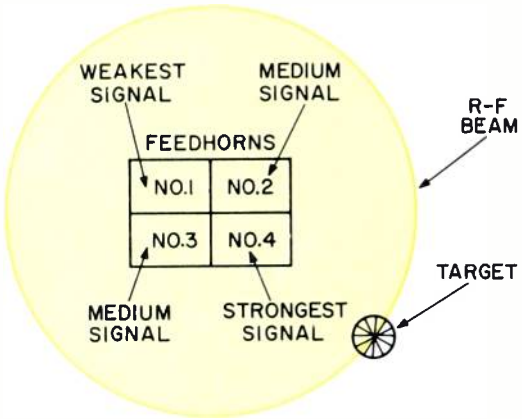


Figure 2. Illustration of Received-Signal Levels with Antenna Pointing Above and to the Right of the Target (Shown Looking Into the Feedhorns)

Signals entering the collinear arms of T2 are in phase but of unequal amplitude. These signals add at the H arm and pass on to T1. They subtract at the E arm of T2, and the difference passes on to T4, the phase being that of the signal in feedhorn No. 1, the strongest signal. At the same time, there are two signals of unequal strength in the collinear arms of T3. At the H arm these signals add and pass on to T1. They subtract at the E arm, and the difference passes on to T4, the phase being that of the signal in feedhorn No. 3. At T4 the two signals enter the collinear arms 180 degrees out of phase and add at the E arm, and the resultant passes on to the receiver as azimuth rf. How this signal is used will be discussed later. The signals leaving the H arms of T2 and T3 enter the collinear arms of T1 180 degrees out of phase because of the 90-degree twists. The output signal

[2] For lens assembly explanation, see Philco Training Manual on Antennas, Volume 1, page 178.

from T2 is larger than the output signal from T3. These two signals add at the E arm, and the resultant is sent out as the sum rf. The signals subtract at the H arm, and the difference is sent to the receiver as the elevation rf, the phase being that of the strongest signal.

Note that, in the output of the r-f system, the azimuth rf, and the sum rf are 180 degrees out of phase, as also are the elevation rf and sum rf, whenever the pointing error is to the right or above. If the pointing error is to the left or below, the error signals are in phase with the sum rf. These phase relationships are important in the receiver determination of pointing error.

A simple arithmetic analysis of the feedhorn signal comparison may be given as:

$$\text{Sum rf} = (1 + 2) + (3 + 4)$$
$$\text{Az rf} = (1 - 2) + (3 - 4)$$
$$\text{El rf} = (1 + 2) - (3 + 4)$$

Figure 3 is a block diagram of the three-channel receiver used with a monopulse r-f system. Each r-f signal is sent to a balanced converter, mixed with the local-oscillator signal, and converted to an i-f signal. The i-f signal is then amplified and sent through an i-f phase shift compensator. The output of the sum channel is sent to the range system for automatic ranging and is also sent to the angle error detectors for use as a reference signal. The angle error detectors compare the phase and amplitude differences of the error i-f signals and the sum if. If they are in phase, the output is a negative video pulse, indicating a pointing error to the left or below. If they are 180 degrees out of phase, the output is a positive pulse, indicating a pointing error to the right or above.

The amplitude of the output pulses depends upon the amplitude difference between the sum and the error signals, and indicates the amount of pointing error. These outputs are rectified and sent to a servo system to position the antenna on target.

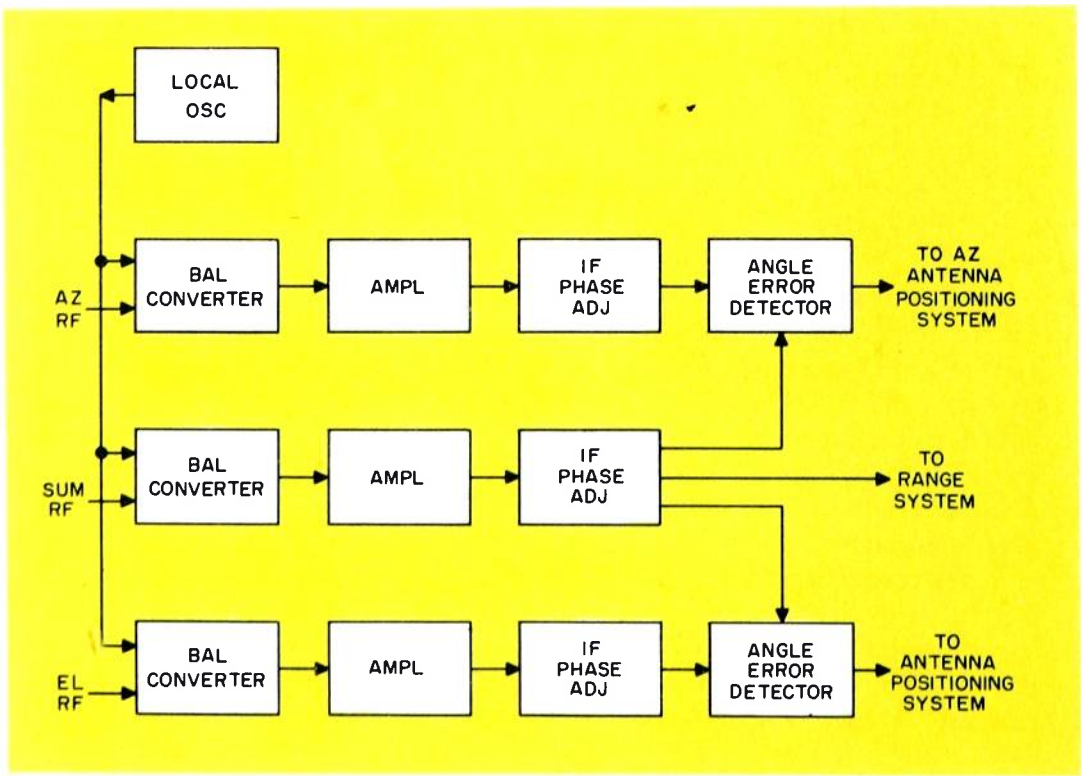


Figure 3. Block Diagram of Three-Channel Monopulse Receiver

Because the entire operation depends upon phase relationships, it is necessary to make corrections for r-f attenuation, r-f phase shift, and i-f attenuation. R-F attenuation is corrected by a lateral adjustment of the feedhorn assembly. The system is locked on a fixed target by line of sight, and then it is electrically zeroed in by the lateral adjustment. R-F phase shift is compensated for by design. When the antenna is directly on target, if there is an output in the error channel because of r-f phase shift, this output will be 90 degrees out of phase with the sum signal. Therefore, cancellation will occur in the angle error detectors, because they are designed to give zero output if the two inputs are 90 degrees out of phase.

I-F phase shift is corrected in the receiver by manually adjusting the i-f phase adjust control to obtain the same amount of phase shift in each channel. This insures that the phase relationships of the signals entering the angle error detectors are the same as they were when the signals left the r-f system.

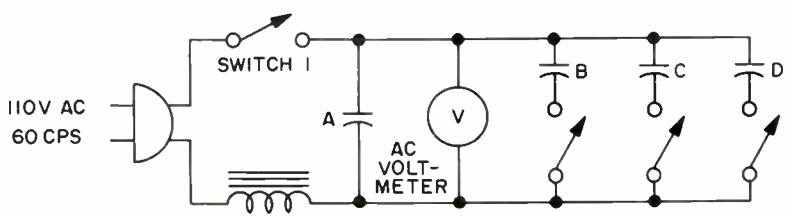
A major advantage of this system is the rapid a-g-c response. Since there is no lobing on the part of the antenna, the agc is not limited to a response of approximately one-tenth the lobing rate. Instead, it is limited to one-tenth the prf, which is a much higher rate, and therefore has a much faster response, making the receiver much more sensitive.

The monopulse type radar, therefore, is able to furnish target position information with greater speed and accuracy than earlier types of radar because it derives target information from each returned echo pulse, and because it contains a receiver with much greater sensitivity and response.

"What's Your Answer?"

We are indebted to Philco TechRep Field Engineer Gabe Rumble for the problem below.

An instructor constructed a breadboard to demonstrate the simple phenomenon of series resonance. He selected an inductor of unknown value out of a group, placed a capacitor (A) in series with it, and connected the series combination to a wall outlet. As a resonance indicator, he connected an a-c voltmeter across the capacitor. Since he did not have enough capacitance at A to reach resonance, he kept adding capacitance at B, C, and D until the reading on the meter (in the actual case, over 1200 volts) indicated a close approach to resonance. Then leaving B, C, and D connected, he opened switch 1, allowing any residual charges on the capacitors to leak off through the meter. At the demonstration, he closed switch 1 and was surprised to find only 200 volts or so on the meter, not the 1200 volts he expected. No component had been damaged. What's going on here?



A TEST SET FOR SYNCHRO ALIGNMENT

By William G. Howard
John G. Porter
Averill M. Whitlatch, Jr.
Philco TechRep Field Engineers

The test set described in this article was designed and constructed to fill the definite need for simplification of alignment procedures for synchros and servomechanisms and to shorten the time required for this alignment.

THERE ARE THREE MAJOR problems associated with the maintenance of systems involving synchros and servomechanisms — the excessive time required for alignment, the danger of severe electrical shock, and the provision of a voltage source having sufficient current capacity to allow proper alignment of the synchros and servomechanisms found in data converters and computers. The test set described below was constructed with the primary object of overcoming these problems. This instrument is very compact, inexpensive to construct, and extremely simple to use.

The test set eliminates the need for connecting short pieces of wire across the various terminals to provide the necessary test conditions. Also, the shock hazard resulting from reaching in confined spaces and near exposed terminals is minimized by the use of insulated clips on the test leads.

Replacement or repair of signal data converters and fire control computers usually necessitates practically a complete disassembly of the equipment, and involves complete re-zeroing of the numerous synchros upon reassembly of the gear train mechanisms. The time required for the re-zeroing process can be decreased by almost three fourths by the use of this test set. There are two versions of this set, shown in figures 1 and 2. The "Ideal" model, shown in figure 1, utilizes a 5-ampere Variac as the voltage source. The "Utility" model, shown in figure 2, is a less expensive version which is the same as the Ideal model except that 100-ohm, 50-watt resistors connected in parallel combinations are used in place of the Variac to supply the proper voltages. The resistance combination offers the advantage that the input power source can be at any frequency for which the item under test is designed. In order to attain this same advantage in the Ideal model, it is necessary to use a 50—1000 cycle Variac. Schematic diagrams

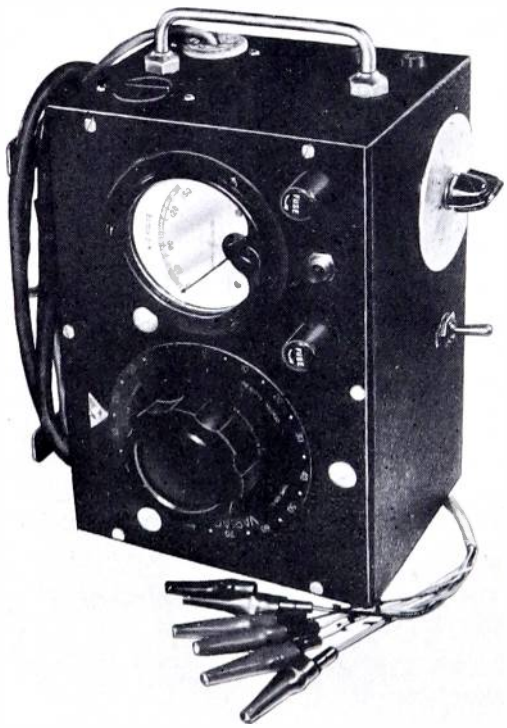


Figure 1. Ideal Synchro Test Set

for the two models are given in figures 3 and 4.

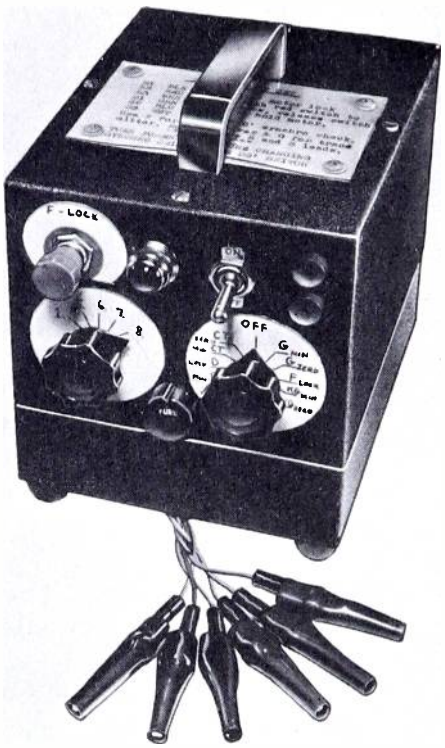


Figure 2. Utility Synchro Test Set

As can be seen from either figure 3 or figure 4, the 9-pole, 11-position rotary switch (S4) provides the correct interconnections for the 10 types of checks normally used. It switches the alignment voltages to the proper leads of the synchro, and connects the meter pin-jacks to the proper position for measurement of the output voltage of the synchro. In the "motor lock," "generator minimum," and "generator zero" positions, of the switch, motor excitation comes from the line to increase the versatility of the instrument by allowing the technician to check size 8 synchros, which draw more current than is available from the 5-ampere Variac. This method is acceptable in accordance with Ordnance Pamphlet 1303, *U. S. Navy Synchros.* The push-to-lock switch (S2) is used with the Utility model to eliminate phase shift and consequent loss of torque and the possibility that motors and differential motors may lock 180 degrees out of phase.

The sequence of positions of S4 is arranged to reduce operating time and resultant wear on the unit. This is accomplished by locating the most-used positions adjacent to the center "off" position. The minimum usage, or check, positions are located before the zero position, to further reduce the operating time required by eliminating the possibility of a 180-degree error.

KG and KCT type synchros are checked by adjusting the Variac output to 20 or 30 volts, a.c., to compensate for the design characteristics in these units.

Zeroing 400-cycle synchros with the Ideal model, it is necessary to reduce the 60-cycle excitation to approximately one-fourth that of the 400-cycle value, in order to compensate for the lack of iron in the rotor and field poles. Since there are no frequency-sensitive components in the Utility model, no compensation for frequency is necessary when this model is used if the source voltage frequency is the same as that for which the synchro is designed.

The use of potentiometers and rheostats is not feasible because of the prohibitive wattages required when current is high and only a small part of the potentiometer is used. Inadvertent burnouts will occur under these conditions.

A DPDT switch, S5 (not shown in figure 2), removes R2 from the circuit and inserts a 1000-ohm, 50-watt variable resistor in its place. Two pin-jacks are added for connecting a meter into the circuit to measure the excitation voltage. This circuit in the Utility model is used for the checking of all currently used 3-phase devices for position control. I-C type synchros or autosyns can be checked and zeroed by the reversal of the "R" and "S" leads on the test set, as these devices have three rotor leads and two or three stator leads according to the type used.

In the Utility model, the one-pole, five-position rotary switch (S3) and the 100-ohm, 50-watt resistors (R4 through R11) are used in conjunction with the differential generator "minimum," "zero," and "differential motor lock" positions to provide the proper voltage drops, since both the rotors and stators are rated for 78 to 90 volts ac in these units. These resistors and switches can be eliminated for an even more economical model, but caution must be observed, because the 155-volt, a-c power on these units will cause over-heating in a short time. This change is shown on the schematic in figure 5.

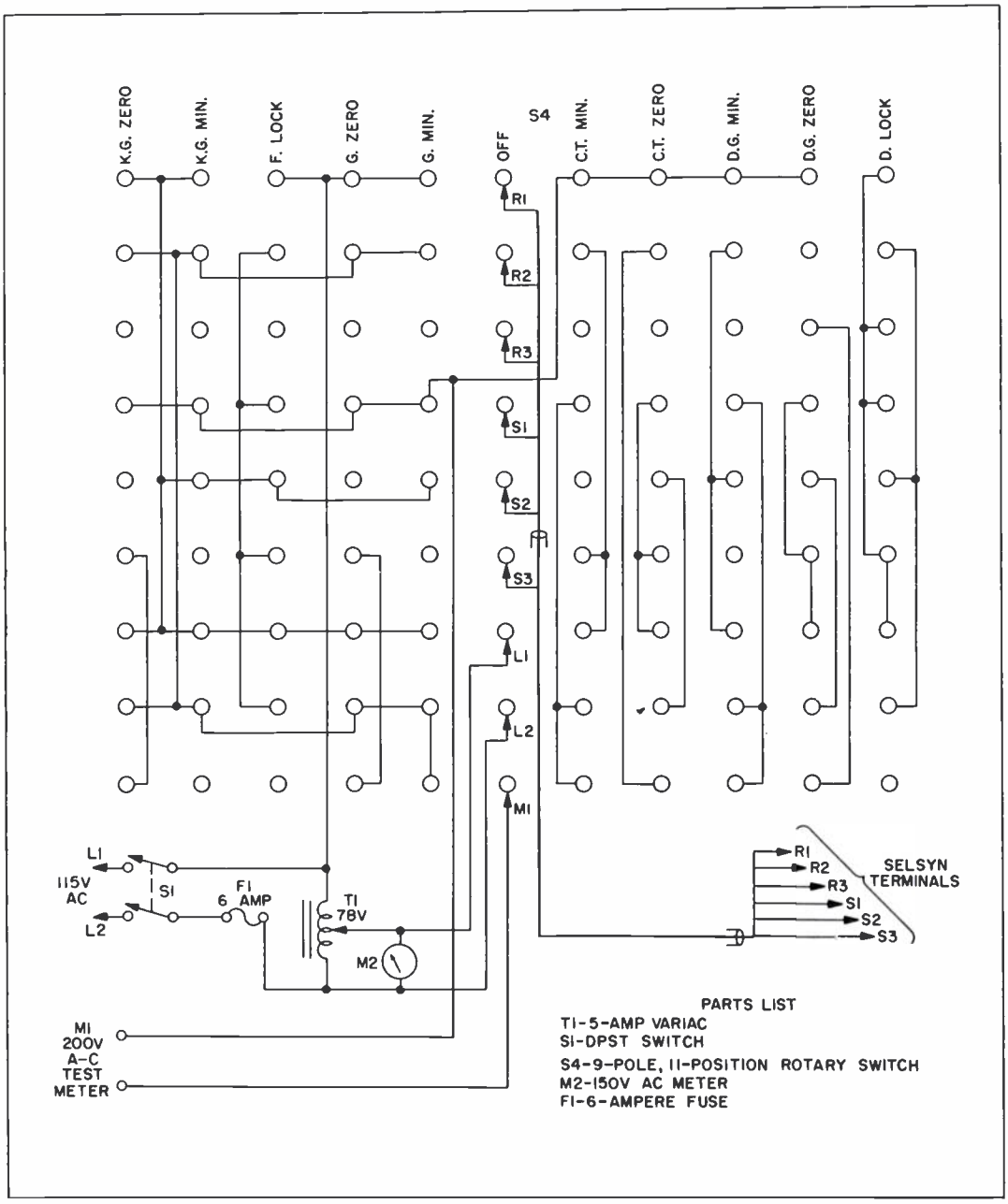


Figure 3. Schematic Diagram of Ideal Synchro Test Set

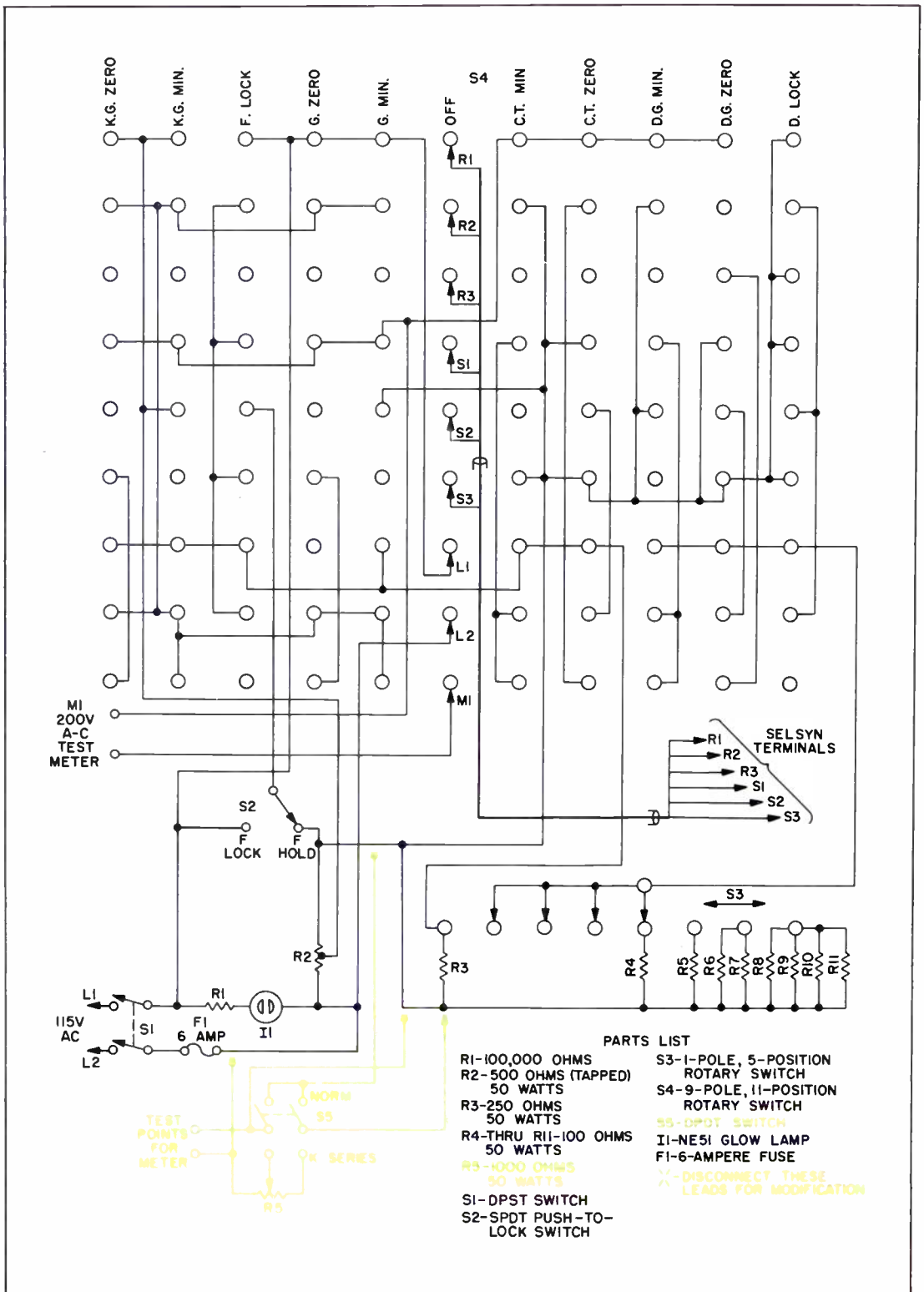


Figure 4. Schematic Diagram of Utility Synchro Test Set

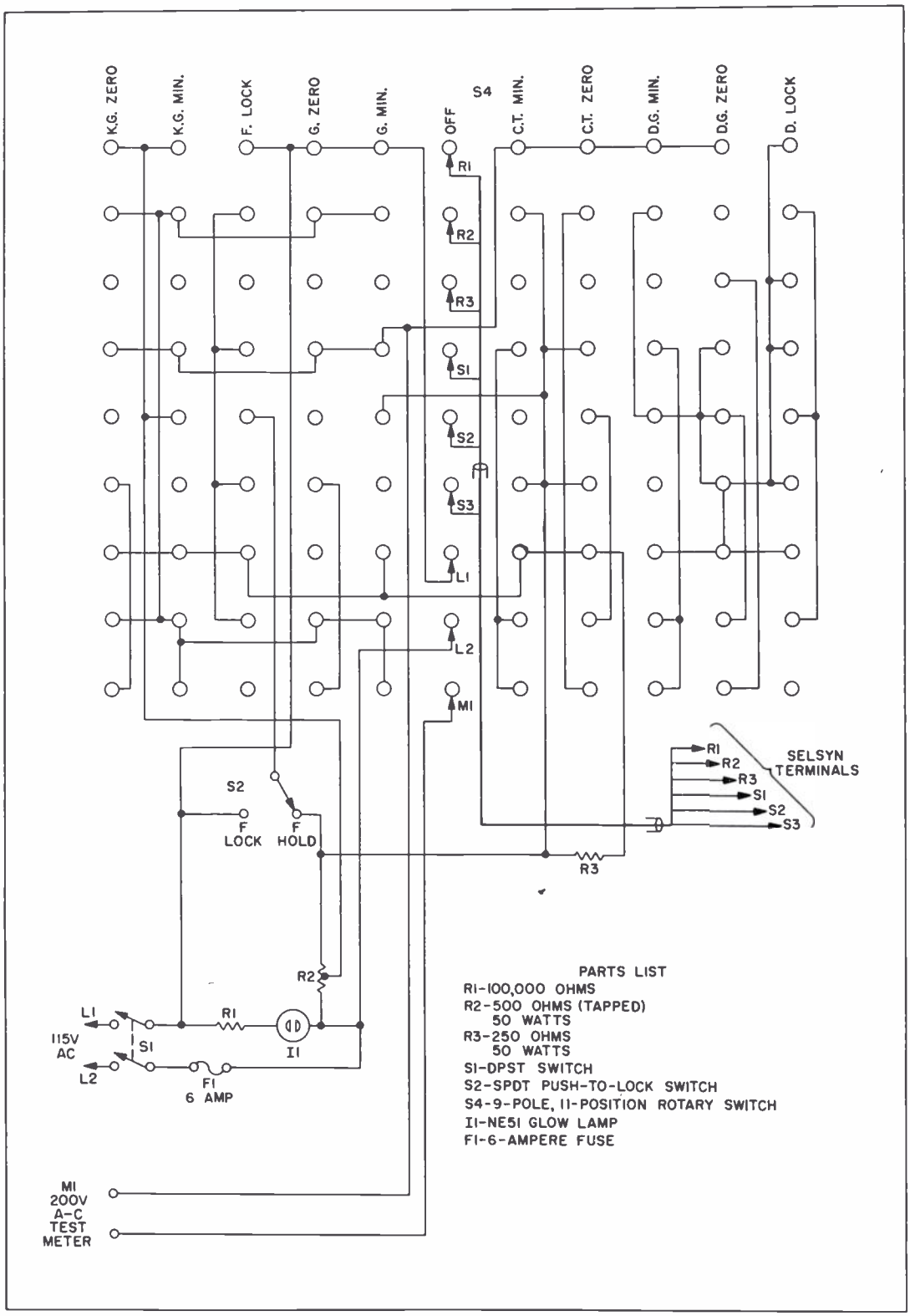


Figure 5. Schematic Diagram of Utility Synchro Test Set without Switch S3 and Resistors R4 through R11

DIGITAL COMPUTER MEMORY REQUIREMENTS

By Harold Small
Philco G & I Division

Editor's Note: This article describes the requirements of the memory section of an electronic digital computer and illustrates these requirements with the memory section of the Philco TRANSAC. It makes use of information contained in the author's article on magnetic core storage which appeared in the previous issue of THE BULLETIN.

A MODERN ELECTRONIC digital computer performs arithmetic operations with great rapidity, requiring only a few microseconds for each operation. For such a computer, the use of an operator to set up the instructions for each succeeding operation, as is done in an ordinary desk calculator, would result in much idleness of the computer, because the setting-up time would greatly exceed the computing time. Therefore, for maximum computer use, the instructions must all be set up and stored, before the computation starts, and made accessible for use by the computer. The computer may then follow the instructions in sequential order or in the order called for by the instructions. The device in which the instructions are stored is called a *memory*. In addition to the storage of instructions, the memory serves as a "scratch pad" in which the arithmetic units store partial results, as well as final answers that must be held until needed by an output device.

Many types of memory units have been successfully operated. A few of these include the cathode-ray tube, which stores information on its screen, the capacitor-diode storage unit, the magnetic drum, the delay line, and the magnetic core.

In addition to having one or more drawbacks in regard to size, speed, cost, etc., most of these memories need some form of regeneration cycle. This cycle is necessary because the contents of the particular memory are lost under certain conditions, such as when the power is turned off. Magnetic storage, however, will last almost indefinitely under favorable circumstances, without any form of regeneration, and is therefore a very useful approach to the storage problem. Generally speaking, if it is not desirable to use a form of tape storage, magnetic storage presents a choice of a magnetic drum or a ferrite core matrix type memory.

It should be noted that, although a core memory has faster access and is generally a smaller package than a magnetic drum, it does have the disadvantage of a destructive readout, requiring the information to be rewritten after having been read. However, the over-all read/write time is still much less than that for a magnetic drum.

The characteristics and specifications of a memory vary considerably, and are in general dependent on the function of the memory. In a high-speed digital computer, where the time required for an arithmetic operation is on the order of one or two microseconds, the longest operation that the computer performs (exclusive of input/output) is the memory reference. The time of a memory operation may be 10 to 20 times as long as that of an arithmetic operation. Hence, it may be seen that the speed and efficiency of the computer

are directly proportional to the access time of the memory unit.

For the purpose of this article the memory unit under discussion is assumed to be for use with a high-speed computing device, and all explanations are based on Philco TRANSAC S2000 type memory circuitry.

With the advent of transistors, the trend in the packaging of computers, as well as other electronic equipment, turned toward full-scale miniaturization. The goal was to make a computer light enough, small enough, and with sufficiently low power requirements that it could be easily installed as office equipment, requiring no more space than a large desk. The core memory, which is small and compact and an ideal match for the miniaturized transistors, is well suited to the miniaturization requirements of computers. Transistor manufacturers, aware of the rapidly expanding computer field and the ever-growing need for fast switching transistors, are now concentrating on the production of transistors designed for computer applications.

However, there is still much to be desired in high-current transistors, and this factor alone places great limitations on the design of memory circuits. The basic circuits required in a typical core memory include:

1. Inhibit current driver circuits.
2. Read and write current driver circuits.
3. Sense amplifiers.
4. Timing chain circuitry.

Much of the difficulty of core memory design centers around the current driver circuits. Specifically, the problem consists of obtaining a transistor that will handle high currents at high switching speeds, and of minimizing the resultant hole storage, which is almost inevitable, especially in the slower type transistors that have to be driven harder. One of the few transistors capable of being used in current driving circuits and available in the medium-price range is the Philco T-1337. This transistor was developed for the task as a result of the cooperative efforts of Philco memory experts and the Lansdale Tube Company's transistor specialists.

One of the most popular methods of combating hole storage is the use of complementary symmetry emitter follower circuits, to drive the output transistor on and off. These circuits, employing NPN and PNP transistors in series, use the PNP transistor to drive the PNP type output transistor on, and the NPN transistor to supply a positive turnoff voltage to assist in rapid recombination of electrons and holes. In the typical current driver circuit shown in figure 1, it may be seen that transistors T1 and T2 are used to change the voltage level from 0 to 3 volts to the 6 volts needed for the complementary symmetry emitter followers, with two stages of the emitter follower drivers driving a grounded-emitter output transistor. This type circuitry performs two functions in the memory:—

1. It serves as an inhibit current driver, which is used for the purpose of writing 0, and it also doubles as a post-write disturb driver.

2. It serves as a read/write current driver, which is used in conjunction with a transistor switch circuit to drive a number of core lines economically.

The switch circuit shown in the top half of figure 2 also makes use of complementary emitter follower circuits. T8, T9, T10, and T11 are used to "turn on" the four T1337 parallel emitter followers. A choice of read or write drivers for the odd- or even-numbered core line results in the energizing of only one transformer winding. Note that each transformer has two primary windings, and that these are out of phase with each other. Therefore, for the same input pulse, it is possible to obtain a current pulse of

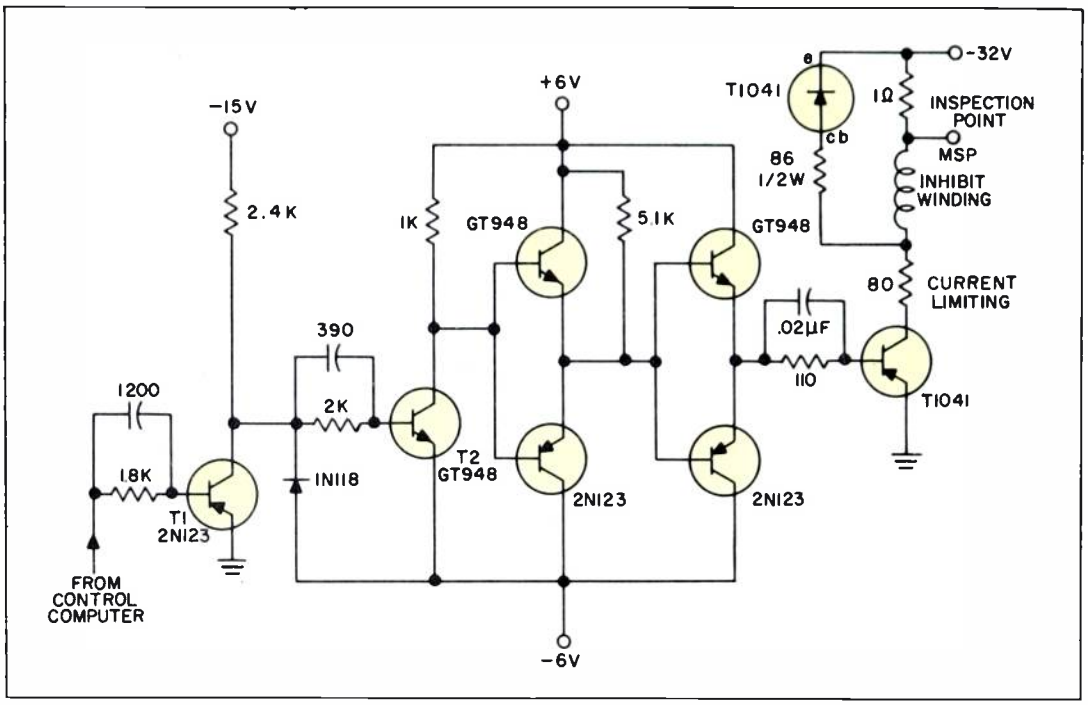


Figure 1. Inhibit Circuit

either polarity in the output winding, merely by selecting the appropriate primary.

To fully appreciate how the switch read-write combination of circuits works, it must be understood that switching current could be supplied to any number of core lines in a core matrix with one current driver per line. However, in the circuit combination mentioned above, each switch circuit selects two core lines, and a choice of odd- or even-numbered line is made in the selection of the driver circuits. For example, assume a 64 x 64 core matrix. If 32 switches, each selecting two core lines (see figure 2) are used in selecting one coordinate, it will be seen that each line has its own transformer. The primaries of each transformer are connected to the appropriate read or write current drivers. If 0 and 1 designate even- and odd-numbered lines respectively, then read 0 (R_0) and write 0 (W_0) are the read and write drivers for the even-numbered line, and read 1 (R_1) and write 1 (W_1) are the corresponding drivers for the odd-numbered lines. By connecting all R_0, W_0, R_1 and W_1 connections in parallel on all switch circuits, it can be seen that only four read/write drivers are needed to select any one of the 64 lines and also to select reading or writing currents. Although current drivers are connected to all the switches, only the one connected to the switch that is turned on will be affected. A similar set of switches and current drivers would be required for the other coordinate.

The Sense Amplifier — When a selected core in the matrix is interrogated, if the state of magnetism changes and induces a voltage in the sense winding, the core is considered to have held one type of information; similarly, if there is no change of flux and no voltage induced in the winding, the core is considered to have held the opposite information, i.e., 0 or 1, this being the language or intelligence of a computer. A good sense amplifier must fulfill at least three requirements:—

1. It must possess fast recovery time, that is, a good high-frequency response.
2. It must be able to amplify signals

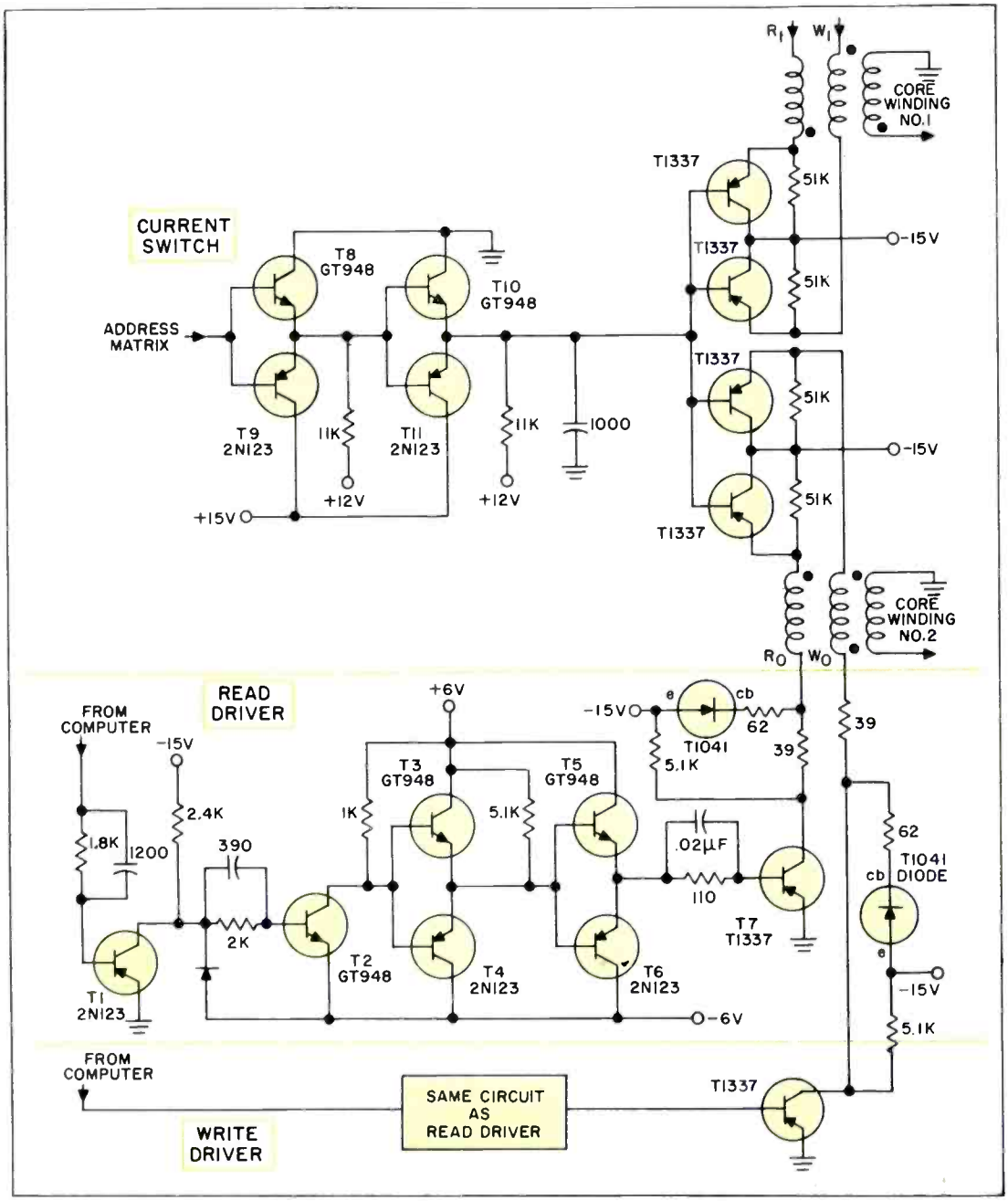


Figure 2. Read-Write Driver and Current Switch

of very low level (on the order of a few millivolts).

3. It must be able to reject common mode noise.

To understand common mode noise, it is necessary to consider broadly the two types of signals that are present at the output terminals of a sense winding.

One type is the correctly sensed signal, which is produced by the flux change in a core (or cores) through which the sense winding passes. This signal appears at each output terminal, but the polarity at one terminal is opposite that at the other. The other type is common mode noise, which also appears at each output of the sense wire. In this case, however, the polarity is the same at both outputs.

A comparison of common mode noise versus the required output signal is shown in figure 3.

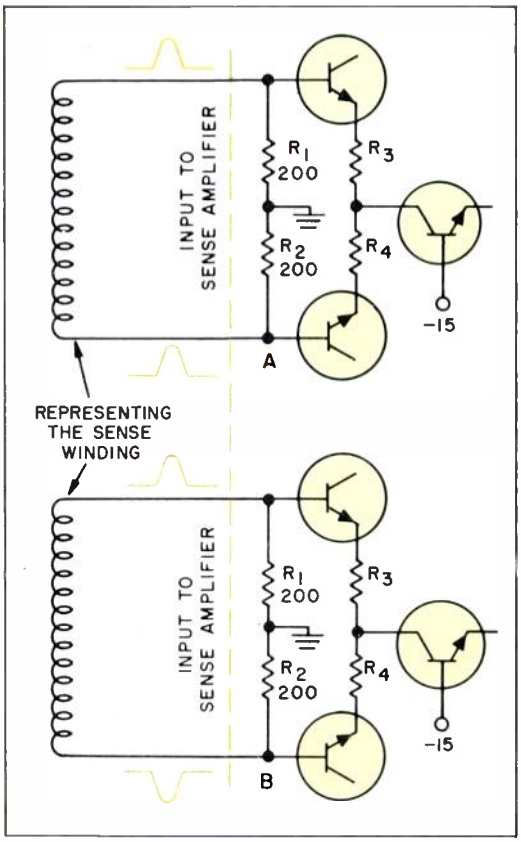


Figure 3. Sense Amplifier, Showing Comparison of Signals of Same Polarity (A) and of Opposite Polarity (B)

Sense windings are wound in several designs, but the aim in all cases is to eliminate as much of the disturbed pulse noise as possible by cancellation. However, in a 64 x 64 matrix all core noise can be cancelled except that from two cores, and the noise from these cores will either add or subtract from the required sense, depending on the position of the interrogating core in the matrix. It can be seen in figure 4 that the sense amplifier has a balanced input. T1 and T2 are supplied with an emitter bias by a constant-current source consisting of R5 and T3. Two ends of the sense wire are terminated at the bases of T1 and T2 with 200-ohm resistors to ground. If the inputs to T1 and T2 are alike, as in the case of common mode noise, the transistors continue to share the emitter current equally, and no change occurs in the primary current through L1 and L2. Since there is no induced voltage in L3 and L4, it can be seen that common

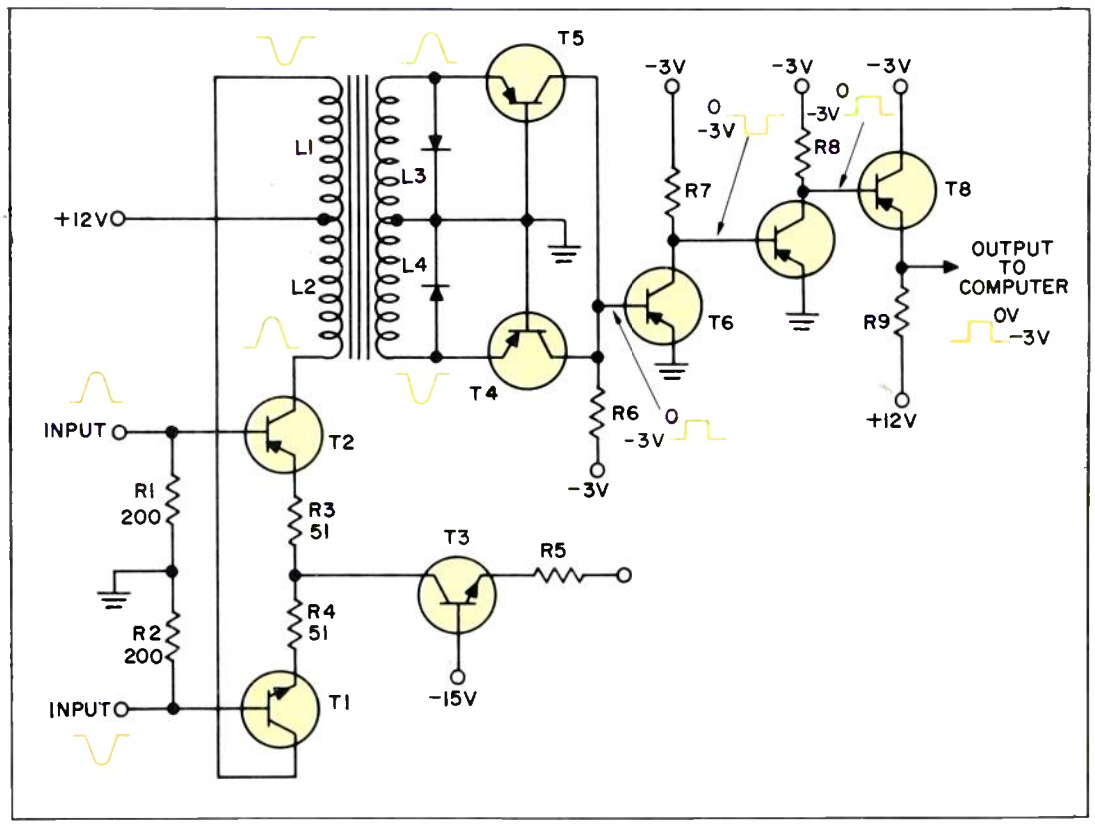


Figure 4. Sense Amplifier Circuit

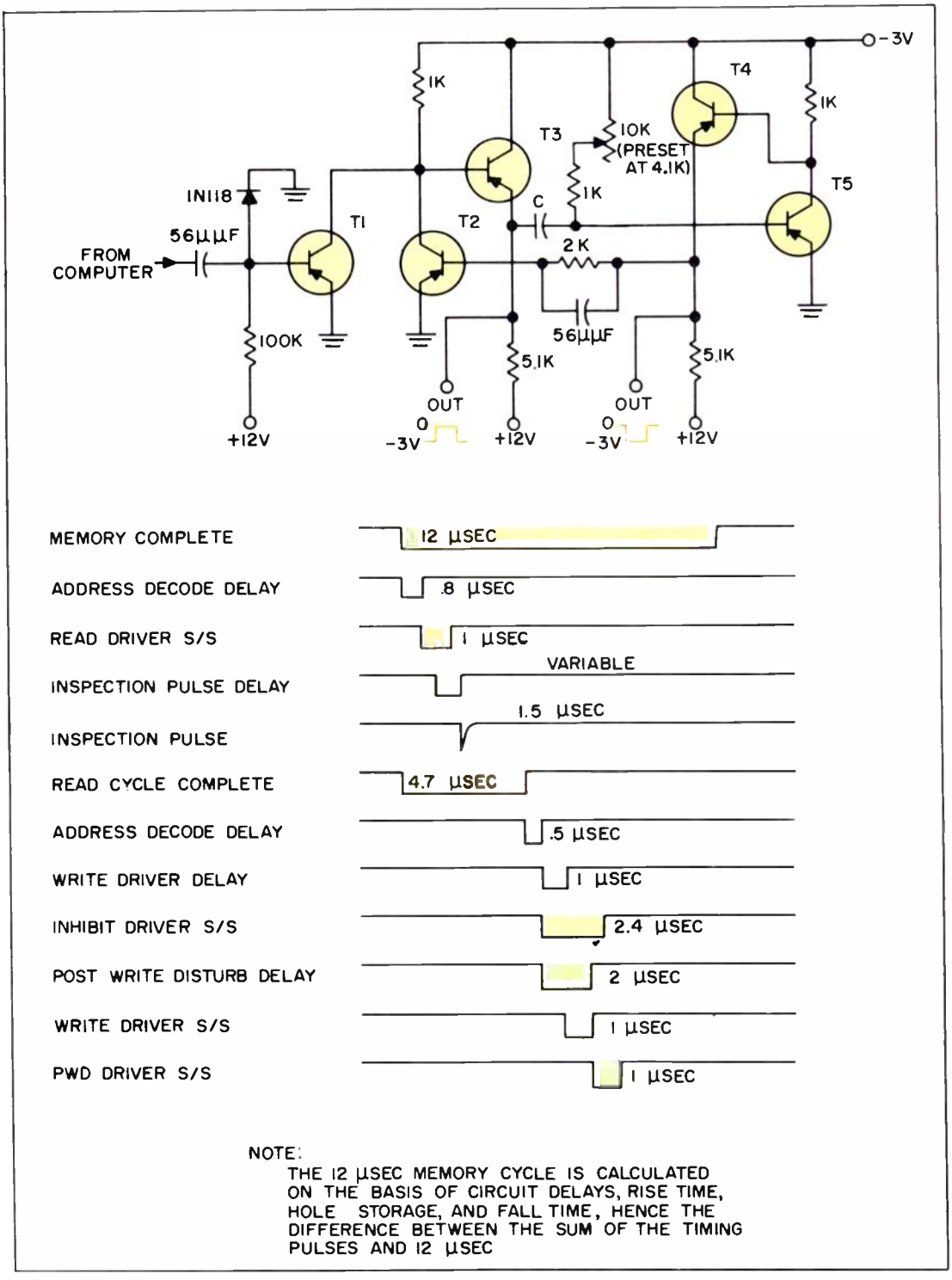


Figure 5. Single-Shot Multivibrator Circuit

mode noise will not be passed beyond this point in the amplifier. When a voltage is induced in a sense wire by the switching of a core, the input signals presented to the bases of T1 and T2 will be of opposite polarity, as shown in figure 4. From the example in figure 4 it may be seen that, since T1 and T2 are NPN transistors, T2 will be caused to draw more current, and T1 to draw less current; consequently, the current through L2 will increase and the current through L1 will decrease. Voltage waveforms will

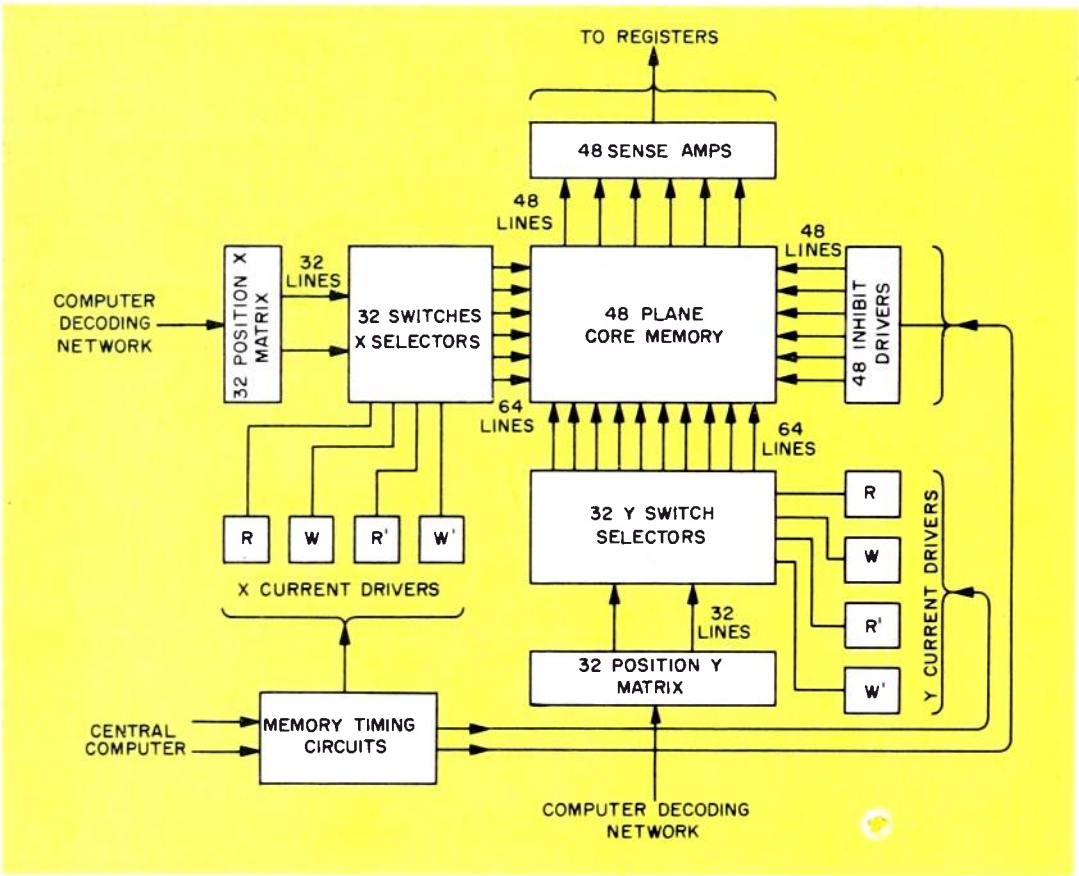


Figure 6. Memory Block Diagram

be induced in secondaries L3 and L4, as indicated in the figure. T5 will be turned on by the positive voltage on its emitter, and the resultant current through R6 will cause a 3-volt positive-going signal to be applied to the base of T6. This signal is amplified by a two-stage amplifier, and a positive-going pulse is fed out to the main computer via emitter follower T8. When the input to T1 and T2 reverses, T4 will conduct, but the output will appear the same at T8.

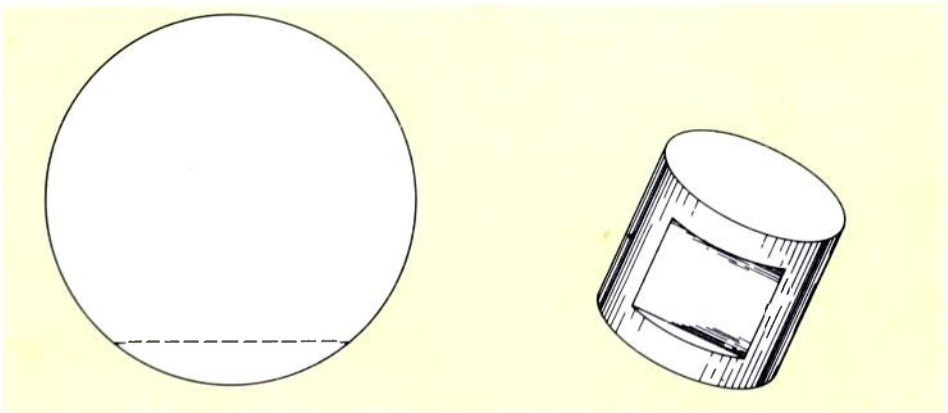
Memory Timing — One of the most important sections of the memory is its timing chain. The timing chain to be discussed uses one-shot, multivibrator circuits, as shown in figure 5. When a pulse is applied to the input of the single-shot circuit, it is differentiated and the negative portion turns on T1, causing a positive-going voltage to be applied to the base of T-3. This positive-going voltage is coupled through capacitor C to the base of T5, cutting it off. This results in a negative voltage being applied to the base of T4, turning T4 on and applying a negative-going voltage to the base of T2. This voltage turns T2 on, reinforcing T1. As C discharges through the resistors, the voltage at the base of T5 goes negative, and at some point T5 turns on. The positive-going voltage from the collector of T5 is in turn fed back to T2, cutting it off and ending the cycle. The outputs are taken from emitter followers T3 and T4 as shown. Also illustrated in figure 5 is a typical timing diagram showing the time at which each memory operation is triggered, and the reason for the delays between certain operations. The entire memory cycle is bracketed by one of these single-shot pulses, which not only serves to indicate the end of the mem-

ory cycle, but prevents the memory being used at a higher repetition rate than the calculated duty cycle would permit safely.

Figure 6 illustrates the manner in which the various memory units go together to form the complete memory. The computer decoding network and matrix, together with the memory timing circuits, select the memory position required, and transmit the information via the sense amplifiers to the registers in the central computer. As dictated by the requirements of the computer, the inhibit and write drivers are set up to restore previous information or to write new information into the memory. The estimated access time of a memory of the type that has been discussed in this article is 12 microseconds.

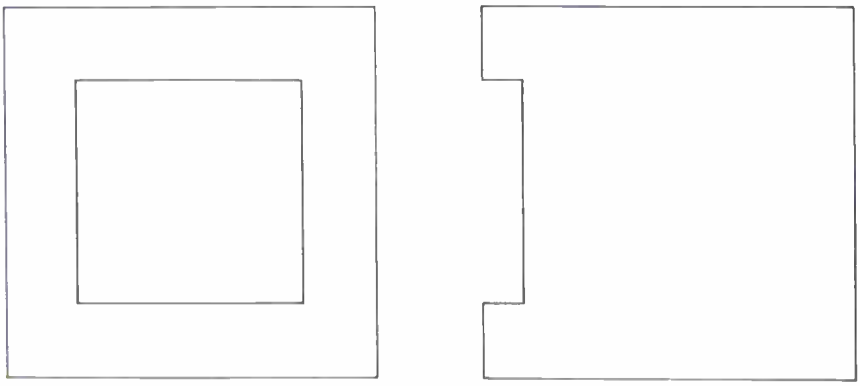
Solution to March - April "WHAT'S YOUR ANSWER?"

The drawings below indicate the solution to the problem of the solid object. The top view which was required is shown on the left, and a three-dimensional view illustrating the solid object is shown on the right. Notice that the dashed line indicates that the edge is not visible from the top.



TOP VIEW

PICTORIAL



FRONT VIEW

SIDE VIEW

AGING CRYSTAL PLATES

By Harold C. Reynolds
Technical Publications Department

This article describes a method of changing the resonant frequency of a crystal by chemical etching. Such a change is often desirable, to permit the use of inexpensive crystals in applications requiring precisely controlled frequencies.

THE PROBLEM OF FREQUENCY stability in communications equipment is of extreme importance to all who are concerned with such equipment. Crystal control provides the necessary stability, but, in order to use this method, it is necessary to have crystals which operate at specific frequencies. For those concerned with military or commercial equipment, obtaining such crystals when needed may sometimes be difficult because of an emergency, shortages in stock, or isolation from normal sources of supply. For the amateur radio operator, obtaining the correct crystals for his specific requirements at a reasonable cost is often a problem. Many inexpensive crystals at various frequencies are available to the amateur, but, in general, such crystals were manufactured for use in military equipment and, in most cases, will not operate at a desired frequency within the bands assigned to amateur radio.

By using one or more of a number of different methods, inexpensive crystals which are a few kilocycles below the desired frequency may be "aged" until they operate at the desired frequency. "Aging" is a general term which is applied to all methods of changing the frequency characteristics of a crystal. One such method is the use of a chemical erosion action on the crystal to change the resonant frequency.

The resonant frequency of a crystal is determined to a great extent by its thickness. Hence, by etching the crystal surfaces with an appropriate solution, it is possible to reduce the crystal thickness and thus increase the resonant frequency. It is important to realize that, although the thickness of the crystal plate is the major factor in determining the resonant frequency, many other factors will, over a period of time, produce slight changes in the frequency characteristics of a particular crystal. These factors include small irregularities in the crystalline structure of the plate, the development or release of gas from the crystalline structure, the addition or growth of foreign matter, temperature changes and thermal reaction, mechanical or frictional wear, and the absorption of gas or moisture as a result of leakage in the crystal holder. In addition, the unpredictable effects of overdriving the crystal should not be overlooked.

Commercial manufacturers, in general, age crystals by grinding with an abrasive and lapping. However, many manufacturers also include a final step consisting of etching to reduce small lapping marks, to remove foreign particles from the surfaces, to meet precise frequency specifications, and to improve crystal activity.

Many etching solutions may be used; two common ones are a good commercial grade of 47% hydrofluoric acid (HFl) and a 25% water solution of ammonium difluoride. A word of caution is important at this point. Since etching solutions and their fumes are highly toxic, it is necessary to perform the etching in a clean, well-ventilated working area. These chemicals are also extremely harmful to the skin, and to many other surfaces. Extreme care

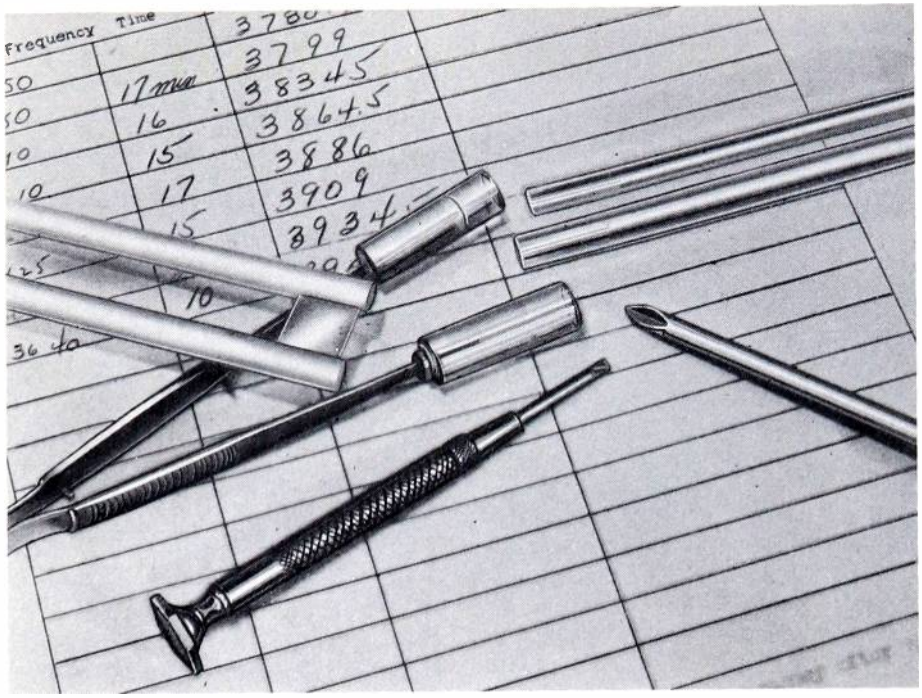


Figure 1. Tools Required for the Aging Process and Log in which Data is Recorded

must be exercised to insure that proper (polystyrene) containers are used and that they are protected so that the solution does not spill. If the solution inadvertently comes into contact with the skin, the area of contact should be thoroughly washed with soap and running water. Although best results will be obtained with distilled water, the use of tap water is suggested because it is readily available in a renewing supply. However, if the available tap water contains chemicals which would inhibit the neutralizing action, distilled water should be used. Other neutralizers for hydrofluoric acid are trisodium phosphate, ammonium hydroxide, and baking soda dissolved in water. THE IMPORTANCE OF OBSERVING THESE PRECAUTIONS CANNOT BE OVEREMPHASIZED.

Figure 1 shows the tools required for assembling and disassembling the crystal holder (small slot screwdrivers and a small Phillip's head screwdriver are sufficient for all generally used crystal holders), the necessary polystyrene containers for immersing the crystal, and a record sheet used to log the etching time and frequency during the aging procedure. Also shown are two types of implements used to hold the crystal plate in the etching solution. One of these implements was fabricated from a medium size forceps by heating the tongs and forcing two polystyrene rods onto them to a depth of approximately 3/8 inch. (The polystyrene rods used are 1 inch long and 3/8 inch in diameter.) The forceps should be allowed to cool in the polystyrene before using. (To aid in the cooling process, warm water is applied to the forceps approximately 1/2 inch from the polystyrene rods.) The U-shaped tool is made from a polystyrene rod, by applying the heat from a normal soldering iron or a small flame a short distance from the polystyrene, bending, and allowing the assembly to cool. The grooves which hold the crystal are produced with a hacksaw blade. Shaping should be such that when used, the tongs will apply sufficient pressure to the edges of the crystal to prevent sliding or slipping.

Figure 2. Test Oscillator Used To Determine Crystal Frequency

Figure 2 shows the test oscillator used to determine the mechanical mode of vibration and its sensitivity, which indicates the degree of vibration or the "Q" of the crystal. The degree of oscillation is indicated on the plate current meter, and crystal sensitivity is determined by the amplitude of the dip in plate current at resonance.

Either the transmitter oscillator itself or an equivalent circuit may be used as a test oscillator. However, if an equivalent circuit is used, it should have the same input capacitance as the transmitter oscillator.

As a preliminary to etching, the resonant frequency of the crystal is measured in the test oscillator. Figure 3 illustrates a crystal-holder adaptor, which is fabricated by modifying a standard spring-loaded wooden clothespin as shown in figure 3. The modification consists of adding conducting surfaces to the inner surfaces of the jaws and attaching connecting wires between the surfaces and a modified crystal holder which is plugged into the test oscillator. In use, the crystal sandwich is grasped by the edges and inserted between the jaws of the clothespin. Pressure holding the clothespin open is then released, so that the crystal and plates are rigidly held between the two conducting surfaces. It should be noted that the conducting surfaces of the modified clothespin will make contact with the metal plates (taken from the crystal holder assembly) that sandwich the crystal under test. The frequency of the crystal is then measured and recorded on the record sheet. For good results, it is necessary that the faces of the crystal and the surfaces of the conducting plates be clean and free of lint and other foreign matter. These surfaces can be cleaned with carbon tetrachloride, alcohol, gasoline, or any other cleansing agent, rinsed in water, and carefully dried with clean, absorbent, lintless material. (Since carbon tetrachloride fumes are toxic, cleaning with this agent should be performed in a clean, well-ventilated area.)

After measurement of the resonant frequency, the crystal is placed in the grooves of the polystyrene rods and immersed in the etching solution as shown in figure 4. Best results are obtained if the crystal is slowly agitated while in the solution, because agitation tends to smooth out surface irregularities and remove the lapping pattern, loose particles, and particles of old abrasives. The resulting flat surface improves crystal sensitivity.

After approximately 30 seconds, the crystal plate is removed from the etching solution and quenched in a prepared neutralizing bath for a minimum

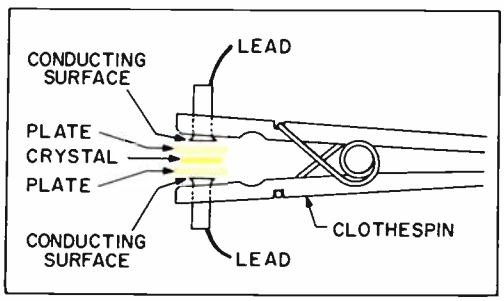


Figure 3. Modified Spring Clothespin Used in Crystal Frequency Measurement

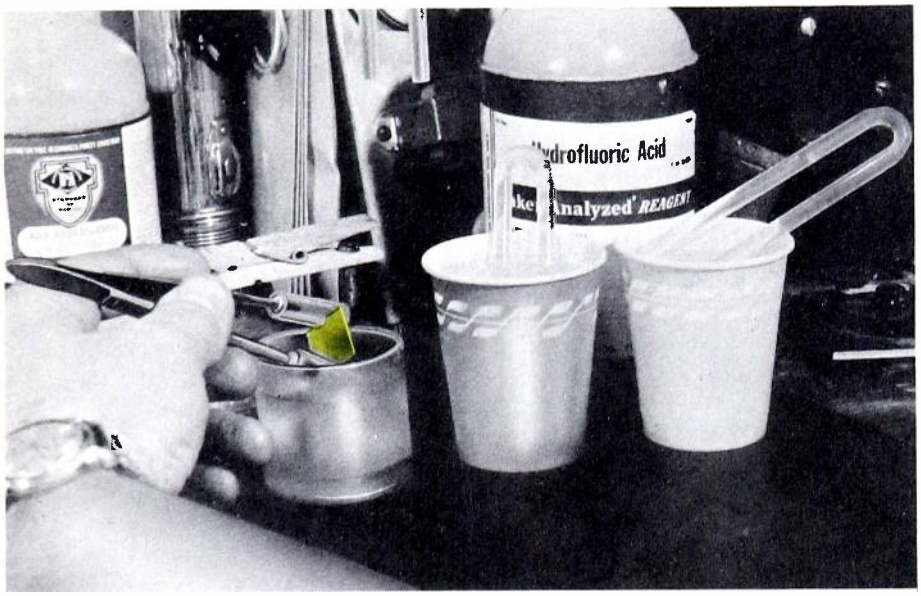


Figure 4. Equipment Required for Crystal Etching, Including Tongs, Acid Bath, Neutralizer Bath with Tongs, and Rinse Bath with Tongs

of one minute. When the etching action has been quenched, the crystal is rinsed in clean water, carefully dried, and inserted in the test oscillator. The resonant frequency is measured and recorded, along with a note of the exact time for which the crystal was immersed. A knowledge of the change in frequency over a given etching time allows computation of the etching rate. From this rate, it is then possible to determine the etching time required to reach the desired frequency. It has been experimentally verified that the frequency increase with time in the etching solution is approximately linear, but that this increase varies with both the type of crystal and the individual crystal itself. Because of the many variables (cut of the crystal, structural characteristics such as synthetic having piezoelectric properties, age of the etching bath, etc), it is not possible to give specific values for the expected etching rate. The 30-second etching period is included to provide this information, and etching rates of 100 to 5000 cps (an extremely broad range) for the 30-second period have been encountered. As soon as the measured frequency is within a few hundred cycles of the required frequency, to obtain a precise frequency, the etching should be performed in a series of short etching periods (1 to 2 minutes) with a frequency measurement being made and recorded at the end of each period. In this way it is possible to minimize the possibility of etching for too long a time.

When the desired frequency has been reached, the crystal should be slowly agitated in the neutralizing bath for a period of at least 5 minutes, rinsed in water, and immersed in a fresh neutralizing bath for several hours to remove all traces of acid. It is then carefully rinsed and dried and a final frequency check performed.

Since the etching action tends to round off the edges, it is desirable to grind these edges to improve the activity of the crystal. The equipment required for this operation (shown in figure 5) consists of two pieces of plate glass and two different mesh abrasives, a relatively coarse abrasive such as silicon carbide (average mesh 1250) and a fine abrasive such as aluminum oxide (average mesh 800). It

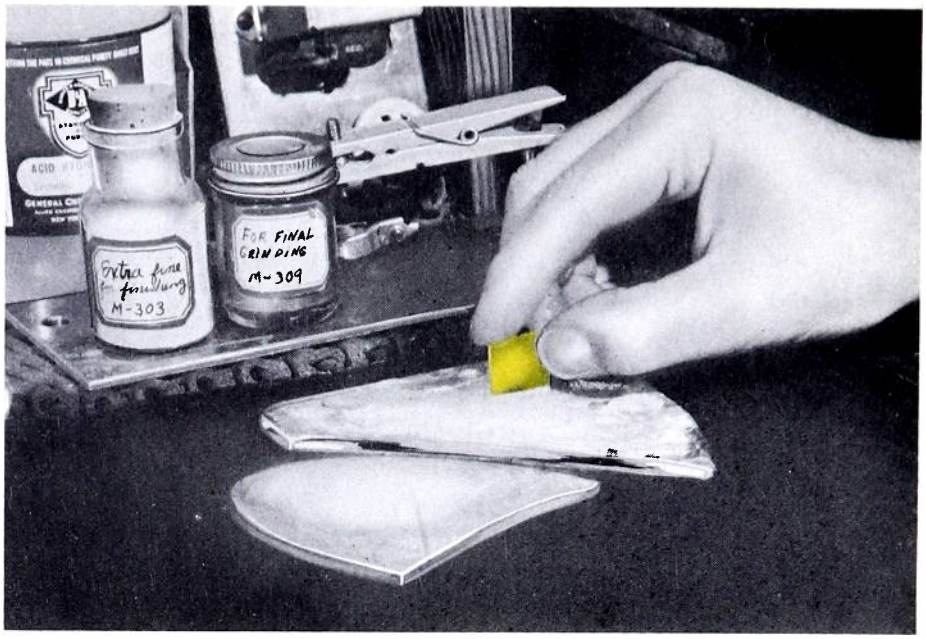


Figure 5. Edge Grinding a Crystal, Illustrating Equipment and Proper Method of Holding Crystal

is also possible, though not desirable, to use abrasives such as valve-grinding compound, household scouring powder, and jeweler's rouge.

Edge grinding is comparatively simple if one is relaxed while performing the operation. A firm hold on the crystal may result in cracking or crushing and, at the very least, increases the possibility of dropping, with possible resultant damage. As illustrated in figure 5, the crystal should be held in a vertical position by the thumb and two fingers and moved with a figure-eight motion in the abrasive, which has been converted into a paste by the addition of water or kerosene. (Kerosene is preferable, because it will retain the abrasive in a thin paste form for a longer period of time.) Care must be exercised to prevent applying too much pressure during the grinding operation, since excess pressure will result in chipping or cracking of the plate. Screeching, resulting from an improper crystal angle with the glass surface, should be avoided if possible. Do not under any conditions hold or guide the crystal plate by the flat etched surfaces. Contact with these surfaces can have an effect on the resonance of the crystal and also decrease its sensitivity.

When grinding all four edges, it is preferable to keep a systematic orientation and to perform the same number of figure-eight grinding motions on each edge. After all edges have been squared (determined by visual inspection), the crystal should be carefully washed with water or previously suggested cleansing agent to remove the abrasive, rinsed in clean water, dried, and checked in the test oscillator before reassembling it in the crystal holder.

The method of chemical etching is a simple and fairly rapid way of obtaining crystals of a specific frequency at a low cost. Although primarily intended for amateur radio operators, it may be useful to those concerned with military and commercial equipment if crystals of the proper frequencies are not immediately available.

POLES, ZEROS, AND THE FOSTER REACTANCE THEOREM

By H. W. Merrihew
Headquarters Technical Staff

There are a number of methods which may be used in predicting the behavior of a network. The most common of these is the steady-state and transient analysis given in most textbooks on network theory. This article describes another approach, the pole and zero method, which makes use of the points at which the impedance becomes either zero or infinite.

THE POLE AND ZERO method of characterizing the behavior of a network makes use of the points at which the impedance function of the network becomes either zero or infinite. Although for the sake of simplicity this article will be restricted to networks containing only reactive components (a severe restriction), it is also possible to employ the pole and zero approach to characterize the behavior of networks which contain both resistance and reactance. In addition to determining the behavior of a network, it is also possible to reverse the process, that is, to design a network having a desired response curve, by using the pole and zero method.

Before proceeding further, it is necessary to define the terms *pole* and *zero*. A pole is defined as a point at which the value of a function (for present purposes the impedance function of a reactive network) becomes infinite, and a zero is defined as a point at which the value of the function becomes zero.

As an illustration of these definitions, consider the equation representing the impedance function of an inductive reactance.

$$X_L = \omega L$$

It can be seen that, if L is regarded as constant, $X_L = 0$ when $\omega = 0$, and that $X_L \to \infty$ as $\omega \to \infty$. (The sign $\to$ is a mathematical convention which means "approaches" or "gets close to".) Thus this particular impedance function displays a zero at $\omega = 0$ and a pole at $\omega \to \infty$.

As shown in figure 1, which shows the graph of the impedance function $X_L = \omega L$, the zero is signified by the symbol 0. Since the pole at $\omega \to \infty$ is not on the diagram, it is not indicated. Note that the graph is not extended to the left of the vertical axis, since this would represent negative frequency, a meaningless concept from a practical point of view.

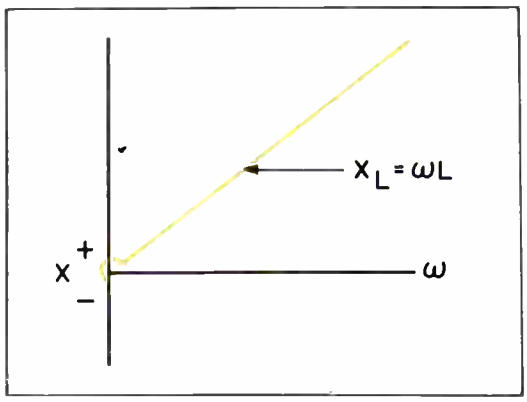


Figure 1. Graph of the Equation $X_L = \omega L$

As another illustration of the definitions, consider the equation representing the impedance function of a capacitive reactance.

$$X_C = \frac{1}{\omega C}$$

The graph of this impedance function is illustrated in figure 2, and shows that as $\omega \to 0$, $X_C \to \infty$, and that as $\omega \to \infty$, $X_C \to 0$. This impedance function displays a pole at $\omega = 0$ (repre-

sented by the X on the ω axis) and a zero at $\omega \to \infty$. Since the zero is off the diagram, it is not indicated.

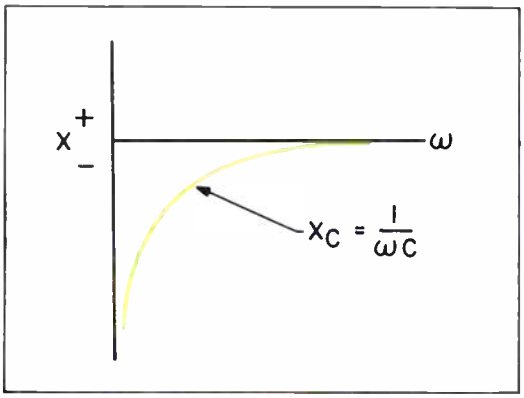


Figure 2. Graph of the Equation $X_C = \frac{1}{\omega C}$

The poles and zeros illustrated in the two preceding examples are known as *external poles* and *external zeros*, because they occur at the ends of the impedance function graphs. It is also possible for a pole and/or a zero, or more than one of each type, to exist between the ends of an impedance function graph. Such poles and zeros are called *internal*, and are used together with the external poles and zeros to characterize the impedance function of more complex two-terminal reactance networks.

As an illustration of a slightly more complex network, consider the series L-C circuit shown in part A of figure 3. The equation representing the impedance function of this circuit is

$$Z = j\omega L - \frac{1}{j\omega C} \qquad (1)$$

(This is the complex number representation of a vector, where Z is a vector quantity and $j = \sqrt{-1}$.) The graph of this impedance function is given in part B of figure 3.

Although equation (1) is the simplest representation of the function, equation (2) below may be obtained from equation (1) by comparatively simple manipulations.

$$Z = j\omega L \left(\frac{\omega^2 - \frac{1}{LC}}{\omega^2} \right) \qquad (2)$$

It can be seen by examining equation (2) that if the value of ω is such that

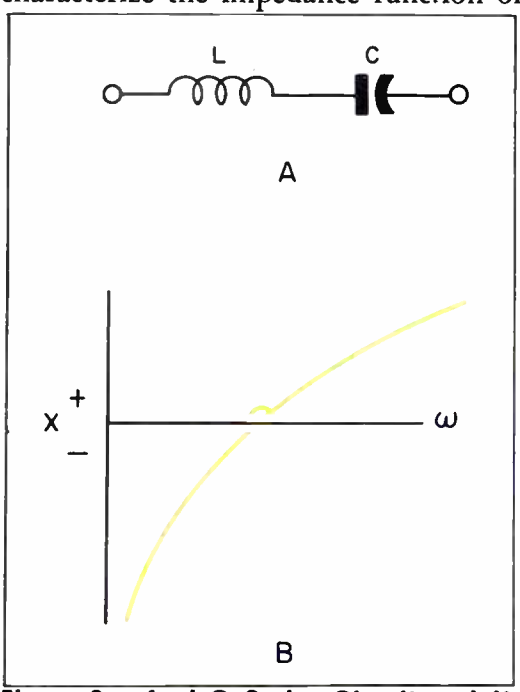


Figure 3. An L-C Series Circuit and Its Reactance Curve

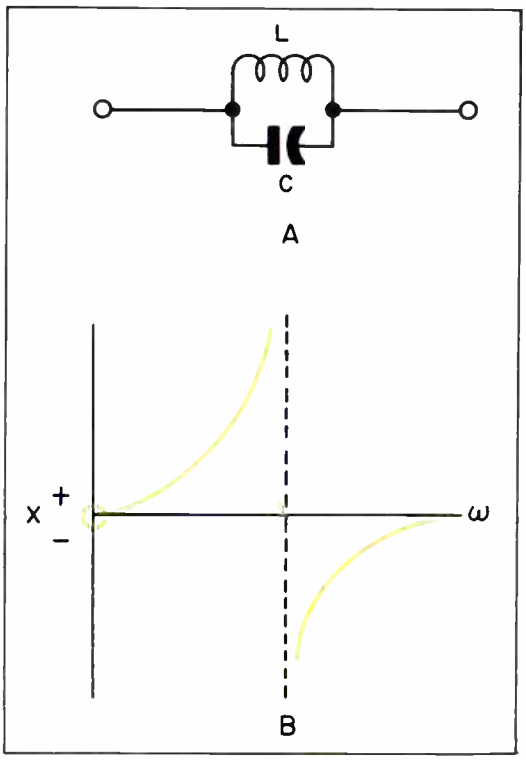


Figure 4. A Parallel L-C Circuit and Its Reactance Curve

$$\omega^2 = \frac{1}{LC}$$

or

$$\omega = \pm\frac{1}{\sqrt{LC}} \qquad (3)$$

then Z becomes equal to 0, and a zero exists at this point. Since negative frequency is meaningless from a practical point of view, only the positive solution in equation (3) is used. The internal zero at the frequency specified by equation (3) (ω is the angular frequency, and is equal to $2\pi f$) is the series-resonant frequency of the circuit.

It can also be seen from equation (2) that two external poles exist, because as $\omega \to \infty$, $Z \to \infty$, and as $\omega \to 0$, $Z \to \infty$.

Since the graph representing the impedance function given by equation (2) is a smooth curve, the two poles and the zero found above provide enough information to enable a curve (correct except for a scale factor) to be drawn. Thus, the poles and zeros completely specify the network impedance function. The manipulation employed to obtain equation (2) is used to more clearly indicate that an internal zero occurs at $\omega = 1/\sqrt{LC}$. Since the denominator, ω, does not become zero except at $\omega = 0$, there is no internal pole, and series resonance is therefore characterized by an internal zero which occurs at the resonant frequency.

The impedance function of the parallel circuit (the dual of the series circuit) shown in part A of figure 4 is given by the equation:

$$Z = \frac{-\frac{j}{\omega C}(j\omega L)}{j\omega L - \frac{j}{\omega C}} \qquad (4)$$

Again by comparatively simple manipulations, equation (4) above can be changed into the form below.

$$Z = \frac{-j\omega}{C}\left(\frac{1}{\omega^2 - \frac{1}{LC}}\right) \qquad (5)$$

From this equation, it can be seen that if the value of ω is such that

$$\omega^2 = \frac{1}{LC}$$

or

$$\omega = \pm\frac{1}{\sqrt{LC}} \qquad (6)$$

the impedance will become infinite, and that if ω^2 is slightly smaller than $1/LC$, the impedance will be a large positive value, while if ω^2 is slightly larger than $1/LC$, the impedance will be a large negative value. Thus an internal pole exists at $\omega^2 = 1/LC$, and Z approaches either ∞ or $-\infty$, depending upon the direction from which ω approaches $1/\sqrt{LC}$.

It can also be seen that two external zeros exist, because $Z = 0$ when $\omega = 0$ and $Z \to 0$ as $\omega \to \infty$. Since equation (5) represents a smooth curve, a knowledge of the internal pole and external zeros is sufficient to enable the curve representing the reactance function to be drawn as shown in part B of figure 4. This curve is accurate except for a scale factor, and parallel resonance is therefore characterized by an internal pole which occurs at the resonant frequency.

In connection with the comparison between series and parallel resonant circuits, it is interesting to note that, as might be expected, a pole is the dual of a zero, and vice versa.

Before considering more complex networks, it is desirable to indicate several general features of reactance curves. These features are summarized in the four statements given below, and it should be noted that these statements hold only for networks containing pure reactive elements.

1. Poles and zeros alternate along the real frequency axis.
2. The slope of the reactance curves is always positive.
3. Either a pole or a zero must exist at $\omega = 0$ (the origin).

4. Either a pole or a zero must exist at $\omega \to \infty$.

These four statements are the result of an important network theorem known as the Foster Reactance Theorem, which states that the impedance of any two-terminal lossless network is completely specified, except for a scale factor, by the internal poles and zeros. (The proof of this theorem is quite complex, and will not be given in this discussion.)

Figure 5 illustrates a more complex reactive circuit and the response curve which results. In this case, the equation representing the impedance function is

$$Z = \frac{\left(j\omega L - \frac{j}{\omega C_1}\right)\left(-\frac{j}{\omega C_2}\right)}{j\omega L - \frac{j}{\omega C_1} - \frac{j}{\omega C_2}} \qquad (7)$$

By suitable manipulations, equation (7) above can be written in the form:

$$Z = -\frac{j}{\omega C_2}\left(\frac{\omega^2 - \frac{1}{LC_1}}{\omega^2 - \frac{C_1 + C_2}{LC_1C_2}}\right) \qquad (8)$$

It can be seen from this form of the equation for the impedance that an internal zero exists when

$$\omega = \omega_1 = \sqrt{\frac{1}{LC_1}} \qquad (9)$$

and that an internal pole exists (the impedance becomes infinite) when

$$\omega = \omega_2 = \sqrt{\frac{C_1 + C_2}{LC_1C_2}} \qquad (10)$$

Since an external zero exists at $\omega \to \infty$ and an external pole exists at $\omega = 0$, the impedance function is accurately represented by the graph in part B of figure 5.

As a final illustration of this method, consider the network shown in part A of figure 6. The equation representing the impedance function of this network

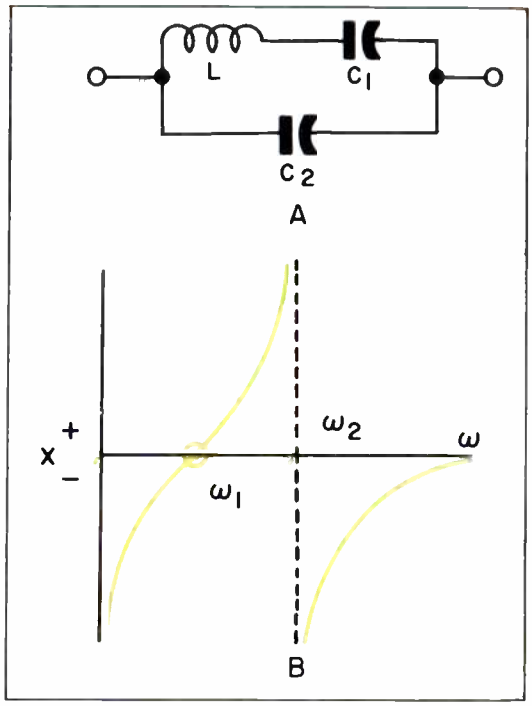


Figure 5. A More Complex Reactive Network and Its Reactance Curve

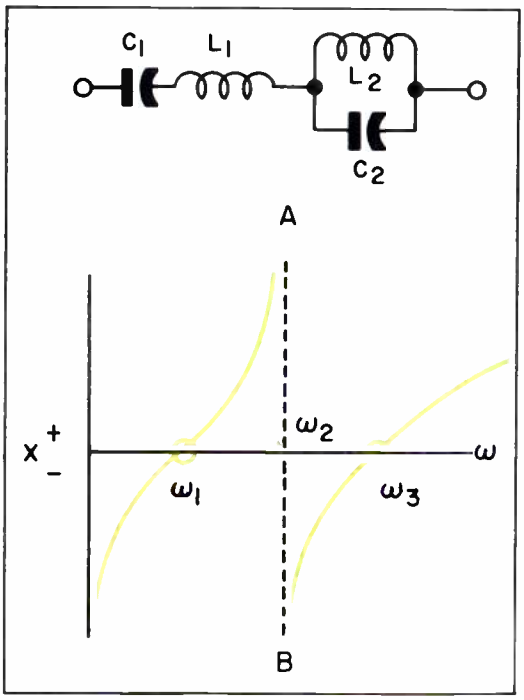


Figure 6. A Series-Parallel Circuit and Its Response Curve

is

$$Z = j\omega L_1 - \frac{j}{\omega C_1} + \frac{(j\omega L_2)\left(-\frac{j}{\omega C_2}\right)}{j\omega L_2 - \frac{j}{\omega C_2}} \qquad (11)$$

By proper manipulations, this can be rearranged to give

$$Z = (j\omega L)\left[\frac{\omega^4 - \omega^2\left(\frac{1}{L_1 L_2}\right)\left(\frac{L_1 + L_2}{C_2} + \frac{L_2}{C_1}\right) + \frac{1}{L_1 L_2 C_1 C_2}}{\omega^2\left(\omega^2 - \frac{1}{L_2 C_2}\right)}\right] \qquad (12)$$

There are two values for ω (designated ω_1 and ω_3) for which the numerator of equation (12) above becomes zero. Thus there are two internal zeros, one at ω_1 and one at ω_3. The denominator of equation (12) above will become zero at $\omega = 0$ and also at

$$\omega = \omega_2 = \frac{1}{\sqrt{L_2 C_2}}$$

Thus the impedance function has an internal pole at ω_2, and an external pole at the origin. From these facts, the graph of the impedance function can be drawn as shown in part B of figure 6.

By using an extension of the preceding illustrations and the Foster Reactance Theorem, it is possible to write a general expression for the impedance function that aids in predicting the forms that a general two-terminal lossless network can assume. This general expression is given as equation (13) below.

$$Z = A\,\frac{(\omega^2 - \omega_a^2)(\omega^2 - \omega_b^2) \ \ldots \ (\omega^2 - \omega_n^2)}{(\omega^2 - \omega_{a'}^2)(\omega^2 - \omega_{b'}^2) \ \ldots \ (\omega^2 - \omega_{n'}^2)} \qquad (13)$$

where:

A is equal to either $j\omega H$ or $\frac{H}{j\omega}$

H depends upon the value of L and/or C.

$\omega_a, \omega_b, \ldots \omega_n$ are values of ω which create internal zeros in Z.

$\omega_{a'}, \omega_{b'}, \ldots \omega_{n'}$, are values of ω which create internal poles in Z.

Equation (13) can assume four different forms. Each of these forms corresponds to one of the four possible reactance curves which can be obtained by assigning poles and zeros according to the requirements of the Foster Reactance Theorem. These four possible forms are given below, and for each case the impedance curve and the network which gives the function are also shown.

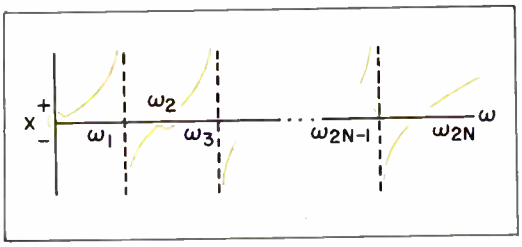


Figure 7. Reactance Curve for Case 1

Case 1: $A = j\omega H$.

An external zero at $\omega = 0$.
An external pole at $\omega \rightarrow \infty$.
The number of internal poles equals the number of internal zeros.

The graph of the impedance function for this case is shown in figure 7, and the function is represented by equation (14) below.

$$Z = j\omega H\,\frac{(\omega^2 - \omega_2^2)(\omega^2 - \omega_4^2) \ \ldots \ (\omega^2 - \omega_{2n}^2)}{(\omega^2 - \omega_1^2)(\omega^2 - \omega_3^2) \ \ldots \ (\omega^2 - \omega_{2n-1}^2)} \qquad (14)$$

It should be noted that the subscripts in equation (14) above represent increasing values of ω. Since a zero exists at the origin, the next point must be a pole (designated by ω_1). This is followed by a zero, ω_2. Thus the zeros are all even subscripts, and the poles are all odd subscripts. Since as $\omega \rightarrow \infty$, $Z \rightarrow \infty$, there is an external pole. The impedance curve shown in figure 7 therefore represents equation (14), and

a network which fulfills the specified conditions is illustrated in figure 8.

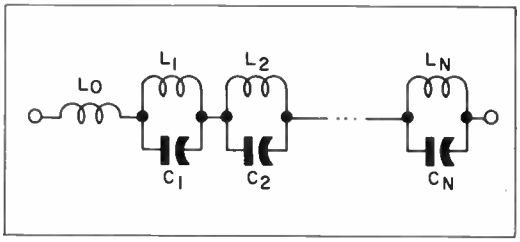


Figure 8. A Reactance Network Which Fulfills the Requirements of Case 1

Case 2: $A = j\omega H$.

A zero at $\omega = 0$.
A zero at $\omega \to \infty$.
The number of internal poles is one larger than the number of internal zeros.

In this case, equation (13) can be written as:

$$Z = j\omega H \frac{(\omega^2 - \omega_2^2)(\omega^2 - \omega_4^2)\cdots(\omega^2 - \omega_{2n}^2)}{(\omega^2 - \omega_1^2)(\omega^2 - \omega_3^2)\cdots(\omega^2 - \omega_{2n+1}^2)} \quad (15)$$

Equation (15) above, combined with the conditions for external poles and zeros, gives the impedance curve shown in figure 9, and a network which fulfills the specifications of the poles and zeros is shown in figure 10.

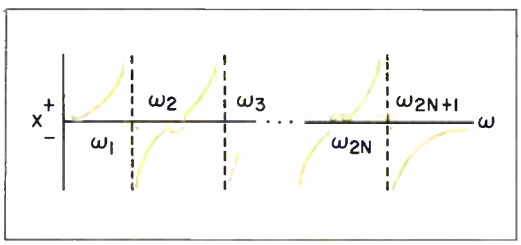


Figure 9. Reactance Curve for Case 2

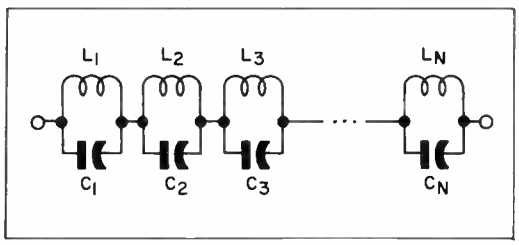


Figure 10. A Reactance Network Which Fulfills the Requirements of Case 2

Case 3: $A = \frac{H}{j\omega}$

A pole at $\omega = 0$.
A zero at $\omega \to \infty$.
The number of internal poles is equal to the number of internal zeros.

In this case, equation (13) can be written as:

$$Z = \frac{H}{j\omega} \frac{(\omega^2 - \omega_1^2)(\omega^2 - \omega_3^2)\cdots(\omega^2 - \omega_{2n-1}^2)}{(\omega^2 - \omega_2^2)(\omega^2 - \omega_4^2)\cdots(\omega^2 - \omega_{2n}^2)} \quad (16)$$

The curve representing the impedance function in this case is shown in figure 11, and a circuit which fulfills the specifications is shown in figure 12. Note

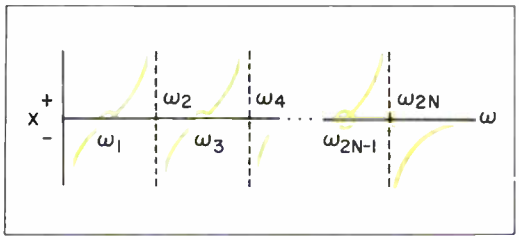


Figure 11. Reactance Curve for Case 3

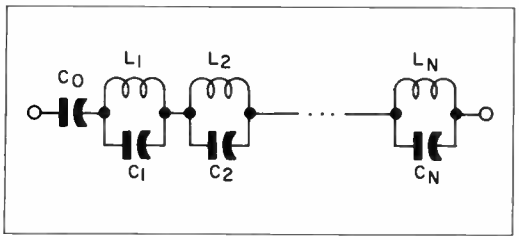


Figure 12. A Reactance Network Which Fulfills the Requirements of Case 3

that, as in the previous cases, the subscripts indicate increasing values of ω, and that, since there is a pole at $\omega = 0$, ω_1 represents the first zero.

Case 4: $A = \frac{H}{j\omega}$

A pole at $\omega = 0$.
A pole at $\omega \to \infty$.
The number of internal poles is one less than the number of internal zeros.

For this final case, equation (13) can

be written in the form:

$$Z = \frac{H}{j\omega} \frac{(\omega^2 - \omega_1^2)(\omega^2 - \omega_3^2) \ldots (\omega^2 - \omega_{2n+1}^2)}{(\omega^2 - \omega_2^2)(\omega^2 - \omega_4^2) \ldots (\omega^2 - \omega_{2n}^2)} \quad (17)$$

The curve representing this impedance function is given in figure 13, and a circuit which meets the specifications is shown in figure 14.

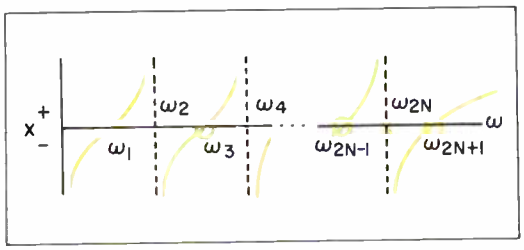


Figure 13. Reactance Curve for Case 4

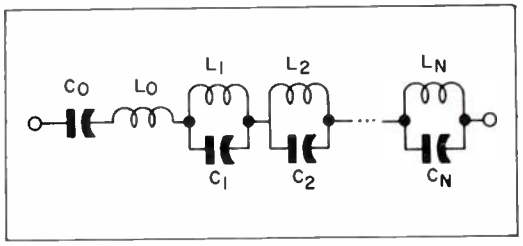


Figure 14. A Reactance Network Which Fulfills the Requirements of Case 4

In order to see the use of the pole and zero method and the Foster Reactance Theorem in network design, assume that it is necessary to design a network which has the characteristics listed below.

1. A pole at $\omega = 0$.
2. A zero at $\omega = \omega_1 = 2000$ radians/sec.
3. A pole at $\omega = \omega_2 = 6000$ radians/sec.
4. A zero at $\omega \to \infty$.
5. An inductive reactance of 1000 ohms $(0 + j\ 1000)$ at $\omega = 5000$ radians/sec.

In comparing these requirements with the various cases, it is seen that case 3 fits the requirements, and that equation (16) can therefore be used. However, equation (16) is not usable in the form given, but must be manipulated to solve for the required values. This manipulation is given below.

$$Z = \frac{H}{j\omega} \left[\frac{\omega^2 - \omega_1^2}{\omega^2 - \omega_2^2} \right]$$

Multiplying both numerator and denominator by ω gives

$$Z = \frac{H\omega}{j\omega^2} \left[\frac{\omega^2 - \omega_1^2}{\omega^2 - \omega_2^2} \right]$$

$$= \frac{H\omega}{j} \left[\frac{\omega^2 - \omega_1^2}{\omega^2(\omega^2 - \omega_2^2)} \right] \quad (18)$$

The term in the brackets can be solved as follows:

$$\frac{\omega^2 - \omega_1^2}{\omega^2(\omega^2 - \omega_2^2)} = \frac{K_1}{\omega^2} + \frac{K_2}{\omega^2 - \omega_2^2}$$

$$\omega^2 - \omega_1^2 = K_1(\omega^2 - \omega_2^2) + K_2\omega^2 \quad (19)$$

To evaluate K_1 and K_2 in equation (19) above, let $\omega = 0$. Equation (19) thus becomes

$$-\omega_1^2 = K_1(-\omega_2^2) + K_2(0)$$

and hence:

$$K_1 = \frac{\omega_1^2}{\omega_2^2} \quad (20)$$

If ω is made equal to ω_2, equation (19) becomes

$$\omega_2^2 - \omega_1^2 = K_1(0) + K_2\omega_2^2$$

and hence:

$$K_2 = \frac{\omega_2^2 - \omega_1^2}{\omega_2^2} \quad (21)$$

Substituting in equation (18) results in:

$$Z = \frac{H\omega}{j} \left[\frac{K_1}{\omega^2} + \frac{K_2}{\omega^2 - \omega_2^2} \right]$$

$$= \frac{HK_1}{j\omega} + \frac{H\omega K_2}{j(\omega^2 - \omega_2^2)}$$

This form of Z represents two elements in series, where the first element is given by

$$\frac{HK_1}{j\omega} \text{ (a capacitive term)}$$

and the second element is given by

$$\frac{H\omega K_2}{j(\omega^2 - \omega_2^2)}$$

This second element is an L-C parallel circuit.

The capacitive term can be evaluated by using the formula for capacitive reactance, as shown below.

$$X_c = \frac{1}{j\omega C_K} = \frac{HK_1}{j\omega}$$

Solving for C_K gives

$$C_K = \frac{1}{HK_1} \qquad (22)$$

The second element represents a parallel circuit, and therefore equation (5) may be used to give

$$Z = \frac{\omega}{jC_p}\left[\frac{1}{\omega^2 - \frac{1}{L_pC_p}}\right] = \frac{H\omega K_2}{j(\omega^2 - {\omega_2}^2)}$$

This may be solved for L_p and C_p to give

$$C_p = \frac{1}{HK_2} \qquad (23)$$

$$L_p = \frac{HK_2}{{\omega_2}^2} \qquad (24)$$

Since K_1 and K_2 are given in terms of the known quantities, ω_1 and ω_2, in equations (20) and (21), it is possible to solve for C_K, C_p, and L_p in terms of H as shown below.

$$K_1 = \frac{{\omega_1}^2}{{\omega_2}^2}$$

$$= \frac{(2 \times 10^3)^2}{(6 \times 10^3)^2}$$

$$= \frac{4 \times 10^6}{36 \times 10^6}$$

$$= \frac{1}{9}$$

$$K_2 = \frac{{\omega_2}^2 - {\omega_1}^2}{{\omega_2}^2}$$

$$= \frac{(6 \times 10^3)^2 - (2 \times 10^3)^2}{(6 \times 10^3)^2}$$

$$= \frac{(36 \times 10^6) - (4 \times 10^6)}{36 \times 10^6}$$

$$= \frac{32}{36}$$

$$= \frac{8}{9}$$

Since a given impedance (j 1000) is required at $\omega = 5000$, it is possible to solve for H by substitution in the equation:

$$Z = \left[\frac{H}{j\omega} \quad \frac{\omega^2 - {\omega_1}^2}{\omega^2 - {\omega_2}^2}\right]$$

Making the necessary substitutions gives

$$j\,1000 = \frac{H}{j\,5000}\left[\frac{(5 \times 10^3)^2 - (2 \times 10^3)^2}{(5 \times 10^3)^2 - (6 \times 10^3)^2}\right]$$

$$1000 = -\frac{H}{5000}\left(\frac{21 \times 10^6}{-11 \times 10^6}\right)$$

$$= \frac{21H}{55 \times 10^3}$$

Therefore:

$$H = \frac{55 \times 10^6}{21}$$

It is now possible to evaluate C_K, C_p, and L_p.

$$C_K = \frac{1}{HK_1}$$

$$= \frac{1}{\frac{55 \times 10^6}{21} \cdot \frac{1}{9}}$$

$$= 3.44 \times 10^{-6} \text{ farads}$$

$$= 3.44\ \mu f. \qquad (22)$$

$$C_p = \frac{1}{HK_2}$$

$$= \frac{1}{\frac{55}{21} \times 10^6 \times \frac{8}{9}}$$

$$= 0.43 \times 10^{-6} \text{ farads}$$

$$= 0.43\ \mu f. \qquad (23)$$

$$L_p = \frac{HK_2}{{\omega_2}^2}$$

$$= \frac{\frac{55}{21} \times 10^6 \times \frac{8}{9}}{(6 \times 10^3)^2}$$

$$= \frac{\frac{55}{21} \times \frac{8}{9} \times 10^6}{36 \times 10^6}$$

$$= \frac{55 \times 8}{21 \times 9 \times 36}$$

$$= 0.064 \text{ henry}$$

$$= 64 \text{ mh} \qquad (24)$$

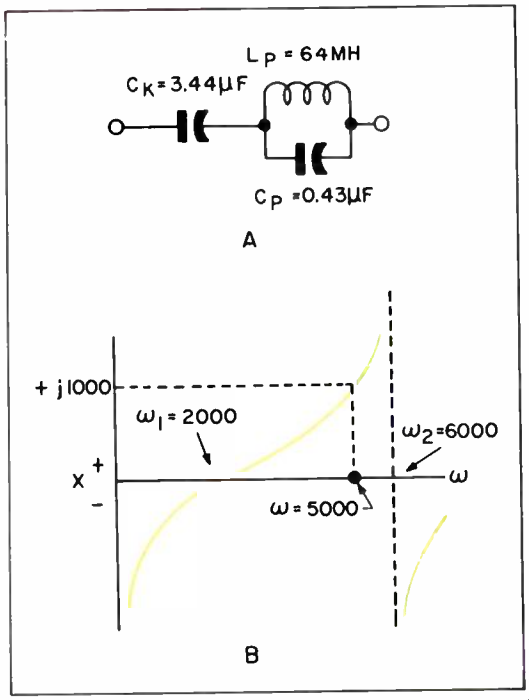


Figure 15. The Synthesized Network and Its Reactance Curve

The desired network is shown in part A of figure 15, and the impedance curve is shown in part B.

It can be seen that poles and zeros characterize the behavior of lossless two-terminal networks, and that one of four possible reactance curves can be obtained from any general network of this type. Associated with each of these curves is a series type of circuit which displays the desired impedance function. Since the series and parallel circuits are duals, it is, of course, also possible to design, for each series type of circuit, a parallel type of circuit which meets the conditions imposed by the Foster Reactance Theorem.

REFERENCES

1. *Communications Engineering*, by Everett and Anner, McGraw-Hill Book Co.
2. *General Network Analysis*, by LePage and Seeley, McGraw-Hill Book Co.
3. *Electrical Engineering Circuits*, by H. H. Skilling, John Wiley and Sons, Inc.

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