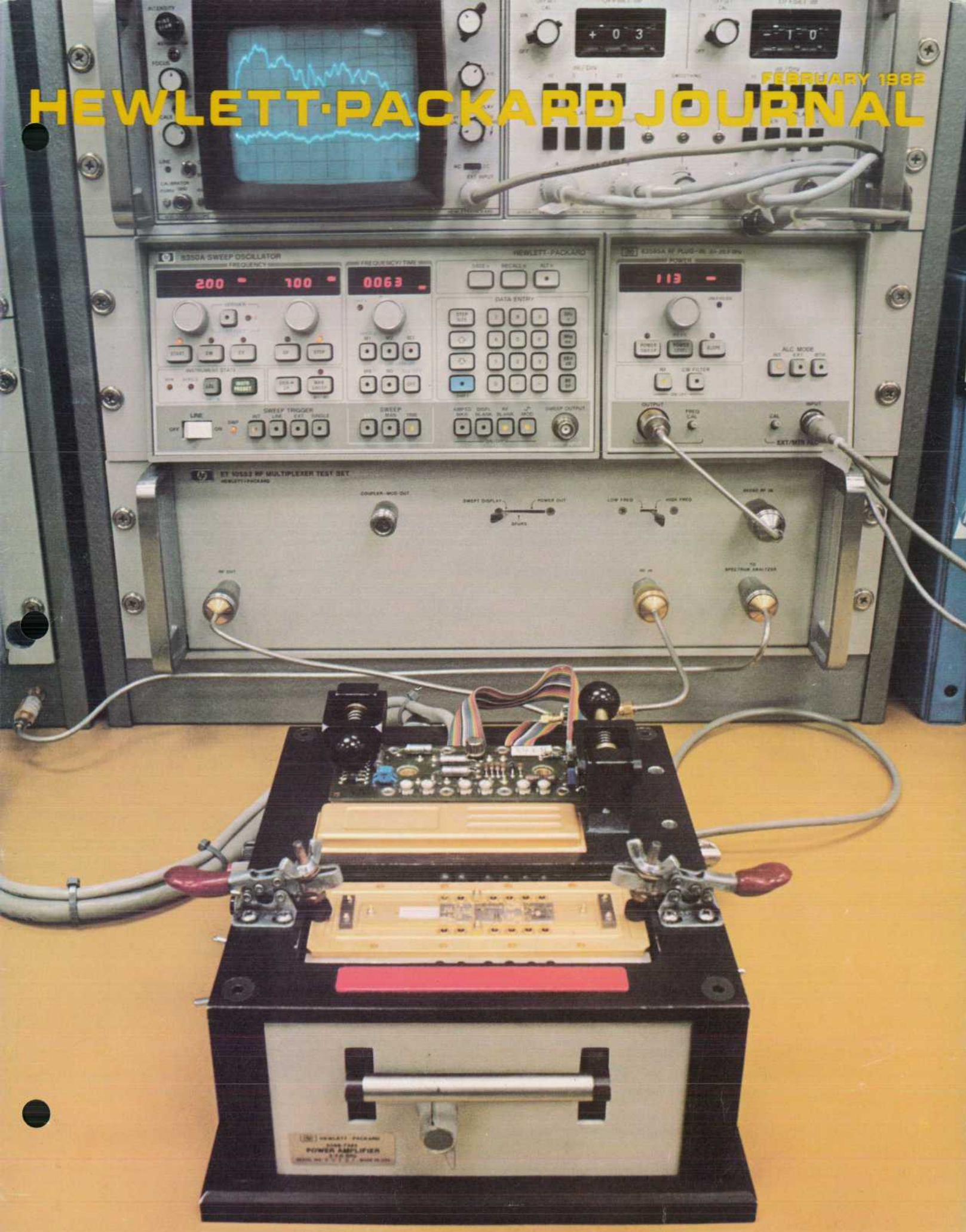
FEBRUARY 1982

HEWLETT-PACKARD JOURNAL



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Frequency response is an important characteristic of receivers, filters, amplifiers, stereo systems, and nearly every other kind of electronic device. With a voltage of a given frequency applied, what is the device's output voltage? How much current does it draw from the source? If you are designing a device, designing with a device, or testing a device, you need to know these things. Typically, the answers vary with the applied frequency; for example, an amplifier will have a different output for different input frequencies even if the input voltage doesn't vary. A device whose response is the same for all frequencies is said to be flat, meaning that it has a flat or nonvarying frequency response.

People used to measure frequency responses point by point: connect an oscillator to the device, tune the oscillator to some frequency, measure the device's response, write it down, tune the oscillator to another frequency, and repeat as necessary. Sweep oscillators, or sweepers, freed us from this drudgery. These signal sources tune themselves rapidly and automatically across a band of frequencies, making it possible to see a device's frequency response on an oscilloscope or plot it using an X-Y recorder. A good sweeper has to be able to sweep different frequency bands, depending on the application. Its own output voltage should be flat with frequency and accurately known, and its output frequency should be accurate, too. Over the years, sweeper performance in these areas has steadily improved as new technology has made higher performance possible.

Hewlett-Packard's latest microwave sweep oscillator, Model 8350A, is our cover subject this month. It sets new standards for frequency coverage and output accuracy. It's highly versatile, first because it's microprocessor-controlled, and second because it accepts a wide variety of plug-in modules for different frequency ranges and power levels. A major contribution is its complete programmability, which makes it suitable for use in automatic computer-controlled test systems. The article on page 3 describes the design of the 8350A mainframe and the article on page 11 discusses the 83500 Series plug-ins, a new group of high-performance plug-ins designed for the 8350A. Our cover photo shows the production test system for some of the microcircuits used in 83500 plug-ins; an 8350A Sweep Oscillator provides stimulus signals for the measurements.

When a person's heart stops beating normally and begins the ineffective quiver known as fibrillation, quick action is necessary to save the victim's life. The treatment of choice is usually the application of a high-voltage pulse to the victim's chest, causing a momentary current to pass through the heart. This is known as defibrillation, and the device that delivers the high-voltage pulse is known as a defibrillator. A problem with most defibrillators is that they don't tell the operator whether they've done their job, that is, how much energy they've actually delivered to the heart. HP's Model 78660A Defibrillator/Monitor not only displays and records actual delivered energy, but also records the date and time, the selected energy, the peak current during discharge, and patient impedance. An alarm light signals the operator if the paddles aren't making good contact, and an intelligent electrocardiograph records the patient's ECG waveform while rejecting noise and false beats. The 78660A records all of this information automatically, providing valuable medical and legal documentation of the procedure. Many of these features aren't found in the most sophisticated hospital defibrillators. Yet the 78660A is a compact, lightweight portable. The design story begins on page 22.

-R. P. Dolan

A Broadband, Fully Programmable Microwave Sweep Oscillator

Nearly thirty RF and microwave plug-in modules are available to tailor this high-performance swept signal source to a wide range of applications in the frequency range from 10 MHz to 26.5 GHz.

by Rolf Dalichow and Douglas E. Fullmer

IT IS SOMETIMES DIFFICULT to remember that there was a time when the microwave designer didn't have the help of a sweep oscillator and had to make measurements point-by-point. Once frequency tuning on a swept basis became available with the first mechanically driven sweepers, improvements came in a steady flow: electronic tuning of backward-wave oscillators (BWOs), solid-state sweepers using YIG-tuned oscillators, and broadband coverage by means of multiple oscillators or frequency multipliers and YIG-tuned filters.* Now a microprocessor-controlled, fully programmable sweeper, the HP Model 8350A Sweep Oscillator, Fig. 1, represents the state of the art in this field.

In addition to controllability and usability, the 8350A makes other substantial contributions through innovative RF and microwave design. These contributions are in areas considered important by microwave designers, such as frequency coverage—0.01 to 26.5 GHz in one plug-in (83595A), frequency accuracy—10 MHz at 20 GHz, and calibrated output power. Internal leveling holds output power constant within ±0.25 dB with a 2-GHz plug-in and ±1 dB with a 26.5-GHz plug-in (Fig. 2).

In the design of the 8350A, strong emphasis was placed on product continuity and the use of well proven design concepts, with advances made where significant improvements could be achieved. For example, the plug-in concept of earlier HP sweep oscillators has been retained (Fig. 3). The 8350A mainframe accepts high-performance 83500 Series plug-ins designed especially for it (see article, page 11). It also accepts older 86200 Series plug-ins with the 11869A Adapter, and gives the user nearly complete programmability of these plug-ins. As advances in RF, microwave, and millimetre-wave technology become available, it will be easy to upgrade an 8350A measurement system with a new plug-in. The basic control, programming, and power supply circuits reside in the mainframe while the circuits with the highest potential for improvement reside in the plug-in.

Great care was taken to make the mainframe/plug-in interface reliable and supportive of the performance of the instrument. Important power supplies use remote sensing, and the tuning and modulation voltages are connected via shielded cables. The firmware controlling the plug-in functions resides in the plug-in, so the system firmware is automatically updated when a plug-in with additional capabilities and sophistication is inserted.

An Approachable Instrument

For ease of use, the front panel is organized into blocks of associated functions (Fig. 1). Major parameters, such as start and stop frequencies, sweep time, and power level, have their own displays and knobs. The sensitivity of each knob adapts to its speed of rotation and to the range of values being modified. Parameter values can also be incremented or decremented with the step keys or entered on

*YIG = yttrium-iron-garnet, a ferrite material. See reference 1 for an explanation of YIG tuning.

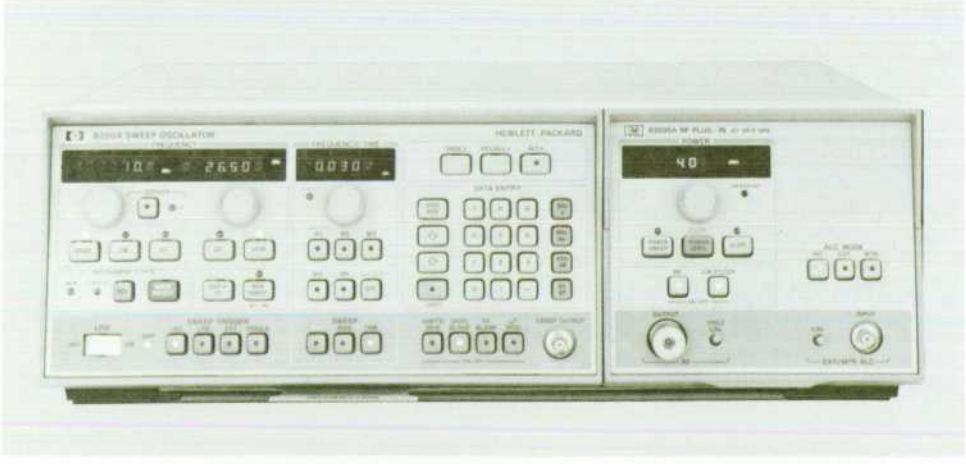


Fig. 1. *Model 8350A Sweep Oscillator is a fully programmable instrument that can accept various RF and microwave plug-in modules to provide broadband frequency sweeps (0.01 to 26.5 GHz with the 83595A RF Plug-in shown), calibrated output power, and high frequency accuracy (±10 MHz at 20 GHz).*

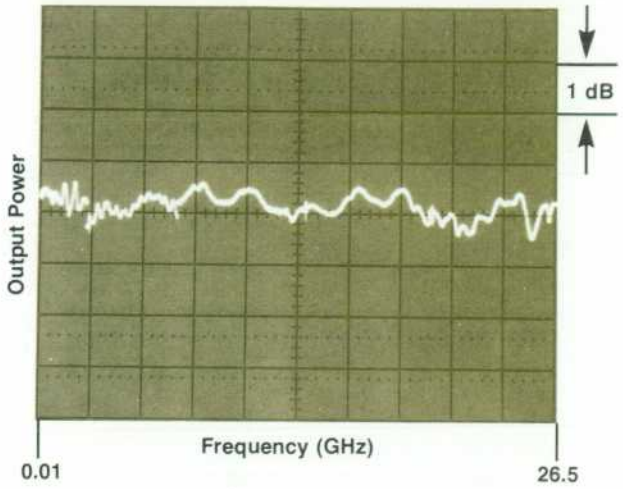


Fig. 2. *Internal leveling keeps 8350A/83595A output power constant within ±1 dB to 26.5 GHz.*

the numerical keyboard.

Functions are designed for ease of use. For example START/STOP and CF/ΔF aren't separate sets of sweep frequencies, but just two ways of displaying and entering the same sweep. Pressing **CF** or **ΔF** after the start and stop frequencies are entered displays the equivalent center frequency and span and allows modification of these parameters.

Five independent markers can be set to frequencies of interest and used to simplify microwave measurements. For example, the marker difference mode aids bandwidth measurements by displaying the difference in frequency between any two markers. The trace between the two markers is intensified (Fig. 4).

A second function, marker sweep, sets the endpoints of the sweep to marker 1 and marker 2 (Fig. 5). The resulting display is a more detailed view of some area of interest, such as the passband of a filter. A related function, marker to center frequency, positions the sweep about some point of interest identified by the marker.

Lastly, the sweep can be stopped momentarily at a marker while the frequency is measured by the HP 5343A Microwave Counter. Thus even while sweeping, a marker at 26.5 GHz can be determined within ±100 kHz.

Up to nine front-panel settings can be saved and recalled, either singly or in sequence. The memory is nonvolatile, so stored front-panel settings are retained even with the instrument turned off. A footswitch may be connected to a rear-panel connector to sequence settings in a hands-free production setup.

Device response in two independent frequency ranges may be observed "simultaneously" by using the alternate sweep feature (Fig. 6). At the end of each sweep, the 8350A switches between internal settings corresponding to two different front-panel settings. This allows, for example, adjustment of the passband of a filter while concurrently observing the effect on the filter's rejection band.

Second-Generation HP-IB Compatibility

All 8350A front-panel functions are programmable via the HP-IB,* a standard feature. The programming language uses easy-to-remember mnemonics and a straightforward numerical format (e.g., CW 7.55 GZ).

The HP-IB interface not only lets the user program every front-panel function, but also provides a number of special-purpose functions to aid remote operation. For example, a learn mode transfers the complete front-panel setting into the memory of a controller, where it can be stored on tape and later used to program the 8350A. This allows multiple manually entered test setups to be saved and recalled by means of a generalized program in the controller.

To give the user the ability to interact with the instrument in an automated test system or to document the present value of a parameter, the 8350A allows interrogation of any numeric function. For example, OPCF (output center frequency) outputs the center frequency to the controller in a human-readable form.

An HP-IB service request (SRQ) can alert the controller to a number of conditions in the 8350A. SRQs can be issued when a sweep ends, the RF output becomes unleveled, the airflow ceases, a self-test fails, an HP-IB syntax error is detected, or a numerical entry is out of bounds.

Mainframe Design

As a completely programmable mainframe for two

*The HP Interface Bus is HP's implementation of IEEE Standard 488-1978.

Fig. 3. *Two types of plug-ins can be used in the 8350A Sweep Oscillator mainframe. The 83500 Series (right) is a group of high-performance plug-ins designed specifically for the 8350A. Existing 86200 Series plug-ins (left) can be used with the 11869A Plug-in Adapter (rear portion of unit at left).*

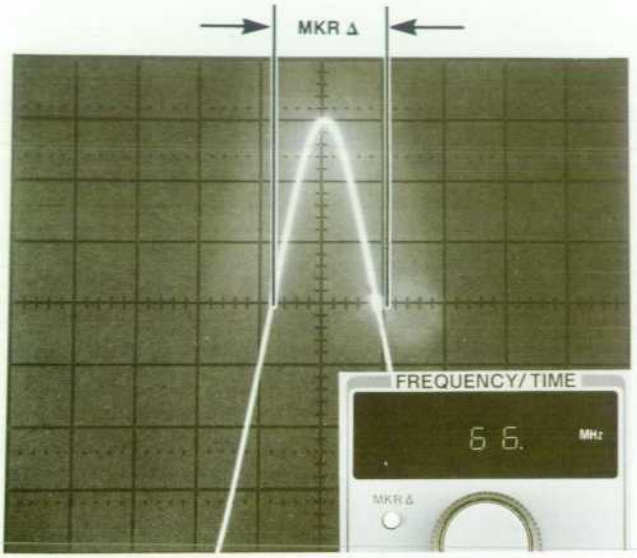


Fig. 4. *Five independent, continuously variable markers identify significant frequencies. The marker difference function simplifies frequency bandwidth measurements as shown here. The frequency difference between any two of the five markers is displayed.*

families of RF and microwave plug-ins, the 8350A is designed to meet a number of potentially conflicting objectives:

- Compatibility with existing and future plug-ins. The 8350A can be used with both the high-performance 83500 plug-ins and, through an adapter, the 86200 plug-ins. Generous power supply capacity is provided for future plug-ins.
- Controllability and usability via powerful but easy-to-use front-panel and HP-IB functions.
- Maximum performance with a minimum number of components. For example, one microprocessor controls both mainframe and plug-in.
- High reliability and serviceability. Generous airflow and extensive self-test routines are key contributions in this area.

Internally, the 8350A mainframe is organized into three sections (see Fig. 7): the instrument control section, the sweep, tuning and marker section, and the power supply section.

The microcomputer controls the sweep, tuning and marker section and interfaces with the front panel, the HP-IB, and the plug-in. To produce the tuning voltage for the plug-in, a fixed-amplitude ramp from the sweep generator is scaled and offset. Markers are generated by comparing the output of a DAC (digital-to-analog converter) to the sweep ramp. Voltages from regulated supplies in the mainframe are also used in the plug-in.

Instrument Control

One microprocessor controls both mainframe and plug-in. An HP-IB preprocessor integrated circuit simplifies the HP-IB interface. To reduce board count and increase reliability, the microprocessor, 2K bytes of CMOS RAM (complementary metal-oxide semiconductor random-access memory), and 32K bytes of read-only memory organized as four 64K-byte ROMs, are all on one board. A nickel-cadmium battery and an on-board charging circuit ensure nonvolatile storage of the instrument state in the CMOS RAM.

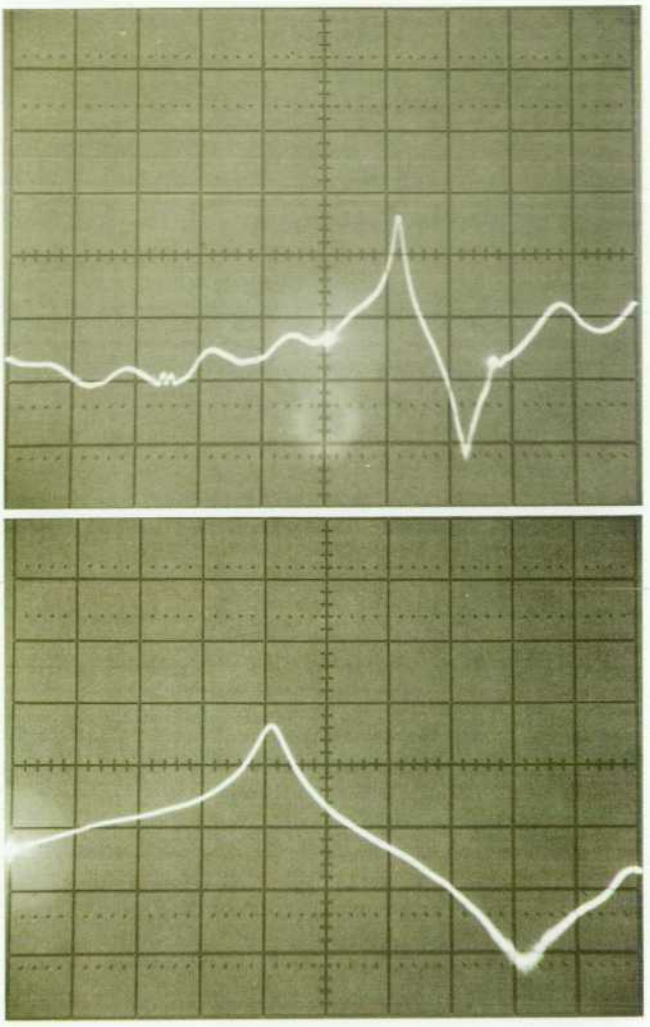


Fig. 5. *Marker sweep is useful for examining narrow responses in more detail. The 8350A sweeps only the span between markers 1 and 2.*

Instrument self-tests pinpoint failed components via either the numerical display or, if the front panel is inoperative, light-emitting diodes on the microcomputer board (see box, page 10).

Clock signals for both mainframe and plug-in are generated by a state machine. The state machine design insures that the address and data lines stay valid for 93 ns after the interface clock changes state, thus allowing ample time for address decoding.

Plug-in Interface

The 83500 Series plug-ins interface to the 8350A via a dedicated bus and an extensive software protocol. Programs in the plug-in's ROM are executed by the microprocessor in the mainframe. An address space of 10K bytes is provided for the plug-in: 8K bytes for firmware and 2K bytes for I/O.

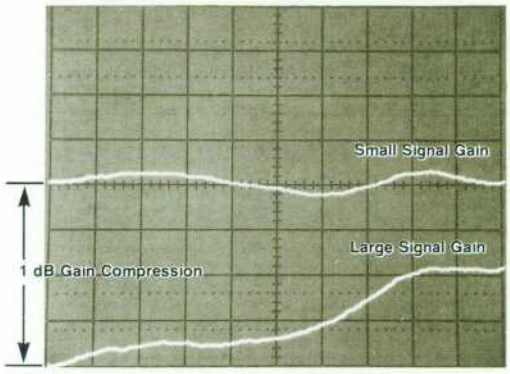


Fig. 6. *The alternate sweep function causes the 8350A to switch, on successive sweeps, between the current front-panel settings and any of nine front-panel states stored in memory. This makes it possible to observe a device's responses to two different stimulus conditions on the same display.*

In addition to data and address lines, the plug-in interface bus contains flag, interrupt, and hardwired control lines. Special attention was paid to minimizing bus transients that could cause errors on the bus lines. Ringing and crosstalk are reduced by reverse-terminating each bus driver with a 100Ω resistor. To reduce crosstalk further, each group of bus lines is separated from other groups by at least one ground line. Schmitt-trigger gates are used to sense the received signals.

Front-Panel Interfacing

Interrupts are generated by the front panel at a 1.6-kHz rate. The microprocessor refreshes one of the 15 display digits each time an interrupt is received, thus refreshing the entire front panel at a rate of about 100 Hz. Other front-panel tasks are performed at submultiples of the 1.6-kHz rate. These tasks and others described below take only a small percentage of the microprocessor's time.

The front-panel knobs function as rotary pulse generators (RPGs). In addition to scanning and debouncing the keyboard, the interrupt routine reads and resets the RPG counters at a 60-Hz rate. Counter overflow isn't possible at this rate, and the delay from the time a knob is turned to the time processing is initiated is less than 16 ms.

The count is proportional to the rate of rotation, so it can be used to index a table of rate-dependent knob sensitivities. The values in the table are chosen such that rapid rotation causes the entire range of the parameter to be covered in a few turns, while slow rotation results in fine adjustment. RPG and display resolutions are linked to hardware resolution, and display digits always increase or decrease monotonically when an RPG is turned.

Sweep Generation

A current-output DAC, a retrace current source, and an integrator are key components in the generation of the sweep waveform (Fig. 8). When the output of the integrator, a linear ramp, reaches +10.8 volts the retrace current source is switched on, forcing the ramp to reverse direction (Fig. 9). When the ramp falls to −0.9 volts, the retrace current source is turned off and the output of the integrator again ramps upward, completing the cycle. The sweep may be stopped by the plug-in (during bandcross, for example), or by an external input.

Sweep time is set by both the integrator capacitor and the DAC current. The 10,000:1 range of 10 ms to 100 seconds is covered by switching between two capacitors, 100:1 in value, and adjusting the DAC current over a 100:1 range.

When the sweep is stopped, the output of the operational amplifier jumps in voltage as the current through the on resistance of the analog switches is suddenly cut off. This voltage jump is eliminated by taking the output of the integrator directly from the capacitor via a high-impedence buffer.

Upper and lower ends of the sweep are clamped to precision voltage levels. YIG-tuned oscillator (YTO) settling occurs during the time the output of the integrator is clamped to zero volts. The lower clamp eases YTO delay compensation by starting the sweep with a maximally smooth function.

Forward sweep starts when the output of the integrator is −0.3 volts and ends when the upper clamp turns on at 10 volts. RF or Z-axis blanking is activated when not in forward sweep.

Sweep Scaling

To produce the tuning voltage, the sweep waveform is

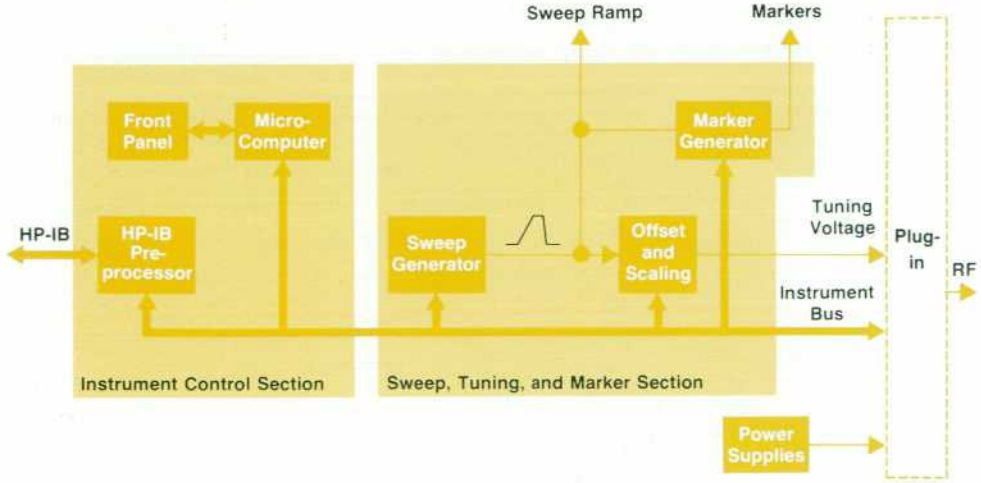


Fig. 7. *Block diagram of the 8350A Sweep Oscillator.*

A System-Oriented Instrument

The 8350A was designed to be used in systems. Therefore, all inputs and outputs necessary to synchronize and operate test systems are provided on BNC and multipin connectors. Both hardware and firmware were designed to make system applications of the instrument possible.

A simple example of an 8350A system is a master/slave configuration using two 8350As, making it possible to test mixers and receivers very efficiently. The frequency offset feature of the 8350A simplifies the setting of the two instruments' frequencies.

There is a powerful synergism between the HP 8350A, the HP 5343A Microwave Counter, and the HP 5344A Source Synchronizer. A two-wire interface allows measurement of start, stop, and marker frequencies with counter accuracy. The counter can receive the RF energy from the auxiliary output of the broadband plug-ins, thus eliminating any output power reduction caused by power splitters or couplers. With the HP 5344A and the HP 5343A, the sweeper can be part of a phase-locked system that allows CW and swept frequencies to be set with counter accuracy. Sweeps of up to 40 MHz are completely phase-locked, while wider sweeps use the "lock and roll" principle. In this mode, the start frequency is phase-locked and then, after achieving high accuracy, the frequency is swept in an analog fashion. All of the frequency controls are handled by the HP 5344A, which acts as an HP-IB controller.

Another measurement system employing the 8350A is the 8755P Automatic Scalar Network Analyzer. This system is controlled by an HP-85 Computer and operates from 0.04 to 18 GHz. Its amplitude resolution at 10 dB per division is 0.1 dB over the full range of the screen and 0.02 dB over a 40-dB range at the center of the screen.

The most economical way to perform phase and magnitude measurements at microwave frequencies is to use the HP 8408A Automatic Network Analyzer, Fig. 1, which also employs an HP 8350A as a source. This analyzer has a range from 0.05 to 18 GHz and an effective directivity greater than 40 dB.

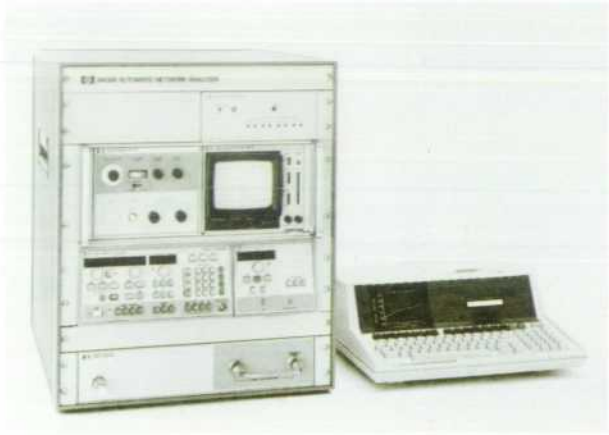


Fig. 1. *8408A Automatic Network Analyzer.*

Software available for the HP-85 Computer allows vector error-corrected measurements that eliminate all degradation of system performance because of imperfect adapters and cables. These nonideal but necessary pieces of hardware used to adapt the device under test to the measurement system normally drastically impair the performance of any otherwise well designed network analyzer.

Finally, the 8350A is used in the HP 8409C Automatic Network Analyzer. Besides the new sweeper, this extension of the well-known network analyzer family incorporates an HP 9845B Option 250 Desktop Computer and new accuracy enhancement software. The interface between the 8409C system and the sweeper is simplified and the software needed to program the source is greatly streamlined.

scaled by the ΔF DAC and the ΔF attenuators, then summed with the CW and vernier DACs (Fig. 10). Attenuating the output of the 10-bit ΔF DAC expands its 1,000:1 range to 64,000:1. The eight-bit vernier DAC covers ±2 least-significant bits of the 12-bit CW DAC, thus resolving 262,000 points per plug-in band.

A precision voltage reference, used in sweep generation and scaling, reduces noise by averaging the voltage of three Zener diodes. Since the noise contributions from the individual diodes are uncorrelated, the reference is only 58% as noisy as a single Zener diode.

Marker Generation

Markers are generated by comparing the sweep ramp to the output of a DAC (Fig. 11). Each time the comparator fires, a counter advances the address of the marker RAM, setting the DAC to the next marker-on or marker-off value. When the marker shown in the front-panel display is reached, a digital comparator turns on the active marker line. The active marker has enhanced brightness and the frequency at which it occurs can be measured with the 5343A Frequency Counter.

Since the marker is toggled each time the comparator fires, the RAM holds pairs of marker-on and marker-off positions. Marker positions are calculated from the start, stop, and marker frequencies, sorted, and then loaded into the marker RAM before the next sweep starts. The markers are normally one bit wide, 0.4% of the display screen. In marker difference mode, the entire trace between two markers is intensified by eliminating the first marker's off entry and the second marker's on entry.

Counter Interface

During the sweep, start, stop, or marker frequencies can be measured on the 5343A Frequency Counter. A user-selected pulse at the start of the sweep, the end of the sweep, or the active marker triggers the counter. The counter responds by stopping the sweep and counting the frequency, then releasing the sweep when the measurement is complete. While the frequency is being counted, the RF display is blanked and the internal 27-kHz modulation used by the 8755C Scalar Network Analyzer is disabled.

Other Interfaces

When an 8755C Scalar Network Analyzer is connected to an 8350A in alternate sweep mode, interface lines force the 8755C's channel 1 to display the normal sweep and channel 2 to display the background sweep. Separate sensitivities can be used for the two channels so that, for example, a broadband sweep at 10 dB per division can be alternated

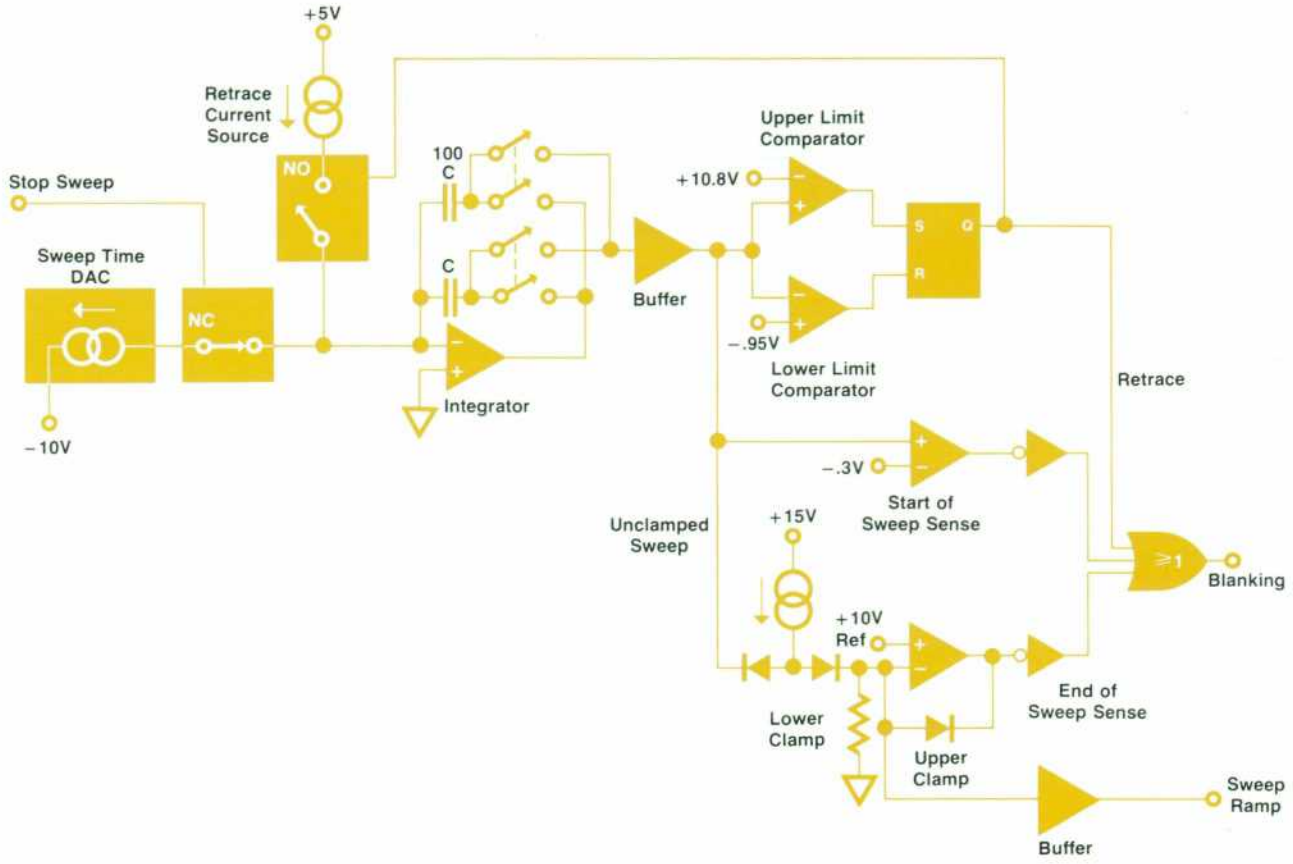


Fig. 8. *8350A sweep generation circuits.*

with a narrow sweep at 1 dB per division.

External sweep capability, along with the offset function, allows two 8350As to test mixers and receiver front ends. One sweeper acts as a master and externally sweeps the slave, which is offset in frequency by the desired intermediate frequency. The 8350A can also be used as an up-converter simulator for HP Microwave Link Analyzers such as the HP 3712A.

Rear-panel interface lines allow the 8350A to lift the pen or mute the response of an X-Y recorder, trigger an HP 8410C Microwave Network Analyzer, or indicate that the sweep is retracing. Other lines allow external instruments to trigger the sweep, create a marker, or blank the RF. Digital ground and a +5V output with 100 mA capacity are provided for custom interface circuitry.

Power Supplies

To handle the 86200 Series plug-ins, the 8350A provides +20V, −10V, and −40V, all remotely sensed and therefore unaffected by the voltage drop across wiring and connector resistance. The 8350A and the new 83500 Series plug-ins share a ±15V supply, but have separate high-current +5V supplies. Microcircuits in the new plug-ins also use +10V and unregulated +5V. All of the supplies are current-limited. Crowbars protect both plug-in and mainframe from expensive damage caused by power supply failure. If a monitor circuit detects that a supply has failed, an error message is written to the front-panel display.

Reliability of the 8350A power supplies is improved by a

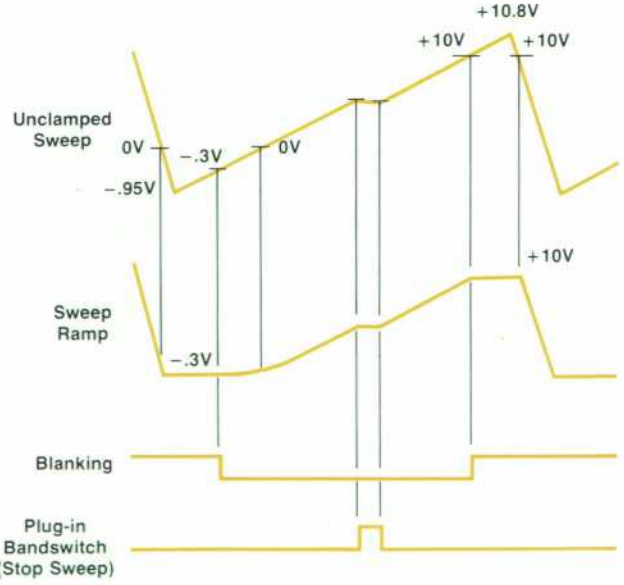


Fig. 9. *Sweep waveforms generated by the circuit of Fig. 8.*

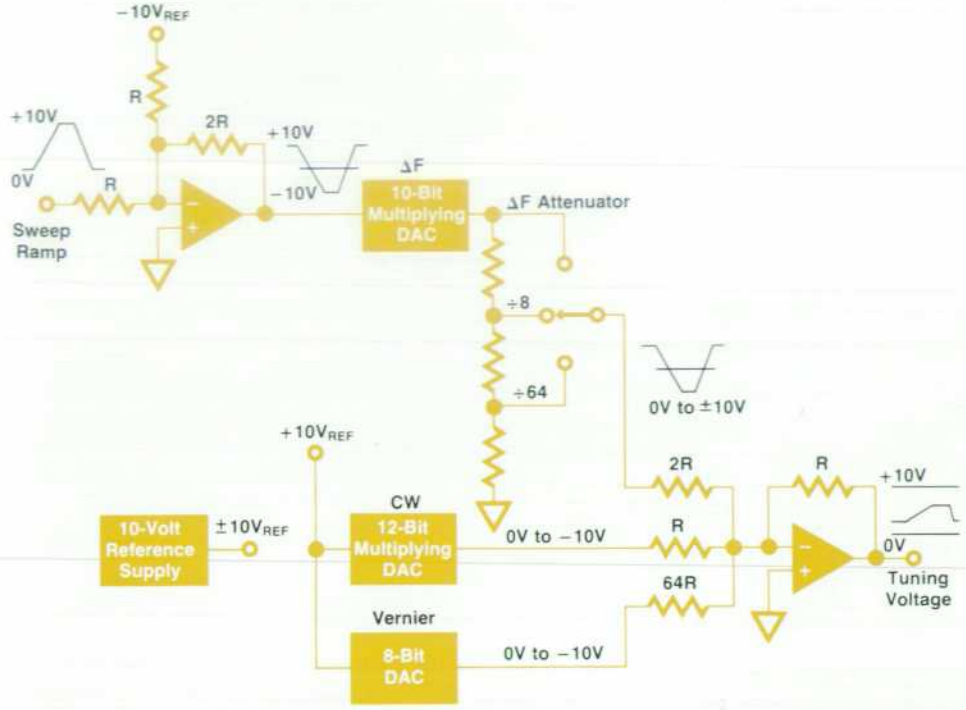


Fig. 10. *Sweep scaling and offset circuits condition the sweep ramp before it is sent to the plug-in.*

large heat sink. If the temperature of the heat sink exceeds a safe limit, a thermal switch removes line power.

Airflow

A generous flow of air minimizes temperature rise and further improves the reliability of both mainframe and plug-in. The front panel displays an error number if the airflow is impaired. Decreased airflow because of a clogged filter or blocked ventilation allows a heated transistor to increase in temperature, but has no affect on an unheated one. An airflow-monitoring comparator turns on, indicating insufficient airflow, when the forward voltages and hence the temperatures of a heated transistor and an unheated transistor differ by more than a preset limit (Fig. 12).

Acknowledgments

We would like to acknowledge the efforts and contributions of the many people who so effectively worked together to create the 8350A. The original concept was provided by Jack Dupré and received its initial support from Rit Keiter. Arlen Dethlefsen and Irv Hawley gave us the encouragement and support needed to successfully complete the project. Special thanks go to R.C. Ho for designing the power supply, the sweep generator and the HP-IB interface. The product design was well executed by Bill Misson and Bob F. Schaefer. Bill McDonald designed the self-test capability. Diane Heggie and Roy Church provided the industrial design effort. Gary Dooley and Jay Gregerson helped during the final design phase of the mainframe and the adapter and arranged a smooth transfer into production.

Reference

1. P.R. Hernday and C. Enlow, "A High-Performance 2-to-18-GHz Sweeper," Hewlett-Packard Journal, March 1975.

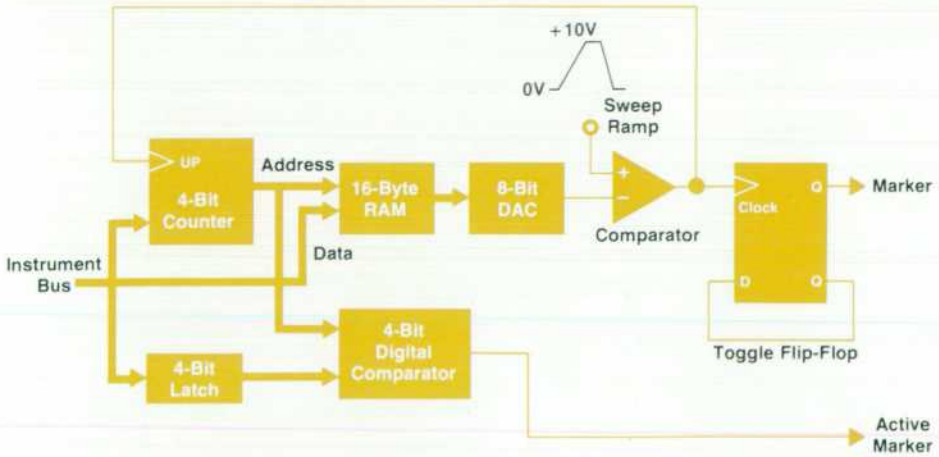


Fig. 11. *Markers are generated by comparing the sweep ramp to the output of a DAC that has been loaded with the next marker frequency from a 16-byte RAM.*

8350A Self-Test Capabilities

Microprocessor-controlled instruments present both difficulties and advantages in the areas of repair and maintenance. On one hand, a single defective component may render an instrument totally inoperative. On the other hand, self-tests can detect faulty components or sections of circuitry and operator-initiated tests can pinpoint the specific problem. Built-in test capabilities thus increase the usefulness of the instrument by building confidence and shortening the repair cycle.

When the 8350A is switched on or when the **PRESET** key is pressed, routines test the microprocessor, RAM, ROM, I/O buses, power supply, DACs and plug-in. If either the microcomputer board or the front panel fails a test, four LEDs on the microcomputer board indicate, in binary code, which component is defective. If RAM or ROM tests fail, the test program goes into an endless loop and does not proceed to routines that rely on the defective components.

If the microcomputer and front-panel tests pass, normal instrument operation resumes and error numbers are displayed on the front panel as well as on the error-indicator LEDs.

Each byte in RAM is tested without altering its contents. The byte is read, complemented and written back, then read again and EXCLUSIVE-ORed with the original. If the result is all ones, the byte is not defective and its original contents are restored. ROMs are tested by comparing a calculated checksum to a reference checksum in the self-test ROM.

The front-panel and instrument buses are tested by writing patterns into a latch, then reading and verifying the contents of the latch. Address lines on the instrument bus are tested by writing out a pair of complementary address patterns. A counter on the bus is incremented and decremented by the decoded patterns, after which the count is read and verified.

A checksum is performed on the plug-in's ROM. If the test isn't passed, the 8350A indicates a plug-in failure and defaults to an emulation of a 0-to-10-GHz plug-in.

Analog Tests

If the power supply voltages are found to be within limits, the DACs are checked by comparing their outputs. An analog switch allows the marker DAC to be compared to both the CW and sweep-time DACs.

During normal instrument operation, the power supply and the airflow are tested at ten-minute intervals.

User-Initiated Tests

Special tests can be run to isolate faulty components. If the self-test of the microprocessor fails or if faulty address decoding is suspected, the microprocessor can be forced to free-run. If the DAC tests fail, a rotating-1 exercise, specific to each DAC, allows a quick check using an oscilloscope.

For general testing, the user may read from or write to any RAM, ROM, or I/O location. For example, a rotating-1 pattern may be written to some location, such as a latch. An oscilloscope can then be used to trace the pattern from the microcomputer board through the bus and data buffer to the selected latch and any circuitry it drives.

-Bill McDonald

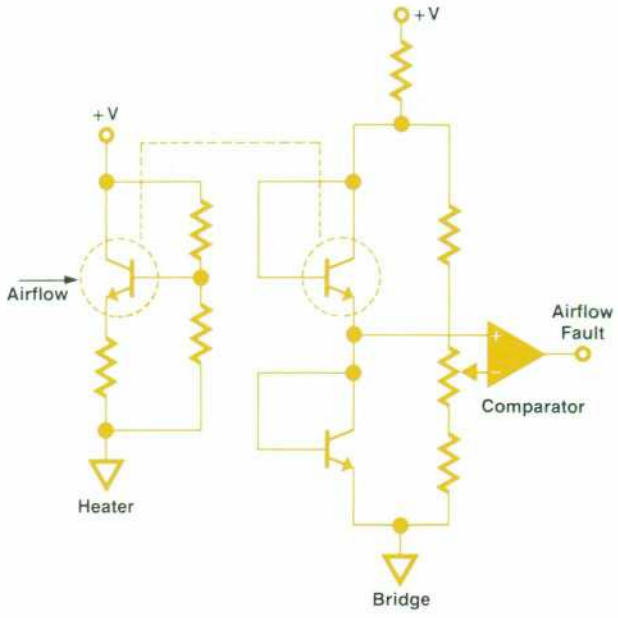


Fig. 12. *Airflow sensor detects decreased airflow by sensing a temperature difference between a heated transistor and an unheated one.*

Douglas E. Fullmer

Doug Fullmer graduated from the University of Washington with a BSEE degree and joined HP in 1975. He has contributed to the design of several 86200 Series sweeper plug-ins, had overall responsibility for 8350A firmware, and designed the 8350A microcomputer and front-panel boards. In June he will receive his MSEE degree from Stanford University. Born in Seattle, Washington, Doug is married and lives in Santa Rosa, California. His leisure activities include gardening, hiking, swimming, home projects, and learning about history, anthropology, and animal behavior.

Rolf Dalichow

Rolf Dalichow was born in Braunschweig, Germany and received his Ing. Grad. degree from the Staatliche Ingenieurschule Giessen. He joined HP in 1973 with 12 years' experience in hybrid RF circuits and communications transmitters in Berlin and the U.S.A. He has served as project manager for the 8350A Sweep Oscillator and as a project leader for the 8505A Network Analyzer. He is named as a co-inventor on a frequency counter patent. Rolf is married, has two children, and lives in Santa Rosa, California. He enjoys backpacking and is in the startup phase of building a new house for himself and his family.

A New Series of Programmable Sweep Oscillator Plug-ins

by Gary W. Holmlund, Glenn E. Elmore, and Duaine C. Wood

AS TEST SYSTEMS have become more automated to increase their efficiency, a need has arisen for a new generation of swept signal sources that are completely programmable. The 83500 Series plug-ins for the 8350A Sweep Oscillator are designed to meet that need.

In the design of a new series of plug-in swept signal sources, several objectives needed to be met:

- Programmability of all plug-in functions
- Wide frequency coverage
- Improved frequency accuracy
- Calibrated output power.

Table I lists the plug-ins in the 83500 Series along with their frequency ranges and power output levels. Fig. 1 shows representative plug-ins in the series and Fig. 2 shows the general block diagram of an 83500 Series plug-in. The front panel of each plug-in contains controls that affect RF output power and the power leveling mode. All front-panel settings can be saved and recalled in any of the 8350A's nine save/recall registers. Any two settings can be alternated in the alternate sweep mode. Each plug-in has a keyboard/display processor that refreshes the front-panel power level display and enters keys as they are pushed.

Table I

Model	Frequency (GHz)	Power Out (mW)
83522A	0.01-2.4	20
83525A	0.01-8.4	20
83540A	2-8.4	40
83545A	5.9-12.4	50
83570A	18-26.5	10
83590A	2-20	10
83592A	0.01-20	10
83594A	2-26.5	2.5**
83595A	0.01-26.5	2.5**

**10 mW below 20 GHz

On most plug-ins, the calibrated power level is adjustable over a 15-dB range. It can be set by keyboard entry, rotary pulse generator, step up and down keys, and the HP-IB.* With the addition of an optional 70-dB attenuator (55 dB on the 83594A and 83595A) the power level can be adjusted over an 85-dB range.

A slope adjustment allows the user to compensate for attenuation in cables, connectors or other hardware that increases with frequency. The adjustment causes the plug-in to increase power output as frequency increases. This feature can also be used with test sets in network analyzers so that the device under test has nearly constant incident power in spite of frequency-dependent losses between it and the sweeper. This is particularly important when measuring active devices at higher power levels.

The power sweep mode is useful for measuring the compression points of amplifiers. It is used to sweep the power level at a single frequency to measure the gain of an amplifier as a function of input power level. When used with the 8755C Scalar Network Analyzer, the horizonal scale is calibrated in input power level to the device under test. The vertical scale can be adjusted to display the gain of the device. The 1-dB compression point can then be read directly from the display. The step keys may be used to step the measurement frequency up or down so that compression level information can be measured as a function of frequency.

The user also has the ability to alternate the power between two different levels as the oscillator sweeps. This feature can also be used to measure an amplifier's performance. For example, one sweep can be set to measure the small signal gain of the amplifier while the power level in the second sweep is adjusted to a given compression point. This allows simultaneous observation of the small and large-signal performance.

*HP-IB is Hewlett-Packard's implementation of IEEE Standard 488-1978.

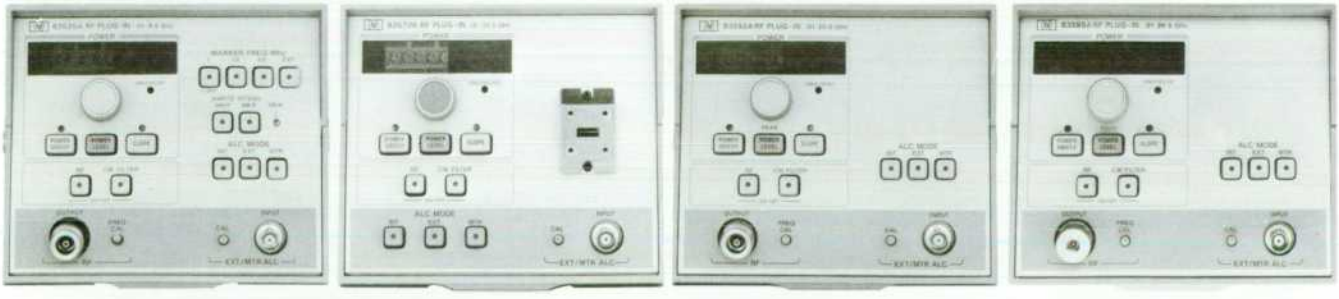


Fig. 1. *83500 Series plug-ins for the 8350A Sweep Oscillator span the frequency range from 0.01 to 26.5 GHz.*

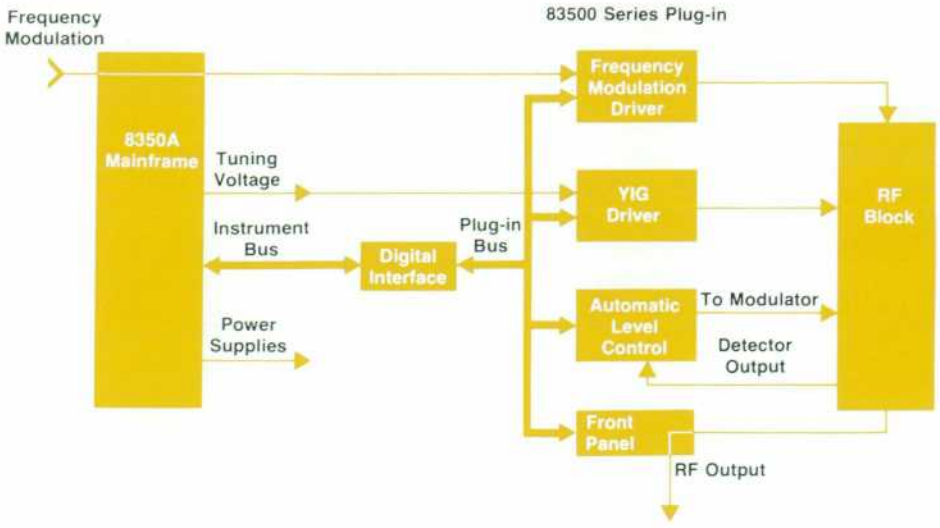


Fig. 2. *General block diagram of an 83500 Series plug-in.*

The automatic level control (ALC) has three modes of operation. Internal leveling uses the internal coupler and detector to measure the power level at the output of the instrument and hold it at a specified power level. The external leveling mode is similar but uses an external coupler and detector to measure the output power. The external **CAL** adjustment on the front panel adjusts the power level out of the coupler to agree with the power displayed by the plug-in. The power meter leveling mode uses an HP 432A/B/C Power Meter to measure and control the output power.

RF Designs

Fig. 3 is the RF block diagram of the 83525A plug-in. This plug-in is a combination of the 83522A (0.01-2.4 GHz) and the 83540A (2-8.4 GHz). The high band of the 83525A is formed by the YIG-tuned oscillator, the modulator/amplifier, two PIN diode switches, and a coupler/detector. If the two PIN diode switches are removed, the remaining components form the RF block for the 83540A. The YIG-tuned oscillator, PIN diode switch, modulator-mixer, amplifier, coupler/detector, and PIN diode switch form the low-band block. If the PIN diode switches are removed the 83522A RF block diagram remains. When sweeping the full frequency range, the 83525A first sweeps the low band from 0.01 to 2.05 GHz. Then the PIN diode switches change to the high band, which sweeps from 2.05 to 8.4 GHz.

The block diagram of the 83570A (18-26.5 GHz) plug-in is shown in Fig. 4. The YIG-tuned oscillator operates over a frequency range of 9.0 to 13.25 GHz and drives the frequency doubler (see page 17), which delivers 10 mW output power over the 18-to-26.5-GHz range. The output port is a WR 42 waveguide which provides a reliable connection in this frequency range and assists in the reduction of fundamental feedthrough. An auxiliary output allows the use of equipment in the 9-to-13.25-GHz range, thus eliminating, for example, the need of an 18-to-26.5-GHz frequency counter. The output power is internally leveled and is adjustable and HP-IB programmable over a 10-dB range.

The 83545A plug-in covers the 5.9-to-12.4-GHz range. It consists of a FET YIG-tuned oscillator and a power amplifier capable of delivering 50 mW of output power. An optional step attenuator together with the ALC circuitry provides a calibrated output power range of 84 dB.

Fig. 5 is the RF block diagram of the 83595A (0.01-26.5

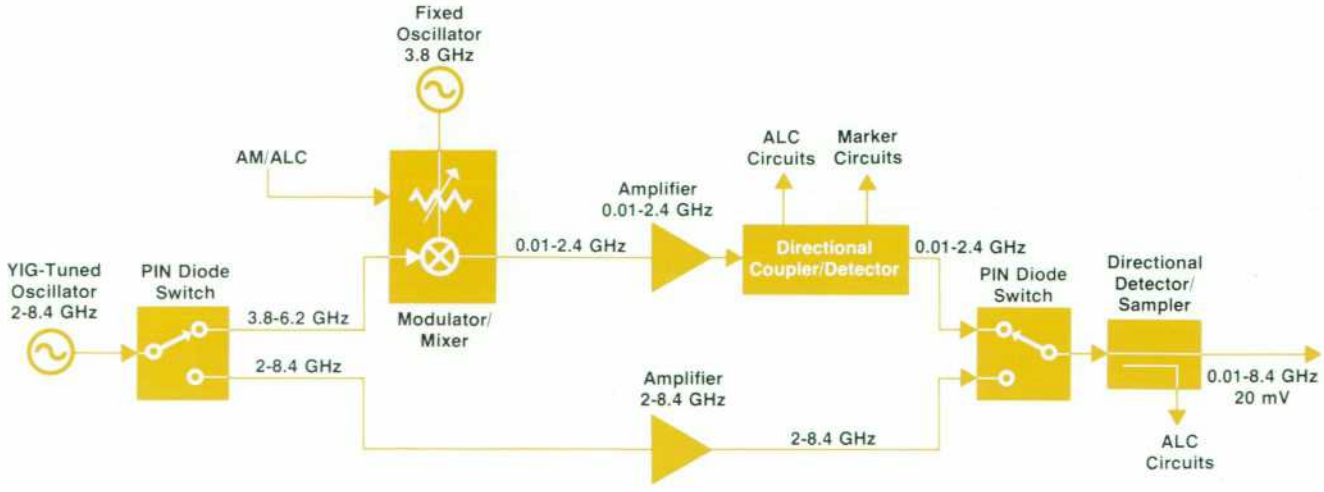


Fig. 3. *Block diagram of the 83525A 0.01-to-8.4-GHz plug-in. This plug-in is a combination of the 83522A 0.01-to-2.4-GHz plug-in and the 83540A 2-to-8.4-GHz plug-in.*

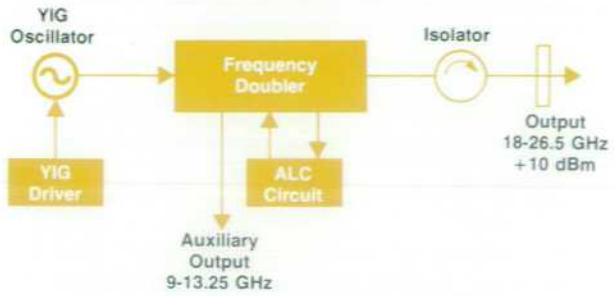


Fig. 4. *Block diagram of the 83570A 18-to-26.5-GHz plug-in.*

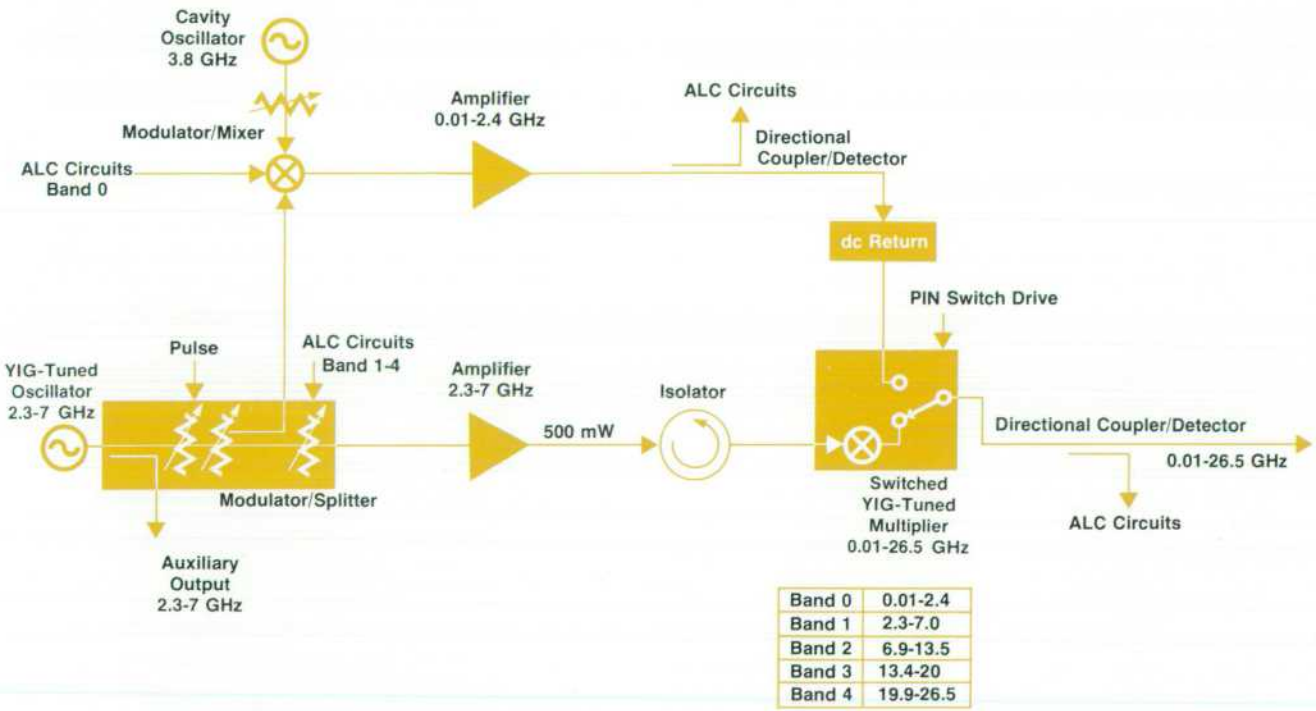
GHz). The top of the diagram shows the low band (0.01-2.4 GHz). It is very similar to the low band of the 83525A except that the modulator-splitter replaces one PIN diode switch and the switched YIG-tuned multiplier (SYTM) replaces the other PIN diode switch. In the high bands the RF from the YIG-tuned oscillator goes through the modulator/splitter to the power amplifier. It is amplified to 500 milliwatts and goes to the high-band port of the SYTM. The SYTM generates harmonics of the signal and tunes out all but the desired harmonic (see page 15). The 83594A (2-26.5 GHz) is made by deleting the low-band components and changing the modulator-splitter to a simple modulator. The 83592A (0.01-20 GHz) and 83590A (2-20 GHz) are similar to the 83595A and 83594A, respectively, but with the RF components operating only to 20 GHz.

Microprocessor Control of Plug-ins

To the microprocessor, which is in the 8350A mainframe, the plug-in looks like auxiliary read-only memory and input/output space. Address, data, and control lines are brought from the mainframe to the plug-in. Addresses are decoded in the mainframe so that 8K bytes of ROM and 2K bytes of I/O are available in the plug-in. Fig. 6 is a block diagram of the digital control section of the plug-ins.

The sweep oscillator interface consists of buffers that receive the address, data, and control signals from the mainframe. These signals are sent to ROM, interrupt control, or the plug-in interface depending on the address. If the signals are sent to the plug-in interface they go to other control boards of the plug-in (i.e., front panel, YIG control, frequency modulation, or automatic power level control boards).

The interrupt control section can generate interrupts to get the processor's attention. The interrupts can come from other boards of the plug-in or from timers within the interrupt control block. Interrupts that come from other boards generally occur at the beginning or end of a sweep or at the bandswitch of a multiple-band plug-in. At bandswitch, frequency gains and offsets are changed to cause the plug-in to sweep the next band. The timers are used only on the multiple-band plug-ins. After the band number is switched during a sequential sweep, the timers are used to control the time spent waiting for the frequency to settle. The 200-kHz clock drives the timers and the keyboard/display processor on the front panel.



Band 0	0.01-2.4
Band 1	2.3-7.0
Band 2	6.9-13.5
Band 3	13.4-20
Band 4	19.9-26.5

Fig. 5. *Block diagram of the 83595A 0.01-to-26.5-GHz plug-in. The 83594A 2-to-26.5-GHz plug-in is made by deleting the low-frequency section. The 83592A (0.01-20 GHz) and the 83590A (2-20 GHz) are similar, but use RF components designed to operate to only 20 GHz.*

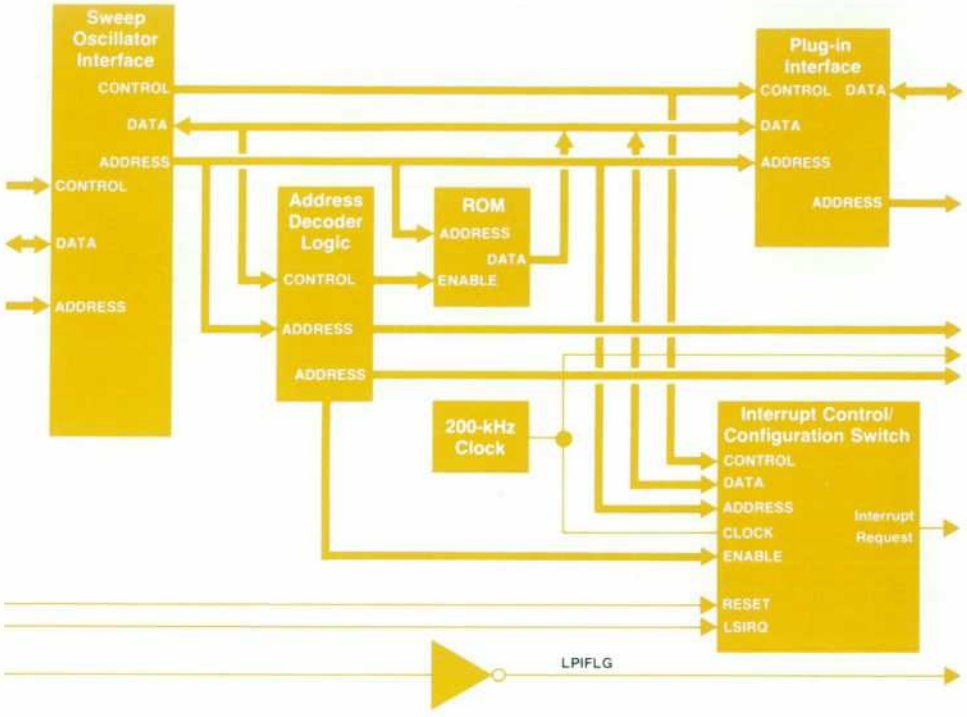


Fig. 6. *Digital control section of the 83500 Series plug-ins.*

The configuration switch is a set of eight switches that can be used to control the state of the plug-in at power-up. Among other things, the switches tell the firmware which model plug-in is present, whether the attentuator option is present, and the FM sensitivity.

The plug-in firmware contains the routines to control the plug-in from front-panel inputs and HP-IB commands. An HP-IB controller can read power level, slope, and power

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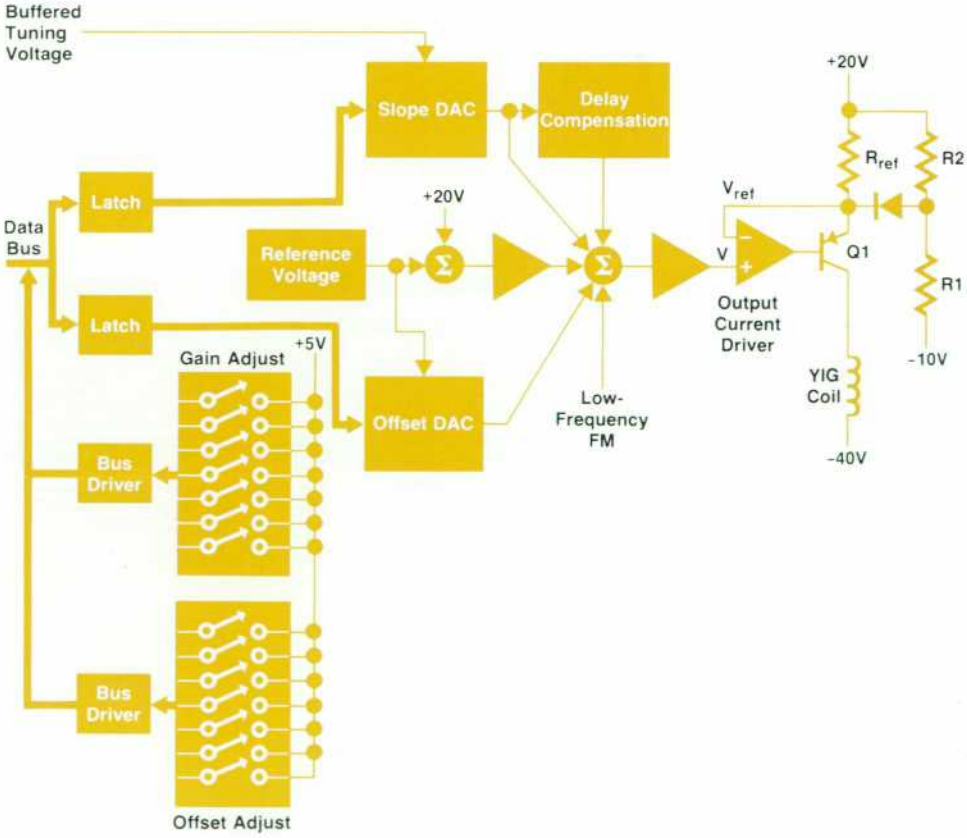

Fig. 7. *83500 YIG driver converts the tuning voltage received from the mainframe to the correct magnet current for the plug-in's YIG-tuned oscillator or multiplier.*

A Switched YIG-Tuned Multiplier Covering 0.01 to 26.5 GHz

A new frequency multiplier capable of producing output frequencies from 0.01 to 26.5 GHz was developed for the wideband 83590-Series plug-ins for the 8350A Sweep Oscillator. The new multiplier is tuned by means of a YIG (yttrium-iron-garnet) sphere and is called a switched YIG-tuned multiplier, or SYTM. It has two inputs: 0.01 to 2.4 GHz, which is switched to the output bypassing the YIG filter, and 2.4-7.0 GHz, which is multiplied by 1, 2, 3 and 4, filtered, and summed into the same output path. Because of the wide tuning range, the electrical, mechanical, and magnetic designs had to overcome significant challenges to maintain low cost and high production yields, yet achieve state-of-the-art performance.

The SYTM is constructed on a single 0.25-mm sapphire substrate containing bias circuitry, impedance matching circuits, a step recovery diode, the YIG filter, and a PIN diode switch (see Figs. 1 and 2). Substrate temperature is maintained at 85°C with a heater control loop consisting of two load resistors and a thermistor sensor on the substrate. Band 0 input is applied to port 1, which is connected to the output coax by means of the output coupling loop of the YIG filter. During Band 0 operation, the PIN diode is reverse biased, thus minimizing losses. Typical insertion loss in this band is less than 1 dB.

In the frequency range 2.0 to 26.5 GHz, a maximum input of +25.5 dBm is applied to port 2 of the SYTM. In band 1, this signal passes through the impulse generator including the step recovery diode with little attenuation, since the diode is heavily forward biased. As the input sweeps from 2.4 to 7 GHz, the YIG filter is tuned to the same frequency, thereby coupling the input signal to the output structure. The PIN diode switch is also turned on, providing the ground return for the output coupling loop of the YIG filter.

For bands 2, 3 and 4 the step recovery diode is actively biased so that during one half of the input RF cycle the diode depletion layer stores charge. As the input polarity reverses, the diode current reverses, sweeping out the stored energy. By adjusting the bias so that the remainder of the energy is depleted at the maximum of the input current, an impulse rich in harmonics is produced. The YIG filter is tuned to the desired harmonic and couples that frequency to the output.

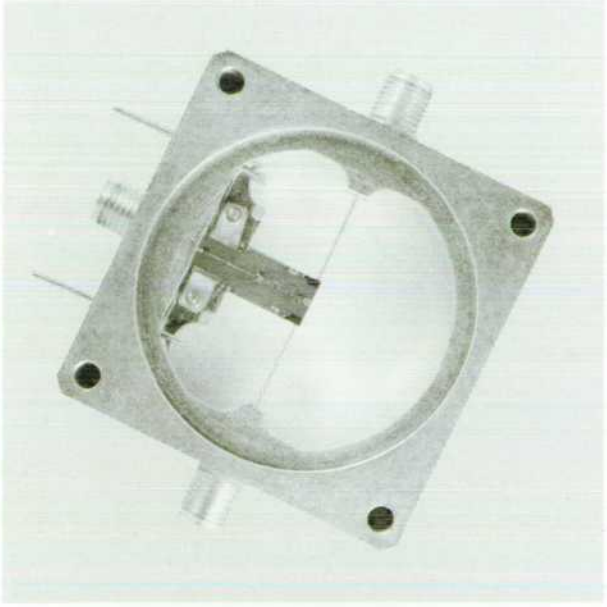

Fig. 1. *Switched YIG-tuned multiplier (SYTM) produces output frequencies from 0.01 to 26.5 GHz.*

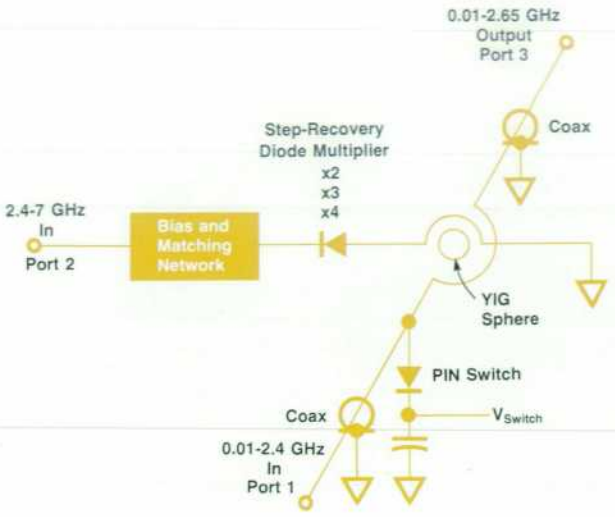

Fig. 2. *Equivalent circuit of the SYTM.*

Tuning the filter to 26.5 GHz required a new magnetic design, capable of producing a 10,000-gauss magnetic field in the 1.27-mm air gap containing the YIG sphere. The magnet pole tips are made of two materials, one of high permeability and the other capable of handling high flux densities without saturation. By adjusting the ratio of the materials, the temperature coefficients are minimized while reducing the hysteresis to approximately 15 MHz for a ±12-GHz tuning change. A linearity error of less than 3% between bands is achieved.

The YIG filter is a single 0.66-mm sphere mounted near the temperature-compensated axis, between the ⟨100⟩ and ⟨110⟩ axes.[1] This position was found empirically to give the best temperature stability with satisfactory insertion loss. Typical filter 1-dB bandwidth is 25 MHz from 2 to 20 GHz and 35 MHz from 20 to 26.5 GHz. Passband modes are less than 0.5 dB when tuned over the complete frequency range. Typical suppression of unwanted harmonics is 35 dBc.

Acknowledgments

The majority of the electrical design was done by Ganesh Basawapatna. Bob Jewett invented the PIN switch concept and contributed to the electrical design. Lee Olmstead produced the mechanical design and with Steve Sparks developed the magnet.

-Lynn Rhymes

Reference

1. G.L. Matthaei, L. Young, and E.M.T. Jones, "Microwave Filters, Impedance Matching Networks, and Coupling Structures," Artech House Books, 1980 (Reprint of McGraw-Hill Book Co. Edition, 1964), Sec. 17.05.

sweep settings. Plug-in front-panel conditions are saved and recalled by the plug-in firmware, which also contains self-test routines that check the state of the plug-in at power-up and routines to check the front panel for invalid operation. All digital-to-analog converters (DACs) in the plug-in can be checked for valid operation with a series of operator-initiated tests.

YIG Coil Drivers

The technique for converting the tuning voltage received from the mainframe to the correct YTO or SYTM magnet current is the same in all 83500 Series plug-ins. Since the tuning voltage is defined to be 0 to 10V for any complete frequency band regardless of its length, the tuning sensitivity (Hz/volt) can vary depending on the particular frequency band. One of the primary functions, therefore, of the YTO and SYTM coil drivers is to scale the tuning voltage in each band to create a constant-sensitivity ramp. In addition, the driver must add to that ramp an offset that tunes the YTO or SYTM magnet to the start frequency of each band when the input tuning voltage is 0V. Finally, it must convert the resulting voltage to the required magnet current, thus tuning the YTO or SYTM across the desired frequency range. Fig. 7 is a block diagram of the YIG driver.

The first two driver functions are accomplished using multiplying DACs. One DAC scales the tuning voltage and the other scales a precision −10.000V reference voltage. The outputs of the two multiplying DACs are summed and sent to the output current driver which performs the third function. The digital scale factors for each band are stored in the plug-in ROM and the DACs are updated whenever the plug-in changes bands. This results in greatly increased flexibility over previous plug-in YIG driver designs which required custom precision resistors for each separate frequency band. By making the drivers programmable, it was possible to use identical driver boards for an entire family of plug-ins, thus reducing inventories and simplifying service.

Programmability also realizes improvements in another key area: instrument adjustment and calibration. Because YIG magnet sensitivities can vary over a significant range, previous plug-in YIG drivers required gain and offset potentiometers for each band and factory-selected resistors to adjust for these variations. For a multiband plug-in such as the 83595A, which has five frequency bands and two driver boards (one for the YTO and one for the SYTM), a total of nineteen pots, together with their associated custom-value precision resistors, would be required to make the necessary offset and slope adjustments. (The SYTM is not swept in the low band, so only an offset adjustment is needed in that band.) Since potentiometers degrade both temperature performance and reliability, a reduction in their number was considered very desirable. Thirteen potentiometers were eliminated by using the slope and offset DACs as digital potentiometers. By modifying the slope and offset DAC scale factors in firmware, adjustments for variations in YIG magnet sensitivities can be made over a relatively wide range with no sacrifice in performance or reliability. Furthermore, since the tuning is linear, knowing the required offset and slope corrections in any one band allows computation of the required corrections in every other band. Thus, by calibrating the beginning and end frequencies of one band in the 83595A, for example, all five bands can be calibrated simultaneously. For convenience, a calibrate mode can be entered by using the **SHIFT** key on the mainframe which allows adjustment of the offset and slope

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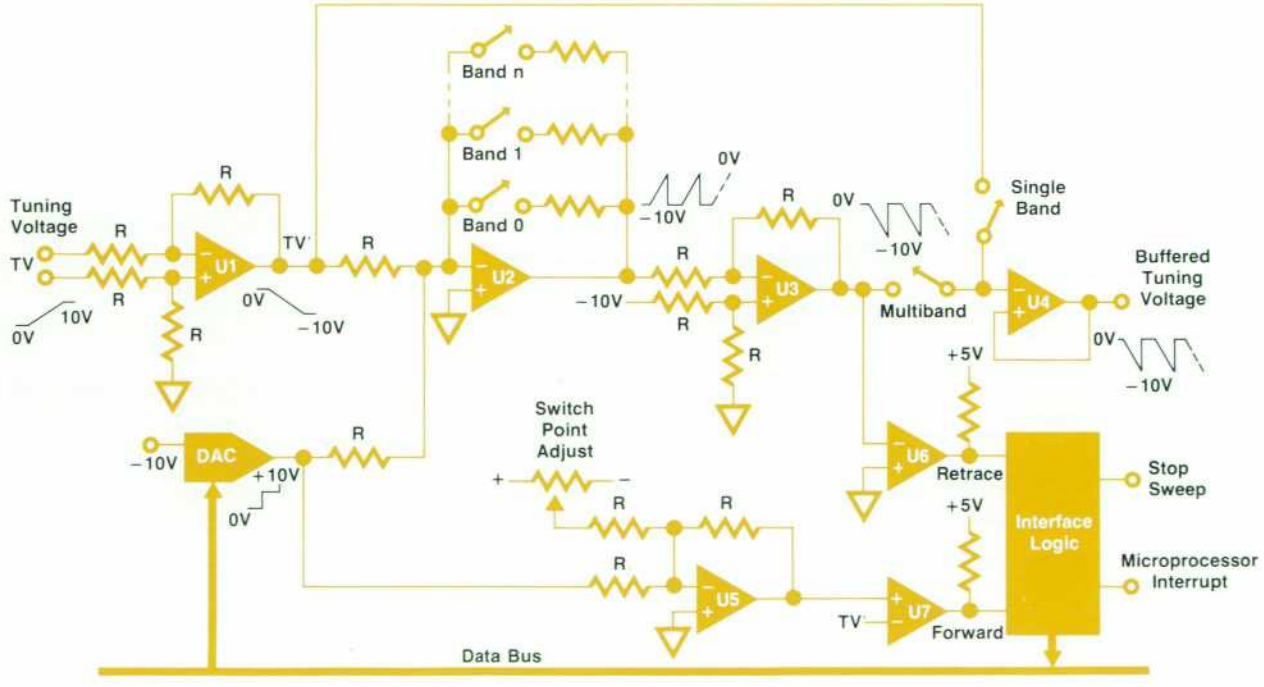

Fig. 8. *Plug-ins capable of very wide sweeps actually sweep several individual frequency bands in sequence. The additional circuitry required to do this is shown here.*

A Frequency Doubler with High Output Power from 18 to 26.5 GHz

One of the plug-ins for the 8350A Sweep Oscillator, Model 83570A Swept Source, uses a frequency doubler to deliver +10 dBm output power from 18 to 26.5 GHz. Doubling is achieved by operating dual-gate field-effect transistors in a highly nonlinear mode.[1] Two dual-gate FETs are used in a full-wave rectifier configuration which provides effective suppression of fundamental (input) frequency feedthrough as well as all odd-harmonic components. Fig. 1 is a photograph of the doubler and Fig. 2 is a schematic diagram.

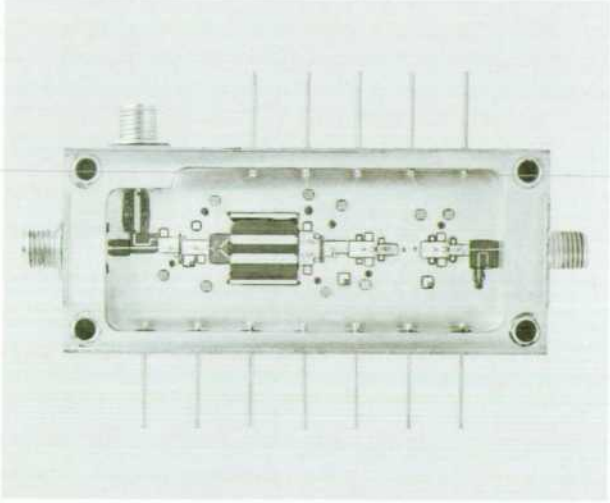

Fig. 1. *Frequency doubler delivers +10 dBm output power from 18 to 26.5 GHz.*

Input power to the doubler is split and directed to two sections of coplanar transmission lines. The conductors in one section are reversed with respect to those in the other. This accomplishes a broadband 180° phase shift allowing the first gates of the doubling FETs to be driven out-of-phase. The drains (outputs) of the FETs are directly combined through short lengths of transmission line. A virtual ground is presented at this point to the fundamental frequency and to all odd harmonics since equal-amplitude, opposite-phase components are being combined. The desired second harmonics generated in the two devices are combined in-phase.

Optimum device terminations were found using a harmonic load pull network analyzer system.[2] This allowed separate determination of optimum fundamental and second-harmonic frequency load terminations. As expected, the fundamental load yielding best doubling efficiency is a pure reactance, shifted slightly from an open circuit because of device output shunt capacitance. The optimum load for the desired second-harmonic output was found to be a large-signal conjugate match. Recall that the fundamental frequency sees a virtual ground through some length of transmission line. Thus the optimum fundamental load termination is easily realized by varying the length of transmission line between the output of each device and the combining point. The optimum second-harmonic load is near 50 ohms and is also not difficult to achieve.

Dual-gate FETs have been found empirically to be significantly more efficient as frequency doublers than single-gate FETs. This is believed to result from their superior gain during the linear amplification portion of the cycle and their greater output nonlinearity. Input nonlinearity is not believed to be a significant contributor to FET harmonic generation. The dual-gate FETs' first gates are conjugately matched at the input frequency and the second gates are grounded through a short wire bond.

Use of the dual-gate FET output nonlinearity for harmonic generation implies higher second-harmonic signal level for larger output signal swings. Thus it was desirable to provide one stage of FET preamplification to drive the doubler. This was accomplished by using another of the dual-gate FETs with conventional conjugate input and output matching. Again the dual-gate device offers advantages over the single-gate device by virtue of its superior gain through the input frequency range.

Two stages of postamplification are used to boost the output signal and compensate for the insertion loss of the PIN diode AM modulator which is placed between the postamplifier stages. Each of these amplifiers uses a 0.5-μm-gate-length FET (gate width is 350 μm) which is conjugately matched for its medium-power output operating conditions.

Finally, a microstrip coupler at the output delivers power to a Schottky diode detector. The dc signal from this detector is then fed to the instrument's automatic leveling control loop which in turn drives the PIN modulator. A coupler at the component's input provides a signal to the rear panel of the instrument. A customer might wish to use this 9-to-13.25-GHz signal to drive a counter or other instrument limited to 18-GHz operation.

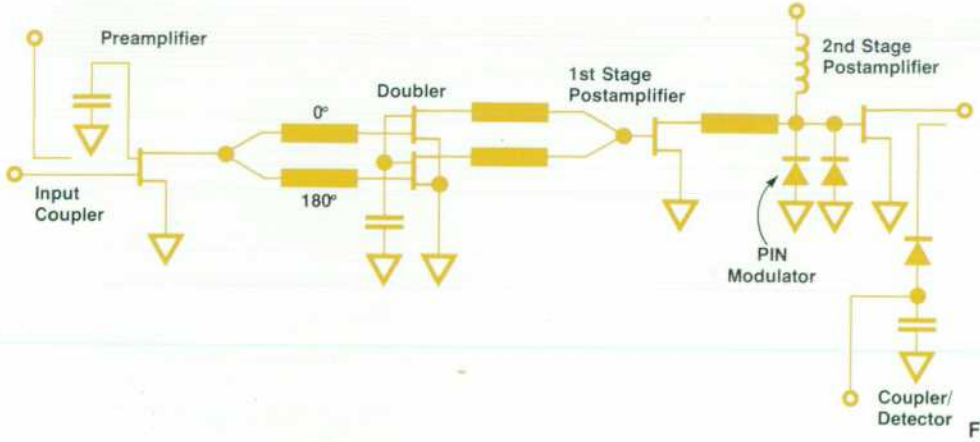

Fig. 2. *Schematic diagram of the frequency doubler.*

The doubler component is driven with +13 dBm from 18 to 26.5 GHz. The doubler stage itself delivers a minimum of +10 dBm to the postamplifiers and modulator. The resulting +13 dBm output level is sufficient to exceed the instrument specification of +10 dBm output even with the inclusion of an 18-to-26.5-GHz isolator which directly follows the doubler component.

Acknowledgments

We would like to thank Roger Stancliff and Rolf Dalichow for their guidance and technical leadership. We also wish to recognize Washington Gonzalez for his infinite patience as the first test technician on the product, Ron Blanc for his early production engineering support, and Larry Studebacker and Bill Loofbourrow for their process engineering efforts. Many others have worked hard to build this complex product, and their efforts are greatly appreciated.

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1. R. Stancliff, "Balanced Dual Gate GaAs FET Frequency Doublers," IEEE MTT Symposium Digest, 1981, pp. 143-145.
2. R. Stancliff and D. Poulin, "Harmonic Load Pull," IEEE MTT Symposium Digest, 1979, pp. 185-187.

-Val Peterson
-Jerry Orr

corrections using the front-panel power knob. The plug-in light-emitting diode display in this mode displays a hexadecimal code indicating the switch settings of two switches (one for offset, the other for slope) which are mounted on the driver boards. When the instrument is powered-up, or when **INST PRESET** is pushed, these switches are read by the microprocessor, which then calculates the required corrections for each band, adds them to the nominal offset and slope DAC scale factors stored in ROM, and saves them in RAM for use whenever a band change is necessary.

To enhance the overall frequency accuracy of the plug-ins, the YIG drivers compensate for errors introduced by YIG magnet nonlinearity, power supply variations, and magnet eddy current delay caused by sweeping. Fig. 7 shows how magnet nonlinearity compensation is accomplished. The output current driver uses feedback to force V_{ref} equal to V, the drive voltage. Since Q1's base current is negligible (the actual circuit uses three transistors) and the input impedance of the operational amplifier is high, all of the current through R_{ref} is required to flow through the coil. As V_{ref} drops with increasing magnet current, it crosses the level set by selected resistors R1 and R2 and the diode conducts, thus shunting R_{ref} with the parallel value of R1 and R2. The ratio of R1 and R2 determines the switch point and their magnitudes govern the amount of correction applied. Several such networks are required to reduce the nonlinearity of a given YIG device to a few megahertz across any band. To correct for variations in the +20V current driver supply, its voltage is added to the offset and slope DAC voltages in such a way that V_{ref} tracks any changes in +20V, thus resulting in no net voltage change across R_{ref}. This technique also assures good immunity to variations in +20V among mainframes.

When the current in a YIG magnet is changed rapidly, eddy currents are produced in the core, causing the net magnetic field at the YIG sphere to lag the drive current. A good approximation of the resulting frequency error caused by this delay is given by the equation,

$$f_{error} = a\,(df/dt)(bF(f) + c)$$

where df/dt is the sweep rate, a, b, and c are all constants, and F(f) is a function that is directly proportional to frequency, but whose value is zero at the start of any sweep. The delay compensation circuitry uses a differentiator and an analog multiplier to implement the above equation, and the resultant correction voltage is added to the main drive voltage. This technique represents an improvement over previous designs, since it results in better swept frequency accuracy while reducing the number and complexity of the adjustments required.

Care was taken throughout the design of the YIG drivers, as well as all other sensitive circuitry, to see that residual FM at the output was kept to a minimum. Precision, low-noise components are used throughout the tuning circuitry, and particular attention was given to the routing of signal and ground lines to avoid unwanted noise due to crosstalk or ground loops. Low-noise Zener diodes were used in the offset DAC reference circuitry, and in the case of plug-ins using harmonic multiplication (8359x), the uncorrelated noise of three Zener diodes is averaged to further reduce their total noise. As a result of these techniques, the maximum residual FM of the 83595A, for example, is only 12 kHz peak at 26.5 GHz.

Multiband Sweep Circuitry

Plug-ins capable of wide, multiband sweeps, such as the 83590A, 83592A, 83594A, and 83595A, do so by sweeping several individual frequency bands in sequence. When doing this, the plug-in stops the sweep and requests a band change whenever it reaches the end of a band. Once the band change has been completed, the sweep is released and the plug-in proceeds to sweep the next band. The additional circuitry required to accommodate multiband sweeps is shown in Fig. 8. It performs two main functions. First, it monitors the tuning voltage TV and indicates when a predetermined switch point is reached. Second, it converts the 0-to-10V tuning voltage ramp into multiple 0-to-−10V ramps, one for each of the separate bands in the multiband sweep. These functions are performed only during a multiband sweep.

FM Driver

The 83500 Series of plug-ins offers as a standard feature wideband FM capabilities previously obtainable only with a few specific plug-in models. The 10-MHz external FM bandwidth of all 83500 plug-ins is made possible by an FM driver design that is common to the entire series. A simplified schematic of this circuit is shown in Fig. 9.

The FM input signal is first separated into low (<700 Hz) and high (>700 Hz) frequency channels. The low-frequency portion of the signal is buffered, scaled, and sent to the YIG driver board(s) where it is summed with the main YIG coil driver voltage(s). The high-frequency component is also scaled, but drives instead a small FM coil internal to

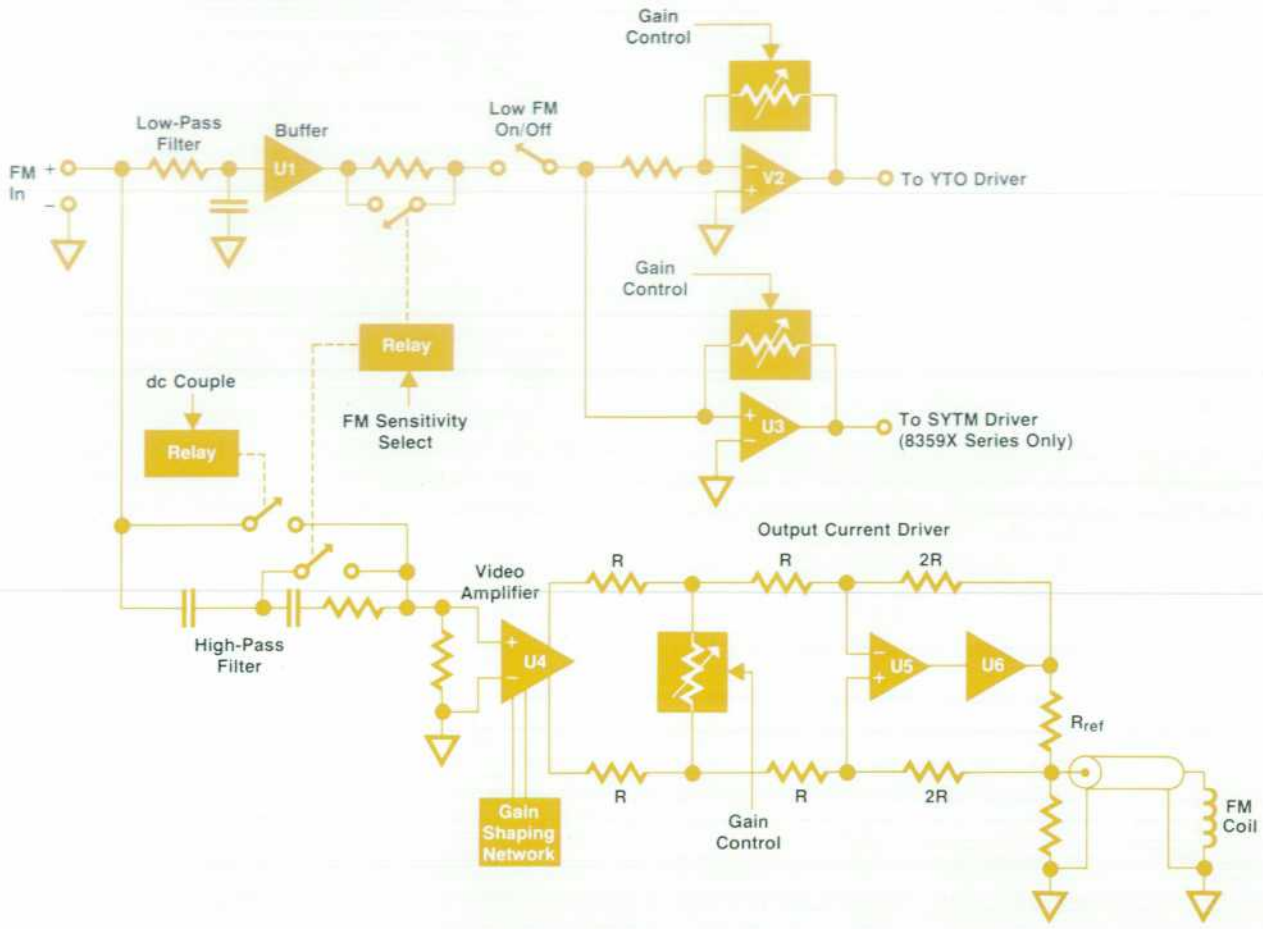

Fig. 9. *The FM driver used in all 83500 plug-ins provides a wide 10-MHz external FM bandwidth. This is a simplified schematic of the FM driver.*

the YIG oscillator. The microprocessor selects the gain of both channels depending on the FM sensitivity selected (−6 or −20 MHz/V), whether that sensitivity is relative to the plug-in's output frequency or to an auxiliary, fundamental output, and whether the plug-in is operating in a fundamental or harmonic frequency band. Of course, the last two of these factors apply only to those plug-ins using the SYTM; the others require only a sensitivity select, and the unneeded gain control components are deleted.

The high-frequency channel consists of a video amplifier (U4), and a broadband, bilateral output current driver consisting of a high-speed operational amplifier (U5) and current buffer (U6).

Automatic Power Level Control

In addition to controlling and modulating the RF output frequency of a sweeper, it is very desirable to control the amplitude of the signal being produced. Knowledge of a source's absolute amplitude and the ability to vary it are needed in the measurement of many nonlinear devices. To achieve this the automatic level control (ALC) circuitry in the 83500 Series performs several functions:

- Maintenance of calibrated power at the output connector as frequency changes
- Provision for operation with the 8755C Scalar Network Analyzer
- Compensation for increasing attenuation versus frequency in external hardware between the sweeper and the device under test (slope)
- Continuously increasing power as a function of sweep voltage (power sweep)
- Generation of amplitude markers
- Blanking of RF during reverse sweeps
- Provision for use of an external crystal detector or an HP 432A/B/C Power Meter for power control
- Provision for analog and square-wave amplitude modulation.

All of these functions are under the control of the microprocessor in the 8350A mainframe.

To provide for the potentially large range of output power that could be desired from a source, the decision was made to maintain logarithmic rather than linear control of output power. That is, the output is controlled in dBm (decibels compared to one milliwatt) rather than in milliwatts or watts. This decision also reduced the extremes over which the control loop needed to operate. Fig. 10 shows a block diagram of the ALC circuits.

In internal leveling mode a directional coupler produces an output that is a small sample of the forward power appearing at the output connector. This sample is then converted by a diode detector to a dc voltage proportional to

A Broadband 2-to-7-GHz Power Amplifier

The broadband GaAs MESFET Amplifier for the 8359x sweep oscillator plug-ins provides 500 mW of RF power from 2 to 7 GHz to the YIG-tuned multiplier. The signal input to the amplifier is approximately 10 mW from the preceding oscillator and modulator. The YIG-tuned multiplier generates harmonics and filters unwanted signals to create a 2-to-26.5-GHz sweeping output (see page 15).

The new amplifier design is based on an existing 2-to-6.2-GHz, 300-mW amplifier.[1] The requirements are an operating frequency of 2-7.0 GHz, a power output of 500 mW, and power consumption less than the existing design's 18 watts. A logical block diagram, simple design, uniform performance, and ease of manufacturing are as important as the electrical specifications.

The basic block diagram is shown in Fig. 1, and a photograph in Fig. 2. The numbers indicate the gate widths of the devices. The final stage consists of two 1500-μm gate-width FETs in a balanced configuration. These FETs use a V_{DS} of 7 volts and are 100% wafer tested for drain breakdown voltage greater than 14 volts. The optimum power match for this device was measured using the load pull technique.[2] The results revealed that a single quarter-wavelength transformer would produce adequate output matching across the 2-to-7-GHz frequency range.

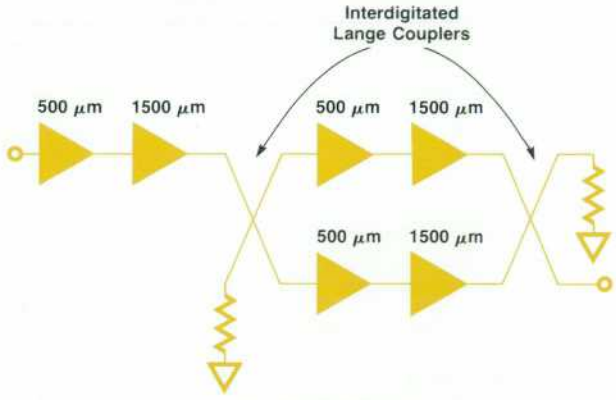

Fig. 1. *2-to-7-GHz amplifier block diagram. Numbers are gate widths of the FET amplifier stages.*

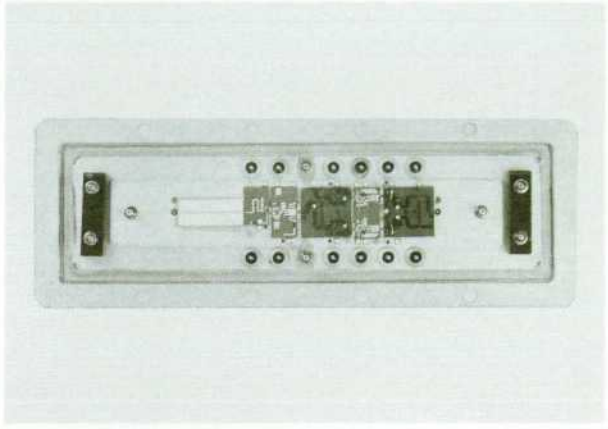

Fig. 2. *2-to-7-GHz Amplifier.*

The interdigitated coupler[3] has four fingers with 0.03-mm spacing between conductors. An advanced thin-film technology produces conductors with this spacing to an accuracy of 0.0025 mm on a 0.64-mm-thick sapphire substrate.

Typically, the small-signal gain is flat within ±2.5 dB, large-signal gain is flat within ±1.0 dB, and output VSWR is less than 2.0 from 2 to 7.0 GHz. Total power consumption is typically less than 10 watts including the bias board.

Acknowledgments

The original amplifier was designed by Derry Hornbuckle, who also gave guidance to this amplifier design.

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2. D. Poulin, "Load pull measurements help you meet your match," Microwaves, November 1980, p. 61.
3. J. Lange, "Interdigitated Stripline Quadrature Hybrids," IEEE Transactions, Vol. MTT-17, December 1969, p. 1150-1.

-Michio Furukawa

output power. After being processed by appropriate switches and buffering, the signal is applied to a logarithmic amplifier which produces an output proportional to the logarithm of the output power. This voltage is scaled and compared at the summing node to a voltage proportional to the desired output power which is generated in the reference circuits.

The reference voltage is dependent on a number of inputs: the requested power input from the rotary pulse generator, keyboard, or HP-IB, modification of that power due to power sweep or slope requirements, any signal applied at the external AM input for amplitude modulating the RF, and any correction applied to compensate for coupler/detector variations. The power sweep and slope functions are produced by processing a voltage proportional to the sweep (0-10V, start to stop) in a multiplying DAC. In slope mode, the microprocessor calculates the power modification required based on the frequency range being swept and the slope correction requested. Because of the logarithmic amplifier in the detector path and the definition of the signal from the reference path, any voltage difference at the summing node is proportional to the error between the desired output and the obtained output, expressed in dB.

The error voltage is applied to the main loop integrating amplifier. The output of this amplifier is used to control an exponential current source which drives the appropriate PIN diode modulator. The exponential current source enables the RF output to respond linearly in decibels to a voltage change at its input. This is necessary since the loop variable is dBm. The main loop amplifier also drives a comparator to indicate an unleveled power condition. Unleveled power may occur when output power greater than the specified instrument power is requested.

External leveling operates in a manner very similar to internal leveling. In the case of external crystal detector

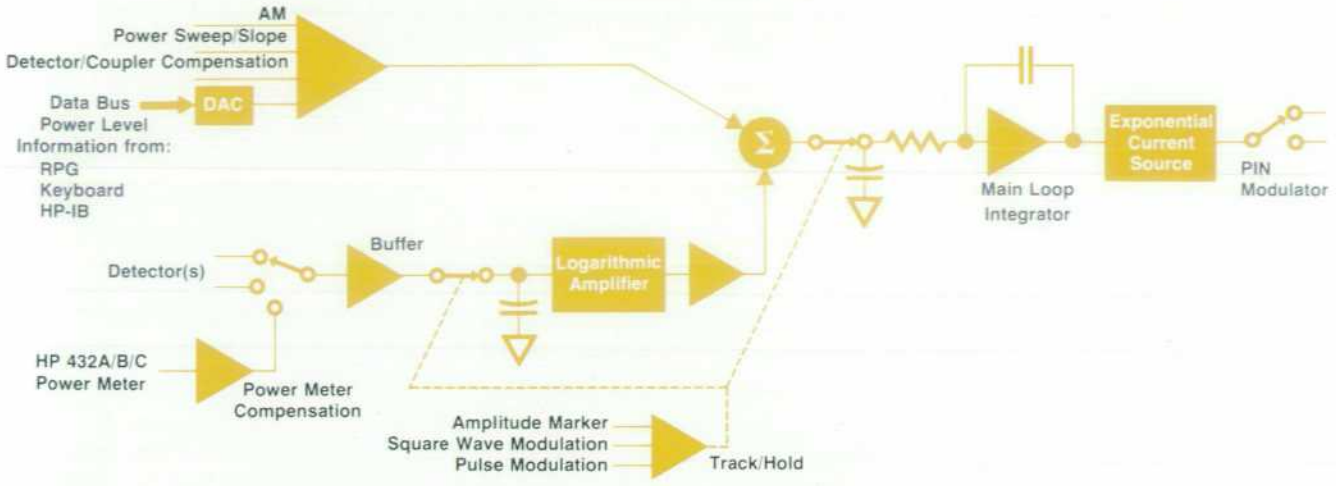

Fig. 10. *Block diagram of the internal leveling circuits that maintain constant output power and provide for amplitude modulation.*

control, the external detector input is applied to the buffer and logarithmic amplifier. HP 432A/B/C Power Meter operation is similar, with the exception of additional loop compensation included ahead of the logarithmic amplifier and in the main loop integrator. This compensation is necessary to stabilize the loop with the slower response time of the power meter.

To provide compatibility with the 8755C Scalar Network Analyzer, the RF signal is modulated with a 27.8-kHz square wave. To provide this, a track-and-hold circuit is used. This allows use of the internal ALC modulator and avoids any additional losses that an external modulator would produce in the RF path. The track-and-hold circuit allows the RF power to be removed without requiring that the loop follow. The amplifiers in the loop hold the levels that existed just before power was removed and then begin tracking again when power is returned.

Amplitude markers operate in a similar manner, with power removed and the track-and-hold circuit holding during an amplitude marker.

Acknowledgments

We would like to acknowledge the contributions that many people made to the design of these plug-ins. We would like to thank Irv Hawley and Arlen Dethlefsen for their managerial support. Paul Hernday and Roger Stancliff were project managers during the early phases of the design. The product design was done by Daniel Swan, David Copley, and George Baker. Lynn Rhymes, Sue Conway, John Regazzi, and Jerry Orr worked on the printed circuit board design.

Duaine C. Wood

Duaine Wood received his BSEE and MSEE degrees from Brigham Young University in 1976 and 1977. With HP since 1977, he had primary design responsibility for the 835xx YTO drivers, the 8359x YTM driver, and the 835xx FM driver. He also helped design the 8359x multiband sweep circuitry. Duaine was born in Provo, Utah, grew up in the San Francisco Bay Area, and now lives in Santa Rosa, California. He's married and has three children. In addition to running, gardening, woodworking, and electronics, Duaine is involved in church work and enjoys family activities.

Gary W. Holmlund

A native of Bucklin, Missouri, Gary Holmlund attended the University of Missouri at Columbia, receiving his BSEE and MSEE degrees in 1972. He joined HP in 1973, helped design the 8620C/86290A Sweep Oscillator, and has served as project manager for the 86290B and several 83500 Series RF plug-ins. He is a co-inventor on a patent on a method of providing crystal-accuracy markers while sweeping. Gary is married, has two sons, lives in Santa Rosa, California, and has a strong interest in microcomputers.

Glenn E. Elmore

Glenn Elmore joined HP's Santa Rosa Division in 1972 after two years of running his own communications system business. He spent four years in instrument test, then joined the R&D lab and helped design several sweeper products, most recently serving as an associate engineer on the new 83500 Series plug-ins. Glenn was born in Sebastopol, California and now lives in nearby Santa Rosa. He is married and his interests include bicycling, amateur radio, and signal propagation via man-made and natural satellites.

Portable Defibrillator-Monitor for Cardiac Resuscitation

This new portable defibrillator monitors the patient, measures its effectiveness in delivering a high-voltage pulse to the patient, and provides a permanent record of the resuscitation procedure.

by Paul I. Bennett and Victor C. Jones

A VERY TENSE DRAMA begins when a human heart ceases to beat. Death from irreversible damage of the nervous system is three to five minutes away but can be avoided if proper action is taken to restore blood circulation promptly. Since the probability of a successful resuscitation procedure is highly dependent upon the amount of time the heart is not beating, little time is available for setting up equipment and looking for things; attention must be directed to the patient. Afterwards, the procedure must be documented for legal purposes, and for the review committee who will analyze the entire event for possible improvement at the next emergency procedure. The new HP Model 78660A Defibrillator-Monitor (Fig. 1) is designed for this type of medical emergency.

The heart is a mechanical pump that is bioelectrically controlled. During a heart attack the muscle action of the heart deteriorates from a coordinated periodic contraction to a convulsive quiver known as fibrillation. This is often brought about when the myocardial muscle is deprived of blood by a restricted artery (myocardial infarction) leading to a condition where many areas of the heart rather than one attempt to electrically initiate the pumping contraction. The ensuing biological pandemonium is ineffective in pumping blood through the body. Cardiac resuscitation requires that fibrillation be terminated and the heart be left in a condition allowing the body's natural electrical pacemaker to stimulate proper pumping action.

Medical personnel must make many assessments before emergency treatment is begun. The status of heart action is indicated by its bioelectrical activity which can be observed by placing electrodes on the chest and connecting them to an ECG (electrocardiogram) monitor or recorder. Vital signs are checked. Attention is given to ensure an open breathing passage. Patient history is mentally reviewed but time constraints dictate that action be quick and optimal.

Among the treatment options open to medical personnel

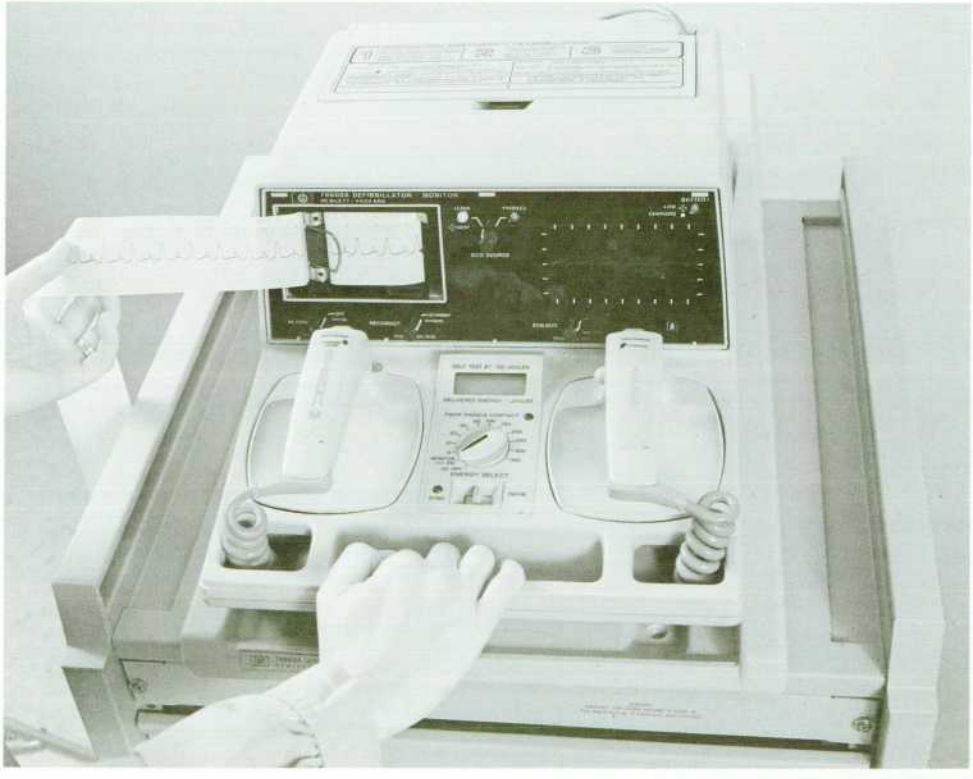

Fig. 1. *The HP Model 78660A Defibrillator-Monitor is a convenient portable instrument for resuscitation, monitoring, and documentation in cardiac-arrest emergencies.*

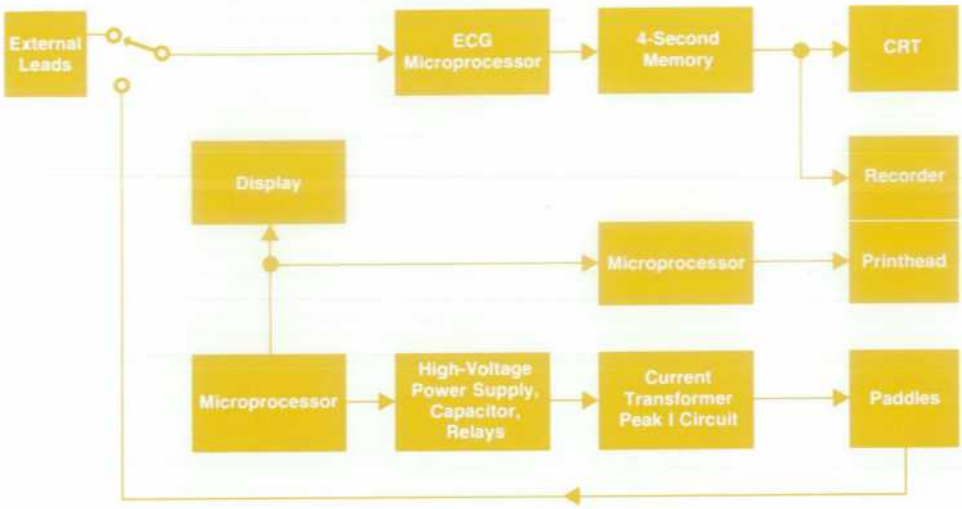

Fig. 2. *Block diagram of the 78660A.*

are chemical, mechanical and electrical stimulation of the body. Chemical or drug injections are more effective in managing the situation after the heart is restarted than in arresting fibrillation. Mechanical means such as the CPR (cardiopulmonary resuscitation) technique of compressing the heart between the anterior chest wall and the thoracic spine restores only about 20% of normal blood flow and it does not alter the basic problem of fibrillation. It may prolong life, however, until additional help arrives. Precordial thumping or beating on the chest to terminate fibrillation has enjoyed only limited success. The chaotic bioelectrical activity of the heart can be stopped if a momentary electrical current is passed through it. This can be done by applying a high-voltage pulse to the chest. This procedure is known as defibrillation and is now a standard emergency treatment in the hospital and for paramedic teams in many areas.

Hewlett-Packard has produced defibrillators since the procedure became standard in the early 1960s. At that time a defibrillator was simply an ac-power-line-operated box that produced a high-voltage pulse. However, resuscitation is an evolving science and so is the equipment. Researchers are satisfied that a dc damped-sinusoid waveform having an energy up to several hundred joules (watt-seconds) and a duration of several milliseconds has a high probability of success if applied promptly. However, much work remains to optimize the required equipment. In the heat of battle to save a patient's life the operator must not be faced with distractions or confusion about operating the instrument and should be provided with as much pertinent information as possible to aid in making correct decisions. Traditionally, informational feedback from the defibrillator has been minimal. An ECG monitor which displays the bioelectrical activity of the heart is usually provided and a recorder to document the waveforms has been available, but judgment about the effectiveness of the high-voltage discharge is often based on an observation as to how high the patient's body jumps (convulses) during the procedure.

The HP Model 78660A Defibrillator-Monitor measures the current flowing through the patient during the high-voltage discharge and the patient's impedance is calculated from the knowledge of the peak current. During discharge, transthoracic impedance is usually within the range of 25 to 100 ohms so anything over 100 ohms is immediately brought to the attention of the operator.

A block diagram of the basic components used in the 78660A is shown in Fig. 2. For various operator activities the recorder runs automatically, minimizing the need for operator attention. Time and heart rate are periodically printed and procedure parameters such as selected energy, discharge energy, peak discharge current and patient impedance are recorded automatically. The ECG monitor has been improved with an automatic gain setting, baseline (offset) restore, 60-Hz filter and a very effective heartbeat detector. Should a drug injection or other special treatment be given, the operator can press a button and the exact time of that event is recorded. The instrument package is designed to solve some logistics problems by providing on-board storage for most desired accessories and a novel mounting scheme for use on carts and storage between emergencies.

Measurement of Defibrillation Parameters

Providing an effective defibrillation pulse during an emergency procedure is critical to the success of the resuscitation effort. Many variables can change the output dose, but without direct feedback the operator has little information to use in assessing the performance of the procedure. A method of providing defibrillation pulse information in-

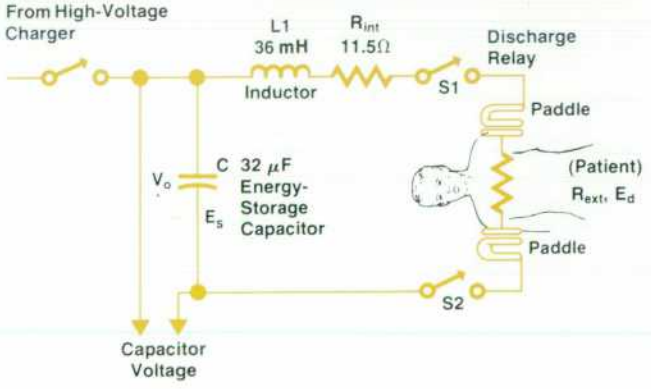

Fig. 3. *Schematic diagram of the basic defibrillator discharge circuit.*

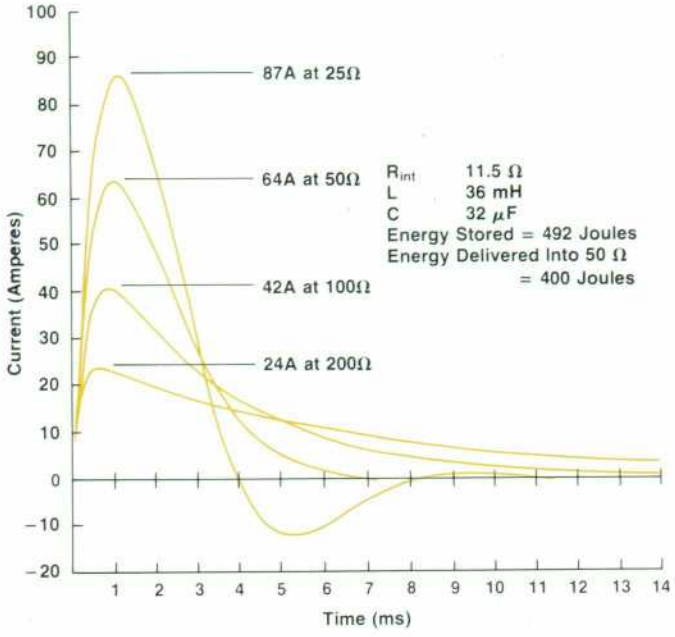

Fig. 4. *Discharge currents versus time for various patient resistances given a fixed stored energy of 492 joules.*

stantly is needed along with direct documentation of the parameters for clinical use.

Fig. 3 shows a schematic diagram of a defibrillator circuit. A selected amount of electrical energy E_s is stored in a capacitor. The discharge waveform is determined by the defibrillator circuit parameters (capacitance C, inductance L, and internal resistance R_{int}) and by the external resistance R_{ext} presented to the defibrillator paddles. Unless poor skin preparation produces a significant interface resistance, the external resistance should be very close to the patient's transthoracic impedance. The following discussion assumes that the external resistance is essentially equal to the patient's impedance.

It is now thought that, in addition to patient related parameters, defibrillation effectiveness depends primarily on the current density through the myocardium, and hence correlates more directly with peak current than with delivered energy.

Fig. 4 shows the discharge current going through the chest for four values of external resistance R_{ext}, given a fixed amount of stored energy (that which would deliver 400 joules into 50 ohms). When R_{ext} is of the order of 50 ohms the circuit is critically damped and the discharge duration is minimal at approximately 5 milliseconds. These conditions are considered optimum for effective defibrillation and therefore the defibrillator circuit parameters are usually chosen to yield a critically damped discharge for a value of R_{ext} close to the average observed value of patient impedance.

Fig. 5 shows the relationship between the peak current and delivered energy for different values of patient impedance using the 78660A. If we accept the present theory that current defibrillates and assume that, for instance, a certain adult patient requires a peak current of 40 amperes, Fig. 6 shows that the required delivered energy is 150 joules at 50 ohms, but ranges from a low value of 60 joules at 20 ohms to 400 joules at 100 ohms and as much as 780 joules at 150 ohms, an energy variation greater than 10 to 1.

It is therefore clear that because patient impedance can vary considerably it has a strong effect on defibrillation effectiveness. Hence, knowledge of peak current, patient impedance and actual delivered energy will greatly enhance the ability of the operator to assess and improve defibrillation effectiveness. Optimizing patient impedance through appropriate techniques will enhance the probability of successful defibrillation at lower selected energies.

Patient impedance and delivered energy can be directly determined from the peak discharge current I_m if the stored energy E_s and the defibrillator circuit parameters (capacitance C, inductance L and internal resistance R_{int}) are known.[1] Peak current can be expressed in the most general form:

$$I_m = f(E_s,R,L,C)$$

where R is the total circuit resistance, i.e., $R = R_{int} + R_{ext}$.

The dependence of peak current I_m on stored energy E_s is very simple, I_m being proportional to the square root of the stored energy. For instance, Fig. 5 shows that the peak current at any external resistance is exactly twice as high at 400 joules as at 100 joules. Consequently, the general ex-

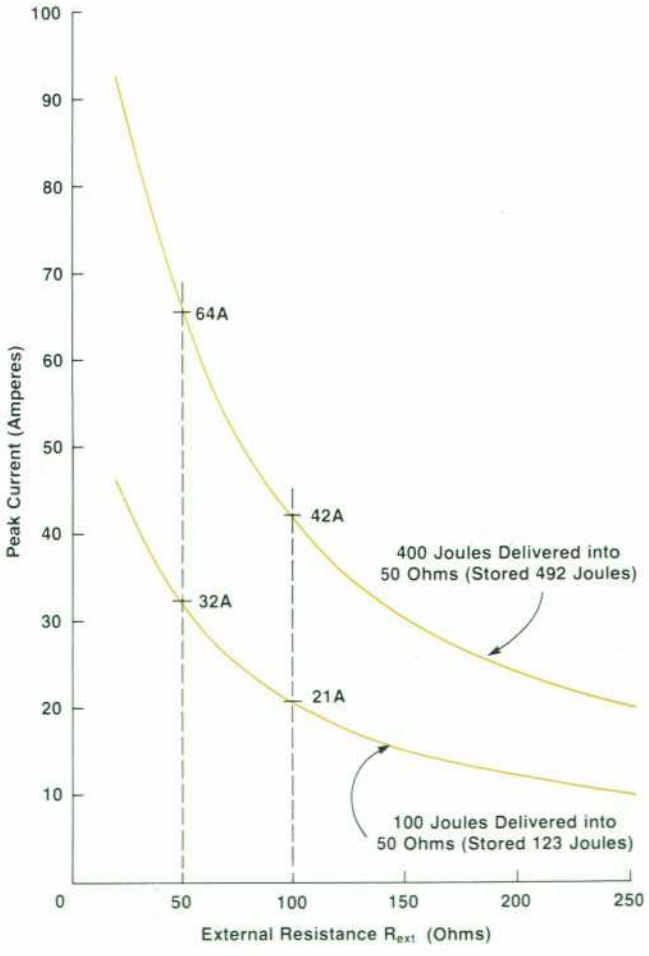

Fig. 5. *Peak discharge current versus external load resistance for two stored energies.*

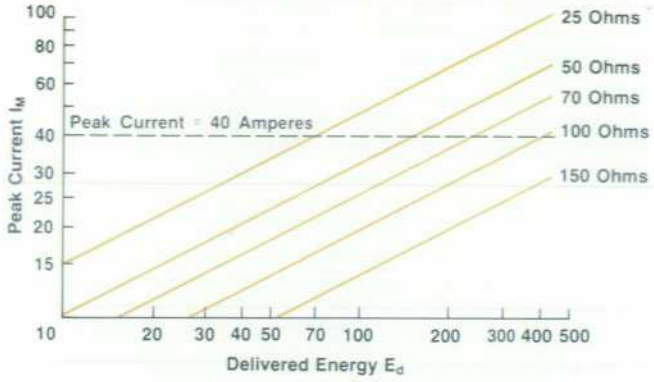

Fig. 6. *78660A peak discharge current I_m versus delivered energy E_d for various values of patient resistance.*

pression for peak current can be restated:

$$I_m = (\sqrt{E_s}) \times f[(R_{int} + R_{ext}),L,C]$$

The defibrillator circuit parameters (R_{int},L,C) are known and fixed for a given defibrillator, thus the only unknown variable is patient impedance R_{ext}. Hence, substituting known values for the defibrillator circuit parameters, the normalized peak discharge current i_m becomes a function of R_{ext} only:

$$i_m = I_m/\sqrt{E_s} = f(R_{ext})$$

The function of R_{ext} is most conveniently derived from general circuit equations, and can also be measured directly through a series of discharges with different external resistors. The function is single-valued and monotonic, hence there is a one-to-one correspondence between I_m and R_{ext}.

Fig. 7 shows a simplified diagram of the discharge control and recording circuit. Before the discharge the operator selects the desired energy E_d to be delivered into a 50-ohm load. The microprocessor determines the corresponding value of stored energy E_s by using the expression $E_s = E_d(R_{ext} + R_{int})/R_{ext}$. The corresponding storage capacitor voltage V_o ($E_s = 0.5CV_o^2$) is sensed and regulated by the microprocessor. The discharge current passes through a current-sensing transformer placed in the wiring. Use of a sensing transformer provides ground isolation for the patient circuit, yielding a safe, simple method for measuring the discharge current. The transformer provides a voltage signal that is peak-detected and recorded by the microprocessor. Since the entire waveform is not needed, it is much more practical to sample the peak current in a highly filtered noise-immune analog circuit than to digitize the entire waveform. The microprocessor takes the measured peak discharge current and uses this value along with the stored energy E_s to determine patient impedance R_{ext} and delivered energy E_d as discussed above. The microprocessor then drives a three-digit display and annotates peak current, patient impedance and delivered energy on a strip-chart recorder. A **POOR PADDLE CONTACT** warning indicator is also activated when the patient impedance exceeds 100 ohms. The 100-ohm caution level was selected because, with good paddle preparation and location, the patient impedance should almost always be well below 100 ohms. The time of day is added to the strip-chart to complete documentation of the defibrillation episode and produce a good permanent record.

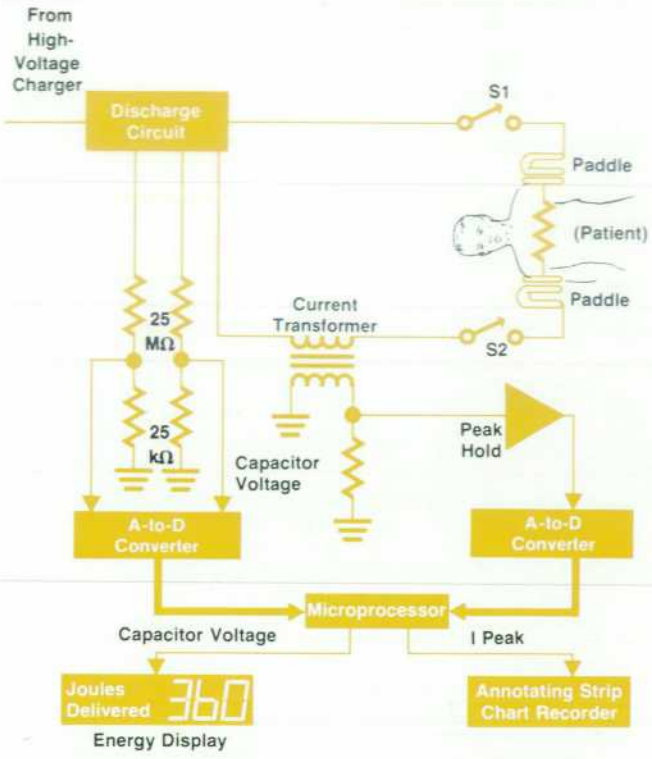

Fig. 7. *Simplified block diagram of the 78660A's discharge control and recording circuitry.*

QRS Detection

Both the heart-rate calculation and a procedure called synchronized cardioversion require that the R-wave portion of the ECG signal be detected. To terminate atrial fibrillation, the defibrillator can be used in a synchronized mode where the high-voltage pulse to the heart is initiated at the moment of the patient's R-wave. To be effective, the QRS detector must detect the QRS complex (see Fig. 8) within 20 milliseconds of the peak of the R wave and also minimize chances of triggering the discharge during other portions of the ECG signal, such as the T wave, which could change atrial fibrillation into the more serious ventricular fibrillation.

Also, calculation of the heart rate, which is displayed on the instrument, is highly dependent upon the reliability of the signal from the QRS detector. Should a high-level signal occur, a simple peak-following threshold would miss the next several R waves. By using a floating threshold that is an average of several previous peak values, the number of undetected beats is reduced.

An integrating analog-to-digital (A-to-D) converter supplies digitized ECG data to the microprocessor at 4-ms intervals. It is then digitally bandpass filtered, full-wave rectified and compared with the floating threshold (Fig. 9).

The equation for the bandpass filter of 7 to 35 Hz is:

$$Y(t) = (3/4)\,Y(t-1) + [X(t) - X(t-4)]$$

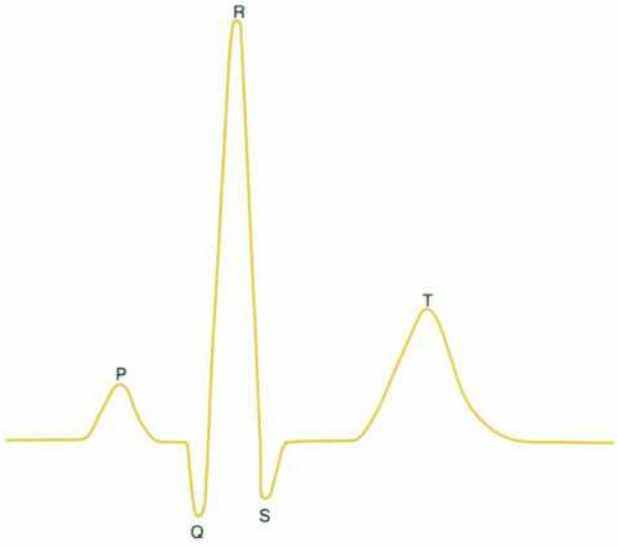

Fig. 8. *Typical ECG heartbeat waveform.*

where X(t−4) represents the fourth previous input into the filter and Y(t−1) is the previous output of the filter. This filter is preferred over a simple differentiator because the spectral density of a QRS complex centers about 10 to 20 Hz. Using this filter delays the signal only about 16 ms.

A pulse is output whenever the filtered signal exceeds the floating threshold level. This level varies with the time elapsed since the last detected R wave. For the first 200 ms after an R wave all detection is inhibited, establishing the upper limit of 300 beats per minute. After this period, the threshold is set at 75% of the average peak value detected during the previous heartbeats. If no signal exceeds the threshold after 75% of the time measured between the two previous detections, the threshold is reduced again by 25%. If no R wave is detected after two seconds (corresponding to 30 beats per minute) the threshold drops to a predetermined minimum level.

Automatic Gain Control

Before the ECG waveform is digitized it passes through a variable-gain stage which is simply an operational amplifier with one of five inverting feedback resistors selected by the microprocessor (Fig. 9). If the signal is greater than a maximum threshold, the processor selects the next lower gain setting. If the signal is below a minimum threshold for two seconds, the processor selects maximum gain and then decrements the gain until the maximum threshold is no longer exceeded.

This gain algorithm works fine until the patient being monitored moves and the ECG baseline wanders with the patient's motions. By filtering the ECG signal with a high-pass filter the baseline wander can be removed. Sampling at 4.1-ms intervals a high-pass pole below 2 Hz can be accomplished and represented by an equation somewhat like this one:

$$Y(t) = (31/32)Y(t-1) + [X(t) - X(t-1)].$$

But when an 8-bit signal is being divided by a number greater than 16 the resulting quotient is 3 bits or less (integer arithmetic). However, if consecutive A-to-D samples are added in pairs, the result is essentially a 9-bit A-to-D conversion with an 8.2-ms sampling time. After this, the same filter can be derived from

$$Y(t) = (15/16)Y(t-1) + [X(t) - X(t-1)]$$

Both methods yield a high-pass filter with a pole at 1.2 Hz but the latter increases the resolution of the division by 2 bits—one from the extra ninth A-to-D bit and the other from dividing by 16 instead of 32.

An advantage of software signal processing is the manipulation of filters without component changes. With crystal timing, poles and zeros are unaffected by temperature changes. Also, optimization of the floating threshold algorithm would be impractical in hardware.

Noise Susceptibility

Microprocessors and other high-density large-scale integrated (LSI) circuits have small voltage differences be-

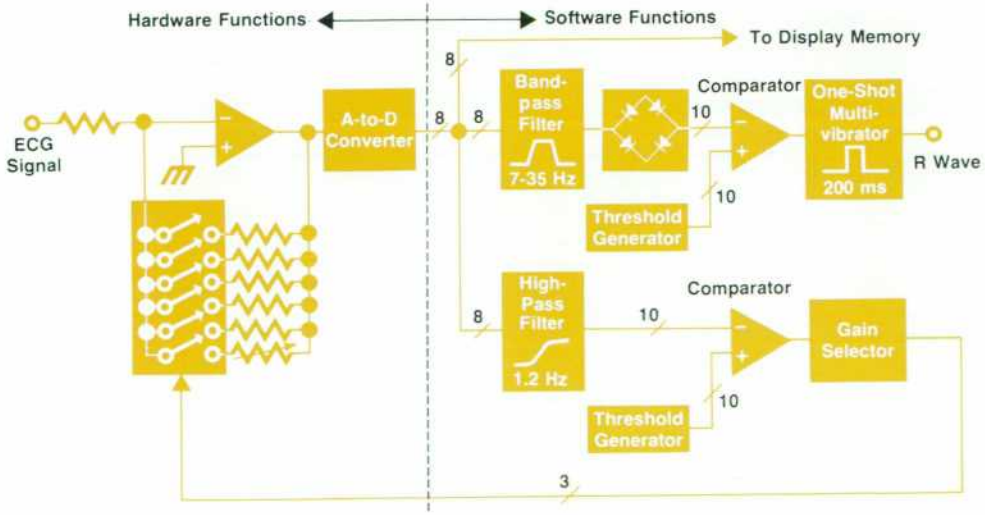

Fig. 9. *Block diagram of heartbeat detection circuitry.*

tween logic states, small transistor cell size, high-speed performance, and numerous leads to the outside world. All of these factors make them prime targets for noise, both conducted and radiated. Malfunctions can take the form of altered RAM (random-access memory) cell contents, output latches that change state, and altered internal registers such as the program counter. If the program counter is modified, software execution continues, but operation becomes erratic and highly unpredictable. Normal operation is restored only when the operator switches the power off and on again.

When the instrument in question is a critical medical device, malfunctions cannot be tolerated. In a defibrillator noise is a problem because the instrument must control discharge of a capacitor charged to as much as 5000 volts along current paths to both the patient and a safety bleeder resistor through low-bounce relay contacts. Electrical noise of frequencies up to 100 MHz is rampant during the brief discharge interval. Cables and printed circuit board foils become receiver antennas and capacitive couplers.

Power-supply bypassing must be well applied and augmented by bypass networks on the I/O (input/output) ports and control signal lines. An additional mandatory technique involves joining the software to the automatic hardware reset of the microprocessor. Called a tickle circuit, a retriggerable oscillator will reset the processor if a software-generated signal, called the heartbeat, does not continually inhibit the oscillator. If noise causes the processor to run off to execute some other section of software and fail to produce the heartbeat on schedule, the tickle reset restarts the processor back at address location zero. The processor then looks in the RAM for the presence of a password, previously installed upon the successful completion of the power-up sequence. The presence of this code differentiates this warm start (was on, but got reset) from a cold start (power was just turned on).

Each of the three processors in the 78660A uses this technique in a slightly different manner. In the control processor, this warm-start code identifies the particular software module that was operating before the malfunction and a vectored jump to that module after the reset immediately restores operation, completely transparent to the operator. Since the control processor is aware of each impending discharge and its attendant noise, the processor goes into a sleep function after energizing the discharge relays and remains in a reset state during the noise period.

The recorder processor has a number of tasks, each in a software module, that are sequentially performed every 16 ms. As each is performed it adds one bit to the code. At the end of 16 ms, the code byte is examined and if proper, a heartbeat pulse is output. If improper, signifying irregular processor activity, a software halt is issued terminating heartbeat output. The tickle circuit will then reset the processor and the presence of the proper password will warm start the processor back into normal operation. Time to rectify the abnormal operation is about 25 ms and is transparent to the operator. The ECG processor issues a heartbeat to its tickle circuit every 4 ms and will reset in 30 ms if it experiences abnormal software execution. In addition, its software contains halt traps in blank ROM (read-only memory) areas.

Package

The attractive polycarbonate case allows the 12.7-kg instrument to be easily carried by its integral handle. The center of gravity is directly below the handle to avoid banging against the carrier's body and the perimeter of the case is designed to absorb energy when accidently hitting walls, doors, etc. Integral paddle holders and cables that retract into the instrument ensure that cables are not snagged when rushing down the hall (Fig. 10). A pouch is provided to hold the necessary ECG lead set and paddle electrode paste. The unit is stable when placed on its bottom or back and is rainproof. Small electrodes for pediatric patients are available by simply unscrewing the adult electrodes from the paddles. The nickel-cadmium battery pack can be replaced in a few seconds. The standard power base mounts vertically, horizontally, or on a drug cart, and provides a socket for automatic connection to ac power when the 78660A is placed in the base. Various display bezel overlays snap in on the front panel for different production models and language options.

Acknowledgments

The noise studies and implementation of patient impedance were accomplished by Paul Long. ECG software and hardware are to the credit of Peter Wai. Industrial designer Kail Peterson evolved the highly functional yet attractive package. Many others including Martin Rockwell, Mickey

Fig. 10. *The 78660A can be quickly detached from its 78668A Quick-Mount Power Base and easily carried to a cardiac emergency. All of the necessary cables, electrodes, and recording paper are contained in the instrument.*

Victor C. Jones

Vic Jones joined HP in 1973 after earning the MS degree in electrical engineering at Rensselaer Polytechnic Institute. He also received the BS degree in the same subject in 1971. Vic started at HP's Waltham Division and worked on bedside monitors, production engineering, and defibrillator reliability studies. He transferred to the McMinnville Division in 1977 and was the project manager for the 78660A. Vic is now back at Waltham as a project manager for bedside monitors. He has written four papers on the 78660A and its delivered-energy algorithm. Vic was born in Buffalo, New York and now lives in Stow, Massachusetts with his wife and their two adopted children. He is a member of the local Kiwanis club and enjoys skiing, automotive sports, and furniture building.

Paul I. Bennett

Paul Bennett received a BA degree in physics from Linfield College, Oregon in 1960. After experience working overseas in Italy and Brazil he went to work for Field Emission Corporation which became HP's McMinnville Division in 1973. Paul has worked on high-voltage and control systems for x-ray equipment and was the division's international sales manager for several years. More recently he has worked on microprocessor control of a medical x-ray system and the 78660A. Paul was born in Chicago, Illinois and now lives in McMinnville, Oregon. He is married, has three children, and enjoys playing volleyball and the piano, working with his home computer, and sailing catamarans.

PRODUCT INFORMATION

HP Model 78660A Defibrillator-Monitor
MANUFACTURING DIVISION:
McMinnville Division
1700 S. Baker Street
McMinnville, Oregon 97128 U.S.A.
TECHNICAL DATA: HP Publication Nos. 5952-6834, 6835, 6836.
PRICE IN U.S.A.: 78660A, $7,400; includes 78668A Quick Mount Power Base.

HP Model 8350A Sweep Oscillator
MANUFACTURING DIVISION:
Santa Rosa Division
1400 Fountain Grove Parkway
Santa Rosa, California 95404 U.S.A.
TECHNICAL DATA: HP Publication No. 5952-9321
PRICE IN U.S.A.: 8350A Mainframe, $4250.
83500 Series RF Plug-ins, $5100 to $27,000.

Mathena, John Brewster, and Ty Hegna contributed in no small part together with inputs from marketing and production engineering in a cooperative fashion which exemplifies the excellent communication possible in a small division.

Reference

1. V.C. Jones, et al, "A New Method of Determining Transthoracic Impedance, Delivered Energy and Peak Current During Defibrillator Episodes," Journal of the Association for the Advancement of Medical Instrumentation, Vol. 15, no. 6, November-December 1981.

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