Mullard Book 4 Part 6a 1983

Professional analog ICs

Mullard

technical handbook

Book 4

Integrated circuits

Part 6a

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1983

PROFESSIONAL ANALOG ICs

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Integrated circuits

Professional analog ICs

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The Mullard technical handbook system.

The Mullard Technical Handbook is made up of four sets of Books, each comprising several parts:-

Book 1 (light blue)	Semiconductor Devices
Book 2 (orange)	Valves and Tubes
Book 3 (green)	Components, Materials and Assemblies
Book 4 (purple or dark blue)	Integrated Circuits

Book 4, Integrated Circuits, comprises the following parts:-

Part 1	Bipolar ICs for radio and audio equipment
Part 2	Bipolar ICs for video equipment
Part 3	ICs for digital systems in radio, audio and video equipment
Part 4	Digital ICs – CMOS
Part 5	High-speed CMOS
Part 6	Analog ICs (Signetics)
Part 6a	Professional analog ICs
Part 7	Bipolar memory ICs
Part 7a	Integrated fuse logic
Part 8	TTL Logic ICs
Part 9	Microprocessors, microcomputers and peripheral ICs

....a comprehensive data library

Most of the devices for which full data is given in these books are those around which we would recommend equipment to be designed. Where appropriate, other types no longer recommended for new equipment designs but generally available for equipment production, are listed separately. Data sheets for these types may be obtained on request. Older devices for which data may be obtained on request are also included in the index of the appropriate part of each book.

Because the Technical Handbook system forms a comprehensive data reference library the current Mullard Quick Reference Guides should always be consulted for details of the Mullard preferred range.

The data contained in these books is as accurate and up to date as possible at the time of going to press. It must be understood, however, that no guarantee can be given on the availability of the various devices, or that their specifications may not be changed before the next edition is published.

Each part is reviewed regularly, and revised and re-issued where necessary. Revisions to previous data are indicated by an arrow in the margin.

Requests for copies of Quick Reference Guides and individual data sheets (please quote the type number) should be sent to:-

Technical Publications Department, Mullard Limited, New Road, Mitcham, Surrey CR4 4XY. Telex 22194.

Prices and availability information for Mullard components should be obtained from Mullard House, or from one of the Mullard Distributors listed on the back cover.

The Mullard Data Base

For the equipment designer, technical information on electronic components is vital. Mullard market the widest range of components in the U.K., supported by a comprehensive information service – the Mullard Data Base.

Brief details are given here. For further information and an order form, please write to:-

Technical Publications Dept.
Mullard Limited,
New Road, Mitcham,
Surrey CR4 4XY.

Regular Publications

Mullard Bulletin

A must for designers, this bi-monthly, newspaper-style publication briefly describes new components and offers further information on subjects of interest.

Consumer Electronics

A review, in newspaper style, published every four months. Articles and features of interest to those in the consumer electronics industry, with emphasis on television technology and allied subjects.

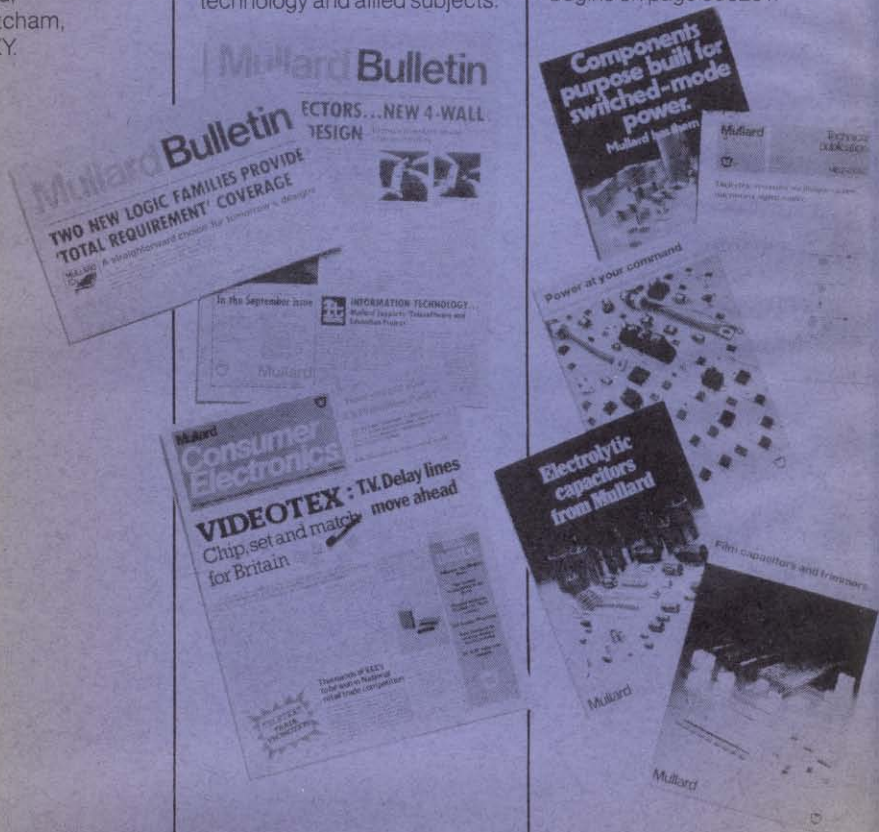
Technical Brochures and Range Leaflets

Mullard publish hundreds of different brochures on components and their application. Make sure your name is on the mailing list for the Mullard Bulletin, which describes and offers new publications.

Prestel too!

Mullard publications may also be ordered directly through PRESTEL.

The Mullard data base begins on page 556201.



Electronic Components and Applications

A quarterly technical journal covering, in depth, developments in electronics based on the work of Philips, Signetics and Mullard laboratories. Please ask for a sample copy and subscription form.

Quick reference guides

All products marketed by Mullard are listed alpha-numerically and described briefly in these guides. Part 1 covers passive components, discrete semiconductors, and valves and tubes; Part 2 deals with integrated circuits, including Signetics.

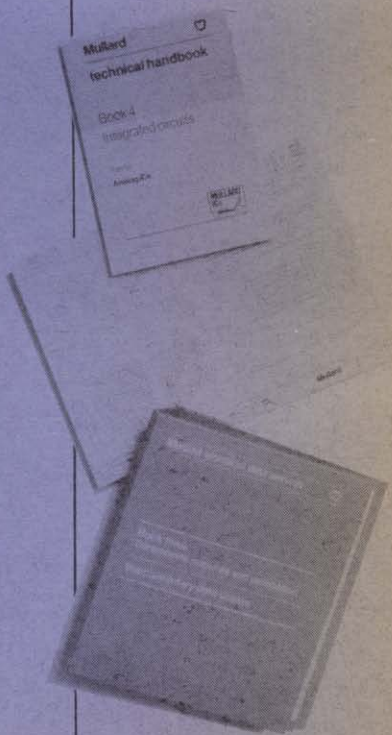
Technical Data Service

This service provides detailed, up-to-date information on the characteristics and performance of Mullard components.

Subscribers to any or all of the four handbook sections receive all relevant handbooks, looseleaf binders, monthly mailings of new data sheets, and new handbook parts as they are published.

For those not wishing to subscribe to the Data Service, handbook parts can be purchased individually.

Individual data sheets are available free-of-charge, and can be obtained by quoting the type number.



FUNCTIONAL AND NUMERICAL INDEX
MAINTENANCE TYPE LIST

SELECTION GUIDE BY FUNCTION

SELECTION GUIDE BY FUNCTION (continued)

NUMERICAL INDEX

NUMERICAL INDEX (continued)

MAINTENANCE TYPE LIST

SAA1114; Z
SAK140
TAA960
TAA970
TBA221D

TBA915 — successor type: TBA915G
TCA410A; B; D
TCA580
TCA680; B; D
TCA980 — successor type: TCA980G

TDA0301D
TDA0319D
TDA0324D
TDA0358D
TDA0555D

TDA0723D
TDA0741D
TDA0748D
TDA1034; N
TDA1034B; NB

TDA1034D; ND
TDA1458D
TDA3082
TDA4250B; D

GENERAL

Type designation
Rating systems

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

The FIRST LETTER divides the solitary circuits into:

S : Solitary digital circuits
T : Analogue circuits
U : Mixed analogue/digital circuits

The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

MA : { Microcomputer / Central processing unit
MB : Slice processor (see note 2)
MD : Correlated memories
ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

The FIRST TWO LETTERS identify the following:

NH : Hybrid circuits
NL : Logic circuits
NM : Memories
NS : Analogue signal processing, using switched capacitors
NT : Analogue signal processing, using CTDs
NX : Imaging devices
NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

PACKAGE OUTLINES

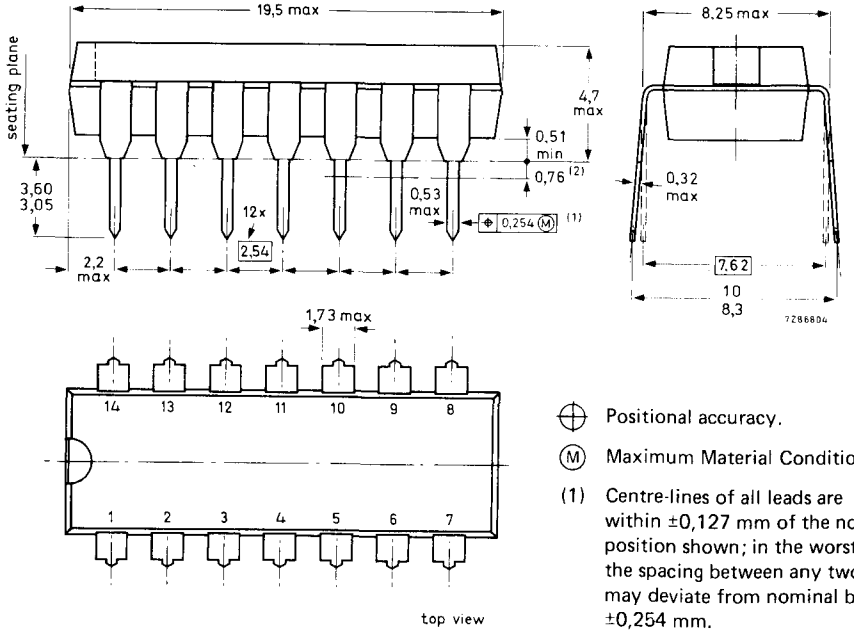
PACKAGE OUTLINES

In this chapter the package outlines are given for the following types, except for those marked with an asterisk which are included in the device data sheet.

type number	package code	description
CA3046	SOT-27T	14-lead dual in-line; plastic (SOT-27K, M, T)
SAA1027	SOT-38A	16-lead dual in-line; plastic (SOT-38A)
SAA1029	SOT-38	16-lead dual in-line; plastic (SOT-38)
SAK150BT	SO-14; SOT-108A	14-lead mini-pack; plastic (SO-14; SOT-108A)
TBA673*	SOT-14	10-lead cylindrical; metal (TO-74; reduced height; SOT-14)
TBA915G	SOT-110B	9-lead single in-line; plastic (SOT-110B)
TCA210	SOT-38	16-lead dual in-line; plastic (SOT-38)
TCA210T	SO-14; SOT-108A	14-lead mini-pack; plastic (SO-14; SOT-108A)
TCA220	SOT-38	16-lead dual in-line; plastic (SOT-38)
TCA240	SOT-38	16-lead dual in-line; plastic (SOT-38)
TCA240D	SO-16; SOT-109A	16-lead mini-pack; plastic (SO-16; SOT-109A)
TCA280A	SOT-38	16-lead dual in-line; plastic (SOT-38)
TCA520B	SOT-97A	8-lead dual in-line; plastic (SOT-97A)
TCA520D	SO-8; SOT-96A	8-lead mini-pack; plastic (SO-8; SOT-96A)
TCA770A	SOT-38	16-lead dual in-line; plastic (SOT-38)
TCA770D	SO-14; SOT-108A	14-lead mini-pack; plastic (SO-14; SOT-108A)
TCA980G	SOT-110B	9-lead single in-line; plastic (SOT-110B)
TDA1023	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA1024	SOT-97A	8-lead dual in-line; plastic (SOT-97A)
TDA1060	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA1060A	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA1060B	SOT-74	16-lead dual in-line; ceramic (cerdip) (SOT-74)
TDA1540D	SOT-135A	28-lead dual in-line; ceramic (cerdip) (SOT-135A)
TDA3081	SOT-38Z	16-lead dual in-line; plastic (SOT-38Z)
TDA3083	SOT-38Z	16-lead dual in-line; plastic (SOT-38Z)
TDA3083D	SO-16; SOT-109A	16-lead mini-pack; plastic (SO-16; SOT-109A)
TDB1080	SOT-38S	16-lead dual in-line; plastic (SOT-38, S)
TEA1010	SOT-97C2	8-lead dual in-line; plastic (SOT-97A, C2)
TEA1010T	SO-8; SOT-96AC1	8-lead mini-pack; plastic (SO-8; SOT-96A, AC1)
TEA1016	SOT-38	16-lead dual in-line; plastic (SOT-38)
TEA1017	SOT-102HE	18-lead dual in-line; plastic (SOT-102HE)
TEA1021P	SOT-38	16-lead dual in-line; plastic (SOT-38)
TEA1021D	SOT-74B	16-lead dual in-line; ceramic (cerdip) (SOT-74, B)
TEA1039	SOT-110B	9-lead single in-line; plastic (SOT-110B)
TEA1042	SOT-101A	24-lead dual in-line; plastic (SOT-101A)
TEA1043P	SOT-38	16-lead dual in-line; plastic (SOT-38)
TEA1043D	SOT-74B	16-lead dual in-line; ceramic (cerdip) (SOT-74, B)
TEA1044P	SOT-102A	18-lead dual in-line; plastic (SOT-102A)
TEA1044D	SOT-133	18-lead dual in-line; ceramic (cerdip) (SOT-133)
TEA1046P	SOT-101A	24-lead dual in-line; plastic (SOT-101A)

type number	package code	description
TEA1046D	SOT-149	24-lead dual in-line; ceramic (cerdip) (SOT-149)
TEA1053	SOT-102A	18-lead dual in-line; plastic (SOT-102A)
TEA1054	SOT-102A	18-lead dual in-line; plastic (SOT-102A)
TEA1055	SOT-102A	18-lead dual in-line; plastic (SOT-102A)
TEA1058	SOT-97C2	8-lead dual in-line; plastic (SOT-97A, C2)
TEA1058T	SO-8; SOT-96AC1	8-lead mini-pack; plastic (SO-8; SOT-96A, AC1)
TEA1060	SOT-102A	18-lead dual in-line; plastic (SOT-102A)
TEA1061	SOT-102A	18-lead dual in-line; plastic (SOT-102A)
TEA1062	SOT-38	16-lead dual in-line; plastic (SOT-38)
TEA1063	SOT-38	16-lead dual in-line; plastic (SOT-38)

14-LEAD DUAL IN-LINE; PLASTIC (SOT-27K,M,T)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

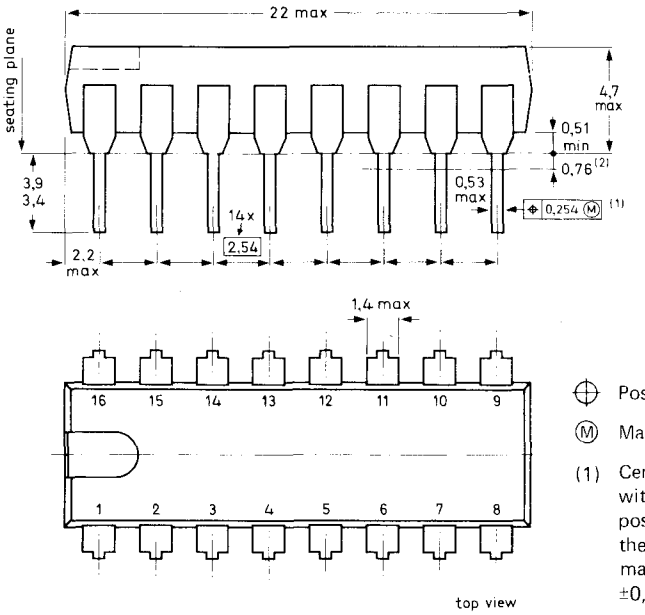
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves *must not exceed 5 seconds.*
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38,S)



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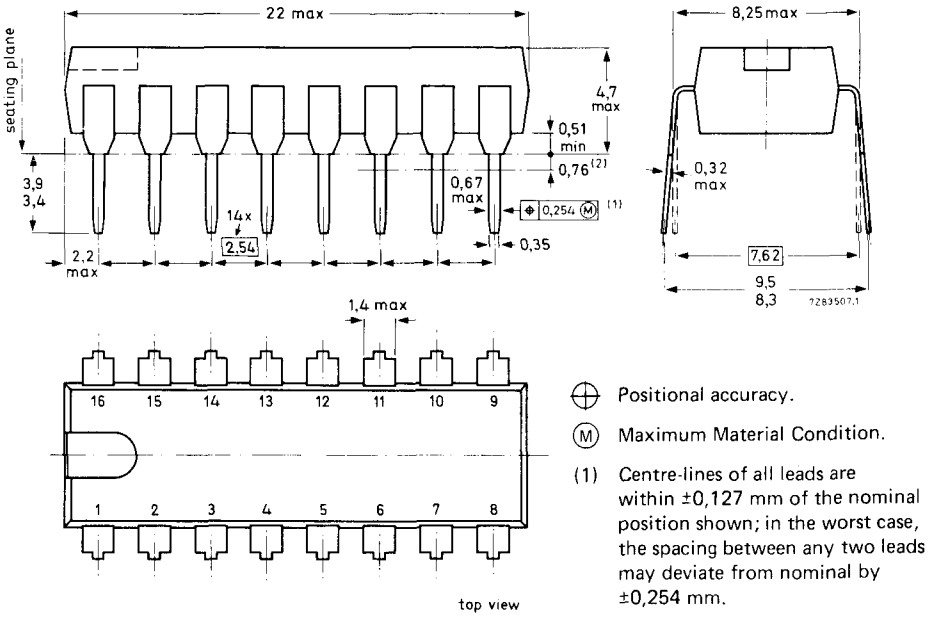
3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38A)



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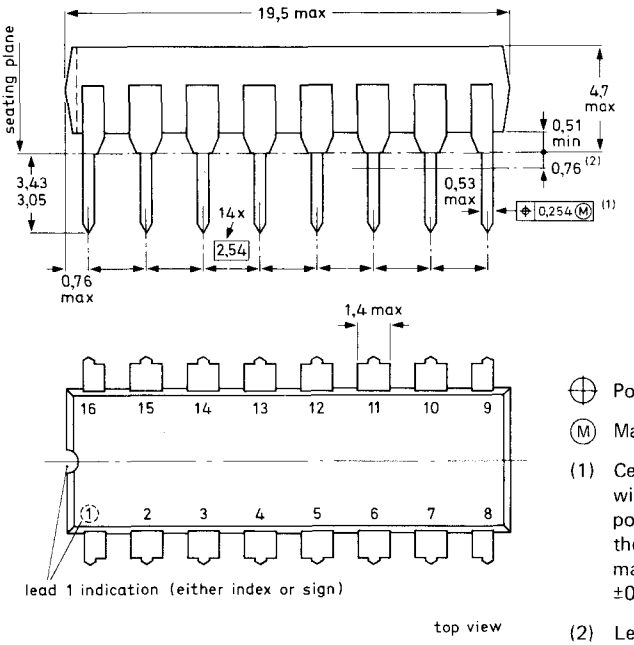
3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38Z)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

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Dimensions in mm

SOLDERING

1. By hand

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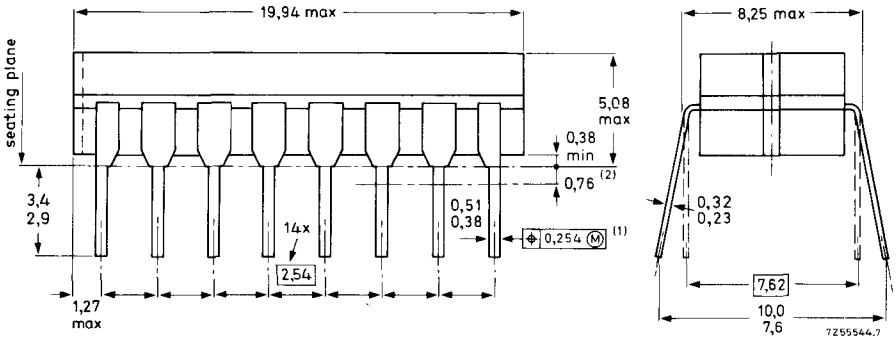
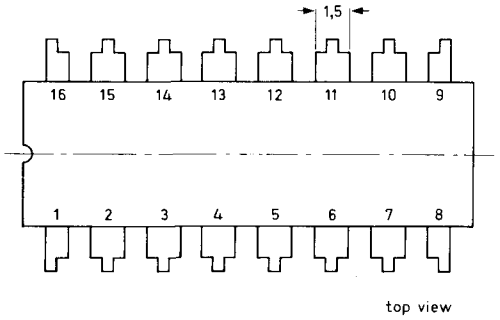
3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; CERAMIC (CERDIP)(SOT-74,B)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

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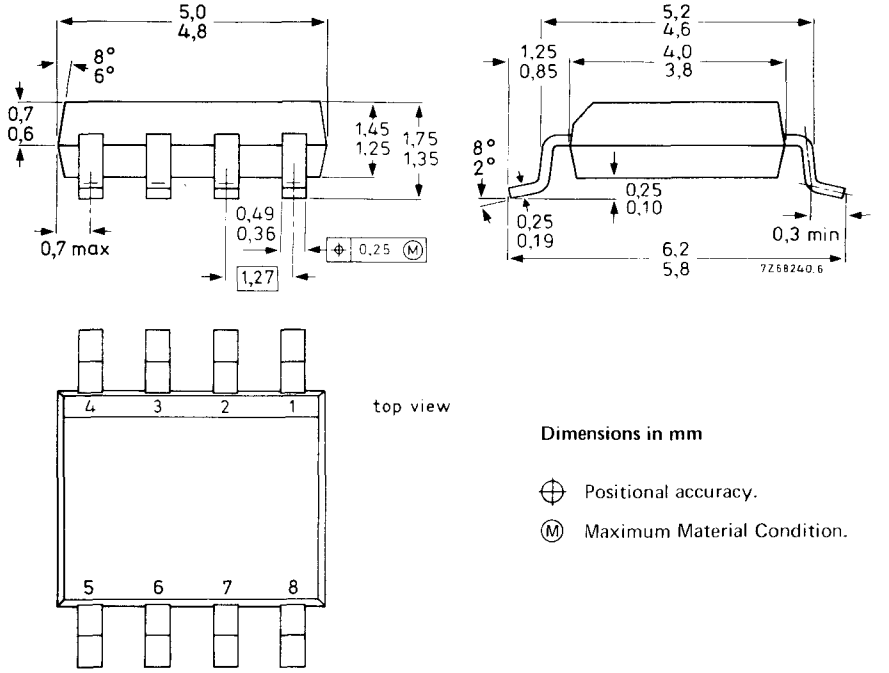
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO-8; SOT-96A,AC1)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

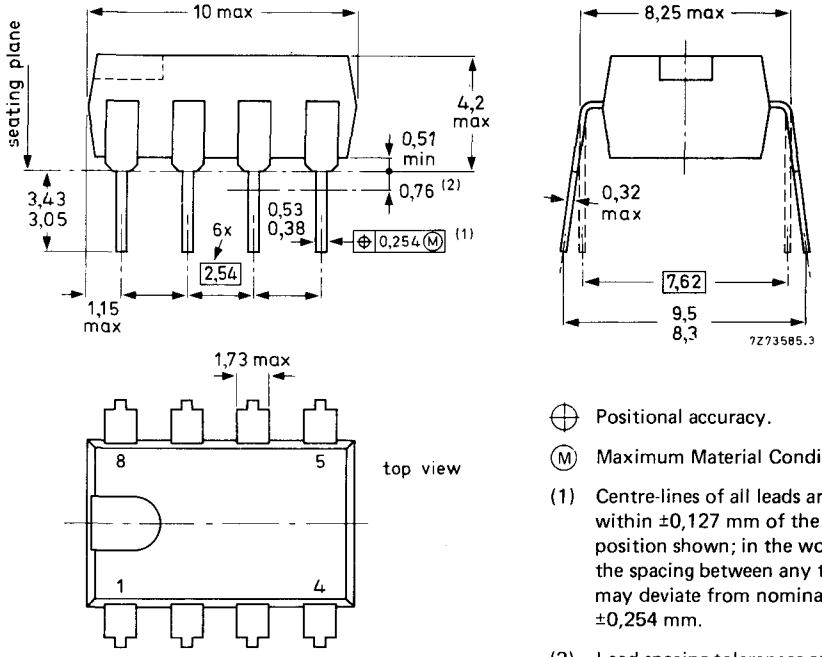
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

8-LEAD DUAL IN-LINE; PLASTIC (SOT-97A,C2)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

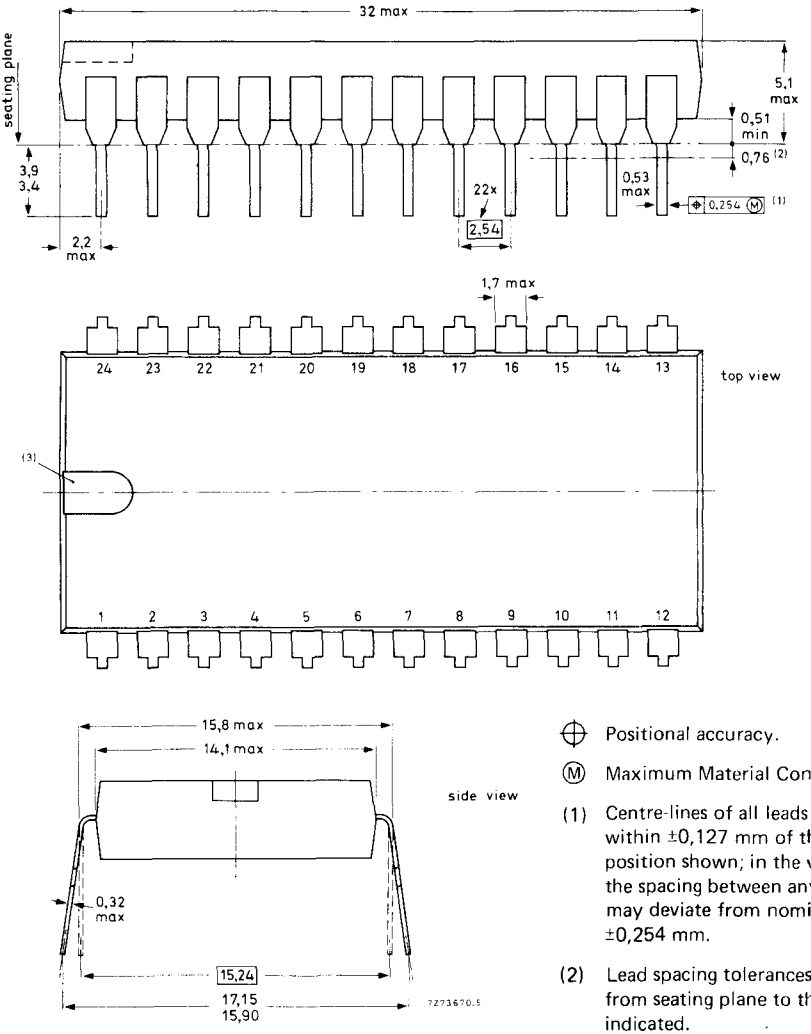
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

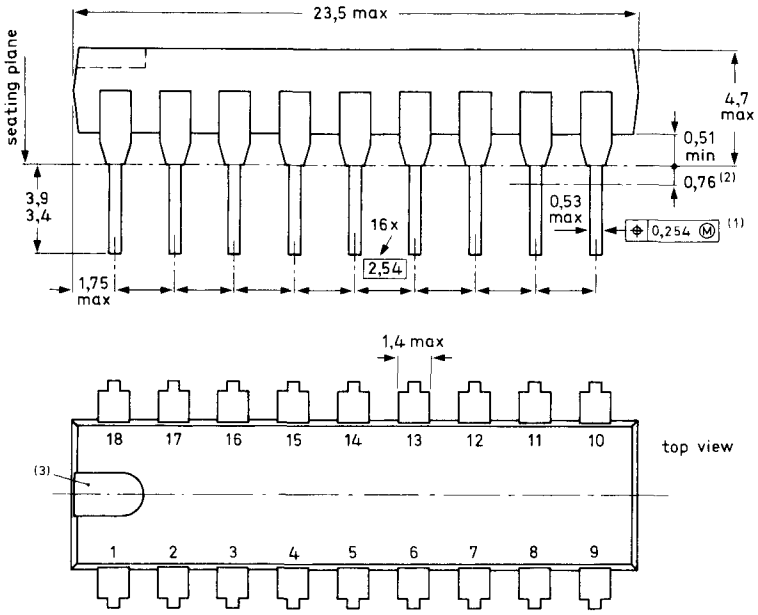
(3) Index may be horizontal as shown, or vertical.

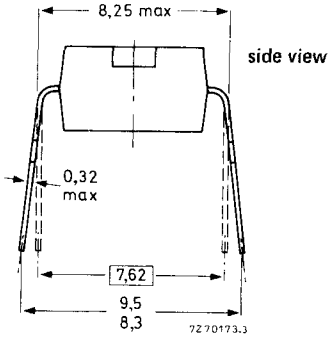
Dimensions in mm

SOLDERING

See page 17 of this chapter (SOT-27K, M, T).

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

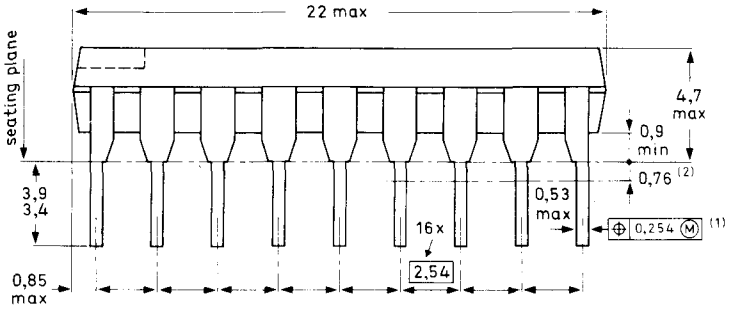
(3) Index may be horizontal as shown, or vertical.

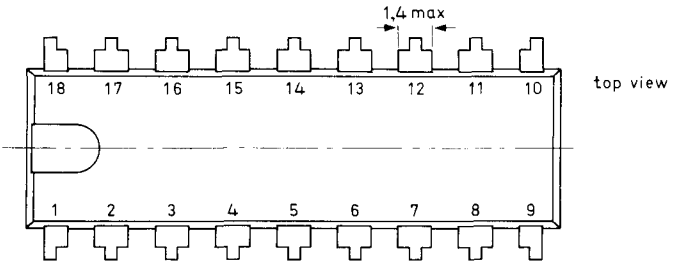
Dimensions in mm

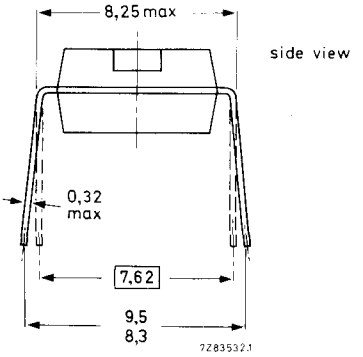
SOLDERING

See page 17 of this chapter (SOT-27K, M, T).

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102HE)







⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

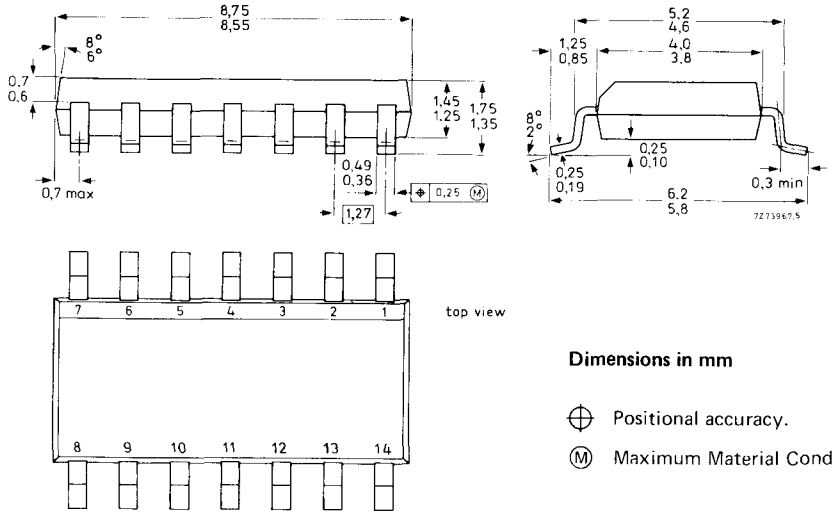
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

See page 17 of this chapter (SOT-27K, M, T).

14-LEAD MINI-PACK; PLASTIC (SO-14; SOT-108A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

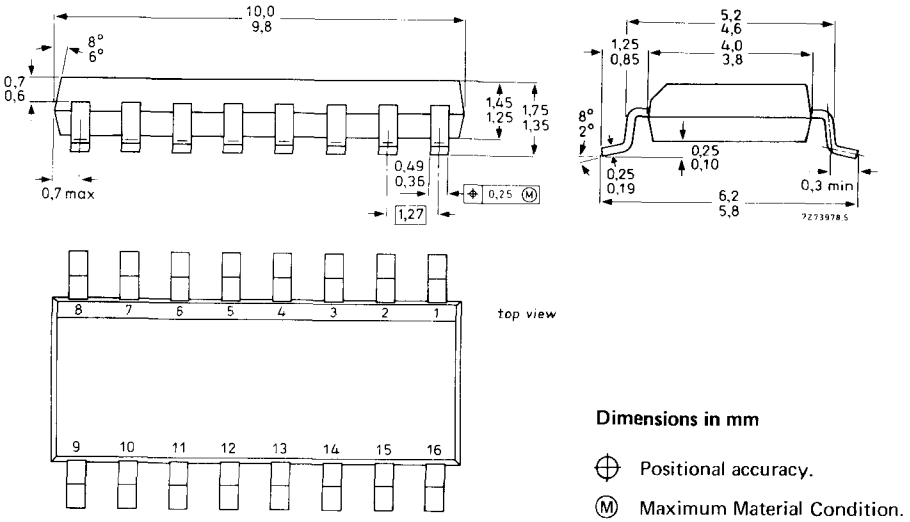
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

16-LEAD MINI-PACK; PLASTIC (SO-16; SOT-109A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

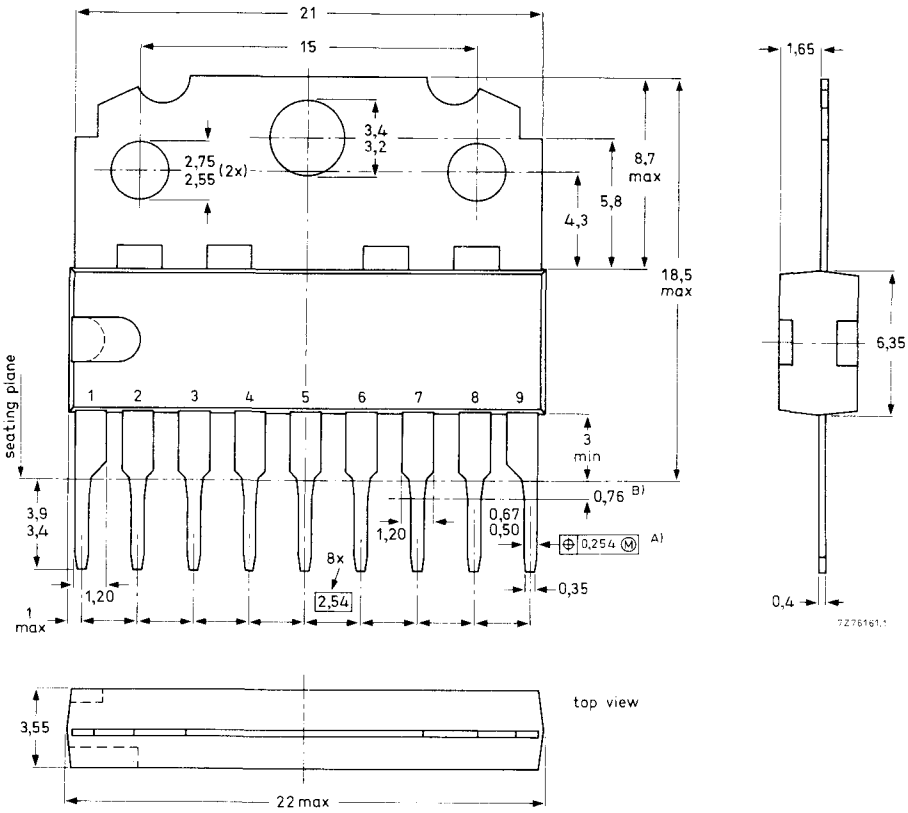
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

9-LEAD SINGLE IN-LINE; PLASTIC (SOT-110B)



Dimensions in mm

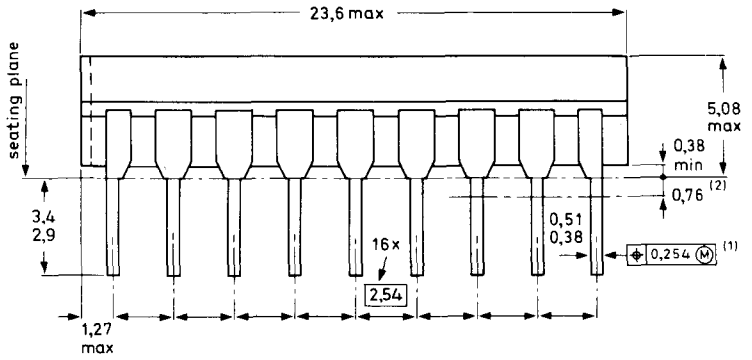
⊕ Positional accuracy.

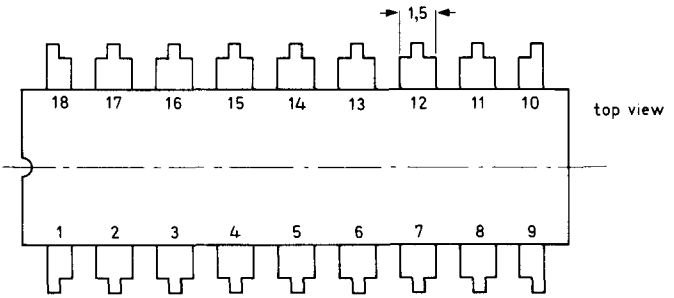
Ⓜ Maximum Material Condition.

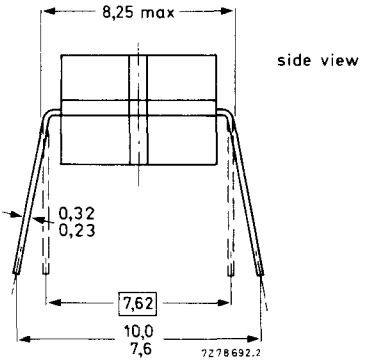
A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

18-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-133)







⊕ Positional accuracy.

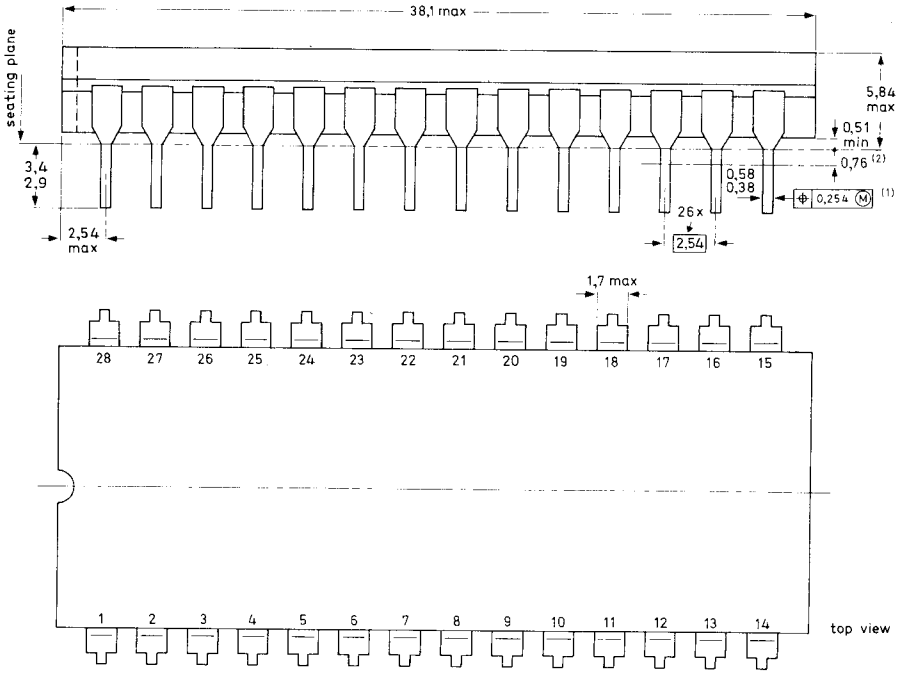
Ⓜ Maximum Material Condition.

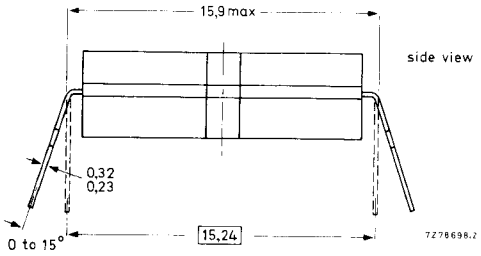
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-135A)





⊕ Positional accuracy.

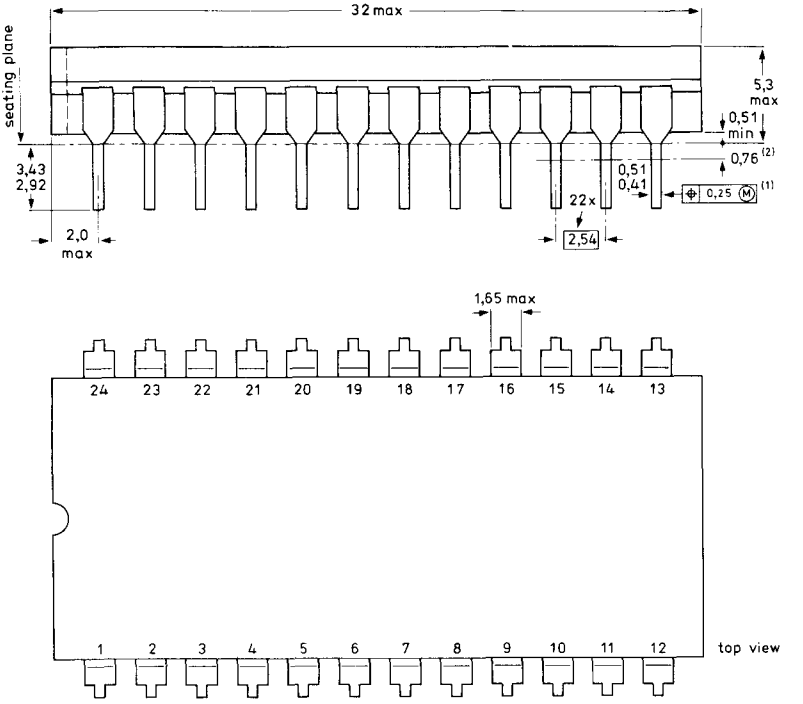
Ⓜ Maximum Material Condition.

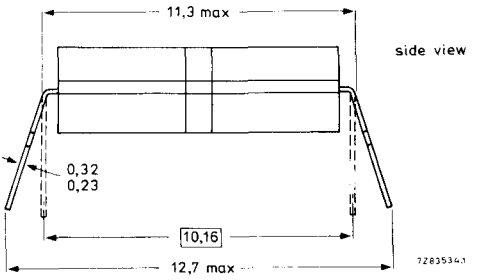
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

24-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-149)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

OPERATIONAL AMPLIFIERS

TRIPLE OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The TCA220 is a bipolar integrated circuit consisting of three identical high-gain amplifiers. The amplifiers have differential inputs and an emitter-follower output which can deliver up to 100 mA output current. The unity-gain frequency with 6 dB/octave compensation is at least 5 MHz. No latch-up will occur when the input voltage range is exceeded.

QUICK REFERENCE DATA

Supply voltages				
positive	V_{CC}	nom.	6	V
negative	$-V_{EE}$	nom.	6	V
Supply current, unloaded	$I_{CC} + I_{RX}$	typ.	1,4	mA
Large-signal voltage amplification	A_{VD}	typ.	4000	
Slew rate	S_{VOAV}	typ.	0,4	V/μs
Input voltage range	V_I	−4,3 to	+5,6	V
Input offset voltage	V_{IO}	typ.	2	mV
Input offset current	I_{IO}	typ.	0,2	μA
Common-mode rejection ratio	k_{CMR}	typ.	90	dB
Supply-voltage rejection ratio	k_{SVR}	typ.	75	dB
Operating ambient temperature range	T_{amb}	−55 to	+125	°C

PACKAGE OUTLINES

16-lead DIL; plastic (SOT-38).

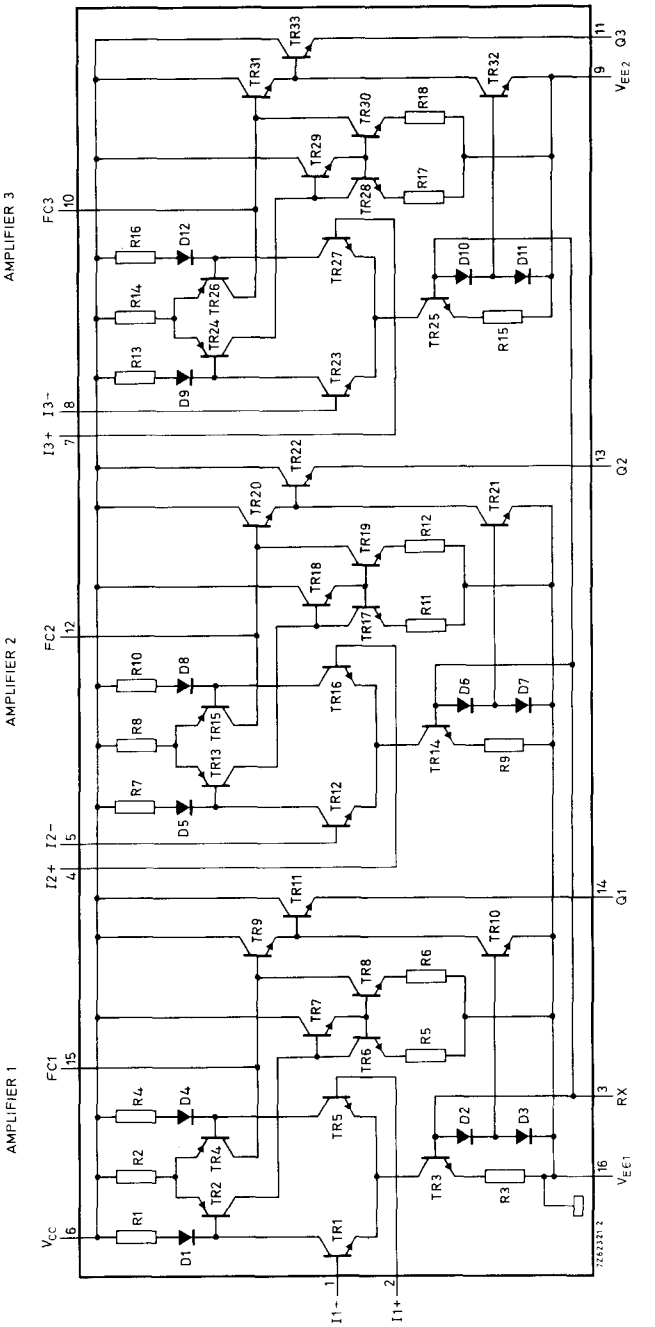


Fig. 1 Circuit diagram.

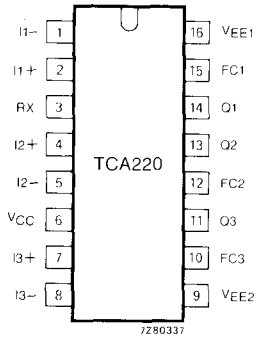


Fig. 2 Pinning diagram.

PINNING

1	I1−	inverting input, amplifier 1
2	I1+	non-inverting input, amplifier 2
3	RX	external resistor
4	I2+	non-inverting input, amplifier 2
5	I2−	inverting input, amplifier 2
6	V_{CC}	positive supply
7	I3+	non-inverting input, amplifier 3
8	I3−	inverting input, amplifier 3
9	V_{EE2}	negative supply, amplifier 3
10	FC3	frequency compensation, amplifier 3
11	Q3	output, amplifier 3
12	FC2	frequency compensation, amplifier 2
13	Q2	output, amplifier 2
14	Q1	output, amplifier 1
15	FC1	frequency compensation, amplifier 1
16	V_{EE1}	negative supply, amplifiers 1 and 2

FUNCTIONAL DESCRIPTION

Supply

The TCA220 requires a positive and a negative supply. V_{CC} is the common positive supply to the three amplifiers. V_{EE1} is the common negative supply to amplifiers 1 and 2, which always has to be connected to the negative supply. V_{EE2} is a separate negative supply for amplifier 3, which should be left open when this amplifier is not used.

External resistor; RX

The current level in the amplifiers is determined by current sources. These current sources need a minimum current into RX of 200 μA. This current is usually derived from the positive supply via an external resistor.

Frequency compensation; FC1, FC2 and FC3

Each amplifier may be frequency compensated by connecting an RC network from its FC to its V_{EE} (see Fig. 4).

Outputs Q1, Q2 and Q3

The outputs are emitter followers with open-emitter outputs which require an external load resistor.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	$V_{CC} - V_{EE}$	max.	18 V
Input voltage range	V_I	V_{EE} to V_{CC}	V
Differential-mode input d.c. voltage	$\pm V_{ID}$	max.	5 V
Input current	I_I	max.	0,5 mA
Current into RX	I_{RX}	max.	5 mA
Output current	$-I_O$	max.	100 mA
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range (see also Fig. 3)	T_{amb}	−55 to +125	°C

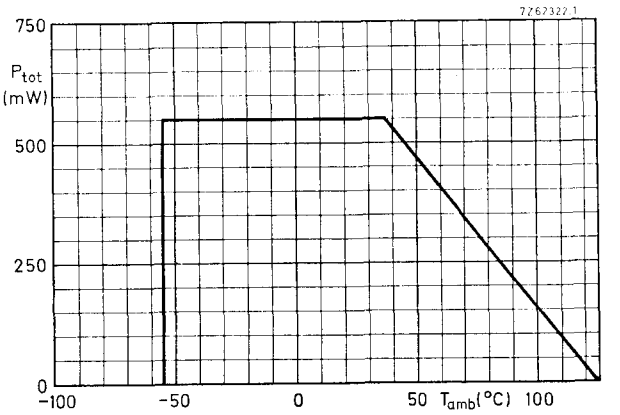


Fig. 3 Power derating curve.

CHARACTERISTICS

V_{CC} = 6 V; $-V_{EE}$ = 6 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage range	$V_{CC}-V_{EE}$	8	12	16	V
Supply current, V_Q = 0 V; unloaded	I_{CC}	--	1,2	3	mA
Supply-voltage rejection ratio* at R_S = 2 kΩ	k_{SVR}	–	75	–	dB
External resistor; RX					
Voltage with respect to negative supply	V_{RX-EE}	–	1,5	–	V
Current into RX	I_{RX}	200	–	–	mA
Inputs I + and I–					
Input voltage range	V_I	−4,3	–	+5,6	V
Input bias current	I_{IB}	–	1	2	μA
Differential input impedance	$\|z_{id}\|$	25	–	–	kΩ
Input offset voltage at R_S = 200 Ω max.	V_{IO}	–	2	10	mV
Input offset current	I_{IO}	--	0,2	--	μA
Common-mode rejection ratio at R_S = 2 kΩ; f = 1 kHz	k_{CMR}	–	90	–	dB
Outputs Q1, Q2 and Q3					
Output voltage range	V_Q	−6	–	+3,5	V
Large-signal differential-mode voltage amplification at $V_{Q(p-p)}$ = 7 V	A_{VD}	2000	4000	–	
variation with temperature at T_{amb} = −20 to + 70 °C	ΔA_{VD}	–	8	--	dB
Slew rate at unity gain	S_{VOAV}	–	0,4	–	V/μs
Gain-bandwidth product at 6 dB/octave compensation	f_1	5	–	–	MHz
Broadband noise figure at R_S = 2 kΩ; f = 10 Hz to 10 kHz	F_{AV}	–	4	–	dB
Channel separation at R_S = 2 kΩ; f = 10 kHz (see Fig. 5)					
from amplifier 1 to amplifier 2		--	94	–	dB
from amplifier 1 to amplifier 3		–	130	–	dB
from amplifier 2 to amplifier 1		--	94	--	dB
from amplifier 2 to amplifier 3		–	110	–	dB
from amplifier 3 to amplifier 1		–	130	–	dB
from amplifier 3 to amplifier 2		–	110	--	dB

* The supply-voltage rejection ratio is the ratio of the change in input offset voltage to the change in supply voltages producing it.

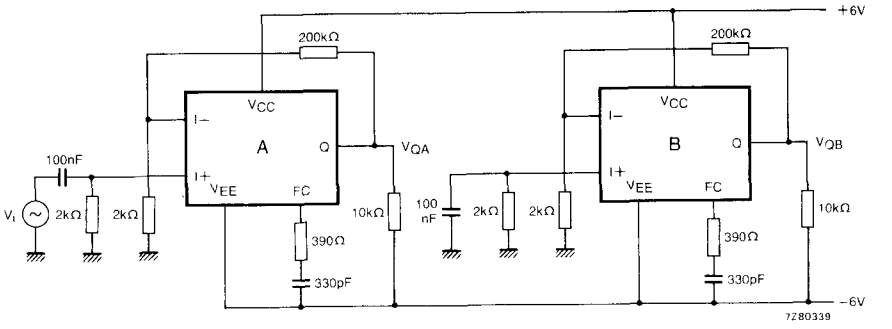


Fig. 4 Test circuit for channel separation. Channel separation from amplifier A to amplifier B is defined as:

$$20 \log \frac{V_{QA}}{V_{QB}} \times A_{c1B}.$$

A_{c1B} being the closed-loop gain of amplifier B; in this case $A_{c1B} = 100$.

APPLICATION INFORMATION

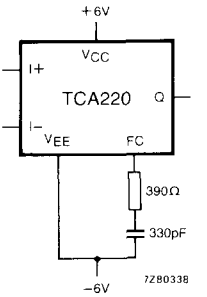


Fig. 5 Frequency compensation circuit.

OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The TCA520 is a bipolar integrated operational amplifier primarily intended for low-power, low-voltage applications and as a comparator in digital systems.

Features

- wide supply voltage range
- low supply voltage operation
- low power consumption
- low input bias current
- offset compensation facility
- frequency compensation facility
- high slew rate
- large output voltage swing
- TTL compatible output

QUICK REFERENCE DATA

Supply voltage range	V_{CC}	2 to 20	V
Supply current	I_{CC}	typ. 0,8	mA
Input bias current	I_{IB}	typ. 60	nA
Output voltage range	V_O	0,1 to V_{CC}–0,1	V
D.C. differential voltage amplification	A_{VD}	typ. 15 000	
Slew rate	S_{VOAV}	typ. 25	V/μs
Operating ambient temperature range	T_{amb}	–25 to + 85	°C

PACKAGE OUTLINES

TCA520B : 8-lead DIL; plastic (SOT-97A).
TCA520D: 8-lead mini-pack; plastic (SO-8; SOT-96A).

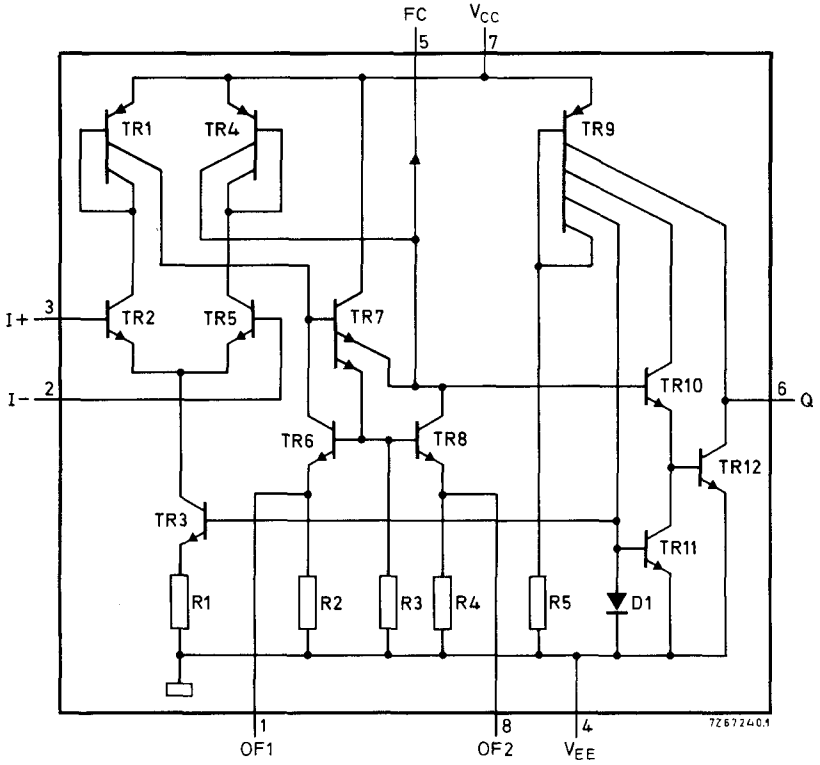


Fig. 1 Circuit diagram.

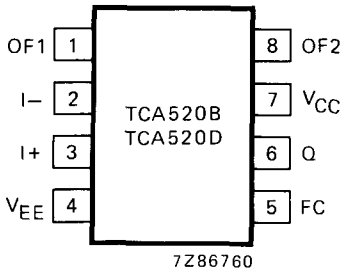


Fig. 2 Pinning diagram.

PINNING

1	OF1	offset compensation connection
2	I−	inverting input
3	I+	non-inverting input
4	V_{EE}	ground connection
5	FC	frequency compensation connection
6	Q	output
7	V_{CC}	positive supply connection
8	OF2	offset compensation connection

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC}	max.	22 V
Input voltage	V_I	max.	V_{CC} V
	$-V_I$	max.	0 V
Differential input voltage	$\pm V_{ID}$	max.	7 V
Power dissipation at T_{amb} = 85 °C	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}		−55 to + 125 °C
Operating ambient temperature range	T_{amb}		−25 to + 85 °C

CHARACTERISTICS

V_{CC} = 5 V; V_{EE} = 0 V; T_{amb} = 25 °C; R_L from Q to V_{CC} unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply V_{CC}; pin 7					
Supply current, unloaded	I_{CC}	0,5	0,8	1,2	mA
Inputs I+ and I−; pins 3 and 2					
Input voltage	V_I	0,9	–	V_{CC}−0,5	V
Input bias current	I_{IB}	–	60	250	nA
Input offset voltage	V_{IO}	–	1	6	mV
Variation with temperature	ΔV_{IO}	–	5	–	μV/K
Input offset current	I_{IO}	–	10	75	nA
Common-mode rejection ratio	k_{CMR}	70	100	–	dB
Input noise voltage at f = 1 kHz	$V_{n(rms)}$	–	15	–	nV/√Hz
Input noise current at f = 1 kHz	$I_{n(rms)}$	–	0,4	–	pA/√Hz
Output Q; pin 6					
Output voltage range at R_L = 5 kΩ	V_Q	0,1	–	V_{CC}−0,1	V
Output current					
HIGH at $V_Q = V_{CC} - 0{,}4$ V	$-I_{OH}$	100	200	–	μA
LOW at V_Q = 0,4 V	I_{OL}	6	12	–	mA
D.C. voltage amplification at R_L = 5 kΩ	A_{VD}	10 000	15 000	–	
A.C. voltage amplification at f = 1 kHz; C_{FC} = 100 pF	A_{vd}	–	58	–	dB
Slew rate (average rate of change of the output voltage) at R_L = 1 kΩ					
C_{FC} = 0 pF	S_{VOAV}	–	25	–	V/μs
C_{FC} = 100 pF	S_{VOAV}	–	500	–	mV/μs

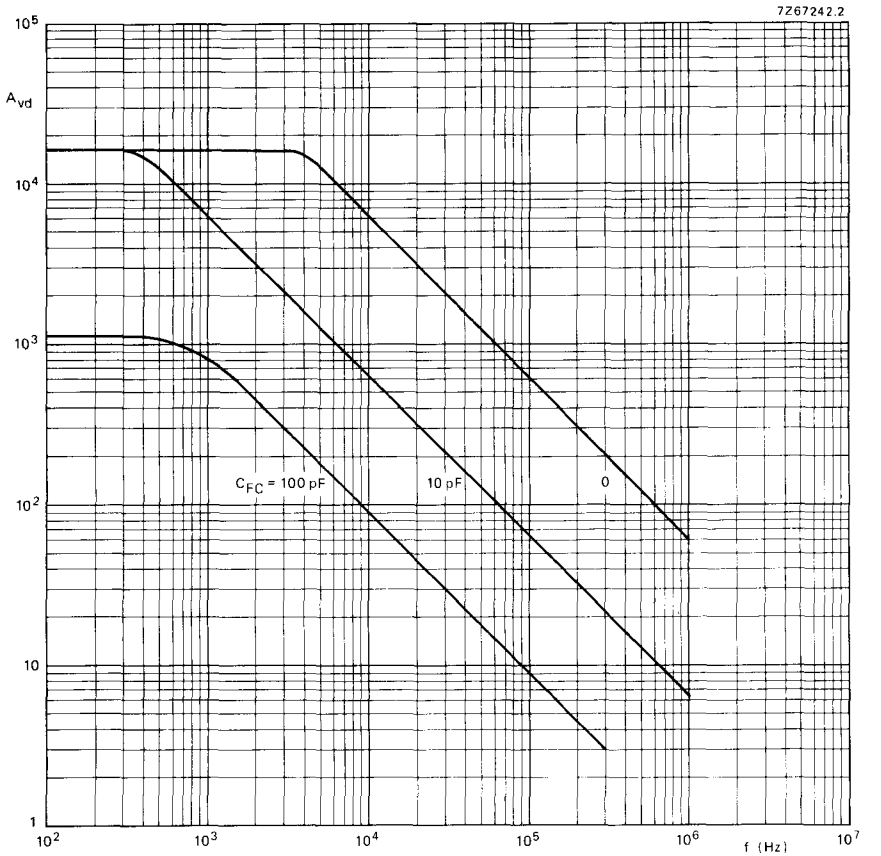


Fig. 3 Typical values of the open-loop voltage amplification as a function of frequency.

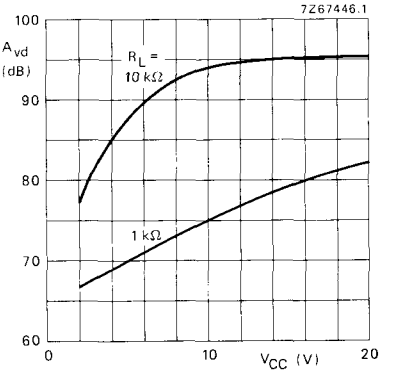


Fig. 4 Typical values of the open-loop voltage amplification as a function of supply voltage.

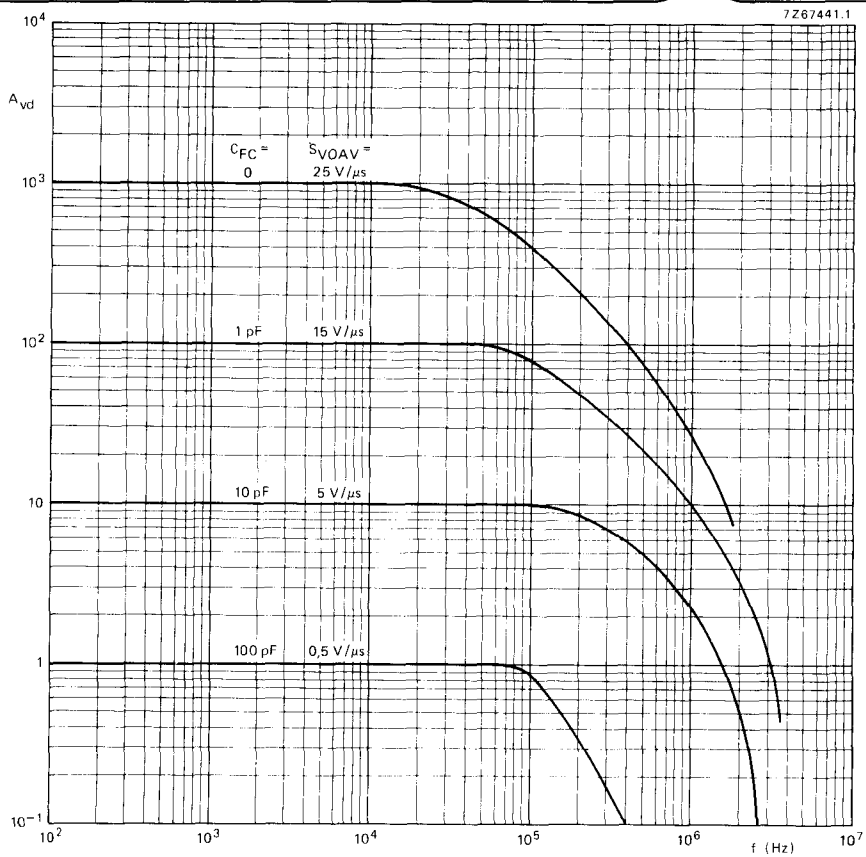


Fig. 5 Typical frequency response and slew rate for various closed-loop gains.

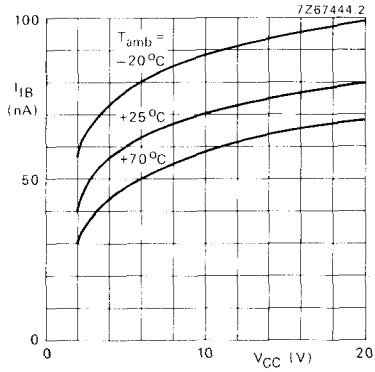


Fig. 6 Typical values of the input bias current as a function of supply voltage, with ambient temperature as a parameter.

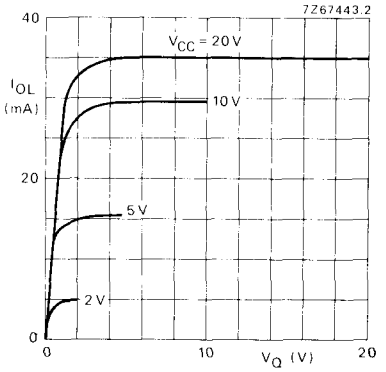


Fig. 7 Output current LOW as a function of output voltage, with supply voltage as a parameter.

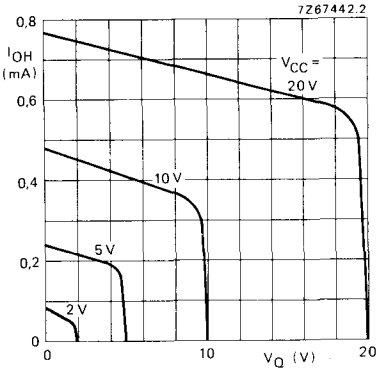


Fig. 8 Output current HIGH as a function of output voltage, with supply voltage as a parameter.

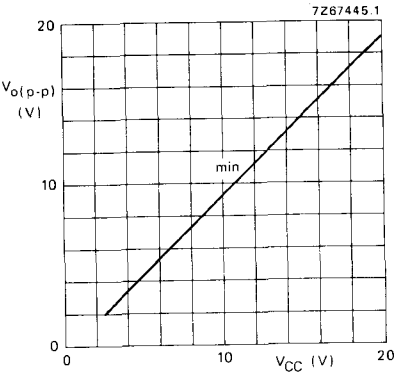


Fig. 9 Minimum values of the output voltage swing as a function of supply voltage for R_L = 1 kΩ.

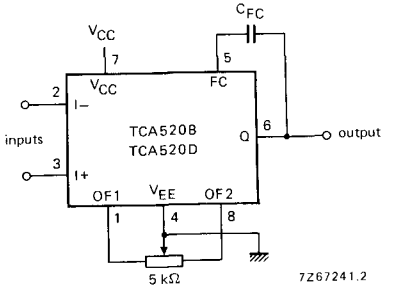


Fig. 10 Typical arrangement of the TCA520 with frequency and offset compensation.

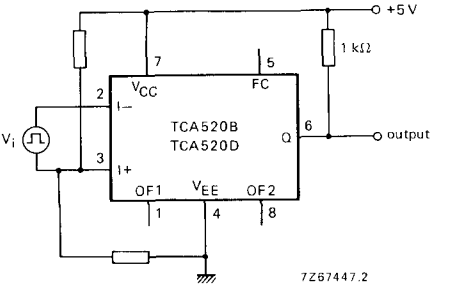


Fig. 11 Typical application of the TCA520 as a comparator.

DUAL OP-AMP AND COMPARATOR

GENERAL DESCRIPTION

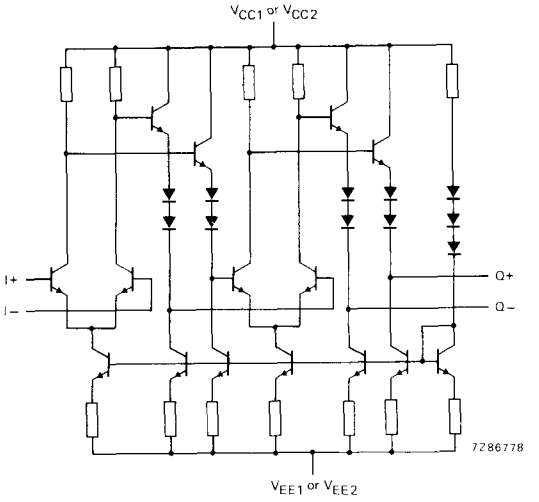
The TEA1016 is a bipolar integrated circuit containing two operational amplifiers and a high-speed comparator. The circuit requires a single 5 V supply, this makes it especially suited for digital applications. The comparator has a level-shifted output for driving an external switching transistor. With this transistor the circuit is TTL compatible; the transistor may also drive a transmission line.

QUICK REFERENCE DATA

Supply voltage range	V_{CC1}; V_{CC2}	4,75 to	5,25	V
Supply current	$I_{CC1} + I_{CC2}$	typ.	28	mA
Open-loop differential voltage amplification				
amplifiers	A_{vd}	typ.	43,5	dB
comparator	A_{vd}	min.	47	dB
Input offset voltage	V_{IO}	max.	5	mV
Input offset current				
amplifiers	I_{IO}	max.	5	μA
comparator	I_{IO}	max.	6	μA
Comparator total response time	$t_{tot(r)}$, $t_{tot(f)}$	max.	60	ns
Operating ambient temperature range	T_{amb}	−40 to	+105	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).



(a)

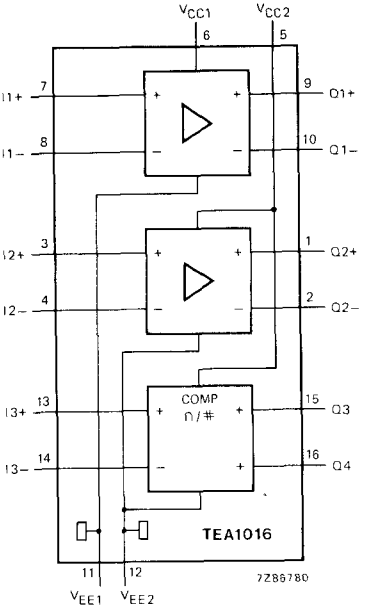
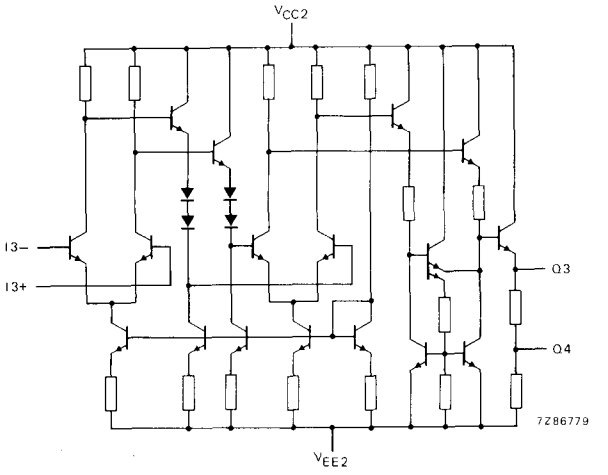


Fig. 2 Block diagram.



(b)

Fig. 1 Circuit diagram.
(a) one amplifier.
(b) comparator.

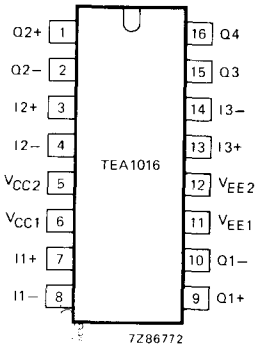


Fig. 3 Pinning diagram.

PINNING

1	Q2+	non-inverting output, amplifier 2
2	Q2−	inverting output, amplifier 2
3	I2+	non-inverting input, amplifier 2
4	I2−	inverting input, amplifier 2
5	V_{CC2}	positive supply, amplifier 2 and comparator
6	V_{CC1}	positive supply, amplifier 1
7	I1+	non-inverting input, amplifier 1
8	I1−	inverting input, amplifier 1
9	Q1+	non-inverting output, amplifier 1
10	Q1−	inverting output, amplifier 1
11	V_{EE1}	ground, amplifier 1
12	V_{EE2}	ground, amplifier 2 and comparator
13	I3+	non-inverting input, comparator
14	I3−	inverting input, comparator
15	Q3	direct comparator output
16	Q4	level-shifted comparator output

DEVELOPMENT SAMPLE DATA

FUNCTIONAL DESCRIPTION

Supply

The TEA1016 requires a single 5 V supply. The first operational amplifier has separate supply and ground pins. If only one operational amplifier is to be used, than V_{CC1} may be left open.

Amplifier outputs Q1+, Q1−, Q2+ and Q2−

The amplifiers have complementary outputs. The outputs are emitter followers with current sources to ground.

Comparator outputs Q3 and Q4

The comparator has a single emitter follower output stage with a resistor to ground. Q3 is the emitter output, Q4 is a tap on the resistor which provides a level shift. This output is intended to drive an external transistor directly. This transistor will produce a TTL compatible signal; it may even drive a transmission line.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC1}, V_{CC2}	max.	6 V
Input voltage, all inputs	V_I	max.	V_{CC} V
Output current, all outputs	$-I_O$	max.	10 mA
Total power dissipation	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}	−40 to +125	°C
Operating ambient temperature range	T_{amb}	−40 to +105	°C

CHARACTERISTICS

$V_{CC1} = V_{CC2} = 4{,}75$ to 5,25 V; $V_{EE1} = V_{EE2} = 0$ V; $T_{amb} = -40$ to $+105$ °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply: V_{CC1} and V_{CC2}; pins 5 and 6					
Supply current	$I_{CC1}+I_{CC2}$	15	28	40	mA
Amplifier inputs I1+, I1−, I2+ and I2−; pins 7, 8, 3 and 4					
Input voltage	V_I	1,5	–	3,7	V
Input bias current	I_{IB}	0	10	80	μA
Input impedance at f = 1 kHz	$\lvert z_{is}\rvert$	3	–	30	kΩ
Input offset voltage	V_{IO}	−5	0	5	mV
Input offset current	I_{IO}	−5	0	5	μA
Amplifier outputs Q1+, Q1−, Q2+ and Q2−; pins 9, 10, 1 and 2					
Open-loop differential voltage amplification	A_{vd}	39	43,5	48	dB
Output voltage at $T_{amb} = 25$ °C					
HIGH	V_{OH}	2,2	2,8	3,6	V
LOW	V_{OL}	0,9	1,6	2,4	V
Output voltage swing	$V_{O(p-p)}$	0,35	–	1,5	V
at $T_{amb} = 25$ °C	$V_{O(p-p)}$	0,7	0,95	1,3	V
Comparator inputs I3+ and I3−; pins 13 and 14					
Input voltage	V_I	1,5	–	3,5	V
Input bias current	I_{IB}	0	10	40	μA
Input offset voltage	V_{IO}	−5	0	5	mV
Input offset current	I_{IO}	−6	0	6	μA
Comparator outputs Q3 and Q4; pins 15 and 16					
Open-loop differential voltage amplification to Q3	A_{vd}	47	–	–	dB
Output voltage Q4					
HIGH	V_{OH}	0,95	–	1,7	V
LOW	V_{OL}	–	–	250	mV
Output voltage ratio	V_{Q4}/V_{Q3}	0,53	–	0,6	
Output short-circuit current, Q4 at $V_{I3+} = 3$ V; $V_{I3-} = 2$ V; $V_{Q4} = 0$ V	I_{OS}	3	6,5	12	mA
Comparator total response time					
rising edge	$t_{tot(r)}$	–	30	60	ns
falling edge	$t_{tot(f)}$	–	30	60	ns

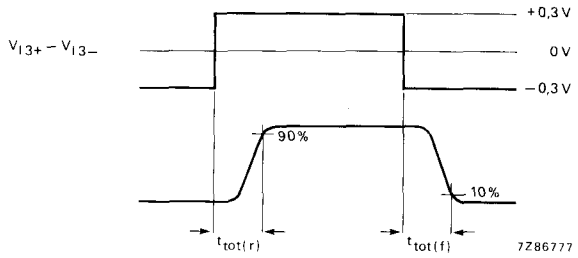


Fig. 4 Timing diagram of the comparator showing the total response times.

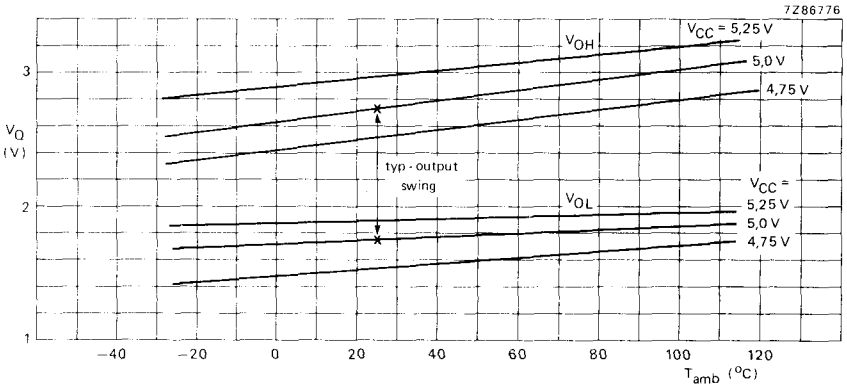


Fig. 5 Amplifier HIGH and LOW output voltage as a function of ambient temperature with the supply voltage V_{CC} as a parameter.

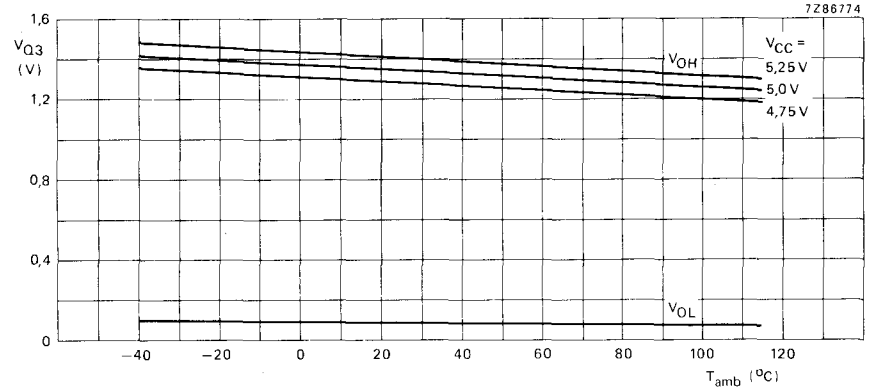


Fig. 6 Comparator output level at direct output Q3 as a function of ambient temperature with the supply voltage V_{CC} as a parameter.

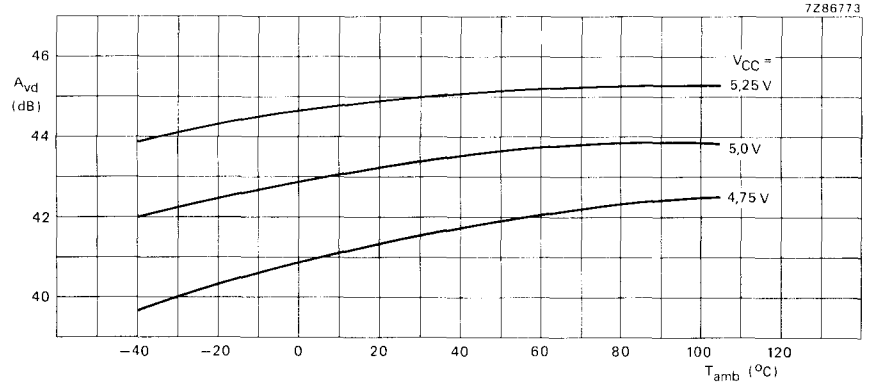


Fig. 7 Amplifier open-loop differential voltage amplification as a function of ambient temperature with the supply voltage V_{CC} as a parameter.

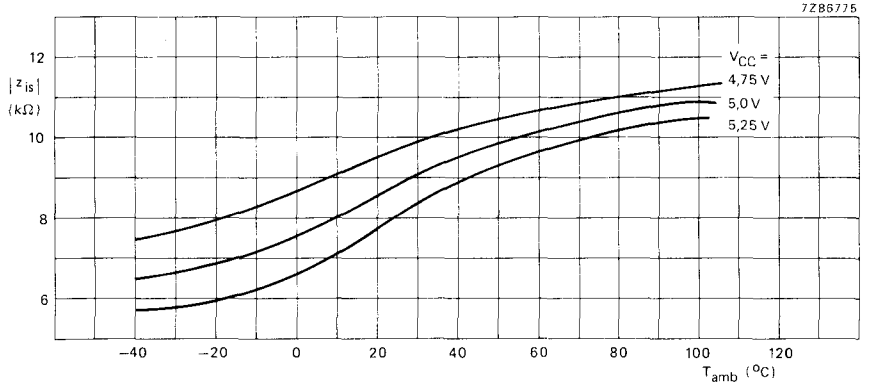


Fig. 8 Amplifier input impedance as a function of ambient temperature with the supply voltage V_{CC} as a parameter.

APPLICATION INFORMATION

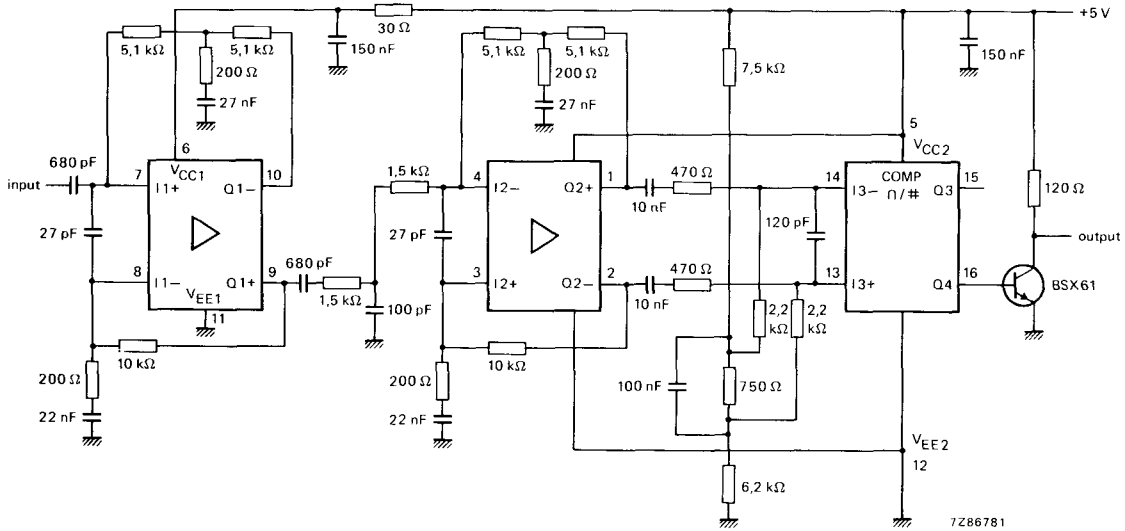


Fig. 9 Typical application of the TEA1016 as a band-pass filter with anti-noise threshold. In the absence of an input signal the collector of the switching transistor will be HIGH. Performance of the circuit at V_{CC} = 5 V, R_S = 3 kΩ, T_{amb} = 25 °C and f = 300 kHz:

Voltage amplification, each amplifier	A_{vd}	typ.	24 dB
Voltage amplification, two amplifiers	A_{vd}	typ.	49 dB
Amplifier frequency range, −3 dB limits	f	typ. 60 kHz to	1,1 MHz
Roll-off below 60 kHz and above 1,1 MHz	$\Delta A_{vd}/\Delta f$	typ.	12 dB/octave
Threshold of comparator stage		typ.	260 mV
Input voltage for clipped Q2+ and Q2− output signal	$V_{i(rms)}$	min.	3 mV
Input voltage for switched Q3 and Q4 output	$V_{i(rms)}$	min.	0,7 mV

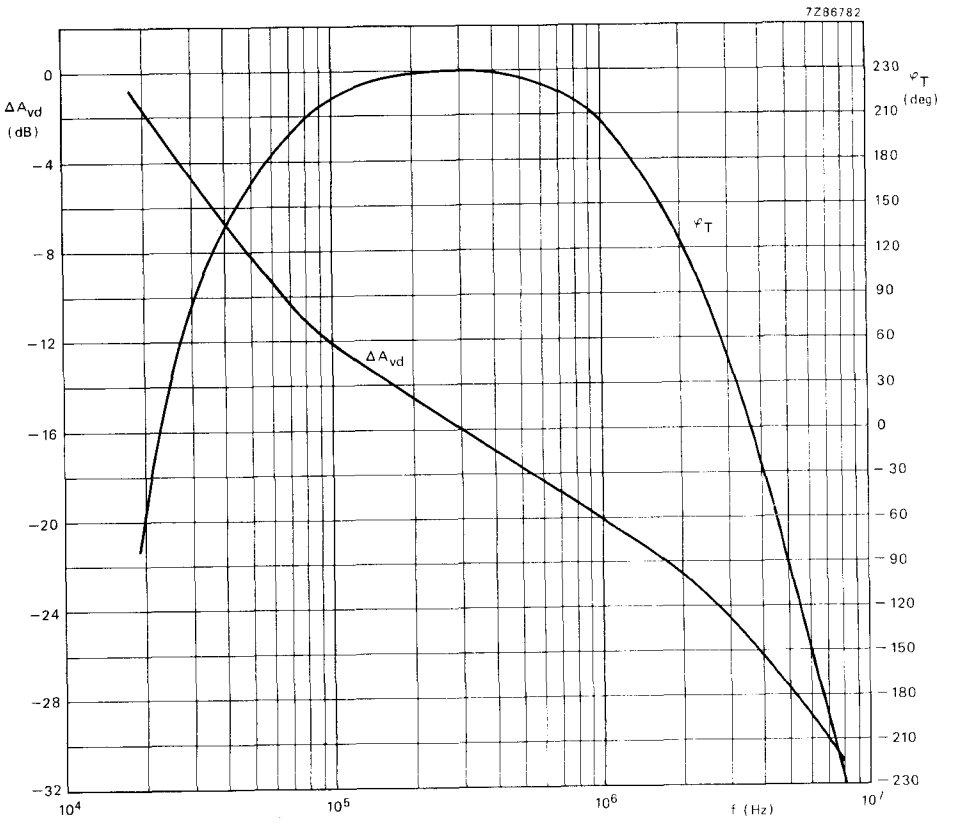


Fig. 10 Gain and phase characteristics of the arrangement of Fig. 9.

TELECOMMUNICATIONS

RING MODULATOR FOR TELEPHONY AND INDUSTRIAL EQUIPMENT

GENERAL DESCRIPTION

The TBA673 is a bipolar integrated circuit comprising a 4-transistor modulator or demodulator circuit. The excellent matching and temperature tracking of the four transistors in the circuit makes it suitable for applications that are not possible with discrete components.

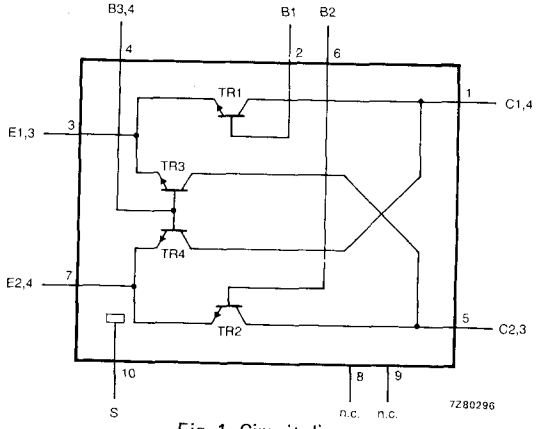


Fig. 1 Circuit diagram.

QUICK REFERENCE DATA

Collector-emitter voltage	V_{CE}	max.	17,5 V
Collector current	I_C	max.	20 mA
Base-emitter voltage difference between transistors at $-I_E$ = 150 μA	$\lvert\Delta V_{BE}\rvert$	max.	5 mV
D.C. current gain difference between transistors at $-I_E$ = 150 μA	$\lvert\Delta h_{FB}\rvert$	max.	0,008
Transition frequency at I_C = 1 mA	f_T	typ.	320 MHz
Collector-base capacitance at V_{CB} = 5 V	C_{cb}	typ.	0,4 pF
Conversion loss at f_c = 34 kHz	$-A_c$	typ.	0,75 dB
Carrier output power at f_c = 34 kHz	P_{oc}	typ.	3 nW
Operating ambient temperature range	T_{amb}		−25 to +125 °C

PACKAGE OUTLINE

10-lead cylindrical; metal (TO-74; reduced height; SOT-14).

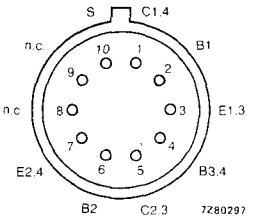


Fig. 2 Pinning diagram, bottom view.

PINNING

1	C1, 4	collectors of TR1 and TR4
2	B1	base of TR1
3	E1, 3	emitters of TR1 and TR3
4	B3, 4	bases of TR3 and TR4
5	C2, 3	collectors of TR2 and TR3
6	B2	base of TR2
7	E2, 4	emitters of TR2 and TR4
8	n.c.	*not connected*
9	n.c.	*not connected*
10	S	*substrate*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage, open base	V_{CEO}	max.	17,5 V
Emitter-base voltage, open collector	V_{EBO}	max.	6,2 V
Collector-substrate voltage	V_{CS}	max.	65 V
Collector current, each transistor	I_C	max.	20 mA
Emitter cut-off current	I_{EBO}	max.	10 μA
Total power dissipation*	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		−55 to +125 °C
Operating ambient temperature range*	T_{amb}		−25 to +125 °C

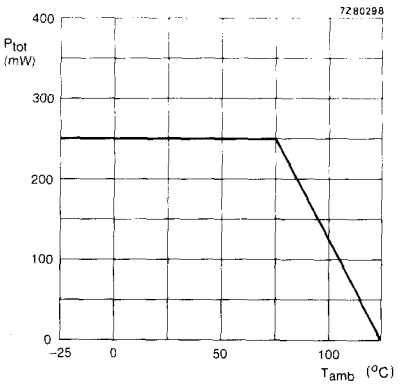


Fig. 3 Power derating curve.

* See derating curve, Fig. 3.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Collector-base breakdown voltage at $I_E = 0$; $I_C = 50\ \mu A$	$V_{(BR)CBO}$	45	–	–	V
Collector-emitter breakdown voltage at $I_B = 0$; $I_C = 200\ \mu A$	$V_{(BR)CEO}$	17,5	–	–	V
Collector-substrate breakdown voltage at $-I_S = 50\ \mu A$	$V_{(BR)CS}$	65	–	–	V
Emitter-base breakdown voltage at $I_C = 0$; $I_E = 10\ \mu A$	$V_{(BR)EBO}$	6,2	–	–	V
D.C. current gain at $V_{CB} = 5$ V; $I_C = 150\ \mu A$	h_{FE}	35	90	–	
$I_C = 10$ mA	h_{FE}	35	75	–	
D.C. current gain difference between transistors TR1 and TR2 or TR3 and TR4 at $V_{CB} = 5$ V; $-I_E = 150\ \mu A$	$\lvert\Delta h_{FB}\rvert$	–	0,002	0,008	
Base-emitter voltage difference between transistors TR1 and TR2 or TR3 and TR4 at $V_{CB} = 5$ V; $-I_E = 150\ \mu A$	$\lvert\Delta V_{BE}\rvert$	–	2	5	mV
Collector cut-off current at $I_E = 0$; $V_{CB} = 5$ V	I_{CBO}	–	5	100	nA
Collector-substrate leakage current at $V_{CS} = 5$ V	I_{CS}	–	5	100	nA
Emitter cut-off current at $I_C = 0$; $V_{EB} = 1$ V	I_{EBO}	–	5	100	nA
Transition frequency at $V_{CB} = 5$ V; $I_C = 150\ \mu A$	f_T	–	140	–	MHz
$I_C = 1$ mA	f_T	–	320	–	MHz
Collector-base capacitance at $V_{CB} = 5$ V; $I_E = 0$	C_{cb}	–	0,4	–	pF
Collector-substrate capacitance at $V_{CS} = 5$ V; $I_E = 0$	C_{cs}	–	2,8	–	pF

APPLICATION INFORMATION

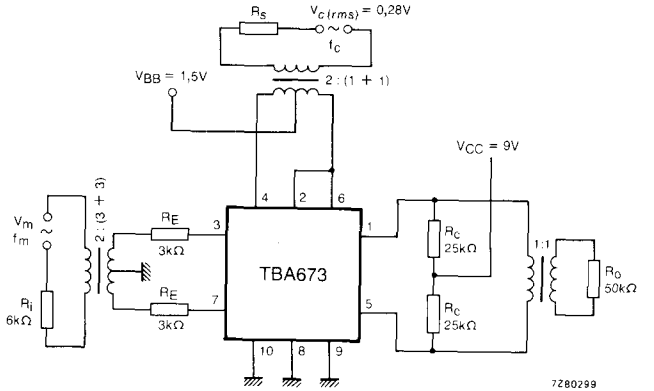


Fig. 4 Typical application of the TBA673 as a telephony carrier ring modulator.

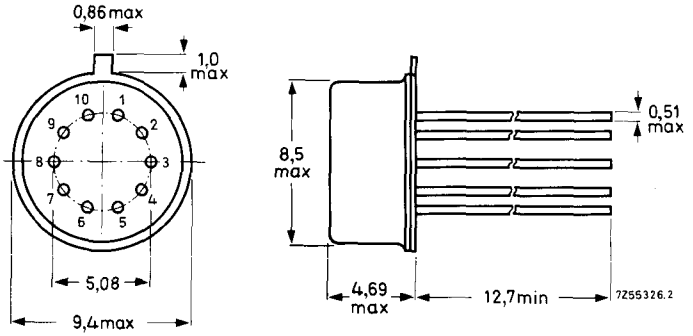
Performance at T_{amb} = 25 °C:

Conversion loss $-A_c$ = typical 0,75 dB
at f_m = 1 kHz; $V_{m(rms)}$ = 0,4 V; f_c = 34 kHz.

Carrier output power (leakage) P_{oc} = 3 nW typ. at f_c = 34 kHz;
$V_{c(rms)}$ = 0,28 V.

PACKAGE OUTLINE

10-lead cylindrical; metal (TO-74; reduced height; SOT-14).



bottom view

AUDIO AMPLIFIER

The TBA915G is a bipolar integrated a.f. amplifier intended for small communication receivers, where low battery drain is of paramount importance. The maximum output power is 850 mW and the zero-signal supply current is only 2 mA (typ.). The circuit can be squelched to a stand-by current of typ. 0,4 mA.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		3,5 to 15 V
Supply current at V_{CC} = 12 V			
squelched	I_{CC}	typ.	0,4 mA
no signal	I_{CC}	typ.	2 mA
P_o = 500 mW	I_{CC}	typ.	72 mA
Input signal for P_o = 500 mW	$V_{i(rms)}$	typ.	10 mV
Input impedance, single-ended	$\lvert z_{is} \rvert$	typ.	9 kΩ
Output power at d_{tot} = 2,5%	P_o	typ.	500 mW
Operating ambient temperature range	T_{amb}		−20 to +80 °C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

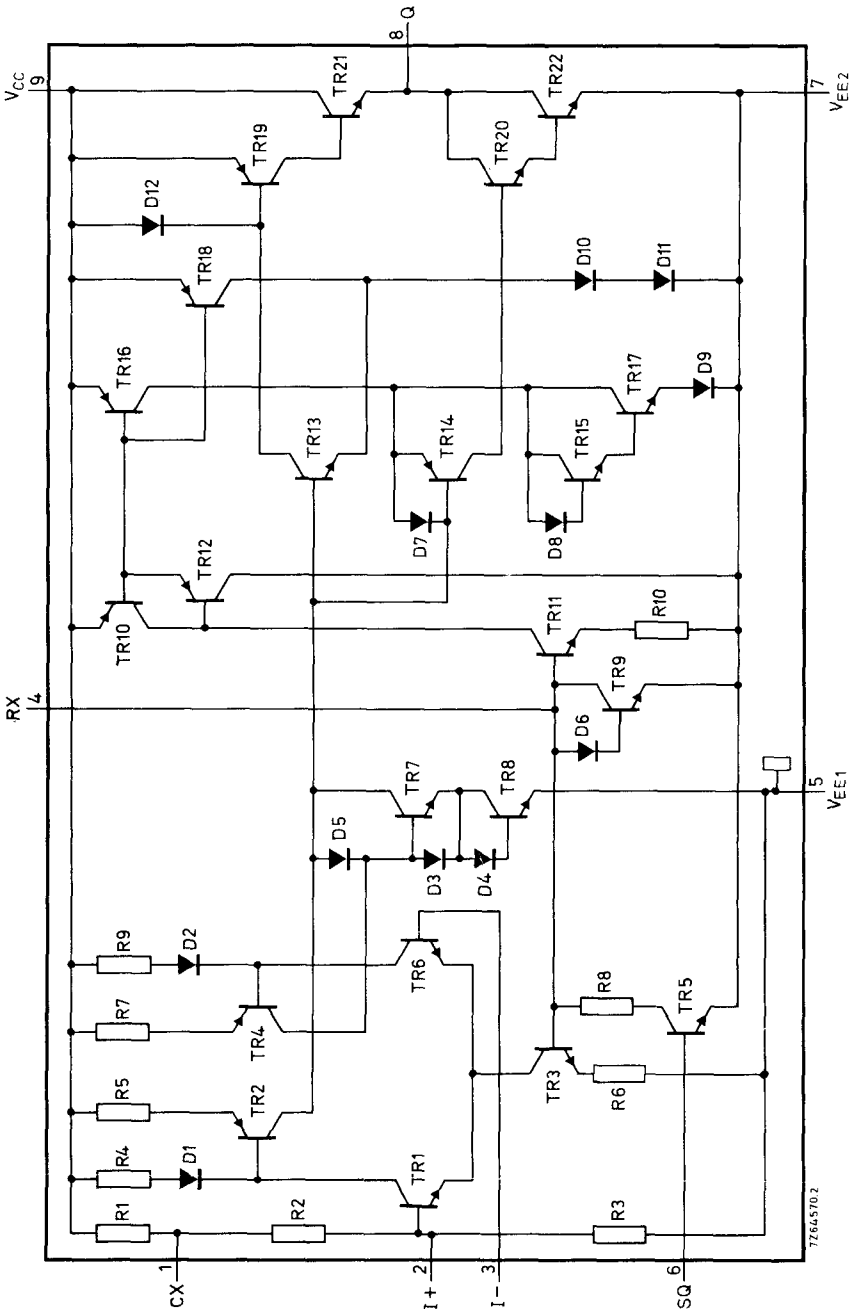


Fig. 1 Circuit diagram.

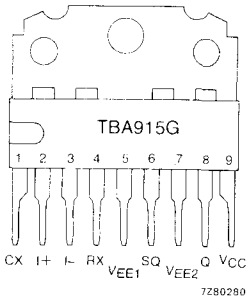


Fig. 2 Pinning diagram.

PINNING

1	CX	external capacitor
2	I+	*non-inverting input*
3	I−	inverting input
4	RX	external resistor
5	V_{EE1}	ground
6	SQ	squelch input
7	V_{EE2}	ground
8	Q	output
9	V_{CC}	positive supply

FUNCTIONAL DESCRIPTION

Supply V_{CC} and RX (pins 9 and 4)

The TBA915G has been designed primarily for use in pocket-size portable communication receivers, with a low supply current as its main feature. The supply current is mainly determined by the output current. The current into the RX connection sets an internal current source.

The circuit may be used over a wide range of supply voltages, viz. 3,5 to 15 V. At 12 V the circuit is capable of delivering a power of 500 mW into a load of 20 Ω. The maximum output power may be increased to 850 mW by increasing the supply voltage to 14 V and reducing the load impedance to 15 Ω.

Inputs I+ and I− (pins 2 and 3)

Inputs I+ and I− are differential inputs. I+ is the non-inverting input, I− the inverting input. The circuit may be driven asymmetrically, as is done in the test circuit of Fig. 4, where I− is used as a feedback input. The circuit has an open-loop gain of 60 dB.

Squelch input SQ (pin 6)

A current into the SQ input squelches the amplifier, it brings the circuit in a stand-by state with a substantially reduced supply current.

Output Q (pin 8)

The circuit has a quasi-complementary class-B output stage.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC}	max.	17	V
Supply current	I_{CC}	max.	350	mA
Bias current into RX	I_{RX}	max.	5	mA
Input voltage, differential, I + and I− inputs	$\|V_{ID}\|$	max.	5	V
Input current, I + and I− inputs	I_I	max.	0,5	mA
Input current, SQ input	I_{SQ}	max.	1	mA
	$-I_{SQ}$	max.	10	μA
Output voltage	V_Q	max.	17	V
Output current	$\pm I_Q$	max.	350	mA
Total power dissipation	P_{tot}	max.	900	mW
Storage temperature range	T_{stg}	−55 to	+125	°C
Operating ambient temperature range	T_{amb}	−20 to	+80	°C

CHARACTERISTICS

V_{CC} = 12 V; V_{EE} = 0 V; T_{amb} = 25 °C; measured in test circuit Fig. 3; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply V_{CC}					
Supply current					
squelched	I_{CC}	–	0,4	0,6	mA
quiescent	I_{CC}	–	2	3,7	mA
P_o = 500 mW	I_{CC}	–	72	—	mA
Variation of quiescent supply current with supply voltage	$\Delta I_{CC}/\Delta V_{CC}$	–	0,06	–	mA/V
Thermal resistance	$R_{th\ j\text{-}a}$	–	50	–	K/W
RX					
Bias current into RX	I_{RX}	25	–	75	μA
Inputs I + and I−					
Input voltage for P_o = 500 mW	$V_{i(rms)}$	–	10	15	mV
Input impedance, single-ended	$\|z_{is}\|$	–	9	–	kΩ
Open-loop differential voltage amplification	A_{vd}	–	60	–	dB
Squelch input SQ					
Input current HIGH (circuit squelched) at I_{RX} = 25 to 75 μA	I_{SQH}	10	–	–	μA
Input voltage HIGH at I_{SQH} = 10 μA	V_{SQH}	–	0,65	–	V
Input voltage LOW (circuit on)	V_{SQL}	–	–	0,4	V
Output Q					
Total distortion at P_o = 500 mW	d_{tot}	–	2,5	5	%
Signal-to-noise ratio at P_o = 500 mW; R_S = 600 Ω, f = 300 Hz to 6 kHz	S/N	–	72	–	dB

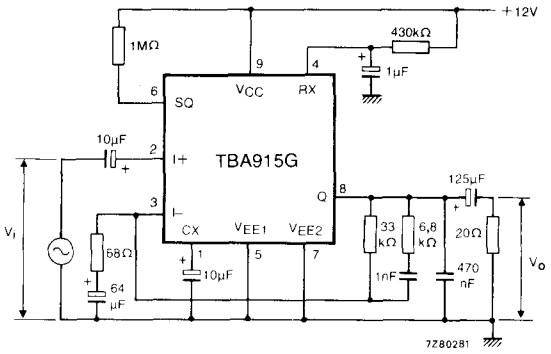


Fig. 3 Test circuit.

APPLICATION INFORMATION

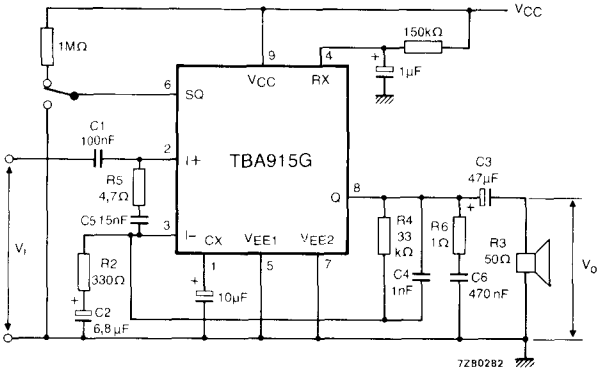


Fig. 4 Typical application of the TBA915G. The frequency range is 185 Hz to 5,2 kHz; the lower frequency limit is determined by the time constants $|z_{is}|$ x C1, R2 x C2 and R3 x C3 and the upper frequency limit by R4 x C4. The closed-loop gain is 39,5 dB with a stability margin greater than 18 dB which is determined by R5 x C5 and R6 x C6. The arrangement produces an output voltage and output power at 1 kHz which are (typical):

$V_{o(rms)}$ = 1,24 V, P_o = 30 mW at V_{CC} = 5 V and d_{tot} = 5%

$V_{o(rms)}$ = 1,7 V, P_o = 56 mW at V_{CC} = 6,8 V and d_{tot} = 0,25%

$V_{o(rms)}$ = 1,9 V, P_o = 72 mW at V_{CC} = 6,8 V and d_{tot} = 5%

AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TCA210 is a bipolar integrated circuit comprising an amplifier for use in intercoms and other audio systems. The amplifier is split into two parts. The first part is a high-gain preamplifier with differential inputs and a class-A output stage which can deliver 2,5 mW into an 800 Ω load. The second part is a power amplifier with a class-B output stage capable of delivering 500 mW into a 25 Ω load and up to 800 mW into 15 Ω for short periods.

Without signal the supply current is typ. 8 mA. Both amplifiers may be squelched to extend battery life in battery-operated equipment.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		8 to 16 V
Supply current, no signal	I_{CC}	typ.	8 mA
Preamplifier			
Open-loop voltage amplification	A_{vd}	typ.	10 000
Output power at R_L = 800 Ω	P_o	typ.	2,5 mW
Noise figure (R_S = 500 Ω; B = 300 to 4000 Hz)	F	max.	6 dB
Unity-gain bandwidth (compensated)	f_t	min.	10 MHz
Power amplifier			
Open-loop voltage amplification	A_{vd}	typ.	500
Output power at d_{tot} = 5%;			
R_L = 25 Ω	P_o	typ.	500 mW
R_L = 15 Ω	P_o	typ.	800 mW
Operating ambient temperature range	T_{amb}		−55 to + 125 °C

PACKAGE OUTLINE

TCA210: 16-lead DIL; plastic (SOT-38).
TCA210T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

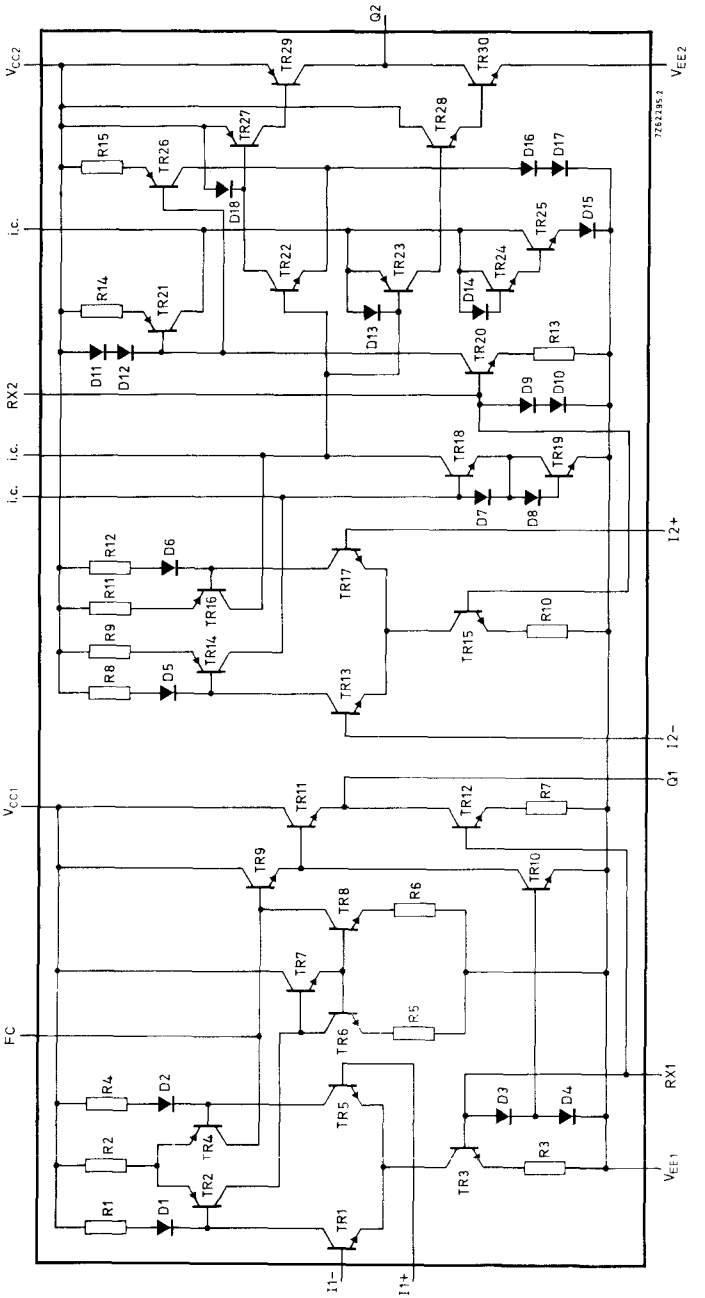
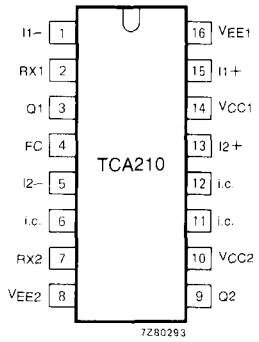
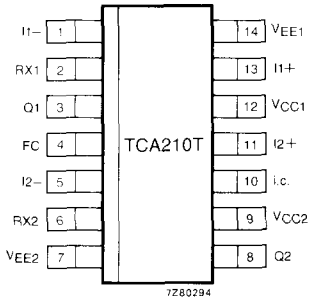


Fig. 1 Circuit diagram.



PINNING TCA210

1	I1−	preamplifier inverting input
2	RX1	external resistor, preamplifier
3	Q1	preamplifier output
4	FC	frequency compensation
5	I2−	power amplifier inverting input
6	i.c.	internally connected
7	RX2	external resistor, power amplifier
8	V_{EE2}	ground connection, output stage of power amplifier
9	Q2	power amplifier output
10	V_{CC2}	positive supply, power amplifier
11	i.c.	internally connected
12	i.c.	internally connected
13	I2+	power amplifier non-inverting input
14	V_{CC1}	positive supply, preamplifier
15	I1+	preamplifier non-inverting input
16	V_{EE1}	ground (except for output stage power amplifier)



PINNING TCA210T

1	I1−	preamplifier inverting input
2	RX1	external resistor, preamplifier
3	Q1	preamplifier output
4	FC	frequency compensation
5	I2−	power amplifier inverting input
6	RX2	external resistor, power amplifier
7	V_{EE2}	ground connection, output stage of power amplifier
8	Q2	power amplifier output
9	V_{CC2}	positive supply, power amplifier
10	i.c.	internally connected
11	I2+	power amplifier non-inverting input
12	V_{CC1}	positive supply, preamplifier
13	I1+	preamplifier non-inverting input
14	V_{EE1}	ground (except for output stage power amplifier)

Fig. 2 Pinning diagrams.

FUNCTIONAL DESCRIPTION

Supply

The preamplifier and the power amplifier have separate supply pins. When one of the amplifiers is not used the corresponding V_{CC} pin may be left open to save supply current.

The ground pin V_{EE1} is common for both amplifiers except for the output stage of the power amplifier which has a separate ground pin V_{EE2}. This minimizes undesirable feedback to the rest of the circuit.

External resistor pins RX1 and RX2

The current in the amplifiers is determined by current sources. These current sources need a minimum current into their RX pins of 200 μA. This current is usually derived from the positive supply via an external resistor.

The preamplifier and the power amplifier may be switched off (squelched) by applying a LOW level to RX1 and RX2 respectively.

Preamplifier inputs I1+ and I1−

The preamplifier has differential inputs I1+ and I1−, I1+ being the non-inverting input and I1− the inverting input. The circuit may be driven asymmetrically, e.g. I1− may be used for negative feedback.

Frequency compensation pin FC

Frequency compensation of the preamplifier may be obtained by connecting an external RC network between FC and ground (see Fig. 4).

Preamplifier output Q1

The preamplifier has a class-A output consisting of an emitter follower with a current source from the emitter to ground.

Power amplifier inputs I2+ and I2−

The power amplifier has differential inputs I2+ and I2--, I2+ being the non-inverting input and I2− the inverting input. The circuit may be driven asymmetrically, e.g. I2− may be used for negative feedback.

Power amplifier output Q2

The power amplifier has a class-B output stage. This output stage is current-driven, which guarantees negligible crossover distortion even at small output signals.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC1}; V_{CC2}	max.	17 V
Supply current	I_{CC1}	max.	20 mA
	I_{CC2}	max.	550 mA
	I_{RX1}; I_{RX2}	max.	5 mA
Input voltage, all inputs	V_I	max.	V_{CC} V
Differential input voltage	$\lvert V_{I1+} - V_{I1-} \rvert$	max.	5 V
	$\lvert V_{I2+} - V_{I2-} \rvert$	max.	5 V
Input current, I1+, I1−, I2+ and I2−	I_I	max.	0,5 mA
Output voltage, Q1 and Q2	V_{Q1}; V_{Q2}	max.	17 V
Output current			
Q1	$\lvert I_{Q1} \rvert$	max.	20 mA
Q2	$\lvert I_{Q2} \rvert$	max.	550 mA
Storage temperature range	T_{stg}	−55 to + 125	°C
Operating ambient temperature range*	T_{amb}	−55 to + 125	°C

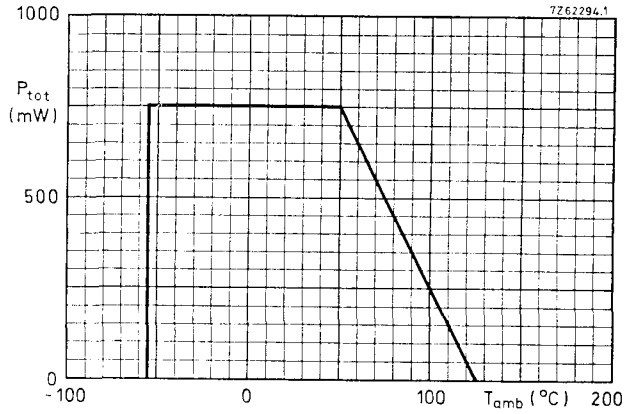


Fig. 3 Power derating curve.

* See Fig. 3.

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply V_{CC1} and V_{CC2}					
Supply current (d.c.), no signal	I_{CC1}	–	4	–	mA
	I_{CC2}	–	4	–	mA
External resistor pins RX1 and RX2					
Voltage at RX: ON	V_{RXH}	1,1	1,35	1,6	V
Voltage at RX: squelched	V_{RXL}	–	–	250	mV
Current into RX: ON	I_{RXH}	200	–	–	μA
Preamplifier inputs I1+ and I1–					
Average input current	I_{I1+}; I_{I1-}	–	2,5	–	μA
Preamplifier output Q1					
Quiescent current in output stage	I_C	2,5	–	–	mA
Open-loop voltage amplification	A_{vd}	65	80	–	dB
Unity-gain bandwidth with 6 dB/octave compensation	f_I	–	10	–	MHz
Noise figure at R_S = 5 kΩ; B = 300 to 4000 Hz	F	–	4	–	dB
Power amplifier inputs I2+ and I2–					
Average input current	I_{I2+}; I_{I2-}	–	2	–	μA
Power amplifier output Q2					
Open-loop voltage amplification	A_{vd}	–	54	–	dB
Output power at R_L = 25 Ω; d_{tot} = 5%	P_o	–	450	–	mW
Total distortion at f = 1 kHz; P_o = 50 mW; R_L = 25 Ω	d_{tot}	–	1,5	–	%

APPLICATION INFORMATION

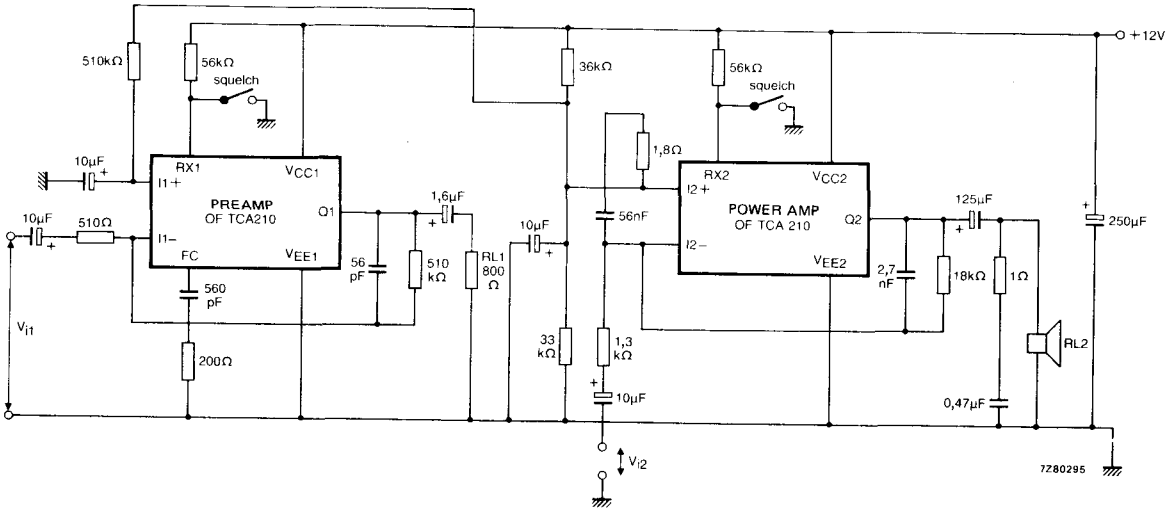


Fig. 4 Typical application of the TCA210 as an amplifier in an intercom system.

PERFORMANCE at V_{CC} = 12 V; T_{amb} = 25 °C

Preamplifier

Input impedance	$\lvert z_{is} \rvert$	typ.	500 Ω
Input voltage for full output drive	$V_{i(rms)}$	typ.	1,5 mV
Output power at R_{L1} = 800 Ω	P_o	typ.	2,5 mW
Cut-off frequency (−3 dB)	f_{co}	typ.	4 kHz
Supply current (d.c.)	I_{CC1}	typ.	4 mA

Power amplifier

Input impedance	$\lvert z_{is} \rvert$	typ.	1,3 kΩ
Input voltage for full output drive	$V_{i(rms)}$	typ.	260 mV
Output power at d_{tot} = 5%;			
R_{L2} = 25 Ω	P_o	typ.	500 mW
R_{L2} = 15 Ω	P_o	typ.	800 mW
Total distortion at P_o = 50 mW	d_{tot}	typ.	1,5 %
Cut-off frequency (−3 dB)	f_{co}	typ.	4 kHz
Supply current (d.c.; no signal)	I_{CC2}	typ.	4 mA

DUAL LONG-TAILED PAIR/DOUBLE-BALANCED MODULATOR

GENERAL DESCRIPTION

The TCA240 is a bipolar integrated circuit comprising two long-tailed pairs with current sources. The circuit may be connected to form a double-balanced modulator. It features great flexibility and the excellent matching and temperature tracking of the transistors in the circuit makes it suitable for applications that are not possible with discrete components.

The circuit is especially suited for the following applications:

- modulator
- mixer
- switch or chopper
- AM synchronous demodulator
- FM quadrature demodulator
- phase comparator
- differential amplifier

QUICK REFERENCE DATA

Supply voltage at C1, C2, C5 and C6	V_C	max.	16 V
Emitter current (each transistor)	$-I_E$	max.	10 mA
D.C. current gain at $-I_E$ = 750 μA	h_{FE}	min.	23
Base-emitter voltage difference between transistors at I_{tail} = 1,5 mA	$\lvert\Delta V_{BE}\rvert$	max.	2,5 mV
Cut-off frequency (3 dB point)	f_{co}	typ.	34 MHz
Noise figure at f = 100 MHz; I_C = 1 mA	F	max.	3,7 dB
Operating ambient temperature range	T_{amb}	−20 to + 70	°C

PACKAGE OUTLINE

TCA240: 16-lead DIL; plastic (SOT-38).
TCA240D: 16-lead mini-pack; plastic (SO-16; SOT-109A).

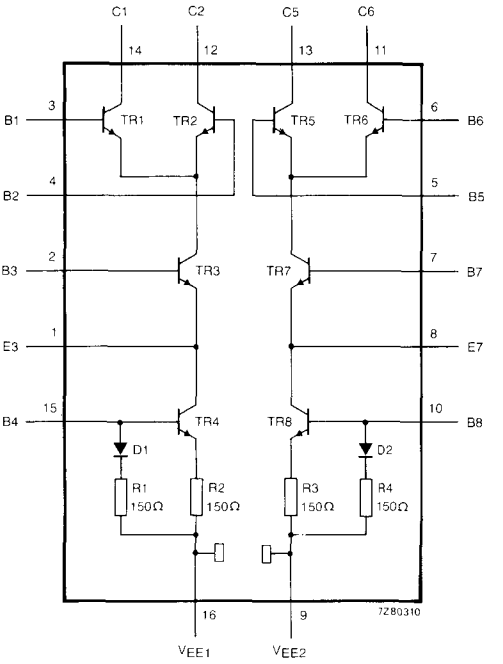


Fig. 1 Circuit diagram.

Pins 9 and 16 are both connected to the substrate. When both long-tailed pairs are used these pins should be interconnected externally.

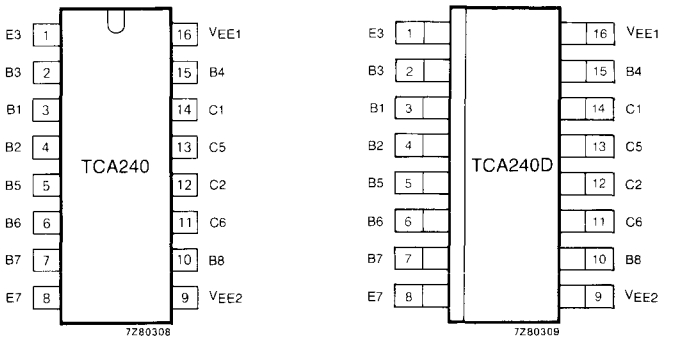


Fig. 2 Pinning diagrams.

FUNCTIONAL DESCRIPTION

The TCA240 contains two long-tailed pairs, each with a current source and a series transistor in the tail.

The current sources contain a current mirror. The tail current will be equal to the current flowing into pin 15 (10) with a deviation of less than 5%.

The TCA240 may be used as two long-tailed pairs or as a single double-balanced modulator. When used as two long-tailed pairs the tail currents may be adjusted separately. V_{EE1} and V_{EE2} (pins 9 and 16) should be interconnected and E3 and E7 (pins 1 and 8) should be left open. Transistors TR3 and TR7 reduce the influence of the long-tailed pair on the tail current.

When the circuit is used as a single double-balanced modulator only one current source is required. E3 and E7 (pins 1 and 8) should be interconnected and B8 and V_{EE2}, pins 10 and 9 (or B4 and V_{EE1}, pins 15 and 16) should be left open. TR3 and TR7 form a long-tailed pair now, each with a long-tailed pair at its collector.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-substrate voltage (open base and emitter)	V_{CSO}	max.	16 V
Collector-base voltage (open emitter)	V_{CBO}	max.	16 V
Collector-emitter voltage (open base)	V_{CEO}	max.	12 V
Base-emitter voltage (open collector)	$-V_{BEO}$	max.	5 V
Emitter current (each transistor)	$-I_E$	max.	10 mA
Base current (each transistor)	I_B	max.	10 mA
Total power dissipation (see also Fig. 3)	P_{tot}	max.	500 mW
Storage temperature range	T_{stg}	−55 to + 125	°C
Operating ambient temperature range	T_{amb}	−20 to + 70	°C

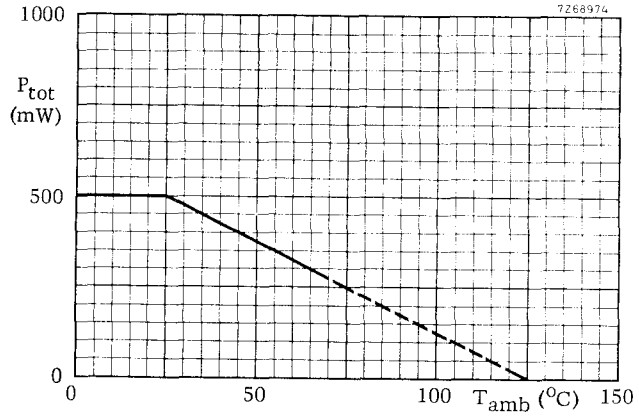


Fig. 3 Power derating curve.

CHARACTERISTICS

at $V_{C1} = V_{C2} = V_{C5} = V_{C6} = 12$ V;
$V_{B1} = V_{B2} = V_{B5} = V_{B6} = 6$ V;
$V_{B3} = V_{B7} = 4$ V; $V_{EE1} = V_{EE2} = 0$ V;
$T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Transistors TR1, TR2, TR5 and TR6					
D.C. current gain, each transistor, at $-I_E = 750\ \mu A$	h_{FE}	23	–	190	
Relative d.c. current gain difference of transistors TR1 and TR2 at $I_{E1} + I_{E2} = -1{,}5$ mA	$\frac{h_{FE1}-h_{FE2}}{h_{FE1}+h_{FE2}} \times 200$	−60	0	+60	%
Relative d.c. current gain difference of transistors TR5 and TR6 at $I_{E5} + I_{E6} = -1{,}5$ mA	$\frac{h_{FE5}-h_{FE6}}{h_{FE5}+h_{FE6}} \times 200$	−60	0	+60	%
Base-emitter voltage difference between TR1 and TR2 (TR5 and TR6) at $I_{tail} = 1{,}5$ mA	$\lvert\Delta V_{BE}\rvert$	–	–	2,5	mV
D.C. current gain of the parallel connection of TR1 and TR6 (TR2 and TR5) at $I_{tail} = 3$ mA	h_{FE1+6}, h_{FE2+5}	23	–	190	
Relative d.c. current gain difference of the parallel connection of TR1, TR6 and TR2, TR5 at $I_{tail} = 3$ mA	$\frac{h_{FE1+6}-h_{FE2+5}}{h_{FE1+6}+h_{FE2+5}} \times 200$	−60	0	+60	%
Base-emitter voltage difference between the parallel connection of TR1, TR5 and TR2, TR6 at $I_{tail} = 3$ mA	$\lvert\Delta V_{BE}\rvert$	–	–	2,1	mV
Transistors TR3 and TR7					
D.C. current gain, each transistor, at $I_{tail} = 3$ mA	h_{FE}	23	–	190	
Relative d.c. current gain difference of transistors TR3 and TR7 at $I_{tail} = 3$ mA	$\frac{h_{FE3}-h_{FE7}}{h_{FE3}+h_{FE7}} \times 200$	−60	0	+60	%
Base-emitter voltage at $-I_E = 1$ mA	V_{BE}	690	–	770	mV
Transistors TR4 and TR8					
Collector current difference at $I_{B4} = I_{B8} = 1{,}5$ mA	ΔI_C	–	–	0,07	mA

parameter	symbol	min.	typ.	max.	unit
Cut-off frequency					
3 dB point at I_{tail} = 5 mA; R_C = 600 Ω; see test circuit Fig. 4	f_{co}	–	34	–	MHz
Noise figure					
at f = 100 MHz; I_C = 1 mA; V_{CB} = 5 V; G_s = 3,7 mA/V; $-B_s$ = 2,5 mA/V	F	–	–	3,7	dB
at f = 100 MHz; $-I_E$ = 2,5 mA; V_{CB} = 5 V; G_s = 6,5 mA/V; $-B_s$ = 2,5 mA/V	F	–	–	4,2	dB

y parameters

at V_{CE} = 5 V; f = 100 MHz

		$-I_E$ =		1	5	mA
Input conductance		g_{ie}	typ.	4,4	13,6	mA/V
Input susceptance		b_{ie}	typ.	7,6	9	mA/V
Feedback admittance		$\|y_{re}\|$	typ.	0,4	0,4	mA/V
Phase angle of feedback admittance		$-\varphi_{re}$	typ.	100°	100°	
Transfer admittance		$\|y_{fe}\|$	typ.	22	55	mA/V
Phase angle of transfer admittance		$-\varphi_{fe}$	typ.	45°	96°	
Output conductance		g_{oe}	typ.	0,4	0,5	mA/V
Output susceptance		b_{oe}	typ.	1,8	18	mA/V

Switching times

(See test circuit, Fig. 5)

	I_{tail} =		0,5	1	2	4	mA
Rise time	t_{TLH}	typ.	2,9	2,7	2,7	3,1	ns
Fall time	t_{THL}	typ.	1,4	1,3	1,6	2,1	ns
Rise propagation delay time	t_{PLH}	typ.	1,1	1,1	1,4	1,7	ns
Fall propagation delay time	t_{PHL}	typ.	1,1	1,2	1,4	1,7	ns

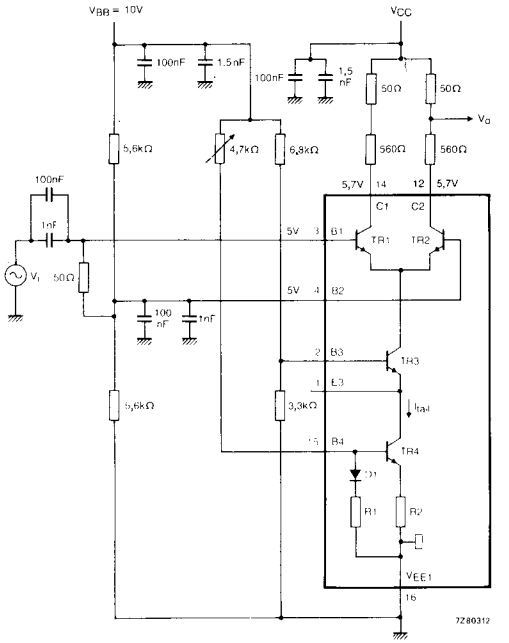


Fig. 4 Test circuit for the frequency response, shown for one half of the circuit.

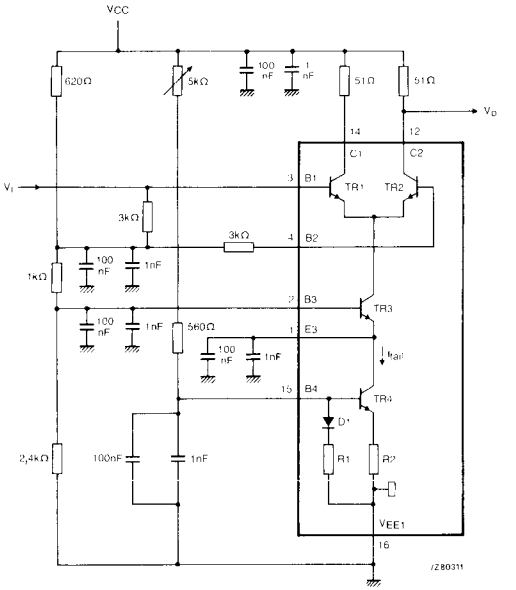


Fig. 5 Test circuit for the switching times, shown for one half of the circuit.

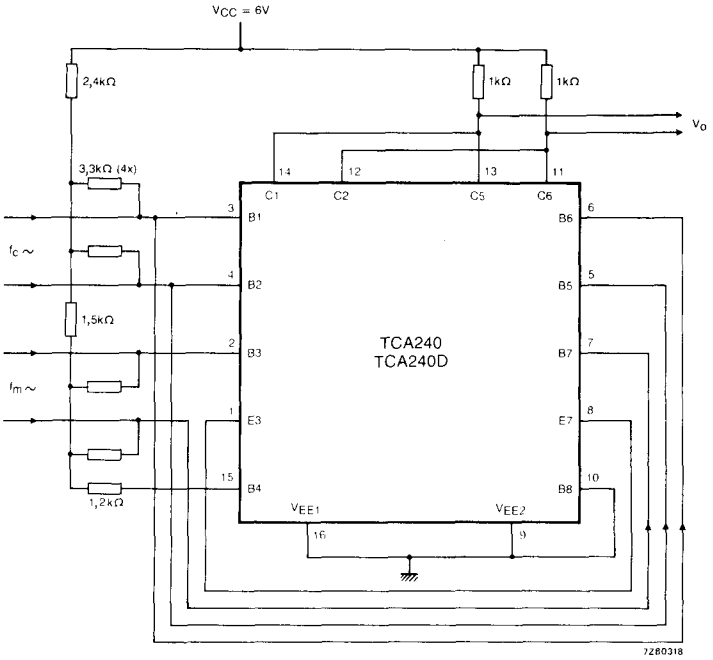


Fig. 6 Typical application of the TCA240 as a double-balanced AM modulator with suppressed carrier.

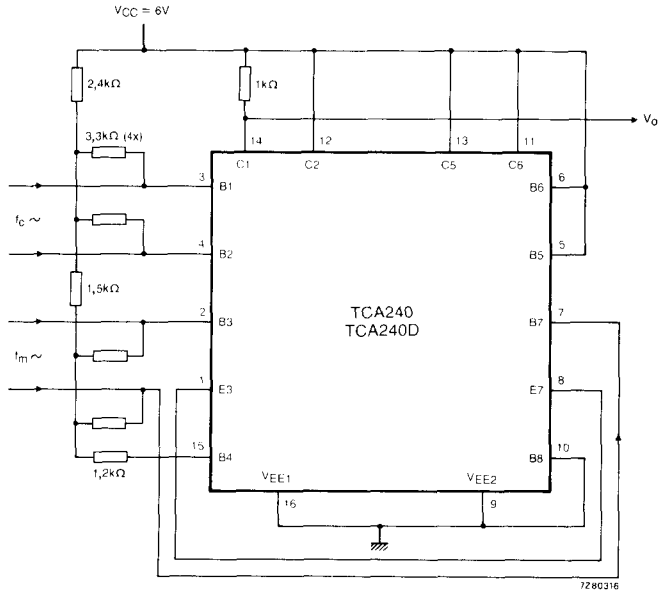


Fig. 7 Typical application of the TCA240 as an AM modulator.

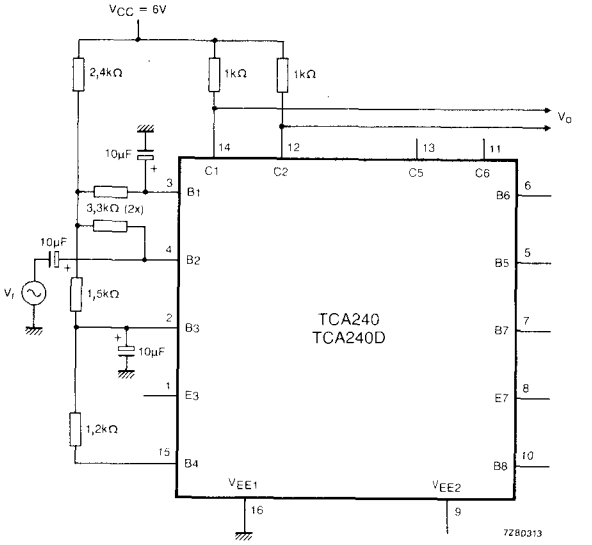


Fig. 8 Typical application of the TCA240 as a differential amplifier.

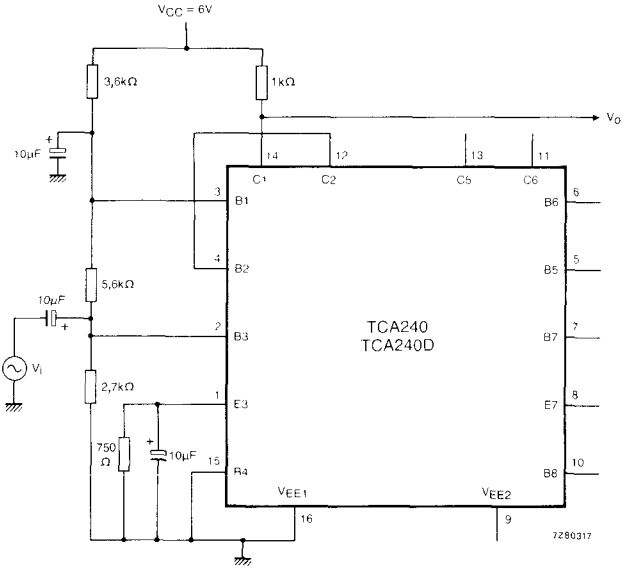


Fig. 9 Typical application of the TCA240 as a cascode amplifier.

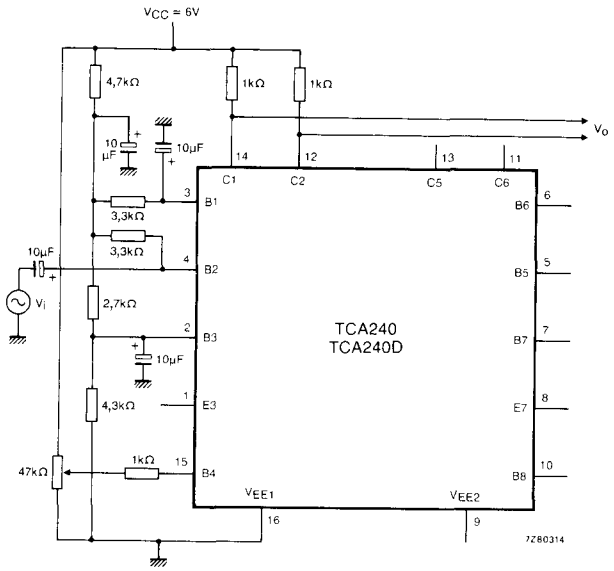


Fig. 10 Typical application of the TCA240 as a differential amplifier with gain control.

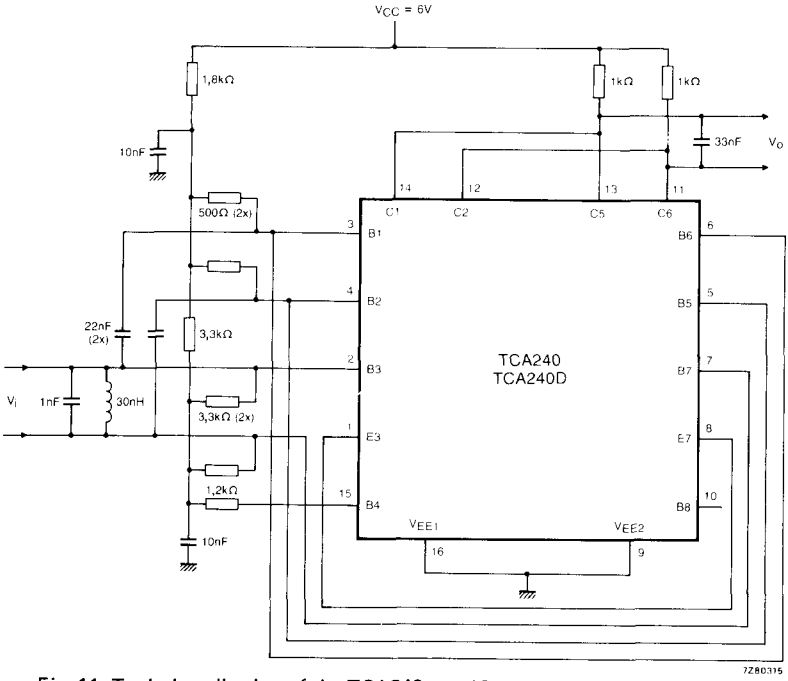


Fig. 11 Typical application of the TCA240 as a 10,7 MHz double-balanced FM demodulator.

I.F. LIMITING AMPLIFIER, FM DETECTOR & AUDIO PREAMPLIFIER

with low supply current

GENERAL DESCRIPTION

The TCA770 is a bipolar integrated circuit comprising a limiting amplifier, a balanced FM detector and an audio preamplifier. It is intended for a frequency range of 100 to 500 kHz with narrow-band FM. The circuit is especially suited for use in portophone sets, where low supply current and high sensitivity are of paramount importance.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		5 to 10	V
Supply current	I_{CC}	typ.	450	μA
I.F. frequency	f_{if}	typ.	100	kHz
Input voltage at onset of limiting	$V_{LI\,lim(rms)}$	typ.	30	μV
AM rejection at $\Delta f = \pm 3{,}5$ kHz; m = 0,3; f_m = 1 kHz; $V_{LI(rms)}$ = 1 mV	k_{AMR}	typ.	50	dB
A.F. output voltage at $\Delta f = \pm 3{,}5$ kHz	$V_{QA(rms)}$	typ.	90	mV
Audio preamplifier open-loop voltage amplification	A_{vd}	typ.	600	
Operating ambient temperature range	T_{amb}	−30 to	+70	°C

PACKAGE-OUTLINES

TCA770A: 16-lead DIL; plastic (SOT-38).
TCA770D: 14-lead mini-pack; plastic (SO-14; SOT-108A).

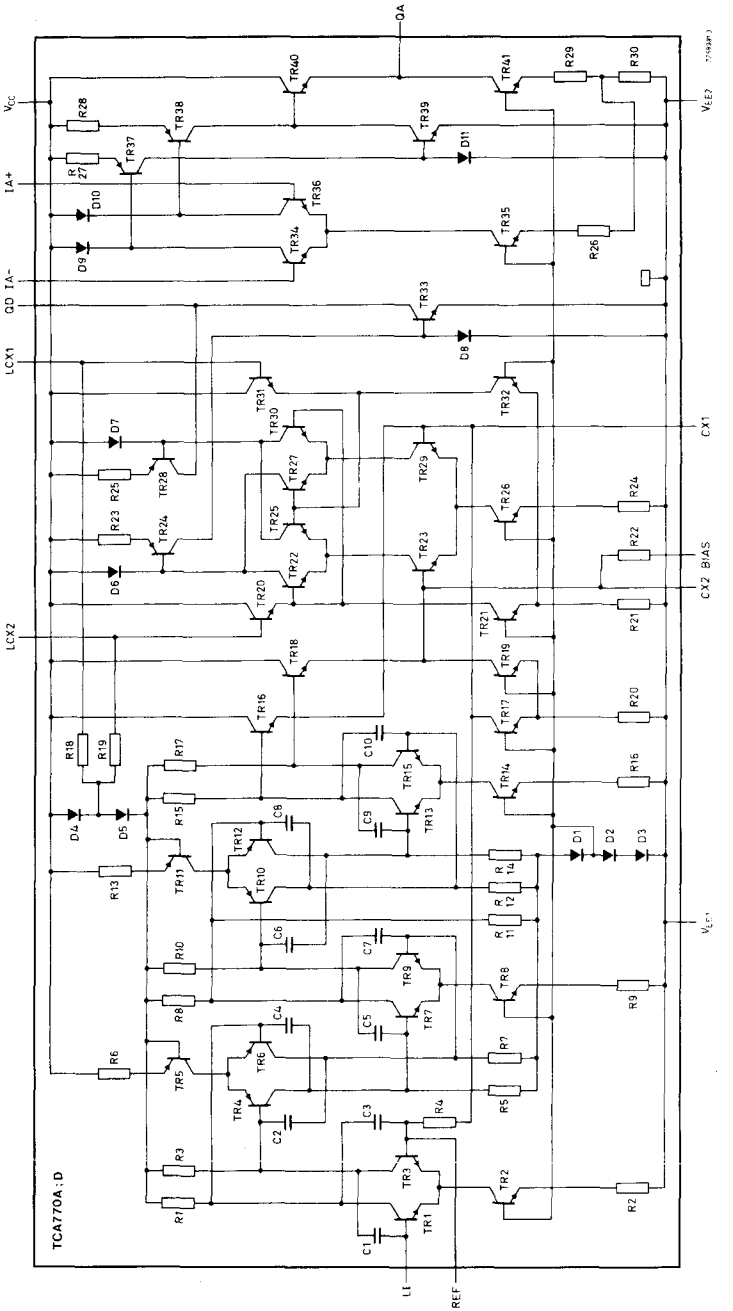
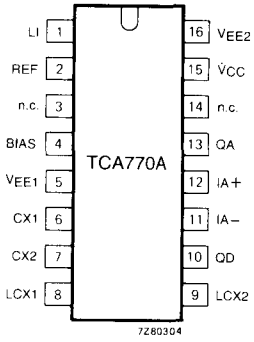


Fig. 1 Circuit diagram.



PINNING TCA770A

1	LI	limiting amplifier input
2	REF	reference input, limiting amplifier
3	n.c.	not connected
4	BIAS	input biasing output
5	V_{EE1}	ground
6	CX1	external capacitor
7	CX2	external capacitor
8	LCX1	external tank circuit
9	LCX2	external tank circuit
10	QD	detector output
11	IA−	audio preamplifier out-of-phase input
12	IA+	audio preamplifier in-phase input
13	QA	audio preamplifier output
14	n.c.	not connected
15	V_{CC}	positive supply
16	V_{EE2}	ground

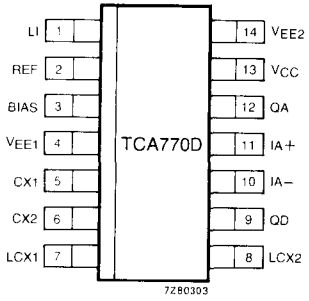


Fig. 2 Pinning diagrams.

PINNING TCA770D

1	LI	limiting amplifier input
2	REF	reference input, limiting amplifier
3	BIAS	input biasing output
4	V_{EE1}	ground
5	CX1	external capacitor
6	CX2	external capacitor
7	LCX1	external tank circuit
8	LCX2	external tank circuit
9	QD	detector output
10	IA−	audio amplifier out-of-phase input
11	IA+	audio preamplifier in-phase input
12	QA	audio preamplifier output
13	V_{CC}	positive supply
14	V_{EE2}	ground

FUNCTIONAL DESCRIPTION

The TCA770 consists of two parts that may be used independently; a limiting amplifier with balanced detector, and an audio preamplifier.

Supply

The TCA770 has two ground connections V_{EE1} and V_{EE2} which are internally interconnected. For minimum interference it is recommended that both V_{EE} connections be grounded.

The circuit is built on the basis of long-tailed pairs with current sources in their tails. Thanks to these current sources the supply current varies little with the supply voltage. This allows the circuit to be used over a wide supply voltage range (5 to 10 V) without resulting in an excessive battery drain.

When the audio preamplifier is not used, its output QA should be connected to V_{CC}.

Limiting amplifier

The limiting amplifier has differential inputs LI and REF. One of the outputs provides a bias voltage for these inputs via the BIAS connection; this gives a feedback adjustment of the working point.

The onset of limiting is specified by the input voltage giving 3 dB gain reduction. This input voltage varies with frequency (see Fig. 3).

Balanced FM detector

The outputs of the limiting amplifier are connected internally to the balanced detector. A tank circuit has to be connected to this detector via CX1, CX2, LCX1 and LCX2 (see Fig. 5).

The balanced detector has a single output QD. Its output voltage varies with temperature (see Fig. 4).

Audio preamplifier

The audio preamplifier has differential inputs IA+ and IA−. IA+ is the in-phase input, IA− the out-of-phase input.

The output QA is an emitter follower with a current source to ground which sinks typ. 56 μA. The output is suited to drive an output stage with an input impedance of approx. 10 kΩ.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{CC}	max.	15 V
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−30 to +70	°C

CHARACTERISTICS

V_{CC} = 7,5 V; T_{amb} = 25 °C; f_{if} = 100 kHz; measured in test circuit of Fig. 6; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply V_{CC}					
Supply voltage	V_{CC}	5	7,5	10	V
Supply current	I_{CC}	300	450	600	μA
Limiting amplifier input LI					
Input impedance	$\lvert Z_{LI}\rvert$	10	–	–	kΩ
Input voltage for onset of limiting (3 dB gain reduction)	$V_{LI\,lim(rms)}$	–	30	–	μV
AM rejection FM signal: Δf = ±3,5 kHz; f_m = 70 Hz AM signal: m = 0,3; f_m = 1 kHz					
at $V_{LI(rms)}$ = 300 μV	k_{AMR}	–	40	–	dB
at $V_{LI(rms)}$ = 1 mV	k_{AMR}	–	50	–	dB
at $V_{LI(rms)}$ = 10 mV	k_{AMR}	–	60	–	dB
Detector output QD					
A.F. output voltage at R_{load} = 100 kΩ; Δf = ±3,5 kHz; f_m = 1 kHz; $V_{LI(rms)}$ = 10 mV	$V_{QD(rms)}$	–	90	–	mV
variation with temperature	$\frac{\Delta V_{QD(rms)}}{\Delta T}$	–	0,062	–	dB/K
Distortion at Δf = ± 5 kHz; f_m = 1 kHz	d_{tot}	–	2	3	%
Audio preamplifier inputs IA+ and IA–					
Input bias current	I_I	–	270	–	nA
Audio preamplifier output OA					
Sink current in output stage	I_{sink}	–	56	–	μA
Open-loop voltage amplification (unloaded)	A_{vd}	–	600	–	

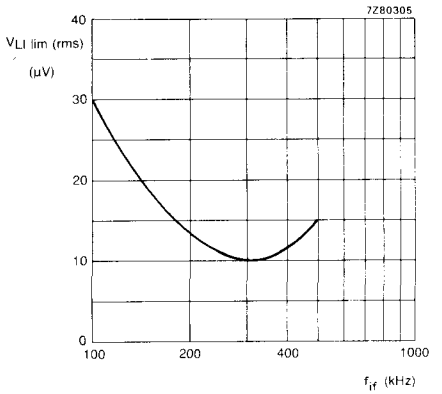


Fig. 3 Variation of input voltage at onset of limiting with frequency.

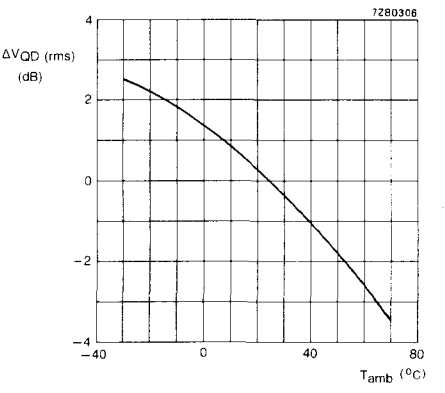
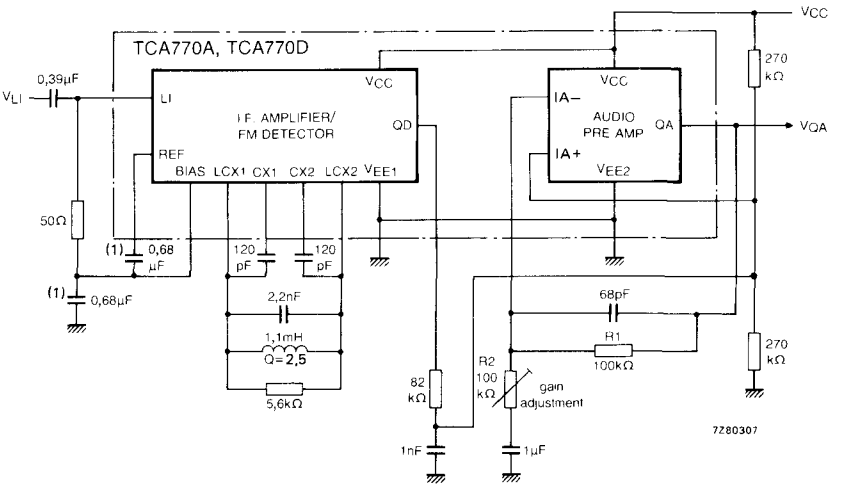


Fig. 4 Variation of detector output voltage with temperature.



(1) The input limiting voltage depends on the capacitance values. Suggested type: solid aluminium capacitor, 2222 122 56687; 0,68 μF/25 V.

Fig. 5 Test circuit and typical application of the TCA770. The output voltage is $V_{QA} = (R1 + R2)/R2 \times V_{IA+}$.

MICROPHONE AMPLIFIER

GENERAL DESCRIPTION

The TCA980G is a bipolar integrated microphone amplifier. It is primarily intended for use with low-impedance microphones in telephone systems. The output of the amplifier is 210 V/kPa when used with a microphone having an impedance of 200 Ω and a sensitivity of 10 mV/kPa.

A capsule assembly containing the TCA980G, a low-impedance microphone and a 220 nF capacitor can directly replace a carbon microphone. The circuit is intended to be supplied from the telephone line, the line current may be of either polarity.

QUICK REFERENCE DATA

Supply current range	$\pm I_{LN2}$	10 to 100	mA
Supply voltage drop at $\pm I_{LN2}$ = 10 mA	$\lvert V_{LN1}-V_{LN2}\rvert$	typ. 4,75	V
Voltage amplification at $\pm I_{LN2}$ = 30 mA	A_{vd}	typ. 220	
at $\pm I_{LN2}$ = 10 mA	A_{vd}	min. 160	
Output impedance at $\pm I_{LN2}$ = 30 mA	$\lvert z_{od}\rvert$	typ. 150	Ω
Operating ambient temperature range	T_{amb}	−35 to +75	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

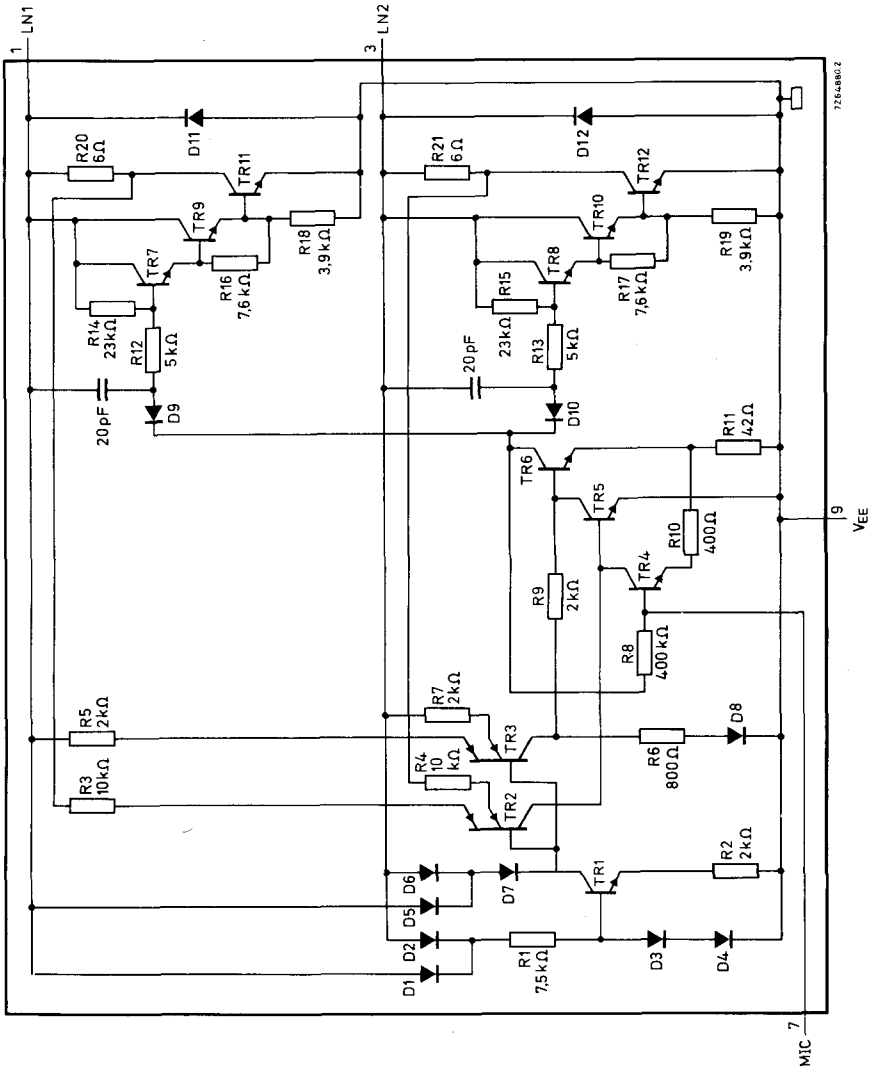


Fig. 1 Circuit diagram.

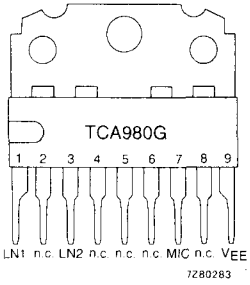


Fig. 2 Pinning diagram.

PINNING

1	LN1	line terminal 1
2	n.c.	not connected
3	LN2	line terminal 2
4	n.c.	not connected
5	n.c.	not connected
6	n.c.	not connected
7	MIC	microphone input
8	n.c.	not connected
9	V_{EE}	reference

FUNCTIONAL DESCRIPTION

At its line terminals LN1 and LN2 the TCA980G is compatible with a classical carbon microphone. The circuit then is supplied from the telephone line and produces its own supply voltage, irrespective of the direction of line current flow. The output voltage is produced across the same line terminals LN1 and LN2. The circuit is well stabilized with the result that circuit properties such as gain and d.c. voltage drop vary little with line current.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current, LN1 and LN2		
d.c.	$\pm I_{LN}$	max. 100 mA
non-repetitive peak	$\pm I_{LN(SM)}$	max. 100 mA a.c. superimposed on 100 mA d.c.
Input current, d.c.	$\pm I_{MIC}$	max. 100 μA
Total power dissipation	P_{tot}	see Fig. 3
Storage temperature range	T_{stg}	−55 to +125 °C
Operating ambient temperature range	T_{amb}	−35 to +75 °C

CHARACTERISTICS

$\pm I_{LN2}$ = 10 to 60 mA; T_{amb} = 25 °C unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage drop					
at $\pm I_{LN2}$ = 10 mA	$\lvert V_{LN1} - V_{LN2}\rvert$	3,5	4,75	5,75	V
at $\pm I_{LN2}$ = 30 mA	$\lvert V_{LN1} - V_{LN2}\rvert$	4,45	–	6,75	V
at $\pm I_{LN2}$ = 60 mA	$\lvert V_{LN1} - V_{LN2}\rvert$	5,0	–	7,8	V
Gain					
Voltage amplification at f = 2 kHz; T_{amb} = 25 °C; see Fig. 4;					
at $\pm I_{LN2}$ = 10 mA	A_{vd}	160	–	260	
at $\pm I_{LN2}$ = 30 mA	A_{vd}	190	220	260	
Variation of voltage amplification with temperature for T_{amb} = −20 to +55 °C	$\Delta A_{vd}/A_{vd}$	–	–	10	%
Variation of voltage amplification with frequency for f = 0,3 to 2 kHz	ΔA_{vd}	–	1	3	dB
Output					
Output voltage swing, clipped,					
at $\pm I_{LN2}$ = 10 mA	$V_{LN1\text{-}LN2(p\text{-}p)}$	2,6	–	–	V
at $\pm I_{LN2}$ = 30 mA	$V_{LN1\text{-}LN2(p\text{-}p)}$	3,5	–	–	V
at $\pm I_{LN2}$ = 60 mA	$V_{LN1\text{-}LN2(p\text{-}p)}$	2,6	–	–	V
A.C. output voltage at f = 2 kHz; d_{tot} = 5%;					
at $\pm I_{LN2}$ = 10 mA	$V_{LN1\text{-}LN2(rms)}$	1	–	–	V
at $\pm I_{LN2}$ = 30 mA	$V_{LN1\text{-}LN2(rms)}$	1,35	–	–	V
at $\pm I_{LN2}$ = 60 mA	$V_{LN1\text{-}LN2(rms)}$	–	1,5	–	V
Noise output voltage at B = 0,3 to 4 kHz	$V_{n(rms)}$	–	–	1,3	mV
Output impedance at f = 2 kHz; $\pm I_{LN2}$ = 30 mA	$\lvert z_{od}\rvert$	–	150	–	Ω

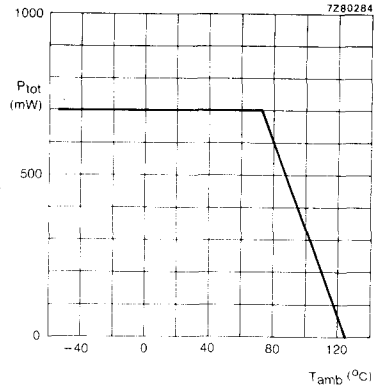


Fig. 3 Power derating curve.

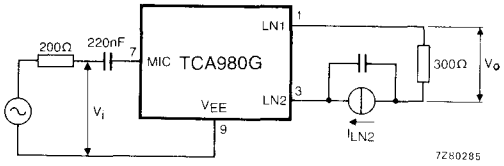


Fig. 4 Test circuit for voltage gain.

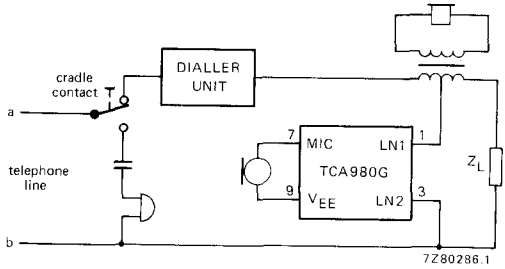


Fig. 5 Typical application of the TCA980G. At pins LN1 and LN2, the IC is compatible with a carbon microphone in a classical subscriber set.

I.F. LIMITING AMPLIFIER, FM DETECTOR & AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDB1080 is a bipolar integrated circuit comprising a limiting amplifier, a balanced FM detector and a class-B audio amplifier. It is intended for frequencies up to 500 kHz with either narrow-band or wide-band FM. The circuit is especially suited for use in portophone sets, where a low supply voltage, a low supply current and a high sensitivity are of paramount importance.

QUICK REFERENCE DATA

Supply voltage range				
I.F. part	V_{CC1}		2,3 to 3,5	V
A.F. part	V_{CC2}		2,3 to 10	V
Supply current at $V_{CC1} = V_{CC2} = 2{,}5$ V, no signal	$I_{CC1} + I_{CC2}$	typ.	3	mA
Input voltage at onset of limiting	$V_{I1lim(rms)}$	typ.	30	μV
AM rejection at $V_i = 1$ mV	k_{AMR}	typ.	50	dB
Open-loop voltage amplification of audio amplifier	A_{vd}	typ.	200	
Output power of audio amplifier at $V_{CC2} = 9$ V	P_o	typ.	65	mW
Operating ambient temperature range	T_{amb}		−20 to + 70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38S).

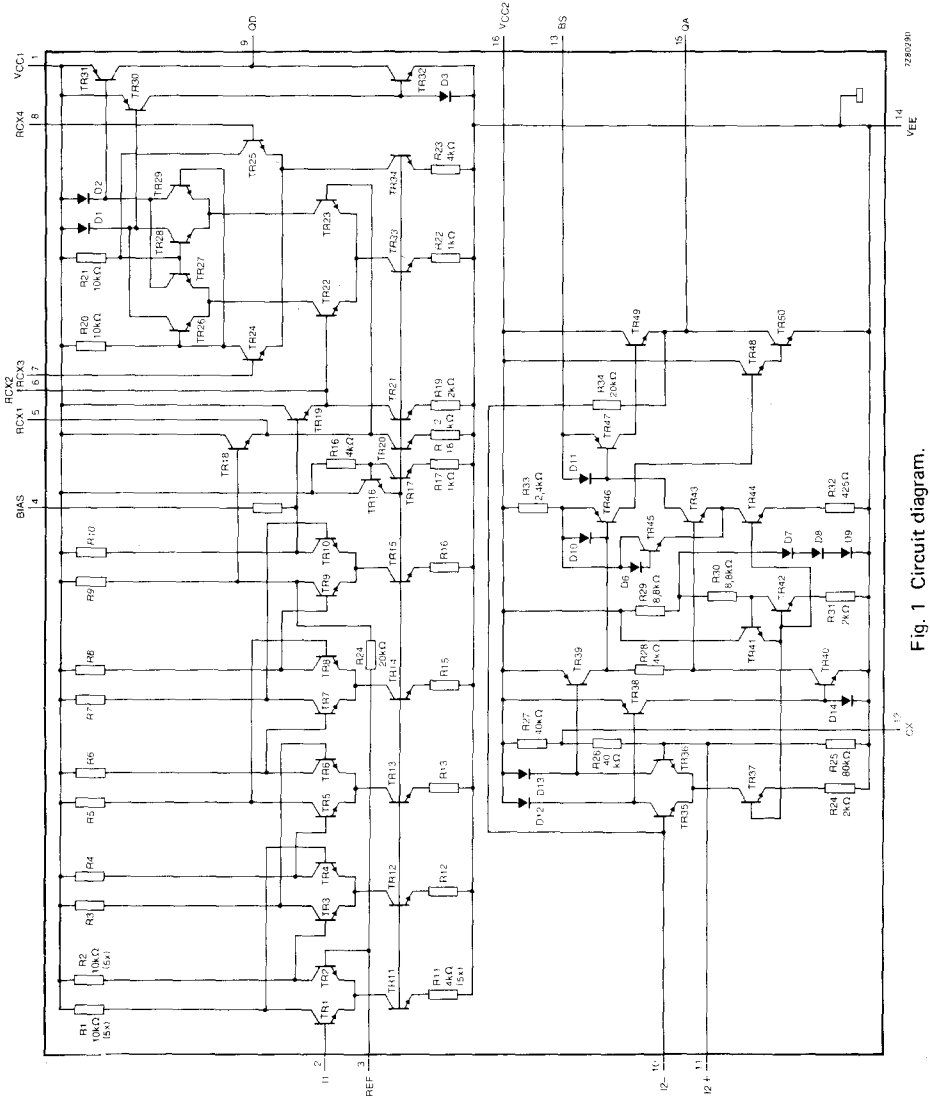


Fig. 1 Circuit diagram.

PINNING

1	V_{CC1}	positive supply, limiting amplifier
2	I1	limiting amplifier input
3	REF	reference input, limiting amplifier
4	BIAS	input biasing output
5	RCX1	external RC network
6	RCX2	external RC network
7	RCX3	external RC network
8	RCX4	external RC network
9	QD	FM detector output
10	I2−	out-of-phase input, audio amplifier
11	I2+	in-phase input, audio amplifier
12	CX	external capacitor
13	BS	bootstrap
14	V_{EE}	ground
15	QA	audio amplifier output
16	V_{CC2}	positive supply, audio amplifier

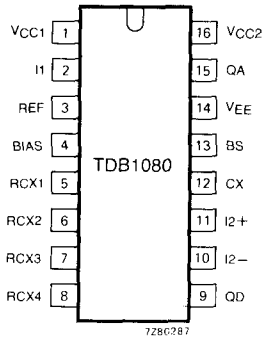


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The TDB1080 consists of two parts that may be used independently, viz. a limiting i.f. amplifier with balanced FM detector, and a class-B audio amplifier.

Supply

The two parts of the circuit have a common-ground pin V_{EE} but separate supply pins V_{CC1} and V_{CC2}. The limiting amplifier and detector may be used with a supply voltage up to 3,5 V, the audio amplifier up to 10 V. The circuit is built to a large extent on the basis of long-tailed pairs with current sources in their tails. Thanks to the stabilizer diodes (D7, D8 and D9) the supply current of the audio amplifier varies little with the supply voltage. This permits the circuit to be used over a wide supply voltage range without an excessive battery drain as a result.

Limiting amplifier inputs I1 and REF and biasing output BIAS (pins 2, 3 and 4)

The limiting amplifier has differential inputs I1 and REF. I1 is intended to be used as an input; it should be biased externally by connecting it to the input biasing output BIAS via a resistor or an inductor. The reference input REF is biased internally; it should be decoupled by connecting a capacitor from REF to ground.

The onset of limiting is specified as the input voltage giving 3 dB gain reduction.

External RC network pins RCX1 to RCX4 (pins 4 to 8)

The TDB1080 contains a quadrature detector which requires an RC phase shifting network. This has to be connected to RCX1, RCX2, RCX3 and RCX4 as shown in Fig. 4. The component values have to be chosen in accordance with the i.f. centre frequency.

Audio amplifier inputs I2+ and I2− (pins 11 and 10)

The audio amplifier has differential inputs I2+ and I2− which are biased internally.

FUNCTIONAL DESCRIPTION (continued)

External capacitor pin CX (pin 12)

The internal biasing network for input I2 + should be decoupled by connecting an external capacitor between CX and ground.

Audio amplifier output QA and bootstrap pin BS (pins 15 and 13)

The audio amplifier has a class-B output stage. The maximum output voltage swing is obtained by connecting a capacitor between the bootstrap pin BS and the output QA and the load from BS to V_{CC2} (see Fig. 4).

The maximum output power varies from typ. 15 mW at V_{CC2} = 2,5 V to typ. 65 mW at V_{CC2} = 9 V.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages, d.c.	V_{CC1}	max.	5 V
	V_{CC2}	max.	10 V
Supply current	$I_{CC1} + I_{CC2}$	max.	50 mA
Total power dissipation	P_{tot}	see Fig. 3	
Storage temperature range	T_{stg}	−55 to + 125	°C
Operating ambient temperature range	T_{amb}	−20 to + 70	°C

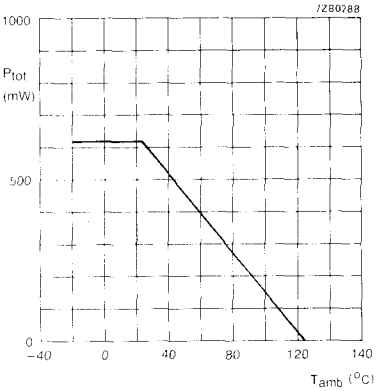


Fig. 3 Power derating curve.

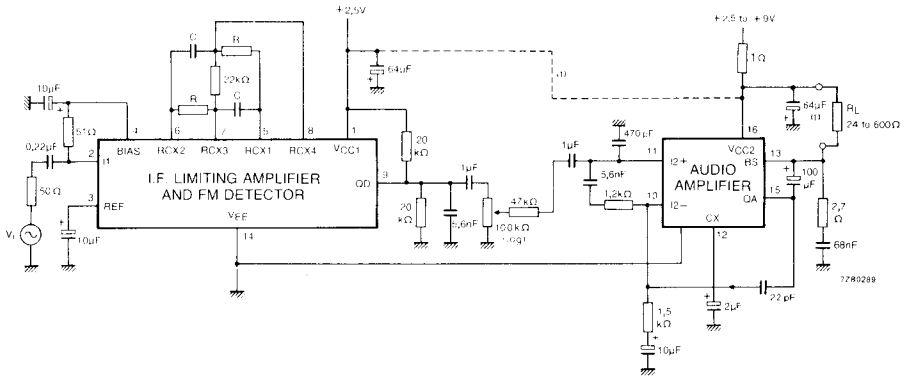
CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2{,}5$ V; $f_i = 95$ kHz; $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $T_{amb} = 25\ ^{o}C$ unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies V_{CC1} and V_{CC2} (pins 1 and 16)					
Supply voltages	V_{CC1}	2,3	2,5	3,5	V
	V_{CC2}	2,3	2,5	10	V
Supply currents					
at $V_{CC1} = 2{,}5$ V	I_{CC1}	–	1,5	2	mA
at $V_{CC2} = 2{,}5$ V, no signal	I_{CC2}	–	1,5	2	mA
at $V_{CC2} = 9$ V, no signal	I_{CC2}	–	3,5	–	mA
Limiting amplifier input I1 (pin 2)					
Input impedance	$\lvert z_{id} \rvert$	15	–	–	kΩ
Input voltage for onset of limiting (3 dB gain reduction)	$V_{I1lim(rms)}$	–	30	–	μV
Source impedance (between I1 and REF)	$\lvert Z_S \rvert$	–	–	5	kΩ
A.M. suppression					
at $\Delta f_i = 70$ Hz; $f_m = 1$ kHz; m = 0,3; $R_S = 50\ \Omega$					
at $V_{I1(rms)} = 300\ \mu$V	k_{AMR}	–	40	–	dB
at $V_{I1(rms)} = 1$ mV	k_{AMR}	–	50	–	dB
at $V_{I1(rms)} = 10$ mV	k_{AMR}	–	50	–	dB
$R_S = 5$ kΩ					
at $V_{I1(rms)} = 300\ \mu$V	k_{AMR}	–	30	–	dB
at $V_{I1(rms)} = 1$ mV	k_{AMR}	–	40	–	dB
at $V_{I1(rms)} = 10$ mV	k_{AMR}	–	50	–	dB
FM Detector output QD (pin 9)					
Output voltage at $d_{tot} = 0{,}5\%$;					
at $f_i = 95$ kHz; $\Delta f = \pm 50$ kHz	$V_{QD(rms)}$	100	–	–	mV
at $f_i = 250$ kHz; $\Delta f = \pm 50$ kHz	$V_{QD(rms)}$	100	–	–	mV
Signal-to-noise ratio					
at $f_i = 95$ kHz; $\Delta f = \pm 50$ kHz	S/N	70	–	–	dB
at $f_i = 250$ kHz; $\Delta f = \pm 50$ kHz	S/N	70	–	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Audio amplifier					
Open-loop voltage amplification	A_{vd}	–	200	–	
variation with frequency, f = 50 Hz to 15 kHz	ΔA_{vd}	−1,5	–	+ 1,5	dB
Load resistance	R_L	24	–	600	Ω
Output voltage at R_L = 24 Ω; d_{tot} = 1%	$V_{QA(rms)}$	–	600	–	mV
Total distortion at R_L = 24 Ω; $V_{QA(rms)}$ = 500 mV	d_{tot}	–	0,5	1	%
Output power at V_{CC2} = 9 V; R_L = 115 Ω; d_{tot} = 5%	P_{QA}	–	65	–	mW
Signal-to-noise ratio at R_L = 115 Ω; V_o = 600 mV; f = 0,5 to 11 kHz; 80 dB/octave cut-off filter	S/N	70	–	–	dB



(1) If V_{CC2} is equal to V_{CC1} pin 16 can be connected to pin 1 and the capacitor to pin 16 can be omitted.

Fig. 4 Test circuit and typical application of the TDB1080. For f_i = 95 kHz R = 100 kΩ and C = 82 pF, for f_i = 250 kHz R = 33 kΩ and C = 47 pF.

DTMF GENERATOR FOR TELEPHONE DIALLING

This integrated circuit is a dual-tone multi-frequency (DTMF) generator, supplying frequency combinations (in accordance with CCITT recommendations) for use in pushbutton telephones, with a common contact on the keyboard for muting.

The various frequencies are derived from a crystal-controlled oscillator followed by a sinewave synthesizer.

I^2L technology allows digital and analogue functions to be implemented on the same chip. The built-in current/voltage regulator and active output amplifier substantially reduce the number of external components. Only a quartz crystal of 4,78 MHz and a few resistors and capacitors are required.

The circuit features:
- wide operating line current range
- operating voltage down to 1,3 volt
- no individual tone level adjustment required
- temperature stabilized signal levels
- line current independent signal levels
- output stage and line regulator included
- all pins protected against electrostatic discharges
- two key roll-over provided
- operates with a low cost quartz crystal
- few external components required

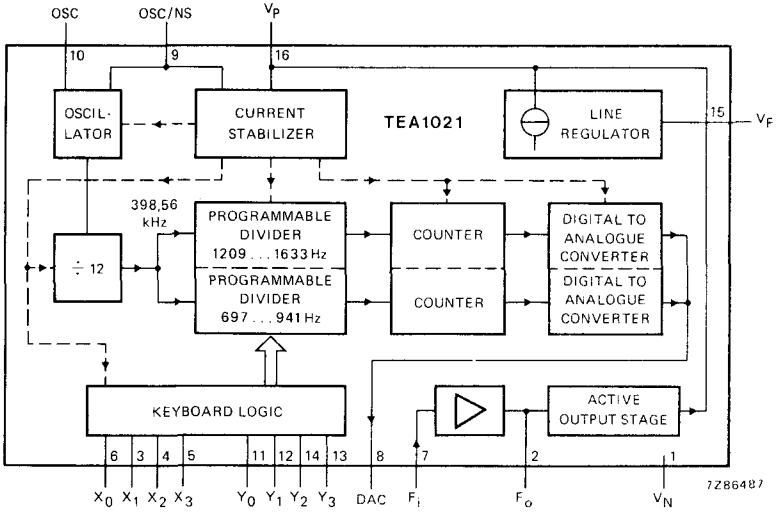


Fig. 1 Block diagram (dotted lines are stabilized supply rails).

PACKAGE OUTLINES

TEA1021P: 16-lead DIL, plastic (SOT-38).
TEA1021D: 16-lead DIL, ceramic (SOT-74B).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current	I_P	max.	150 mA
Surge current ($t_p < 250\ \mu s$)	I_S	max.	850 mA
Input series resistance	R_s	min.	18 Ω
Operating ambient temperature range	T_{amb}	−25 to + 70	°C
Storage temperature range	T_{stg}	−55 to + 125	°C
Junction temperature	T_j	max.	125 °C

CHARACTERISTICS

V_N = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified.

	symbol	min.	typ.	max.	unit	conditions
operating voltage d.c.; $-I_L$ = 10 mA	V_L	2,8	3,3	3,8	V	
line current						
level − 7 dBm	I_L	10	8	120	mA	
level − 2 dBm	I_L	12	9	120	mA	
internal impedance	Z_i	640	900	1150	Ω	300 − 3400 Hz
tone frequencies						
low	f_{x0}	–	697	–	Hz	frequency quartz crystal 4 782 720 Hz
	f_{x1}	–	770	–	Hz	
	f_{x2}	–	852	–	Hz	
	f_{x3}	–	941	–	Hz	
high	f_{y0}	–	1209	–	Hz	
	f_{y1}	–	1336	–	Hz	
	f_{y2}	–	1477	–	Hz	
	f_{y3}	–	1633	–	Hz	
dividing error		–	–	0,11	%	
nom. output level						
lower frequency	V_{LG}	–	–	−6	dBm	adjustable
higher frequency	V_{HG}	–	–	−4	dBm	adjustable
tolerance on output level	ΔV_o	2	–	2	dB	
pre-emphasis		1,3	2	2,7	dB	without filter components
distortion with respect to total level	d_{tot}	–	−34	−24	dB	maximum tone level and with first-order filter
start up time	t_s	–	5	–	ms	with recommended external components
switch bounce elimination	t_{sb}	1	1,5	2	ms	
required keyboard resistance						
contact on	$R_{k\ on}$	–	–	10	kΩ	
contact off	$R_{k\ off}$	500	–	–	kΩ	

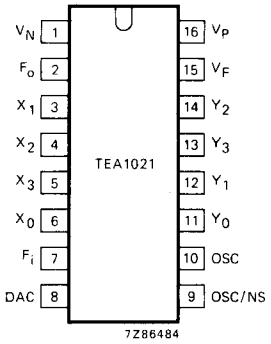


Fig. 2 Pin designation.

PINNING

1	V_N	negative supply
2	F_o	filter output
3	X1	row keyboard input 1
4	X2	row keyboard input 2
5	X3	row keyboard input 3
6	X0	row keyboard input 0
7	F_i	filter input/input audio amplifier
8	DAC	output DAC/DTMF tones
9	OSC/NS	oscillator/noise suppression output
10	OSC	oscillator input
11	Y0	column keyboard input 0
12	Y1	column keyboard input 1
13	Y3	column keyboard input 3
14	Y2	column keyboard input 2
15	V_F	input low-pass filter
16	V_P	positive supply

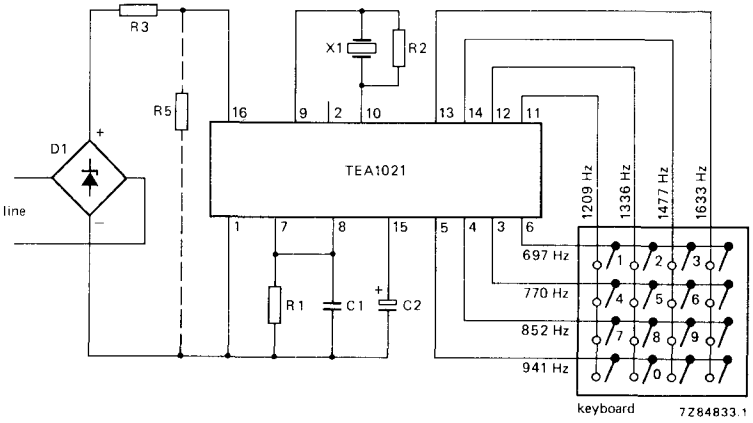


Fig. 3 Application diagram with first-order filter.

R1	metal film resistor	MR16	1%	see Fig. 7
R2	metal film resistor	SFR16	5%	3,3 MΩ
R3	metal film resistor	SFR16	5%	18 Ω
R5	metal film resistor	SFR16	5%	2700 Ω (for Z_o = 600 Ω; no resistor for Z_o = 900 Ω)
C1	metallized polyester film capacitor			see Fig. 7
C2	solid aluminium electrolytic capacitor		6,3 V	4,7 μF
D1	polarity guard and transient suppressor bridge (see Fig. 6)			2 x BAS11 and 2 x BZW03-..
X1	quartz crystal			4,783 MHz

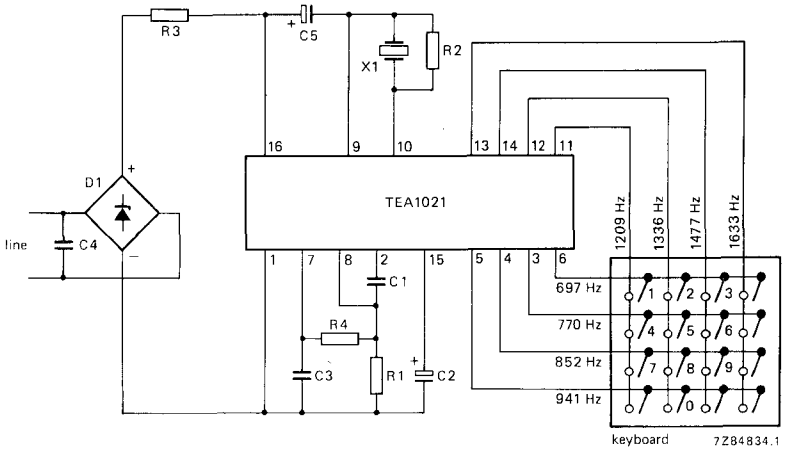


Fig. 4 Application diagram with second-order filter to minimize harmonic distortion (meets CEPT CS203 requirements).

R1	metal film resistor	MR16	1%	see Fig. 7
R2	metal film resistor	SFR16	5%	3,3 MΩ
R3	metal film resistor	SFR16	5%	18 Ω
R4	metal film resistor	SFR16	5%	270 kΩ
C1	metallized polyester film capacitor			see Fig. 7
C2	solid aluminium electrolytic capacitor		6,3 V	4,7 μF
C3	miniature ceramic plate capacitor			180 pF
C4	metallized polyester film capacitor			22 nF
C5	solid aluminium electrolytic capacitor		6,3 V	4,7 μF
D1	transient suppressor bridge (see Fig. 6)			2 x BAS11 and 2 x BZW03-..
X1	quartz crystal			4,783 MHz

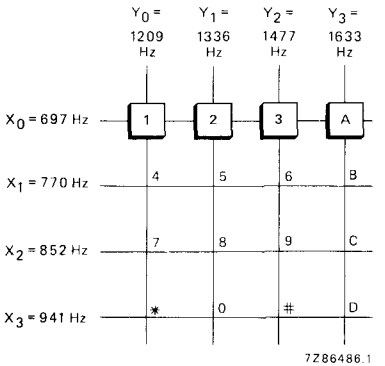


Fig. 5 Allocation of dialling tones to keyboard functions.

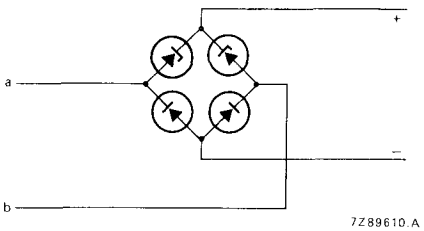


Fig. 6 Polarity-guard and line-transient suppression bridge D1.
Diodes 2 x BAS11.
Voltage regulators 2 x BZW03-..

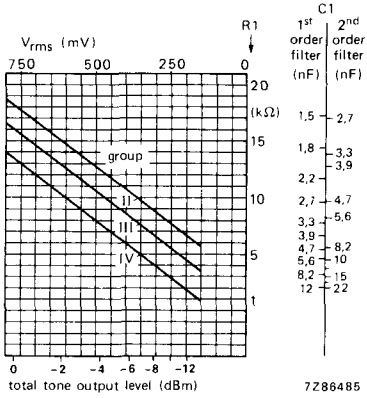


Fig. 7 Level adjustment (see Figs 3 and 4).

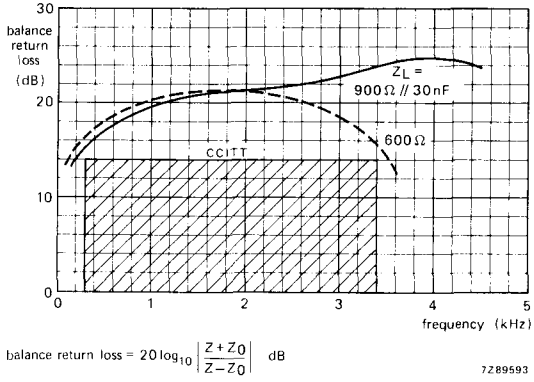


Fig. 8 Balance return loss measured with external components as in Fig. 4.

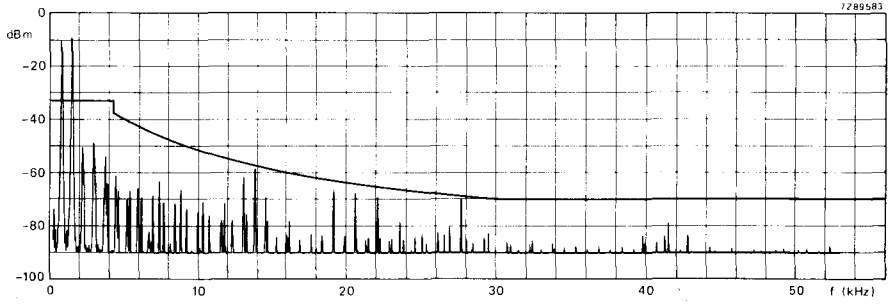


Fig. 9 Frequency spectrum of circuit with second-order filter (see Fig. 4).

APPLICATION (see Fig. 4)

Line matching

If there is an impedance match between the lines and the dialling circuit, the balance return loss will be high and reflections on the line will be highly damped. Figure 8 shows that the balance return loss when using the application diagram as shown in Fig. 4 is more than 14 dB. The variation of balance return loss with the frequency is largely caused by an impedance variation due to the low-pass filter capacitor (C2) and the radio-frequency interference filter capacitor C4. Since the highest line impedance that is likely to be encountered is 900 Ω the internal impedance of the dialling circuit is set at this level and can be reduced to match lower impedance lines by adding an external resistor between pins 1 and 16. If direct current must be eliminated a capacitor must be connected in series with the resistor.

– internal impedance Z_i = 900 Ω; no external resistor between pins 1 and 16.
– internal impedance Z_i = 600 Ω; external resistor between pins 1 and 16 = 2700 Ω.

Output level adjustment

The tone output levels are subject to some spread due to manufacturing tolerances and can be adjusted by selection of the value of the resistor connected to pin 8.
The level of the higher-frequency tone however is always 2 ± 0,7 dB above that of the lower-frequency tone. The total production of the circuits is therefore divided into groups. The group to which any of the integrated circuits belongs is identified by dots on the body of the circuit, the number of dots corresponding with the group number. The combined tone output level is shown as a function of resistor value with group number as a parameter in Fig. 7. After the resistor value has been selected to obtain the required tone output level, the value of the filter capacitor connected to the same pin must be determined. For passive first-order filters (Fig. 4) the time-constant (RC) must be 26 μs. For active second-order filters it must be 46 μs. These values accommodate the different attenuation levels for the various tone frequencies due to the 0,3 dB hump at the breakpoint of the filters.

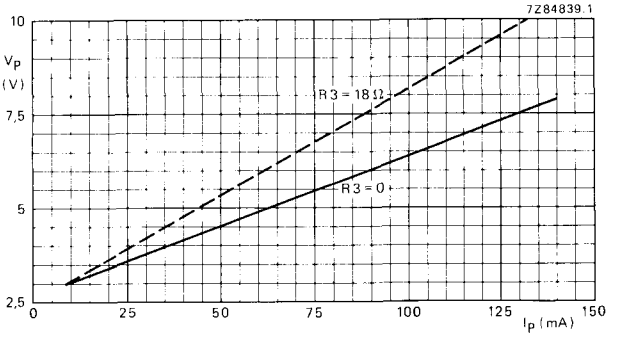


Fig. 10 D.C. characteristics.

TELEPHONE TRANSMISSION CIRCUIT FOR HANDSFREE LOUDSPEAKING

GENERAL DESCRIPTION

The TEA1042 is a bipolar integrated circuit performing all speech and line interface functions in electronic telephone sets. It is especially designed for handsfree loudspeaking equipment.

Its features are:

- Supplied from telephone line current
- Voltage regulator with adjustable d.c. voltage drop and d.c. resistance
- High and low-impedance handset microphone inputs
- High-impedance base microphone input
- Handset/base selection input
- Muting input for pulse or DTMF dialling
- Gain setting facility on all amplifiers
- Line current dependent gain control facility with corrections for the exchange supply voltage and its feeding bridge resistance
- Supply output for additional circuits.

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{line}	typ.	4,2 V
Line current operating range	I_{line}		10 to 140 mA
Telephone line impedance	$\|Z_{line}\|$	nom.	600 Ω
Supply current	I_{CC}	typ.	1 mA
Voltage gain, transmitting amplifier			
MIC1 input	A_{vd}	typ.	44,1 dB
MIC2 input	A_{vd}	typ.	20 dB
MIC3 input	A_{vd}	typ.	20 dB
DTMF input	A_{vd}	typ.	25,6 dB
Voltage gain, receiving amplifier	A_{vd}	typ.	27 dB
Gain adjustment range			
transmitting amplifier	ΔA_{vd}	typ.	± 6 dB
receiving amplifier	ΔA_{vd}	typ.	± 8 dB
Range of gain control with line current, all amplifiers	ΔA_{vd}	typ.	6 dB
Exchange supply voltage range	V_{exch}		24 to 60 V
Exchange feeding bridge resistance	R_{exch}		400 or 800 Ω
Operating ambient temperature range	T_{amb}		−25 to + 70 °C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

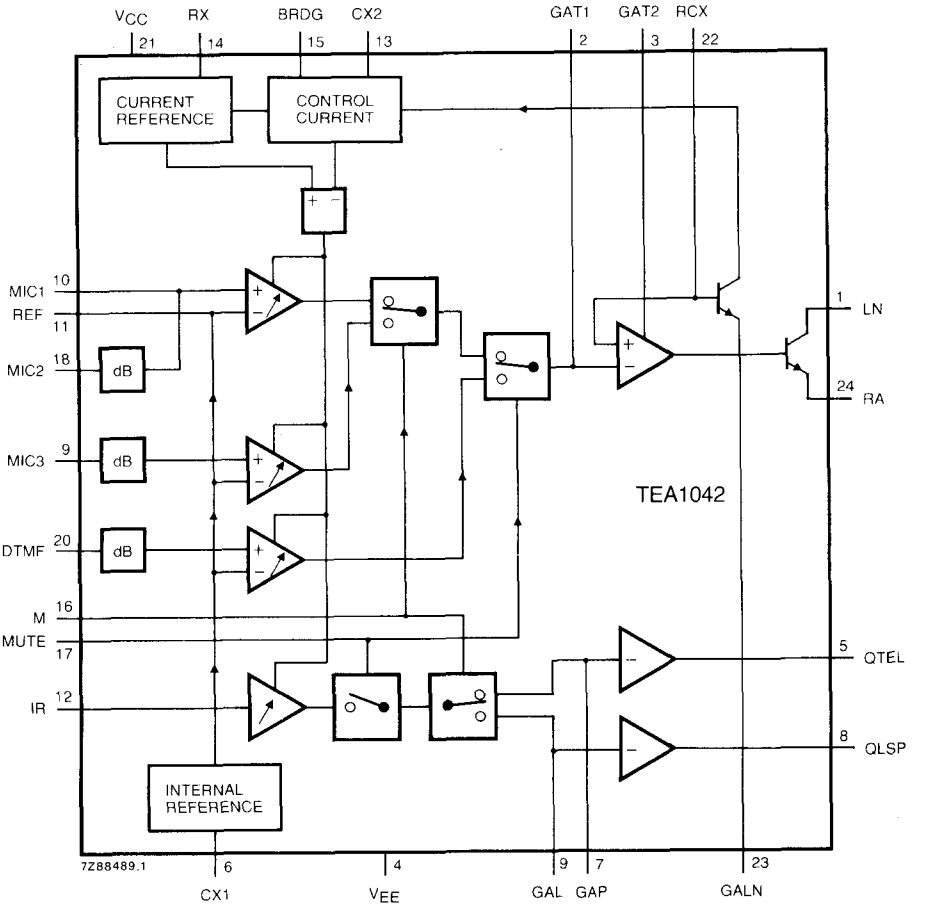


Fig. 1 Block diagram. The blocks marked dB are attenuators. The M and MUTE inputs operate analogue switches that activate or inhibit the inputs and outputs as required by their function.

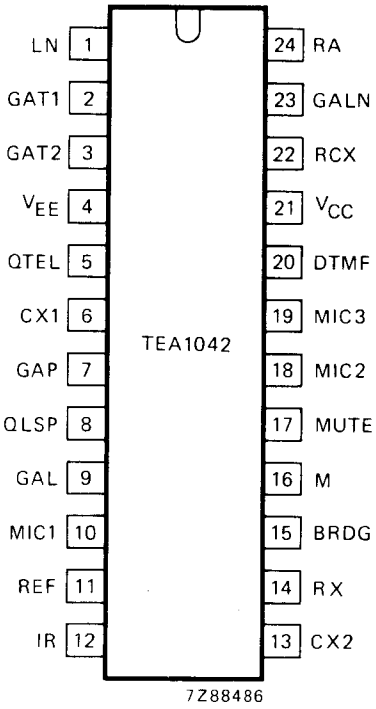


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAT1	gain adjustment; transmitting amplifier
3	GAT2	gain adjustment; transmitting amplifier
4	V_{EE}	negative line terminal
5	QTEL	handset telephone output
6	CX1	reference decoupling
7	GAP	gain adjustment; telephone amplifier
8	QLSP	loudspeaker preamplifier output
9	GAL	gain adjustment; loudspeaker preamplifier
10	MIC1	low-impedance handset microphone input
11	REF	reference voltage
12	IR	receiving amplifier input
13	CX2	external stabilizing capacitor
14	RX	external resistor
15	BRDG	selection input for gain control adaptation to feeding bridge impedance
16	M	mode (handset/base selection) input
17	MUTE	mute input
18	MIC2	high-impedance handset microphone input
19	MIC3	base microphone input
20	DTMF	dual-tone multi-frequency input
21	V_{CC}	positive supply
22	RCX	line voltage adjustment and voltage regulator decoupling
23	GALN	gain control with line current; all amplifiers
24	RA	d.c. resistance adjustment

FUNCTIONAL DESCRIPTION

The TEA1042 contains two receiving amplifiers, a transmitting amplifier, means to switch the inputs and the outputs, means to adjust the gain of all amplifiers individually, means to vary the gain with the line current and means to adjust the d.c. voltage drop and d.c. resistance. See the block diagram, Fig. 1.

Supply: LN, V_{CC}, V_{EE}, RA, CX1 and CX2 (pins 1, 21, 4, 24, 6 and 13)

The circuit is supplied from the line current, the arrangement is shown in Fig. 3. The circuit develops its own supply voltage at V_{CC} (pin 21). This supply voltage may also be used to supply an external circuit, e.g. a CMOS pulse or DTMF dialler or an electret microphone amplifier stage. The current available for this circuit depends on external components, see Fig. 4.

All line current has to flow through the circuit. If the line current exceeds the current required by the circuit itself via V_{CC} (pin 21), i.e. about 1 mA, plus the current required by the peripheral circuits connected to this pin, then the excess current is diverted via LN, the positive line terminal (pin 1), to RA (d.c. resistance adjustment; pin 24).

The minimum line voltage may be chosen by external resistor R5 and the variation with line current by external resistor R10. The circuit regulates the line voltage at $T_{amb} = 25\ ^{o}C$ to:

$$V_{line} = V_{LN} = \frac{R5 + R9}{R9} \times 0{,}62 + I_{LN} \times R10,$$

I_{LN} being the current diverted via LN.

A regulator decoupling capacitor has to be connected between RCX (pin 22) and V_{EE}, the negative line terminal (pin 4), a smoothing capacitor has to be connected between V_{CC} (pin 21) and V_{EE}, and a stabilizing capacitor between CX2 (pin 13) and V_{EE}. Further a decoupling capacitor has to be connected between CX1 (reference decoupling; pin 6) and V_{EE} (pin 4).

The dynamic impedance that the circuit presents to the line in the speech band is determined primarily by resistor R1 connected between LN (pin 1) and V_{CC} (pin 21).

Mode (handset/base selection) input M (pin 16)

The mode input permits selection of operation via the handset or via the base. A HIGH level on the M input or an open circuit selects handset operation, i.e. it activates the microphone inputs MIC1 and MIC2 and the handset telephone output QTEL. A LOW level on M selects the base microphone input MIC3 and the loudspeaker preamplifier output QLSP.

Microphone inputs MIC1, MIC2 and MIC3 (pins 10, 18 and 19)

Handset and base may be equipped with a sensitive microphone, e.g. an electret microphone with pre-amplifier. This has to be connected to the MIC2 or MIC3 input respectively. The available gain from these inputs is typ. 20 dB.

The handset may also be equipped with an insensitive low-impedance microphone, e.g. a dynamic or magnetic microphone. This has to be connected between MIC1 (pin 10) and (REF (pin 11). The available gain from this input is typ. 44,1 dB.

Dual-tone multi-frequency input DTMF and mute input MUTE (pins 20 and 17)

A HIGH level on the MUTE input inhibits all microphone inputs and the telephone and loudspeaker outputs QTEL and QLSP and enables the DTMF input, a LOW level does the reverse. Switching the MUTE input will not produce any clicks on the line or in the telephone or loudspeaker. The available gain from the DTMF input is typ. 25,6 dB.

Telephone output QTEL and loudspeaker preamplifier output QLSP (pins 5 and 8)

As described before, the M input determines which of the outputs QTEL and QLSP will be activated. The receiving amplifier input IR (pin 12) is the input for both outputs. For both outputs the available gain is typ. 27 dB. The output QTEL is intended for telephone capsules with an impedance of 150 Ω or more. The QLSP output is intended to drive a power amplifier. Its output impedance is less than 1 kΩ.

Gain adjustment: GAT1, GAT2, GAP and GAL (pins 2, 3, 7 and 9)

The gain of the transmitting amplifier may be adjusted by an external resistor R2 connected between GAT1 and GAT2 (pins 2 and 3; see Fig. 9). This adjustment influences the sensitivity of the inputs MIC1, MIC2, MIC3 and DTMF to the same amount. The gain is proportional to R2 and inversely proportional to R10 and R12.

The gain of the telephone amplifier may be adjusted by an external resistor R14 between GAP (pin 7) and CX1 (pin 6). The gain is proportional to R14 and inversely proportional to R12.

The gain of the loudspeaker preamplifier may be adjusted by an external resistor R13 between GAL (pin 9) and CX1 (pin 6). The gain is proportional to R13 and inversely proportional to R12.

***Gain control with line current*: GALN** (pin 23)

The circuit offers a facility to automatically vary the gain of all its amplifiers with the line current. In this way the circuit compensates for differences in line attenuation. The variation is accomplished by connecting an external resistor R11 between GALN (pin 23) and V_{EE} (pin 4). The value of this resistor should be chosen in accordance with the supply voltage of the exchange (see Figs 5 and 6).

If no gain variation with line current is required the GALN connection may be left open. All amplifiers have their maximum gain then.

Selection input for gain control adaptation to feeding bridge impedance: BRDG (pin 15)

A LOW level at the BRDG input optimizes the gain control characteristics of the circuit for a 400 Ω feeding bridge in the exchange, a HIGH level for 800 Ω.

Side tone suppression

In the circuit diagram shown in Fig. 9 side tone suppression is obtained with components C2, R3, R4, R7 and R8. Their component values have to be chosen to suit the cable type used. This network attenuates the signal from the telephone line to the IR input of the receiving amplifier. This attenuation may be adjusted by choosing the value of R7 without affecting the side tone suppression.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current			
d.c.	I_{line}	max.	140 mA
non-repetitive ($t < 100$ h)	I_{line}	max.	250 mA
Storage temperature range	T_{stg}	−40 to +125	°C
Operating ambient temperature range	T_{amb}	−25 to +70	°C
Junction temperature	T_j	max.	150 °C

CHARACTERISTICS

I_{line} = 10 to 140 mA; f = 1000 Hz; T_{amb} = 25 °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 21)					
Line voltage					
I_{line} = 15 mA	V_{line}	4	4,2	4,4	V
I_{line} = 50 mA	V_{line}	–	–	5,8	V
I_{line} = 100 mA	V_{line}	–	–	7,3	V
Variation with temperature	$-\Delta V_{line}/\Delta T$	8	10	12	mV/K
Line current operating rage	I_{line}	10	–	140	mA
Supply current at V_{CC} = 2 V	I_{CC}	–	–	1	mA
Mode (handset/base selection) input M (pin 16)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{16}$	–	8	20	μA
Attenuation of non-selected signals	$-\Delta A_{vd}$	45	–	–	dB
Low-impedance handset microphone input MIC1 and reference voltage pin REF (pins 10 and 11)					
Input impedance	$\lvert Z_{10\text{-}11}\rvert$	–	3	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	43,1	44,1	45,1	dB
High-impedance handset microphone input MIC2 (pin 18)					
Input impedance	$\lvert Z_{18\text{-}4}\rvert$	40	48	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	19	20	21	dB
Base microphone input MIC3 (pin 19)					
Input impedance	$\lvert Z_{19\text{-}4}\rvert$	40	48	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	19	20	21	dB
DTMF input (pin 20)					
Input impedance	$\lvert Z_{20\text{-}4}\rvert$	10	15	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	24,6	25,6	26,6	dB
Gain adjustment pins; transmitting amplifier: GAT1 and GAT2 (pins 2 and 3)					
Gain adjustment range	ΔA_{vd}	–	± 6	–	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to +45 °C	ΔA_{vd}	–	± 0,5	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Transmitting amplifier output LN (pin 1)					
Output voltage at I_{line} = 15 mA; R_{line} = 600 Ω; d = 2%	$v_{LN(rms)}$	1,4	–	–	V
Psophometrically weighted* noise output voltage at I_{line} = 15 mA; R_{line} = 600 Ω	$v_{LN(rms)}$	–	245	–	μV
MUTE input (pin 17)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{17}$	–	8	20	μA
Attenuation of non-selected signals	$-\Delta A_{vd}$	45	–	–	dB
Receiving amplifier input IR (pin 12)					
Input impedance	$\lvert Z_{12\text{-}4}\rvert$	–	10	–	kΩ
Telephone output QTEL (pin 5)					
Voltage gain at I_{line} = 15 mA; R_{load} = 150 Ω; R13 = 15 kΩ; see Fig. 8	A_{vd}	26	27	28	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to +45 °C	ΔA_{vd}	–	± 0,5	–	dB
Maximum output voltage at I_{line} = 15 mA; R_{load} = 150 Ω; d = 2%	$v_{O(rms)}$	350	–	–	mV
Psophometrically weighted* noise output voltage at I_{line} = 15 mA	$v_{O(rms)}$	–	40	–	μV
Gain adjustment pin; telephone amplifier: GAP (pin 7)					
Gain adjustment range	ΔA_{vd}	–	± 8	–	dB
Loudspeaker preamplifier output QLSP (pin 8)					
Voltage gain at I_{line} = 15 mA; R_{load} = 10 kΩ; R14 = 15 kΩ; see Fig. 8	A_{vd}	–	27	–	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature	ΔA_{vd}	–	± 0,5	–	dB
Psophometrically weighted* noise output voltage at I_{line} = 15 mA	$v_{O(rms)}$	–	40	–	μV
Output impedance	$\lvert Z_{8\text{-}4}\rvert$	–	–	1	kΩ
Gain adjustment pin; loudspeaker preamplifier: GAL (pin 9)					
Gain adjustment range	ΔA_{vd}	–	± 8	–	dB

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Selection input for gain control adaptation to feeding bridge impedance BRDG (pin 15)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{15}$	–	8	20	μA
Gain control with line current pin GALN (pin 23)					
Gain control range	ΔA_{vd}	–	6	–	dB
Highest line current for maximum gain, R11 = 105 kΩ;					
BRDG = HIGH (R_{exch} = 800 Ω)	I_{line}	22,5	25	27,5	mA
BRDG = LOW (R_{exch} = 400 Ω)	I_{line}	31,5	35	38,5	mA
Lowest line current for minimum gain, R11 = 105 kΩ;					
BRDG = HIGH (R_{exch} = 800 Ω)	I_{line}	49,5	55	60,5	mA
BRDG = LOW (R_{exch} = 400 Ω)	I_{line}	81	90	99	mA

* P53 curve.

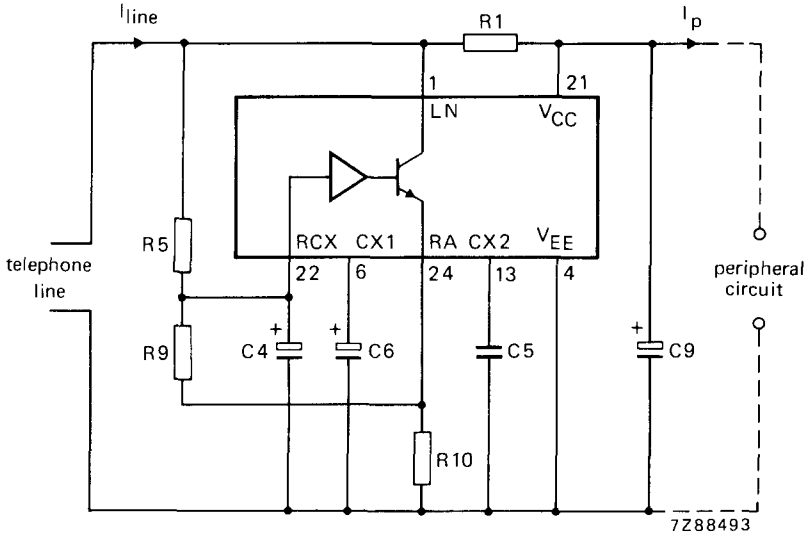


Fig. 3 Supply arrangement.

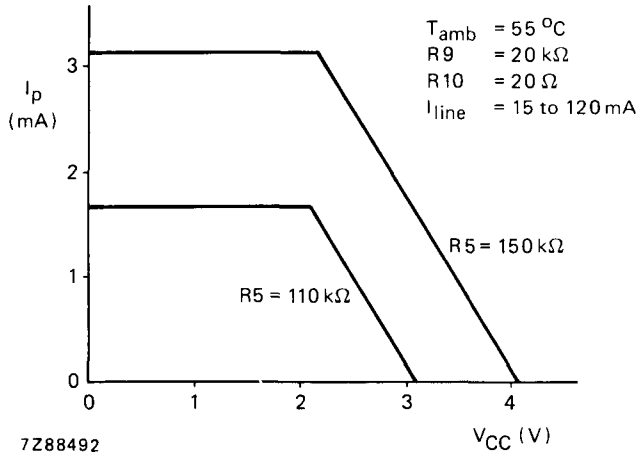


Fig. 4 Maximum current I_p available from V_{CC} for external (peripheral) circuits.

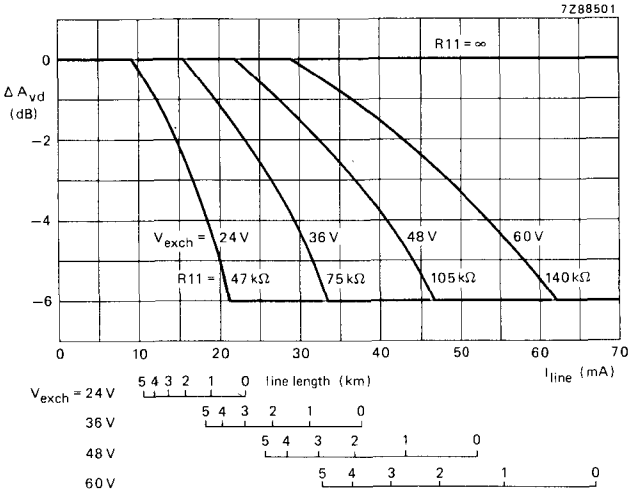


Fig. 5 Gain variation with line current, with R11 as a parameter, and with the BRDG input HIGH, i.e. the circuit optimized for 800 Ω. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

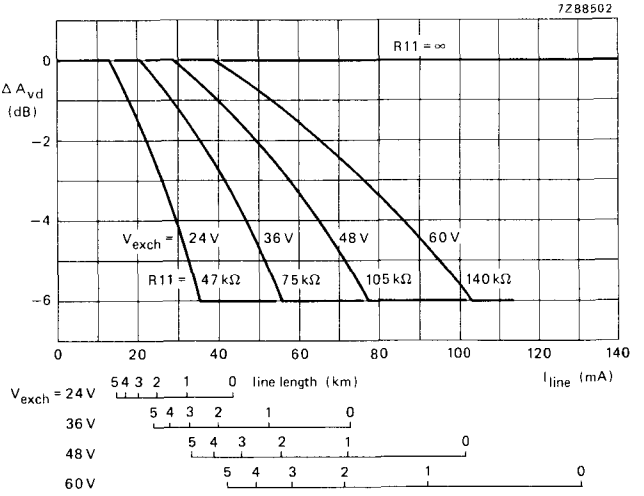


Fig. 6 Gain variation with line current, with R11 as a parameter, and with the BRDG input LOW, i.e. the circuit optimized for 400 Ω. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

DEVELOPMENT SAMPLE DATA

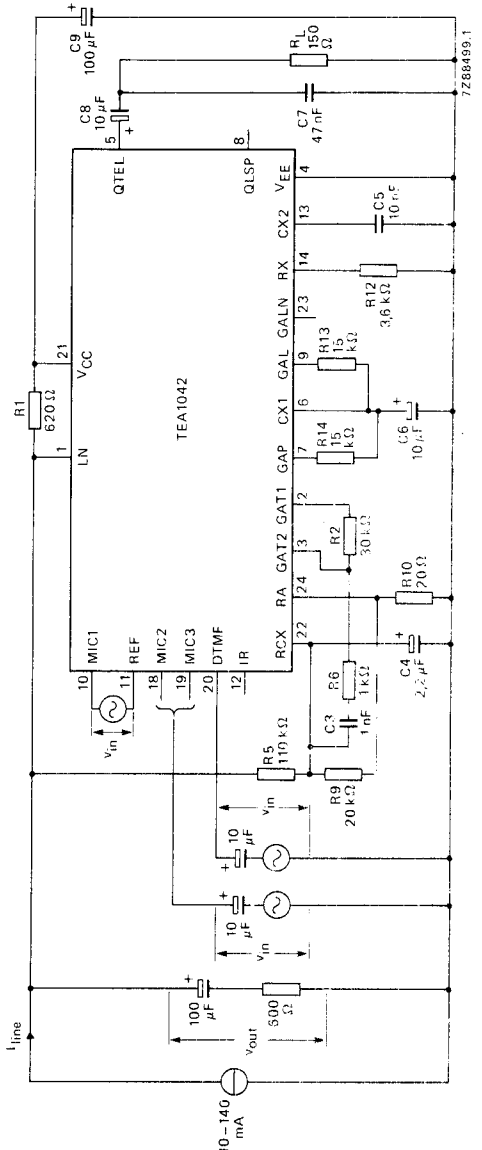


Fig. 7 Test circuit for defining voltage gain of MIC1, MIC2, MIC3 and DTMF inputs. Gain is defined as: $A_{vd} = 20 \log |v_{out}/v_{in}|$. For measuring the MIC1 or MIC2 input the M input should be HIGH and the MUTE input LOW, for measuring the MIC3 input M and MUTE should both be LOW and for measuring the DTMF input M and MUTE should be HIGH. Inputs not under test should be open.

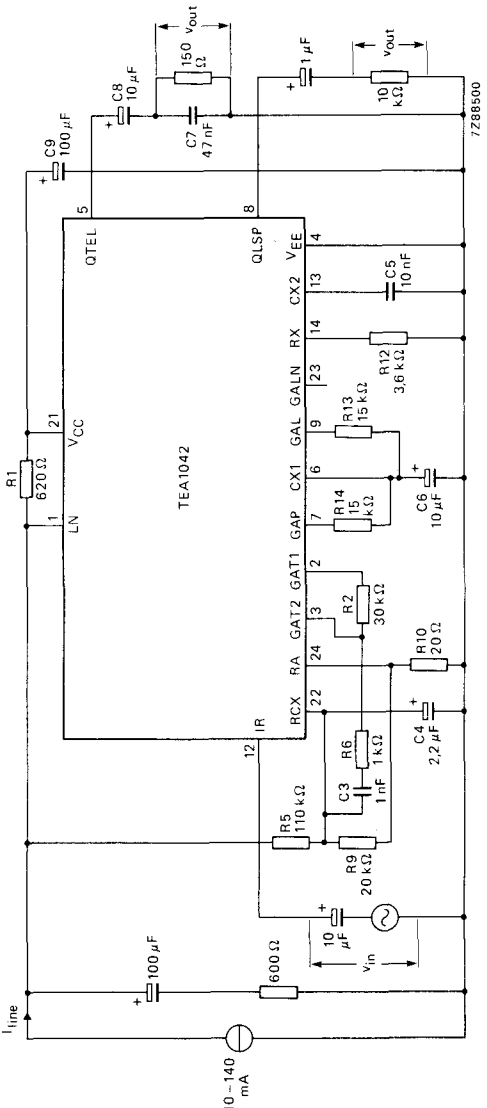


Fig. 8 Test circuit for defining voltage gain of QTEL and QLSP outputs. Gain is defined as: $A_{vd} = 20 \log |v_{out}/v_{in}|$. For measuring the QTEL output the M input should be HIGH and the MUTE input LOW, for measuring the QLSP output M and MUTE should both be LOW.

DEVELOPMENT SAMPLE DATA

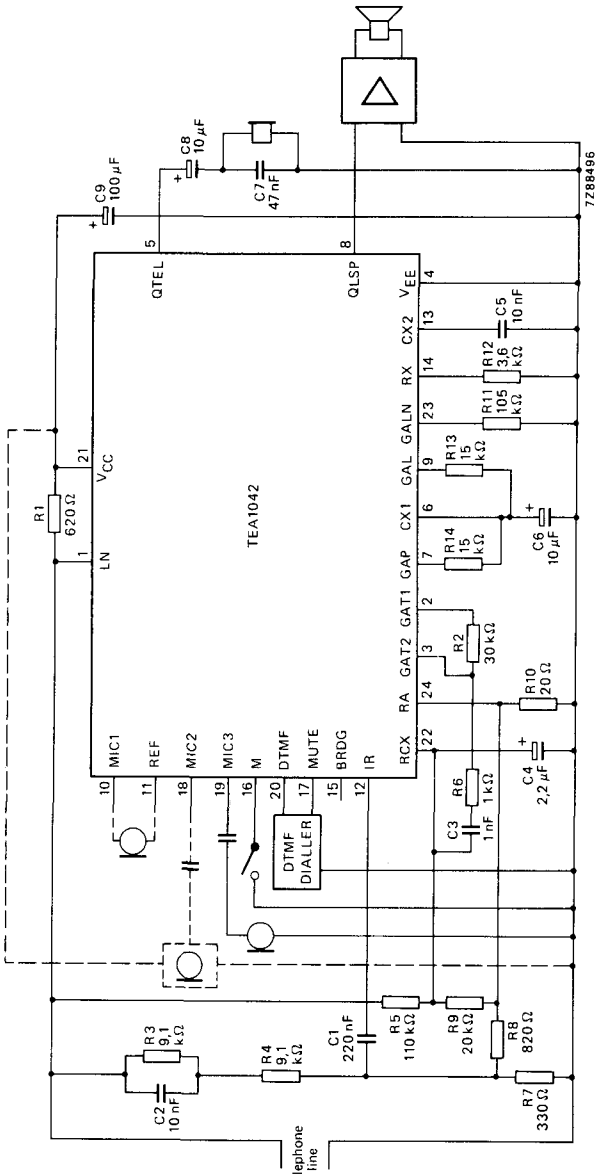


Fig. 9 Typical application of the TEA1042 in an electronic handsfree telephone set. The connections to the MIC1 and MIC2 inputs are alternatives. The connection to the BRDG input is not shown, see the Functional Description. The diagram does not show voice switches and associated control circuits *required in a practical circuit* for stable loudspeaking operation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

DTMF GENERATOR FOR TELEPHONE DIALLING

This integrated circuit is a dual-tone multi-frequency (DTMF) generator, supplying frequency combinations (in accordance with CCITT recommendations) for use in pushbutton telephones, with a single contact keyboard.

The various frequencies are derived from a crystal-controlled oscillator followed by a sinewave synthesizer.

I^2L technology allows digital and analogue functions to be implemented on the same chip. The built in current/voltage regulator and active output amplifier substantially reduce the number of external components. Only a quartz crystal of 4,78 MHz and a few resistors and capacitors are required.

The circuit features:

- wide operating line current range
- operating voltage down to 1,3 volt (standby 0,7 volt)
- no individual tone level adjustment required
- temperature stabilized signal levels
- line current independent signal levels
- output stage and line regulator included
- all pins protected against electrostatic discharges
- two key roll-over provided
- operates with a low cost quartz crystal
- few external components required
- electronic mute facility
- low power consumption in standby mode

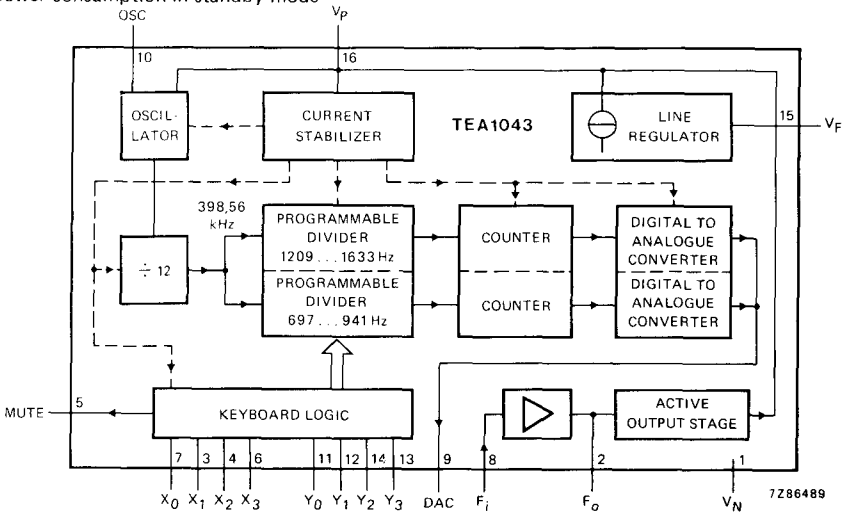


Fig. 1 Block diagram (dotted lines are stabilized supply rails).

PACKAGE OUTLINES

TEA1043P: 16-lead DIL, plastic (SOT-38).
TEA1043D: 16-lead DIL, ceramic (SOT-74B).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current	I_P	max.	150	mA
Surge current ($t_p < 250\ \mu s$)	I_S	max.	850	mA
Input series resistance	R_s	min.	18	Ω
Operating ambient temperature range	T_{amb}	−25 to +70		°C
Storage temperature range	T_{stg}	−55 to +125		°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS

V_N = 0 V; T_{amb} = −25 to +70 °C unless otherwise specified.

	symbol	min.	typ.	max.	unit	conditions
operating voltage						
d.c.; $-I_L$ = 10 mA	V_L	2,8	3,3	3,8	V	
line current						
level − 7 dBm	I_L	10	8	120	mA	
level − 2 dBm	I_L	12	9	120	mA	
standby mode	I_L	–	50	–	μA	
internal impedance	Z_i	640	900	1150	Ω	300 − 3400 Hz
tone frequencies						
low	f_{x0}	–	697	–	Hz	
	f_{x1}	–	770	–	Hz	
	f_{x2}	–	852	–	Hz	frequency
	f_{x3}	–	941	–	Hz	quartz crystal 4 782 720 Hz
high	f_{y0}	–	1209	–	Hz	
	f_{y1}	–	1336	–	Hz	
	f_{y2}	–	1477	–	Hz	
	f_{y3}	–	1633	–	Hz	
dividing error		–	–	0,11	%	
nom. output level						
lower freq.	V_{LG}	–	–	−6	dBm	adjustable
higher freq.	V_{HG}	–	–	−4	dBm	adjustable
tolerance on output level	ΔV_o	2	–	2	dB	
pre-emphasis		1,3	2	2,7	dB	without filter components
distortion with respect to total level	d_{tot}	–	−34	−24	dB	maximum tone level and with first-order filter
start up time	t_s	–	5	–	ms	with recommended external components
mute output sink current	I_{MS}	–	–	0,5	mA	
switch bounce elimination	t_{sb}	1	1,5	2	ms	
required keyboard resistance						
contact on	$R_{k\ on}$	–	–	10	kΩ	
contact off	$R_{k\ off}$	500	–	–	kΩ	

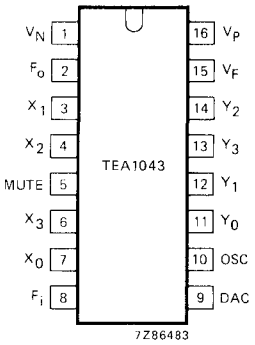


Fig. 2 Pin designation.

PINNING

1	V_N	negative supply
2	F_o	filter output
3	X1	row keyboard input 1
4	X2	row keyboard input 2
5	MUTE	mute output
6	X3	row keyboard input 3
7	X0	row keyboard input 0
8	F_i	filter input/ input audio amplifier
9	DAC	output DAC/DTMF tones
10	OSC	oscillator input
11	Y0	column keyboard input 0
12	Y1	column keyboard input 1
13	Y3	column keyboard input 3
14	Y2	column keyboard input 2
15	V_F	input low-pass filter
16	V_P	positive supply

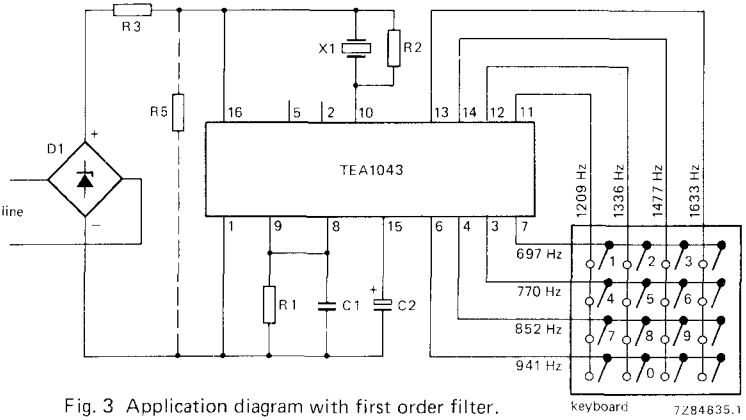


Fig. 3 Application diagram with first order filter.

R1	metal film resistor	MR16	1%	see Fig. 7
R2	metal film resistor	SFR16	5%	3,3 MΩ
R3	metal film resistor	SFR16	5%	18 Ω
R5	metal film resistor	SFR16	5%	2700 Ω (for Z_o = 600 Ω; no resistor for Z_o = 900 Ω)
C1	metallized polyester film capacitor			see Fig. 7
C2	solid aluminium electrolytic capacitors		6,3 V	4,7 μF
D1	polarity guard and transient suppressor bridge (see Fig. 6)			2 x BAS11 and 2 x BZW03–..
X1	quartz crystal			4, 783 MHz

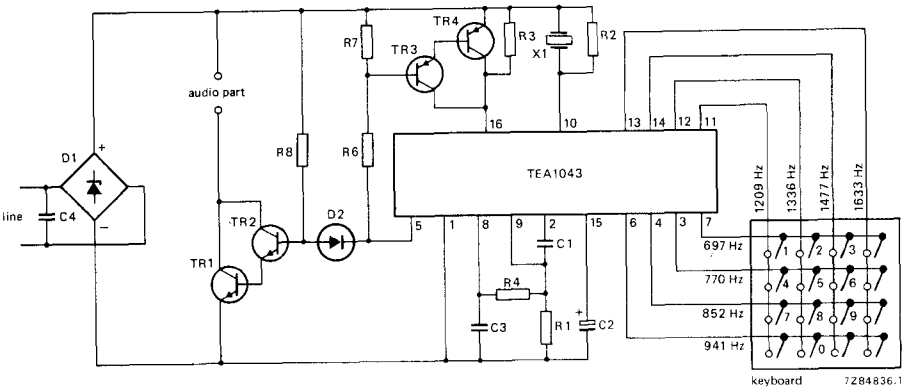


Fig. 4 Application diagram with electronic mute switch and second-order filter.

R1	metal film resistor	MR16	1%	see Fig. 7
R2	metal film resistor	SFR16	5%	3,3 MΩ
R3	metal film resistor	SFR16	5%	39 kΩ (depends on audio voltage)
R4	metal film resistor	SFR16	5%	270 kΩ
R6	metal film resistor	SFR16	5%	330 kΩ
R7	metal film resistor	SFR16	5%	820 kΩ
R8	metal film resistor	SFR16	5%	470 kΩ
C1	metallized polyester film capacitor			see Fig. 7
C2	solid aluminium electrolytic capacitor		6,3 V	4,7 μF
C3	miniature ceramic plate capacitor			180 pF
C4	metallized polyester film capacitor			22 nF
D1	transient suppressor bridge (see Fig. 6)	2 x BAS11 and 2 x BZW03–..		
D2	diode	BAW62		
TR1	transistor	BC338		
TR2	transistor	BC548		
TR3	transistor	BC558		
TR4	transistor	BC328		
X1	quartz crystal			4,783 MHz

If TR1/TR2 = BSR50 and TR3/TR4 = BSR60 then R6 = 39 kΩ, R7 = 120 kΩ and R8 = 33 kΩ.

An additional choke of 15 mH in series with the circuit is required to meet the CEPT CS203 distortion requirements.

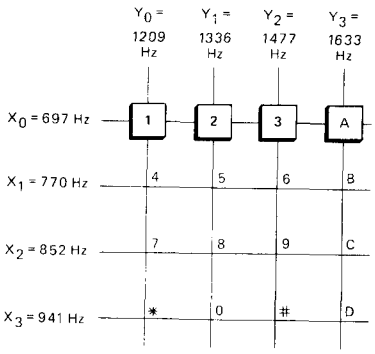


Fig. 5 Allocation of dialling tones to keyboard functions.

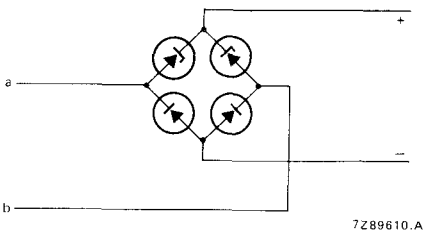


Fig. 6 Polarity-guard and line-transient suppression bridge D1. Diodes 2 x BAS11. Voltage regulators 2 x BZW03–..

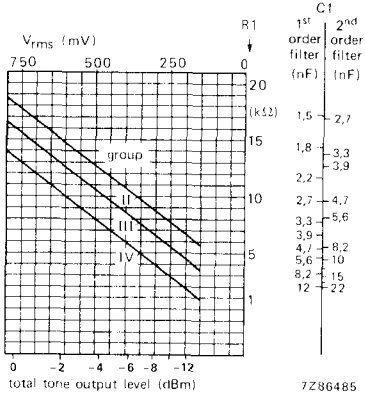


Fig. 7 Level adjustment (see Figs 3 and 4).

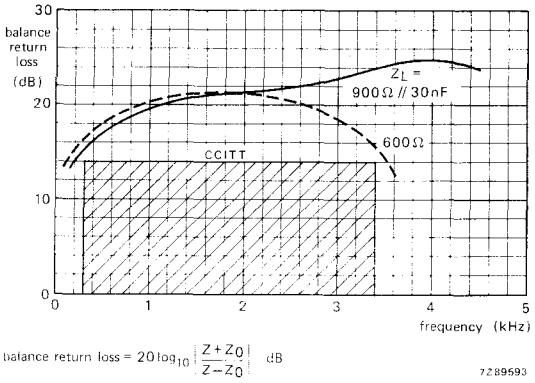


Fig. 8 Balance return loss measured with external components as in Fig. 4.

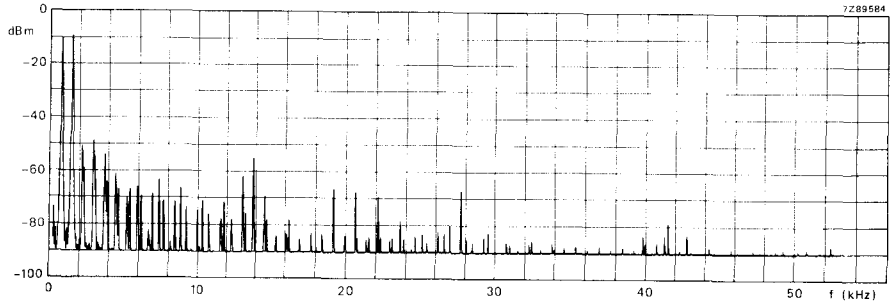


Fig. 9 Frequency spectrum of circuit with second order filter (see Fig. 4).

APPLICATION (see Fig. 4)

Line matching

If there is an impedance match between the lines and the dialling circuit, the balance return loss will be high and reflections on the line will be highly damped. Figure 8 shows that the balance return loss when using the application diagram as shown in Fig. 4 is more than 14 dB. The variation of balance return loss with the frequency is largely caused by an impedance variation due to the low-pass filter capacitor (C2) and the radio-frequency interference filter capacitor C4. Since the highest line impedance that is likely to be encountered is 900 Ω the internal impedance of the dialling circuit is set at this level and can be reduced to match lower impedance lines by adding an external resistor between pins 1 and 16. If direct current must be eliminated a capacitor must be connected in series with the resistor.

– internal impedance Z_i = 900 Ω; no external resistor between pins 1 and 16.
– internal impedance Z_i = 600 Ω; external resistor between pins 1 and 16 = 2700 Ω.

Output level adjustment

The tone output levels are subject to some spread due to manufacturing tolerances and can be adjusted by selection of the value of the resistor connected to pin 8.
The level of the higher-frequency tone however is always 2 ± 0,7 dB above that of the lower-frequency tone. The total production of the circuits is therefore divided into groups. The group to which any of the integrated circuits belongs is identified by dots on the body of the circuit, the number of dots corresponding with the group number. The combined tone output level is shown as a function of resistor value with group number as a parameter in Fig. 7. After the resistor value has been selected to obtain the required tone output level, the value of the filter capacitor connected to the same pin must be determined. For passive first-order filters (Fig. 4) the time-constant (RC) must be 26 μs. For active second-order filters it must be 46 μs. These values accommodate the different attenuation levels for the various tone frequencies due to the 0,3 dB hump at the breakpoint of the filters.

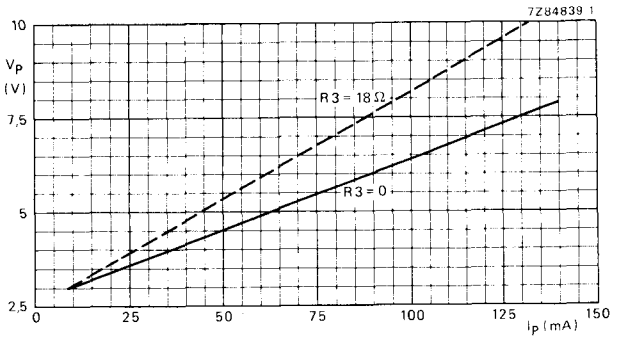


Fig. 10 D.C. characteristics.

DTMF GENERATOR FOR TELEPHONE DIALLING

This integrated circuit is a dual-tone multi-frequency (DTMF) generator, supplying frequency combinations (in accordance with CCITT recommendations) for use in pushbutton telephones, with a single contact keyboard.

The various frequencies are derived from a crystal-controlled oscillator followed by a sinewave synthesizer.

I^2L technology allows digital and analogue functions to be implemented on the same chip. The built in current/voltage regulator and active output amplifier substantially reduce the number of external components. Only a quartz crystal of 4,78 MHz and a few resistors and capacitors are required.

The circuit features:
- wide operating line current range
- operating voltage down to 1,3 volt (standby 0,7 volt)
- no individual tone level adjustment required
- temperature stabilized signal levels
- line current independent signal levels
- output stage and line regulator included
- all pins protected against electrostatic discharges
- two key roll-over provided
- operates with a low cost quartz crystal
- few external components required
- electronic mute facility
- adjustable impedance
- low power consumption in standby mode

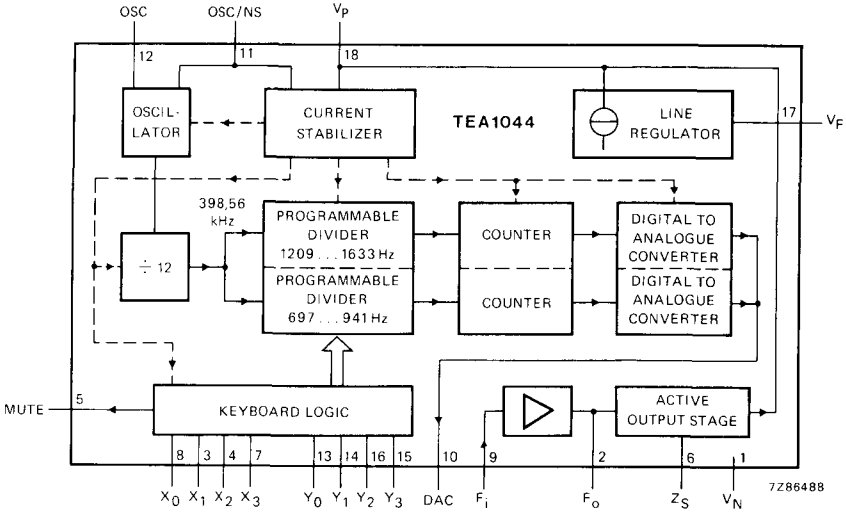


Fig. 1 Block diagram (dotted lines are stabilized supply rails).

PACKAGE OUTLINES

TEA1044P: 18-lead DIL, plastic (SOT-102A).
TEA1044D: 18-lead DIL, ceramic (SOT-133).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current	I_P	max.	150 mA
Surge current ($t_p < 250\ \mu s$)	I_S	max.	850 mA
Input series resistance	R_s	min.	18 Ω
Operating ambient temperature range	T_{amb}	−25 to	+ 70 °C
Storage temperature range	T_{stg}	−55 to	+ 125 °C
Junction temperature	T_j	max.	125 °C

CHARACTERISTICS

V_N = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified.

	symbol	min.	typ.	max.	unit	conditions
operating voltage d.c.; $-I_L$ = 10 mA	V_L	2,8	3,3	3,8	V	
line current						
level − 7 dBm	I_L	10	8	120	mA	
level − 2 dBm	I_L	12	9	120	mA	
standby current	I_{LS}	–	50	–	μA	
internal impedance	Z_i	640	900	1150	Ω	300 − 3400 Hz
tone frequencies						
low	f_{x0}	–	697	–	Hz	frequency quartz crystal 4 782 720-Hz
	f_{x1}	–	770	–	Hz	
	f_{x2}	–	852	–	Hz	
	f_{x3}	–	941	–	Hz	
high	f_{y0}	–	1209	–	Hz	
	f_{y1}	–	1336	–	Hz	
	f_{y2}	–	1477	–	Hz	
	f_{y3}	–	1633	–	Hz	
dividing error		–	–	0,11	%	
nom. output level						
lower frequency	V_{LG}	–	–	−6	dBm	adjustable
higher frequency	V_{HG}	–	–	−4	dBm	adjustable
tolerance on output level	ΔV_o	2	–	2	dB	
pre-emphasis		1,3	2	2,7	dB	without filter components
distortion with respect to total level	d_{tot}	–	−34	−24	dB	maximum tone level and with first-order filter
start up time	t_s	–	5	–	ms	with recommended external components
mute output sink current	I_{MS}	–	–	0,5	mA	
switch bounce elimination	t_{sb}	1	1,5	2	ms	
required keyboard resistance						
contact on	$R_{k\ on}$	–	–	10	kΩ	
contact off	$R_{k\ off}$	500	–	–	kΩ	

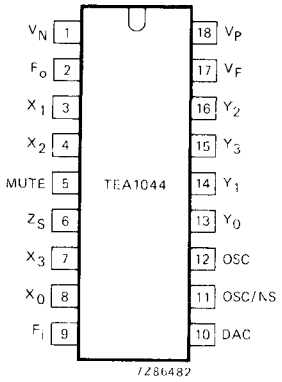


Fig. 2 Pin designation.

PINNING

1	V_N	negative supply
2	F_o	filter output
3	X1	row keyboard input 1
4	X2	row keyboard input 2
5	MUTE	*mute output*
6	Z_S	impedance setting
7	X3	row keyboard input 3
8	X0	row keyboard input 0
9	F_i	filter input/input audio amplifier
10	DAC	output DAC/DTMF tones
11	OSC/NS	oscillator/noise suppression output
12	OSC	oscillator input
13	Y0	column keyboard input 0
14	Y1	column keyboard input 1
15	Y3	column keyboard input 3
16	Y2	column keyboard input 2
17	V_F	input low-pass filter
18	V_P	positive supply

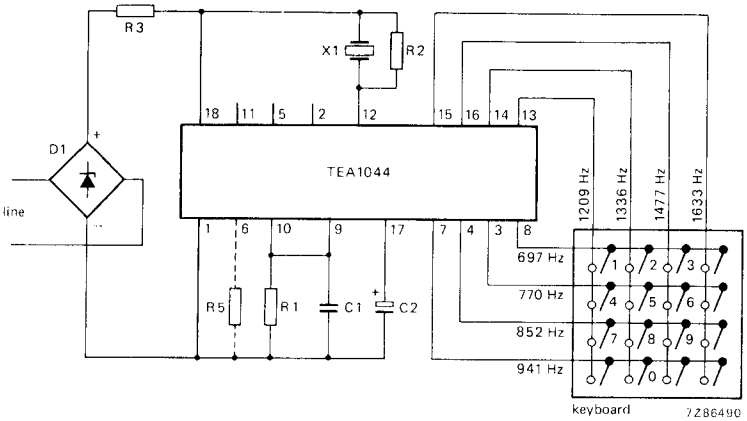


Fig. 3 Application diagram with first-order filter.

R1	metal film resistor	MR16	1%	see Fig. 7
R2	metal film resistor	SFR16	5%	3,3 MΩ
R3	metal film resistor	SFR16	5%	18 Ω
R5	metal film resistor	SFR16	5%	240 Ω (for Z_o = 600 Ω) no resistor for Z_o = 900 Ω
C1	metallized polyester film capacitor			see Fig. 7
C2	solid aluminium electrolytic capacitor		6,3 V	4,7 μF
D1	polarity quard and transient suppressor bridge (see Fig. 6)			2 x BAS11 and 2 x BZW03-..
X1	quartz crystal			4,783 MHz

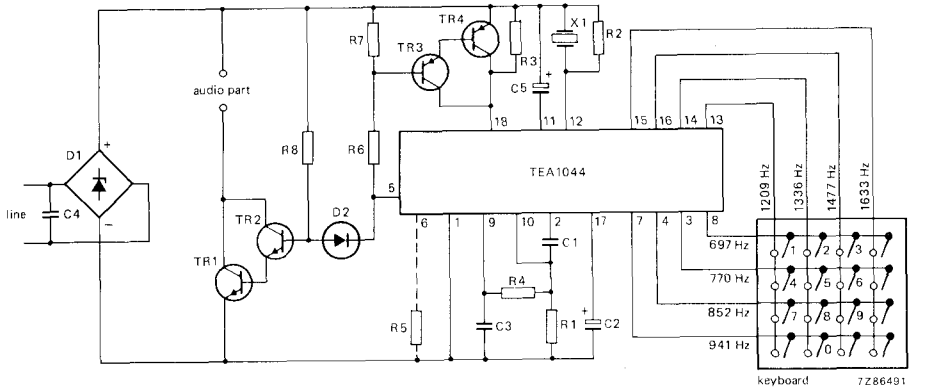


Fig. 4 Application diagram with electronic mute switch and second-order filter (meets CEPT CS203 requirements).

R1	metal film resistor	MR16	1%	see Fig. 7
R2	metal film resistor	SFR16	5%	3,3 MΩ
R3	metal film resistor	SFR16	5%	39 kΩ (depends on audio voltage)
R4	metal film resistor	SFR16	5%	270 kΩ
R5	metal film resistor	SFR16	5%	240 Ω (for Z_o = 600 Ω; no resistor for Z_o = 900 Ω)
C1	metallized polyester film capacitor			see Fig. 7
C2	solid aluminium electrolytic capacitor		6,3 V	4,7 μF
C3	miniature ceramic plate capacitor			180 pF
C4	metallized polyester film capacitor			22 nF
C5	solid aluminium electrolytic capacitor		6,3 V	4,7 μF
D1	transient suppressor bridge (see Fig. 6)			2 x BAS11 and 2 x BZW03-..
D2	diode	BAW62		
TR1/TR2	transistors	BC338/BC548		
TR3/TR4	transistors	BC558/BC328		
X1	quartz crystal			4,783 MHz

If TR1/TR2 = BSR50 and TR3/TR4 = BSR60 then R6 = 39 kΩ, R7 = 120 kΩ and R8 = 33 kΩ

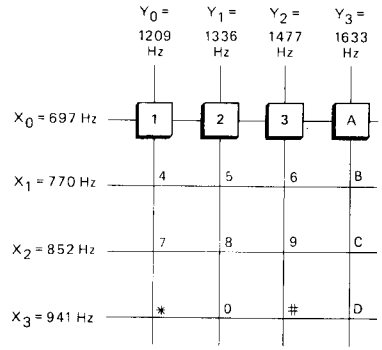


Fig. 5 Allocation of dialling tones to keyboard functions.

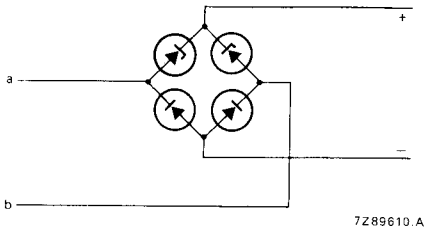


Fig. 6 Polarity-guard and line-transient suppression bridge D1. Diodes 2 x BAS11. Voltage regulators 2 x BZW03-..

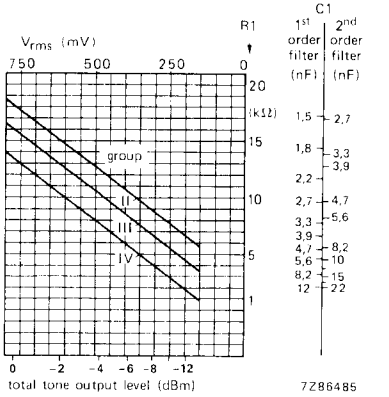


Fig. 7 Level adjustment (see Figs 3 and 4).

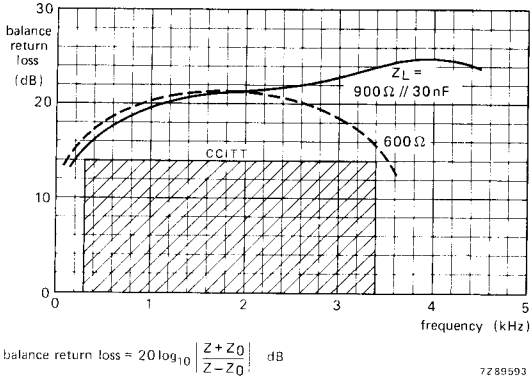


Fig. 8 Balance return loss measured with external components as in Fig. 4.

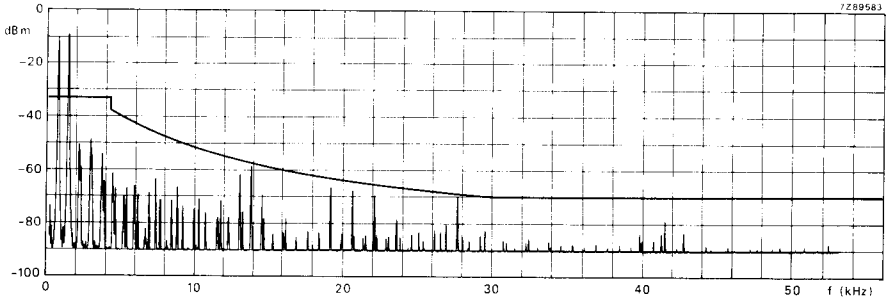


Fig. 9 Frequency spectrum of circuit with second-order filter (see Fig. 4).

APPLICATION (see Fig. 4)

Line matching

If there is an impedance match between the lines and the dialling circuit, the balance return loss will be high and reflections on the line will be highly damped. Figure 8 shows that the balance return loss when using the application diagram as shown in Fig. 4 is more than 14 dB. The variation of balance return loss with the frequency is largely caused by an impedance variation due to the low-pass filter capacitor (C2) and the radio-frequency interference filter capacitor C4. Since the highest line impedance that is likely to be encountered is 900 Ω the internal impedance of the dialling circuit is set at this level and can be reduced to match lower impedance lines by adding an external resistor between pins 1 and 6.

– internal impedance Z_i = 900 Ω; no external resistor between pins 1 and 6.
– internal impedance Z_i = 600 Ω; external resistor between pins 1 and 6 = 240 Ω.

Output level adjustment

The tone output levels are subject to some spread due to manufacturing tolerances and can be adjusted by selection of the value of the resistor connected to pin 8.
The level of the higher-frequency tone however is always 2 ± 0,7 dB above that of the lower-frequency tone. The total production of the circuits is therefore divided into groups. The group to which any of the integrated circuits belongs is identified by dots on the body of the circuit, the number of dots corresponding with the group number. The combined tone output level is shown as a function of resistor value with group number as a parameter in Fig. 7. After the resistor value has been selected to obtain the required tone output level, the value of the filter capacitor connected to the same pin must be determined. For passive first-order filters (Fig. 4) the time-constant (RC) must be 26 μs. For active second-order filters it must be 46 μs. These values accommodate the different attenuation levels for the various tone frequencies due to the 0,3 dB hump at the breakpoint of the filters.

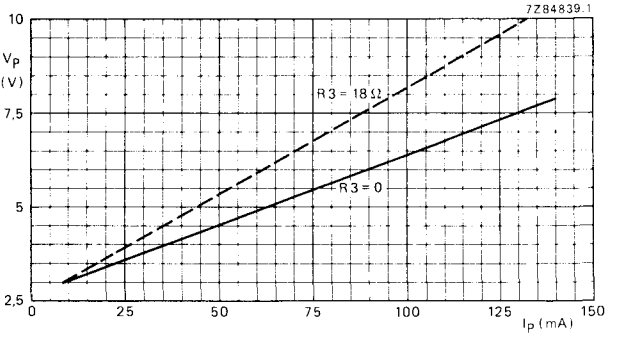


Fig. 10 D.C. characteristics.

DTMF/SPEECH TRANSMISSION INTEGRATED CIRCUIT FOR TELEPHONE APPLICATIONS

This integrated circuit is a dual-tone multi-frequency (DTMF) generator and a speech transmission circuit on a single chip. It supplies frequency combinations in accordance with CCITT recommendations for use in pushbutton telephones. It can be operated with a single contact keyboard or via a direct interface with a microcomputer. I^2L technology allows digital and analogue functions to be implemented on the same chip.

The speech-transmission part incorporates microphone and telephone amplifiers, anti-side tone and line adaption. The microphone inputs, suitable for different types of transducers, are purely symmetrical to allow long cable connections with good immunity against radio-frequency interferences.
The logic inputs contain an interface circuit to guarantee well-defined states and on and off resistance of the keyboard.

The circuit features:
- stabilized DTMF levels to be set externally
- wide operating range of line current and temperature
- no individual DTMF level adjustments required
- microcomputer compatible logic inputs
- gain setting for microphone and receiver amplifiers
- internally generated electronic muting
- low spreads on amplifier gains
- low number of external components

QUICK REFERENCE DATA

Line voltage	V_L	typ.	4,8 V
Line current	I_L	10 to 140	mA
Adjustable dynamic resistance	R_i	600 to 900	Ω
Microphone signal amplification	A_M	typ.	50 dB
Telephone signal amplification	A_T	typ.	20 dB
DTMF tone levels (adjustable)			
lower frequency	V_{LG}	max.	−6 dB
higher frequency	V_{HG}	max.	−4 dB
Operating temperature range	T_{amb}	−25 to + 85	°C

PACKAGE OUTLINES

TEA1046P : 24-lead DIL, plastic (SOT-101).
TEA1046D: 24-lead DIL, ceramic (SOT-149).

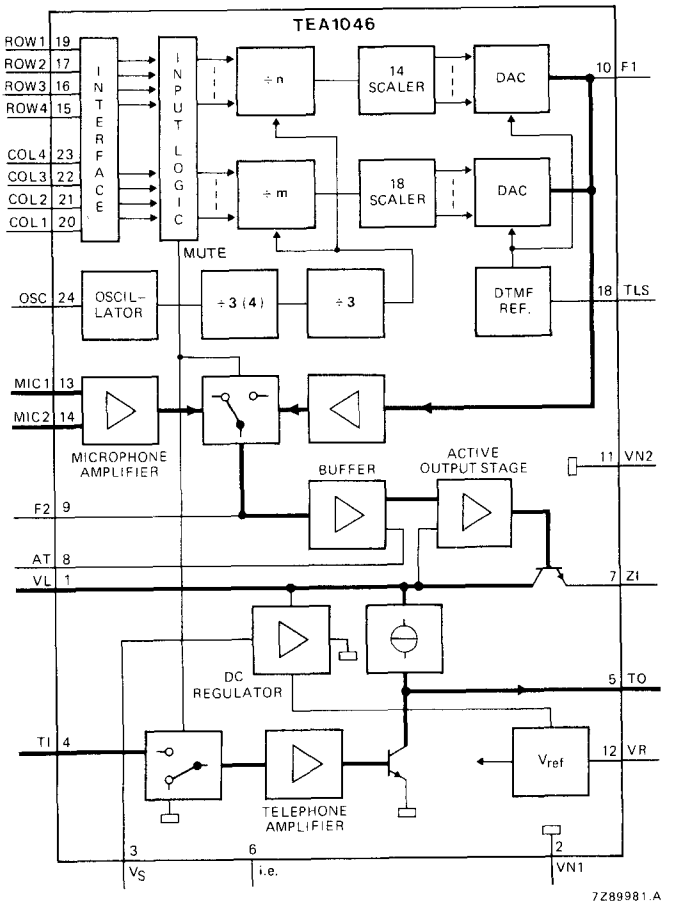


Fig. 1 Functional block diagram.

TELEPHONE TRANSMISSION CIRCUIT

GENERAL DESCRIPTION

The TEA1053 and TEA1054 are bipolar integrated circuits performing all speech and line interface functions in electronic telephone sets.
Their features are:

- Supplied from telephone line current
- Voltage regulator with adjustable d.c. voltage drop and d.c. resistance
- Low-impedance microphone input
- Muting input for pulse or DTMF dialling
- Gain setting facility on all amplifiers
- Line current dependent gain control facility with corrections for the exchange supply voltage
- Supply output for additional circuits

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{line}	typ. 4,2	V
Line current operating range	I_{line}	10 to 140	mA
Telephone line impedance	$\lvert Z_{line}\rvert$	nom. 600	Ω
Supply current	I_{CC}	typ. 1	mA
Voltage gain, transmitting amplifier			
MIC input	A_{vd}	typ. 44,1	dB
DTMF input	A_{vd}	typ. 25,6	dB
Voltage gain, receiving amplifier	A_{vd}	typ. 27	dB
Gain adjustment range			
transmitting amplifier	ΔA_{vd}	typ. ± 6	dB
receiving amplifier	ΔA_{vd}	typ. ± 8	dB
Range of gain control with line current, all amplifiers	ΔA_{vd}	typ. 6	dB
Exchange supply voltage range	V_{exch}	24 to 60	V
Exchange feeding bridge resistance			
TEA1053	R_{exch}	800	Ω
TEA1054	R_{exch}	400	Ω
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINE

TEA1053; TEA1054: 18-lead DIL; plastic (SOT-102A).

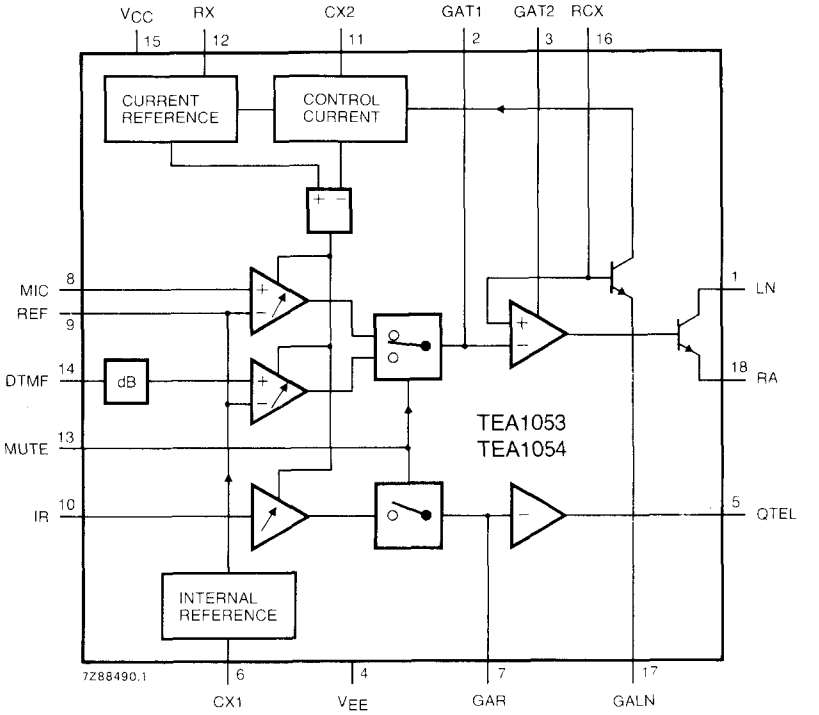


Fig. 1 Block diagram. The blocks marked dB are attenuators. The MUTE input operates analogue switches that activate or inhibit the inputs and outputs as required by the function of the MUTE input.

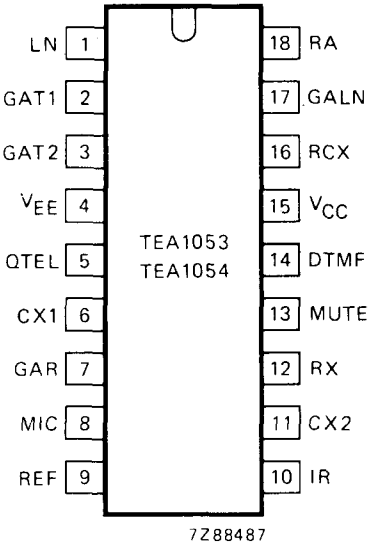


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line connection
2	GAT1	gain adjustment connection, transmitting amplifier
3	GAT2	gain adjustment connection, transmitting amplifier
4	V_{EE}	negative line connection
5	QTEL	telephone output
6	CX1	reference decoupling connection
7	GAR	gain adjustment connection, receiving amplifier
8	MIC	microphone input
9	REF	*reference voltage connection*
10	IR	receiving amplifier input
11	CX2	external stabilizing capacitor connection
12	RX	external resistor connection
13	MUTE	mute input
14	DTMF	dual-tone multi-frequency input
15	V_{CC}	positive supply connection
16	RCX	line voltage adjustment and voltage regulator decoupling connection
17	GALN	gain control with line current connection, all amplifiers
18	RA	d.c. resistance adjustment connection

DEVELOPMENT SAMPLE DATA

FUNCTIONAL DESCRIPTION

The TEA1053 and TEA1054 contain a receiving amplifier, a transmitting amplifier, means to switch the inputs, means to adjust the gain of the amplifiers individually, means to vary the gain with the line current and means to adjust the d.c. voltage drop and d.c. resistance. See the block diagram, Fig. 1.

Supply: LN, V_{CC}, V_{EE}, RA, CX1 and CX2 (pins 1, 15, 4, 18, 6 and 11)

The circuit is supplied from the line current, the arrangement is shown in Fig. 3. The circuit develops its own supply voltage at V_{CC}, the positive supply connection, pin 15. This supply voltage may also be used to supply an external circuit, e.g. a CMOS pulse or DTMF dialler. The current available for this circuit depends on external components, see Fig. 4.

All line current has to flow through the circuit. If the line current exceeds the current required by the circuit itself via V_{CC}, pin 15, i.e. about 1 mA, plus the current required by the peripheral circuits connected to this pin, then the excess current is diverted via LN, the positive line connection, pin 1, to RA, the d.c. resistance adjustment connection, pin 18.

The minimum line voltage may be chosen by external resistor R5 and the variation with line current by external resistor R10. The circuit regulates the line current at 25 °C to:

$$V_{line} = V_{LN} = \frac{R5 + R9}{R9} \times 0{,}62 + I_{LN} \times R10,$$

I_{LN} being the current diverted via LN, the positive line connection.

A regulator decoupling capacitor has to be connected between RCX, pin 16, and V_{EE}, the negative line connection, pin 4, a smoothing capacitor has to be connected between V_{CC}, pin 15, and V_{EE}, and a stabilizing capacitor between CX2, pin 11 and V_{EE}, pin 4. Further a decoupling capacitor has to be connected between CX1, the reference decoupling connection, pin 6, and V_{EE}, pin 4.

The dynamic impedance that the circuit presents to the line in the speech band is determined primarily by resistor R1 connected between LN, pin 1, and V_{CC}, pin 15.

Microphone input MIC (pin 8)

The MIC input has a low input impedance, especially suited for a dynamic or magnetic microphone. This has to be connected between MIC, pin 8, and REF, pin 9. The available gain is typ. 44,1 dB.

Dual-tone multi-frequency input DTMF and mute input MUTE (pins 14 and 13)

A HIGH level on the MUTE input inhibits the microphone input MIC and the telephone outputs QTEL and enables the DTMF input, a LOW level does the reverse. Switching the MUTE input will not produce any clicks on the line or in the telephone. The available gain from the DTMF input is typ. 25,6 dB.

Receiving amplifier input IR and telephone output QTEL (pins 10 and 5)

The available gain from input IR to output QTEL is typ. 27 dB. The output QTEL is intended for telephone capsules with an impedance of 150 Ω or more.

Gain adjustment connections GAT1, GAT2, and GAR (pins 2, 3 and 7)

The gain of the transmitting amplifier may be adjusted by an external resistor R2 connected between GAT1 and GAT2, pins 2 and 3 (see Fig. 9). This adjustment influences the sensitivity of the inputs MIC and DTMF to the same amount. The gain is proportional to R2 and inversely proportional to R10 and R12.

The gain of the receiving amplifier may be adjusted by an external resistor R14 between GAR, pin 7, and CX1, pin 6. The gain is proportional to R14 and inversely proportional to R12.

Gain control with line current, GALN connection (pin 17)

The circuit offers a facility to automatically vary the gain of all its amplifiers with the line current. In this way the circuit compensates for differences in line attenuation. The variation is accomplished by connecting an external resistor R11 between GALN, pin 17, and V_{EE}, pin 4. The value of this resistor should be chosen in accordance with the supply voltage of the exchange (see Figs 5 and 6).

If no gain variation with line current is required the GALN connection may be left open. All amplifiers have their maximum gain then.

Side tone suppression

In the circuit diagram shown in Fig. 9 side tone suppression is obtained with components C2, R3, R4, R7 and R8. Their component values have to be chosen to suit the cable type used. This network attenuates the signal from the telephone line to the IR input of the receiving amplifier. This attenuation may be adjusted by choosing the value of R7 without affecting the side tone suppression.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

Supply current				
d.c.	I_{line}	max.	140	mA
surge, $t < 100$ h	I_{line}	max.	250	mA
Storage temperature range	T_{stg}	−40 to	+125	°C
Operating temperature range	T_{amb}	−25 to	+70	°C
Junction temperature	T_j	max.	150	°C

CHARACTERISTICS

I_{line} = 10 to 140 mA; f = 1 kHz; T_{amb} = 25 °C unless otherwise specified.

	symbol	min.	typ.	max.	unit
Supply, LN and V_{CC} (pins 1 and 15)					
Line voltage					
I_{line} = 15 mA	V_{line}	4	4,2	4,4	V
I_{line} = 50 mA	V_{line}	–	–	5,8	V
I_{line} = 100 mA	V_{line}	–	–	7,3	V
Variation with temperature	$-\Delta V_{line}/\Delta T$	8	10	12	mV/K
Line current operating range	I_{line}	10	–	140	mA
Supply current at V_{CC} = 2 V	I_{CC}	–	–	1	mA
Microphone input MIC and reference voltage connection REF (pins 8 and 9)					
Input impedance	$\lvert Z_{8\text{-}9}\rvert$	–	3	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	43,1	44,1	45,1	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = –5 to +45 °C	ΔA_{vd}	–	± 0,5	–	dB
DTMF input (pin 14)					
Input impedance	$\lvert Z_{14\text{-}4}\rvert$	10	15	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	24,6	25,6	26,6	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = –5 to +45 °C	ΔA_{vd}	–	± 0,5	–	dB
Gain adjustment connections, transmitting amplifier, GAT1 and GAT2 (pins 2 and 3)					
Gain adjustment range	ΔA_{vd}	–	± 6	–	dB
Transmitting amplifier output LN (pin 1)					
Output voltage at I_{line} = 15 mA; R_{line} = 600 Ω d = 2%	$v_{LN(rms)}$	1,4	–	–	V
Psophometrically weighted * noise output voltage at I_{line} = 15 mA; R_{line} = 600 Ω	$v_{LN(rms)}$	–	245	–	μV

	symbol	min.	typ.	max.	unit
MUTE input (pin 13)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{13}$	–	8	20	μA
Attenuation of non-selected signals	$-\Delta A_{vd}$	45	–	–	dB
Receiving amplifier input IR (pin 10)					
Input impedance	$\lvert Z_{10\text{-}4}\rvert$	–	10	–	kΩ
Telephone output QTEL (pin 5)					
Voltage gain at I_{line} = 15 mA; R_{load} = 150 Ω; R14 = 7,5 kΩ; see Fig. 8	A_{vd}	26	27	28	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to +45 °C	ΔA_{vd}	–	± 0,5	–	dB
Maximum output voltage at I_{line} = 15 mA; R_{load} = 150 Ω; d = 2%	$V_{O(rms)}$	350	–	–	mV
Psophometrically weighted * noise output voltage at I_{line} = 15 mA	$V_{O(rms)}$	–	40	–	μV
Gain adjustment connection, receiving amplifier, GAR (pin 7)					
Gain adjustment range	ΔA_{vd}	–	± 8	–	dB
Gain control with line current connection GALN (pin 17)					
Gain control range	ΔA_{vd}	–	[illegible]		dB
Highest line current for maximum gain, R11 = 105 kΩ; TEA1053	I_{line}	22,5	25	[illegible]	mA
TEA1054	I_{line}	31,5	35,5	38,5	mA
Lowest line current for minimum gain, R11 = 105 kΩ; TEA1053	I_{line}	49,5	55	60,5	mA
TEA1054	I_{line}	81	90	99	mA

DEVELOPMENT SAMPLE DATA

* P53 curve.

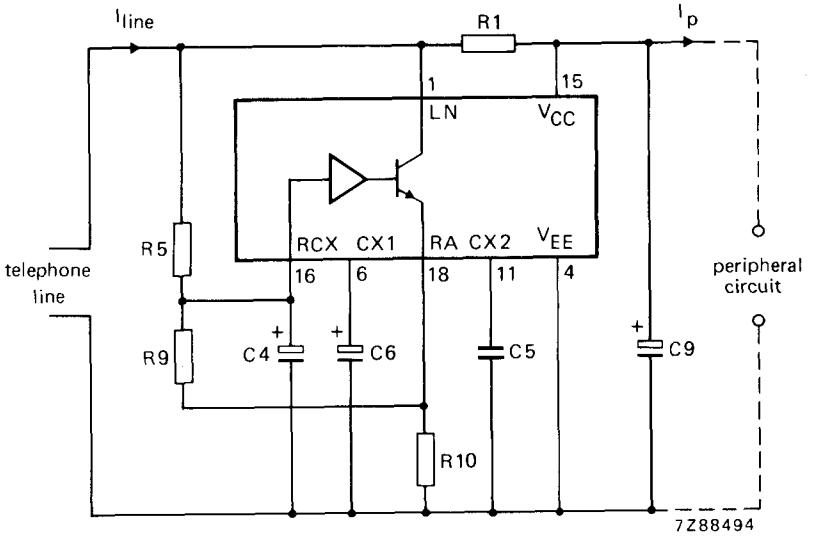


Fig. 3 Supply arrangement.

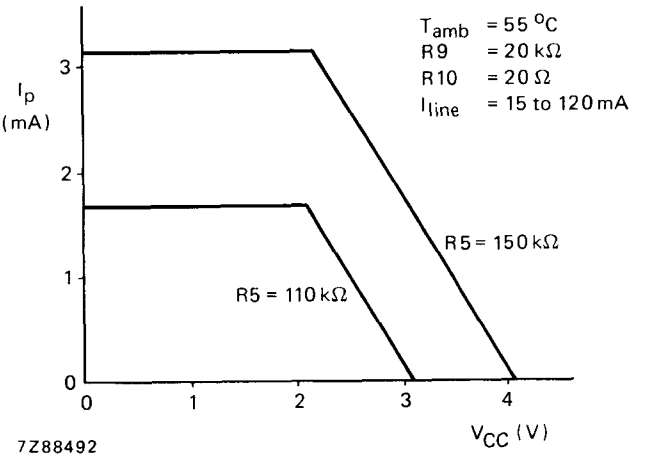


Fig. 4 Maximum current I_p available from V_{CC} for external (peripheral) circuits.

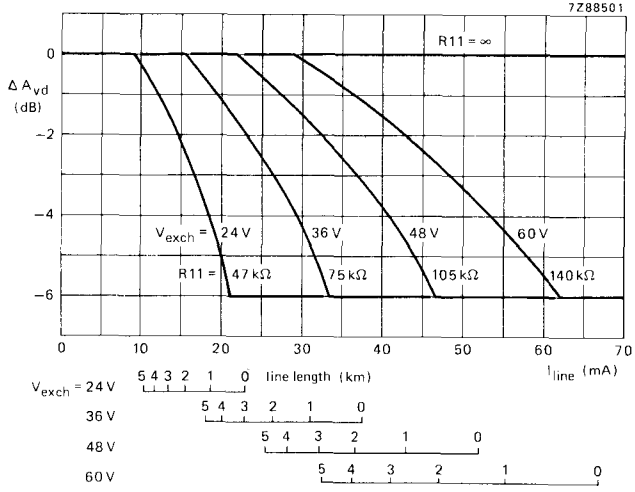


Fig. 5 Gain variation with line current for the TEA1053, with R11 as a parameter. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

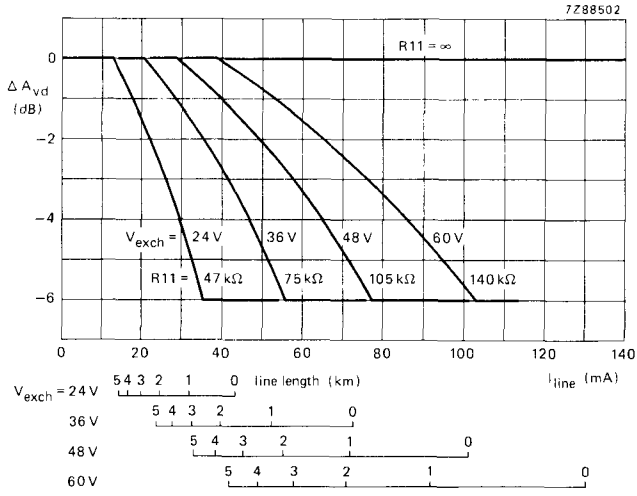


Fig. 6 Gain variation with line current for the TEA1054, with R11 as a parameter. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

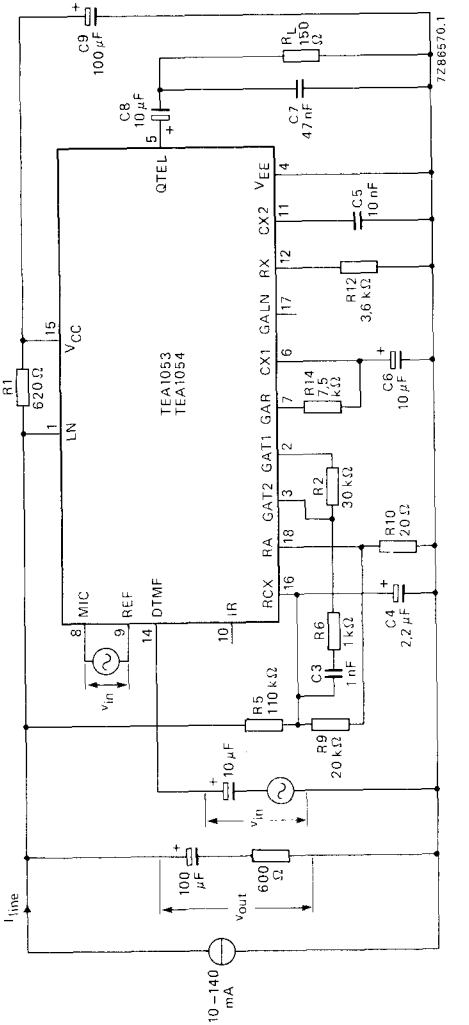


Fig. 7 Test circuit for defining voltage gain of MIC and DTMF inputs. Gain is defined as: $A_{vd} = 20 \log |v_{out}/v_{in}|$. For measuring the MIC input the MUTE input should be LOW and for measuring the DTMF input MUTE should be HIGH. The input not under test should be open.

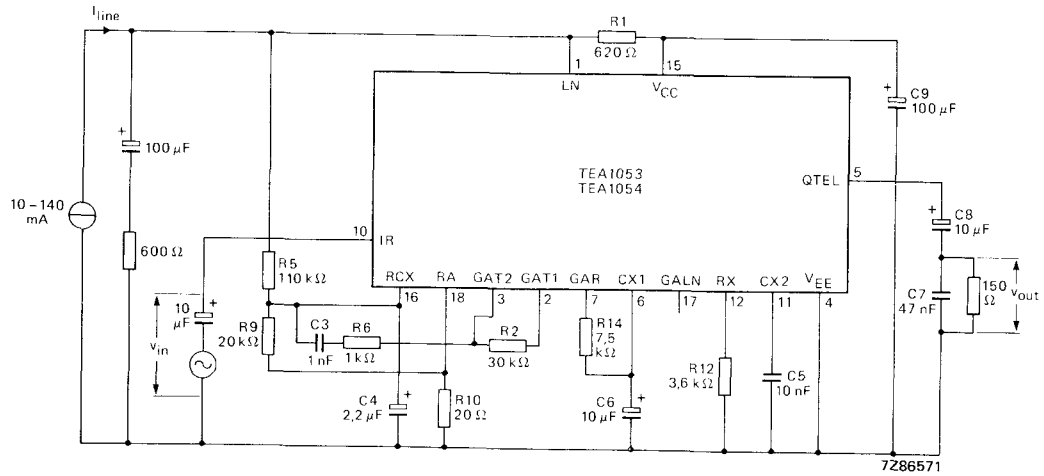


Fig. 8 Test circuit for defining voltage gain of the receiving amplifier. Gain is defined as: $A_{vd} = 20 \log |v_{out}/v_{in}|$. The MUTE input should be LOW.

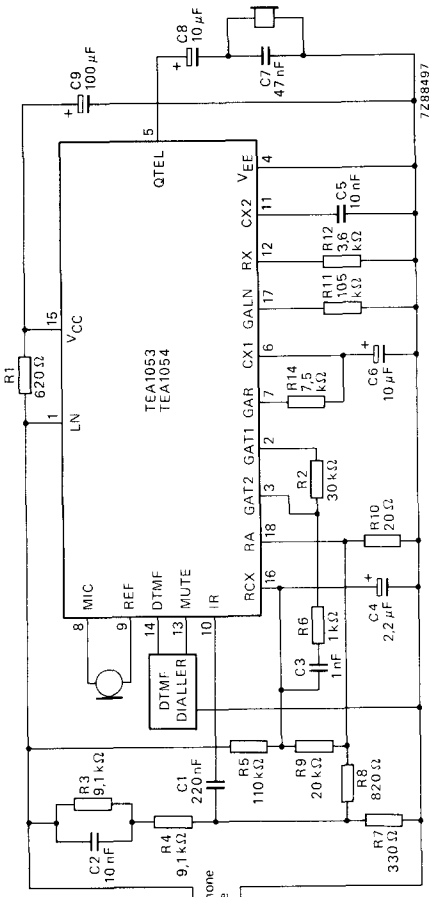


Fig. 9 Typical application of the TEA1053 or TEA1054 in an electronic telephone set.

APPLICATION INFORMATION SUPPLIED ON REQUEST.

TELEPHONE TRANSMISSION CIRCUIT

GENERAL DESCRIPTION

The TEA1055 is a bipolar integrated circuit performing the speech and line interface functions in electronic telephone sets.

Its features are:

- Supplied from telephone line current
- Voltage regulator with adjustable d.c. voltage drop and d.c. resistance
- High-impedance microphone input
- Muting input for pulse or DTMF dialling
- Gain setting facility on all amplifiers
- Line current dependent gain control facility with corrections for the exchange supply voltage and its feeding bridge resistance
- Supply output for additional circuits

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{line}	typ.	4,2 V
Line current operating range	I_{line}		10 to 140 mA
Telephone line impedance	$\|Z_{line}\|$	nom.	600 Ω
Supply current	I_{CC}	typ.	1 mA
Voltage gain, transmitting amplifier			
MIC input	A_{vd}	typ.	20 dB
DTMF input	A_{vd}	typ.	25,6 dB
Voltage gain, receiving amplifier	A_{vd}	typ.	27 dB
Gain adjustment range			
transmitting amplifier	ΔA_{vd}	typ.	± 6 dB
receiving amplifier	ΔA_{vd}	typ.	± 8 dB
Range of gain control with line current, all amplifiers	ΔA_{vd}	typ.	6 dB
Exchange supply voltage range	V_{exch}		24 to 60 V
Exchange feeding bridge resistance	R_{exch}		400 or 800 Ω
Operating ambient temperature range	T_{amb}		−25 to + 70 °C

PACKAGE OUTLINE

TEA1055: 18-lead DIL; plastic (SOT-102A).

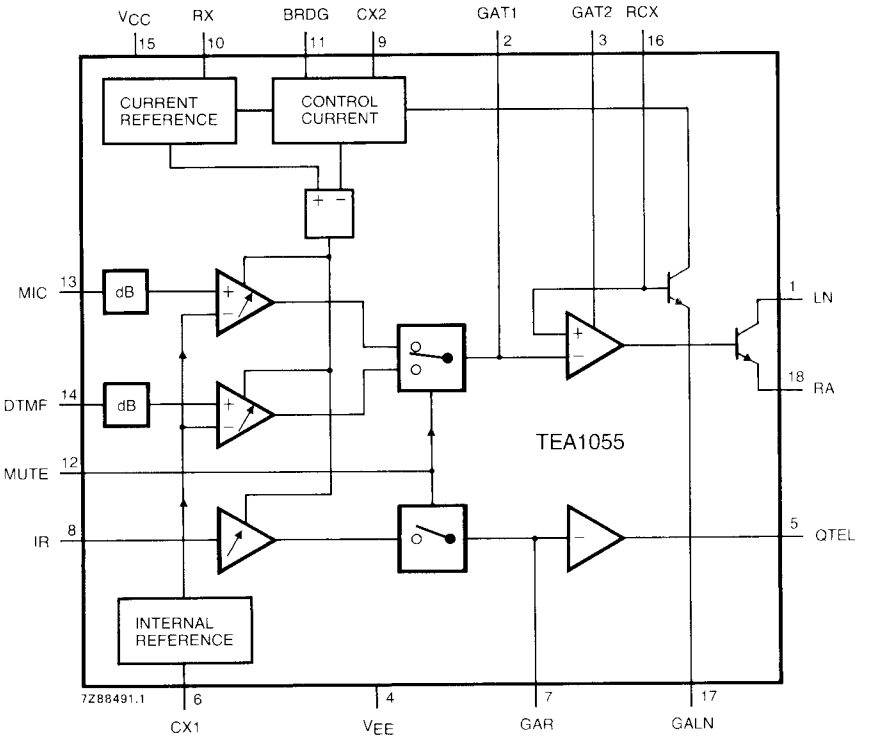


Fig. 1 Block diagram. The blocks marked dB are attenuators. The MUTE input operates analogue switches that activate or inhibit the inputs and outputs as required by the function of the MUTE input.

DEVELOPMENT SAMPLE DATA

PINNING

1	LN	positive line connection
2	GAT1	gain adjustment connection, transmitting amplifier
3	GAT2	gain adjustment connection, transmitting amplifier
4	V_{EE}	negative line connection
5	QTEL	telephone output
6	CX1	reference decoupling connection
7	GAR	gain adjustment connection, receiving amplifier
8	IR	receiving amplifier input
9	CX2	external stabilizing capacitor connection
10	RX	external resistor connection
11	BRDG	selection input for gain control adaption to feeding bridge impedance
12	MUTE	mute input
13	MIC	microphone input
14	DTMF	dual-tone multi-frequency input
15	V_{CC}	positive supply connection
16	RCX	line voltage adjustment and decoupling connection
17	GALN	gain control with line current connection, all amplifiers
18	RA	d.c. resistance adjustment connection

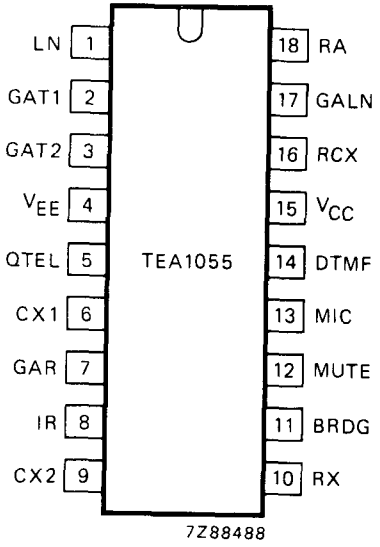


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The TEA1055 contains a receiving amplifier, a transmitting amplifier, means to switch the inputs, means to adjust the gain of the amplifiers individually, means to vary the gain with the line current and means to adjust the d.c. voltage drop and d.c. resistance. See the block diagram, Fig. 1.

Supply: LN, V_{CC}, V_{EE}, RA, CX1 and CX2 (pins 1, 15, 4, 18, 6 and 9)

The circuit is supplied from the line current, the arrangement is shown in Fig. 3. The circuit develops its own supply voltage at V_{CC}, the positive supply connection, pin 15. This supply voltage may also be used to supply an external circuit, e.g. an electret microphone amplifier stage or a CMOS pulse or DTMF dialler. The current available for this circuit depends on external components, see Fig. 4.

All line current has to flow through the circuit. If the line current exceeds the current required by the circuit itself via V_{CC}, pin 15, i.e. about 1 mA, plus the current required by the peripheral circuits connected to this pin, then the excess current is diverted via LN, the positive line connection, pin 1, to RA, the d.c. resistance adjustment connection, pin 18.

The minimum line voltage may be chosen by external resistor R5 and the variation with line current by external resistor R10. The circuit regulates the line voltage at $T_{amb} = 25\ ^{o}C$ to:

$$V_{line} = V_{LN} = \frac{R5 + R9}{R9} \cdot 0{,}62 + I_{LN} \cdot R10,$$

I_{LN} being the current diverted via LN, the positive line connection.

A regulator decoupling capacitor has to be connected between RCX, pin 16, and V_{EE}, the negative line connection, pin 4, a smoothing capacitor has to be connected between V_{CC}, pin 15, and V_{EE}, and a stabilizing capacitor between CX2, pin 9 and V_{EE}, pin 4. Further a decoupling capacitor has to be connected between CX1, the reference decoupling connection, pin 6, and V_{EE}, pin 4.

The dynamic impedance that the circuit presents to the line in the speech band is determined primarily by resistor R1 connected between LN, pin 1, and V_{CC}, pin 15.

Microphone input MIC (pin 13)

The circuit has a high-impedance microphone input, especially suited for a sensitive microphone, e.g. an electret microphone with preamplifier. The available gain is typ. 20 dB.

Dual-tone multi-frequency input DTMF and mute input MUTE (pins 14 and 12)

A HIGH level on the MUTE input inhibits the microphone input and the telephone output QTEL and enables the DTMF input, a LOW level does the reverse. Switching the MUTE input will not produce any clicks on the line or in the telephone. The available gain from the DTMF input is typ. 25,6 dB.

Receiving amplifier input IR and telephone output QTEL (pins 8 and 5)

The output QTEL is intended for telephone capsules with an impedance of 150 Ω or more. The available gain is typ. 27 dB.

Gain adjustment connections GAT1, GAT2 and GAR (pins 2, 3 and 7)

The gain of the transmitting amplifier may be adjusted by an external resistor R2 connected between GAT1 and GAT2, pins 2 and 3 (see Fig. 9). This adjustment influences the sensitivity of the inputs MIC and DTMF to the same amount. The gain is proportional to R2 and inversely proportional to R10 and R12.

The gain of the receiving amplifier may be adjusted by an external resistor R14 between GAR, pin 7, and CX1, pin 6. The gain is proportional to R14 and inversely proportional to R12.

Gain control with line current, GALN connection (pin 17)

The circuit offers a facility to automatically vary the gain of all its amplifiers with the line current. In this way the circuit compensates for differences in line attenuation. The variation is accomplished by connecting an external resistor R11 between GALN, pin 17, and V_{EE}, pin 4. The value of this resistor should be chosen in accordance with the supply voltage of the exchange and its feeding bridge resistance (see Figs 5 and 6).

If no gain variation with line current is required the GALN connection may be left open. All amplifiers have their maximum gain then.

Selection input for gain control adaption to feeding bridge impedance, BRDG (pin 11)

A LOW level at the BRDG input optimized the gain control characteristics of the circuit for a 400 Ω feeding bridge in the exchange, a HIGH level for 800 Ω.

Side tone suppression

In the circuit diagram shown in Fig. 9 side tone suppression is obtained with components C2, R3, R4, R7 and R8. Their component values have to be chosen to suit the cable type used. This network attenuates the signal from the telephone line to the IR input of the receiving amplifier. This attenuation may be adjusted by choosing the value of R7 without affecting the side tone suppression.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current			
d.c.	I_{line}	max.	140 mA
surge, $t < 100$ h	I_{line}	max.	250 mA
Storage temperature range	T_{stg}	−40 to + 125	°C
Operating temperature range	T_{amb}	−25 to + 70	°C
Junction temperature	T_j	max.	150 °C

CHARACTERISTICS

I_{line} = 10 to 140 mA; f = 1 kHz; T_{amb} = 25 °C unless otherwise specified.

	symbol	min.	typ.	max.	unit
Supply, LN and V_{CC} (pins 1 and 15)					
Line voltage					
I_{line} = 15 mA	V_{line}	4	4,2	4,4	V
I_{line} = 50 mA	V_{line}	–	–	5,8	V
I_{line} = 100 mA	V_{line}	–	–	7,3	V
Variation with temperature	$-\Delta V_{line}/\Delta T$	8	10	12	mV/K
Line current operating range	I_{line}	10	–	140	mA
Supply current at V_{CC} = 2 V	I_{CC}	–	–	1	mA
Microphone input MIC (pin 13)					
Input impedance	$\lvert Z_{13\text{-}4}\rvert$	40	48	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	19	20	21	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to + 45 °C	ΔA_{vd}	–	± 0,5	–	dB
DTMF input (pin 14)					
Input impedance	$\lvert Z_{14\text{-}4}\rvert$	10	15	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	24,6	25,6	26,6	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to + 45 °C	ΔA_{vd}	–	± 0,5	–	dB
Gain adjustment connections, transmitting amplifier, GAT1 and GAT2 (pins 2 and 3)					
Gain adjustment range	ΔA_{vd}	–	± 6	–	dB
Transmitting amplifier output LN (pin 1)					
Output voltage at I_{line} = 15 mA; R_{line} = 600 Ω d = 2%	$V_{LN(rms)}$	1,4	–	–	V
Psophometrically weighted* noise output voltage at I_{line} = 15 mA; R_{line} = 600 Ω	$V_{LN(rms)}$	–	245	–	μV
MUTE input (pin 12)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{12}$	–	8	20	μA
Attenuation of non-selected signals	$-\Delta A_{vd}$	45	–	–	dB

	symbol	min.	typ.	max.	unit
Receiving amplifier input IR (pin 8)					
Input impedance	$\lvert Z_{8\text{-}4}\rvert$	–	10	–	kΩ
Telephone output QTEL (pin 5)					
Voltage gain at I_{line} = 15 mA; R_{load} = 150 Ω; R14 = 7,5 kΩ; see Fig. 8	A_{vd}	26	27	28	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to + 45 °C	ΔA_{vd}	–	± 0,5	–	dB
Maximum output voltage at I_{line} = 15 mA; R1 = 150 Ω; d = 2%	$V_{O(rms)}$	350	–	–	mV
Psophometrically weighted* noise output voltage at I_{line} = 15 mA	$V_{O(rms)}$	–	40	–	μV
Gain adjustment connection, receiving amplifier, GAR (pin 7)					
Gain adjustment range	ΔA_{vd}	–	± 8	–	dB
Selection input for gain control adaption to feeding bridge impedance, BRDG (pin 11)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{11}$	–	8	20	μA
Gain control with line current connection GALN (pin 17)					
Gain control range	ΔA_{vd}	–	6	–	dB
Highest line current for maximum gain, R11 = 105 kΩ; BRDG = HIGH (R_{exch} = 800 Ω)	I_{line}	22,5	25	27,5	mA
BRDG = LOW (R_{exch} = 400 Ω)	I_{line}	31,5	35	38,5	mA
Lowest line current for minimum gain, R11 = 105 kΩ; BRDG = HIGH (R_{exch} = 800 Ω)	I_{line}	49,5	55	60,5	mA
BRDG = LOW (R_{exch} = 400 Ω)	I_{line}	81	90	99	mA

DEVELOPMENT SAMPLE DATA

* P53 curve.

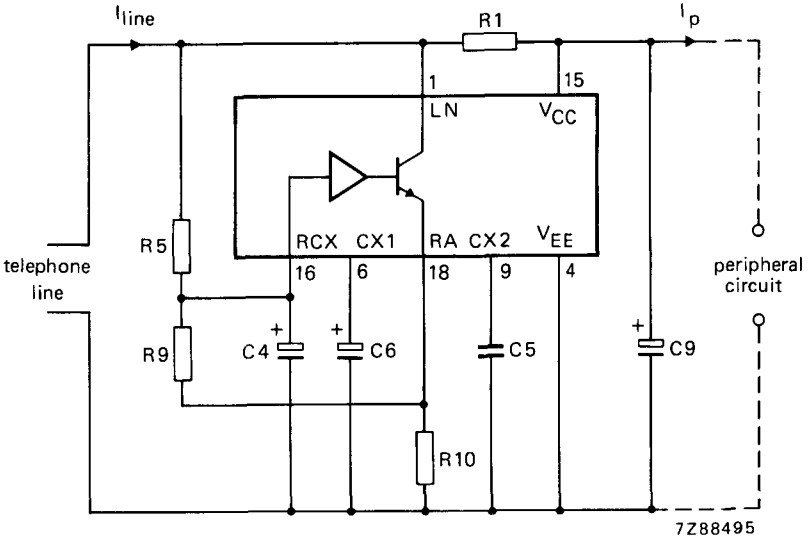


Fig. 3 Supply arrangement.

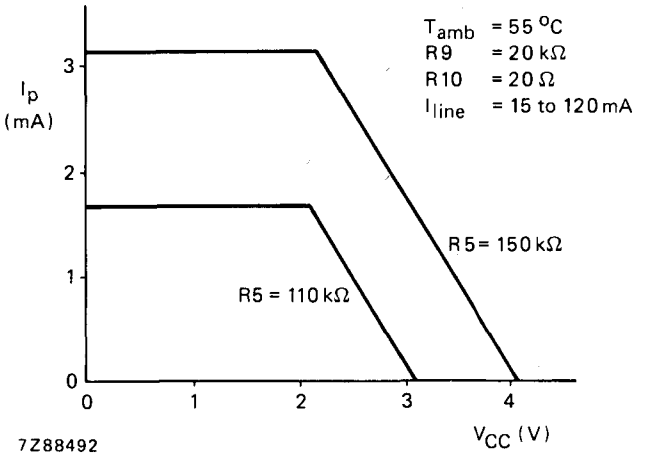


Fig. 4 Maximum current I_p available from V_{CC} for an external circuit.

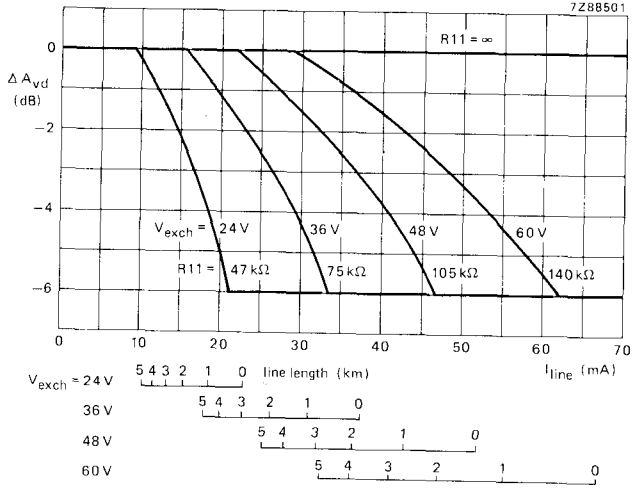


Fig. 5 Gain variation with line current, with R11 as a parameter, and with the BRDG input HIGH, i.e. the circuit optimized for 800 Ω. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

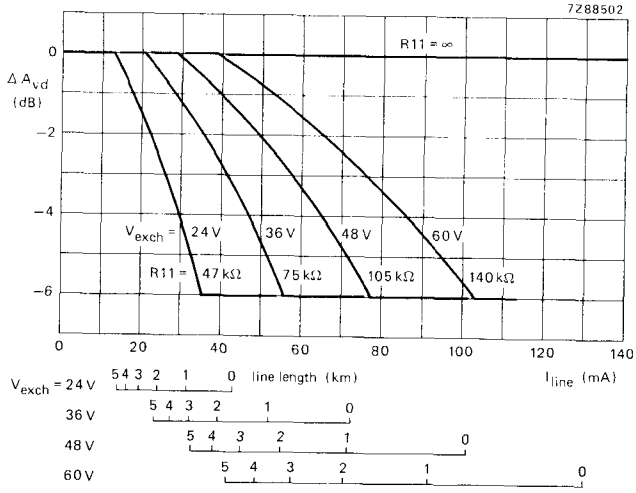


Fig. 6 Gain variation with line current, with R11 as a parameter, and with the BRDG input LOW, i.e. the circuit optimized for 400 Ω. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

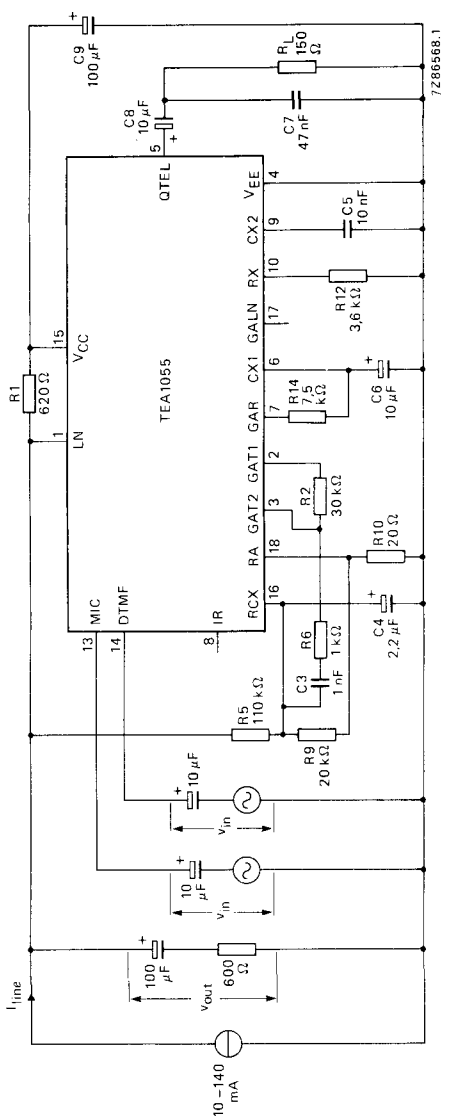


Fig. 7 Test circuit for defining voltage gain of MIC and DTMF inputs. Gain is defined as: $A_{vd} = 20 \log |v_{out}/v_{in}|$. For measuring the MIC input the MUTE input should be LOW and for measuring the DTMF input MUTE should be HIGH. The input not under test should be open.

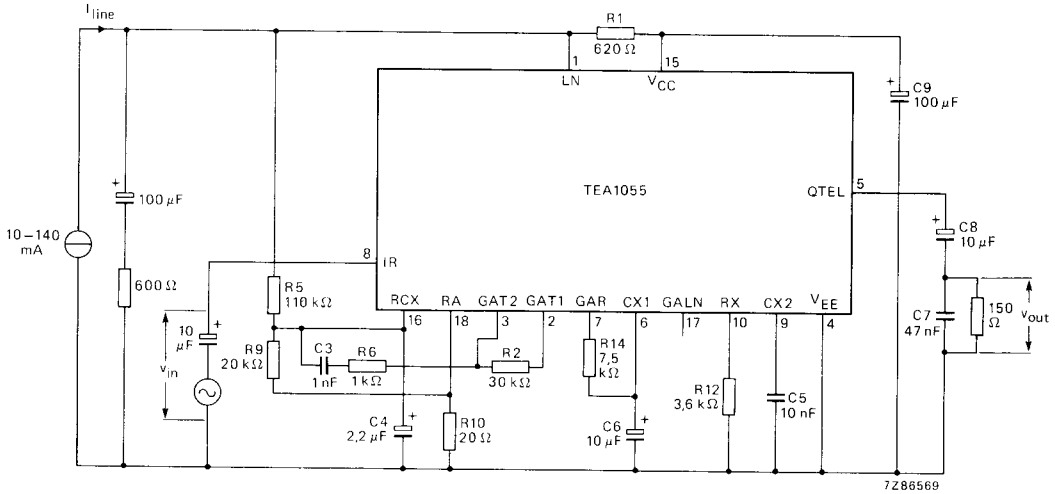


Fig. 8 Test circuit for defining voltage gain of the receiving amplifier. Gain is defined as: $A_{vd} = 20 \log | v_{out}/v_{in} |$. The MUTE input should be LOW.

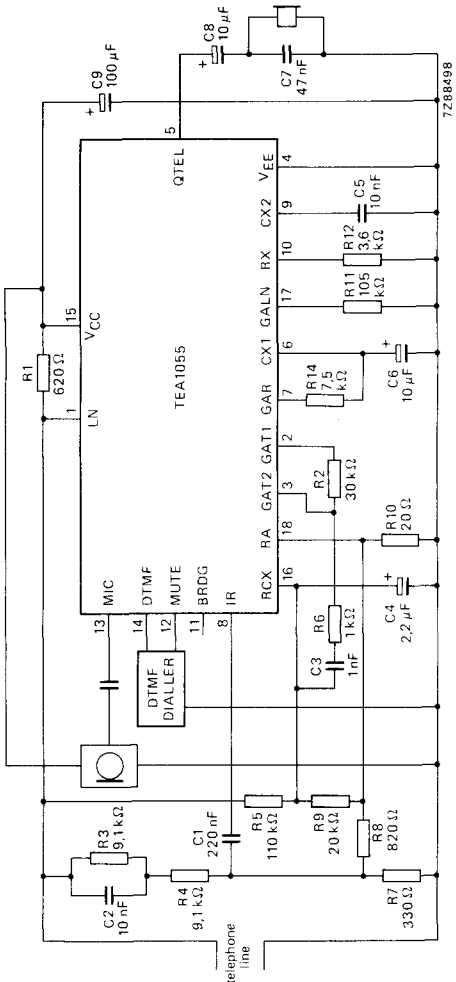


Fig. 9 Typical application of the TEA1055 in an electronic telephone set. The connection to the BRDG input is not shown, see the Functional Description.

APPLICATION INFORMATION SUPPLIED ON REQUEST

VERSATILE TELEPHONE TRANSMISSION CIRCUITS WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1060 and TEA1061 are bipolar integrated circuits performing all speech and line interface functions required in fully electronic telephone sets. The circuits internally perform electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones (TEA1060)
- Symmetrical high-impedance inputs for piezoelectric microphone (TEA1061)
- Asymmetrical high-impedance input for electret microphone (TEA1061)
- DTMF signal input
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on all amplifiers
- Line loss compensation facility, line current dependent
- Gain control adaptable to exchange supply

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{LN}	typ.	4,5 V
Line current operating range	I_{line}	10 to	140 mA
Supply current			
power down input LOW	I_{CC}	typ.	1 mA
power down input HIGH	I_{CC}	typ.	50 μA
Voltage amplification range microphone amplifier			
TEA1060	A_{vd}	44 to	60 dB
TEA1061	A_{vd}	30 to	46 dB
receiving amplifier	A_{vd}	17 to	39 dB
Amplification control range	ΔA_{vd}	typ.	6 dB
Exchange supply voltage range	V_{exch}	24 to	60 V
Exchange feeding bridge resistance range	R_{exch}	400 to	1000 Ω
Operating ambient temperature range	T_{amb}	−25 to	+75 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102A).

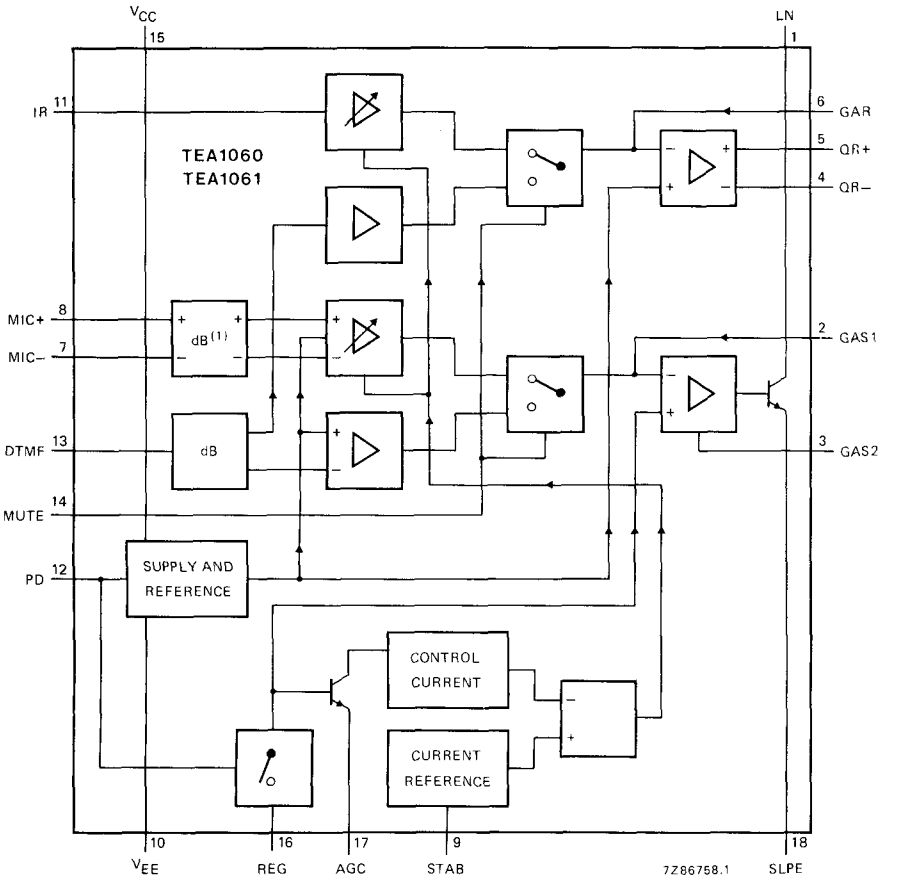


Fig. 1 Block diagram. The blocks marked "dB" are attenuators. The block marked (1) is only present in the TEA1061.

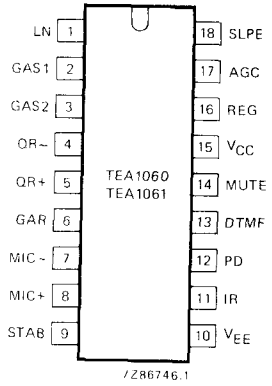


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	OR−	inverting output; receiving amplifier
5	OR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC−	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (d.c. resistance) adjustment

DEVELOPMENT SAMPLE DATA

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits usually are supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3,6 kΩ between STAB and V_{EE}.

The d.c. current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the d.c. resistance of the subscriber line R_{line} and the d.c. voltage on the subscriber set (see Fig. 3).

If the line current I_{line} exceeds the current I_{CC} required by the circuit itself, i.e. about 1 mA, plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:

$$V_{LN} = V_{ref} + I_{LN} \times R9 = V_{ref} + (I_{line} - I_{CC} - I_p) \times R9,$$

V_{ref} being an internally generated temperature compensated reference voltage of 4,2 V and R9 being an external resistor connected between SLPE and V_{EE}. Under normal conditions $I_{LN} >> I_{CC} + I_p$. The static behaviour of the circuit then equals a 4,2 V voltage regulator diode with an internal resistance R9. In the audio-frequency range the dynamic impedance equals R1.

FUNCTIONAL DESCRIPTION (continued)

The current I_p available from V_{CC} for supplying peripheral circuits depends on external components. Figure 4 shows this current for V_{CC} = 3 V min., this being the minimum supply voltage for most CMOS circuits including a diode voltage drop for an enable diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.

Microphone inputs MIC+ and MIC− and gain adjustment pins GAS1 and GAS2

The TEA1060 and TEA1061 have differential microphone inputs.

The TEA1060 is intended for low-sensitivity, low-impedance dynamic or magnetic microphones. Its input impedance is 2 x 4 kΩ and its voltage amplification is typ. 52 dB.

The TEA1061 is intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 2 x 20 kΩ and its voltage amplification is typ. 38 dB.

The arrangements with the microphone types mentioned are shown in Fig. 5.

The amplification of the microphone amplifier in both types can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier, a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage amplification from DTMF to LN is typ. 32 dB and varies with R7 in the same way as the amplification of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig. 6). Amplification from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the amplification is increased by 6 dB. This makes differential drive possible, which is required for high-impedance dynamic, magnetic and piezoelectric earpieces with load impedances exceeding 450 Ω.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and r.m.s. value is higher.

The amplification of the receiving amplifier can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R4 connected from GAR to QR+.

An external capacitor C4 of 100 pF between QR+ and GAR is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 form AGC to V_{EE}. This automatic gain control varies the amplification of the microphone amplifier and the receiving amplifier in accordance with the d.c. line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0,5 mm diameter copper twisted-pair cable with a d.c. resistance of 176 Ω/km and an average attention of 1,2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 7 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum amplification as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input, which reduces the supply current from typ. 1 mA to typ. 50 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the circuit's impedance equals a 4,2 V voltage regulator diode with an internal resistance equal to R9. This results in rectangular current waveforms in pulse dialling and register recall.

When this facility is not required PD may be left open.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of R2, R3, R8 and Z_{bal} (see Fig. 10). Maximum compensation is obtained when Z_{bal} equals the line impedance Z_{line} as seen by the set.

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal} approaches the *average line impedance.*

The anti-side-tone network attenuates the signal from the line. With R8 = 620 Ω and R9 = 20 Ω the *attenuation is* 29,1 dB. *The attenuation is* flat over the audio-frequency range.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive line voltage	V_{LN}	max.	15	V
Line current				
average	$I_{line(AV)}$	max.	140	mA
non-repetitive (t_{max} = 100 hours)	$I_{line(S)}$	max.	250	mA
non-repetitive peak (t_{max} = 1 ms)	$I_{line(SM)}$	max.	1	A
Voltage on all other pins	V	max.	V_{CC} + 0,7	V
	−V	max.	0,7	V
Total power dissipation	P_{tot}	max.	640	mW
Storage temperature range	T_{stg}	−40 to	+125	°C
Operating ambient temperature range	T_{amb}	−25 to	+75	°C

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 15)					
Voltage drop over circuit					
at I_{line} = 5 mA	V_{LN}	–	4,3	–	V
at I_{line} = 15 mA	V_{LN}	4,3	4,5	4,7	V
at I_{line} = 100 mA	V_{LN}	–	6,2	7	V
Variation with temperature	$\Delta V_{LN}/\Delta T$	−2	0	+2	mV/K
Supply current					
PD = LOW; V_{CC} = 2,8 V	I_{CC}	–	0,96	1,25	mA
PD = HIGH	I_{CC}	–	50	–	μA
Microphone inputs MIC+ and MIC−					
Input impedance					
TEA1060	$\lvert z_{is}\rvert$	–	4	–	kΩ
TEA1061	$\lvert z_{is}\rvert$	–	20	–	kΩ
Standard deviation on input impedance	σ	–	12	–	%
Common-mode rejection ratio; TEA1060	k_{CMR}	–	t.b.f.	–	dB
Voltage amplification at I_{line} = 15 mA; R7 = 68 kΩ					
TEA1060	A_{vd}	51	52	53	dB
TEA1061	A_{vd}	37	38	39	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	±0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to +75 °C	$\Delta A_{vd}/\Delta T$	–	±0,5	–	dB

parameter	symbol	min.	typ.	max.	unit
Dual-tone multi-frequency input DTMF					
Input impedance	$\|z_{is}\|$	–	20	–	kΩ
Standard deviation on input impedance	σ	–	12	–	%
Voltage amplification at I_{line} = 15 mA; R7 = 68 kΩ	A_{vd}	31	32	33	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	±0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to +75 °C	$\Delta A_{vd}/\Delta T$	–	±0,5	–	dB
Gain adjustment pins GAS1 and GAS2					
Amplification variation with R7, transmitting amplifier	ΔA_{vd}	−8	–	+8	dB
Transmitting amplifier output LN					
Output voltage at I_{line} = 15 mA; d_{tot} = 2%	$V_{LN(rms)}$	1,4	2,4	–	V
d_{tot} = 10%	$V_{LN(rms)}$	–	2,7	–	V
Noise output voltage at I_{line} = 15 mA; R7 = 68 kΩ; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	−70	–	dBmp
Receiving amplifier input IR					
Input impedance	$\|z_{is}\|$	–	20	–	kΩ
Receiving amplifier outputs QR + and QR−					
Output impedance; single-ended	$\|z_{os}\|$	–	15	–	Ω
Voltage amplification at I_{line} = 15 mA; R4 = 100 kΩ; single-ended; R_L = 300 Ω	A_{vd}	24	25	26	dB
differential; R_L = 600 Ω	A_{vd}	30	31	32	dB
Variation with frequency, at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	±0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to +75 °C	$\Delta A_{vd}/\Delta T$	–	±0,5	–	dB
Output voltage at I_p = 0; d_{tot} = 2%; sine-wave drive single-ended; R_L = 150 Ω	$V_{o(rms)}$	0,35	0,4	–	V
single-ended; R_L = 450 Ω	$V_{o(rms)}$	0,5	0,6	–	V
differential; C_L = 47 nF; f = 3400 Hz	$V_{o(rms)}$	0,9	1,1	–	V
Noise output voltage at I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve) single-ended; R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential; R_L = 600 Ω	$V_{no(rms)}$	–	100	–	μV

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Gain adjustment pin GAR					
Amplification variation with R4, receiving amplifier	ΔA_{vd}	−8	–	+8	dB
MUTE input					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{MUTE}	–	8	15	μA
Reduction of voltage amplification from MIC+ and MIC− to LN at MUTE = HIGH	$-\Delta A_{vd}$	–	70	–	dB
Voltage amplification from DTMF to QR + or QR− at MUTE = HIGH; single-ended load; R_L = 300 Ω	A_{vd}	–	−12	–	dB
Power-down input PD					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{PD}	–	5	10	μA
Automatic gain control input AGC					
Amplification control range	$-\Delta A_{vd}$	–	6	–	dB
Highest line current for maximum amplification at R6 = 100 kΩ	I_{line}	–	23	–	mA
Lowest line current for minimum amplification at R6 = 100 kΩ	I_{line}	–	58	–	mA

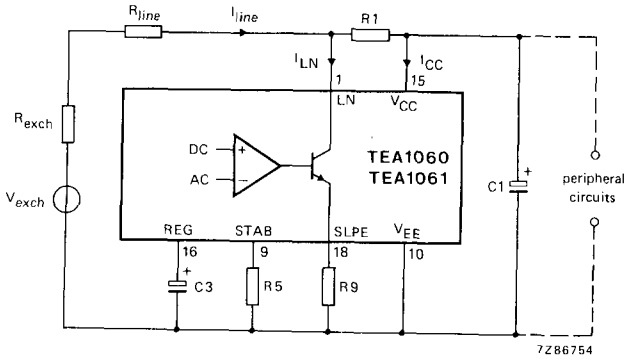


Fig. 3 Supply arrangement.

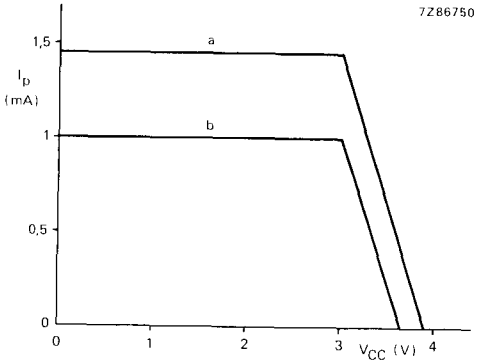


Fig. 4 Maximum current I_p available from V_{CC} for external (peripheral) circuitry. Curve "a" is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve "b" is valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)}$ = 150 mV, R_L = 150 Ω.

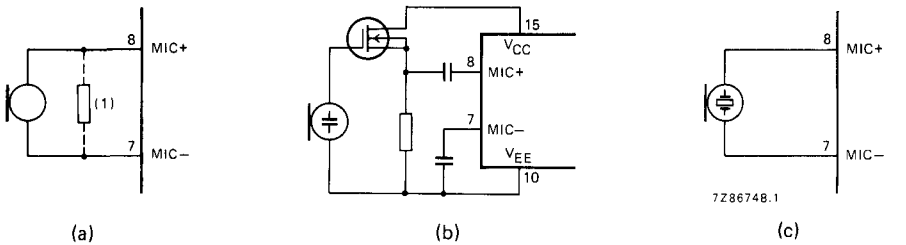


Fig. 5 Alternative microphone arrangements. (a) magnetic or dynamic microphone, TEA1060. The resistor marked (1) may be connected to lower the terminating impedance. (b) electret microphone, TEA1061. (c) piezoelectric microphone, TEA1061.

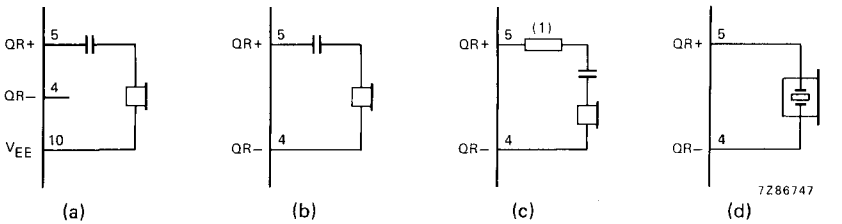


Fig. 6 Alternative receiver arrangements. (a) dynamic telephone with less than 450 Ω impedance. (b) dynamic telephone with more than 450 Ω impedance. (c) magnetic telephone. The resistor marked (1) may be connected to obtain an appropriate acoustic frequency characteristic. (d) piezoelectric telephone.

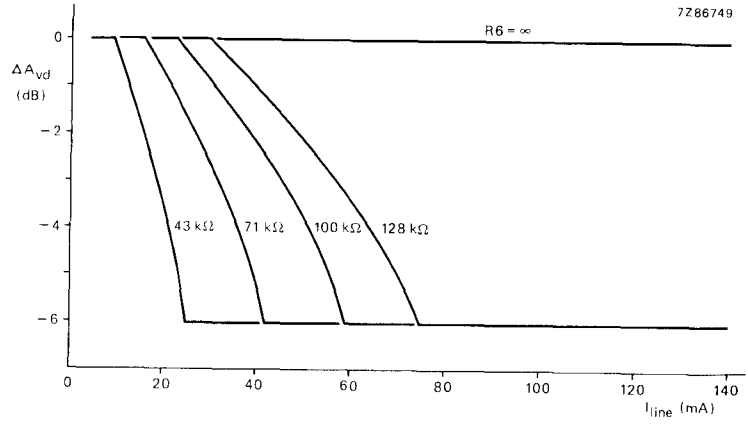


Fig. 7 Variation of amplification with line current, with R6 as a parameter.

Table 1. Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	55	43	X	X
	36	91	71	60	52
	48	128	100	84	71
	60	X	X	107	92

DEVELOPMENT SAMPLE DATA

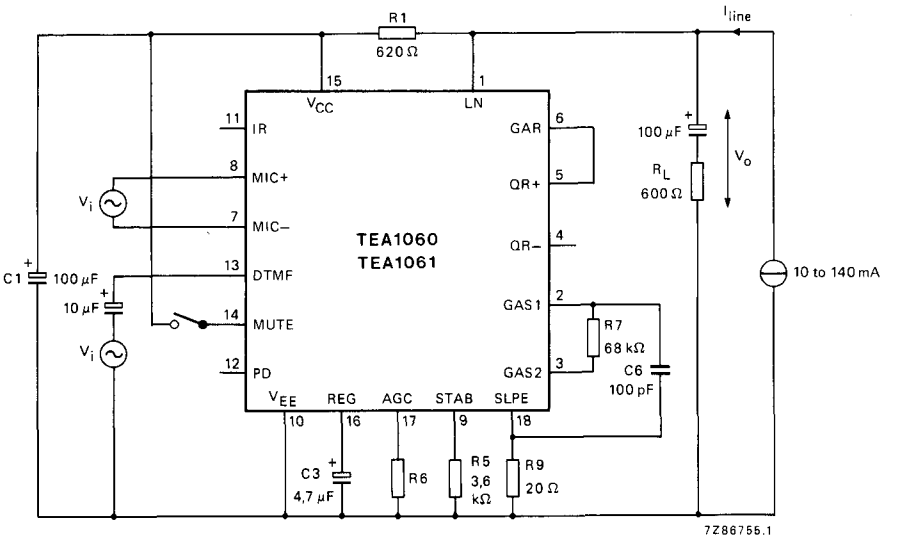


Fig. 8 Test circuit for defining voltage amplification of MIC+, MIC– and DTMF inputs. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$. For measuring the amplification from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

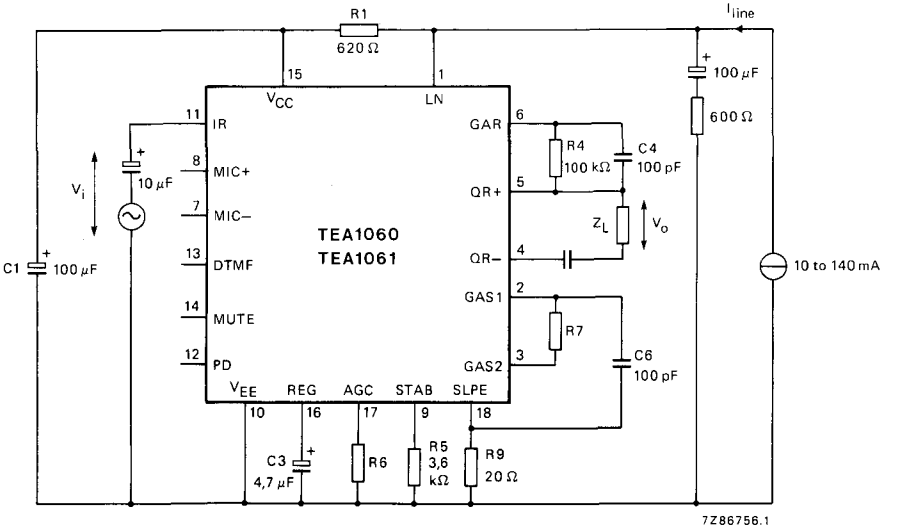


Fig. 9 Test circuit for defining voltage amplification of the receiving amplifier. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

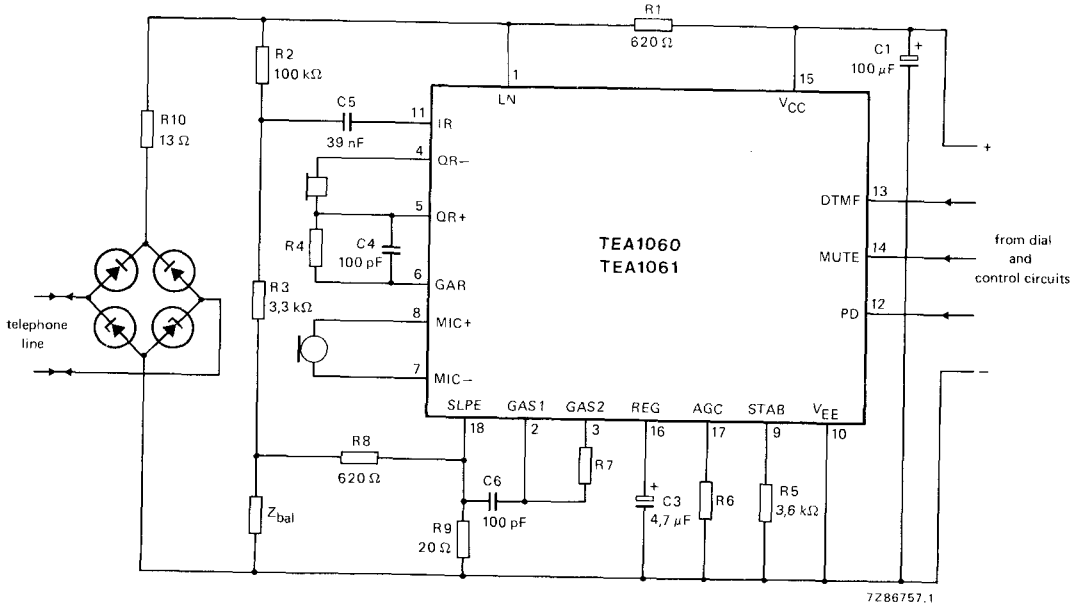


Fig. 10 Typical application of the TEA1060 or TEA1061, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

APPLICATION INFORMATION SUPPLIED ON REQUEST

APPLICATION INFORMATION (continued)

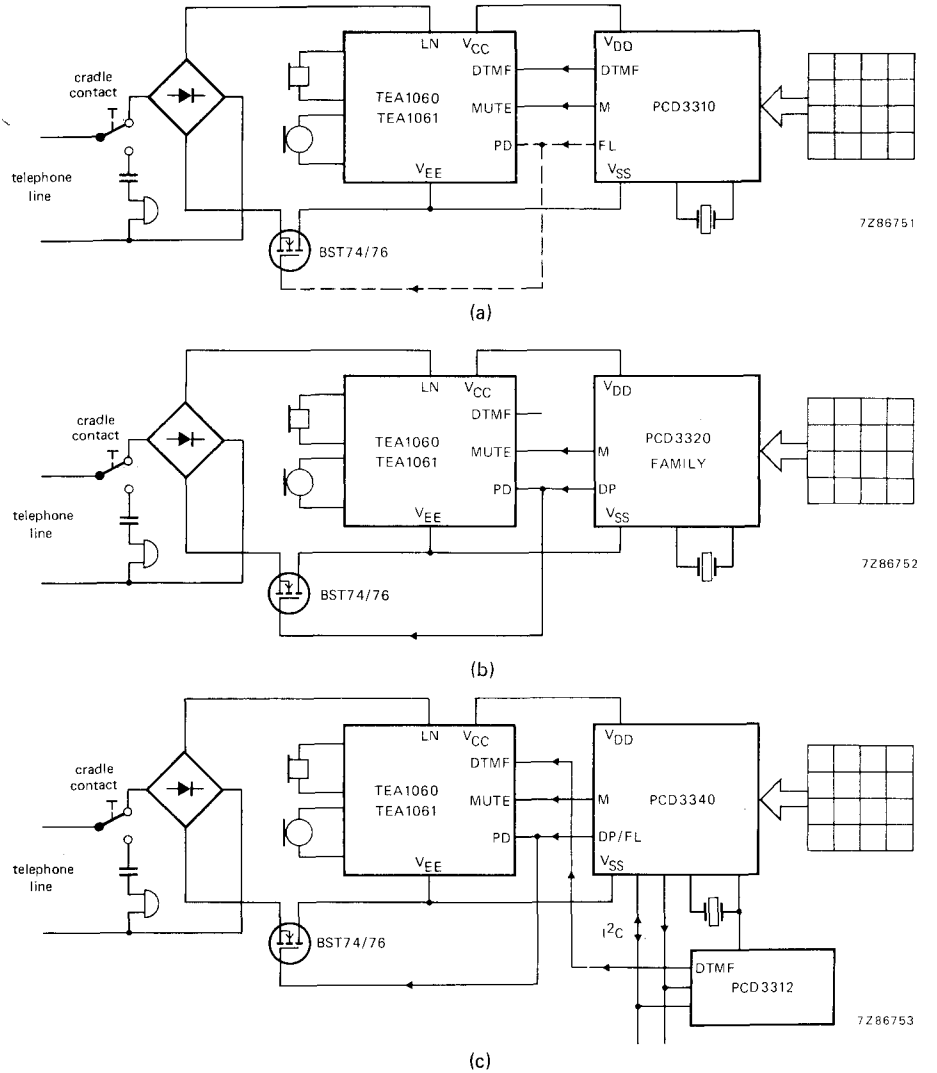


Fig. 11 Typical applications of the TEA1060 or TEA1061 (simplified).

(a) DTMF set with the PCD3310 CMOS DTMF dialling circuit with redial. The dashed lines show an optional flash (register recall by timed loop break).

(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

(c) Dual-standard (pulse and DTMF) feature phone with the PCD3340 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C bus.

VERSATILE TELEPHONE TRANSMISSION CIRCUITS

GENERAL DESCRIPTION

The TEA1062 and TEA1063 are bipolar integrated circuits performing all speech and line interface functions required in fully electronic telephone sets. The devices can be installed in the handset to facilitate two-wire connection to the dial and control circuits mounted in the base of the telephone set.

Features

- Voltage regulator with adjustable static resistance
- Symmetrical low-impedance inputs for dynamic and magnetic microphones (TEA1062)
- Symmetrical high-impedance inputs for piezoelectric microphone (TEA1063)
- Asymmetrical high-impedance input for electret microphone (TEA1063)
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on all amplifiers
- Line loss compensation facility, line current dependent
- Gain control adaptable to exchange supply

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{LN}	typ.	3,75	V
Line current operating range	I_{line}		10 to 140	mA
Supply current	I_{CC}	typ.	1	mA
Voltage amplification range				
microphone amplifier				
TEA1062	A_{vd}		44 to 60	dB
TEA1063	A_{vd}		30 to 46	dB
receiving amplifier	A_{vd}		17 to 39	dB
Amplification control range	ΔA_{vd}	typ.	6	dB
Exchange supply voltage range	V_{exch}		24 to 60	V
Exchange feeding bridge resistance range	R_{exch}		400 to 1000	Ω
Operating ambient temperature range	T_{amb}		−25 to + 75	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

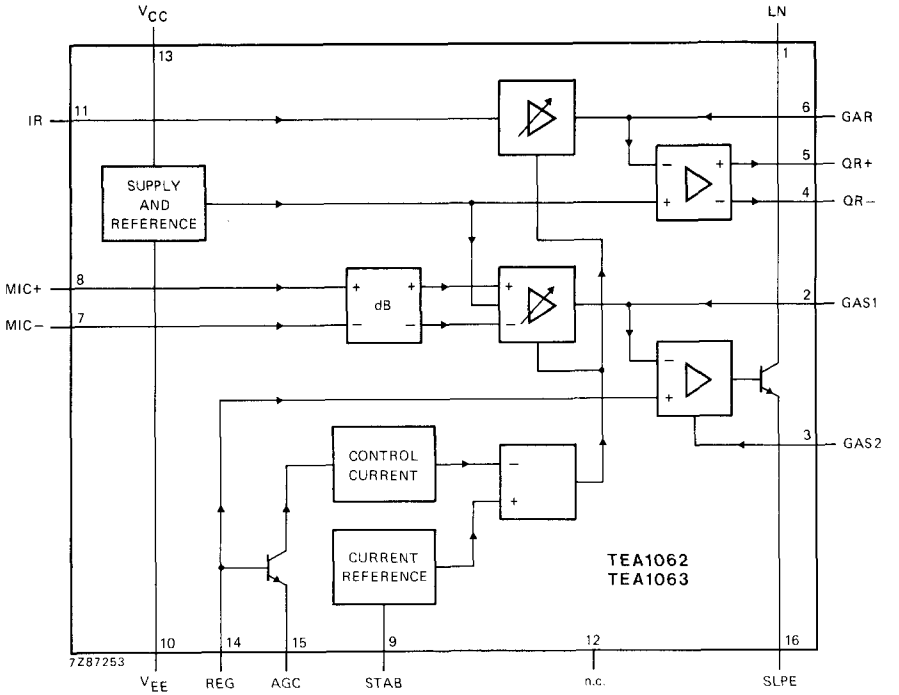


Fig. 1 Block diagram. The block marked "dB" is an attenuator which is present only in the TEA1063.

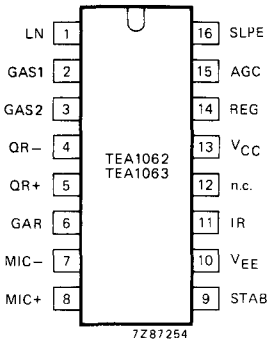


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR−	inverting output; receiving amplifier
5	QR+	non-inverting output; receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC−	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	n.c.	not connected
13	V_{CC}	positive supply decoupling
14	REG	voltage regulator decoupling
15	AGC	automatic gain control input
16	SLPE	slope (d.c. resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its associated dial and control circuits usually are supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be applied to a FET source follower to be used as an impedance converter for an electret microphone.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3,6 kΩ between STAB and V_{EE}.

The d.c. current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the d.c. resistance of the subscriber line R_{line} and the d.c. voltage on the subscriber set (see Fig. 3).

If the line current I_{line} exceeds the current I_{CC} required by the circuit itself, i.e. about 1 mA, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:

$$V_{LN} = V_{ref} + I_{LN} \times R9 = V_{ref} + (I_{line} - I_{CC}) \times R9,$$

V_{ref} being an internally generated temperature compensated reference voltage of 3,45 V and R9 being an external resistor connected between SLPE and V_{EE}. Under normal conditions $I_{LN} \gg I_{CC}$. The static behaviour of the circuit then equals a 3,45 V voltage regulator diode with an internal resistance R9. In the audio frequency range the dynamic impedance equals R1.

Microphone inputs MIC+ and MIC− and gain adjustment pins GAS1 and GAS2

The TEA1062 and TEA1063 have differential microphone inputs.

The TEA1062 is intended for low-sensitivity low-impedance dynamic or magnetic microphones. Its input impedance is 2 x 4 kΩ and its voltage amplification is typ. 52 dB.

The TEA1063 is intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 2 x 20 kΩ and its voltage amplification is typ. 38 dB.

The arrangements with the microphone types mentioned are shown in Fig. 4.

The amplification of the microphone amplifier in both types can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Receiving amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig. 5). Amplification from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the amplification is increased by 6 dB. This makes differential drive possible for high-impedance dynamic, magnetic and piezoelectric earpieces with load impedances exceeding 180 Ω.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and r.m.s. value is higher.

FUNCTIONAL DESCRIPTION (continued)

The amplification of the receiving amplifier can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R4 connected from GAR to QR+.

An external capacitor C4 of 100 pF between QR+ and GAR is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the amplification of the microphone amplifier and the receiving amplifier in accordance with the d.c. line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0,5 mm diameter copper twisted-pair cable with a d.c. resistance of 176 Ω/km and an average attenuation of 1,2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 6 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required, AGC may be left open. The amplifiers then all give their maximum amplification as specified.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of R2, R3, R8 and Z_{bal} (see Fig. 9). Maximum compensation is obtained when Z_{bal} equals the line impedance Z_{line} as seen by the set.

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal} approaches the average line impedance.

The anti-side-tone network attenuates the signal from the line. With R8 = 620 Ω and R9 = 20 Ω, the attenuation is 29,1 dB. The attenuation is flat over the audio frequency range.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive line supply voltage	V_{LN}	max.	15 V
Line current			
average	$I_{line(AV)}$	max.	140 mA
non-repetitive (t_{max} = 100 hours)	$I_{line(S)}$	max.	250 mA
non-repetitive peak (t_{max} = 1 ms)	$I_{line(SM)}$	max.	1 A
Voltage on all other pins	V	max.	V_{CC} + 0,7 V
	−V	max.	0,7 V
Total power dissipation	P_{tot}	max.	640 mW
Storage temperature range	T_{stg}		−40 to + 125 °C
Operating ambient temperature range	T_{amb}		−25 to + 75 °C

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 15)					
Voltage drop over circuit					
at I_{line} = 5 mA	V_{LN}	–	3,55	–	V
at I_{line} = 15 mA	V_{LN}	3,55	3,75	3,95	V
at I_{line} = 100 mA	V_{LN}	–	5,4	6,2	V
Variation with temperature	$\Delta V_{LN}/\Delta T$	−2	0	+ 2	mV/K
Supply current at V_{CC} = 2,8 V	I_{CC}	–	0,96	1,25	mA
Microphone inputs MIC+ and MIC−					
Input impedance					
TEA1062	$\lvert z_{is} \rvert$	–	4	–	kΩ
TEA1063	$\lvert z_{is} \rvert$	–	20	–	kΩ
Standard deviation on input impedance	σ	–	12	–	%
Common-mode rejection ratio; TEA1062	k_{CMR}	–	t.b.f.	–	dB
Voltage amplification at I_{line} = 15 mA; R7 = 68 kΩ					
TEA1062	A_{vd}	51	52	53	dB
TEA1063	A_{vd}	37	38	39	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	± 0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,5	–	dB
Gain adjustment pins GAS1 and GAS2					
Amplification variation with R7, transmitting amplifier	ΔA_{vd}	−8	–	+ 8	dB
Transmitting amplifier output LN					
Output voltage at I_{line} = 15 mA;					
d_{tot} = 2%	$V_{LN(rms)}$	1,2	1,8	–	V
d_{tot} = 10%	$V_{LN(rms)}$	–	2,1	–	V
Noise output voltage at I_{line} = 15 mA; R7 = 68 kΩ; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	−70	–	dBmp
Receiving amplifier input IR					
Input impedance	$\lvert z_{is} \rvert$	–	20	–	kΩ

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Receiving amplifier outputs QR+ and QR−					
Output impedance; single-ended	$\lvert z_{os} \rvert$	–	15	–	Ω
Voltage amplification					
at I_{line} = 15 mA; R4 = 100 kΩ; single-ended; R_L = 150 Ω	A_{vd}	24	25	26	dB
differential; R_L = 450 Ω	A_{vd}	30	31	32	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	± 0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,5	–	dB
Output voltage					
at d_{tot} = 2%; sine-wave drive single-ended; R_L = 150 Ω	$V_{o(rms)}$	0,25	0,3	–	V
differential; R_L = 450 Ω	$V_{o(rms)}$	0,45	0,55	–	V
differential; C_L = 47 nF; f = 3400 Hz	$V_{o(rms)}$	0,6	0,75	–	V
Noise output voltage					
at I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve) single-ended; R_L = 150 Ω	$V_{no(rms)}$	–	50	–	μV
differential; R_L = 450 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment pin GAR					
Amplification variation with R4, receiving amplifier	ΔA_{vd}	−8	–	+ 8	dB
Automatic gain control input AGC					
Amplification control range	$-\Delta A_{vd}$	–	6	–	dB
Highest line current for maximum amplification at R6 = 100 kΩ	I_{line}	–	23	–	mA
Lowest line current for minimum amplification at R6 = 100 kΩ	I_{line}	–	58	–	mA

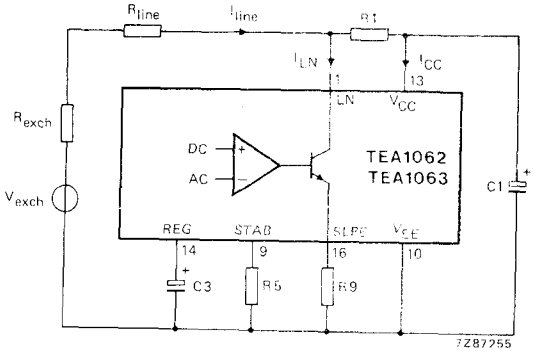


Fig. 3 Supply arrangement.

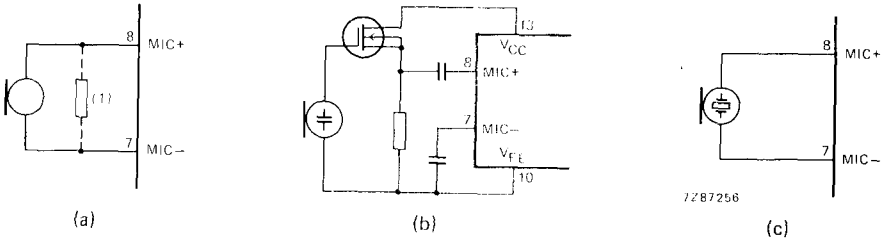


Fig. 4 Alternative microphone arrangements: (a) magnetic or dynamic microphone, TEA1062 (the resistor marked (1) may be connected to lower the terminating impedance); (b) electret microphone, TEA1063; (c) piezoelectric microphone, TEA1063.

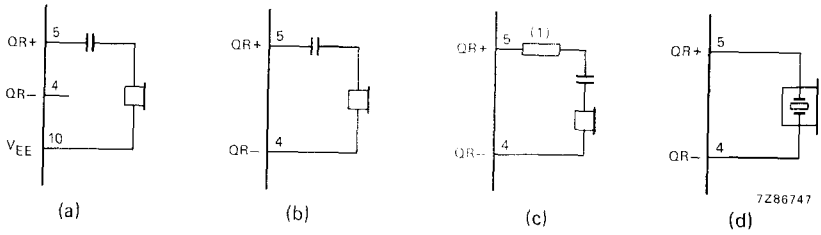


Fig. 5 Alternative receiver arrangements: (a) dynamic telephone with less than 180 Ω impedance; (b) dynamic telephone with more than 180 Ω impedance; (c) magnetic telephone (the resistor marked (1) may be connected to obtain an appropriate acoustic frequency characteristic); (d) piezoelectric telephone.

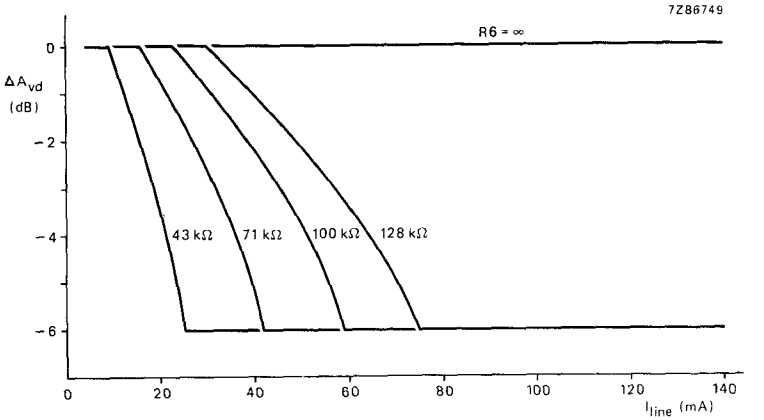


Fig. 6 Variation of amplification with line current, with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for common values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	55	43	X	X
	36	91	71	60	52
	48	128	100	84	71
	60	X	X	107	92

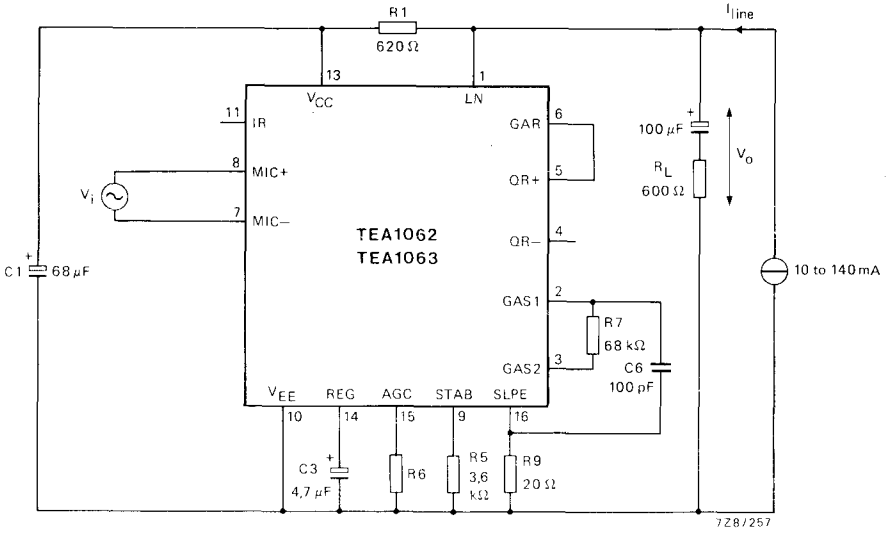


Fig. 7 Test circuit for defining voltage amplification of MIC+, MIC− inputs. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$. Inputs not under test should be open circuit.

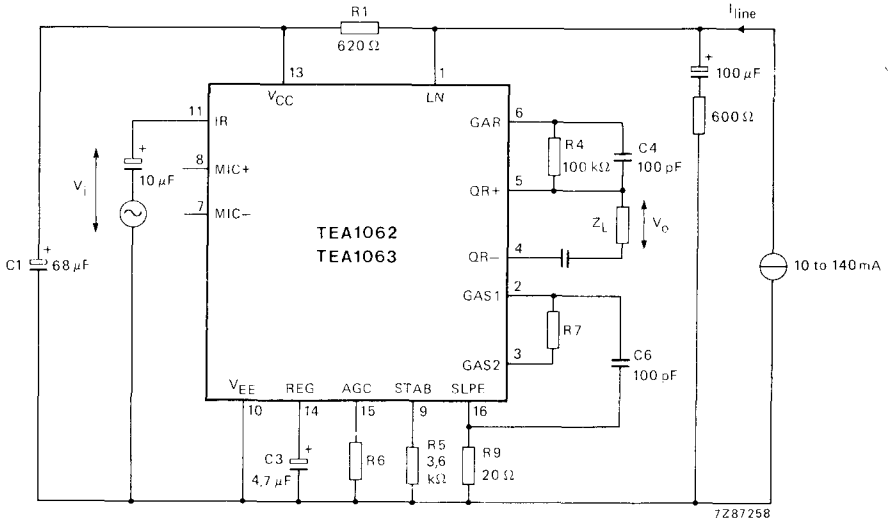


Fig. 8 Test circuit for defining voltage amplification of the receiving amplifier. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

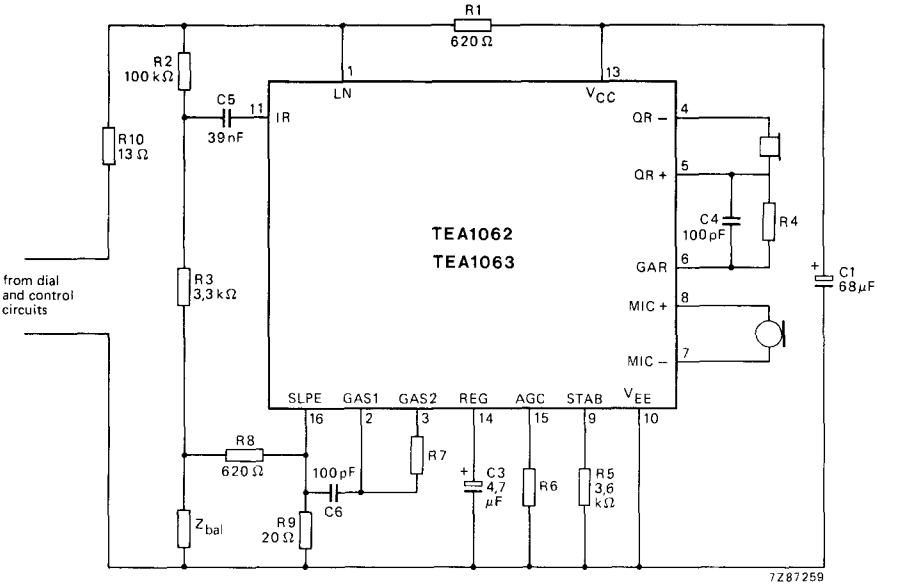
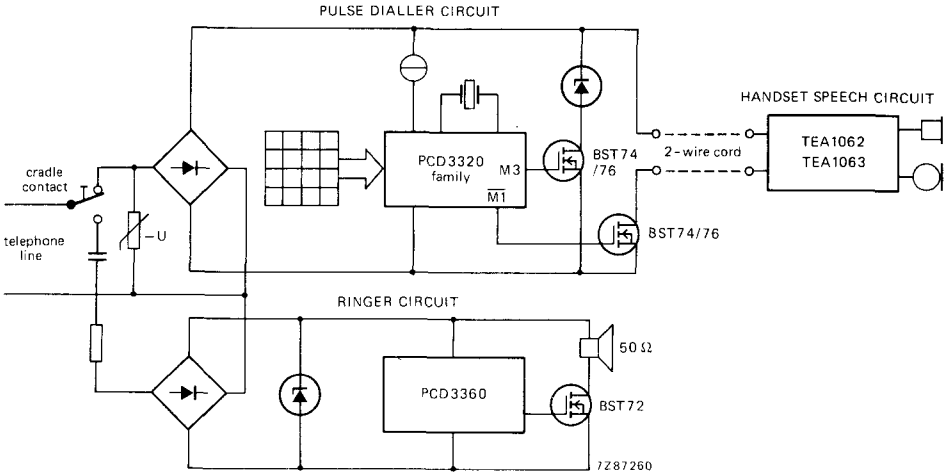
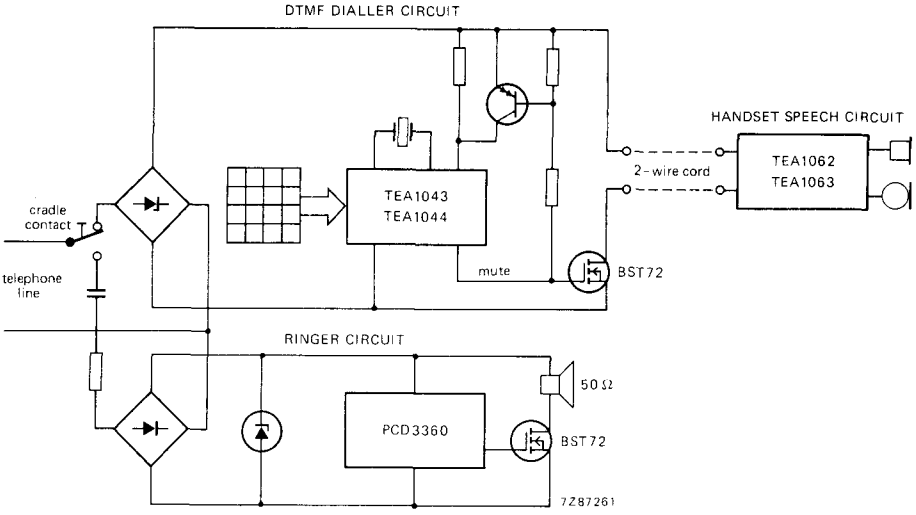


Fig. 9 Typical application of the TEA1062 or TEA1063, shown here with a piezoelectric earpiece. Resistor R10 limits the current into the circuit during line transients. Voltage limitation resulting from transients depends on the dialling system and is not indicated.

APPLICATION INFORMATION SUPPLIED ON REQUEST



(a)



(b)

Fig. 10 Typical applications (simplified) of the TEA1062 or TEA1063: (a) basic pulse dial set with one of the PCD3320 family of C-MOS interrupted current-loop dialling circuits; (b) basic DTMF set with TEA1043/TEA1044 bipolar DTMF dialler.

DOMESTIC APPLIANCES

GENERAL-PURPOSE TRIGGERING CIRCUIT

GENERAL DESCRIPTION

The TCA280A is a bipolar integrated circuit delivering positive pulses for triggering a triac or a thyristor. The flexibility of the circuit makes it suited for a great variety of applications, such as:

- synchronous on/off switching
- phase control
- time-proportional control
- temperature control
- motor speed control

Features

- adjustable proportional range
- adjustable hysteresis
- adjustable firing burst repetition time
- adjustable pulse width
- supplied from the mains
- provides supply for external temperature bridge
- low supply current, low dissipation

QUICK REFERENCE DATA

Supply voltage, d.c. (derived from mains voltage)	V_{CC}	typ.	14,4 V
Supply current (average value)	I_{CC}	typ.	1 mA
Output current	$-I_{OH}$*	max.	200 mA
Output pulse width	t_w	typ.	190 μs
Power dissipation, unloaded	P	typ.	15 mW
Operating ambient temperature range	T_{amb}		−20 to + 80 °C

* Negative current is defined as conventional current flow out of a device. A negative output current is suited for positive triac triggering.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

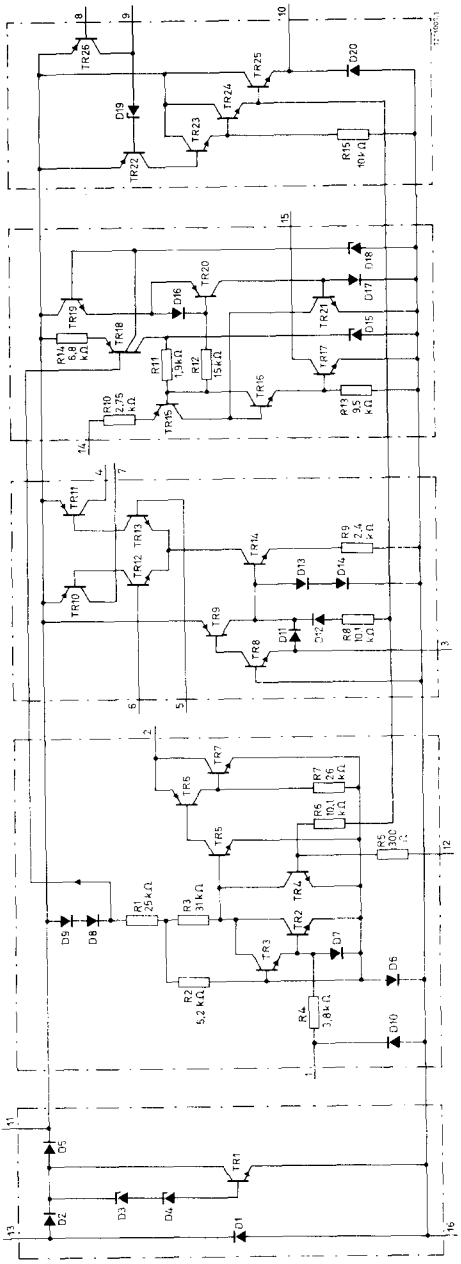


Fig. 1 Circuit diagram.

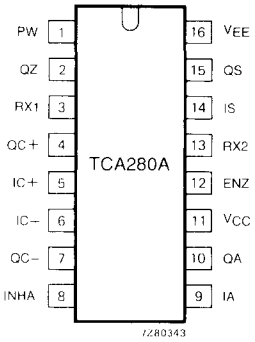


Fig. 2 Pinning diagram.

PINNING

1	PW	pulse width control input
2	QZ	zero-crossing detector output
3	RX1	external resistor
4	QC+	comparator non-inverting output
5	IC+	comparator non-inverting input
6	IC−	comparator inverting input
7	QC−	comparator inverting output
8	INHA	output stage inhibiting input
9	IA	output stage input
10	QA	output stage output
11	V_{CC}	positive supply
12	ENZ	enable input, zero crossing detector
13	RX2	external resistor
14	IS	sawtooth generator trigger input
15	QS	sawtooth generator output
16	V_{EE}	ground

FUNCTIONAL DESCRIPTION

The TCA280A contains four circuits that may be interconnected externally to perform the function required, and a supply part. The four circuits are a zero-crossing detector, a differential amplifier, a sawtooth generator and an output stage.

Supply: V_{CC} and RX2 (pins 11 and 13)

The TCA280A may be supplied by an external d.c. power supply connected to V_{CC} (pin 11), but usually it is supplied directly from the mains voltage. For this purpose the circuit contains a string of stabilizer diodes between V_{CC} and V_{EE} that limit the d.c. supply voltage. An external resistor R_d has to be connected from the mains to RX2; V_{EE} is connected to the neutral line (see Figs 5 and 6). A smoothing capacitor C1 has to be connected between V_{CC} and V_{EE}. The circuit produces a positive supply voltage at V_{CC}; this may be used to supply an external circuit such as a temperature sensing bridge.

During the positive half of the mains cycles the current through external voltage dropping resistor R_d charges the external smoothing capacitor C1 to the stabilizing voltage of the internal stabilizer diodes. R_d should be chosen such that it can supply the current for the TCA280A itself (see Fig. 4) plus any current taken up by an external (peripheral) circuit connected to V_{CC}, and recharge the smoothing capacitor C1. Any excess current is bypassed by the internal stabilizer diodes. Note that the maximum rated supply current must not be exceeded.

During the negative half of the mains cycles external smoothing capacitor C1 supplies the circuit. Its capacitance must be high enough to maintain the supply voltage above the minimum specified limit. For values of R_d and C1 see Figs 5 and 6.

Dissipation in resistor R_d is halved by connecting a diode in series (see Figs 7 and 8). For phase control applications this arrangement should always be used.

A suitable VDR connected across the mains provides protection of the TCA280A and of the triac against mains-borne transients.

FUNCTIONAL DESCRIPTION (continued)

Zero-crossing detector

The TCA280A contains a zero-crossing detector intended to produce pulses that coincide with the zero crossings of the mains voltage for minimum r.f. interference and transients on the mains supply.

The pulse width control input PW (pin 1) permits adjustment of the pulse width at output QZ (pin 2) to the value required for the triac by choosing the value of the external synchronization resistor R_S between PW and the a.c. mains. The pulse width is inversely proportional to the input current and to the mains frequency.

The zero-crossing detector is inhibited when the ENZ input (pin 12) is HIGH, and it is enabled when ENZ is LOW, e.g. connected to V_{EE}.

Output QZ is an n-p-n open-collector output requiring an external collector resistor to V_{CC}. QZ produces negative-going output pulses.

Comparator

IC+ and IC− (pins 5 and 6) are differential inputs of a comparator or difference amplifier, with QC+ and QC− (pins 4 and 7) as complementary outputs. QC+ and QC− are p-n-p open-collector outputs requiring external collector resistors to V_{EE}. QC+ will be HIGH and QC− will be LOW when IC+ is higher than IC−.

The comparator contains a long-tailed pair with a current source in its tail. The tail current is activated by a current into RX1 (pin 3). When an inductive load is driven with phase control the trigger pulse may be terminated at the instant of firing of the thyristor or triac. This may be achieved by connecting RX1 via a resistor to the anode of the thyristor or triac.

Sawtooth generator

The sawtooth generator may be used to produce bursts of trigger pulses, with the net effect that the load is periodically switched on and off.

The heart of the sawtooth generator is a thyristor arrangement. The firing burst repetition time is usually determined by an external resistor and capacitor connected to the sawtooth generator trigger input IS (pin 14). The repetition time is typ. 0,7 x RC.

The output QS (pin 15) is an n-p-n open-collector output. During the flyback of the sawtooth the transistor is ON and is capable of sinking current.

Output stage

The output stage is driven by a current drawn out of input IA (pin 9). This drive may be inhibited by drawing a current out of inhibiting input INHA (pin 8). Hence the output will be HIGH only if current is drawn out of IA and no current is drawn out of INHA i.e. if inhibiting input INHA (pin 8) is HIGH and input IA (pin 9) is LOW. Both inputs may be used as a single input provided the other one is suitably biased.

The output QA (pin 10) is an n-p-n open-emitter output capable of sourcing an output current, i.e. conventional current flow out of the circuit.

A gate resistor R_G should be connected between the output QA and the triac or thyristor gate to limit the output current to the minimum required by the triac or thyristor. This minimizes the total supply current and the power dissipation. Output QA is protected with a diode to V_{EE} (pin 16) against damage by undershoot of the output voltage, e.g. caused by an inductive load.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (voltage source)	V_{CC}	max.	17 V
Supply current (current source)			
average	$I_{RX2(AV)}$	max.	30 mA
repetitive peak	$I_{RX2(RM)}$	max.	80 mA
non-repetitive peak ($t < 10\ \mu s$)	$I_{RX2(SM)}$	max.	2 A
Input voltage, all inputs	V_I	max.	17 V
Differential input voltage between IC+ and IC−	V_{ID}	max.	7 V
Input current, all inputs	I_I	max.	10 mA
Output current			
average	$-I_{QA(AV)}$	max.	30 mA
non-repetitive peak ($t < 300\ \mu s$)	$-I_{QA(SM)}$	max.	600 mA
Total power dissipation	P_{tot}	see Fig. 3	
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +80	°C

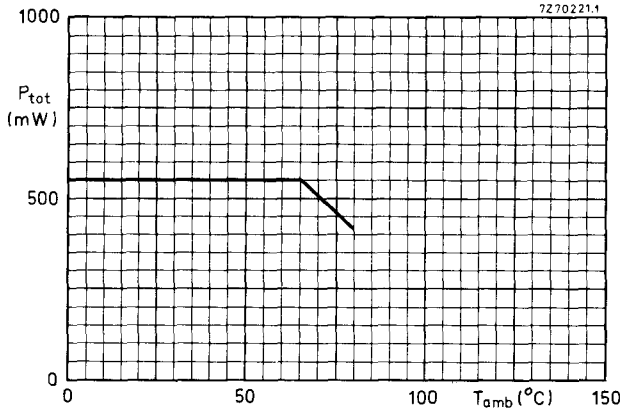


Fig. 3 Power derating curve.

CHARACTERISTICS

V_{CC} = 11 to 17 V; V_{EE} = 0 V; I_{RX1} = 10 μA or $-I_{RX1}$ = 30 μA; T_{amb} = 25 °C unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage, external	V_{CC}	11	–	17	V
Supply voltage, internally generated, at $I_{RX2(RMS)}$ = 5 mA, unloaded	V_{CC}	11	14,3	15	V
Supply current, unloaded	I_{CC}	0,3	–	0,75	mA
Variation with supply voltage	$\Delta I_{CC}/\Delta V_{CC}$	–	–	0,03	mA/V
Pulse width control input PW (pin 1)					
Input voltage at I_{PW} = 100 μA	V_{PW}	–	–	1,9	V
at $-I_{PW}$ = 100 μA	$-V_{PW}$	–	–	0,25	V
Input current at I_{QZ} = 0,5 mA	$I_{PW(RMS)}$	30	–	50	μA
Pulse width at $I_{PW(RMS)}$ = 1 mA; f = 50 Hz (at pin 2)	t_w	–	190	–	μs
Variation with supply voltage	$\Delta t/\Delta V$	–	27	–	μs/V
Zero crossing detector enable input ENZ (pin 12)					
Input voltage HIGH (inhibit)	V_{ENZH}	1,2	–	–	V
LOW (enable)	V_{ENZL}	–	–	0	V
Zero crossing detector output QZ (pin 2)					
Output current HIGH	I_{QZH}	–	–	1	μA
LOW	I_{QZL}	–	–	40	mA
Comparator input IC+ and IC– (pins 5 and 6)					
Differential input voltage	$\pm V_{ID}$	–	–	7	V
Input bias current at $V_{IC+} > V_{IC-} + 1$ V	I_{IC+}	–	5	10	μA
at $V_{IC-} > V_{IC+} + 1$ V	I_{IC-}	–	5	10	μA
Comparator outputs QC+ and QC– (pins 4 and 7)					
Output voltage at $-I_{OH}$ = 0,3 mA	V_{OH}	$V_{CC}-1,5$	–	–	V
Output current HIGH	$-I_{OH}$	–	–	0,3	mA
LOW	$-I_{OL}$	–	–	90	nA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Sawtooth generator trigger input IS (pin 14)					
Input trigger voltage	V_{ISH}	7	–	8,3	V
Input trigger current	I_{ISH}	–	–	3	μA
Thyristor holding voltage	V_{ISL}	1,8	–	2,8	V
Thyristor holding current	I_{ISL}	95	–	210	μA
Sawtooth generator output QS (pin 15)					
Output current					
LOW	I_{QSL}	–	–	5	mA
HIGH	I_{QSH}	–	–	100	nA
Output stage inhibiting input INHA (pin 8)					
Input current at $-I_{IA}$ = 100 μA	$-I_{INHA}$	20	–	50	μA
Input voltage at $-I_{IA}$ = 100 μA	V_{INHA}	–	$V_{CC}-2$	–	V
Output stage input IA (pin 9)					
Input current at $-I_{QA}$ = 200 mA	$-I_{IA}$	15	–	–	μA
Input voltage at $-I_{IA}$ = 50 μA	V_{IA}	$V_{CC}-8,3$	–	$V_{CC}-7$	V
Output stage output QA (pin 10)					
Output voltage HIGH at $-I_{QAH}$ = 200 mA; V_{CC} = 13 V; INHA open	V_{QAH}	$V_{CC}-2,8$	–	–	V
Output current					
HIGH	$-I_{QAH}$	–	–	200	mA
LOW at V_{QA} = 0	I_{QAL}	–	–	1	μA

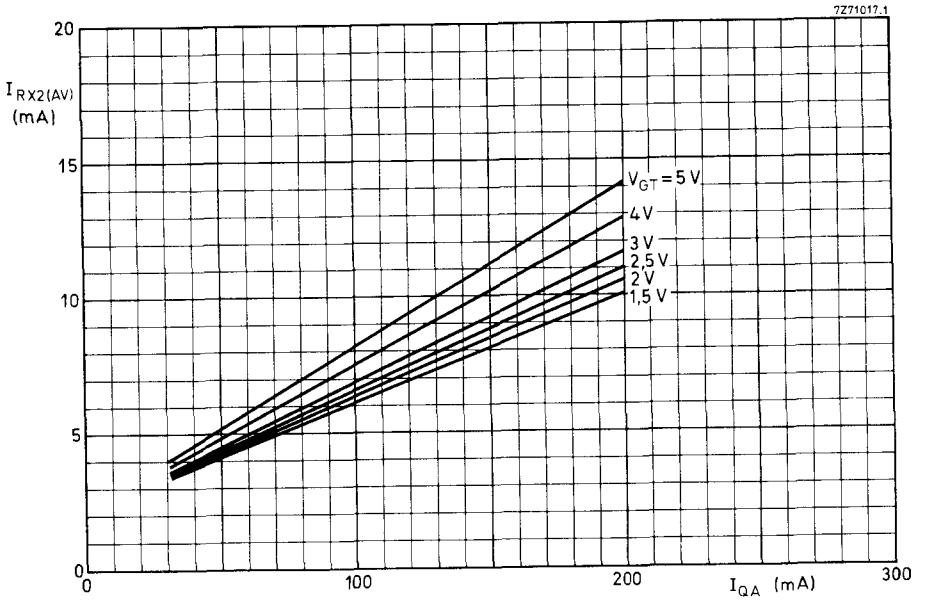
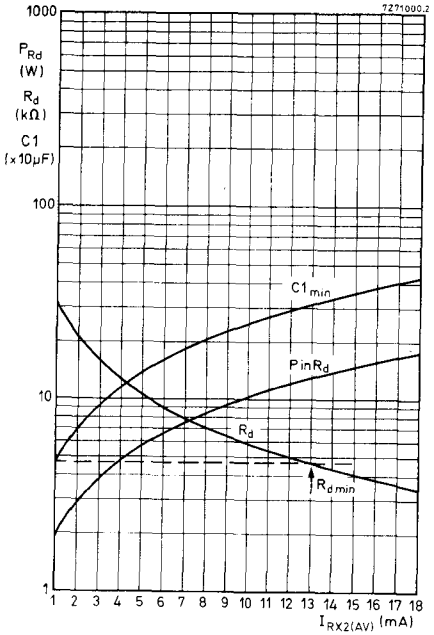


Fig. 4 Average supply current $I_{RX2(AV)}$ as a function of output current I_{QA} with triac gate trigger voltage V_{GT} as a parameter; typical performance.



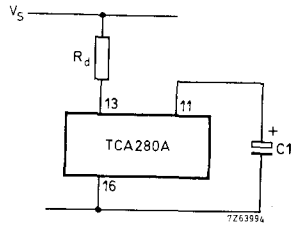
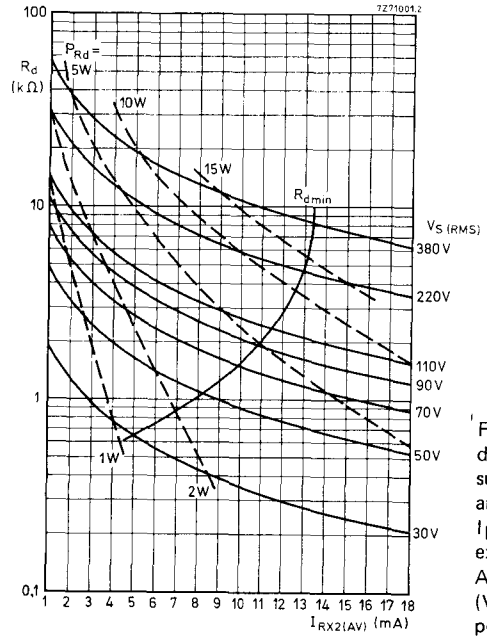


Fig. 5 Voltage dropping resistor R_d, dissipation P_{Rd} in this resistor, and recommended minimum value of smoothing capacitor C1 as a function of average supply current $I_{RX2(AV)}$, for the supply arrangement without series diode. Note that the supply current $I_{RX2(AV)}$ includes the supply current of any external (peripheral) circuit supplied from V_{CC}; typical performance.



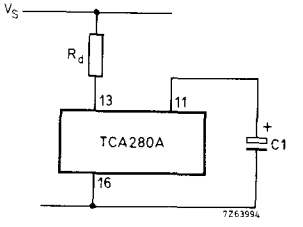
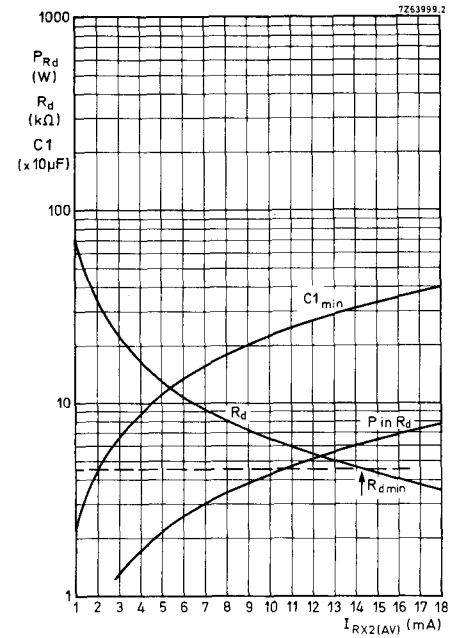


Fig. 6 Voltage dropping resistor R_d and power dissipation P_{Rd} in this resistor as a function of supply current $I_{RX2(AV)}$, for the supply arrangement without series diode. Note that $I_{RX2(AV)}$ includes the supply current of any external (peripheral) circuit supplied from V_{CC}. Also shown is the r.m.s. mains supply voltage ($V_{S(RMS)}$) as a function of $I_{RX2(AV)}$; typical performance.



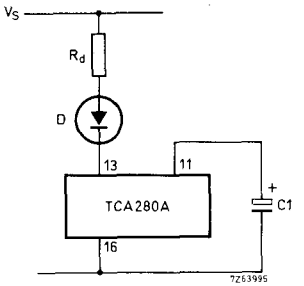
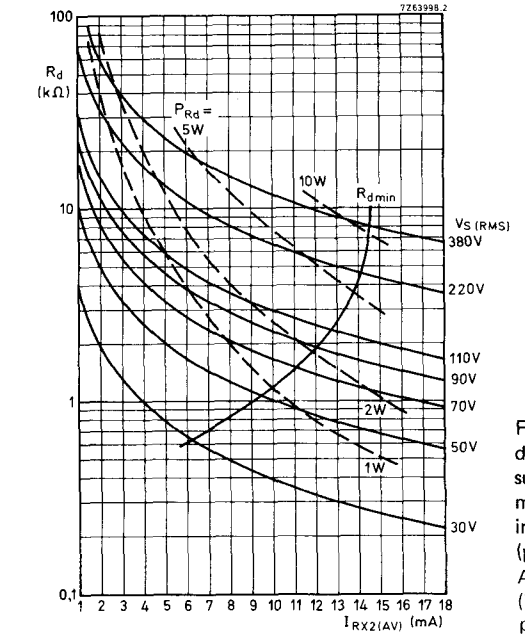


Fig. 7 Voltage dropping resistor R_d, dissipation P_{Rd} in this resistor, and recommended minimum value of smoothing capacitor C1 as a function of average supply current $I_{RX2(AV)}$, for the supply arrangement with series diode D. $I_{RX2(AV)}$ includes the supply current of any external (peripheral) circuit supplied from V_{CC}.
It should be noted that certain applications like the time proportional controller require a value of the smoothing capacitor C1 that is up to three times higher; typical performance.



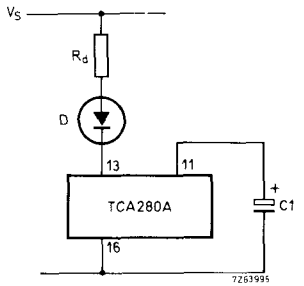


Fig. 8 Voltage dropping resistor R_d and power dissipation P_{Rd} in this resistor as a function of supply current $I_{RX2(AV)}$, for the supply arrangement with series diode. Note that $I_{RX2(AV)}$ includes the supply current of any external (peripheral) circuit supplied from V_{CC}.
Also shown is the r.m.s mains supply voltage ($V_{S(RMS)}$) as a function of $I_{RX2(AV)}$; typical performance.

APPLICATION INFORMATION

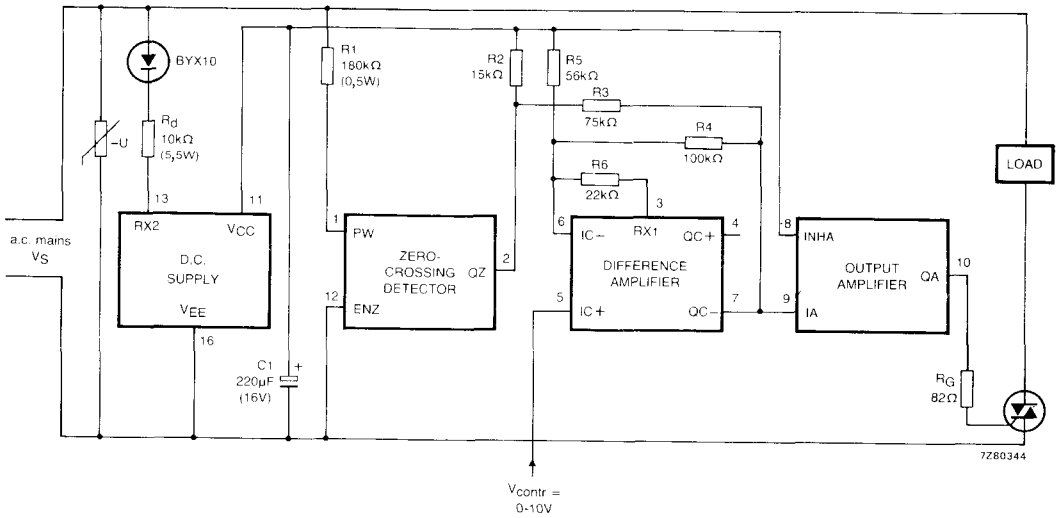


Fig. 9 Typical application of the TCA280A as a static switch for resistive loads. The arrangement gives triggering around the zero crossings of the mains voltage. The values shown for R_d, R_G and C1 give a gate current I_{GT} = 100 mA typical at V_{GT} = 2,5 V and a trigger pulse duration t_w = 160 μs typical.

APPLICATION INFORMATION (continued)

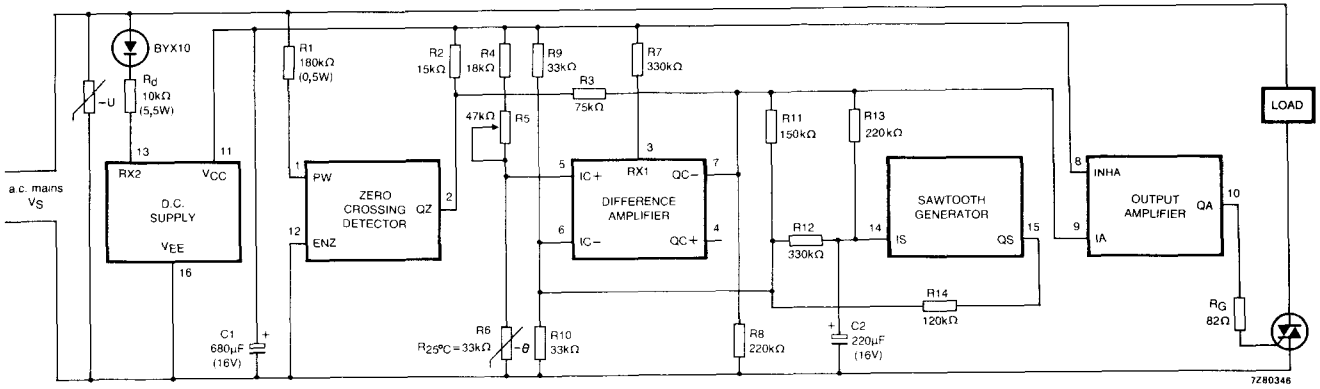


Fig. 10 Typical application of the TCA280A as a time proportional temperature controller. The arrangement gives triggering around the zero crossings of the mains voltage as long as the voltage produced by the temperature bridge connected to IC+ (pin 5) is higher than the voltage on IC− (pin 6). The voltage on IC− is a sawtooth superimposed on a d.c. reference voltage. The sawtooth has a repetition time of about 30 s; this time is determined by C2. The proportional band is determined by the amplitude of the sawtooth; this can be chosen by the value of R12. The values shown for R_d, R_G and C1 give a gate current I_{GT} = 100 mA typ. at V_G = 2,5 V and a trigger pulse duration t_w = 160 μs typ.

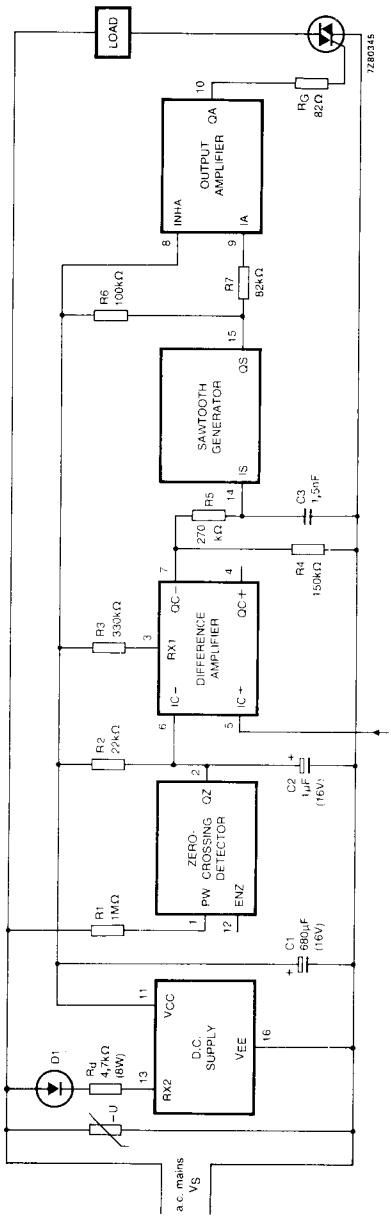


Fig. 11 Typical application of the TCA280A as a single-phase control circuit. The circuit produces bursts of trigger pulses at the gate of the triac or thyristor. The pulses coincide with the zero crossings of the mains voltage. The arrangement forms a full-wave a.c. controller when used with a triac, and a controlled half-wave rectifier when used with a thyristor.

PROPORTIONAL-CONTROL TRIAC TRIGGERING CIRCUIT

GENERAL DESCRIPTION

The TDA1023 is a bipolar integrated circuit for controlling triacs in the time proportional or burst firing mode. It permits very precise temperature control of heating equipment and is especially suited for the control of panel heaters. The circuit generates positive-going trigger pulses and complies with the regulations on radio interference and mains distortion.

Special features are:

- adjustable proportional range width
- adjustable hysteresis
- adjustable trigger pulse width
- adjustable firing burst repetition time
- control range translation facility
- failsafe operation
- supplied from the mains
- provides supply for external temperature bridge

QUICK REFERENCE DATA

Supply voltage (derived from mains voltage)	V_{CC}	typ.	13,7 V
Stabilized supply voltage for temperature bridge	V_Z	typ.	8 V
Supply current (average value)	$I_{16(AV)}$	typ.	10 mA
Trigger pulse width	t_w	typ.	200 μs
Firing burst repetition time at $C_T = 68\ \mu F$	T_b	typ.	41 s
Output current	$-I_{OH}$*	max.	150 mA
Operating ambient temperature range	T_{amb}		−20 to + 75 °C

* Negative current is defined as conventional current flow out of a device. A negative output current is suited for positive triac triggering.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

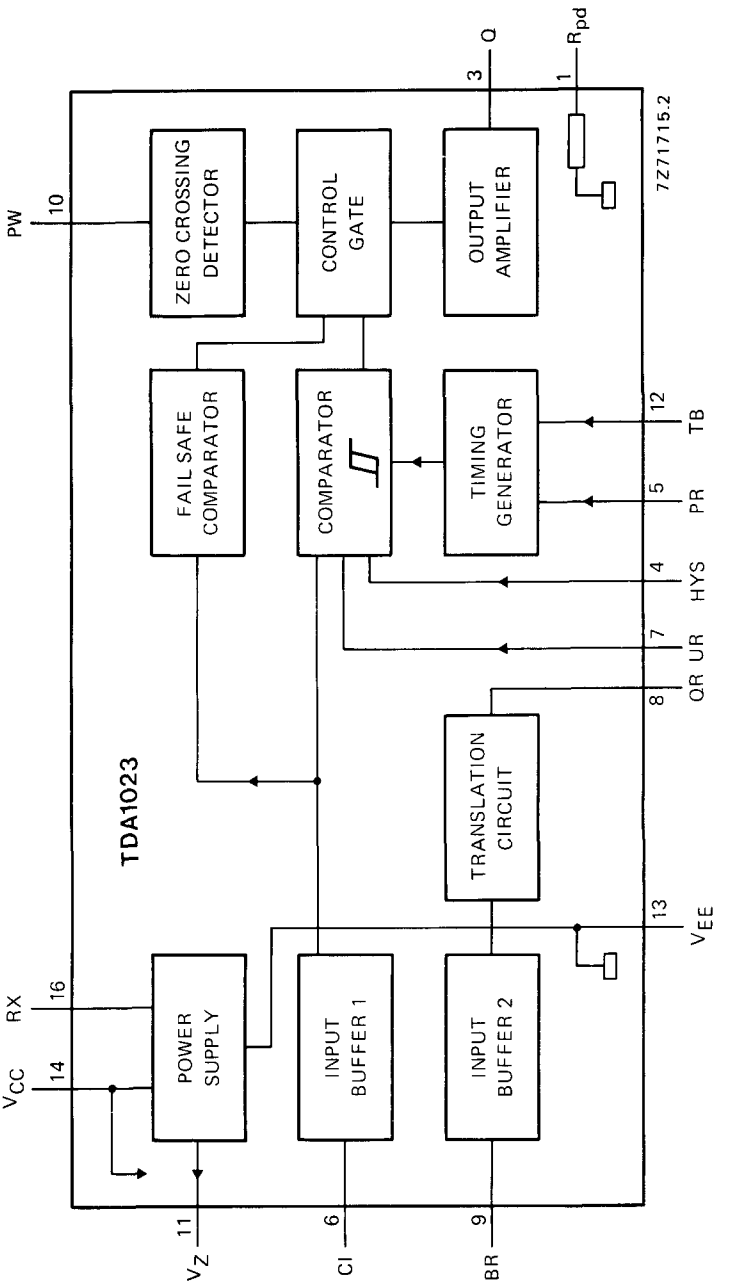


Fig. 1 Block diagram.

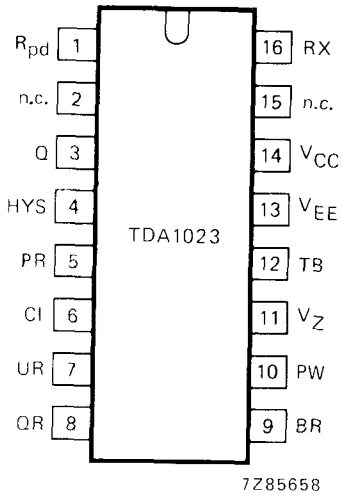


Fig. 2 Pinning diagram.

PINNING

1	R_{pd}	internal pull-down resistor connection
2	n.c.	not connected
3	Q	output
4	HYS	hysteresis control input
5	PR	proportional range control input
6	CI	Control input
7	UR	unbuffered reference input
8	QR	output of reference buffer
9	BR	buffered reference input
10	PW	pulse width control input
11	V_Z	reference supply output
12	TB	firing burst repetition time control input
13	V_{EE}	ground connection
14	V_{CC}	positive supply connection
15	n.c.	not connected
16	RX	external resistor connection

FUNCTIONAL DESCRIPTION

The TDA1023 generates pulses to trigger a triac. These trigger pulses coincide with the zero crossings of the mains voltage. This minimizes r.f. interference and transients on the mains supply. The trigger pulses come in bursts, with the net effect that the load is periodically switched on and off. This further minimizes mains pollution. The average power in the load is varied by varying the duration of the trigger pulse burst, in accordance with the voltage difference between the control input CI and the reference input, either UR or BR.

Power supply: V_{CC}, RX and V_Z (pins 14, 16 and 11)

The TDA1023 is supplied from the a.c. mains via a resistor R_D to the RX connection (pin 16); the V_{EE} connection (pin 13) is connected to the neutral line (see Fig. 4a). A smoothing capacitor C_S has to be connected between the V_{CC} and V_{EE} connections.

The circuit contains a string of stabilizer diodes between the RX and V_{EE} connections that limit the d.c. supply voltage, and a rectifier diode between the RX and V_{CC} connections (see Fig. 3).

At pin 11 the device provides a stabilized reference voltage V_Z for an external temperature sensing bridge.

The operation of the supply arrangement is as follows. During the positive half of the mains cycles the current through external voltage dropping resistor R_D charges the external smoothing capacitor C_S until RX reaches the stabilizing voltage of the internal stabilizer diodes. R_D should be chosen such that it can supply the current I_{CC} for the TDA1023 itself plus the average output current $I_{3(AV)}$ plus the current required from the V_Z connection for an external temperature bridge, and recharge the smoothing capacitor C_S (see Figs 9 to 12). Any excess current is bypassed by the internal stabilizer diodes. Note that the maximum rated supply current must not be exceeded.

During the negative half of the mains cycles external smoothing capacitor C_S has to supply the sum of the currents mentioned above. Its capacitance must be high enough to maintain the supply voltage above the minimum specified limit.

FUNCTIONAL DESCRIPTION (continued)

Dissipation in resistor R_D is halved by connecting a diode in series (see Fig. 4b and 9 to 12).

A further reduction of dissipation is possible by using a high-quality voltage dropping capacitor C_D in series with a resistor R_{SD} (see Figs 4c and 14). Asuitable VDR connected across the mains provides protection of the TDA1023 and of the triac against mains-borne transients.

Control and reference inputs CI, BR and UR (pins 6, 9 and 7)

For room temperature control (5 °C to 30 °C) the best performance is obtained by using the translation circuit. The buffered reference input BR (pin 9) is used as a reference input, and the output of the reference buffer QR (pin 8) is connected to the unbuffered reference input UR (pin 7). In this arrangement the translation circuit ensures that most of the potentiometer rotation can be used to cover the room temperature range. This provides an accurate temperature setting and a linear temperature scale.

If the translation circuit is not required, the unbuffered reference input UR (pin 7) is used as a reference input. The buffered reference input BR (pin 9) must be connected to the reference supply output V_Z (pin 11).

For proportional power control the unbuffered reference input UR (pin 7) must be connected to the firing burst repetition time control input TB (pin 12) and the buffered reference input BR (pin 9), which is inactive now, must be connected to the reference supply output V_Z (pin 11).

In all arrangements the train of output pulses becomes longer when the voltage at the control input CI (pin 6) becomes lower.

Proportional range control input PR (pin 5)

With the proportional range control input PR open the output duty factor changes from 0% to 100% by a variation of 80 mV at the control input CI (pin 6). For temperature control this corresponds with a temperature difference of only 1 K.

This range may be increased to 400 mV, i.e. 5 K, by connecting the proportional range control input PR (pin 5) to ground. Intermediate values are obtained by connecting the PR input to ground via a resistor R5, see Table 1.

Hysteresis control input HYS (pin 4)

With the hysteresis control input HYS (pin 4) open the device has a built-in hysteresis of 20 mV. For temperature control this corresponds with 0,25 K.

Hysteresis is increased to 320 mV, corresponding with 4 K, by grounding HYS (pin 4). Intermediate values are obtained by connecting pin 4 to ground via a resistor R4. See Table 1 for a set of values for R4 and R5 giving a fixed ratio between hysteresis and proportional range.

Trigger pulse width control input PW (pin 10)

The trigger pulse width may be adjusted to the value required for the triac by choosing the value of the external synchronization resistor R_S between the trigger pulse width control input PW (pin 10) and the a.c. mains. The pulse width is inversely proportional to the input current (see Fig. 13).

Output Q (pin 3)

Since the circuit has an open-emitter output, it is capable of sourcing current, i.e. supplying a current out of the output. Therefore it is especially suited for generating positive-going trigger pulses. The output is current-limited and protected against short-circuits. The maximum output current is 150 mA and the output pulses are stabilized at 10 V for output currents up to that value.

FUNCTIONAL DESCRIPTION (continued)

A gate resistor R_G must be connected between the output Q and the triac gate to limit the output current to the minimum required by the triac (see Figs 5 to 8). This minimizes the total supply current and the power dissipation.

Pull-down resistor R_{pd} (pin 1)

The TDA1023 includes a 1,5 kΩ pull-down resistor R_{pd} between pins 1 and 13 (V_{EE}, ground connection), intended for use with sensitive triacs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC}	max.	16 V
Supply current			
average	$I_{16(AV)}$	max.	30 mA
repetitive peak	$I_{16(RM)}$	max.	100 mA
non-repetitive peak	$I_{16(SM)}$	max.	2 A
Input voltage, all inputs	V_I	max.	16 V
Input current, CI, UR, BR, PW input	$I_{6;7;9;10}$	max.	10 mA
Voltage on R_{pd} connection	V_1	max.	16 V
Output voltage, Q, QR, V_Z output	$V_{3;8;11}$	max.	16 V
Output current			
average	$-I_{OH(AV)}$	max.	30 mA
peak, max. 300 μs	$-I_{OH(M)}$	max.	700 mA
Total power dissipation	P_{tot}	max.	500 mW
Storage temperature range	T_{stg}	−55 to + 150	°C
Operating ambient temperature range	T_{amb}	−20 to + 75	°C

CHARACTERISTICS

V_{CC} = 11 to 16 V; T_{amb} = −20 to + 75 °C unless otherwise specified

	symbol	min.	typ.	max.	unit
Supply: V_{CC} and RX (pins 14 and 16)					
Internally stabilized supply voltage at I_{16} = 10 mA	V_{CC}	12	13,7	15	V
Variation with I_{16}	$\Delta V_{CC}/\Delta I_{16}$	–	30	–	mV/mA
Supply current at $V_{16\text{-}13}$ = 11 to 16 V; I_{10} = 1 mA; f = 50 Hz; pin 11 open; $V_{6\text{-}13} > V_{7\text{-}13}$; pins 4 and 5 open	I_{16}	–	–	6	mA
pins 4 and 5 grounded	I_{16}	–	–	7,1	mA
Reference supply output V_Z (pin 11) for external temperature bridge					
Output voltage	$V_{11\text{-}13}$	–	8	–	V
Output current	$-I_{11}$	–	–	1	mA
Control and reference inputs CI, BR and UR (pins 6, 9 and 7)					
Input voltage to inhibit the output	$V_{6\text{-}13}$	–	7,6	–	V
Input current at V_I = 4 V	$I_{6;7;9}$	–	–	2	μA
Hysteresis control input HYS (pin 4)					
Hysteresis, pin 4 open	ΔV_6	9	20	40	mV
pin 4 grounded	ΔV_6	–	320	–	mV
Proportional range control input PR (pin 5)					
Proportional range, pin 5 open	ΔV_6	50	80	130	mV
pin 5 grounded	ΔV_6	–	400	–	mV
Pulse width control input PW (pin 10)					
Pulse width at $I_{10(RMS)}$ = 1 mA; f = 50 Hz	t_w	100	200	300	μs
Firing burst repetition time control input TB (pin 12)					
Firing burst repetition time, ratio to capacitor C_T	T_b/C_T	320	600	960	ms/μF
Output of reference buffer QR (pin 8)					
Output voltage at input voltage $V_{9\text{-}13}$ = 1,6 V	$V_{8\text{-}13}$	–	3,2	–	V
$V_{9\text{-}13}$ = 4,8 V	$V_{8\text{-}13}$	–	4,8	–	V
$V_{9\text{-}13}$ = 8 V	$V_{8\text{-}13}$	–	6,4	–	V

	symbol	min.	typ.	max.	unit
Output Q (pin 3)					
Output voltage HIGH at $-I_{OH}$ = 150 mA	V_{OH}	10	–	–	V
Output current HIGH	$-I_{OH}$	–	–	150	mA
Internal pull-down resistor R_{pd} (pin 1)					
Resistance to V_{EE}	R_{pd}	1	1,5	3	kΩ

Table 1. Adjustment of proportional range and hysteresis.
Combinations of resistor values giving hysteresis > ¼ proportional range.

proportional range mV	proportional range resistor R5 kΩ	minimum hysteresis mV	maximum hysteresis resistor R4 kΩ
80	open	20	open
160	3,3	40	9,1
240	1,1	60	4,3
320	0,43	80	2,7
400	0	100	1,8

Table 2. Timing capacitor C_T values.

effective d.c. value	marked a.c. specification		catalogue number*
μF	μF	V	
68	47	25	2222 016 90129
47	33	40	– – 90131
33	22	25	– 015 90102
22	15	40	– – 90101
15	10	25	– – 90099
10	6,8	40	– – 90098

* Special electrolytic capacitors recommended for use with TDA1023.

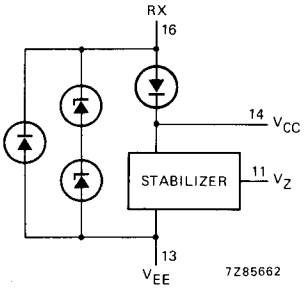


Fig. 3 Internal supply connections.

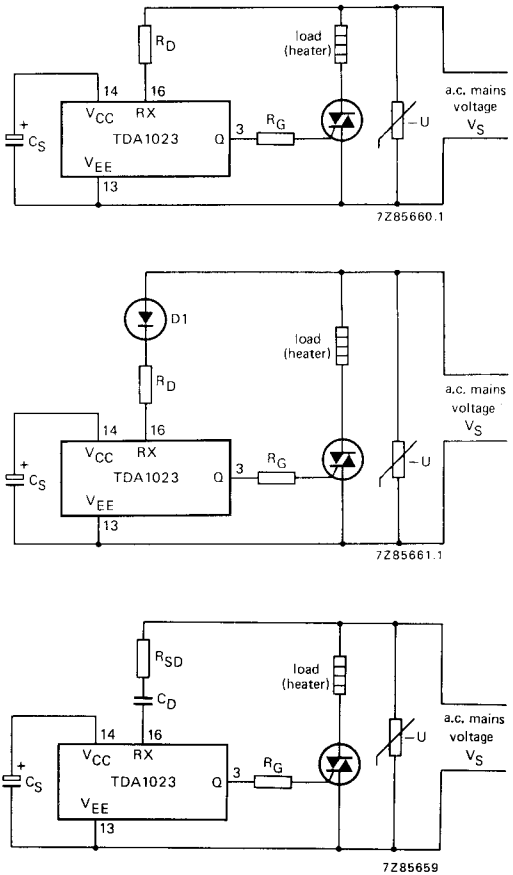


Fig. 4 Alternative supply arrangements.

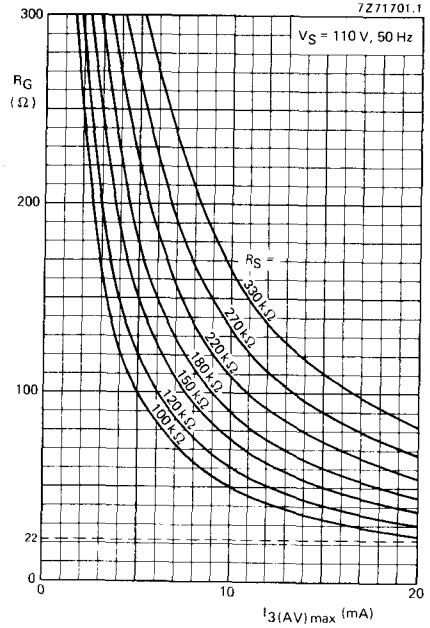


Fig. 5.

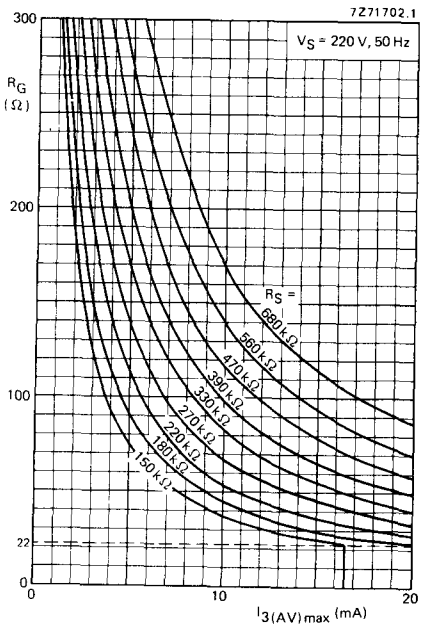


Fig. 6.

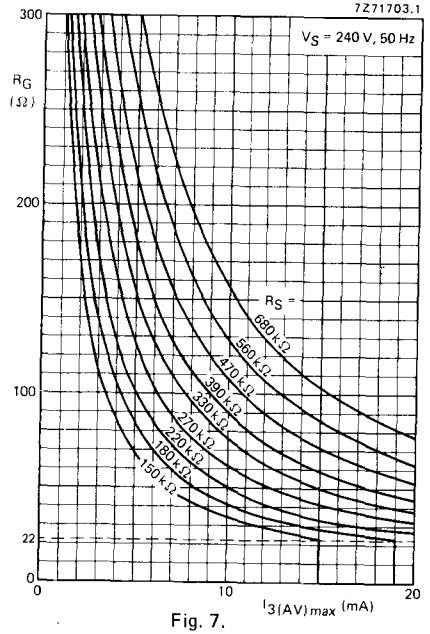


Fig. 7.

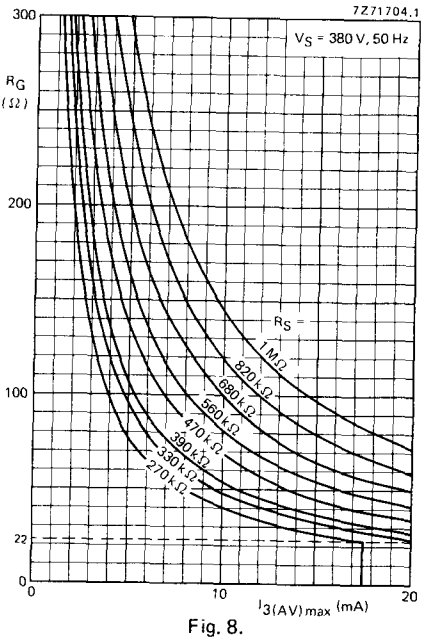


Fig. 8.

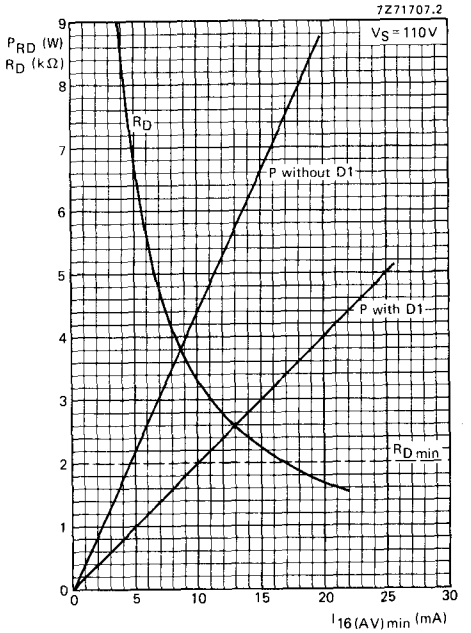


Fig. 9.

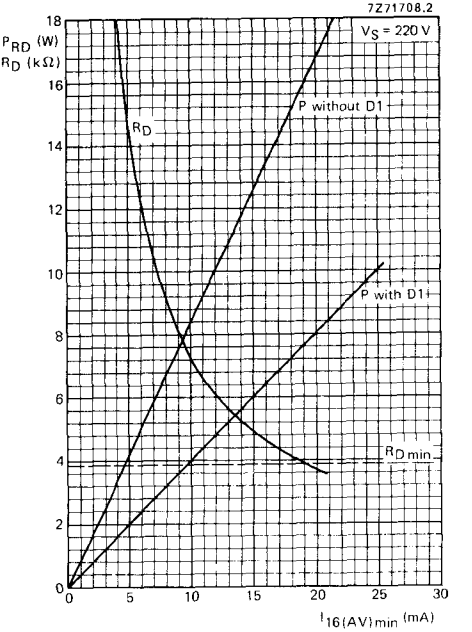


Fig. 10.

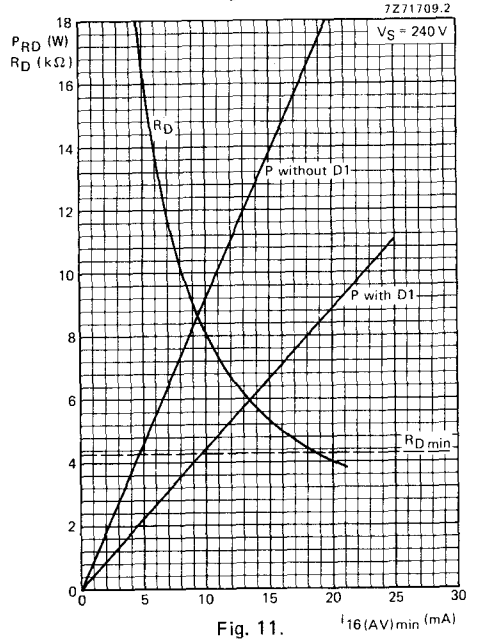


Fig. 11.

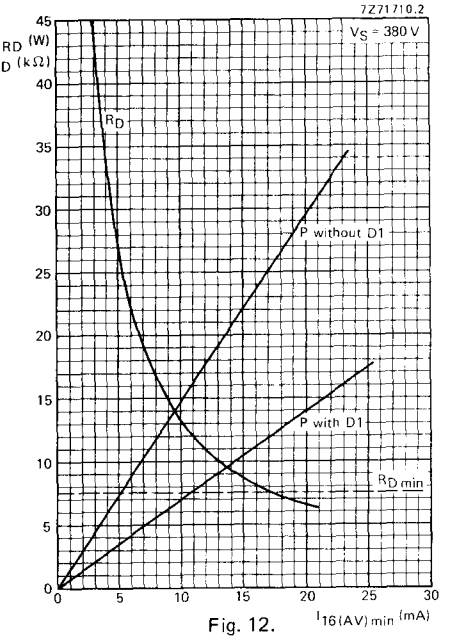


Fig. 12.

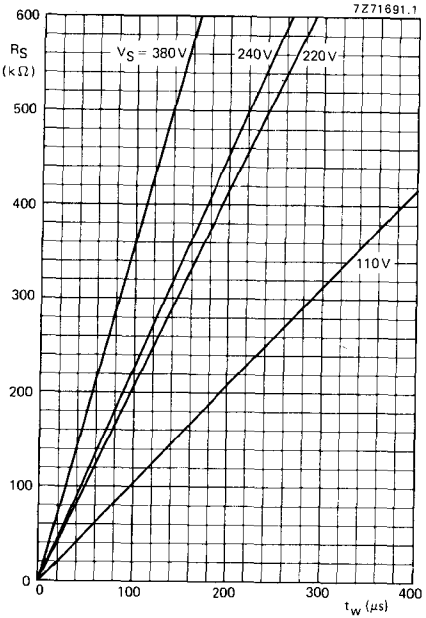


Fig. 13 *Synchronization resistor* R_S *as a function of required trigger pulse width* t_w *with mains voltage* V_S *as a parameter.*

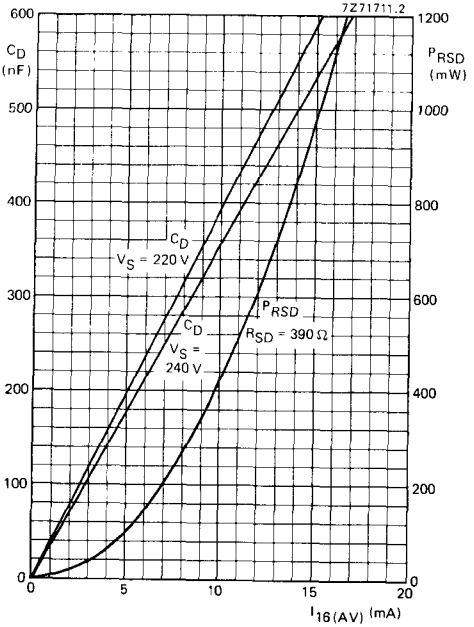


Fig. 14 Nominal value of voltage dropping capacitor C_D and power P_{RSD} dissipated in voltage dropping resistor R_{SD} as a function of the average supply current $I_{16(AV)}$ with the mains supply voltage V_S as a parameter.

APPLICATION INFORMATION

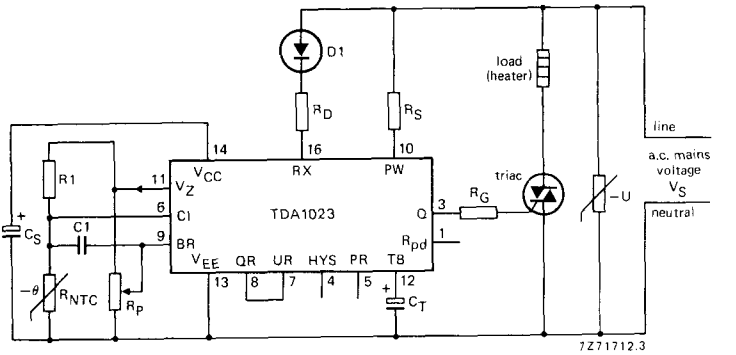


Fig. 15 The TDA1023 used in a 1200 to 2000 W heater with triac BT139. For component values see Table 3.

Conditions

Mains supply: V_S = 220 V

Temperature range = 5 to 30 °C

BT139 data: $V_{GT} < 1{,}5$ V
$I_{GT} > 70$ mA
$I_L < 60$ mA
} at T_j = 25 °C

Table 3. Temperature controller component values (see Fig. 15).

parameter	symbol	value	remarks
Trigger pulse width	t_w	75 μs	see BT139 data sheet
Synchronization resistor	R_S	180 kΩ	see Fig. 13
Gate resistor	R_G	110 Ω	see Fig. 6
Max. average gate current	$I_{3(AV)}$	4,1 mA	see Fig. 8
Hysteresis resistor	R4	n.c.	see Table 1
Proportional band resistor	R5	n.c.	see Table 1
Min. required supply current	$I_{16(AV)}$	11,1 mA	
Mains dropping resistor	R_D	6,2 kΩ	see Fig. 10
Power dissipated in R_D	P_{RD}	4,6 W	see Fig. 10
Timing capacitor (eff. value)	C_T	68 μF	see Table 2
Voltage dependent resistor	VDR	250 V a.c.	cat. no. 2322 593 62512
Rectifier diode	D1	BYW56	
Resistor to pin 11	R1	18,7 kΩ	1% tolerance
NTC thermistor (at 25 °C)	R_{NTC}	22 kΩ	B = 4200 K cat. no. 2322 642 12223
Potentiometer	R_P	22 kΩ	
Capacitor between pins 6 and 9	C1	47 nF	
Smoothing capacitor	C_S	220 μF; 16 V	
If R_D and D1 are replaced by C_D and R_{SD}			
Mains dropping capacitor	C_D	470 nF	
Series dropping resistor	R_{SD}	390 Ω	see Fig. 14
Power dissipated in R_{SD}	P_{RSD}	0,6 W	
Voltage dependent resistor	VDR	250 V a.c.	cat. no. 2322 594 62512

Notes

1. ON/OFF control: pin 12 connected to pin 13.
2. If translation circuit is not required: slider of R_P to pin 7; pin 8 open; pin 9 connected to pin 11.

APPLICATION INFORMATION SUPPLIED ON REQUEST

ON-OFF TRIAC TRIGGERING CIRCUIT

GENERAL DESCRIPTION

The TDA1024 is a bipolar integrated circuit delivering positive pulses for triggering a triac or a thyristor. It is primarily intended for use as a static switch to replace mechanical thermostats that switch resistive loads, such as:

- central heating installations
- washing machine heaters
- water heaters
- smoothing irons

The TDA1024 provides its own d.c. supply and will supply an external circuit, e.g. a temperature sensing bridge. The circuit complies with the regulations on radio interference and mains distortion.

Its main features are:

- adjustable trigger pulse width
- adjustable hysteresis
- supplied from the mains
- provides supply for external temperature bridge
- protected inputs and output
- low supply current, low dissipation

QUICK REFERENCE DATA

Supply voltage (d.c.) (internally derived from mains voltage)	V_{CC}	typ.	6,5 V
Supply current (average value, unloaded)	$I_{RX(AV)}$	max.	1,8 mA
Output current HIGH	$-I_{OH}$*	max.	100 mA
Output pulse width	t_w	typ.	195 μs
Power dissipation (unloaded)	P	typ.	12 mW
Operating ambient temperature range	T_{amb}		−20 to +80 °C

* Negative current is defined as conventional current flow out of a device. A negative output current is suited for positive triac triggering.

PACKAGE OUTLINE

8-lead DIL; plastic (SOT-97A).

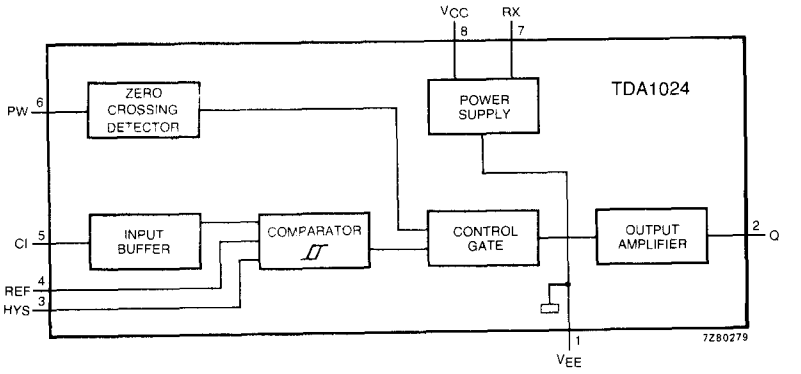


Fig. 1 Block diagram.

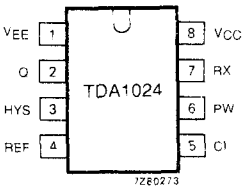


Fig. 2 Pinning diagram.

PINNING

1	V_{EE}	ground
2	Q	output
3	HYS	hysteresis control input
4	REF	reference input
5	CI	control input
6	PW	pulse width control input
7	RX	external resistor
8	V_{CC}	positive supply

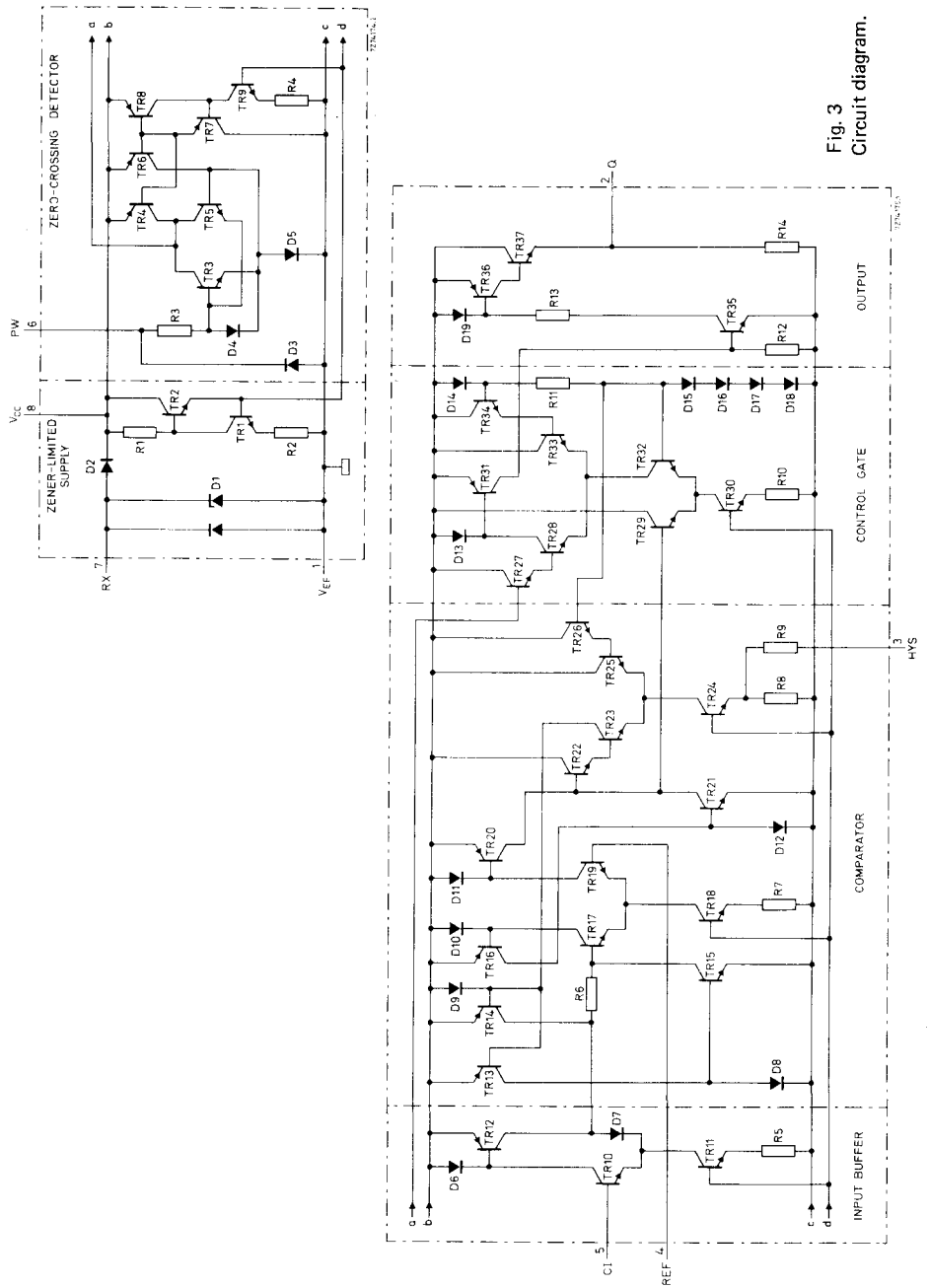


Fig. 3
Circuit diagram.

FUNCTIONAL DESCRIPTION

The TDA1024 generates positive-going output pulses to trigger a triac. These trigger pulses coincide with the zero crossings of the mains voltage. This minimizes r.f. interference and transients on the mains supply.

Supply: V_{CC} and RX (pins 8 and 7)

The TDA1024 may be supplied by an external d.c. power supply connected to V_{CC} (pin 8), but usually it is supplied directly from the mains voltage. For this purpose the circuit contains a stabilizer diode between RX and V_{EE} that limits the d.c. supply voltage (see Fig. 4). An external resistor R_D has to be connected from the mains to RX (pin 7); V_{EE} is connected to the neutral line (see Fig. 5a). A smoothing capacitor C_S has to be connected between V_{CC} and V_{EE}.

During the positive half of the mains cycles the current through external voltage-dropping resistor R_D charges the external smoothing capacitor C_S up to the stabilizing voltage of the internal stabilizer diodes. R_D should be chosen such that it can supply the current I_{CC} for the TDA1024 itself plus the average output current $-I_{Q(AV)}$, and recharge the smoothing capacitor C_S. Any excess current is bypassed by the internal stabilizer diode. Note that the maximum rated supply current must not be exceeded.

During the negative half of the mains cycles external smoothing capacitor C_S supplies the circuit. Its capacitance must be high enough to maintain the supply voltage above 5 V, the minimum specified limit (see Fig. 10).

Dissipation in resistor R_D is halved by connecting a diode in series (see Figs 5b and 11).

A further reduction of dissipation is possible by using a high-quality voltage-dropping capacitor C_D in series with a resistor R_{SD} (see Figs 5c and 12).

A suitable VDR connected across the mains provides protection of the TDA1024 and of the triac against mains-borne transients.

Control and reference inputs CI and REF (pins 5 and 4)

The TDA1024 produces output pulses when the CI input is at a higher potential than the REF input. For power control as a function of temperature the inputs may be connected as shown in Fig. 14.

An input buffer circuit at the CI input gives a high input impedance and a low output impedance. This makes the hysteresis of the circuit independent of the input voltage.

Hysteresis control input HYS (pin 3)

With the hysteresis control input HYS open the device has a built-in hysteresis of 20 mV. For temperature control this corresponds with a temperature difference of 0,25 K.

Hysteresis is increased to 300 mV, corresponding with a temperature difference of 4 K, by grounding HYS. Intermediate values are obtained by connecting HYS to ground via a resistor.

Pulse width control input PW (pin 6)

The output pulse width may be adjusted to the value required for the triac by choosing the value of the external synchronization resistor R_S between the pulse width control input PW and the a.c. mains. The pulse width is inversely proportional to the input current (see Fig. 13).

Output Q (pin 2)

Since the circuit has an open-emitter output, it is capable of sourcing current, i.e. supplying a current out of the output. Therefore it is especially suited for generating positive-going trigger pulses. The output is current-limited and protected against short-circuits. The maximum output current is 100 mA and the output pulses are stabilized at 4 V for output currents up to that value.

FUNCTIONAL DESCRIPTION (continued)

Output Q (pin 2) (continued)

A gate resistor R_G must be connected between the output Q and the triac gate to limit the output current to the minimum required by the triac (see Figs 6 to 9). This minimizes the total supply current and the power dissipation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{CC}	max.	8 V
Supply current			
average	$I_{RX(AV)}$	max.	30 mA
repetitive peak	$I_{RX(RM)}$	max.	80 mA
non-repetitive peak ($t < 50\ \mu s$)	$I_{RX(SM)}$	max.	2 A
Input voltage (all inputs)	V_I	max.	8 V
Input current (CI, REF, PW)	I_{CI}; I_{REF}; $\pm I_{PW}$	max.	10 mA
Output voltage HIGH	V_Q	max.	8 V
Output current			
average	$-I_{OH(AV)}$	max.	30 mA
peak, max. 300 μs	$-I_{OH(M)}$	max.	400 mA
Total power dissipation	P_{tot}	max.	225 mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +80	°C

CHARACTERISTICS

V_{CC} = 5 to 8 V; T_{amb} = −20 to +80 °C unless otherwise specified.

	symbol	min.	typ.	max.	unit
Supply: V_{CC} and RX (pins 8 and 7)					
Internally stabilized supply voltage at $I_{RX(AV)}$ = 10 mA	V_{CC}	5,5	6,5	7,5	V
variation with I_{RX}	$\Delta V_{CC}/\Delta I_{RX}$	–	15	–	mV/mA
Supply current at V_{CC} = 5,5 V; unloaded; f = 50 Hz; $V_{CI} > V_{REF}$ pin 3 open (minimum hysteresis)	$I_{RX(AV)}$	–	–	1,8	mA
Supply current increase pin 3 grounded (maximum hysteresis)	$\Delta I_{RX(AV)}$	–	1,4	–	mA
Control and reference inputs CI and REF (pins 5 and 4)					
Input current, CI input, at $V_{CI} > V_{REF}$	I_{CI}	–	–	5	μA
Input current, REF input, at $V_{REF} > V_{CI}$	I_{REF}	–	–	5	μA
Hysteresis control input HYS (pin 3)					
Hysteresis, pin 3 open (minimum hysteresis)	ΔV_{CI-REF}	10	20	30	mV
pin 3 grounded (maximum hysteresis)	ΔV_{CI-REF}	150	300	500	mV
Pulse width control input PW (pin 6)					
Pulse width at $I_{PW(RMS)}$ = 1 mA; V_{CC} = 5,5 V; f = 50 Hz	t_w	130	195	265	μs
Output Q (pin 2)					
Output voltage HIGH at $-I_{OH}$ = 100 mA	V_{OH}	4	–	–	V
at $-I_{OH}$ = 1 mA	V_{OH}	1	–	–	V
Output current HIGH	$-I_{OH}$	–	–	100	mA

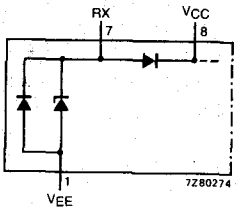
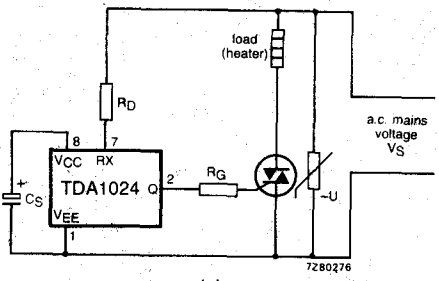
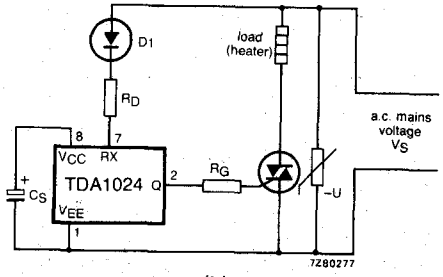


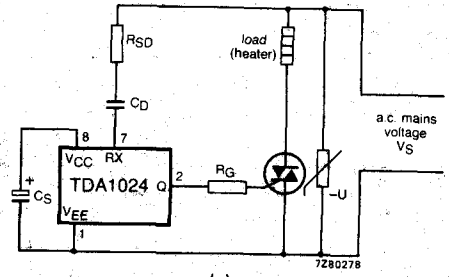
Fig. 4 Internal supply connections.



(a)



(b)



(c)

Fig. 5 Alternative supply arrangements.

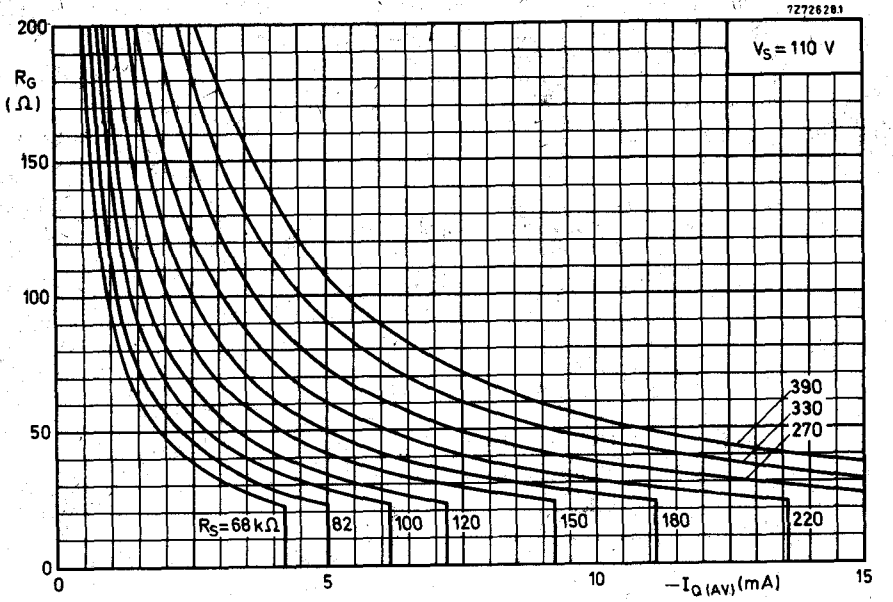

7Z72628.1
V_S = 110 V
R_G (Ω)
200
150
100
50
0
0
5
10
15
$-I_{Q\,(AV)}$ (mA)
R_S = 68 kΩ
82
100
120
150
180
220
390
330
270

Fig. 6.

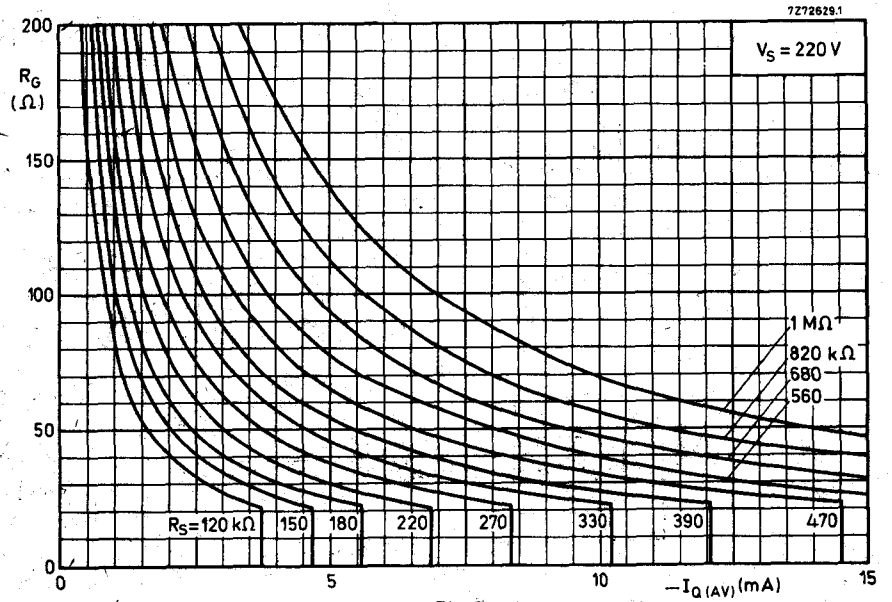

7Z72629.1
V_S = 220 V
R_G (Ω)
200
150
100
50
0
0
5
10
15
$-I_{Q\,(AV)}$ (mA)
R_S = 120 kΩ
150
180
220
270
330
390
470
1 MΩ
820 kΩ
680
560

Fig. 7.

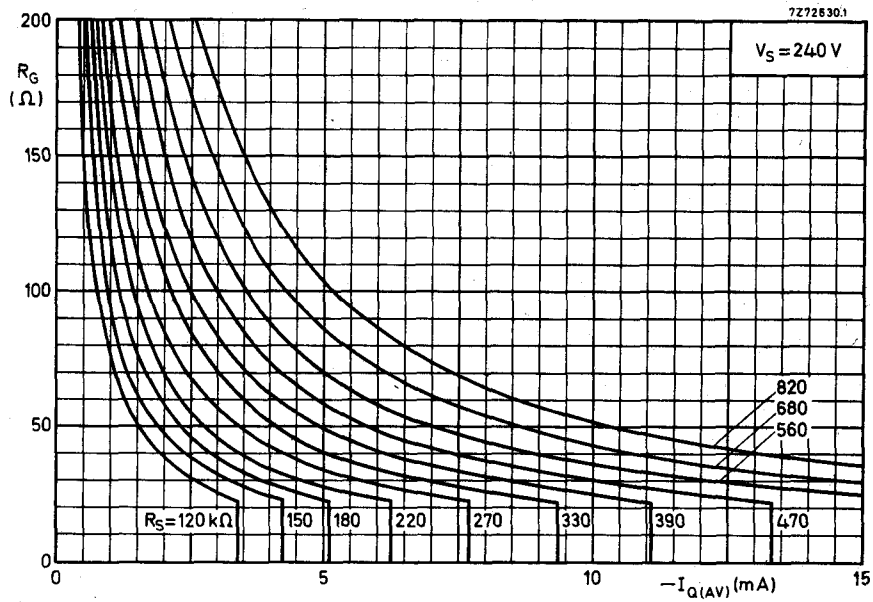

7Z72630.1
$V_S = 240$ V
R_G (Ω)
200
150
100
50
0
R_S=120 kΩ
150
180
220
270
330
390
470
820
680
560
0
5
10
15
$-I_{Q(AV)}$ (mA)

Fig. 8.

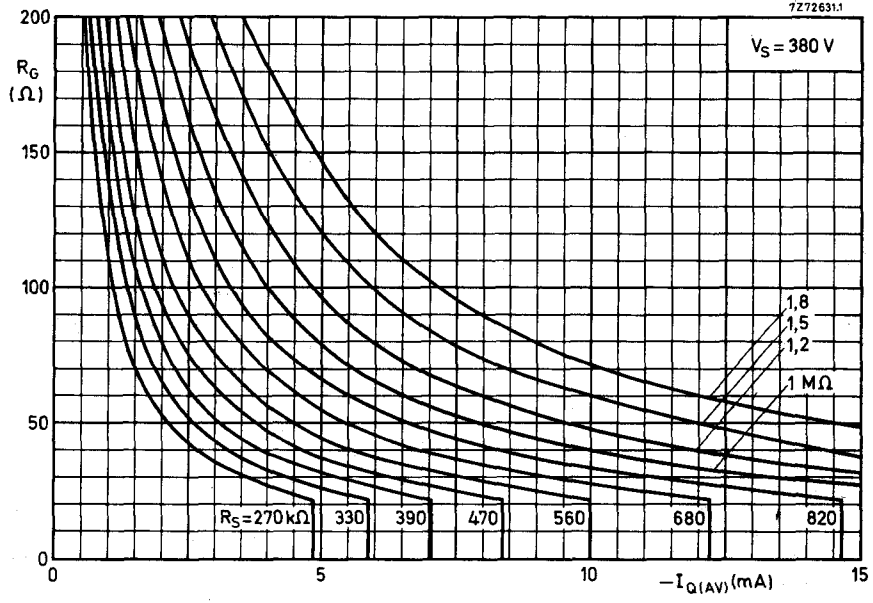

7Z72631.1
$V_S = 380$ V
R_G (Ω)
200
150
100
50
0
R_S=270 kΩ
330
390
470
560
680
820
1,8
1,5
1,2
1 MΩ
0
5
10
15
$-I_{Q(AV)}$ (mA)

Fig. 9.

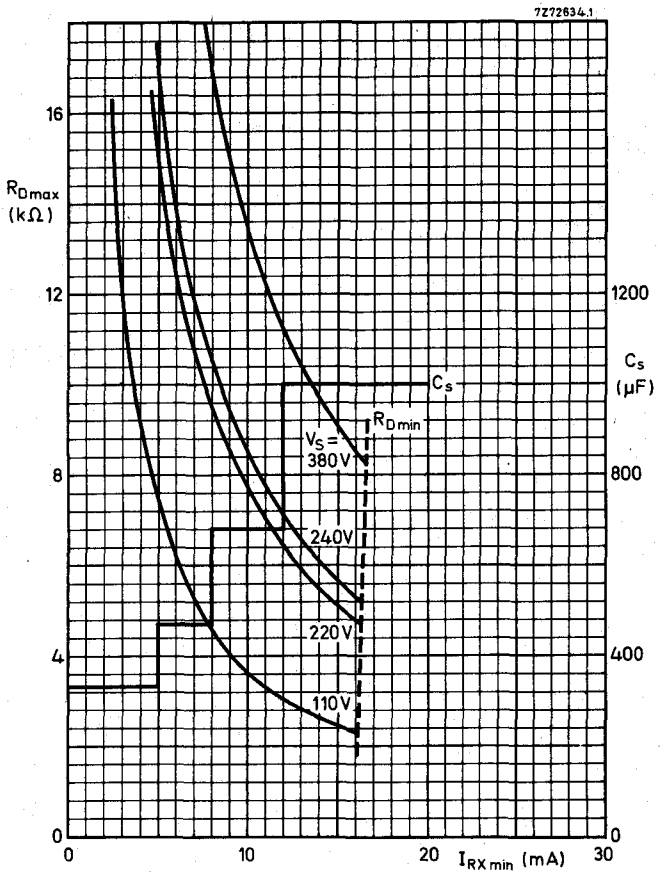


Fig. 10 Maximum value of voltage-dropping resistor R_D as a function of minimum value of the current into RX with the mains supply voltage V_S as a parameter for the supply arrangements of Figs 5a and 5b, and recommended value of smoothing capacitor C_S as a function of the current into RX for all three supply arrangements of Fig. 5. When V_{CC} is used to supply external circuitry such as a temperature-sensing bridge, the current required by that external circuitry should be added to I_{RXmin}.

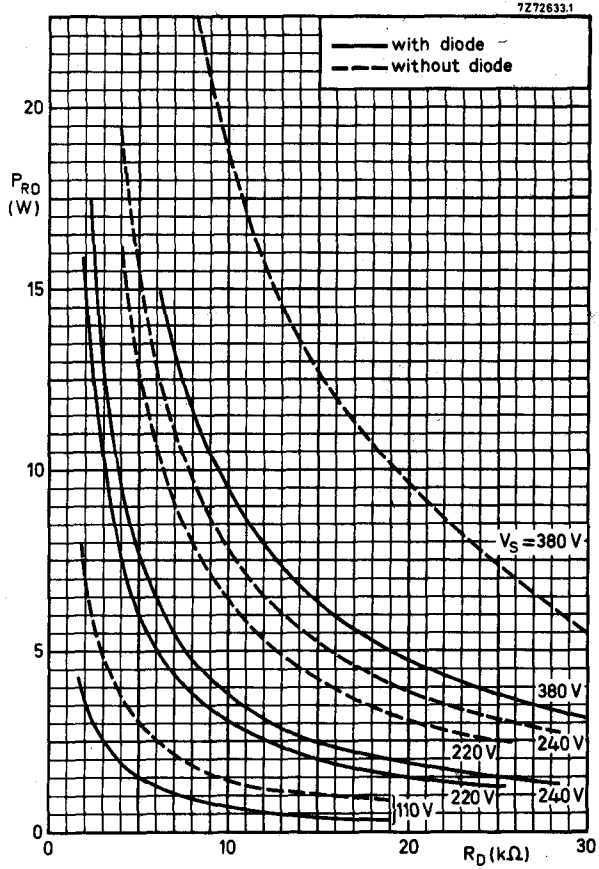


Fig. 11 Power dissipated in voltage-dropping resistor R_D as a function of its value with the mains supply voltage V_S as a parameter, for the supply arrangements of Figs 5a and 5b.

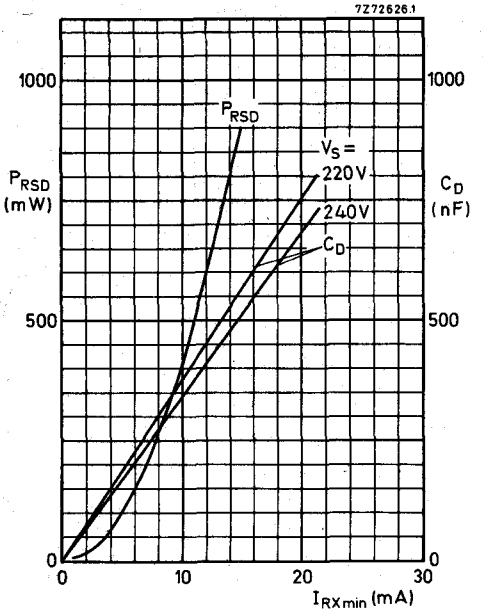


Fig. 12 Power dissipated in voltage-dropping resistor R_{SD} and dropping capacitor C_D as a function of the minimum current into RX with the mains supply voltage V_S as a parameter, for the supply arrangement of Fig. 5c. When V_{CC} is used to supply external circuitry such as a temperature-sensing bridge, the current required by that external circuitry should be added to I_{RXmin}.

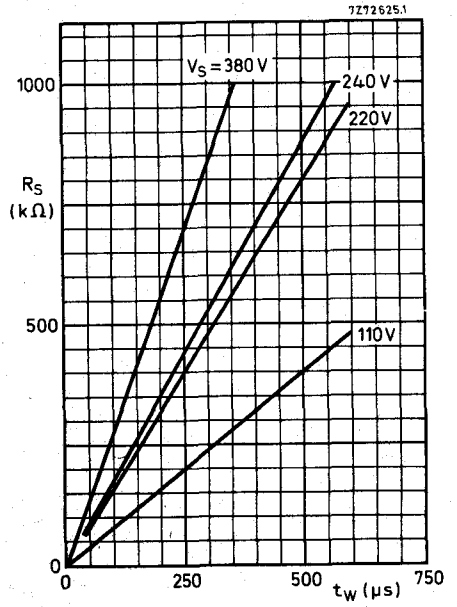


Fig. 13 Synchronization resistor R_S as a function of required trigger pulse width t_W with mains supply voltage V_S as a parameter.

APPLICATION INFORMATION

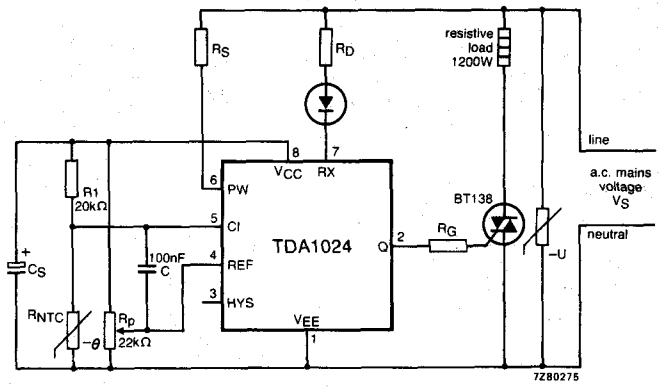


Fig. 14 Typical application of the TDA1024 in a 1200 W thermostat covering the temperature range 5 to 30 °C. For component values see Table 1.

Conditions

Mains supply voltage $V_{S(RMS)}$ = 220 V

Temperature range: 5 to 30 °C

BT138 data: $V_{GT} < 1{,}5$ V, $I_{GT} > 70$ mA, $I_L < 60$ mA } at T_j = 25 °C

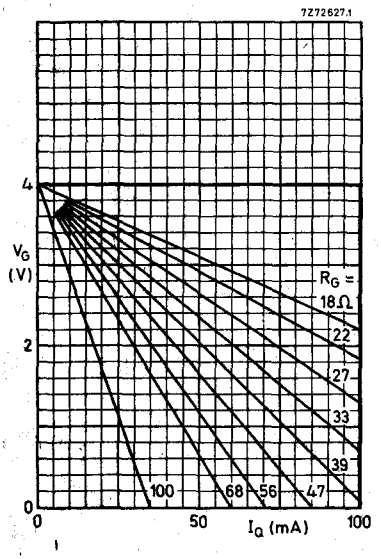
Table 1

Temperature controller component values (see Fig. 14)

parameter	symbol	value	remarks
Trigger pulse width	t_W	105 µs	see BT138 data sheet
Synchronization resistor	R_S	180 kΩ	see Fig. 13
Gate resistor	R_G	33 Ω	see Fig. 7
Average output current	$I_{Q(AV)}$	3,7 mA	
Min. required supply current	$I_{RX(AV)}$	6,5 mA	
Voltage-dropping resistor	R_D	10 kΩ	see Fig. 10
Power dissipated in R_D	P_{RD}	3,2 W	see Fig. 11
Voltage dependent resistor	VDR	250 V a.c.	cat. no. 2322 593 62512
Rectifier diode	D1	BYW56	
NTC thermistor (at 25 °C)	R_{NTC}	22 kΩ	B = 4200 K cat. no. 2322 642 12223
Smoothing capacitor	C_S	220 µF; 16 V	

If R_D and D1 are replaced by C_D and R_{SD}

Voltage-dropping capacitor	C_D	270 nF	
Series dropping resistor	R_{SD}	390 Ω	
Power dissipated in R_{SD}	P_{RSD}	190 mW	
Voltage dependent resistor	VDR	250 V a.c.	cat. no. 2322 594 62512



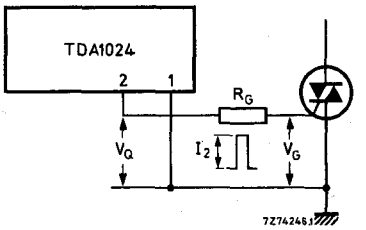


Fig. 15 Gate voltage (V_G) as a function of trigger current (I_Q) with gate resistor (R_G) load lines.

TOUCH-CONTROLLED LAMP DIMMER CIRCUIT

GENERAL DESCRIPTION

The TEA1010 is a bipolar integrated circuit for switching and regulating lamps and other loads with a minimum of external components. It provides ON/OFF switching and a physiological power regulation (equal brightness steps). It is suited for touch plates and for switches, and may combine local and remote control. It produces negative pulses to drive a triac. The circuit is suited for resistive and for inductive loads, i.e. it is not only suited for dimming lamps but also for regulating motors in fans, vacuum cleaners, etc.

The TEA 1010 and TEA1010T switch on at the maximum brightness level upon a brief touch of the contacts.

The circuits feature:

- Alternative ON/OFF switching by a brief touch of one or both contacts.
- ON switching at minimum brightness by a long touch of one or both contacts.
- Gradual change to maximum brightness during a long touch of the UP contact.
- Gradual change to minimum brightness during a long touch of the DOWN contact.
- No action during a long touch of both contacts in the ON state.

QUICK REFERENCE DATA

Supply voltage, d.c. (derived from mains voltage)	V_{CC}	typ.	15 V
Supply current	I_{CC}	typ.	1 mA
Output current	I_O	max.	100 mA
Firing phase range	φ	typ.	30^o to 140^o
Time to change from minimum to maximum brightness, or vice versa	t_v	typ.	3,8 s
Power dissipation in the ON state	P	typ.	19 mW
Operating ambient temperature range	T_{amb}		0 to + 85 °C

PACKAGE OUTLINE

TEA1010 : 8-lead DIL; plastic (SOT-97C2).
TEA1010T: 8-lead mini-pack; plastic (SO-8; SOT-96AC1).

FUNCTIONAL DESCRIPTION

The TEA1010 generates negative output pulses to trigger a triac. These output pulses are phase shifted with respect to the mains voltage. The amount of phase shift is determined by the difference between the initial states of two 7-bit counters. Both counters are driven by the same clock pulse generator. One of the counters is preset to a number determined by the required phase angle. The higher the required brightness, the smaller the required phase angle, the lower the number to which the counter is preset. The relation between brightness and preset number has been chosen so that almost equal brightness steps are obtained (physiological control). The minimum phase shift corresponds with 32 clock pulses and the maximum with 160.

Upwards and downwards regulation inputs UP and DN (pins 7 and 6)

At 50 Hz mains frequency the device ignores signals with a duration of less than 80 ms and signals with a duration of 80 to 320 ms are accepted as brief commands, these cause the circuit to switch on and off alternatively. Signals that last longer than 320 ms are interpreted as long commands. A long command via the UP input causes the output phase angle to decrease, i.e. the brightness to increase gradually; a long command via the DN input has the opposite effect. A long signal on both inputs will switch on the lamp at minimum brightness. If the lamp is already on, a long signal on both inputs will have no effect.

The UP and DN inputs may be activated by touch plates or by switches. For the input arrangements see Fig. 2.

Slave input SLV (pin 2)

The SLV input operates in the same manner as the UP and DN inputs, but with a two-wire connection, ideal for remote control. The SLV input is only suited for switches. For the arrangement see Fig. 3. If the SLV input is not used it must be connected to the load via a 1,5 MΩ resistor (see Fig. 4).

Oscillator RC pin OSC (pin 1)

The frequency of the clock pulse generator is determined by an external resistor and capacitor, both connected to the OSC terminal (see Fig. 4). The generator switches at levels equal to 1/6 and 1/2 of the difference between the injector voltage V_{inj} and the supply voltage V_{CC}. The clock pulse period is about 50 μs.

Output Q (pin 3)

Since the circuit has an open-collector output, it is capable of sinking current, i.e. drawing a current into the output. Therefore it is especially suitable for delivering negative trigger pulses.

The maximum output current is 100 mA. A gate resistor R_G must be connected between the output Q and the triac gate to limit the output current to the minimum required by the triac (see Fig. 4). This minimizes the total supply current and the power dissipation.

A negative-going trigger pulse is generated at the output after every zero crossing of the mains voltage. The output pulse has a maximum duration of one clock pulse period, i.e. 50 μs. To reduce the power dissipation the output pulse is terminated as soon as the triac has switched on.

Supply V_{CC} and V_{EE} (pins 8 and 4)

The TEA1010 is supplied from the a.c. mains via a capacitor C_D and a diode to V_{EE}; V_{CC} is connected to the line (see Fig. 4). A smoothing capacitor C_S has to be connected between V_{CC} and V_{EE}. The circuit contains a string of stabilizer diodes between V_{CC} and V_{EE} that limit the d.c. supply voltage.

During the positive half of the mains cycles the current through external voltage dropping capacitor C_D charges the external smoothing capacitor C_S up to the stabilizing voltage of the internal stabilizer diodes. C_D should be chosen such that it can supply the current I_{CC} for the TEA1010 itself plus the average output current $I_{3(AV)}$, and recharge the smoothing capacitor C_S.

Any excess current is bypassed by the internal stabilizer diodes. Note that the maximum rated supply current must not be exceeded.

During the negative half of the mains cycles external smoothing capacitor C_S supplies the circuit. Its capacitance must be high enough to maintain the supply voltage above the minimum specified limit.

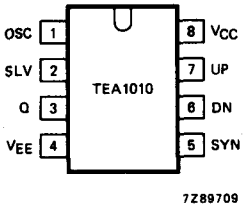
A supply voltage at V_{EE} that is negative with respect to V_{CC} and the line is developed at the V_{EE} pin. Note that in the characteristics the voltages are mainly measured with respect to V_{EE} and not with respect to V_{CC} and the line.

The circuit has an internal power-on reset, which forces the circuit into the OFF state.

Synchronization input SYN (pin 5)

The connection to the SYN input should be short and must be decoupled via a capacitor to V_{CC} (pin 8).

PINNING



1	OSC	oscillator (RC)
2	SLV	slave input
3	Q	output
4	V_{EE}	common
5	SYN	synchronization input
6	DN	downward regulation input
7	UP	upward regulation input
8	V_{CC}	positive supply

Fig. 1 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range, d.c.	V_{CC}	−0,5 to + 18	V
Supply current, d.c.	I_{CC}	max. 20	mA
peak, max. 10 μs	I_{CCM}	max. 0,5	A
Input voltage range, all inputs	V_I	−0,5 to + 18	V
Input current, all inputs	$\pm I_I$	max. 20	mA
Output voltage range	V_O	−0,5 to + 18	V
Output current range	I_O	−20 to + 150	mA
Power dissipation	P_{tot}	max. 250	mW
Storage temperature range	T_{stg}	−55 to + 125	°C
Operating ambient temperature range	T_{amb}	0 to + 85	°C

CHARACTERISTICS

V_{CC} = 5 to 18 V; T_{amb} = 0 to + 85 °C

parameter	symbol	min.	typ.	max.	unit
Supply V_{CC} (pin 8)					
Internally stabilized supply voltage, at I_{CC} = 1,5 to 20 mA	V_{CC}	13,3	15	16,8	V
Supply current at V_{CC} = 15 V, unloaded,					
OFF state	I_{CC}	–	1	1,2	mA
ON state	I_{CC}	–	1,25	1,5	mA
Power dissipation, unloaded,					
OFF state	P	–	15	–	mW
ON state	P	–	19	25	mW
Thermal resistance					
TEA1010	$R_{th\ j\text{-}a}$	–	162	–	K/W
TEA1010T (note 1)	$R_{th\ j\text{-}a}$	–	140	–	K/W
TEA1010T (note 2)	$R_{th\ j\text{-}a}$	–	220	–	K/W
Power-on reset threshold voltage	V_{CCpor}	–	–	4,8	V
Oscillator RC pin OSC (pin 1)					
Injector voltage	V_{inj}	550	–	700	mV
Synchronization input SYN (pin 5)					
Input current (r.m.s. value)	$I_{5(rms)}$	3	–	–	μA
Upwards and downwards regulation inputs UP and DN (pins 7 and 6)					
Input voltage	$V_{6\text{-}4}$; $V_{7\text{-}4}$	1	–	–	V
Input current	$-I_6$; $-I_7$	–	3 $I_{5(rms)}$	–	μA
Slave input SLV (pin 2)					
Input current	$\pm I_2$	10	–	–	μA
Output Q (pin 3)					
Output current	I_3	–	–	100	mA

Notes

1. TEA1010T mounted on a ceramic substrate of 50 x 50 x 0,7 mm.
2. TEA1010T mounted on a printed-circuit board of 50 x 50 x 1,5 mm.

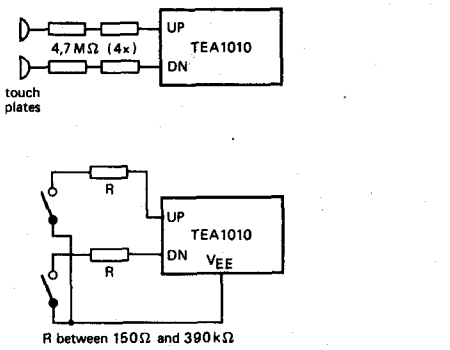


Fig. 2 Alternative arrangements for the UP and DN inputs.

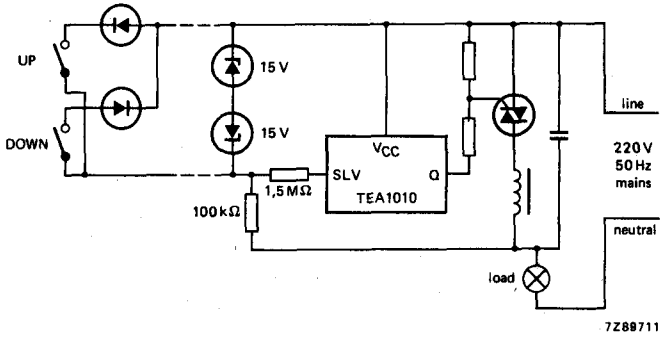
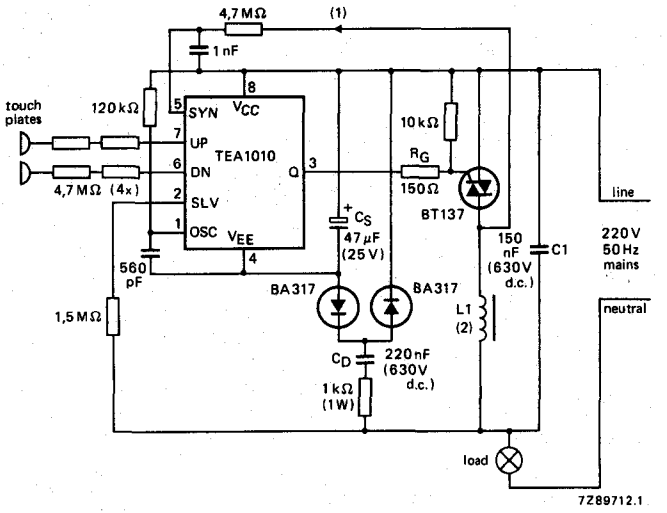


Fig. 3 SLV input arrangement.

APPLICATION INFORMATION



(1) The connection to the SYN input should be short and must be decoupled near to pins 5 and 8.
(2) For example, Vakuumschmelze FD 2.5 1N1 KN.

Fig. 4 Touch-controlled lamp dimmer circuit for max. 450 W. L1 and C1 form a radio-frequency interference filter with a quality factor Q of less than 1. This filter is necessary to satisfy the regulations of C.I.S.P.R. and V.D.E.

APPLICATION INFORMATION AVAILABLE ON REQUEST

TOUCH-CONTROLLED LAMP DIMMER CIRCUIT

GENERAL DESCRIPTION

The TEA1058 is a bipolar integrated circuit for switching and regulating lamps and other loads with a minimum of external components. It provides ON/OFF switching and a physiological power regulation (equal brightness steps). It is suited for touch plates and for switches, and may combine local and remote control. It produces negative pulses to drive a triac. The circuit is suited for resistive and for inductive loads, i.e. it is not only suited for dimming lamps but also for regulating motors in fans, vacuum cleaners, etc.

The TEA1058 and TEA1058T switch on at the level at which they were switched off.

The circuits feature:
- Alternative ON/OFF switching by a brief touch of one or both contacts.
- ON switching at previous brightness by a long touch of one or both contacts.
- Gradual change to maximum brightness during a long touch of the UP contact.
- Gradual change to minimum brightness during a long touch of the DOWN contact.
- No action during a long touch of both contacts in the ON state.

QUICK REFERENCE DATA

Supply voltage, d.c. (derived from mains voltage)	V_{CC}	typ.	15 V
Supply current	I_{CC}	typ.	1 mA
Output current	I_O	max.	100 mA
Firing phase range	φ	typ.	30° to 140°
Time to change from minimum to maximum brightness, or vice versa	t_v	typ.	3,8 s
Power dissipation in the ON state	P	typ.	19 mW
Operating ambient temperature range	T_{amb}		0 to + 85 °C

PACKAGE OUTLINE

TEA1058 : 8-lead DIL; plastic (SOT-97C2).
TEA1058T: 8-lead mini-pack; plastic (SO-8; SOT-96AC1).

FUNCTIONAL DESCRIPTION

The TEA1058 generates negative output pulses to trigger a triac. These output pulses are phase shifted with respect to the mains voltage. The amount of phase shift is determined by the difference between the initial states of two 7-bit counters. Both counters are driven by the same clock pulse generator. One of the counters is preset to a number determined by the required phase angle. The higher the required brightness, the smaller the required phase angle, the lower the number to which the counter is preset. The relation between brightness and preset number has been chosen so that almost equal brightness steps are obtained (physiological control). The minimum phase shift corresponds with 32 clock pulses and the maximum with 160.

Upwards and downwards regulation inputs UP and DN (pins 7 and 6)

At 50 Hz mains frequency the device ignores signals with a duration of less than 80 ms and signals with a duration of 80 to 320 ms are accepted as brief commands, these cause the circuit to switch on and off alternatively. Signals that last longer than 320 ms are interpreted as long commands. A long command via the UP input causes the output phase angle to decrease, i.e. the brightness to increase gradually; a long command via the DN input has the opposite effect. A long signal on both inputs will switch on the lamp at previous brightness. If the lamp is already on, a long signal on both inputs will have no effect.

The UP and DN inputs may be activated by touch plates or by switches. For the input arrangements see Fig. 2.

Slave input SLV (pin 2)

The SLV input operates in the same manner as the UP and DN inputs, but with a two-wire connection, ideal for remote control. The SLV input is only suited for switches. For the arrangement see Fig. 3. If the SLV input is not used it must be connected to the load via a 1,5 MΩ resistor (see Fig. 4).

Oscillator RC pin OSC (pin 1)

The frequency of the clock pulse generator is determined by an external resistor and capacitor, both connected to the OSC terminal (see Fig. 4). The generator switches at levels equal to 1/6 and 1/2 of the difference between the injector voltage V_{inj} and the supply voltage V_{CC}. The clock pulse period is about 50 μs.

Output Q (pin 3)

Since the circuit has an open-collector output, it is capable of sinking current, i.e. drawing a current into the output. Therefore it is especially suitable for delivering negative trigger pulses.

The maximum output current is 100 mA. A gate resistor R_G must be connected between the output Q and the triac gate to limit the output current to the minimum required by the triac (see Fig. 4). This minimizes the total supply current and the power dissipation.

A negative-going trigger pulse is generated at the output after every zero crossing of the mains voltage. The output pulse has a maximum duration of one clock pulse period, i.e. 50 μs. To reduce the power dissipation the output pulse is terminated as soon as the triac has switched on.

Supply V_{CC} and V_{EE} (pins 8 and 4)

The TEA1058 is supplied from the a.c. mains via a capacitor C_D and a diode to V_{EE}; V_{CC} is connected to the line (see Fig. 4). A smoothing capacitor C_S has to be connected between V_{CC} and V_{EE}. The circuit contains a string of stabilizer diodes between V_{CC} and V_{EE} that limit the d.c. supply voltage.

During the positive half of the mains cycles the current through external voltage dropping capacitor C_D charges the external smoothing capacitor C_S up to the stabilizing voltage of the internal stabilizer diodes. C_D should be chosen such that it can supply the current I_{CC} for the TEA1058 itself plus the average output current $I_{3(AV)}$, and recharge the smoothing capacitor C_S.

Any excess current is bypassed by the internal stabilizer diodes. Note that the maximum rated supply current must not be exceeded.

During the negative half of the mains cycles external smoothing capacitor C_S supplies the circuit. Its capacitance must be high enough to maintain the supply voltage above the minimum specified limit.

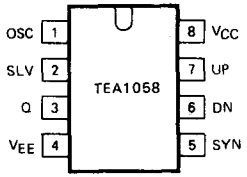
A supply voltage at V_{EE} that is negative with respect to V_{CC} and the line is developed at the V_{EE} pin. Note that in the characteristics the voltages are mainly measured with respect to V_{EE} and not with respect to V_{CC} and the line.

The circuit has an internal power-on reset, which resets the brightness to minimum and forces the circuit into the OFF state.

Synchronization input SYN (pin 5)

The connection to the SYN input should be short and must be decoupled via a capacitor to V_{CC} (pin 8).

PINNING



1	OSC	oscillator (RC)
2	SLV	slave input
3	Q	output
4	V_{EE}	common
5	SYN	synchronization input
6	DN	downward regulation input
7	UP	upward regulation input
8	V_{CC}	positive supply

Fig. 1 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range, d.c.	V_{CC}	−0,5 to + 18	V
Supply current, d.c.	I_{CC}	max. 20	mA
peak, max. 10 μs	I_{CCM}	max. 0,5	A
Input voltage range, all inputs	V_I	−0,5 to + 18	V
Input current, all inputs	$\pm I_I$	max. 20	mA
Output voltage range	V_O	−0,5 to + 18	V
Output current range	I_O	−20 to + 150	mA
Power dissipation	P_{tot}	max. 250	mW
Storage temperature range	T_{stg}	−55 to + 125	°C
Operating ambient temperature range	T_{amb}	0 to + 85	°C

CHARACTERISTICS

V_{CC} = 5 to 18 V; T_{amb} = 0 to + 85 °C

parameter	symbol	min.	typ.	max.	unit
Supply V_{CC} (pin 8)					
Internally stabilized supply voltage, at I_{CC} = 1,5 to 20 mA	V_{CC}	13,3	15	16,8	V
Supply current at V_{CC} = 15 V, unloaded,					
OFF state	I_{CC}	–	1	1,2	mA
ON state	I_{CC}	–	1,25	1,5	mA
Power dissipation, unloaded,					
OFF state	P	–	15	–	mW
ON state	P	–	19	25	mW
Thermal resistance					
TEA1058	$R_{th\ j\text{-}a}$	–	162	–	K/W
TEA1058T (note 1)	$R_{th\ j\text{-}a}$	–	140	–	K/W
TEA1058T (note 2)	$R_{th\ j\text{-}a}$	–	220	–	K/W
Power-on reset threshold voltage	V_{CCpor}	–	–	4,8	V
Oscillator RC pin OSC (pin 1)					
Injector voltage	V_{inj}	550	–	700	mV
Synchronization input SYN *(pin 5)*					
Input current (r.m.s. value)	$I_{5(rms)}$	3	–	–	μA
Upwards and downwards regulation inputs UP and DN (pins 7 and 6)					
Input voltage	$V_{6\text{-}4}$; $V_{7\text{-}4}$	1	–	–	V
Input current	$-I_6$; $-I_7$	–	3 $I_{5(rms)}$	–	μA
Slave input SLV (pin 2)					
Input current	$\pm I_2$	10	–	–	μA
Output Q (pin 3)					
Output current	I_3	–	–	100	mA

Notes

1. TEA1058T mounted on a ceramic substrate of 50 x 50 x 0,7 mm.
2. TEA1058T mounted on a printed-circuit board of 50 x 50 x 1,5 mm.

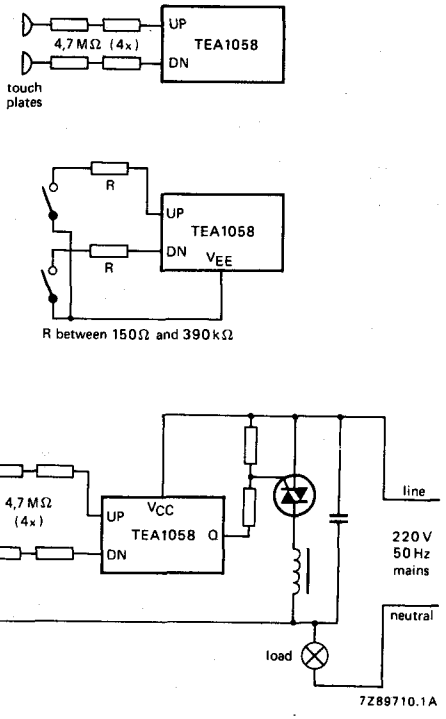


Fig. 2 Alternative arrangements for the UP and DN inputs.

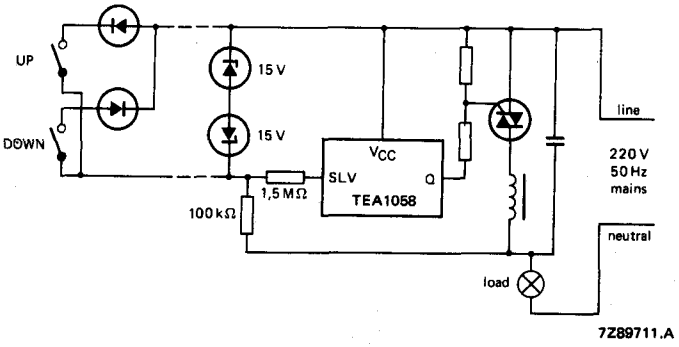
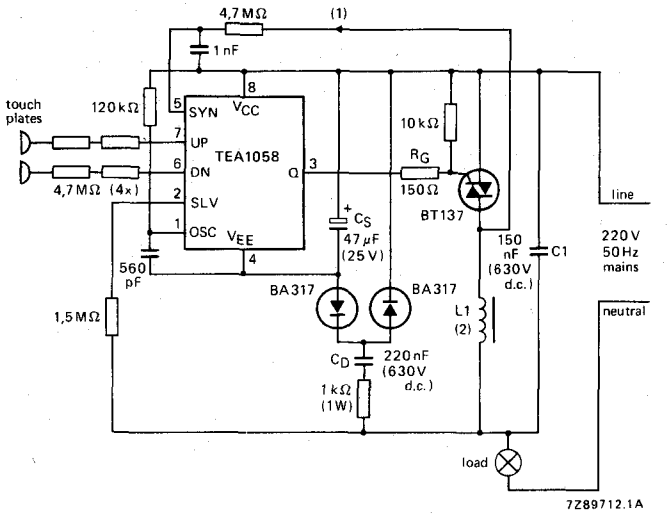


Fig. 3 SLV input arrangement.

APPLICATION INFORMATION



(1) The connection to the SYN input should be short and must be decoupled near to pins 5 and 8.
(2) For example, Vakuumschmelze FD 2.5 1N1 KN.

Fig. 4 Touch-controlled lamp dimmer circuit for max. 450 W. L1 and C1 form a radio-frequency interference filter with a quality factor Q of less than 1. This filter is necessary to satisfy the regulations of C.I.S.P.R. and V.D.E.

APPLICATION INFORMATION AVAILABLE ON REQUEST

GENERAL INDUSTRIAL

FIVE-TRANSISTOR ARRAY

GENERAL DESCRIPTION

The CA3046 is a bipolar integrated circuit consisting of five n-p-n transistors. Two transistors have common emitters, the others are freely accessible. The transistors are capable of driving loads up to 100 mA. The transistor geometry is such that it reaches its maximum current gain at quite low currents, making the devices also suitable for small-signal applications.

The transistors are partly matched, i.e. TR1 and TR2 form a matched pair, TR3 and TR4 also.

QUICK REFERENCE DATA

Collector-base voltage (open emitter)	V_{CBO}	max.	18 V
Collector-emitter voltage (open base)	V_{CEO}	max.	18 V
Collector current (d.c.)	I_C	max.	100 mA
Power dissipation			
each transistor	P	max.	400 mW
total	P_{tot}	max.	500 mW

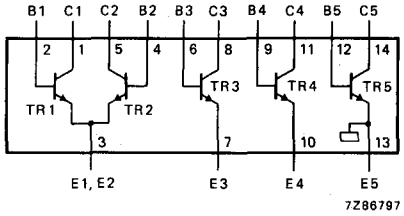


Fig. 1 Circuit diagram.

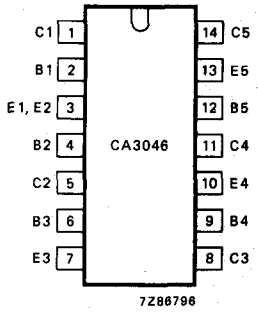


Fig. 2 Pinning diagram.

PACKAGE OUTLINE

14-lead DIL; plastic (SOT-27T).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Each transistor			
Collector-emitter voltage (open base)	V_{CEO}	max.	18 V
Collector-base voltage (open emitter)	V_{CBO}	max.	18 V
Collector-substrate voltage (open base and emitter)	V_{CSO}	max.	18 V
Emitter-base voltage (open collector)	V_{EBO}	max.	5 V
Collector current (d.c.)	I_C	max.	100 mA
Base current (d.c.)	I_B	max.	20 mA
Power dissipation			
each transistor	P	max.	400 mW
total (see also Fig. 3)	P_{tot}	max.	500 mW
Storage temperature range	T_{stg}		−50 to + 125 °C
Operating ambient temperature range	T_{amb}		−40 to + 125 °C

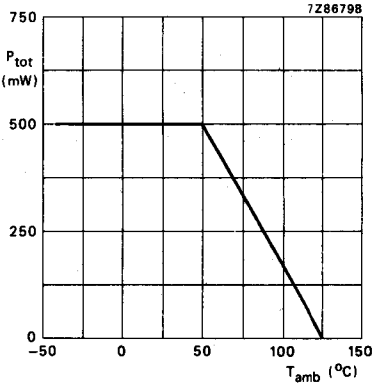


Fig. 3 Power derating curve.

OPERATING NOTE

As each collector forms a parasitic diode with the substrate, the substrate has to be connected to a voltage which is lower than any collector voltage. To minimize parasitic coupling between the transistors, this voltage should be signal ground.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Collector-emitter breakdown voltage at I_C = 1 mA; I_B = 0	$V_{(BR)CEO}$	30	–	–	V
Collector-substrate breakdown voltage at I_C = 1 mA; I_E = 0	$V_{(BR)CSO}$	30	75	–	V
Collector-base breakdown voltage at I_C = 100 μA; I_E = 0	$V_{(BR)CBO}$	30	75	–	V
Emitter-base breakdown voltage * at I_E = 100 μA; I_C = 0	$V_{(BR)EBO}$	6,2	7	7,8	V
D.C. current gain					
I_E = 350 μA; V_{CE} = 5 V	h_{FE}	75	–	525	
I_E = 20 mA; V_{CE} = 5 V	h_{FE}	47	–	365	
Saturation voltage					
at I_C = 5 mA; I_B = 0,5 mA	V_{CEsat}	–	200	400	mV
at I_C = 50 mA; I_B = 5 mA	V_{CEsat}	–	400	840	mV
Input offset voltage at V_{CE} = 5 V; I_C = 1 mA					
any two transistors	V_{IO}	–	1	–	mV
matched pair TR1 and TR2	V_{IO}	–	0,5	–	mV
Input offset current at V_{CE} = 5 V; I_C = 1 mA					
any two transistors	I_{IO}	–	1	–	μA
matched pair TR1 and TR2	I_{IO}	–	0,5	–	μA
Collector cut-off current					
at I_B = 0; V_{CEO} = 10 V	I_{CEO}	–	–	0,6	μA
at I_E = 0; V_{CBO} = 10 V	I_{CBO}	–	–	1	μA

* Breakdown of the emitter-base junction will cause degeneration of the current gain of the transistor.

STEPPING MOTOR DRIVE CIRCUIT

GENERAL DESCRIPTION

The SAA1027 is a bipolar integrated circuit intended for driving a four-phase two-stator motor. The circuit consists of a bidirectional four-state counter and a code converter to drive the four outputs in the sequence required for driving a stepping motor.

Features

- high noise immunity inputs
- clockwise and counter-clockwise operation
- reset facility
- high output current
- outputs protected against damage by overshoot.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}	9,5 to 18	V
Supply current, unloaded	I_{CC}	typ. 4,5	mA
Input voltage, all inputs			
HIGH	V_{IH}	min. 7,5	V
LOW	V_{IL}	max. 4,5	V
Input current, all inputs, LOW	I_{IL}	typ. 30	μA
Output current LOW	I_{OL}	max. 500	mA
Operating ambient temperature range	T_{amb}	−20 to +70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38A).

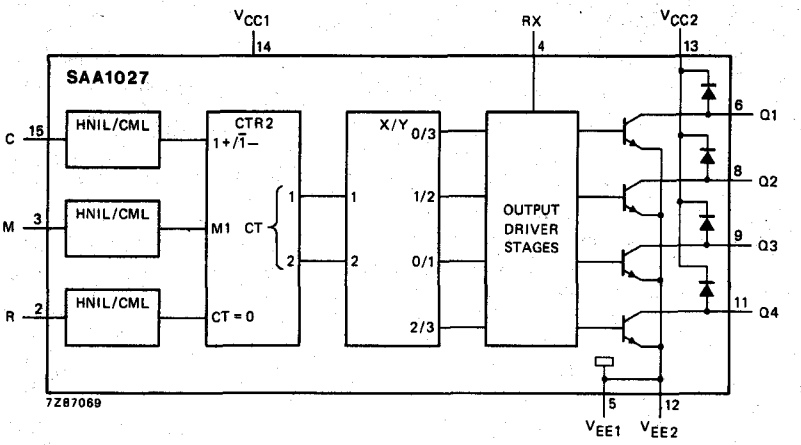


Fig. 1 Block diagram. The blocks marked HNIL/CML are high noise immunity input stages, the block marked CTR2 is a bidirectional synchronous 2-bit (4-state) counter and the block marked X/Y is a code converter. C is the count input, M the mode input to select forward or reverse counting and R is the reset input which resets the counter to content zero.

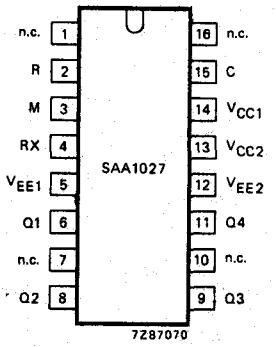


Fig. 2 Pinning diagram.

PINNING

1	n.c.	not connected
2	R	reset input
3	M	mode input
4	RX	external resistor
5	V_{EE1}	ground
6	Q1	output 1
7	n.c.	not connected
8	Q2	output 2
9	Q3	output 3
10	n.c.	not connected
11	Q4	output 4
12	V_{EE2}	ground
13	V_{CC2}	positive supply
14	V_{CC1}	positive supply
15	C	count input
16	n.c.	not connected

FUNCTIONAL DESCRIPTION

Count input C (pin 15)

The outputs change state after each L to H signal transition at the count input.

Mode input M (pin 3)

With the mode input the sequence of output signals, and hence the direction of rotation of the stepping motor, can be chosen, as shown in the following table.

counting sequence	M = L				M = H			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
0	L	H	L	H	L	H	L	H
1	H	L	L	H	L	H	H	L
2	H	L	H	L	H	L	H	L
3	L	H	H	L	H	L	L	H
0	L	H	L	H	L	H	L	H

Reset input R (pin 2)

A LOW level at the R input resets the counter to content zero. The outputs take on the levels shown in the upper and lower line of the table above.

If this facility is not used the R input should be connected to the supply.

External resistor pin RX (pin 4)

The external resistor R4 connected to RX sets the base current of the output transistors. Its value has to be chosen in accordance with the required output current (see Fig. 5).

Outputs Q1 to Q4 (pins 6, 8, 9 and 11)

The circuit has open-collector outputs. To prevent damage by an overshooting output voltage the outputs are protected by diodes connected to V_{CC2}, pin 13. High output currents mainly determine the total power dissipation, see Fig. 3.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC1}; V_{CC2}	max.	18	V
Input voltage, all inputs	V_I	max.	18	V
Current into pin 4	I_{RX}	max.	120	mA
Output current	I_{OL}	max.	500	mA
Power dissipation	P_{tot}	see Fig. 4		
Storage temperature range	T_{stg}	−40 to +125		°C
Operating ambient temperature range	T_{amb}	−20 to +70		°C

CHARACTERISTICS

V_{CC} = 9,5 to 18 V; V_{EE} = 0 V; T_{amb} = −20 to 70 °C unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply V_{CC1} and V_{CC2} (pins 14 and 13)					
Supply current at V_{CC1} = 12 V; unloaded; all inputs HIGH; pin 4 open	I_{CC}	2	4,5	6,5	mA
Inputs C, M and R (pins 15, 3 and 2)					
Input voltage					
HIGH	V_{IH}	7,5	–	–	V
LOW	V_{IL}	–	–	4,5	V
Input current					
HIGH	I_{IH}	–	1	–	μA
LOW	$-I_{IL}$	–	30	–	μA
External resistor pin RX (pin 4)					
Voltage at RX at V_{CC} = 12 V ± 15%; R4 = 130 Ω ± 5%	V_{RX}	3	–	4,5	V
Outputs Q1 to Q4					
Output voltage LOW					
at I_{OL} = 350 mA	V_{OL}	–	500	1000	mV
at I_{OL} = 500 mA	V_{OL}	–	700	–	mV
Output current					
LOW	I_{OL}	–	–	500*	mA
HIGH at V_Q = 18 V	$-I_{OH}$	–	–	50	μA

* See Figs 3 and 4.

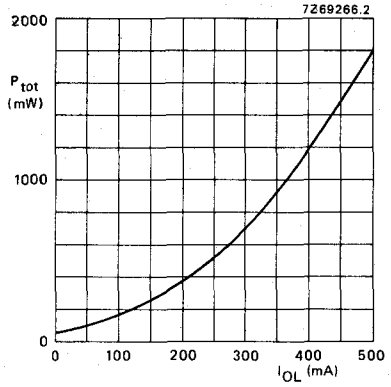


Fig. 3 Total power dissipation P_{tot} as a function of output current I_{OL}.

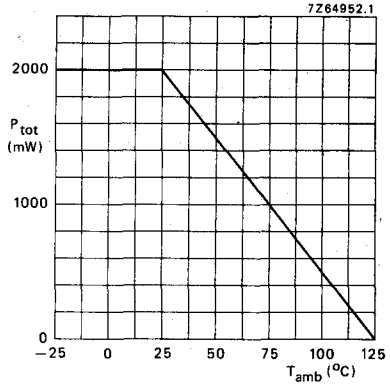


Fig. 4 Power derating curve.

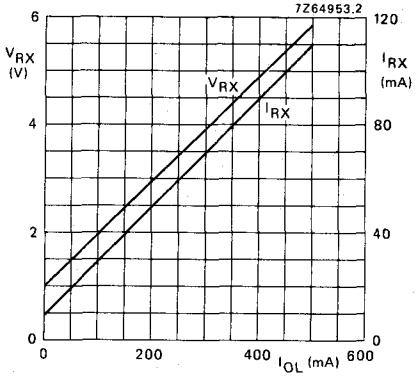


Fig. 5 Current I_{RX} into RX and voltage V_{RX} on RX as a function of required output current I_{OL}.

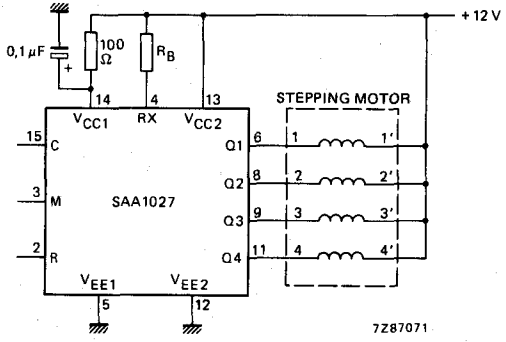


Fig. 6 Typical application of the SAA1027 as a stepping motor driver.

UNIVERSAL INDUSTRIAL LOGIC AND INTERFACE CIRCUIT

GENERAL DESCRIPTION

The SAA1029 is a universal bipolar logic and interface IC with high noise immunity and operational stability for industrial control applications. The most fundamental industrial control functions can be accomplished with only one SAA1029 IC. Figure 1 shows the logic configuration.

The IC comprises,
(1) Gate 1: 4-input AND gate with 1 inverted input,
(2) Gate 2: 3-input AND gate with 1 inverted input and adjustable propagation delay,
(3) Gate 3: 2-input AND gate with 1 inverted input.
The SAA1029 can be used as direct interface with LOCMOS (CMOS) ICs for realizing more complex functions. Therefore, the output signal can be limited to the voltage level of the common output clamping pin Z.

The propagation delay of NAND gate 2 is adjustable from microseconds to seconds by using an external capacitor at pin C. This makes it possible to adapt the control frequency limits to the system, so the optimum dynamic noise immunity can be achieved.

All the static and dynamic circuit values (including the output voltage) are independent of the supply voltage over a wide operating range. This allows the use of a simple unstabilized power supply.

The output is held to the LOW state automatically during switching on the power supply, so a special reset pulse can be omitted.

Features

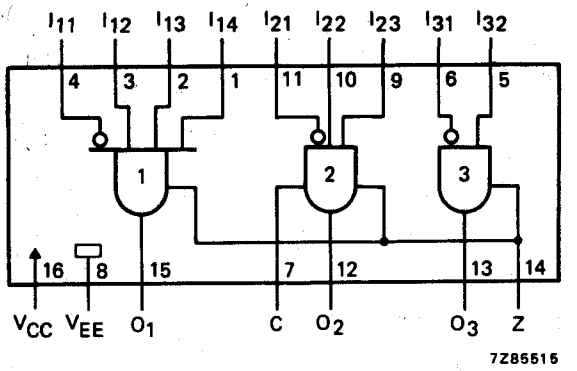
- Simple realization of the basic industrial control functions (logic functions, timing functions, memory functions).
- High dynamic and static noise immunity.
- High operation stability.
- Short-circuit protection of inputs and outputs to both V_{EE} and V_{CC}.
- Wide supply voltage range, so a simple power supply can be used.
- Wire interruption results in a safe input LOW state.
- LOCMOS (CMOS) compatible.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}	14 to 31,2	V
Operating ambient temperature range	T_{amb}	−30 to +85	°C
Input voltage HIGH	V_{IH}	6,5 to 44	V
Output voltage HIGH (without clamping)	V_{OH}	13 to 30	V
Output voltage HIGH (with clamping at pin Z)	V_{OH}	2,0 to (V_{CC} −0,7)	V
Input current	I_I	max. 10	mA
Quiescent supply current	I_{CC}	typ. 7,8	mA

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).



Logic equations:

$O_1 = \overline{I_{11}} \cdot I_{12} \cdot I_{13} \cdot I_{14}$

$O_2 = \overline{I_{21}} \cdot I_{22} \cdot I_{23}$

$O_3 = \overline{I_{31}} \cdot I_{32}$

Fig. 1 Logic diagram.

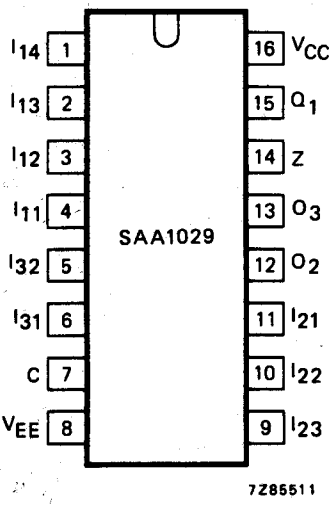


Fig. 2 Pinning diagram.

PINNING

4	I_{11}	inputs of gate 1
3	I_{12}	
2	I_{13}	
1	I_{14}	
15	O_1	output of gate 1
11	I_{21}	inputs of gate 2
10	I_{22}	
9	I_{23}	
12	O_2	output of gate 2
6	I_{31}	inputs of gate 3
5	I_{32}	
13	O_3	output of gate 3
7	C	external delay capacitor
14	Z	common output clamping
16	V_{CC}	positive supply voltage
8	V_{EE}	ground

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{CC}		0 to + 35 V
Input voltage (independent of V_{CC})	V_I		−0,15 to + 44 V
Output clamping voltage (pin 14)	V_Z		0 to + 35 V
Voltage at any output (pins 12, 13 and 15)			
pin 14 (Z) open	V_O		−0,15 to V_{CC} V
pin 14 (Z) at V_Z	V_O	max.	V_Z V or V_{CC} if $V_{CC} < V_Z$
Current into any input			
d.c.	$\pm I_I$	max.	10 mA
t_p = 0,5 μs; δ = 0,1% (peak value)	$\pm I_{IM}$	max.	100 mA
Sum of input currents			
d.c.	ΣI_I		−90 to + 10 mA
t_p = 0,5 μs; δ = 0,1% (peak value)	ΣI_{IM}		−900 to + 300 mA
External applied current at any output (pins 12, 13 and 15)			
pin 14 (Z) open			
d.c.	$\pm I_O$	max.	30 mA
t_p = 0,5 μs; δ = 0,1% (peak value)	$\pm I_{OM}$	max.	500 mA
External applied current at any output (pins 12, 13 and 15)			
pin 14 (Z) at V_Z			
d.c.	I_O		−30 to + 10 mA
t_p = 0,5 μs; δ = 0,1% (peak value)	I_O		−500 to + 100 mA
Voltage at pin 7 (C)	V_C		−0,15 to + 6 V
External capacitor at pin 7 (C)	any value		
Short-circuit of outputs (pins 12, 13 and 15)			
pin 14 (Z) open	allowed to V_{CC} and V_{EE} (0 V)		
at $V_Z < V_{CC}$	allowed only to V_{EE} (0 V)		
Total power dissipation (see also Fig. 3)			
at T_{amb} = 50 °C; continuous	P_{tot}	max.	1100 mW
at T_{amb} = 65 °C; max. 1000 hours	P_{tot}	max.	1100 mW
Storage temperature range	T_{stg}		−40 to + 150 °C

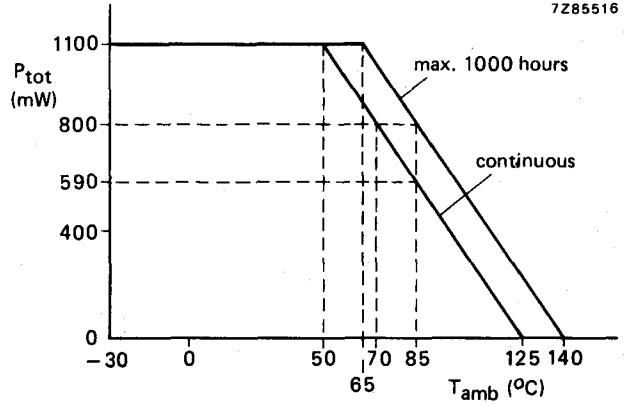


Fig. 3 Power derating curves; $R_{th\ j\text{-}a}$ = 70 K/W.

CHARACTERISTICS

At T_{amb} = −30 to + 85 °C; $T_j \leqslant 125$ °C; V_{CC} = 14 to 31,2 V; unless otherwise specified

	symbol	min.	typ.	max.	unit	conditions
Supply voltage	V_{CC}	14	24	31,2	V	
Quiescent supply current	I_{CC}	–	7,8	–	mA	
	I_{CC}	–	–	12,2	mA	V_{CC} = 31 V; T_{amb} = 25 °C
Quiescent current ratio	$\frac{I_{CC1}}{I_{CC2}}$	–	0,67	–		$I_{CC1} = I_{CC}$ at T_j = 125 °C $I_{CC2} = I_{CC}$ at T_j = 25 °C
Input voltage LOW	V_{IL}	–	–	5	V	
Input voltage HIGH	V_{IH}	6,5	–	–	V	
	V_{IH}	6,55	–	–	V	
Input current LOW	$-I_{IL}$	–	–	100	μA	
	$-I_{IL}$	–	–	95	μA	
Input current HIGH	I_{IH}	300	–	–	μA	
Rate of change of input signal	dV/dt	3	–	–	V/ms	
Input current*	$-I_I$	–	–	120	μA	V_I = 1 V
	I_I	–	–	280	μA	V_I = 35 V
Output clamping voltage*	V_Z	–	–	30	V	$V_Z = V_{CC} - 1$ V
Output voltage without clamping (pin 14 open)* non-inverting input: V_I = 5,1 V inverting input: V_I = 6,3 V						V_{CC} = 14 V
LOW	V_{OL}	–	–	1	V	I_O = 1,32 mA
	V_{OL}	–	–	1,5	V	I_O = 2,91 mA
HIGH	V_{OH}	$V_{CC}-1,4$	–	–	V	$-I_O$ = 5 mA
Output voltage with clamping (pin 14 at V_Z)*						V_{CC} = 31,2 V $V_Z < V_{CC}-1$ V
LOW	V_{OL}	–	–	1	V	I_O = 1,32 mA
	V_{OL}	–	–	1,5	V	I_O = 1,91 mA

HIGH	V_{OH}	$(V_Z - 0{,}475)$	–	$(V_Z + 0{,}225)$	V	$I_O = 0$ mA
	V_{OH}	$(V_Z - 0{,}455)$	–	$(V_Z + 0{,}12)$	V	$-I_O = 1$ mA
	V_{OH}	$(V_Z - 0{,}41)$	–	$(V_Z + 0{,}055)$	V	$-I_O = 3$ mA
Output short-circuit current*						
LOW-signal	I_{OscL}	2,95	–	9,6	mA	output at V_{CC}
HIGH-signal	$-I_{OscH}$	10,1	–	21,9	mA	output at V_{EE} (0 V)
Capacitor charging current*	I_C	–	30	–	μA	
Propagation delays*						
gates 1, 2 and 3						
HIGH to LOW	t_{PHL}	–	3,5	–	μs	C = 0 (at gate 2)
LOW to HIGH	t_{PLH}	–	3,5	–	μs	C = 0 (at gate 2)
gate 2						
HIGH to LOW	t_{PHL}	1,85	–	5,2	ms	C = 47 nF ± 1%
LOW to HIGH	t_{PLH}	7,5	–	14	ms	C = 47 nF ± 1%; $R_{insulation} > 100$ MΩ

* At $T_{amb} = 25\ ^oC$; $V_{CC} = 24$ V; unless otherwise specified.

CHARACTERISTICS (worst case conditions)

At T_j = + 125 to + 140 °C; maximum 1000 hours

	symbol	min.	typ.	max.	unit	conditions
Input voltage LOW	V_{IL}	–	–	5	V	
Input voltage HIGH	V_{IH}	6,55	–	–	V	
Input current	I_I	95	–	300	μA	V_I = 1 to 44 V
Change of input current overdrive of other inputs $\Sigma(-I_I) < 10$ mA	ΔI_I	–	–	120	μA	$V_I < V_{CC}$ −1 V
	ΔI_I	–	–	158	μA	$V_I > V_{CC}$ −1 V
overdrive of other inputs $\Sigma(-I_I) < 90$ mA	ΔI_I	–	–	280	μA	$V_I < V_{CC}$ −1 V
	ΔI_I	–	–	320	μA	$V_I > V_{CC}$ −1 V
Input voltage by current overdrive	V_I	46	–	65	V	$\Sigma(-I_I)$ = 10 mA
Output voltage without clamping (pin 14 open) LOW	V_{OL}	–	–	0,35	V	$I_{OL} \leqslant$ 0,095 mA
	V_{OL}	–	–	1	V	I_{OL} = 0,095 to 1 mA
	V_{OL}	–	–	1,5	V	I_{OL} = 1 to 2,5 mA
HIGH	V_{OH}	V_{CC}−1,5	–	–	V	$-I_{OH} \leqslant$ 5 mA
Output voltage with clamping (pin 14 at V_Z)						V_Z = 2,5 to V_{CC} −1 V
HIGH	V_{OH}	(V_Z −0,5)	–	(V_Z + 0,245)	V	I_{OH} = 0 mA
	V_{OH}	(V_Z −0,5)	–	(V_Z + 0,15)	V	I_{OH} = 1 mA
	V_{OH}	(V_Z −0,5)	–	V_Z	V	I_{OH} = 3 mA
	V_{OH}	–	–	0,75	V	I_{OH} = 0 mA; V_Z = 0 V
Output short-circuit current LOW-signal	I_{OscL}	–	–	11	mA	output at V_{CC}
HIGH-signal	$-I_{OscH}$	5	–	28,5	mA	output at V_{EE} (0 V)
HIGH-signal	$-I_{OscH}$	–	–	10	mA	output at V_{EE} (0 V); T_j = 140 °C

Current out of pin 14 (Z) when currents are forced into outputs	$-I_Z$	–	–	2,2	mA	$-I_O \leqslant 3$ mA
	$-I_Z$	ΣI_O	–	–	mA	$\Sigma I_O = (I_{O1} + I_{O2} + I_{O3})$
Current into pin 14 (Z) when inputs are set for output to be LOW	I_Z	–	–	300	μA	$-I_O = 30$ mA; $V_O \leqslant V_{EE}$
Supply current change	ΔI_{CCmax}	$(0{,}3 \times \lvert I_I \rvert) + (0{,}55 \times \lvert I_O \rvert)$			mA	input and/or output voltages are negative with respect to V_{EE}
Propagation delays gates 1 and 3						
HIGH to LOW	t_{PHL}	1	–	7	μs	
LOW to HIGH	t_{PLH}	1	–	7	μs	
gate 2						
HIGH to LOW	t_{PHL}	0,1	–	4	μs	without capacitor
LOW to HIGH	t_{PLH}	0,3	–	6	μs	without capacitor
HIGH to LOW	t_{PHL}	38 x C	–	113 x C	μs	with capacitor; C in μF
LOW to HIGH	t_{PLH}	142 x C	–	334 x C	μs	with capacitor; C in μF
Voltage spikes output LOW	V_{OL}	–	–	2	V	see note

Note

V_{CC} rising from 0 to 14 V; all inputs open; internally it is guaranteed that the input threshold voltage $V_{IL} > V_{OL}$.

APPLICATION INFORMATION

The following figures (Figs 4 to 11) give some examples of the basic industrial control functions.

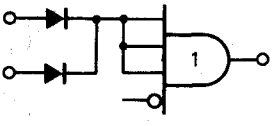


Fig. 4 OR function.

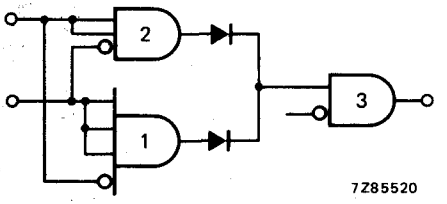


Fig. 5 EXCLUSIVE-OR function.

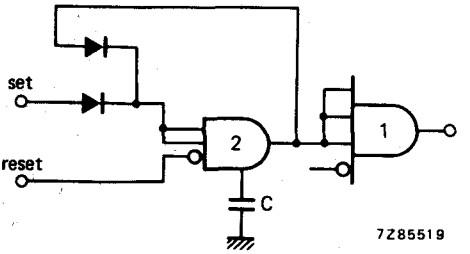


Fig. 6 Delayed memory; reset is dominating.

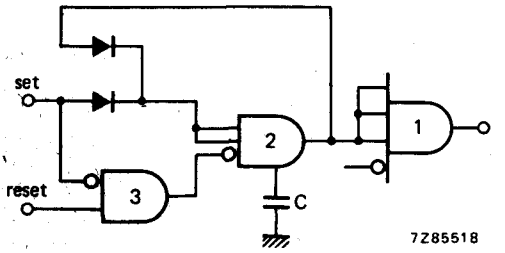


Fig. 7 Delayed memory; set is dominating.

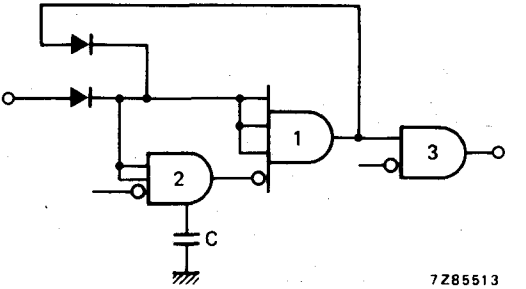


Fig. 8 Monostable flip-flop; for C = 4,7 μF, 1 s no reaction.

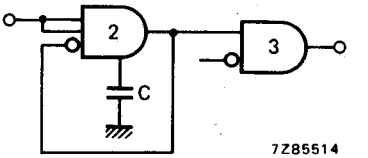


Fig. 9 Start delay function.

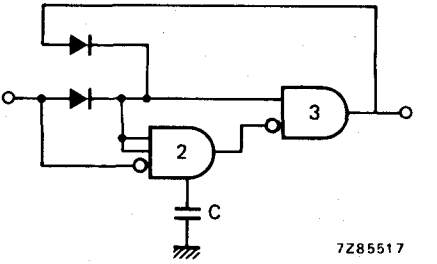


Fig. 10 Decay delay function.

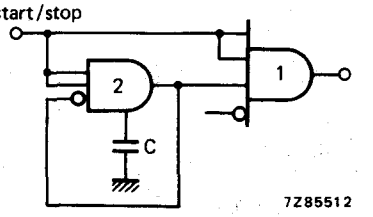


Fig. 11 Square-wave oscillator.

SERVO-MOTOR CONTROL CIRCUIT

GENERAL DESCRIPTION

The SAK150BT is a bipolar integrated circuit intended for remote control applications in digital proportional systems or other closed-loop position control applications, in which it will translate the width of its input pulses into a mechanical position. It incorporates a linear one-shot for improved positional accuracy. The circuit has additional outputs for driving external p-n-p transistors to form a bidirectional bridge.

Features

- high output current
- bidirectional bridge output facility with single power supply
- adjustable deadband
- adjustable proportional range
- high linearity
- wide supply voltage range
- low standby supply current
- provides stabilized supply for external circuit

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		3 to 9 V
Supply current, standby, at V_{CC} = 4,8 V	I_{CC}	typ.	4 mA
Stabilized supply voltage for external circuit	V_Z	typ.	2 V
Output current at V_{CC} = 4,8 V	I_Q	max.	500 mA
Operating ambient temperature range	T_{amb}		−20 to + 60 °C

PACKAGE OUTLINE

14-lead mini-pack; plastic (SO-14; SOT-108A).

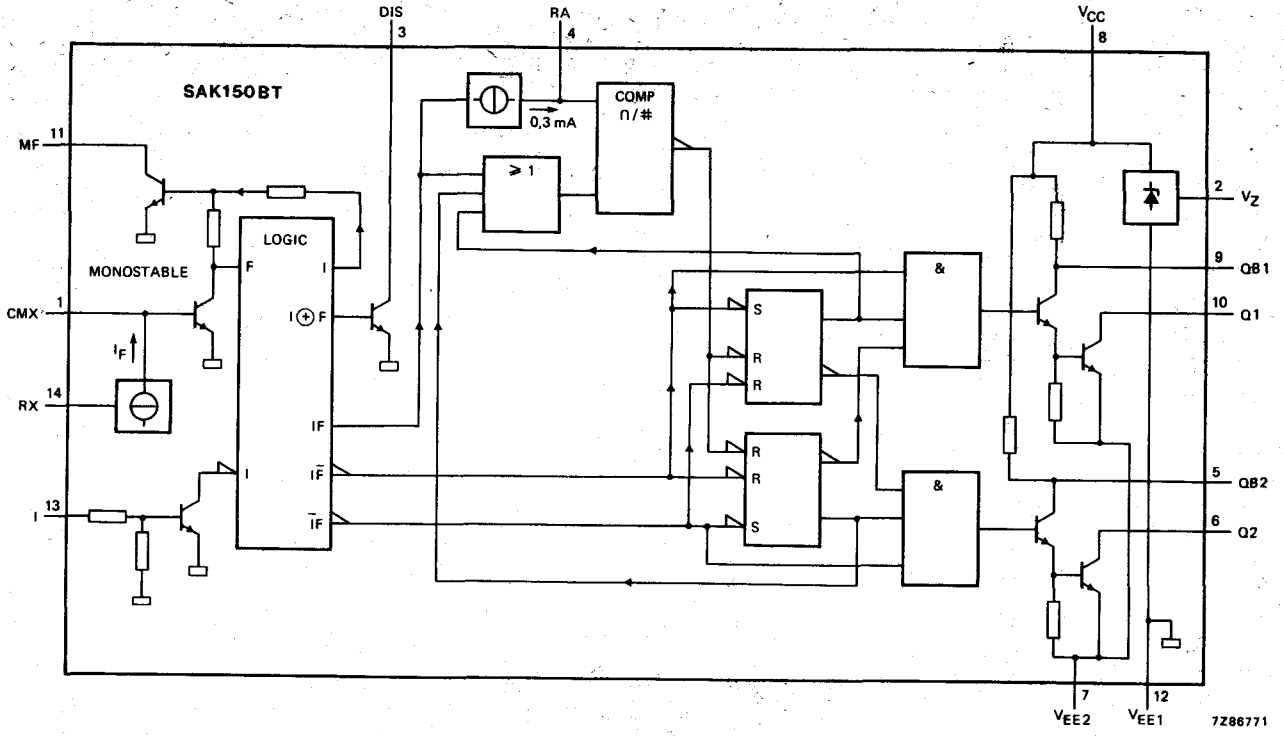


Fig. 1 Block diagram. The blocks marked "&" are AND gates, the block marked "≥1" is an OR gate, the blocks with inputs marked S and R are set-reset flip-flops and the block marked "COMP" is a comparator. The inputs of this comparator have unequal weights; this particular comparator may be considered as a high-gain amplifier for the upper input with the lower input giving a small shift of the switching level. The triangles at some of the inputs and outputs are polarity indicators showing that the internal logic 1-state at that input or output corresponds with the external logic L-level (LOW). At inputs and outputs without polarity indicator the internal logic 1-state corresponds with the external logic H-level (HIGH).

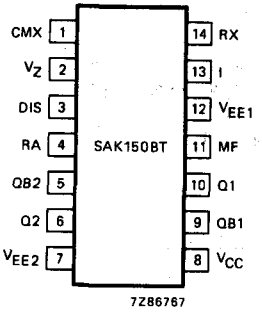


Fig. 2 Pinning diagram.

PINNING

1	CMX	external monostable capacitor
2	V_Z	stabilized voltage output
3	DIS	discharging resistor
4	RA	reset amplifier
5	QB2	p-n-p driver output
6	Q2	power output
7	V_{EE2}	ground of output stage
8	V_{CC}	positive supply
9	QB1	p-n-p driver output
10	Q1	power output
11	MF	monostable feedback
12	V_{EE1}	ground of circuit (except output stage)
13	I	input
14	RX	external resistor

FUNCTIONAL DESCRIPTION (See also Fig. 5)

The SAK150BT has two sets of outputs on which it is capable of producing output pulses of variable width. The output arrangement is such that these output pulses can drive a servo-motor in both directions. The servo-motor actuates a potentiometer. The width of the output pulses is reduced to zero when the position of the potentiometer slider corresponds with the width of the input pulses.

The circuit operates as follows. The positive-going leading edges of the input pulses trigger a monostable element. Its output pulses have a duration that is a linear function of the position of the potentiometer slider. These pulses therefore will be referred to as feedback pulses.

The presence of both the input pulse and the feedback pulse switches on a current source of approx. 0,3 mA which charges an external capacitor C2 connected from RA (pin 4) to ground. The variation of the voltage on this capacitor after some time causes the output of the high-gain reset amplifier to change state and reset the two output flip-flops.

Depending on the relative durations of input pulse and feedback pulse the following happens.

1. Difference in duration of input pulse and feedback pulse less than the deadband time: no output signals generated.
2. Input pulse shorter than feedback pulse: outputs Q1 and QB1 activated.
3. Input pulse longer than feedback pulse: outputs Q2 and QB2 activated.

The trailing (negative-going) edge of the shorter of the two pulses (input pulse or feedback pulse) switches off the current source that charged C2. It further switches on the discharging of C2 via R2, connected to DIS (pin 3). As a consequence the output of the reset amplifier changes state after a short delay and no longer resets the flip-flops. Finally the code converter generates a signal which sets the appropriate output flip-flop but inhibits the output.

At the trailing edge of the longer of the two pulses the signal that has set one of the flip-flops changes state. This enables the corresponding output. It further finishes the discharging of C2 via R2. C2 will now be charged via R3. When the voltage on C2 reaches the switching level of the reset amplifier its output signal will reset the flip-flops again and this will terminate the output pulse (see Fig. 3). The duration of the output pulse is proportional with the charge required by C2 to reach the switching level of the reset amplifier, and this charge is proportional to the time that C2 has been discharged via R2, i.e. the difference in duration of the input pulse and the feedback pulse.

The maximum output pulse duration is reached when the output pulse is terminated by the next input pulse.

FUNCTIONAL DESCRIPTION (continued)

Supply: V_{CC}, V_{EE1}, V_{EE2} and V_Z (pins 8, 12, 7 and 2)

The SAK150BT contains a voltage stabilizer. This permits the circuit to be used over a very wide supply voltage range without substantial variation of its performance. The stabilized supply voltage is available at V_Z (pin 2) to supply an external peripheral circuit, e.g. a feedback potentiometer.

The circuit has two ground pins, one for the output stage (V_{EE2}) and one for the rest of the circuit (V_{EE1}). They should be interconnected externally.

Input I (pin 13)

Input pulses should be positive-going, i.e. the time that the input signal is HIGH is the input parameter. Usual values are 1 to 2 ms for the pulse to be HIGH and 20 ms for the pulse repetition time.

Feedback pulse duration: CMX, MF and RX (pins 1, 11 and 4)

The duration of the feedback pulse is determined by external capacitor C1 connected between CMX and MF. This capacitor is charged by a current source whose current is determined by external resistor R1 connected between RX and ground.

Deadband time

The deadband time is the maximum difference in duration between the input pulse and the feedback pulse that will not give an output signal (see Fig. 4). The deadband time is determined by external resistor and capacitor R2 and C2 connected to RA and by the threshold voltage V_{thr} of the Schmitt trigger and by its deadband V_{db}, according to the following approximative formula:

$$t_{db} \approx \frac{R2 \times C2 \times V_{db}}{V_{thr} - V_{db}} = 0{,}0215\ R2 \times C2\ (\text{typical})^*.$$

Proportional range

The output pulse width is proportional to the input pulse width up to the point that the output pulse width equals the time between the input pulses t_{IL} (see Fig. 4). The input pulse width at which the maximum output pulse width is reached may be chosen by the ratio of R2 and R3. It is given by the following approximative formula:

$$t_{prop} \approx \frac{R2}{R3} \times \left(\frac{V_{CC}}{V_{thr}} - 1\right) \times t_{IL}{}^*.$$

Outputs Q1, QB1, Q2 and QB2 (pins 10, 9, 6 and 5)

The outputs Q1 and Q2 are open-collector outputs capable of sinking up to 500 mA. The outputs QB1 and QB2 are intended to drive external p-n-p transistors. Together with the Q outputs these p-n-p transistors may form a bidirectional bridge output with a single power supply, see Fig. 4.

*If $e^x \approx 1 + x$ for charge and discharge at RA (pin 4).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC}	max.	12 V
Current at V_Z	$-I_{VZ}$	max.	3 mA
Input voltage	V_I	max.	12 V
	$-V_I$	max.	5 V
Voltage at CMX	$-V_{CMX}$	max.	5 V
Current at CMX	I_{CMX}	max.	5 mA
Current at RX	$-I_{RX}$	max.	1 mA
Voltage at MF	V_{MF}	max.	12 V
Current at MF	I_{MF}	max.	3 mA
	$-I_{MF}$	max.	3 mA
Current at RA	I_{RA}	max.	6 mA
	$-I_{RA}$	max.	5 mA
Output voltage, Q1 and Q2	V_Q	max.	24 V
Output current, Q1 and Q2, repetitive peak	I_{QRM}	max.	800 mA
	$-I_Q$	max.	10 μA
Output voltage, QB1 and QB2	V_{QB}	max.	12 V
Output current, QB1 and QB2	I_{QB}	max.	70 mA
	$-I_{QB}$	max.	10 mA
Storage temperature range	T_{stg}	−35 to + 125	°C
Operating ambient temperature range	T_{amb}	−20 to + 70	°C

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS

V_{CC} = 3 to 9 V; $V_{EE1} = V_{EE2}$ = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply: V_{CC} and V_Z (pins 8 and 2)					
Supply current at V_{CC} = 4,8 V; T_{amb} = 25 °C; output stages OFF	I_{CC}	–	4	–	mA
Stabilized voltage output	V_Z	–	1,95	–	V
Variation with temperature	$\Delta V_Z/\Delta T$	–	6	–	mV/K
Output current at V_{CC} = 4,8 V for ΔV_Z = 40 mV	$-I_Z$	–	–	1	mA
Input I (pin 13)					
Input voltage					
HIGH	V_{IH}	2,4	–	–	V
LOW	V_{IL}	–	–	0,6	V
Input current					
HIGH at V_I = 2,4 V	I_{IH}	–	–	250	μA
LOW at V_I = 0,6 V	$-I_{IL}$	–	–	30	μA
External resistor pin RX (pin 14)					
Voltage at $-I_{RX}$ = 100 μA	V_{RX}	–	0,7	–	V
Current range	I_{RX}	10	–	200	μA
Monostable feedback pin MF (pin 11)					
Voltage at I_{MF} = 2 mA	V_{MF}	–	–	300	mV
Output current	I_{MF}	–	–	3	mA
Reset amplifier pin RA (pin 4)					
Switching level of reset amplifier, internal current source OFF	V_{sw}	–	1,9	–	V
Deadband (shift of switching level by internal current source)	V_{db}	–	40	–	mV
Input current					
HIGH	I_{RA}	–	–	6	mA
LOW	$-I_{RA}$	–	300	–	μA
External monostable capacitor pin CMX (pin 1)					
Current	I_{CMX}	–	–	1	mA
	$-I_{CMX}$	–	I_{RX}	–	

parameter	symbol	min.	typ.	max.	unit
Outputs Q1 and Q2 (pins 10 and 6)					
Output voltage at V_{CC} = 4,8 V; I_{QB} = 50 mA; I_Q = 500 mA	V_Q	–	450	550	mV
Output current at V_{CC} = 4,8 V; I_{QB} = 20 mA	I_Q	–	–	500	mA
Outputs QB1 and QB2 (pins 9 and 5)					
Output voltage at V_{CC} = 4,8 V; I_{QB} = 50 mA	V_{QB}	–	1,2	1,6	V
Output current at V_{CC} = 4,8 V	I_{QB}	–	–	50	mA
Discharging pin DIS (pin 3)					
Output voltage LOW at I_{DIS} = 2 mA	V_{DISL}	–	–	300	mV
Output current					
HIGH at V_{DIS} = 9 V	$-I_{DISH}$	–	–	500	nA
LOW	I_{DISL}	–	–	5	mA

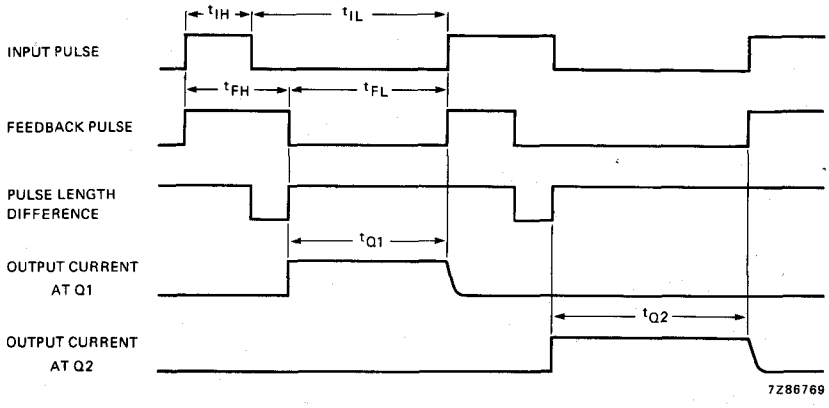


Fig. 3 Timing diagram.

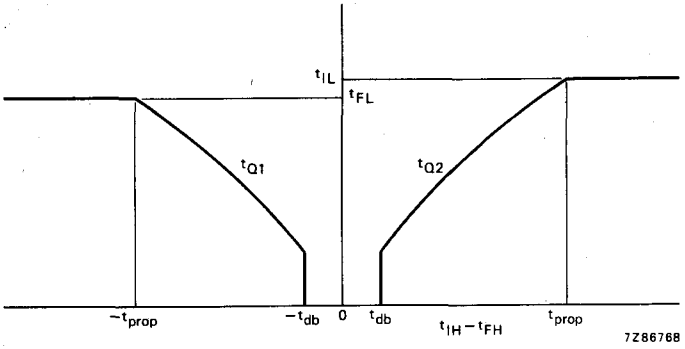


Fig. 4 *Output current* pulse duration t_Q as a function of the difference between input pulse duration t_{IH} and feedback pulse duration t_{FH}. There is no output signal for differences less than the deadband time t_{db}. The maximum output pulse duration at outputs Q1 and QB1 is equal to the time between the feedback pulses t_{FL}, the maximum duration at Q2 and QB2 is equal to the time between the input pulses t_{IL}. The maximum pulse duration is reached at a pulse duration difference t_{prop}.

APPLICATION INFORMATION

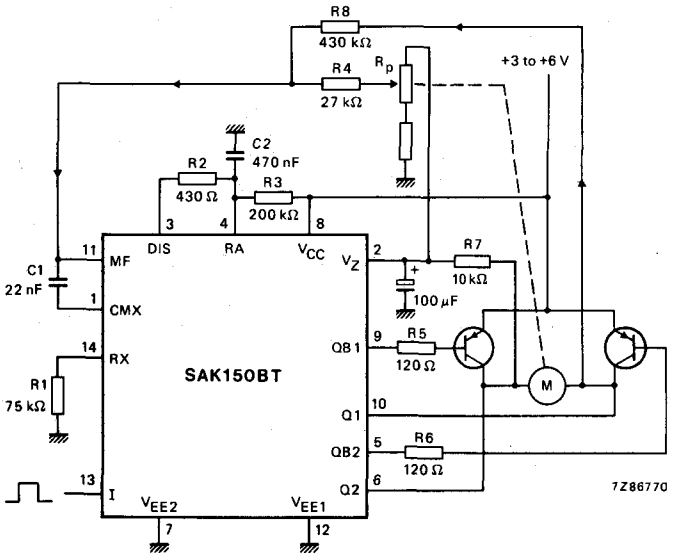


Fig. 5 Typical application of the SAK150BT for remote control of a model. The arrangement may be the last part at the receiving side, e.g. after a multi-channel time division multiplex system, to drive the steering motor. The potentiometer R_p is actuated by the motor.

CONTROL CIRCUIT FOR SWITCHED-MODE POWER SUPPLY

GENERAL DESCRIPTION

The TDA1060 is a bipolar integrated circuit intended for the control of a switched-mode power supply. It incorporates all the control functions likely to be required in switched-mode power supplies for professional equipment.

The circuit features:

- Suitability for a wide range of supply voltages
- Built-in stabilized power supply for external circuitry
- Built-in temperature-compensated voltage reference
- Adjustable frequency
- Adjustable control loop sensitivity
- Adjustable pulse width
- Adjustable maximum duty factor
- Adjustable overcurrent protection limit
- Low supply voltage protection with hysteresis
- Loop fault protection
- Slow-start facility
- Feed-forward facility
- Core saturation protection facility
- Overvoltage protection facility
- Remote ON/OFF switching facility

QUICK REFERENCE DATA

Supply voltage (voltage source)	V_{CC}	max.	18 V
Supply current (current source)	I_{CC}	max.	30 mA
Output current	$-I_{14}; I_{15}$	max.	40 mA
Stabilized voltage	V_Z	typ.	8,4 V
Reference voltage	V_{ref}	typ.	3,72 V
Output pulse repetition frequency range	f_o	50 Hz to 100	kHz
Operating ambient temperature range			
TDA1060	T_{amb}	−25 to +125	°C
TDA1060A	T_{amb}	0 to +70	°C
TDA1060B	T_{amb}	−55 to +150	°C

PACKAGE OUTLINES

TDA1060, TDA1060A: 16-lead DIL; plastic (SOT-38).
TDA1060B: 16-lead DIL; ceramic (SOT-74).

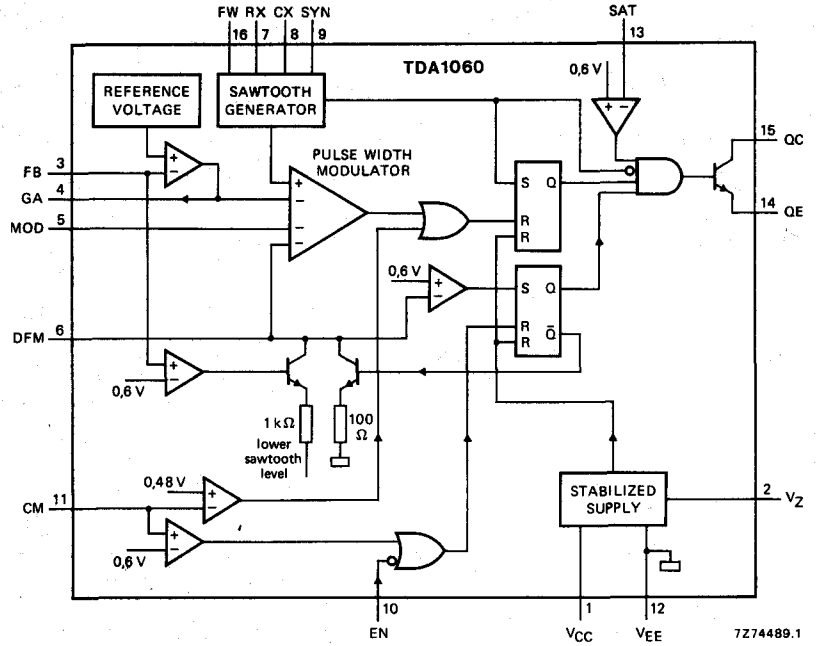


Fig. 1 Block diagram.

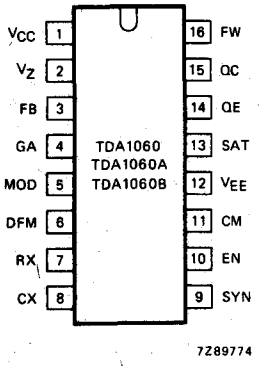


Fig. 2 Pinning diagram.

PINNING

1	V_{CC}	positive supply connection
2	V_Z	stabilized voltage output
3	FB	feedback input
4	GA	gain adjustment output
5	MOD	modulation input
6	DFM	maximum duty factor input
7	RX	external resistor connection
8	CX	external capacitor connection
9	SYN	synchronization input
10	EN	ENABLE input
11	CM	overcurrent protection input
12	V_{EE}	common
13	SAT	core saturation and overvoltage protection input
14	QE	emitter output
15	Q_C	collector output
16	FW	feed-forward input

FUNCTIONAL DESCRIPTION

The TDA1060 contains the control loop for a fixed-frequency pulse-duration regulated SMPS. The device works as follows. The output voltage V_O of the SMPS is sensed via a feedback network and compared with an internal reference voltage V_{ref}. Any difference between V_O and V_{ref} is amplified and fed to a pulse-width modulator (PWM), where it is compared with the instantaneous level of a ramp waveform (sawtooth) from an oscillator. The output from the PWM is a rectangular waveform synchronized with the oscillator waveform; its duty factor depends on the difference between V_O and V_{ref}. This signal drives the base of the SMPS power switching transistor so that its conduction period and hence the amount of energy transferred from the input to the output of the SMPS is controlled, resulting in a constant output voltage.

Stabilized power supply: V_{CC} and V_Z (pins 1 and 2)

The circuit contains a voltage/current regulator and may be supplied either by a current source (e.g. a series resistor connected to the high voltage input of the SMPS), or a voltage source (e.g. a 12 V battery).

The stabilized voltage, typically 8,4 V, is also available at V_Z, pin 2 for supplying external circuitry, e.g. a potentiometer to adjust the maximum duty factor. This supply output is protected against short-circuits. The current drawn from this output increases the total IC supply current by the same amount.

When the supply voltage V_{CC} becomes too low, i.e. $V_{CC} < V_Z + 0{,}2$ V, the circuit is automatically switched off. As soon as the supply voltage exceeds this threshold value by more than 0,2 V the circuit starts the SMPS via the slow start procedure.

Operating frequency: RX and CX (pins 7 and 8)

The frequency of the sawtooth generator, and hence of the output pulses, is set by an external resistor R7 at RX, pin 7, and an external capacitor C8 at CX, pin 8. The frequency will be 1,2/R7C8. It may be set between 50 Hz and 100 kHz and is virtually independent of the supply voltage.

Maximum duty factor and slow start: DFM (pin 6)

The maximum duty factor is set by the voltage on the duty factor input DFM (see Fig. 4). This voltage usually is derived from the stabilized power supply V_Z, pin 2, by an external voltage divider, see Fig. 6. As the upper and lower levels of the sawtooth waveform are set by an internal voltage divider, the accuracy of the maximum duty factor setting is determined by resistor ratios rather than by absolute values.

In case of a short-circuited feedback loop ($V_{3\text{-}12}$ less than typ. 600 mV) the duty factor input is internally biased to the lower level of the sawtooth waveform via a resistor of typ. 1 kΩ. The maximum duty factor permitted in that case sets a maximum limit to the impedance level of the external voltage divider at pin 6.

During the flyback of the sawtooth the output pulse is inhibited. For a 1 nF capacitor C8 at pin 8 this flyback time is 1 μs. This sets a natural limit to the duty factor.

The time constant for the slow start is determined by an external capacitor connected between the maximum duty factor input DFM and V_{EE}, pin 12, together with the impedance of the voltage divider at pin 6. This capacitor also determines the dead time before the slow start procedure for remote ON/OFF or when the current sensing voltage has exceeded 600 mV, see below.

If the DFM input is not used it should be connected to V_Z via a resistor of 5 kΩ.

FUNCTIONAL DESCRIPTION (continued)

Control loop sensitivity, stability, and feedback loop fault protection, FB and GA (pins 3 and 4)

The device contains a control loop error amplifier, i.e. a differential amplifier that compares the voltage on the feedback input FB, pin 3, with the internal reference voltage. This reference voltage is a temperature-compensated voltage source based on the band-gap energy of silicon.

The control loop sensitivity is determined by the closed-loop gain A_f of the error amplifier. Normally the output from the SMPS is connected to the feedback input FB via a voltage divider and a series resistor. The closed-loop gain of the error amplifier is set by applying feedback from the gain adjustment output GA, pin 4, to the feedback input FB by a resistor R3-4, see Fig. 6.

To avoid instability a capacitor should be connected between the gain output GA and V_{EE}, pin 12. A 22 nF capacitor will cause the frequency response to fall off above 600 Hz.

The feedback input FB is internally biased to the HIGH level, this gives a protection against a feedback loop fault: an open feedback loop will make the duty factor zero.

A shorted feedback loop (feedback voltage less than typ. 600 mV) causes the maximum duty factor input DFM to be internally biased to the lower level of the sawtooth waveform via a resistor of typ. 1 kΩ, thus substantially reducing the maximum duty factor. This duty factor will then be determined by the impedance of the external voltage divider at DFM, pin 6, and the internal biasing resistor.

Overcurrent protection input CM (pin 11)

There are two current limits, corresponding with voltages on the overcurrent protection input CM of typ. 480 mV and 600 mV. As soon as the voltage on this input exceeds 480 mV, the running output pulse is immediately terminated; the next pulse starts normally at the next period. If the voltage exceeds 600 mV, the output pulses are inhibited for a certain dead time, during which the slow start capacitor at pin 6 is unloaded. After this the circuit starts again with the slow start procedure.

If the overcurrent protection input CM is not used, it should be connected to V_{EE}, pin 12.

Feed-forward input FW (pin 16)

The feed-forward input FW can be connected to an external voltage divider from the input voltage of the SMPS, see Fig. 6. It has the effect of varying the supply voltage of the sawtooth generator with respect to the stabilized voltage. When the voltage on the feed-forward input increases, the upper level of the sawtooth is also increased. Since neither the voltage level that sets the maximum duty factor nor the feedback voltage are influenced by the feed-forward, the duty factor reduces (see Fig. 5). This can therefore compensate for mains voltage variations.

If feed-forward is not required the feed-forward input FW should be connected to V_{EE}, pin 12.

Synchronization input SYN (pin 9)

The frequency of the sawtooth waveform, and hence of the output pulses, can be synchronized via the TTL compatible synchronization input SYN. The synchronizing frequency must be lower than the oscillator free-running frequency. When the synchronization input is LOW the sawtooth generator is stopped; it starts again when the input goes HIGH. Synchronization pulses do not influence the slope of the sawtooth, and hence not the width of the output pulses, they only change their separation in time.

For free-running operation it is advisable to connect the synchronization input SYN to V_Z, pin 2.

Core saturation and overvoltage protection input SAT (pin 13)

To obtain a protection against core saturation, especially during transient conditions, the output transformer of the SMPS has to be fitted with a winding serving as a current sensor. Its output voltage is rectified and fed to the SAT input.

This core saturation protection may be combined with an overvoltage protection. To this end a portion of the SMPS output voltage is also fed to the SAT input either via a voltage divider or via a suitable regulator diode (zener diode). The output pulses are inhibited as long as the voltage on this input exceeds the threshold voltage, typ. 600 mV.

The voltage at the SAT input does not influence the frequency of the sawtooth generator and hence not of the output pulses.

If none of these protection facilities are used, the SAT input should be connected to V_{EE}, pin 12.

Remote ON/OFF switching: ENABLE input EN (pin 10)

The output pulses can be switched on and off by applying logic levels to the TTL compatible ENABLE input. A LOW level causes immediate inhibition of the output pulses, a subsequent HIGH level switches the circuit on with the slow-start procedure.

If this facility is not required, EN should be connected to V_Z, pin 2.

Modulation input MOD (pin 5)

The duty factor of the output pulses may be reduced below the value resulting from the voltages on the maximum duty factor input DFM and the gain adjust output GA by applying a lower voltage to the modulation input MOD. This input may be used with an external control loop, e.g. for constant-current control, or to obtain a fold-back characteristic.

If the modulation input is not used, it should be connected to V_Z, pin 2.

Outputs QC and QE (pins 13 and 14)

To avoid double pulses that might occur at an excessively low mains voltage or an excessively high output current the output is preceded by a latch. The two outputs offer a choice of output current polarity, QC giving a positive current, i.e. a current flowing into the output, and QE giving a negative current, a current flowing out of the output. The two connections have the additional advantage that the relatively large output currents do not flow through the V_{CC} and V_{EE} connections, where they could induce noise.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (voltage source)	V_{CC}	−0,5 to +18	V
Supply current (current source)	I_{CC}	max. 30	mA
Feed-forward input voltage range			
$V_{CC} < 24$ V	V_{16-12}	0 to V_{CC}	V
$V_{CC} > 24$ V	V_{16-12}	0 to 24	V
Input voltage range (all other inputs)	V_I	0 to V_Z	V
Emitter output voltage range	V_{14-12}	0 to 5	V
Collector output voltage range	V_{15-12}	0 to V_{CC}	V
Output current			
d.c. (see Figs 3a, c and e)	$-I_{14}$; I_{15}	max. 40	mA
peak; t = max. 1 μs; duty factor d < 10%	$-I_{14}$; I_{15}	max. 200	mA
Storage temperature range			
TDA1060	T_{stg}	−40 to +125	°C
TDA1060A	T_{stg}	−40 to +125	°C
TDA1060B	T_{stg}	−40 to +125	°C
Operating ambient temperature range			
TDA1060	T_{amb}	−25 to +125	°C
TDA1060A	T_{amb}	0 to +70	°C
TDA1060B	T_{amb}	−55 to +150	°C
Power dissipation (see Figs 3b, d and f)	P_{tot}	max. 1	W

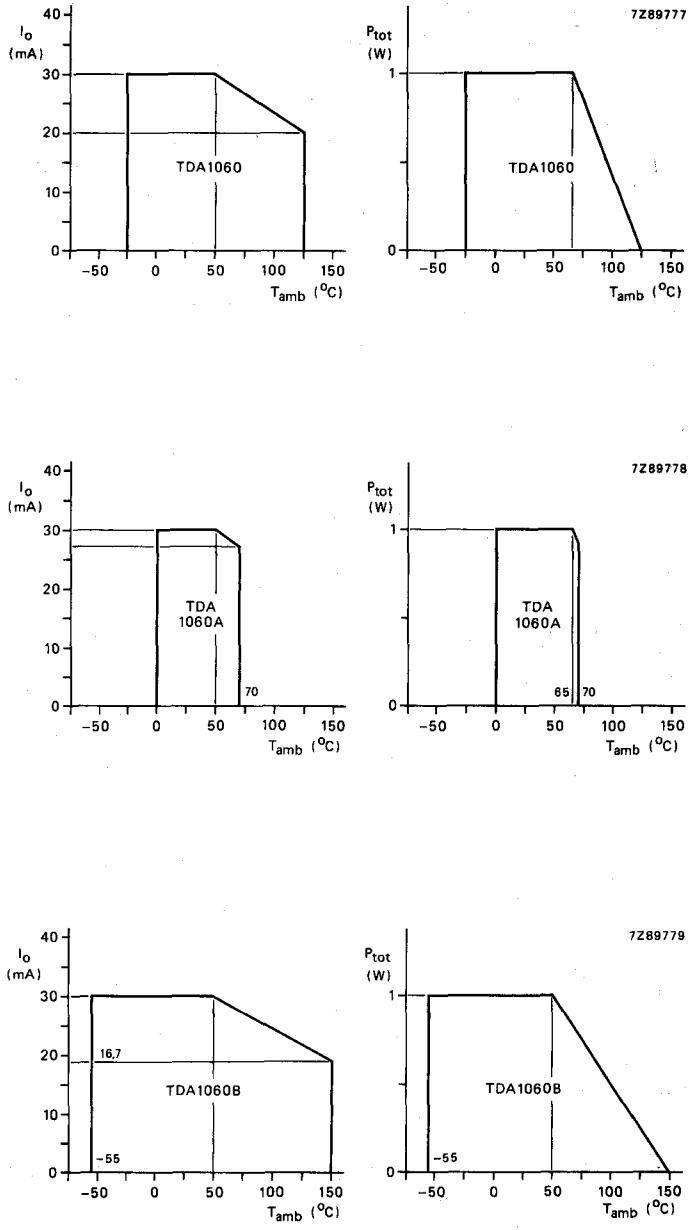


Fig. 3 Output current and power dissipation derating curves.

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = operating ambient temperature range, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Operating ambient temperature range					
TDA1060	T_{amb}	−25	–	125	°C
TDA1060A	T_{amb}	0	–	70	°C
TDA1060B	T_{amb}	−55	–	150	°C
Supply V_{CC} (pin 1)					
Supply voltage at I_{CC} = 15 mA					
TDA1060	V_{CC}	18,5	23	27	V
TDA1060A	V_{CC}	18,5	23	27	V
TDA1060B	V_{CC}	18	23	27,5	V
at I_{CC} = 30 mA					
TDA1060	V_{CC}	19,5	24	29	V
TDA1060A	V_{CC}	19,5	24	29	V
TDA1060B	V_{CC}	19	24	29,5	V
Supply current; R7 = 25 kΩ; duty factor d = 50%; I_Z = 0; at T_{amb} = 25 °C	I_{CC}	2,5	—	10	mA
over ambient temperature range	I_{CC}	2,5	–	15	mA
Threshold voltage of low supply voltage protection at T_{amb} = 25 °C	V_{CC}	8,85	–	10,8	V
Variation with temperature	$-\Delta V_{CC}/\Delta T$	–	7,5	–	mV/K
Hysteresis of low supply voltage protection	ΔV_{CC}	–	500	–	mV
Stabilized supply output V_Z (pin 2)					
Output voltage at T_{amb} = 25 °C	V_Z	7,5	8,4	9	V
Variation with temperature	$\Delta V_Z/\Delta T$	−1,5	–	+1,5	mV/K
Output current	$-I_Z$	–	–	5	mA
Feedback input FB (pin 3)					
Input voltage, feedback operation	$V_{3\text{-}12}$	2	–	V_Z-1	V
Input current at $V_{3\text{-}12}$ = 2 V	$-I_3$	1,5	12	35	μA
Internal reference voltage, measured at pin 3; pins 3 and 4 interconnected and grounded via a 100 nF capacitor; T_{amb} = 25 °C	V_{ref}	3,42	3,72	4,03	V
Variation with temperature	$\frac{\Delta V_{ref}/V_{ref}}{\Delta T}$	–	0,01	–	%/K
Variation with supply voltage	$\frac{\Delta V_{ref}}{\Delta V_{CC}}$	–	0,8	–	mV/V

parameter	symbol	min.	typ.	max.	unit
Long-term variation with time	$\pm\Delta V_{ref}/\Delta t$	–	2	–	μV/h
Threshold voltage of feedback loop short-circuit protection at T_{amb} = 25 °C	$V_{3\text{-}12}$	460	600	720	mV
Variation with temperature	$\frac{\Delta V_{3\text{-}12}/V_{3\text{-}12}}{\Delta T}$	–	0,01	–	%/K
Gain adjustment output GA (pin 4)					
Open-loop gain, pin 3 to pin 4	A_o	–	60	–	dB
External feedback resistor	$R_{3\text{-}4}$	10	–	–	kΩ
Modulator input MOD (pin 5)					
Input current at $V_{5\text{-}12}$ = 2 V; $V_{4;6\text{-}12} > 2$ V	$-I_5$	–	–	5	μA
Maximum duty factor input DFM (pin 6)					
Input voltage for limiting the duty factor to 50%; f_o = 10 to 100 kHz; $V_{16\text{-}12}$ = 0 V	$V_{6\text{-}12}$	–	0,4V_Z	–	V
Input current at $V_{6\text{-}12}$ = 2 V	$-I_6$	–	–	6	μA
Capacitor discharge current during fault condition	I_6	2,5	–	–	mA
Minimum output OFF time at C7 = 1,8 nF	t_{off}	–	1	–	μs
Variation of max. duty factor with temperature at f_o = 20 kHz and d_{max} = 50%	$\Delta d_{max}/\Delta T$	–	0,02	–	%/K
Internal biasing resistor to V_{EE} at $V_{3\text{-}12}$ = 0 V	$R_{6\text{-}12}$	0,75	1	1,25	kΩ
Synchronization input SYN (pin 9)					
Input voltage, sawtooth ON	V_{IH}	2	–	V_Z	V
sawtooth OFF: TDA1060; TDA1060A	V_{IL}	0	–	0,8	V
TDA1060B	V_{IL}	0	–	0,6	V
Input current at $V_{9\text{-}12}$ = 0 V	$-I_{IL}$	20	–	120	μA
External resistor connection RX (pin 7)					
External frequency adjustment resistor	R7	5	–	40	kΩ
External capacitor connection CX (pin 8)					
Sawtooth, upper level at $V_{16\text{-}12}$ = 0 V	$V_{8\text{-}12}$	–	5,7	–	V
lower level	$V_{8\text{-}12}$	–	1,3	–	V
Output pulse repetition frequency	f_o	0,05	–	100	kHz
Variation with temperature	$\frac{\Delta f_o/f_o}{\Delta T}$	–	0,01	–	%/K

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Feed-forward input FW (pin 16)					
Input voltage					
for $V_{CC} < 24$ V	V_{16-12}	0	–	V_{CC}	V
for $V_{CC} > 24$ V	V_{16-12}	0	–	24	V
Input current at $V_{16-12} = 16$ V; $V_{CC} = 18$ V; $T_{amb} = 25$ °C	I_{16}	–	–	60	μA
Frequency variation with input voltage at $V_{16-12} > 8$ V	$\frac{\Delta f_o/f_o}{\Delta V_{16-12}}$	–	1	–	%/V
Overcurrent protection input CM (pin 11)					
Input voltage	V_{11-12}	0	–	V_Z	V
Input threshold voltage for single pulse inhibit (current limit mode); $T_{amb} = 25$ °C	V_{T1}	370	480	575	mV
Ratio of threshold voltages for shut down/ slow start and for single pulse inhibit	V_{T2}/V_{T1}	–	1,25	–	
Threshold variation with temperature	$\Delta V/\Delta T$	–	60	–	μV/K
Input current at $V_{11-12} = 250$ mV	$-I_{11}$	–	–	10	μA
Turn-off delay, $I_{15} = 30$ mA; $V_{11-12} = 1{,}2 \times V_{T1}$	t_d	–	–	0,8	μs
Core saturation and overvoltage protection input SAT (pin 13)					
Input voltage	V_{13-12}	0	–	V_Z	V
Input threshold voltage at $T_{amb} = 25$ °C	V_{13-12}	460	600	720	mV
Threshold variation with temperature	$\Delta V/\Delta T$	–	60	–	μV/K
Input current at $V_{13-12} = 250$ mV	$-I_{13}$	–	–	7	μA
ENABLE input EN (pin 10)					
Input voltage					
ON	V_{IN}	2	–	V_Z	V
OFF: TDA1060; TDA1060A	V_{IL}	0	–	0,8	V
TDA1060B	V_{IL}	0	–	0,6	V
Input current at $V_{10-12} = 0$ V	$-I_{IL}$	20	–	120	μA
Outputs QC and QE (pins 14 and 15)					
Output current	$-I_{14}; I_{15}$	–	–	30	mA
Emitter output voltage	V_{14-12}	–	–	5	V
Collector output voltage at $V_{14-12} = 0$ V; $I_{15} = 30$ mA	V_{15-14}	–	–	400	mV

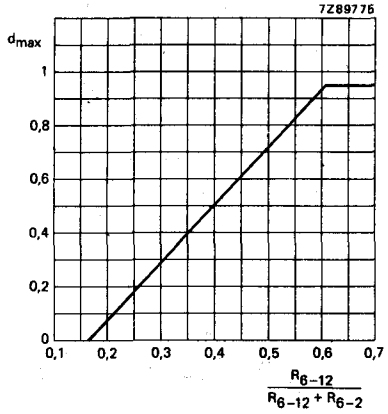


Fig. 4 Maximum duty factor d_{max} as a function of the voltage divider ratio at the duty factor input DFM.

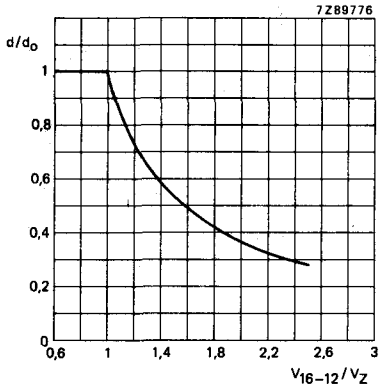


Fig. 5 Feed-forward regulation characteristic. Duty factor d as a function of the voltage V_{16-12} on the feed-forward input FW. d_o is the duty factor for $V_{16-12} \leqslant V_Z$.

APPLICATION INFORMATION

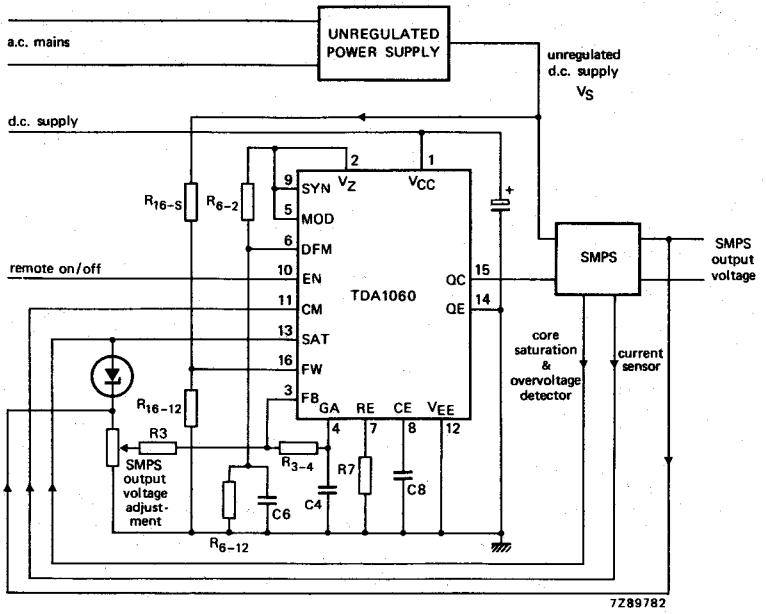


Fig. 6 Connections to the TDA1060 in a switched-mode power supply.

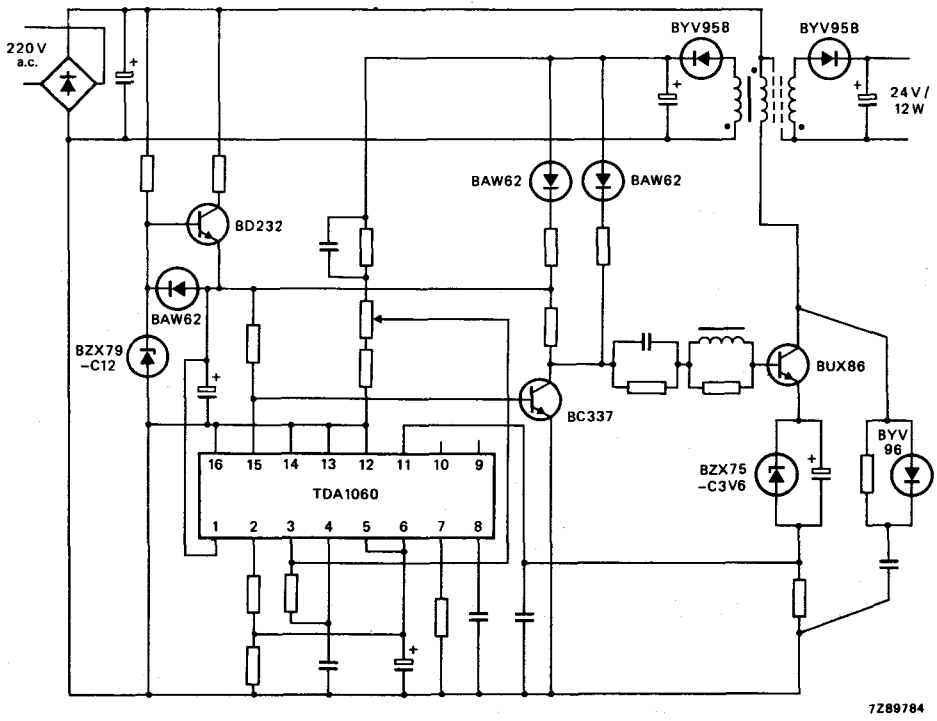


Fig. 7 Application of the TDA1060 in a 24 V, 12 W SMPS with flyback converter.

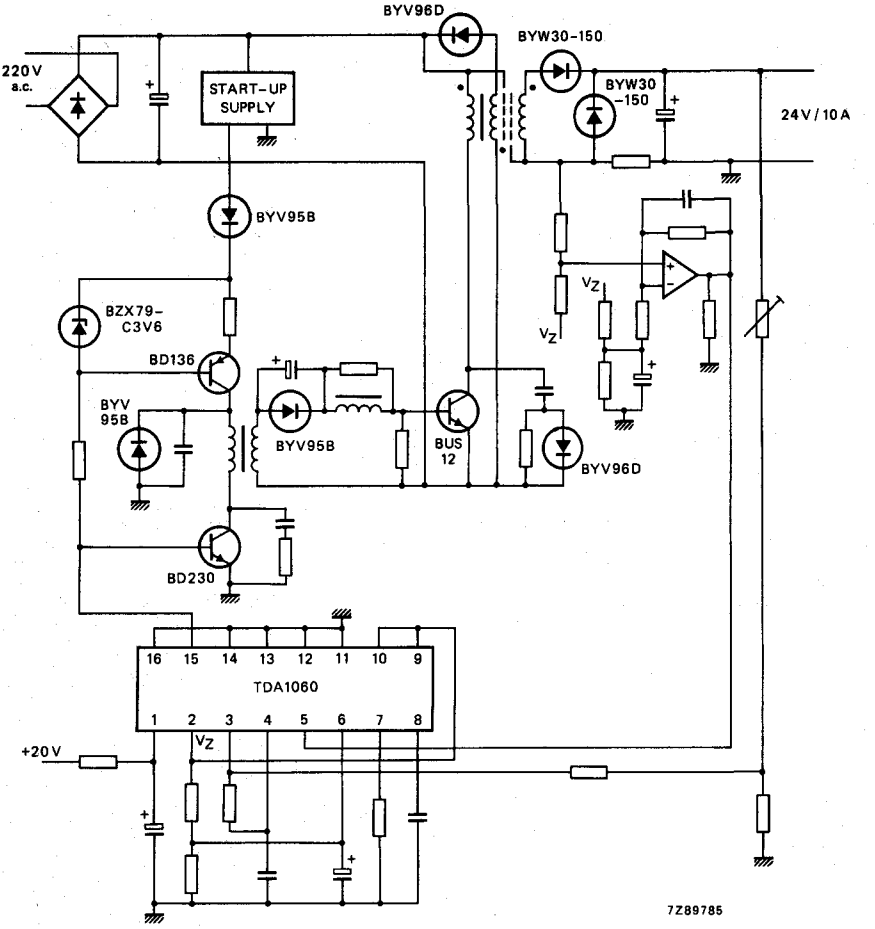


Fig. 8 Application of the TDA1060 in a 24 V, 240 W SMPS with forward converter.

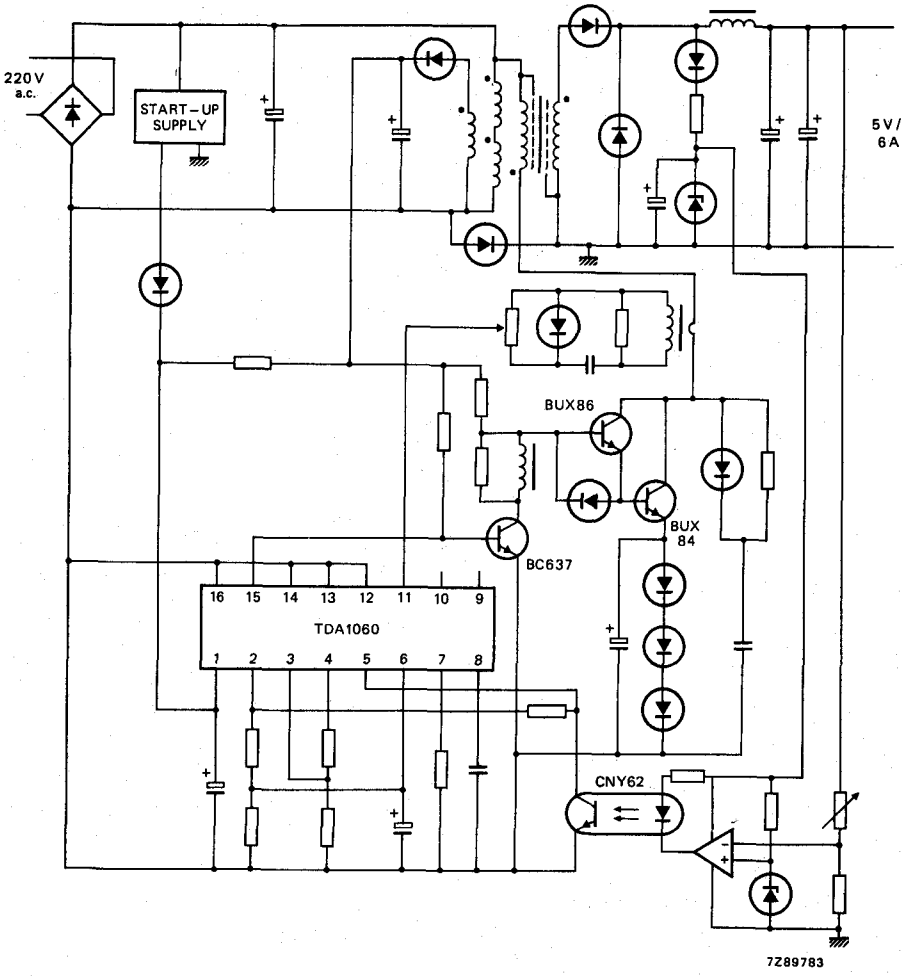


Fig. 9 Application of the TDA1060 in a 5 V, 30 W SMPS with forward converter and with an optocoupler CNY62 for voltage separation.

APPLICATION INFORMATION SUPPLIED UPON REQUEST.

SUPERSEDES DATA SHEET OF TDA1540

14-BIT DAC WITH 85 dB S/N RATIO

GENERAL DESCRIPTION

The TDA1540D is a monolithic integrated 14-bit digital to analogue converter (DAC). It incorporates a 14-bit input shift register with output latches, binary weighted current sources with switches and a reference source.

The IC features an improved switch circuitry which eliminates the need for a deglitcher circuit at the output. This results in a signal-to-noise ratio of typical 85 dB in the audio band.

QUICK REFERENCE DATA

Supply voltages				
pin 4	V_{P1}	typ.	5	V
pin 7	V_{N1}	typ.	−5	V
pin 11	V_{N2}	typ.	−17	V
Signal-to-noise ratio (full scale sine-wave) at analogue output (pin 22)	S/N	typ.	85	dB
Non-linearity at T_{amb} = −20 to + 70 °C		typ.	½ LSB	
Current settling time	t_{cs}	typ.	0,5	μs
Maximum input bit rate at data input (pin 1)	BR_{max}	min.	12	Mbit/s
Maximum clock frequency at clock input (pin 28)	$f_{cl\,max}$	min.	12	MHz
Full scale temperature coefficient at analogue output (pin 22)	TC_{FS}	typ.	$\pm 30 \cdot 10^{-6}$	K^{-1}
Operating ambient temperature range	T_{amb}		−20 to + 70	°C
Total power dissipation	P_{tot}	typ.	350	mW

PACKAGE OUTLINE

28-lead DIL; ceramic (cerdip); SOT-135A.

FUNCTIONAL DESCRIPTION

The binary weighted current sources are obtained by a combination of a passive divider and a time division concept. Figure 1a gives the diagram of one divider stage. The total emitter current 4 I of the passive divider is divided into four more or less equal output currents.

The output currents of the passive divider are now interchanged during equal time intervals generated by means of a shift register. The average output currents are exactly equal as a result of this operation. A ripple on the output current, caused by a mismatch of the passive divider, is filtered by an a.c. low-pass filter, requiring an external filter capacitor.

The outputs of the dividers are combined to obtain the output currents I ($\bar{I}_1$), I ($\bar{I}_2$) and 2I ($\bar{I}_3$) (see Fig. 1b). The current of the most significant bit is generated by an on-chip reference source. A binary weighted current network is formed by cascading the current division stages (see Fig. 2).

The interchanging pulses are generated by an on-chip oscillator and a 4-bit shift register. The binary currents are switched to the current output (pin 22) via diode-transistor switching stages; therefore, the voltage on the output pin must be 0 V ± 10 mV. The output current can be converted into a voltage by means of a summing amplifier.

Figure 3 represents the data input format, and an application circuit is given in Fig. 4.

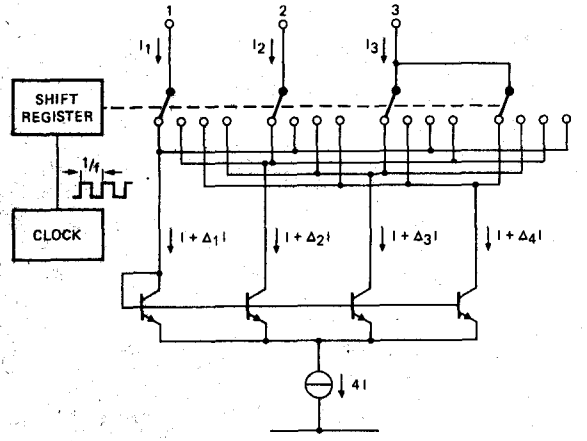


Fig. 1a Circuit diagram of one divider stage.

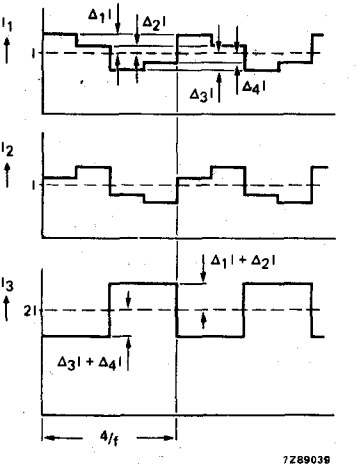


Fig. 1b Waveforms showing output currents I_1, I_2 and I_3 of Fig. 1a.

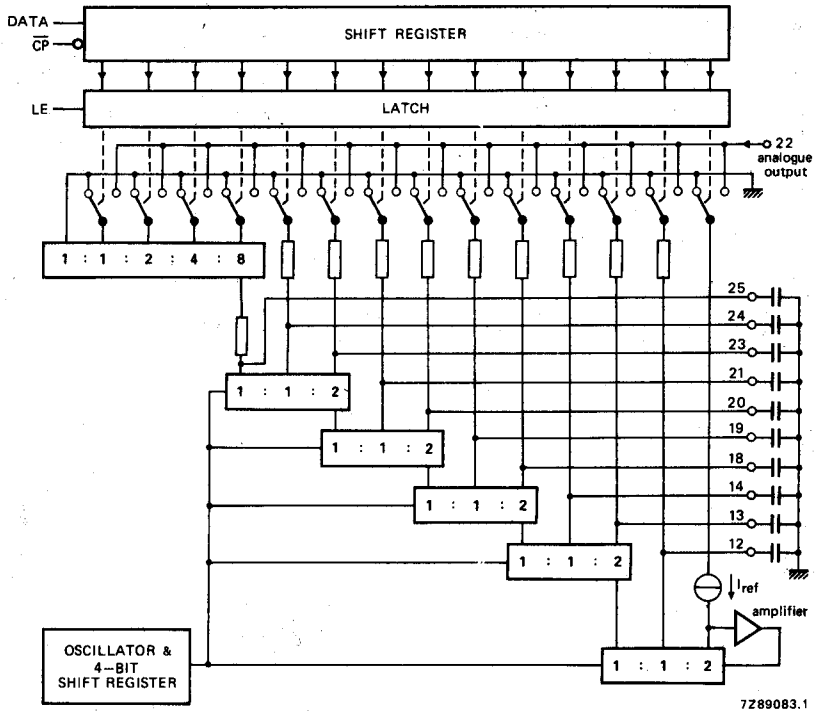


Fig. 2 Functional diagram showing cascading of current division stages.

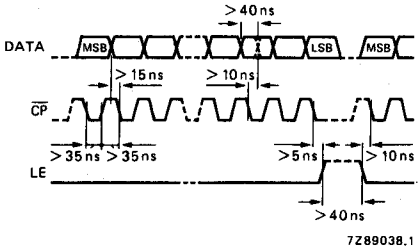


Fig. 3 Format of input signals.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages with respect to GND (pin 6)			
at pin 4	V_{P1}	max.	12 V
at pin 7	V_{N1}	max.	−12 V
at pin 11	V_{N2}	max.	−20 V
at pin 4 with respect to pin 11	$V_{P1}-V_{N2}$	max.	32 V
at pin 7 with respect to pin 11	$V_{N1}-V_{N2}$		−1 to + 20 V
Total power dissipation	P_{tot}	max.	600 mW
Storage temperature range	T_{stg}		−55 to + 125 °C
Operating ambient temperature range	T_{amb}		−25 to + 80 °C

CHARACTERISTICS (see application circuit Fig. 4)

T_{amb} = 25 °C; at typical supply voltages; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages with respect to GND (pin 6)					
at pin 4	V_{P1}	3	5	7	V
at pin 7	V_{N1}	−4,7	−5	−7	V
at pin 11	V_{N2}	−16,5	−17	−18	V
Supply currents					
at pin 4*	I_{P1}	–	12	14	mA
at pin 7	I_{N1}	–	−20	−24	mA
at pin 11	I_{N2}	–	−11	−13	mA
Power dissipation					
Total power dissipation	P_{tot}	–	350	410	mW
Temperature					
Operating ambient temperature range	T_{amb}	−20	–	+ 70	°C

* When the output current is $\frac{1}{2}I_{FS}$ ($\frac{1}{2}$ full scale output current).

parameter	symbol	min.	typ.	max.	unit
Data input DATA (pin 1)					
Input voltage HIGH	V_{IH}	2,0	–	7,0	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input current HIGH at V_{IH}	I_{IH}	–	–	50	μA
Input current LOW at V_{IL}	$-I_{IL}$	–	–	0,2	mA
Maximum input bit rate	BR_{max}	12	–	–	Mbits/s
Latch enable input LE (pin 2)					
Clock input $\overline{CP}$ (pin 28)					
Input voltage HIGH	V_{IH}	2,0	–	7,0	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input current HIGH at V_{IH}	I_{IH}	–	–	50	μA
Input current LOW at V_{IL}	$-I_{IL}$	–	–	0,2	mA
Maximum clock frequency	f_{CPmax}	12	–	–	MHz
Oscillator (pins 8 and 9)					
Oscillator frequency at C_{8-9} = 820 pF	f_{osc}	100	160	200	kHz
Analogue output I_{out} (pin 22)					
Output voltage compliance	V_{OC}	−10	–	+ 10	mV
Full scale current	I_{FS}	3,8	4,0	4,2	mA
Zero scale current	$\pm I_{ZS}$	–	–	100	nA
Full scale temperature coefficient T_{amb} = −20 to + 70 °C	TC_{FS}	–	$\pm 30 \times 10^{-6}$	–	K^{-1}
Settling time to ± ½LSB all bits on or off	t_{cs}	–	0,5	–	μs
Signal-to-noise ratio*	S/N	80	85	–	dB

DEVELOPMENT SAMPLE DATA

* Signal-to-noise ratio within 20 Hz and 20 kHz of a 1 kHz full scale sinewave, generated at a sample rate of 44 kHz.

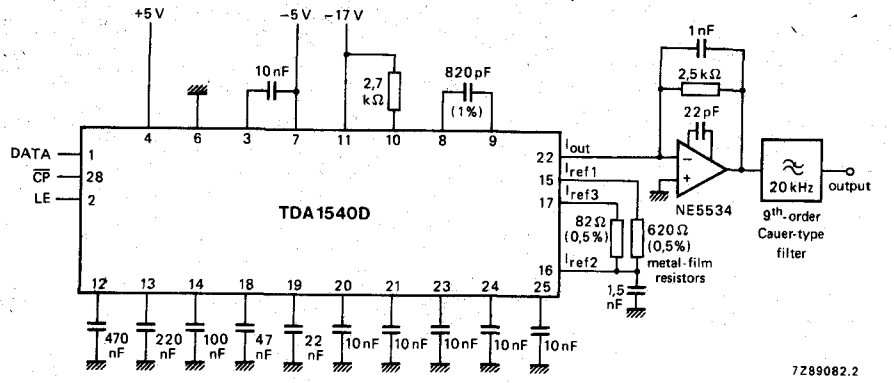


Fig. 4 Application circuit.

PINNING

1	DATA	data input
2	LE	latch enable input
3	V_{ref1}	voltage reference
4	V_{P1}	positive supply
5	i.c.*	frequency compensation on-chip operational amplifier
6	GND	ground
7	V_{N1}	negative supply
8	OSC1	oscillator capacitor
9	OSC2	
10	V_{ref2}	voltage reference
11	V_{N2}	negative supply
12	C1	decoupling binary weighted current sources
13	C2	
14	C3	
15	I_{ref1}	current reference sources
16	I_{ref2}	
17	I_{ref3}	
18	C4	decoupling binary weighted current sources
19	C5	
20	C6	
21	C7	
22	I_{out}	analogue output
23	C8	decoupling binary weighted current sources
24	C9	
25	C10	
26	i.c.*	voltage reference
27	i.c.*	voltage reference
28	$\overline{CP}$	clock pulse input

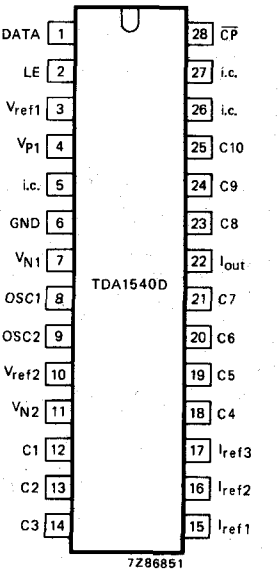


Fig. 5 Pinning diagram.

* i.c.: internally connected.

SEVEN-TRANSISTOR ARRAY

GENERAL DESCRIPTION

The TDA3081 is a bipolar integrated circuit consisting of seven common-emitter n-p-n transistors. The transistors are capable of driving loads up to 100 mA. This makes them particularly suited for driving light-emitting diodes and seven-segment displays. The transistor geometry is such that it reaches its maximum current gain at quite low currents, making the devices also suitable for small-signal applications.

QUICK REFERENCE DATA

Collector-base voltage (open emitter)	V_{CBO}	max.	18 V
Collector-emitter voltage (open base)	V_{CEO}	max.	18 V
Collector current (d.c.)	I_C	max.	100 mA
Power dissipation			
each transistor	P	max.	500 mW
total	P_{tot}	max.	750 mW

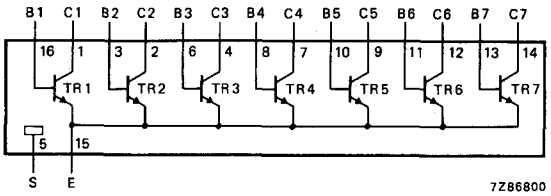


Fig. 1 Circuit diagram.

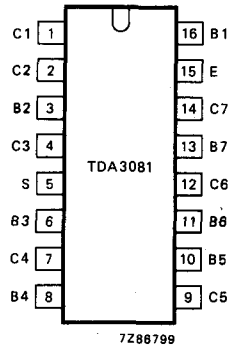


Fig. 2 Pinning diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38Z).

RATINGS

Limiting values in accordance with the Absolute Maximum Systems (IEC 134)

Each transistor			
Collector-emitter voltage (open base)	V_{CEO}	max.	18 V
Collector-base voltage (open emitter)	V_{CBO}	max.	18 V
Collector-substrate voltage (open base and emitter)	V_{CSO}	max.	18 V
Emitter-base voltage (open collector)	V_{EBO}	max.	6 V
Collector current (d.c.)	I_C	max.	100 mA
Base current (d.c.)	I_B	max.	20 mA
Power dissipation			
each transistor	P	max.	500 mW
total (see also Fig. 3)	P_{tot}	max.	750 mW
Storage temperature range	T_{stg}		−50 to + 125 °C
Operating ambient temperature range	T_{amb}		−40 to + 125 °C

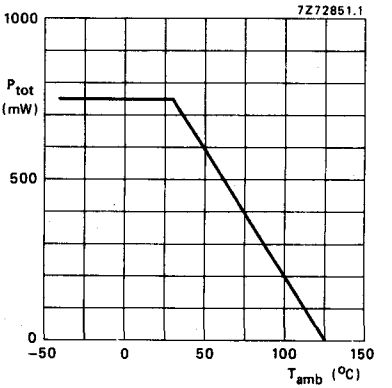


Fig. 3 Power derating curve.

OPERATING NOTE

As each collector forms a parasitic diode with the substrate, the substrate has to be connected to a voltage which is lower than any collector voltage. To minimize parasitic coupling between the transistors, this voltage should be signal ground.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Collector-emitter breakdown voltage at I_C = 1 mA; I_B = 0	$V_{(BR)CEO}$	32	–	–	V
Collector-substrate breakdown voltage at I_C = 1 mA; I_E = 0	$V_{(BR)CSO}$	50	75	–	V
Collector-base breakdown voltage at I_C = 100 μA; I_E = 0	$V_{(BR)CBO}$	50	75	–	V
Emitter-base breakdown voltage at I_E = 100 μA; I_C = 0	$V_{(BR)EBO}$	6,5	7,2	7,8	V
D.C. current gain					
I_E = 350 μA; V_{CE} = 5 V	h_{FE}	75	–	525	
I_E = 20 mA; V_{CE} = 5 V	h_{FE}	47	–	365	
Saturation voltage					
at I_C = 5 mA; I_B = 0,5 mA	V_{CEsat}	–	200	400	mV
at I_C = 50 mA; I_B = 5 mA	V_{CEsat}	–	400	840	mV

FIVE-TRANSISTOR ARRAY

GENERAL DESCRIPTION

The TDA3083 is a bipolar integrated circuit consisting of five n-p-n transistors. The transistors are capable of driving loads up to 100 mA. This makes them particularly suited for driving light-emitting diodes and seven-segment displays. The transistor geometry is such that it reaches its maximum current gain at quite low currents, making the devices also suitable for small-signal applications.

The transistors are partly matched, i.e. TR1 and TR2 form a matched pair, TR3 and TR4 also, and TR2 and TR5 likewise.

QUICK REFERENCE DATA

Collector-base voltage (open emitter)	V_{CBO}	max.	18 V
Collector-emitter voltage (open base)	V_{CEO}	max.	18 V
Collector current (d.c.)	I_C	max.	100 mA
Power dissipation			
each transistor	P	max.	500 mW
total	P_{tot}	max.	750 mW

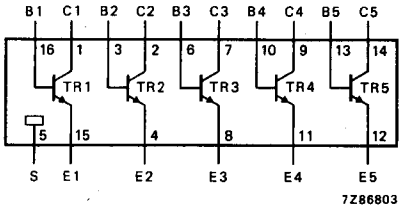


Fig. 1 Circuit diagram.

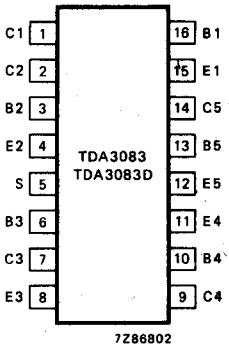


Fig. 2 Pinning diagram.

PACKAGE OUTLINE

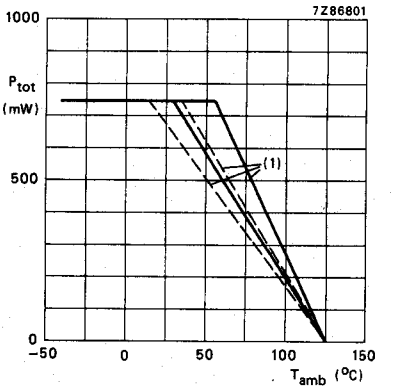
TDA3083 : 16 lead DIL; plastic (SOT-38Z).
TDA3083D: 16-lead mini-pack; plastic (SO-16; SOT-109A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Each transistor

Collector-emitter voltage (open base)	V_{CEO}	max.	18 V
Collector-base voltage (open emitter)	V_{CBO}	max.	18 V
Collector-substrate voltage (open base and emitter)	V_{CSO}	max.	18 V
Emitter-base voltage (open collector)	V_{EBO}	max.	6 V
Collector current (d.c.)	I_C	max.	100 mA
Base current (d.c.)	I_B	max.	20 mA
Power dissipation			
each transistor	P	max.	500 mW
total (see also Fig. 3)	P_{tot}	max.	750 mW
Storage temperature range	T_{stg}		−50 to + 125 °C
Operating ambient temperature range	T_{amb}		−40 to + 125 °C



(1) Derating curve for TDA3083D (SO-16; SOT-109A) mounted on a ceramic substrate of 50 x 50 x 0,7 mm with heatsink compound: $R_{th\ j\text{-}a}$ = 90 K/W; without heatsink compound: $R_{th\ j\text{-}a}$ = 120 K/W typical. Mounted on a printed-circuit board of 50 x 50 x 1,5 mm: $R_{th\ j\text{-}a}$ = 180 K/W.

Fig. 3 Power derating curves.

OPERATING NOTE

As each collector forms a parasitic diode with the substrate, the substrate has to be connected to a voltage which is lower than any collector voltage. To minimize parasitic coupling between the transistors, this voltage should be signal ground.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Collector-emitter breakdown voltage at I_C = 1 mA; I_B = 0	$V_{(BR)CEO}$	32	–	–	V
Collector-substrate breakdown voltage at I_C = 1 mA; I_E = 0	$V_{(BR)CSO}$	50	75	–	V
Collector-base breakdown voltage at I_C = 100 μA; I_E = 0	$V_{(BR)CBO}$	50	75	–	V
Emitter-base breakdown voltage * at I_E = 100 μA; I_C = 0	$V_{(BR)EBO}$	6,5	7,2	7,8	V
D.C. current gain					
I_E = 350 μA; V_{CE} = 5 V	h_{FE}	75	–	525	
I_E = 20 mA; V_{CE} = 5 V	h_{FE}	47	–	365	
Saturation voltage					
at I_C = 5 mA; I_B = 0,5 mA	V_{CEsat}	–	200	400	mV
at I_C = 50 mA; I_B = 5 mA	V_{CEsat}	–	400	840	mV
Input offset voltage at V_{CE} = 5 V; I_C = 1 mA					
any two transistors	V_{IO}	–	1	–	mV
matched pairs	V_{IO}	–	0,5	–	mV
Input offset current at V_{CE} = 5 V; I_C = 1 mA					
any two transistors	I_{IO}	–	2	–	μA
matched pairs	I_{IO}	–	0,5	–	μA

* Breakdown of the emitter-base junction causes degeneration of the current gain of the transistor.

13-BIT SERIES-PARALLEL CONVERTER

GENERAL DESCRIPTION

The TEA1017 is a bipolar integrated circuit intended to drive displays, triacs and relays. The data is serially shifted into the device and is stored in 13 latches that drive the outputs.

Features

- TTL and CMOS compatible inputs
- Outputs drive load in both directions
- Power-on reset makes outputs floating
- Wide supply voltage range

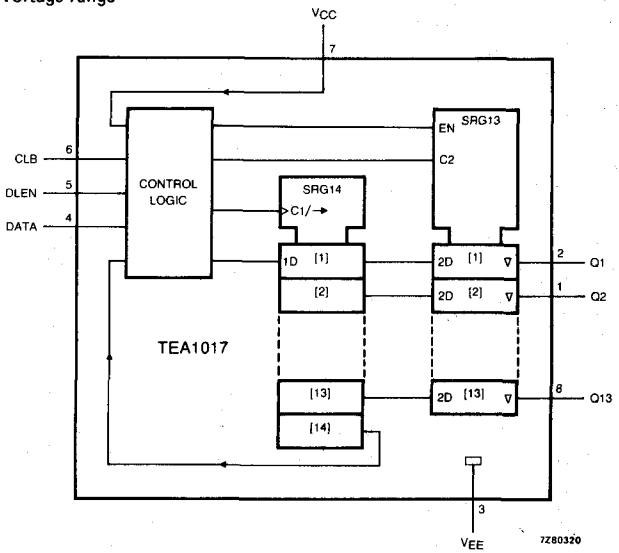


Fig. 1 Block diagram. The block marked SRG14 is a 14-bit shift register, the block marked SRG13 is an array of 13 latches.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		5 to 18 V
Output current, each output	I_{OL}; $-I_{OH}$	typ.	80 mA
Clock frequency	f_{CLB}	max.	50 kHz
Operating ambient temperature range	T_{amb}		−20 to +80 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

FUNCTIONAL DESCRIPTION

The control logic performs a key function in this device. It checks whether the input information has the correct format: a DLEN signal that has been HIGH for 14 clock pulses, and a DATA signal with its first bit LOW. When the format is found to be correct, the 15th clock pulse makes the control logic generate a signal that loads the content of the first 13 bits of the shift register into 13 latches. These drive the output stages.

Supply V_{CC} (pin 7)

The supply current of the TEA1017 is regulated internally. This permits the circuit to be used over a very wide range of supply voltages, viz. 5 to 18 V, with little variation of supply current.

The circuit has a power-on reset arrangement that resets the circuit and brings the outputs in a high-impedance state.
The power-on reset ends when a complete set of information has been received and is transferred to the latches, i.e. at the 15th HIGH-to-LOW transition of the clock pulse.

DATA input (pin 4)

The circuit requires input information on the DATA input consisting of 14 bits, the first bit being LOW. This information should be synchronous with the clock pulse. Data is loaded into the shift register at the HIGH-to-LOW transitions of the clock pulse.

Data line enable input DLEN (pin 5)

A HIGH level on the DLEN input enables the shift register. This HIGH level should have a duration of 14 clock pulses (see Fig. 3). After the DLEN input has returned to LOW the subsequent (15th) clock pulse transfers the content of the shift register to the latches and from there to the outputs.

Clock input CLB (pin 6)

The shift register shifts at the HIGH-to-LOW transitions of the clock pulse. The clock signal may be a continuously running clock or a clock burst of 15 clock pulses.

Outputs Q1 to Q13

The outputs are capable of supplying a load current in both directions, i.e. they can drive a load to the supply (V_{CC}) or to ground (V_{EE}). A load current to ground increases the supply current I_{CC} by the same amount.

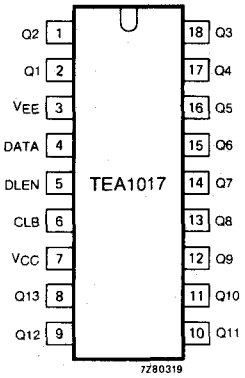


Fig. 2 Pinning diagram.

PINNING

1	Q2	output 2
2	Q1	output 1
3	V_{EE}	common
4	DATA	data input
5	DLEN	data line enable input
6	CLB	clock input
7	V_{CC}	positive supply
8	Q13	output 13
9	Q12	output 12
10	Q11	output 11
11	Q10	output 10
12	Q9	output 9
13	Q8	output 8
14	Q7	output 7
15	Q6	output 6
16	Q5	output 5
17	Q4	output 4
18	Q3	output 3

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	18 V
Input voltage range, all inputs	V_I	$-0,3$ to $V_{CC}+0,3$	V
Output current, all outputs			
HIGH	$-I_{OH}$	max.	150 mA
LOW	I_{OL}	max.	150 mA
Total power dissipation	P_{tot}	max.	1,4 W
Storage temperature range	T_{stg}	-40 to $+150$	°C
Operating ambient temperature range	T_{amb}	-20 to $+80$	°C

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS

V_{CC} = 5 to 18 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 7)					
Supply current					
during normal operation, unloaded					
at V_{CC} = 5 V	I_{CC}	–	45	60	mA
at V_{CC} = 18 V	I_{CC}	–	50	70	mA
during power-on reset, unloaded					
at V_{CC} = 5 V	I_{CC}	–	1,5	2	mA
at V_{CC} = 18 V	I_{CC}	–	5	7	mA
Clock input CLB (pin 6)					
Input voltage					
HIGH	V_{IH}	2	–	–	V
LOW	V_{IL}	–	–	0,4	V
Input current					
HIGH at V_{CLBH} = 2 V	I_{IH}	–	–	10	μA
LOW at V_{CLBL} = 0,4 V	$-I_{IL}$	–	–	10	μA
Clock pulse duration					
HIGH	t_{wH}	10	–	–	μs
LOW	t_{wL}	10	–	–	μs
DATA input (pin 4)					
Input voltage					
HIGH	V_{IH}	2	–	–	V
LOW	V_{IL}	–	–	0,4	V
Input current					
HIGH at V_{DATAH} = 2 V	I_{IH}	–	–	10	μA
LOW at V_{DATAL} = 0,4 V	$-I_{IL}$	–	–	10	μA
Data line enable input DLEN (pin 5)					
Input voltage					
HIGH	V_{IH}	2	–	–	V
LOW	V_{IL}	–	–	0,4	V
Input current					
HIGH at V_{DLENH} = 2 V	I_{IH}	–	–	10	μA
LOW at V_{DLENL} = 0,4 V	$-I_{IL}$	–	–	10	μA
Outputs Q1 to Q13					
Output voltage during normal operation					
HIGH at $-I_{OH}$ = 80 mA	V_{OH}	V_{CC} – 1,5	–	–	V
LOW at I_{OL} = 80 mA	V_{OL}	–	–	1	V
Output current during power-on reset					
HIGH	$-I_{OH}$	–	–	10	μA
LOW	I_{OL}	–	–	10	μA

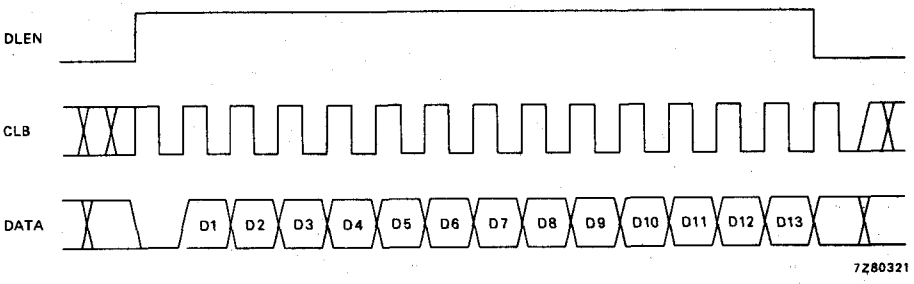


Fig. 3 Timing diagram.

CONTROL CIRCUIT FOR SWITCHED-MODE POWER SUPPLY

GENERAL DESCRIPTION

The TEA1039 is a bipolar integrated circuit intended for the control of a switched-mode power supply. Together with an external error amplifier and a voltage regulator (e.g. a regulator diode) it forms a complete control system. The circuit is capable of directly driving the SMPS power transistor in small SMPS systems.

It has the following features:

- Suited for frequency and duty factor regulation.
- Suited for flyback converters and forward converters.
- Wide frequency range.
- Adjustable input sensitivity.
- Adjustable minimum frequency or maximum duty factor limit.
- Adjustable overcurrent protection limit.
- Supply voltage out-of-range protection.
- Slow-start facility.

QUICK REFERENCE DATA

Supply voltage	V_{CC}	nom.	14 V
Supply current	I_{CC}	max.	13 mA
Output pulse repetition frequency range	f_o	1 Hz to 100	kHz
Output current LOW	I_{OL}	max.	1 A
Operating ambient temperature range	T_{amb}	−25 to +125	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

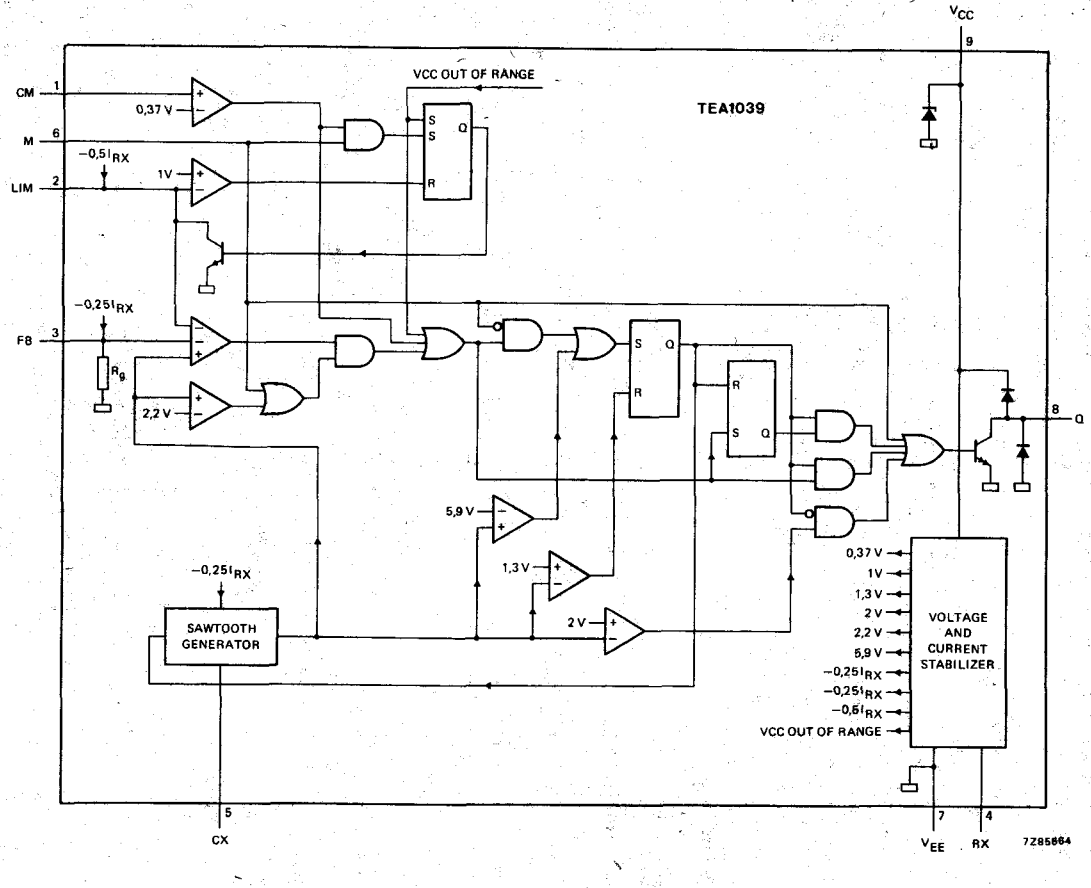


Fig. 1 Block diagram.

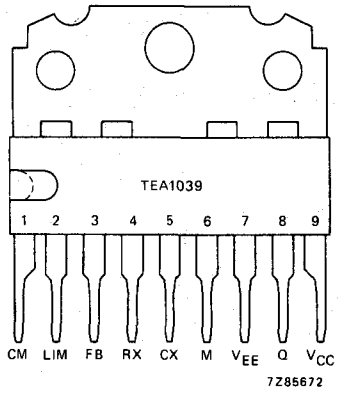


Fig. 2 Pinning diagram.

PINNING

1	CM	overcurrent protection input
2	LIM	limit setting input
3	FB	feedback input
4	RX	external resistor connection
5	CX	external capacitor connection
6	M	mode input
7	V_{EE}	common
8	Q	output
9	V_{CC}	positive supply connection

FUNCTIONAL DESCRIPTION

The TEA1039 produces pulses to drive the transistor in a switched-mode power supply. These pulses may be varied either in frequency (frequency regulation mode) or in width (duty factor regulation mode).

The usual arrangement is such that the transistor in the SMPS is ON when the output of the TEA1039 is HIGH, i.e. when the open-collector output transistor is OFF. The duty factor of the SMPS is the time that the output of the TEA1039 is HIGH divided by the pulse repetition time.

Supply V_{CC} (pin 9)

The circuit is usually supplied from the SMPS that it regulates. It may be supplied either from its primary d.c. voltage or from its output voltage. In the latter case an auxiliary starting supply is necessary.

The circuit has an internal V_{CC} out-of-range protection. In the frequency regulation mode the oscillator is stopped; in the duty factor regulation mode the duty factor is made zero. When the supply voltage returns within its range, the circuit is started with the slow-start procedure.

When the circuit is supplied from the SMPS itself, the out-of-range protection also provides an effective protection against any interruption in the feedback loop.

Mode input M (pin 6)

The circuit works in the frequency regulation mode when the mode input M is connected to ground (V_{EE}, pin 7). In this mode the circuit produces output pulses of a constant width but with a variable pulse repetition time.

The circuit works in the duty factor regulation mode when the mode input M is left open. In this mode the circuit produces output pulses with a variable width but with a constant pulse repetition time.

FUNCTIONAL DESCRIPTION (continued)

Oscillator resistor and capacitor connections RX and CX (pins 4 and 5)

The output pulse repetition frequency is set by an oscillator whose frequency is determined by an external capacitor C5 connected between the CX connection (pin 5) and ground (V_{EE}, pin 7), and an external resistor R_4 connected between the RX connection (pin 4) and ground. The capacitor C5 is charged by an internal current source, whose current level is determined by the resistor R4. In the frequency regulation mode these two external components determine the minimum frequency; in the duty factor regulation mode they determine the working frequency (see Fig. 4). The output pulse repetition frequency varies less than 1% with the supply voltage over the supply voltage range.

In the frequency regulation mode the output is LOW from the start of the cycle until the voltage on the capacitor reaches 2 V. The capacitor is further charged until its voltage reaches the voltage on either the feedback input FB or the limit setting input LIM, provided it has exceeded 2,2 V. As soon as the capacitor voltage reaches 5,9 V the capacitor is discharged rapidly to 1,3 V and a new cycle is initiated (see Figs 5 and 6).

For voltages on the FB and LIM inputs lower than 2,2 V, the capacitor is charged until this voltage is reached; this sets an internal maximum frequency limit.

In the duty factor regulation mode the capacitor is charged from 1,3 V to 5,9 V and discharged again at a constant rate. The output is HIGH until the voltage on the capacitor exceeds the voltage on the feedback input FB; it becomes HIGH again after discharge of the capacitor (see Figs 7 and 8). An internal maximum limit is set to the duty factor of the SMPS by the discharging time of the capacitor.

Feedback input FB (pin 3)

The feedback input compares the input current with an internal current source whose current level is set by the external resistor R4. In the frequency regulation mode, the higher the voltage on the FB input, the longer the external capacitor C5 is charged, and the lower the frequency will be. In the duty factor regulation mode external capacitor C5 is charged and discharged at a constant rate, the voltage on the FB input now determines the moment that the output will become LOW. The higher the voltage on the FB input, the longer the output remains HIGH, and the higher the duty factor of the SMPS.

Limit setting input LIM (pin 2)

In the frequency regulation mode this input sets the minimum frequency, in the duty factor regulation mode it sets the maximum duty factor of the SMPS. The limit is set by an external resistor R2 connected from the LIM input to ground (pin 7) and by an internal current source, whose current level is determined by external resistor R4.

A slow-start procedure is obtained by connecting a capacitor between the LIM input and ground. In the frequency regulation mode the frequency slowly decreases from f_{max} to the working frequency. In the duty factor regulation mode the duty factor slowly increases from zero to the working duty factor.

Overcurrent protection input CM (pin 1)

A voltage on the CM input exceeding 0,37 V causes an immediate termination of the output pulse. In the duty factor regulation mode the circuit starts again with the slow-start procedure.

Output Q (pin 8)

The output is an open-collector n-p-n transistor, only capable of sinking current. It requires an external resistor to drive an n-p-n transistor in the SMPS (see Figs 9 and 10).

The output is protected by two diodes, one to ground and one to the supply.

At high output currents the dissipation in the output transistor may necessitate a heatsink. See the power derating curve (Fig. 3).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range, voltage source	V_{CC}	−0,3 to +20	V
Supply current range, current source	I_{CC}	−30 to +30	mA
Input voltage range, all inputs	V_I	−0,3 to +6	V
Input current range, all inputs	I_I	−5 to +5	mA
Output voltage range	V_{8-7}	−0,3 to +20	V
Output current range			
output transistor ON	I_8	0 to 1	A
output transistor OFF	I_8	−100 to + 50	mA
Storage temperature range	T_{stg}	−55 to +150	°C
Operating ambient temperature range (see Fig. 3)	T_{amb}	−25 to +125	°C
Power dissipation (see Fig. 3)	P_{tot}	max. 2	W

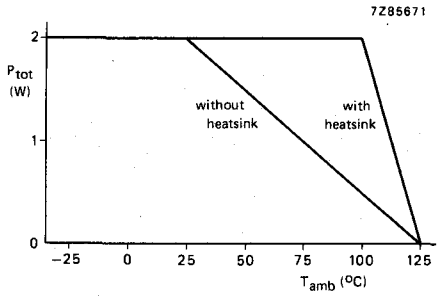


Fig. 3 Power derating curve.

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C unless otherwise specified

	symbol	min.	typ.	max.	unit
Supply V_{CC} (pin 9)					
Supply voltage, operating	V_{CC}	11	14	20	V
Supply current					
at V_{CC} = 11 V	I_{CC}	–	7,5	11	mA
at V_{CC} = 20 V	I_{CC}	–	9	12	mA
variation with temperature	$\frac{\Delta I_{CC}/I_{CC}}{\Delta T}$	–	–0,3	–	%/K
Supply voltage, internally limited at I_{CC} = 30 mA	V_{CC}	23,5	–	28,5	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	18	–	mV/K
Low supply threshold voltage	V_{CCmin}	9	10	11	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	–5	–	mV/K
High supply threshold voltage	V_{CCmax}	21	23	24,6	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	10	–	mV/K
Feedback input FB (pin 3)					
Input voltage for duty factor = 0; M input open	V_{3-7}	0	–	0,3	V
Internal reference current	$-I_{FB}$	–	0,5 I_{RX}	–	mA
Internal resistor R_g	R_g	–	130	–	kΩ
Limit setting input LIM (pin 2)					
Threshold voltage	V_{2-7}	–	1	–	V
Internal reference current	$-I_{LIM}$	–	0,25 I_{RX}	–	mA
Overcurrent protection input CM (pin 1)					
Threshold voltage	V_{1-7}	300	370	420	mV
variation with temperature	$\Delta V_{1-7}/\Delta T$	–	0,2	–	mV/K
Propagation delay, CM input to output	t_{PHL}	–	500	–	ns

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.	unit
Oscillator connections RX and CX (pins 4 and 5)					
Voltage at RX connection at $-I_4$ = 0,15 to 1 mA	V_{4-7}	6,2	7,2	8,1	V
variation with temperature	$\Delta V_{4-7}/\Delta T$	–	2,1	–	mV/K
Lower sawtooth level	V_{LS}	–	1,3	–	V
Threshold voltage for output H to L transition in F mode	V_{FT}	–	2	–	V
Threshold voltage for maximum frequency in F mode	V_{FM}	–	2,2	–	V
Higher sawtooth level	V_{HS}	–	5,9	–	V
Internal capacitor charging current, CX connection	$-I_{CX}$	–	0,25 I_{RX}	–	mA
Oscillator frequency (output pulse repetition frequency)	f_o	1	–	10^5	Hz
Minimum frequency in F mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Maximum frequency in F mode, initial deviation	$\Delta f/f$	−20	–	+20	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	−0,16	–	%/K
Output LOW time in F mode, initial deviation	$\Delta t/t$	−25	–	+25	%
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Pulse repetition frequency in D mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Minimum output LOW time in D mode at C_5 = 3,6 nF	t_{OLmin}	–	1	–	µs
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Output Q (pin 8)					
Output voltage LOW at I_8 = 100 mA	V_{8-7}	–	0,8	1,2	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	1,5	–	mV/K
Output voltage LOW at I_8 = 1 A	V_{8-7}	–	1,7	2,1	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	−1,4	–	mV/K

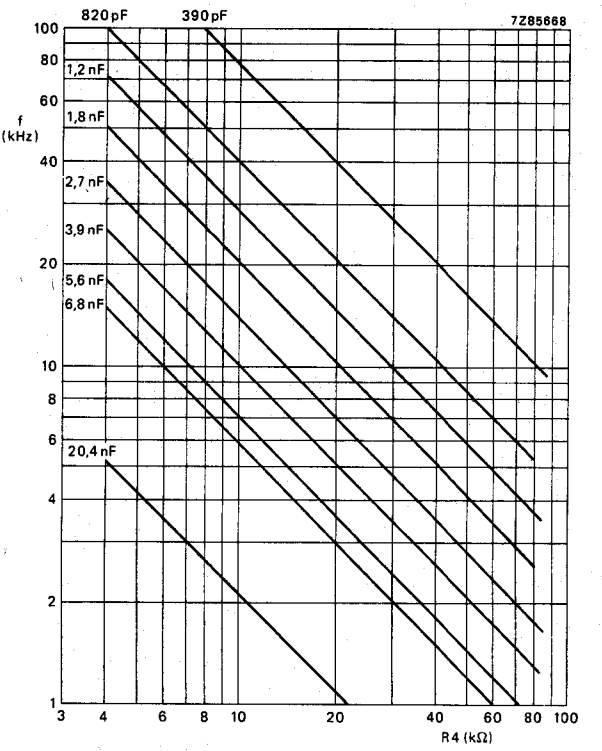


Fig. 4 Minimum pulse repetition frequency in the frequency regulation mode, and working pulse repetition frequency in the duty factor regulation mode, as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

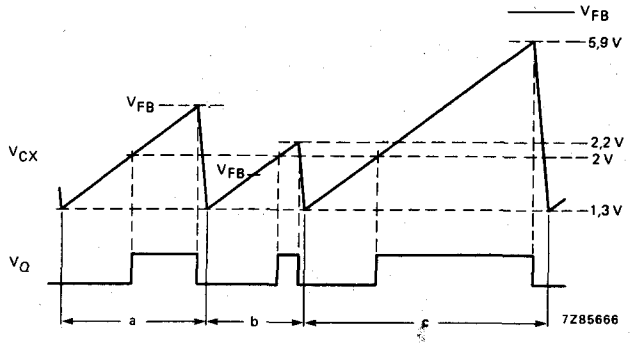


Fig. 5 Timing diagram for the frequency regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for three combinations of input signals. *a:* The voltages on inputs FB or LIM are between 2,2 V and 5,9 V. The circuit is in its normal regulation mode. *b:* The voltage on input FB or input LIM is lower than 2,2 V. The circuit works at its maximum frequency. *c:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit works at its minimum frequency.

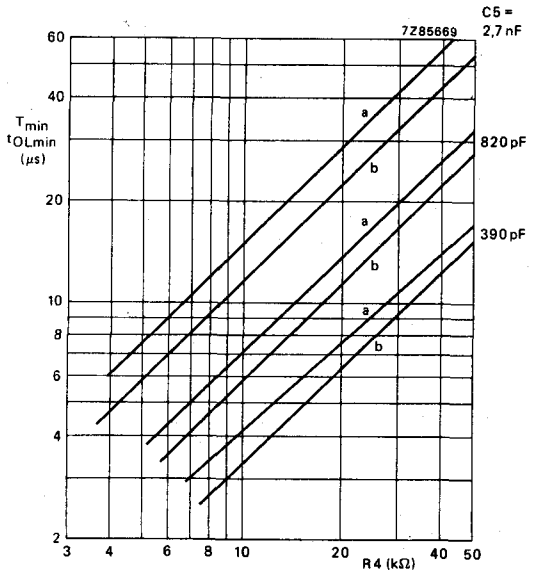


Fig. 6 Minimum output pulse repetition time T_{min} (curves a) and minimum output LOW time t_{OLmin} (curves b) in the frequency regulation mode as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

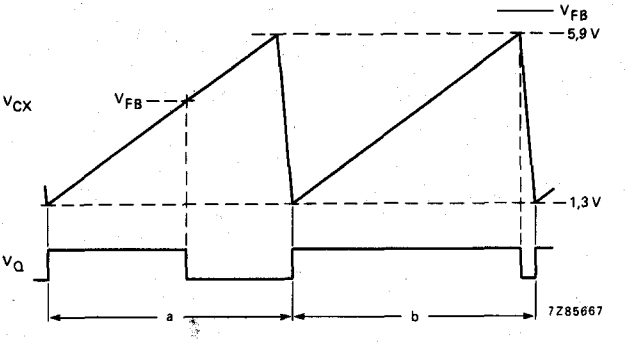


Fig. 7 Timing diagram for the duty factor regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for two combinations of input signals. *a:* The voltages on inputs FB or LIM are below 5,9 V. The circuit is in its normal regulation range. *b:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit produces its minimum output LOW time, giving the maximum duty factor of the SMPS.

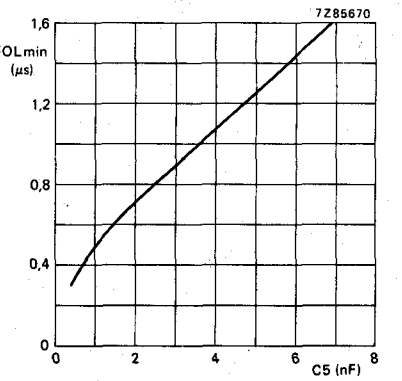


Fig. 8 Minimum output LOW time t_{OLmin} in the duty factor regulation mode as a function of external capacitor C5 connected between CX and ground. In this mode the minimum output LOW time is independent of R4 for values of R4 between 4 kΩ and 80 kΩ.

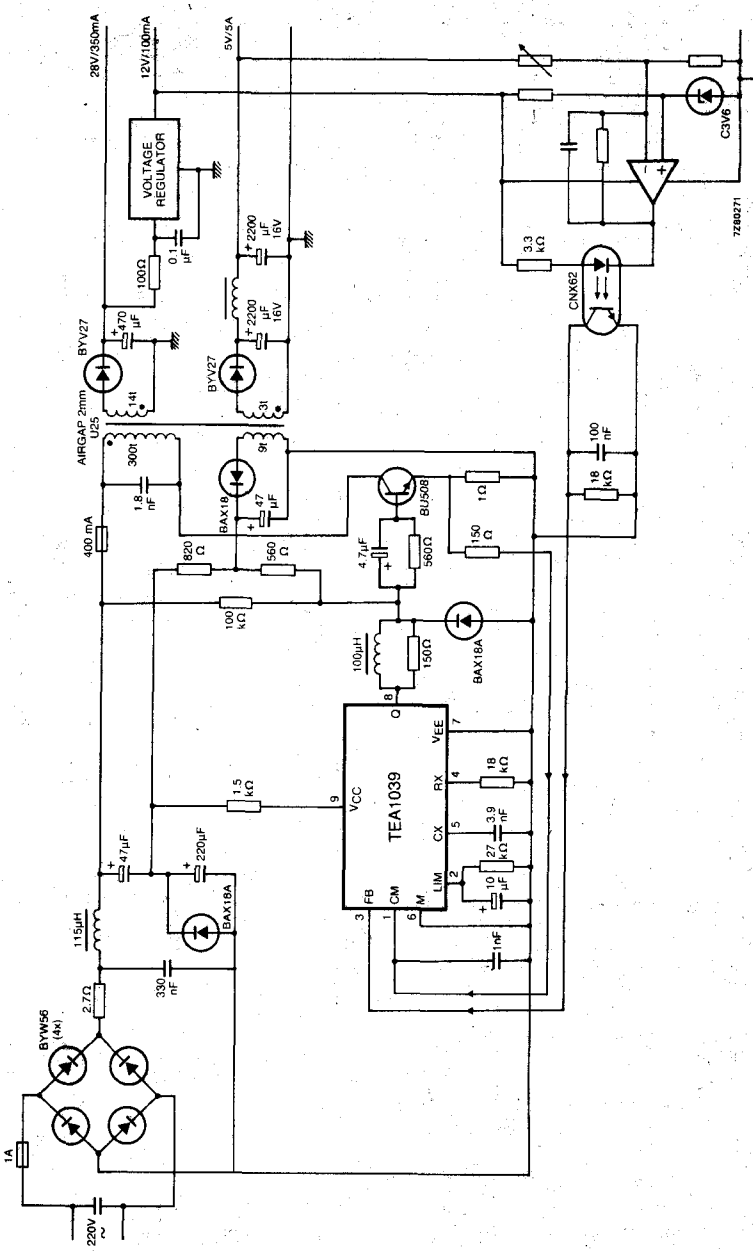


Fig. 9 Typical application of the TEA1039 in a variable-frequency flyback converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

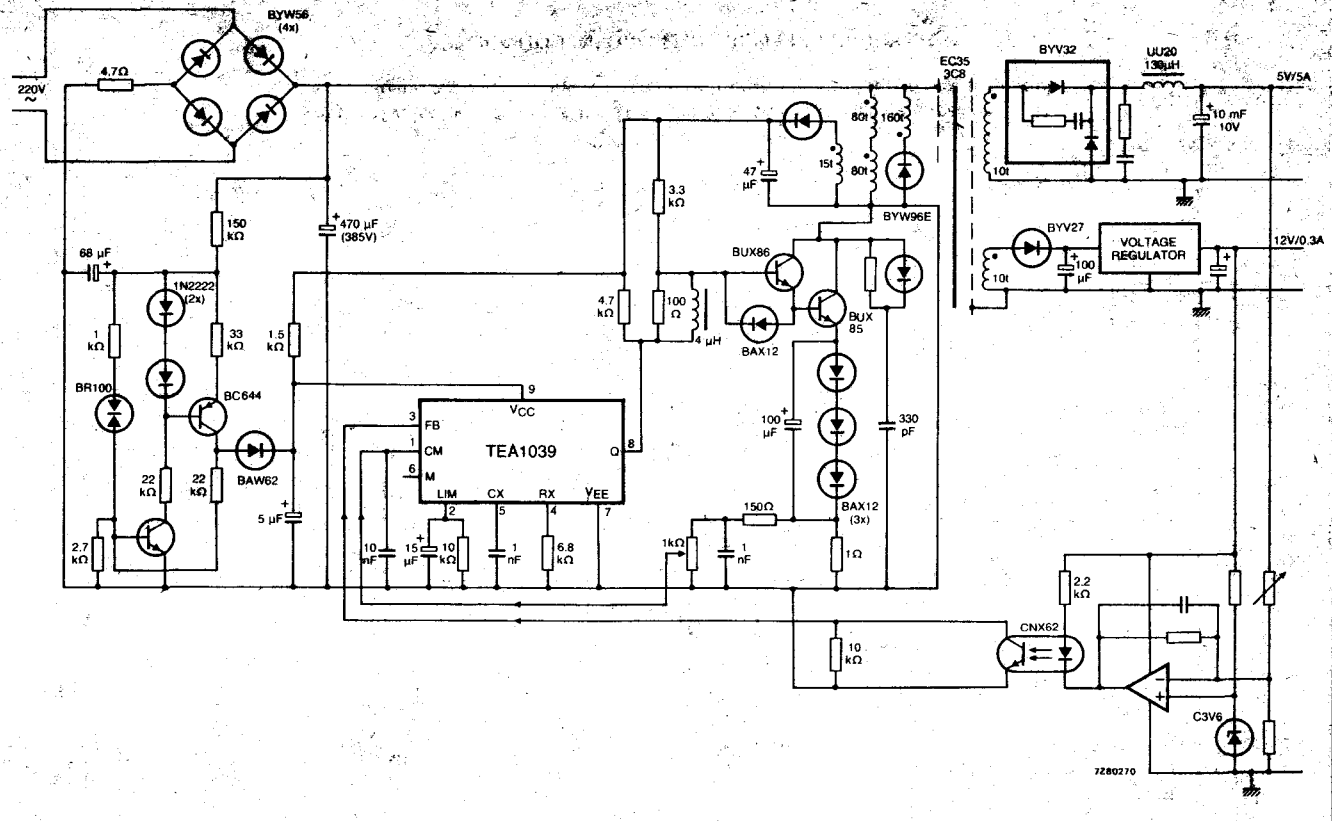


Fig. 10 Typical application of the TEA1039 in a fixed-frequency, variable duty factor forward converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

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