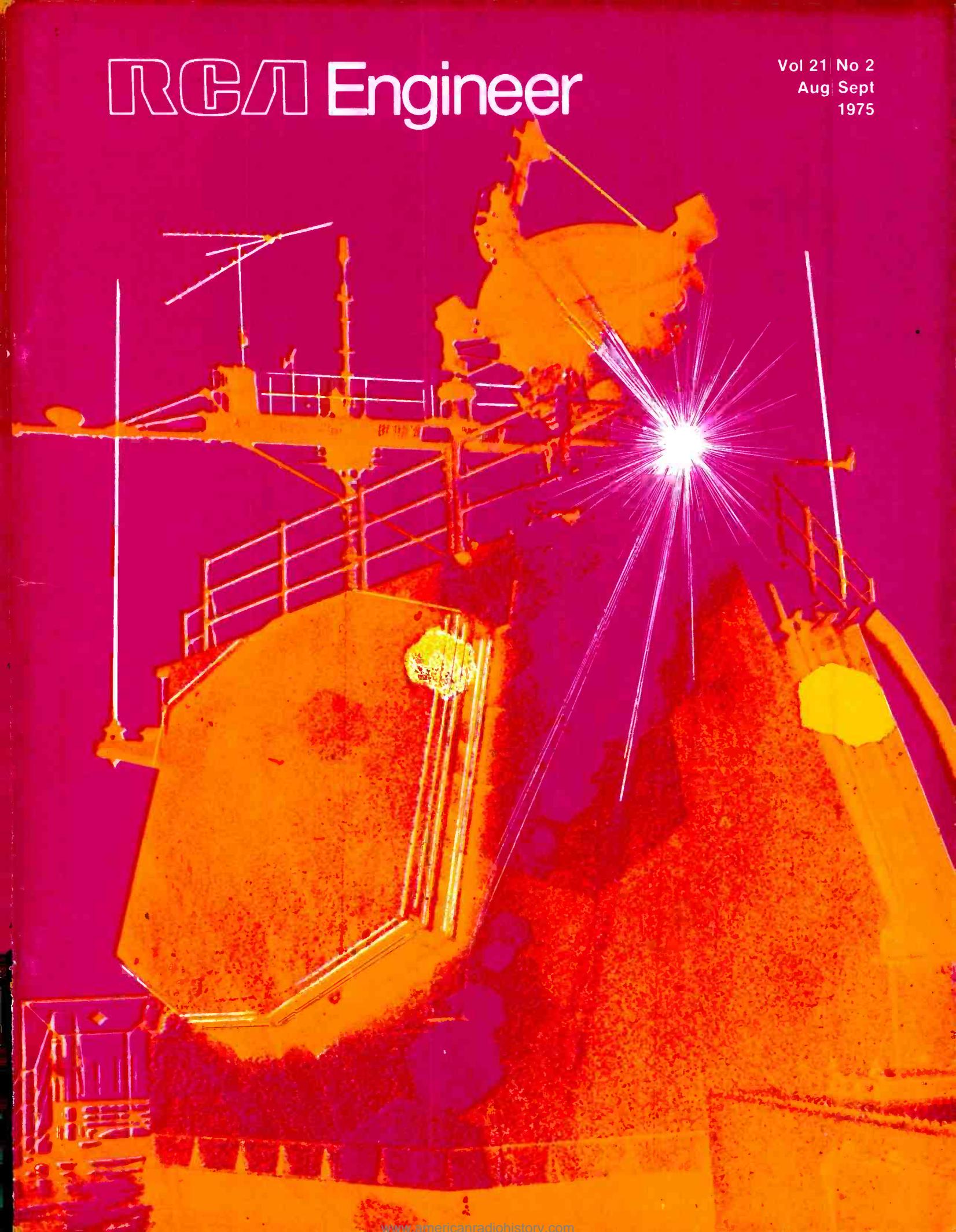


RCA Engineer

Vol 21 | No 2
Aug | Sept
1975



Our challenge

Challenge has always been an important part of the American success story in science and engineering. We thrive on it. It brings out our creative best. We proved it on the Manhattan Project, by going almost directly from a theoretical concept to an operating device in an unprecedented fashion. We also proved it with an incredible production output that caused our allies to refer to us admiringly as the Arsenal of Democracy.

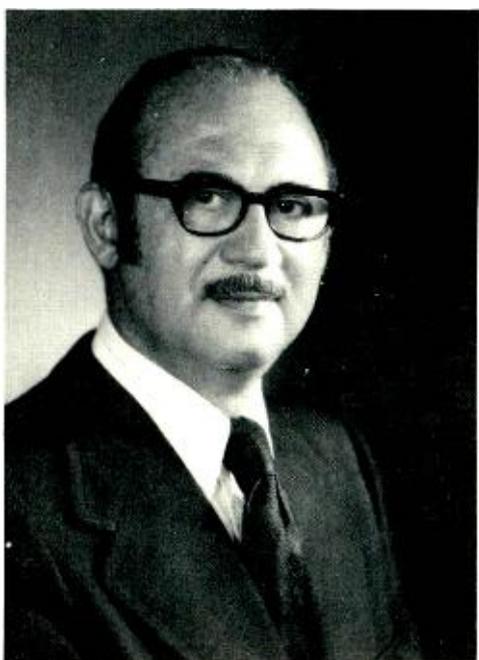
We proved it yet again by overcoming an early Russian lead in space technology to enable a U.S. astronaut to be the first man to walk on the moon.

Today we face greater challenges. In the past we could devote virtually unlimited resources to solving national problems. In today's environment, however, a \$20 billion Apollo Program would have scant likelihood of adoption. Present and prospective program cost has become a critical factor in national decision-making. The growth of "consumerism" has also increased the importance of cost and value in the commercial world.

For the past two years, "design-to-cost" has become a new Government catchword. This is part of a conscious effort to apply key aspects of commercial procurement practices to Government operations. While it is still merely a slogan to many, it inevitably will be a way of life. The pressures of inflation make this unavoidable.

In the past, an engineer could derive considerable satisfaction from devising a technically elegant solution to a problem. Today that may be counter-productive. What we need are simple, reliable, affordable solutions. "Design-to-cost" must be a driving force from the outset. Simply stated, our future depends on our ability to design and provide products and services with reasonable profits — at affordable prices.

It is as exciting and as serious a challenge as any our company or our country has ever faced. It is a challenge we can meet. We have to.



A handwritten signature in cursive that reads "Max Lehrer".

Max Lehrer
Division Vice President
and General Manager
Missile and
Surface Radar Division
Moorestown, N.J.



Our Cover

...is a posterization of the photo shown above, which was taken by Andy Whiting of MSRD on-board *USS Norton Sound* during AEGIS at-sea evaluation exercises. With the ship's superstructure and the sun as a background, Mr. Whiting photographed one phased-array face (the octagonal shape at the left) of the AN/SPY-1 phased-array radar system — the heart of AEGIS.

In sea trials aboard *USS Norton Sound* recently, the AEGIS System, using information gathered and processed by the AN/SPY-1, successfully intercepted six targets in six attempts. To complement the striking cover, Mr. Whiting has provided a photo essay of this at-sea evaluation exercise (p. 48).

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• To disseminate to RCA engineers technical information of professional value • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer • To serve as a medium of interchange of technical information between various groups at RCA • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions • To

help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field • To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

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editorial input

Typically, *RCA Engineer* issues emphasize specific themes — each supported by ten or twelve papers related topically to the subject of interest. The anniversary issue is the one exception; it contains representative papers from most RCA divisions and covers many different technologies.

This issue fits neither description: rather, it carries at least three areas of emphasis and several special features.

Energy problems and solutions introduce the issue. Dr. Moore (p. 3) critically examines the current literature and past studies to derive cost comparisons between photovoltaic energy sources and other more traditional sources of energy. Mr. Shelpuk (p. 10) also discusses solar energy conversion; however, the system he describes uses a collector to capture solar energy and transfer its heat to a medium (liquid or air) for heat transfer. Mr. Carver's message (p. 16) is that we will reduce fuel consumption when our vehicles — cars, trains, or planes — are running at peak efficiency, and that automatic checkout equipment can be a significant force in achieving that peak efficiency. Electronic devices and systems are certain to have a profound effect on future energy consumption for transportation. In this sense, Mr. Carver's message relates to the later discussion of automotive electronics by Messrs. Sanquini and Cohen (pp. 78 and 80).

The largest segment of papers — those related to computer-aided design and test (pp. 20 through 41) — is actually a legacy of two past *RCA*

about this issue

Engineer issues: Computer aided design (Vol. 20, No. 4) and Automatic Testing (Vol. 20, No. 6). These six papers — added to the forty or so from the past four issues — provide strong proof of the quantity and quality of effort underway in these areas throughout RCA.

A new feature of this issue is a photo essay (p. 48). Through a carefully arranged series of photos, Mr. Whiting captures the mood and activity aboard the *USS Norton Sound* while getting under way, preparing for missile launch, launching missiles, and returning to port — all in support of the AEGIS system checkout. One of the photos is the basis of the striking cover for this issue.

Other papers rounding out this issue represent several areas of intense interest at RCA, including space-related work, television, and radar. Mr. Jenny's summary of the RCA-MIT research conference (p. 42) highlights work in progress at MIT that may be of interest and is accessible to the RCA technical staff through the Industrial Liaison Program.

One significant observation about this issue is that there are probably more general-interest papers in this issue than in previous issues. This is a trend we hope to continue.

—J.C.P.

Future issues

The next issue of the *RCA Engineer* emphasizes automated manufacturing systems at RCA. Some of the topics to be covered are:

Productivity

Minicomputers and microprocessors in manufacturing

Semiconductor processing

Glass plant control

Automatic test systems

Wiring equipment

Discussions of the following themes are planned for future issues:

Product design

Palm Beach Division engineering

Meadow Lands engineering

NBC switching central

Automotive electronics

Optics, electro-optics, lasers

Cost predictions for photovoltaic energy sources

R.M. Moore

This paper critically examines solar-cell cost predictions, both in terms of a review and analysis of the prior literature and through an extension of these prior studies. The first step in this process is to use the existing market studies to establish a self-consistent system of "reasonable" assumptions. The second step is to analyze the prior studies in terms of the key assumptions, if any, which dominate the resulting cost predictions. Finally, the results of these first two steps are combined to form an alternative set of cost predictions which are based on a common framework of base-line input data. These alternative cost predictions are made for single-crystal Si cells (Czochralski vs. "ribbon" growth), current technology polycrystalline cells, and a "generalized" thin-film photovoltaic device

ONE of the more intriguing of the alternative energy sources under current study is the direct conversion of solar radiation to electrical energy via the photovoltaic effect; i.e., the use of the so-called "solar cell". The successful implementation of this technology for spacecraft and communication satellites, for example, has made this particular alternative popularly familiar and widely accepted as a technical reality. As a result, a significant level of government support has become available for the development of this technology. In addition, current forecasts indicate a substantial increase in this support will occur over the next five to ten years.

The photovoltaic effect can occur in any semiconductor p-n junction device. If optical radiation is able to penetrate into the interior of the device, then the absorption of light quanta (photons) by the semiconductor material generates hole-electron pairs. These mobile charge carriers are separated by the built-in electric field associated with the p-n junction structure. This effect is undesirable in conventional integrated-circuit and semiconductor-device technology, since the optically generated current acts as excess reverse current across the junction.

Solar cells, however, are designed to optimize this effect by providing maximum coupling of the available solar radiation into the p-n junction region or semiconductor base region. They typically have shallow junctions, very finely gridded top-contact-electrode patterns, and often utilize anti-reflection coatings

or other equivalent techniques to prevent excessive reflection losses at the semiconductor surface. When exposed to solar radiation, they behave essentially as current generators, delivering an output current proportional to the incident light intensity. The output voltage is relatively independent of the incident radiation intensity. The quality of a particular solar cell is usually characterized in terms of a conversion efficiency for standard solar radiation; i.e., the ratio of the electric power delivered at the terminals of the cell to the total incident solar radiation energy on the surface of the device—expressed as a percentage.

Although there is no doubt about the technical feasibility of photovoltaic solar-energy conversion, the potential of this technique as a significant terrestrial energy source is the subject of current debate. To be economically viable, the cost of photovoltaic devices must undergo a substantial decrease from the present level of capital investment per peak watt of generating capacity. Thus there are two fundamental, and essentially independent, questions that must be answered as part of any realistic appraisal of terrestrial photovoltaic solar-energy conversion:

- 1) What magnitude of cost reduction is required for photovoltaic energy sources to become commercially viable?
- 2) What basis exists for predicting the costs of solar cells in mass production, and do these estimates satisfy the criteria of commercial viability?

An acceptable answer to the first question can be based on an analysis of commercial energy source costs. This leads to

a series of estimated cost levels at which photovoltaic energy would be competitive with various established energy sources. Such an analysis can be extended to include predictions of market size at each of these cost levels; i.e., a price — demand curve can be generated. A number of studies of this type has led to various required-cost-level and market-size estimates.¹⁻⁴

There are two basically different methods for generating an answer to the second question. A very general estimate can be developed, without reference to specific processes or technologies, by the use of experience-curve concepts.¹⁷ This technique uses the base-line data of current costs and current cumulative volume to predict the future cost for a future cumulative volume level that is obtained from an independent market-growth estimate. The alternative approach is to assume a specific process or technology and use an economy-of-scale argument to develop a predicted cost at some future large-scale production level. Several prior studies have used one or both of these methods to predict future costs for single-crystal silicon⁵⁻¹⁰ and polycrystalline Cu_2S-CdS ¹⁰⁻¹⁴ solar cells.

Although a number of different types of solar cells are presently under active research on a world-wide basis, only two candidates are currently being developed

Dr. Robert M. Moore, Physical Electronics Research Laboratory, RCA Laboratories, Princeton, N.J., received the BSE, MSE and DSc from the George Washington University, where he held a NASA Pre-Doctoral Fellowship. His experience includes positions with Jansky and Bailey, Inc., the Naval Research Laboratory, and four years as an instructor and then assistant professor at the George Washington University. Since 1966, he has been a Member of the Technical Staff of the RCA Laboratories. He was awarded RCA Laboratories Outstanding Achievement Awards in 1969 and 1973. His primary interests are semiconductor device theory and photoeffects in semiconductors. Dr. Moore is a member of the IEEE, Tau Beta Pi, Sigma Pi Sigma, Sigma Tau and Theta Tau.

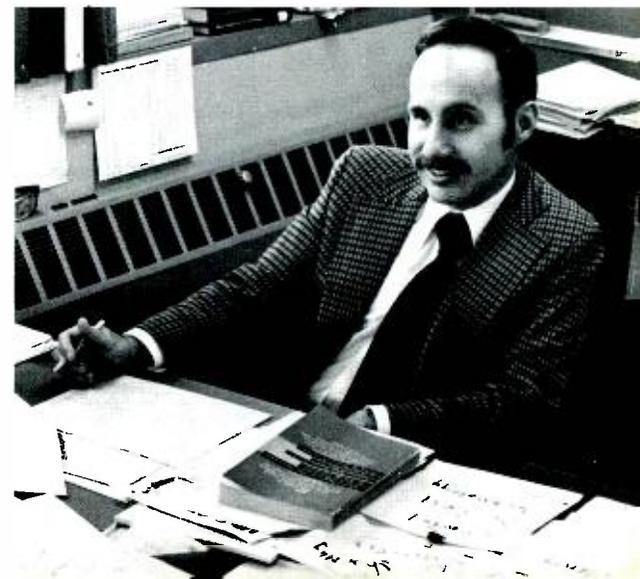


Table I — Some typical energy costs.

Primary sources	
• Central generating stations	1 to 5 cents/kWh
• Diesel engines/generators	5 to 15 cents/kWh
• Gasoline engines/generators	10 to 30 cents/kWh
• Dry-cell batteries	\$20 to \$100/kWh
Electrical storage	
• Lead-acid batteries	15 to 45 cents/kWh

on an intensive commercial basis. These two are a) *Si* solar cells utilizing conventional single-crystal *Si* wafers, and b) *Cu₂S-CdS* cells utilizing polycrystalline semiconductor layers.

Si cells are commercially available in an integrated array form at a cost of \$20/peak Watt, in quantity. They are based on a technology adapted for terrestrial application from the established space-satellite design. Current-design *Cu₂S-CdS* cells are based on a technology developed to a high degree in Europe during the last decade, following the earlier development programs in the U.S. There is a current commercial effort in the U.S. to produce *Cu₂S-CdS* cells on a large-volume-production scale.

The advocates of each of these competitive technologies are confident that the desired technological goals of peak efficiency, stability, and usable lifetime can be achieved. In addition, a high production yield is typically incorporated in detailed cost estimates, and the occurrence of significant technological breakthroughs is an integral part of long-range prediction; e.g., the use of low-cost "*Si* ribbon" for *Si* cells, and ultra-thin *CdS* layers for the *Cu₂S-CdS* devices. The primary commercial barrier foreseen is development of sufficient demand to justify the required large capital investment in solar cell production capacity.

An overview of the current state-of-the-art in solar-cell cost prediction is presented in Fig. 1. The cost range indicated for *Si* solar cells includes the use of both Czochralski wafer and "ribbon" single-crystal material.^{5-8,10} The spread indicated by the solid portion of the vertical line essentially includes current costs and estimates based on Czochralski wafers,^{8,10} and the dashed portion covers estimates based on "ribbon" substrates.^{5,6,7} For the *Cu₂S-CdS* cells, the solid portion of the vertical line covers the range accessible by current "state-of-

the-art" technology cells,^{10,11,12} and the dashed portion includes devices based on an "order-of-magnitude" reduction in *CdS* semiconductor thickness.^{13,14}

The cost estimates illustrated in Fig. 1 correspond generally to the production of an integrated solar-cell array or power module. Typically, such an integrated array would include internal series or parallel cell interconnection, array encapsulation, and array mechanical support. In use, a single array or assembly of standard arrays might be combined with specialized additional equipment needed for the particular application. The additional capital investment required for any support or shelter structures, power conditioning (e.g., dc-to-ac conversion), energy storage, and control functions utilized in the specific application are, of course, not included in the estimated manufacturing cost of the arrays.

The right-hand margin of Fig. 1 provides some context for judging the significance of the capital cost estimates indicated for *Si* and *Cu₂S-CdS* solar cells. First, the nominal cost per peak kW associated with the market demand predictions for the years of 1977, 1985, and 2000 are indicated, and are considered in more detail in the following discussion of the *future market environment*. Second, two ranges of capital cost are presented and are labeled with specific competitive electrical power sources. The origin of these cost range estimates requires some clarification for full understanding.

Since the input solar energy is available "free of charge", the cost of solar-cell-

generated electric power is based entirely on the capital investment required to convert and make available the output energy. In addition to the basic cost of the solar-cell arrays, there may be associated structural, storage, power conditioning, and control function costs. The true cost of solar-cell-generated power is determined by this total supply system cost, the cost of capital, the expected lifetime (amortization period) for the various system components, the load factor (~ 20%) for solar energy conversion, maintenance costs, etc.

The range of competitive cost levels indicated in Fig. 1, and identified with specific commercial sources, represents the total system cost per peak kW capacity at which a solar energy system would be commercially viable on the basis of cost per kWh of energy delivered. It does not represent the capital cost per kW capacity of the gasoline and diesel generators or central power stations, where factors such as fuel cost or very high load factor are dominant features of any cost analysis.

Future system concepts and applications proposed for photovoltaic energy sources range from simple sub-kW modules supplying irrigation water pumping power on an as-available basis to huge multi-square-mile solar stations integrated with a national power distribution system and supplying demand power from large-scale energy-storage facilities. The single element which is common to these dramatically differing views of the future is the need for integrated arrays of solar cells produced at a cost, and on a scale, commensurate with the required overall systems costs of the specific application. It is this common-core building block, the solar cell array, that is the subject of interest in this paper.

The wide range covered by the solar-cell cost estimates presented in Fig. 1 is rooted in the basic assumptions made for each of the cost estimates in terms of input parameters such as production volume, raw materials costs, and extent of vertical integration. For example, the production rates span a ratio of > 10⁶ between the lowest and highest rates assumed for the estimates of Fig. 1.^{5,6,10}

As a result of the extreme diversity in these fundamental assumptions, it is quite difficult to assign a relative credibility or confidence level to the individual predictions. Thus, both the

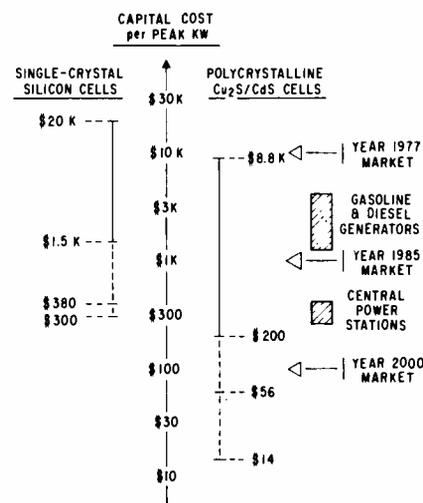


Fig. 1 — Current status of solar-cell cost-prediction art.

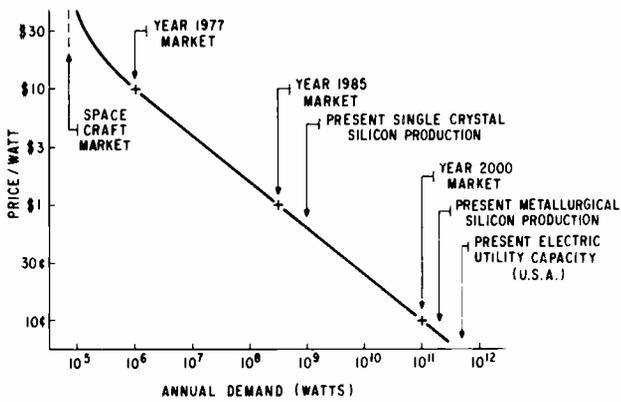


Fig. 2 — Price—demand curve.

advocates and opponents of the general technique of photovoltaic conversion, and of specific approaches to this technology, are free to choose the estimate best suited to their individual viewpoint. This also allows the absurd situation in which contemporary evaluations of the feasibility of photovoltaic energy sources can proceed from base-line economic data that differ by several orders-of-magnitude.

Future market environment

An extrapolation from current solar-cell costs to future large-scale production costs requires a number of basic assumptions or hypotheses about the parameters of the future markets; e.g., competitive prices, demand levels, and growth rates. Much of the dramatic spread in existing capital-cost estimates (illustrated in Fig. 1) is traceable to drastically different assumptions about the nature of this future market environment.

A particular market environment is presented here for use as a conceptual framework within which the credibility of any particular cost estimate can be judged. The plausibility of this particular hypothesis rests primarily on its self-consistency when tested by *pro forma* experience-curve concepts.

Table 1 presents a range of commercial energy costs in current dollars.^{1,4,15} The primary energy sources that are shown group naturally into three distinct cost levels: 1) central generating stations, 2) diesel and gasoline engine generators, and 3) dry-cell batteries.

The estimated cost of storage per kWh in lead-acid batteries is also shown in Table I. At present prices, photovoltaic energy

systems using lead-acid battery storage have been able to penetrate certain specialized application areas previously served by the very expensive dry-cell energy sources.³ This application represents the only significant terrestrial market, at present, for solar-cell energy sources.

On the basis of the energy costs shown in Table 1, an estimate can be made of capital cost per kW at which photovoltaic cells would become competitive with each of the specific alternative sources.^{1,2,4,9} If these data are combined with estimates of the market size available to penetration by solar cells at each such cost level, then a price—demand curve can be generated.

An example of a particular price—demand curve obtained by this procedure is given in Fig. 2.⁴ In addition to the essential price—demand relationship shown, an additional context is provided by indicating chronological milestones, current material-usage benchmarks, and the present US electric utility capacity.

The material-usage benchmarks are for present single-crystal Si production,^{2,5,9,10} and for present metallurgical grade (> 99% pure) Si production.^{9,10} These benchmarks suggest the comparative impact that the various levels of solar-cell demand will have in relation to current non-photovoltaic Si use, assuming that Si is the dominant solar-cell material. The material-usage benchmarks refer only to the horizontal axis; i.e., they represent the approximate area that could be covered by 200- μ m and 100- μ m thick layers at the present volume of single-crystal and metallurgical Si, respectively. This is of course translated into peak watts of generating capacity by assuming a particular conversion efficiency and peak insolation (10% and 1kW/m² for Fig. 2).

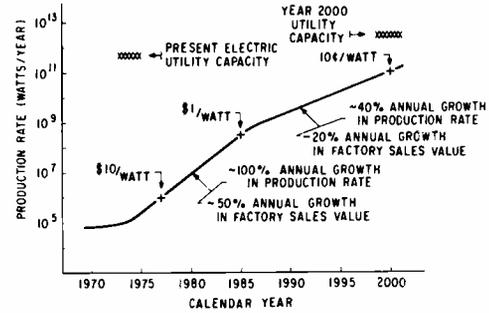


Fig. 3 — Growth rates.

The intersection of these benchmark quantities with the price—demand curve does not have any significance with respect to price or cost levels.

The impact of various demand levels relative to national energy needs is shown by comparison with the present US electric utility capacity.¹⁵ Finally, a set of chronological milestones are provided for the price—demand relation expected in 1977,³ 1985,⁴ and the year 2000.^{2,9}

The interrelation of this particular chronology with the resulting production growth rate is illustrated in Fig. 3. In this Figure, the benchmarks are provided in terms of price levels at certain specific times, the current electric utility capacity, and the electric utilities capacity estimated for the year 2000.¹⁵ Two distinct periods of production growth are identified: the periods 1975 to 1985, and 1985 to 2000. Both periods are assumed to have exponential growth in production, but the rate of growth differs. The indicated annual growth rate in factory sales value for these two periods is determined by the interaction between

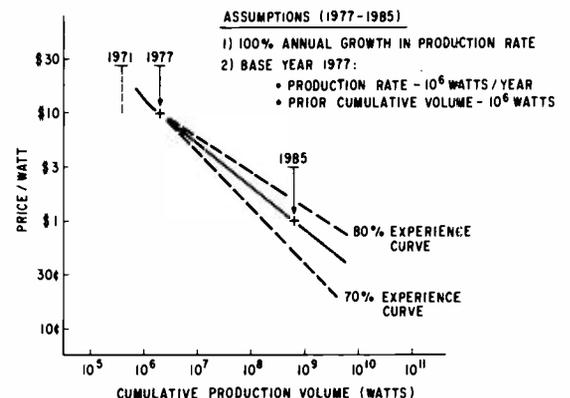


Fig. 4 — Experience-curve extrapolation.

the rate of production and the indicated variation in price per unit production.

Fig. 4 illustrates the use of the experience-curve concept to test the particular combination of price, annual production rate, and production-rate growth presented in Figs. 2 and 3. With the base-year assumptions indicated in Fig. 4, a 75% experience curve can represent the 1977-85 period quite adequately. Experience curves in the 70 to 80% range are typical of device fabrication and *Si* crystal growth for the semiconductor industry.^{6-9,17}

On this basis, the future-market environment used to test the credibility of existing cost estimates is that summarized in Fig. 2. This base-line data is used as the fundamental framework for the alternative set of cost estimates presented in this paper.

Cost prediction models

A review of the existing cost-prediction studies for photovoltaic energy sources reveals that none of these studies relies solely on the use of experience-curve concepts to estimate future costs.⁵⁻¹⁴ In several cases, the experience-curve argument is used as a plausibility test, but the predominant cost-prediction model relies on an economy-of-scale principle referred to here as the *mass-production assumption*.

Not all of the prior cost estimates supply sufficient detail to permit detection of the underlying assumptions or principles. However, an analysis of those references that can support a detailed dissection reveals a consistent pattern. The most fundamental aspect of this pattern is

illustrated in Fig. 5.^{5,6,10-13} In this Figure, the estimated direct or raw-materials cost is expressed as a percentage of the total estimated factory cost and is presented as a function of declining factory cost. These data show the recurring assumption that when unit cost declines (i.e., as the scale of production increases), then raw materials become the dominant cost element. This is the most general form of the mass-production assumption.

For the particular case of solar-cell cost estimates under study here, a more specialized form of this model has evolved. A further analysis of the existing cost estimates shows that there is a consistent assumption about the major component within the total raw-materials cost. This assumption is illustrated in Fig. 6.^{5,6,10,13} Here the estimated materials cost for the semiconductor-plus-substrate is expressed as a percentage of total materials cost, and presented as a function of declining total unit cost. The data clearly show that the lowest cost-per-watt estimates assume that the direct materials cost for the semiconductor-plus-substrate essentially equals, and thus replaces, the total direct materials cost.

This is the specialized form of the mass-production assumption as used for photovoltaic cost estimation.

The concept of a semiconductor-plus-substrate entity has been introduced here on the basis that it is a generalization of the function that the single-crystal *Si* wafer, or ribbon, performs for the standard *Si* solar cell. This entity allows the analysis to be extended to include the polycrystalline *Cu₂S-CdS* solar cell, where the major semiconductor layer (i.e., *CdS*) and substrate (e.g., plastic,

metal foil, glass) are physically separate materials, as well as a generalized thin-film cell.

To summarize, it has been illustrated that for the solar-cell cost estimates of primary importance in large-scale applications (i.e., cost-per-watt < \$1) the fundamental assumption is that ~75% of the factory cost is attributable to the direct materials cost for the substrate — semiconductor combination alone. Thus, the primary question that must be examined in establishing a confidence level for these existing predictions is the credibility of the basic estimates for the semiconductor-plus-substrate cost. The overall prediction for cell cost can be no better than the underlying estimate for the dominant cost element.

Revised cost estimates

In Fig. 7, the range of prior cost estimates is again presented, this time in the more familiar economic context of cost per watt. The span indicated for *Si* solar cells includes the use of both Czochralski and ribbon single-crystal material.^{5-8,10} The spread indicated by the solid portion of the vertical line for *Si* cells essentially includes current costs as well as estimates based on Czochralski wafers,⁸⁻¹⁰ and the dashed portion covers estimates based on ribbon substrates.^{5,6,7} For the *Cu₂S-CdS* cells, the solid part of the vertical line covers the range accessible by current state-of-the-art technology cells,^{10,11,12} and the dashed portion includes devices based on an order-of-magnitude reduction in *CdS* semiconductor thickness.^{13,14} By combining the future market environment summarized in Fig. 2, and the cost-prediction model illustrated in Figs. 5 and

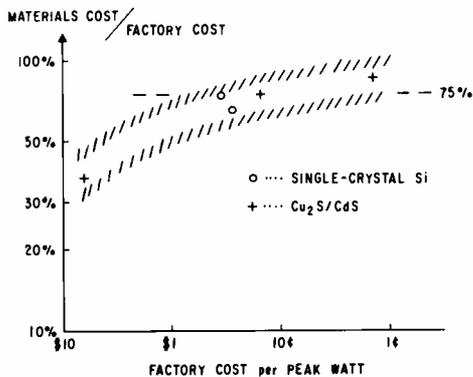


Fig. 5 — Relative materials cost vs factory cost.

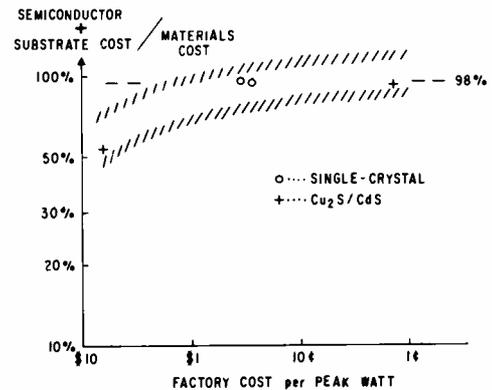


Fig. 6 — Relative semiconductor-plus-substrate cost vs. factory cost.

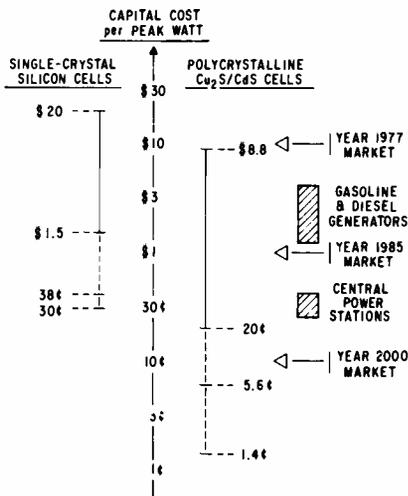


Fig. 7 — Overview of prior cost estimates.

6, the credibility of the basic semiconductor-plus-substrate cost estimates underlying these Si and Cu_2S-CdS cost predictions can be tested for plausibility.

In the case of single-crystal Si cells, the essential problem is to estimate the cost of the single-crystal wafer or ribbon substrate, and to establish that the estimate is consistent with the future market environment of Fig. 2. A convenient method of accomplishing this estimate is through the use of the graphical technique represented in Fig. 8.

Basically, Fig. 8 is a type of nomogram for converting cost per kilogram into cost per watt. For a given material thickness (e.g., 100 to 300 μm for ribbon substrates, or 500 to 1000 μm for Czochralski wafers), the projection of a cost-per-kg figure through the diagonal line representing a specific thickness yields a cost-per-area for the Si single crystal. The cost per watt is, of course, obtained from the cost per area by using the solar-cell conversion efficiency (10% in Fig. 8).

Having obtained the cost-per-watt estimate for the Si substrate, the cost-prediction model represented by Figs. 5 and 6 allows an estimate to be made for the total solar-cell cost. Finally, this cost can be used in the price — demand curve of Fig. 2 to approximate the solar-cell production rate that can be sustained at this cost, and this production rate can then be used to check the plausibility of the original cost-per-kg assumption. If inconsistent, the procedure can be repeated in an iterative fashion until an acceptable cost-per-kg assumption is ob-

tained. The documented experience curve for Czochralski Si supplies the essential final link between production rate and cost per kg in the case of Czochralski wafer substrates.^{5,6}

The results of this procedure are indicated in Fig. 8 by the regions within the solid lines. These regions represent the ranges of estimates for Czochralski and ribbon Si that are found to be consistent with the future market environment and cost-prediction model used in this study.

The level of production rate obtained for these cost ranges (see Fig. 2) does not indicate that there will be any substantial impact on a single-crystal Si production due solely to Si solar-cell manufacture. Any cost improvements that occur because of general semiconductor market growth would be reflected equally in the cost of both the Czochralski and ribbon substrates, according to the prediction method used in this study.

The spread in cost per watt for Czochralski wafer blanks is based on the current costs for Czochralski Si in boule form^{5,6,10} and a range in the wafer thickness and kerf loss due to wafer slicing.^{6,10,18} The lowest cost per watt assumes a state of the art corresponding to a 250- μm wafer with 250- μm kerf loss,¹⁸ and the indicated median cost is for a 300- μm wafer with 700- μm kerf loss. The latter combination represents the standard for space-type photovoltaic devices.^{6,10}

Estimating ribbon-substrate cost is considerably more difficult because of the

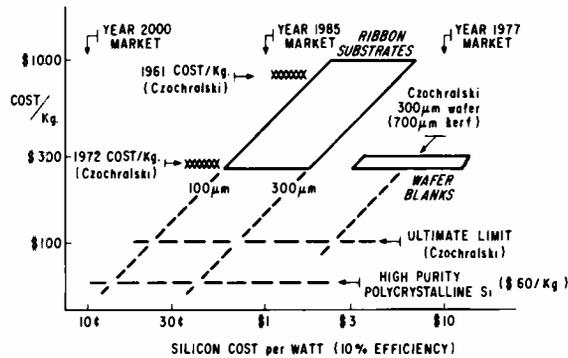


Fig. 8 — Semiconductor-plus-substrate cost for single-crystal silicon.

lack of any substantial experience or base-line data for the prediction. The existing estimates imply that the ribbon growth technology will proceed down the same experience curve as has been experienced for Czochralski growth, with equal cost per kg at equivalent cumulative production volume levels.^{5,6} This assumption has been accepted for use here, and forms the basis of the ribbon substrate cost per watt in Fig. 8.

The results from the present analysis differ from the prior estimate because of the input parameters assumed for production rate and cumulative production volume. The basis for the frequently quoted \$25-per-meter² cost for ribbon substrates is the assumption that the cost per kg for ribbon growth would have reached the ultimate limit for Czochralski growth (see Fig. 8), which is attained at an increase of $> 10^3$ over current single-crystal Si production.^{5,6} If, in contrast, the production volume and cumulative volume for ribbon growth is required to be consistent with the price — demand curve of Fig. 2, then a lower limit approximately equal to the current Czochralski cost per kg is obtained for ribbon substrates, as shown in Fig. 8. On this basis, a range of about 70 cents to \$2 per watt is estimated here as the most plausible low-cost limit within the present context of ribbon-growth technology.¹⁹

Reaching the minimum cost level requires the combination of three positive factors with high yield: 1) ribbon growth at 100- μm thickness, 2) ribbon growth at a cost per kg equal to the very mature Czochralski technology (for equivalent production rates and cumulative

volumes), and 3) conversion efficiency equal to that obtained for Czochralski-quality wafers under simplified device processing (nominally 10%). As can be seen from Fig. 8, relaxing either the first or second of the conditions (e.g., 1961 cost per kg with 100- μ m thickness, or 1972 cost per kg with 300- μ m thickness), while still assuming 10% efficiency, leads to a significantly higher minimum cost (\sim \$2/watt). If both of these ribbon-growth parameters are relaxed to the indicated higher levels, then the ribbon substrate has no cost advantage *vis-a-vis* the current Czochralski-wafer technology, even assuming a 300- μ m wafer blank with 70% kerf loss.

Using the *Si* cost estimates of Fig. 8 and the cost-prediction model of Figs. 5 and 6, it appears unlikely that single-crystal *Si* photovoltaic devices can significantly penetrate the \$1 per-peak-watt price level at a production rate consistent with the price—demand curve of Fig. 2. Based on the experience-curve prediction of Fig. 8, a significant penetration of the \$1/watt barrier can occur only at production rates that are entirely inconsistent with the future market environment summarized in Fig. 2; e.g., production rates equivalent to that predicted for a 10 cents/watt price are required.^{5,6}

A somewhat different procedure can be used in evaluating the confidence level of the cost estimates for Cu_2S -*CdS* solar cells. As with the single-crystal *Si* cells, the credibility of each overall cost estimate is no better than the predicted direct materials cost for the semiconductor-plus-substrate. In order to permit as general an analysis as possible, several high-purity polycrystalline materials have been considered as potential source materials for vacuum-deposited (evaporated) semiconductor layers. The materials considered included a rather broad range of costs, on a per kilogram basis,^{2,5,6,9,10,16,20} but on a cost-per-volume basis there is considerable uniformity for a number of potentially important materials. The per-volume cost is a more rational basis for evaluating the materials cost within the context of polycrystalline layers prepared by vacuum deposition. The data presented in bar graph form in Fig. 9 indicate the cost per volume of five particularly interesting semiconductor materials. These costs are all based on commercial quantities.^{2,5,6,9,10,16} The compounds are assumed to be formed by co-evaporation of the high-purity elements;

this results in a reduction of approximately 20 to 1 in raw materials cost *vis-a-vis* the use of high-purity compound as the source material. Of the five materials indicated, four have been used in photovoltaic devices (*Si*, *CdS*, *CdTe*, *Se*) and the fifth (*CdSe*) has a high absorption coefficient and desirable bandgap (\sim 1.7 eV). *GaAs* is not included in this figure because the available data for the constituent elements indicate that they are at least an order of magnitude more expensive per unit volume than the materials considered in Fig. 9.^{16,20} The data in Fig. 9 illustrate that a very general analysis can be made of semiconductor film material costs without reference to any specific material within the group considered

The results of such an analysis are presented in Fig. 10. Both the semiconductor film costs and substrate costs are summarized in this Figure. As indicated, the substrate cost represents a fixed range of 1 to 3 cents per watt (at 5% conversion efficiency),^{13,14} and the semiconductor layer material cost is dependent on the layer thickness and the deposition efficiency from source to substrate. Two basically different types of cells are considered in Fig. 10: 1) a device based on the technology for the space-design Cu_2S -*CdS* cell,¹⁰ and 2) an advanced-technology thin-film cell. For the former, the direct materials cost for the semiconductor layer is 15 to 50 cents per watt for a layer thickness of 20 to 30 μ m and a deposition efficiency of 20 to 40%. In the case of the advanced-technology device, the layer thickness is between 2 and 5 μ m and the direct-materials cost covers a range of 1.5 to 7.5 cents per watt. These

two cost ranges must of course be combined with the substrate costs of 1 to 3 cents per watt to form the basic semiconductor-plus-substrate direct materials cost. The resulting totals are 16 to 52 cents per watt for conventional technology Cu_2S -*CdS* cells, and 2.5 to 10.5 cents per watt for the generalized thin-film cells.

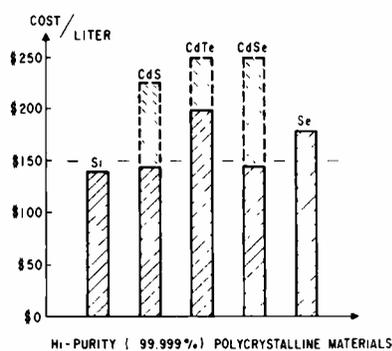
When these semiconductor-plus-substrate cost estimates are combined with the cost prediction model of Figs. 5 and 6, it appears likely that the conventional-technology Cu_2S -*CdS* cell can significantly penetrate the \$1/W price level, and that an advanced-technology thin-film cell can approach and perhaps satisfy the 10 cents/W price criterion required for large-scale power generation.

Although the generalized thin-film cell of Fig. 10 is explicitly based on the use of vacuum-evaporation deposition technology, this is not intended to constitute an endorsement of this method as the optimum technique for the semiconductor layer formation. This specific method has been used only to illustrate that the desired cost levels can be approached or penetrated by one particular technique. Alternative deposition techniques that promise reduced raw-materials costs or lower capital-equipment costs must be considered as viable candidates in any detailed evaluation. One such technique, for example, is the chemical-spray method.¹⁴

An overview of the revised estimates that have been developed here for single-crystal *Si*, conventional Cu_2S -*CdS*, and the generalized thin-film cell is presented in Fig. 11. The predictions for semiconductor-plus-substrate direct-materials-cost are shown within the context of the price—demand curve of Fig. 2, the current single-crystal *Si* production, the competitive cost/watt levels for several selected commercial energy sources, and the present electrical utility generating capacity.

Summary and Conclusions

The purpose of this study was to critically examine the issue of solar cell cost predictions, both in terms of a review and analysis of the prior literature and through modification and extension of the existing studies. The end result of this procedure is a set of revised estimates



NOTES: (1) COST FOR *Si* IS BASED ON LARGE-SCALE COMMERCIAL PRODUCTION; COSTS FOR OTHER MATERIALS ARE BASED ON SMALL QUANTITIES.
 (2) COST RANGE INDICATED FOR COMPOUNDS IS BASED ON SUPPLYING 0- to 100% EXCESS OF THE MORE VOLATILE CONSTITUENT.

Fig. 9 — Cost-per-volume for high-purity polycrystalline semiconductors.

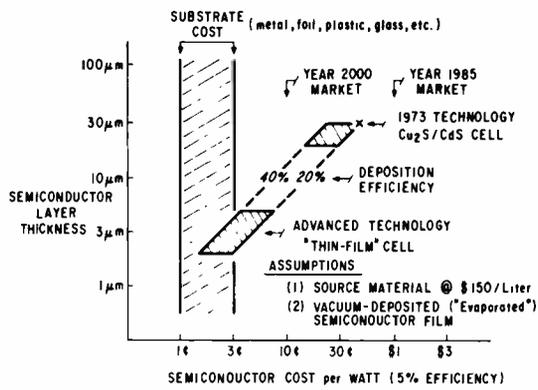


Fig. 10 — Semiconductor-plus-substrate cost for polycrystalline solar cells.

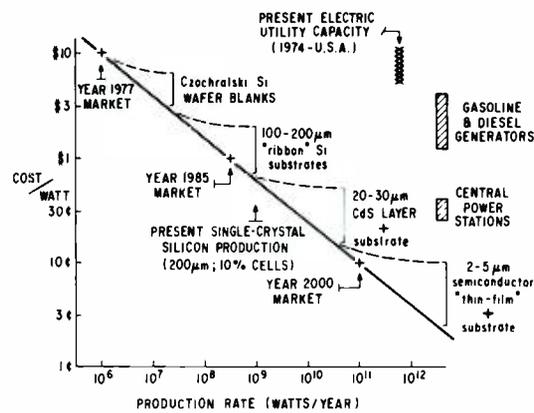


Fig. 11 — Overview of alternative cost predictions.

for the dominant cost elements of single-crystal *Si*, polycrystalline *Cu₂S-CdS*, and generalized thin-film photovoltaic cells.

The validity of these revised estimates, *vis-a-vis* the prior predictions, is based primarily on the credibility of a particular future market environment that forms the basic framework for the revisions. The plausibility of the hypothetical environment used here rests essentially on the demonstration of internal self-consistency under testing via experience-curve concepts.

On the basis of the revised estimates obtained in this study, a number of tentative conclusions can be reached with respect to both prior cost predictions and their implications for terrestrial solar-energy conversion. The most significant of these conclusions are highlighted below:

Single-crystal *Si* Cells

- The existing cost estimates for the ribbon-growth technology are based on unrealistically optimistic market parameters *vis-a-vis* the current status and expectations for Czochralski growth.
- There is no reasonable current prospect that a technology based on either ribbon or Czochralski growth can satisfy the cost criteria defined here for large-scale terrestrial conversion of solar energy.
- The near-term (1985) price-demand requirements can be met by single-crystal ribbon cells, based on optimistic technology forecasts.

Polycrystalline *Cu₂S-CdS* cells

- Current technology devices have the potential of satisfying the near-term (1985) market price-demand requirements, provided that historically optimistic stability and yield are assumed.
- There is no reasonable prospect of meeting the requisites for large-scale terrestrial

applications within the present technological framework.

Generalized thin-film cells

- Photovoltaic devices based on a thin-film (2 to 5 μm) polycrystalline semiconductor layer (e.g., as prepared by vacuum evaporation technology) can satisfy the economic criterion for large-scale terrestrial solar-energy conversion, as defined here.
- On the basis of a purely economic estimate, there are at least five possible semiconductor materials (*Si*, *CdS*, *CdTe*, *CdSe*, *Se*) and three potential substrates (metal foil, glass, plastic) that must be considered as plausible candidates for the generalized thin-film photovoltaic cell.

These conclusions should be placed in a proper context by noting that they refer to the *possibilities* of meeting the hypothetical goals rather than the *probabilities*. It should be clear that the estimates based on Czochralski crystal growth have the highest confidence level, in a very broad economic and technical sense, whereas, at the opposite extreme, the estimates for the generalized thin-film devices are predicated on a currently non-existent technological base.

In addition, cost reductions will occur independently in the Czochralski wafer technology because of the continued strong growth in the general *Si* semiconductor market. This will also produce a second-order effect on the polycrystalline *Si* material cost for the ribbon *Si* and thin-film *Si* devices.

The reduction factor for Czochralski wafer costs could be as large as four (relative to current costs) by the mid-1980's. Although this is a significant consideration in assessing the potential relative impact of the "ribbon" *Si* technologies, it will not materially alter the general conclusions reached in this study.

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Solar energy as a consumer product

B. Shelpuk

Solar heating is economically feasible now in locations with favorable solar collection. Fuel shortages and price increases will make it more attractive and technology advances and increased production volume will lower its cost — with all of these factors working to increase its applicability. The high initial capital cost is the major deterrent to its greater use, and this could be alleviated by tax incentives, special financing, etc.

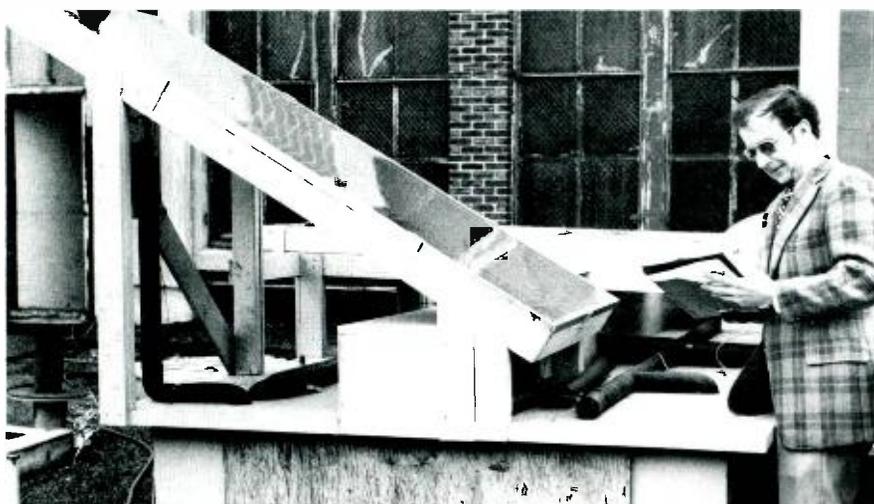
PRESENT ENERGY FLOW patterns for the United States are outlined in Fig. 1. Note that in 1970 energy was consumed primarily in four roughly-equal areas: electrical energy generation, residential and commercial, industrial, and transportation. The units are millions of barrels of oil (equivalent) per day. Petrochemical use is represented by the nonenergy category. The figure shows that approximately half of all energy is not available to society. The greatest percentage of energy losses occur in the electrical energy generation and transportation areas due to the thermodynamic losses and resulting low

efficiency in converting from heat to mechanical energy. This figure points up the inadequacy of present domestic oil production if oil imports are restricted.¹

Projected needs

The projected energy flow pattern for 1980 (Fig. 2) shows the growth in the demand in all areas. Because of the large growth projected in transportation and petrochemical needs without attendant growth in domestic production, substantial increases in imported oil will be required.

Ben Shelpuk, Thermodynamics Group, Advanced Technology Laboratories, Camden, N.J., received the BSME and MSME from Drexel University. Since Mr. Shelpuk became a member of Advanced Technology Laboratories, he has been actively involved in much of the thermoelectric cooling activity in RCA. This has included the design and fabrication of thermoelectric water chillers, air conditioners, cascaded Peltier coolers for application to infrared sensitive image tubes, and several energy conversion devices. He was responsible for several thermal analyses of spacecraft systems, and conducted an advanced energy conversion study for a major weapon system. In 1966, Mr. Shelpuk became Engineering Group Leader for the Thermal Systems Group at ATL. As such, he was responsible for programs in air conditioning, cryogenic refrigeration, infrared device refrigeration, heat transfer analysis and design, and heat pipe development. More recently, he has been responsible for the application of much of this technology in the environment of space. This included feasibility studies of a spacecraft cryogenic cooler using a nuclear energy source as well as thermal control using a fusion heat sink for several electronics systems used in the Apollo program. Mr. Shelpuk is currently responsible for technique work in solar energy utilization. This work includes experimental programs to apply the VM thermodynamic cycle to air conditioning for a solar heat source and another to build and test solar collectors and photovoltaic arrays. In addition, he is responsible for technical and economic analyses on solar energy and thermal storage systems and demonstration programs to show feasibility of this technology on a larger scale. Mr. Shelpuk is a member of the American Society of Heating, Refrigeration and Ventilation Engineers, Tau Beta Pi, and Pi Tau Sigma.



Author Ben Shelpuk recording data from solar collector setup at Camden.

In addition to showing a large increase of imported oil by 1980, Fig. 2 shows a large increase in the electrical energy needs. This increase will be supported mainly by increased use of coal and nuclear energy.

No simplistic solution

It is clear from this brief look at present and projected energy flows that meeting the energy needs of the nation is highly complex, and does not lend itself to simplistic solutions in any one area. Several elements of a possible national energy strategy are suggested by consideration of the fuel-use patterns and projected consumption patterns:

- 1) A reduction of oil consumption in the transportation area would have great impact. But as was seen in 1974, high prices and long lines during the Arab oil embargo did not significantly reduce consumption. By the end of the year, with the price above 50 cents/gallon, the consumption level of 6.5 million barrels a day was only slightly below the 6.6 million barrels a day in the Fall of 1973 when the price was below 40 cents/gallon.
- 2) Another part of the strategy would be to use oil only for transportation and petrochemical needs and to devote substantial effort to reducing demand by promoting mass transit, higher efficiency engines, and less wasteful use of plastic and other petrochemicals. The use of natural gas and gasified coal could supplement the petroleum supply as occurred in wartime Germany and Japan.
- 3) A third element would call for use of the diminishing source of natural gas and coal to supply the high grade thermal requirements of industry, and use nuclear sources predominately for the electrical utility fuel requirement. This was the plan of the electrical utilities in the 1960s, but it is falling victim to rapidly escalating costs and environmental and safety concerns. Alternatives to nuclear energy are geophysical sources such as hydroelectric, geothermal and solar and/or greatly reduced societal energy demands. Then the low grade heat required for environmental comfort in the residential, commercial and industrial sectors must be supplied from (a) what is left over when needs are met, (b) heat recovery from the other higher grade uses of energy, or (c) solar energy.

New approaches

Several alternatives are being considered that are not based primarily on reduction of consumption and waste or establishment of priorities. These include:

- Conversion of coal into liquid or gas
- Fusion
- Geophysical sources

Large scale programs are being proposed

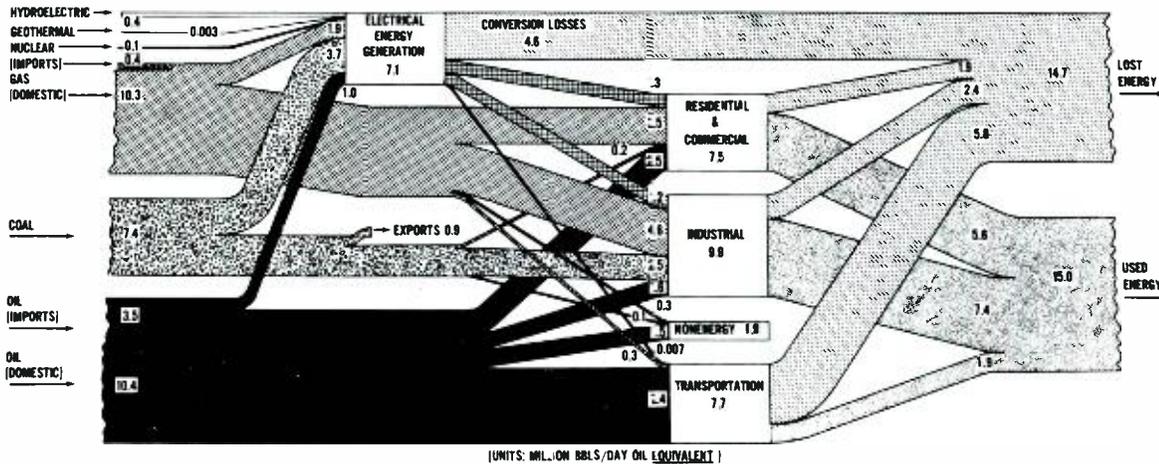
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and funded to achieve economic coal gasification of the large coal deposits in Montana and North Dakota. While such fuel generation could be an important factor in future U.S. needs, the development of coal to a much larger scale will require a substantial investment, a guarantee of the market for the product, adequate guarantees of environmental protection, and time.

Fusion has been suggested as the ultimate energy source, but it has not yet been demonstrated in the laboratory. Fermi achieved a fission reaction in 1942 at the University of Chicago and 32 years later fission impacts the energy picture only to the extent of 5% of electrical output. In this century, fission is probably the only nuclear reaction we can consider as a practical energy source.

Although nuclear energy (fission or fusion) is being promoted by many as the best solution to future energy needs and will get the bulk of research funding, there will be continuing resistance to this approach from environmentalists. This resistance can vary with the balance between energy supply and demand, the resistance being strongest when the supply is adequate. Most environmental ob-

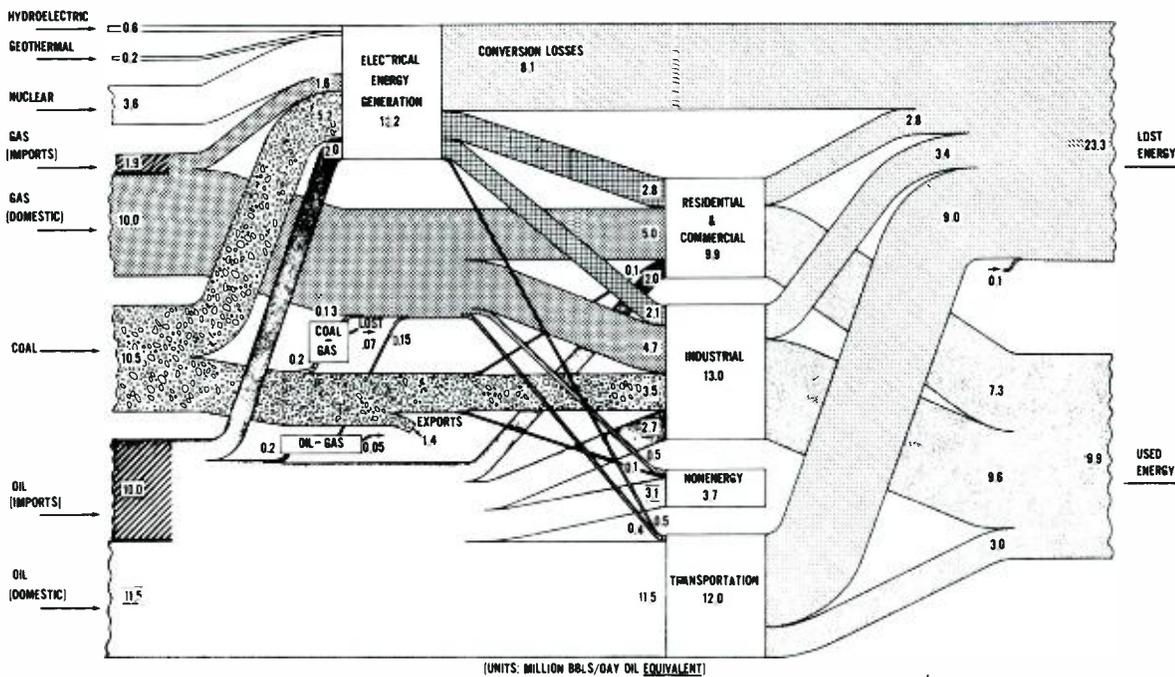
1970



SOURCE: "UNDERSTANDING THE 'NATIONAL ENERGY DILEMMA'," JCAE, 1973

Fig. 1 — United States energy flow pattern (actual — 1970).

1980



SOURCE: "UNDERSTANDING THE 'NATIONAL ENERGY DILEMMA'," JCAE, 1973

Fig. 2 — United States energy flow pattern (projected — 1980).

jections will probably never be resolved to the satisfaction of all concerned groups.² As the number of plants, their thermal pollution, and safety problems increase, resistance to this energy source promises to grow. Implementation of fast breeder technology with its substantially increased waste-storage problem could also intensify environmental and safety objections.

Geophysical sources, such as ocean thermal gradients, tidal power, wind, geothermal, and solar power, have the advantage of minimum environmental impact, but the disadvantage of diffuse nature which requires substantial capital facilities to use the available energy. Solar energy is well suited for providing low grade heating requirements and can be considered on any scale — ranging from a minor supplement to more conventional sources to an exclusive primary energy source. Solar energy can have an important role in closing the energy deficit.

Thus, a multifaceted approach is required. We must create an acceptable scenario for the increased deployment of nuclear power plants, promote all types of energy conservation programs and

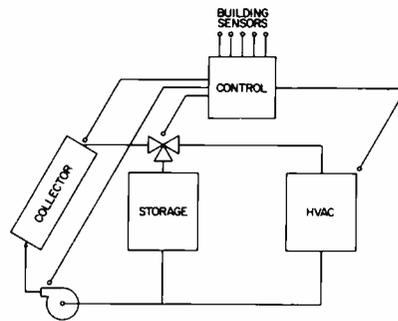


Fig. 3a — Simplified solar energy environmental system.

equipment, develop environmentally acceptable methods for mining and using coal, and develop economically sound methods for heating and cooling buildings with solar energy.

Solar energy for heating and cooling

Much of what can be done to relieve the energy problem is out of the hands of the individual consumer. At the consumer level, such energy conservation measures as effective home insulation, efficient automobiles, efficient appliances and energy-conservative architecture will be widely integrated into our society by

1980. But an important alternative is available to the consumer now — the use of solar energy.

Application of solar energy

Solar energy is expected to be a significant factor in the future in the production of electricity — but it can be important now as an option available to the consumer for heating and cooling.

The feasibility of using solar energy to produce electricity through the photovoltaic effect has been convincingly demonstrated in the U. S. space program in which the electrical power is supplied primarily through solar cells. Application of this technology to the terrestrial environment is being actively pursued by various agencies of the government and by industry. Rather formidable cost reduction objectives have been targeted for an installed silicon solar cell plant cost of \$500/peak kW in 1985. Feasibility for further reduction to the \$100/peak kW range are being sought for other material systems in the same time frame.³ Substantial technological and automation developments will be required to reach these objectives. This application of solar

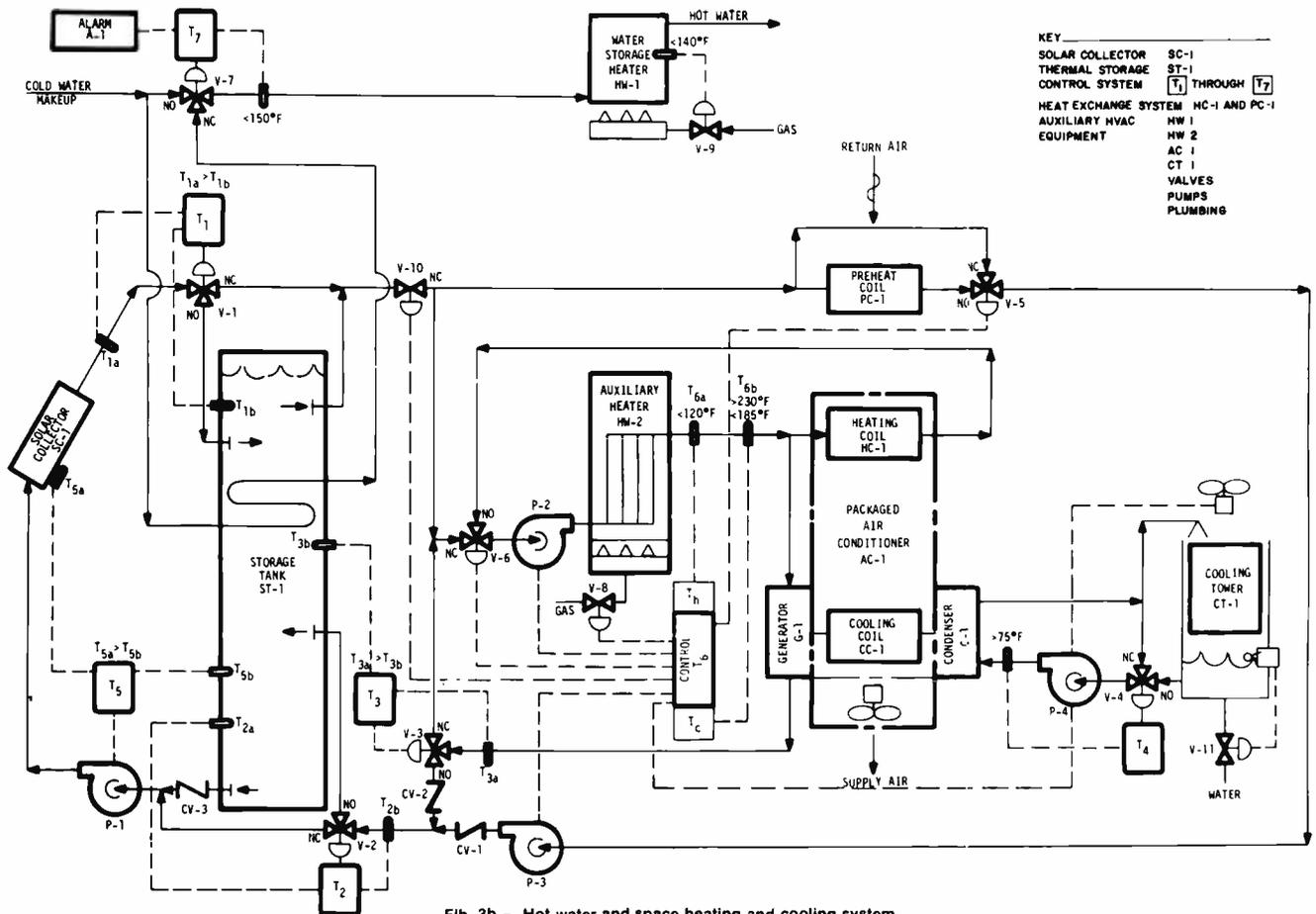


Fig. 3b — Hot water and space heating and cooling system.

energy will find broader use as costs are reduced by the combination of increased product volume and technological advances.

The use of solar energy for heating and cooling, even by individual consumers, is an application of technology which is already here. Descriptions of this application have appeared in the popular press and scientific journals. Demonstration projects are being funded by the U.S. government as well as private companies and individuals.

Solar heating system configuration

Typically, solar heating systems are configured as shown in Fig. 3. They consist of a collector; thermal storage means; a heat exchanger; a control system; and auxiliary heating, ventilating and air conditioning (HVAC) equipment to supply building demand when there is inadequate solar energy.¹

Solar collector

The solar collector is the most visible and costly part of the system. It generally consists of an enclosure containing an absorber panel which is heated by solar energy incident through one side which is transparent to visible light. The transparent material, which can be glass or transparent plastic, is opaque to radiation in the long wave IR at which the hot absorber radiates. The captured solar energy is thus retained within the container by the "greenhouse effect". Heat is transferred from the absorber into air or water which is then used to heat the living space.

Substantial research is underway to improve the performance of solar collectors by:

- Building focused collectors so that the absorber size and its associated losses can be reduced;
- Developing coatings and structures for the transparent collector cover which suppress thermal losses back through the cover; and
- Developing absorber coatings which maximize collected incident energy and minimize reradiated energy.

The best available economic collectors have an insulated glass window over a blackened aluminum or copper absorber/heat exchanger which is insulated on its back face with 2 to 3 inches of

fiberglass insulation. A cross-sectional view of this construction is shown in Fig. 4. The heat collecting efficiency of such a collector is dependent mainly on the difference between collector temperature and the ambient air temperature. Fig. 5 shows the typical calculated performance of the two-glass, flat-black collector. These characteristics have generally been correlated to a wide range of experimental test results, and show the following:

- Little energy can be collected at temperatures near 190°F
- Collected energy depends greatly on incident energy Q , with Q decreasing to the right in Fig. 5. The maximum value of Q for which one could design is 280 to 300 Btu/h-ft².

The impact of the former is more pronounced on cooling since existing heat-driven air conditioning equipment requires heat at temperatures in the 200° to 225°F range (120° to 150°F above typical summer ambient temperature), while 120°F water is adequate to meet heating needs in a 15° to 25°F winter ambient temperature. The latter characteristic creates a strong bias for solar heating in high sunshine regions such as the southwestern United States. A further ramification of the solar collector characteristic is that it makes system performance estimation on the basis of average values of Q somewhat risky. Most solar heating and cooling system designs and analyses use computer-aided calculations with actual weather bureau data as input.

Other parameters affect collector performance. A liquid flow rate is required which achieves good collector performance by promoting effective heat transfer to the absorber and minimum auxiliary pump power; a 10°F temperature rise in water flowing through the absorber is a good compromise. Collector tilt is an important parameter. A collector tilted from the horizontal at the local latitude plus 15° will collect the most energy during the heating season. A collector tilted at the local latitude minus 15° will collect the most energy in the cooling season. For year-round collection, a collector tilted from the horizontal at an angle equal to the latitude gives maximum collection. Collectors should generally be pointed due south, although a 10° azimuth orientation to the west may be desirable because it favors afternoon collection when ambient temperature is higher and thus collector losses lower

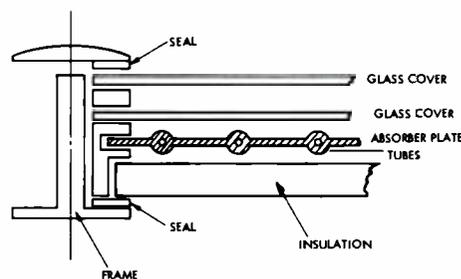


Fig. 4 — Schematic diagram of a solar collector.

Alternatively, an open heat exchanger such as found on lower cost systems, could be used. This is an absorber plate from which heat is removed by uncontained liquid or air flowing over its surface. These collector alternatives and parameter selection involve some performance compromise; most designers now use the collector described in Fig. 4.

There is intensive research underway to improve materials and structures which can be used in collector systems. There is a potential for breakthrough in this area. More likely, however, is the possibility that cost will be reduced through a combination of technology and increased production volume.

Thermal storage means

Thermal storage and collector size and cost must be balanced in a solar energy application. In the ideal situation, solar collector area could be kept at a minimum if energy required for winter heating is supplied by supplementing the available winter solar energy with energy stored from summer collection. While this would result in the most efficient use of the available energy, energy cost and thermal storage size considerations would not be optimum. Therefore, the preferred system should not be based on

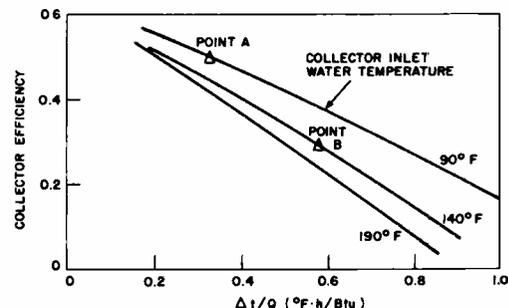


Fig. 5 — Typical calculated performance of two-glass, flat-black collector.

maximum collection efficiency, but should balance collector and storage subsystem size and cost. Studies show that minimum cost for the collected solar energy (in a well-designed residential dwelling in a moderate climate) is achieved with a thermal storage of the equivalent of 10 lb of water per square foot of collector area.⁵ Such a storage load will be heated from 90°F to 140°F in the equivalent of only 3 to 4 hours of collection on a bright warm day. This would provide adequate capacity from storage for overnight heating or for one day at most. With such a cost-effective system, consecutive cloudy day needs would be supplied by the auxiliary heating system. The relative percentages of total demand shared by the solar heating system and the auxiliary system are also a matter of economics and will be dealt with in the discussion of economic factors.

The most widely used storage medium is water. Energy is stored in the specific heating of the water and then rejected to the living space by its specific cooling. The penalty for operating in this mode is that, as energy is stored, temperature rises and collector efficiency drops as was indicated in Fig. 5. As a specific example, assume that the ambient temperature is 25°F and the incident solar flux is 200 Btu/h-ft² (a fairly clear day during the hours of 10:30 a.m. to 1:30 p.m.). For this case $\Delta t/Q = (90 - 25)/200 = 0.325$ (point A, Fig. 5) for 90°F storage temperature and $(140 - 25)/200 = 0.575$ (point B) when the temperature rises to 140°F. Collector efficiency at these conditions is 50% and 29%, respectively, a 40% drop.

This effect on system performance has been the driving force for research in the area of thermal storage by reversible phase or chemical changes in materials. The best materials under consideration absorb 110 to 140 Btu/lb during

transitions at temperatures around 120°F. Cost and cumulative irreversibilities limit usefulness of these systems at present. Successful development of phase-change thermal storage will substantially reduce the amount of storage material required in a heating system and improve the total system capacity and efficiency. For the present, water storage must be used in liquid heating systems and gravel or rock bed storage in air heating systems.

Heat exchanger and control system

The heat exchanger and control of a solar heating system are important in determining performance but are not unique to solar energy. The heat exchanger can generally be a standard hot water system although an intermediate liquid-to-liquid exchanger as shown in Fig. 6 can be used to limit the amount of antifreeze required to protect the collector loop from freeze up. As shown in the diagram, the heat exchange loop consists of circulating pumps, control valves, bleed valves, liquid-to-liquid exchangers, and liquid-to-air exchangers. To a large extent there is commonality between a conventional and a solar heating heat exchanger.

Control of a solar heating system has some impact on its efficiency. Although there has not been much work done to define optimized operating strategies, several control parameters seem clear:

- There should not be any system operation until collector temperature exceeds storage temperature.
- There should be no system operation if there is not temperature rise through the collector.
- Flow rate should be varied in proportion to amount of collected heat, and
- Load should be shared between solar heat and the backup auxiliary fuel in such a way as to maximize collected solar energy. This might involve use of solar heat as a preheat

source especially in an air conditioning or domestic hot water application.

Up to this point, multipoint and differential thermostats have been used to accomplish these functions. However, Fig. 3b shows seven temperature decisions (T1 — T7), and an even larger number of pumps or valves which must be controlled on the basis of the seven temperatures. As operating strategies become better defined and microprocessors become cheaper, more sophisticated control will become an avenue to further performance improvement.

Economic factors

The biggest drawback to widespread use of solar energy for heating and cooling is more economic than it is technical. Because the cost of a solar heating system is almost all in the fixed capital investment required, capacity installed for an infrequent requirement results in a high cost of the collected energy. Also the cost of components which are independent of system size must be spread over less output if the unit is used in a low demand application.

There is an optimum size for the most cost-effective solar heating and cooling system for any application. This can be clearly seen when building demand is coupled with solar system parameters determining the size and auxiliary fuel requirements which result in minimum cost per unit of output. Fig. 7 shows the results of a detailed analysis for one of the most favorable sites for solar energy in the United States — Albuquerque, New Mexico.⁶ This analysis utilizes a realistic estimate of system cost at \$6/ft² of collector (\$4/ft² — collector; \$1/ft² — storage; \$1/ft² — plumbing and control costs) and includes the cost of money (8% interest rate) to finance the installation. The preferred system size from the curves

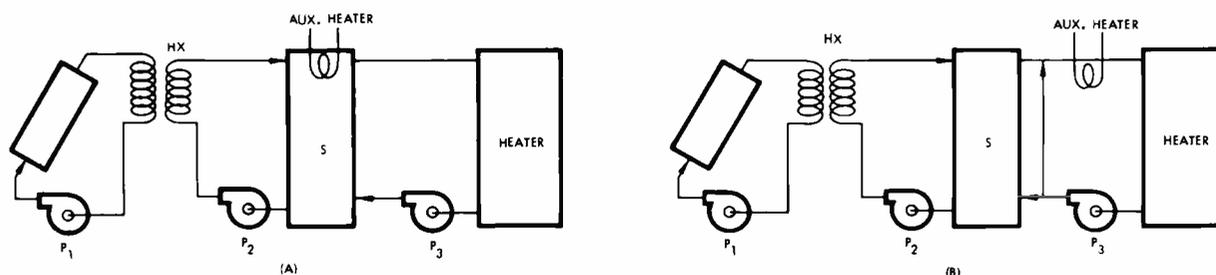


Fig. 6 — Space heating concepts, with heat exchanger.

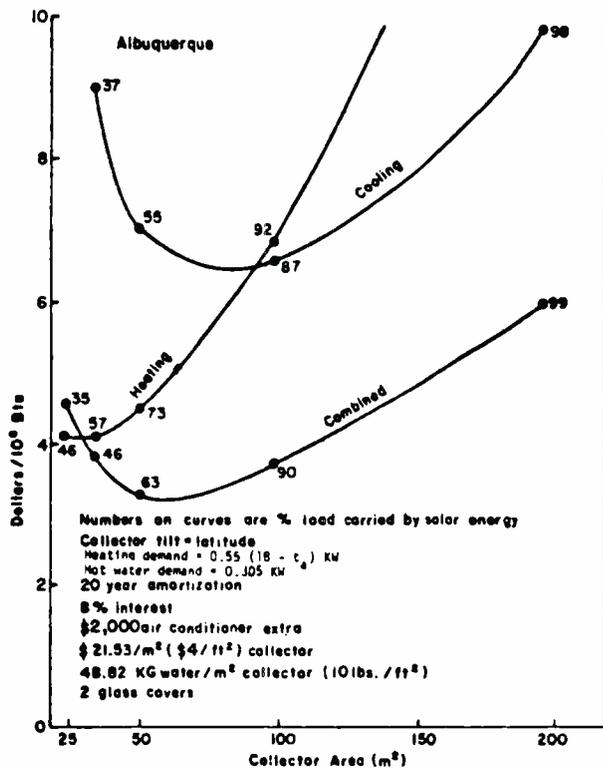


Fig. 7 — Cost of solar energy conversion system for Albuquerque, New Mexico.

calls for a collector area of 60 m² (645 ft²). The building load is 25,000 Btu/degree-day (DD) which corresponds to a large house. Total system cost would be \$5870 including a \$2000 premium for the additional expense of an absorption air conditioner and associated plumbing instead of a conventional vapor compression machine.

Fig. 7 also shows that, for the preferred system size, over 73% of the winter heating demand will be supplied by the solar energy. This does not correspond to minimum unit heating cost because the need to supply enough heat for the air-conditioning load biases the system to a larger size than would be indicated by heating alone. At the preferred system size, over 55% of the air conditioning load would be provided by the solar energy.

The average cost of the energy used year round is just over \$3/10⁶ Btu. Use of solar energy is attractive when compared to the cost of fuel oil which is \$3.67/10⁶ Btu (\$0.37/gallon) and electricity which is \$14.65/10⁶ Btu (\$0.05/kWh). However, direct comparisons of cost must consider that it takes almost four times as many Btu's of low temperature heat (200°F) as the equivalent Btu's of electricity to get an equivalent amount of air conditioning. Also, the complete cost optimization must include the cost of the auxiliary fuel

in addition to the cost of the solar energy. If the cost of the auxiliary fuel is greater than the solar energy, then the proportion of the total energy supplied by solar energy will increase in a minimum cost system.

A clearer picture of the cost comparison for the house in Albuquerque can be achieved by looking at total energy cost for the year. Albuquerque has 4348 heating degree-days/year and 1362 cooling degree-days/year. The 25,000 Btu/degree-day house would have a 108.7 × 10⁶ Btu heating requirement and a 34.05 × 10⁶ Btu cooling requirement per year. The energy required for domestic hot water would be 11 × 10⁶ Btu/year. This household would spend \$439.30 a year for fuel oil and \$212.80 for electricity to run its air conditioning assuming an EER (energy efficiency rating) of 8 Btu/watt-hr and \$0.05/kWh electrical power cost. If 75% of its heating and 60% of its cooling is supplied from a solar source, a cost savings of \$457.16/year would be realized on an investment of \$5870.

The use of solar energy for heating and cooling is on sound economic ground today in the locations favorable to solar collection. Fuel shortages and price increases will tend to increase its potential applicability to other parts of the coun-

try. Recent studies^{1,2} indicate that 4 to 10% of commercial and residential heating and cooling requirements in this country will be satisfied with solar energy by the 1990 to 2000 period. Such usage will be equivalent to 0.5 to 1.0 million barrels of oil/day. The primary barrier to broader use will be the capital cost of the required installation. While this certainly is not the sweeping answer to our energy needs that some writers have predicted, it is a substantial step in the direction of energy independence that this country desires. Tax incentives, changes in financing methods, government restrictions on allotments for heating fuel, and other factors could change this picture

The RCA Role

RCA is applying its technical resources across a broad spectrum to meet the challenge of energy sufficiency. In its traditional role as semiconductor manufacturer, RCA is conducting active programs directed toward achievement of low cost solar cells for electrical power conversion. As a user in the heating and cooling field, RCA is planning a pilot project to demonstrate the feasibility of solar energy as the power source for air conditioning the new management center at RCA headquarters. Under contract to the U.S. Energy Research and Development Agency (ERDA), RCA is striving to apply technology developed for aerospace systems to air conditioning and thermal storage applications with solar energy. Additional efforts planned to exploit solar capabilities in such fields as computers, electro-optics, material sciences, systems integration, and building management will form the basis for an expanding RCA role in this national challenge.

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Energy management and automated support systems

O.T. Carver

Our use of expendable energy resources has increased at an untenable rate. Long-term solutions involve recovery of less accessible reserves. For short term, we must depend upon more efficient use of existing fossil fuel, and energy conservation. We must learn and apply new concepts of energy management. Energy management forces re-thinking of old trade-offs. For example, the manpower savings through automated test may not be as significant as the fuel savings. Automated support systems offer potential advantage in reduced energy consumption per tested item through reduced test time and more efficient operation of energy consuming devices.

IF there is nothing so powerful as an idea whose time has come, there is nothing so weak as an idea ahead of its time. Few people were concerned 30 years ago with the reality of expendable energy resources. The essence of the situation is simply that: worldwide, our needs for

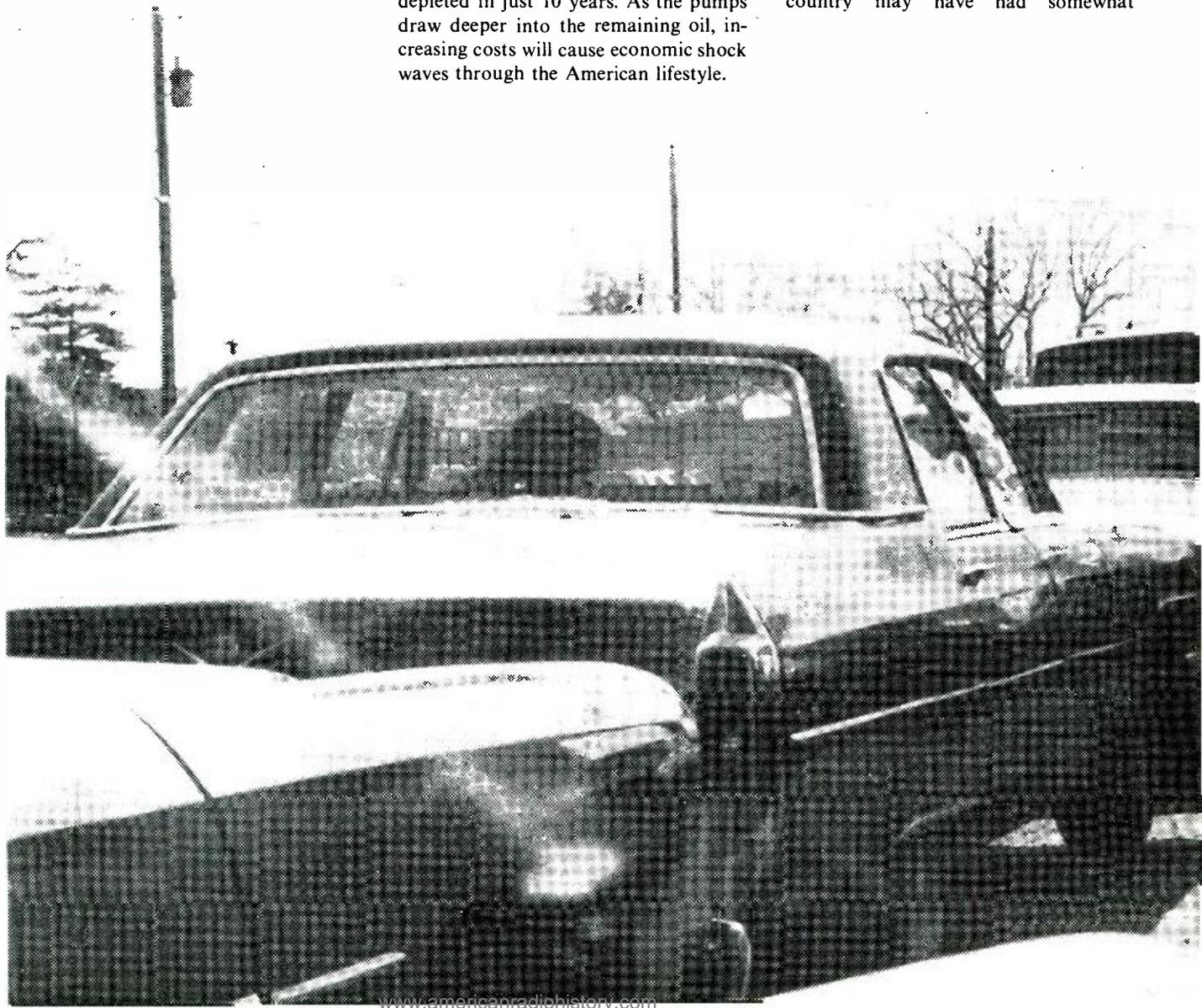
energy have been growing at a rate of 5% per year. We are meeting most of those needs with fossil fuels, predominately petroleum products, because they are the easiest source to acquire, transport, and consume. If the present rate of oil consumption were held constant, the total estimated U.S. oil resources will be depleted in 45 years. Proven reserves, those verified by actual drilling, will be depleted in just 10 years. As the pumps draw deeper into the remaining oil, increasing costs will cause economic shock waves through the American lifestyle.

Harrison Brown's, *The Next Hundred Years* created a stir when it was published in 1957.¹ His was one of the voices announcing troubles ahead, joined by many others over the past 20 years. Harrison Brown looked at the impact of population growth, food supply, energy sources and rates of industrial growth and concluded that we would face energy source problems sooner than we cared to believe.

Harrison Brown indicated that, should the level of world petroleum production rise to more than two and a half times the 1957 level of 5 billion barrels per year, oil would be well beyond its peak use by the year 2000. World oil consumption passed the 12½ billion barrel threshold within 10 years of Harrison's observation and is now at about 20 billion barrels.

It took waiting in line for 45 minutes at 7:00 o'clock on a cold February morning to get \$3.00 worth of gasoline for the New Englander to acknowledge the clarity of Brown's crystal ball. Other parts of the country may have had somewhat

Photos courtesy of Gloucester County Times.



different experiences, but suddenly, energy management moved from an abstraction to reality. In the typical American way, we focused the sixteen-inch guns of tv special reports, magazine feature articles and consumer advertising on the 'energy crisis' and we all but blew the whole subject out of the water, driving us to numbing insensitivity.

Among the energy-related statistics that have passed across the scene in the last twelve months, there are some basic concepts and relationships which will be useful in considering the role of automatic test equipment. These basics

concern, first, how much do we consume and where does it come from.

What do we consume?

Energy consumption in the U.S. has increased at a rate of about 5% per year for the past 20 years. Fig. 1 shows the major consumables — oil, natural gas, and coal.² About 25 years ago, natural gas and petroleum were the cleanest and most convenient fuels. They were also the cheapest, so they began to displace coal. As the consumption of oil exceeded U.S. production rates, imports of foreign oil increased because it was cheaper than domestic.

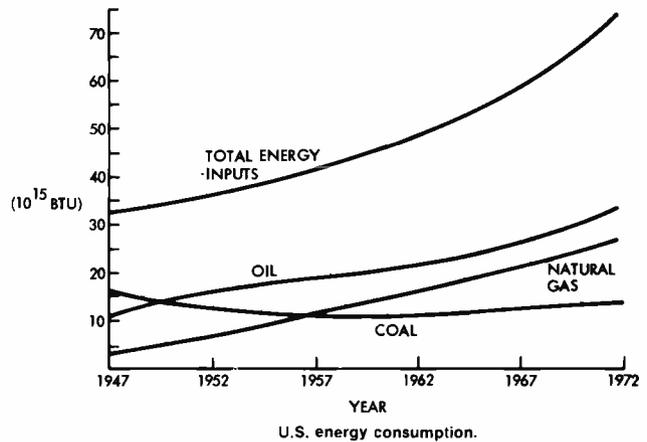
The Department of Defense, incidentally, needed 2.4% of the U.S. total consumption in 1974.¹ Of the DOD energy consumption, about 70% is petroleum, so the DOD is relatively more dependent on oil than the U.S. average, but still represents only a small part of the U.S. petroleum demand. Fig. 2 shows the DOD uses of its petroleum energy. This figure is also an indicator of petroleum use by the individual services, the Air Force being the largest user, the Navy next, and then the Army. So, our rate of energy consumption is increasing and our consumption of petroleum products is increasing at an even higher rate.





O.T. Carver, Mgr., ATE Systems, Government Communications and Automated Systems Division, Burlington, Mass., received the BSEE from West Virginia University in 1949, graduate studies in engineering management at George Washington University and received an M Ed at Northeastern University in 1972. He has participated in ATE programs at RCA since 1956. On the Multi-Purpose Test Equipment programs, he was responsible for test requirements analyses and the configuration of the basic automatic test system for checkout of Army missile systems. He has directed test technique studies aimed at increasing the ability of ATE to perform fault diagnosis and failure prediction. He directed early studies resulting in the specification of functional test assemblies which could be electrically configured by a central programmer. He was responsible for systems design on the MTE program and for test requirement analysis of the advanced Army missile systems, Mauler, Shillelagh, Lance, and TOW. In the latter task, he performed test system design concurrent with missile system development requiring close coordination and data exchange to ensure compatibility of the end product. An important part of his task responsibility involved the location of test access points and criteria for performance evaluation. He also supervised the study of fault isolation by mathematical approach and studies investigating improved programming procedures for Automatic Test Equipment. The latter studies developed tradeoffs between hardware and software aspects of the total test system. Recent programs under his direction have developed support system simulation models for effectiveness evaluation of alternate support concepts. Current programs include improved inspection procedures for helicopter maintenance, on-board monitoring systems, and advanced maintenance concepts for new ship classes.

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Where are our energy resources?

In July, we consumed 16.3 million barrels of oil per day, of which 6.5 million barrels or 40% were imported.⁴ In 1972, about 30% of our oil was imported; in 1952 we imported only about 8%. Our oil resources, including Alaska, represent about 5% of the world's known oil reserves. Over half of the U.S. resources of oil have already been consumed. Of all U.S. fossil fuel reserves, 90% are in the form of coal and over 95% of our coal is still in the ground. The U.S. uranium resources, more than 200 times all the oil resources we ever had, are virtually untouched.

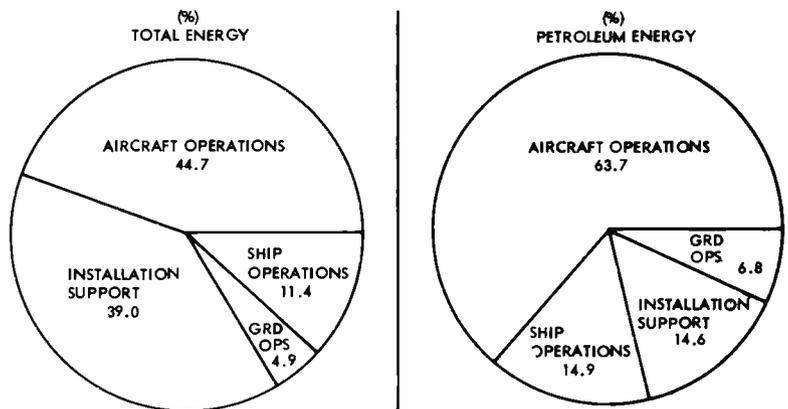
There is a mismatch between the energy sources we are using and the sources we must be using 25 years from now. This mismatch has to be corrected and all the incentives are shifting so as to make it happen (e.g., 4 to 1 increase in crude oil costs in one year). But for the next decade, we must get along with relatively minor changes in the present patterns of energy consumption. Beyond 1985, energy

management concepts will shape the political and cultural lives of every nation.

Where do automated support systems fit?

Automated test equipment can impact the short-term in areas of energy consumption efficiency and consumption alternatives. Relative to energy consumption efficiency, consider the following:

About 25% of the total U.S. energy consumption goes to transportation and 80% of the source is gasoline and jet fuel — the energy resource which is in shortest domestic supply and with the most rapidly increasing cost.⁵ A typical automobile engine may operate acceptably even though fuel consumption per mile is greater than that designed into the engine. Tuning the engine (a balance of ignition and fuel mixture variables) could reduce fuel consumption by 20% to transport the same load over the same distance. A 5% retard from the basic ignition timing setting consumes about a



Department of Defense energy consumption.

half-mile per gallon of gas. One misfiring plug at 60 miles an hour will degrade engine efficiency by 1.2 miles per gallon.

The average automobile owner trades off the cost and inconvenience of engine tune-up versus acceptable, but less-than-optimum performance. But if gasoline at 60 cents per gallon is coupled with less costly, more consistently effective engine tune-up, he may make the trade-off in favor of improved gasoline mileage. Automated test equipment can reduce the time and cost of returning the engine to near its inherent efficiency.

If the Army has 300,000 vehicles and if they average 5000 miles per year and 10 miles per gallon, the annual fuel consumption is about 150 million gallons. If half the vehicles were in a condition improvable by minor tune-up and 10% improvement were achieved, the potential annual savings would be on the order of 7 million gallons. Of course, the same savings could be achieved by manual test equipment; but a quicker, easier-to-use automated vehicle test meter is more likely to be used and used properly.

There are other incentives for the military user. The DOD must not only contend with increased fuel costs, but with the burdens of supplying fuel to aircraft, ships, and trucks at the end of a long and tenuous logistics pipeline. How much fuel must be expended to deliver 50 gallons of fuel to a truck on Kwajalein Island?

The U.S. Air Force procured 165 million barrels of jet fuel in fiscal 1973.³ A typical modern jet engine is the J-79. Versions of the J-79 power the F-104, F-4B, RF-4B and F-4C. The J-79 develops 17,000 pounds thrust, and in doing so, burns 240 pounds of fuel a minute.

The overall process for jet engine overhaul includes a final test of engine operation through a test profile during which fuel is metered by the engine's fuel controller. The fuel controller is, in reality, an analog computer which deals with such variables as altitude and temperature in determining the proper fuel flow to the combustion chambers in response to requested thrust. The fuel controller is, itself, subjected to overhaul and alignment before it is mounted on the engine, and the engine fired up for test runs. The penalty for incorrect alignment of the fuel controller is having to abort the engine test and replace the controller.



There is also the penalty of fuel expended at rates upward of 240 pounds a minute for no useful purpose other than detecting that a fuel controller thought to be good, was indeed faulty. Using manual test stands for fuel controller testing, the rejection rate is about 10%. With automated test stands, the incidence of engine test aborts due to faulty fuel controller is, for all practical purposes, zero. In this example, the fuel saved is a function of how far into the engine run the test has progressed before the faulty fuel controller is detected, but the rate of expenditure makes for significant savings.

In the long term, automatic test equipment can have a positive, albeit indirect, effect on energy management. As we begin to use alternative energy sources such as coal gasification, nuclear fission, geothermal, and solar resources, the energy content of end products will change. The fuels now used vary from one industry to another. The chemical industry is a primary consumer of petroleum and natural gas, as well as electricity. The stone, glass and concrete industries consume little petroleum products, using largely coal and natural gas. Aluminum production consumes primarily electrical energy, while iron and steel production rely mainly upon coal and coke.

As a consequence of uneven price increases for the different energy resources,

the value of one metal versus another, one insulating material compared to another, may change. Energy content, such as identifying BTU per pound, may become as much a part of the selection process as dollars per pound. Further, the value of repairable assemblies, subassemblies, and components in the logistics pipeline may have to reflect energy content as well as dollar cost. Old trade-offs will have to be re-examined and ATE acquisition cost may appear even more attractive when compared to high energy/dollar content of spares provisioning and downstream operation and maintenance costs.

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CCAT — computer controlled automatic test system

H.R. Lambert

The computer controlled automatic test (CCAT) system, centrally supported, was intended to become widely used throughout RCA. A high degree of success can be claimed for the ten individual systems that were established. This article includes a summary of the history, hardware and software complement, test applications, and a particular example of this computerized test system.

Hugh R. Lambert, Design Automation, Solid State Technology Center, Somerville, N.J., received the Bachelor's degree in Physics from Oxford University, England, in 1951. He spent the next ten years with Ferranti Ltd., Manchester, in guided missile R&D work, specializing in guidance and control, analog simulation, and flight performance assessment. He then worked in Australia at the Weapons Research Establishment, Salisbury, SA, covering field trails for Ferranti Ltd. On return to England in 1961, industrial process control by digital computer became his main concern. In 1963, he joined Electronic Associates Inc., Princeton, N.J., to work in general purpose analog computation, and contribute to the basic software project for the EAI/8400 digital computer. In 1967 he joined the New Business Programs group at the David Sarnoff Research Laboratories, Princeton, where he contributed to various software projects, one of which is the computer-controlled automatic test system. While with NBP he wrote the software for the pilot phase of the supermarket project, besides establishing the control software for several CCAT test systems. Following transfer to the Solid State Technology Center, Somerville, N.J., in 1970, his activities have been concerned mainly with computerized test systems, one of which is the integrated circuit CCAT tester described in this article.



THE CONCEPT of the computer controlled automatic test (CCAT) system was originated in 1966 by the New Business Programs (NBP) group at the David Sarnoff Research Laboratories as a means of providing a standard, centrally supported test system for use in the corporation.

The RCA 1600 computer and Spectra peripherals were adopted to provide computing power and standard input and output capability. However, all the software, which included a real-time executive, a language-defining compiler (SECTRAN), a test program compiler (TPG), a run-time test program interpreter (TPH) and various utility programs, was contracted to Keystone Computer Associates, who discharged the contract with excellence.

A distinguishing hardware feature of CCAT, considered by NBP to be appropriate in a testing environment, is the special equipment controller (SEC) which provides parallel outputting capability of up to 256 eight-bit bytes, suitable for programming in a single computer output operation all the test equipment associated with one test station (e.g., pulse generators and programmable power supplies). A similar parallel inputting capability for gathering several results in one reading operation into the computer is also provided. Design and manufacture of the SEC was carried out within RCA.

Responsibility for corporate applications of the CCAT test system was transferred to the Automatic Test and Measurement (AT&MS) Corporate Staff at Camden,

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Table 1 — Summary of CCAT test applications.

<i>Approximate date operation</i>	<i>RCA location</i>	<i>Test application</i>
1) 1968	G&CS, Camden	Logic board
2) 1968	AED, Van Nuys	Logic board
3) 1968	SSD, Somerville & Findlay	Integrated circuit wafer probe and finished product (9-station, three systems)
4) 1969	CSD, Marlboro	Disc unit 564&594; (2 station)
5) 1970	CSD, W. Palm Bch	Logic board
6) 1971	AED, Van Nuys	Analog devices (shares CPU & SEC with operation No. 2)
7) 1972	G&CS, Camden	Audio and rf devices (shares CPU & SEC with operation No. 1)
8) 1974	G&CS, Camden	Audio/video and rf devices, with enhanced testing features.
9) 1974	G&CS, Camden	High-speed dynamic logic (shares CPU & SEC with operation No. 7)
10) 1975	G&CS, Camden	High-speed dynamic logic, with enhanced testing requirements.

Under their auspices from 1967 onward, nine CCAT test systems became operational. A tenth CCAT test system was recently started by G&CS, Camden, independently of AT&MS, who had gradually withdrawn its active sponsorship after 1972. Two non-testing data gathering systems were also sponsored by AT&MS. These made use of the general executive software provided by Keystone (enhanced later by Keystone to provide support of the 564 disc unit together with disc file management software) and by a FORTRAN compiler bought by AT&MS from the DIGITEK Corporation. These systems were installed at RCA's Memphis and Indianapolis plants. When the disc software became available, test CCAT systems also made heavy use of this facility.

At the time of this writing, eight CCAT test systems are still operational. The two CCAT test systems no longer in existence were victims of the demise of the Computer Division. Also operational is the data-gathering, report generating system originally installed at Memphis, now at Bloomington, Indiana. The other data gathering system was also a victim of

divisional demise. The author has been involved in the design of software on all but two of the CCAT test systems and the implementation of the software of five of them.

CCAT as a general test system has probably come to the end of its career in that no specific new test systems built around the SEC will be established. With the disbandment of RCA's Industrial Automation Systems at Plymouth, Mich., where the SEC was made, manufacture of the SEC is no longer practicable. Also the use of Spectra peripherals to which most of the executive software applies is too costly relative to comparable disc and tape peripherals offered by other minicomputer manufacturers. However, the established CCAT systems continue to render profitable, reliable service, fulfilling the roles for which they were designed. Some, notably those at G&CS, Camden; and those at SSD, Somerville and Findlay, have also enjoyed a vigorous continuing development because of the availability of suitable in-house programming services. The RCA 1600 computer itself has a particularly praiseworthy history of reliability.

Hardware complement

The basic hardware configuration (see Fig. 1) for a CCAT system comprises:

- RCA 1600 minicomputer (up to 65 kilobytes of memory)
- SEC — special equipment controller for interfacing with test apparatus
- Dual magnetic tape unit (Spectra peripheral) interfacing through its control electronics.
- KSR typewriter interfacing through its control electronics

The SEC is the general purpose interface between computer and test equipment required to drive and monitor the product being testing. Each piece of equipment is allotted a range of bytes or bits on the SEC to/from which the computer transfers information either by direct memory access (DMA) covering a range of successive bytes, or by programmed single-byte transfer. Typically, DMA is used to transfer at one time all bytes relevant to one test station.

The SEC also provides a hardware priority interrupt structure, which is not available on the RCA 1600. In practice it was found that the main benefit of this was not the priority feature but the multiplicity of interrupts provided.

Additional peripherals supported on CCAT configurations are:

- Spectra Line Printer peripheral interfacing through a standard interface control electronics
- Card reader interfacing as above
- Card punch interfacing as above
- KSR and ASR teletypes interfacing through a telegraph line controller
- Disc 7 MBYTE — interfacing through its own control electronics
- Video terminal interfacing through a telegraph line controller.

In all but one of the CCAT systems known to the author, the test equipment and SEC interface were always close to the computer. In the one case the separation was approximately 200 ft. However, if it had been necessary, test equipment and SEC could have been situated as far away as 1000 ft provided that the SEC with extender interface were used.

Software complement

The general name adopted for CCAT software is TESTRAN. Available under

the TESTRAN software are the following:

- An executive for handling all acceptable peripherals on an interrupt driven basis and also/the SEC priority interrupts. The executive also embodies a disc data and application program file management system and software for loading, relocating, de-allocating, and interpreting test programs. A complete customized executive configuration may be obtained by a few macro calls.
- A test language compiler (SECTRAN), which permits the definition of a set of symbols to be used in writing of test programs.
- A test program compiler (TPG) which compiles programs written in terms of the defined language.
- A tape utility program (TPU) for maintaining libraries of test programs and application programs on tape.
- A disc utility program (DISCU) for maintaining libraries of test programs, application programs and data files on disc.
- An interactive debug package (CLNCH) written by the author.
- An application program "patch & rename" program (ABSOL) written by AT&MS.

Application programs are normally prepared in RCA 1600 assembly language and assembled on a Spectra computer by the XMAP cross-assembler. A

particularly valuable feature of XMAP is the macro feature, which matches the powerful macro feature of the Spectra assembler.

One of the most important application programs is the control program (TPC) which must be written for each test environment and accounts for the major software customizing effort required with each system. Although the activity scheduler for each CCAT system operates on the same straightforward cyclic polling of each activity, commonality beyond this has not been found, so that it was not practicable to formalize the preparation of control programs, by packaged macros, as was the case with executive software.

The size of an executive to support a typical disc-oriented CCAT system is of the order of 10 kilobytes, while typical control programs are of the order of 20 kilobytes.

Examples of specific CCAT system

The integrated circuit test system in Solid State Division will be briefly sketched as an example of a CCAT system. There are

three installations in the division: one uses tape as the storage medium for test programs, two use disc. The testing requirements are that each integrated circuit must be subjected to a sequence of many test steps, typically 50 to 100, with limit checks conducted at most of these steps. Depending on the combination of limit check results, the integrated circuit is "binned" as qualifying for one of several categories of product, or rejected as a total failure.

Testing is more usually conducted on the integrated circuit while it is still one "chip" of hundreds on a wafer. Special wafer probe machines permit selection and contact with individual chips of a wafer. Testing of individual items of finished product may also be done.

There are nine test stations on one CCAT installation (See Fig. 1). Three stations are serviced by one test set, which multiplexes the necessary power supplies, signals, and connections to the integrated circuits at the three stations. Each set has one typewriter through which the operator specifies the test program, various testing options, and datalogging requirements at each of the three test stations.

The CCAT control program governs the multiplexing of each test set to one of the three stations it services, passes the appropriate next test statement to the current station, and if possible, attends to the processing needs (such as binning or data collection) of stations that are not actually testing and do not require the services of the set. Testing and binning times of integrated circuits on wafers range from a half to several seconds per chip. System throughput is of the order of one hundred thousand chips and better per shift.

Typical of the trend with computer-controlled systems has been the continual evolution and enhancement that has taken place in the software of this CCAT system. To accommodate the requested features, yet preserve adequate computer memory for working areas, overlay and virtual memory schemes have been instituted in the control program. A major innovation not provided in the original TESTRAN software is on-line test program editing and compilation, which may now be conducted in parallel with testing. These various software enhancements have been a major pre-occupation of the author.

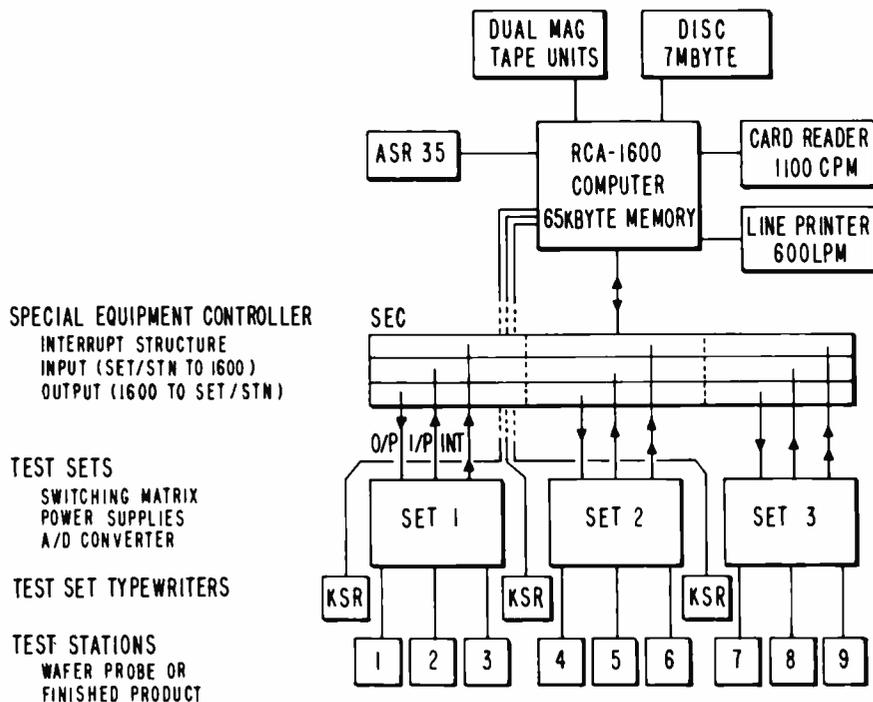


Fig. 1 — Configuration of CCAT System at Somerville and Findlay.

Automated printed-wiring-board design

A.C. Spear

Design automation has been used by the Government Communications and Automated Systems Division at Burlington, Mass. to reduce the engineering/drafting/factory production time cycles for printed-circuit board design and production.

BURLINGTON's design automation system, which automates the printed wiring board design process, is a generalized linkage of programs that were developed and proved-out as stand-alone entities. Included in this linkage are the printed wire routing program, DSGCAR, the interactive graphics station, DA701 AGS, the connectivity checking program, NETLST, the photoplotter drive program, GERBER, the continuity test program for DITMCO and the generation of the control tape for the NC drill machines. The printed wiring boards produced by this self-checking automated system move from release to fabrication in a much shorter time span than previous methods permitted, and fabrication problems and quality rejects are almost eliminated. Two factors contribute to this: 1) the error checking routines which insure that the precision artwork is a direct reproduction of the schematic or logic diagram, and 2) release being made closer to the required start of production reduces in-process engineering changes.

Depending on the complexity of the

printed-circuit board layout, the design draftsmen may use all or only a few of the programs in the linkage. Simple two-sided boards do not require the use of all the programs. The steps of the design automation process are shown in Fig. 1.

As a board family requirement is defined, certain mechanical information is fed into the design automation system: the board dimensions, the available routing area, position of mounting holes, type of edge connector, row and column spacing for component holes, and the hole patterns for all the components expected to be used. Once captured in the design automation system, the data can be called up as needed and does not need to be regenerated for each board to be routed. If a previously defined board family can be used for a new project, this mechanical data is immediately available and non-recurring costs on the project are consequently reduced.

There is no limit as to the types of components, except that their mounting hole patterns must fall on a regular grid, preferable multiples of 0.025 inch. On any

one board there may be any mixture of components. Even single-leaded components such as a test point or stand-off terminal can be accommodated.

Once these mechanical requirements are established and checked for accuracy, there are only two sets of data which have to be generated for all the other boards of this family: 1) the component placement and 2) the interconnections to be made by the etch runs. The placement is made with a grease pencil sketch on mylar regardless of complexity; the interconnections may also be sketched, or, if it is to be routed using DSGCAR, the net listing will be coded for key punch. Placement is entered in DSGCAR by giving the row/column location of pin 1 and the reference designation, i.e., Z12, C6, R22.

Amy C. Spear. Government Communications and Automated Systems Division, Burlington, Mass. received the BSEE from Cornell in 1948 and the MSEE from Northeastern University in 1966. As a member of the System Design Support section, she provided staff support in plans and performance of all aspects of systems effectiveness and logistics support analysis. In addition, she was responsible for coordinating and advancing the division's Design Automation capability. She was instrumental in bringing the Automatic Artwork Generation program into a fully operational status. She also established several additional computerized systems for data collection and analysis and record keeping. She is currently developing the interfaces to link many of the existing design automation programs into a cohesive system. After joining RCA in 1963, Mrs. Spear was engaged primarily in the fields of Product Assurance and System Effectiveness. From 1963 to 1965 she was assigned to the Reliability Program for the LM radars. Moving to the LM PMO in October 1965, Mrs. Spear monitored and directed the reliability effort on all LM contracts, participated in LM subcontractor design reviews, coordinated and reviewed failure reporting and analysis, requiring additional corrective action where necessary. She assumed the position of Manager, LM Product Assurance in February 1967, and served in this capacity through the early Apollo missions including the first moon landing.

Since this article was written Mrs. Spear has left RCA.

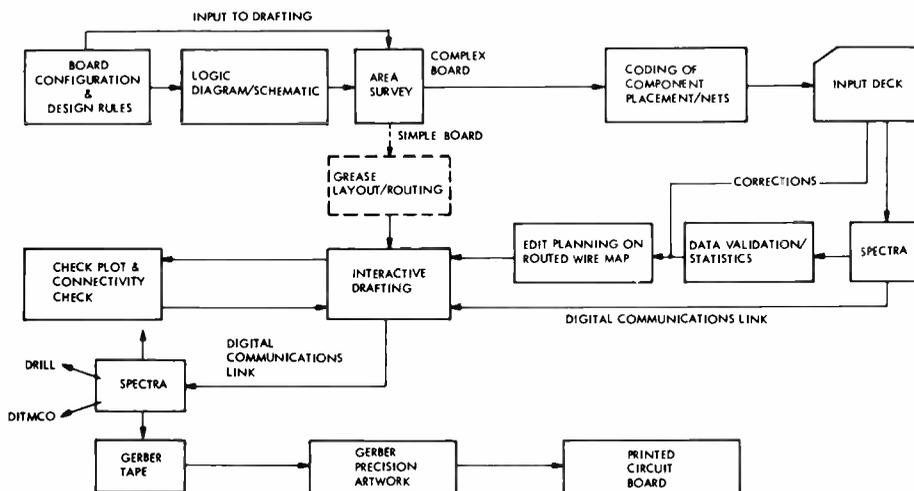


Fig. 1 — Steps in the design automation process.



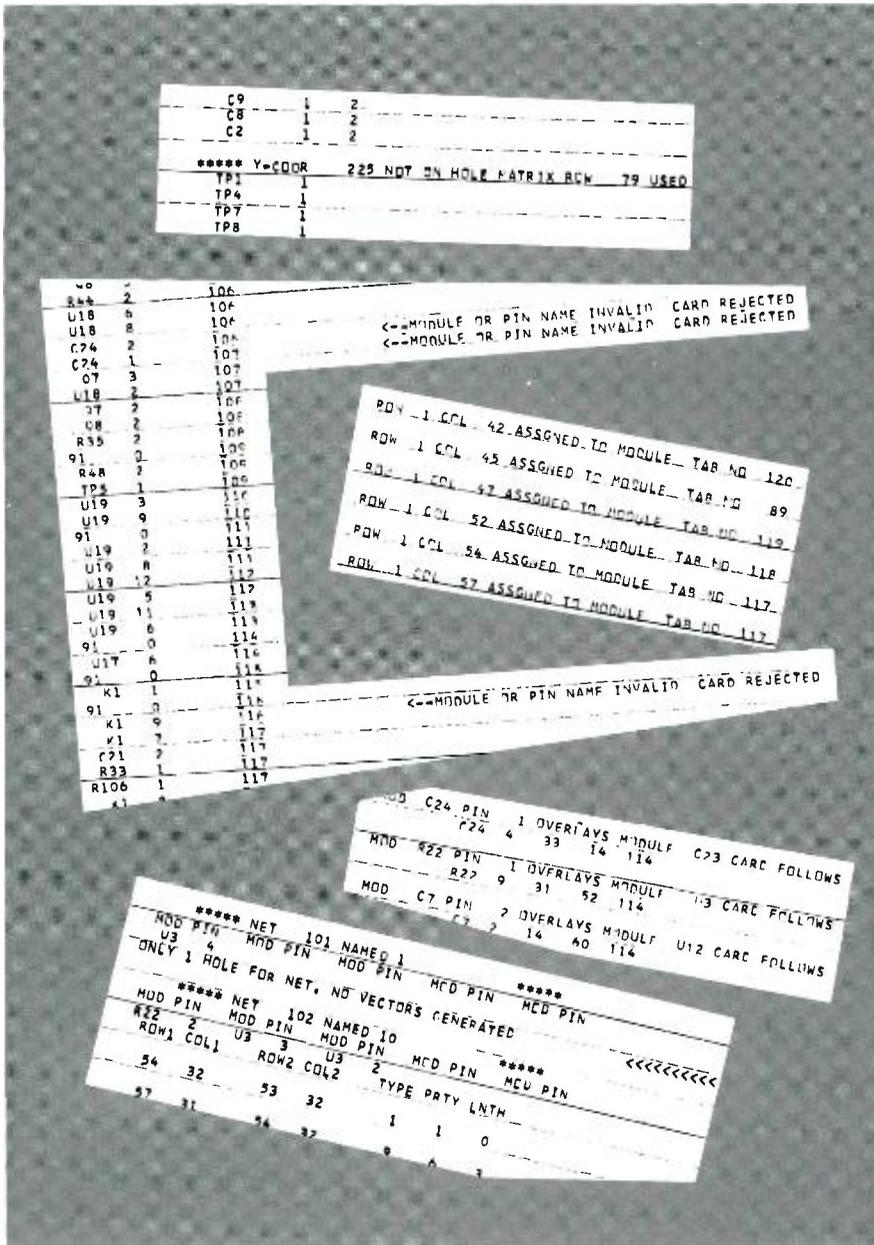


Fig. 2 — Error messages.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
1							M	M				M	M										M	M	
2																									
3								M	M				126	M					157	162				248	M
4							M						M	183					123	245				243	250
5																								M	252
6	101																								
7		102																							
8																									
9	148	159																							
10																									
11																									

Fig. 4 — Hole map.

BREAKUP STATISTICS		
TYPE	VECTOR	LENGTH
1	35	35
2	29	176
3	30	122
4	8	36
5	1	5
6	0	0
7	7	14
8	71	268
9	31	163
10	8	124
11	7	221
12	0	0
13	13	86
		578
HORIZ TOTAL	163	972
VERT TOTAL	124	1690
		1779

Fig. 3 — Net break-up statistics.

The source for this data is the schematic or logic diagram.

User orientation

When the design automation system was made operational in the Burlington plant, one of the first considerations was to create a user-oriented system that would make it an easily usable working tool. To this end, the method of entering data into the wire routing system was evaluated by the initial group of draftsmen to use the system. The programmer's approach, which made maximum utilization of the 80 column card, was changed to a simpler form that reduced entry and key punch errors to an insignificant amount.

Error checking

The error checking routines built into the first subroutine of DSGCAR are designed to screen out other human errors, such as a mistake in locating pin 1 of one component which caused it to overlap another component. Other errors it checks for are:

- Calling for a component pin in two different nets.
- A net that has only one end of an interconnection.
- A net that calls for a component pin that was not placed.
- A component that was placed such that its hole pattern did not fit the established grid or fell on a forbidden hole.

Typical error messages are shown in Fig. 2.

The first subroutine also breaks up the nets into horizontal and vertical routing

vectors, placing "via" holes where necessary to break up diagonal interconnections into the preferred horizontal and vertical etch runs. It also sorts down the vectors by type and length, and lists them by net. It compiles the statistics on the number of each part type, which can be used as a guide to ascertain the probable success of the router, and it prints a graphic representation of the board with the holes as placed and via holes identified. Net break-up statistics are illustrated in Fig. 3, and a hole map is shown in Fig. 4.

Since this subroutine requires only 10 to 15 minutes of computer time, the amount of data resulting can insure that the longer routing subroutine will run without a problem or without expensive reruns. It is worth running this short subroutine several times to be sure the data is error-free and the net lists and statistics are good before running the 45 to 60 minute total routing program.

Routing program

The total routing program has two main outputs: 1) the graphic representation of the vectors routed and the accompanying unrouted vector list and 2) the translation into the interactive graphics terminal data base.

It would be well here to note the restrictions intentionally entered into the routing subroutine. The program was not designed for 100% completion of the routing. The introduction of the interactive graphics terminal made it economically undesirable to introduce into the router all of the human decision making for the alternatives in order to accomplish complete routing on the designated number of layers. As a corollary, the program is not permitted to add layers to complete the routing. The number of wiring layers is a design decision which can be any even number and is entered as a parameter card in defining the board to the computer.

Thus, there is always a small percentage of unrouted wires in the list accompanying the chain printer graphic representation. These are used together in planning the changes to be made in order to place the remaining routing vectors. Once entered into the graphics terminal data base, a picture of the routed board can be called up for display on the storage

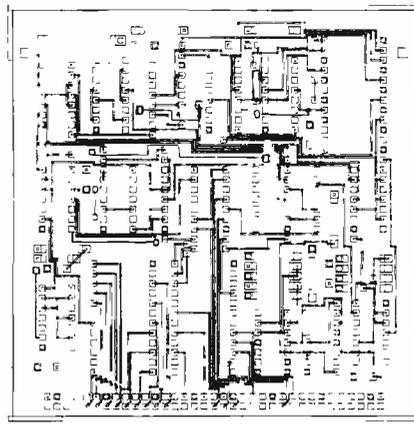


Fig. 5 — CalComp checkplot with planned editing.

tube or plotted on the CalComp ink plotter (see Fig. 5).

When changes are made using the graphics terminal, these changes are immediately captured in the data base and are shown to the operator in the scope display where he can check to see that they were made correctly. The ease and inherent accuracy of making changes using this system permit the introduction of engineering changes quickly and without the errors that were frequently made in the manual method.

Once completed, as accurately as the draftsman can make it, a scaled-up ink plot is made to assist the engineering check. For simple boards, this plot may be all that is required to be sure the board is an accurate representation of the schematic. For complex and multilayer boards, such a manual check requires several days of engineer and engineering aide time to complete; even then they may have missed an inaccuracy.

Connectivity program

The connectivity program, NTLST, is a time saving tool to assist this engineering check. To eliminate the possibility of an initial coding error, the net list is again coded from the current schematic/logic diagram. This desired connectivity is compared in the computer with the completed connectivity in the graphics terminal data base. Any discrepancies are listed as an output. This list of discrepancies is always quite small and the program does not attempt to judge which source is correct. It has proven to be a simple job for the engineer and the draftsman to find the source of the error. This program reduces a tedious, error-prone, expensive process to a ten-minute

computer run and about four hours each for the draftsman and the engineer.

Outputs of the D.A. system

When all the checks have been completed, the design automation system is exercised to generate several outputs from the common, verified data. A drive tape is created which is sent to Camden to drive the Gerber Photoplotter resulting in the glass masters at 1:1. A 1:1 ink plot is made to provide Camden with a checking tool for the masters. Drive tapes are provided for the numerically-controlled drill machines in the factory. In each of these programs, the data is sorted to insure that the light and drill heads have a minimum excursion and indexing.

If the board is complex and it becomes cost effective to provide DITMCO-automated continuity testing on the finished boards (before parts are added), the desired connectivity will be translated to an input for the DITMCO.

The design automation system for printed wiring boards has been fully operational at Burlington since mid 1972, and all boards fabricated in the plant now come out of the system. About one-third of all the boards were considered sufficiently complex to require using the total system; the other two-thirds were routed using the draftsman's sketch and the interactive graphics terminal.

The ease with which the Gerber drive tape can be generated and the resultant improvements in factory yield make the use of the Gerber for precision artwork a cost effective process even for simple boards. Previous rejections for having too thin an annular ring after drilling the pads have essentially been eliminated because of the precision artwork and the fact that the drill tape was generated from the same data.

Just as the drafting time cycle was reduced, the factory's fabrication cycle was shortened and in both cases rework with its subsequent degradation of quality was reduced. On several critical programs, it was possible to meet seemingly impossible schedules. As the design engineers have gained confidence in the design automation system, they are willing to release schematics later in the program, with the result that there are fewer changes generated after the initial layout.

Test support software

P. Schwartz

Present-day radar systems are often so complex that sophisticated testing facilities are necessary for debugging and checkout. Typically, the test device requires programmable stimuli, display/print capability — and should permit an interactive dialogue with the test director. Manual test generator/evaluators result in a relatively inflexible and prohibitively expensive test method. Thus, a computer-controlled test facility with appropriate peripherals is indicated. Such a test model is described herein, delineating the major properties and performance requirements of the computer-peripheral hardware configuration and associated software package.

A COMPLETE and modern test facility should support the debug/checkout effort with a cradle-to-grave approach. That is, it should be capable of implementing all required tests from the start of equipment integration, through completion of Category I (subsystem) and Category II (system) testing.

The cost effectiveness of such a test facility, when efficiently developed, is readily apparent, especially when the test facility design is sufficiently general and

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modular to serve more than one application without excessive modification. There are, thus, two distinct possibilities.

First, the test facility can be designed as a semi-permanent, flexible unit capable of testing any large, complex electronic system with minimum adaptive modification; in this case, it may be prudent to make the computer and associated software a capital expenditure (Fig. 1).

The second possibility (as done in smaller systems) is to plan the test facility from the start as an integral part of the system to satisfy checkout and monitoring (CAM) and other diagnostic functions.

In the first case, with the large system, it is likely that the system will contain an integral control computer that may ultimately also serve as the built-in checkout computer. Software must be designed with this application in mind... to be ultimately adaptable to the host computer with only minor modification *before selloff*.

Test support requirements

Major requirements of the test facility and suggested methods of implementation are described below under the following subtopics:

- Applications of test support software
- General requirements of test support software
- Recommended computer configuration
- Structure of test software
- Test language

The first part of each description below is devoted to the general requirements for that topic, whereas the second part defines a workable implementation approach as demonstrated by a typical test software model, AFSTEP. However, the

thrust of this paper emphasizes the general performance requirements of test support software. AFSTEP is used as a practical, reference model.

Application of test support software

A computerized test program is required for many complex systems. Such electronic systems, even with computer-assisted testing, often take three to six months to complete checkout. Manual or less automatic methods make the testing program prohibitively long and frequently result in inadequate testing of many system functions. System bugs and performance inadequacies, unfortunately, are often not discovered until the system is finally integrated. Typical complex electronics systems which require test support software are:

- 1) signal processors
- 2) data communication systems
- 3) industrial processors

For example, the signal processor starts at the receiver i.f. stage and its output drives the system displays. The computer peripheral configuration (Fig. 2) must be able to support all required display/print operations and operator interaction and control functions.

A typical data communication system (DCS) can be represented by a model consisting of a simulated, demodulated serial data-stream, under computer program control, driving the DCS decoder unit. The test computer and software determine both the error rate of the source data and the ability of the DCS data decoder to extract meaningful information.

As a third example, a test computer can be used to control a synthesized analog and/or digital stimulus fed to an industrial processor (IP) under test. In addition, the test computer and its peripherals could verify the ability of the IP to implement linear displays and recordings of the synthesized stimulus information content. The IP may also be evaluated for its ability to indicate status of monitored events and to initiate out-

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Final manuscript received January 27, 1975..AFSTEP (AFAR Signal Processor Test Program described in this paper) was developed to perform required tasks for the AFAR radar (Advanced Field Array Radar, Contract DAHC60-73-C-0014), program for running on a minicomputer (PDP-11). AFSTEP permits use of either operator-programmed stimuli or individual test programs as a debugging/performance evaluation tool.



of-limit alarms. In the following discussions, the signal-processor example is used as the system model under test.

The test-support-software program should be modular and capable of being run on a minicomputer. It must be flexible to permit operator-injected stimuli and, as well, sets of individual test programs. It should be designed to be useful from the start of subsystem debugging through total system performance evaluation.

General requirements of the test-support software

The developed test software should support the system test effort through all test phases. That is, at the beginning of the checkout period, the software must offer straightforward test techniques to be used during the initial debug effort. As additional electronics (both digital and analog) are added during the system integration phase, the test-support software should correspondingly provide more equipment debugging capability. The test-support software must also be sufficiently flexible to allow the debugging effort to proceed regardless of the order of equipment integration, or the failure of a particular subsystem under test. During the final test phase and system sell-off, the test software must be capable of providing both varied and complex stimuli that are readily programmable. Also, test results should be printed out and/or recorded for either immediate analysis or later data reduction and analysis.

The test software should have at least two basic modes of operation; 1) operator mode, and 2) test-program mode.

In the operator's mode, individual typewriter keys (herein called function keys) are available for the initiation of a corresponding testing aid. Two of the keys comprise the test-program mode to 1) select, and 2) start a particular test program. These function keys, contained on the alphanumeric display terminal, are used as the man/machine interface. The operator's mode, especially structured to support initial hardware debugging, should offer several capabilities:

- Staticize the required system functions.
- Output a programmable stimulus at a periodic rate.
- Read/print system data reports resulting

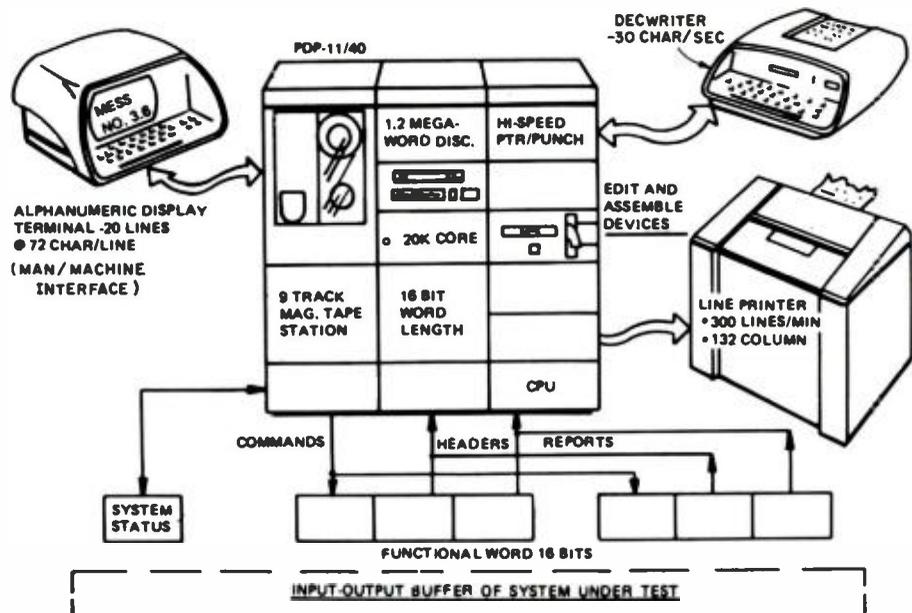


Fig. 1 - Hardware test configuration - PDP-11/40 and its peripherals.

from a programmed stimulus.

- Display/modify selected parameter fields of addressed command block (set of stimuli).
- Provide utility functions:
 - a) display/modify any specific core location.
 - b) print out all memory data between two limit addresses (core dump).
 - c) display/print out all stimuli and simulated return data.
 - d) initiate simulation mode for debugging individual test programs.
 - e) permit independent operator override of test program message display printout, and
 - f) provide addressable test program breakpoint.

The most commonly used test artifice during the initial hardware debugging period is the ability to output stimuli in a periodic manner. This feature enables the test team members to externally synchronize their oscilloscopes and then monitor pertinent system waveshapes with minimum lateral, time-jitter of the waveshapes.

Initially, only a continuous, rudimentary test pattern is transferred across the

computer-I/O buffer interface. The test program permits the operator to compose the rudimentary pattern. That is, the operator selects the sequence of individual commands and the time (leading edge-to-leading edge) between commands (see Fig. 3).

As system development progresses, the operator begins to examine system data reports. The variable number of reports is organized into a data unit called a report block. The data content per field of the addressed report block may be displayed in any code dictated, such as both decimal and octal. The test program should permit the command-block/report-block sequence to be performed on a single cycle or continuous basis, where the response to the last "n" commands is available for analysis.

As an example, the operator mode of software should permit the operator to program a periodic or single-cycle command that defines a simulated receiver signal amplitude. After the signal amplitude has been measured by external

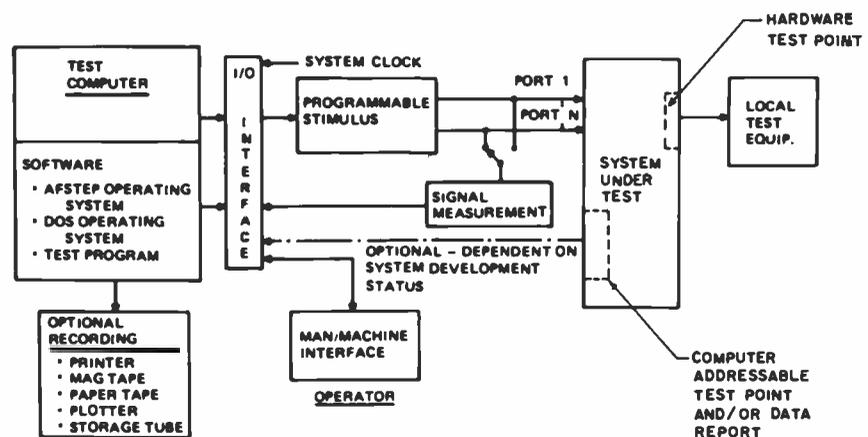


Fig. 2 - Typical system test configuration.

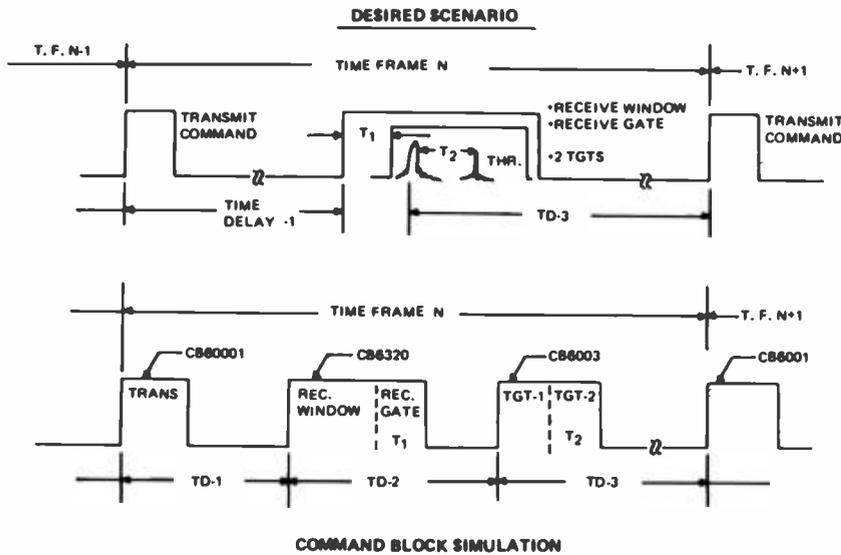


Fig. 3 — Scenario composition by FK-2 or test program.

test equipment (part of the analog-digital signal simulator), the commanded amplitude is modified by changing the signal amplitude control field in the command block. If the equipment under test is in such a completion state that the data report contents are receivable and processable, then the reports are printed or displayed by operator selection. Thus, a complete command/response loop may be simulated in sequential operator-controlled steps. Finally, when the hardware system reaches the final stages of development, the more complex test programs will be even more useful. Test programs are designed to contain the following properties, depending on their application:

- Automated sequence of commanded stimuli and storage of received data reports for "n" (programmable) iterations.
- Real-time processing and evaluation of these data reports.
- Test program interruption for display/printing of critical messages.
- Structured test programs that permit performance of first level of real-time data processing. As an example, a given measurement is repeated "n" times, and the test program then computes the average (and rms value) and variance (e.g., 1 and 3 sigma) of a specific received system parameter. These statistical computations remove the measurement uncertainty normally associated with complex electronics. If more comprehensive computations are required, the raw data must be stored for later analysis.

The test programs for a radar system will probably have no time scheduling problems in performing required computations because a radar beam (or other set of commands) is scheduled only after all computations pertinent to the last

radar beam (or set of commands) are completed.

Recommended computer configuration

A recommended economical computer configuration to support test support software consists of:

- 1) A minicomputer with adequate core size. This implies a nominal 1- μ sec memory cycle time and 16-bit word length. Data parameters of greater than 16 bits length can be separated into two parts, e.g., PARH1 and PARLO.
- 2) A line printer capable of a minimum of an 80-column page format and a 60 line/minute print rate.
- 3) An alphanumeric display terminal with its own refresh memory, keyboard, and standard cursor control for the man/machine interface.
- 4) A medium-capacity disc; this is the nerve center of an efficient test computer configuration. The disc is used to store all computer-supplied and test-support software. Since the disc is file structured, all program modules are stored and accessed by their file name — NAME.EXT.
- 5) High-speed punch/reader (paper tape) containing initial version of larger test programs.
- 6) Magnetic tape recorder to store high-volume test data that will be analyzed/reduced in an offline operation. It may also be used as disc backup.
- 7) Computer-supplied software, preferably including a versatile operating system, editor, assembler, Fortran compiler, linker, librarian, utility, and debug programs. This vendor-supplied software dictates the ease of test program development and controls its ultimate capability. It is a major component in determining the cost effectiveness of the test facility.

Structure of test software

Test-support software has unique structure requirements over and above the standards of general-purpose programs. These requirements result from the peculiar needs of test personnel (whose principal orientation is not software) to develop and use software tools in the checkout of sophisticated electronic systems. In addition to a straightforward approach for the user and developer, the final product must permit fast and efficient checkout of the system under test in a time-equals-money environment. A number of characteristics are essential to test-support software, such as:

- Modular structure.
- Ease of usage to allow test personnel full program utility without extensive training.
- Straightforward software organization with a comprehensive instruction repertoire. The software should be customized to interface with hardware test requirements. Frequently used test coding should be included as part of the test language instruction (TLI) repertoire. TLI's are synthesized computer instructions, structured as subroutines or assembler-recognized macros.
- Maximum use of vendor-supplied software.
- Controlled management of the development of the operating program, each test program, and each stimulus.

The test software organization is best described by defining the contents and creation of a load module. As shown in Fig. 4, a load module is any core-resident operating program. The figure also shows the steps involved in developing the test-program load modules: the load module is made up of object modules derived from four sources, the test program itself, and three libraries. A library is a collection of independent object modules, with each of the modules having its own disc file name (NAME.OBJ). All the object modules within a library are available for inclusion in the load module if the library is included in the linking operation. Thus, the representative keyboard command statement for the composition of a test program load module is:

```
TSTNAM.LDA<TSTNAM.OBJ,
AFSTEP.LIB/L, GENLIB/L,
FTNLIB/L/GO where NAME.LIB/L
indicates a library and GO indicates
execute the TSTNAM.LDA program.
```

The complete set of object module components of the typical operating program is contained in the test program library (AFSTEP.LIB in the example above). GENLIB contains all command blocks,

report blocks, support Fortran subroutines and developed general-purpose subroutines, all stored under their own file names. FTNLIB is the set of Fortran subroutines that support the running of any program written in Fortran IV compiler language.

The co-resident Disc Operating System (DOS) monitor performs several major functions during the running of the test program:

- Provides the drivers (interface program modules) to the printer, keyboard and magnetic tape.
- Contains SYSMAC.SML (system macros) which is a library of the definitions of all macros, both permanent in the DOS software system and user defined. A macro is a subroutine having a NAME recognized by the macro assembler in the computer. A macro definition is the listing of input and output arguments to the subroutine and the actual machine language (PDP-11 instructions) expansion of the subroutine. For the user-defined macros (actually the test language instructions) the format and subroutine input-output arguments are listed in SYSMAC.SML, but the supporting subroutines are contained in the test program library.
- Monitors any invalid program operation.
- Maintains software on disc: a single disc-to-disc transfer permits the saving of all developed software.

The test program is also structured to contain an adequate number of display messages. The message display technique is used to give instructions to the test engineer (e.g., SET ATTENUATOR NO. 3 to 5 dB) and permits the test engineer to control the test program branching. The latter is performed by having the display

message instruct the operator to insert specific codes into indicated core locations via the assigned function key.

The test program software should make maximum use of computer (vendor) supplied software such as that used for edit, reassembly, library, link, and utility processes.

Interface program modules (device drivers) should be used for peripheral data interchange and are usually integral to minicomputer operating systems.

The test program modularity must also be exploited. Individual program modules can be components of threads initiated by function keys and test language instruction.

Test language

The implementation of a versatile, easily understood and applied test language is a requisite for any test software. Principal characteristics should include:

- Modest development time.
- Straightforward, simply applied instruction repertoire to accommodate programmers with limited software background.
- Instruction repertoire that is sufficiently comprehensive to permit easy coding of all test programs.
- Test language instructions or subroutines for repeated test-program coding.
- Flexibility for development of additional test language instructions on an as-needed basis, and
- Specially developed subroutines as part of the test language instructions mix.

An all-interpretative test language struc-

ture should be implemented only as a last resort when the requirement for a higher level test language is dictated by test programmer limitations. An all-interpretative approach is expensive to develop, uses a large amount of core, and can easily increase the program running time by a factor of 50-100. The test language should be composed of three instruction subsets:

- 1) The normal assembly language instruction set of the minicomputer used.
- 2) A specially developed test language instruction (TLI) set, and
- 3) Fortran IV (ANSI) instruction set.

An individual TLI should only be developed if the functional equivalent cannot be obtained via the supplied minicomputer instruction subset or the Fortran library. Usually such TLIs are special purpose functions unique to the system testing effort.

Conclusions

Test-support software implementation must have inherent flexibility and test efficiency that can be obtained from the imaginative design of test software. It is also clear that the implementation should exploit all test-support advantages that may be accrued. Furthermore, the program must be designed for use by hardware-oriented personnel. It should permit full printout control but with minimized test running time (rapid test completion). Its modular structure makes modification (such as the addition of function keys) relatively easy and adds program flexibility. It should also include a hardware simulator for test program debugging and checking. For extensive, sophisticated equipment test programs, the purchase of capital equipment is frequently desirable. The use of more powerful computers, additional peripherals, further software design, more advanced simulators, etc. will enhance this valuable test tool capability.

Acknowledgments

The work of B. Longmire is gratefully acknowledged; without his ingenious program coding technique and incorporated suggestions, AFSTEP and would have been a far less powerful test tool. W.S. Perecinic provided the opportunity and motivation for the development of AFSTEP and for the preparation of this paper.

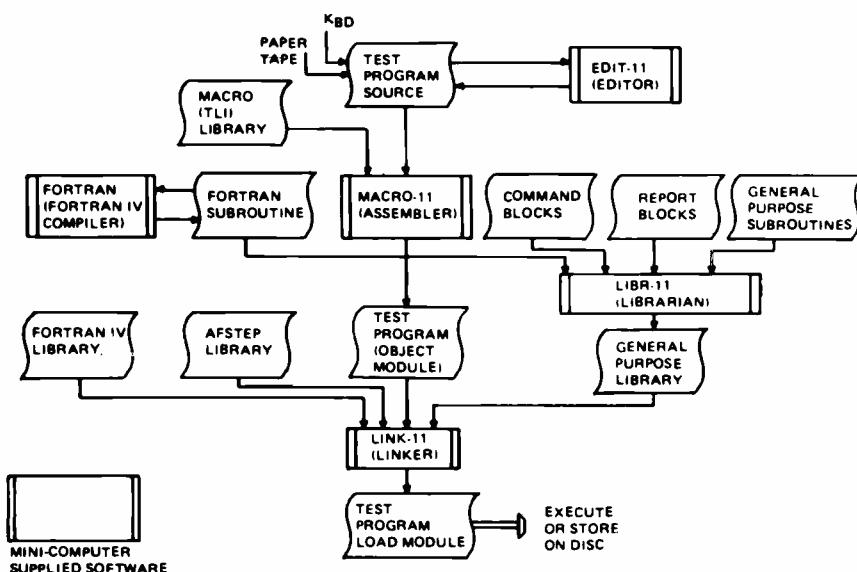


Fig. 4 — Test program development.

Adult II test system

V. L. Fowler | M. T. Roden

ADULT II is a computer-driven, linear integrated circuit (IC) dynamic test system. The software for the ADULT tester was developed for RCA in 1970 by General Automation to meet the requirements of an economical test system that would facilitate high-volume dynamic testing. Significant software and hardware enhancements to the ADULT system have resulted in a tester, the ADULT II, with more capabilities and flexibility to facilitate the dynamic testing of linear IC's in engineering and production environments and have minimized system down time.

PRIOR to the ADULT tester, dynamic testing of linear integrated circuits involved complicated hardware procedures to set up the test sequence, and meters and oscilloscopes were used to measure the output of the unit under test. This method of testing was time-consuming and prone to operator error. The ADULT II system presently is used by Linear Engineering in Somerville; Linear Engineering Production and COS/MOS Type and Test Engineering in Findlay, Ohio; and Linear Production in Taiwan.

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There are currently 12 ADULT II systems operational at these three locations.

ADULT hardware system

The ADULT test system is based on a General Automation SPC-12 minicomputer with 8 kilobytes of memory which is time-shared among 3 test stations and a terminal (see Fig. 1). Time-sharing divides the cost of the central processor

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among the test stations to make a more economical system configuration. The approximate cost of an ADULT II system is \$34 000.

The test station panels display information about the current test being performed and the unit under test. The panels also provide operator control over several hardware testing functions, such as the various methods used to step through the test sequence.

The device to be tested is inserted into a socket on the test set. The test sets are designed for a particular function or device to be tested. For example, the CA3068 pix i.f. circuits for the RCA XL-100 color television receiver require special rf signals which are built into the hardware of the test set. Relays in the test set are controlled by test information stored in memory. In the test, bits which correspond to the relays are set 'on' or 'off.' The computer then transmits dc logic levels to the test set according to the bit configuration in the test to open and close the relays. The electronics internal to each test set use these relays to apply electrical stimuli, whether ac, dc, rf, or another type of signal which is dependent on the test set hardware, to the device under test.

The test stations contain power supplies for the circuits and relays in the test set hardware. A programmable power supply for each test set is controlled by the test program and provides flexibility in dc testing and bias supply. Since the test system only provides control over the relays in the test set and the signal applied to the device is implemented in the test set hardware, the ADULT system provides flexibility in dynamic testing.

ADULT software system

Dynamic or ac testing on the ADULT system involves the application of a signal, which is implemented in the test set hardware, to the device and measuring the output of the device which is also dependent on the hardware of the test set. A test program resides in memory for each test station, and each test in the program contains specific testing information for the device under test. Examples of the type of information are the relay configuration in the test set and (to permit stabilization of the output signal)

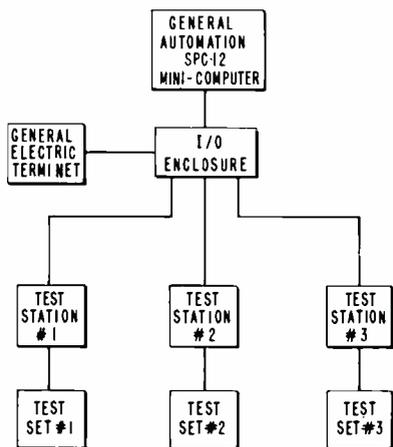


Fig. 1 — Adult II test system.

the time delay before the output of the device is to digitized.

To determine whether a device passes a test, the digitized or test value is compared to limits stored in the test in memory using one of four algorithms:

- 1) The test values against the limits in a straight comparison.
- 2) The difference between the test values of the previously performed test and of the current test is compared to the limits.
- 3) The ratio of the current test reading to the value of the previous test is compared to the limits. and
- 4) The value of the previous test is compared against the limits (this permits multiple limit checks of a test value).

If the test value is not within the limits, the unit fails that test and information in the test indicates the bins or modes of acceptability for which the unit is to be disqualified. There are twelve modes of acceptability and one failure mode. Thus, the final mode of acceptability for which the unit qualifies, determined after all the tests have been performed, is dependent upon the tests which the unit failed.

Dynamic testing on the ADULT system includes measurement of distortion, limiting sensitivity, gain, linearity, and AGC characteristics, and is dependent on the design of the test set. To test linearity on the CA3068 pix i.f. circuits, the 45-MHz input is modulated by a staircase waveform repeated every 64 μ s. The maximum amplitude of the output, which is a demodulated staircase, is measured and must fall between 4.0 and 9.3 V. At each step of the staircase, the sampled output is compared to the maximum amplitude of the staircase and the

resulting percentage must fall within quality limits established for the CA3068 circuit. To test limiting sensitivity on the CA3065 television sound i.f. circuits, the 4.5-MHz input is frequency modulated by a 400-Hz sine wave with deviation of ± 25 kHz (maximum modulation level for a television sound channel). The input signal level is set at a level of 100 mV rms and the measured audio output must be between 0.5 and 1.2 V rms. The input signal level is then set to 400- μ V rms and the audio output is measured and compared to the first audio measurement. The second measurement must not be less than 70.7% (-3dB) of the first for a unit to pass the quality limits for the CA3065 device.

The General Electric TermiNet provides hard-copy datalogging of the test results for each test applied to the device or summary information accumulated on a lot of units, such as the number of units failing each test in the program and the number falling into each mode or bin of acceptability. The TermiNet also allows operator interaction with the software to select various methods of datalogging, such as logging all units tested or logging only units that qualified as failure, or to exercise control over the test program and various modes of testing, as for example, editing of the test program or omitting certain tests from the test sequence. The TermiNet paper tape reader is used for loading the operating system program into memory and for test program entry. The paper tape punch may be used for datalogging test values and test programs.

Improvements to original system

After a study in 1972 of the ADULT tester developed by General Automation, several enhancements to the software and hardware were recommended to better meet user requirements. Utilization of the existing software and hardware minimized development costs. However, several software and hardware testing features were added to permit greater flexibility in testing, such as the addition of the programmable power supplies. Also, additional test and device information are displayed on the panels of the test stations.

The original ADULT tester utilized an ASR33 Teletype. Replacing this unit with

a General Electric TermiNet significantly reduces the time required to load the executive system and test programs into memory. Performing input/output at the TermiNet does not require the test stations to stop operating as in the original tester. The addition of a basic instruction set which is entered via the TermiNet permits operator interaction with the software to control various modes of datalogging, testing, and editing of test programs. In the earlier system these features, not available on-line, required the three test stations to stop operation to read or change certain locations in memory via the computer console. One of the major accomplishments in the ADULT II tester is the formation of an "operator proof" system. With the earlier software, the tedious methods needed to retrieve data, select testing options, and edit test programs often resulted in the system crashes due to operator error. These down periods were costly in the production areas.

The new features and enhancements were incorporated into the existing software by E. Helpert, Design Automation, and resulted in a major restructuring and rewriting of the software. Equipment Technology and Linear Engineering in Somerville updated the hardware in parallel with the software enhancements.

Summary

Version 18A of the ADULT II operating system has been operational at three RCA locations since November, 1973. In September, 1974, version 19 of the operating system was released with a modification to the datalogging of test values and an additional test program editing feature. Further major software enhancements to the ADULT II system are restricted because the continuing development of the system has resulted in a shortage of memory space.

The software and hardware enhancements to the ADULT system have resulted in a tester, the ADULT II, with additional flexibility and facilities for the dynamic testing of linear IC's in both the engineering and production environs. The successful development of the ADULT II tester has led to the inquiry into a future generation dynamic tester with additional capabilities over the ADULT II system.

Test data analysis for device and process characterization

R.F. DeMair

Device and process characterization is an important step leading into process control. Process control involves the monitoring of material and process variables in the manufacturing of integrated circuits both in-process and upon completion. Such procedures produce quality devices at higher yield and thereby lower cost. The purpose of test data analysis is to acquire and analyze electrical parameters and failure modes on devices at various steps in the manufacturing process. The results are correlated to material and process variables so that means are established for corrective action.

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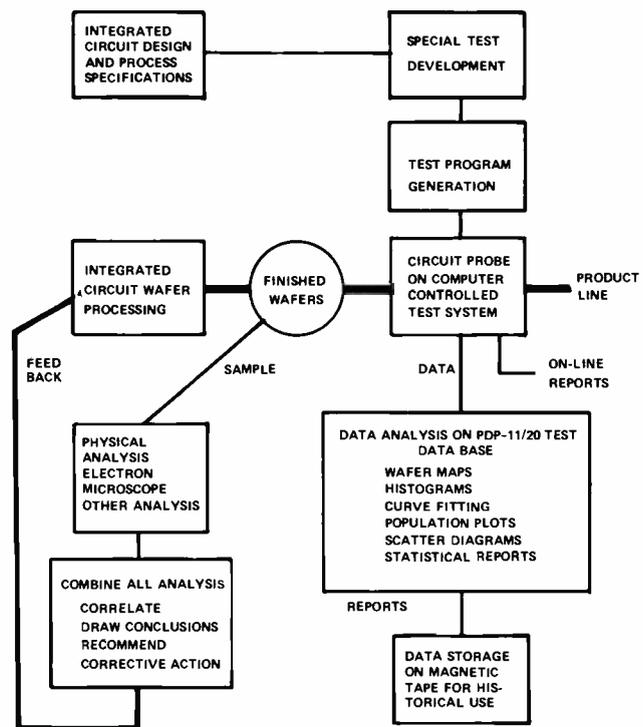


Fig. 1 — Process control program organization.

TEST DATA analysis consists of answering the four basic questions:

- 1) Which data is to be analyzed?
- 2) Where is the test data acquired?
- 3) How should this data be analyzed?
- 4) What is the meaning of the analysis?

These four steps for successful data analysis are very highly interrelated. It is just as foolish to provide sophisticated analysis programs without relating the results back to the process or product, as to acquire large volumes of data, hoping that some conclusions will mysteriously emerge. For test data analysis to be meaningful, then, consideration must be given to these four basic areas. Generally, it requires process knowledge for determining which data to analyze, and for interpreting what to do as a result of the analysis. For establishing the how of the analysis, device testing and computer applications expertise is required.

The organization of a process control program makes use of the four aspects of test data analysis (Fig. 1). From the integrated circuit design and process specifications, the type of data for analysis is established. Through test development, test program generation, and circuit probing on a computer-controlled test system, the data is acquired. Data analysis is then performed by computer using special analysis

programs. Data is interpreted, corrective action is fed back into the processing area, and the final results are evaluated.

Which data is to be analyzed?

Data is acquired at many points in the manufacturing and testing cycle. Resistivity measurements are made on wafers early in the production line. Wafers of pellets consisting of resistor arrays have been specially made to evaluate the ion implantation process. Test samples of key circuits containing transistors and resistors are placed on wafers for acquiring data. The type of electrical data obtained is a function of the process technology. For bipolar devices, the parameters measured are leakage current and breakdown voltage between elements, beta, saturation voltages, and resistance. For devices manufactured using COS/MOS technology, the measurements include leakage, breakdown, resistance, current gain and threshold voltages. As will be explained later, the threshold voltages on N and P devices are measured over a range of drain currents and substrate bias voltages for special analysis.

For producing maps of wafers, data for all pellets on a wafer are recorded along with their locations. Positional information is expressed in terms of a two digit X and Y coordinate value. The center test

key of a wafer is usually assigned some reference, such as 50,50 ($X=50, Y=50$).

Data is also obtained on the integrated circuit while still in wafer form. At circuit probing, each pellet is tested to determine whether it is to be subsequently mounted and bonded into a finished device. The types of tests are similar to those performed on packaged units, and the bad devices are linked for discard at separation. While probing however, both variable (test value) and attribute (test pass or fail) data can be recorded. The data relates to power supply current, input leakage, output current, functionality at low and high voltages, noise immunity, and any other circuit-oriented static parameters. Such data recording is generally done on a sample basis.

Data recorded on finished digital type circuits consists of circuit static parameters and failure mode in the form of bin information. Here again as in circuit probe, a bin number is assigned to failure categories such as leakage, noise immunity, low-voltage functionality, etc. Measurements relating to linearity, gain, distortion, output level and AGC characteristics are taken on linear type circuits. Applicable transistor or diode type data is also of use in test data analysis.

Quality assurance and product reliability programs require data recorded prior to and after elevated temperature storage, operating life and other mechanical and environmental tests. Static parameters relating to device degradation or failure are recorded along with positive unit and lot identifications.

An important aspect of the data to be collected is its traceability. Unit numbers, wafer number, lot identity, process step, and perhaps experiment number are other items that should accompany test result data.

Reference data also includes information relating to some previous analysis, or to some special output report requirement. For example, data boundary conditions for *windowing* the analysis may be entries into an analysis system. Through this procedure, test results outside certain numerical values, usually caused by some other unrelated failure mechanism, are properly prevented from influencing the analysis. Additional data relates to parameter and device identity; generally, such data is not included in the tester output.

Where is the test data acquired?

Data can be obtained by the direct observation of measuring instruments, and transcribed manually for eventual analysis. However, this is obviously inefficient and prone to error. Computer-controlled test systems are available to perform all kinds of electrical tests, and output the results on some recording medium. The data is then entered into a computer for analysis.

Systems for producing static and dynamic data exist in the Solid State Division (SSD) and the Solid State Technology Center (SSTC). Teradyne J283 test equipment outputs electrical test data onto magnetic tape cartridges; the data format is shown in Fig. 2. Raw data in this form indeed emphasizes the need for further treatment in the way of reduction and analyses. A computer-controlled system for linear, bipolar product testing produces a similarly formatted paper tape output for dynamic parameters. The introduction of test systems producing data on both floppy disc and industry-compatible, 9-channel magnetic tape is underway. Ultimately, a direct communication link between the test system on which data is acquired and the system on which data is analyzed can be of enormous benefit. To some extent this problem is being solved with on-line analysis; this technique utilizes the same

processor that controls the testing to perform the analysis. Unless a foreground-background mode of operation exists, and sufficient core is available, there is a limit to the complexity of on-line analysis. Since the goal of analysis is control, data from many sources, and at time-related (and thereby process-related) intervals must be coordinated and examined. Therefore, the problems connected with data acquisition and sophisticated data analysis, though highly associated, have been treated separately.

In gathering data from computer-controlled test systems, the test programs must be appropriately written. The instructions for selecting the parameters to be logged, or indicating the failure mode (bin), are included in the program, but can also be overridden. Logging can be on a sample or 100 basis. The routine to gather coordinate information for wafer mapping is simply appended to the test program.

How should this data be analyzed?

A prime requirement for performing data analysis is to be able to manage data efficiently. This is best accomplished by the application of a data base whose structure lends itself to the type of test data analysis required. Such an approach must be capable of accepting test data from many different test systems and sources, on a variety of recording media, and must have an easily accessible internal data structure for test-data archiving. Such a system, has been implemented on a PDP-11/20 computer. It was developed to fulfill the following specific tasks:

- Convert the latest data from the testers' output medium to an easier form to manipulate than raw data and add it to a historical file (magnetic tape or disc).
- Allow the user to select various historical entries from the historical file for analysis.
- Permit analysis programs to access selected data and to perform the desired analysis.

The overall structure of the data base is not complicated. There is a header for each unit in a lot or file — followed by the tests in that unit — and, in turn, followed by the unit header for the next unit and so forth.

Headers contain information such as unit number, coordinates for mapping, and

1 MK1 4807FACTCPL07#		1 10-4-72									
1	4800 WIR	2	4800 WIR	3	4800 WIR	4	-15.00 UAR	5	-15.00 UAR		
6	3.07 MA	7	15.00 MA	8	1181. UA	9	1368. UA	10	3.80 MA	11	1368. UA
12	3.80 MA	13	4.18 MA	14	3.80 MA	15	882. UA	16	-16.00 MA	17	4.07 MA
18	20A .60 V	19	20B .60 V	20	20C .60 V	21	20D .90 V	22	21A .60 V	23	21B .50 V
24	21C .60 V	25	21D .90 V	26	21E .50 V	27	21F .50 V	28	21G 1.42 V		

2 MK1 4807FACTCPL07#		1 10-4-72									
1	4800 WIR	2	4800 WIR	3	4800 WIR	4	-15.00 UAR	5	-15.00 UAR		
6	4.52 MA	7	15.00 MA	8	1506. UA	9	1800. UA	10	2.51 MA	11	1800. UA
12	4.98 MA	13	2.00 MA	14	2.51 MA	15	250. UA	16	-14.34 MA	17	3.11 MA
18	20A .60 V	19	20B .60 V	20	20C .60 V	21	20D .50 V	22	21A .60 V	23	21B .54 V
24	21C .60 V	25	21D .50 V	26	21E .54 V	27	21F .54 V	28	21G 1.27 V		

Fig. 2 — Test system data — two units, 28 tests each.

Remote design system for linear IC building blocks

H.R. Beelitz

This paper describes a Remote Design System for linear integrated circuit building blocks. The Remote Design System is defined and specified with its purpose and objective established. A detailed description of the functioning of the system is presented highlighting the actual design process. Economic considerations are discussed with emphasis given to the yield and cost ramifications of pre-engineered library cells.

THE REMOTE DESIGN System is intended to be a growing, evolving set of computer and procedural techniques. As such, consideration is given to those organizations best able to play a leadership role in directing and supporting its growth and development.

Significant attributes of the Remote Design System are:

- a) Exclusive use of pre-engineered, standard circuit library elements.
- b) Emphasis on computer aided design techniques of circuit analysis and simulation.
- c) Standardized cell topology and techniques of placement and interconnection.
- d) Adaptability to evolving terminal equipments.

System definition and description

The Remote Design System for linear bipolar integrated circuits is defined as that total means by which circuit design engineers within remote user organizations have immediate access to a standardized technology. (see Table I).

Time-share computer systems store libraries of standardized linear building block components in both electrical and topological form. Time-share or batch computer programs remotely access these libraries to enable analysis and simulation of proposed linear systems synthesized from these components. Layout and artwork programs assist the designer in achieving rapid and error-free custom circuits. A key feature enables the system to be exercised from user locations, allowing the user to specify and design

custom linear bipolar integrated circuits in his own environment.

Purpose

The purpose of the Remote Design System (RDS) is two-fold:

- 1) Reduce engineering time and cost associated with the development of custom linear bipolar integrated circuits, and
- 2) Provide the user activity the remote access means to a standardized technology.

System objective

The RDS has as its objective the establishment and synthesis of computer and procedural means for permitting circuit engineers at customer locations to fully design custom monolithic circuits. It is expected that the system will draw heavily upon existing analysis and artwork computer programs developed at Design Automation, Solid State Technology Center, Somerville. In addition, hardware systems such as flat-bed plotters and digitizers, (with supporting software) must be available in a supportive service role.

Design Automation plays the key, pivotal role in the RDS. The system must both support existing software and hardware CAD systems as well as lead the development and evolution of advanced techniques. In particular, design automation must support the continuing development of a comprehensive CAD system with:

- Expanded memory capacity and methods for storing libraries of cell topologies and analysis parameters.
- Circuit analysis and simulation programs, both time-share and batch.

Table I — Remote design system.

Definition — That total means by which circuit design engineers within remote user organizations have immediate access to a standardized technology.

Key ideas

- Circuit Design Engineers — not semiconductor specialists
- Remote User — outside the semiconductor manufacturer environment
- Immediate Access — minimal turn around time.
- Standardized technology — calibrated process, characterized library elements.

Purpose of the Remote Design System is:

- Reduce engineering time and cost associated with the development of custom linear bipolar integrated circuits, and
- Provide the user activity the remote access means to a standardized technology.

System objective — The establishment and synthesis of computer and procedural means for permitting circuit designers at customer locations to fully design custom linear monolithic circuits.

- Artwork programs and equipments including digitizers, interactive graphic editors, etc.
- Improved man-machine interface utilizing improved terminals and user-oriented languages, etc.
- Provide the proper balance between the designer's problem solving abilities with the computer's computational and data logging/retrieval capabilities.

How to do it

A capability for remote access and design of integrated circuits is predicated upon the availability of a standardized family of building blocks suitably stored for retrieval and manipulation in remote access computers. Building blocks are stored both in topological form, for placement and interconnection, and in parametric form for circuit analysis and simulation. The basic building blocks may be either individual devices (transistors, resistors), circuit fragments (differential pair, voltage reference source) or complete simple circuits. Regardless of the cell complexity, a given family of building blocks must be self-consistent in relation to a standardized process. It is anticipated that several families of library elements would be developed corresponding to the several basic, standardized bipolar processes now available.

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The actual design process can be visualized as follows: The circuit designer typically selects the actual circuit function to be synthesized, either in response to customer requirements or as a result of his own assessment of industry needs. Tentative specifications are established and a choice of technology made (bipolar, MOS, hybrid, etc.) consistent with both circuit requirements and the state-of-art of the various technologies. Assuming that linear bipolar integrated circuit processing is chosen as most appropriate, then the further choice must be made as to synthesizing the circuit by use of available linear building blocks within the constraints of the RDS, or possibly resorting to a completely custom IC development (see Fig. 1)

Should the designer choose to use the building block approach, he then assumes complete control over the entire IC design. By assuming *all* design functions, the designer maintains control over scheduling, priorities, cost, and engineering trade-offs between circuit function and chip complexity. There are no human communication problems with divisions or organizations outside his own activity.

If, however, the designer decides that circuit goals can best be met with custom design, he must proceed somewhat differently. Typically, he first establishes contact with an IC development or

product group within a semiconductor manufacturing house, and induces them to schedule the development (IC design) of the circuit. Needless to say, conflicts as to schedules, priorities, and engineering trade-offs invariably arise.

From the above, the motivation for using a CAD-building block approach becomes obvious. The *user design engineer*, in choosing the building block approach, can efficiently control and direct the entire design process starting with circuit function selection and specification and culminating in artwork photomask generation.

Considering again the design cycle using building blocks, the designer, with the circuit function identified and the objective specification agreed upon, generates a block schematic for the circuit. The designer has at his disposal:

- Listings of building block elements, characterized both topologically and parametrically.
- User manuals for computer analysis and simulation programs. The user requires authorization and access (user code) to a suitable time-share computer service (RCA NTSS or IBM TSO) maintaining these programs (R-CAP, LECAP, etc.) in common as well as suitable terminal equipment.
- User manuals for artwork programs maintained by design automation, SSTC (PLOTS, DPS system, etc.).
- A selection of packaged building-block library elements suitable for breadboarding.

With the selection and connectivity of library elements established and first verified with either computer analysis programs, breadboarding, or both, the designer proceeds to the actual layout of the circuit. Layout is accomplished in two stages:

- 1) A gross placement and interconnection is sketched, with particular attention paid to pin-out, power supply routing, thermal considerations, chip size, etc. The basic topological problems are first solved,
- 2) The detailed placement and interconnections are laid out either by use of

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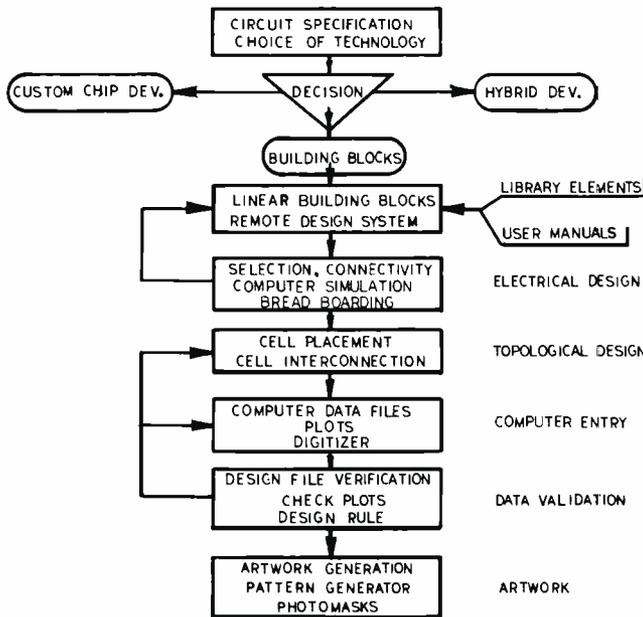


Fig. 1 — Building block approach to IC development.



manual techniques exclusively or with the aid of an interactive CRT graphic system such as the *Applicon*.

With either of these two techniques, cell placement and interconnect routing are accomplished by the designer.

A new third technique could utilize the computer itself to help solve the basic placement and routing problem, using proprietary programs such as the Banning program for MOS LSI. This approach of course, is a final desired objective, but since such programs are in the developmental stage for bipolar applications, the designer must, for the near term, solve the cell placement and routing problem himself.

Let us assume that the designer manually performs the detailed IC layout because of either personal preference, lack of a CRT graphic system, or general suitability for the particular task. He would proceed by using, in general, 500X scale *pasties* or *paper dollies* of the appropriate library elements. The scale replicas would be obtained either from the manual of building blocks or alternatively, could be re-created locally on a time-share terminal fitted with a drum plotter.

With the detailed layout completed, including cell placement and interconnection wiring, the designer proceeds to either create the necessary computer data file himself using artwork programs such as PLOTS, or passes along the layout to design automation for digitizing. Either way, the net consequence is that a computer file is created containing all necessary cell placement and interconnection data. Existing computer design programs would now exercise the data file in conjunction with the stored building-block library elements to synthesize all the detailed patterns which constitute the chip layout.

With the entire chip layout now residing in computer files, in design file language, the designer proceeds to layout verification. A number of procedures are available to him. First, he can obtain a preliminary verification by viewing on his terminal plotter or graphic display several key mask levels such as metal and isolation. In this way, the designer detects gross errors in layout as soon as possible. Satisfied that there are no gross errors, the layout can be further computer-checked for design-rule violations.

Finding none, or correcting those found, the designer instructs design automation to generate one or more large scale (500X typical) hard copy check plots on a flat bed plotter. Such check-plot patterns, with all required levels called out, provide the final visual verification of the detailed structure exactly as it will appear on the photomask set (except for tone and geometry). The patterns also provide the documentation drawings required for user records and for proper interface with the manufacturer.

Upon completion of layout verification, the designer releases the IC data files to the batch-run computer artwork program to generate magnetic tape for the automatic pattern generator. Examples of automatic pattern generators are the D.W. Mann automatic reticle generator and the Gerber large-bed plotters. Either system can be used although the D.W. Mann equipment produces the scale reticle directly, without need for photoreduction.

Standard elements

A centrally stored library computer file of standardized building-block elements or cells forms the back-bone of the remote design system. One very important reason for this is the limited speed of data transmission of the remote access system utilizing the switched telephone line system. Hence, there is a strong practical motivation for limiting data transmissions to the minimum required for completely specifying a chip design. With the building-block approach, only the minimal data required for placement and connectivity of the cells is transmitted. In general, the inner details of cells are not called out for remote transmission to or from *user* locations.

A second important justification for the use of building-block cells is the general lack of an in-depth familiarity with the current practice of semiconductor design technology. Indeed, system circuit designers should not have to be semiconductor design specialists as well (see Table II).

Partially, to overcome these limitations, the concept of pre-engineered, library-element, building-blocks has been developed. Thus, the actual design of all active elements comprising the integrated circuit will *not* be done by the *user*! All active elements will be designed by the

semiconductor manufacturer in accordance with his rules to ensure design integrity, manufacturability and suitably stored in central computer files for remote access.

The two principal forms in which the library elements will be stored are electrical and topological. The electrical form will comprise listings of device parameters, parameter distributions, etc. suitable for computer circuit analysis and simulation. The topological form will include geometries of all levels required for photomask generation programs and will not be transmitted remotely. Only a sub-set of levels, usually a cell outline (for

Table II — Standard elements: their advantages and disadvantages.

Rule for standard elements — All active elements will be designed by the semiconductor manufacturer in accordance with his rules to insure design integrity and manufacturability.

Computer storage: standard elements

Electrical

- a) Device parameter lists
- b) Parameter distributions

Topological

- a) Geometries of all levels required for Photomasks generation
- b) Sub-set only available for remote user access

Advantages of standard elements

- All library elements are pre-engineered by the manufacturer; pre-constructed, tested and verified.
- Manufacturer warranted as to performance, parameter distribution and yield.
- User circuit designer need not be proficient in solid state physics, manufacturing processes, device modeling, etc. The design process is returned to the circuit designer.
- User functions in traditional design role concentrating on component (cell) selection and interconnection.

Disadvantages of standard elements

- A complete library of building-block elements must be available.
- Remote Design System must be responsive to user requirements for new or modified building-block elements.
- Procedures for the development and adoption of new library elements must be established.
- Manufacturer must fabricate, test and characterize all building-block library elements.
- Manufacturer must parameterize all elements for existing computer models.

placement) and contacts or metal (for interconnection) will be remotely available for user access.

The *advantages* of such pre-engineered, standard elements are:

- a) All library elements are pre-engineered by the manufacturer; preconstructed, tested and verified. All elements are manufacturer warranted as to performance, parameter distribution and yield.
- b) The user circuit designer is not required to be proficient in solid state physics, manufacturing processes, devices modeling, etc. The user functions in his traditional design role concentrating on component (cell) selection and interconnection.

The *disadvantages* are:

- a) For the Remote Design System to be effective, a complete library of building-block elements must be available. It is anticipated that this library will grow and evolve, as new requirements emerge.
- b) It must be responsive to user requirements for new or modified building-block elements. For the element library to grow in a timely and expeditious manner, formal procedures for the development and adoption of new library elements must be established.
- c) The manufacturer must fabricate, test, and characterize all building-block library elements. He must parameterize elements for existing computer models.

Circuit analysis and simulation

Circuit design usually starts with an objective specification for a new or modified circuit. The designer typically derives what he considers to be an appropriate circuit configuration, based on his prior experience or research. Initial transistor types and resistor values are loosely specified with the aim of starting an analysis of the trial circuit. The expectation is that device types, resistor values, etc., as well as the probable circuit configuration itself, will be modified as analysis progresses (see Table III).

Analysis is initiated by modeling the device types, both active and passive, consistent with both the computer analysis program to be used and the desired degree of accuracy. With building-block components, a complete parameterization of several models for the several computer analysis programs will be provided. Such analysis programs now include R-CAP, a time share or batch transient analysis program; and

Table III — Circuit analysis, simulation, and layout.

Analysis programs

R-Cap, time-share transient analysis
FASTRAC, time-share entry, batch run
bipolar transient analysis
LECAP, time-share small signal linear analysis

Device simulation models

Ebers-Moll (R-CAP, FASTRAC)
Hybrid-Pi (LECAP)

Parameterization

Hybrid-Pi
S-Parameters

Circuit layout: manual placement and routing — The designer himself solves the placement/routing problem using "dollies" as aids.

Circuit layout: automated placement and routing — The designer utilizes a computer to wholly or in part solve the placement/routing problem.

- Example: Banning System for MOS LSI
- No Design Automation supported computer placement/routing program exists for bipolar IC's.

LECAP, a time share small signal linear analysis program. At present, only R-CAP is supported by design automation, SSTC.

As an adjunct to computer analysis and simulation, packaged building-block library element components will be available for traditional breadboarding purposes. Breadboarding serves as a check or confirmation of computer simulation. It is especially desirable if there is a lack of confidence in the adequacy of the computer modeling for the particular application.

With the circuit configuration established and the device types and values tentatively specified, the designer carries the circuit forward to layout. Layout, including the placement and interconnection of the specified library elements, is done by the circuit designer or a layout specialist. When the trial layout is completed, the designer may re-enter the circuit analysis phase and up-date the analysis to include layout related parameters such as device parasitic capacitances, and tunnel reactances.

It is expected that a variety of types of analysis might be employed. Among these would be: dc sensitivity, dc worst case, dc Monte Carlo, and ac transient, frequency and stability.

Circuit layout

The layout of a complex integrated circuit is comprised of essentially two operations; placement and interconnection. There are a number of techniques available whereby these operations can be accomplished, including those which can be characterized as *manual* and those characterized as *computer-aided*. Computer-aided techniques utilize the computer to wholly or partially solve both the placement and interconnection of library cells. Examples of such software packages are the Banning System for MOS LSI. Currently, no comparable design-automation-supported placement/routing program exists for bipolar IC's.

Manual techniques imply that the designer himself solves the placement/routing problem typically using *dollies* as aids. *Dollies* are scale outlines of library cells which the designer moves about on a gridded Mylar or paper field while simultaneously sketching connection paths between cells. The design objective is to minimize the IC chip size consistent with design rules and circuit specifications.

The precise layout techniques depend, in part, on the nature of the cells available and on the technology used. For instance, consider the optimum case with the cells completely pre-designed. The designer performing the layout need only concern himself with two photomask levels: *Isolation*, corresponding to the cell outline and placement; and *Metal*, corresponding to the cell contacts and interconnection. No other levels need be considered and, indeed, would not normally be available to the designer for editing.

If the designer must design certain simple elements, such as resistors, then he must interact on additional mask levels. The designer must thereby have a greater understanding of current IC technology and device design practice.

As a further example, consider the situa-

tion where the designer decides that he needs multi-level metallization to efficiently implement a circuit function. A still greater depth of understanding of current semiconductor practice would be required, as it relates to alternate metallization techniques. Obviously, greater flexibility in cell definition and placement is obtained at the expense of additional semiconductor-practice skill requirements on the part of the user circuit designer.

From the above discussions, it is clear that the desired flexibility of design within the context of the RDS must be established at the outset! One of the stipulated purposes of the RDS has been to permit user design engineers, who are not necessarily semiconductor specialists, access to a standardized technology. Strict adherence to this goal would require that all building-block cells be pre-engineered to the fullest extent feasible!

Terminals

The RDS must function with, and not be severely limited by, a broad spectrum of computer peripheral equipments. The system must function with the various terminal equipments available today, and make allowance for the rapid evolutionary growth expected to continue.

Terminal equipments can readily be classified in a hierarchical manner. At the lower end of the spectrum is the simple but basic keyboard terminal of which the Teletype ASR33 is representative. The keyboard terminal permits the necessary access to a time-share computer service allowing circuit analysis and simulation programs to be utilized. Inputting of graphics data is possible using artwork programs such as PLOTS, but no effective output graphics are feasible.

A display-only graphic terminal would be obtained by combining the keyboard terminal with auxiliary graphic output devices and controller. Examples of such devices are a Cal-Comp Drum Plotter, for hard-copy high-resolution graphics, and a Tektronix Storage Oscilloscope with controller, for soft-copy low-resolution graphics.

An interactive graphics terminal, usually with light-pen control, provides considerably more flexibility and control.

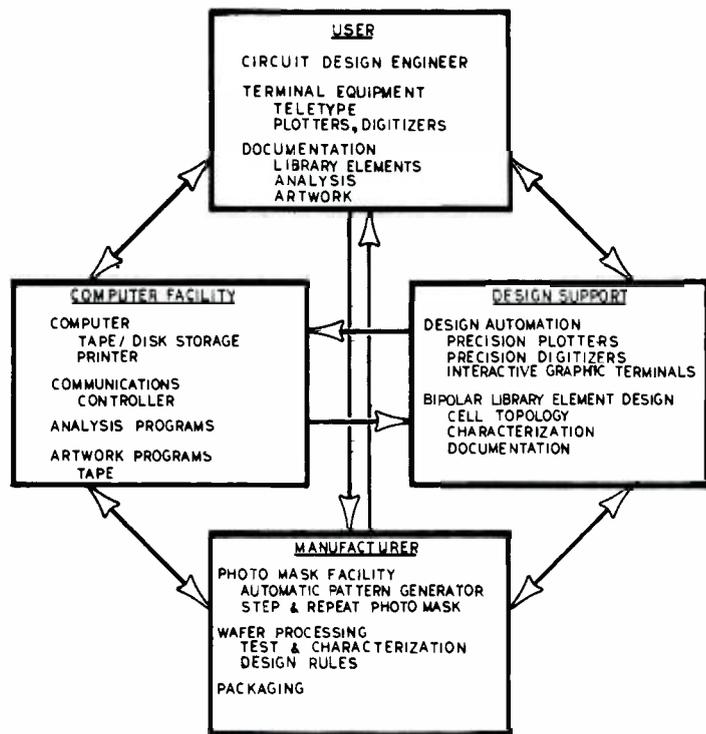


Fig. 2 — Remote design system.

Such terminals are particularly useful for library cell manipulation and interconnection, especially when augmented by a minicomputer.

Of course, considerably more elaborate and powerful computer-aided terminal equipments are being developed and should be considered. However, since the focus here is on an RDS accessible by a circuit design engineer with minimum training in computer-aided design and graphics techniques, equipments of this class are best operated by specialists at the central design automation facility.

Preliminary specification for the remote design system

Standard elements — Families of standardized building-block elements or cells are pre-engineered and warranted by the manufacturer, stored in remote-access computer libraries, and called out without modification (see Fig. 2).

User circuit designers will not design

their own active elements or cells. Possible expectation — the user may find it necessary to tailor resistor values or shapes and so modify existing library elements or create new ones. User modified or created cells are not supported or warranted by the manufacturer without first passing appropriate design review and acceptance procedures. Formal procedures will be established.

Circuit design and analysis — The Remote Design System will provide or bring together the necessary computer analysis and simulation tools for Linear Integrated Circuits. Standard elements or cells will be sufficiently parameterized and modeled by the manufacturer to permit the User ready access to the analysis and simulation programs. Packaged standard element components will be made available for breadboarding.

Circuit layout and topology — The library of standard building-blocks are topologically optimized into a grid-oriented interconnection system. First efforts will be restricted to single-level

aluminum metallization using extended transistor collector regions and resistors for cross-unders. Later efforts will include two-layer, beam-lead metallization. It is to be expected that separate families of cell topologies would be developed corresponding to the separate metallization schemes.

Terminals and communication links — The Remote Design System will permit a broad spectrum of terminal equipments from basic Teletypes to sophisticated interactive graphic terminals. All will interface with both the central computer activity at the RCA Laboratories and with Design Automation, SSTC, over standard switched-line telephone links.

Documentation — Complete listings of all library elements will be made available to interested application groups. Full data describing building block operating characteristics, including circuit analysis parameters, will be provided. Systems manuals describing all the computer programs available and how to access them will be provided. Circuit analysis manuals will be available. These include R-CAP, LECAP, etc. Artwork manuals will be available including PLOTS, DPS system etc.

A placement and interconnect manual will also be available. This guide will describe the design rules and techniques required for manual placement and routing. As automated techniques and programs become available, suitable documentation will be provided.

Economic and commercial considerations

The key concept of the RDS is the placement of all integrated circuit chip design functions, inclusive of cell selection, placement and interconnection, into the hands of the non-semiconductor specialist user. This is done because the user is best qualified to:

- Select the proper trade-offs between electrical performance and design refinements.
- Schedule the part development in relation to his other system requirements.
- Balance the engineering costs of a custom development against the performance achievable with standardized building-blocks.
- Gauge potential quantity of production.

However, assignment of IC design

responsibility to the user circuit designer, while retaining process responsibility with the manufacturer, raises the question of allocation of responsibility for yield between the circuit designer and the manufacturer.

The method of allocation of yield responsibility proposed here is essentially that found workable by semiconductor manufacturers (notably General Electric) who have adopted similar remote design systems.

This method requires the manufacturer to warrant the performance of all library elements. That is, the manufacturer guarantees that the production distribution of cell parameters falls within a specified range. The user would then assume the responsibility for the circuit meeting the required performance standards. The presumption here is that if the library elements perform in accordance with manufacturer standards, it should be considered a design error if the circuit performance falls outside circuit specifications. This is proper because, in fact, it is the circuit designer who has assumed the responsibility for establishing the balance between chip size and complexity, yield, performance, etc.

It should be re-stated here that the Remote Design System restricts the circuit designer to the use of standard elements only. This insures that the library elements meet all manufacturing

Table IV — Systems support for RDS involves a key role to be fulfilled by the Design Automation group.

Design automation must:

- Support existing software and hardware CAD systems, and
- Lead the development and evaluation of advanced techniques.

Design automation must continue to develop a comprehensive CAD system with provisions for:

- Expanded memory capacity and method for storing libraries of cell topologies and analysis parameters.
- Circuit analysis and simulation programs.
- Artwork programs and equipments including digitizers, interactive graphic editors, etc..
- Improved man-machine interface utilizing improved terminals and user-oriented languages, etc., and
- Proper balance between the designer's problem solving abilities with the computer's computational and data logging/retrieval capabilities.

design rules and are producible at high yield. The user is further constrained to manufacturer-designated design rules for interconnections, standard chip shapes and sizes, etc. for the same reasons of manufacturability at predictable yield.

As a consequence of adherence to a policy of fixed design rules, potential yield versus chip area can be predicted. Hence, chip price versus chip size can be established allowing the designer to pre-estimate chip cost for a given design.

System support

The remote design system is planned to be a growing, evolving set of computer and manual techniques supported by terminal and graphics equipments (see Table IV).

It is further expected that the Design Automation group, SSTC, must play a vital role providing leadership in the development and enhancement of analysis and artwork computer programs. Design Automation is the preferred organization to provide the necessary systems support of computer program maintenance and documentation.

New terminal equipments, including so-called *intelligent* terminals, plotting and digitizing systems, etc. are continually being evaluated by Design Automation. Again, Design Automation must provide the leadership and support in providing necessary specialized equipment services and also in specifying and providing guidance in selecting hardware systems to meet specialized user needs.

The development of families of linear bipolar building-blocks would be the primary responsibility of the Bipolar Design group of the Solid State Technology Center. However, since the RDS for linear bipolar integrated circuits is aimed at meeting the quick-turn around needs of user organizations, it is expected that user organizations would participate in the identification and initial specification of the building-block cells.

All building-block cells will be designed, laid-out in standardized modular fashion, stored in suitable computer libraries, fabricated and characterized by the Solid State Technology Center. The SSTC is responsible for full documentation of all SSTC supported library cells.

1975 RCA-MIT Research Review Conference

H.K. Jenny*

Editor's note: This report on the RCA-MIT Seminar held earlier this year represents the author's impressions of the various technical and management presentations given at that time. It is not intended to represent, precisely, the presentation of the speakers, nor can the material be made extensive enough to include all of the technical content. However, the author and the editors have selected those parts which were felt to be meaningful and of interest to our engineers and scientists at RCA. The titles of the summaries and the names of the professors, and their titles, who presented the material are shown for purposes of communication: if RCA engineers wish to communicate with these men, it is hoped that this information will facilitate that need.

AS one of the various services provided by Massachusetts Institute of Technology under the RCA-MIT Industrial Liaison Program (ILP) agreement, MIT earlier this year conducted a special two-day seminar at Cambridge, Mass., for RCA research, engineering, and technical planning personnel. The two-day briefing included oral presen-

tations and question-answer sessions on major areas of research at MIT that were preselected topically by RCA. Also included were three different laboratory tours.

Basically, the topics covered national (and international) problems such as science policies, energy, communications

regulations, lifetime costs of consumer durables; research in areas of RCA's interests and management/organization impact on new product pursuit.

The two-day program was introduced by Prof. Wilbur Davenport, Jr., Head, Dept. of Electrical Engineering and Computer Science. Specifically, the topics discussed at the seminar are as follows:

"Optical Communication"; "Problems of Research Utilization"; "Networks, Digital Communications"; "Acoustic Surface Waves"; "Research with Magnets"; "Amorphous Semiconductors"; "A Mode of University-Industry Interaction"; "Artificial Intelligence and the Future of Productivity Technology"; "Energy"; "Productivity in Servicing Consumer Durables"; "New Policies for Science and Technology"; "Regulation of Communications"; "Career Anchors"; "Perception"; and "Computer Science".

Industrial Liaison Program

MIT administers the ILP through an

National problems

MIT is addressing a variety of national problems. The following questions were covered by the briefing: Are we developing an adequate National Energy Policy? Is our pursuit of commercial products competitive worldwide? How can consumers be supplied the most lifetime cost effective durables? How can more cost effective applied research be obtained with industry-university cooperative effort?

New policies for science and technology

Professor J. H. Holloman, Dir., Center for Policy Alternates, addressed changes in areas, not as explicit as energy and inflation, that have taken place in Research and Development (R&D). From 1955-1967 the United States committed its primary technical resources to space and defense. The rate of growth was so large that the technical reservoir was preempted, inferior talent upgraded, and salaries inflated relative to other professions. As a result of decreasing R&D productivity (rising cost), less R&D was carried out.

Except for Russia, the other countries did not follow the lead of the United States, engineering prices were less inflated, and today Japan and West Germany have 25-50% more scientists engaged in non-military R&D than the United States.

Ability to advance state-of-the-art technology has an enormous impact on military and space programs, but much less on commercial products. Evidence shows most commercial developments to be market-driven (customer need perceived, then technology sought). The character of education is biased in the same direction (science of engineering vs. engineering).

What is happening now? Since 1965, industrial productivity improvement has fallen substantially below past performance.

The U.S. balance of payment is saved by agriculture (food export). We are less than technically capable compared to some other countries which have developed a greater understanding of the consequence of

integrated economic planning. We resist that kind of strategic analysis of our industrial economic complex. However, Europe and Japan have found this planning necessary.

It is predicted that there will be legislation that requires such planning in the U.S. (expected technology in industry). What happens to RCA, the automobile companies, affects the country; how we invest our resources matters to everybody.

Most Europeans and Japanese realize that the problem is not that of R&D, but of the innovation process. How governments can support this process is more important than R&D funding. R&D does not lead to products, it represents only a resource.

Recognition is increasing that social consequences arise from political decisions. Limitations will continue and industry must anticipate social consequences.

Integrated planning must take place in the U.S. and support technology for collective purposes. The security of the U.S. is as dependent on a healthy economy as it is on a strong military machine.

Almost all legislation in the U.S. is reactionary today. We have serious technological problems. The challenge is to learn to treat the cause, not the symptoms.

Further reading:

Holloman, J.H.: "Technical Change and American Enterprise," MIT-ILP Report 139-74, Dec. 1974.

Energy

Professor D. White, Dir., Energy Lab., noted that the Energy Lab was established two years ago as an industry-government-academia coupling. It has a \$3.5 million annual budget and addresses:

- Energy management and economics
- Fossil fuel technology
- Nuclear technology
- Environmental technology

*This article by Hans K. Jenny, Staff Technical Specialist, Engineering Professional Programs, is based on notes taken at the 1975 RCA-MIT Conference.

Industrial Liaison Office, staffed by Industrial Liaison Officers. One of the Officers, Dilip Mathur, is assigned to interface with RCA in rendering the services available under the program. Mr. Mathur maintains direct contact with Doris Hutchison, Administrator, Technical Information Systems, Corporate Engineering, who coordinates the program for RCA Research and Engineering.

For those interested in pursuing certain subjects in more depth with MIT, there is the opportunity to utilize the Industrial Liaison Office to get reports and other additional information or arrange for visits to the pertinent MIT activity. Mr. Dilip Mathur can be reached on A.C. 617-253-2691. Doris Hutchison is in Bldg. 204-2, Cherry Hill, ext. PY 5412.

Summary of Research-Review Seminar

One of the most impressive aspects of a

visit to MIT is the initiative and enthusiasm with which the organization tackles new problem areas and attempts to increase the efficiency of its educational efforts. Among the timely new activities are the Energy Lab, the Center for Policy Alternatives, and the Innovation Center. Several activities are aimed at cooperative technical effort and joint MIT-industry (and where pertinent, government) programs such as the Polymer Research Co-op. Technical problems often face an entire industry. They may involve technical standards, energy saving, or environmental control devices. The costs may be prohibitive for a single firm but by pooling resources the results benefit the entire industry. In this respect some foreign countries are now operating more effectively than the United States.

The purpose of this report is to bring to the attention of RCA technical personnel a cross-section of the efforts of various MIT activities. The material presented here was prepared by the author based on

his notes taken at the RCA-MIT meeting. The material is grouped in a sequence fitting the four general themes shown below in italics:

The focus on our future is represented by *national* (and, to a more limited extent, international) *problems*. In the past, our reactionary process (political and technical) has kept us prominent; however, countries practicing long-range planning and pooling of resources towards commercial objectives are becoming increasingly competitive. Such action is now also required by the United States.

The exploitation of the market needs developed by planning requires effective pursuit of the *innovation process* in which the *technical task* (R&D) is but one of several necessary ingredients. Perception of the market needs as well as *business and organizational* considerations represent other inputs to successful pursuit of innovation.

Electric power technology
End-use technology
Alternate energy technology

Energy management and economics

Under this heading are included econometric modeling, policy development, and technology assessment. For example, a November 1973 position paper by MIT submitted to the government helped stave off gasoline rationing (published in May, 1974 in *Technology Review*).

Presently "Project Independence" is under evaluation with a first draft of MIT comments and recommendations made in March, 1975.

To help the government in policy making, demand forecast and 1980 energy equilibrium conditions were developed as a function of several oil price levels (1980 demand, in equivalent millions of barrels of oil per day of 42.6, should be met by 10.4 oil, 2.2 natural gas liquids, 15.8 natural gas, 8 coal, and 6.2 nuclear).

The recommendation of the study: World and U.S. consumption will decrease with increasing prices. Wait and see what happens now, before bemuddling the situation!

What about synthetic fuels?

Recent estimates show reduced oil resources to 100 - 150 billion barrels. This, if correct, is very worrisome and would require a shift in transportation market fuel.

The cost to liquify or gasify coal (synthesized methane) would be about \$15 per barrel today and \$25 per barrel by 1985. Nothing is foreseeable in the technology that would allow the cost to be cut to half.

It is wrong to put too many eggs into this potentially long-run, expensive, and inefficient method - as the Energy Research and Development Agency policy appears to be doing now. There are better ways of using coal by converting user installations instead of gasifying or liquifying it.

Fossil fuel technology

Fluidized combustion - keeping the combusting particles in suspension

for better mixing and in intimate contact with the heat transfer pipes can improve efficiency substantially.

Electric power technology

Electric power technology should concentrate on working on waste heat management (what should be measured and how to utilize data gained) and reactor safety.

End-use technology

MIT is designing a solar-energized air-conditioning system for the New York City Corp. which will be followed by a 5-year test program evaluating different panels.

References

1. "Energy Self-Sufficiency. An Economic Evaluation." *Technology Review*, May 1974.
2. Dorian and Bupp; "The Breeder Reactor in the U.S." *Technology Review*, Jul. Aug. 1974.

Productivity in servicing consumer durables

R. Lund, Center for Policy Alternatives, noted that the productivity track record of the United States has been poor in the last few years; productivity improvement in the service area is the most sluggish.

Findings

The refrigerator and color television industries provided excellent opportunities to evaluate how the life-cycle costs of two different household products are affected by the various elements of the total servicing system.

The MIT study's findings included the following:

- Servicing costs account for 35% of the total dollars spent on a color television set during its useful life, while the purchase price and electrical power costs account for 53% and 12%, respectively. This means that the owner of a \$400 color TV can expect to spend another

\$400 during its usable life.

- Servicing costs account for only 6% of the refrigerator life-cycle cost, with electrical power cost accounting for the largest portion, 58%, and purchase cost totaling 36%. The owner of a \$300 refrigerator will spend another \$530 over the life of the product.
- Product reliability in both has increased substantially over the last decade, as evidenced by the dramatic decline in the measured need for service in the first year (a 50% decline in the past 14 years for refrigerators, a 50% decline in the past 8 years for color television). However, the cost of such service – labor and parts – has increased so sharply as to offset what would have been a reduced life-cycle cost of each during those periods.
- Inclusive product warranties, covering labor and parts for the first year of the products' lives, were initiated by manufacturers as marketing tools but subsequently have had a decidedly positive influence on design, reliability, and serviceability. Too, warranties have provided new information about the causes for service calls that has increased manufacturers' effort to educate consumers on the use of their products.
- Manufacturers, consumers, and repair services were found to be jointly responsible for increasing the cost of warranty service. Fully 30% of all warranty service calls are unnecessary, requiring only minor set adjustment the owner could have performed. Manufacturers' rules regarding service calls paid under warranty can be misleading and sometimes wrongly place the repair-cost burden on service establishments and consumers. And repair services can abuse the warranty system by fraudulent billing.
- Reduced service costs will be achieved most readily not from a more efficient service industry, as has been proposed, but from greater product reliability. The number of service calls by a repairman has remained at five to seven per day for the past several years and is unlikely to increase significantly. However, the need for service calls is projected to decline by 10% to 15% for color television and 11% for refrigerators in the next seven years, based on the current rate of reliability improvement.
- Manufacturers have not performed as well as they could regarding product reliability, consumer information, and servicing during and beyond the warranty period. For example, products could be designed for greater long-term reliability, product life-cycle cost information could be made available at the point of purchase, and service warranties could be extended beyond the one-year norm.

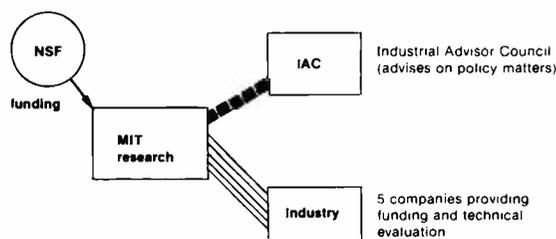
Reference

"Consumer Appliances: The Real Cost." Study by MIT Center for Policy Alternatives.

A mode of university-industry interaction

Professor N. Suh, Department of Mechanical Engineering, in his presentation posed the following questions for consideration:

- 1) Is R&D essential to RCA's future?
- 2) Are there areas where RCA can cooperate with others?
- 3) Is RCA doing enough basic research?
- 4) Does the 10+ year engineer get enough stimuli?
- 5) Are we, as a nation, fully utilizing academic and industrial institutions?
- 6) Should we look for synergistic events?



As an example of the university-industry interaction, Professor Suh

indicated that MIT is presently conducting a cooperative research program in polymer processing. This program, shown in the block diagram, has been underway for over 2 years. A full-day review meeting is held every two months. An MIT staff of 24 (6 faculty, 2 post doctorate, 9 graduate, 7 undergraduates) are on the program. Industry provides \$20K to \$60K per year, depending on the company's size. Publications are delayed for 12 months to give participants a competitive lead.

For its participation industry gets:

- New processes
- New products
- Ideas (complementary because university looks at problems in different way)
- Royalty-free license
- Royalty payment
- Manpower
- Information

The university gets:

- Balanced educational program
- Early exposure of student to industrial problems
- More effective education in creative engineering (analytical techniques, synthesize solutions)
- Better interaction with industry
- New financial resources

The Nation gets:

- Effective use of R&D
- Better technology transfer
- Greater R&D investment
- Greater utilization of R&D investment (less duplication of similar efforts)

Innovation

To better prepare the engineer and scientist for a career of successful innovation, MIT has established a new Innovation Center.

The MIT Innovation Center

MIT, approximately a year-and-a-half ago, set up an innovation center, one of three funded by the National Science Foundation; the other two being at Carnegie Mellon and University of Oregon. The center is an experiment in engineering education and allows interested students of any year and study direction to practice innovation and learn how to start a business.

The whole idea is rather exciting and should produce graduates with much higher awareness of business needs; specifically, what needs to be done to achieve a successful product in addition to the technical task?

The effort at the innovation center is in addition to, not in lieu of, the student's regular study schedule.

The route for the student is as follows:

- 1) He takes courses covering innovation, entrepreneurship, and marketing of new products. Here he learns the role of innovator and/or entrepreneur and generates ideas that may lead to innovation projects.
- 2) The next step is to develop a working model of the idea, study the marketing aspects, and prepare a business plan.
- 3) A student can then either go on independently with his idea or join the innovation co-op and pursue the idea with a number of colleagues. A business plan is proposed and, if accepted by the innovation co-op, funded (\$20 to \$40K NSF funding) for marketing as a new venture or to enter into a license agreement with existing firms.

The MIT innovation center has received a \$5 million 5-year NSF grant. To date, \$400K have been consumed. In another 2 to 3 years, the center is supposed to be self-supporting, living from income derived through licensing.

One of the major assets to this operation is the availability of MIT's vast resources (including the Sloan School of Management).

The innovation center is looking to industry for product ideas and concepts which for some reason or other (lack of funds, interest, fit, etc.) companies are not pursuing. An arrangement will be developed by which industry then receives a compatible share of the income derived from their suggested venture.

Examples of projects

— HVAC Controller (Phil Doubet, inventor): The HVAC controller (heating, ventilating and air conditioning) is a system utilizing state-of-the-art components for use in maintaining and improving the comfort of factory and office workers while at the same time minimizing the costs of power. Both the software and hardware are nearing completion in anticipation of installing the system in a local industrial firm for on-site testing.

Mr. Doubet is in the process of setting up his own company to produce the HVAC. The prototype is presently in pre-installation testing. Cost of the basic unit (including an 8-bit microprocessor) is \$15,000. It is expected to assure at least a 10% saving in heating, ventilating, and air-conditioning energy and pay for itself in less than 8-1/2 years.

— Wideband electronic guitar (Jake Moskowicz, inventor): A line of guitars ranging from a low cost to a superior model has been produced, based upon inventions by a student, which utilize an entirely different pickup system from any now commercially available. The guitars are expressly designed to provide for special effects and duplicating the sounds of other guitars by permitting the separation of signals emanating from individual strings. The new pickup system (separate for each string) gives wider harmonics (as much harmonic distortion as desired with no intermodulation distortion, greater duration of time, individual volume control, etc.).

This project was accepted with reservations; it was thought it would not work, the subject was not suitable, and the innovator not an entrepreneur. Nevertheless, the inventor produced a prototype within two weeks and the project was funded. The inventor works till 4:00 a.m. regularly; plenty of perspiration and prototypes were demonstrated. Guitars are now being evaluated by amateur musicians and by professionals.

— Current limiting device (Steve Cuddles, inventor): The current limiting device is a faculty-student innovation comprising a family of new solid state devices designed to operate non-destructively in limiting current overloads. These solid state devices are a type of FET.

The device utilizes pinch-off current technology of J-FET. It can be used in series or parallel and uses fewer diodes for voltages control. A 10-ampere device will be brought out first. The cost is about \$1/ampere. The market is estimated at \$20 million/year. The business plan is completed, now looking for new facility funding or utilization of an ongoing semiconductor facility.

— Precious metals detection system: Five students and one faculty member have conceived and designed preliminary equipment to detect forgeries in gold bullion.

The objectives for the system are a price under \$500 and a device that is easy to handle for use in every bank. The five students involved have diverse backgrounds and experience. The prototype has been built. Royalty payments of 35% will go to students according to their contributions. Negotiations are underway to set up a company for production of the equipment.

Reference

L. Jenny, H.K.; "The MIT Innovation Center and Aspects of Technical Innovation," report dated March 4, 1975.

Networks, digital communications

Professor R. Gallager, Department of Electrical Engineering and Computer Science, discussed point-to-point data transmission. Enormous progress has occurred in point-to-point data transmission during the last 10 years; transmission data rates have increased from 1200 bits/s to 9600 bits/s over phone lines (4800 bits/s over switched phone lines). Moreover, the decreasing cost of digital logic allows the use of complex modems.

The main problem is now well understood — phase delay represents the major challenge, with carrier shifts and phase distribution, as secondary problems.

Data networks systems represent a much more complex problem that must take into account the rapidly changing cost of the sectors involved. For example, between 1973 and 1983 the following cost factor changes will occur:

- 1) People — twofold increase
- 2) Long transmission — will decrease by factor of 2.
- 3) Short transmission — no change.
- 4) Logic — will decrease by a factor of 20, and
- 5) Memory — will decrease by factor of 50.

The *bursty* nature of messages presents two major problems: 1) the statistical concentration in networks, and 2) the speed mismatch between computer, transmission medium, and people. Presently, the available equipment for polling, concentrating and processing is very inefficient. It appears that packet switching is being chosen as the most expedient network communications process, utilizing a network architecture such as that of ARPA or IBM SNA shown below.

ARPA									
Idle	Start frame 16	Header 64	Message 1100	End frame 12	Error check 24	Idle			
IBM SNA									
Idle	Flag 8	Address 8	Cont 8	Header	Message	Error check 12	Flag	Idle	

However, it is Professor Gallager's opinion that it is too early to fully commit or standardize on packet switching.

MIT is continuing to develop a strategy for minimum protocol information through modeling of receiver pairs, connections, concentrator tasks, etc., and evaluating line versus packet switching.

Reference

L. Gallager, R.; "Basic Limits to Protocol Information In Data Communications Networks," MIT-ILP Report 318-75.

Optical communication

Professor R. Kennedy Department of Electrical Engineering and Computer Science noted the exaggerated claims that followed the invention of the laser, namely that optical communications, with enormous bandwidth capability, uncongested frequency band, and small size would capture the communications market. Research in optical communications is now tackling the most nitty-gritty problems — the influence of second-order effects (spatial and quantum) on system performance.

At first glance, optical communication techniques look very similar to those of microwave communications. However, when signal processing is transferred to the optical system much of the signal may be lost due to the spatial and quantum effects.

Receiver characterization

A comparison of different types of receiver configurations including heterodyne mixer, homodyne mixer, and direct detection shows the following error probabilities:

Research and engineering

MIT carries out research and engineering in many areas; a few of those matching RCA's interests are described below.

Type of operation	Optimal system	Heterodyne	Homodyne	Direct detection
General	n	n/4	n/2	
On-Off	E/nfo	E/4nfo	E/2nfo	E/nfo
Orthogonal	2E/nfo	E/2nfo	E/nfo	
Antipodal	4E/nfo	E/nfo	2E/nfo	1n2

The optimal system consists of a photon detector, counter, local oscillator, and a feedback system.

Channel characterization

The transmission channels encountered include: free space, waveguide, clouds, fog, over the horizon and turbulent atmosphere. While optical communications systems may perform great in good weather, they can become inoperable in bad weather, not so much because of signal absorption, but mainly due to the ensuing forward-scatter properties. The question is: how can systems be made to perform well in bad weather?

MIT has a 9-mile-long test link to study these effects. Tests have shown that 3- to 5-mile visibility, as compared to clear weather, increases forward scatter by an order of magnitude. Also, tests showed that energy level is more important than signal coherence.

Problems of scattering are similar to those of diversity systems. Research is underway on the electro-optic phase plate which attempts to convert the incoming wave to a plane wave at its output.

Acoustic surface waves

E. Stern Group Leader, Lincoln Labs, indicated that acoustic surface wave devices find use in signal processing applications where they can replace very complex multistage filters with relatively simple configurations. Uses range from pulse compression in military systems to strong i.f. filters. Most applications are below 1 GHz, but strong effort is directed at increasing the frequency capability through refined fabrication technology.

Effort on acoustic surface wave development proceeded for several years at Lincoln Labs, and the following presents the Labs' capability.

Typical acoustic wave characteristics include: Wavelength of 10 μm , field intensity 1kV/cm, amplitude 1 to 2 \AA and a peak voltage in wave of 1 V.

Mr. Stern reviewed several filters made:

- A 16-channel filter band (one input, 16 outputs) with sideband suppression of close to 40 dB. 2-MHz channel bandwidth in the 200-MHz range.
- A matched filter for a 1.2-GHz pulse compression radar, with a 10- μs waveform duration, and 500-MHz frequency excursion resulting in a compression gain of 5000. The acoustic wavelength of this filter is 3 μm , the electrode cross-section 0.8 μm , and the depth of the grooves vary between 20 \AA and 300 \AA .

This \$200,000 compression filter replaces seven seven-foot racks of equipment costing \$5 million. To fabricate the finer structures required for the above filter examples, new fabrication technologies have been developed during the past two years. These include:

- Groove depth control using a plasma gun providing a 1% relative accuracy.
- X-ray technology, and
- Electron beam technology, which has achieved 1/2 μm lines with $\pm 0.05 \mu\text{m}$ uniformity. The major disadvantage of the electron beam technology is the required exposure time of about 10 minutes.

Reference

1. Smith, H.L.: "Fabrication Techniques for Surface-Acoustic-wave and Thin-film Optical Devices," MIT-ILP Report 444-75.

Amorphous semiconductors

Professor D. Adler, Department of Electrical Engineering and Com-

puter Science, noted that following the 1968 exaggerated announcement of amorphous semiconductors with its subsequent disillusionment, these devices have slid into relative obscurity. Work is continuing at MIT particularly studying modes of switching (threshold and memory). Typical characteristics of threshold switching provide resistance switching from 10 megohms to 10 ohms with a 1/10 mA holding current at 1V. The amorphous material is very temperature sensitive yielding a 10^6 factor resistance change over a 600°C temperature range.

Studies of the switching mechanism indicate an electronic rather than a thermal process due to its extremely high speed (100 ps).

Among the applications of threshold switching semiconductors explored at MIT are flat screen displays using those devices to switch on electroluminescent cells as well as their use as clock and binary gates.

Memory switching — This type of switching is similar to threshold switching except that if the device is in the on-state a minimum amount of time, it will remain in the on-state even after turn-off. A reset pulse must then be applied to turn it off.

Heterojunctions — The study of more complex structures such as combinations of silicon and chalcogenides have shown unidirectional blocking properties for p-silicon-chalcogenide structures, and bi-directional blocking for n-silicon-chalcogenide structures. Also pn-type transistors have been demonstrated which show memory possibilities due to the pulse operation lock-on phenomena.

The future of amorphous devices is not clear; their major advantages are that they are highly radiation resistant, simple to make (sputter process, no diffusion required), and provide an extra off-state of glass.

Reference

1. Adler, D.: "Fabrication and Operation of an Amorphous-Emitter Transistor," MIT-ILP Report 1221-74.

Research with magnets

Dr. B. Lax, Dir., Francis Bitter National Magnet Lab, observed that the Bitter Laboratory was established in 1965 with National Science Foundation sponsorship. The facility has, as a main power supply, two motor-generator sets with flywheels that furnish 10 megawatts of dc power and 40 megawatts of pulse power.

Magnets built — Several magnets have been designed and built in the research laboratory; the following deserve mention:

- A one-inch bore Bitter solenoid having a 100-kilogauss rating was designed with copper/insulator discs in a helical configuration.
- A large outside magnet, surrounding a Bitter solenoid, provides a 230-kilogauss field and requires full laboratory power-supply capability.
- A hybrid magnet (outside superconducting magnet) 100-kilogauss rating requires less input power. (The Russians have a similar but larger 250-kilogauss magnet.)

Applications in quantum electronics and biomagnetics:

- Quantum electronics — Several applications for magnet research occur in quantum electronics studies; for example, a tunable laser (70 μm to 7 mm) was built for use in spectroscopy, and a tunable laser was built for isotope separation studies by ARPA.
- Biomagnetics — The applications in the field of biomagnetics are more numerous. A shielded room was built for such studies where the earth's magnetic field is reduced by a factor of more than 10^3 . Minute peak magnetic field values as low as 10^{-7} Gauss can be measured in this facility. Listed below are applications.

- Magnetocardiogram: magnetic cardiograms can be obtained wherein damaged hearts show a magnetic field reading in addition to an ac component.
- Encephalogram research: tracings similar to EEG tracings can be obtained.
- Asbestos analyzer: this apparatus analyzes asbestos content in the lung (asbestos contains magnetic particles) and has been developed

for portable use in mines.

- Aneurism treatment: a thin plastic tube with a magnetic tip can be navigated to any spot in the brain (within 5 minutes) to reinforce enlarged vessels.
- Esophagus repair: Some babies are born with broken esophagi. Magnetic cylinders are moved in from both ends toward a rupture and the ruptured ends are brought in line through the influence of a magnetic field; then, the surgeon can sew the fractured ends together.
- Plasma physics: Tokamak-Alcator, the small MIT fusion machine, provides a 100 kilogauss field to contain the plasma. The cleanest, highest current density plasma has been demonstrated, over 1 KeV in temperature (about 6 KeV is required for fusion). Heating of the plasma with a high-power laser is being investigated.
- Magneplane: a model of a magnetically levitated vehicle (having a superconductive magnet in the vehicle and using a linear coil for movement) is operating at the Wayland Raytheon plant. The vehicle has a 300 mi/h potential. The Japanese plan to build such a train in early 1980's to replace their present high-speed system.

Materials for the advanced applications: Several elements are being investigated which promise to produce unusually high-field strengths up to 600 kilogauss. (See chart below.)

Element	Critical field (kG)
NbTi	140
Nb ₃ Sn	240
Nb ₃ Ge	370
PbMo ₈ S ₆	600

Management Organization

The effective pursuit of new products depends heavily on the management/organizational aspects. The questions of how an organization anchors the individual's career and how research results are utilized and transferred effectively are pursued below.

Career anchors

Professor E. Schein, Chairman, Organization Studies Group, Sloan School of Management, explained that career studies are attempts to understand an organization through the lives of its key members. If a better knowledge of individual careers can be achieved, the operation of the company can be better understood.

A study, concerned with technically based careers, covered 44 graduates of the Sloan School of Management as well as a cross-section of the 1951, 1955, and 1959 MIT undergraduate classes. The key question relates to how companies effect change in the individuals in their employ. To evaluate this factor, Professor Schein considers the *internal career* (career anchor) which is a measure of what the individual seeks... and the *external career* which represents what the company and society expect from him. The matching of internal and external careers represents a crucial problem which determines the successful outcome for both the individual and the organization.

Professor Schein found that he could readily classify technical personnel according to the following categories:

- Technical/functional competence
 - Managerial competence (quickly break down problem, see essence, initiate action)
 - Security/stability (the organization man, few takers)
 - Autonomy/independence
 - Creativity
- } Desire freedom from organization

The study monitored the individual's career anchors throughout his career, starting with college graduation. To date, at least 10 years of career experience has been accumulated and the study is continuing. The result to date shows that the organization has had very little or no effect on the individual's career anchors. It is, therefore, of prime importance that the organization properly appraise a candidate's career anchors at the beginning of employment and provide him a supportive environ-

ment (match of external career and anchor) to obtain the most effective performance. An attempt to pull an individual away from his career anchor is shown to be the major cause of job dissatisfaction and turnover.

Reference

1. Schein, E.: "Career Anchors & Career Paths," MIT-ILP Report 707-74.
2. Bailyn and Schein: "A Taxonomy of Technically Based Careers," MIT Report WP754-74, Nov. 1974.

Problems of research utilization

Professor E. Roberts, David Sarnoff Professor of Management, indicated that problems in utilizing the efforts of central research organizations were studied (both technical and management history were researched). The following conclusions were reached concerning the factors facilitating the transfer of information:

1) Project management

- a) Early appointment of project manager (can be a principal scientist).
- b) Early laboratory/management involvement (can be used later for key linkage relationships).
- c) A visible and committed transfer manager who has responsibility to move project out of the lab. This assignment is often ignored and the project falls through the cracks.
- d) Favorable economic analysis (a formal analysis is necessary).
- e) Sufficient patent protection.

2) Movement of project personnel to support interchange and transfer

- a) The receiving unit transfers personnel to the laboratory (3 to 6 months should elapse before move starts).
- b) The labs transfers personnel to receiving unit during move (some danger that transplanted person may be rejected by the receiving organization).

3) Project skill requirements

- a) Researcher is given freedom, but is also coupled with personnel having complementary skills for teamwork and management direction.
- b) A project member is needed who is knowledgeable about applications areas; fifty percent of entrepreneurs pursue their own ideas; success is not dependent on whether ideas are theirs.

4) Strategic planning

- a) Outside pressure on receiving unit is very beneficial.
- b) A project member is needed who is knowledgeable about applications areas; fifty percent of entrepreneurs pursue their own ideas; success is not dependent on whether ideas are theirs.

4) Strategic planning

- a) Outside pressure on receiving unit is very beneficial.
- b) Strategic identification of target market *before* transfer starts (obvious, but often neglected).
- c) Reports and meetings to inform others of project (low-level approach).
- d) The novelty of innovation turns people on.
- e) A courageous, tenacious inventor is needed (if not the case, management intervention must take this over).

In summary, not all of above attributes are required for successful project transfer; but, the more, the better. On the problem of "when to abandon a dead horse," an incentive system encouraging such action should be established.

References

1. Allen, T.J.: "Communications in the Research and Development Laboratory," *Technology Review*, Vol. 70, Oct-Nov. 67.
2. Allen, T.J.: "Communication Networks in R&D Laboratories," *R&D Management*, Vol. (1970) pp. 14-21.
3. Allen and Cooney: "The International Technological Gatekeeper," *Technology Review*, Vol 73, No. 5, March 1971.
4. Roberts, E. and Frohman, A.L.: "Internal Entrepreneurship and Strategy for Growth," MIT ILP Report 1130-72.

AEGIS at sea — successful evaluation exercises

A.J. Whiting

In March of this year, the AEGIS Integrated Fleet Defense System completed nearly a year of intensive shipboard performance demonstrations with a highly successful six-day Navy Preliminary Evaluation Exercise (NAVPREVEX). This latest exercise was designed to assess AEGIS tactical operability and its capability against modern threats, and to prove that the system can be operated and maintained by a Navy crew.

THE montage on these pages, photographed by Andy Whiting of MSRDC, gives a broad panoply of AEGIS deployed at sea in *USS Norton Sound*, showing the wide variety of equipment, operating personnel, and scope of activity. The clear success of Navy/RCA engineering development hardware in meeting all types of threats in an operating environment was a major project milestone for this sophisticated anti-air warfare system. The AEGIS system development is under prime contract to the Missile and Surface Radar Division in Moorestown; related *RCA Engineer* papers include the following:

"The AEGIS Weapon System Acquisition" by W.V. Goodwin (RE-18-1-22)

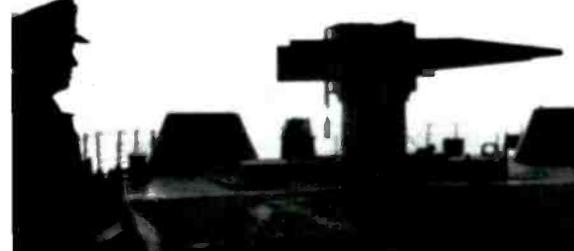
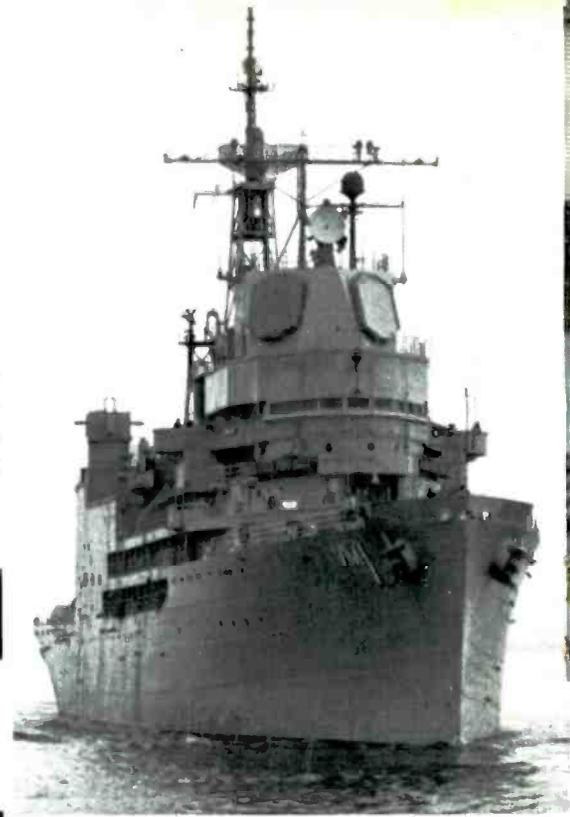
"AEGIS Weapon System Engineering Management Tools" by J.T. Nessmith (RE-18-1-13)

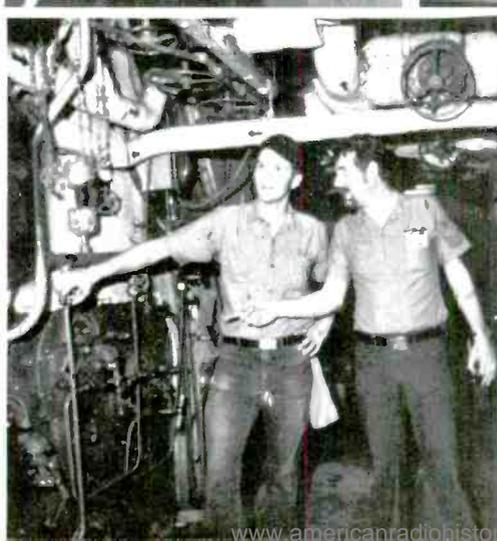
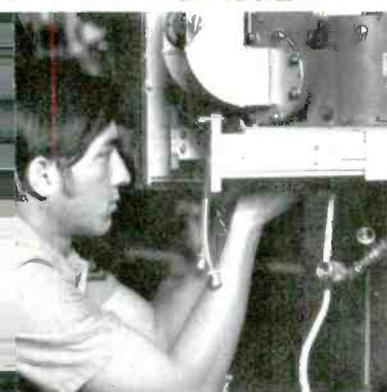
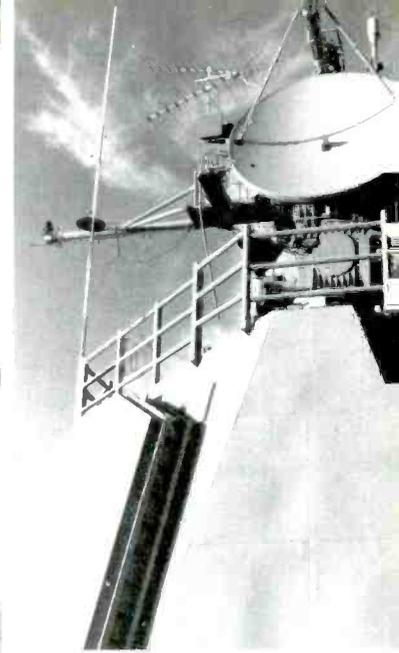
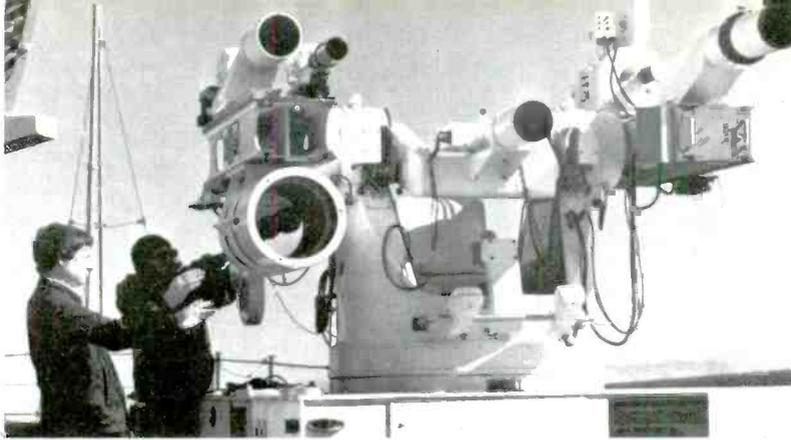
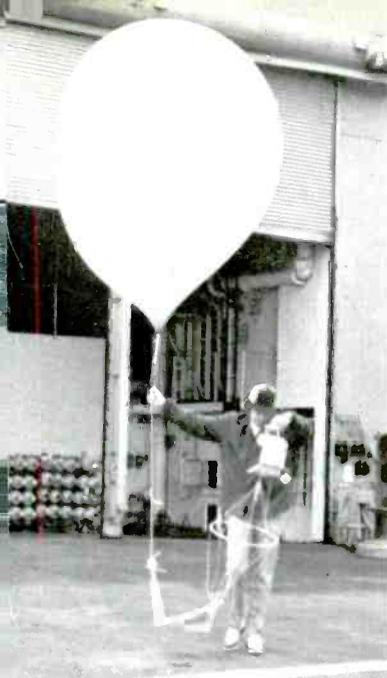
"Computer Control of a Multifunction Radar" by W.W. Weinstock (RE-18-1-5)

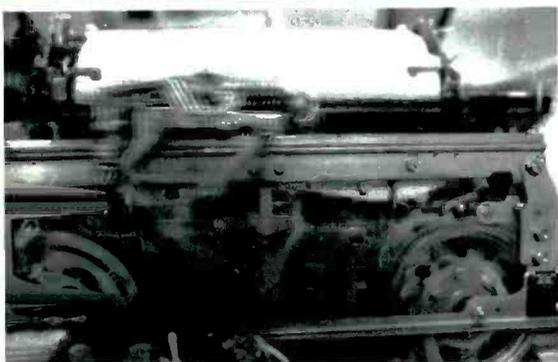
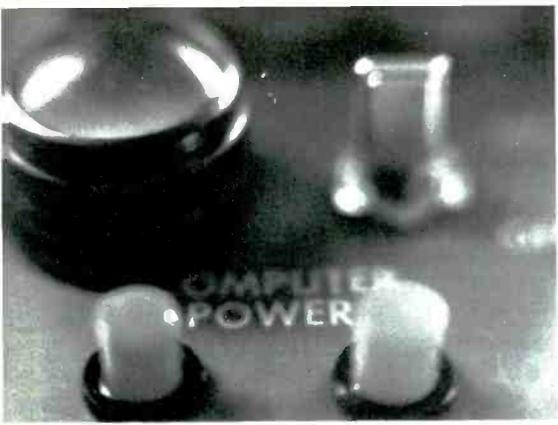
"AEGIS Engineering Model Command and Control System" by F. Bernstein and J. Strip (RE-19-5-20)

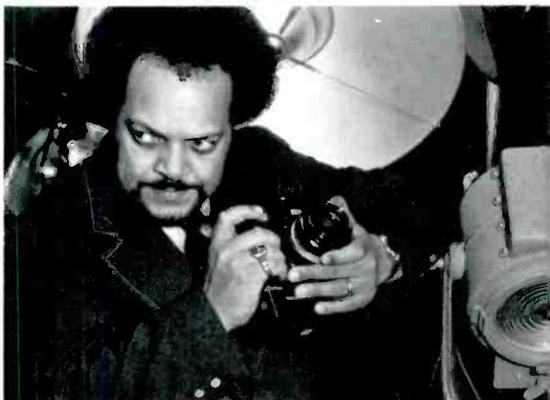
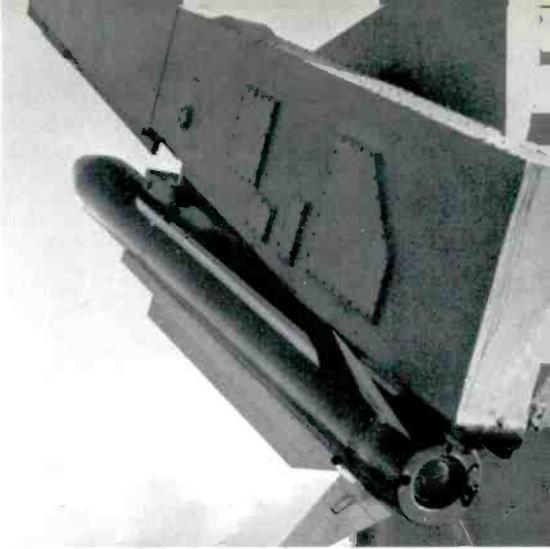
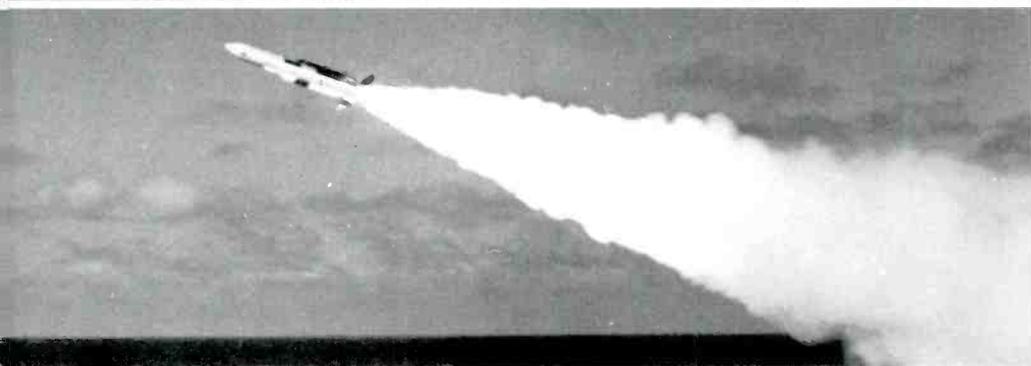
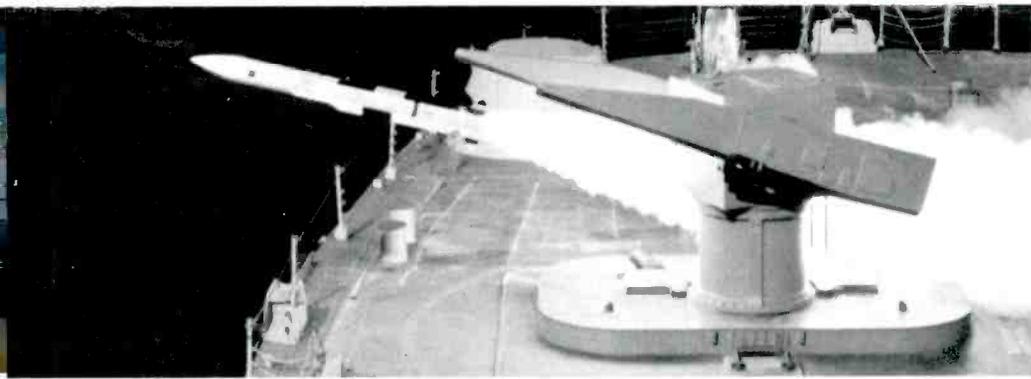
"Computer Program Architectural Design for Weapon System Radar Control" by T.H. Mehling (RE-20-1-14)

"Evaluating Computer Programs for Control of Multifunction Sensors" by S. Batterman (RE-20-6-21)









The success of the Navy's Preliminary Evaluation Exercise can best be described in messages from RADM (then CAPT) Wayne E. Meyer, AEGIS Program Manager, immediately following the exercise:

"The Navy evaluation of AEGIS in *USS Norton Sound* involved 74 manned raids, single and in groups, and in all types of profiles. All were detected and tracked. Six drone presentations were made including low altitude subsonic and supersonic as well as supersonic diving targets. All were engaged successfully including two warshot kills of the TALOS Los Altitude Supersonic Target. Only one maintenance action required contractor assistance. All others were accomplished by the Crew of *USS Norton Sound* while maintaining operational availability during the exercise in excess of 90%."

"This performance is not only a milestone in the AEGIS project, it is a high-water mark in anti-air warfare in the Navy. The professional contribution of every individual in our organization who helped make this achievement possible is most gratefully acknowledged."

Andrew J. Whiting, Ldr., Photographic Services, MSRD, Moorestown, New Jersey went to sea in the *USS Norton Sound* during the six-day NAVPREVEX to record the official exercise events as well as general shipboard activity. He selected the photos on these pages as representative of life at sea with AEGIS. Mr. Whiting is a 1958 graduate of the Hussian School of Art in Philadelphia, where he studied commercial art with emphasis on painting and illustration. He was employed as an illustrator in a number of Delaware Valley graphic specialty firms before joining RCA in 1962 as an artist-illustrator in the Camden plant Art Department. During this time, Mr. Whiting did artwork, page layouts, and design for the *RCA Engineer*. He was transferred to MSRD in 1972, serving in a similar capacity in the Technical Art Services group until his promotion to his present position in October 1974. His background in the creative arts includes more than five years of free-lance photographic work, covering all Society Hill Playhouse productions as well as work with the Jo Anderson Modeling Agency. Mr. Whiting is a member of the Society of Professional Photographers of Delaware Valley.

Reprint RE-21-2-22

Final manuscript received June 4, 1975.

Low-light-level camera used to measure the quantum efficiency of the eye

Dr. R. W. Engstrom

A low-light-level tv camera utilizing a 16-mm intensifier-silicon-intensifier target (I-SIT) camera tube¹, RCA Type 4849, was used to observe a test pattern irradiated with monochromatic light. The same pattern was also observed visually but the irradiation level for the two modes of observation was adjusted until the information content observed was the same. The quantum efficiency of the eye was deduced from a comparison of the two observations assuming that direct visual information is statistically limited by the number of detected photons. The deduction also required the tv camera to operate such that the presentation was limited by the statistics of the numbers of photoelectrons emitted from the photocathode of the image-tube section. This latter requirement was checked by a specially devised reciprocity test.

Dr. Ralph W. Engstrom, Staff Consultant, Electro-Optics and Devices, Lancaster, Pa., completed his undergraduate work at St. Olaf College in 1935 and received the PhD in Physics from Northwestern University in 1939. Since joining RCA in 1941, he has been associated as an engineer, group leader, and engineering manager with various photosensitive devices, including photomultipliers, image tubes, and camera tubes. He has published numerous articles relating to these devices and their applications. At present Dr. Engstrom is a senior engineer serving as a staff consultant. He is a Fellow in the American Physical Society, a member of the Optical Society of America and of Sigma Xi.



DEVELOPMENT of electronic image sensors for very low-light-level operation was primarily a result of military sponsorship for use in reconnaissance and surveillance. As these devices became available commercially, many scientific and medical applications followed such as the intensification of light images in astronomy to take advantage of the higher quantum efficiency of photocathodes relative to photographic plates, the observation of very feeble bioluminescent effects, and the intensification of fluoroscopic X-ray images.

The SIT (silicon intensifier target) tv camera tube is one of the more remarkable of the new low-light-level devices. A diagram of the SIT tube is shown in Fig. 1. Photoelectrons resulting from the light imaged on the photocathode are accelerated through about 10 kV and imaged on a silicon-diode-array target consisting of approximately 750000 p-n junctions in parallel. The high-energy electrons each release more than 1000 hole-electron pairs within the target. This high gain provides sufficient signal so that, for moderately low light levels, the signal from the target exceeds the input amplifier noise. This is not the case in a conventional vidicon or silicon vidicon where the amplifier noise is the limit to low-light-level operation. The low-light-level capability of the SIT tube can be

further increased by coupling an image intensifier tube to the front of the SIT tube. The combination image tube and SIT tube coupled with fiber optics is shown in Fig. 2. This two-element device is referred to as an I-SIT tube and is capable of operation at illumination levels corresponding to starlight where the information is limited by the statistical fluctuation in the number of photoelectrons per picture element.

Dr. A. Rose of RCA Laboratories in Princeton, N.J. has long been interested in the capability of electronic imaging techniques relative to the human eye. He is particularly noted for his early paper² in which he estimated the quantum efficiency of the eye by an analysis of the statistics of perceiving contrast patterns at low light levels. In his book, *Vision: Human and Electronic* (Plenum Press, 1973, p. 37), Rose suggests a unique way of applying low-light-level camera tubes to the measurement of the quantum efficiency of the eye by a direct comparison of information content.

In a dimly lit scene the information reaching the brain is determined by the aperture of the eye and by the corneal quantum efficiency of the eye. For the tv camera tube, the display information is

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Final manuscript received March 14, 1975.

limited by the aperture of the objective lens and by the quantum efficiency of the primary photocathode sensor. It is possible to adjust the aperture of the camera objective lens until the information content in the two cases is the same. A simple proportionality then permits the evaluation of the quantum efficiency of the eye. In the experimental arrangement, however, the relative scene irradiance was varied instead of the lens. This also accomplished an equivalence of information received. Monochromatic radiation was used in the experiment. The equation resulting from the information equivalence is then:

$$\eta_v(\lambda) = \eta_p(\lambda) E_p A_p T / E_v A_v \quad (1)$$

where η is quantum efficiency. The subscript, v , indicates the case of direct vision, p , the photocathode. The terms E_v and E_p are the respective scene irradiances; T is the transmission of the lens for the I-SIT camera; A_v and A_p are the respective aperture areas. The term A_v was taken as the area of both pupils in the visual test, although the question is open as to whether the brain takes statistical advantage of the two channels. The lens for the tv camera and the eyes of the observer were located at essentially the same position relative to the test chart.

Experimental details and test chart

The test arrangement is shown in Fig. 3. A special test chart was fabricated consisting of 5 "white" circular spots and 5 "black" circular spots arranged in a random pattern on a grey background. The size of each of the 5 white and 5 black spots was selected so that the area of each was in a sequence twice that of the next smaller spot. The angular size of the largest circle as seen by the observer was 1° and the smallest $1/4^\circ$. The cluster of circles on the test chart was framed by a black border to provide an orientation reference similar to that of the tv monitor. The reflectivities of the paper were 90.3, 68.15 and 19.3% for the white, grey and black, respectively, at 533 nm, the wavelength of the monochromatic irradiance.

Calibrations

The monochromatic source of irradiance

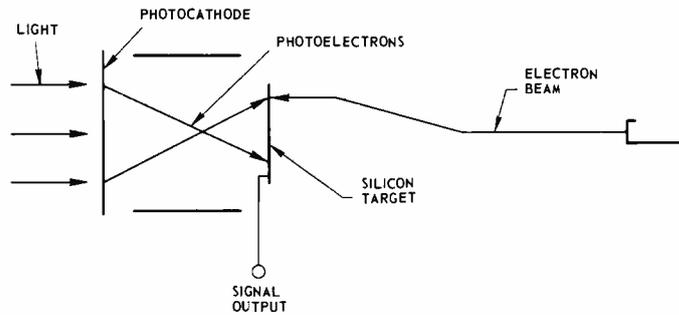


Fig. 1 — The SIT camera tube utilizes a photocathode as the light sensor. Photoelectrons are focussed onto a very thin silicon wafer target upon which a very tightly spaced matrix of p-n junctions has been formed. The spacing of the diodes is of the order of 14 micrometers. The gain mechanism is provided when a primary photoelectron accelerated to perhaps 10 keV energy impinges upon the target and causes multiple dissociation of electron-hole pairs. The holes are collected at the p-side of the diode where the charge is neutralized by the scanning beam. Signal is read out on the backplate of the target.

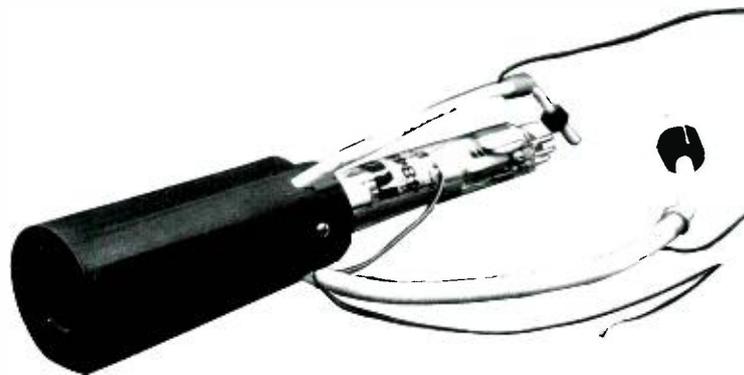


Fig. 2 — The I-SIT tube — an image intensifier tube coupled by means of fiber optics to a SIT camera tube.

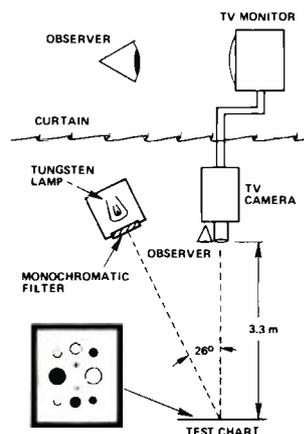


Fig. 3. — Experimental arrangement for the visual and tv comparison tests.

for the test chart was a small tungsten lamp and a spike filter centered at 533 nm. The spectral transmission of this filter was measured with a Cary Model 17 Spectrophotometer and is displayed in Fig. 4 together with the relative luminosity values for scotopic and photopic vision. During the course of the experiment, the scene irradiance was such that the adaption of the eye ranged from scotopic to the luminance level where photopic adaption begins (2×10^{-1} candles m^{-2} , according to Blackwell³). Note, therefore, that the wavelength of the test was such as to provide about 90% or better of the maximum luminosity value regardless of the state of adaption.

The test pattern was oriented normal to the viewing direction; the radiation source was located on a line from the test chart at approximately 26° away from normal to the plane of the chart. The off-axis position was chosen to avoid any possible specular reflections. The irradiation was controlled and monitored with a dc power supply and a current meter. An image tube having a multialkali photocathode (S-20 spectral response) was used as a photometer to measure the 533-nm irradiance in the plane of the test chart as a function of lamp current. Calibration of the photocathode (0.0336 A W^{-1}) at this wavelength was directly traceable to Bureau of Standards data. Fig. 5 is a plot of the scene irradiance so obtained as a function of the lamp current. This chart was used with the measured value of lamp current to interpolate an appropriate value of scene irradiance for the quantum-efficiency comparison.

Transmission of the tv camera zoom lens (F/1.5, 22.5-to 90-mm focal length; Cosmicar, No. 74597) was found to be 55% at the test wavelength of 533 nm.

Responsivity of the first photocathode of the I-SIT camera tube was determined by comparing it with that of the image tube previously calibrated. The value found was 0.0187 A W^{-1} at 533 nm which corresponds to a quantum efficiency at that wavelength of 6.67%.

Finally, in order to make a determination of the quantum efficiency of the eye, it was necessary to determine the area of pupil apertures at the darkened level of

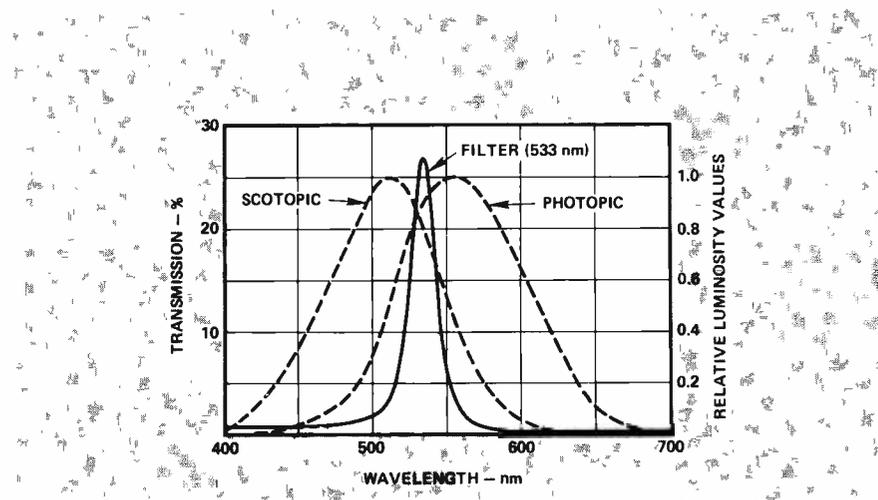


Fig. 4 — Transmission of the narrow pass-band filter used to provide monochromatic scene irradiance. The scotopic and photopic visual characteristics are displayed for comparison.

the perception test. Data on the pupil diameter at various levels of luminance are available in the literature.⁴ There is also evidence that the pupil diameter varies with age.⁵ It was decided, therefore, to measure the pupil diameter directly under the conditions of the actual perception tests.

A three-stage image intensifier tube, RCA-4450, packaged in the form of a night telescope with power supply, lenses, and scale-reticle was used as the measuring instrument. Sufficient infrared sensitivity from the extended-red type multialkali photocathode was available so that an auxiliary infrared source provided an easy means of observing the pupil without affecting dark adaption.

Six individuals were involved in the quantum efficiency tests; their ages varied from 30 to 59. Each individual was exposed to the test scene irradiated with a monochromatic source at 533 nm at a level of approximately $15 \mu\text{W m}^{-2}$. Measurements of pupil diameter were made after intervals of dark adaption of from 3 to 20 minutes. The accuracy of the individual measurement was about 0.5 mm. The data indicated no perceptible change in diameter after 10 minutes; and most of the adaption took place in less than 5 minutes. The last several readings were averaged; diameters for the dark-adapted eyes are given in Table I.

The variation of pupil diameter with the level of scene irradiance was not measured. Instead, the average values as shown in Table I were used and adjusted in proportion to the data by Reeves⁴ for the different levels of scene luminance. The pupil-area variation, reported by Reeves, is of the order of 17% in the luminance range of the present measurements.

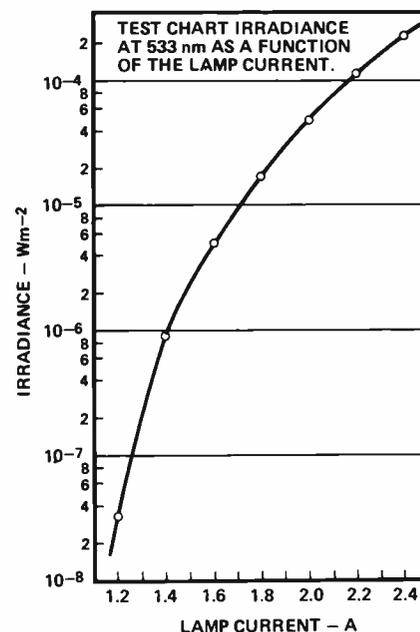


Fig. 5 — Calibration characteristic showing the scene irradiance at 533 nm as a function of the tungsten lamp current.

Perception tests

In the actual quantum efficiency measurements the observer was given a period of 15 minutes to become dark adapted. Generally, the direct visual part of the experiment was begun with the irradiance level low enough so that only one black and no white spots were observed. The irradiance was increased in steps, at each of which the observer studied the chart and, taking advantage of peripheral vision, stated the number of black and white circles observed. When all the black and white circles could be seen, the irradiance was reduced in the same steps and the experimental data taken in reverse. The total elapsed time of the visual experiment was of the order of 10 to 15 minutes.

When the visual test was completed, the same observer viewed the tv monitor being driven by the I-SIT camera. The level of irradiance on the scene was then adjusted until the observer estimated that the information content in the scene was the same as had been observed at each of the steps of irradiance in the direct visual test. In the tv test, the observer was permitted to adjust the level of luminance of the monitor as well as the contrast and it was suggested to him that he might step back from the monitor if he felt it was advantageous. All observers set the luminance level quite low and adjusted the contrast so that the scintillations were not overly prominent. The data was then recorded and the ratio of the irradiance for the monitor test to that for the visual test was calculated. A typical set of data are shown in Table II.

Table I — Pupil diameter of participants in perception test.

Individual	Age	Pupil diameter (mm)
G	30	9.5
R	41	6.1
F	44	6.25
N	47	5.8
V	50	6.0
E	59	6.0

Table II — Typical data showing number of circles observed visually as irradiance level was increased and the ratio of the test-chart irradiances (monitor-to-visual).

Lamp Current	No. of black circles observed		No. of white circles observed		Ratio of test-chart irradiances (Monitor/visual)
	(Increasing current)	(Decreasing current)	(Increasing current)	(Decreasing current)	
1.5A	1	1+	0	0	0.39
1.6	2	2+	0	0	0.22
1.7	2+	3	1	0+	0.16
1.8	3	3+	1	1	0.11
1.9	4	4	2	2	0.09
2.0	4	4	2+	2+	0.10
2.1	5	5	3	4	0.13

Lens aperture = 15 mm
Focal length = 22.5 mm

TV camera limitations

The use of the I-SIT camera as a comparative standard in these experiments assumed that the monitor presentation is limited by the statistical fluctuation of the numbers of photoelectrons from the primary photocathode. Since the current gain of the camera tube from the first photocathode to the second photocathode, by means of the phosphor-fiber-optic sandwich, is about 30, the degradation in signal-to-noise (S/N) is negligible — a factor of $1/(1 + 1/30)^2 = 0.984$, assuming Poissonian statistics. Furthermore, there is no S/N loss in the multiplication process at the silicon target where the gain is of the order of 1000 or more. At very low current levels, however, other factors than photoelectron statistics can limit S/N and, consequently, the resolution capability of the camera. For example, some phosphors show a loss of efficiency⁶ at excitation current densities less than $10^{11} \text{ A cm}^{-2}$. Secondly, for low target currents, amplifier noise may be a problem.

In order to determine whether photoelectron-statistical behavior was maintained at the lowest irradiance levels of these experiments, a reciprocity test was devised. This test is based on the concept that for a photoelectron-statistical-limited mode, the number of photons entering the lens aperture from a particular test spot should be the determining factor in detection regardless

of the focal length of the lens systems or the size of the image on the first photocathode — provided that the image is not so small as to be significantly limited by the modulation transfer function (MTF) of the tv camera. Therefore, if the focal length of the camera lens is varied by means of its zoom capability while maintaining the same lens aperture diameter, one would expect no change in the detectability of the spot pattern.

Such a reciprocity experiment was run using three levels of irradiance. The data are shown in Table III. Reciprocity was indeed demonstrated over a range of image sizes and irradiance levels as indicated by the equal numbers of black and white spots observed. At the large image magnifications, it was found expedient to observe the monitor at greater distances than those for the short-focal-length cases. Nevertheless, at the largest magnifications, reciprocity very obviously failed, especially at the lower irradiance levels. In the fifth column of Table III, the photocathode irradiance is given corresponding to the particular condition of the radiance of the test-chart background paper. Note that there is a reciprocity failure for photocathode irradiance of $0.028 \mu\text{W m}^{-2}$ or less. Therefore, in the experimental determination of the quantum efficiency of the eye, data for photocathode irradiance of less than $0.028 \mu\text{W m}^{-2}$ were excluded. It was obviously advantageous to conduct the experimental study with the smallest magnification available: focal length of 22.5 mm.

At this magnification, there is some loss in signal amplitude for the case of the smallest spot which subtended $1/4^\circ$. Projected on the photocathode, this spot size corresponds to about 0.1 mm or about 1% of the raster height of 9.6 mm. For the I-SIT Tube Type RCA-4849, the contrast transfer function value at 100 tv lines per picture height is about 90%. It is estimated that the light level would have to be increased about 10% to compensate for the loss in S/N resulting from the effect of the contrast transfer function. Thus, in the highest light levels of the quantum-efficiency test, the values calculated for the eye may be high by about 10%. Since other errors were larger, this effect was not compensated for.

The failure of the reciprocity test at low photocathode-irradiance levels could very well be the result of the interference from the amplifier noise. Measurements and calculations supported this conjecture. With the light off and with dark current being negligible, the amplifier noise was measured using the line-select feature of the system. A bandwidth of 1.25 MHz was selected for the measure-

ment because the lower frequencies result in the most interference with perception of the particular patterns being observed. High-frequency noise could be ignored by the observer simply by backing away from the monitor screen, or by the innate ability of the eye to ignore interference which does not correspond to the spatial frequency of the test object. The peak-to-peak value of the amplifier noise in the 1.25-MHz bandwidth was 0.017 V, corresponding to an rms noise voltage of 2.8 mV. The photocurrent at the first photocathode corresponding to the limiting irradiance level of $0.028 \mu\text{W m}^{-2}$ was 0.096 pA for the total raster area of 1.2 cm^2 . The signal corresponding to this light level was found to be 2.8 mV as measured at the output of the amplifier with the line-select equipment. The expected output photoelectron noise for this level of current in a bandwidth of 1.25 MHz is

$$V_{rms} = R (2 e i B)^{1/2} \quad (2)$$

where R is the transresistance from the first photocathode to the output of the amplifier (equal to $0.0028/0.096 \times 10^{-12}$ or 2.9×10^{10} ohm.); e is the electron

charge; i is the first photocathode current; and B is the bandwidth. Thus, V_{rms} is equal to 5.7 mV. If this photoelectron noise component is added in quadrature to the amplifier noise component, the result is 6.4 mV. It seems reasonable that the corresponding loss in S/N would just be detectable as the experimental evidence of Table III seems to indicate. It should be noted, however, that it is not known whether the degradation of perception can really be determined by adding the two types of noise in quadrature because of the different visual character of the two noise components on the tv monitor. The choice of 1.25 MHz for the noise measurement may not have been optimum with respect to perception considerations, but in this relatively low-frequency bandwidth, the ratio of amplifier noise to the photoelectron noise is relatively insensitive to a small variation in bandwidth. It is concluded that amplifier noise is the cause of the lower limit of irradiance in the reciprocity perception test.

Quantum efficiency measurements of the eye

Following the procedures outlined above, tests were made with six individuals. The lens of the tv camera was operated in the 22.5-mm focal-length position. The lower limit of useful test-chart irradiance was determined by the failure of the reciprocity relationship, as discussed above. The upper bound was pretty much determined by the level where the chart became totally visible. Final data are plotted in Fig. 6.

Except for the individual G , the data indicated the corneal quantum efficiency of the eye to be in the range of 1 to 4%. The data for G are something of an anomaly. He normally wears contact lenses. The perception test in his case was repeated with glasses after several hours adaption to the change. The measured transmittance of a contact lens, using a tungsten source through a Wratten No. 58 filter (peaking at 530 nm), was 75%. This transmittance does not explain the low values of quantum efficiency, only some of the difference between the two tests of G .

These results may be compared with other data. S. Hecht⁷, using flashes of light at the absolute threshold of visibility, estimated a corneal quantum efficiency of 7% based on a statistical analysis of

Table III — Data of reciprocity experiment showing range of photocathode irradiance over which spot detection on monitor was independent of spot image size.

F/No	Focal length (mm)	Number of black spots detected on the monitor	Number of white spots detected on the monitor	Photocathode irradiance corresponding to the test-chart background ($\mu\text{W m}^{-2}$)	Reciprocity failure
<i>A. Lamp current = 1.60 A; scene irradiance (533 nm) = 5.05 mW m⁻².</i>					
1.5	22.5	5	3	0.207	
2.0	30	5	3	0.116	-
2.8	42	5	3	0.059	
4.0	60	5	2+	0.028	X
<i>B. Lamp current = 1.50 A; scene irradiance (533 nm) = 2.35 $\mu\text{W m}^{-2}$.</i>					
1.5	22.5	4+	1+	0.096	
2.0	30	4+	1+	0.054	-
2.8	42	4	0+	0.027	X
4.0	60	3	0	0.013	X
<i>C. Lamp current = 1.40 A; scene irradiance (533 nm) = 0.90 $\mu\text{W m}^{-2}$.</i>					
1.5	22.5	3	0	0.037	-
2.0	30	1+	0	0.021	X
2.8	42	0	0	0.011	X

Lens aperture = 15 mm

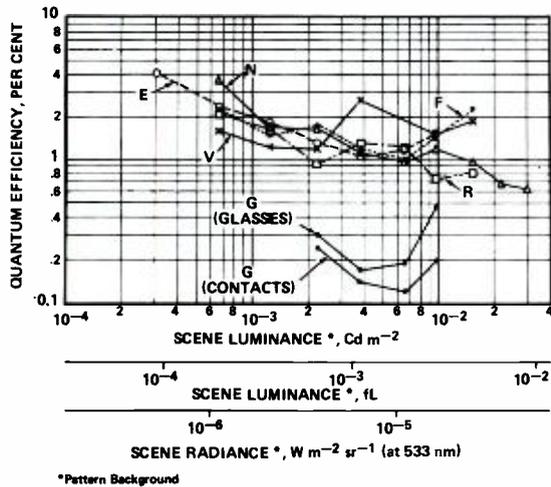


Fig. 6 — Measured quantum efficiency of the eye (corneal) at 533 nm vs. scene luminance.

the probability of detection. A. Rose² deduced the quantum efficiency of the eye from contrast threshold data using statistical theory for the S/N required for detection; his values range from 5% at 3×10^{-6} cd m⁻² to 0.5% at 300 cd m⁻². Recently, A.D. Schnitzler⁸ computed quantum efficiencies that range from 0.2% at 3×10^{-3} cd m⁻² to 6% at 3 cd m⁻² and back to 2% at 300 cd m⁻². In 1973, A. van Meeteren⁹ obtained the quantum efficiency of the eye by measuring the contrast sensitivity as a function of the corneal photon flux and comparing the results with the perception of dot images produced on a kinescope by a flying-spot scanner system, where each dot represented a photon. His values for peripheral vision are approximately 1% over a range from 10^{-4} to 10^{-1} cd m⁻².

Except in the case of observer G, the magnitude of the quantum efficiency of the eye lies between the values reported by Rose and by van Meeteren. The downward trend with increasing luminance supports that observed by Rose, but not the reverse trend reported by Schnitzler or the fairly constant quantum efficiency observed by van Meeteren.

Sources of error and recommendations for further tests

The precision of the measurement is displayed by the irregularities in the individual curves traced in Fig. 6. It is at best about 1 part in 3 and is determined primarily by the uncertainty of defining the condition where an extra spot in the

test chart is seen or not. Since the spot areas varied by 2:1, one might expect the definition of the number of spots to provide only a precision of 1 part in 2. However, because spots of two different contrasts were used, and because the observer attempted to distinguish less than 1 whole spot-size category, the precision was somewhat better.

Some criticism might be directed to the time for adaption taken between the different readings. Any error, however, is not expected to be large since perception readings tracked fairly well in the typical experiment where the light level was first increased step by step and then decreased step by step to the original level.

Finally, one might criticize the tacit assumption of equal time constants for the direct visual test and for the observation of the monitor. It is quite possible that the effective time constant of the eye increases as the light level is decreased. The optimum monitor screen luminance was found to be rather low — but it was substantially greater than that of the scene, especially at the lowest levels. A longer time constant for the eye at the lower light levels would result in too high a quantum efficiency reading at those levels. It would be interesting to investigate tests with light flashes of controlled time duration in order to explore this possibility.

If the perception tests were repeated, it would be useful to provide several test charts with variations in contrast, particularly with rather small contrast distinction to the background. Smaller

ratios of spot areas would aid in the precision of the test. An effort might be made to provide lower amplifier noise, particularly below 1 MHz.

The experiments described in this report were all carried out with monochromatic radiation at 533 nm, near the peak of the eye sensitivity. The tests might be repeated with other wavelengths — for instance, near the short and near the long wavelength thresholds of the eye. The spectral luminosity curves for the eye represent a balance of luminances at the different wavelengths. But equal luminosity does not necessarily imply equal quantum efficiency, even for the scotopic curve.

Acknowledgment

I wish to acknowledge particularly the help of Dr. A. Rose of RCA Laboratories for his initial suggestion of the experiment and for his valuable discussions. Numerous members of the RCA organization at Lancaster, Pa., assisted as subjects and in various other ways. Without the development of the low-light-level tv camera, of course the experiment would not have been possible. It is gratifying that the SIT tube development is finding application not only in the military but also in numerous scientific and medical applications.

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Antenna system of a 12/14-GHz communication satellite

P.Foldes | R. Csongor | R. Whitehouse

The design and development of the antenna subsystems for a 12/14-GHz communication satellite program is described and experimental results are given. Two antenna subsystems are covered: 1) an S-band (2025 to 2300 MHz), circularly polarized nearly omni-directional antenna and belt array for telemetry, tracking, and command; and 2) a pair of shf-band (11.7 to 14.5 GHz), dual-polarized, steerable, high-gain antennas for communication.

THE 12/14-GHz communication satellite project started in 1970 with a study of requirements and basic design concepts. By late 1971, the development phase of the program was initiated, aimed at the complete, detailed design of the spacecraft. The next and final phase—the construction of the flight hardware—is presently being carried out.

The purpose of the program is to develop and try out new technologies and implement communication experiments in the shf band. The spacecraft is planned for synchronous orbit with a 3-axis stabilization system.

The antenna system consists of two unrelated subsystems. One antenna subsystem (TT&C) designed for telemetry,

tracking, and command purposes. This antenna has low gain, but nearly complete spherical coverage in the 2025-to-2300-MHz frequency range. The second antenna subsystem (shf) is designed for the communication experiments, with two 2.5° beams independently steerable within earth coverage and operated in the 11.7- to 14.5-GHz frequency range.

The development phase of the program called for the design and a breadboard model verification of the TT & C antenna. However, work on the shf antenna included the delivery of a final engineering model.

TT&C antenna subsystem

For telemetry, tracking, and command

purposes, two antennas are required. A "belt array" provides coverage in the vicinity of the equatorial plane of the satellite. One advantage of such an array is that it does not interfere with the communication antennas or other equipment placed on the top deck of the satellite. The main use of the belt array is during the transfer-orbit phase, when the satellite is spinning. However, the belt array can be used during operational conditions when the requisition of the spacecraft is necessary.

A "beam antenna" provides coverage in the vicinity of the satellite axis (perpendicular to the top deck). The beam antenna is the main telemetry and command antenna during the operational phase of the satellite.

The belt array and beam antenna together form the TT&C antenna subsystem. The basic requirements for this subsystem are summarized in Table I and Fig. 1.

Table II shows the variation of peak-to-peak ripple amplitude with N at 2025 MHz.

It can be seen that for $N < 28$, the ripple magnitude becomes comparable with the 6-dB total ripple allowance. However, for $N \geq 36$, no worthwhile improvement can be obtained. The criteria for minimum weight require the smallest possible N . The criteria for simplicity of feeding favor

Table I — Basic requirements of the TT&C antenna subsystem.

Command frequency range	2025 to 2120 MHz
Telemetry frequency range	2200 to 2300 MHz
Gain	See Fig. 1
Polarization	RCP
Input reflection coefficient	>20 dB
Power handling	10 W
Antenna location for covering $0^\circ \leq \theta \leq 60^\circ$ angular range	Top deck
Antenna location for covering the $60^\circ \leq \theta \leq 130^\circ$ angular range	16.3 in. below bottom deck with max. antenna diameter of 46 in.
Azimuth (ϕ) coverage	Isotropical
Weight	< 8 lbs.

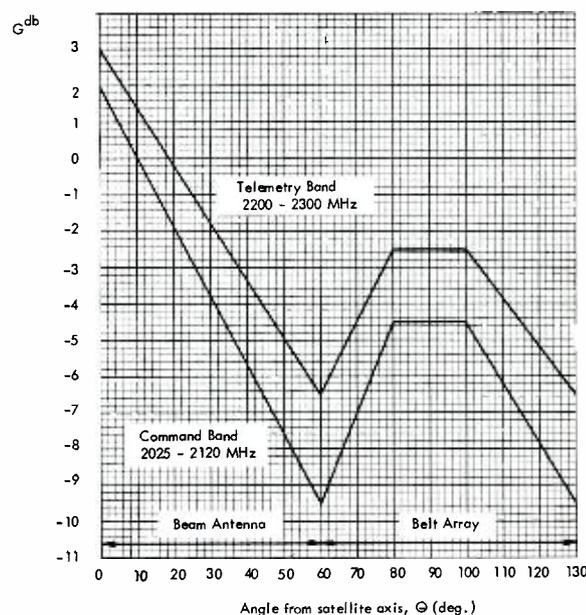


Fig. 1 — TT&C antenna minimum gain requirements (with respect to circularly polarized isotropic radiator).

Table II — Calculated amplitude ripple for an ideal N -element array in the equatorial plane for $D = 46$ in., $f = 2026$ MHz.

N	r (dB)
26	6.91
28	1.91
30	0.17
32	0.13
36	0.06

a number N that is an integer power of 2. Since the only such number in the above range is 32, this was accepted for the number of elements.

After N is fixed, the design problem of an optimum feed circuit is reduced to the distribution of the input power to 32 elements in such a way that the loss, weight, and power-division error in the circuit are minimized. The loss from the

Symbols used

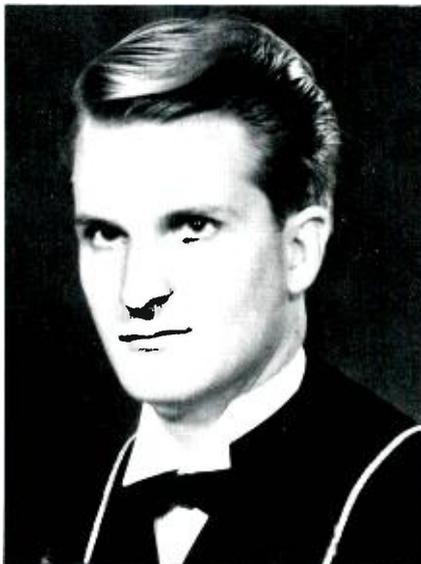
a	circumferential width of a radiating element
a	worst axial ratio within the 3-dB beamwidth and within the frequency range
b	height of an element
CP	circularly polarized
D	diameter of belt array
f	frequency
g	gram
G_t	gain at the edge of the 2.5° beamwidth
G_M	gain on the axis of the beam
l	length of cable to an individual radiating element, normalized to the inner radius of the belt array
L	total length of cables leading to all the individual elements, normalized to the inner radius of the belt array
N	number of radiating elements in the belt array
r	amplitude ripple
R	radius of belt array
RCP	right circularly polarized
TT&C	telemetry, tracking, and command
TWT	traveling wave tube
w	weight per unit length
W	total weight
α	loss per unit length
αw	figure of merit: loss times weight per unit length squared
ΔR	change in the radial position of an individual radiating element
θ	elevation angle (measured from the satellite axis)
θ_c	3dB beamwidth in the elevation plane at the center of the frequency range
θ'	elevation angle for a single element
ϕ	azimuth angle
ϕ	azimuth angle for a single element



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Peter Foldes, Mgr., Antenna Laboratories, Montreal, Que., received the diploma of electrical engineering from the Technical University of Budapest in 1950. He did his Post Graduate work at the Telecommunication Research Institute and Academy of Science in Budapest between 1953 and 1956. In the early part of his career, he was involved in the design of airborne communication radio, radar transmitters and antennas, propagation studies and system design of radar and microwave communication systems at the Army Research Institute and at the Telecommunication Research Institute of Budapest. In 1957, he joined RCA Limited in Montreal, where he became involved in the rf multiplexer, waveguide and antenna system design. During this period, he was pioneering in the use of Cassegrainian antennas for communication systems, which led to a participation of various NASA-JPL programs. Since 1962, he was leading RCA Limited's antenna laboratory and in this capacity, he designed a number of rf optics and feed systems for the Intelsat network. During the same period he designed rf optics and feed systems for various domestic satellite system earth stations. He was also involved in various spacecraft antenna studies and designs. He lectured widely on various international symposiums and gave lectures for several years at the Technical University of Budapest and at the McGill University in Montreal. He published over thirty papers, three books, and has five patents to his credit. He received the 1974 David Sarnoff Award for Outstanding Technical Achievement "for sustained outstanding achievement in antennas for satellite communications."

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Robert C. Whitehouse, RCA Limited, Montreal, Que., received the BSc in Electrical Engineering at the University of British Columbia in 1967. Following graduation he joined the Broadcast Antenna Engineering Group of RCA Limited where he was involved in the design, development and project implementation of television and other antennas, such as a uhf and vhf antenna for the ISIS II Satellite. In 1969 he joined the Aerospace Engineering Group of RCA where he worked on the antennas and the telemetry and command rf systems of the ISIS II Satellite. He also participated in the Communications Technology Satellite (CTS) definition phase. In May 1971 he joined the Antenna Engineering Group. He participated in the design of various Earth Station antennas and was responsible for the rf development of the shf antenna and the initial development of the TT & C antenna of the CTS project.

Since this article was written, Mr. Whitehouse has left RCA to join the Canadian Marconi Co.

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input terminal to an element is essentially characterized by the length of line to ar. element. The total weight is related to the total length of transmission line in the system and the selection of these lines.

Table III shows the length characteristics of the possible layout combinations.

In Table III, l_i is the length of cable to an individual element and L_r is the total

length of the cables. (Both lengths are normalized to the inner radius of the array).

Table III outlines the two basic alternatives: case 1) power dividers can occupy the center region of the spacecraft; case 2) the complete circuit must be at the circumference of the satellite. Since case 2 results in more flexibility, only this alternative was considered. It can be seen from Table III that the optimum layout configuration resulting in near minimum l_i and L_r is utilizing the equivalent of three 2-way power dividers and four 8-way power dividers. (An 8-way divider may consist of a single 2-way and two 4-way dividers.)

For the given frequency band, the practical network elements are either coaxial or striplines. Table IV shows the available characteristics of these elements.

Obviously, loss in a transmission line can be reduced at the expense of increasing weight. To compare the effectiveness of the available elements, a figure of merit can be defined from product of the loss/unit length (α) and weight/unit length (w). As shown in Table IV, the SH50250 coaxial cable has the lowest αw value; thus, it is very attractive for the sections that contain small numbers of connectors or power dividers. This is the case for the input line and the sections after the first and second tiers of two-way power dividers. The weight loss product of the stripline is rather poor. However, this disadvantage is offset by the fact that stripline 2-way power divider junctions are practically weightless. Thus, the selection of stripline is advantageous for line sections containing large numbers of junctions. This is the case for the 8-way power dividers.

On the basis of the above considerations, a coaxial-stripline mixed-feed circuit was selected, resulting in the characteristics shown in Table V.

The layout of the 8-element stripline power divider is illustrated in Fig. 2.

The optimum selection of the radiating element is very important because it influences the vertical pattern, axial ratio, input reflection coefficient, required tolerances, and possible power-division error. A total of ten potentially interesting elements were analyzed during the development phase. Some of the interesting characteristics of these

Table III Characteristic of various power divider schemes.

Variant	Type and No. of power dividers				Total No. of power dividers	l_i	No. of cables L_r		
	1:2	1:4	1:8	1:16			1:32		
Case 1									
1					1	1	2	33	33
2	1				2	3	2	33	33
3	3	4				7	2.69	37	26.98
4	1	10				11	2.29	41	18.45
5	7	8				15	2.68	43	17.56
6	31					31	2.10	51	20.14
Case 2									
1					1	1	3.04	32	97.31
2	1				2	3	3.04	34	50.24
3	3	4				7	3.04	38	28.26
4	1	10				11	3.04	42	22.05
5	7	8				15	3.04	46	18.84
6	31					31	3.04	62	15.70

Table IV — Loss and weight characteristics of various possible transmission lines ($f = 2158$ MHz).

Transmission line	Material	Type	OD (in.)	α (dB/ft.)	w (lb/100 ft.)	w (g/ft.)	αw (dB _v /ft.)
Coaxial line	Copper	UT-85	0.0865	0.244	1.4	6.31	1.52
	Al	UT-141	0.141	0.190	1.9	8.60	1.63
	Copper	UT-141	0.250	0.143	3.2	14.45	2.05
	Copper	UT-250	0.250	0.090	10	45.36	4.07
	Al	SH50250	0.250	0.083	2.93	13.25	1.10
Microstrip, 1/2-in.-wide base	Teflon/copper	1/16 in. thick		0.275	3.31	15	4.13

Table V — Loss and weight characteristics with four 8-element belt-array modules.

Element	length to element (ft.)	loss to element (dB)	total length (ft.)	total weight W(g)
Coaxial line	4.15	0.345	11.5	151
Stripline	1.4	0.385	23.1	348
2-way power dividers (qty. 3)				36
12 connectors				109
Total		0.730		644

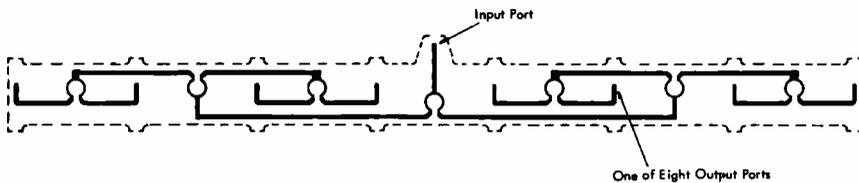


Fig. 2 — Layout of the microstrip 8-way power divider.

Table VI — Some characteristics of various CP radiating elements.

Element	Axial* Length(in.)	Aperture size (in.)	θ , ^o	A (dB)	Note
Dielectric-tube-mounted helix	4.5	1.25 dia.	84	1.8	Selected for the beam antenna.
Circular-cavity-mounted helix	4.0	3.5 dia.	72	3	Largest gain, very long.
Circular-cavity-mounted spiral	2.0	3.5 dia.	76		
Square-cavity-mounted balun-fed turnstile	2.0	3 x 3	90	3	Somewhat complex.
Circular-cavity-mounted parasitic turnstile	1.75	4 dia.			
2.75-in. x 4.5-in. rectangular-cavity-mounted-parasitic turnstile	1.5	2.75 x 4.5	93	2	Simple, compact element.
2.75-in. x 4.5-in. rectangular cavity mounted-parasitic turnstile in tilted configuration.	1.5	2.75 x 4.5	93	6	
2.75-in. x 4.5-in. rectangular cavity with 1-in. extension on spacecraft side.	2.5	2.75 x 4.5	93		
2.75-in. x 4.5-in. rectangular cavity with 1-in. extension and tilted dipoles.	2.5	2.75 x 4.5	96	3	Best element for reduction of satellite interference at expense of increase of length.
3.3-in. x 4.5-in. rectangular-cavity-mounted parasitic turnstile.	1.5	3.3 x 4.5	84	2.9	

*Axial length of an element is defined in the radial direction of the belt array.

elements are summarized in Table VI.

A survey of Table VI shows that most of the listed elements are electrically similar. However, only a few are attractive simultaneously from the point of axial length, aperture size, directivity, axial ratio, and simplicity. On the basis of the detailed electrical and mechanical trade-off study, the crossed dipole backed by a rectangular cavity (parasitic turnstile) fed by an unbalanced line was selected. The geometry of this configuration is shown in Fig. 3. Fig. 4 exhibits the input reflection coefficient; Fig. 5, the azimuth

(a) and elevation (b) patterns.

The principle of operation for this element is simple. The length of the crossed dipoles are selected in such a way that one is above, the other is below resonance so that the phase of the currents are 90° relative to each other on the two orthogonal crossed dipoles. To make such a pair of crossed dipoles unidirectional, a ground plate at approximately a quarter wavelength from the plane of dipoles is required. If this ground plate is extended into a rec-

tangular cavity, then the walls of the cavity can be used to support the dielectric board on which the crossed dipoles are printed, and the a and b dimensions of the cavity as well as the orientation of the crossed dipoles relative to the cavity can be used to optimize axial ratio and input reflection coefficient. When this optimization is done properly, the total radiation from the element is coming from a "dipole mode" and from a "cavity mode" in such a manner that the directivity of the composite system is larger than that of the component modes.

Once the directivity of the element and the internal loss in the system are selected, the manufacturing tolerances and thermal design can be chosen in such a way that the allowable ripple in the radiation field is not exceeded. Table VII shows the selected tolerance budget, which is compatible with this requirement. The tolerance budget is based on the effect of amplitude and phase tolerances as shown in Table VIII and on the temperature distribution calculated for the nonspinning satellite as shown in Table IX.

Measured array characteristics

Table VIII gives the peak-to-peak field variations relative to the average field in the azimuth plane in the presence of manufacturing tolerances and thermal distortions. Actually, the ripples are larger because of the presence of the asymmetrical satellite in the vicinity of the array. The array must operate approximately 16.3 in. below the bottom deck of the satellite, which acts as an odd-shaped ground plate on which various scattering objects are mounted. The presence of the satellite primarily causes a ripple in the elevation plane. However, secondary effects (projecting tube for the shf TWT, corners of the satellite, apogee motor supporting struts, nonparallelness of array and satellite bottom plane make the elevation and azimuth patterns non-separable. Under these circumstances, deep elevation-plane ripples have an influence on the azimuth-plane ripples.

The satellite interaction was studied on a full-size dummy model of the spacecraft on which the array was mounted (see Fig. 6). Fig. 7 indicates a typical equatorial plane pattern, while Fig. 8 shows an elevation pattern for an integrated configuration. During the development phase, a large number of patterns was recorded for various array locations and

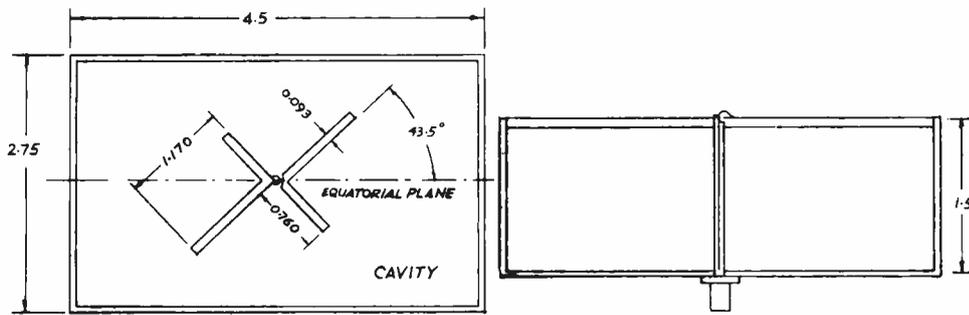


Fig. 3 — Geometry of the parasitic turnstile radiating element backed by a rectangular cavity.

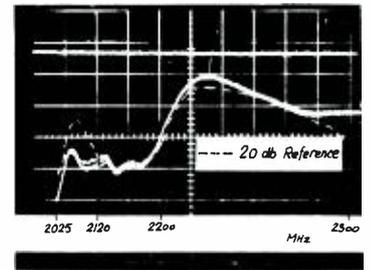


Fig. 4 — Input reflection coefficient of the rectangular-cavity-backed parasitic turnstile in the belt array.

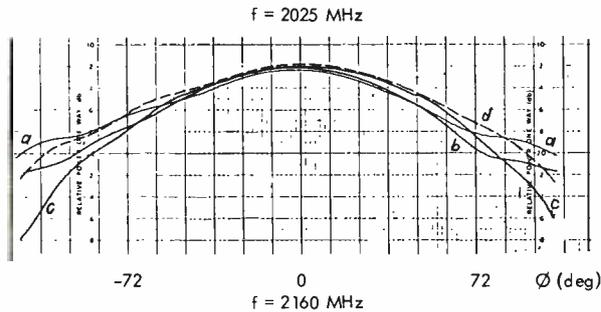


Fig. 5a — Azimuth pattern of the rectangular-cavity-backed parasitic turnstile radiating element: (a) 0° (vertical), (b) 45°, (c) 90° (horizontal), (d) 135° component.

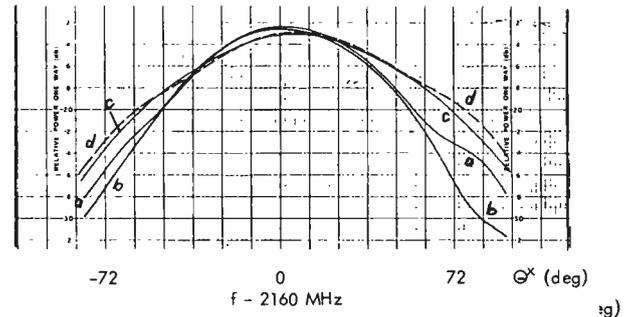


Fig. 5b — Elevation pattern of the rectangular-cavity-backed parasitic turnstile radiating element: (a) 0° (vertical), (b) 45° (c) 90° (horizontal), (d) 135° component.

Table VII — Peak-to-peak ripple components caused by inherent fabrication tolerances and thermal effects.

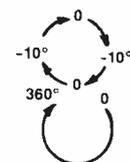
Reason for Ripple	Tol. (%)	Phase error (°)	Ripple (dB)
Finite number of radiating elements			0.13
Manufacturing tolerance of support ring (ellipticity)	60	4.2	0.15
Ellipticity of support ring due to thermal reasons	22	1.5	0.05
Cavity location	±14	±1	0.26
Cavity-bottom-to-element distance	±8	±0.6	0.13
Location of element relative to center of cavity	±8	±0.6	0.13
Reproducibility of dipole junction	±3		0.25
Stripline power dividers (3 in series 0.05 dB ampl. error at each)			0.20
Stripline length (input to output)	±20	±1.5	0.40
Stripline width	±1		0.15
Input connector to stripline			0.10
Connector on short cables			0.10
2-way power dividers (2 in. series)		±1	0.58
Coaxial cable length	±14		0.26
Total			2.89

Table VIII — Calculated azimuth-pattern ripple for various amplitude and phase errors.

θ°	Error		Ripple
	Ampl. (dB)	Phase (°)	(dB) p p
90	0	10 progr.	0.36
90	±0.5	± 5	2.67
90	±0.75	± 7.5	3.93
90	±1.0	0	5.84
90	±1.0	10 progr.	5.86
90	±1.0	±10	5.2
90	0	±10	2.6
90	0	0	0.13
90	±0.75	±15	5.13
90	0	±20	5.46
90	0	360 progr.	0.21
90	±0.75	±7.5 +10 progr.	4
90	+0.75	+7.5 +360 progr.	4
130	±0.75	±7.5	3.83
130	±0.75	±7.5 +10 progr.	3.84
130	±0.75	±7.5 +360 progr.	3.82

Notes

1) 10° progressive means:



(linearly varying)

2) 360° progressive means:



(linearly varying)



Fig. 6 — Belt array mounted on the full-size satellite mock-up.

surface designs for the bottom of the satellite (bare deck, scatterer covered deck, absorber covered deck).

For each investigated case, a series of patterns was taken for various θ angles and frequencies; from these recordings, field contour maps were assembled showing field-strength-level lines relative to isotropic source or specification. The beam antenna was a 4.5-turn helix mounted on a dielectric tube.

Communication antenna

The requirements for the shf antenna are summarized in Table X. Note that the microwave requirements for the antenna are fairly simple. On the other hand, the relatively narrow beam and small weight requirement poses considerable difficulty on the mechanical design.

Design considerations

The basic concept of the shf antenna was selected to minimize the complexity of the steering system and the associated microwave circuitry. Since the total steering range is only approximately 3 beamwidths ($\pm 7.5^\circ$) and the gain of an antenna at the 3-dB point of the beam is not particularly sensitive to beam steering, it is obvious that the steering require-

ment allows the use of a fixed feed and main reflector with a steerable subreflector or a fixed feed with a steerable main reflector. Both of these configurations have advantage of eliminating flexible waveguides or rotary joints.

Dual-reflector (Cassegrainian) optics have the potential advantage of a possible

shaped-reflector design. This leads to higher gain for medium- or large-gain antennas. However, the presently required relatively small on-axis gain makes such optics very marginal. Indeed, it was verified experimentally that such a system had a similar gain to the focal-point feed for the unscanned beam, but a lower edge gain when the beam was

Table IX — Temperature distribution and associated distortion of the array radius with position of the element.

Arc degree* (ϕ)	T° (Rankine)	$T^{\circ} F$	ΔR (in.)
0*	512	52	0.0
22.5	497	37	-0.005
45	456	-4	-0.0136
67.5	400	-60	-0.0373
90	345	-115	-0.0557
112.5	324	-136	-0.0626
135	315	-145	-0.0657
157.5	312	-148	-0.0667
180	311	-149	-0.0670

* $\phi=0^\circ$ is at the point of highest temperature.

Table X — Basic requirements of the shf antenna subsystem.

Transmit frequency range	11.983 \pm 0.150 GHz
Receive frequency range	14.150 \pm 0.150 GHz
Beam cross-section	2.5 $^\circ$
Beam steerability	Earth coverage
Minimum beam edge gain (transmit)	33.7 dB
Minimum beam edge gain (receive)	33.2 dB
Transmit polarization	Vertical (nominal)
Receive polarization	Horizontal (nominal)
Crosspolarized level	30 dB
Transmit-receive isolation	35 dB
Input reflection coefficient	
transmit	20 dB
receive	20 dB
Antenna mount	x - y
Steering cross-coupling	<0.01% / 1'
Pointing accuracy	$\pm 0.1^\circ$
Qty. of antennas	2
Unit weight	12.5 lb

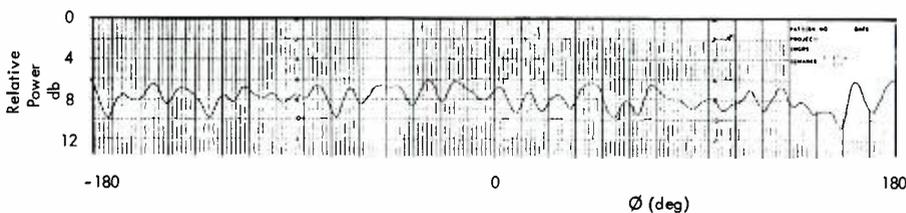


Fig. 7 — Equatorial-plane azimuth pattern ($f=2200$ MHz; elevation angle = 90° , azimuth angle = 0° is at the center of a straight side of the spacecraft).

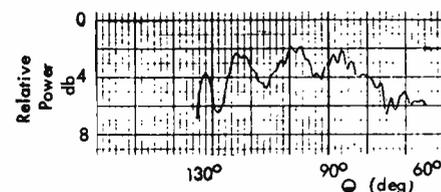


Fig. 8 — Elevation pattern. ($f=2200$ MHz, elevation cut at the center of the straight side of the spacecraft, i.e. at elevation angle = 0°).

steered out to the 3-beamwidth limit by subreflector steering. On the other hand, the edge gain of the focal-point feed system for the same condition was independent of the steering angle and, therefore, resulted in a higher edge gain than the Cassegrainian geometry.

To meet the edge-gain requirement and to provide an optimum optical pointing characteristic, a focal-point-fed paraboloid of 28 in. diameter and 12.45 in. focal distance was selected. It might be pointed out that, in such a system, the main reflector has to be rotated only by approximately 3.8° to achieve the 7.5° beam steering with a fixed feed, because the rotation of a reflector at the same time displaces the feed horn off the axis of the reflector.

Since the transmit and receive polarizations are orthogonal, the feed must contain an orthogonal coupler and a horn, which can optimally illuminate the reflector for both polarizations and frequency bands. Furthermore, either a dual-mode waveguide or two single-mode waveguides must be provided between the orthogonal coupler and horn. The connecting waveguide is shortest for an offset-fed paraboloid design, but such a paraboloid has some inherent limitation on pointing accuracy and, mechanically, is more complicated. On this basis, a symmetrical paraboloid was selected. Such a configuration leaves two possible locations for the orthogonal coupler: 1) close to the focal point, 2) behind the reflector. The first arrangement allows the use of two independent, single-mode waveguides, but it exposes the

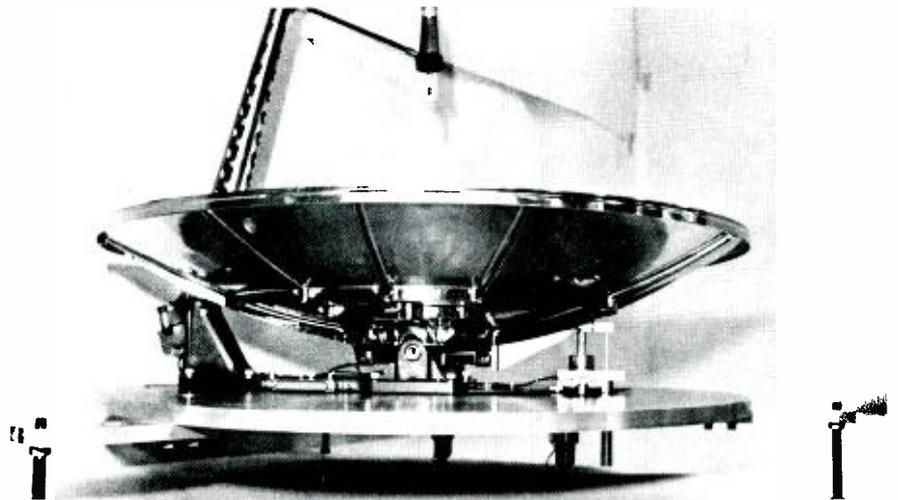


Fig. 9 — Photograph of the shf antenna system.

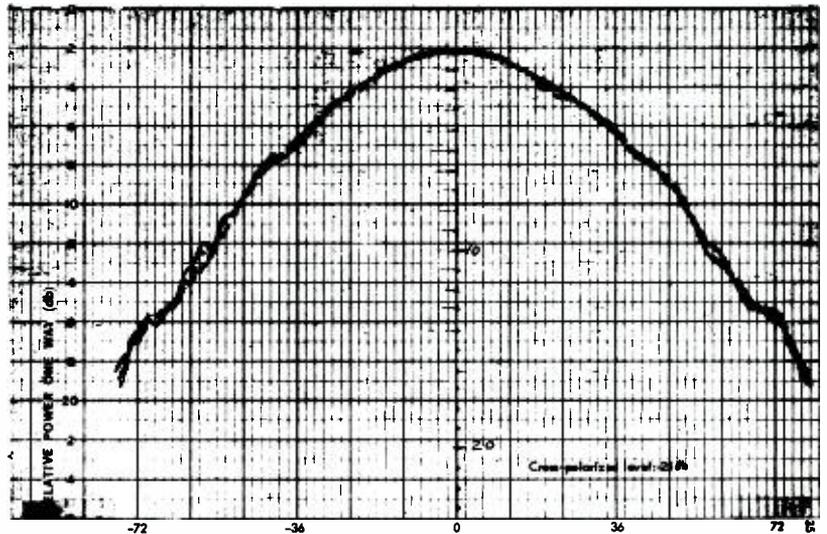


Fig. 10a — Primary patterns of the feed, $f = 11.833$ GHz.

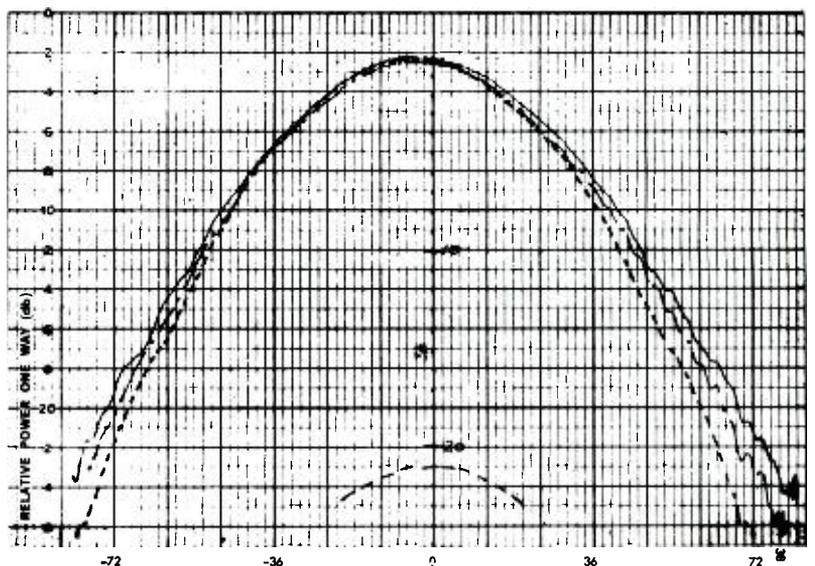


Fig. 10b — Primary pattern of feed, $f = 14.3$ GHz.

Table XI — Weight breakdown of the shf antenna.

	<i>Weight (lbs.)</i>
Antenna	
Reflector	3.00
Baseplate	0.75
Actuator assembly	2.28
Feed	1.28
Skirt	1.80
Cross	0.61
Mounting hardware	0.48
Total	10.2
Electronics package (drives two antennas)	2.6
Electronics interface harness (for two antennas)	1.40

orthocoupler more to the thermal environment of space and it necessitates the support of this relatively heavy unit far away from the top deck of the satellite. The second arrangement is free from the shortcomings of the first, but it requires the use of a dual-mode waveguide. Furthermore, this waveguide must be curved in order that the feed horn directs its radiation toward the reflector.

During the development phase, a detailed study was made to investigate various possible waveguide cross-sections. The end result of this study led to the selection of a circular waveguide cross-section, capable of supporting the wanted orthogonal modes with negligible cross-coupling and resulting in an extremely simple, minimum weight system.

The overall shf antenna consists of a steering electronics unit, antenna mount, reflector, and feed system. The antenna mount contains two linear translators made by Hughes Aircraft Co., identical to the ones employed in the Intelsat IV satellite. The linkage assembly, however, was designed specially for the present antenna. The reflector was made as a single-piece machined unit from a magnesium casting. One of the interesting aspects of the reflector fabrication is the 0.06-in. wall thickness, resulting in 3.1-lb overall weight including its reinforcing ribs. The accuracy of the reflector is ± 0.005 in. rms.

The complete feed system consists of an orthogonal coupler, straight waveguide section, curved waveguide section and conical horn. In one alternative, these parts were made by nickel electroforming in order to obtain close tolerances, low weight, and acceptable thermal distortion characteristics. However, the straight waveguide section and curved waveguide section was also produced from carbon fiber material to reduce weight. Typically, a factor of 2.5 reduction of weight relative to nickel is possible with carbon fiber. The carbon fiber feed had comparable temperature dependency to the nickel feed and slightly higher rf loss. One possible compromise is to use the nickel feed with a carbon fiber deformation restraining element across the curved section of the waveguide.

Fig. 9 shows the antenna system using this configuration. The weight breakdown of this system is summarized in Table XI.

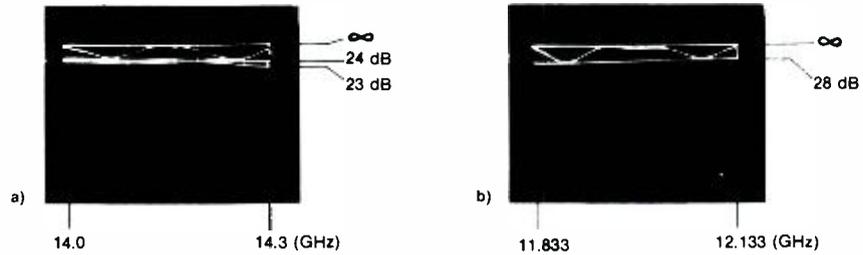


Fig. 11 — Reflection coefficient of the feed: a) Receive frequency range: 14.0 to 14.3 GHz, b) Transmit frequency range: 11.833 to 12.133 GHz.

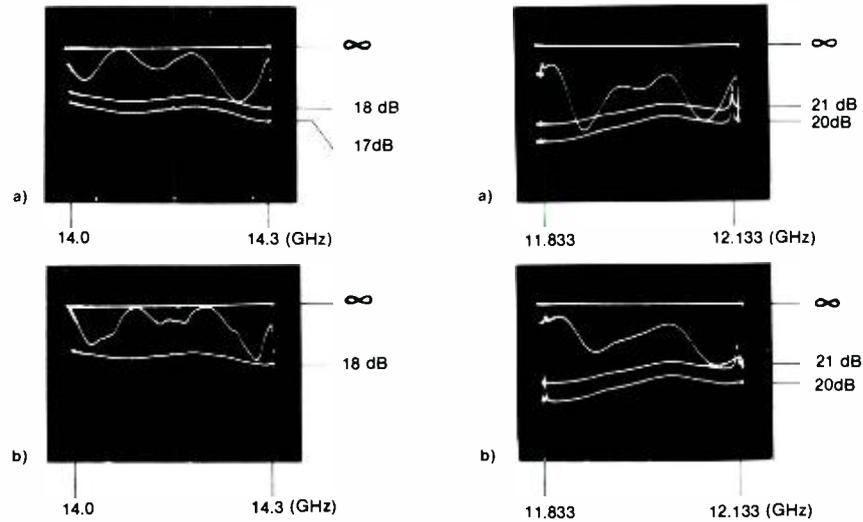


Fig. 12a — Reflection coefficient of the overall antenna system: a) no beam steering, b) 7.5° beam steering. Frequency range: 14.0 to 14.3 GHz (receive band).

Fig. 12b — Reflection coefficient of the overall antenna system: a) no beam steering, b) 7.5° beam steering. Frequency range: 11.833 to 12.133 GHz (transmit band).

Measured characteristics of the shf antenna

The primary patterns of the feed are shown in Fig. 10, while the input reflection coefficient is exhibited in Fig. 11. It can be seen that the crosspolarized power level of the orthocoupler/curved-waveguide/horn system is fairly low. The reflection coefficient of the overall antenna system is exhibited in Fig. 12.

Two techniques were experimentally investigated to compensate for the effect of the reflected power from the reflector back into the horn. The first technique tried was the use of the conventional vertex plate. The vertex plate, however, deteriorated the antenna's gain and sidelobe performance. Furthermore, the resultant impedance match obtained with the vertex plate system was noted to deteriorate when the antenna was optically pointed to a new direction. Thus, the vertex plate method gave rather limited performance for the tradeoff involved. The second technique tried was the use of a short-circuited stub made up of a length of miniature coaxial cable coupled into the waveguide at the input of the orthocoupler. The length of the stub was adjusted to be identical with the electrical length of the path starting from the input

of the waveguide, continuing through the feed, exiting at the horn, and ending at the vertex of the reflector. This method would have the potential advantage of improving the impedance match relatively independently of pointing angle and would also be free of sidelobe deterioration. The gain degradation would be similar since a practical stub would be lossy. The impedance-match improvement obtained, however, was quite small for a match which was already in the order of 23 dB. Greater improvement was noted if the match beforehand was in the range of 18 to 20 dB.

Better improvement might have been obtained with high-directivity coupling devices instead of the simple coupling probe, but this would have led to additional hardware and weight.

It was decided, following the experimental investigation, that the tradeoffs in gain and weight did not justify the small improvement in impedance match. The final design of the antenna, therefore, did not include compensation for the power reflected from the dish back into the horn. The system performance, however, in spite of this additional reflected power, is adequate.

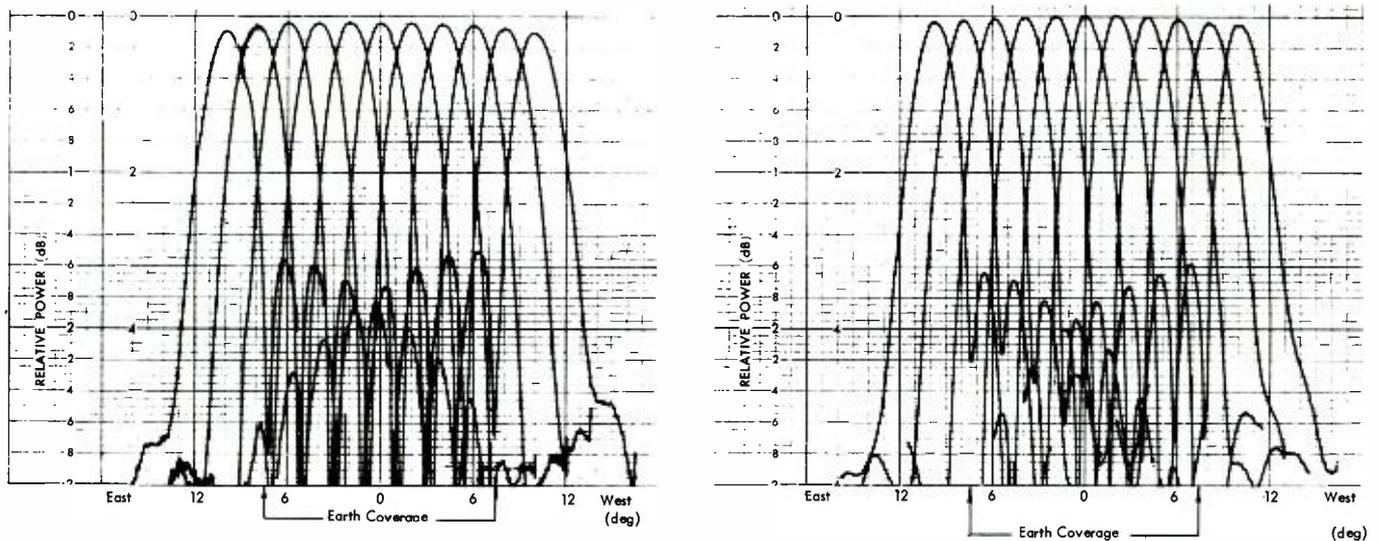


Fig. 13a — Secondary pattern for various steering angles at the transmitting center frequency $f = 11.983$ GHz.

Fig. 13 shows the secondary pattern for various steering angles, while Fig. 14 exhibits the effect of thermal variations on a given beam position.

The measured maximum and edge gain of the antenna are shown in Table XII. The edge gain refers to 2.5° of coverage.

It can be seen from Table XII that the edge gain of the antenna is nearly independent of frequency and steering angle. At the same time, the edge gain is also independent of thermal variations. However, the thermal environment has a small effect on the position of the beam ($\approx \pm 0.04^\circ$) which represents only a portion of the overall pointing error budget.

Conclusion

The design of the antenna system for the project was essentially completed during the development phase of this program. These activities included the complete electrical development for both antennas. In the case of the shf antenna, an electrical engineering model was also delivered.

For the TT&C antenna, the design effort covered the development of a new wide-band, compact circularly polarized radiating element, and the experimental investigation of the effect of the satellite body on the radiation pattern.

For the shf antenna, a novel steering concept was developed and a low cross-polarized level was achieved in spite of the use of a curved, dual-mode circular

Table XII — Measured on-axis gain and edge of the shf antenna

$f(\text{GHz})$	0.0° steering		Maximum steering (7.5°)	
	$G_M(\text{dB})$	$G_E(\text{dB})$	$G_M(\text{dB})$	$G_E(\text{dB})$
11.833	37.2	34	37.1	34
12.133	37.5	34	37.4	34
14.000	38.6	34.3	38.5	34.3
14.300	38.8	34.3	38.7	34.3

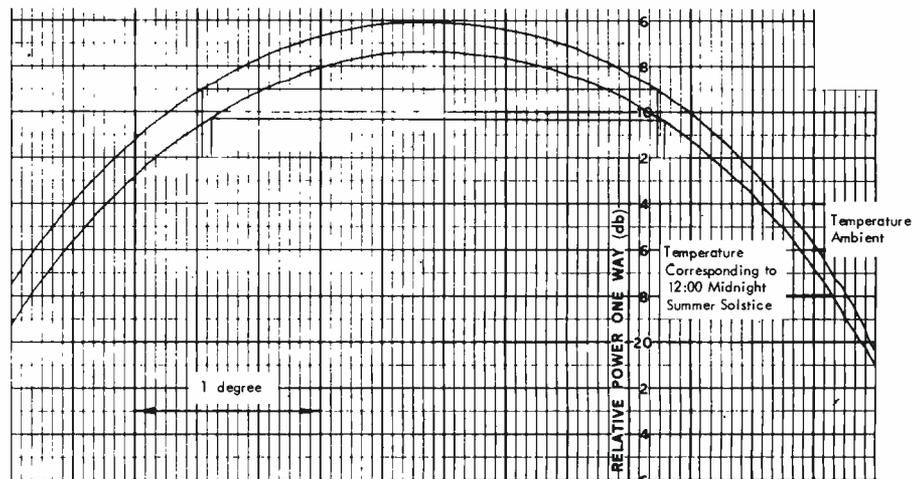


Fig. 14 — Effect of temperature variation on a given beam position in the North-South plane (The patterns are displaced by about 1 dB for clarity of analysis).

waveguide and an asymmetrically fed orthogonal coupler.

Acknowledgment

The authors express their thanks to V.

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Atmosphere Explorer electrical power subsystem

J. Bacher | P. Callen

This paper describes the design, configuration, and operation of the electrical power subsystem aboard Atmosphere Explorer "C" (upon successful orbit, the spacecraft was given the NASA designation, Explorer 51). The subsystem supplies an unregulated voltage, which varies between -26 and -38 V, and a regulated voltage of -24.5V.

THE BASIC DESIGN of the Atmosphere Explorer (AE) electrical power subsystem is similar to that incorporated in flight-proven ITOS and Nimbus spacecraft, but functional redundancy has been expanded in several areas to improve reliability. This involves the battery-charging technique, cut-off of battery-charging current if battery voltages become abnormally high, and disconnection of non-essential electrical loads if battery voltages become abnormally low. Also, redundancy was added to the control circuit for a shunt dissipator, and series redundant pass transistors were incorporated to prevent a single-point failure from loading the solar array. All automatic functions can be overridden by ground control.

The Atmosphere Explorer "C" (AE-C) discussed here is the first of three AE spacecraft to be launched over a two-year period. No significant changes in the power supply are anticipated for the latter two spacecraft (known as AE-D and AE-E). The spacecraft mission is to investigate the photochemical process and energy transfer mechanisms accompanying the absorption of solar ultraviolet radiation in the earth's atmosphere. Measurements will be made in the largely unexplored low-altitude region between 120 and 300 km, but properties of the region above 300 km will also be investigated. AE-C was launched on December 13, 1973 and has been in successful operation for more than a year.

Electrical power requirements

The AE power subsystem provides all electrical power to the spacecraft loads and has a design lifetime of one year. The basic power subsystem requirements are 1) to generate the required voltages, 2) to control battery charging, 3) to provide regulation of the solar-array voltage, and 4) to provide control of the spacecraft heaters and automatic temperature con-

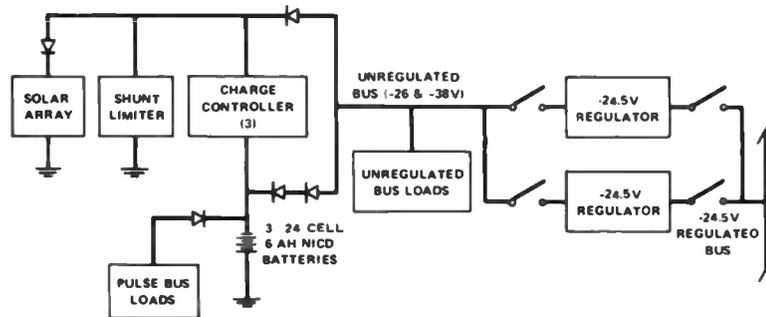
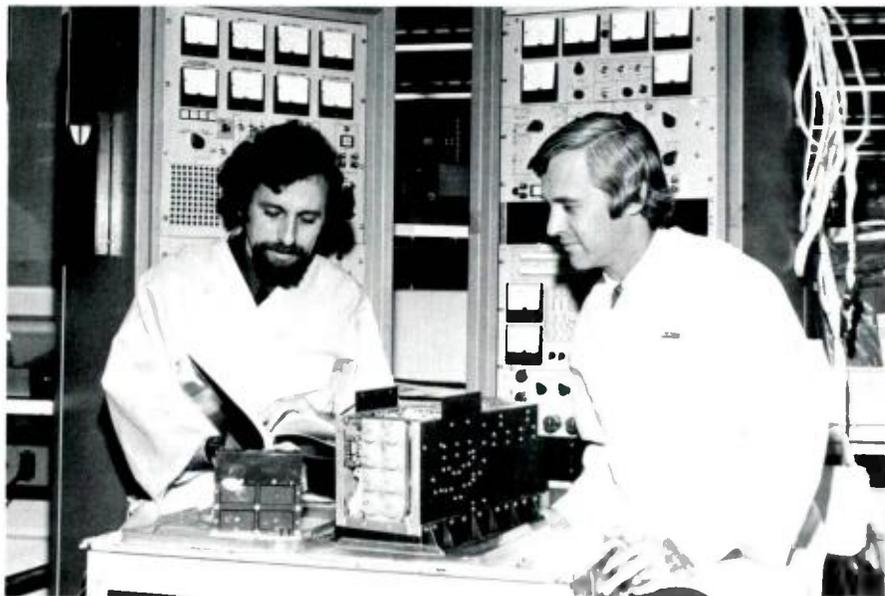


Fig. 1 — Power subsystem, basic block diagram.

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Authors Joel Bacher (left) and Pat Callen.

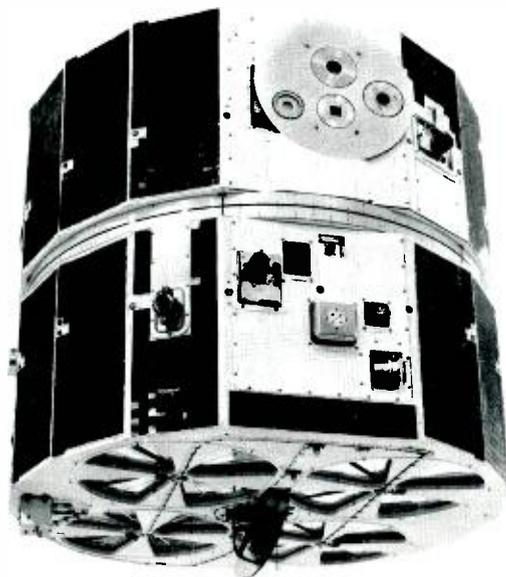


Fig. 2 — AE-C spacecraft, launch configuration.

Table 1 — Power subsystem performance requirements.

Power output:

- 66.7 Wh of experiment operating time (BOL)
- 33.3 Wh of experiment operating time, end of life (EOL)

Bus voltage distribution:

- Unregulated load bus of -26 to -38 V
- Regulated experiment bus of -24.5 V ($\pm 1\%$)
- Pulse load bus of -26.0 to -35.5 V

Maximum voltage to loads:

- -38.75 V, worst case

Maximum voltage control:

- 1) Multiple power dissipating elements
- 2) Series redundant pass transistors in dissipating legs
- 3) Redundant shunt limiter control circuitry
- 4) Automatic removal of a malfunctioning control circuit.

Load control:

- 1) Redundant pulse-width-modulated (PWM) regulators
- 2) Automatic removal of non-essential spacecraft load and turn-off of regulated bus when unregulated voltage falls below -25.7 V
- 3) Automatic turn-off of regulated bus should voltage on bus exceed range of -23.0 to -26.0 V

Battery charge control:

- 1) Individual charge controller for each battery
- 2) Current-limited battery charge at $C/4$ rate maximum (C is equal to battery nominal capacity in Ah)
- 3) Voltage-temperature taper charger characteristic
- 4) Third electrode cell overcharge control to reduce battery to $C/40$ when full recharge is accomplished (2 third-electrode cells per battery)
- 5) Automatic termination of all battery charge should high battery voltages, dependent upon battery temperature, be detected.
- 6) Automatic termination of all battery charge if battery temperature exceeds 37.5°C
- 7) Series redundant battery discharge diodes to preclude a single part failure from permitting uncontrolled battery charge.

Thermal control:

- Active control of battery (spacecraft upper baseplate) temperatures to range of 10 - 13°C , nominal.

trol subsystem. Table 1 lists the major subsystem performance requirements.

Subsystem configuration

The power subsystem, shown in Fig. 1, consists of a solar array (mounted on peripheral side panels) three batteries and a power supply electronics (PSE) unit. The design is based heavily on previous Nimbus and ITOS power subsystems, although several improvements have been made over earlier designs. (For example, battery charger performance has been improved.) Power generated in the solar array is supplied to the spacecraft loads through an unregulated power bus, which varies between -26 V and -38 V. All loads which are normally powered during the complete spacecraft orbit, whether essential for spacecraft operation or not, are fed directly from the unregulated bus. Those loads which are normally on only during data collection phases of an orbit (e.g., tape recorder, experiments, etc.) are fed from a tightly regulated -24.5 V bus. Battery charge power is supplied to each battery through an individual charge controller; during eclipse periods, and at those times when the load power exceeds the array's power generating capability, load power is supplied from the batteries through discharge diodes. The shunt limiter maintains the maximum unregulated bus voltage at -38 V by dissipating excess array power in resistance wiring mounted on the inside of the solar array substrates.

Solar array

The solar array for the AE satellite is located on the 16 side panels and the "bottom" of the satellite housing. Fig. 2 shows the assembled spacecraft. The side array (both upper and lower portions) is composed of a total of 86 parallel strings, with 81 to 87 cells in series for a total of 7380 cells. The bottom solar array consists of 2508 solar cells: 20 parallel strings with either 125 or 126 cells in series. The output of the two solar arrays is paralleled inside the PSE unit.

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This article was condensed from a paper presented by Bacher and Callen of AED and A. Obenschain of NASA-GSFC at the Intersociety Engineering Energy Conversion Conference, San Francisco, California, on August 20, 1974.

The work described herein was performed by the Astro-Electronics Division for the National Aeronautics and Space Administration under Contract NAS5-23003.

The solar cells are nominal 2 cm × 2 cm crucible-grown silicon cells, with a base resistivity of 1 to 3 ohm-cm. (The cells are slightly oversize, measuring 2.024 cm × 2.024 cm). The cells have an average base-cell efficiency of 11.7% at 0.46 V and 28°C; minimum beginning of life (BOL) "maximum power point" is 61.2 mW. Each solar cell is covered with a 1.5-mm (60 mil) fused silica coverslide; the coverslides have an antireflection coating applied to the outer surface to enhance transmission of energy to the solar cell. A blue filter is applied to the lower surfaces of the platelet. The cut-in point (50% transmission) for the blue filter is 400 nm ±15 nm with less than 1% average transmission characteristics from 300 to 370 nm. Sylgard 182 silicon rubber adhesive is used to bond the coverslides to the solar cells. Interconnection between solar cells within a circuit is accomplished using an expanded silver mesh material 0.058-mm (2 mil) thick. A fiberglass scrim cloth is used to isolate the solar cell circuits from the aluminum face-sheets of the solar hat substrates. The materials and fabrication techniques employed on AE have been used successfully for several years by RCA. The solar array characteristics are shown in Figs. 3 and 4.

The selected design was qualified by a two-step test program. In the initial phase, a small test panel (1 × 2 in.) was

cycled three hundred times in air through the expected worst-case-in-orbit temperature extremes of -80 to +120°C; no evidence of degradation appeared. The second phase attempted to simulate the effect of aerodynamic heating on the solar cell/coverslide assembly. The test panel was cycled 300 times from +20 to 130°C in vacuum, with a heat-up time of 30 seconds. The panel's cool-down from 130°C back to 20°C took approximately 15 minutes. Post-exposure electrical testing and visual inspection again revealed no degradation in performance.

Batteries

Each of the three batteries consists of 24 series-connected nickel-cadmium cells, including 2 cells which contain signal electrodes. The cells have a rated capacity of 6 Ah and a nominal voltage of 1.25 V. The batteries contain thermistors for charge control, temperature telemetry, and for signal-electrode temperature reference. The inter-cell series wiring is dual-redundant. The 24 cells are packaged upright, in 2 parallel rows of 12 cells each.

The junction between each cell and the baseplate is insulated by a 0.005-in. layer of mylar film, with thermally conducting grease at the interfaces. An organic coating on the top surfaces of the cells

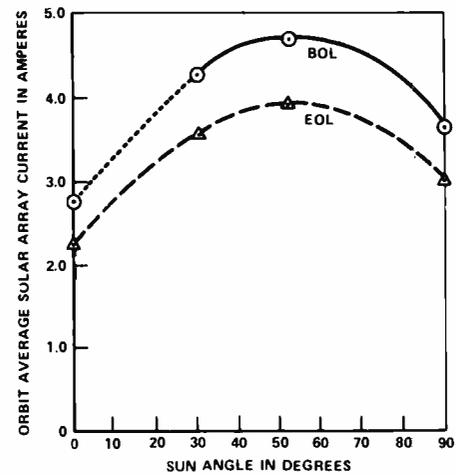


Fig. 4 — Solar array current vs sun angle.

(including terminals) prevents accidental short circuits and protects the cells from handling damage. The total battery weight is 8.9 kg (19.6 lb).

The battery cell is manufactured by General Electric for aerospace use. The cell separator is Pellon 2505 non-woven nylon, and the cell container is deep-drawn of 304L stainless steel. The average cell weight is 264 g. The cell design provides a minimum negative-to-positive ratio of 1.5:1, as verified on sample completed cells. The actual capacity is 7.0 to 7.5 Ah, measured at the 3.0 A discharge

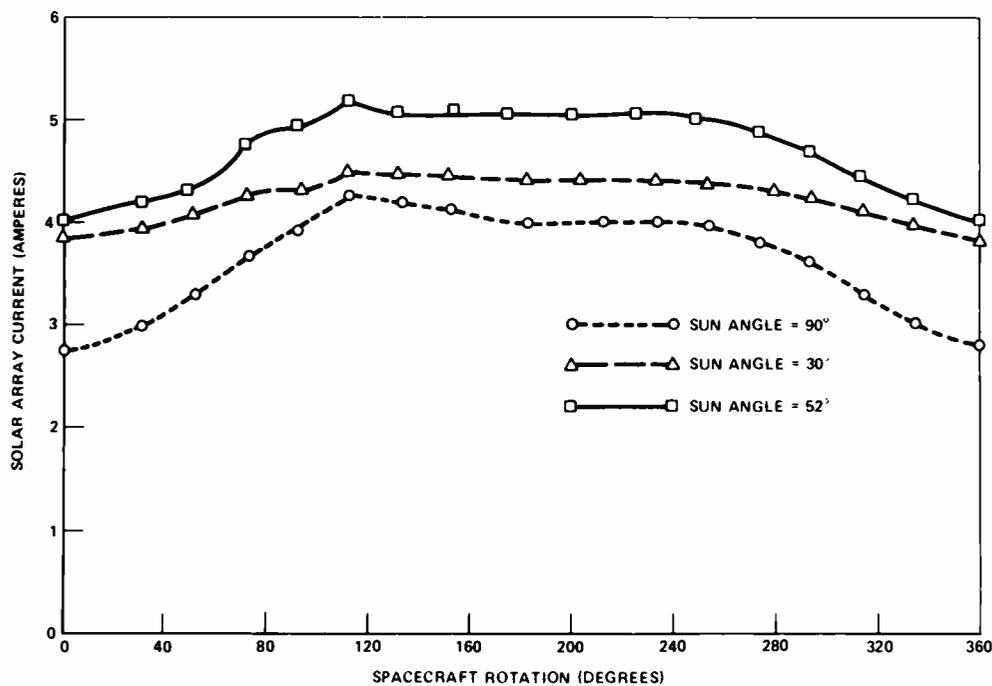


Fig. 3 — Solar array output vs spacecraft rotation angle.

rate to the 1.10-V cutoff. Both electrodes are insulated from the cell container by ceramic feed-through terminals, manufactured by Ceramaseal.

The cell signal electrodes indicate when the battery reaches full charge. The signal electrode is in common electrolyte with the positive and negative plate stack. When the electrode is connected to the negative terminal through an external resistor, a current flows through the external resistor if oxygen is present within the cell. The oxygen pressure can thus be determined by reading the voltage drop across the load resistor. The magnitude of the signal electrode output is dependent upon the resistance of the load resistor, cell temperature, and oxygen pressure. The system is set so that when the temperature-dependent trip level is reached (due to oxygen evolution), the battery charge current will be reduced from full level or voltage-limited taper current to the trickle charge level. The system will remain under trickle charge (C/40) until the oxygen pressure decreases below the reset point.

The battery charge control system is based upon a primary current limit (C/4) with a temperature-sensitive voltage limit. The purpose of the signal electrode is to cause further reduction in charge current to the trickle level (0.150 A), in order to decrease the resultant overcharge heating and gas evolution and to increase battery reliability. Fig. 5 shows the variation of signal electrode trip and reset point with temperature. The charge current will be reduced to the trickle level when either of the two signal electrodes in each battery reaches the trip point. The current will not be returned to the full charge (or voltage-tapered level) until the output of both electrodes is below the cutback point (also temperature dependent). Each battery is independently controlled.

To assure proper operation of the charge control system, the first group of cells received was subjected to test programs for characterization of charge voltage and signal electrode voltage. The charge voltage characterization test consisted of

repetitive charge-discharge cycling to 18% depth of discharge (typical AE spacecraft operation). The V/T curve, lower curve of Fig. 6, was selected to provide the desired charge-to-discharge ratio for a typical orbit.

The value of the signal electrode cell load resistor was selected after extensive characterization testing at the expected temperature extremes of the AE batteries. The relationship between pressure and voltage level was determined for different load resistors. The greatest signal sensitivity was observed with a load resistor of 2000 ohms, particularly at the lower temperature range.

A more complete description of the battery charging system is provided in a later section of this paper.

Power supply electronics

A block diagram of the PSE unit is shown in Fig. 7. The major design changes in the AE PSE from its predecessors are in the

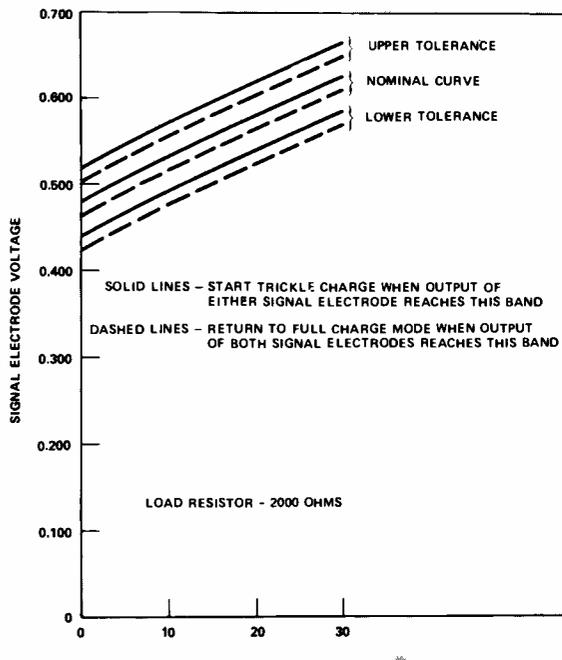


Fig. 5 — AE signal electrode control curves.

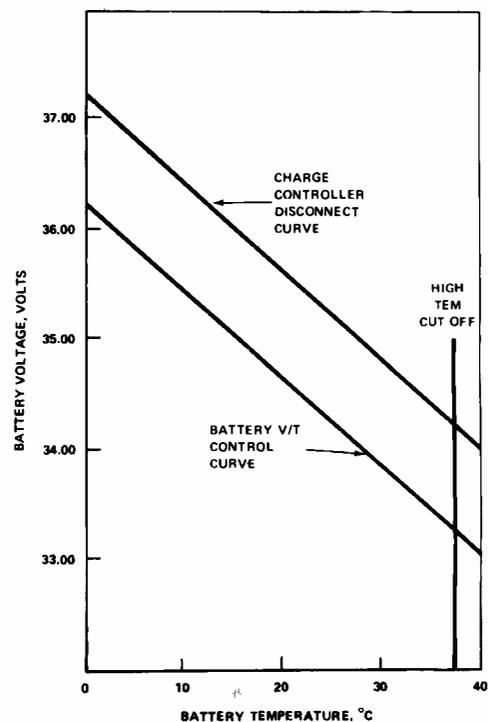


Fig. 6 — Battery charging voltage limit vs. temperature.

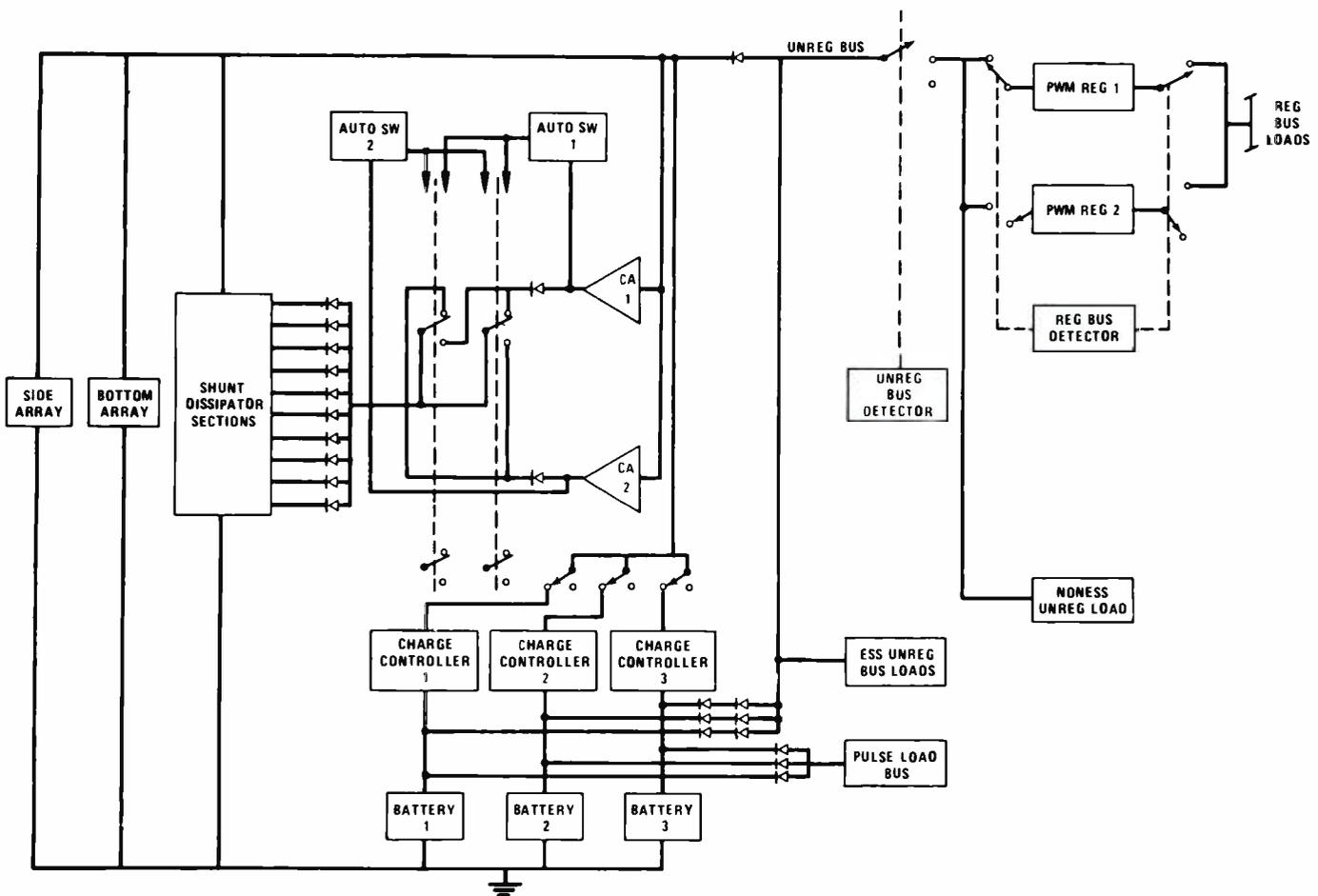


Fig. 7 — Power supply electronics block diagram.

area of subsystem protection — to insure that spacecraft equipment failures do not degrade the power subsystem's performance.

Unregulated bus voltage distribution

As shown in Fig. 7, the unregulated bus is connected to both the solar array and the battery through blocking diodes; the connection with the solar array is through parallel redundant diodes, while each battery discharge leg contains two series redundant diodes. During the daylight portion of the orbit, the unregulated bus voltage telemetry is 0.6 to 0.8 V lower than the solar array bus voltage. At night, the unregulated bus is 1.0 to 1.2 V lower than the battery voltage.

The pulse load bus is formed by connecting the three batteries together with the PSE and is used to power high current demand devices. Supplying power to devices such as squibs, thruster, and tank valves, etc., from the unregulated or regulated busses would present unaccept-

table voltage spikes to the other spacecraft loads.

Regulated bus

The design of the pulse-width-modulated (PWM) regulator for AE draws heavily on the proven Nimbus design. It permits the transfer of power from the unregulated bus to a regulated -24.5 V bus with a 92% conversion efficiency at a nominal 6-A load. The unit is current-limited at 16 A, so that a regulated bus load failure can not damage the unit. Fig. 7 shows that there are two identical regulators, only one of which can be connected at a time; of course, both regulators can be disconnected. To insure regulation within the required $\pm 1\%$ of -24.5 V a minimum 400-mA load is placed on the regulator when it is connected. This load is automatically connected whenever a ground command is sent to turn on a regulator and is commanded "off" when other loads (in excess of 400 mA) are applied to the regulated bus.

Battery charge control

The charge controller electronics efficiently charges each battery and protects the battery from over-current, over-temperature, over-voltage (as a function of temperature), and excessive over-charge. Circuitry in the PSE provides these functions by monitoring and operating upon the following parameters:

- a) Battery charge current,
- b) Battery voltage (as a function of temperature),
- c) Battery signal electrode voltage (third electrode oxygen-sensing device, and
- d) Battery temperature.

Normally, each battery will be charged at C/4 (1.5 A) when sufficient current is available from the solar array. When the voltage of the battery reaches a preset limit (temperature dependent), the charge current will be automatically reduced, to maintain the battery voltage at the desired limit. The current will decay to a value dependent upon voltage limit and

temperature. The signal electrode's output will be used to reduce the steady-state overcharge current to a trickle value of $C/40$ (150 mA).

The combination of voltage-temperature limit and signal electrode control is reliable because of long and successful experience with the former and extensive test data for the latter. This system combines the best features of each. The voltage-temperature limit does not drastically cut the charge current when the limit is reached; it merely reduces the current, according to the rate of voltage rise. The signal electrode control, which is used to reduce the current to $C/40$, will trigger after the cells have reached full charge and have started into the overcharge period.

The controller will operate in four normal modes: current regulator, voltage-temperature (battery voltage limit mode), battery signal electrode, and the hi-

voltage, hi-temperature cutout mode. Each mode is discussed separately.

Current regulator mode — In this mode of operation, the charge controller operates as a current regulator, limiting the charging current to the maximum pre-established limit of $C/4$ ($1.5 A \pm 8\%$). This feature is unchanged from previous designs.

Battery voltage limit mode (voltage-temperature) — In this mode, the maximum voltage at which the battery can charge is limited. Also, the battery's maximum voltage limit is adjusted as a function of temperature, as indicated by the lower curve of Fig. 6.

Normally, at the beginning of charge, the state of the battery will require the controller to operate in the current-limited mode. As the battery is charged, its terminal voltage is increased. Should

the voltage-temperature combination exceed the limits, the controller senses this condition and acts to maintain the operating state of the battery within this mode. In this mode, the controller acts as a battery voltage regulator where the circuitry is designed to vary current in order to maintain control of battery voltage.

Battery signal electrode — When the output from either of the third-electrode cells in a battery reaches the limit shown in Fig. 5, the charge rate is reduced to a nominal 150-mA level. This circuitry responds to temperature: the higher the temperature, the greater the required signal electrode output.

When both cells indicate that the battery needs to be recharged, return to a normal (either current-or voltage-limited) charge mode is made. This circuit can be disconnected via ground command should a

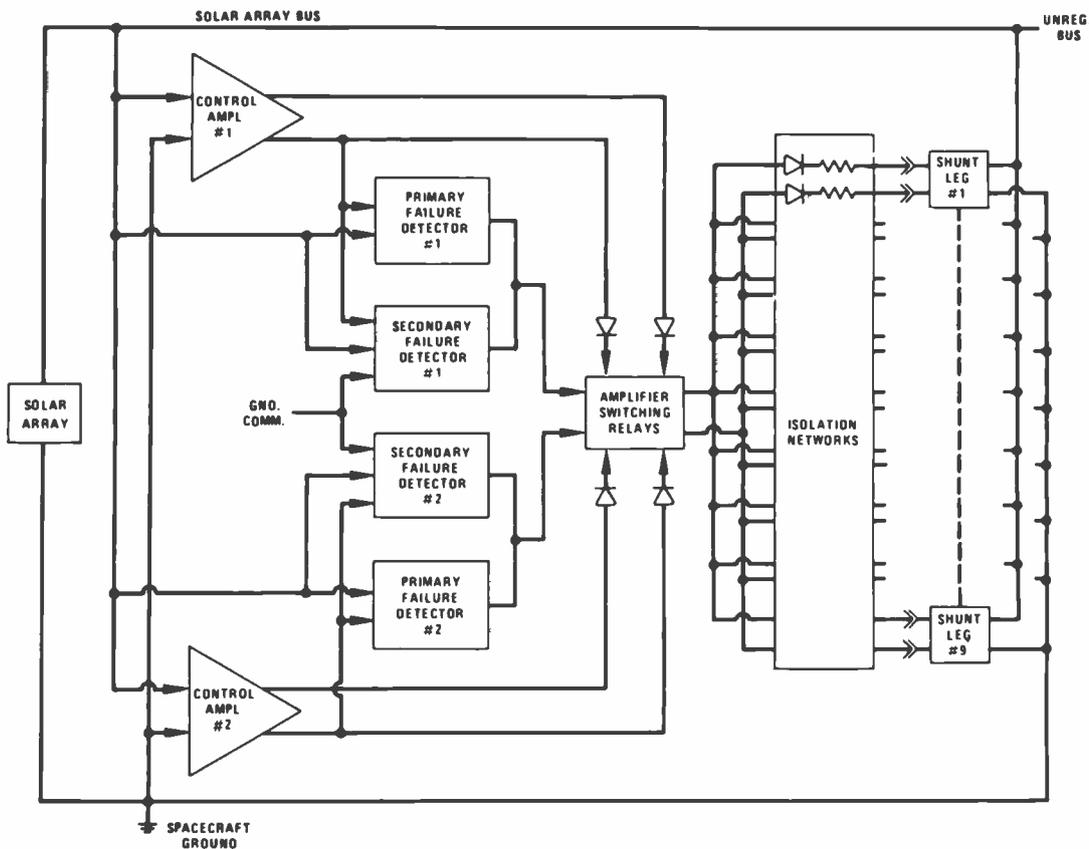


Fig. 8 — Shunt regulator.

failure occur that locks the charge into a trickle charge mode.

Hi-voltage, hi-temperature disconnect circuit — The charge controller will be disconnected from the solar array bus if the battery voltage, as a function of temperature, exceeds the voltage-temperature upper limit as shown in Fig. 6. This is a new protection feature developed for AE.

When the battery voltage (as a function of temperature) or the battery temperature exceeds the limits in Fig. 6 (upper curve), a Schmitt trigger is driven such that it actuates the disconnect relay; the relay is a latching type and return-to-charge mode must be initiated by a ground command. Also included in the design is a high-temperature cutoff circuit, which removes all battery charge current at a battery temperature of 37.5°C. In the event of circuit failure, the entire cutoff circuit may be disabled by another ground command.

Solar array shunt regulator control

The shunt dissipator limits the solar array bus voltage to -38.75 V by dissipation of excess solar-array power. A block diagram of the shunt regulator is shown in Fig. 8. Control of the maximum solar-array bus voltage is achieved by shunting current through the shunt dissipator sections when the control amplifier(s) sense an increase in solar-array voltage above the cut-in level.

The shunt limiter consists of nine shunt dissipator power sections on the solar-array panels and two control amplifiers in the PSE unit. Only eight of the nine power sections are required to control the solar-array bus.

Each control amplifier compares the solar bus voltage to a voltage reference and provides an output current which is proportional to the difference (error signal). The control-amplifier output current is fed through isolation diodes to a common bus and then through isolation networks to each of the power shunt dissipators, which are located on the solar array. The shunt dissipator amplifies the control current causing some of the solar-array current to become shunt limiter current, which in turn decreases the solar-bus voltage to a level where the control-

amplifier error signal is minimized. The net effect is a closed-loop, negative-feedback control system which provides voltage limiting.

The control-amplifier failure detection control protects the spacecraft against any failure in a control amplifier which would cause the shunt dissipators to be turned on in error. This is accomplished by detecting a simultaneous condition of a solar-array voltage less than 36 V and the presence of control-amplifier output current. Each of the two redundant control amplifiers is provided with an independent failure-detection control. A ground command is available to remove a "failed-on" control amplifier should the failure detection circuit not perform. The ground command is routed through a secondary failure detector which requires the simultaneous condition of solar-array voltage less than -36V and the presence of control-amplifier output current to allow the ground command to "gate" through. This arrangement prevents the inadvertent removal of a non-failed control amplifier in the event the redundant control amplifier has previously failed open; otherwise an excessive solar-array voltage condition could occur. An additional ground command is provided to permit the reconnection of a control amplifier that was automatically or ground-commanded "off".

Each of the nine dissipation legs is broken into two series sections, having a pass transistor associated with each. The use of serially redundant pass transistors precludes a single part failure from loading the solar array. The dissipation element is resistive wiring, bonded on the inside of each solar hat to distribute the generated heat evenly over the entire spacecraft surface.

Regulated bus detector

The regulated bus detector will automatically disconnect the on-line PWM voltage regulator if the regulated bus voltage leaves the range of -23.0 to -26.0 V. Voltage levels derived from the regulated bus are compared with a reference voltage by two differential amplifiers, one of which detects an over-voltage condition, and the other an undervoltage condition. The amplifier outputs are combined by an "OR" gate leading to a Schmitt trigger. If either amplifier detects an error, the Schmitt

trigger changes state and actuates a relay in the regulated bus line, thereby disconnecting the on-line PWM voltage regulator. The regulator may also be switched on-line or off-line via the relay by ground commands. In the event of a circuit failure, the entire circuit may be disabled or enabled by two ground commands which drive a relay in the power supply line.

Unregulated bus undervoltage detector

The undervoltage detector will a) automatically disconnect the on-line PWM regulator from the unregulated bus, and b) provide a 40-ms pulse of unregulated bus power to the CDU when the unregulated bus voltage falls below -25.7 V. The pulse to the CDU is used to remove all non-essential spacecraft unregulated bus loads.

A voltage derived from the unregulated bus is compared with a reference voltage by a differential amplifier. When the amplifier detects an error, the Schmitt trigger changes state and actuates a latching relay in the unregulated bus line. As a result, the relay disconnects the PWM regulator from the unregulated bus, and also supplies an ac pulse to a nonlatching relay, which supplies a momentary relay closure to the CDU. The latching relay may also be switched to either state by ground commands. In the event of a circuit failure, the entire circuit may be disabled or enabled by two ground commands which drive a relay in the power supply line. The use of an undervoltage detector is unique to the AE design.

An important feature of the PSE design is that all protection functions can be overridden via ground command. This insures that a failure in a protection circuit does not jeopardize the proper operation of the power subsystem.

Acknowledgment

The authors wish to acknowledge the significant contribution of Elmer Holloway of AED who was responsible for the design of the solar array.

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Automatic monitoring in phased-array radar systems

H.P. Brockman|J. Liston

A hypothetical yet practical phased-array radar system is used to illustrate automatic monitoring techniques for evaluating performance and operational readiness of modern day radars. Testpoint monitoring throughout the system, including checks of the arithmetic logic in the beam steering controller, and the implementation of target simulation for overall system performance evaluation are described. Particular emphasis is placed on measurements of the electrical characteristics of individual array elements and associated hardware. A brief discussion of the algorithms used to monitor array-element amplitude and phase is included. Although an L-band phased-array model was used, the concepts are generally applicable to virtually any frequency band used by modern phased-array radars.

THE COMPLEXITY of present-day phased-array radars dictates some form of automatic monitoring equipment to confirm premission and postmission operational readiness. When the system is operated continuously on a 24-hour basis

or when a high availability/reliability (A/R) product is required, automatic fault detection and fault isolation are required to obtain an acceptable mean-time-to-repair (MTTR). This paper describes such automatic monitoring

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Jack Liston, Principal Member Engineering Staff, Systems Engineering, Missile and Surface Radar Division, Moorestown, N.J., received the BSEE from Drexel University in 1953 and the MSEE degree in 1963 from the University of Pennsylvania. His early experience included design and systems engineering work at RCA MSRDC, Bell Telephone Laboratories, and General Electric. Since rejoining MSRDC in 1970 he has been assigned major systems responsibility for concept design, performance analysis, and design optimization on advanced phased-array radar system developments. Some of the areas of his principal contributions include system computer modeling for cost optimization and performance tradeoffs, advanced self-duplexing receiver concepts, and system performance verification through simulation. Mr. Liston is a member of the IEEE and Eta Kappa Nu, he is a registered professional engineer in Pennsylvania.



concepts; although the model chosen is typical of large phased-array radar systems, many concepts described are equally applicable to other radar system types.

Consider a conceptual phased-array radar whose antenna array is composed of several thousand *transmit/receive* (T/R) elements or modules essentially operated in parallel. This model also includes a signal processor and a data processor to provide simultaneous tracking and signature analysis of multiple targets. The interface of the central monitoring equipment with the rest of the system is the central feature of the block diagram (Fig. 1). The term central monitoring is used to distinguish between the remote built-in-test equipment (BITE), located in each major subsystem, and the central monitoring equipment which provides direct control of the monitoring functions and acts as the central collection agency for all monitoring data. Overall control of the monitoring system resides in the system computer so that each monitoring function can be performed automatically under software control in synchronization with normal system operation.

Monitoring functions

Major monitoring functions performed in the system include:

- Testpoint monitoring
- Loop tests
- Summary status reporting
- Target simulation
- Array monitoring

Testpoint monitoring consists of the monitoring of testpoints such as power supply voltages, detected rf signals, switch closures and arithmetic quantities in each major subsystem.

Loop tests are used to exercise and check the digital logic. Known word patterns are inputted from the computer to a subsystem, where they are looped around at various stages of the logic, and outputted back to the computer where a bit-

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by-bit correlation is made between input and output words.

Summary status reporting is the reporting of the status of key parameters in each subsystem on a go, no-go basis which is used to alert the operator of major system failures.

Target simulation at i.f. is built into the system to facilitate alignment and calibration of the system and to act as a test stimulus for other monitoring functions in the system.

Array monitoring is a series of tests used to check for degradation in the phase and amplitude response of each of the thousands of T/R elements in the antenna array.

To achieve automatic control, individual test routines (software modules) are provided for each of the monitoring functions just described. Each test routine may be initiated by the operator at the computer keyboard or included as normal system operation at a pre-established priority level. All tests are performed automatically by computer commands which include mode selection, test stimuli generation and data requests. A request for specific data is handled in the equipment on a dwell (or timing interval) basis or on an address basis, sequentially, one at a time. That is, one data word is outputted for each data request. Test results are printed out on a hard-copy printer, at operator request, for evaluation. In addition, an alarm light is lit on the display console in the event of a malfunction or no-go indication on any testpoint.

Testpoint monitoring

The primary purpose of testpoint monitoring is to detect and isolate faults throughout the system. Except for arithmetic quantities, the go, no-go thresholding of all test points is performed in the parent equipment so that the status of each test point is a one-bit digital level. These data bits are formatted in parallel into words of nominally 10 bits which are identified by unique monitoring addresses received from the computer. Arithmetic quantities are formatted and identified in the same manner. In general, the number of bits in the parallel word is tailored to the size of the largest arithmetic word. Test points are monitored on an address basis se-

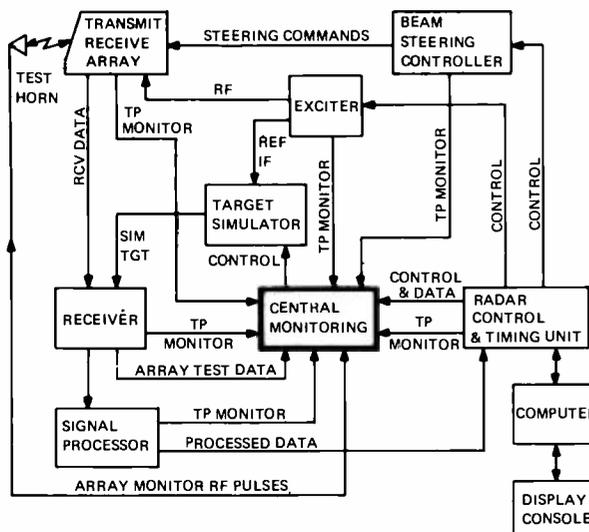


Fig. 1 — Block diagram of illustrative system.

quentially, one at a time.

Power supplies monitored in each subsystem verify that the voltage is within a specified percentage of the nominal value. A comparator, precision reference voltage, and thick-film precision resistor-divider network may be used to threshold the upper and the lower voltage limits — and convert the signal to a go, no-go digital level. A similar approach may be used to monitor video and detected rf signals. If the go, no-go amplitude threshold range of these signals varies widely from one testpoint to another, a potentiometer adjustment may be provided to set the threshold for each signal. Switch closures for interlocks and temperature sensors are monitored by using a simple resistor-divider network to convert the signals to digital levels. The open-switch state should always be defined as the no-go condition so that the circuit will alarm, if the wiring to the switch is disconnected.

As illustrated in Fig. 1, testpoint data is sent to the computer via the central monitoring equipment. This equipment provides the timing and control for the selection of testpoints in each subsystem on an address basis, and for the collection and formatting of the data for orderly transfer to the computer. Since central monitoring has a testpoint monitoring interface with each major subsystem, a common digital interface is developed for all subsystems. In the development of the interface, three major constraints should be considered in obtaining a cost-effective design: 1) the logic should be capable of operating asynchronously with respect to the timing of the subsystem under test, 2) the size and com-

plexity of the logic in the remote monitoring equipment should be minimized, and 3) the number of interface cables necessary to extract the monitoring data from each subsystem should be small. A tradeoff of these constraints suggests the adoption of a serial digital data transmission system for both the monitoring address and data.

Arithmetic monitoring

Our system model has several thousand array elements requiring steering commands to form and point the radar beam. By forming subarrays of 32 elements each and by using digital subarray steering, the number of steering command (arithmetic quantities) needed to steer the array may be reduced by a factor of approximately 15 to 1. To minimize the signal distribution complexity, this data is sent serially from the beam steering controller (BSC) to the array signal-distribution system. To verify the integrity of the arithmetic logic in the BSC, each of the steering command signals is monitored, one at a time, at the BSC output line drivers by a digital multiplexer. As the data is shifted out to the array, the data from one line is also shifted into a 10-bit shift register via the multiplexer for monitoring. Monitor addresses, one for each steering command signal, are allocated to monitor these signals. The arithmetic quantities obtained are compared with expected values, for selected steering commands (phase taper) in the computer, to verify that the arithmetic performed by the logic is correct. Bit patterns of all ones and alternate ones and zeros are used in the steering command word to fully exercise the logic and to ensure that carry bits are propagated properly in the

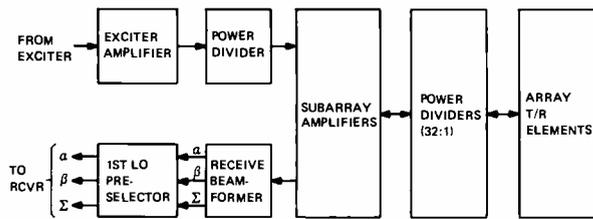


Fig. 2 — Phased-array antenna signal distribution.

arithmetic operations. Logic associated with the distribution system which distributes the steering command signals to the T/R modules is checked indirectly by performing phase and amplitude measurements on each T/R module during array monitoring.

Target simulation

An i.f. target simulator is built into the system for alignment and calibration. Because the system under consideration is coherent, using pulse expansion (chirped fm waveforms) and pulse compression techniques, adequate checkout of the signal processor requires the same chirped fm waveforms as input stimuli. Since the antenna array is checked separately by the array monitoring equipment (described below) and the receive signal is converted to an i.f. frequency of 282 MHz prior to being sent to the receiver portion of the signal processor, the generation of simulated targets at i.f. was justified as a cost-effective tradeoff. In this manner, the cost and complexity of injecting rf waveforms via a relatively high far-field test tower is avoided.

To adequately check the monopulse tracking loops of the signal processor, three signals are required, namely, the sum (Σ) and two error signals (α and β). These signals should be variable in range, doppler, attenuation and relative phase with respect to each other. In addition, all waveforms normally transmitted in the system should be programmable. These conditions can be met with a simulated target generator; the simulated target waveform exercises most of the hardware used to generate the transmit waveform for the transmit array during normal operation. The only hardware added is a frequency synthesizer which provides for target doppler. Either the chirped waveforms or a 60-MHz CW signal may be selected by the waveform select switch. The selected waveform is mixed with 342 MHz $\pm f_d$ to generate the required 282 MHz $\pm f_d$ i.f. target signal. It should be noted that 60-MHz CW is selected to generate either a CW or pulsed-CW

signal for test purposes only and is not used during normal system operation. Pulsed-CW is obtained by gating the 342-MHz signal with the LO gate.

Array monitoring

The phased array antenna has several thousand T/R elements and associated signal distribution elements (see Fig. 2). Each T/R element is a wideband transmit/receive module containing a 4-bit diode phase shifter, T/R switch, transistor amplifiers, circulator and TR limiter. For signal distribution purposes, there are over one hundred subarrays of 32 modules each to form the array. Each subarray is driven by one subarray amplifier. Transmitter drive to these units is provided by the exciter amplifier and power divider. The receive signals are fed to the beamformer to form the three monopulse tracking signals (i.e., Σ , α , and β). These three signals are translated down to 282 MHz in the first local oscillator preselector prior to transmission to the receiver cabinet.

The primary objective of array monitoring is to measure the performance of the several thousand T/R modules and the associated subarray amplifiers and to

check for performance degradation on a day-to-day basis.

The technique employed to make gain and phase measurements on each TR module is to use a near-field test horn, located approximately 100 feet from the array face, and to transmit or receive from only one T/R module at a time. Array measurement tests are implemented as illustrated in the block diagram of Fig. 3. All tests are made using an uncoded 400 microsecond L-band pulse. Appropriate switching is provided to select either the Σ channel output of the beamformer during receive mode or the test horn output during transmit mode for gain and phase measurements. The L-band test signal is converted to 282 MHz in a mixer and fed to the network analyzer along with a 282-MHz CW coherent reference signal. The test signal is also sent to a power meter which is used as a standard for initial calibration of the network analyzer. Under these conditions, the gain and phase outputs of the analyzer phase-magnitude display are two video pulses with sufficient rise time such that the response is flat to within 1% of the final value after 200 μ s. These signals are sampled approximately 25 μ s prior to the end of the 400 μ s pulse by the A/D converter via the multiplexer, for transfer to the computer via the RCTU.

For receive mode measurements, all T/R modules except the one under test are switched to transmit mode without radiating rf. The test signal is then injected at rf via the test horn on the near field tower. The signal is received and monitored at the beamformer Σ channel

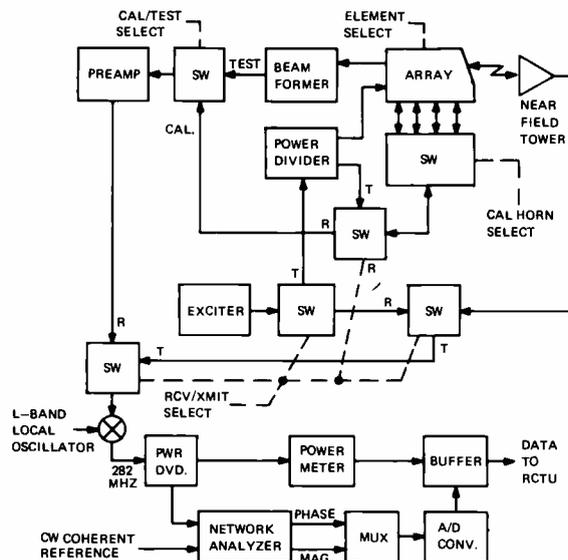


Fig. 3 — Array measurements block diagram.

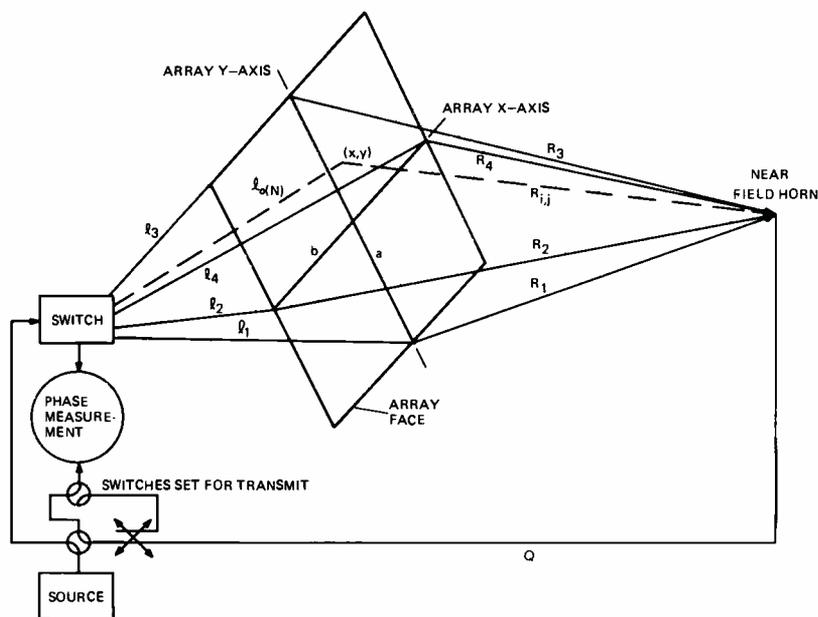


Fig. 4 — Phase measurement schematic.

output by the network analyzer at a frequency of 282 MHz. For transmit mode of operation, all modules, except the one under test, are switched to receive mode and rf power is transmitted from the module under test. Gain and phase measurements are performed on each T/R module for both modes and for several phase shifter positions as tabulated below:

Mode	Phase-shifter phase (degrees)	Measurement
Transmit	0	Gain and phase
Receive	0	Gain and phase
Receive	22.5	Phase
Receive	45	Phase
Receive	90	Phase
Receive	180	Phase

In addition, gain and phase measurements are made on each of four calibration horns located on the periphery of the array for computation of relative gain and phase on each T/R module so that the current data can be correlated with previous data in an archival file. Using this approach, gain and phase measurements on each element can be made with a maximum rms error of 0.3 dB and 5 degrees, respectively. The manner by which the data are processed by the computer is considered next.

Algorithms for phase and amplitude measurement

The equations used to measure amplitude

and phase at individual elements of a phased array are based on the geometry shown in Fig. 4. The amplitude measurement algorithms are derived from one-way, range-dependent, path-loss considerations similar to those used to determine signal strength at the terminal of a one-way communication link. The phase measurement algorithm is based upon the consideration of the phase difference between the rf path containing the array element under test and each of four reference elements located around the array periphery. In this manner, the resulting phase measurement is made relatively insensitive to bias errors in the estimated lengths of the interconnecting cables, which are program input parameters.

Phase measurement

The phase measurement test consists of sequentially measuring: 1) the phase (relative to a coherent reference) at a convenient point in the rf path which serves the array element under test, and 2) the phase in the rf path which serves one of the four reference horns. The measured phase difference is simply the arithmetic difference of measurement (2) from measurement (1).

This measured phase difference is then compared with the calculated phase difference computed on the basis of the geometry existing among the reference horns, the near-field test horn, and the array element under test; the cable lengths required for rf signal distribution are

taken into account. The difference between the measured phase difference and the calculated phase difference is defined as the differential phase disparity. For a given element under test, the process is repeated with respect to each of the four reference horns and the differential disparity values are averaged.

Amplitude measurement

The amplitude measurement is executed at the same time that the phase data is gathered. The raw amplitude data is obtained from the same instrument that provides the raw phase data. Gains through the paths containing the element under test are measured and compared with calculated nominal values; those elements whose path gains are outside specified gain tolerance limits are flagged accordingly.

Conclusions

To obtain an effective automatic monitoring system in large complex phased-array radars, several monitoring techniques have been considered. Each technique described was tailored to meet the requirements of the monitored subsystem.

The following monitoring philosophy has emerged from this effort: 1) testpoint monitoring is best suited for monitoring static signals such as power supply voltages and switch closures, while loop tests are best suited to checking digital logic; 2) target simulation provides the best technique for evaluating the performance of the signal processor, and 3) special techniques must be used to evaluate phased array performance at the element level.

Phased-array integrity verification requires rather sophisticated measuring techniques. Although the use of a near-field test horn to radiate or receive rf energy from an element of the antenna array appears to be straightforward, phase and amplitude measurement at L-band are complicated by the physical geometry of the test horn with respect to the array. Computer techniques provide a means of accounting for the array and test-horn geometry so that array amplitude and phase measurements can be made at the element level without providing hard wired interconnections from the array elements to the monitoring equipment.

An IC for breakerless ignition systems in automobiles

R.L. Sanquini

In automotive applications there is a need for an integrated circuit to effect breakerless ignition systems, and thus, result in reduced maintenance and improved engine performance. Such a circuit is described which is also applicable to a wide variety of industrial applications.

THE PRIMARY purpose of the system shown in Fig. 1 is to eliminate the need for breaker-points in controlling the ignition coil commonly used to fire the spark-plugs of an internal-combustion engine. Breaker-points are a significant maintenance item; worn points adversely affect engine performance. A breakerless system consists of a distributor with a contactless pick-up, an electronic control unit, and an ignition coil. Operation of the circuit shown in Fig. 1 is based on the accurate amplitude-modulation of a resonant-circuit oscillator in which the inductor acts as the sensor. When the conductive material of a toothed, metallic trigger wheel in the distributor enters the field of the sensor (L), eddy current losses in the non-magnetic wheel-tooth reduce the Q of the resonant circuit and decrease the amplitude of oscillations to a specific level at which discrete transistor Q_c interrupts the coil current. When the oscillator amplitude has decreased below

the switching level, a variable-feedback system in the IC maintains a minimum amplitude of oscillation. This lower amplitude level eliminates timing variations which would occur if the oscillator had to be restarted by random noise. Therefore, either transition may be used to control event timing. The system performance is comparatively independent of dQ/dt ; i.e., pulse amplitude and noise immunity are maintained over a wide range of rotor (engine) speeds. In a typical automotive application, capacitor C_2 parallel-resonates the circuit at a frequency between 200 and 400 kHz.

An output circuit produces a switching signal ϕ at terminal 4 and its complement $\bar{\phi}$ at terminals 6 and 7; signal ϕ is high in response to a high oscillator state. When ϕ is high, Darlington-connected transistors Q_b and Q_c are driven by base current supplied via resistors R_f and R_g , so that current flows through the primary

winding of the ignition coil. The peak coil current is limited by a "current-setting" transistor, Q_a , in response to the voltage-drop developed across current-sampling resistor R_h .

A spark is generated when ϕ goes low and $\bar{\phi}$ high. Switching is initiated by a low signal at terminal 4; the signal turns transistors Q_b and Q_c off. When the current flowing through the coil primary is interrupted, its stored energy is transferred to the secondary circuit where it produces a high voltage that fires a spark plug. Diode D_1 protects Q_b and Q_c against excessive negative voltages and the application of reverse battery voltage. Although noise produced by the spark is suppressed to meet the applicable standards, an additional circuit consisting of C_1 , R_c , D_3 , C_5 , R_1 , and the output amplifier in the IC, assures that noise will not affect the switching.

Description of the IC

The block diagram of the IC is shown in Fig. 1; Fig. 2 shows the schematic diagram. The 0.063×0.075 -inch chip, Fig. 3, is contained in a 14-lead dual in-line-plastic package.

The basic oscillator is of the tuned collector type, with emitter feedback. It comprises transistors Q_6 , Q_7 , Q_{11} , associated current-sources, and external I.C. Transistors Q_{13} and Q_{14} constitute an active envelope detector. The aux-

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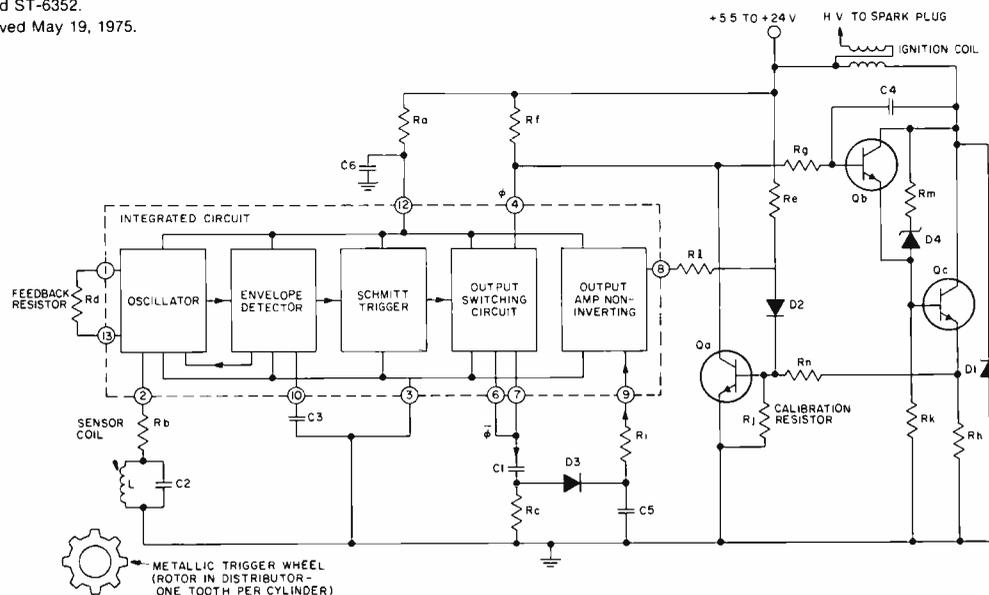


Fig. 1 — Block diagram of the breakerless ignition system.

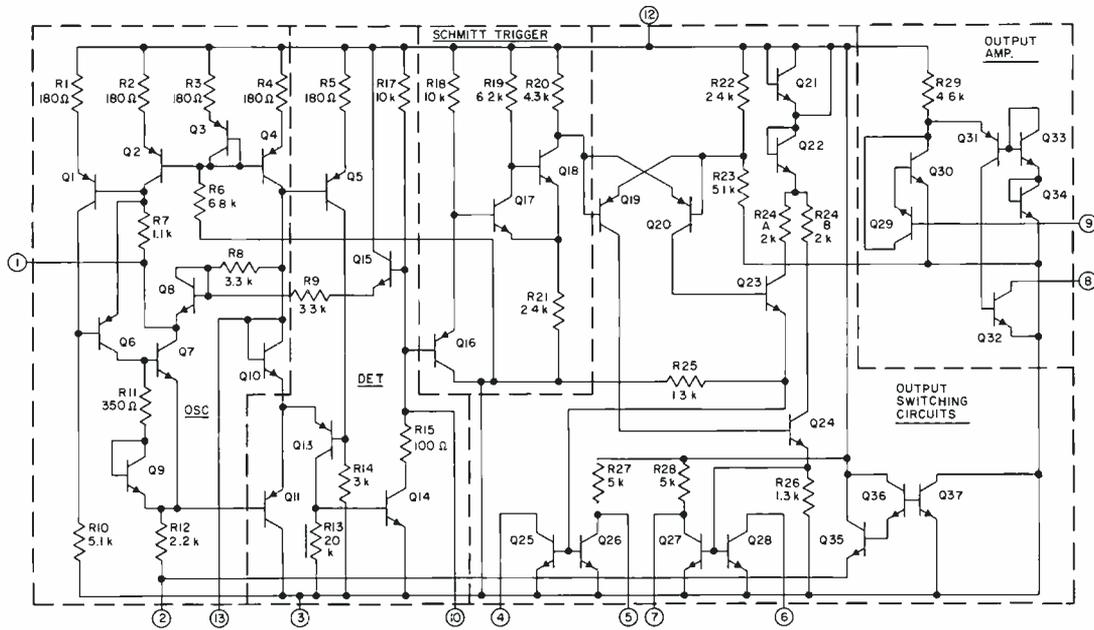


Fig. 2 — Schematic diagram of the IC.

92CM-25646

illary feedback circuitry mentioned above consists of diode-connected $Q8$, $R9$, and $R8$; it is actuated when the output of the detector goes high as the oscillator amplitude decreases. In the low-amplitude state when diode-connected $Q8$ is turned on, additional feedback is provided to the oscillator through resistor $R8$.

The Schmitt trigger circuit utilizes transistors $Q16$, $Q17$, $Q18$ and resistors $R19$, $R20$, and $R21$. It is isolated from the envelope detector by transistor $Q16$ and current-limiting resistor $R18$. The two threshold voltages are developed across resistor $R21$; the high threshold voltage is developed when $Q18$ is driven to saturation.

Transistors $Q19$ and $Q20$ develop signals with 180° phase difference; transistor $Q20$ controls the ϕ -signal at terminal 4, and $Q19$ controls the $\bar{\phi}$ -signal at

terminals 6 and 7. Transistors $Q29$, $Q30$, and $Q32$, the active transistors in the output amplifier, provide the noise immunity feature described above.

Since terminal 2 leads into the distributor, it is imperative that protection against spurious transients which might otherwise damage the IC be provided. A degree of transient attenuation is supplied by resistor $R6$, Fig. 2. Additional protection is provided on-chip by transistors $Q35$, $Q36$, and $Q37$.

Conclusion

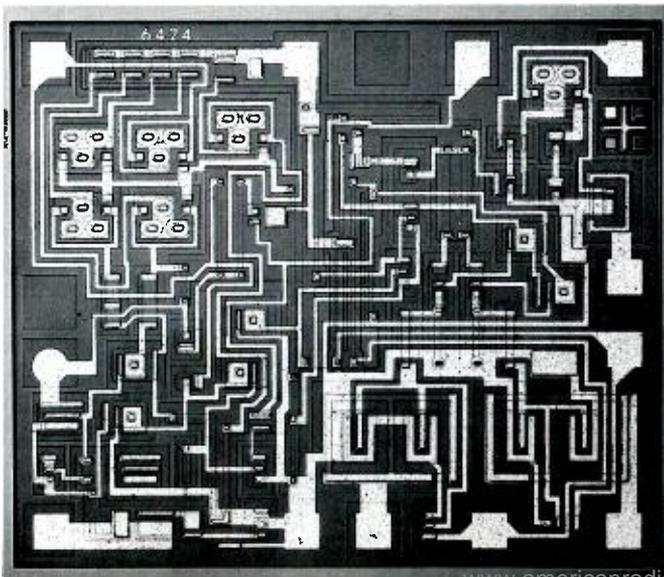
Although the IC has been described in connection with an automotive application, it should be apparent that it is equally applicable to a wide variety of industrial applications; e.g., tachometers, speed-control systems, and proximity detectors.

Acknowledgment

The author thanks A. Leidich, the IC circuit designer, and M.V. Hoover, M.E. Malchow, and R. Bertoldo for their efforts in converting this product from a laboratory curiosity to a reliable, low cost product for the automotive industry.

Richard L. Sanquini, Director, Bipolar IC Products, SSD, Somerville, N.J., received the BSEE from the Milwaukee School of Engineering in 1959, and has done graduate work in electrical engineering at Columbia. In 1959, Mr. Sanquini joined RCA as a design and development engineering trainee. After concluding the training program, he was engaged in the design and analysis of customer applications using solid state devices. In 1962, he joined the Integrated Circuit Design group as an application engineer. From 1962 to 1966, he was engaged in the design, application and testing integrated circuits. From 1966 through 1971, Mr. Sanquini held various engineering management positions in the Linear and Digital Integrated Circuit groups. In 1971, he assumed the responsibility for all engineering in the Linear Integrated Circuit product line. Mr. Sanquini was promoted to Director, Bipolar Integrated Circuit products in 1974. He has published 9 technical articles concerning integrated circuits and has been active on the Micro-electronic's Committee of the EIA, Electronic Industries Association.

Fig. 3 — Photograph of the IC.



Auto electronics — a semiconductor supplier's view

R.M. Cohen

This paper reviews the steps taken by the semiconductor industry to be responsive to the requirements of the automotive industry, with special emphasis on one recently developed and highly cost-effective method to control and improve device reliability. Two new product innovations — one combining MOS and bipolar technology to produce a high performance and versatile operational amplifier integrated circuit, and the other an inherently more reliable process for IC manufacture involving a hermetic silicon die and a corrosion-resistant lead-connection system — are also described, particularly as they relate to automotive applications.

R.M. Cohen, Dir., Solid State Product Assurance, Solid State Division, Somerville, N.J. received the BSEE and BSME from Stevens Institute of Technology in 1948. He joined RCA in 1940 in the Receiving Tube Applications Laboratories in Harrison. He continued in Receiving Tube Engineering until 1956 when he transferred to Solid State Applications Engineering. In 1963 he became Manager of the combined Receiving Tube and Solid State Consumer Product Engineering Department, and in 1967, he assumed his present position. Mr. Cohen received the RCA Award of Merit in 1957 and was made a Fellow of the IEEE in 1966. He is a member of the Editorial Board of the *RCA Engineer* and has served on a number of United States Government and Industrial Technical Committees. He is currently a member of the JEDEC Council. Mr. Cohen is the author of several papers and holds seven U.S. Patents.



THE SEMICONDUCTOR industry has enjoyed a long and, we believe, mutually successful relationship with the automotive industry over a span of several decades, or in other words almost since the origin of the semiconductor industry. Starting with the substitution of transistors for the vibrator in the auto radio, to the present am-fm stereo multiplex system, the transition to solid state in the entertainment portion of automobile electronics is now virtually an accomplished fact; and, we think most would agree that the change has resulted in substantial product improvement. The non-entertainment or functional portions of the automobile began to employ solid-state devices later, but they also show a series of successful innovations such as alternator diodes, voltage regulators, electronic ignition, automatic speed-control systems, various forms of fuel-management systems (most still in development) and a host of other innovations, some made better by electronics and others made possible only through the use of electronic control systems.

Emphasis on reliability

Many in the solid-state industry believe that the automobile industry, compared with other major electronics customers, is slow to accept the benefits of solid-state devices. But those who work in the areas of product reliability; those who are cognizant of safety implications, the high

cost of product recall, and the detrimental effects on continued customer satisfaction caused by a poorly performing product — fully appreciate the special need for exhaustive product development and field evaluation in the auto industry. From the point of view of the semiconductor supplier, the rate of development of solid-state applications in the auto industry has been extraordinarily fast, and generally more thorough in terms of reliability evaluation than that of many other industries which may appear to show a greater rate of solid-state innovation. Despite this rapid rate of progress, we believe the present progress in the non-entertainment area of automotive applications is impressive, but just the tip of the iceberg in terms of what lies ahead in the near future. The semiconductor industry is putting great emphasis on new product development to extend device performance capabilities so that automotive industry needs may be well served; recently, we have become equally responsive to the real needs for cost-effective reliability control. Just as much or more emphasis is being exerted in the reliability area, as was previously placed on technological innovation.

Commercial aspects

What are some commercial aspects of the relationship between the automotive and the semiconductor industries? How does the automotive industry, as a customer, relate to the semiconductor industry, as a supplier?

For the U.S. where we have fairly accurate marketing statistics, Table I shows

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automotive solid-state product consumption in recent years as a percentage of the total U.S. dollar consumption projected to 1979.¹ Though the automotive industry is a major significant market worthy of special consideration in our product development plans, the extreme diversification of the semiconductor industry is clearly revealed in these figures. The solid-state industry is fully capable, from a logistical point of view, of serving the needs of the automotive industry, providing we have reasonable lead time and can work together in product development and in planning for production implementation. While the percentages shown may not be overwhelming, they do represent a very substantial unit volume for our industry, and an important segment of the business which RCA aims to serve to the best of its capability. Table II shows the estimated power transistor usage in millions of units during the period from 1973 to 1975. The figures reflect only one type of semiconductor product. We believe that the increase in 1975 will occur despite the depressed economy, since a larger percentage of current production cars utilize solid-state ignition systems.

Automotive applications, located in the engine compartment, present an unusually severe environment for electronic components — and especially for solid-state devices which are fundamentally sensitive to temperature, humidity, and voltages stress. Table III, a summary of previously presented data, shows the relatively difficult conditions to which devices are exposed.^{2,3} While these conditions are well recognized now, the extremes of voltage encountered under some unusual conditions were not always so well understood, so that the often referred to *learning curve* in the solid-state industry has a different connotation to some of us who lived through the investigation and subsequent solution to some early systems-failure problems.

Reliability

Coupled with these challenging environmental conditions is the need for a level of field reliability which has as the only practical objective virtually trouble-free performance. We recognize that under-the-hood applications require a much higher level of reliability than that of other high-volume consumer-product

applications; thus, new highly cost-effective approaches must be developed to meet this challenge. Some of us in the solid-state industry are responding to this difficult problem for present applications in an effective way which sets the stage for continued progress towards our ultimate goal of failure-free systems performance.

Table IV illustrates what happens when the old, conventional method of indicating the reliability of solid-state com-

ponents is applied to control very-low-failure-rate performance objectives. The practical absurdity of the conventional approach is immediately obvious. Furthermore, the 1000-hours life test provides information on the level of product reliability in a much delayed and after-the-fact fashion. To use these life tests as a *gate* to control the flow of product to a customer involves excessively high inventories (about 6 weeks production). Moreover, if the product

Table I — Automotive solid-state consumption.

Year	Percent of total consumption
1973	3.3
1974	3.9
1975	4.6
1979	5.7

Table II — Estimated power-transistor usage in millions of units in domestic automotive systems.

Year	Millions of units
1973	95
1974	145
1975	160

Table III — Comparison of conditions in automobile passenger and engine compartments.

Environmental parameter	Passenger compartment	Engine compartment
Chemical	100% relative humidity	100% relative humidity plus grease, oil, water, anti-freeze, solvent fuels, salt spray.
Temperature		
Operating ambient	-30°C to +85°C	-40°C to +125°C
Temperature cycling	5000 cycles from 15°C to 75°C to 15°C for typical 50,000 miles service	5000 cycles from 15°C to 95°C to 15°C for typical 50,000 miles service
Thermal Shock		10°C water spray quench from 125°C
Electrical	Short-term battery voltage ranging from 5 to 24 volts Transients: to +120 with 45 ms time constant, to -80 V with 30 ms time constant Reversed battery polarity	

Table IV — Sample size required for 1000-hr life test.

Failure Rate %/1000 Hrs.	With zero failures at 90% confidence	With one failure at 90% confidence	With three failures at 90% confidence
1.0	231	390	668
0.1	2 303	3 891	6 681
0.01	23 026	38 980	66,808
0.001	230 000	389 000	668 000

fails, both the customer and supplier are faced with the difficult choice of holding the product for further screening, possible scrapping, a shut-down of the customer's line for lack of product, or a review of the nature of the failure and rationalizing as to how much reliability risk may be involved in its use. Neither situation is satisfactory for the supplier or the customer. The semiconductor manufacturer's production department is also concerned about the reported life-test failure, and when members of this group question the quality department or the engineering department for information concerning product improvement and progress of life tests, they take an understandably dim view of being told to wait 1000 hours for the completion of life testing before their questions can be answered. This situation, as incredulous as it seems, is actually a fair representation of what was occurring in our industry as the modus operandi regarding the life testing of high-volume consumer-oriented products. At the time, it was a cost-effective way of serving a market that expected and could tolerate a few percent of field failures. For those special applications requiring a high degree of reliability control, the industry offered various types and levels of *high-reliability* products which met very tight AQL

levels, were 100-percent burned in, and which were backed by expensive documentation involving every stage of manufacture and test.

Although, such approaches eliminated many risks associated with the consumer-product type of life control, the same methods were not cost-effective for high-volume applications because the incremental costs associated with such procedures ranged from a minimum of about 50 cents per device to costs as high as \$50 per unit. Clearly, a different method of measuring and controlling the life portion of our products on a real-time basis, rather than on a 1000-hour, after-the-fact basis was required. We believe we have developed a viable solution to providing these real-time controls, and have already gathered substantial field evidence on the improvement in reliability which these controls can provide without generating excessive costs in the process.

A program of real-time controls begins with the early stages of device development, continues through systems evaluation, and is then applied as a manufacturing process control. Furthermore, the real-time concept continues as field failures are examined, analyzed, and the

procedure is continually honed until every form of inherent, latent failure mechanism which has ever appeared or will likely appear is detected. Real-time indicators (RTI) are usually derived from a series of stress tests made on newly developed products. The samples are tested to destruction under incremental stress levels; the stress level which causes failure is recorded on each sample in the group. All devices are analyzed to determine the physics of failure mechanisms, and those units found to fail at significantly lower levels than the "norm" are especially scrutinized to determine why they are different. Generally, this inspection results either in design corrections or process improvements to correct the faults revealed. Several of these stress tests, some applied sequentially, termed *reliability verification sequence* tests (RVS), are selected for use as process controls on the manufacturing line. These tests take only minutes, hours, or at the very most several days to perform, and offer a very effective control of the reliability of the product.

In SSD, design and selection of these controls is the responsibility of the Reliability Engineering Laboratory, an independent engineering service group reporting to the Division Manager of

Table V — Differences between classical group-B tests and real-time controls.

<i>Approach</i>	<i>Group-B tests</i>	<i>Real-time controls</i>
1. Test Considerations	At maximum device ratings or less	Overstress many times to destruction
2. Overall	General, multi-subgroups, "shotgun" approach	Specific, predetermined reliability engineering experimentation necessary, "rifle" approach.
3. Types of Failure	Non-predictable multi-failure modes: read 6 to 15 electrical parameters	Visually one failure mode; i.e., look for evidence of one specific failure mechanism. Many times electrical readings not required.
4. Frequency	Usually once per month	Weekly — Daily — Hourly
5. Product Stage	Completed, electrically tested product	All stages of product
6. Sample Size	Large (approximately 150 per each subgroup)	Small (approximately 40), taken more frequently
<i>Effectiveness</i>		
1. Decisions	Very poor, after the fact	Immediate and Direct
2. Reliability Predictability	Poor, considering current low level failure rates	Excellent, considering protection from accelerated conditions
3. Problem Detection, Feedback, Corrective Action	Poor	Excellent, quick response on today's product with measurable quick evaluation of corrective action
4. Efficiency of One Test Rack	8 tests/rack/year (1000 hr. test and down period)	90 tests/rack/year (3 day max. and 1 day for changing product)
5. Test Duration	Approximately 6 weeks	Minutes to three days maximum

Quality and Reliability Assurance. This work is done with the complete cooperation and assistance of the design and materials engineering groups, and through our applications laboratory with the assistance and cooperation of our customers as we attempt to cover their particular field-environment requirements. The development of RTI's requires a thorough understanding of the device design and the materials and processes involved in its fabrication and assembly, excellent failure-analysis capability, and a very thorough understanding of applied statistics. In our company, determination of RTI's represents a major effort during new device development, but we consider it crucially significant in order to meet the increasing pressures for improved reliability control represented by the emerging automotive applications.

Table V illustrates the contrast between the classical methods of life testing and the RTI generalized approach. This table, while accurate, is by no means the full or even a partially detailed description of RTI⁴. Admittedly, some extra production-line testing is done under the RTI system, but no one challenges its cost-effectiveness in terms of reducing potential product losses or field-failure costs. For the present at least, because the concept is relatively new, we continue to run life tests and correlate the results with the RTI's. Analysis of life-test failures may indicate the need for additional RTI's or the modification of existing tests. If so, this adjustment is made, and thereafter we see little or no additional life failures from this cause, not because the failures are screened out by the RTI's, but as a result of the process modifications which reduce or eliminate that particular failure mechanism.

Fig. 1 shows how the application of RTI's effectively removes those lots which contribute to early field failure. Continued application of the RTI to the manufacturing process coupled with field-failure analysis and corrective action should lead to a continuing improvement in the reliability levels, one of the fundamental advantages in this approach.

New products

While these successful efforts to improve reliability and devise better approaches to

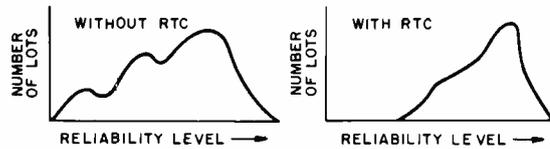


Fig. 1 — Distribution of reliability levels with and without RTC.

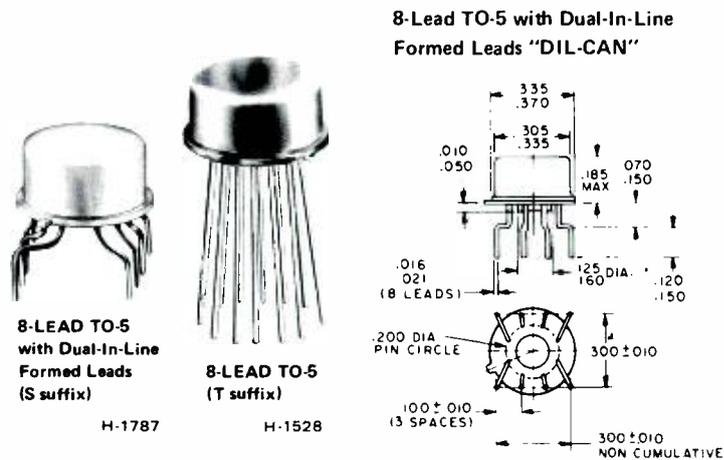


Fig. 2 — The CA3130BT. COS/MOS operational amplifier with MOS/FET input.

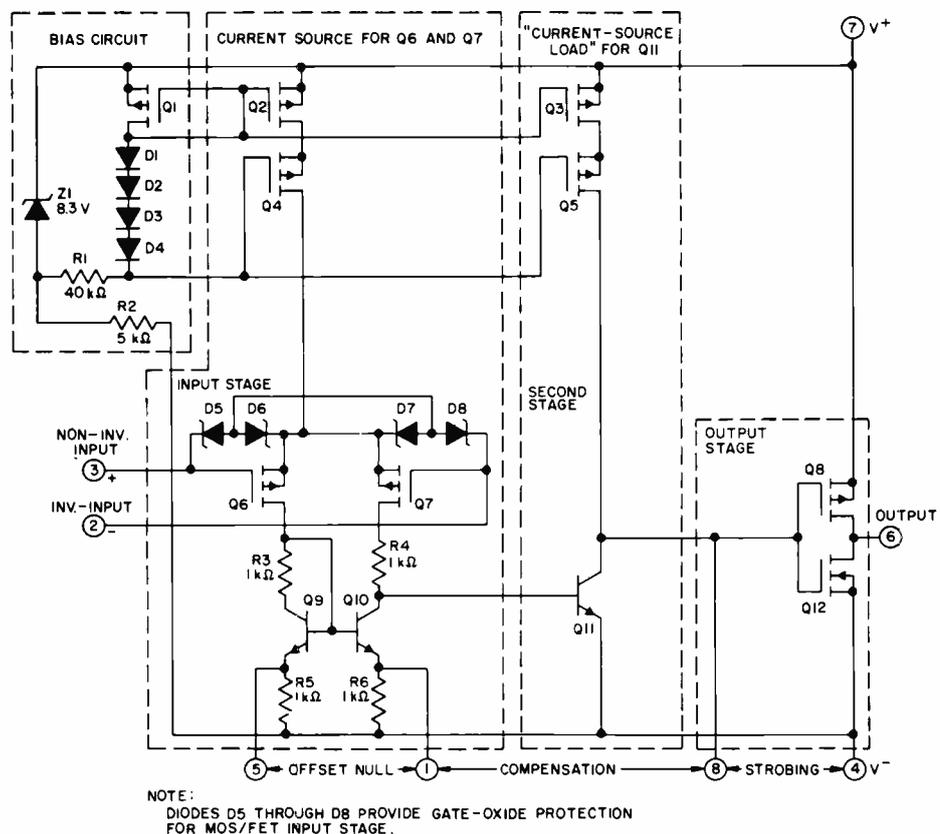


Fig. 3 — Schematic diagram of the CA3130 series.

reliability control continue, product innovation also continues in the semiconductor industry. Two new RCA solid-state developments are especially worthy of note. One advances the state-of-the-art of operational amplifiers and is useful in sensing, timing, and control circuits. The other provides an order of magnitude improvement in the reliability level of plastic-encapsulated integrated circuits exposed to extremely severe temperature and humidity cycling.

Fig. 2 is a photo of a new operational amplifier, the RCA-CA3130 series, among the first to combine on one monolithic chip MOS and bipolar devices. This combination of technologies provides an integrated circuit which offers the very high input impedance of the MOS process with the high current gain and stability inherent in bipolar devices. Its high gain coupled with fast response time and extreme circuit versatility makes it an interesting new component. The device also features diode-gate protection to reduce its susceptibility to damage by electrostatic discharge or low-energy circuit transients. Fig. 3 is a schematic diagram of this new IC showing the functional location of the PMOS input devices, the bipolar devices used to convert the differential input to single-ended output and to provide high and stable stage gain, and the complementary-symmetry output stage. This IC is especially suited for single-supply applications found in automotive electrical systems.

The other development which will undoubtedly have far-reaching effects in improving the reliability of plastic-encapsulated IC's used in under-the-hood automotive environments involves the development of a truly hermetic chip; the plastic case serves only to provide some mechanical support for the external lead assembly. The titanium, platinum, and gold metallization system coupled with the silicon nitride pellet passivation used in this device provides a terminal connection system which is highly resistant to the corrosive effects of moisture penetration. The first of these devices, the RCA CA3724G, is a high-current n-p-n transistor array consisting of four separate transistors, each one of which is capable of handling up to one ampere and is rated for a collector-to-base voltage of 80 volts under cut-off conditions. Fig. 4

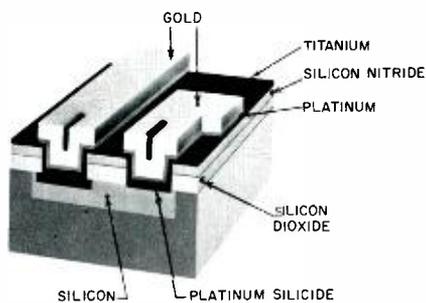


Fig. 4 — Plastic encapsulated IC metallization system.

shows the metallization system employed in this new series of IC's. Note that this system provides a wafer in which the only active surfaces exposed to the ambient atmosphere are silicon nitride and gold. Silicon nitride (Si_3N_4) even in very thin layers is impervious to water penetration and the commonly troublesome junction-damaging contaminants, such as sodium.

Table VI, an extension of data presented in an earlier report on the general subject of plastic-packaged IC reliability⁵, reveals the resistance of these devices to extremely accelerated temperature and humidity tests. Conventional aluminum-metallized plastic-packaged IC units show high failure rates when subjected to similar exposure. Realizing that this is just the first of a series of devices planned to utilize this new process, it shows real evidence of the responsive attitude on the part of the semiconductor industry to develop new devices which are more capable of meeting the specialized reliability requirements of the automotive industry.

Table VI — Reliability of silicon nitride passivated tri-metal (titanium, platinum, gold) devices an epoxy package.

Test	Duration	Failures
Temperature Cycle -65 to +150°C	1000 Cycles	0/250
Thermal Shock -65 to +150°C	600 Cycles	0/30
Pressure Cooker 203 KN/M ² (30 PSIA) and 121°C	100 Cycles	0/233
Bias Pressure Cooker 85°C, 85% RH 15 Volts Reverse Bias	208 Hours	0/230
	72 Hours	1/250

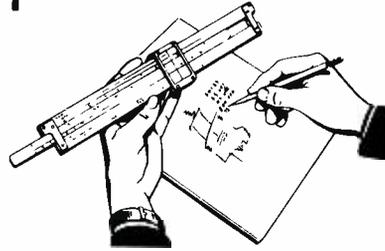
Conclusion

It is interesting to note that despite unanticipated systems problems, and a few device problems, no new application of solid-state devices in the automotive field has even reverted back to the original system, even on a temporary basis. The semiconductor industry is gradually maturing, and is at last listening to the the automotive manufacturers and doing something concrete about enhancing reliability and reducing and controlling field failures. There is now more understanding of this need than ever before. It is also apparent that the automotive industry is becoming more aware of the fact that electronics really can contribute to the system performance advantages that are of increasing significance to all. Future efforts of the semiconductor and automotive industries will result in continued cooperation and a host of new and important innovations that will contribute to automotive safety, performance, and economy.

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Engineering and Research Notes



Thermal duplication of magnetic tape using rf energy



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A device for high speed duplication of magnetic tape, such as video recording tape, is shown in Fig. 1. The face of the copy tape, having a layer of magnetic material, is heated above its Curie temperature by contact with an intermediate thermally conductive transfer medium.

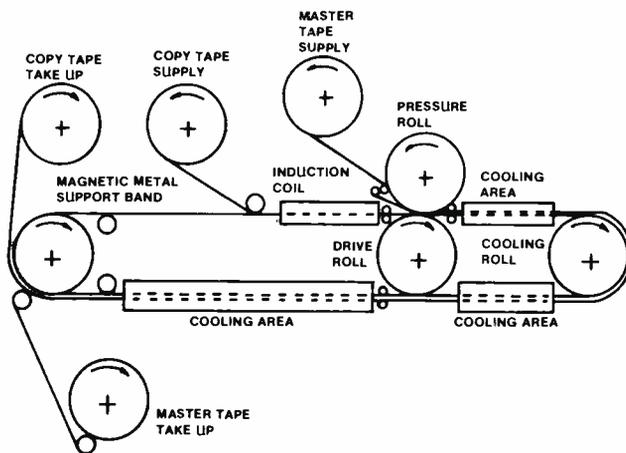


Fig. 1 — Device for high speed duplication of magnetic tape.

The device consists of several feed and take-up reels, a thin metal band (less than ten mils in thickness) and an appropriate radio-frequency energy source to heat the metal band. The device operates by feeding the

copy tape onto the metal band and heating both the tape and band from a radio-frequency energy source. The master tape is fed onto the copy-tape/metal-band combination and all three are allowed to cool while remaining in contact, during which time the transfer of information from master to copy is effected. The master tape and the copy tape are wound on take-up reels after duplication.

This process depends on the master tape having a relatively high Curie temperature as compared to the slave or copy tape. It also depends on the physical fact that when the copy tape is elevated in temperature, it becomes paramagnetic so that as it cools under the influence of another magnetic field (*i.e.*, the master tape), it takes on the mirror image of the master tape. For video recording use, the master tape would therefore be a mirror image of the information first recorded.

The system provides a desired even distribution of heat and a desired low degree of thermal deformation of the physical shape of the copy tape. In addition, such a system affords higher thermal duplicating speeds than are presently available.

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Soldering flux for dissipation of thermal shock



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This flux is designed to diminish the problem of thermal stress-cracking of semiconductor wafers. Stress cracking usually occurs when metallic contacts are formed on the wafers by dipping them into liquid solders maintained molten at elevated temperatures.

A previous method has been to preheat the wafer to a higher temperature, but below that of the melting point of the solder. Another prior method has been to preheat the liquid solder flux to a temperature below the evaporation temperature of the water of water-based fluxes. The draw-back of both these methods is that there is no "cushion" to diminish the thermal shock while the wafer is being immersed into the molten solder.

The present flux employs glycerine, or physico-chemically similar fluid, as a solvent and carrier for the components of an otherwise standard

flux. The glycerine can be preheated to temperatures substantially higher than conventional water-based fluxes. This reduces the thermal gradient between the temperature of the wafer and the temperature of molten solder.

Furthermore, the heat of glycerine evaporation or its pyrolytic decomposition, and the vapor film layer between the wafer and molten solder, formed while immersing the wafer, dissipates the thermal shock which otherwise would be acting upon it.

A typical formulation is 20 grams of $ZnCl_2$ and 20 grams of NH_4Cl dissolved in 100 milliliters of water-white glycerine. The formulation is used at $150^\circ C$ to $200^\circ C$. Any aliphatic, or aromatic, non-polymerizing (poly) alcohol, or any derivative thereof, exhibiting solvency for $ZnCl_2$ and NH_4Cl flux components, may be used in place of glycerine.

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60-Hz cordless clock

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The clock described in this note need not be connected to a 60-Hz source but must be sufficiently close to a power line to be able to receive a signal at this frequency.

The 60 Hz signal is picked up by an antenna and applied to the active passband filter (Fig. 1). The filter includes a complementary symmetry (COS/MOS) amplifier, a pair of capacitors (C_1 and C_2) and an input resistor R_1 . Looking from input point A into the antenna, the resistance at 60 Hz is approximately 1 megohm. In an active passband filter of this kind with an impedance at this level, the input impedance to the inverter must be of an extremely high value. This impedance (i.e., in the order of 60 megohms) is provided by the COS/MOS inverter within the filter. While the gain of the inverter (approximately 50) is far less than that of a bipolar operational amplifier, it is adequate to provide a Q of about 10. At this Q, and a center frequency of 60 Hz, the passband is 60 ± 3 Hz which is found to be adequate for most conditions of electrical noise.

The amplifier stage comprises three COS/MOS inverters. The first two

inverters are biased to operate as linear amplifiers by dual high impedance transmission gates connected between the inverter input and output terminals. Each inverter comprises two p-type devices and two n-type devices to increase the inverter gain.

The amplifier drives a phase-locked loop which includes an *exclusive-or* gate operating as a phase comparator, a low-pass rf filter, and a voltage controlled oscillator (VCO). The phase-locked loop compares the oscillator frequency with the 60-Hz line frequency supplied by the amplifier to lock the voltage controlled oscillator to the line frequency. If for some reason the 60 Hz input signal disappears for a short period, thereby unlocking the loop, the low-pass filter output voltage causes the voltage controlled oscillator to continue to oscillate at 60 Hz. This results from the long RC time constant of the filter which, during this short period, continues to hold the oscillator frequency at 60 Hz. This long RC time constant also provides good noise immunity.

The phase-locked loop drives a 60 Hz synchronous motor via inverter buffer stages; this motor, in turn, drives the hands of the clock.

A principal advantage of this circuit is that the clock does not require a crystal. In addition, most of the circuitry can be integrated. Moreover, because of the use of COS/MOS circuits, the clock requires very little power.

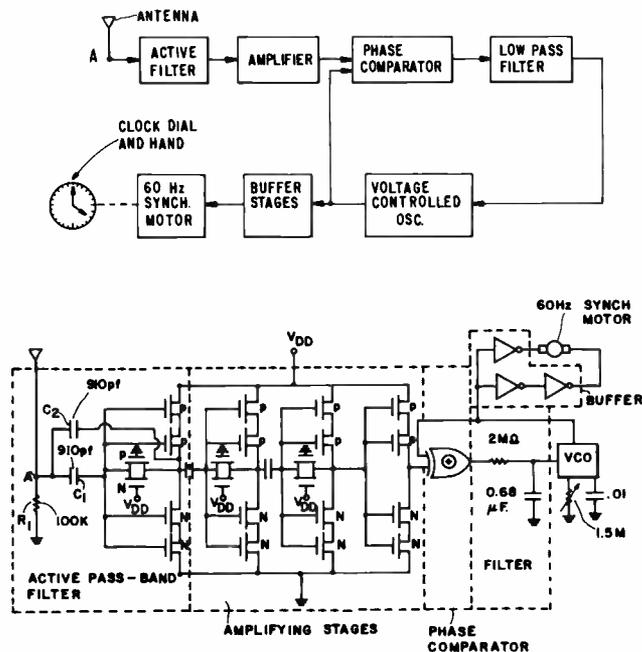
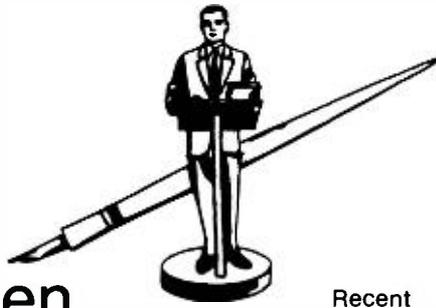


Fig. 1 — 60-Hz cordless clock — block diagram and schematic.

Reprint RE-21-2-2| Final manuscript received October 18, 1974.



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CYCLIC ARITHMETIC CODES, A program for the study of — T. E. Kupfrian (GCASD,Burl) Thesis for Masters at Lowell

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OBJECTIVE DIAGNOSIS of pathologic cytology smears by SEES, Preliminary results of — S. Larach (Labs,Pr) Automatic Cytology Conference, Asilimar, Calif.; 6/8-13/75.

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INDUSTRIAL LOGISTICS MANAGEMENT — J. W. Hurley (MSRD,Mrstn) Two-hour lecture on "Procurement (purchasing, design, production, etc.)" — 4/22/75, The Philadelphia Chapter of the Society of Logistics Engineers at Temple University.

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SPACE, TV requirements for manipulation in — L. Freedman (AED,Pr) W.H. Crooks (Perceptronics, Inc.) P.P. Coan (NASA) 2nd Conf. of Remotely Manned Systems, Los Angeles, Calif.; 6/9-11/75

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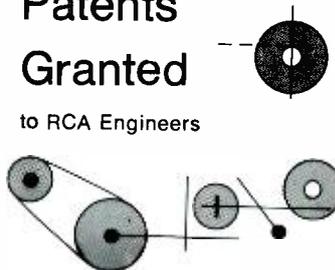
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Patents Granted

to RCA Engineers



Laboratories

Modified czochralski-grown magnesium aluminate spinel and method of making same — G.W. Cullen, S.R. Bolin, J.F. Corboy, J.E. Creamer, A.J. Wasilewski (Labs, Pr) U.S. Pat. 3883313, May 13, 1975

Efficiency light emitting diode — H. Kressel, H.F. Lockwood (Labs, Pr) U.S. Pat. 3883888, May 13, 1975

Dual growth rate method of depositing epitaxial crystalline layers — J.F. Corboy, G.W. Cullen, N. Pastal (Labs, Pr) U.S. Pat. 388506*, May 20, 1975

High voltage regulator — D.H. Pritchard, A.C. Schroeder (Labs, Pr) U.S. Pat. 3885198

Image display employing filter coated phosphor particles — S. A. Lipp (Labs, Pr) U.S. Pat. 3886394, May 27, 1975

Control Apparatus for a two-way cable television system — C.B. Oakley, H.G. Schwarz (Labs, Pr) U.S. Pat. 3886454, May 27, 1975

Scanning antenna — W.C. Wilkinson, Jr. (Labs, Pr) U.S. Pat. 3887924, June 3, 1975

Energying technique for electroluminescent devices — J.J. Hanak, P.D. Southgate (Labs, Pr) U.S. Pat. 3889151, June 10, 1975

Method for depositing on a substrate a plurality of epitaxial layers in succession — M. Ettenberg (Labs, Pr) U.S. Pat. 3890194, June 17, 1975

Stabilized semiconductor devices and method of making same — W.E. Ham, D.W. Flatley (Labs, Pr) U.S. Pat. 3890632, June 17, 1975

Charge-coupled circuits — W.F. Kosonocky (Labs, Pr) U.S. Pat. 3890633, June 17, 1975

Transistor biasing arrangement — A. L. Limberg (Labs, Pr) U.S. Pat. 3891935, June 24, 1975

Deposition of epitaxial layer from the liquid phase — I. Ladany, V.M. Cannuli (Labs, Pr) U.S. Pat. 3891478, June 24, 1975

Start-up control circuit for SCR deflection — W. Bohringer (Labs, Zurich, Switzerland) U.S. Pat. 3891892, June 24, 1975

Pocketable direct current electroluminescent display device addressed by MOS or MNOS circuitry — A.G. Fischer (Labs, Pr) U.S. Pat. 3885196, May 20, 1975

Method of making a multialkali electron emissive layer — A.H. Sommer (Labs, Pr) U.S. Pat. 3884539, May 20, 1975

Self-biased complementary transistor amplifier — A.G.F. Dingwall (SSTC, Pr) U.S. Pat. 38886464, May 27, 1975

Method of shaping semiconductor workpiece — J.P. White, P.J. Delpriore (SSTC, Pr) U.S. Pat. 3888053, June 10, 1975

Method of making a compact guard-banded MOS integrated circuit device using framelike diffusion-masking structures — A.G.F. Dingwall (SSTC, Pr) U.S. Pat. 3888706, June 10, 1975

Impatt diode — H. Huang (Labs, Pr) U.S. Pat. 3890630, June 17, 1975

Solid State Division

Temperature sensing circuit — H.A. Wittlinger (SSD, Som.) U.S. Pat. 3882728, May 13, 1975

Fabrication of liquid crystal devices — H. Sorkin (SSD, Som.) U.S. Pat. 3885860, May 27, 1975

Bias circuitry for stacked transistor power amplifier stages — C.F. Wheatley, Jr. (SSD, Som.) U.S. Pat. 3886466, May 27, 1975

Semiconductor package having means to tune out output capacitance — D.S. Jacobson (SSD, Som.) U.S. Pat. 3886505, May 27, 1975

Current mirror — J.S. Radovsky (SSD, Som.) U.S. Pat. 3887879, June 3, 1975

Bias circuitry for stacked transistor power amplifier stages — A.J. Leidich (SSD, Som.) U.S. Pat. 3887880, June 3, 1975

Ground fault detection — H.A. Wittlinger (SSD, Som.) U.S. Pat. 3891895, June 24, 1975

Transistor series amplifier — O.H. Schade, Jr. (SSD, Som.) U.S. Pat. 3887878, June 3, 1975

Photographic method for printing viewing-screen structure including treatment of exposed coating with ammonium compound — R.S. Baker (SSD Lanc.) Pat. 3887371, June 3, 1975

Global Communications, Inc.

Method for conditioning transmission lines utilizing adjustable equalizers and a recording technique — J.K. Unger (Global, NY) U.S. Pat. 3883703, May 13, 1975

Communications Systems Division

Redundant signal processing error reduction technique — C.R. Thompson, R.J. Flint (CCSD, Cam.) U.S. Pat. 3883891, May 13, 1975

Short circuit protection apparatus for a regulated power supply — H.G. Seer, Jr. (CCSD, Cam.) U.S. Pat. 3886410, May 27, 1975

Consumer Electronics

Fail-safe high voltage protection circuit — R.E. Fernsler (CE, Indpls.) U.S. Pat. 3885201, May 20, 1975

On-off system for television receivers — W.W. Evans, D.W. Christensen (CE, Indpls.) U.S. Pat. 3886307, May 27, 1975

VBE voltage source temperature compensation network — S.A. Steckler (CE, Som.) U.S. Pat. 3886435, May 27, 1975

Apparatus for inhibiting a plurality of records from being disposed on a turntable — L.A. Torrington, F.R. Stave (CE, Indpls.) U.S. Pat. 3888493, June 10, 1975

High voltage protection circuit — J. Stark, Jr. (CE, Indpls.) U.S. Pat. 3891891, June 24, 1975

Picture Tube Division

Hermetic seal and method — D.L. Thoman (PTD, Lanc.) U.S. Pat. 3884007, May 20, 1975

Cathode ray tube having a luminescent screen including a two component white-emitting phosphoric mixture — L. Wootner (PTD, Marion) U.S. Pat. 3891886, June 24, 1975

Missile and Surface Radar Division

Pulse position discriminator — R.E. Wilson (MSRD, Mrstn) U.S. Pat. 3886460, May 27, 1975

Equipose mechanism — W.A. Harmening (MSRD, Mrsnt) U.S. Pat. 3889551, June 17, 1975

Non-coherent multi-channel optical spectrum analyzer — P.J. Donald, G.W. Hunka, J.J. Rudnick (MSRD, Mrstn) U.S. Pat. 3883803, May 13, 1975

Avionics Systems Division

Correlator and control system for vehicular collision avoidance — R.B. Goyer (ASD, Van Nuys) U.S. Pat. 3887916, June 3, 1975

Raster-scan display system having improved means for reading out stored game-score information — W.L. Ross (ASD, Vay Nuys) U.S. Pat. 3889253, June 10, 1975

Analog echoprotection circuit for DME — E.H. Griffin (ASD, Van Nuys) U.S. Pat. 3889260, June 10, 1975

Dates and Deadlines



As an industry leader, RCA must be well represented in major professional conferences . . . to display its skills and abilities to both commercial and government interests.

How can you and your manager, leader, or chief-engineer do this for RCA?

Plan ahead! Watch these columns every issue for advance notices of upcoming meetings and "calls for papers". Formulate plans at staff meetings—and select pertinent topics to represent you and your group professionally. Every engineer and scientist is urged to scan these columns; call attention of important meetings to your Technical Publications Administrator (TPA) or your manager. Always work closely with your TPA who can help with scheduling and supplement contacts between engineers and professional societies. Inform your TPA whenever you present or publish a paper. These professional accomplishments will be cited in the "Pen and Podium" section of the *RCA Engineer*, as reported by your TPA.

Calls for papers

—be sure deadlines are met

Ed. Note: Calls are listed chronologically by meeting date. Listed after the meeting title (in bold type) are the sponsor(s), the location, and deadline information for submittals.

DEC. 1-3, 1975 — **1975 IEEE Int'l Electron Devices Meeting (IEEE)** Washington Hilton Hotel, Washington, D.C. **Deadline info:** (abst) 8-4-75 to Dr. C. Neil Berglund, 1975 IEDM Technical Program Chairman, Bell-Northern Research Ltd., POB 3511, Station C, Ottawa, Canada K1 Y 4H7.

DEC. 9-12, 1975 — **Magnetism & Magnetic Materials Conference (MAG, AIR et al)** Benjamin Franklin Hotel, Phila., Pa. **Deadline info:** (abst) 8-15-75 to B. Stein, Univac Div., Sperry Rand, POB 500, Blue Bell, 19422

JAN. 25-30, 1976 — **1976 IEEE Power Engineering Society Winter Meeting (IEEE)** Statler Hilton Hotel, New York, N.Y. **Deadline info:** Immediately request an author's kit from the Technical Conference Svcs Ofc at IEEE Hdqtrs., 345 E. 47th St., New York, N.Y. 10017; (ms) 9-1-75 to IEEE Hdqtrs.

FEB. 18-20, 1976 — **IEEE International Solid-State Circuits Conference (IEEE SSCC, IEEE Phila. Section, Univ. of Pennsylvania)** Sheraton Hotel, Phila., Pa.

Deadline info: (abst) 10-1-75 to D. Koehler, Bell Laboratories /Room 2A131, 600 Mountain Ave., Murray Hill, N.J. 07974

APR. 12-14, 1976 — **Acoustics, Speech and Signal Processing Int'l Conference (ASSP, Phila. Section)** Marriott Hotel, Phila., Pa. **Deadline info:** (abst) 10-1-75 to Thomas Martin, Threshold Tech. Inc., Rt. 130 Union Landing Rd., Cinnaminson, N.J. 08077

APR. 27-29, 1976 — **Circuits and Systems Int'l Symposium (CAS, FDE, (NTG))** Tech. Univ., Munich, Germany. **Deadline info:** (ms.) 10-15-75 Alfred Fettweis, Lehrstuhl für Nachrichtentechnik, Univ. of Bochum, Postfach 2148, D-4630 Bochum, F.R. Germany

JUNE 1976 — **Microwave Field-Effect Transistors (IEEE Transactions on Microwave Theory and Techniques)** **Deadline info:** (3 copies of Ms.) 10-1-75 to C.A. Liechti, Hewlett-Packard Company, Solid-State Laboratory, 1501 Page Mill Road, Palo Alto, CA 94304

JUNE 14-16, 1976 — **International Conference on Communications (COMM)** Marriott Motor Hotel, Phila., Pa. **Deadline info:** 2-1-76 to Ralph Wyndrum, Bell Labs., Whippany Rd., 1B306, Whippany, N.J. 07981

JUNE 21-24, 1976 — **1976 International Symposium on Information Theory (IEEE)** Ronneby Brunn, Ronneby, Sweden. **Deadline info:** 11-15-75 to Jack Salz, Bell Laboratories, Room 1G-509, Holmdel, N.J. 07733

JULY 18-23, 1976 — **Power Engineering Society Summer Meeting (PE)** Portland Hilton Hotel, Portland, Oregon. **Deadline info:** 2-1-76 to W.S. Greer, Westinghouse Elec. Corp., 1414 N.E. Grand Ave., Portland, Ore. 97212

AUG. 25-27, 1976 — **Product Liability Prevention Conference (R et al)** Newark College of Engineering, Newark, N.J. **Deadline info:** 11-1-75 to John Mihalasky, Newark College of Engr., 323 High St., Newark, N.J. 07102

SEPT. 26-29, 1976 — **14th Biennial Mechanisms Conference (The American Society of Mechanical Engineers)** Sheraton-Mt. Royal Hotel, Montreal, Quebec. **Deadline info:** (Ms.) 3-31-76 to Dr. Frederick R. Tepper, U.S. Army Picatinny Arsenal, Fuze Development Branch, Bldg. 62-H, Dover, N.J. 07801

SEPT. 26-30, 1976 — **1976 ASME Design Technology Transfer Conference (The American Society of Mechanical Engineers)** Montreal, Canada. **Deadline info:** (Ms. & 3 copies) 4-1-76 to Professor A.H. Soni, School of Mechanical and Aerospace Engineering, Oklahoma State University, Stillwater, OK

DEC. 6-10, 1976 — **Submillimeter Waves and Their Applications (MTT, OSA et al)** San Juan, Puerto Rico. **Deadline info:** (Ms.) 8-1-76 to K.J. Button, MIT, National Magnet Lab., Cambridge, MA 02139

Dates of upcoming meetings

—plan ahead

Ed. Note: Meetings are listed chronologically. Listed after the meeting title (in bold type) are the sponsor(s), the location, and the person to contact for more information.

AUG. 17-22, 1975 — **Intersociety Energy Conversion Engineering Conference** (ED, AES, et al) Univ. of Delaware, Newark, Del. **Prog info:** D.S. Goldin, TRW Syst. Group, 1 Space Park, Redondo Beach, CA 90278

AUG. 20-22, 1975 — **Product Liability Prevention Conference** (R, et al) Newark College of Engineering, Newark, N.J. **Prog info:** R.M. Jacobs, Newark College of Engineering, 323 High St., Newark, N.J. 07102

SEPT. 2-5, 1975 — **European Solid State Circuits Conference** (IEE, IEEEE UKRI Section et al) Univ. of Kent, Canterbury, UK. **Prog. info:** IEE, Conference Dept., Savoy Pl., London W.C. 2 R OBL England

SEPT. 3-5, 1975 — **Computer Hardware Description Language & Their Applications** (C, ACM et al) City Univ. of New York, New York, N.Y. **Prog. info:** S.Y.H. Su, EE Dept., City College of CUNY, New York, N.Y. 10031

SEPT. 9-11, 1975 — **COMPCON FALL** (C) Mayflower Hotel, Washington, D.C. **Prog:** R.E. Merwin, BMDPO, 1300 Wilson Blvd., Arlington, Va. 22209

SEPT. 9-11, 1975 — **Hybrid Technology** (IERE, IEEE UKRI Section, IEE et al) Univ. of Tech., Loughborough, U.K. **Prog info:** IERE, 8-9 Bedford Sq., London W.C. 1 B 3 RG England

SEPT. 11-12, 1975 — **Software Engineering** (C, NBS) Mayflower Hotel, Washington, D.C. **Prog info:** Harlan Mills, IBM Corp., 18100 Frederick Pike, Gaithersburg, Md. 20760

SEPT. 14-19, 1975 — **Environmental Sensing & Assessment Int'l Conf.** (EQC, Univ. of Nev., et al) Stardust, Las Vegas, Nevada. **Prog info:** D.S. Barth, Environmental Protection Agency, POB 15027, Las Vegas, Nev. 89114

SEPT. 16-19, 1975 — **Optical Fiber Communication Int'l Conference** (IEE, IEEE UKRI Section, Inst. of Physics, IERE) IEE, London, England. **Prog info:** IEE, Savoy Place, London WC2R OBL England

SEPT. 20-24, 1975 — **Engineering in Medicine & Biology Conference** (EMB, AEMB) Fairmont Roosevelt Hotel, New Orleans, La. **Prog info:** AEMB, Suite 1350, 545 Wisconsin Ave., Chevy Chase, Md. 20015

SEPT. 22-24, 1975 — **Int'l Congress on Instrumentation in Aerospace Simulation** (AES) Canadian Gov't Conf. Ctr. **Prog info:** E.S. Hanff, Nat'l Research Council of Canada, Montreal Rd., Ottawa, Ontario, Canada K1A 0R6

SEPT. 22-24, 1975 — **Engineering in the Ocean Environment OCEAN 75** (IEEE) Oceanography Coord. Comm., MTS) **Prog info:** C.B. Bishop, Marine Physical Lab., SIO/UCSD, San Diego, Calif. 92132

SEPT. 22-24, 1975 — **1975 Joint Fall Meeting Basic Science and Electronics Divisions** (American Ceramic Society, Inc.) Indianapolis Hilton, Indianapolis, Ind. **Prog info:** Basic Science Div.-Dr. Kenneth W. Lay, General Electric R&D Center, Box 8, Schenectady, N.Y. 12301; Electronics Div.-Dr. Thomas G. Reynolds III, Ferroxcube Corp., Box 359, Saugerties, N.Y. 12477

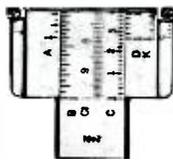
SEPT. 22-24, 1975 — **Ultrasonics Symposium** (SU) Los Angeles Hilton Hotel, Los Angeles, Calif. **Prog info:** R. Stern, Mechanics Structures Dept., Sch. of Engrg. & Applied Sci., Univ. of Calif., Los Angeles, CA 96024

SEPT. 23-25, 1975 — **Instrumentation in Oceanography** (IERE, IEEE UKRI Section et al) Univ. College of North Wales, Bangor, Wales. **Prog info:** IERE, 8-9 Bedford Sq., London WC 1 B 3RD UK

SEPT. 23-25, 1975 — **Material Handling Conference** (IA et al) Cleveland Expos. Ctr., Cleveland, Ohio. **Prog info:** F.A. Stevens, Bituminous Coal Res. Inc., 350 Hochberg Rd., Monroeville, PA 15146

SEPT. 23-25, 1975 — **Cybernetics and Society Int'l Conference** (SMC) Hyatt Regency Hotel, San Francisco, Calif. **Prog info:** L.S. Coles, Artificial Intelligence Ctr., SRI, Menlo Park, CA 94025

SEPT. 25-26, 1975 — **Broadcast Symposium** (B) Washington, D.C. **Prog info:** The Institute of Electrical and Electronics Engineers, Inc., Office of Technical Activities Board, 345 East 47th St., New York, N.Y. 10017



Engineering

News and Highlights



Firestone named Division V.P. Avionics Systems

Andrew F. Inglis, Division Vice President and General Manager, RCA Commercial Communications Systems Division has announced the appointment of **Dr. William L. Firestone** as Division Vice President, RCA Avionics Systems.

Dr. Firestone was previously a Corporate Vice President with the General Instru-

ment Corporation in New York.

Dr. Firestone will direct a program, announced earlier this year, to strengthen and expand RCA's position as an important supplier of avionics to the airline, general aviation, and military aviation markets. The program calls for a stepped-up schedule of development engineering to keep RCA in the forefront of avionics technology, and for a new product line, Mr. Inglis said. The first two products in the new PRIMUS line — a 300-nautical-mile range weather radar and a distance measuring equipment (DME) — were introduced last month.

In announcing the new management, Mr. Inglis said **John P. Mollema**, Director of Marketing for RCA Avionics Systems, will hold a key position in the organization and his duties will be broadened to include strategic business planning in addition to his world-wide executive responsibility for sales.

Mr. Mollema has an extensive background in avionics and has held the top RCA Avionics marketing post since 1970. He joined the company in 1965 and first served as Manager of the Wichita, Kansas, field office for sales and service. Before moving up to marketing director he was Manager of General Aviation Sales for all of North America.

Dr. Firestone, during his service with General Instrument, also was President of its Jerrold Electronics Corp. subsidiary; Vice President and Group Executive, Entertainment Group; and Vice President and Division Manager, F. W. Sickles Division.

Earlier, he was with the Whittaker Corporation as a Vice President and Group Executive, Aerospace Group, and previously was Vice President and General Manager for two divisions of Hallicrafters Corporation.

He was with Motorola Inc. earlier in his career and held the posts of Director of Engineering, Communications Division, and Assistant General Manager, Military Electronics Division.

Dr. Firestone earned the BS in engineering at University of Colorado; MSEE at the Illinois Institute of Technology, and the PhD at Northwestern University.

He is a private pilot, has been issued nine patents in the electronics field, and has published a number of technical papers. He is a member of the IEEE, Electronic Industries Association, the American Management Association, the American Institute of Management and several other professional organizations.



Pritchard named Fellow of RCA Laboratories Staff

Dalton H. Pritchard has been named a Fellow of the Technical Staff of RCA Laboratories for his many contributions to the development of color television.

The Fellow designation is comparable to the same title used by universities and technical societies. It is given by RCA in

recognition of a record of sustained technical contributions in the past and of anticipated continuing technical contributions in the future.

Mr. Pritchard received the BSEE from Mississippi State University in 1943. After graduation, he entered the U.S. Army Signal Corps and received a year of specialized radar training at Harvard University and MIT

During World War II, he served in the Asiatic-Pacific Theater, rose to the rank of Captain, and was awarded the Bronze Star Medal.

Mr. Pritchard joined RCA Laboratories at Riverhead, New York, in 1946 and transferred to Princeton in 1950. He has received eight RCA Laboratories Outstanding Achievement Awards for his research in various aspects of color television, including receivers, cameras and recording.

Mr. Pritchard has received more than 30 U.S. Patents and has published numerous technical papers. He is a Senior Member of the Institute of Electrical and Electronics Engineers, and a Member of the Society of Information Display, Sigma Xi, Tau Beta Pi and Kappa Mu Epsilon.



Kaufman elected Fellow of ASM

Jerome W. Kaufman, Metallurgist, Central Engineering, Government Communications and Automated Systems Division, Camden, N.J., has been elected a Fellow of the American Society of Metals. The honor will be conferred at the annual meeting of the ASM in Cincinnati in November of 1975.

Mr. Kaufman acts for RCA as the Sustaining Member Representative in the American Society for Metals. He is an authority on joining and metals utilization. His academic background includes the BS in Metallurgical Engineering from Lehigh University in 1949, satisfactory completion of major graduate course work in Metallurgy at the University of Pennsylvania, graduate of course at Penn State University Ogontz Center in Solid State Electronics, and graduate of RCA course in Value Engineering. He has obtained professional engineer licenses in Pennsylvania and New Jersey. Among other activities at RCA he is the metallurgical engineering consultant for the antenna tower for the World Trade Center and for the communications towers for the Alaska Pipe Line.

Prior to joining RCA Mr. Kaufman was the metallurgical engineer at the U.S. Naval Air Development Center where he received the Navy's Meritorious Award for his original development of pre-stressing of bomb hooks.

Law receives Darne Award

Dr. Harold B. Law, Director, Materials and Display Device Laboratory, at the DSRC, received the 1975 Frances Rice Darne Memorial Award from the Society for Information Display at the recent SID International Symposium in Washington, D.C.

Dr. Law was cited for "outstanding contributions to color picture tube development resulting in practical color television."

Licensed engineers

When you receive a professional license, send your name, PE number (and state in which registered), RCA division, location, and telephone number to: *RCA Engineer*, Bldg. 204-2, RCA, Cherry Hill, N.J. New Listings (and corrections or changes to previous listings) will be published in each issue.

Commercial Communications Systems Division

Douglas J.H. Frank, Gibbsboro, N.J.; NJ-22147, New Jersey.

Service Company

John A. Williams, Fredriksted, U.S. Virgin Islands; PE-325E, U.S. Virgin Islands; PE-2464, New Hampshire.



Promotions

Astro-Electronics Division

C.A. Berard from Engineer to Manager (Speciality) Engineering (A. Aukstikalnis, Hightstown)

Missile and Surface Radar Division

J.V. Amatrudi from Tech. Opns. Anal. to Admr. Logistics (T. Stecki, Moorestown)

R. Wood from Sr. Mbr. Engrg. Staff to Ldr., Eng. Sys. Proj. (H. Boardman, Moorestown)



Rogers receives Alumni Award

Edward S. Rogers, Communications Research Laboratory, and his wife, the former Blanche Forney, were honored recently by the Susquehanna University Alumni Association. Mr. and Mrs. Rogers were awarded bronze medals as joint recipients of the association's 1975 Service Award. The Rogers are both members of Susquehanna's class of 1942.

The Rogers' work in support of Susquehanna University has included hosting parties for freshmen in their home, helping with telethons, recruiting students, and holding office on alumni association and university boards and committees.

Thomas is Manager Engineering Documentation and Standards

William W. Thomas has been appointed Manager, Engineering Documentation and Standards, for Government and Commercial Systems, Moorestown, N.J. Mr. Thomas will report to **Dr. Harry J. Woll**, Division Vice President, Government Engineering.

Mr. Thomas joined RCA in 1959 as Administrator, Drafting Coordination, for the Missile and Surface Radar Division. He moved to the G&CS organization in 1961 and has held several engineering management positions. He represents G&CS on a number of technical and professional society committees, and serves on Department of Defense and industrial groups.

A University of Pennsylvania graduate in aeronautical engineering, Mr. Thomas worked for the Glenn L. Martin Company, Vertol Aircraft Corporation and Lockheed Aircraft Corporation before joining RCA.

He was awarded the Robert H. Stearns' Memorial Award for National Leadership in Engineering Documentation and the American Ordnance Association's Bronze Medallion.



Wells elected Fellow of AES

Joseph F. Wells, Manager of Electronic Recording Development, RCA Records, Indianapolis, Ind., has been elected a Fellow of the Audio Engineering Society. Mr. Wells, who is also the Technical Publications Administrator for RCA

Professional Activities

Laboratories

Paul Brown, Mgr., Technical Relations, and **Lowell Good**, Coordinator, Technical Relations, have been commended by the faculty of the College of Engineering, Rutgers University, for their participation through exhibits and demonstrations at the Rutgers Engineering Open House through the past three years.

Liston Abbott, of the Communications Research Laboratory has received a 1975 Council of Community Services Award. The Council, a Princeton area United Fund agency, honored Mr. Abbott for his work with the Hightstown Human Relations Council, the Community Action Council, and the Better Beginnings Day Care Center.

Newly elected IEEE Princeton Section officers for 1975-76 include: Chairman, **Robert F. Sanford**, Process and Applied Materials Research Laboratory; Vice Chairman, **Lubomyr S. Onyshkevych**, Systems Research Laboratory; and Secretary-Treasurer, **Jules D. Levine**, Materials Research Laboratory.

Government and Commercial Systems

William W. Thomas, Government Engineering, G&CS, chaired a meeting of an *ad hoc* industry committee and government representatives in a successful effort to eliminate several cost-inducing features of a proposed revision to specification MIL-D-1000 on the acquisi-

tion of engineering drawings.

Records, received the BSEE from Duke University in 1949. He also attended the technological Institute, Northwestern University.

Upon graduation, Mr. Wells was employed by RCA Records as a maintenance engineer and later as a recording engineer. In 1958, he was appointed Manager, Recording—Chicago. Mr. Wells was instrumental in founding Midwest Section, AES and served as Central Vice President in 1966. He also assisted in establishing Chicago Section, National Academy of Recording Arts and Sciences and served as Chapter President and national trustee.

In 1972, Mr. Wells was appointed Manager, Electronic and Recording Development in Indianapolis, and is responsible for electronic and magnetic development for RCA's recording studios, record and recorded tape manufacturing operations.

He is a member of Tau Beta Pi, and has served on panel 6 of National Quadraphonic Radio Committee and is a member of Electronic Industries Association Panel P8.2.

tion of engineering drawings.

The Electronic Industries Association was represented by **H.R. Ketcham** of GCASD — Camden.

Max Lehrer, Division Vice President, Missile and Surface Radar Division, Moorestown, N.J., was elected President of the Philadelphia Chapter of the National Security Industrial Association. **Joseph G. Mullen**, Manager, Customer and Marketing Relations, Government and Commercial Systems, Moorestown, N.J. is a member of the Chapter's Executive Committee.

Missile and Surface Radar Division

Harold G. Behl of the AEGIS Project Management Office and **Walter Harris** of GCASD in Camden have been elected to the Council of the AIAA — Greater Philadelphia Chapter.

Staff Announcements

Government and Commercial Systems

I.K. Kessler, Executive Vice President, Government and Commercial Systems has announced the following appointments: **Kassel K. Miller** as Director, Kish Island (Iran) Telecommunications Program and **James Vollmer** as Division Vice President and General Manager, Palm Beach Division.

David Shore, Division Vice President, Advanced Programs Development, RCA Government and Commercial Systems has announced the appointment of **Peter B. Korda** as Manager, Position Locating Programs Operations.

RCA Global Communications, Inc.

John Christopher, Director, Spacecraft Engineering and Production has announced the organization as follows: **Charles Lundstedt**, Manager, TTC and Mission Operations; **Peter Plush**, Manager, Launch Vehicle Procurement; and **John Christopher**, Acting, Spacecraft Engineering.

Picture Tube Division

Wellesley J. Dodds, Manager, Quality and Reliability Assurance has announced the organization as follows: **Sherman L. Babcock**, Administrator, Quality Control Engineering and **Rex E. McNickle**, Manager, Quality and Reliability Assurance Systems.

RCA Service Company

Julius Koppelman, President, RCA Service Company has announced the following appointments: **Alfred W. Pedrick**, Division Vice President, Materials and Support Services and **Sigmund Schotz**, Division Vice President, Consumer Affairs.

Solid State Division

Robert A. Donnelly, Manager, Findlay Operations Support has announced the organization of Materials and Stem Manufacturing as follows: **Ted L. Hauman**, Manager, Materials and Stem Manufacturing; **Bruce M. McVey**, Manager, Production and Material Control; **James D. Reynolds**, Superintendent, Stem Manufacturing; **Gary A. Roser**, Administrator, Materials Coordination and Services; **Robert B. Sullivan**, Leader, Stem Engineering; and **Gene H. Wyckoff**, Manager, Purchasing.

Robert P. Jones, Manager, Manufacturing — COS/MOS has announced the appointment of **Richard E. Davey** as Manager, Manufacturing — MOS High Reliability.

Richard E. Davey, Manager, Manufacturing — MOS High Reliability has announced the following appointments: **John W. Young** as Manager, MOS High Reliability Manufacturing Administration and **John D. Young** as Leader, MOS High Reliability Engineering.

Philip R. Thomas, Division Vice President, Solid State MOS Integrated Circuits has announced the appointment of **Robert D.**

Wright as Director, Microprocessor Products.

Robert D. Wright, Director, Microprocessor Products has announced the organization as follows: **Donald R. Carley**, Manager, Applications Engineering - Microprocessors; **Robert O. Winder**, Manager, Design Engineering - Microprocessors; and **Robert D. Wright**, Acting Manager, Market Planning - Microprocessors.

Jacques M. Assour, Manager, Design Engineering - Thyristors & Rectifiers has announced the appointment of **Patricia A. Roman** as Leader, Type Engineering - Thyristors.

Dale M. Baugher, Director, Thyristor & Rectifier Products has announced the organization of Manufacturing & Operations Planning as follows: **Daniel J. Smith**, Manager, Manufacturing & Operations Planning and **Charles E. Farley**, Administrator, Operations Planning - Thyristors.

John E. Mainzer, Manager, Power Manufacturing Operations has announced the organization as follows: **James A. Amick**, Manager, Materials & Process Development; **Edward A. Czeck**, Manager, Wafer Fabrication; **Henry A. Kellar**, Manager, Device Fabrication; and **David A. Riggs**, Manager, Materials & Operations Control.

James C. Miller, Director, Power Transistor Products has announced the appointment of **Louis V. Zampetti** as Manager, Type Engineering— Power Transistors.

Technical Excellence Team Award winners (standing, left to right) Barry Altschuler, Ken McGuire and Kal Prost, with Dan Hampel, who succeeded Dr. Wen Yuan Pan (seated) as Manager of the Advanced Communications Laboratory in Somerville. Dr. Pan retired July 1.



Awards

Government Communications and Automated Systems Division — Camden

Barry Altschuler, Dick Blasco (who has left RCA), Ken McGuire, and Kal Prost of the Advanced Communications Laboratory in Somerville received a Technical Excellence Team Award for their design of a custom CMOS/SOS multiplier-accumulator chip. This chip is a key building block for a real time programmable adaptive array now being developed.

Hampel named Manager, Advanced Communications Laboratory

Daniel Hampel has been appointed Manager, Advanced Communications Laboratory, RCA Government Communications and Automated Systems Division, Camden, N.J. He replaces **Dr. W.Y. Pan**, who retired recently.

In his new position, Mr. Hampel is responsible for providing new solid state circuit technology for government communications systems.

Prior to his appointment, Mr. Hampel was Leader, Advanced Digital Techniques at the Advanced Communications Laboratories, which is located in Somerville, N.J. He has been with RCA since 1960.

Before joining the company, Mr. Hampel worked for ITT and the Bell Telephone Laboratories.

Mr. Hampel earned the BSEE and MSEE from Newark College of Engineering. He is a senior member of the IEEE, a member of the Communications Society and has authored several technical papers.

1975 David Sarnoff Awards for Outstanding Technical Achievement presented



In recognition of his many outstanding technical contributions enhancing RCA's reputation as a leading supplier of television systems: Arch Luther (center) of Broadcast Systems with Mr. Sarnoff and Dr. Hillier.



For outstanding contributions in the development of a multifunction tactical phased array radar system: Mr. Sarnoff (left) and Dr. Hillier (right) congratulate the Missile and Surface Radar Division team of (left to right) George Stevens, Tom Mehling, Dick Baugh, and Bill Patton.



For outstanding achievement in the development and practical implementation of a high-contrast phosphor television screen: Mr. Sarnoff (left) presenting an Award medal to Theodore Saulnier of the Picture Tube Division and fellow team members Stephen Trond of the Picture Tube Division (center) and Steven Lipp of RCA Laboratories. Dr. Hillier (right) adds his congratulations.



For excellence in the design and development of a hand-held, two-way portable radio: Mr. Sarnoff (left) and Dr. Hillier (right) congratulate (from left to right) Lee Crowley, Bill Autry, and Andy Missenda of Commercial Communications Systems Division, and Heshmat Khajezadeh of Solid State Division.

Degrees Granted

Record Division

Richard M. Petroski of Operations Engineering at Indianapolis, Ind., received the MS with a major in Industrial Operations from Purdue University.

Solid State Division

John G. Martin of Power Devices Engineering at Somerville, N.J., received the BS in Chemical Engineering from

Newark College of Engineering.

Missile and Surface Radar Division

John R. McClernan of MSRD Administration at Moorestown received the BS in Business Administration (Management) from Drexel University.

John P. Montemurro of Engineering Operations at Moorestown received the BA in Industrial Arts Education from Glassboro State College.

George Suhy of Command and Controls Engineering received the MS in Systems Engineering from the University of Pennsylvania.

Laboratories

Richard J. Hollingsworth of Integrated Circuit Technology in Somerville received the MS in Electrical Engineering from the University of Pennsylvania.

Herzog honored by American Helicopter Society

Donald Herzog, Engineering Leader, Advanced Technology Laboratories, Camden, N.J., was a member of the industry team that recently received the Grover E. Bell Award from the American Helicopter Society.

The award was in recognition of the Flight Control System Development for the U.S. Army's Heavy Lift Helicopter. RCA developed the Precision Hover Sensor (PHS) for the program. The PHS is a unique electronic sensor that helps the helicopter's flight control system to maintain the craft's precise position as it hovers. RCA developed the system for the Vertol Division of the Boeing Company which designed and built the helicopter.

GCASD — Burlington Annual Professional Recognition Dinner

Burlington Operations of Government Communications and Automated Systems Division held its eighth Professional Recognition Dinner to honor 55 engineers for their professional accomplishments. These achievements include papers published, patents filed or awarded, professional committee memberships, and Engineering Excellence Awards.

At the dinner, **E.M. Stockton**, Chief Engineer of Burlington Operations, who hosted the affair, congratulated the group for their dedication. He mentioned that last year he gave out a challenge for each of the individuals being recognized to encourage a peer to write a paper, a disclosure, or participate in any of the other activities. In 1973 there was a total of 23 authors and patent filings, in 1974 the number went to 42. He also cited some numbers showing how RCA Burlington was well ahead of other Divisions on disclosures, filings and papers on a per-capita basis.

Mr. Stockton also talked about the relationship between technical papers and patents and bookings. He felt the image and technical competence displayed by technical papers, for example, did much to strengthen RCA's marketing position.

The challenge that he presented for the next year is to see professional activities such as papers, disclosures, and technical committee leadership in new areas of technology of vital business interest to GCASD and RCA.

Guests included **Dr. Harry J. Woll**, Division Vice President, Government Engineering; **James M. Osborne**, Division Vice President, Government Communications and Automated Systems Division; **Dr. James Hillier**, Executive Vice President, Research and Engineering; **Howard Rosenthal**, Staff Vice President, Engineering; **Dr. William J. Underwood**, Director, Engineering Professional Programs; and **John V. Regan**, Staff Vice President, Patent Operations.

Clip out and mail to Editor, *RCA Engineer*, 204-2, Cherry Hill, N.J.

RCA Engineer

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New Editorial Representatives

Editorial Representatives are responsible for planning and processing articles for the *RCA Engineer* and for working with the Technical Publications Administrators in their Divisions to support the corporate-

wide technical papers and reports program. A complete listing of Technical Publications Administrators and Editorial Representatives is provided on the inside back cover of each *RCA Engineer* issue.



Ketcham appointed Ed Rep for GCASD — Camden

Anthony Liquori, Technical Publications Administrator, Government Communications and Automated Systems Division, Camden, N.J., has announced the appointment of **H.R. Ketcham** *RCA Engineer* Editorial Representative for GCASD in Camden, N.J.

Mr. Ketcham received the BS in Economics from the University of Pennsylvania and the MBA from Drexel University. He is currently a Documentation and Configuration Management Specialist for GCASD. He is also responsible for coordination and publication standards used by RCA divisions engaged in government contract work. He also represents RCA on the Electronic Industry Association (EIA) G-33 committee. Mr. Ketcham's prior RCA experience includes such engineering support functions as material breakdown and ordering, technical manual preparation, engineering stockrooms, test equipment maintenance and calibration, and an engineering library.



Ronan is Ed Rep for SSD Mountaintop

Eleanor McElwee, Technical Publications Administrator for Solid State Division in Somerville, N.J., has announced the appointment of **Harold Ronan** as *RCA Engineer* Editorial Representative for SSD's Mountaintop plant.

Mr. Ronan received the BSME from MIT in 1952 and the MSEE from Newark College of Engineering in 1960. He is presently a Senior Member of the Technical Staff in Electrical Equipment Technology at Mountaintop. Since joining SSD in Somerville in 1959, Mr. Ronan has been engaged in manufacturing test equipment design for all of SSD's product lines. In 1971, he transferred to the division's semiconductor manufacturing facility at Mountaintop where he has worked primarily with SCOPE computer-controlled testing systems. Mr. Ronan has been responsible for significant advances in thyristor high voltage testing, rectifier switching time measurements, and transistor breakdown and gain circuitry.

Editorial Representatives

The Editorial Representative in your group is the one you should contact in scheduling technical papers and announcements of your professional activities.

Government and Commercial Systems

Astro-Electronics Division I. M. SEIDEMAN* Engineering, Princeton, N.J.

**Commercial Communications
Systems Division**
Broadcast Systems

W.S. SEPICH* Broadcast Systems Engineering Camden, N.J.
R. E. WINN Broadcast Systems Antenna Equip. Eng., Gibbsboro, N.J.
A. C. BILLIE Broadcast Engineering, Meadowlands, Pa.
F. A. BARTON* Advanced Development, Meadowlands, Pa.

Mobile Communications Systems

Avionics Systems

C. S. METCHETTE* Engineering, Van Nuys, Calif.
J. McDONOUGH Equipment Engineering, Van Nuys, Calif.

**Government Communications and
Automated Systems Division**

A. LIGUORI* Engineering, Camden, N.J.
H.R. KETCHAM Engineering, Camden, N.J.
K. E. PALM* Engineering, Burlington, Mass.
A.J. SKAVICUS Engineering, Burlington, Mass.

Government Engineering

M. G. PIETZ* Advanced Technology Laboratories, Camden, N.J.
J. E. FRIEDMAN Advanced Technology Laboratories, Camden, N.J.

Missile and Surface Radar Division

D. R. HIGGS* Engineering, Moorestown, N.J.

Palm Beach Division

B. B. BALLARD* Palm Beach Gardens, Fla.

Research and Engineering

Laboratories

C. W. SALL* Research, Princeton, N.J.
A. L. STRADER Solid State Technology Centers, Somerville, N.J.

Solid State Division

E.M. McELWEE* Engineering Publications, Somerville, N.J.
J.E. SCHOEN Engineering Publications, Somerville, N.J.
H.R. RONAN Power Devices, Mountaintop, Pa.
S. SILVERSTEIN Power Transistors, Somerville, N.J.
A.J. BIANCULLI Integrated Circuits and Special Devices, Somerville, N.J.
J.D. YOUNG IC Manufacturing, Findlay, Ohio
R. W. ENGSTROM Electro-Optics and Devices, Lancaster, Pa.

Consumer Electronics

C. W. HOYT* Engineering, Indianapolis, Ind.
R. BUTH Engineering, Indianapolis, Ind.
P. CROOKSHANKS Television Engineering, Indianapolis, Ind.
F. HOLT Advanced Products, Indianapolis, Ind.
J. OLIVER Consumer Electronics, Indianapolis, Ind.

RCA Service Company

M. G. GANDER* Consumer Services Administration, Cherry Hill, N.J.
J. E. STEOGER Consumer Services Engineering, Cherry Hill, N.J.
R. MacWILLIAMS Marketing Services, Government Services Division, Cherry Hill, N.J.
R. DOMBROSKY, Technical Support, Cherry Hill, N.J.

Distributor and Special Products Division

C. C. REARICK* Product Development Engineering, Deptford, N.J.
J. KOFF Receiving Tube Operations, Woodbridge, N.J.

Picture Tube Division

C. A. MEYER* Commercial Engineering, Harrison, N.J.
J. H. LIPSCOMBE Television Picture Tube Operations, Marion, Ind.
E.K. MADENFORD Engineering, Lancaster, Pa.

RCA Global Communications Inc.

W. S. LEIS* RCA Global Communications, Inc., New York, N.Y.
P. WEST* RCA Alaska Communications, Inc., Anchorage, Alaska

NBC, Inc

W. A. HOWARD* Staff Eng., Technical Development, New York, N.Y.

RCA Records

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Corporate Development

C. A. PASSAVANT* International Planning, New York, N.Y.

RCA Ltd

W. A. CHISHOLM* Research & Eng. Montreal, Canada

Patent Operations

J. S. TRIPOLI Patent Plans and Services, Princeton, N.J.

Electronic Industrial Engineering

J. OVNICK* Engineering, N. Hollywood, Calif.

*Technical Publications Administrators (asterisked * above) are responsible for review and approval of papers and presentations

RCA Engineer

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