# ELFCTRONICS <br>  

## MARCH $1994 \quad £ 1.95$

## RF DESIGN

Polyphase SSB receiver

## REVIEW

CircuitMaker 1.1: worth the layout?

APPLICATIONS Bootstrapped jfet amplifiers, Driving clock lines

AUDIO
Class A ultra-low distortion amplifier
ENGINEERING
Using the Smith chart

COMPUTING
VHDL: design tool for tomorrow?

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DESICNEZRS CUIDETC
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The PC82 is the US version of the Sunshine Expro 60, and therefore can be offered at a very competitive price for a product of such high quality. The PC82 has undergone extensive testing and inspection by various major IC manufacturers and has won their professional approval and support. Many do in fact use the PC82 for their own use!

The PC82 can program E/EPROM, Serial PROM, BPROM, MPU, DSP, PLD, EPLD, PEEL, GAL, FPL, MACH, MAX, and many more. It comes with a 40 pin DIP socket capable of programming devices with 8 to 40 pins. Adding special adaptors, the PC82 can program devices up to 84 pins in DIP, PLCC, LCC, QFP, SOP and PGA packages.

The unit can also test digital ICs such as the TTL 74/54 series, CMOS $40 / 45$ series, DRAM (even SIMM/SIP modules) and SRAM. The PC82 can even check and identify unmarked devices.

Customers can write their own test vectors to program non standard devices. Furthermore it can perform functional vector testing of PLDs using the JEDEC standard test vectors created by PLD compilers such as PALASM, OPALjr, ABLE, CUPL etc. or by the user.

The PC82's hardware circuits are composed of 40 set pin-driver circuits each with TTL I/O control, D/A voltage output control, ground control, noise filter circuit control, and OSC crystal frequency control. The PC82 shares all the PC's resources such as CPU, memory, I/O hard disk, keyboard, display and power supply.

A dedicated plug in card with rugged connecting cable ensures fast transfer of data to the programmer without tying up a standard parallel or serial port. Will work in all PC compatibles from PC XT to 486.

The pull-down menus of the software makes the PC82 one of the easiest and most user-friendly programmers available. A full library of file conversion utilities is supplied as standard.

The frequent software updates provided by Sunshine enables the customer to immediately program newly released ICs. It even supports EPROMs to 16 Mbit .

Over 20 engineers are employed by Sunshine to develop new software and hardware for the PC82. Not many competitors can boast of similar support!

Citadel, a 32 year old company are the UK agents and service centre for the Sunshine range of programmers, testers and in circuit emulators and have a team of engineers trained to give local support in Europe.

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## FEATURES



## SMPS DESIGN.

 188Switchmode power circuits are more complex than their linear counterparts but the benefits they offer outweigh the extra complexity. The first of two design articles covers switching topologies and basic design considerations. By Duncan Smith.

## COMPUTING FOR REALTIME

Unlike office computers, industrial control systems need to respond to a number of stimuli simultaneously. Although standard msdos PCs are cheap, the interrupt and multitasking performance simply does not compare with an OS-9 operating system running on a 68000 series processor. By Bill Dickinson.

## THE VERSATILE WORLD OF OTAs

$\qquad$ .197
Operational transconductance amplifiers can introduce programmability into almost any conventional fixed gain circuit. Multipliers, VCAs, VCOs and voltage controlled filters are all part of the repertoire. By Dan Ayers.

POLYPHASE SSB .. 202
Of all the transmission modes for plain speech, single sideband suppressed carrier is the most spectrally efficient. Richard Hosking presents a design study based on the polyphase RC network, the heart of a simple SSB receiving system which may used reciprocally for transmission.

## RF TRANSISTORS.

 218How to optimise printed circuit board construction and transistor mounting techniques with a view to long term reliability. By Norm Dye and Helge Granberg.

DISTORTION IN POWER AMPLIFIERS .225
In the final part of his series on designing out distortion in audio amplifiers, Douglas Self examines the compromise in class A circuitry. Trading efficiency for performance, he presents a worked design for the nearest thing to straight wire with gain.

VLSI MEANS VHDL? 250
Programmable gate arrays offer even the smallest user the possibility of integrating a complete system onto a single chip. Such complexity inevitably requires a new design tool claims Simon Parry.

SAILING BY SATELLITE .254
Plotting the next move in marine electronics, Peter Willis examines the second generation GPS systems with moving map displays for yachtsmen.


## REGULARS

## COMMENT

Very hopeless design language
UPDATE. .182
Copyright battle over multimedia, ultra-fast SiGe transistors are cheap, room temperature quantum tunnelling devices, Intel P6 preview.

## RESEARCH NOTES.

Satellites for the blind, Is thinking bad for you?, wire-less chips, ceramic memories, proof of power line cancer?

PC ENGINEERING
Circuitmaker, circuit training? Read about an education package that combines schematic capture with digital simulation. John Anderson discovers if there are lessons to be learned.

## CIRCUIT IDEAS

Wide range capacitance comparator, ceramic VFO, varicap power supply, temperature variable voltage reference, flipflop protector, video operated relay, even up the marks and spaces, RF field strength meter.

APPLICATIONS..................................................... 234
Minimise distortion from jfet op-amps, power control for portable computers, clocks for data, lead-acid battery charger.
NEW PRODUCT CLASSIFIED ..... 239

The latest new products presented in the industry's most readable format.

LETTERS 244
Technology of spark transmission; Rotten radio quality; Amateurs up in arms; Sick writers and deaf ears; Allophone? My Archimedes is better than your 486DX, etc; Musical (body) organs; Cricket not calculus; Cold fusion hotter?; Square law is old hat; True arrogance, Sagnac and the usual crop of metaphysical hypotheses which this magazine publishes but does not necessarily endorse... And is there anyone from Bolton?

## DESIGN BRIEF

This is the best article which you will ever read on the use of Smith Charts, that indispensable graphical aid to the design of matching networks for RF applications. Ian Hickman will even tell you which way up to hold it.

In next month's issue: Microwave electronics now finds its way into many types of consumer and professional electronics systems. The component manufacturers have responded with off-the-shelf filters, mixers and other modular components. Mike Hosking begins a major new series on applied microwave engineering. APRIL ISSUE ON SALE MARCH 31
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## Very Hopeless Design Language

What do you need to know to work in electronic systems design?
The obvious answer to this question seems to be "knowledge of practical electronic circuitry". This encompasses such basic activities as being able to read the function of a circuit from its schematic; an ability to set up linear networks so that they will behave acceptably towards the signals which they are designed to handle; to be able to predict from calculation the component values required to return a required function; a grasp of logic and logic function.
On page 250 of this issue, we are presenting an article on hardware description languages or HDLs. You will probably become aware on reading it (just as I did) that the world of computer assisted design-by-function bears absolutely no relation to the way that real designers think or operate. It uses a level of abstraction which is simply not appropriate to the development of practical electronics. The only group of designers who think in that structured, lifeless fashion are computer programmers. And they have no business in setting design paradigms for electronics engineers.
If this sounds a bit Luddite, I don't mean it to be. One can and should be able to embrace thoroughly the use of computing in design. It is simply that the data entry method should empathise with the design process. For electronics engineers, this almost always means working with a circuit diagram showing gates, counters, linear amplifiers and
even the odd transistor. Really gifted designers see things visually... a schematic becomes a canvas on which they paint their system. The textual data entry system of current VHDL inhibits creativity.
Computer people see our visual method of working as an object oriented data structure with ill-defined transfer functions. This makes it very difficult to implement in software. However, if electronics designers were prepared to work with a rigidly defined library of parts and functions, then they (the programmers) would be able to simply the design process enormously... And thus was born the nonsense of VHDL.
Most worthwhile computer design tools use schematic entry as the starting point. They then provide simulation and compaction as an intermediate process and subsequently deliver circuit layout or gate programming as output function. HDL software writers point to circuit complexity limits beyond which schematic entry becomes impractical.
This raises a couple of points. A sensible designer will divide up the system into manageable chunks; the actual partioning is much better done by men than machines. Secondly,
debugging problems increase exponentially with circuit size: it pays to do things in small bits.
A large circuit design requires of cad tools that test routines should also be an output function; the one thing it does not require is a change in the way that electronics designers think or work.

Frank Ogden.

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# Copyright battle over multimedia 

The US Patent Office is taking the drastic step of voluntarily re-examining a patent which it granted last August. US 5241671 was filed by Encyclopaedia Britannica, and is now owned by Compton's New Media. The patent claims legal monopoly on a computer search system which covers virtually all the multimedia computer and interactive game software currently going on sale.
The patent was filed in October 1989, by a team of 14 inventors. It claims the basic concept of searching a master database of pictures and text, through different paths, to provide an ideas search, a title search, a topic search, a time line search, a picture explorer search or world atlas search.
Such a broad claim effectively gives

Compton's the right to claim royalties from virtually all its competitors in the multimedia market. This creates strange anomalies. Philips is investing heavily in developing multimedia software to support it CD-I system, so would be especially badly hit by a claim from Compton's. But Philips buys copies of Compton's own multimedia Encyclopaedia to give away with its CD-I players.
Compton's competitors are quick to point to similar search software that was in use before 1989, such as a CD-based maintenance manual for the Boeing 757, Pergamon's Educational Encyclopaedia on CD-ROM, the Guinness Disc of Records and Microsoft's ROM disc called Bookshelf. Many of the software companies under legal

## Tunnelling to victory:

Texas Instruments has successfully built transistors which employ quantum mechanical resonant tunnelling while operating at room temperature. Two of these transistors were integrated with 15 heterojunction bipolar transistors on a test chip which functioned as a 1 -bit full adder. The circuit was unveiled at last December's International Electron Devices meeting in the US. Engineers believe the IC is the world's first to comprise resonant tunnelling electrons operating at room temperature.
The resonant tunnelling bipolar transistors attained a current gain of 100 , and an in-resonance to off-resonance current ratio of 70 . The transistor operated from 3 V with a voltage swing of 1.2 V . The resonant tunnelling double barrier
heterostructure was incorporated into the emitter region of a heterojunction bipolar transistor.
The device was made using molecular beam epitaxy of aluminium and gallium arsenide compounds on an indiumphosphide substrate.
The transistor exploits quantum resonances in the electron tunnelling across barrier region giving rise to a number of negative resistance switching states.

For an input voltage between 0 and 0.8 V the transistor is turned off and the output sits at 2.9 V . As the input voltage is increased, the transistor turns on and reaches its peak resonant current at 1.7 V . The collector current is 0.6 mA and the output voltage 0.56 V . Beyond this input voltage, a plateau region is established. Beyond 2V, the transistor's output goes high again.

threat from the patent cannot afford to fight Compton's in Court. By ordering a reexamination of the patent, the US Patent Office may relieve them of this burden.
Compton also filed a string of foreign patents, including a PCT application WO $91 / 06916$ which covers over 40 countries. This has even more legal claims, a total of 93 , and their scope is even broader. The main claim is to blanket monopoly on a search system with text and graphical paths. There has been little progress with this patent.
Patent searchers believe that Comptons may be finding it a lot harder to convince patent examiners that the idea of searching for text and graphics was novel in 1989 and a patentable invention in Europe Barry Fox.

## Check out radio chip

Supermarket shopping could be revolutionised with a radio chip which will make it possible to price a shopping trolley without unloading it.
A passive cmos memory and transmitter uses the power transmitted by a transceiver placed at the till. The item's stock number and price are stored in the chip's memory which is re-transmitted back to the till. A small wire-dipole will be printed on the inner side of the product's packaging where the chip will be placed.
The British Technology Group is keen to commercialise the tag developed by the South African Council for Scientific and Industrial Research. The developers are attempting to meet a price of 1 p per chip to make the system viable.

## Intel's hot chip?

Intel has given a preview of the $P 6$, the next major microprocessor upgrade to the Pentium line. The new device will contain over six million transistors and will operate at 300 mips . Intel chief Andy Grove claimed that with a four-processor system, manufacturers will find that "building a 1000 mips system will be straightforward with P6 technology."
He made no mention of the power which the device will consume.
-In a continuing bid to distance its products from encroaching competition from competitors, Intel says it is dropping the 486 name when applied to its higher end microprocessors and that its forthcoming triple-clock microprocessor will be simply called the DX4 . The device will offer 100 MHz performance through clock tripling.

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REF: MAG50

## Fast SiGe transistors match silicon costs

| t seems unlikely that gallium arsenide will I ever become a high volume semiconductor material following recent announcements about the availability of a low cost silicon/germanium alternative process.
IBM and Analog Devices have already stated their intention to jointly develop microwave front end chips using the process. Most other semiconductor companies producing high frequency silicon and GaAs have expressed similar interest. Potential uses include antenna switches, low noise amplifiers and down converters
Silicon bipolar circuits have the performance potential but are power hungry - a significant disadvantage for hand-held systems. Silicon/germanium semiconductors are now seen as the natural successor to cmos for high speed circuits. The IBM process gives transistor speeds of 75 GHz and can be made on 8 in wafers. Devices operate from 3 and 1.5 V supplies.
The process employs a SiGe heterojunction bipolar transistor (HBT) in which an epitaxial film of boron doped SiGe alloy, deposited on the silicon wafer, forms the base region of a vertical npn transistor. The film is grown using ultra-high vacuum chemical vapour deposition. A relatively

small number of the HBTs can be integrated on an otherwise conventional silicon cmos process, minimising the changes to the production steps.
The limited number of changes needed to incorporate the SiGe HBTs into a cmos process is key because the incremental wafer processing cost is minimal.
According to Peter Osbourne, an engineer with GEC-Plessey Semiconductors, the changes would amount to no more than "one or two per cent" of the total number of processing operations on a cmos wafer.

Osbourne reports that GPS has been working on SiGe materials for the "past couple of years". He quotes an incremental cost of about $5 \%$ to add SiGe devices to a cmos wafer.
This contrasts sharply with the costs of a GaAs process. The wafer costs are about five times those of silicon.
Other companies are taking note. While Motorola currently favours GaAs for high speed, low power and low voltage processing, it has been investigating SiGe circuits for the past three years.

## Advert eliminator

$A_{w}^{\mathrm{u}}$US company is to market a system which is claimed to remove adverts from any video recording of a broadcast tv programme.
Arista, of Hauppage, NY, inventors of Commercial Brake, noted that all tv stations in North America broadcast commercials in the same way. The screen fades to black between each advert.
The unit connects between the tv aerial and the VCR, and between the VCR and $t v$ set and contains a memory and IR transmitter. It continually monitors the tv signal, looking for fades to black, and logging them in the memory. At the same time a broad band timing signal is added to the to signal as it is recorded on tape.
When the tape is replayed, the unit distinguishes between individual fades which are likely to be part of the programme, and clusters of closely spaced fades which are likely to represent a commercial break containing several adverts in succession. At the start of each cluster the remote control blanks the sound and picture while fast-forwarding the VCR to the end of the cluster. Thus instead of seeing three
minutes of commercials, the viewer sees ten or fifteen seconds of blank screen. But the adverts are recorded on tape in case the user ever wants to view them.
Other aids are also available to the determined viewer. Gemstar of Pasadena in California will modify its VideoPlus system to help people who still have difficulty taping programmes. The handset contains its own clock and switches the VCR on to start recording at whatever time the programme begins.
The complication is that each handset must be set up to work with the viewer's particular brand of VCR: the viewer has had to enter identification codes which do not always work. The new VideoPlus handsets, which will cost around $\$ 60$, have a microphone which responds to control tones. The owner simply dials Gemstar's hotline, tells the operator the name of the VCR, and holds the handset to the telephone ear piece. The company sends tones down the line which set up the handset to work with the VCR. If the owner buys a new VCR, the handset can be re-programmed with another phone call. Barry Fox

## CD action line

F ollowing on from last month's story Fabout rotting CDs, Philips has set up a telephone hotline to help anyone who thinks they have bought faulty CDs pressed by its PDO factory in Blackburn. Where discs are genuinely faulty, Philips will try to replace them with good pressings of the same music.
Philips' PDO factory in Blackburn is unique because it uses silver as a reflective material, whereas other plants use aluminium. The plant was originally built to produce video discs. The original video production process covered the silver with a nitrocellulose lacquer, applied in a solvent which was then evaporated in hot air. Philips used this too for CD production.
Between 1989 and 1990 PDO found that sulphur released from some crudely processed paper CD sleeves was getting through the lacquer to tarnish the silver. As tarnishing progresses, the reflectivity decreases until the laser in the CD player cannot read the disc.
The enquiry number is 0800 387063. BF

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## Satellite systems that help the blind to see

E very so often we find welcome evidence that miniaturisation has achieved more than just packing a few more megabytes of memory onto the same bit of silicon. A personal gps navigation system for blind people, currently being studied by an interdisciplinary group of scientists at the


Substitute for a guide dog? Virtual sound and gps navigation combine to help blind people see their way around. The gps reference, accurate to within 3 m , is augmented by a geographic database showing pavements, buildings, etc.

University of California, Santa Barbara, is a prime example.
After nearly eight years of research, the Santa Barbara team has produced a prototype personal guidance system - a portable device, designed to provide visually impaired users with information about their location and surroundings. In its fully developed form it would allow a blind user to navigate around an unfamiliar area without assistance.
The group developing the system in conjunction with colleagues at CarnegieMellon University, points out that the gps system is not designed to replace guide dogs or white canes. It cannot, for example, help users avoid small obstacles or pot-holes in the pavement. But what it can do is provide the geographical and directional information that can otherwise only be obtained by stopping people and asking the way.
The 281b prototype combines three technologies: a gps satellite receiver, a geographic database and an "acoustic display".
The receiver gives a grid location accurate to within 3 m , while the geographic database tracks the user's position in relation to buildings, walkways, roads and other permanent hazards. Velocity sensors are also being incorporated for dead-reckoning when the satellite signals are temporarily obscured.
The hardest task has been to provide a meaningful way to convey the information to blind people. It is one thing to create a visual display, but quite another to convey a large amount of continually changing data to someone without sight. Santa Barbara's

## Could thinking too hard be bad for us?

Once we have learned a skill - from driving a car to using morse code - it is hard to believe we ever found it difficult. Even complex tasks seem to require almost no mental effort when they have been mastered.
The obvious conclusion is that the human brain somehow switches into autopilot and uses a more economical circuit configuration for capabilities that have been laboriously learned.
Professor Marcus Raichle of Washington University School of Medicine in St Louis, writing in the January issue of Cerebral Cortex), believes he may have gone some way to explaining these observations.
He and his co-workers have found a circuit
in the brain that automates certain learned processes. According to the researchers, there seem to be two distinct circuits for completing a task.
When learning, we use a circuit specifically adapted to handling new data. But after practice, we switch to a second circuit in a different part of the brain that is adapted to handle already-learned tasks.
The team used a positron emission tomography (pet) scanner to study the brains of volunteers while they learned to associate certain nouns with particular verbs. As they memorised the associations, the scanner revealed that the mental activity shifted from one area of the brain to another.
Raichle says that, for simple learning
solution is a "virtual acoustic display", relaying specially synthesised sounds through stereo headphones. The sounds are generated by customised circuits which make them appear to come from specific external locations.
Blindfold tests have shown that people can walk to the location of a "virtual" sound as accurately as they can walk towards a real, external, sound.
So what happens if the blind person turns his or her head? Surely the position of the virtual sound will change?
That is true, except for the fact that the researchers have built a compass into their prototype. If the subject turns around, the sound image will remain fixed relative to the outside world.

At the moment, the group are still working on how best to interface the gps, receiver, the geographic database and the virtual acoustic display. Voiced instructions might be the simplest method, but computergenerated speech can rapidly become irritating and intrusive.

Another method would be to use a moving auditory beacon. In this case, the virtual acoustic display might produce a tone from the direction towards which the user should proceed. This could swing from hard left, through straight ahead to hard right (though front/rear ambiguity might be a problem).
Looking beyond the immediate needs of blind people, professor Jack Loomis at Santa Barbara believes that normally-sighted tourists could carry hand-held navigation systems to tell them where they are and provide full details of how to find other places in the area.
tasks, the transfer occurs after less than 15 min practice. The purpose of the shift could be to free the front-line "input" areas of the brain from the need to work hard over mundane tasks; like putting a plane on autopilot.
Well-practiced activities demand much less attention and energy than activities which are unfamiliar. But problems can arise when we start concentrating inappropriately hard on something that has already become automatic. Nervousness often causes us to mistrust our automatic reactions and (on Raichle's theory) to replace them with a brain circuit more adapted to early learning.
Raichle quotes the example of a skilled
basket-ball player about to take a free throw. The tension of the moment leads the player to think hard and so use an inappropriate brain circuit. The result is the disappearance of a normally-automatic skill and a miss.
Research has also identified examples of the opposite fault; a tendency to remain on autopilot when we should be doing some original thinking: taking the home exit from a motorway when we're actually going somewhere else, for example. In this situation, says Raichle, we should make a conscious effort to disengage the autopilot.
The findings tie in remarkably well with our everyday experiences, and explain why learning is such a frustrating experience. But will the conclusions be fully grasped by designers of computer systems, producing machines that have the brain's ability to switch repetitive tasks to an autopilot, eliminating data bottlenecks and reducing the need for processing power?
If so, there could be a price to pay. Such machines would become terribly absent minded and get very set in their ways. Like humans, they had also have to be put on the scrap-heap after a certain age.


Activity in various areas of the brain while learning, right, carrying out a familiar task, middle, and thinking about something already learned, left. When working on something already learned, activity in the brain is shifted. Researchers believe that this is to free the input areas of the brain for more important tasks. Activity is indicated by blood flow.

## Dotty way to make quantum devices

A safer way to synthesise gallium arsenide and other important III-V semiconductors, devised by chemists at Duke University in North Carolina, could also be used to produce semiconductor crystals of "quantum dot" dimensions.
Quantum dots consist of only a few thousand atoms and, in electronic terms, behave in a very different way from bulk material. Traditional methods for making III-V semiconductors call for high temperatures and chemicals that are either poisonous or which spontaneously ignite if exposed to air. For example, trimethyl gallium - the usual starting point in the manufacture of gallium arsenide - is reacted with highly toxic arsine (arsenic hydride) gas at $700^{\circ} \mathrm{C}$ in the presence of highly explosive hydrogen. Needless to say, scientists have been putting considerable effort into perfecting a less lethal cocktail.
Just over three years ago a Duke team, led by Professor Richard Wells, discovered that the same results could be achieved by reacting gallium trichloride with "tris" trimethylsilylarsine. Not only were the ingredients much safer, the reaction took place at only $75^{\circ} \mathrm{C}$.
Soon after, another team led by Dr Paul

Alivisatos at the University of California at Berkeley, discovered that gallium arsenide made by Wells' method would crystallise as quantum dots when the reaction was made to take place in the organic solvent quinoline. The quantum dots, or nanocrystal, measured only a few billionths of a metre in diameter.
Since then, the original group at Duke University has developed the lowtemperature chemistry to produce other III-V compounds such as gallium phosphide, indium phosphide and indium antimonide. They have shown that these alternative chemical reactions can also produce quantum dot structures, the sizes of which vary according to the conditions of the reaction and the solvent used.
Beyond that, the Duke researchers have shown it is possible to deposit the quantum dots in orderly arrays on substrates such as glass, porous silicon and various conductive polymers. This should enable them, soon, to measure the electronic properties of the dots directly.
Professor Wells stresses that the work is not directly aimed at the commercial production of quantum electronic devices. It does, nevertheless, create the theoretical basis for a whole new fabrication technology.

## Wire cutters unleash chip performance

$\mathrm{O}^{\mathrm{n}}$ne of the fundamental barriers to faster processing in multi-chip modules, MCMs, could soon be overcome if electronics engineers at Loughborough University can perfect their new technique for wireless interconnection.
The Loughborough method (Electronics Letters, vol 29, No.2) eliminates wiring for interconnecting chips and so removes one of the commonest drags on speed.
Microelectronic devices are now so fast that the biggest limitations in system performance nearly always lie in the metallic interconnections between chips. Standard problems include propagation delays, reflections from sharp bends and other discontinuities, together with cross talk between adjacent conductors.
The Loughborough proposal is to replace the metal interconnects with millimetric or quasi-optical links, as shown in the diagram. Devices would be placed on a substrate and covered with a reflecting metal lid. Instead of being joined by wires, the chips would communicate with each other by signals reflected off this lid.
Techniques for making chips generate millimetric signals are already well advanced - so too are ideas for etching


To see whether microwaves instead of wires could be used to interconnect multi-chip modules, researchers at Loughborough University built this scaled-up model. Initial tests at $I$-band have proved positive. Now the team is to try planar transmission lines operating at $Q$ band in preparation for final feasibility tests at millimetric-wavelengths.
monolithic feed lines and steerable radiating elements. The Loughborough researchers have constructed a large-scale J-band model, shown in the photos, to test the concept
Leaky wave antennas were modelled in software and then tested in the lab. Practical tests showed that it would be feasible to use beamed microwave transmissions for interchip communication in high speed systems.
The next step is including a scale model using planar transmission lines at Q-band. After that has been evaluated, the aim is to proceed to the higher millimetric frequencies required for practical MCM interconnects.

Connecting multichip modules via wires limits speed, causing propagation delays, reflections at bends and crosstalk. Connecting via microwave beams could offer a significant improvement in MCM speed by removing these restrictions.


## IC memories with a touch of amnesia?

The next generation of ultra-large scale ics could fail because of 'soft' faults inherent in their design. That is the conclusion of Texas Instruments researchers in Japan and the USA (Electronics Letters, Vol 29, No 24).
The fear stems from the growing use of ferroelectric materials in replacing silicon nitride and silicon oxide as the insulating material in memory-cell capacitors. Ferroelectric ceramics, such as strontium titanate (STO) and lead zirconate (PZT), have a high permittivity so a memory-cell capacitor with a relatively small electrode area can be built. This avoids complex 3D structures.
But there is a major problem with both STO and PZT. Commonly used electrode materials such as aluminium, titanium, copper and tungsten become oxidised and so reduce the maximum achievable capacitance. Platinum appears best suited electrode material, because it doesn't readily oxidise. But though it is ideal from a chemical point of view, it has one serious disadvantage - in addition to the price.

All natural platinum contains $0.01 \%$ of radioactive isotope $\mathrm{Pt}^{190}$. The isotope emits alpha radiation with an energy of 3.18 MeV enough to cause local ionisation and soft errors in any dram memory cells incorporating it, so the theory goes. The TI team has put this to the test by fabricating film structures on silicon similar to those used for the bottom electrodes of ferroelectric memories. One test wafer used a $\mathrm{Ti} / \mathrm{SiO}_{2} / \mathrm{Ti}$ construction while the other had an additional platinum layer.
The researchers compared alpha emissivity of the two structures, allowing for background radiation and found that any real device based on platinum would have an unacceptable rate of soft failure. Calculations show that a 256 Mbitk dram based on sto would produce $7 \times 10^{-3}$ errors per hour. This, says the group, is around a hundred times worse than the minimum acceptable figure, even assuming that only $1 \%$ of alpha particles cause soft errors.
Platinum, it seems, is not the material of eternal memories!

## Statistical proof claimed for power-line cancer

A
'study of studies' by Swedish, Finnish and Danish cancer experts has concluded that children living near highvoltage overhead power lines have around twice the risk of getting leukaemia. In a letter to The Lancet (Vol 342 No 8882), the researchers claim that this latest work overcomes many of the weaknesses of the earlier individual studies - particularly statistical significance of small numbers.

Anders Ahlborn of the Karolinska Institute in Sweden is lead author of a letter giving brief details of new facts emerging from the pooling of three recent Nordic studies. Two of the studies, one in Denmark the other in Finland, have previously been reported in this journal; the third in Sweden is, at the time of writing, unpublished.
Although the three studies were planned in concert, there have been considerable difficulties in pooling the results. As Ahlborn and colleagues point out in their latest letter, local circumstances led each
study to adopt slightly different criteria. The Danish and Finnish studies were based on entire populations while the Swedish study looked particularly at those children living under power lines. Several differences also existed in the ways the data were collected and the methods used for calculating exposure to 50 Hz fields.

Nevertheless, given these limitations, the researchers are agreed that a pooled analysis of their individual results has overcome one particular limitation of each individual study, namely the statistically small number of cancer cases. Ahlborn and his co-authors conclude that 50 Hz magnetic fields are statistically associated with an increase in childhood leukaemia, whereas for other childhood cancers the evidence is less clear.
For those who are fearful of bringing up their children near overhead power lines, it must be emphasised that the doubled risk of leukaemia is two multiplied by something very small. Leukaemia is extremely rare,
even among children exposed to strong ac magnetic fields. It is this very rareness that has made the recent Nordic studies so difficult. Another encouraging observation is that there appears to be a lower cut-off value of around $0.2 \mu \mathrm{~T}$, below which ac fields cause no increase in the risk of leukaemia. This value is considerably higher than any magnetic field encountered in $99.5 \%$ of normal domestic environments.

Finally, a wholly convincing biological mechanism has yet to be found to explain how ac magnetic fields could exacerbate the risk of leukaemia. One of the authors of the latest letter to The Lancet has readily admitted that ac fields could be a co-variable of some purely social factor.

Open-mindedness, rather than panic action, would appear to be the most appropriate reaction at present.

Research Notes is written by John Wilson of the BBC World Service.

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Marconl TF1245 Circult magnification meter +1246 \& 1247 Oscillators - $£ 100-£ 300$. Marconl microwave 6600A sweep osc., maintrame with $6650 \mathrm{PI}-18-26.5 \mathrm{GHz}$ or $6651 \mathrm{PI}-26.5$ $40 \mathrm{GHz}-£ 1000$ or PI only $£ 600$
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Microwave Systems MOS/ 3600 Microwave frequency stabilizer - 1 GHz to 40 GHz £ 1 k . Tehtronix Plug-ins 7A13-7A14-7A18-7A24-7A26-7A11-7M11-7S11-7D10-7S12S1 - S2 - S6 - S52 - PG506 - SC504 - SG502 - SG503 - SG504 - DC503 - DC508 - DD501 WR501 - DM501A - FG501A - TG501 - PG502 - DC505A - FG504 - P.O.R
Alitech Stoddant recelver type 17/27A-.01-32MC/s - £2500.
Altech Stoddar recelver type $37 / 57-30 \cdot 1000 \mathrm{Mc/s}-\Sigma 2500$.
Gould J3B Test osclllator + manual - £200.
Intra-red Binoculars in fibre-glass carrying case - lested - $£ 100$. Infra-red AFV sights $£ 100$. ACL Field Intenstity meter receiver type SR - 209-6. Plugs-ins from $5 \mathrm{Mc} / \mathrm{s}$ to $4 \mathrm{GHz}-\mathrm{P} . \mathrm{O}$. R Tektronlx 491 spectrum analyser $-1.5 \mathrm{GHz}-40 \mathrm{GHz}$ - as new $-£ 1000$ or $10 \mathrm{Mc} / \mathbf{s} 40 \mathrm{GHz}$. Teltronix Malnirames - 7603-7623A - 7633-7704A - 7844-7904 - TM501 - TM503 -TM506-7904-7834-7104.
Knott Polyskanner WM1 001 + WM5001 + WM3002 + WM4001 - $£ 500$.
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Altech 757 Spectrum Analyser - 00122 GHz - Digital Storage + Readout - $£ 3000$. Dranetz 606 Power line disturbance analyser - $£ 250$.
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Datron 1065 Auto Cal digital multimeter with instruction manual - $\mathbf{\Sigma 5 0 0}$.
Racal MA 259 FX standard. Output $100 \mathrm{kc} / \mathrm{s}-1 \mathrm{Mc} / \mathrm{s}-5 \mathrm{Mc} / \mathrm{s}$ - intemal NiCad battery - $£ 150$, Aerial array on metal plate $9^{\prime \prime} \times 9^{\prime \prime}$ contalning 4 aernals plus Narda detector $-.100-11 \mathrm{GHz}$. Using N type and SMA plugs \& sockets - ex eqpt - $£ 100$.
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Marconl RF Power Amplifier TF2175-1.5Mc/s to 520Mc/s with book - $\mathbf{8 1 0 0}$
Marconl 6155 A Slgnal Source -1 to 2 GHz - LED readout - $£ 600$.
Schlumberger 2741 Programmable Microwave Counter - 10 Hz to $7.1 \mathrm{GHz}-£ 750$.
Schlumberger 2720 Programmable Universal Counter 0 to $1250 \mathrm{Mc/s}$ - $£ 600$.
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TEK 576 Callbration FIxture - 067-0597-99 - $£ 250$.
HP 8006A Word Generator - £150.
HP 1645A Data Error Analyser - $£ 150$
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Barr \& Stroud varlable filter EF3 $0.1 \mathrm{~Hz}-100 \mathrm{kc} / \mathrm{s}+$ high pass + low
Barr \& Stroud varlable filter EF3 $0.1 \mathrm{~Hz}-100 \mathrm{kC} / \mathrm{s}$ + high pass + low pass - $£ 150$.
S.E. Lab SM215 Mk11 transter standard voltmeter - 1000 volis.

Alitech Stoddart P7 programmer - $£ 200$.
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thermometer +9 probes. $£ 350$ all three items.
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H.P. 3438 A digital multimeter.
H.P. 6177C DC current source. §150.
H.P. 62078 DC power supply.
H.P. 741 BACDC differential volimeter standard (old colour) $£ 100$.
H.P. 6209B DC power unit.

Fluke 80 high voltage divider.
Fluke 431C high voltage DC supply.
Tektronix M2 gated delay calibration fixture. 067-0712-00
Tektronix precislon DC divider calibration fixture. 067-0503-00
Tektronlx overdrlve recovery calibration fixture. 067-0608-00.
Avo VCM163 valve tester+book $£ 300$.
H.P. 5011 logic trouble shooting kit. $£ 150$.
Marconi TF2163S attenuator -1 GHz . $£ 200$.

Marconi TF2163S attenuator - 1 GHz . $£ 200$.
Fluke 730A DC transter standard.
B\&K 4815 calibrator nead

## B\&K 4812 calibrator head

Farnell power unlt H60/50- $£ 400$ tested.
H.P. FX do ubler 938A or 940A - £300.

Racal/Dana 9300 RMS voltmeter - $£ 250$.
H.P. sweeper plug-Ins - 86240A - $2-8.4 \mathrm{GHz}-86260 \mathrm{~A}-12.4-18 \mathrm{GHz}$ - $86260 \mathrm{AH} 03-10-$
$15 \mathrm{GHz}-86290 \mathrm{~B}-2-18.6 \mathrm{GHz}$. 86245A $5.9-12.4 \mathrm{GHz}$.
Telequipment CT71 curve tracer - $£ 200$.
H.P. 461 A amplifier - $\mathbf{1 k c}-150 \mathrm{Mc} / \mathrm{s}$ - old colour - $£ 100$.
H.P. 8750A storage normalizer.

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Racal/Dana signal generator $9082-1.5-520 \mathrm{Mc} / \mathrm{s}-£ 800$.
Claude Lyons Compuline - line condition monitor - in case - LMP1 + LCM1 $£ 500$
Efratom Atomic FX standard FRT - FRK -. 1-1-5-10Mc/s. £3K tested.
Racal 4D recorder - £350-£450 in carrying bag as new
HP8350A sweep oscillator mainframe + HP1 1869A RF PI adaptor - $£ 1500$.
Altech - precision automatic noise figure indicator type $75-£ 250$.
Adret FX synthesizer $2230 \mathrm{~A}-1 \mathrm{Mc} / \mathrm{s}$. $£ 250$.
Tektron|x-7S12-7S14-TT11-7S11-S1-S52-S53.
Aotek 610 AC/DC calibrator. £2K + book.
Marconl TF2512 RF power meter - 10 or 30 watts - 50 ohms - $£ 80$
Marconi multiplex tester type 2830.
Marconi digital simulator type 2828A.
Marconi channel access switch type 2831.
Marconi automatic distortion meter type TF2337A - $£ 150$.
Marconl mod meters type TF $2304-£ 250$.
HP 5240 A counter - 10 Hz to $12.4 \mathrm{GHz}-\mathrm{I} 400$.
HP 3763 A error detector.
HP 8016 A word generator.
HP 489A micro-wave amp - $1-2 \mathrm{GHz}$
HP 8565 a spectrum analyser $-.01-22 \mathrm{GHz}$ - 24 k
HP 5065A rubidium vapour FX standard - $£ 5$
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Systron Donner counter type $6054 \mathrm{~B}-20 \mathrm{Mc} / \mathrm{s}-24 \mathrm{GHz}$ - LED readout - $\mathbf{£ 1} \mathbf{1 k}$
Takeda Rlken TR4120 tracking scope + TR1604P digital memory.
EG\&G Parc model 4001 indicator +4203 signal averager PI.
Systron Donner 6120 countertimer $A+B+C$ inputs - $18 \mathrm{GHz}-£ 1 \mathrm{k}$
Systron Donner signal generator 1702-synthesized to 1 GHz - AM/FM
Systron Donner microwave counter 6057 - 18GHz - Nixey tube - $£ 600$.
Racal/Dana synthesized signal generator $9081-520 \mathrm{Mc} / \mathrm{s}-\mathrm{AM}-\mathrm{FM} . \mathrm{£} 600$.
Farnell SSG520 synthesized signal generator $-520 \mathrm{Mc} / \mathrm{s}-£ 500$.
Farnell TTS520 test set - $£ 500$-both $£ 900$.
Tektronix plug-ins - AM503 - PG501 - PG508 - PS503A.
Tekfronix TM515 mainframe + TM5006 mainfr ame.
Cole power line monitor T1085-£250.
Claude Lyons LCM1P line condition monitor - $£ 250$.
Ahodes \& Schwarz power signal generator SLRD-280-2750Mc/s. £250- 6600 .
Ahodes \& Schwarz vector analyser - ZPV +E1 + E3 tuners - $3-2000 \mathrm{Mc} / \mathrm{s}$.
Bell \& Howell TMA 3000 tape motion analyser - $£ 250$.
Ball Efratom PTB-100 rubidium standard mounted in Tek PI.,
Ball Efratom rubidium standard PT 2568 -FRKL.
Trend Data tester type 100-£150.
Farnell electronic load type RB1030-35.
Falrchild interterence analyser model EMC-25-14kc/s-1GHz.
Fluke 1720A instrument controller + keyboard.
Marconi 2442-microwave courter-26.564
Racal/Dana counters -9904-9905-9906-9915-9916-9917-9921-50Mc/s-3GHz-
100- $£ 450$ - all fitted with FX standards
B\&K 7003 tape recorder - $£ 300$
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wiltron swep maintrame 6100 .
HP32008 VHF osclliator $-10-500 \mathrm{Mc} / \mathrm{s}-\mathrm{E} 200$.
HP3747A selectlve level measuring 5 et
HP3586A selectlve level meter
HP5345A electronic counter.
HP 4815A RF vector Impedance meter c/w probe. £500- $\mathbf{5 6 0 0}$
Marconi TF2092 noise receiver. A, B or C plus fiters.
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Tektronlx oscilloscope $485-350 \mathrm{Mc} / \mathrm{s}-\mathrm{E} 500$.
HP 180TR, HP 182 T maintrames $£ 300-£ 500$.
Bell \& Howell CSM2000B recorders.
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Fluke 8506A thermal RMS digital multimeter.
HP3581A wave analyser.
Phillips panoramic receiver type PM7800-1 to 20 GHz
Marconi 6700A sweep oscillator $+6730 \mathrm{~A}-1$ to 2 GHz
Wiltron scaler network analyser $560+3$ heads. $£ 1 \mathrm{k}$.
R\&S signal generator SMS $-0.4-1040 \mathrm{Mc} / \mathrm{s}-£ 1500$.
HP8558B spectrum ANZ PI-. 1-1500 Me/s - o/c - $£ 1000$. N/C - $£ 1500$ - To fit HP180 series malntrame avallable - $£ 100$ to $£ 500$.
HP8505A network ANZ + 8503A S parameter test set +8501 A normalizer - £4k.
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acal/Dana 9087 signal generator - $1300 \mathrm{Mc} / \mathrm{s}-$ § 2 k .
Racal/Dana VLF frequency standard equipment. Tracor receiver type 900A + difference
meler type 527 E+rubldum standard type $9475-£ 2750$.
4.2GHz - £800- 1000 .
HP8444A-HP8444A opt 59 tracking generator $£ 1 \mathrm{k}-£ 2 \mathrm{k}$.

HP8444A-HP8444A opt 2308.
HP8755A scaler ANZ with heads $£ 1 \mathrm{~K}$.
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Bradley oscliloscope calibrator type $192-£ 600$.
Spectrascope SD330A LF realtime ANZ -20Hz-50kHz - LED readout - tested - $£ 500$. HP8620A or 8620C sweep generators - $£ 250$ to $£ 1 \mathrm{k}$ with IEEE.
Bart : Stroud varlable filter EF3 $0.1 \mathrm{~Hz}-100 \mathrm{kc} / \mathrm{s}+$ high pass + 10 w pass - $£ 150$.
Tektronix 7 L 12 analyser -. $\mathrm{IMC} / \mathrm{s}-1.8 \mathrm{GHz}-£ 1500-7 \mathrm{~L} 14 \mathrm{ANZ}$ - E 2 k .
Marconi TF2370 spectrum ANZ - 110 MC /s - $\mathbf{~} 1200-£ 2 \mathrm{k}$.
Marconl TF2370 spectrum ANZ + TK2373 FX extender 1250Mc/s+trk gen - £2.5k-£3k.
Racal recelvers - RA 17 L-RA1217-RA1218-RA $772-$ RA1792 - P.O.R.
Systron Donner microwave counter $6057-18 \mathrm{GHz}$ - nlxey tube - $£ 600$
HP 8616 signal gen $1.8 \mathrm{GHz}-4.5 \mathrm{GHz}$ old colour $£ 200$, new colour $£ 400$
 htems markeo tested have 30-oay warranty. Wanteo: test eopt - valves - plugs a sockets - syncros - tramsmiting a receiving eapt. eic.
Johns Radio, Whitehall Works, 84 Whitehall Road East, Birkenshaw, Bradford BD11 2ER. Tel. No. (0274) 684007 . Fax 651160.


Switch-mode power circuits are more complex than their linear counterparts but the benefits they offer can be well worth the extra design effort. Duncan Smith explores the various topologies.

The most common use of the switchedmode power supply, SMPS, is in mains derived supplies for computers and other such equipment. Over the past few years the use of, and the need for, switch-mode power supplies has grown. This is partly due to the rise in demand for portable battery-driven equipment, and partly due to the need to use power more efficiently for environmental as well as economic reasons.
Relative to a linear supply, the major advantage of an SMPS is its efficiency. For example a linear $+5 \mathrm{~V}, 1 \mathrm{~A}$ supply derived from a 12 to 24 V source would be $42 \%$ efficient at 12 V and $21 \%$ at 24 V , the remaining power being dissipated as heat. A poor SMPS supply would be around $75 \%$ efficient irrespective of input voltage. Charge pumps aside, only a switch-mode PSU can provide an output voltage higher than the input.

## Converter topologies

With the exception of capacitive voltage doubler/inverter circuits, switch-mode power supplies use inductors or transformers to transfer energy from the input supply to the load. Energy is stored in the inductor while the switching element is closed. It is then released when the switch is opened (see panel).
Only a specific amount of energy can be stored in the inductor, and this is limited by the material it is wound on. When the inductor core saturates, the end result may be destruction of the switching element. The winding insulation may also be damaged by the heat generated, which can lead to short-circuiting.
Two methods are commonly applied to control the output voltage of an SMPS. Either the frequency, or the pulse width, is modulated by
the circuit. Changing the operating frequency often produces a simpler circuit, but results in the generation of a broad spectrum of unwanted interference signals. These signals can be difficult to filter out.
Using pulse-width modulation however allows simpler filtering to remove the unwanted signals. A useful feature of a PWM SMPS is that more than one supply can be slaved to a central clock which limits 'beating' between supply oscillators. This beating effect produces frequency components below the operating frequency of the supply. In turn, this can cause significant noise and interference problems if these components lie in the frequency range of the equipment being powered.
An important criterion when designing a switched-mode supply is: "can the basic source supply enough current to meet the power requirements of the load?" For example, a $15 \mathrm{~V}, 0.5 \mathrm{~A}$ maximum supply is needed from a 5 V source. The output load will dissipate 7.5 W . Assuming a $100 \%$ efficient converter, the source must deliver an identical power. This means that the source must be able to provide 1.5 A without collapsing the input supply voltage.
In addition, depending on the converter topology, large peak currents may also need to be catered for. As a result, the source supply must have a low enough impedance to be able to deliver this demand. This can be a problem when running from almost discharged batteries.
A wide variety of converter forms exist, each with their own particular advantages and disadvantages. The scope of this article is limited to the basic forms. It is worth noting that similar supplies can be constructed from dissimilar switching circuits. For instance, $a+5 \mathrm{~V}$
supply can be designed around either a buck or isolated flyback topology.
Various books and literature often refer to the same converter topologies by different names which can be confusing. As an example, with buck and forward converters the basic switching circuit is identical. However some authors are referring to the isolated form when they refer to the forward converter.

## The buck or forward converter

Buck converters perform a similar task to step-down transformers. In the forward converter, Fig. 1, when switch $S$ is closed current flows through the inductor $L$ producing a positive voltage across the load. Diode $D$ does not conduct as it is reverse biased.
When the switch is opened, voltage across the inductor reverses polarity. Diode $D$ thus becomes forward biased and allows current to flow from the inductor through the capacitor. Voltage across the load remains positive. The diode is known as a flyback diode.

## Deriving step-down converter output voltage

Output voltage from a step-down converter can be derived by considering the voltage across the inductor. In steady-state operation the voltage waveform across the inductor must repeat from one switching cycle to the next. As a result the integral of the inductor voltage over a single time period, $T$, i.e. $t_{\text {on }}+t_{\text {off, }}$ must be zero.

To derive the output voltage the assumption is made that a fixed frequency oscillator is used to derive the PWM signal:

$$
\int_{0}^{T} V_{L} \mathrm{~d} t=0
$$

which is:

$$
\int_{0}^{T} V_{L} \mathrm{~d} t=\int_{0}^{t_{0}} V_{L} \mathrm{~d} t+\int_{t_{f e x}}^{T} V_{L} \mathrm{~d} t
$$

Referring back to Fig. 1 in the main text, when the switch is closed during $t_{\text {on }}$, voltage across the inductor is the input, $V_{\mathrm{in}}$, minus the output, $V_{o}$. When the switch is open, during the time $T$ minus $t_{o n}$ (i.e. $t_{\text {off }}$ ) voltage across the inductor is $V_{o}$, the output. Thus:

$$
\int_{0}^{t_{0}}\left(V_{t n}-V_{0}\right) \mathrm{d} t+\int_{t_{t e n}}^{T} V_{0} \mathrm{~d} t=0
$$

which is:

$$
\left[0-\left(V_{i n}-V_{0}\right) t_{o n}\right]+\left[V_{0} T-V_{0} t_{o n}\right]=0
$$

Therefore:

$$
-\left(V_{\mathrm{in}}-V_{\mathrm{o}}\right) t_{\mathrm{on}}=V_{\mathrm{o}}\left(T-t_{\mathrm{on}}\right)
$$

which rearranging gives:

$$
V_{0}=V_{i n}\left(t_{o n} / T\right)
$$

Output equations for all the other SMPS configurations can be derived in a similar way.

While the input current pulses at the switching frequency, the forward converter has a continuous flow of output current. The switch configuration always results in an output voltage lower than the input. It can also be configured to regulate negative input voltages by simply turning the diode round the other way. Zero load output voltage is given by:

$$
V_{\mathrm{o}}=V_{\mathrm{in}} \mathrm{t}_{\mathrm{on}} / T
$$

where $t_{\mathrm{on}}$ is switch on time and $T$ is total oscillator period, i.e. $t_{\mathrm{on}}+t_{\mathrm{off}}$, ignoring the forward voltage of the diode. This can be derived by considering the average voltage across the inductor, i.e. the input voltage multiplied by the ratio of the switch on time to total period. A more rigorous solution is given in the second panel.
In a buck converter circuit, Fig. 2, output level is regulated by a simple pulse-width modulator control circuit. Block functions are as follows. Output voltage is sensed via the potential divider $R_{1,2}$. This is compared with the reference voltage by error amplifier $A_{1}$, producing a difference signal.
Error voltage output is then used to control the 'trip point' of comparator $A_{2}$, the other input of which is driven by a sawtooth or triangular waveform. Resulting output is a pulsewidth modulated signal. To achieve negative feedback and therefore regulate the output voltage, the switch must open when the output is low and close when the PWM control pulse is high.
If output voltage level rises, the potential divider voltage, and thus the error signal level, also increases. The time taken for the oscillator sawtooth to ramp up to the same level as the error signal is increased. Comparator output goes high, i.e. switch $S$ is closed, for a shorter period of time than normal, i.e. $t_{\mathrm{on}}$ becomes smaller. This reduces the current rise in the inductor, and hence the amount of energy transferred.

Likewise, when output voltage drops, the error signal level falls increasing the on-time of the switch. More current flows into the inductor and, as a result, the output voltage rises. It is important to note that it may well take a number of oscillator cycles to correct the rise and fall of the output, introducing a ripple component onto the output voltage.

## Boost converter

Figure 3 shows the basic boost configuration. When the switch is closed, current flows through the inductor storing energy. Diode $D$ is reverse biased blocking the supply $+V_{\text {in }}$. When the switch is opened, voltage across the inductor reverses polarity. Diode $D$ thus becomes forward biased and current flows through the diode and the charging capacitor. Output voltage is therefore positive and always larger than the input.
This type of circuit can generate large amounts of ripple current at the input of the converter. A similar control circuit to that described previously can be used to provide regulation. Output voltage is given by:


Fig. 1. Forward SMPS converters, also known as buck circuits, perform a similar task to step-down transformers.


Fig. 2. Additional functions needed to regulate output of the buck-converter. Error voltage affects the point at which the comparator switches on the oscillator ramp. This produces the rectangular pulse-width modulation waveform.


Fig. 3. With the boost converter, output voltage is always larger than the input. This configuration can produce large amounts of ripple at the input.


Fig. 4. Flyback or buck-boost converters can be used to invert the input voltage and step the voltage up or down. The drawback is large amounts of ripple at the input and output.


Fig. 5. Using a transformer with the flyback configuration adds isolation and flexibility -allowing step up, step down, inversion and extra supply rails.

$$
V_{\mathrm{o}}=V_{\mathrm{in}}\left(1+t_{\mathrm{on}} / t_{\mathrm{off}}\right)
$$

where $t_{o n}$ is the switch on time, and $t_{\text {off }}$ is the switch off time.

## Flyback or buck-boost converter

The basic flyback or buck-boost configuration, Fig. 4, can be used to invert the input supply. When switch $S$ is closed during $t_{\text {on }}$, current flows through the inductor storing energy. Diode $D$ is reverse biased blocking the supply. When the switch is opened the voltage across the diode reverses polarity. The diode thus becomes forward biased and current flows through it charging the capacitor. Output voltage is therefore the inverse of the input, and may be larger or smaller in magnitude than the supply.
This configuration is known as a flyback circuit as the energy is stored and transferred to the load while the switch is open - the flyback
period. Flyback topologies can cause large amounts of ripple current at both the input and output of the converter. Regulation can be provided by the circuit described previously and output voltage is given by:

$$
V_{0}=-V_{\mathrm{in}} t_{\mathrm{on}} / t_{\mathrm{off}}
$$

## Isolated supplies

Both of the topologies discussed so far do not provide any form of isolation between the input source and the output supply. In the event of a failure, the input supply is passed directly to the output, as with a linear supply. Should it be necessary to provide isolation, as in medical equipment, floating instruments for example, then a transformer is needed.
Control is identical to that described previously, but the feedback arrangement to the error amplifier can be an additional transformer winding or opto-isolator. If complete isolation is not necessary, then a simpler resis-
tive or transistor based feedback circuit will suffice.

## Isolated flyback conversion

An isolated flyback converter arrangement is shown in Fig. 5. Closing the switch allows current to flow in the primary winding. Windings on the transformer are in anti-phase, so diode the diode is reverse-biased and no energy is transferred to the load.

When the switch is opened, voltage on the windings reverses due to the collapsing magnetic field. Being biased on, the flyback diode is now conducting, charging the output capacitor and delivering current to the load.
As a transformer is the energy transfer element, either a step-up or step-down winding ratio can be used to give respectively higher or lower output voltages. Output voltage is given by:

$$
V_{\mathrm{o}}=V_{\mathrm{in}}\left(N_{\mathrm{s}} / N_{\mathrm{p}}\right)\left(t_{\mathrm{on}} / t_{\text {off }}\right)
$$

## The inductor's role in SMPS design

An essential element of a switched mode converter is the inductor. Energy is stored in the form of a magnetic field in the core material of the inductive element during the time that the switching element is on ( $t_{0 n}$ ).
In a switched mode PSU a voltage, $v$, is applied across an inductor, $L$, and the current through the inductor changes with time. This current change is 'impeded' by the inductance - hence the term choke - and is described mathematically as,
$d i / d=V / L$
When the switch is turned off, energy stored in the inductor is released. Magnetic field through the windings collapses as there is no current flow or voltage to maintain it. The collapsing field now 'cuts' the windings, which generates a voltage opposite in polarity to that originally applied. This voltage gives rise to a current flow in the same direction. An energy transfer can therefore take place between the input and output of the converter.
Use of the inductor in this way can be seen as a direct application of Lenz's law. As an aside, at first glance it appears that no energy can be stored 'permanently' in an inductor as with a capacitor. However, imagine an inductor be made of superconducting wire. After being 'charged' and shorted with similar wire; its energy is retained indefinitely as a magnetic field. Readily extracting this energy is a totally different matter.
The amount of energy that can be stored in an inductor is limited by the saturation flux density, $B_{\text {max }}$ of the material that the coil is wound on. This
material is normally a ferrite. When an inductor saturates, the core material can be magnetised no further. The magnetic dipoles within the material are all aligned, and thus no more energy can be stored as a magnetic field within it.
Saturation flux density of the material is affected by temperature, and can be reduced to half of its room temperature value by $100^{\circ} \mathrm{C}$. On a practical front, if the core is allowed to saturate, the current through the inductor is no longer controlled by the inductive effect. It is now limited only by the resistance of the windings and the ability of the source supply to deliver it. In a switched-mode regulator, the maximum on-time of the switching element is usually limited. Current and voltage across the inductor can thus be determined. It is the current change with time that is of interest in an SMPS design. This is given by:

$$
i=\left(V_{\mathrm{in}} / L\right) t_{\mathrm{on}} .
$$

This assumes that there is no resistance in series with the inductor. In practice the resistance of the switching element, inductor, and even the PCB track will limit the maximum current through the inductor. A resistance of $1 \Omega$ is not an unreasonable value to assume. Current through the inductor is now described by:

$$
i=\left(V_{i n} / R\right) \times\left(1-\mathrm{e}^{-t_{m} R / L}\right)
$$

The first plot illustrates the difference in current through a $10 \mu \mathrm{H}$ inductor with no series resistance, and when $1 \Omega$ is added in series. Voltage applied is 10 V . If there is no series 'limiting'
resistance, the implication is that the current will rise to infinity over an infinite period of time. Obviously, this is not possible, but the statement does highlight that the current in an inductor can rapidly reach large and potentially destructive values. This equation only holds true whilst the inductor remains out of saturation.
When the inductor core saturates, the inductive effect no longer keeps the current rise in check. Current will rapidly rise beyond that predicted by the equation. In saturation, the current will limit at a value determined by the series resistance and applied voltage.
Small values of inductor give rise to rapid increases in current, and can store large amounts of energy in a given period. Large inductor values give slower rises in current, but store less energy within the same time. This is demonstrated in the second and third plots, the former showing current rise in $10 \mu \mathrm{H}, 100 \mu \mathrm{H}$, and 1 mH inductors when a 10 V source is applied. Plot 3 shows energy stored over time for the same set of inductors.
In the fourth plot the current rise is shown for the same set of inductors, again with a 10 V source applied but with a series resistance of $1 \Omega$ included. Plot 5 shows energy stored for the same set of inductors. It is clear that the current in the $10 \mu \mathrm{H}$ inductor rises quickly to the maximum of 10A in approximately 50 ms . But because of the $1 \Omega$ resistor it stores only around 500 mJ . However, the $100 \mu \mathrm{H}$ and 1 mH inductor current rises and stored energy are relatively unaffected by the series resistance within the same time period.
where $N$ is the turns ratio between the windings, and $t_{\text {on }}$ and $t_{\text {off }}$ are respectively the switch on and off times.
Additional supplies can be obtained by adding windings to the transformer. Note that voltage regulation of these supplies will be poor, and dependent upon both their load currents and the load of the main regulated supply. If the load demand increases on the main supply, the controller will compensate by increasing the duty cycle to maintain the set output voltage. This will raise the output levels of the additional supplies, and vice versa.
Some degree of regulation is provided due to the flux linkage between the windings. In addition to the disadvantage of high input and output ripple currents, the isolated flyback converter also suffers by having to store high energy levels in the transformer. This leads to a larger core size to avoid saturation as a consequence of the dc currents flowing in the windings.

Fig. 6. Isolated forward converter. Winding Nd is needed for demagnetising the coil. Since duty cycle is always less than $50 \%$ however, ripple at input and output can be high with this configuration.

## Isolated forward converter

With an isolation transformer and an energy storing inductor, $L$, the isolated forward converter looks daunting at first sight because of its plethora of windings. However, the operation is relatively straightforward, Fig. 6. All three transformer windings are on the same
former, with $N_{\mathrm{p}}$ and $N_{\mathrm{s}}$ wound in-phase and $N_{\mathrm{d}}$, the demagnetisation winding, wound in anti-phase.
Firstly, consider only the primary and secondary windings. When the switch is closed current flows through the primary winding $N_{\mathrm{p}}$, transferring energy. Because of transformer



These plots illustrate the effects of inductance. In the first, the effects of adding a $1 \Omega$ resistor in series with a $10, \mathrm{H}$ inductor are shown. How large inductors store less energy in a given time is demonstrated in the second and third plots. In each, three inductors are involved, of $10 \mu \mathrm{H}$, 100 HH and 1 mH . The second plot shows current rise for each, the third energy stored. Plots four and five are identical to plots three and four but with a $1 \Omega$ series resistor.
action a voitage in phase with the primary appears across $N_{\mathrm{s}}$. Diode $D_{2}$ is therefore forward biased (diode $D_{3}$ is off) and this energy is stored in $L$ for transfer to the load.

When the switch is opened the transformer winding voltages reverse polarity and diode $D_{2}$ turns off, while $D_{3}$ turns on. Thus current flows through $D_{3}$ and $L$, delivering power to the load.
Ripple currents at the input can be high as duty cycles are always less than $50 \%$. Output voltage is given by:

$$
V_{\mathrm{o}}=V_{\mathrm{in}}\left(N_{\mathrm{s}} / N_{\mathrm{p}}\right)\left(t_{\mathrm{on}} / T\right)
$$

where $T$ is the total oscillator period.
The purpose of the third winding $N_{\mathrm{d}}$ is to remove any excess energy stored in the transformer. When the switch is closed and current build up is occurring in $N_{\mathrm{p}}$, diode $D_{1}$ is reverse biased blocking any current flow through $N_{\mathrm{d}}$.
Opening the switch causes the voltage across $N_{\mathrm{d}}$ to become negative. Diode $D_{1}$ thus becomes forward biased and current flows back into the input supply. This removes the excess energy stored in the windings and core returning it to the input capacitor, and consequently demagnetises the transformer. If this was not done, the switching elements breakdown voltage could be exceeded at turn-off,
destroying the device. It is normal to have an equal number of turns for the primary ( $N_{\mathrm{p}}$ ) and demagnetising ( $N_{\mathrm{d}}$ ) windings which results in a maximum allowable on/off duty cycle of $50 \%$, i.e. equal on and off switch times. If the duty cycle exceeds this value, then the switch current will rise uncontrollably as the primary cannot maintain zero dc voltage.

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# M \& B RADIO (LEEDS) THE NORTH'S LEADING USED TEST/EQUIPMENT DEALER 





# COMPUTING for real time 


#### Abstract

Unlike office computers, industrial control systems need to respond a number of stimulii simultaneously. William Dickinson* and Alwyn Breame* discuss the special hardware and software that has evolved to cater for minimum response time.


n the area of industrial control systems, demand for more features, higher performance and greater reliability is growing rapidly. Industrial systems are now routinely called upon to perform tasks in realtime that were unimaginable only five years ago.
The term computing platform describes a collection of elements. As well as the hardware, operating system and applications software, it encompasses the architecture of the project and quality management systems. Real-time simply means that the computer system has the ability to acquire information and process it faster than any changes of interest.
Real-time systems tend to be one-offs or high-end products manufactured in low volumes. Developing software for these systems is costly because of the intricate structure of $\mathrm{i} / \mathrm{o}$ hardware, interrupts, the CPU and associated software. To fully appreciate the complex interactions within such systems needs significant hardware and software skills.
A system designed to measure growth of a
blade of grass and another tracking an aircraft at Mach- 3 can both be considered to be realtime operating system. The only difference is the rate at which data is processed. Monitoring grass growth puts considerably lower demands on the hardware and software than tracking the aircraft.
In real-time systems overtaxing the CPU leads to critical events passing by unseen or distortion of the time references between events. In the early stages of development, this may manifest itself as a series of frustratingly intermittent and equally indeterminate problems. In the latter stages it will result in system failure.
The trick is to design the computing platform with this in mind. When overtaxing occurs - and it will sooner or later - shifting the software to a more capable platform will not cause excessive costs and time penalties. The best application software is written by a single programmer for running on a single CPU. However the complexity of many projects often precludes this approach.
Dividing the software into discrete run-time

## Single tasking

This diagram illustrates the typical run-time environment of a single-task operating system such as MS-DOS. It is possible to construct real-time systems within this environment but the programmer must create a scheduler if the application cannot tolerate the traditional 'round robin' approach to sequential program module execution. While Windows provides a pseudo multi-tasking environment through the use of a cooperative scheduler it is generally unsuitable for real time applications due to the lack of control over the windows scheduler.
If debug or functions F2 or F3 uses too much CPU time, function F1 will miss real-time events. The slowest loop iteration time must always be faster than the real-time stimulus and control reactions.
Blocks F1 to F3 are user software functions executed sequentially like a train passing several stations along its track. The software is usually maintained in separate source files with associated libraries. The sources are compiled to form a single monolithic program for the run-time environment.
Debug is typically a set of resources developed by the programmer to monitor, and often control, functions 1 to 3 at run time. A typical debug program would allow a VDU to be attached to a serial port and provide resources to monitor and control the run-time functions.

modules simplifies compliance with quality management system (QMS) audits. Both development and run-time environments should allow the software to be partitioned into separate, independent function blocks.
Ideally the software modules will be able to run without the real $\mathrm{i} / \mathrm{o}$ hardware being present. Hardware system actions and responses may then be simulated by software in order to introduce the variability that often causes software models to fail. Being able to develop the software before the hardware saves time. Warranty support costs are also reduced as problems can be simulated under controlled conditions in order to locate the software defect.
In summary, design features of the computer hardware, operating system and applications software should be chosen on their combined ability to cope with real-time data acquisition, changes and updates in specification, modular software design and integration of several programmers. Additionally, the project management and QMS should be able to adapt quickly to the predestined changes that will take place and be capable of auditing the performance of the software as it evolves.
These requirements deter the use of systems with only one CPU. A single processor restricts expansion capability. It limits you to single-task operating systems and monolithic programs that poll $\mathrm{i} / \mathrm{o}$ in all but the smallest of projects. In order to successfully manage, isolate, test and debug the software in a complex real-time application, a multi-tasking operating system with comprehensive intertask communication resources becomes an essential requirement.
Memory designs are critical to the overall
reliability of industrial systems, particularly those that deal with safety related issues. The storage element of dram is a capacitor which is recharged during refresh cycles while that of static ram is a flip-flop. There is a considerable difference in reliability between the two. Static or dynamic ram with error detection/checking and correction is essential to ensure reliability in unattended or safety related systems. In very demanding applications the application software may be committed to read only memory. Modern flash EPROM makes software upgrades a simple process.
To allow easy maintenance and upgrading, the computer hardware should be bus oriented. The ability to expand the hardware platform using distributed processing through Lans is also beneficial. These can be used to provide intelligent front end systems which divide up the real-time data acquisition and processing amongst several CPUs. Distributed processing can also eliminate a lot of cabling by placing the computer hardware near the i/o devices they serve.
The operating system should provide a multi-tasking environment for the application software and the ability to alter process priorities. It should also have vectored hardware interrupts for data acquisition and convenient standardised mechanisms for interprocess communication as a minimum. Above all else the operating system should assist the formation of effective barriers between the costly application software and the physical nature of the hardware implementation. This involves more than just programming in C with $\mathrm{i} / \mathrm{o}$ interface libraries because this does not remove the close relationship between the

## Real-time, hands on

For readers wanting to delve further into real-time computing, we are publishing an article describing specifically-designed multi-tasking system in the next issue. The hardware is a 68020-based single-board computer, the software OS-9/68020 Professional.
applications software and the underlying hardware architecture.
Without effective separation between the software and its physical environment a massive and costly re-write of the application software will be required if the single CPU ever runs out of steam. If this interface is implemented properly the application software will be impervious to changes in the hardware environment.

## VME and OS9

VME bus systems incorporating the Motorola MC680xx family of processors and the Microware OS9/680xx operating system were designed from the ground up for real-time industrial control applications. This operating system is multi-tasking - and hence multiuser. A PC/dos combination is anywhere between one half and one twentieth the price of a VME/OS9 system. The problem with this simplistic comparison is that it assumes the hardware platforms and operating systems are equally capable and the software development costs within the two systems will be similar. This is not the case.


## Multi-tasking

A typical run-time environment of a multi-tasking operating system that uses a preemptive scheduler such as OS9 is shown here. Each of the user software functions, F1 to F3, may be allocated CPU time as required by

## the application.

If function F2 or F3 uses too much CPU time function F1 may miss realtime events. In these circumstances the programmer alters the process priorities. This may be done while the software is running.
Functions F1 to F3 are userdetermined soft ware modules. These are time-sliced by the pre-emptive scheduler which will typically allocate a maximum of 10 ms of CPU execution time to a task before it is switched out and a new one switched in. If the running task has nothing to do, for example while waiting for an input to change state, it may relinquish the remainder of its timeslice to improve the overall efficiency of the system.

Through its file managers, device drivers and device descriptors, the
operating system provides effective isolation between the application code within the three function modules and the hardware environment. This allows major alterations to occur within the hardware environment without having to alter the applications software, which is typically the most complex and difficult to modify.
The inter-process communications resources of OS9 enables programmers to quickly attach VDUs and other debugging resources to the run-time software modules using standard system resources. If the functions are properly designed they may, be run, tested and debugged in isolation from one another. They may also be run without the need for real i/a hardware. Additionally, they can have their internal local variables monitored and altered by the attached debugging resources. The resources within OS9 enable programmers to construct generic debug tools that will work with a wide range of application programmes.

## What is VME?

VME is an acronym for Versabus Module, Eurocard. It is an open architecture computer bus pioneered in 1981 by a consortium formed by Motorola, Mostek and Signetics. It was developed to support the VERSAbus developed by Motorola in 1979 on the emerging Eurocard PCB standard IEC297-3.

Although VME bus has its origins in the Motorola $680 \times x$ family it was designed to support a wide range of processors and was standardised in IEEE 1014 and IEC821.
VME bus is supported by hundreds of suppliers with thousands of boards. It has several extensions, eg VXI, VSB, VMX and VME64 which all use the basic VME bus in different ways to support a wide range of applications. For further information contact VMEbus International Trade Association (VITA), PO Box 192, 5300 AD Zaltbommel, The Netherlands.

## OS9

Modelled on Unix version 7, OS9 was developed by Microware Systems Corporation in the US. This version of Unix was the last 'small' version and made a suitable basis for a real-time system. Microware coded the kernel to be compact with an efficient mechanism for pre-emptive task switching. There is no support for virtual memory and no disk swapping which lead directly to high speeds.
The operating system, output from compilers and utilities lend themselves to being ROM based. They can also be position independent without needing special switches. This makes the production of small embedded systems quite simple.
At startup, the kernel searches through memory looking for 'modules' which may be in RAM or ROM. Tables are then constructed to form the run-time operating system making the system fully dynamic. OS9 will only run on 680xx processors but in the form of OS9000, it also runs on the 80386 and other processors.
Inter-process communication mechanisms supported include files, pipes, signals, events, semaphores and data modules. The system tick provides pre-emptive scheduling. Via a user definable process priority mechanism, this allows high priority tasks to obtain more of the CPU resource than others at a lower process priority. There is also an 'ageing' procedure which guarantees a low priority task some resource.
OS9 is low cost, compact, extremely efficient. It suits applications from small embedded instrument controllers to large networked factory automation and management information systems. There are very few operating systems capable of such a wide range of applications. Network connections between OS9 machines, Unix machines, PCs, VAXs, etc., are straightforward.
The ability to temporarily incorporate editors, compilers and debuggers within the target hardware during software debugging and enhancement considerably improves software productivity.

It is noteworthy that of all the CPUs and real-time operating systems available, Sony and Philips chose the Motorola MC680xx and OS9 for their Compact Disk Interactive (CD-I) systems.

Firstly, the VME system will be physically constructed and tested to withstand the rigours of industrial applications. VME hardware is commonly used in military and aerospace applications. Since industry demands stability and continuity most hardware is available, unchanged, for a considerable period of time. Hardware based on VME is also flexible and modular. It is quite easy to construct a system with more than 300 slots for i/o boards if necessary.

The VME bus architecture was specifically designed to support multiple bus masters. Program memory may be rom, sram or dram with error detection and correction for reliability. VME systems may use SCSI disk drives with internal caches and an interleaving DMA controller. These release a significant amount of CPU resource.
Dedicated graphics processors with in-built resources to manage windows, draw lines, etc., again relieve the main CPU. While it is possible to use a PC for graphics you will be restricted to a narrow range of suppliers. In addition the cost of specialised hardware will approach or exceed that of VME bus hardware. Further, due to the rapid evolution of the PC market, it is unlikely that you will be able to buy the identical hardware in a few years time.
On the software side, C compilers for PCs are generally supplied with 'hooks' into the graphics and disk file management system. In addition there are many support 'tools' for the PC graphics environment that make developing the graphical user interface (GUI) easy.
OS9 is normally supplied configured for a specific processor board for a development system. Its user interface, modelled on Unix, was designed to be used with conventional

## PC operating systems

MS-DOS. This is a single task operating system which leads to monolithic programmes which are difficult to debug and maintain. Metrics are very difficult to produce in all but the smallest of applications. The Windows add on will give a degree of multitasking but inter-process communications become problematical and a 'roll your own' methodology naturally follows. OS2 has multitasking capability with a preemptive scheduler and many features required for a real time operating system. Size of the operating system causes problems in small applications as does the lack of support for ROM application code.

OS9000. Microware has recoded OS9 in ' C ' and is available for 680 xx and 80386 processors. OS 9000 has all the features of OS9. If the PC architecture has to be used in an industria! environment, one should use an industrial processor on a VME card with EDAC memory and use OS9000. The price would be very similar to OS9 and 680xx systems.

RS232 terminals. The supplied 680xx assembler and C compiler have 'hooks' into the considerable resources of the operating system.
Designed to provide a unified i/o system, the OS9 file manager, or FMS, has an uneasy relationship with graphics, digital and analogue $\mathrm{i} / \mathrm{o}$. As a consequence there is a lack of 'enforceable' standards in these areas. Integrating additional hardware into the memory map and interrupt architecture of a VME/OS9 system is not a trivial task.

When programmers first attempt to work with VME systems and OS9 they are confronted with several learning curves. Progress is often perceived as being slow as

## Glossary

C - the most frequently used processor and operating system independent programming language outside of ADA which is used in military and aerospace applications.
Cooperative describes a scheduler that usually relies on system calls rather than interrupts to form a multi-tasking operating system. Such a system will continue an execution thread until the system call is completed and then switch tasks. Such constructions are generally unsuitable for real-time applications. ECC, EDC or EDAC - error checking and correction, error detection correction, error detection and correction. These are the various techniques used to improve the reliability of dynamic RAM. When errors occur the system has the resources to not only detect the error but also correct it.
DMA is direct memory access. It is hardware that can perform memory to memory or memory to peripheral transfers without involving the main processor. As there are no program instructions to execute, these transfers are very fast and may be hidden in unused processor bus cycles.
Embedded controller is a small SBC with dedicated i/o hardware to serve a specific purpose, e.g. control of a digital voltmeter,
oscilloscope, washing machine, car engine, etc. GUI - graphical user interface. It is the most frequently used method of forming a man-machine-interface or MMI.
MIS - management information system. This is a system which obtains information from a manufacturing environment, processes it and presents it in a manageable form.
Multi-tasking is the ability of a processor to execute several programs 'simultaneously'. This is usually done via a cooperative or pre-emptive scheduler.
Pre-empting is the action of a scheduler used to construct a multi-tasking operating system where, typically, an interrupt is used to terminate execution of the current program and start/continue execution of another. Interrupts make this an ideal basis for real-time applications.
QMS - quality management system. A system designed to maintain and steadily improve the quality of the end product or service.
RUN-TIME - the operating environment.
SCADA - supervision, control and data acquisition. Computer and often PLC based systems that perform control and MIS functions. SPC - statistical process control. A technique whereby the trends of a large population of product can be evaluated using sampling techniques.
there may be little to show after many weeks of work. Having said all this it is quite easy to construct a monolithic program under OS9 that completely circumvents the operating system and directly accesses the I/O hardware.
The features that provide VME systems and OS9 with their power and flexibility can be extremely frustrating to programmers conditioned by the ease of integrating hardware into, and programming within, the single task PC environment. However, systems integrators, many VME suppliers and Microware Systems (UK) can provide considerable assistance.
The multi-tasking and inter-process communication resources of OS9 will assist
programmers in adopting a structured and considerably more disciplined approach to software development. Changes in specifications that occur during software development become far easier and less costly to manage. Provided the software is designed properly, moving a complex real-time application to a radically different hardware configuration will be commercially viable.
Resources within OS9 enable quality management to easily measure the performance of software at each stage of its construction thereby improving quality. The productivity and quality improvements quickly recoup the price difference between PC/MS-DOS and VME/OS9 systems.

## Hardware/software sources

For information on OS9, Microware Systems (UK) Limited, Leylands Farm, Nobs Crook, Colden Common, Winchester, Hampshire SO2 1 TH. Telephone 0703 601990, Fax 601991 OS9NME hardware and software, Windrush Micro Systems Ltd, Station Road, Worstead, North Walsham, Norfolk NR28 9SA. Telephone 0692 404086, fax 404091.
VMEbus, VMEbus International Trade
Association (VITA), PO Box 192, 5300 AD Zaltbommel, The Netherlands.

## Real time operating systems

Real-time operating systems currently available includ e,

| LynxOS | $680 x x$ and 80386 and others |
| :--- | :--- |
| OS9 | $680 x x$ only |
| OS9000 | $680 x x$ and 80386 and others |
| PDos | $680 x x$ |
| PSOSt | $680 x x$ |
| Unix | too many to name |
| VMEexec | 68020,68030 and 68040 only |
| VRTX | $680 x x$ |
| VxWorks | $680 x x, 80960$, Mips and others |

Clearly this is not exhaustive but give the general impression that the $680 x x$ family is most commonly used for industrial real-time control applications. Most have used Unix as the user interface model and often the virtual memory model.
The more you look into real-time systems the more you will find that they are all very much alike. They all try to solve the problems of realtime by using a small kernel and additional features to provide extra functionality. All claim to be the best real-time solution. The differences, mainly price, are very small compared to their similarities. The things to look for are the range of processors supported, modularity of the operating system, hardware isolation mechanisms and network support.
The cost of many of these packages is quite high and often requires a host, like a Sun workstation, to do the editing, compiling, etc. The code is then copied to the target. Debug facilities are available either via serial communications or a network. This approach aggravates the time scales of real-time software development, often resulting in an empirical approach to resolving problems.

LynxOS is available on a variety of processors and conforms the POSIX 1003.1 standard and is compatible at the source level with 4.3 BSD and System V Unix. The real-time extension complies with POSIX 1003.4 and threads interface to POSIX 1003.4a. LynxOS provides a mechanism whereby process priorities can be modified resulting in high priority tasks obtaining more of the CPU resource.
Inter-process communications mechanisms provided include pipe, files, messages, semaphore and signals which give a suitable vehicle for most requirements. LynxOS supports demand-paged virtual memory which impacts the real time performance but the user can select the priority of these processes but can execute programmes larger than memory allows. There are LynxOS tools which allow LynxOS to be rom based.

PDos was designed for Motorola $680 \times x$ (including the $683 \times x$ ) processors and has a deterministic real-time kernel for handling system startup, exception processing, inter-process communications, basic i/o management and memory resource allocation. There is a monitor module providing a command line interpreter. This allows basic functions like file/disk, memory and task management, including alteration of task priorities. The debugger module is non intrusive. It may be accessed from the monitor and supports single stepping, multiple break points and modifications of memory and CPU registers. PDos supports binary semaphores, shared memory modules and ram disks for inter-process
communications. A maximum of 127 tasks are can be set up. Networking to other machines is via TCP/IP protocols and includes telnet and ftp.

PSOS+ was specifically designed for embedded applications using custom hardware. The kernel provides process management, memory management and inter-process communication mechanisms. The operating system is highly modular with additions including file managers for disk and terminals and networking. Inter-process communications include all the standard mechanisms. The ADA runtime system can be supplied with an ADA compiler. Smalltalk is also an option. PSOS +3 is available for $680 \times x, 88 K, 80386 / 486$ and several other processors.

Unix, although multi-tasking, is not capable of real-time operation in its standard form. While various extensions are available for Unix to enable it to cope with real-time activities these are not part of the Unix specification and vary considerably from vendor to vendor. Unix originated with the Multics project jointly developed by General Electric Company and Project MAC of the Massachusetts Institute of Technology. The aim of this project was to provide a 'multi-user service' to a wide range of users. Unix was developed by Bell Laboratories when they ended participation in Multics. Although Unix is multi-user, it is not generally suitable for real-time processing due to timing problems. There is a plethora of 'real time' Unix systems which support many of the features of real time processing.

VMEexec provides the task management, meniory management and inter-process communications mechanisms. These inter-process communications systems include queued messages, events, signals, semaphores and shared memory. Additions to the kernel include access to serial communications, disks and networking. Target processors 68020 and above.

VRTX supports device independent $\mathrm{i} / \mathrm{o}$ for most devices. The C compiler libraries provide modules for real-time operations. The operating system has priority-based, pre-emptive task scheduling. A range of inter-process communications mechanisms is available for messages, counting semaphores, mailboxes, events and sharing memory. Streams based open networking is an option, as is TCP/P, BSD sockets and NFS. Supported processors include 680xx, Sparc, Mips, i960 and 683xx single chip alternatives.

VxWorks provides the fundamental operating system primitives of multitasking, pre-emptive scheduling and inter-task communications. Its interrupt driven priority based scheduling supports 256 priority levels, allowing a high priority task to pre-empt a lower one. Inter task communications include semaphores and shared memory data. Networking is via TCP/IP,NFS and others to allow data to be passed between VxWorks and Unix, etc. Many debug aids are provided including a symbol ic debugger which allows easy debugging of the code across a network using the RPC protocol from another Unix machine. Processor support is very wide covering most $16 / 32$ bit Cisc devices and some of Risc processors. Among these are 680 xx , Sparc, Mips, 1960 and 683 xx.

## The versatile world of

> Operational transconductance amplifiers can introduce programmability into almost any conventional fixed gain circuit. Multipliers, VCAs, VCOs and voltage controlled filters are all in the design repertoire. By Dan Ayers.
n the pre-semiconductor days, a figure quoted for valves was the ratio of change of anode current to change of grid voltage. This value was known as mutual conductance $\left(g_{\mathrm{m}}\right)$, and allowed the designer to predict the current or voltage gain of a particular circuit. Owing to the prevalence of voltage in, voltage out building blocks, transconductance (now quoted in Siemens, $S$ ), is only occasionally encountered. This is rather surprising when one considers that transistors are essentially voltage in-current out devices.
The $g_{\mathrm{m}}$ model of the transistor, derived from the hybrid-pi model ${ }^{1}$, is shown in Fig.1. In common-emitter mode, the base receives an input voltage which the transistor converts to a current at the collector. This current is usually fed into a resistive load, thus giving a voltage output. One can therefore consider the $g_{\mathrm{m}}$ of a transistor as a figure of merit, related to the $h_{\mathrm{fe}}$.
Since the $g_{\mathrm{m}}$ is roughly proportional to the emitter current, it follows that if we supply the emitter current with another voltage to current converter, we have a voltage controlled gain cell. The simplest version of this is shown in Fig. 2a. Despite having a limited operating region, this arrangement lends itself to rf modulation when loaded with a tuned circuit to discriminate the desired product.

Extending the transconductance principle a little further yields the operational transconductance amplifier (OTA). In general, an OTA is an op-amp whose output current is proportional to the voltage difference between the input pins. An extra pin ( $I_{\text {set }} I_{\text {bias }}$ or $I_{\text {abc }}$ ) on OTA chips allows variation of $g_{\mathrm{m}}$. An OTA with a resistive load can be considered to be an op-amp with open loop gain $A_{0}=g_{\mathrm{m}} \times R_{\text {load }}$.
Figure $\mathbf{2 b}$ reveals how a simple OTA operates. A long tail pair, LTP, provides differential input, as in a conventional bipolar op-amp. Two current mirrors, $M_{1}$ and $M_{2}$, serve as active loads for the input transistors. Current into $M_{2}$ is directly echoed to the output, whereas the current from $M_{1}$ is mirrored again to give a single ended output. The current from mirror $M_{3}$, set by the control input, determines the emitter current of the input pair, and consequently the gain. A functional diagram of an ideal OTA is shown in Fig. 3.

## IC transconductance amplifiers

The CA3080 OTA owes its longevity to simple but versatile design. Devices such as the LM13700, Fig. 4, have significantly better specifications. The internal circuitry of the CA3080 differs only a little from that of Fig. 2 b , and adds significant harmonic distortion to signals above a few tens of millivolts. The cir-


Fig. 1. Transconductance model of a transistor
cuit of Fig. 5 produced the transfer function of Fig. 6, which has a curve remarkably close to a section of the sine function, making the cir cuit useful as a triangle to sine wave converter2.
Low distortion from the CA3080 is usually achieved by attenuating the signal before the device and using subsequent stages to restore the amplitude. An undesirable byproduct is a degradation of the signal to noise ratio. This distortion/dynamic range problem has been partially tackled in the LM13700 which has a diode network to linearise the chip's response for larger signals ( 10 dB improvement in $\mathrm{s} / \mathrm{n}$ referred to $0.5 \%$ THD). The same device also includes two darlington pairs, whose collectors are internally connected to the positive supply pin. These can act merely as buffers or play a more active role in circuits as separate gain elements.

## Practical applications

The current output of OTAs make them ideal for circuits involving signal summing. One can simply wire the outputs of separate devices together to share the same load. The summing and gain control capabilities of OTAs are perfect for the core of a multiplexer, where applying a current to the appropriate $g_{\mathrm{m}}$ control pin selects one of several inputs. The CA3080 has an extra benefit here: its standby power demand is only $10 \mu \mathrm{~W}$.
The $50 \mathrm{~V} / \mu \mathrm{s}$ slew rate of OTAs makes them usable for high frequency amplification and switching applications. The current output also simplifies impedance matching to cables, as the OTA load is the output impedance.
Since the gain may be remotely set, it is


Fig. 3. Functional diagram of an OTA


LM13700


Fig. 4. Devices such as the LM13700 have significantly better specifications. The internal circuitry of the CA3080 differs only a little from that of Fig. 2b, and adds significant harmonic distortion to signals above a few tens of millivolts.
straightforward to design voltage controlled amplifier circuits such as Fig. 7a. A few extra components bring the linearising resistors into play as in 7 b . This modification can be made to any of the following LM13700 circuits
OTA chips already configured as VCAs are available, such as the SSM2024 quad current output VCA. This device is optimised for audio and musical instrument work and offers $82 \mathrm{~dB} \mathrm{~S} / \mathrm{N}$ at $03 \%$ THD. A 4 k 7 pot wired to the power rails, with a $1 \mu \mathrm{~F}$ capacitor shunting the wiper to ground (local to the VCA) will supply a virtually noise-free control voltage
and can be as far away from the mixer amplifier as demanded without loss.

## Multiplier mixer

The VCA behaves as a two-quadrant multiplier, the output being the product of the input and a positive control. When one wishes to multiply in all four quadrants, where the control has values of both polarities, one may also apply transconductance techniques ${ }^{3}$.
Where precision is not a key factor, standard OTAs are ideal. Using a VCA circuit and making a resistor connected to one of the sig-


Fig. 5. Circuit to demonstrate nonlinearity of CA3080

## CA3080 Mon-Linearity



Fig. 6. CA3080 nonlinearity compared with sine function (actual measurements, scaled) using the circuit shown in Fig. 5.
nal source act as part of the OTA load, the input and control will be multiplied at the output. Several analogue music synthesizers featured modified VCAs with circuitry to cancel out two-quadrant products as ring modulators. Even when the CA3080 is wired as a VCA, this chip has four-quadrant multiplication products at its output because of its nonlinearity.
An unusual use of this function is in a bat detector, Fig. 8. Bats employ a sonar system to avoid obstacles and locate prey, a system as much as $10^{12}$ times more efficient than sonar contrived by humans ${ }^{4}$.

A standard ultrasonic transducer $(32 \mathrm{kHz}$ in the prototype) will pick up bat squeaks (usually around 16 kHz to 150 kHz ), which are amplified by $A_{1}$. A highpass filter with cutoff around 20 kHz then removes audible noise $\left(A_{2}\right)$. Wein bridge oscillator $A_{3}, A_{4}$ produces a sine wave with a range of around 20 kHz to 120 kHz . This reference modulates the bat signal in the OTA $\left(A_{5}\right)$. Op-amp $A_{6}$ converts the current output of the OTA back to a voltage. The signal now contains not only the two frequencies fed into the CA3080 but also components at their sum and difference. The sounds from the bat, the signal from the reference oscillator and their sum should all be well above the 10 kHz low filter, $A_{7}$, leaving only the difference signal. The prototype had two PP3s as power supply, and included a


Fig. 7a (left) Basic voltage controlled amplifier and the addition of linearising resistors ( 7 b , right)



Fig. 9. Low pass filter using voltage controlled resistance. Grounding the input and feeding the signal through a capacitor to point $X$ produces a tunable highpass filter.

TBA820 amplifier, although a high impedance earpiece would suffice. The correct functioning of the prototype loudly demonstrated itself by ultrasonic emissions from a nearby video monitor. If this configuration looks familiar to radio enthusiasts, it is because the circuit is effectively a direct conversion receiver.
There is a great deal of potential for any device that can represent signals out of the range of human senses (and that of typical measuring equipment) to an accessible form. For instance, plants make ultrasonic gurgling noises when they begin to run out of water ${ }^{5}$. American researchers have even designed control equipment for timber drying kilns that changes the drying temperature according to ultrasound generated by microfracture in the wood structure.

## Filters

In many circuits it is possible to replace existing components with OTA circuitry and thereby introduce voltage control of otherwise fixed parameters. A simple application of this is to replace the $R$ of an $R C$ lowpass filter with an OTA, as in Fig. 9. Grounding the input of this circuit, and feeding the signal through a capacitor to point X (omitting the existing capacitor) produces a voltage controlled version of the $R C$ highpass filter. Like their passive counterparts, one may cascade stages to increase the order of the filter.
The circuit of Fig. 10 was designed to find the best frequency for a loudspeaker crossover for given speakers. A voltage controlled filter with a 2nd order Butterworth response is constructed around the OTA. The lowpass output is then subtracted from the input signal to give a highpass output. The crossover frequency of the complementary outputs can be moved over the range of around 250 Hz to 2500 Hz . In this circuit, as in the other filter circuits featured here, one can change the frequency range by scaling capacitors.
Active differentiators and integrators may be easily constructed with OTAs, with the advantage that their time constant is voltage controlled. The versatility of the standard dualintegrator state variable filter increases with

the addition of voltage control, as in Fig. 11. The Q may by adjusted by changing $R_{\mathrm{Q}}$ (adding another OTA here would give voltage control of Q ). With the values shown, the centre frequency range is roughly 150 Hz to 7.5 kHz . Coupled to a sweep generator, this would allow plotting of system output against frequency. With the circuit tracking a swept sine wave, distortion against frequency could be plotted from the notch output.
By adding frequency dependent components to the feedback path of the simulated resistance in Fig. 9, reactance may be synthesized, the reactance appearing between $X$ and ground. A circuit with more interesting possibilities is shown in Fig. 12. If a reactance is
placed at the input port, its reciprocal appears at the output port. This gyrator-type circuit gives a simulated reactance that is fully floating - as long as the differential voltage does not exceed the voltage range of the LM13700 - and has a value dependant on the control voltage.

## VCO

Minor structural changes to the OTA state variable filter produce a good quality voltage controlled oscillator. The circuit of Fig. 13 generates a sine wave with a frequency range between 100 Hz and 1250 Hz . Although this circuit has a range considerably narrower than the circuit given in National Semiconductor
data, it uses one LM13700 rather than two. If an op-amp buffers the output, and the preset adjusted to give 4 V p-p output, the distortion is in the region of $0.01 \%$ at 1 kHz , an order of magnitude better than the NS circuit.
With a little experimentation it is possible to build voltage controlled versions of many standard op-amp circuits. For example, the standard triangle/square wave oscillator becomes voltage controlled by little more than substitution of OTAs for op-amps and tweaking of circuit values. Similarly, an op-amp Schmitt trigger transforms to an OTA Schmitt with voltage control of hysteresis.
One final word. OTAs have a frustrating vulnerability to current overload on their control pins. Connecting the control of a CA3080 to ground without a limiting resistor will instantly destroy the chip. You have been warned.

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Fig. 12. Gyrator-type circuit transforms reactance


Fig. 13. Low distortion voltage controlled oscillator

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Of all transmission modes for plain speech, single sideband suppressed carrier is the most spectrally efficient. Richard Hosking presents a design study based on the polyphase RC network, the heart of a simple SSB receiving system which may be used reciprocally for transmission.

## Polyphase direct conversion

The direct conversion receiver has become popular with radio experimenters, particularly on the HF bands where SSB and CW are common communication modes. A simple receiver can be realized using a mixer and local oscillator at signal frequency, followed by a high gain audio amplifier. The system is simple but has significant drawbacks for the serious user. The opposite sideband or 'audio image' cannot be filtered out and hum and microphony can be a problem.
Phasing techniques were once commonly used to generate and receive SSB signals, Fig. 1. This system can be used to eliminate the audio image, one of the major drawbacks of the conventional direct conversion receiver.
The difficulty with phasing systems has always been producing accurate $90^{\circ}$ phase shifts over suitable RF and audio bandwidths. For example, to achieve a sideband suppression of 60 dB , a phase and amplitude accuracy of $0.1 \%$ is required.

## RF phase shift networks

RF quadrature networks are usually simple passive systems, accurate over only a limited bandwidth. Passive quadrature networks which work over a decade of bandwidth or more with acceptable accuracy are available but at a price.


An accurate, broadband RF quadrature generator can be produced using a dual edge triggered flip flop such as the 7474. (Fig. 2) This circuit has several advantages over passive phase shift networks. It operates from DC to the limit of its clock speed and, because it is edge triggered, it acts as a filter to remove AM noise and other spurii from the LO signal.
Using $74 F$ series devices this circuit will work up to 25 MHz ( 100 MHz clock). If 74ACT series devices were used it should be possible to achieve 40 MHz output with a quoted clock speed of 160 MHz . Phase accuracy of this circuit depends on minimising differences in propagation delay in the flip flops and surrounding circuitry; circuit layout and symmetry in the RF sections is important. For instance, a 25 mm difference in track length
between the two RF quadrature signals would produce a phase error in the order of $1^{\circ}$ at 30 MHz , which translates to a maximum sideband suppression of 40 dB .

## Audio phase shift circuits

All-pass networks using op amps or passive components provide the traditional route to audio phase shift in SSB circuits. Phase accuracy is approximately proportional to component tolerance and thus it is difficult to realize sideband suppression better than about 45 dB at $0.5 \%$ component accuracy. This type of circuit restricts audio bandwidth to about a decade.
The Polyphase network was first described in the 1970's as an alternative to the conventional all pass network. It is a passive network

## Polyphase phase shift network

T-he four inputs to the polyphase network are fed from a low impedance source with audio at $0,90,180$ and 270 degrees. If a phase pair is reversed, ie $180,90,0$ and 270 , then the audio signal is cancelled.
For maximum output two or four phases are terminated into high impedance such as a voltage follower and the outputs of these are summed in a differential amplifier. In this case the sideband cancellation occurs outside the network in the summing amplifier. Network loss is about 6 dB and does not increase significantly with increasing number of poles as long as the network is terminated in a high impedance.
Alternatively the outputs from the four phases are tied together in pairs and fed to a differential amplifier. In this case cancellation appears to occur in the network. Network loss is greater at about 12 dB but the sideband suppression does not appear to be significantly different using this termination.
Each section of the network has a pole frequency $f_{p}$ of

$$
f_{\mathrm{p}}=1 / 2 \pi R C
$$

Poles are spaced equally on a log scale across the desired bandwidth, which is easily increased by adding more sections. Using eight sections with the values shown delivers
an audio bandwidth of 300 to 8000 Hz . Note that the capacitors can be all one value and the resistors varied if desired. The practical network used $1 \%$ metal film resistors and $5 \%$ MKT capacitors. The network may be used in reverse to generate accurate audio quadrature signals for an SSB exciter.

with resistors and capacitors connected in a ring configuration.(See box) It is also known as the 'four path' method. Each path is cross coupled with adjacent paths, maintaining $90^{\circ}$ phase difference between the paths. This property tends to cancel phase errors due to component tolerance and the sideband suppression possible with this circuit approaches 60 dB , an order of magnitude better than with conventional all-pass networks. (Macario and Mejallie)
Experiments and computer simulations were performed to assess the effect of a single $10 \%$ component error on sideband suppression. The maximum effect occurred when the affected component was in the first section of the network where sideband suppression was degraded from about 60 to 40 dB . In the second section the effect was less but still measurable while at other locations within the network the reduction in sideband suppression was minimal.

Fig. 1. SSB phasing receiver. Two mixers are fed by local oscillator signals in phase quadrature. This produces two audio signals of equal amplitude and frequency but $90^{\circ}$ out of phase. The phase relationship of the two audio signals is reversed when changing sidebands. An audio phase shift network produces a further $90^{\circ}$ phase shift of one signal relative to the other. When the two signals are summed, audio from one sideband is cancelled while the other is added, thus producing a single sideband receiver.


Fig. 2. Flip Flop quadrature generator. The IO signal at four times the output frequency is connected to the clock inputs of both flip flops. The flip flops are connected in a ring as a divide by four Johnson counter. One flip flop is 'chasing' the other but lagging by one clock cycle due to propagation delay. The result is two signals in phase quadrature at one quarter of the clock frequency.



Fig. 4. Receiver front end.

Polyphase network bandwidth may be extended by adding more sections, a major advantage over the all-pass network where it is difficult to produce more than about a decade of bandwidth.

## Mixer design

The mixer is crucial in any receiver and especially so in a direct conversion system. The goals for mixer design must include strong signal handling ability; any nonlinearity here will manifest itself as envelope detection of interfering signals which can't be removed by subsequent filtering. The direct conversion receiver has additional considerations due to the high audio gain which follows the mixer.

These sets are particularly susceptible to 50 Hz mains interference from local oscillator hum modulation or via earth currents in the antenna. The first problem is reduced by a good quality local oscillator and, in this receiver, by the flip flop circuit. The receiver operates at one quarter of the local oscillator frequency which reduces LO radiation to the mixer input. Also the flip flop effectively reduces AM noise from the LO signal.

Antenna 50 Hz earth currents can be reduced using isolators or simply a balanced mixer input and output to reject common mode signals. Ring diode mixers were tried but hum was a problem due to their single ended inputs and high post mixer audio gain requirements. The NE602 active mixer provides a compromise solution at reasonable cost.

This device uses balanced inputs and outputs and provides conversion gain and a good noise figure through an inbuilt RF amplifier and active mixer. The distribution of gain between RF and audio reduces the microphony problem. The NE602 does suffer however from poor strong signal handling with a third order intercept of -15 dBm because it incorporates RF gain and low power design. Strong signal handling would be greatly improved by using a high level mixer such as the SL6440 but I have not investigated this. In practice strong signal handling when using the NE602 is not a problem provided that an attenuator is used on the lower hf bands.


## Receiver circuit

The antenna is coupled through a bandpass filter and balanced transformer to the inputs of the mixers. The local oscillator is level shifted and squared up by the 74 F14 before being fed to the 74F74. Sideband switching is accomplished with a 74LS157 multiplexer. Figure 3 shows the block diagram of a practical receiver, and Fig. 4 the front end circuit. The polyphase section of the receiver is shown in Fig. 5.
To achieve good noise performance, SSM2017 audio amplifiers were used following the mixers. The amplifier inputs are balanced which matches the NE602 outputs. The device is set up with a gain of 100 as a compromise between sensitivity and overload performance. A capacitor across the inputs to the amplifier improves strong signal and noise performance by providing high frequency rolloff.
The amplifier sections feed into a phase splitter circuit to drive the four inputs of the polyphase network. The gain of one amplifier is adjustable to allow accurate amplitude balance. The outputs of the polyphase network were tied together in pairs and buffered with voltage followers feeding a differential ampli-
fier. With this arrangement there is no need for accurate amplitude balance in the summing amplifier. A low pass filter follows the buffer. This is a 5 -pole Sallen-Key design with a cutoff of 2.7 kHz and flattest amplitude response.
Note that the frequency response of the polyphase network was extended to 8 kHz to allow a simpler low pass filter following the network. If the polyphase network response was limited to 3 kHz , the opposite sideband suppression above 3 kHz would depend entirely on the low pass filter response and a more complex filter would be required.
The prototype receiver included a CW filter, AGC and S meter which were conventional in design and are not shown here.

## Performance

Subjectively, the receiver performs as well as commercial designs. Audio quality is clean,
without the effects often heard with crystal fillters. Opposite sideband suppression is approximately 55 dB from 1 to 10 MHz which approaches that achievable with crystal filters. This figure degrades above 12 MHz due to phase errors in the RF sections of the circuit, but is still usable up to 25 MHz . See Fig. 6 . Frequency response close to the carrier is shown in Fig. 7.
Sideband suppression below $\mathbf{3 0 0 H z}$ is relatively poor but in practice this does not interfere with signal intelligibility. In any case it could be improved by adding more low frequency poles in the polyphase network or a high pass filter in the audio section. Receiver selectivity is dependent on the low pass filter. In practice selectivity is adequate but it could certainly be improved with a sharper filter.
Sensitivity is about -115 dBm for 10 dB S/N at 3.5 MHz . Strong signal handling is acceptable with a dynamic range of 90 dB , though an


attenuator may have to be used on the lower bands.
A bandpass filter is necessary between mixer and antenna to reduce response at harmonics of the LO and crossmodulation from local broadcast stations. Alternatively a scheme using phasing techniques such as that described by Hamilton ( $E W+W W$, April 93) could be used to cancel the higher order harmonics.

The VFO should run at four times the

Fig. 7. Close to carrier response.
desired operating frequency. The receiver will operate from under 1 MHz (the lower limit of the input transformer) to about 25 MHz (upper clock limit of 100 MHz ). A VFO input voltage of approximately -10 dBm (about 70 mV ) to the level shifting circuit is required.
The author would like to thank Rod Green for his knowledge and contribution to the project.

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Circuitmaker is a schematic capture and digital simulation system working under Windows. This is a rather strange combination, but on closer inspection it is really targeted at the education market. So how does it compare with the professional packages and other educational products? John Anderson reports.

Circuitmaker comes as a single 3.5 in disk together with a professionally produced loose-leaf manual. Installation was uneventful, accomplished with a simple set-up program run from Windows. By today's standards the 800 K of hard disk space taken by the program and its libraries is modest.
On running the program for the first time the user is presented with a familiar Windows desktop with a top menu and a tool ribbon. Missing from the menu is a help option pressing F1 (the alternative standard Windows help request) only results in a display of the company's name and telephone number in the USA. Not very helpful.

## Operation

Opening a sample schematic for the first time revealed an immediate shock - a simple counter circuit adorned with a 7 -segment display and an led drawn as bulb. Selecting run from the tool ribbon (a running man of course!) resulted in the display changing and the led flashing on each carry out. Most of the example files provided were in the same vein. Note that no current limit resistors are used and thus the student is effectively encouraged to use the display and led components incorrectly.
Reverting to the manual, usually the last resort with a Windows application, described not only the functionality of the software, but also a series of "experiments". Each experiment is designed to promote understanding of the software in the context of education about the function of each circuit.
Producing a schematic using Circuitmaker is by no means as simple as it should be. Parts may be selected from the libraries, and placed on the screen. They may be selected by dragging a box around them and then operated on, e.g. selected items may be rotated in this way. But the line drawing scheme is particular about the mouse arrow being very close to the target component node: if you miss, then the scheme remains in line drawing mode, only aborting when a key is pressed. At


Above, this counter is included as an example of Circuitmaker's simulation capabilities. Note how the led is depicted and its lack of current limiting.

Left, attempting to access a help file results in this rather unhelpful display.


State-machine example.


TTL and other library items


Waveform window
this point the complete line is erased and you must start from the beginning again.
This problem could be alleviated by a dynamic zoom, to increase the magnification in the area where the connection is to be made. But Circuitmaker has no zoom or alternative view facilities, only the Windows scroll bars. Component identifications are possible using the free text drawing facility, but the text is not tied to the component and will not move when the component is moved.

## Linear circuits

The simulation system only works with the digital components, but there are linear components in the library and these may be used to build a circuit diagram. But this is really a dead end, because the schematic cannot be simulated, analysed or exported (except as a picture). Indeed entering a linear circuit into Circuitmaker is just a waste of time.

## Libraries

The menu has six libraries available for immediate access. Selecting a library brings up a list of components to choose from. Each library can contain up to 24 items - a quantity determined by the height of the screen. The libraries are generated in a unique fashion built from primitive existing components and drawings generated by any other Windows drawing package. Library elements are referred to as macros (because of this hierarchy of object definition calls) and you can add your own macros and thus change and extend the libraries. A logical function can be packaged in an alternative shell by importing a drawing of the new outline from any Windows drawing package and assigning an existing logic diagram to it.

## In use

Any professional schematic capture system needs to provide import and export facilities. This system should include netlist in one or more of the standard formats so that it may be used for pcb work. Sadly Circuitmaker only supports bitmap and metafile formats suitable only for Windows pictures, publishing and the macro system. Furthermore there is no design rule check to make sure that all inputs are connected for example.

Alternatively, the simulation output can be displayed as an 'oscilloscope waveform' window, with the outputs represented as changing in time as they slide across the oscilloscope display from right to left.

## SYSTEM REQUIREMENTS

Windows 3.1, mouse, 1 MB of memory for the application, 800 KB of hard disc space, printer.

## SUPPLIER DETAILS

Microcode Engineering, 1943 North 205
West-Orem, Utah 84057. Telephone (801) 226-4470, fax 226 6532. Price \$199, express shipping to UK only, \$44 extra.

Six experiments form the tutorial section of the manual. These are presumably aimed at course lab sessions. The introduction suggests that some grounding in logical systems is a pre-requisite. However, as the first experiment is only a switch and an led, and more complex ideas such as flip flips, gates, flip-flops and counters are introduced gradually in the later experiments, it is probable that almost any GCSE student could use it. Each experiment is accompanied by a series of questions, the answers to which are listed at the back of the manual.

## Conclusions

Circuitmaker represents an entry level route to Windows schematic capture and simple digital simulation. However, the functionality falls a long way short of what is required from a professional package; the only conceivable use beyond education is as a drawing tool for a manual or other document. From the educational standpoint, I'm not sure whether the program represents a useful introduction, or muddle and incompetence, from a system which should be easier to use than paper and pencil.
The simulations could be built on to make a useful educational tool, even for use in lab sessions. But in order to get the best out of such sessions, the course tutor will have to


Multiple simulations - note the simulated logic probe
prepare files in advance because, if the students were instructed to do so, they might be alienated from computer aided electronic engineering forever.

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Two cmos gates form an astable flip-flop, the unknown capacitor and the reference forming the timing components; unlike transistor astables, the circuit

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 self-starts for capacitors in the range $100 \mathrm{pF}-470 \mathrm{nF}$. Capacitors $C_{\mathrm{x}}$ and $C_{\text {ref }}$ determine the on and off periods of the output square wave, whose duty cycle is therefore $d=$ $C_{\mathrm{x}} /\left(C_{\mathrm{x}}+C_{\text {ref }}\right)$. After the $R_{1} C_{1}$ filter, the direct voltage is $d V_{c c}$, which is compared in the Siemens TCA965 window discriminator with a voltage derived from $R_{4}, R_{5}$ and $R_{6}$ (the window centre) and $R_{2.3}$ for the window half-width. Leds show theresult of the comparison. In the prototype, capacitors from 100 pF to 470 nF were compared to within $1 \%$.
José M Miguel
Barcelona
Spain
With two ICs and a few passives, compare two capacitors within $1 \%$ over the 100 pF 470 nF range. Three leds give over, under or



## Wide-range ceramic VFO



Wider frequency range than usual enables ceramic VFO to cope with wide tolerance on ceramic resonators.

## Flip-flop PSU protection his circuit will protect a series pass

Ttransistor or voltage regulator, which has access to the input of its output stage, against shorts.
Two additional transistors crossconnected in the form of a flip-flop provide the protection. If the regulator output is forced low by a short, zener $D_{1}$ stops conducting. Transistor $T r_{1}$ cuts off and $T r_{2}$ is hard on, disabling the regulator, which remains in that condition until, the short having been removed, the pushbutton is pressed and the circuit returns to normality. The led indicates the state of the circuit.
D Danyuk and G Pilko
Kiev
Ukraine


Flip-flop disables voltage regulator in the presence of a short-circuit.

## Noisy video operates relay

Even when a video signal is almost -submerged in noise, this circuit recognises it and operates a relay.
An input tuned circuit selects the 15.625 kHz component of the signal, which is then amplified by the BC548, charging the $22 \mu \mathrm{~F}$ capacitor. After a time determined by that process, at least Is, the $B C 213 L$ draws enough current to pull in the relay, the delay being necessary to prevent noise on the signal affecting the result.
There is sufficient input impedance to allow parallel connection to a video monitor without trouble. The circuit is less critical than the PLL often used for this purpose. John Cronk (GW3MEO)

## Prestatyn

Clwyd
North Wales

## Even up the marks and spaces

f your application demands a precise 1:1 mark/space ratio from an analogue drive signal of indeterminate waveform, this arrangement for steady-state signals exploits the fact that HC signals approach both supply rails.
It depends on DC feedback to the input of a couple of Schmitt-trigger inverters via an op-amp biased midway between zero and the supply voltage. Maintaining the DC average of the output signal at half the supply voltage gives the condition for a 1:1 square wave.
Ian Braithwaite
St Albans
Hertfordshire


## 12V-33V DC-to-DC converter

At a cost of about 50 p , this circuit supplies 33 V at 1.5 mA to a synthesised TV tuner front end, taking the tuner's 12 V as its supply.
Two buffers, $I C_{\text {labb }}$, make a 50 kHz oscillator, which is buffered by the other four devices to provide complementary outputs driving the voltage multiplier, $D_{1-4}$ and $C_{2-4}$. Zener $D_{5}$ is a safety limiter, since the tuner holds the output to the value selected for tuning.
Full-load current requirement is around 10 mA . Do not short the output before the series output resistor, since this will cause latch-up and destruction unless there is a current limit in the 12 V line.

## Mike Harrison

White Wing Logic


Obtaining a 33V tuning voltage for a synthesised TV tuner from the tuner's own 12V supply.

South Woodford
London E18

## Temperature-variable voltage reference

A
precise reference voltage with a controlled temperature coefficient is needed for charging sealed lead-acid cells. This circuit provides an output of 2.3 V $3.9 \mathrm{mV} /{ }^{\circ} \mathrm{C}$.
Temperature-sensing device $I C_{1}$, an LM39II temperature controller from National Semiconductor, gives a voltage output at pin 2 of $10 \mathrm{mV} /$ kelvin with respect to pin 4 , and incorporates a 6.8 V active voltage regulator between pins 1 and
$4 ; I C_{2}$ is the MAX872 2.5 V low-drift voltage reference, the resistors $R_{3,4,7}$ dividing its output to provide pin 3 of the op-amp with a very stable 2.3 V . Current source $T r_{1}$ and $R_{2}$ are controlled by the output of $I C_{1}$, these values giving a collector current of $10 \mu \mathrm{~A} / \mathrm{kelvin}$, or 2.98 mA at $298 \mathrm{kelvin}\left(25^{\circ} \mathrm{C}\right)$; the emitter voltage of $T r_{1}$ is taken to the feedback input of the internal op-amp. This current in $R_{5,6}$ produces a voltage of 2.3 V at pin 2
of the op-amp and therefore at the output. Temperature changes vary $_{1}$, collector current and the voltage at pin 2 of the opamp, which varies the output voltage at the required rate of 2.3 V less the voltage derived from a $10 \mu \mathrm{~A} /$ kelvin current variation - with the values shown, $3.9 \mathrm{mV} /{ }^{\circ} \mathrm{C}$.
Kimet Rees
Brentwood
Essex



## RF sniffer and interference tester

A lthough intended to indicate the presence of RF emissions with the 1996 EMC Directive in mind, this circuit has been used for many other purposes, including testing car alarm keys and as a bug detector. It detects fields down to 1 mW at 1 m and from 100 kHz to 500 MHz . In essence, it is simply a broad-band input circuit, a rectifier and meter, but for the
necessary sensitivity an amplifier is needed and the diodes must be correctly chosen. Germanium diodes conduct at lower forward voltages than do the silicon type, and frequency response is higher with point-contact devices, so pointcontact, germanium OA90 diodes are the ideal choice.
A 1 mH inductor on the input reduces LF

Meter zeroing is not essential, but it does allow the nulling of background signals. The meter may need series resistance to adjust sensitivity; reading is not linear and simply indicates the presence of RF and its relative level.
Alan I lones
Newcastle
sensitivity, as does the feedback capacitor.

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## USING RF TRANSISTORS

## Power construction techniques

> Norm Dye and Helge Granberg show how rf transistor package design, board construction and mounting techniques must all be optimised for efficient circuit operation and long term reliability.
> From the book RF Transistors: principles and practical applications.
n a common emitter/source amplifier configuration, maximum power gain of a given device depends on the emitter/source-to-ground inductance being kept as low as possible. For low impedance devices, such as high power transistors operating at low voltages, minimising their inductance is critical.

Two factors inside the package should be analysed: die design and package construction. Small signal transistor dice are tiny (die size around 0.5 mm square or less) and generally have a single bond pad for attaching a wire to the emitter/source portion of the transistor (Fig. 1). A power transistor die is created by combining large numbers of small signal transistor cells on a single die and interconnecting these cells with a metal "feed structure", as Fig. 2 illustrates.
Several bond pads are available for attaching wires to the emitter/source portions of the transistor die, with the bond pad sizes in the dice made relatively small to minimise parasitic capacitances. Largest wire sizes used are around $50 \mu \mathrm{~m}$, while many higher frequency transistors are designed to use $37 \mu \mathrm{~m}$ or even $25 \mu \mathrm{~m}$ wire.
A $50 \mu \mathrm{~m}$ wire over a ground plane has an associated inductance of approximately 20 nH per inch of length. So both die and package design must be coordinated to produce minimum inductance from bond wires. In dice for high power transistors, this is achieved by making the die long and narrow with a large


Fig. 1. Low power rf fransistor die.
number of bond pads.
The emitter/source inductance outside the transistor consists of the transistor lead inductance to ground and the inductance of the circuit board ground plane.
Thickness of the circuit-board copper-clad foil could affect maximum power gain. But in practice the effect is negligible, except in spe-

Fig. 2. High power rf transistor die.

cial cases such as very high power and low voltage applications.
Most professional designs use double-foilsided circuit board, providing a continuous ground plane at the bottom side of the board. Electrical access is by plated through-holes or feed-through eyelets around the transistor mount opening near the emitter/source area. If a designer lacks the facility for plated-through holes, the emitter/source areas in the transistor mount opening can be wrapped around with straps of metal foil, connecting the areas on the top of the board to the ground plane as illustrated in Fig. 3.
Ground feed-throughs can also be created by using small lengths of hook-up wire placed through holes drilled in the pcb and then soldered to each side. In some cases - such as low frequency three to four octave bandwidth linear designs with biasing circuitry and feedback networks - the ground plane must be the top layer of the circuit board, eliminating feedthrough connections for the emitter/source grounding.
Great care has to be taken by semiconductor manufacturers to minimise emitter/source inductance when characterising of transistors because higher inductance - in addition to causing reduced power gain - also leads to errors in input impedance values.
To minimise lead inductance, the transistor mount opening in the circuit board, which allows the device to be attached to a heat sink, should be no larger than necessary for a given package type. The emitter/source inductance affects the device's power gain to the same extent as an un-bypassed resistance with a value equal to the inductive reactance in question. The only differences are that the inductive reactance does not generate a dc voltage drop and its effective value is more frequencydependent.
If the lead inductance is converted to reactance at the frequency of operation, its effect

can be compared to that of an equal value resistance between the emitter/source and ground. For small signal amplifiers the voltage gain is simply defined as $R_{\mathrm{L}} / R_{\mathrm{E}(\mathrm{S})}$, where $R_{\mathrm{L}}$ is the load impedance and $R_{\mathrm{E}(\mathrm{S})}$ is the external emitter/source resistance or reactance.
But phase errors - generally, greater reactance values and lower device impedances complicate the situation for power devices at high frequencies. The effect of emitter/source inductance on the power gain of an rf power transistor can be calculated using $S$-parameters, if available.
The transistor wire bond (for a specified number of bond pads) and lead frame induc-

## Tips for systematic printed circuit layout

Assuming the frequency or frequency range of operation, power output level desired, and supply voltage as well as the circuit details are known:

1) Is a double-sided design necessary? Would a partial ground plane on each side help design or save board space?
2) Select the laminate with proper dielectric characteristics and foil thickness according to the specifications.
3) Make a sketch to see how much area is required. Where size is limiting, parts of the layout, such as widths of the rf- and dccarrying foil runners, may have to be compromised.
4) Remember that in intermittent operation (eg two way communications) or in pulse operation, much less stress is placed on passive components than in applications
with longer "on" durations, such as tv or fm broadcast. So components (such as capacitors) could have lower of current ratings and smaller sizes.
5) Provide as many grounding feedthroughs as possible within practical limits. Too many is always better than too few.
6) In a push-pull circuit, locate transistors as close to each other as possible for optimum power gain and broad band performance.
7) Laminates with organic dielectric materials tend to have a higher temperature expansion coefficient than transistors. If the pcb becomes very large, divide it into two sections, one for input and one for output. Splitting input and output boards minimises the expansion stresses on the transistor leads and their solder joints, especially useful in high power push-pull designs.
tances are usually fixed by package dimensions. They can only be reduced by selecting the physically-smallest package in which the die can be mounted, note however that making the package too smail could increase thermal resistance.

Sometimes the same transistor die is housed in various package styles - for example, the standard 0.380 soe, 0.500 soe or plastic to220 . Of the three, the 0.380 style would give the highest power gain since its internal package inductance is lower than in the two other case styles.

Stud mounted packages, though not as good thermally as flange types, allow closer access to the ground plane since no openings are needed for the flange ears. But many devices are not available in these packages, nor could they be used in designs where the rear side of the heat sink is not accessible.

## Push-pull inductances

In push-pull circuits, the emitter/source-toground inductance becomes less important and the ground path only provides the dc supply to the devices. Analysis of push-pull operation reveals that the rf current is now flowing from emitter-to-emitter (or source-to-source), so devices should be mounted as physically close to each other as possible. Where existing circuit layout or other reasons precludes this, some improvement can be obtained by connecting all the emitters or sources together with a wide metal strip placed over the transistor caps (Fig. 4).
Flange mounted devices allow each emitter to be connected to the flange using solder lugs or wire loops under the mounting screws, enabling the heat sink to provide a low inductance connection between emitter leads. In practice, emitter-to-emitter (or source-to-

## RF power transistor mounting

1) Control torque on mounting screws and observe manufacturer specifications. Avoid over-torque as it usually produces a worse thermal interface than under-torque. Use proper mounting hardware.
2) Avoid excessive thermal compound, or risk a poor thermal interface and
deformation of the flange in some device types.
3) When soldering down leads, apply solder abundantly to leach most of the gold from the leads and prevent formation of a brittle joint.
4) Never mount the device in such a way to apply force on the leads in a vertical direction towards the cap.
5) Never mount to place ceramic-to-metal joints in tension.
6) Make sure that mounting holes are deburred.
7) Always fasten the device to the heat sink prior to soldering the leads.
8) Avoid bending the leads repeatedly to prevent their breakage.
9) Do not hold the leads of stud mounted devices to prevent device rotation while tightening the nut. A wrench flat is provided for this purpose.
10) Leave sufficient clearance between the circuit board opening and the device body. 1.25 mm is adequate.
source) inductance can be made lower than emitter/source to ground inductance, so it is obvious that a push-pull circuit will exhibit a higher power gain than a single-ended one using the same devices.
For push-pull operation at vhf and uhf, special packages have been developed where two transistor dice are attached next to each other, limiting the emitter-to-emitter inductance to that of the bonding wires. This is probably the only practical approach to using push-pull techniques at uhf frequencies, particularly at higher power levels.

## Laying out a circuit board

Requirements for rf circuit layouts depend on frequency, power level, and voltage of operation.
Today, practically all solid state rf circuits use some type of laminate of dielectric material and metal foil (usually copper) - referred to as copper clad laminate - available either with the foil attached to only one side or both sides. Foil thickness is measured in ounces per square foot, with the thinnest being a half ounce laminate, converting to a foil thickness of 0.018 mm . Similarly, one ounce would be 0.036 mm .

The half ounce would be sufficient for small signal circuits, and in some instances can be used at higher power levels, at uhf to
microwaves where the skin depth is shallow

## Skin effect

AC concentrates in the surface layer of a conductor, due to the "skin effect." The lower the frequency, the deeper this layer extends (or the thicker it is), and vice versa. But part of the current also passes below the top layer. So the conductor can be visualised as having a number of layers, each one of the thickness of one skin depth.
By definition, a skin depth is the distance in which the current decreases to a value of $1 / \mathrm{e}$ or $36.8 \%$ of its initial value, analogous to sigma in a Gaussian distribution. So for practical purposes, all current is contained in about five or six layers, each having the thickness of a skin depth.

Skin depth, $\delta$, of a copper conductor is approximately 0.009 mm at 100 MHz . Using this as a reference, the skin depth versus frequency in practice can be calculated as $\delta=0.009 \times \sqrt{ }(100 / f)$, where $\delta$ is the skin depth in $\mathrm{mm}, f$ is the actual frequency in MHz , and 100 is the reference frequency in MHz .
The formula shows that low frequencies require heavier foil thicknesses than high frequencies. But other factors also affect total circuit losses: including dielectric losses; ir losses in the rf circuitry and ir losses in dc carrying conductors.


Fig. 5. Partial ground plane on each side of a circuit board. The black rectangle (bottom) is connected to the top ground plane (shaded area) via feed-throughs.

## Board materials

Single-sided circuit board is primarily used in circuits designed for very low frequencies where ground plane inductance is not critical. It can also be used in uhf and microwave circuits where coplanar striplines (waveguides) are used for impedance matching or other functions. Since there is no ground plane, the coplanar waveguide is most practical where relatively high impedances are involved.
Two-sided circuit board laminate is the most commonly used material, and is useful where a ground plane is required on top of the board with other circuitry underneath it (method 1). Openings to the top ground plane can be made in locations requiring clearances for component lead feed-throughs.
Probably the most common circuits using two-sided laminate board layouts are those designed for higher frequencies (vhf to microwave), with a continuous ground plane on the bottom side of the circuit board (method 2). This may be needed to provide solid grounding points for the components on the top using feed-throughs, or to establish a specific impedance for a microstrip. (Microstrip is commonly referred to as stripline although stripline is actually the name given to a transmission line consisting of a current-carrying conductor with a ground plane above and below.
Stripline is mostly used for constructing filters, hybrid couplers and other passive components. Sometimes, a combination of the two grounding methods gives the best result, with a partial ground plane on each side of the board, Fig. 5. In If applications two-sided boards are used to reduce emitter-to-ground inductance for increased power gain.
Several dielectric materials are used in making pcb. In a single-sided laminate the quality of the dielectric and how well the foil adheres to it at elevated temperatures are more important than the material's relative dielectric constant $\left(\varepsilon_{\mathrm{r}}\right)$ except in designs with high impedance lines or relatively high $Q$ resonating elements: relative dielectric constant of a material is defined as the material's actual dielectric constant referred to the dielectric constant of a vacuum $\varepsilon_{0}$.
The dielectric constants most commonly used for insulating media in circuit board laminates range from 2 to 7 , although aluminium oxide with its $\varepsilon_{\mathrm{T}}$ of 9.5 has gained popularity due to advances in ceramic technology, laser machining and metal deposition on such substrates. The higher $\varepsilon_{\mathrm{r}}$ of $\mathrm{Al}_{2} \mathrm{O}_{3}$ produces more compact circuit designs and circuits capable of withstanding high temperatures without changes in performance (compared to ones using organic based dielectrics).

## Material lossiness

The dielectric constant of a material is actually a complex number with a real and imaginary part. The imaginary part, sometimes referred to $\varepsilon^{\prime \prime}$, when divided by the real part, $\varepsilon^{\prime}$, is called the loss tangent of the material. $\varepsilon^{\prime \prime}$ is referred to as the loss factor, a measure of the lossiness of the material.

The real part, $\boldsymbol{\varepsilon}^{\prime}$, is usually normalised to the dielectric constant of a vacuum $\left(\varepsilon_{0}\right)$ and is referred to as $\varepsilon_{T}$.
In insulating materials, $\varepsilon_{\mathrm{T}}$ is temperature and frequency dependent. The changes are largest in high loss materials such as phenolic and epoxy fibreglass and lowest in materials such as Teflon (tfe) and $\mathrm{Al}_{2} \mathrm{O}_{3}$. The effect is true for both the real and imaginary parts of $\varepsilon_{\mathrm{T}}$, making phenolic materials usable only at audio or ultrasonic frequencies; or perhaps to frequencies of $10-20 \mathrm{MHz}$, particularly in small signal applications.
Epoxy fibreglass is usable to about 200 MHz . Beyond that, glass tfe, Duroid, or plain tfe should be used.
Rather complex formulas can be used to calculate microstrip impedance, when $\varepsilon$ and height $H$ are known. But a graph plotted from data obtained by such calculations (Fig. 6) should be accurate enough for most applications. The term $H$, in the expression $W / H$ is confusing to many, but it actually refers to the thickness of the dielectric medium (Fig. 7)
For a given characteristic impedance, the line gets wider with a dielectric medium of low $\varepsilon_{\varepsilon}$, and vice versa. As apoint of comparison, air is assumed to have an $\varepsilon_{\mathrm{r}}$ of 1.0 .
Materials with an $\varepsilon_{\mathrm{r}}$ in the range of 100 and higher have been used for dielectrics in capacitors for many years. But only recently have high-dielectric ceramics (most of them bari-um-titanium-oxide-based substances) been developed that are stable enough at temperature to be used for microstrip substrates.
Also, for high values of $\varepsilon_{\mathrm{r}}$, the line width decreases, and so more accurate dimensioning is required.

## Velocity reduction

Electrical wavelength in transmission lines that have a relative dielectric constant greater than one is reduced by a factor related to the square root of the dielectric constant. This is given by $\lambda_{\mathrm{m}}=\lambda_{0} / \sqrt{ } \varepsilon_{\mathrm{r}}$ where $\lambda_{\mathrm{m}}$ is the wavelength in the dielectric, $\lambda_{0}$ is the wavelength in free space and $\varepsilon_{T}$ is the relative dielectric constant of the transmission line.
Sometimes this wavelength reduction is thought of as a reduction in velocity of the propagated wave (which it is) giving rise to the term "velocity factor" for a dielectric material.
Velocity factors for typical materials, from lowest to highest ratios are:

| Duroid: | 0.68 to 0.66 |
| :--- | :--- |
| Teflon: | 0.65 to 0.63 |
| Glass-epoxy: | 0.52 to 0.49 |
| $\mathrm{Al}_{2} \mathrm{O}_{3}:$ | 0.36 to 0.32. |

In uhf and microwave circuit layouts, using coplanar waveguides, striplines or microstriplines, sharp corners (Fig. 8a) in folded lines should be avoided. They create standing waves in these areas and result in the line having an irregular impedance along its length. Angling the corner is a common practice to avoid this discontinuity (Fig. 8b).
In case of a folded microstrip, a length cor-

rection factor must be entered as $L-W n / \sqrt{2}$, where $L$ is the calculated line length, $W$ is the line width, and $n$ is the number of folds.
As recently as 1980 circuit board layouts had to be made with black adhesive tape laid down on a transparent or opaque Mylar foil: or for more demanding applications by cutting and peeling red "ruby" coating from its Mylar backing. Since the ruby peel-off layer is very thin, more precise layouts can be realised with this method than with the adhesive tape.
The tape and ruby layouts are typically produced oversize ( 200 to $800 \%$ ) and reduced to normal size by photolithography, yielding the very accurate dimensioning required for microwave and other microstrip designs. Ruby printed circuit artwork is still used for the most demanding circuit designs.
Now, most circuit board layouts are made using computers, and special software is available from a variety of sources. Depending on the hardware, accurate dimensioning is possible, especially if the initial artwork is made on an expanded scale.
Images can be printed with a suitable printer to produce black and white art work, which
can photographed and reduced for the final layout film.
The computer image can also be directly transferred to a printed circuit board-manufacturing facility, via modem, speeding up the procedure though accuracy is not guaranteed. A point to note is that printers such as laser writers can change the artwork dimensions typically in a negative direction by 1-2\%, requiring a correction factor.

## Suitability for continuous operation

Low-frequency and high-power amplifier circuits are frequently realised in push-pull configurations with wide band transformers as matching elements - even where only single frequency operation is desired. Such designs are much easier to implement and more reliable than either a push-pull or a single-ended one with narrow band $L C$ matching networks.
In the latter case, the $L s$ would reach very low values and the $C$ s would be required to carry high rf currents. Excessive heating of components and possibly even solder melting could be the result.
Transistor manufacturers frequently show



Fig. 9. Two possible mounting methods for of transisfors. Stud mounted devices are shown for simplicity. In (a) the transistor is mounted directly on the top surface of the heat sink, with the circuit board spaced an appropriate distance to be at the same level as the package leads. In (b), the circuit board is flush mounted to the heat sink into which a recess has been cast or machined. Note that for stud packages the upper portion of the stud is shaped like the letter D to provide a self-locating key.
single-ended narrow band circuits as test circuits in device data sheets. But not many of the circuits (for very high power devices) are suitable for continuous operation - though they may permit the rated peak performance of the device to be achieved.

For example, in the characterisation of a 600 W transistor, where narrow band test circuits were required for three frequencies (330 MHz ), problems similar to those described above were encountered. The circuits barely held intact during a $2-3 \mathrm{~min}$ tune-up operation, despite providing forced-air cooling on the passive components.

Even at low frequencies (such as $2-30 \mathrm{MHz}$ ), when designing a high power amplifier (say 300 W ) ground planes and circuit layout are just as important as they are at higher frequencies $(500 \mathrm{MHz}$ ) with lower power amplifiers ( 50 W ).
Impedance levels in the two instances are comparable, both being relatively low, and if wideband transformers are used, special attention should be paid to minimising the inductance between the device's output terminal and the transformer's connection points. Excessive series inductance results in loss of output power and early saturation and deterioration in wide band performance. Performance would also be affected by excessive series inductance on the input side in the form of possible resonances within the passband.

But resorting to exact $50 \Omega$ lines at the inputs and outputs of amplifiers below vhf is not nec-
essary because the line lengths are only a fraction of the wavelength. So discontinuities do not noticeably affect circuit performance.
In addition to the rf carrying conductors, dc circuitry should also be examined.

At a power level of 300 W and with a 28 V supply, typical dc currents are approximately 16 A , assuming a $50 \%$ efficiency.
In pulsed operation, under certain conditions over twice the power output of CW can be obtained from the same device: peak dc can be as high as 40 A . But a particular problem with pulsed operation is that any ir voltage drops, in addition to reducing the peak power output, also deform the shape of the pulse. So a laminate foil thickness heavier than normal may be required for the rf circuitry

## Mounting power transistors

RF power transistors are reliable devices and can operate for over 100,000 hours without failure when proper mounting techniques and electrical specifications are observed.

Excessive torque in fixing both stud-mounted and flange mounted devices is a relatively common cause of premature failure. Overtorque, especially with flange mounting, makes thermal contact to the heat sink worse than under-torque. It also prevents the flange from expanding longitudinally with heat, resulting in upwards bowing and separation of its centre area from the heat sink.
Maximum recommended screw torques are: 6.5 and 11.0 inlbs for the $8-32$ and $10-32$ studmounted packages respectively, and 5.0inlbs

for flange-mounted packages. In all cases, split lock washers and flat washers are recommended, of which the latter should be in immediate contact with the flange top surface or with the bottom of the heat sink when using stud packages.

Along with flat washers, some equipment manufacturers use Belleville washers made of thin steel sheet bowed by $10-30^{\circ}$. They are available in a variety of torque ratings and so probably provide the most constant and controlled pressure for flange mounted devices.

Metric system hardware, with its finer threads than British standard hardware (\#4 = $3 \mathrm{~mm}, \# 6=4 \mathrm{~mm}$ ), continues to cause debate. But according to experts in thermal studies, a difference would only be noticeable if proper mounting torque and selection of other mounting hardware were not observed.

Certain packages are less critical in their mounting than others. Examples are packages having the flange made of mechanically hard material such as a copper-tungsten mixture, commonly referred to as Elkonite. This material, although not as good a heat conductor as copper, is often used because its thermal expansion coefficient is closer to that of ceramics than is pure copper.

On the other hand, large push-pull packages (Gemini), which can be up to 40 mm long and have flange thicknesses of only 1.5 mm , are more critical in mounting than normal flange packages. With these headers, over torque of the mounting screws and an excessive amount of thermal compound can make the flange bow upwards in the centre. In addition to forming a bad thermal interface, the result could be fractures in the BeO insulators and the dice.
Good deburring of the mounting holes, whether for a stud or flange device, is vital. The transistor must make good physical contact with the heat sink and should not sit on burrs surrounding the mounting holes.

Flatness required of the heat sink also depends on the transistor package type. Most flange transistors have an unpublished flatness standard of $\pm 0.25 \mu \mathrm{~m}$. So the heat sink surface at the mounting area should have at least the same flatness, which is not difficult to achieve.

Some devices come in pill headers, conventional headers with standard lead configurations but without the mounting stud or flange. Pills are mounted with the heat sink by soldering, using heat conductive epoxy or pressing the pill against the heat sink by some mechanical means with a thermal compound interface. Soldering yields the best thermal interface of all mounting methods and so is common practice in most high reliability equipment.
Two common methods for mounting rf power transistors (Figs. 9a and 9b) are to mount them directly on the top surface of the heat sink, with the circuit board at the same height as the package leads; or to have the circuit board flush mounted to the heat sink, which has a recess in it. Both are equally good and used in the industry, except that the recessed heat sink surface is thinner by the
amount of the depth of the recess. But If the ratio of the recess to the total thickness is $1: 4$ or more, there will be no appreciable difference in thermal transfer.
To improve reliability and to minimise lead inductance, the seating plane of the transistor lead frame should be close to that of the circuit board (Fig. 10c). Lead ends should be bent upwards to aid soldering and to make removal of the device easier in case of a failure.
If the circuit board is very large and the soldered area of leads is small, a long term failure mechanism may develop. Depending on the temperature excursions, a difference in thermal expansion coefficients could cause eventual separation of the electrical connection due to solder fatigue. Gold plating on the transistor leads is approximately $1.25-2.5 \mu \mathrm{~m}$ thick and is essential since rf power transistors are exposed to $425-450^{\circ} \mathrm{C}$ during die bonding. These temperatures would oxidise or liquify most metals having good properties of solderability.
But gold does form a very brittle intermetallic compound with the tin in most solders. This makes the immediate interface of lead and solder a more likely candidate for the solder fatigue problem. Using more solder helps to some extent, but in military projects transistor leads are generally pre-tinned to leach the gold out of the solder joint before mounting.
Where formation of intermetallics is a serious problem, tin-based solders should be switched, for example, to those having an indium base.
Some military specifications call for strain reliefs in the transistor lead frame in the form of small loops in the leads, close to the transistor housing. But these are generally difficult to implement.
RF power transistors should always be fastened to the heat sink before soldering leads to the circuit board - though the opposite procedure may make automated assembly easier in production. If the leads are soldered first, achieving tolerances tight enough to prevent tensions that push the leads up, down or sideways is almost impossible, and in such cases semiconductor manufacturers usually limit their responsibility for failed devices.
Semiconductor leads are usually made of materials such as Kovar or other nickel-based alloys, which have thermal expansion coefficients close to those of ceramics. But such alloys are hard, have low ductility, and harden easily. Only a few sharp bends in a given area can easily break a lead This usually occurs in the interface between the lead and ceramic. If repeated bends cannot be avoided, they should be made as far from the transistor housing as possible.

## Solderless mounting

Unique to flanged devices is a solderless method for mounting (Fig. 11). First the flange is fastened to the heat sink with spacers, then the transistor leads are pressed against contacts on the circuit board surface by a Teflon ring, a silicone rubber ring and an aluminum ring. Circuit board contact areas must


Fig. 11. Solderless method of mounting flanged devices, showing a 0.5 in SOE package.
be clean. Solder plating is acceptable but gold plating would be best in the areas of contact.
Depending on rigidity of the circuit board and the location of its mounting points to the heat sink, additional support may be required to prevent the board from bending downwards under pressure.
The advantage is that this method allows for various degrees of expansion of the heat sink, circuit board and the transistor with temperature. The more usual method of soldered lead connections does not allow for any movement through temperature expansions, resulting in mechanical tension in the transistor leads. Breakage of the leads or separation of the solder joints may occur, risking long term failure. But the solderless method does not guarantee a positive contact between transistor leads and the circuit board surface at uniform distances from the transistor housing. So it is not recommended for frequencies higher than $100-150 \mathrm{MHz}$ where circuit series inductances of the leads become increasingly critical. Mechanically clamped transistors have been tested in a 2 kW prototype rf amplifier for ten years with over 5000 hours of operation without failures.
One common practice with stud mounted transistors is to tighten the mounting nut while holding the device by the leads to prevent it from turning. This should never be permitted. Stud mounted transistors generally have a "wrench flat" at the end of the stud to prevent the stud from turning while tightening the mounting nut.

An even worse practice is initially to fasten the transistor to the heat sink with a low torque, then solder the leads and finally tighten the mounting nut to its full torque. Such a method will always leave some twisting tension in the leadframe.

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> In the final part of his series on designing out distortion in audio amplifiers, Douglas Self examines the compromise in class $A$ circuitry. Trading efficiency for performance he presents a worked design for the nearest thing to a straight wire with gain.

# Distortion in power amplifiers 

## 8: class A amplifiers

There are two salient facts about Class A amplifiers: they are inefficient; they give the best possible distortion performance. The quiescent dissipation of the classic Class A amplifier is equal to twice the maximum output power, making massive output power impractical. But the nature of our hearing means that the power of an amplifier must be considerably increased to sound significantly louder. It is well known that power in watts must be quadrupled to double sound pressure level, (SPL) but this is not the same as doubling subjective loudness; this is measured in Sones rather than dB above threshold, and some researchers have reported that doubling subjective loudness requires a 10 dB rather than 6 dB rise in SPL, implying that amplifier power must be increased tenfold, rather than merely quadrupled ${ }^{\prime}$. This may help to put worries abour amplifier size into perspective...
There is an attractive simplicity about class A. Most of the distortion mechanisms studied so far stem from class B, and we can thankfully forget crossover and switchoff phenomena (Distortions 3b, 3c), non-linear vas loading, (Distortion 4) injection of supply-rail signals, (Distortion 5) induction from supply currents. (Distortion 6). and erroneous feedback connections. (Distortion 7) Beta-mismatch in the output devices can also be ignored.

## The art of compromise

The only real disadvantage of class A is inefficiency, so inevitably efforts have been made to compromise between A and B. As com-
promises go, traditional class AB is not a happy one because, when the $A B$ region is entered, the step change in gain generates significantly greater high order distortion than that from optimally biased class B. However, a well-designed $A B$ amplifier will give pure class A performance below the $A B$ threshold, something a class B amp cannot do.


Another compromise is the so-called nonswitching amplifier. with its output devices clamped to pass a minimum current. However, it is not immediately obvious that a sudden

Fig. 1. The major class $A$ configurations. $1 c, 1 d$ and te are push-pull variants, te being simply a class B stage with higher Vbias.

halt in current-change as opposed to complete turn-off makes for a better crossover region. Those residual oscillograms that have been published seem to show that some kind of discontinuity still exists at crossover ${ }^{2}$.

A potential problem is the presence of maximum ripple on the supply rails at zero signal output; the PSRR must be taken seriously if good noise and ripple figures are to be obtained. This problem can be simply solved


Fig. 2. How output device current varies in push-pull class A. The sum of the currents is nearconstant, simplifying biasing.


Fig. 3. Gain linearity of the class A emitter-follower output stage. Load is 88, and quiescent current $(l q)$ is 1.6A. Upper trace class $A$, lower trace optimal class B.
by the measures proposed for class B designs
There is a kind of canonical sequence of efficiency improvement in class A amplifiers. The simplest kind is single-ended and resistively loaded, as at Fig.1a. When it sinks output current, there is an inevitable voltage drop across the emitter resistance, limiting the negative output capability, and resulting in an efficiency of $12.5 \%$ (erroneously quoted in at least one textbook as $25 \%$, apparently on the grounds that power not dissipated in silicon doesn't count) This would be of purely theoretical interest - and not much of that - except that a single ended design has recently appeared. This reportedly produces a 10 W output for a dissipation of 120 W , with output swing predictably curtailed in one direction ${ }^{3}$.

A better method - constant current class Ais shown in Fig. 1b. The current sunk by the lower constant current source is no longer related to the voltage across it, and so the output voltage can approach the negative rail with a practicable quiescent current. (Hereafter shortened to " $I_{q}$ ") Maximum efficiency is doubled to $25 \%$ at maximum output; for an example with 20 W output (and a big fan) see reference 4. Some versions (Krell) make the current source value switchable, controlling it with a kind of noise gate.
Push-pull operation once more doubles fullpower efficiency, producing a more practical $50 \%$; most commercial class A amplifiers have been of this type. Both output halves now swing from zero to twice the $I_{\mathrm{q}}$, and least voltage corresponds with maximum current, reducing dissipation. There is also the intriguing prospect of cancelling the even-order harmonics generated by the output devices.
There are several ways to induce push-pull action. Figs 1 c , d show the lower constant current source replaced by a voltage controlled current source. This can be driven directly by the amplifier forward path, as in Fig. $1 c^{5}$, or by a current control negative feedback loop, as at $1 d^{6}$. The first of these methods has the drawback that the stage generates gain, phase splitter $T r_{1}$ doubling as the vas; hence there is no circuit node that can be treated as the input to a unity gain output stage, making the circuit hard to analyse, as vas distortion cannot be separated from output stage non-linearity. There is also no guarantee that upper and lower output devices will be driven appropriately for class $A$ if the effective quiescent varies by more than $40 \%$ over the cycle ${ }^{5}$.
The second push-pull method in 1d is more dependable, and I can vouch that it works well. The disadvantage with the simple form shown is that a regulated supply is required to prevent rail ripple from disrupting the current loop control. Designs of this type have a limited current control range. In Fig. Id, $\mathrm{Tr}_{3}$ cannot be turned on further once the upper device is fully off - so the voltage controlled current source will not be able to respond to an unforeseen increase in the output loading. If this happens there is no way of resorting to class $A B$ to keep the show going and the amplifier will show some form of asymmetrical hard clipping.

The best push-pull stage seems to be that in Fig. 1e, which probably looks rather familiar. Like all the conventional class B stages examined in Part 4, this one will operate effectively in push-pull class $A$ if the bias voltage is sufficiently increased; the increase over class B is typically 700 mV , dependant on the value of the emitter resistors. For an example of high biased class $B$ see reference 7 . This topology has the great advantage that, when confronted with an unexpectedly low load impedance, it will operate in class AB . The distortion performance will be inferior not only to class A but also to optimally biased class $B$, once above the $A B$ transition level, but can still be made very low by proper design.
Although the push-pull concept has a maximum efficiency of $50 \%$, this is only true at maximum sinewave output. Due to the high peak/average ratio of music, the true average efficiency probably does not exceed $10 \%$, even at maximum volume before obvious clipping.

Other possibilities are signal controlled variation of the class A amplifier rail voltages, either by a separate class $B$ amplifier, or a modulated switch mode supply. Both approaches are capable of high power output, but involve extensive extra circuitry, and present some daunting design problems.
A class B amplifier has a limited voltage output capability, but can be flexible about load impedances, as more current will be simply turned on when required. However, class A has also a current limitation, after which it enters class AB , and so loses its raison d'etre. The choice of quiescent value has a major effect on thermal design and parts cost so a clear idea of load impedance is important. The calculations to determine the required $I_{q}$ are straightforward, though lengthy if supply ripple, $V_{\text {ce(sat) }}$, and $R_{\mathrm{e}}$ losses, etc., are all considered, so I just give the results here. An unregulated supply with $10,000 \mu \mathrm{~F}$ reservoirs is assumed.
A $20 \mathrm{~W} / 8 \Omega$ amplifier will require rails of approx $\pm 24 \mathrm{~V}$ and a quiescent of 1.15 A . If this is extended to give roughly the same voltage swing into $4 \Omega$, then the output power becomes 37 W , and to deliver this in class A the quiescent must increase to 2.16 A , almost doubling dissipation. If however full voltage swing into $6 \Omega$ will do, (which it will for many reputable speakers) then the quiescent only needs to increase to 1.5 A ; from here on I assume a quiescent of 1.6 A to give a margin of safety.

## The class a output stage

I consider here only the high biased class $B$ topology, because it is probably the most popular approach, effectively solving the problems presented by the others. Fig. 2 shows a Spice simulation of the collector currents in the output devices versus output voltage for the emitter follower configuration, and also the sum of these currents. This sum of device currents is, in principle, constant, but need not be so for low THD. The output signal is the difference of device currents and is not inher-


Fig. 4. Gain linearity of the class A quasi-complementary output stage. Conditions as Fig. 3. Upper trace class $A$, lower class B.

| TABLE 1. |  |  |  |
| :--- | :--- | :--- | :--- |
| Harmonic: | Emitter <br> Follower | Quasi <br> Comp | CFP |
| Second | $.00012 \%$ | $.0118 \%$ | $.00095 \%$ |
| Thlrd | $.0095 \%$ | $.0064 \%$ | $.0025 \%$ |
| Fourth | $.00006 \%$ | $.0011 \%$ | $.00012 \%$ |
| Fifth | $.00080 \%$ | $.00058 \%$ | $.00029 \%$ |

ently related to the sum. However, a large deviation from this constant sum condition means inefficiency, as the stage is conducting more quiescent than it needs to for some part of the cycle. The constancy of this sum is important because it shows that the voltage measured across $R_{\mathrm{e} 1}$ and $R_{\mathrm{e} 2}$ together is also effectively constant so long as the amplifier stays in class $A$. This in turn means that $I_{q}$ can be simply set with a constant voltage bias generator, in very much the same way as class B.
Figs 3, 4, 5 show Spice gain plots for open loop output stages, with $8 \Omega$ loading and 1.6 A quiescent; the circuitry is exactly as for class $B$ in Part 4. The upper traces show class A gain, and the lower traces gain under optimal class B bias for comparison. Fig. 3 shows an emitter follower output, Fig. 4a simple quasi complementary stage, and Fig. 5 a CFP output.

We would expect class A stages to be more linear than B, and they are. Harmonic and THD figures for the three configurations, at 20 V peak, are shown in Table 1. There is absolutely no gain wobble around 0 V , and
push-pull class A genuinely does cancel even order distortion. Class B only does this in the crossover region, in a partial and unsatisfactory way.
It is immediately clear that the emitter follower has more gain variation, and therefore worse linearity, than the CFP, while the quasi comp circuit shows an interesting mix of the two. The more curved side of the quasi gain plot is on the negative side, where the CFP half of the quasi circuit is passing most of the current. However we know by comparing Fig. 3 and Fig. 5 that the CFP is the more linear structure. Therefore it appears that the shape of the gain curve is determined by the output half that is turning off, presumably because this shows the biggest $g_{\mathrm{m}}$ changes. The CFP structure maintains $g_{\mathrm{m}}$ better as current decreases, and so gives a flatter gain curve with less rounding of the extremes.
The gain behaviour of these stages is reflected in their harmonic generation; Table 1 reveals that the two symmetrical topologies give mostly odd order harmonics as expected.


Fig. 5. Gain linearity of the class A CFP output stage. Upper trace class A, lower trace class B

The asymmetry of the quasi comp version causes a large increase in even order harmonics, and this is reflected in the higher THD figure. Nonetheless the THD figures are still two to three times lower than for their class B equivalents.
If this factor of improvement seems a poor return for the extra dissipation of class A, this is not so. The crucial point about the distortion from a class A output stage is not just that is low, but that it is low order, and so benefits much more from a typical NFB factor that falls with frequency than does high order crossover distortion.
The choice of class A output topology is
now simple. For best performance, use the CFP. Apart from greater basic linearity, the effects of output device temperature on $I_{q}$ are servoed out by local feedback, as in class B. For utmost economy, use the quasi complementary with two NPN devices: these need only a low $V_{\text {ce(max) }}$ for a typical class A amp, so here is an opportunity to recoup some of the money spent on heatsinking.
The rules are different from class B; the simple quasi configuration will give first class results with moderate NFB, and adding a Baxandall diode to simulate a complementary emitter follower stage makes little difference to linearity ${ }^{7}$.

It is sometimes assumed that the different mode of operation of class A makes it inherently short circuit proof. This may be true with some configurations, but the high biased type shown here will continue delivering current until it bursts. Overload protection is no less necessary.

## Quiescent control systems

Unlike class B, precise control of quiescent current is not required to optimise distortion. For good linearity there just has to be enough of it. However, $I_{q}$ must be under some control to prevent thermal runaway, particularly if the emitter follower output is used, and an ill conceived controller can ruin the THD. There is also the point that a precisely held standing current is considered the mark of a well bred class A amplifier; a quiescent that lurches around like a drunken sailor does not inspire confidence.
Thermal feedback from the output stage to a standard $V_{\mathrm{be}}$ multiplier bias generator will work ${ }^{8}$, and should be sufficient to prevent runaway. However, unlike class B, class A gives the opportunity of tightly controlling $I_{q}$ by negative feedback. This is profoundly ironic because now that we can precisely control $I_{\mathrm{q}}$, it is no longer critical. Nevertheless it seems churlish to ignore the opportunity.
There are two basic methods of feedback current control. In the first, the current in one output device is monitored, either by measuring the voltage across one emitter resistor, ( $R_{\mathrm{S}}$ in Fig. 6a), or by a collector sensing resistor. The second method monitors the sum of the device currents, which as described above, is constant in class A.
The first method as implemented in $6 a^{7}$ compares the $V_{\text {be }}$ of $T r_{4}$ with the voltage across $R_{\mathrm{S}}$, with filtering by $R_{\mathrm{F}}, C_{\mathrm{F}}$. If quiescent is excessive, then $\operatorname{Tr}_{4}$ conducts more, turning on $\mathrm{Tr}_{5}$ and reducing the bias voltage between points $A$ and $B$.
In $\mathbf{6 b}$, which uses the voltage controlled current source approach, the voltage across collector sensing resistor $R_{\mathrm{s}}$ is compared with $V_{\text {ref }}$ by $T r_{4}$, the value of $V_{\text {ref }}$ being chosen to allow


FIG 6A


FIG 6B


FIG 6C
for $\operatorname{Tr}_{4} V_{\mathrm{be}}{ }^{9}$. Filtering is once more by $R_{\mathrm{F}}, C_{\mathrm{F}}$. For either 6 a or 6 b , the current being monitored contains large amounts of signal, and must be low pass filtered before being used for control purposes. This is awkward as it adds one more time constant to worry about if the amplifier is driven into asymmetrical clipping, and implies the desirability of large electrolytic capacitors to minimise the ac voltage drop across the sense resistors. In the case of collector sensing there are unavoidable losses in the extra sense resistor. It is my experience that imperfect filtering can produce a serious rise in distortion.
The better way is to monitor current in both emitter resistors. As explained above, the voltage across both is very nearly constant, and in practice filtering is unnecessary. An example of this approach is shown in Fig. 6c, based on a concept originated by Nelson Pass ${ }^{10}$. Here $T r_{4}$ compares its own $V_{\text {be }}$ with the voltage between $X$ and $B$; excessive quiescent turns on $\boldsymbol{T r}_{4}$ and reduces the bias directly. Diode $D$ is not essential to the concept, but usefully increases the current feedback loop gain; omitting it more than doubles $I_{q}$ variation with $\operatorname{Tr}_{7}$ temperature in the Pass circuit.
The trouble with this method is that $T r_{3} V_{\text {be }}$ directly affects the bias setting, but is outside the current control loop. A multiple of $V_{\text {be }}$ is established between $X$ and $B$, when what we really want to control is the voltage between X and $\mathbf{Y}$. The temperature variations of $\operatorname{Tr}_{4}$ and $T r_{3} V_{b e}$ partly cancel, but only partly. This method is best used with a CFP or quasi output so that the difference between Y and B depends only on the driver temperature, which can be kept low. The "reference" is $T_{4} V_{\text {be }}$,

Table 2. $I_{q}$ change per ${ }^{\circ} \mathrm{C}$ change in temperature

|  | Changing <br> Tr7 temp only | Changing <br> Global temp. |
| :--- | :--- | :--- |
| Quasi+ $V_{\text {be }}$ mult | $+0.112 \%$ | $-0.43 \%$ |
| Pass: as Fig. 6 c | +0.0257 | $-14.1 \%$ |
| Pass: no diode D | +0.0675 | $-10.7 \%$ |
| New system: | $+0.006 \%$ | $-0.038 \%$ |

(assuming $0.22 \Omega$ emitter resistors and $1.6 \mathrm{~A} / \mathrm{I}$ )
which is itself temperature dependent. Even if it is kept away from the hot bits it will react to ambient temperature changes, and this explains the poor performance of the Pass method for global temperature changes. (Table 2).
To solve this problem, I would like to introduce the novel control method in Fig. 7. We need to compare the floating voltage between X and Y with a fixed reference, which sounds like a requirement for two differential amplifiers. This can be reduced to one by sitting the reference $V_{\text {ref }}$ on point Y . This is a very low impedance point and can easily swallow a reference current of 1 mA or so. A simple differential pair $T_{\mathrm{r} 15,16}$ then compares the reference voltage with that at point $Y$ : excess quiescent turns on $\operatorname{Tr}_{16}$, causing $\operatorname{Tr}_{13}$ to conduct more and reducing the bias voltage.
The circuitry looks enigmatic because of the high impedance of $T r_{13}$ collector would seem to prevent signal from reaching the upper half of the output stage; this is in essence true, but the vital point is that $T r_{13}$ is part of a NFB loop that establishes a voltage at A that will
keep the bias voltage between A and B constant. This comes to the same thing as maintaining a constant $V_{\text {bias }}$ across $T r_{5}$. As might be imagined, this loop does not shine at transferring signals quickly, and this duty is done by feedforward capacitor $C_{4}$.
Without it, the loop (rather surprisingly) works correctly, but HF oscillation at some part of the cycle is almost certain. With $C_{4}$ in place the current loop does not need to move quickly, since it is not required to transfer signal but rather to maintain a DC level.
The experimental study of $I_{\mathrm{q}}$ stability is not easy because of the inaccessibility of junction temperatures. Professional Spice implementations like PSpice allow both the global circuit temperature and the temperature of individual devices to be manipulated; this is another aspect where simulators shine. The exact relationships of component temperatures in an amplifier is hard to predict: I show here just the results of changing the global temperature of all devices, and changing the junction temp of $\operatorname{Tr}_{7}$ alone (Fig. 7) with different current controllers. $T r_{7}$ will be one of the



Fig. 8. Class A anplifier THD performance with quasi-comp output stage. The steps in the LF-portion of the trace are measurement artifacts.


Fig. 9. Class A distortion performance with CFP output stage.
hottest transistors and unlike $T_{9}$ it is not in a local NFB loop, which would greatly reduce its thermal effects.

## A new class A design

The full circuit diagram shows a 'blameless' $20 \mathrm{~W} / 8 \Omega$ class A power amplifier. This is as close as possible in operating parameters to the previous class $\mathbf{B}$ design to aid comparison.

In particular the NFB factor remains 30 dB at 20 kHz . The front end is as for the class B version, which should not be surprising as it does exactly same job, input Distortion 1 being unaffected by output topology.
As before the input pair uses a high tail current, so that $R_{2,3}$ can be introduced to linearise the transfer characteristic and set the transconductance. Distortion 2 (vas) is dealt with as

Table 3

|  | 1 kHz | 10 kHz | 20 kHz | Power |
| :--- | :--- | :--- | :--- | :--- |
| class B EF | $<.0006 \%$ | $.0060 \%$ | $.012 \%$ | 50 W |
| class B CFP | $<.0006 \%$ | $.0022 \%$ | $.0040 \%$ | 50 W |
| class B EF 2-pole | $<.0006 \%$ | $.0015 \%$ | $.0026 \%$ | 50 W |
| class A quasi | $<.0006 \%$ | $.0017 \%$ | $.0030 \%$ | 50 W |
| class A CFP | $<.0006 \%$ | $.0010 \%$ | $.0018 \%$ | 20 W |
| class A CFP 2-pole | $<.0006 \%$ | $.0010 \%$ | $.0012 \%$ | 20 W |

(All for $8 \Omega$ loads and 80 kHz bandwidth. Single pole compensation unless otherwise stated)
before, the beta enhancer $\operatorname{Tr}_{12}$ increasing the local feedback through $C_{\text {dom }}$. There is no need to worry about Distortion 4 (non linear loading by output stage) as the input impedance of a class A output, while not constant, does not have the sharp variations shown by class $B$.
The circuit uses a standard quasi output. This may be replaced by a CFP stage without problems. In both cases the distortion is extremely low but, gratifyingly, the CFP proves even better than the quasi, confirming the simulation results for output stages in isolation.
The operation of the current regulator $T r_{13,15,16}$ has already been described. Using a band gap reference, it holds a $1.6 \mathrm{~A} I_{\mathrm{q}}$ to within $\pm 2 \mathrm{~mA}$ from a second or two after switch on. Looking at Table 2, there seems no doubt that the new system is effective.
As before, an unregulated power supply with $10,000 \mu \mathrm{~F}$ reservoirs was used, and despite the higher prevailing ripple, no PSRR difficulties were encountered once the usual decoupling precautions were taken.

## Performance

The closed loop distortion performance (with conventional compensation) is shown in Fig. 8 for the quasi comp output stage, and in Fig. 9 for a CFP output version. The THD residual is pure noise for almost all of the audio spectrum, and only above 10 kHz do small amounts of third harmonic appear. The suspected source is the input pair, but this so far remains unconfirmed.
The distortion generated by the class B and A design examples is summarised in Table 3, which shows a pleasing reduction as various measures are taken to deal with it. As a final tweak, two pole compensation was applied to the most linear (CFP) of the class A versions, reducing distortion to $0.0012 \%$ at 20 kHz , at some cost in slew rate (Fig. 10). While this may not be the fabled straight wire with gain, it must be a near relation...

## And finally...

The techniques in this series have a relevance beyond power amplifiers. Applications obviously include discrete op-amp based preamplifiers ${ }^{11}$ and extend to any amplifier offering static or dynamic precision. My philosophy is that all distortion is bad, and high order distortion is worse... $\mathrm{n}^{2} / 4$ worse, according to many authorities ${ }^{12}$. Digital audio routinely delivers the signal with less than $0.002 \%$ THD, and I can earnestly vouch for the fact that analogue console designers work hard to keep the distortion in long and complex signal paths down to similar levels. I think it an insult to allow the very last piece of electronics in the chain to make nonsense of these efforts.
I do not believe that an amplifier yielding $0.001 \%$ THD is going to sound much better than another generating $0.002 \%$. However, if there is ever a doubt as to what level of distortion is perceptible, then using the techniques I have presented, it should be possible to reduce the THD below the level at which there can be any rational argument.

I am painfully aware of the school of thought that regards low distortion as inherently immoral, but this is to confuse electronics with religion. The implication is that very low THD can only be obtained by huge global NFB factors which in turn require heavy dominant pole compensation that severely degrades slew rate. The obvious flaw in this argument is that, once the compensation is applied, the amplifier no longer has a large global NFB factor: Its distortion performance presumably reverts to mediocrity, further burdened with a slew rate of four volts per fortnight.
To me low distortion has its own aesthetic appeal. All of the linearity enhancing strategies examined in this series are of minimal incremental cost to existing designs with the possible exception of using class A. Thus the answer to the question "if all other arguments fail" is "Why Not?


Fig. 10. Distortion performance for CFP output stage with 2-pole compensation. The THD drops to $0.0012 \%$ at 20 kHz , but the extra vas loading has compromised the positive-going slew capability. The 2-pole trace is shown moving off the graph at 50 kHz .
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## Minimising THD from JFET op-amps

$\mathrm{A}^{1}$
Ithough they have many benefits, opamps with JFET inputs suffer from nonlinearity of the capacitance seen at the two inputs, which is typically $3-5 \mathrm{pF}$. This causes distortion which increases as the source impedance of the input signal rises.
Parasitic substrate capacitance is nonlinear as a function of applied commonmode voltage. It lowers with increasing bias voltage. and varies instantaneously with applied ac common-mode voltage.
For input source impedances from 0.1 to $1 \mathrm{M} \Omega$, the non-linear capacitance can result in distortion as high as several tenths of a percent in the audio band. According to Analog Devices note AN232-Bootstrapped IC substrate lowers distortion in JFET opamps $-50 \mathrm{k} \Omega$ is the threshold where the effect "starts to be easily detectable at audio frequencies".
One way round the problem is to use input impedance compensation, as shown in the circuit. This balances the source $R C$ components at the two amplifier inputs.

Feedback resistor $R_{\mathrm{S} 2}$ is simply made equal to the net nominal source impedance represented by $R_{\mathrm{S} 1}$. If the source is capacitive, feedback capacitance can also be added.
In some cases unbalanced feedback and source impedances are unavoidable. The circuit diagram illustrates a further technique for reducing the effects of common-mode input capacitance bootstrapping the IC substrate. This technique has the capability to reduce distortion due to $C / V$ non-linearity below the residual noise level.
Loading on the input amplifier is negligible, which helps improve linearity. The buffer following the input op-amp provides a high impedance load yet operates at video speeds and drives at up to 100 mA .
As with a conventional non-inverting amplifier, gain of this circuit is $\left(R_{1} / R_{2}\right)+1$. Divider $R_{3} / R_{4}$ feeds back a proportion of the buffered output to the negative supply pin of the input amplifier. Since the ratios of $R_{1} / R_{2}$
and $R_{3} / R_{4}$ are the same, the substrate of the IC is driven with a signal equal to that at the non-inverting input. This reduces input capacitance by reducing the voltage across it.
For overall stability, the feedback via $R_{3} / R_{4}$ must be less than that of $R_{1} / R_{2}$. Because divider $R_{3} / R_{4}$ reduces supply voltage to the input op-amp, this configuration can limit dynamic range so it should only be used for gains of five and above.
With the transistor shorted, i.e. the bootstrapping removed, the circuit distorts a $10 \mathrm{kHz}, 3 \mathrm{~V}$ rms signal by about $0.1 \%$. Unbootstrapped performance is illustrated in the first photograph. Advantages of bootstrapping are shown in the second photograph, where distortion is swamped by the residual noise.

Analog Devices, Walton House, Walton on Thames, Surrey KT12 1PF. Tel. 0932 253320, fax 0932247401.



If source impedance is high, distortion caused by non-linear capacitance at a JFET op-amp input is considerable. Top trace is output at 3 V and the bottom trace is $0.3 \%$ distortion.


Bootstrapping the JFET op-amp reduces distortion caused by non-linear input capacitance to $0.03 \%$ - most of the bottom trace is noise.

## Power supply control

In order to conserve energy in batterypowered equipment, power controller circuits are becoming increasingly complex.
The first of these two designs, from Maxim's Battery management and DC-DC converter circuit collection not only provides regulated supply rails but also switch-mode battery charge control and fet gate drives for power switching. A currentmode PWM buck configuration produces the main 3.3 V supply while a flyback circuit converts the battery voltage to produce the 15 V rail. There is also a $25 \mathrm{~mA}, 5 \mathrm{~V}$ supply provided by a low-dropout linear regulator. In shut-down mode, initiated via the chip's serial port, the circuit consumes around $10 \mu \mathrm{~A}$. At the minimum input of 5 V , quiescent current is 1 mA while maximum load on the 3.3 V supply is 1.5 A . Two PCMCIA feeds switching between $0 \mathrm{~V}, 5 \mathrm{~V}$, 12 V and high-impedance are available in addition to the five gate drivers. These drivers are used to disable parts of the equipment being powered when not in use. There is also an analogue multiplexer that allows voltages to be monitored externally
Although the chip provides switch-mode power for battery charging, external control is needed. Switching regulator current is set by an on-chip 7bit d-to-a converter. Code for this converter is input via the SPI three-wire serial interface.
The second circuit is a higher-power dual PWM controller but has no facilities for battery charging. In this case, maximum current output is up to 3A on both the 5 V and 3.3 V outputs and 300 mA for the 15 V rail. Unlike the first circuit, whose input is


Switching frequency is 300 kHz in both designs. In the second circuit, a novel current-mode SMPS configuration employs


## Clocks for data

R
evision 3 of Motorola's Timing R solutions handbook has recently been published. It contains over 180 pages of data sheets together with applications information on design considerations and techniques for distributing clock signals.

These diagrams are from a discussion on low-skew clock drivers. Transmission line effects become significant when a driving device's rise or fall time, whichever is smallest, is less than three times the propagation delay of a switching wave
along a track.
The first two diagrams are Spice simulations assuming a propagation delay of 0.234 ns per inch of track and a driver delay of lns . On the above assumption regarding transmission-line effects, the

A. TRANSMISSION LNE WITH NO TERMINATION

C. TRANSMISSION LINE WITH PARALLEL TERMINATION

E. TRANSMISSION LINE WITH AC TERMINATION




WHERE, $Z_{D}=$ DRIVING DEVICE OUTPUT IMPEDANCE
B. TRANSMISSION UNE WITH SERIES TERMINATION

D. TRANSMISSION UNE WTH THEVENIN TERMINATION

Options for terminating clock lines, above, together with resulting waveforms, bottom. All are a compromise but Motorola concludes that ac termination is generally best below 25 MHz , and Thévenin for above 40 MHz .



A. UNTERMINATED $0.5-$ INCH, $41 \Omega$ TRANSMISSION LINE
B. UNTERMINATED 9-INCH, 41 $\Omega$ TRANSMISSION UNE

Although only simulations, these diagrams clearly demonstrate the effects of unterminated transmission lines.
maximum track length is about 1.5 in but as is clear significant ringing already occurs at 0.5 in when no termination is used

Terminating clock lines is simpler than terminating buses since there is only one driving source. The second set of diagrams shows commonly used terminating methods and resulting output waveforms. It demonstrates the effects of various types of termination on a $230 \mathrm{~mm} 41 \Omega$ transmission line using an MC88941 as a driver.
Each method has its own fortes and drawbacks. Series termination is recommended where the load is lumped at the end of the track and the output impedance of the driver is less than the loaded characteristic impedance of the track.
Series termination needs only one component and does not create a DC current path, which means that the driver output levels are not degraded. This method causes problems however if the driver has different impedance characteristics in its high and low states. Since the clock normally has more than one destination, series termination is rarely appropriate.
Parallel termination involves a loading resistor whose value is equal to the characteristic impedance of the line. Its major disadvantage is the DC path which causes signal level degradation and additional power dissipation. The main consideration with this type of termination is how much degradation in logic level - low or high depending on whether the resistor is tied to ground or the supply - can the receiving device tolerate?
Two resistors are used in Thévenin termination. An important task here is selecting the resistors to avoid settling of the signal between the high and low logic thresholds of the receiver. Designers of TTL circuits often use a $220 / 330$ combination but with CMOS the switching point is half the supply voltage. In a 5 V system, choosing a 1:1 divider ratio would result in a level of 2.5 V if the driver failed. This means that the level would be indeterminate.
In Thévenin termination, the combined
resistances should equal the characteristic impedance of the line. Although the resistors cause a DC path in both high and low states, they are less problematical than the single parallel termination resistor. This is because the Thévenin DC path sees twice the resistance of its parallel counterpart. The improved on level is shown in the diagram. A further reduction in the loss of signal level is obtained by adding a capacitor in series with the parallel termination resistor to open the DC path. Combined, the R and C should exhibit a time constant more than twice as great as the loaded line delay.

As well as reducing signal level degradation, this method lowers power consumption. An additional bonus is that resistors and capacitors for this task are obtainable in SIL packaging. At higher frequencies however, the benefits fall off. The book concludes that for frequencies below $25 \mathrm{MHz}, \mathrm{AC}$ termination is generally best while above 40 MHz , Thévenin is best.

Motorola, European Literature Centre, 88 Tanners Drive, Blakelands, Milton Keynes MK14 5BP. Tel. 0908 614614, fax 0908 618650.

## Lead-acid battery charger has thermal control

- aving 10A minimum current limit threshold, the LT1038 can form the basis of a substantial battery charger. This circuit, from Linear Technology's PowerSolutions handbook (publication LT/GP 079325 M ), is for lead-acid cells and features both voltage and thermal control. Temperature control is provided by the pnp transistor which is thermally coupled to the battery. The npn transistor shuts down the circuit if the input voltage falls
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With a 10A minimum current-limit threshold and comprehensive fault protection, the LT1038 is ideal for applications in battery charging.

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## A-to-D \& D-to-A converters

Sensor interface. AD1B60 is Analog's software-configurable interface between Industrial sensors and digital systems. It accepts input from thermocouples, RTDs, and analogue voltage and current, output being engineering units in digital form on two serial interfaces. All excitation, compensation, scaling and linearisation is carried out by the IC. For non-standard sensors, two software-programimed ranges can be stored in internal eeprom. An evaluation board, the $A D 1 B 60 / E B$, is available. Analog Devices Ltd, 0932 253320.

Asynchronous-clear D-to-A. Analog's serial/byte input, 16-bit digital-to-analogue converter AD660 has an asynchronous clear-to-zero function, for use in applications concerned with precise motion, as in machine tools. Complete with built-in output amplifier and zener reference, the AD660 offers $\pm 1$ lsb integral linearity and 15 -bit monotonic performance; signal-to-noise ratio is 83 dB . Interfacing to processors is serial or byte-wide, with doublebuffered latches. It settles to 0.51 sb in $10 \mu \mathrm{~s}$ for a full-scale step. Analog Devices Ltd, 0932253320

High-level graphics. Blue Micro's new range of palette digital-toanalogue converters run at clock frequencies up to 250 MHz and have graphics memory ports from 64bit to 200 bit wide, including in their application the newer types of monitor offering 1600 by 1280 pixel resolution. Three types are avallable or being released: RGB530, for low and midrange workstations; RGB525, for enhanced graphics PCs; and RGB561, intended for higher-level working with the high-resolution monitors. Blue Micro, 0604603310.

## Discrete active devices

Power mosfets. Hitachi's DIV-L. series of power mosfets feature very low on resistance, one of them at $7 \mathrm{~m} \Omega$ at a gate/source voltage of 10 V , said to be the lowest available. They are meant for dc-to-dc converters and
power management and the range includes three p-channel types, 2SJ244/317/361 and two n-channel devices, 2SK1579/1950. Drain currents are up to 3 A at $12-60 \mathrm{~V}$ and the smallest of three package styles is the surface-mounted $\mu$ pak, measuring 4.5 mm by 2.5 mm . Hitachi Ltd, 0628 585000.

SM power mosfets. Four of the six new Zetex medium-power SOT-89 surface-mounted transistors form complementary pairs with 200 V and 60 V ratings. There is also a 200 V n channel device with a 1.5 V threshold and a 60 V -channel type rated for 0.87A continuous. All the devices dissipate 1.5 W and peak currents of all are around ten times the continuous figure, which in the two pairs are 0.61 A and $0.39 \mathrm{~A}(60 \mathrm{~V})$ and 0.27 A and 0.17A (200V). Turn-off delays are $10-20 \mathrm{~ns}$ and input capacitance $75-100 \mathrm{pF}$ maximum. Zetex plc, 061-6275105.

## Digital signal processor

Audio for PCs. AT\&T's new DSP3207 digital signal processor provides real-time processlng for multimedia applications featuring sound and communications as well as imaging. In this latest member of the DSP32xx family, i/o is removed from the core DSP functions by taking the serial interface from the chip. The power-down mode works at reduced power from the DSP3210 and an even lower-power mode now works via a clock-gating pin that virtually shuts the chip down. AT\&T Microelectronics, 0732742999.

33Mips DSP at 0.5 mW . ADSP-2171 by Analog is a digital slgnal processor with 33 mips performance and three power-reduction modes, needing 0.5 mW maximum. It handles GSM, IS-54 VSELP (North America) and JDC (Japan Digital Cellular) speech coding standards for digital mobile communications. It operates from a half-rate clock, generating the 33 MHz rate internally to reduce hf noise and lower crystal cost. Both hardware and software development support is on offer. Analog Devices Ltd, 0932 253320.

GSM vocoder. On one chip, the AMSAS3501 vocoder to the CEPT Group Special Mobile standard integrates an analogue front end and a software-configurable digital signal processor. With a range of powersaving facilities, the device dissipates only 100 mW and has a 13 -bit linear sigma-delta codec and a 16 -bit risc

DSP core, programmed for the RPE/LTP $13 \mathrm{~kb} / \mathrm{s}$ speech transcoding function. Its 16 -bit parallel control port interfaces to most microcontrollers. Austria Mikro Systeme, 027623399.

## Linear integrated circuits

350 MHz dual op-amps. Two dual unity-gain current feedback op-amps, HFA1205/1245 from Harris, are claimed to offer twice the bandwidth of any available op-amp at about the same supply current and at lower prices than some single op-amps. Main characteristics are: 350 MHz -3 dB bandwidth at 6 mA per A supply current, $1100 \mathrm{~V} / \mu$ s slewing, 0.04 dB gain flatness to 50 MHz and $0.02 \% / 0.02^{\circ}$ differential gain and phase while putting out 60 mA drive from a $\pm 5 \mathrm{~V}$ supply. HFA1245 incorporates a pair of enable/disable pins for each op-amp, switching outputs to high impedance for line sharing. Harris Semiconductor (UK), 0276686886.

Thrifty PLL. Sony's CXA1786 frequency-synthesiser PLL chip for 1 GHz moblles is pin-compatible with Fujitsu's MB1511, but draws only 6 mA from 3 V when active and $300 \mu \mathrm{~A}$ in the software programmed power saving mode. Sony Semiconductor Europe, 0256478771.

RF modulator. An integrated uhf ff modulator, the CXA 1733 from Sony, combines the oscillator with video clamp, white clip, video modulator, audio FM modulator; test pattern generator and intercarrier switch, reducing the need for external support circuitry and easing board layout. An on-board voltage regulator accepts supply variations of up to 2 V on a 5 V supply. Bandwidth is $470-750 \mathrm{MHz}$ and peak-to-peak video imput is 0.5 V . RF output is 10 mV nominal. Sony Semiconductor Europe, 0256 478771

## Logic building blocks

High-speed buffers. Two low-power buffer amplifiers from Comlinear, are suitable for ultra-fast flash A-to-D conversion and other high-frequency applications. CLC109 has a bandwidth of 250 MHz , settling to $0.2 \%$ in 5 ns and a THD of -65 dBc at 20 MHz , driving 30 mA at $\pm 4 \mathrm{~V}$. CLC111 is for low cost per channel design. With a bandwidth of 800 MHz , slew rate of $2700 \mathrm{~V} / \mathrm{\mu s}$, distortion of -62 dB 2nd and 3rd at $20 \mathrm{MHz}, 60 \mathrm{~dB}$ crosstalk at 10 MHz and differential gain and phase of $0.08 \% / 0.04^{\circ}$ at


8 -bit microcontrollers. The MB89620 serles of 8 -bit microcontrollers are added to Fujitsu's F2MC-8L family, the new series being low-power types. Seven internal and four external level or edgecontrolled interrupt sources are used and peripheral blocks include A-to-D converter, PWMs, a 16 -bit-timer, a watchdog timer, serial Interface and 52 i/o ports. The chip combines the accumulator with a shadow register, the temporary accumulator, the two forming a stack for arithmetical operations. Supply voltage is $2.2 \mathrm{~V}-6 \mathrm{~V}$ and clock frequency 10 MHz . Fujitsu Microelectronics Ltd, 062876100.
3.58 MHz , the device is particularly suited to low-cost video buffering. Comlinear Europe Ltd, 0203422958.

LCD controller/driver. Hitachi's HD66710 IC controls and drives an LC display of up to 16 characters by two lines and up to 40 icon symbols, also producing a drive voltage of up to 9 V from a $3 \vee$ supply. Individual symbols may be flashed without software intervention. Hitachi Europe Ltd, 0628585000.

6ns comparators. Two new Maxim edge-triggered comparators resolve inputs down to $2 n \mathrm{~V}$ and exhibit propagation delays of 6 ns , insensitive to any amount of overdrive. Timing skew between complementary outputs is about 500ps. MAX915/6 are single/dual, TTL-compatible devices, operating from dual $\pm 5 \mathrm{~V}$ or a single 5 V to -10 V supply and, since input common mode extends to the
negative rail, they are usable in 5 V ground sensing. Maxim Integrated Products UK, 0734845255.

40 MHz dram controllers. National's DP8440 40 MHz dynamic ram controller is programmable to support a range of processors and memories up to 16 Mbit with data paths to 32 bits; the 8441 being a 64 Mbit . controller driving up to 0.5 Mbyte of memory on 64-bit data paths. The devices support auto processor burstmode access, fast page mode, static column mode and nibble mode dram configurations. PLLs on-chip provide a precision delay generating sub-clock-cycle delays. No memory buffers are needed. National Semiconductor, 010498141103269.

## Memory chips

Fast dram. Four times as fast as standard drams, NEC's 16 -bit synchronous drams have a 10 ns access time and were designed for use in 100 MHz microprocessor-based systems. Pipelining is used to obtain the speed increase, as well as arranging memory in two independent banks, so that a new page can be selected from one while data is read from the other. NEC Electronics, 0908 691133.

## Microprocessors and controllers

32-bit 486. Claimed to be the fastest 486-compatible, 32-bit
microprocessor in the industry, Blue Micro's Blue Lightning is sold as a motherboard or card-level part and is fully compatible with the Intel 80486 series, but with advantages. It is a true 32 -bit device with 32 -bit external data bus width. It has 16 Kbyte of fourway set assoclative cache memory and double or triple internal clocking allows CPU speeds of up to 100 MHz with a 33 MHz bus speed. Power consumption is $1.5-3 \mathrm{~W}$ from 3.3 V , 3.6 V or 4.1 V , depending on frequency. This is not the same device as the IBM 486SLC, which uses a 16 -bit external bus. Blue Micro is the official IBM representative. Blue Micro Electronics, 0604603310.

## Mixed-signal ICs.

Single-chip audio decoder. A complete audio decompression system on one chip, the Crystal CS4920 audio decoder dac contains everything needed to receive and process compressed audio and to convert it to high-quality stereo output, its digital signal processor supporting a wide range of decompression standards. Signal-tonoise ratio is up to 90 dB and THD less than $0.01 \%$. Crystal
Semiconductor Corp, (512) 4457222 (US).

RS-323C interface. Linear's LTC1338 RS-232C interface IC shuts down to $1 \mu \mathrm{~A}$, with a $50 \mu \mathrm{~A}$ supply current to keep the receivers alive. It offers protection against repeated $\pm 10 \mathrm{kV}$ discharges and uses the Flowthrough package layout in which inputs are on one side of the package and outputs on the other. Speed is up to 120kbaud. Linear Technology (UK) Ltd, 0276677676.

RS-232 transceiver. MAX214 by Maxim is a programmable, 5 V RS232 transceiver with three drivers and five receivers. One control pin programs the device as a complete eight-line serial port for data terminal equipment or as data circuit terminating equipment. A dual charge pump, which needs external capacitance, generates the necessary voltages to produce the RS-232 standard $\pm 5 \mathrm{~V}$ transmitter output levels. Data rates are up to $116 \mathrm{~kb} / \mathrm{s}$. In shutdown mode, supply current is $20 \mu \mathrm{~A}$, receivers remaining active. Maxim Integrated Products UK, 0734 845255.

## Optical devices

Photodiode/amplifier. Burr-Brown's OPT201 photodiode plus amplifier IC is a 2.29 by 2.29 mm photodiode and a transimpedance amplifier which gives an output voltage proportional to the incident light intensity; the large diode size reduces the need for critical positioning. Response is 0.45 AW , dark error 2 mV , bandwidth 4 kHz and quiescent current $400 \mu \mathrm{~A}$. Package is an 8 -pin transparent plastic dip and dice are available. Burr-Brown International Ltd, 0923 233837.

Laser for fibres. A 1300 nm laser diode by Hitachi, the HL1326MF, is for use in short and medium range optical communications, offering stable operation over the $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ range of temperatures. It is based on a muiti-quantum well structure and is an InGaAsP FabryPerot diode with a threshold current of 10 mA and high efficiency. Output power is 5 mW at 1310 nm and operating current 25 mA at $25^{\circ} \mathrm{C}$. Package is low-cost and hermetically sealed. Hitachi Europe Ltd, 0628 585000.

InGaAs avalanche photodiodes.
Photodiodes from EG\&G are now available from Pacer Components. C30644/5 series diodes are for use in communications at 1300-1550nm wavelengths and have a gain of 10 . Quantum efficiency is $80 \%$ at 1300 nm and response 8.4A/W. The diodes come in a variety of packages, including pigtail types. Pacer Components Ltd, 081-642 9997.

Keyboard components. Range of keyboard switches from Rafl has versions using a combination of multi-
colour leds to provide red, green and yellow as well as their combinations. PCB-mounted RF15 types now include round-actuator versions, lowprofile types and high-profile models. Keyboards may be assembled that have the protective capability of membranes with the rather better feel of short-travel keys. Rati (GB) Ltd, 0737778660.

## Oscillators

Smallest VCO? Measuring 7.62 mm by 7.63 mm by 2.97 mm and taking only 16 mA from a 3 V supply, the Z Comm SMV2500 voltage-controlled oscillator tunes the $2 \cdot 4-2.485 \mathrm{GHz}$ band and is intended for use in wireless lans and personal communications, a whole transceiver now being able to fit on a "credit-card"-sized board. Band is covered by a $0-3 \mathrm{~V}$ tuning voltage. Power output is 10 mW across the band, phase noise -85 dBc at 10 kHz offset and second harmonic -20 dBc . Eurosource Electronics, 081-568 3332.

## Programmable logic

 arrays270 MHz FPGAs. Now in $0.6 \mu \mathrm{~m} \mathrm{cmos}$ instead of the earlier $0.8 \mu \mathrm{~m}$ technology, AT\&T's ATT30XX series of FPGAs toggle at $190-270 \mathrm{MHz}$ with gate densitles of 2000-9000 usable gates. The series is a true second source to the Xilinx XC3100 family and provides direct equivalents. ATT30XX-4 at 230 MHz toggling rate and ATT30XX-5 with 190 MHz rate are now available, the ATT30XX-3, toggling at 270 MHz , to come during the first half of 1994. AT\&T Microelectronics, 0732742999.

## Power semiconductors

PSU controller. For use in batterypowered equipment, Maxim's MAX786 comprises separate stepdown regulators for 3.3 V and 5 V , two comparators for low-battery detection and two low-dropout, micropower linear regulators to supply backup power to cmos ram and real-time clocks. Efficiency with a 2 A load is $95 \%$, and $80 \%$ for $3 \mathrm{~mA}-3 \mathrm{~A}$ loads. At the heavier loads, operation is shifted to synchronous rectification with pulse-width modulation at 200 kHz or 300 kHz . Standby and shut-down modes are provided. Maxim Integrated Products Ltd, 0734 845255.

500W transient suppressors. SA series silicon transient voltage suppressors made by Semtech handle 500W peak pulse power. They are both unidirectional and bidirectional types, have a response time of 1 ps and a voltage range of 5 170 V , with forward surge rating of 70A and steady-state power dissipation of 1W. Semtech Itd, 0592 773520.

High-power IGBT. Handling 600A from a 1200 V supply, Toshiba's new insulated-gate bipolar transistor saturates at 2.7 V . Fall time and reverse recovery times are 200 ns and 250 ns and there is a built-in collector sense terminal. Tosh'ba Electronics (UK) Ltd, 0276694600.

## PASSIVE

## Displays

Tantalum chips. TPS tantalum chip capacitors from AVX find application in any power supply in which low equivalent series resistance is necessary: $100 \mathrm{~m} \Omega$ at up to $330 \mu \mathrm{~F}$. The capacitors are surface-mounted and have a particularly smooth case for better machine handling. AVX Lid, 0252336868.

RF/microwave capacitors. Porcelain and ceramic capacitors in the Q-MAX series by Capax Technologies have values in the $0.1-100,000 \mathrm{pF}$ range and work in the $10 \mathrm{MHz}-4 \mathrm{GHz}$ band. These units meet or exceed the applicable MIL-C-55681/4 characteristics and have solder-overnickel ends for increased solder dwell time. Alternatively, they are made with gold-over-nickel and palladium silver ends. Anglia Microwaves Ltd, 0277 630000 .

Large LCDs. New technology used in the FP Displays Visilight liquid-crystal displays allows the production of displays larger than the previous maximum of 6 in , going up to 18 in . Good visibility in all light conditions and a viewing angle of $160^{\circ}$ make the displays suitable for public information systems and low weight reduces mounting and enclosure requirements. Reflective or transreflective types can be made, the latter belng a combination of reflective and back-lit types. FP Displays, 0272 251125.

Chip thermistors. Surface-mounting PTC thermistors in the PTH9C22 range by Murata are chiefly intended to protect hybrid circuits against thermal overload, and complement the company's Posistor range. Three types rapidly reduce current when temperature reaches 80,100 or $120^{\circ} \mathrm{C}$, depending on type. Nominal resistance at $25^{\circ} \mathrm{C}$ is $470 \Omega$ and the devices operate at $16 \mathrm{~V}, 30 \mathrm{~mA}$ maximum. Murata Electronics (UK) Ltd, 0252811666.

## Filters

2.5 GHz chip filters. Murata LFK3O chip filters are claimed to have better
performance than discrete-component types. The LC filters are of the lowpass variety with a range of 1.6 GHz 2.5 GHz , the first to become available being a 1.9 GHz version for DECT and a 1.66 GHz type. These filters handle powers up to $3 W$ in $50 \Omega$ systems and exhibit an Insertion loss of less than 0.7 dB , increasing by 0.1 dB over the range -30 to $85^{\circ} \mathrm{C}$. Attenuation is 30 dB at twice cut-off and at least 20 dB up to the tenth harmonic. Dimensions are 4.5 mm by 3.2 mm by 2 mm . Murata Electronics (UK) Ltd, 0252811666.

Saw filters. The range of surface acoustic-wave filters from OKI is available with frequencies of 700 MHz to 2 GHz . Input and output are both $50 \Omega$, so that no adjustment is needed. Packaging is in ceramic, 4.8 mm square, 12-pad units, which can be reflow soldered. OKI Semiconductor (UK) Ltd, 0753516577

## Hardware

DC blowers. Brushless, DC, centrifugal blowers by Eastern Air Devices Inc. measure 1.43 in by 5.13 in by 4.96 in , weighing under 1 lb . Two models deliver air at 20 or $30 \mathrm{ff}^{3} / \mathrm{m}$ with maximum static pressure up to 0.45 or 1.3 in of water. Operating at 24 V DC, speeds are 2300 or $3500 r e v / m i n ~ a n d ~ b a l l ~ b e a r i n g s ~ a r e ~$ permanently lubricated. Options include a 5V Hall sensor output giving two pulses per revolution, TTL control with ground disable, auto restart, active current limlting and $80^{\circ} \mathrm{C}$ operation. Laser Lines Ltd, 0295 267755.

Quad mosfet driver. Linear's LT1161 quad mosfet driver is meant for highside switching in adverse conditions. It is a quad $n$-channel type providing $100 \%$ operating voltage margin in 24 V and 28 V systems. Each switch channel has its own charge pump and needs no extra components to boost the n-channel gate 12 V above supply. Each has its own protection, which latches-off or resets with no effect on the other three. Current limit, delay time and auto restart period are all programmable. Ratings are $-15 \mathrm{~V}-50 \mathrm{~V}$ on supply pins and 75 V maximum on gate pins. Linear Technology (UK) Ltd, 0276677676.

Plastic cases. New range of plastic, hand-held equipment enclosures by West Hyde come in four sizes, in black or white, and are designed to afford a comfortable grip. The body is moulded in two parts in ABS, the halves being held by three selftapping screws. A flat panel either matches the ABS case or is made in translucent material for infrared application. Mounting pillars are provided, as are battery compartments and contacts. West Hyde Enclosures, 0453731831.

## Instrumentation

50 GHz spectrum analysers. Two new spectrum analysers from H-P, the HP8564E and HP8565E provide single-connection measurement to 50 GHz with a very low noise floor. Sensitivity at that frequency is -117 dBm in a 10 Hz bandwidth. The single coaxial connection sweeps all signals from 30 Hz to 50 GHz , eliminating the need for external mixers and, since the preselector removes unwanted signals, there is no need to identify signals. HP8564E has a range of $9 \mathrm{kHz}-40 \mathrm{GHz}$, while the HP8565E goes from 9 kHz to 50 GHz . Both have a low-end 30 Hz limit and are preselected over 2.7 GHz . Hewlett-Packard Ltd, 0344362867.

Oscilloscope probe. The PR30 oscilloscope current probe by Lem Heme has a resolution of 1 mA , measuring in the range 0 to $\pm 20 \mathrm{~A}$ AC/DC with a flat response from zero to 100 kHz and response time of better than $1 \mu \mathrm{~s}$. A Hall-effect probe provides low noise and an accuracy of $\pm 1 \%$ of reading $\pm 2 \mathrm{~mA}$, the clampon jaws taking conductors up to 19mm diameter. Lem Heme Ltd, 0695 20535.

Synthesised function generator. The Yokogawa FG1 10 and 120 are single and dual channel synthesised function generators, which provide frequency accuracy to within $\pm 0.0001 \%$ and amplitude setting to within $0.5 \%$ of setpoint and $0.2 \%$ of range. Waveforms are set up in an 8 K digital memory and converted by a 12-bit D-to-A. Output is sine or square from $1 \mu \mathrm{~Hz}$ to 2 MHz and triangle, ramp or pulse to 100 kHz . In the dualchannel FG120, outputs are independent, relative phase being set from $-10,000^{\circ}$ to $+10,000^{\circ}$ in $0.01^{\circ}$ increments. Martron Instruments Ltd, 0494459200.

Eight oscilloscopes. A range of eight instruments in Leader's 8000 serles of oscilloscopes cover the 20 100 MHz band, all having a 12 kV CRT except the 20 MHz type, on which it is optional. All models over 40 MHz have delayed sweep and fixed-level triggering, with CRT readout and cursor measurement. Thandar Instruments, 0480412451.

Digital storage adaptor. A digital storage oscilloscope adaptor by Van Draper, the H3001 is unlike other designs in that it allows full use of the associated oscilloscope controls to give post-storage analysis, cursor and annotation display. Several units may be connected together to give up to four channels. Van Draper Electronics Ltd, 0533813091.

## Literature

Spice newsletter. Entirely concerned with the Spice circuit simulation program, the free Intusoft Newsletter

contains, in its most recent edition, application notes on simulating sensors and variable phase generators, and an introduction to an interactive verslon of Spice. A floppy disk, obtainable for a fee, contains all the circuit diagrams and Spice models in the publication, models for pressure and Hall-effect sensors and new device models. Intusoft, 0101
(310)833-9658.

RF Designer's Guide. A new designers' guide from Mini-Circuits Europe is a short-form catalogue of IF/RF/microwave signal-processing components, containing details of over 1000 standard items. Custom devices are also manufactured. Mini-Circuits Europe, 0252835094.

## Materials

CFC-free solvents. Rosstech 106FE CFC-free solvents are designed to replace toxic and hazardous cleaning solvents such as Xylene, Trichlor, Freon, MEK, Toluene and all ODCs and CFCs. They are also biodegradable. Various types are meant to remove grease, oils, flux, solder paste, cermet, inks, oxidised paint, uncured adhesives, etc., by wiping, immerslon and ultrasonic methods. Hughes Wynne Ltd, 0932569700.

## Power supplies

Small lead-acid battery. Claimed to be the smallest available, PowerSonic's PS605 sealed lead-acid battery is a 6 V type with a 500 mAh capacity, measuring 57 mm by 50 mm by 14 mm and fitted with surface contacts or wire leads. It can be charged up to 1000 times or floatcharged with a life expectancy of five years. The price at $£ 4.86$ is around 10\% cheaper than NiCd packs. Power-Sonic Europe Ltd, 0268 560686.

DC-to-DC converters. Combining wide input ranges and $80-96 \%$ efficiency, Powerline's CPR series of PCB-mounted converters are either dil 3 W types or 7 W models in a 2 in by

Probes for SM devices. Highdensity probes by Polar
Instruments for surface-mounted devices provide a test interface for ICs with lead pitches of 0.65 mm or 0.025 in . A retractable comb guides the 32 springloaded pins into contact with the IC pins and prevents them slipping off.
Polar Instruments Ltd, 0481 53081.

1 in package. Standard inputs are $9.5 \mathrm{~V}-36 \mathrm{~V}$ and $18 \mathrm{~V}-72 \mathrm{~V}$. Quiescent current is less than 5 mA at 24 V and less than 3 mA at 48 V . Powerline Electronics, 0734868567.

Modular power supply. Unipower's HPB series of power supplies incorporate a VDE level B interference filter, power-factor correction up to 0.98 and battery backup, all in a 5 by 9 by 11 in case. It is auto-ranging for global working and is fitted with six slots to take modules from the range of 25 available, which provide up to 1200 W at voltages from $2 \mathrm{~V} D \mathrm{t}$ to 48 V DC, dual and single. Unipower Europe Ltd, 0273420196.

## Switches and relays

High-temperature microswitch. For low-current switching at temperatures in the $-40^{\circ} \mathrm{C}$ to $120^{\circ} \mathrm{C}$ range, Cherry's Type $D C$ is available in a new version, which has a
silicone/neoprene temperatureresistant gasket to IP 67 rating to exclude oil, moisture and dust. Gold crosspoint contacts on a silver base enable the switching of currents down to 100 mA at 125 V AC , but 3A, 6A and 10A types are also made. A custom design facility is offered. Cherry Electrical Products, 0582763100.

Microswitch actuators. Push-button, panel-mounted actuators for the Burgess $V 4 \mathrm{~N}$ range of microswitches are on offer. The switches are intended for both power and logic switching and are in several styles,
including sealed versions. Actuators for close-tolerance work are available, which combine operating tolerance of $\pm 0.4 \mathrm{~mm}$ with minimum overtravel of 5.5 mm . Switches and actuators are ready assembled or in kits
Gothic Crellon Ltd, 0734788878.
Memory relays. A range of magnetic latching relays by Teledyne Electronic Technologles offer a method of switching incorporating a non-volatile memory. A 4.5 ms pulse sets the relay, which remains set until another pulse resets it. Single and two-pole changeover contacts cope with anything from low-level switching without wetting current to 1 A at 28 V DC. Two models in the range carry signals up to 4 GHz . Teledyne, 081 5719596.

## Transducers and sensors

Hall-effect sensors. Allegro's 3185 and 3187 Hall-effect latches are temperature-stable and stress-

One-slot processor card. The Blue Chip DXI is a single-slot card containing a PC based on processors ranging from 486SX25 to 486DX2-66, wth P24T Pentium versions coming shorlly Standard features include a VESA local-bus expansion slot, local-bus video with GUI accelerator, on-board solid-state disk and peripheral support. Onboard memory is to 64 Mb dram and to 256 Kb cache. Blue Chip Technology, 0244520222.

resistant magnetic sensor ICs working up to $150^{\circ} \mathrm{C}$. They are operated by the pole of a ring magnet, remaining latched until the opposite pole Is applied, the two types differing in the required field strength. The chips contain the sensor, voltage regulator, quadratic Hall generator, temperature compensation, signal amplifier, Schmitt and buffered open-collector output. Temperature compensation maintains operating symmetry. Allegro Microsystems Ltd, 0932 253355.

## COMPUTER

## Computer board level products

Neural network system. Combining data capture, learning and simulation, Amplicon's NT6000 neural networking system for 386 or higher PCs can be trained to perform tasks without the need for any programming. It combines neural networking software with a plug-in data acquisition and DSP board with eight 8 -bit or 12 -bit analogue inputs, two or four analogue outputs, digital I/o and a TMS320 DSP with 128 K on-board ram. The network is created on a graphical network editor and trained using the captured input data. Amplicon Liveline Ltd, 0800525335

IEEE 488.2 interface. This 488 PC2 interface board converts a PC XT/AT/ISAbus PC to an IEEE 488.2 controller and allows it to be used as an IEEE 488bus devlce. It performs all the basic functions as talker listener and system controller or controller-in-charge. The board is fully compatible with the IEEE 488.2 specification. The board is half length and supports 300Kbyte/s DMA transfers, a single switch selecting i/o address, DMA channel, interrupt level and wait states. Amplicon Liveline Ltd, 0800525335.

Memory cards. IBM
Microelectronics's memory cards and PCMCIA peripherals are strong enough, it is claimed, to bear the weight of a lorry, being contained in stainless steel welded packages. Lorry-strength sram cards for 5 V systems are now available up to 2Mbyte, having lithium cell compartments and bullt-in capacitors for up to two hours' data retention. There are also 4Mbyte flash cards and flash/sram combinations. Cards are to the PCMCIA type 2 format. Blue Micro, 0604603310.

## Computer systems

Industrial PC. AWS-850C from Fairchild is an industrial PC workstation with a 10 in colour thin-film transistor colour LCD screen, giving 100:1 contrast ratio, and a membrane keypad. Front panel is sealed to IP56. Printer port, keylock switch, floppy drive and LCD controls are protected by a lockable hinged panel and are accessible from the front. There is an optional touch screen. Processor options range from 286 to 486D×2-66 on plug-in CPU cards and an optional silicon disk allows boot-up and running without the need for floppy or hard disks. Fairchild Ltd, 0703 559090.

## Software

VHDL entry for PLDs and FPGAs. A VHDL-Direct facility, introduced by Data//O for ABEL-5, allows design entry and synthesis for programmable devices in VHDL, logic synthesis enabling users to describe circuits in VHDL at a much higher level than with language translators. VHDL Direct works in parallel with ABELHDL compiler and can be used as an optional front end for the $A B E L$ Device Fitter. Data I/O Ltd, 0734 440011

Algorithm development. Version 2.0 of LSI's Hypersignal for Windows generates C code automatically from a graphical signal-processing development package; the code for implementation of an algorithm is generated'directly from a block diagram assembled by the designer from blocks on the Windows worktop. Blocks represent "primitive" circuit functions and may be themselves formed by the user. There are drivers for asynchronous communication between host and target board; algorithms are simulated in real time via object code on the target DSP. Loughborough Sound Images Ltd, 0509231843.

Add-on LabView toolkit. New for LabView instrumentation software is
he Joint Time-Frequency Analysis Toolkit, which is an add-on virtual instrument library to increase LabView's capabilities on nonstationary signals. It includes the Time-Frequency Analyser for those not in possession of LabView but who wish to perform joint time-frequency analysis. Signals are acquired by data-acquisition hardware and one of the six algorithms transforms the signal, which is displayed as a twodimensional intensity plot of timefrequency data. National Instruments UK, 0635523545.

SpiceAge V3. Version 3 of SpiceAge for Windows simulates logic over ten times as fast as $\mathrm{V} 2-9$ s against 120 s on the digital test. A new 32-channel logic analyser display is available, more digital models are provided and input signal bus structures are supported. Zetex's analogue semiconductor library comes with the package and there is a new op-amp model to take advantage of the linear extrapolation in the SpiceAge polynomial functions. Redundant transient analysis calculations are now eliminated. Those Engineers Ltd, 081-906 0155.

## Computer peripherals

Hard disk microcontroller. H P's Kittyhawk microminiature 40 Mbyte hard disk, used mainly in personal computers, is now harnessed by Triangle, together with the TDS2020 computer, to make an industrial controller, the TDS2020HD, which incorporates the Forth language. Half a megabyte of data can be held in the computer, so that the hard disk needs to turn on only when that is used. The whole thing is less than 3in long, including the disk, and takes about 3 mA Triangle Digital Services Ltd, 081-539 0285



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LETTERS

## Spark beating

George Pickworth's article on spark transmitters $(E W+W W$, November 1993) refers to beating in the output wavetrain when the primary and secondary circuits are tuned to slightly different frequencies.

This is not right; beating will occur even if two circuits are tuned to the same frequency if, to get more power to the aerial, the output coupling is pushed beyond critical.

When done, the tuning curve becomes double-humped, and rf energy swings back and forth between primary and secondary circuits at a frequency dependent on the separation of the humps, producing an output train like Pickworth's Fig. 5d.
This has two unfortunate effects: the loss of rf energy because of the repeated recycling of of through the lossy primary circuit; and that the transmitter radiates on two frequencies instead of one, which is wasteful and irritating to other operators.
I always understood that the object of a carefully timed arc-break is, by making it happen when the wavetrain amplitude reaches its first maximum in the secondary circuit.
The primary circuit is effectively disconnected, leaving the aerial
circuit to radiate at its single natural frequency. Unnecessary primary losses are avoided and the aerial coupling can be above critical.
It is possible this only became relevant in later spark transmitter designs, in which case Mr Pick worth is right to leave them out. I don't know what sort of coupling coefficients Marconi used; presumably he made them as high as he could.
PEK Donaldson
Otford, Kent
I read George Pickworth's article The spark that gave radio to the world in $E W+W W$, November 1993. I have built and operated a laboratory version of a spark transmitter.
Mr Pickworth's description is interesting, and more or less factual, except he does not seem to clearly understand antennas. He makes several incorrect statements, one with reference to Fessenden's electrolytic detector. And, he gives minimal credit to Fessenden, who invented the rotary spark transmitter and radio as we know it today.

Mr Pickworth says early spark transmitters were untuned, which is not correct because the antenna is an L-C-R resonant circuit and therefore the antenna determined the oscillation frequency.

Including a secondary circuit does not change the frequency of a properly tuned transmitter and antenna system, but lengthens the train of damped waves. When the spark ceased in the primary the secondary continued to oscillate for a little bit longer because most energy had been transferred to the antenna circuit and the antenna had a return path to ground.
Fessenden devised the synchronous rotary spark transmitter in 1905. His transmitter produced sparks at a predetermined point on the input waveform. Therefore the magnitude of the peak of each damped wave was exactly the same - not varying with the point on each AC half cycle where the discharge occurred, as described by Pickworth.

Fessenden's rotary spark transmitter was a kind of mechanically quenched transmitter, since the spark ceased when the rotary terminal passed the stator terminal. His transmitter was probably the best quenched spark gap transmitter devised. The output tone would have been very much more clear and musical than the ones Mr Pickworth describes.
Fessenden's barretter or electrolytic detector was not a relay type as Pickworth said, but behaved like a modern detector.

The reproductions were such that operators using Fessenden's liquid barretter could identify several wireless telegraph stations in the pass band of the receiver by different characteristics of the spark transmissions - just as a friend's voice is recognised by its tone. It made possible the detection of voice and music when the hf alternator was invented in the fall of $1905-$ operating on a frequency of about 88 kHz .

## John S Belrose

Ottawa, Canada

## George Pickworth replies:

An article intended for a radio journal has to fealure a specific pioneer and subject but, as space is limited, essential references to other pioneers and radio systems have to be very short. As the article in question featured the evolution of Marconi's synchronised spark transmitter it is unreasonable to expect it 10 major on the work of Fessenden.

Nonetheless, I am a great admirer of Fessenden; his system was technically ahead of Marconi's but his achievements were overshadowed by publicity given to Marconi. I mentioned Fessenden's contribution to radio in my article 'Germany's imperial wireless

## Radio weariness

For some time we have been able to buy audio systems that sample cd levels and set an optimum amplitude before recording onto cassette. Now systems can automatically spectrum analyse and preset their own multichannel graphic equalisation.
Very clever; obviously the record producers did not really know what they were doing! But at least the new response is set and will not sudden ly change.
The letter from Robert Ellis ( $E W+W W$, November 1993) struck home with me, for I too am fed up with radio audio.
Active frequency-selective gain deviations are dynamically distracting and cause uncomfortable effects that once would have been seen as faults, such as pluminess on human voice, excessive sibilance, tiring transient distortions, and so on.
There is no point in buying a quality radio system for normal listening. Broadcasters with their hands on the technical tiller have blasted down-market straight through the high street.
Not even tv audio has escaped.
Transmitted distortion cannot be removed by the receiver, so it is not for the listener to choose and provide any processing beyond that necessary for reasonable modulation efficiency and linearity.
Take AM in particular. The last clean UK signal was Radio 3 medium wave. Now we have a national wall of noise on its old frequencies. Co-channel transmitters create
problems enough without the exuberant mush introduced by so-called optimum modulation processors at individual sites.
It is as though AM engineers have a fixation with electrical efficiency. The carrier is expensive, but there is no need to fully modulate it at all times. It is the carrier that sets the dynamic range - the stronger the signal field the quieter the background.
Normal compression techniques had been satisfactory for years, but now there are average signals in the $40 \%$ to $70 \%$ range unnaturally truncated at around $95 \%$ levels.
The combined effect of this active processing is that pre-radiation signal distortion can easily be $50 \%$ when compared to original linear levels; observe Radios 4 and 5.
And the problem is further compounded most receivers distort with high AM modulation levels. Long gone are the days when demodulation tests at $30 \%$ levels had relevance; see Jon Dyer's article ( $E W+W W$, December 1993).

Taking this topic further, Dyer says AM noise figures are 9 to 10 dB worse than for $\mathrm{SSB} / \mathrm{CW}$, and this has been accepted for too long.
Automatic audio processing renders modulation levels similar so, for any given bandwidth, one sideband of BFO recovered AM can be received as well as SSB; a method known to DXers as ECSS, or exalted carrier selectable sideband.
For true reception the BFO must be synchronised with the original carrier, but this is easily achieved.

Suppose we recover both AM sidebands, again with synchronous reception. Their components add coherently and recovered audio sounds much better.
Assume an 8 kHz DSB passband to recover
4 kHz audio. The recovered noise is that of two 4 kHz passbands adding, but not coherently, and this is relatively quieter.
Similar results are not so easily achieved with envelope detection, though a close approach is possible with sharp low pass audio filtering used to limit noise frequencies above half those of the passband, to quieten demodulation noise in the 4 to 8 kHz range.
Also too long accepted is the graph of atmospheric noise shown in Dyer's Fig. 1, and the mathematical minimum receiver sen sitivities based on it. I'm glad not all manufacturers rely on it.
Leipzig 531 kHz , Lithuania 666 kHz and Beograd 684 kHz are received here on back garden antennas with synchronous DSB during summer day time. Levels are obviously less than $5 \mu \mathrm{~V} / \mathrm{m}$ and hence much below chartered atmospheric noise.
If you want to hear the signals that are there, receiver sensitivities better than $1 \mu \mathrm{~V}$ are essential with predetermined wave polarisation and directional antennas in quiet conditions, even on medium wave.

As old timers will attest, it is real life performance that counts. Over technicalisation demeans progress.
Graham Maynard
Newtownabbey, $N$ Ireland
system' and again in the article
'Marconi's transatlantic transmitter' (EW+WW, January)
I am working on an article featuring Fessenden's work, which includes a study of my replica of his liquid or electrolytic detector. In the meantime I stand by my brief sidenote that the liquid detector is a relay device; it is triggered by rf current, but power which creates the sound in the earpiece flows from a local do source.

The term 'untuned' was invented by the pioneers to differentiate this early system from later systems using inductors and capacitors. As the word 'untuned' was deliberately placed in quotation marks and was supported by a schematic, I did not consider further explanation necessary for $\mathrm{EW}+\mathrm{WW}$ readers.
The principle of Fessenden's rotary discharger is the same as Marconi's one-dischargelAC halfcycle, synchronised-discharger. The physical difference is that Fessenden's system used a three phase alternator producing sequential discharges. So, for a given drive speed, discharge repetition rate and the resultant tone was higher than with Marconi's transmitter.
Finally, the earliest reference I have to the rotary discharger is that clearly descrihed in Tesla's 1898 Colorado Springs Notes

## Constructing solutions

I agree with your comment on amateur radio ( $E W+W W$, December 1993).

When I became interested in amateur radio at in the early 1970 s, I undertook all sorts of constructional projects. I almost got banned from the local club when I built a 2 m Super-regen that transmitted almost as good as it received.

It is true that interest in construction has waned to a point where few amateurs build anything of use, even though the quality and availability of components is at a level we only dreamed of in years gone by. It is only necessary to dismantle a modern tv set to get an idea of modern component technology.
Articles in your journal with data sheets of common semiconductors and suggestions as to how they could be used in
telecommunications would stimulate younger readers into reviving the art of construction.
Secondly, I am trying to find a data sheet for the C81-004 25 diode. It is probably made by Goldstar or Samsung and is used as a low
tension rectifier in a switching power supply. Can any of your readers help me find a replacement? Steve Banner G8FPG/OE3SBN Phone 01043747261357
Fax 01043747267481
Austria
I am a radio amateur and, in response to your comment (EW+WW, December 1993), the world is full of radio communications engineers using computers and modern electronics who have never had hands on experience with practical radio systems, and so an amateur in radio contributes significantly to a radio science laboratory.
John S Belrose
Ottawa, Canada
1 was interested in your comment on amateur radio ( $E W+W W$, December 1993). We live in an age of instant results responsible for attracting most radio amateurs to commercial equipment and the demise largely of home construction and experimenting.
Even if the challenge of experimenting with radio is only to one's own intellect, this is more worthwhile than communication with the new influx.

What I think we need to correct is a change to the licensing conditions that removes some facilities from users of commercial equipment and reinstates them only to experimental home-made stations. But since amateur radio is predominantly selfgoverning, a majority view will always find this unacceptable.
Tony Martin G4HBV
Hucclecote, Gloucester

## Naive and exotic

I think Graham Nalty's letter ( $E W+W W$, January) may do his cause more harm than good.

His dismissal of Drs Blake-

## Coleman and Yorke's letter

( $E W+W W$, May 1993) is as naive as it is insulting.
And his remarks about conduction and insulation, with no evidence, amount mainly to a re-run of the quasi-scientific spiel trotted out by exotic cable makers. Such statements may impress some hi-fi enthusiasts but are unlikely, as they stand, to carry much weight with the technical readership of this journal. If the cables are as good as claimed the matter deserves a convincing explanation.
Colin Latham
Beaumaris, Anglesey
In response to Graham Nalty
( $E W+W W$, January) I would like to raise three of many points on complex and exotic cables for

## Sick writers?

So vivid was Jerry Mead's description of his reaction to the faulty CMRR trimmer ( $E W+W W$, November 1993), that I too felt nauseous

Would it not be possible to conduct listening trials and put an end to this tedious debate?
I would contribute to the cost of such trials, as I am sure would many other readers. I suggest your journal organise these trials and collect contributions from readers. As for test subjects, perhaps some of the writers to the letters pages would be prepared to justify their claims.

## Alun Thomas

London

## Turning a deaf ear

Douglas Self's emotional attack ( $E W+W W$, January) on my description of listening in the development of audio-related products ( $E W+W W$, November 1993) is unconvincing.

Research has shown that, ergonomics, price and facilities all being acceptable, the audio equipment we build and sell will ultimately be judged by our customers' ears. They will buy one brand over another because it sounds better to them. They can identify audible differences.

Yet Self would have us believe these professional listeners are under-educated, delusional or tricksters, or visitors from Alpha Centauri, or just plain wrong. Sounds dangerously patronising and a little unlikely.
Like Self, many of us subjectivists (or listeners) have access to sophisticated test equipment and employ it with rigour. We want to correlate what we hear with measurement because it makes good commercial sense.
The full and proper use of such tools is vital if we are to further the art. The suggestion is, though, that we need to look a little beyond today's simple audio performance criteria of amplitude and frequency response if our measurements are to be relevant to our hearing mechanism.
It may be all well-conceived power amplifiers, mixing consoles and the like do sound the same to Self. That personal limitation, however, can hardly justify his persistent trivialising of my own and others' attempts to encourage constructive debate and wider research into this fascinating topic. If there was nothing more to do and learn then we could all have turned a deaf ear to this debate long ago.

## Jerry Mead

Royston, Herts
transmitting audio signals.
First, with the signal having already passed through several thousand metres of cables, PCBs and connectors, what difference will a mere dozen or so metres of exotic cable make?
Secondly, it is suggested that silver and PTFE have some mysterious physical qualities Nalty claims 'give a more focused sound'. This must be investigated as it appears the silver and PTFE combination can re-focus the damage to a signal caused by the thousands of metres of ordinary cable used in thousands of recording studios. The exotic cable story not only defies physics, it also defies sense.

The third point concerns another human faculty - sight. Why is there no great debate on the virtues of exotic cables and materials for video equipment? I assume the video signal, because of its higher operating frequency, broad
bandwidth and synchronisation requirements, is even more susceptible to cable types than audio signals.

Or is it perhaps easier to create myths and legends about audio because it is so much easier to dabble with than video?
Gareth Connor
London

## What happened to the allophone?

It is a general rule that as technologies mature they become available to a larger range of users. But there is an exception.
Some years ago several speech synthesis products were available to amateur users. National Semiconductor's Digitalker would speak one word from its fixed vocabulary when a digital word was entered and General Instruments'

SP0256 chips could say any message by stringing together a sequence of the 64 allophones it could produce. Both needed very little development equipment.
They had drawbacks. Both used single-polarity mos and had high power consumptions by today's cmos standards. The SP0256 paid for its infinite vocabulary with mediocre speech quality (it has been compared with a Dalek with adenoids). For whatever reason, neither device is available today
I am unaware of any available allophone-based speech synthesiser chip; their simplicity of development and infinite vocabulary are not available in current speech synthesis devices, which depend on large memories, data compression and expensive development kit (NEC) or analogue eeprom with limited message duration (Integrated Storage Devices and Sequoia).
While both these devices give excellent quality, I regret that no manufacturer has produced a cmos allophone-based speech synthesiser with its inherently infinite vocabulary and simple development. The absence of such devices complicates life for anybody who wants to put together a one-off speaking device for, perhaps, a visually handicapped user.
Colin Attenborough
Waterbeach, Cambs

## Long live Archimedes

I am very pleased that the subject of Windows versus Risc Os has been aired (EW $+W W$, December 1993). I also agree with Les May's comments.
I have two primary school children and in 1992 as the season of glad tidings made its inevitable approach, we decided that it would be nice to buy them a computer.
I was determined that they would not get some mind-numbing games only piece of electronic exploitation, but a real computer.

The question was which? I already own a somewhat ageing XT PC and have been using PCs at work for word processing and cad. The children, however, use Acorn computers at school.
After much soul searching we took the plunge and purchased an Acorn Archimedes A3010. The first impression (apart from the lower resolution screen) is the sheer speed and ease with which the GUI operates. Having the operating system in rom is an advantage but I wonder how many Windows machines can go from cold to the desktop in 15 s . It was not long before I realised that this machine is

## Oven gloves

With reference to Ann C Arnold Silk's letter (EW + WW, January), I agree that a little research always makes communication more worthwhile. It is therefore with regret that I note she didn't have time 10 read my letter ( $E W+W W$, October 1993) before replying to it.
Had she done she would have seen my comments refer to the claim that bodily organs responded to certain acoustical frequencies; in other words an inappropriate musical note might send a concert audience plummeting into insulin coma due to some sort of mercifully
imaginary pancreatic resonance.
I would not seek to deny the human body responds to electromagnetic radiation; the simple experiment of placing the head in a suitably modified microwave oven should convince even the most sceptical.
Silk's letter, on the other hand, deals only with electromagnetism, which has nothing to do with the point I was making. This was that, while the original assertion is obviously nonsense, since it appears in an authoritative journal such as $E W+W W$, it cannot pass without challenge. Without hanging onto some sense of true and false, where are we?
Douglas Self,
London
more than just a learning computer.
So why is the Arc not more successful? It is no good wringing our hands and moaning about the remuneration of Messrs Gates et al. We are the ones who buy from them and then pay them again and again to correct the deficiencies and errors in their product. They have lived well on our belief that we need the latest this, that or whatever in computer systems.
There are two basic answers. One is compatibility the other, marketing.
Despite the fact that the $B B C$ Micro was in before the IBM PC, IBM attacked the global marketplace with aggression. Remember the Charlie Chaplin adverts? The Beeb was always considered as the first choice for education but the PC gained acceptance in industry worldwide. The need to keep compatibility with older hardware and software has proved to be lucrative and restricting for Microsoft and Intel.
I believe Acorn must polish up its act when it comes to selling computers outside of the classroom. It is no good expecting the average punter to take an objective view of this computer's features versus that and make a sound decision. They have to be told.
It must open up the Archimedes architecture to third parties. Cloning is one of the reasons the IBM compatible machine has gained such world dominance. It should also look hard at who it chooses to market its products. Did you know, for example, that Dixons is supposed to be selling Acorns? Wander into most of its stores and you will quickly see where it thinks its profits lie.

And what about Acorn's owner Olivetti? Surely here is a conflict of
interests. If your parent company is actively engaged in the manufacture of PC clones I believe that one is bound to suffer at the hands of the other.
Like the VHS versus Betamax battle, it is not necessarily the best that wins but the best promoted. Hopefully when the Archimedes generation leave school they will have different ideas about what they want from a computer.

## Simon Wyre

Salisbury, Wilts

## The song should not remain the same

I agree with your comment (EW+WW, January) that the dream of a hard-disk-free computer should have been reality long ago.
Yet there have been attempts. I wrote this letter on a 1985 Atari ST. This machine was after the costly Apple Macintosh, the first solution of a computer with integrated operating system and graphical user interface.
The further development of this computer shows the problems on the way to solid-state computers: the operating system had several very unpleasant bugs and the first solution is the boot disk!
I collected many public domain products to solve the problems, maintain ram-disks and so on. Soon the spacious 800 K byte of free memory was too small for all the patches and utility programs. I fitted a ram upgrade to 4Mbyte, connected a 240 Mbyte hard disk, all of which worked perfectly.
It is a pleasure to have programs run up in half a second rather than half a minute!
Updating is the real enemy of a stable solid-state computer. Build a
perfect machine today, and someone will have a better solution
tomorrow.
Give the incredible amount of 100 Mbyte to a programmer, and he or she will fill it up at with unnecessary stuff that no-one wants to miss afterwards. Do you want to miss the animated racing horse cursor of Windows NT in favour of a stupid hourglass? Never again. Modesty is an unknown word to computer users and programmers.
Since the arrival of C ,
programming in assembler is really out. No programmer is interested to know the details of the machine he or she is dealing with, and so most programs like spreadsheets, wordprocessors and such have to fulfil the smallest common denominator.
This means, for less sophisticated machines, the programs have to be oversized and the code modules grant a flexible combination for the implementation at the cost of inefficiency and code size.
As long as the cycles of update and replacement of existing programs come shorter, no one will even try to use all the potential of a special machine. Software today is like hit-list music: you hear it all day for weeks, and then you look for the next one because you can no longer stand the old song.
Maybe the recession gives a chance for a rest. Who says that not producing new technology on the hardware side means a stagnation on software? I hope a rethinking will start on the goal of reducing hardware garbage with a more creative use of the existing platforms, leading to leaner and more use-oriented software.

## Johnnes M Heuss

Nürnberg, Germany

## Science or religion?

Michael Weatherill's letter (EW +WW, December 1993) demonstrates the gulf that can sometimes exist between theory and practice. It is fortunate that the magazine's liberal editorial policy permits occasionally widely different viewpoints to be aired. Electromagnetic wave propagation is still a bit of a black art that requires more not less light shed on it.

Equating velocity of electromagnetic waves involves $\varepsilon_{\tau}$ and $\mu_{\mathrm{r}}$. If both are unity then $\nu=c$, the speed of light in a vacuum, which according to the Weatherill school of thought is about $299,792,458 \mathrm{~m} / \mathrm{s}$ give or take a few nanoseconds.
But how can $\varepsilon_{\mathrm{r}}$ and $\mu_{\mathrm{r}}$ be unity
when the measurement is made within the Earth's magnetosphere, which extends several times beyond the geosynchronous satellite orbit, beneath which the global positioning satellites circulate? And beneath the GPS orbit, water vapour, cloud cover, rain, snow and sleet must have some effect on $\varepsilon_{r}$.
The Earth is basically a large chunk of iron which has a $\mu_{r}$ up to 9000 surrounded by all three states of water with $\varepsilon_{\mathrm{r}}$ up to 75 !
So why should one expect c to be measurable to any degree of accuracy in near earth conditions? Also space is not so much space as a vast envelope of a variety of materials of extremely variable density; so why expect $c$ to be constant in space?
The excellent and very practical series on the GPS system by Philip Mattos shows that the biggest correction which has to be made by the user is for ionospheric distortion accounting for about 30 m of error budget.
This can be seen in graphic form in his fifth article ( $E W+W W$, April 1993). A distance of 30 m or about 100 ns in a transit time of about $1 / 6 \mathrm{~s}$ corresponds to an error of around 600 ns per second instead of the few nanoseconds which appears to be implied by Weatherill's letter.
Is it not about time that a determined effort is made to plot $v$ and characteristic impedance throughout explorable space? The commonly held misconception appears to be that $v=c$ anywhere beyond a few feet above ground level.
Euan Orr
Portchester, Hants

## Transmitter request

I am looking for a T1154 type aircraft transmitter to help me complete an aircraft restoration project.
This will be used for static display only so the transmitter does not have to be in working order.
Can any of your readers help? John Boden
Lewiston, Australia

## Choking fusion

In my letter 'Out in the cold' ( $E W+W W$, December 1993), I suggested those who challenged the cold fusion claim by tests assuring more precise and controlled measurement of temperature were choking off the possibility of a fusion reaction by ensuring there could be no adequate temperature gradient in the palladium cathode.
That gradient, if non-linear, sets up a thermoelectric effect that affects the deployment of residual
charge inside the metal and that charge, if negative, can bring two positive deuterons into a fusing relationship.
Thermoelectric effects also arise where two different metals combine and there is a temperature difference between them.
My message was that heat was needed as an input trigger to get the fusion reaction going inside that host metal and if one avoided heat differentials one was not performing a valid test.
Readers may find interesting an NTT Japanese press announcement in December 1992, which declared that when thin films were used, in which palladium was first filled with deuterium and then a thin layer of gold deposited on top of that film, the application of heat had a trigger effect by which the temperature of the palladium suddenly rose several hundred degrees and the production of helium-4 showed there was a fusion reaction.

## Harold Aspden

Chilworth, Southampton

## Beyond Windows

I read with interest the correspondence on Windows ( $E W+W W$, December 1993).
Les May finds it hard to believe people are not finding worthwhile and commercially viable uses for computers like the Amiga, Atari or Acorn Risc machines. In the last of the three letters, RG Silson asks: "When will someone produce a 32bit operating system that combines all essential basic facilities with maximum processor utilisation and excludes complex gimmicks?"

This has been done in the form of the SMS2 multitasking operating system that runs on the Atari ST machines. This comes with pointer driven user interface on a twin AT29C512 Perom rom board that plugs into the Atari cartridge slot and takes over the machine. A hard disc is not essential.
This should be particularly attractive to programmers because of the speed, efficiency and simplicity of SMS2. Anyone interested could obtain further details from Furst of Southampton. Tel: 0703322132.

## Frank Gutteridge

Geneva, Switzerland

## Cricket is not calculus

On the 13th January, I watched a programme 'Big science' on BBC2 in which Mark Ramprakash cooperated in a scientific experiment that suggested the human brain's calculations required to catch a
cricket ball involved complex calculus.

All references I can find say calculus was invented independently by the 17th century mathematicians Isaac Newton in England and Gottfried von Leibniz in Germany.
This surely poses a number of questions, not least of which is: Was calculus invented or discovered?
If the human brain involves calculus in its calculations to guide the body to intercept a moving object then it must surely follow that calculus was discovered as it is well known that man and animals have been intercepting moving objects for millions of years.
May I suggest that what has occurred in the cricket ball experiment is that a statistically obtained formula has been made to fit the observed data and that it appears obvious that something very different applies.

If calculus was discovered, then might I claim independent recognition for its discovery on behalf of my two dogs who can also intercept moving objects.

## John A McKay

Settle, Yorkshire

## Lining up

I have no knowledge of how the statistics of power lines causing cancer are calculated but guess it is a case of population living under a power line compared with population not living under a power line.

The effect under what is relatively a single diniension, the power line, is being compared to the effect over a two dimensional area, the area where the rest of the population live.
Surely a true comparison can only be obtained by comparing those living under a power line with those living under an imaginary line parallel to and of the same dimensions as the power line and traversing a similar terrain. Any other comparison will be biased.

## Kelvin Vaughan

Bishops Stortford, Herts

## Any old valves

I draw your attention to an article "The development of radio valves" by Dr JHE Griffiths in Proceedings IEE.

Griffiths mentions 51 valves with CV numbers, and 15 others, and gives brief outlines of their development and use. There were more than 1000 CV common valve numbers issued by various military groups in the UK and the US by the end of WW2, and about 5000 subsequently.

I am anxious to know if there exists a record of the data,

## Cold magnets <br> With all the talk of room

 temperature superconductors, could it be they are all around us in the form of permanent magnets?In this case the currents are not evident in an extemal circuit but I wonder what might happen with wires or strips made from some newer permanent magnet materials such as rare earth cobalt or neodymium iron boron.
Pass a powerful current through the wire or strip, perhaps as it cooled from its critical point, and the magnetic field will not be along the wire as when magnetised with a solenoid but inside the material, perhaps with a superconducting core.
If so, will it conduct better in a unilateral direction like a sort of rectifier or will there be no change in the material's conductive properties?
After all, it seems there are strong reasons to suppose the new superconductors are very like permanent magnet materials - hard and brittle and difficult to shape and handle.
I would be interested to know if any research has been attempted along these lines.
A) Quinton

Victoria, Australia
manufacturing details, and test procedures of these valves.

Very few of them had commercial equivalents, but those that did were published in this joumal in 1946. I do know there were at least two sets in Australia, but they were never declassified and were destroyed.

## Peter Ward

Victoria, Australia

## Under the sun

I was surprised reading Michael Williams' article 'Making a linear difference to square law fets' ( $E W+W W$, January) to find with three decades in electronics hechas not seen the books of FE Terman the guru of radio engineering when I was young.

In his Measurements in radio engineering in 1935 he describes a power meter using the D2S principle. A current derived voltage was applied differentially to the grids of a pair of square-law triode valves and the voltage component was applied in phase to the two grids. The difference between the two plate voltages gave the true power, taking into account the power factor.

He repeated the circuit in his Radio engineers handbook in 1943.

As an apprentice about 60 years ago I helped develop such a device. The problem was in catching one's goose before one could cook it - not many triodes had extensive squarelaw characteristics.
Terman describes another feature of the square-law characteristic which lets the output level of a second harmonic signal generator be accurately defined by the rectified anode current.

I have used a similar principle in bridge work where one needs to balance a variable capacitor in one arm against an unknown capacitance in another. Usually a straight line capacitance law is required but such components are difficult to find. By using a variable capacitor in each arm, and operating them differentially through insulated gearing, a more linear scale is obtained from commercially available capacitors.
This is because the capacitance law can be represented by a power series and the even powered terms cancel out. This system also avoids the need for an additional capacitor for zero setting since initial balance is obtained at roughly the mid-range of the two units and scale zero can be set by moving the cursor to the calibration point. No switching is required to measure $L$ and $C$ but this is at the cost of halving the available range.
Truly as the preacher said there is no new thing under the sun.

## SF Brown

Pant, Shropshire

## Blessed memory

With regard to the article 'Making a linear difference to square law FETs' ( $E W+W W$, January), perhaps it should be mentioned that the principle is that employed in the quarter square multiplier found in analogue computers of blessed memory. The square law functions were then formed by resistor and diode networks.

## D Owen

Crawley, West Sussex

## Console defence

While I have not followed every detail of the relay versus solid state switch device debate, I would like to add my comments on three aspects in the letter from Mike Meechan ( $E W+W W$, December 1993).
He is right when he says Focusrite studio consoles cost a couple of hundred thousand pounds each, but this is very competitive with other world class consoles offering similar facilities implementing their audio switching with solid state devices.

Our design approach lets us offer significantly better switching and audio performance than other products with solid state switching devices. The reliability of any switch circuit depends on many aspects. The individual component quality and construction can be critical, but the surrounding circuit configuration will usually have a greater effect.
Meechan's comments about the careful design of the surrounding environment should apply equally whatever switching device is used. Relays are no more onerous than solid state devices, and in many ways easier, allowing complete electrical isolation between logic and audio systems.
Good engineering does not have to add insidiously to the cost of a product. Good quality does not always cost more than poor quality.

## Richard Salter

Focusrite Audio Engineering

## Bourne End

## Anyone from Bolton?

May I appeal to readers who are former students of Bolton Institute of Higher Education or who, before 1982, attended Bolton College of Education (Technical) or Bolton Institute of Technology.

We shall also be glad to hear from anyone who during the last 50 years or so prior to the institute's creation pursued a higher-level course in
Bolton, for example at Bolton
College of Art or Bolton Technical College.

Bolton Institute is setting up an alumni association and we are trying to trace anyone who has studied at the institute, no matter when, as we want to reestablish contact.
This year we hope the institute will become Bolton University, and former students will be invited to celebrate with us. We hope also to establish international alumni associations in other countries.

Please write to Jan Lancaster, alumni relations officer, Bolton Institute, Deane Road, Bolton BL3 5 AB , or phone 020428851
extension 3808, or fax us on 0204 399074.

Dr R Oxtoby
Principal, Bolton Institute
Bolton, Lancs

## True arrogance

I was pleased to see that Michael Weatherill ( $E W+W W$, December 1993) has presented the establishment view of the constancy of the speed of light. I still find difficulty in reconciling his views
with the observed Doppler effect as it affects electromagnetic radiation.
I have even more difficulty in accepting his accusation of arrogance. None of us who write to this journal asking how the accepted theories can be reconciled with the facts as we know them is casting doubt on the brilliance of those giants whose theories are accepted by the establishment.
If there is difficulty in answering our enquiries then our questions may be annoying to those who accept the established doctrine without doubt but no one can ever be accused of arrogance for asking how and why.
True arrogance lies with those who tell us we have no right to ask questions about theories because the originators of those theories are such great thinkers. Had questioners accepted such advice long ago we might well be still believing in a flat earth.

Weatherill's argument is not helped by his reference to the global positioning system 'assuming the speed of light to be constant' when your own series on the GPS in December 1992 tells us the speed of light varies due to gravity.
My problem is that if a light signal is emitted by a source at speed $c$, travels to a destination and is received at speed $c$ then if the destination is moving away from the source and so increasing the distance from the source then how did the light reach the destination without travelling at a speed greater than $c$ ?
Weatherill implies speed is nothing more than the relationship between time and distance and if he is firm in his beliefs then he must be able to explain how, if distance is increasing, speed and time remain constant.

Or does he merely solve the difficulty by accepting as an article of faith that $c$ is constant? If so, we have left the realm of science for religion and I am reading the wrong journal.

## Martin W Berner

## Trinidad

## Studying Sagnac

Your journal has been carrying the debate about whether or not the results of the Michelson-Morley experiment and Airy's failure constitute a proof (or at least strong evidence) for a stationary earth. I am writing to respond to the letter by Michael Weatherill ( $E W+W W$, December 1993).

Although relativity can explain why the relative velocity of earth and space (or ether) is not detectable (it does so by applying an elliptical transform to Newton's equations of
motion), it cannot explain the Sagnac effect.
Sagnac's experiment, repeated on a large scale by Michelson, Gale and Pearson, shows a relative rotation of the earth and ether. So we have a dilemma: on the one hand we cannot detect any orbital motion of the earth, but we can detect a relative rotation.
Einstein's theory of relativity is contradicted by the Sagnac effect. Thus things are not as clear-cut as Weatherill believes.
Likewise, in a 1977 paper, PF Browne concluded that the geocentric model could be falsified if the universe is assumed to be the smallest isolated system. This means that the only way to tell would be to go outside the universe, look around, and then communicate from there back into the universe. Since we cannot do that, the burden of proof shifts from physics to theology. The question of the immobility of the earth is no longer a question answerable by physics.

It appears that the geocentric theory has not been exorcised by the likes of relativity. Several papers over the last century concur with that conclusion.

A 1977 paper by Barbour and Bertotti is of particular interest, for the authors show that relativistic and some quantum mechanical effects result automatically from a geocentric model. And they derive the correct perihelion precessions for Venus, Mars and Mercury.

By contrast, relativity can only account for the perihelion precession of Mercury. These factors suggest that the geocentric model may be more comprehensive than the modern heliocentric view. This is not surprising since the heliocentric view generally ignores the universe whereas the geocentric view incorporates the presence of the universe into almost all its derivations.
As well as the work of these thinkers, I have shown in a paper last year that the presence of Planck particles in physics (particles that follow from the values of physical constants, particularly the speed of light, Planck's constant and the gravitational constant, which combine to yield a mass of $10^{-5} \mathrm{~g}$ x size of $10^{33} \mathrm{~cm}$, time of $10^{-44} \mathrm{~s}$ and density of $10^{93} \mathrm{~g} / \mathrm{cm}^{3}$ ) requires that, for the universe to be stable, it must rotate with a period of about 24 hours.
It seems that the geocentric mind is not as devoid of thought as Weatherill would have us believe.

## Gerardus D Bouw

Association for Biblical Astronomy Ohio, USA

# Electronic encineers REFERENCE BOOK 

## T

 his reference book is divided into five parts: techniques, physical phenomena, materials and components; electronic design and applications. The sixth edition was updated throughout to take into account changes in standards and materials as well as advances in techniques, and was expanded to include new chapters on surface mount technology, hardware and software design techniques, semi-custom electronics and data communications.Fraidoon Mazda has worked in the electronics and telecommunications industry for over twenty years, and is currently Product and Operations Manager, Generic Network Management, with Northern Telecom. He is the author of six technical books (translated into four languages) and the editor of the Communications Engineers Reference Book published by ButterworthHeinemann.

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## V LS <br> |:

# design language present and future 

> Programmable gate arrays offer even the smallest user the possibility of integrating a complete system onto a single chip. Such complexity cannot be handled without software tools which can describe the system as functional components working together. By Simon Parry

The major problem in VLSI and systems design is managing complexity. The commonplace dram may use many millions of transistors but it has a regular, easily understood structure. A microprocessor, or specialist digital signal processing IC, may have an equal number of transistors but will have them divided between a collection of complex functions. These ICs are a serious design challenge.
Silicon systems designers are turning to a shorthand which uses functional descriptions to imply structure. The further along the path the engineer proceeds, the more the description becomes compacted, implying greater functionality and structure, at each step. A hardware description language (HDL) helps the engineer in that role by providing a standard means of describing electronic functions at many levels of abstraction. Its purpose is to simplify and speed the design process.
This seemingly rarefied design technique increasingly applies to low volumes and small

companies. The great benefit of VLSI development has been its availability to the whole industry. Even the smallest hardware design company may routinely use field programmable logic arrays (FPGAs) and even metal-programmable gate arrays (ASICs). These may also benefit from HDL design entry.
The change, though beneficial, has brought its own demands. Widening the appeal of VLSI has required appropriate design tools for complex circuits.
A consequence of this cycle has been the expectation of greater productivity from engineers. If a hardware designer of five years ago, say, was content with completing one or two huindred gates per month, his modern day counterpart must aim for around 1000 . Yet productivity may not exclude quality; completing the design of a circuit with 1000 gates within one month is worthless if they are just plain wrong.
The history of HDLs is short but full. There are been many proprietary languages and some de facto industry standards, such as Verilog. But the establishment of VHDL as an IEEE standard at the time that VLSI entered many engineer's lives has seen HDLs become a basic part of the design tool kit.
Any HDL, whether a standard or not, is a software language in which an engineer can describe, and iteratively refine, a design concept for a circuit. The process often starts with a model of the complete system architecture, proceeds through abstract notions of the system's functional elements, to detailed logic and individual circuit elements such as transistors. Along the way, these models are repeatedly simulated and tested to check that,

[^0]at each stage of refinement, the detail has remained true to the original description.
The single most important reason for using an VHDL is to save time and money. Any electronic component or circuit - single logic gates or massively parallel computers - can be described in terms of a behavioural function, like a decoder that has inputs, a series of transfer equations and outputs. The inputs can first be represented as integers, refined as bit patterns, with a corresponding change in the equations, until finally the circuit description is composed of a matrix of logic gates.
This design flow imposes a rigour upon the engineer that is often lacking in other design environments. It forces him to think about the circuit's intended function: if a component has to add two numbers, the VHDL code must include an ADD statement at the functional level that, when simulated, will actually add two numbers together. The outcome of this reflection is a circuit that works as originally envisaged, with no specification errors and, hopefully, no time or money spent correcting them.
VHDL is like a programming language to some degree. The difference is that VHDL allows designers to model structure as well as behaviour, the timing relationships between structural elements, and signal rise and fall times.
There are other similarities to program software. VHDL allows the engineer to reuse models written for a previous circuit and to define alternative representations of a given design... A serial or parallel implementation, for example. The different constructions have the same interface, since the serial to parallel conversion takes place inside the circuit block, but one might perform better than the other.
Employing VHDL across a company can also have important productivity benefits. Designers may exchange models easily with others working on different projects; VHDL maintains the same external behaviour of a functional block but allows the lower level construction to change for different applications.
Finally, hierarchy is an important characteristic of any useful VHDL code because it underpins several significant design techniques.
First, the ability to ignore extraneous design detail lets the user concentrate on the functional block that concerns him. It also allows work in the structural domain using only the names of the arithmetic and logic units.
Second, functionally decomposing the entire circuit into manageable pieces helps give the engineer a better understanding of the total concept. Consequently, he is less likely to make mistakes because of a misunderstanding.
Lastly, and perhaps most significantly, because the design can be partitioned easily using VHDL, a number of designers can work on different functional blocks all at once. Each will have a clear idea of his piece of the pie.
Although a separate VHDL simulator can bestow useful benefits in the design environment and is often the first step towards an

## All in the code

The hierarchical nature of VHDL allows the engineer to specify a circuit component at a number of abstrction levels. For example a description of a full adder may be any one of these three descriptions:
architecture behavioural view of full adder is
begin
process
variable $N$ : integer;
constant sum_vector : bit_vector (0 to 3) := "0101";
constant car $\bar{r} y_{-} v e c t o r ~: ~ b i ̄ t \_v e c t o r ~(0 ~ t o ~ 3) ~:=~ " 0011 " ; ~ ;$
begin
wait on $X, Y, C i n$;
$\mathrm{N}:=0$;
if $X=' 1$ ' then $N:=N+1$; end if;
if $\mathrm{Y}=$ ' 1 ' then $\mathrm{N}:=\mathrm{N}+1$; end if;
if Cin = ' 1 ' then $N:=N+1$; end if;
Sums <= sum_vector ( N ) after 20 ns ;
Cout <= carry_vector $(\mathrm{N})$ after 30 ns ;
end process;
end behavioural_view;
architecture dataflow_view of full adder is
signal S : bit;
begin
$\mathrm{S}<=\mathrm{X}$ xor Y after 10 ns ;
Sum <= S xor Cin after 10 ns ;
Cout $<=(X$ and $Y)$ or ( $S$ and Cin) after 20 ns;
end dataflow_view;
architecture structure view of full adder is
component half adder port (I1, I2 : in bit; C,S : out bit); end component;
component or_gate port (I1, I2 : in bit; 0 : out bit); end component;
signal $a, b, c$ : bit;
begin
U1 : half adder port map $(X, Y, a, b)$;
U2 : half_adder port map ( $c, C i n, c, S u m$ ) ;
U3 : or_gäte port map (a, c, Cout);
end structure_view;

This example clarifies how hardware-orientated design works showing the main features of the design style. The circuit performs the crossproduct of two vectors of integers.
package cross product types is
type int_vector is array (integer range $\rangle$ ) of integer;
end;
use work.cross product types.all;
entity cross_product is
port ( $a, b$ : in int_vector ( 10 to 7); result : out integer);
end;
architecture system of cross_product is
begin

```
        process (a,b)
```

variable accumulator : integer;
begin
accumulator $:=0$;
for $i$ in a'range loop
accumulator: $:=$ accumulator $+(a(i)$ * $b(i))$;
end loop;
result <= accumulator;
end process;
end;
integrated HDL based design system, the maximum advantage is gained from the combination of VHDL and logic synthesis.

## Logic synthesis

Logic synthesis automates the decomposition of the lower layers of a VHDL description into logic gate primitives. Many engineers consider its inclusion as decisive and, in reality, VHDL and logic synthesis are often viewed as an inseparable single entity.

VHDL was developed as a hardware description language which could be used at every stage of the design process, from system specification to a gate-level netlist. It tries to be all things to all engineers and, although this ambitious objective has been largely achieved, there is some confusion over how VHDL should be written throughout the design cycle.
A different style of VHDL must be used for each level of the design. This is particularly true when logic synthesis is to be employed
where the use of the language must be constrained to those structures which have a hardware mapping. A disciplined approach is needed to get the most from synthesis.
Logic synthesis works on a register-transfer model of a circuit. Register-transfer design is a grand name for a simple concept in which a circuit is depicted as a set of registers with transfer functions describing the flow of data between them. The registers are implemented directly as flip-flops, while the transfer functions become blocks of combinational logic. This division of the circuit is an important part of the design process and should be the main objective of the engineer using synthesis.
The written style of VHDL for synthesis should have a direct one-to-one relationship with the registers and transfer functions in the circuit. The first stage of the design process is to specify at a system level what is to be achieved by the circuit. Typically this will be a set of arithmetic and logic operations on data at the primary inputs. At this stage there is no hardware implementation in mind; the purpose is simply to create a simulation model which can be used as the formal design specification. The system level model can also be used to confirm that a customer's requirements have been understood.

## The history of VHDL

TThe VHDL language was created to mute the US Department of Defense's growing Tower of Babel. Numerous electronic systems had been designed using incompatible languages and engineers could not understand the systems' design descriptions because they did not know the languages.
The development of the language was contracted out to a consortium of IBM, Texas Instruments and Intermetrics in 1983 under the aegis of the DoD's Very High Speed Integrated Circuit (VHSIC) programme. This is the origin of the language's name: the VHSIC Hardware Description Language or VHDL for short.
The language was finally ratified by the IEEE as a standard - IEEE 1076 - in 1987. It quickly attracted both a loyal following and bitter criticism in equal measure. Proponents believed it would be a new beginning for language based hardware design. It would replace proprietary HDLs because it was a de jure standard. Opponents, however, preferred languages expressly designed for systems hardware design - not for description and documentation purposes.
The adoption of the language was spurred by MILSTD 454L which mandates that all asic designs completed for DoD projects be documented in VHDL. It was then just

The second stage is to transform the system level specification into a register-transfer design. However, it is rare for a direct transformation to take place.
If, for example, the circuit performs a number of multiplications, the area of the direct implementation would be excessive. Hence the transformation process identifies the number of registers required and makes changes to the data flow to allow sharing of critical hardware resources. The VHDL model of the register transfer design can be simulated and checked against the system specification.
The third stage is to synthesise the register transfer design. The resulting gate level netlist may be simulated against the register transfer design to confirm that the synthesised circuit has the same behaviour. Finally, the netlist or schematic produced by the synthesis package is supplied to the placement and routing tools for layout.
The main purpose in establishing a distinct, synthesis related design style is to achieve a number of objectives such as control of the design process, design maintenance, design debug and reusability. A direct and clear mapping from the VHDL model to hardware implies there should be no unpleasant surprises after synthesis.
a short step to employing VHDL throughout the design cycle.
The past two years have been eventful ones. The language had met with wide industry acceptance and was becoming the premier hardware design language. However, VHDL had been a standard for five years and the IEEE stipulates that every standard must be reaffirmed in that period. Consequently teams of engineers were working hard to revise and redefine VHDL so that it could become a new standard IEEE 1076-92.
Voting on proposed changes first took place in 1992 which resulted in a substantial revision of the language. Several more months work followed to document these changes before VHDL92 was ratified by the Standards Board of the IEEE in September 1993.
Shortage of time caused a number of proposed changes to be excluded from this revision of the standard. However, a number of IEEE working groups were established to address these issues which included timing and back annotation, analogue VHDL, standard synthesis packages, standard maths packages and formal methods and verification. Some of these requirements have already been developed in bodies such as Vital. Others will be included in the next revision of the language in 1997.

A VHDL model could have a long life. It may be revised by different engineers and sections may be incorporated into other designs. Consequently the VHDL code has to be readable and easy to follow. The design style should make the flow of data in the circuit visible so that it can be debugged using current VHDL simulators. The design should be partitioned in such a way that subcomponents can be simulated and debugged in isolation. Also general purpose subcomponents should be identified so that they can be isolated and bundled into libraries for future use.
In the same vein, existing subcomponents which have already been placed in libraries should be used wherever possible.
Bearing in mind these objectives, there are good and bad design styles for synthesis. A poor style often used by inexperienced engineers is software oriented design. It is characterised by large processes with extensive use of functions and procedures as the main means of partitioning.
This causes several major problems. First, control of the design process is difficult because there is no clear one-to-one mapping from sequential VHDL to hardware. The size of circuit which implements a particular function may, for example, vary considerably depending on the parameters passed to that function. An innocuous looking section of VHDL code may, in fact, occupy considerable circuit area. Also subprograms cannot define registers - they can only describe combinational logic.
Secondly, the sequential VHDL code is often complex and hard to understand, making modifications and maintenance difficult. Also, debugging the code is troublesome because the data flow is largely characterised by variables instead of signals; most simulators give only limited visibility of variables and some give none at all.
Finally, although packages of functions and procedures may be reused, they are never as flexible or easy to use as generic components and are more difficult to write in a general form.
Recommended VHDL design style could be classed as hardware orientated. It is characterised by concurrent signal assignments, simple processes and the extensive use of components as the main means of partitioning. It has several advantages. Control of the design process is now much simpler to perform because there is a direct mapping from concurrent signal assignments to hardware. The size of the circuit is easier to judge from the VHDL code and, since the registers are explicitly stated, there is a direct correspondence from the register transfer design to the circuit.
The VHDL code is easier to read and therefore to modify and maintain. Debugging is uncomplicated because the data flow is via signals providing visibility of all intermediate values; the extensive use of components allows each one of them to be simulated in isolation. Also components are ideal for future reuse and can be written in a generic fashion to retain flexibility.

The vital library
A third, crucial element in a VHDL design flow is a model library - a set of circuit primitives - that directly pass timing and layout information back to the VHDL simulator. This is the business of the Vital initiative, which is developing a standard for VHDL Asic library modelling practices.
The motivation behind Vital was to standardise timing functions, primitives and modelling practices so that asic vendors could have a universal syntax for describing library cells. The work has drawn heavily on the existing IEEE 1164.1 standard, which is the basis of VHDL multi-value logic system (MLV-9) and the pin-to-pin delay mechanism employed by Cadence's Verilog simulator.
A Vital model contains the functional behaviour and timing characteristics of the device. These are held separately so that all the tools employed in the design cycle, such as simulator, synthesis package, timing analyser and delay calculators, use a single library. Tools which require timing information read from the timing file while others, such as place and route software, are allowed to modify it.
This separation of timing and functional data also allows asic vendors to use the same library across different process technologies while simplifying production and maintenance. Distinct equation in the delay calcula-

The typical design in the HDL-equipped environment proceeds from a behavioural description of the system specification through several stages of refinement and logic synthesis to a gate level implementation. The engineer that doesn't use an HDL has to start at the gate level which is an overly complicated start point and extremely error-prone.
tor accommodate the different process performances.
The first Vital compliant model libraries from Asic vendors will probably be launched during the next few months. When this happens the final major link will have been completed allowing a smooth flow of the design from initial concept and system specification in VHDL to actual hardware implementation.
More work still needs to be done. For instance... While asynchronous logic, by gating clock lines to registers is easily described in VHDL, the current generation of synthesis tool cannot cope.
In spite of this, it is clear is that the combjnation of VHDL and synthesis is an excellent means of boosting both engineering productivity and quality of output. Much like the soap powder advertisements on television, all those engineers who have changed to VHDL based design are adamant they will not go back.


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# Plotting the next 

Now that GPS is within reach of almost every seafarer who wants it - prices continue to fall and now start at well under $£ 500$ - the next stage is to get it to do more than simply tell you where on earth, or sea, you are. "The emphasis has moved on from GPS to charting systems - providing something to do with all the numbers GPS gives you," says one product innovator.
The result was a crop of new plotting devices for this year's Boat Show including a stylish handheld model from Raytheon, which looked distinctly Segainspired. Plotters display a chart on a screen. and can be used for setting courses, monitoring progress and position fixing. These charts can be used for all the navigational chores that used to be done by hand, with parallel rules on paper charts, or by standing on deck, taking
bearings with a hand-held compass. The charts can be zoomed in for harbour entrances, or out for passage planning, and, of course, they can be interfaced with GPS.
Ploters for yachts are not so new: there were a few at last year's show. So far they have used one of two mapping systems -C-Map or Navionics. Charts are available in the form of mini-cartridges. In the case of Navionics, they are now based on a seamless world database, achieved by means of a numerical algorithm which converts all the individual component charts to a $1: 1$ scale at latitude zero (and therefore with zero deformation). The claimed advantages over the old chart-by-chart method include constant scale, the elimination of duplication on chart overlap, and simplification of updates.
However both these systems - although useful - are disadvantaged by their use of
raster scanning - building up the image in dots, akin to a newspaper picture. This not only produces rather rudimentary charts with limited detail, but makes them slow to draw and is heavy on memory.
They are now being challenged by a new, PC-based system which uses line-following software to create layered, vectored charts. These redraw themseives for each zoom level, and appear on-screen with the same colour and detail as the paper hydrographic charts on which they are based. Produced by Livechart in Romsey, Hants, using application software developed by Euronav at Port Solent, Portsmouth, they are already being marketed by Brookes \& Gatehouse (as Smartchart) and by ICS (as Sea-Pro).
The layered charts allow the navigator to click-off layers of information to highlight a particular buoyed channel for instance, or to zoom right in to a detailed street map of a


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## move

seaboard town. Updating is a straightforward, and for the customer, lowcost, operation.
In addition Livechart is building up a database of pilot-book information - strip views of coasts, photos of particular buoys which may be incorporated onto the disk. Other advantages include the graphic display of tidal information, and incorporation of tidal effects into passage plans. As well as all the usual interfaces


Digitised vector graphics map of the Solent from Livechart: since the database stores cartographic detail as vector mapped objects, the system stores - and can display - at the same detail as the original paper maps from which the information was taken (above). Zooming is illustrated immediate left, together with additional navigational data.
(pull-down windows can display instrument data on-screen) the charts can also import weather information by fax.
The superiority - in terms of convenience and information management - of electronic plotters over paper charts is offset by the reliability of the paper charts, which cannot crash or be rendered inoperable by power loss. Plotter systems all carry health warnings advising users not to rely on them as the primary source of navigation, but only as "a back-up to official government paper charts and traditional navigational methods." The yachting fraternity is already debating whether yachtmaster navigation classes ought to be teaching use of electronic instrumentation as a primary skill, with traditional techniques as a back-up.
However, Livechart has already done something that would have been impossible in the era of paper. When the British yacht Dolphin \& Youth lost its rudder during the second leg of the Whitbread Round the World Race, it decided to put into the South Atlantic Kerguelen Islands for repairs. Not having a detailed chart of the difficult, rockstrewn approaches onboard, they contacted the race office, which spoke to Livechart. Within 30 hours, the company had produced a digital chart ready to be transmitted via Inmarsat to $D \& Y$ 's navigational computer. ■

Peter Willis

Chartmate LCD GPS plotter from Magellan uses C-Map charts, although it can function as GPS navigator without. Its price is $£ 1195$.

## Smith charts add the dimensions needed to bring together the complex interrelated parameters of rf circuits on one plot. lan Hickman tell how to read, use and compile them.

Fig. 1. Series and parallel versions of the same lossy capacitive impedance (a) plotted on real and imaginary axes. Note that a particular radian frequency $\omega$ is assumed. In (b) is an impedance and its corresponding admittance plotted on the same real and imaginary axes. In (a) or (b) is there no simple construction which will derive the one from the other. Also shown in the diagrams are lines indicating loci of constant resistance, and of constant reactance.
n rf circuits, achieving optimum performance usually depends upon obtaining a good match between the source and load. One of these is often a resistive impedance of $50 \Omega$ - ignoring for the moment those cases where a mismatch is deliberately arranged to achieve stability in an amplifier circuit.
For example, the input circuit of an IC designed for rf applications may present an impedance looking like a lossy capacitance. A network of two or more reactances may be used to bring it to a $50 \Omega$ resistive impedance - at least at the desired operating frequency and possibly over a rather wider bandwidth. Occasionally, one reactance will suffice.
Numerous articles covering the design of L and more complicated networks have appeared over the years. The necessary calculations can often be made by expressing an impedance in terms of a series resistance and reactance, or as a parallel combination of conductance and susceptance. Converting from one
to the other is straightforward, if cumbersome, as explained in the panel.
Also involved is the addition of impedances or admittances. This is easy if they are in $R+\mathrm{j} X$ (resistance and reactance in series) or $G+\mathrm{j} B$ (conductance and susceptance in parallel) form, as in Fig. 6 of reference 1. If they are in magnitude and phase form $M / \Phi$, Fig. 8 (ibid.) shows how they may be added graphically.
However, Fig. 1 shows that linear real and imaginary axes, as used in the reference, do not provide a simple way of converting series resistance and reactance to the parallel form. Nor do they make it simple to convert it to $G+\mathrm{j} B$ form. Further, really large values of $R$ or $X$ cannot be shown, as infinite values of these are off the page infinitely far to the east, north or south.
There is a mathematical transformation of axes that solves both of these problems. It also turns out to have



Fig. 2. Resistive axis is modified in (a) to show all values from zero to infinity.
In (b), all points representing infinity off the page to top and bottom, and on the constant resistance line at $R$ is infinity - have been condensed into a unique infinity point on the right. In the lefthand chart, constant resistance lines have become circles while on the right, constant reactance lines have become arcs.
Chart (c) shows how simply series impedance values are converted to parallel admittance values, compared with the calculations shown in the panel. Significance of the dotted circle concentric with the centre of the chart is covered later in the text. Adding series inductance or shunt capacitance (d) moves the resulting complex impedance or admittance clockwise around a constant resistance
(conductance) line while series capacitance of shunt inductance moves it anticlockwise.
other extremely useful features. To bring the point representing infinite resistance onto the page, start by plotting values of resistance from zero to $1 \Omega$ on a base which becomes more compressed as it nears unity.

Now for values greater than unity, plot the reciprocal of resistance to the same scale, so that infinity comes as far to the right of the point $I$ as zero is to the left, Fig. 2a. Next, gather up the tops and bottoms of the constant resistance lines, at infinity. Bend them round to the right so that they become circles terminating at the point representing infinity now unique - at the right hand end of the diagram, Fig. 2b.
In the process, the constant reactance lines have become arcs as shown. This is in fact a 'Smith chart'. The constant resistance lines form an orthogonal set with the constant reactance lines. Each line of the one sort crosses every line of the other sort at right angles.
Constant resistance circles all have their centres on the horizontal diameter of the diagram. On the other hand, the constant reactance, or susceptance, lines are all arcs of circles with their centres on a vertical line running from minus to plus infinity through the right hand end of the diagram's horizontal diameter.

This chart serves two purposes. It can represent zero resistance at the left of the horizontal diameter up to infinite resistance at the right. It can also show purely inductive reactance increasing from zero to infinity clockwise around its upper rim and capacitive

reactance and likewise anticlockwise around its lower. But equally, the horizontal diameter can represent zero conductance, at the left hand end, up to infinite conductance at the right. Zero conductance and infinite conductance represent open circuit and short circuit respectively.
The upper arc now becomes capacitive susceptance from zero to infinite clockwise and the lower arc zero to infinite inductive susceptance anticlockwise. At this point a very simple construction takes one from a series value ( $R+\mathrm{j} X$ ) of impedance to the corresponding parallel ( $G+\mathrm{j} B$ ) admittance.
Imagine any point on the chart, point A in Fig. 2c, representing an impedance $(R+\mathrm{j} X) \Omega$. The point at the same distance from the centre and diametrically opposite gives the corresponding value of $(G+\mathrm{j} B) \mathrm{S}$. Note that siemens, which has replaced mhos as a unit, is represented by a capital $S$ since lower case $s$ indicates the SI unit of time, the second.
In addition to providing a simple graphical conversion from series impedances to shunt admittances, the chart also provides a simple graphical means of finding the result of adding a series reactive component to an impedance. This is shown in the lower half of Fig. 2d. The series reactive component can be inductive or capacitive, i.e. positive or negative.

## Resistance or conductance?

Moving round the circle in this way is the same as moving up or down a constant resistance line in Fig. 1. Adding more and more inductance would eventually take you right round through the top half of the chart, to the point of infinite reactance at the right hand end
of the horizontal diameter. Similarly, adding a parallel susceptance to the starting admittance shown in the upper half of Fig. 2d moves its effective value around the constant conductance circle $G$, which is 0.5 .
Two points are very important when using the Smith chart. The first is that you will either be using series components expressed in ohms or parallel components expressed in siemens. Parallel vàlues in ohms such as those shown in Fig. 1(a), or series values in siemens, are not used. As a result, an impedance Z 1 , which is $\mathrm{R} 1+\mathrm{j} \mathrm{X} 1$, in series with Z 2 results in $\mathrm{Ztot}=(\mathrm{R} 1+\mathrm{R} 2)+\mathrm{j}(\mathrm{X} 1+\mathrm{X} 2)$. An inductor with a $Q$ of 20 at a particular frequency at $10+j 200$, in series with $90-\mathrm{j} 90$, a capacitor so lossy that tand is 1 , gives Ztot $=(100+\mathrm{j} 110) \Omega$. This is characteristic of a very lossy inductor or maybe a wire-wound resistor.
Likewise an admittance $Y_{1}$, which is $\left(G_{1}+\mathrm{j} B_{1}\right)$ in parallel with $Y_{2}$ gives a resultant
$Y_{\text {tot }}=\left(G_{1}+G_{2}\right)+\mathrm{j}\left(B_{1}+B_{2}\right)$. For example, a capacitive admittance $0.01+\mathrm{j} 0.1$ in parallel with an inductive $0.01-\mathrm{j} 0.1$ gives $(0.02+j 0.0) \mathrm{S}$. This provides an excellent match in a $50 \Omega$ system at one frequency, and a good match near the centre frequency since $Q$ is only 5 .

Working out the parallel combination of $Z_{1}$ and $Z_{2}$ above is untidy. It is much easier to convert them to $Y_{1}$ and $Y_{2}$ first. Secondly, that the chart is drawn in terms of normalised impedances/admittances. This means that the impedance you may want to match, say the input of an amplifier, is assumed to be $1 \Omega$.

Having found the required normalised values of the components of the matching network, they are converted to those for, say, a $50 \Omega$ system. This is done by multiplying all inductive and capacitive

## Converting impedance to parallel admittance

Conversion of a series resistance plus reactance circuit into the equivalent parallel components and vice versa is shown in the diagram. It summarizes the results of some fairly straightforward algebra. Converting from parallel impedances to parallel admittances is simple since the real parts of these - the conductances - add directly, as do the imaginary or susceptance parts. In-phase and reactive parts $G_{p}$ and $B_{p}$ of the parallel admittance $Y_{p}=G_{p}+B_{p}$ are given by

$$
G_{p}=1 / R_{p} \text { and } B_{p}=1 / X_{p} .
$$

As a result,

$$
G_{\mathrm{p}}=R_{\mathrm{s}} /\left(R_{\mathrm{s}}^{2}+X_{\mathrm{s}}^{2}\right) \text { and } B_{\mathrm{p}}=X_{\mathrm{s}} /\left(R_{\mathrm{s}}^{2}+X_{\mathrm{s}}^{2}\right) .
$$

Similarly, turning the algebra around,

$$
R_{\mathrm{s}}=G_{\mathrm{p}} /\left(G_{\mathrm{p}}^{2}+B_{\mathrm{p}}^{2}\right) \text { and } X_{\mathrm{s}}=B_{\mathrm{p}} /\left(G_{\mathrm{p}}^{2}+B_{\mathrm{p}}^{2}\right) \text {. }
$$

Both sets of formulae have exactly the same form but with $R$ and $G$ changing places, and $X$ and $B$ doing likewise.

Parallel resistance and reactance equivalent to a given series resistance-reactance combination, and vice versa.


For equivalence, $M_{s}=M_{p}$ and $\phi_{s}=\phi_{p}$

Serial to parallel,
$R_{p}=\frac{R_{s}^{2}+X_{s}^{2}}{R_{s}} \quad X_{p}=\frac{R_{s}^{2}+X_{s}^{2}}{X_{s}}$

Parallel to serial,
$R_{s}=\frac{R_{p} X_{p}^{2}}{R_{p}^{2}+X_{p}^{2}}, \quad X_{s}=\frac{R_{p}^{2} X_{p}}{R_{p}^{2}+X_{p}^{2}}$,
reactances by 50 and dividing all the susceptances by 50 , or by 75 in the case of a $75 \Omega$ system.
Knowing the reactance or susceptance of each component, then given the desired operating frequency, the actual combined value is defined.
As an example of the Smith chart in action, imagine matching the input of an IC. At the desired operating frequency, the input looks like a normalised admittance of $(0.71+\mathrm{j} 1.72) \mathrm{S}$. In a $50 \Omega$, system this corresponds to a resistive component of $1 / 0.71 \times 50=70.4 \Omega$ in parallel with a capacitive reactance of $29.1 \Omega$. In the normalised admittance, the capacitive term has a $+j$ sign as it is a susceptance, the reciprocal of a capacitive reactance.
Adding a shunt inductive susceptance of -j 1.72 is the simplest course. The value can be read off round the edge of the chart where the constant reactance (susceptance) lines are labelled. This would resonate out the capacitance, moving the point A in Fig. 3 anticlockwise round the line of constant conductance to the point 0.71 on the horizontal axis.
But a pure resistance of $70.4 \Omega$, while an improvement, is not a perfect match to a $50 \Omega$ source. You need to modify the effective resistive component as well as removing any residual reactive component. This can be done in two stages. First add the inductance as before, but this time series inductance. To do this, first convert the starting parallel admittance point A to the series impedance form, point $B$, as described earlier. Series inductance can now be added to bring us to point C .
The trick is to choose a point C diametrically opposite to point D on the constant conductance line $G=1$. It should also be the same distance from the centre of the chart. Point $D$ represents exactly the same admittance as $C$ but the latter expresses it in series impedance terms. Value of inductance needed is represented by the length of the arc BC . Values at B and $C$, read off from the edge of the chart, are -j 0.5 and +j 0.43 respectively. As a result, a normalised series inductive reactance of $0.93 \Omega$ is required.
Expressed as a parallel circuit, the input of the IC plus the series inductance looks like the admittance at point D. Adding the shunt capacitive susceptance indicated by the arc from D to the centre of the diagram, in this case +j 2.0 , completes the process of matching.
The clever part is locating point C and hence D . Lay a graduated straight edge, preferably transparent, across the diagram, passing through the centre. Now swivel it round until the distance from the centre of the diagram to the intercept on the constant resistance line which passes through $B$, is equal to that on the constant resistance line passing through the centre of the diagram. Note that as one intercept increases, the other decreases.
Now repeat the exercise starting with point $\mathrm{A}^{\prime}$ at ( $0.4-\mathrm{j} 0.8$ ) S, representing an inductive input admittance looking like $125 \Omega$ in parallel with an inductive reactance of $62.5 \Omega$. You will find that from point $B^{\prime}$ it is necessary to proceed anticlockwise adding series capacitance to arrive at a point $\mathrm{C}^{\prime}$. This point is diametrically opposite a point $\mathrm{D}^{\prime}$ on the unity conductance circle and equidistant from the centre of the chart.
Adding shunt capacitance as before, but rather less of it this time, brings the point to the centre of the diagram, the point of normalised impedance or admittance $1+j 0$. Where the first example required a matching network of series $L$ and shunt $C$, this one

needed two capacitors. Starting with other admittances could require series $C$ and shunt $L$ or even two inductors.

## Transmission line matching

This explanation of the construction and use of the Smith chart has been based on the assumption that the circuitry in question operates at a frequency where lumped components - capacitors and inductors - are appropriate. Such circuits extend up to vhf and low uhf. At much higher frequencies, the values of lumped components may be inconveniently small, so it may be preferable to use lengths of transmission lines instead.
A transmission line less than $\lambda / 4$ in length at the frequency of operation, and with its far end open circuit, looks like a capacitance, or an inductance if the end is short-circuited ${ }^{2}$. Capacitive susceptance of the open circuit line varies from zero when its length $l$ is zero, up to infinity when / is $\lambda / 4$. Inductive reactance of the short circuit line varies in just the same way.
On such a line of length $\lambda / 4$ or more, the voltage standing wave ratio - the ratio of the maximum voltage on the line to the minimum - is infinity. This applies for any other purely reactive termination. On the other hand, on a line resistively terminated with the line's characteristic impedance $Z_{0}$, the vswr is unity.
If the shunt resistive component of the termination is not equal to $Z_{0}$, or if there is also a reactive component, then there will be some energy reflected from the end of the line. This reflection appears as a wave front travelling back towards the source. Thus voltage on the line will vary with distance from the

Fig. 3. Using the Smith chart to match a load to the source via lumped components.
The object of the excercise is to get from the starting point of the graph (the combination of intial resistance and reactance) back to the centre for perfect matching. The dotted lines represent a conversion from parallel to series components while the solid arcs represent the addition of real reactances in either serial or parallel form to achieve matching.

b

Fig. 4. Radial lines on a Smith chart match a load to its source using transmission lines.
Once again the points on the graph represent specific combinations of resistance or reactance (serial) or their inverse for parallel components. The difference with Fig. 3 is that the angular path between points - a change in reactance within the
circuit - can be effected by the addition or subtraction of bits of transmission line. The required length can be read directly from the periphery of the graph.
termination. For example if the voltage of the reflected wave front is $10 \%$ of the incident, the voltage will vary between 1.1 where the incident and reflected voltage are in phase to 0.9 where they are in antiphase. Resulting vswr is $1.1 / 0.9$ to unity or $1.222: 1$.

Variation of reactance along a short circuited line, moving away from the shorted end towards the source, can be plotted clockwise around the edge of the Smith chart.

Starting point of the plot is zero (short circuit) at the left hand end of the horizontal diameter. It passes through $X_{0}$, which is an inductive reactance numerically equal in ohms to $Z_{o}$, at the top of the chart. From there it travels to infinity (open) at the right hand end, which corresponds to a distance $\lambda / 4$ along the line. Now it passes again through a capacitive reactance equal to $Z_{0}$ to a capacitive short circuit back at the starting point. This point is at a distance $\lambda / 2$ along the line.

The outer edge of the chart is thus a circle of constant vswr, namely infinity:1. Smaller circles, concentric with the centre of the chart, represent lower vswrs, right down to unity at the centre. Impedance seen looking into a line at an increasing distance from an arbitrary finite termination other than $Z_{0}$ is given by following clockwise round a circle of constant vswr passing through the point representing the termination.
Armed with these results, plus the earlier ones concerning the addition of series and shunt components, the matching of a load to the source using lines is straightforward.

Figure 4 shows a Smith chart with a load comprising resistance and capacitance in parallel. This load is in normalised form of $(0.2+j 0.4) S$ marked in at point A .

Moving a distance of $(0.187-0.062) \lambda=0.125 \lambda$ towards the source brings you to the point B. Here the admittance consists of a conductance 1.0 in parallel with a susceptance +j 2.0 . Continuing around the chart - forwards or backwards - on a constant vswr circle to point C shows that without matching, the vswr on the line would be $1 / 0.175=5.7: 1$
Remembering that shunt admittances add directly, adding a susceptance of -j 2.0 across the line at a point $0.125 \lambda$ from the load will cancel out the susceptance of +j 2.0 at B. In fact the inductive shunt susceptance of -j 2.0 parallel-resonates with the +j 2.0 capacitive susceptance. Viewed from the source, point B is moved around the constant conductance line to point F , representing a perfect match.
Shunt susceptance at -j2.0 can be a 'stub', a short circuit length of transmission line. Point $E$ represents -j 2.0 susceptance while the required length of line, starting from the short circuit (infinite inductive susceptance) at $D$, is ( $0.32-0.25) \lambda=0.07 \lambda$. Thus connecting a short circuit stub of length $0.07 \lambda$ in parallel with the main line at a distance $0.125 \lambda$ from the load completes the process of matching.
This example of matching using lengths of transmission lines ignores the effects of any losses in the lines. In practice this is permissible as the lengths involved are so small. When working with coaxial lines, a short circuit stub is usually preferred to an open circuit. It is more 'ideal', reflecting all of the incident power. An open circuit can radiate a little of it , the more so the higher the frequency, resulting in a finite rather than a zero return loss. In microstrip and stripline however, open circuit stubs can readily be employed.
Various other parameters around the edge of the chart are also shown in the Smith chart of Fig. 4. In addition it shows the labels for the constant reactance/susceptance arcs, and the distance in wavelengths along the line. These additional items are the angle of the reflection coefficient, and attenuation. The latter is shown on an arbitrary scale of 10 dB per half wavelength. If for example on an actual line, attenuation is known to be $0.1 \mathrm{~dB} /$ wavelength. Attenuation read off from the chart for a given length of line should be divided by the figure $10 / 0.05=200$.

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## Further reading

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## Acknowledgments

Several of the illustrations in this article are reproduced by courtesy of GEC Plessey Semiconductors, from the application note The care and feeding of High Speed Dividers, which appears in their Personal communications IC handbook, Publication No. PS21 23, June 1990. Note - this application note does not appear in the later version of the handbook, HB2123-2, dated May 1992

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| Chelmar Value | 233 | Pico Technology Ltd | 206 |
| Dataman Programmers Ltd | OBC | Powerware | 183 |
| Display Electronics Ltd | 214 | Ralfe Electronics | 264 |
| Electrovalue Ltd | 233 | Research Communications | 183 |
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## The Package

S4 comes fully charged and contigured for immediate use. You get a mains charger, emulation lead, write lead, personal organiser instruction manual, MS-DOS communications software and a spare Library ROM. Optional modules available for Serial EEPROMS, 40 -pin EPROMS, 8751 's and PIC's.

## Availability

S4 is always in stock. Phone through your credit card details to ensure next working day delivery. Full 30 day no-risk refund.


Credit card hotline: 0300320719 for same-day dispatch


[^0]:    One stop design: this screen shot of the VSS VHDL simulator from synopsys shows a block level functional schematic, a listing of the the VHDL source code and a view of the VHDL code debugger.

