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• Optimise valve o/p transformers

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A new technology for detecting concealed weapons doesn't rely on X rays. In fact it's completely passive. To find out more, turn to page 5.

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An exercise in real-time programming – Tim Wilmshurst demonstrates how to produce time-critical systems using this microcontroller-based multitasking metronome.Turn to page 54.



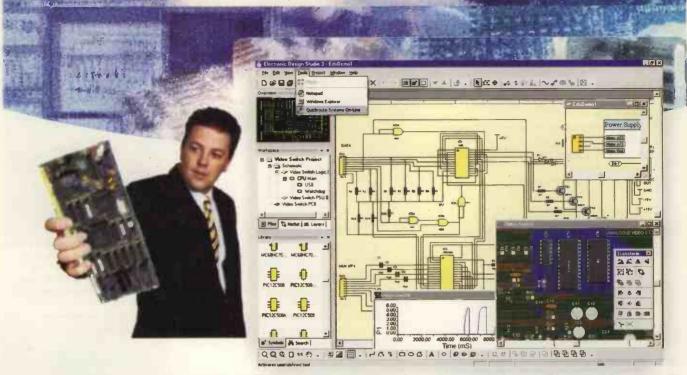
Locate your current position using lan Hickman's direction finder,. It works by seeking out VHF transmitters – turn to page 62.



Class-D audio amplifier evaluation kits – less-than 0.05% closed-loop distortion and 50W continuous. Find out more about this and lots more exciting new products, starting on page 39.

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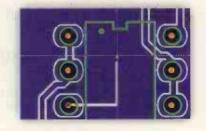
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Misguided meddling

he UK government has restated its goal of giving access to the Internet to everyone who wants it by 2005. Great news for Great Britain. Or is it?

In the electronics community there'll clearly be some beneficiaries. Some £200 million is to be invested in a network of 6000 UK online centres in communities across the country. Firms that import PCs or assemble them from imported components will do nice business, while British Telecom and other telcos will undoubtedly get a look-in on the gravy train.

Beyond this though, what benefit will this bring the British electronics industry? Will it support innovative research and development? Will there be allowances for start-ups? Will it help British firms to win government contracts?

No, no and no. According to e-commerce minister Douglas Alexander, people will be able to surf the Internet at these centres and get advice and training while doing so. The report doesn't mention free coffee and chocolate biscuits, but no doubt these are on the menu as well.

The government considers this is the best means of enabling all UK citizens to benefit from the web and thus "bridge the digital divide" by extending access.

"Few would question seriously that in the global economy access to information is unevenly distributed," he declares and then delivers the remarkable revelation that although the Internet now reaches one in three households, only seven per cent of citizens in the poorest income group, for example, have home access, compared to 71% in the highest group.

One suspects the figures for private health insurance or ownership of high-end audiophile systems are similar but one sees no government intervention to rectify inequality in these quarters.

Yet the government is committed to providing low-income families with low cost, recycled PCs and pilot initiatives to wire up all of the homes in some of the poorer communities in the country. It is connecting all public libraries as well, which it claims as the biggest single investment in the UK libraries network since the middle of the 19th century – too bad there's no budget for books.

It justifies this intervention by the argument that governments have a vital role to play in the modern economy, balancing the countless private choices of individuals and companies with public choices that society has to make. "Extending opportunities makes both social and economic sense, creating a fairer and more prosperous Britain."

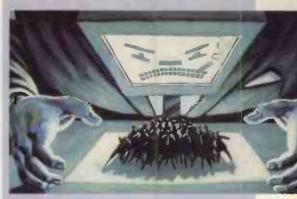
This makes interesting rhetoric, but the logic that reallocating resources for a fairer marketplace will create greater prosperity is debatable. HMG has failed singularly to hasten the onset of broadband communications nor has it achieved the hotbed of ebusiness that the government stated it would.

What this move crucially fails to recognise is that Internet access is purely a means to an end – not an end in itself. It is a communications medium, no different from the telephone, newspapers or television. People having an application for

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"...Extending [Internet] opportunities makes both social and economic sense, creating a fairer and more prosperous Britain." This makes interesting rhetoric, but...

communication of this kind can doubtless make excellent use of it. But it's debatable whether offering cut-price Internet access to the severely disadvantaged will transform their situation.

For some beneficiaries this endowment may be entirely inappropriate – and as welcome as the complete works of Shakespeare or a boxed set of two dozen classical CDs. Handing out top-flight fountain pens will not improve people's handwriting any more than giving them painting sets will turn them into eminent artists. Without also grounding in numeracy, literacy, economics and technology, these marginalised citizens will be no further advanced towards creating more wealth for the nation. In short, what they need is not hand-outs but a structured approach to building up their knowledge, understanding and skills.

Says Alexander: "Appropriate government action will not only strengthen social cohesion but also strengthen economic competitiveness. The challenge is how best to assist our communities and equip our companies in the face of these challenges."

Quite right. But the way ahead is to educate people systematically to a level where they can create wealth, at the same time creating an environment that favours greater investment in people by employers. Handing out free computers and modems is a scatter-shot tactic and will not achieve this.

The results of proactive investment policies will not be seen overnight; it will take time to devise training schemes and even longer to argue how they should be funded and organised. Yet this is precisely where government intervention would be benign, to encourage professional competence and create a climate that truly rewarded commitment to training employees instead of abetting the poaching of skilled staff from the firms that trained them.

The government states it is committed to helping people acquire the skills they need for the jobs of the future. Let's see if it can also create an environment that'll sustain those jobs. To leave that task to market forces while intervening in online access is no less than double standards.

Mark Nelson

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UPDATE

New camera detects concealed weapons without using X-rays

Researchers at Qinetiq, the UK's defence research group, have developed a millimetre-wave camera that can spot concealed weapons and find stowaways hidden in trucks.

The human body reflects some 50 per cent of incident radiation at 35 and 94GHz, a fact that the camera exploits.

"The camera doesn't transmit anything – it's purely passive," said Roger Appleby, team leader for passive mm-wave imaging at QinetiQ.

Contrast is generated by the sky temperature, which is about 200K colder than ground or other objects. This makes the camera a radiometer, measuring thermal noise and amplifying it to produce a voltage.

"Anything that reflects that cold sky gives a huge contrast," said Appleby.

QinetiQ is reluctant to give out resolution figures, but says the camera works at a range of a few metres, and runs at around 12 frames/s.

Originally intended for soldiers and pilots to use in thick fog, the mmwave camera has been tested finding stowaways on lorries passing through Eurotunnel's French terminus.

"When illegal immigration became such a political hot potato and the Government introduced £2000 fines for travel operators, we agreed to work with Eurotunnel to assess the millimetre-wave camera," said Kevin Murphy, a business manager at QinetiQ.

"In just three months we saved Eurotunnel tens of thousands of pounds in fines."

The camera works through the sides of lorries when visual inspections and CO_2 sensors are impractical, and lorries don't need to stop as they pass the camera.

Because clothing is transparent to the system, the camera could also be used in security applications, searching out dense objects such as knives and guns.



LEDs five times more efficient than common bulbs

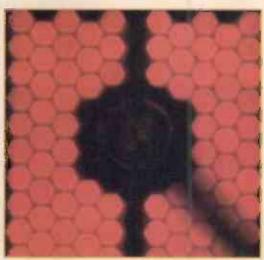
50 lumens per watt – that is five times the efficiency of a conventional light bulb – is now available from LEDs. The claim comes from Osram which has doubled the light output of the best 615nm (reddish-orange) LEDs. The technique is said to work from yellowish-green to red.

LEDs are formed in epitaxial layers grown on various substrates, normally gallium arsenide at these longer wavelengths. According to the company, the GaAs substrate absorbs, and therefore wastes, light.

To counter this, Osram is turning the LED structure on its head and then removing the GaAs completely.

Initially it metal-coats the epitaxial layer after normal LED construction, then bonds another wafer on top. This second wafer then acts as a new substrate while the original is removed. Now it has the epitaxial layer bonded upside down to the new substrate with a metal layer in between. The metal acts as light reflector and back contact.

From the beginning, said Osram, the process has been designed for 100mm LED production wafers.



New LEDs have five times the efficiency of a conventional light bulb.

World's first

gallium nitride

wafer. GaN is

likely to lead to

better blue and

Fingerprint

sensors have a

fingers. Tens of

micromachined

push buttons look

set to provide the

answer to this

thousands of

problem with wet

UV LEDs.

World's first gallium-nitride wafer

A US firm claims to have made the world's first pure gallium nitride (GaN) wafers.

Technologies and Devices International (TDI) said production of such wafers could lead to improved green, blue and ultraviolet LEDs.

GaN is the only mainstream semiconductor substrate not available in pure wafer form. Today GaN devices are made on epitaxial lavers. grown on substrates of silicon carbide or sapphire (Al₂O₃). A pure GaN wafer would increase the thickness of the GaN layer well beyond the few

microns that is typical today.

This bulk GaN, rather than epitaxial GaN, will increase performance and lifetime of devices, the firm said.

"Within one year TDI's bulk GaN could be the basis of next generation commercial blue-spectrum high brightness light emitting diodes and blue-spectrum semiconductor lasers," said Vladimir Dmitriev, chief executive of TDI. The company is looking

Most powerful blue LEDs

LED manufacturer Cree has increased the power output of its blue semiconductor devices to 18mW, around 50 per cent higher than current production diodes.

As with the firm's existing devices, X-Bright LEDs will use a silicon carbide wafer, topped with indium gallium nitride (InGaN).

Devices are expected to include ultraviolet at 395 and 405nm, a 460nm deep blue, and 470nm blue LEDs All Cree's LEDs have a vertical

structure with a metallised base for

for partners to move to volume

characterisation by Arizona State

According to the firm, an external

University concluded the wafers have

"fairly high crystal quality with low

TDI's wafers are 35mm in diameter.

slightly smaller than the 50mm available from GaN on SiC or

production of the wafers.

dislocation density"

sapphire.

the cathode and a single gold bond pad on the top of the device for the anode connection. Light exits around the bond pad.

Existing devices measure 300×300µm and have a 30mA forward current at around 3.6V.

Cree sells its LEDs as cut dice from the wafer. Typical applications would be as the basis for white LEDs, traffic lights and other solid-state illumination.

Fingerprint sensor deals with clammy hands

Most fingerprint sensor chips use capacitive sensing and fail to work with wet fingers. Mechanically sensing the ridges and grooves on a finger tip entirely gets over this problem. But how do can you do it?

NTT thinks it has the answer and has micromachined an array of 60000 push buttons.

Each pixel, as NTT calls the push buttons, is 50µm square and consists of a membrane over a hollow chamber.

A 10µm high polyamide bump on top of the membrane bends the membrane into the chamber when touched. This decreases the spacing of two electrodes, one at the bottom of the chamber and one under the membrane. The spacing change is detected by capacitive means isolated from any moisture, grease or dirt on the finger tip.

The chamber is built from electroplated gold, using polyamide as a sacrificial material in the micromachining process.

The membrane, which also seals the chamber and supports the top electrode, is applied using a specially-developed technique called 'spin coating film transfer and hotpressing' which does not allow material to flow into the cavity and clog it during manufacture.

50000 heavy taps with a simulated

problem.

finger, said NTT, failed to break the sensor.

In a separate paper, researchers from Analog Devices' Irish research labs have created a cavity-based touch sensor using floating gate technology.

This time, the cavity is entirely made from polysilicon. The poly membrane couples capacitively to another polysilicon layer on the substrate below. This second layer also acts as a floating gate for a Fet channel in the substrate below.

Displacing the membrane causes the voltage on the lower poly layer to change, as charge is constant. In turn, this alters the resistance of the channel below.

Overall, the device converts a pressure to a current in the channel.

Analog Devices says the sensor is scalable and can be made on a standard CMOS process with four extra mask steps.

NTT's fingerprint sensor

- 57 334 off 50 by 50µm pixels
- 11 by 13mm active area
- 102 transistors per pixel
- 256 step grey scale
- 300ms read time .
- 3.3V, 60mW power



Fets with carbon nanotubes look set to outperform their silicon counterparts

Fets made from carbon nanotubes have been demonstrated by scientists at IBM's TJ Watson Research Center, while simple circuits based on such devices have been made at Delft University of Technology in the Netherlands.

Such research might help solve some of the fundamental physical limitations that silicon Fets are facing.

IBM's researchers dispersed semiconducting single-walled nanotubes (s-SWNTs) with a diameter of 1.4nm onto a heavily doped silicon wafer, which acts as the gate, separated by a 150nm gate oxide.

Titanium or cobalt are used as the source/drain contact material with an anneal process to form low-resistivity Co or TiC at the junction between the contact and the nanotube. This scheme is claimed to be a big improvement over previous attempts to make nanotube Fets.

The resulting transistor has a relatively long nanotube of just over 1 μ m in length (see image). Hole mobility is around 60cm²/V/s, while transconductance for a p-type device reaches 122 μ S/ μ m.

The latter metric, scaled for a 100nm nanotube Fet, would give a transconductance of over $1200\mu S/\mu m$ – a figure that is similar to that of conventional silicon Mosfets.

However, unlike silicon Mosfets, reducing the gate oxide thickness will not give the same level of performance improvement. This is because the capacitance for a cylinder varies inversely with the logarithm of the distance to the centre of the cylinder. A standard Fet has a linear response to gate oxide thickness.

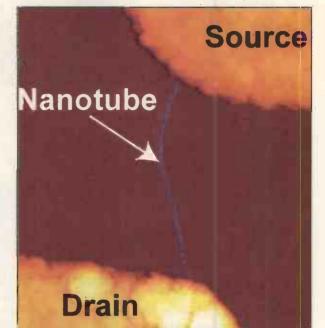
The team at Delft University have gone a step further by avoiding the use of the wafer as the gate, which limits options for multiple transistors.

The team patterned aluminium wire on the wafer, followed by oxidation to make the gate insulator. Nanotubes around 1nm wide were deposited on top of the gate. Thus each transistor has its own separately controlled gate.

Resulting devices have gain above ten and an on/off current ratio of greater than 10^5 .

The team then constructed simple

circuits with up to three transistors, and were able to create functions such as an inverter, a NOR gate, an SRAM cell and a ring oscillator. The circuits use resistor-transistor logic, with the resistors off-chip.



DC-to-DC converters fill a gap in the market

International Rectifier claims to be successfully exploiting a niche between discretedevice on-board DC-to-DC converters and power 'brick' types.

Earlier this year, the company introduced the iP2001 - a power hybrid containing all of the semiconductors required for a multiphase microcontroller power supply, but leaving out the inductors and large capacitors.

This put it between lower cost all-discrete implementations and 'no-brainer', but costly, power bricks.

According to company product marketing engineer Carl Smith, the iP2001 has already won a design-in with a customer.

IR has now followed up with the iP1001, a similar building block for telecom network infrastructure.

The iP1001 includes all semiconductors needed to make a 20A non-isolated DC-to-DC converter with an output between 0.925 and 3.3V. All the designer has to do, said Smith, is add input and output capacitors and an inductor.

Output voltage is set by an internal D-to-A converter whose inputs can be hardwired or manipulated on-the-fly.

Input range is 2.5 to 12V, providing the input voltage is greater than the required output as this is a buck converter.

The converter requires a 4.5 to 5.5V auxiliary voltage supply which must be separately generated if it is not available on-board: a reference design is available. Overall efficiency can be as high as 97 per cent $(3.3V_{in}, 2.5V_{out} \text{ at 4A})$, and stays around 90 per cent for most line-load combinations.

There is no internal thermal protection, but, said Smith, a step-by-step thermal design guide is available which should guarantee no thermal problems.

> Sitting between brick-type DC-to-DC converters and onboard discretecomponent alternatives, the iP1001 only needs capacitors and an inductor to deliver 20A output.

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Cheaper solar power from polymer semiconductors

Plastic semiconductors may spawn cheaper solar cells, say researchers at Belgian research organisation IMEC.

"Polymer solar cells are a long-term application that could be enormous in quantity," said professor Robert Mertens, v-p for polymer devices at IMEC.

Currently his cells are at a very early development stage. "It will be another 15 years or so before we really have the materials under control, but the pay-off is so enormous."

Solar cells are chosen on cost. According to Mertens, part of the costing comes down to efficiency. "You need an efficiency of six to eight per cent for an integrated solar roof. Efficiency below six per cent is not economical," he said.

Currently performance is too low. "We have polymer solar cells with efficiencies of two to three per cent over a few square millimetres."

Matching cell characteristic to the solar spectrum is one route to better output. The bandgaps of most plastics are too high. "IMEC is researching low bandgap materials. The optimum is 1.0 to 1.4eV – we can actually do



these now – and these could be cascaded for wider absorbency." said Mertens.

Cascaded solar cells use stacks of materials with different bandgaps to convert more solar spectrum. III-V semiconductor solar cells have been made using this technology. IMEC is working on a solar cell that uses buckyballs (C_{60}) in a p-type polymer. "The C_{60} [molecules] are in contact with each other. This makes an n-channel that collects electronhole pairs very efficiently. The cell is only a few tenths of a micron thick and pair creation occurs very close to the n-type region," said principal opto researcher professor Paul Heremans.

Alternative energy boost

Government plans to increase the use of alternative energy sources have taken another step forward with the awarding of \pounds 4m in grants for solar power projects.

The grants will pay for 380 homes throughout the UK to be fitted with photovoltaic solar panels. Each system will supply up to 1.5kW to the home.

Brian Wilson, minister for energy, said the Government is serious about

the use of renewable energy sources. "I am determined to give real meaning to all the talk about renewable energies. This £4m will result in hundreds of households being in the front line of our commitment to solar energy," said Wilson.

Over the next three years a further £100m is due to be doled out to projects covering solar, wind and wave energy generation. The next round of solar photovoltaic projects will receive a share of this plus another £10m.

"These projects will provide the right learning experience before the UK embarks on a much larger installation programme. I want to see thousands, rising to tens of thousands of roofs covered by solar panels every year over the next ten years, rivalling the large programmes in Germany and Japan," said Wilson.

STM produces MOSFET gate just 16nm long

An n-channel Mosfet with a gate length of just 16nm (0.016µm) has been fabricated by STMicroelectronics.

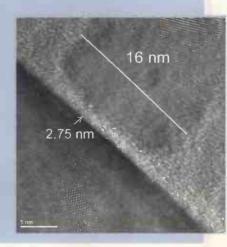
The company carried out the work to prove that Fets can continue to operate at room temperature with so narrow a gate.

One of the biggest hurdles to manufacturing such tiny gates is controlling their size, as standard lithography and even e-beam do not have the resolution.

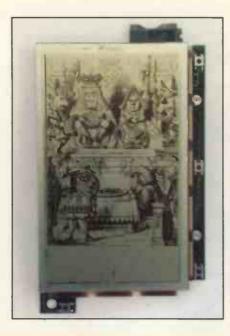
ST's researchers solved this problem by first forming the gate stack wider than required and then etching unwanted material from the sides.

The gate stack is made up from layers of 2.75nm thick oxide, 50nm of silicon germanium and 100nm of polysilicon. Lithography can make the stack down to 80nm wide, but by etching the SiGe, this is cut down to 16nm. The rest of the processing uses standard 0.13µm equipment.

At room temperature and a supply of 1.5V, the device has an I_{on} of 400 μ A/ μ m and an I_{off} of 0.8 μ A/ μ m. Performance could be improved by using a thinner gate oxide, below the existing 2.75nm.



In an attempt to prove that Fets with extremely short gate lengths will work at room temperatures, STM has produced this gate – which is just 0.016µm.



LCD holds image without power

Malvern-based ZDB Displays, recently spun out of ex-government research lab QinetiQ, has released this picture of its 18cm 200dpi technology demonstrator.

The technology is bistable, which means it holds its image without power. It can also be passively scanned at any resolution. These attributes make it suitable for portable high-resolution applications including electronic books.

"We are not really limited in resolution," said company research director Cliff Jones. "200dpi is where text starts to become as easy to read as print."

According to Jones, display

contrast is higher than conventional reflective monochrome LCDs. "Ours is pure TN when it is not being addressed – a pure twist, or hybrid aligned nematic. We chose these states for their high contrast and 360° viewing angle."

Zenithal bistable displays, from whence the company gets its name, differ from conventional 'wristwatch' types only in the alignment layer. "Our basic challenge is to persuade people that you only have to use a holographic layer as an alignment layer. We use photolithography to make this at the moment, but we are working on an embossing technique," said Jones.

Gigahertz transistors announced at IEDM

A couple of record-breaking transistors were announced at December's International Electron Devices Meeting (IEDM) in Washington, DC.

They are a 341GHz bipolar transistor from NTT Photonics Laboratory and 135GHz CMOS from Mitsubishi.

NTT's bipolar transistor is aimed at 100Gbit/s integrated circuits and has a double heterojunction structure made from InP/InGaAs. An operating current density of 800kA/cm² is one of the reasons for its startling speed.

The CMOS device uses a 70nm body-tied partiallydepleted silicon-on-insulator technology with offsetimplanted source-drain extension (SDE) and a thick cobalt salicide.

The structure was chosen to get high performance in RF, analogue and logic applications said Mitsubishi. Further improvements in logic performance are predicted from going to a dual-offset implanted SDE process.

The company sees its Si-CMOS affecting GaAs and Sibipolar RF markets.

New power IGBT is 50% more efficient

Leicestershire power chip maker Semelab has developed an insulatedgate bipolar transistor claimed to be 50 per cent more efficient than existing devices.

Called a clustered IGBT, the device has a novel cathode and gate structure, and was co-developed by the Emerging Technologies Research Centre at De Montfort University. The research team have moved away from the trench structures used in the latest production IGBT devices.

"We feel we've got a novel structure that is better than anything else," said David Klein, MD of Semelab. "In this instance we're looking for higher efficiency." The layout helps reduce switching

The layout helps reduce switching and on-state losses by between 30

and 50 per cent, Semelab said. Forward voltage drop is as low as 1.8V for 100A/cm² current density.

Development has moved from the University and into Semelab's plant. "At the moment we've got sample quantities and wafers running through the fab," said Klein. This should lead to improved process parameters and better yield, he said.

The firm hopes to be able to move to commercial production of the clustered IGBT by 2003, if not sooner.

Klein hopes to tap into a \$1bn market for IGBT devices. "There seems to be a market need for better IGBT structures," he said. Applications would include motor drives and faster high power switches.

Altera's Risc processor gets a boost

Altera has revealed details of its 80MHz Nios 2.0, an updated Nios soft-core Risc processor.

Changes to the original Nios are intended to improve the core for high-bandwidth applications such as networking, telecommunications, and mass storage, said Altera.

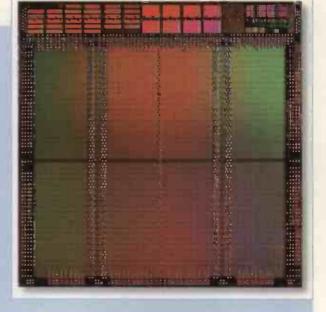
The major change is the instruction set is now customisable, with the processor core identifying non-native instructions and allowing user-designed logic to process them.

User logic is connected in parallel with the Nios ALU, picking up data

from the ALU input registers and feeding into its output buffer.

The other major change is in the arbitration scheme that handles multiple bus masters on the system bus, which connects the CPU to peripherals, programme memory and data memory.

Previously high rate access from a secondary master, perhaps an Ethernet interface, would swamp the bus. Now the CPU and the secondary master still fight for data memory access, but the CPU has unrestricted access to peripherals and programme memory.



Virtual oscilloscope combines 12-bit resolution with 100Msamples/s

PC instrumentation firm Pico Technology has developed a 12-bit module that turns a PC into a 100Msample/s oscilloscope or a 50MHz spectrum analyser.

The Cambridgeshire firm is using a 12-bit A/D converter to give the ADC212/100 a basic DC accuracy of one per cent. In spectrum analyser mode this equates to a dynamic range of 80dB, the firm said.

Input voltage ranges from plus or minus 50mV to 20V, while the device has an internal buffer memory of 128kbyte. Timebases in the oscilloscope range from 100ns per division to 50s per division.

An 100Msample/s device will cost £699, while a 50Msample/s version will cost £499, Pico said. Software is provided free of charge for data acquisition and logging.

Inductorless converters for more compact backlighting

Inductorless boost converters could cut the cost of white LED backlights says California-based chip company Semtech.

Space-saving LED backlights are becoming more popular in hand-held devices as LEDs become more efficient. Unfortunately for single cell-powered devices, white LEDs need around 4V to operate.

Inductive boost converters are available, but Semtech has developed an alternative inductorless driver chip that only needs four external 1μ F ceramic capacitors.

Called the SC600, it can deliver up to 120mA of output current from input voltages ranging from 2.85V to 6.5V – intended to match single lithium-ion cells.

Different chips in the family give preset output voltages of 4.0V, 4.5V or 5.0V accommodating the forward voltage requirements of all LED colours, but best matched to blues and whites.

The chip is output voltage rather

than current regulated, so series resistors are required with each LED. Switched-capacitor regulators tend

to suffer efficiency loss when the output voltage is not an exact multiple of the input. The SC600 includes Semtech's 'mAhXLife' technology which adds a 1.5× voltage multiplication mode to fill in the efficiency dip below exact doubling. This keeps efficiency above 70 per cent, said Semtech, peaking above 95 per cent.

The chips come in MSOP-10 packages, prices beginning at \$1.40 (1000 pieces). www.semtech.com

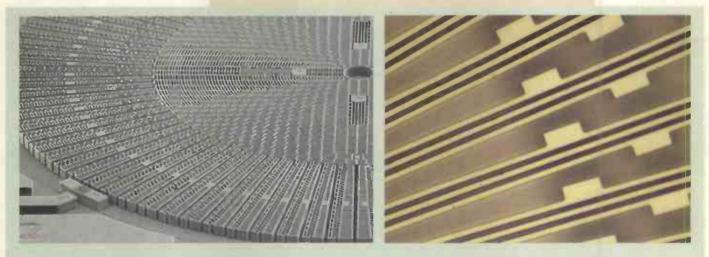
Processing power – Motorola ships five billionth HC05

Eight bit microcontrollers have always been popular, but Motorola has shipped its five billionth 68HC05 chip, part of an order for white goods maker Electrolux.

"While high-end microprocessors tend to gain the bulk of publicity, the 8-bit MCU is the workhorse of the industry," said Paul Grimme, v-p and general manager of Motorola's 8/16-bit microcontroller division.

The HC05 has a classic von Neumann architecture with its 8-bit accumulator, index register, 5-bit stack pointer and 5-bit condition code register. It is descended from Motorola's first processor, the 6800 introduced in 1974, which was designed by Chuck Peddle and Charlie Melear. The former also created the 6502 and the Commodore Pet computer.

The HC refers to the HCMOS process that allows the micro to be fully static and have a power down mode. Motorola now has over 150 versions of the HC05.



This is a prototype silicon micromachined rotational actuator for hard drive heads. The read/write head is attached to this rotor and, compared to electromagnetic actuation, says maker STMicroelectronics, electrostatic drive avoids magnetic fields close to the disk surface. Voltages applied to a stator and rotor cause angular movements of the rotor. Drive amplitude of ±10V on the actuator provides a 1µm stroke. High linearity, said ST, simplifies drive software.

A special package allows movement while keeping contamination out.

Douglas Self describes one of the lesserknown classes of audio power amplifier, showing how it is considerably more power-efficient than Class-B when handling realistic signals. Class-G has a reputation for sacrificing linearity for efficiency, but the innovative and fullyworked design presented here has lower distortion than all but the very best of Class-B.

his Class-G amplifier uses the same small-signal circuitry as the 'Blameless' Class-B power amplifier, as it is known to generate very little distortion of its own¹. If the specified supply voltages of ±50 and ±15V are used, the maximum

HASS-H

power output is about 120W into 8Ω , and the rail transition occurs at 28W.

Practical load-invariant design

Figure 1 shows the circuit of a design. The design incorporates various techniques of mine. The first technique greatly reduces time-lag in the thermal compensation.

With an emitter-follower output stage, the bias generator aims to shadow output device junction temperature rather than the heatsink temperature.

The junctions themselves are clearly inaccessible, but the next best thing is to mount the bias generator transistor Q_8 on top of the output device, rather than on the heatsink. The main heatsink mass is thus largely decoupled from the thermal compensation system, speeding up the response by two orders of magnitude².

The design closely follows the 'Blameless' Class-B amp described in references 3 and 4. Some features though are

derived from the trimodal⁵ and load-invariant⁶ amplifiers, notably the low-noise feedback network. This feedback is complete with its option of input bootstrapping if a $10k\Omega$ input impedance is required.

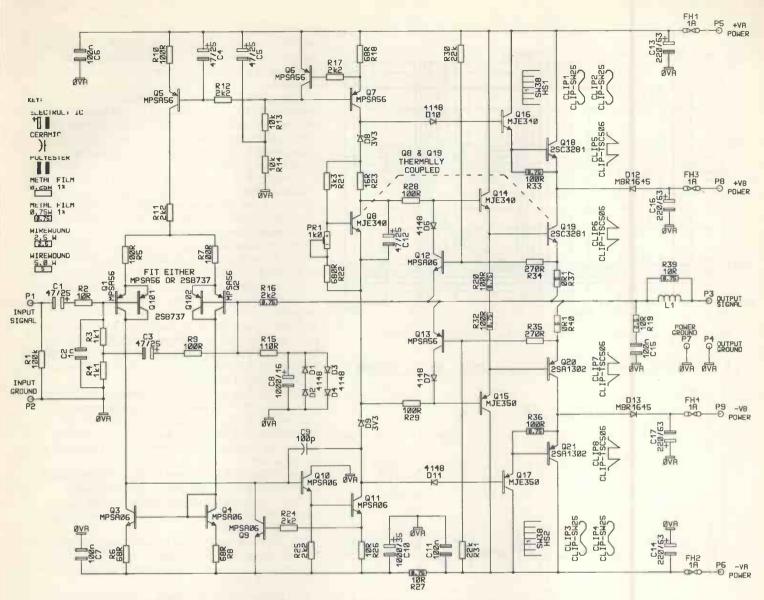
Single-slope voltage/current limiting is incorporated for overload protection; see $Q_{12,13}$. As usual in my 'Blameless' amplifiers the global negative-feedback factor is a modest 30dB at 20kHz.

The input stage – current-source Q_5 and differential pair $Q_{1,2}$ – is heavily degenerated by R_5 and R_7 to delay the onset of third-harmonic distortion. An unusually high tail current of 6mA is used to minimise the contribution of transistor internal emitter resistance variation.

Transistors $Q_{3,4}$ form a degenerated current-mirror that enforces accurate balance of Q_1 and Q_2 's collector currents. This prevents the input stage from generating secondharmonic distortion – something that should never happen.

Input resistance, defined by R_3+R_4 , and feedback resistance R_{16} are made equal. They are also made unusually low, so that base current mismatch caused by beta variations will give a minimal DC offset; this does not affect $Q_1-Q_2 V_{be}$ mismatches, which appear directly at the output, but these are much smaller than the effects of base current.

AUDIO DESIGN



Even if $Q_{1,2}$ are high-voltage types with low beta, the output offset should be within ± 50 mV, which I have found adequate. This approach eliminates balance presets and DC servos.

A low value for R_{16} means a low value for R_{15} to maintain gain. This reduction in the impedance seen by Q_2 improves noise performance. However, the low value of R_3+R_4 at $2.2k\Omega$ gives an input impedance that is inconveniently low in some applications.

What we need here is a low DC resistance, but a high AC resistance; in other words a 50H choke is needed, or alternatively recourse to some form of bootstrapping; not much doubt about the way to go there, and bootstrapping it is.

At Q_2 's base, the signal is almost exactly the same as the input. The mid-point of R_3 and R_4 is driven by C_3 , so that as far as input signals are concerned, R_3 has a high impedance.

When I first used this arrangement I had the gravest doubts about its HF stability, and added R_9 to give some isolation between the bases of Q_1 and Q_2 . In the event I had no trouble with instability, and no reports of any from the many constructors of the trimodal and load-invariant designs, both of which incorporate this option.

The presence of R_9 limits the bootstrapping factor, as the signal at R_3/R_4 junction is a little less than at Q_2 base, but it is still adequate. With R_9 at 100 Ω , the AC input resistance is raised to 13k Ω , which should be high enough.

The value of C_8 shown - 1000 μ F - gives a low-frequency

Fig. 1. Full circuit of the Class-G amplifier – probably the lowest distortion amplifier of its class.

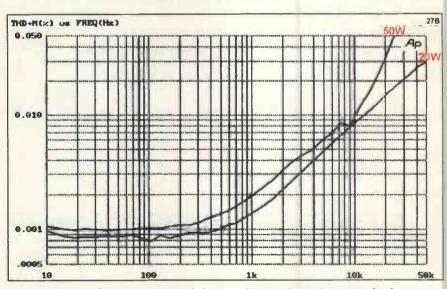


Fig. 2. THD versus frequency, at 20W (below transition) and 50W into an 8Ω load. The joggle around 8kHz is due to a cancellation of harmonics from crossover and transition. 80kHz bandwidth.

AUDIO DESIGN

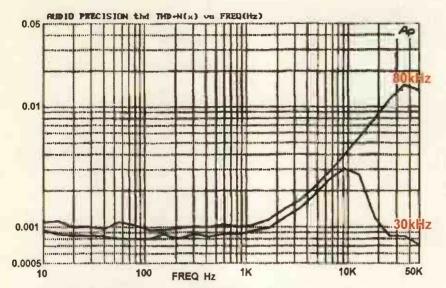


Fig. 3. THD versus frequency for a Blameless Class-B amplifier at 50W, 8Ω.

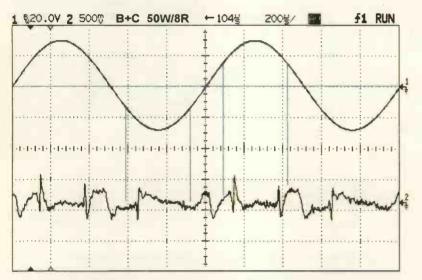


Fig. 4. THD residual waveform at 50W into 8Ω . This residual may look rough, but in fact it had to be averaged eight times to dig the glitches and crossover out of the noise; THD is only 0.0012%. The vertical lines show where transition occurs.

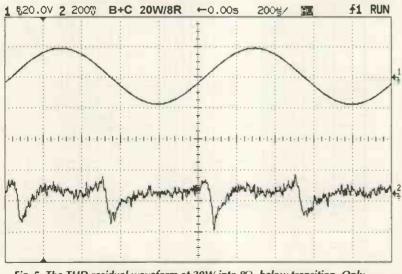


Fig. 5. The THD residual waveform at 20W into 8Ω , below transition. Only crossover artefacts are visible as there is no rail switching.

roll-off in conjunction with R_{15} that is -3dB at 1.4Hz. The purpose is not unreasonably extended sub-bass, but the avoidance of a low-frequency rise in THD due to non-linearity in C_8 .

When a 100μ F capacitor was used here, the THD at 10Hz worsened from < 0.0006% to 0.0011%, and I say this is unacceptable aesthetically – if not audibly. The place for low-frequency bandwidth definition is earlier in the signal chain, where it can be implemented with accurate non-electrolytic capacitors.

Protection diodes D_{1-4} prevent damage to C_2 if the amplifier suffers a fault that makes it saturate in either direction; it looks like a dubious place to put diodes but since they normally have no AC or DC voltage across them, no detectable distortion is generated.

The voltage-amplifier stage, Q_{11} , is enhanced by an emitter-follower Q_{10} inside the Miller-compensation loop, so that the local negative feedback that linearises the voltage amplifier is increased by augmenting the total beta.

This extra local feedback effectively eliminates voltageamplifier non-linearity. Thus increasing the voltage amplifier's beta also reduces the collector impedance. This is due to the greater local feedback. So a voltage amplifier buffer to eliminate distortion due to loading of the voltageamplifier's collector by the non-linear input impedance of the output stage is unnecessary.

The Miller capacitor, C_{dom} , that implements the dominant pole is relatively big at 100pF. It swamps the transistor internal capacitances and circuit strays, and makes the design more predictable. Slew rate calculates as 40V/µs. The voltage amplifier's collector-load, Q_7 , is a standard current source.

Since almost all the THD from a 'Blameless' amplifier is crossover, keeping the quiescent conditions optimal is essential. The bias generator has to cancel out the V_{be} variations of four junctions in series; those of two drivers and two output devices.

This task is not as difficult as it sounds. In the emitterfollower output-stage driver, dissipation is almost constant as power output varies. The problem reduces to tracking the output device junctions.

Bias generator Q_8 is a standard V_{be} -multiplier, with R_{23} chosen to minimise drift. This should be in contact with the top of one of the inner output devices, *not* the heatsink, as this is much the fastest and least attenuated route for thermal feedback.

The VAS collector circuit incorporates not only the bias generator but also zener diodes D_8 and D_9 . These diodes determine how early rail-switching occurs as the inner device emitters approach the lower voltage rails.

The output stage is an EF (emitter-follower) type as this is less prone to parasitic or local oscillations than the complementary-feedback pair version. Since this design was heading into the unknown, it seemed wise to be cautious where possible.

Resistor R_{32} is the usual shared-emitter resistor for the inner drivers. Outer drivers $Q_{16,17}$ have their own emitter resistors, $R_{33,36}$. These have the usual role of establishing a reasonable current in the drivers as they turn on, to increase their transconductance, and also speeding up turn-off of the outer output devices.

As explained in the previous article, the inner driver collectors are connected to the outer rails to minimise gainsteps caused by the abrupt change in rate-of-change of collector voltage at rail transition.

Heat sink requirements

Deciding on the size of heatsink required is not easy, because the heat dissipated by a Class-G amplifier depends very much on the rail voltages chosen and the signal

AUDIO DESIGN

statistics. A Class-B design giving $120W/8\Omega$ would need a heatsink with thermal resistance of the order of 1°C/W per channel; a good starting point for a Class- G version giving the same power would be about half the size, ie 2°C/W.

Not much heat sinking is needed for the Schottky diodes. They conduct only intermittently and have a low forward voltage drop, but it is usually convenient to mount them on the main heatsink.

Capacitor C_{15} combined with R_{38} form the Zobel network. Inductor L_1 , damped by R_{39} , isolates the amplifier from load capacitance.

Performance

Figure 2 shows the THD at 20W/50W. I think that this proves at once that the design is a practical competitor for Class-B. Compare these results with the upper trace of Fig. 3, taken from a Blameless Class-B amplifier at 50W into 8Ω .

Note the lower trace of Fig. 3 is for 30kHz bandwidth, to demonstrate the lack of distortion below 1kHz. All the Class-G plots here are taken at 80kHz to make sure any high-order glitching is properly measured.

Figure 4 shows the actual THD residual at 50W. The glitches from the gain steps are more jagged than the crossover disturbances, as would be expected from the output stage gain plots in the first article.

Figure 5 confirms that at 20W, below transition, the residual is indistinguishable from that of a Blameless Class-B amplifier; in this region, where the amplifier is likely to spend most of its time, there are no compromises on quality.

In Fig. 6, you will find THD plotted against level. This diagram demonstrates how THD increases around 28W as transition begins. The steps at about 10W are an artefact due to internal range-switching in the measuring system.

Figure 7 shows for real the beneficial effect of powering the inner drivers from the outer supply rails. In simulation, detailed in the previous article, the gain-steps were roughly halved in size by this enhancement. Figure 7 duly confirms that in the HF region – the only area where it is clear of the noise floor and can be measured – the THD is halved.

A new kind of amplifier - Class A+C

A standard Class-B amplifier can be converted to push-pull Class A simply by increasing the biasing to make the required quiescent current flow. This is the only circuit change, though naturally major increases in heatsinking and power-supply capability are required for practical use.

The same applies to the Class-G amplifier. Recently I suggested a new and more flexible amplifier classification system⁷ and here it is distinctly useful; describing Class-G operation as Class B+C underlines the fact that only a bias change is required to turn this into Class A+C, and a new type of amplifier is born.

This new amplifier configuration has the superb linearity of classic Class-A up to the transition level. Only minor distortion artefacts occur at higher levels, as demonstrated for Class B+C above. The use of Class A means that the simple V_{be} -multiplier bias generator can be replaced with precise negative feedback control of the quiescent current as in my Trimodal amplifier⁸. There is no reason why the amplifier could not be configured as a Class-G trimodal, i.e. switchable between Class A+C and B+C.

Figure 8 gives the THD for such an A+C amplifier working at 20W and 30W. At 20W the distortion is very low indeed – no higher than a pure Class-A amplifier. At 30W the transition gain-steps appear, but the THD remains very well controlled, and no higher than a Blameless Class B design. Note that as in Class B, when the THD does start to rise, it only does so at 6dB/octave. The quiescent current was set to 1.5A.

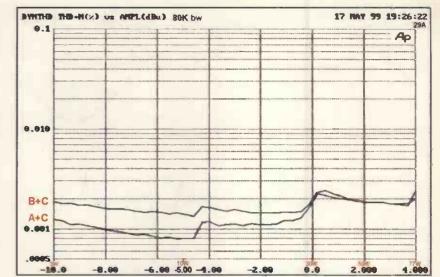


Fig. 6. THD versus level, showing how THD increases around 28W as transition begins. Class A+C is the lower and Class B+C the upper trace.

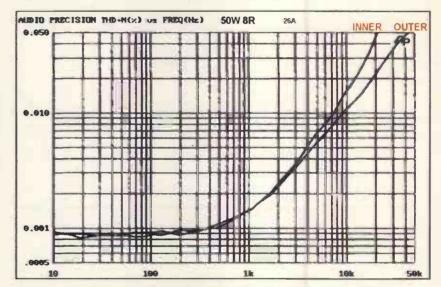


Fig. 7. THD plot of real amplifier driving 50W into 8Ω . Rails were ±40 and ±25V. Distortion at HF is halved by connecting the inner drivers to the outer supply rails rather than the inner rails.

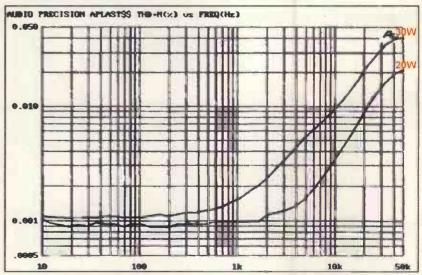


Fig. 8. The THD plot of the Class A+C amplifier. (30W and 20W into 8Ω) Inner drivers powered from outer rails.

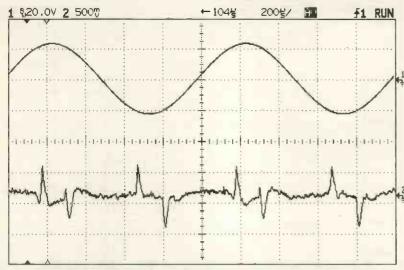


Fig. 9. The THD residual waveform of the Class A+C amplifier above transition, at 30W into 8Ω . Switching artefacts are visible but not crossover distortion.

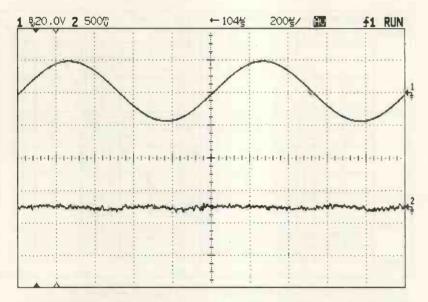


Fig. 10. The THD residual waveform plot of the Class A+C amplifier. (20W into 8Ω)

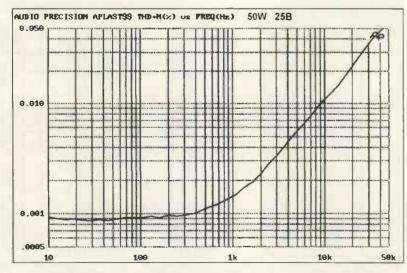


Fig. 11. The THD plot plot of the Class A+C amplifier. (50W into 8Ω) Inner drivers powered from outer rails.

In Fig. 9, the THD residual for A+C operation is revealed. There are absolutely no crossover artefacts, and the disturbances that do occur are at such a high signal level that I really do think it is safe to assume they could never be audible.

Figure 10 shows the complete absence of artefacts on the residual when this new type of amplifier is working below transition; it gives pure Class-A linearity.

Finally, Fig. 11 gives the THD when the amplifier is driving the full 50W into 8Ω ; as before, the A+C THD plot is hard to distinguish from Class B, but there is the immense advantage that there is no crossover distortion at low levels. There is also no need for critical bias settings.

Two-pole compensation

I have previously shown⁹ that amplifier distortion can be very simply reduced by changes to the compensation. This means a scheme more sophisticated than the near-universal dominant pole method.

It must be borne in mind that any departure from the conventional 6dB/octave-all-the-way compensation scheme is likely to be a move away from unconditional stability. (I am using this phrase in its proper meaning; in control theory, unconditional stability means that increasing openloop gain above a threshold causes instability, but the system is stable for all lower values. Conditional stability means that lower open-loop gains can also be unstable.

A conditionally-stable amplifier may well be docile and stable into any conceivable reactive load when in normal operation, but show the cloven hoof of oscillation at powerup and power-down, or when clipping. This is because under these conditions the effective open-loop gain is reduced.

Class-G distortion artefacts are reduced by normal dominant-pole feedback in much the same way as crossover non-linearities, i.e. not all that effectively. This is because the artefacts take up a very small part of the cycle and are therefore composed of high-order harmonics. Therefore a compensation system that increases the feedback factor at high audio frequencies will be effective on switching artefacts, in the same way that it is for crossover distortion.

The simplest way to implement two-pole circuit compensation is shown in Fig. 12. Further details are given in reference 10.

The results of two-pole compensation for B+C are shown in Fig. 13; comparing it with Fig. 2 – the normally compensated B+C amplifier – the above-transition (30W) THD at 10kHz has dropped from 0.008% to 0.005%; the sub-transition (20W) THD at 10kHz has fallen from 0.007%to 0.003%.

Comparisons have to be done at 10kHz or thereabouts to ensure there is enough to measure. Now, comparing the two-pole B+C amplifier with the A+C amplifier, Fig. 8, the above-transition (30W) THD at 10kHz of the former is lower at 0.005% compared with 0.008%.

As I have demonstrated before, proper use of two-pole compensation can give you a Class-B amplifier that is hard to distinguish from Class-A – at least until you put your hand on the heatsink.

Further variations

This by no means exhausts the possible variations that can be played on Class-G. For example, it is not necessary for the outer devices to operate synchronously with the inner devices. So long as they turn on in time, they can turn off much later without penalty except in terms of increased dissipation.

In so-called syllabic Class- G, the outer devices turn on fast but then typically remain on for 100ms or so to prevent glitching; see reference 11 for one version. Given the good

results obtained with straight Class-G, this no longer seem seems a promising route to explore.

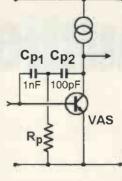
In summary

With the unstoppable advance of multi-channel amplifier and powered sub-woofers, Class-G is at last coming into its own. It has recently even appeared in a Texas ADSL driver IC.

I hope I have shown how to make it work – and then how to make it work better. From the results of a Web search done today, I would modestly suggest that this might be the lowest distortion Class-G amplifier so far.

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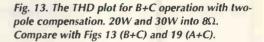


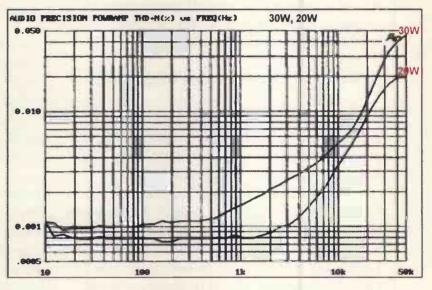
compensation.

Fig. 12. Circuit

two-pole

modification for





PCBs for Class G

Circuit boards for Doug Self's Class-G amplifier are available. These PCBs are double-sided with full solder masks and roller-tinning. Full component identifications are also included. Their size is approximately 190mm by 175mm each. To order a pair of these boards, send a cheque or postal order for £43.50 to Jackie Lowe, Class-G PCBs, Anne Boleyn House, 9-13 Ewell Road, Cheam, Surrey SM3 8BZ. E-mail electronics.world@ntlworld.com for details of overseas postage. You can also fax your credit-card details – name and address of card holder and card type, number and expiry date – on 01782 878233 (+44 1782 878233). Please make cheques payable to Cumulus Business Media.



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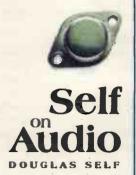
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Why not visit:http:www.radio-tech.co.uk Firing off with an explanation of why multiple shielding layers work, Joe Carr presents a multitude of tips for making your designs more EMI proof.

> f you delve into very sensitive equipment, such as receivers and scientific instruments, you will find certain critical circuits double-shielded. The reason is that each shield will produce a reduction of signal by 60 to 100dB – although the latter figure requires very good shielding.

Let's assume that the run-of-the-mill shield provides 60dB of attenuation. If two such shields are provided, one inside the other, then the total attenuation will be of the order of 120dB. This is why very sensitive or very high gain instruments use double shielding – especially in their front-end circuitry.

Multi-compartment shielding

In some sensitive instruments, it is necessary to provide multiple internal shielded compartments to isolate circuits from each other, and from the external environment.

In Fig. 1 three circuits are placed inside individual

shielded compartments within an overall shielded box. General rule No 2 is:

The number of shielded compartments required is equal to the number of individual circuits that must be protected, plus one for each power entrance.

Spray-on shielding

A lot of equipment today is built in plastic or other synthetic non-conducting forms of cabinet. Unfortunately, such cabinets are an EMI nightmare.

In some instances, the manufacturer may apply a conductive coating to the inside of the plastic case to provide shielding. Copper, aluminium and silver conductive sprays and paints exist. However, they don't always provide a very good shield, so care must be taken.

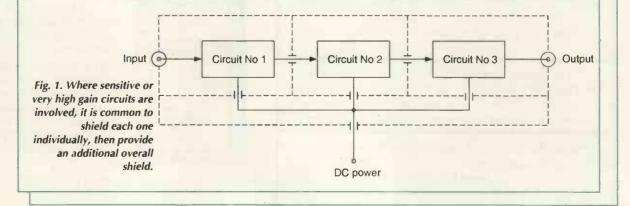
First, of course, is to make sure that the material selected is intended for making shielding. Not all silver, copper or aluminium paints are truly conductive. And many such paints are not intended for shielding, so may produce a metal density and thickness that is insufficient.

The best one can say about some products is that they are better than nothing – but not much.

Connectors, meters and dials

Objects that penetrate a front or rear panel, or go through the wall of a shielded compartment, pose special problems of shielding.

Figure 2 shows several different problems, and how they can be handled. The case of a digital or analogue meter is shown in Fig. 2a). The large hole cut in the panel for the meter can provide a means for EMI to



enter or leave the compartment.

A shielding cover is placed over the rear of the meter movement, completely enclosing it except for a small hole with grommet that allows the DC wires to pass in and out. If only DC is carried by the wire, then it's also possible to use feed-through capacitors to carry the wires.

In some other instances, a connector for multi-conductor cable is used, Fig. 2b). The cable selected should be a shielded multi-conductor type. The rear of the connector is treated pretty much the same way as the meter movement. For many forms of connector the manufacturer will offer optional EMI shields, but for others a shield will have to be formed.

Figure 2c) shows the wiring for a multi-conductor shielded cable and connector. Assume that a generic circuit or signal source is inside a shielded housing, and it is connected to a shielded instrument through the cable. The signal, common and DC power supply lines are fed through separate conductors, while the shield for the source end is connected to the shield of the cable.

At the end where the connector on the

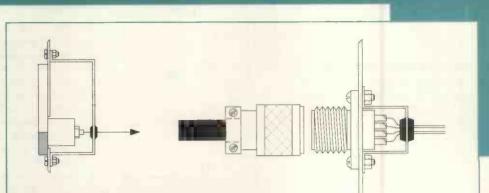
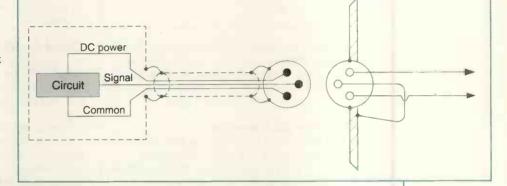
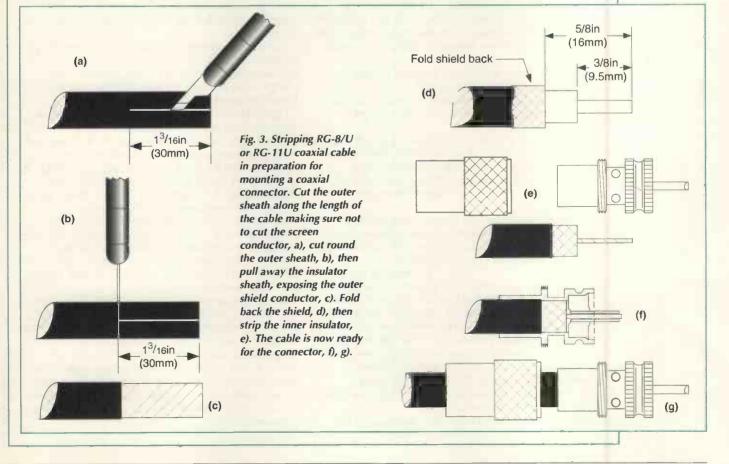
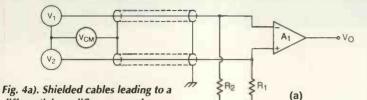


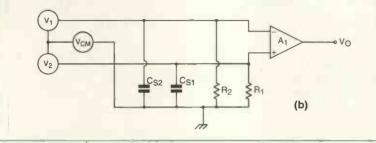
Fig. 2. Objects that penetrate a front or rear panel, or go through the wall of a shielded compartment, pose special shielding problems. Here are some solutions.







differential amplifier can produce a differential signal voltage, causing errors, a). An equivalent circuit is shown in b)



cable mates with the connector on the equipment panel, the same thing is repeated: shield of cable to shield of connector, with the wires kept separate. At some point just inside the cabinet it may be that the ground and shield are connected together with the cabinet shield.

Installing a coaxial connector

I've messed up my share of RG-8/U and RG-11/U coaxial cable in my time. Putting a PL-259 'UHF' coaxial connector on the end of a length of coaxial cable appears to be a daunting task. But it's really quite easy.

Figure 3 shows the steps. First, cut the cable to the length needed. In Fig. 3a), you can see the first connector step: slitting the outer insulation. Take care to slit *only* the outer insulation, and not damage the shield braid beneath it.

Use a razor knife, hobby knife or scalpel to make a 1^{37} (30mm) slit from one end of the cable. Next, as shown in Fig. 3b) make a circumferential cut at the inner end of the long slit, so that the outer insulation can be removed, Fig. 3c).

Once the outer insulation is removed, use a soldering iron to lightly tin the braid, making it stiff. Take care not to use too much heat, or the inner insulation will be damaged. Also, if too thick a layer of solder is laid on, then the connector will not slip over the end in the following steps.

Figure 3d) shows the next step: cut away the inner insulation so that 5/8in (16mm) of inner conductor is exposed. The inner insulator and shield will be flush with each other at the end of the 16mm section.

Figure 3e) shows the PL-259 UHF connector and the prepared cable. Now here's a bit of wisdom: unless the cable is relatively short, and you have free access to both ends, now is the time to slip the outer shell – the piece with the thumb threads – over the cable, back first.

Next, slip the inner portion of the connector over the exposed cable end, making sure that the inner conductor goes into the hollow connector centre pin, without bending or buckling, Fig. 3f). Some people prefer to solder tin the inner conductor, especially if the cable uses a stranded wire for the inner conductor.

Once the connector is firmly seated on the cable, Fig.

3g), use an ohmmeter to make sure there is no short circuit between inner and outer conductors. If the cable checks out on the ohmmeter, solder the outer shield to the connector by soldering through the view holes in the thinner portion of the connector.

Make sure that *all* of the holes are soldered. I've seen a connector 'tacked on' by soldering only one hole go bad. The connection failed... and the blankety-blank cable was buried inside a wall – which itself was an installation mistake! Finally, solder the inner conductor at the end of the hollow centre pin. After it has cooled check the cable with an ohmmeter.

I use a soldering gun with 100-200-250-watt three-way switchable settings, rather than a pencil iron. The pencil iron is fine for printed circuit boards, but the metal of the braid and connector sink heat enough to cool off the connection too much.

Give it a try... the connector is actually relatively easy to install.

Guard shielding

One of the properties of the differential amplifier – including the instrumentation amplifier – is that it tends to suppress interfering signals from the environment. The common-mode rejection process is at the root of this capability.

When an amplifier is used in a situation where it is connected to an external signal source through wires, those wires are subjected to strong local 50 or 60Hz AC fields from nearby power line wiring. Fortunately, in the case of the differential amplifier the field affects both input lines equally, so the induced interfering signal is cancelled out by the common mode rejection property of the amplifier.

Unfortunately though, the cancellation of interfering signals is not total. There may be, for example, imbalances in the circuit that tend to deteriorate the CMRR of the amplifier. These imbalances may be either internal or external to the amplifier circuit.

Figure 4a) shows a common scenario. In this figure, you can see the differential amplifier connected to shielded leads from the signal source, V_{in} . Shielded lead wires offer some protection from local fields, but there is a problem with the standard wisdom regarding shields: it is possible for shielded cables to manufacture a valid differential signal voltage from a common mode signal!

Figure 4b) shows an equivalent circuit that demonstrates how a shielded cable pair can create a differential signal from a common mode signal. The cable has capacitance between the centre conductor and the shield conductor surrounding it. In addition, input connectors and the amplifier equipment internal wiring also exhibit capacitance.

These capacitances are lumped together in the model of Fig. 4b) as C_{S1} and C_{S2} . As long as the source resistances and shunt resistances are equal, and the two capacitances are equal, there is no problem with circuit balance. But inequalities in any of these factors – which are commonplace – creates an unbalanced circuit in which common mode signal V_{cm} can charge one capacitance more than the other. As a result, the difference between the capacitance voltages, V_{CS1} and V_{CS2} , is seen as a valid differential signal.

A low-cost solution to the problem of shield-induced artifact signals is shown in Fig. 5a). In this circuit a sample of the two input signals are fed back to the shield, which in this situation is not grounded. Alternatively, the amplifier output signal is used to drive the shield. This type of shield is called a guard shield. Either double shields – one on each input line as shown – or a common shield for the two inputs can be used.

An improved guard shield example for the instrumentation amplifier is shown in Fig. 5b). In this case a single shield covers both input lines, but it is possible to use separate shields. In this circuit a sample of the two input signals is taken from the junction of resistors R_8 and R_9 , and fed to the input of a unity gain buffer/driver 'guard amplifier', A_4 . The output of A_4 is used to drive the guard shield.

Perhaps the most common approach to guard shielding is the arrangement shown in Fig. 5c). Here you will notice that two shields are used; the input cabling is double-shielded insulated wire.

The guard amplifier drives the inner shield, which serves as the guard shield for the system. The outer shield is grounded at the input end in the normal manner, and serves as an electromagnetic interference suppression shield.

Guard shielding on PCBs

The guard shield concept can be extended to the input pins of high-gain amplifiers on printed circuit boards. Figure 6 shows the method for placing a guard ring around a printed circuit pad – an IC pin for example.

The ring is grounded in most cases, but is always connected to the guard shield of the input cable. The centre conductor of the cable is connected to the pad itself.

The version shown in Fig. 6 keeps one end of the ring open in order to accommodate connection to the circuit board pad. If the board is two-sided or multi-layered, then the ring can be complete, with the connection to the pad occurring on the top or on one of the intermediate layers.

Guard shielding specialised amplifiers

There's a number of specialist integrated circuits on the market. These are often designed specially for analogue subsystems in PC-based instruments. In many cases though, they are more general in format.

An example of a general IC amplifier is Burr-Brown's INA-101AG device shown in Fig. 7. This is an integrated circuit instrumentation amplifier, A_1 , with the gain being

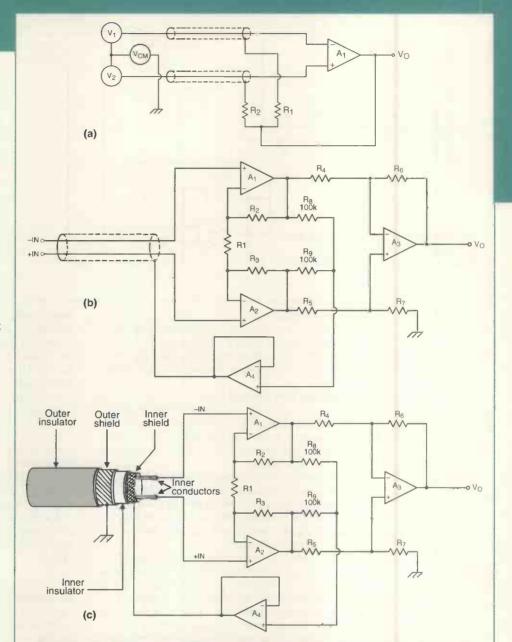


Fig. 5. It is possible to prevent signals from being generated in the shielded cables that feed a differential amplifier by using configuration a). Circuit b) is an improved – but more elaborate – solution. The most common implementation of this circuit, shown in c), uses cable with two shields and two conductors.

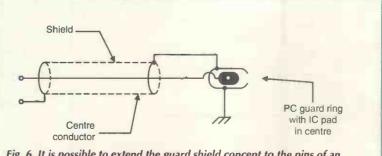
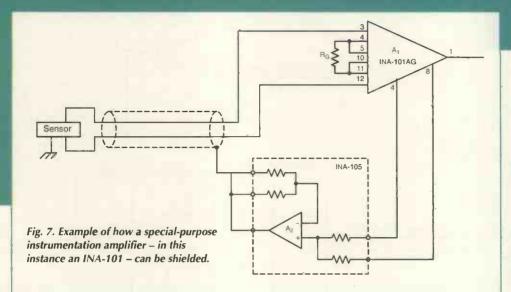


Fig. 6. It is possible to extend the guard shield concept to the pins of an integrated circuit, as shown.



set by an external resistor R_G .

This type of device has provision for guard shield connections directly to the IC - pins 4 and 8. These pins are fed to the separate inputs of a summing amplifier, the output of which drives the guard shield.

Grounding and ground loops

Impulse noise due to electrical arcs, lightning bolts, electrical motors and other devices can interfere with the operation of sensors and their associated circuits. Shielding of lines (see above) will help somewhat, but it isn't the entire answer.

As discussed below, filtering is useful, but it is at best a two-edged sword, and it must be implemented prudently and properly. Filtering on signal lines tends to broaden fast rise time pulses, and attenuate high frequency signals... and in some circuits causes as many problems as it solves.

Other electrical devices nearby can induce signals into the instrumentation system, the chief among these sources being the 50/60Hz AC power system. It is wise to use only differential amplifier inputs, because of their high common-mode rejection ratio. Signals from the desired source can be connected across the two inputs, and so become a differential signal, while the 50/60Hz ac interference tends to affect both inputs equally. As a result, it is common mode.

It is sometimes possible to manufacture a differential signal from a common-mode signal. Earlier I said that this phenomenon was due to bad shielding practices. In this section I am going to expand on that theme and consider grounds as well as shields.

One source of this problem is called a ground loop, and is shown in Fig. 8a). This problem arises from the use of too many grounds. In this example the shielded source, shielded input lines, the amplifier and the dc power supply are all grounded to different points on the ground plane.

Power supply dc currents, *I*, flow from the power supply at point A to the amplifier power common at point E.

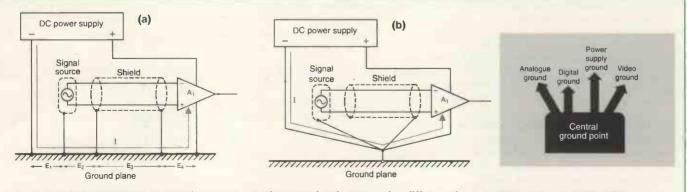
Since the ground has ohmic resistance – albeit very low resistance – the voltage drops E1 through E4 are formed. These voltages are seen by the amplifier as valid signals, and can become especially troublesome if I is a varying current.

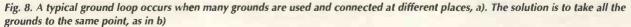
The solution to this problem is to use single-point grounding, as shown in Fig. 8b). Some amplifiers used in sensitive graphics or CRT oscilloscopes keep the power and signal grounds separate, except at some single, specific common point. In fact, a few models go even further by creating several signal grounds, especially where both analogue and digital signals might be present.

In some instances the shield on the input lines must not be grounded at both ends. In those cases, it is usually better to ground only the amplifier ends of the cables.

In summary

The matter of shielding electronic circuits for EMI isn't as simple as it appears. The guidelines in this article and the one last month will help you determine the correct way to go.





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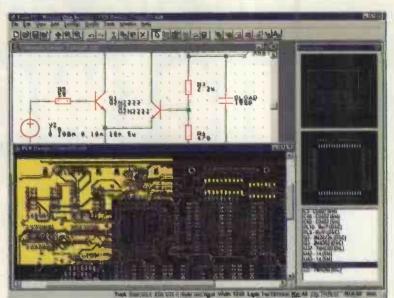
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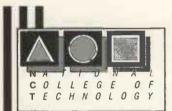
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36 via optical core Networking

Moe Rahnema* presents a vision for optical core networks in future 3G systems.

The explosive growth anticipated for the 3G wireless data applications and multimedia services is a major concern to wireless operators at the moment. The convergence of voice, data, and video services and the close integration with the fixed networks is raising issues of network inter-working, interoperability, mobility management and the provision of dynamic and flexible bandwidth in the core network.

A crucial factor is being able to meet the everchanging demand with a scalable network infrastructure and flexible transport technology. Flexible transport architecture is needed that is Internet-protocol friendly and provides efficient bandwidth on demand. It also

*Moe is a Senior Principal Consultant with LCC International, Inc.

What is a core network?

Third Generation – or 3G for short – is the name given to the wireless mobile networks that will offer broadband connections to data services – such as the Internet and intranets – at speeds of up to 2Mbit/s. Such networks are planned to support applications like streaming video, web searching, and access to location based data services, in addition to mobile telephony.

Second-generation networks, or '2G', are the digital networks currently in use. They operate at speeds between 9.6kbit/s and 16kbit/s, including GSM, TDMA, and CDMA technologies.

The 3G systems will be based on packet switching and transport on both the radio link, and within the core network used to provide the interface between the radio access network and the land line packet networks such as the Internet.

High throughput requirements and the service quality demand placed on the core network will make the design of the core transport infrastructure a challenge on its own. This article discusses alternative core network transport architectures based on evolving optical technologies, in the short and the long term, to provide scalable highcapacity core networks. needs to be easily reconfigured to meet the demands of mobile users.

This new transport infrastructure should be flexible to allow the rapid introduction of new services and be managed with minimal complexity.

Core network – a key investment

For 3G network deployments, the core network is a key investment that operators must make in order to secure a superior competitive position by allowing them to offer an extensive variety of services.

Customers will measure their wireless operator on both the ease and flexibility of the access to this expanding variety of services. The core network should ideally be based on an architecture that is independent of the type of access technology. This will allow interoperability with existing and future access technologies.

Most of the current models proposed for core networks consist of four layers: IP and other contentbearing traffic, ATM for traffic engineering, the SONET/SDH transport network, and dense wave division multiplexing (DWDM) for fibre capacity. Such models involving mixing and matching of numerous technologies can ultimately suffer from functional overlaps. They can also suffer from conflicting performance tuning among their layers, and unnecessary complexity. This approach is ineffective in using the evolving optical transport and switching technologies.

The numerous data and multimedia services in the 3G networks, and the scaling of the core network, can make the traffic between pairs of backbone routers reach a single optical carrier level such as OC-48c or OC-192c, making the ATM's virtual path equivalent to a wavelength.

Benefits of ATM's fine virtual path granularity – including quality of service – make it eminently suitable for the access network. In the optical core, where the appropriate switching granularity becomes the wavelength, path granularity becomes irrelevant.

In addition, effective management of these large and numerous virtual paths depends on the widespread introduction of the private network-to-network interface (PNNI). This is ATM's dynamic virtual path provisioning and restoration protocol.

Even then, PNNI's restoration times will be measured in seconds to minutes – far inferior to the 50ms benchmark set by the SONET/SDH ring. As a result, ATM switches do not offer compelling value for the long-term inclusion in the optical core. In addition, the availability of IP routers capable of operation at the wire speed of 10Gbit/s will make the SONET/SDH grooming function unnecessary.

Other bottlenecks – current architectures

A further drawback in the four-layer architecture is in providing multigigabit bandwidth across a pair of routers located in two cities. This will require the availability of bandwidth across all Sonet/SDH rings along the connection route, and the manual intervention at the ring junctions. Furthermore, the optical ring interconnects can result in increased worst-case network delays due to the failure initiated re-routeing mechanisms used in the ring architecture.

A second drawback is the fact that the layers are unaware of each other, resulting in increased overhead and duplication of their services. Error correction may be performed twice, or flow control may be performed both at the ATM, and the TCP windowing level, potentially resulting in conflicting actions.

With all said considerations, the future optical-core network is envisaged to be based on the transport of IP over WDM using the evolving wavelength switching and optical cross connect (OCX) technologies.

With intermediate SONET/SDH and ATM switches eliminated, only two switching elements – the wavelength router and the IP router – are needed in the long-haul optical infrastructure with dense wavelength division multiplexing (DWDM) elements.

The IP routers placed at the edge of the optical meshed network groom packets from DS-1, DS-3, OC-3, and OC-12 flows to OC-48c or OC-192c streams. The wavelength router maps these streams to wavelengths for end-to-end transport across the network.

SONET/SDH ADMs, and ATM switches may still be used at the edge of the network, in addition to the IP routers, for the grooming and transport of circuit switched traffic such as voice, signalling, and video through the multigigabit transport network.

Provisos for success

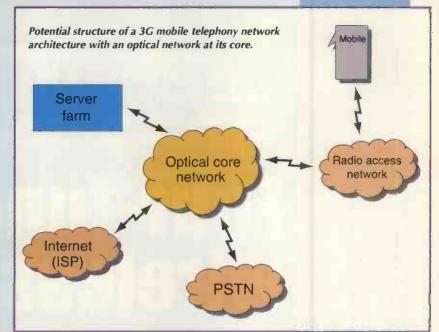
The success of IP over WDM will depend of course on whether the IP layer can support the necessary QOS mechanisms, and whether the WDM can provide survivability as robust as SONET and SDH.

The efforts at the IETF for providing effective QOS at the IP layer has led to the creation of the multiprotocol label switching (MPLS) standard. MPLS combines the intelligence of IP routing and the fast switching of ATM and thereby introduces the notion of connectionoriented forwarding to IP networks.

When packets from a particular session enter the network, they are sent along the same path by giving them all the same initial label by the edge router. Each intermediate node on the path uses the packets label as an index into a look-up table to find the next hop for the packet and a new outgoing label, hence the term label switching.

At the WDM layer, the label-switching concept of MPLS is extended to include wavelength-routed and switched-light paths. Hence, MPLS takes the name multiprotocol wavelength switching (MPLS).

As the name implies, in MPLS, the wavelength of the light serves as its own label. In MPLS, IP packets from one or multiple sessions are mapped to a wavelength by the edge IP routers which are then routed through a mesh of wavelength switching optical cross connect (OXC) nodes.



Currently, there are OXC technologies available (for instance from Ciena, and Sycamore) that allow the network operator to rapidly configure optical paths between any pairs of routers. The routers placed at the edge of the network are connected through a mesh of the optical cross connect wavelength switching elements.

The configuration of paths within the optical meshed interconnect is done through a rather simple point and click process. These available technologies can be used advantageously in the migration process to the future models of optical transport and routeing.

In the longer run, the provision of optical paths will be made automatically through real-time signalling exchanges between the edge IP routers and the optical wavelength routers. Initially, this realisation will most likely take place by having the signalling exchange performed through an optical cross connect controller (OCC) entity using separate signalling interfaces. The OCC uses the topology and resource availability information it maintains on the optical transport network to provide circuit switched services to IP and other higher layer protocols.

As the standards for addressing and signalling for a unified control plane are resolved and worked out, the border routers and the optical cross-connects will be able to directly exchange signalling and routing information. This model will distribute the route determination and paths set up process and result in a scalable network control infrastructure.

Also, the use of standardised protocols and mechanisms for the exchange of signalling and routing information will allow for the mixing of equipment from different vendors and open up competition for the equipment markets.

The network operators will be able to take advantage of the evolving optical networking technologies both in the short and the long run to provide scalable high capacity core networks. This will allow the support of a diverse range of services with different bandwidth and QOS requirements through a single core infrastructure with the advantages of simplified management, operation and maintenance. Working over a 433MHz wireless link via standard RF modules, J Terrade's remote-control system drives four functions – left, right, forwards and backwards for example – without resorting to the complexity of a microcontroller. An addressing system allows many such controllers to be used in the same environment and a PWM motor drive scheme provides an extra degree of control.

Four-function wireless remote

y original idea was to design a four-way remote control system with constraints on size, cost and complexity. Two three-way switches provide the control information. Parallel data representing the switch positions is translated to serial form read for transmission. The serial data is conveyed over a 433MHz wireless link then, on receipt, translated back to parallel data.

Functional diagram Fig. 1 shows that a 9-bit data packet is used. On the transmitter side, the four data bits and a five bits of identification code are converted from parallel to serial. The data packet is sent continuously. Then the total information arrives at the HF transmitter.

On the receiver side, the nine bits are converted from serial to parallel. Then the received identification code is compared to the local code. The comparison result clocks the four data bits for the D-type latch. I use this configuration to control a small batterypowered boat with a two-way remote control switches. The boat has two DC motors, one for propulsion, the other for direction.

Transmitter analysis

Figure 2 details the transmitter. Since power consumption is 10mA during transmission, a 9V battery can be used, allowing the unit to be fully portable.

Diode D_1 protects the device against polarity inversion. Components K_1 and K_2 are momentary three-way switches with a normally centre off position. The user must push the switch in one direction and keep it there to maintain the desired action. When released, the switch returns to its null position.

When K_1 and K_2 are centred, the logical levels on D6

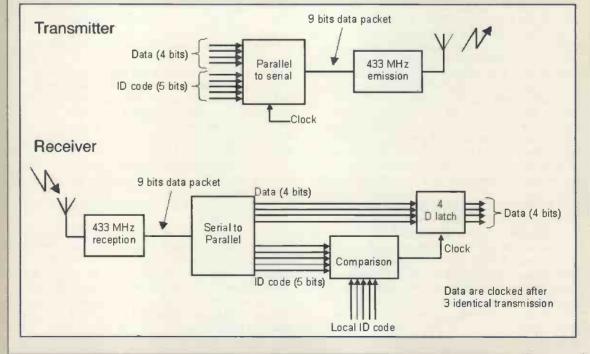
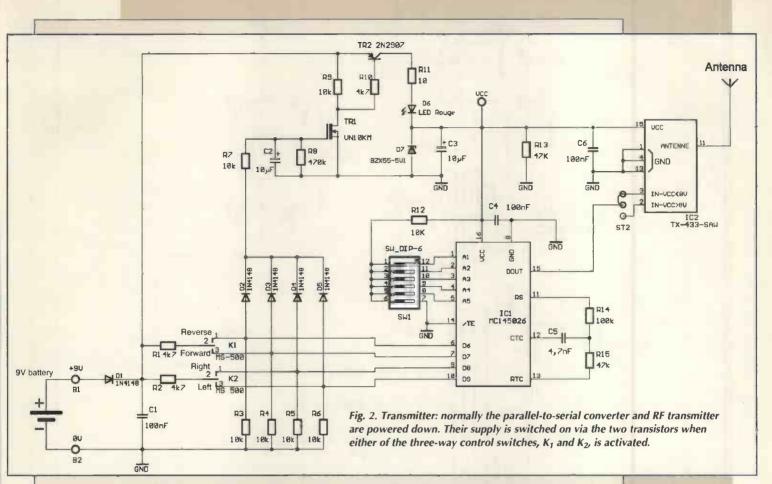


Fig. 1. Block diagram of the complete wireless remotecontrol system. The transmitter/recei ver combination is set by the user to respond to a unique identification code, or 'address'. In theory, over 200 such systems could be used in the same location without conflicts.



to D9 of IC_1 are low due to $R_{3.6}$. When K_1 or K_2 is activated, the voltage at the corresponding data input D6 to D9 of IC_1 becomes close to 5 volts, resulting in a logic high level. Note that K_1 and K_2 can be activated at same time.

Divider R_1/R_3 or R_1/R_4 resulting from activating K_1 , and likewise dividers R_2/R_5 or R_2/R_6 from K_2 , produces an acceptable level for IC_1 's inputs.

Diodes D_2 to D_5 ensure rapid charging of capacitor C2 through R_7 . When this capacitor is charged, Tr_1 conducts, as does Tr_2 . Diode D_6 acts as a power-on indicator. When the two transistors are turned on, zener diode D_7 is fed via D_6 , and R_{11} , resulting in a +5V power supply being fed to both IC_1 and IC_2 with 5 volts.

Capacitor C_2 remains charged until both switches return to their off position. Then C_2 discharges through R_8 . After approximately 8 to 10 seconds, the transistors turn off, removing power supply to the two ICs.

Inputs A1 to A5 of IC_1 are three-state inputs representing low level, high level and not connected level. This would allow 243 combinations, i.e. 3^5 . But threestate DIP switches are expensive and besides, 64 possibilities are enough for most applications.

If pin 6 of DIP switch SW_1 forces a low level – i.e. the switch element associated with pin 6 is closed so that it is connected directly to ground – address inputs A1 to A5 can be used to select between low level and open circuit. If pin 6 of SW_1 is allowed to be pulled high through R_{12} , address inputs A1 to A5 can be used to select between high levels and open-circuit. This arrangement gives 64 combinations.

Components R_{14} , R_{15} and C_5 attached to IC_1 form the local oscillator. Output from IC_1 at pin 15 provides the 9 bits of data packet for the HF transmitter, IC_2 . An amplitude-modulated HF module is used.

Our antenna comprised a single wire of 17cm length attached directly to the PC board.

Note that during all time power is on, transmission occurs. After K_1 and K_2 have been released, the transmitter continues to send null position information until power goes off. This period is around eight seconds. Timing relationships for the transmitter are shown in Fig. 3.

Receiver details

Figure 4 shows the circuit for the receiver. Its antenna is again a single wire of 17cm attached directly to the circuit board.

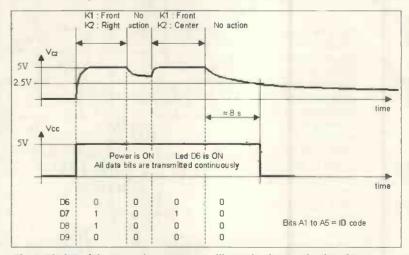
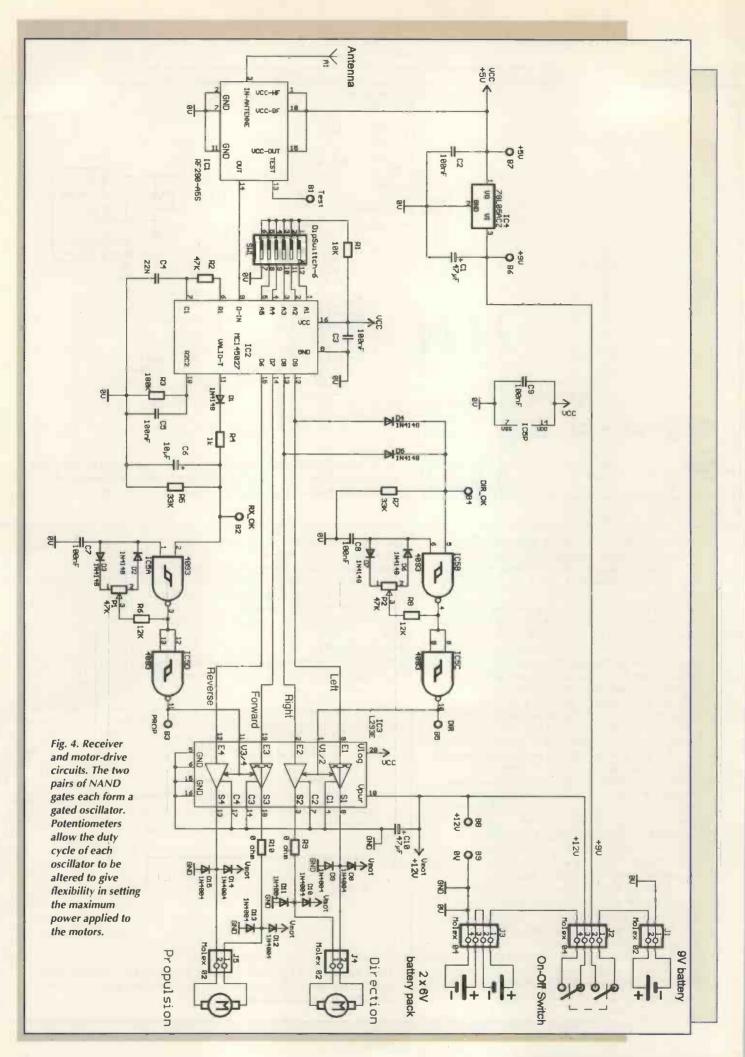
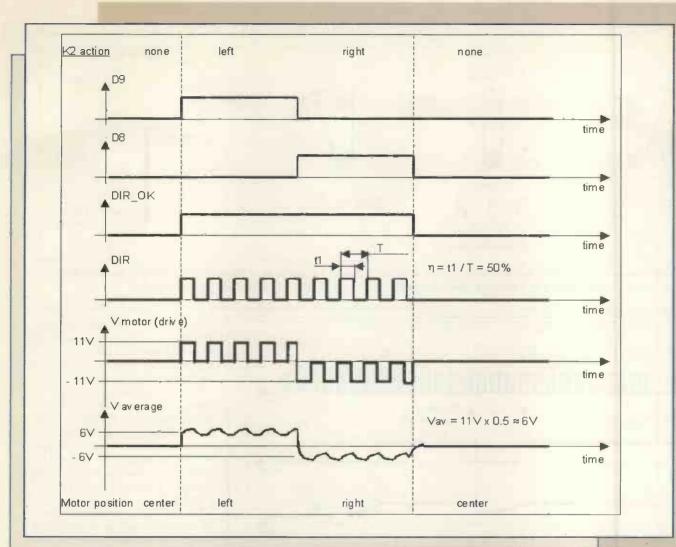


Fig. 3. Timing of the transmitter sequence, illustrating how activating either switch causes the auxiliary power supply to turn on. This supply stays on for around 8s after the switches are released.





Incoming signals arrive at the HF module, IC_1 , which is powered by a stable 5V supply. The 9-bit data packet is available at its output, pin 14. As with the transmitter, the DIP switch SW_1 gives up to 64 possibilities for the identification code. This switch must be set to the same combination as that of the transmitter.

The four data bits are available at outputs D6 to D9. Direction bits D9 and D8 connect to R_7 via diodes D_4 and D_5 . They form a wired-OR function. When either 'direction' bit is active – i.e. at a high level – the 'DIR_OK' signal is high.

Components IC_{5B} , R_8 , P_2 , D_6 , D_7 and C_8 form a gated oscillator. When the 'DIR_OK' signal is high, this oscillator is gated on and produces a square wave at pin 4 of IC_{5B} – resulting in the 'DIR' signal. Gate IC_{5C} inverts the 'DIR' signal.

When neither direction bit is active, 'DIR_OK' signal is low and the oscillator stops, Fig. 5.

Direction control

The 'DIR' signal connects to the enable input of IC_3 , pin 1. This pin controls the three-state output of IC_3 , an L293 wired as an H bridge.

A low level at pin 1 creates a high impedance at output pins 8 and 3. A high level allows outputs D9 and D8 – on pins 9 and 2 – to drive the direction motor right or left, Table 1.

When the 'DIR' signal is low, the left/right motor is not driven and returns to its centred (zero) position with the mechanical action from a spring

When 'DIR' signal is a square wave, the direction motor is driven by a square wave voltage. The period of DIR signal is small compared to the motor's time

Table	1		
Logic t	able for	the 'left	/right' motor drive.
DIR	L	R	Motor
0	Ø	Ø	free wheel
1	0	0	electrical brake
1	0	1	turn right
1	1	0	turn left
1	1	1	not used
Ø = do	n't care		

constant so the motor works as if a reduced DC voltage was present.

The equivalent voltage for the motor is given by :

 $V_{average} = V_{max} \times \eta$

where η is the duty cycle, i.e. tl/T. This technique is a form of pulse-width modulation, Fig. 5.

Adjusting potentiometer P_2 gives control between 20% and 80%. In this way, you can vary the direction motor current and power. Should you expect the motor to become jammed in either direction, you can adjust P_2 to avoid its destruction.

In this application, the motor drive a rudder with an 45° angle. This angle is limited by an arm attached to the rudder and a mechanical stop. The centred (null) position is fixed by a helical double-action spring. In this way, when the motor is not electrically driven, the rudder returns automatically to the null position, Fig. 6.

Forwards and backwards?

When a valid transmission arrives at the receiver,

Fig. 5. Timings for the receiver's 'left' and 'right' functions. A potentiometer allows the duty cycle of the pulse to be set to suit the motor.

Tx/Rx modules Apologies, but I was unable to find out who makes the transmitter and receiver modules before this article went to press. I'll publish a note

availability in the next issue - Ed.

about their

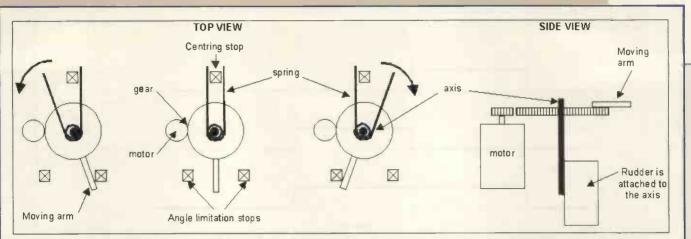
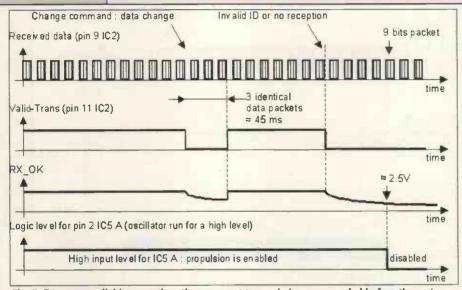


Fig. 6. The remote controller described here was originally designed to control a model boat. In the prototype, rudder left and right drive was provided by a motor fitted with a spring to return the rudder to its centre position when there was no drive signal.



voltage at pin 11 goes high. But each time the user changes the commands from the transmitter, the 'Valid-Trans' signal goes low until the new transmission is considered as valid.

Three correct transmissions are needed. Therefore a stable 'RX_OK' signal is necessary. Toward this end, D_1 , R_4 , R_5 and C_6 create a time constant. As a result of this constant, the 'RX OK' signal goes low only when transmission stops, i.e. when transmitter has no supply and stops transmitting, Fig. 7.

The 'RX_OK' signal acts exactly as the 'DIR_OK' signal in the receiver. It controls an oscillator whose duty cycle can be adjusted via P_1 . Then the Prop signal can enable the bridge with pin 11 of IC_3 , Table 2.

Data bits D6 and D7 control the propulsion motor's direction of rotation to drive the model, or whatever, forwards or backwards.

The part of IC_3 taking care of forward and reverse works in a three-state configuration, Fig. 8. Propulsion motor power and energy consumption can be adjusted be set via potentiometer P_1 .

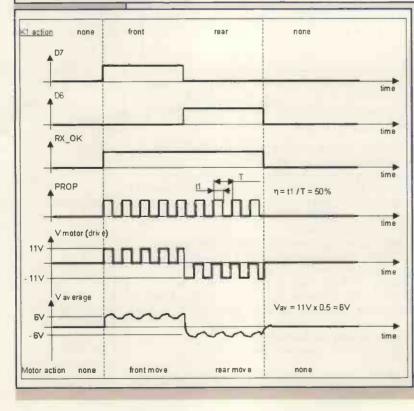
One of the two power supplies for this section is a 9V battery pack used in conjunction with a voltage regulator IC_4 . This supply provides a stable 5V for the receiver and the logic section.

The other supply is a 12V battery pack – or accumulator – which provides power for the two motors.

Fig. 8. Timing of the remote-control system's propulsion functions.

Table	2		
Logic ta	ble for for	ward, rev	verse and braking.
Prop	Front	Rear	Motor
0	Ø	Ø	free wheel
1	0	0	electrical brake
1 -	0	1	forward
1	1	0	reverse
1	1	1	not used
Ø = do	n't care		

Fig. 7. To ensure reliable operation, three correct transmissions are needed before the system allows a propulsion action.



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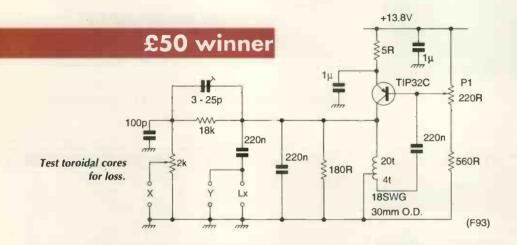
CIRCUITIDEAS

Toroidal core analyser

Toroidal cores are useful things, but the problem is that many are unmarked, and most core manufacturers have their own colour code. Furthermore, individual cores can exhibit bad properties.

Professional inductance analysers must be provided with powerful excitation generators, having very little harmonic content, and this is reflected in the price. A simple oscillator is not suitable, but it can be provided with an attenuator that allows you to distinguish between the harmonics of the generator and those of interest, caused by the core material

The display on the oscilloscope screen is not a hysteresis loop, but a distorted Lissajous figure. It is essential to use polypropylene capacitors in the circuit, or better still polystyrene capacitors, whose power factor is even better. With these capacitors an '80 metres' coil can be successfully tuned down to 85kHz. Even so, a 180 Ω bleeder resistor is still needed in order to make it less



sensitive to load variations.

A p-n-p transistor was chosen as it allows the cold end of the coil to be connected to ground. About an amp of current is applied to the test item, which ensures enough signal for a scope with 50mV per division sensitivity.

Using a 2.2μ F polypropylene capacitor as test item, adjust the phase trimmer so that a diagonal line, sloping up from left to right, appears on the screen. A diagonal line, sloping down from left to right, would indicate a perfect inductance.

With a practical coil, the included area in the display is proportional to the ohmic loss. With cores down to a permeability of 100, a single turn will suffice. Otherwise, 2 or 3 turns can be tried.

Note that the oscilloscope is used in 'XY'mode. The Y probe tip should be connected directly to the toroidal hot lead-out wire, and both the cold lead-out and the probe return lead connected to ground as directly as possible.

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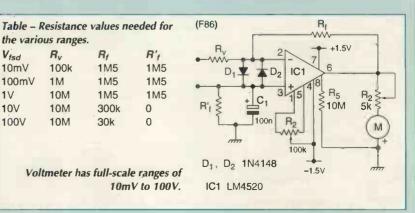
Clear hand-written notes on paper are a minimum requirement: disks with separate drawing and text files in a popular form are best – but please label the disk clearly.

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Wide range dc voltmeter

A resistor inserted in series with one of the input leads of the basic meter amplifier converts it into a wide range dc voltmeter.

Gain of the inverting amplifier is -30for the 10mV full scale deflection range, falling to -0.003 for the 100V fsd range. Values of R_v , R_f and R'_f for each range are listed in the table. Diodes D_1 and D_2 provide complete amplifier protection for overvoltages up to 500V on the 10mV range, but if overvoltages of this magnitude are expected under continuous operation, the power and voltage ratings of R_v must be taken into account. **Rajik Gorkhali** Address not supplied F86



CIRCUIT IDEAS

Measure rotation speed and direction

M any applications require the speed and direction of rotation of a shaft to be determined. Usually, this involves decoding the Gray coded output of an optical or magnetic sensor.

The circuit shown performs this decoding with just four NOR gates. It works as follows.

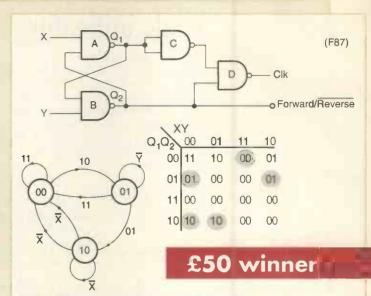
NOR gates A and B are connected as a bistable with inputs X and Y. Output $Q_1 = /(X+Q_2)$ and $Q_2 = /(Y+Q_1)$. The response of the Bistable to a Gray coded input on X and Y can be seen from the excitation map.

Rotation of the shaft is equivalent to traversing the map from left to right for one direction or right to left for the other.

You will notice that the circuit leaves state '10' to either state '00' or '01', depending on the direction that the code is moving in. NOR gates C and D produce a low-going clock edge as the circuit leaves state '10'.

The circuit can be used to drive a simple up/down counter, or interrupt a micro for further processing.

Jeremy Smith Sutton Coldfield West Midlands



Four NOR gates decode Gray code into direction and speed.

Latching touch switches with battery backup

One of the problems of avoiding the use of unreliable mechanical switches by using a fully electronic substitute is that the last state is usually lost when the power is switched off.

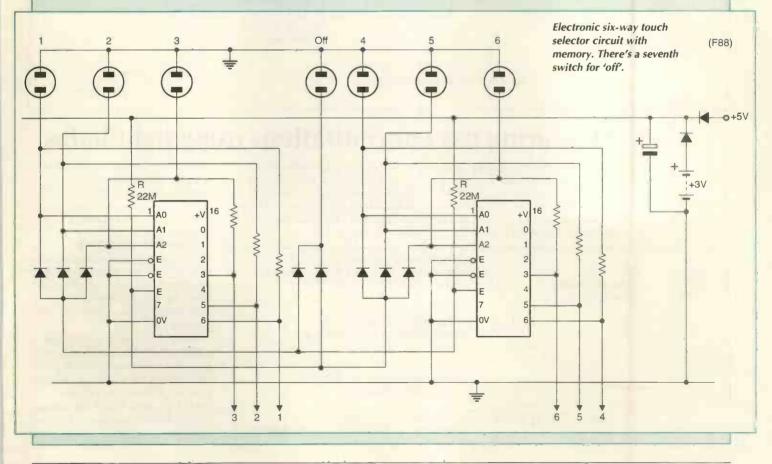
This design uses a pair of 74HC138 decoders, each providing three ways in a 6 way switch with a seventh 'off' position. A single chip could be used if only three ways plus 'off' is sufficient. With suitable gating, several such circuits could be cascaded to increase the number of switches.

Outputs are standard HCMOS active low, and quiescent current from a small lithium button cell little more than $10\mu A$.

Decouple all touch pads to the negative

line with 1nF capacitors to reduce possible triggering by interference. Resistors R are 22M Ω ; all others are 3.3M Ω . Gating diodes are 1N4148, the two power switching diodes 1N4001. A Ziemacki Rotherham

F88

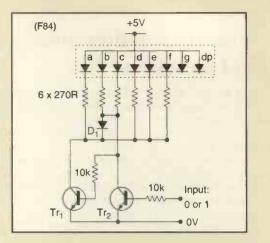


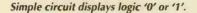
Logic indicator

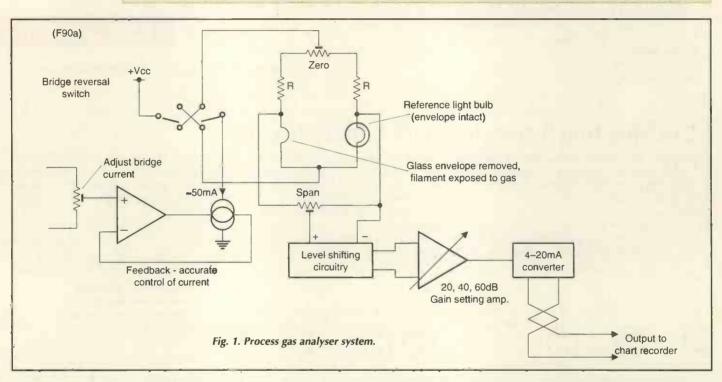
needed a logic circuit to display '0' or '1' when logic lines were low or high respectively. This circuit uses a seven segment display to achieve this..

When the input line is low Tr_2 will be off. Transistor Tr_1 will be biased on via the display segments and resistors, turning on segments a - f to display '0'. When the input line is high Tr_2 will turn on and Tr_1 off. Now, Tr_2 will turn on segments b and c only, to display '1'. **Brian T Cox**

Exeter F84



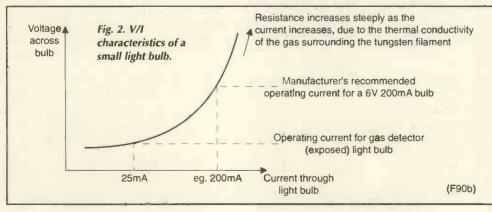




Measuring gas concentrations using light bulbs

An in-line process-gas measuring device can cost £5000 pounds or more, but a gas measuring transducer can be constructed for much less.

An in-line, continuous-running gasmeasuring device works by the principle of thermal conductivity. Conventionally this involves using two ultra-fine platinum wires fed by a stable current source. These wires are configured in a bridge arrangement as shown in Fig. 1.



A constant current through the cells linearises the output of the bridge. Platinum thermal conductivity cells, as they are known, are expensive and they may have an operational life of only five days.

Bench testing the feasibility of replacing expensive platinum cells by ordinary 6V torch bulbs, showed that 6V 200mA MES bulbs not only work better, but they also have a considerably greater service life than platinum cells.

A tungsten filament will burn out straight away without its protective glass envelope if operated at the manufacturer's recommended current. However, if the exposed filament is run at a quarter or less of the manufacturer's recommended current, then a 6V 200mA MES bulb exposed

CIRCUIT IDEAS

filament was found to work for weeks without burnout or failure. At 25mA through each bulb, the system was found to yield significant gain and excellent bandwidth.

To increase the gain of the bridge simply adjust the current source to a higher setting, but remember, increasing the current will shorten the cell's life and *vice versa*. With the zero/span adjustments, wide ranges may be obtained particularly if the output of the bridge feeds into a reset/zero op-amp (ICL7650s).

To remove the glass envelope without destroying the filament,* fix the bulb in a vice and then gently close the jaws until the glass envelope shatters, leaving the exposed filament intact. The associated electronic circuit blocks may be of a very simple design.

Figure 2 shows the response of a typical 6V MES bulb and Fig. 3 shows the necessary mechanical arrangement of the system.

Ďarren Heywood Buckley Flintshire

*While wearing eye protection of course - Ed

Antenna Toolkit

Second Edition

Joe Carr has provided radio amateurs and short-wave listeners with the definitive design guide for sending and receiving radio signals with Antenna Toolkit 2nd edition.

Together with the powerful suite of CD software, the reader will



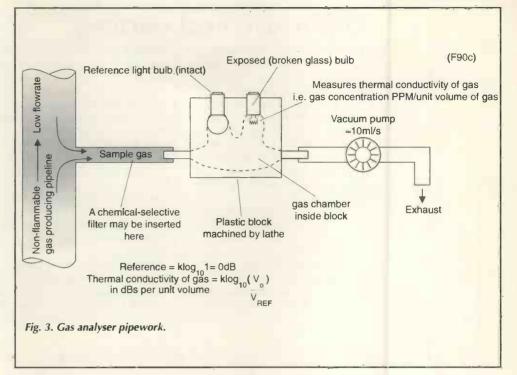
have a complete solution for constructing or using an antenna – bar the actual hardware! The software provides a simple Windows-based aid to carrying out the design calculations at the heart of successful antenna design. All the user needs to do is select the antenna type and set the frequency -a much more fun and less error prone method than using a conventional calculator to solve formulae. The new edition has been revised to include further cases of propagation, additional antennas and also two new chapters - Small Loop Antennas (a topic of considerable interest, which has been the subject of much recent debate in the amateur radio press); and Yagi Beam

Antennas (widely used at HF and VHF). The CD software has also been updated.

Joe Carr's expertise in the area of antenna design is legendary. Antenna designers, whether hobbyist or technician, can be assured they need look no further than Antenna Toolkit for the complete guide to understanding the practicalities of using and designing antennas today.

Preface; Radio signals on the move; Antenna basics; Wire, connection, grounds; Marconi and other unbalanced antennas;

Doublets, dipoles and other Hertzian antennas; Limited space antennas; Large loop antennas; Wire array antennas; Small loop antennas; Yagi beam antennas; Impedance matching; Simple antenna instrumentation and measurements; Getting a 'good ground'; Index.



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Engine overheat warning

Some time ago, the plastic radiator on my car split, causing the engine to overheat. I failed to notice the temperature gauge in time and some damage occurred.

I decided to make an audible alarm to avoid the same thing happening again. The circuit needed to be simple and reliable. This led to the three-transistor design incorporating an emitter-coupled differential amplifier.

Many car temperature sensors rely on a robust thermistor device screwed into the engine block. This device is often in series with a simple thermal ammeter.

As the engine heats up the thermistor its resistance, and hence the voltage across it, drops. This causes an increase in current flow and a higher reading on the thermal current meter. A simple check of the voltage on a given car thermistor at cold and running conditions will determine suitability for the following alarm circuit.

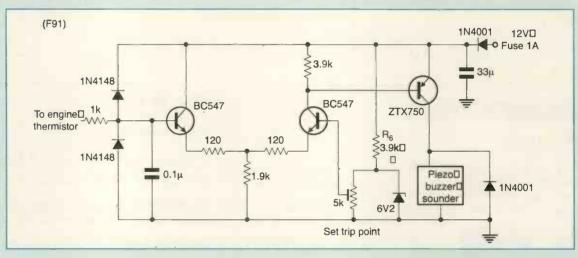
The two BC547 transistors form a temperature stable differential amplifier comparing the voltage set by the trimmer with the voltage drop across the engine thermistor. The trimmer should be a high-quality type or replaced with fixed resistors to assure maximum reliability.

On my Ford Sierra, the voltage change went from 5V cold to 2.5V with the engine at the full scale hot reading. I set the trip to around 3V. When the trip voltage is reached the ZTX750 conducts switching in the warning device; I used a small encapsulated alarm sounder which was ideal.

The whole circuit was mounted under the dashboard with the sense wire connected out to the engine block thermistor, avoiding runs that went close to hot or high voltage areas.

A 12 volt supply was taken from an ignition switched source using a clamp on 'scotch' connector and an in-line fuse. If desired a test button can be fitted across the 0. 1μ F capacitor at the input. *P W Fry*

Southampton F91



Optimising valve amplifier output transformers

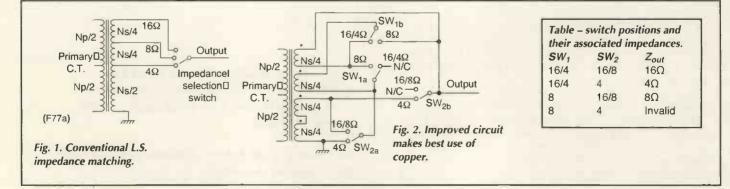
This idea arose while I was designing a 200W amplifier for bass guitar, and finding difficulty fitting the windings into a transformer core on hand.

Figure 1 shows the classic multi-tap method of connecting different loads to such a transformer. Half the turns are found in the 4Ω portion of the winding, so both this and the tap selection switching must be rated for the maximum load current.

There is a method of connection that reduces the wire gauge in this section to that required by the 8Ω load, Fig. 2; dots denote the winding phasing. This makes much better use of the copper and the switches need only be rated at the 8Ω load current.

Typically, one would wind the primary in four sections and interleave the secondary in sections, to reduce both the leakage inductance and the primary self-capacitance. Switch settings for the various loads are shown in the table. Care must be taken to select the corresponding settings. SW_1 set to '8' and SW_2 to '4' will result in shorting the transformer output. Malcolm Watts

Wellington New Zealand F77



NEWPRODUCTS

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Crosspoint switch with 85Gbit/s of bandwidth

I-Cube's latest crosspoint switch is an SRAM-based device that features a non-blocking 128 by 128 I/O switch matrix, delivering 667Mbit/s data bandwidth per port. The crosspoint-matrix CMOS is designed for use in Sonet and SDH and DWDM optical networking equipment running at OC-12 speeds. The foundation of the OCX device is the supplier's non-blocking crosspoint architecture that uses the switch matrix to connect input/output buffers in one-toone or one-to-many connections. A special broadcast mode routes a single input to all outputs at the maximum data rate for highbandwidth applications. A parallel interface allows fast configuration of the switch connections. The OCX256 is available with either low voltage differential signalling (LVDS) or low-voltage positive emittercoupled logic (LVPECL) I/O ports. I-cube

Tel: 001 408 341 1888 www.icube.com



Ceramic capacitors rated to 250V AC

Syfer Technology has introduced a range of surface-mount ceramic-multilayer chip capacitors approved by BSI to meet IEC safety standards. The Type A range features X1/Y2 devices in a 2220 chip size with a nominal capacitance range from 150pF to 4.7nF. The Type B capacitors are X2 devices, also in a 2220 package, and offer a nominal capacitance range from 150pF to 10nF. With a rated voltage of 250V AC, the capacitors operate over the -55to 125°C temperature range. They are specified with an insulation resistance of 1G Ω and are voltage proof tested to 3kV DC/2kV AC. Syfer Technology Tel: 01603 723310 www.syfer.com

5W laser diode

Available through Pacer Components, a 5W CW laser diode from Coherent Semiconductor comes in the 790 to 813nm range for solid state laser pumping, direct thermal medical and material processing applications. Based on an active area aluminium-free technology. which has extended diode lifetimes, the broad area emitter comprises three facets of 150µm length on $25\mu m$ gaps, making an overall emission area of 500 by $l\mu m$. The device is mounted on a standard 10.5mm wide by 25mm long conduction cooled package and operates at typically less than 6A and under 2V. Pacer Components Tel: 0118 984 5280 www.pacer.co.uk



Miniature colour and monochrome cameras

The Pecan range of miniature cameras available from Stortech Electronics has been designed where unobtrusive monitoring is required. Around the size of a 50 pence piece, these cameras are ideal for a wide variety of situations and can be installed in clock faces, in suitcases, doors, and bookshelves. Their small size also means that they will easily blend in with the surrounding environment. The cameras are available with monochrome or colour output options. These lightweight cameras are PCB based and are housed in a robust cast aluminium case including a mounting bracket. With a low current consumption of between 80-135mA, these miniature cameras come complete with an electronic iris that automatically adjusts itself to varying light conditions; contrast is thus continually optimised to provide the best image. Stortech Electronics Ltd Tel: 01279 451100



NEWPRODUCTS

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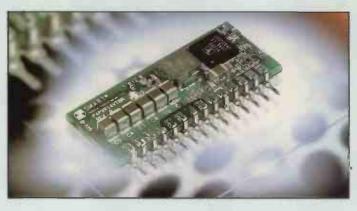
18GHz RF switch for multi-channel testers

Test engineers can increase channel count of their high frequency measurement applications with an 18GHz RF switch from National Instruments. The SCXI-1192 reduces the number of standalone RF instruments required for high-frequency test systems by expanding the number of available channels. The switch multiplexes signals up to 18GHz and features 50Ω characteristic impedance. With its eight singlepole double-throw (SPDT) relays, the module can route high frequency signals with minimal signal loss, said the company. The RF relays are bi-directional, so that engineers and scientists can route signals from multiple inputs to a single instrument or direct signals from a signal instrument to multiple destinations. National Instruments Tel: 01635 523545

Switching regulators

www.nicom/uk

Smart Modular Technologies is offering 14-pin integrated voltage switching regulator modules. These modules transfer input ranges from 3.3 to 5V to output ranges of 0.7 to 3.6V at 7A. Built onto a 14-pin smallinline-package (SIP) module, the switching regulators are designed to reduce the need for DC/DC brick-type regulators.



The range offers a lower output voltage to multiple subsystems without redesigning the central power supply.

Smart Modular Technology Tel: 0870 870 8747 www.smartmodulartech.com

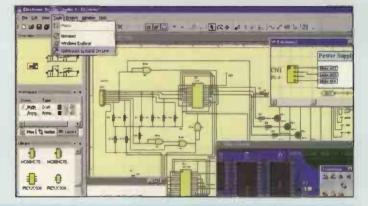
All-in-one CAD package

Ouickroute has launched Electronic Design Studio 3 - a combination of three programs in one integrated package. A new feature of EDS 3 is 'desktop manufacture,' which works together with precision CAM hardware to machine a range of prototype PCBs directly on your desktop and without using chemicals. EDS is project based. With project and net navigators, you can jump to any document, module, symbol, gate or pin with the click of a mouse. A new overview window lets you zoom to any part of your document with a single click. CADCheck keeps the PCB design synchronised with the schematic

in real time. EDS is available with full support for modular, hierarchical, multi-sheet schematics. Visual tags make linking between modules and sheets easier, and there is full support in the project navigator. The package includes an enhanced Spice/XSpice based simulator. All the symbol and simulation properties can be set directly within EDS, and you can create your own models, extend the libraries supplied, or use external SPICE models. All output is displayed in graph windows within EDS ready for pasting into your reports. There's a range of new PCB editing tools including 'follow me' wiring, intelligent pads which change colour when correct links are made. A new polyblend module lets you weld polygons, punch holes in polygons and more. With the latest 'XP' look and feel, EDS 3 is available in four variants, with prices starting at under £100 for systems with autorouting and simulation. A free demo pack is available. Quickroute systems Tel: +44 1422 255010 www.dotgr.com

Multi-source generator for Bluetooth

IFR Systems has launched its first multi-source signal generator capable of generating multiple Bluetooth and GSM carriers within one instrument. For Bluetooth interoperability testing, the 2026B with



Audio amplifier boards with better than 0.2% distortion and noise

Built around the ZXCD1000 switching amplifier controller, two new evaluation boards from Zetex provide complete mono and stereo Class D audio amplifiers attaining total harmonic distortion plus noise (THD+N) ratings of less than 0.2% in open loop, reducing to a typical of 0.05% in a closed loop configuration. Enabling a full appraisal of a high performance 50W RMS (4Ω load) class D solution, the evaluation boards employ Zetex components throughout. Comprising audio input stage, PWM controller, output bridge and magnetics, these compact reference designs achieve efficiencies of greater than 90%, some 40% better than Class A or B alternatives. With the enhanced amplifier efficiency obviating the need for heatsinks and enabling power supplies to be reduced in size, the reference designs offer lower cost per watt solutions for a wide range of equipment, from DVD players to PA systems. The evaluation boards are supported by full documentation, bill of materials and pcb layout files. *Zetex*

Tel: 0161 622 4444 www.zetex.com



Please quote Electronics World when seeking further information

Bluetooth option 117 can replace two or three separate signal sources, says the company. The signal generator is a 10kHz to 2.51GHz source. It can be fitted with either two or three signal sources that can be combined together onto a common combiner output, or routed to individual outputs. Each of the signal sources can be frequency and amplitude-coupled so that common measurements, such as intermodulation or receiver selectivity can be made. The Bluetooth option 117 can accept external data sources for Bluetooth and GSM generators or it can use internal pseudorandom binary sequence (PRBS) generators. Bluetooth Option 117 has a new RF combiner system that allows an external source of signals (a GSM test set or Bluetooth test set) to be added to the combiner output while using all three of the 2026B sources

IFR Systems Tel: 01438 772087 www.ifrsys.com

600V IGBTs for motor driving

International Rectifier has expanded its line of Co-Pack IGBTs with the IRG4BC15UD. 15UD-S and 20UD-S devices. The IGBTs are for appliance motor drive applications such as variable speed fans, blowers, refrigeration compressors and washing machine pumps and agitators. The IRG4BC15UD and IRG4BC15UD-S deliver up to 5.5A or 1.1kW with a smaller silicon die than previously available devices with the same efficiency level, said the supplier. The IRG4BC20UD is

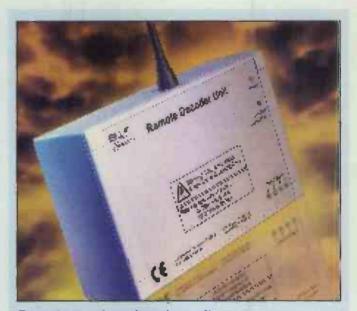


available in a D2Pak surface mountable version as the IRG4BC20UD-S for power levels up to 1.3kW. In appliance applications, motor drive designers increase frequency up to 20kHz to reduce the size and cost of passive components and to reduce undesirable audible noise. The Co-Pack IGBTs are capable of switching at speeds up to 20kHz. International Rectifier Tel: 020 8645 8003 www.ift.com

Wireless Tx and Rx modules for high interference

The latest miniature FM transmitter and receiver modules from RF Solutions, the QFMT6 transmitter and OFMR6 receiver are fully shielded, off-the-shelf modules that will suit vehicle alarms, domestic and commercial security systems, process monitoring schemes and computer networking applications. Particularly suited to applications operating in areas of high interference or high levels of radio traffic, the modules allow designers to implement data links with speeds up to 64kbit/s and operating distances of 200m. Both the OFMT6 and OFMR6 are fully pin compatible with existing modules. Each device can operate from a 5V supply and will work at temperatures of up to 55°C as standard. The QFMR6 is also available in an extended temperature version that is rated for operation between -40 and 80°C. **RF** Solutions Tel: 01273 898 000 www.rfsolutions.co.uk





Remote receiver decoder unit

The 105 series remote decoder from RF Solutions can operate as either a radio, infrared or pager system. The unit is compatible with most transmitter encoders offered by the Sussex based company. This enables the user to select the optimum transmitter frequency, modulation and range characteristics to suit their specific application. Operation as a stand alone pager controller can be achieved by using a Globemaster module G100UK. The unit is suited for use in applications such as remote power control, remote restart for computer equipment and remote security control. The 105 receiver decoder is available with radio frequencies of either 433, 458 or 868MHz, and features an innovative selflearning feature that enables it to decipher the signature code of up to 50 RF Solutions KEELOQ Tx encoders. The KEELOQ encryption algorithm provides the world's most advanced security protocol.

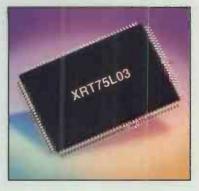
RF Solutions Tel: 01273 898 000 www.rfsolutions.co.uk

E3 transceiver with jitter attenuator

Exar has introduced a threechannel line interface unit (LIU) with an integrated transceiver and jitter attenuator for E3, D83 and STS-1 applications. The XRT75L03 is the first in a family of multi-channel, multifunction products using low power CMOS process technology. It incorporates three independent receivers, transmitters and jitter attenuators in a single-chip. The device is targeted at applications including access equipment, digital crossconnect systems, ATM switches, routers and fibre optic terminals. The device incorporates a B3ZS/HDB3 encoder and decoder, transmit drivers with tri-state output capability and

line monitoring circuitry for redundancy applications. It also contains an onboard pseudorandom binary sequence (PRBS) generator and detector with the ability to insert and detect single bit errors. This function can be used for diagnostic purposes. *Exar Tel: 00 33 4 9364 7755*

Tel: 00 33 4 9364 7755 www.exar.com



NEWPRODUCTS

Please quote Electronics World when seeking further information

Buck controller with dynamic output control

Maxim's latest buck controller features a dynamically adjustable output and is designed for use in CPU core power supplies. The firm's proprietary Ouick PWM constant on-time PWM control scheme is claimed to handle wide input/output voltage ratios and provides 100ns response to load transients, while maintaining a constant switching frequency. The MAX1813 is designed specifically for CPU core applications requiring a voltage-positioned supply. The voltage positioning input, combined with a high DC accuracy control loop, is used to implement a power supply that modifies its output set point in response to the load current. This arrangement decreases full-load power dissipation and reduces the required number of output

capacitors, said the firm. The output voltage is dynamically adjusted via the 5-bit DAC inputs over a range of 0.6V to 2.0V. Output slew rate control minimises battery and inductor surge currents. With this precision circuit, V_{OUT} slew rate can be tailored to a given application, providing a 'just-intime' arrival at the new d-to-a converter setting. Maxim Tel: 0118 930 3388

www.maxim-ic.com

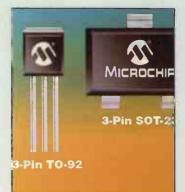
Low-power voltage reference for hand-helds

Microchip's latest precision voltage references are designed to combine a low operating current and an initial accuracy down to ±1 per cent. The 2.5V MCP1525 and 4.096V MCP1541 are capable of



1.4MHz switching regulator cuts external components

National Semiconductor has introduced a pulse-width modulation (PWM) inverting switching regulator which is capable of supplying -5V from a 5V or 12V input and is designed to deliver the power for set-top box tuner and LCD display designs or other voltage inverter requirements. Its 1.4MHz oscillator permits the use of smaller external components while the Cuk topology reduces peak current and the external component count, said the supplier. The LM2611 operates from inputs of 2.7V to 14V and is capable of producing a negative output voltage of up to $-(36V - V_{in})$. It has a low 0.5Ω switch and features internal compensation and cycle-by-cycle current limit. It is suitable for creating the negative bias for active matrix displays or CCDs in digital cameras or creating -5V for the tuners in set-top boxes and cable modems. National Semiconductor Tel: 0870 240 2171 www.national.com



supplying up to 2mA of load current, while operating at an operating current of 100pA at 25°C. EPROM trimming provides an initial tolerance of lper cent (maximum) and temperature stability of 50ppm/°C. The devices are available in 3-pin SOT-23 and TO-92 packages. *Microchip Tel:* 0118 921 5858 www.mlcrochip.com

Optical-fibre connectors

Radiall's range of fibre-optic connectors, cables and assemblies, called the LC series, are designed for high density applications where space is a key consideration since, according to Radiall, they are half the size of currently available standard fibre optic connectors. Incorporating precision zirconia 1.25mm ferrules, the series can accommodate 0.9 and 1.6mm cable diameters and are compatible with the industry RJ45 standard. Radiall Tel: 020 8991 7700 www.radiall.com

Dual-mode RF chip set

Zarlink Semiconductor (formerly Mitel Semiconductor) has a new



RF chip set for cellular hand-sets operating in dual-mode TDMA/AMPS networks that are installed primarily in North America. The MGCMO2 and MGCTO4 devices have a complete intermediate frequency receiver, baseband interface and transmitter in a two-chip solution. The MGCMO2 is an IF receiver and baseband interface chip. The device integrates Zarlink's existing MGCRO1 IF receiver and MGCMO1 baseband interface chips into a single 49-pin 7 by 7mm ball grid array (BGA) package. The MGCTO4 transmit circuit provides the transmit function in dual-band, dual-mode TDMA/AMPS and CDMA/AMPS mobile telephones. The chip is in a 5 by 5mm micro lead frame (MLF) package. Total chip-set area is 75mm² of board space. The chips are now sampling. The chip set is priced at about \$5 in high volumes. To support customer evaluation and ease of design, Zarlink offers an evaluation board featuring both devices, plus a reference design. Zarlink Semiconductor Tel: 01793 518128 www.zarlink.com

Integrated colour sensors

From Pacer are the new range of integrated colour sensors from Texas Advanced Optoelectronic Solutions (TAOS). Designated the TSL X257 series, the new devices consists of three individual optoelectronic sensors that provide on-board conditioning plus colour filters. Each of the three new colour sensors is designed to detect one of three primary colours: red, blue or green. The TSLR257 detects red light; the T5LB257 blue light and the T5LG257 detects green light. All three TAOS colour sensors are built on the TAOS light-to-voltage converter platform with a colour filter deposited on the detector chip. Colour identification applications for the sensors include CRT screens test and set up, colour tone scanning applications on printed materials, paints and cosmetics, process control, medical diagnostics such as body fluid analysis as well as

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Kit will program ALL 8, 18, 28 and 40 pin serial AND parallel programmed PIC micro controllers. Connects to the parallel port of a PC. Supplied with fully functional pre-registered PICALL DOS and WINDOWS AVR software packages all components and high



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ATMEL 89xxxx Programmer



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Powerful programmer for Atmel 8051 micro controller family. All fuse and lock bits are programmable. Connects to serial port. Can be used with ANY computer & operating system. 4 LEDs to indicate programming status. Supports 89C1051,

89C2051, 89C4051, 89C51, 89LV51, 89C52, 89LV52, 89C55, 89LV55, 89S8252, 89LS8252, 89S53 & 89LS53 devices. NO special software required - uses any terminal emulator program (built into Windows). **NB ZIF** sockets not included.

Order Ref	Description	inc. VAT ea
3123KT	ATMEL 89xxx Programmer	£32.95
AS3123	Assembled 3123	£47.95

Atmel 89Cx051 and AVR programmers also available.

PC Data Acquisition & Control Unit

With this kit you can use a PC parallel port as a real world interface. Unit can be connected to a mixture of analogue and digital inputs from pressure, temperature, movement, sound, light intensity,

LASAP



weight sensors, etc. (not supplied) to sensing switch and relay states. It can then process the input data and use the information to control up to 11 physical devices such as motors, sirens, other relays, servo motors & two-stepper motors.

FEATURES:

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- 11 Analogue Inputs: 0-5V, 10 bit (5mV/step.)
- 1 Analogue Output: 0.2.5V or 0-10V. 8 bit (20mV/step.)

All components provided including a plastic case (140mm x 110mm x 35mm) with pre-punched and silk screened front/rear panels to give a professional and attractive finish (see photo – lid removed) with screen printed front & rear panels supplied. Software utilities & programming examples supplied.

Order Ref	Description	inc. VAT ea
3093KT	PC Data Acquisition & Control Unit	£99.95
AS3093	Assembled 3093	£124.95

Number

Mitten

'Hotchip'

or sound a buzzer? The ABC Mni 'Hotchip' Board is based on Atmel's AVR 8535 RISC technology and will interest both the beginner and expert allke. Beginners will find that they can write and test a simple program,

leaming

microcontrollers? Need to do something more than flash a LED

about

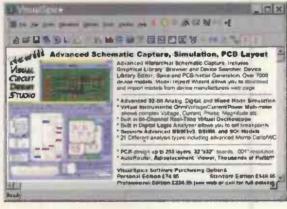
using the BASIC programming language, within an hour or two of connecting it up. Experts will like the power and flexibility of the Atmel microcontroller, as well as the east with which the little Hot Chip board can be "designed-in" to a project. The ABC Mini Board 'Starter Pack' includes just about everything you need to get up and experimenting right away. On the hardware side, there's a pre-assembled micro controller PC board with both parallel and serial cables for connection to your PC. Windows software Included on' CD-ROM features an Assembler, BASIC complier and in-system programmer The pre-assembled boards only are also available separately.

ABC Mini 'Hotchip' Board

Currently

ŧ.	Order Re	Description	inc. VAI ea
I	ABCMINISP	ABC MINI Starter Pack	£64.95
l	ABCMINIB	ABC MINI Board Only	£39.95

Advanced Schematic Capture, Simulation Software



Serial Port Isolated I/O Controller

Kit provides eight 240VAC/12A (110VAC/15A) rated relay outputs and four optically isolated inputs. Can be used in a variety of control and sensing applications including load switching, external switch input



sensing, contact closure and external voltage sensing. Programmed via a computer serial port, it is compatible with ANY computer & operating system. After programming, PC can be disconnected. Serial cable can be up to 35m long, allowing 'remote' control. User can easily write batch file programs to control the kit using simple text commands. NO special software required - uses any terminal emulator program (built into Windows). All components provided including a plastic case with pre-punched and silk screened front/rear panels to give a professional and attractive finish (see photo).

Order Ret	Description	inc. VAT ea	
3108KT	Serial Port isolated I/O Controller Kit	£54.95	
AS3108	Assembled Serial Port Isolated I/O Controller	€69.95	

Full details of these and over 200 other projects can be found at <u>www.QuasarElectronics.com</u>

NEWPRODUCTS

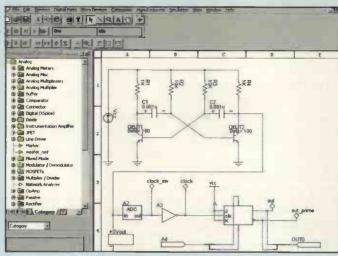
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dental, fabric and fashion applications. Colour filtering applications include fluorescence and mark detection, optical band pass filters as well as medical diagnostic applications. The devices are mounted in side looking plastic packages. Future devices will include linear array colour detectors and single packaged devices with three primary colour detection plus reference photodiode. Pacer Tel: 0118 9845280

www.pacer.co.uk

B² Spice now has PCB facilities

Due to be released in the UK in January 2002, new B² Spice AD version 4 replaces B² Spice 2000. Key features of the new version are its integrated PCB facility and its ability to model radio frequency circuits and networks. The user interface has been redesigned, and the resulting graphs and diagrams produce accurate data that is of practical use to professional designers and students alike. To help you to produce meaningful graphs, B² Spice AD version 4 enables each trace to be selected. processed and measured at any point for an exact result. The data can also be viewed in a range of formats to suit the user and exported for further processing. The new feature list



includes a standard library of over 8000 analogue and digital models; it even includes many vacuum tubes. B² Spice AD version 4 comes with a library management tool enabling the user to add to or modify existing symbols or models and make entire new libraries if required. The generic parts list is extensive and includes all the normal components that you would expect, as well as everything from a seven-segment display to a multi-way connector. The developers have made sure that B² Spice AD Version 4 sets no limit on the size of the circuit, its maker claims. It can be as large or as complex as the user wants. Just about everything can be customised to suit user requirements while the list of

simulation options is as extensive as a designer could wish for. The software comes with a comprehensive 400-page user manual with tutorials and there's free unlimited technical support.

RD Research 01603 872331 www.spice-software.com

Small surface-mount crystals

Advanced Crystal Technology has further reduced the size of its surface mount crystals with the ACT200. Measuring 8.0 by 3.8 by 2.5mm, the 32.768kHz ACT200 is compatible with existing PCBs, yet occupies 50% less volume. Suitable for many personal, portable domestic and mobile applications, the ACT200 also requires very low drive level at lµW maximum. Frequency tolerance to ±5ppm, combined with low frequency temperature coefficient at -0.034ppm/°C, create a stable reference throughout the industrial temperature range -40°C to +85°C. By retaining the footprint of previous generation 32.768kHz watch crystals, the ACT200 is drop in compatible with existing designs, while the reduced dimensions allow designers to save weight and space

The ACT200 is suitable for automatic placement from tape and reel. It is able to withstand peak soldering temperature up to 260°C, and therefore compatible with the majority of reflow profiles.

ACT Tel: 0118 979 1238 www.advancecrystaltechnology .com

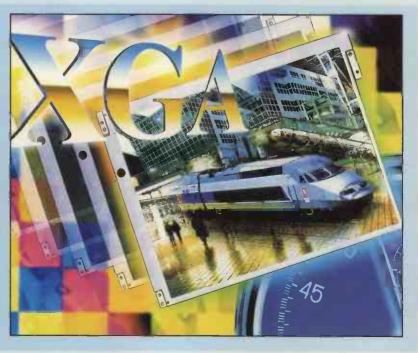


XGA LCD reduces circuitry

With an eye to reducing additional circuitry and components in applications ranging from industrial displays to automated cash machines and electronic ticket kiosks, Toshiba has introduced this 38cm (15 inch) XGA LCD. Called the LTM15C441, it comes with analogue RGB video interface, an integrated inverter, and two built-in CCFL backlights. Brightness levels are up to 200cd/m² and display luminance is adjustable over the range 30 to 100 per cent by means of an on-screen menu. Backlight life is a claimed 50 000 hours. The on-screen display features language options of English, German, French, Spanish and Japanese. Pixel pitch is 0.297 by 0.297mm, maximum resolution is 1024 by 768 and active display area is 304 by 228mm. Horizontal and vertical viewing angles are 120° and 90° respectively. Overall size is 340x257x29mm and it weighs 2.3kg. Operating voltage

is 12V, with TTL-level inputs providing horizontal and vertical synchronisation signals.

Tel: 0049 529625 www.toshiba-europe.com



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MISCELLANEOUS ITEMS HP 4261 LCR meter - £650. HP 4261 LCR meter - E550. HP 4274 FX LCR meter - £1,500. HP 3488 Switch Control Unit + PI Boards - £500. HP 35000 VXI Bus Controllers + £13268 DVM-quantity. HP 35204 GSM 05:92605 1090 MC/S convertor for use with 8922A - £2,000. HP 1530-1651-1550 Lopic ANZ's in st. dk; HP 9554 - £2,000. A + c

1P 87544 100 k ANZ 4- 00MC/S 8754A Network ANZ H2 4-2600MC/Su 8502A E2,000. HP 8350A Sweeper MF + 83540A Pt 2-8,4GHz 1 5.9-12 4GHz at 3 - C3,500. HP MICROWAVE TWT AMPLIFIER 4891 -20.

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 FOR FRANCHIPER 8447A 0.1-400MC/S
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 HP PREAMPLIFIER 8447A 0.1-400MC/S
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 HP POWER AMPLIFIER 8447E 0.01-1.3GHz - £400.
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 Odal - £300

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 Odal - £300

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 Odal - £300

 MARCONI 2505 Modulation Meter- 50KHz - 2.3 GHz - F100
 Odal - £300

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 Odal - £300

 MARCONI 2505 Modulation Meter- 50KHz - 2.5 GHz - 5100
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TM500% 5006. TEK PI 5010-M3 - Pi og Multi Interland - 1250, FG Pro-20MC/S Function Fran - 1400 - S1 Prog Scanner - 12 - D-DM Prog DM1 - 12400 TEK 7000 OSCILLOCOPE MAINFRAME - 603 - 23 - 634 7854 7904 7904 7104 - 6160-51000, TEK 7000 - 75 - 7411-7412 74137 4137 4194 - 22-7424 7426 7429 7442-7810-7615 78534 78 - 7885 78924 - 1011 1020. TEK 7000 - 7511-7512-7514-7MT1-S1-52-S3A-S4-S5-S6-S51-S53-85

S51-S53-864 HP POWER SAPPLIES - 6621A-6623A Grys available: Also 6000 types £PO

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 LT50.

 P 3582.A 01.al 0.2Hz-25.5kHz
 LT50.

 P 3582.A 01.al 0.2Hz-25.5kHz
 E150.

 HP 3583.A 00Hz-40MC/S
 L5.500.

 HP 3583.A 10Hz-150MC/S
 L5.500.

 HP 3583.A 10Hz-1.50Hz
 L5.3500.

 HP 85688.100Hz-1.5GHz
 L5.400.

 HP 85688.100Hz-1.5GHz
 L5.000.

 HP 85080 SCC
 L5.147.241.500.

 HP 85081 SCC
 L5.147.241.500.

 HC 8021 SCH 80.142.241.500.001.225.500.
 L5.2500.

 TE(4922P S0kHz-21GHz-21GHz OPT 1-2-3.500.
 L5.350.001.240.001.240.000. TEK492BP 50KHz-21GHz - £3,000-£4,000 TEK495 100kHz-1.8GHz - £2,000. HP 8557A 0.01MC/S-350MC/S - £500 + MF180T or 180C -£150 - 182T - £500. H9 85588 0.01-1500MC/S - £750 - MF180T or 180C - £150 -182T - £500. HP 8559A 0.01-21GHz - £1,000 - MF180T or 180C - £150 -HP 8901A AM FM Modulation ANZ Meter – £800. HP 8901B AM FM Modulation ANZ Meter – £1,750.

HP 8903A Audio Analyzer - £1,000. HP 8903B Audio Analyzer - £1,500.

MARCONI 2370 SPECTRUM ANALYZERS - HIGH QUALITY - DIGITAL STORAGE - 30th-1101, cfc berne gty to clear as received from Gov - all solvas is from the complete or add £100 for basic testing and adjustment - railers preferred adjustment - allers preferred pick your own from five

A EARLY MODEL GR. Y - horizontal alloy cooling fins -

B LATE MODEL GREY - vertical alloy cooling fins - £300. LATE MODEL BROWN - as above (few only) - £500.

SCILLOSCOPES

TEK 465-455B 100MC/S + 2 probes - £250-£300. TEK 466 100MC/S storage + 2 probes - £200. TEK 475-475A 200MC/S-250MC/S + 2 probes - £300-£350. TEK 2213-2213A-2215-2215-2215-225-2236-2245-60-100MC/S - 2250-2400 TEK 2243 4ch 150MC 2 2 p pes - £450. TEK 24454 4ch 150MC 2 2 p pes - £450. 100MC/S - £250-£400 TEK 2445 4ch 150MC - 2 partes - £450, TEK 2445 4ch 150MC - 2 partes - £450, TEK 24454 4ch 100 + 2 partes - £500, TEK 4468 3.5, 100 + 2 + 2 partes - £500, K 465 350MC/S - £ 1,550, TEK 2465 4 ch-350MC/S - £1,550, TEK 2465 4 ch-350MC/S - £1,550, TEK 256 246-350MC/S - £1,550, TEK 256 2465 - 100MC/S - 2 partes - £1,750, TEK 256 2465 - 800MC/S - 2 partes - £1,750, TEK 256 2465 - 800MC/S - 2 partes - £2,000, TEK 256 2456 - 800MC/S - 2 partes - £2,000, TEK 256 2456 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 200MC/S - 40 - 2 partes - £2,000, TEK 256 246 - 800MC/S - 200MC/S - 40 - 200MC/S - 40

TEK TAS 475-485 -100MC/S-20MC/S-4 ch + 2 probes - £900-£1.1K

HE1740A - 100MC/S + 2 probes - £250. HE1740A - 100MC/S storage + 2 probes - £200. HP1220A - 1722A - 1725A - 2 MC/S + 2 probes - £300-taol

5400 HP 745A - 100MC S - 1026 - 1026 - 2250. HP 745A - 1126A - 300 - CS - 1026 - 2350. HP 54100A - 16H2 - 104 - 105 - 105 - 105 HP 54200A - 100 - CS - 100 - 105 HP 54200A - 100 - CS - 100 - 105 HP 54200A - 100

ROWAVE COUNTERS - ALL LED READOUT MH 251D Autohet 20H2-18GHz – £750. EIP 371 Micro Source Locking – 20H2-18GHz – £550. EIP 451 Micro Pulse Counter – 300MC/S-18GHz – £550. P Microwave Frequency Counter 5484 Microwave Frequency Counter

ng - 10 crowave Source - £1.2K. P Fall z BGHz - £1.2 MC/S-26.5GHz -Microwave Pulse AK

1

Er.4K. SD 6054B Micro Counter 20Hz-24IGHz – SMA Socket – £800. SD 6054B Storto Counter 20Hz-18GHz – N Socket – £700. SD 6054D Micro Counter 800MC/S-18GHz – £600. SD 6246A Micro Counter 20Hz-26GHz – £1.2K. SO 8244A Micro Counter 20Hz-26GHz – £400. HP3052B Micro Counter OPT 010-005-46GHz – new in box – HD

 HP5340A
 Micro Counter OP1 010-005-46GH2 - new in box

 C5k
 HP5340A
 Micro Counter 10Hz-18GHz - Nixey - £500.

 HP5342A
 Micro Counter 10Hz-18-24GHz - £800-£1K - OPTS
 001 002-003-003-011.

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 HP5345A + \$00MCR5
 11 Digit LED Readout - £400.
 HP5345A + 5355A
 Plugin - 4GHz - £700.

 P5345A + 5355A
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 1536A 18GHz Head - £1K.

 P5385A
 IGHz 5386A-5386A
 3GHz Counter - £1K-£2K.
 Bacal/Danz Counter + £14.
 Racal/Dana Counter 1991-160MC/S – £200. Racal/Dana Counter 1992-1.3GHz – £600. Racal/Dana Counter 9921-3GHz - £350.

SIGNAL GENERATORS

HP8640A – AM-FM 0.5-512-1024MC/S – £200-£400. HP8640B – Phase locked – AM-FM-0.5-512-1024MC/S – 500-£1.2K. Opts 1-2-3 available. HP8654A – B AM-FM 10MC/S-520MC/S – £300. HP8656A SYN AM-FM 0.1-990MC/S – £900. HP8656B SYN AM-FM 0.1-990MC/S – £1.5K. HP86505 STN AMI-FM 0.1-3300MC/S - £13A. HP8657A SYN AMI-FM 0.1-1040MC/S - £2K. HP8660C SYN AMI-FM -PM-0.01-1300MC/S-2600MC/S - £2K. HP8660D SYN AMI-FM -PM-0.01-1300MC/S-2600MC/S - £3K. HP8630D STM AM-FM-FM-0.01-26.5 GHz – 612K. HP86312A Function Generator AM-FM 13MC/S-Dual – 6300. HP3312A Function Generator AM-FM 13MC/S-Dual – 6300. HP3325A SYN Function Generator 21MC/S – £800. HP3326A SYN 2CH Function Generator 13MC/S-IEEE – £1.4K

HP3336A-B-C SYN Func/Level Gen 21MC/S - £400-£300-

Racal/Dana 9081 SYN S/G AM-FM-PH-5-520MC/S - £300. Racal/Dana 9082 SYN S/G AM-FM-PH-1.5-520MC/S - £400. Racal/Dana 9084 SYN S/G AM-FM-PH-.001-104MC/S - £300.

MARCONI 2019A SYNTHESIZED SIGNAL GENERATORS -80KC/S-1040MC/S - AM-FM - £400 inc. instruction book tested

HP8444A Tracking Generator • 5-1300Mc/s - £450.

HP844A ADT 059 Tracking Gen 6-1500 Mc/s - £650. HP35601A Spectrum Anz Interface - £300. HP4953A Protocol Anz - 3400. HP8970A Noise Figure Meter + 346B Noise Head - £3k. HP8755A-B+C Scalar Network Anz PI - £250 + MF 180C -Heads 11664 Extra - £150 each.

Heads 11664 Extra - £150 each. HP37098 Constellation ANZ £1,000. FARNELL TVS70MKII PU 0-70V 10 amps - £150. MARCONI 6500 Network Scaler Anz - £500. Heads available to 40GHz many types in stock. Mixers are available forANZs to 60GHz.

Marconi TF2374 Zero Loss Probe - £200. Racal/Dana 1250-1261 Universal Switch Controller +

200Mc/s PI Cards and other types. Racal/Dana 9303 True RMS Levelmeter + Head - £450. TEKA6902A also A6902B Isolator - £300-£400.

TEK CT-5 High Current Transformer Probe - £250. HP Frequency comb generator type 8406 - £400. HP Sweep Oscillators type 8690 A+B + plug-ins from 20Mc/s to 18GHz also 18-40GHz. HP Network Analyser type 8407A + 8412A + 8601A

GHz - plus most other units and displays used in this

Racal/Dana 9301A-9302 RF millivoltmeter 15-2GH

Racal/Uana Modulation Meter Type 9009-9008 Racal/Dana Modulation Meter Type 9009-9008

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100Kc/s - 110Mc/s - £500 - £1000. HP 8410-A-B-C Network Analyser 110Mc/s to 12 GHz or 18

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Racal/Dana Modulation Meter Ty er9008-9608 - 814a/s -1.5GHz - £150/£250 - 90024 2550 Marconi Microwave 66000 1 straep.os., wainframe.eth 6650PI - 18-26.5 GHz or 6651 PI / 26.5-40GHz-£750 d - uor 600.0 MF only £20. Gould JSB test cacillator + manual - £150. Berr & Stroud Variable filter EF3 0.1Hz-100Kc/s + Jet Yoas + low pass - £160, other makes in stock. Racal/Dana 9300 RMS voltmeter - £250. HP 8760A storage normalizer - £400 with lead + S.A. or N. Marconi mod meters type TF2304 - £250 - TF2305 - £1,000 Racal/Dana counters-99904-9905-9905-9915-9919. 9921-500K-siGHz - £100 - £400 - all filtand with. #X

9921-50Mc/s-3GHz - £100 - £400 - all fitted with P

HP3455/3456A Digital voltmeter - £400. HP5370A Universal time interval counter

HP8699B Sweep PI YIG oscillator .01 MF-£250. Both £500.

HP8508A Vector voltmeter - £2500.

1.3SM - £500 + one PI.

1.3SM - £500 + one P.I. Anritsu MZ100A E/O Converter.

Light Source £350. Anritsu MZ118A O/E Converter

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standards. HP180TR. HP181T, HP182T — inframes £300 - 500. HP432A-435A or B-436A-point inters + pointerheads to 60GHz - £150 - £1750 - spare — or allable. HP36586A or C selective level meter - £500. HP8622A+B Sweep PI -01 -2.46Hz - ATT £1000 -£1250. HP86290A+B Sweep PI -1 16GHz - £1000 - £1250. HP86290C Mainframe - £250. IEEE £350. HP8155A Programmable signal source - 1MHz - 50Mc/s -£1k.

18GHz - microwave parts new and ex equipt - relays -attenuators - switches - waveguides - Yigs - SMA - APC7

Jugs - adaptors etc. qty, in stock. B&K Items in stock - ask for list. Power Supplies Heavy duty + bench in stock - Farnell - HP -Weir - Thurtby - Racal etc. Ask for list. Large quantity in stock, all types to 400 amp - 100Kv. HP8405A Vector voltmeter - late colour - £400.

Battery Pack MLS9A. Anritsu MW97A Pulse Eono Testec PI available - MH914C 1.3 - MH919B 1.3 - MH913B 0.85 -MH925A 1.3 - MH929A 1.55 - MH925A 1.3GI - MH914C

Anritsu MW98A Time Domain Reflector. Pl available - MH914C 1.3 - MH915B 1.3 - MH913B 0.85 -MH925A 1.3 - MH929A 1.55 - MH925A 1.3GI - MH914C

+ MG912B (LD 1.35) Light Source + MG92B (LD 0.85)

+MH922A 0.8 O/E unit + MH923 A1.3 O/E unit £350. Anritsu ML96B Power Meter & Charger £450.

£1k.

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2000 969

MARCONI 2022E SYNTHESIZED SIGNAL GENERATOR -10KC/S-1.01GHz AM-FM - £500 inc. Instruction book tested R&S APN 62 LF Sig Gen 0.1Hz - 260 kHz c/w book - £250.

MARCONI 2383 S.ANZ 100Hz - 4.2 GHz. £2K H.P RF AMP 8349A 2-20 GHz microwave. £2K H.P. RF AMP 8347A 100 kHz - 3GHz £1,500. H.P. 8922 radio communication test sets. G - H - M. options various. £2,000 - £3,000 each. H.P. 4193A VECTOR IMPEDANCE METER + probe kit. 400 kHz. To 110 ML/S. £3,500

SPECIAL OFFERS

H.P. 83220A – E GMS UNITS for above. £1,000 - £1,500. WAVETECK SCLUMBERGER 4031 RADIO COMMUNICATION TEST SET. Internal Spectrum ANZ. £2 000 £1 800 ANRITSU MS555A2 RADIO COMM ANZ. To 1000MC/S.

No C.R. tube in this model. £450. TEK 2445A – 4CH – 150MLS SCOPE + New X1 + X10-probe. Instruction book. £500 each.

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Johns Radio, Whitehall Works, 84 Whitehall Road East, Birkenshaw, Bradford BD11 2ER. Tel: (01274) 684007. Fax: 651160

NEWPRODUCTS

Please quote Electronics World when seeking further information

64-channel, 14-bit I/O board

Adept Scientific has announced the PCI-DAS64/M1/14 analogue and digital I/O board from Measurement Computing, formerly known as ComputerBoards. The plug-andplay board is a 64-channel. 14-bit 1MHz board at a price that is lower than many competitors' equivalent 12-bit boards, claimed the supplier. Prices for the PCI-DAS64/M1/14 start at £1750 excluding VAT. The board provides 64 single-ended, or 32 differential inputs (the input mode is softwareselectable), as well as 14-bit analogue inputs with a sample rate of 1MHz, 32 bits of digital I/O and one 16-bit downcounter. Analogue and digital

trigger levels and direction are also software-selectable. There are no switches, jumpers or potentiometers on the board. All board addresses, interrupt channels, etc., are set by the computer's plug-and-play software. Calibration is fully digital. Adept Scientific Tel: 01462 480055 www.adeptscience.co.uk

Low-dropout regulators for battery powered systems

Two micropower CMOS low dropout regulators (LDOS) for battery-powered applications are available from Micrel Semiconductor. The MIC5255 and MIC5256 are 150mA LDOs in SOT-23 packaging. In operation, the devices draw

90µA and 'zero' current in the off-mode. They also offer dropout voltage of 135mV at 150mA and load transient response output settles in less than 10us from a change in load. The MIC5255 features a noise bypass pin to further reduce the output noise to 30µV rms. The MIC5256 provides an error flag to indicate detection of an overcurrent, thermal shutdown, or dropout condition. Micrel Semiconductor Tel: 01635 524455 www.micrel.co.uk

DSP modules based on Xilinx Virtex 11 FPGAs

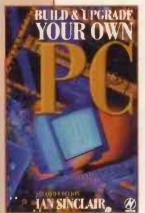
Building on the recent addition of FPGA modules to its Heron range for modular DSP, Hunt Engineering is offering two modules to use the Virtex II

FPGAs from Xilinx. HERON-FPGA3V has a Virtex II with 1 million gates, together with 90 digital I/O and serial options. HERON-IO2V has a Virtex II with a million gates plus two channels of 105Msample/s 12bit A-to-D converter and 2 channels of 125Msample/s 14bit D-to-A converter. The Virtex II architecture has been specifically designed for DSP applications. According to the supplier, these products are already being designed in to software radio type applications (where FPGA-based digital down conversion can be used to feed the C6000 with baseband only data), and also sonar, imaging and data acquisition systems. Hunt Engineering Tel: 01278 760188 www.hunteng.co.uk

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Claudia Colombini describes how to use a fieldprogrammable analogue array to implement a universal single-chip programmable tone detector for telecoms applications.

Universal tone decoder using an FPAA

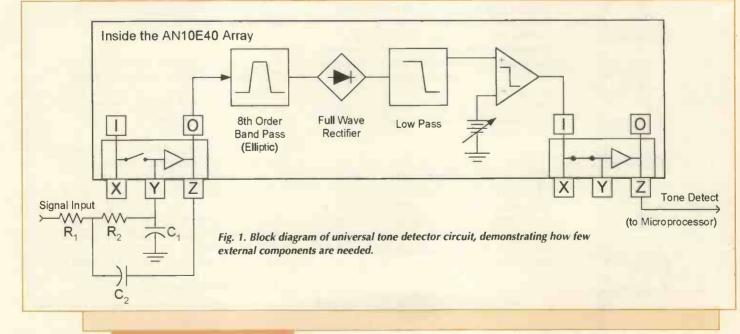
y article in last month's issue described the technology behind a new type of component on the market – the fieldprogrammable analogue array, or FPAA. These devices are intended to provide

analogue designers with the same level of in-system configuration flexibility as digital designers nowadays take for granted with FPGAs. This article describes how to implement a universal programmable tone detector, using just one FPAA.

The AN10E40 FPAA is a natural design platform for many of the elements used in telecommunications systems. The inherent flexibility of the device, combined with its excellent signal processing capabilities, allow it to implement up to 20th-order filters for example. Minimal design work is needed to create fully software programmable band-pass, low-pass, high-pass and band-stop filters. And all of the essential filter parameters – such as corner frequencies, Q and gain – are readily adjustable, without the need for any external passive components or complex and costly network tuning procedures.

Multi-system adaptability

In wired telecommunications systems – especially in public switched telephone networks, or PSTNs, both messaging and services information are passed using analogue signalling. Baseband voice, single-tone, multi-tone, or modulated signals (ASK, FSK, PSK, QAM) – each have their place in various systems around the world. Virtually every system employs a 'dial tone', such that



when a user lifts the handset, the telephone network sends out a dial tone to inform the user and all midstream equipment that the circuit is ready to accept dialling information.

The dial tone may be a continuous steady tone, or an on/off modulated tone. The goal of the receiving equipment at that point is to accurately detect the dial tone in strict conformance with the requirements of the local telephone network.

The different telephone networks around the world have differing dial tone and signalling requirements. Some of the parameters that change from region to region are tone frequency, frequency tolerance, amplitude level, and cadence timing if it is not a steady dial tone.

By using FPAA components in the design of telecom equipment, it is possible to adapt a single physical design to the specific requirements of unique PSTNs with simple reprogramming.

ETSI dial tone detection requirements

This article explains the detection of dial tones conforming with the specific requirements of the European telephone network. It goes on to explain how, with simple programmable circuit changes, the circuit can be adapted to detect other messaging information, such as the pay-phone identification tone (PIT) and the operator notification tone (ONT).

The European Telecommunications Standards Institute (ETSI, at www.etsi.org) has issued TBR21. This specification covers the requirements for attaching terminal equipment. In particular it sets forth the compliance parameters for 'automatic dialling functionality' (dialling with dial tone detection). The terminal must absolutely recognise a dial tone within the relatively large range of parameters given by:

Frequency (Hz)	Level (dBV)
300 to 500	-35.7 to -0.7

Furthermore, a valid dial tone may be steady or cadenced. The nominal valid cadence structure is 200ms on, 200ms off, 600ms on, 1000ms off, then repeated.

Implementation details

Design of a dial tone detector begins with a block diagram that conveniently translates directly to some of the analogue circuit functions – known as IPmodules. These modules are in the library that Anadigm supplies with its free PC-based CAD software, for use when configuring FPAA components. As shown in Fig. 1, the circuit comprises the following functions:

- An anti-aliasing input filter
- A band-pass filter eighth-order elliptic
- A full wave rectifier
- A low-pass low-Q filter
- A dual-input comparator
- A precision DC reference voltage
- A logic level output

Anti-aliasing input filter

The continuous low-pass anti-aliasing input filter is realised using a standard Sallen-Key topology. This is readily accommodated by the analogue I/O cells of the AN10E40 FPAA, as Fig. 2 shows.

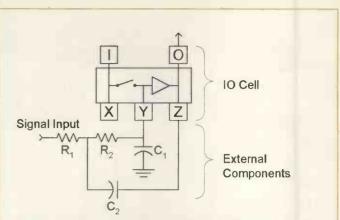


Fig. 2. Anti-aliasing input filter is a standard Sallen-Key type and readily implemented using analogue I/O cells of the FPAA.

The cut-off frequency for this low-pass anti-aliasing filter should be set close to the maximum frequency to be handled by the FPAA. This continuous time filter band limits the input signal well below the switching frequencies present in the subsequent sampled data system, preventing unwanted aliasing artifacts.

Only two external resistors and capacitors are needed to implement the filter. There is no specific need to maintain tight tolerances. The filter response may use either a Butterworth or Chebyshev filter approximation. The desired in-band attenuation for the Butterworth is less than 0.5dB, and for the Chebyshev less than 0.1dB ripple.

For the circuit shown, the following equations are easily worked out to yield a filter with the desired response:

Set the corner frequency:

$$F_c \ge \frac{Flat_bana}{0.55}$$

Here, $Flat_band$ is 500Hz and F_c is 909.1Hz. Resistances R_1 , R_2 and R are equal. For Butterworth,

$$C_1 = C, C_2 = 2$$

For Chebyshev,

 $C_1 = C, C_2 = 2.355C$

C

Corner frequency is set by,

$$F_c = \frac{1}{2\pi R \sqrt{C_1 C_2}}$$

A quick bit of algebra, keeping common component values in mind, yields the following suitable selections:

Butterwo	rth		
R ₁	R ₂	C1	C ₂
12400Ω	12400Ω	10.0nF	20.0nF
Chebysh	ev		

Eighth-order band-pass filter

The second signal processing block to implement is an 8th order band-pass filter. Higher-order filters are often frustrating to build using more conventional components. However, this function is easily realised in

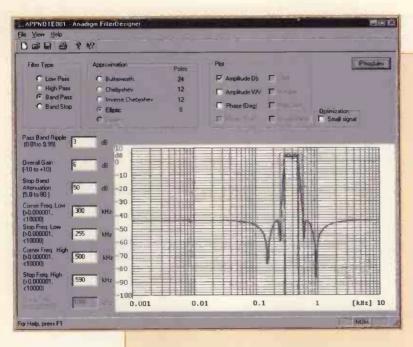


Fig. 3. Screen shot of Anadigm's FilterDesigner software. an FPAA by cascading four high-Q bi-quad band-stop filters.

The desired total filter specification is given by:

Pass band: 300Hz to 500Hz, 3dB maximum ripple Stop band: ≤255Hz and ≥590Hz, >50dB attenuation

Some ripple in the pass band is perfectly acceptable for this application, provided that a valid dial tone is always detected. Allowing some ripple is consequently an easy trade-off to make, enabling construction of a filter with a response that is close to ideal.

There are plenty of text books around that attempt to explain filter design, but it is undeniably a complex

subject. However, Anadigm offers a filter synthesis tool that simplifies the process significantly.

Known as FilterDesigner, the tool is an extension to the FPAA configuration software. It allows you to create high-order filters by employing combinations of the standard bi-linear and bi-quad filter IPmodules from the FPAA's associated analogue function library.

By keying-in the above filter specification, you can obtain an accurate graphical representation of the filter's response, as shown in Fig. 3. For the purposes of example, I've chosen an elliptic filter, but there are no constraints placed on the user with regard to filter type. The IPmodules required to implement the circuit are:

The IPmodules required to implement the circuit are:

Filter No	F _o (Hz)	DC gain	High freq. gain	Q
1 - F08	346	0.097	0.471	8.93
2 - F08	433	2.270	0.471	8.93
3 - F08	303	0.317	0.471	28.5
4 - F08	495	0.702	0.471	28.5

To realise this tightly-specified filter network using the more conventional components on the market today, the choices are somewhat limited. Traditional op-amps or a switched-capacitor filter IC could be used, but both may require the use of precision external components.

Because the frequency tolerances are so tight, even with precision components it would be necessary to use a network analyser and trimming potentiometers to accurately fix the F_o , Q, and gain of each stage.

The only other option is the use of ultra-precision thick-film resistor networks with trimming. Either way, the conventional route costs time and money, and will still suffer from the effects of component ageing and thermal drift.

The AN10E40 FPAA, on the other hand, offers a

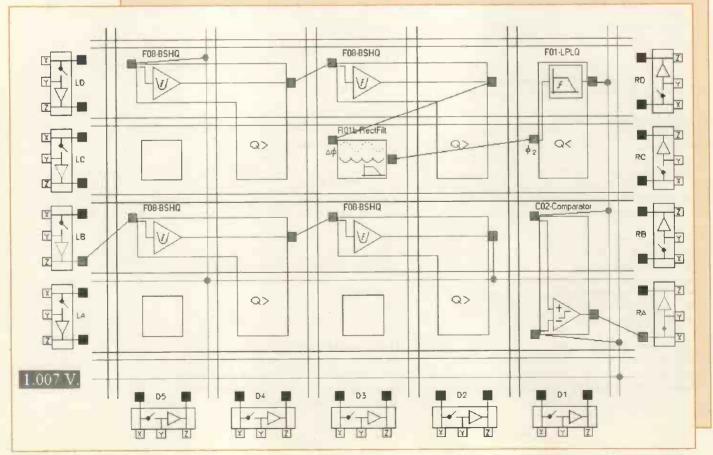


Fig. 4. Screen shotdeof the dial-tonetradetect circuitredesigned using thereFPAA's software.ex

List 1.

Report file for the dial-tone detect circuit.

solution to these problems. There
are no external passive component
procurement problems, no trimming
elements, no need to tune each
circuit produced, no component
ageing drift and no significant
thermal drift. And there is another
significant benefit – in-circuit
reconfigurability.

The full wave rectifier

After the filter, the next IPmodule placed is a simple full wave rectifier with its gain set to 4V/V. The default corner frequency is left unadjusted at 16.7kHz. Rectified dial tone is then passed on to the next stage.

Generating a very low frequency signal

Now that the dial tone is passed and rectified, the next job is to convert it to a nearly DC signal that can be compared to a reference. A low-pass bi-quad low-Q filter IPmodule is selected for this task.

Sample clock is 83.3kHz and F_{o} is set to 80Hz. Pass band gain is set to 2.3 and Q is 0.5879. Note that the realised value of any parameter specified within an IPmodule is a function of the sampling clock's frequency. For this particular design, 83.3kHz was a frequency already existing in the target system.

While 83.3kHz would usually be considered a bit low for a sampled data system operating in the audio band, in this particular instance it easily meets all the requirements: it is several times higher in frequency than the signal being processed, easily derived from the existing

system, and appropriate to achieving the specified parameters in each of the nominated IPmodules.

Creating a logic signal

Output from this low-pass filter is connected to the positive input of a comparator IPmodule. The negative input of the comparator is driven by the AN10E40 FPAA's built-in precision DC reference voltage source.

The output of the comparator switches between the supply rails, yielding a logic signal suitable for any family of logic.

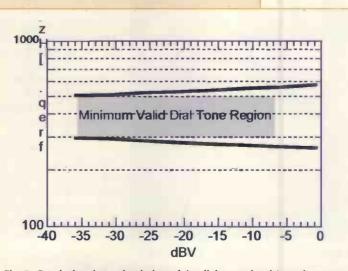
Tone type	Tone durations
Dial tone	Continuous
Dial tone	200ms on, 200ms off, 600ms on, 1s off
Busy tone	500ms on, 500ms off
Congestion tone	200ms on, 200ms off

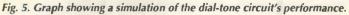
The logic signal is now easily monitored by a timer or generic I/O port of a microprocessor; by counting on/off times, it is possible to detect the unique PSTN control signals listed above.

Cell(B,5) - Anadigm A: (F08) Bar Clock Frequency:		d (High Q)		
*Center Freq (Fo) [kHz]		0.3460	Realized:	0.346
DC Cain	Desired:	0.0977	Realized:	
High Freq. Gain	Desired:		Realized:	
Quality factor (Q)			Realized:	
Cell(D,5) - Anadigm A: (F08) Bar		d (High Q)		
Clock Frequency:				
*Center Freq (Fo) [kHz]	Desired:	0.3030	Realized:	
DC Gain	Desired:	0.3170	Realized:	
High Freq. Gain	Desired:		Realized:	
Quality factor (Q)	Desired:	28.5000	Realized:	28.300
(all (B 2) Anadien A. (B02) Bar	d Cton Dimin	d (Wigh O)		
Cell(B,3) - Anadigm A: (F08) Bar Clock Frequency:		(Aign Q)		
*Center Freq (Fo) [kHz]		0 4330	Realized:	0.432
DC Gain	Desired:		Realized:	
High Freq. Gain			Realized:	
Quality factor (Q)		8.9300	Realized:	
gaarrey raccor (g,	DODLLCU.	0.9000		0.900
Cell(D,3) - Anadigm A: (F08) Bar	nd Stop Biqua	d (High Q)		
Clock Frequency:	83.333kHz			
*Center Freq (Fo) [kHz]	Desired:	0.4950	Realized:	0.495
DC Gain	Desired:	0.7020	Realized:	0.706
High Freq. Gain	Desired:	0.4710	Realized:	0.471
Quality factor (Q)			Realized:	
Cell(D,1) - Anadigm A: (F01) Low		(Low Q)		
	83.333kHz			
*Corner Freq (Fo) [kHz]				
Pass-Band Gain				
Quality factor (Q)	Desired:	0.5880	Realized:	0.594
Cell(B,1) - Anadigm A: (CO2) Dua Clock Frequency: 1		arator (Two	cells)	
	monting Dull	Mana Dasti	finn with T	De ee

Cell(C,3) - Anadigm A: (R01b) Inverting Full Wave Rectifier with Low Pass Filter Clock Fr

Clock Frequency:	83.333kHz				
*Corner Freq [kHz]	Desired:	16.7000	Realized:	16.700	
Pass-Band Gain	Desired:	4.0000	Realized:	4.000	





Circuit details and performance

Building the circuit using AnadigmDesigner software is simply a case of selecting the appropriate IPmodules from the library by 'drag and dropping' them onto the screen display of the FPAA's complete array, and then 'clickdragging' appropriate signal interconnects.

The final implementation of the tone detect circuit is shown in Fig. 4, which is a screen shot produced by the software. Figure 5 shows a plot of the data obtained from the actual circuit.

List 1 shows the accompanying report file, illustrating that the design goals were more than adequately satisfied. The ETSI standard requires that any tone on the phone circuit falling with the bounding box shown be recognised as a valid dial tone.

The upper and lower curves bound the actual region within which the circuit's logic output asserts, signalling a dial tone.

Factory or field reconfigurability

Once a particular line card or terminal has been designed using an FPAA, it is possible to adjust all of the signal processing parameters to meet the varying requirements of other PSTNs around the world. This is done with a quick and simple reconfiguration.

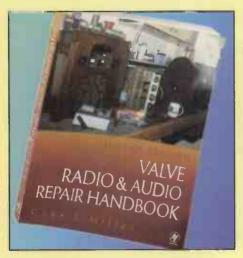
Users can elect to have the AN10E40 configure itself on

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power-up using data from a companion serial EPROM, or from a microprocessor. In the case of the former, to accommodate new regional requirements it would be necessary to insert a new EPROM on the board. This is probably more than adequate for many applications, but if the board already contains a microprocessor it can be used to facilitate an even more flexible solution, by enabling regionspecific configuration files to be downloaded to the FPAA.

Reconfiguring on the fly

Once the dial tone has been detected, there is no reason to ignore the FPAA and engage some other physical circuit. It takes less than 100μ s to reconfigure the AN10E40 for another task.

For example, once a valid dial tone has been detected, the FPAA could be sequentially reconfigured to generate key press tones, detect a pick-up, and then to pass on a previously digitised voice message.

Alternatively, immediately after dial-tone detect it could be reconfigured to a data access arrangement, or DAA, to facilitate modem communications. The only limit to this new form of analogue design is your imagination!

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For more details of this new version, see New Products, page 44

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Exploring real-time programming

Using a multi-tasking metronome as a design example, Tim Wilmshurst explains the ins and outs of real-time programming using a microcontroller. D res

esigners of embedded systems must understand the timing requirements of their target system, regardless of whether the system is large or small. They should also have at least a general appreciation of the principles of real time operation.

This electronic metronome has been designed to explore some of the issues relating to a simple real time system, and to illustrate how such a system can be achieved.

Real-time operating system

When confronted with the demands of real-time operation, many designers of embedded systems make use of a real-time operating system, or RTOS. This allows the programming needs to be achieved in an orderly manner, and leads to reliable software.

An important function of the RTOS is to ensure that tasks are scheduled according to their priority. However, the operating system comes with its own overheads; it can be expensive, it occupies valuable programme memory, and it can slow down programme operation.

Deciding whether to go for an RTOS or not depends mainly on the number and characteristics of the tasks. As a general guide, an RTOS should be considered if tasks are many, or if their timing demands are widely different. It should be possible to do without an RTOS if the tasks are few, and/or if they can readily be synchronised to each other.

When an RTOS is *not* used, the demands of real time still need to be understood, and means have to be found to structure the programme for successful operation. The beginner's approach – of setting the clock

What is 'real time?'

While many believe that a system working in 'real time' must be fast, this is not necessarily true. A real-time system is simply defined as one that must provide the correct results or outputs in time for the required deadlines.

Depending on the system, deadlines may be expressed in microseconds, or in days. Meeting deadlines may involve the ability to measure time, to generate time-based activity, or respond to external events occurring at unpredictable times. Some deadlines are fixed and immovable, while others may have some flexibility. Some are synchronised with each other, while others are asynchronous.

Most real-time systems involve multi-tasking. That is, they

must create the illusion of doing several things at the same time. Those 'things', distinct activities undertaken by the system, are called *tasks*.

Tasks may be long or short, they may be synchronised to each other, or asynchronous. They may be instigated by the processor, under its control, or be caused by external events.

The relative importance of tasks, in terms of successful system operation, may differ. In other words, they have different *priority*. Each task generally relates to one of the deadlines already mentioned. The process by which tasks are chosen to run, in a real time system, is called *scheduling*.

Cyclic scheduling

Two simple scheduling strategies, which can be applied without an RTOS, are shown in the diagram below. In each case there are four tasks, A, B, C and D

In cyclic scheduling, diagram a), tasks execute in turn, each one completing what it has to do before handing over to the next task. This is effectively a simple looping programme.

The rate that any one task receives attention depends on its duration, and the duration of all other tasks. This is often a disadvantage, as the rate is more or less uncontrolled, and it is difficult therefore to undertake time-based activity. If one task was for example to sample an incoming signal, it would be impossible to guarantee a stable sampling rate.

An advance on this is 'timed cyclic scheduling', diagram b). Now a regular clock 'tick' is set up. This is not to be confused with the clock oscillator; a typical tick rate might for example be once every millisecond.

Tasks execute once, in turn, every time the 'tick' occurs. The total time needed to execute all tasks must be less than the tick interval, and some idle time is now introduced to fill up the

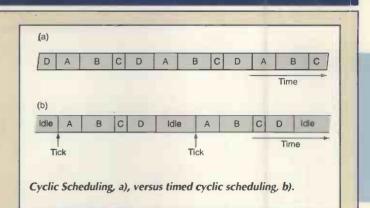
oscillator to the highest possible speed, and then hoping for the best - often does not work. What is needed is an understanding of what the tasks are, what are their timing demands, and how they relate to each other. A simple task scheduling strategy, like cyclic scheduling, can then be applied.

The metronome specification

This application is an example of a simple design that applies timed cyclic scheduling. It gives out a regular beat, at rates from 40 to 199 beats per minute. This represents the first task, which I will call 'Task 1'.

240

7



spare time between ticks. Now the repetition rate of each task is predictable, and with a reliable clock tick, timed activity can readily be carried out. Such timed activity can occur at every clock tick, or at multiples of the tick period.

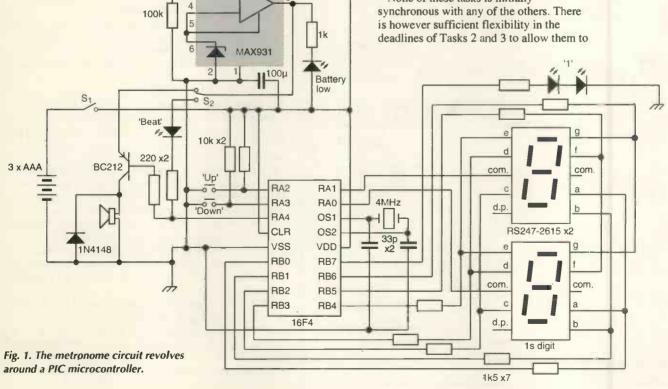
For a given beat rate, its deadline is rigid. The beat rate is shown by two multiplexed seven-segment led displays, and a further 'l' digit, represented by two leds. The displays are driven in turn by the same

microcontroller port bits, and must be alternated sufficiently fast that the eye does not perceive any flicker. This represents the second task - 'Task 2'. There is some flexibility in its deadline, as the eye is fairly tolerant of some variation in repetition rate in such displays.

The beat rate is adjusted by two push buttons. One increases the rate while the other decreases it. The beat output must continue uninterrupted while it is being

adjusted. This represents the third task -'Task 3'. Again there is some flexibility in its deadline, as the human user will barely perceive a delay of a few milliseconds in response.

None of these tasks is initially synchronous with any of the others. There is however sufficient flexibility in the deadlines of Tasks 2 and 3 to allow them to



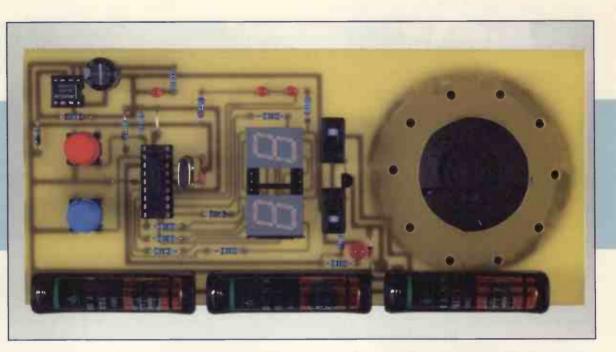


Fig. 2. Metronome constructed on standalone PCB.

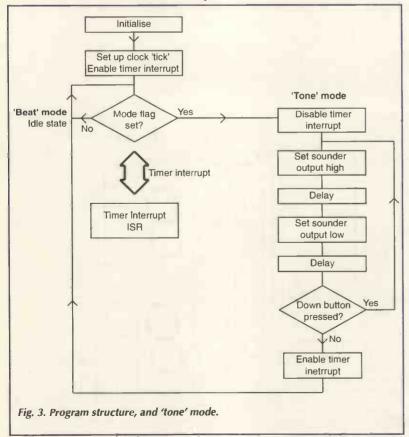
be made synchronous. This simplifies the programme design considerably.

All integer beat rates within the specified range must be possible. As the rate changes, the display is updated. The beat is caused by a nominal 10ms pulse from a port bit to a sounder, loudspeaker, or light-emitting diode.

The beat must continue at the displayed rate, whatever else the metronome is doing. It is also possible to place the metronome in a mode in which it outputs, for tuning purposes, the note 'Concert A'.

The hardware

The circuit diagram is shown in Fig. 1. It is designed around a Microchip PIC 16F84 microcontroller¹.



To save control lines, the display digits are multiplexed. That is, they are activated in turn, at a speed fast enough that the eye perceives them as both being continuously on.

Port B drives the seven segments of the display, and the '1' digit, while bits 0 and 1 of Port A control the common cathodes of the digits. A seven segment digit is illuminated when its common cathode connection is at logic low, and the required pattern of its segment lines – i.e. bits 0 to 6 of Port B – are high.

The 'up' and 'down' buttons, which change the beat rate, are connected to bits 2 and 3 of Port A. The beat output is activated by a logic low on Port A bit 4, while a slide switch determines whether led or sounder is to be active.

Power is supplied from three AAA cells in series. The battery voltage is not regulated, but is monitored via a MAX931 comparator plus reference combination. The low power led – labelled 'lo bat' – is designed to illuminate when the supply voltage drops to 4V. The oscillator frequency is set by a 4MHz crystal.

All leds are RS 588-386 types, except for 'beat', which is standard size, 10mA forward current. The sevensegment displays are common cathode types.

The circuit has been built on a single pcb, pictured in Fig. 2.

Creating the software

A programme overview appears in Fig. 3. First comes initialisation, and setting up of the clock 'Tick', based on the timer 'interrupt on overflow', as explained later. After that, the programme enters an idle state.

From here, driven repetitively by the clock tick, the programme executes the timer interrupt service routine, ISR, which contains the three tasks of beat mode. This implements the principle of timed cyclic scheduling.

Alternatively, if the 'mode' flag has been set – caused by both buttons being pressed simultaneously – the programme enters the tone mode, generating concert A at 440Hz through a timed loop. A return to the idle state, and re-enabling of the Timer interrupt, occurs if the Down button is pressed.

The timer interrupt ISR used in beat mode follows the flow diagram of Fig. 4. This ISR occurs on every clock tick, and the tasks performed are all timed to take a certain number of clock ticks, or to occur after a certain number of clock ticks.

The occurrence of each is determined by the state of an

What is 'interrupt-on-overflow

The simplified block diagram of almost any microcontroller counter/timer is shown below. Central to the module is a digital up-counter, which can be read via the data bus.

Input to the counter can be an external source. The counter is then normally used simply as a counter, e.g. to count events or objects. Alternatively, it can be the internal oscillator. In this case the counter is then used as a timer, as the clock period is known and stable.

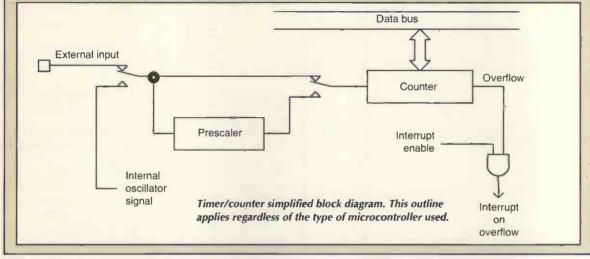
The incoming signal may also be divided down by a prescaler, which can typically be set to divide by binary powers, for example 2, 8, 16. When the Counter reaches its maximum value, and then overflows, an overflow output is generated which can be used as an interrupt source.

With a stable counter input frequency, a regular interrupt is achieved. Mathematically speaking,

$$f_{\rm inv} = \frac{J}{2^n \times 2^p} \tag{2}$$

where f_{int} is the interrupt frequency and f is the internal oscillator frequency. The counter has n bits, and the prescaler divides by 2^{p} .

In the 16F84 controller, the 'internal oscillator signal' is the clock oscillator frequency divided by four, and the counter/timer is eight bits, i.e. *n* is 8.



associated counter, in practice a memory location. These each count down every clock tick from a value preset in them, and trigger activity when they reach zero. They are:

period_counterdetermines beat period (initial value
dependent on beat setting)sounder_counterdetermines duration of sounder/led
beat pulse (initial value fixed)display_counterdetermines duration of display of
multiplexed digit (fixed)button_counterdetermines interval at which buttons
are polled (fixed)

The main requirement of Task 1 is to decrement period_counter, and activate the sounder if the counter reaches zero. If it has reached zero, it is necessary to reload the counter. The new value of beat period is stored in next_period, which may have been changed by the user (Task 3) since the previous beat.

Task 1 starts out by testing whether the sounder needs to be deactivated, by decrementing sounder_counter and testing for zero.

Task 2 decrements display_counter, and changes the active digit if the counter has reached zero. Task 3 decrements button_counter. If it reaches zero, it checks if either of the buttons are being pressed. If they are, then the beat rate is changed accordingly, and the value of next_period is updated.

If both buttons are simultaneously pressed, then the mode flag is set, which will cause a change to Tone mode when the idle state is reached.

The metronome actually displays the beat rate, while the programme itself requires the beat period, expressed in

number of tick periods. The value of **next_period** is derived according to:

$$next_period = \frac{00}{(beat rate \times tick period)}$$
(1)

In an eight-bit microcontroller, this has the potential to require a fairly lengthy piece of processing, which runs the risk of taking excessive time. As a result, I used a look-up table, written using a C program, which was used to derive the **next_period** values.

The table requires two bytes for each of its (199-40) values, and therefore crosses page boundaries in the PIC programme memory. Standard recommended techniques¹ for accessing tables of this length must be applied, and are seen within the programme listing.

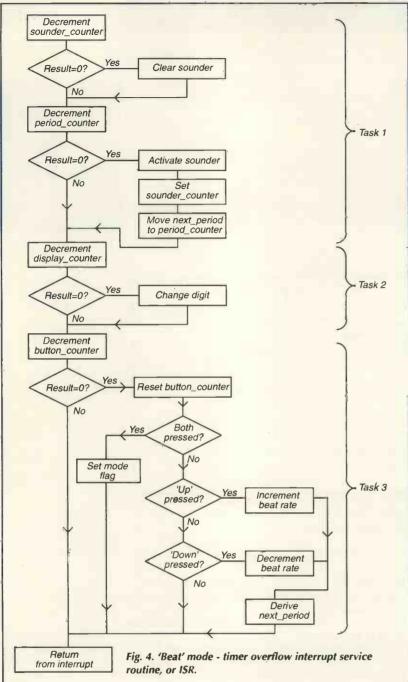
A complete programme listing, with detailed commenting, may be downloaded from the web site of reference 2.

Setting up the clock tick

A fundamental decision in this type of programming is choosing the clock tick repetition rate. Clearly it must be long enough to accommodate execution of all tasks occurring within its period. Furthermore, it will govern resolution of all timed activity depending on it.

To clarify timing demands for the metronome, I explored the beat period requirements. The extremes of the highest and lowest beat rates are shown in **Table 1**. You can see that the interval between beats ranges from around 300ms to 1.5s.

A trial tick period of 0.5ms was then considered, as shown in the Table. At the slowest beat rate, the beat duration will consist of 3000 clock ticks, at the highest 603.



Several beat periods based on this tick rate were calculated, as shown in the column entitled, 'Resulting beat rate'. This column illustrates that this technique leads to good beat rate accuracy. This is no longer the case however if you increase the tick period to 1ms.

The clock tick is derived by using the Interrupt on Overflow facility of the 16F84 Counter/Timer ("TIMER0") module, as explained in the accompanying panel. In this design a 4MHz clock oscillator crystal was used. Applying formula (2), and setting n to 8, it was found that a 0.512ms tick period could be derived if the prescaler was set to divide by 2. This led to accurate results.

It is essential in this form of programme structure, Fig. b) in the 'Cyclic scheduling' panel, to ensure that there is no chance of the tasks over-running the time available between clock ticks. While this may not occur under normal programme operation, it is very important to

	timing demands		
Beat rate	Beat period	No of ticks	Resulting beat rat
40/min	1.5000 s	3000	40.000
41	1.4634	2927	40.998
42	1.4286	2857	42.002
43	1.3953		
197	304.57 ms	609	197.04
198	303.03	606	198.02
199	301.51	603	199.00

consider carefully whether there is a situation when it can. In this programme, the worst case occurs when the contents of period_counter, sounder_counter, display_counter, and button_counter all decrement to zero on the same clock tick, and at the same time the user is demanding a change of beat setting which causes BCD digit overflow (for example from 99 to 100). This circumstance in the Timer Overflow ISR can be simulated using the simulator in MPLAB, the Microchip Integrated Design Environment. Alternatively, it can be determined by careful addition of all instruction durations in the worst case execution path. By doing this the worst case ISR duration was found to be 105 instruction cycles, i.e. 105mµ for our 4MHz clock frequency, implying the idle time is always greater than 400mµ. It may be concluded that there is no apparent risk to reliable operation of the Timed Cyclic Scheduling.

Testing and evaluation

The metronome has overall been found to work reliably and well. Beat rates have all proved to be accurate. The beat and display respond smoothly to changes in settings. The generated "Concert A" tone was measured at 439.9493Hz. The power down led comes on reliably at 4V, although the circuit goes on functioning, more or less, down to a supply of 1.8V.

Further information and background on the design techniques described in this article may be found in reference 3.

Finally, Many thanks to Trevor Noble, who quickly and skillfully built the several metronome versions.

References

- http://www.microchip.com/10/Lit/PICmicro/16f8x/index.htm
 http://computing
 - technology.derby.ac.uk/index.php?node=10348
- Wilmshurst T., An Introduction to the Design of Small-Scale Embedded Systems, Palgrave Publishers, ISBN 0-333-92994-;

tone.	he electronic metronome, which also generates a concert A	;initia	mc
;Config Word:	HS oscillator, WDT off,	; INILIA	1 V8
:	power-up timer on, code protect off		mo
Clock freg 4MHz	approx (Crystal osc.)		mo
;Port A 4	beat (op)		mo
; 3	"down" button (ip)		mo
; 2	"up" button (ip)		mc
; 1	Common cathode, ms digit (op)		mc
; 0	Common cathode, 1s digit (op)		;b
;Port B 6-1	Display segments (all op)		bc
;	6=g, 5=f, 4=e, 3=d, 2=c, 1=b, 0=a		bc
; 7	"1" digit		mo
;7-Segment bit p			mc
; Displaye	ed No Port B pattern		mc
; 0	0011 1111=3f		mc
; 1	0000 0110=06		mc
; 2	0101 1011=5b		mo
; 3	0100 1111=4f	;set tim	
; 4	0110 0110=66		bs
	0110 1101=6d		mc
; 6	0111 1101=7d 0000 0111=07		mo
; 8			bc
; 9	0111 1111≃7f 0110 1111≃6f		bs
; A	0110 0111=81		bc bs
:	VIII VIII-//		DE
Define RAM locat	cions	wait	bt
	10 ;used in delay SRs	n ot a to	go
	11 ; " " " "		30
	ions hold time durations, all measured in	;here if	E er
units of ticks		;Aim for	
	12 ;holds beat period, hi byte	tone ger	
	13 ;holds beat period, lo byte		bs
	14 ;holds next beat prd, hi byte		mo
next_prd_lo equ	15 ;holds next beat prd, lo byte		mo
digit_cntr equ	16 ;decrements every tick, digit changed on		bc
zero			bs
	17 ;decrements every tick, buttons checked on	; wait fo	
zero		tgl	bt
	18 ;decrements every tick, sounder cleared on		go
zero		;now set	
	relate to beat rate, and display	tg2	mc
	19 ;holds (BCD) value of ms digit	t = 2	mor
	1a ;holds (BCD) value of 1s digit	tg3	nop
parallel to BCD	20 ; digital value of beat rate, runs in		nop
	21 ;holds address of "table2" look-up		dec
	22 ;various flags		got bc
	0 ;ms "one" of display		no
	1, ;next value of ms "one" of display		no
digit equ	2 ; current displayed digit, 0 = 1s digit is		no
displayed			no
mode equ	3 ;0 = beat, 1 = tone		;1
;Some constants			mo
digit_durn equ d'	20' ; duration of each digit illumination		mo
	1'200' ;period between button checks	tg4	no
sounder_durn equ	d'05' ;duration of beat led/sounder		no
org 00			de
goto star			go
org 04	;here if timer has overflowed		bs
goto act	lon		no
-			no
org 0010	1 **************		bt
org 0010 ;Configure System			go
org 0010 ;Configure System ;set port bits	totus you galact back t		;1 bs
org 0010 ;Configure System ;set port bits start bsf s	tatus,rp0 ;select bank 1		
org 0010 ;Configure System ;set port bits start bsf s movlw 0		tas	
org 0010 ;Configure System ;set port bits start bsf s movlw 0	crisa (all porta bits input	tg5 otherwig	bt
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t	crisa (all porta bits input ;except 2&3	tg5 otherwis	bt Ie
org 0010 ;Configure System ;set port bits start bsf s movlw 00 movwf t movlw	crisa ₍ all porta bits input ;except 2&3 00	-	bt le go
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t movlw t	erisberta bits input ;except 2&3 ;isberta bits output	-	bt ie go bc
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t movlw t	c all porta bits input ;except 2&3 00 risb ;all portb bits output status,rp0 ;select bank 0	-	bt go bc bs
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t movvwf t bcf s movlw	c all porta bits input ;except 2&3 00 risb ;all portb bits output status,rp0 ;select bank 0	-	bt go bc bs go
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t movvwf t bcf s movlw	action of the set of t	otherwis	bt go bc bs go ver
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t bcf s movlw movwf t bcf s movlw movwf movwf	action of the second se	otherwis ;Timer C	bt go bc go go ver de
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t bcf s movlw movwf t bcf s movlw movwf movwf	<pre>de call porta bits input ;except 2&3 00 crisb ;all portb bits output status,rp0 ;select bank 0 00 ;set up initial port output values portb 1f</pre>	otherwis ;Timer C	bt go bc bs go ver go
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t bcf s movlw movwf movlw movwf movlw movlw movlw	<pre>de call porta bits input ;except 2&3 00 crisb ;all portb bits output status,rp0 ;select bank 0 00 ;set up initial port output values portb 1f</pre>	otherwis ;Timer C action	bt go bc go ver de go
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t bcf s movlw movwf movwf gdiagnostic ; bcf	all porta bits input ;except 2&3 00 rrisb ;all portb bits output status,rp0 ;select bank 0 00 ;set up initial port output values portb 1f porta	otherwis ;Timer C action	bt go bc bs go ver de go bs bs
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t bcf s movlw movwf movwf diagnostic ; bcf ; call	<pre>content of the second sec</pre>	otherwis ;Timer C action ;clear s	bt go bc go ver de go bs: th
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t bcf s movlw movwf movwf diagnostic ; bcf ; call	<pre>de carisa {all porta bits input ;except 2&3 00 crisb ;all portb bits output ttatus,rp0 ;select bank 0 00 ;set up initial port output values portb 1f porta portb,7 delay200 portb,7</pre>	otherwis ;Timer O action ;clear s ;decreme	bt go bc go ver de go bs nt
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t bcf s movlw movwf tbcf s movlw movwf ;diagnostic ; bcf ; call ; bsf ; call del:	<pre>de carisa {all porta bits input ;except 2&3 00 crisb ;all portb bits output ttatus,rp0 ;select bank 0 00 ;set up initial port output values portb 1f porta portb,7 delay200 portb,7</pre>	otherwis ;Timer O action ;clear s ;decreme	bt go bc go ver de go our bs ent mo sul
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t bcf s movlw movwf tbcf s movlw movwf ;diagnostic ; bcf ; call ; bsf ; call del:	<pre>de carisa {all porta bits input ;except 2&3 00 crisb ;all portb bits output status,rp0 ;select bank 0 00 ;set up initial port output values portb 1f porta portb,7 delay200 portb,7 ay200</pre>	otherwis ;Timer O action ;clear s ;decreme	bt go bc go ver de go our bs mo sul bt
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t bcf s movlw movwf tbcf s movlw movwf ;diagnostic ; bcf ; call ; bsf ; call del:	<pre>de crisa {all porta bits input ;except 2&3 00 rrisb ;all portb bits output status,rp0 ;select bank 0 00 ;set up initial port output values portb 1f porta portb,7 delay200 portb,7 ay200 portb,7 ay200</pre>	otherwis ;Timer O action ;clear s ;decreme	bt go bc go ver go oun bs soun bs sul bt:
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t bcf s movlw movwf diagnostic ; bcf ; call ; bsf ; call del;	<pre>de risa {all porta bits input ; except 2&3 00 risb ;all portb bits output ttatus,rp0 ; select bank 0 00 ; set up initial port output values portb 1f porta portb,7 delay200 portb,7 ay200 portb,7 ay200 portb,7 ess for registers</pre>	<pre>otherwis ;Timer O action ;clear s ;decreme action1</pre>	bt go bc go ver de go soun bs ent mo sul bt
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t bcf s movlw movwf diagnostic ; bcf ; call ; bsf ; call del ; bcf ; call del ; bcf	<pre>de risa {all porta bits input ; except 2&3 00 risb ;all portb bits output ttatus,rp0 ; select bank 0 00 ; set up initial port output values portb 1f porta portb,7 delay200 portb,7 ay200 portb,7 ay200 portb,7 ess for registers</pre>	otherwis ;Timer O action ;clear s ;decreme action1 higher	bt go bc bs go ver de go soun bs ent mo sul bt de
org 0010 ;Configure System ;set port bits start bsf s movwf t bcf s movlw movwf tbcf s movlw movwf ;diagnostic ; call ; bsf ; call del ; bcf ; call del ; bcf ; call del ; bcf	<pre>de risa {all porta bits input ;except 2&3 00 risb ;all portb bits output status,rp0 ;select bank 0 00 ;set up initial port output values portb 1f porta portb,7 delay200 portb,7 ay200 portb,7 ress for registers portal operation</pre>	otherwis ;Timer C action ;clear s ;decreme action1 higher ;byte sh	bt go bc go ver de go sour bs sub bt de oul t f
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t bcf s movlw movwf diagnostic ; bcf ; call ; bsf ; call del ; bsf ; call del ; bcf ; call del ; bcf	<pre>de carisa call porta bits input ;except 2&3 00 rrisb ;all portb bits output status,rp0 ;select bank 0 00 ;set up initial port output values portb 1f porta portb,7 delay200 portb,7 ay200 portb,7 if es for registers rmal operation digit_durn</pre>	otherwis ;Timer C action ;clear s ;decreme action1 higher ;byte sh	bt go bc go over de go bs ent mo sul bt de de de t f t f
org 0010 ;Configure System ;set port bits start bsf s movlw 0 movwf t bcf s movlw movwf ;diagnostic ; call ; bcf ; call del ; bcf ; call del ; bcf ; call del ; bcf	<pre>de carisa call porta bits input carisa call porta bits input carise care care care care care care care car</pre>	otherwis ;Timer C action ;clear s ;decreme action1 higher ;byte sh	bt go bc bs go ver de go soun bs ent mo sul bt: de coun

```
f
     sounder cntr
les of variables
iod counters
    0a1
                       ;prd for 60bpm
tut.
f
    prd_cntr_lo
f
    next_prd_lo
    07
    prd cntr hi
f
    next prd hi
f
ts per minute and display counters
    flags, one
    flags, mode
    hi digit val
f
    00
f
    lo_digit_val
    d' 60'
    beat_val_bin
f
terrupt
    status, rp0
    b'11000000' ;set up timer, prescaler=2
    option_reg
    status, rp0 ; select bank 0
    intcon,t0ie ; enable timer overflow int
    intcon,t0if ; clear any pending timing int
    intcon, gie ; enable global int
    flags, mode
             ; wait for next overflow interrupt
    wait
              ; if in beat mode
ring tone mode. Concert A has prd 2.2727272ms.
instruction cycles, giving freq of 439.947Hz.
    intcon,t0ie ; disable timer overflow int
    porta,4 ;clear sounder
    77
             ;display A
   portb
    porta,0
    porta,1
ease of down button, which will cause mode exit
   porta,3 ;"down" button pressed?
    tq1
              ;yes
 running
  d' 226'
             :226x5 = 1130
   delcntr1
              ;5 cycles in single loop
              ;1129 total
z delcntr1,1
    tq3
    porta,4
cycles to here
   a'226' ;226x5 = 1130
delcntr1
             ;5 cycles in single loop
             ;1129 total
z delcntr1.1
    tq4
    porta,4
    porta,3 ;exit button pressed?
 tg2;no, so continue
cycles in this half, total of 2273
    porta,0 ;clear displayed "A'
    porta, 3 ; wait for exit button to be cleared,
             ;beat is immediately decremented
    tq5
    flags, mode
    intcon,t0ie ; enable timer overflow int
wait ; beat mode will clear other conditions
ow Interrupt Routine (where all the action is)
z sounder_cntr
   action1
    porta,4
riod count, emit beat if 0
    1
    prd_cntr_lo,1
   status,0 ;skip if no borrow, ie C is 1
prd_cntr_hi,1 ;borrow, underflow of this
never happen (zero condition detected first)
zero
   prd_cntr_lo
    action2
   prd_cntr_hi
   action2
```

	the second se	
	;here if period co	ount is zero
		porta,4 ; initiate beat
		sounder_durn ;set sounder counter
		sounder cntr
		period counter
		next prd hi
		prd cntr hi
7		next_prd_lo
J	movwf	prd_cntr_lo
	action2 decfsz	digit_cntr ;decrement digit counter
		action3
	;here if digit com	unter is zero, so change displayed digit
		porta,0 ;first switch off both digits
		porta,1
		flags, digit
l		action21
		laying 1s digit, change to ms digit
		hi_digit_val
		table_dig ;get requd bit pattern
1		portb
7		porta,1 ;enable that digit flags,digit
		action22
		laying ms digit, change to ls digit
	action21 movfw	
		table dig ;get regud bit pattern
		portb
		porta,0
		flags, digit
		flags, one
		portb,7 ;set ms "one" (which was cleared
		;when new pattern was written to port b)
1		digit_durn ;update digit counter
		digit_cntr
		tton counter, and test buttons if time
	action3 decfsz	may a second sec
	5	action4
		check buttons, first update button counter button durn
		button_cntr
		ttons, ie mode change
		porta,2 ; "up" button pressed?
		action30 ; no
		porta, 3 ;"down" button pressed?
d		action30 ;no
- 1		
1	;here if both but	tons pressed, ie mode change called
1	bsf	flags, mode
	bsf goto	flags, mode action4
	bsf goto ;test for	flags,mode action4 : single buttons
	bsf goto ;test for action30 btfss	flags,mode action4 s single buttons porta,2 ;"up" button pressed?
	bsf goto ;test for action30 btfss goto	flags,mode action4 r single buttons porta,2 ;"up" button pressed? action31 ;yes
	bsf goto ;test for action30 btfss goto btfss	<pre>flags,mode action4 r single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed?</pre>
	bsf goto ;test for action30 btfss goto btfss goto	<pre>flags,mode action4 c single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes</pre>
	bsf goto ;test for action30 btfss goto btfss goto goto	<pre>flags,mode action4 r single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed</pre>
	bsf goto ;test for action30 btfss goto btfss goto goto ;here if "up" but	<pre>flags,mode action4 r single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw	<pre>flags,mode action4 c single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed ton pressed</pre>
	bsf goto ;test for action30 btfss goto btfss goto goto ;here if "up" but action31 movlw subwf	<pre>flags,mode action4 r single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed ton pressed d'199' ;test for max value</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment	<pre>flags,mode action4 r single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed ton pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf	<pre>flags,mode action4 r single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf	<pre>flags,mode action4 cr single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed ton pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version</pre>
	bsf goto ;test for action30 btfss goto btfss goto goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw	<pre>flags,mode action4 r single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed ton pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf movlw subwf	<pre>flags,mode action4 c single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed ton pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf movlw subwf bz	<pre>flags,mode action4 r single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed ton pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf movlw subwf bnz clrf	<pre>flags,mode action4 c single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed ton pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w</pre>
	bsf goto ;test for action30 btfss goto btfss goto goto ;here if "up" but action31 movlw subwf bz increment incf movlw subwf bnz clrf incf	<pre>flags,mode action4 r single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed ton pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf bnz clrf incf movlw	<pre>flags,mode action4 cr single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed ton pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val, here if overflow hi_digit_val</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf bnz clrf incf incf movlw subwf	<pre>flags,mode action4 c single buttons porta,2;"up" button pressed? action31 ;yes porta,3;"down" button pressed? action32 ;yes action4 ;next if neither button pressed ton pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val d'10'</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf	<pre>flags,mode action4 cr single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val,w action33 hi_digit_val ;here if overflow</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf movlw subwf bnz clrf incf movlw subwf bnz clrf	<pre>flags,mode action4 c single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed ton pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val,w action33 hi_digit_val ;here if overflow flags,one ;(earlier test assures no</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw subwf bnz clrf incf movlw subwf bnz clrf bnz clrf baf	<pre>flags,mode action4 cr single buttons porta,2;"up" button pressed? action31 ;yes porta,3;"down" button pressed? action32 ;yes action4 ;next if neither button pressed ton pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val d'10' hi_digit_val ;here if overflow flags,one ;(earlier test assures no ;overflow beyond 199)</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf incf bnz clrf incf incf incf bnz clrf bsf bsf	<pre>flags,mode action4 cr single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val,w action33 hi_digit_val ;here if overflow flags,one ;(earlier test assures no ;overflow beyond 199) action33</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf movlw subwf	<pre>flags,mode action4 cr single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val,w action33 hi_digit_val ;here if overflow flags,one ;(earlier test assures no ;overflow beyond 199) action33 utton pressed</pre>
	bsf goto ;test for action30 btfss goto btfss goto goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf movlw	<pre>flags,mode action4 cr single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val,w action33 hi_digit_val ;here if overflow flags,one ;(earlier test assures no ;overflow beyond 199) action33 utton pressed d'40' ;test for min value</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw subwf bnz clrf incf movlw subwf bnz clrf bf goto ;here if "down" b	<pre>flags,mode action4 cr single buttons porta,2;"up" button pressed? action31 ;yes porta,3;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val,w action33 hi_digit_val ;here if overflow flags,one ;(earlier test assures no ;overflow beyond 199) action33 utton pressed d'40' ;test for min value beat_val_bin,w</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw subwf bnz clrf incf movlw subwf bnz clrf baf goto ;here if "down" b action32 movlw subwf bz	<pre>flags,mode action4 cr single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val,w action33 hi_digit_val ;here if overflow flags,one ;(earlier test assures no ;overflow beyond 199) action33 utton pressed d'40' ;test for min value</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf incf solwf bnz clrf incf incf incf incf solwf bz clrf incf incf movlw subwf bz clrf bsf bz clrf bsf bz clrf bsf bz clrf bsf bz clrf bsf bz clrf bsf bz clrf bsf bz clrf bsf	<pre>flags,mode action4 cr single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val,w action33 hi_digit_val ;here if overflow flags,one ;(earlier test assures no ;overflow beyond 199) action33 utton pressed d'40' ;test for min value beat_val_bin,w action4 ;cannot go under 40, so must not</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf movlw subwf bz clrf incf movlw subwf bz clrf incf movlw subwf bz clrf incf movlw subwf bz clrf incf movlw subwf bz clrf incf movlw subwf bz clrf incf movlw subwf bz clrf incf movlw subwf bz clrf incf	<pre>flags,mode action4 cr single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val d'10' hi_digit_val ;here if overflow flags,one ;(earlier test assures no ;overflow beyond 199) action33 utton pressed d'40' ;test for min value beat_val_bin,w action4 ;cannot go under 40, so must not beat_val_bin,1 ;decrement digital version</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw subwf bnz clrf bnz clrf bsf goto ;here if "down" b action32 movlw subwf bz decrement decf decf	<pre>flags,mode action4 cr single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val,w action33 hi_digit_val ;here if overflow flags,one ;(earlier test assures no ;overflow beyond 199) action33 utton pressed d'40' ;test for min value beat_val_bin,w action4 ;cannot go under 40, so must not</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw subwf bnz clrf bnz clrf bsf goto ;here if "down" b action32 movlw subwf bz decrement decf decf	<pre>flags,mode action4 cr single buttons porta,2;"up" button pressed? action31 ;yes porta,3;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val,w action33 hi_digit_val ;here if overflow flags,one _;(earlier test assures no ;overflow beyond 199) action33 utton pressed d'40';test for min value beat_val_bin,w action4;cannot go under 40, so must not beat_val_bin,1;and decrement BCD version lo_digit_val,1;and decrement BCD version</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf incf incf bnz clrf incf bsf bnz clrf bsf bsf goto ;here if "down" b action32 movlw subwf bz decrement decf btfss inspecting meb	<pre>flags,mode action4 cr single buttons porta,2;"up" button pressed? action31 ;yes porta,3;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val,w action33 hi_digit_val ;here if overflow flags,one _;(earlier test assures no ;overflow beyond 199) action33 utton pressed d'40';test for min value beat_val_bin,w action4;cannot go under 40, so must not beat_val_bin,1;and decrement BCD version lo_digit_val,1;and decrement BCD version</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf movlw subwf bz clrf incf movlw subwf bz clrf incf movlw subwf bz clrf incf incf incf incf joto ;here if "down" b action32 movlw subwf bz decrement decf decf btfss inspecting meb goto ;underflowed, so	<pre>flags,mode action4 cr single buttons porta,2;"up" button pressed? action31 ;yes porta,3;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val,w action33 uton pressed d'40' ;test for min value beat_val_bin,w action4 ;cannot go under 40, so must not beat_val_bin,1 ;and decrement BCD version lo_digit_val,7 ;test for underflow preset this digit and decrement next</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw subwf bnz clrf bnc f goto ;here if "down" b action32 movlw subwf bz decrement decf decf btfss inspecting mab goto ;underflowed, so movlw	<pre>flags,mode action4 cr single buttons porta,2;"up" button pressed? action31 ;yes porta,3;"down" button pressed? action32 ;yes action4 ;next if neither button pressed ton pressed d'199' ;test for max value beat_val_bin,v action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ; and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val ;here if overflow flags,one ;(earlier test assures no ;overflow beyond 199) action33 utton pressed d'40' ;test for min value beat_val_bin,1 ;decrement digital version lo_digit_val,7 ;test for underflow by action33 ;here if no underflow set this digit and decrement next 09</pre>
	bsf goto ;test for action30 btfss goto btfss goto goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw subwf bnz clrf incf movlw subwf bz clrf incf movlw subwf bz clrf bsf goto ;here if "down" b action32 movlw subwf bz decrement decf btfss inspecting msb goto ;underflowed, so movlw movwf	<pre>flags,mode action4 cr single buttons porta,2; "up" button pressed? action31 ;yes porta,3; "down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val ;here if overflow flags,one ;(earlier test assures no ;overflow beyond 199) action33 utton pressed d'40' ;test for min value beat_val_bin,1 ;decrement digital version lo_digit_val,7 ;test for underflow presset this digit and decrement next 09 lo_digit_val</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf incf incf sof bf bsf goto ;here if "down" b action32 movlw subwf bsz decrement decf btfss inspecting mb goto ;underflowed, so movlw	<pre>flags,mode action4 cr single buttons porta,2 ;"up" button pressed? action31 ;yes porta,3 ;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val,w action33 hi_digit_val,w action33 hi_digit_val, ;err if overflow flags,one ;(earlier test assures no ;overflow beyond 199) action33 utton pressed d'40' ;test for min value beat_val_bin,1 ;decrement digital version lo_digit_val,1 ;and decrement BCD version lo_digit_val,7 ;test for underflow presset this digit and decrement next 09 lo_digit_val,1 </pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf movlw subwf bnz clrf incf movlw subwf bnz clrf incf movlw subwf bz clrf incf movlw subwf bz clrf incf movlw subwf bz clrf incf incf incf incf incf incf incf inc	<pre>flags,mode action4 cr single buttons porta,2;"up" button pressed? action31 ;yes porta,3;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow flags,one ;(earlier test assures no ;overflow beyond 199) action33 utton pressed d'40' ;test for min value beat_val_bin,1 ;decrement digital version lo_digit_val,7 ;test for underflow </pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw subwf bnz clrf bnz clrf bsf goto ;here if "down" b action32 movlw subwf bz decrement decf decf btfss inspecting msb goto ;underflowed, so movlw movwf decf btfss goto	<pre>flags,mode action4 cr single buttons porta,2;"up" button pressed? action31 ;yes porta,3;"down" button pressed? action32 ;yes action4 ;next if neither button pressed d'199' ;test for max value beat_val_bin,w action4 ;cannot exceed 199, so must not beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow hi_digit_val,w action33 lo_digit_val ;here if overflow hi_digit_val ;here if overflow flags,one</pre>
	bsf goto ;test for action30 btfss goto btfss goto ;here if "up" but action31 movlw subwf bz increment incf incf movlw subwf bnz clrf bnz clrf bsf goto ;here if "down" b action32 movlw subwf bz decrement decf decf btfss inspecting msb goto ;underflowed, so movlw movwf decf btfss goto	<pre>flags,mode action4 cr single buttons porta,2;"up" button pressed? action31 ;yes porta,3;"down" button pressed? action32 ;yes action4 ;next if neither button pressed ton pressed d'199' ;test for max value beat_val_bin,1 ;increment digital version lo_digit_val,1 ;and increment BCD version d'10' ;action if BCD overflow lo_digit_val,w action33 lo_digit_val ;here if overflow flags,one ;(earlier test assures no ;overflow beyond 199) action3 utton pressed d'40' ;test for min value beat_val_bin,1 ;decrement digital version lo_digit_val,n action4 ;cannot go under 40, so must not beat_val_bin,1 ;decrement BCD version lo_digit_val,7 ;test for underflow flagit_val,7 ;test for underflow </pre>

movlw 09 hi digit_val movwf flags, one ; (assumes this digit was set to bcf one) ;now find 2-byte prd duration, expressed in tick counts, from table2 action33 movlw 2 ;define higher byte of lu table start address movwf pclath d'40' ;lu table starts at 40 beats per movlw minute, therefore offset subwf beat_val_bin,w movwf lu_address bcf status.c lu address ;there are 2 period values per rlf beat value, therefore ;multiply this address by 2 status,c ;is page rolling over?
pclath,1 ;yes, so increment higher address btfsc incf bits movfw lu address table2 call movwf next_prd_hi incf lu_address,1 ; check if roll-over will occur, ie movlw OFF if 255 subwf lu address,w btfsc status,z incf pclath,1 ;would cause page roll-over, so increment higher address bits movfw lu address call table2 movwf next_prd_lo ;reset pclath movlw 0 pclath movwf ; time to exit this routine action4 bcf intcon,t0if retfie ******* ; introduces delay of 1ms delay1 movlw Ofa movwf delcntr1 del1 nop nop nop nop nop nop nop decfsz delcntr1,1 goto del1 return delay10 movlw 0a movw£ delcntr2 call delay1 del2 decfsz delcntr2,1 goto del2 return ;200ms delay delay200 movlw 0c8 movwf delcntr2 del3 call delay1 decfsz delcntr2,1 goto del3 return ;determines output 7-seg led pattern table_dig addwf pcl retlw 3£ ;digit0 ;1 ;2 retlw 06 5b retlw retlw 4f retlw 66 retlw 6d retlw 7d retlw 07 7f retlw retlw 6f ;digit 9 ;this table determines the tick count required for given beat rate ;define start at beginning of page. org 0200 addwf pcl include<\pacific\bin\met_data.dat> table2 addwf end

Letters to the editor

Letters to "Electronics World" Cumulus Business Media, Anne Boleyn House, 9-13 Ewell Road, Cheam Road, Surrey SM3 8BZ e-mail j.lowe@cumulusmedia.co.uk using subject heading 'Letters'.

Morse codes

Prompted by Ian Poole's article in the October issue, I thought the following may be of interest.

The distress signal in Morse is one single character, di di di dah dah dah di di dit. It was chosen as being easily recognised and unlikely to be mistaken for something else. It isn't, never has been, and was never intended to be, SOS.

However, in text it is symbolised by SOS, indicating that it sounds like those three characters transmitted without inter-character spaces. It is probably this which led to the common misconception. It could equally be symbolised by, for instance, VMS or 3B.

The older distress signal, CQD, – which was three characters – was formed by adding the D, to indicate distress, to the the "all stations" call, CQ.

There has been speculation as to whether CQ is the phonetic for 'seek you.' This may or may not be so but I have never come across any reference to support this. David M Bridgen Camberley Surrey

A question of ratios

My apologies to Cyril for not being more explicit in the Letters pages, August 2001 issue. I'd assumed that it was obvious what I was referring to.

On page 217, Cyril states that "The LM3900 IC responds to current ratios at its inputs, not voltages as is more usual," which is of course incorrect.

The LM3900 is a differential amplifier, it responds to differences between its inputs (as most amplifiers do). A circuit that responded to the ratio of its inputs might be called a ratiometric amplifier, and an example of that would be a divider such as the AD734.

From the Concise Oxford Dictionary: ratio n. (pl. -os) the quantitative relation between two similar magnitudes determined by the number of times one contains the other integrally or fractionally. **Phil Denniss** Sydney

Sydney Australia

Homopolar generator

I found the article on Faraday's homopolar generator in the October 2001 issue very interesting.

The homopolar generator principle was used during the early part of last century for low-voltage welding and electrolysis. This type of machine was also known as the nonpolar or uni-polar generator.

One example is the C A Parsons & Co. motor generator. Briefly, its construction was

Enhanced audio power amplifier?

Putting two different voltage sources in parallel is asking for trouble. I am sure Dr White knows that too.

Putting two different current sources in series is also asking for trouble, but apparently that doesn't bother him. He did exactly that in his attempt to enhance the Maplin amplifier, described in the August 2001 issue, pp. 578-583.

Resistor R_9 has been replaced by a current source. Since R_9 is connected to the collector of Tr_3 – also a current source – either his current source or Tr_3 will saturate.

Nevertheless the amplifier will operate, but in the first case the power dissipation in Tr_3 is excessive and in the latter case the loop gain will have been halved and performance degraded.

The only purpose of resistor R_9 is to take most of the heat out from Tr_3 and not to set the collector currents of Tr_3 and Tr_4 . This is done by the tail current of the input stage, plus R_4 , R_5 and R_{10} . This is at least for me rather obvious. **Edmond Stuart**

Amsterdam

The Netherlands

David replies:

I'm pleased that Mr Stuart took enough interest in my power amplifier design to attempt an analysis of its workings.

If you refer to Fig. 1 and estimate the collector current of Tr_3 as suggested by Mr Stuart – i.e as a function of the tail current of the input stage, R_4 , R_5 and R_{10} alone – then you obtain a figure of approximately 14mA.

a three pole electro-magnet with a N-S-N arrangement. It had a centre coil and a rotating iron bar or armature inside a copper tube. The iron bar and the copper tube rotated together at 2000rev/min, generating one volt under the left-hand N pole and one volt under right-hand N pole. The resultant two-volt output was taken off through brushes.

A construction for obtaining higher voltages consisted of several insulated copper bars arranged around the central iron bar in what was virtually like a commutator.

Corrections

Buck/boost regulator: My circuit idea 'Buck/boost regulator' on page 628 in the August 2001 issue contains an error. The two tantalum capacitors are printed as "47" which could be misinterpreted. My submission did quote 4 μ 7, i.e. 4.7 μ F. Also, the 35V rating did not appear, which has equal significance.

Henry Maidment Salisbury Wiltshire

However, the actual collector current, as measured under quiescent conditions, is around 7-8mA. This is because the collector current of Tr_3 is restricted to a maximum value of around 7-8mA by R_9 .

The collector voltage of Tr_3 is measured at about 5V above the negative supply rail, so its not saturated. Consequently, the constant current source isn't saturated either.

Mr Stuart is correct in asserting that seriesconnected constant-current sources usually give rise to unstable circuit conditions, or often no current flow at all. But the constant current source used in my power amplifier is rather more than two series connected current sources. It is perfectly stable, with equal currents in each 'half' of the circuit, under all conditions. It is also, surprisingly, 100% self-starting; which it shouldn't be if you assume that the transistors involved are ideal.

My version of this type of constant current source is based on an original idea by T.D.S. Hamilton.

The proof of the pudding is in the eating. Both measurements and listening tests, by a fair number of different listeners, confirm that my design is superior to data sheet engineered versions of the Hitachi original.

Finally, can I use this opportunity to correct a small omission from my article. I've had a number of letters and e-mails querying the function and purpose of the component labelled "J" in Fig. 3 (attached to the collector of Tr_9). I'm afraid its nothing esoteric, merely a wire jumper, or zero ohm resistor, used to facilitate the PCB layout.

Pairs of brushes spaced around the lefthand pole and the right-hand pole were connected together in zig-zag fashion so adding up the voltage output. Depending on the number of copper bars, 5, 10 and even 12 volts could be obtained at very high currents.

The principle of operation of these generators is certainly interesting and worth further study and consideration for future applications.

R C T Stead Hampton Middlesex

Minimal audio oscillators:

The circuit idea in the September issue shows no transistor type number: my submission quoted the BC337 for the earpiece oscillator and the BC238 for the ceramic sounder oscillator. **D. Di Mario** Milan Italy

Direction finder using VHF

Ian Hickman designed this direction finder for determining the bearing of any given VHF transmitter. Assuming you can receive from transmitters in two different locations, you can then determine your position with the aid of a map and compass. This type of design normally needs two matched receivers. Ian keeps his unit simple by using one receiver and a multiplexer.

designed this direction finding system for determining the bearing of any given transmitter, relative to the direction-finding system. So that I could check that the system really did work, the direction finder was

designed to work in the VHF FM broadcast band, since the positions of the nearest transmitters of both national and local programmes, both BBC and commercial, were known.

The system was broken down into separate free-standing blocks, each of which a group of two to four students could build and test independently. As the end of the academic year neared, the most difficult part – system integration – was undertaken.

Choice of direction-finding method

There are numerous methods of arranging antennas so as to provide information on the direction of arrival of a signal. These range from the traditional 'Adcock' array of four vertical dipoles – with its 'octantal errors' – through more complicated systems such as the Rohde and Schwarz VHF maritime direction-finding stations using a circular array of dipoles, up to the most modern super-resolution systems using an asymmetrically placed array of antennas. These all use a fixed array of antennas, and are capable of direction finding over the full 360° range in azimuth.

The simplest array has only two antennas, but such a direction-finder using a fixed array suffers from ambiguities – a failing it shares with a direction-finder using a loop antenna.

Clearly, a signal arriving at right angles to the line joining the two antennas could be arriving from in front of, or behind the array – a 'reciprocal bearing'. There are ambiguities at all angles; for example a signal arriving from 45° front right could equally well be coming from 45° left rear. However, for simplicity a two antenna system was chosen, and the ambiguity can in fact be resolved.

How it works

In Fig. 1, imagine a signal arriving at right angles to the line joining the two short vertical whip antennas, which are spaced about 0.15λ apart. The signal from each antenna is split into two parts, A and A', B and B'.

One part of the signal (A) from the left antenna is combined with signal B' from the right antenna, which is delayed by its passage through a coaxial cable of physical length 0.15λ .

Due to the propagation velocity in the cable of about 60% of the speed of radio waves and light, 'c', the sample of signal from the right antenna is delayed by 90° – equivalent to a 0.25 λ electrical length – relative to the local left-hand signal. Thus signal B' emerges from the $\lambda/4$ delay cable as signal B", and is summed in the block labelled Σ with A.

When combined, the two signals give the resultant Channel A signal, lagging 45° on the left-hand antenna signal A, and of amplitude 1.414 times (+3dB) greater than either. This is shown in the top left vector diagram in Fig. 2. A similar arrangement produces the Channel B signal, Fig. 2, top right.

If now the transmitter were to move to the left of centre, the signal path to antenna B would be longer than that to antenna A. This extra delay is partially compensates the delay suffered in the A'-A'' delay cable, so that the two signal inputs to the Channel B Σ block are more nearly in phase, and the resultant Channel B signal is greater, Fig. 2 lower right. Conversely, the phase difference between A and B'' increases to greater than 90°, and the amplitude of the Channel A signal is reduced, Fig. 2 lower left.

By and large, transmitters don't move, but the same effect could be produced by rotating the antenna array in the opposite direction – to the right, or clockwise viewed from above. In practice, this is how the system is intended to be used; rotating the antenna array until the signals in the two channels are equal.

Measuring the relative amplitudes

Having converted changes in bearing into changes in the relative amplitudes of the Channel A and Channel B signals, it only remains to compare the amplitudes, to determine the bearing of the transmitter.

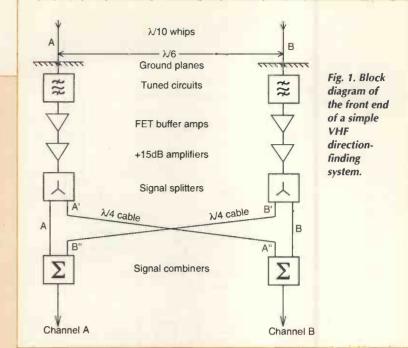
Clearly, each signal could be applied to one of two identical receivers, and I did once attempt to make a direction-finding system on this basis. But equally clearly, there are potential difficulties with this approach. The gain of either channel might vary with time, temperature, and even signal level, changing the relative gain of the two channels. Using a single receiver obviates this problem, and provides a useful economy in the sheer amount of kit required.

Hardware

Figure 3 shows the rest of the system, again in block diagram form. A local oscillator, mixer and integrated IF chip form a conventional FM receiver.

RF input to the mixer comes alternately from Channel A and Channel B, under the control of a two-way multiplexer (MUX) amplifier. Multiplexed signals pass through the receiver, producing an RSSI output.

The received signal strength indicator output is



demultiplexed, synchronously with the multiplexer/amplifier, to recover alternate measures of the strength of each channel's signal. Each demultiplexed signal's level is smoothed by a leaky integrator, the outputs of which drive a centre-scale meter.

For convenience in use, the audio output from the IF strip is fed to an audio amplifier and loudspeaker. This provides a ready means, in conjunction with the *Radio Times*, of identifying the station being received, and hence pinpointing its local transmitter.

Except when the transmitter is dead ahead of the array, the amplitude of the IF signal fed to the demodulator will be varying at the commutation rate of the multiplexer/amplifier. However, this is no problem, as an FM signal carries the programme information in the phase of the carrier.

The demodulator circuitry provides virtually complete immunity to the effects of amplitude variations. As is clear from Fig. 2, however, the multiplexed signal will also exhibit periodic changes in phase, synchronously with the commutation oscillator and multiplexer. This runs at a relatively low frequency, and the resultant phase change is small, a few degrees, even when the transmitter is well off centre.

Compared with the phase changes of many radians due to the programme modulation, the phase changes due to

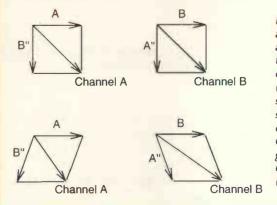


Fig. 2. For a signal arriving at right angles to the array, the two channel outputs are equal (upper), while for a signal arriving from somewhat left of centre, the B Channel output is greater than the A Channel output (lower).

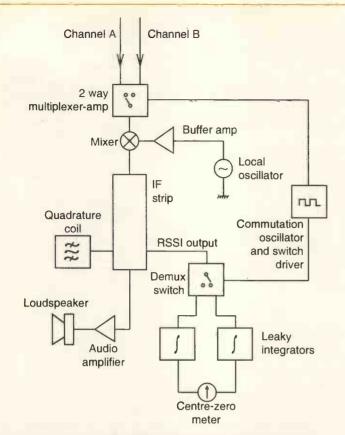


Fig. 3. Block diagram of the back end of the simple VHF directionfinding system. The multiplexed channel signals share a single receiver, saving costs and removing the need for matched receivers.

the multiplexer are negligible. At 150Hz, for example, the maximum permitted frequency deviation of \pm 75kHz at full modulation, results in phase changes of \pm 500 radians or \pm 29000° relative to the unmodulated carrier.

Solving the ambiguity

The ambiguity inherent in a two-antenna array is resolved as follows. The system is designed for use with an operator standing behind it with one antenna to the left of the operator, the other to the right.

Assume that the operator is looking in the direction of the transmitter of interest; the horizontally mounted meter therefore reads centre scale, pointing at the transmitter.

The meter is wired so that if the equipment is rotated to the left, putting the right-hand Channel B antenna



Fig. 5. The splitter and 3dB pads are ideally as shown. In practice, they will consist of standard value resistors as in Fig. 4.

nearer the transmitter than the Channel A antenna, the pointer of the meter moves to the right, i.e. it continues to point at the transmitter. If, however, the transmitter were behind the operator, then when the equipment was rotated to the left, putting the right-hand Channel B antenna further from the transmitter than the Channel A antenna, the pointer would also move to the left, the 'wrong way'. This clearly indicates that the transmitter is behind the equipment.

The antenna and splitter block

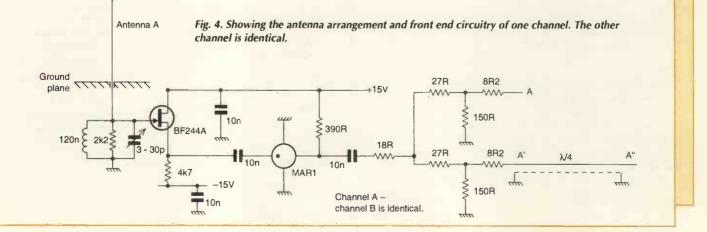
Figure 4 shows the antenna and splitter block. The antenna is a 16cm length of 18SWG tinned copper wire above a 30cm square ground plane consisting of single sided copper-clad board, copper side downwards.

The circuitry is all mounted below the ground plane, the antenna feeding a tuned circuit and FET buffer stage. The buffer drives a MiniCircuits MAR1 amplifier stage, which in turn feeds a resistive signal splitter. This splitter consists of a $Z_0/3$ three port 'Y' splitter with each output arm feeding a 3dB pad, ideally as in Fig. 5.

The output arms of the splitter have been combined with the input resistors of the 3dB TEE pads, and approximated to 27Ω . In fact, all the resistors are standard values, 16.66Ω not being a very convenient value. The 3dB pads add an extra 6dB isolation between the two outputs.

Output A is used direct while output A' is connected to a delay cable of electrical length $\lambda/4$, consisting of a 50cm length of miniature coaxial cable, and emerging as signal A". Channel B is identical to Channel A, producing outputs B and B". The circuitry is run from $\pm 15V$ stabilised supplies, which are used throughout the whole equipment.

Two more articles on this topic are to follow, containing details of other subunits of the equipment. The first will cover the sigma blocks, multiplexer amplifier, mixer, local oscillator, IF strip and quadrature coil. The second article will deal with the commutation oscillator, the demultiplex switch, leaky integrators and the audio section.







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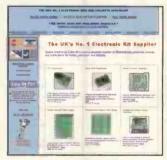
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Following on from the newsgroup discussion last month there is a UK Emaîl group for TV technicians where you can send an Email to everyone in the group. There's just over 30 people in the group at present. For more details and how to register look at the egroup home page. Just a general comment though you do have to be careful who you give your Email address to so that you can avoid "spamming" - that is getting lots of unwanted Email about dubious Russian site (amongst others).

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