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DIMENSIONS
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£17 25*

| OUTPUT POWER | 125 Watts RMS continuous |
| :---: | :---: |
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| INPUT A.C. VOLTAGE | $33-40 \mathrm{~V}$ |
| :--- | :--- |
| OUTPUTDC.VOLTAGE | 33 V nominal |
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| OVERLOAD CURRENT | $\frac{17 \mathrm{amps} \text { approx. }}{}$ |
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$\frac{\text { SENSITIVITY }}{\text { EQUALISATIOAN }}$
INPUTT IMPEDANCE
SUPPLY
DIMENSIONS
3.5 mV for 100 mV output

( | $110 \approx 50<25 \mathrm{~mm}$ (inc DIN |
| :--- |
| socket) |

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$\underset{20 \mathrm{kHz}}{\text { Withint }} 1 \mathrm{~dB}$ from 20 Hz to $50 \times$ ohms
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The PA12 Stereo Pre
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FREOUENCYRESPONSE $\quad 20 \mathrm{H}_{z}-20 \mathrm{kHz}(-3 \mathrm{~dB})$
BASS CONTROL
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INPUT IMPEDANCE INPUT IMPEDANCE INPUT SENSITIVITY $\quad . \quad \frac{1}{300} \mathrm{meg}$. oh CROSSTALK $\quad-60 \mathrm{~dB}$ SIGNALINDISE RATIO OVERLOADFACTOR TAPE OUTPUT IMPEDANCE 25 K ohms DIMENSIONS
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PS12 POWER SUPPLY
Designed for use with the AL30A S.450 and MPA30 in conjunction with transformer T538 INPUT VOLTAGE OUTPUT VOLTAGE $17-20 \vee A C$
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800 mA
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\section*{MORE RAM}

WE HAVE heard plenty about the 64 K RAM over the last few months-so much that we hesitate to mention it again-however, it was only a couple of months ago that everyone was contemplatting the government proposals and wondering if a sponsored company would be competitive. We have today received news of a Texas TMS 4164 which isyou've guessed it-a 64 K RAM. This new device comes in a standard 16 pin d.i.l. package and is expected to be available in sample quantities towards the end of the year; volume production early 1979-where were we?

It is interesting to note that the photomasks for volume production will be made using electron-beam equipment. It has been stated that the 64 K RAM is probably as far as we can go using the present production methods, this does not however mean that we are about to come to the end of further miniaturisation.

\section*{THE BUBBLE BURSTS!}

New technologies are always coming along. One that we heard much of a few years ago was the discovery of magnetic bubbles and how they would effect the whole electronics industry.

Well they haven't, have they? But wait, development of such things takes time and the bubble is just about to burst.

It seems that far from being contented with a probable first in the 64 K RAM area, Texas have also been playing with a few bubbles. A few did we say, the TIBO303 92k bit bubble memory will soon be available. This device contains 252 minor loops each with 1137 bubble positions! Of course this takes up more room than the regular 64 K semiconductor device and is therefore mounted in a 20 pin d.i.I. package! Can we go on believing it's all possible? (More details on this bubble memory can be found on page 1170 .)
We find it harder to accept the fact that the quarter million bit bubble chip is with us than that 100,000 active elements can be put on a silicon chip. This is probably because we tend to think of bubbles as having a relatively large minimum size, whereas we hardly had time to accept the transistor before it became integrated. We must look at bubbles again.

\section*{COMPONENT COUNT}

Dr. Robert R. Heikes, Vice President of Motorola Inc. and Assistant General Manager Semiconductors Group, speaking at a recent press conference
made the following statement:
"By the early 1980's, we will no doubt see the routine production of integrated circuits containing at least 100,000 active elements per chip, and by the mid-80's, that device count will reach an incredible one million components on a chip no larger than one-quarter of an inch square; or several billionths LAmerican billionths that is-Ed.) of a square inch per device.

With this degree of chip density, it is perfectly logical to assume that we will see the development, for example, of a product no larger than a hand-held calculator that will contain the computing power of today's largest main-frame computer. That's obviously a tremendous amount of computing capability."

It has been calculated that theoretically \(10,000,000\) components per chip might be achievable and, at the rate things are progressing (generally speaking the chip count has been doubling every year since the sixties), this will only take to the end of the eighties. What then? Many will say we will have gone far enough by then, but history tells us that we will continue to progress.

Mike Kenward

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\section*{Technical Queries}

We are unable to offer any advice on the use or purchase of commercial equipment or the incorporation or modification of designs published in Practical Electronics.

All letters requiring a reply should be accompanied by a stamped, self addressed envelope and each letter should relate to one published project only.

Components are usually available from advertisers; where we anticipate supply difficulties a source will be suggested.

\section*{Back Numbers}

Copies of most of our recent issues are available from: Post Sales Department, IPC Magazines Lid., Lavington House, 25 Lavington Street, London SE1 OPF, at 750 each including Inland/Overseas p \& \(p\).

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\section*{CONTROLLED DESCENT}

You are pilot of the first British expedition to the Moon. At one minute before touchdown the flight control computer blows a fuse, leaving you to land under manual control. There is a lever to control rocket motor thrust and a meter which can be switched to read velocity, height or fuel reserves. Your object is to achieve touchdown at a safe landing speed.

Two lights are provided; one tells you that you have landed and the other indicates whether or not the touchdown was at a safe velocity. Therefore when both lights are on together you have completed a successful landing.

A "Panic" button is provided. In the event of fuel running out before landing (because of a bit of ham fisted driving on the part of the pilot) it will divert the contents of the medicinal whisky tank into the rocket fuel tanks, giving an extra 15 per cent fuel.

\section*{SCHEMATIC}

The analogue computer in Moon Landing represents a simplified view of a space craft landing on the Moon. No account is taken of the changing mass of the rocket as it burns fuel or changing gravitational attraction, etcetera.

A schematic diagram of the game is shown in Fig. 1. It is not intended to explain in detail the theoretical background of integral calculus and analogue computers. Those interested in finding out more could start by reading the "Analogue Computer" series currently running.

In Fig. 1, the value of thrust selected by the pilot is fed into Integrator 1 which calculates the total quantity of fuel used. When fuel runs out a level detector switches off the thrust. A "Panic" switch feeds more fuel into the fuel tank when it is pressed. Thrust from the rocket engines is added to Moon gravity to give total acceleration acting on the ship. Integrator 2 calculates the resulting velocity and a level switch lights the "Safe Landing Velocity" light when the downward velocity of the space craft falls below a certain value. Velocity is integrated by Integrator 3 to give space craft height and another level switch detects when this is zero to light the "Surface Contact" light.

\section*{CIRCUIT}

The circuit diagram is shown in Fig. 2. Switch S2 has three positions. In the "Off" position power is disconnected


Control panel layout
from the circuit. In the "Reset" position capacitors in each integrator are charged to \(+5 \cdot 1 \mathrm{~V}\) to fill the fuel tanks (Integrator 1), give the rocket a large downward velocity (Integrator 2) and set the initial height above the Moon (Integrator 3).

When S2 is moved into the "Go" position the analogue computer starts its calculation. Slider pot VR1 ("Thrust") controls the voltage across R4. This voltage is fed into Integrator 1 (IC1) through R3. Output voltage of IC1 falls at a rate determined by the voltage across R4 (the "Thrust" setting) until point \(A\) goes sufficiently negative to forward


Fig. 1. Schematic diagram


Fig. 2. Moon Landing circuit
COMPONENTS . . .

\section*{Resistors}
\begin{tabular}{|c|c|c|c|}
\hline R1 & \(1 \mathrm{k} \Omega\) & R11 & \(100 \mathrm{k} \Omega\) \\
\hline R2 & \(100 \mathrm{k} \Omega\) & R12 & \(10 \mathrm{k} \Omega\) \\
\hline R3 & \(100 \mathrm{k} \Omega\) & R13 & \(1 \mathrm{k} \Omega\) \\
\hline R4 & \(240 \Omega\) & R14 & \(1 \mathrm{k} \Omega\) \\
\hline R5 & \(100 \mathrm{k} \Omega\) & R15 & \(10 \mathrm{k} \Omega\) \\
\hline R6 & \(6 \cdot 2 \mathrm{M} \Omega\) & R16 & \(10 \mathrm{k} \Omega\) \\
\hline R7 & \(10 \mathrm{k} \Omega\) & R17 & \(2 \cdot 2 \mathrm{k} \Omega\) \\
\hline R8 & \(10 \mathrm{k} \Omega\) & R18 & 330 k ת \\
\hline R9 & \(10 \mathrm{k} \Omega\) & R19 & \(10 \mathrm{k} \Omega\) \\
\hline R10 & \(220 \Omega\) & & \\
\hline
\end{tabular}

\section*{Capacitors}
\begin{tabular}{ll} 
C1 & \(0.1 \mu \mathrm{~F}\) \\
C2 & \(1 \mu \mathrm{~F}\) \\
C3 & \(0.47 \mu \mathrm{~F}\) \\
C4 & \(4.7 \mu \mathrm{~F}\)
\end{tabular}

All capacitors polyester

\section*{Diodes}
\begin{tabular}{ll} 
D1 & 1 S44 \\
D2 & 1 S44 \\
D3 & 1 S44 \\
D4 & 5.1V Zener \\
D5-D6 & TIL209 (2 off)
\end{tabular}

\section*{Transistors}
\begin{tabular}{ll} 
TR1 & BC214L \\
TR2 & BC184L \\
TR3 & BC214L \\
TR4 & BC214L \\
IC1 & 741 \\
IC2 & 741 \\
IC3 & 741
\end{tabular}

\section*{Potentiometers}

VR1 \(250 \mathrm{k} \Omega\) slider pot
VR2 \(10 \mathrm{k} \Omega\) trimmer pot

\section*{Switches}

S1 s.p.d.t. push-button
S2 PO type 1000 lever switch
S3 PO type 1000 lever switch

\section*{Miscellaneous}

ME1 1 mA meter. B1 and B2 PP3 batteries and suitable connectors. RLA d.i.l. reed relay \(500 \Omega\) coil \(3.7-10 \mathrm{~V}\) operation. Veroboard, suitable plastic case, nuts and bolts, etc.


Fig. 3. Veroboard component layout
bias D1. Current drawn through D1 reduces the voltage across R4 to zero and effectively switches off the thrust.

If the "Panic" button is pressed, charge on capacitor C1 is fed into Integrator 1 which increases the voltage at \(A\) by about +0.9 V thus adding to the fuel reserves.

The voltage across R4 is also fed into Integrator 2 (IC2) along with the effect of gravity (voltage across D2). These two inputs represent the accelerations acting upon the space craft and the output of Integrator 2 is the resulting velocity.

This output is monitored by TR2 which forms the "Safe Landing Velocity" level switch. When the voltage at B is above +0.5 V , TR2 is biased on and feeds current into the base of TR3, via R18, which also switches on.

TR3 collector voltage is about +9 V when it is switched on and so no current can flow through R16 to switch on TR4. D6 is therefore off. As the voltage at point \(B\) falls below +0.5 V TR2 switches off and so TR3 also switches off. TR3 collector voltage becomes more negative, current flows into TR4 base, switching it on and lighting D6. When the relay pulls in upon landing. TR3 and TR4 are connected into a bistable circuit, by feedback through R15, which remembers the condition of D6 at the instant of landing.

The voltage at B ("Velocity") is fed through a potential divider R9 and R10 and then into Integrator 3 (IC3) which calculates the space craft height. When the voltage at C ("Height") falls to about -0.4 V ("Surface Contact") diode D3 becomes forward biased and current flows through R12. The resulting voltage across R12 appears on the non inverting input of IC3 and is amplified in a positive feedback loop which forces the output of IC3 to -9V. D5 becomes forward biased and lights ("Surface Contact") and the relay is energised which latches D6 into the state it was in when the rocket landed.

\section*{METERING}

The meter ME1 may be switched by S3 to read "Fuel", "Velocity" or "Height". When the voltage at C switches to -9 V on landing, TR1 is switched on and shorts out the meter so that all readings fall to near zero on landing.


Fig. 4. Control panel wiring to Veroboard


Fig. 5. Rescaling an existing milliammeter

\section*{CONSTRUCTION}

The Veroboard layout of the Moon Landing circuit is shown in Fig. 3 and should present no constructional difficulties. Connections between the Veroboard circuit and the switches, l.e.d.s, etc. are shown in Fig. 4. These components are all mounted on the front panel. A plastic sandwich box was used to house the complete game and the layout chosen for the front panel controls is shown in the photograph.

\section*{CALIBRATION}

The 1 mA meter ME1 requires a new scale. Fig. 5 shows the relationship between the original \(0-1 \mathrm{~mA}\) calibration and the new one for fuel, velocity and height. The new scale may be drawn on plain white paper, cut to shape and glued into position. Take great care not to damage the meter movement while taking it apart.

Use the zero adjusting screw on the meter to set the pointer at zero on the velocity scale with the power off. Adjust VR2 to make the initial values (immediately after "Reset") of fuel, velocity and height agree with the new scale. The meter is now calibrated and landing is for "go".



\section*{with L686S SAFETY STAND}

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This lightweight thermal balance iron has a short heating element barrel for greater tip control and the Noryl plastic handle remains cool even after extended use. The bit supplied is 4.7 mm dia. with a 1 mm screwdriver face and other bits are easily fitted. Mains operated, the K1000 comes complete with two metres of three core cable and a solid stand especially designed for these type of irons.
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\section*{SPECIAL GERMAN SATELLITE}

A satellite is being built at the Max Planck Institute for Extraterrestrial Physics near Munich. It will contain sub-satellites made in Britain, Germany, USA and, it is hoped, the Soviet Union. The main portion is the Firewheel Satellite. It will perform like a firecracker when it begins its special mission.

The satellite will be launched from Kourou in French Guinea. The sub-satellites will eject ionised barium and lithium which will become clouds of plasma. Instruments on the ground, in aircraft and in the satellites will monitor the way in which the plasma is affected by the Earth's magnetic field. This will create similar circumstances that exist in the fusion experiments where a plasma is confined by a magnetic field in a Torus. The great advantage in doing this in space compared with the Earth based laboratory is that in space the plasma will continue to exist for 30 minutes or more, whereas in the laboratory it lasts for only a few seconds.

The satellite will be launched using the Ariane 200 ton vehicle from the new site in Guyana. It is a relatively cheap launch since its work load will last only a few hours. This means a very large saving in equipment and back up facilities. It is an important launch under the auspices of the European Space Agency.

\section*{MILITARY WEATHER SATELLITE}

A third satellite has been launched by the US Air Force from the Vandenberg base. The satellite which weighs 513 kg was put into a circular orbit at 833 km by a Thor launcher. This satellite is part of what is known as Block D Integrated Spacecraft System and is part of the Defence Meteorological Satellite programme. These rather special satellites have been designed to operate in the higher radion levels which are expected during the increase of radiation as the sunspot cycle nears maximum. It is heavier than its predecessors.

A particular technological note in respect of these satellites is that the on-board computers eliminate the need for a separate booster guidance system. The computers can also keep the pointing of the vehicle to Earth with an accuracy of \(0 \cdot 1^{\circ}\). Block D can take pictures of the whole of the Earth's surface twice a day. It has a high resolution, both in the visible and infra-red bands, of up to 0.5 km . Other facilities carried are an auroral detector, a line scanning radiometer, temperature-moisture sounder and pressure measuring equipment. The weather information is distributed to civilian users as well as the armed services.

\section*{TRACKING AND DATA RELAY SATELLITE SYSTEM, TDRSS}

An expensive re-design of the TDRSS has been set in motion after a report of the preliminary design review. The report showed that there was a hazard from Soviet interference. Several of the present ground stations will be replaced by two geosynchronous satellites capable of handling television, voice telemetry and scientific data to and from Earth orbiting spacecraft in the next decade.

The new programme was conceived when the fact was realised that the shuttle would demand extensive expansion because of the increase in traffic. NASA decided that the answer was to orbit spacecraft that could collect information and then pass it to selected stations. The report showed that the present designs were vulnerable and could be disabled by Soviet radar.

Western Union is providing \(\$ 796\) million for the design of six of the satellites. NASA will lease two of the satellites for its own communications purposes in late 1980, at the time of the first shuttle launch. The two satellites will operate at \(41^{\circ} \mathrm{W}\) over the Atlantic and \(171^{\circ} \mathrm{W}\) over the central Pacific basin. Engineers were particularly concerned about the vulnerability, and have begun the complete redesign of the integrated circuits and ground facilities to make for immunity.

The present time allowed for data entry is 0.01 sec . As the time to be used in order to avoid interference is of the order of 0.00001 sec, NASA finds itself in dispute with the contractors who claim that this item was not stipulated in the original requirement.

\section*{PIONEER VENUS 2}

Pioneer Venus 2 made a flawless start on its journey with four special probes to achieve a controlled landing through the atmosphere of Venus and make special observations. These were described in detail in a previous Spacewatch. Pioneer Venus 1 is due to encounter Venus on December 4th. It is the orbiter spacecraft of the mission and will observe Venus 2 as it approaches on December 9th. The probes will be released ahead of the main craft.

The important thing about the Venus 2 is that it is the last of the spacecraft to be launched by an expendable rocket. The next missions will be flown by shuttle techniques, in 1982. That will be the Galileo flight to the planet Jupiter.

Under monitor now there are no less than eight missions. In addition to the Venus encounters on the 4th and 9th of December,
there is continuous coverage of Voyager 1 which will fly past Jupiter in March 1979, Voyager 2 will follow in July. Pioneer 11 is due to reach Saturn by September 1979. The Viking orbiter and the landers will continue to report from Mars at least to the end of this year.

\section*{teleoperator retrieval SYSTEM}

NASA have contracted to Martin Marietta the development project for the service work on satellites in orbit. Teleoperator Retrieval System, TRS, is a reusable TV equipped spacecraft which will be used by the crew of the shuttle to deliver and stabilise satellites and when necessary recover them from orbit.

The TRS is a low thrust type of spacecraft which is to be operated by remote control from the shuttle. It is possible to carry it from, and return it to, Earth in the cargo bay. It can, if required, be left in orbit, parked, until it is collected at a later date. From time to time it would be returned to Earth for service.

The shuttle will take the TRS into a low orbit, and an astronaut will operate it by remote control from the Orbiter. A camera mounted on the bow of the vehicle will be the eye for the operating astronaut, enabling him or her to carry out the necessary manoeuvres required for docking with satellites and carrying out any task required.

The TRS has its own guidance control system. It will be able to take itself to higher orbits in order to deliver payloads or deliver them to the shuttle. It is a very exciting step for the new shuttle age.

The TRS chassis, or core as it were, will measure 1.2 m by 1.5 m . There will be 24 attitude thrusters on its eight corners, three to each corner. With the thrusters, three axis controls will be available, also forward and reverse movements. Up to four 680 kg Hydrazine propulsion kits \((90 \mathrm{~cm}\) in diameter and 1.5 m long) will each have eight rocket engines.

On the after flight deck of the Orbiter will be the hand controls for the TRS together with the communications and data management equipment, also a television monitor and displays which will allow control of the TRS through all its operations. From here it will be possible to transmit, receive and process telemetry, receive television pictures and to issue commands. A flight unit is scheduled to be delivered by September 1979.

\section*{INTELSAT TERMINAL}

At Goudji in Chad, the Central African Republic, an Earth satellite station has been installed by Thomson-CSF and CIT-Alcatel. The station is equipped with a 14.5 m antenna and can handle telegraph, telex and telephone communications via the Intelsat satellites. After 14 years of operation Intelsat is still expanding.

\section*{SPACELAB 2}

It is announced that there will not be a British astronaut on the Spacelab 2 mission. Two Britons were short listed but lost place to two Americans. The British pair were Bruce Patchett of the Appleton Laboratory and Keith Strong of the Mullard Space Science Laboratory.


OUR DECEMBER ISSUE WILL BE ON SALE FRIDAY, 10 NOVEMBER, 1978.

\section*{PRACIICAL EIECTRONICS uv uv DDODDD DODODOD DD DD UU}

N PART 1 of this article, the theory and circuit description of the VDU and its operational characteristics were presented along with a block diagram. In this part, construction, testing and setting up are dealt with. Construction falls readily into two component units: the RAM module and the main p.c.b.

\section*{RAM MODULE}

The 1 K block of RAM is constructed from eight 2102 i.c.s. Each of their ten RAM Address lines (RA1-10) must be connected together from chip to chip ( 80 interconnections). Similar common lines are required for their power supplies, chip select and RM lines (a further 32 interconnections). The RAM unit Data-In (DI . . .) and Data-Out (DO . . .) lines are all separate. Conventionally these i.c.s would be placed on an area of p.c.b., with all interconnections being made by fragile narrow copper tracks of minimal spacing (easy to solder-bridge or break) and consuming a considerable area of the board. The RAM module featured in this design drastically reduces the area of p.c.b. required, and the number of interconnections.

Two pieces of \(0 \cdot 1\) in matrix stripboard are cut to incilude 8 tracks by 17 holes each, and on one of these boards, 14 cuts are required as shown in Fig. 3(e). The leads of the eight RAM i.c.s must be fully and carefully straightened using a pair of long-nosed pliers (preferably non-serrated). These packages, even in plastic, are very robust and no harm will come to them as long as the pins are bent just once and with the minimum of stress. The pins may then be inserted through the Veroboards into alternate rows of holes leaving the copper tracks outwards. One complete row of holes is left free at each end of these boards to use as solder pads for connection to the main p.c.b. Check that the orientation of the chips is such that pins 11 and 12 are fitted into the
isolated portions of tracks of Fig. 3(e).
As soon as the i.c.s are in place, a couple of pins on each board should be soldered down to prevent the boards from slipping apart. The soldering should be done as fast as possible with a clean narrow bit, working along one track at a time so that successive solder joints are made to different i.c.s. This exposes each element to the minimum build-up of heat. Finally, the bottom two tracks (holding pins 8 and 9 of the i.c.s) are soldered to the copper strips on the main p.c.b. via stiff copper wire "legs", ensuring that the Vero track containing the pin 9 s of the i.c.s is soldered to the OV rail, refer to Fig. 3(a). Two legs should be used for each stripagain using the minimum heat necessary.

This technique, of course, is not restricted to 1 K blocks of memory, and the reader will appreciate how easy it is to extend this method to large blocks of RAM for the MPU main memory.

An excellent investment of effort is to carefully and fully clean away the solder flux from the work with cellulose thinners using a paint brush. This facilitates a check with a watchmaker's glass or magnifying lens, for solder bridges and dry joints, thus preventing flux laying across the joints, picking up moisture, and causing noise and cross-talk.

Having produced the RAM module, it is now necessary to connect buses of ribbon cable between the block and the main p.c.b. Three buses need to be connected to the RAM module: Data In (D1O to DI7), Data Out (DOO to DO7), and RAM Address RAO to RA9). The p.c.b. component layout of Fig. 8 contains the above identifications (in brackets) marked against their respective vero-pin positions, and this should simplify interwiring of the RAM module and main p.c.b. Figs. \(3(c)\) and (e) show the connections at the RAM end of the buses. Alternatively, Fig. 5 showing the RAM module circuit


Fig. 1. Circuit diagram of VDU. (The video switching stage and stripline modulator are shown in Fig. 2)


Fig. 2. UHF (stripline) modulator and video switching stage. See P.E. June 1977 for description of this modulator
diagram can be used for wiring up. It should be remembered that the RAM address lines are separate from the MPU address lines. but the Data in lines connect both to the MPU and the RAM module.

The order of connection of the data bits is irrelevent. except that data bit numbers IN must agree with bits OUT. Thus, if one of the i.c.s is chosen to accept data bit 4 IN (i.e. from the MPU bus) make sure that the same chip is chosen to supply data bit 4 OUT (to the buffer IC13).

The use of ribbon cable (preferably coloured) greatly facilitates checking faults. However, any type of thin wire is suitable, and p.t.f.e. covered wire is useful since the insulation is not prone to the usual effects of heat.

The RAM \(R / W\) line, and +5 V line may now be added. Finally, connect CS (pins 13) to the OV rail. This completes the RAM module and its wiring.

\section*{MAIN BOARD ASSEMBLY}

The construction of this section is conventional and straightforward. All pins for through-connections should be soldered in place first. Veropins will be found suitable. Next insert and solder all the i.c.s except for IC1 and IC10. Pay careful attention to i.c. orientation, positioning and minimum application of heat. It is better to make successive solder joints to different i.c.s, swopping back and forth between devices to expose each element to as small a temperature rise as possible. The i.c.s chosen are robust devices and, apart from IC1 and IC10, reasonably cheap, making sockets less important. However, ICs 1 and 10 should be provided with sockets. These should be soldered in next, taking care not to overheat them as the thermoplastic of which they are usually constructed melts easily at soldering temperatures.

The capacitors, resistors and transistors may now be soldered in, afterwards clipping all leads as close to the board as possible. Particular care should be taken to construct the modulator components neatly. It should be borne in mind that many of the copper foil sections on the modulator are deliberately employed as inductors. The precision of their geometry, for those who are producing their own boards, is therefore, of utmost importance.


Fig. 3. RAM module construction. Four pieces of stiff wire can be soldered to each end of each bottom track, to produce mounting "legs"' which can then be soldered to secure the module to the p.c.b.



The external wire links, sockets, variable resistors, PP3 battery connector (with appropriate lead length) may now all be soldered in place. The 1 MHz crystal can then be inserted with a piece of insulating material between its case and the p.c.b. The crystal should be pressed up against the board and soldered, very carefully. A note of caution on this final component is necessary. Whether the crystal be of the wire or the pin type, excessive heat or vibrational shock will detach it from its connections within the metal case, as the author has discovered to his cost. Thus, once the crystal is in place, subject the board to as little physical impact as possible.

The final operation should be, as mentioned before, to fully clear the p.c.b. of flux. This is especialiy important around the pins of i.c.s \(12,17,19\) and associated components, and the whole of the UHF modulator section.

\section*{SETTING UP}

Provision has been made on the p.c.b. for an inverting switch (S1). Initially, link \(\overline{\mathrm{O}}\) (pin 7) output of IC12 to the centre wiper position of the switch (i.e. to R2). Q may be used later, and an external switch fitted.

IC1 and IC10 may now be inserted and, after a final check of the other i.c.s to ensure all are inserted correctly, the 5 V and OV lines may be connected to their appropriate pins on the p.c.b. A 'scope is quite useful at this point to check for the presence of a signal at the video output (collector of TR1). This should appear as in Fig. 4 when using a range of about \(10 \mu\) s per centimetre.

The portion \(A-B\) is a negative going TV line synchronisation pulse to ensure that the electron beam strobes across the TV screen at the right time to catch and display the video information from the VDU board. Portion \(B-C\) is at a high level to ensure that the part of the line before the character display is bright. C-D contains information controlling the line's brightness across the screen (depending upon which line of characters is being built up, and the height along these characters at which the electron beam is passing through). D-E produces the bright portion at the end of the line. Bright portions are also placed at the top and the bottom of the picture as well as between character rows. This displays the 16 lines of characters as black upon a white background and spaced away from the distorting edges of the screen. VR2 is used to set the length of the character rows and may be varied to suit the TV set being used.


Fig. 4. Video output signal. Several of these sweeps are required to build up a line of characters on the screen, and the "light-dark" information is contained between C and D





Fig. 8. Component layout for VDU board

If the correct waveform is not found at the collector of TR 1, try looking at the \(\varnothing_{1}\) input to the CRTC. If no oscillation is observed, suspect IC17, IC18, the crystal, R1, R6, VR2 or C3. If 1 to 2 MHz oscillations are present at \(\varnothing_{1}\) with a good amplitude, check that \(R_{0}, R_{1}, R_{2}, P T\), address lines and sync are all oscillating. CRTC is suspect if not. If all are in working order, only IC10 and IC12 are left. \(R_{0}, R_{1}, R_{2}\) and PT inputs in a state of oscillation will produce dynamic information on \(b_{0}\) to \(b_{5}\) outputs of IC1O. LOAD and CLOCK oscillations to IC12 will produce outputs on Q and \(\overline{\mathrm{Q}}\) of IC12. By this process, the fault should be narrowed down easily.

The TTL oscillator IC18, should produce between 10 and 15 MHz , which will be difficult to resolve into a sine-wave on 'scopes with a lower band-width, but the waveform \(\varnothing_{1}\), out of pin 12 of IC17 should be seen easily on most 'scopes.

If either a monitor or modified TV set (which can accept video directly) is available, link SK1 on the p.c.b. to the video output, and turn VR1 to minimum signal and connect up. Turn VR1 up and a display of random characters should be seen. If necessary, adjust the horizontal and frame holds. The line length can then be adjusted by VR2. VR1 should be set for the clearest display setting. The prototype gave the best picture on a modified TV by feeding the video through a very small capacitor, about \(0.0001 \mu \mathrm{~F}\) is adequate but some experimentation is worthwhile here.

If there is only an unmodified UHF ( 625 line) TV available, setting up is restricted to linking SK1 to the modulator output, plugging in the PP3 battery and tuning the set (with VR1 up full), until it receives the field and then adjusting VR1 for the best picture. Use coaxial cable with proper coaxial plugs for connections.

\section*{UHF MODULATOR}

For those experiencing trouble with the modulator, the following information should be of use. The modulator has an isolated power supply which will last for some time with normal use. Check that its e.m.f. is 8 to 9 volts on load. The modulator section should not be resting on anything. Raise the whole board and support it an inch or two from the bench. The foil pattern or the value of the capacitor, C 4 , may be inaccurate-try replacing C4 by a trimmer and, with the TV tuned well away from any stations, tune the trimmer in to the TV.

If the TV tunes in, but the picture is unsatisfactory, even after adjustment, then the only recourse is to house the p.c.b., or at least the modulator and battery, in a properly earthed metal box (connected to the OV line). This final
construction gives very good results with the modulator if the p.c.b. is properly suspended away from the box sides (about 25 mm being sufficient).

\section*{TV MODIFICATION}

If you have decided to modify a TV to accept video, a few words of advice will be useful. As most sets do not have a mains isolating transformer, the first check must be to determine whether the live side of the mains is connected to the TV's chassis. Use an ohmmeter between mains plug and chassis. If so reverse the live and neutral wires and use a polarised mains plug to ensure neutral remains connected to chassis.

Somehow, the video line in the TV has to be found, broken and fed from the video output of the VDU. As mentioned before, video may be fed through a small capacitor to the TV set. The chassis of the set may also be connected through a capacitor to the OV line of the VDU, though it was found that too small a capacitor caused an intolerable degree of mains "beating" on the display. Once again some experimentation is advantageous here.

Some sets cannot be modified as the video line is contained within an integrated circuit, and so it is as well to check this before beginning.

One final note: the constructor should appreciate that the neater the wiring, the better the display. Use coaxial cable and sockets wherever possible, especially if using UHF.

\section*{CONSTRUCTOR'S NOTE}

A complete kit of parts including drilled p.c.b. is available from Technomatic Ltd. (01-452 1500) for \(£ 49\) including VAT and P. \& P. The p.c.b. is not platedthrough as previously stated, and we apologise for this error. Constructors will find that minimal extra effort results from using the p.c.b. supplied.

A limited number of assembled and tested boards will also be available at \(£ 69\) inclusive, from Technomatic Ltd., 17 Burnley Road, London, NW10, where a model is available for demonstration during normal hours.

Note: C9 in Part 1 components list, does not exist.

NEXT MONTH: Some ideas for interfacing to a system, some expansions of the basic VDU, and some hints on hardware for using the cursor control referred to last month.

News Briefs

\section*{STARLIGHT VISION}

AHIGH sensitivity proximity image intensifier now available from Mullard weighs less than 100 grams, and measures only 30 mm in length and 43 mm diameter. It is therefore particularly suitable for use in night-vision goggles and other applications where low weight and
small size are of prime importance. The intensifier, type XX1410, operates from a level of illumination below starlight ( \(10^{-4} \mathrm{lux}\) ), has a luminance gain of between 7500 and 15000 and incorporates automatic gain control which maintains a constant level of \(3 \mathrm{~cd} / \mathrm{m}^{2}\) on the screen.

The XX 1410 comprises a fibre-optic input window on the rear of which is deposited a low noise, high sensitivity, tri-alkali S25 photocathode ( 300 to 900 nm ). A micro-channel plate multiplies the electrons from the photocathode which are then focused onto the eyeadapted JEDEC P20 phosphor screen of a fibre-optic image inverter to form a bright image. Resolution is 25 line pairs \(/ \mathrm{mm}\) over the useful photocathode diameter of 18 mm .

The intensifier is encapsulated in a white plastic body together with its own integral d.c./d.c. converter incorporating switched-mode power supply techniques. Nominal supply voltage is 2.7 V d.c. and the current drain is typically 15 mA .


\section*{DAVID SHORTLAND}

W/hen bipolar transistors are used in high power circuits, many limitations are imposed on the designer because of inherent problems within the structure of the device. These limitations, which include thermal runaway, secondary breakdown, non-linear distortion and a limited frequency response, restrict the use of the device and have resulted in the need for complex and expensive protection circuits.

With the introduction of the Junction Field Effect Transistor (J-FET) and the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) many of these limitations were overcome but the FETs themselves were limited by their poor power handling capability. Now new fabrication processes are enabling FETs suitable for high power applications to be manufactured and these power FETs will directly challenge the supremacy of the bipolar transistor in many applications.

The new processes have resulted in the manufacture of three basic devices:

The VMOS power FET
The V-JFET
The power MOSFET
The first two devices utilise vertical current flow whilst the third retains the conventional horizontal current flow normally associated with low power field effect transistors.


Fig. 1a. Cross section of a typical VMOS device

\section*{VMOS POWER FETs}

VMOS, which is currently being developed by the Siliconix Corporation, enables a vertical channel MOSFET structure to be fabricated using a diffusion process similar to that used in the manufacture of double diffused bipolar transistors. After diffusion a "V" groove is cut into the silicon to create the vertical current channel which is a characteristic of VMOS FETs. A cross section of a typical device is shown in Fig. 1. (A double diffused bipolar transistor and a conventional MOSFET are also shown for comparison.)

The substrate of the device which is \(n+\) material is used as the drain with the \(p\) - body separated from it by an epitaxial layer of n - material. This epitaxial layer increases the drain-source breakdown voltage by absorbing the depletion layer from the drain-body junction. Because the gate overlaps n- rather than \(\mathrm{n}+\) material the concentration of impurities is less, the feedback capacitance is reduced and the frequency response of the device increased. After the " \(V\) " groove has been etched through the


Fig. 1b. Cross section of a conventional Mós device


Fig. 1c. Cross section of a typical double diffused bipolar transistor
source and body into the epitaxial layer, oxide is then grown over the surface of the device and aluminium deposited to form the source and gate connections.

\section*{ADVANTAGES AND DISADVANTAGES}

A comparison between VMOS and bipolar transistors includes many of the trade offs which are associated with their low signal counterparts. There are, however, several important differences which exist at higher power levels. These include:
(1) The very high input impedance of VMOS, which enables it to directly interface with other high impedance devices such as CMOS and opto-isolators. With a typical leakage current of less than 0.01 mA a fanout of more than 100 can be obtained from a CMOS device which is far higher than is possible with any bipolar transistor.
(2) The absence of minority carrier storage time. This is the time taken for excess charge carriers stored in the base


Fig. 2. Output characteristic curves of a VN66AJ VMOS device
region of a bipolar transistor to be depleted before the junction can change from the forward to reverse bias state. This delay affects the efficiency of a circuit especially when transistors are used in switching applications, with the result that in some switching circuits faster switching transistors with a low power rating are sometimes preferred to the slower types with a high power rating. As a VMOS power FET is a majority carrier device, with its charge carriers being controlled by electric fields rather than the injection and recombination of minority carriers, the only delay is caused by parasitic elements such as series gate inductance. A typical switching delay for a VMOS device is about 4 nano seconds to tum a 1 amp current on or off which is about 10 to 200 times faster than for a bipolar device.
(3) The absence of secondary breakdown. In power transistors this is caused by the very narrow base structures that are used to improve their high frequency response. The condition occurs because the distribution of current becomes nonuniform at certain high levels of current and voltage. With the current being focused on very small areas, localised thermal runaway or "hot spots" develop which melt the silicon, causing a short circuit between the collector and emitter. This problem cannot develop in a VMOS device because its temperature coefficient is negative (a bipolar's is positive). Therefore as its temperature increases it draws less current instead of more thus eliminating the device from both ther-
mal runaway and secondary breakdown problems.
(4) The very high gain of these devices enables them to directly replace Darlington pairs with improved reliability.
The two major disadvantages of VMOS are:
(1) With VMOS technology still being relatively new there is no "p" channel device presently available for complementary circuits although one is planned for the near future. It is however possible to overcome this problem by using " \(n\) " channel devices in a quasi-complementary configuration which does not appear to impose many of the problems associated with similar bipolar designs.
(2) The saturation voltage of a VMOS device (up to 3 V at 10A) is higher than for a comparable bipolar device ( 2 V or less). This affects the efficiency of an amplifier using VMOS and as a result slightly higher power supply voltages must be used for a given power output or with the saturation region being resistive, two devices can be connected in parallel which halves saturation voltage of a single device. However, as the technology improves the saturation voltage should be substantially reduced.
There are also several advantages offered by VMOS over conventional MOS:
(1) The current density of a VMOS channel-which is deter-


Fig. 3. Output characteristic curves of à conventional MOSFET device
mined by its width/length ratio-can be increased in a VMOS device by making the length shorter. This is because the channel length is determined by diffusion depths which can be more precisely controlled than the photolithographic techniques used to define the source-drain spacings of the horizontal MOSFET. The minimum channel length obtained in VMOS is \(1.5 \mu \mathrm{~m}\) while a conventional MOSFET is limited to about \(5 \mu \mathrm{~m}\).
(2) Because its characteristic "V" groove creates two drain channels (one on each face of the " \(V\) " groove) the current density of a VMOS device is inherently doubled.
(3) With the substrate of the device being used as the drain there is no need for drain metallisation runs on the surface of the chip. This allows the size of the chip to be further reduced and also keeps the saturation resistance low.
(4) In conventional MOS the amount by which the gate overlaps the source and drain must be large to allow for the tolerances in the photolithographic mask. This overlap increases the channel capacitance and limits the frequency response of the device, whereas the overlap in VMOS can be controlled more precisely by the diffusion techniques used.

\section*{CHARACTERISTIC CURVES}

The output characteristic curves of a VN66AJ are shown in Fig. 2. If these curves are compared to those of a conventional MOSFET (shown in Fig. 3) the main difference is that the drain
current is in amps rather than milliamps. The output curves are very flat because the output conductance is low, therefore any increase in the drain to source voltage, i.e. variations in the power supply voltage, will have little effect on the drain current above 1.0 volts due to the buffering effect of the epitaxial layer, allowing the current flow to be almost entirely controlled by the gate voltage.

\section*{HEAT DISSIPATION}

Although VMOS has a negative temperature coefficient which inherently reduces the current flowing in the device as its


Fig. 4. Graph showing drain-source resistance against temperature (Siliconix)
temperature increases, it is not totally immune from thermal problems. From the graph in Fig. 4, which shows how the drainsource resistance (Rds) is affected by increases in temperature, it can be seen that as the temperature of the device rises its "on" resistancé increases causing the current through the device to decrease. However, this rise in resistance causes an increase in the gate-source voltage which will increase the temperature of the device. If no action is taken to dissipate this increase in temperature the resistance of the device would not stabilise until after the safe operating temperature of the junction has been exceeded. So although the device is free from both thermal runaway and secondary breakdown problems it can still be permanently damaged by operating temperatures unless it is mounted on a suitably sized heatsink.

\section*{SERIES AND PARALLELCIRCUITS}

The negative temperature coefficient of VMOS enables several devices to be connected in parallel to increase the current handling capacity without the need for either power wasting ballast resistors or matching networks. If one of the devices shown in the parallel arrangement of Fig. 5 starts to draw more


Fig. 5. Method of correcting VMOS devices in parallel (Siliconix)
current, its temperature increases causing the current flow to be reduced and equalised throughout the devices. When two or more VFETs are connected in parallel their total "on" resistance is lowered. This effect results in low insertion losses when VMOS is used to switch low impedance systems. If parallel devices are used in the output stage of an amplifier the lower resistance enables the same amplification to be achieved with less current being drawn from the driver stage, whereas parallel bipolar devices require current to be supplied to both bases with the result that the driver must be uprated to handle this increase in current.


Fig. 6. Method of correcting VMOS devices in series (Siliconix)
When two or more devices are connected in series, as shown in Fig. 6, the breakdown voltage is increased. The resistors R1 and R2 have very high values because the gate drive current to TRI is very small. To ensure a fast switching time the gate is dynamically balanced by the capacitance divider formed by Cl and C 2 . If the values of the resistors and capacitors are chosen correctly any number of VFETs can be connected in this way.

\section*{VMOS DEVICES}

The complete range of VMOS devices available from Siliconix is shown in Table I. They are split into three main categories: general purpose, RF and power peripheral drivers.

General Purpose N-Channel
Enhancement Mode VMOS FETs
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Type} & \multirow[b]{2}{*}{Pmekrag} & \multirow[t]{2}{*}{\[
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& \text { Dexaspipation } \\
& \mathrm{T} e=250 \mathrm{C} \\
& (\mathrm{w})
\end{aligned}
\]} & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{}} & \multirow[t]{2}{*}{\begin{tabular}{l}
Vasionylo
Vosion \\
 \\
(V/A)
\end{tabular}} & \multicolumn{2}{|l|}{\[
\begin{gathered}
V a(t \mathrm{t}) \\
10=1.0 \mathrm{~mA} \\
10
\end{gathered}
\]} & \multirow[b]{2}{*}{\[
\begin{aligned}
& \text { (nemect }
\end{aligned}
\]} & \multirow[b]{2}{*}{(nowf} \\
\hline & & & & & & (Min) & (Mex) & & \\
\hline \(2 \mathrm{NB656}\) & 10-3 & 25 & 2.0 & 35 & 1.81 .0 & 0.8 & 2.0 & 10.0 & 10.0 \\
\hline 2 N6657 & T0-3 & 25 & 2.0 & \({ }^{60}\) & 3.011 .0 & 0.8 & 2.0 & 10.0 & 10.0 \\
\hline \(2{ }^{\text {N6E5S }}\) & \({ }^{10} 0\) & 25 & 2.0 & 90 & 4.011 .0 & 0.8 & 2.0 & 10.0 & 10.0 \\
\hline \(2 \mathrm{N6859}\) & T0-39 & 8.25
6.25 & 2.0 & 36 & 1.8.8.0. & \({ }^{0.8}\) & 2.0 & 10.0
10.0 & 10.0 \\
\hline \(2 \mathrm{NEG60}\) & - & \({ }_{6}^{6.25}\) & 2.0 & 90 & 4.011.0 & 0.8 & 2.0 & 10.0 & 10.0 \\
\hline VNEAEAF & 10-202 & 12.5 & 2.0 & 40 & 3.0/\% & 0.8 & 2.0 & 10.0 & 10.0 \\
\hline VNB6AF & T0-202 & 12.5 & 2.0 & 80 & 3.0/1.0 & 0.8 & 2.0 & 10.0 & 10.0 \\
\hline VNB8AF & 10-202 & 12.5 & 2.0 & 80 & 4.011.0 & 0.8 & 2.0 & 1.0 & 10.0 \\
\hline VN84GA & то-3 & 80.0 & 12.5 & 日о & - & - & - & 50.0 & 50.0 \\
\hline
\end{tabular}

F N-Channel Enhancement Mode VMOS

ower Peripheral Drivers
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{vos} & \multirow[b]{2}{*}{} & \multirow[b]{2}{*}{} & & & Hego & & \multirow[b]{2}{*}{Pechupe} \\
\hline & & &  & \[
\begin{aligned}
& \text { Lopicem } \\
& \text { (v) }
\end{aligned}
\] &  &  & \\
\hline S77v01 & 析 \({ }_{35}\) & \({ }_{20}^{2.0}\) & \({ }_{8.0}^{8.0}\) & 0.8 & 5:0 & 25
25 & \({ }_{\text {TO-3 }}^{\text {TO-3 }}\) \\
\hline \(5{ }^{\text {S7 } 7412}\) & \(9{ }^{9}\) & 2.0 & 8.0 & 0.8 & 5.0 & 26 & -10.3 \\
\hline (ty & 35
90 & 2.0
2.0
2.0 & 8.0 8 & 0.8 & 5.0
5.0 &  & (10.39 \\
\hline & \multicolumn{7}{|c|}{TABLE 1} \\
\hline
\end{tabular}

The general purpose range has ten types of VFET available in three different packages according to the power dissipation required. This range was designed primarily for amplifier and switching circuits and can be obtained in the following voltage ratings: the 2 N series \(35 \mathrm{~V}, 60 \mathrm{~V}\) and 90 V ; the VN series 40 V , 60 V and 80 V . All the general purpose VFETs except the VN84GA include a gate to source Zener diode to protect the gate oxide from rupture due to static charge build up.

The VN84GA is a second generation device capable of handling up to \(12 \cdot 5 \mathrm{~A}\) with a breakdown voltage of 80 V . At low frequencies it can deliver up to 80 watts whilst at 30 MHz its power output is only reduced to 50 watts.

Of the seven RF types available six are in the VN range and are used in RF power amplifiers, high current analogue and bridge switching circuits. These are available in TO3 and TO39 packages with voltage ratings of \(35 \mathrm{~V}, 60 \mathrm{~V}\) and 90 V . The VMP4 device, designed for VHF broad band amplifiers, receiver front ends and power oscillators, is available in the flange mounted, opposing source, strip line 380 -SOE-F package.

The third category covers power peripheral drivers designed to switch reactive loads such as solenoids, relays, lamps, displays and alarms. Because VMOS devices do not have secondary breakdown problems they are particularly well suited to handling the high voltages and currents which simultaneously occur in inductive loads.

\section*{PRACTICALCIRCUITS}

In order to drive a VMOS device the supply voltage must be applied to the source and drain with the drain being positive with respect to the source. Then because it is an " \(n\) " channel enhancement type device the gate voltage must be taken positive with respect to the source and body. The electric field set up by the gate voltage induces an " \(n\) " channel on both surfaces of the body facing the gate. This induced channel enables electrons to
flow from the negative source through the epitaxial layer and into the drain via the substrate. This current flow is almost entirely controlled by the gate voltage.

The simple audio power amplifier shown in Fig. 7 has an output power of 4 W over a frequency range of 100 Hz to 15 kHz . A


Fig. 7. Circuit diagram of a simple 4W audio power amplifier (Siliconix)
small signal JFET is used for the gate drive of TR2 and the design is greatly simplified by using an output transformer. The negative feedback applied via R8 keeps the overall distortion to 2 per cent at 3 W .

The amplifier design shown in Fig. 8 is a basic configuration using the second generation VN84GA device which is capable of handling 12.5 A . It will deliver 100 W into \(4 \Omega\) or using 120 V VNGs and raising the supply voltages to 55 V .100 W into \(8 \Omega\).


Fig. 8. Basic circuit configuration of a 100W audio amplifier (Siliconix)

\section*{THE VERTICAL JUNCTION FET (V-JFET)}

The vertical junction FET, the first commercially manufactured power FET, was developed in Japan based on conventional JFET technology. Yamaha were commissioned by the Japan Development Foundation to develop a device using techniques invented by Professor Jun'ichi Nishizawa of the Electronic Telecommunications Laboratory, Tohuku University.

A cross section of a typical device is shown in Fig. 9. The body of the device which is \(n-\) material has a \(\mathrm{p}+\) type grid mesh diffused into it. This grid mesh structure has the effect of splitting the device into thousands of tiny FETs connected in parallel. Current flows through the channels between the gate grid and into the source. The depth of the depletion region around the gate is controlled by the gate voltage and if the depletion region is increased the current flowing through the device is reduced. Although the operation of a V-JFET is similar to that of a conventional JFET, it has many of the same advantages over the JFET that VMOS has over conventional MOS.


Fig. 9. Cross section of a typical V-JFET device
There are two main differences between the operation of a \(V\) JFET and a VMOS power FET:
(1) The V-JFET is a normally on device with its maximum drain current being delivered when the gate voltage is zero. In order to bias a V-JFET off, a voltage must be applied to its gate. This effect does not cause problems at low power levels but if a V-JFET is to be used in high power applications the gate must be biased off before the supply is switched on, otherwise the drain current will rise rapidly and damage both the V-JFET and associated circuitry. On switch off the power must be removed from the output stage before the driver stage. This requirement results in a very complex power supply arrangement.
(2) Because the input capacitance of a V-JFET is higher than for a comparable VMOS device, its frequency response is lower.
V-JFET amplifiers are currently being manufactured by both Yamaha and Sony. For use in their B2 amplifier Yamaha have developed the 2SK-76 ( n channel) and 2SJ-26 (p channel) power FETs which have complementary characteristics. Their respective performance figures are shown in Table 2, with their output characteristic curves shown in Fig. 10. The output power stage of the B2 is shown in Fig. 11. A higher supply voltage is used on the driver stage to ensure the FETs turn on to full conduction,



Fig. 10. Output characteristic curves of the 2SK-76 and 2SJ-26 devices
and to reduce the effect of the input capacitance a symmetrical push-pull drive circuit is used. This also reduces the time taken for the gate to source input capacitance to charge or discharge and gives the largest possible high frequency response


Fig. 11. Output power stage of the Yamaha B2 audio power amplifier
\((0-100 \mathrm{kHz})\). To ensure effective heat dissipation the power FETs, which are connected in parallel, are mounted on separate heatsinks by a special process which reduces the thermal resistance to less than half that achieved with conventional mica construction.

\section*{THE POWER MOSFET}

The power MOSFET developed by Hitachi for use in their range of audio power FET amplifiers is a horizontal current device capable of handling 7 amps at 160 volts. This high current capability is achieved (as it is in all power FETs) by using a wide channel of short length which, in the case of the power MOSFET, is constructed under the gate electrode.

The power MOSFET has the same advantages over bipolar transistors that VMOS and V-JFETs have, but because it has both a high input capacitance and gate resistance, applications for the device are restricted to the audio power range.


Fig. 12. Cross section of a typical power MOSFET device
A cross section of a typical MOSFET device is shown in Fig. 12. The high drain to source breakdown voltage is obtained by using an ion implanted offset gate structure. This technique, which is also used in small signal MOSFETs, reduces the electric field around the gate electrode and also helps prevent an excessive gate charge damaging the device.
\begin{tabular}{|lrr|}
\hline & \(2 S K 135\) & \(2 S J 50\) \\
& 160 V & -160 V \\
Drain-Gate Breakdown Voltage & 14 V & 14 V \\
Gate-Source Breakdown Voltage & 7 A & -7 A \\
Drain Current & 0.63 A & -0.63 A \\
Gate Current & 100 W & 100 W \\
Drain Dissipation & \(150^{\circ} \mathrm{C}\) & \(150^{\circ} \mathrm{C}\) \\
Max. Junction Temperature & & \\
& \\
& & \\
\hline
\end{tabular}

The performance figures of two complementary devices are shown in Table 3, and the graph in Fig. 13 compares the respective input powers required to drive bipolar and MOSFET devices, to achieve a 100 W power output over a frequency range of 100 Hz to 1 MHz . With the MOSFET requiring a much smaller input power the driving circuit is greatly simplified.


Fig. 13. Graph of the input power required to obtain 100W using MOSFET and bipolar devices (Hitachi)
The circuit diagram in Fig. 14 shows the basic design of a 100W MOSFET amplifier with parallel complementary devices in its output stage. The first two stages of the amplifier use differential pair configurations with an active collector load in the second stage to provide the push-pull action. The coil in the output line reduces the residual distortion which is induced by magnetic coupling between the output line and power supply wiring, from 0.01 per cent to 0.003 per cent. The total harmonic distortion at 100 W is about 0.01 per cent, which is about ten times better than ordinary bipolar amplifiers.


Fig. 14. Basic circuit configuration of a 100W MOSFET amplifier (Hitachi)

\section*{\(4: 43\)}

\section*{PROXIMITY}

\section*{SWITCH}

THE touch switch described here evolved from a need for a switching method that would activate the display of a digital clock for a short viewing period, the display being normally off.

To do this without modifying the fascia of the clock suggested the use of a proximity type sensing plate mounted inside the plastic top cover, so that touching the top cover would operate the time display. The system devised was found to be sensitive, and could be suitable for many similar applications.

\section*{CIRCUIT OPERATION}

No originality can be claimed for this type of circuit, although systems of this type usually operate directly from
the 240 V mains. However, it was found that by incorporating a gain adjustment, adequate sensitivity was obtained from low voltages in the range \(12-25 \mathrm{~V}\) a.c. The principle of operation of the switch can be explained by considering the input to gate 1 . This gate is biased into conduction by the \(1 \mathrm{M} \Omega\) resistor, and the voltage at the input settles to about midway between \(V_{D D}\) and \(V_{S S}\); but by virtue of the single wave rectification of D4 from the secondary winding of the power transformer, the amplifier gate input is swept from approximately \(V_{D D} / 2\) to peak a.c. volts- \(V_{D D} / 2\) at 50 Hz . Consequently when the plate is touched the input is referenced to zero volts by hand capacitance, and an a.c. voltage appears at the input to gate 1. Negative a.c. feedback via R1 and C 1 reduces the sensitivity of the amplifier to stray high



Fig. 2. P.c.b. layout


Fig. 3. Component layout

\section*{COMPONENTS . . .}

Resistors
R1 \(27 \mathrm{k} \Omega\)
R2 \(1 \mathrm{M} \Omega\)
R3 \(6.8 \mathrm{k} \Omega\)
R4 \(10 \mathrm{M} \Omega\)
R5 \(1 \mathrm{M} \Omega\)
R6 100k
R7 \(2.2 \mathrm{k} \Omega\)
R8 \(56 \mathrm{k} \Omega\)
All \(\frac{1}{2} \mathrm{~W}\) carbon \(10 \%\)
Potentiometer
VR1 \(50 \mathrm{k} \Omega\) preset
Capacitors
C1 27pF
C2 \(1 \mu \mathrm{~F}\)
C3 \(\quad 0.05 \mu \mathrm{~F}\)
C4 \(150 \mu \mathrm{~F}\) elect. 40 V
\begin{tabular}{ll}
\multicolumn{3}{l}{ Semiconductors } \\
TR1 & BC477 \\
TR2 & BC107 \\
IC1 & CD4011 \\
D1-D2 & OA200 (2 off) \\
D3 & \(4.7 V\) Zener 400 mW (BZY88C) \\
D4 & OA200
\end{tabular}
frequency pickup by the plate
The amplified 50 Hz signal is fed to the second gate which has its input switching threshold set by VR1, serving as a sensitivity control. The setting of this level is stabilised by the output voltage of gate 1 being used as the reference. By the action of R2, this is the characteristic switching voltage for the i.c.

Gate 2 shapes the signal and this charges C2 through D1, thus switching gate 3 . The R4/C2 time constant determines the period for which the display is on. With the values shown this is about five seconds.

The output from gate 3 is not suitable for driving logic circuitry working from the zero volt supply. Therefore TR1, TR2 are used as level shifters, with TR1 acting as an inverting current switch driving TR2.

This was used to operate the blanking input to a CD4511 decoder/latch/driver. This input was held high to inhibit the display, with operation of the proximity switch causing TR2 to turn on and so allow the time to be seen.

For other applications it may be that reverse operation of TR2 is required (i.e. TR2 normally on, and is turned off by touching) and for this purpose gate 4 is available to invert the output from gate 3. If this is the case the connection \(A-D\) is removed and connections \(A-B, C-D\) substituted.

\section*{CONSTRUCTION}

A printed circuit layout is shown in Fig. 2. Extra holes are not shown for optional mounting of a horizontal preset resistor for VR1. Here the choice will depend on the mounted position of the board so that there is easy access to adjust for sensitivity.

Further holes are present to allow for the addition of the inverting gate 4 , if this is required. Alternatively the printed circuit could be modified to include this gate.

The sensing plate may be a piece of aluminium foil or copper laminate glued inside the plastic or wooden case of the switched equipment, and is connected by a short length of wire (less than 12 in ) to the component board.

\section*{ADJUSTMENT}

The size of the sensing plate is not critical and a 5 cm square worked well on both 12 and 25 V a.c.

The sensitivity control should be finally adjusted when the plate and switch board are mounted in their permanent positions. If the zero volt line is "mains earthed" then there will be a change in sensitivity, but this is easily compensated for by adjustment of VR1. The sensitivity can be adjusted to trip at a distance of several inches, or by lightly touching the case-depending on individual preference.


\section*{8-DIGIT COUNTER-TIMER}

The 8 -digit counter/timer introduced by Lascar Electronics is claimed to perform all the major counting and timing functions. The module can measure frequency from \(0-10 \mathrm{MHz}\), period from 0.5 micro-seconds to 10 seconds, frequency ratio between two inputs, time intervals in increments of 0.1 micro-seconds, and can also function as a normal 8 -digit totaliser. Mode selection is by a single external switch.


Four different ranges can be selected which determine the time or the number of cycles that the displayed data is accumulated over.

Fitted with 0.4 in , high efficiency orange l.e.d.s, the modules operate from +5 V d.c. Controls include store, hold and reset, while various outputs enable all functions to be monitored externally. The module is fitted with a 10 MHz quartz crystal to give a highly accurate timebase, with a temperature stability of \(\pm 10 \mathrm{ppm}\) over a temp range \(-20^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\). Price is \(£ 54.95\) plus VAT.

For further information contact Lascar Electronics Limited, P.O. Box 12, Module House, Billericay, Essex.

\section*{ALL THAT GLITTERS}

Autumn is here and the beauties on the beach are covering up, so take a last look at this deiectable detector by courtesy of Dixons publicity department.


Dixons offer four versions; one for children and beginners at \(£ 29.95\), two sophisticated models at \(£ 39.95\) and \(£ 49.95\), and an enthusiasts machine with meter, at \(£ 69.95\), which Dixons claim can detect a single coin at one foot, or larger objects at four feet.

\section*{ANY OLD IRON/ALLOY/CARBON}

Rumour has it that there is five hundred million pounds of lost or buried treasure in the country.

Market Place has been trying out an induction balance detector over lawns, paths, flower beds, etc. We didn't find any valuables

but did dig up one of Uri Geller's old spoons, a six inch nail, aluminium lawn edging, a pair of rusted secateurs, a large garage door hinge pin, and a piece of coke.

At only \(£ 13\), inc. p\&p, you might well uncover the cost of your investment.

Readers P.C.B. Services Limited, P.O. Box 11, Worksop, Notts.

\section*{HANDY DETECTOR}

Pocket size detectors which can trace wiring or water pipes and show the presence of iron reinforcing are available from sole U.K. distributors HDP Electronics Ltd.


There are three models: a metal detector (403), a voltage indicator (405), and a combination unit (407).

The detectors run off one 9 V battery and indication is by a signal lamp.

Volltronic is the name of the range which is manufactured in West Germany.

403 and 405 are \(£ 13.19\) and the 407 is £28.64, including \(\mathrm{p} \& p\) and VAT. Trade enquiries invited.

HPD Electronics Limited, 34/38 Dock Street, Leeds LS 10 1JF. Telephone 450222.

\section*{6800 PROGRAMS}

JCN Electronics have four programs for 6800 based microprocessors. They have been written to run with MIKBUS firmware and are available as photocopy listings or all together on a Cuts Format Cassette at \(£ 2\) inc.
\begin{tabular}{ll} 
Lunar Landing & \(75 p\) \\
Mastermind & \(30 p\) \\
Matchsticks & \(30 p\) \\
Print Formatter & \(20 p\)
\end{tabular}

Send large s.a.e. to JCN Electronics, Hodsock Park, Langold, Worksop, Notts. S81 0TF. Telephone Worksop 730282.
Note. October Market Place, Wonderboards. Orders should include 30 p for \(\mathrm{p} \& \mathrm{p}\).

\section*{ON BOARD SWITCHING}

If you are prone to housing small projects in tobacco tins these dual in line switches may help the aesthetics.

Fit them on the track side of 0.1 inch matrix board, then stand the board off the lid.

As well as smarten up a front panel they can be used, on board, as function/mode selectors, test switching, range changing, etc.

Contact ratings: \(1 \mu \mathrm{~V}\) to 100 V a.c., \(1 \mu \mathrm{~A}\) to 1 A -at up to 10 VA .


They are colour coded as per the resistor colour code and are available in banks of 4,6 and 8 at \(84 \mathrm{p}, £ 1.24\) and \(£ 1.52\) each, including \(p \& p\) but add VAT at eight per cent.

Verospeed, Barton Park Industrial Estate, Eastleigh, Hants SO5 5RR. Telephone: 0703 618525/6.

\section*{MINIATURE PUSH BUTTON SWITCHES}

A range of miniature snap-action push button switches, designed for 0.1 in printed circuit board mounting is now available from Impectron Ltd.


They have a positive snap or rocker action. Single pole press-to-break and changeover configurations are all available as standard, and an l.e.d. indicator can be incorporated to provide visual warning of function selected.

The basic body size of all types is \(12.4 \times\) \(12.4 \times 7.5 \mathrm{~mm}\). The selected push button or rocker action will add a further 5 mm to body depth.

Switches may also be mounted in line or block format to form key sets with mechanical interlocking and release mechanisms.

Despite their small size the switches are capable of handling up to 25 mA at 50 V d.c. Contact resistance is less than \(20 \mathrm{~m} \Omega\) and operational life is in the excess of \(10^{5}\) operations at full load. Operating temperature range is \(-25^{\circ}\) to \(+75^{\circ} \mathrm{C}\).

Impectron Limited, Impectron House, 23-31 King Street, London W3 9LH. Telephone 01-992 5388.


\section*{'"I AM YOUR AUTOMATIC MUSIC CENTRE'}

Sharp's SG500 has front located controls so that there is no need to lift the dust cover to operate. It has a LW/MW/SW/FM/FM MPX stereo tuner amplifier, a two motor drive cassette deck and a direct drive record player.

The amplifier has a \(45 \mathrm{~W} /\) channel (r.m.s.) output with 0.5 per cent THD at \(4 \Omega\) and sensor touch tuning on FM with up to seven preset stations.

Sharp's Auto Programme Search System is included in the cassette section, which locates and plays back automatically the track required, as well as Dolby noise reduction and tape selectors and changeover facilities.

The sensor touch player has a 31 cm turntable and a VM type cartridge. An auto disc detection system determines whether there is a record on the turntable and also its size, so that it automatically plays at the right speed and leads the arm to the correct position. Price is \(£ 644.95\). Remote control accessory, £84-95.

\section*{LARGE THROAT P.C.B. DRILL}

A p.c.b. drill stand, specially designed for drilling small quantities of boards, prototypes, one-off production specials, missed production holes and modifications, is now available from Technomark, Maidstone, Kent.


The motor body is supported on a cantilever spring system which switches the motor on when depressed. If the motor body is adjusted so that the motor switches on with the drill just touching the board surface, drill wander can be eliminated to enable accurate drilling of plain copper surfaces.

It has an integral 12 V d.c. power supply, fused and switched, low voltage lighting and a reliable high speed motor. Throat depth is 168 mm .

Each unit comes complete with chuck, collets, light and \(x-y\) locating jigs. Price is \(£ 61\) plus VAT.

Technomark, Allnut Mill, Church Road, Lower Tovil, Maidstone, Kent.

\section*{CLOCK DISPLAY}

A four-digit, seven-segment light-emittingdiode display designed for digital-clock applications has been introduced by Micro Electronics Ltd. The MCD 461 Series has a red numeric display which uses 0.6 in ( 15 mm ) high gallium arsenide phosphide light-emitting diodes. Both 12 and 24 hour versions are available.


The display is designed to offer a wide viewing angle, and can be mounted with a 0.1 in-pitch edge connector or connection pins.

The static forward voltage per segment is 1.7 V and the maximum ratings at \(25^{\circ} \mathrm{C}\) are: reverse voltage 5 V ; peak forward current per segment 200 mA ; continuous forward current per segment 20 mA ; and power dissipation 300 mW . Operating temperature range is \(-20^{\circ} \mathrm{C}\) to \(+75^{\circ} \mathrm{C}\).

The price of the unit is \(£ 54.95\) plus VAT and for further information contact Micro Electronics Limited, York House, Empire Way, Wembley, Middlesex.


\section*{REVIEW OF INTRUDER ALARMS AND SECURITY SYSTEMS}

Beat the burglar if you can. He'll be straight in through everyday doors and windows. Mortice locks will make him think twice, but until we have shuttered windows like our EEC neighbours then a piece of treacled paper is all he needs for a silent entry-unless you detect him and sound the alarm. Vandalism of private property is on the increase too. Big dogs are expensive to feed so how about this doppler fido.

\section*{ELECTRONIC WATCHDOG}

The BD 100 is a security device which combines the function of electronic clock with an intruder alarm. Unobtrusively built into a digital clock, the burglar alarm is brought into readiness by removal of an electronic 'key'. This sets up transmission of an inaudible highfrequency signal which establishes a sensitive field completely filling the room in which the alarm is set. Disturbance of the field by an intruder or any movement in the room is registered by the unit. setting off a high intensity audible alarm similar to that of a motor car horn. The alarm signal may be silenced only by the insertion of a uniquelymatched electronic key.


The device allows a 20 -second delay between entry into the room and insertion of the key without setting off the alarm. A similar delay allows removal of the key on departure.

Unlike many burglar alarm systems designed for the home, the BD 100 requires no special wiring. The unit simply plugs into a standard 13-amp mains socket. If there is a power cut, or if the plug is removed from the socket, internal batteries take over the power supply. The batteries are recharged when mains power is resumed.

The price of the BD 100 is \(£ 62.00\) plus VAT and further information can be obtained from Fotherby, Willis Electronics Ltd, Gladstone Terrace, Stanningley, Leeds.

\section*{ALARM KIT}

The "Remick" burglar alarm kit, complete with instructions and wiring diagram enables a handyman to install the system to suit his own requirements. The kit-which includes a control unit, four sets of magnetic switches (for doors or windows), pressure pad (for front door mat), mini siren and cable-can be extended to suit any size premises by fitting additional sensors and alarms which can be obtained separately


The system operates from mains supply with the loop circuits and alarm bell at 12 V d.c. The double loop circuit is provided so that any attempt to cut or short the leads will result in the alarm operating. Whenever the alarm rings it continues until it is manually switched off by the keyholder. A 12 V battery is supplied to maintain the operation of the system during a mains failure.

The price of the kit is \(£ 56\) plus VAT. For further information contact Photain Controls, Unit 18, Hangar No. 3, The Aerodrome, Ford, Sussex.

\section*{MINI-MICRO}

The ML-1500, which is also available from Photain Controls, is a miniature doppler microwave detector which has a linear range of 15 metres with a wide 140 degrees horizontal beam pattern. A special protection circuit prevents any interference from fluorescent lights affecting the circuit.


The unit should be mounted \(2-3\) metres above floor level and as microwaves can penetrate certain building materials such as glass and thin partitions, the unit should be pointed away from windows wherever possible. Price \(£ 80\) plus VAT.

\section*{TOUCHLESS CONTROL}

The door control system marketed by Inertial Systems is virtually vandalproof because the sensor and control equipment are concealed in the wall near the door and operated by presenting a "command key". rather like a credit card. a few inches away
from the sensor. Once the validity of the card is established the control unit operates the electronic lock on the door.

The command keys are precision tuned passive circuits which when energised by the sensor return a specific frequency pattern. The keys can be programmed with individual private codes to enable the system to grant or deny individual access according to the time and day. If required, the system can maintain a printed record of individual entries and exits by the time and date.

For further information contact Inertial Systems Limited, Elvaco House, High Street, Egham, Surrey.

\section*{SELF TEST SYSTEM}

The Mk III Harley alarm system has a self test facility which checks the unit when it is switched on. The complete system includes a 12 V battery, key bypass switch, battery level indicator, a "bell test" circuit, five magnetic contacts for doors or windows and two anti-

tamper micro switches, one of which will operate the alarm whether or not the unit is on or off if any attempt is made to interfere with the control unit.

For further information contact Harley Security Systems, 94 Normandy Street, Alton, Hants.

\section*{DOOR ANSWERING SYSTEM}

The Siedle 2000 door communication system available from Baron Security is a D.I.Y. unit suitable for use in individual homes.

The system consists of a door loudspeaker/microphone, home telephone, bell transformer and door release mechanism. The front plate of the door loudspeaker unit is flush mounted and includes a call button in the name plate.


The entrance door latch can be released by pressing the button mounted on the telephone.

The recommended price of the Siedle 2000 is \(£ 76.15\) plus VAT and it is available from Baron Security, 52 Monmouth Street, London.


Here is a collection of simple projects for use in vehicles with 12 V systems

\section*{AUTO-LIGHT}

\author{
P. Scargill
}

THE circuit to be described will be especially useful to those motorists who have been in the unfortunate situation of being left with a flat battery through leaving their lights on all day, or worse still, those who have been stopped at night by the police for having no lights on, as it will automatically switch both side and dipped lights on when the ambient light level warrants such action.

It is left unaffected by short tunnels, street lights, etc. so that before long the user will wonder why all cars don't have such a device.

Construction should present no problems, and as an added bonus, the front panel has a couple of indicators so that you can amaze non-technical friends with the wonders of modern science. These also function as lighting status indicators so that if you should ever have cause to use the car lighting on manual, they will act as a handy switch off reminder. By the use of moderately rated components, it is most likely that the life of the unit will outlast that of the vehicle.

\section*{CIRCUIT}

The operation of the circuit is shown in block form in Fig. 1. The ambient light level present at any one time is sensed by a

photocell and the output of this is compared to a fixed reference. When the light level falls, a timing circuit is started up. The instantaneous light level is hence averaged out over a period of time.

The output from this section is again compared to a fixed reference and when a certain level is exceeded, the resulting output is fed to a relay which controls the car lighting.

Fig. 2 shows the basic diagram of a Schmitt of the type used in this circuit.
\(R_{a}\) and \(R_{b}\) hold the op amp + input at a level of around half the supply voltage.


Fig. 2. Schmitt circuit

Fig. 1. Block diagram

Hence if \(V_{\text {in }}\) exceeds \(+V / 2\), the output will swing low. \(R_{c}\) introduces positive feedback to the circuit which as well as ensuring sharp switching of the output, introduces a certain amount of hysteresis which is determined by the combination of the relative values of \(R_{a}, R_{b}\) and \(R_{c}\).

The format used in Fig. 1 ensures that there is no loading of the input by the presence of \(R_{c}\)

In referring to Fig. 3-R1, VR1, and R11 form a resistive voltage divider across the supply rails, the voltage at the junction of R11 and VR1 varying in accordance with changes in ambient light level.

This voltage is fed via R2 to IC1, a Schmitt as described previously, so that the output of IC1 changes state at two different light levels, an upper and lower level brought about by the hysteresis produced by the presence of R5.

So we have a simple light sensor, but one incapable of distinguishing between light-up time and, say, a short dark tunnel.


Fig. 3. Circuit of Auto-Light
Fig. 4 (below). Modification for positive earth

The following stages are therefore essentia for correct operation of the circuit for the application with which we are concerned.

Components R6 and C1 form a charging circuit which produces a 20 second delay in conjunction with IC2. C1 has been taken to \(+V\) so that at switch-on, it will be discharged and will hold IC2 input high, keeping the output low.

If the situation was reversed and C 1 was returned to OV , when the ignition was switched on, there would be a momentary flicker of the lights in daylight. This could be put to good use if a momentary delay was introduced to the output to combat this pulse, as a delay defeat would be realised at ignition switch-on.
However, for the sake of reliability and simplicity this feature has been omitted from the present circuit.
D1 ensures that the delay is not cumulative-a succession of short tunnels will not trigger the relay.

In this situation without D1, the motorist would find his lights triggering prematurely which, to say the least, might annoy other motorists.
TR1 is the relay driver, with C2 preventing any supply generated pulses from reaching the relay.
D3 is not used as an indicator (although there is no reason why it should not be brought out to the front panel if desired) but is used as a form of Zener to ensure that TR1 receives no input when IC2 output is low.

Feedback is applied from the relay back to IC2 pin 3 to ensure that any battery voltage changes do not cause relay chatter. Normally this would not occur but it has been found that in freak conditions this can occur if R7 is not present. It is essential to prevent relay chatter in this application in order to prolong the life of the relay contacts.


In this circuit, use is made of the output current limiting of the 741 op amp in restricting the current to D3, therefore it is not recommended to use any other type of op amp. However, most npn power transistors are suitable for TR1 and the relay is not critical provided it has a 12 V coil and that the contacts are capable of handling the current.

\section*{CONSTRUCTION}

Construction and layout are not critical as there are no particularly sensitive sections in the unit. However, good soldering is essential in any gadget for use in a vehicle because of vibration effects.

In the prototype, a copper-clad etched circuit board was used, details of which are given in Figs. 5 and 6.

A relay with 5 amp contacts was used in this prototype as the headights in many modern cars have their own relay drive. If the unit is to be used in a vehicle without this facility (particularly if extra lights have been fitted) a relay with 10A contacts may be better.

Tandy sell a very nice enclosed relay with DPCO contacts with this rating. However, a
bigger case will be required than that shown unless the relay is housed separately to the main unit.

\section*{FITIING AND SETTING UP}

The unit should be mounted as near to the lights switch as possible. From that switch it will be possible to obtain tappings into dipped lights, side lights and in some cases a live switched through the ignition. An earth will have to be found elsewhere

Finding out which wire is which on the car lights switch is a matter of consulting the vehicle wiring diagram and no advice can be given as all cars are different in this respect.

The sensor should not be mounted in a position where it is in direct line with any strong source of artificially generated light, i.e. opposing traffic headlights, although the unit is not particularly sensitive to this light. The best place to mount it is in the left hand corner of the dash, preferably out of sight. Positioning is not critical, however.

Having wired the unit up, it is simply a matter of waiting till lighting up time for final adjustment of VR1. A voltmeter across OV and IC1 output will give an


Fig. 5. P.c.b. layout instantaneous indication of triggering rather than having to wait out the delay after every small adjustment.

Adjust VR1 until the exact point at which IC1 output goes low is found and leave the preset at this exact point. Now fasten the case up and that is all there is to it.

The car lights should now come on after about 20 seconds, and should go off immediately the ignition is switched off. On turning the ignition back on, there should be a further 20 second delay before the lights come back on. Check to make sure the correct lights are operating and also that both of the indicators on the unit itself are working correctly. If the auto/manual switch is fitted. switch to manual, put side lights on manually in the normal way, and make sure the correct indicator shows on the unit.


Fig. 6. Component layout

\section*{COMPONENTS}

\section*{Resistors}
\begin{tabular}{|c|c|}
\hline R1 & \(100 \Omega\) \\
\hline R2 & \(10 \mathrm{k} \Omega\) \\
\hline R3 & \(15 \mathrm{k} \Omega\) \\
\hline R4 & \(15 \mathrm{k} \Omega\) \\
\hline R5 & \(27 \mathrm{k} \Omega\) \\
\hline R6 & 470k』 \\
\hline R7 & \(15 \mathrm{k} \Omega\) \\
\hline R8 & \(15 \mathrm{k} \Omega\) \\
\hline R9 & \(56 \mathrm{k} \Omega\) \\
\hline R10 & \(10 \mathrm{k} \Omega\) \\
\hline R11 & ORP12 \\
\hline All re & istors \(\frac{1}{8}\) \\
\hline
\end{tabular}

Potentiometer
VR1 \(10 \mathrm{k} \Omega\) preset

\section*{Capacitors \\ C1, C2 \(22 \mu \mathrm{~F}\) elect 16 V (2 off)}

\section*{Semiconductors}
\begin{tabular}{ll} 
D1 & 1N4001 \\
D2 & 1N4001 \\
TR1 & BD131 \\
IC1, IC2 & 741 (2 off) \\
D3 & TIL209
\end{tabular}

Relay
RLA 12 V d.c. \(110 \Omega\) coil two-pole changeover (R.S Cat. No. 348-835).

\section*{Miscellaneous}

S1* S.p.s.t. miniature on/off lif required)
LP1-LP2 12V indicator lamps

\section*{VARI-WIPE}

AN intermittent wiper control facility is now standard equipment of many new cars. Such a unit proves indispensible in British weather, and the present design allows a wiper delay to be added to any car. It is of very simple design, making it easy to build successfully. The small number of components make the unit reliable, and keeps the cost below that of four gallons of petrol.

\section*{CIRCUIT DESCRIPTION}

The circuit is shown controlling a twospeed wiper motor with a motor-shorting parking switch; this represents the arrangement on most recent cars. The simpler circuit used on older cars, with a non-shorting parking switch, will also work with this design.

In normal operation of the wipers, with the unit turned off by S1, RLA/1 restores the original connection which is broken on installation. When the wiper switch is moved to "Slow" or "Fast", the appropriate winding on the motor is disconnected from Qhe limit switch and connected to the 12 volt supply. the motor running
continuously. On switching the wipers off, the motor is connected to the limit switch which maintains the 12 volt supply until the park position of the wipers is reached. The limit switch then disconnects the 12 volt supply and short circuits the motor, providing rapid braking.

If the intermittent control is now switched on with \(\mathrm{S} 1, \mathrm{C} 2\) begins to charge at a rate determined by R2 and VR1. When the voltage across C 2 exceeds the Zener voltage of D1, the Zener diode conducts and switches TR 1 on. RLA/ 1 operates and connects the 12 volt supply to the motor "slow" winding via the wiper switch. As the motor runs, the limit switch moves to the "Run" position to maintain the motor supply, and also short circuits the intermittent control unit, discharging C2 via D2 and S1, and resetting the circuit completely. At the completion of one sweep of the wipers, the limit switch parks the motor and removes the short circuit across the intermittent control, restarting the cycle.

The repetition rate of the cycle depends on the setting of VR1, and the values given in the circuit provide a delay adjustable

\section*{B. A. Bell}
between five and 30 seconds. R2 may be decreased in value if a shorter sweep delay should be required. R1 limits the base current in TR1 when D1 conducts, and C1 charges rapidly when RLA/1 operates to hold the relay closed until the limit switch takes over the supply to the motor.

\section*{CONSTRUCTION}

The components making up the circuit can be conveniently housed in a small plastics box.

The box may be mounted underneath the dashboard or may be mounted remotely, with VR 1 connected by flying leads. Only three connections are required to the vehicle, a 12 volt supply from the ignition switch, and an interruption in the wire which connects the wiper switch to the motor.

This connection can be made by unplugging this wire from the switch behind the dashboard, and connecting the unit to the now vacant terminal on the switch and to the free end of the unplugged wire. If the unit is removed from the car at a future date, this wire must be replaced.
Resistors
R1 \(39 \Omega\)
    R2 \(1 \mathrm{k} \Omega\)
    All \(\frac{1}{4}\) watt \(10 \%\) carbon
Potentiometer
    VR1 \(10 \mathrm{k} \Omega\)
Capacitors
    C1 \(1,000 \mu \mathrm{~F}\) elect 15 V
    C2 \(1,000 \mu \mathrm{~F}\) elect 15 V
Semiconductors
    D1 1N5239
    D3 1N4002
    TR1 BD131
Relay
    RLA KMK1/12DC Keyswitch

\section*{Miscellaneous}

Plastics bo \(5 \mathrm{in} \times 2 \mathrm{in} \times 2 \mathrm{in}\) with lid S1 on/off switch

\section*{IN USE}

The unit is operated by rotating VR1 and setting the desired delay. If there is a temporary increase in spray or rainfall, the intermittent action is over-ridden by operating the wiper switch in the normal way. This automatically disconnects the unit until the wiper switch is turned off, when the intermittent action will be resumed. The prototype has functioned faultessly for two years on a number of cars, and worked first-time when it was assembled.


Vari-Wipe circuit

\title{
ASSISTED IGNITION SYSTEM
}

\section*{G. C. Wride}

BACK in the early 1900's a man invented an ignition system comprising of two coils of copper wire, one with a large number of turns, the secondary, and the other a few turns, the primary; he then connected the primary across the battery via a pair of contact breakers across which he connected a condenser. This is the Kettering system which has changed very little since then with the exception of improved materials. Well, way back in 1905 I doubt if they had an engine which would rev much over 2,500 r.p.m. so the system worked very adequately, but most cars these days can rev to at least 5,500 and quite a few to 7,000 and the Kettering system starts to have a hard time keeping up.

Let's look at the low rev end first, for instance, tick over-the points are opening slowly, this gives some of the stored energy in the coil time to arc across the gap so not only burning the points but losing valuable output to the plugs. At the mid range, say, between 2,000 to 4,000 , things are not so bad, the output rising to about the maximum to be expected. Things start to go wrong at about 5,000 and above as the available time for the coil to recharge itself is very short (coil recovery time).

Points may bounce, further reducing coil
current, and to make matters even worse, because of high cam speed the points tend to close late and the net result of all this is very low output to the plugs.

Finally, after 5,000 miles, the points are so burned that they have to be thrown away and the timing re-done.

\section*{SYSTEMS COMPARED}

Now we've looked at the problems, let's see how we can get over them. About 10 years ago the "Capacitive Discharge System" arrived on the scene; this was really excellent but in the early days it suffered from s.c.r. "hang-up's" or "latch on's'", also the discharge capacitor was somewhat unreliable.

It operated by inverting the 12 volt supply up to 350 volt with a pair of 2 N3055s, charging a capacitor then dumping the lot across the coil via the s.c.r. which was triggered by the points.

Its counterpart the "Points Assisted System" basically replaces the points with a power transistor capable of withstanding \(300-400\) volts or so, which is a very good move since the transistor in this position is a far better switch; secondly, point burn is
eradicated, other than this, unfortunately, the system mimics the points exactly. Taking a long look at the aforementioned system I decided there were a number of improvements that could be made.

The ignition coil is basically efficient, its losses mainly being due to its own internal resistance, which we can't do anything about and the external components, which we can. Firstly, we replace the points with a transistor, preferably the type specially designed for switching; secondly we can "tune" the coil to the engine's requirements, these being:
(a) A fast rising waveform
(b) Large amplitude
(c) A slow decay

Unfortunately, none of these conditions are complementary so a compromise must be found.

This design ensures that the maximum possible current for the longest possible time flows in the primary of the ignition coil, this being determined very simply by the use of a monostable; the only work that the contact breaker does is to trigger the monostable via a differentiator so their life is only determined by mechanical wear.

By careful differentiator design it was possible to build in three other innovations,
these being
(a) Contact bounce suppression
(b) Over-rev limitation
(c) Anti-theft provision

The system was tried on varous makes of car and was found to work very well, even on those with very dubious electrical systems. Four connections are all that are required and no modifications need be carried out to rev counters or tachometers.
It should be noted that although the cars tested were four cylinder, I see no reason why the system shouldn't work equally well on six or eight cylinder engines.

\section*{CIRCUIT}

Resistor R1 supplies the contact breaker with approximately 120 mA . This is sufficient current to wet the points to prevent corrosion and provide a low impedance source for the differentiator (Fig. 1).
The differentiator is formed by components C1, R1, D3, R2, R3, VR1, R4, D2, R5 and R8. R5 and R8 are also a potential divider to the input of TR2. VR1 sets the upper revolution limit, R4 being normally short circuited by the anti-theft switch and is selected according to the maximum revs required before the engine starts to misfire.

The anti-theft switch is obviously mounted discretely under the dash or other convenient place.

The time constants on the positive half cycle of the differentiator las the points open) mainly consists of R2 as D2 is conducting; D3 also conducts, raising the base of TR2 to its triggering potential, i.e. 2 volts. As the points close the output across C 1 swings negative, D2 and D3 are nonconducting and C1 now discharges through R3 and VR1.

The time constant on the positive swing (points open) is arranged to allow C1 to be fully charged at the shortest dwell time or maximum revs (Fig. 2a). When the points close the negative output swings to -12 volts approximately, Fig. 2b. Now as the time constant is longer the voltage across C1 becomes progressively larger (-ve) as the revs are increased, therefore, eventually a point will be reached where the positive output pulse will be below the trigger voltage of TR4 and engine misfire will result (Fig. 2c). Point bounce suppression is effected in the same way. The bounce occurs just after closure so as C 1 has had very little time to discharge the resulting pulse is well below the trigger potential of TR2 (Fig. 2c).


Fig. 1. Assisted Ignition System

\section*{MONOSTABLE AND OUTPUT STAGE}

The monostable is conventional except for the offset diodes D4 and D5 which, in conjunction with the base emitter voltage of TR2 and D3, define the triggering potential.

The output pulse width is set within the limits of 1.9 ms to 5.5 ms with VR2 ("Set Dwell').

Regulating the 6.2 volt supply ensures a constant pulse width, even if there is a considerable change in battery voltage.

The negative going pulse is taken from TR2 collector to TR3 base via R13 which turns off TR3, TR4 and TR5. R17 is chosen to fully bottom TR4.

The output transistor TR5 carries all the coil current and is driven as a fast switch. D6, 7 and 8 protect TR5 from the negative swing from the ignition coil. When TR5 is


Fig. 2. Differentiator output waveforms at 7,000 rpm
turned off the collector swings to approx imately 400 volts. D6, 7 and 8 conduct, charging C 4 to this potential, as the potential at the anodes of the diodes moves below that on the cathode D6, 7 and 8 become non-conducting so isolating TR5 from the negative transient. The discharge time of C4 is through R19.

By the time TR5 is ready to turn on again the voltage across C 4 will be approximately +24 volts, so the remaining charge left in C4 will not damage TR5.

TR5 must be mounted on a heatsink of 18 s.w.g. aluminium of not less than 4 square inches.

\section*{CONSTRUCTION}

The prototype was constructed on 0.1 in copper strip board and mounted in an "MK" wall mounting box with a cover plate; this was found to be eminently suitable as it can be made almost watertight. There is no need to screw down the component board as this can be made a snug fit, also if the cables are all taken out from one side in the event of service, the top plate can be unscrewed and the whole panel hinged out for service.

A recommended layout is shown in Fig. 4 and is by no means critical with the exception of the components R17, D6, 7 and 8 which run warm; these must be mounted away from the panel.

Leads carrying high currents, i.e. 100 milliamps or more, should not have long lengths of print between them unless a wire
link is also inserted (my experience is that if you don't do this, the print will fuse at the holes, this of course being the weakest point).

If the construction is done on 0.1 in matrix board, the heavy duty auto cables will not pass through the holes so the use of Veropins is a good idea.

The cover plate can be drilled to accept TR5 and heat sink.

COMPONENTS . . .


INTRUDER ALARM

\section*{A. Chadwick}

THIS car burglar alarm incorporates many of the attractive features of previously published circuits.

In operation is is enabled and disabled by a hidden switch in the interior of the car. There is a delay between applying the switch and the enabling of the alarm, giving time for leaving the vehicle.

The alarm is triggered by any load put on the battery; for example the interior light on opening the door.

A shorter delay exists between triggering and any audible output, giving time for the circuit to be disabled.

\section*{ALARM}

The actual alarm consists of pulsed operation of the horn. After a set time the horn is switched off, and the alarm reverts to the enabled state, ensuring that false triggering does not lead to a flat battery.

\section*{CIRCUIT}

Operation of the enable switch S1 causes the output of the R-S flip-flop, formed by IC1a and IC1b, to go to logical zero. After a delay determined by VR1 and C 2 , the input to IC1c goes to zero. This allows any triggering pulses from TR1, C5, D2 and VR3 caused by a load being put on
the battery to set the output of the R-S flipflop IC2a, IC2b to logical one.

After another delay, caused by VR2/C4 monostable IC2c, IC2d is triggered, enabling the astable multivibrator IC3a, IC3b and thus producing pulsed operation of the horn via TR2, TR3, D6 and relay RLA.

\section*{TRIGGER GUARD}

Triggering of the monostable causes flipflop IC2a, IC2b to be reset via IC3c, IC3d. R4, C3 cause the reset to IC2b to be held for a short interval after the end of the monostable timing cycle to prevent retriggering of the alarm by the horn or relay RLA.

Disabling of the alarm resets both the flip-flops and the monostable.

All i.c.s are CMOS 4001 quad 2 -input NOR gates. D4 protects the circuit against incorrect supply polarity which would quickly destroy the i.c.s. The contacts of RLA must be fairly substantial, as they carry the full horn current.

VR1, VR2 were set to give exit and entry delays of 80 seconds and 15 seconds respectively. R9, C6 gave an alarm time of about 3.5 minutes, at a frequency (governed by R10, C7) of 0.4 Hz .
\begin{tabular}{cl} 
Resistors & \\
R1, R2 & \(1 \mathrm{M} \Omega\) (2 off) \\
R3 & \(1 \mathrm{k} \Omega\) \\
R4 & \(470 \mathrm{k} \Omega\) \\
R5 & \(1 \mathrm{k} \Omega\) \\
R6 & \(1 \mathrm{M} \Omega\) \\
R7, R8 & \(1 \mathrm{k} \Omega(2\) off) \\
R9 & \(10 \mathrm{M} \Omega\) \\
R10 & \(4.7 \mathrm{M} \Omega\) \\
All \(10 \% \frac{1}{2} \mathrm{~W}\) carbon \\
& \\
Capacitors & \\
C1 & \(150 \mu \mathrm{~F}\) elect 25 V \\
C2 & \(150 \mu \mathrm{~F}\) elect 16 V \\
C3 & \(4.7 \mu \mathrm{~F}\) elect 63 V \\
C4 & \(150 \mu \mathrm{~F}\) elect 16 V \\
C5 & \(0.1 \mu \mathrm{~F}\) \\
C6 & \(22 \mu \mathrm{~F}\) elect 16 V \\
C7 & \(0.33 \mu \mathrm{~F}\)
\end{tabular}

\section*{Potentiometers}

VR1, VR2 \(1 \mathrm{M} \Omega\) miniature preset (2 off)
VR3 \(100 \mathrm{k} \Omega\)
miniature preset

Semiconductors
IC1-IC3 CD4001 (3 off)
TR1-TR3 BC108 (3 off)
D1-D3 1 N4148 (3 off)
D4, D6 1N4001
D5, D7 1N4148

\section*{Miscellaneous}

S1-Single pole double throw switch
RLA \(-12 \mathrm{~V}, 110 \Omega\) (R.S. 348-835)


Circuit of Intruder Alarm

\title{
BATTERY STATE INDICATOR
} generator.
 granted, rarely giving it the maintenance it requires. As the winter nights advance the demands made on this vital power source increase. When you combine this with the inevitable ageing process and the diminishing ability to store a charge for a long period, the requirement for a simple aid to continuous battery voltage monitoring is obvious.

The indicator was therefore designed to forestall any incipient failure by providing "at a glance" information on battery state with three coloured l.e.d.s; green indicating a battery voltage adequate for normal use; yellow, that the voltage is fairly low and red that there is a failure in the electrical system, such as a dead cell, poor connection, defective regulator or

An upper and lower battery voltage limit is set by selection of two Zener diodes which allow the transistors to be turned on at set points. These are in turn interconnected via a conventional diode and l.e.d.s to give a display of the state of the car's battery.

When the car's battery is in top condition, its output voltage will be around 14 V and of course even higher when charging. This potential is applied, via D8 (reducing it by some 0.8 V ), through R5. D7 and R6 to the base of TR2 which will be turned "on" causing D6 to illuminate via R4. TR2 at this time, effectively places a short-circuit across the rest of the circuit via D5 preventing D2 and D3 from emitting light as the potential across them is only some 2 V .

As the battery voltage becomes lower, TR2 begins to turn off as the threshold of D7 is reached. This allows D2 to start to come on as TR1 has all the time been turned on via R1, D1, R2. The current thus drawn via R3 precludes D3 from illuminating as the potential across it and D4 is not above the Zener level.

Eventually, at still lower battery voltage, TR 1 will begin to turn off in the same manner as for TR2, allowing the potential at the junction of D2, D3, D5 to rise in excess of the 5 V Zener level of D4 which begins to pass current and illuminates D3.

Zener diodes may be selected for other switching points and/or battery voltages.

\section*{COMPONENTS}
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{Resistors} \\
\hline R1/R5 & \(1 \mathrm{k} \Omega\) \\
\hline R2/R6 & \(8.2 \mathrm{k} \Omega\) \\
\hline R3/R4 & \(470 \Omega\) \\
\hline All \(\frac{1}{2} \mathrm{~W} 10\) & \% carbon \\
\hline \multicolumn{2}{|l|}{Semiconductors} \\
\hline TR1, TR2 & BFY50 (2 off) \\
\hline D1 & BZY88-9.1 \\
\hline D2, D3 & TIL209 (Yellow, red) \\
\hline D4 & BZY88-5.1 \\
\hline D5 & 1 N4001 \\
\hline D6 & TIL209 (Green) \\
\hline D7 & BZY88-12 \\
\hline D8 & 1N4001 \\
\hline
\end{tabular}

Battery
Voltage (Vb)
\(\mathrm{Vb} \leqslant 10 \mathrm{~V}\)
\(10 \mathrm{~V}<\mathrm{Vb}<12 \mathrm{~V}\)
\(\mathrm{Vb} \geqslant 12 \mathrm{~V}\)

\section*{L.e.d. Illuminated}

Red (D3)
Yellow (D2)
Green (D6)

\section*{POLARITY INVERTER}

\section*{C. D. Williams}

THE circuit illustrated was originally designed to enable a negative earth eight-track player to be used in a car with a positive earth, but other uses are obvious, since polarity is reversible.

\section*{CIRCUIT}

Diode D1 is arranged to prevent incorrect connection to supply. D2 and 3 increase the \(V_{b e}\) ratings of TR1 and 2 which are connected as a multivibrator operating at about 700 Hz .

The output of this is buffered by the AD161 which drives the transformer T1. This must be a low voltage (12V) high current ( \(\sim 1 A\) ) one to one transformer, which are rare and expensive. The solution was to use a low voltage mains transformer with individual 12 V secondaries and ignore the primary and use the two secondaries. Components D4-8, C3, R5 and TR4 rectify and stabilise the output at 12.6 V which is floating relative to the supply rails.


COMPONENTS


\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{2}{|l|}{Edge Connector 1} & pin 13 ' & U3 Patch Panel & Edge & ector 6 \\
\hline From & To & pin 14 & U2 Patch Panel & From & To \\
\hline pin 3 & A3 Patch Panel & pin 15 & TB9 Terminal Block & pin 3 & -15V Supply \\
\hline pin 4 & Earth & pin 16 & VR59 & pin 4 & S2c Common \\
\hline pin 5 & A2 Patch Panel & pin 17 & Edge Connector 5 pin 27 & pin 5 & S1c Common \\
\hline pin 6 & -15V Supply & pín 18 & W5 Patch Panel & pin 9 & TB1 Terminal Block \\
\hline pin 7 & A4 Patch Panel & pin 19 & W4 Patch Panel & in 10 & S1b Add \\
\hline pin 8 & Edge Connector 6 pin 10 & pin 20 & W3 Patch Panel & pin 11 & S2b Add \\
\hline pin 9 & C5 Patch Panel & pin 21 & W2 Patch Panel & pin 12 & TB2 Terminal Block \\
\hline pin 10 & C4 Patch Panel & pin 22 & TB10 Terminal Block & pin 12 & TB2 Terminal Block \\
\hline pin 11 & C3 Patch Panel & pin 23 & VR60 & pin 13
pin 14 &  \\
\hline pin 12 & C2 Patch Panel & pin 24 & X2 Patch Panel & pin 15 & S4b Add \\
\hline pin 13 & TB1 Terminal Block & pin 25 & \(\times 4\) Patch Panel & pin 16 & TB4 Terminal Block \\
\hline pin 14 & VR51 & pin 27 & X3 Patch Panel & pin 17 & TB5 Terminal Block \\
\hline pin 15 & Edge Connector 6 pin 11 & & & pin 18 & S5b Add \\
\hline pin 16 & E5 Patch Panel & \multicolumn{2}{|l|}{Edge Connector 4} & pin 19 & S5a Common \\
\hline pin 17 & E4 Patch Panel & From & To & pin 20 & S4c Common \\
\hline pin 18 & E3 Patch Panel & pin 2 & +15V Supply & pin 21 & S3c Common \\
\hline pin 19 & E2 Patch Panel & pin 3 & VR51 & pin 22 & S11a Compute \\
\hline pin 20 & TB2 Terminal Block & pin 4 & B6 Patch Panel & pin 23 & TB2 Terminal Block \\
\hline pin 21 & VR52 & pin 5 & S1d Add & pin 24 & TB1 Terminal Block \\
\hline pin 22 & Edge Connector 6 pin 14 & pin 6 & B5 Patch Panel & pin 28 & Earth, Edge Connector 7 pin 3 \\
\hline pin 23 & G5 Patch Panel & pin 7 & C6 Patch Panel & pin 28 & Earth, Edge Connector 7 pin 3 \\
\hline pin 24 & G4 Patch Panel & pin 8 & VR52 & & \\
\hline pin 25 & G3 Patch Panel & pin 9 & D6 Patch Panel & Edge & nector 7 \\
\hline pin 26 & G2 Patch Panel & pin 10 & S2d Add & From & To \\
\hline pin 27 & TB3 Terminal Block & pin 11 & D5 Patch Panel & pin 1 & S1a Integrate \\
\hline pin 28 & VR53 & pin 12 & E6 Patch Panel & pin 2 & S2a Integrate \\
\hline & & pin 13 & VR53 & pin 3 & Edge Connector 7 pin 4 \\
\hline \multicolumn{2}{|l|}{Edge Connector 2} & pin 14 & F6 Patch Panel & pin 4 & Edge Connector 7 pin 7 \\
\hline From & To & pin 15 & S3d Add & pin 5 & S3a Integrate \\
\hline pin 1 & Edge Connector 6 pin 15 & pin 16 & F5 Patch Panel & pin 6 & S4a integrate \\
\hline pin 2 & J5 Patch Panel & pin 17 & G6 Patch Pane & pin 7 & Edge Connector 7 pin 8 \\
\hline pin 3 & J4 Patch Panel & pin 18 & VR54 & pin 8 & Edge Connector 8 pin 9 \\
\hline pin 4 & J3 Patch Panel & pin 19 & H6 Patch Panel & pin 9 & S5a Integrate \\
\hline pin 5 & J2 Patch Panel & pin 20 & S4d Add & pin 10 & TB5 Terminal Block \\
\hline pin 6 & TB4 Terminal Block & pin 21 & H5 Patch Panel & pin 11 & TB4 Terminal Block \\
\hline pin 7 & VR54 & pin 22 & J6 Patch Panel & pin 12 & TB3 Terminal Block \\
\hline pin 8 & Edge Connector 6 pin 18 & pin 23 & VR55 & pin 13 & S7c Common \\
\hline pin 9 & L5 Patch Panel & pin 24 & K6 Patch Panel & pin 14 & S6c Common \\
\hline pin 10 & 14 Patch Panel & pin 25 & S5d Add & pin 18 & TB6 Terminal Block \\
\hline pin 11 & L3 Patch Panel & pin 26 & K5 Patch Panel & pin 19 & S6b Add \\
\hline pin 12 & L2 Patch Panel & pin 27 & L6 Patch Panel & pin 20 & S7b Add \\
\hline pin 13 & TB5 Terminal Block & & & pin 21 & TB7 Terminal Block \\
\hline pin 14 & VR55 & \multicolumn{2}{|l|}{Edge Connector 5} & pin 22 & TB8 Terminal Block \\
\hline pin 15 & Edge Connector 5 pin 19 & From & To & pin 23 & S8b Add \\
\hline pin 16 & N5 Patch Panel & & & pin 24 & S9b Add \\
\hline pin 17 & N4 Patch Panel & & & pin 25 & TB9 Terminal Block \\
\hline pin 18 & N3 Patch Panel & & & pin 26 & TB10 Terminal Block \\
\hline pin 19 & N2 Patch Panel & \begin{tabular}{l}
pin 3 \\
pin 4
\end{tabular} & M6 Patch Panel & pin 27 & S10b Add \\
\hline pin 20 & TB6 Terminal Block & pin 5 & M5 Patch Panel & pin 28 & S10c Common \\
\hline pin 21 & VR56 & pin 6 & N6 Patch Panel & & \\
\hline pin 22 & Edge Connector 5 pin 20 & pin 7 & VR57 & Edge & nector 8 \\
\hline pin 23 & 05 Patch Panel & pin 8 & P6 Patch Panel & & To \\
\hline pin 24 & 04 Patch Panel & pin 9 & S7d Add & & \\
\hline pin 25 & 03 Patch Panel & pin 10 & P5 Patch Panel & pin 1 & S9c Common \\
\hline pin 26 & 02 Patch Panel & pin 11 & Q6 Patch Panel & pin 2 & S8c Common \\
\hline pin 27 & TB7 Terminal Block & pin 12 & VR58 & & +15V Supply \\
\hline pin 28 & VR57 & pin 13 & R6 Patch Panel & pin 4 & TB7 Terminal Block \\
\hline \multicolumn{2}{|l|}{\multirow[b]{2}{*}{Edge Connector 3}} & pin 14 & S8d Add & pin 9 & Edge Connector 8 pin 12 \\
\hline & & pin 15 & R5 Patch Panel & pin 10 & S6c Integrate \\
\hline From & To & pin 16 & S6 Patch Panel & pin 11 & S7a Integrate \\
\hline pin 3 & Edge Connector 5 pin 23 & pin 17 & VR59 & pin 12 & Edge Connector 8 pin 13 \\
\hline pin 4 & S5 Patch Panel & pin 18 & T6 Patch Panel & pin 13 & Edge Connector 8 pin 16 \\
\hline pin 5 & S4 Patch Panel & pin 19 & S9d Add & pin 14 & S8a Integrate \\
\hline pin 6 & S3 Patch Panel & pin 20 & T5 Patch Panel & pin 15 & S9a Integrate \\
\hline pin 7 & S2 Patch Panel & pin 21 & U6 Patch Panel & pin 16 & Edge Connector 8 pin 17 \\
\hline pin 8 & TB8 Terminal Block & pin 22 & VR60 & pin 18 & S10a Integrate \\
\hline pin 9 & VR58 & pin 23 & V6 Patch Panel & pin 19 & TB10 Terminal Block \\
\hline pin 10 & Edge Connector 5 pin 24 & pin 24 & S10d Add & pin 20 & TB9 Terminal Block \\
\hline pin 11 & U5 Patch Panel & pin 25 & \(V 5\) Patch Panel & pin 21 & TB8 Terminal Block \\
\hline pin 12 & U4 Patch Panel & pin 26 & W6 Patch Panel & pin 22 & Reset Switch (S12) \\
\hline
\end{tabular}

\section*{Edge Connector 2}

From To
Edge Connector 6 pin 15
pin 3 J4 Patch Panel
pin 4 J3 Patch Panel
pin 6 TB4 Terminal Block
pin \(7 \quad\) VR54
pin \(8 \quad\) Edge Connector 6 pin 18
L5 Patch Pane
in 10 Patch Panal
L. 2 Patch Pane
pin 13 TB5 Terminal Block
pin 15 Edge Connector 5 pin 19
pin 16 Patch Panel
pin 17 N4 Patch Panel
N3 Patch Panel
pin 20 TB6 Terminal Block
pin 21 VR56
Edge Connector 5 pin 20
in 24 Pat Panel
pin 25
pin 26 Q2 Patch Panel
pin 27 TB7 Terminal Block

Edgé Connector 3
From To
pin 3 Edge Connector 5 pin 23
pin 6
pin 7 S2 Patch Panel
pin 8 TB8 Terminal Block
pin 10 Edge Connector 5 pin 24
pin 13
- 15
pin 16
pin 17
pin 19
pin 20
pin 22
pin 23
Pin 25
pin 27

\section*{Edge Connector 4 \\ To \\ pin 3 VR5 \\ pin 4 \\ in 6 \\ pin 7 \\ pin 8 \\ pin 10 \\ in 12 \\ pin 13 \\ pin 14 \\ pin 16 \\ pin 17 \\ pin \\ pin 20 \\ pin 21 H5 Patch Panel \\ pin 23 VR55 \\ K6 Patch Panel \\ pin 26 K5 Patch Panel}

Edge Connector 5
From To
pin. \(2 \quad\) VR56

S6d Add
pin
pin
pin 10
Q6 Patch Panel
pin 13 R6 Patch Panel
8 d Add
R5 Patch Panel VR59
pin 18 T6 Patch Panel
pin 19 S9d Add
6 Patch Panel
pin 22 VR60
pin \(25 \quad\) V5 Patch Panel
pin 26 W6 Patch Panel

\section*{Edge Connector 6}

From To
15 V Supply
pin 5 S1c Common
pin 9 TB1 Terminal Block
pin 12 TB2 Terminal Block
pin 13 TB3 Terminal Block
pin 15 Sbb Add
TB4 Terminal Block
TB5 Terminal Block
b Add
S4.

S11a Compute
TB2 Terminal Block
Earth, Edge Connector 7 pin 3

\section*{Edge Connector 7}

To
pin 2 S2a Integrate
pin \(3 \quad\) Edge Connector 7 pin 4
pin 5 S3a integrate
S4a integrate
Edge Connector 7 pin 8 Edge Connector 8 pin 9
S5a Integrate
TB4 Thmial Block
TB3Termial Black
S7c Common
TB6 Terminal Block
S6b Add
TB7 Terminal Block TB8 Terminal Block S8b Add

TB9 Terminal Block TB10 Terminal Block S10b Add S10c Common

Edge Connector 8

SAc 2 Common
(nin +15 V Supply
TB7 Terminal Block Edge Connector 8 pin 12 S6c Integrate Edge Connector 8 pin 13 Edge Connector 8 pin 16 S8a Integrate Edge Connector 8 pin 17 S10a Integrate TB10 Terminal Block B8 Termina Reset Switch (S12)

Fig. 3.3. Wiring Schedule

\section*{Wiring Schedule-cont.}

\section*{From}

S1b, S1d Common
S2b, S2d Common S3b, S3d Common S4b,S4d Common S5b, S5d Common S6b, S6d Common S7b, S7d Common S8b, S8d Common S9b, S9d Common S10b, S10d Common Reset Button (S12) S11a S11b -15V Supply VR51 Wiper

To
TB1 Terminal Block TB2 Terminal Block TB3 Terminal Block TB4 Terminal Block TB5 Terminal Block TB6 Terminal Block TB7 Terminal Block TB8 Terminal Block TB9 Terminal Block TB10 Terminal Block S11b Compute +15 V Supply -15V Supply VR51 Wiper
VR52, 53, 54, 55,56, 57, 58, 59, 60 (Wipers)


Fig. 3.4. Layout arrangements for edge connectors, patch panel and switches

\section*{MODE CONTROL TEST}

Set amplifier A1 to "integrate", and the mode to "compute" and monitor the output with one of the meters. Apply a voltage to a \(\times 1\) input. The needle should deflect gradually in the positive direction, if the applied input voltage is negative, and vice-versa, until the amplifier saturates. When this happens, adjust the meter sensitivity so that the needle is at maximum deflection. Put the computer in the "hold" mode and press the "reset" switch. The needle should go to zero. Release "reset" and switch to "compute". The needle will again start to deflect and this time switch the mode to "hold" before the amplifier saturates. The needle should then stop moving. Carry out this test with all the amplifiers. While doing this, observe the operation of the overload warning circuit. The appropriate l.e.d. should come on when the amplifier output exceeds +11 V or goes below -11 V . Check both positive and negative operation by applying both positive and negative input voltages.

The above tests are not complete by any means but any remaining problems will show up when the examples described under "programming" are attempted.

\section*{COMPONENTS}

Resistors
R6, R7 \(100 \mathrm{k} \Omega \frac{1}{4} \mathrm{~W}\) carbon (2 off)
Potentiometers
VR41-VR48 \(100 \mathrm{k} \Omega\) linear ( 8 off)
VR49-VR50 \(300 \mathrm{k} \Omega\) linear (2 off)

\section*{Miscellaneous}

1 off d.p.d.t. switch (R.S. type 316-793)
20 off d.p.d.t. sub-min slide switch
2 off \(50-0-50 \mu \mathrm{~A}\) (ME15 T40 Watford Electronics)
1 off Push button (R.S. type 337-914)
151 off Square 4 mm panel mounted sockets ( 55 red, 32 yellow, 22 green, 21 white, 21 black)
8 off Skirted knob
12 off Plain knob
6 off 28 way edge connector 0.1 in matrix
2 off 28 way edge connector 0.15 in matrix Banana plugs (as required)

\section*{PROGRAMMING}

It has already been mentioned, that it is necessary to form a mathematical model of the problem to be solved and the computer cannot help us to do this, but being very faithful however, it will happily try to solve a problem even if the wrong information is fed into it. Fortunately, in such cases the programmer could get an indication that something had gone wrong by studying the results which are usually meaningless. The general rule "'Garbage In, Garbage Out" (well known to digital computer programmers) applies here also. Unfortunately, error checks cannot be incorporated in the analogue programs, as is the case with digital programs. It is important therefore to adopt a methodical procedure for programming to avoid errors.

Having formed the mathematical model, the equations are rearranged and a flow diagram is constructed which satisfies the equations. All values to be input and all computing elements to be used, are marked on the flow diagram to avoid confusion, Referring to the diagram the computer is then programmed by patching the panel. This procedure will be illustrated by several examples. The flow diagrams are constructed using standard symbols representing computing elements. Some of these have already been given. Fig. 3.5 shows all the symbols to be used in this article.


Fig. 3.5. Computing element symbols: (a) coefficient multiplier; (b) Four quadrant multiplier; (c) Summer; (d) Integrator with initial conditions.

As a first example let us examine the operation of potentiometers, adders and integrators, using simple experiments.

Apply a reference voltage to the input of \(P 1\) and connect the output to \(M 1\). Adjust the sensitivity of \(M 1\) so that when P1 is at maximum, M1 deflects fully. Operate the potentiometer and observe the results.

Switch the power on and calibrate M1 by applying a known voltage (e.g. supply voltage), to read 15 V at full deflection. Switch A1 to "add" and apply the output of P1 to the input of \(A 1\) and the output of \(A 1\) to \(M 1\). The flow diagram and patch panel connections are shown in Fig. 3.6. Test all A1 inputs in turn and observe the gain of the adder each time.


Fig. 3.6. Flow diagram and patch panel layout for the potentiometer example

To examine the operation of the integrators, we can integrate various functions and study the results. First let us see what happens when we integrate a constant, \(C\). The mathematicians will immediately give us the answer as C.t + \(K\), where \(t\) is the variable (time in this case) and \(K\) is another constant. This is a straight line, of gradient C and passing through the origin, if we have no initial conditions, i.e. \(\mathrm{C}=0\) at \(\mathrm{t}=0\). To verify this we can set up the program shown in Fig. 3.7.



Fig. 3.7. Flow diagram and patch panel layout for the integration example

To run this program follow these steps:
(1) Check A1 is in "integrate"
(2) Computer mode: "hold"
(3) Switch power on
(4) Press reset for a few seconds and release
(5) Switch to "compute" and observe the meter.

Vary the value of \(C\) by adjusting \(P 1\) and repeat the above steps. If an \(X-Y\) plotter is available the results can be plotted for different values of \(C\). The graph would look like Fig. 3.8. With \(C\) set to 1 volt the output should increase at 1 volt per second ( \(C=C . t\) ). This can be verified by timing the deflection of the needle.


Fig. 3.8. Graph showing the resultant curves when various values for the constant \(\mathbf{C}\) are integrated

These examples serve to illustrate the use of the analogue computer as a function generator. By integrating a step function we obtained a ramp function, the slope of which we could easily control. The ramp function can be integrated again to produce a square law function. This is shown in the flow diagram in Fig. 3.9. Still higher power functions can be obtained by successive integrations.


Fig. 3.9. By integrating waveforms the analogue computer can be used as a function generator

\section*{INITIAL CONDITIONS EXAMPLE}

In the previous integrator examples we assumed that at time \(t=0\) all variables had zero value. Suppose that we wanted to give a value to the output of the integrator, before the computation begins. It is not difficult to imagine examples where this might be used. We may for example like to investigate the flight of a rocket, not from the point of launch but from some height above the launching pad, at which the rocket will have some velocity and acceleration. To illustrate the use of initial conditions we can repeat the first integrator example, but this time we are going to give an initial value to the integrator output of 5 V . We therefore
require 5 V to be applied to the initial condition socket of A 1 . Since the value of the reference voltages is only about 1.5 V , we shall have to multiply this value. This we can do with the aid of an adder and a potentiometer. The flow diagram and patch panel connections are shown in Fig. 3.10.


Fig. 3.10. Flow diagram and patch panel layout for the initial condition example

To run this program follow these steps after the panel has been patched.
(1) Switch power on
(2) Amplifier A1 integrating and A2 adding
(3) Computer mode: "hold"
(4) Monitor A2 output and adjust to 5 V using P2
(5) Set output of P 1 to 1 V
(6) Press "reset" for a few seconds and release (Output of A1 should now show 5 V )
(7) Switch mode to "compute" and observe M1.

The initial condition value is invariably formed using an adder and a potentiometer, unless of course the exact value is available. It is therefore common practice not to show these two computing elements, but simply to note the value being applied to the initial condition socket as shown in Fig. 3.11 .


Fig. 3.11. Initial condition symbol
Another point worth noting here is that it is not essential for the potentiometer to precede the adder as shown in the flow diagram. In fact in such cases it is better for the amplifier to precede the potentiometer, as the former presents a higher input impedance to the battery than the latter and therefore saves battery energy.

\section*{ENGINEERING PROBLEMS}

Consider a mass \(M\) supported on a spring of stiffness \(K\). If the mass is disturbed, the system will begin to oscillate about the equilibrium position. Mechanical systems usually have electrical equivalents or vice-versa. The electrical equivalent to the spring mass system is the capacitor inductor series circuit. Both systems are shown in Fig 3.12.

The equation of motion of the spring mass system is \(M \ddot{x}\) \(+K x=0\). The electrical system is described by a similar


Fig. 3.12. The mechanical spring/mass circuit and its electrical equivalent the inductor/capacitor series circuit
equation but with electrical symbols substituted for the mechanical ones. The "dot" notation is used where time derivatives are involved. For example, one dot means the first derivative of the variable in question, with respect to time, two dots mean the second derivative and so on. So if \(x\) represents displacement, then \(\dot{x}\) represents velocity, and \(\ddot{x}\) acceleration. The equation can be rearranged so that the highest derivative appears on the left-hand side, with everything else on the right-hand side. This is normal practice when solving a problem on the analogue computer. The equation becomes \(\ddot{x}=-\frac{K}{M} \times\) and the flow diagram is shown in Fig. 3.13.


Fig. 3.13. Flow diagram and patch panel layout for the spring/mass example

By integrating \(\ddot{x}\) twice we obtain \(-\dot{x}\) and \(x\). In our equation, however, we require \(-x\) and so \(A 3\) is used as a sign inverter. The value \(K / M\) is set up on potentiometer \(P 1\), the output of which becomes \(-K / M . x\). This is equal to \(\ddot{x}\) and therefore we can close the loop by connecting the output of P1 back to the input of A1. The system as it stands will not vibrate unless it is disturbed. Theoretically once it is disturbed, it should go on vibrating for ever. In practice, however, we know that this is not true, because of the presence of some damping, due to air resistance in the case of the mechanical system and electrical resistance in the case of the electrical system. The analogue computer should produce results very near to the theoretical predictions, i.e. very little damping should be present. To run this program follow these steps.
(1) Check A1 and A2 are integrating and A3 is adding.
(2) Switch power on.
(3) Switch mode to "compute".
(4) Apply a disturbance to the input of A2 or A3. (This can be done by momentarily touching the input socket, with a wire lead connected to a reference voltage socket. This is equivalent to giving the weight a gentle push.)
(5) Observe the meters and adjust the sensitivity to produce a reasonable needle deflection.
(6) Operate P1 and see what happens to the frequency and amplitude of oscillation.
You should find that a high value of \(K / M\) (i.e. high spring stiffness or small mass or both) gives a high frequency and vice versa. The other point to note is that the oscillation is sinusoidal. The output of A1 (i.e. the velocity) is a cosine function, whereas that of A2 (the displacement) is a sine


Fig. 3.14. Graph showing the phase difference between velocity and displacement
function. There is a phase difference of 90 degrees between the velocity and the displacement. (The mass comes to a momentary stop when the displacement is at a maximum.) This is shown in the graph in Fig 3.14.

In this last example we have seen how the analogue computer can be used as a function generator for sine or cosine functions, with variable frequency. The frequency of oscillation is given by
\[
f=\frac{1}{2 \pi} \sqrt{\frac{K}{M}} \mathrm{~Hz} \text { (cycles per second) }
\]

This can be checked by counting the number of cycles in one minute and dividing by 60 to convert to cycles per second. If the value of \(P 1\) is set to 1.0 and the input of \(A 1\) is multiplying by 10 then \(\mathrm{K} / \mathrm{M}=10\) and the frequency should be \(\mathrm{f}=1 / 2 \sqrt{ } 10=0.503 \mathrm{~Hz}\).

\section*{NEXT MONTH: PROGRAMMING AND SPECIAL CIRCUITS (conclusion of series)}


\author{
by Mike Abbott
}

\section*{BUBBLING WITH BITS}

THe IDEA of the magnetic bubble conjures up a picture of quivering clusters gurgling their way to the North Pole. In fact powerful magnetic bubble memories are about to "pop" onto the scene from at least two major electronics manufacturers in the near future, one of which is Texas Instruments.

Sample quantities of a new quarter-million-bit bubble memory will be available from T.I. before the end of this year, but at \(\$ 500\) each there probably won't be many P.E. constructors in the queue. (A 92 k --bit bubble memory is now in volume production at a price of \(\$ 100\) in 100 unit quantities). The big one however, designated the TIB0303, is full of three micron diameter magnetic bubble domains, and uses separate I/O, minor loop architecture, and features block replication of data. Separate read and write tracks with minor loop data storage are at the heart of this block replicate-based architecture to provide improved performance.

A total of 252 minor loops, each consisting of 1,137 bubble positions, results in a single-chip memory capacity of 286,524 bits. However, 224 loops are utilised resulting in a minimum data capacity of 254,688 bits.

Data bits are written into the write track and exchanged with stored data in the minor loops via swap gates. Data blocks are replicated simultaneously at minor loop and output track junctions, rather than serial duplication which is characteristic of major/minor loop architecture. Consequently, power-down cycle time is significantly reduced from 12.8 milliseconds in the 92 K -bit major/minor loop configuration to 12.5 microseconds for block replicate, representing three orders of magnitude improvement.

Other key features include: advanced asymmetric chevron design for improved bubble propagation and transfer, merged data that allows a continuous flow of data bits at the read track, and a dedicated loop for storage of on-chip redundancy information and address synchronisation.

Performance specifications at 100 kilohertz operation are an average access time of 7.3 milliseconds for the first bit of the 224-bit page and a typical power consumption of 0.9 watt for continuous operation. A data-merge function allows a read data of 100 K bits per second. Operating temperature is \(0^{\circ}\) to \(50^{\circ} \mathrm{C}\) with non-volatile storage range of \(-40^{\circ}\) to \(85^{\circ} \mathrm{C}\).

Bubble control functions are executed by providing current pulses through the appropriate control element on the chip.

The bubble chip is comprised of a gadolinium-gallium garnet substrate upon which a magnetic epitaxial film is grown. Patterns of permalloy metal are deposited on the epitaxial film to define the path of the bubble domains in the presence of a rotating magnetic field. As the field rotates, the bubble domains move under the permalloy pattern in shift register fashion.

The TIB0303 will be offered in a 20-pin dual-in-line package, measuring \(30 \times 30 \times 10 \mathrm{~mm}\). The package contains the quarter-millionbit bubble chip surrounded by two orthogonal coils that provide the rotating magnetic field, a permanent magnet set, and a magnetic shield to protect data from external fields.

Taking a systems approach, TI will offer a family of interface and control circuits for the TIB0303 in the second quarter of 1979.

\section*{BLINKING GOOD}
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Available from the Norbain Optoelectronics Division is the first Flashing Light Emitting Diode, Type FRL 4403, to appear on the market. The T \(1 \frac{3}{4}\) l.e.d. is manufactured in Gallium Arsenide Phosphide technology with a red diffused plastic lens. The built-in integrated circuit flashes the l.e.d. on and off at roughly 3 pulses per second, and can be driven directly by standard TTL and CMOS devices, eliminating the need for external switching circuitry.

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The l.e.d. gives a large full flood radiating area, wide viewing angle and finds application as a condition warning light, monitoring process control system and in many other applications where warning of failure is essential.

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\section*{ON THE LEVELL}

THE very popular and stout a.c. microvolt meters, type TM3B, made by Levell Electronics Ltd., have just been upgraded.
The improvements include increased input impedance and meter scale length. A brief specification follows:

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RESPONSE: \(\pm 3 \mathrm{~dB}\) from 1 Hz to \(3 \mathrm{MHz}, \pm 0.3 \mathrm{~dB}\) from 4 Hz to 1 MHz above \(500 \mu \mathrm{~V}\).

INPUT IMPEDANCE: Above \(50 \mathrm{mV}: 10 \mathrm{M} \Omega<20 \mathrm{pf}\). On \(50 \mu \mathrm{~V}\) to \(50 \mathrm{mV}:>5 \mathrm{M} \Omega<50 \mathrm{pf}\).

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A selection of readers' original circuit ideas. It should be emphasised that these designs have not been proven by us. not been proven by us.
They will at any rate They will at any rate
stimulate further thought. Why not submit your idea? Any idea published will be awarded payment according to its merits.

Articles submitted for publication should conform to the usual practices of this journal, e.g. with regard to abbreviations and circuit symbols. Diagrams should be on Diagrams should be on serted in the text.

Each idea submitted must be accompanied by a declaration to the effect that it is the original work of the undersigned, and that it has not been accepted for publication elsewhere.
\(\rightarrow \mathrm{mb}\)


\section*{741 SUPPLY}

WHEN two independent power supplies are used to run 741 circuits, problems can arise if one is loaded more than the other. This is particularly so if the circuits use reference voltages taken from the supply rails, e.g. the comparator in Fig. 1.

The power supply circuit shown (Fig. 2) avoids this by using a negative feedback loop; a 741 sensing the mid-voltage between the two supply rails and controlling the voltage at the bases of the transistor pairs. This feedback keeps the point "A" at zero volts so, provided that the two sensing resistors (R6 and R7) are equal, the two output voltages are equal and opposite.

In the circuit tested AD161, 162 and AC 127, 128 transistors were used which could give a \(\frac{1}{2}\) amp supply.
M. G. Kiff,

Wallingford, Oxon.


Fig. 1


Fig. 2

\section*{SOLDERING IRON SIMMER CONTROL}

WHEN soldering intermittently it is annoying to wait for the iron to heat up each time, while leaving it on uses up both the bit and electricity. This circuit supplies half power to keep the iron just warm, giving rapid rise to full temperature.

A common type of switched 13A plug is used with a rectifier in parallel with the switch. The rectifier (type 1 N 4004 is suitable) is soldered, either way round. The neon is left connected as before, giving full and half brightness to indicate power selected.


\section*{L.F. FREQUENCY METER}

THIS instrument is capable of measuring frequencies in the range 10 Hz to 100 kHz . Four switched ranges are available, these being:
1. \(0-100 \mathrm{~Hz}\)
2. \(0-1 \mathrm{kHz}\)
3. \(0-10 \mathrm{kHz}\)
4. \(0-100 \mathrm{kHz}\)

The meter scale is linear to facilitate reading the frequency. The power consumption is 9 V at 10 mA , and this may be conveniently supplied from a battery.

The first stage of the circuit is an LM311 comparator which converts the input waveform into a square-wave. The LM311 i.c. was chosen because of its low input current and because of its ability to run off a single supply. The output of this i.c. is then fed to the 555 which is connected as a monostable. Hence, the average voltage at the output of IC2 is directly proportional to the frequency at its input. The length of the pulses from the 555 depends on the value of C3 and R6, R7, R8 or R9.

The output of IC2 is fed first to a 5.6 V Zener diode via a current limiting resistor. This has the effect of preserving instrument accuracy despite fluctuations in supply voltage. The output from the Zener is then fed to the meter. VR1, a preset potentiometer, is adjusted to calibrate the instrument.

Finally, components that govern the pulse length should be high quality types R6-R9 need to be \(2 \%\) or better, and C3 must be a 5\% polycarbonate type.
D. P. Akerman,

Dagenham,
Essex.


\section*{AUTO-TUNE GENERATOR}


THIS circuit enables a preset series of 10 notes to be played over and over again.

With this basic operation, possible applications could be: novel doorbells; background to music synthesis; audiovisual displays, etc. IC1 (CD4017A) is a decade counter which counts one on each positive transition of a clocking oscillator. That is, it applies a high signal to D1, then D2, then D3 and so on up to D10. Depressing S1 resets the counter.

Each note is set by adjusting the current drawn from a particular output (D1 to D10), with VR4-13. A l.e.d. is placed on each output to indicate which note is being
played at that moment; they are optional and can be omitted (tuning is much harder without the l.e.d.s). The varying current taken by IC 1 , as it counts along the preset notes, is monitored by TR2 and R1 which convert the current into a corresponding, changing voltage. TR1 amplifies this and presents it to an audio VCO. VR1 varies the range of notes over which each preset note can be tuned.

IC2 forms the VCO from a CD4007A, IC2a, b being the audio oscillator tuned manually with VR2. IC2c, which is a CMOS f.e.t., is in parallel to VR2 and R4 and so a changing potential on the f.e.t.'s gate will cause a changing frequency.

VR 14 then attenuates the output signal for an amplifier.

The clock oscillator is a CD4000A (IC3) and oscillates from about 0.2 Hz to 5 Hz -fully variable with VR3. S2 will stop the oscillator (a tuning aid), and D1I and R8 ensure that the oscillator's fluctuating current doesn't affect the VCO's steady tone.

Finally, C2 can be added for an interesting effect. The whole unit will run from a small 9V battery. IC1, 2 and 3 are CMOS and should be handled with care.
T. D. Davey,

Berkhamsted,
Herts.

\section*{TOUCH TUNER}

T
HE circuit shown forms a simple "touch tuner" for use with varicap devices. It is based on the CMOS integrated circuit MC14514 which is a 4 line to 16 line latch/decoder, so up to 16 channels can be switched (if only 8 are required input \(D\) can be grounded as shown).

When the strobe input is high the BCD inputs to the i.c. are encoded as 1 of 16 outputs.
The touch buttons are decoded by the diodes to produce the BCD pattern, at the same time pulling the strobe input high (STR). This selects one of the 16 outputs which drive up to almost \(V_{d d}\) which is in turn divided down, by preset potentiometers, to give the tuning voltage that is applied to the tuner via the isolating diodes.

When the touch button is released the state at the BCD input is retained for a short time by the capacitors C2-C4, but the strobe input immediately goes low thus latching the BCD inputs and retaining the selected output.

The circuit formed by C1 and RI cause a pulse on the strobe input during switch on to reset the tuner to the station selected by the \(\mathrm{S}_{0}\) output.

If it is required that the common contact of the touch buttons be at earth, the decoding diodes could be reversed, the BCD inputs pulled up to \(V_{d d}\) together with the capacitors and the strobe input inverted.
K. R. Drage, Edmonton, London N9.




\section*{MICRO SWITCHES}


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\title{
Semiconductor UPDATHEm FEATURING: tda2002 TDA 1083 нSCH 1001
}

\section*{BRICK OUTHOUSE}

The first integrated circuit I managed to lay my hands on, way back in 1966 I think, was an audio amplifier device from R.C.A. By today's standards, that pioneering miracle would be a joke, needing transformers on the input and output and delivering only about 250 mW , but to me at the time it was pure magic!

Apart from the fact that you could hardly see the i.c. for its supporting "cast-ofthousands", the thing which eventually disappointed me the most about it was its short life.

Yes, you guessed it, whilst trying my precious miracle in one of a variety of data sheet applications circuits there was a wisp of smoke-then silence.

Now all that is behind me. We have become accustomed to the blow out proof, short circuit proof devices which the wise chip designers provide for us.

Or have we? I still see myself as the arch enemy of the audio amplifier chip, blow-out proof or not, and wisps of smoke are by no means unknown on my breadboard socket!

With this sort of background, then, I am always interested in the latest "built-like-a-brick-outhouse" claim for a new audio amplifier chip. Take the TDA2002 device from Fairchild for example, a much more difficult nut to crack than any I have come across lately.

It comes in a tiny five pin plastic powertab package and yet boasts an output power of 8 W with loads down to 1.6 ohm and output currents of up to 3.5 A .

The thing that makes the TDA 2002 such a worthy adversary is its long list of fiendish protective measures, Thermal Shutdown, Short Circuit Protection and Overvoltage Protection, not bad for a chip which boasts a typical T.H.D. of 0.2 per cent at 5 W .

This apparent challenge to my reputation will not go unanswered however. I am already burnishing the tip of my soldering iron in anticipation.

Oh, and by the way Fairchild, I am into lightning-strikes at the moment!

\section*{SNUFF TIN SPECIAL}

If there is any electronic subject likely to raise a yawn from our readers, it must surely be the prospect of an "even smaller" pocket broadcast receiver of the type I like to call squawk boxes! I must confess to having entered the electronics fraternity via the crystal set, the two valve t.r.f (ask your dad!) and the "ham-band-special", before

15 W bridge circuit
using the TDA2002

ever discovering the delights of op-amps or logic gates, but even so, the suggestion of yet another advance in radio receiver miniaturisation, did not exactly have me choking on my breakfast cornflakes!

Not that I wouldn't have been keen 15 years ago mind you (as a lad, I once built a transistor set in a snuff tin) but our oriental cousins have had the whole thing so well tied up for so long now, that even before the introduction of integrated circuits, all the stuffing (should this be snuffing? -ed) had been knocked out of the subject as far as I was concerned. If I have any yen (sic) at all for broadcast receivers nowadays, it's for the antique variety with rows of fat glowing valves, solid mahogany cabinets, and the vain hope that one day whilst tuning through "Hilversum" or "Athens" I might just detect an eerie "Germany callingGermany calling!"

But enough of my life story. The new development I am about to update you with, is, believe it or not, of the very sort to which I have just been objecting. The reason it appears at all, is because I consider it a development so final in its scope, that I confess to feeling a twinge of the old "snuff tin excitement", and if you can stifle your yawns long enough, I think you might agree with me.

The device is an integrated circuit from Sprague, coded ULN 2204A by its American maker, but already boasting a European Proelectron code of TDA 1083. Quite simply this new chip is a complete radio receiver in a sixteen pin dual in line package. Complete, because it contains an a.m. front end, an i.f. amplifier, an a.m. and f.m detector stage, an audio amplifier and a power supply regulator.

True, it does not boast a loudspeaker, and you do still need a couple of r.f. coil cans and a capacitor or two, but until we switch to telepathic broadcasting, it's about as integrated as a radio receiver can get.

You can't even fault it on its performance. It is a full superhet with a.g.c. facilities, and has a 20 microvolt sensitivity for full output on a.m. When used in a dual mode receiver, a.m./f.m. switching is all carried out at d.c. so you could use a D.P.S.T. toggle switch if you wanted to. The audio amplifier, depending on supply voltage (the dip works on 2 to 12 volts, or much higher voltages with a single external resistor) will provide up to a watt into an 8 ohm speaker.

It's true that my snuff tin special needed an earphone and about 200 feet of aerial for correct operation, but how can mere technology replace it?

\section*{BARRIERS DOWN}

Still using germanium diodes in low forward voltage applications such as r.f. detector circuits and logic clamps? Do yourself a favour and try a Shottky barrier diode instead.

Shottky barrier diodes have a forward drop of only about 400 mV at 1 mA and have low capacitance and pico-second switching speeds to match. Hewlett Packard have now introduced a low cost S.B.D. in a common or garden DO35 package, coded HSCH1001.

Apart from the usual advantages of S.B.D.s, the new device features a 60 V reverse breakdown voltage, and only a 200nA leakage at 50V.


When a resistor is placed in the test clips it forms a bridge circuit with VR1, R8 and one of the resistors R1-R7 (according to the position of S1).

If a capacitor is to be measured S1 should be switched to the TR position which transfers the circuits through to the capacitor range and the bridge then balanced using VR 1 and S2. When measuring the value of electrolytic capacitors it will be necessary to "bias" these with the appropriate voltage.

\section*{CONSTRUCTION}

The components for the bridge are mounted on a 18 s.w.g. aluminium panel \(150 \times 130 \mathrm{~mm}\), which is fitted to two wooden side pieces so the front panel is inclined at an angle of 60 degrees.

The resistors and capacitors should be mounted on the two 12 -way wafer switches as shown in the photograph before the switches are mounted onto the front panel. The free ends of the components are connected to a bus-bar across the two switches and the leads for the test clips are passed through a grommet on the front panel and have two small crocodile clips connected to them.

The scaleplate should be marked out as shown in the photograph; no component values should be marked on the scale plate until the calibration stage. The cursor consists of a piece of thin perspex sheet scribed with a centre line which is drilled so that the holes correspond with the lines on the scaleplate, enabling accurate calibration. The cursor is then fixed to a suitable knob.

\section*{AF OSCILLATOR}

The circuit diagram of the AF oscillator is shown in Fig. 2. The unit consists of an astable multivibrator formed by-TR 1 and TR2 with TR3 used as an output amplifier stage. VR2



Rear view of CR Bridge

Fig. 1. Complete circuit diagram of the CR Bridge

\section*{COMPONENTS}
\begin{tabular}{ll} 
Resistors & \\
R1 & \(10 \Omega\) \\
R2 & \(100 \Omega\) (2 off) \\
R3 & \(1 \mathrm{k} \Omega\) \\
R4 & \(10 \mathrm{k} \Omega\) \\
R5 & \(100 \mathrm{k} \Omega\) \\
R6 & \(1 \mathrm{M} \Omega\) \\
R7 & \(10 \mathrm{M} \Omega\) \\
R8 & \(2.2 \mathrm{k} \Omega 10 \%\) carbon \\
R9, R12 & \(7.5 \mathrm{k} \Omega\) (2 off) \\
R10,R11, R13 & \(120 \mathrm{k} \Omega(3\) off) \\
R14 & \(1 \mathrm{k} \Omega \frac{1}{8} \mathrm{~W} 5 \%\) \\
All \(1 \% \frac{1}{4} \mathrm{~W}\) unless otherwise stated
\end{tabular}

\section*{Potentiometers \\ \begin{tabular}{ll} 
VR1 & \(5 k \Omega\) wirewound \\
VR2 & \(25 k \Omega\) linear
\end{tabular}}

\section*{Capacitors}
\begin{tabular}{ll} 
C1 & 10 pF \\
C2 & 100 pF \\
C3 & \(1,000 \mathrm{pF}\) \\
C4 & 10 nF \\
C5 & \(0.1 \mu \mathrm{~F}\) \\
C6 & \(1 \mu \mathrm{~F} 16 \mathrm{~V}\) tant \\
C7 & \(10 \mu \mathrm{~F} 16 \mathrm{~V}\) tant \\
C8 & \(100 \mu \mathrm{~F} 16 \mathrm{~V}\) tant \\
C9, C10 & \(0.01 \mu \mathrm{~F} \mathrm{C280} \mathrm{(2} \mathrm{off)}\) \\
C11, C12 & \(47 \mu \mathrm{~F}\) tant 16 V (2 off)
\end{tabular}

All \(2 \%\) polystyrene unless otherwise stated

\section*{Semiconductors}

TR1,TR2, TR3 BC113 (3 off)

\section*{Miscellaneous}

3 off 3.5 mm jack plugs and sockets
2 off 1 pole 12-way wafer switch
2 off pointer knobs
2 off crocodile clips
1 off PP3 battery
battery clips (if req) crystal earphone
enables the output of the oscillator to be adjusted as required

The prototype unit was constructed using the printed circuit board layout shown in Fig. 3 with the component overlay shown in Fig. 4. The unit which is connected to the bridge via 3.5 mm jack plugs and sockets uses a screened lead and is powered by a PP3 battery.

\section*{CALIBRATION}

After the unit has been assembled and checked the earphone should be plugged in and the AF generator connected and switched on. VR1 shouid be adjusted for maximum output and then VR2 adjusted so the output to the earphone is not excessive.

To calibrate the unit a wide range of close tolerance components are required. Starting at range \(A\) the upper and lower limits of each range should be marked on the


Fig. 3. Printed circuit board design for the AF Oscillator

Fig. 4.
Component layout for AF Oscillator

scaleplate by uitable value resistors in the test clips and adjusting VR1 until the bridge balances (when the output to the earphone is at minimum). The rest of the values can then be filled in. The null will not be so well defined on the higher ranges but the linear markings around the outside of the scale should make it easier to judge the effective null point. The capacitance ranges should be calibrated using the same method. The lettering on the scale is arranged so that the range letter is at the minimum end of the range. Resistor values increase clockwise and capacitor values anticlockwise.

News Briefs

\author{
by Mike Abbott
}

\section*{DATA ENCRYPTION UNIT}

\({ }^{1}\)M SURE many readers will have been struggling for some time now, to get to grips with the bytes and bits of machine code and computer programs. Well, you've arrived just in time to be left behind again, because data encryption is here. Actually, this development shouldn't worry you unless you intend to tap confidential data lines for illicit purposes. A less impressive name for Intel's Data Encryption Unit would be data scrambler/unscrambler, and it is intended as a processing peripheral chip which prohibits "listening in"" to confidential information in data form which is communicated using land lines.

Applications that immediately spring to mind are in inter-bank communication, military communications and inter-company confidential reports. The American National Bureau of Standards
(NBS) have defined a Federal Information Data Encryption Standard, and Intel's new integrated circuit codes and decodes data in accordance with the NBS standard. The new chip, known as the 8294 Data Encryption Unit, has been approved by NBS.

The 8294 codes and decodes 64-bit blocks of data in accordance with a 56 -bit user specified key (algorithm) to produce 64 -bit cipher words. It is necessary to use the same key for both coding and decoding to produce intelligible information at the receiving end. This means that \(2^{56}\)-1 ways of encoding the data are provided. In other words, even with the services of a large and very fast computer, it would be virtually impossible for an unauthorised person to hit upon the right key.

The 8294 is designed to act as a peripheral chip in a processing system. The 56 -bit key and the 64 -bit message are transferred to the 8294 over the system data bus a byte at a time. A DMA interface and three interrupt outputs are available to minimise the software overhead associated with data transfer. With a DMA interface two or more 8294 s may be used in parallel to achieve effective conversion rates which are virtually any multiple of 80 bytes per second. As a bonus, the 8294 has a general-purpose seven-bit TTL output port for user specified functions.

The 8294 operates from a \(5 \mathrm{~V} \pm 10\) per cent power supply and is based in a standard 40-pin package.

Inhave been fortunate this year that my work has taken me to New York on a couple of occasions. This has enabled me to take a quick look at the electronics hobby scene on the other side of the pond. To an outsider the market place seems to be dominated by Citizens Band radio and computers.

\section*{C.B.}

The Citizens Band consists of a group of 40 channels around 27 MHz set aside for private low power communication. Any U.S. national can apply for a licence and there is no test to pass. The equipment used usually runs about four watts on a.m., although s.s.b. is creeping in, and it is designed to be idiot proof. There are no tuning controls to set up, you just turn the knob to the required channel, adjust the volume as desired and press the button on the mike to speak.

Homebrew rigs are frowned upon, as are linear amplifiers. Prices range from just under 40 dollars for a mobile rig for the car to several huindred dollars for a microprocessor controlled, keyboard entry, band scanning, base station.

The system may have some faults, with a few million rigs in service there is bound to be some abuse, but it has a lot going for it too. It provides communication between home and the car and enables you to get traffic reports and directions from other drivers. It is reassuring to see a sign beside the road saying "Nassau police monitor channel \(x x\) ", allowing you to call for help in case of accident or emergency. The coastguard have also started to monitor one of the channels allowing small C.B. equipped boats to call for help in an emergency.

\section*{COMPUTERS}

As far as home computers are concerned it seems to be a sellers market; they are selling like hot cakes. The demand is for machines with high level language with a good size memory, cassette recorder and/or floppy disc. When you consider that electronics prices in the U.S. are about half these over here and salaries over there are about three times ours, this gives the computer enthusiast in the States a 6-1 advantage over us in purchasing equipment. This means he can afford to skip the switch and l.e.d. machines and buy or build from a kit a relatively powerful machine.

For the kit builder the local Heathkit showrooms had the H8 and Heath/Dec 11 machines on display. The local computer shops stock various S 100 bus compatible p.c.b. kits for memory, I/O, etc. and
numerous mail order firms offer boards and card frames for this bus. There are various ready to use machines available via the computer shops and a bewildering array of books on software to get you started programming.

One machine that seems to be going to lead the field is the TRS80, retailed by the Radio Shack shops. The Radio Shack shops are not as their name might suggest ham radio shops, they sell hi-fi units, C.B. transceivers, car radios, tape players, etc. and now the TRS 80 computer. As there are Radio Shack shops everywhere and each one seems to have one TRS80 in the window and a demonstration model inside, sheer weight of numbers should help the machine fight its way to the front. It also seems to be a rather nice machine (The TRS80 is available from Tandy in the U.K.-Ed)

It has the \(Z 80\) C.P.U., level 1 basic in 4 K ROM, and 4 K RAM. Level II basic and 16 K RAM are available as an option, and there are printers, floppy discs, etc. available to order.

The computer section seems to be well served by magazines such as Kilobaud, Byte and Interface Age, etc. and there appears to be a thriving market in software offerings for the more popular machines, cassettes being available with games and maths programs from numerous sources.

\section*{RACING CARS}

One interesting offering in the hobby shops was a radio controlled electric racing car with a single chip microprocessor in the transmitter and another one in the car. The method of encoding allows four cars to be raced together although the receivers in the cars are simple superregen types. The frequency band it operates in is around 50 MHz but it should be possible to use the sets at 27 MHz with suitable mods. to the r.f. side.

1 was lucky enough to visit a small exhibition put on by the Long Island Mobile Amateur Radio Club. The club is very active and they operate five repeaters on v.h.f. and above, one of them for TV. They put on quite a good show, with a couple of 2 metre stations, RTTY and slow scan using the ROBOT slow/fast scan convertor. Apparently repeaters are very thick on the ground in the area. I was told that there were 200 within a 70 mile radius of the Empire State building. This gives good coverage but interference between repeaters must be a problem!

Dave Coutts

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}

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\section*{The Great Debate (3)}

One of the hazards of monthly comment is that of being overtaken by events. This has happened in the Great Debate. The philosophical impact of VLSI on life-style and attitudes on which I wrote two months ago still stand.

But since my comments last month on the practicality or otherwise of pushing Britain into the forefront of technology and large-scale production of VLSI circuits, there has been positive action, or at least some positive statements.

First came the news of INMOS, the completely new entrant in the field, backed by the National Enterprise Board and headed up by former Texas Instruments and Mostek employee Dr Richard Petritz, assisted by Dr Paul Schroeder, another exMostek man, and Iann Barron, the British whizz-kid who founded Computer Technology some years ago and said to have been the mediator between Dick Petritz and the NEB.

Then, the well-ventilated rumour that GEC was seeking an arrangement with Fairchild was confirmed by a public statement that this was indeed the case and that a joint 50/50 GEC/Fairchild venture was going ahead.

INMOS will get \(£ 25\) million of goverment backing initially, with another \(£ 25\) million top-up, if necessary, later on. Headquarters will be in the UK but pilot production in the USA. Eventually, so it is claimed, INMOS will have a manufacturing plant in the UK employing 4,000 people in a depressed area. INMOS director Paul Schoeder is quoted, 'We think we have the most exciting enterprise in the world."

GEC's move is more realistic. It involves a working capital of \(£ 20\) million (GEC is flush with cash and will put up \(£ 10\) million) and aims at a production rate of \(£ 40\) million of product in the first full year in 1981. The plant will be set up in existing buildings and
employ about 1,000 people, will be onstream ahead of INMOS and using proven technology the plant will actually be producing in 1980. GEC Semiconductors, in more specialised products, will continue as a separate entity and will enjoy some of the goverment support channelled through the Department of Industry.

Good news indeed. But it doesn't take much imagination to see which of these two operations will be the more successful. Realism, the GEC approach, must be a better bet than optimism. Private cash is always spent more prudently than public cash. GEC/Fairchild is already in the business and has marketing outlets. Not to mention technology. And from the business point of view GEC's Sir Arnold Weinstock has an unparalleled track record in shrewd management.

Among the many handicaps facing INMOS is uncertainty. A change of goverment could kill the project stone dead before it gets beyond the planning stage. Powerful voices in industry regard INMOS plans as controversial, if not downright fanciful, and should the Conservatives be returned to power it is already clear that they would not encourage the establishment of any new state-backed enterprises that could become a future burden on the economy.

A factor which could affect both INMOS and the GEC/Fairchild venture and, for that matter, all the semiconductor industry in the UK is the availability of scientists and engineers. INMOS is reported to be seeking 800 graduates and development engineers. GEC/Fairchild will need 300 engineers and 150 technicians. If these, or a fair proportion of them, are milked from existing operations this could weaken the whole infrastructure of the established UK semiconductor industry. One thing is certain, that any semiconductor engineer worth his salt need never be in the dole queue.

\section*{Employment}

Accompanying the immediate convenience of new microelectronic applications, welcome to most of us, is the unwelcome impact on employment. Yet another set of figures, this time from Plessey, underlines the downward trend. In financial years 1973/74 turnover was £400 million with a world total of \(76,000 \mathrm{em}\) ployees. In FY 1977/78 the figures were f611 million with only 58,700 employees. If the overseas employees are eliminated from the figures, the UK employment by Plessey has dropped from 50,600 to 43,600 in the past three years.

Plessey, of course, was particularly hardhit by savage cut-backs in orders from the Post Office, but even allowing for that special circumstance the trend is obvious and will continue.

\section*{Economics}

The economics of microcircuits are fascinating. A study by Marconi engineers points out that for a four-channel mobile radio you can break even in cost by using a
frequency synthesiser rather than four separate crystals. For a ten-channel set, use of a synthesiser saves \(£ 25\) per unit. The synthesiser, of course, only uses a single standard reference crystal. So on a tenchannel set there is a saving of nine crystals. The set-maker gets more profit, the set-user has a simplified and less costly spares holding, but the poor old crystal manufacturer loses 90 per cent of his business. Well, not quite, because mobile radio is still a big growth area with the world market increasing at over nine per cent a year.

\section*{Electronic Warfare}

The hush-hush business of electronic warfare (EW) is flourishing as never before. Mostly kept under security wraps in the UK, a glimpse of happenings is occasionally allowed. Decca, for example, has over a dozen equipments of various types in production for detection, analysis and jamming of radar signals. A £2 million order is in hand for the Royal Danish Navy and another f 8 million of Decca EW equipment will go into Lynx helicopters for the Royal Navy.

What makes EW such good business (and so expensive) is that every advance in technology needs a new countermeasure. Marconi Radar Systems, for example, has just announced a new mobile long-range air-defence radar, the very thing for the 1980 s and 1990s. Called Martello, it has every refinement to beat the hostile jammers. But back-room boffins will rise to the challenge. Marconi is one of the biggest firms in EW and it is conceivable that while Martello was in development in one laboratory, another team of engineers next door was already working on how to defeat the system.

\section*{Video War}

Discounts of up to 20 per cent are said to be offered by US dealers to shift home VTRs to a reluctant public. VTR sales in the USA have been only half those predicted. UK sales, however, have been as expected, according to manufacturers and dealers. But if stocks pile up in the USA it seems likely that surplus production could come to Europe and there could be some bargains in the shops, next year if not this.

\section*{TV Progress}

The Matsushita factory in South Wales, opened only last year, is now stepping up production of National Panasonic colour TV sets to nearly 1,000 a week. The factory employs some 250 people.

Mullard is spending \(£ 24\) million on updating TV tube production in the UK. The Department of Industry is helping with a £4.5 million handout. Mullard supply some 50 per cent of all tubes used in the UK and would like to supply as much as 75 per cent of the popular 22 -inch size. Hopes that the tide of imports of TV tubes would be reduced by increased tariffs or import quotas are not bright. It looks therefore as if Mullard can increase market share only by intense price competition which would erode profits.



\section*{... a selection from our postbag \\ Readers requiring a reply to any letter must include a stamped addressed envelope.}

Opinions expressed in Readout are not necessarily endorsed by the publishers of Practical Electronics.

\section*{Another Range}

Sir-Whilst attempting to construct the Linear Capacitance Meter, a few "deliberate mistakes", were found. After correcting these errors the instrument was tested and found to work correctly on all ranges, but 7 and 8 were found to be \(\times 10\) high.
To rectify this the \(10 \mathrm{M} \Omega\) resistor connected to S2b terminals 7 and 8 was disconnected, and terminals 7 and 8 were connected to 5 and 6 of S2b. This then brought ranges 7 and 8 into line with the others, i.e. in steps of ten. The switch used for the range selection has more than 8 positions, it was therefore decided to add another range: 1 volt \(=10,000 \mu \mathrm{~F}\).

This was achieved by connecting terminal 8 of S2a to terminal 9 of S2a, and connecting the \(10 \mathrm{M} \Omega\) resistor that was removed from terminals 7 and 8 of S2b to terminal 9 of S2b.

A \(50 \mu \mathrm{~A}\) meter movement which was calibrated \(0-5\) has been used, hence the capacitance meter now has nine switched ranges:
(1) 500 pF
(2) 5 nF
(3) 50 nF
(4) 500 nF
(5) \(5 \mu \mathrm{~F}\)
(6) \(50 \mu \mathrm{~F}\)
(7) \(500 \mu \mathrm{~F}\)
(8) \(5,000 \mu \mathrm{~F}\)
(9) \(50,000 \mu \mathrm{~F}\)

potentiometers. These were adjusted to obtain the correct reading on the moving coil meter. whilst observing the readout on a digital meter connected between Vout and 0 V . The meter used to read this voltage must be a high impedance meter or an oscilloscope, not the "run of the mill" \(20 \mathrm{k} \Omega / \mathrm{V}\) type.

This design has been proven by a friend of mine who has made the instrument incorporating the mods; needless to say he is highly delighted.
T. L. Woodger Reading.

\section*{Oh Yes!}

Sir-I have just read "Readout" in P.E. October 1978 and find myself compelled to reply to R. E. Hurst's letter about pH. The concept of pH is a chemical one, and as a chemistry graduate I feel the pH scale must be looked at in context. The pH of a solution in equilibrium is equal to the negative logarithm
of the hydrogen ion concentration i.e.
\[
\mathrm{pH}=-\log \left[\mathrm{H}^{+}\right]
\]

Using this expression the pH of a solution I molar in \(\mathrm{H}^{+}\)is in fact 0 .
\[
\mathrm{pH}=-\log 1=0
\]

All commercially available pH meters use a \(0-14 \mathrm{pH}\) scale. As to R. E. Hurst's theory of "absolute acid" this is utter nonsense. If we were to push the theory to its limit a solution of 10 molar acid would have a pH of -1 .
\[
\mathrm{pH}=-\log 10=-1
\]

Since concentrated acids are often stronger than 10 molar, even \(\mathrm{pH}=-1\) does not constitute "absolute acid". In short W Hediger is quite correct in giving his pH meter a "0" on the scale and R. E. Hurst would do well to get his facts straight before going off the deep end over technicalities which have deeper roots than simple logarithm theory.
A. K. Strange, Grad R.I.C., F.Chem Soc

Bristol.

\section*{Okay!}

Sir-When today I read what I had written in trying to make a simple point (No Oh! Readout, October 1978) my eyes nearly popped out. This is an object lesson in what can happen if you over simplify. My real point is that the logarithmic scale is an absolute with an origin which can be approached and conceived of but never reached. Log graduated scales disclose this, but scales which are linear because the log is used conceal the nature of the basis of the measurement. By omitting the " 0 " the nature of the underlying concept is shown.
Ugh! Mea culpa, mea maxima culpa. I hope the ancient alchemists will rest in peace.
R. E. Hurst

Blackpool.
(Enouph, the matter is now at pH7-Ed.)

To increase the accuracy of the instrument a divide by 5 switch has been added as shown in the diagram. The switch used for this must be a push-to-make type so that it cannot be inadvertently left on, as this could lead to funny shaped meter pointers.

The meter multipliers used were miniature

\section*{FUMBLE NUDGE GAME (April 1978)}

Resistor R23 appears correctly in the power supply diagram Fig. 5. It is shown incorrectly in the centre of the wiring diagram Fig. 6 , where, in fact, IC2 pin 11 connects directly to IC11 pin 11.

\section*{KEYBOARD (September 1978)}

\section*{Under "components", IC8 should be a 7474}

METRONOME (September 1978)
Diode D3 should be 7.5 V and not 5.1 V .
CAR BURGLAR ALARM (December 1977)
Constructors still undertaking this project, and unable to obtain the capacitors specified for C 1 and C 4 should follow the author's recommendation, which is to obtain \(100 \mu \mathrm{~F} / 16 \mathrm{~V}\) tantalum bead capacitors from Watford Electronics and increase R6 and R8 to \(150 \mathrm{k} \Omega\).

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