PRACTICAL

#  <br> NOVEMEER 1977 

15-WATT KIT IN CHASSIS FORM When you are looking for a good speaker. why not build your own from this kit. It's the unit which we supply with the enclosures illustrated below Size 13": 8" \{approx. woofer (EMI),tweeter, and matching crossover components Power handing capacity
15 watts rms. 30 watts peak
£ 1700 PER STEREO PAIR


EASY-TO-BUILD WITH ENCLOSURE
Specially designed by RT-VC for cost-conscious hi-fi enthusiasts, these kits incorporate two teak-
simulate enclosures, two EMI $13^{\prime \prime} \times 8^{\text {" }}$ (approx, woofers, two tweeters and a pair of matching crossovers. Easily constructed. using a few basic tools. Supplied complete with an easy-to-follow circuit diagram, and crossover components. Input 15 watts rms. 30 watts peak, each unit £ $28^{00}$ Cabinet size $20^{\circ} \times 11^{\prime \prime} \times 9^{\frac{1}{2} \times}$ PER STEREO PAIR (approx.).
$+p \& p £ 5.50$

COMPACT' FOR TOP VALUE
How about this for incredible bookshelf value from RT-VC! A pair of high efficiency units for only $£ 7.50$ - just what you need for lowpower amplifiers. These infinite baffle enclosures come to you ready mitred and professionally finished. Each cabinet measures $12^{*} \times 9^{*} \times 5^{\prime \prime}$ (approx.) deep, and is in wood simulate. Complete with wo B " $^{\prime \prime}$ (approx.) speakers or max, po
of watts.


 | per |
| :--- |
| sereo |
| pair |
| fir |
| 80 |
| $+p 8 p$ |
| $£ 2.20$ |

SPEAKERS Two models - Ouollb, teak eneer, 12 watts rms, 24 watts peak. $18 \frac{1 \frac{1}{2}^{*} \times 13 \frac{1}{2}^{*} \times 7 \frac{1}{6}}{}$
(approx).
34 PER PAIR
$34+p$ \& p f6.50
Duo III. 20 watts rms.
40 watts peak.
$27^{\prime \prime} \times 13^{\prime \prime} \times 11_{2}{ }^{\prime \prime}$ (approx.)
f5 2 PER PAIR

amp. Module, Garrard auto/manual
deck with cueing device, pre-cut and finished cabinet work, Output 4 watt per channel, phones socket and ecord / replay socket
${ }^{\text {£ }} 26^{9}$
 KIT
Complete with speaker, baffle and fixing strip The Tourist IV for the experienced constructor only. The Tourist IV has five push buttons. tour medium band and one for long wave band The tuning scale is illuminated and attractive small aluminium control knobs are used for manual tuning and volume control. The modern style fascia has been designed to blend with most car interiors and the finished radio will slot into a standard car radio aperture.
Size approx. $7^{\prime \prime} \times 2^{\prime \prime} \times 4 \frac{1}{4}^{*} .12$ voits pos or neg earth (altered internally). p \& $p \mathrm{f} 1.50 \mathbf{f} 12^{50}$
FREE TO PERSONAL SHOPPERS BUYING
CAR RAOIO KIT ELECTROMATE Rear window heat


TO PERSONAL SHOPPERS See Below

## $20 \times 20$ WATT STEREO AMPLIFIER

superb viscount $\mathbf{X}$ unit in teak-fimished cabinet. Silver fascia with alimunium rofary controls and pushtiuttons, red mains indicator and stereo jack sockel Function switch for mic. magnetic and crystal pick-ups, tape, tuner, and ㅊ auxiliary Rear panel features two mains outers. OIN speaker and input p\&p $£ 2.50$ sockets, plus fuse $20+20$ watts rms, $40+40$ watts peak.
-FREE To cash or cheque personal shoppers
A 4 channel Stereo Adaptor to all buyers of the visicpunt $20 \times 20$ Amplifier at $£ \mathbf{2} \mathbf{9}^{90}$ limited offer. Available separately at $£ \mathbf{3}^{95}$

## SPECIAL <br> OFFER for example. <br> Duo speaket system viscount Amplther. Miscount Amplther. MP60 'ype luntable comple <br>  <br>  <br> ( on complete stereo systems using

ADD-ON STEREO CASSETTE TAPE DECK KIT Designed lor the experienced O.I.Y. man. This kit comprises of a tape fransport mechanism. ready built and tested record/replay electronics with twin V.U. meters and level control ready for mating together with the mechanism
Specifications: Sensitivity - Mic. 0.85 mV a 20 K DHMS Oin. 40 mV /a 400 K OHMS : Output - 300 mV RMS per channel ia 1 KHz from 2 K OHMS source : Cross Talk - 30 db Tape Counter - 3 Digit - Resettable : Frequency Response $40 \mathrm{~Hz}-8 \mathrm{KHz} \pm 6 \mathrm{db}$ : Oeck Motor -9 Volt OC with $\mathbf{f 1 9 9 5}$ electronic speed regulations: Key Functions Record, Rewind, Fast Forward, Play. Stop \& Eject. p\&pf2.5


Optional extras Pair of Oynamic microphones $\mathbf{E} 3.95+\mathbf{£ 1 . 0 0} p 8 p$ Mains transformer $\mathbf{f} 2.50+£ 1.00 p$ \& $p$

STEREO CASSETTE record/replay fully built
P.C. board incorporating 41 .C. $s$. GRUNDIG $5 \frac{3}{4}$ " tape 1800 ft .
£ 120 each. 5 for $£ \int_{000}$ PAIR SIEREO 8 WATT SPEAKERS

## personal shoppers

## PORTABLE

MONO
DISCO

with built-in pre-amplifiers
Here's the big-value portable disco console from RT-VC! It features a pair of BSR MP 60 type autoreturn, single play professional series record deck Plus all the controls and features you need to give fabulous disco performances.
Simply connects into your existing slave or externa! amplifier.

## 45 WATT MONO DISCO AMP

 ${ }^{〔} 35^{00}$$+\mathrm{p} \% \mathrm{p}$
£ 2.50
Size approx
$13 \frac{3}{8}$ " $\times 5 \frac{1}{4}^{\prime 2} \times 63^{\prime \prime} \times$ ?
Here's the mono unit you need to start off with. Gives you a good solid 45 watts rms, 90 watts peak output. Big features include two disc inputs, both for ceramic cartridges, tape input and microphone input. Level mixing controls fitted with integral push-pull switches. Independent bass and treble controls and master volume.
$70 \& 100$
WATTMONO
DISCO AMP
Size approx.
Sloping facia, you can use the controls
without fuss or bother. Brushed alumimium fascia and rotary controls. Five smooth acting, vertically mounted slide controls - master volume, tape level mic level, deck level, PLUS INTER- OECK FAOER for perfect graduated change from record deck No. 1 to No. 2, or vice versa. Pre-fade level control (PFL) lets YOU hear next disc before fading 70 wat1 57 it in. VU meter monitors output level. 100 watt ${ }^{E} 65$ Output 100 watts RMS 200 watts peak. p \& p 54.00


BSR BOS95 SERIES
Belt drive turnable unit, speed, semi automatic operation $\quad \mathbb{2} \mathbf{2}^{95}$

PRACTICE GUITAR AMPLIFIER WITH BUILT-IN SPEAKER This budget practice amplifier, has been
specially designed for the

amateut, who requires a quality
self-contained unit with all facilities. 2 inputs for mic or guitar, the 2nd for record player or cassette deck, it also can be used for cine-sound amplification 2 volume controls, 1 for each input. also base and ueble controls. Power output with internal speaker 10 watts RMS. with remote
$30 \times 30$ WATT AMPLIFIER KIT Specially designed by RT.VC for the experienced constructor, this kit comes complete in every detail. Same facilities as Viscount IV amplifier of $p$ Chassis is ready punched, drilled and $£ 2.50$ formed Cabinet is finished in teak $\mathbf{2 9}^{00}$ veneer. Silver fascia and easy-tohandle aluminium knobs.

NOW AVAILABLE fully built and tested. Output $30+30$ watts rms, $60+60$ peak. $£ 3500+p \& p £ 2.50$

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 This matching loudspeaker system is hand made kit comprises of two 8 "diameter approx. base drive unit, with heavy die cast chassi laminated cones with rolled P. V.C. surrounds two $3 \frac{1}{2}$ " diameter approx. domed tweeters comp with crossover networks
## f4.00p $\& \mathrm{p}$ stereo pair ${ }^{\mathbf{2}} \mathbf{2 0 0}$


$\qquad$

Send stamped addressed
envelope for further details.

speaker (not supplied) 20 watts ${ }^{£} 32^{50}$

## HOME 8 TRACK CARTRIDGE PLAYER Automatically switches programmes monitored by indicators.

 with manual override track selection. This unit will match with the Unisound modules and is compatable with the Viscount IV amplifier with Sim teak

## PYE STEREO

GRAM CHASSIS
(Complete with
circuit-diagrams)


Complete ready to install-Wave bands LM. VHF SIEREO, VHF MONO Controls for tuning volume. balance, bass and treble. Power output 7 watts R.M.S per channel 14 watts peak 8 ohms.
$2^{\prime \prime} 8^{8}$ approx chassis speakers and
BSR auto record player deck
personal shoppers ontr ${ }^{〔} 3$

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| AC127 | 0.25 | -BD135 | 0.35 | OA10 | 0.55 | 1N4007 | 0.15 | 7412 | 0.26 0.45 |
| AC128 | 0.25 | *8D136 | 0.35 | OA47 | 0.14 | 1N4009 | 0.15 | 7416 | 0.40 |
| AC141 | 0.20 | *BD137 | 0.37 | OA70 | $0 \cdot 30$ | 1N4149 | 0.07 | 7417 | 0.40 |
| AC141K | 0.30 | *BD138 | 0.40 | OA79 | 0.30 | 1N5400 | 0.14 | 7420 | 0.20 |
| AC142 | 0.20 | *BD139 | 0.43 | OAB1 | 0.30 | 1N5401 | 0.16 | 7422 | 0.25 |
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| -AFZ12 | 2.75 | BF181 | 0.45 | OC36 | 1.50 | 2N1308 | 0.60 | 7475 | 0. 59 |
| ASY26 | 0.45 | BF182 | 0.45 | 0 C 41 | $0 \cdot 50$ | 2N1309 | 0.60 | 7476 | 0.42 |
| ASY27 | 0.50 | BF 183 | 0.45 | OC42 | 0.50 | 2N1613 | 0.33 | 7480 | 0.60 |
| ASZ15 | 1.25 | EF184 | 0.39 | OC43 | 1.50 | 2N1671 | 1.50 | 7482 | 0.85 |
| ASZ16 | 1.25 | ${ }^{\text {BF185 }}$ | 0.37 | 0044 | 0.50 | 2N1893 | 0.33 | 7483 | 1.00 |
| ASZ17 | $1 \cdot 25$ | *BF194 | 0.12 | OC45 | 0.50 | 2N2147 | 1.40 | 7484 | 1.00 |
| ASz20 | 0.75 | *BF195 | 0.11 | 0 O 71 | 0.45 | 2N2148 | 1.65 | 7486 | 0.40 |
| AS221 | 1.50 | *BF196 | 0.13 | $00^{72}$ | 0.45 | 2N2218 | 0.33 | 7490 | 0.52 |
| AU113 | 1.70 | *BF197 | 0.14 | 0 O 73 | $1 \cdot 00$ | 2N2219 | 0.42 | 7491AN | 0.85 |
| AUY10 | 1 -70 | BF200 | 0.32 | 0 O 74 | 0.75 | 2N220 | 0.35 | 7492 | 0.60 |
| BA145 | 0.15 0.15 | *BF224 | 0.29 0.35 | ${ }_{0} 0 \times 75$ | $0 \cdot 60$ | 2N2221 | 0.22 | 7493 | 0.70 |
| baisa | 0.10 0 | BF257 | 0.37 | ${ }_{0} 0 \mathrm{Cl} 7$ | 1. 200 | 2N2322 | 0.25 | 7494 | 0.80 |
| BA155 | $0 \cdot 12$ | BF258 | 0.42 | $0 \mathrm{CB1}$ | 0.75 | 2N2368 | 2.75 0.17 | 7495 | 0.80 |
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| BC109 | 0.13 | *BFS61 | 0.25 | ${ }^{\circ} \mathrm{Cl} 130$ | 2.25 | 2N2907 | 0.21 | 74116 | 1.69 |
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| $\begin{array}{r} * \\ * \\ * \\ * B C 114 \end{array}$ | 0.15 0.19 | BFW10 | 0.90 0.90 | OC141 OC170 | 2.25 | +2N2925 | 0.15 0.17 | 74119 | 1.95 2.00 1 |
| *BC116 | 0.19 | BFX84 | 0.38 | OC171 | $0 \cdot 60$ | ${ }^{\text {2 }}$ 2N3926 ${ }^{\text {N }}$ | 0.13 | 74120 | $1 \cdot 10$ |
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| BC177 | 0.19 | BY127 | 0.15 | T1P31A | 0.62 | 2N3772 | 1.70 | 74155 74156 | 0.90 |
| ${ }^{\text {BC176 }}$ | 0.16 | BZX61 | 0.20 | T1P32A | 0.75 | 2N3773 | $2 \cdot 65$ | 74157 | 0.50 |
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Component set with special foot operated switches $\mathbf{8 7} \mathbf{7 9}$ Alternative component set with panel mounting switches
$84 \cdot 96$
$51 \cdot 43$
SOUND EENDER (P.E. May 74)
A multi-purpose sound controller, the functions of which include envelope shaper. tremolo, voice-operated fader, Comatic fader and frequency-doubler
Component set for above functions (excl. SWs)
Printed circuit board
Optional extra-additional Audio Modulator, the use of which, in conjunction with the above component set, can produce "jungle-drum'" rhythms
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52.88

PHASING UNIT (P.E. Sept. 73)
A simple but effective manually controlied unit for introducing the "phasing" sound into live or recorded Com
E. 8.3

PHASING CONTROL UNIT (P.E. Oct. 74)
For use with the above Phasing Unit to automatically control
the rate of phasing.
Component set (incl. PCB)
4.48

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22.33
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The Wah-Wah effect produced by this unit can be controlled
manually or by the integral automatic controller.
Component set (incl. PCB)
£3. 55
AUTOWAH UNIT (P.E. Mar. 77)
Automatically produces Wah-pedal and Swell-pedal sounds
each time a new note is piayed.
Component set. PCB, special foot awitches
Component set and PCB, with panel switches
P.E. JOANNA (P.E. May/Sept. 75)

A five-octave electronic piano that has switchable alternative voicing of Honky-Tonk piano, ordinary piano, harpsichord, of the three. together with facilities including fast and slow tremolo, loud and soft pedal switching, and sustain pedal switching. The power amplifier typically delivers 24 watts into 8 ohms. The PCBs have been redesigned by ourselves making improved use of the space available.
Main power supply, tone generator. 61 envelope shapers,
voicing and pre-amp circuits.
Set of basic component kits for above
Set of printed
Printed circuit board for power amp

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5-octave electronic organ with 5 basic voices that can be used individually or together, 5 pitches ( $2 \mathrm{ft}, 4 \mathrm{ft}, 8 \mathrm{ft}, 16 \mathrm{ft}, 32 \mathrm{ft}$ ) variable attack, tremolo, vibrato. phasing, and variable sustain. Details in our list.

## ORGAN CONVERSION KIT

Converta the P.E. Joanna electronic piano to also provide most of the facilities offered by the above electronic organ.
Basic component set and PCB
\&12.34

SYNTHESISER TUNING INDICATOR (P.E. July 77)
A aimple 4-octave frequency comparator for use with synthesisers and other instruments where the full versatility Component $P$ PCB (but axd

## GUITAR FREOUENCY DOUBLER (P.E. Aug. 77)

A modified and extended version of the circuit published Details in liat

> SEE OTHER PAGE FOR KEYBOARDS, AND OUR LISTS FOR OTHER COMPONENTS AND ACCESSORIES STOCKED

## WIND AND RAIN UNIT

A manually controlled unit for producing the above-named sounds.
Component set (incl. PCB)
ع3. 72

## GUITAR OVERDRIVE UNIT (P.E. Aug. 76)

Sophisticated, versatile Fuzz unit, including variable and switchable controls affecting the fuzz quality whilst retaining the attack and decay, and also providing fittering. Does no duplicate the effects from the Guitar Effects Pedal and can be used with it and with other electronic instruments. Component set using dual slider pot Printed circuit board

## FUZZ UNIT

Simple Fuzz unit based upon P.E. "Sound Design'" circuit.

## TREMOLO UNIT

Gased upon P.E. 'Sound Design' circuit
Component set (incl. PCB)
E3. 64
TREBLE BOOST UNIT (P.E. Apr. 76)
Gives a much shriller quality to audio signals fed through it. Compth of boost is manually adjustable.
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83.76
84.69

ENVELOPE SHAPER WITHOUT VCA (P.E. Oct. 75)
Provides full manual control over attack, decay, sustain and release functions, and is for use with an existing voltage Component amplifier.
Component set (incl. PCB)
[4. 66

## ENVELOPE SHAPER WITH VCA (P.E. Apr. 76)

This unit has its own voltage controlled amplifier and has full manual control over attack, decay, sustain and release Component set (incl. PCB)

E5.68

## TRANSIENT GENERATOR (P.E. Apr. 77)

An envelope shaper, without VCA, having the usual attack, decay, sustain and release functions, and in addition it also provides a "Repeat Effect" enabling a synthesiser to be programmed to imitate such instrumenta as a mandolin or Com
Printed circuit board
84.52
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ع8 $\cdot 22$

## RING MODULATOR (P.E. Jan. 75)

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NOISE GENERATOR (P.E. Jan. 75)
Part of the P.E. Minisonic now released as an independent
Component set (incl. PCB) (Order
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c4. 58

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## AND OTHER PROJECTS

PHOTOGRAPHS in this advertisement show two of our units containing some of PCBs. The cases were built by ourselves and are not for sale, hough a small selection of other cases is avaliable.

LIST-Send stamped addressed anvelope with all U.K. requests for free list giving fuller details.of PCBs, kits and other components
OVERSEAS enquiries for list: Europesend 20 p ; other countries-send 40 p .


KEYBOARDS AND CONTACTS
Kimber-Allen Keyboarde as required for many published circuits, including the P.E. Joanna, P.E. Minisonic, and P.E. Synthesleer. The menufacturers claim that these are the finest moulded plastic keyboards avaliable. All octave
3 Octave ( 37 notes) £25•50. 4 Oct (49 notes) £32-25. 5 Oct ( 61 notes) £39.75.
Contact Assembiles for use with above keyboards: Single-pole change-over (type SP) as fop P.E Joanna and P.E. Minisonic. Two-pole normally-open make-break (type DP) as for P.E. Synthesiser. Special contact assembly (type 4PS) having 4 poles, 3 of which are normally-open make-break contacts and the fourth is a change-over contact-etis specia assembly enables SAME KEYBOADDUs beise the cost of more han one keyboard. See our list for other simultaneo


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(Elektor Magazine 1977). Very sophisticated music
synthesiser tor the advanced constructor and for whom
cOst la secondary to performance.
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Details in lists. Please send S.A.E.

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FEATURES: complete pre-amplifier in single pack; multi-function equalisation: low noise: low distortion; high overload; two simply combined for stereo.
APPLICATIONs: hi-fi; mixers; disco: guitar and organ; public address.
SPECIFICATION: Inputs-magnetic pick-up 3 mV : ceramic pick-up 30 mV ; tuner 100 mV ; microphone 10 mV ; auxiliary $3-100 \mathrm{mV}$; input impedance $47 \mathrm{k} \Omega$ at 1 kHz . Outputs-tape 100 mV ; main output 500 mV R.M.S. Active 1 kHz ; signal/noise ratio 68 dB . Overload- 38 dB on magnetic pick-up. Supply Voltage- $\pm 16-50 \mathrm{~V}$. Price $55 \cdot 22+65 \mathrm{p}$ VAT. P. \& P. free HY5 mounting board B.1. 48p + 6p VAT. P. \& P. free
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FEATURES: COmplete $A$ alich low APPLICATIONS: updating audio equipment: guitar practice amplifier: test amplifier; audio oscillator.
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Price $£ 5 \cdot 22+65 p$ VAT. P. \& P. free
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external components.
SPECIFICATION: Input Sensitivity- 500 mV . Output Power-25W R.M.S. Into $8 \Omega$. Load Impedance-$4-16 \Omega$. Distortion- $0.04 \%$ a: 25 W at 1 kHz . Signal/Noise Ratio- 75 dB . Frequency Response -10 Hz $45 \mathrm{kHz}-3 \mathrm{~dB}$. Supply Voltage- $\pm 25 \mathrm{~V}$. Size- $105 \times 50 \times 25 \mathrm{~mm}$.
Price $56 \cdot 82+85 p$ VAT. P. \& P. free
The HY120 is the baby of I.L.P.'s new high power range, designed to meet the most exacting requirements including load line and thermal protection this amplifier sets a new standard in modular design.
FEATURES: very low distortion; integral heatsink: load line protection; thermal protection: five connections; no external components.
APPLICATIONS: hi-fi; high quality diaco; public address: monitor amplifier: guitar and organ.
SPECIFICATION: Input Sensitivity- 500 mV . Output Power--60W R.M.S. into $8 \Omega$. Load Impedance-$4-16 \Omega$. Distortion- $0.04 \%$ at 60 W at 1 kHz . Signal/Nolse Ratio- 90 dB . Frequency Response- 10 Hz $45 \mathrm{kHz}-3 \mathrm{~dB}$. Supply Voltage $- \pm 35 \mathrm{~V}$. Size $-114 \times 50 \times 85 \mathrm{~mm}$.
Price $115 \cdot 84+£ 1 \cdot 27$ VAT. P. \& P. free
The HY200 (now improved to give an output of 120 watts) has been designed to stand the most rugged conditions such as disco or group while still retaining true hi-fi performance.
FEATURES: thermal shutdown; very low distortion; load line protection; integral heatsink: no external components.
APPLICATIONS: hi-fi; disco: monitor: power slave: industrial; public address.
SPECIFICATION: Input Sensitivity- 500 mV . Output Power-120W R.M.S. Into $8 \Omega$. Load Impedance-$4-16 \cap$. Distortion- $0.05 \%$ at 100 W at 1 kHz . Signal/Noise Ratio- 96 dB . Frequency Response- 10 Hz $45 \mathrm{kHz}-3 \mathrm{~dB}$. Supply Voltage- $\pm 45 \mathrm{~V}$. Size $-114 \times 50 \times 85 \mathrm{~mm}$.
Price $223 \cdot 32+£ 1 \cdot 87$ VAT. P. \& P. free
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## WINDOW GAZING

ANY student of electronics knows what a difficult task it is keeping up with the ever expanding range of monolithic circuit devices. Manufaciurers' literature, ranging from single data sheets and application notes to impressive tomes of hundreds of pages, reveals a staggering variety of purposedesigned chips covering a multitude of applications including newly opened-up fields. It is all mouth-watering. But all too frequently, we can only gaze at the goods and not touch.

Some lsi devices hit the headlines, become household names, and feature almost continuously in constructional projects. But there is a far greater number of lesser-known i.c.s which have not been so well exposed in the constructor area, although they may be commonplace in the industrial scene.

Included amongst the latter will be a host of intriguing devices which have been designed for equipment manufacturers' specific requirements, and have no immediate obvious application outside this intended area. Yet unsuspected possibilities do often come to light when these chips are subjected to scrutiny by independent and unbiased eyes. Give the amateur enthusiast a chance, and it is almost a certainty that he will come up with a new idea for exploiting some such device beyond its originally intended purpose.

In terms of devices produced, it is clear that we in the constructor area have seen only the tip of the iceberg.

It is more by luck than plan when custom designed i.c.s find their way into amateur hands. More is the pity; not only for the constructor himself, but also the manufacturer and supplier. These commercial interests stand to gain by a fuller exposure of these devices.

Microcircuit manufacturers ought to consider the advantages of making their products more widely known and accessible to the amateur market. By doing so, they will be doing themselves a favour. They will be interfacing with a large body of uncommitted technical free thinkers. Any worthwhile achievements arising from these non-professional endeavours must help increase the value, repute, and sales of specific devices.

This topic was briefly touched on here last month. But it is a matter of fundamental importance and deserves underlining from time to time. And this month is particularly opportune, since we have included an extra 8-page supplement entitled I.C. Specials.

## A choice selection

Some examples of the kind of devices we have in mind are mentioned in this supplement. It has been possible to include only a.few, but these have been selected to cover a variety of applications and interests.

Musical interests are well catered for and this reflects the i.c. industry's current large commitment to this expanding area of home entertainment. What's good for
the commercial organ maker is equally good for the constructor. Electronic delay lines represent an important technical development, and have endless possibilities apart from "flanging", so this particular "bucket brigade" chip does not have to be confined to the musical domain.
Temperature controllers and fluid detectors bring us into the strictly workaday area of instrumentation. Timing requirements ranging from 5 milliseconds to over 3 months are provided for by one single chip-a device which should satisfy an awful lot of requirements. And of course TV games. Our selection would not be complete without some representation from this growing area.

There's plenty of food for thought in our supplement. It provides just a small sampling of notable devices currently available but will trigger off sufficient ideas to keep our imaginative readers busy for quite awhile.

## PRICE INCREASE

As readers will have discovered, the cover price of Practical Electronics has been increased to 45 p as from this issue. News of this decision came too late for mention in last month's issue. We very much regret the need for this increase, which is due to factors beyond our control.
F. E. BENNETT,

Editor.

EDTORIA

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## Letters

Queries regarding articles published in PE should be addressed to the Editor, at the Editorial Offices, and a stamped, addressed envelope enclosed. We cannot undertake to answer questions regarding other items, nor to answer technical queries over the telephone.


Can be added to Minisonic for sequencing melodies or rhythm pattern

THE sequencer circuit to be described will enable a voltage controlled synthesiser to automatically play a pre-programmed tune, consisting of up to 32 pitches, in a sequence up to 128 notes long. All programs are keyboard initiated.

## BLOCK DIAGRAM

The heart of the sequencer is an nmos ram (random access memory) capable of storing 128 eight bit words of data. The circuit operation can best be understood by referring to the block diagram of Fig. 1. Here the ram is driven from a clocked binary counter. The binary number at the output of this defines the position in the memory that is present at the data terminals. The sequence is written into the memory via a modified 49 note keyboard which converts the 32 possible pitches into five bit words.

The 128 note sequence is built up by stepping the counter each time a new note is written in. When a sequence is complete, it is played by clocking the counter at a steady rate by means of the clock oscillator. The five bit words are then read out from the memory into a digital to analogue converter ( $\mathrm{D}-\mathrm{A}$ ) which produces a 32 level output. This is used to drive the v.c.o. in the synthesiser.

## SEQUENCE LENGTH

Although the maximum sequence length available is 128 notes, it is often desirable to use a shorter sequence. For example, if the tune to be written consists of 32 bars with three beats to the bar, it is obvious that the total number of beats would be only 96. To cope with this type of situation the circuit was designed so that the counter could be reset at any desired point in a sequence, thus producing tunes of any length from 1-128 beats.

Only five of the eight bits of memory are used to produce a control voltage for the v.c.o., the other three bits are available to perform other functions. One of these spare bits is used to provide the variable reset function, and the other two bits are used to generate trigger pulses for envelope shapers, thus adding rhythm to the generated melody.

## CLOCK OSCILLATOR AND COUNTER

The complete circuit is shown in Fig. 2. Here clock pulses are produced by a simple transistor astable multivibrator. The frequency may be varied over a wide range by adjusting VR1. Clock pulses are fed to the binary counter via $S 1$, the stop/run switch.


Fig. 1. Block diagram of sequencer


Fig. 2. Complete circuit of sequencer


Fig. 3. IC3 pin-outs and internal block diagram

ICl and 2 are cascaded to form a seven bit binary counter which drives the address inputs of the ram. The stop/run switch disconnects the first stage of the counter and instead provides the counter with pulses from the keyboard. The reset inputs of ICl and 2 are connected via S4 and S2 to one of the data lines of the ram, the

## COMPONENTS . . .

| Resistors |  |
| :---: | :---: |
| R1 $1.5 \mathrm{k} \Omega$ | R20 18k $\Omega$ |
| R2 $22 k \Omega$ | R21 $27 \mathrm{k} \Omega$ |
| R3 $22 k \Omega$ | R22 $120 \Omega$ |
| R4 1.5 k , | R23 $6.8 \mathrm{k} \Omega$ (see text) |
| R5-19 1kS (14 off) |  |
| All $\frac{1}{4}$ W 5\% carbon |  |
| Capacitors |  |
| C1 $10 \mu$ F elect. 25 V | C4 $10 \mu \mathrm{~F}$ elect. 25 V |
| C2 $0.01 \mu \mathrm{~F}$ | C5 $0.22 \mu \mathrm{~F}$ |
| C3 $16 \mu \mathrm{~F}$ elect. 25 V | C6, $70.01 \mu \mathrm{~F}$ |
| Integrated Circuits |  |
| IC1 7493 | IC5 7402 |
| IC2 7493 | IC6 ZN425E |
| IC3 MCM6810L | IC7 741 |
| IC4 74121 |  |
| Transistors and Diodes TR1-3 BC184 or similar D1-90 Any general purpose type |  |
|  |  |
|  |  |
| Relay |  |
| RLA D.i.I | single pole |
| Variable Resistors |  |
| VR1 $2 \mathrm{M} \Omega$ pot. (lin.) |  |
| VR2 $10 \mathrm{k} \Omega \mathrm{min}$. preset |  |
| VR3 $10 \mathrm{k} \Omega \mathrm{min}$. preset |  |
| Switches |  |
| S1 s.p.c.o. miniature toggle |  |
| S2 d.p.c.o. miniature toggle |  |
| S3 single pole miniature toggle |  |
| S4 miniature push to break switch |  |
| S5 miniature push to make switch |  |
| S6 miniature push to make switch |  |
| S7 miniature push to make switch |  |
| S8 miniature push to make switch |  |
| Miscellaneous |  |
| PCB board, front panel material |  |
| Veroboard for diode mounting |  |

automatic reset pulse is written into this line by selecting "Reset Write" with S2 and depressing S5.

Returning S2 to the "Reset Read" position reconnects the data line to the counter resets. Thus, when the end of a sequence is reached, the reset data line goes high and the counters reset to zero.

## RANDOM ACCESS MEMORY

Integrated circuit IC3 is a RAM, type MCM6810 designed for use with the M6800 microprocessor system. The block diagram and pin outs of the device are shown in Fig. 3. Pins 4-9 are data input/output terminals, the state of pin 16 deciding whether the device is in the read or write mode.

Pins 17-23 are the memory address inputs. The binary code fed to these pins determines which of the 128 memory cells is connected to the data terminals. Thus, when the clock and counter are running, each memory cell in turn is presented at the data terminals of the chip.

## KEYBOARD BINARY CODER

In the prototype synthesiser a four octave keyboard is used to write the required sequence of notes into the memory. This accomplished by diode keying circuitry of Fig. 4. It will be seen from this that each contact connects the five data lines to the five volt rail via a combination of diodes.

These are arranged so that a binary number corresponding to the number of the key pressed appears on the data lines. The five data lines, plus an extra line for key one are also routed through diodes to a monostable IC4 which generates a read/write pulse at pin 16 of the RAM, so that whenever a key is pressed, the binary code appearing on the data lines is written into the memory.

IC4 also produces a clock pulse which drives the counter.
Therefore operation of any key causes three things to happen:

1. A binary number corresponding to the number of the key will appear on the data lines.
2. A write pulse will occur at pin 16 of IC3.
3. The trailing edge of the pulse from IC4 will clock the counter and hence step the memory on one position.

## ENVELOPE TRIGGER OUTPUTS

There are eight data lines in the ram. As already mentioned, five of these are used to produce pitch information, and one to provide the automatic reset facility. The two spare data lines are used in the prototype to store trigger pulses for the synthesiser's envelope shapers.


Fig. 4. Diode keying from keyboard to main sequencer circuit


Fig. 5. Trigger inverter


Fig. 6. Alternative output circuitry

Push button switches S7 and S8 are used to write in the trigger pulses when required. When the circuit is in the read mode, the outputs from pins 3 and 2 of IC3 are gated in IC5 with clock pulses. This ensures that whenever two consecutive pulses are written, two separate pulses appear at the output. Without the gating, only one long pulse would be produced.

It should be noted that the trigger pulses produced are positive-going, and are suitable for driving either of the ADSR envelope shaper circuits that have appeared recently in this magazine. The es/VCA circuits of the Minisonic however, require negative-going pulses. These can be produced, if necessary, by the simple circuitry of Fig. 5 (three of these are needed).

The keyboard is fitted with two sets of contacts, one being used to drive the coding diodes, the other to drive a resistor chain for normal playing. For normal playing, a separate envelope trigger output is provided from the point which drives IC4. If the keyboard isolating relay (Minisonic Mk. 2) is being used it can be driven as shown in the main circuit diagram. (If not TR3 and associated components may be omitted.)

## D-A CONVERTER

Early versions of the prototype utilised a number of different $\mathrm{D}-\mathrm{A}$ converters, all of them using discrete components. All the circuits tried suffered from one problem or another, and all had the disadvantage of needing close tolerance resistors to function accurately. The integrated circuit D-A finally decided upon solved all these problems, although at somewhat increased cost.

The D-A chip feeds an inverting op-amp with gain and offset controls. The voltage at the output of the op-amp is of the correct sense for the Minisonic v.c.o.s, i.e. it is negative going for increasing pitch. For oscillators requiring positive-going control voltages the alternative output circuitry of Fig. 6 can be used.

NEXT MONTH: Construction and programming detail.

THis battery powered unit displays a subject's reaction time on a "non related" scale from one to nine, and although pocket sized, it is simple to construct, costing in the region of five pounds.

It should be made clear that the device is not intended to indicate reaction delay on a true scale of time, such as in milliseconds, because generally speaking the usefulness of a simple reaction timer lies not in measuring reactions precisely in fractions of a second, but in comparing them.

If the object of the exercise is to sharpen one's personal reaction time, or to compare yours with another's, then it is of little consequence if the readout is, for example, 170 ms , since this may mean little to a subject in any case!

## Digital hiflion



This novel and robust unit was designed to fill the slot requiring simple indication, and not expensive precision timing. Digital operation with numerical display was chosen however, because this eliminates argument over the results. It also precludes the possibility of a declining reading due to a discharging capacitor while the argument takes place, something which can happen with some analogue types.
The scale factor can be set to measure only those reaction times likely to be attained, and when the one to nine range of this device has been expanded to the desired time limit, it will be found to have adequate resolution, leaving no scale redundancy. This freedom to adjust the "difficulty" aspect should be found useful.

## USING THE TIMER

A reaction timer must provide the user with a subtle, but clear signal to which he can react. In this circuit, it takes the form of the seven segment display decimal point, which lights up after a semi-random time delay. After switching on, the display either remains blank, or shows a spurious number. The user then pushes the button on the front panel, and waits. Any number on the display will then be cleared.
When the signal l.e.d. illuminates, he must release the button as quickly as possible. Providing he was not so slow as to be "unclassified", his response time will remain displayed, and the lower the figure, the better. Should he attempt to cheat, or if he misses the signal altogether, the display merely remains blank. For another try, the button is pushed again, whereupon the display resets and the signal is awaited once more.

COMPONENTS

| Resistors |  |
| :--- | :--- |
| R1, R2 | $1 \mathrm{k} \Omega \frac{1}{4} \mathrm{~W} 5 \%$ |
| R3 | $100 \mathrm{k} \Omega \frac{1}{4} W 5 \%$ |
| R4 | $47 \Omega \frac{1}{4} W 5 \%$ |
| R5-R11 | $220 \Omega$ (7 off) $\frac{1}{4} W 5 \%$ |

Potentlometers
VR1 $220 \Omega 0.1 \mathrm{~W}$ vert min preset
VR2 $\quad 1 \mathrm{k} \Omega 0.1 \mathrm{~W}$ vert min preset
Capacitors
C1-C3 $100 \mu \mathrm{~F} 10 \mathrm{~V}$ elect (3 off)
C4 $\quad 0.1 \mu \mathrm{~F}$
Semiconductors

| IC1 | 7413 | TR1 | BC108 |
| :--- | :--- | :--- | :--- |
| IC2 | 7400 | D1 | 1N4148 |
| IC3 | 7493 | D2 | 1N4001 |
| IC4 | 7447 | X1 | DL707 |

## Switches

S1 Min slide switch ( $\frac{1}{2} \mathrm{~A}$ )
S2 Push-to-make push button

## Miscellaneous

Aluminium box $100 \times 70 \times 38 \mathrm{~mm}$ (type AB9, available Maplin)
Printed circuit board
Offcut of plain matrix board
Píece of copper laminate board
Battery holder for four HP7 cells, and connector stud
Socket, d.i.I. 14 pin
Four stand-off pillars (approx 23 mm )

## THE CIRCUIT

The complete circuit diagram is shown in Fig. 1, and may be divided into three functional sections: (a) The Delay Pulse Generator, consisting of ICla and its associated components. This drives the signal l.e.d. and initiates a timing cycle via the latch comprising IC2a and IC2b. (b) The Clock/Counter section formed by IC1b and IC3, which performs the actual timing operation, and (c), the Display Decoder/Driver (IC4), along with display X1.

Consider the circuit with S2 held closed. To start with, the 4 bit binary counter IC3 is held in reset because pins 2 and 3 are held high by the set/reset latch. Periodically, at about once every 5 seconds, the Schmitt Pulse Generator produces a brief positive going pulse. Transistor TRI is necessary in this circuit because the
low, pulled down by R1. This disables the clock oscillator, clamping the output high, and in turn arresting counter IC3. The BCD information on the outputs of IC3, is decoded continuously by IC4, to be displayed on X 1 . Therefore, when IC3 stops counting, a number corresponding to the reaction time is held on display until S2 is pushed for another try.

The zero blanking facility of the 7447 has been used to conserve battery power, and to eliminate distraction whilst awaiting the signal.

Gate IC2d is added, in order to inhibit pulses from the Delay Pulse Generator to the latch, when S2 is open. Without this, the latch could, under certain circumstances, be set with the push button up, which would cause a count the moment it was pressed. But as it stands, it is possible for the generator to be at any point in its


Fig. 1. Circuit diagram of the Digital Reaction Timer
minimum frequency that can be obtained from the simpler form of Schmitt oscillator, is too high for this application. Diode D1 modifies the mark space ratio of the output.

This periodical pulse is inverted by IC2d while pin. 12 is high, and is used to set the latch. The output on IC2 pin 3 then goes low. This event causes two things to happen. The signal light comes on immediately, and C3 commences discharge through VR2, and when the voltage across C3 is sufficiently low, counter IC3 is enabled, thus allowing it to be clocked by the other Schmitt oscillator comprising ICIb and VRI, etc. which runs at about 50 Hz .

If S 2 remains closed, IC3 will continue counting until it reaches 1010 (the binary equivalent of 10 ), when both inputs of IC2c will be satisfied, causing a low output. This will reset the latch again, forcing IC3 back to zero. With the arrival of the next pulse from the Delay Generator the whole cycle will be repeated.

If $\mathbf{S} 2$ is opened during one of these timing periods, however, the input on pin 9 of IC1b immediately goes
cycle at the instant of pressing S2. The signal can be expected at any time, ranging from almost immediately, up to about five seconds.

The circuit should be powered by four HP7 batteries. Diode D2 is necessary to drop the supply voltage to less than 5.5 volts, the maximum permissible for TTL. It will also protect the circuit from reverse polarity.

## CONSTRUCTION

The prototype circuitry was housed neatly in an aluminium box, using a simple mounting method that avoids the use of nuts, bolts or screws, other than a pair of small self-tappers for securing the lid.

All the components are readily available types, the only proviso being that the capacitors, resistors, and presets are not too large physically. A recommended p.c.b. layout is shown in Fig. 2, employing a fair number of wire links on the component side of the board, so that the copper pattern is kept reasonably simple. The component layout is shown in Fig. 3.

## (DICHITM REMOTIOMN THMER



Fig. 2. Printed circuit board (full size)

Fig. 3. Component layout and interwiring to off-board components



The left-hand blank p.c.b. plate is shown in detail above, and can be seen in position with the right-hand plate in the adjacent photograph


The method of fixing everything together can be seen in the incidental photographs. Two pieces of blank p.c.b. are cut out and stuck to the lid around the switch and display holes, with the copper side facing upwards. The display unit is mounted on a small piece of unclad perforated board ( 0.1 inch pitch), and a 14 -way i.c. holder is pushed on from behind to secure it. Loops of tinned copper wire can now be passed through the perforated board and soldered to the copper cladding. A piece of red tinted plastics film can be placed over the display before fastening it. The switch S1 can also be soldered to the cladding by means of its mounting lugs.

When assembling the p.c.b., it is quite in order to solder the i.c.s directly to the board, providing this is done with care. Nevertheless, a socket ought to be used for XI, as this allows it to be disconnected from the flying leads to the p.c.b. during wiring up. Flying leads also connect the p.c.b. to push button $\mathbf{S} 2$, the battery positive via S1, and battery negative.

## FINAL ASSEMBLY

At this point, with all the connections made, the unit may be tested, and if all is well, the p.c.b. can be attached to the lid. First solder four pieces of stout wire perpendicularly to the lid, on the copper clad plates previously glued to same. Position them in a square configuration to match the mounting holes of the p.c.b. A stand-off pillar is then placed over each, and the p.c.b. is threaded over the protruding wires, onto the pillars, and soldered at each corner, The p.c.b. is mounted component side down; so the stand-off pillars must be long enough to keep the components clear of the display socket, yet not so long as to exceed the space within the box. If you have an expired ball point pen of the hexagonal plastics tube type, this could be cut to provide the spacers.

Finally, snip off any surplus wire from the p.c.b. and tape the bottom of the box to prevent shorts occurring. The battery holder should fit tightly into the recommended box, and require no other fastening, but precautions may be necessary to prevent the self-tap screw from biting into one of the cells when this lid is finally secured.

## ADJUSTMENTS

There are only two of these; namely clock frequency, and commencement delay, controlled by VR1 and VR2 respectively. Both of these presets are accessible with the p.c.b. in place.

It is entirely up to the user as to how these are set, but the most useful setting is realised with a relatively high clock frequency, and the delay adjusted so that an average reaction time scores 5 or 6 . The higher the clock frequency, the higher the resolution

NEWS BRIEFS

## System X

Contracts worth $£ 20$ million have bee placed by the Post Office with British manufacturers, as the next step in the System X project, the biggest development ever undertaken in British telecommunications.
It covers the design of trunk, tandem, and small! medium capacity local exchange equipment, based on microelectronic and software control technologies, and will carry the telephone system into the 21 st Century.

Already some 500 engineers are involved in System $\mathbf{X}$. a modular system which should lay the foundations for an expanding range of future customer facilities, and is expected to cost more than $£ 100$ million.

## CES Ho Longer

OSeptember 1st, 1977, Combined Electronic Services Ltd, the service company for Philips and Pye household products, changed its name to "Philips Service".

Now part of the recently announced Philips Industries: new Central Merchandising Management Group, Philips Service (claimed to be the largest manufacturers service organisation of its kind in the UK), will continue to be responsible for the total provision of after sales service support for the Philips and Pye Consumer Division.

A new computerised order handling system was intro-duced, which is a customisation of a package already used in Europe by Philips Services. The basic philosophy is to provide the best possible service support on a local basis, by the creation of 25 Service Centres.

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FRANK W. HYDE

## SPACE SUITS

The advent of the space shuttle brings many changes in space methods and activity. One of the most important of these changes is that of the space suit. The Apollo suits had certain disadvantages which became apparent in use and were costly indeed since each suit was virtually tailored to fit and made one mission only. The same applied to the backpacks and life support systems. The new suits will be less than half the cost.

Contrasting with the Apollo suits, the new generation of space suits will have a life of fifteen years. Many missions will be flown during that time. The new suits have a rather different arrangement from the moon suits. For example, the moon suits were pressurised and designed for the $1 / 6$ gravity of the moon. With the extra vehicular activity (EVA) of Spacelab and similar missions, zero gravity will be the norm. Also a quick turn round is necessary. The Apollo suits required about 90 minutes to don and check but the new ones will take only 15 minutes. The actual donning time is about 5 minutes.

## CONSTRUCTION

The construction of the new suits is such that there are two parts. The torso and backpack are integral and hard. This allows life support systems to be solid and internal as against flexible and external in the moon suits. The lower half is soft and is "stepped into". In dressing the lower half is donned first and then the arms head and torso are "inserted" in the top half which is in a support on the wall. The two halves "of the suit are closed by a ring.

Added to the ease of dressing is the extra mobility which is obtained using joints of constant volume in place of the pulley joints in the Apollo suit. There is also another important advantage in that whereas the Apollo suit worked against the effont of the astronaut the constant volume system enables free movement without great effort.
Another basic difference between the Apollo suit and the shuttle suit is the fact that Apollo had zippers which could leak whereas the shuttle ring closures are virtually leakproof. The pressure bladder used in Apollo is now replaced by a polyurethane bladder which has seams sealed by heat. The Apollo suit had latex bladders which were tape and glue sealed.

## MONITORING

The new suit will be easier to monitor, as to status, than the old ones. A microprocessor/light emitting diode unit will tell the astronaut whether there is a problem with the suit systems and what to do about them. The Apollo suits had an electric warning system but no instruction readout to tell the astronaut what to do about it. The microprocessor, which is carried in the chest pack, is a great advantage in the new suit.

The joints in all the suit electronics are solderless. These necessary joints caused trouble in the Apollo suits. The arrangement of suit/backpack design places all controls where the astronaut can see them. The 12 character readout display replaces the Apollo "cuff card" systems where warnings from the suit had to be checked by reading procedure lists carried on the sleeve.

The new suits will not be allocated to individuals. Each astronaut will choose the one he or she likes. The suits will be in three basic sizes allowing for the accommodation of male or female participants. A different urine collection system will be required but the final details will await the choosing of female astronauts.

## COOLING

The liquid cooling garment which is worn by the astronaut is fitted with ventilation tubes. Oxygen is fed in through the helmet and taken to the hands and feet then returned through the backpack for reuse after conditioning. The initial length of extra-vehicular activity for the missions can be up to 7 hours. Oxygen pressure will be 4.1 psi. Astronauts will have to pre-breathe oxygen at 4.1 psi for 3 hours before extra-vehicular activity to denitrogenate the blood to avoid "bends". As little work will be required to be done with their legs, as on Apollo moon mission,
there is less loading and metabolic activity.

Recharging of the systems will take only a few minutes. Battery recharging will only take an hour while replacement takes only a few minutes. Crew and specialists will wear suits for their activities but if it should be necessary to move other personnel to or from shuttle to installation this will be done in a sphere mancuvred by astronauts.

## SPINNING SOLAR SAIL

Another propulsion system, for the mission to Halley's comet in 1986, is being studied by NASA. This is a rotating sail system. It consists of 12 sails each 4 miles long by 28 ft wide.

The sails would be unfurled by centrifugal force after deployment of the vehicle from the space shuttle. The pressure of the solar wind would spin the sails and gradually accelerate the craft to the rendezvous point. The time of spin is expected to be one revolution every three minutes.

This system is now favoured over the square sail version. It is competing with the ion motor. A decision is expected soon.

## SPACE TELESCOPE

Lockheed-Missiles and Space have been chosen to build the new space telescope. The optics are to be supplied by Perkin-Elmer. Among these will be the 94 in diameter primary mirror. The space telescope is large being 43 ft long and 14 ft in diameter. The shuttle will launch it into Earth orbit in 1983.

## JUPITER ORBITER PROBE

The house of representatives voted out the funds for the Jupiter orbiter probe mission. There has been a reversal of that decision now and the budget for 1978 has been restored. The orbiter Jupiter Probe is now ratified by the Senate Appropriations Sub-committee.

This is an important mission in view of a number of new facts regarding the largest planet in the solar system. The cost of the two spacecraft and ancillary requirements including launching is estimated at some 450 million dollars.

Orbiters will be launched by shuttle and will be the first payload to go into deep space. It will also be the first payload to be boosted by the upperstage. The probable date of launch will be January 1982 and the encounter with the planet will be late 1984.

An aeroshell will be released to descend into the Jovian atmosphere from where radio information will be received for the first time.

## Kx goon

## SIMPLE ELECTRONICS FOR MODELLERS

By I. R. Sinclair
Published by Argus Books Ltd.
110 pages, $140 \times 215 \mathrm{~mm}$. Price $£ 2.95$
|N times gone by, it would have seemed ridiculous to electronically control something like a model railway, using valves and relays as large as the locos themselves. But the birth of microcircuits has reversed this situation to create a new branch of interest, and this book is based on such techniques, covering current and voltage control, generating signals and delays, measurement, counting and logic circuits, motor speed control, power supplies and p.c.b.s.

In the book, which is intended as a "methods" source rather than an instructional manual, the author proposes that many of the skills required by the modeller, are similar to those required for modern electronics construction.

## RADIO CONTROL FOR MODELS

## By R. H. Warring

Published by Pitman Publishing Ltd.
213 pages, $194 \times 255 \mathrm{~mm}$. Price $£ 6.95$
Extensively revised, this second edition of Radio Control For Models is mainly about "proportional" control, and starts with some historical notes which prepare you for a chapter on basic radio theory; but it's not too technical! In fact, the aim of the book is to show that your can treat all the electronics as simple black boxes, and just concentrate on the modelling aspect of the hobby.

There are no constructional features, although diagrams and photos of R/C "bits and pieces" are included, along with explanations of their basic principles. Practical workshop hints are given, and it is in this chapter that a jolly photograph appears showing various types of miniature switches compared to a threepenny piece-for those who can remember them!

## ELECTRONICS FAULT DIAGNOSIS

## By I. R. Sinclair

Published by Argus Books Ltd.
108 pages, $138 \times 216 \mathrm{~mm}$. Price $\mathbf{£ 2 . 7 5}$

c.IRCUITS in this book are graded, starting with the most simple and working upwards. There is no particular tendency towards domestic equipment, since much of the servicing guidance given applies to industrial or communications type electronics. This book should be useful to students studying the C \& G 272 and 222 courses.

The chapters are: Power Supplies, Audio Frequency Amplifiers, Timing Circuits, Measuring Circuits, Oscillators, Trigger Circuits, Control and Interface Circuits, and Digital and Counting Circuits.
Each chapter comprises one or more circuit diagrams with corresponding sets of voltage readings, or oscillograms, for certain points. After taking in the circuit description, it is then up to you to deduce which set of readings is correct.

The answers are in the back of the book, along with an explanation of which component failures would have caused the other incorrect readings shown.

The effect on voltages of various types of measuring instrument is also covered, and in some tables your are expected to take such loadings into account when seeking the right answer. This book is not for the absolute beginner.


## PQACTICAL



OUR DECEMBER ISSUE WILL BE ON SALE FRIDAY, NOVEMBER 11


## FOR 74 FAMILY OF QUAD-GATE PACKAGES

THIS gate tester was designed to be cheap, and to be capable of testing a wide range of simple QUAD-GATE packages. The unit works by applying to each gate in the i.c. under test, every possible combination of inputs, and monitoring the outputs with l.e.d.s.

## TEST SOCKETS

There are two basic pinout configurations used in the 7400 series of quad gate packages, and these are illustrated in Fig. 1, where the 7400 , and the 7401 are shown.

Two i.c. sockets are fitted in this tester, to accommodate each pin arrangement.

## THE CIRCUIT

Referring to Fig. 2, the 555 timer (IC1) is wired as an astable multivibrator with a frequency of about 2 Hz . The output from this is fed to at 7470 flip-flop (IC2), which divides the signal by two. This, and the original oscillator signal are taken to every gate in the i.c. under test; each


Fig. 1. Pin configurations of the 7400 and 7401

## COMPONENTS . . .

## Resistors

$$
\begin{array}{ll}
\text { R1, R2 } & 10 k \Omega \frac{1}{4} W 5 \% \text { (2 off) } \\
\text { R3-R10 } & 390 \Omega \frac{1}{4} W 5 \% \text { (8 off) }
\end{array}
$$

## Capacitors

## C1 $47 \mu \mathrm{~F} 10 \mathrm{~V}$ elect

C2 $22 \mu \mathrm{~F}$ 10V elect

## Semiconductors

| D1-D8 | 0.2 in red l.e.d. |
| :--- | :--- |
| IC1 | NE555 Timer |
| IC2 | 7470 |

## Miscellaneous

Verobox type $65-2518 \mathrm{H}$
Veroboard 0.1 in
Red 4mm terminal (SK1)
Black 4 mm terminal (SK2)
14 pin d.i.l. sockets for test positions (2 off)


Fig. 2. Circuit diagram of the TTL tester. A capacitor of $0.01 \mu \mathrm{~F}$ connected from IC1 pin 5 to ground may be found necessary for reliable operation
signal going to each of the two inputs. These input waveforms are shown in Fig. 3, and the correct output for a 7400 is shown as an example.

The outputs, drive l.e.d.s. D1 to D8, causing them to illuminate when the signal generated by the gate under test is low, thus allowing open collector type gate to be tested with this system.

Testing a 7400 , it can be seen from Fig. 3 that the output l.e.d.s should be on for one quarter of the total waveform period. This, and the relationships for other quad gate packages, can be seen in Table 1.

Table 1. Output l.e.d. illumination times for correctly operating gates. Ten 74 series quad gate packages are shown

| Package type | Test socket | l.e.d. duty cycle |
| :---: | :---: | :---: |
| 7400 | B | $25 \%$ |
| 7401 | A | $25 \%$ |
| 7402 | A | $75 \%$ |
| 7403 | B | $25 \%$ |
| 7408 | B | $75 \%$ |
| 7409 | B | $75 \%$ |
| 7428 | A | $75 \%$ |
| 7432 | B | $25 \%$ |
| 7433 | A | $75 \%$ |
| 7438 | B | $25 \%$ |



Fig. 3. Test waveforms applied to each gate. The correct output for a 7400 is shown


Fig. 4. Stripboard layout of prototype

## CONSTRUCTION

The basic circuit was assembled on a piece of stripboard (see Fig. 4), which was then mounted in a small polystyrene case, by the integral mounting pillars.

The lid of the case was cut to accommodate two 14 pin i.c. holders, and the eight l.e.d.s. Dimensions will depend upon the type of l.e.d.s preferred, and i.c. holders used, but the photographs will show the general layout involved.

The l.e.d.s can be fixed, either by adhesive, or using the proper bezels, and the i.c. holders will best be mounted
each on a small square of stripboard, to which they can be soldered. The plate so formed, can then be used to glue the holder to the lid.

Cut holes for the two 4 mm socket terminals (SK1 and SK2), and mount these. Next drill the main component board so that it can be mounted in the base of the box.
A harness of four wires should be formed, to link the main board to the i.c. socket boards. This will carry the two signal lines, and the two supply lines. Wire both the i.c. socket units for +5 V and 0 V , and next, the two signal


In the prototype, the i.c. sockets were soldered to pieces of Vero. board which were then glued to the lid. The sockets and l.e.d.s were linked directly using the $390 \Omega$ resistors

Power is applied via the 4 mm terminals, but using a larger box would allow room for operation from an internal battery. An on/ off switch could be mounted in , place of the terminals

lines to all the appropriate pin numbers detailed in Fig. 2. The +5 V line should also be wired common to all the l.e.d.s (check for correct polarity), and the other side of each l.e.d. wired to its respectịve i.c. socket pin, by means of a $390 \Omega$ resistor (R3-R10).

The l.e.d.s should be wired up so that they are adjacent to the outputs they represent. The lid was lettered using dry letter transfers sprayed with laquer, and it may be advantageous to put the related pin numbers against each 1.e.d.

Finally, do not forget to connect up the two 4 mm terminals for the supply input.

## OPERATION

In use, the i.c. to be tested is inserted in the appropriate socket (use Table 1), power is applied, and the l.e.d.s will indicate the condition of the i.c.

A gate with a faulty output stage will cause the incorrect flashing of its associated l.e.d., and a gate with a damaged input stage will possibly cause all the l.e.d.s to flash incorrectly. The operator can learn to interpret the meaning of the various indications.

The prototype is powered by an external supply, but since current consumption is only about 30 mA average, battery operation is feasible.

## marker PLACE

ltems mentioned in this feature are usually available from electronic equipment and component retailers advertising in this magazine. However, where a full address is given, enquiries and orders should then be made direct to the firm concerned. All quoted prices are those at the time of going to press.

## CONDUCTIVE PAINT

After five years of selling exclusively to industry, Industrial Science Ltd., are now introducing one of their most successful products-Elecolit 340 -into the consumer electronics market.

This is a pure, silver filled, electrically conductive acryllic paint. It exhibits excellent conductivity because of the pure silver and outstanding environmental protection due to its acryllic base and sets by solvent evaporation similar to most good lacquer systems forming a tough film with good adhesion to ceramics, glass, rubber, plastics and most plastics films.

Typical applications include r.f. shielding, printed circuit repair, use as a conductive ink, prototype circuit manufacture
and one of the most interesting and unusual applications of all which is to repair the rear window demister of a car by means of painting over the existing track which may have either broken or shorted out.

Although it is air drying, conductivity can be improved by heating.

The shelf life is a minimum of 1 year in a closed container, and the operating temperature is from $-60^{\circ} \mathrm{C}$ to $+175^{\circ} \mathrm{C}$.

It can be applied by painting, silk screening or roller, and if necessary it can also be thinned with a solvent to lower the viscosity.

Details of price and further information can be obtained from Industrial Science Ltd., Leader House, Dept. P.E., 117-120 Snargate Street, Dover, Kent.


The Elecolit 340 conductive paint from Industrial Science


## ALARM CLOCK

A particularly elegant digital alarm clock, the Fairchild Timeband is available from Tempus.

Available in white or black, and taking up little more space on your bedside table than an old-fashioned mechanical alarm clock, the Timeband offers timekeeping and alarm accurate to the second.

The readout is on large sevensegment l.e.d. displays, showing hours and minutes or, at the touch of a button, last minute digit and seconds. Indicators are provided for AM/PM, Mains Failure, and Alarm On. The alarm should be loud enough to waken the heaviest sleeper, and includes a "doze" feature which can call you up to six times in an hour.

The Timeband costs $£ 14.95$, including VAT, post, packing and insurance, from Tempus, 19-21 Fitzroy Street, Cambridge, CB1 1EH.

# Semiconductor UPDATITE FEATURING : TMM142C h.L.c.D. 0024 LIm194 R.W. Coles 

## FORGET ME NOT

The nice thing about old fashioned magnetic core stores was that, like the elephant, they never forgot. Fill them full of lovely binary data and then hit the mainsoff switch, and next week when you switched on again it would all be just as you left it (brings tears to my eyes!).

Problem was, of course, that their uncanny resemblance to the elephant extended also to their physical bulk and their rather slow response, and those little drawbacks soon got them the chop when fast, cheap semiconductor RAM chips emerged from the undergrowth.

With semiconductor RAM of course, if you hit the power-off-switch all you end up with is a garbage, a problem the data processing industry decided it would have to live with if it wanted the other goodies on offer.

Where loss of data was a problem, non volatility could be arranged by providing battery back-up supplies, or by transferring crucial data to permanent storage media such as magnetic tapes or discs, but this proved either expensive or a headache for the software designers. In recent years the CMOS RAM has emerged to make the battery back-up solution more viable, with a stand-by life measured in years now possible with quite small batteries, but CMOS RAMs are expensive, slower, and less dense than their NMOS cousins and so the problem of volatility is still not completely solved.

A new solution to this problem has recently been introduced by Toshiba in the form of their TMM142C $256 \times 4$ RAM chip which uses a double cell in each bit position, to provide the rapid access read/ write capability of standard RAM combined with the non-volatility of the MNOS electrically alterable ROM technology.

The MNOS (Metal Nitride Oxide Semiconductor) alone is certainly non-volatile but it can't be used in place of standard RAM because writing and erasing data is slow and requires high voltages. By combining MNOS devices with conventional RAM circuitry the best of both worlds can be achieved. With power up, normal fast read/write access is possible, but when a power fail condition is detected the RAM data is transferred to the MNOS devices where it will remain for very long periods. When power is restored the stored data is duplicated in the RAM array ready for instant use. The data also remains in the

MNOS latches and must be erased before re-use by means of a positive pulse applied to the MG input.

## THE DRIVER

Liquid crystal displays are pretty, popular, offer extremely low power drain, and are, unfortunately, excrutiatingly difficult to drive.

Take a standard clock or voltmeter chip with multiplexed $B C D$ or seven segment outputs and any fool can interface it with the l.e.d., Minitron, or gas discharge display of his choice, but the thought of hooking it up to a $3 \frac{1}{2}$ digit liquid crystal panel makes brave amateurs buckle at the knees and even experienced designers cough nervously.

The l.c.d.s require an a.c. display drive supply of about 30 to 100 Hz , and they cannot be multiplexed, a combination completely alien to most likely display sources. To interface to a clock chip, for example, you would first have to demultiplex and latch each display digit, then wire these to the l.c.d. via decoders and exclusive OR gates, and finally provide an l.f. backplane drive source. A glance at the serried ranks of standard CMOS chips that you would need to hanig around your clock chip might well convince you that l.e.d.s are not so bad after all!

Well, you know what I was going to say next, didn't you. Yes, somebody has gone out and done it all for us again, a complete multiplexed BCD input, to decoded seven segment l.c.d. output display system on a single chip. Hughes Microelectronics are the people to blame, and the device in
question is the H.L.C.D. 0024 which is made using CMOS technology and lives in a 40 pin plastics package.

On its inputs, the H.L.C.D. 0024 talks directly to the $B C D$ and digit strobes produced by most clock and voltmeter chips, on its outputs, it speaks parallel seven segment a.c. drive liquid crystal. Two extra uncommitted drivers are available for use with plus/minus signs, decimal points or a.m. p.m. displays, and leading digit zero blanking is provided internally.

## THE PERFECT COUPLE

I remember spending hours with an AVO transistor analyser and a few dozen OC29 germanium power transistors trying to get a matched pair for use in an audio amplifier output stage. Well, I'm not sure that it was much help in the end, but I enjoyed myself anyway, there is something rather satisfying.

As a close approach to the perfect matched pair, National now produce the LM194 "Supermatch pair" which consists of two monolithic npn silicon transistors in a TO5 metal can. The emitter-base voltage match is within 50 microvolts, the current gain match to within 1 per cent, and the offset drift is less than 0.1 micro volts per degree $C$ which as far as I remember, is a hell of a lot better than I was able to do with my OC29s!

Match pairs such as the LM194 are useful where extremely high performance operational amplifiers or high accuracy analogue multipliers must be assembled.

Fig. 1. Low drift operational amplifier using the LM194


## B. BAMBER ELECTRONICS

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## DIGITAL INSTRUMENTS

The digital instrument market is becoming even more competitive. Never has so much been offered by so many companies, and prices are still tumbling. For any price range there is better value in specifications and facilities and you can now get a professional quality instrument for $£ 100$. Even that troublesome measurement of true r.m.s. can be yours for $\$ 150$.

The dilemma facing the manufacturers is whether to cut prices to the bone or hold them and build in more performance for the money. Those taking the middle course are giving their instruments an enhanced performance with a modest price cut.

In the scramble to present instruments in the best possible light there are some big claims being made. The thing to remember is that even with the latest LSI techniques which cut instrument assembly costs, long term accuracy still costs money. If you go for price alone, don't expect too much. And prices, as advertised, can be misleading. One instrument, for example, looks world-beating value with a boldly displayed price tag of under $£ 50$. But with carrying case and accessories, plus value-added tax, you can end up paying over $£ 60$.

The new trend is towards liquid crystal displays and smaller and smarter cases. For sheer smaliness there is one digital multimeter on the market which measures $48 \mathrm{~mm} \times 68.5 \mathrm{~mm} \times 99 \mathrm{~mm}$. It has a 7.5 mm l.e.d. display described as "big".

Another model has its rear moulded to conform to the wrist and back of the hand so it can be strapped on like a wrist watch. The idea is that you can work with both hands probing a circuit and right there in front of you on your wrist is the voltage or current or resistance read-out, this one with l.c.d. Another variation on the same
theme is for the whole of the multimeter to be built into the test probe.

In the UK it is estimated that over 60 per cent of low cost and general purpose digital instruments are now sold through instrument distributors as off-the-shelf items. And when you see that a digital panel meter can be bought in one-off quantities for as little as £25 you can understand the reason why.

## DISPLAYS

Electronic displays have become an industry within an industry with their own specialised exhibition and conference in London extending over three days. The displays sector of the electronics market is currently expanding at 25 per cent per year.
For sheer volume the calculator, clock and watch makers are the leading customers consuming billions of digits per year. The next huge market breakthrough, somewhat delayed but beginning to materialise, is the automotive market world-wide. The oldest form of electronic display of all, the cathode ray tube, has been given a new lease of life by the enormous growth of computer graphics and visual display units.

The problem of l.c.d.s being rather drab compared with l.e.d.s looks like being solved by a fluorescence acti-vated-I.c.d. developed by the West German Institute of Applied Solid State Physics. The new technique is said to give l.c.d.s comparable brilliance to l.e.d.s and a bonus is that a choice of colours in red, green or orange will be available. The product will be massproduced by Siemens next year.

## LOBBIES

Pressure groups, lobbies, call them what you will, multiply like bacteria. Do they do any good or do they neutralise themselves? I note that the antiFar East. electronics lobby is now counterbalanced by the International Consumer Electronics Association which represents importers and distributors of electronic goods from overseas including the powerful Japanese companies. ICEA members fear for the safety of their incomes if imports are restricted.

In all the sometimes secret, sometimes public wrangling, the poor old consumer often gets forgotten. The one irrefutable argument is that if the Japanese or any other nation can produce a better product at a cheaper price surely the man-in-the-street should be given the choice of buying it. Meanwhile, the free-traders and the protectionists seem to be winning.

The other great battle between lobbyists is the vexed question of Citizen's Band Radio. A statement released from the office of the Prime Minister concludes with, "It is a question of balance, and at present the Government feel that the badance of the argument is against the introduction of Citizen's Band'.

The operative words are "at present" so this leaves the door slightly ajar and the respective lobbies will battle on, each hoping for final victory.

## SAFETY FIRST

The "Earth Leakage Circuit Breaker" (ELCB) described by K. A. Smith in the July 1977 issue of P.E. seems to have aroused a lot of interest including a word of warning in our correspondence columns.

On the professional front $B$ \& $R$ Relays have been making them for years. But it has been a long uphill struggle getting the sales message across to potential users. Everybody wants safety but when it comes to the point, few want to pay for it.

The Health and Safety at Work Act of 1975 is beginning to change the situation and now Kevin Walker, B \& R's sales manager, is forecasting an immediate UK market of about $\Sigma 1$ million rising to $£ 5$ million or more by 1980. $B \& R$ are expecting to capture 25 per cent of the business.

Walker has made a good start by selling $£ 60,000$ worth of ELCB's to Watney Mann to protect the barmen and barmaids against faults on electric beer pumps in the Watney Mann chain of pubs. The next move will possibly be to fit them to the catering equipment in pubs.

They are currently working on six new models of ELCB's, all designed for ease of fit and designed to trip within 25 milliseconds of detection of a fault.

I note that K. A. Smith says that his intention was to fit a commercial model in his colour processing darkroom"but the frustration of trying to buy such an article for private use made me determined to make one for myself". Anyone interested in buying the commercial product could try contacting $B$ \& R Relays, Temple Fields, Harlow, Essex.

## BPO BLOODHOUNDS

The Post Office's Radio Interference Service which includes a fleet of specially equipped vehicles to sniff out illegal transmissions, man-made static and other forms of interference to radio and TV reception is in process of modernisation.

The Marconi Instruments and Racal Instruments are among the firms which will benefit. MI is supplying 94 type TF2015 signal generators and RI a similar number of their type 9915 frequency meters.

The controlling authority for the Service is the Home Office so the technical requirement was drawn up by the Home Office's Directorate of Radio Technology. Both companies are delighted that their products passed evaluation tests with flying colours.

# ANALOGUE/LOG AMPIIIIERS <br> <br> D. F. BOWERS, bsc 

 <br> <br> D. F. BOWERS, bsc}

MOST voltage amplifiers in present use are designed to have a linear transfer characteristic-in other words, to multiply the voltage at the input by a fixed factor-and to have well-defined impedances at the input and output. There are, however, amplifiers which are termed "non-linear", which multiply input voltages by a factor in some way dependent on the magnitude of the input voltage.

Many non-linear amplifiers are designed for specialist applications, but certain types which have more general transfer characteristics are useful in wider fields. In the latter category, one of the most interesting is an amplifier having a logarithmic or exponential transfer characteristic.

Because many sensing devices obey exponential laws (thermistors and photodiodes, for example), logarithmic amplifiers find uses here. Compression of a wide range of voltages into a more easily handled spread is also a common use of logarithmic amplifiers. In analogue computers, they are used in conjunction with exponential amplifiers to perform multiplication and division.

## WHAT IS A LOGARITHMIC AMPLIFIER?

If an amplifier has input voltage $\mathrm{V}_{\text {in }}$ and output voltage $V_{\text {out }}$, and if $V_{\text {out }} \propto \log \left(V_{\text {in }}\right)$, then the amplifier is said to be a logarithmic amplifier. If $V_{\text {out }} \propto \exp \left(\mathrm{V}_{\text {in }}\right), \exp \left(\mathrm{V}_{\text {in }}\right)=$ $\left.e\left(\mathrm{~V}_{\text {in }}\right)\right]$ or $\log \left(\mathrm{V}_{\text {out }}\right) \propto \mathrm{V}_{\text {in }}$, then the amplifier is said to be exponential or antilogarithmic.

A logarithmic amplifier in the feedback path of an operational amplifier converts the op. amp. into an exponential amplifier. Similarly an op. amp. with an exponential amplifier in its feedback path becomes a logarithmic amplifier. Hence, we need only find a way of achieving one type of transfer to create both types of amplifier.

## SHOCKLEY'S EQUATION

Although very expensive logarithmic amplifiers may use intermediate digital techniques, the vast majority of analogue logarithmic amplifiers rely on the intrinsic logarithmic behaviour of a semiconductor $p-n$ junction when subjected to low bias voltages.


Fig. 1. Forward bias current curve for a typical silicon diode

The familiar transfer curve for a typical silicon diode in the forward bias mode is shown in Fig. 1. As the voltage across the diode increases from zero to about half a volt, very little current flows, but above about 0.6 V the current increases rapidly. The inverse of this curve is shown in Fig. 2, where it can be seen that the voltage across the diode increases rapidly as the current approaches $\mathrm{I}_{0}$, and then more slowly until several milliamps is achieved, when the diode's bulk resistance becomes important. Between these two current values, the voltage increases (approximately) in proportion to the logarithm of the current.

To explain this, it is necessary to investigate an equation derived from statistical considerations by W. Shockley, which states:

$$
I=I_{0}\left(\exp \left(\frac{q V}{k T}\right)+1\right) \ldots \ldots(1)
$$

where
$1=$ Current through junction (amps)
$1_{0}=$ Theoretical reverse current (amps)
(This is the same $l_{o}$ as previously described)
. $V=$ Voltage across junction (volts)
$\mathrm{q}=$ Charge on the electron (coulombs)
$\mathrm{k}=$ Boltzmann's constant
$\mathrm{T}=$ Junction temperature (kelvin)
If qv> $k T$, a condition normally satisfied, then:

$$
\begin{equation*}
V=\frac{k T}{q}\left(\ln I-\ln I_{0}\right) \tag{2}
\end{equation*}
$$

(where $\ln =\log _{\mathrm{e}}=$ the natural or Naperian logarithm)
and hence we obtain logarithmic behaviour. Departure from this equation is mainly due to qV approaching kT at low currents, to the effect of the bulk resistance at high currents, and to misbehaviour of the semiconductor junction in between.
The latter problem can be solved to some extent by using diodes designed to have a good logarithmic behaviour (such as type G130), but not very much can be done to better the


Fig. 2. Forward bias voltage curve for a typical silicon diode

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extremes. Even so, a range of over seven decades of current can be accommodated if great care is taken in the design of the logarithmic amplifier.

## SIMPLE LOGARITHMIC AMPLIFIERS

A simple logarithmic amplifier based on the principles described is shown in Fig. 3. Assuming a positive input signal, the inverting input of the op. amp. will be maintained at virtual earth (by normal feedback action), and so the input current is $V_{1 n} / R$. This current must also flow through the diode, and hence we can show that:

$$
\begin{align*}
V_{\text {out }} & =-\left(\ln \frac{V_{\text {in }}}{R}-\ln \mathrm{I}_{0}\right) \frac{\mathrm{kT}}{\mathrm{q}} \\
& =-\left(\ln \mathrm{V}_{\mathrm{in}}-\ln \mathrm{R}-\ln \mathrm{I}_{0}\right) \frac{\mathrm{kT}}{\mathrm{q}} . \tag{3}
\end{align*}
$$

Thus there is a region where (at constant temperature) the output is proportional to the logarithm of the input. In this region, the output moves about 60 mV (at $25^{\circ} \mathrm{C}$ ) for every decade change in input voltage, but this can be increased by using several diodes in series. The main drawback of this arrangement, however, is temperature dependence.

Besides the $\mathrm{kT} / \mathrm{q}$ term outside the brackets, the term $\mathrm{I}_{0}$ is also very dependent on temperature, and on the physical construction of the junction. It effectively causes the output level to shift up and down with small fluctuations in temperature. Although this can be corrected with simple amplifiers of this type, it is more common to replace the diode with a transistor, the base-emitter junction being used as the logarithmic law generator. A "differential" compensation method is then relatively simple to implement. Details of a practical amplifier will now be given, for the benefit of those who may wish to experiment.

## A COMPENSATED LOGARITHMIC AMPLIFIER

Although the temperature problems can be solved by "ovening" the junction to keep it at a constant temperature (as in the G. D. Shaw monolithic oven used in the PE Sound Synthesiser), this arrangement is not always satisfactory, and can be difficult to set up. We will therefore explore an alternative system.

If $\mathrm{qV}>\mathrm{kT}$, then the relationship between the collector current ( $\mathrm{I}_{\mathrm{c}}$ ) and base-emitter voltage ( $\mathrm{V}_{\mathrm{BE}}$ ) of a transistor will be:


Fig. 4. Practical logarithmic amplifier utilising the differential compensation technique


Fig. 5. Thermistor compensation circuit to be used in place of $\mathbf{R 1}$ in Fig. 4. The thermistor should have a resistance of $10 \mathrm{k} \Omega$, at $25^{\circ} \mathrm{C}$

## AN IMPROVED AMPLIFIER

The form of logarithmic amplifier described above has three major drawbacks which limit its overall performance.

1. The dynamic range is limited to about three decades of input voltage, due largely to the relatively high input offset (about 2 mV ) and bias current (about 100 nA ) of IC1.

The former can be improved by using as large an input signal as possible, together with a high value for $\mathrm{R}_{\mathrm{in}}$. To improve the latter, however, an f.e.t.-input op. amp. (such as the NE536T) should replace ICl . It should be possible to achieve over six decades range with this configuration.
2. The current $I_{\text {ret }}$ does not remain constant, because the non-inverting input of IC2 is not a true virtual earth. This is not too important with power supplies in the range $10-15$ volts, but for greater accuracy $V_{\text {ref }}$ and $R_{\text {ret }}$ could be replaced by a 1 mA current source.
3. Last, but not least, the $\mathrm{kT} / \mathrm{q}$ term in equation (5) introduces a temperature dependence. This causes the scale factor to alter with variations in absolute temperature. The error over normal domestic temperature variations will not exceed about $\pm 2.5$ per cent, which will be adequate for many applications.

Special temperature proportional resistors have been developed to compensate for this error over wide temperature ranges, but these are neither easy to obtain, nor cheap. In Fig. 5 is shown a method of compensation using a resistorthermistor network in place of R1 in Fig. 4. This circuit was designed by a colleague, Mr C. R. Francis of Sheffield University, and provides good compensation over the limited temperature range of a domestic environment, if greater accuracy is required.

## EXPONENTIAL AMPLIFIER

To obtain an exponential amplifier, it is only necessary to rearrange the components of Fig. 4, as shown in Fig. 6. If $V_{\max }$ is the maximum output voltage, then $I_{\text {out }}=V_{\max } / 1 \mathrm{k} \Omega$. Potentiometer VR5 is adjusted to give $V_{\text {out }}=V_{\text {max }}$ when $V_{\text {in }}$ is zero, and VR2 again sets the scale factor, which is adjustable over the range 0.43 decades/volt to 1.33 decades/volt.

## INTEGRATED CIRCUIT TECHNIQUES

,The amplifier system described, with its need for closely matched transistors and good op. amps., would seem a good subject for integration, and indeed this has been done by several manufacturers. Unfortunately, i.c. logarithmic amplifiers of good quality are not very cheap, but two which have proved to be good all-round performers are the Intersil 8048 (logarithmic) and 8049 (exponential) amplifiers.

The configuration of these amplifiers is basically a monolithic version of those already described, with dual f.e.t.-input op. amps. Fine temperature compensation is carried by means of a specially designed thin film resistor instead of the resistorthermistor network, and this is effective from $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$. The 8048 features a 60 dB voltage input range, and a 120 dB current input range.

## BANDWIDTH CONSIDERATIONS

Bandwidth is always a problem where semiconductor junctions operate at low currents, due to capacitive phenomena across the narrow junction. To a first approximation, the bandwith of a logarithmic amplifier will increase proportionately to the average current through the junction concerned, assuming that the perturbations are small.

It follows that to obtain the best frequency response from a logarithmic amplifier, it should be used over the upper section of its input range. Even so, it is difficult to obtain a -3 dB bandwidth past 100 kHz over three decades. Over five decades, the -3 dB point may well be only a few kilohertz. For large fluctuations of input signal the situation is even worse, and usually less predictable.

## CONCLUSION

Although logarithmic circuits are not the easiest to implement, a good quality logarithmic amplifier is not over difficult to make, provided care is taken in the setting up process. It is hoped that this article will have provided a useful introduction to the subject.

## ACKNOWLEDGEMENTS

Thanks are due to Mr W. Gibbons and Mr C. R. Francis, both of Sheffield University, for help given in the preparation of this article.



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THE TDA2020 monolithic operational amplifier is a front runner in the power game. It is intended for use as a low frequency class B power amplifier providing 20 W into $4 \Omega$ at I per cent total harmonic distortion with a $\pm 15 \mathrm{~V}$ supply. This is a guaranteed output. At lower power levels-less than 8 W -the distortion does not exceed 0.2 per cent and at most frequencies is about 0.1 per cent.
The absolute maximum voltage is $\pm 26 \mathrm{~V}$. Although higher voltages are likely to damage the i.c. it will operate quite correctly from supply voltages down to $\pm 5 \mathrm{~V}$.
The 14 pin (alternative quad or d.i.p. plastic packages aváilable), incorporates short circuit protection which automatically limits the output transistors to their safe operating area if, say, the output was short-circuited. Thermal overload protection is also incorporated which a.llows more economic heatsink


Fig. 2. A single channel 180 W hi fi audio amplifier
design as the risk of thermal runaway found in discrete amplifier designs does not exist. All of this makes the device virtually indestructible.


Fig. 1. The TDA2020 used in a basic 20 W configuration

Unlike most audio amplifiers the TDA2020 does not require a coupling capacitor from output pin to loudspeaker (see Fig. 1) which means a saving in money and space. The omission does make it necessary to maintain the quiescent output potential to prevent d.c. flowing through the speaker. This of course means balanced power supplies but the possibility of switch on "thump" is reduced.

A single 180 W channel using a $4 \Omega$ ? loudspeaker can be built around two TDA2020's. This type of circuit (Fig. 2) is known as a bridge or push-pull amplifier. As can be seen the component count is small for such a large output.

The i.c. package includes a copper insert which is normally clamped to an external heatsink to remove circuit power dissipation. A range of heatsinks appropriate to different voltages is available from Redpoint and assembly of these is facilitated by the spacer and screws supplied with each device so that heatsink and chip will securely mate to a p.c.b.

The TDA 2020 can be obtained from Technomatic Ltd., 54 Sandhurst Road, London, NW9, approximate price $\mathbf{£ 4 . 2 0}$.



Fig. 3. A 104 battery charger timer ( 20 minutes to 2 days). When start button is activated RLA energises and connects the battery to the charging supply and the timer to the battery, holding RLA through TR1. At the end of the timing period the circuit switches off

About four years ago Elremco launced their 14 pin LRI71E timer chip which took two years in gestation and $£ 100,000$ in develoment. Since then the price of the device has fallen by more than a third-currently $£ 7.50$.

Long duration electronic time delays using conventional CR methods require resistance of hundreds of megohms and capacitance of hundreds of microfarads To connect components together of this dimension presents all sorts of problems most of them being inherent so that accurate timing is virtually impossible. The LRI7IE cleverly overcomes this using simple digital techniques to provide time delays from 5 ms to over 3 months with a repetitive timing accuracy of $\pm 0.015$ per cent.
Even more astonishing, if a second LRI7IE is added in series the period can really be pushed out-in this configuration an external time constant of is $(10 \mathrm{k} \Omega / \mathrm{lnF})$ would produce a six month delay.

Basically the i.c. contains a timing oscillator to which external CR components are added to determine the timing period. A chain of 12 binary dividers follows which effectively multiplies the external CR time constant by a factor of 4095 .

A digital to analogue converter connected to the final six divider stages allows external meter monitoring of the elapsed time from the moment the timer is triggered. Outputs from the last three dividers in the chain provide facilities for specialised timing from $\frac{1}{\square} T$ to $\frac{7}{8} \mathrm{~T}$ in steps of $\frac{3}{8} T$ where $T$ is the preset time. If you combine this with the eight possible operational modes it can be seen that the device will suit almost all timing requirements.

With a suitable dropping resistor the device can work from a wide supply range since the on-chip voltage requirement is stabilised. Typical unloaded consumption is 5 mA .

Some suggested applications by Elremco for the motorist are

1. A lime delay can be set by the user within a $0-24 \mathrm{hr}$ range after which the parking lights automatically switch on.
2. The parking lights can be switched on and off in a $0-24 \mathrm{hr}$ period.
3. A set number of minutes after switching off the ignition the headlights are automatically switched off. This prevents parking with headlights left on.
4. The car radio can be made to switch on after a preset time delay acting as an alarm clock or to synchronise with a favourite programme.
5. Providing control for a combined windscreen wiper/washer.
In the home it can be arranged to switch off any manual over-ride facility for domestic central heating.

Central heating and night storage systems are normally controlled by a programme time switch which the user presets. When heating or hot water is required outside the programme times the manual over-ride is used but usually left on with consequent fuel wastage.

The LRI7IE can be time adjusted for this to switch the system back to automatic. Switching on a morning kettle or radio alarm are other applications.

The approximate price of the LR171E is $\mathbf{£ 7 5 0}$. For more information refer to Elremco Ltd., P.O. Box 10, Bush Fair, Harlow, Essex.


Fig. 4. Battery operated alarm timer from 2 seconds to 5 minutes duration


## MM57100-LM1889-MM53104-AY-3-8550-AY-3-8600-AY-3-8700

AFEw years ago the TV games market did not exist-today it is a multimillion pound industry and growing all the time.
Recently we published a design featuring the GIM AY-3-8500 games chip. It offered three basic games; tennis, soccer and squash. Additional discrete circuitry was required-a clock generator and a u.h.f modulator for interfacing to a monochrome receiver.
A more elegant games circuit available is the National MM57100 i.c. This offers bockey, tennis and handball in colour plus a lot more unpredictable play as a ball reflection from a bat can appear at eight possible angles. Complete game assembly is eased with the LM1889 video modulator i.c. and MM53104 clock generator i.c.

Of course, the LM1889 is a very useful chip in its own right since it can be used for relaying information from video tape recorders, closed circuit t.v. cameras or test equipment for display on monochrome or colour receivers.

A variant of the AY-3-8500 is the AY-3-8550 which provides the same basic games but the players' bats can be moved both vertically and horizontally requiring a lot more skill. The AY-3-8600 improves on the basic four games with basketball, hockey and gridball and increases in sophistication.

A spin-off from the popular microprocessor unit-based "tank battle" videogame commonly seen in amusement arcades is the GIM AY-3-8700.

This offers a two player "tank battle" where each player has a completely steerable tank with forward and reverse speed controls and a firing button. The screen "battlefield" includes anti-tank barricades and exploding mines to retard each tank's progress. The object of the game is to score as many hits as possible on your opponent's tank. The first player with 31 hits ends the game. Shell firing, explosion and tank sounds all add to the excitement.

All the above mentioned devices are available from A. Marshall (London) Ltd., 40-42 Cricklewood Broadway, NW2 3ET.

The MM57100 and MM53104 are available as Kit No. SK1122 for $\mathbf{£ 1 7} 18$.

|N THE consumer area probably one of the most exciting chips to appear is the digital or analogue delay line otherwise known as a "bucket-brigade" device (b.b.d.).

Some of the effects that can be achieved with these are the generation of chorus-where single instruments or voices are made to multiply which has become a popular sound usually associated with the string synthesiser; "Flanging" or "phasing", another effect similar to chorus but in performance equivalent to the sound produced when using a variable comb-filter; Vibrato which is defined as a $5-10 \mathrm{~Hz}$ cyclic pitch variation used generally to add richness to a sound produced and finally the synthesis of reverberation which is probably the most obvious application.

Of the devices around the two most readily available are the Mullard TDA1022 a PMOS circuit and the nmos Reticon SAD1024. Both are in 16 pin d.i.l. packages.


## SADIO24/TDA1022-DELAY LINES

Simply explained a "bucket brigade" delay consists of 512 capacitors separated by f.e.t.s. A sample of the incoming audio waveform is stored in the first capacitor end to the command of a clock pulse, the sample moves down the capacitor chain. to emerge 512 clock pulses later as delayed audio. For fidelity the number of samples per second clocked should be twice the band width of the incoming signal.
The successive samples can be likened to buckets of charge moving down the capacitor chain hence the analogy with the old fire-fighting "bucket brigade" line. The original signal is normally retrieved by passing the output through a low pass filter to remove the clock frequency.
The sampling frequency is very much related to the reverberation time of the bucket brigade the delay for N "buckets" being N 2 f seconds, where f is the clock frequency in hertz.


Fig. 5. Achieving a vibrato effect with a bucket brigade device (b.b.d.)

Reverberation is the echo effect produced by a sound after it has ceased and accounts for the richness in "live" performance. By using b.b.d.s in parallel or serial form it is possible to add artificial reverberation to existing music systems and so enhance the sounds produced.

A typical set-up for vibrato with a b.b.d. is shown in Fig. 5. By changing the clock rate in a slow cyclical manner $(5-10 \mathrm{~Hz})$ the delay through the device and hence the pitch varies in manner analogous to the Doppler effect when
the clock frequency is high, delay time is low and vice versa.

For chorus or multiple voice effects a typical block arrangement would be as shown in Fig. 6.

Chorus produced by delay alone is likely to sound lifeless because each reproduction is a replica of the previous signal. If the clock rates of the b.b.d.s are varied slightly there is enough difference between the direct and delayed signal to make them appear to come from separate sources or "chorus" together. There are obviously lots of variations to this-the clock oscillators could be modulated in antiphase or run irregularly, say, from noise passed through a narrow band filter or another b.b.d. could be added

A "flanger" or "phaser" can be created by combining an input signal with a slightly delayed version of itself as shown in Fig. 7. Obviously the magnitude of the effect is controlled by the ratio of delayed to undelayed signal (Balance Adjust) and the amount of delay which can be varied with control of the clock frequency. These are only some of the exciting possibilities of the b.b.d. but it obviously is a device we are going to see a lot more of in the future.

The SAD1024 is available for approximately $\mathbf{£ 1 8}$ from Herbert Sigma Ltd, Spring Road, Letchworth, Herts.


Fig. 6. A block diagram for setting up chorus effects


Fig. 7. Block diagram for phasing effects


THE National LM1830 is a 14 pin monolithic bipolar i.c. for use in liquid detection systems. Application areas include sump pumps, aquaria, radiators, boilers, etc. in fact anywhere where high or low fluid levels need to be detected.
The basic circuit of the chip is shown in Fig. 8. To complete the oscillator circuit a capacitor is connected across pins 1 and 7. The frequency of oscillation is inversely proportional to this capacitor value. Pin 13 is normally connected to the probe via a capacitor so that there is no chance of probe plating.
The oscillator output amplitude is approximately $4_{\text {be }}$ so that the emitterbase junction detector will be switched on when the probe resistance to ground is equal to the $13 \mathrm{k} \Omega$ resistor.


Fig. 8. Schematic of the LM1830 fluid detector i.c.

The diode at the detector transistor base symmetrically limits the input signal so that the probe is excited with $\pm 2 \mathrm{~V}_{\text {he }}$ from a $13 \mathrm{k} \Omega$ source. If the $13 \mathrm{k} \Omega$ source is incompatible with the probe resistance range a variable resistor, say $0-100 \mathrm{k}$ ! could be connected from pin 5 to the probe coupling capacitor.
Fig. 9 shows an application where an audio warning is given when a conductive liquid falls below a certain level, for example, the water level in a car radiator. When the liquid falls below the probe tip the resistance will rise between probe and radiator causing the output transistor to conduct the oscillator tone to the loudspeaker. An l.e.d. could equally be used in this position.

In such car applications the internal regulator on the LM1830 provides protection against supply transients.
An example of the device being used for sump pump drive or drain valve opening when a liquid is high is shown in Fig. 10. Here the relay or solenoid drive is arranged to be switched off when


Fig. 9. Low liquid level alarm using the LM1830
the liquid level is below the probe. With the probe tip immersed it switches on. The filter capacitor ensures on-off switching.

Although the LM1830 is designed primarily for use in sensing conductive


Fig. 10. High liquid level alarm suitable for opening a drain valve
fluids, a phototransistor, 1.d.r. or thermistor could readily be substituted for the probe path.

The LM1830 is available from $A$. Marshall (London) Ltd (see below), approximate price £1.72.

## LM3911-TEMPERATURE CONTROLLER

WHEN making up a thermistor thermometer bridge the greatest single problem is maintaining any sort of linearity in the meter scaling. This arises because of the instrinsic nonlinearity of this transducer.

If a silicon junction diode is used as a sensor this usually requires amplification as the sensitivity is only around 2.5 to 3.5 mV per degree Centigrade but there is an improvement in linearity. The usual circuit configurations are either amplification across a bridge configuration with the diode in one arm, or simply an op amp differentiating between a fixed set voltage at one input and the temperature variable diode voltage.

All of these problems have been neatly overcome in the National LM3911. Fabricated on a single monolithic chip it includes a temperature sensor, a stable voltage reference and an optional amplifier which can be used for both temperature measurement and control over a range of $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$.

The output voltage is directly proportional to temperature at 10 mV per degree Centigrade with tracking linearity of 0.5 per cent. By using the internal op amp with external resistors any temperature scale factor is easily obtained.

By operating the device as a comparator the output will switch as the temperature traverses any set-point making the device useful as an on-off temperature controller. Lamps or a relay can be driveri from the op amp


Fig. 11. Block diagram of the LM3911
output as this can be returned to a 35 V rail.
The LM3911 itself has a 6.8 V Zener reference for its sensing system. This allows the use of any power supply voltage with suitable external dropping resistor.
Block layout of the device is shown in Fig. 11 with an example of a basic


Fig. 12. Circuit of a temperature controller
temperature controller in Fig. 12 and a centrigrade thermometer in Fig. 13. The unity gain comparator allows for zero setting of an attached meter.

The LM3911 can be obtained from $A$. Marshall (London) Ltd, 40-42 Cricklewood Broadway, NW2 3ET, approximate price $\mathbf{f l}^{103}$.


Fig. 13. A centigrade thermometer using the LM3911



Fig. 14. Block diagram showing front end of an electronic piano

THE modern electronic piano has all the features and more of the conventional strung instrument. It has a sustain and soft pedal, usually a choice of additional voices such as honky-tonk piano or harpischord, but most important of all special circuitry that ensures the loudness and tonal quality of a note sounded is proportional to the velocity of the keys as in a conventional instrument.

A strung piano also produces complex harmonic resonances which means that for successful electronic synthesis the sound produced needs to die away at a realistic rate.

To achieve this special envelope shape it has required in the past a great deal of discrete circuitry. Because of the component intensity in this area and obvious advantage of reducing assembly cost and increasing instrument reliability with an appropriate integrated circuit substitute, GIM have developed the AY-1-1320 piano envelope or keyer circuit.

This 40 pin d.i.l. package reduces the hard work of electronic piano assembly to keyboard contact wiring and discrete voicing circuitry.

A typical electronic piano block arrangement is shown in Fig. 14. Here because of harmonic variations over the conventional instrument keyboard the voicing filters are divided giving more high harmonic at the low frequency end, and lower harmonic content for the top octaves.
The twelve note top octave generator directly feeds the top keyer and twelve five stage i.c. dividers to give 60 frequencies to the keyers which is the
keyboard range plus one top note to complete the compass of a normal 61 note keyboard.

One chip keyer circuit is shown in Fig. 15. When the key is up Cl is charged to -12 V . When the key is depressed Cl is first disconnected and starts to discharge through the $390 \mathrm{k}!$ with a time constant of 18 ms . When the key is grounded the Cl 's voltage has been transferred to C2 via the gates TR2 and TR3. The faster the key velocity the larger the initial voltage on C2 and the louder the note.
The d.c. voltage on C 2 is chopped via R1 and the output from a divider to give the decaying chopped waveform shown which is fed to the voicing circuit.

When the key is released the $50 \mathrm{k}!$ ! damping resistor is optionally connected across C2 to damp the notes with a 110 ms time constant. Different values of RI are used for each octave to give variation in decay time across the compass.
A negative pedal voltage applied to the sustain input dampens the output with a time constant of 180 ms when the key is released. This input simulates the action of the loudpedal in a piano.
The AY-1-0212 ( $\mathbf{( 6 . 5 0 )}$ ) and the AY-15050 ( $\mathbf{~} 2 \cdot 50$ ) is available from Technomatic Ltd, 54 Sandhurst Road, London, NW9.

A complete i.c. kit based on Fig. 14 is available from Semiconductor Specialists (UK) Ltd, Fairfield Road, Yiewsley, Middlesex, price $\mathbf{£ 3 6} \mathbf{2 5}$.


Fig. 15. The basic piano keying circuit

## AY-1-0212-AY-5-1317A-TBA 0470-D-ORGAN CIRCUITS-M147-AY-5050/1-AY-1-6721/5/6

## Top Octave Generator

The hearts of any electronic organ are the main oscillators from which all the distinctive voices derive. Years ago in the free phase system a separate oscillator was used for each note which represented an awful problem in tuning. Today, in what is known as the divider organ system, a digital tone generator produces from a single input frequency a full octave of twelve frequencies which with subsequent division can provide all the frequencies required by an electronic music synthesiser such as an organ or piano.
A good example of an i.c. top octave generator is the General Instrument Microelectronics 16 pin AY-1-0212. It is made up of twelve divider circuits which divide a typical input frequency of about 2 MHz into twelve notes. If any one of the adjacent figures of division in Fig. 16 are divided they will be seen to approximate to ${ }^{12} \sqrt{2}$ so that the whole makes up a well tempered chromatic octave.

## Frequency Dividers

Another component intensive area which has surrendered to integration is the subsequent dividers to the Top Octave Generator which in combination with the latter give all the required instrument notes. GIM provide a whole range of $4-5-6$ or 7 stage frequency divider in 14. 10 or 12 lead packages which have the same specification and are wholly compatible with each other to fulfil any arrangement of division. All circuits can be driven from a sine or square wave from, say, the AY-1-0212.
Choice of configurations are: AY-1-5050-7 stage frequency divider $3+2+1+1: \quad$ AY-1-5051-4 stage frequency divider $2+1+1$; AY-1-6721/55 stage frequency divider $3+2$; AY-1-6721/6-6 stage frequency divider $3+2+1$

## Distribution

In an organ there can be several contacts under a key which when closed simultaneously route the various signals to the busbars, from the dividers, and then onto the voicing filters. The trouble is key contacts corrode and are therefore electrically unreliable, producing as they do, all sorts of nasty noises over the years. The current trend in electronic organs is to replace these contacts with electronic gates so that pressing a key and a single contact, octave related notes from a divider can be passed onto a selected voicing filter.

On this simple idea TTT came up with the TBA $0470-\mathrm{D}$ organ gate which makes


Fig. 16. Block schematic of top octave generator AY-1-0212
it possible to reduce a ten contact key assembly to one per key. The circuit simply consists of ten transistors, each transistor is a gate which is d.c. switched with the input signal information via each emitter.

## Priority Latching

One bit of electronics which makes organ playing a lot easier is priority latching. This is a LSI subsystem which can be applied to pedals or keyboard but is probably more appropriate to pedals. The M147 from SGS-ATES is an example of a latch pedal sustain i.c. This has 24 pins with 13 pins for input stub pedais. When a pedal is depressed the corresponding square wave frequency spread over five octaves is immediately present at five pins. These outputs remain when the pedal is released until a new pedal is depressed. When two or more pedals are depressed only the left
one is accepted-corresponding to the lower frequency. This priority pedal produces a trigger percussion pulse when depressed and a sustain trigger with which the output sounds can be tailored.

## Chord Generator

Some would say the most magical innovative thing about organs is the chord generator; as besides generating static chords the chip can be multiplexed internally to provide a walking bass, rhythn arpeggio or alternating bass.
A block diagram of the GIM 40 pin AY-5-1317A is shown in Fig 17. Here the bottom twelve notes of the divided top octave generator are fed to the chord multiplexer.

All the above devices are available from Technomatic Ltd, 54 Sandhurst Road, London, NW9.


Fig. 17. Block diagram of the AY-5-1317A chord generator


LAST month we looked at the operation of the main system components used on the CHAMP board, including the 4040 MPU chip itself, and we are now about ready to look at the operation of the circuit in more detail. Before we start to discuss the hardware at the "gates and wire" level though, a word about the system operation as defined by the CHOMP software would be helpful.

## SYSTEM OPERATION

When considering CHAMP as a development system, i.e. with the CHOMP program running, there are a number of specific tasks to be performed which can be listed as follows:-
(a) Refresh 8 -character 7 -segment l.e.d. display at a rate which eliminates flicker.
(b) Accept and store hexadecimal keyboard entries of up to three characters.
(c) Scan the control panel to detect any of the following switch closures:-
enter data, enter address, dump, run-mode, test.
(d) In response to ENTER DATA, take data from temporary keyboard storage and load into the ram location pointed to by the "current address pointer" register, then increment the pointer.
(e) In response to ENTER ADDRESS, take data from temporary keyboard storage and load it into the "current address pointer" register.
(f) In response to $D U M P$, read data in the program location pointed to by the "current address pointer" register and load it into the display buffer, then increment the pointer.
(g) In response to RUN MODE, leave the CHOMP program by jumping to the start of a user program in the first program ram location (Address 200 Hex ).
(h) In response to TEST, leave the CHOMP program by jumping to the start of a program in the second PROM chip (Address 100 Hex ). This would normally be the PROMPT programmer firmware if fitted.
The important thing to remember about the operations listed above is that they are controlled by software, or to be more correct, firmware and are not purely hardware operations like RESET, RUN/STOP, or SINGLE STEP.

This means that although I shall be discussing the circuitry as it relates to these operations, you should bear in mind that you can use the circuitry for other purposes, providing you produce the software to do it.

This means, for example, that when you switch to RUN, your program can redefine ENTER DATA as "change points", ENTER ADDRESS as "sound horn", and $D U M P$ as "pull the flush", without you having to change a single wire!

## CIRCUIT DETAIL

Referring to Fig. 2.3 (last month), let's start with IC1, the 4201 clock generator. This device is fully described starting on page 5-77 of the users manual, but in outline it is a cMOS chip in a 16 -pin package which contains the oscillator and dividers necessary to produce the 4040 twophase clock signals and the logic for the SINGLE STEP and RESET operations.

The important point about this chip is that it provides high current clock outputs capable of driving the phase 1 and phase 2 inputs of a complete 4040 system, and this leads to a requirement for special decoupling circuitry.


Fig. 3.1. The CHAMP control panel connections

R 1 , and $\mathrm{C} 1, \mathrm{C} 2$ isolate the drive current pulses from the supply line and R2, R3 help to reduce the rise time of the clock waveforms when a complete set of 4040 system components is not used, as is the case with CHAMP. The insertion of R1 produces a separate $4201 \mathrm{~V}_{\mathrm{DD}}$ node and since the reset switch and the single step switch require a $\mathrm{V}_{\mathrm{DD}}$ connection, it is to this node that they must be connected.

Pin 5 on the 4201 is a mode control pin which changes the division ratio of the internal counter to slow down the resultant clock output. Since there are tangible advantages in sticking to a 10.8 microsecond clock cycle this pin is permanently connected to +5 volts in CHAMP. Pins 2 and 16 are clock outputs at TTL rather than mos levels, and are unused in the CHAMP system, R5 and C3 provide the "power-on-reset" time constant and can be altered as necessary to set an appropriate delay which ensures that the complete system is reliably "cleared" whenever power is first applied.

## 4040 CHIP

The mpu chip, the centre of the CHAMP system, is of course IC2. Note that pins 1, 2, 3, and 4 carry the fourbit multiplexed bus which is the key to 4040 operation and which of course was covered in detail in Part 2 last month. This bus provides communication with the 4002 data rams, the 4265 I/O chip, the 4289 program memory interface chip, and can also be accessed via the sockets for system expansion when required. Note the SYNC output, pin 16, and its interconnection to the other system components, and also the STOP input, the STOP ACKNOWLEDGE output, and the RESET input which link to the 4201 clock generator. TEST, pin 13, is an input which can be tested directly with software (e.g. "JUMP IF TESTS EQUALS LOGIC ONE") and is a unique 4004/4040 feature.

The COMMAND RAM lines, pins $17,18,19$ and 20 can each control a data ram bank which in turn may consist of four 4002 s , or three 4002 s and one 4265 . Ondy $\mathrm{CM}_{\mathrm{o}}$ is used on the CHAMP board, but CHAMP PROG uses banks 1 and 2 for the two extra 4265 s. These lines are activated using the $D C L$ instruction and are used to increase the address range over that possible with only
an 8 -bit $S R C$ operation. The 4040 also has two COMMAND ROM lines so that cwo separate rom banks can be used to allow a total of 8 K of program if needed. In CHAMP only CM ROM ${ }_{0}$ is used to control a single 4289 , and it is considered unlikely that CM ROM $_{1}$ would ever be used in a CHAMP derived system.

## NEGATIVE LOGIC

When first introduced the 4004 and 4040 were defined with respect to a negative logic convention, because this is more "natural" in a PMOS system where a transistor turned "on" produces a positive output level and a transistor turned "off" allows its output to be pulled down to a negative level. Inside a 4040 system this convention still holds, so that for example, a logic 1 on the DATA BUS is actually represented by a negative level, but on the inputs and outputs from the 4265 the more familiar positive logic convention is employed.

This means that a logic inversion takes place inside the 4265 , so that if for example your program writes binary 1111 ( F in Hex) to 4265 port Z you can expect to see four tTL-compatible positive logic levels on the output pins even though they passed over the bus as negative levels. The 4289 Prom address and data, and the I/O and CS pins are also defined in positive logic to make life easier, and so usually you don't have to worry about which convention applies for interfacing operations, you can assume good old TTL-type positive logic.

The main exception as far as external interfacing is concerned is the 4002 ram output port which is defined in negative logic, although this port is really only a secondary facility anyway, and only becomes available when a second 4002 is added to the system. It is of course always advisable to check in the MCS-40 User's Manual what the logic convention is on individual pins like INT or INT ACK before connecting these to external circuitry.

## CONTROL PANEL INTERFACE

In Fig. 3.1 we show the interconnection of the CHAMP control panel switches, which of course are mounted on the plinth and hooked up to the CHAMP main board
via a 16 -way flat strip cable. The reset, run/Stop and SINGLE STEP switches connect directly to the 4201 chip IC1, but the other four switches are wired into the system via the rom i/o lines and some til conditioning circuitry which forms, collectively, a special kind of four-bit input port.

The enter data, enter address and dump push switches directly control the PRESET and CLEAR inputs of 7474 D-type flip-flops (IC11-IC13) which are used as latches to "debounce" the switch operations and provide a clean positive-going edge for each press. The outputs from these latches are used to "clock" further D-type flip flops which have logic 1s hard-wired to their $D$ inputs, and the $\bar{Q}$ outputs of these pass via a 74125 tri-state buffer, IC14 to the 4289 I/o bus. This second set of three latches can be cleared via a $W R R$ instruction since they are controlled by what is, in effect, a rom output port (part of IC24 and IC25).

Suppose the enter data switch is pressed, this sets the $Q$ output of its associated latch to a 1 and this in turn clocks a 1 into the second flip-flop whose $\overline{\mathrm{Q}}$ output is then available at the input to the 74125. This sequence of events in itself initiates no further action, since the 4040 will not realise that anything has happened until it carries out an $R D R$ instruction which strobes the 74125 and allows all four switch data bits to be transferred via the 4289 and the data bus to the accumulator.

## WAIT LOOP

There won't be long to wait of course, and normally the 4040 sits in a "wait loop" which is embodied in the CHOMP software, continuously carrying out a read and check operation on these very control switches. When the enter data closure is recognised the 4040 jumps to a part of CHOMP which deals with the entry of data, and one of the first things this section of the program does is to clear all the switch flip-flops via the 4289 and part of IC24 and IC25. This is necessary to prevent multiple recognitions of the same switch closure, and points to the reason for the second D-type, since with this arrangement no matter how long you keep the switch pressed it can only be recognised once.

Note that the prog mode/run mode switch is not provided with TTL latch conditioning circuitry since it is a toggle switch and is not used repetitively like the others; its contacts are connected directly to the 74125 . We have termed the switch conditioning circuitry, just described, the switch FLAGS and in future we will use this shorthand name, and refer to the 74125 as the flag port.

## KEYBOARD INTERFACE

The on-board keyboard interface, comprising IC7-IC10, interposed is between the 4265 ports and the keyboard sockets SK3, and also between the 4040 interrupt lines and SK3. The 4265 is connected to this interface circuitry via a 16-way flat strip jumper which connects SK7 to SK8 when the keyboard is in use. As mentioned in Part 1, this jumper can be removed for direct access to the 4265 when "custom" interfacing is required for user programs.

The keyboard produces a ready encoded hexadecimal output on four lines together with a common strobe, and the display section requires eight-segment anode drives (a-g \& d.p.) and a clock and data input to the internal digit-strobe shift register (see Fig. 3.2). The internal circuitry of the keyboard will be covered in detail later on.


The four hexadecimal keyboard outputs connect directly to the 4265 port $W$ which is defined as a mode 9 input port during 4265 initialisation under CHOMP, but the common strobe is fed to the 74123 dual monostable to produce a de-bounced strobe which sets the interrupt latch (half of IC9) aid is also used to enter the hex code into the part $W$ input latches via the port Z 1 asychronous strobe line (See MCS-40 User's Manual, pages 5-36 for further details.)

## DISPLAY REFRESH

The display refresh drive is achieved by loading the next eight segment bits into output ports X and Y and then clocking the shift-register produced digit strobe along to the next common-cathode digit line. This operation has to be repeated eight times for the complete eightcharacter display, and has to be carried out rapidly enough to prevent display "flicker". The digit strobe is in effect a logic 1 shifting through a field of 0 s , a new logic 1 being presented to the shift-register via 4265 output line Z3 under software control at the start of a new display sequence.

The shift-register clock pulses are provided by output Z2 which is a synchronous strobe produced when port Y is loaded with segment data during a WR2 instruction. IC7 and IC8 are special l.e.d. anode driver arrays (75491) which provide the high-current segment drive needed by the multiplexed display, the cathode drives (75492) are contained within the keyboard case and are of course driven by the shift-register outputs. R51-R 58 perform the usual l.e.d. current-limiting function and therefore control the display brightness.

## PROGRAM RAM

The original 4004 microprocessor expected its program in a rom and its data in a ram and never the twain shall meet, but CHAMP is a development system. which requires programs to be easily modified and kept in RAM and so


Fig. 3.2. The CHAMP board/keyboard interface
some special arrangements have to be made to provide this facility. Fortunately the 4040 does have instructions for writing to and reading from ram program memory, namely $W P M$ and $R P M$ respectively, but since the 4040 deals with four-bit nibbles while its program comes in 8 -bit bytes, some jiggery-pokery is still required to allow painless operation of the ENTER DATA and DUMP commands which of course are used to modify and examine program ram when required.

When a program in ram is actually running the program ram is addressed via the 4289 just as if it were prom, and eight-bit instructions are fetched from ram via the 4289 without the MPU ever knowing the difference. The need for "special treatment" arises when the so-called transitive read or write operations using the $R P M$ and $W P M$ instructions are undertaken because of the nibble/byte conflict.

To achieve proper operation of the transitive instructions the 4289 contains a FIRST/LAST flip-flop which is toggled by each use of $W P M$ or $R P M$. The output of this flip-flop is used externally to steer a nibble to either the FIRST half-byte or the LAST half-byte of a program RAM location during transitive write operations, or used internally to send the FIRST half-byte or LA'ST half-byte of program ram data back to 4040 over the data bus during transitive read operations. To accommodate this mode of operation CHAMP program ram is organised so that it may be read as a byte-orientated array of $512 \times 8$ bits but loaded as a nibble-orientated array of $1024 \times 4$ bits.

The program ram write operation is achieved using the 4289 I/o bus to transfer the data a nibble at a time, the correct half-byte of ram being selected using a logical combination of the 4289 outputs $\mathrm{F} / \mathrm{L}, \mathrm{PM}$, and OUT to produce individual write strobes for each of the two $256 \times$

4 ram chips which together form the equivalent of a single 4702A Prom chip. This gating logic is performed by the remaining parts of IC24 and IC25.

## ADDRESSING PROGRAM MEMORY

As mentioned last month, the 4289 is used to demultiplex the 4040 bus to produce a 12 -bit wide address output to program memory. The lower 8 bits of this address are wired directly to each program memory device via what we shall call the 4289 address bus (pins 23 to 30 from 4289). The upper four bits are decoded by a 3205 TTL decoder to produce a unique CHIP SELECT strobe for each of the two 4702A PROM chips and each of the two pairs of 5101 ram chips so that only one "memory chip" (one 4702A or two 5101s) can be enabled at one time.

The 12 -bit address is provided by the 4040 program counter during normal operations, but when a transitive read or write is carried out the eight low order address bits must be provided by an $S R C$ operation, and the four chip-select bits must be provided via an output port. In CHAMP the port employed for this purpose is the 4002 output port from IC4, buffered by a 74L00 gate IC3, which also provides the necessary logic level inversion.

We now have two possible sources for the four chipselect bits, either pins 31 to 34 of the 4289 (normal operation) or pins 13 to 16 of the 4002 (transitive operation) and so the 74157 quad two-line to one-line data selector (IC16) is interposed between the two sources and the 3205 decoder. The 74157 SELECT input is controlled by the 4289 PM output which is active only during transitive operations, so that proper selection of the source of chipselect data is maintained.


Fig. 3.3. Simplified schematic diagram of addressing CHAMP RAM program memory

To carry out a transitive write then, as required by an ENTER DATA command, the following sequence is necessary.

1. Select 4002 port
2. Write chip code to 4002 port
3. $S R C$ to select location within chip
4. $W P M$ to write first half-byte
5. WPM to write second half-byte.

A similar procedure is necessary to achieve a transitive read, as required by the $D U M P$ command. Further details of the intricacies of addressing program memory can be gained from the 4289 data sheet, although of course to use CHAMP as a development system it is not essential to be familiar with these. See Fig. 3.3 for simplified circuit operation.

## BATTERY BACK-UP

The 5101 program ram chips are cmos devices which have extremely low standby current drain. Components B1, D19, D20 and R40 form a battery supply circuit which will power the 5101s with the CHAMP main supplies turned off. B1 is a three-cell DEAC nickel cadmium battery which provides about 4 volts and is recharged via D20 and R40 when the power is on. When power is removed D20 becomes reverse biased, isolating the 5101s from the +5 V line, and D19 becomes forward biased to supply the memory standby current. Note that a dry cell battery of 4.5 volts could be used instead of the DEAC
if $\mathbf{R} 40$ is left out, although you could end up losing data when the battery eventually runs flat. It is difficult to say just how long this would take.

## POWER FAIL DETECT

To ensure that the memory is not corrupted by write transients during power failure or recovery, it is necessary to raise the $\mathrm{CE}_{2}$ input to the 5101 s only when the main 5 volt supply is available, and to achieve this control a "power-fail-detection" circuit formed by D13, R32, R33, TR1, R34 and part of IC10 is provided. The transistor is held on by the conduction of D13 until the 5 volt line starts to drop. When it drops below about 4.5 volts D13 and TR1 turn off and $\mathrm{CE}_{2}$ is grounded via the 74L00 gate.

## USING OTHER MEMORIES

If you can do without the non-volatile feature made possible by the 5101 devices for all or part of your program ram, then you can leave out the battery circuit and the power fail detect circuit and plug in 2101 devices which are available at very low cost. The 2101s are completely compatible with the rest of the CHAMP circuit and have been tried on the prototype.

One final note, the 5101 cmos devices must not have their inputs taken negative more than a few hùndred millivolts, and this is the reason for clamp diodes D1 to D12. The use of good quality germanium devices in these locations is essential.
NEXT MONTH: CHAMP Keyboard, power supplies, construction

Copies of Patents can be obtained from : the Patent Office Sales, St. Mary Cray, Orpington, Kent Price 95p each

## 

A column or line source loudspeaker for use in a public address system which is capable of directing sound "off axis" in a chosen direction is covered by Paul Taylor, of Hertford, in BP 1456790.

Conventionally a column loudspeaker is constructed as a long box with a series of loudspeaker units arranged along its length and fed with equal, in-phase signals. Such a speaker column produces a narrow and symmetrical beam of sound which can only be directed at the intended audience by carefully mounting the column so as to point in their direction. This necessitates tilting a high column down at an awkward angle. The object of the invention is to produce a column which has an assymetrical sound characteristic and may thus beam sound down on an audience from a vertical position.
The column (Fig. 1) includes a line of loudspeaker units comprising end speakers, inner groups of equally spaced units and a central unit. The first phase reverser ensures that the input signal is fed in opposite phase to the units $A$

above and below the central unit $C$. Attenuators R1, R2, R3, R4, between the units $A$ ensure that the relative amplitudes of the sounds radiated from these units decreases progressively in each half of the column away from the centre unit. $A+90^{\circ}$ phase shift is introduced into the signal fed to the central unit and $-90^{\circ}$ phase shift is introduced into the end units $E$, to minimise residual side lobes in the upper quadrant.

The phase and amplitude discrepancies along the remainder of the line produce a sound output radiation pattern which is vertically lopsided, so that a considerable amount of sound power is directed downwards and reiatively little upwards. This enables the column to be installed vertically without tilt but still beam the majority of sound reproduced down at the audience rather than up and over their heads.

## HIUI : Allisile BP $145 \mathrm{~F}: 77$

There has recently been patenting activity in the field of liquid brushes for motors. In BP 1468 155, Eric Wilcox of the Isle of Man patented a slip ring formed from an alloy having 18.8 per cent tin, 50 per cent bismuth and $31 \cdot 2$ per cent lead. This alloy, which has a melting point of $95^{\circ} \mathrm{C}$, is kept liquid by a heater and is claimed not to react with a copper commutator.

In BP 1475 877, Siemens A.G. of Germany claim the use of a new type of liquid brush. The object is to cope with high current levels, up to $50 \mathrm{~A} / \mathrm{cm}^{2}$ and at all motor speeds, without loss of the liquid from the annular gap where
it is serving as a slip ring between the stationary and moving parts.

To-date gas pressure has been used to counteract the effect of skin-friction and centrifugal force. The proposed new answer is to use a ferro-magnetic liquid, for instance ferro-magnetic particles in a non-magnetic, metallic liquid. Sodiumpotassium, gallium, or gailium-indium are suggested as the liquid metal, with iron or iron alloys suitable as the particles.
A magnetic field is generated in the area of the annular gap, by the provision of carefully located windings additional to those which form an integral part of the motor or dynamo which the slip ring is serving. When the rotor is stationary the liquid is held in a stable position by a static field from the additional coils. As the rotor turns, fric-
tional forces entrain the liquid, so that it is continually interrupting the radially directed magnetic field. The frictional forces are directed axially inwards or outwards depending on the sense of rotation and upon the direction of the magnetic field.

The direction of the magnetic field produced by the additional coils is thus chosen so that the magnetic containing forces act in opposite directions inwards, towards the middle of the fluid. Provision is made to reverse the direction of the magnetic field, by reversing the current flow in the coils, when the direction of the rotor is reversed. It is also possible to increase the current to the coils as the speed of rotation increases, so that the magnetic containing field is always greater than the forces tending to disturb the liquid in the gap.


For remote control of mains and battery powered electrical equipment such as garage doors drive motor, porch light . . . also an intruder alarm

## V.H.F. PORTABLE RADIO

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INN the last issue, the timing circuits were described and an introduction was given to the operation of the scoring logic, where the " $P$ " flip flops were discussed. The description of the scoring logic is to be continued this month, commencing with the details of four flip flops that are used to produce the results for the number of coloured pegs correct for colour but incorrect for position, the "I" results.

## COMBINATIONS THAT CAN OCCUR

At this stage it is worthwhile considering the various combinations of entries and internal colours that may occur in a typical game, as it is the nature of this combination that determines the particular mode in which the scoring logic will operate. The combinations that may occur can be divided into four categories:
(a) The entries may be non-repeated and the internal colours may be non-repeated,
(b) the player may repeat the colours in a deduction,
(c) there may be repeated colours within the machine, and
(d) a combination of (b) and (c).

Each of these categories may be sub-divided to include the cases where there are only " I ", " P ", or " I " and " P " results occurring.

Fig. 4.1 is the overall functional diagram of the scoring logic, and this will be referred to extensively throughout the description of the operation.

## THE "II" FLIP FLOPS

Four flip flops, called the "I' flip flops, are used to produce the "I" results. These flip flops are clocked by signals $C_{1} \overline{\mathrm{C}}$ to $C_{4} \bar{C}$, for $I_{1}$ to $I_{4}$ respectively, so as to eliminate any adverse effects that may otherwise have been produced by time delays inherent in the comparator logic, had signals $C_{1}$ to $C_{4}$ been used instead. This point was discussed in detail last month.

[^3]With reference to Fig. 4.1 it will be seen that the E (Equality) signal (from IC15) is common to the "J" inputs of all "I" flip flops, so that if, for example, $C_{1} \bar{C}$ and $E$ are present simultaneously, $I_{1}$ will be set on the trailing edge of $\mathrm{C}_{1} \mathrm{C}$. The " $K$ " inputs to these flip flops are connected to logical zero, so that a flip flop may only be cleared by the application of logical zero to the clear input.

A simple example, in category (a), showing the collective action of the " $I$ " and " $P$ " flip flops, is illustrated in Table 4.1.

An example in category (b) is shown in the simplified diagram of Fig. 4.2(iii). Here the player has entered two blue pegs, the first of which will set $P_{1}$ and $I_{1}$; the second one will produce no further change. However, according to the rules of play,

Table 4.1

| ENTRIES | $\times$ CODES |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Red $\{$ | $\begin{aligned} & \text { Black } \\ & \mathrm{K}=1 \\ & \mathrm{C}_{1}=1 \\ & \mathrm{E}=0 \\ & \mathrm{P}_{1}=0 \end{aligned}$ | $\begin{aligned} & \text { Red } \\ & \mathrm{K}=1 \\ & \mathrm{C}_{2}=1 \\ & \mathrm{E}=1 \\ & \mathrm{I}_{2}=1 \end{aligned}$ | White $\begin{aligned} & K=1 \\ & C_{3}=1 \\ & E=0 \\ & I_{3}=0 \end{aligned}$ | Green $K=1$ $\mathrm{C}_{4}=1$ $\mathrm{E}=0$ $I_{i}=0$ |
| Black $\{$ | $\begin{aligned} & \mathrm{L}=1 \\ & \mathrm{C}_{1}=1 \\ & \mathrm{E}=1 \\ & \mathrm{I}_{1}=1 \end{aligned}$ | $\begin{aligned} & \mathrm{L}=1 \\ & \mathrm{C}_{2}=1 \\ & \mathrm{E}=0 \\ & \mathrm{P}_{2}=0 \end{aligned}$ | $\begin{aligned} & \mathrm{L}=1 \\ & \mathrm{C}_{3}=1 \\ & \mathrm{E}=0 \\ & \mathrm{I}_{3}=0 \end{aligned}$ | $\begin{aligned} \mathrm{L} & =1 \\ \mathrm{C}_{4} & =1 \\ \mathrm{E} & =0 \\ \mathrm{I}_{4} & =0 \end{aligned}$ |
| Blue $\{$ | $\begin{aligned} & M=1 \\ & C_{1}=1 \\ & E=0 \\ & I_{1}=1 \end{aligned}$ | $\begin{aligned} & M=1 \\ & C_{2}=1 \\ & E=0 \\ & \mathrm{I}_{2}=1 \end{aligned}$ | $\begin{aligned} & M=1 \\ & C_{3}=1 \\ & E=0 \\ & P_{3}=0 \end{aligned}$ | $\begin{aligned} & M=1 \\ & C_{4}=1 \\ & \mathrm{E}=0 \\ & \mathrm{I}_{4}=0 \end{aligned}$ |
| White $\{$ | $\begin{aligned} & N=1 \\ & C_{1}=1 \\ & E=0 \\ & I_{1}=1 \end{aligned}$ | $\begin{aligned} & \mathrm{N}=1 \\ & \mathrm{C}_{2}=1 \\ & \mathrm{E}=0 \\ & \mathrm{l}_{2}=1 \end{aligned}$ | $\begin{aligned} & N=1 \\ & C_{3}=1 \\ & E=1 \\ & I_{3}=1 \end{aligned}$ | $\begin{aligned} & \mathrm{N}=1 \\ & \mathrm{C}_{4}=1 \\ & \mathrm{E}=0 \\ & \mathrm{P}_{4}=0 \end{aligned}$ |

[^4]

Fig. 4.1. Overall functional diagram of the scoring logic
only $P_{1}$ must remain set. Correct operation is ensured by arranging that when a given " $P$ " flip flop sets it's corresponding "I' flip flop, $I_{1}$ in this case, is cleared and inhibited for the remainder of the deduction. A " P " correct entry is therefore a dominant one, as shown in Fig. 4.2(iv).

This dominance of a " $P$ " flip flop over its corresponding 'I'" flip flop can be seen in Fig. 4.1, since the complements of


Notice that comparisons that are "ignored" or "erased" are deleted in the above tables

Fig. 4.2. Examples showing collective action of "p" and "I' flip flops
the " $P$ " outputs are connected to the inputs of the NAND gates labelled "Level 1". If, therefore, $P_{1}$ has set, then $P_{1}=0$ acts to inhibit $I_{1}$ via the NOR gates of "Level 0 ".

A further example in category (b) is shown in Fig. 4.2(v), where there are repeated " $I$ " correct entries. The first blue entered sets $I_{1}$ and the subsequent blue entries are then ignored, since $I_{1}$ can only set once.

Category (b) has now been fully explored, but before proceeding to (c) it is firstly necessary to describe the hierarchy of gates serving to clear the "I" flip flops.

## RESET LEVELS

There are three levels, of four gates each, serving to generate the various resets required for correct operation of the scoring logic, see Fig. 4.1.
"Level 0 ", comprised of NOR gates, is an unconditional level, since a logical one applied to any gate input will clear the corresponding " I " flip flop. One input to each gate of this level is derived from "Level 1", whilst the other input is connected to the logic labelled "Reset Logic", to be described next month.
"Level 1" is likewise an unconditional level, since a logical zero applied to any input sends the gate's output high and clears an "I" flip flop via "Level 0 ". The four signals $\overline{\mathbf{P}}_{1}-\bar{P}_{4}$ are each taken to a gate in this level, performing the "clear and inhibit" function mentioned previously.

The clear line, $\overline{\mathrm{R}}_{\mathrm{L} 2}$, is also connected to these gates, so that since this signal is taken low whenever the scoring logic has to be cleared, all "I" flip flops are reset unconditionally to zero.

The third set of inputs to the gates of "Level 1" comes from "Level 2". This is a conditional reset level, since all inputs to a given gate must be high in order to clear an "I" flip flop via levels 1 and 0 .

## THE "S" FLIP FLOPS

Just how these reset levels function in the logic will be discussed later, but in order to proceed with the description of "Level 2" the four "slave" or " $S$ " flip flops must be introduced. Briefly, these flip flops serve to indicate which of the "I's have set in response to any particular entry made by the player. Examples Fig. 4.2(i) and (ii) illustrate why these additional flip flops are required. Note that these are both examples in category (c).

In 4.2(i) the first colour the player enters will set flip flops $P_{1}, I_{2}, I_{3}$ and also $S_{2}$ and $S_{3}$, the "slaves" corresponding to $I_{2}$ and $I_{3}$. The fact that both $S_{2}$ and $S_{3}$ are set indicates that two "I" flip flops have been set in response to a single entry.

Example (ii) illustrates why this information cannot always be gained from the "I" flip flops themselves, since they contain not only a record of the current entry but also of any previous entries.

In both of these examples a single entry is seen to set both an " $I$ " and a " $P$ " flip flop. However, one entry, by the rules of play, cannot be counted as being correct for colour and position and yet correct for colour and incorrect for position at the same time, albeit with two identical internal colours in different positions. Both examples therefore give an incorrect score. It is the main function of "Reset Level 2 " to overcome this problem.

Since a " P " correct entry is dominant it is necessary to clear any "I" flip flops that may also have been set by the entry. Therefore, in Fig. 4.2(i), both $I_{2}$ and $I_{3}$ must be cleared. To do this the PI signal is used, which, it may be remembered, produces a logical one output whenever a " $P$ " correct entry has been made (until such time as a subsequent entry is made).


Fig. 4.3. Scoring logic circuitry

This signal is used to enable "Reset Level 2" in order to gate the outputs of the " $S$ " flip flops to clear those "I" flip flops whose " S " flip flops have set. It will be seen from Fig. 4.1 that gates 3 and 4 of "Level 2 " have three and four inputs respectively. The additional inputs are inhibit inputs and will be described next month. For the moment they may be regarded as being held at logical one.

The operation of the system, with reference to Fig. 4.2(i), is now as given below.
(1) Enter first colour-Red.
$K($ from $I C 20)=1$.

$$
\begin{array}{ccc}
\mathrm{KC}_{0} & - & \text { All logic cleared. } \\
\mathrm{C}_{1} \overline{\mathrm{C}} & - & \mathrm{P}_{1} \text { set, } \mathrm{I}_{1} \text { and } \mathrm{S}_{1} \text { cleared and inhibited. } \\
\mathrm{PI}=1 .
\end{array}
$$

(2)-(4) No change. Only $P_{1}$ remains set, which is the correct score for this deduction.
Referring to the latter sequence of events, it is seen that when PI gates $\mathbf{S}_{2}$ to clear $\mathrm{I}_{2}, \mathrm{~S}_{2}$ is also cleared, and similarly for $S_{3}$ following $C_{3} \overline{\mathrm{C}}$. The precise reasons for this will be examined next month, but it is important to note that the reliability of these resets depends solely on the existence of a time delay around the reset loop. Hazard free operation can only, therefore, be assured if "on spec" gates are used. The clearing of the "S" flip flops as described may be seen in Fig. 4.1, since the outputs of "Level 1" are connected to "Level S", which serves to clear the " $S$ " flip flops.

The "S" flip flops must only provide a record of those "I"s set in response to a single entry, so they are cleared by $\mathrm{C}_{\mathrm{o}}$, connected to "Level S", at the start of each entry.

## CONSTRUCTION

The positions of this month's i.c.s are shown in Fig. 4.4. Construction is fairly straightforward, reference being made to the circuit diagram of Fig. 4.3 as well as to Fig. 4.4.


Fig. 4.4. Prototype component layout for "C" section of main board (see photo last month). For assembly details one should refer to the circuit diagram

A number of input connections cannot be completed until next month and it is therefore recommended that these be left completely unconnected for the moment.
The best order in which to complete the construction is as follows: IC $31-39,41 \mathrm{c}, 45 \mathrm{a}, 41$ and 42 respectively.

The outputs from the "I" flip flops are taken to the " I " adder, described last month. Connection details are given in Fig. 4.3.

Note that $\bar{E}$ and not E is taken to IC33, and also that $\overline{\mathrm{PI}}$, from IC30, is inverted by IC36b.

## "S" FLIP FLOP J INPUTS

Again due to the fact that these flip flops must only provide a record of those " 1 "'s set by the current entry, an " $S$ " flip flop must not set if its corresponding "I" flip flop has set in response to a previous entry. This is arranged by gating the $J_{\mathrm{s}}$ inputs such that $\mathrm{J}_{\mathrm{s}_{1}}=E \overline{\mathrm{I}}_{1}, \mathrm{~J}_{\mathrm{s}_{2}}=E \overline{\mathrm{I}}_{2}$, etc.

## COMPONENTS . . .

| Integrated Circuits |  |
| :---: | :---: |
| IC31-32 | SN7473N (2 off) |
| IC33-35 | 74402 (3 off) |
| IC36 | 7404 |
| IC37-38 | 7473 (2 off) |
| IC39 | 7400 |
| IC41-42 | 7410 (2 off) |
| IC45 | 7420 |

## Capacitors

C11-C13 $\quad 0 \cdot 1 \mu \mathrm{~F}$ (3 off) 10 V ceramic
C14 $3,500 \mu \mathrm{~F} 10 \mathrm{~V}$ electrolytic

This gating is performed by IC33 which is a 7402 quad two input NOR gate.

The circuit diagram is shown in Fig. 4.3. All flip flops are JK types SN 7473 N . The reset levels are implemented as follows:
${ }^{3}$ IC34+IC36a-Level 0
$\frac{1}{2}$ IC39 + IC4Ic + IC45a-Level 2
$\frac{2}{3}$ IC41 $+\frac{2}{3}$ IC42-Level 1
IC35-Level S.

## TESTING

Testing is somewhat complicated by the fact that a number of connections have not yet been made. For example, the " 1 " flip flops are always held "clear" owing to the floating inputs to IC34, awaiting connections from the "reset logic". However, provided that the constructor connects pins 9, 6 and 3 of IC34 temporarily to 0 V , then very worthwhile testing may be performed by simply playing the game and noting the scores (the "I'" flip flops are enabled by these temporary connections).

The randomly generated codes may firstly be monitored using a d.c. voltmeter. These codes are contained in i.c.s 3-6.

The " $P$ " results may be "read" from Veropins 16 -18 and the " 1 ". results from pins $13-15$ (see Fig. 3.5).

The scoring given by the machine should follow the rules of the game in all cases except where there are certain repeated codes within the machine, that is a combination in category (c) or (d). Remember that fault tracing can be enhanced by slowing down the internal clock, as described last month, should any problems be encountered.

NEXT MONTH: The final part of this series of articles will deal with the remainder of the scoring logic and the display circuits.


A selection of readers' original circuit ideas. It should be emphasised that these designs have not been proven by us. They will at any rate stimulate further thought.

Why not submit your idea? Any idea published will be awarded payment according to its merits.
Articles submitted for publication should conform to the usual practices of this journal, e.g. with regard to abbreviations and circuit symbols. Diagrams should be on separate sheets, not inserted in the text.

Each idea submitted must be accompanied by a declaration to the effect that it is the original work of the undersigned, and that it has not been accepted for publication elsewhere.


## WASH-WIPE CONTROLLER



## Fig. 1

Aclear windscreen is essential for safe driving. However, on some older cars, operating the windscreen washer and wipers simultaneously while still remaining in perfect control, is not easy.

The circuit in Fig. 1 is designed to wash the screen and then wipe it clear, having switched off the washer; all at the touch of a button. When S 1 is pushed, Cl charges up almost instantly, which holds TR1 on, and operates RLA. Consequently RLA1 charges up C2 and turns on TR2, thus energising RLB also. At this point both washer and wipers are working.

When Cl has lost enough charge through the base of TR1, RLA will drop
out, leaving C2 fully charged and RLB still energised. At this point, just the wipers are left operating. Eventually, when C2 has lost sufficient charge, RLB will drop out to switch off the wipers, and then the sequence is complete.
The values of C 1 and C 2 are a matter of choice, but with the values shown ( $250 \mu \mathrm{~F}$ ), the washer and wipers should run together for about five seconds, and then just the wipers for a further five seconds. The resistance of the relay coils will affect this timing relationship.

Any 12 volt relay should be suitable as long as the coil current does not exceed the rating of the transistors used. When
considering the contact ratings of the selected relay, remember that the stall (starting) current of the washer or wiper motor, may well be several times the running current.

A convenient position for the WashWipe Controller switch is on the steering column, similar to indicator or headlamp flasher switches. If the button is pressed before the cycle is complete, the sequence will begin again irrespective of how far the process has gone.
J. R. Ellis,

Hitchin,
Herts.

SIMPLE LOGIG PROBE


ALogIC probe is a vital instrument in the checking of digital equipment. The circuit of Fig. 1 shows a simple threefunction probe which can be built very economically.

A high logic level at the probe tip causes TRI to conduct, illuminating the 1.e.d. marked " 1 ". A low logic level produces a high at the output of the inverter G1, causing the l.e.d. marked " 0 " to be lit.

If, however, the logic level at the probe tip is being pulsed, either a 0 pulsing to 1 , or a 1 pulsing to 0 , the monostable ICl will detect the pulses and stretch them to about 0.4 s duration. The l.e.d. marked " $P$ " will then flash briefly.
The whole circuit was constructed on Veroboard and mounted in a small metal pill box, using three 1.5 V batteries to supply the power. The inverter Gl can be one section of any TTL package, such as a 7400,7402 or 7404 , which may be to hand, with inputs paralleled if appropriate.
A. C. Hay,

Bristol

Sequence generators find wide application as counters, and in the field of digital communications. One form of sequence generator is the feedback shift register, comprising a shift register with combinational logic feedback from its outputs to its input. This feedback determines the next logical state to be entered into the register.


The circuit diagram of Fig. 1 uses an SN7495 4-bit shift register, operating in the serial in, parallel out mode, and is suitable for use as the binary number generator for a digital die. As the shift register is clocked, its three outputs follow the 6 -state cyclic sequence shown in Fig. 2.

The SN7451 dual, 2 -wide, 2 -input And-or-Invert gate forms the combinational logic feedback network which processes the outputs $\mathbf{A}, \mathrm{B}$ and C to determine the next logical state for the register. This combinational logic performs the Boolean function:

$$
\mathrm{F}=\overline{\mathbf{A C}+\mathbf{B C}}
$$

Fig. 1

## SEQUENCE GENERATOR

A suitable clock source is shown in Fig. 3. This consists of a simple unijunction relaxation oscillator, plus a pulse amplifier to boost its output. Closing S1 activates the oscillator and thus creates the "roll" effect for the die. An important characteristic of this clock source is that when S1 is released, the effect of any contact bounce does not appear at the output of the clock source. Such contact bounce can cause the register to clock spuriously, leading to unwanted output combinations appearing, i.e. 000 or 111.
P. Hutchinson,
Brockenhurst,
Hants.


Fig. 2


# UNIVERSAL <br> P.A. PREAMPLIFIER 

Fig. 1


THE circuit of Fig. 1 was developed to provide improved dynamic range, distortion and signal-to-noise ratio on an otherwise conventional 741 -based, 16-channel mixer. It also incorporates a number of novel features which simplify the input switching requirements for the mixer.
This preamplifier will handle signal levels ranging from less than 1 mV , such as might come from a highquality microphone, up to several volts r.m.s., as can be produced by a high output guitar pick-up. The differential input provided by TR1 and TR2 operates over this range with low distortion, and allows a balanced input to be achieved without the expense and inconvenience of a microphone transformer.

The arrangement of the input connections eliminates the need for switching between balanced and unbalanced modes. A stereo jack is used, providing two signal connections for a balanced lead, connected by means of a stereo jack-plug. The signals are then fed via R1 and R2, giving a differential input impedance of about $90 \mathrm{k} \Omega$.

## Fig. 2

An unbalanced signal source would be connected via a mono jack-plug, whose sleeve will short R2 to earth, so that the amplifier functions as a non-inverting single-ended input stage, with an input impedance of about 45 kS .

For input impedances les than those quoted above, a loading resistor $R_{L}$ should be connected across the input ends of R1 and R2 so that the resultant paralleled value approximates to that requried (e.g. $\mathrm{R}_{\mathrm{L}}=680 \mathrm{2}$ for 60012 line). This resistor could be inserted by means of a front panel switch, but a simpler and more versatile solution is to wire an $\frac{1}{8} \mathrm{~W}$ resistor inside the actual jack-plug, as shown in Fig. 2. A robust screened jack-plug with solder terminals should be used, and colour-coded tape applied to the cable to show that it has been "preloaded" and now matches a standard high impedance input on virtually any amplifier.

The input stage feeds a high gain common-emitter voltage amplifier, TR3, with a bootstrapped collector load for increased efficiency. This is followed by an emitter-follower based on TR4, which provides a lowimpedance output for tight control of the feedback circuit, and is capable of driving channel fader or tone controls without detriment to the signal, which is closely balanced about earth.

Gain is variable between unity and $60(36 \mathrm{~dB})$, providing a minimum output of 50 mV r.m.s. for further amplification. Several such preamplifiers could be incorporated into a mixer or public address amplifier, with tone and volume controls and mixing-withgain based on i.c. op. amps. The balanced supplies could then be derived from the op. amp. supply, decoupled and Zener-stabilised as appropriate.
P. J. Willcox, London W11.

## TTL FREQUENCY DOUBLER

The circuit shown in Fig, 1 is a frequency doubler using TTL gates. It provides two complete output pulses for one complete input pulse.

On the positive-going edge of the input pulse, the output for ICla goes tow and this sudden change is passed through C2 to turn D1 hard on. This causes ICl pin 5 to go low and pin 6 to go high. If no further changes are made at the input, C 2 discharges and the output returns to the low condition. On the negative-going edge of the input pulse, D2 is turned on
via Cl , causing the output of Cl b to go high again, returning to low shontly after.
The two diodes are included to prevent execessive voltages being applied to the inputs of IClib. The values of Cl and C 2 depend upon the input frequency being used. The table gives a rough guide to the actual values required for four different frequency ranges.

The shape of the output pulse may be improved by using a Schmitt nand gate (such as the 7413) for IC1b.
P. J. Hambridge, Ilford.


Fig. 1


The circuit in Fig. 1 uses a seven segment l.e.d. display to show characters that indicate a car system fault, such as low hydraulic fluid or coolant, and are accompanied by an audible tone. Altogether, these eight characters and their meanings are shown in table 1.

When any one of the sensor outputs falls to logical 0 (when a fault occurs) the output of the 7430 eight

## CAR SYSTEM MONITOR

input gate, goes high. This enables a simple three gate oscillator, and TR1 drives the loudspeaker. The 7430 output also enables the seven segment display drivers (7401s). The original sensor output pulls its associated driver gate (7407) output to ground. This output pulls down the 7401 driver inputs via the diode matrix. When the drivers are enabled, the output is at ground level, therefore switching on that segment connected to it, the DL707 being a common anode display

Sensor circuits of the type used with the display are shown in Figs. 2 to 5. Fig. 2 shows a spark plug monitor. This has a discrete l.e.d. which will glow when that plug is firing. The coil picks up impulses which are fed via an amplifier to a monostable which fires for about 0.7 second. This charges up a capacitor and produces a logical 1 at the Schmitt gate input. Missing pulses will allow the capacitor to discharge, changing the state of the Schmitt trigger, and causing a final display of " S ". One circuit can be used for each plug, each feeding into the SN7413.

Fig. 3 shows an oil pressure monitor. When the input falls to zero volts, the first transistor switches off and the second transistor switches

on. This produces a zero at the "0" input of the display circuit The preset must be adjusted so that the display comes on only when the input is at exactly zero volts.


Pig. 2-SPARK PLUG MONITOR


Fig. 4 shows the headlamp and brake-light sensors, one of which is required for each bulb to be monitored. When the lamp is on, a voltage is produced across the $0.5 \Omega$ resistor, turning on TR1 and consequently TR2. This produces a low input at G1, and so too does TR3 if the headlight switch is on. The exclusive or function of G1 produces a low output whenever the two inputs are the same.

The output of G1 is fed to the exclusive or array, which will produce a low, only if one or more lamps do not draw current when switched on. The brake-light will have a similar circuit, but with effectively only gates G3 and G5 in its or array. The value of the 0.55 ) resistor may need to be varied according to the bulb rating it is in series with.

Fig. 4-headlamp \& brake light sensor


The battery level indicator is shown in Fig. 5a. This is a simple comparitor, working from a reference Zener diode with its voltage divided down, to minimise the effects of supply voltage variation. When the input voltage falls below 11 volts, the output drops to logical 0.

The fluid indicators apply to hydraulic and coolant levels. The output of these probe networks are connected to similar comparitors to that shown in Fig. 5a. A typical probe arrangement is shown in Fig 5 b , where, if the fluid drops below the probe, conduction ceases and the output voltage drops. The comparitor output becomes logical 0 , displaying " F " or " C " on the display, depending on which probe.
The temperature unit is similar to the fluid level sensor, but a thermistor replaces the probe. The reference voltage is connected to the positive input of the comparitor, and the signal input to the negative. The reference voltage is set so that a logical 0 is produced when the temperature becomes excessive.

Decoupling of the i.c.s is essential due to the large amount of electrical noise produced in a motor car.
P. M. Glover, $\begin{array}{r}\text { Ockbrook, } \\ \text { Derby }\end{array}$

Fig. 3-OIL PRESSURE


Hig. E-LEVEL INDICATORS


## COUNTER

1 T is often a requirement to reset a 7490 counter to one instead of zero. The 7490 is in fact two separate counters in one package, with an external connection required between the $A$ output of the divide-by-two stage and the $B$ input of the divide-by-five stage.

These counters change state on a negative-going edge, so that if an inverter is put in the external loop between the stages, and the output of the inverter ( $A^{\prime}$ in Fig. 1) is now read as the output of the divide-bytwo stage; on reset the output count will read one.

TRUTH TABLE

| Basic <br> Count | A | $A^{\prime}$ | B | C | D | Modified <br> Count |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 2 |
| 2 | 0 | 1 | 1 | 0 | 0 | 3 |
| 3 | 1 | 0 | 0 | 1 | 0 | 4 |
| 4 | 0 | 1 | 0 | 1 | 0 | 5 |
| 5 | 1 | 0 | 1 | 1 | 0 | 6 |
| 6 | 0 | 1 | 1 | 1 | 0 | 7 |
| 7 | 1 | 0 | 0 | 0 | 1 | 8 |
| 8 | 0 | 1 | 0 | 0 | 1 | 9 |
| 9 | 1 | 0 | 0 | 0 | 0 | 0 |
|  | Outputs |  |  |  |  |  |
|  | to decoder |  |  |  |  |  |

After the first input pulse, the $A^{\prime}$ output will go to a low logic level, and as this is a negative-going edge

Fig. 1

BD INPUT

the $B$ output will go high, giving an output count of two.
lit can be seen from the truth table that the normal counting sequence will be followed, but running from one through to zero instead of zero through to nine.
M. R. Oakley,

Walsall.

## DIGITAL GLOCK TOUCH-SWITCHES

AMAINS alarm clock using the MK50253 clock chip was built, and it was decided that touchswitches were desirable for all functions. The high input impedance, low power consumption and cost, of cmos i.c.s made them ideal for this purpose, and in fact they worked out cheaper than ordinary push switches!

Two CD4.011 quad 2 input Nand gates (G1 and G2) were used. Most of the switches consist of simple refinements to Fig. 1, which is that used for the SNOOZE control. A $10 \mathrm{M} \Omega$ resistor ( R 1 ) holds both the inputs of Gla high, thus giving a low at the output. By placing a finger
across the input and ground, the output goes high, thereby enabling the respective pin on the clock i.c.
The circuit for setting minutes, tens-of-Minutes, and hours (Fig. 2), is similar, except that two diodes connected to the inputs of G1b and Gic allow the minutes to be advanced.

For the RUN, STOP, ALARM SET function, three gates and two diodes are required (Fig. 3). Diodes D3 and D4 are necessary to allow pin 15 of the clock i.c. to be floating when in the RUN mode.

The alarm on/off circuit shown in Fig. 4 is a simple flip-flop. The l.e.d. D5, and TR1, allow visual indication when the alarm is set.

Power can be derived straight from the existing supply if it does not exceed about 16 volts. TR1 can be any cheap p.n.p. transistor such as a 2N3703. Diodes DI to D4, are small signal silicon diodes such as 1 N 914 .

For the touch-plates, pairs of "defunct" metal cased TOI8 transistors were used. The heads were passed through small holes in the top of the case, and the appropriate wire soldered to the collector lead, which is usually connected internally to the case of the transistor. This gives a very neat appearance.
G. Watts,

Bordon, Hants.


Fig. 1


Fig. 2


Fig. 3


Fig. 4
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(Fig. 3), and then etched in the usual way.

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This process should work out considerably cheaper and simpler than conventional double sided p.c.b.s.
R. M. Henderson,

Newcastle upon Tyne.

## RIGHT DISPLAY

Sir-I would be grateful if any of your readers can explain to me why there are always two versions of 7 -segment display available? I refer to the l.h. and r.h. decimal point options.

If only they were manufactured with the decimal point (d.p.) "half way up", we could turn them through 180 degrees and make them into l.h. or r.h. decimal point as required
A little further thought on the pinout would ensure that no alteration need be made to the segment connections either
C. P. Finn, Beverley.

considerable care to be taken that both sides aligned correctly.

The difficulty can be overcome using single-sided board, by placing a strip of Veroboard, track-side down, on the copper clad surface of the circuit board. The position of the Veroboard is maintained by clamping it to the circuit board via pins inserted in diagonally opposite holes drilled through both boards simultaneously. As shown in Fig. 2, now that the Veroboard is held in register the copper surface can be marked through the Vero-holes with a sharp point. Next the printed circuit can be marked out, incorporating the points made through the Veroboard

## DOUBLE-SIDED BOARD

Sir-There are many cases where double-sided printed circuit board is a necessity, such as to provide a ground plane, or to meet the requirements of certain r.f. circuits. Another situation, where a double-sided p.c.b. would be useful to overcome a logic layout problem is shown in Fig. 1, in which a printed data bus is to feed various i.c.s. To do this on single-sided board would require many tedious and untidy hard wired links. The use of conventional double-sided p.c.b. would call for

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## 

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## NEW FROM CASIOTRON

A new range of these superb watches, available from October. Full details and photographs are not available yet but they should knock spots off all the competition. All with at least 9 functlon including backlight, plus Stopwatch to competition. All with at least 9 functiont including backlight, plus Stopwatch to measuring lap times to One Hundredth of a second. Slimmer than ever, around inch thick in some cases. We witl also be having a Casiotron Alarm Wateh with five way programming of the alarm. These watches will be All Stalniess'Steel with Mineral Glases face and Weter Reslstant to 3 atmospheres, 100 feet. We anticipate they will have a battery hatch with one battery lasting 15 months or more.
Fairchild Timeband Mains Digital Alarm Clocks
$\mathbf{C 5 0 0}$ (left) black or white £14•35; C6110 (centre) £15.90; C590 (right) $\mathbf{2} 24.95$


NEW FROM IBICO. Slim 6 digit 6 function watch plus backlight and CHRONOGRAPH, $1 / 100$ second to 1 hour. Lap and Net times. In the all Stainless Steel 402 ES Water Reslstant case. 451 ES £49.95. On leather strap 451 ELB c42. 50
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|  |  |  |  |  |  |  |  | ｜ 80116 |  | Bfx85 |  |  | 仡 |  | CIR | CUITS |  |
| ${ }^{2} \mathbf{N 6 9 7}$ | 0.30 | 2N3704 | 0.15 | 40361 | 0.50 |  | ${ }^{35}$ | － | 0.51 | BFX87 | 0.30 |  |  |  |  |  |  |
| 2N698 | 0.62 | 2N3705 | 0.15 | 40362 | 0.55 | BC161 | 0． 35 | 80132 | 0.54 | BFX88 | 0.30 | CA3020 | 2.00 | LM1800 |  |  | 30 |
| 2 N 699 | 0.55 | ${ }^{2} 33706$ | 0.16 | 40363 | 1.30 | BC167 | 0.12 | ${ }^{80135}$ | 0.37 | BFX89 | 1.25 | ca3020a | 2.29 | LM 1808 | 1．92 |  | 1．85 |
| 2 N 7 | 0.28 | 2N3707 | 0.18 | 40406 | 0.60 | BC158 | 0.12 | 80136 | 0.37 | BFY50 | 0.25 | CA3028B | 1.29 | LM | 1．75 |  | 2．75 $\begin{aligned} & 2.5 \\ & 1.50\end{aligned}$ |
| 2N7 | 0.28 | 2N3708 | 0.13 | 40407 | 0.52 | BC169 | 0.12 | 80137 | 0.38 | BFY51 | 0.25 | CA3028A | 1.01 |  | 0．85 |  | $\begin{array}{r}1.50 \\ 1.50 \\ \hline\end{array}$ |
| 2 N | 0.28 |  | 0.15 | 40408 | 0.75 | BC | 0.18 | ${ }^{80138}$ | $0 \cdot 38$ | ${ }^{\text {BFY }}$ | －0．30 | CA3030 | 1.35 2.00 |  | 1.40 |  | 1.50 3.91 1 |
| ${ }^{2 N}$ | 0.58 | ${ }^{2}$ | － 0.16 | 404098 | 0.75 |  | 0.16 | 8 | 0.40 |  | ${ }^{0.34}$ |  | 2.00 |  | $\bigcirc$ |  |  |
| ${ }_{2}^{2 N 718}$ | 0.27 0.50 | ${ }_{\text {2N3712 }}^{2 N}$ | 1.20 | ${ }_{40419}^{40410}$ | 2.85 | BC | 0．14 | ${ }^{80140}$ | 0.40 0.40 | ${ }^{\text {BFY90 }}$ | 1.20 0.50 | ${ }_{\text {CA }}$ | 1.40 0.99 | LM39 | 0.75 1.60 | TAA9308 | 1.30 |
| ${ }_{2 N T 20}^{2 N 7}$ | （ 0.90 | ${ }_{2}^{2 N 3773}$ | 2.30 | 40594 | ${ }_{0} 0.80$ | ${ }^{8 C 178}$ | ${ }_{0} 0.20$ | 8 B 2 | 0.45 | BSK | 0.33 |  | $2 \cdot 23$ | LM399 | 0.58 |  | 1.95 |
| 2 N 14 | 0.35 | 2N3714 | 2.45 | 40595 | 0.90 | BC179 | 0.23 | ${ }^{80241}$ | 0.45 | BSx21 | 0．32 | CA3049 | ${ }^{1.80}$ | MC1035 | 1.75 | ${ }^{\text {TBA }}$ TRA200 | 0．75 |
| 2N916 | 0.30 | 2 2N3715 | 2.55 | 40673 | 0.75 | BC182 | 0.11 | ${ }^{60242}$ | 0.50 | ${ }^{\text {Bu105 }}$ | 1.40 | CA3050 | 2.42 | MC1303 | 1.03 | ${ }^{\text {TBAACOO }}$ | 2．00 |
| 2N918 | 0.38 | 2N3716 | 3.00 | AC126 | 0.45 | BC182L | 0.14 | 8024 | 0.60 | Bu205 | 2.20 | CA3052 | ${ }^{1.62}$ | MC1304 | 1.40 | teasoo | 2．21 |
| $2 \mathrm{NS29}$ | 0.25 |  | ${ }^{1.95}$ | ${ }^{\text {ach127 }}$ | 0.45 | BC | 0.11 | ${ }^{80244}$ | 0.65 | MEO402 | 0.20 | ${ }_{\text {c }}^{\text {CA3080 }}$ | 0.75 1.85 | MC1305 | 1．40 | T8A | 2．21 |
|  | 0.28 | ${ }_{\text {a }}^{\text {2N3772 }}$ | 2．00 2. | ${ }_{\text {a }}^{\text {AC128 }}$ AC151V | 0.45 | BC183L | －0．14 | ${ }^{80245}$ | 0.65 0.66 | MEO404 | 0.15 | CA303086 | 1．88 | MC1310 MC1327 | 1 | tBas100 |  |
| 2N11 | 0.30 0.37 | ${ }_{2}^{2 \times 37789}$ | ${ }_{2}^{2.90}$ | ${ }_{\text {AC152V }}$ | ${ }_{0}^{0.40}$ |  | 0.12 0.14 0.10 | ${ }^{805296}$ | 0.65 0.45 | MEE4122 | 0.20 0.10 | CA3088 | 1.70 | ${ }_{\text {MC }}$ | 碞 | teas 20 | 2.21 |
| ${ }^{2} 1613$ | 0.30 | 2 N 3790 | 3．10 | AC153 | 0.55 | BC207 | 0.16 | 80530 | 0.50 | ME41 | 0.10 | CA3083 | 2.52 | MC | 0.90 |  | 2．30 |
| 2 N 1711 | 0.30 | ${ }^{2 \times 3791}$ | 3.10 | AC153k | 0.55 | BC208 | 0.16 | Bovzo | 1.00 | M 4481 | 1.55 | cas | 4.00 | MC1351 | 1.20 |  |  |
| ${ }^{2} 11693$ | 0.38 | ${ }^{2} 2 \times 3792$ | 3．50 | ${ }^{\text {ACLI76 }}$ | 0．50 | BC212 | 0.14 | ${ }_{\text {BFI } 121}$ | － $\begin{array}{r}0.38 \\ 0.55\end{array}$ | M．490 | 1．35 | CA3130 | ${ }^{0.98}$ | MC1352 | 10 | TBA540 | ${ }_{2}^{2.21}$ |
| ${ }_{\text {2 }}^{\text {2N22182 }}$ | 0.98 | ¢ | 0.20 0.36 | AC176K <br> AC187K | 0.65 0.60 | BC212L BC213 | － 0.17 | ${ }^{\text {BF } 121}$ | 0.55 0.55 | ${ }_{\text {MJ }} \mathbf{M} 491$ | 1.85 1.25 | LM301A | 0.67 0.45 | MC1558 | 1.91 0.40 |  | 2.21 2.30 20 |
| ${ }^{2} \mathrm{~N} 2218$ | 0. | 2N3320 | 0.38 | AC 188K | 60 | BC2 | 0.14 | BF152 | 0．25 | MJE340 | 1.25 0.58 | LM304 | 2.45 | NE556 | 1.10 | tras | 3．13 |
|  |  |  |  |  |  | BC214 | 0.16 | BF153 | 0.25 |  | 0.58 | LM307N | 0.65 | NE565 | 1.30 | teas500 | 3.22 |
| 2 2219A | 0.36 | ${ }^{2 N 3004}$ | 0.21 | adi62 | 1.05 | BC214L | $0 \cdot 11$ | ${ }^{\text {8F5 } 154}$ | 0.25 | M ME 371 | 0.60 | Lm3 | 1．82 | NES | 1.55 |  | ${ }^{3.22}$ |
| ${ }^{2 N 2220}$ | 0.35 | ${ }^{2 N 3906}$ | $0 \cdot 22$ | Afto6 | 0.55 | BC237 | 0.14 | ${ }^{8 F 159}$ |  | MJE | 0.45 | LM308N |  |  |  |  |  |
| ${ }^{2 N 2221}$ | 0.25 | ${ }^{2 N 4036}$ | 0.67 | AF109 | ${ }^{0.75}$ | BC238 | 0．12 | ${ }_{\text {BFF60 }}$ | －0．30 | MJE522 | 0.65 1.50 | ${ }_{\text {LM309K }}^{\text {LM317K }}$ | 1.85 <br> 3.00 | SAS | 2.50 | ${ }^{\text {TBACA4 }}$ |  |
| ${ }_{\text {2n }}^{\text {2n } 22222}$ | 0．26 | $\substack{\text { 2N }}_{2 \sim 1005}$ | 0.55 0.20 | ${ }_{\text {AF }}^{\text {AF } 124} \begin{aligned} & \text { AF } 125\end{aligned}$ | ${ }_{0}^{0.65}$ | ${ }_{\text {BC239 }}$ | 0.15 0.15 | ${ }^{8 F}$ | － 0.60 | MJE2955 | 1.50 0.95 | ${ }_{\text {LM318N }}$ | 3.00 2.26 | ${ }_{\text {SO4 }}$ | 2.58 <br> 1.25 | TEA651 | 2．20． |
| 2N2222A | 0.25 | 2N4059 | 0.15 | ${ }_{\text {af } 126}$ | 0.65 | BC253 | 0.22 | BF167 | 0.35 |  | 0.35 |  | 6．46 | 78001 N | 1.30 | TBA | 1．52 |
| 2N2368 |  | 14060 |  |  |  | －c3 | 0.17 | BFit3 | 0.35 | MP8112 | 0.40 | Lm339N | 1.40 |  | 20 | teapoo | ${ }^{1.61}$ |
|  |  |  |  |  | 0.50 |  |  | BF177 | 0.25 | MP8113 | 0.45 | LM348N | 1.50 |  | 1.50 | TB |  |
| $2{ }^{2} 23594$ | 0.25 |  | 0.18 | AF200 | 1.20 | BC2598 | 0.18 | BF778 | 0.25 | MPP102 | $0 \cdot 30$ | LM36N | 2.75 |  | ${ }^{50}$ |  | 98 |
| ${ }^{2 N 2646}$ | 0.75 | 2 N 4126 |  | AF239 | 0.65 | 8c261a | 0.24 |  | 0．30 |  | 0．25 |  | 2.50 1.70 |  |  |  | 2．25 |
| ${ }^{2} \mathrm{~N} 2647$ | 1.40 | ${ }^{\text {2Na } 289}$ | 0.20 | AF240 | ${ }^{1} 1.14$ | BC728 | 0．24 | ${ }_{\text {BFF191 }}$ | 0.35 0.35 | MPS | O．25 | LM | 70 | 7602 | 1.45 | TBAB10 | 1.25 1.25 |
| ${ }_{2}{ }^{2 N 292904}$ | ${ }_{0}^{0.36}$ | ${ }^{2} 129420$ | ${ }_{0}^{0.65}$ | ${ }_{\text {AF280 }}^{\text {AF279 }}$ | － 0.85 | ${ }_{\text {BC300 }}$ | O． 0.40 0.40 | ${ }_{\text {BF182 }}$ | O．35 | MPSA5S | 0.25 | Lм373N | 2.80 | ${ }_{76023 \mathrm{ND}}$ | 1.26 | teaszo | ${ }^{1.25}$ |
| 2 N 2905 | 0.37 | 2 N 4921 | 0.50 | BC 107 | 0.15 | BC301 | 0.40 | 8FF183 | 0.40 | MPSASS | 0.25 | LM374N | ＋1．10 | 763 | 2．20 |  | （2．90 |
| ${ }_{2}^{2 N}$ | 边 $\begin{aligned} & 0.38 \\ & 0.28 \\ & 0\end{aligned}$ | ${ }_{2}^{2 N}$ | 0.55 0.70 | BC108 BC109 | 0.15 0.15 | BC333 BC307 | 0.50 0.15 | ${ }_{8 F}^{8 F}$ | ${ }_{0}^{0.38}$ | MPSU05 | 0.50 0.56 | LM377N | 1.75 2.25 | ${ }_{761}^{761}$ | 1.18 1.51 1.51 |  | ${ }^{2.99}$ |
| ${ }_{2}^{2} \mathrm{~N} 2$ | － 0.35 |  | 0.70 0.60 | ${ }_{\text {BC }}$ | 20 | ${ }_{\text {BC }}$ | 0.15 0.15 0 | ${ }_{8 F}$ | － 0.15 | MPSUS5 | 0.56 0.55 | LM379s | ${ }^{2} .95$ | ${ }_{7616 \mathrm{~N}}$ | 1.65 | TCA160C | 1．65 |
| 2 N 2907 |  | 2N5191 | 0.70 | BC115 | 0.20 | BC309C | 0.15 | BF995 | 0.15 | MPSU56 | 0.60 | Lma | 0.90 | 76131 N | 1.20 |  | 1．61 |
| 2 N 290 | 0.25 | 2 N 5192 | 0.75 | BC116 | 0.19 | BC317 | 0.14 | ${ }^{\text {BF }} 196$ | 0.15 | T1P29A | 0.45 | LM38 | 0．988 |  | 1.56 |  | 2.25 1.30 |
| ${ }^{\text {2N2224 }}$ | 0.15 | 2N5195 | 0.90 | BC115A | 0.20 | ${ }^{\text {BC318 }}$ | 0.13 | ${ }^{\text {BF }}{ }^{197}$ | 0.17 | ${ }_{\text {T1P23C }}$ | 0.60 | lim381A | 2.45 1.60 1 | ${ }_{76228}^{7622}$ | 1.20 1.41 | TCA290a |  |
| ${ }_{2}^{2 N 32929}$ | 0.17 0.55 | ${ }^{2 N}{ }^{2 N 5245}$ | 0.34 0.40 | ${ }_{\text {BC117 }}^{\text {BC11 }}$ | 0.22 0.20 | ${ }_{\text {BC3 }}{ }^{8 C 37}$ | 0.20 | ${ }^{8 F 198} 8$ | 0.18 0.35 | ${ }_{\text {T1P30A }}^{\text {T1P }}$ | ${ }^{0.69} 0$ | LM3882N | 1.60 1.25 1 | ${ }^{762353 N}$ | 0.75 |  | 1．84 |
| 2 N | 0.2 |  | 0.40 | BC119 | 0.30 | BC337 | $0 \cdot 19$ | BF225 | 0.25 | TIP31A | 0.50 | LM 384 N | 1.45 | ${ }^{76532 \mathrm{~N}}$ | 1.40 |  | ${ }^{3.22}$ |
|  |  |  |  |  |  | －3038 |  |  | 0.35 |  | 0.66 | LM386N | 0.80 | ${ }^{76533 N}$ | 1.20 | CA740 | 76 |
| ${ }^{2} \times 3055$ | 0.70 | 2N5298 | 0.40 | ${ }^{\text {BC132 }}$ | 0.30 | BC547 | 0.12 | 8F245 | 0.40 | TIP32A | 0.55 | LM3 | 1.05 | 7654 |  | tca | 30 |
| ${ }^{2} \mathrm{~N} 3380$ | 0.20 | 2 N 547 | 0.15 | BC134 | 0.20 | BC548 | 0.12 | ${ }^{85246}$ | －0．75 | ${ }_{\text {TP3 }}$ | 0.75 | LM | 0．90 |  | 1．65 |  |  |
| ${ }^{2} 123391$ | 0.20 | ${ }^{2 N 5448}$ | － 0.15 | ${ }^{\text {BC135 }}$ | 0.20 | ${ }^{\text {BC54 }}$ 8． | － $0 \cdot 1.13$ | ${ }_{\text {er }}^{\text {BF254 }}$ | 0.24 0.24 | ${ }_{\text {T1P }}^{\text {T1P33A }}$ | 0．30 |  | 1.00 0.75 |  | 1．44 | UAA170 |  |
| ${ }_{2 N}^{2 N 392}$ | － 0.16 | ${ }_{\text {2NS457 }}$ | ${ }_{0} .32$ | BC137 | 0.20 | ${ }_{8 C r 31}$ | 1.00 | $8{ }^{\text {P25 }}$ | 0.37 | T1P34A | 0.90 | LM70 | 0.65 | ${ }^{76552 N}$ | 0.55 | UAA180 | 2.00 |
| 2 N | 0. | $2{ }^{2 \times 5456}$ | 0.33 | BC 140 | 0.35 | BCY32 | 1.00 | ${ }^{\text {BF225 }}$ | 0.45 | ${ }^{\text {T1P34C }}$ | 1.20 | LM70 | 0.45 | ${ }^{765770 N}$ | ${ }^{1.68}$ |  |  |
|  |  |  | 0.29 | BCL41 | 0.40 | $\mathrm{BCr}^{3} 3$ | 1.00 | 8F259 | 0.49 | ${ }^{\text {T1P }}$ TP3A | 2.50 | LM710 | 0．60 | ${ }^{766202 N}$ | 0.90 1.10 |  |  |
|  | 0.88 0.64 |  | 0.34 0.38 | － | O． 0 0.30 | 8 | 1.00 2.00 | ${ }^{\text {BFF439 }}$ | 0.50 0.28 |  | 2．80 | LM |  | ${ }_{76656} 76$ | ${ }_{0} 0.60$ |  |  |
|  | 0.64 0.81 |  | 0.38 0.60 | ${ }^{\text {BCC147 }}$ | －． 0.12 |  | 2.00 0.80 | BFS21A | 2.60 | ${ }_{\text {TIP41C }}^{\text {T1 }}$ | 0.90 | LMTz3N | 0.75 | 76666 N | 0.92 |  |  |
| $2{ }^{2} 3442$ | 1.35 | 2N6101 | 0.45 | BC148 | 0.12 | BCY58 | 0.25 |  | 1.38 | ， | 0.80 | LMT74C | 0.65 | TAA32 | 1.00 |  |  |
| 2 N 3 | 0.16 | 2 N 6107 | 0.42 | BC149 | 0.14 | BCY59 | 0.25 | BF | 0.30 | TiP | 1.00 | LM7 | 0.40 | TAA350A | 2.48 |  |  |
|  |  |  |  | ${ }^{\text {BC } 153}$ | 0.27 | ${ }^{8 C Y 70}$ | 0．25 |  | 0.30 0.35 |  | 0．65 |  | 0.40 0.90 | TAAS52 | 90 |  |  |
| － 2 23639 31 | $\bigcirc$ | ${ }^{2}$ | 0．41 | ${ }^{\text {BCF57 }}$ | 0.14 | BCY72 | 0.24 |  | 0.35 |  | 0.43 |  | 0.55 | taA550 | $0 \cdot 60$ | and |  |
| 2 N 3702 | 0.13 | 2N6123 | 0.43 | BC558 | 0.14 | 80115 | 0.80 | BFx84 | 0.35 |  |  | LM 748 N | 55 | tas60 | 1．75 |  |  |

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| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 04001 | 0.24 | CD4019 | 0.70 | CD4042 | 0.96 | CD4060 | 1.27 | CO4082 | 0.25 | 74 LSO4 |



 | CD4010 | 0.64 | CD 402 |
| :--- | :--- | :--- | :--- |
|  | 0.64 | CD 4025 |

 CO4029
CD4030

1. | 74LS 138 |
| :--- |
| $74 \mathrm{LS} 15 \dagger$ |
| 74 S |
| 1 | 74LS151 74LS 5160

74LS161 74LS162 $742 S 162$
745163
74 LS 164 $\begin{array}{ll}74 \text { LS } 173 \\ 74 \\ 74 \mathrm{LS} 174 & 1\end{array}$ 74LS

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| M119 | 0.04 | BC178B | 0.11 | BF167 | 0.21 | 0071 | 0.35 | 2 23703 0.14* | 1125 0.10* |  |  | 2.2. 4 | 7,6. 10 | 22, 33.3 | 47, 100. 200. | 555 | 0.490 | 7400 |  | 74191 | 2.10p |
| AC125 | 0.25 | BC1798 | 0.11 | ${ }^{\text {BF }} 173$ | 0.20 | DC72 | 4.45 | $2 \mathrm{~N} 37040.0 .13^{\circ}$ | 1/59 0.10* | 47/35 | $0 \cdot 12^{*}$ | 470, 560, 1000, 1500, 2200, 3000, 4700, 10000 47000pt: tMFD 10V. All at $6 p^{*}$ -ach. 1 MFD $63 \mathrm{~V} \mathrm{tp}_{\mathrm{p}}$. |  |  |  | 709 (TOS9) <br> 709 (8 PIN DIL) <br> 741 ( 8 PIND D ) <br> AY-5-1224 | 0.35 p | 7401 | 95 30 80 |  |  |
| ${ }_{\text {AC126 }}$ | 0.23 | BC1828 | $0.12^{*}$ | 8F 178 | 0.24 | 0 C 74 | 0.45 | $2 \mathrm{3} 37050.14{ }^{\text {a }}$ | 1/75 $\quad 0.10^{\circ}$ | 50/10 | 0-10" |  |  |  |  | 0.40 p | 7402 | 1 Bp | 7192 |  |
| AC127 | 0.21 | BC182L | 0.119 | 8 F 179 | 0.25 | OC81 | 0.60 | ${ }^{2} \mathbf{N} 3707080.12^{*}$ | $2.2250 .10^{\circ}$ | 50/15 | $0.10^{\circ}$ |  |  |  |  | 0.26 | 7403 | $1 \mathrm{H}_{1}$ |  |  |
| ${ }_{\text {AC128 }}$ | $0 \cdot 20$ | BC1838 | $0.10^{*}$ | BF183 | 1.34 | OC82 | 0.70 | $2 \mathrm{~N} 378880.12^{*}$ | ${ }^{2.2633} 0.10{ }^{\circ}$ | 100118 | $0.06{ }^{\circ}$ |  |  |  |  | 3-759 | 7404 | $23 p$ | C/MOS |  |
| ${ }^{\text {ACIL5 }}$ | 0.35 | BC183 | - 0 10** | ${ }^{8 F 184}$ | 0.25 | ORP12 | 0.68 | ${ }^{2} 23370900.14{ }^{\circ}$ | ${ }^{2.5664} 0.10^{*}$ | 10025 | $0.10^{\circ}$ |  |  |  |  |  | AY-3-8500 T.V. |  | 7409 | 408 | 4000 | 0.19 |
| ${ }^{\text {AC153 }}$ | 1.35 | 8 Cl 184 B | 0.12** | ${ }^{8 F 185}$ | $0 \cdot 20$ | TIP82a | 0.47** | ${ }^{2 N 3710} 0 \cdot 11^{* *}$ | $\begin{array}{ll}4.7 / 16 & 0.044^{*} \\ 4.763 & 0.10^{*}\end{array}$ | $100 / 35$ 100.50 | $0.11{ }^{0.10}$ |  | hird WA | E92 (5\% |  |  | Game CA 3130 | ${ }_{0}^{6.009} 0$ | 7408 | 240 | 4001 | $0 \cdot 10$ |
|  | 0.22 | ${ }^{\text {CCl }} 1845$ | 0.11* | ${ }^{\text {BF }} 194$ | \$.10* | Tip30A | 0.56" | $\begin{array}{ll}\text { 2N3711 } \\ \text { 2N3619E } & 0.11^{*} \\ 0.25 *\end{array}$ | $\begin{array}{ll}4.7 / 63 & 0.10^{\circ} \\ 50.10 & 0.10^{\circ}\end{array}$ | $100 / 50$ $400 / 35$ | ${ }^{0.155^{\circ}}$ | fohm | -10m oh | m . |  |  | CA 3130 LM 3014 A | $0.1770^{\circ}$ 0.550 | 7410 | 110 | 4002 | 0.19 |
| AC187 AC188 | 0.23 0.20 | BC186 BC187 | 0.25 | BF 195 BF96 | - $6.100^{\circ}$ 6.12 | TiP31a | 0.57 0.67 | $\begin{array}{ll}\text { 2N3819E } & 0.25^{*} \\ \text { 2N3820 } & 0.45^{*}\end{array}$ | $\begin{array}{ll}5.10 & 0.10^{\circ} \\ 5 / 16 & 0.11^{\circ}\end{array}$ | $100 / 35$ $20 / 16$ | $\begin{aligned} & 0.15^{\prime \prime} \\ & 0.15^{\circ} \end{aligned}$ |  | m |  |  | LMM 3014 AN | $\begin{aligned} & 0.550 \\ & 1.400 \end{aligned}$ | 7411 7412 | 240 250 | 4006 | 1.45 0.15 |
| 187/188 |  | BC204A | $0.16{ }^{\circ}$ | 8F197 | $0 \cdot 12^{*}$ | TIP33A | 0.81 | 2N3823E 0.25* | 6-8,25 0.10* | 220125 | $0.16^{\circ}$ | POTE | NTIOME |  |  | LM 3 309k | 2.00p | ${ }_{74 \%}^{74}$ | 330 | 4007 | 0.19 1.49 |
| mich. pr. | 0.85 | BC2048 | 0.16* | BF199 | $0.15{ }^{*}$ | tipza | 1.13 | $2 \mathrm{~N} 4036 \quad 0.40$ | 6.840 0.10* | 20063 | $0.25 *$ | Linilo | +10m |  |  | L.M 324 | 2.050 | 7414 | 72 | 4009 | 1.49 0.55 |
| AD149 | 0.68 | BC2098 | 0.13* | BF200 | - 38 | TIP41A | 0.77 | 2N4058 $0.15^{*}$ | 8170 | 250112 | -120' |  | 25K. |  | 250K, 500k. | LM 380 SL60745 | 1.290* | 7416 | 36 p | 4010 | 0.54 |
| AD161 | 0.52 | BC212A | 0.13* | $\mathrm{BFX} 29^{\text {a }}$ | ${ }^{0} 28$ | TTP42A | 0.80 | 2N4059 $0 \cdot 10^{\circ}$ | 10116 0.00* | 250.50 | *130 | 1M, 2 | $1{ }^{2} 85 \mathrm{C}^{+}$ | soch. | 250k. 500 K . | LM 38.1 N | 2.009* | 7417 | 380 | 4011 | ${ }_{0.19}^{0.5}$ |
| ${ }^{\text {ADA62 }}$ | 0.52 | ${ }^{\text {BC212L }}$ | 0.15** | ${ }_{\text {BFX }}$ BF30 | 0.25 | TIP2955 | 0.77 | ${ }^{2} \mathrm{~N} 4061$ O.12* | $10 / 250$ | 250/64 | *. $25^{2 *}$ |  |  |  |  | LM 555 | 0.490 | 7420 | 14 p | 4012 | 0.19 |
|  | 1.24 | 3C2138 | $0.12{ }^{\circ}$ |  | 0.24 | TiP3055 | \%.50 |  | $\begin{array}{ll}\text { H0/35 } & 0.10^{*} \\ 10.64 \\ 0.10 *\end{array}$ | $330 / 16$ $470 / 6 \mathrm{~V} 3$ |  |  |  |  |  | LM 723 | 0.59 p 0.69 p | 7421 | \% ${ }^{2}$ | 4013 | 0.54 |
| ${ }_{\text {AF116 }}{ }_{\text {AF117 }}$ | 0.24 0.24 | BC213L | 0.14** | 8FX84 $8 \times \times 88$ | 0.22 0.22 | T1S43 |  | $\begin{array}{ll}\text { 2N4126 } & 0.30 * \\ \text { 2N5298 } & 0.50\end{array}$ | $\begin{array}{ll}10 / 64 & 0.10^{*} \\ 10250 & 0.18^{*}\end{array}$ | 470:6V3 47010 | - $0.10^{*}$ | PRES | ET MIN. | VERT. |  | MC 1310/CA1310E | $0.69 p^{\prime}$ 2.550 | 7427 | 329 | 4014 | 1.42 |
| AF124 | 0.30 | BC214L | 0.17* | BFY50 | 0.25 | T1×300 | $0.13^{*}$ | $\begin{array}{ll}2 N 5457 & 0.50\end{array}$ | 15.40 0.10* | 470.16 | $0.14 *$ | SU8 | MN 4 |  |  | MC 1327/SN76227 | ${ }_{1} .355^{\circ}$ | 7428 7430 | 509 180 | 4015 | 1.16 |
| AF185 | 0.95 | BC237A | $0.16{ }^{\text {* }}$ | BFY51 | 0.25 | 27X301 | $0.13^{*}$ | 2 N 5458 B | 15.400 0.35* | 470/25 | - 220 | 4000 ${ }^{\text {a }}$ | OK, 2200 | 50k, 4700 |  | MC 1330 P | $0.750^{*}$ | 7432 | ${ }_{29}{ }^{\text {ap }}$ | 4016 4077 | 0.52 1.12 |
| AF239 | 0.46 | BC238A | 1.15* | 8FY52 | 0.25 | $27 \times 302$ | $0.11{ }^{*}$ | 2 N 5459 0.40* | 16.10 0.16* | 68025 | $0.25{ }^{\circ}$ |  | 10k, 2 k . | 50k. 100 | 20K, 40K. | MC 1350P | $0.750^{\circ}$ | 743 | 420 | 4018 | 1.8 |
| AU113 | $2 \cdot 20^{\circ}$ | 8C261a | $0 \cdot 16$ | BSX20 | 0.23 | $27 \times 500$ | $0.15 *$ | $2 \mathrm{SC1172} 3.60^{*}$ | $20 / 15 \quad 0.10^{*}$ | 100016 | $0.25{ }^{\text {a }}$ |  | up |  |  | NE 535 | 0.490 | 7440 | 150 | 4019 | 0.51 |
| BC107 | 0.11 | BC262A | 0.19 | 84108 | ${ }^{2.500}$ | TXX502 | $0.10^{*}$ | 40361 0.50 | 20770 | 1000225 | $0.30{ }^{\circ}$ |  |  |  |  | SK 1122 T.V. |  | 742 | sep |  |  |
| BC107A | 0.12 | BC267A | 0.17 | BU208 | $3.00 \times$ | $27 \times 504$ | $0.25{ }^{*}$ | 40363 0.86 | 22\%673 - $0 \cdot 10^{*}$ | t000, 50 | 0.40** |  |  |  |  | Game | 10.00 D | 74 | 1.00p |  |  |
| BC1078 | 0.13 | BC268 | 0.17 | ${ }^{\text {BY126 }}$ | ${ }^{6} 168$ | $27 \times 530$ | $0.23{ }^{*}$ | 40673 0.65 | ${ }^{22 / 16} 00 \cdot 100^{\circ}$ | 1500225 | $0.35{ }^{\text {0, }}$ | 60 V | 14 |  |  | SN 76003 N | 2. $\mathrm{cop}^{*}$ | 744 | 1.80p |  |  |
| BC108 | 0.10 | 8C299 | 0.17 | ${ }^{8 Y 127}$ | 0.16 | tN914 | 0.05 |  | $25 / 25$-11** | 220016 V 3 | -1.30** |  | 1A | 0.38 |  | SN 76013ND | 1. $60 \mathrm{p} \mathrm{P}^{*}$. | 7446 | 1.000 | diodes |  |
| CILS08 | 0.08 | 8C287 | 0.21 | $8 Y 133$ $8 Y 164$ | 0.20 | ${ }^{1} 12009$ | 0.05 |  | $\begin{array}{ll}3350 \\ 47 / 543 & 0.12^{*} \\ 0\end{array}$ | 2200040 | $0.50^{\circ}$ 0.45 | 200 V | ${ }_{1}^{1}$ | 0.60 | TAG 1200 | SN 76013N | 1.75p** | 7447 | 34 | 50 V 3 A | 0.13 |
| BC108B BC109C | 0.91 0.12 | $8 C 300$ $8 C 301$ | 0.35 0.34 | CY164 | 0.40, | 1N4002 in4003 | 0.06 0.09 |  |  | 250015 $3300 / 30$ | $0.45^{*}$ 0.45 | 600 V | ${ }_{1 A}^{1 A}$ | 0. 010 | TAG 1600 | SN 76023N | 1.75p** | 7448 | 2 | 100V 3 A | 0.15 |
| BC109 | 0.12 | BC303 | 0.35 | ME0402 | 0.13: | 1 N 4004 | 0.08 |  | $47 / 16 \quad 0.10^{*}$ | 5000.12 | $0.45^{*}$ | T00V | ${ }^{14}$ |  | BT 106 | SN 76033N | 2.750* | 7460 | ${ }_{18 p}^{18 p}$ | 200V3 ${ }^{\text {a }}$ | 0.10 0.21 |
| BC:4098 | - 13 | BC327 | 0.26 - | ME0411 | $0.18{ }^{\text {' }}$ | 1N4005 | 0.09 | tran |  |  |  |  | $\stackrel{4}{6+}$ |  | C10601 | SN 76660 | $0.90 \mathrm{p}^{*}$ | 7470 | ${ }_{39}$ |  |  |
| ${ }^{\text {BCICOSC}}$ | 0.13 | $8 \mathrm{BC328}$ | $0.10{ }^{\text {0 }}$ | MEOM12 | 0.19* | iN4006 | 0. 10 | FORMERS |  |  |  |  |  |  |  | TAA 550 | $0.600^{*}$ | 7472 | 30 p |  |  |
| BC117 | $0.18 *$ | BC338 | $0 \cdot 16{ }^{*}$ | meopil | $0.15{ }^{\circ}$ | 1 N 4007 | 0:11 | 50-6 100mA | P0LY. A/Lead tovo 0 (09\% |  |  |  |  |  |  | tba lzaso | 1.30. $0^{\circ}$ | 1473 | 30 p |  |  |
| 8 C 136 | 0.18* | 8C310 | $0.16{ }^{\prime \prime}$ | MEOP14 | ${ }^{0.15 *}$ | 1 N 4148 | 0.05 | ${ }^{1.20}$ | $\begin{array}{ll}009 \\ 0022 & 0.06{ }^{\circ} \\ 0.06\end{array}$ |  |  |  |  |  |  | TBA 395 | 2.25p* | 7474 | 35p | brioges |  |
| ${ }_{8}^{8 C 142}$ | 0.24 | BC340 | $0.15 *$ 0.35 | ME0461 ME0462 | ${ }^{0.27 *}$ | 1N5430 in5401 | ${ }^{0.13}$ | 20.975 ma | $\begin{array}{ll}.0022 \\ .0033 & 0.06 * \\ 0.06 *\end{array}$ |  | $\begin{aligned} & 0.07^{*} \\ & 0.07{ }^{\circ} \end{aligned}$ | 2ENE | 3S ( 400 m |  |  | TBA 4800 | 1.25p** | 7475 | 49p | 100V 1A | 0.21 |
| BC143 BC147 | 0.24 0.09 | BC451 BC557 | 0.35 0.15. | ME0462 | $0.21^{\prime \prime}$ 0.14 | 1N5401 | 0.15 |  | .0033 .0077 | . 15 | $0.07^{0 .}$ | 3V. $18 \mathrm{~V}, 2$ | 3. 30 V . | All al 12 p | ach. | TEA 5200 TEA 5300 | \$.70p** | 7776 | 329 | 200V 1A | 0.30 |
| BC1478 | $0 \cdot 10$ | BC558 | 0.15* | MEA101 | 0.14* | 2 N 708 | -20 | $12.0-12 \quad 50 \mathrm{~mA}$ | 0058 0.060 | . 22 | $0.10{ }^{\circ}$ |  |  |  |  | TBA 5400 | 4.90P* | 7480 7481 | 85p 1.000 | 400 V 1 A | 0.75 0.65 |
| BC148 | $0.08{ }^{\text {c }}$ | 8C559 | -15* | MJE340 | 0.76 | 2N1613 | $0 \cdot 30$ | 1.30 | 0150.00 | . 37 | -.11* |  |  |  |  | TBA 5500 | $3.00 \mathrm{P}^{\prime}$ | 7485 | 1.30 p | 400 V 2 p |  |
| BC1488 | 0.70* | BCY70 | 0.15 | MJE3055 | 1.25* | 2N1711 | -.30 | 12-a-12 1A 3 - 50 | $0150007 *$ | 47 | 0.15* | LEO T | 7L 2090 | $125 \cdot 0.2$ |  | tBa 560CO | $2 \cdot 30 \mathrm{p}^{*}$ | 7486 | 430 |  |  |
| 8 C 149 | $0.10 *$ | BCY71 | 0.14 | MPF102 | 0.40* | 2N2102 | 0.50 | min $0 / P$ for | .022 0.07* | 1250 V | ${ }^{0.10^{*}}$ |  |  |  |  | TBA 641 | 2. 550 \% ${ }^{\text {c }}$ | 7490(A) | 35p |  |  |
| ${ }_{8 C 1498}$ | $0.11{ }^{*}$ | BC772 | 0.14 | OAS | 0.71 | 2N2219 | $0 \cdot 30$ | Oc71/2 use 75p | $\begin{array}{ll}.033 \\ .047 & 0.07 *\end{array}$ | $1.1600 V$ 1.0400 V |  |  |  |  |  | T8A 750 | 9. $90 \mathrm{p}^{*}$ | 7492 | 55p |  |  |
|  | $0.11{ }^{*}$ | BD123 | $0 \cdot 8$ | 0A10 | 0.62 | 2 N 2222 | 0.20 | $06-06 \quad 280 \mathrm{~mA}$ | -047 0.07* | 1.0400 V | $0.12^{+}$ | CIp fo | rabove |  |  | TBA 8000 | 1.35p** | 7493 | 55p | RED LED |  |
| ${ }_{8}^{8 C 153}$ | $0.78^{\circ}$ | 80124 | 0.30 | OAM | . 14 | 2N2646 | 0.65 | 2.40 |  |  |  |  |  |  |  | tba 810 So | 1.49P. ${ }^{\text {a }}$ | 7496 | 90 p |  | $\begin{aligned} & 10 \text { for } \\ & 0 \text { ? } \end{aligned}$ |
| BC154 | $0 \cdot 10^{\circ}$ | 80131 | 0.42 | OAB1 | 0. 30 | ${ }^{2 N 29260}$ | 0.13* | $12-6-12150 \mathrm{~mA}$ |  |  |  |  |  |  |  | T8A 8200 | 1. $20.0{ }^{*}$ | 7407 | 40 P |  |  |
| $\begin{aligned} & \mathrm{BC157} \\ & \text { BC157B } \end{aligned}$ | ${ }^{0.72^{*}} 0$ | 80132 80139 | 0:42, | OA90 | 0.07 0.08 |  | 0.15* | MOT $\quad 200.40$ | TANTALJM BEAD 0.1 MFD 35 V 130* |  |  |  |  |  |  | TBA $92200{ }^{\text {TRA } 9000}$ | 2. $2.50 \mathrm{p}^{*}{ }^{\text {a }}$ | 74.121 | 34 p | 8 Cl 108 C | 11 for 51 |
| BC158A | $0 \cdot 12^{\circ}$ | BD140 | $0.510^{\circ}$ | OA95 | ${ }^{0} 008$ | 2N3054 | 8.54 | P-1K2 8n | 0.15 MFD 35 V 13p* | 6.8 MFD:16V | $13 p^{*}$ *, |  |  |  |  | TCA 2700 | $2.20 \mathrm{p}^{\prime \prime}$ | 74141 | 30 p |  | 100 for ${ }^{\text {cos }}$ |
| BC159A | 0.12 * | .8D155 | 0.75 * | OA200 | 0.10 | 2N3663 | 0.28 | 200 mW 50p | $0.22 \mathrm{MFD} / 35 \mathrm{~V} 13 \mathrm{p}^{*}$ | $10 \mathrm{MFD} / 6 \mathrm{~V} 3$ | 13p* |  | cl. |  | ., pol | $\cup 14552300 \mathrm{~mW}$ |  | 74145 | 1.15p | 2N3702 |  |
| 8C172A | $0.15{ }^{\circ}$ | BDYZ | 0.60 | OA202 | 0.11 | 2N3055 | 0.80 |  | 0.47 MFD 35 V 13p* | 10 MFOLOV |  |  |  |  |  | Audio with data | 0.35p* | 74151 | $94 p$ |  | 100 for 8 |
| ${ }_{8 C 1738}$ | $0.10^{\circ}$ | 8F115 | 0.22 | 0 O 35 | 1.20 | $2 \mathrm{~N}_{364}{ }^{2}$ | 0.17* | displays | 1 MFD 35V 130* | 22 MFD 16 V | 140. |  |  |  |  | 2 N 1414 | $1.40 \mathrm{p}^{*}$ | 74974. | 1.20p | 2 N 3704 |  |
| 8 BC 17 | 0.17 | BF158 | $0.20 *$ | 0 OCH | 0.45 | 2N3646 | 0.17* | DL704 0.95 | $2.2 \mathrm{MFD} / 35 \mathrm{~S}^{13 p^{*}}$ | 17 MFD 10 V | 160. |  |  |  |  | 2102 | 2. $50 \%$ | 74180 | $1 \cdot 200$ |  | 100 for |
| BC178 | 0.18 | BF166 | 0.30 | 0.45 | 0.45 | 2N3702 | $0 \cdot 11$ | DL707 0.75 | 4.7 MFO/16V 13p* | $100 \mathrm{MFD} / 6 \mathrm{~V} 3$ | $2 \mathrm{p}^{\circ}$ |  |  |  |  | 2513 UC | 8.50p | 7490 | 1.60 p |  |  |

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| LM309K T03 5V | (1* |
| LM318 70 V U.S. | ¢2.25* |
| LM380N 2W A.F. | ${ }^{1}$ |
| LM3900 Quad op. amp. | amp. 75p* |
| MC1310 Yes only | $y$ 15p* |
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| SN76611 and 60 IF | IF $\quad$ ¢1.25 |
| TBAB10 7W A.F. | c1 |
| LEDa tin and $0 \cdot 2 \mathrm{in} \mathrm{dia}$ | 2 in dia |
| Red no cllo | 11p* |
| $0 \cdot 2 \mathrm{in}$ Red and clip | clip 15p* |
| Colour LEDs | 29p* |
| DISPLAYS (Red LED) | LED) |
| $0 \cdot 3 \mathrm{in}$ DL704/2 | $65 p *$ |
| - 3in DL707/2 | 65p* |
| $0 \cdot 51 \mathrm{n}$ DL747/2 | ¢1* |
| IGS308 Gas Detector | ector ¢5* |
| 390pF Med /Short Tuner | + Tuner \$1* |
| Audible warning blee 12V 100 mA | ing bleeper §1.49* |
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