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Encouragement for the Components Industry

EARLY this year a new kind of intervention into the British Electronics industry by the Secretary of State for Industry took place, when Mr Eric Varley announced in January that he was applying a scheme of selective assistance for the electronic components sector as envisaged under Section 8 of the Industry Act 1972. In the first instance a sum of £20,000,000 was being provided. Looked at in relation to the total turnover of the components sector, estimated to be nearly £1,000M for 1976, this can be considered a mere drop in the ocean, but apart from the stated intention that further assistance will be given if the response warrants it, the aid scheme has been welcomed by the industry who see it as providing support and encouragement for a limited number of relatively small projects which it might not otherwise be able to carry out.

Under the scheme UK-based firms will be encouraged to undertake projects intended to improve their efficiency and competitiveness. New products and production technologies can be promoted, companies can be restructured to rationalize production and independent studies by consultants can be commissioned.

In more detail, assistance may be given for design, development and production launching of new products and production technologies, including the research, design, development and production of new products and key electronic materials; the improvement of production technologies for productivity, quality and standardization through BS 9000; and the strengthening of engineering support in production launching. Assistance will be available in the form of a grant usually not exceeding 25% of the total eligible cost of the project but could be a 50% shared-cost contract recoverable by a levy on future sales. Costs of a project must normally not be less than £50,000 and it must be completed by 31st December 1980 as far as the Department's contribution is concerned.

Assistance will also be available for wide ranging projects involving restructuring of a company or a group of companies and associated resources, including the cost of independent consultants to advise on improvements to efficiency. Grants towards investment in capital equipment, plant, machinery and buildings with both production and restructuring projects, can also be made.

Clearly the Department of Industry requires to be satisfied that projects are viable and industrially desirable and that restructuring proposals are beneficial to the companies involved and desirable in terms of the industry as a whole. It may therefore not be just a coincidence that very soon after the announcement of the aid scheme, a streamlining of the component industry's trade associations was announced. Historically these have tended to be somewhat diverse, active components at one time being covered by two associations (BVA and VASCA), respectively linked with consumer and professional devices, while there was an association (RECMF) looking after the interests of the passive device manufacturers. Several years ago the first two merged to form the Electronic Components Board and now there is to be one organization, the Electronic Components Industry Federation (ECIF). It could be said that this change reflects that integration of active and passive components themselves which is now a technical fact of life.

The new Federation has stated that it looks forward to working closely with the National Economic Development Office Sector Working Party on Components who originally advised the Department of Industry on the desirability of the £20,000,000 aid which is now to be given. These close relations between industry, government-sponsored organization and a government department, though on the face rather involved, should provide a means of enabling the industry to meet new challenges—and these today are legion!

F. W. S.

General Interest Paper

The application of microprocessors to main frame design

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Keynote Address at the Conference on Computer Systems and Technology held at the University of Sussex from 29th to 31st March 1977.

Microelectronics has given us low-cost microprocessors and will soon give us low-cost high-speed memory. Some of the ways in which main frame computer architecture may develop are discussed against this background.

Introduction

At the present time we have both large computer centres consisting of main frames with a variety of peripheral and telecommunication equipment attached and also innumerable mini-computers scattered in laboratories and offices. Many of these are free-standing, but some have a data link to other computers. A feature of the last few years has been the growth of computer networks to which both large computer centres and small mini-computers can be, and often are, attached.

The essential feature of a main frame as found in a large present-day computer centre is that it provides processing power in a highly centralized way. It consists of several banks of core or semiconductor memory, amounting perhaps to as much as four megabytes serving one or two—rarely more—very fast processors. Everything is done to maximize the throughput of the processors, for example, by providing them with pipe-lines and with slave or cache memories. Directly connected to the main frame are banks of disk files, magnetic tape decks, card readers and punches, plotters, and similar devices. There are also remote job entry stations that are similarly directly connected. Indirectly connected, usually via a small computer used for switching, are teletypes, v.d.u.s, and small satellite computers.

The work-load of a typical large computer installation having a fast powerful main frame commonly consists partly of jobs big enough to tax the resources of the entire system and partly of a miscellaneous collection of small jobs. The operating system required to handle this work and to share the resources of the system between the various jobs in hand is very complex. In a purely batch operation this complexity can be handled and the object of the operating system, which is to achieve a high throughput through the sharing of resources between the various jobs, can be achieved. If, however, the same system is required to provide interactive access with a rapid response to a hundred or more users, then the problem of designing, implementing and tuning the operating system increases very greatly in complexity and is on the limit of what can be successfully achieved by a software team. Moreover the proportion of system resources consumed by the operating system itself tends to increase. In order to secure satisfactory performance, especially as regards interactive response time, it is necessary to provide a great deal of high-speed memory. Some of this is occupied by modules of the operating system and some is shared between the various jobs. None of the latter are permanently resident, but are brought in from a disk or drum when they become eligible for a slice of processor time. This is accomplished in one of several ways, namely, by rolling in and rolling out the entire program, by bringing modules in under the control of a space allocation routine in the operating system, or by the use of a hardware-supported paging system. There must be enough high-speed memory to support a sufficiently high level of multi-programming to enable use to be made of processor time that would otherwise be wasted in waiting for disk or drum transfers to take place.

Microelectronics has already given us low-cost microprocessors, although those at present available are slow in operation compared with the processors in main frames. We have yet to experience the availability of very low-cost high-speed memory. At present the relatively high cost of memory is limiting what can be done with microprocessors. Their main application—and it is one for which they are ideally suited—is in special-purpose applications, such as the control of peripheral equipment, the instrumentation of experiments, the control of industrial and other systems, and the like. In such applications each microprocessor can be provided with exactly the right amount of memory for the function that it has to perform.

An Operating System Implemented in Microprocessors

A computer operating system may be regarded as—and indeed is—a control system. There would thus appear to be scope for implementing an operating system by means of a number of interconnected microprocessors dedicated to the purpose, each microprocessor handling some specific task, for example, scheduling, memory allocation, etc. The operating system so implemented would control a main frame of the conventional kind. As far as possible its design would follow conventional practice, except that the various processes would run in microcomputers provided for the purpose instead of running in the main frame under multi-programming. The messages (sometimes known as events) that are sent from one process to another in a normal operating system would be sent from one computer to another along a low-speed channel provided for the purpose. A separate high-speed channel would be provided for the transfer of data in bulk and this would be connected to the main frame via one of the regular channels. Certain high level scheduling and accounting operations, while being properly considered as the concern of the operating

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With two colleagues, Professor Wilkes published, in 1951, the first book on computer programming and he is author of several other books. He has received numerous honours from universities and societies in Great Britain and abroad, and the British Computer Society, of which he was the first President (1957–1960), has made him a Distinguished Fellow.

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system, are conventionally performed by programs that run under the operating system as though they were programs belonging to users. These would continue to be run in the main processor. The filing system would be under the control of a microprocessor, but some help from object programs running in the main frame might be provided.

Since the various functions of the operating system would be performed in microcomputers and only object programs run in the main processor, the amount of process switching in the main processor would be much less than in a normal system. This would simplify the problem of memory management and reduce the amount of memory needed by the main frame. One would like to think that this, together with an increased throughput of object programs, would more than compensate for the cost of the microprocessors and their associated communication system.

The philosophy behind the proposal that has just been made is that functions that are well understood, and for which the necessary resources can be closely determined, are better done in inexpensive and relatively slow microcomputers, with direct access to the memory that they need, rather than in a very fast central processor. There is, however, the further motivation that, by divorcing the operating system from the central processor, one could hope to reduce significantly the excessive complexity of modern operating system that has already been remarked on. At the present time the designer of an operating system can have no confidence that it will not be misused in practice, for example, by attempting to run it with too small an allocation of memory. A self-contained system, with its resources permanently allocated to it, is likely to have advantages in this respect.

The Main Frame of the Future

One sometimes hears it suggested that the time is approaching when the costly main frame at present in use could be economically replaced by a group of microcomputers capable together of executing the same number of operations per second. For example, one could replace a pipe-lined processor with an average instruction time of 100 nanoseconds by a group of 25 microprocessors with an instruction time of 2·5 microseconds. If one divided up the memory with which the fast processor might be equipped—say 1 million words—among the microprocessors they would each get about 40 k words each. It could be claimed that the resulting system of separate computers would have the same power as far as small jobs are concerned as the original one. However, input and output must also be considered and it would be expensive to provide each of the 25 computers with its own input device and printer. Moreover no one running a computing service would want to have to look after 25 independent machines. He would prefer to have a common input route and for the results to come out on a group of printers. Moreover, he would want to have a single filing system in which library programs and users' programs and data could be kept. Viewed in this way it will be seen that what we are really discussing is whether the conventional main frame should be replaced by a main frame with 25 separate computing channels and a suitable buffering and control system for sending work through them and collecting the results. In other words, we are not so much discussing the replacement of the main frame in a computer centre by a battery of independent microcomputers, but rather we are discussing an alternative design for the main frame. The numbers in the above example reflect the state of affairs in late 1976 and will very rapidly become out-of-date. Microprocessors will improve in speed and semiconductor memory will become less costly; fewer channels will therefore be needed and the total amount of memory installed will much exceed what we are used to today.

Another argument sometimes advanced is that computing centres will become a thing of the past and that anyone who needs computing facilities will be able to have a personal computer of his own. Few people, however, would find this entirely adequate to their needs. They would require facilities for obtaining hard-copy on an adequate scale and would also require access to a central filing system, so that they could obtain the use of standard material and could share their programs and data with other users. This is sharing as a user requirement and is to be clearly distinguished from sharing imposed by a need to use equipment economically.

If a personal computer is to be connected to a central filing system there must be a telephone line between the user's office and the central facility; it becomes a good question to ask: at which end of the line should the personal computer be put? Personal possessiveness and distrust of central services demand that it should be at the user end, but the technical arguments tend to go in the other direction. The personal computer needs to communicate both with its owner via his v.d.u. and with the central filing system. The former it can perfectly well achieve through a telephone line of limited bandwidth; the latter can well use a greater bandwidth both in order to speed up transmission and to simplify buffering. Maintenance and testing would be much simplified if the computers were centrally located and those responsible for the maintenance would have the satisfaction of knowing that they were housed in suitable conditions. Finally, there would be a pool of central computers that could be allocated to casual users who dialled in. We are here back to sharing and even the most staunch advocates of low-cost stand-alone computers must recognize that there will always be users whose work-load would not justify the owning of their own computer.

There is, however, one economic argument in favour of the user having his personal computer in his own office and that is connected with the cost of telephone lines. Some users may need only infrequent access to the central filing system; given a computer of their own they could dial in briefly when they required such a connection and would not need to bear the cost of a connection maintained the whole time that they were working. This is perhaps the strongest argument for the installation of personal computers and the outcome depends on the attitude of the telephone administrations in the various countries. If they are able and willing to give us low-cost computer communications, we in the computing community will be glad to make use of them to their profit as well as our own. Otherwise we will seek to take advantage of the power that developments in microelectronics give us to make ourselves as independent as possible of communications.

The above argument has led to another view of the design of the main frame of the future, namely, that it should consist of a number—perhaps a large number—of computers each with its own memory. When he logged in, a user would become linked to one of these computers and would have exclusive use of it for the remainder of the session. When he was not computing it would remain idle.

All the computers available to users would not necessarily have the same amount of high-speed memory and a user would choose one suited to the needs of his work. It is tempting to propose that there should also be some high-speed memory available for sharing. It would then be the responsibility of the user—I am thinking of a sophisticated user dealing with a large problem—to distribute his programs and data between the dedicated and shared memory to the best advantage. This is the kind of challenge that experienced computer users take up readily and there is something to be said for letting them come to grips with it, instead of attempting to provide a system solution which can in the nature of things be only partially successful. I have always felt that existing multi-user console

systems do not make as much use as they might of the combined intelligence of the users who connect themselves to the system, but instead, put their entire trust in unintelligent software. However, any proposal for sharing high-speed memory presents formidable switching problems. If a satisfactory way of enabling a large number of processors to share a large bank of high-speed memory could be devised, then we would not be talking about dedicated memory at all.

Conclusion

This paper has explored some of the ways in which microprocessors might find application in the design of computer main frames. So far the application of microprocessors has been limited by the fact that the necessary memory to associate with them is still expensive, but this situation will change.

Many of the difficulties experienced with present-day computer systems using main frames with one or two multi-programmed processors arise from the acute disparity of speed between their high-speed memories and the fixed-head disks or drums used for paging or swapping. In due course it will become possible to replace the disks or drums by solid-state devices, such as bubble memories or charge-coupled memories, operating at greater speed. In the long term, the availability of really low-cost semiconductor memory may enable this level of memory hierarchy to be done away with altogether. In view of the improvement in performance that these developments will give, it would be a mistake to assume that main frames of the type that we are used to will not survive in essentially their present form.

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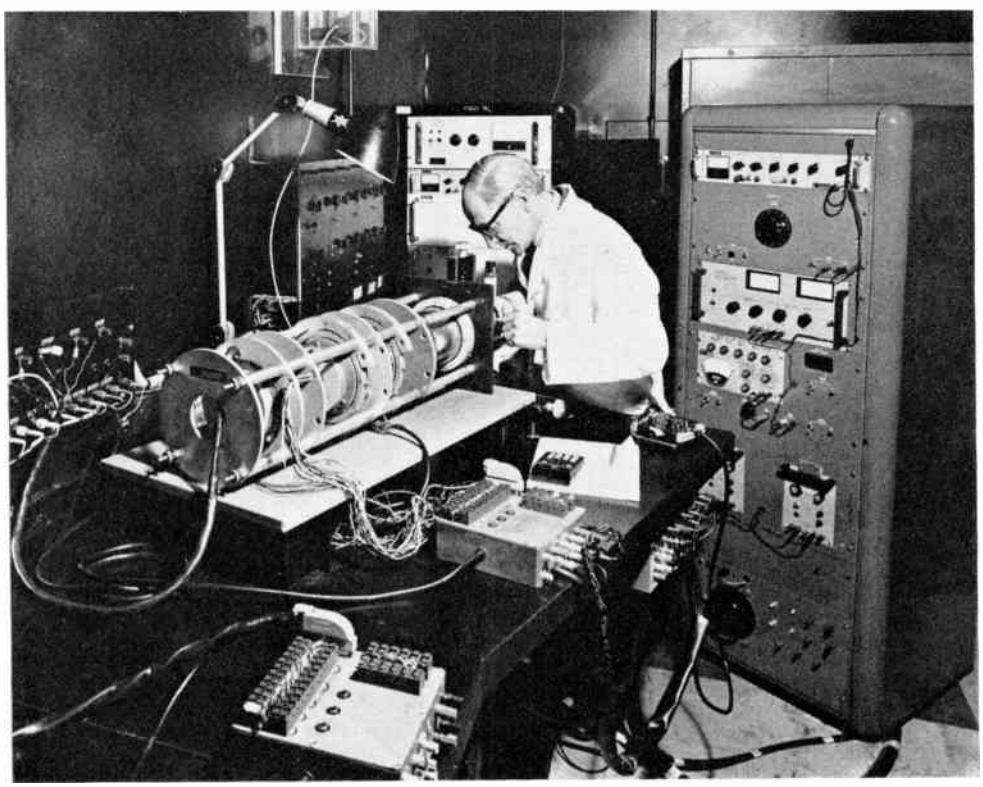
Cathode Ray Tube Testing



The photograph shows part of the new test facility at the Ferranti Special Components Department's new inspection area at Moston for precision coils and c.r.t. package systems. These include fibre optic c.r.t. packages for a medical recorder, large precision packages for photo-type-setting, flying-spot scanner units for telecine applications and a wide range of c.r.t. coil assemblies.

UDC 621.391.812.3.029.55

A digital high-frequency multipath propagation simulator

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and

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SUMMARY

A digital h.f. multipath propagation simulator is described which can be applied to communications receiver and modulation techniques evaluation and operator training. It can also be applied to a variety of applications in the high-frequency field where programmable and repeatable ionospheric conditions require simulation. Simultaneous communications paths are simulated, four of which exhibit independent delays, Doppler shifts, Rayleigh fade and phase variations and attenuation consistent with ionospheric reflection (skywave) paths.

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1 Introduction

The requirement for the High-Frequency Multipath Propagation Simulator described in this paper originated from investigations into modulation techniques suitable for use in the 1 to 30 MHz communications band. The resulting instrument is a novel exploitation of current semiconductor technology and embraces some new system concepts in propagation simulator design.

Severe ergonomic problems were posed by the requirement for both manual and remote computer control of the large number of settable coefficients. This led to the design of a special interface panel.

Propagation simulation is carried out at the intermediate frequency of 100 kHz to facilitate integration of the medium propagation characteristics into the total system studies.

The design study and development of the simulator were carried out by a university team under the auspices of the Industrial Electronics Group of the University of Surrey.

2 Simulator Parameters

The operational requirement was for an equipment to simulate the multipath propagation medium which is experienced in h.f. communications. Specifically, five independent and simultaneous communication paths were to be simulated, relating to a communications bandwidth of $\pm$ 10 kHz. The paths comprise: one specular (or ground wave) subject only to attenuation, and four ionospheric reflection (or sky wave) paths each subject to independent delays, Doppler shifts, Rayleigh fade and phase variations and attenuation. The equipment works at the receiver i.f. of 100 kHz (in real time) or at a lower frequency for expanded time scale operation. Control of the simulator parameters is carried out locally with an electronically interlocked panel or remotely from a digital computer. The specification is set out in Table 1, and the requirements are shown in schematic analogue form in Fig. 1.

3 Design Approach

At the core of the investigation was the problem of the implementation of a long delay line with suitable attenuation and dispersal characteristics and able to be tapped at several points simultaneously over 100 steps from 0 to $>$ 10 ms. A previous project, reported in this Journal,[1] suggested that a digital delay line provided a reasonably economical and compact solution and one which could be implemented using r.a.m.s with a sliding address algorithm.

Commitment to a digital delay line leads naturally to digital methods for the implementation of the various other machine parameters, i.e. Doppler shifts and Rayleigh phase control. Delay for all of these can be achieved through r.a.m. address modification. Consideration of all the phenomena to be realized through delay line manipulation led to a specification for the r.a.m. in terms of bits per sample, read/write rates and number of locations.

Having decided on so much of the simulator being

Table 1. Specification of the h.f. simulator

Number of simulated paths:	1 specular (SPEC) 4 ionospheric
Operation:	Real time (100 kHz) and non-real time
Non-real time operation:	10 kHz, 1 kHz (20% bandwidth)
Path parameters:	*Delay*—0 to > 10 ms in increments of 100 μs *Doppler*—0 to ±30 Hz in increments of 1 Hz *Fade rate*—0·1 to 25 fades per second in a binary geometric progression. Fading can be omitted from any channel, if desired *Attenuation*—0 to 40 dB in increments of 1 dB. Infinite attenuation can be applied to any channel that is not required
Calibration accuracy:	Better than ±1%
Noise sources:	Gaussian white noise (G.w.n.) level variable from 0 to −40 dB (or zero level) Impulsive noise (IMP) level as for G.w.n. Mean interpulse-arrival-time (MIT) variable from 0·1 to 16 seconds in a binary geometric progression
Parameter control:	Either by front panel controls or digital control from a Hewlett-Packard 2100 processor; control source selectable
Environment:	Laboratory

Notes:

(i) All parameters which are independent random variables, e.g. fading, are derived from pseudo-random sequence generators whose initial conditions can be defined to ensure repeatability of the simulated propagation conditions.

(ii) Since the specular (or ground wave) path must always arrive first at any receiving location, it can be subjected to zero delay in the simulation, so that all sky wave delays are relative to the ground wave datum.

implemented digitally, consideration was naturally given to digitizing the rest of the processor, i.e. the Rayleigh fade mechanism, attenuation control, noise generation signals mixing and parameter setting. Parameter setting is inherently digital if computer originating data are used and noise generation is easily implemented digitally using m-sequence generators. Therefore, it was decided to execute all processing digitally. Figure 2 shows, in outline, the translation of the analogue model of Fig. 1 into digital form.

Input signals, which are at an i.f. of 100 ± 10 kHz, are passed through a narrow window sample-hold amplifier and converted to digital samples in an analogue to digital convertor. The processed digital output, from the channels summer, is a series of digital samples which are converted to a train of analogue levels by a fast slew rate digital to analogue convertor (d.a.c.). The output envelope of the d.a.c. is at a sub-carrier frequency defined by the original sampling frequency. This sample train can be converted to a 100 kHz i.f. signal either by straight filtering as shown in Fig. 2 or by a low-pass sub-carrier followed by an up-convertor.

4 Design Concepts

It was decided to sample the incoming i.f. at 80 kHz at 8 bits per sample. This was based on information bandwidth/Nyquist sampling and dynamic range criteria respectively, backed up by the precedents of Reference 1. From these two fixed parameters, the storage capacity of the r.a.m. could be calculated and the slipping address algorithm defined. At 80 (eight bit) samples per millisecond, the rate of storage of bits is 640/ms. The requirement was for a signal delay of at least 10 ms leading to

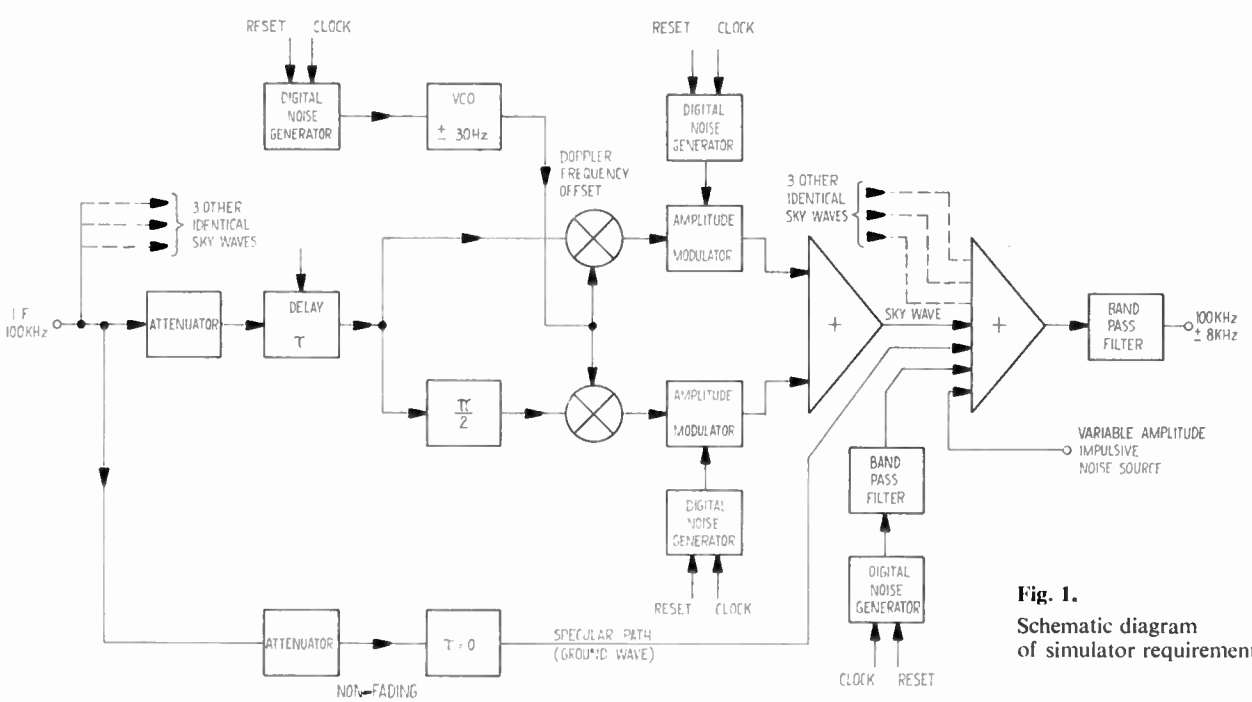

Fig. 1. Schematic diagram of simulator requirements.

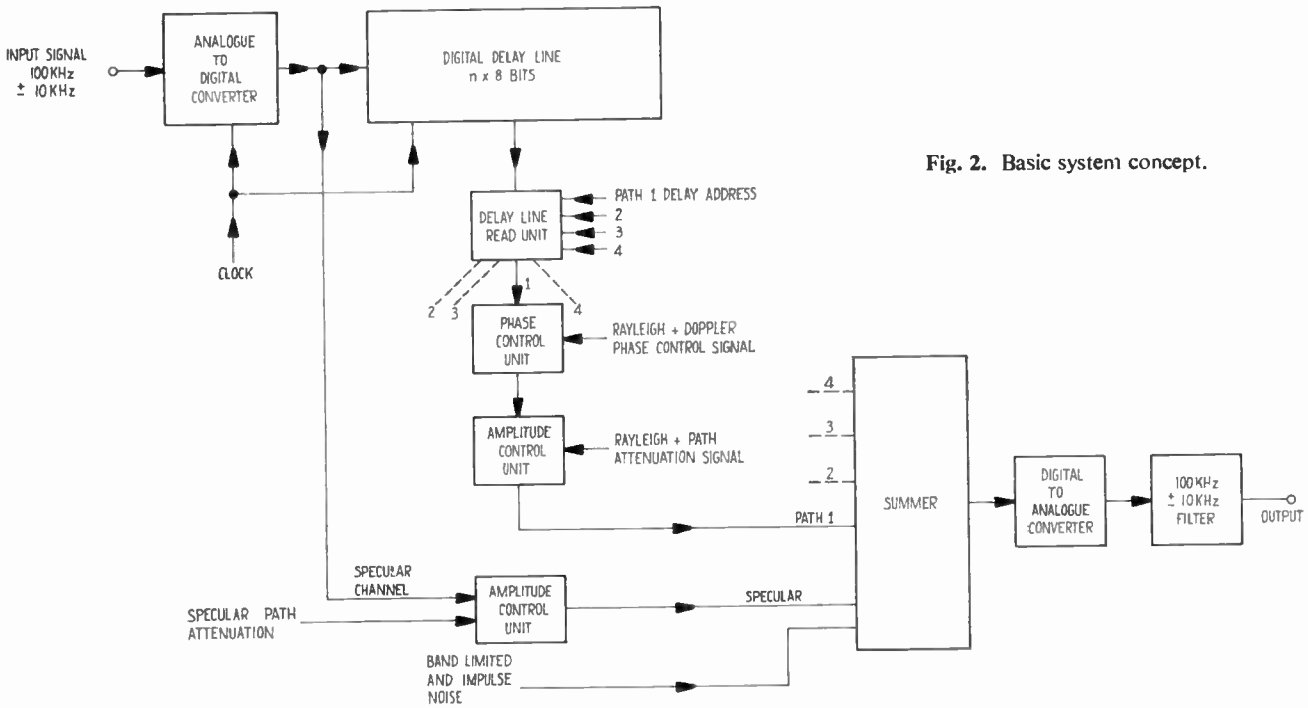

Fig. 2. Basic system concept.

6400 bits of storage. However, since the high density semiconductor r.a.m.s are available in units of 4096 bits, it was agreed that 2 of these should be used, yielding a total capacity of 8192 bits or 12·7 ms of delay.

The delay for each sky wave can then be determined by selecting the appropriate word address in the delay line. In principle, there is no limit (apart from resolution) to the number of delayed channels which may be generated; this is not so in practice, since the r.a.m. read/write rate imposes an upper limit of about 20 to 30 channels for the method of r.a.m. organization chosen.

In addition to the control of the delay time per channel, two other channel parameters need to be controlled independently; these are phase and amplitude.

(a) Phase control is exercised by utilizing the fact that the envelope of the samples on the delay line is at a frequency of 20 kHz (a down-conversion product of the input i.f. at 100 kHz and the sampling frequency of 80 kHz) and adjacent word addresses in the delay line represent a signal phase difference of 90°. Referring to Fig. 3, if the signal envelope appearing at word address $(n+1)$ is represented by $A \sin(\omega t)$ then the signal envelope at word address n is $A \cos(\omega t)$. These two adjacent address points, when multiplied by $\cos\alpha$ and $\sin\alpha$ respectively, and summed together, produce an output $A \sin(\omega t + \alpha)$.

Phase control is thus effected by controlling α which in turn makes possible a signal sample with any phase relative to the current signal sample. Rayleigh phase variations are caused by pseudo-random Markovian variations of α at the appropriate rates, and Doppler shift by steady increments of α at a rate determined by the selected Doppler frequency for the channel in question.

(b) Amplitude control is fulfilled by passing the digital signals through further multipliers. The multiplier coefficients are: a steady programmable number which determines the path attenuation and a pseudo-random variable which simulates the Rayleigh amplitude variation.

The two multiplications are done digitally as are the two for phase control. Therefore, for sky-wave processing alone, 16 multiplications are carried out in one 12·5 μs interval (corresponding to 80 kHz). Including the processing of the ground wave and noise sources, the total is 20.

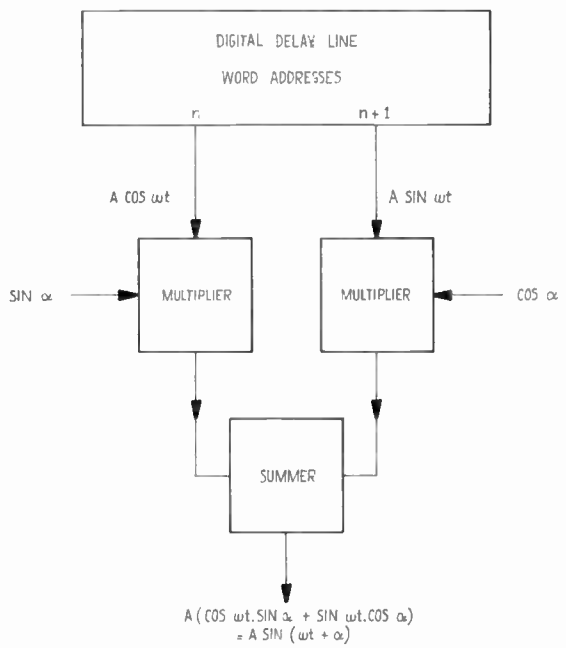

Fig. 3. Implementation of skywave phase control.

The four independently controlled sky-wave channel signals are summed together in a final summer together with (a) a ground-wave signal controlled in amplitude only, (b) a combined band-limited and impulsive noise signal and (c) an external noise source, to form a final composite output digital signal. After conversion from the resultant series of digital samples into analogue form, the composite simulated signal of 100 ± 10 kHz is recovered by suitable filtering.

All the nominally random digital noise signals are derived from a master pseudo-random binary sequence (m) generator which enables any correlation between the phase and amplitude component of the Rayleigh fades to be readily implemented.

5 Ergonomics

Since the requirement was for both local (i.e. front panel) and remote computer control, and because there are a total of 8 channels each with about 5 independent variables, it was important that considerable effort be devoted to optimizing the man/machine interface.

Because the proposed simulator is a digital machine, it was originally envisaged that parameter control would be exercised by a series of digital thumbwheel switches which would also act as parameter stores. However, this method of interface design was not considered to be in accord with established ergonomic principles since the operator would be confronted by around 90 decade thumbwheel switches (in addition to the system control functions, e.g. sequence start, clock rate start/stop, etc.). This leads, in turn, to difficulties such as the small non-optimum size of indication of the parameter numerals, problems of logical grouping of controls to help operator appreciation, etc. Consequently, it was proposed that a keyboard entry system be adopted with an optimized data indication and editing facility. The general format of the control panel is shown in Fig. 4, the control keys for the select parameter, select channel and status control functions are of the illuminated type; the data set-up keys control the lower parameter read-out display with its editing facility.

The design is such that when the simulator is in the 'auto (remote)' condition, all parameter control is exercised by a remote computer (which enters data directly into a parameter store (r.a.m.) and takes over the running of 'sequence reset'). While in this condition, the stored parameter data can be displayed by keying the appropriate parameters and channels, the stored data from the computer then appearing in the upper digital read-out position (labelled 'store display' in Fig. 4). The data set-up keyboard is not operative when in 'auto (remote)'.

When manual is selected, the operator's panel becomes available. As before, selection of the appropriate parameter and channel keys causes the appropriate stored data to be displayed in the upper position, the selected keys remain illuminated to identify the displayed parameter. Additionally, if the operator wishes to enter new data into the parameter store, he can key in the data which appear in the lower read-out position. In case of wrong keying, a clear key is available. After visual verification, the new data may be entered to the parameter store using the 'enter' key.

Facility is provided for resetting all the pseudo-random sequences to a fixed starting condition, altering the clock frequency for expanded time-scale operation and stopping the clock.

In order to provide for logical grouping of controls and unambiguous state indications, extensive interlocking logic is provided. Design of this system was almost an engineering project in its own right in view of the large number of keys and permissible (and impermissible) combinations. The resulting system prevents the operator from selecting impossible parameter configurations, e.g.

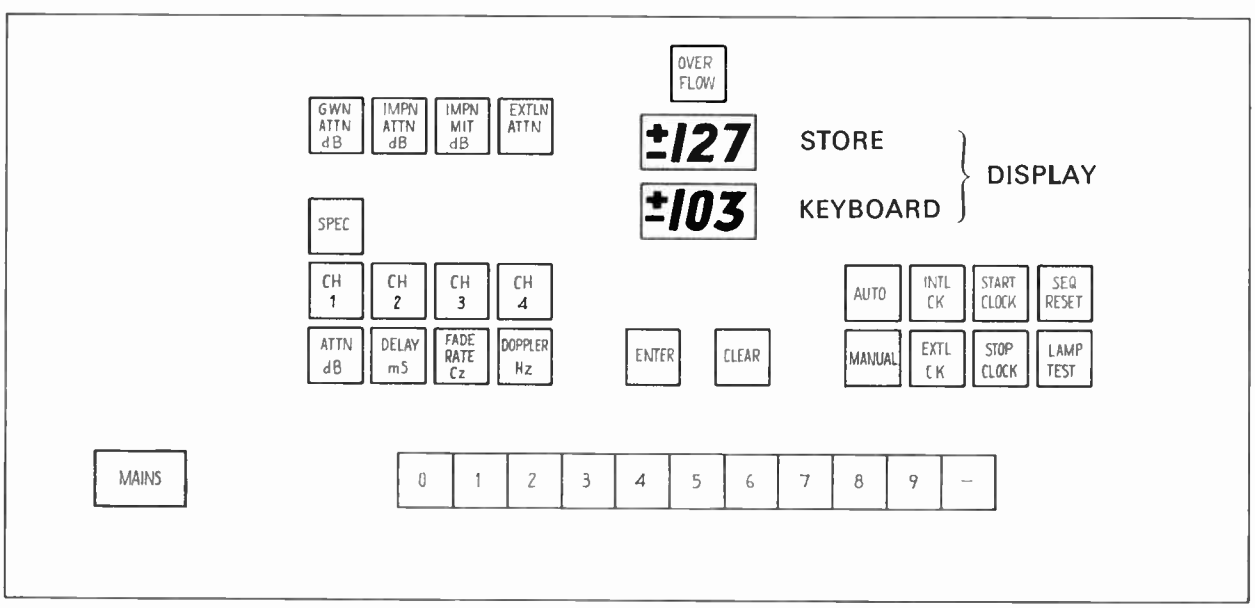

Fig. 4. General format of control panel.

out-of-range parameters (say >12·7 ms delay) or impossible combinations such as 'ground wave Doppler coefficient'.

6 Engineering Design

Standard 74 series (or equivalent) logic is used throughout, because of its availability, cost and compatibility with other equipment to which the simulator is interfaced. Discrete m.o.s. logic and all microprocessor technologies were considered but discarded on account of the processing speeds demanded. An appreciable proportion of the logic is needed to provide an operator interface which is foolproof. It would have been unnecessary if only computer originating data had been used as software checking could have been implemented in the HP 2100.

6.1 Panel Interface

The operator selects a channel (or noise source) and a parameter prior to keying in a decimal value. A typical example might be: channel No.: 4; parameter: attenuation coefficient (dB); parameter value: 39 (dB). In order to (a) avoid impossible combinations (in the logic), (b) avoid the need for invalid combinations detectors/indicators and (c) reduce the operator loading, a system of 4 *n*-stables is employed to ensure that any key operation results in a valid combination (which is related to the last key pressed). Each *n*-stable operates so as to make each of its *n* outputs mutually exclusive.

The *n*-stable outputs are:

(i) channel 1, 2, 3 and 4 (4 states)

(ii) specular channel, null (2 states)

(iii) delay, Doppler, Rayleigh fade, Rayleigh phase, attenuation (5 states)

(iv) G.w.n., external noise, IMP-MIT, null (4 states).

In addition, certain key operations associated with a given *n*-stable forces the states of other *n*-stables or extinguishes the indicators associated with a given *n*-stable (without changing the latter's state). For example, selection to 'specular channel' extinguishes the channel number indicators without losing track of the last channel number selected. Selection of a non-specular parameter causes a return to the channel selected immediately before specular was selected. Any key selected which is associated with *n*-stable (i) puts *n*-stables (ii) and (iv) in the null state. Selection of 'specular' forces *n*-stable (iii) to the attenuation state.

The channel/parameter combination is always valid and is indicated by the appropriate keys being illuminated. Each parameter value is entered via a decimal (0–9) keyboard which assembles the value as a 2½-digit signed b.c.d. quantity. This quantity is displayed on a 2½-digit seven-segment gas discharge indicator. As it is keyed in, a check is made that the value entered so far is within range for the parameter selected. If not, the display is automatically cleared so that a fresh quantity may be immediately keyed in. When this has been achieved, the value may be entered to the parameter store r.a.m. The 'enter' key also has the effect of clearing down the parameter value displayed in the lower indicator and returning the sign to '+'.

6.2 Computer Entry of Data

When computer originating data are to be entered, they are received by the simulator as a fixed format block of 21 eight-bit signed binary words: 8 attenuation coefficients for the ground and sky wave channels and 3 noise sources, IMP-MIT, and Doppler, Rayleigh fade rates and delay coefficients for the sky wave channels. To receive external data, the simulator is first put into an Auto mode which makes the panel inoperative (except for return to the Manual mode). Furthermore, Stop and Start signals are also derived externally when the system is in Auto.

6.3 Parameter Storage

The 21 parameters are stored in sign and modulus b.c.d. in r.a.m.s, as received. This is convenient, for binary to b.c.d. conversion is unnecessary when the r.a.m. contents have to be displayed. This latter occurs automatically as a result of data entry or merely selection of any channel/parameter combination. The store display is, like the key parameter value display, a 2½-digit gas discharge indicator. However, in the case of the store display, IMP-MIT and Rayleigh fade rates are displayed as absolute rather than encoded values. (Suitable decoders exist on the r.a.m. data output lines for this purpose.)

6.4 H.f. Signal Entry

The incoming signal to be processed may take the form of an analogue waveform (100 kHz carrier modulated at 10 kHz bandwidth and to be sampled at 80 kHz) or an 80 kiloword, 8 bits/word data stream. If it is analogue, the waveform is sampled with a narrow window (~50 ns) sample-hold amplifier, analogue-to-digital converted and stored in a buffer register ready for writing into the m.o.s.-r.a.m. delay store. If the data are received digitally, they are merely logged in the buffer register. The a.d.c. is required to convert in less than 12·5 μs and in practice operates in around 10 μs.

No anti-aliasing filters are provided at the input of the simulator because of the incoming signal bandwidth specification.

The signal samples are mapped in reverse order contiguous locations in the delay m.o.s.-r.a.m. (which has 1024 eight bit locations). Wrap-around therefore occurs once per 12·8 ms (Fig. 5). The m.o.s.-r.a.m. is read 8 times in each 12·5 μs interval to give 4 pairs of contiguously addressed samples—1 pair of each sky wave channel. As the two members of a pair are only 1 location apart, their phase difference is $\pi/2$ radians based on a down-converted carrier of 20 kHz derived from 80 kHz sampling. The pair is then used in the angle interpolation system described in Section 3.5. The m.o.s.-r.a.m.

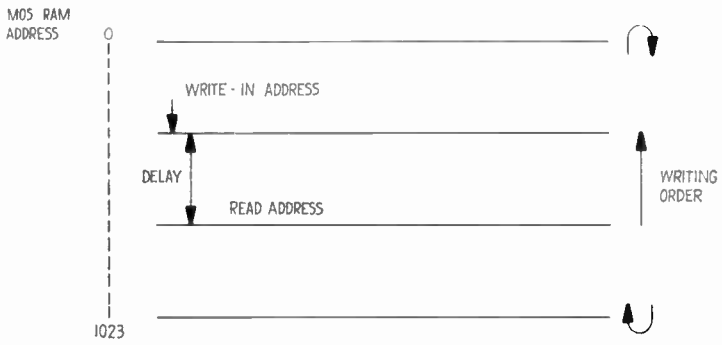

Fig. 5. Delay m.o.s. r.a.m. addressing.

address for the pair is $(a+b)$ modulo-1024 and $(a+b+1)$ modulo-1024 where a is the current m.o.s.-r.a.m. write address (stored in a down counter) and b is the channel delay coefficient (obtained from the delay location of the parameter r.a.m.). (For each unit of delay, i.e. 100 μs, b is incremented by 8, i.e. the m.o.s.-r.a.m. address is advanced by 8 units.)

The specular channel has no delay associated with it (the ground wave arrival instant is taken to be the time origin for the simulation). Thus each sample of the incoming analogue waveform is used directly it arrives as well as being written in the m.o.s.-r.a.m.

6.5 Doppler Shifting

Doppler shifts could have been simulated by advancing or retarding the delay value for a channel at a certain steady rate but this is impractical as the delay required would become excessively large (positive or negative) within a very short time. The method adopted is to advance or retard the delay in a 'marking time' mode (Fig. 6). In this, the delay is increased steadily by interpolation between m.o.s.-r.a.m. locations n and $n+1$; returned to n, then $n+1$. The sine and cosine values (of α) are obtained from a sine table r.o.m., the address for which is obtained from a counter whose count rate and direction is determined by the desired Doppler frequency. (This r.o.m. address may be further modified if Rayleigh phase components are also to be expressed.) If the Doppler shift is 1 Hz, the phase advance/retard required of the carrier is 2π or 4 sample intervals/second. The sine r.o.m. has 1 quadrant ($\pi/2$) divided into 128 parts (approx. 0·71 degrees), and sampling occurs at 80 kHz. Thus the sine r.o.m. address needs to be changed by 1 every $80\,000/512 \approx 156$ samples. At the maximum Doppler rate of 30 Hz, the sine table address is changed once per 156/30 samples (Fig. 7). Both sine and cosine Doppler weighting coefficients are obtained from the same r.o.m. by using complementary addressing. In order to obtain rolling of the phase over 2π radians, whilst retaining use of the same pair of contiguous samples (which are only separated by $\pi/2$), a combination of complementary addressing and the annexing of a suitable sign bit to the sine table output is employed. Thus, for cos 210°, sine 60°

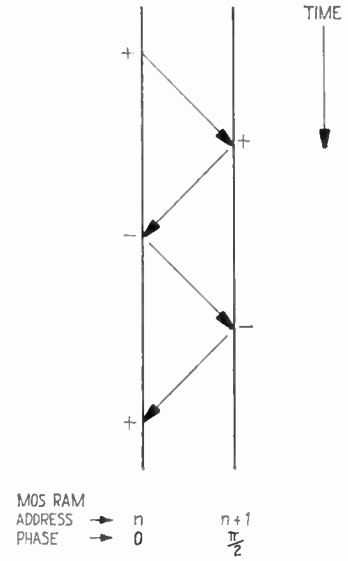

Fig. 6. Doppler rolling mechanism.

is looked up and a sign (negative) annexed to the r.o.m. output.

The resulting 9-bit word is then in binary (sign and modulus) notation.

6.6 Noise Sources

'Noise sources' in this section refer to the G.w.n. and impulsive noise generators, Rayleigh amplitude and phase coefficient generators. They are obtained from a single 31st order m-sequence generator for which the polynomial $1+x^3+x^{31}$ is used. The generator is clocked 32 times at 10 MHz once per 12·5 μs. It therefore has a period of about 7 hours.

Five functions of a suitable distribution are then derived from combinations of bits in the generator at each 12·5 μs iteration.

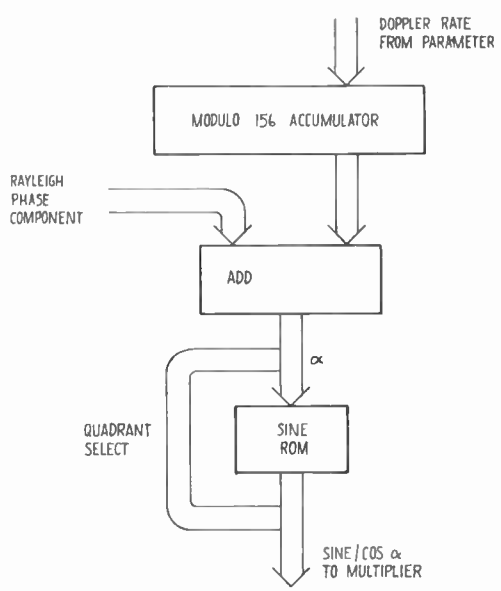

Fig. 7. Doppler frequency to 'α' weighting coefficients translation.

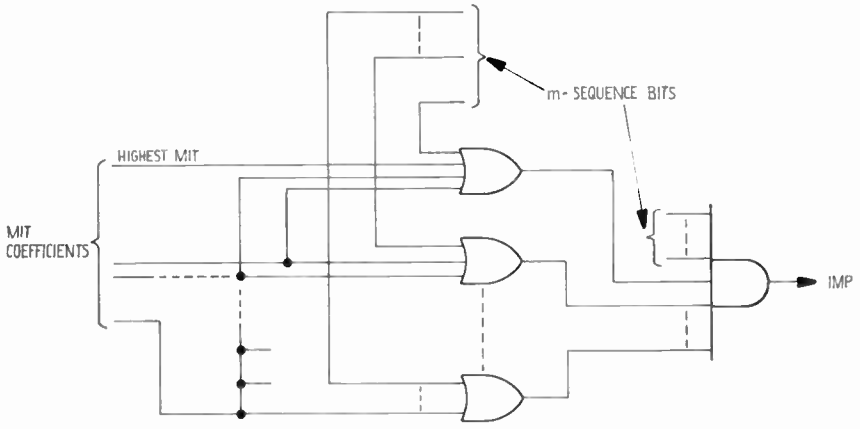

Fig. 8. Impulsive noise generator.

6.6.1 *Impulsive noise*

There is a single source of impulsive noise for the simulator which is generated as 200 μs (16 iterations) wide pulses of constant amplitude. The noise can then be subjected to up to 40 dB of attenuation using the multiplier. The time of occurrence of each noise impulse is determined by taking a group of m-sequence bits (x^n) from the polynomial and passing them through an AND gate. In order to vary the mean inter-pulse arrival time, some of the bits are ORed with the MIT coefficient so as to effectively disable them, causing a greater impulse rate to be effected (Fig. 8). The m-sequence generator is ideally suited for impulsive noise generation as such noise is assumed to have a distribution of impulse inter-arrival times which follows a negative exponential law. (Any bit of an m-sequence generator has the same property.)

The output from this noise generator is then passed to the multiplicand input of the multiplier as a unit signal.

6.6.2 *Gaussian white noise (G.w.n.)*

There is a single source of G.w.n. which is also derived from the 31-bit m-sequence generator. The group of bits used is split into two groups, one for the most significant portion of the noise signal which follows a roughly Gaussian distribution and a second group which is left untreated and merely used to provide an even distribution of signal amplitudes between the more coarsely quantized levels. The coarsely quantized Gaussian levels are obtained by taking a group of 8 m-sequence terms, using one for an otherwise untreated sign bit and the remaining 7 to create the desired distribution. Each of the 7 bits is passed to an adder tree to determine the weight of the bits (0–7) and then into a combinational logic circuit which transforms this weight into levels according to Table 2. This transformation logic is also used to convert what

Table 2
G.w.n. distribution generator

Input weight (plus sign)	Output level	2's Complement code
7	3	011
6	2	010
5	1	001
4	0	000
3	0	000
2	1	001
1	2	010
0	3	011
−0	3	101
−1	2	110
−2	1	111
−3	0	000
−4	0	000
−5	1	111
−6	2	110
−7	3	101

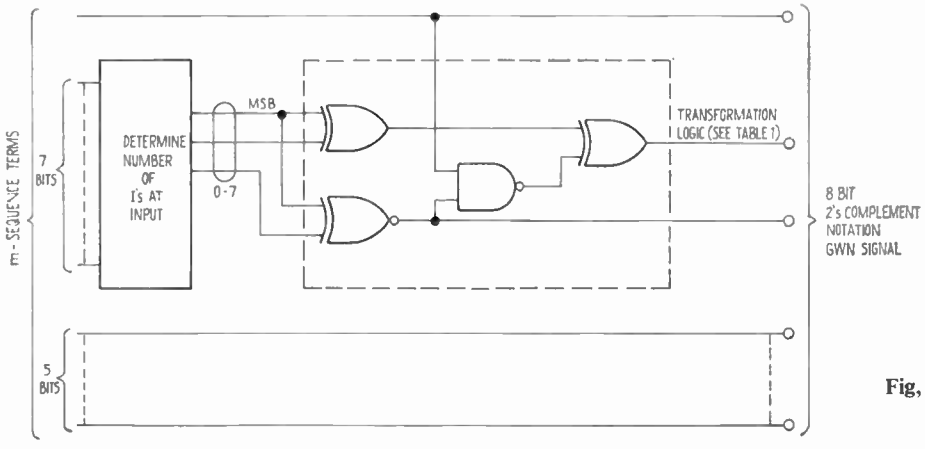

Fig. 9. Gaussian white noise generator.

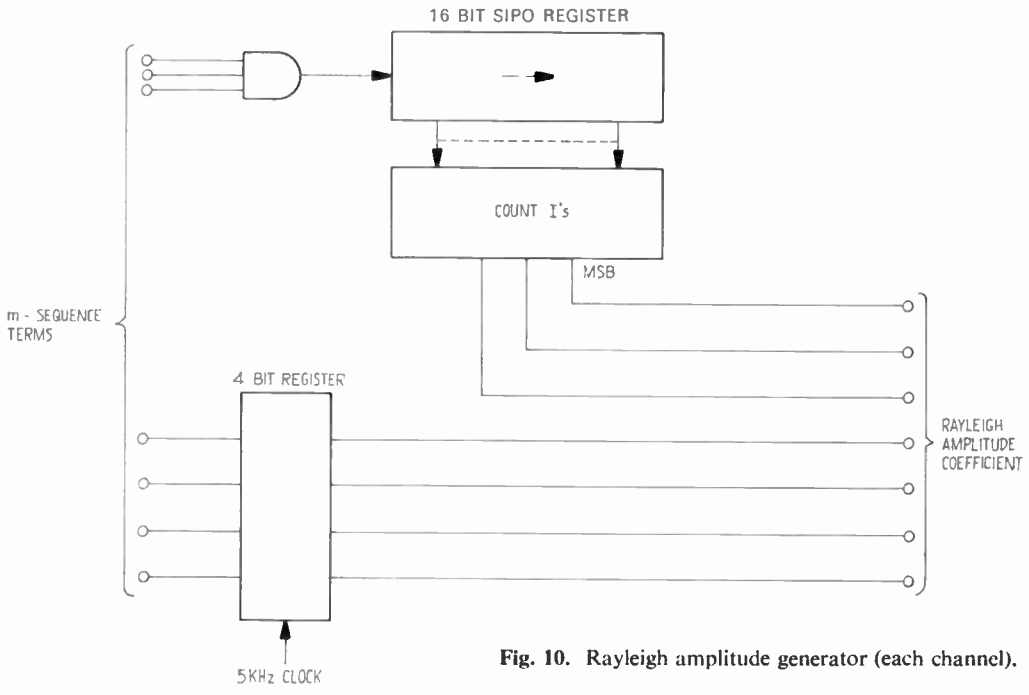

Fig. 10. Rayleigh amplitude generator (each channel).

would otherwise be sign and modulus information into 2's complement notation, suitable for the multiplier's multiplicand port. The multiplier is used to append the appropriate attenuation factor (Fig. 9).

6.6.3 *Rayleigh amplitude*[3]

Four signals are generated to modulate each of the four sky-wave channels according to a Rayleigh distribution. Three m-sequence terms are obtained for each of the 4 channels. These bits are passed through a 3-input AND gate to give an 8-fold division in the occurrence of 1's from the m-sequence generator and then through a 16-bit shift register whose content of 1's at any time is used as a coarse amplitude (modulation) coefficient for the sky-wave channel in question. On average, the shift register has only two logic 1's in it but the distribution will roughly follow a law of the form $x \,.\, \exp(-x)$. The shift register contents are monitored in a saturable counter whose contents are limited to 7 quanta. The counters contents (3 bits) are then used as the most significant portion of the Rayleigh instantaneous amplitude coefficient. For each channel, a group of 4 m-sequence terms are then used to provide a less significant 'fill-in' of uniform distribution. These are only updated at a low rate (around 5 kHz) so that the band-pass filter on the simulator's output does not cause 'dips' in the Rayleigh distribution between the coarse quantization points (Fig. 10).

6.6.4 *Rayleigh phase 'walk'*

Four channels of this phenomenon are provided, one for each sky wave. It is generated in the manner of a pseudo-random rate limited walk using terms from the m-sequence generator to determine walk 'direction' ($\Delta\phi$). ϕ is used to drive the trigonometric r.o.m. to provide $\sin\alpha$ and $\text{cosine}\,\alpha$, in conjunction with the Doppler generator. The latter provides a steady 'rolling' of α between 0 and 2π radians whilst the former superimposes an additional Markovian walk. For each channel, a single m-sequence term provides the walk direction at any time and a suitable sub-multiple of the 80 kHz system clock provides rate limitation (Fig. 11).

6.7 Arithmetic

The arithmetic unit for the h.f. simulator has only multiplication and two levels of accumulation to perform. However, a complete process has to take place within 12·5 μs (including m.o.s.-r.a.m.) cycles. The arithmetic processes are:

(i) Weighting of 4 pairs of m.o.s.-r.a.m. words with sine and cosine components and multiplication by

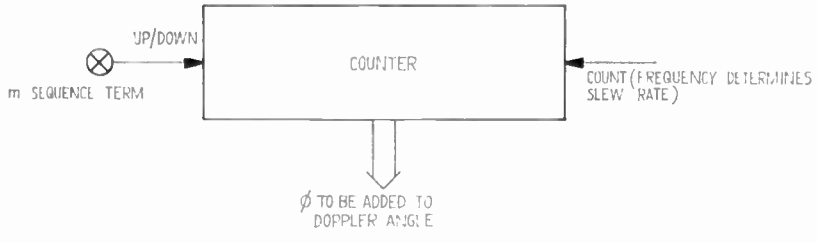

Fig. 11. Rayleigh phase generator.

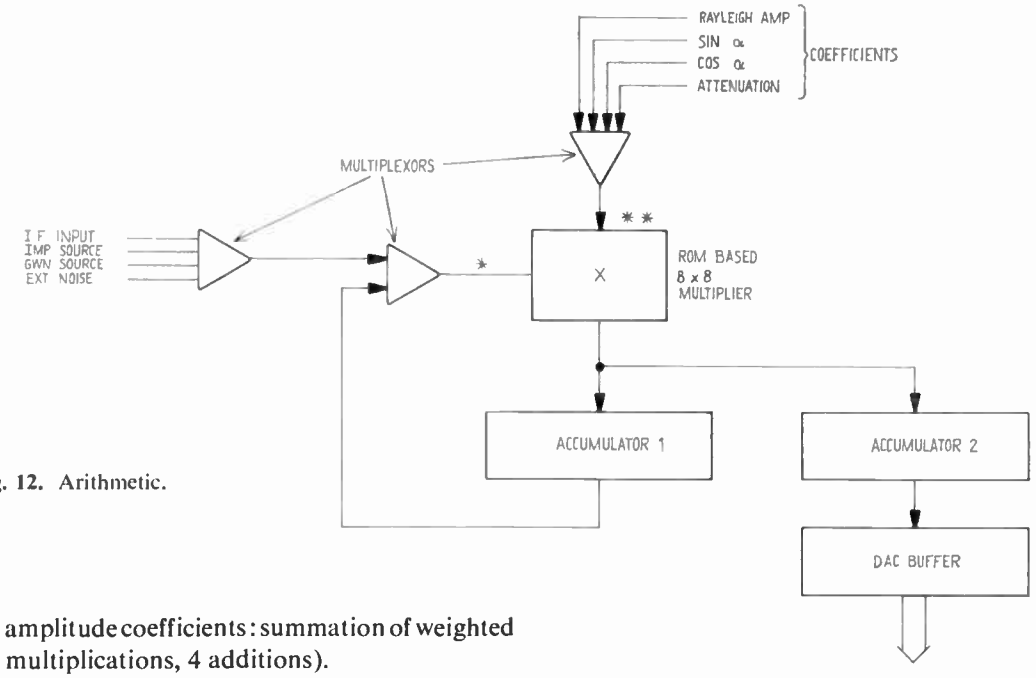

Fig. 12. Arithmetic.

Rayleigh amplitude coefficients: summation of weighted pairs (12 multiplications, 4 additions).

(ii) Weighting of weighted pairs, noise sources and the specular signal with attenuation coefficients (8 multiplications, 8 additions) (Fig. 12).

Accumulator 1 collects the trigonometrically weighted samples for each channel prior to the application of the Rayleigh amplitude control and attenuation coefficients; accumulator 2 collects the finally weighted signals from the 5 channels and the noise sources. Signals enter the multiplier at port * and are in 2's complement notation. Multiplier values enter at ** and are in sign and modulus form. The multiplier output is in 2's complement notation so that it is suitable for both (i) re-entry to the multiplier at input port * and (ii) and for a conventionally signed accumulator.

As 20 multiplications have to be performed in about 4 μs, a purely combinational design, based on r.o.m.s, is used.[2] Although 8-bit operands are used, only an 8-bit product is derived because of the uncertainty associated with each operand. Treating each operand (x, y) as a signed fraction of range ± 1 in steps of 2^{-7}, then the uncertainty of each operand is $\pm 2^{-8}$ (at least). Thus the product $x.y$ has an uncertainty of about $2^{-8}(x+y)$. If x and y assume their maximum magnitudes and the uncertainties are assumed to aggregate, the product uncertainty becomes $\sim \pm 2^{-7}$.

The accumulators are conventional adder/register pairs but use multi-bit adders with internal carry look-ahead to improve speed. Accumulator 2 contains the final result after all the arithmetic operations have been carried out.

6.8 Output

The digital results can be presented, *per se*, to any 8-bit (80 kiloword/second) receiver or, more often, passed

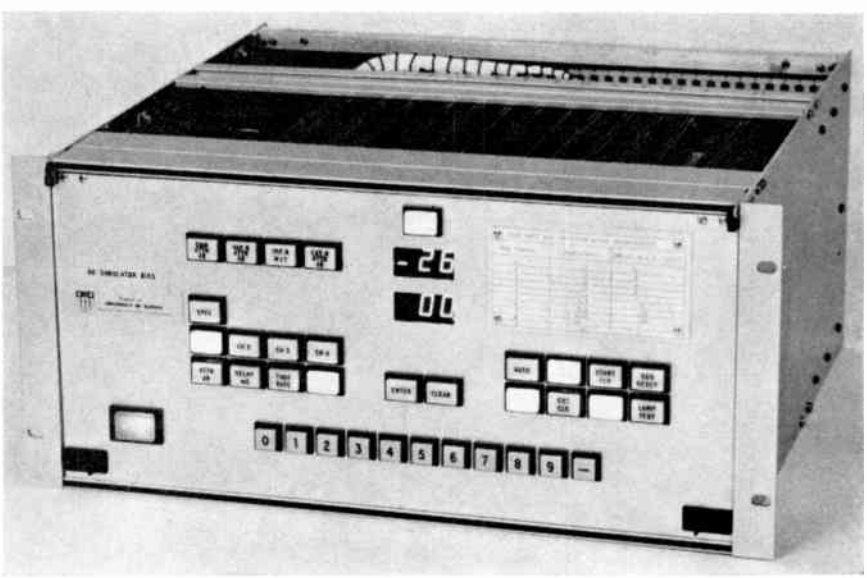

Fig. 13. Rack mounting version of H.F. Multipath Propagation Simulator.

through a digital-to-analogue convertor, sample-hold amplifier (to remove glitches, etc.) and a 100 kHz fourth-order Butterworth filter for presentation in band-limited analogue form.

6.9 Construction and Power Supply

The construction follows conventional practice using vertically mounted cards in a card frame. However, the amount of power required, around 80 W, has required careful choice and placement of the power supply units. Heat dissipation is greatly reduced by the use of a switching regulator for the main logic supply. The complete prototype instrument is shown in Fig. 13.

7 Conclusion

The h.f. propagation simulator described in this paper is currently undergoing trials at the Admiralty Surface Weapons Establishment and all the design criteria have been verified except for the nature of the correlation requirement between the Rayleigh amplitude and phase noise generators. This point is being studied in the initial evaluation programme, and, if required, any necessary minor modifications to the Rayleigh noise sources can be carried out.

Field trials have suggested that the digitally derived models of Gaussian noise and Rayleigh fade and phase phenomena correspond well with those experienced in ionospheric propagation. A mathematical treatment of these models is to be the subject of a later paper.

8 Acknowledgments

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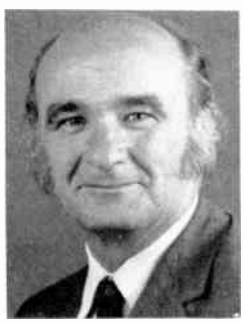
The Authors



Wallace Matley is a graduate of London University and the first eleven years of his professional career were spent in the Royal Naval Scientific Service on all aspects of radar R & D from systems research to post design development. From 1954 to 1956 he was with the Australian Department of Supply designing and developing rocket range instrumentation. He returned to the RNSS in 1956 and for the next five years worked on microwave aerial research, missile system command and display development. From 1961 to 1964 he was Chief Engineer at the Royal Observatory, Edinburgh, implementing the application of electronics to astronomy, and in 1964 he went to the Government Communication Headquarters to do communication system research. Since 1969 he has been a Senior Lecturer and Leader of the Industrial Electronics Research Group in the Department of Electronic and Electrical Engineering, University of Surrey.

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Analysis of insertion loss repeatability of coaxial connectors

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and

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Based on a paper presented at the IMEKO VII Conference held in London on 10th to 14th May 1976

SUMMARY

The repeatability of insertion loss of the most commonly used coaxial connector pairs was tested between 100 MHz and 12 GHz. The resolution of the measurements was better than 0·0001 dB. With carefully performed connections the repeatability expressed in standard deviation varied between 0·0002 and 0·002 dB. These values are some 2–3 times smaller than those published by Bergfried and Fisher.[1] The method described is particularly suitable for measuring the attenuation of small-loss elements such as adapters, air-spaced lines, etc.

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Nomenclature

σ standard deviation of the insertion loss variation of the connector pair, dB.

σ_Γ standard deviation of the reflection factor variation of the connector pair (ratio).

$|\Gamma_0|$ mean of the absolute value of the connector pair reflection factor.

1 Introduction

During the last few years considerable work has been done to improve the characteristics of r.f. and microwave instrumentation. This has increased interest in coaxial connectors as no measuring system can omit them.

Coaxial connectors are specified by performance characteristics such as v.s.w.r., insertion loss, contact resistance, r.f. leakage, electrical length, as well as the repeatability of these parameters. Repeatability is the permanency of the given parameter during the connect–disconnect cycles. Among the parameters mentioned, insertion loss has a particular importance, since its repeatability includes in practice the effects of all the other parameters.

The difficulty in measuring the insertion loss repeatability of precision coaxial connectors results from the fact that very small variations of attenuation, often of the order of 10^{-4}, must be detected. This needs a measuring system of appropriate stability and resolution capability. To meet these requirements an improved version of the a.f. substitution method described by Korewick and Pakay[2,3] was used for the present tests. The most widely applied precision and semi-precision coaxial connectors were tested between 100 MHz and 12 GHz. The repeatability of the insertion loss was expressed in terms of the standard deviation and system drift was excluded from the results by applying linear correction. From the results conclusions can be drawn concerning the choice of suitable connector types and their fields of application.

2 Measurement Method

The block diagram of the dual-channel a.f. substitution measurement system is shown in Fig. 1. The given method is specially capable for the precise measurement of small attenuations. The dual channel system assured a compression of the r.f. signal source level instability by a factor of 30–40 depending of the symmetry of the barretter demodulators. The 7-digit inductive ratio transformer used as a.f. reference attenuator was capable of indicating the small changes of attenuation of the order of 10^{-4}–10^{-5} dB. For detector a phase-sensitive device was used. Its reference signal was obtained by detecting the square wave modulated r.f. signal. By means of the indication of the signals below noise level the phase-sensitive detector made possible the extension of the dynamic range of the measurement by approximately 10 dB in comparison with that of the usual narrow-band detector or an equivalent one-order extension of the resolution. With 100 μW r.f. input power the a.f. output voltage of the applied barretter

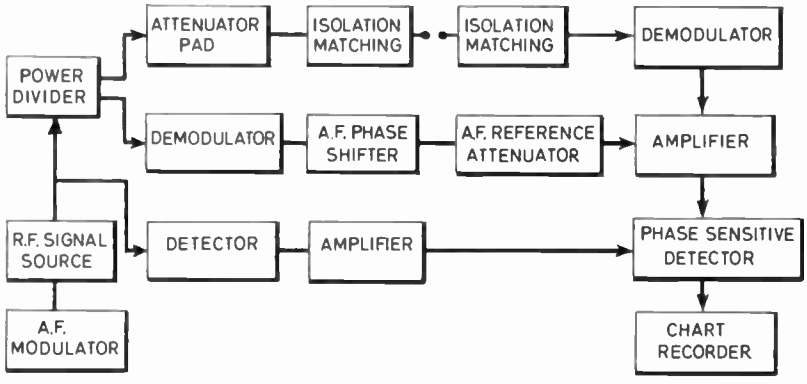

Fig. 1. Block diagram of the insertion loss repeatability measurement equipment.

mounts was some 2 mV. In this case a change of level of 30–40 nV at the ratio transformer corresponded to a change of attenuation of $\sim 10^{-4}$ dB. The sensitivity of the phase-sensitive detector permitted a resolution better than 10^{-4} dB. However it would not have been reasonable as the short-time stability of that simple system without any particular concern for r.f. source level control of thermostatic facilities is of the order of 10^{-4} dB. For better evaluation the results were displayed on a chart recorder connected to the output of the phase-sensitive detector (Fig. 2). The generator and detector sides were matched at the insertion point for v.s.w.r. < 1·01 by means of coaxial tuners. The matching elements gave some thermal isolation between the insertion point and the test barretter as well which was needed to reduce heat transfer from operator's hands.

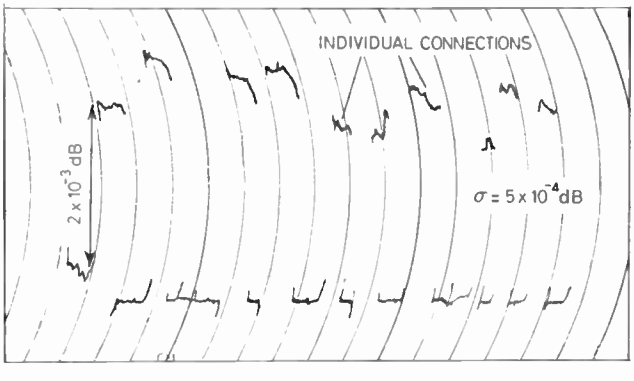

Fig. 2. Typical insertion loss repeatability chart for SMA connector pair at 10 GHz.

In assembling the measurement system care was taken to eliminate the parasitic signals, e.g. earth loops.

The measurements were performed under normal laboratory conditions with a temperature stability $\pm 0{\cdot}5°C$.

3 Measurement Technique

The intention was to test the repeatability with carefully performed connections, made under usual working conditions.

During the tests it was found that the quality of the connections depends on two factors of mainly mechanical character; namely, tightening torque and transverse alignment force.

Therefore the connectors to be tested were mounted vertically to minimize the transverse alignment force necessary for proper connection. However to get a better approach to real life conditions the connectors were tightened by hand though in a careful way. Average torque for 7 mm connectors was about 1 Nm. The importance of the alignment of the connectors is demonstrated by the 10 GHz measurements performed on the same connectors in both vertical and horizontal arrangements. (Table 1.)

Table 1. The results of insertion loss repeatability measurements

	Standard deviation (dB)					
	100 MHz	1 GHz	6 GHz	10 GHz	10 GHz†	12 GHz
APC 7	0·0002	0·0005	0·0009	0·0007	0·0009	0·0008
SMA Sub-miniature, semi-precision (Amphenol)	0·0003	0·0004	0·0004	0·0006	0·0008	0·0010
N stainless steel (MIL C39012)	0·0002	0·0006	0·0009	0·0010	0·0014	0·0014
Dezifix A	0·0003	0·0012	0·0014	0·0020	0·0021	0·0019‡
GR 900	0·0003	0·0003	0·0002			
GR 874	0·0002	0·0009				
UHF	0·0002	0·0009				
Dezifix B	0·0004	0·0009				

† Horizontal arrangement. ‡ Connector Prezifix A.

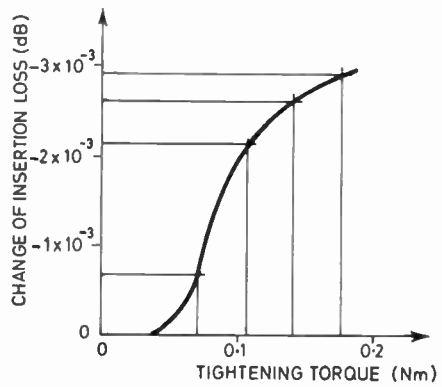

Fig. 3. Insertion loss versus tightening torque for SMA connector pair at 10 GHz.

A wrench (with about 0·2 Nm torque) was used only for SMA connectors since it is customarily used in practice. The insertion loss versus tightening force characteristics of these connector pairs were also measured (Fig. 3).

4 The Results of the Measurements

The results of insertion loss repeatability tests versus frequency are presented in Fig. 4(a–f) and in Table 1.

Three or four specimens of each connector types were tested. The average number of measurements varied between 20 and 30 and experience showed that 20 was the number of measurements where the standard deviation approached the value characteristic of the given connector pair. Since the standard deviations for the individual connectors and for repeated series of measurements on the same connectors were not necessarily identical the boundaries belonging to the maximum and minimum σ values are shown at the diagrams. In Table 1 and Fig. 4(f) the σ represents a mean of the repeated series of measurements and it can therefore be considered as an average standard deviation characteristic of the type of connector pair at the given frequency.

At 100 MHz and 1 GHz the tests included those semi-precision coaxial connectors as well at which the measurements at higher frequencies were not reasonable. The results of the 10 GHz measurements performed in horizontal arrangement are presented separately.

Table 2 summarizes the results of the insertion loss measurements of some commonly used coaxial adapter pairs. Since only one specimen of each type was tested the results are of informative nature. The systematic error of the measurement estimated from the v.s.w.r. at the insertion point and that of the item to be measured was $<0{\cdot}003$ dB with the exception of the u.h.f. adapter pair at which it was well over $\pm 0{\cdot}01$ dB at 1 GHz. The

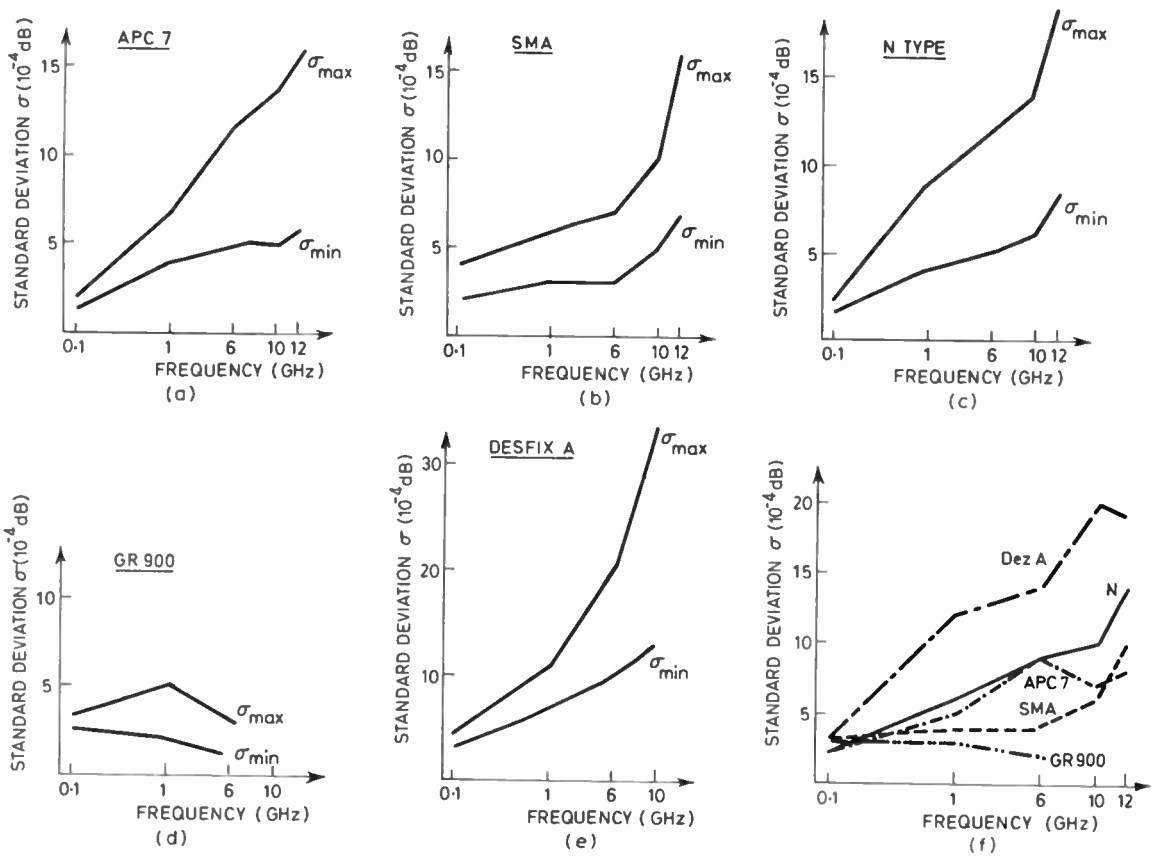

Fig. 4. Insertion loss repeatability versus frequency for various types of connector.
(a) APC 7 connectors; (b) SMA connectors; (c) N type connectors; (d) GR 900 connectors; (e) Dezifix A connectors; (f) Mean of the plots for each of the five types of coaxial connector.

measurements were performed on adapters between the connector listed and N type connectors (100 MHz and 1 GHz) and APC 7 connectors (6 GHz and 10 GHz). The adapter pairs were formed with the connectors listed in Table 2 interconnected, so that male and female N connectors (100 MHz and 1 GHz) or APC 7 connectors (6 GHz and 10 GHz) appeared at each end of the assembly for testing.

5 Evaluation of the Results

To estimate the confidence of the data one must determine the error sources of the a.f. substitution system. The errors are partly of random and partly of systematic character[3]:

(a) reference attenuator errors
(b) errors due to demodulator and the associated circuitry (primarily the barretter non-linearity error)
(c) mismatch error
(d) parasitic signals
(e) noise-limited detector sensitivity
(f) system instability.

The errors (a) to (e) can be neglected partly because very small changes in attenuation had to be measured and partly because of reasons mentioned above. The accuracy of the results obtained was determined ultimately by the overall instability of the measuring system resulting from the following principal components:

power variations of the r.f. signal source (secondary effect because of non-identical characteristics of the test and reference barretters);
temperature sensitivity of the r.f. elements first of all of the barretter mounts;
mechanical instability of the r.f. circuitry (this means to what degree the associated r.f. elements are resistant to the small but unavoidable deforming forces during the connection cycles).

The above instabilities were each of the order of 10^{-4} dB for a short time. The slow drift of the measurement system was $<0{\cdot}0006$ dB over the 10 minutes time taken for 20 measurements.

Table 2
Insertion loss of adapter pairs

	Insertion loss (dB)			
	100 MHz	1 GHz	6 GHz	10 GHz
APC 7	0·008	0·040		0·113†
SMA	0·007	0·024	0·069	0·097
N stainless steel	0·004	0·011	0·064	0·082
Dezifix A	0·005	0·017		
GR 900	0·005	0·021	0·054†	
GR 874	0·004	0·015		
UHF	0·028	0·26		
Dezifix B	0·003	0·017		

† Between N type connectors.

The slow drift can be eliminated from the results by a simple first-order correction because it is equivalent to a certain reduction of the basic system instability. In this way the typical standard deviation of the system instability calculated from the one-minute samples on chart recording was $\sigma \sim 10^{-4}$ dB for a 10-minute period.

The standard deviation of the connection repeatability was evaluated in a similar way by using linear correction. The application of the more complicated second-order correction would not have been reasonable.

Figure 2 gives an example for the recorded results of some 10 cycles in a test series. Here the slow drift being very small, the standard deviation calculated with and without correction was nearly identical.

At 10 GHz, as mentioned previously, repeatability measurements were performed in both vertical and horizontal arrangements. The vertical arrangement mounted on a stand made easier the axial alignment of the connector pairs to be measured (Fig. 5). The deviation between the results of the two kinds of measurements is an index of how definitely the axial alignment is assured by the coupling mechanism itself at the given type of connectors (Table 1).

The insertion loss versus tightening torque relationship was examined for SMA connector pairs at 10 GHz. The results in Fig. 3 indicate that to get a good reproducibility it is necessary to use a torque $>0{\cdot}2$ Nm, i.e. where the gradient of the curve significantly decreases. The decrease in insertion loss of the SMA connector pair with increasing tightening torque is related to that insertion loss value corresponding to 0·035 Nm torque at reference 0 dB.

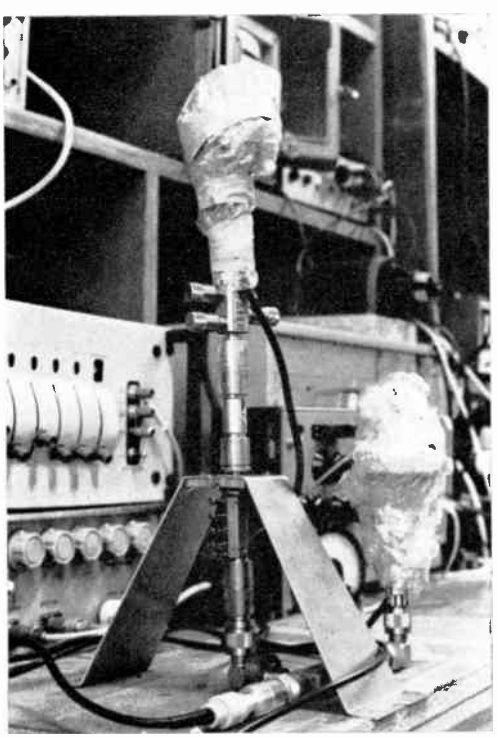

Fig. 5. The vertical system for repeatability measurements.

Because of the small physical dimensions of the connector, however, good reproducibility could be ensured only by torque wrench.

The standard deviation values obtained at the 100 MHz reproducibility measurements fell nearest to the system instability level, representing a limit for the applicability of the method.

The reasons for the variation of insertion loss of connector pairs are associated with both the variation of dissipation and reflexion of energy at the junction point. The permitted change in contact resistance can appreciably influence the dissipation loss, whereas the effect of a possible change in r.f. leakage is quite negligible for precision connector pairs. The variation of the reflection coefficient at the junction can also have a considerable effect on the reflection loss and in this way alter the insertion loss.

This relationship can be expressed in explicit form provided the other effects are neglected and the system reflection at the insertion point is small compared to the reflection of the connector pair to be tested. The approximate relation in this case is as follows:

$$\sigma \approx 8{\cdot}7\,|\Gamma_0|\,\sigma_r.$$

If the system reflection cannot be neglected full phase information becomes necessary to describe the phenomenon.

6 Conclusions

According to the results obtained under normal conditions but with carefully performed connections, the insertion loss repeatability of the precision coaxial connector pairs ranged between 2×10^{-4} and 20×10^{-4} dB up to 12 GHz. These values seem to determine the practical limits of accuracy for insertion loss measurements of coaxial attenuators and other components.

In the frequency range of the present tests the differences in repeatability between the various types of precision and semi-precision connector pairs did not surpass one order of magnitude. However the sharp degradation of repeatability above 10 GHz indicates that in the vicinity of the upper frequency limits of the connectors considerable differences are to be expected.

With the applied method it was possible to examine how variations of some mechanical parameters influence the quality of the connections. In that respect the connector insertion loss versus tightening torque and loss repeatability versus connector positioning relationships were tested.

Concerning the better repeatability of the coaxial connector pairs compared with those obtained by Bergfried and Fischer this is thought to be due partly to the improvement of the measurement apparatus regarding its stability and sensitivity, and partly to the carefully performed connections.

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Letters

From: **H. M. Merklinger**, Ph.D.

J. M. Hovem, Dr.Ing.

R. Benjamin, D.Sc., Ph.D., C.Eng., F.I.E.E., F.I.E.R.E.

Non-linear Acoustics

The paper 'A new sub-bottom profiling sonar using a non-linear sound source'[1] accurately presents one of the promising applications of non-linear acoustics. The references cited in the paper fail, however, to emphasize the role of British Science in this development.

Until the 1965 publications of Tucker[2] and Berktay[3] from the University of Birmingham, the phenomenon reported by Westervelt[4] was largely of academic interest. The recognition that this non-linear effect was of practical utility was a very significant event. The methods by which the effect could be exploited were set down by Berktay.[3] With only one exception, the acoustic theory reported by Pettersen *et al.*[1] is contained in the papers of Westervelt,[4] Berktay[3] and Merklinger.[5] References 7–12 cited by Pettersen *et al.* consist largely of developing and polishing these original ideas.

The authors are to be commended for engineering a sophisticated instrument, but I feel their references might lead readers to believe that the acoustic principles involved were probably developed entirely within the United States of America. I think it would be true to say that the original invention was American, but that the subsequent practical development was largely British.

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27th May 1977

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1 Pettersen, P., Hovem, J. M., Lovik, A. and Knudsen, T., *The Radio and Electronic Engineer*, **47**, No. 3, pp. 105–11, March 1977.

2 Tucker, D. G., 'The exploitation of non-linearity in underwater acoustics', *J. Sound Vib.*, **2**, pp. 429–34, 1965.

3 Berktay, H. O., 'Possible exploitation of non-linear acoustics in underwater transmitting applications', *J. Sound Vib.*, **2**, pp. 435–61, 1965.

4 Westervelt, P. J., 'Parametric acoustic array', *J. Acoust. Soc. Am.*, **35**, pp. 535–7, 1963 (Ref. 6 of paper by Pettersen *et al.*).

5 Merklinger, H. M., 'Of finite amplitude plane waves and of endfire arrays', Proc. 3rd Symposium on Nonlinear Acoustics, pp. 114–25, University of Birmingham, 1st–2nd April 1971.

In reply to Dr Merklinger's letter we would like to point out that the purpose of our article was to describe the engineering and successful application of a new equipment. The design was based on previously documented research and we do not claim any originality in the acoustic theory. The references cited in our paper were those which had a direct influence on the design.

We recognize the significant role of British Science in the practical development of non-linear acoustics and agree that in a complete list, the references cited by Dr Merklinger should have been included.

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27th June 1977

The Physical Basis of Signal Theory

In Section 2 of my paper on 'The physical basis of signal theory,'* I have derived an indication of an information capacity of $BT\log_2(1+S/N)$ in *voltage* terms for a single, phase-coherent channel, and have extended this as twice that quantity for two phase-quadrature channels. This is indeed correct, if—as implied—the two quadrature channels have independent power sources, and if perfect phase reference signals are available for their independent phase-coherent detection. However, I failed to refer explicitly to the more common practical problem, and that normally treated in the literature, where the combined power available to the two quadrature channels is limited. For this case, the exact analogy to the simplified single-dimensional argument given in my paper is as follows.

A signal vector of peak amplitude S can define any point in a vector space of area πS^2. A noise vector of 'equivalent peak amplitude' N will subject the vector termination to an area ambiguity of πN^2. Hence the number of discrete states identifiable, in the presence of a signal, is the ratio S^2/N^2. In addition there is the single state which denotes 'no signal'. But the logarithm of the number of discrete states defines the corresponding number of 'bits' of information. Hence the information potential per unit cell on the frequency-time plane is then

$$I=\log_2(1+S^2/N^2)=\log_2(W_S/W_N),$$

where W_S and W_N are the relevant signal and noise powers.

In most practical applications $S\gg N$, and then the two formulations give substantially identical results. For $S/N\ll 1$, on the other hand, the revised formulation, above, is asymptotic to a constant total signal energy, for conveying a given amount of information. The implication here is that, at low S/N, further spreading of the signal energy in the time-bandwidth plane cannot add further to the information capacity, but its effect on signal detectability can always be reversed by coherent combination as shown in Section 1 of the paper.

The situation implied in Section 2 of the paper, i.e. totally independent phase-quadrature channels, is less likely to apply for $S/N\ll 1$. When it does apply, it requires the total signal energy to be inversely proportional to the time-bandwidth occupancy, for a given information capacity. Thus that formulation errs on the safe side, in assessing the penalty of reducing the time-bandwidth product, but may over-estimate the potential benefit of increasing it.

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24th June 1977

* *The Radio and Electronic Engineer*, **47**, No. 1/2, pp. 49–58, January/February 1977.

UDC 681.325.65

The design of easily tested circuits using mapping and spectral techniques

C. R. EDWARDS, B.Sc., Ph.D., M.I.E.E.E.*

SUMMARY

The results of a theoretical study of the application of mapping and spectral techniques to the design of digital circuits, with special emphasis on combinational circuits, are given.

The method has the great advantage that the derivation of circuit tests is an integral part of the circuit synthesis procedure. Other advantages of the method are that very elegant designs are produced which are compatible with all modern fabrication technologies and permit low-cost implementation. This technique is fundamentally different to conventional methods of deriving easily tested circuits.

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1 Introduction

With the development of modern complex digital circuit systems has come an increasing need for viable fault diagnosis. In the past fault diagnostics have traditionally been derived from the analysis of circuits, as a post-design exercise. In small systems this approach was adequate, if cumbersome. With the advent of more complex circuits it is necessary to consider the diagnosibility of circuits at the design stage. The reasons for this are twofold: firstly, circuits which are designed without considering diagnostics may prove to be impossible to test completely, and secondly the generation of the required testing sequences may be very tedious. There is a case, in fact, for designing circuits which, although not 'minimal' in the classic sense, employ extra modules and/or interconnections to aid diagnostics. The importance of diagnostics in modern systems is mirrored by the fact that in many cases the cost of testing a complex logic system exceeds the original system production costs. It is also true that in the case of very complex assemblies the probability that the hardware will function correctly after manufacture is almost zero. At present, there are no systematic techniques for designing digital circuits which are easy to test and maintain.[1]

It has been suggested that a design method is required which incorporates diagnosis criteria directly.[2] In this paper a preliminary study of such a method is described. The method is related to the Rademacher–Walsh transform[3,4] and also uses the properties of function symmetries.[5]

2 Some Current Techniques

Techniques for the design of circuits which are easy to test fall into two camps. The first method is to take existing designs and provide additional logic elements which may substantially increase the complexity of the circuits both in terms of the number of gates and also the number of interconnections,[6,7] but significantly reduce the number of tests required. The second approach is to design circuits which themselves are easily tested.[8,9]

These methods currently have quite severe drawbacks. In the first case the number of additional gates and interconnections may prove prohibitive and, perhaps more important, many more test nodes must be provided. The second method may be implemented by factorization of the Reed–Muller expansion which, although attractive because a very simple test set is required, suffers from large propagation delays, interconnection complexity and gate count.

The method presented below seeks to design circuits with minimal gate counts and interconnections and which are also easily tested by virtue of:

(i) Reducing the number of interconnections, often substantially, when compared to conventionally designed circuits. This in turn reduces the number of faulty ('stuck-at') nodes possible.

(ii) Reducing the fan-out, and thus the possibility of reconvergence paths within the circuit—a major cause

of test pattern generation problems.

(iii) Generating irredundant designs which eliminate 'fault-masking'.

In addition, the method has the great advantage that the derivation of tests is an integral part of the synthesis procedure. Additional properties of the method are that very elegant designs are generated which are compatible with modern circuit fabrication technologies and that, from computed results, delays and gate counts are smaller than in Reed–Muller derived designs.

3 The Method of Boolean Differences

One method of deriving test patterns for digital systems is that of the Boolean Difference.[10] The method is, in essence, very simple.

Suppose that it is required to test a node Q of a circuit to determine if it is 'stuck-at' logical 1. (This may be due to an electrical short-circuit between the node and supply or perhaps the malfunction of a gate connected to this node.) It will further be supposed that it is not possible to measure the state of this node directly. In practice this means that the fault must be determined by applying logical test patterns to the inputs of the circuit and observing resultant outputs. Specifically, for Q 'stuck-at-1' (s.a.1) we need an input test pattern which:

(a) Attempts to drive node Q to logical 0.

(b) If this node is not, in fact, driven to 0 then the circuit gives an incorrect output.

If logical 0 is replaced by logical 1 in the above then (a) and (b) test for Q 'stuck-at-0' (s.a.0).

In fact test (b) can be generalized, for both Q s.a.0 and Q s.a.1, by the Simple Boolean Difference with respect to node Q, namely the test set which generates different outputs for different states of Q.

This technique is illustrated by example, first for *input* nodes faulty and then (as above) for internal nodes. See also Ref. 10.

The simple Boolean difference of a function $f(X)$ with respect to one of its defining variables, x_j, is defined[10] as

$$\frac{\mathrm{d}f(X)}{\mathrm{d}x_j} = [f(x_1, \ldots, x_i, x_j, \ldots, x_n) \oplus f(x_1, \ldots, x_i, \bar{x}_j, \ldots, x_n)] \quad (1)$$

where $\oplus$ is the exclusive-OR operator.

Note the function $\mathrm{d}f(X)/\mathrm{d}x_j = 1$ is independent of x_j and defines the input states for which a change in state of x_j causes a change of output state. The set of tests for a fault on x_j is given by

$$\left\{x_j \cdot \frac{\mathrm{d}f(X)}{\mathrm{d}x_j}\right\} = 1, \quad \text{for } x_j \text{ stuck at 0} \quad (2)$$

and

$$\left\{\bar{x}_j \cdot \frac{\mathrm{d}f(X)}{\mathrm{d}x_j}\right\} = 1, \quad \text{for } x_j \text{ stuck at 1.} \quad (3)$$

Example

Figure 1 shows a very simple circuit which synthesizes

$$f(x_1, x_2, x_3) = [x_1 \,.\, x_2 \,.\, x_3].$$

Now

$$\frac{\mathrm{d}f(x_1, x_2, x_3)}{\mathrm{d}x_1} = [x_1 \,.\, x_2 \,.\, x_3 \oplus \bar{x}_1 \,.\, x_2 \,.\, x_3] \text{ from (1).}$$

To test for x_1 stuck at zero (s.a.0) we apply

$$\left\{x_1 \cdot \frac{\mathrm{d}f(x_1, x_2, x_3)}{\mathrm{d}x_1}\right\}, = [x_1 \,.\, (x_1 \,.\, x_2 \,.\, x_3 \oplus \bar{x}_1 \,.\, x_2 \,.\, x_3)]$$

$$= [x_1 \,.\, x_2 \,.\, x_3] = 1,$$

namely by setting $x_1 = 1$, $x_2 = 1$, $x_3 = 1$ and observing output Z it is possible to detect the fault x_1 s.a.0. (among others).

Fig. 1. Basic AND function $f(X) = x_1 x_2 x_3$. (Output node Z.)

Similarly to test for x_1 stuck at one (s.a.1), we apply

$$\left\{\bar{x}_1 \cdot \frac{\mathrm{d}f(x_1, x_2, x_3)}{\mathrm{d}x_1}\right\} = [\bar{x}_1 \,.\, x_2 \,.\, x_3] = 1,$$

and thus by setting $x_1 = 0$, $x_2 = 1$, $x_3 = 1$ and observing output Z it is possible to detect the fault x_1 s.a.1.

It can also be shown that the simple Boolean difference can be applied to internal circuit nodes. For example, Fig. 2 shows a circuit with internal node Q where $Q = [x_1 + x_2]$. The difference with respect to Q is:

$$\frac{\mathrm{d}f(Q, x_3)}{\mathrm{d}Q} = x_3, \quad (4)$$

and

$$\left\{Q(x_1, x_2) \cdot \frac{\mathrm{d}f(Q, x_3)}{\mathrm{d}Q}\right\} = 1, \quad \text{tests for } Q \text{ s.a.0} \quad (5)$$

whilst

$$\left\{\overline{Q(x_1, x_2)} \cdot \frac{\mathrm{d}f(Q, x_3)}{\mathrm{d}Q}\right\} = 1, \quad \text{tests for } Q \text{ s.a.1} \quad (6)$$

The double Boolean difference is defined as[10]

$$\frac{\mathrm{d}f(X)}{\mathrm{d}(x_i, x_j)} = [f(x_1, \ldots, x_i, x_j, \ldots, x_n) \oplus f(x_1, \ldots, \bar{x}_1, \bar{x}_j, \ldots, x_n)], \quad (7)$$

and enables tests to be determined for simultaneous faults on two nodes.

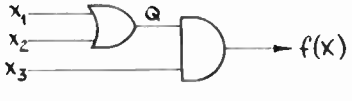


Fig. 2. Function $f(X) = (x_1 + x_2)x_3$.

It is not proposed to elaborate further on the theory of test generation under the Boolean difference, as this technique is well known, but to derive certain relationships between Boolean function symmetries and the Boolean difference.

From these relationships a synthesis method which is directly related to a test generation procedure will be developed.

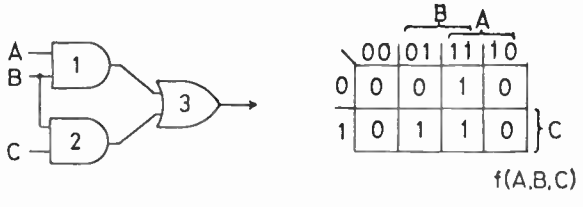
4 Introduction to Synthesis of Combinational Circuits under Function Symmetries

It is first noticed that the mathematical techniques employed below are essentially straightforward; no algorithms or heuristics are employed. At each synthesis level, however, a multiple choice of gate configuration may present itself. This choice may be resolved on the basis of the technology to be employed and optimization required. The heuristics required in making this choice are thus a product of the inherent flexibility of the method.

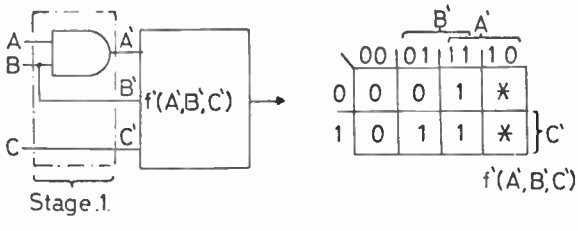
Because of the impossibility of detailing syntheses with all possible complex gate configurations only the simpler cases will be considered initially.

The exclusive-OR (NOR) function will be found to play a predominant role in designs generated by this method. This follows directly from the results and observations on the importance of the exclusive-OR function in the composition of Boolean functions given in Ref. 4. It is known that the ⊕ function may be efficiently implemented, both in the simple and complex form, in different technologies.[11,12] The ⊕ function is also a class of easily tested functions by virtue of the result

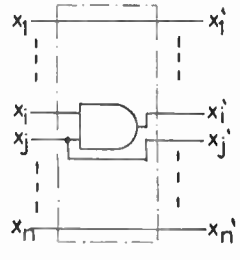
$$\frac{\mathrm{d}f(x_i \oplus x_j)}{x_i} = \frac{\mathrm{d}f(x_i \oplus x_j)}{x_j} = 1. \qquad (8)$$



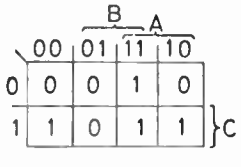
(a) Example with conventional synthesis.



(b) Interpretation in terms of symmetry.



(c) Generalized implementation of symmetry.



(d) Function exhibiting same symmetry.

Fig. 3

4.1 Many-one Mappings

By way of introduction, consider the very simple example shown in Fig. 3(a).

Suppose that this circuit is re-drawn as in Fig. 3(b), where the AND gate 1 of Fig. 3(a) has been treated as a synthesis stage. The general module (shown dotted) for this stage has inputs A, B, C, and outputs labelled A', B', C'. A function $f'(A', B', C')$ represents the remainder function to be synthesized. Now consider the relationship between A, B, C and A', B', C':

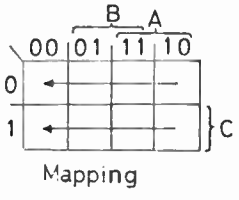
A	B	C	A'	B'	C'
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	0	0	0
1	0	1	0	0	1
1	1	0	1	1	0
1	1	1	1	1	1

Clearly

$(A, B, C) = (1, 0, 0)$ has mapped to $(A', B', C') = (0, 0, 0)$,

and

$(A, B, C) = (1, 0, 1)$ has mapped to $(A', B', C') = (0, 0, 1)$;



the remaining points map one-to-one and onto (they remain unchanged). (Fig. 3(b).)

Note that this mapping is allowed because in the given function $f(A, B, C)$

$$f(1, 0, 0) = f(0, 0, 0) \quad \text{and} \quad f(1, 0, 1) = f(0, 0, 1).$$

For the remainder function $f'(A', B', C')$ note that the input vector $A' = 1$, $B' = 0$ *cannot* occur. This n-space is thus given the unspecified value $*$ (don't care). Note that if the $*$ states are given the value 1 then $f'(A', B', C') = [A' + B' \,.\, C]$ which gives the solution shown in Fig. 3(a).

This result may be generalized as:

for a function $f(x_1, \ldots, x_i, x_j, \ldots, x_n)$ the module o[illegible]

Fig. 3(c) may be employed as a synthesis step if

$$f(x_1, \ldots, 1, 0, \ldots, x_n) = f(x_1, \ldots, 0, 0, \ldots, x_n).$$

This may be otherwise stated as:

Module 3(c) may be employed if the given function, in n-space $x_j = 0$, is symmetric in x_i (i.e. identical for both x_i and $\bar{x}_i$).

Note that in the above example both

$$f(1, 0, 0) = f(0, 0, 0) = 0$$

and

$$f(1, 0, 1) = f(0, 0, 1) = 0.$$

This is not generally the case; Fig. 3(d) shows another example valid under $A' = (A \,.\, B)$, $B' = B$ for which

$$f(1, 0, 0) = f(0, 0, 0) = 0$$

$$f(1, 0, 1) = f(0, 0, 1) = 1.$$

The example of Fig. 3(a), (b) illustrates the different philosophy between a conventional design method and the new method. In Fig. 3(a), AND gate 1 is conventionally associated with the factor $(A \,.\, B)$. Under the new method, however, this gate is associated with the symmetry properties of the function in n-space $\bar{B}$.

This approach can be interpreted in a more general way. If we can identify two areas in n-space which have identical patterns (sub-functions), and the areas are suitably close together, we can opt to synthesize only one such pattern and include a module to 'reflect' this pattern into the other area. In the case of Fig. 3(b) two identical 'patterns' can be identified in areas $(A, B) = (0, 0)$ and $(A, B) = (1, 0)$ so we opt to synthesize area (0, 0) and include a module to reflect this pattern into area (1, 0).

This synthesis approach may be repeated (with certain exceptions mentioned later) using various symmetry modules, until a remainder function corresponding to a simple connection is generated. The function is then completely synthesized.

It is of fundamental importance to note that, in the case shown in Fig. 3(b), (d), the mapping is allowed because the sub-function in area $(A, B) = (0, 0)$ is the same as that in area $(A, B) = (1, 0)$; it follows directly that there is no change in output for input $B = 0$ if input A is changed.

Thus for $f(A, B, C)$:

$$f(A, 0, C) \oplus f(\bar{A}, 0, C) = 0$$

but this may be expressed as

$$\frac{\mathrm{d}f(A, B, C)}{\mathrm{d}A} = 0 \quad \text{where} \quad B = 0.$$

The property of function symmetry is thus directly related to the Boolean difference. In addition the Boolean difference may be used to generate the required test parameters.

In practice it has been found that (working the other way about) the Boolean difference can be used to evaluate both the function symmetries and the associated tests for the module nodes used to implement such symmetries.

5 Function Symmetries and their Implementation

Some of the fundamental function symmetries are now discussed. For ease of presentation this discussion is restricted to examples of the characteristics of the various symmetries and their implementation. Interested readers should consult Appendix 3 for a listing of the respective mathematical derivations and definitions.

5.1 Partial Symmetry (P.S.)

The symmetry shown in Fig. 3 is, in fact, a special case of what will be called partial-symmetry. In fact this type of symmetry may be exploited in several different ways, as shown in Fig. 4. If, for example, a symmetry exists as shown in Fig. 4(a) we can opt to synthesize the pattern (sub-function) in area $x_i = 0$, $x_j = 1$ and use a NOR gate, with a complemented input for x_i, to 'reflect' this pattern into area $x_i = 0$, $x_j = 0$ as shown in Fig. 4(d). (The arrow in Fig. 4(d) is used to show the area which will be synthesized, Fig. 4(a) shows the 'reflection'.) Alternatively, the area $x_i = 0$, $x_j = 0$ may be synthesized and the result 'reflected' into area $x_i = 0$, $x_j = 1$, as shown in Fig. 4(e), using an AND gate.

The symmetry shown in Fig. 4(a) may thus be exploited in two different ways and using two different types of gate. This characteristic is common in all types of symmetry designs and allows a flexibility of choice of implementation. This property is of great practical importance because certain gate types may be favoured by certain technologies. Using the symmetry method of design it is thus possible to synthesize circuits which are technology-compatible. This choice of gate type is also important when, as in complete designs, such gates are cascaded.

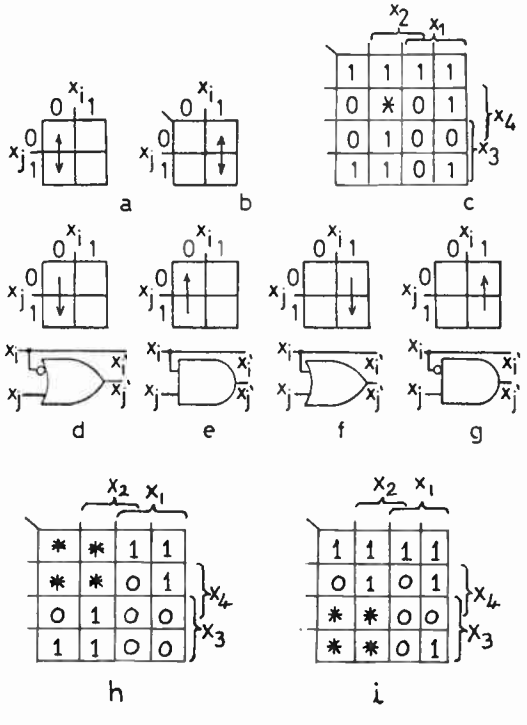


Fig. 4. Partial symmetry and its implementation.

It is then sometimes possible to 'merge' two, say 2-input AND gates to give a multiple 3-input AND gate. More of this later.

An alternative symmetry is shown in Fig. 4(b). In fact this symmetry is identical to that of Fig. 4(a) save that x_i has been replaced by $\bar{x}_i$. This property is exhibited in the corresponding gate configurations of Fig. 4(f), (g).

In order that partial-symmetry may be quickly referred to, the notation $\{\bar{x}_i, x_j\}$ will be used to define the partial-symmetry shown in Fig. 4(a). That is, in area $\bar{x}_i$, a sub-function exists in both areas for which $x_j = 0$ and $x_j = 1$.

The symmetry of Fig. 4(b) is thus denoted by $\{x_i, x_j\}$.

Figure 4(c) shows a practical example where $\{\bar{x}_1, x_3\}$ holds. That is, the 'third quadrant' of the map 'reflects' onto the 'fourth quadrant' *if* the unspecified (don't care) state $*$ is allocated as logical 1. This is most easily seen by taking a mirror and placing it along the horizontal centre-line of the map. The lower left 'quadrant' now reflects onto the upper 'quadrant' if $*$ is set to 1. This example thus illustrates that it is meaningful to consider symmetries of functions with don't-care states. Indeed, this is essential since each stage of synthesis has the effect of creating more don't-care states. For example, if the implementation of Fig. 4(d) is used for the case shown in Fig. 4(c), the function remaining to be synthesized is shown in Fig. 4(h) and three extra don't-care states are created. In practice the synthesis procedure would now be applied to the function of Fig. 4(h).

Figure 4(i) shows the effect of implementing the circuit type shown in Fig. 4(e).

It is not proposed that a mirror should be appended to the logic design aids currently available!—in fact the digital computer may be used for the detection of function symmetries.

An exhaustive list of partial-symmetry maps is given in Appendix 2(a) for functions of fourth-order ($n = 4$) for the purpose of 'pencil-and-paper' computation.

Some further possible implementations are shown in Appendix 1(a).

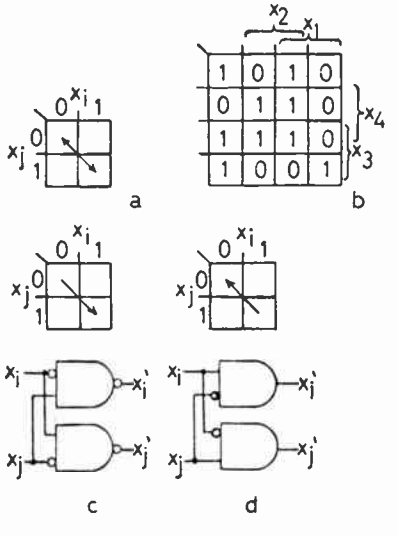


Fig. 5. Equivalence symmetry and its implementation.

It can also be shown (see Appendix 3.1) that partial-symmetries can be expressed directly in terms of the Boolean differences. Specifically, for the case shown in Fig. 4(a), i.e. $\bar{x}_i, x_j$:

$$\bar{x}_i \cdot \frac{\mathrm{d}f(x_i, x_j)}{\mathrm{d}x_j} = 0.$$

It follows directly that the existence of the symmetry $\bar{x}_i, x_j$ can be established by inspection of the first-order Boolean differences. These differences can also be used to detail the test parameters for the nodes corresponding to x_i, x_j.

5.2 Simple Symmetry

Simple symmetries are divided into two types:
equivalence-symmetry and *non-equivalence-symmetry*.

5.2.1 *Equivalence symmetry* (E.S.)

This symmetry is so-called because, referring to Fig. 5(a), identical sub-functions appear in areas where $x_i = x_j$. In fact this notation will be used to identify equivalence-symmetry.

It will be noted that, again, there are several possible implementations [Fig. 5(c), (d), Appendix 1(b)] but that in this case two conventional gates are required. Unlike the case of P.S. the 'reflections' are no longer between adjacent parts of the map (Hamming distance = 1) but across 'diagonals' (Hamming distance = 2). Figure 5(b) shows a practical example which exhibits equivalence-symmetry $x_1 = x_3$ that is, 2nd 'quadrant' to 4th 'quadrant'.

Equivalence-symmetry can be defined in terms of the double Boolean difference, as shown in Appendix 3.2.1.

See Appendix 2(b) for $n = 4$ maps.

5.2.2 *Non-equivalence symmetry* (N.E.S.)

In this case identical sub-functions appear in areas where, referring to Fig. 6(a), $x_i \neq x_j$. This symmetry can be identified with equivalence-symmetry if one of the inputs x_i, x_j are complemented; the corresponding implementations make this clear. [Fig. 6(c), (d), Appendix 1(b).] The practical example of this symmetry is shown in Fig. 6(b) where $x_1 \neq x_3$.

The definition of this symmetry in terms of the double Boolean difference is given in Appendix 3.2.2.

5.3 Multiform Symmetry (M.F.S.)

A function which exhibits both equivalence and non-equivalence symmetry in x_i, x_j, is multiform-symmetric in x_i, x_j. This is clear from the inspection of Fig. 7(a). This symmetry is thus denoted as: $x_i \overset{=}{\neq} x_j$ (referring to Fig. 7(a)).

The exploitation of this symmetry is shown in Fig. 7(c–f). It should be noted that a single exclusive-OR/NOR gate is employed. In fact the synthesis method is capable of optimally utilizing the exclusive-OR/NOR gate†, a

† Some interesting properties of the exclusive-OR operator are given in Ref. 13.

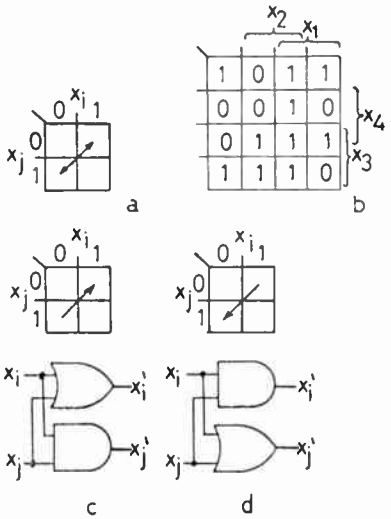


Fig. 6. Non-equivalence symmetry and its implementation.

capability unique to this method. (The Reed–Muller expansion[8,9] employs the exclusive-OR gate, but not optimally.)

Note that the implementations of Fig. 7(c), (d) are related to those of Fig. 7(e), (f) by a simple change of output label.

Unlike the symmetries previously considered, the modules employed to exploit multiform symmetry have two inputs and *one* output. This means that after utilizing such modules the number of variables in the function remaining to be synthesized is one less than in the previous stage of synthesis.

Figure 7(b) shows a practical example which is $x_1 \overline{\neq} x_3$ *if* the don't-care state $*$ is set to logical 1. (See also Appendix 2(c).)

Appendix 3.3 gives the definition of this symmetry in terms of the Boolean difference.

5.4 Compatible Symmetry (C.S.)

It is possible that functions may exhibit partial symmetry in two variables as shown in Fig. 8(a–d). In Fig. 8(a), for example, both x_i, x_j and x_j, x_i exist. This is a case of

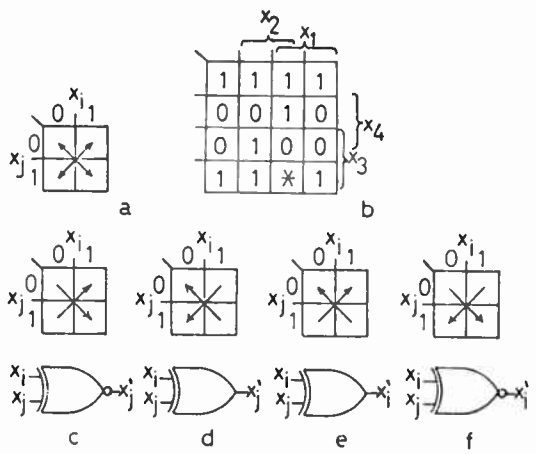


Fig. 7. Multiform symmetry and its implementation.

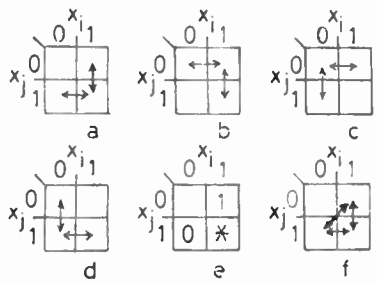


Fig. 8. Compatible symmetry.

compatible-symmetry. Note also that the multiform symmetry $x_i \neq x_j$ is implied (Fig. 8(f)). In fact, when don't care states are present, $x_i \neq x_j$ is a necessary condition. This is illustrated by Fig. 8(e) where: if $*$ is set to 1 then x_i, x_j exists, and if $*$ is set to 0 more x_j, x_i exists, but $*$ cannot simultaneously take values 0 and 1! No symmetry $x_i \neq x_j$ exists therefore for the function of Fig. 8(e). (See also Appendix 3.4.)

Some possible implementations are shown in Fig. 9. Here again the implementation modules have two inputs and one output, resulting in variable redundancy. (See also Appendix 1(d).)

5.5 General Observations

The symmetries considered above have given rise to implementations which execute many-one mappings, that is, one 'area' in n-space is mapped *onto* another 'area'.

From a theoretical viewpoint there are only two fundamental symmetries, that is, partial and simple. All other symmetries can be derived from these. However, from a practical viewpoint the multiform and compatible symmetries have been considered as separate cases to emphasize the special gate forms possible for their implementation.

6 Spectral Translation and its Implementation

In this Section techniques are considered which promote function synthesis by one-one mappings. That is, the states of the function are simply 'rotated' in n-space and no new don't-care states are created.

The reasons for employing spectral translation techniques are twofold. Firstly, certain functions exist which

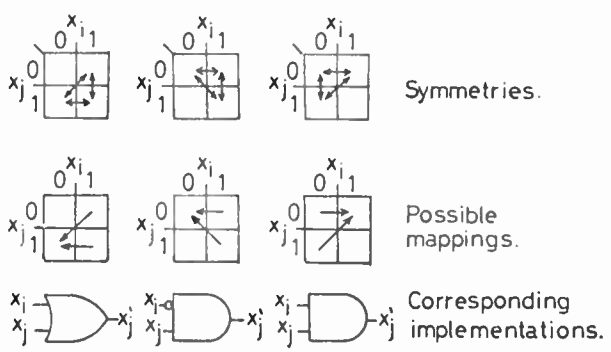


Fig. 9. Implementations of compatible symmetry.

exhibit none of the symmetries so far discussed. Such functions could not therefore be synthesized using the techniques discussed so far, unless some partition of the function was allowed. Secondly, certain functions may be implemented at lower cost when both spectral *and* symmetry techniques are used than when only symmetry methods are applied. Since spectral techniques are implemented in terms of the exclusive-OR/NOR gate, a simple realization[12,14] of this gate in the technology employed is normally a pre-requisite for minimum cost.

Details of the following spectral techniques appear in Refs. 4, 15, 16, 17, and only a brief résumé of the theory will be given here.

6.1 The Rademacher–Walsh Transform

The purpose of taking the Rademacher–Walsh transform of a Boolean function is that, under the transform, certain operations, which are cumbersome using conventional techniques, are greatly simplified. An analogy can be drawn between the Walsh Transform applied to Boolean data and the Discrete Fourier Transform applied to time-dependent signals.

In order to take the Rademacher–Walsh transform of a Boolean function, we first express the function as a truth-table. Referring to the example of Fig. 10(a), the truth table is:

x_1	x_2	x_3	$f(x_1, x_2, x_3)$	
0	0	0	1	−1
0	0	1	1	−1
0	1	0	0	+1
0	1	1	1	−1
1	0	0	1	−1
1	0	1	0	+1
1	1	0	1	−1
1	1	1	1	−1
Truth Table				$B]$

The output vector is then modified by replacing logical 1 by '−1' and logical 0 by '+1', to give the vector $B]$ above.

The Walsh transform is then taken as:

$$[W]B] = R] \tag{9}$$

where $R]$ is the Walsh spectrum of the function. $[W]$ is the Walsh matrix.

Now each of the components of $R]$, termed 'spectral components', are related to Rademacher functions and give information about the Boolean function originally transformed.

The spectral components are given coefficient values labelled 'R' and a subscript 's' which indicates to which combinations of Rademacher functions they are associated.

For the example of Fig. 10(a) the spectrum is:

R_0	R_1	R_2	R_3	R_{12}	R_{13}	R_{23}	R_{123}
−4	0	0	0	−4	+4	−4	0

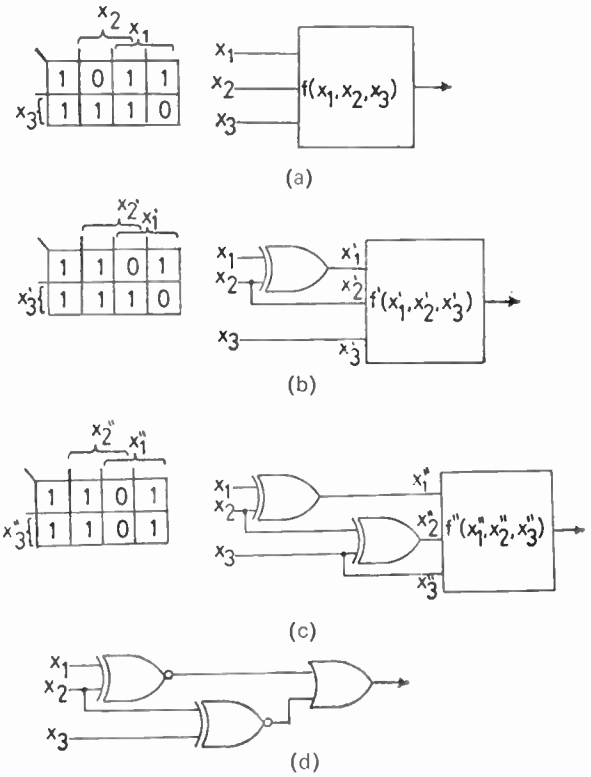


Fig. 10. Spectral translation and its implementation.

The components R_1, R_2, R_3 are a measure of the correlation between the function and inputs x_1, x_2, x_3 respectively; the coefficients R_{12}, R_{13}, R_{23} are a measure of the correlation between the function and $(x_1 \oplus x_2)$, $(x_1 \oplus x_3)$ etc. The larger the *magnitude* of the component the higher the correlation. Negative components indicate a complementary correlation. For example the negative value of R_{12}, above, indicates that the original function correlates with $(x_1 \overline{\oplus} x_2)$. Coefficients with only one subscript, namely R_1, R_2, are termed first-order coefficients whereas those with two subscripts, namely R_{12}, R_{13} are termed second-order. The zero-order term R_0 is a measure of the ratio of the number of true/false minterms of the original function.

It has been found that the functions which are easiest to synthesize are those which have their highest-magnitude components in first- and zero-ordered positions. The reason for this can be illustrated by considering a function whose spectrum is only one positive component at, say, R_2. This function then not only has a strong correlation with x_2 but in fact *is* x_2. This function can be synthesized by simply connecting the input x_2 to the output. If however, this component were situated at R_{12}, say, then the synthesis would be implemented by an exclusive-OR gate connected between inputs x_1, x_2 and the output. This increase in circuit complexity with increase of function order also holds for functions having 'spread' spectral components, as in the example above, which is predominantly second-order.

The order of a function can be reduced by employing exclusive-OR/NOR gates using the following techniques.

6.2 Spectral Translation

Spectral translation moves certain high-order spectral components into lower-order positions.

The Theorem of Spectral Translation:[4] If in a Boolean function $f(x_1, \ldots, x_k, \ldots, x_n)$ having a spectrum R, x_k is replaced by $[\{x_a \oplus x_b - - - \oplus x_h\} \oplus x_k]$ where the set of subscripts $\langle a, b, - - -, h \rangle$ is denoted by $\langle s \rangle$, then the spectrum R' of the new function is generated from the spectrum R if in every subscript of the spectral coefficients R_s containing k, the members of $\langle s \rangle$ are deleted if they exist, and appended if they do not.

In the example of Fig. 10(a), let x_1 be replaced by $(x_1 \oplus x_2)$; a new spectrum R' is generated where $R_1' = R_{12}$, $R_{12}' = R_1$, $R_{123}' = R_{13}$, $R_{13}' = R_{123}$, and $R_2' = R_2$, $R_3' = R_3$, $R_{23}' = R_{23}$.

The new spectrum R' corresponds to a new (but linearly related) function $f'(x_1', x_2', x_3')$. For the implementation and effect of this operation, see Fig. 10(b). The new spectrum is:

R_0'	R_1'	R_2'	R_3'	R_{12}'	R_{13}'	R_{23}'	R_{123}'
−4	−4	0	0	0	0	−4	+4

(derived as detailed above).

Repeating this operation for x_2' replaced by $(x_2' \oplus x_3)$ gives

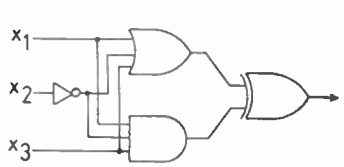
R_0''	R_1''	R_2''	R_3''	R_{12}''	R_{13}''	R_{23}''	R_{123}''
−4	−4	−4	0	+4	0	0	0

(See Fig. 10(c).) The function simplification is now clear:

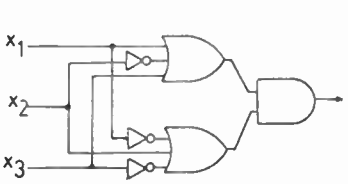
$$f''(x_1'', x_2'', x_3'') = [\bar{x}_1'' + \bar{x}_2'']$$

giving a possible solution shown in Fig. 10(d).

It was stated above that it is sometimes advantageous to implement a stage of synthesis using this method instead of the symmetry approach. To illustrate this point consider Fig. 11(a) which shows a representative synthesis of the example of Fig. 10 using only spectral methods. Figure 11(b) shows, for comparison, a NOT/OR/AND solution. The major parameters are set out in Table 1.



(a) Synthesis of example shown in Fig. 10 using many-one mappings.



(b) Synthesis of same example using NOT/OR/AND method.

Fig. 11

Table 1.

Synthesis type	Mapping	No. of gates	No. of inter-connections	No. of crossovers	Delay
Translation (Fig. 10(d))	one-one	3	6	0	2
Symmetry	many-one	4	9	3	3
NOT/OR/AND	—	6	11	3	3

The translation technique clearly has an advantage in this case. Note that, in general, syntheses will employ both symmetry and spectral techniques.

Spectral translation may also be defined in terms of the Boolean difference. (See Appendix 3.5.)

6.3 Disjoint Spectral Translation

This operation gives rise to a feed-forward signal path (thus the name 'disjoint'), as shown in Fig. 12. The great advantage of this operator is that several spectral components may be translated to lower orders simultaneously (if they share a common variable in their coefficient subscripts). This operation differs from that of spectral-translation in that it allows first-order spectral components to be translated into the zero-order (R_0) position; thus changing the ratio of true/false minterms.

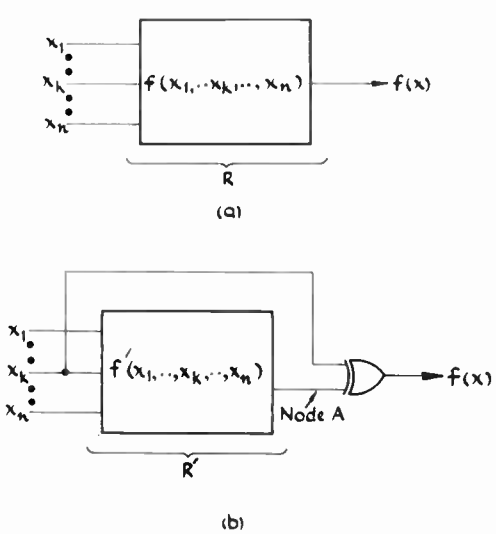


Fig. 12. Implementation of disjoint-spectral translation.

The Theorem of Disjoint Spectral Translation:[4] If, given a Boolean function $f(x_1, \ldots, x_k, \ldots, x_n)$ having a spectrum R, it is required to generate a new function $f'(x_1, \ldots, x_k, \ldots, x_n)$ having a spectrum R' where $f(x_1, \ldots, x_k, \ldots, x_n) \triangleq [x_k \oplus f'(x_1, \ldots, x_k, \ldots, x_n)]$ then R' may be generated from R if in every subscript of the spectral coefficients of R, k is deleted if it exists and is appended if it does not.

By way of example consider the function shown in Fig. 22(a) (the synthesis of this function is considered later). It has the spectrum:

	R_0	R_1	R_2	R_3	R_4	R_{12}	R_{13}	R_{14}	R_{23}	R_{24}	R_{34}	R_{123}	R_{124}	R_{134}	R_{234}	R_{1234}
$f(X)$	0	0	0	−2	−6	0	−2	+2	−2	+2	0	−2	+2	0	0	0

After applying disjoint spectral translation in x_4, the new spectrum is:

	R_0	R_1	R_2	R_3	R_4	R_{12}	R_{13}	R_{14}	R_{23}	R_{24}	R_{34}	R_{123}	R_{124}	R_{134}	R_{234}	R_{1234}
$f'(X)$	−6	+2	+2	0	0	+2	0	0	0	0	−2	0	0	−2	−2	−2

Note that the highest-valued component has been translated to the zero-order position, R_0; this results in a great simplification of the problem. (See Fig. 22(c), (d)).

The operation of disjoint spectral translation may be repeated to give more than one feed-forward path. A possible disadvantage of this operation is that 'hazards' may be created.

See also Appendix 3.6.

7 Some Practical Considerations

It will be noted that the above operations have involved only two variables (or signal lines). How then were the three-input gates shown in Fig. 11(a) generated? To answer this question, and also to give a step-by-step synthesis example under symmetry mappings consider Fig. 13(a). The function considered is that of Fig. 10(a). This function has no multiform symmetries, three simple symmetries (two E.S. and one N.E.S. as shown), and no partial symmetries or compatible symmetries. Suppose that it is decided to implement $x_1 \neq x_3$ using the gate configuration shown in Fig. 13(b), perhaps because it suits the technology to be employed. The mapping generated is shown together with the resulting new function $f'(x_1', x_2', x_3')$. (See also Appendix 1.) Note that the two true minterms have been replaced by 'don't cares'—this would be the case for the implementation of any of the symmetries shown in Fig. 13(a).

The symmetries associated with $f'(x_1', x_2', x_3')$ are shown in Fig. 13(c). Some of these mappings are 'trivial' in the sense that when implemented the function will not be simplified. (The total number of 'don't care' states will remain constant.) A summary of the extra number of true/false minterms replaced or 'updated' by mappings associated with each of the symmetries together with the required gate count is given in Table 2.

Table 2.

Symmetry	True minterm update	False minterm update	Gates for implementation	Comment
$x_1' = x_2'$ (E.S.)	1	0	2	
$x_1' \neq x_3'$ (N.E.S.)	0	0	2	trivial, as stage 1
$x_2' = x_3'$ (E.S.)	1	0	2	
$\bar{x}_2', x_1'$ (P.S.)	1	0	1	
$\bar{x}_1', x_3'$ (P.S.)	0	0	1	trivial
x_3', x_1' (P.S.)	0	0	1	trivial
x_2', x_3' (P.S.)	1	0	1	

Note: Although $\bar{x}_1'$, x_3' and x_3', x_1' are present this does not constitute a compatible symmetry since $x_1' = x_3'$ does not hold (see Sect. 5.4). Although 'trivial' is used here in the sense that no extra 'don't care' terms are generated, it should be noted that in certain cases such symmetries may be used to carry out one-one mappings without using the exclusive-OR operator.

The non-trivial cases that most efficiently generate don't care terms above are thus $\bar{x}_2'$, x_1' and x_2', x_3'. Several gate configurations may be used to implement these partial symmetries (see Appendix 1). Suppose that the configuration shown in Fig. 13(d) is chosen for $\bar{x}_2'$, x_1', then it is possible to merge the OR gate of this stage with the OR gate of the first stage (Fig. 13(e)). This 'merging' process thus reduces the overall gate count and gives rise to gates with fan-ins of more than two. Of course this process may be limited to give syntheses where the gate fan-in is restricted. The choice of gate configuration at each stage illustrates the flexibility of the method.

The synthesis at the second stage is now as Fig. 13(f). The non-trivial symmetries of $f''(x_1'', x_2'', x_3'')$ are $x_2'' = x_3''$; x_2'', x_3''; $\bar{x}_3'', x_2''$ (see Fig. 13(g)). These form a compatible symmetry. A suitable implementation which allows 'merging' is shown in Fig. 13(h). The result is shown in Fig. 13(i). Note that the remainder function is independent of x_2'''.

The only non-trivial symmetry of $f'''(x_1''', x_3''')$ is multiform for $x_1''' \neq x_3'''$, Fig. 13(j). A suitable implementation is shown in Fig. 13(k). The remainder function (Fig. 13(l)) is of order 1 and thus is either invert or non-invert. Inspection shows the non-invert form is required here: $f''''(x_3'''') = x_3''''$ (by inspection) so that the final circuit is as was shown in Fig. 11(a).

A note here on mappings applied to functions with 'don't care' terms. The possible mappings appear in Table 3.

An example of the mapping $0 \xrightarrow{A \quad B} *$ appeared in the example of Fig. 13 (Fig. 13(f), (h), (i)). The explanation for the corresponding mapping rule is that $B = *$ must take the value 0 in order that the mapping be legal; after execution the n-space A will not be addressed and so may then take the value $*$. A similar argument may be applied to $1 \rightarrow *$. (See Sect. 5.1.)

Figure 14(a) gives an example of some of the above mapping types. It is interesting to note that the method cannot distinguish between 'don't care' states generated by previous stages of synthesis and those present in the

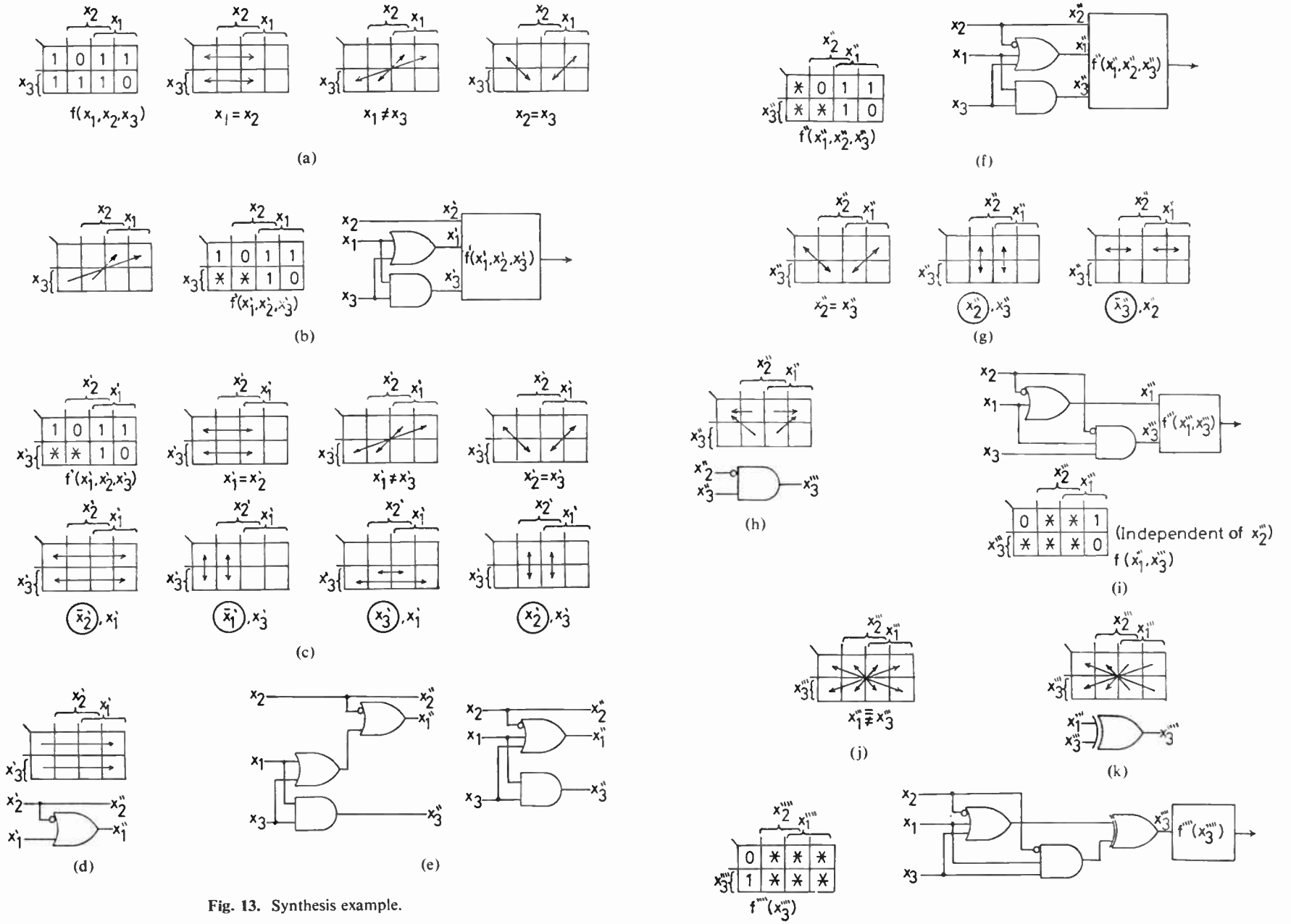


Fig. 13. Synthesis example.

Note.—The encircled symbols represent partial symmetry and correspond to $\bar{x}'_2$ etc. in the text.

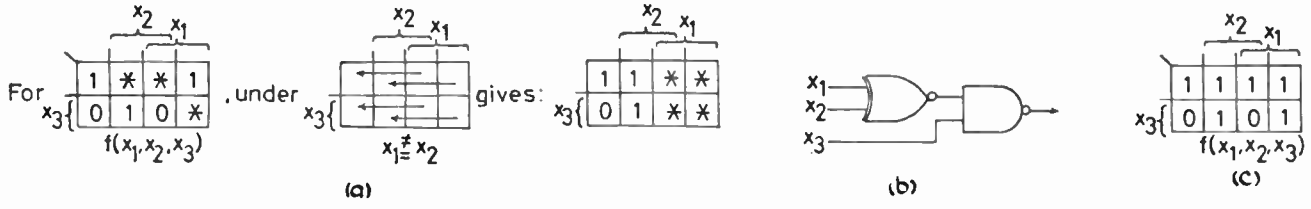


Fig. 14. Mapping example.

original function. In either event the 'don't care' terms are optimally allocated values 0 or 1. Suppose, for example, that the function $f(x_1, x_2, x_3)$ of Fig. 14(a) was the original required function. A synthesis obtained by the many-one mapping method is shown in Fig. 14(b). The function solved by this implementation is shown in Fig. 14(c). The allocation of values to 'don't care' states can be seen by comparing $f(x_1, x_2, x_3)$ Fig. 14(a) and Fig. 14(c).

The examples given so far have only considered single-output syntheses. The techniques described may, however, also be applied to multiple-output syntheses. Consider the schematic of Fig. 15 which involves a 3-output problem. The stages of synthesis 1 to α are common to all three functions. The term 'common' also implies non-trivial, since trivial mappings will serve to increase propagation delay and power consumption without increasing the elegance of solution. At stage α it is found that the non-trivial symmetries and/or useful one-one mappings associated with $f_1(X)$ are disjoint with respect to those of $f_2(X)$ and $f_3(X)$ with the result that the $f_1(X)$ synthesis is completed disjointly using stages β, γ. Now $f_2(X)$ and $f_3(X)$ have one further common synthesis stage δ before disjointing to be solved by ϵ and ζ respectively. The stages 1 to α will be referred to as common mappings hereinafter. The implementation of common mappings can prove to provide very elegant solutions to multiple-output problems where the exclusive-OR operator is efficiently utilized, particularly where the required functions are related, e.g. arithmetic units, decoders, majority logic, threshold logic.

Table 3.

Mapping		Operation	Comments
From A=	To B=		
0	1	—	illegal
1	0	—	illegal
1	1	replace A by *	true minterm replaced by 'don't care'
0	0	replace A by *	false minterm replaced by 'don't care'
*	1	none	no change in the number of 'don't cares'
*	0	none	no change in the number of 'don't cares'
0	*	replace A by *, replace B by 0	no change in the number of 'don't cares'
1	*	replace A by *, replace B by 1	no change in the number of 'don't cares'

In certain cases single/multiple output functions may be realized by the repeated application of the same type of mapping. This gives rise to syntheses which employ identical logic modules (cells) for implementation. Such solutions are otherwise known as cellular arrays.[18]

As an example of a multiple-output synthesis having common-mappings and giving rise to a cellular array consider the universal 8th-order universal-threshold gate[19] of Fig. 16. This solution was generated under many-one (N.E.S., $x_i \neq x_j$) mappings and implemented using AND/OR cells, see Appendix 1. It will be noted that the first four levels of synthesis are generated from common mappings for all 8 outputs.

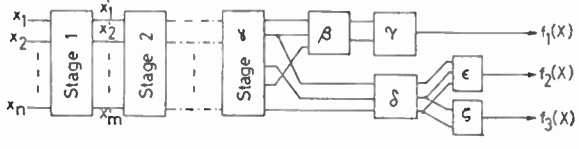


Fig. 15. Common mapping (schematic).

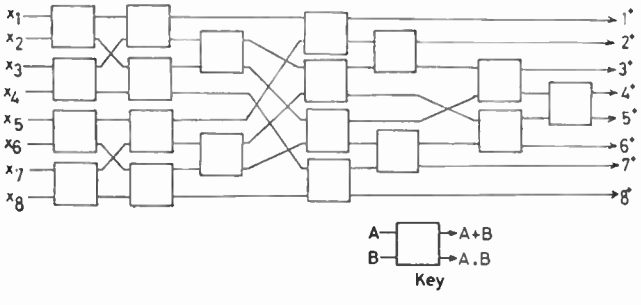
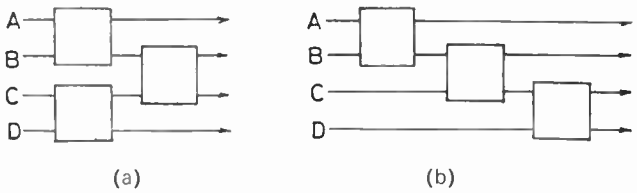


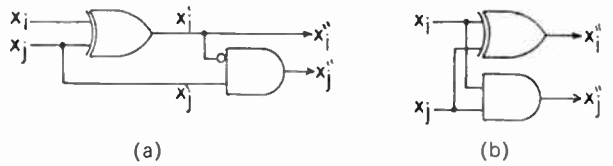
Fig. 16. Cellular array generated using common mappings.

The minimization of signal propagation delays can be accomplished in several ways under the synthesis method. The most obvious of these, and one which was introduced above is gate 'merging'. The second method is to employ consecutive synthesis stages which involve disjoint variable sets, whenever possible, i.e. Fig. 17(a) rather than Fig. 17(b). Another technique, which may reduce propagation delay without employing gate merging, is applicable for cases when syntheses utilize both symmetry and spectral methods. Consider the function of Fig. 18(a). The first synthesis stage has been generated by the one-one mapping (spectral translation) $x_i' = [x_i \oplus x_j]$, $x_j' = x_j$; the second



(a) (b)

Fig. 17. Reduction of propagation delays by disjoint synthesis.



(a) (b)

Fig. 18. Propagation delays reduced by circuit re-arrangement.

stage implements the partial-symmetry $\mathbf{x}_i, x_j$ (see Appendix 1).

Now these two stages can be replaced by the circuit shown in Fig. 18(b) with a gate propagation-delay saving of 1. Note that the vertex function $(\bar{x}_i' \,.\, x_j')$ has been replaced by $(x_i \,.\, x_j)$. This observation applies in general cases where

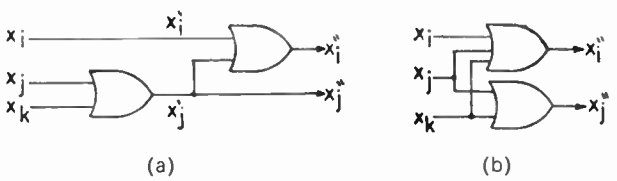
$$f_1(x_i, x_j) = [x_i \oplus x_j] \quad \text{and} \quad f_2(x_i, x_j) = f'(x_i, [x_i \oplus x_j]),$$

or where

$$f_1(x_i, x_j) = f'(x_i, x_j) \quad \text{and} \quad f_2(x_i, x_j) = [x_i \oplus f'(x_i, x_j)],$$

where $f'(x_i, x_j)$ is some vertex function.

It should be noted that, for an n-variable problem, no more than $n+1$ signal lines are generated between each stage of synthesis. This is because each module used to implement a synthesis stage has two inputs and not mere than three outputs. This is a signal-path restriction inherent to the symmetry and spectral method. However, propagation delay may also be reduced by the re-arrangement of circuits of the type shown in Fig. 19(a) to give solutions having gates with increased fan-in



(a) (b)

Fig. 19. Propagation delays reduced by circuit re-arrangement.

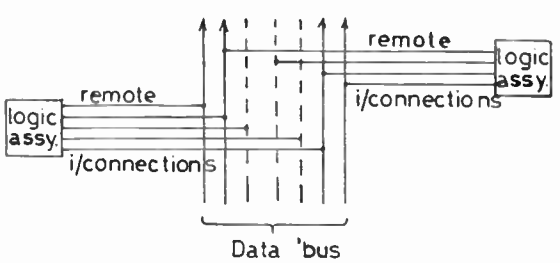


Fig. 20. Minimization of data bus connections.

(Fig. 19(b)). Although this re-arrangement is a post-mapping exercise (the signal-path restriction may be infringed), it may be used as a criterion for choosing the gate-type in syntheses requiring minimal delays.

The efficient use of the exclusive-OR operator has been found to give rise to circuits requiring signal inputs which are of single polarity, i.e. variable x_i is generally required only in the true or complemented mode, but not both. Neither is it necessary usually to generate both x_i and $\bar{x}_i$ by using inverters in the circuits themselves. This is in marked contrast to the NOT/AND/OR configurations. In the case of logic assemblies driven from a data bus which is physically remote, this results in the reduction of 'remote connections' required (Fig. 20) or the reduction in the number of duplicated inverter gates. This saving can be very significant in the utilization of surface area in l.s.i., e.g. microprocessors.

8 The Design Method and Testing

It has been shown that function symmetry and one-to-one mappings may be employed in the synthesis of combinational digital circuits. Moreover the mathematical definitions of such symmetries may be formalized in terms of the Boolean difference. It will now be shown that the test data for a circuit may be generated by consideration of the symmetries and/or one-to-one mappings giving rise thereto.

The examples below are taken from Zissos.[20]

8.1 Example 1: Synthesis of the Function shown in Fig. 21(a)

The first-order Boolean differences appear in Fig. 21(b) to (d). We have immediately:

Fault	Test	
x_1 s.a.0	$x_1 \,.\, \{1\} = 1$	(a)
x_1 s.a.1	$\bar{x}_1 \,.\, \{1\} = 1$	(b)
x_2 s.a.0	$x_2 \,.\, \{x_3\} = 1$	(c)
x_2 s.a.1	$\bar{x}_2 \,.\, \{x_3\} = 1$	(d)
x_3 s.a.0	$x_3 \,.\, \{x_2\} = 1$	(e)
x_3 s.a.1	$\bar{x}_3 \,.\, \underbrace{\{x_2\}}_{\frac{df(X)}{dx_i}} = 1$	(f)

In addition

$$\left.\begin{aligned} &\left\{\bar{x}_3 \,.\, \frac{df(X)}{dx_2}\right\} = 0, \quad \text{i.e. } \bar{\mathbf{x}}_3, x_2 \\ \text{and} \quad &\left\{\bar{x}_2 \,.\, \frac{df(X)}{dx_3}\right\} = 0, \quad \text{i.e. } \bar{\mathbf{x}}_2, x_3 \end{aligned}\right\} \text{ from Appendix 3, equation (15)}$$

which form a compatible symmetry

$$\bar{\mathbf{x}}_3, x_2; \quad \bar{\mathbf{x}}_2, x_3; \quad x_2 \neq x_3,$$

which may be implemented (see also Appendix 1) as shown in Fig 21(e), leaving a remainder function $f'(X)$ shown in Fig. 21(f).

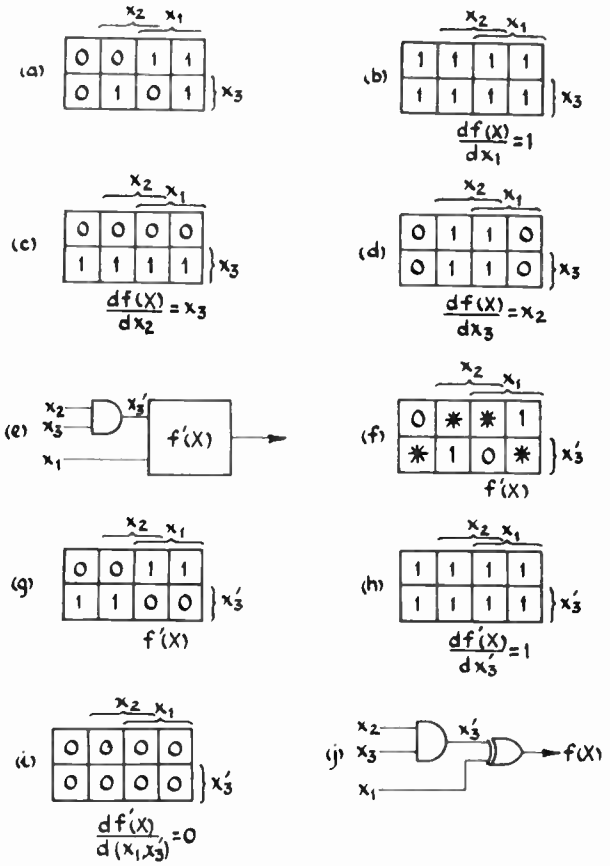


Fig. 21
(a) Given example.
(b) to (d) First-order Boolean differences.
(e) First-stage implementation.
(f) Remainder function.
(g) to (i) Allocation of states and differences.
(j) Final synthesis.

Suppose that the undetermined state s_* are allocated as shown in Fig. 21(g). Then $df'(X)/dx_3' = 1$, as shown in Fig. 21(h), and hence we have

Fault	Test	
x_3' s.a.0	$x_3' \cdot 1 = (x_2 \cdot x_3) = 1$	(g)
x_3' s.a.1	$\bar{x}_3' \cdot 1 = \overline{(x_2 \cdot x_3)} = 1$	(h)

Now we have generated 8 tests for 'stuck-at' faults for each node of the circuit of Fig. 21(j). Consider the input:

x_1	x_2	x_3
1	1	1

This input satisfies *any one* of the tests (a), (c), (e), (g). That is, by applying this input and observing the output we can detect any one of the faults (a), (c), (e), (g). Similarly, the input:

x_1	x_2	x_3
0	1	0

can be used to detect any one of the faults (b), (f), and

x_1	x_2	x_3
0	0	1

can be used to detect any one of the faults (d), (h). It may be concluded therefore that the set

x_1	x_2	x_3
1	1	1
0	1	0
0	0	1

may be used to find any *single* 'stuck-at' fault (with the exception of the output node) of the final circuit (Fig. 21(j)). This set is known as a reduced test set. Note that if multiple 'stuck-at' faults are present these tests are not sufficient. See also Ref. 1.

In addition $df'(X)/d(x_1, x_3') = 0$, cf. equation (21), see Fig. 21(i), and a multiform symmetry $x_1 \overset{=}{\neq} x_3'$ exists. This may be implemented (see also Appendix 1) as shown in Fig. 21(j). This completes the synthesis. Note:

(a) The final synthesis is very elegant and very easily tested, having only one 'internal' node x_3'.

(b) The allocation of undetermined states is fundamental to both the synthesis and test criteria.

(c) The method is capable of utilizing the exclusive-OR gate optimally—the exclusive-OR function forms the basis of many 'easily tested' networks by virtue of the result:

$$\frac{d(x_i \oplus x_j)}{dx_i} = \frac{df(x_i \oplus x_j)}{dx_j} = 1.$$

(d) The method gives rise to multi-level realizations which generally require far fewer tests than two-level realizations (see also Ref. 1, chapter 6).

8.2 Example 2: Synthesis of the Function shown in Fig. 22(a)

The first-order differences are shown in Fig. 22(b). The tests for the primary inputs: x_1, x_2, x_3, x_4 are thus:

Fault	Test		
x_1 s.a.0	$x_1 \cdot \{\bar{x}_2 \cdot (x_3 \oplus x_4)\} = 1$		(a)
x_1 s.a.1	$\bar{x}_1 \cdot \{\bar{x}_2 \cdot (x_3 \oplus x_4)\} = 1$		(b)
x_2 s.a.0	$x_2 \cdot \{\bar{x}_1 \cdot (x_3 \oplus x_4)\} = 1$		(c)
x_2 s.a.1	$\bar{x}_2 \cdot \{\bar{x}_1 \cdot (x_3 \oplus x_4)\} = 1$		(d)
x_3 s.a.0	$x_3 \cdot \{\bar{x}_1 \cdot \bar{x}_2\} = 1$		(e)
x_3 s.a.1	$\bar{x}_3 \cdot \{\bar{x}_1 \cdot \bar{x}_2\} = 1$		(f)
x_4 s.a.0	$x_4 \cdot \{\bar{x}_1 + \bar{x}_2\} = 1$		(g)
x_4 s.a.1	$\bar{x}_4 \cdot \underbrace{\{\bar{x}_1 + \bar{x}_2\}}_{\frac{df(X)}{dx_i}} = 1$		(h)

The first stage of the synthesis chosen is disjoint spectral translation in variable x_4 (Fig. 22(c)). (See also Sect. 6.3.)

The effect of this stage is to significantly lower the order of the spectrum of the required (remainder) function as follows:

	R_0	R_1	R_2	R_3	R_4	R_{12}	R_{13}	R_{14}	R_{23}	R_{24}	R_{34}	R_{123}	R_{124}	R_{134}	R_{234}	R_{1234}
$f(X)$	0	0	0	−2	−6	0	−2	+2	−2	+2	0	−2	+2	0	0	0
$f'(X)$	−6	+2	+2	0	0	+2	0	0	0	0	−2	0	0	−2	−2	−2

The result is to generate the remainder function shown in Fig. 22(d).

It can be shown that

$$\frac{\mathrm{d}f'(X)}{\mathrm{d}(x_3, x_4)} = 0 \text{ for this function.}$$

This shows that the remainder function is multiform-symmetric: $x_3 \overline{=}_{\neq} x_4$, see equation (21). The second stage of synthesis is then taken as shown in Fig. 22(e), giving the remainder function $f''(X)$ shown in Fig. 22(f). The first-order Boolean differences of this function are shown in Fig. 22(g). From $\mathrm{d}f''(X)/\mathrm{d}(x_3')$ we have immediately:

Fault	Test	
x_3' s.a.0	$x_3' \cdot \bar{x}_1 \cdot \bar{x}_2 = (x_3 \overline{\oplus} x_4) \cdot \bar{x}_1 \cdot \bar{x}_2 = 1$	(i)
x_3' s.a.1	$x_3' \cdot \bar{x}_1 \cdot \bar{x}_2 = (x_3 \oplus x_4) \cdot \bar{x}_1 \cdot \bar{x}_2 = 1$	(j)

Note that these fault conditions can be propagated to the output node B by setting $x_4 = 0$ or $x_4 = 1$.

From Fig. 22(g) we note that

$$\left\{x_2 \cdot \frac{\mathrm{d}f''(X)}{\mathrm{d}x_1}\right\} = \left\{x_1 \cdot \frac{\mathrm{d}f''(X)}{\mathrm{d}x_2}\right\} = 0,$$

so that there exists a compatible symmetry from equation (25), of

$$x_1, x_2;\ x_2, x_1,$$

which may be implemented as shown in Fig. 22(h) and gives rise to node x_2''. The tests for x_2'' will not be derived here because, as is shown below, this node is finally merged.

The remainder function $f'''(X)$ is shown in Fig. 22(i). The first-order differences thereof are shown in Fig. 22(j); it is noted that

$$\left\{x_3' \cdot \frac{\mathrm{d}f'''(X)}{\mathrm{d}x_2''}\right\} = \left\{x_2'' \cdot \frac{\mathrm{d}f'''(X)}{\mathrm{d}x_3'}\right\} = 0,$$

so that there exists a compatible symmetry, from equation (25), of

$$x_2'', x_3';\ x_3', x_2,$$

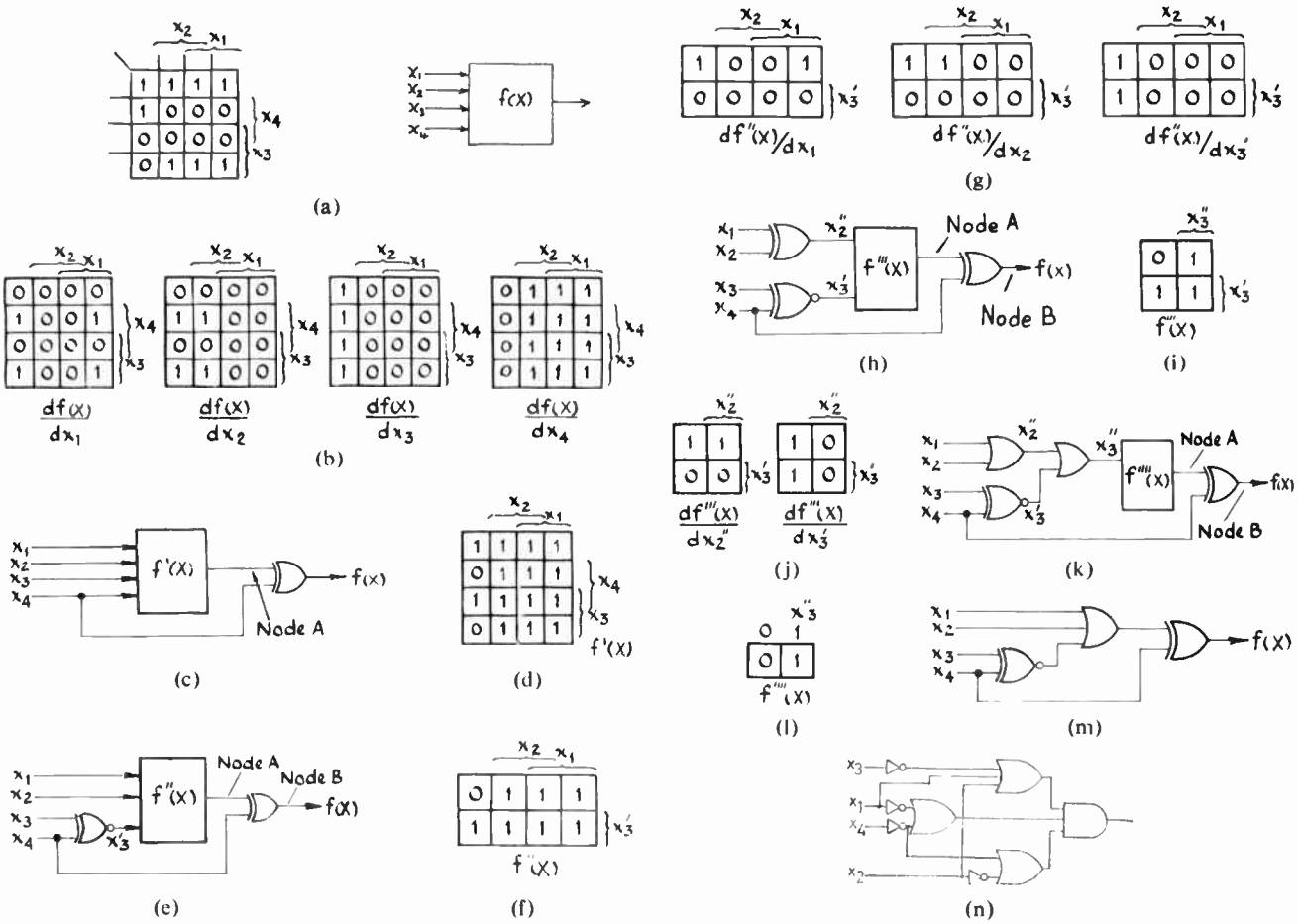


Fig. 22. (a) to (m) Synthesis example using spectral translation. (n) Solution due to Zissos.

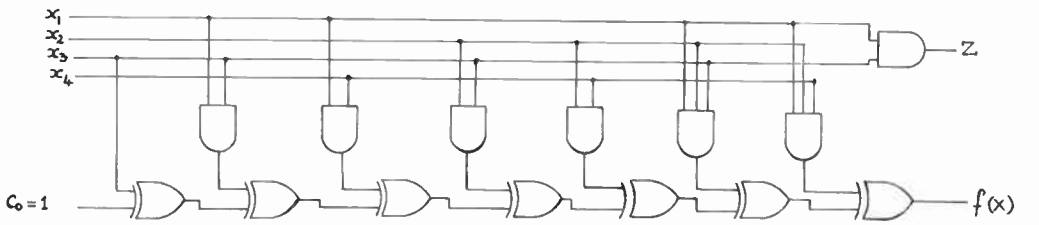


Fig. 23. Reed–Muller implementation.

which may be implemented as shown in Fig. 22(k). The remainder function is shown in Fig. 22(l) and is $f''''(X) = x_3$, that is, x_3 is directly connected to node A. It can be shown that $df''''(X)/d(x_3'') = 1$, this gives:

Fault	Test	
x_3'' (node A) s.a.0	$x_3'' . 1 = (x_3 \overline{\oplus} x_4) + x_1 + x_2 = 1$	(k)
x_3'' (node A) s.a.1	$\bar{x}_3'' . 1 = \overline{(x_3 \overline{\oplus} x_4) + x_1 + x_2} = 1$	(l)

Again this fault may be propagated to the output node B by setting $x_4 = 0$ or $x_4 = 1$.

The final synthesis appears in Fig. 22(m).

As in the previous example, a reduced test set can be generated, namely:

Reduced Test Set				Tests Covered
x_1	x_2	x_3	x_4	
1	0	1	0	(a), (h), (k)
0	0	1	0	(b), (d), (e), (j), (l)
0	1	0	1	(c), (g)
0	0	0	0	(f), (i)

This synthesis may be contrasted with the conventional solution of Zissos[22] shown in Fig. 22(n), which has many more possible 'stuck-at' nodes, greater circuit complexity and a larger Reduced Test Set than the new design.

8.3 Comparison with Other Methods

Reddy[8] has proposed the use of the Reed–Muller expansion to design combinational circuits which may be tested by a set of $(n+4)$ tests. For example, the Reed–Muller expansion of the function shown in Fig. 22(a) is:

$$f(X) = 1 \oplus x_3 \oplus x_1 . x_3 \oplus x_1 . x_4 \oplus x_2 . x_3 \oplus x_2 . x_4 \oplus x_1 . x_2 . x_3 \oplus x_1 . x_2 . x_4$$

The corresponding circuit is shown in Fig. 23. The AND gate connected to output Z is required to detect s.a.0 faults on the primary inputs. This configuration has many disadvantages when compared to the circuit of Fig. 22(m). The circuit complexity and propagation delay are much higher and, because input C_0 and output Z are required for testing, an extra two observable test points are required. In addition the number of tests required (8) is larger than those (4) required for the circuit of Fig. 22(m). The great advantage of the Reed–Muller expansion method is that the required test set is very easily determined. In fact circuits of the Reed–Muller type may be reduced if complementation of input variables is allowed but this procedure is difficult for functions with 'don't-care' states. Similar observations may be applied to the design of circuits using a cellular structure based upon the Reed–Muller expansion.[9]

A method devised by Hayes[6] gives rise to circuits which may be tested using only 5 tests, independent of the number of variables. Unfortunately the complexity of such circuits is very high because the method is restricted to syntheses implemented by two-input NAND gates which have an extra exclusive-OR gate at each input. Additional test inputs are required for each exclusive-OR gate.

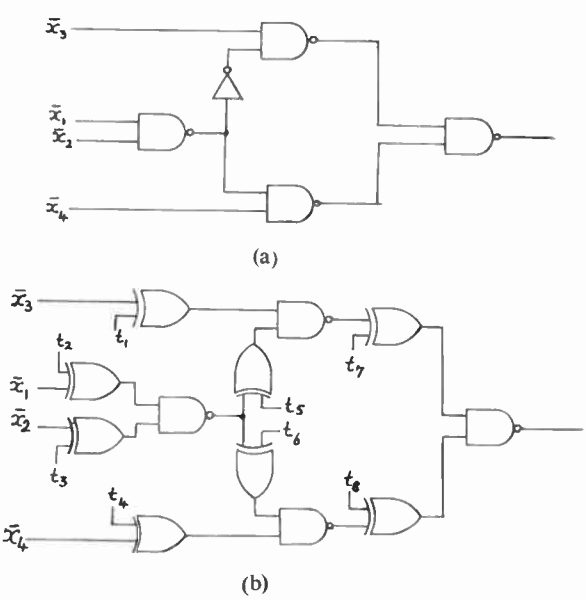


Fig. 24. Method due to Hayes.

Figure 24(a) shows a possible 2-input NAND gate implementation of the function of Fig. 22(m). The circuit, modified to be tested by Hayes' method is shown in Fig. 24(b). Eight extra test points are required, t_1–t_8, and the circuit is very complex. The great advantage of Hayes' method is that both single and multiple 'stuck-at' faults can be detected. Nevertheless the complexity of resultant circuits together with the need for extra test points is likely to prove prohibitive. Similar observations apply to the method proposed by Saluja and Reddy.[7]

9 Discussion

A novel method of designing circuits has been detailed and compared with existing methods. Unlike the methods proposed by other[6–9] authors, the new method produces

circuits which have very few gates and interconnections. The new method does not guarantee to produce circuits with some minimal test set, but to synthesize circuits which are very elegant and are easily tested by:

(a) Substantially reducing the number of possible stuck-at nodes.
(b) Reducing circuit fan-out.
(c) Generating irredundant designs.
(d) Optimally employing exclusive-OR gates—which are easily tested.

In addition the derivation of tests is an integral part of the new design methods.

Other advantages of the method include: the possibility of designing circuits with restricted gate types suited to particular technologies, the optimal implementation of cellular structures and the exploitation of complex gate assemblies. (See Sect. 10.)

Fundamental to the design method is the generation of the Boolean difference. A novel method of deriving these data using the Gibbs Differential[21] has been developed and will be presented in another paper.

10 Further Research

The syntheses and mappings considered thus far have involved simple gates, e.g. AND, OR, exclusive-OR etc. In fact it is sometimes very convenient to be able to design circuits using complex gate configurations; that is, gates which implement mappings normally associated with a mixture of AND, OR and exclusive-OR functions. Such complex gates are usually efficient synthesis modules because they may be very easily fabricated in a particular l.s.i. technology.[12,14] As an example consider the circuit shown in Fig. 25(a) which is easily fabricated in transistor-transistor technology and maps as shown in Fig. 25(b). It should be noted that this mapping is considerably more complex than that generated by simpler gates. (See Appendix 1.) The effect of applying this gate in the synthesis of the function shown in Fig. 25(c) is shown in Fig. 25(d), which is multiform in x_1' and x_3'. The complete solution is shown in Fig. 25(e), the final transistor configuration being a novel exclusive-OR gate.[14]

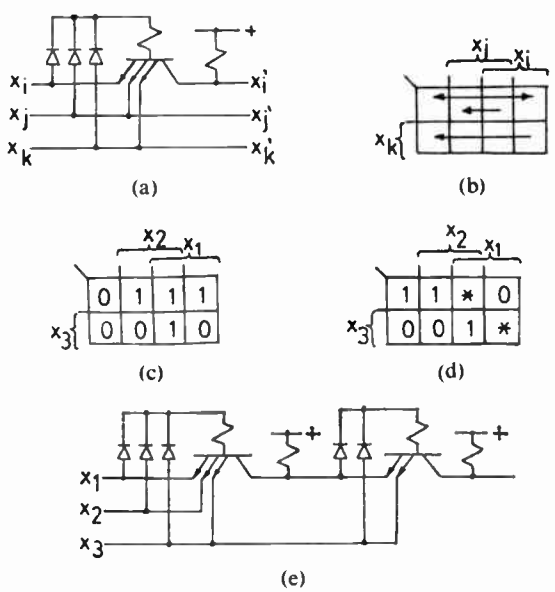


Fig. 25. Complex gates.

This very simple example shows that the method is capable of designing circuits with complex gates suited to particular technologies. It is believed that the method is unique in this respect.

Further research is required to determine the best method of implementing such gates.

Further development of the criteria which determine the most suitable gate implementation at each stage of synthesis is required. (At present, alternatives are exhaustively investigated.)

When the new design methods are employed circuits result which have, in general, larger propagation delays, than conventionally designed circuits. However, these delays generally seem smaller than those arising from the designs aimed at minimal test sequences (Sect. 8.3). From results computed to date, the delay path on an nth order function, assuming any gate type may be employed, has always been less than n gates. This observation needs to be quantified.

It is known that 'hazards' may occur in some of the proposed gate configurations. No account of this has been taken in the circuits described. The question may be asked: can easily tested minimal gate–interconnection hazard-free circuits be designed using the new method?

It is proposed that these methods shall be extended to include the design and testing of finite-state-machines.

11 Acknowledgments

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12 References

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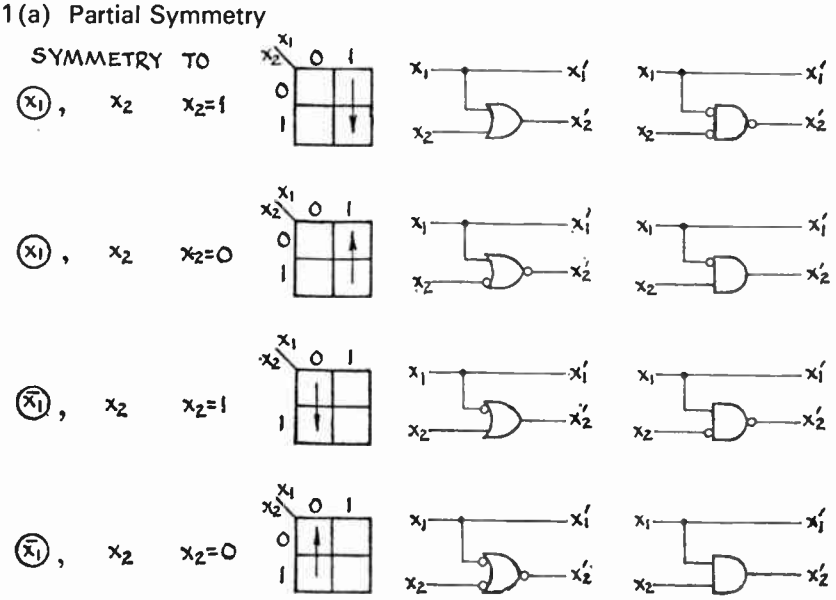
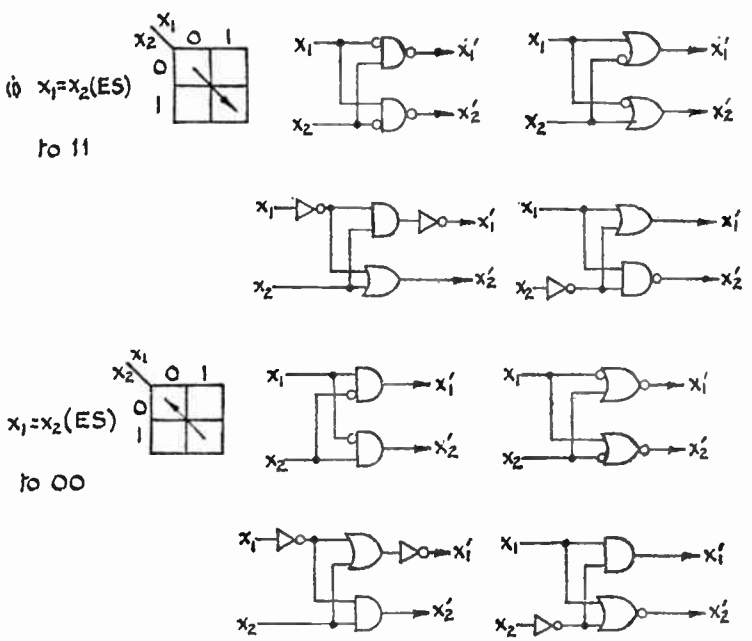
13 Appendix 1

Note.—In the diagrams an encircled symbol represents partial symmetry. i. e.corresponds to x_1 etc. in text.

1(a) Partial Symmetry



1(b) Simple Symmetry



15 Appendix 3: Basic symmetries, their definitions and relationships to the Boolean difference

3.1 Partial Symmetry (P.S.)

(i) Definition:

A function $f(x_1, \ldots, x_i, x_j, \ldots, x_n)$ exhibits partial symmetry (P.S.) in x_i, x_j, if

$$f(x_1, \ldots, 0, 0, \ldots, x_n) = f(x_1, \ldots, 0, 1, \ldots, x_n) \quad (10)$$

or if

$$f(x_1, \ldots, 1, 1, \ldots, x_n) = f(x_1, \ldots, 1, 0, \ldots, x_n) \quad (11)$$

In the first case the function will be said to exhibit partial symmetry for x_j in n-space $x_i = 0$.

In the second case the property is exhibited in n-space $x_i = 1$.

(ii) Illustration:

Figures 4(a) and (b) show equivalent n-spaces.

Figure 4(c) shows a simple example for $n = 4$th-order function exhibiting partial symmetry for x_3 in n-space $x_1 = 0$. (See Appendix 2(a).)

Figures 4(d)–(g) shows some possible implementations of partial symmetry. Further examples are given in Appendix 1(a).

(iii) Notes:

A function exhibiting partial symmetry:

(a) for x_j in n-space $x_i = 0$ will be denoted by $\bar{\mathbf{x}}_i, x_j$ (12)

(b) for x_j in n-space $x_i = 1$ will be denoted by $\mathbf{x}_i, x_j$. (13)

If a function has *both* properties, that is $\bar{\mathbf{x}}_i$, x_j and $\mathbf{x}_i$, x_j, it is *independent* of x_j.

(iv) Definition in terms of Boolean differences:

The simple Boolean difference of a function $f(X)$ with respect to one of its defining variables, x_j, is defined[10] as

$$\frac{\mathrm{d}f(X)}{\mathrm{d}x_j} = [f(x_1, \ldots, x_i, x_j, \ldots, x_n) \oplus f(x_1, \ldots, x_i, \bar{x}_j, \ldots, x_n)].$$

Now consider the function

$$\left\{x_i \cdot \frac{\mathrm{d}f(X)}{\mathrm{d}x_j}\right\} = 0; \quad (14)$$

when $x_i = 0$, $\mathrm{d}f(X)/\mathrm{d}x_j$ may take the value 0 or 1, and thus $f(X)$ may take any value.

However when $x_i = 1$, then $\mathrm{d}f(X)/\mathrm{d}x_j$ must equal 0, and hence

$$f(x_1, \ldots, 1, x_j, \ldots, x_n) = f(x_1, \ldots, 1, \bar{x}_j, \ldots, x_n),$$

that is

$$f(x_1, \ldots, 1, 1, \ldots, x_n) = f(x_1, \ldots, 1, 0, \ldots, x_n).$$

But this is exactly the definition of partial symmetry for $\mathbf{x}_i$, x_j from equation (10). It may be similarly shown that

$$\left\{\bar{x}_i \cdot \frac{\mathrm{d}f(X)}{\mathrm{d}x_j}\right\} = 0 \quad (15)$$

defines the partial symmetry $\bar{\mathbf{x}}_i$, x_j.

3.2 Simple Symmetry

Simple symmetries are divided into two types: *equivalence symmetry* and *non-equivalence symmetry.*

3.2.1 *Equivalence symmetry* (E.S.)

(i) Definition:

A function $f(x_1, \ldots, x_i, x_j, \ldots, x_n)$ exhibits equivalence symmetry in x_i, x_j if

$$f(x_1, \ldots, 0, 0, \ldots, x_n) = f(x_1, \ldots 1, 1, \ldots, x_n). \quad (16)$$

(ii) Illustration:

Figure 5(a) shows equivalent n-spaces.

Figure 5(b) gives a simple example for a $n = 4$th order function E.S. in x_1, x_3, see Appendix 2(b).

(iii) Implementations:

Two E.S. mappings and their possible implementations are shown in Figs. 5(c) and (d).

No variable independencies follow directly from these mappings.

(iv) Notes:

The symmetry is termed 'equivalence' because the function exhibiting this property in x_i, x_j, is the same in n-spaces where x_i is *equal* to x_j. Other possible implementations are shown in Appendix 1(b). E.S. has been considered in Ref. 22. E.S. in x_i, x_j, will be denoted $x_i = x_j$.

(v) Definition in terms of Boolean differences:

The double Boolean difference is defined as

$$\frac{\mathrm{d}f(X)}{\mathrm{d}(x_i, x_j)} = [f(x_1, \ldots, x_i, x_j, \ldots, x_n) \oplus f(x_1, \ldots, \bar{x}_i, \bar{x}_j, \ldots, x_n)] \text{ from (7)}$$

Now consider the function

$$\left\{\overline{(x_i \oplus x_j)} \cdot \frac{\mathrm{d}f(X)}{\mathrm{d}(x_i, x_j)}\right\} = 0. \quad (17)$$

When $x_i \neq x_j$, $\mathrm{d}f(X)/\mathrm{d}(x_i, x_j)$ may take the value 0 or 1 and thus $f(X)$ may take any value.

However, when $x_i = x_j$, then $\mathrm{d}f(X)/\mathrm{d}(x_i, x_j)$ must equal 0, and hence

$$f(x_1, \ldots, x_i, x_j, \ldots, x_n) = f(x_1, \ldots, \bar{x}_i, \bar{x}_j, \ldots, x_n),$$

that is

$$f(x_1, \ldots, 0, 0, \ldots, x_n) = f(x_1, \ldots, 1, 1, \ldots, x_n).$$

But this is exactly the definition of equivalence symmetry given in equation (16), namely $x_i = x_j$.

3.2.2 *Non-equivalence symmetry* (N.E.S.)

(i) Definition:

A function $f(x_1, \ldots, x_i, x_j, \ldots, x_n)$ exhibits non-equivalence symmetry in x_i, x_j, if

$$f(x_1, \ldots, 0, 1, \ldots, x_n) = f(x_1, \ldots, 1, 0, \ldots, x_n) \quad (18)$$

(ii) Illustration:

Figure 6(a) shows equivalent n-spaces.

Figure 6(b) shows a simple example for $n = 4$th order

function N.E.S. in x_1, x_3. (See Appendix 2(b).)

(iii) Implementations:

Two many-one mappings and examples of possible implementations are shown in Figs. 6(c) and (d).

No variable independencies follow directly from these mappings.

(iv) Notes:

The symmetry is termed non-equivalence because the function exhibiting this property in x_i, x_j is the same in n-spaces where x_i is *not equal* to x_j. Another interpretation of N.E.S. is that the function remains the same under the interchange of variables x_i, x_j. Other possible implementations are shown in Appendix 1(b). N.E.S. has been considered in Ref. 22. N.E.S. in x_i, x_j, will be denoted $x_i \neq x_j$.

(v) Definition in terms of Boolean differences:

In a similar manner to that proved for equivalence symmetry, it may be shown that

$$\left\{(x_i \oplus x_j) \cdot \frac{df(X)}{d(x_i, x_j)}\right\} = 0 \qquad (19)$$

defines the non-equivalence symmetry of equation (18), namely $x_i \neq x_j$.

3.3 Multiform Symmetry (M.F.S.)

A function which exhibits both equivalence *and* non-equivalence symmetry in x_i, x_j, is multiform symmetric in x_i, x_j. This follows directly from equations (16), (17) and (18). Functions multiform symmetric in x_i, x_j, are thus denoted as $x_i \overset{=}{\neq} x_j$.

(i) Definition:

A function $f(x_i, \ldots, x_i, x_j, \ldots, x_n)$ exhibits multiform symmetry in x_i, x_j if

$$\left.\begin{aligned} &f(x_1, \ldots, 0, 0, \ldots, x_n) = f(x_1, \ldots, 1, 1, \ldots, x_n) \\ &\text{and} \\ &f(x_1, \ldots, 0, 1, \ldots, x_n) = f(x_1, \ldots, 1, 0, \ldots, x_n) \end{aligned}\right\} \qquad (20)$$

(ii) Illustration:

Figure 7(a) shows equivalent n-spaces.

Figure 7(b) gives a simple example for a $n = 4$th order function M.F.S. in x_1, x_3. Note that the unspecified value at $x_1.x_2.x_3.\bar{x}_4$ matches with '1' at $\bar{x}_1.x_2.\bar{x}_3.\bar{x}_4$. (See Appendix 2(c).)

(iii). Implementations:

Possible many-one mappings and their circuit implementations are shown in Figs. 7(c) to (f). Note that Figs. 7(c), (f) and also (d), (e) are trivially related by variable interchange; (c) and (d) suffice for synthesis purposes.

These implementations generate a one-variable redundancy.

(iv) Notes:

This symmetry form gives rise to the efficient utilization of the exclusive exclusive-OR(NOR) gate. M.F.S. has been considered in Ref. 22.

M.F.S. in x_i, x_j, will be written as $x_i \overset{=}{\neq} x_j$ for reasons given above.

(v) Definition in terms of Boolean differences:

Multiform symmetries of the type $x_i \overset{=}{\neq} x_j$ may be defined by:

$$\left\{(x_i \oplus x_j) \cdot \frac{df(X)}{d(x_i, x_j)}\right\} = \left\{\overline{(x_i \oplus x_j)} \cdot \frac{df(X)}{d(x_i, x_j)}\right\} = 0, \qquad (21)$$

whence it follows that $df(X)/d(x_i, x_j)$ must equal 0.

Proof follows from the two simple symmetry developments (Appendices 3.2.1 and 3.2.2).

3.4 Compatible Symmetry (C.S.)

(i) Definitions:

Clearly it is possible for a function to exhibit partial symmetry, in say x_i, x_j, in different ways:

(a) x_i, x_j and $\bar{x}_i$, x_j (=independent of variable x_j)
(b) x_i, x_j and x_j, x_i See Fig. 8(a)
(c) x_i, x_j and $\bar{x}_j$, x_i See Fig. 8(b)
(d) $\bar{x}_i$, x_j and $\bar{x}_j$, x_i See Fig. 8(c)
(e) $\bar{x}_i$, x_j and x_j, x_i See Fig. 8(d)

Each of these cases with the exception of the trivial case (a) will be said to exhibit compatible symmetry.

Now if a function is completely specified (contains no unspecified states), then criteria (b) to (e) suffice to guarantee compatibility. On the other hand for functions with certain unspecified (don't care) states these criteria are not sufficient. Figure 8(e) shows an example of a function of the latter type (c.f. Fig. 8(a)), which has partial symmetries x_i, x_j; x_j, x_i. However in Fig. 8(e)

x_i, x_j constrains $*$ to be 1

and

x_j, x_i constrains $*$ to be 0; the symmetries are thus *not* compatible since $*$ cannot simultaneously take logical values 0 and 1.

A necessary and sufficient method of checking such ambiguous cases for compatibility is to include the criterion of simple symmetry. In the case of Fig. 8(a) the simple symmetry $x_i \neq x_j$ must be included (Fig. 8(f)).

This is illustrated in Fig. 9. (Note that in Fig. 8, symmetries 8(b) and 8(d) are essentially the same, but x_i and x_j have been interchanged; this case is thus omitted in Fig. 9.)

The compatible symmetries may be summarized as:

Partial symmetries		Simple symmetry	
x_i, x_j	x_j, x_i	$x_i \neq x_j$	(22)
x_i, x_j	$\bar{x}_j, x_i$	$x_i = x_j$	(23)
$\bar{x}_i, x_j$	$\bar{x}_j, x_i$	$x_i \neq x_j$	(24)

It should be noted that a variable redundancy results from the implementation of compatible symmetry.

Further possible implementations are shown in Appendix 1(d).

(ii) Definition in terms of Boolean differences:

Compatible symmetries of the type x_i, x_j and x_j, x_i may be defined as

$$\left\{x_i \cdot \frac{df(X)}{dx_j}\right\} = \left\{x_j \cdot \frac{df(X)}{dx_i}\right\} = 0 \qquad (25)$$

and so on.

3.5 Definition of Spectral Translation in terms of the Boolean Difference

One-to-one mappings or spectral translation may also be expressed using the Boolean difference. The mapping which replaces x_j by $[x_i \oplus x_j]$ may be defined as

$$\left\{\left\{x_i \cdot \frac{df(X)}{dx_j}\right\} \oplus f(X)\right\}. \qquad (26)$$

3.6 Definition of Disjoint Spectral Translation in terms of the Boolean Difference

Since, by definition, $[f'(x_1, \ldots, x_k, \ldots, x_n) \oplus x_k] = f(x_1, \ldots, x_k, \ldots, x_n)$,

$$\frac{df(X)}{d\{f'(X)\}} = 1. \qquad (27)$$

Thus from Fig. 12(b),

$$\frac{df(X)}{dA} = 1$$

and also

$$\frac{df(X)}{dx_k} = 1.$$

Manuscript first received by the Institution on 5th August 1976 and in revised form on 26th January 1977 (Paper No. 1776/Comp. 181).

The Author

C. R. Edwards received the degrees of B.Sc. and Ph.D. in electrical engineering from the University of Bath, in 1970 and 1974 respectively. His Ph.D. thesis was based upon research into the application of matrix methods to the design of combinational logic circuits. He is at present a Research Fellow of The University of Bath where his research interests include the application of spectral techniques to the design of digital integrated circuits, computer-aided logic design and automatic circuit testing. Dr. Edwards is the author of 13 published papers in the digital design field and he has originated several patent applications.

IERE News and Commentary

The Institution's Library

The Institution's Library at 9 Bedford Square will be closed for reorganisation and relocation from Monday, 29th August—Friday, 23rd September inclusive. During this period, however, the Librarian will be available to meet members' urgent reference requirements and research enquiries. Any such urgent requirements should be notified initially to Mr F. W. Sharp at Bedford Square, telephone 01-637 2771, extension 1.

Institution Meetings For The 1977/78 Session

The coming session of Lecture Meetings and Colloquia promises to be more than usually interesting and it is hoped that this preview will serve to whet members' appetite; fuller details are, of course, published regularly a few weeks beforehand in *The Radio and Electronic Engineer* as well as being publicized by means of posters, regional programme cards and booklets, and meeting notices. Mention of meeting notices serves as a reminder to draw members' attention to a feature first published in the July 1975 issue of the Journal and repeated every few months which describes the activities of the Institution's Specialized Groups and Local Sections. This feature included amongst other things, a request form enabling members to indicate which Group's and Local Section's activities they would wish to receive details.

The first meeting of the session is unusual in that it is not being held in London but in the county of Avon. The Education and Training Group are continuing their series of colloquia with the general theme of 'Training' and an all-day meeting, 'Training Technicians in Engineering', will be held at RAF Locking, Weston-Super-Mare on Wednesday, 28th September. Full details of the programme and registration procedure are available upon request.

The London Meetings will start, as is customary, with the Annual General Meeting. Apart from the usual business transacted on this occasion members will also have a chance to meet both the incoming President, Professor Alec Gambling and the new Secretary of the Institution, Air Vice-Marshal Sinclair Davidson. The A.G.M. will be held in the Goldsmiths' Theatre of the London School of Hygiene and Tropical Medicine, Keppel Street, (off Gower Street), WC1, on Thursday, 13th October at 6 p.m. Tea will be served from 5.30 p.m. onwards in the refectory.

The first London colloquium of the session 'A Comparison of SAW, CCD and Digital Technologies', will be held on October 18th at the Royal Institution, Albemarle Street, W1. The meeting, a follow-up to one on SAWs held a year or so ago, will commence at 2 p.m.

On November 1st, the Automation and Control Systems Group are presenting a colloquium on 'Laboratory Automation'. The six speakers will come from widely different backgrounds and can be expected between them to have many ideas on aspects of the automation of quite different equipments. Two weeks later, on November 15th, the Components and Circuits Group is organizing an all-day meeting on 'Analogue Filters'; the speakers will include representatives from universities and from industry. The following week, on November 22nd, the Aerospace, Maritime and Military Systems Group, in conjunction with the Communications Group, is organizing a half-day meeting entitled 'Portable Communications Systems'. On November 29th, the joint IEE/IERE Computer Group will discuss 'Electronic Security and Personal Access Systems'. Methods of regulating personal access to premises, money, goods or services have hitherto been the province of human operators (who easily become inattentive), supplemented by a variety of mechanical and electro-mechanical techniques. Modern semiconductor technology is increasingly providing solutions to such problems and this colloquium will examine in detail many of the latest developments in the field of what may loosely be termed access control. Examples include the incorporation of l.s.i. chips in cash dispensers, automatic car park controls and public telephones, and in the readers for railway tickets, cash cards and security passes. The colloquium should prove of interest to all who have any dealings whatsoever with any aspect of 'Security'—which includes most of us! The last London meeting of 1977 is a colloquium on December 6th, entitled 'New Electronic Techniques as Aids to Production'. This meeting, which is being organized by the Electronics Production Technology Group, is aimed at production engineers and managers.

The first half session extends to the end of January 1978 and plans have already been made for colloquia to be held on the following topics: Measurements and Pollution, Interworking between P.C.M. and F.D.M. systems, and Communications between Engineers and the Outside World; also, an evening lecture meeting, 'Highways and Byways of Ultrasonics' will be given by A. E. Crawford of the DDS Engineering Co. Ltd.

Further details of the earlier meetings are given on page 350 of this issue and information on subsequent events will be given in latter issues of the Journal.

Health and Safety and the Engineer

Engineers are the largest single body to be brought within the scope of the Health and Safety at Work, etc., Act 1974 and for this reason CEI viewed the absence of an engineer from the policy-making committees of the Commission and its Executive with grave concern.

CEI's Health and Safety Committee was established in the Autumn of 1975, its terms of reference being:

1. To co-ordinate the work of individual committees/panels, within Constituent Members, that deal with matters related to Health and Safety.
2. To make recommendations to the Executive Committee of the CEI on the role and policy of the engineering profession in the field of Health and Safety.
3. To make recommendations for dealing with matters in detail, affecting the engineering profession as a whole, that stem from the Health and Safety Act 1974 and similar legislation.

In the CEI Annual Report for 1976, it is pointed out that representations are continuing to be made, to have the ninth

place on the Commission, at present unfilled, allocated to a representative of CEI. With the absence of professional advice it is felt that the full implications of Section 6 of the Act are not appreciated by the Health and Safety Executive nor is there adequate understanding of the role of Codes of Practice and Standards in Engineering. It has not been clear how these last will be related to the approved Codes which the Health and Safety Executive intends to issue, neither is it clear by what machinery they are to be prepared.

The Committee therefore met Mr J. H. Locke, Director General, Health and Safety Executive in July 1976, in order to discuss its apprehensions and it was learnt that the Executive has been concentrating on creating a viable organization and is now preparing a list of activities which will occupy it over the next five years. This list has been issued as a consultative document and is being considered by the Committee. Mr Locke stated that he will be looking to the chartered engineering institutions as a source of expert advice in the matters to which the Executive has to give attention.

A representative of the Committee gave evidence to the Health and Safety Commission's Sub-Committee on Major Hazards set up to report on the operation of hazardous processes. He was mainly questioned on the views of the Council on the registration and certification of engineers engaged in these processes. The First Report of the Advisory Committee on Major Hazards has been issued for comment but there is no reference to registration or certification, merely to 'competent people'. The question of registration and certification of engineers engaged in chemical processes has been examined by the Institution of Chemical Engineers.

Representatives of the Committee met Mr Locke and Mr D. Richardson, Director of the Safety and General Group of the Executive, to discuss safety training for engineers and representation of the profession on the Industry Advisory Committees set up by the Health and Safety Executive. The importance attached by the Council to post-graduate training of engineers in the practice of engineering was explained and the relevance of this to any scheme of registration discussed as well as the difficulties inherent in any such scheme. The need for independent professional advice to be made available to the Industry Advisory Committees was stressed. The Health and Safety Executive consider however that this would be made available to them through technical sub-committees that would be appointed with the help of the engineering institutions.

Comment was made by the Committee on draft legislation on noise prepared by the Health and Safety Executive. The Committee is unhappy about the process of consultation adopted by government bodies in that the very wide dissemination of papers and the brief periods of time allowed for comment scarcely represents consultation where matters of critical technical import are involved.

The Institutions' member on the CEI Health and Safety Committee is Colonel Frank Spragg who will be pleased to hear from any member wishing to raise matters of relevance to the Committee's terms of reference. His address is: Colonel F. R. Spragg, C.Eng., F.I.E.R.E., School of Electronic Engineering, Arborfield, Reading, RG2 9NH. (Telephone: Arborfield Cross 760421, Ext. 330).

Standard Frequency Transmissions—May 1977

(Communication from the National Physical Laboratory)

May 1977	Relative Phase Readings in Microseconds NPL—Station (Readings at 1500 UT)		
	MSF 60 kHz	GBR 16 kHz	Droitwich 200 kHz
1	5·7	6·5	4·8
2	5·7	6·8	6·6
3	5·6	6·6	8·0
4	5·8	6·3	9·4
5	5·8	6·4	10·6
6	6·0	6·3	11·7
7	5·8	6·3	12·6
8	5·8	6·3	13·4
9	6·0	6·4	14·4
10	5·8	6·5	15·5
11	6·0	6·3	17·0
12	5·8	6·3	18·3
13	6·0	6·5	19·8
14	5·5	6·3	20·8
15	5·8	6·5	21·8
16	5·9	6·4	23·5
17	6·1	6·5	24·7
18	6·0	6·4	26·0
19	6·0	6·3	27·5
20	6·3	6·4	28·9
21	6·3	6·4	29·9
22	6·3	6·4	31·0
23	6·3	6·5	31·7
24	6·3	6·4	31·4
25	6·5	6·6	31·2
26	6·4	6·5	30·9
27	6·6	6·5	30·9
28	6·3	6·4	31·2
29	6·5	6·4	31·5
30	6·3	6·4	31·3
31	6·1	6·0	31·0

Notes: (a) Relative to UTC scale (UTC_{NPL}–Station) = +10 at 1500 UT, 1st January 1977.

(b) The convention followed is that a decrease in phase reading represents an increase in frequency.

(c) Phase differences may be converted to frequency differences by using fact that 1 μs represents a frequency change of 1 part in 10^{11} per day.

Preparation for the CEI Part 2 Academic Test

As those Graduate members who have consulted the Institution are already aware, courses of preparation for the CEI Part 2 Academic Test are few and far between. We are therefore pleased to be able to report that North East London Polytechnic has indicated willingness to offer a course in the 1977/78 session if the demand is sufficient. The course could be on a one day or two evenings per week basis. Inevitably the choice of subjects offered would be limited: tentatively, it has been suggested that they might be:

300 The Engineer in Society

341 Electromagnetic Fields and Networks

345 Electronic Engineering

346 Computer Engineering

The Polytechnic will, however, be willing to consider other groupings if there is sufficient demand. Graduate members who have not yet consulted the Institution may be interested to know that, because of the problems of preparation for the Test, it will now accept 'The Engineer in Society' provided the other subject offered is 'Electronic Engineering'.

All Graduate members interested in the possible course should communicate as soon as possible with:

The Engineering Faculty Registrar, North East London Polytechnic, Longbridge Road, Dagenham, Essex, RM8 2AS (Tel: 01-590 8007)

Engineering Profession Inquiry

Mr Eric Varley, Secretary of State for Industry, in answer to a Parliamentary Question from Mr Arthur Palmer, C.Eng., MP (Bristol, North East), told the House of Commons on July 5th:

'I have decided to appoint a Committee of Inquiry with the following terms of reference:

'To review for manufacturing industry, and in the light of national economic needs—

(i) the requirements of British industry for professional and technician engineers, the extent to which these needs are being met, and the use made of engineers by industry;

(ii) the role of the engineering institutions in relation to the education and qualification of engineers at professional and technician level;

(iii) the advantages and disadvantages of statutory registration and licensing of engineers in the UK;

(iv) the arrangements in other major industrial countries, particularly in the EEC, for handling these problems, having regard to relevant comparative studies, and to make recommendations.

'I am glad to say that Sir Montague Finniston has accepted my invitation to chair the committee. I am certain that the inquiry will not impede the many useful initiatives already in existence or planned, both inside and outside the Government; rather I see the inquiry as building on these initiatives and drawing together the results. It is my intention that this inquiry should not be unduly prolonged and I will keep the House fully informed of progress.'

Commenting on the Secretary of State's announcement, Sir Charles Pringle, Chairman of the Council of Engineering Institutions said that the announcement removed the uncertainty which had been handing over the profession for too long. Whilst CEI had always questioned the need for such an inquiry, if it did anything to improve the public standing of engineers then it would be well worthwhile. He continued:

'CEI will, of course, co-operate fully with the Committee under the chairmanship of Sir Monty Finniston whose appointment we particularly welcome since he is, himself, an engineer with a very wide experience in industry.

'We are aware that the setting up of the inquiry is not to be taken in any way as a criticism of the engineering profession as a whole or of the very high reputation of British engineers throughout the world.

'We are glad that the Secretary of State's announcement recognizes that it is important that initiatives already in existence or planned shall not be impeded by the inquiry and that the Committee's deliberations shall not be prolonged.'

New Director for National Physical Laboratory

Mr Eric Varley, the Secretary of State for Industry, has approved the appointment of Dr Paul Dean as Director of the National Physical Laboratory. He is succeeding Sir Ieuan Maddock, C.B., O.B.E., F.R.S. who has been in charge of the National Physical Laboratory since giving up his appointment as the Department's Chief Scientist and who has now retired from the public service. Dr Dean who will take up his appointment on 1st October 1977 joined the National Physical Laboratory in 1957 in the Theoretical Physics Section of the Mathematics Division and was later Head of the Central Computer Unit and of the Quantum Metrology Division before becoming a Deputy Director of the Laboratory in 1974. On promotion to Under Secretary in 1976 he moved to the Headquarters of the Department of Industry as Head of the Space and Air Research and of the Research and Development Contractors Division. He is a graduate of Queen Mary College, London University.

Belated Tribute to a Genius: Alan Dower Blumlein 1903-1942

On 1st June 1977, a commemorative blue plaque, erected by the Greater London Council, was unveiled at 37 The Ridings, Ealing, in West London, the home of the electronics engineer, Alan Dower Blumlein. One of the most outstanding engineers of his generation, Blumlein has never received the public recognition which he deserves for his revolutionary work in the fields of telephone engineering, gramophone recording, stereophonic sound, television and airborne radar, most of it carried out at EMI's Research Laboratories at Hayes, Middlesex. Indeed many electronics engineers of today are unaware of his contributions which is strange even allowing for the wartime secrecy which the circumstances of his death made necessary.

Just 35 years previously, on 7th June 1942, an RAF *Halifax* aircraft carrying experimental H2S radar equipment crashed in the foothills of the Welsh Black Mountains. All eleven on board were killed, including three civilian scientists from EMI Research Laboratories at Hayes, among them A. D. Blumlein. Because of the nature of the equipment and his work, only the barest mention of his death was made.

In his short professional career of less than 18 years Blumlein had, among other things, commissioned the first trans-European high-quality telephone lines, invented the closely-coupled inductor ratio arm bridge (both while with International Western Electric, now ST&C), devised and set to work the first electromagnetic sound recording system, laid the foundations for the current methods of stereo recording on disk, formulated the transmission standards for the British 405-line television system (the first public high-definition system in the world, still in use today) and made significant contributions to radar technology, particularly airborne radar. Between 1927 and 1942 he was granted 125 patents (plus 3 posthumously) either as sole patentee or in association with others.

The variety of Blumlein's circuit developments alone is incredibly large: scanning and synch. separator circuits, stabilized h.t. and e.h.t., cathode-follower and a.g.c. improvements, filters, delay-lines, time-bases, long-tail pair, Miller-effect integrator etc. and these were also electro-mechanical and mechanical inventions. But it is probably even more significant that, as was pointed out at the ceremony by Dr Percy Allaway, Chairman of EMI Electronics (President of the IERE) and underlined by Sir Alan Hodgkin, F.R.S., Nobel Laureate and a wartime associate of Blumlein, who unveiled the plaque, he may truly be regarded as the first 'systems engineer'. Stereophony (or binaural sound as he called it), a low level altimeter, high-definition television, airborne radar were some areas in which his multi-disciplinary approach was so fruitful.

An interesting and comprehensive short article on A. D. Blumlein was contributed by B. J. Benzimra to *Electronics and Power* in June 1967 and will no doubt arouse anticipation for the definitive biography which is being prepared by Mr F. P. Thomson (a Member of the IERE). It was in fact through Mr Thomson's initiative that this belated tribute by the commemorative plaque was realized.

Eurocon 77

European Conference on Communications

Venice 3rd to 6th May 1977

Organized jointly by EUREL Convention of National Societies of Electrical and Engineers of Western Europe) and the Institute of Electrical and Electronics Engineers in association with the International Union of Radio Science (URSI) and the Associazione Elettrotecnica ed Elettronica Italiana.

Venice, which has for centuries acted as a bridge between Europe and the East, became for a few days the meeting point for electronic engineers and scientists from all over the world who gathered in a cultural centre on the historically notable Isola di San Giorgio Maggiore, to participate in a cross-fertilization of scientific knowledge in an academic environment enriched by the Adriatic springtime.

A refreshing aspect of the organization was the liberal interpretation of the term 'communications' which was extended beyond the traditional frontiers of definition to embrace not only telephone and radio communications, but also audio and video distribution by metallic and fibre optical cables with particular emphasis on bilateral video transmission, satellite communications, data processing and computer technology as applied to a wide range of disciplines including medicine, and the increasing impact of telecommunications upon electrical energy production and distribution. Special consideration was given to the problems of communications in developing countries and to those of the student and newly qualified engineer.

More than 500 men and women of no less than 32 nations and from every continent attended the conference, the official language of which was English.

After formal but very cordial welcoming addresses on behalf of the Italian Government, the Fondazione Cini, the City of Venice and the sponsoring organizations, Professor Diodata Gagliardi, Central Director of ASST (Azienda di Stato per i Servizi Telefonici), presented the opening lecture on 'The Evolution of Communications: Technical Aspects and Social Incidence' in which he identified the sociological impact of recent electrotechnological advances and envisaged the acquisition of data at its source, such as by the use of mini-computers within domestic energy meters.

As a commencement to the academic proceedings, Dr A. A. L. Reid of the British Post Office Telecommunications Strategy Department gave an invited paper on 'The Long Term Demand for, and Planning of, New Telecommunications Services'. He discussed the effects on long term planning arising from the conflict between 'uncertainty' and 'inertia'. The former was said to stem from factors such as the prevailing economic situation, political philosophies and social patterns which in some respects can dictate the impetus of technological change. Inertia was dominated by multi-million pound capital investment in existing plant that could not be replaced without major adverse consequences, the resultant requirement for compatibility between old and new technologies, state monopolies and the interaction between national and international systems, all of which militate towards a slow rate of change. On a philosophical note Dr Reid pondered over a possible correlation between this monolithic inertia and the two years of additional longevity enjoyed on average by certain employees of the British Post Office.

Obviously it was not possible for any participant to attend anything more than a cross-sectional proportion of the total number of talks, which were of necessity time-scheduled in parallel. This summary will therefore refer to but a few representative examples of the papers which I was privileged to hear or to discuss informally.

Under the title 'Ground-to-train telecommunication system for a.c. electrical traction railways', two authors from Telettra explained how duplex two-way speech plus control and alarm data is possible between moving trains and fixed base centres, by using the railtrack as the radiating element of a communications network. It is understood to be applicable also to d.c. traction systems.

F. Crofts of the British C.E.G.B. described 'A radiating cable communication system for a tunnel carrying 400 kV cables under the Rivers Severn and Wye'. Unlike the conclusions of some recent researchers involved with this important subject which indicate frequencies around 3 MHz for optimum efficiency, this paper described a functional system operating on about 85 MHz based on commercially available hand-portable radio transceivers.

A Dutch paper 'Earth station antennae with reduced side lobes and maximum G/T yield' outlined the results of a joint technical study by France, Italy, the Netherlands, Switzerland and Yugoslavia towards the design of a high efficiency earth station antenna. This is for use with satellites operating on frequencies in the 10–14 GHz region and has minimal side lobes to help minimize intreference between neighbouring satellites. Reference was made to the cumbersome administrative machinery of such a cooperative venture and how results were forthcoming only when the technical experts got together. Their choice of the Cassegrain system was clearly explained by a well illustrated comparison between the centre fed parabolic antenna, the horn antenna with off-set feed and the Cassegrain antenna. Field perturbation from antenna feed-supporting struts was dealt with later in greater detail in a supporting paper on 'An approach to blocked aperture synthesis'.

A fascinating practical application of voice-synthesis by electronic technology to a real life telephone system was described in a French paper. On receipt of a dialled number which has been changed, the caller is told the correct number in plain language via a central computer. Clearly not so easy as it sounds, but due for active service in 1978.

'Viewdata—a computer based visual information and communications system with interactive capabilities' was one of a number of excellent papers on tele-visual data systems. The faultless demonstration by S. Fedida of the British Post Office of active hardware which accompanied the presentation made a noticeable impact on an intensely interested audience.

During the Communications and Computers sessions I was most interested in a well-planned live demonstration of EIN, the European Informatics Network, in action. Basically this is a computer terminal linked by land-line to a variety of computer systems in a number of different countries within the European Economic Community, via a network established jointly by member nations, from which

to gain a working knowledge of the use of computers in a data communications network. Implicit in the use herein of the term 'computer systems' is intercommunication between equipment by different manufacturers and access to a host of data banks and processing resources. It is too vast a subject to consider in depth within the scope of this commentary, but an experiment was made whereby an attempt was made to gain access to a computer in Milan, which was found to be occupied, but which automatically transferred the request to a computer at the N.P.L. in England, where it was validated.

It is generally believed that repetitive exposure to X-ray radiation has a cumulative adverse effect on human physiology, and yet it is sometimes necessary to apply such techniques for clinical diagnosis. A paper from the University of Turin proposed a method by which cardiovascular motion may be observed, based on the use of a television camera and videotape recorder, so reducing the levels of X-ray exposure required for the more conventional ' kimography' technique.

Although not very obvious from the complex title of 'Analog image processing by a photographic spatial filtering technique', another Italian paper gave a practical description of how to sharpen up the contours or changes in contrast of a photographic image, with particular emphasis on the new application of a well-known technique to the visual anlysis of clinical X-ray films. Its effectiveness was convincingly demonstrated.

'A system for the computer analysis of chromosome autoradiographs', from the University of Saskatchewan clearly dealt with a very specialized field of physiological investigation but it was expertly presented in unambiguous terms. It described a successful attempt to automate the hitherto tedious manual analysis of large quantities of microphotographic-X-ray images of chromosomes.

An entire day was devoted to the vital topic of 'Communications in the Developing Countries', the opening session of which was chaired by B.S. Rao of the Indian Space Research Organization and the inaugural address was by M. Mili, Secretary General, International Telecommunication Union (ITU). Subsequent session titles give an idea of its scope:

Problems and possible Solutions in the Development of Communications with particular reference to Developing Countries;

Techno-economic Problems and Needs of Communication Development in the Developing Countries;

Worldwide Assistance Programmes Aimed at Communications Development in Developing Countries, including Training, Maintenance and Operation;

Industrial Approaches Suited for Developing Countries;

and Impact of Satellite Technology for Different Applications.

Three of the papers in these sessions were particularly notable. Speaking from a background of related experience in Nigeria, ' Communications in Developing Countries (E. M. Hicken, Microwave Associates Ltd. Great Britain) was deliberately couched in provocative terms intended to promote discussion. It included debatable proposals for radio frequency band planning with emphasis on the use of a multiplicity of low capacity systems. A lively and informative discussion was generated.

In 'Small receive-only terminals for broadcast satellites' (J. W. Edens, Philips Research Laboratories, The Netherlands) the experimental results of reception of television signals from satellites on 2·6 and 12 GHz, using a simple low cost antennae, with frequency conversion to provide direct input to domestic television receivers were discussed.*

'Image data security in the concept of the (ARTISS) Agricultural Realtime Image Receiving Satellite System' (H. A. Van Ingen Schenau, L. J. M. Joosten and J. L. Simmons, National Aerospace Laboratory, The Netherlands) described the extraordinary and almost unbelievable precautions and facilities to be incorporated into this Earth's resources observational satellite to ensure that its image data will be available only to designated users. Although said to have been designed specifically for developing countries, its restrictive concept evoked a strong critical reaction from representatives of the intended user nations.

In many respects the late evening open forum following these sessions was the highlight of the conference. It commenced with brief talks by engineers from India, Brazil, Japan, the USA and Chile and developed into a frank exchange of viewpoints, many of which were delivered with eloquence and confidence.

For example, in response to a description by P. Van der Veen of Hughes Aircraft Corporation of the recently commissioned duo-satellite system which is now providing total communications coverage to the Indonesian islands, the Indonesian spokesman was quick to emphasize that we must not forget that his country was in a privileged position of economic strength, unlike that of many nations who were not only without adequate resources, but were also unaware of how to ask for and of whom to seek assistance and guidance.

The expositions by I. K. Gupta of India and Kresch Roberto of Brazil described with clarity and justifiable pride the outstanding progress of their own countries in the provision of a viable telecommunications service in a very short time span, starting as they did from little more than an absolutely basic nucleus.

Overall this was a most successful and fruitful conference in that it stimulated the production of a large number of useful papers on a wide range of scientific topics which might otherwise have remained unpublished and it demonstrably promoted the establishment of many close and hopefully long-lasting personal relationships between engineering scientists from many parts of the world.

E. CHICKEN

* See also, for instance, K. G. Freeman, ' Experimental direct broadcast reception of 12 GHz television signals from the Canadian Communications Satellite,' *The Radio and Electronic Engineer*, 47, pp. 234-6, May 1977.

The complete Conference Proceedings 'Communications' are published in 2 volumes (1357 pages), containing more than 200 papers in English. A limited number of copies are available from Associazione Elettrotecnica ed Elettronica Italiana, Viale Monza 259, I-20126 Milano (Telex: Milano 33207; Telephone: Milano 2550642) at a price of $50 (for the two volumes).

World Administrative Radio Conference 1979

In September 1979 a World Administrative Radio Conference (WARC) is being convened in Geneva by the International Telecommunication Union for the purpose of revising, where necessary, the international Radio Regulations. The last conference was almost twenty years ago, and the most important task of the Conference will be to amend the international Frequency Allocation Table (Article 5 of the Radio Regulations) to take account of the changing frequency requirements of the various radiocommunication services and to meet any additional frequency requirements likely to arise in those services up to the end of this century.

The United Kingdom delegation to the WARC will contain representatives of different interests, many of which have already indicated to the Home Office the ways in which they feel the present frequency allocations should be revised to meet their needs. The Home Office is the Government department responsible for radio regulatory matters in the United Kingdom and as such is responsible for preparing the UK proposals to the Conference. This preparation will involve the co-ordination and, in many cases, the reconciliation of conflicting interests between different services.

On 26th January 1977 the Home Secretary, in a written reply to a Parliamentary question, announced that he was widening the field of consultation to include any organization or individual whose interests might be affected by the results of the conference but comments from members of the public were also invited. There had been some criticism in the technical press and elsewhere that consultation had up to that time covered too narrow a field.

These matters have closely occupied the attention of the IERE Council and its relevant Committees in the light of comments on the important issues involved which have been made by members in areas having possibly mutually conflicting professional interests, e.g. civil versus military, point-to-point communications versus broadcasting, fixed versus mobile, users versus industry, technical versus commercial etc. It was however generally felt that the Institution would be failing in its aims and objects if it did not bring forward broad principles associated with good engineering practice to assist the Home Office in presenting well-thought-out UK proposals for the Conference.

The following submission has therefore been sent to the Home Office as the IERE contribution to achieving a successful Conference.

'The Institution of Electronic and Radio Engineers takes the view that the effective exploitation of radio as a natural resource will be of primary economic importance in the years ahead, as well as making a major impact on the quality of life. Because the electromagnetic spectrum is limited in extent, so far as use for radio is concerned, congestion is already serious on some bands, and general congestion at all radio frequencies can be expected to develop over the next quarter century unless steps are taken to alleviate the situation.

'The principal matter for debate is the means by which the developing congestion may best be moderated. In the opinion of the Institution there are very many possible technical advances, already known in principle, which could lead to substantially more economical use of the spectrum, and it is essentially towards technical solutions to this problem that we should look. To this end, regulation of use of the radio bands should, above all, not be such as to discourage technical innovation. In particular we deprecate attempts to dictate in detail the technical characteristics of radio systems in such a way as to inhibit new developments.

'The Institution also wishes to support the framing of policies in the most liberal spirit so far as encouraging radio use is concerned, since it is convinced that to attempt to combat congestion by a restrictive attitude to future use, for example by denying allocations to particular classes of users, will be economically damaging. It appears better in the national interest to make radio channels as freely available as possible, whilst insisting on a high technical standard in equipment as a means of combating congestion.

'In regard to the weight to be given to the relative claims on the spectrum by different potential users, the Institution is aware of the inevitably difficult decisions which may have to be made, but feels that certain principles should guide our thinking in this area, notably:

(a) Attention must be given to the cost of providing the required service in some other way than by radio transmission, and priority must be given to those cases where this cost would be particularly high.

(b) Duplication of services at a number of different frequencies deserves particularly close attention.

(c) Frequency bands should be used only for those services for which they are most suitable technically.

(d) In general, satellite systems achieve better spectrum economy than terrestrial systems, and the development of new satellite services should be safeguarded by adequate frequency allocations.

(e) Finally, it should not be forgotten that there are some uses of radio which make an important contribution even though their economic impact is small, for example in distress and emergency situations, and the needs of the services ought not to be underestimated.

'To summarize, the Institution believes that the public interest will be best served if future use of the radio spectrum is planned on expansive, rather than constrictive, assumptions. The goal should be to make the advantages of radio as freely available as possible to all who can benefit from it. Problems of spectrum congestion are best dealt with by technical innovation, which, in the opinion of the Institution, will prove well able to meet the challenge, provided that it goes hand in hand with a rational approach to allocation to particular users, along the lines discussed above.'

During the coming year it is hoped to publish papers in the Journal on the issues raised in the Institution's submission to the Home Office. Letters from members commenting on these and associated topics for consideration for publication, or for discussion by interested Standing and Group Committees will be welcomed.

Members' Appointments

SILVER JUBILEE AND BIRTHDAY HONOURS

The following members' names appear in Her Majesty's Silver Jubilee and Birthday Honours List.

MOST EXCELLENT ORDER OF THE BRITISH EMPIRE

To be an Additional Commander of the Civil Division (C.B.E.)

Michael William Clark (Companion 1965) Deputy Chairman and Deputy Chief Executive, The Plessey Company Limited.

To be an Additional Officer of the Military Division (O.B.E.)

Commander William Cliffe Hodgson, RN (Ret.) (Member 1954, Graduate 1948) Latterly Assistant Director, Surface Weapons Projects (In-Service Equipments) at the Admiralty Surface Weapons Establishment.

IMPERIAL SERVICE ORDER

To be an Additional Companion of the Order (I.S.O.)

Cyril Arthur Teer, B.Sc. (Member 1947) Senior Principal Scientific Officer, Admiralty Underwater Weapons Establishment.

JUBILEE MEDAL

The following members of the Institution have been awarded the Jubilee Medal:

Frank William Sharp (Fellow 1969, Member 1959). Editor, The Institution of Electronic and Radio Engineers.

Percy Edwin Albert Brightmore (Associate Member 1952). Manufacturing Assurance Manager, Avionics and Communications Division, The Plessey Company Ltd.

CORPORATE MEMBERS

Dr. J. D. E. Beynon (Fellow 1977) has been appointed to the Chair of Electronics at the University of Wales Institute of Science and Technology, Cardiff. Professor Beynon has been on the staff of Department of Electronics, University of Southampton since 1964 and was elected to a Readership in 1974. From 1972 to 1975 he was Assistant Dean of the Faculty of Engineering and Applied Science. His main specialization has been in solid-state devices and in 1975 a paper on charge-coupled devices was published by the Journal.

Dr. P. K. Patwardhan (Fellow 1969, Member 1959, Graduate 1962) has received a National Award from the Fuel Instrument Engineers Foundation Ichalkarangi (Maharashtra State), 'for outstanding contributions to Nuclear Electronics, Data Handling Systems and Instrumentation', according to the citation on the presentation plaque. Dr. Patwardhan who is Chairman of the Institution's Indian Divisional Council, is with the Bhabha Atomic Research Centre, near Bombay. He has contributed several papers to the Institution's Journal as well as to the Indian Proceedings on subjects associated with those for which he receives this notable Indian prize. The value of the award is Rs25 000 and it was presented at a ceremony in Bombay on May 18th on behalf of the Trust by Mr. M. C. Chagla—a former Minister of Education and of External Affairs in the Government of India and High Commissioner in London in 1962–63.

Mr. E. G. Avery (Member 1968, Graduate 1963) is shortly taking up an appointment in Jeddah, where he will manage a Training Centre for the Civil Aviation Directorate of Saudi Arabia. Mr. Avery, who has been on the staff of International Aeradio Ltd. since 1961, has held a number of similar appointments in this country and overseas.

Major F. B. Barnett, REME (Member 1976, Graduate 1973) has recently taken up an appointment as Officer Commanding 12 Light Air Defence (Rapier) Regiment REME Workshop. For the past year he has been on the staff of the REME Wing at the Royal School of Artillery, Larkhill.

Mr. A. J. Chrystal (Member 1973, Graduate 1969) who has been a Senior Air Traffic Engineer with the Civil Aviation Authority for the past 2 years, has been appointed Managing Director of Rickard Miller Ltd., Bognor Regis.

Commander M. G. M. W. Ellis, RN (Member 1971) has taken over as Officer in Charge, User Requirements and Trials Section, HMS *Mercury*. He has recently completed two years' exchange service in the faculty of the U.S. Naval War College, Newport, R.I., where he held the Moorer Chair of Electronic Warfare.

Mr. B. Foster (Member 1973, Graduate 1963) has been appointed Telephone Engineer—Software at the GTE Automatic Electric Laboratories in Melrose Park, Illinois. Following appointments with the British Post Office and in industry, he joined the GTE subsidiary company in Italy in 1968.

Mr. W. Gay (Member 1973) is now tutor in the Electrical Engineering Department of the New Zealand Technical Correspondence Institute Wellington. Following training and service with the RAF and the RNZAF he was with the New Zealand Post Office from 1962 to 1976.

Lt. Col. N. R. F. Mackinnon, R. Sigs (Ret) (Member 1970, Associate 1964) has been appointed a Consultant to Racal Datacom Ltd. He joined the Company in 1974 as Executive Manager for EW Systems Division of the company, following Service Staff appointments and a year as Commander Force Communications in the Qatar Security Force.

Mr. J. R. Ransley (Member 1965, Graduate 1962) who joined the Signals Research and Development Establishment, Christchurch, in 1961 as an Experimental Officer, has been transferred to the Royal Signals and Radar Establishment, Malvern, to take up an appointment as a Communications Engineer.

Mr. H. J. Rippiner (Member 1972, Graduate 1967) has been appointed Sales Manager of the Information Display Division of Tektronix UK Ltd., whom he joined in 1969 as a Field Engineer.

Major N. Rome (Ret.) (Member 1970) who joined Marconi Radar Systems Ltd., as a Senior Sales Engineer in 1973, has been appointed Senior Projects Manager, 800 series Radar Systems.

Mr. P. Rosen (Member 1971, Graduate 1964) has been appointed Chief Engineer HV Fuses with Brush Power Equipment Ltd. He was previously with English Electric Fusegear Ltd., latterly as Fuse Design Manager.

Mr. G. Salter (Member 1964) has been awarded an Imperial Relations Trust Bursary to visit Canada for some 4 months, for the purpose of studying Radio and Television Development in that country. Mr. Salter who joined the BBC in 1943, is now Head of Programme Services and Engineering, Wales.

Mr. L. A. Shillong (Member 1966, Graduate 1962) has recently taken up the appointment of Assistant Engineering Manager in the Eimac Division of Varian at Salt Lake City, Utah. He was previously with Hughes Research Laboratories, Malibu, California.

Mr. A. M. D. Smith, B.Sc. (Member 1976) has been appointed Training Officer (Engineering) with the Sierra Leone Broadcasting Service. For the past 8 years he was with the Inner London Education Authority's Television Service.

Mr. T. C. Smith (Member 1973, Graduate 1969) who was with Texas Instruments Ltd., has been appointed Group Leader, Active Components with the Plessey Company, Titchfield, Fareham, Hants.

Mr. J. A. Surtees (Member 1973, Graduate 1969) is now with HQ, Directorate General of Electrical and Mechanical Engineers, Logistics Executive (Army). He was previously Officer in Charge, Common Purpose Test Equipment, REME Christchurch.

Major J. M. Sweetman, B.Sc., R. Sigs (Member 1973, Graduate 1966) has taken up an appointment as a Squadron Commander in 22 Signals Regiment BAOR. He previously held a Technical Staff appointment in the Signals Branch at HQ BAOR.

NON-CORPORATE MEMBERS

Lt. Cdr. R. Stewart, RN (Graduate 1974) has completed a 2 years' appointment as Assistant Manager, Weapons and Radio, HM Dockyard Gibraltar, and he has been posted to HMS *Ark Royal* as Deputy Weapons Electrical Officer.

Colonel R. A. Stopford, M.B.E. (Graduate 1970) formerly Commanding Officer, Royal Scots Dragoon Guards, has been appointed Project Manager, Main Battle Tank '80, at the Procurement Executive, Ministry of Defence.

Applicants for Election and Transfer

THE MEMBERSHIP COMMITTEE at its meeting on 13th June 1977 recommended to the Council the election and transfer of the following candidates. In accordance with Bye-law 23, the Council has directed that the names of the following candidates shall be published under the grade of membership to which election or transfer is proposed by the Council. Any communication from Corporate Members concerning the proposed elections must be addressed by letter to the Secretary within twenty-eight days after publication of these details.

Meeting: 13th June 1977 (Membership Approval List No. 235)

GREAT BRITAIN AND IRELAND

CORPORATE MEMBERS

Direct Election to Fellow

WISE, Frederick Henry. *Middle Wallop, Hampshire.*

Transfer from Graduate to Member

BERRY, Alan James. *Hawarden, Deeside, Clwyd.*
KELLY, Stephen William. *Rainham, Kent.*

Transfer from Associate Member to Member

MACEY, Ian David. *Reading, Berkshire.*

Direct Election to Member

REED, William Vaughan. *Cherry Hinton, Cambridge.*

NON-CORPORATE MEMBERS

Transfer from Student to Graduate

WATSON, Robert Victor. *Cardiff.*
WYNNE, John Matthew. *Dublin.*

Direct Election to Graduate

YOUNGER, Barrie. *Stockton-on-Tees, Cleveland.*

Direct Election to Associate Member

IKE, Emezie Thaddeus. *London.*
OJUTIKU, Bandele. *London.*
SIDDIQUI, Mohammad Muneer. *London.*

STUDENTS REGISTERED

SMITH, Anthony Kim. *Castleford, West Yorkshire.*
WINSTANLEY, Graham. *Congleton, Cheshire*

OVERSEAS

CORPORATE MEMBERS

Direct Election to Fellow

LLOYD, Douglas D. *Warren, New Jersey, USA.*

Direct Election to Member

BIN DAUD, Abdul Rahim. *Kuala Lumpur, Malaysia.*
CHAN, Kwok Fai. *Hong Kong.*
NG, Chi-ho. *Hong Kong.*
YAM, Peter K. H. *Hong Kong.*

Transfer from Graduate to Member

MASHMOOR, Ishack. *Tel Aviv, Israel.*

NON-CORPORATE MEMBERS

Direct Election to Graduate

HO, Tat Seng. *Singapore.*

Transfer from Student to Associate Member

AKPAN, Nnamso Udo. *Calabar, Nigeria.*

Direct Election to Associate Member

AGALA, Melford. *Port Harcourt, Nigeria.*
LEE, Soh Mooi. *Penang, West Malaysia.*
OFONG-EKPE, Emmanuel U. *Calabar, Nigeria.*
SCHIFFER, Heinz-Egon. *Dusseldorf, West Germany.*
TAN, Chin Peng. *Singapore.*

STUDENTS REGISTERED

AU-YONG, Lin Song. *Singapore.*
CHONG, Teck Ming. *Singapore.*
LEE, Boon Hoo. *Malacca, Malaysia.*
PNG, Siak Meng. *Singapore.*
THAM, Wai Tuck. *Petaling Jaya, Malaysia.*

Report of the IERE Benevolent Fund Trustees for 1975-1976

The Benevolent Fund of the Institution exists to provide help to members, their widows and dependents in time of need. It has been built up over the past 36 years by the voluntary contributions of members and such has been their generosity that no deserving call for assistance has ever had to be denied.

The help that the Trustees may offer is not restricted to financial assistance. Bursaries which have been purchased over the years at well-known schools are available to the children of deceased members who could not otherwise have the benefit of the education they need and deserve. During the year a further bursary for this purpose has been established, this time at King Edward's School, Witley, Surrey.

No new major demands have been made on the Fund during the year but disbursements have included regular grants in association with other funds to a member incapacitated and unable to follow his profession and to a widow whose husband died suddenly and tragically, leaving her with an inadequate income with which to provide for two young children.

The Reserve Account remains healthy despite the fact that the number of regular subscribers to the Fund has declined recently. But in the present economic climate there is no room for complacency. Members who feel able to help are therefore invited to contribute, however modestly, in the knowledge that by so doing they are reinforcing the Institution's power to safeguard the well-being of their professional colleagues and their dependents in times of need and distress. Contributions can be made more beneficial by the execution of a simple deed of covenant undertaking to give a fixed sum each year for a period of seven years. This enables the Fund, being a charity, to recover income tax at the standard rate from the Inland Revenue on the sum contributed. A deed of covenant form for this purpose can be obtained from the Honorary Secretary to the Trustees at 9 Bedford Square, London WC1B 3RG.

INSTITUTION OF ELECTRONIC AND RADIO ENGINEERS BENEVOLENT FUND

INCOME AND EXPENDITURE ACCOUNT FOR THE YEAR ENDED 31st MARCH, 1976

	1976		1975	
	£	£	£	£
COME				
ubscriptions and Donations		480		777
Dividends and Interest on Investments		3,528		3,175
egacy		1,465		—
al Income		5,473		3,952
duct:				
PENDITURE				
Grants and Donations ..	366		543	
Purchase of Bursaries ..	600		100	
Postage, Telephone and Stationery	115		88	
		1,081		731
urplus for the year carried to Reserve Account ..		£4,392		£3,221

BALANCE SHEET AS AT 31st MARCH 1976

	1976		1975	
	£	£	£	£
SETS				
stments at Cost .. .. (Market Value as at 31st March 1976 £51,340 (1975 £39,700))		51,412		48,933
rent Assets				
ank Balances on Current and Deposit Account ..	3,285		2,945	
ncome Tax repayment claim	1,167		310	
undry Debtors	746		79	
		5,198		3,334
		56,610		52,267
s:				
rent Liabilities				
undry Creditors		34		83
		£56,576		£52,184
resented by:				
eserve Account—Balance 1st April 1975	52,184		48,960	
dd: Surplus for the year ..	4,392		3,224	
nce as at 31st March 1976 ..		£56,576		£52,184

Trustees Signed: IEUAN MADDOCK (*Chairman*)
G. D. CLIFFORD (*Honorary Secretary*)
S. R. WILKINS (*Honorary Treasurer*)

SCHEDULE OF INVESTMENTS AS AT 31st MARCH 1976

Nominal		*Cost* £
£100	Associated Electrical Industries Ltd. 6% Debenture Stock 1978/83	99
£1,000	Barnet Corporation 7¾% Loan 1982/84	982
112	Bowater Paper Corporation Ltd. Ordinary Stock ..	343
£2,000	British Transport 4% Gtd. Stock 1972/77	1,864
170	Burmah Oil Co. Ltd. £1 Ordinary Stock	702
£800	Commonwealth of Australia 5½% Loan 1977/80 ..	788
1,200	Henderson Industrial Trust	150
£4,000	4% Consolidated Stock	3,527
340	Courtaulds Ltd. 25p Ordinary Shares	500
£500	Courtaulds Ltd. 7% Debenture Stock 1982/87 ..	467
750	Currys Ltd. 25p Ordinary Shares	1,580
400	De La Rue Co. Ltd. 5p Ordinary Shares	764
1,600	E.M.I. Ltd. 50p Ordinary Shares	2,003
£210	E.M.I. Ltd. 8½% Convertible Unsecured Loan Stock 1981	210
320	English China Clays Ltd. 25p Ordinary Shares ..	501
£2,375	5¼% Funding Stock 1978/80..	2,000
£2,225	5½% Funding Stock 1982/84..	1,994
£2,250	6½% Funding Stock 1985/87..	2,007
£1,830	6% Funding Loan 1992	1,001
2,249	G.E.C. Ltd. 25p Ordinary Shares	885
332	Grattan Warehouses Ltd. 25p Ordinary Shares ..	622
200	Great Universal Stores Ltd. 5⅜% Redeemable Unsecured Loan Stock	106
£300	Great Universal Stores Ltd. 8½% Unsecured Loan Stock 1993/98	248
£150	I.C.I. Ltd. 7¼% Unsecured Loan Stock 1986/91 ..	148
1,000	I.C.I. Ltd. £1 Ordinary Stock Units	2,925
£1,000	Islington Corporation 10% Redeemable Stock 1982/3	995
£100	London County 6% Loan Stock 1975/78	99
637	Lonrho Ltd. 25p Ordinary Shares	690
2,000	Marks & Spencer Ltd. 25p Ordinary Shares ..	1,772
£4,000	New Zealand 7¼% Stock 1977	3,972
1,000	Plessey Co. Ltd. 50p Ordinary Shares	1,479
156	Reed Group Ltd. £1 Ordinary Shares	392
£35	Reed Group Ltd. 10% Unsecured Loan Stock 2004/09	35
1,000	Shell Transport and Trading Co. Ltd. 25p Ordinary Shares	3,140
£1,000	Slough Corporation 8¾% Redeemable Stock 1979/80	990
200	Tanganyika Concessions Ltd. 50p Ordinary Shares	703
1,330	Transport Developments Group Ltd. 25p Ordinary Shares	743
£1,225	Treasury Stock 7¾% 1985/88	992
£1,320	Treasury Stock 8¼% 1987/90	1,006
£1,991	Treasury Stock 8½% 1980/82	2,000
£1,125	Treasury Stock 9% 1994	999
£1,500	Treasury Stock 12% 1983	1,432
£2,180	Treasury Stock 13% 1990	2,200
796	Unicorn General Trust	125
£1,200	3½% War Loan	498
400	Watts, Blake, Bearne & Co. Ltd. 25p Ordinary Shares	437
500	Whitbread & Co. Ltd. 25p 'A' Ordinary Shares ..	297
		£51,412

AUDITOR'S REPORT TO THE TRUSTEES OF THE INSTITUTION OF ELECTRONIC AND RADIO ENGINEERS BENEVOLENT FUND

n my opinion the annexed accounts show a true and fair view of the Benevolent Fund's affairs at 31st March 1976 and of the surplus for the ended on that date, and comply with the Rules thereof.

Signed: R. O. O. FREEMAN,
Chartered Accountant
Honorary Auditor

Bloomsbury Street, London WC1B 3QY
March 1977

Forthcoming Institution Meetings

Wednesday, 28th September

EDUCATION AND TRAINING GROUP

Colloquium on TRAINING TECHNICIANS IN ELECTRONICS

No. 3 Radio School, RAF Locking, Weston-Super-Mare, Avon, 10.30 a.m.

Advance registration essential. For further details and registration forms, apply to Project Officer, RAF Locking, Weston-Super-Mare, BS27 7AA.

Thursday, 13th October

ANNUAL GENERAL MEETING OF THE INSTITUTION

London School of Hygiene and Tropical Medicine, 6 p.m. (Tea 5.30 p.m.).

Tuesday, 18th October

JOINT IERE/IEE COMMUNICATIONS AND COMPONENTS AND CIRCUITS GROUPS

Colloquium on A COMPARISON OF SAW, CCD AND DIGITAL TECHNOLOGIES

Royal Institution, Albemarle Street, London W1, 2 p.m.

Advance registration necessary. For further details and registration forms apply to Meetings Officer, IERE.

Tuesday, 1st November

AUTOMATION AND CONTROL SYSTEMS GROUP

Colloquium on LABORATORY AUTOMATION

Royal Institution, Albermarle Street, London W1, 2 p.m.

Advance registration necessary. For further details and registration forms apply to Meetings Officer, IERE.

Thursday, 3rd November

JOINT IERE/IEE MEDICAL AND BIOLOGICAL ELECTRONICS GROUP IN ASSOCIATION WITH SOUTH WALES SECTION

Colloquium on MODERN TRENDS IN THE ASSESSMENT OF CARDIO—PULMONARY FUNCTION

Welsh National Medical School, Cardiff.

Advance registration necessary. For further details and registration forms apply to Meetings Officer, IERE.

Thames Valley Section

Thursday, 20th October

Microprocessor systems—principles and applications

By L. A. Crapnell (*Ferranti*)

Caversham Bridge Hotel, Reading, 7.30 p.m.

Kent Section

Wednesday, 5th October

Microprocessing: Chapter 2

By a speaker from Jermyn Industries

Medway and Maidstone College of Technology, Horstead, Chatham, Kent, 7 p.m. (Tea 6.30 p.m.)

Southern Section

Wednesday, 12th October

JOINT MEETING WITH IEE

Communications—a personal view

By D. L. Cooke

Room AB011, Portsmouth Polytechnic, King Henry I Street, Portsmouth, 6.30 p.m.

Beds and Herts Section

Thursday, 27th October

Automobile electronics—some aspects of research

By Dr. R. C. Codd (*Joseph Lucas*)

Luton College, Luton, Beds., 7.45 p.m. (Tea 7.15 p.m.).

South Western Section

Wednesday, 26th October

CEEFAX—A new form of broadcasting

By J. P. Chambers (*BBC*)

Chemistry Lecture Theatre No. 4, University of Bristol, 7 p.m. (Tea 6.30 p.m.)

South Midlands Section

Thursday, 10th November

The Voltage to Current Transactor (VCT)

By Professor W. Gosling (*University of Bath*)

Majestic Hotel, Cheltenham, 7.30 p.m.

East Midlands Section

Tuesday, 18th October

JOINT MEETING WITH CEI

Advances in railway technology

By R. Kemp (*British Rail*)

Room J001, Edward Herbert Building, Loughborough University of Technology, 7 p.m. (Tea 6.30 p.m.)

West Midlands Section

Tuesday, 18th October

JOINT MEETING WITH RAES

The spirit of nineteen-o-one (1901)

By Dr. D. McLean (*Loughborough University of Technology*)

An account of the successive application of steam, air, oil, amps and bits to solve the last major flying problem.

Astra Cinema, RAF Cosford, 7.15 p.m. (Tea 6.45 p.m.)

Yorkshire Section

Thursday, 29th September

The professional, the amateur and the microprocessor

By P. Jackson (*Music Hire Group*)

Synopsis: This lecture highlights the low cost of microprocessors and looks at systems and applications for both professional and amateur users. Leeds Polytechnic, 6.30 p.m.

Merseyside Section

Wednesday, 12th October

Daresbury nuclear physics facility

By Dr. H. Price (*Daresbury Nuclear Physics Establishment*)

Synopsis: A review of the experimental work being carried out at the Daresbury establishment.

Department of Electrical Engineering and Electronics, University of Liverpool, 7 p.m. (Tea 6.30 p.m.).

North Western Section

Thursday, 20th October

Quadraphonics

By Dr. K. Barker (*Sheffield University*)

Synopsis: The lecture will introduce the subject of quadraphonics through the historical development of sound recording and will illustrate the subject extensively with visual and audio demonstrations. All presently available quadraphonic systems will be covered including some new aspects of multi-channel broadcasting.

Bolton Institute of Technology, Deane Road, Bolton, Lancs, 6.15 p.m. (Tea 5.45 p.m.).

East Anglian Section

Tuesday, 18th October

ANNUAL GENERAL MEETING

followed by

Microprocessors/microcomputers?

By Robert Robinson (*Jermyn Industries*)

Civic Centre, Chelmsford, 6.30 p.m. (Tea 6 p.m.).

South Wales Section

Wednesday, 12th October

Quadraphonics

By K. Oliver (*BBC*)

Synopsis: The intention is to discuss quadraphony mainly from the broadcasting point of view covering the following aspects: mono/stereo/quad compatibility, discrete versus matrix quadraphony, and the limitations of matrix quadraphony BBC Matrix H.

Room 112, Department of Physics, Electronics and Electrical Engineering, UWIST, Cardiff, 6.30 p.m. (Tea 5.30 p.m.).

Northern Ireland Section

Tuesday, 4th October

The professional engineer

By a speaker from UKAPE

Cregagh Technical College, 7 p.m.