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The Public Image of the Engineer

SINCE the amenities of civilization have been largely created by engineers it is sad to see a revival of Shakespeare's thought, 'For 'tis the sport to have the engineer hoist with his own petard'. Written over 350 years ago into his most exaggerated tragedy Shakespeare's words still '. . . go hard' with those who have had the patience and diligence to prove their right to be called 'engineers' only to receive little praise and, so often, little reward. Too often criticism of their labours is but a diversion to distract from political, economic and other ills.

Does the engineer therefore stand in need of tutors to inform government and the public on the importance of the engineer in society? Maybe public appreciation of the engineer has been dulled by the munificence of his products: radio and television in all its international communication roles; electronic navigation systems without which air travel could never have reached its present magnificence; the art of recording for entertainment, for teaching and as a scientific tool; and as a final example the electronic processing of food and steel manufacture. These are but a few demonstrations of how the public benefit from the labours of the professional radio and electronic engineers. Are these not as great monuments as the one that over 200 years ago gave Christopher Wren his epitaph 'Si monumentum requiris, Circumspice'—'If you would see his Monument, look around'.

The examples chosen do not deprecate the contributions of members of our sister Institutions to modern living. To the contrary even members of much older branches of the engineering profession are equally concerned with undervaluation of the status of engineers whose services to modern society are taken for granted. Such lack of appreciation acts as a brake on recruitment, especially to the manufacturing industry which creates the main wealth of the country. A Gilbertian situation which might be corrected by using promoters of public relations as recommended by the Council of Engineering Institutions. A far cry from the epitaph of Wren but a consequence uf the soccess of pressure groups which now influence legislation and public opinion.

Before embarking on a public relations exercise it is important to understand both problem and purpose. The problem is to educate all sectors of the public on the fact that the professional engineer provides 'skilled services for which both an academic and a vocational qualification are required. These require previous training and years of delay before earning capacity is achieved. All professional men and women therefore begin their lives with a sacrifice of leisure and income.'

These basic qualifications apply to engineers of varying specializations. Just as the Civil, Municipal, Mining or Marine Engineer would never claim to have engendered the technology of radio and electronics nor does the electronic and radio engineer claim *especial* public recognition of his training and achievements. There is common concern about the evaluation of the engineers rôle in society.

This theme was developed by Lord Hailsham when he gave the 'Rivers Lecture' at The Institute of Chartered Secretaries and Administrators in which he asked, 'If there can be a Confederation of British Industry why can there not be a Confederation of British Professional Associations, however loosely associated, to identify the problems which affect us all?'

It is in identifying '. . . the problems which affect us all' which is the nub of Lord Hailsham's Lecture. He emphasized the growth in the number of professions and that their services more than ever in the past were essential in the common weal. How best can engineers present this case?

G.D.C.

The Rt. Hon. Lord Hailsham of St. Marylebone was Lord President of the Privy Council when in 1961 the Institution received its Royal Charter.

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*See also pages 331 and 336.

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The development of an automatic wiring analyser system for testing telephone switching rack backplanes

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and

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Based on a paper presented at the Conference on Advances in Automatic Testing Technology held in Birmingham from 15th to 17th April 1975.

SUMMARY

This paper describes the various stages in the evolution of a computer controlled automatic test system for checking the validity of the backplane wiring of very large electronic telephone exchange switching racks. Although the basic testing requirements are simply wiring continuity and insulation testing, the large physical size and the diversity of hardware to be tested in an essentially random sequence necessitated a very large and complex test system.

The solutions to the difficult interface problems and those of handling are described, together with the approach taken to solve the complex software and programming problems, including those caused by the large volume of data to be handled.

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1 Introduction

TXE 4 is the name of the new generation of electronic telephone switching systems currently being installed in telephone exchanges by the Post Office. It was a firm requirement that the backplane wiring on the racks must be demonstrated to be better than one wiring error in every five thousand wiring terminations. This was intended to minimize the expensive and time-consuming task of rectifying wiring errors on installation, a situation which is aggravated by the increasing shortage of skilled engineers to do the work.

Until this time production wiring inspection had always been done manually by conventional 'bridge and buzz' methods. Apart from the difficulty of establishing exactly the efficiency of a manual inspector, there is the overriding problem that however good the inspection is, there is no final demonstrable evidence of the quality of the finished wiring, particularly the presence of additional wires.

A design study was therefore started to examine the problems and produce a specification for an automated test system. A system of this type divides into two halves, the first half being the fixturing, which includes product handling, contact accessing and machine interface, and the second half which is the wiring analyser and control system.

Initial consideration was given to manufacturing the whole test system in-house, but neither the time nor the expertise was available to produce the analyser and control half as appeared to be required for such a test system. A number of small test systems are being operated within STC for testing the modules which plug into the TXE 4 racks but experience with these was insufficient to build a rack wiring analyser with confidence. A market survey was therefore conducted to find a suitable supplier for this part of the system, and work continued on the design requirements of the fixturing with a view to producing this ourselves.

2 TXE 4 Racks

A TXE 4 rack is a bulky structure, standing 3·2 m (10 ft 6 in) high by 0·91 m (3 ft) wide by about 0·46 m (18 in) deep, with a framework made from aluminium alloy extrusions. Figure 1 is an outline of the rear view of a typical rack.

The rack is subdivided into a number of sub-racks or shelves with sets of guides for printed circuit cards or card modules, and the main backplane consists largely of rows of edge connectors with wire wrap pins. There are several rectangular 12-pin power connectors in various positions on the backplane for power supply modules, the wiring to these being soldered.

Above the main backplane is a variable-sized terminal field positioned in a different vertical plane, built up from loosely retained 72-pin blocks with wire wrap pins on both sides. This field is used for the inter-rack exchange cabling. The bulk of the rack wiring consists of interconnections between these three types of connector, with a limited number of additional wires to a fuse panel

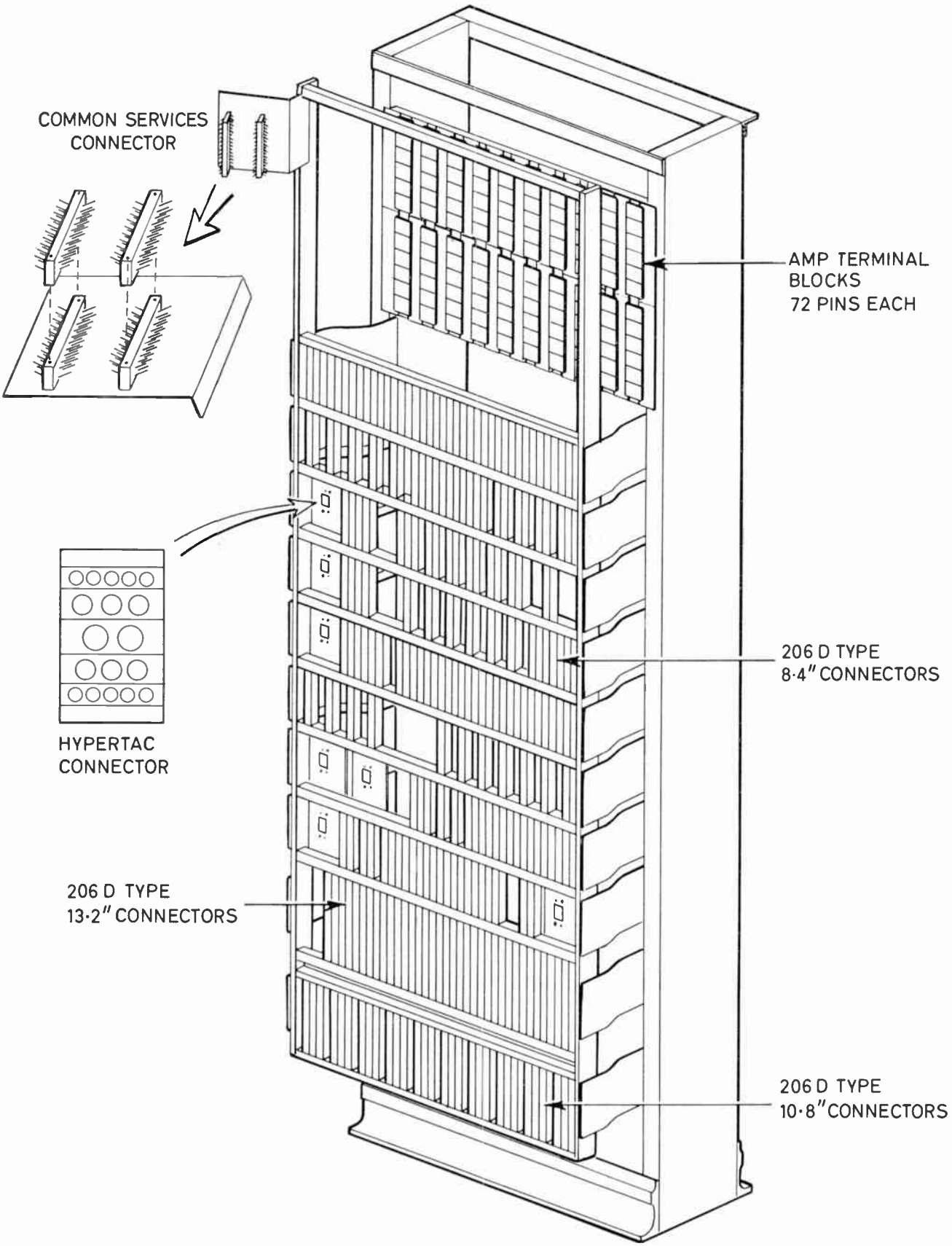

Fig. 1. Rear view of a typical rack.

at the top, and to a small but highly variable number of test sockets and indicator lamps on a lower front panel.

There are about thirty different basic rack types, each of which has a different number or combination of the four basic shelf sizes, to a maximum of ten shelves per rack. The number and position of edge connectors on the shelves is variable up to a maximum of 40 per shelf. The number and position of the power connectors is also variable. On a number of racks there is an additional problem of having from one to four of the 72-way terminal field connectors mounted at the end of certain shelves, but more or less in the same plane as the edge connectors (see Fig. 2). By virtue of this variability, each rack type is physically different, in the way it is equipped, from any other type.

Apart from the physical differences, there are also problems with the wiring. Due to the unique switching requirements of each telephone exchange, a small percentage of the wiring on each rack has to be specific to the exchange where the rack will be installed. The bulk of the wiring on a rack, that which remains the same from one unit to the next on any type, is termed basic wiring, and the additional variable wiring (which in practice may also include some deleted wires) is termed contractual strapping. The overall effect is that each rack manufactured is virtually a one-off model.

Production is organized on a small batch basis, partly due to the exchange by exchange ordering procedure, and partly because any attempt to build longer runs of basic rack types would require excessive storage space and tie up large sums of capital. It is also doubtful if any significant improvement in quality or throughput would be achieved, as most of the wiring is of a random and non-repetitive pattern. One of the basic requirements of a test system was therefore, that it should be able to test racks presented in an essentially random sequence.

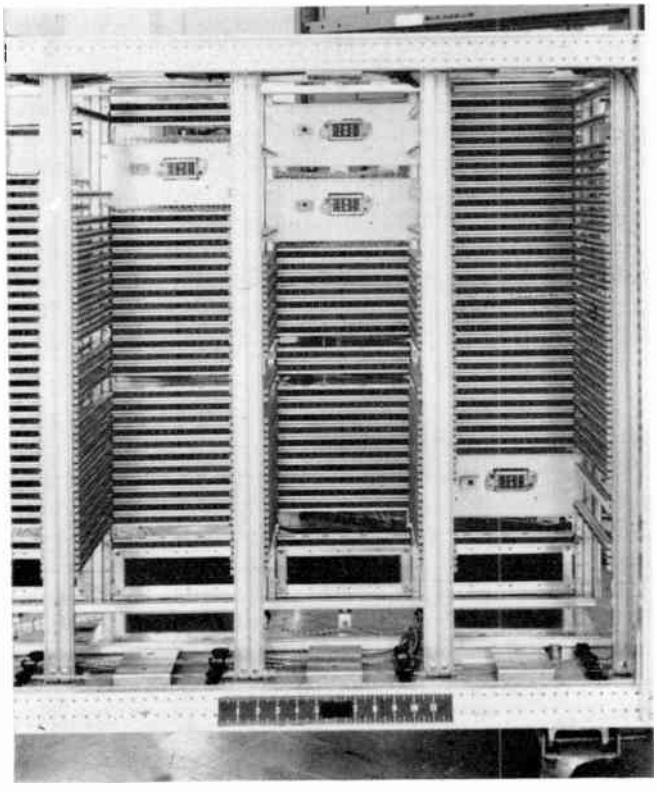

Fig. 2. A view of part of a typical TXE 4 rack showing the variety of connectors to be accessed.

3 Access Problems

One of the basic and most important problems was how to make access to the wiring terminations. There are up to 50 000 termination points on some racks and although not all points are wired, they should be accessed to detect possible wrong terminations and extra wires.

Access to the rear of the backplane was ruled out due to a number of factors such as the possibility that wire wrap pins become bent out of line during manufacture; the mixture of solder tags and wire wrap pins; the float in the connectors; and the thick mat of wiring which would hinder access. Additionally, of the various access techniques available, the only one generally applicable in this case would be spring pin probes, and apart from the lack of adaptibility to cope with the variations of rack configuration, this technique would require an impossibly complex and massive back-up structure to resist the huge total spring loads applied.

Frontal access to the backplane requires entry into the body of the rack, and the question then is, 'Can the backplane be removed and tested independently?' The problems here include the fact that the terminal field is a separate item, but integrally wired to the main backplane, which would present handling problems. Due to noise segregation, some of the wiring runs are away from the backplane, inside the rack structure, which would make removal and replacement hazardous. The backplane is an assembly of separate connector frames built-in as an integral part of the jig assembled main structure thereby making removal impracticable.

In retrospect it is clear that considerable simplification of the whole test system might have been achieved had the automatic test access requirements been a requirement of the initial rack equipment practice design. But the design was now too far along the road to full production to effect more than minor modifications to ease the access problems and so we were faced with an additional problem of devising a mechanical handling system for massive racks weighing up to 320 kg each in the process of testing them.

For the method of accessing the edge connectors, which contain the bulk of the access points, there was really only one technique; to use test cards plugged into the edge connectors and wired via some form of interface to the test system, as yet unknown. In view of the large number of cards involved and their relatively high insertion force, it was decided that the best, the most economic and least time-consuming method would be to devise an adapter unit system, comprising some form of box-like structure containing a shelf load of cards, which would be loaded into a shelf position, and to have a mechanism to push the cards the last half an inch into engagement. The adapter units would be easily re-equipable with new cards, and this would also enable us to provide a special module to mate with the power connectors which could

be quickly inserted in the appropriate position just prior to loading the adapter units. This general approach was made easier by virtue of the fact that the racks are designed using a modular dimensioning system. The connectors are mounted on insert strips with holes at a precise 0·8 in (20·32 mm) pitch, and in the rack vertical axis, all equipment sizes and spacing is based on an exact 0·6 in (15·24 mm) pitch. Also, there are basically only two shelf aperture sizes although, as previously mentioned, these can have connector arrays of four different heights fitted to them on the backplane. Fortunately any one connector frame will only have one size of connector fitted to it. This meant that the adapter system could be limited to two basic sizes of adapter units and cards with only the mating ends of the cards in different sizes.

The most difficult access problem remained to be solved, how to access the terminal field connectors. These are a specially developed design with 72 through pins of rectangular cross-section in an 8×9 layout on 0·2 in (5·08 mm) pitch in both axes. On each side of the connector there is room for one wire wrap, then the ends of the pins are reduced in cross-section to receive special 18-way sockets on the exchange cabling. This plug and socket arrangement is a deliberately high insertion force design (approximately 4·5 kg per 18 ways) with very sharp-edged tin plated pins. This provides reliable connections for a few insertions in normal use but is a highly destructive combination for any socket used on test equipment which must withstand many hundreds of insertions. Additionally the high insertion force prohibited the ganging of sockets for manual insertion, and the limited strength of the backplane eliminated ganged mechanized insertion. It was clear that a specially designed zero or low insertion force connector would have to be used which, to minimize plug-up time, would have to access large groups of pins at one time.

There remained a number of terminations not so far considered, such as the fuses and lower front panel. With one exception, however, these had such highly variable configurations that in view of the small number of wires involved, the complexity and cost of making access would be prohibitive. The rationale was therefore applied, that providing that the machine accessed terminations could be verified to a very high accuracy, say 1 error in 20 000, then the anticipated error rate from manually inspecting these few remaining wires would not derate the error level for the whole rack to worse than 1 error in 5000 as required. This residual wiring was also of a nature which was inherently much more easily inspected.

The one exception to this philosophy was for a group of rack common services connectors which were of a consistent configuration, and although they were difficult to access, it was felt that a connector could be devised, and would probably be used on a flying cable.

4 Test System/Adapter Unit Interface

In order to be able to connect to the test system the various combinations of adapter unit with which a rack might be equipped, it would be necessary for every adapter unit to be fitted with some form of common interface connector or connectors.

The initial schemes for the system envisaged some form of fixture to hold and support the rack, the latter being loaded with appropriate adapter units, and then, with some form of structure supporting the cabling, the interface connectors would be manually positioned and attached to the adapter units. This simple-sounding plan had a multitude of pitfalls.

Firstly, for example, the majority of shelves have a total of either 3120 or 5040 possible terminations. Therefore, for a common interface, this requires connectors with at least 5040 pins. The largest connectors commercially available have only about 100 or so pins, which would require at least 50 connectors for each adaptor. This was obviously not practicable. A prototype low insertion force connector was produced by Smiths Hypertac which was a compact 1276-pin connector with a single jacking screw. The prototype was surprisingly easy to operate and if used would have only required four connectors for each adapter unit; but it would still have needed a considerable amount of effort to use and, more important still, a long time to interface the rack on line with the tester, thereby wasting valuable testing time.

The second problem was the bulk of cabling to the interface connectors. Whatever testing attitude was adopted for a rack, only a proportion of the weight of cabling and connectors could be supported mechanically, leaving probably between 4·5 and 6·4 kg per connector to be handled by the operator, and in addition, with the large numbers of wires involved, each cable would be very stiff and difficult to handle.

Partly in response to these cabling problems, a parallel study was carried out, to investigate the approach of mounting semiconductor switching logic directly on to the access cards in the adapter units. This would have the advantage of drastically reducing the number of wires to the access array. The major disadvantage of semiconductor logic is the low operating voltage, typically 5 volts, which precludes high voltage insulation testing. It was decided that, as commercially available test systems using this technique, at that time, were insufficiently well proven to our satisfaction, and to embark on an in-house development programme was not desirable, we would have to reject this approach.

5 Choice of Supplier

It was becoming evident that the extent of the unsolved fixturing problems, of which only a few have been enumerated, was too great to allow us to develop an optimum solution in a reasonable timescale with our available manpower and resources. With a requirement for progressively more of the fixturing to be machine-controlled it also seemed desirable to have the fixturing manufactured by the supplier of the analyser and control system, to ensure the maximum degree of compatibility between the various parts.

Our market survey had found very few potential suppliers of large wiring analysers with adequate complex fixturing experience, who did not also appear to

consider fixture designing as some form of engineering loss leader to encourage analyser sales.

After very careful assessment of overall capability, we chose Hughes Aircraft Company of Los Angeles to design and build the test system to a very comprehensive specification produced by STC.

6 Basic Test System

The heart of the Hughes test system is the FACT II (Flexible Automatic Circuit Tester) wiring analyser. This is a high-speed reed-relay based continuity and insulation leakage tester. With its built-in control, which is in effect a dedicated mini-computer, it is able to receive a prepared test program from any one of a variety of peripheral devices, execute the circuit testing of the unit under test (u.u.t.), including the issuing of command instructions to any automated fixturing, and will then output the test results to the chosen peripheral device. A comprehensive range of features and facilities are available on this reliable machine, which is extensively used in the aerospace and telecommunications industries in particular. The test rate for this machine is 4000 continuity tests per minute and 2000 leakage tests per minute.

This company has also developed a number of specialized techniques to assist in the rapid adaptation of a u.u.t. In our case, in particular, they were the only supplier capable of demonstrating a proven method of zero insertion force adaptation to our terminal field connector. This particular adaptation method is called LIFT (low insertion force technique, see Fig. 3) and consists of rows of terminal pins set in a non-conductive base material, at a spacing adequate to allow the friction-free insertion of the contacts to be mated. Inflation of a thin pneumatic bladder threaded between the LIFT pins causes them to engage and hold the test contacts. Operation is at about 240 kN/m^2 (35 lbf/in^2) and is positive and rapid.

With the use of this technique it was possible to design drop-in adapter units for the terminal field on the racks, to access blocks of 2880 pins at once with the only effort being to support the weight of the unit whilst locating it in position. This size of adapter was chosen as a convenient part of the terminal field nearest in pin total and physical size to a small shelf adapter. A number of this size of terminal field adapter and some smaller sizes, a total of six units, can be used in various combinations to access any size of terminal field on a rack, using no more than three units at any one time. Hughes have also had considerable experience in designing adapter units similar to those required for our shelves of edge connectors. In this application the adapter units were designed to contain a full complement of 40 extender cards. Each card has a set of contact pads to mate with an edge connector in the rack, and at the opposite end another set of smaller contact pads, both sets of pads linked by copper strips. The shape of the extender cards is tailored to match the various sizes of edge connectors used on the rack, but in every case the opposite end of the card has a common pattern of contact pads. The end result is that when a rack is loaded with adapter units, all adapter units irrespective of size, present a uniform array of rows of 40 identical printed card edges. This corresponds to the adapter unit common interface described earlier. Using another application of the LIFT technique, the test access heads of the analyser contain rows of bladder-actuated pins, behind a slotted check plate guide, matched to the extender cards in the adapter units. In order to reduce the number of redundant contacts and due to a number of other constraints, the larger sizes of shelf extender cards have the interface contact pads divided into two groups, both equal in size to those on a small adapter unit, and therefore large adapter units are mated with two test access heads at once. The six terminal field adapter units are internally hard wired from their LIFT contacts to a set of printed card edges so that they also present a common interface when loaded into a rack (see Figs. 4 and 5).

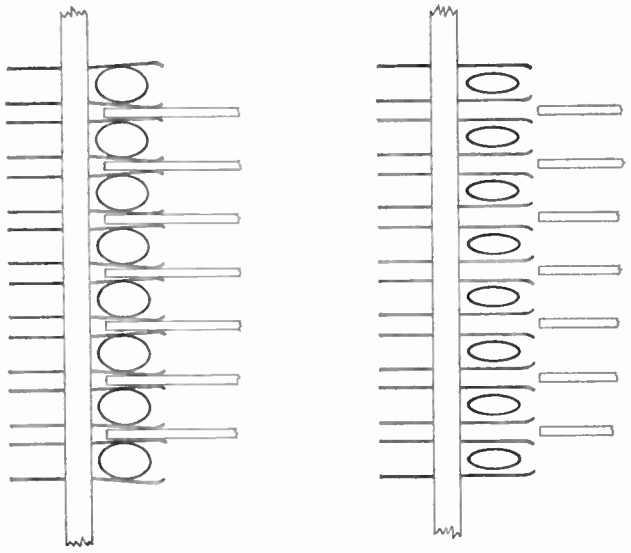

Fig. 3. Schematic representation of LIFT connector shown in pressurized and depressurized states.

The use of this combination of techniques results in the time taken to connect the test access heads of the analyser being reduced to a few seconds, minimizing wasted testing time, with the job of loading adapter units, which takes about 30 minutes, carried out as an off-line operation. The basic method of operation is to leave the adapter units in the racks until all test, rework and retest cycles have been completed, but they may be off-loaded if, for instance, the first rework is likely to take a long time, or there is a temporary shortage of a particular type of adapter unit.

7 Test System Mechanical Operation

A TXE 4 rack is normally moved between work stations lying on its side on a set of castors bolted to it. When ready for testing, it is rolled into one of a number of large mobile holding jigs, known as rack transporters, where it is manually clamped in position. The transporters are equipped with electrically-powered lifting and rotation facilities. The rack is raised from the floor and turned on to its back, that is, with the wiring plane on the underside. Adapter units are now loaded, with the assistance of overhead hoists, and the extender cards are pushed into the edge connectors with a portable automatic card inserter. The transporter is docked against

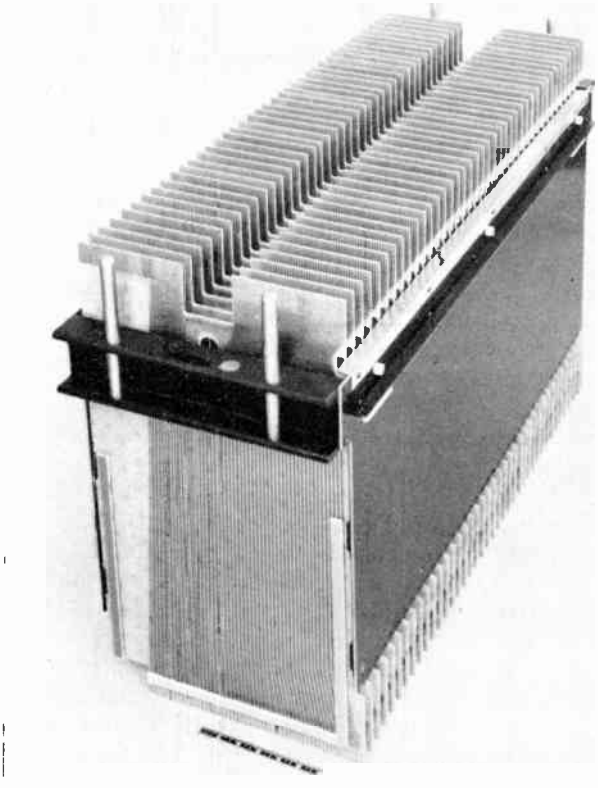

Fig. 4. Rack adapter unit to access one large shelf in a rack.

the front of the access fixture and automatically clamped in position beneath eight test access heads. The test is initiated and the rest of the test cycle is carried out automatically. The eight heads are lowered together sufficiently to be able to engage pairs of index pins on the adapter units. The heads are then traversed along the rack until they are correctly registered over an adapter unit, using the index pins as a reference, and are then lowered to engage the extender cards with the LIFT connectors in the heads. The LIFT bladders are inflated

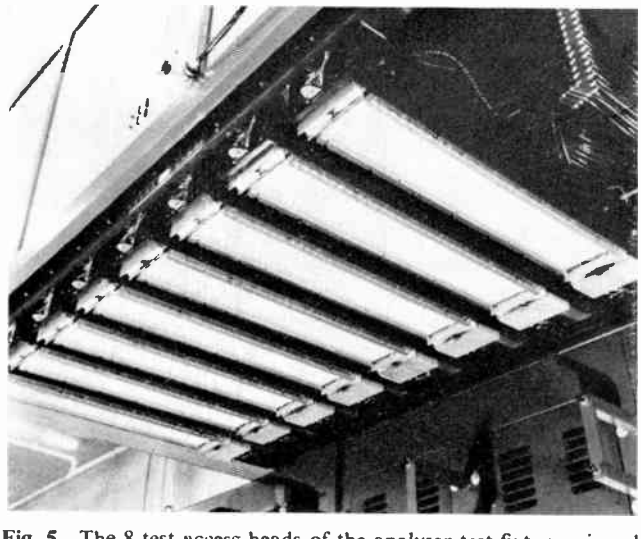

Fig. 5. The 8 test access heads of the analyser test fixture, viewed from below. These accept the plug blades at the top of the boards in Fig. 4.

to make contact and testing is carried out. When testing is completed, the bladders are deflated, the heads are raised fully up and traverse back to their starting point. After disengaging the transporter and collecting the wiring error print-out, the rack is wheeled away for rework. The rack can be rotated in the transport to a suitable attitude for rework and is also adjustable for height.

Although TXE 4 racks contain up to possibly 50 000 termination points, of which the vast majority must be tested by the machine, in fact only 26 400 test points were specified for the analyser. Of these, only 25 920 are allocated to the test access heads, and 80 are used on two small hand-attached LIFT adapters for the common services connectors on the rack, which are on flying leads from the fixture. The remaining terminations are used for calibration or spare.

This economy of test points is effected by the adoption of a multi-pass mode of operation, described in Section 9.

8 Size of Machine and Test Philosophy

The choice of what size of analyser to have, in terms of the number of points accessed at one time, is more difficult than it might appear at first sight. There are two basic options, firstly to choose a machine with sufficient test access points to test the largest foreseeable product in one accessing operation, or secondly to have a smaller analyser, only partially accessing the product in one step, and to use a multi-pass mode of operation, where the test access points are moved along the product in discrete steps, performing testing, in effect, as a permutation of any X from Y number of stages.

The choice is primarily an economic one, with the cost of any analyser being almost directly proportional to the number of test points after an initial basic price, not forgetting that for every analyser test point there must be an additional adapter access point in the fixture, the relative cost of both being very high.

Some secondary considerations affecting the choice are, for a single-pass mode, the advantage of only performing the minimum number of tests without duplication, and the minimum on-line accessing time which is important with high production throughput, with a fairly simple fixture control system, set against the drawbacks of the fact that for a large part of the time some test points may remain unused if the product is of variable size as in our case, and also the need for a more massive fixture. The pros and cons of a multi-pass mode, apart from cost, are, as generalizations, not impressive. The system is fully utilized, the hardware is less bulky and is easier to repair and maintain, but it will take longer to perform a whole test, due to the extra time taken to reposition the test access heads and the large potential number of redundant tests that would be carried out. This last factor can be significantly improved by a carefully planned test routine which suppresses a proportion of these extra tests.

The control of the fixture is, of course, more complex in a multi-pass mode and if, as in our case, the pattern of passes is different from one product to another, the programming is more complicated. Despite this lack of

positive advantages, in some circumstances multi-pass can be a quite satisfactory method. Consideration of the parameters of the STC system may bring this out better.

9 Multi-pass Operation

When a rack is loaded with adapter units, there are normally between 8 and 13 rows of card edges presented to the 8 test access heads. Their pattern of movements is in fact more complicated than the simplified sequence quoted in Section 7. Let us assume our u.u.t. has 12 access positions. The cycle will start as indicated earlier by the heads being partially lowered, followed by traverse to the first 8 access positions. The heads are lowered, testing carried out, and heads raised, but now heads 5 to 8 move to access positions 9 to 12 and all heads are lowered and a second test pass is carried out. The 8 heads are raised again, and this time heads 1 to 4 move to positions 5 to 8 and a third test pass is made. Finally all heads are raised and return home. For racks with only 8 positions, of course, only one test pass is needed; for racks with up to 11 or 12 positions, which are the majority, some variation on the 3 test pass sequence above is used; and for racks with 13 positions 4 test passes are required.

However, the total time for all head movements in any test cycle does not exceed 2½ minutes in a total test cycle time of between 12 and 20 minutes per rack. This rate is fast enough to deal with the anticipated rack throughput.

10 Control System

At some stage in the evolution of the specification it became obvious that we needed a computer to control the system. One very strong reason was that the solution to the contractual strapping wiring problem referred to in Section 2 required the use of a computer. Rather than generating a completely different test program for every rack that is to be tested, which would be very costly and cumbersome, an alternative method was sought. Examination of the wiring data for the racks revealed the fact that the contractual strapping was generally of a fairly stereotyped pattern even though the pattern changed from rack to rack, with recognizable single or groups of wires to be added or deleted. A table of these strapping elements was produced so that any set of strapping could be defined as a series of these elements or options. Therefore a test program would consist of the basic wiring plus the contractual strapping options. Some constraints had to be imposed on our engineering departments to adhere to this format when generating the rack wiring data. The test system mini-computer works in conjunction with a dual disk storage unit. A number of basic wiring test programs are stored on disk together with the library of strapping options. Only a short call-up tape needs to be generated for each rack giving its code, the appropriate reference for its basic test program and list of contractual strapping option references. When these data are received by the computer, it extracts the information from the disk and amalgamates this to produce the rack test program. The operation takes from a few seconds to a few minutes, but will not normally constitute a delay as the processing is carried out whilst the rack is being set up for testing.

This arrangement has another important advantage in that because each rack is virtually unique, its test program is of value only whilst that rack is in the test area, hence the short call-up tape, which need only be punched just before the rack is ready for test, can be easily disposed of afterwards and is much more suitable for keeping with the manufacturing paperwork accompanying the rack than would the half dozen or more reels of paper tape of a discrete test program.

With a computer we were now able to operate a more efficient multi-pass mode of operation, and use it to perform translations between analyser pin notation and rack pin notation.

The system was also specified to be able to operate a second analyser with the same computer, on a time-sharing basis, to enable the system to be expanded at a later date.

The computer is used to derive data from the test results for a management information system (m.i.s.). Various statistics are compiled whilst the system is in operation, such as the number of racks of various types processed, the number of faults per rack, the accumulative totals of faults, system faults failures and input messages, all referenced to a time of day clock built into the system. These statistics are stored and transferred periodically to magnetic tape for off-line analysis, in order to provide a management tool for production monitoring.

The test system is furnished with a comprehensive collection of fault monitors and error detection devices. These range from internal electronic test circuits, to air and power supply monitors and to physical fault detectors such as access head position and misalignment, u.u.t. and adapter unit alignment, and various other fixture parameter checks.

Faults which arise during operations, either shut down or stop the operations if sufficiently important, or else produce an error information printout on a teletype. There is also a comprehensive array of monitor displays to assist in rapid fault isolation and repair.

The test system is programmed to perform automatically a full self-test routine once every day, which exercises the system down to the contacts in the LIFT heads, beginning at start-up in the morning and continuing between periods of product testing until a complete self-test cycle has been made.

11 Software Philosophy

Although the provision of suitable data for the test system is an obvious necessity, it perhaps is less apparent that it must be made an integral part of the system design and will even affect the choice and design of the hardware. For TXE 4 the manufacturing information for backplane wiring was already computer-produced from engineering data input. It was found possible to use the same engineering data input also to generate the test data, thereby guaranteeing the validity of the tests, i.e. manufacturing has been correctly carried out to the wiring information. If the test data had been manually prepared, the cost would have been prohibitive and the accuracy would have been poor.

Having opted for a computer-controlled test system, careful decisions were made on how much processing could reasonably be expected from the SPC16 mini-computer controlling the analyser. The manufacturing information is produced in a batched processing mode on an IBM 370/135 and it was decided to split the new software required between the IBM main processor and the mini-computer. The data processing involving large table look-ups with massive rearrangement of data was put on the main processor. The mini-computer was used for the analyser control, the storage and retrieval of test programs and control of the contractual strapping options, and generation of the m.i.s. statistics.

This division enables full use of a large computer with batched processing and on-line facilities without overload on the analyser system. The format of the engineering data input had been dictated by manufacturing requirements and certain incompatibilities were found when considering the new interface for the analyser. These were resolved with either extra constraints on the input data or extra software. An example of this difficulty was a first assumption that pins of the same signal name represent a wired net. In practice this was not the case as sometimes the net is not completed until the units are plugged into the rack. In order to satisfy the need that only complete nets are presented to the analyser, all pins associated with a signal name were checked for continuity by the software and split into one or more nets.

A further complication was introduced as some wiring does not appear on the original engineering rack wiring data input. This is sub-assembly pre-wiring of the TXE 4 connectors and was required to be tested. As the analyser system does not fully access all rack terminations simultaneously, the software had to divide the test data into separate analyser cycles. The large number of rack types and the variable nature of the shelves means that the cycle division is complex. Permanent system files containing physical information for each rack type, details for each shelf type and connector types were set up. For manufacturing purposes only those pins wired had been identified, but the insulation tests required that all pins on the rack be identified.

12 Software Description

The software can be split into functional areas of system file generation and maintenance; production of a test program in magnetic and paper tape forms; storage of the test program on the analyser disk; retrieval of the test program and an analyser run on the rack under test. For system file generation and maintenance software, programs were of a simple utility nature. Ease of file maintenance using minimum input, and the provision of comprehensive checks and reports were essential.

The interface between the two computers was exactly defined. For each rack an analyser test program was made in magnetic and paper tape forms. This test program was produced by a suite of software programs in sequence. The physical data relating to the rack is extracted from the system files, including shelf heights and details of pre-wiring and special connectors. The engineering input data are read and all the relevant data consisting of wire segments and associated signal name are placed on a disk work file. At the same time the pins used are marked in a complete bit matrix for every pin on the rack. A list of unused pins is thus generated. The

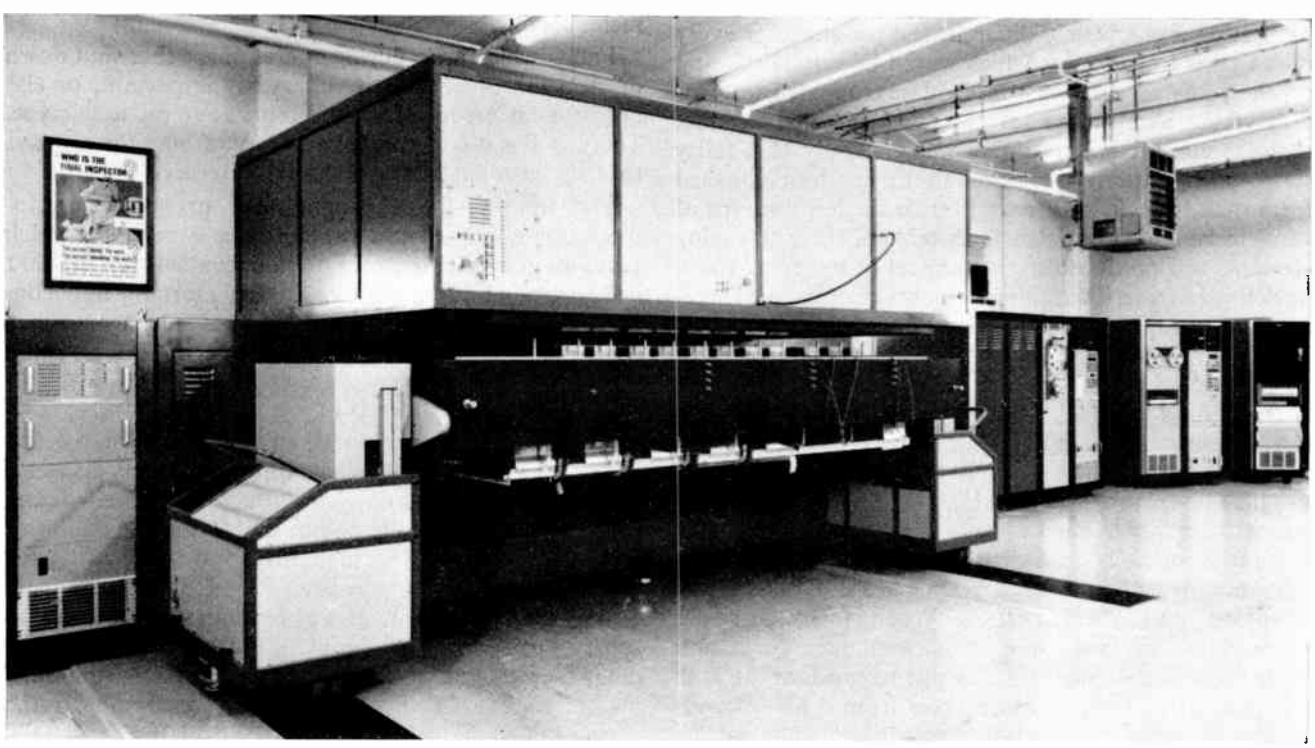

Fig. 6. Overall view of the analyser, computer, and test fixture, showing a TXE 4 rack loaded into a transporter in position for testing.

disk work file is sorted to bring all the wire segments associated with a signal together. One signal at a time is read into core and is checked for logical continuity as one electrical net or is split into several nets. Pre-wiring of TXE 4 connectors is merged at this stage by checking every pin against the table of connectors. These nets are written to a second disk work file which is used by the next stage to break the nets into the separate analyser cycles and output to a third file. A sort is made to divide the information on the third work file by analyser cycle. The list of unused pins is also similarly divided by analyser cycle and is merged with the third work file in producing the final output test program. At this final stage the translation from the manufacturing pin numbering system to that required by the analyser is carried out and extra control information for the analyser is inserted at the start of each cycle.

The separate, one stage at a time approach was essential because of the large volume of data being input and generated. A large rack will have an engineering input of 16 000 card images and an output of 1500 m (5000 ft) of paper tape. Some earth nets have over 1000 pins to be sorted. As the paper tape is only for emergency use, in the event of a mini-computer failure, it only contains data for continuity testing, in order to keep the total quantity of tape to be produced and stored to a manageable amount, and can only contain tests on the basic wiring. The magnetic tape holds all the data for both continuity and leakage tests. The mini-computer will transfer the contents of the magnetic tape to its removable disk pack so that rapid access can be obtained for any stored rack test program.

13 Conclusions

The complete test system is physically very large (Fig. 6), the fixture and cabinet assembly being nearly 6 m (20 ft) from end to end, with a very high capital investment. In addition, the amount of floor space needed to operate all of the peripheral hardware such as rack transporters, and adapter unit handling and servicing facilities, is also high with over 1100 m^2 (12 000 ft^2) of factory floor committed to testing alone. Nevertheless, it has been estimated that the system will pay for itself quite quickly, for instance, the saving on not having to rectify wiring faults during installation alone would probably repay the cost in about three years, apart from obvious savings in other areas.

Therefore, although the initial reasons for acquiring the system were technical, it has also proved to be an investment.

14 Acknowledgments

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Graham Lovitt was educated at Imperial College, London, and Enfield College, studying mathematics and physics. With this background, he joined Standard Telecommunication Laboratories Ltd. in 1964 and for two years was concerned with the study of the optical properties of thin evaporated films used for infra-red optical filters. The mathematical evaluation led naturally into computer programming and in 1966 he was engaged as a full-time analyst programmer in the computer applications division of STL. He is now a senior systems analyst and has worked on various systems including printed circuit board design and a compiler of a high-level test language for circuit boards. Currently he is developing and improving systems for telephone exchange cabling and back plane wiring.

Letters

From: **Professor J. Kroszczyński,** Dr. habil. ing.
J. K. Hsiao, M.Sc., Ph.D.

Dual-frequency M.T.I. System

In a recent paper[1], Hsiao analyses the dual-frequency moving target indication system. While acknowledging that an analysis of this kind of m.t.i. system was conducted in my papers published before,[2,3] he writes further: 'Unfortunately, Kroszczyński's analysis is based on the assumption that the clutter return has only a single Doppler frequency . . . Furthermore, Kroszczyński's result is not in a convenient form to compare with a conventional single-frequency m.t.i. system. In this paper we shall attempt to treat this subject in more general terms.'

I find Hsiao's remarks rather astonishing, because in my second paper[3] the analysis is conducted explicitly under the assumption that both the signal and clutter return are Gaussian stochastic processes (compare the text between eqn. (1) and (2) and summary in Ref. 3). In Hsiao's paper[1] only the clutter return is assumed to be a random process, but the signal has only a single frequency (compare eqns. (2a) and (2b) in Ref. 1). Therefore, I would have serious doubts if Hsiao's approach can be described as treating the subject in more general terms. It should be noted, of course, that Hsiao is to be credited for including in his analysis the effects of noise and an interesting discussion of its influence on the performance of the dual-frequency m.t.i. system.

I would also call attention to the fact that in my second paper[3], eqns. (17) and (21) express the results in a very simple form, containing only the input signal-to-clutter power ratio and the clutter attenuation ratio (CA) of the canceller; the latter is known and has been used for quite a long time in the literature[4] concerning conventional m.t.i. radar systems. The question of convenience may be of course a matter of personal opinion, but I feel that eqns. (16), (17) and (20), (21) in my paper convey essentially the same meaning as expressed in Hsiao's conclusions on page 353 of Ref 1.

In further discussion, one point concerning the method of analysis may be stressed. To derive the improvement factor of a m.t.i. system, the input and output signal-to-interference ratios must be known. For such inherently non-linear systems as the dual-frequency m.t.i. this offers some difficulties, at least as far as the output signal-to-interference ratio is concerned. Hsiao circumvented this by separating appropriate terms in his theoretical expression (eqns. (4 a–f) in Ref. 1), while I have introduced a new concept: the ratio of average power at the output when signal present to the average power at the output when signal absent eqn. (11) in Ref. 3. This ratio can be measured in a straightforward manner at the output of any circuit, while it seems that rather the opposite may be stated in the case of an attempt to measure the signal-to-random clutter ratio at the output of a real, highly non-linear circuit. Therefore, while Hsiao's analysis is quite interesting from a theoretical point of view and gives much insight into the functioning mechanism of the dual-frequency m.t.i. system, it seems that for many applications the other way of approach would be more practical.

At the end of these comments I would like to add that I was very glad to learn that my papers have stimulated interest in the dual-frequency m.t.i. system. In my opinion, Dr. Hsiao conducted a detailed and worthwhile analysis of many aspects of this system and, apart from the points discussed above, I found his paper very interesting.

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29th December 1975

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Kroszczyński's papers on the two-frequency m.t.i. system are interesting and useful. However, I found that certain areas in these papers can be extended. For the first paper, clutter should be treated as a random process. For the second paper, the m.t.i. performances analysis can be extended to the cases of more than three cancelling pulses. Discussion on the choice of optimal filter weights and performance comparison with single-frequency system may be included. Effects of noise should be treated. These motivations were intended to be explained in the introduction to my paper. Unfortunately, during the process of editing, rewriting and oversight on my part, these comments are changed and replaced by sentences which may sound very critical. I regret this and wish to offer my sincere apology to Professor Kroszczyński.

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24th June 1976

(*Editorial Note.* The original copy of Prof. Kroszczyński's letter was lost in transit to Dr. Hsiao.)

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Radio propagation in London at 462 MHz

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SUMMARY

Propagation measurements at 462 MHz relevant to a base station on a ten-storey office block and a mobile operating at seventeen locations in London are described. Signal level as a function of range is given and a slightly altered version of Okumura's prediction is shown to agree well with the measurements. Mean signal level distributions are found to be log normally distributed with a standard deviation of 5 dB. The envelope of the received signal level is shown to have a Rayleigh distribution.

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1 Introduction

Information on radio propagation is necessary for the successful design of mobile radio systems for the police, fire brigade, ambulance service and many commercial users. Propagation is rarely line of sight and generally a number of waves are received at the vehicle by reflection from hills and buildings, etc. The interference of these waves produces a standing wave pattern which gives a variation of field strength (known as 'fading') along the street. As the vehicle moves through the fading pattern rapid fluctuations in the received signal level occur. This paper gives the analysis of measurements of received signal level (or, more accurately, the level of the signal envelope) made during field measurements in London.

A method of predicting the mean received signal level is given in references 1 and 2, based largely on measurements by Okumura *et al.* in Japanese cities and in cities in the USA. In essence the method consists of calculating the free space path loss and adding an empirical excess path loss given in graphical form against range and frequency. Corrections can be made for the base station and vehicle antennae height and for the type of buildings, which may be urban, suburban or rural. Measurements are compared with predictions made in this manner.

The measured signal level information is considered in three ways. First the dependence of the mean signal on range is found; this is needed to determine the coverage given by a transmitter. Secondly, the variation in the mean is found at a given range, which gives the expected error in a signal level prediction. Finally the variation in the received signal level relative to the short term mean is found at a number of locations at which the vehicle was driven over a prearranged route of about 1 km length. In a number of cities in the USA and Japan the signal level has been reported as having a Rayleigh distribution and consequently a 'Rayleigh' model is generally used in assessing diversity techniques aimed at reducing the signal variations. It is therefore important to know whether or not in London the signal level has a Rayleigh distribution.

2 Measurement System

Figure 1 shows a conventional mobile radio receiver front-end driving a precision logarithmic i.f. amplifier and filter. An envelope detector passes the received signal level to an analogue-to-digital converter which samples at 600 Hz to 7-bit accuracy. A single bit from the vehicle odometer (used in vehicle speed measurements not reported here) is added to give a 4800 b/s data signal for recording on a digital cassette recorder. In the laboratory the cassettes are replayed to a Philips P860 mini-computer for analysis. It should be noted that the signal level information is recorded as a function of time, not distance run by the vehicle.

Measurements were made at 462·425 MHz with a base station transmitter of 3·5 watts output mounted on the roof of Mullard House, a ten-storey office block near Tottenham Court Road, London. The vertical base station aerial was 35 m high and had a gain of 2 dB relative to an isotropic aerial. The mobile aerial was 2 m high and had a gain of 5 dB. Signal levels are quoted in

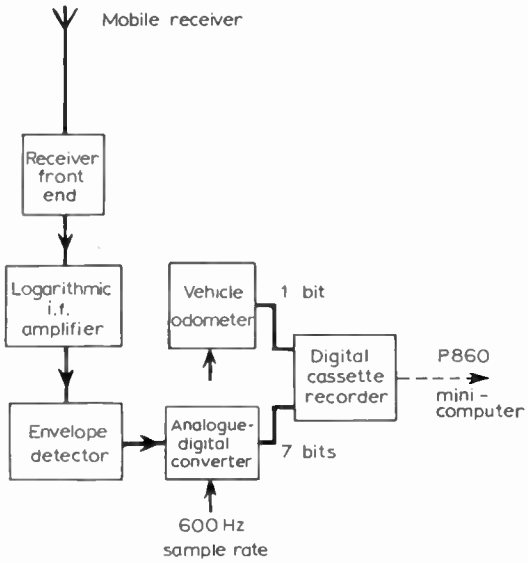

Fig. 1. Measurement system.

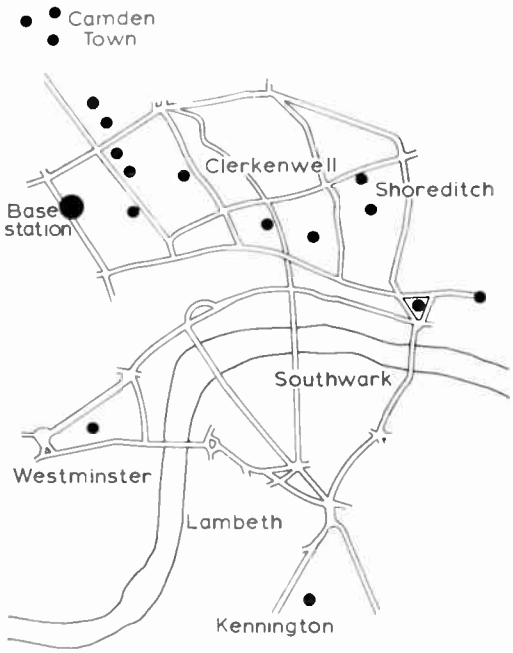

Fig. 2. Locations in London.

dB relative to 1 μV p.d. in 50 ohms (−107 dB mW). A map of some of the seventeen locations where measurements were made is shown in Fig. 2.

3 Mean Signal Level against Range

A mean signal level for a location was found by averaging the $2{\cdot}5 \times 10^5$ signal level samples collected during a seven-minute run over the prearranged route. Before averaging the samples were converted to linear form. Figure 3 shows a plot of these means as a function of range. Each group of points results from repeated measurements at a location.

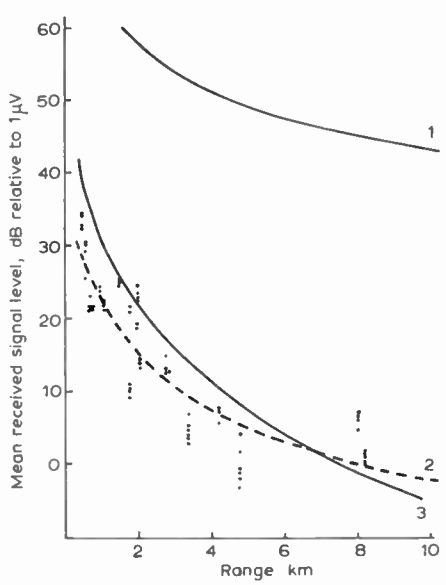

Fig. 3. Mean signal levels as function of range for various conditions (462 MHz).
1. Free space
2. Best fit inverse power law
3. Okumura prediction

Three curves are also plotted in Fig. 3; one is the free-space signal level derived from the equation:

$$P_0 = P_t \left[\frac{c}{4\pi df}\right]^2 g_b g_m \qquad (1)$$

where P_0 and P_t are the received and transmitted signal powers, d and f are the range and frequency in metres and hertz, and g_b and g_m are the base and mobile aerial gains. The second curve in the Figure is an inverse power law where the power has been chosen to give the best fit to the plotted data in the sense of minimizing the r.m.s. error between curve and data points. The third curve is the Okumura prediction obtained from reference 1, with London taken as an urban environment even though its buildings are more suburban in height.

As seen in the Figure the measured signal levels are 30 to 50 dB lower than would be received in free space, according to the inverse square law (curve 1). The Okumura prediction (curve 3) is mainly optimistic and lies about 7·5 dB higher than the best fit inverse power law (curve 2) at 1 km range and about 5 dB at 2·5 km range. At 7 km the curves cross. The best fit inverse power law has a power of 2·5 which shows a faster rate of attenuation than indicated by the inverse square law. This corresponds with the increasing excess path loss with range in the Okumura prediction.

The prediction agrees quite well with the measured data, even though London and Tokyo are very different from a propagation point of view, and Tokyo was the source of the empirical data used in the prediction. London has short streets with random directions and frequent bends and has few tall buildings. The lower buildings make London look more suburban from a propagation point of view which according to reference 1

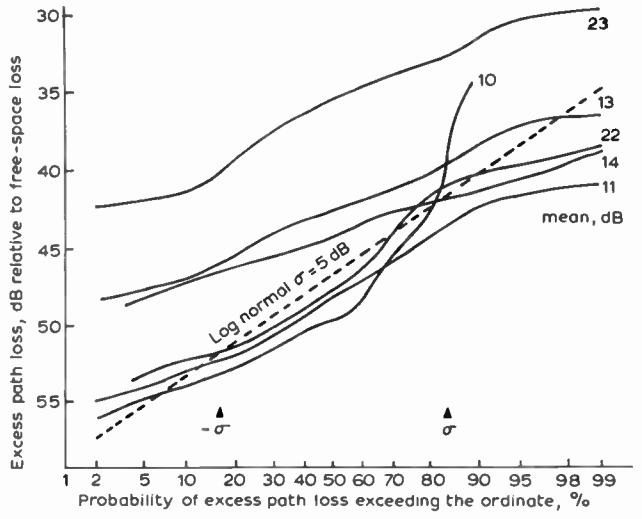

Fig. 4. Cumulative distribution of short-term mean signal level for six locations.

should lead to signal levels 18 dB stronger than in a city. In practice they are 5 dB lower.

One speculation to account for the difference is that London streets will prevent the long range propagation of radio waves that occurs down the streets and avenues of a city built on a grid. Fewer waves will contribute to the sum at each point, leading to lower signal levels.

4 Mean Signal Level Distribution

In Fig. 4 the cumulative distribution of the short term mean signal level is plotted for six locations. For convenience excess path loss is plotted (free space signal—mean) rather than the mean. The probability axis is scaled so that a variable with log normal distribution will give a straight line.

A short-term mean is calculated over 2800 signal samples, corresponding to 4·7 seconds or 42 m at 20 miles/h. The next short-term mean is found by adding 400 new samples and discarding the oldest 400, giving in effect a sliding mean. Between 300 and 600 such means are used in the distributions of Fig. 4.

The plotted curves show a reasonable approximation to log normal in the 10 to 90% region, which is all that can be expected with the number of measurements made. The standard deviation of the distributions is about 5 dB which agrees well with the result of 6 dB in reference 1 (page 123).

5 Signal Level Distributions

The received signal level varies as the vehicle moves along a street. There are two aspects to this variation, one is the rapid variation caused by multi-path propagation and the other is a much slower variation due to changes in parameters like street width or building height. The first is wave interference, which can result in sharp nulls caused by wave cancellation, and the second is shadowing. To study the rapid variations due to fading it is necessary to separate them from the slower changes in signal level, which result from a different mechanism and have a different statistic. The slower variations are represented by the short-term means found above and the rapid variations are extracted by normalizing the signal levels to their short-term mean. Four hundred signal samples are considered at a time and normalized to a mean extending over 2800 samples centred on the 400.

The cumulative distribution of the signal level relative to the short-term mean is plotted on a probability axis scaled by the function:

$$y = \text{constant} + \frac{1}{n}\log_{10}(-\log_e \text{prob}) \qquad (2)$$

Consequently functions with a cumulative distribution of the form:

$$y = \exp(-x^n) \qquad (3)$$

will give a straight line, of slope equal to n. The Rayleigh distribution has $n = 2$ and this slope is shown in Figs 5 and 6 where the results for a number of locations are given. (The $\log_{10}$ is included because the signal is plotted in dB.)

Figure 5 shows the distribution for three locations where the mean signal level is about 20 dB. The distribu-

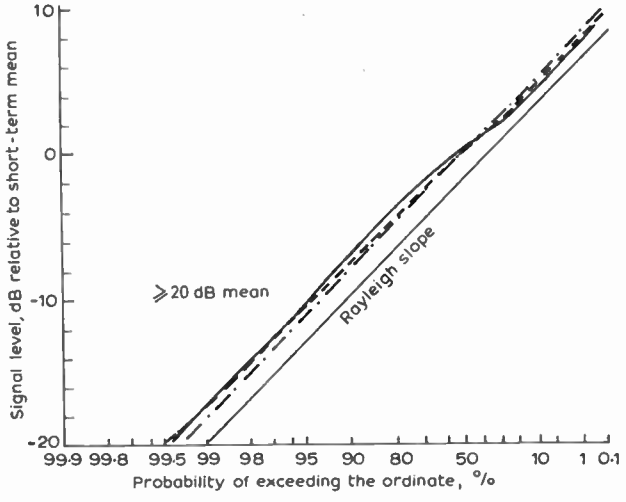

Fig. 5. Signal level distributions for three locations.

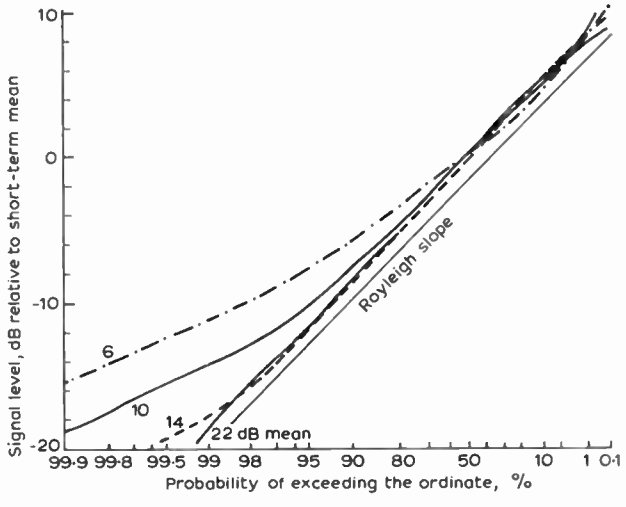

Fig. 6. Signal level distribution for four locations.

tions are very close to Rayleigh, and are typical of six such results. Figure 6 shows the distributions in four locations with long-term mean signal levels ranging from 6 dB to 22 dB. With a long-term mean of 6 dB the plotted distribution falls away from the 'Rayleigh' slope for relative signal levels below 0 dB, indicating an increased probability of exceeding these low signal levels. This is caused by receiver front-end noise which produces an output from the envelope detector during the deeper fades which obscures the distribution of the smaller signal levels. To prevent the receiver noise ($\sim$0 dB) from obscuring a signal distribution down to -20 dB relative to the short-term mean, the short-term mean must be greater than 20 dB. With lower means the departure from a straight line does not indicate a non-Rayleigh distribution. The conclusion is that where the mean signal level permits a valid measurement the signal level has a Rayleigh distribution.

6 Conclusions

Propagation measurements in London at 462 MHz have shown that the mean signal level as a function of range can be predicted using Okumura's method (and subtracting 5 dB). In the prediction London is considered to be an urban environment even though its building height is nearer to suburban by American and Japanese standards. Alternatively the propagation can be taken to be inverse 2·5 power law with an excess path loss of 20 dB.

London's short streets with their random orientation is offered as a reason why the lower building height in London compared with those of Tokyo has not resulted in signal levels higher than predicted.

The mean signal level has been shown to be roughly log normally distributed with a standard deviation of 5 dB. The prediction method is therefore useful since the probable error is quite small.

The signal level (envelope) has been shown to have a Rayleigh distribution for a variety of locations in London.

7 Acknowledgments

I should like to acknowledge the contribution made to this work by my colleagues P. J. Mabey, R. Wells, T. W. Whiter and K. J. Wheatley; and to thank Pye Telecommunications, Cambridge, for their advice about the radio equipment.

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A circuit for high-speed carry propagation in l.s.i.-f.e.t. technology

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and
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SUMMARY

A circuit configuration for high-speed carry propagation employing serial floating field effect transistors in parallel digital adders is presented. Circuit parameters affecting the performance of the suggested configuration are evaluated. Results of comparisons with alternative m.s.i. and l.s.i. adder circuits are given and show that the present suggestion is superior to the alternatives.

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1 Introduction

The speed of parallel binary adders is affected, mainly, by the speed of carry propagation. Many methods of speeding-up carry propagation are known.[1] The most popular methods rely on some variation of the carry-look-ahead technique which is, in fact, a procedure for resolving the problems of fan-in and fan-out limitations of the logic circuit. Another method, carry completion detection, relies on the fact that the average length of propagation is obviously shorter than the full length of the adder —which is the maximum length of propagation. A different solution to the same problem employs a special high-speed switch in the carry chain.[2,3] This circuit which is, conceptually, very simple has not, apparently, become popular with logic circuit designers and manufacturers, probably because of circuit complications involved in the realization of the serial switch.

The dramatic increase in recent years of the usage of f.e.t. technology in digital systems justifies an updated evaluation of the carry problem under the constraints of that technology. This is true in particular when considering m.s.i. and l.s.i. circuits.

Two features of the field effect transistor prove to be important with regard to its implementation in the serial switch configuration:

(1) its general characteristics as a switch,

(2) the action of the f.e.t. as a floating device.

Generally, the f.e.t. proved to be very suitable for use in the configuration of serial switch. Nevertheless, because f.e.t.s are not in fact, perfect switches, the actual performance achieved with the carry circuit is device dependent and its behaviour and characteristics are investigated in the sequel.

2 Carry Propagation Employing Serial Switches

A possible elementary representation of sum (S_i) and carry (C_i) equations for stage i of an adder with inputs X_i and Y_i follows in equations (1) and (2):

$$S_i = (X_i Y_i U \overline{X}_i \overline{Y}_i) C_{i-1} U (X_i \overline{Y}_i U \overline{X}_i Y_i) \overline{C}_{i-1} \quad (1)$$

$$C_i = X_i Y_i U X_i C_{i-1} U Y_i C_{i-1} \quad (2)$$

The dependence of the carry of stage i on stage $i-1$ and consequently on all previous stages is apparent. Another carry logic configuration which employs a serial switch is presented in Fig. 1. The circuit employs three switches $G1_i$, $G0_i$ and Q_i. The action of this circuit is as follows: switch $G0_i$ is closed when $\overline{X}_i$ and $\overline{Y}_i = 1$ and forces $C_i = 0$, switch $G1_i$ is closed when X_i and $Y_i = 1$ and forces $C_i = 1$ and finally switch Q_i is closed when $X_i \neq Y_i$ and causes $C_i = C_{i-1}$. The three cases are the 'zero carry' generation, 'one carry' generation and 'carry-propagate' conditions respectively. For any input combination one and only one of the three switches is closed. For an n bit parallel adder ($i = 1, n$), all switches in the n stages are controlled concurrently when X_i and Y_i ($i = 1, n$) are applied. The speed of addition is dependent on the speed of propagation of the carry signal which, in worst case must be propagated via the series of all switches Q_i (in fact for addition $i = 2, n$ only

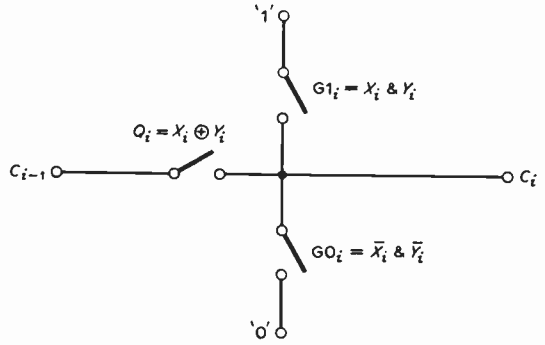

Fig. 1. Carry circuit.

but in other operations the first stage may be involved also). That is, the total delay of an adder based on this configuration consists of three parts: (1) delay of concurrent actuation of switches $G0_i$, $G1_i$ and Q_i in all stages. (2) Propagation of the carry via all stages in which carry propagation conditions exist, and (3) sum generation—which, for any stage of the adder, can be generated only after its input carry is known.

In many cases a major effort is devoted to minimization of carry propagation delay. Adder circuits based on this configuration employing bi-polar germanium transistors have been reported by the previously mentioned sources. But, as stated in the Introduction, the two versions of the circuit seemed to have encountered severe problems which have actually prevented their wide acceptance in the industry. To the best of the authors' knowledge no equivalent circuit using silicon transistors has been adapted probably because of similar reasons. In particular, the specifications of switch Q_i necessitate the employment of a 'symmetrical' floating switch which can propagate signals of both polarities. This symmetry is difficult to achieve in planar bi-polar silicon integrated circuits technology.

3 An Adder Stage Employing Field Effect Transistors

A circuit implementing one stage of the adder using m.o.s. circuits is shown in Fig. 2. The logic gates A_i, B_i, D_i and S_i perform the input and sum logic, A_i being a NOR and D_i a NAND gate while B_i and S_i are exclusive-OR gates. B_i provides the invert of its output also.

Assuming positive logic (high for '1') a p-type transistor acts as a $G1_i$ switch an n-type transistor acts as $G0_i$ switch. A parallel combination of a p and n transistor provide for the Q_i switch. In similar manner to the operations of the switches explained with regard to Fig. 1, here also when both X_i and Y_i are '1', D_i is low and causes $G1_i$ to conduct forcing '1' to C_i; under these conditions transistors $G0_i$ and Q_i are non-conducting. Similarly when both X_i and Y_i are '0' (low) A_i is high causing $G0_i$ to conduct forcing '0' to C_i. Finally, when either X_i or Y_i is '1' but not both of them, one of the transistors in switch Q_i conducts causing $C_i = C_{i-1}$. In this case, transistors $G1_i$ and $G0_i$ are non-conducting. Gate S_i performs the sum logic in a simple manner.

The explanation so far deals with the static behaviour of the circuit. Dynamically other problems arise. First,

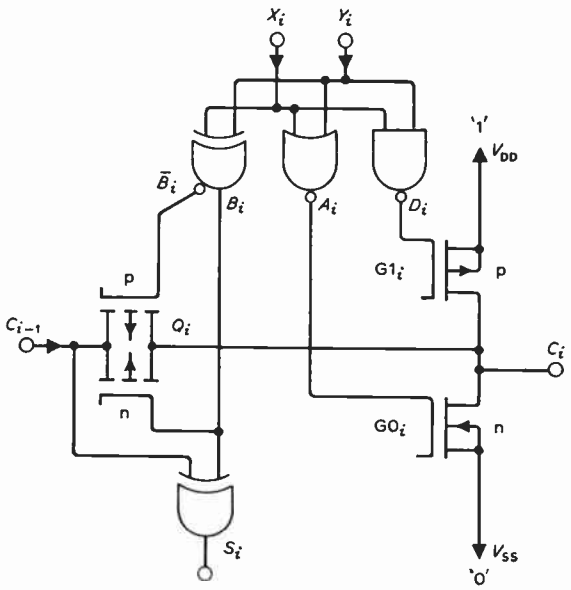

Fig. 2. Full adder stage.

under transient conditions more than one switch may be conducting. The effect of this is to reduce the speed of the initial settling time but has no accumulative effect on the operation of the parallel adder. The extra current and power dissipated as a result of this transient effect is limited by the internal impedance of the transistors and practically may be neglected.

Also, the transistors do not behave as ideal switches, in particular input and output capacitances of the various components and the resistance of conducting transistors have appreciable effect on the speed of operation of this configuration. This problem is discussed in detail in the following Section.

4 An *n*-stage Parallel Adder

Using the basic circuit of Fig. 2 a parallel adder is implemented by connecting such stages in series. An *n*-bit parallel adder uses *n* stages in which the 'carry out' line of one stage is connected as 'carry in' of the next stage. The 'carry in' of the first stage is controlled in the proper way. In order to be able to evaluate the dynamic performance of the parallel adder, in particular its behaviour in the carry propagate mode, its equivalent circuit may be studied. In the state of carry propagation, a single-stage carry circuit can be replaced by an equivalent *RC* network and the whole adder carry circuit may be represented by an *RC* ladder network being driven by a voltage step. *R* represents the resistance of the conducting serial transistor and *C* the total capacitance loading the carry out node. In the present work the lumped parameter equivalent circuit proved to give good results when compared to experimental measurements as is shown in the following Sections.

Note that in practice the driver is not an ideal voltage source and the real circuit should be approximated by shaping the source accordingly. The delay T_D, and the rise-time, T_R of the ladder network have been calculated for a practical circuit using a circuit simulation program

(Appendix I) and the strong dependence of T_R and T_D on the number of stages is obvious. Comparable results have been obtained when calculating the 'Elmore'[4] delay $T_{(e)D}$ and rise-time $T_{(e)R}$ for an RC ladder network fed by a voltage source. It can be shown that at any point M of an N stage RC ladder:[8]

$$T_{(e)D} = \frac{RC}{2}\left[N^2-(N-M)^2\right] \tag{3}$$

which for the case $M = N$ reduces to:

$$T_{(e)D} = \frac{RC}{2}N^2 \tag{4}$$

Also, from calculations for specific values of RC, it was found that[6]

$$T_{(e)R} \gtrsim RCN^2. \tag{5}$$

For practical circuits T_R may become prohibitive and measures are needed for its reduction. This can be achieved, at the expense of increasing the delay T_D, by just introducing buffer stages at selected points along the carry path.

5 An Adder Circuit for Experimental Evaluation

In order to evaluate the proposed configuration experimentally an adder was built using available c.m.o.s. i.c.s, components from the RCA CD4000A series[5] being chosen. The circuit for a one-stage full adder (Fig. 3), consists of two NOR gates (type 4001) and two 'exclusive-OR' gates (type 4030) for performing input and sum logic and three bilateral switches (type 4016) for the carry. All interconnections between packages were done by wiring. Measurements reported here are for 10 V supply at room temperature (25°C).

The settling time for the input logic was measured to be equal to 44 ns. Similarly, the delay of the sum logic measured with respect to the carry in signal was 28 ns. Note that these measured delays are about 25% faster than those expected from the typical delay times quoted in data sheets.

In order to measure the carry propagation delay an 8-stage adder, shown in Fig. 4, was built on a 10 × 15 cm board. Inverters C_0, C_7 and C_8 are added for the purpose of reshaping of signals.

Carry propagate conditions are established at inputs X and Y and a pulse generator feeds carry signal to input of C_0. Shapes of wave forms at various points along the carry path are reproduced in Fig. 5. C_{0g} and C_0 are, respectively, the unloaded and loaded output signals of inverter C_0.

The measured results for this circuit are summarized in Table 1. The current limiting effect due to the input stage, C_0, driving the ladder network is manifested by the initial linear rise time of the waveforms. The knee in the waveforms at about the threshold voltage due to the higher resistance of the transistor is evident.

Table 1. Measured results for the 8-stage adder.

Stage No.	T_D (ns)	T_R (ns)
C_0	55	165
C_1	68	250
C_2	85	300
C_3	105	330
C_4	115	360
C_5	130	365
C_6	140	370
C_7	155	375

These results, for the higher stages, such as stages 6 and 7 are in good agreement with the results accepted from *ECAP* simulation for an RC ladder network with $R = 250\ \Omega$, $C = 21$ pF (these values for R and C are deduced from the manufacturer's data on devices being used) and source current limit of 7 mA as presented in

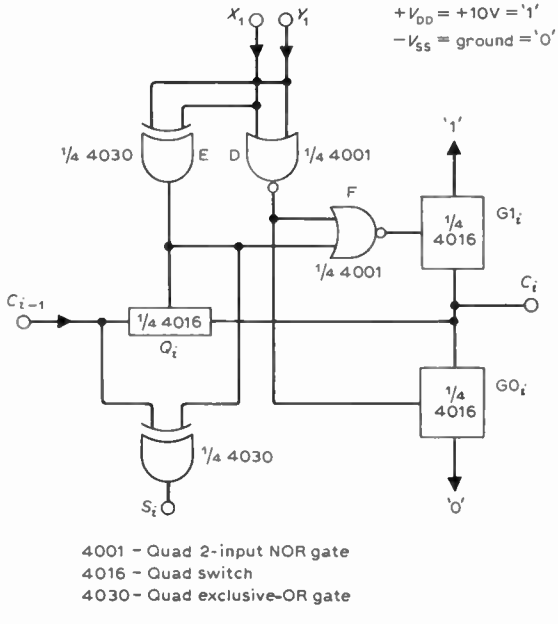

Fig. 3. C-m.o.s. adder stage.

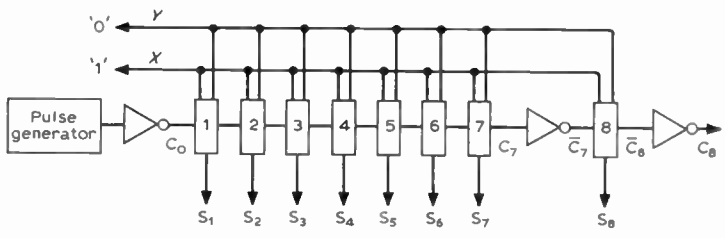

Fig. 4. Eight-stage adder—carry delay measurement.

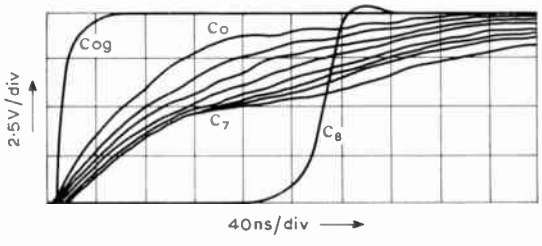

Fig. 5. Carry waveforms—8-bit adder.

Table 2 of Appendix 1. Also, the results are in fair agreement with the Elmore delay, $T_{(e)D}$, and rise-times, $T_{(e)R}$, calculated for a similar circuit (Appendix 2).

6 Improved Speed Performance of the Adder and Comparison with Commercial M.S.I. Adder Circuit

In order to improve the speed performance of the present basic configuration, several methods are possible. Generally one can try either to improve the logical configuration of the adder or to improve the electronic circuit performance. Obviously, faster operation of the same adder, if manufactured on a single chip (m.s.i.), is to be expected as a result of the reduction of C due to compact packaging; C may be decreased by at least 10 pF, resulting in doubling the speed of the carry path (excluding buffer delays). Further reduction can be achieved by proper control of manufacturing process aiming at reduction of either R or C or both. (Just for reference purpose it is worthwhile to note that m.o.s. f.e.t. with equivalent R of the order of 20 Ω (e.g. 3N214) while C is about the same, are commercially available). Using similar transistors in the carry path will result in an order of magnitude of further improvement.

A different approach to speeding up the operation of the adder is possible employing logical techniques, such as carry look-ahead (Ref. 1, p. 68). For evaluation purposes a 4-bit block with carry skip over the four stages was built, enabling comparison with the four-bit full adder RCA type CD40008A. The proposed circuit in Fig. 6 incorporates both a skip circuit and buffers following stages 2 and 4 of the adder thus avoiding the rise-time problem while still preserving the same phase for carry signals at input and output of the unit. Similarly, inverters have been introduced in the sum circuits of stages 3 and 4.

An 8-bit adder consisting of two 4-bit blocks was implemented using, as before, standard i.c.s and carry delay was measured. The delay of C_8 is about 175 ns, 80 ns of which are due to the four buffer stages in the carry path. One should note that, for this configuration, the worst case delay for the 1st unit (the low-order 4 bits) is in fact the delay involved in propagating a carry generated in the first stage via the switches of the 2nd, 3rd and 4th stages. Of course, a full carry look-ahead adder could be designed which, in this respect, will improve the performance.

When comparing the suggested configuration with the commercially available RCA CD4008A, one should remember that the latter employs extensive measures for improving the performance of the carry path: these include minimization of capacitance loading and improving gate performance along the carry path. The carry path in this adder consists of two 2-inputs NAND gates connected in series.

From typical delays quoted in data sheets for CD4008A one gets, for example, for a 16-bit configuration a typical delay of 535 ns for addition. For this circuit there is an appreciable deterioration of the transition times of output signals which will slow the adder in practice even more. For the experimental adder the equivalent value

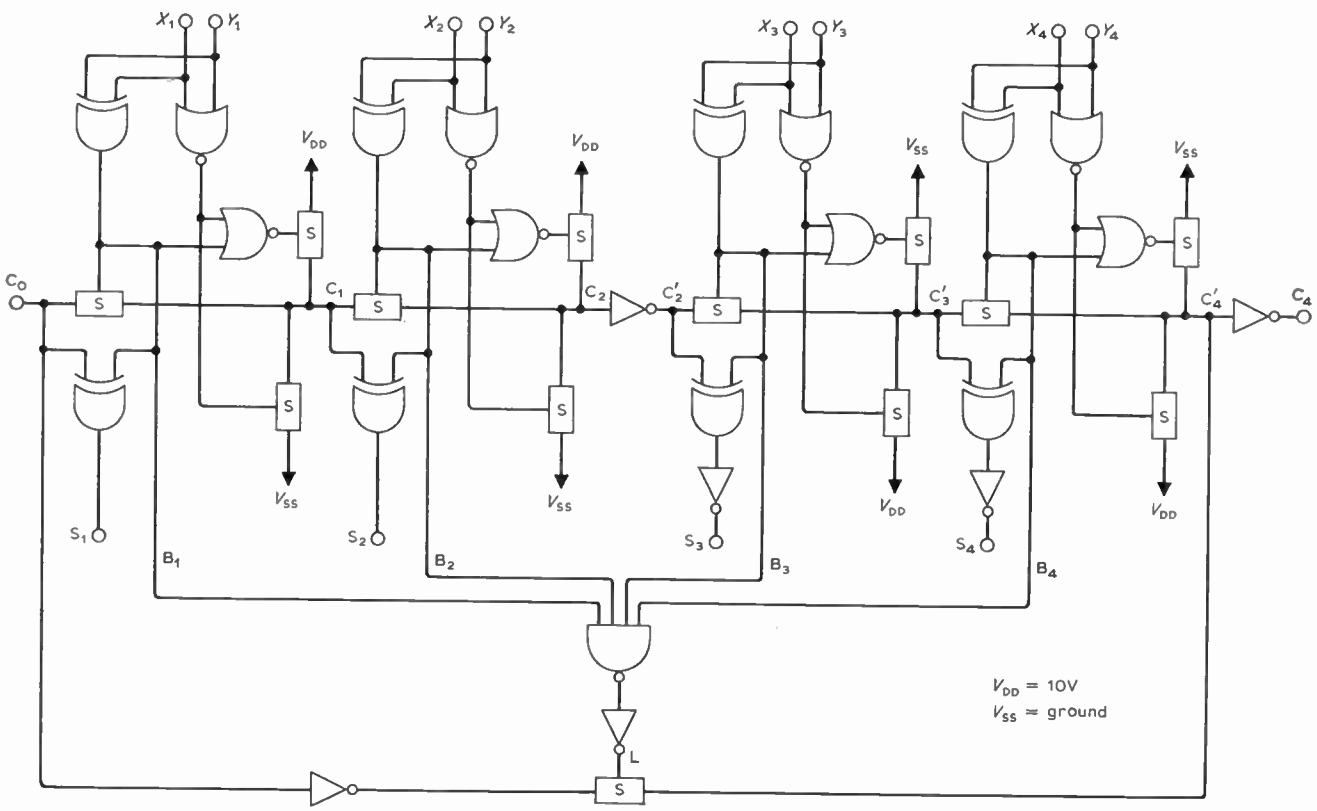

Fig. 6. Four-bit adder block with skip.

is 430 ns. Using the techniques mentioned previously, namely manufacturing an m.s.i. device and controlling the 'on' resistance of the signal transistors, the results can be improved appreciably. The transistor count in the CD4008A unit is 158, the 4-bit adder block described in the present work consists of 154 transistors. Both counts are practically the same though the latter can be reduced somewhat at the expense of non-uniform phases of input and output signals. Also transistor count in the latter adder can be further reduced by employing different logic configuration in the input logic at the expense of somewhat longer delay for settling of the input logic. Since, as described before, this occurs in parallel for all stages it will not affect the total delay appreciably.

7 Conclusions

An evaluation of the performance of the proposed scheme for high-speed carry propagation in f.e.t. technology has been presented. The configuration is flexible enabling many circuit combinations to be adapted. In particular, it can be easily adapted to m.s.i. and l.s.i. manufacturing processes benefitting from the reduction of stray capacitance loading associated with it. Further speed improvement can be achieved by improving device characteristics, in particular those of the serial switches.

Other logic configurations, such as counters, decoders and more complex units may benefit from using the serial floating switch circuit.

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9 Appendix 1: Calculations of T_R and T_D of Adder Circuit

The equivalent circuit of the carry path for the adder circuit used in the calculation is shown in Fig. 7. This circuit was simulated using *ECAP*.[7] The response to a

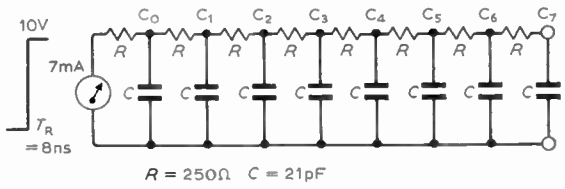

Fig. 7. Equivalent circuit for 8 bits adder.

voltage step of 10 V, T_R = 8 ns and current limit of 7 mA was calculated and the results are shown in Table 2. T_R is measured between the 10% to 90% points and T_D is the delay to the 50% points of the waveforms measured at the specified points of the circuit.

Table 2. *ECAP* calculation of T_R and T_D.

Carry	T_D (ns)	T_R (ns)
C_0	35	152
C_1	60	251
C_2	85	296
C_3	110	329
C_4	135	341
C_5	150	350
C_6	162	350
C_7	167	350

These results are in fair agreement with the results accepted in the experimental measurements, especially for the higher stages 4 to 7.

10 Appendix 2: Calculation of $T_{(e)D}$ and $T_{(e)R}$

Table 3 denotes the results for R = 250 Ω, C = 21 pF (RC = 5·25 ns) which apply to the experimental 8-stage carry circuit. For this ladder circuit N = 8. The values of $T_{(e)R}$ were calculated using Elmore equations.

Table 3. Calculation of $T_{(e)D}$ and $T_{(e)R}$.

M	Stage No.	$T_{(e)D}$		$T_{(e)R}$	
		RC units	ns	RC units	ns
1	0	7·5	39·4	42·2	221
2	1	14·0	73·5	54·3	285
3	2	19·5	102·4	60·5	317
4	3	24·0	126	63·6	334
5	4	27·5	144·7	65·1	341
6	5	30·0	157·5	65·6	344
7	6	31·5	165·4	65·7	345
8	7	32	168·0	65·7	345

These results are in good agreement with the results of Tables 1 and 2.

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Letters

From:
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R. Benjamin, D.Sc., Ph.D., C.Eng., F.I.E.E., F.I.E.R.E.

Delays for Wide-band Superdirective Beam Forming

Dr. Benjamin's paper in the September 1975 issue of *The Radio and Electronic Engineer** gives a systematic account of superdirective arrays which has long been needed but there are some details which could be further discussed.

The author writes entirely in terms of receiving aerials and so does not explicitly refer to the fact that a superdirective array used for transmitting has a lower radiation resistance and feed-point resistance than a 'normal' array. He does refer to 'the poor match to free space' towards the end of Section 20, but this is not quite the same since one can match the drive source to the feed-point resistance by means of a transformer or the like, provided this resistance is not so low as to be comparable with the material loss resistance of the array. For a transmitter one is concerned with the overall match between drive and free space; and for a receiver one is concerned with the ratio between power delivered to the receiver and radiation power incident on the area of the array.

The law of channel capacity resulting from Shannon's work is best put in the form:

$$I = BT \log (1 + S/N) + \log \varepsilon$$

where ε is the error rate which is to be tolerated. (Transforming to $C = I/T$ may be regarded as a device for suppressing the error term on the assumption that $T \rightarrow \infty$). If we tacitly drop the log ε term, which is of course negative, this leads directly to the author's:

$$I \propto BT\theta\, D \log (1 + S/N)$$

In order to keep I dimensionless, the aperture D is presumably d/λ where d is the geometric dimension of the array.

From a transmitting viewpoint, the ambiguity between *superdirectivity* and *supergain* can be avoided by using the concept of *directional gain*. This is measured for a transmitting array by the reduction in input power to the array compared with the input power to a reference radiator (usually $\lambda/2$ dipole) which would produce the same signal strength in the favoured direction. The same concept can be applied to reception if one considers the power delivered from an aerial or aerial system to a receiver for a given incident field-strength. Hence I am puzzled by the author's conclusion (2). However, I admit that this argument does not necessarily apply to near-field noise and I am in doubt whether the reverberation or clutter found in practice falls in the category of near-field or far-field noise.

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1st June 1976

Professor Bell makes some useful points in amplification of my original paper. My main concern has been with superdirective reception, where the phenomenon can be of proven practical value when the performance is otherwise limited by external far-field noise. (A forthcoming paper of mine in this Journal defines this condition in quantitative terms.†) The mechanism I have discussed entails a degree of *cancellation* of the incident signal for all directions of arrival, with least rejection for signals from the desired direction. Hence it produces superdirective enhancement of relative directivity, but a reduction of gain. In the external-noise limited scenario, it is the resulting 'factor of superdirectivity' which defines the enhancement in directional discrimination—i.e. the benefit sought—whilst Professor Bell's 'directional gain' determines the crossover point where the system becomes near-field or thermal noise limited.

Superdirective reception cannot increase the energy incident on the given aperture or avoid mutual coupling between closely-spaced elements. We can however minimize interaction, by applying amplitude weightings and sign changes only to the independently-amplified signals from the various antenna elements. This superdirective processing may then be performed in an on-line analogue circuit or by off-line computation.

The nearest equivalent process in transmission would entail the superposition of fields which cancel to some extent in the desired direction but more completely in other directions. It is this cancellation which accounts for the low impedance referred to by Professor Bell. Any low-loss mechanism for returning the rejected field-energy to the antenna-drive network for re-use might then produce some increase in directional gain relative to a conventional array. This would however entail a high-Q recirculation and hence a narrow bandwidth.

I suspect that the persistent failure to produce practically useful transmitting antennas of this type has diverted attention from the real utility of superdirectional receiving antennas in a significant—though limited—range of appropriate applications. Similarly, the high-Q and narrow bandwidth arising from the attempt to maximize directional gain has diverted attention from the fact that superdirective processing of received signals can be designed to cover a very wide bandwidth.

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14th June 1976

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*'On the use of delays for wide-band superdirective beam forming in endfire and broadside arrays', *The Radio and Electronic Engineer*, 45, No. 9, pp. 451–61, September 1975.

†Superselectivity in the azimuth and frequency dimensions, *The Radio and Electronic Engineer*, 46, 1976. (To be published.)

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Trends in failure survival techniques for avionic systems

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Based on a paper presented at meetings of the West Midland Section at Cosford on 2nd October 1974 and the Kent Section at Rochester on 25th September 1975.

SUMMARY

Electronic equipment installed in aircraft has to satisfy extremely demanding requirements to achieve the requisite levels of safety and reliability, while operating in a physical environment at variance with the desirable conditions for long life of electronic components. The techniques in present use are reviewed, in particular the use of digital control systems, and likely future developments are surveyed.

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1 Introduction

Avionic systems exist to make it possible for the crew of an aircraft to fly, navigate, detect and find ground cues, intercept and strike, depending on the role of the aircraft. There are few functions which are performed entirely automatically; most involve the crew in some sort of management task in selecting a role and a performance datum for an avionic system such as the selection of waypoints, the choice and tuning of radio aids and the identification of a destination or target. All require some degree of supervision by the crew who alone are responsible for the success of the mission.

The efficacy of an avionic system is judged on a number of counts amongst which are the following:

(1) Safety, i.e. an acceptably low probability of catastrophic failure.

(2) Performance, including accuracy and independence of outside influences.

(3) The acceptability of the workload they demand from the crew (a) under normal conditions and (b) in the presence of in-flight failures.

(4) The availability, defined as the proportion of 'on' time in which with acceptable maintenance they can carry out their task with acceptable performance.

(5) Their total cost of ownership, being a sum of first cost and cost of maintenance in service.

In order to meet requirements (1) and (3) for safety and acceptable crew workload, the more essential services incorporate spare capacity or redundancy in the form of a number of lanes of control arranged in such a way that if one lane should fail the facility can be carried out effectively by the remaining lane or lanes. The special problems which arise are concerned with implementing changeover of control with very high reliability and speed, and engineering the system at an economic cost.

2 Particular Problems in Failure-Surviving Avionic Systems

The particular problems arising in redundant avionic systems stem from the near impossibility of carrying out repairs in flight and the very short times available in flight for diagnosing defects and restoring the system to an acceptable state following a random failure. Recovery from a flight control system defect is commonly demanded in at most tens of milliseconds, of primary flight data and powerplants seconds at most, and of navigation systems, tens of seconds. The configuration of a system adopted for in-flight failure survival depends critically on this permitted time out of service. Automatic reversion to manual or alternative electrical paths must be provided on the most critical systems, but whether reversion is automatic or as a result of crew action, the indications must have a very high probability of correctness and must reduce to a minimum the likelihood of pilot error (the primary cause of aircraft accidents). A system providing failure survival together with the property of a very low probability of incorrect status indication is termed a high integrity system. As the effect of a false

indication of failed status is highly disruptive of the capacity of the crew to cope with situations, the nuisance warning rate must be kept low; conventionally a nuisance warning in a critical system such as an automatic landing system is classed as being as significant as complete system failure.

Satisfying these requirements while maintaining an acceptable cost of ownership presents a challenging problem.

The in-service maintenance cost of an average avionic system unit throughout its working life is commonly twice its first cost. The cost factor attributable to an essential 'dispatch critical' system tends to be higher as the standards of overall performance are correspondingly greater and the crew more likely to declare it faulty in cases of doubt. An additional less tangible cost in service is that of training the crew to be able to cope with in-flight failures and providing sufficient practice to ensure that their reactions are correct in times of stress.

This factor is alleviated if the operating procedures can be made to change as little as possible when a failure has been detected, isolated and by-passed.

3 Trends in Requirements and Techniques

Redundancy is commonly provided in the following avionic systems:

Autostabilization

Primary attitude sensors

Automatic pilot systems

Power plant control, including on-line engine control, air intake control, automatic throttle

Primary power systems, in the form of automatic 'changeover' systems.

It is also provided in the form of automatic monitoring, but with reversion involving the crew in decision taking, in systems such as:

Air data sensing

Navigation

Primary flight instruments.

The failure survival performance, whether the crew are involved or not, depends vitally on the ability to detect failures with some degree of certainty. Two basic approaches may be compared, namely:

Monitoring or built-in test equipment, and Cross-comparison.

The former is based on a built-in test facility, which is capable of detecting failures by exercising the function under test according to a set of pre-determined rules. Experience with small on-line digital computers in particular shows that a fair degree of confidence in status can be obtained by quite a simple test routine. The general-purpose computer which can read instructions, add, jump and collate is highly likely to be capable of all its functions (in the absence of design defects). Figure 1 is a summary of built-in test performance for a number of differing digital avionic systems and shows that for a modest penalty an 80% confidence in status can be obtained. For more essential systems however where

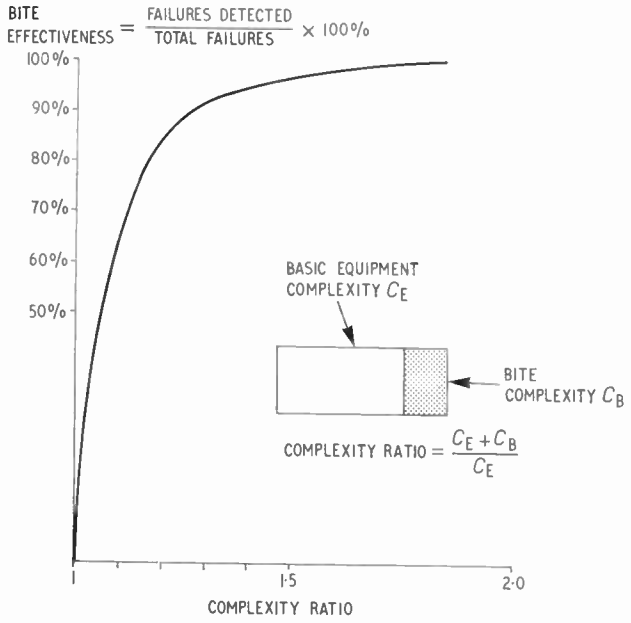

Fig. 1. Relation between monitoring effectiveness of built-in test equipment (BITE) and the complexity of the system.

confidence limits of 99·99% are typically required, experience shows that a large increase in complexity in additional software (and hence storage capacity and run time) and additional monitoring hardware are required. To achieve such levels of confidence therefore it is more economic to provide an additional comparison channel and cross-compare the outputs, as the total hardware cost will not be greater and the performance is not degraded by the necessity to add to the control program many interleaved program sectors for test purposes.

4 Failure Survival Flight Control Systems

The most demanding application up to the present has been flight control because of the rapidity with which control runaways can put the aircraft into dangerous attitudes, and the difficulty of crew-activated recovery at high speeds and near proximity to the ground. The discussion on techniques will thus be centred on this application (Fig. 2).

Failure survival flight control systems have always made high demands for accuracy in computation. This arises for two main reasons. Firstly the dynamic range of the sensor outputs is high. To provide an acceptable ride and to make the aircraft into a stable weapon-aiming platform the rates of turn must be controlled to fractions of a degree per second. At the same time the instantaneous rates of turn in yaw, pitch, and particularly roll reach values measured in radians per second. The control servos operating on the error signal must have better than 12 bit resolution, i.e. 1 part in 4096. Since also the only valid method of monitoring performance is cross-comparison with another similar channel (there are no absolute standards of reference) it is important to make allowance for statistical variations in the differences between the outputs of the lanes which will occur in the absence of malfunction. Such variations can cause the

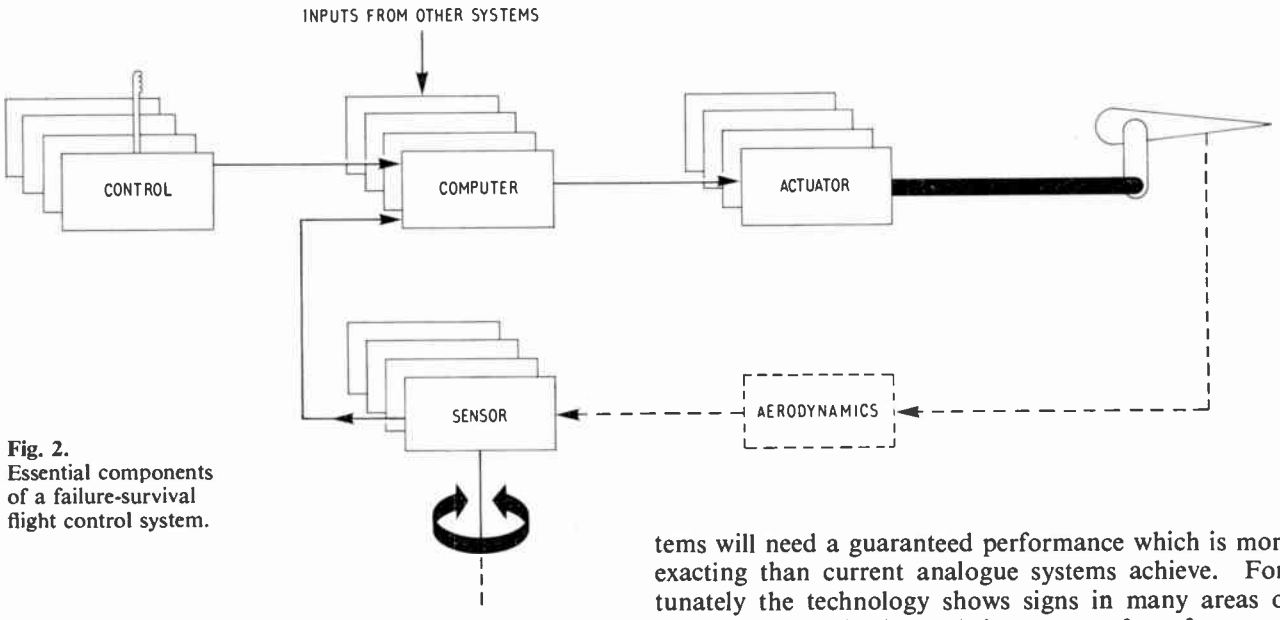

Fig. 2.
Essential components of a failure-survival flight control system.

comparators to trip out the system unnecessarily, and therefore provision must be made for a 'statistical' tolerance band between lanes within which the comparators will not initiate disconnect but which is sufficiently narrow to catch failures before too much disparity occurs. The difficulty of maintaining such a tracking accuracy leads to two alternative solutions—analogue computing broken up into segments with many cross-comparison points to avoid tolerance build-up, or digital systems operating within 1-bit precision on a consolidated set of inputs. With the increasing requirement for complexity of calculation arising from high performance in a number of different flight regimes and the availability of relatively cheap digital components, the cost effective solution tends now to be digital. This solution also offers some flexibility in meeting changes to the servo response characteristics in that major changes to transfer functions are accomplished as easily and in the same way as minor ones.

The requirement in terms of failure-survival ability is also tending to escalate. An automatic landing system specification currently demands a probability of system failure of 10^{-7} per landing in which the time at risk of the system is conventionally 30 seconds. On the drawing board in the UK and in prototype flight in the USA, however, are aircraft which demand working automatic flight control facilities throughout flight, increasing the time at risk to several hours. This arises because more efficient and more manoeuvrable airframes can be designed if automatic stabilization can take the place of inherent stability, to the extent that manual flying is not possible or demands an unacceptable pilot work-load (active control technology). At the same time the use of vectored thrust and direct lift control demand a similar degree of integrity from powerplant control and the control of surfaces in addition to the primary flying controls. The trends to eliminate mechanical reversion in flight control and in powerplant systems also increase the demands for integrity.[1] Thus the emerging digital systems will need a guaranteed performance which is more exacting than current analogue systems achieve. Fortunately the technology shows signs in many areas of keeping up with demand in terms of performance, reliability, ease of monitoring and cost.

5 Trends in Component Technology

Digital avionic processors are able to take advantage of the higher packaging density now available in logic elements with attendant benefits in cost and in the increased reliability which results from the reduction in the number of connections between packages. Typically a processor can be built with only 20–30 m.s.i. components. The store, implemented in semiconductors to obviate the corruptibility of magnetic core stores can be contained in another 20 or so packages; the packing density of storage media is increasing rapidly. On the horizon are l.s.i. processing packages in which the central processor is built of 1–6 modules only.[2] Thus the functions of increased complexity are not necessarily any less reliable (Appendix 1).

The corruptibility of digital data transmission links has been reduced markedly by modern integrated circuit elements of high noise rejection and electrical cables of well controlled design and manufacture. These enable links to be constructed with sufficiently small error rates and high-integrity error detection circuits.

Pulse pick-up and short circuit immunity are offered by optical links, with the promise of superior error-rate performance and bandwidth and, in the long run, no cost increase and an attendant weight saving. The use of fibre optic data links also provides earth loop elimination and complete electrical isolation.[3]

The reliability of systems tends now to hinge on those of the sensors, in particular gyroscopes, and of the primary power systems. Here there are signs that mechanical sensors with wear-out problems may be displaced by 'solid state' devices, of which the vibrating gyro and the laser gyro are two showing promise.[4]

The problems inherent in the sharing of primary power by high-integrity systems and other more power-consuming systems, have led to complex switching and fault location systems.[5] It is probable that special

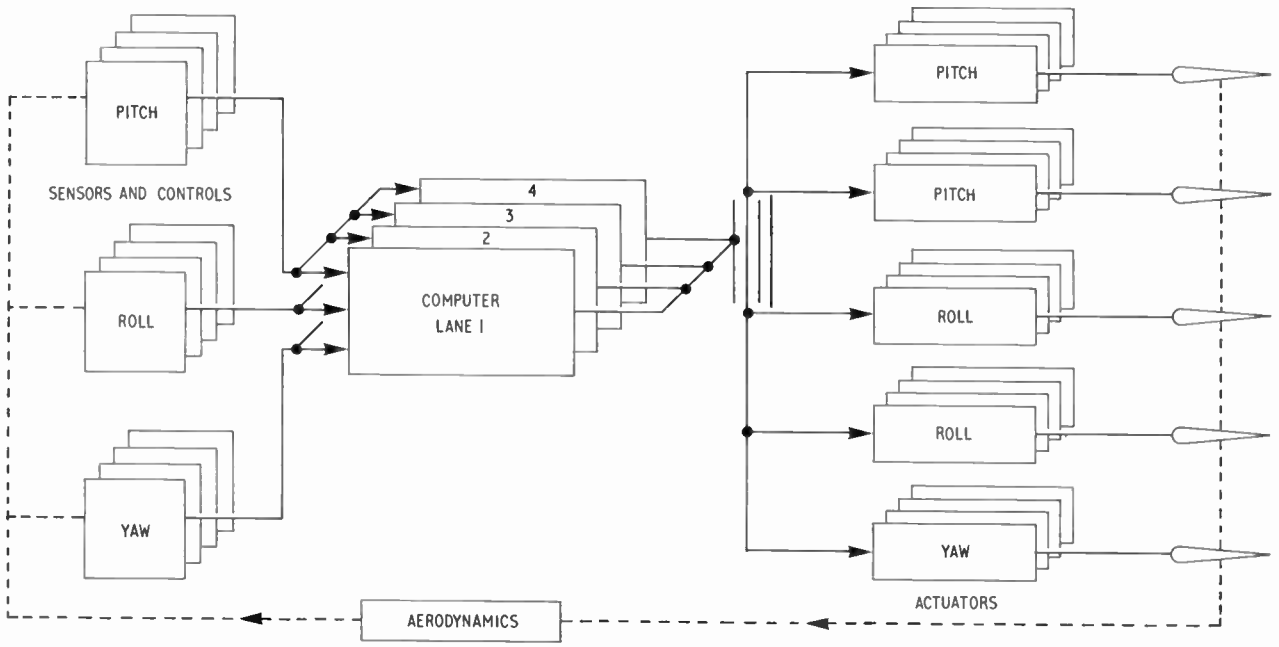

Fig. 3. Schematic layout of a high-integrity control system.

solutions will be developed to ensure failure-free systems for critical avionic requirements, in particular 'fly-by-wire' flight control where even a temporary loss of power can result in sudden catastrophe.

6 Typical Current Configurations in High-Integrity Digital Systems

Figure 3 illustrates a representative configuration for a high-integrity autostabilizer of adequate integrity for full-time fly-by-wire implementation. It is of quadruplex redundancy throughout. It should be noted that each computing lane handles simultaneously pitch, yaw and roll information. Since there is necessary interaction between the axes, e.g. to perform coordinated turns, there is minimal loss in integrity and significant economy in such a solution.

In Fig. 4 is shown the interconnection of the four computing lanes in greater detail for, say, the pitch channel. The inputs comprise pilot inputs, motion sensors and demands from the automatic pilot. The autopilot may well have redundancy and to a different degree (probably duplex).

To obtain an integrity of the order 10^{-7} per hour any hardware common to all lanes must be a minimum, and any possibility of defects in one lane being transmitted to another (e.g. false data or secondary failures such as loading of a power supply) must be eliminated. To this

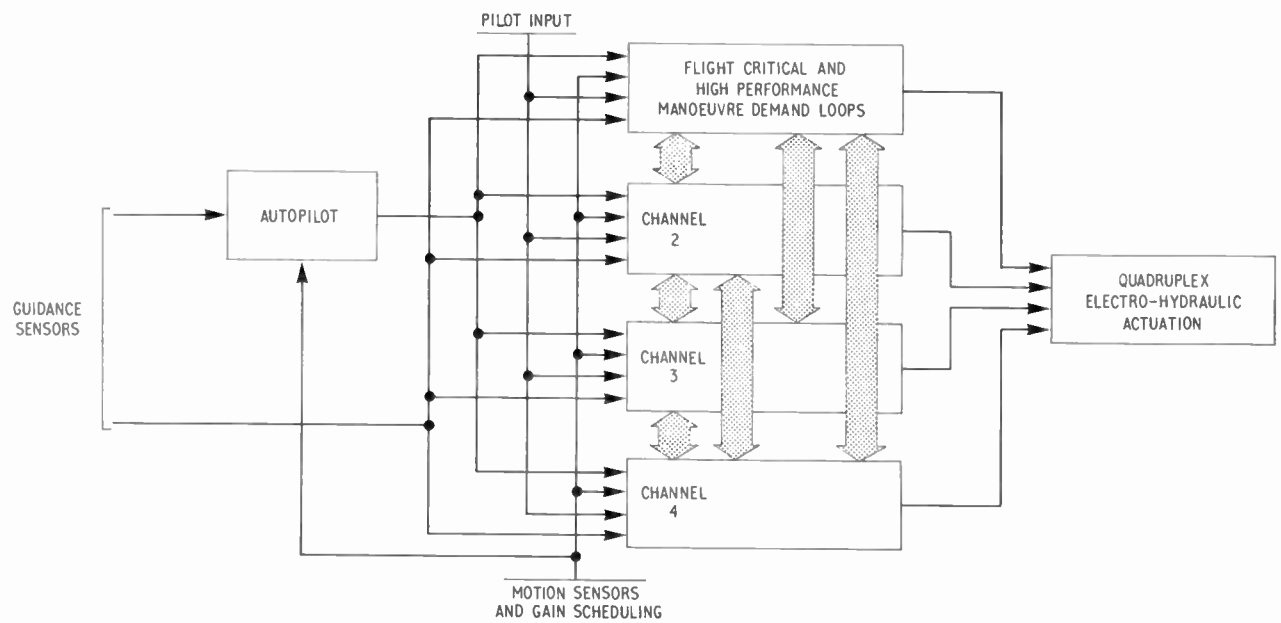

Fig. 4. Digital flight control system schematic. Wide arrows show optical links for interlane data transfer.

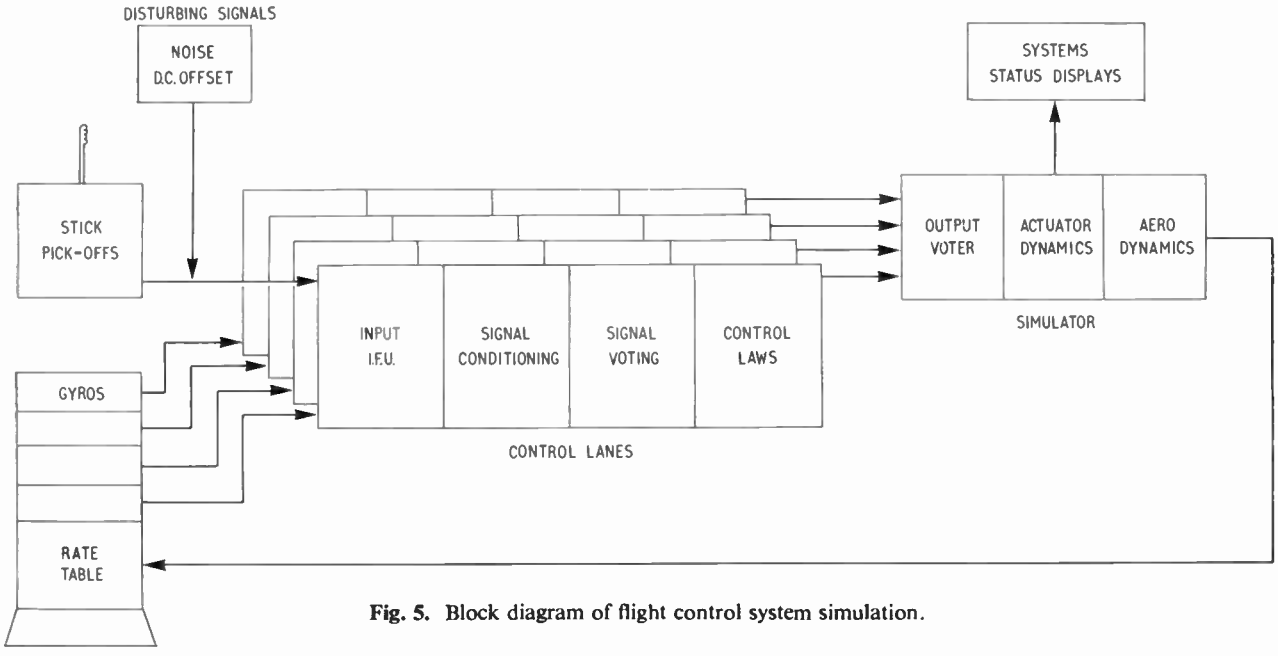

Fig. 5. Block diagram of flight control system simulation.

end intercommunication between lanes is only permitted over fibre optic data links which are short-circuit-proof, fireproof and not subject to transient interference.

Depending on the dynamic performance required from the system it may be necessary to synchronize the computers in each lane to one another to avoid samples of the input data being taken at different instants (differential data staleness). If this facility is required it is carried out over the optical links.

To obtain the advantage of the excellent tracking capability of digital computing lanes it is arranged that, although each sensor of a quadruplex set is connected only to one computing lane, each lane can obtain all sensor inputs by cross transfer over the optical link. This enables each lane to weed out failed sensors and to select, say, a median input as the identical input to be processed. Each computing lane is built around a small task-oriented general-purpose-organized processor carrying identical control algorithms and identical failure-isolation and signal selection logic.

The component parts of a test rig incorporating these facilities are illustrated in Fig. 5. The rig enables failures to be simulated and the aerodynamic-loop to be closed to provide realistic conditions in the system. A current hardware implementation is illustrated in Fig. 6 which is typical of two digital flight control systems now well into development, the Multi-Role Combat Aircraft (*Tornado*) and the Boeing *YC-14* s.t.o.l. transport.

7 Critical Development Areas and Trends Towards the Future

In the author's opinion the areas of development which will form the key to successful implementation in the future are:

The elimination of common failure hazards.

Resolution of the need for dissimilar redundancy.

Cost-effectiveness in service.

7.1 Common Failure Hazards and Dissimilar Redundancy

The practice of redundant systems demands critical attention to aspects of a redundant system which can cause all lanes to fail in a similar manner simultaneously (or strictly between two adjacent instants of cross-monitoring). Such known mechanisms could be:

transient interference

power supply failure

coffee poured over a common circuit area

structural failure

fire or explosion

software errors common to all lanes.

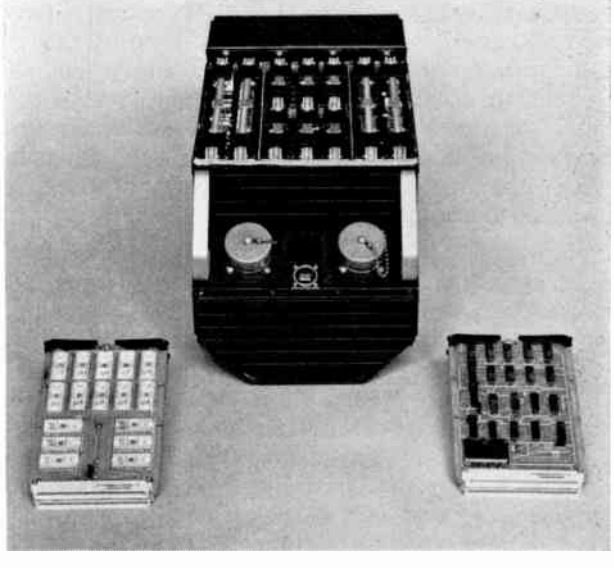

Fig. 6. Typical hardware implementation of a digital flight control system.

Such common failure hazards are to a large extent predictable and can be taken into account during design. It is the unpredicted hazard that is particularly difficult to contain; it is experience, both of those involved in the design process and those responsible for system certification that provides the best defence. All current British systems use mechanical reversion for survival in face of such hazards. The disadvantages of this approach are the cost, weight and structural design limitations and the training problem in teaching pilots how to maintain control on the rare occasions that reversion is needed. Certainly there is a real cost involved and alternatives are perpetually under consideration. What is required is a stand-by system which is sufficiently dissimilar in technology that it can be seen not to be subject to any common failure hazard to which the prime system may be prone. Suggestions have been analogue or fluidic computing, and dissimilar sensors. It is difficult to find a substitute for hydraulic actuation. In the long run a complete dissimilar stand-by system may be found impractical, and an alternative found by implementing dissimilar redundancy piecewise. Examples are to use a mix of electrical and optical data transmission, and a mix of alternator power and batteries.

The development of software to meet the high standards demands disciplines in modularity and testability which have taken some time to develop for the analogue systems which are being superseded.

A critical parallel problem is to select the implementation in such a way that the process of proving and certification can proceed step by step at a fast pace, with the minimum number of flight hours for each step.

7.2 Achieving Cost-effectiveness without Prejudicing Safety

Aside from the common failure hazard problem we can improve failure survival performance by adding more lanes. The drawback is that whereas a lane m.t.b.f. of, say, 1000 hours may be perfectly acceptable on integrity grounds, and 1000 hour servicing (mean) acceptable to maintenance staff, a quadruplex system which requires lane replacement on average every 250 hours may be totally unacceptable. Thus integrity and availability requirements conflict. Even with highly professional quality assurance procedures and system engineering this clash can prove hard to resolve. There are in the author's opinion four routes of action, each of which can contribute to a solution.

Policy One is to improve the piece-part failure rates of the components by thorough screening, testing and process control. The American ICBM programme achieved dramatic improvements by this means but at a cost in R & D and in the final component cost which is likely to yield a poor return if it is attempted to push this procedure further. Certainly the avionics industry itself could not afford to 'go it alone', particularly as it is necessary to test (destructively) millions of identical components to find out whether an improvement has been made. Such considerations daunt designers tempted to use special-grade or custom-built components.

Policy Two is to reduce piece-part failure rates by improving the environment in which the systems work. A working temperature of 90°C (because of dense packaging demanded) with dirty 'cooling' air supplied at 50°C does not make for low failure rates in either electronic or mechanical assemblies. The Airlines Electronic Engineering Committee which exercises a powerful influence on the design of civil avionic systems (and also affects military thinking) has proposed the use of refrigerated protected cabinets to house new airline electronic systems (the Arinc New Installation Concept).

The applicability to small tightly-packed executive jets and military combat aircraft is not clear. The benefits of a reduction from 90°C to 20°C are however significant (conservatively a factor of five for integrated circuits).

Policy Three recognizes that the capability required from an individual function or subsystem within a total avionics system is not constant and that both performance and degree of failure survival depend on role and phase of flight. Given a degree of systems integration and the flexibility of digital processing systems, it is conceivable to construct an assembly or network of processing power which can concentrate its energy into different areas at different times. Such flexibility can make possible new patterns of failure survival and provide a processing and display centre which acts as if it were quadruplex in carrying out some functions and simplex in others. This approach draws a parallel with the use of available manpower and has the property of 'fitting' the crew capability more closely.

The probable mechanization is a form of multiprocessor in which a number of processors each contain the programs for the highest integrity tasks, voting on the input and output data as previously described. Tasks of lower integrity are carried out by only one or a smaller number of processors, and tasks of the lowest integrity accessed from a common source of program instructions by any processor with free time and a failure-free record. The master task-scheduling and failure-isolation programs are of course stored in each processor and cross-compared and voted on before they are obeyed. This permits the construction of a multi-task system with a very high status confidence and graceful degradation properties. In the event of failures tasks of lesser importance may be shed or iteration rates reduced.

Policy Four recognizes the ability of the crew to respond to failure conditions and by improving the man-machine interface provides a greater capability from the man-machine combination. Examples are the use of electronic displays and the contrast between the automatic landing approach in which the crew involvement is minimal (and quite often dangerous if the pilot attempts to 'take over'), and an approach which recognizes and optimizes the part played by the man in the loop.

It is likely that each one of these policies may be applied to systems of the future.

8 Conclusions

Redundant digital avionic systems will be shortly going into service. The flexibility and reliability of modern m.s.i. logic components, the emergence of l.s.i. processor

components and the ability to construct failure survival systems using optical elements will facilitate many new approaches to redundancy management. Its success will depend on new disciplines in safe system design, which are developing fast to keep pace with the demand.

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10 Appendix: Reliability of Microcircuit Computers in the Field

Direct comparisons of different technologies are difficult and field experience of the most modern components is inadequate. However, the experience obtained for an airborne computer in service in a military environment is indicated below. The equipment is the control computer for the A-7 head-up display of which over 1000 units have been delivered and which uses DTμL components.

Before components boards are assembled the components are 'burned-in' by operating at full rating for 150 hours and failed components eliminated. Completed units are then 'burned-in' by operating in the simulated environment and failed components replaced. The improvement in infant mortality effects in the field is indicated by the failure statistics as follows:

A-7—DTμL Failure Rates

Component Burn-in	
No. of devices screened	47 689
Device burn-in time	150 h
No. of device hours	47 689 × 150 = 7 153 350 h
No. of rejected devices	1671
Failure rate	233·6 parts/10^6/h
Unit Burn-in	
No. of devices per unit	765
No. of unit hours	17 230 h
No. of device hours	17 230 × 765 = 13 180 950 h
No. of device failures	161
Failure rate	12·2 parts/10^6/h
Operational Experience	
No. of operational systems	454
No. of devices per system	765
No. of operational devices	765 × 454 = 347 310
No. of operational hours per year/system	527
No. of operational device hours per year	527 × 347 310= 1·8 303 237 × 10^8h
No. of primary failures due to DTμL devices recorded in one year	50
Failure rate	0·273 parts/10^6/h

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An improved voltage variable resistor m.o.s.t.

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and

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SUMMARY

A method of designing enhancement-mode m.o.s.t.s having controllable turn-on characteristics is described. The m.o.s.t.s are specifically aimed at performing the functions of voltage-controlled resistors and the design called for a log-linear variation in channel resistance with gate voltage over as wide a range as possible. The devices were made using a conventional p-channel oxide gate process with an additional n^+ diffusion stage to give the required variation of threshold voltage at different points within the device. In the final form of the m.o.s.t. the log-linear range of channel resistance variation extended from 5MΩ to 500Ω for an applied gate voltage range 4–15 V. The design method used for these devices could equally well be applied to making composite m.o.s.t.s having another form of channel resistance variation from the log-linear variation studied here.

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1 Introduction

It is a property of conventional enhancement mode m.o.s.t.s that they switch rapidly from a high to a low impedance state when gate voltage is applied. In previous papers[1, 2] an m.o.s.t. has been proposed and demonstrated that has a more controllable channel resistance vs. gate voltage characteristic. In this device control is achieved by a gradual turning on of the channel current as the gate voltage is increased. The present contribution extends the earlier work and gives the results obtained from three designs of variable resistance f.e.t. The devices all use the principle that placing a number of f.e.t.s in parallel, each f.e.t. having a different channel aspect ratio ($W/_L$) and threshold voltage (V_{th}), allows one to construct a composite device having almost any desired channel resistance characteristic.

There is of course little difficulty in making m.o.s.t.s having different aspect ratios but the incorporation on a single clip of devices having different threshold voltages is more difficult. One approach to this problem is to use a tapped resistance chain and to feed the gates of succeeding devices from tapping points on the chain.[3] This method suffers the major drawback that the input is shorted by a low value resistor chain, this is particularly the case if the resistors are formed by diffusion at the same time as the source and drain. In the present work the variation in V_T is achieved by changing the surface doping concentration of the substrate using lateral diffusion of phosphorus under an oxide mask to give regions in the silicon slice where m.o.s.t.s having different threshold voltages may be formed.

For the purpose of computation and design the composite m.o.s.t. can effectively be considered to consist of a large number of elemental devices each having a different value of $W/_L$ and V_{th}. When operated with a common source and drain so that the channels are all connected in parallel, the resulting channel resistance characteristic will be determined by the sum of the contributions of the individual devices. Using this approach and considering the channel to have a large number of elements it should be possible to achieve control over a wide range of channel resistance variation with applied voltage and to make the variation follow some prescribed law. In the present work the device aimed at was to have a log-linear variation of channel resistance with gate voltage over as wide a range of channel resistance as possible. Devices of this type would have application as voltage-controlled resistors, in phase-shifting networks, voltage-controlled attenuators, voltage-controlled variable-frequency-oscillators, filters, etc.[4]

2 Device Design Considerations

Considering the device figuration of Fig. 1 it can be inferred that the threshold voltages of the elemental devices will vary along the width of the device because of the impurity gradient at right angles to the flow of current caused by lateral diffusion from the additional n^+ diffused sources. The channel elements nearest to the n^+ source will have the highest values of V_{th} and those remotest from it will have a value of V_{th} determined

The Radio and Electronic Engineer, Vol. 46, No. 7, pp. 350-354, July 1976

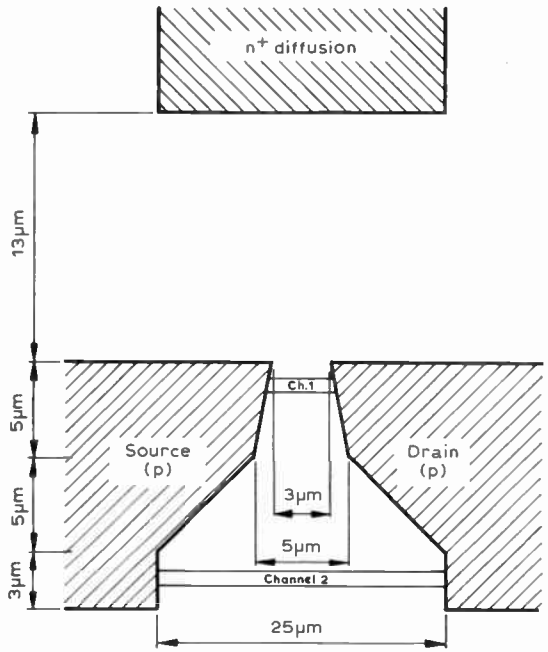


Fig. 1. Schematic diagram showing layout of a variable resistance m.o.s.t. Two of the elemental channels having widely differing values of W/L and V_{th} are indicated. The gate electrode has been omitted to simplify the diagram.

by the initial doping level of the silicon wafer. V_{th} may be estimated from the usual relation so that V_{th} is proportional to the gate oxide thickness (τ_{ox}) and proportional to $N^{\frac{1}{4}}$ where N is the substrate doping level. The channel conductance (G) for low values of drain voltage can be written as:

$$G = \mu_p \frac{\varepsilon_{ox}}{\tau_{ox}} \frac{W}{L} (V_G - V_{th})$$

from which a linear variation for G with V_G can be predicted. This relationship will only hold for gate voltages within a few volts of V_{th} because above this there is a departure from linearity caused largely by the fall off in the channel mobility (μ_p).

In order to design devices having a log-linear variation of $R(=1/G)$ with V_G it was obviously vital to establish for the m.o.s. process to be used the variation of V_{th} with N, and of μ_p with both V_G and N before attempting to fabricate composite devices. To do this a number of simple block devices having channel aspect ratios $W/L = 6$ were processed for a range of surface doping levels achieved by depositing and then driving in phosphorus to the substrate surface. Table 1 gives typical measured values of V_{th} and μ_p obtained for low values of $V_G - V_{th}$. Figure 2 shows the calculated and measured values of V_{th} plotted as a function of the surface impurity concentration N. In practice V_{th} varied about the mean value on a slice by ± 2 V.

Considering the mobility variation, from Table 1 it may be seen to be a function of N as well as $V_G - V_{th}$. As N rises the mobility falls. It is necessary to estimate this variation of mobility in order to make meaningful calculations of the device geometry and the impurity profile required to give a specified resistance characteristic. This was done by considering more closely the variable resistance device incorporating a built-in doping gradient described in a previous paper (Fig. 3).[2] Further devices of this type were processed and their characteris-

Table 1

Mobility and threshold voltage measurements for different channel doping levels

Slice number	Deposition temperature (°C)	Drive-in time (hours)	Average V_{th} (V)	Variation of mobility μ_p (cm²/V-s)	Average mobility (cm²/V-s)
1	800	24	10·0	135–106	120·5
2	800	12	13·0	132–103	117·5
3	810	24	28·0	130–100	115
4	810	12	31·0	130– 98	114
5	820	24	40·0	125– 85	105
6	820	12	43·0	120– 75	98

Phosphorus deposition time: ½ hour.
Drive-in temperature 1200°C. $\tau_{ox} = 1250$ Å.

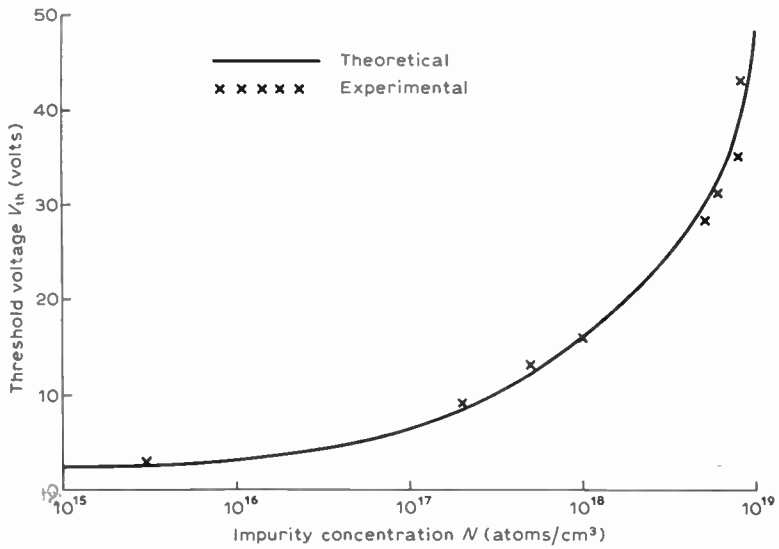


Fig. 2.
Measured threshold voltage as a function of surface impurity concentration for gate oxide 1250 Å thick.

tics measured. These were then compared with computed curves using a program that considered the channel to consist of 100 parallel elements, and which allowed various assumptions to be made regarding the mobility variation. At low gate voltages the mobility is determined by the region of the device having the lowest channel doping, this will be similar to that found in a conventional p-channel m.o.s.t. As V_G increases the regions of the device having shorter channels and higher channel dopings start to conduct until at large values of V_G the entire channel is conducting. For the last parts of the channel to conduct, the mobility will be determined by the highest channel doping, which could be estimated knowing the surface carrier concentration. By a process of successive approximation and curve fitting a variation of mobility with voltage was arrived at for voltages between the onset of conduction of the device and the final section of channel switching on that gave good agreement between the measured and calculated resistance characteristic over the entire range of applied voltage (Fig. 3).

3 Improved Device Geometries

Using this empirically derived mobility variation in the computer program that gave the resistance characteristic of a composite device, a new geometry having a more linear resistance characteristic was found. The revised geometry is shown in Fig. 4, where it differs from that of Fig. 3 in that the n^+ diffusion to create the channel impurity gradient is in the centre of the device, thereby making the device more compact and also allowing the n^+ deposition temperature and the subsequent drive in time to be reduced. The characteristics

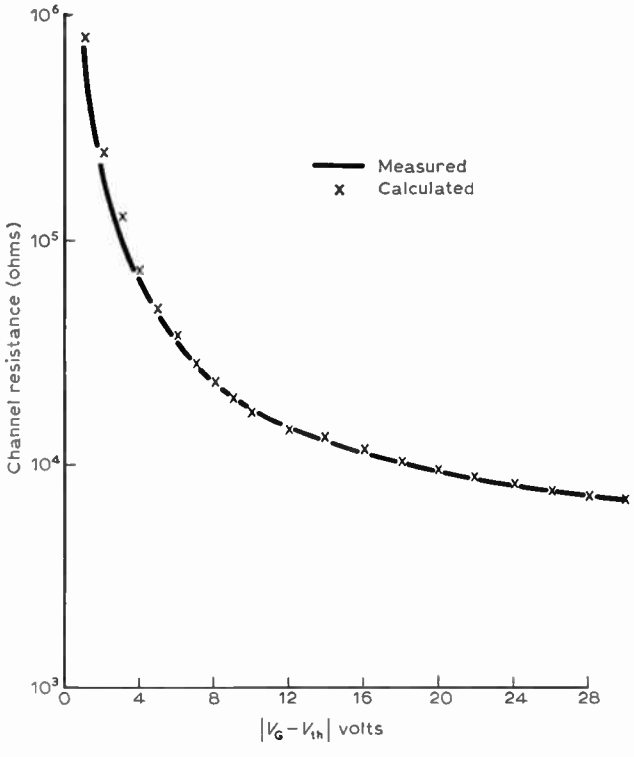
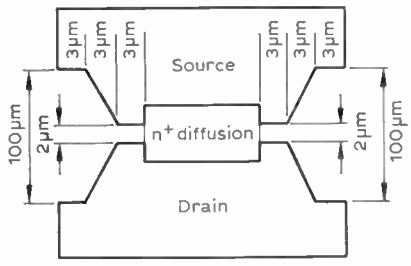
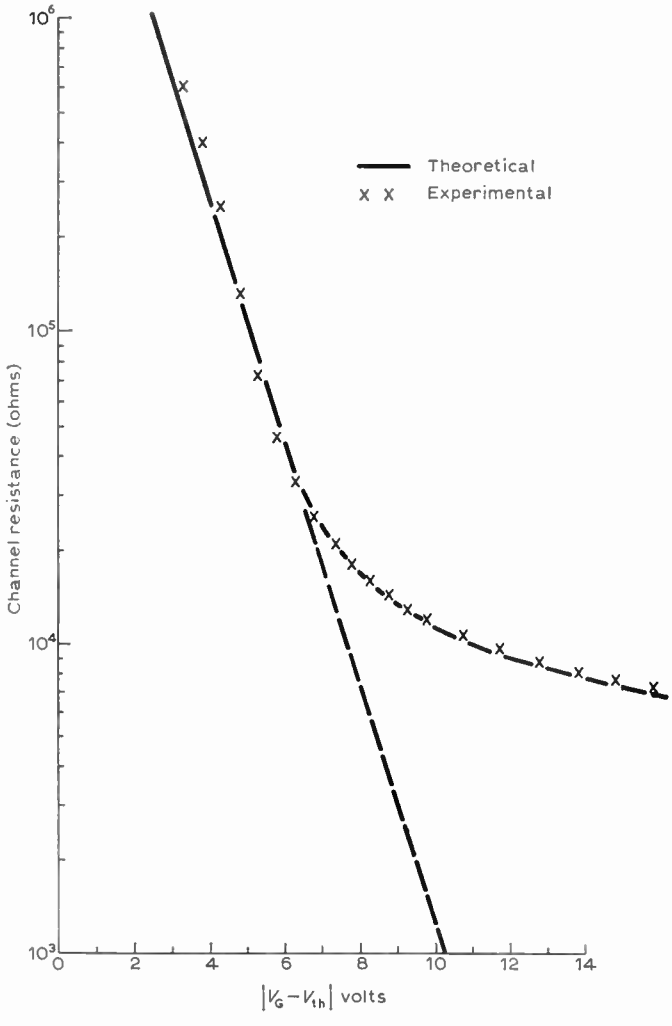


Fig. 3. Computed and measured channel resistance characteristic for device shown in Fig. 1.



(a) Device geometry

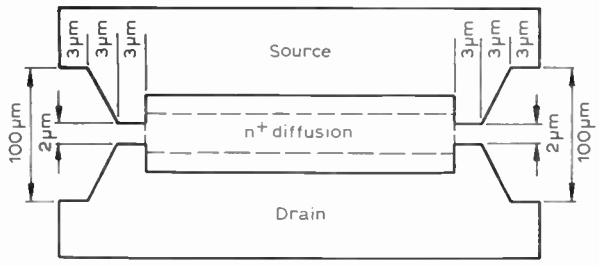


(b) Channel resistance characteristic.

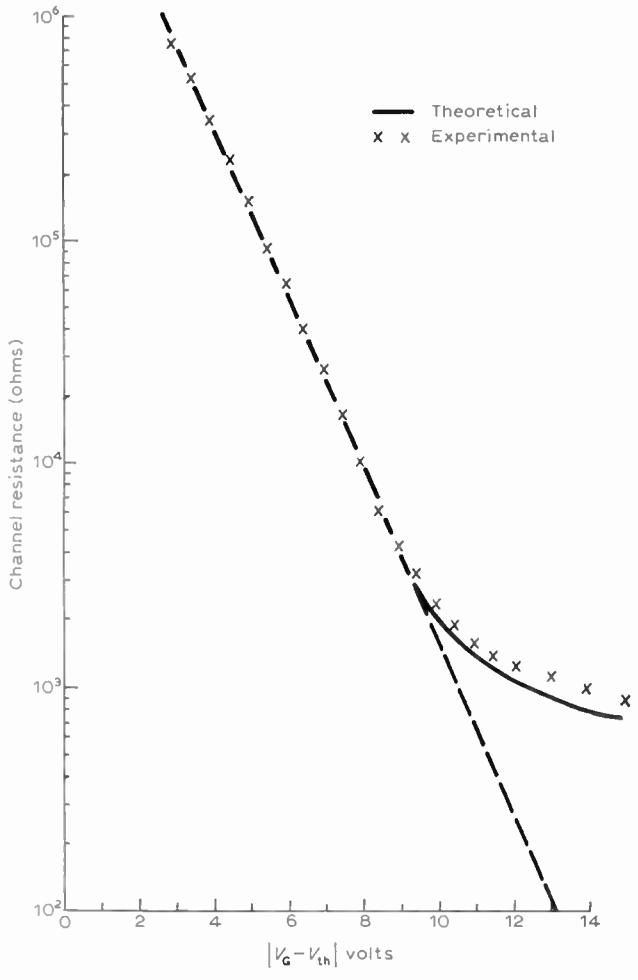
Fig. 4.

obtained show that there is a log-linear range of channel resistance variation extending for nearly two decades of R and good agreement between the predicted and measured form of the variation over the entire range.

The result of Fig. 4 supported the assumed mobility variation, so ways were sought of further extending the log-linear region of the characteristics to lower values of channel resistance. This was achieved by adding a further block device in parallel with the design just considered. This was simply done by forming the additional device within the n^+ diffused region of the sub-



(a) Device geometry, block device $W/L = 1/30$



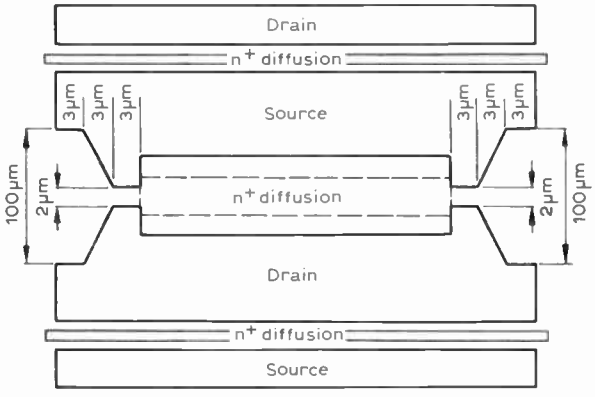
(b) Channel resistance characteristic.

Fig. 5.

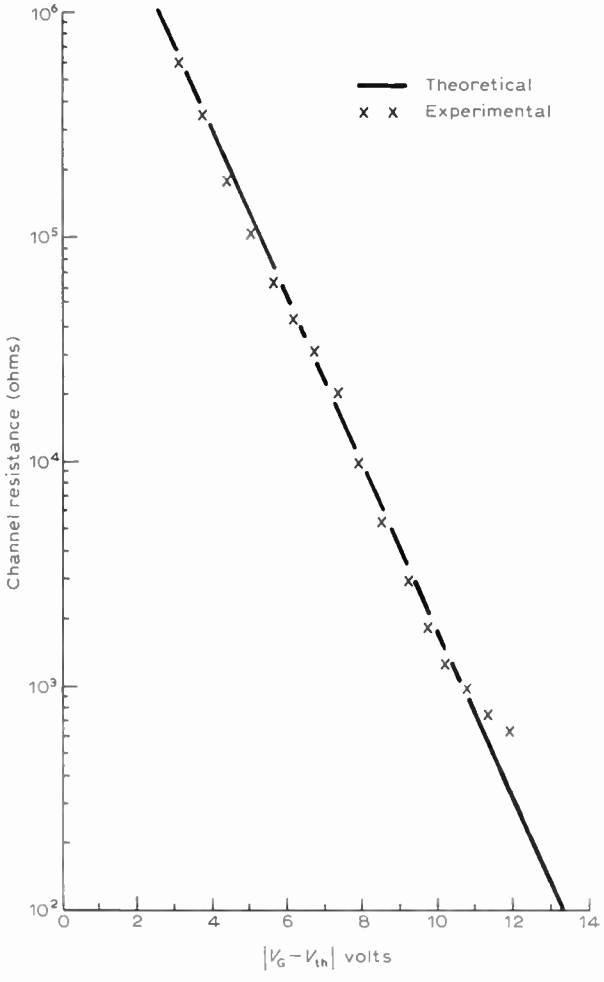
strate, the additional device turning on immediately after the last element of the laterally diffused device. Using the same computer program as an aid an optimum device geometry was arrived at for an f.e.t. having a log-linear channel resistance range from 3 kΩ – 5 MΩ. The mobility values assumed in the computation for different parts of the device were the same as those used previously.

Figure 5 shows the geometry of the f.e.t. together with the measured and calculated characteristics. Again good agreement between experiment and theory was found, giving further confidence to the design process used. It should be noted that this improved characteristic was achieved without any change in the processing stages, only the photolithographic masks were modified.

As a final exercise to check on the design method and in an effort to further reduce the channel resistance at high values of V_G two further parallel elements were



(a) Device geometry, centre block device $W/L = 1/30$, end block device $W/L = 1/60$



(b) Channel resistance characteristic.

Fig. 6.

added to the f.e.t. Since these elements required still higher values of V_{th} they again had channels formed within heavily doped n^+ regions but in addition had an extra thick gate oxide, 1·7 μm against 1·2 μm for the other channels. This of course necessitated a further masking and oxidation stage as in practice the gate oxide for the high V_{th} m.o.s.t.s was grown for twice the usual period.

The specification for the final device called for a range of log-linear resistance variation from 500 Ω–5 MΩ for a range of gate voltage of 4–15 V. The computed geometry of the composite f.e.t. together with the measured and calculated characteristics are shown in Fig. 6. Again there is good agreement between the two curves—the undulation in the curves is due to the fact that basically one is adding together the characteristics of a number of discrete devices operating in parallel. The purpose of the design exercise is to give as long a range of log-linear variation as possible within a specified tolerance, ±5% in this case. A longer range could be achieved if the tolerance were relaxed to allow greater undulations on the curve about the ideal straight line.

The designs of the devices of Figs. 4, 5 and 6 were ultimately all incorporated into a single chip together with a number of test devices for assessing mobility, the threshold voltages of different sections of the composite devices, sheet resistivities, etc. The characteristics given here are typical of those measured for a number of slices and chips within a given slice. From the measurements of threshold voltage it was shown that values of V_{th} for devices having undoped channels were ~3·5–4 V and were therefore quite unaffected by the long n^+ drive-in times required to form the higher threshold devices (~ 12–24 hours). Values of V_{th} for the thin oxide m.o.s.t.s with doped channels were typically 9 V whereas the thick oxide m.o.s.t.s had values of V_{th} between 5–12 V, depending whether the channel was doped or not.

The characteristics shown in Figs. 4(b), 5(b) and 6(b) were typical of those measured for devices in which the values of V_{th} for the different sections of the channel were within ±0·5 V, and the channel lengths L were within ±0·5 μm of the specified values. For these devices, about 50% of all working devices, the spread of channel resistance characteristics from device to device and batch to batch was ~ ±20%. Larger variations in V_{th}, or more particularly in L, gave rise to a very much larger variation in the characteristics. Under these conditions complete sections of the channel may well not conduct at all.

Typical values of V_{th} for the test f.e.t.s were measured together with the two thicknesses of gate oxide present on each chip. The ratios of the values of V_{th} and τ_{ox} were compared for a number of slices and shown to give excellent agreement for both doped and undoped channels.

4 Conclusions

It was concluded from this work that good control over the device parameters could be achieved even for a complex multichannel f.e.t. It would appear therefore quite feasible to use a computer program similar to the one developed for this investigation to design variable resistance f.e.t.s having predictable channel resistance characteristics.

It should be noted that no attempt was made during the processing of these devices to stabilize the gate oxides and no measurements were made on device stability. All the channel resistance measurements were made at 1 kHz. Obviously the device geometries could be optimized to reduce the input capacitance and capacitances associated with the junctions. In the case of the device shown in Fig. 6 the input capacitance was ~ 10 pF. This could probably be reduced by at least an order of magnitude if a self-aligned gate process was used together with a revised geometry.

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The floating point unit of the *Golem B* computer

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SUMMARY

The *Golem B* computer is a fast machine using emitter-coupled logic and multi-layer circuits. The autonomous floating point arithmetic unit obtains its instructions and operands from buffers loaded ahead of need. Its main part, for 56-bit fractions, uses two 4-operand adder complexes with stored carries.

In multiplication instructions, 4 bits of the multiplier are used to form a new partial product in each pass through an adder complex. Division instructions use a base-4 non-restoring algorithm. Addition favours the case of equal or nearly equal exponents, but 112 sum bits are accumulated for all exponent differences.

An effort has been made to provide instructions and number formats that will aid the writing of compilers and operating systems.

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1 Introduction

The *Golem B* computer has been completed recently. The general systems organization has been described elsewhere,[1] and this paper is concerned only with the floating-point arithmetic unit. However, some remarks are in order to describe the place of this unit in the system.

Roughly speaking the computer consists of three autonomous machines, a fixed-point and look-ahead unit, an input–output unit and a floating-point unit. All the memory communications are under the control of the look-ahead unit. This unit fetches all instructions in a program stream from memory and sends those intended for the floating-point unit to the two floating-point instruction buffers. The fixed point and look-ahead unit computes the effective address of floating-point operands, fetches such operands and deposits them in two floating-point input buffers, for later use by the floating-point unit. The look-ahead unit also computes the effective destination of words to be stored. The floating-point unit leaves such words in the output buffer for later disposal by the look-ahead unit.

An effort has been made to balance all components of the system, including core memory, in such a way that the speed of scientific computations is only limited by the speed of the floating-point unit itself. Instructions and operands are supplied to this unit at a rate large enough to prevent this unit from ever standing idle.

MECL III integrated circuits are used both in the floating-point and in the fixed-point and look-ahead unit. These integrated circuits are mounted on multi-layer printed circuit daughter cards (up to 40 packages per card) which are plugged into multi-layer printed circuit mother boards (up to 80 daughter cards per mother board). Communication between mother boards is by means of 50 ohm flat cables.

Although speed is the main objective, it was decided, in the interest of economy, not to have multiple and specialized floating-point arithmetic units, but to execute all floating-point instructions in one single processor.

2 Word Formats

Three word formats are used by floating-point instructions, and they are shown in Fig. 1.

Data in long word lengths consist of

(a) One sign bit for the fraction.

(b) Seven exponent bits, for a base 16 exponent in the range -64 to $+63$.

(c) 56 fraction bits.

Negative fractions are represented by their two's complement. Negative exponents are represented by their complement with respect to 128.

Data in short word lengths have the same fraction sign and exponent bits, but only 24 fraction bits.

In the third format, the operand is a 32-bit signed integer. This operand is loaded into 32 high-order bits of the floating-point arithmetic unit. The fraction sign is made equal to the sign bit of the fixed-point operand.

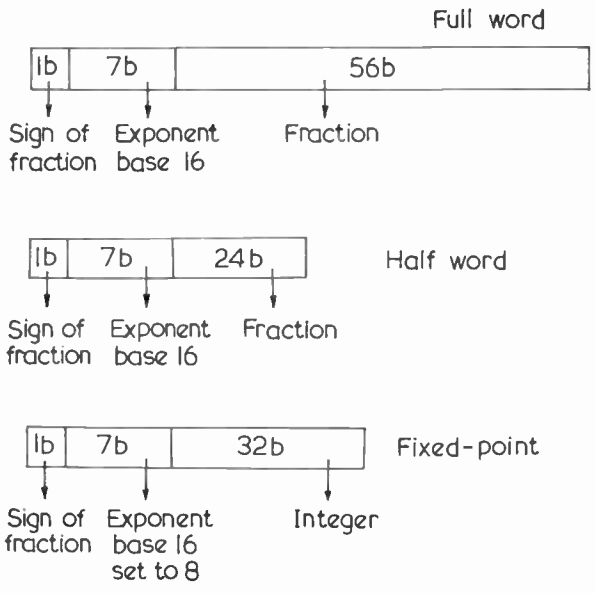

Fig. 1. Floating-point arithmetic word formats.

(Thus, the sign bit of the fixed-point operand goes to two places in the floating-point arithmetic unit. One of these is the fraction sign position, the other is the highest significance position of the fraction.) At the same time, the exponent is set to the value of +8. An integer is thus converted to a floating-point number, and can be handled as such by the floating-point unit.

Conversely, a floating-point number is stored as a 32-bit integer by

(1) shifting the fraction right or left and decrementing or incrementing the exponent by 1 for each 4-bit shift until the exponent equals +8,

(2) truncating the fraction to 32 bits and shipping only those to the output buffer.

Checks and alarms for overflow of course are provided in this operation.

This format simplifies conversions from fixed-point to floating-point format and vice versa, and implementation of computations involving a mixture of integers and real numbers.

3 Block Diagrams

Figure 2 shows the main floating-point arithmetic unit which handles the fractional parts of floating-point numbers. This arrangement of registers and adders derives from *Illiac II*,[2] via *Golem A*.

The three registers M, A and S are capable of holding 56-bit fractions and their signs. Registers Q and R hold 56-bit fractions. Register M accepts the incoming operand from the input buffers. This will be the multiplicand in multiplication, the divisor in division and the addend/subtrahend in floating-point addition/subtraction (called addition for short in the rest of this paper). Registers A and Q together form a 112-bit wide accumulator. Before a multiplication, AQ holds the multiplier; after multiplication the product. Before division, AQ holds the dividend; after division the quotient. Before addition, AQ holds the augend; after addition the sum.

Registers S and R are temporary storage platforms and will not be addressed by the programmer, except after division, when the remainder is available in R. (A load R instruction is also provided.) Operands returned to storage pass the R register on their way to the output buffer. Registers A and S hold numbers in stored carry representation, a stored carry flipflop being provided in all even numbered columns.

Two adder complexes are provided: the A-adder and the S-adder. Each complex consists essentially of two cascaded carry-save adders and is capable, in one pass, of summing 4 operands. The first two operands are the contents of the A-register (or the S-register) and its stored carries. The other two operands are selected multiples of m, the number in the M-register. Each of the two selectors shown in Fig. 2 contains storage platforms for two such multiples. The multiples available

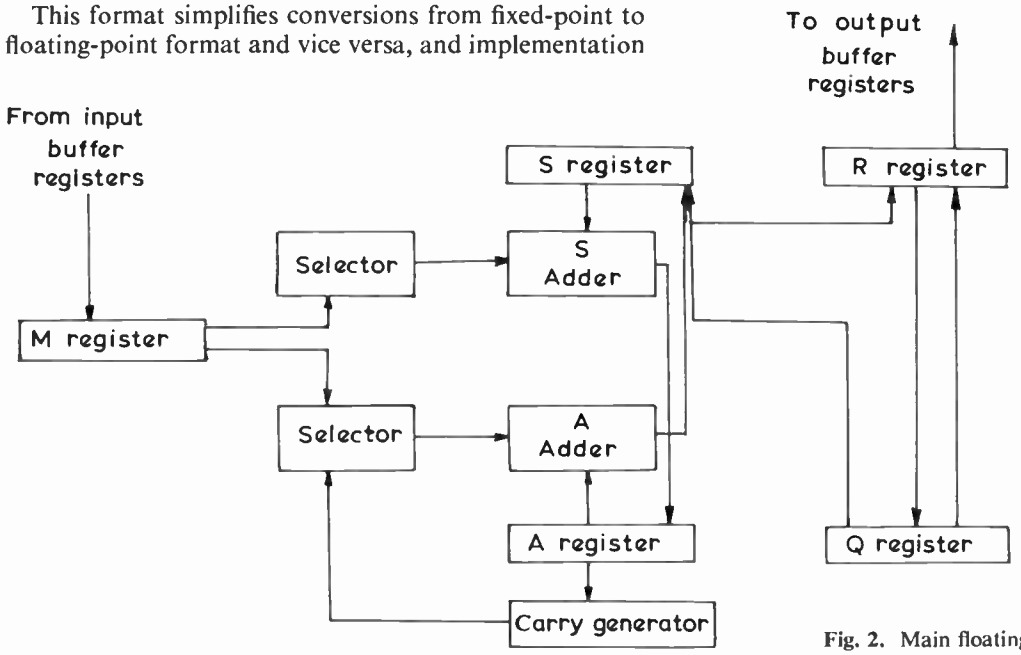

Fig. 2. Main floating-point arithmetic unit.

are:

$$m, 2m, 4m, 8m, -m, -4m, -8m$$

Finally, the box labelled 'carry generator' serves, together with the A-adder, for the assimilation of stored carries when required.

The following shift paths are provided:

(a) From the A-adder into the R-register; 4 bits right into the S-register; 4 bits left into the S-register.

(b) From the Q-register into the S-register; 4 bits right into the R-register; 4 bits left into the R-register.

(c) From the S-adder into the A-register; 4 bits right into the A-register; 4 bits left into the A-register.

(d) From the R-register into the Q-register; 4 bits right into the Q-register; 4 bits left into the Q-register.

Figure 3 shows a block diagram of the exponent arithmetic unit and the shift counter. Registers E, EA and EM hold 7-bit exponents. Registers CU and CL hold 6- and 7-bit shift numbers, respectively. At the end and beginning of an operation E holds the exponent (to base 16) belonging to the fraction in AQ. Register EM receives the exponent of the incoming operand (fraction in M). The selector can choose either $+em$ or $-em$ for entry into the adder, where em means the contents of register EM. In a load operation, the new exponent is gated into E. In a multiplication, the contents of E go to EA and the sum of the exponents is formed in the adder for gating into E. In division, the contents of E go to EA and the difference of the exponents is formed in the adder for gating into E. Finally, in floating addition, the larger of the two exponents is left in E, but the difference of the two exponents, formed as in division, goes into CL to serve as a shift number. The count network increments the number in CU by 2 on its way to CL. Exponents going into storage pass through register CL on their way to the output buffer.

4 Multiplication

Different multiplication orders are provided and they can handle either 56-bit or 24-bit fractions. The multiplicand is loaded into M initially.

In the first step of the multiplication, the multiplier, in AQ is normalized, rounded and truncated to 56 or 24 fraction bits. (An instruction is available which skips normalization and round-off.) The four least significant bits of the truncated multiplier are decoded to select appropriate multiples of m into the S-adder. The multiplier is transferred to R, and thence to Q, with a 4-bit right shift. At the same time, the first partial product is gated into the A-register.

Seven (in long word lengths) or three (in short word lengths) repetitive steps are then performed, in which the action is as follows:

Four low-order bits of the multiplier, in R, are inspected. An appropriate multiple of the multiplicand is selected from the M-register into the A-adder and added to the partial product accumulated so far. This new partial product is then shifted 4 bits to the right into S, 4 bits moving over into R, and at the same time the multiplier, in Q, is shifted 4 places to the right into R. A similar operation is then performed, with 4 low-order bits in Q decoded and the new partial product gated into A and Q. Thus, 8 bits of the multiplier are used up in each up and down pass.

One up and down pass takes about 60 nanoseconds. Measured multiplication times are 800 ns for long word length operands and 450 ns for short word length operands.

The appropriate multiple of the multiplicand, selected according to the 4 low-order bits of the multiplier, is formed by a multiplier recoding shown in Table 1. Consider first the column headed by Carry In = 0. It will be observed that the multiples from 0 to 10 times of the multiplicand can be formed directly with the binary multiples available. Multiple 11 is treated as 16–5 and similarly for multiples 12, 13, 14 and 15. Thus if 4 multiplier bits inspected are 1011, we add −5 times the multiplicand to the partial product, but set the carry-in flipflop in order to cause addition of 1 to the next

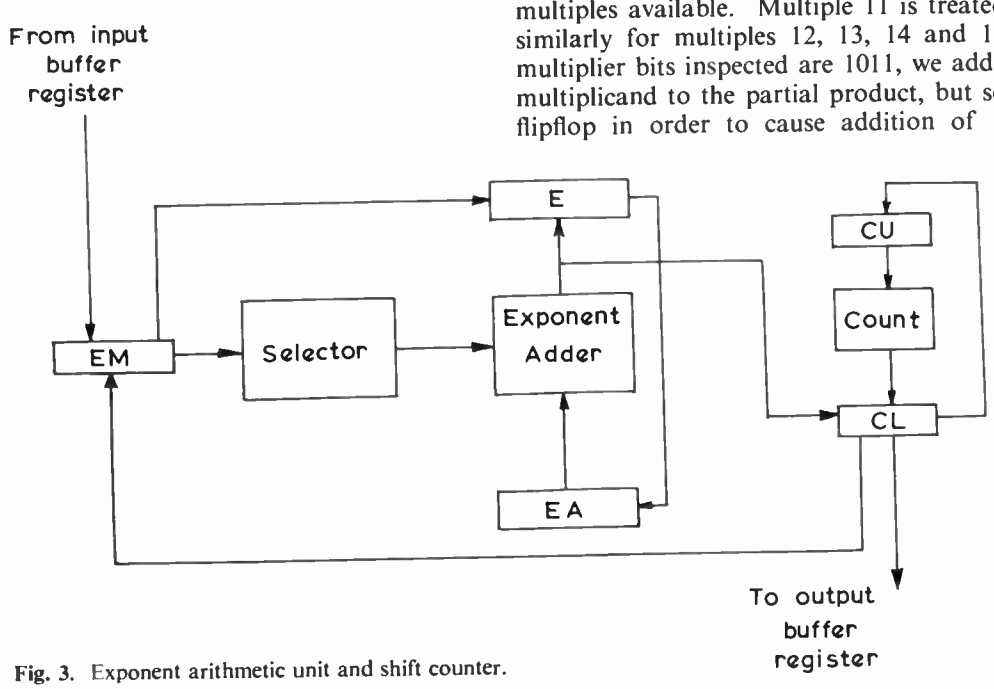

Fig. 3. Exponent arithmetic unit and shift counter.

Table 1. Multiplier recoding

Carry In = 0

4 bits of Multiplier	Choices		Carry Out
0000	0	0	0
0001	M	0	0
0010	2M	0	0
0011	−M	4M	0
0100	0	4M	0
0101	M	4M	0
0110	2M	4M	0
0111	−M	8M	0
1000	0	8M	0
1001	M	8M	0
1010	2M	8M	0
1011	−M	−4M	1
1100	0	−4M	1
1101	M	−4M	1
1110	2M	−4M	1
1111	−M	0	1

Carry In = 1

4 bits of Multiplier	Choices		Carry Out
0000	M	0	0
0001	2M	0	0
0010	−M	4M	0
0011	0	4M	0
0100	M	4M	0
0101	2M	4M	0
0110	−M	8M	0
0111	0	8M	0
1000	M	8M	0
1001	2M	8M	0
1010	−M	−4M	1
1011	0	−4M	1
1100	M	−4M	1
1101	2M	−4M	1
1110	−M	0	1
1111	0	0	1

higher 4-bit group. This will now be decoded according to the column headed by Carry In = 1.

As an example, consider the 8-bit string

1001 1011 i.e. 155

For the lower 4-bit group, multiples −M and −4M are chosen; for the higher group 2M and 8M are chosen. Therefore, including the effect of the 4-bit right shift between the two choices, the multiple of M added to the partial product is

$$(2+8)16+(-1-4) = 155.$$

5 Division

Division uses a base 4 non-restoring algorithm. Four quotient bits are generated in each up and down pass.

During the first part of a repetitive step, the partial remainder is in AQ. Depending on the signs of the divisor (in M) and the partial remainder and on their relative magnitudes one of the following multiples of the divisor is chosen and added to the partial remainder:

$$-3m,\ -2m,\ -m,\ 0,\ m,\ 2m,\ 3m.$$

The choice is always such as to decrease the absolute magnitude of the partial remainder. For each such addition the choice of multiple implies two quotient bits. The new partial remainder is then gated into SR with a 4-bit left shift.

During the second part of a repetitive step a number equal to four times the new partial remainder is in SQ. Multiples selected and added are

$$-12m,\ -8m,\ -4m,\ 0,\ 4m,\ 8m,\ 12m.$$

Each choice implies another two quotient bits.

All these multiples of the M-register are conveniently available in the 4-input adder complex described. Use of all the multiples permits simplification of the decision rules.[3]

Floating-point division, in long precision, can take up to 16 up and down passes. Average times are 3000 ns for long word length and 2000 ns for short word length division.

Integer division has not been implemented in many computers, though an integer quotient is required in many programs, especially those compiled from high-level languages. In many cases the operands involved are relatively small numbers, and an appreciable saving of time may result if the division process is terminated as soon as the integer part of the quotient has been determined. In *Golem B*, the number of up and down passes required is computed in the integer division instructions, in the following way:

(a) Let the normalized divident be $a.16^{ea}$, the normalized divisor $m.16^{em}$. Then the exponent of the quotient is 14 for long precision numbers, and 6 for short precision numbers. The exponent of the remainder is em, which is the exponent of the normalized divisor, except in the case where the

quotient is zero and the dividend, fraction and exponent, becomes the remainder.

(b) The number of quotient bits to be computed is $4(ea-em+1)$, so that the number of passes is $ea-em+1$. This number is counted down in the repetitive loop.

Table 2 gives an example of the results of integer division. Note that floating-point division of 20/3 would yield a quotient of 6·66...67 with a remainder of −0·00...01.

Table 2. Integer division

$\frac{20}{3}=6,$	$R=+2$
$\frac{-20}{3}=-6,$	$R=-2$
$\frac{20}{-3}=-6,$	$R=+2$
$\frac{-20}{-3}=6,$	$R=-2$

6 Floating Addition

The basic process in floating addition or subtraction is to form the difference between two exponents, to shift the operand having the smaller exponent to the right by a number of places equal to this difference, and then to add (or subtract) two fractions. One of the ways of doing the shifting is to have a universal shift network, which can shift an operand by an arbitrary number of places, up to the full width of the accumulator, in one pass through the network. If we wish to accumulate fractions 112 bits wide, which is very desirable,[4] we require

(a) a shift network 112 bits wide,

(b) an adder network 112 bits wide.

An arrangement of this type may be preferred in a specialized floating-add unit but has at least two disadvantages for *Golem B*:

(a) The wide shifter and adder are unnecessarily expensive for shifts by a large number of places, which are rare.

(b) Passage through the shift unit leads to a loss of time in cases where the exponents are almost equal. These cases are very frequent. (According to Sweeney,[5] 73% of all cases of floating-addition, with base 16 exponents, involve an exponent difference in the range ±1.)

A universal shifter is therefore not provided in the *Golem B* floating-point unit. The scheme adopted favours the case with exponent differences of −2, −1, 0 and +1. This case is completed in one up and down pass through the arithmetic unit and takes 270 ns. Other exponent differences are sorted into a number of different cases and handled accordingly. For each case, shifts are minimized by using full register transfers wherever advantageous. In all cases, 112 significant fraction bits are preserved.

7 Other Instructions

Addition, subtraction, multiplication and division, plus loads and stores, are the basic instructions essential in a floating-point arithmetic unit. A large number of variations of these basic instructions as well as additional ones are available, but a detailed discussion of all of them would take us too far. Some mention of the more important groups may, however, be helpful. These are: Replace Add, Exchange and Store Double.

7.1 Replace Add

This is an add, followed by a store, the operand fetch and store addresses being identical. The instruction provides not only a convenience and a saving in program space, but is of some special importance to the writers of operating systems, due to the fact that a machine interrupt cannot take place between the add and the store.

7.2 Exchange

The contents of the accumulator and a specified memory cell are interchanged in one instruction.

7.3 Store Double

These instructions facilitate double precision operations. In the most important version, the sign and the 56 higher bits of the number in AQ are sent to storage. Then the lower bits, in Q, are transferred to A, and Q is cleared. The lower part can now be stored by an ordinary store order. It is given a sign and an appropriate exponent, such that the original double precision number in AQ can be reconstituted by a load and add sequence.

8 Acknowledgments

I wish to thank all my friends and colleagues who worked on various parts of the *Golem B* project without losing patience, in particular, C. L. Pekeris, S. Ruhman, M. Melman, T. Lamdan, A. Caspi, G. Rosenfeld, O. Smikt and A. Ramon. I wish to thank Z. Lapidot, R. de Roos and T. Raisky who worked with me on the floating-point unit. I also wish to thank all the programmers whose opinions helped to settle the final order code, especially W. Silverman, R. Perlman, M. Natanael and Y. Accad.

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Accurate analytical determination of quasi-static microstrip line parameters

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SUMMARY

In the design of microstrip components, the analytical equations of Wheeler have an advantage in handling-speed and simplicity over alternative quasi-static analyses involving complex computation by numerical methods. Wheeler equations can produce excessive errors, however, unless care is taken particularly in the choice of changeover point between equations for narrow or wide strips. This paper shows that for alumina-type substrates with $8 < \varepsilon_r < 12$, the Wheeler analysis and synthesis equations produce results within 1% of those given by selected numerical methods, when the changeover points are correctly chosen. Additional new and modified formulae are presented for the direct calculation of microstrip effective permittivity from either W/h or Z_0, also to an absolute accuracy of less than 1%. These complete an accurate set of analytical equations for quasi-static analysis or synthesis of microstrip lines.

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1 Introduction

Most theoretical work on microstrip line parameters has necessarily concentrated on the analysis approach, that is, the determination of the characteristic impedance Z_0 of a line of given width W, on a substrate of thickness h having a relative permittivity ε_r. If the substrate relative permittivity is unity, then the characteristic impedance is denoted by Z_{01}. The phase velocity v of the propagating quasi-TEM mode is then given by $v = (Z_0/Z_{01})c$, c being the wave velocity in free space. It is customary to define an effective microstrip permittivity which in the low-frequency limit is ε_{e0}, such that

$$\varepsilon_{e0} = \left(\frac{Z_{01}}{Z_0}\right)^2 = \left(\frac{c}{v}\right)^2$$

Clearly ε_{e0} differs from ε_r, and is a function of both ε_r and W/h. The parameters Z_0 and ε_{e0} alone are required to describe the quasi-static behaviour of a microstrip line with given W/h, and the methods of analysis endeavour to calculate them.

The designer of microstrip line components requires a different approach, however. The specified design data comprise sets of characteristic impedances and line length normalized to wavelength, l/λ_g, for the various parts of the complete circuit. The problem is now one of synthesis for which W/h must be calculated for each Z_0 value, and ε_{e0} found as a function of ε_r and Z_0. The microstrip wavelength λ_g is obtained from $\varepsilon_{e0} = (\lambda_0/\lambda_g)^2$, where λ_0 is the free-space wavelength. It is possible to synthesize indirectly by lengthy computational interpolation[1] or by relatively inaccurate graphical interpolation,[2] but direct synthesis using simple but accurate formulae is clearly preferable.

Apart from the fundamental difficulty in establishing ε_r for a given substrate, referred to again below, current thin-film technology and microstrip measurement techniques are good enough to justify a requirement for errors of under $\pm 1\%$ in the calculation of microstrip parameters. Although this can be achieved by analysis using complex computer programs, there is a need for a set of accurate semi-empirical equations to meet both analysis and synthesis requirements, which may be used quickly on desk computers or calculators.

Ultimately the usefulness of any quasi-static microstrip parameter calculation is governed by the accuracy of the parameter ε_r, which is known to vary considerably from batch to batch in many alumina-type substrates. Some recently described methods of determining ε_r involve measurements on microstrip resonators,[3,4] and the analysis of the results requires accurate knowledge of how the quasi-static parameters depend on ε_r. This is a further justification for seeking computation errors of under $\pm 1\%$.

The problems of analysis and synthesis will be dealt with in turn in the following Sections, although they have much in common. The discussion deals particularly with the published work of Wheeler,[5,6] but several refinements, modifications and additions to his work are shown to be necessary in order to derive sufficiently accurate equations. The paper is particularly orientated towards alumina-type materials, with relative permit-

The Radio and Electronic Engineer, Vol. 46, No. 7, pp. 360-364, July 1976

tivities in the range 8 to 12. Outside this range accuracy is in some cases not maintained, but the procedures to be described may be used to derive modified equations to fit alternative substrate materials.

Because the wave propagated down a microstrip line is not a pure TEM wave, its velocity is frequency dependent, that is, the line is dispersive. It is convenient to account for this by using a frequency-dependent effective permittivity ε_{ef}. This paper deals exclusively with the low-frequency limit $\varepsilon_{ef}\ (f \to 0) = \varepsilon_{e0}$. The values of ε_{e0} calculated as described below may be used in available analytic equations[4, 7] to determine ε_{ef} as required.

2 Microstrip Analysis

2.1 Calculation of Z_0

The analytical equations of Wheeler[5, 6] form the basis of the theoretical discussion. After making the necessary conversions from his balanced transmission-line case to conventional unbalanced microstrip, we obtain the following familiar equations (using $c = 2{\cdot}998 \times 10^8$ m/s).

$$Z_0 = \frac{119{\cdot}9}{\sqrt{2(\varepsilon_r+1)}}\left[\ln\frac{8H}{W} + \frac{1}{32}\left(\frac{W}{h}\right)^2 - \tfrac{1}{2}\left(\frac{\varepsilon_r-1}{\varepsilon_r+1}\right)\times \times\left(\ln\frac{\pi}{2} + \frac{1}{\varepsilon_r}\ln\frac{4}{\pi}\right)\right] \quad (1)$$

for 'narrow strips', and

$$Z_0 = \frac{119{\cdot}9\pi}{2\sqrt{\varepsilon_r}}\left[\frac{W}{2h} + \frac{\ln 4}{\pi} + \frac{\ln e\pi^2/16}{2\pi}\left(\frac{\varepsilon_r-1}{\varepsilon_r^2}\right) + + \frac{\varepsilon_r+1}{2\pi\varepsilon_r}\left(\ln\frac{\pi e}{2} + \ln\left(\frac{W}{2h} + 0{\cdot}94\right)\right)\right]^{-1} \quad (2)$$

for 'wide strips', where e = exponential.

We note that the conversion referred to above involves writing $2Z_0$ for Wheeler's 'R', and $W/2h$ for his 'a/b'. The changeover point between the equations is suggested by Wheeler to be $a/b = 1$, which corresponds to $W/h = 2$, and not 1 as is very often quoted. It will be shown later that a changeover at $W/h = 1$ is very inadvisable.

An alternative equation for the 'narrow strip' case may be derived as follows from another part of Wheeler's paper.[6] In the discussion on the derivation of an equation for synthesis, the following equations are quoted, for 'narrow strips':

$$\frac{h}{W} = \frac{\exp(H')}{8} - \frac{1}{4\exp(H')} \quad (3)$$

where

$$H' = H_a + \tfrac{1}{2}\left(\frac{\varepsilon_r-1}{\varepsilon_r+1}\right)\left(\ln\frac{\pi}{2} + \frac{1}{\varepsilon_r}\ln\frac{4}{\pi}\right) \quad (4)$$

and

$$H_a = \frac{Z_0}{119{\cdot}9}\sqrt{2(\varepsilon_r+1)} \quad (5)$$

From (3),

$$H' = \ln\left[\frac{4h}{W} + \sqrt{16\left(\frac{h}{W}\right)^2+2}\right] \quad (6)$$

and solving for Z_0, we find:

$$Z_0 = \frac{119{\cdot}9}{\sqrt{2(\varepsilon_r+1)}}\left[\ln\left(4\frac{h}{W} + \sqrt{16\left(\frac{h}{W}\right)^2+2}\right) - -\tfrac{1}{2}\left(\frac{\varepsilon_r-1}{\varepsilon_r+1}\right)\left(\ln\frac{\pi}{2} + \frac{1}{\varepsilon_r}\ln\frac{4}{\pi}\right)\right] \quad (7$$

which differs slightly from equation (1).

To assess the accuracy of these equations it is necessary to compare them with a reliable alternative calculation. To begin with they may be compared with Wheeler's own work. Equations (1) and (2) are only approximations to the accurate conformal mapping solutions derived by Wheeler, which form a simultaneous set of equations which may be solved numerically by successive approximation techniques on a computer.[8] Program C270 of Reference 8 is in fact a synthesis program, which solves these simultaneous equations for $W/h > 1{\cdot}3$, and uses equations (3)–(6) for $W/h < 1{\cdot}3$. Figure 1 shows the percentage difference between Z_0 calculated from equations (1), (2) and (7), and Z_0 calculated by program C270, for the range $8 < \varepsilon_r < 12$. A slight discontinuity of about 0·1% in the C270 result is apparent at $W/h = 1{\cdot}3$. Two firm conclusions may be made from this Figure.

(a) Equation (7) lies closer than equation (1) to equation (2) over a wider range, and therefore should be used for improved accuracy.

(b) The changeover point between equations should be at about $W/h = 3{\cdot}3$ for minimum discontinuity (0·4%) or at about $W/h = 4{\cdot}5$ for smallest error (0·6%) relative to the C270 results. The choice of $W/h = 3{\cdot}3$ is recommended, since the error is about 0·9% at this value, whereas at $W/h = 4{\cdot}5$ the discontinuity just exceeds 1%. It will be noticed that a changeover at $W/h = 1$ would produce a discontinuity of 4% between equations (1) or (7) and equation (2). The minimum percentage difference between equations (1) and (2) is about 2·5% and occurs at $W/h = 1{\cdot}7$.

An independent assessment of the accuracy of these equations may be made by comparing them with Z_0 calculated from the Bryant–Weiss Green's function technique.[9] Program C267 of Ref. 8 is based on this method. Calculations are somewhat lengthy, and the accuracy depends on the number of subdivisions of the strip specified in the data. The broken curve in Fig. 1 represents C267 results involving 80 subdivisions for each W/h, for $\varepsilon_r = 10$, compared with C270 results. The accuracy of equations (2) and (7) is seen to be within 1% provided the changeover is made correctly.

2.2 Calculation of ε_{e0}

For narrow strips, from equation (7)

$$\sqrt{\varepsilon_{e0}} = \frac{Z_{01}}{Z_0} = \sqrt{\frac{\varepsilon_r+1}{2}} \times \left[\frac{H'}{H' - \tfrac{1}{2}\left(\frac{\varepsilon_r-1}{\varepsilon_r+1}\right)\left(\ln\frac{\pi}{2} + \frac{1}{\varepsilon_r}\ln\frac{4}{\pi}\right)}\right] \quad (8)$$

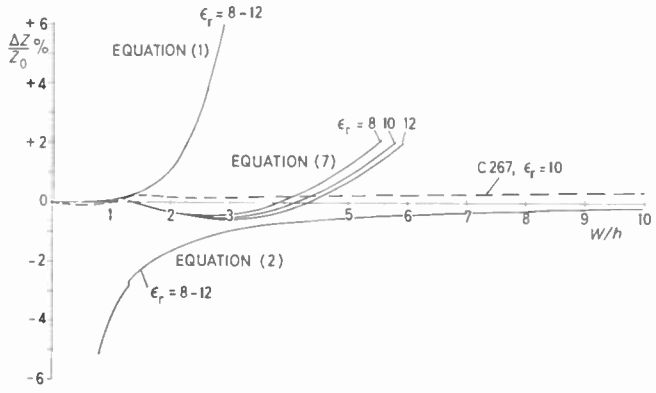

Fig. 1. Errors in Wheeler analysis equations.

Therefore

$$\varepsilon_{e0} = \frac{\varepsilon_r+1}{2}\left[1 - \frac{1}{2H'}\left(\frac{\varepsilon_r-1}{\varepsilon_r+1}\right)\left(\ln\frac{\pi}{2} + \frac{1}{\varepsilon_r}\ln\frac{4}{\pi}\right)\right]^{-2} \quad (9)$$

where H' is given in terms of W/h by equation (6). Wheeler[6] gives the expression

$$\varepsilon_{e0} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2H'}\left(\ln\frac{\pi}{2} + \frac{1}{\varepsilon_r}\ln\frac{4}{\pi}\right) \quad (10)$$

which is seen to be merely the first two terms of the binomial expansion of equation (9) and will therefore not be as accurate as equation (9). Figure 2 shows for the range $W/h < 2{\cdot}0$ the percentage difference in ε_{e0} calculated from C270 program results and from equations (10) and (9), the latter equation being identical to the results from the C270 program for $W/h < 1{\cdot}3$. The Bryant and Weiss results (C267) are also compared with C270 results in the figure. Equation (10) is seen to be unacceptably inaccurate for all W/h above 0·3, so equation (9) should always be used up to $W/h = 1{\cdot}3$. Above this value the error in equation (9) rises quite sharply, so an alternative equation is required.

It might be thought that accurate results for wide strips would be obtained from the ratio of impedances calculated from equation (2), but because of a larger

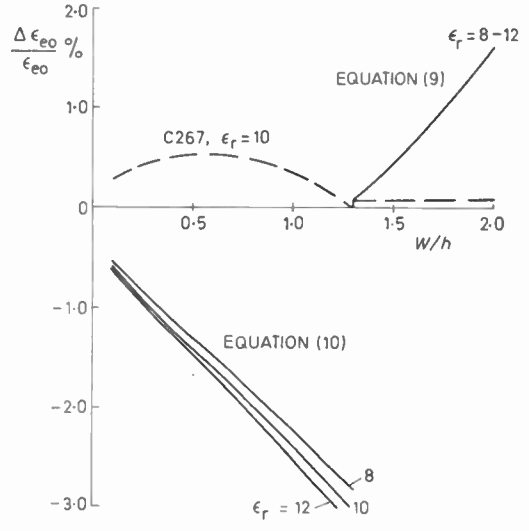

Fig. 2. Errors in ε_{e0} for narrow strips.

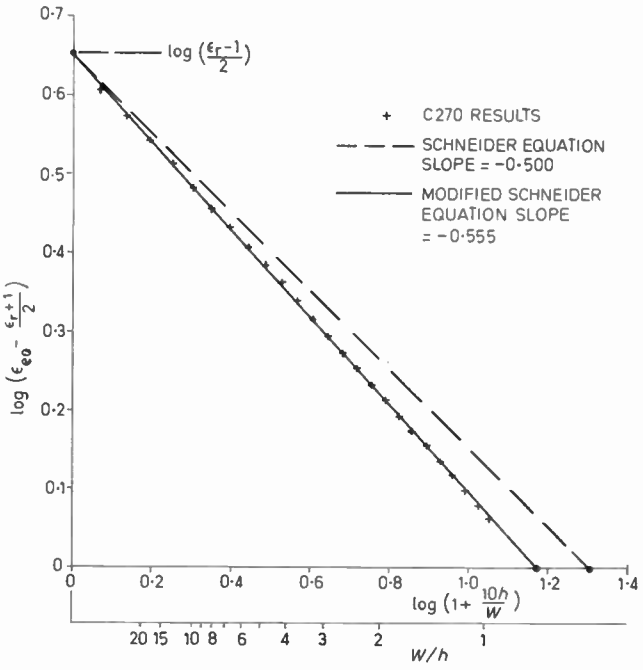

Fig. 3. Schneider equation for $\varepsilon_r = 10{\cdot}0$.

percentage error associated with Z_{01} in this equation, the accuracy is acceptable only in the range $1{\cdot}3 < W/h < 2{\cdot}0$. A much better result is obtained over the whole range $W/h > 1{\cdot}3$ by using a slightly modified form of Schneider's empirical equation for ε_{e0}. Schneider's original equation is[10]

$$\varepsilon_{e0} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left(1+10\frac{h}{W}\right)^{-0\cdot5} \quad (11)$$

The modified equation is

$$\varepsilon_{e0} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left(1+10\frac{h}{W}\right)^{-0\cdot555} \quad (12)$$

These two equations are compared in Fig. 3 with the C270 program results, and Fig. 4 shows that the percentage error associated with equation (12) is very small. The figure also shows the percentage difference between the C270 program and the Bryant and Weiss (C267) calculation of ε_{e0}, for $\varepsilon_r = 10$.

3 Microstrip Synthesis

3.1 Calculation of W/h

For narrow strips, equations (3), (4) and (5) are used, i.e.

$$W/h = \left[\frac{\exp H'}{8} - \frac{1}{4\exp H'}\right]^{-1} \quad (3A)$$

where

$$H' = \frac{Z_0\sqrt{2(\varepsilon_r+1)}}{119{\cdot}9} + \tfrac{1}{2}\left(\frac{\varepsilon_r-1}{\varepsilon_r+1}\right)\left(\ln\frac{\pi}{2} + \frac{1}{\varepsilon_r}\ln\frac{4}{\pi}\right) \quad (4A)$$

For wide strips, Wheeler gives the equation:

$$W/h = 2/\pi[(d_\varepsilon-1) - \ln(2d_\varepsilon-1)] + \frac{\varepsilon_r-1}{\pi\varepsilon_r}\left[\ln(d_\varepsilon-1) + 0{\cdot}293 - \frac{0{\cdot}517}{\varepsilon_r}\right] \quad (13)$$

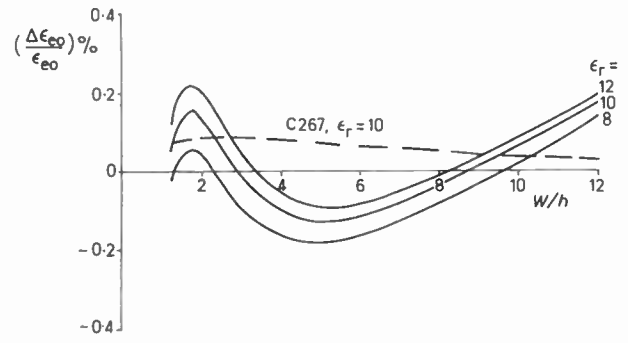

Fig. 4. Error in ε_{e0} using modified Schneider equation.

where

$$d_\varepsilon = \frac{59{\cdot}95\pi^2}{Z_0\sqrt{\varepsilon_r}} \qquad (14)$$

The errors associated with these equations when compared with the C270 results are shown in Fig. 5. The optimum changeover point between equations is this time more dependent on ε_r. A good compromise between small discontinuity between curves and low absolute error is achieved if the changeover is made when $Z_0 = (44-2\varepsilon_r)$ ohms. The discontinuity is then about 0·3% and the absolute error about 1·0%. Again, if the changeover were made at an impedance corresponding to $W/h = 1$, the error would exceed 4%.

3.2 Calculation of ε_{e0}

By definition $\sqrt{\varepsilon_{e0}} = Z_{01}/Z_0$ for a given W/h, so the permittivity calculation is better suited to the analysis approach where W/h is specified. For narrow strip synthesis however, direct calculation of ε_{e0} for a given Z_0 is possible, independent of W/h. From equations (8) and (4) we find

$$\sqrt{\varepsilon_{e0}} = \frac{Z_{01}}{Z_0} = \sqrt{\frac{\varepsilon_r+1}{2}} \times \times \left[\frac{H_a + \frac{1}{2}\left(\frac{\varepsilon_r-1}{\varepsilon_r+1}\right)\left(\ln\frac{\pi}{2} + \frac{1}{\varepsilon_r}\ln\frac{4}{\pi}\right)}{H_a}\right]$$

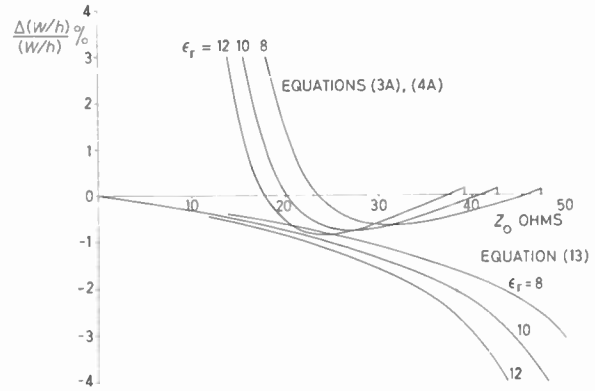

Fig. 5. Errors in Wheeler synthesis equations.

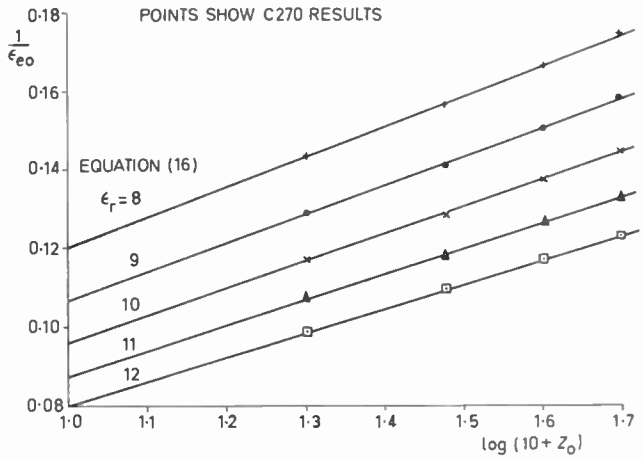

Fig. 6. $1/\varepsilon_{e0}$ versus log $(10 + Z_0)$.

hence using equation (5),

$$\varepsilon_{e0} = \frac{\varepsilon_r+1}{2}\left[1 + \frac{29{\cdot}98}{Z_0}\left(\frac{2}{\varepsilon_r+1}\right)^{\frac{1}{2}} \times \times \left(\frac{\varepsilon_r-1}{\varepsilon_r+1}\right)\left(\ln\frac{\pi}{2} + \frac{1}{\varepsilon_r}\ln\frac{4}{\pi}\right)\right]^2 \qquad (15)$$

This equation gives results identical to those computed by program C270 for $W/h < 1{\cdot}3$, i.e. for $Z > (63-2\varepsilon_r)$ ohms. The errors rise rapidly when W/h exceeds 1·3, so for wide strips a purely empirical relationship must be sought. The following formula has been found to give results with the required accuracy for the permittivity range $8 < \varepsilon_r < 12$ and for $8 < Z_0 < (63-2\varepsilon_r)$ ohms.

$$\varepsilon_{e0} = \varepsilon_r/[0{\cdot}96 + \varepsilon_r(0{\cdot}109 - 0{\cdot}004\varepsilon_r)(\log(10+Z_0) - 1)] \qquad (16)$$

Figure 6 shows how equation (16) is derived from a plot of $1/\varepsilon_{e0}$ versus log $(10+Z_0)$, and Fig. 7 shows the errors involved in using this formula. They are well within the required $\pm 1\%$ imposed limits.

It is of course possible to obtain W/h from the synthesis equations given in Section 3.1 and then use the analysis equations given in Section 2.2 to calculate ε_{e0}. This procedure is only necessary when $W/h > 1{\cdot}3$ and equation (15) is not useful. It requires separate application of two equations and does not find ε_{e0} independently of W/h. The error involved is shown in Fig. 7 to be lower than that given by equation (16). The variation in

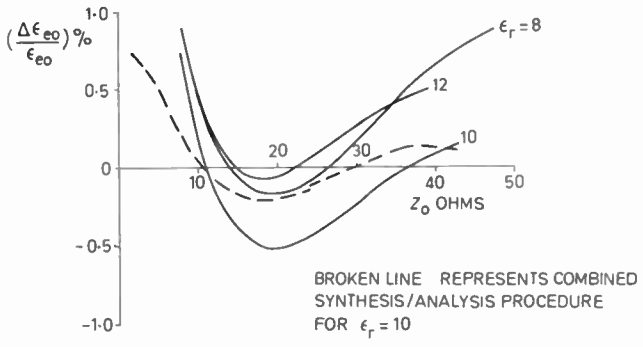

Fig. 7. Errors in ε_{e0} using equation (16).

error over the permittivity range 8–12 is also very much smaller than for equation (16). It may be considered preferable to use this procedure for calculating ε_{e0}, particularly since it is accurate to well below $Z_0 = 8\ \Omega$, but the more simple and direct calculation using equation (16) will be accurate enough for most purposes.

4 Conclusions

It has been shown by comparison with basic Wheeler mapping theory and independent Bryant and Weiss theory computations that certain specified analytical equations of Wheeler are suitable for the accurate calculation of quasi-static single microstrip line parameters. The accuracy involved is better than $\pm 1\%$ for alumina-type substrates, provided that the changeover between equations is made at the appropriate values of W/h for analysis, or Z_0 for synthesis. For the calculations of ε_{e0} direct from W/h, a more accurate equation has been obtained from Wheeler's equations for narrow strips, and a modification of Schneider's equation has been introduced for wide strips. Direct calculation of ε_{e0} from Z_0, which has hitherto not been discussed in the literature, is possible using an expression based on Wheeler's equations for high impedances, and a new empirical equation for low impedances.

The conclusions are summarized as follows. For analysis, equations (7) and (2) may be used to calculate Z_0, with a changeover at $W/h = 3{\cdot}3$ to minimize both the discontinuity and the absolute error. ε_{e0} may be calculated from equation (9) for $W/h < 1{\cdot}3$, and equation (12) for $W/h > 1{\cdot}3$.

For synthesis, W/h is calculated from equations (3A) and (4A), and from equation (13), with the changeover at $Z_0 = (44 - 2\varepsilon_r)$ ohms. ε_{e0} is calculated from equation (15) for high impedances, and from equation (16) for low impedances, the changeover being made at $Z_0 = (63 - 2\varepsilon_r)$ ohms, corresponding to $W/h \simeq 1{\cdot}3$.

All equations may be calculated quickly on desk computers or calculators, thereby providing rapid and accurate quasi-static design information for single-line microstrip components on alumina-type substrates. If extra accuracy is required, the error curves given in Figs. 1, 2, 4, 5 and 7 can be used to make the appropriate corrections to values calculated from the analytical equations.

5 Acknowledgments

Helpful discussions with Prof. M. H. N. Potok and Mr. T. C. Edwards at this laboratory are gratefully acknowledged.

Postscript

Since this paper was written the author has become aware of two papers with the same aim as this one, namely to present analytical equations for the accurate calculation of quasi-static microstrip parameters.[11, 12] The detailed approach is different in each paper, but in some respects there are close similarities between all three.

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IERE News and Commentary

New Plans for the D.M.S.

From 1st September the Diploma in Management Studies will be awarded by the Council for National Academic Awards. The CNAA is the body which validates undergraduate and postgraduate courses taken in polytechnics and other colleges outside the university sector. This year there are 77,500 students registered for the Council's awards in more than 100 colleges throughout the United Kingdom.

Over the past 15 years the D.M.S. has established a national reputation as an advanced course designed to meet the needs of practising managers, and in particular to enable them to achieve their maximum potential both as individuals and as members of a team. Whilst the philosophy of the D.M.S. is that of the general approach to the study of management, there are opportunities in the content of some courses, and more particularly through the teaching methods (small groups' work, projects, etc.), to cater for people drawn from a particular function or sector of industry, commerce or the public sector.

The normal entry requirement is a first degree, H.N.D. or H.N.C., membership of an approved professional body or an equivalent qualification, but other candidates who are over 27 and who have at least four years of managerial experience at an appropriately high level can also be considered. About 45% of candidates who completed the D.M.S. last year were between 28 and 35, 25% were more than 35 years old and 30% were 27 or under. Courses may be taken full-time, part-time or by block release, and arrangements can usually be made for someone who has to move during his course to join a course at another college. Many employers support the scheme and more than 70% of the students who completed the D.M.S. last year received some form of sponsorship.

Further details may be obtained from the CNAA, 344–354 Gray's Inn Road, London WC1 (Tel.: 01-278 4411), which also provides a list of colleges which offer the D.M.S.

Register of Retired Chartered Engineers

The RRCE (Register of Retired Chartered Engineers) is available, free, to industry and commerce as a source of recruitment for short-term, *ad hoc* consultative services, quality assurance inspection, etc. All Registrants are retired members of one or more of CEI's fifteen constituent member institutions and they offer, collectively, a vast range of accumulated knowledge, skills and experience. Details of RRCE can be supplied on receipt of a stamped addressed envelope to The Engineering and Building Centre, Broad Street, Birmingham 1; or to G. M. Stephens, C.Eng., Hon. Registrar, RRCE, 1414 Warwick Road, Knowle, Solihull, West Midlands B93 9LG.

British Pattern Recognition Association Formed

Pattern Recognition is usually taken to mean theory, technique and instrumentation for retrieval, processing and classification of optical, acoustic and other patterns. This has become a subject in its own right and at a recent meeting in University College London, the British Pattern Recognition Association was formed.

The aims of the Association are to promote the knowledge and application of pattern recognition and to serve as the British Branch of the proposed International Association for Pattern Recognition. The Association, which has already eighty members who have belonged to an informal discussion group set up some years ago, hopes to attract further members from universities, industry and the Civil Service, linking basic research with commercial applications.

There are now many machines which use pattern recognition techniques, for example the optical character readers used for sorting post or processing cheques and baggage handling equipment for airport terminals which will recognize simple spoken commands. In the laboratory there are instruments which will analyse a wide range of visual material from microscopes, photographs, X-rays etc., and will automatically select, count and measure specific objects in the image.

Further information on the Association can be obtained from the Secretary, Dr. M. J. B. Duff, Department of Physics and Astronomy, University College, London WC1E 6BT.

Standard Frequency Transmissions—May 1976

(Communication from the National Physical Laboratory)

May 1976	Deviation from nominal frequency in parts in 10^{10} (24-hour mean centred on 0300 UT)	Relative phase readings in microseconds NPL—Station (Readings at 1500 UT)	
	Droitwich 200 kHz	*GBR 16 kHz	†MSF 60 kHz
1	0·0	698·5	612·8
2	0·0	698·4	612·6
3	0·0	698·5	612·6
4	0·0	698·4	612·6
5	0·0	698·5	612·6
6	0·0	698·4	612·3
7	0·0	698·3	612·2
8	0·0	698·3	612·0
9	0·0	698·1	612·2
10	0·0	698·5	612·4
11	0·0	698·2	612·4
12	0·0	698·0	612·5
13	0·0	698·1	612·4
14	0·0	698·2	612·4
15	0·0	697·9	612·5
16	0·0	697·9	612·5
17	0·0	698·0	612·7
18	—	697·8	612·7
19	0·1	697·7	612·6
20	0·1	698·7	612·5
21	0·1	697·9	612·4
22	0·1	—	612·5
23	0·1	697·7	612·7
24	—	697·7	612·3
25	0·1	697·5	612·3
26	0·1	697·5	612·3
27	0·1	697·8	612·3
28	0·1	697·8	612·5
29	0·1	697·8	612·2
30	0·1	697·9	612·0
31	0·1	698·0	612·0

All measurements in terms of H-P Caesium Standard No. 344 agrees with the NPL Caesium Standard to 1 part in 10^{11}.

Institution Premiums for 1975

The Council of the Institution announces that authors of the following papers are to receive Premiums for outstanding papers published in the Journal during 1975.

MAIN PREMIUMS

HEINRICH HERTZ PREMIUM *Value £50*

(Physical or mathematical aspects of electronics or radio)

'Solar-terrestrial relations and short-term ionospheric forecasting'
by F. E. Cook and C. G. McCue (Ionospheric Prediction Service, Department of Science, Australia)
(Published in the January/February issue of the Journal)

MARCONI PREMIUM *Value £50*

(Engineering)

'Microwave device applications of epitaxial magnetic garnets'
by Dr. J. D. Adam, Professor J. H. Collins and Dr. J. M. Owens (University of Edinburgh)
(December)

SPECIALIZED TECHNICAL PREMIUMS

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(Computers)

'Magnetic bubble domain memories in epitaxial garnet films'
by Dr. J. L. Tomlinson (State Polytechnic University, Pomona, California) and Dr. H. H. Wieder (Naval Electronics Laboratory Centre, San Diego, California)
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by P. D. L. Williams (Decca Radar, Chessington)
(August)

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Lord Rutherford Premium (Atomic or nuclear physics)

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Dr. V. K. Zworykin Premium (Medical or biological electronics)

Leslie McMichael Premium (Management techniques)

Eric Zepler Premium (Education)

Hugh Brennan Premium (North Eastern Section Paper)

Sir J. C. Bose Premium (Paper by Indian author)

Local Sections Premium

The presentation of Premiums will be made by the President at the Institution's Annual General Meeting in London on Wednesday, 6th October, 1976.

Colloquium Report

'Automatic Production'

Organized by the Electronics Production Technology Group and held in London on 21st April 1976

This inaugural colloquium of the Group was held at the Royal Institution and was attended by over eighty members. Opening the meeting, the Group Committee Chairman, Mr. A. F. Dyson, first briefly described the newly-formed Group's sphere of interest and projected activities, and then introduced the Colloquium programme by explaining that the paper presentation order followed normal production sequence from component insertion, through soldering, to final test.

The first paper, by Mr. P. Fenner of Universal Instruments (Electronics) Ltd. entitled 'Automatic Component Insertion', concentrated on the machinery used for this process, starting with descriptions of early simple types and the constraints on machine design dictated by the physical characteristics of the components to be processed. He particularly emphasized the lack of mechanical standards in components typified by the infinite variation of size and shape of capacitors alone which made the machine designer's task a difficult one. A notable exception was the introduction of the automatic insertion equipment. Mr. Fenner went on to describe the modern bandolier-type component sequencing machines. He indicated general limitations of printed board size and component layout which such methods imposed upon the designer and emphasized the necessity of close co-operation between design and production departments. Mr. Fenner extolled the advantages of automatic insertion which included economy of assembly time, repeatable accuracy, flexible production and guarantee of quality. He concluded by giving examples of production rates and forecast more common use of machines which would allow direct link-up with computer aided design and production management information systems.

The next paper, 'What a Designer Must Remember' by Mr. J. C. Guerin from the Production Engineering Department of La Radiotechnique, France, carried the colloquium theme further by describing first-hand experience of automatic assembly, in particular the considerations of printed board layout and component choice made at the design stage. Mr. Guerin showed a number of tables and layout diagrams to illustrate his points and there was no doubt that the problems had been considered very carefully. The paper included analyses of costs and production rates which Mr. Guerin supplemented with comparisons between theoretical figures and those which emerged from a sample period of work at his factory.

The third paper, 'Reliability in Automatic Soldering Processes' delivered by Dr. W. Rubin, Research Director of Multicore Solders Ltd., changed the emphasis from component handling and assembly to the joining process. Dr. Rubin said that insufficient attention was given to the soldering phase in automatic production as poor solderability of component leads could seriously reduce the cost advantages mentioned by the previous speakers. He showed slides of various soldered joints to illustrate the problem which affected subsequent testing and service reliability. Referring to the regularized component layout imposed by automatic insertion, Dr. Rubin stated that this helped to attain good joints when utilizing mass soldering machinery, and chemical aids such as liquid fluxes or anti-oxidants together with low impurity solders would go a long way towards trouble-free soldering. Dr. Rubin described various conveyor soldering apparatus and finished by discussing solderability testing and a new device for non-destructive testing on through-hole-plated printed boards.

The final stage of electronic equipment production is testing and a paper by Mr. D. G. Gemmell, Director of Operations of Membrain Ltd., concluded the proceedings. Mr. Gemmell started by showing typical examples of printed board assemblies common throughout the industry which ranged from analogue circuitry discrete component types to large digital d.i.l. integrated circuit types. He appreciated the pressure on designers to produce ever more sophisticated hardware in reduced space but the trend was leading to testing problems of massive proportions. Manual methods were becoming impracticable so automatic testing in some degree was the alternative. Mr. Gemmell gave a general appraisal of equipment such as simple diagnostic aids, comparison analysers utilizing a 'known good board', and lastly full computer-controlled diagnostic equipment. He explained that the choice of equipment must take into account the skill of the technicians available and the cost of sustaining them. Recent trends provided for automatic diagnostic aids on production lines which allowed testing and fault location to be carried out rapidly, largely by technically unskilled operators with a small amount of technician support. The trend was particularly evident on digital printed board assemblies. Diagrams showed the application of software simulation of logic assemblies, a technique which has been significant in providing quantitative data on the capability of the test procedure to detect faults. The last part of Mr. Gemmell's paper was taken up with methods of gaining access to circuit nodes such as hand-held computer guided probes, 'bed-of-nails' jigs and in-circuit testing techniques for analogue and discrete component assemblies.

A useful discussion followed in which several questions requiring answers to which more than one speaker contributed emphasized the continuity of the colloquium theme. The unique gathering of automatic production expertise led to many questions concerned with specific applications of the techniques described.

R. MARIE

Members' Appointments

CORPORATE MEMBERS

Mr. J. R. Brinkley (Fellow 1952, Member 1948) has been appointed Managing Director of Redifon Ltd. He joined Redifon in 1971 as an Executive Director, subsequently becoming Deputy Chairman of the Company. Mr. Brinkley is also Chairman and Managing Director of Redifon Telecommunications Ltd. and Chairman of Redifon Computers Ltd. He served as a member of the Institution's Council from 1963-66.

Mr. P. L. Mothersole (Fellow 1961, Member 1957, Graduate 1952) has been appointed Managing Director of V. G. Electronics Ltd., who produce specialized electronic equipment, notably digital television and associated transmission equipment. Mr. Mothersole was with the Philips Group for some 23 years, initially at Mullard Research Laboratories, then with the Central Application Laboratory at Mitcham. In 1969 he went to Pye TVT as Engineering Manager and four years ago he rejoined Mullard as Commercial Chief Engineer.

Mr. Mothersole has contributed several papers to the Institution's Journal and Conference Proceedings, and served on the Communications Group Committee, for several years as its Chairman. He has been a member of the Council since 1973.

Mr. R. W. Timms (Fellow 1973, Member 1963) has been promoted to Site Quality Manager at Marconi Space and Defence Systems Ltd. at Hillend, Fife, where he has been Engineering Services Manager since May 1974.

Mr. J. I. Brown (Member 1946) has taken up a technical liaison appointment with Avel-Lindberg Ltd. In 1954 Mr. Brown established the firm of Aveley Electric Ltd., of which an offshoot was Avel Products Ltd., forerunner to Avel-Lindberg Ltd. He was for a number of years a member of the Medical and Biological Electronics Group Committee.

Captain M. D. Cherry, R.Sigs. (Member 1973, Graduate 1970) has returned to Europe from Malaysia, where he had been posted on secondment as Lecturer in Communications Engineering with the Malaysian Armed Forces Signal School, and is now serving with BAOR as Technical Officer, Communications.

Mr. F. K. Chorley (Member 1956, Graduate 1951) has been appointed Managing Director and Chief Executive of the newly formed product subsidiary, Plessey Electronic Systems Ltd (PESL); he was Managing Director of Plessey Avionics and Communications, Ilford.

Mr. P. J. Gallagher, Ph.D., M.Sc. (Member 1969, Graduate 1966) who was Principal Lecturer at Bradford College, has been appointed Head of the School of Technology and Design. Dr. Gallagher joined the College in 1964 as Senior Technician.

Mr. J. H. Gidman (Member 1965, Graduate 1963) has been promoted to Principal Air Traffic Engineer with the National Air Traffic Services in London. From 1971 he was with the Civil Aviation Flying Unit at Stansted Airport, first as a Planning and Evaluation Officer and subsequently as Senior Air Traffic Engineer.

Inst. Lt. Cdr J. Grady (Member 1973) who served as Training Design Technology Officer in the Air Engineering School HMS *Daedalus* for the past three years, is now reading for the degree of M.Phil. in the Department of Education at the University of Southampton.

Mr. M. W. G. Hall (Member 1962, Graduate 1958) who has been with Marconi Instruments Ltd. since 1958, latterly as Sales Manager with the Service Division, has been appointed Product Sales Manager with Electronic Brokers Ltd., who distribute electronic instruments produced in Italy and the United States.

Mr. A. J. Henk (Member 1973) has joined Crow of Reading Ltd. as Chief Engineer in charge of the Company's design, development and production activities in the television field. Mr. Henk was previously a Telecommunications Engineer with Burmah Engineering Petrocarbon Developments, working on North Sea oil-rig communication systems.

Mr. D. Hickey (Member 1966, Graduate 1959) has been appointed Head of the Department of Electrical Engineering, Hobart Technical College, Tasmania. He took up permanent residence in Australia in 1972 on retirement from the Royal Artillery with the rank of Major.

Mr. R. H. Jones (Member 1973, Graduate 1967) has become Engineering Sales Manager, Instrument Division, with Circuitaire (Pty.) Ltd., Booysens, Transvaal, South Africa. He was previously Biomedical Sales Engineer with Baird & Tatlock (Pty.) Ltd. of Johannesburg.

Mr. F. Kocsis, Dip. Ing. (Member 1967, Graduate 1958) has been appointed Chief Engineer of Lee Green Precision Industries Ltd. He retains his directorship of Acoustic Laboratories Ltd., Bodmin.

Mr. U. K. Leung (Member 1972, Graduate 1969) who emigrated to the United States from Hong Kong in 1975, has taken up the post of Customer Engineer with the ITEL Corporation in Palo Alto, California.

Mr. J. Soobarah, B.E. (Member 1973, Graduate 1969) who was previously Superintendent Engineer for the Port Louis and Northern Area, in the Mauritius Telecommunications Department has joined the Department of Civil Aviation as Aeronautical Communications Engineer.

Mr. J. A. S. Weir (Member 1967, Graduate 1964) has completed a Master of Business Administration degree at Cranfield Business School, and has joined ICL Ltd. in London as a Systems Consultant. He was previously with the National Economic Development Office, London, as Secretary to the Advisory Group on Data Transmission.

Mr. Y. A. B. D. Wickramasinghe (Member 1974, Graduate 1971) is now Electronics Engineer in the Electronics Department of the Faculty of Engineering, University of Sri Lanka. His previous appointment was Scientific Officer (Electronics) with the Faculty of Medicine in the University.

NON-CORPORATE MEMBERS

Mr. P. J. R. Hughes (Graduate 1968) who since 1968 has been Industrial Engineer for integrated circuits with Mullard Ltd., Southampton, has been awarded the Sir Henry Fildres Medal and Prize by the Institution of Works Managers, after completing a course of study at Southampton College of Technology for the IWM's Certificate in Industrial Management. This award is given every year to the best student over 30 years of age gaining the Certificate.

Mr. M. Part, B.A. (Graduate 1970) has been promoted from Assistant Executive Engineer to Executive Engineer, and is now with the Post Office External Telecommunications Executive.

Sgt. I. D. Matthews, RAF (Associate Member 1974) has been transferred from the posting of SNCO, Airfield Radar Servicing, RAF Gan, to SNCO 3rd Line Radar Servicing, RAF North Luffenham, Leicestershire.

J. R. BRINKLEY

P. L. MOTHERSOLE

J. I. BROWN

INSTITUTION OF ELECTRONIC AND RADIO ENGINEERS

Applicants for Election and Transfer

THE MEMBERSHIP COMMITTEE at its meetings on 17th June and 15th July 1976 recommended to the Council the election and transfer of the following candidates. In accordance with Bye-law 23, the Council has directed that the names of the following candidates shall be published under the grade of membership to which election or transfer is proposed by the Council. Any communication from Corporate Members concerning the proposed elections must be addressed by letter to the Secretary within twenty-eight days after publication of these details.

Meeting: 17th June 1976 (Membership Approval List No. 222)

GREAT BRITAIN AND IRELAND

CORPORATE MEMBERS

Transfer from Member to Fellow

SLAMIN, Brendan Joseph. *Glasgow.*

Direct Election to Fellow

BEAMOND, Roger Hugh. *Ilford, Essex.*

Transfer from Graduate to Member

CONIBEAR, Peter Terence. *Havant Hampshire.*
HALL, John Alfred. *Sutton, Surrey.*
MARKS, David. *London.*
McCABE, Eugene Pearse. *Dundalk, Co. Louth, Ireland.*
PAYNE, Peter Alfred. *Newport, Gwent.*

Direct Election to Member

COOK, James Robin Watson. *Pershore, Worcestershire.*
DAVIES, Eric Mansel. *Pontardawe, West Glamorgan.*
GLEN, Kenneth Munley. *Alexandria, Dunbartonshire, Scotland.*
RAINBOW, Keith Herbert James. *Surbiton, Surrey.*
STEPHENS, John Brian. *Staines, Middlesex.*

NON-CORPORATE MEMBERS

Direct Election to Graduate

DEACON, Christopher Lawrence. *Bosham, Sussex.*
DEANE, Phillip. *Woodbridge, Suffolk.*
OLANIYI, Joseph Abimbola. *London*

Direct Election to Associate Member

BRYANT, Arthur James. *Brentwood, Essex.*
GILLHAM, Christopher Anthony. *Bishopthorpe, York.*
MANUH, Emmanuel Kwasi. *London*

STUDENTS REGISTERED

HEWITT, David Paul. *Strood, Kent.*
RICHARDS, Peter James. *Harlow, Essex.*

OVERSEAS

CORPORATE MEMBERS

Transfer from Member to Fellow

SHERWOOD, Sydney Dean. *Hong Kong.*

Direct Election to Fellow

SWAILEM, Abdul Mohsen. *Riyadh, Saudi Arabia.*

Transfer from Graduate to Member

LEWIS, Keith. *Randburg, Transvaal.*

NON-CORPORATE MEMBERS

Direct Election to Graduate

NG, Ha Wai. *Hong Kong.*
THEIVASIGAMANY, Selliah. *Dehiwela, Sri Lanka.*

Direct Election to Associate Member

ACHIEKWELU, Felix Ehalu. *Calabar, Nigeria.*
DOWLMAN, Edward Rex. *Abu Dhabi, United Arab Emirates.*
TAN, Tew. *Singapore.*

STUDENTS REGISTERED

CANAGASABEY, Darrell Radley. *Nugegoda, Sri Lanka.*
CHAN, Pak Ching. *Hong Kong.*
HARJIT SINGH. *Selangor, Malaysia.*
HO Siew Wah. *Singapore.*
LIM, Chee Beng. *Singapore.*
MAK, Lai Weng. *Singapore.*
SET, Nge Yong. *Singapore.*
SIM, Thong Liang. *Singapore.*
TEO, Kok Sin. *Singapore.*
UMARU, Mohammed Ndatsu. *London.*
WONG, Mee Choy. *Selangor, Malaysia.*
WOO, Foong Kheen. *Singapore.*
YU, Khee Chen. *Singapore.*

Meeting: 15th July 1976 (Membership Approval List No. 223)

GREAT BRITAIN AND IRELAND

CORPORATE MEMBERS

Transfer from Graduate to Member

KENNARD, Gordon Michael. *Basingstoke, Hampshire.*
LANDSBERG, Peter John Nicholas. *Morden, Surrey.*
THOMAS, Stephen Joseph William. *Lichfield, Staffordshire.*

Transfer from Associate Member to Member

HURRELL, Ernest Peter. *Holyhead, Gwynedd.*

Transfer from Student to Member

DANIEL, Barry George. *Borehamwood, Hertfordshire.*

Direct Election to Member

ALEXANDER, John. *Purley, Surrey.*
FLAVELL, David Graham. *Sturminster Newton, Dorset.*
WILLIAMS, Raymond Henry. *Great Mollington, Cheshire.*

NON-CORPORATE MEMBERS

Transfer from Student to Graduate

ADEPOJU, Samson Ibitayo. *Woolwich, London.*
ASHWORTH, Martyn Keith. *Sheffield.*
CRAWFORD, Ian Fergus. *Gillingham, Kent.*
ELSTOB, Harry Leigh. *Hemel Hempstead, Hertfordshire.*

Direct Election to Graduate

EVANS, David Meurig. *Portsmouth, Hampshire.*
STEVENSON, John Graham. *Grimsby, South Humberside.*

Transfer from Student to Associate Member

CLARKE, Nigel William. *Harlow, Essex.*

Direct Election to Associate Member

ALLEN, Dudley Keith. *Ashford, Kent.*
BROOKS, Kenneth Robert. *Bristol.*
CLARK, Kenneth Norman. *Slough, Buckinghamshire.*
GIRRARD, Anthony Edward. *Bromley, Kent.*
HAMILTON, Ian George Shand. *Scarborough, Yorkshire.*
METCALFE, Peter John. *SHAPE.*
O'CONNELL, Sean Oliver. *Leixlip, County Kildare, Republic of Ireland.*
STEWARD, Michael John. *Church Crookham, Hampshire.*
YATES, Edwin. *East Grinstead, Sussex.*

Direct Election to Associate

BLACK, Sidney Henry. *Bottisham, Cambridgeshire.*
FRASER, James Mathieson. *Elie, Fife, Scotland.*

STUDENTS REGISTERED

COULES, Victoria. *Plymouth, Devon.*
STACKHOUSE, Thomas Keith. *North Shields, Tyne and Wear.*
THORNE, Brian John. *Swansea, South Wales.*
WAUGH, William Richard. *Anglesey, North Wales.*

OVERSEAS

CORPORATE MEMBERS

Transfer from Member to Fellow

PHILADELPHIA, James Lambert. *Georgetown, Guyana.*

Transfer from Graduate to Member

WONG, Man Him. *Hong Kong.*

Direct Election to Member

THORPE, Leslie James. *Bulawayo, Rhodesia.*

NON-CORPORATE MEMBERSHIP

Transfer from Student to Graduate

KWAN, Hon Keung. *Hong Kong.*
LO, Yu Chiu. *Hong Kong.*
SIU, Wan Chi. *Hong Kong.*

Direct Election to Graduate

NAKHLA, Nagat Benjamin. *Khartoum, Sudan.*
PAU, Wai Man. *Hong Kong.*

Direct Election to Associate Member

BAKARE, Taoheed Abiodun Adedeji. *Ikorodu, Nigeria.*
CHEW, Teck Ching Tek Kium. *Ulu Tiram, Malaysia.*
LEO, Teng Yong. *Tao Payoh, Singapore.*
METCALFE, Leonard. *Nairobi, Kenya.*
NUGENT, Daniel. *Limassol, Cyprus.*
OKORO, Nkume Livingstone. *Enugu, Nigeria.*
RECKORD, Winston Anthony. *Kingston, Jamaica.*
REECE, Kenrick Francis. *Barbados.*
SALAM, Abdus. *Hazara, Pakistan.*
TSANG, Chiu Man. *Hong Kong.*

Direct Election to Associate

JASSA, Singh. *Klang, West Malaysia.*

STUDENTS REGISTERED

ANG, Koon Han. *Singapore*
CHOW, Weng Thim. *Singapore.*
CHUAH, Tai Eu. *Penang, Malaysia.*
METAX, Sotos. *Nicosia, Cyprus.*
TAN, Siak Ann. *Singapore.*
TEH, Peng Guan. *Malacca, West Malaysia.*
YAM, Siu-Ning. *Hong Kong.*
ZAINUDDIN, Ahmad Sapon. *Singapore.*

New Books Received

All the books which are described below are available in the Library and may be borrowed by members in the United Kingdom. A postal loan service is available for those who are unable to call personally at the Library.

Teletext: Data Transmission by Television

TIMOTHY JOHNSON. The Financial Times, London 1975. 296 × 207 mm. 187 pp. £80·00.

CONTENTS: The United Kingdom unified standard. Receiver design and costs. The broadcasting unit. Comparison of teletext standards. Public broadcasting applications. Broadcasting requirements. Communications, data processing and data recording. Consumer markets for receivers. Other associated markets. Future development and commercial implications. Active organizations.

This book, published in early 1975, was the first to deal with Teletext in its widest technical and commercial aspects. There are chapters covering the United Kingdom system itself and its reception and transmission. The range of systems proposed in other countries are compared historically and in terms of the applications, general communications and data processing are considered. The predictions in this section have now come to pass with the development of the Post Office 'Viewdata' system. They gain importance since recent market surveys indicate the importance of interactive systems like Viewdata and give general encouragement to the commercial development of Teletext. This book is completed by a detailed analysis of the consumer and commercial markets for Teletext and likely future developments. There is a wealth of excellent tables and illustrations and a list of active organizations.

The 1976 reader must bear in mind that much further experience has now been gained and the UK system has proved itself both subjectively and objectively. The critical aspects of the system and the effect of tolerances is now understood. Certain details of the system have been the subject of change both to increase its flexibility and to achieve a high degree of compatibility between broadcast Teletext and Viewdata. Another new feature is the use of the micro-processor in the receiver decoder as an alternative to special l.s.i.

In spite of these changes, Mr. Johnson's opinions are confirmed and as a result, some of the reservations are dispelled. To summarize, anyone interested in Teletext should read it.

B. J. ROGERS

The Bruneval Raid

GEORGE MILLAR. The Bodley Head, London, 1974. 22·5 × 14 cm. 208 pp. £2·50.

A very readable account of a notable operation of the Second World War which captured important equipment from a German coastal radar station.

Industrial Lasers and their Applications.

J. E. HARRY. McGraw-Hill Ltd., Maidenhead, 1974. 25 × 19·5 cm. 201 pp. £6·00.*

CONTENTS: Introduction to optical radiation processes. Laser characteristics. Materials and components used in laser systems. Industrial lasers. Industrial laser applications. Safety.

Intended for the engineer wishing to apply lasers in his own industry.

(*Mr. Harry is Electricity Council Senior Lecturer in Electroheat at Loughborough University.*)

Gunn-effect Electronics

B. G. BOSCH and R. W. H. ENGELMANN. Pitman, London 1975. 235 × 155 mm. 434 pp. £16·00.*

CONTENTS: The transferred-electron effect ((Generalized Gunn effect). Space-charge dipole domains (Gunn effect in strict sense). Dipole-domain free operation. Comparative description of mode properties. Material and device technology. Microwave devices and applications. Pulse generation and processing.

It is valuable to have an important field of development systematically reviewed and assessed by active and senior experts as soon as it has acquired a certain maturity. It is therefore certainly the right moment for Professor Bosch and Dr. Engelmann to present their extensive treatment of the physics, materials technology and microwave applications of the transferred electron effect. The many contributions which have been published in this rapidly developed field are critically assessed in this coherent and extensive volume. It will be useful both for the newcomer to this field because all basic concepts are carefully described, as well as for the well established expert, as the treatment is indeed comprehensive with innumerable references. Personally I enjoyed therefore the latter chapters particularly as I found many interesting details which I had not found reviewed previously in such a consistent manner.

Of course one has to keep in mind that the field of Gunn devices and its materials technology is still moving rapidly. Therefore, the understanding achieved since the beginning of 1974 has not been covered by this book which must have been completed in 1973 judging from the publication dates of the latest references. Thus, some of the later studies are not yet included, for example on energy relaxation affecting oscillator efficiency and mode selection (even down to X-band frequencies), the design of special cathodes for InP in view of high efficiencies, and the cut-off frequency assessment. However, these are fine details which possibly represent now the final development stages of an otherwise mature and completed device type.

This book can therefore be expected to be a comprehensive and useful source of information for many years to come.

H. L. HARTNAGEL

(*Professor Bosch is at the Ruhr Universität, Bochum, and Dr. Engelmann is with Hewlett Packard, Palo Alto, California.*)

Dictionary of Television and Video Recording

W. E. CLASON. Elsevier Scientific Publishing Co., Amsterdam 1975. 22 × 15 cm. 608 pp. £22.

Based on Elsevier's Dictionary of Television Radar and Antennas but completely revised, this six-language dictionary (English/American, French, Spanish, Italian, Dutch and German) will be invaluable for engineers faced with publications in these languages. Brief definitions of terms are associated with the English/American section and other languages are cross referred to these entries.

(*Mr. Clason, who is now retired, was head of the Translation Department of N. V. Philips Gloeilampenfabrieken, Eindhoven.*)

Power Electronics

F. CSAKI (Editor). Akademiai Kiado, Budapest, 1975. 24·5 × 17 cm. 708 pp. £18·70.

CONTENTS: Line commutated convertors. A.c. choppers. D.c. choppers. Inverters. Reactors, transformers, magnetic amplifiers. Vacuum elements. Gas filled elements. Semiconductor devices. Convertor control. Design, temperature, cooling and protection of semiconductor equipments. Power-electronics equipment.

An impressively comprehensive and authoritative book, competently translated into English.

(*Professor F. Csaki is in the Department of Automation at the Technical University of Budapest.*)

Electronics—an Elementary Introduction for Beginners (S I Units)

L. W. OWERS. Publication Mailing Services 1974. 21 × 15 cm. 119 pp. £1·45.

CONTENTS: Electric charge. The fundamental particles. Atoms and energy. Free electrons. Electric current. Conductors and resistors. Capacitors and inductors. Thermionic valves. Semiconductor devices.

(*Mr. L. W. Owers (Member 1970) is with Mullard Mitcham, Surrey.*)

Book Supply Service

As a service to members, the Institution can supply copies of most of the books reviewed in the *Journal* at list price, plus a uniform charge of 35p to cover postage and packing.

Orders for these books, which are denoted by an asterisk (*) after the price, should be sent to the Publications Department at Bedford Square and **must** be accompanied by the appropriate remittance.

Magnetic Bubbles

T. H. O'DELL. Macmillan, London 1975. 24 × 16 cm. 159 pp. £8·50.*

CONTENTS: Magnetic bubble domains and bubble domain devices. Magnetostatics. Magnetic bubble domain materials and their characteristics. Bubble domain dynamics. Bubble domain propagation tracks and detectors.

An introductory monograph collecting fundamental theory in this relatively new field.

(*Dr. O'Dell is Reader in Electronics in the Department of Electrical Engineering, Imperial College, London.*)

Videotape Recording

J. F. ROBINSON. Focal Press, London 1975. 23·5 × 16 cm. 303 pp. £4·50.

CONTENTS: Tape recording principles. Basic requirements of videotape recording. The broadcast quadruplex format. CCTV formats. FM theory. Signal systems. Servo-mechanisms. Geometrical errors. Time base error correction. Colour correction in CCTV. Cassettes and cartridges. Editing. Magnetic video discs and slow motion techniques.

A comprehensive coverage for student, user and development engineer.

(*Mr. Robinson, formerly with Ampex GB Ltd. is now chief engineer of a television station overseas.*)

Elements of Transistor Pulse Circuits (2nd edition)

T. D. TOWERS. Newnes-Butterworths, London 1974. 22 × 14 cm. 198 pp. £3·50.*

CONTENTS: Semiconductor and pulse circuits. Linear pulse amplifiers. Astable multivibrators. Monostable multivibrators. 'Eccles-Jordan' bistable multivibrators. Waveform shaping. 'Pumps' and 'Schmitts'. Blocking oscillators. 'Gates'. Counter/timers (frequency meters). Timebases (sweep-generators).

Based on a series of articles in *Wireless World*.

(*Mr. T. D. Towers (Member 1968) was with Newmarket Transistors Ltd. from 1958 to 1973.*)

Integrated Circuit Databook

Plessey Semiconductors Ltd., Swindon, Wilts 1974. 21 × 15 cm. 249 pp. £1·00.

CONTENTS: Linear integrated circuits. Consumer (including TV) integrated circuits. MNOS (non-volatile memory elements). Digital integrated circuits. Packages and ordering information.

Linear Electronic Circuits and Systems

G. D. BISHOP. Macmillan, London 1974. 23 × 15·5 cm. 114 pp. £2·25.*

CONTENTS: Signal processing. Network analysis. Transistors and their use in linear circuits. Amplification. Feedback. The operational amplifier. Basic operational amplifier functions. Operational amplifier applications.

Intended for students and technicians.

(*Mr. Bishop is Senior Lecturer at Paddington Technical College.*)

What Goes on in Telecommunications?

PAUL ROBERSON. Woodhead-Faulkner (Publishers) Ltd., Cambridge, 1974. 21 × 15 cm. 80 pp. 90p.

CONTENTS: Introducing telecommunications. Telegraphy. The telephone. Radio. Television. World-wide communications. Data communications. The future. Careers in telecommunications.

A popular description sponsored by Swedish Ericsson Telecommunications.

(*Dr. Roberson is a scientific journalist.*)

Telecommunications (2nd edition)

J. BROWN and E. V. D. GLAZIER (revised by J. Brown). Chapman & Hall Ltd., London 1974. 23 × 15·5 cm. 382 pp. £3·00.*

CONTENTS: The nature of the signal. Amplitude and angle modulation. The properties of communication channels. The response of linear channels. Noise and its limiting effect on communication. Digital communication. Communication theory. Communication systems. The principles of position fixing by radio.

This edition introduces digital systems. It is appropriate for CEI Part II (Section A of Subject 347—Communication Engineering.)

(*Professor Brown is Head of the Department of Electrical Engineering, Imperial College, London.*)

Principles of Heavy Current Engineering

115 pp. £1·65.*

CONTENTS: Electric and magnetic fields. Electrical machines. Power networks. Ionized gases. Three-phase circuits and systems.

From Circuits to Computers

184 pp. £2·50.*

CONTENTS: Passive circuits. Low frequency amplifiers and oscillators. Radio. Television. Digital computers. Analogue computers.

Modern Physical Electronics

213 pp. £2·95.*

CONTENTS: Vacuum tubes. Electron optics. Microwave tubes. Electrons and holes in solids. Semiconductor devices. Semiconductor technology and microelectronics. Masers and lasers. Superconducting devices. Electron microscopes. Plasmas. Particle accelerators.

Microwaves, Communications and Radar

190 pp. £2·50.*

CONTENTS: Microwaves. Aerials. Communication theory. Noise. Communication systems. Radar.

L. SOLYMAR (Editor). Chapman & Hall, London 1974. 24·5 × 19 cm.

This series of books is intended to inform or 'up-date' the non-specialist.

(*Dr. Solymar is Lecturer in Engineering Science at the University of Oxford, and Tutor in Engineering Science at Brasenose College.*)

Synthesis of Planar Antenna Sources

D. R. RHODES. Clarendon Press: Oxford University Press, Oxford 1974. 24 × 16 cm. 210 pp. £8·50.

CONTENTS: Physical nature of antenna synthesis. Fields of planar sources. The fundamental principle of planar sources. Rectangular and circular sources. Strip and line sources. Sampling synthesis. Maximum resolution. Maximum directivity. Minimum pattern-shaping error.

A new and thorough approach to the subject, parts of which have not been published previously.

(*Professor Rhodes is at the North Carolina State University.*)

First-Year Technician Mathematics

RHYS LEWIS. Macmillan, London 1974. 23 × 15·25 cm. 207 pp. £1·95.*

CONTENTS: Arithmetic. Aids to calculation. Formulae and equations. Graphs. Geometry. Trigonometry.

(*Mr. Lewis is a Senior Lecturer at Openshaw Technical College, Manchester.*)

The Radio Amateur's Handbook

Headquarters Staff. American Radio Relay League, Connecticut U.S.A. 1975. 24 × 16·5 cm. 704 pp. £2·90 limp.

CONTENTS: Amateur radio. Electrical laws and circuits. Vacuum-tube principles. Semiconductor devices. AC-operated power supplies. HF transmitting. VHF and UHF transmitting. Receiving systems. VHF and UHF receiving techniques. Mobile and portable/emergency equipment and practices. Code transmission. Amplitude modulation and double-sideband phone. Single-sideband transmission. Frequency modulation and repeaters. Specialized communications systems. Interference with other services. Test equipment and measurements. Construction practices and data tables. Wave propagation. Transmission lines. HF antennas. VHF and UHF antennas. Assembling a station. Operating a station. Vacuum tubes and semiconductors.

The Audio Handbook

GORDON J. KING. Newnes-Butterworths, London 1975. 25·5 × 16 cm. 286 pp. £4·90.*

CONTENTS: Audio fundamentals. Requirements for hi-fi. Preamplifier and control circuits. Power amplifiers and power supplies. Adjustments and measurements in amplifiers. Loudspeakers and headphones. Disc recording. Disc reproduction. Microphones and mixers. Tape recording. F.m. radio. Surround sound and four-channel systems.

Intended for the amateur enthusiast.

(*Mr. King is a Consultant.*)

110 Operational Amplifier Projects for the Home Constructor

R. M. MARSTON. Newnes-Butterworths, London 1975. 22·5 × 14·5 cm. 123 pp. £2·80.*

CONTENTS: Basic principles and applications. 25 a.c. and d.c. amplifier projects. 25 instrumentation projects. 20 oscillator and multivibrator projects. 20 sound generator and alarm projects. 20 relay-driving switching projects.

Despite its title, the non-specialist engineer could find this book of use.

(*Mr. Marston is a free-lance technical author and design engineer.*)

Radio Servicing Pocket Book

VIVIAN CAPEL. Newnes-Butterworths, London 1975. 19·25 × 12·5 cm. 230 pp. £1·95.*

CONTENTS: Modern radio components. Valve receivers. Modern transistor receivers. F.M. receivers. Stereo broadcasting. Car radios. Radio aerials. Interference. Setting up the workshop. Workshop equipment. Workshop techniques. Fault diagnosis. Receiver alignment. Useful data. Directory of radio manufacturers and service depots.

A practical book for the radio servicing technician.

(*Mr. Capel is a freelance technical author.*)

Delta Modulation Systems

R. STEELE. Pentech Press, London 1975. 22·2 × 14·3 cm. 382 pp. £10·00.

CONTENTS: Linear delta modulation. Double integration and exponential delta modulation. Calculation of quantization noise. Slope overload noise in linear d.m. systems. Idle channel noise and transmission errors in linear d.m. systems. Asynchronous delta modulation systems. Syllabically companded delta modulation. Instantaneously companded delta modulation systems. Delta and pulse code modulation. Encoders with multi-level quantizers. Delta modulation digital filters. Instrumentation using d.m.

Introduces the basic delta modulation system in a descriptive way before a mathematical analysis is presented. The more complex delta modulation systems used in the transmission of speech are subsequently described, after which a review of instantaneously adaptive delta modu-

lation systems is made. It is then shown how uniform and logarithmic pulse code modulation can be produced from delta modulation systems, and comparisons are made between the performance of p.c.m. and delta modulation. Multi-level delta modulation, which is a form of differential p.c.m., is also investigated. Directed to practising engineers and research workers in the fields of telecommunications and instrumentation although it will also be of value for advanced undergraduate and postgraduate courses in these subjects.

(*Dr. Steele is a Senior Lecturer in the Department of Electronic and Electrical Engineering at Loughborough University.*)

Talking Back—Citizen Feedback and Cable Technology.

I. DE S. POOL (Editor). MIT Press, Cambridge, Mass. 1974. 26 × 18·5 cm. 325 pp. £4·50.

CONTENTS: What cable can bring. Technologies. Two-way communication.

A collection of papers by US specialists on CATV and its applications and implications.

(*Professor Pool is in the Department of Political Science at the Massachusetts Institute of Technology.*)

Computer Techniques for Electromagnetics

R. MITTRA (Editor). Pergamon Press, Oxford 1973. 25·5 × 18 cm. 403 pp. £10·00.

CONTENTS: Wire antennas. Numerical solution of electromagnetic scattering problems. Integral equation solutions of three-dimensional scattering problems. Variational and iterative methods for wave-guides and arrays. Some numerically efficient methods. Inverse scattering and remote probing.

A detailed monograph for research workers concerned with aerials and similar problems.

(*Dr. Mittra is with the University of Illinois.*)

Butterworth and Chebyshev Digital Filters

R. GENESIO *et al.* Elsevier Scientific Publishing Co., Amsterdam 1973. 17 × 25 cm. 624 pp. £16·50.

CONTENTS: Z-transform. Difference equations. Butterworth and Chebyshev digital filters. Use of the tables. Highpass, bandpass and bandstop filters. Examples. Optimization of fixed-point implementations.

(*The author and his colleagues are with the Politecnico di Torino, Turin, Italy.*)

Electronic and Switching Circuits

S. M. BOZIC, R. M. H. C. CHENG and J. D. PARSONS. Edward Arnold, London 1975. 22·5 × 15 cm. 380 pp. £10·00 hardback, £3·95 limp.

CONTENTS: Physical electronics. Principles of amplification. Switching devices. Design of switching circuits. Amplifiers and their applications. Oscillators. Power supplies. Data processing and transmission. Industrial application of switching circuits. Electronic instrumentation.

Based on a lecture course for undergraduate students in the Department of Mechanical Engineering at Birmingham University.

(*Dr. S. M. Bozic and Mr. J. D. Parsons (Member 1968) are with the Department of Electronic and Electrical Engineering, University of Birmingham. Dr. Cheng is Associate Professor in Engineering, Sir George Williams University, Montreal.*

A New Concept of the Differential and Integral Calculus

K. PHILLIPS. Abbey Dene Publications, London 1974. 21 × 14·5 cm 19 pp. 30p.

CONTENTS: The differential calculus. The integral calculus.

(*Mr. Phillips (Member 1968) is a Consultant Engineer in London.*)

Vibration Analysis for Electronic Equipment

D. S. STEINBERG. Wiley-Interscience, New York 1973. 23·5 × 15·5 cm. 467 pp. £12·50.*

CONTENTS: Introduction. Vibrations of simple systems. Lumped-mass systems. Beams and suspended electronic components. Electronic components, frames and rings. Printed-circuit boards and flat plates. Electronic boxes. Mathematical models. Vibration fixtures and vibration testing. Structural fatigue.

Deals with a subject which is not widely documented, and will be useful to practising design engineers.

(*Mr. Steinberg is a consulting engineer to major US aircraft and electronics companies.*)

Electronic Engineering (third edition).

C. L. ALLEY and K. W. ATWOOD. Wiley, New York 1973. 23·25 × 16 cm. 838 pp. £7·95.*

CONTENTS: Semiconductors. Diodes. Common-base transistor amplifiers. Common-emitter amplifiers. High input impedance circuits and devices. RC-coupled amplifiers. Transformer-coupled amplifiers. Small-signal tuned amplifiers. Direct-coupled amplifiers. Multistage amplifiers. Amplifier noise. Negative feedback. Linear integrated circuits. Active filters. Power supplies. Large-signal tuned amplifiers. Oscillator circuits. Amplitude modulation and detection. Frequency modulation. Switching and pulse circuits. Digital integrated circuits.

A comprehensive treatment for degree students.

(*The authors are with the Electrical Engineering Department of the University of Utah.*)

Systems Documentation

F. WHITEHOUSE. Business Books Limited, London 1973. 24 × 16 cm. 191 pp. £4·50.

CONTENTS: Organisational behaviour. The creative organisation. Rules, commands and practices. Systems, procedures and methods. Penetrating the psychological barriers. The basic assumption. The requirement. An appraisal of methods. The slimline system. Computer systems documentation. The atomic procedures. Dealing with forms. The procedure molecule. The communication meeting. In-house typesetting and printing. Distribution on demand.

Subtitled 'Techniques of persuasion in large organizations', the book deals with a system of project management.

(*Mr. Whitehouse is with the Engineering Management Systems team of the Guided Weapons Division of the British Aircraft Corporation.*)

Rapid Servicing of Transistor Equipment

G. J. KING. Newnes-Butterworths, London 1973. 21·5 × 14 cm. 171 pp. £1·90.*

CONTENTS: Transistor fundamentals. Preliminary circuit and transistor tests. Signal conditions and tests. Fault-finding in audio and video curcuits. Fault-finding in R.F. circuits. Fault-finding in oscillator stages. Fault-finding in transistor radios and hi-fi amplifiers. Practice of transistor equipment servicing.

For the servicing technician, the student or the amateur.

(*Mr. King is a Consultant.*)

Materials and Processes for Electrical Technicians

L. C. MOTT. Oxford University Press, London 1974. 23·5 × 15·5 cm. 169 pp. £5·00 hardback. £1·95 limp.

CONTENTS: Properties of materials. Production and properties of cast iron. Production and properties of steel. Heat treatment of carbon steel. Copper and copper alloys. Aluminium and aluminium alloys. Magnetic materials. Conducting materials. Electrical resistance materials. Bimetals and thermocouple materials. Electrical insulating materials. Transformers, resistors and capacitors. Cables, lines and supports. Foundry processes. Forging. Rolling. Drawing and extrusion. Pressing and press tools. Solders and soldering. Brazing and welding. Bench work. The drilling machine. Taps and dies. The lathe. Cutting tools and lubricants.

Specifically aimed at the Materials and Processes section of C & G Course 281.

(*Mr. Mott is Senior Lecturer at the School of Electrical and Mechanical Engineering, Bordon, Hampshire.*)

Receiving PAL Colour Television

A. G. PRIESTLEY. Fountain Press, Hemel Hempstead 1974. 22·5 × 14·5 cm. 261 pp. £5·00.

CONTENTS: The origin of the PAL system. The transmitted PAL system. Colour display tubes. Decoding PAL. The complete PAL decoder. Colour display adjustments. The colour receiver. Further aspects of the PAL system. Servicing colour receivers.

An introduction for those concerned primarily with receiver techniques.

(*Mr. Priestley has spent many years in the TV design department of Philips Electrical Ltd.*)

A First Course in Applied Electronics

W. GOSLING. Macmillan, London 1975. 21·5 × 13·5 cm. 162 pp. £2·95 limp.*

CONTENTS: Introduction to electronics. Fundamental principles of amplification. More about amplifiers. Unwanted outputs. Feedback. Feedback in practice. Feedback problems. Integrated amplifiers. Some practical examples.

An introduction mainly based on microelectronics techniques for the first year undergraduate.

(*Professor W. Gosling (Fellow 1968) occupies the Chair in Electronic Engineering at the University of Bath.*)

Mechanical Survival: The Use of Reliability Data

J. H. BOMPAS-SMITH. Editor: R. H. W. BROOK. McGraw-Hill, Maidenhead, Berkshire 1973. 23·5 × 15·5 cm. 199 pp. £4·95.*

CONTENTS: Putting values to reliability. Mortality curves—uses and construction. The special case of constant local failure rate. The theory of failures. The case of increasing failure rate with time when the duty is constant: the normal and log normal distributions. The Weibull, binomial, and Poisson distributions: confidence levels. The initial strength and failure distributions of parts under constant duty: the extreme-value and log extreme-value distributions. Some further considerations regarding distributions of fatigue-test results and minimum fatigue life. The form of the duty distribution. The case where both strength and duty are variables. The effect of 'weak spots'. Mixed distributions. Degradation and replacement curves. The 2-distribution, tests for frequency, confidence limits for MTBF. Simple systems, multiple items, and the effect of maintenance on their reliability. Making the best use of early-failure experience. Pointers from one, two, or three failures. Is reliability a saleable commodity ?

Intended primarily for Q and R, and production engineers.

(*The late Mr. Bompas-Smith was Staff Reliability Engineer with Rolls-Royce.*)