FOUNDED 1925
INCORPORATED BY
ROYAL CHARTER 1961

"To promote the advancement of radio, electronics and kindred subjects by the exchange of information in these branches of engineering."

THE
RADIO AND ELECTRONIC
ENGINEER

The Journal of the Institution of Electronic and Radio Engineers

VOLUME 39 No. 6 JUNE 1970

A Government Corporation for R & D?

THE increasing activity of Government laboratories in Great Britain, an evolving process starting with the inauguration of the National Physical Laboratory at the beginning of the century, continuing with the formation of the Department of Scientific and Industrial Research in 1916 and now strengthened by the emergence of the Ministry of Technology in 1965, is an accepted part of the industrial life of this country. Earlier this year a 'Green Paper' was published by the Minister of Technology which puts forward proposals, to be regarded at this stage as providing the basis for public debate, for reorganizing industrial research and development in Government laboratories.*

The essential feature of the proposals is that a 'British Research and Development Corporation' (B.R.D.C.) should be formed with the following aims and functions:

(i) to encourage and support the development and application of innovation and technological improvement in industry for the benefit of the U.K. economy; and to carry out research and development for this purpose, both itself and in collaboration with industry and on repayment;

(ii) to carry out research programmes necessary in the public interest, including basic research, and other specific programmes of work required by Government departments and other public authorities;

(iii) to exploit where appropriate innovations resulting from Government financed programmes carried out by other agencies.

The B.R.D.C. would comprise the Ministry of Technology's industrial research establishments (N.P.L. and N.E.L., for instance), the Research Group and Reactor Group Establishments of the Atomic Energy Authority, and the National Research Development Corporation (N.R.D.C.). These organizations at present employ 4750 professional staff and their gross annual cost, including capital expenditure, is about £70 M.

The reasons for making these proposals for reorganization are the changes which are to be made in the structure of the A.E.A. which is shortly to have its production side turned into two separate companies, nuclear fuel and radiochemicals respectively, and the development of work for industry in the Ministry of Technology's own organization. It is felt to be desirable to bring all these activities under the same management régime rather than to contrive rationalization procedures between dissimilarly-organized bodies. The 'Green Paper' states that non-nuclear work which the A.E.A. does for industry cannot be easily divorced from its nuclear activities and it straightaway rejects the idea that the new organization should be within the Civil Service—it would have greater flexibility and 'customer' awareness if it were to be set up as a statutory corporation.

It is pointed out that the very considerable involvement of the Ministry's research and development in aerospace work is bound too closely to defence programmes, despite the growing amount of civil applications arising out of defence, for this to be associated with the proposed corporation. This is perhaps easy to appreciate but it is not immediately apparent why the cooperative industrial Research Associations should remain under the Ministry of Technology for allocation of Government support. Other problems which the reorganization will present include separation of the non-nuclear work and nuclear reactor programme work being undertaken by the Atomic Weapons Research Establishment; the defence side could logically go to the Ministry of Defence or the Ministry of Technology.

As electronic engineers we naturally look at this proposed reorganization from our own standpoint. The A.E.A. Reactor and Research Groups both carry out considerable work in the control and instrumentation fields and the National Physical Laboratory and the National Engineering Laboratory also have sizeable commitments in electronics. The N.R.D.C. employs an unknown but presumably large part of its 100 professional staff on work connected with electronics research and development in Government establishments, the universities and industry, and here the 'input' may sometimes be unconnected with other work of the B.R.D.C.

It is, however, useful to have proposals such as the 'Green Paper' gives aired before the Government takes action, as these are all matters of considerable importance to industry. The B.R.D.C. is envisaged as exploiting inventions made by other bodies, government establishments and universities in the main—the present N.R.D.C. role—and also as working for industry on a contractual basis. The goodwill of industry is obviously essential if a new organization is to succeed.

F.W.S.

* 'Industrial Research and Development in Government Laboratories—A New Organization for the Seventies'. H.M.S.O. 1970. Price 2s. 6d.

INSTITUTION NOTICES

A Report from Canada

At the last Annual General Meeting of the Ottawa Section the following Committee was elected:

Chairman:	R. W. Wray (Fellow)
Vice-Chairman:	R. F. Brett (Fellow)
Secretary:	T. Curtis (Graduate)
Treasurer:	Capt. P. Coderre (Member)
Program Convenor:	B. M. Davies (Graduate)
Co-convenor:	C. West (Graduate)
Membership Secretary:	N. MacFarlane (Member)
and	Capt. R. G. Dreyer, R.N. (Retd.) (Fellow)
	G. W. Sparks (Fellow)
	G. D. Seabrook (Member)

A number of technical meetings have been held at which prominent Canadian Engineers and Scientists presented papers. On 25th February 1970, Mr. Robert Hoge, Vice-President of Engineering, Computing Devices of Canada, presented his second paper to an Ottawa Section meeting. Mr. Hoge's first paper was published in the Institution's *Journal* of January 1970.

A number of technical visits have been arranged including one to see the facilities of The Skyline Cablevision Company and, recently, one to the Northern Electric Company's Laboratories to see the SPI Electronic Switching System which was preceded by a talk on the system.

Many Ottawa members of the Institution have been registered as Professional Engineers by the Association of Professional Engineers of Ontario following the successful negotiations initiated by Mr. Graham D. Clifford, Director and Secretary of the Institution, during his visit to Canada in April 1966.

The continued enthusiasm of the members in the Ottawa area and the high quality of the meetings bode well for the Institution's future activities in Ottawa.

Conference on Centralized Control Systems

An International Conference on Centralized Control Systems will be held at the Institution of Electrical Engineers, Savoy Place, London W.C.2, from 28th September to 1st October 1971. It is being organized by the I.E.E. Power and Control and Automation Divisions in association with the Institution of Electronic and Radio Engineers.

This Conference is intended to be of interest to those responsible for centralized control of the distribution of energy, fuel, water etc. The central theme will be the design and operation of alarm systems, remote control, signalling and telemetry including special problems arising from the use of radio and line channels, and it is intended that a session will be devoted to control room organization and philosophy.

It is proposed that the scope of the Conference will include the following main items:

Choice of system control; Facilities; Presentation; Basic designs of centralized control systems; Components; Bearer circuits and communication paths; Commissioning and maintenance; Evaluation of equipment.

Offers of contributions to the conference programme are invited and intending authors should submit a 250-word synopsis to the I.E.E. Conference Department by 5th October 1970.

Further details and registration forms will be available in due course from the Manager, Conference Department, I.E.E., Savoy Place, London WC2R 0BL.

Institution Ties

Members are asked to note that, with effect from 1st July 1970, the prices of Institution ties will be:

Terylene (navy-blue or wine background)	20s. post free
Silk (navy-blue background only)	30s. post free

It is regretted that these increased prices have been made inevitable through increases in the costs of weaving charged to the manufacturer.

Wearing of the Institution tie is, of course, restricted to members; these ties are obtainable only from the Institution at 9 Bedford Square, London, WC1B 3RG. Orders by post should include remittances.

Engineering Congress in Israel

The Second World Congress of Engineers and Architects in Israel will be held in Tel Aviv from 14th to 18th December 1970. The main theme of the Congress will be 'Dialogue in Development —Integration of Interdisciplinary Planning and Its Implementation in Development Work', and it will be covered in a series of plenary and group discussion sessions. Aspects to be covered include 'Scientific Research and Technological Development for Industry' and this and the Panels devoted to Education and Technical Training will be of special interest to the Members of the I.E.R.E. Members of the Institution have been invited by the organizers to participate in the Congress and offers of papers and requests for further information should be addressed to: Congress Secretariat, 200 Dizengoff St., P.O.B. 3082, Tel Aviv, Israel.

A comprehensive series of professional post-congress tours has been arranged, including a visit to Technion, the Israel Institute of Technology, at Haifa.

U.D.C. 621.396.963

Digital Control for Primary Radar Systems

By

H. GILES,
C.Eng., M.I.E.E.†

Presented at a meeting of the East Anglian Section of the Institution in Cambridge on 13th November 1969.

An investigation into the use of digital logic techniques for simple pulse-modulated radar systems resulted in their application to provide the necessary controlling and timing waveforms for a display. The paper describes a conventional analogue display and its digital counterpart and compares both systems. Results for the performance of a logic system are given.

List of Symbols

d	c.r.t. spot diameter
f	control waveform frequency
f_c	calibrator oscillator waveform
f_r	transmission pulse repetition frequency
f_0	clock waveform frequency
r	range scale
r_{max}	maximum radar range
r_{min}	minimum range discrimination
t_b	bearing marker pulse duration
t_c	range marker pulse duration
t_p	transmission pulse duration
t_s	time-base scan period
c	transmission velocity
D	c.r.t. diameter
I_y	deflector coil current
N	c.r.t. resolution number
S	aerial turning speed
T	duration of the radar cycle
T_c	interval between fixed markers
T_s	divide-by-six interval
U	radar reflection interval
V_f	time-base feedback voltage
V_r	time-base ramp voltage
V_t	time-base reset voltage

1. Introduction

A pulse-modulated primary radar system requires a number of controlling electrical waveforms to determine the timing of the different functions. Most of these must change with the range displayed.

In conventional systems, pulse durations and repetition rates are usually determined by a number of individual circuits, each being selected by the range-change switch and many having separate pre-set controls for each range in use. A complex system of switched circuits results, which normally requires setting-up adjustments to be made to a number of controls for each range scale. These are time-consuming operations, they require external calibrating equipment, and are subject to inaccuracy and drift.

The growth of digital computer techniques and the resulting development of microelectronic elements led to the concept of a system of digital logic capable of determining all the functional pulses required for a pulse-modulated radar with a minimum of manual switching and no setting-up adjustments. Extreme accuracy of timing can be provided by driving the system from a crystal-controlled oscillator, with drift lower by several orders of magnitude than that of conventional systems.

2. Design Objectives

The first consideration is the design objective. For this particular case, it is the application of digital logic techniques to an equipment which provides an indication and means for measuring, relative to its own position, the position of other objects.

A marine radar is such an equipment. Figure 1 illustrates the information presented at the plan position indicator of a typical marine radar display unit which has embodied the following features:

A cathode-ray tube incorporating a long persistence phosphor at its screen.

A range scan or time-base describing a radial line which rotates synchronously with the radar aerial system, about its origin.

The c.r.t. is intensity-modulated by marker pulses and signals reflected from objects and because of its long persistence screen, their luminance remains sensibly constant per revolution of the time-base.

Range marker pulses are timed to modulate the c.r.t. beam current at regular intervals along the time-base and therefore appear as a series of concentric rings.

The bearing marker is formed by a train of square waves timed to modulate the c.r.t. during a time-base period at any given position in azimuth.

The full line at the 12 o'clock position is produced by a single modulating pulse lasting at least one

† Plessey Radar Ltd., Cowes, Isle of Wight.

time-base period. Its purpose is to indicate some bearing datum such as ship's head or magnetic north. As this pulse is derived from the aerial turning mechanism, it will also indicate whether the rotation of aerial and time-base are locked in frequency and phase.

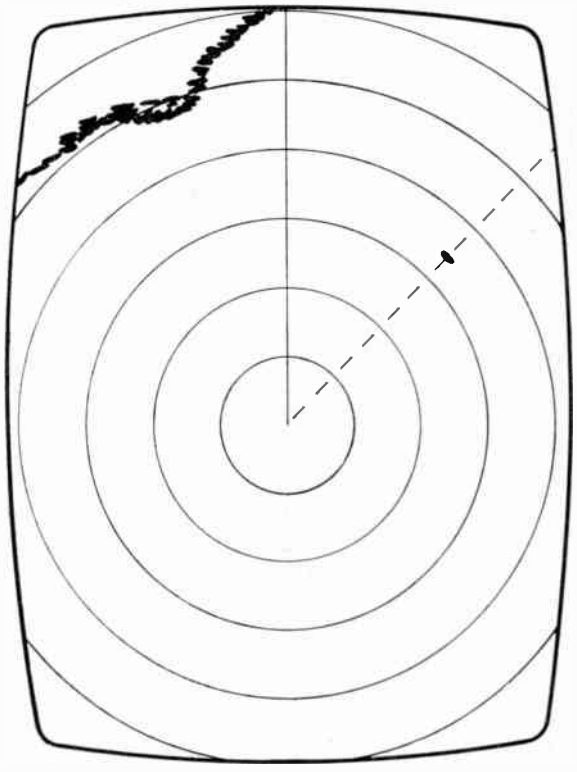


Fig. 1. Plan position indicator type display.

Pulses of r.f. energy are transmitted from the aerial system in synchronism with the commencement of each time-base. Reflected pulse signals from surface objects and coast lines are received by the aerial system and are processed to appear as a discrete dot or form of mosaic of dots, depending on the nature and reflexion coefficient of the object. The reflected signal appears at a position along the time-base from the origin which is proportional to the range of the corresponding object.

The range of the object is determined by the position of its reflected signal or echo, relative to the nearest range marker ring. Its corresponding bearing is determined by placing the dotted marker line over the echo and reading off bearing on a scale provided.

The essential functions of a typical marine radar display unit and their complementary waveforms, as set out above, are shown in their idealized form in Fig. 2, together with their identifying symbols by which they are termed in later arguments.

At this particular stage only the lower section of Fig. 2 is applicable. The columns at the left- and right-hand side show that the waveforms and corresponding terminology are equally applicable to analogue and digital systems.

The next consideration is the prescribed operational and performance requirements for the radar. From

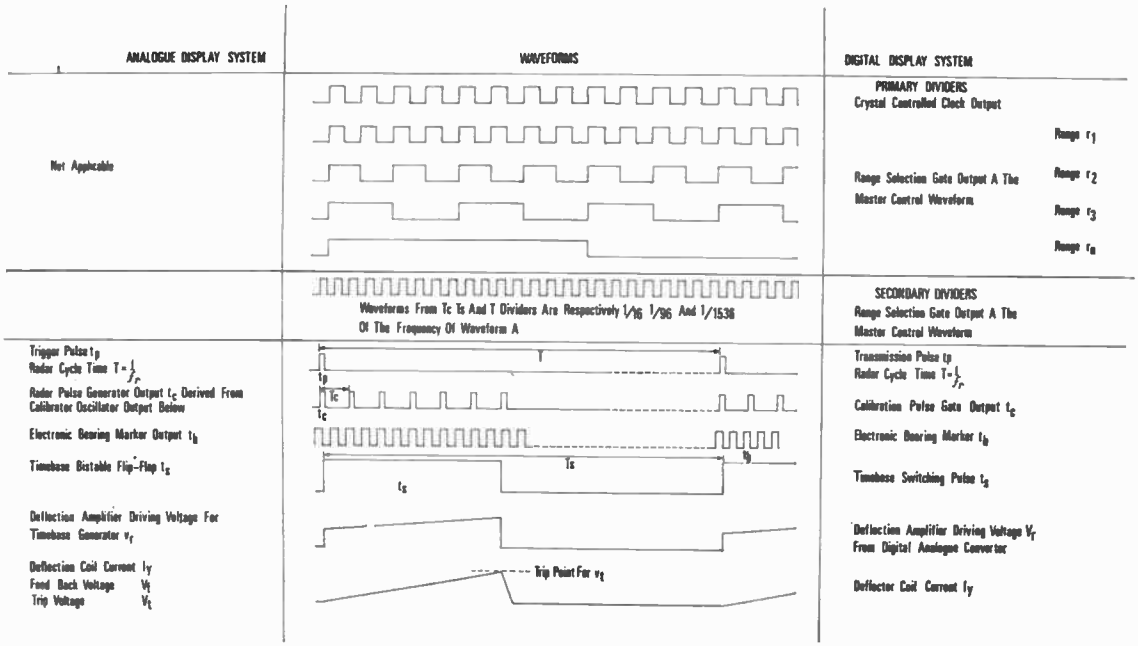


Fig. 2. Waveforms.

Table 1. Principal parameters and their relationships

Item	Parameter	Related to or limit	Relationship and limitation	Remarks
1	t_p	minimum		determined by magnetron
2	t_p	maximum		determined by magnetron
3	t_p	f_r	$t_p.f_r \leq$ duty ratio	limited by magnetron
4	t_p	f_r	$t_p.f_r =$ constant	for constant mean power
5	t_p	c.r.t. spot diameter, d	spot length $= \frac{Dt_p}{2t_s} \geq d$	limit of resolution
6	t_p	min. range discrimination r_{min}	$r_{min} = \frac{t_p}{U}$	for coincidence of echo start with end of t_p
7	f_r	t_p		see above
8	f_r	max. range r_{max}	$f_r \leq \frac{1}{Ur_{max}}$	second trace echoes
9	f_r	aerial turning speed S (rev/min)	$f_r \geq \frac{\pi DS}{60d} \geq \frac{\pi NS}{60}$	to avoid gaps between scans on periphery of cathode-ray tube
10	t_o	T_o	$\frac{T_o}{t_o} =$ constant	for constant spacing of range rings on display
11	T_o	t_p	$t_o \leq t_p$	to avoid obscuring targets
12	t_s	range	$t_s = rU$	
13	U	velocity of radiation c	$U = \frac{2}{c}$	definition

these can be determined the transmitted pulse duration and repetition rates for the specified range scales of view. For each range provision is made for a scanning waveform for the time-base, and the requisite marker pulses for range and bearing measurement.

3. Elements of a Digital Display System

The picture resolution of a typical radar cathode-ray tube is normally better than 300 spot diameters per effective radius. However, conventional pulsed radar displays seldom achieve this degree of resolution for range scales below two miles and normally exceed the optimum value at range scales about twelve miles.

Constant picture resolution for all range scales is obviously desirable. The retention of suitable long range resolution at short range will satisfy the performance requirements for minimum range detection and adjacent target resolution.

For the ideal case it is also desirable to maintain other facilities constant when the range scale is changed, for example, picture brilliance level, the number and position of fixed range markers, and the apparent mark/space ratio of a dotted bearing marker. However, the probability of target detection can improve if certain parameters increase with the range scale of view and, conversely, others decrease. For this case, the duration of the transmission pulse should increase with range scale, but for optimization, the receiver bandwidth should decrease proportionally, Furthermore, the mean supply and transmitted powers remain constant if the ratio of the transmission pulse repetition frequency is inversely proportional to the change of transmission pulse duration (i.e. constant duty ratio).

Unfortunately, the advantages of the ideal system are seldom realizable and some compromise results if the scaling factor for minimum to maximum ranges of view, when applied to transmission pulse and repetition frequency parameters, exceeds the magnetron duty cycle. However, this may not be the only limiting factor and Table 1 shows the relationship and limitations of the principal radar parameters.

Items 1 and 2 show that the minimum and maximum transmission pulse durations are determined by the magnetron characteristics.

Likewise, items 3 and 4 show that the product of transmission pulse duration and repetition frequency is limited by the magnetron duty ratio. However, this product should have as high a value as possible and remain constant at all range scales for optimum detection.

Item 5 indicates that optical resolution is determined by the number of spot diameters per effective radius of the c.r.t. and is denoted by the symbol N. For optimum radar resolution the transmission pulse duration should be comparable to the spot diameter.

Item 6 shows that minimum range discrimination is given by the equivalent radar range for the duration of transmission pulse.

In item 8 the maximum repetition frequency is inversely proportional to the radar ranging interval for the most distant target to be seen. If repetition period exceeds this timing interval second trace echoes will appear.

Item 9 indicates that the minimum repetition frequency is dependent on the aerial turning speed and c.r.t. spot diameter. If repetition frequency is less than the possible radial resolution, picture spoking occurs.

Item 10 requires that the duration of range marker pulses and the interval between them should be constant for constant ranging accuracy.

Item 11 shows that the duration of range marker pulse should be not greater than that of transmission pulse so as not to obscure echoes.

Finally, for Item 12 the duration of the time-base is proportional to the radar ranging interval for the required range scale of view.

To achieve the desired facilities and performance a digital logic system is postulated in preference to the circuit complexity required for a conventional analogue display. However, valid limitations still apply. These will be considered after the basic principles of a digital system have been explained.

4. Review of Requirements

Recapitulating requirements for a typical pulsed radar system the following basic waveforms are necessary for its operation:

(a) A transmitter control pulse, recurring at a frequency, f_r.

(b) A time-base switching pulse, whose duration is proportional to the range scale of view, i.e. range 1 to nth range as selected by the range switch.

(c) A means of determining the rate of rise of the scan current appropriate to the range in view.

(d) A cathode-ray tube brightening or signal switching pulse which enables received signals and markers to be displayed only during the time-base forward stroke.

(e) Fixed, accurate marker pulses, spaced at intervals appropriate to the range in view, to provide a visible range measuring scale.

Additionally in certain cases the system may require:

(f) A bearing reference pulse to indicate some bearing datum such as ship's head or magnetic north.

(g) A bearing marker pulse or pulses, distinguishable from the bearing reference pulse, to indicate the bearing of any chosen target.

It is shown that the output from a master oscillator, suitably formed into a square wave and scaled as required by a combination of bistable dividers and single-state recognition gates, may be used to provide the required waveforms and functions for a pulsed radar system. Such a system reduces the number of adjustments necessary to secure accuracy.

5. Description of Basic System (Fig. 3)

The output from the master oscillator is formed into a square waveform in the clock pulse generator, at frequency f_0 and applied to a bank of primary dividers $d_1 \ldots d_n$, each producing a square waveform similar to that of the clock pulse generator, but reduced in frequency by the division applied. The output from the clock pulse generator or from any of the primary dividers is selected by means of AND gates, the range selection gates, controlled by the range switch, $r_1 r_n$, to provide a control waveform appropriate to the range scale required, at point A.

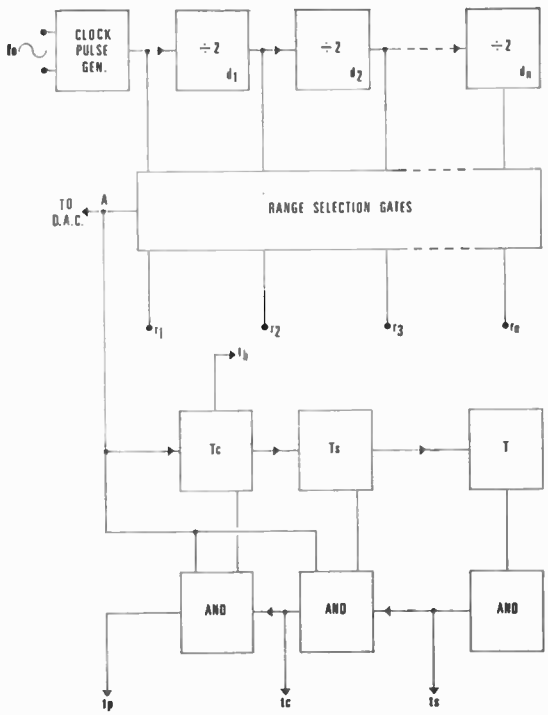


Fig. 3. Schematic diagram of basic digital display unit.

Division ratios of 2 are used throughout, corresponding to range ratios of 2, but other integral ratios or combinations of ratios may equally be adopted. Since the output waveform from each divider stage is identical with f_0 except in frequency, a simple 'ripple through' dividing system may be used.

The selected control waveform at point A is further scaled by secondary dividers, T_c, T_s and T which, in conjunction with suitable single-state recognition gates, provide the special pulses at predetermined intervals required by a radar system. The waveform at this point may also be applied to a digital/analogue converter, which provides the time-base waveform.

The first of the secondary divider stages provides the range calibration marker interval from which, by means of a suitable coincidence gate, 'unit' calibration marker pulses are derived. In this case a 'unit' pulse is defined as one half-cycle of the control waveform.

The second stage of division, T_s, determines the time-base duration corresponding to a fixed number of range marker pulses, and, in conjunction with suitable gates, produces either one pulse of the required length or initiating and terminating pulses from which a long pulse may be derived for time-base gating.

The long pulse so formed also provides cathode-ray tube brightening (or signal gating) during time-base scan.

The final stage of division T determines the duration of the complete radar cycle, the recommencement of other functions, and, by a coincidence gate, the generation of one 'unit' pulse, t_p, for modulator control.

At each coincidence or single-state recognition gate a unique state exists at a predetermined number of control waveform cycles from the commencement of each radar cycle or at predetermined intervals thereafter.

A square waveform electronic bearing marker, t_b, is derived from one of the secondary divider stages and requires no gating. This remains locked to scan and its frequency is directly proportional to that of the control waveform.

The scanning waveform to provide a time-base may be derived by digital/analogue conversion of the waveform at the output of the primary dividers, (point A), or by gating a more conventional form of ramp generator with the waveform at the t_s terminal. The former can be of the pulse counting type of digital/analogue convertor, either by current integration from sequentially opened gates, or a linearized voltage pulse step integrator, where at any instant, output amplitude is proportional to the number of master control waveform cycles from the commencement of the radar cycle.

5.1 *Salient Features of the Digital System*

The system offers, quite automatically, a number of advantages, some of which cannot be obtained at all with analogue radar systems and others that can only be approached with considerable expense and difficulty. These may be summarized briefly as follows:

(a) All functions follow automatically from the selection of the control waveform.

(b) Range selection requires only d.c. switching.

(c) Control of basic scale, for example, nautical miles or kilometres, rests in selection of master oscillator frequency.

(d) Optimum radar resolution, with respect to the number of 'unit' pulses per corresponding time-base duration, may be selected by suitable choice of the master frequency.

(e) Since the 'unit' pulse provides both the modulator pulse length and the calibration pulses, these are equal and remain proportional to the selected range scale, yielding a constant-resolution display.

(f) Time-base duration varies inversely with recurrence frequency resulting in a display of constant brilliance.

(g) The transmission pulse duration varies inversely with recurrence frequency, resulting in constant mean transmitted power.

(h) The number of calibration pulses is constant on all ranges.

(i) Neglecting logic propagation delays which are small, calibration pulse spacing accuracies are equal on all ranges.

(j) Pulse spacing accuracy is determined by the master oscillator which may be designed for a very high degree of stability and accuracy.

5.2 *Limitations Imposed by Practical Considerations*

Certain fundamental factors and the limitations of radar components prevent the full exploitation of all the advantages offered, and limited modifications must be provided in a practical system. It will be shown that the simplicity with which a typical modification may be made is also a feature of the system.

6. Design for Practical System

6.1 *Operational and Performance Requirements*

The following requirements were postulated for the design of an experimental logic display system for a

prototype radar:

(a) *Cathode-ray Tube Resolution*
The plan position indicator shall have an effective diameter of 300 mm and a spot size not greater than 0·5 mm diameter.

(b) *Scale of Display*
The equipment shall provide five scales of display whose ranges of view shall be ¾, 1½, 3, 6 and 12 nautical miles.†

(c) *Range and Bearing Markers*
Six fixed range rings shall be provided on each scale of display. An electronic bearing marker shall be provided and displayed in the form of a radial dotted line whose dot size shall be constant for any range scale of view.

(d) *Range Accuracy*
The fixed range rings shall enable the range of an object, whose echo lies on a range ring, to be measured with an error not exceeding 1% of the maximum range scale in use, or 50 yards, whichever is the greater.

(e) *Range Discrimination*
On the most open scale appropriate, the echoes of two corner reflectors, having an equivalent echoing area of 10 m^2, shall be displayed separate and distinct when the reflectors are on the same bearing 25 yards apart and at a range of ½ mile.

(f) *Minimum Range*
On the shortest range scale of view a corner reflector, having an equivalent echoing area of 10 m^2, placed 25 yards from the antenna, shall be displayed separate and distinct from the transmission pulse.

(g) *Climatic Performance*
The equipment shall perform within the limits prescribed, whilst operating in ambient temperatures ranging from −15°C to +55°C.

(h) *Other Desirable Features*
Display brilliance shall remain sensibly constant on all ranges, and burning of the c.r.t. centre shall be minimized by the elimination of the zero marker, and slight delay of the brightening pulse.
Some control of scan start relative to transmission is desirable.
Transmission pulse duration shall change in proportion to range scale in use.

(i) *Other Limiting Factors Applicable to Table 1*
Magnetron duty ratio—must not exceed 0·001.
Magnetron transmission pulse minimum—0·06 μs.
Magnetron transmission pulse maximum—1·0 μs.
Aerial rotation speed—25 rev/min limits minimum repetition frequency to 785 Hz.
Second trace echoes—for 12 miles range repetition frequency must not exceed 6750 Hz.

† 1 nautical mile (n.m.) = 1852 metres.

To summarize the salient requirements for a design basis, the system chosen is a radar having five range scales, successively increasing by a factor of two, six fixed range markers per scale and a minimum range resolution of 25 yards.

6.2. *Determination of Design Parameters*

The starting-point for optimum design is conditioned by a number of interrelated factors and constraints:

(a) The minimum duration for transmission pulse is controlled by the magnetron characteristics.

(b) For the shortest range scale, the maximum duration for transmission pulse is controlled by the 25 yards range resolution requirement (in respect of the equivalent radar range for the transmission pulse).

(c) The choice of transmission pulse determines the duration of a 'unit' logic pulse and for optimum display resolution its equivalent radar range should not be more than the equivalent radar range of the c.r.t. spot diameter.

(d) To derive the specified number of 6 range marker pulses one division by 6 is required. For simplicity, all other dividers should be binary. This requires that the total number of 'unit' pulse lengths per range scale be divisible by 6 and that the quotient be a binary number.

Combining these constraining factors, expressions may be derived to determine a suitable binary number. Thus, for range discrimination

$$2^n \geq \frac{r_1}{6r_{min}} \qquad \text{.....(1)}$$

while for the shortest permissible magnetron pulse

$$2^n \leq \frac{t_s}{6t_{p(min)}} \qquad \text{.....(2)}$$

where

r_1 = shortest range scale, 0·75 n.m. or 1518 yards approx.

r_{min} = minimum range discrimination, 25 yards.

t_s = shortest range scale period = $r_1 U$

$t_{p(min)}$ = minimum permitted transmission pulse duration = 0·06 μs

Table 2. Summary of design parameter values

No.	Range n.m.	Range t_s μs	Cal. interval n.m.	Cal. interval μs	'Unit' pulse t_p μs	Recurrence period T μs	Frequency Hz
r_1	0·75	9·271	0·125	1·5451	0·09657	148·336	6741
r_2	1·5	18·542	0·25	3·0902	0·19314	296·672	3370
r_3	3·0	37·084	0·5	6·18	0·38628	593·344	1685
r_4	6·0	74·17	1·0	12·36	0·77256	1186·688	842
r_5	12·0	148·34	2·0	24·72	1·54512	2373·376	421

U = radar reflexion interval, time taken to receive a reflection from a target at one nautical mile = 12·361 μs/n.m. = $2/c$

c = velocity of radiation, n.m./μs.

The limits set by equations (1) and (2) for the values given are approximately 10 and 26. The only binary number lying between these limits is 16, hence the number of 'unit' pulses lengths per scan interval is 96.

In respect of c.r.t. resolution

diameter $D = 300$ mm

spot size $d \leq 0{\cdot}5$ mm

spots per radius = $D/2d = 300$

no. of spots per 'unit' pulse = $300/96 \simeq 3$.

Thus, the 'unit' pulse is adequately resolved. Optimum parameter values may now be determined for the shortest range scale:

minimum range from equation (1)

$r_{min} = r_1/96 = 15{\cdot}8$ yards

transmission pulse duration from equation (2)

$t_p = t_s/96 = 0{\cdot}0965$ μs

fixed range marker pulse duration

$t_c = t_p$

'unit' pulse period of control waveform derived from clock pulse generator = $2t_p$.

Thus, clock pulse frequency

$f_0 = 1/2t_p = 5{\cdot}177$ MHz.

For other range scales, $r_2 = 1{\cdot}5$ n.m., $r_3 = 3{\cdot}0$ n.m. and $r_4 = 6{\cdot}0$ n.m., the frequency of the control waveform is divided by 2, 4 and 8 respectively by the primary dividers, and the duration for transmission pulse and range marker increases proportionately. Design limitations, considered later, preclude scaling r_5 in a similar manner.

The system resolution comprises 96 'unit' pulse lengths per range scale time-base period, corresponding to 48 'unit' pulse periods of the control waveform f, whose frequency is determined by range scale selection and the primary dividers. To provide the six range markers, the first stage of secondary dividers divides by 8 giving $f/8$. The total range interval is determined by the second stage of dividers providing a division by 6, giving $f/48$, that is, a full cycle of 96 'unit' pulses.

The radar was considered to have a maximum range of 12 n.m. The next transmission must not, therefore, occur before reflected signals at that range have been received. The distance of the shortest range scale divides into the maximum radar range 16 times. Hence a further division of 16 is required by the secondary dividers to determine a safe recurrence interval, corresponding to a frequency, $f_0/768$ which is equal to 6741 transmissions per second for the shortest range scale.

Thus, a system is defined for range 1, having the parameters tabulated in line 1 in Table 2. The remaining parameters for other ranges resulting solely from binary divisions of the control waveform are set out in the following lines.

The resulting values for range 5 fall outside the limiting values in two respects; (a) transmitted pulse length exceeds the maximum permitted for the magnetron by about 50% and (b) the repetition frequency falls below the bottom limit necessary to avoid 'spoking' of the display with an aerial rotation speed of 25 rev/min.

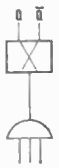
6.3. *Corrective Modifications to Logic Circuits*

It was considered that the simplest modification was that which retained all existing values for the first four ranges but retained the same repetition frequency and the same transmitted pulse length on ranges 4 and 5. In this way constancy of transmitted power was retained throughout, whilst both brightness and resolution improved on range 5.

7. Experimental Logic Units

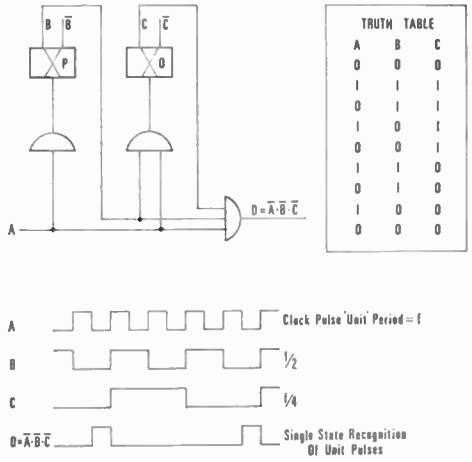
7.1. *Basic Logic Elements and their Application*

The type of logic and its processing arrangement to obtain the desired waveforms at the frequencies involved requires careful selection. All logic elements have some propagation delay and if a large number of such elements is cascaded, the delay build-up can be appreciable. In a divider containing many binary



(a) Basic counter element.

(b) NAND/NOR gate.



(c) Divide-by-4 parallel clocked counter and single state recognition.

Fig. 4. Basic logic elements and their application.

elements connected in cascade, a change of state will be propagated sequentially along the counter. If the outputs of such a counter were combined in a gate to produce a single wanted pulse, numerous spurious pulses would result and the wanted pulse might also be shortened owing to the cumulative delay in the system.

At high frequency clock pulse rates, the propagation delay times for 'ripple through' counter systems could be greater than the duration of the 'unit' pulse. Consequently, suitable alternatives were investigated for the proposed logic system.

The system ultimately employed is based on the counter element of the form shown in Fig. 4(a). This counter comprises a bistable element switched by a multi-input gate. For its operation positive logic is assumed, that is, 1 = positive line, 0 = earth. If the gate inputs are at the 0 state, the counter terminals Q and $\bar{Q}$ will change state if one of the gate inputs changes to a 1 state. Conversely, if any gate input is at 1, it is not possible to change the state of the counter by operating on the other inputs; thus, the counter is said to be inhibited.

A number of basic counters may be combined to form a parallel clocked counter of the type shown in Fig. 4(c). Here the clock pulse is connected to the input gates of all counters and the gate of each counter is conditioned by the states of all counters preceding it in the chain. Thus, the clock pulse can only change the state of a counter if the active terminals of all preceding counters stand at 0. The first counter in the chain is clocked directly by the clock pulse train and changes state for each clock pulse change from 0 to 1. The state of the second counter is changed by a clock pulse, only when the active terminal is already standing at the 0 state. Further counters so connected would behave in a similar fashion, their outputs being inhibited until the states of the preceding counters stand at 0. Their subsequent change of state is synchronously related, and controlled by the following clock pulse. Thus, a binary count is obtained, the active terminals for each counter changing in accordance with the truth table shown in Fig. 4(c).

The salient feature of this form of divider is that a simultaneous change of all counters in the divider chain eliminates the delay between the operation of individual counters. There is, however, the inherent delay between the arrival of the clock pulse and the change of counter state, which is equal to the propagation delay of one counter element.

The process to determine a 'unit' pulse is illustrated by this counter and its associated waveforms. Here a control waveform at frequency f is combined in the NAND/NOR gate with the outputs from two following binary dividers. The gate passes only those parts of the input waveforms which are coincident, that is, 'unit' pulses spaced by four control waveform cycles. Thus the spacing is determined wholly by division of the control waveform.

A 'unit' period is defined as one complete cycle of the control waveform. Therefore, a pulse lasting for the duration of a 'unit' period would take the form of one half-cycle of the waveform $f/2$ in Fig. 4(c).

The division ratio of a parallel clocked counter may be other than a binary number. A divider of this form is shown in Fig. 5 and requires the NAND/NOR gate in Fig. 4(b) to achieve the non-binary count. This gate has more than one input and only one output.

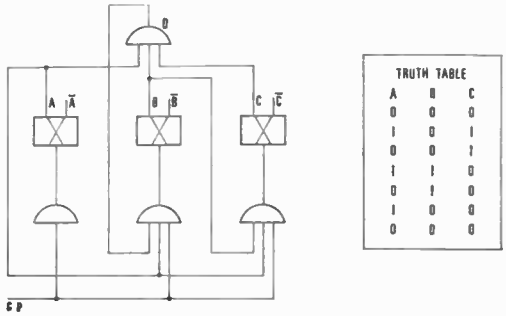


Fig. 5. Parallel clocked counter for divide-by-6.

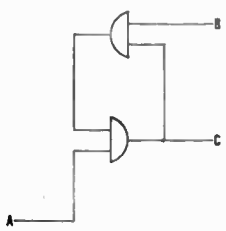


Fig. 6. NAND/NOR gates connected as bistables.

For a pulse at the 1 state applied to one or more input, the output will be at 0; only when every input is at 0 will the output be at the 1 state.

An *n*-input gate may take its inputs from an *n*-stage parallel clocked counter and perform the function of a recognition gate, so named because of the ability to recognize a particular state in the count and to give a 1 output while that state exists. The state to be recognized is determined by connecting the requisite output terminal of each counter to the gate input terminals. If connexions are made from the Q terminals of a three-stage counter, the gate will recognize the state 000. If, however, connexions were made to the Q terminals on the first and last counters and to $\bar{Q}$ on the second counter, the gate would recognize the state 010 at the Q terminals. Thus, a recognition gate can be connected to recognize any selected state in the count.

To obtain division with a parallel clocked counter by less than its natural radix, it is required to omit the appropriate number of states in its truth table, following the 0 state for all counters.

To divide by six, two states, namely 111 and 011, are omitted, giving the truth table shown in Fig. 5, whose accompanying diagram shows the interconnexion of basic logic elements necessary to achieve those omissions. Division is performed in the following manner.

Recognition by gate D of the 000 state provides an inhibiting signal to the input of the second counter to which the output of the recognition gate is connected. Hence the next state of the divider is 101. At this change inhibition ceases and the divider follows the normal sequence until state 000 is again reached. This involves a total of six states instead of 8 per cycle, normal to a three-stage divider. It will be noted that the outputs from the second and third stages of the counter are asymmetric pulses at 1/6th of the clock frequency.

Other division ratios may be obtained by connecting the output of the recognition gate to a different input gate or to more than one gate in parallel. Thus, by

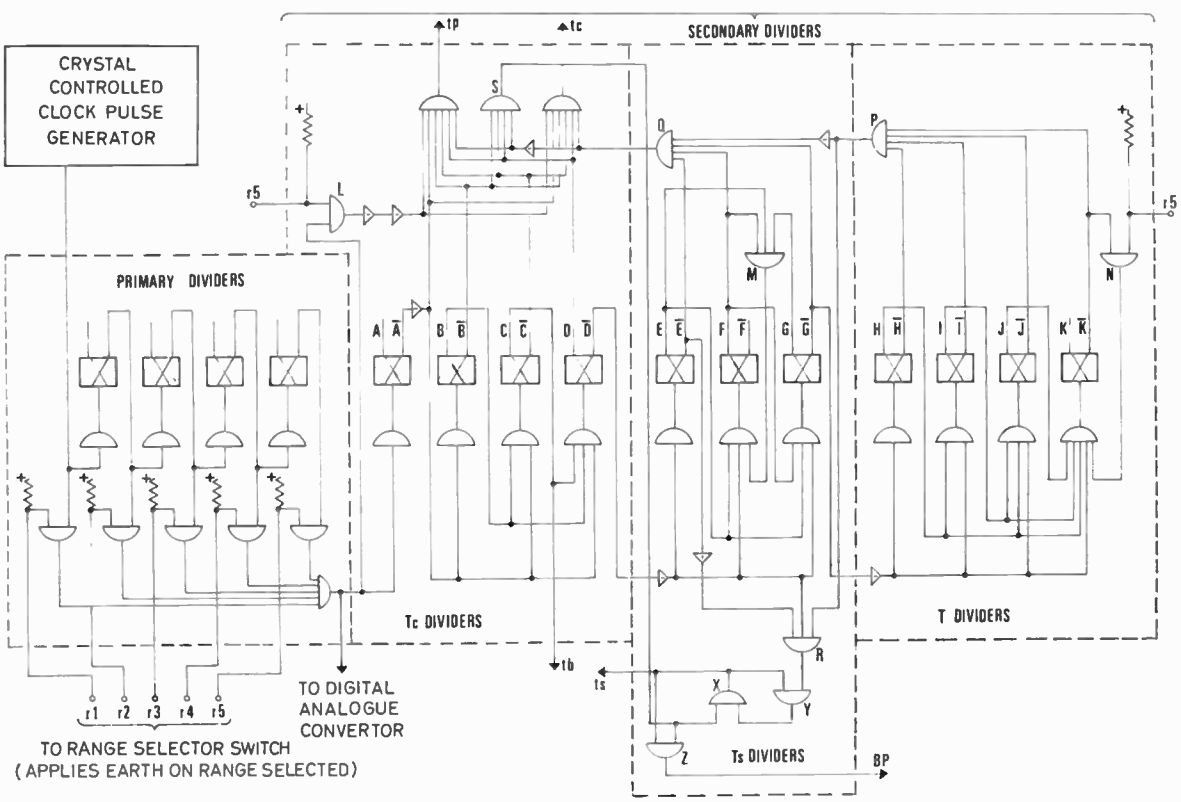


Fig. 7. Display logic diagram.

suitable connexion of the recognition gate output of an n-stage counter, any division ratio from 2 to 2^n may be obtained.

A pair of two-input NAND/NOR gates may be connected as shown in Fig. 6 to form a bistable element. The action of this bistable arrangement is that a 1 state of input terminal A sets output terminal C to 0 and a 1 state on input terminal B sets terminal C to 1, the alternative input in each case being held at 0. However, if the alternative input terminals are held at the 1 state, the change of state will be temporary, lasting only for the duration of the applied 1 state.

By connecting a number of these few basic logic elements in the arrangement shown in Fig. 7, a logic unit was constructed from which to derive the desired functional pulses and waveforms.

In preparation for a higher resolution system, it was decided to employ a clock pulse generator operating at twice the design frequency. For this reason the circuit arrangement in Fig. 7 shows an extra stage of division A. However, use is made of this divider as well as the two additional gates L and N to satisfy the transmission pulse and repetition frequency limitation for range 5.

The duration of t_p is equal to a 'unit' period of the control waveform for ranges 1 to 4. For range 5 the gate L is enabled and permits a 'unit' pulse to be recognized at the t_p gate, thereby halving the duration of the transmission pulse only for that range position. Likewise, gate N is inhibited and permits a count of 16 at the H I J K counters for ranges 1 to 4. For range 5, N is enabled, thereby inhibiting the last stage of division by counter K and effectively doubling the repetition frequency for that range position.

Other deviations from the original schematic diagram are the safety precaution arrangements to minimize the burning of a centre spot at the c.r.t. screen by the removal of the t_c pulse coincident with t_p, and a brightening pulse delay achieved by the S and Z gate combination.

8. Practical Performance

An experimental model (Fig. 8) was built to study system feasibility. The elements employed were from the Plessey SP.200 family of low-power r.t.l. units, comprising gates, bistable units, buffers and expanders in T05-type packages. The series operates from a 3–4 V power supply and consumes exceedingly low power. The maximum specified counting rate for a single counter element is 10 MHz, or 5 MHz for a clocked counter, with a typical gate delay of 30 ns. In fact, the experimental model operated correctly at a basic clock pulse rate up to 27 MHz.

Very little modification was required after assembly and wiring, and then only to reduce capacitive loading on some of the ouputs. Propagation over long lines required pulse reshaping at the remote end.

However, the number of elements necessary in this range was large and the external interconnexion pattern complex. A high degree of simplification was found possible by use of a family of multiple units in dual-in-line packages, and this series was employed in later work.

A complete radar system was built using the foregoing methods. The logic system (Fig. 9) was found to present no difficulties, the required accuracy being easily achieved and maintained over a temperature range of $-15°C$ to $+55°C$. A 3·6 V supply was used, and power consumption of the clock unit and primary and secondary divider systems, though considerably higher than that required by the SP.200 system, did not exceed 2 W. Tolerance to supply voltage variation was found to exceed $\pm 10\%$.

9. Conclusions

From the equipment manufacturer's point of view, the advantages of logic control in marine radar equipment are: economic storage due to the standardized logic family being few in number and physically identical; simplified assembly, made possible by repetitive terminal patterns and printed interconnexions and few, if any, conventional components. All these factors are favourable to the employment of semi-skilled labour. As a complement to this is added the economic advantage gained from the significant reduction of costs achieved by large-quantity purchases of standardized logic packages and the continuous reduction of costs enforced by competition.

Furthermore, unit and functional testing is simplified by the 'go no go' characteristic of logic assemblies eliminating the need for adjustment and the employment of skills. The after-sales service also shares the

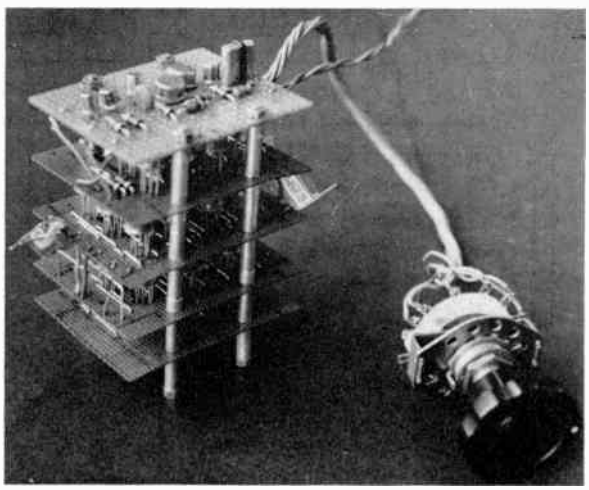


Fig. 8. Experimental logic unit.

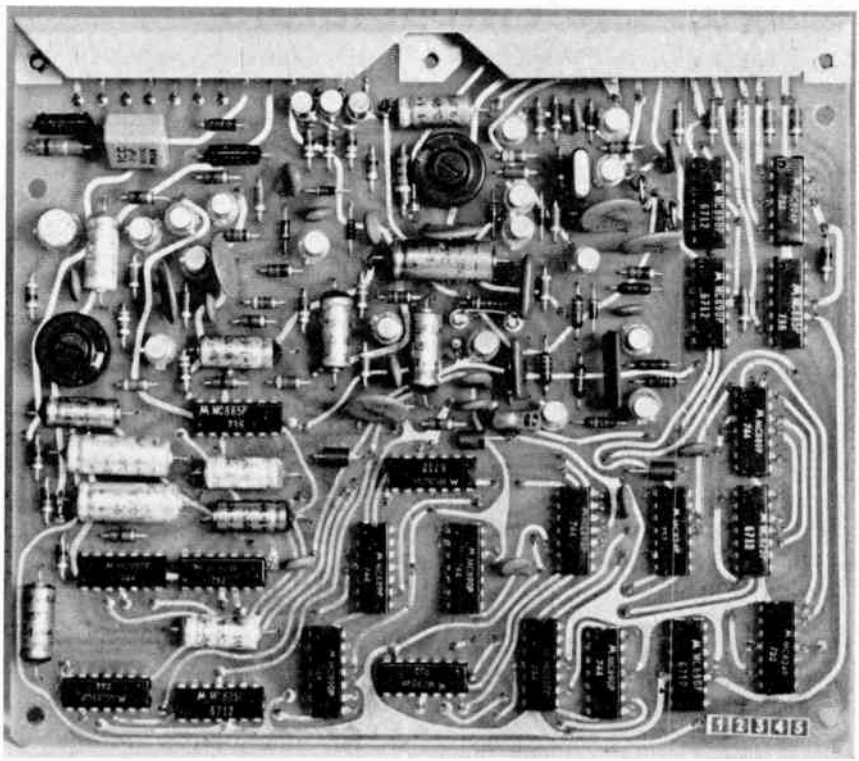


Fig. 9. Master timing unit for pulse radar system.

advantages, by virtue of the simple check-out and replacement of units if designed on a module basis, and the high degree of reliability expected from a logic assembly reduces service calls.

Finally, it is postulated that present performance standards for a pulsed radar system are device-limited. If, therefore, the practical achievement of higher standards by a superior technology is possible, such analogue systems that may be replaced with technical and economic advantage by digital logic will have been driven into obsolescence by their own shortcomings.

10. Acknowledgments

The author wishes to thank Dr. R. C. Foss and A. Richardson of the Microelectronics Division of the Plessey Company Limited, for their helpful advice, his colleagues for their assistance and co-operation, and the Plessey Company Limited for permission to publish this paper.

11. References

1. Schwartz, S. A., 'Transistor Range Marker and Sweep Generator for Radar Display', S. G. S.-Fairchild. Application Report No. 96.
2. Waddington, D. E. O'N., 'The diode-transistor pump', *Wireless World*, 72, pp. 338–42, July 1966.
3. Foss, R. C., 'Present Application of Microelectronics to Equipment Engineering', Semiconductors Ltd. Technical Communications.
4. Ridenour, L. N., 'Radar System Engineering', Vol. 1, M.I.T. Radiation Laboratory Series. (McGraw-Hill, New York, 1949).
5. Soller, T., Starr, M. and Valley, G. E., 'Cathode Ray Tube Displays', Vol. 22, M.I.T. Radiation Laboratory Series. (McGraw-Hill, New York, 1949).
6. Millman, J. and Taub, H., 'Pulse and Digital Circuits'. (McGraw-Hill, New York, 1956).

Manuscript received by the Institution on 11th November, 1969. (Paper No. 1323/AMM30.)

U.D.C. 535.35: 621.376

Magneto-optic Light Modulators

By

R. W. COOPER,
B.Sc., A.Inst.P.†

and

J. L. PAGE†

Reprinted from the Proceedings of the I.E.R.E. Conference on 'Lasers and Opto-Electronics' held at the University of Southampton on 25th to 28th March 1969.

Magneto-optic modulators for near-infra-red radiation (wavelength 1·1 to 5·5 μm) are described. These modulators use the Faraday effect in single crystals of yttrium iron garnet. The modulators operate with low driving voltages and are well suited to transistor drive. The application of yttrium iron garnet as a laser *Q*-switch is also discussed.

1. Introduction

Magneto-optic light modulators present an attractive alternative to the more familiar electro-optic devices for modulation of near-infra-red radiation in the wavelength band 1·1 to 5·5 μm. Over this wavelength range the ferrimagnetic material yttrium iron garnet (YIG) has a transmission 'window' and exhibits high Faraday rotation. Single crystals of this material and related compounds may be used to construct light modulators requiring low drive voltages. The material properties are not strongly temperature-dependent so that temperature control is unnecessary. In this paper we describe two types of light modulator and give performance data relevant to their use as modulators for near-infra-red lasers.

2. The Magneto-optic Faraday Effect

Faraday rotation[1] is a rotation of the plane of polarization of light as it traverses a magnetic medium. The effect may be observed in all transparent materials but its magnitude is usually very small. For example, in flint glass, a diamagnetic material which shows a relatively large effect, Faraday rotations of the order of one degree per kilo-oersted of applied magnetic field per cm thickness of material are observed.

Only in materials of the ferromagnetic class where a high internal field exists, which can be manipulated by a small applied field, are high values for the Faraday effect found.

Usually this high Faraday rotation is accompanied by strong optical absorption which limits its usefulness in practical devices. However, in single crystal yttrium iron garnet and doped YIG materials, there is a transparent 'window' in the near-infra-red part of the spectrum.[2]

For a ferromagnetic material the rotation, θ, of the plane of polarization per unit path length in the material is given by

$$\theta = \alpha_F \cos \phi \qquad \text{.....(1)}$$

where ϕ is the angle between the direction of magnetization and the light direction and α_F is an experimentally determined constant for a material at a given light wavelength and temperature.

For YIG at 300°K α_F (1·15 μm) = 255 deg/cm

α_F (3·39 μm) = 65 deg/cm

Equation (1) applies to a ferromagnetic material magnetized to saturation. For a material partially magnetized proportionately less Faraday rotation is observed.

3. Low-frequency Modulator

A simple form of magneto-optic modulator consists of a parallel-sided disk of material placed in a small coil (Fig. 1). An alternating current in the coil gives a magnetic field normal to the plane of the disk. The material becomes magnetized in this direction and light propagating through the disk suffers a rotation of its plane of polarization. The modulation of the angle of the plane of polarization induced by the alternating current is converted to amplitude modulation by passing the beam through a polarizer. Attractive features of this form of modulator are the large aperture and acceptance angle and the low drive power requirements. The low drive power is a consequence of the use of gallium-doped YIG, a material which has low saturation magnetization. The Faraday rotation introduced by the disk is independent of the angle of incidence.

Since from equation (1) we have

$$\theta = l\alpha_F \cos \phi \text{ (degrees)}$$

where l = path length of the beam in the magnetic medium; but $l = t/\cos \phi$

where t is the disk thickness,

whence $\theta = t\alpha_F$ (independent of ϕ)

For the configurations shown in Fig. 1 the acceptance half-angle is greater than 50°. However, at large angles of incidence, reflexion losses at the YIG surfaces limit the optical transmission of the device.

† Mullard Research Laboratories, Redhill, Surrey.

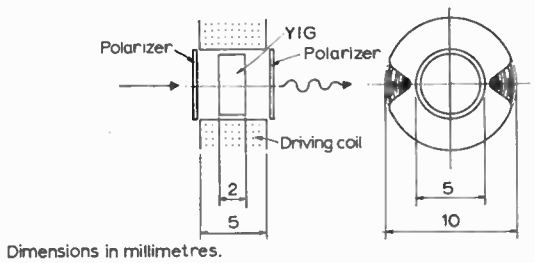


Fig. 1. Low-frequency modulator.

Details of this type of modulator are shown in Table 1.

Table 1. Details of low-frequency modulator

Aperture	5 mm
Acceptable angle	50°
Thickness of element	2 mm
Maximum drive current	25 mA
Drive voltage (1 kHz)	3 V
Coil inductance	5 mH
Coil resistance	100 Ω
Temperature coefficient of modulation depth	0·5%/°C
Polarizer: Polaroid type HR	

The transmission and maximum depth of modulation obtainable from this device is shown in Fig. 2. The maximum depth of modulation is dictated by the α_F value for the material and this is a function of light wavelength. Larger modulation depths are obtained using thicker magneto-optic elements.

For this type of modulator there is an upper frequency limitation. This is because the magnetization is reversed by domain wall processes which are inherently slow and lossy. The response of this modulator is 25% down at 100 kHz for a constant 4 mA drive.

4. V.H.F. Modulators

For light modulation at higher frequencies it is necessary to maintain the modulating element in a magnetically-saturated condition. In this condition the magnetic losses are greatly reduced and operation up to several hundred megahertz is possible. Modulators of this type were first described by LeCraw.[3] The modulating element takes the form of a rod of gallium-doped yttrium iron garnet, typically 1 cm long by 0·5 mm diameter. The light propagates along the rod axis. The rod is subject to a transverse bias field provided by small permanent magnets, and a small coil wound on the rod gives a magnetic field component parallel to the direction of light and thus Faraday rotation. The magnitude of the bias magnetic field is chosen to be sufficiently large to saturate the rod and to ensure that the ferromagnetic resonance frequency of the configuration is outside the operating frequency range of the modulator. The drive current magnitude for a particular modulation depth is dependent on the correct choice of crystal orientation. It may be shown that for a cubic magnetic material with negative magneto-crystalline anisotropy constant (K_1), <100> rod axis and <110> field direction give optimum results, i.e. in this condition the magnitude of the bias magnetic field can be chosen to give high magnetic susceptibility along the light direction combined with high magnetic resonance frequency.

The modulator operates in a non-resonant mode and gives a true broadband response. Table 2 gives details of this modulator.

Table 2. V.h.f. YIG modulator

Rod dimensions	10×0·5×0·5 mm
Coil	25 turns, 38 s.w.g.
Coil inductance	0·2 μH
Drive current	100 mA r.m.s.
Drive voltage (100 MHz)	12 V

The transmission and modulation depth (corresponding to 100 mA drive) are shown in Fig. 3. In Table 3 the data corresponding to some near-infra-red lasers are presented. We note that the absorption edge of YIG materials at 1·1 μm does not permit use of these modulators with the Nd-YAG 1·06 μm emission.

Table 3. Data relevant to near-infra-red lasers

Laser	Wavelength μm	Modulator transmission %†	Modulation depth %
He—Ne	1·15	35	71
Nd—YAG	1·32	96	54
Ho—YAG	2·1	98	28
He—Ne	3·39	98	11

Reduced drive currents may, of course, be obtained by tuning the modulator in a resonant circuit. A

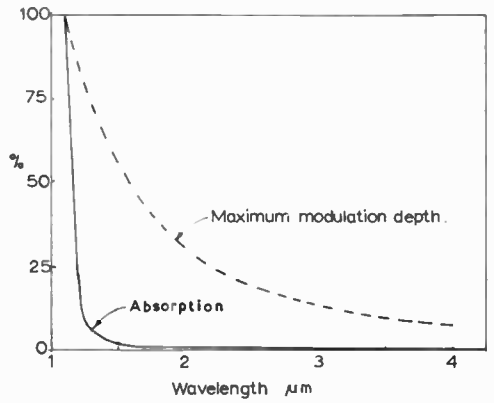


Fig. 2. Performance of low-frequency modulator.

† The transmission data assume good anti-reflexion coatings for these wavelengths.

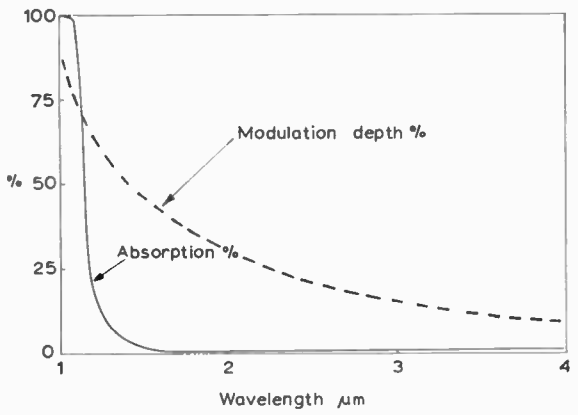


Fig. 3. Performance of v.h.f. modulator.

typical Q-factor of about 50 is obtained at 75 MHz. A photograph of the modulator developed at Mullard Research Laboratories is shown in Fig. 4.

5. Laser Q-Switch

Over the wavelength range 1·3 to 5 μm YIG materials show extremely low loss and may be employed in Q-switch devices for near-infra-red lasers. A scheme for such a Q-switch is shown in Fig. 5. This scheme makes use of the non-reciprocal nature of Faraday rotation. Thus, light which passes through a Faraday element and is subsequently reflected back through the element suffers two rotation *in the same sense*. In the proposed Q-switch the lossless condition is maintained by holding the magnetization in the magneto-optic element normal to the light direction. If the magnetization is switched parallel to the light direction, the subsequent rotation of the plane of polarization results in reflexion losses at the Brewster angle surfaces.

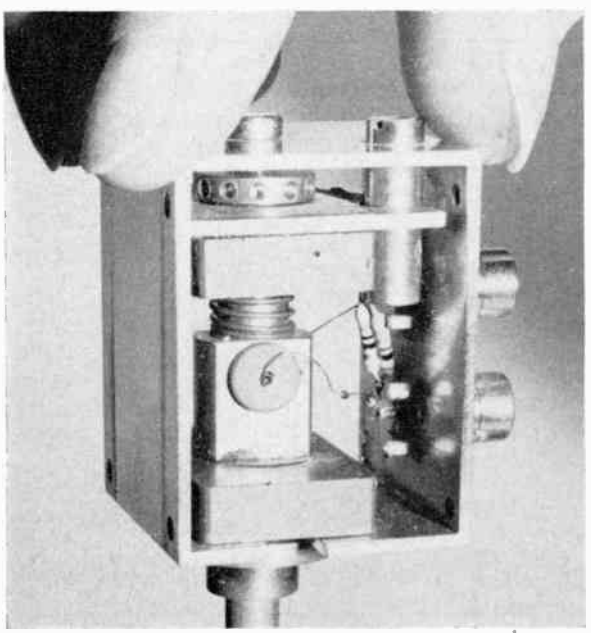


Fig. 4. V.h.f. light modulator.

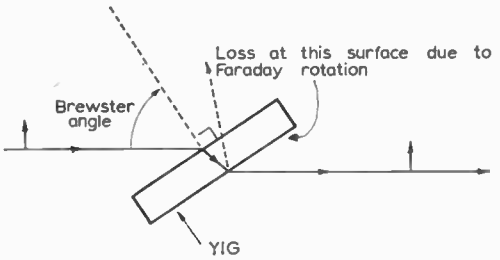


Fig. 5. Magneto-optic Q-switch.

Magnetization perpendicular to light path in the crystal: no loss. Component of magnetization parallel to light path: reflexion at second surface.

The passage of light through the YIG slice is illustrated in Fig. 5. For a beam polarized in the plane of the paper there is no reflexion loss at the Brewster angle. After passing the YIG block the plane of polarization is rotated out of the plane of the paper. There is a component of polarization normal to the paper and this component suffers a reflexion loss at the YIG/air interface. Upon reflexion at the laser mirror and retraversing the YIG block a further rotation of the plane of polarization occurs, resulting again in reflexion loss.

6. Conclusions

Magneto-optic modulators are attractive devices for use in the near-infra-red. The low-frequency type with wide angular aperture find application as radiation choppers for use with lead sulphide detectors. Transmission of television video signals has been demonstrated with the v.h.f. type which may also find applications in distance measurement equipment. As current-operated rather than voltage-operated devices the drive requirements of magneto-optic modulators are well matched to transistor circuitry.

7. References

1. See, for example, Jenkins, F. A. and White, H. E., 'Fundamentals of Optics', p. 596, 3rd ed. (McGraw-Hill, New York, 1957).
2. LeCraw, R. C., Wood, D. L., Dillon, J. F. and Remeika, J. R., 'The optical transparency of yttrium iron garnet in the near-infra-red', *Applied Physics Letters*, 7, pp. 27–8, July 1965.
3. LeCraw, R. C., 'Wide-band infrared magneto-optic modulation', *I.E.E.E. Trans. on Magnetics*, MAG-2, p. 304, September 1966.

Manuscript first received by the Institution on 5th March 1969 and in revised form on 25th February 1970. Short Contribution No. 135/CC79.

Institution Dinner 1970

Over 300 members and guests were present at the Institution Dinner on May 12th at the Mansion House, London, when the President, Mr. Harvey F. Schwarz, made his speech of welcome and thanks to the Lord Mayor of the City of London, Lieutenant-Colonel Sir Frank Bowater. Mr. Schwarz referred to the links of the Institution with the City and, in the wider sense, the dependence of Industry generally on the City's financial backing of expansion. In reply the Lord Mayor spoke of some of the aims of his Corporation in fostering international goodwill. (Both speeches are reported fully in the July issue of the *Proceedings of the I.E.R.E.*)

The third speaker of the evening was H.R.H. Prince Philip, Duke of Edinburgh, who proposed the Toast of 'The Institution of Electronic and Radio Engineers'. He first made observations on the preceding speeches by Mr. Schwarz and the Lord Mayor and His Royal Highness continued:

'I suspect that I owe my invitation to this dinner to the fact that I am President of the Council of Engineering Institutions. This is a body comprising representatives of 14 Institutions of various kinds of engineering, of which this Institution was a founder member. In a way it is a merger, but I believe the C.E.I. could be more aptly described as a successful ecumenical movement amongst the high priests of engineering. It came about because, as everyone knows, engineers are practical people and it began to dawn on them that whereas engineering can be divided into specialities, when it comes to functional technology success can only be achieved by co-operation. Transport for example is one major functional technology to which a whole host of engineering specialities make a larger or smaller contribution. Health, aviation and oceanography are also examples.

'In this connection I hope it did not go entirely unnoticed that the Australian Government established a visiting Fellowship in marine sciences to mark the Queen's visit to Australia for the Cook bicentenary celebrations. This struck me as a particularly suitable way to commemorate Cook's memorable journey and all the more appropriate in that it is open to any specialization in science or engineering.

'This inter-disciplinary approach is well understood by this Institution which has organized and continues to organize conferences and meetings about technologies involving several engineering specialities. Electronics has its sensing probe in every technological concoction, which is just another way of saying that it has its finger in every pie.

'It also became apparent to these, naturally far-sighted, Institutions that unless they got together to establish remotely comparable professional qualifications the teaching situation in universities, technical colleges, and the employment situation in consultant partnerships and in industry would become completely chaotic.

'The Charter of every Institution has something to say about responsibility for education and qualification and the first and principal concern of the C.E.I. has been to establish qualifications for the title of Chartered Engineer. But that is not the end of the problem because education in any technology cannot remain static, the content of the courses, the methods of teaching and the techniques of examination need to change and adapt as fast as the technology develops. It's one thing to get the organization of education right, it's a good deal more difficult to keep the content of education up to date.

'The engineering professions are shirking their responsibilities if they only concern themselves with exams and qualifications. They must take some part in the teaching process as well. Furthermore it is quite useless merely laying down the rules for the engineering "generals" and ignoring the qualifications for all the other ranks from "private" upwards. The training and qualification for each rank must be related to the requirements of the next rank up, and at each stage the vital factors of practical experience and performance in the job must be taken into account. As engineering becomes more complicated, and therefore more specialized, the need for specialist training spreads all the way from operative through technician to Chartered Engineer.

'I am glad to say that the I.E.R.E. has always supported this view and it has opened its doors to senior technicians as Associates and encourages them to continue their studies so that they can become corporate members. Without this extra source of supply the numbers of Chartered Engineers coming directly from the universities would be quite inadequate for the demand.

'The C.E.I. is also tackling this problem and is indeed involved in preparing a register of Technician Engineers. At the same time the Open University has decided to give due recognition to holders of H.N.D. and H.N.C. should they continue their studies for a degree. This is important for two reasons. It means that young people do not have to go to University immediately on leaving school if they are ever to qualify as Chartered Engineers. It also means that technicians with industrial experience are not denied the opportunity to qualify as Chartered Engineers at any stage of their careers.

'All these attempts to rationalize and to bring some sort of coherence into engineering qualifications does not mean creating a rigid and inflexible system. Engineering needs above all people with an individual,

original and inventive turn of mind. This means that there is a need for a healthy variety in courses, different attitudes to teaching methods, and a whole host of opportunities for further training and retraining.

'Even more important is that courses should not be limited to purely academic professional subjects. Engineering is no longer a matter of providing useful structures and helpful gadgets or even simply a matter of creating wealth. Technology is now in effective control of our human environment and as engineering is that vital link between science and its application as technology, engineers are the architects of man's future.

'The way people live and exist in this modern world is governed almost entirely by technology. This places a new and heavy responsibility on all engineers. I get the impression that many people believe that it is only the social sciences and those who study the humanities who end up by working with people or have any control over human society. They seem to think that anything scientific or technical is divorced from human relationships. I believe they are mistaken. It is my belief that now, and increasingly in future, it is the technologists who have the most direct impact on the way we live. If only all those with a burning ambition to change the world realised that their best chance is through technology, there would be no shortage of qualified engineers.

'In the end any kind of professional education is a preparation for decision making. On the professional side decisions relate to design, manufacture and maintenance. On the management side decisions relate to people; the direction and organization of their work. This means in effect that the educational process needs to be organized so as to prepare people for the responsibility of making important decisions. This sort of decision cannot be made entirely on technical knowledge or by looking up reference books, it depends just as much on personal judgement, personal experience and personal understanding. If these decisions are to be in the best interests of mankind as a whole, the people who make them must have a broad view of what life is all about and they must be inspired by a vision or at least a hope for the future.

'No engineering discipline touches human life at so many points or is involved in so many functional technologies, and none offers greater opportunities for future development than electronic engineering. The manner in which these opportunities are grasped depends to a very large extent upon the influence and outlook of this Institution. It therefore gives me the very greatest pleasure to propose a toast to the future well-being of the Institution of Electronic and Radio Engineers.'

On behalf of the Institution, the Immediate Past President, Sir Leonard Atkinson, replied and thanked His Royal Highness for reminding engineers of their interdependence on technicians.

STANDARD FREQUENCY TRANSMISSIONS—May 1970

(Communication from the National Physical Laboratory)

May 1970	Deviation from nominal frequency in parts in 10^{10} (24-hour mean centred on 0300 UT)			Relative phase readings in microseconds N.P.L.—Station (Readings at 1500 UT)		May 1970	Deviation from nominal frequency in parts in 10^{10} (24-hour mean centred on 0300 UT)			Relative phase readings in microseconds N.P.L.—Station (Readings at 1500 UT)	
	GBR 16 kHz	MSF 60 kHz	Droitwich 200 kHz	*GBR 16 kHz	†MSF 60 kHz		GBR 16 kHz	MSF 60 kHz	Droitwich 200 kHz	*GBR 16 kHz	†MSF 60 kHz
1	− 300·0	− 0·1	+ 0·2	619	566·2	17	− 300·0	0	+ 0·2	622	579·3
2	− 300·0	− 0·1	+ 0·1	619	567·0	18	− 300·0	− 0·1	+ 0·2	622	580·1
3	− 300·0	− 0·1	+ 0·1	619	567·8	19	− 300·0	0	+ 0·1	622	580·5
4	− 300·0	0	+ 0·1	619	568·0	20	− 300·0	0	0	622	580·1
5	− 300·0	0	+ 0·1	619	568·3	21	− 300·0	− 0·1	0	622	580·9
6	− 300·0	− 0·1	+ 0·1	619	569·5	22	− 300·1	− 0·1	0	623	581·8
7	− 300·0	0	+ 0·1	619	569·5	23	− 299·9	0	0	622	582·0
8	− 300·0	− 0·1	+ 0·1	619	570·7	24	− 300·0	− 0·1	+ 0·1	622	582·8
9	− 300·0	− 0·1	+ 0·1	619	571·7	25	− 300·0	− 0·1	0	622	583·6
10	− 300·1	− 0·1	+ 0·1	620	572·9	26	− 300·0	0	+ 0·1	622	584·0
11	− 300·1	− 0·1	+ 0·1	621	574·3	27	− 300·0	− 0·1	+ 0·1	622	585·1
12	− 300·1	− 0·1	+ 0·1	622	574·9	28	− 300·0	0	+ 0·1	622	584·7
13	− 300·0	− 0·1	+ 0·1	622	576·3	29	− 300·0	0	0	622	584·5
14	− 299·9	0	+ 0·1	621	576·7	30	− 300·0	0	+ 0·1	622	584·7
15	− 299·9	− 0·1	+ 0·1	621	577·7	31	− 299·9	0	+ 0·1	621	584·5
16	− 300·1	− 0·1	+ 0·2	622	578·9						

All measurements in terms of H.P. Caesium Standard No. 334, which agrees with the N.P.L. Caesium Standard to 1 part in 10^{11}.

* Relative to UTC Scale; $(UTC_{NPL} - Station) = +500$ at 1500 UT 31st December 1968.

†Relative to AT Scale; $(AT_{NPL} - Station) = +468{\cdot}6$ at 1500 UT 31st December 1968.

U.D.C. 621.374 : 681.32

A Micrologic Vector Generator

By

T. S. PLEWS,
M.Sc.,†

C. R. BARBER,
(Graduate)‡

and

K. G. NICHOLS,
M.Sc., C.Eng., F.I.E.R.E.‡

The specification, logical design and construction of a vector generator are described. The input data comprise two coordinate pairs giving the start and end points of the vector and a pair of single decimal digits which determine the gradient of the vector with respect to the two coordinate axes in the plane. The intermediate coordinate points are generated sequentially from the starting point of the vector and are equidistantly spaced from each other by one unit of the least significant digit of the coordinate system. By necessity the intermediate points cannot all lie exactly on the vector joining the start and end points. The generator is intended for the control of the deflexion of an electron beam in an electron beam milling machine or in a cathode-ray tube display system. In these applications the beam is required to trace specific patterns determined by data punched on paper tape. However, the system is potentially useful in many two-coordinate position control systems. The generator has been implemented using r.t.l.-micrologic integrated circuits.

1. Introduction

In many digital positional control systems there is a need for a system whch is able to generate sequentially coordinate points lying along a straight line. It is often inconvenient to provide each such coordinate as input data in the system. This may be because of the very bulk of input material required in the form of paper tape, magnetic tape, or punched cards, or because of the prohibitive time required to read into the system each coordinate from such an input medium. A more satisfactory solution is to read in the coordinates of the starting and end points of the line and to arrange for the system to generate the intermediate coordinate points of the line. To avoid complication of the system it may also be desirable to provide the gradient of the line as input data.

Each coordinate is represented by three decimal digits. The coordinate space is therefore not a continuous one, but is spanned by a discrete array of points. When a straight line is drawn between two specified points in this array it will pass through certain other points in the array and the density of such points along the line will vary with the direction (gradient) of the line. It would be possible to devise a system which would generate only those points which actually lie on the line, but this would be inconvenient for many applications. For example, in controlling the deflexion of the beam in a cathode-ray tube display, this would mean that the brightness and continuity of the trace on the screen would be dependent on the gradient of the line being drawn. In such an application it is desirable to allow the beam to move to discrete coordinate points which are not exactly on the line, but are sufficiently close to it to retain a good approximation to the path of the line. In an ideal situation the selection of these points should be made in such a way that the density of the points along the trace remains approximately constant.

In the system to be described the approximation to the required line is always made up of alternate small segments in the two coordinate directions. Each small segment is formed by incrementing the appropriate coordinate in units of the least significant digit of the coordinate. Although this arrangement does not meet the ideal requirement of a constant density of points along the trace, it was adopted to avoid too complex a logical system. Coordinates are expressed as three-digit decimal numbers in the range 0 to 999, each digit being represented by four bits of a direct binary code. The coordinate space is thus spanned by a 1000-by-1000 array of discrete points. These details of the system were determined by the particular applications for which the system was required, namely, the control of the deflexion of the beam in an electron beam milling machine and in a cathode-ray tube display. The focused spot resolution of the beam in each application was approximately one thousandth part of the maximum beam scan. Also the maximum precision with which a digital number could be converted into an analogue signal for the magnetic or electrostatic deflexion of the beam is only a little better than one part in a thousand. These two factors fixed the choice of the number of decimal digits in each coordinate to three. In other applications it is possible that a different number of decimal digits would be required.

† Formerly at the University of Southampton, now with B.A.C. Ltd., Bristol.

‡ Department of Electronics, University of Southampton, Southampton SO9 5NH.

The system has been designed in such a way that a number of different types of data input mechanisms could be used with appropriate input circuits. In particular almost any form of eight-hole paper tape reader or incremental magnetic tape reader might be used. In the system as constructed, however, a comparatively slow, transport pulse type of paper tape reader (Invac, Model R-110) is used.

The input data format is based on what is substantially the ICL 1900 eight-bit code. An ICL 1907 computer is used to provide output data tapes in a suitable format for operating the system. When the system is required to trace a line in either of the x- or y-coordinate directions the input data comprise two pairs of coordinates (all positive numbers of up to three decimal digits). The first pair is the starting point of the line and the second pair the end point. When the system is required to trace a line with an x to y gradient (diagonal line) the two pairs of coordinates are followed by a pair of single decimal digits in the input data. The ratio of these digits gives the gradient of the required line. This arrangement limits the choice of line gradients but the range of gradient is still adequate for most purposes. As mentioned previously, the line traced is not strictly straight, in the latter case being drawn in small segments alternately in the two coordinate directions. Figure 1 indicates the path of the line when the gradient digits are (a) 1:1, (b) 1:2, (c) -2:1, giving lines of gradient angles 45°, 22½° and $-67\frac{1}{2}$° respectively.

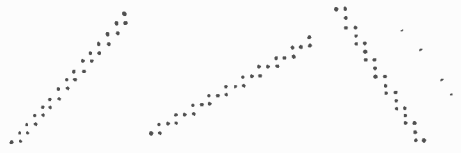


Fig. 1. Method of describing diagonal lines.

In addition to giving the intermediate coordinate points along the line, the system also gives an output pulse at each point. This is used, for example, to switch the electron beam on at each point. When the system is required to give a single point, say for a drilling operation with the electron beam milling machine, this is achieved by drawing a line of zero length. In this case the start- and end-point data in the input are made identical and, of course, the gradient data are omitted.

A number of control characters are also necessary in the input data. These are used to indicate to the system the type of data, for example coordinates or gradient digits, about to be presented to the input. The choice of these control characters and the input data format was largely decided by the format requirements of an x-y digital graph plotter (Benson-Lehner, Electroplotter II) which is used to check input tapes prior to use in the system.

The six control characters used are:

FE2	Carriage return
TC10	Pen lift
TC9	Anti-herald
TC8	Herald
SP	Space
TC4	General stop

The arrangement of the two pairs of coordinates in the input data format is as shown below (d stands for a digit character):

FE2	SP	ddd	SP	SP	SP	ddd	SP	SP	(Start
		x_1				y_1			coordinates)
FE2	SP	ddd	SP	SP	SP	ddd	SP	SP	(End
		x_2				y_2			coordinates)

Each pair of coordinates is preceded with an FE2 character and each coordinate is terminated by two SP characters. Positive signs are replaced by SP characters (all computers do this automatically on output), that is the third SP character between the x- and y-coordinates is equivalent to a positive sign. Non-significant zero digits in the coordinate data may be replaced by SP characters (all computers do this automatically on output) but the coordinate of value zero must have at least its last digit written as a 0 character.

The above two lines of data must be followed by one of the three different sets of data as follows.

Either, (1) FE2 TC10 (Line terminated)

This line is only permissible if either y_1 and y_2 or x_1 and x_2 are identical, thus indicating a line parallel to one of the coordinate directions. In addition the line must be drawn in the positive sense of the coordinate axis to which it is parallel. On receipt of these data the system generates the required intermediate coordinates and provides an output pulse at each position. The x-y graph plotter draws a continuous line between the given coordinates and then lifts its pen. After the above data the system awaits data for the start and end points of a new line: no output pulses are produced as the system subsequently moves to the start position of the new line, nor does the x-y graph plotter draw a line between the end point of the old line and the start of the new line.

Or, (2)

FE2	SP	ddd	SP	SP	SP	ddd	SP	SP	(End coordin-
		x_3				y_3			ates of a new
									line)

Again with these data the original line must be parallel to one of the coordinate axes. On reading the FE2 and first SP characters the original line is drawn as

previously. The new data correspond to the end point of a new line whose starting point is the end point of the original line. The pen of the *x-y* graph plotter does not lift in this case. Just like the first two lines of data, this last line of data can be followed by one of the three different sets of data.

Or, (3)

FE2 TC9

	SP	(Gradient data for the
FE2 SP d SP	or d SP	preceding coordinate data)
	–	

FE2 TC8

The FE2 and TC9 characters indicate to the system that gradient data are to follow. The two single decimal digits, in the order in which they appear, give the *x*-direction and *y*-direction segment increments respectively. On reading the FE2 and the subsequent character following these digits the system generates the intermediate coordinates for the line whose end point is given by the preceding data. The system effectively ignores the following FE2 and TC8 characters which are used to instruct the *x-y* graph plotter. The latter draws the line from (x_1,y_1) to (x_2,y_2) by an analogue technique and hence does not require the gradient data. Enclosing these data between the character sets FE2 TC9 and FE2 TC8 causes it to be ignored by the *x-y* graph plotter.

The data set of type (3) can be followed by data sets of type (1) or (2).

This completes the explanation of the format, an understanding of which is necessary to appreciate the design of the system.

2. Description of the Overall System

A block diagram of the system is given in Fig. 2. In this section a description of the operation of the system will be given in terms of this diagram. Only those blocks of this diagram involving unique features of the design will be described in any detail. The system has been implemented in resistor-transistor-logic integrated circuits (Fairchild μL 900 series) and the figures are drawn in terms of members of this family. Negative logic is used and the elements are then NAND gates and JK flip-flops.

The passage of a sprocket hole in the paper tape through the reader is used to generate read pulses D0, D1 and D2 which are in synchronism with the next three pulses from a master clock generator.† The clock pulse rate from this generator has a nominal maximum of 1 Mp/s, but this can be arranged to be much lower.

† Details of this are not included in the paper nor of the circuits to generate D0, D1 and D2 as these are largely determined by the nature of the input data peripheral. These circuits are quite conventional in design.

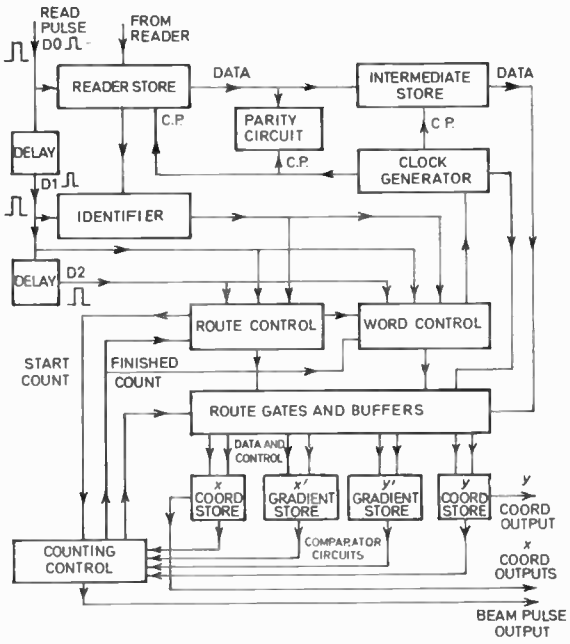


Fig. 2. Block diagram of the system.

This signal D0 causes the character in the reader to be fed in parallel into the reader store. This store is a conventional type of *clocked* shift register, the contents of which can be shifted out to the right by a sequence of eight clock pulses, and no detailed explanation of the operation will be given. The signal D1 causes the contents of the reader store to be examined, in parallel, by the identifier. The latter is simply a collection of coincidence gates, the output of a particular gate indicates the presence of a particular character or character type. The identifier establishes whether the character concerned is a digit or a control character and provides output signals in synchronism with one of the signals D1 or D2 to initiate appropriate action in other circuits. If the character is a null, or TC8, a *reader go* pulse is generated causing the input tape to advance one character.

The route control circuit (Fig. 3), which will be discussed in detail in Section 3, decides whether data which are to follow a control character are coordinates of a start point of a line, end point of a line, or gradient digits. This circuit operates by discriminating the order in which the SP, TC10 and TC9 characters follow an FE2 character.

The word control circuit (Fig. 4), which will be discussed in detail in Section 4, sorts the digit characters of the *x* and *y* words (coordinates) from the SP and the other control characters and controls the assembly of the *x* or *y* word in the intermediate store. This is a conventional twelve-bit shift register in which the word is assembled by serially shifting into it the

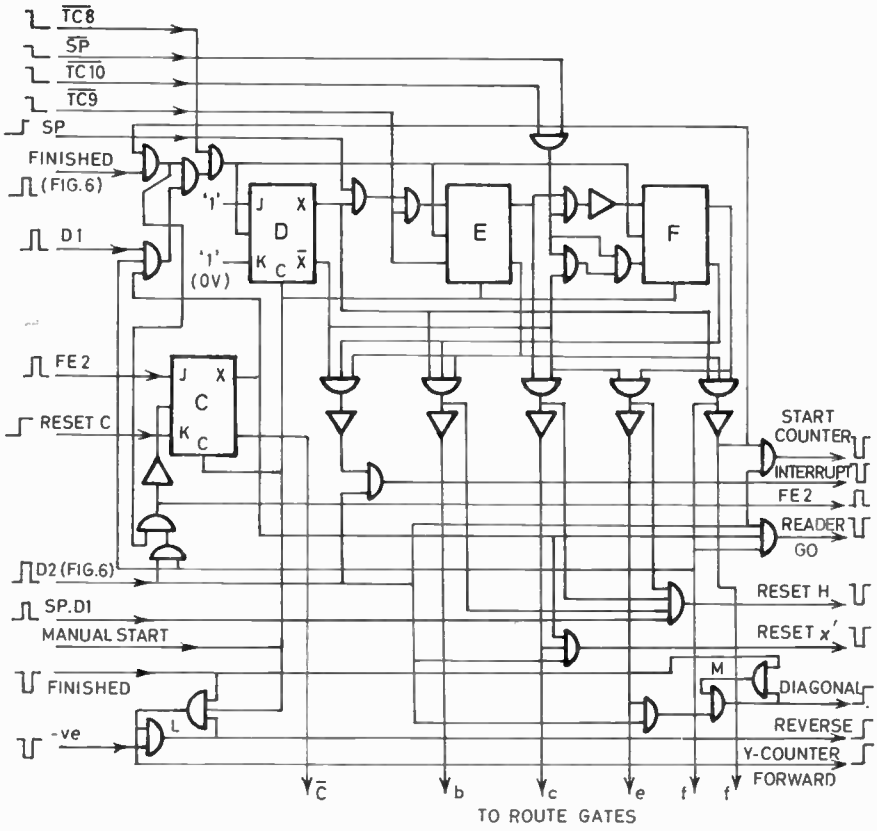


Fig. 3. Route control circuit.

three four-bit binary coded decimal digits from the reader store. This is possible because although there are eight bits in a single character, only the last four are needed to represent the decimal digit. When a complete x or y word is assembled, the word control circuit initiates the parallel transfer of the word from the intermediate store to the correct final store through appropriate routing gates which are enabled by the route and word control circuits. A clock generator (Fig. 5), which will be described in Section 5, is used to provide clock pulses, synchronized with pulses from the master clock circuit, for the transfer of data from the reader store to the intermediate store and from the latter to the final stores.

The final stores are of two kinds: those whose function is to hold a constant value, hereafter called reference registers, and those which are set to an initial value and subsequently count to final values as determined by the reference registers. These counting

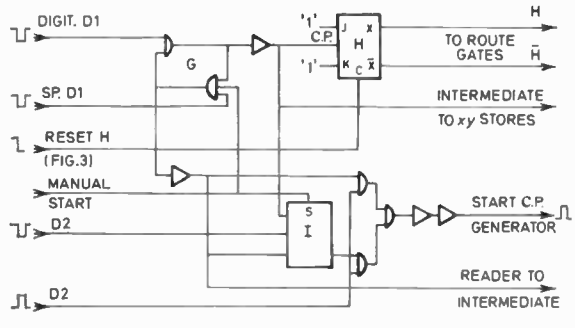


Fig. 4. Word control circuit.

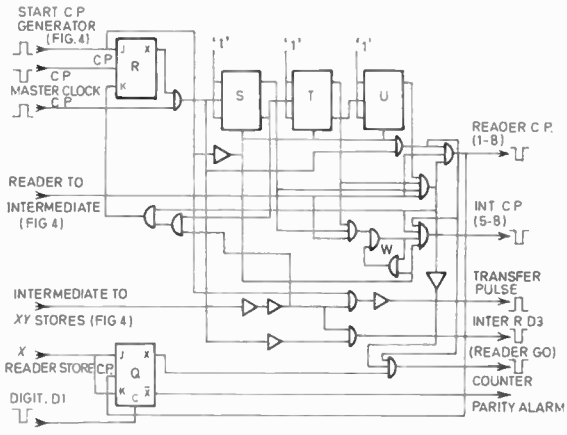


Fig. 5. Clock generator.

stores are subsequently referred to simply as counters. Two twelve-bit reference registers are used to store the x- and y- coordinates of the end point of the line and two twelve-bit counters to store the x- and y-coordinates of the current point of the line. Initially, the latter store the coordinates of the start point of the line and finally, at the end of the counting sequence, the coordinates of the end point of the line. The equivalence of the contents of the reference register and a counter is detected by a coincidence gate system referred to as a comparator. The assembly of the reference register, counter and comparator for one coordinate (x or y) will be referred to as a coordinate store.

The x-coordinate counter is unidirectional for any line can always be traversed in the positive x-sense. The counter for the y-coordinate is, however, bidirectional in order that lines of negative slope may be traversed. These stores are of conventional design and will not be described further.

Two gradient stores similar to the coordinate stores, each having a single decade reference register, counter and comparator are also required. These differ from the coordinate stores in that the initial values written into the counters are always zeros. The gradient digits take the place of the coordinates of the end-point of the line in the reference registers.

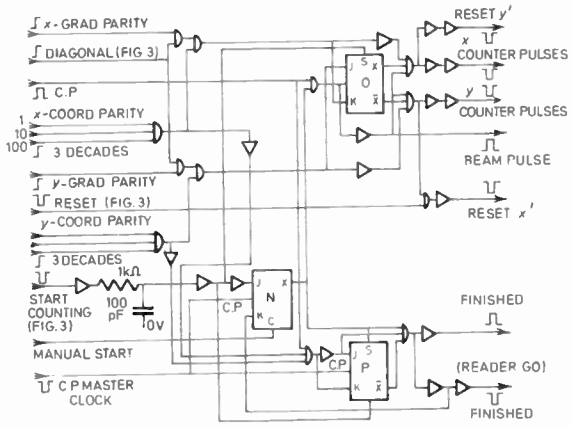


Fig. 6. Counting control circuit.

Under command from the counting control circuit (Fig. 6), to be described in Section 6, the x-gradient and coordinate counters count until the former is at parity with its reference register. The x-gradient counter is then reset. The y-gradient and coordinate counters then count until the former is at parity with its reference register, is then reset, and control returned to the x-counters. This procedure is repeated until both coordinate counters are at parity with their reference registers. This completes the traverse of the line being traced. Control is then returned to the route control circuit which then seeks further input data.

The route and word control circuits, the clock pulse generator and the counting control circuit, have unique features. These circuits will be described in some detail in the following sections.

3. The Route Control Circuit

The route control circuit is shown in Fig. 3. The function of this circuit has already been briefly explained in Section 2. The characters in the input format to which this circuit must respond are FE2 (newline) followed by either TC10 (penup), TC9 (antiherald), or SP (space). The latter character appears in place of the + (positive sign) character and always indicates that a new pair of coordinates or gradient digits are following in the input data. The fact that this SP character is preceded by the FE2 character is used to distinguish it from the other SP characters which appear elsewhere in the format as coordinate or gradient data word terminating spaces or as suppressed zero digits. The reading of an FE2 character always produces a *reader go* signal which causes the next character on the tape to be read. This is also true of a TC8 character.

Referring to Fig. 3, the FE2 character sets flip-flop C, at time D1,† thus opening gates which allow the D1 signal of the subsequent control character, TC10, TC9 or SP, to *clock* the flip-flops D, E and F. The flip-flop C is reset by the D2 signal of this control character unless the route control circuit is in state (f) as described below. The route control circuit has stable states (a), (b), (c), (d), (e) and (f) which are defined by the states of the flip-flops D, E and F as shown in Table 1.

This Table also indicates the outputs of the route control circuit in the various states. The first column of outputs in the table are pulse outputs in synchronism with the D2 signal which *clocks* the circuit and causes it to change state. The second column of outputs of the table are d.c. level outputs which are present for the duration of the state. In addition to the foregoing outputs, each time the route control circuit changes state (except when it switches to state (f)) a *reader go* output is produced which causes the next character on the tape to be read. A flow diagram which indicates the sequence of the states of the route control circuit is shown in Fig. 7. The operation of the circuit to give this sequence of states is explained in the following paragraphs.

† This is meant to imply in synchronism, that is, in AND function with the signal D1. This convention will be used subsequently without further explanation.

Table 1

State	Flip-flop outputs D	E	F	Output at time D2	D.c. (level) output
(a)	0	0	0	intermediate store reset	—
(b)	1	0	0	—	intermediate store to counters of coordinate stores (start coordinates of a line)
(c)	0	1	0	reset counters of gradient stores	intermediate store to reference registers of coordinate stores (end coordinates of a line)
(d)	1	1	0	—	—
(e)	0	0	1	set gradient flip-flop M	intermediate store to reference registers of gradient stores (gradient data of a line)
(f)	1	0	1	start counting	—

The route control circuit is set to state (a) by a *start* pulse, applied to the asynchronous resets of the flip-flops D, E and F, prior to reading any characters on the tape. This also causes the first character on the tape to be read. A blank tape character produces a *reader go* signal and the next character is then read. This will be repeated on any initial sequence of blank tape characters until the first FE2 character is encountered. As explained previously, this allows the D1 signal of the subsequent control character, which is a SP (see the format arrangement in Section 2), to switch the circuit to state (b). No further change of state can occur until another FE2 character is read later in the data sequence. In state (b) control is passed to the word control circuit which deals with the coordinate digits which follow the SP character. Note, however, that the switching to state (b) causes the first digit of the coordinate to be read. In a way which will be described in Section 4, the word control circuit causes the remaining digits of the starting point coordinates of a line to be read and the coordinate words to be assembled in turn in the intermediate store. The word control circuit also causes these coordinate words to be transferred from the intermediate store to the working stores, but it is the state (b) output of the route control circuit which opens the necessary gates to ensure that the words are transferred to the correct address, namely, the counters of the coordinate stores.

On completion of the transfer process, control is passed back to the route control circuit and any blank characters passed over until an FE2 character is encountered. The subsequent control character, a SP, switches the route control circuit to state (c). The gradient counters are also reset to zero as state (c) is entered. The word control circuit again takes over and operates as before but now the state (c) output of the route control circuit ensures that the end point coordinates of the line are transferred to the reference registers of the coordinate stores. Control then reverts to the route circuit.

The next FE2 character again enables the switching of the route control circuit by the following control character. If the latter is a TC10 or a SP, the route control circuit takes up state (f) and an output signal passes control to the counting control circuit (see Section 6). Note, however, that flip-flop C is not *reset* nor is a *reader go* signal generated: the control character, TC10 or SP, remains in the reader store. Either of these latter characters implies that no gradient data are to follow and hence the line to be traced is along one of the coordinate directions. The gradient counters are not used in these cases. As will be explained in Section 6, the counting control circuit then allows the appropriate coordinate counter to increase until there is parity between the counter and the reference register thereby generating, at the *master clock* rate, all the intermediate coordinates of the line between the start and end points. When parity between the counters and the reference register is established, a *finish* signal is generated which, since flip-flop C is still set, switches the state of the route control circuit. If the character in the reader store, left there from before the counting operation, is TC10, the route control circuit reverts to state (a) to await start and end point data for a new line. However, if the character in the reader store is SP, the route control circuit reverts to state (c) to await end point data for a new line, the starting point of which will be the end point of the last line. The finish signal also resets C and produces a *reader go* signal.

When the two pairs of coordinates for a line are to be accompanied by gradient data, the FE2 character of the last paragraph will be followed by a TC9 instead of a TC10 or SP (see data format in Section 2). In this case the route control circuit is switched from state (c) to state (d), an intermediate, no output signal, state. The FE2 and SP characters which precede the gradient data then cause the route control circuit to switch to state (e). As previously, the word control circuit then takes over to read the gradient data but the state (e) output of the route control circuit ensures that the

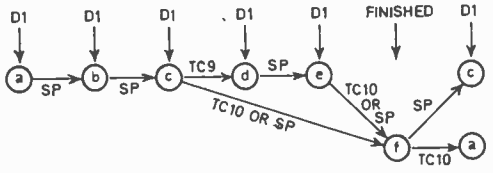


Fig. 7. State flow diagram of route control circuit.

gradient data are routed from the intermediate store to the gradient reference register. The gradient data are followed in the format by an FE2 and a TC8 character. These are required by the X-Y plotter which is used for checking input tapes and are not essential for the system being described. A *reader go* signal is generated by the TC8 character but the route control circuit is not clocked. The system simply looks for the next character. The next non-blank character will be an FE2 followed by a TC10 or a SP, either of which switch the route control circuit to state (f) to initiate counting just as explained at the end of the last paragraph. Of course, the counting is slightly more complex in this case since both the gradient and coordinate counters will be operating. The additional asynchronous flip-flops L and M in Fig. 3 are used in this latter connexion. The gradient flip-flop M is set as the route control switches to state (e) and its output is used to indicate to the counting control circuit (Section 6) that the gradient counters are to be used. The negative slope flip-flop L is set by − (negative) character which may appear in place of SP before the second gradient digit. The output of L controls the direction of counting of the *y*-coordinate counter.

4. The Word Control Circuit

The word control circuit is shown in Fig. 4. The function of this circuit has already been briefly explained in Section 2. When the identifier provides an input signal indication that a digit is in the reader store, the word control circuit must arrange to transfer this to the intermediate store and then cause further digits to be read and be transferred to this store. It must be able to recognize the two SP characters that terminate a word, that is an *x*- or *y*-coordinate or an *x*- or *y*-gradient digit. It also has to be able to interpret SP characters which precede digits, excepting those which follow an FE2 character, as non-significant zeros, and to write zero for those characters in the store. Further it must be able to separate *x*- and *y*-coordinate and gradient data. Finally, it must be able to initiate the transfer of assembled words in the intermediate to the working stores.

The operation of the circuit is as follows. The asynchronous flip-flop G is reset by the *start* signal and the flip-flop I is asynchronously set by the same signal. The flip-flop H is reset by the state (a) output of the route control circuit and the SP character which switches the latter to state (b) (see Fig. 3). In this, and also in states (c) and (e) (see Sect. 3) of the route control circuit, SP characters preceding digits characters applied to the flip-flop G (Fig. 4) cause no change in the state of the circuit. The reading of a SP character always produces a *reader go* signal, so that the next character may be read except in the special case when it follows an FE2 character and the route control circuit is in state (f) as explained in Section 3. When the first digit character is read the corresponding signal from the identifier at time D1 sets flip-flop G. This sets the output control line, marked *reader to intermediate*, which opens an output gate of the clock pulse generator (Sect. 5) thereby routing the clock pulses to the reader and intermediate stores. Once G is set, it opens a gate which allows the D2 signal, from the digit character which set G, to be sent to the clock pulse generator. This output pulse from the word control circuit is marked *start clock pulse generator* in Fig. 4. The trailing edge of the same D2 pulse also causes flip-flop I to reset. The clock pulse generator supplies the correct number of pulses to shift serially the four binary bits, corresponding to the decimal digit, of the character from the reader store to the intermediate store. Each succeeding digit pulse to the word control circuit produces a *start clock pulse generator output* which causes the binary coded decimal digit to be shifted serially from the reader store into the intermediate store. Previous decimal digits in the intermediate store are shifted farther along by the same clock pulses. The most significant decimal digit of a coordinate thus appears in the four most right-hand bits of the twelve-bit intermediate store. The intermediate store is reset to zero by the route control circuit prior to the reading of any digits (see Table 1). Also SP characters which represent non-significant zeros of a coordinate word do not produce *start clock pulse generator* outputs from the word control circuit. It follows therefore that these SP characters are not shifted into the intermediate store, but are represented by zero decimal digits in this store because of its initial resetting to zero. The suppressed zeros of a coordinate word are accordingly accounted for.

The first SP character following a digit character indicates that the end of the coordinate or gradient word has been reached. This SP character, at time D1, resets flip-flop G (Fig. 4), which in turn causes flip-flop H to toggle and also removes the *reader to intermediate* d.c. output and replaces it with one of the line marked *intermediate to xy-stores*. In this state, the output of flip-flop H opens route gates which ensure that *x*-coordinate, or gradient, word in the intermediate store is transferred to the *x*-coordinate, or to the *x*-gradient, store. In its other state, flip-flop H routes the contents of the intermediate store to the *y*-coordinate, or to the *y*-gradient, store. The D2 signal of the same SP character, which caused H to toggle, produces a *start clock generator* pulse through the gate on the output of the flip-flop I. The trailing edge of this D2 pulse sets flip-flop I, thereby preventing any *further start clock generator* pulses being produced by further SP characters. The *intermediate to xy-stores* signal and the *start clock generator* pulse together allow

the clock pulse generator (Section 5) to produce a single clock pulse which transfers in parallel the contents of the intermediate store to the x-coordinate store or to the x-gradient store as determined by the route control circuit.

The word control circuit now remains in the above state, ignoring SP characters, until another digit character is encountered. The preceding sequence of events is then repeated except that, at the time for the transfer of the word from the intermediate store, flip-flop H will have been toggled to the reset state and the word will be transferred to the y-coordinate, or to the y-gradient, store.

This completes the sequence of operation of the word control circuit for a pair of coordinates or gradient digits. The sequence is repeated for all such data pairs.

5. The Clock Generator

The clock generator circuit is shown in Fig. 5. The function of this circuit has already been largely explained. The generator is controlled by the input level lines *reader to intermediate* and *intermediate to xy-stores*, only one of which signals is present at any time, and by a *start clock generator* pulse, from the word control circuit (see Section 4).

The operation of the circuit is as follows. The *start clock generator* pulse sets flip-flop R and resets the counter comprising flip-flops S, T and U. The output of flip-flop R then opens a gate which allows clock pulses from the master clock generator to clock the counter. When the contents of the intermediate store are to be transferred in parallel to the final store, the single *start clock generator* pulse and the *intermediate to xy-store* signal are gated together to produce the single output transfer pulse to the appropriate routing gates. The next pulse from the master clock generator is gated with the output of flip-flop R to produce an output *reader go* signal. The trailing edge of the inverse of this master generator pulse resets flip-flop R, since there is no signal on the *reader to intermediate* output, this inhibiting further *reader go* pulses.

When data are to be shifted from the reader store to the intermediate store, a signal is present on the *reader to intermediate* input line from the word control circuit. The gates to the outputs marked *reader C.P.* and *intermediate C.P.* are normally inhibited by the absence of this signal. The *start clock generator* pulse, in addition to setting flip-flop R and resetting the counter, becomes the first of eight pulses on the *reader C.P.* output which are used to shift digits out of the reader store to the parity check part of the circuit. This *start clock generator* pulse also resets the asynchronous flip-flop W, thus inhibiting the output marked *intermediate C.P.* Pulses from the master clock now cause the counters S, T and U to operate and, for each of its states, the master clock pulses are passed by the gates to the *reader C.P.* output until each flip-flop in the counter is set, after which the output gates close. This provides the eight shift pulses for the reader store. These pulses are also used to clock the parity check flip-flop Q which toggles for each binary '1' at its synchronous inputs. Even parity at the end of the sequence of eight clock pulses allows a *reader go* signal to be generated, odd parity does not and produces an alarm signal output.

In the counting sequence, when flip-flops S and T have become set, the synchronous flip-flop W is set thus opening the gate to the *intermediate C.P.* output. This allows the last four pulses of the sequence of eight to appear on this output. These four pulses are used to shift the four bits of each digit character, corresponding to the binary coded decimal digit from the reader store into the intermediate store. Binary coded decimal digits already in the intermediate store are also shifted four bits to the right by each such sequence of four clock pulses.

When the sequences of clock pulses are finished, and the output gates have been closed, a reset signal appears on the synchronous reset of flip-flop R and this element is reset by the next clock pulse. The circuit then awaits the next *start clock generator* input pulse when the above sequence of operations is repeated.

6. Counting Control Circuit

The counting control circuit is shown in Fig. 6. The function of this circuit is, on receipt of a *start counting* pulse from the route control circuit as it enters state (f), to route clock pulses from the master clock circuit in proper sequence to the x- and y-coordinate and gradient counters. In describing the operation of the circuit, it will be assumed that the system is drawing a diagonal line for which gradient data have been supplied. Accordingly there will be a signal, from the route control circuit, on the input line marked *diagonal*. The operation when this signal is absent and the line to be drawn is parallel to one of the coordinate axes is more readily understood and will not be described.

The *start counting* pulse sets flip-flop N. The output of this flip-flop opens gates allowing pulses from the master clock circuit to clock flip-flop O and the appropriate coordinate and gradient counters. The *start counting* pulse also asynchronously sets flip-flop O and the clock pulses are routed to the x-counters of the x-coordinate and gradient stores through the output marked *x-counter pulses*. The gates on the corresponding output marked *y-counter pulses* are inhibited by the output of flip-flop O. When the contents of the counter and reference register of the

x-gradient store become identical, a signal marked *x-grad parity* is fed from this store to the counter control circuit and causes flip-flop O to reset. Subsequent clock pulses are routed through the output marked *y-counter pulses* to the counters of the y-coordinate and gradient stores. The x-counter pulse output line is then inhibited. In a similar way parity of the counter and reference register of the y-gradient store causes flip-flop O to set again and the clock pulses to be routed once more to the x-counters.

The procedure described in the previous paragraph continues until the contents of all decades of the counter and reference register of the x-coordinate store are identical. This store then provides signals on each of the three input lines marked *x-coord parity* to the counter control circuit. The presence of these three signals causes flip-flop O to be reset and prevents any further clock pulses being routed to the x-counters. A similar input arrangement from the y-coordinate store prevents further clock pulses being routed to the y-counter when the end point of the line being drawn is reached.

The *x-coord parity* and *y-coord parity* signals also set flip-flop P, which was initially reset by the *start counting* pulse. The output of flip-flop P resets flip-flop N, thus preventing any further clock pulses being applied to the counting control circuit, and also provides pulses on the output lines marked *finished*. The output of flip-flop N subsequently resets flip-flop P. These *finished* pulses are required as inputs to the route control circuit and in particular are used to switch the latter from state (f).

The output from the counting control circuit marked *beam pulse* provides a pulse, one clock pulse in duration, at each coordinate position along the line being drawn. For some applications it might be more convenient if this were a level output maintained for the total time required to draw the line. This could be provided with a simple modification of this circuit.

The delay circuit between the start counting input and flip-flop N is used to overcome timing difficulties which may occur when the line to be traced consists of a single coordinate point, that is when the start and end point coordinates are identical.

7. Constructional and Operational Features of the System

All units are arranged to be mounted in a standard 19 inch rack.

The supplies for the tape reader and associated control circuits are constructed as one unit. Supplies for the logic block are from three stabilized and protected commercial units (Farnell Ltd., Type 55B) and these are mounted to form another assembly.

The logic block is contained in one screened unit with external connexions via multi-way plugs and sockets. The r.t.l. elements are mounted on a commercial type of one-sided printed circuit board with end connectors and these fit on runners in an assembly with connecting sockets. Usually 24 r.t.l. elements are mounted per board and 31 such boards comprise the logic block.

Only those socket interconnexions carrying essentially continuous, or repetitive, signals are screened. Other interconnexions are routed in spaced groups according to their function.

The unit described, when allowance is made for those parts which have not been described in detail, comprises over 600 r.t.l. micrologic packages. Reliable operation over a period of almost two years in a somewhat noisy electrical environment has been achieved. This tends to refute the often heard remark that noise problems in large r.t.l. micrologic systems largely invalidate their use in such systems.

8. Acknowledgments

The authors wish to acknowledge a research award from the Science Research Council which enabled the apparatus described in this paper to be built.

Manuscript first received by the Institution on 23rd December, 1968 and in revised form on 5th December, 1969. (Paper No. 1324/IC24.)

U.D.C. 621.317.761:621.373.51.029.64

An Automatic Equipment for Recording the Frequency Variation of X-band Oscillators with Temperature over the Range −40 to + 70°C with particular reference to Gunn Oscillators

By

G. S. HOBSON,
B.A., A.Inst.P., C.Eng., M.I.E.E.†

and

F. L. WARNER,
C.Eng., F.I.E.E.‡

The Gunn oscillator under test is mounted inside an oven and has a thermocouple attached to it. The microwave output from it is fed, via a p-i-n diode leveller, into a microwave frequency discriminator with an almost linear range of 400 MHz. The outputs from the thermocouple and discriminator are fed to an X–Y recorder. This equipment operates with very little attention and it is suitable for making temperature coefficient measurements on large numbers of Gunn diodes. The theory of the frequency discriminator is presented, the experimental performance is shown on photographs and the sources of error are discussed.

1. Introduction

When a Gunn diode is operated in a high-Q waveguide cavity, the microwave signal that is generated is almost as stable, in frequency, as the output from a reflex klystron.[1] With this type of Gunn oscillator, the temperature coefficient is determined almost entirely by the coefficient of expansion of the cavity material and is about −170 kHz per degC at 10 GHz when the cavity is made of copper. Unfortunately, a high-Q Gunn oscillator of this type cannot be tuned electronically over a very wide range with a varactor. In many Gunn oscillator applications, an electronic tuning range of several hundred megahertz is needed and, in such cases, it is essential to use a low-Q cavity.[2] When this is done, the temperature coefficient varies considerably from Gunn diode to Gunn diode and, at X-band, using early samples of the type 106 CXY Gunn diode, it was found from extensive measurements that the temperature coefficient could lie anywhere between +0·5 MHz per degC and −3·5 MHz per degC. The reason for this very wide variation is not yet fully understood. In order to satisfy specifications placed upon Gunn oscillators, the frequency variation over the temperature range −40 to +70°C has to be known. Measurement of this characteristic 'by hand' with a wavemeter is very tedious and the labour involved in testing large numbers of Gunn diodes is economically impractical. To overcome this difficulty, a simple equipment has been designed which will carry out this task automatically.

† Department of Electronic and Electrical Engineering, University of Sheffield, Sheffield S1 3JD.

‡ Ministry of Technology, Royal Radar Establishment, Malvern, Worcestershire.

2. General Description of the Equipment

A block diagram of the complete equipment is shown in Fig. 1. The Gunn oscillator under test is mounted inside a blown air thermostatically-controlled oven which operates from −40°C (using solid carbon dioxide as a coolant) to +70°C. After one of the extreme temperatures has been reached, the oven controls can be set so that the temperature changes slowly without any attention to the other extreme. It was necessary to clamp the oscillator cavity to a sufficiently large thermal heat sink and to shield it from the direct air currents in order to maintain thermal uniformity over the cavity environment. A chromel alumel thermocouple with a sensitivity of about 40 μV per degC is used to measure the temperature of the Gunn oscillator and the output from this thermocouple is fed straight into the X-amplifier of an X–Y recorder.

The microwave signal from the Gunn oscillator is passed first of all through a ferrite isolator, which eliminates frequency pulling and frequency jumping. It is then fed into a p-i-n diode leveller which is adjusted to give a constant amplitude output regardless of frequency. This stabilized output is passed, via an absorption wavemeter, to a microwave frequency discriminator which produces an output voltage that is directly proportional to frequency over a range of 400 MHz centred on 9·5 GHz. Every Gunn diode that is tested in this equipment has its oscillation frequency set at 9·5 GHz by adjustment of the Gunn oscillator cavity, before the temperature cycling is commenced. The output from the diode detector in the frequency discriminator is applied to the Y amplifier in the X–Y recorder. Thus, a curve of the oscillation frequency versus temperature

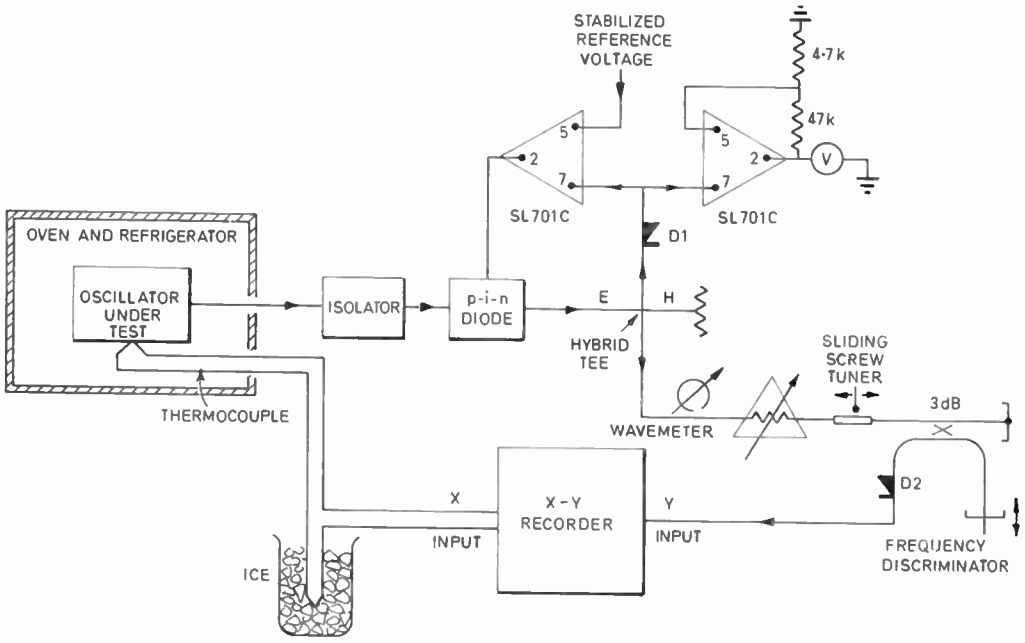


Fig. 1. Block diagram of the complete equipment.

is automatically produced by the X–Y recorder as the oven either warms up or cools down. It is a straightforward matter to set up the X and Y gain controls so that the sensitivities in the X and Y directions are 10 degC per inch (4 degC/cm) and 40 MHz per inch (16 MHz/cm) respectively.

3. p-i-n Diode Leveller

The p-i-n diode leveller generally follows standard practice so it will only be described briefly. Referring to Fig. 1, it can be seen that the microwave power emerging from the p-i-n diode is split into two halves by a hybrid tee. One half is fed into the microwave frequency discriminator and the other half is fed into detector diode D1. The output from this diode is applied to one input terminal of a type SL701C integrated circuit differential amplifier and an adjustable highly-stabilized reference voltage is applied to its other input terminal (see Fig. 2). Any difference between the detector output voltage and the reference voltage is amplified about 3000 times by the SL701C and is then used to control the bias current and hence the microwave attenuation through the p-i-n diode. The gain round this negative feedback closed loop is so high that the output from diode D1 is kept almost exactly equal to the stabilized reference voltage under all conditions. A high frequency oscillation in this closed loop was eliminated by connecting a transitional lag circuit between the first compensation point and earth and a 0·04 μF capacitor between the second compensation point and earth to provide the dominant lag.

The only requirement placed upon the hybrid tee is that it should divide the power in a frequency independent ratio between the two output ports. It is not necessary for it to have a frequency independent transmission characteristic. In order to select a suitable hybrid tee for use in this equipment, a microwave swept source was connected to the input of the p-i-n diode leveller and a second diode, which was accurately matched to D1, was placed on the hybrid tee output port that is normally connected to the frequency discriminator. The hybrid tee gave the best performance for this particular application when the input power was fed into the E arm. The hybrid tee that was chosen gave an output from the second diode which varied by less than 5% when the input signal was swept over a 1 GHz band centred on 9·5 GHz.

It is convenient to have a visual indication of the output from the p-i-n diode leveller so that one can be certain that it is working correctly. At first sight it only appears to be necessary to connect a moving coil meter in series with the load resistor of D1. However, the two diode detectors used in this equipment are a matched pair made by Hewlett-Packard (type X424A/01), and have high output resistances (3 kΩ to 20 kΩ) and therefore require high load resistances. Thus, to avoid the use of a very sensitive and hence expensive microammeter, a second type SL701C integrated circuit amplifier was connected to D1 (see Fig. 2). This second amplifier has its gain reduced to 10 by negative feedback and

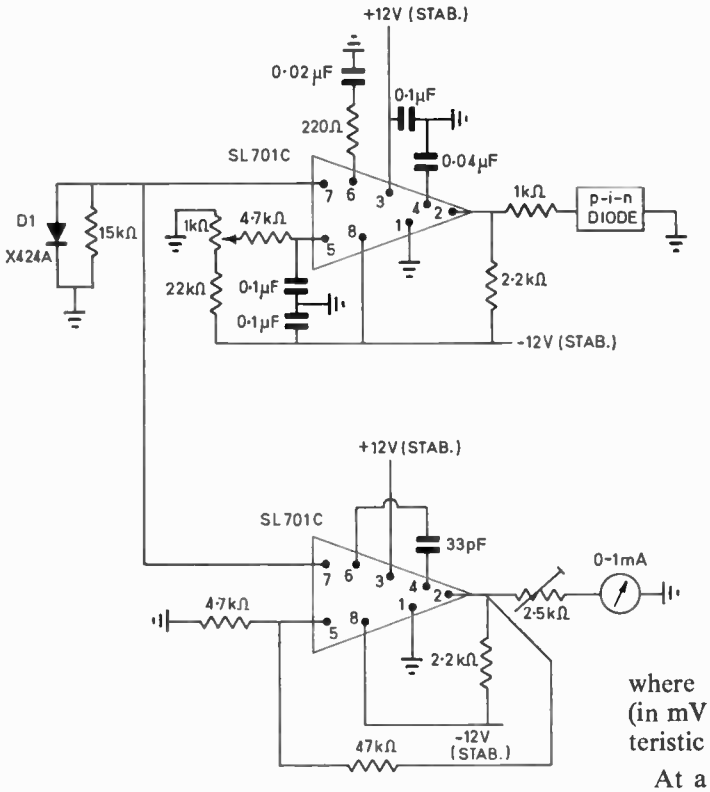


Fig. 2. Circuit diagram of the p-i-n diode leveller.

its output is connected to an inexpensive moving coil meter.

Taking 7·7 kΩ as a typical value for the output resistance of a type X424A diode, the other resistors in the input circuits were chosen so that the total resistance from each SL701C input terminal to earth is about 5 kΩ. This was done to minimize the offset voltages.

4. Frequency Discriminator

The microwave power that is fed into the frequency discriminator is divided equally between the two output arms of a 3 dB directional coupler. These arms have unequal lengths and one of them is terminated with a fixed short circuit while the other is terminated with an adjustable short circuit. Reflected signals from these short circuits are combined vectorially in the fourth arm of the 3 dB coupler which is terminated with a matched detector diode, D2. Let E denote the peak voltage which is sent into the frequency discriminator and let θ represent the phase difference between the two components, each of peak value $E/2$, which arrive at diode D2. Then assuming that this diode is operating within its square law region, the output voltage from it is seen to be

$$V_{out} = \frac{KE^2}{4Z_0}(1+\cos\theta) \qquad \text{.....(1)}$$

where K is the rectification efficiency of diode D2 (in mV per μW or similar units) and Z_0 is the characteristic impedance of the waveguide.

At a frequency, f, the phase difference, θ, is given by

$$\theta = \frac{2\pi f l}{V_p} = \frac{2\pi f l}{c}\{1-(f_c/f)^2\}^{\frac{1}{2}} \qquad \text{.....(2)}$$

where l is the total path difference between the two different routes through the discriminator, V_p is the phase velocity in the waveguide, c is the velocity of light and f_c is the cut-off frequency of the waveguide. Thus, if the frequency is varied over a wide range, it follows from equation (1) that V_{out} will oscillate up and down between the limits $KE^2/2Z_0$ and zero as shown in Fig. 3. Both K and Z_0 will vary to some

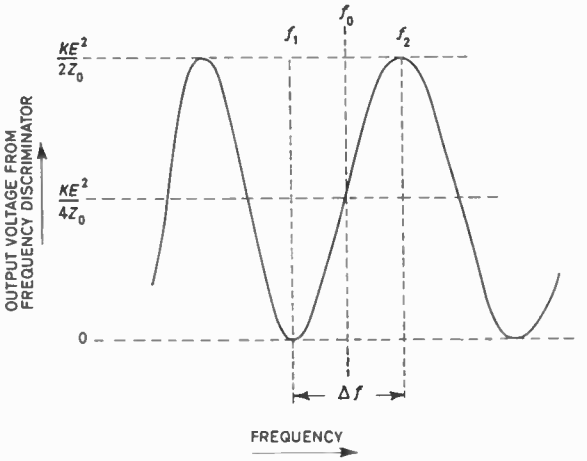


Fig. 3. Theoretical curve of the discriminator output voltage against frequency.

extent with frequency but, for simplicity, these variations are ignored in the following theory. Let us assume that the discriminator characteristic must be centred on a frequency, f_0, as defined in Fig. 3. Then, it follows from equations (1) and (2) that

$$\frac{2\pi l}{c}(f_0^2-f_c^2)^{\frac{1}{2}} = \tfrac{3}{2}\pi+2\pi n \qquad \text{.....(3)}$$

where n is an integer.

Equation (3) may be rearranged to give

$$l = \frac{c(1{\cdot}5+2n)}{2(f_0^2-f_c^2)^{\frac{1}{2}}} \qquad \text{.....(4)}$$

At the points of minima and maxima, adjacent to f_0, the respective frequencies f_1 and f_2 are given by

$$\frac{2\pi l}{c}(f_1^2-f_c^2)^{\frac{1}{2}} = \pi+2\pi n \qquad \text{.....(5)}$$

$$\frac{2\pi l}{c}(f_2^2-f_c^2)^{\frac{1}{2}} = 2\pi+2\pi n \qquad \text{.....(6)}$$

After squaring (5) and (6) and then subtracting them we get

$$f_2^2-f_1^2 = \left(\frac{c}{2l}\right)^2(3+4n) \qquad \text{.....(7)}$$

Let $f_2-f_1 = \Delta f$; then

$$f_2^2-f_1^2 = (f_2-f_1)(f_2+f_1) \simeq 2f_0.\Delta f$$

Therefore, substituting for l from (4), we get

$$\Delta f = \frac{f_0}{(1{\cdot}5+2n)}\left[1-\left(\frac{f_c}{f_0}\right)^2\right] \qquad \text{.....(8)}$$

Table 1 gives the values of l and Δf (calculated from equations (4) and (8) respectively) for six different values of n, when $f_0 = 9{\cdot}5$ GHz and $f_c = 6{\cdot}557$ GHz (the cut-off frequency of WG16 X-band waveguide).

Table 1

n	l cm	Δf MHz
2	12·00	904
3	16·36	663
4	20·73	523
5	25·09	432
6	29·46	368
7	33·82	321

An expression for the slope of the discriminator characteristic, dV_{out}/df, can easily be derived from equations (1) and (2) and theoretically, with perfect components, this slope is linear to within $\pm 5\%$ over a range equal to about 20% of Δf. When experimental work was carried out on this discriminator, it was found that a remarkable improvement in the linear range could be achieved by the insertion and careful adjustment of a variable attenuator and sliding screw tuner between the p-i-n diode leveller and the frequency discriminator. Using this technique it was found that a discriminator characteristic linear to within $\pm 5\%$ could be achieved over a range equal to 60% of Δf. Thus, to achieve the required linear range of 400 MHz, a value for n of 3 was chosen. The advantages gained by using a range equal to 60% of Δf are a larger output and a steeper slope, which tends to 'wash out' ripples in the characteristic. The attenuator and tuner were introduced, partly on intuitive grounds, for the following reasons. The attenuator damped any resonant behaviour owing to reflexions between the leveller and discriminator. Spurious ripples still remaining in the characteristic were reduced by careful adjustment and positioning of the slide screw tuner so that it introduced additional ripples of opposite 'phase' to the undesired ones and cancelled them out. It also increased the linear bandwidth in a similar way by introducing an opposite curvature to cancel that at the band edges of the uncompensated equipment.

Figure 4 contains three photographs of V_{out} versus f, which were obtained with a microwave swept source. Figure 4(a) was obtained with the discriminator connected directly to the p-i-n diode leveller. The irregularities in this curve were caused by multiple reflexions between the leveller and the discriminator and by other component imperfections. The insertion of a good quality ferrite isolator between these two units gave a discriminator characteristic which was more closely related to that predicted by the theory given earlier. Figures 4(b) and 4(c) show the linear range of $0{\cdot}6\Delta f$ which is readily achieved when the variable attenuator and the sliding screw tuner are inserted between the leveller and the discriminator, as shown in Fig. 1. Best results are obtained when the variable attenuator is set at approximately 3 dB. The pip near the centre of the characteristic in Fig. 4(c) was caused by the absorption wavemeter which enables the frequency calibration to be easily checked at any time to an accuracy of about 0·1%.

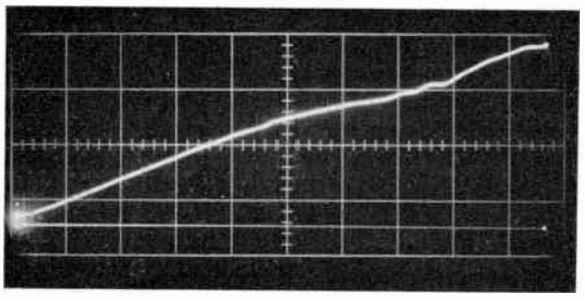
Various hybrid tees were tried out in the frequency discriminator but none of them would give a characteristic as linear as that achieved with the 3 dB coupler.

5. Accuracy

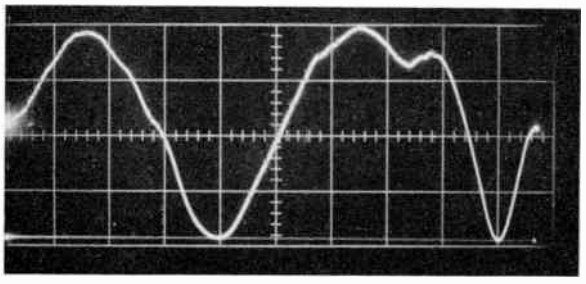
A detailed study was made of a typical curve of the discriminator output voltage against frequency over the range 9·3 to 9·7 GHz and the empirical formula which gave the best fit to this curve was

$$y = \alpha(f-f_0)+\beta\cos[2\pi(f-f_0)/280] \qquad \text{.....(9)}$$

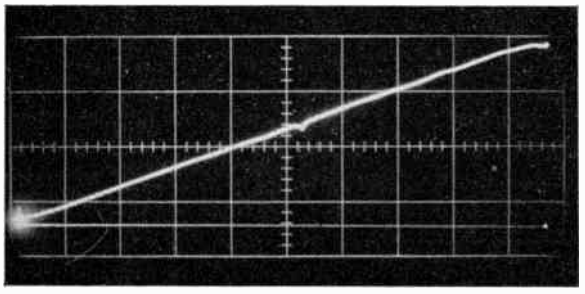
where y is in arbitrary units, f and f_0 are in MHz, $\alpha = 0{\cdot}008$ unit per MHz and $\beta = 0{\cdot}02$ unit. The



(a) Discriminator connected directly to the p-i-n diode leveller; sweep range 9·3 to 9·7 GHz.



(b) Variable attenuator and sliding screw tuner between the p-i-n diode leveller and the discriminator; sweep range 8·3 to 10·7 GHz.



(c) The same configuration as for (b) but with a sweep range of 9·3 to 9·7 GHz.

Fig. 4. Experimental curves of the discriminator output voltage against frequency.

slope of the curve given by this formula is

$$\frac{dy}{df} = \alpha - \frac{2\pi\beta}{280} \sin [2\pi(f-f_0)/280] \quad \ldots\ldots(10)$$

and the maximum percentage error in the slope due to the residual ripples is seen to be

$$\pm \frac{2\pi\beta}{280\alpha} \times 100 = \pm 5{\cdot}6\%$$

If a linear frequency scale is drawn along the Y axis of the recorder paper the maximum error in the relative recorded frequency, due to the residual ripples, is seen from equation (9) to be $\pm\beta/\alpha = \pm 2{\cdot}5$ MHz. This error will vary slowly with frequency and will have a half period of about 140 MHz.

A possible source of error in an equipment of this type is drift in the X and Y amplifiers which are built into the X–Y recorder. However, the recorder that is used in our equipment contains chopper-type d.c. amplifiers which have drift rates in the region of 1 μV per hour and the signals that are fed into them have peak magnitudes of a few millivolts; so the errors due to drifts should be almost negligible.

Changes in the ambient temperature affect the output from a microwave detector diode that is fed with a constant amount of r.f. power. However, in the equipment described here, the p-i-n diode leveller keeps the output voltage from diode D1 constant even when changes occur in the ambient temperature (provided that the reference voltage is unaffected by temperature changes) and, since D1 and D2 are a matched pair of diodes with similar temperature coefficients and are subjected to almost the same ambient temperature variations, there should only be small errors due to this cause.

6. Conclusions

This equipment operates with very little attention and the numerous frequency versus temperature curves that have been obtained with it have helped the development work on an improved type of Gunn diode.

7. Acknowledgments

The authors wish to thank Mr. R. G. T. Morris and Mr. P. Herman of R.R.E. for valuable help with this project and Professor M. H. N. Potok for suggesting the simplification of the mathematics of the frequency discriminator in Section 4.

Mr. G. S. Hobson gratefully acknowledges the support given by a Science Research Council Research Grant during the course of this work.

8. References

1. Court, W. P. N., *et al.*, 'Reduction of frequency-modulation noise from Gunn oscillators', *Electronics Letters*, 3, No. 13, pp. 567–9, December 1967.
2. Warner, F. L. and Herman, P., 'Miniature X-band Gunn oscillators'. Proceedings of the Cornell Conference on High Frequency Generation and Amplification, pp. 206–17, 1967.

Manuscript first received by the Institution on 16th January 1970 and in final form on 1st April 1970. (Paper No. 1325/IC25.)

U.D.C. 621.316.849

Prediction of the Stability of Thin-film Resistors

By

Professor

J. C. ANDERSON, D.Sc.(Eng.), Ph.D., C.Eng., M.I.E.R.E.†

and

Associate Professor

V. RYSANEK, Ph.D.‡

A relationship is derived between the contribution of defects to the resistivity of a thin film and the non-linearity of its $I-V$ characteristic. The latter is characterized by the 'third-harmonic index' (t.h.i.) of the film and it is shown that the initial value of t.h.i. is approximately linearly related to the change in resistivity over 1000 hours. It is concluded that the initial t.h.i. can be used to predict the stability of a thin-film resistor. Some qualitative interpretation of the variation of t.h.i. with time and resistivity is given in the light of the theoretical model.

1. Introduction

Resistor stability is of considerable importance in current electronics technology and particularly so in respect of thin-film resistors which are increasingly being used as high-precision components in micro-circuits. Unfortunately, to determine the stability of a resistor it has to be subjected to a life-test lasting up to as much as 10 000 hours, the change in resistance being measured at intervals during the test. It would be extremely convenient to have a parameter which, measured immediately after preparation of the film, could be used to predict the long-term stability of the resistor. In this paper, we demonstrate that the non-linearity of the resistor, as characterized by its third-harmonic index, is such a parameter.

2. Theoretical Basis

If the value of a thin-film resistor changes as ageing takes place, it is postulated that this will be due to some non-reversible physical or chemical processes. Obvious examples of such processes are annealing out of dislocations, diffusion of vacancies or impurities, recrystallization etc., all of which may affect the electrical resistance of the film. It is further supposed that each of these is an activated process which may be described by an Arrhenius type of expression[1] in which the reaction rate is given by

$$r = KNF \exp\left(\frac{-E_a}{kT}\right) \qquad \text{.....(1)}$$

where K = a material constant
N = the number of reacting particles
F = probability per second of the reaction occurring
E_a = activation energy
T = temperature in °K
k = Boltzmann's constant.

It is assumed that the annealing or other processes with which we are concerned will lead to loss of defects ('reacting particles') so that we may write

$$r = -\frac{dN}{dt} = \frac{KN}{\tau} \exp\left(\frac{-E_a}{kT}\right) \qquad \text{.....(2)}$$

where τ is a mean reaction time defined by $1/F$.

Integrating leads to

$$N_t = N_0 \exp\left(\frac{-bt}{\tau}\right) \qquad \text{.....(3)}$$

where N_0 is the initial number of defects and

$$b = K \exp\left(\frac{-E_a}{kT}\right) \qquad \text{.....(4)}$$

If we assume that the resistance R_D due to defects is proportional to the number of defects, N, then its value at any time t will be given by

$$R_D = R_0 \exp\left(\frac{-bt}{\tau}\right) \qquad \text{.....(5)}$$

where R_0 is the initial value of resistance due to defects.

Using Matthiessen's rule we may write, at any time t,

$$R_T = R_D + R \qquad \text{.....(6)}$$

where R_T is the total film resistance and R is the portion of it that arises from normal scattering processes and is independent of time. Thus

$$\frac{dR_T}{dt} = \frac{dR_D}{dt} = -\frac{bR_D}{\tau} \qquad \text{.....(7)}$$

and the stability of a resistance of given value is determined by the ratio b/τ. Just such an exponential dependence of resistance upon time as is given in equation (5) is often observed in ageing tests, but it is rarely exactly obeyed, especially during the first few hours of a test. This is not surprising since b depends on the activation energy of the defect concerned and it is unlikely that all those present are of the same type having the same value of E_a. Likewise, τ will generally differ for different types of defect. Thus any attempt to predict the long-term stability of a resistor by measurement of b/τ from the initial slope of a resistance/time curve is unlikely to be reliable. Accuracy improves as the length of time over which the test is extended increases and it is preferable to

† Materials Section, Department of Electrical Engineering, Imperial College, London, S.W.7.

‡ Formerly Visiting Research Fellow at Imperial College; now returned to the Czech Technical University, Prague.

extend ageing tests to 10 000 hours in order to assess the stability of a given type of resistor. It will be seen that only the slope of the resistance/time curve will yield information on b/τ; the actual resistance measured will always contain the constant contribution from ordinary resistivity. Thus a single initial measurement of resistance gives no indication of the likely stability of the component. To find a parameter which would do so we now examine our theoretical model further.

If the ith defect represents a barrier of ϕ_i volts to conduction electrons then, under thermal equilibrium, the current across the barrier in any direction will be given by

$$I_i = A \exp\left(\frac{-e\phi_i}{kT}\right) \qquad \text{.....(8)}$$

where A is a constant.

If a voltage V is now applied across the barrier the current I_i^+, in the direction of the voltage, will be

$$I_i^+ = A \exp\left(\frac{-e\phi_i + eV}{kT}\right)$$

and that in the opposite direction will be

$$I_i^- = A \exp\left(\frac{-e\phi_i - eV}{kT}\right)$$

Thus the net increase in current across the ith defect will be

$$I_i^+ - I_i^- = I_i = 2A \exp\left(\frac{-e\phi_i}{kT}\right) \sinh\left(\frac{eV}{kT}\right) \qquad \text{...(9)}$$

If there are N_t defects, the total current crossing defects will be given by

$$I_D = \sum_{i=0}^{N_t} I_i$$

For simplicity we assume, at this stage, that all defects are of the same type with the same value of ϕ.

Then

$$I_D = 2N_t A \exp\left(\frac{-e\phi}{kT}\right) \sinh\left(\frac{eV}{kT}\right) \qquad \text{.....(10)}$$

Expanding the sinh term and substituting for N_t from equation (3) we have

$$I_D = 2AN_0 \exp\left(\frac{-bt}{\tau}\right) \exp\left(\frac{-e\phi}{kT}\right) \times \times \left[\frac{eV}{kT} + \frac{e^3V^3}{3!(kT)^3} + \dots\right] \qquad \text{.....(11)}$$

Thus we see that the effect of the potential barrier type of defect is to introduce odd harmonic components into the current. Furthermore, the coefficient of each harmonic contains b and τ and is therefore a measure of these parameters.

Normal resistance will give a linear I–V relationship so that it is reasonable to attribute any measurable non-linearity to defects which present a potential barrier to the current carriers, as has been pointed out by Kirby.[2] By passing an alternating current of pure sinusoidal form the coefficient of the third-harmonic component can be measured and, on the above rather simplified model, this coefficient includes the parameters which affect resistor stability. It is therefore proposed that this coefficient could be used to predict the stability of a thin-film resistor.

3. The Third-harmonic Index

The total current i through a symmetrical non-linear element giving only odd harmonic distortion can be expressed by the power series[3]

$$i = \alpha v + \beta v^3 + \gamma v^5 + \delta v^7 + \dots \qquad \text{.....(12)}$$

where α, β, γ, δ are constant coefficients independent of voltage and v is the applied voltage at the fundamental frequency. If $v = V \sin \omega t$ and we expand the expression up to seventh order, the coefficient of the third-harmonic term is given by[2]

$$(\tfrac{1}{4}\beta V^3 + \tfrac{5}{16}\gamma V^5 + \tfrac{21}{64}\delta V^7) = V_3 \sin 3\omega t \qquad \text{...(13)}$$

If the term in β is much greater than any of the others we may write

$$\beta = 4V_3/V^3 \qquad \text{.....(14)}$$

where V is the applied peak fundamental voltage, and β is the coefficient of the third-harmonic component. If the fifth- and seventh-order terms are not negligible, however, we may write the third-harmonic voltage as

$$V_3 = DV^n \qquad \text{.....(15)}$$

where D is a constant and the exponent n will differ from 3 by an amount depending on the magnitude of the higher-order components. A typical form of non-linearity occurring in a film resistor is shown in Fig. 1 and is, in general, not purely cubic.

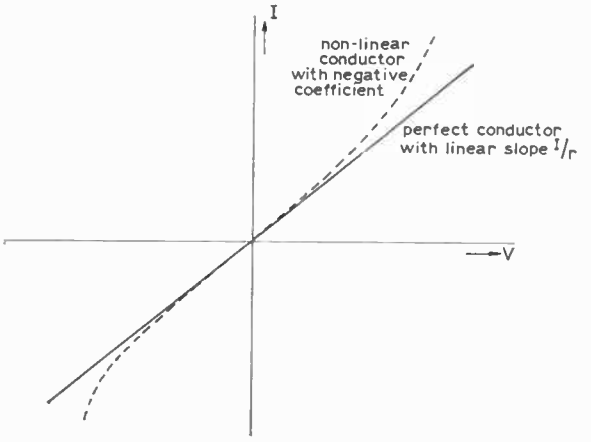


Fig. 1. Typical non-linearity of a thin-film resistor.

Kirby[2] has introduced a measure of non-linearity which he calls the third-harmonic index (t.h.i.) defined in a similar way to the familiar noise index.

$$\text{Thus, t.h.i.} = 20\log\frac{(\text{r.m.s. microvolts of 3rd harmonic})}{(\text{r.m.s. volts of fundamental})} \quad \ldots\ldots(16)$$

in decibels. Being a logarithmic unit, the t.h.i. may be expected, from the foregoing analysis, to be directly proportional to b, $1/\tau$ and ϕ and has therefore been used as a parameter in the present work.

4. Experimental Method

Two series of thin-film resistors were prepared by vacuum deposition on glass substrates at a pressure of 3×10^{-5} torr. The first series was of aluminium and the second of 80–20 Ni-Cr alloy. Contacts of silver were first fired on the substrates and the film was evaporated through a mask to give a width of 1 mm with a length of 16 mm between the contacts. The thickness was varied to obtain a range of 17 Ω per square to 220 Ω per square in the case of the aluminium and from 20 to 1700 Ω per square in the case of the alloy. The glass substrates used were microscope slides of soft soda glass and were cleaned ultrasonically in teepol solution followed by trichlorethylene vapour degreasing. The substrate temperature was between 25 and 35°C during evaporation. Some films were also prepared on cylindrical alumina ceramic substrates, but these did not show properties significantly different from those prepared on glass. Immediately after preparation, non-linearity measurements were made. The films were stored in the laboratory atmosphere and further measurements were made at intervals up to 1000 hours.

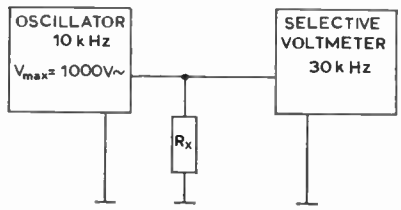


Fig. 2. Schematic diagram of the measurement apparatus.

The non-linearity measurements were made using a frequency sensitive voltmeter.† This generates a very pure sinusoidal current which is driven through the specimen and provides facilities for measurement of the voltage across it at the third-harmonic frequency. The fundamental frequency was 10 kHz which produced a voltage across the resistor that could be varied up to 1000 V peak to peak, depending on the resistor value. The third-harmonic voltage could be measured with a sensitivity of 0·01 μV. A schematic diagram of the system is shown in Fig. 2.

5. Results

For each measurement the third-harmonic voltage was plotted as a function of the fundamental voltage across the specimen and from the slope of this curve n was determined. This value was then used to evaluate t.h.i. at a working level of current such that the film was not overloaded.

5.1. *Aluminium Films*

Figure 3 shows the variation of n with resistance per square (referred to as surface resistivity) of the

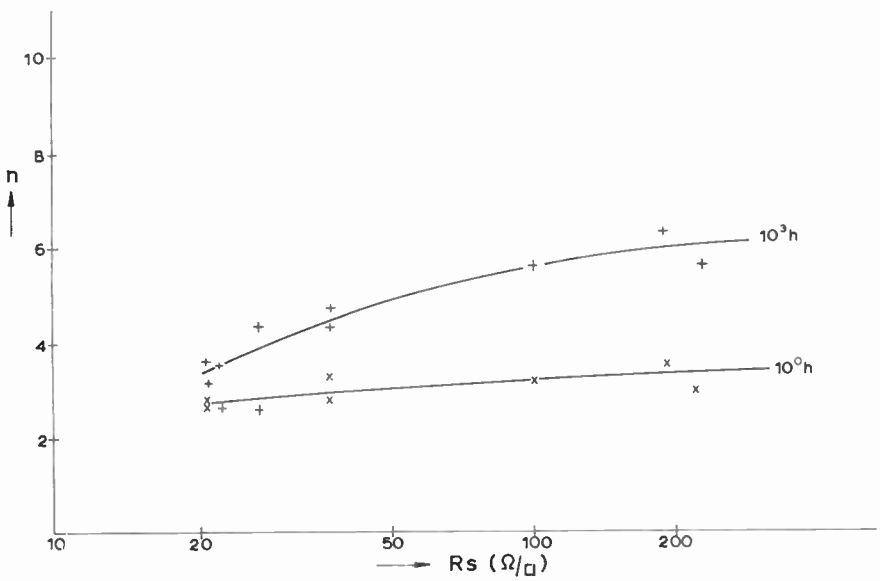


Fig. 3. The exponent n (equation (15)) as a function of surface resistivity for aluminium films at 1 and 1000 hours.

† Type CLT1a, Radiometer A/S, Copenhagen.

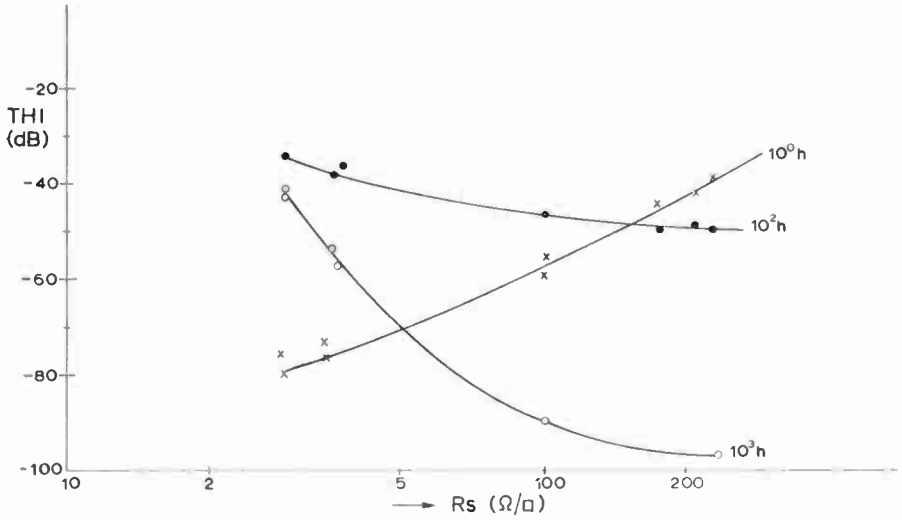


Fig. 4. Third-harmonic index (equation (16)) as a function of surface resistivity for aluminium films at 1, 100 and 1000 hours.

aluminium films. It will be seen that immediately after preparation $n = 2{\cdot}7$ to $2{\cdot}8$ for all specimens. At 1000 hours, however, n varies from 3·2 for low resistivity films to 5 for those with the highest resistivity.

In Fig. 4 the t.h.i. is shown as a function of film resistivity at 1, 100 and 1000 hours. There are seen to be marked changes in the t.h.i. value as the films age: in particular, t.h.i. tends to increase with time for low resistivity films and to decrease for high resistivity ones. In the medium range of resistivity t.h.i. at first increases and then decreases to a value below the initial one.

The fractional change in resistance $\Delta R/R$ expressed in percentage is plotted as a function of resistance for 10, 100 and 1000 hours in Fig. 5. These curves indicate the stability of the films. Assuming that the initial value of t.h.i. is a measure of the stability of resistance it can be used to predict the expected change in resistance during a life-test of a given resistor. The curve predicted in this way is shown dotted in Fig. 5.

The *initial* t.h.i. value is plotted in Fig. 6 as a function of percentage change in resistivity of all the films for 10, 100 and 1000 hours. The linearity of the graphs suggests that the initial t.h.i. has the predictive value suggested.

5.2. *Ni-Cr Films*

Figure 7 shows the variation of the exponent n with film resistivity in Ω per square for Ni-Cr films. For films below 300 Ω/square n has a value close to 3 both initially and at 1000 hours. For higher resistivity

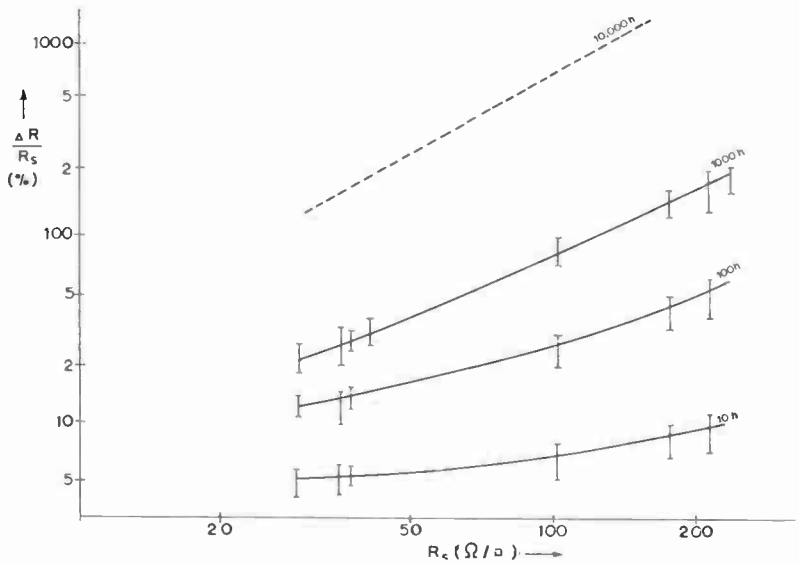


Fig. 5. Fractional change in resistance as a function of resistivity for aluminium films at 1, 100 and 1000 hours. The dotted curve is for 10 000 hours as predicted from the initial t.h.i. value.

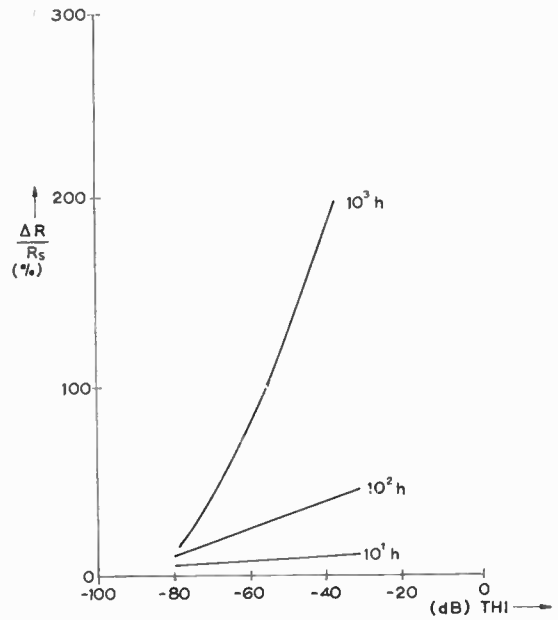


Fig. 6. Initial t.h.i. plotted against change in resistivity for all the aluminium films at 10, 100 and 1000 hours.

films n falls rapidly and is generally lower after 1000 hours.

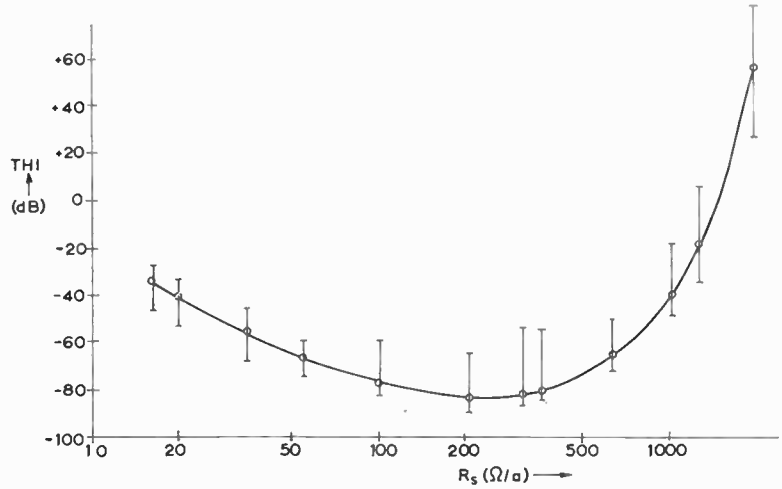
Initial t.h.i. is given as a function of resistivity in Fig. 8. There was considerable scatter in measured values for films of the same resistivity and the lines on this graph represent the spread of values obtained from 10 films. The t.h.i. is seen to rise markedly for thinner (high resistivity) films to values greater than zero. (It should be remembered that the third-harmonic voltage is expressed in microvolts whilst the fundamental is in volts.)

Figure 9 presents stability curves for Ni-Cr films and in Fig. 10 initial t.h.i. is plotted against the stability parameter $\Delta R/R_s$. For 10 and 100 hours the curves are fairly linear, again showing the predictive value of initial t.h.i. The 1000-hour curves depart from linearity for high values (> 0) of t.h.i. but give a considerable linear range.

6. Discussion of Results

From the theoretical model it was postulated that measurement of the third-harmonic coefficient immediately after preparation of the film would give a

Fig. 8. Initial t.h.i. as a function of resistivity for Ni-Cr films.



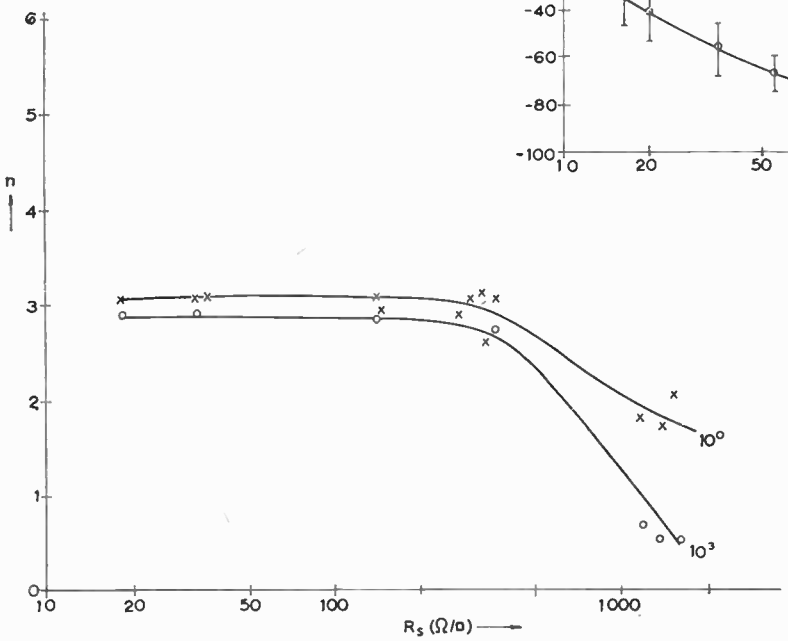


Fig. 7. The exponent n (equation (15)) as a function of surface resistivity for Ni-Cr films at 1 and 10 hours.

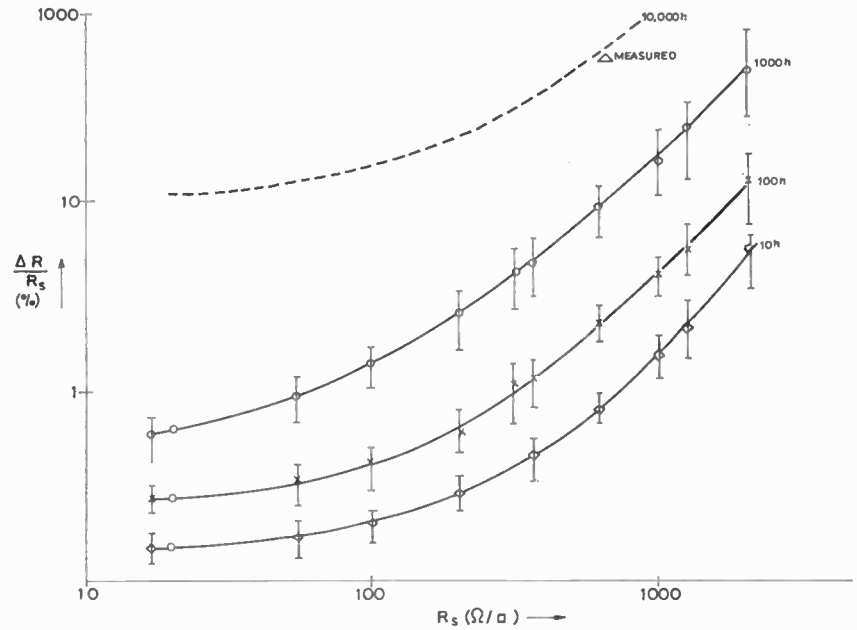


Fig. 9. Percentage change in resistivity as a function of resistivity for Ni-Cr films at 10, 100 and 10 000 hours from the initial t.h.i. value. The triangle is a single 10 000 hour measurement.

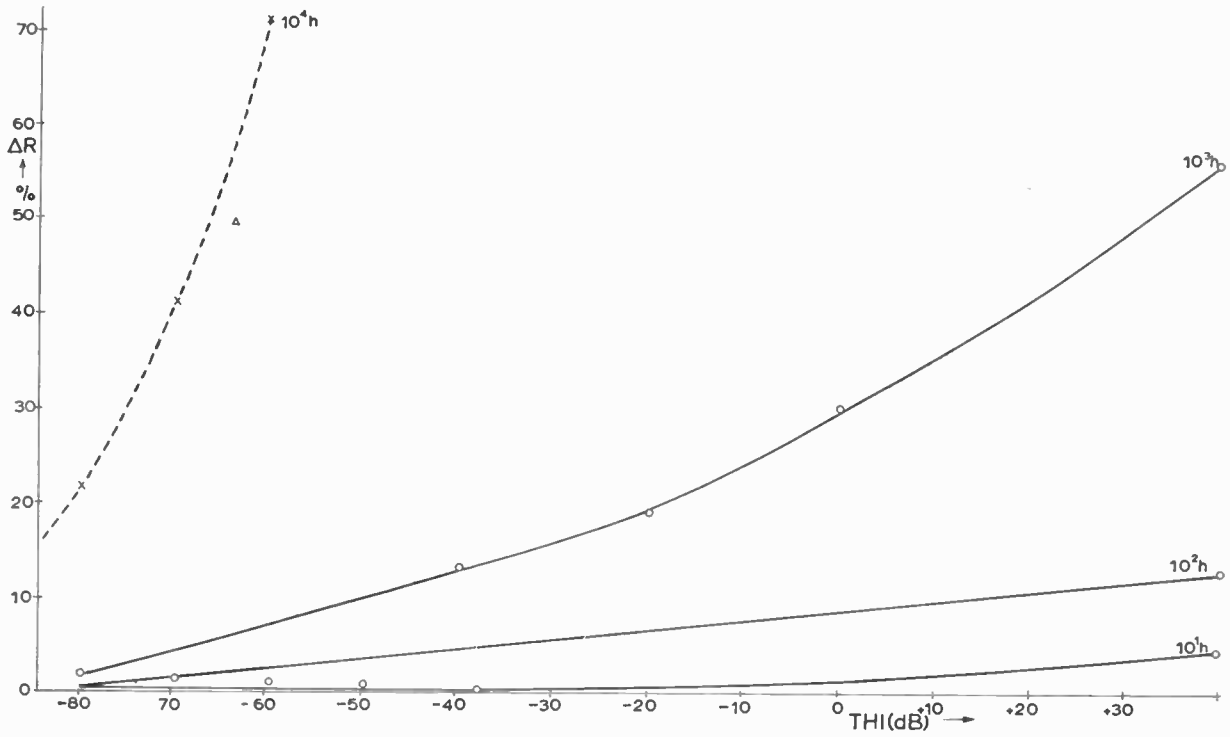


Fig. 10. $\Delta R/R_s$ as a function of *initial* t.h.i. for Ni-Cr films. The dotted curve is predicted for 10 000 hours from the t.h.i. measurements. The triangle is a single 10 000 hour measurement.

measure of the parameters b and $1/\tau$ which determine the stability of the film. The present, admittedly limited, experiments appear to support this view. The initial value of t.h.i. has been found to be reasonably linearly related to the change in resistance with ageing.

The variation of t.h.i. value with time and film resistivity has been found to be complicated. In the case of aluminium films, the initial t.h.i. increases as film thickness decreases. This would be consistent with a higher density of defects in the thinner films. Because of the low thickness, defects will be able to anneal out to the surface relatively easily so that, as is found experimentally, t.h.i. decreases with time. For the thicker films the t.h.i. was found to increase with time; in the absence of a thorough investigation of these films using an electron microscope it is impossible to explain this behaviour explicitly. It would, however, be consistent with clustering of defects as annealing proceeded, the actual proportion annealed out being small due to the relatively large film thickness. If this is correct, the initial increase followed by a decrease, observed in films of intermediate thickness, would correspond to initial clustering of defects, followed by annealing out of the clusters.

In the case of Ni-Cr films the thinner films appear to have a very high density of defects. The annealing out process occurs in all the Ni-Cr films since t.h.i. falls with time in each case.

The behaviour of the exponent n is somewhat complicated. From the theoretical model the coefficients of the various harmonics differ only by powers of e/kT and it is not, therefore, expected that n will vary with time or thickness. However, it is emphasized that the theoretical model is very simplified, and is based on the assumption of constant mean values of b, τ and ϕ. It is quite possible that any or all of these parameters may be voltage-dependent for some particular type of defect (for example a charged impurity). Thus the harmonic coefficients would be voltage-dependent to an extent depending on the preponderance of the particular type of defect. This would lead to variations of n with thickness since the higher resistivity films require a larger voltage across them to maintain the measuring current. It is considered impossible to explain in detail the experimental variations of n, which are observed, on the basis of the present simple theory.

7. Conclusion

It has been demonstrated that a direct relation exists between the third-harmonic index of a thin-film resistor, measured immediately after preparation, and the resistor's stability, at least up to 1000 hours. It is therefore considered that the t.h.i. is a useful predictor of the ageing characteristics of a film resistor. It is also a measure of the quality of the resistive layer, since a large value of t.h.i. indicates a large density of defects. It is believed that t.h.i. measurements, linked with structural studies could provide much useful scientific information on the contribution of different types of defect to electrical properties of films and could lead to an improved theoretical model of defect conductivity in metals. There seems no reason why the t.h.i. should not also be a predictor of the stability of thin-film capacitors.

8. Acknowledgments

One of us (V. R.) gratefully acknowledges the financial support of the British Council during this research.

9. References

1. Glasstone, S., Laidler, K. J. and Eyring, H., 'The Theory of Rate Processes' (Van Nostrand, New York, 1941).
2. Kirby, P. L., 'The non-linearity of fixed resistors', *Electronic Engineering*, 37, pp. 722–6, November 1965.
3. Peterson, V. and Harris, P., 'Harmonic testing pinpoints passive component flaws', *Electronics*, 39, No. 14, pp. 93–100, 11th July 1966.

Manuscript first received by the Institution on 2nd October 1969 and in final form on 9th January 1970. (Paper No. 1326/CC.80).

Contributors to this Issue

Professor J. C. Anderson (M. 1949) graduated at the University of London in 1951, where he subsequently gained his Ph.D. in 1960 and his D.Sc.(Eng.) in 1967. After three years at Electric and Musical Industries Ltd., he became a lecturer in telecommunications at Northern Polytechnic. In 1957 he went to the University of Witwatersrand, Johannesburg, as a senior lecturer in physics and later took up a research fellowship at Royal Holloway College, University of London, followed by a period with Laboratories RCA in Zurich. In 1961 he joined Imperial College, London, as a lecturer in the Department of Electrical Engineering. He became Reader in that department in 1962 and in 1965 assumed his present position as Professor of Electrical Materials.

Dr. V. Rysanek graduated in electro-engineering at the Czech Technical University, Prague, in 1952, after which he joined the research division for capacitors at the Research Institute for Electronics and Physics in Prague. In 1958 he took up a Research Fellowship at the Research Institute for Radio and Telecommunication, obtaining his doctorate from the Slovak University, Bratislava, in 1960. Currently, he holds the position of Associate Professor at the Czech Technical University where he is head of the division for technology in electronics. Dr. Rysanek has published more than thirty papers on his work in Czech, German and English, and he carried out the research for this present paper whilst spending a sabbatical year as a Visiting Research Fellow at Imperial College in 1969.

H. H. Guild received his B.Sc. degree in physics from Chelsea College of Science and Technology, London, in 1959. He subsequently studied noise in photomultiplier tubes at the Northern Polytechnic and joined the staff of Norwood Technical College as an assistant lecturer in Physics in 1962, transferring to Kingston College of Technology in 1964. Mr. Guild is at present a senior lecturer at Kingston Polytechnic, specializing in digital electronics.

Dr. S. H. Izadpanah studied at the University of Teheran, where he obtained the B.Sc. degree in physics in 1964. He subsequently studied in the Department of Electrical Engineering at University College, London, and was awarded an M.Sc. degree and the Microwave Diploma in 1966. He then went to the Department of Electronics and Electrical Engineering of the University of Sheffield and obtained a Ph.D. on the subject of the Gunn effect in semiconductors in June 1969. Since then he has been with the Department of Electrical Engineering of the Pahlavi University in Shiraz, Iran, where he holds a lecturership.

Dr. H. L. Hartnagel received the degree of a Diplom Ingenieur from the Technical University of Aachen, Germany, and the Ph.D. degree in 1964 from the University of Sheffield. After having worked for a short period with Telefunken in Germany, he joined the Institut National des Sciences Appliquées in Villeurbanne/Rhône, France. Since October 1961 he has worked in the Department of Electronic and Electrical Engineering, University of Sheffield, first as a senior research assistant, from October 1962 as a lecturer, and since October 1968 as a senior lecturer. Dr. Hartnagel has recently published a book, entitled 'Semiconductor Plasma Instabilities'. He has been particularly concerned with the development of ultra-fast logic with Gunn diodes and he and Dr. Izadpanah received the Institution's Charles Babbage Award for a paper on this subject which appeared in the *Journal* in 1968.

Dr. K. L. Hughes graduated in electronic and electrical engineering at the University of Birmingham in 1961. He was then granted a B.B.C. Research Scholarship, and in 1964, following work on parametric amplifiers, he received his Doctorate. Dr. Hughes then joined Ferranti Ltd. as a microwave engineer working on parametric amplifiers. In 1967 he transferred to the Semiconductor Division of the Company as section leader responsible for the development of transistors, and at the beginning of this year he was appointed head of integrated circuit development.

U.D.C. 621.382.2: 621.374: 681.325.5

Gunn-Effect Pulse and Logic Devices

By

S. H. IZADPANAH,
Ph.D.,†

and

H. L. HARTNAGEL,
Ph.D.‡

Further developments of high-frequency pulse and logic elements employing semiconductor bulk-effect devices are presented. Regeneration gain of high values has been achieved. The effects of circuit and device parameters have been investigated. Experimental and theoretical results are presented on a wide range of logic gates 'Exclusive OR', 'Inclusive OR', 'AND' and 'Inhibitor'. Designs for three more basic gates, namely, the 'Inverter', 'NOR' and 'NAND' are proposed. Further experimental results on high-speed transformation of analogue information into pulses are presented. A storage loop employing two Gunn devices has been developed.

List of Principal Symbols

C_n magnitude of domain pulse nth harmonic
E_a applied field
E_r sample rest field
E_s domain sustaining field
E_t threshold field
I_{do} domain pulse current
I_G current gain
I_p domain peak current
I_{pt} triggering pulse current
I_v low field (valley) current
K 'AND' threshold ratio
K_C comparator threshold ratio
K_I inhibitor threshold ratio
l device length
n carrier concentration
p ratio of load resistance to device resistance
P_G power gain
r ratio of resistance in series with device to the device resistance
R_d device resistance
R_L load resistance
R_s series resistance
S device cross-sectional area
T_d domain discharging time
T_f (saturated) domain total formation time
T_p triggering pulse duration time
T_t domain transit-time
V_a applied voltage
V_d domain excess voltage
V_p magnitude of triggering pulse voltage across the device
V_t threshold voltage
ε semiconductor permittivity
μ_l low field mobility
μ_n value of negative mobility
ρ material resistivity
τ_d dielectric relaxation time

† Formerly in the Department of Electronic and Electrical Engineering, University of Sheffield; now in the Department of Electrical Engineering, Pahlavi University, Shiraz, Iran.

‡ Department of Electronic and Electrical Engineering, University of Sheffield, Sheffield S1 3JD, England.

1. Introduction

It is well known by now that Gunn-effect domains[1-3] can be made to grow in such a short time that this makes domain devices highly suitable for pulse applications.[4, 5, 6] The sample nl product (n = the carrier density, l = length of domain trajectory) has to be high enough to permit complete growth of dipole domains. The domain properties and its dynamics have already been extensively investigated theoretically[3, 7-9] and experimentally.[10]

In this paper, experimental and theoretical results are described, which we obtained since our last publication in this *Journal*.[5] Although the feasibility of Gunn-domain logic was established in the latter paper, recent further results demonstrate a range of attractive features (e.g. high regenerator gain) and show the successful use of several pulse devices in series (e.g. the memory loop).

2. Results on Pulse Devices

In this Section, results are described on a range of device parameters, such as the rise-time and fall-time, shape and amplitude of output pulses.

2.1. *Gunn Diode as a Stable Pulse Generator*

A Gunn diode with a uniform cross-section and large nl product is subjected to an applied voltage V_a. In series with the device, a current-monitor resistor acts as the load, and the voltage developed across this resistor is fed to a sampling oscilloscope.

A recorded waveform of current vs. time for diode BG30 is shown in Fig. 1. The upper trace is the voltage across the diode and load resistor and the lower trace is the device current through a load impedance of 50Ω.

So far, the device under consideration has been assumed to have a uniform doping profile with a constant cross-section along its length, and hence, in general, to deliver rectangular output pulses. However, Shoji[11, 12] and Sandbank[13] reported several functional circuits and various waveforms to be generated either by modulation of doping density or

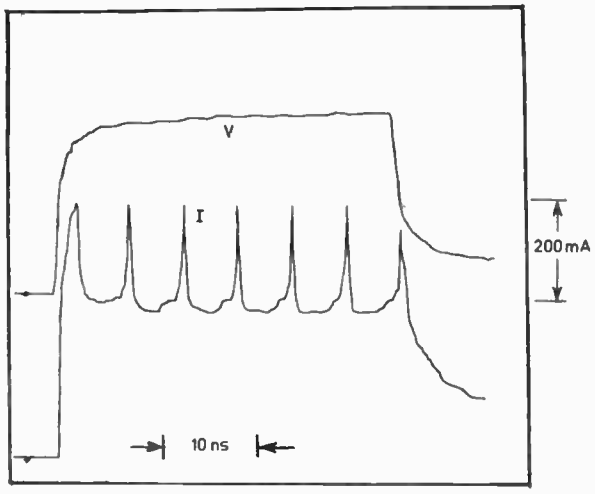


Fig. 1. Voltage and current waveforms for diode (BG30).

by introducing non-uniformity on the device dimensions. A simple example is a device with linear variation of its cross-sectional area (e.g. increase) from the cathode to the anode. The current would monotonically increase as the domain moves along during each cycle of oscillation, hence resulting in sawtooth-like output pulses. Figure 2 shows such a waveform which we obtained for a tapered device of length approximately 0·5 mm.

2.2. *Switching Time and the Effect of Loading*

In pulse applications, the rise and fall times of the pulses are always the primary parameters of concern. Hence it is essential to investigate these switching properties of Gunn-effect devices.

In a Gunn-effect pulse generator, the switching or the fall time T_f of domain pulse is defined as the time during which the current starts to decrease from the peak value I_p, and settles down to the constant valley current I_v. Similarly, the rise or discharge time T_d is the time taken for current to rise from I_v to I_p. For a fixed bias field, it is apparent that T_f is the time during which a domain grows to its full size from the initial fluctuations. For devices of high nl product, these times are very short. Several measurement techniques can be employed to obtain T_f experimentally. One method of investigating the variation of T_f as a function of parameters such as the load resistance is to measure the resulting pulse on a fast sampling oscilloscope. Unfortunately, the harmonic frequencies are usually too high for available sampling oscilloscopes and other experimental techniques have to be employed. An alternative method is described in the following.

Firstly, we assume that the formation and discharge process of domains can be expressed by an exponential function (some justification for this assumption is given by the experimental results of Kuru *et al.*[10]). Thus, the change in device output current, which is the consequence of such growth, also follows an exponential function. Hence, the output pulses are assumed to be flat-topped pulses with relatively short exponential rise and fall times. Therefore, the device current for one period of oscillation is given by

$$I(\omega t) = I_m \begin{cases} \dfrac{1}{e-1}\left[\exp\left(\dfrac{\omega t}{\theta}\right)-1\right], & 0 \leqslant \omega t \leqslant \theta \\ 1, & \theta \leqslant \omega t \leqslant \theta+\phi \\ \dfrac{1}{e-1}\left[\exp\left(\dfrac{2\pi-\omega t}{\theta}\right)-1\right], & \theta+\phi \leqslant \omega t \leqslant 2\pi \end{cases} \quad \ldots\ldots(1)$$

where

$$I_m = I_p - I_v$$

$$\omega = \frac{2\pi}{T_t}, \quad \theta = \omega T_f = \omega T_d, \quad \text{and} \quad \phi = 2\pi - 2\theta$$

The amplitude of the nth harmonic, when the above periodic waveform is expanded in terms of a Fourier series, is a function of the form

$$C_n = f(I_m, \theta, \phi)$$

The relation of C_n to the current transition angle θ allows one to determine the effect of the various parameters on θ, and in particular the domain growth rate. However, here, from the measurement of C_n, we wish to find the effect of different loads and applied bias on the domain total formation time T_f only. During the measurement, it is essential to ensure that the analysing circuit introduces no perturbation on the device operation. In practice, any degree of isolation

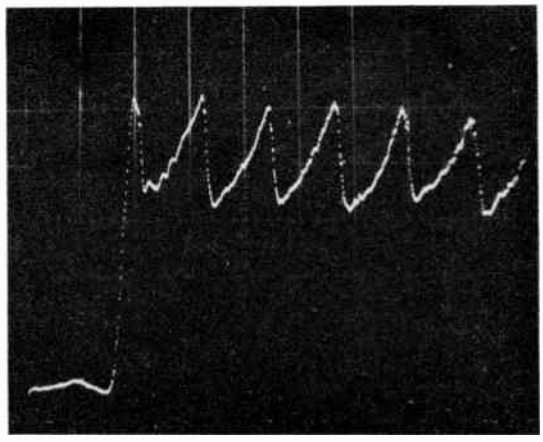


Fig. 2. Sawtooth waveform obtained from a tapered Gunn device.
Horizontal scale 5 ns/div. Vertical scale 0·2 A/div.

can be achieved by the insertion of sufficient attenuation between the two stages.

In order to observe the unperturbed oscillation, a high-impedance probe was used to monitor the device current through the load resistor and was displayed on channel A of a sampling oscilloscope. A high-Q re-entrant cavity was used to filter the desired harmonic. Figure 3 shows the transit-time waveform and some of its harmonics from a 0·5 mm long device which have been produced with the help of a sampling oscilloscope whose frequency waves covered the harmonics of interest. A wave with shorter transit times would of course not have enabled the successful recording of harmonics by a sampling oscilloscope and a different microwave technique would have to be used.

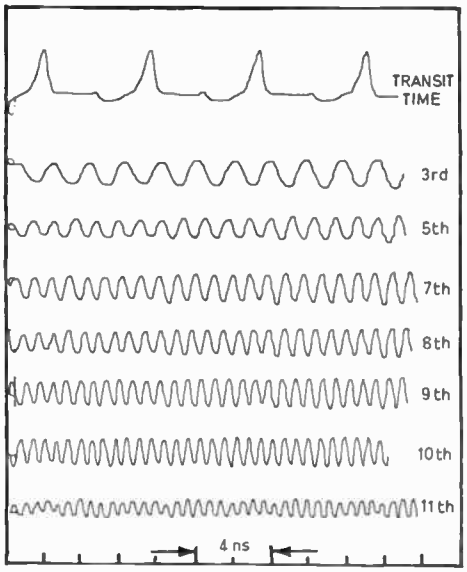


Fig. 3. Typical waveform of transit-time and some of its harmonics.

The amplitudes of the harmonics are not to scale in Fig. 3; they have been enlarged for higher harmonics in order to show that this technique is successful to at least the 10th harmonic. The device was operating into a 50 Ω resistive load with an applied bias of $E_a = 1{\cdot}32\,E_t$. In this case, the amplitude of the transit-time oscillation was 9 V. In addition to the amplitude variation of one selected harmonic, one can employ the rate of harmonic convergence in order to determine the accuracy of the exponential assumption of equation (1).

The measurements have been made with two diodes, BG30 and BG31, of 600 μm and 500 μm lengths respectively. The variation of T_f as a function of applied bias and load resistance is plotted in Figs. 4 and 5 respectively. The broken curves are for device BG30 for which $nl = 3{\cdot}21 \times 10^{13}\ \text{cm}^{-2}$. The solid

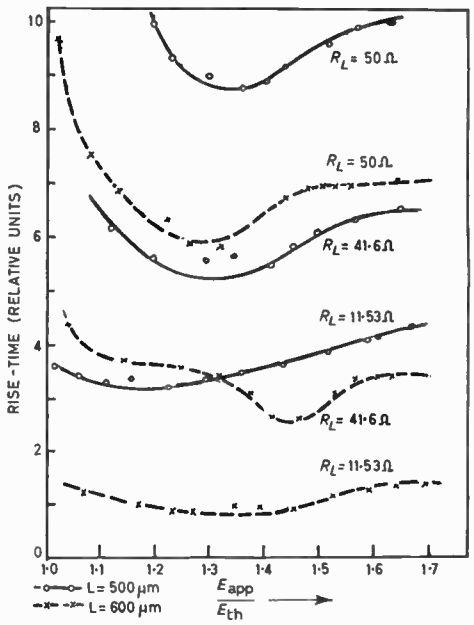


Fig. 4. Variation of domain pulse rise-time with applied bias.

lines belong to device BG31 having an nl product of $1{\cdot}8 \times 10^{13}$. The load values are quoted in the Figure for the proper curve. It is clearly seen from these results that there exists a definite change in transition angle θ due to the change of load. Also, a device with higher electron concentration and hence nl product, produces faster switching time when operating in the same load.

2.3. *Single Domain Mode* (*s.d.m.*)

The high field domain in GaAs once formed can continue to propagate, even if the applied field is decreased below the threshold field.[3, 6] Hence, the devices could be triggered to generate one cycle of operation.

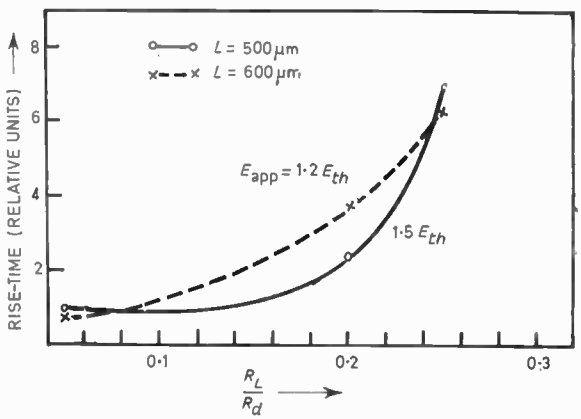


Fig. 5. Variation of domain pulse rise-time as a function of device load resistance.

Table 1
Specification of devices used in experimental investigation

Device number	Resistivity ρ Ωcm	Electron density n cm^{-3}	Mobility cm^2/Vs	Length l mm	Low field resistance R_d Ω
BG30	1·8	$5{\cdot}35\times10^{14}$	6470	0·600	200
GD27	1·95	$3{\cdot}7\times10^{14}$	5300	0·500	350
BG31	1·95	$3{\cdot}7\times10^{14}$	5300	0·500	400
AD38	1·95	$3{\cdot}7\times10^{14}$	5300	0·140	250
DA39	1·95	$3{\cdot}7\times10^{14}$	5300	0·500	620
DA40	1·95	$3{\cdot}7\times10^{14}$	5300	0·200	100
UB20	3·7	$3{\cdot}6\times10^{14}$	6100	1·000	120
DA37	1·95	$3{\cdot}7\times10^{14}$	5300	0·250	180
CB1	1·95	$3{\cdot}7\times10^{14}$	5300	0·300	210
CB7	1·95	$3{\cdot}7\times10^{14}$	5300	0·300	175

The s.d.m. can be realized by biasing the device at a level below the threshold field and introducing a small short triggering pulse of sufficient amplitude to the diode. Subsequently, the device field will momentarily be raised above the threshold value, causing the formation of a high field domain. This domain then continues to propagate when the triggering pulse disappears. The minimum values of bias field required

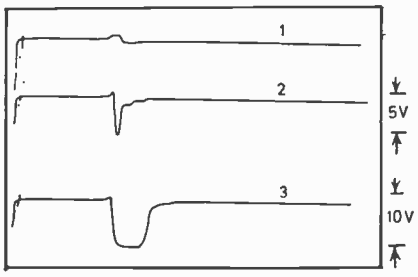


Fig. 6. Single domain mode of operation for two different devices.

to sustain a domain can be determined from the domain potential diagram.[3] The bias field, for reliable operation, should be chosen somewhat higher than the sustaining field.

A short triggering spike can be produced by several techniques;[5, 6, 10] when the device is operating under pulsed-bias condition, a convenient technique is the differentiating method. Typical recorded waveforms of s.d.m. for two diodes, BG31 and AD38, are shown in Fig. 6. The upper curve, trace (1), shows the triggering spike superimposed on the diode bias. Trace (2) is the domain pulse for AD38 of 1·4 ns duration, and trace (3) depicts a domain pulse of 5 ns duration for diode BG31. The value of load resistance was 50 Ω for obtaining these waveforms. The magnitudes of pulse voltages are shown in the Figure.

An important aspect of the single domain mode is its application for regeneration and reshaping of pulses. The shape of output pulse is determined by the device parameters, irrespective of the input pulse shape. This type of regenerator has inherent gain and operates at very high bit rates. It is, therefore, of great advantage for broadband systems.[14, 15]

Considerable regenerator gain has been predicted for the s.d.m. of operation,[16] and provisional experimental results were reported by letter.[17]

The maximum achievable gain is limited by the factor of how close the diode can be biased to threshold. The limit of bias level is set when the device electric field fluctuation in the nucleation region triggers a spurious domain and hence generates an unwanted pulse.

For the series types of pulse amplifier, we have carried out the measurement of gain with several devices working into different load resistances, and the values obtained are given in Table 2.

Table 2
Current and power gain obtained in single domain mode

Device number	Load resistance Ω	Domain current (I_p-I_v)	Current gain dB	Power gain dB
DA39	33·3	120 mA	20	7·6
	50	121	21·64	10
DA37	25	175	12·0	3·1
	50	160	8·6	2
BG30	50	300	14	10·4
DA40	25	380	20·24	13·1
	50	356	18·88	13·5

We have also measured the total single domain pulse voltage of several devices as a function of load resistance. The experiment has been carried out for the same bias field just near threshold for different loads. This, in principle, means that the diode experiences a field which is independent of the value of load resistance.

To measure the voltage pulse across a load resistance higher than 50 Ω, a Tektronix P6032 CF high-impedance active probe was used. The results of domain pulse amplitude measurements are shown in Fig. 7. It is interesting to note that a linear relation occurs between the domain pulse voltage and load resistance, as if the value (I_p-I_v) was independent of load resistance. One can show using Fig. 7 (whose

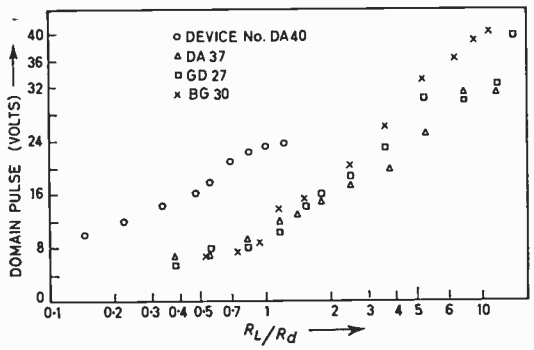


Fig. 7. The magnitude of domain pulse voltage for different values of load resistors.

R_e/R_d axis is logarithmic) that this is approximately correct, except for high resistance ratios, when the domain pulse seems to saturate. This would indicate that the linear relation does not apply in cases where the domain capacitance is not fully charged during half the transit time.[16] (The device lengths are given in Table 1.)

As mentioned earlier in this Section, the maximum achievable gain G_m is limited by electric field fluctuation of nucleating region inside the device. Thus, the ultimate value of gain depends upon the maximum possible applied bias to the device, $V_{B\,(max)}$, in order to obtain no domains whatsoever. However, the smallest pulse amplitude $V_{p\,(min)}$, which causes a definite domain formation, sets the required value of field change from a 'no domain state' to a 'reliable domain state'. In order to obtain an experimental limit to G_m, the bias voltage pulse was applied to a suitable integrating circuit, before it was given to the Gunn-effect element. In this way, the diode experiences a triangular-shaped bias-voltage pulse, where a domain could only be formed at the point of maximum bias field. Using a suitable filter, which permitted only the passage of domain pulses to either a monostable transistor multivibrator, or to an oscilloscope, the number of domains formed for, say, 1000 bias pulses could be counted when the bias voltage level was stabilized very accurately. These measurements were performed for small variations of bias level near the threshold value for domain nucleation. In this way, the level of bias voltage below which no domain is nucleated could be accurately determined. Equally, the required increase in bias voltage is obtained which gives reliable domain formation. From these results, the maximum power gain can be calculated for the 50 Ω load resistor, which was employed during these measurements. If this load resistor R_L is increased to larger values, a further increase in gain is to be expected. The limit of R_L is of course given by the reduction of domain growth time with load, as shown by Fig. 5.

The results of these measurements are summarized in Table 3, whose gain values are, of course, higher than the regenerator gains of Table 2, which presents the performance of regenerators responding to input signals superimposed on the bias voltage, as seen on Fig. 6.

Table 3

Experimental maximum pulse gain from Gunn-effect devices

Device number	$V_t/V_{p\,(min)}$	Load res. Ω	Maximum power gain	P_{Gm} for $R_L \to \infty$
BG30	73	50	24·25 dB	30·8 dB
UB20	23·21	50	16·5	21·27
BG31	80·02	50	22·45	32·0

3. Logic Modules and Elements

Since the power-frequency product of Gunn-effect devices is far above that of present conventional junction devices, logic circuits having much greater switching speeds and power handling capacity can be realized. This approach may be part of the answer to the present need for high-speed, high-capacity computers. Furthermore, the capability of bulk devices for handling and switching higher powers in shorter times makes them also very suitable for the future high-capacity communication systems.

Other advantages of bulk-effect devices are that by using a single chip of crystal, one can perform complex electrical functions (both analogue and digital), which at present require more discrete components or very complex integrated circuits.

3.1. *'Exclusive* OR' *and the Gunn-effect Inhibitor*

Two approaches to the Gunn-effect 'exclusive OR' (i.e. the comparator), namely (i) the single element (see Fig. 8(a)), and (ii) the two-diode comparator (see Fig. 8(b)), have already been reported.[5] The mechanism responsible for the function in the former relies on the control of the domain nucleation field through

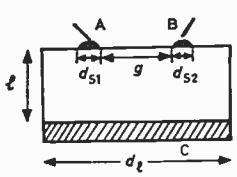


Fig. 8(a). A Gunn-effect comparator (triode).
A, B small electrodes as input terminals,
C large electrode (output terminal),
g distance between two small electrodes,
l sample length.

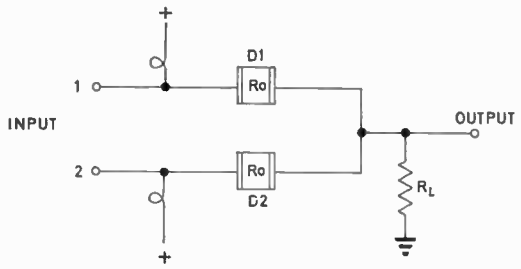


Fig. 8(b). Comparator circuit of two Gunn diodes in parallel.

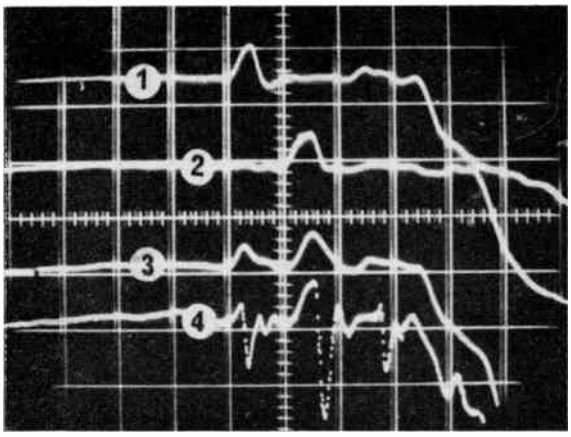


Fig. 8(c). Waveform obtained from two-diode comparators. Horizontal scale 5 ns/div.

an appropriate device geometry. In the latter, the comparator function is obtained due to the different amounts of current shared between the Gunn-element and the load, when one or two input terminals receive the signal.

An experimental waveform obtained for a two-diode comparator using devices CB1 and CB7 operating in s.d.m. is shown in Fig. 8(c). Traces 1 and 2 of this Figure show the triggering-voltage pulses applied to CB1 and CB7. The pulses are separated by a short delay time. Trace 3 is the current through a 50 Ω load resistor before any domain formation. When the level of triggering pulses was made large enough, one domain from each diode was produced as shown by trace 4 of the Figure.

Due to the complexity in the pulse-forming circuit employed, a second subsequent domain in diode CB7 has been triggered, which was caused by the spurious signal on trace 1 in the Figure. When the triggering voltage pulses were applied to both terminals simultaneously, no output domain pulse was detected. A convenient measure of the device performance is the threshold ratio K, which is defined as the ratio of the domain-nucleation threshold voltage with two input electrodes biased, to the threshold with one electrode only biased. The measured K (for 50 Ω load resistance) was 1·12.

A resistor R_s could be placed in series with one of the input terminals of either comparator to form an inhibitor gate, as has been described elsewhere.[5] It is of interest to determine the range of voltages over which the inhibitor function can be obtained. A resistive-network analysis gives the following inhibitor threshold ratios, which both have to be satisfied:

$$K_I = \frac{V_{B(1+2)}}{V_{B(1)}} = 1 + \frac{p}{(1+r)(1+p)} \qquad \text{.....(2)}$$

and

$$K_I = \frac{V_{B(2)}}{V_{B(1)}} = 1 + \frac{r}{(1+p)} \qquad \text{.....(3)}$$

Here $V_{B(1)}$ = threshold voltage for bias only at terminal (1);

$V_{B(2)}$ = threshold for bias only at terminal (2);

$V_{B(1+2)}$ = threshold for bias at (1) and (2);

$$p = \frac{R_L}{R_d}, \qquad r = \frac{R_s}{R_d}.$$

The inhibitor threshold conditions of equations (2) and (3) have been evaluated numerically for various ratios of p and r, and the results are plotted in Fig. 9.

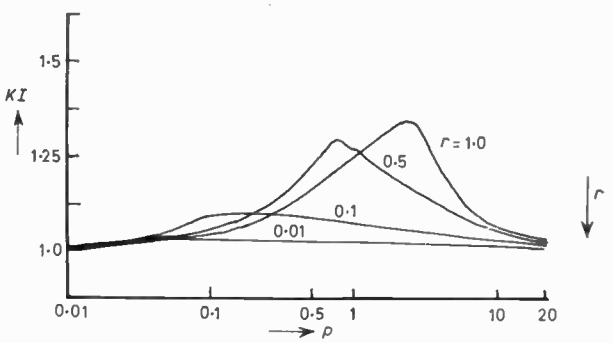


Fig. 9. The variation of 'Gunn-effect inhibitor' threshold ratio with r and p.

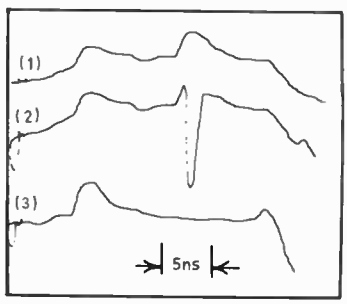


Fig. 10. Output waveform from an 'inhibitor' gate.

Experimentally, a series resistance of $R_s = 100\,\Omega$ has been placed in series with input 1 of the two-diode comparator described above. The same Gunn devices of CB7 and CB1 were used in order to operate the inhibitor in s.d.m. The current waveform at the output terminal before any domain formation is shown by trace 1 of Fig. 10. When the applied voltage was increased to the value of 124 V, a domain pulse was produced by the diode in branch 2 with no series resistor R_s, only. This is shown by trace 2 of Fig. 10. For simultaneous inputs to both terminals, for the same voltage, no output domain pulse was detected as seen by trace 3 in Fig. 10. However, as the voltage was increased to 134 V, a domain pulse, which was produced in branch 2, appeared at the output. Therefore, an experimental $K_I = 1{\cdot}08$ has been obtained, in comparison with the theoretical value of $K_{I(th)} = 1{\cdot}14$.

Another approach to the inhibitor circuit is shown in Fig. 11. The device consists of one Gunn-element in parallel with a resistance $R_s > R_d$ and the resistive load. For a sufficiently large voltage, an output domain pulse will be produced only if the signal is applied to terminal 1. No output occurs if the signal

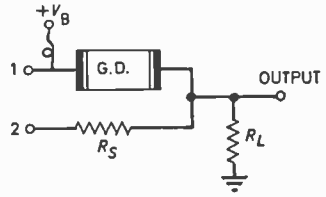


Fig. 11. Single-element Gunn-effect inhibitor.

is received either at terminal 2 alone, or at both terminals 1 and 2 simultaneously. In this circuit the output pulse is defined either by the pulse polarity or by a given amplitude, i.e. the output pulse from the diode is amplified, whereas for the same input pulse from branch 2, the output pulse amplitude is attenuated. The advantage of this circuit to the inhibitor of reference (5) is that instead of two Gunn diodes or a complicated three-terminal diode, one active element is used only, and hence the number of circuit components is reduced. Also, as is obvious, the range of voltage for which inhibitor action is achieved, can easily be chosen and increased by a proper choice of R_s.

3.2. AND *and* OR *Gates*

The 'AND' gate, described in ref. 5, and shown by Fig. 12, produces an output pulse when input signals are applied to its input terminals simultaneously. The application of the same voltage to one input only does not produce any domains.

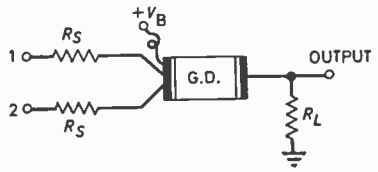


Fig. 12. Circuit diagram suitable for Gunn-effect AND, NOR and NAND gate.

We have constructed an AND circuit to operate in s.d.m. with device number DA40 of Table 1. Two 100 Ω microwave resistors have been employed in parallel before the input terminal and the device has been operating into a 50 Ω load resistance. The experimental waveform is shown in Fig. 13.

The trace 1 of the recorded waveform given in Fig. 13 shows the current pulses through the device. Trace 2 shows the device current when the two inputs have been applied simultaneously with a voltage across the device below V_t. When the voltage amplitude, in this case, was adjusted to 159·2 V, a domain formed in the device and appeared at the output (trace 3 in Fig. 13). The application of the same voltage to the individual inputs, as on trace 1, did not produce any domain pulses. However, when the voltage to one input was increased to 176 V, the device produced an output domain pulse. Hence, an experimental threshold ratio of $K_{exp} = 1{\cdot}1$ is obtained in comparison with the theoretical ratio of $K_{th} = 1{\cdot}25$.

An AND gate with more input terminals can also be constructed by an increase in the number of input resistances R_s. An OR gate may be constructed from the same circuit as an AND element. The condition for a circuit with two equal parallel input resistors is that the OR property results only if the applied voltage to the gates is:

$$V_a \geq V_t(1+p+r) \qquad \text{.....(4)}$$

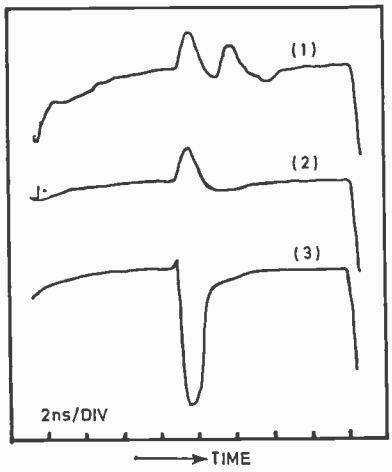


Fig. 13. Output waveform from a Gunn-effect AND gate.

3.3. *Inverting Gates*

3.3.1. The inverter

The function of this logic gate is such that there will be no output pulse if an input signal is applied to the gate and vice versa. The inverter circuit consists of a Gunn diode which is biased above the threshold voltage operating into a resistive load. The gate delivers domain pulses to the load when no input signal is applied. When a pulse of amplitude V_p and polarity opposite to bias is applied, the voltage across the device reduces below the threshold and domain production will be stopped.

3.3.2. NOR gate

For this logic gate, an output is expected only when none of the inputs receives a signal. A two-input circuit suitable for the NOR function is the same as Fig. 12. The bias field is assumed to be sufficient to produce output pulses when no input is applied. As soon as a pulse with opposite bias polarity of amplitude V_p is applied to either input or both inputs, the voltage across the diode drops and no output domain pulse is obtained.

3.3.3. NAND gate

The circuit shown in Fig. 12 is also suitable for a Gunn-effect NAND element with two-input terminals. The Gunn element here is also biased above the threshold field and a pulse is present at the output when there is no input signal or the signals applied to one input only. However, no domain pulse appears at the output when both inputs receive a pulse of amplitude V_p. The device bias and input pulse polarities are in opposition at the device anode.

4. Analogue-to-digital Conversion

In the single domain mode of operation, we showed that when a triggering signal is applied to a GaAs device with a bias level below the threshold field, it causes the formation of one domain. The duration of the triggering pulse has always been chosen to be less than T_t, the domain transit time. Therefore, after the discharge of a domain, no more domains are produced, since the total voltage across the device is no longer above the threshold voltage.

When the duration of input pulse is N times longer than the domain transit time, one obtains N domain pulses. Hence, the number of output pulses can be made proportional to the triggering pulse duration.

As a first approach, we applied an analogue voltage in the form of a step function to a differentiating circuit in order to obtain approximately-triangular pulses, whose total rise is proportional to the analogue amplitude. The triggering pulses produced by this method are superimposed on the Gunn-device bias voltage $V_B < V_t$. Using this technique, we obtained up to 12 output pulses with a 140 μm long diode.

A second approach was made by employing a Gunn diode of non-uniform cross-sectional shape, producing triangular output domain pulses as shown by Fig. 2. These pulses were applied to a second diode together with the analogue voltage and the bias voltage. For a low value of analogue voltage, the top part of the triangular pulse brings this second diode voltage above threshold for a short time and only one domain will be triggered. As the analogue voltage is increased, more of the triangular pulse lies above the threshold level, and there is time for more domains to be formed. Hence, a corresponding number of output pulses is produced. The operating concept is illustrated in Fig. 14.

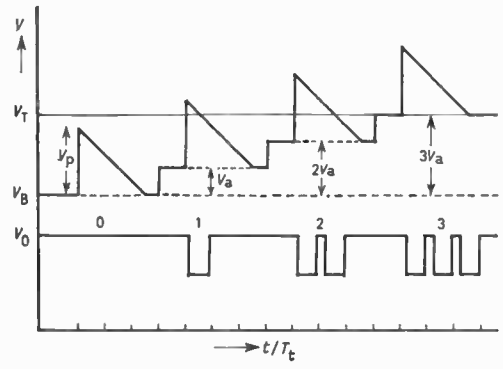


Fig. 14. Operation concept of two-stage Gunn-effect analogue-to-digital converter.

A maximum quantization of 17 has been obtained from device AD38 with the triangular pulse being produced by a pulse forming circuit. The waveform obtained from such converter is shown in Fig. 15. The first trace is the device input voltage pulse. The small dip on the bias pulse is a result of small discontinuity existing in the pulse forming circuit. At a total applied voltage of 56·5 V, the first domain appeared. The subsequent input voltage levels measured from the peak position of the input pulse are given in Table 4.

Table 4

No. of digits	1	2	3	4	5	6	7
Voltage amplitude (volts)	56·5	58·5	60·0	61·5	62·8	64·0	65·2
No. of digits	8	9	10	11	12	13	14
Voltage amplitude	66·2	67·4	68·2	69·0	69·7	70·3	71·0
No. of digits	15	16	17				
Voltage amplitude	71·5	72·0	72·4				

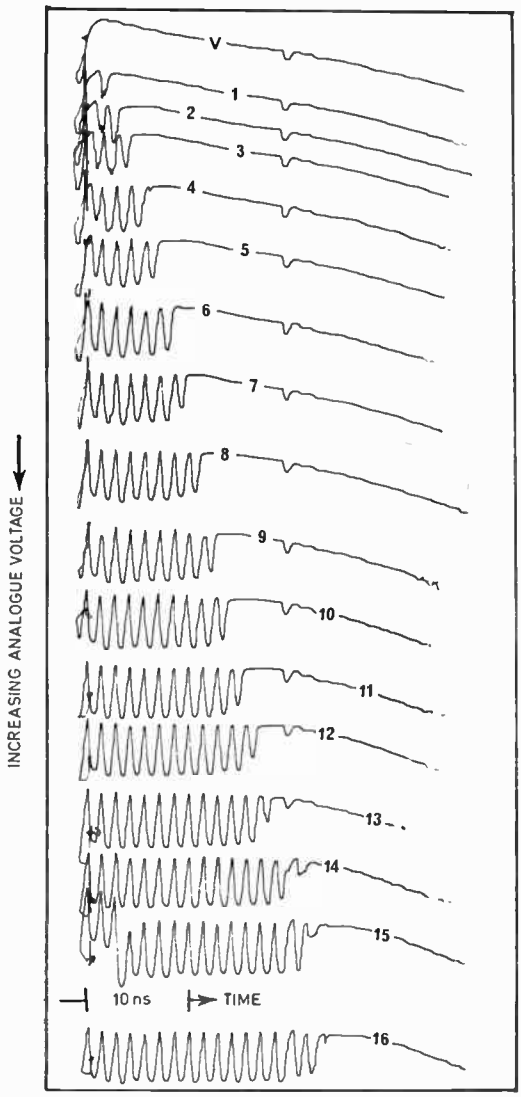


Fig. 15. Output waveform from a Gunn-effect analogue-to-digital converter.

5. Storage Loop

In a complex logic system where several devices and gates operate together, it becomes essential to determine the 'fan-in' and 'fan-out' of the individual elements. These factors, in general, are determined by the total permissible load value, and the device current and power gains. Experimental high pulse power gain obtained allows the achievement of a large 'fan-out'. High 'fan-in' is also possible since the device applied voltage can be increased far above the threshold (up to several times V_t before breakdown). A first investigation has to show that it is possible to trigger one Gunn-diode generator with the domain pulse of another diode. The successful operation of such a circuit was provisionally reported by an early letter.[20]

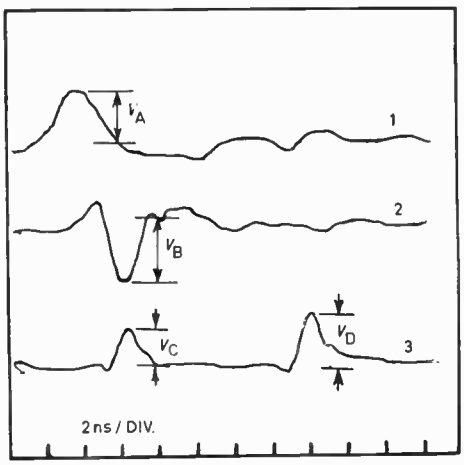


Fig. 16. Waveform obtained from a Gunn-effect storage loop.

A typical waveform obtained from a two-stage capacitively-coupled loop is shown in Fig. 16. In this Figure the pulse V_A in trace 1 is the input triggering pulse which is to be applied to the first Gunn-diode generator. Pulse V_B shows the output of this first diode which is then fed via a coupling capacitor to a second diode. The resulting domain pulse of the second stage is designated by V_C in trace 3. This pulse is applied back to the circuit input of the total two-regenerator chain via a coaxial feedback cable, and a further output signal can be observed at the output of the second regenerator after a given delay; this signal is designated V_D in trace 3 of Fig. 16. The signal is thus stored in the loop formed by the two regenerators and the feedback cable until the bias voltage at at least one of the regenerators is lowered sufficiently to avoid further domain nucleation. The circuit represents therefore the experimental verification of a storage cell, which was predicted in the earlier paper.[5]

6. Storage Element and Variable Frequency Pulse Generator

The frequency of operation for a Gunn pulse generator when it is biased above the threshold field is determined approximately by the diode thickness. A Gunn element can be made to generate pulses with variable repetition frequency if the set-up of Fig. 17 is

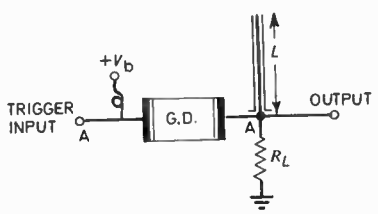


Fig. 17. Variable-frequency Gunn-effect pulse generator.

used. The circuit consists of a Gunn diode closely connected to the load resistance R_L and a length of coaxial transmission-line via a small T-junction. The line is open-ended and has a length L such that

$$2L \geqslant C I_t \qquad \text{.....(4.6)}$$

where C is the wave velocity in the line. The diode is biased below the threshold field and no oscillations occur in the absence of the triggering pulse. When a triggering pulse is applied, a domain pulse is produced at the point A′, travels along the line and is reflected from the open-circuit terminal back to A′. The arrival of the reflected current pulse at A′ causes the voltage between AA′ to be raised. If this voltage change becomes sufficient, another domain will be formed in the diode. This process will be repeated as long as the bias voltage is maintained across the device. Therefore, the circuit acts as a storage cell, in the same way as the above storage loop. A typical waveform obtained from diode DA40 is shown in Fig. 18. Trace 1 is the superimposed triggering pulse on the diode bias. One domain pulse of trace 2 represents the device behaviour when the transmission line was removed from A′. Trace 3 shows the resulting output when the line, of length $L_1 = 0{\cdot}5$ m is connected. If the length of line is increased to $L_2 > L_1$ and $L_3 > L_2$, traces 4 and 5 are obtained. Hence, one has a variable-frequency pulse generator. The maximum operating frequency here is also the device transit-time frequency.

It should be pointed out that the ratio of transmission line characteristic impedance Z_L to the value of load resistance R_L, determines the fraction of current pulse to be delayed in the line for the next operation. If this ratio is small, the reflected pulse current may not be sufficient for the required voltage swing across the device.

It is interesting to note that when $Z_L = R_L$, the amplitude of first output pulse is approximately half of the actual domain pulse. For the next few cycles, the wave had the nature of a growing wave and its amplitude growth will saturate at the value of true domain height after a number of operating cycles. This is because part of the reflected pulse current at point A′, in each early cycle, is added up to the new domain pulse, and half this new combined pulse is developed across the load. Obviously, the new travelling pulse to the line has also higher amplitude and hence makes a greater contribution to the load current in the next cycle. The rate of increase of the pulse amplitude in early cycles depends on values of Z_L, R_d and R_L.

7. Pulse Coincidence

An important point for reliable operating of Gunn-effect logic elements is the coincidence and synchronization of operating pulses. We investigated the coincidence problem for an AND gate. The operating pulses generally have finite rise and fall times. For an AND gate, if the sum of input pulses V_p together with the bias voltage V_B is just equal to V_a of equation (4) a domain is produced only if they are applied simultaneously, i.e. zero separation. On the other hand, if a small time delay T_s is introduced between the input pulses, the gate fails to show the AND property since the field in the diode no longer reaches the threshold level.

Hence, the maximum voltage resulting from the overlapping of input signals gives the value of required pulse coincidence, i.e. the permissible separation range given by T_s, which is a function of signal-pulse rise-time, the amplitude V_p of the signal and the AND threshold ratio K. Assuming that the input signal has the shape of a sine function with a duration equal to T_t at the half amplitude, a numerical analysis has been carried out for a bias voltage of $0{\cdot}75\ V_t$. The results are given in Fig. 19. The time and voltage axes have

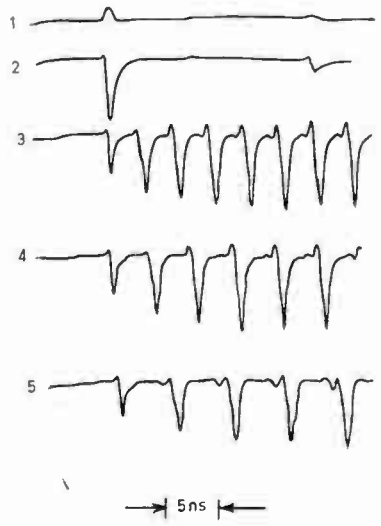


Fig. 18. Output waveform from variable-frequency Gunn-effect pulse generator.

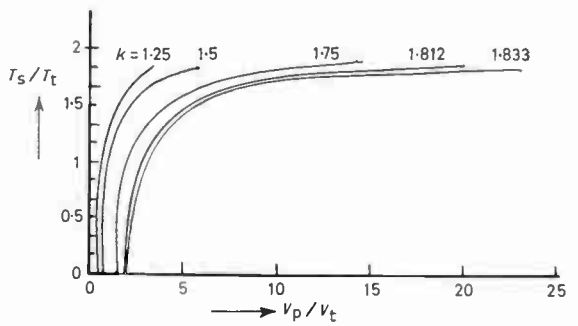


Fig. 19. Maximum allowed pulse separation to an AND gate as a function of applied pulse level.

been normalized to T_t and V_t for comparison purposes. Experimental results obtained with device DA40 for which $K = 1{\cdot}25$ are as follows:

V_p/V_{po}	1·37	1·5	1·75	1·82
T_s/T_t	0·33	0·5	1·51	1·60

where V_{po} is the magnitude of input pulse for zero separation.

8. Conclusions

New results on Gunn-effect high-speed pulse and logic devices have been presented. It has been shown that microwave pulse regeneration is possible with relatively high current and power gains. Experimental and theoretical investigations have produced further results of the following logic gates: 'Inclusive and Exclusive OR', AND and 'Inhibitor'. It has been found that reliable operation can be achieved by a proper choice of circuit and device parameters. A threshold ratio of 1·88 has been obtained for a three-terminal comparator. Circuits for further basic elements such as the 'Inverter', NOR and NAND are proposed.

A circuit which utilizes Gunn elements has been described for fast conversion of analogue information into digital form. Conversion levels up to 17 have been achieved. The possibility of two or more stages of interconnected Gunn devices has been examined and a storage loop employing two Gunn elements has been developed. The requirement of pulse coincidence has been investigated theoretically and experimentally. It has been shown that, with pulses having finite rise-times, the coincidence does not present a serious problem for the reliable operation of logic gates.

9. Acknowledgments

We would like to express our thanks to Professor P. N. Robson and Mr. G. S. Hobson of Sheffield University, and Mr. I. Bott of Royal Radar Establishment, for the benefit of several discussions on this study. One of the authors (S. H. Izadpanah) is grateful to the United Kingdom Ministry of Technology for financial assistance.

10. References

1. Gunn, J. B., 'Properties of a free steadily travelling electrical domain in GaAs', *I.B.M. J. Res. Dev.*, **10**, pp. 300–9, July 1966.
2. Hilsum, C., 'Semiconductor microwave generators', *Brit. J. Appl. Phys.*, (*J. Phys. D.*), **1**, Ser. 2, pp. 265–81, 1968.
3. Copeland, J. A., 'Stable space-charge layers in two-valley semiconductors', *J. Appl. Phys.*, **37**, pp. 3602–9, August 1966.
4. Copeland, J. A., 'Bulk negative-resistance semiconductor devices', *I.E.E.E. Spectrum*, **4**, pp. 71–82, May 1967.
5. Hartnagel, H. L. and Izadpanah, S. H., 'High-speed computer logic with Gunn-effect devices', *The Radio and Electronic Engineer*, **36**, pp. 247–55, October 1968.
6. Heeks, J. S., 'The mechanism and device applications of high field instabilities in gallium arsenide', *ibid.*, **30**, pp. 377–87, December 1965.
7. Kroemer, H., ' Non-linear space-charge domain dynamics in a semiconductor with negative differential mobility', *I.E.E.E. Trans. on Electron Devices*, **13**, pp. 27–40, January 1966.
8. McCumber, D. E. and Chynoweth, A. G., 'Theory of negative-conductance amplification and of Gunn instabilities in two-valley semiconductors', *ibid. ED*–13, pp. 4–21, 1966.
9. Butcher, P. N., Fawcett, W. and Hilsum, C., 'A simple analysis of stable domain propagation in the Gunn effect', *Brit. J. Appl. Phys.*, **17**, pp. 841–50, July 1966.
10. Kuru, I., Robson, P. N. and Kino, G. S., 'Some measurements of the steady-state and transient characteristics of high-field dipole domains in GaAs', *I.E.E.E. Trans. on Electron Devices*, **ED–15**, pp. 21–9, January 1968.
11. Shoji, M., 'Controlled bulk semiconductor current pulse generator', *Proc. I.E.E.E.*, **55**, pp. 710–1, May 1967.
12. Shoji, M., 'Functional bulk semiconductor oscillators', *I.E.E.E. Trans. on Electron Devices*, **ED–14**, pp. 535–47, September 1967.
13. Sandbank, C. P., 'Synthesis of complex electronic functions by solid-state bulk effects', *Solid-State Electronics*, **10**, pp. 369–80, May 1967.
14. Engelbrecht, R. S., 'Bulk effect devices for future transmission systems', *Bell Lab. Record*, pp. 192–300, June 1967.
15. Hartnagel, H. L. 'Gunn-effect pulse code modulation', *Archiv elektr. Übertragung*, **22**, pp. 225–9, 1968.
16. Hartnagel, H. L., 'Theory of Gunn-effect logic', *Solid-State Electronics*, **12**, pp. 19–30, 1969.
17. Izadpanah, S. H. and Hartnagel, H. L., 'Pulse gain and analogue-to-pulse conversion by Gunn diodes', *Electronics Letters*, **4**, No. 15, pp. 315–16, July 1968.
18. Copeland, J. A., Hayashi, T. and Uenohara, M., 'Logic and memory elements using two-valley semiconductors', *Proc. I.E.E.E.*, **55**, pp. 584–5, April 1967 (Letter).
19. Hartnagel, H. L., 'Digital logic-circuit applications of Gunn diodes', *ibid.*, pp. 1236–7, July 1967.
20. Izadpanah, S. H. and Hartnagel, H. L., 'Memory loop with Gunn-effect pulse diodes', *Electronics Letters*, **5**, p. 53, 6th February 1969.

Manuscript first received by the Institution on 28th July 1969, in revised form on 5th November 1969 and in final form on 11th February 1970. (Paper No. 1327/CC81.)

Contributors to this Issue

Roger W. Cooper received the B.Sc. degree in physics of the University of London in 1962. He has since been employed in the Solid State Physics Division of Mullard Research Laboratories. He has specialized in the field of magnetism of oxide materials, in particular the magneto-optic properties of these materials and their application in devices.

John L. Page went into the coal industry on leaving school, working for 1½ years in a chemical research laboratory. This was followed by 5½ years research on white ceramic dielectrics for capacitors. Since 1955 he has been with Mullard Research Laboratories working on magnetic ceramics, principally the production of single crystals of ferrites and iron garnets.

Henry Giles served during the war with the Royal Artillery and Royal Electrical and Mechanical Engineers. He received technical training at the Military College of Science and the Bell Telephone School for War Training in the U.S.A. and from 1943 to 1946 was seconded to the Air Defence Research and Development Establishment, Malvern (now R.R.E.), to work on air defence radar systems. Entering the electronics industry in 1947, Mr. Giles spent 12 years with Kelvin and Hughes Ltd., engaged in the development of marine and airborne navigation equipment. After a short period with the Plessey Company Ltd., he joined Astaron Electronics Ltd. in 1960, as Technical Manager, and was appointed Technical Director of the Astaron-Bird Group in 1963, controlling the development of a diverse range of electronic products, including echo-sounding and marine radar equipment. He returned to the Plessey Company Ltd. in 1965 to start the Marine Products Division of Plessey Radar Ltd. Subsequently, he managed the evolution of an advanced concept in marine radar designed specifically for the export market.

Frank L. Warner joined the Telecommunications Research Establishment (now the Royal Radar Establishment) as a laboratory assistant in 1942. He has been at Malvern since that date and is now a principal scientific officer in the Microwave Standards Division. After joining T.R.E., he continued his studies by means of correspondence courses and passed the I.E.E. Examination in 1947. During his 28 years at T.R.E. and R.R.E., Mr. Warner has worked on the 'Oboe' blind bombing system, millimetre waves, radio astronomy, radar equipments, lasers, Gunn oscillators and microwave standards; and he has had ten papers published on various aspects of this work.

G. S. Hobson read physics at Keble College, Oxford, and joined the Royal Radar Establishment in 1961. His work there included ionospheric plasma diagnosis, conduction properties of germanium, cadmium sulphide acoustic amplifiers and the circuit properties and circuit interpretation of physical properties of Gunn oscillators. In 1968 he joined the Department of Electronic and Electrical Engineering, University of Sheffield, where his research interests are Gunn oscillators and microstrip transmission lines.

Biographical notes on Messrs. T. S. Plews and K. G. Nichols and the late Mr. C. R. Barber will be published in the July issue.

U.D.C. 621.382.3

Stabilization of n-p-n Transistors

By

K. L. HUGHES,
B.Sc., Ph.D., C.Eng., M.I.E.E.†

Presented at the Joint I.P.P.S.—I.E.E.—I.E.R.E. Conference on Solid-State Devices at Exeter in September 1969.

A process for transistor manufacture is described which produces stable leakage currents when junctions are reverse-biased at elevated temperatures. The transistors also have a good gain relationship between 10 mA and 1 μA and this relationship is not seriously degraded during ageing. The process produces a low noise figure in the $1/f$ region which, it is believed, is related to reliability.

1. Introduction

This paper deals with two types of instability. The first is normally called ion drift and is the increase in leakage current over a period of time when a junction is reverse biased at elevated temperatures. The second is the change in current gain (h_{FE}) when a transistor is operated at elevated temperatures. The causes of these instabilities are discussed in detail together with the methods used to prevent them.

The paper also deals with the effect of emitter concentration on noise figure. This is included because it is attempted, nowadays, to correlate low-frequency noise with the reliability of devices and it is implied that the lower the noise level the longer the life span of the device.

2. Types of Instability

There is a class of small signal transistors which maintain a good gain relationship between 10 mA and 10 μA and also have a low noise figure. Of these transistors the 2N930 is the most common. When developed, this class of device not only had low noise and high gain at low currents, but was also extremely stable and reliable. The results and discussions which follow are based on devices like 2N930s, but the principles can also be applied to most classes of planar transistors and integrated circuits.

2.1. *Ion Drift*

Figure 1 shows a diagrammatic representation of a planar p–n junction and its passivating layer. This passivating layer, normally silicon dioxide, has two types of positive charge associated with it. At the silicon–silicon dioxide interface are a number of fixed positive charges which are often attributed to a deficiency of oxygen during the growth of the oxide.[1] Also in the oxide are positive charges which become mobile at elevated temperatures. These are extensively reported to be due to the presence of sodium ions in the oxide.[2,3,4]

Under steady state conditions the positive charges will repel holes from the silicon surface and attract electrons. When the ions become mobile at elevated temperatures and are drifted under the influence of an applied field, which will exist in the oxide when a junction is reverse biased, they will accumulate near

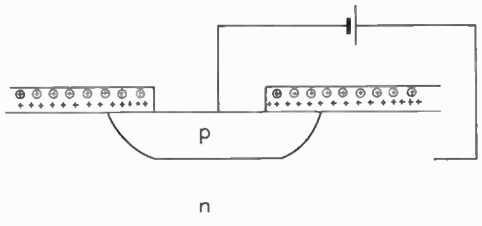


Fig. 1. Planar junction and its passivating oxide.

the silicon–silicon dioxide interface above the p-region. This will further increase the tendency for the p-region to deplete and under gross contamination conditions the p-region can actually be inverted to n-type, a situation illustrated in Fig. 2. Here inversion is illustrated to take place at the edge of the p-region, at the surface. The edge of a junction is always the most likely region to invert since this is the region of lowest concentration.

This inverted n–p type junction is characterized by a low breakdown voltage,[5] and, as the applied voltage is increased, the depletion layer associated with this junction spreads towards the surface of the silicon and pinches off the current path as in a field effect transistor. Eventually the applied voltage is high enough for the major part of the junction to break down.

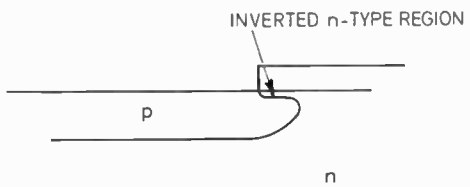


Fig. 2. Inversion of p-type region.

† Ferranti Ltd., Simonsway, Wythenshawe, Manchester.

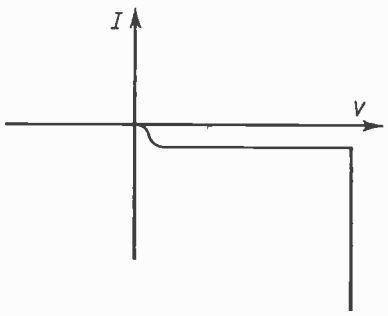


Fig. 3. I/V characteristic of an inverted junction.

An I/V characteristic described above is shown in Fig. 3 and is typical of junctions which are said to 'channel'.

2.2 *Variation in Current Gain* h_{FE}

The second form of instability is the variation in current gain (h_{FE}) when the transistor is operated at elevated temperatures. This variation is caused by a change in the properties of the silicon–silicon dioxide interface. In fact it is a change in the amount of recombination between electrons from the emitter and holes from the base terminal. This recombination takes place in fast surface states located at the surface of the base region and those which predominate when the transistor is operated at low collector currents are within the emitter-base space charge region at the surface.

3. Elimination of Ion Drift

The origin of the mobile ions which cause ion drift is not well understood so that it is easier to cure rather than prevent ion drift. It is apparent that the higher the concentration in the p-region the more difficult it becomes to invert to n-type. In practice only a shallow region near the surface of the p-region is actually inverted, so that it is necessary to maintain a high concentration at the surface only. This can be done in two ways. The first and obvious method is to increase the overall doping level in the base region but this can lead to narrow base-width devices. The second method is to reduce the well-known surface dip in the base concentration. This dip arises because boron, the dopant used in the base region of n–p–n transistors, has a segregation coefficient in favour of the silicon dioxide rather than the silicon itself. This means that there will always be a loss of boron from the silicon when an oxide is grown on a p-type region. However, the amount of boron removed during the oxidation is very dependent both on the temperature and ambient used during the oxidation. This effect is reported by Deal *et al.*[6] and the inference from their report is that the redistribution of boron should take place at as high a temperature as is convenient in a dry oxygen ambient. This ensures that the boron is redistributed quickly while the rate of oxidation (which determines the amount of boron removed from the silicon) is fairly low. The final increase in oxide thickness which is needed for subsequent processing is then achieved with a steam ambient.

Reducing the surface dip alone is not normally sufficient to cure ion drift. However, complete elimination of ion drift can be achieved by a combination of this technique plus the well-known gettering action of phosphorus oxides. It is believed that mobile ions are trapped in a phosphorus-doped oxide and cannot then move to positions where they can invert p-type regions.

When a field is applied to a p–n junction the lines of force usually extend well outside the oxide. This means that mobile ions will tend to be moved under the influence of the field into the top oxide layer. Hence, a phospho-silicate glass over existing oxides can still inhibit or getter ions from the underlying oxide. Alternatively, if the ions usually enter at a late stage during the processing of the devices the glass will act as a barrier.

4. Reduction of Gain Variation

The gain of a transistor at moderate current densities is primarily determined by its emitter efficiency. However, at lower current densities it is also affected by recombination centres at the silicon–silicon dioxide interface in the base region. It has been shown mathematically[7] that these centres are more accessible for recombination when the surface tends towards an intrinsic condition. Clearly, therefore, any tendency for the surface of the base to deplete due to ion drift will cause an increase in the amount of recombination and hence a decrease in gain.

Figure 4 shows a sketch of the forward bias characteristics of an emitter-base diode at the surface and in the

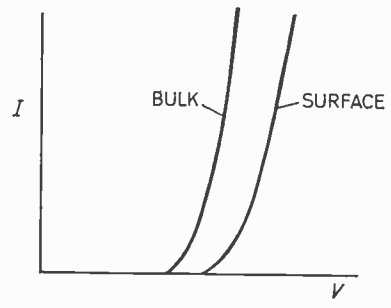


Fig. 4. Forward bias characteristics of emitter/base junction at the surface and in the bulk.

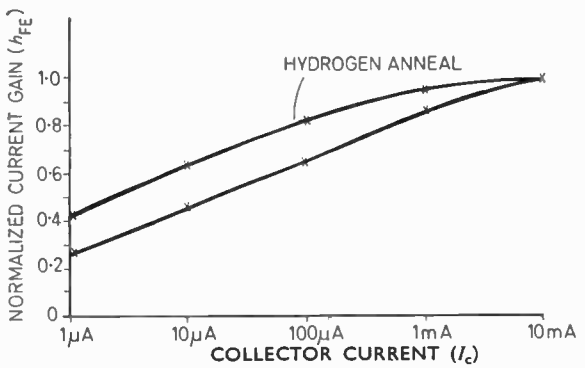


Fig. 5. Effect of hydrogen anneals on the fall-off of h_{FE} at low collector currents.

bulk. Thus there is a built-in tendency for the emitter-base to inject in the bulk rather than the surface and it is difficult for injected electrons to reach the surface. However, if the surface of the base becomes depleted there will be a change in the forward bias characteristic at the surface and more injection will take place there, with a consequent increase in recombination and a decrease in gain. Obviously elimination of ion drift in transistors will help to reduce these gain variations. This again is prevention rather than cure in the sense that electrons from the emitter are prevented from reaching the fast surface states rather than a complete removal of the centres themselves.

It has been known for some time that the use of hydrogen anneals reduces the number of recombination centres, but it has also been found that these hydrogen anneals can be very damaging to the leakage currents of devices. In the experiments described here, it has been found that providing the transistors are stabilized by the use of a phosphosilicate glass then a hydrogen anneal is beneficial to the gain at low collector currents without degrading other parameters. This has been confirmed in a recent paper.[8]

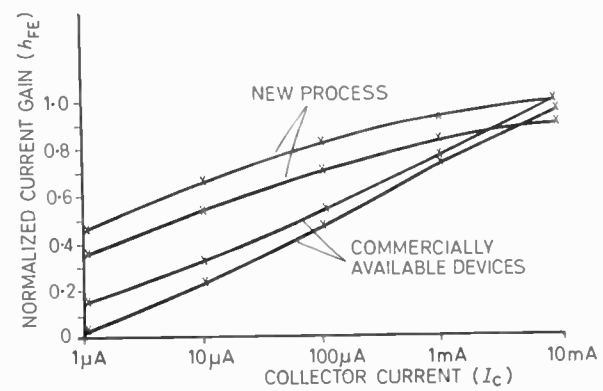


Fig. 6. Effect of ion drift conditions on h_{FE} against collector current.

The effect of these hydrogen anneals is shown in Fig. 5 where the normalized gain is plotted against collector current for transistors which have had a 600°C hydrogen anneal for 15 minutes and for a control batch which had no hydrogen anneal.

5. Stability Results

5.1. *Ion Drift*

The conditions used for testing the stability of the collector-base leakage current were 230°C ambient with 15 V reverse bias on the junction. The transistors were held in this condition for 1000 hours. This resulted in a maximum change in leakage current of a factor of 3.

5.2. *Gain Stability*

The effect of the conditions described in Section 5.1 upon gain of the transistors is shown in Fig. 6. This shows a plot of normalized gain against collector current before and after the above conditions were applied. These results are also compared with devices which were available commercially. This graph emphasizes the degree to which the gain is maintained

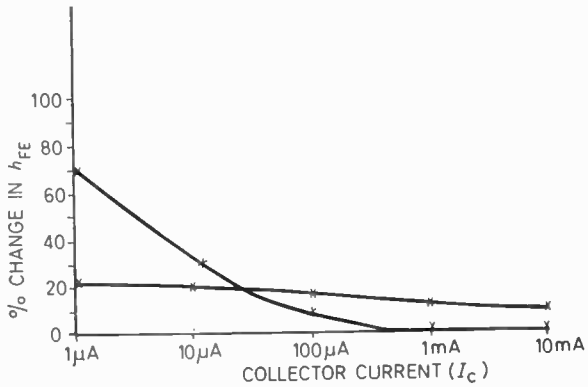


Fig. 7. Percentage change in h_{FE} after transistor is subjected to ion drift conditions.

at low collector currents. However, this method of presenting the gain degradation gives a distorted picture, since devices having, say, only 15% normalized gain cannot decrease by more than 15%. Hence, the results are re-plotted in Fig. 7 where percentage change in h_{FE} is plotted against collector current. Here it is apparent that the devices described above show about 15–20% gain reduction over the range 1 μA to 10 mA, whilst the commercially-available devices showed a decrease in gain of 75% at 1 μA and in fact showed an increase in gain above 10 mA.

6. Noise Figure

Since the gain of a transistor is primarily determined by its emitter efficiency which in turn is determined

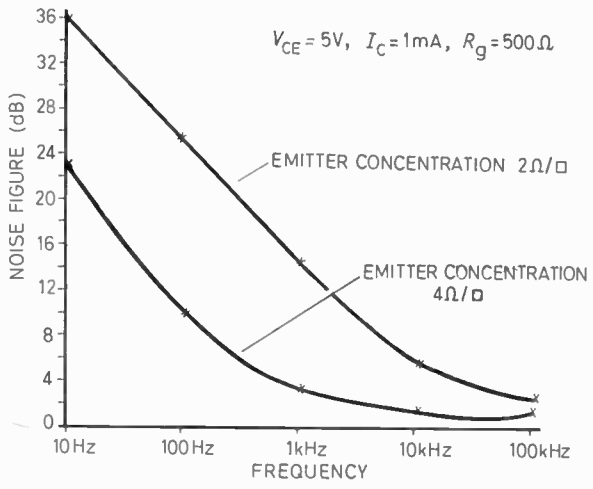


Fig. 8. The effect of emitter concentration on noise figure at various frequencies.

by the relative dopings in the emitter and base regions, there is a tendency to keep the emitter concentration as high as possible. However, this can lead to a serious degradation in transistor noise figure particularly in the $1/f$ region. This is demonstrated in Fig. 8 where noise figure in decibels is plotted against frequency on a logarithmic scale. The effect of reducing the emitter concentration from 2Ω/square to 4Ω/square is seen to reduce the noise figure by about 12 dB in the $1/f$ region.

A paper by van der Ziel and Hu Tong[9] has indicated that there is a relationship between the noise figure of a transistor in the $1/f$ region and the life-span of the device—a low noise device having a long life-span. The indications are therefore that the devices which use an emitter of 4Ω/square will be more reliable than those with an emitter of 2Ω/square.

7. References

1. Thomas, J. E., Jr. and Young, D. R., 'Space-charge model for surface potential shifts in silicon passivated with thin insulating layers', *I.B.M. J. Res. Devel.*, **8**, p. 368, September 1964.
2. Hostein, S. R., 'Stabilization of mos devices', *Solid-State Electronics*, **10**, p. 657, 1967.
3. Deal, B. E., Sklar, M., Grove, A. S. and Snow, E. H., 'Characteristics of the surface-state charge (Q_{ss}) of thermally oxidized silicon', *J. Electrochem. Soc.*, **114**, p. 266, March 1967.
4. Buck, T. M., Allen, F. G., Dalton, J. V. and Struthers, J. D., 'Studies of sodium in SiO_2 films by neutron activation and radiotracer techniques', *J. Electrochem. Soc., Solid State Science*, **114**, p. 862, August 1967.
5. Grove, A. S. and Fitzgerald, D. J., 'The origin of channel currents associated with P+ regions in silicon', *I.E.E.E. Trans. on Electron Devices*, **ED-12**, p. 619, 1965.
6. Deal, B. E., Grove, A. S., Snow, E. H. and Sah, C. T., 'Observation of impurity redistribution during thermal oxidation of silicon using the mos structure', *J. Electrochem. Soc.*, **112**, No. 3, p. 308, March 1965.
7. Reddi, V. G. K., 'Influence of surface conditions on silicon planar transistor current gain', *Solid-State Electronics*, **10**, p. 305, 1967.
8. Bergh, A. A. and Bartholomew, C. Y., 'The effect of heat-treatment on transistor low current gain with various ambients and contamination', *J. Electrochem. Soc.*, **115**, No. 12, p. 1282, December 1968.
9. van der Ziel, A. and Hu Tong, 'Low frequency noise predicts when a transistor will fail', *Electronics*, **39**, p. 95, 28th November 1966.

Manuscript received by the Institution on 29th December 1969.
(Short Contribution No. 136/CC82.)

U.D.C. 621.374.4

Some Cellular Logic Arrays for Non-Restoring Binary Division

By

H. H. GUILD,
B.Sc.†

An array containing controlled adder-subtractor cells is described. An alternative array is presented which uses 2's complement arithmetic to perform subtractions. The operating speeds of the arrays are considered in connection with the logical design of the cells. An application of cellular arrays in generating the Napierian logarithm of a binary number is outlined.

1. Introduction

The development of integrated circuit technology has made possible the production of high reliability, low cost, electronic sub-systems of increasing complexity. The available complexity together with the ever-present requirement for improved operating speed leads naturally to a consideration of combinational circuit designs. Integrated circuit fabrication is facilitated by circuit designs having a repetitive cellular structure; a cellular array which also possesses a regular interconnexion pattern is termed an iterative array.[1]

Recent papers have described combinational cellular arrays for code conversion[2] and binary arithmetic (multiplication[3], division[4], square-root extraction[5]). References 4 and 5 describe arrays based on restoring arithmetical methods. Designs are presented here for binary division using non-restoring arithmetic. This form of arithmetic is advantageous because a sub-cycle, which is necessarily present in restoring arithmetic, is eliminated. Positive binary numbers are considered for simplicity, although the method may be readily extended to deal with signed binary numbers where required.

2. Division Algorithm

In the restoring binary division process the divisor is first subtracted from the high-order positions of the dividend. The partial remainder is then shifted one place to the left, and the divisor is again subtracted. For a subtraction resulting in a positive partial remainder the quotient digit determined is a 1; if a negative partial remainder occurs, the quotient digit is a 0 and the restoring sub-cycle is brought into operation whereby the divisor is effectively added back into the partial remainder before the next shift and subtraction. Denoting the divisor by d, the change in the partial remainder during a restoring sub-cycle and the following shift and subtraction is $+d-(d/2) = +(d/2)$. Hence the restoring sub-cycle may be eliminated if, when a negative partial remainder is produced, a shift and an *addition* are performed. This constitutes the algorithm for non-restoring binary division; a formal treatment of the algorithm may be found in reference 6. In a cycle involving either an addition or a subtraction, a positive result yields a quotient digit of 1, but a negative result gives a quotient digit of 0. A cycle is here defined as the processing required to generate a single digit of the quotient.

In using non-restoring arithmetic for division, when the least significant digit determined for the quotient is a 1, the final remainder appears correctly. If, however, this digit is a 0 the true remainder is obtained by adding the divisor to the final remainder.

3. Array for Division

The design of a combinational array for non-restoring binary division may be based on a cell whose logical operation permits a controlled choice of addition or subtraction to be performed on the data applied to its inputs. Figure 1 shows a single controlled adder-subtractor cell having four inputs A, B, C, D and four outputs E, F, G, H. The cell function may be summarized as follows: for A = 0, E is the difference and F the borrow generated in forming B−(C+D), while for A = 1, E is the sum and F the carry produced by the addition B+C+D.

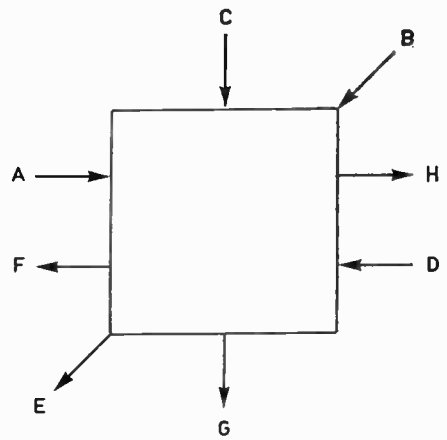


Fig. 1. Single controlled adder-subtractor cell.

† Department of Physics, Kingston Polytechnic, Kingston upon Thames, Surrey.

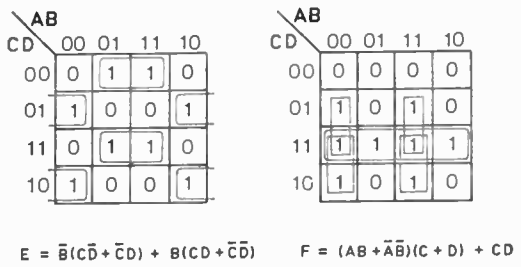


Fig. 2. Karnaugh maps showing the derivation of Boolean expressions for the logic of a controlled adder-subtractor cell.

Also, independently of all other inputs, G = C and H = A. Figure 2 shows Karnaugh maps leading to Boolean expressions for the cell logic.

The structure of the proposed array for non-restoring binary division is shown in Fig. 3. The left-shift of the partial remainder necessary in each cycle is accommodated by the interconnexion pattern. Since a subtraction must be performed in the first cycle, the control inputs (A) to the cells in the top row are set to logic level 0. The sign of the resulting partial remainder is negative if a final borrow is produced, and positive if it is absent. Hence the most significant quotient digit may be determined by negating the logic level at the final borrow output in the top row of the array. During subsequent cycles either an addition or a subtraction is performed depending on the data being processed and an additional cell is required to determine the sign of the partial remainder. The sign digit appears at the output E of these cells. If the sign digit is a 0, the partial remainder is positive and the corresponding quotient digit is a 1 (produced by negation); a 1 sign digit indicates a negative partial remainder resulting in a quotient digit of 0. The sign digit is used to select the subtraction or addition operation in the following cycle, but in the shifting process it is discarded from the partial remainder.

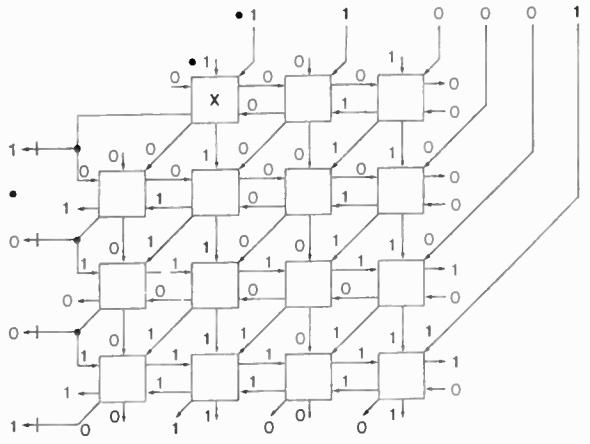


Fig. 3. Cellular array of controlled adder-subtractor cells connected as a divider. The bar symbols on the left of the Figure represent negating gates.

Figure 3 is marked to show the inter-cellular states attained in the division process of Example 1. In the Example, $_a$ denotes an addition and $_s$ a subtraction; sign digits are underlined for identification. The width of the array can be extended to accommodate input data of greater word length, and the number of rows in the array can be increased to give the quotient to as many places as may be required.

The operating speed τ of the array is given by

$$\tau = N\tau_d + N(N+1)\tau_b + \tau_n \qquad \ldots.(1)$$

where τ_d, τ_b are the signal delays for the sum-difference output E and the carry-borrow output F of a single cell; τ_n is the delay for a single negating gate. The word lengths of the dividend, divisor and quotient are respectively $2N$, N and $N+1$ bits; Fig. 3 shows an array for $N = 3$. The formula assumes the maximum occurrence of delays in the array and the use of word lengths satisfying the inequality $N\tau_b \geqslant \tau_d$. The predominant term, $N(N+1)\tau_b$ in this worst case formula for the operating speed, shows that the logical design of the basic cell should be orientated towards the production of a carry-borrow-signal involving as few gate delays as possible (e.g. by use of wired-OR connexions).

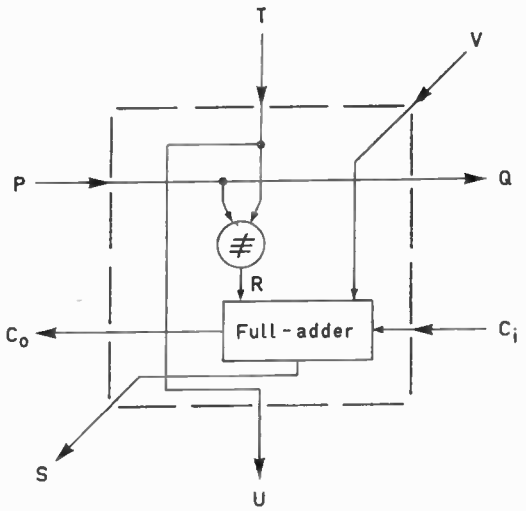


Fig. 4. Adder cell with controlled complementation of the input T.

4. Alternative Array for Division

The design of an array is now described in which subtractions are performed by addition of the divisor in 2's complement form. In the basic cell, shown in Fig. 4, a divisor digit presented at the input T is subjected to a controlled complementation, dependent on the state of the control input P, before application

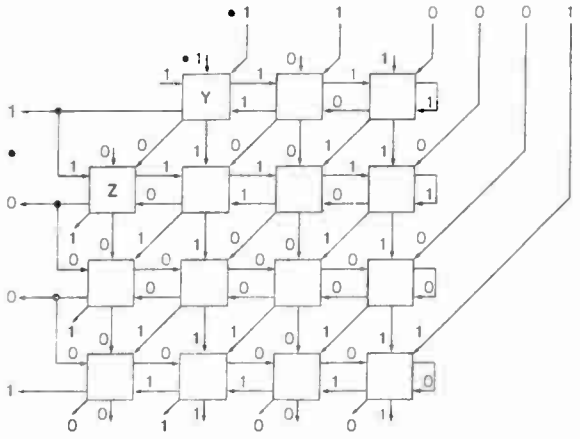


Fig. 5. Iterative array for division comprising cells of the type shown in Fig. 4.

to the input R of the full-adder. For P = 0, R = T, while for P = 1, R = $\bar{T}$. The full-adder performs the addition $V+R+C_i$ to give the sum and carry outputs S and C_0. Also, independently of all other inputs, Q = P and U = T.

Figure 5 shows how cells of this type are interconnected to form an iterative array. When, in a given row of the array, the control inputs (P) to the cells are at logic level 0, the divisor is added to the partial remainder; when the control logic level is a 1, however, the 2's complement of the divisor is added to the partial remainder, thus effecting a subtraction. The 2's complement of the divisor is formed by inversion (yielding the 1's complement) and application of the control signal, of logic level 1, to the lowest order carry input of the row considered. As a consequence of employing 2's complement arithmetic for subtraction, the final carry-signal in each row of the array is directly related to the corresponding quotient digit. The speed of operation is enhanced by a full-adder design giving rapid propagation of carry-signals along the rows of the array. The use of a carry-signal for control enables the processing of data in a given row to proceed correctly prior to the complete formulation of data at the sum outputs (S) of the cells in the previous row.

For an array of the type shown in Fig. 5, the worst case operating speed τ is given by

$$\tau = N\tau_e + N(N+2)\tau_c \qquad \ldots(2)$$

where τ_e is an exclusive-OR (non-equivalence) gate delay, τ_c is a full-adder carry-signal delay, and the word lengths of the dividend, divisor and quotient are respectively $2N$, N and $N+1$ bits. The formula assumes the use of word lengths satisfying the relationship $(N+1)\tau_c + \tau_e \geqslant \tau_s$, where τ_s is the full-adder sum-signal delay.

The number of cells in the array is $N(N+2)$. The array may be implemented using currently available medium-scale integration devices (quadruple exclusive-OR gates and quadruple full-adders) giving an average of two cells per package. Typical t.t.l. integrated circuit parameters (τ_e = 16 ns and τ_c = 8 ns) yield, for N = 10, a value of τ = 1120 ns. Since no delay occurs when a logic level remains unchanged, the operating speed may in practice be less than this worst case value.

In Fig. 5 the cells have been marked to illustrate the division process of Example 2. In this Example an addition $_a$ is performed in each cycle; a suffix c denotes the 2's complement of the divisor.

Example 1: Non-restoring division

quotient digits		·110001	dividend
		·101	divisor
		——$_s$	
m.s.d. → 1	no final borrow	001001	
		001001	shift left
·		0101	divisor
		——$_s$	
0	negative result	110101	
		10101	shift left
		0101	divisor
		——$_a$	
0	negative result	11111	
		1111	shift left
		0101	divisor
		——$_a$	
1	positive result	0100	

remainder after four cycles = 0·000100

Example 2: Non-restoring division using 2's complement arithmetic

quotient digits		·110001	dividend
		·011	divisor$_c$
		——$_a$	
m.s.d. → 1	final carry	001001	
		001001	shift left
·		1011	divisor$_c$
		——$_a$	
0	no final carry	110101	
		10101	shift left
		0101	divisor
		——$_a$	
0	no final carry	11111	
		1111	shift left
		0101	divisor
		——$_a$	
1	final carry	0100	

remainder after four cycles = 0·000100

5. Redundant Cells

When designing hardware to perform a division operation, restrictions are frequently imposed on the magnitudes of acceptable dividend and divisor data. The designs described here are subject to the input data restrictions that the divisor is normalized and that the dividend is presented as a number of value less than unity. When in this form, data may be presented to array inputs with the positions of the binary points as indicated in the array diagrams. The quotient q then lies in the range $2^1 > q \geqslant 0$.

An alternative specification for the input data requires complete normalization (i.e. both the dividend and the divisor are of the form $\cdot 1\ldots$). This specification is attractive since the quotient then lies in the range $2^1 > q > 2^{-1}$ and normalization of the quotient involves, at most, one binary place. Furthermore, an examination of the possible inter-cellular states under these conditions reveals some cellular redundancy. Thus, for example, in Fig. 5 the cells Y and Z may be omitted provided that horizontal and vertical connexions are extended linearly through the locations of these cells. Similarly in Fig. 3 the cell marked X may be replaced by simple connexions when the input data are known to be completely normalized.

6. An Application of Arrays

Cellular logical arrays may be used to evaluate certain mathematical functions by an iteration process, or by generating and summing a truncated series. Figure 6 shows an application of arrays in generating the Napierian logarithm of a binary number y for the range $0 < y \leqslant 1$.

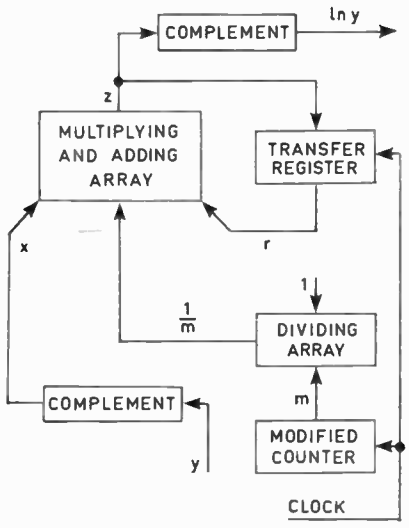


Fig. 6. System for generating the Napierian logarithm of a binary number.

A down-counter is modified to give an output of unity both before and after the final clock pulse, thus producing the output sequence ...4, 3, 2, 1, 1 in binary code. The reciprocal, $1/m$, of the counter output is applied to the adding input of the multiplying and adding array.[3] The output r of the transfer register, and a number $x = 1-y$, are presented to the multiplying inputs to produce a value $z = rx + 1/m$. Initially the transfer register is reset giving $r = 0$. If, for example, the initial value of the counter output is 3, then by applying three clock pulses to the system, the following sequence of values appears for z: $1/3$; $x/3+1/2$; $x^2/3+x/2+1$; $x^3/3+x^2/2+x+1$. Thus z represents the truncated convergent series for $1-\ln(1-x)$. Complementation of z gives an output representing $\ln(1-x) = \ln y$, the accuracy being determined by the number of series terms generated.

7. Conclusions

Two designs (Figs. 3 and 5) have been presented for non-restoring division arrays. Equations (1) and (2) for the operating speeds of these arrays indicate that the logical designs of the cells should primarily achieve the rapid propagation of signals along the rows of the arrays. The use of 2's complement arithmetic to perform subtractions leads to an array, shown in Fig. 5, possessing the following advantages. Quotient digits are obtained from cell outputs without the use of extraneous gates. The use of a carry signal for control, rather than a sum signal, enhances the operating speed. Finally, the array may be implemented using a relatively small number of currently available integrated circuits. The array may be regarded as a candidate for large-scale integration, in which case the logic content of the basic cell should be designed as a whole, replacing the separate components shown in Fig. 4.

8. References

1. Hennie, F. C., 'Iterative Arrays of Logical Circuits'. (Wiley, New York, 1961).
2. Guild, H. H., 'Fast decimal-binary conversion', *Electronics Letters*, **5**, pp. 427–8, 4th September 1969.
3. Guild, H. H., 'Fully iterative fast array for binary multiplication and addition', *Electronics Letters*, **5**, p. 263, 12th June 1969.
4. Dean, K. J., 'Binary division using a data-dependent iterative array', *Electronics Letters*, **4**, pp. 283–4, 12th July 1968.
5. Dean, K. J., 'Cellular logical array for extracting square roots', *Electronics Letters*, **4**, pp. 314–5, 26th July 1968.
6. Chu, Y., 'Digital Computer Design Fundamentals', pp. 39–41 (McGraw-Hill, New York, 1962).

Manuscript first received by the Institution on 24th November 1969 and in final form on 3rd April 1970. Short Contribution No. 137/Comp. 128.

SUBJECT INDEX

Papers and major articles are denoted by printing the page numbers in bold type

INDEX OF PERSONS

Names of authors of papers published in the volume are indicated by bold numerals for the page reference.

Biographical references are denoted by B.