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THE RADIO AND ELECTRONIC ENGINEER

The Journal of the Institution of Electronic and Radio Engineers

VOLUME 36 No. 6 DECEMBER 1968

Encouraging Invention

THE establishment of the MacRobert Award by the Council of Engineering Institutions and the MacRobert Trust, reported on page 348 of this issue, represents a prize for technology equivalent, within Britain, to the international Nobel Prizes which are awarded for scientific achievement. The MacRobert Award will recognize technological achievement and will be widely welcomed as a means of rewarding outstanding engineering innovation. It will assuredly take pride of place among the many retrospective encouragements to inventors and innovators which already exist: these include many more modest prizes and medals given by learned and other societies, such as, for instance, premiums by Institutions for outstanding papers.

Certainly the award should help innovation by providing a handsome incentive. At the same time it is inherent in all such awards and prizes that the work has been done and achievement is obvious: is there not an even greater need for providing encouragement in advance to enable inventions of promise to be developed to a successful conclusion? Most people will agree in principle with this—there have been all too many instances in technological history of an inventor being reduced to penury while the realization of his invention has come years later when backing for development comes from sources more far-sighted than those available in his lifetime. The controversial question is, how best can such support be provided?

The reluctance of all inventors, especially the lone workers, to share their secrets for fear of losing their rights, is understandable and should be respected. Thus, support should desirably be implemented by agencies whose commercial independence is assured and this role might seem most likely to be fulfilled by a government-sponsored organization as has been set up in Great Britain, namely the National Research Development Corporation. The requirement for such an agency to strike relatively short-term balances between its expenditure and the revenue from successful promotions must, however, discourage the support of the more speculative projects and favour the more conventional and obvious 'winners'. This is a very general dilemma for every large industrial enterprise similarly has to assess which of its research projects it shall proceed to develop and exploit and here again caution will usually prevail.

One solution to the problem of affording encouragement and support to promising projects could be through the existence of a multiplicity of sources of finance whereby a measure of competition could operate in bringing more potential winners to the fore. Whether these sources should be government sponsored, or independent non-profit-making agencies, or private-enterprise consortia, or even examples of all these, is a matter for debate.

Perhaps in the electronics field there is a task for both the National Electronics Council and the Institution to bring together all likely funding sources and make recommendations for the award of worthwhile sums.

F. W. S.

INSTITUTION NOTICES

Physiology for Engineers

The Joint I.E.R.E.–I.E.E. Medical and Biological Electronics Group is promoting a series of four special meetings during the early part of 1969. These lecture meetings with demonstrations have the purpose of enabling engineers to increase their background knowledge of physiological subjects directly applicable to the fields of electronic and electrical engineering in medicine.

The meetings, to be held at St. Bartholomew's Hospital Medical College, West Smithfield, London, E.C.1, commencing at 5.30 p.m., are as follows:

February 11th, 'Muscle' by Professor D. R. Wilkie.

March 11th, 'Nerve impulse' by Dr. A. Ritchens, M.B., B.S., B.Sc., Ph.D.

April 22nd, 'Sensation' by Dr. T. A. Quilliam, Ph.D., M.B., B.S., D.L.O.

May 20th, 'Auditory mechanism' by Mr. H. A. Beagley, F.R.C.S.

(*All Tuesdays*)

Admission will be free to members of the Institution of Electronic and Radio Engineers, the Institution of Electrical Engineers, the Institute of Physics and the Physical Society, and the Institute of Mathematics and its Applications. To non-members the fee for the series of four lectures will be £1. Advance registration will be necessary and applications for tickets, accompanied by the fee if appropriate, should be sent to: The Secretary, Medical Electronics Group, The Institution of Electrical Engineers, Savoy Place, London, W.C.2.

Registration of Engineers in Canada

Most members will be aware that the requirement for engineers practising in Canada to be registered as 'Professional Engineer' (P.Eng.) has led to difficulties in equating British engineering qualifications with the regulations of the Professional Associations of the Provinces. Following visits to Canada in recent years, first by the Director of the I.E.R.E., Mr. Graham D. Clifford, and subsequently by the Secretary of the Council of Engineering Institutions, a much clearer policy has emerged. Acceptance of British qualifications by the Association of Professional Engineers of the Province of Ontario is now governed by the following regulations:

(1) Honours degrees in Engineering awarded by universities in the United Kingdom or under the Council for National Academic Awards, are recognized as exempting from the Association's examinations.

(2) Ordinary degrees in Engineering awarded by universities in the United Kingdom, or under the C.N.A.A., and recognized by the Council of Engineering Institutions, are recognized as exempting from the Association's examinations, provided that the degree holder is also a Corporate Member of a constituent member Institution of C.E.I.

(3) Full Members (now Fellows) of constituent member Institutions of the Council of Engineering Institutions are admitted to registration; and Corporate Members (former Associate Members, now Members) who have passed the examinations of C.E.I. or a constituent Institution without exemption, *or* whose academic qualifications at the time of admission to Corporate Membership are certified by the Institution concerned to have been the equivalent of at least Ordinary degree standing, are admitted to registration without further examination of educational qualifications.

The above rules governing admission have been transmitted to the Canadian Council of Professional Engineers and it is hoped that they may, before long, become standard throughout Canada.

Reduced Subscription Rates

Members of this Institution have for several years been able to subscribe to publications of the Institution of Electrical Engineers at a reduced reciprocal privilege rate (25% of normal public subscription).

The following revised prices will apply to I.E.E. publications from January 1969:

	Annually	*Single copy*
	£ s.	
I.E.E. News	1 10	2s.
Electronics & Power	6 0	15s.
Proceedings I.E.E.	15 15	30s.
Electronics Record	7 10	30s.
Power Record	4 10	30s.
Control & Science Record	4 10	30s.
Electronics Letters	7 10	7s. 6d.
Students' Quarterly Journal	15	5s.
SCIENCE ABSTRACTS PUBLICATIONS:		
Current Papers in Electrical & Electronics Engineering (CPE)	3 15	—
Current Papers on Computers & Control (CPC)	2 10	—

Members of the I.E.R.E. wishing to take advantage of these concessionary rates must place orders through the I.E.R.E. Publications Department, 8–9 Bedford Square, London, W.C.1.

U.D.C. 681.32

A New Approach to the Design of Asynchronous Logic

By

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M.I.E.R.E.†

Summary: Asynchronous sequential logic using NOR/NAND integrated circuits is extensively used in fast digital systems. The standard design procedure results in a set of excitation equations for the secondary variables, which must be examined (and corrected) for static logical hazards prior to implementation.

A modified design technique is postulated which allows sequential circuits to be implemented directly in terms of d.c. set/reset bistables (i.e. cross-coupled NOR/NAND elements). It is shown that the use of d.c. bistables in this manner prevents the occurrence of static hazards, thus obviating hazard correction. Additional advantages are that the circuits evolved use fewer modules than conventionally designed logic, and exhibit a simpler logical structure.

Detailed designs (both methods are used for comparison) for an asynchronous Gray-code counter, employing TTL logic, are described.

1. Introduction

There are two main types of sequential switching circuit, *synchronous* (clocked) and *asynchronous* (free-running). In the former type each input, output and internal state is sampled at definite intervals of time, controlled by the fundamental clock frequency of the system. Asynchronous circuits proceed at their own speed, regardless of any basic timing, and are consequently faster in operation since full advantage may be taken of the basic speed of the logic modules —there is no need for circuit transitions to wait for a clock pulse.

The absence of timing pulses however requires the designer to consider two possible circuit conditions for an asynchronous system, namely the *stable* and *unstable* states. The unstable condition exists when the circuit is changing state in response to an input change, the simplest example being in fact the d.c. set/reset bistable (Fig. 1). Consider a bistable element the truth table for which is shown in Table 1.

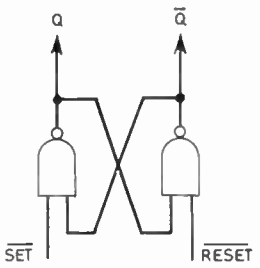


Fig. 1. A NAND d.c. bistable element.

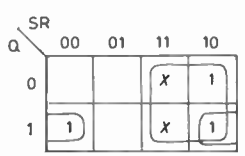
Table 1

Set/reset bistable

(a) Truth table

S	R	Q	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	indeterminate
1	1	1	indeterminate

(b) Characteristic equation



With output Q = 1 and inputs S = R = 0, this is the stable condition. Now an input change to S = 0 and R = 1 requires the output to go to Q = 0. But before the circuit reaches this new stable condition, there is a momentary delay (varying with each module) during which time we have the unstable condition of Q = 1, with inputs S = 0 and R = 1. In designing asynchronous logic it is always assumed that the circuit will eventually arrive at a stable condition, implying that the duration of the inputs will always be such as to allow this to occur. If however the input

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changes before the new stable state is reached a *resolution* hazard could result.

A further requirement is that the input and internal state variables must only change one at a time. The reason for this is again due to inherent delays in the module. Suppose, for example, a variable change from $00 \rightarrow 11$ was required, unless the delay paths were identical (a most unlikely occurrence) the change could be either $00 \rightarrow 10 \rightarrow 11$ or $00 \rightarrow 01 \rightarrow 11$. This could lead to erroneous operation of the circuit. Consequently, since there is no prior means of determining the exact transition path, variable changes must be restricted to one at a time.

In synchronous systems the clock pulses ensure that the output and input variables are examined after circuit delays have settled out, hence problems arising from the finite (and random) switching time of the basic logic modules may be neglected. Because this is not so in the case of asynchronous circuits, a major design problem is to ensure that the circuit functions according to specification regardless of variation in transmission delays within the circuit.

The logical design of asynchronous circuits was first described by Huffman[1] in 1954 with regard to relay circuits, and the technique still remains today as the text-book method of design.[2] The object of this paper is to show how the basic Huffman procedure may be modified to give better (and more economical) results when using integrated circuit logic modules. In particular, the problem of recognizing and eliminating static logical hazards in the excitation equations has been overcome, since the modified design technique results in a hazard-free circuit.

2. Design for a Gray-code Counter

The design approach is best illustrated by means of an actual circuit problem which we shall solve in two ways, firstly by using the Huffman technique, and

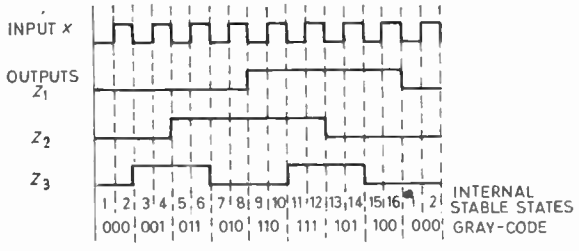


Fig. 2. Timing diagram for Gray-code counter.

secondly by the modified procedure. The circuit we will consider is a 3-bit Gray-code counter, the timing or waveform diagram of which is shown in Fig. 2.

2.1 *Huffman Design Method*

The first step in the design procedure is to draw up a *primitive flow-table*. This may be facilitated by consideration of the timing diagram, where the timing intervals represent the necessary internal stable states and the rise- and fall-times of the waveforms of the unstable states. In a primitive flow-table (see Table 2(a)) each entry represents either a stable (circled entry) or an unstable internal state of the system (or, alternatively, an indeterminate or 'don't-care' condition). It is worth noting that there is only one stable state per row. The stable states correspond to the steady state values of the circuit, and the unstable states to the values during the transition period. The required outputs for each stable state (Z_1, Z_2 and Z_3) are recorded at the end of the appropriate row.

If possible the number of rows in the primitive flow-table should be reduced (by eliminating redundant states) since in general it will contain more stable states than are actually required. For two stable states in a flow-table to be equivalent they must have the same output states, and for all possible input changes their next state transitions must result in the same (or equivalent) states. Furthermore, since a stable state is specified by *both* input and internal state conditions it is only possible to compare states in the same column. For example, in Table 3(a) comparing ① and ⑤ we find that their output and next states are the same thus we can conclude that the states are identical and hence one of them is redundant; however ① ≠ ⑦ since their output states are different, similarly ③ ≠ ⑥. The flow-table may be reduced further by 'merging' rows together. This results in more than one stable state per row of the flow-table and enables the same secondary assignment to be used for different internal states. Thus transition between stable states in the same row will be affected by *input* changes only. Rows may be merged if there are no conflicting state-numbers (irrespective of stable and unstable states) in any column; 'don't care' conditions can be used to represent any state. In Table 3(b) we may merge rows (i, ii, iii) and (iv, v, vi) to produce the final two-row table (Table 3(c)). Generally, there is more than one way of merging the rows of a flow-table, and the choice can appreciably effect circuit economy. In this particular example, as is common with most counter and shift register circuits, further reduction or merging is not possible.

The next step is to allocate a unique binary code to each row in such a way that only one internal state variable changes for each circuit transition (i.e. from one stable state to another). This will require four secondary variables (internal states) for the sixteen row table, i.e. y_1, y_2, y_3 and y_4. In this case we may use reflected-binary thus ensuring a change of one

Table 2

Design tables for Gray-code counter

(a) Primitive flow-table

Input x		Output		
0	1	Z_1	Z_2	Z_3
①	2	0	0	0
3	②	0	0	0
③	4	0	0	1
5	④	0	0	1
⑤	6	0	1	1
7	⑥	0	1	1
⑦	8	0	1	0
9	⑧	0	1	0
⑨	10	1	1	0
11	⑩	1	1	0
⑪	12	1	1	1
13	⑫	1	1	1
⑬	14	1	0	1
15	⑭	1	0	1
⑮	16	1	0	0
1	⑯	1	0	0

(b) Assigned flow-table

	Input x		Outputs
	0	1	
$y_1y_2y_3y_4$	$Y_1Y_2Y_3Y_4$	$Y_1Y_2Y_3Y_4$	$Z_1Z_2Z_3$
0 0 0 0	0 0 0 0	0 0 0 1	0 0 0
0 0 0 1	0 0 1 1	0 0 0 1	0 0 0
0 0 1 1	0 0 1 1	0 0 1 0	0 0 1
0 0 1 0	0 1 1 0	0 0 1 0	0 0 1
0 1 1 0	0 1 1 0	0 1 1 1	0 1 1
0 1 1 1	0 1 0 1	0 1 1 1	0 1 1
0 1 0 1	0 1 0 1	0 1 0 0	0 1 0
0 1 0 0	1 1 0 0	0 1 0 0	0 1 0
1 1 0 0	1 1 0 0	1 1 0 1	1 1 0
1 1 0 1	1 1 1 1	1 1 0 1	1 1 0
1 1 1 1	1 1 1 1	1 1 1 0	1 1 1
1 1 1 0	1 0 1 0	1 1 1 0	1 1 1
1 0 1 0	1 0 1 0	1 0 1 1	1 0 1
1 0 1 1	1 0 0 1	1 0 1 1	1 0 1
1 0 0 1	1 0 0 1	1 0 0 0	1 0 0
1 0 0 0	0 0 0 0	1 0 0 0	1 0 0

variable, and at the same time associating the internal state coding with the required outputs (i.e. the Moore model). Thus each stable state in the flow-table is

Table 3

(a) Primitive flow-table

Inputs xy				Output
00	01	11	10	Z
①	2	–	3	0
1	②	4	–	0
5	–	4	③	0
–	2	④	6	1
⑤	2	–	3	0
7	–	4	⑥	1
⑦	2	–	6	1

(b) Reduced flow-table

Inputs xy				Output
00	01	11	10	Z
①	2	–	3	0 (i)
1	②	4	–	0 (ii)
1	–	4	③	0 (iii)
–	2	④	6	1 (iv)
7	–	4	⑥	1 (v)
⑦	2	–	6	1 (vi)

(c) Merged flow-table

Inputs xy				Output
00	01	11	10	Z
①	②	4	③	0
⑦	2	④	⑥	1

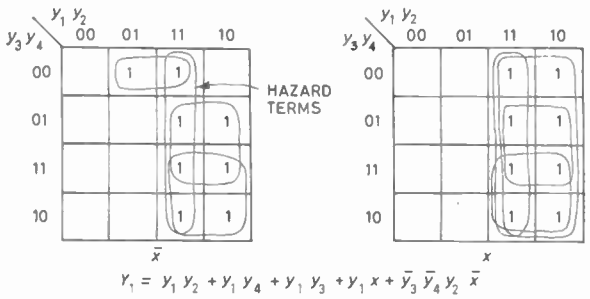
uniquely defined by a combination of inputs (x) and present internal states (y) of the machine (see Table 2(b)).

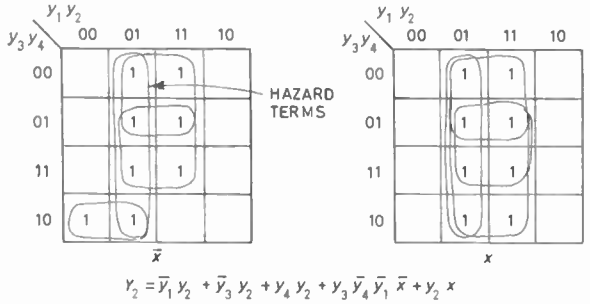
Following the standard Huffman technique we now extract the *excitation* equations (originally representing the combinational logic to energize secondary relay coils). These are obtained by examining the assigned table and noting the input and present-state variables (x, y) that are required to produce the next state variable Y. For example, for the Gray-code counter, $Y_1 = 1$ for the following conditions:

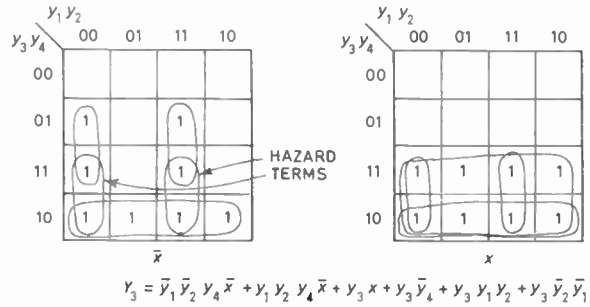
$$\begin{aligned} Y_1 = {} & \bar{y}_1y_2\bar{y}_3\bar{y}_4\bar{x}+y_1y_2\bar{y}_3\bar{y}_4\bar{x}+y_1y_2\bar{y}_3y_4\bar{x}+ \\ & y_1y_2y_3y_4\bar{x}+y_1y_2y_3\bar{y}_4\bar{x}+y_1\bar{y}_2y_3\bar{y}_4\bar{x}+ \\ & y_1\bar{y}_2y_3y_4\bar{x}+y_1\bar{y}_2\bar{y}_3y_4\bar{x}+y_1y_2\bar{y}_3\bar{y}_4x+ \\ & y_1y_2\bar{y}_3y_4x+y_1y_2y_3y_4x+y_1y_2y_3\bar{y}_4x+ \\ & y_1\bar{y}_2y_3\bar{y}_4x+y_1\bar{y}_2y_3y_4x+y_1\bar{y}_2\bar{y}_3y_4x+ \\ & y_1\bar{y}_2\bar{y}_3\bar{y}_4x. \end{aligned}$$

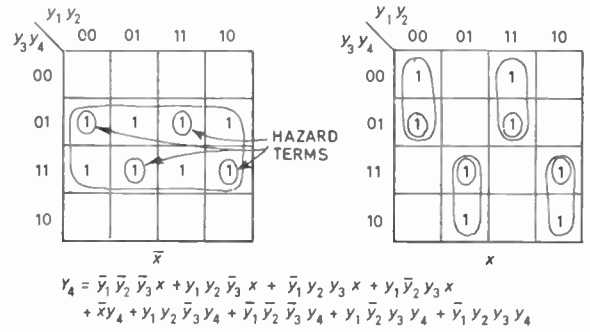
Table 4

Excitation equations





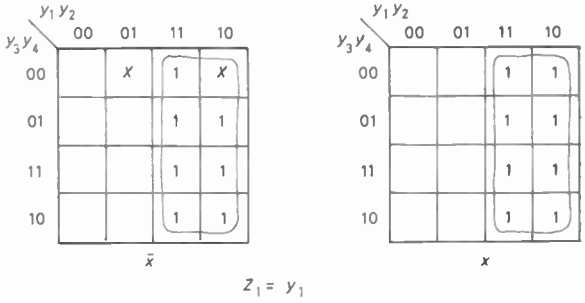


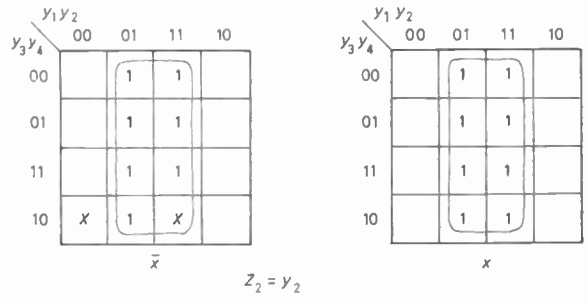


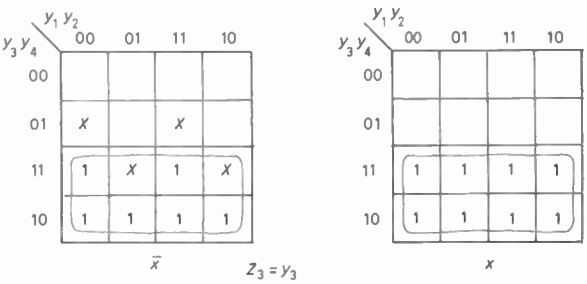
This equation could be plotted on a Karnaugh map (see Table 4) and minimized in the normal manner, similarly the equations for Y_2, Y_3 and Y_4. In obtaining the minimal functions however the possible occurrence of *static circuit hazards* (due to differences in delays in paths carrying the same signal) must be considered. Huffman[1,3] has shown that single variable

Table 5

Output maps







static hazards exist when an input change dictates a transition between internal states in different groupings on the Karnaugh map. For example, the optimum equations for Y_3 are, from Table 4:

$$Y_3 = y_3x + y_3\bar{y}_4 + \bar{y}_1\bar{y}_2y_4\bar{x} + y_1y_2y_4\bar{x}$$

However, a *ones hazard* exists for Y_3 when $\bar{y}_1 = \bar{y}_2 = y_3 = y_4 = 1$ and the input variable (x) changes from $0 \rightarrow 1$; causing Y_3 to change $1 \rightarrow 0 \rightarrow 1$ instead of remaining at 1. In effect the equation for Y_3 reduces to $Y_3 = x + \bar{x}$, but the normal Boolean relationship $x + \bar{x} = 1$ breaks down due to delay between x and $\bar{x}$ (caused in most cases by invertor delay). The hazard is normally eliminated by adding 'redundancy' to the circuit in the form of additional loops (in this case $\bar{y}_1\bar{y}_2y_3$) embracing the two hazard loops, thus the final excitation equation becomes:

$$Y_3 = y_3x + y_3\bar{y}_4 + \bar{y}_1\bar{y}_2y_4\bar{x} + \bar{y}_1\bar{y}_2y_3 + y_1y_2y_4\bar{x} + y_1y_2y_3.$$

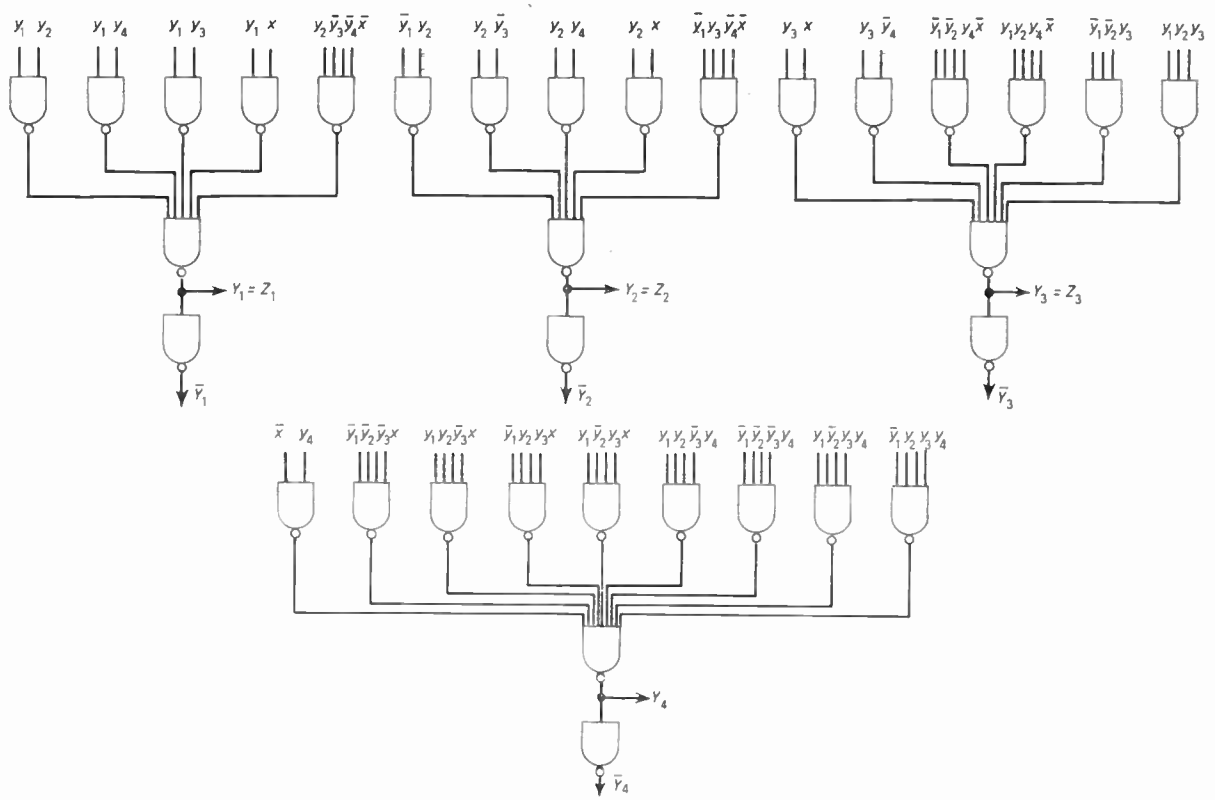


Fig. 3. Implementation of excitation equations for Gray-code counter.

Static hazards can also occur when the output should remain constant at 0 but does in fact change $0 \rightarrow 1 \rightarrow 0$ due to a single input-variable change (i.e. $x\bar{x} \neq 1$). These are called *zero hazards* and Huffman has proved that the logical elimination of one type of hazard will automatically correct for the other. The complete set of excitation equations for the circuit are shown below:

$$Y_1 = y_1y_2 + y_1y_4 + y_1y_3 + y_1x + y_2\bar{y}_3\bar{y}_4\bar{x}$$

$$Y_2 = \bar{y}_1y_2 + y_2\bar{y}_3 + y_2y_4 + y_2x + \bar{y}_1y_3\bar{y}_4\bar{x}$$

$$Y_3 = y_3x + y_3\bar{y}_4 + \bar{y}_1\bar{y}_2y_4\bar{x} + \bar{y}_1\bar{y}_2y_3 + y_1y_2y_4\bar{x} + y_1y_2y_3$$

$$Y_4 = \bar{y}_1\bar{y}_2\bar{y}_3x + y_1y_2\bar{y}_3x + \bar{y}_1y_2y_3x + y_1\bar{y}_2y_3x + \bar{x}y_4 + y_1y_2\bar{y}_3y_4 + \bar{y}_1\bar{y}_2\bar{y}_3y_4 + y_1\bar{y}_2y_3y_4 + \bar{y}_1y_2y_3y_4.$$

The output equations are derived from the assigned flow-table by plotting the required output states on a Karnaugh map (see Table 5). Stable-state outputs are entered first, since the outputs of unstable states may be optional, providing they do not cause transient output changes. The latter can be prevented by noting those stable states which, when involved in a transition, have the same initial and final output states, and then ensuring that unstable states in the transition path have the same output. If the initial and final output states are different, the choice of output for the unstable state is optional. Thus in the counter output maps shown in Table 5, since a transition from ① → ② involves no change in output Z_3, unstable state 2 must be 0. A transition from ② → ③ produces a change in output Z_3 from $0 \rightarrow 1$, consequently unstable state 3 can be optional. The output equations obtained from the maps are:

$$Z_1 = y_1$$

$$Z_2 = y_2$$

$$Z_3 = y_3$$

thus the outputs may be derived directly from the feedback loops and no additional logic is required. The complete logic circuit for the counter is shown in Fig. 3 where it will be noted that thirty-three basic NAND elements are required for the implementation.

2.2. *Modified Design Procedure*

Using the alternative approach, the initial stages of the design are identical. This means that the flow-table is reduced, merged and assigned in the usual manner. This time, however, instead of extracting excitation equations the input equations for d.c. set/reset bistables (i.e. cross-coupled NAND/NOR elements, see Fig. 1) are derived in an analogous

manner to the technique employed in conventional synchronous logic design.[4] The input conditions for a set/reset bistable may be stated as:

Set = 1 when present output Q = 0 and the required next output Q+ = 1

Set = X ('don't-care') when Q = 1, Q+ = 1

Reset = 1 when Q = 1, Q+ = 0

Reset = X when Q = 0, Q+ = 0

Thus to find S_{Y_1}, the input function for setting bistable Y_1, we compare columns y_1 and Y_1 in Table 2(b), noting the value of the present state and input variables for the conditions when $y_1 = 0$, $Y_1 = 1$. These are:

$$S_{Y_1} = \bar{y}_1 y_2 \bar{y}_3 \bar{y}_4 \bar{x}$$

The 'don't care' conditions occur when $y_1 = 1$ and $Y_1 = 1$, thus:

$$\begin{aligned} S'_{Y_1} = {} & y_1 y_2 \bar{y}_3 \bar{y}_4 \bar{x} + y_1 y_2 \bar{y}_3 y_4 \bar{x} + y_1 y_2 y_3 y_4 \bar{x} + \\ & y_1 y_2 y_3 \bar{y}_4 \bar{x} + y_1 \bar{y}_2 y_3 \bar{y}_4 \bar{x} + y_1 \bar{y}_2 y_3 y_4 \bar{x} + \\ & y_1 \bar{y}_2 \bar{y}_3 y_4 \bar{x} + y_1 y_2 \bar{y}_3 \bar{y}_4 x + y_1 y_2 \bar{y}_3 y_4 x + \\ & y_1 y_2 y_3 y_4 x + y_1 y_2 y_3 \bar{y}_4 x + y_1 \bar{y}_2 y_3 \bar{y}_4 x + \\ & y_1 \bar{y}_2 y_3 y_4 x + y_1 \bar{y}_2 \bar{y}_3 y_4 x + y_1 \bar{y}_2 \bar{y}_3 \bar{y}_4 x. \end{aligned}$$

Continuing in this way for the other input functions we can deduce the complete set of input equations, shown plotted on Karnaugh maps in Table 6. The minimized input equations are:

$$S_{Y_1} = y_2 \bar{y}_3 \bar{y}_4 \bar{x} \qquad R_{Y_1} = \bar{y}_2 \bar{y}_3 \bar{y}_4 \bar{x}$$

$$S_{Y_2} = \bar{y}_1 y_3 \bar{y}_4 \bar{x} \qquad R_{Y_2} = y_1 y_3 \bar{y}_4 \bar{x}$$

$$S_{Y_3} = \bar{y}_1 \bar{y}_2 y_4 \bar{x} + y_1 y_2 y_4 \bar{x} \qquad R_{Y_3} = \bar{y}_1 y_2 y_4 \bar{x} + y_1 \bar{y}_2 y_4 \bar{x}$$

$$S_{Y_4} = \bar{y}_1 \bar{y}_2 \bar{y}_3 x + y_1 y_2 \bar{y}_3 x + \bar{y}_1 y_2 y_3 x + y_1 \bar{y}_2 y_3 x$$

$$R_{Y_4} = \bar{y}_1 \bar{y}_2 y_3 x + \bar{y}_1 y_2 \bar{y}_3 x + y_1 y_2 y_3 x + y_1 \bar{y}_2 \bar{y}_3 x$$

The output equations are derived in the normal manner as described above. The logic diagram for the counter is shown in Fig. 4; note that only twenty-four basic NAND elements are required, as compared with thirty-three for the earlier circuit and, moreover, the number of interconnections is considerably reduced. Note also that the OR function can be performed by taking the product terms directly to the input of the bistable NAND gate; the NOR element may be used in an analogous way bearing in mind that the bistable output becomes $\bar{Q}$ and the input variables must be inverted. If the circuit is implemented using Texas TTL logic it would require nine SN7420N dual 4-input NAND units, two SN7430N 8-input NAND units

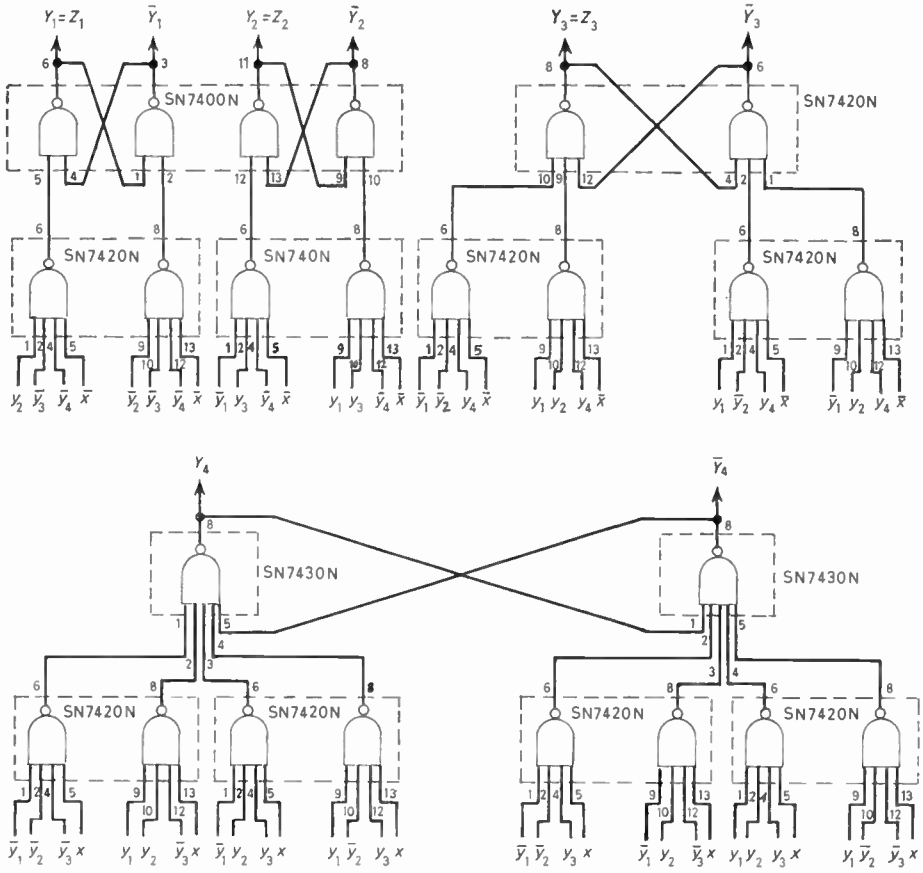
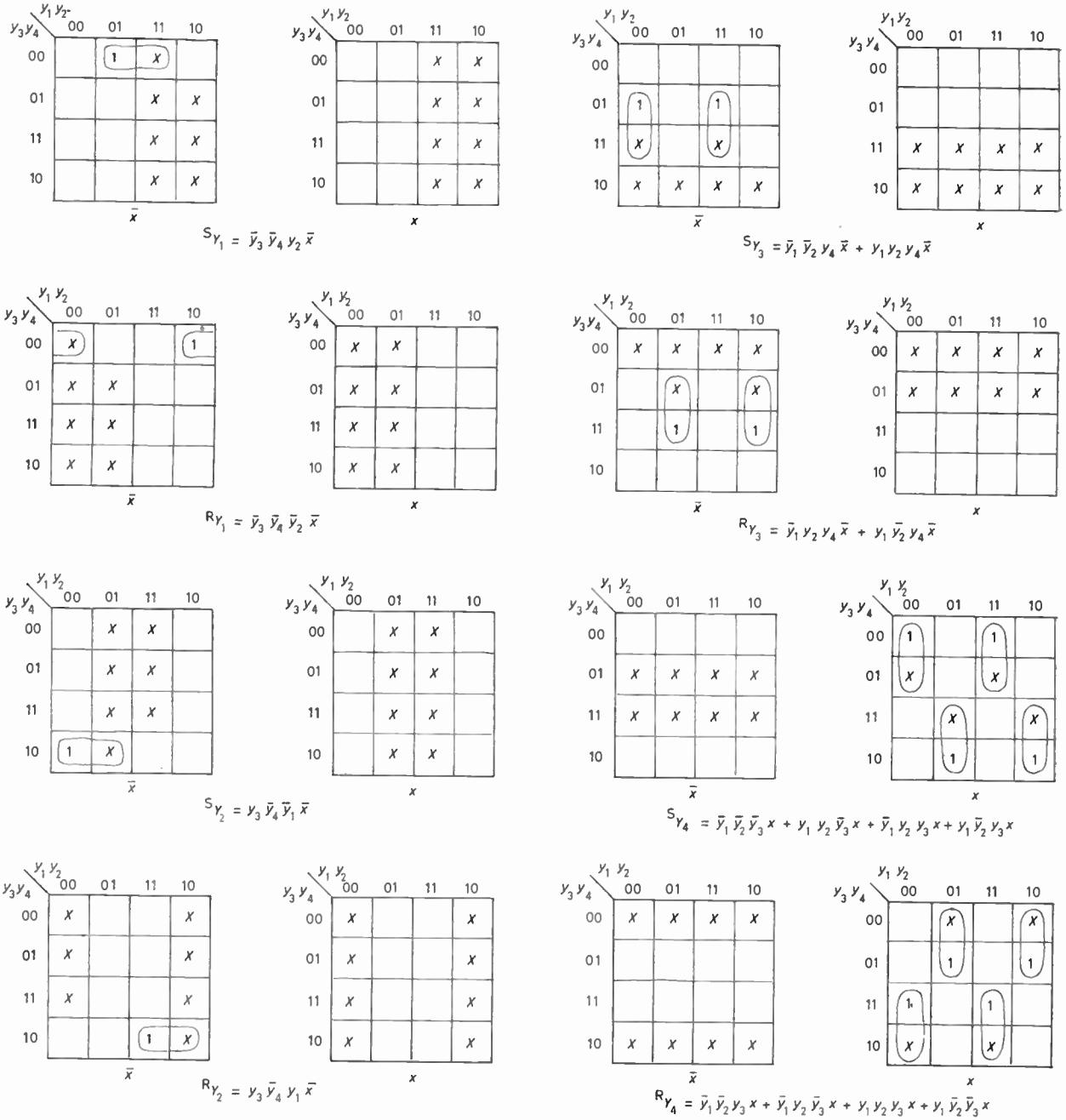


Fig. 4. Bistable version of Gray-code counter.

Table 6

Karnaugh maps for d.c. set/reset bistables



and one SN7400N quad 2-input NAND units, giving a total cost, on the basis of £1 per unit, of approximately £12.

2.3. *Elimination of Static Hazards*

Another very important advantage of using this method is that the static hazard conditions are automatically accounted for by the inherent feedback characteristics of the d.c. bistables. For example, once a bistable is set, variations on the set input will have no effect on its output, since it requires the reset input to go to 1 before a new transition can take place; the same argument holds for the reset input, as can be seen from the truth-table for the SR-bistable (Table 1(a)). This is analogous to using a 'hold-on' contact in the case of relay circuits.

The validity of the hazard-free design technique may be shown theoretically by the derivation of the excitation (i.e. *application*) equations from the bistable set/reset input equations. This is done by using the characteristic equation for the d.c. bistable, which may be obtained from the truth-table shown in Table 1. Thus,

$$Q+ = S+\bar{R}Q$$

(where Q+ is the next output, Q the present output and S and R the set and reset conditions respectively) and substituting the input equations for S and R. Since the expression for Q+ will always be the complete set of prime implicants for the function (this can be proved generally for fully specified machines), there can be no possibility of static logical hazards.[5] This is immediately apparent when the prime implicant terms are plotted on a Karnaugh map since all groups will overlap. Thus:

$$\begin{aligned} Y_3 &= S_{Y_3}+\bar{R}_{Y_3}y_3 \\ &= \bar{y}_1\bar{y}_2y_4\bar{x}+y_1y_2y_4\bar{x}+\overline{(\bar{y}_1y_2y_4\bar{x}+y_1\bar{y}_2y_4\bar{x})}y_3 \\ &= \bar{y}_1\bar{y}_2y_4\bar{x}+y_1y_2y_4\bar{x}+(y_1y_3+\bar{y}_2y_3+\bar{y}_4y_3+y_3x) \\ &\qquad (\bar{y}_1y_3+y_2y_3+\bar{y}_4y_3+y_3x) \end{aligned}$$

Therefore,

$$Y_3 = \bar{y}_1\bar{y}_2y_4x+y_1y_2y_4\bar{x}+y_1y_2y_3+y_3\bar{y}_4+\bar{y}_1\bar{y}_2y_3+y_3x$$

which is of course the complete set of prime implicants for the function Y_3 (see Table 4). A similar result may be shown for Y_4.

It is important to note that the mathematical expressions above have been derived for the output (Q) of the bistable. If the $\bar{Q}$ output is obtained from the feedback loop (as is normally the case with cross-coupled NAND/NOR logic) hazards could still occur due to the fact that NAND bistables will produce ones on both the Q and $\bar{Q}$ outputs if the input conditions S = R = 1 are satisfied. This could occur, for example, if a variable and its complement are used to set and reset (or vice versa) the bistable respectively, assuming all other input conditions are equal to one. With normal single-level circuits, that is circuits with one gate in the path to the bistable set or reset gates (as in Fig. 4), this hazard seldom occurs in practice due to the inherent delay in the bistable. If however multi-level input circuits (or very high speeds) are required, the simple expedient of using an additional invertor to produce $\bar{Q}$ from Q should be employed, since the output Q will always stay constant, as can be seen from the equations above.

It should be emphasized that, though by using this design technique the resultant circuits are free of static hazards, the *essential* hazards, if any, still remain. The essential hazard[4] is basically a critical race between an input signal change and a secondary signal change, and only materializes in very high-speed asynchronous systems. These hazards may be recognized from the flow-table structure and can be eliminated using delay elements[5] or by an adaptation of the circuit techniques due to Zissos.[6]

3. Conclusions

The principal advantage of this modified design technique are:

(1) *Economy in hardware:* This is due in part to the fact that the set and reset input terms can in general be taken directly to the NAND/NOR bistable gates; this is of course limited by the fan-in factor of the element. Perhaps a more important aspect however is that the number of interconnections (and the maximum fan-in) is also considerably reduced in the process.

(2) *Elimination of static hazards:* The necessity to examine the excitation equations for hazards, a difficult and laborious procedure for large variable problems, is obviated.

(3) *Simple circuit structure:* It is easier to understand the operation of an asynchronous logic circuit if presented in terms of bistable devices. This argument is particularly valid from the maintenance engineer's viewpoint, since the rapid assimilation of logical operation is essential to rapid fault-finding.

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Manuscript first received by the Institution on 28th May 1968 and in final form on 29th July 1968. (Paper No. 1223/Comp 108).

U.D.C. 621.382.3

Frequency-response Measurements on Silicon Planar Transistors

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Summary: This paper describes convenient laboratory methods of measuring the hybrid π parameters as a function of collector current. Typical results are given, and the variation of the transition frequency with collector current is discussed.

List of Symbols

General convention: Upper case symbols and suffixes are used for d.c. or instantaneous values of voltage, current or parameter. Lower case symbols and suffixes are used for a.c. or small signal incremental values.

a_v	voltage gain
C	capacitance
$c_{b'c}$	collector-base capacitance (Fig. 2)
$c_{b'e}$	base-emitter capacitance (Fig. 2)
c_{dc}	collector diffusion capacitance
c_{de}	emitter diffusion capacitance
c_{jc}	collector transition capacitance
c_{je}	emitter transition capacitance
C_s	stray capacitance
f	frequency
f_c	corner frequency, at which the gain is 3 dB below its low-frequency value
f_T	transition frequency; the product of $\|h_{fe}\|$ (measured well above its corner frequency) and the frequency of measurement
$f_{T(max)}$	asymptotic maximum value of f_T at large collector current
f_y	frequency at which y_{fe} is reduced by 3 dB
g'_m	mutual conductance between the internal base and the collector (Fig. 2)
h_{fe}	common-emitter current gain
h_{ie}	common-emitter input impedance
I_C	d.c. collector current
$I_{C(corner)}$	collector current at which f_T is reduced to half its asymptotic value
K_1, K_2, n	constants defining $c_{b'e}$ and $c_{b'c}$ (eqns. (1) and (2))
R_S, R_L, R_F	source, load and fixed resistances (see relevant Figures)
$r/(1-r)$	ratio of resistances of two arms of the bridge (Fig. 4)
r_b	series base resistance (Fig. 2)
$r_{b'e}$	base-emitter resistance (Fig. 2)
$V_{B'E}$	d.c. base-emitter voltage
V_{CB}	d.c. collector-base voltage
V_t	$kT/q \simeq 25$ mV at room temperature k = Boltzmann's constant T = absolute temperature q = electronic charge
$v_{b'e}$	a.c. base-emitter voltage (Fig. 2)
y_{fe}	common-emitter mutual conductance
ω_1, ω_2	measured corner frequencies, in rad/s

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1. Introduction

In the last few years silicon planar transistors have become cheap and plentiful. They have low leakage currents and high cut-off frequencies, and make it possible to design low-noise audio amplifiers with many directly coupled amplifying stages and a high degree of negative feedback. Such amplifiers offer much better performance than was previously attainable. But they must be carefully designed to ensure low noise and stability, and the design considerations must extend to relatively high frequencies; for example, an amplifier with 40 dB of negative feedback and a frequency range of 0–20 kHz must have its loop gain and phase controlled up to several megahertz. When the feedback loop contains several stages it is almost impossible to obtain optimum performance by trial-and-error development—there are so many parameters to alter that the process is unlikely to converge. Thus it is necessary to design the amplifier entirely on paper, in order to obtain optimum operating points, circuit configurations and component values.

To perform these calculations one requires detailed information on the frequency-response of each transistor, over the entire usable range of collector currents. Such full information is rarely available in manufacturers' literature.

For these reasons, the practice has grown up in this laboratory of making *ad-hoc* measurements of transistor frequency-response parameters. It is not usually realized how easy such measurements can be,

provided that one takes advantage of the amplifying action of the transistor itself. A good example of this is provided by the method which we usually employ for the measurement of collector-base capacitance $c_{b'c}$. The test rig shown in Fig. 1 can be put together in a few minutes, and its bandwidth ω_1 is dominated by collector-base feedback and is in the audio-frequency range. When ω_1 has been measured, the capacitor C (usually 10 pF) is soldered into the circuit and the new bandwidth ω_2 is measured. The required transistor capacitance $c_{b'c}$ is then obtained from the relation

$$\frac{\omega_2}{\omega_1} = \frac{c_{b'c}}{C + c_{b'c}}$$

It is often possible to use the same test rig for the measurement of f_T if the 47 kΩ resistor is shorted out. If the transistor has a current gain of 150 and f_T of 100 MHz, the bandwidth to be measured will be less than 1 MHz.

Although these 'spot' measurements are extremely valuable, we have found it necessary to supplement them with a series of systematic measurements which are designed to enable us to characterize a transistor so that we can predict its frequency response at any value of collector current. The principle throughout has been to combine simple theory with practical measurement: the measurements serve both to confirm the theory and to give numerical values to the parameters. In this paper we give the results for six transistor types, all low- or medium-power n-p-n silicon planar devices.

2. Simple Theory

The analysis is based on the hybrid π equivalent circuit of the transistor.[1] The important elements for a silicon planar transistor are shown in Fig. 2.†

At low frequencies the effect of the capacitors is negligible, and the performance depends on the other elements. r_b represents the ohmic resistance of the base region between the base connection b and the effective part of the base b' within the transistor; it is usually less than 500 ohms and frequently about 100 ohms. $r_{b'e}$ and g'_m depend on the transistor action, and are discussed theoretically in the above reference; they have been measured for silicon planar transistors by Faulkner and Dawnay,[3] who show that $g'_m \propto I_C$ (as is expected theoretically) and that

$$r_{b'e} = \frac{h_{fe}}{g'_m} \propto I_C^{-m}$$

† More accurately, the collector-base capacitance should be divided between the junction capacitance $c_{b'c}$ and the header capacitance c_{bc}. But since r_b is small, this refinement is usually unnecessary. Throughout this paper, $c_{b'c}$ includes the header capacitance.

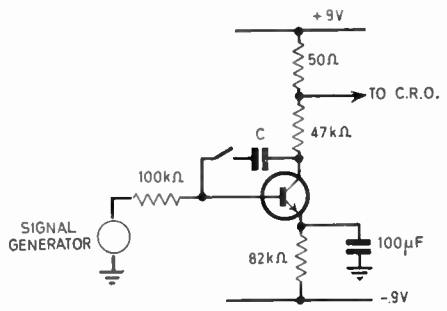

Fig. 1. Test rig for measuring the collector-base capacitance of a transistor.

where m usually lies between 0·65 and 0·90.‡

$c_{b'e}$ is the sum of the emitter transition capacitance c_{je} which depends on $V_{B'E}$ and the emitter diffusion capacitance c_{de} which is theoretically proportional to I_C. Since $V_{B'E}$ changes very little with I_C, one expects a relation

$$c_{b'e} = c_{je} + K_1 I_C \qquad \text{.....(1)}$$

where c_{je} and K_1 are constants. The value of K_1 should decrease with increasing V_{CB}, for this decreases the base width and so the stored charge in the base region.

$c_{b'c}$ is the sum of the collector transition capacitance c_{jc} and the collector diffusion capacitance c_{dc}. Since the collector junction is reverse biased, c_{dc} is almost constant, while $c_{jc} \propto (V_{CB})^{-n}$, where n lies between one half and one third. So one expects

$$c_{b'c} = c_{dc} + K_2 (V_{CB})^{-n} \qquad \text{.....(2)}$$

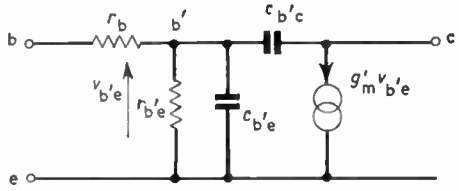

Fig. 2. The hybrid π equivalent circuit of a silicon planar transistor.

It is difficult to predict theoretically the relative values of c_{je}, c_{dc}, K_1 and K_2.

3. Measuring Techniques

The basic experiments are those in which one measures the frequency-response of the transistor in the common-emitter configuration (Sect. 3.1). These confirm the validity of the equivalent circuit. However, if the equivalent circuit can be assumed correct, routine

‡ Reference 3 discusses $h_{ie} = r_{b'e} + r_b$. But since r_b is small, the difference is not significant when I_C is small.

measurements can be performed more quickly by using a bridge technique (Sect. 3.2) to measure the common-emitter input impedance.

3.1. *Frequency-response Methods*

When the transistor is used as a common-emitter amplifier (Fig. 3), it can readily be shown[2] that if the equivalent circuit of Fig. 2 is valid, the frequency-response has the form of a simple lag, whose corner frequency is given by

$$2\pi f_c = \frac{R_S + r_b + r_{b'e}}{r_{b'e}(R_S + r_b)\{c_{b'e} + (a_v + 1)c_{b'c}\}} \quad \ldots\ldots(3)$$

where a_v, the magnitude of the low-frequency voltage gain from base to collector, is $g'_m R_L$.

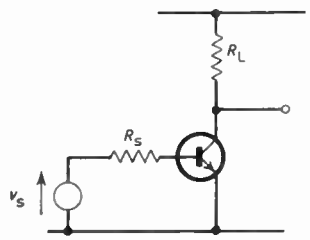

Fig. 3. The common-emitter amplifier.

The corner frequency can be found by driving the transistor from a signal generator and by displaying the output on an oscilloscope. At a low frequency, the input is set to give a convenient output; then the frequency is increased (without change of input level) until the output falls by 3 dB. This frequency is the corner frequency.

Test circuits similar to Fig. 1 have been constructed with arrangements for switching in different emitter resistors to vary the collector current, and for setting values of R_S, R_L and C. As described in Section 1, $c_{b'c}$ can be measured with a single setting of R_S and R_L, and changing C from zero to a suitable value. Values for $c_{b'e}$, $r_{b'e}$ and r_b can be found by keeping R_L small and measuring the low-frequency gain and corner frequency with two values of R_S (usually 50 Ω and 10 kΩ). The applicability of eqn. (3) may be confirmed by using a third value of R_S and comparing the measured corner frequency with that predicted from these parameter values.

Stray capacitances between the emitter, base and collector pins of the test rig are of course included in the measured values. This means that care must be taken in the design of the test rigs not to introduce unusually high stray capacitances.

3.2. *The Bridge Method*

Once the equivalent circuit has been established, it is easier to measure the capacitances by making bridge measurements of the common emitter input impedance of the transistor. If r_b can be neglected, the input impedance is just $r_{b'e}$ in parallel with $c_{b'e} + (a_v + 1)c_{b'c}$.

The simple bridge described here (Fig. 4) is constructed with ordinary circuit components and operates at 100 kHz. The switched resistors are mounted on a 12-position wafer switch, the continuously variable resistor is a 1 kΩ carbon potentiometer, and the variable capacitor C, is an Eddystone type 738 with a slow motion drive. The resistances of the ratio arms, r and $(1-r)$, have been made low to reduce the effect of their inevitable stray capacitance. C is variable from 10 to 100 pF, and R_F is usually 10 kΩ, but may have to be altered by as much as a factor of 10 either way to obtain a balance. The differential amplifier has high-impedance (emitter-follower) inputs. The tuned amplifier is an active filter[4] with a Q of 40 and a gain of 40.

The ratio, r, is calibrated by d.c. measurements. Then C can be calibrated and the stray capacitance C_s can be found by using the bridge to measure a series of known parallel R-C combinations.

The usual arrangements are made for varying the current in the test transistor and the collector load resistance.

Parasitic oscillations at high frequencies can be troublesome, especially when high-frequency transistors are tested at high collector currents. The effect can be reduced by careful decoupling, using short leads to minimize stray inductance.

4. Results

Measured values of $c_{b'e}$ for a single 2N3707 are plotted against I_C in Fig. 5; they agree well with the expected linear relation. The agreement between the bridge measurements and those using frequency-response methods confirms the validity of the equiva-

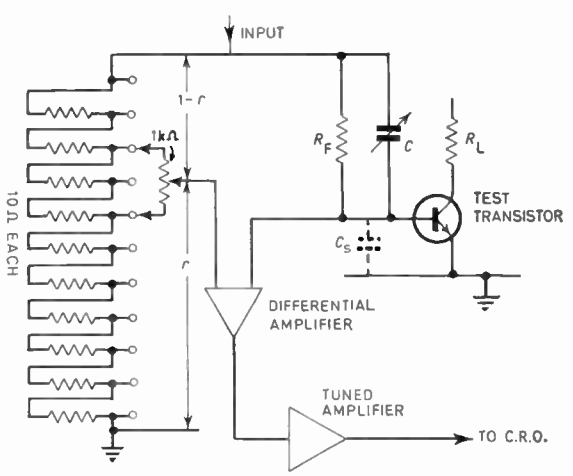

Fig. 4. Bridge circuit for measuring transistor input impedance.

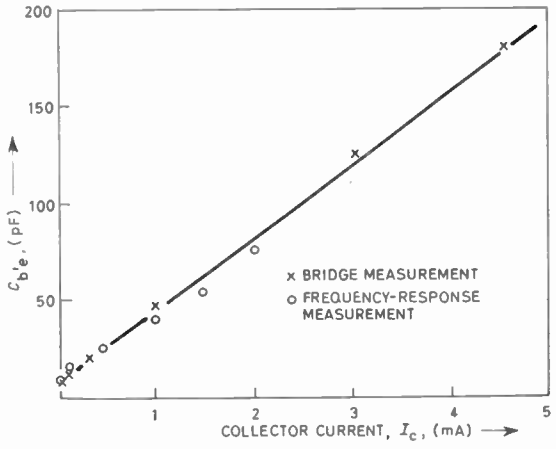

Fig. 5. The variation of base-emitter capacitance, $c_{b'e}$ with collector current for a single 2N3707 transistor. $V_{CB} = 5$ V.

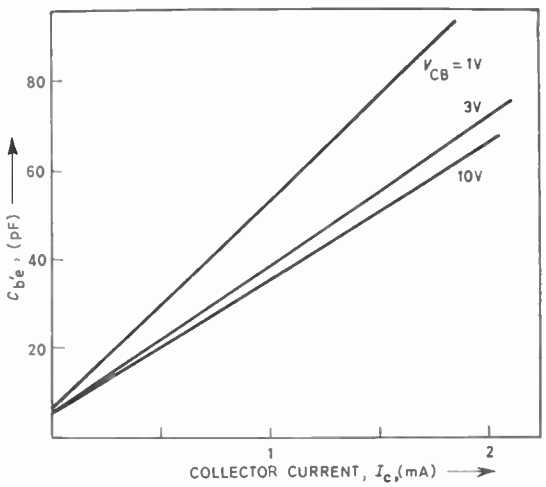

Fig. 6. The variation of $c_{b'e}$ with I_C at three values of collector-base voltage. Same 2N3707 transistor as in Fig. 5.

lent circuit. Other transistors give similar results, though for some types $c_{b'e}$ falls below the straight line at currents above 1 or 2 mA.

Figure 6 shows how this curve moves as V_{CB} is changed. Up to $V_{CB} = 5$ V, the slope decreases as V_{CB} increases, as is expected theoretically. But above 5 V there is no significant change.

Measured values of $c_{b'c}$ for another 2N3707 transistor are plotted against V_{CB} in Fig. 7 for two values of I_C. There is no significant change with I_C. The curve can be fitted by eqn. (2) with K_2 small and, $n = 0{\cdot}5$, but none of the parameters can be determined very accurately. In practice it is usual for V_{CB} to be 5 V or higher, where $c_{b'c}$ is changing slowly, and it is sufficient to take a single value for it.

Table 1 summarizes the measurements for six transistor types. Apart from the capacitances, measured values of r_b are given, and the manufacturer's values of h_{fe} are quoted. These values represent mean values of measurements carried out on several transistors. The estimated error given is a standard deviation that includes both the experimental error and the spread of values over several samples of each transistor.

The values in Table 1 determine the parameters of the equivalent circuit (Fig. 2) in conjunction with the following equations:

$$\left.\begin{aligned} g'_m &= I_c/V_t \qquad V_t \simeq 0{\cdot}025\ V \text{ at room temperature} \\ r_{b'e} &= h_{fe}/g'_m \\ c_{b'e} &= c_{je} + K_1 I_C \\ c_{b'c} &= c_{dc} + K_2/\sqrt{V_{CB}} \end{aligned}\right\} \quad \text{.....(4)}$$

Table 1

Data for calculating equivalent circuit parameters of several transistors

Transistor type	Capacitances at $V_{CB} = 5$ V			$c_{b'c}$ (different V_{CB})		r_b	h_{fe}	$f_{T(max)}$	$I_{C(corner)}$
	$c_{b'e}$		$c_{b'c}$						
	c_{je} pF	K_1 pF/mA	pF	c_{dc} pF	K_2 pF V$^{-\frac{1}{2}}$	Ω		MHz	mA
Motorola MPS6555	61	67	5	3·3	3·9	500	typically 150	95	1·0
Texas 2N3707	8	38	2·7	1·9	1·8	100	100–400	170	0·28
Texas 2N3704	37	30	4·6	2·5	4·7	50	100–300	210	1·4
RCA 2N3053	55	30	10·6	3	17	100	typically 70	210	2·2
Texas 2N4254	0·4	19	2·0			150	>50	340	0·13
Motorola MPS3646	10	12·5	2·7	1·7	2·2	50	30–120	510	1·0
Estimated error	10%	10%	20%	30%	30%	30%			

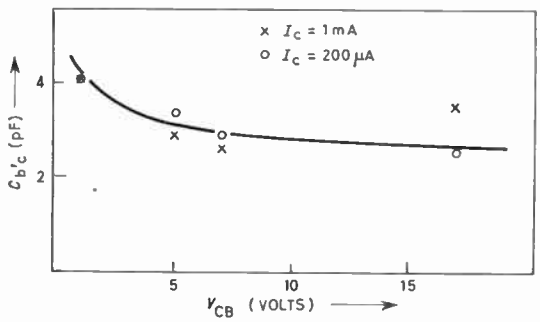

Fig. 7. The variation of collector-base capacitance, $c_{b'c}$, with collector-base voltage, V_{CB}, for a single 2N3707 transistor.

These relations hold within about 10% over a range of I_C from a few microamperes to a few milliamperes, a range of V_{CB} from 1 V upwards and a range of frequencies from d.c. to 20 MHz or higher.

5. The Variation of f_T with I_C

The commonest measure of the high-frequency performance of a transistor is its transition frequency f_T. This is defined as the product of the modulus of the current gain h_{fe} and the frequency at which it is measured, when the measuring frequency is well above the corner frequency of h_{fe}; since $h_{fe} \propto 1/f$ in this region, f_T is independent of the measuring frequency.

It can readily be shown from the equivalent circuit (Fig. 2) that

$$f_T = g'_m/2\pi(c_{b'e}+c_{b'c})$$

and hence that the variation of f_T with I_c is given by

$$f_T = 1\Big/\left\{2\pi V_t\left(\frac{c_{je}+c_{b'c}}{I_C}+K_1\right)\right\} \qquad .....(5)$$

This equation indicates that at high currents f_T tends to a limit $f_{T(max)} = 1/2\pi V_t K_1$ which depends only on K_1 and is independent of I_C. At low currents f_T falls, and approaches the asymptotic value

$$I_C/2\pi V_t(c_{je}+c_{b'c})$$

The asymptotes meet at the collector current

$$I_{C(corner)} = (c_{je}+c_{b'c})/K_1$$

The curve is completely defined by the values of $f_{T(max)}$ and $I_{C(corner)}$, and can be adequately represented by using its asymptotes as a straight line approximation. Figure 8 shows the curve and its asymptotes for a typical 2N3707 transistor. Values of $f_{T(max)}$ and $I_{C(corner)}$ for the six transistor types are given in Table 1.

In practice, this relation holds up to collector currents of a few milliamperes. Above this current, other effects cause f_T to fall again, so measured curves show a maximum. Manufacturers' values of f_T are usually near this maximum, and so approximate to $f_{T(max)}$.

In Fig. 9, the straight line approximation is used to compare the six transistors tested. Clearly, if I_C is greater than 1 mA, the highest frequency transistors are the MPS3646 and 2N4254, as would be expected from the literature, and the 2N3704 is better than the 2N3707. But below 100 μA the 2N3707 is better than all the others except the 2N4254, which retains its performance by having very low values of c_{je} and $c_{b'c}$.

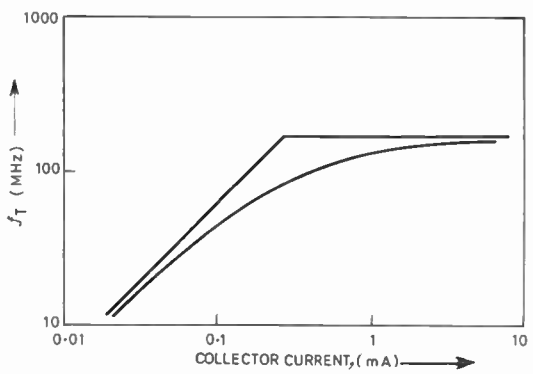

Fig. 8. The variation of transition frequency, f_T, with collector current I_C for a typical 2N3707 transistor. The curve is calculated from eqn. (5), and the straight line approximation from its asymptotes.

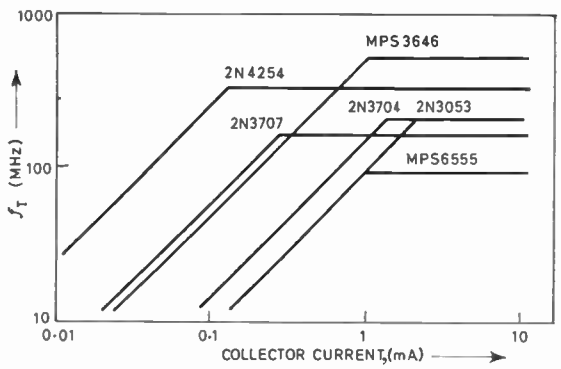

Fig. 9. The variation of transition frequency, f_T, with collector current for the six transistors of Table 1 (straight line approximation, drawn with logarithmic axes).

The results have been assessed first in terms of f_T because it is so widely used to measure the frequency response of a transistor. The use of f_T implies that h_{fe} is the important parameter, and hence that the transistor is driven from a high impedance source. In practice, a transistor is frequently driven from a source impedance that is much lower than $r_{b'e}$ (this can be shown, for example, to improve the noise performance). In the limit, when the source impedance tends to zero, the gain depends on y_{fe}. The frequency response shows a simple lag, with a corner frequency

$$f_y = 1/2\pi r_b(c_{je}+c_{b'c}+K_1 I_C) \qquad .....(6)$$

The variation of f_y with I_C (in the straight-line approximation) is plotted in Fig. 10 for each transistor. The greatest bandwidth is obtained when I_C is very low, and the relative merits of the transistor types differ considerably from those of Fig. 9.

If an intermediate source impedance is used, the computation becomes more difficult. It is usually easier to analyse the circuit, using the equivalent circuit of the transistor with the appropriate capacitances, than to derive the performance from f_T or f_y. Figures 9 and 10 show how much the bandwidth can depend on the choice of operating point and source impedance, and how dangerous it is to rely on published values of f_T when selecting transistors for particular applications.

6. Note on Manufacturers' Parameters

Manufacturers do not yet give all the relevant parameters of their transistors but they are beginning to give more frequency-response information than just a single value of f_T. The usual extra parameters are:

f_T at a range of collector currents;

$c_{b'c}$ at one operating point, usually called C_{ob}, C_{obo} or C_{cb}, and measured at $I_E = 0$. Like the measurements reported in this paper, it includes header capacitance;

c_{je} or something near it, usually called C_{ib}, C_{ibo} or C_{TE}, and measured with the transistor cut off, or even with the base-emitter junction reverse biased, which would make the measured capacitance lower than c_{je}.

Given these and h_{fe}, and guessing r_b as 100 ohms,† the full equivalent-circuit for any value of I_C can be obtained. But in critical cases it is advisable to check the important parameters by *ad-hoc* measurements.

7. Conclusions

This paper has described techniques for measuring transistor frequency-response parameters, and Table 1 gives data for calculating the equivalent circuit parameters of several transistors over a very wide range of operating points. The measurements are not particularly accurate, but great accuracy is not required because of the variation between different transistors of one type, and it is unnecessary when designing feedback amplifiers. The closed-loop performance of the amplifier, which alone needs to be closely specified, depends almost entirely on a few passive components,

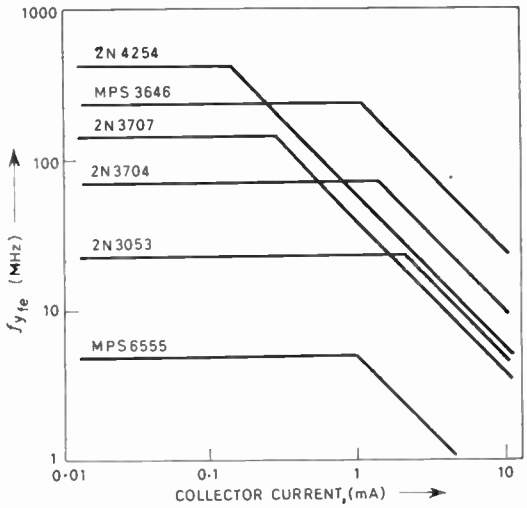

Fig. 10. The variation of f_y, the corner frequency of y_{fe}, with collector current for the six transistors of Table 1 (straight line approximation, drawn with logarithmic axes).

and very little on the transistor parameters. The stability calculations on the other hand depend on the transistor characteristics, but it is usually sufficient to calculate pole locations within a factor of two. If the pole locations are unsatisfactory the necessary adjustments can be made at the design stage by changing the operating points of some of the transistors or adding external components. A knowledge of the variation of transistor performance with operating point is of much more use than extremely accurate parameter-values at one point.

8. Acknowledgments

This work was done in collaboration with the Electronics Group of the J. J. Thomson Physical Laboratory. The author acknowledges the assistance of Mr. D. H. Findlay and Mr. R. Horgan with the experimental work.

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Manuscript first received by the Institution on 21st March 1968 and in final form on 11th July 1968. (Paper No. 1224.)

† Since r_b cannot be derived, it must either be measured or guessed. As r_b is seldom a critical component in the circuit, usually a guess is admissible.

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Microwave Phonons

By

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Based on a lecture at an Institution meeting held in London on 29th November 1967.

Summary: Experiments which use coherent waves at frequencies near 10^{10} Hz are possible in suitable materials at low enough temperatures. The techniques which are used are determined by the very short acoustic wavelength ($\sim$ 5000 Å) and by the availability of transducers and detectors. An interesting area of research is into their use for spectroscopic purposes in crystals, a technique which is complementary to electron spin resonance (e.s.r.). As the selection rules and the quantities which govern the intensities are quite different, it is possible to detect impurities which e.s.r. misses. By obtaining information on the strength of the impurity-lattice vibration coupling a good deal of light is thrown on the problem of spin-lattice relaxation. The propagation of pulses in the vicinity of absorption lines gives some striking demonstrations of anomalous propagation. A related technique is that in which the waves are generated incoherently from a black body source. This extends the range of frequencies which can be used, though at the expense of increased difficulty in the interpretation of the results. Nevertheless, some remarkable changes in the thermal conductivity of crystals at low temperatures can be obtained in a magnetic field. The general field is one of considerable promise and some possible directions in which developments may occur are outlined.

1. Introduction

The study of the electronic energy levels of impurities in crystal lattices is a topic of considerable interest in solid-state physics. Line spectra are often observed, which show that the energy levels of the impurities are discrete, and that the exchange of energy with the environment is a comparatively improbable process. When such an exchange does take place, with the impurity emitting energy, the energy may appear in the form of an electromagnetic disturbance. On the other hand, it may appear in some other form, such as acoustic energy, or, in magnetic crystals, as spin-wave energy. But in whichever form it appears it is a challenging problem to try and understand the factors which determine the absolute and the relative probabilities for the various possibilities.

It is sometimes possible to deduce which process will dominate, but it is clearly preferable to observe the emitted energy. When it is electromagnetic the problem is comparatively simple, for much effort has gone into the detection of electromagnetic waves over a wide frequency range. When it is acoustic the problem of detection is much more severe, particularly if the frequency is somewhere near the Debye limit, say 10^{13} Hz.

2. Absorption of Acoustic Waves

An alternative procedure is to use the well-known result that any emitter is also an absorber, irradiate the impurity with acoustic waves and examine the absorption. The difficulty is then to generate and detect the acoustic waves, and until quite recently this has only been possible up to about 10^8 Hz, for a variety of reasons. One reason is the very short wavelength involved for, taking the velocity of sound as 5×10^3 m/s, the wavelength at 10^{10} Hz is 5000 Å (0·5 μm) and resonant transducers are becoming rather thin. The other main reason is that the attenuation increases with frequency to inconveniently high values, at least at room temperature. The position changes very considerably, however, if the experiments are made at liquid helium temperatures, and it appears that in a number of crystals the attenuation is virtually negligible, up to the highest frequencies ($\sim 10^{11}$ Hz) which have been used.[1] In the early experiments the resonant transducer problem was overcome as follows. A rod of x-cut quartz, of diameter 3 mm and length 20 mm was inserted into a cavity so that when the cavity was excited by a pulse of microwave electromagnetic radiation a strong oscillating electric field was set up across one end of the rod. Each volume element then acts as a source of acoustic radiation, using the piezo-electric effect in quartz. All the elements are driven in phase, the wavelength of the acoustic radiation is about 10^{-5} of that of the electromagnetic wave, and there is a good deal of destructive interference. So much, in fact, that an acoustic pulse appears to be launched from the end-face of the rod

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(see Fig. 1). The shape of the wavefront depends on the geometry of the system, and it is good practice to require the end of the rod to be flat to at least one-fifth of the wavelength of sodium light. Then something approaching a plane, longitudinally polarized acoustic pulse will travel down the rod. With $\nu = 10^{10}$ Hz and a pulse duration of 1 μs the wave train will contain 10^4 wavelengths in an overall length of 5×10^{-3} m. It will take about 2 μs to go down the rod. At the far end it will be reflected and on returning to the launching end it will re-excite the

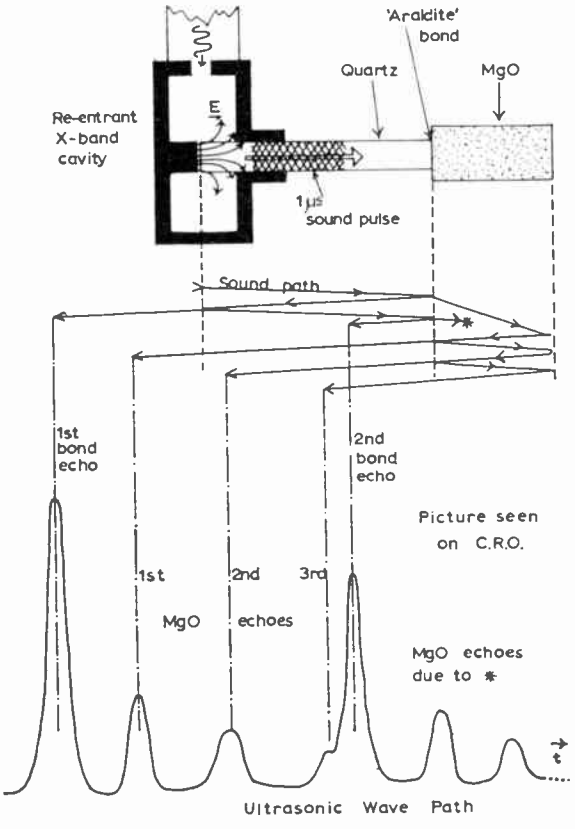

Fig. 1. Re-entrant x-band cavity arrangement.

microwave cavity, again by the piezo-electric effect (in reverse this time). The pulse will make many trips along the rod, gradually becoming attenuated, or dephased. The time intervals are such that while the pulse is traversing the rod the microwave generating system can be converted into a receiver. It is essential that the far end of the rod, where the reflection occurs, should also be flat, and as parallel as possible to the launching end, for the detection depends on the mean phase across the launching end. A plane wave striking it at an angle to the normal may well fail to excite the cavity electromagnetically, due to destructive interference. Even under the best conditions the efficiency of conversion from e.m. to acoustic power, and vice versa, is low, but so far this has not proved to be too much of a limitation, for experiments can be done. As always, though, it is to be expected that improvements in sensitivity may lead to the discovery of new and unexpected phenomena.

The experiment is very like a radar system, but using sound in a solid rather than e.m. waves in free space. Indeed, if it becomes possible to effect all the standard manipulations of amplification, detection, etc., of acoustic waves, rather than e.m. waves, the size of microwave systems might be considerably reduced. However, before real progress along these lines becomes possible, a good deal of development is necessary, particularly of transducers and amplifiers. Encouraging progress has been obtained by a return to the resonant transducer, replacing the rod of quartz by a thin film on a suitable substrate. Cadmium sulphide films have been used successfully. (Their deposition seems to be an art rather than a science.[1])

Assuming that the wave can be launched the next question to consider is what to do with it. The usual practice is to pass it through the material of interest via a suitable bond, and back again, for in general it is not possible to detect the wave in the material of interest. One set of experiments is simply to measure the velocity and the attenuation as functions of temperature. Not too much has yet been published, but some results are given by de Klerk[1] (Al_2O_3, MgO, TiO_2) and also by Lewis[2] (spinel) and Smolyakov *et al*,[3] ($LiNbO_3:Cr^{3+}$). An interesting result of this work is that there are indications that the attenuation at room temperature, in specific crystals, is not as high as was previously supposed, and that it may become possible to study the properties of these waves even at room temperature. The whole question of what determines the attenuation is raised by Oliver and Slack,[4] and it has been suggested that the attenuation at frequencies near 10^{10} Hz can be altered by changing the attenuation of waves near the Debye limit, by adding certain impurities to the lattice. The point is that the irreversible loss at 10^{10} Hz is determined by anharmonic couplings to much higher frequency lattice modes, and the loss is reduced if these can be kept in thermal equilibrium.

3. Acoustic Paramagnetic Resonance

Our interests at Nottingham have been directed in a different direction, namely the interaction of acoustic waves with impurity energy levels, which is the acoustic analogue of electron paramagnetic resonance. The wave is passed through a substance containing

paramagnetic ions, and the ionic energy levels are adjusted by means of an externally applied magnetic field. When resonance is reached the energy separation matches the quantum of the acoustic wave, and the wave shows attenuation and a velocity change. It is comparatively easy to study the effect as the direction of the magnetic field is varied, but it is less easy to vary the direction and polarization of the acoustic pulse, as this is usually determined by the sample. Nevertheless a good many different experimental situations can be realized, and in favourable cases a reasonably complete picture of what is happening can be built up. The theory of the energy levels of paramagnetic ions in crystals involves the details of the charges and positions of neighbouring ions. In the presence of the sound the positions are being periodically varied, and it is this modulation which modifies the orbits of the unpaired electrons. These changes are then conveyed to the electron spin via the spin-orbit coupling. The details of the process are quite complicated, but they are understood. It is, however, important to appreciate that different paramagnetic ions seem to couple in different ways, as far as magnitudes are concerned. In electron paramagnetic resonance (e.p.r.) the quantity that primarily determines the coupling of the ion to the e.m. wave is the Bohr magneton, and all ions have about the same couplings. The coupling to an acoustic field involves the crystal field and the spin-orbit interaction, and the net effect is that some ions seem to be much more strongly coupled than others. This property can also be recognized directly in e.p.r. spectra. Ions which are strongly coupled to the lattice have broad resonance lines. Thus if it were possible to increase the lattice coupling gradually, an e.p.r. line would broaden with constant area. That is, its height would decrease as its width increased. If, however, the same transition were observed using ultrasonic excitation, the line would again broaden, but its intensity would increase, so that its height remained constant. This is because the excitation takes place by the same mechanism which gives the width. It follows that high sensitivity in e.p.r. is associated with ions which are weakly coupled to the lattice, for it is peak height compared with the noise background which matters. In acoustic excitation the ions most easily detected are those which are strongly coupled to the lattice, and the two techniques are therefore complementary. A further difference is that the selection rules for acoustic excitation are different from those for e.m. excitation, so transitions which are forbidden in e.p.r. may not be forbidden in acoustic paramagnetic resonance (a.p.r.).

These points were shown to be of considerable importance in some of our early experiments. In one set an attempt was made to pass ultrasonic waves at 10^{10} Hz through a sample of magnesium oxide which had been doped with chromium ions. No echoes were obtained, for any values of the magnetic field. In such a situation one does not know whether this is because the transmission through the various bonds is poor, so that the echo is too weak to be detected, whether the crystal polishing and alignment is giving a distorted wave front, or whether the impurity ions are completely absorbing the pulse. We now know that the absence of the echo was due to absorption. At the time we were fortunate in having thermal conductivity results on the same sample, a point to be discussed later (Sect. 6). In a similar experiment now, it is probable that we would use the purest MgO available. All MgO contains transition metal ions as impurities, and ferrous and chromous ions are particularly easily detected by a.p.r. Chromic ions can be detected by e.p.r., but not chromous ions. X-irradiation is a particularly useful tool, for it can be used to change the valencies of ions. For example, chromic ions can be converted into chromous ions and it seems that our original samples, doped with chromium, contained a fair number of ions in the chromous state, enough to attenuate the pulse so that the echo was unobservable. A detailed study[5] has been made of the properties of chromous ions, present in concentrations of the order of a few parts in 10^7, and Fig. 2 shows a typical spectrum. It varies as the direction of the field is changed, with the temperature, with external strain, and to some extent from specimen to specimen. No information about chromous ions is available from e.p.r. measurements, and the theoretical interpretation of the results presented some new features, the most interesting of which are connected with the Jahn–Teller effect.

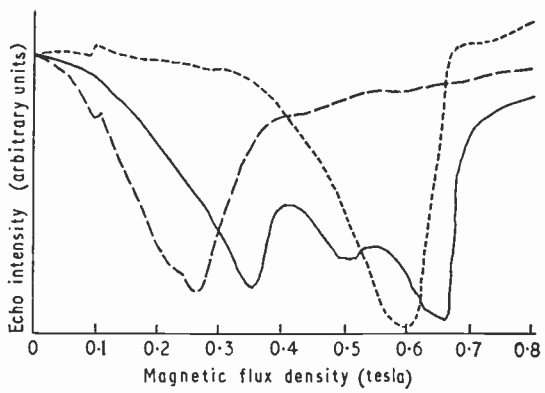

Fig. 2. Acoustic paramagnetic resonance spectra of chromous ions in magnesium oxide taken at 4·2°K. Full curve: no applied stress; dotted curve: compression applied along Z(001); broken curve: compression applied along Y(010) (after Marshall and Rampton[5]).

A chromous ion substituting for a magnesium ion in MgO would be in an octahedron of oxygen ions. The orbital levels of the chromous ion, $3d^4\ {}^5D$, would be split, so that there would be a low-lying doubly degenerate orbital level. However, the ion is not really at a truly octahedral site, for the lattice is vibrating due to thermal motion, and the perfect octahedral symmetry is constantly being disturbed. Now any disturbance splits the doublet, and it is a straightforward calculation to show that the order of magnitude of the splitting is likely to be much larger than any splittings coming from spin-orbit or Zeeman effects. Further, the magnitude of the splitting may be time-dependent, but even if it is not, the nature of the state of lowest energy keeps changing. Such an effect is an example of the dynamic Jahn–Teller effect[6] and it is difficult to treat. In the above description it is implied that the vibrations of the neighbours are determined solely by the temperature, and that they would be unaltered if the chromous ion were replaced by a magnesium ion. In fact, it is more complicated than this, and the presence of chromous ion appears to give additional distortions, through a non-linear coupling with the lattice vibrations. Incident lattice waves of high frequencies may mix at the chromous ions to give local disturbances of large amplitudes and much lower frequencies. The theory is given by Bates *et al.*[7] The further steps which are needed to take into account the spin-orbit coupling and the Zeeman effect, and thereby to interpret the experimental results, are described by Fletcher and Stevens.[8] It has seemed of importance to devote considerable effort to understanding what is happening. Acoustic paramagnetic resonance could be regarded as the difficult way of doing e.p.r. In fact, by choosing the right system it provides a powerful method of studying the way in which orbital levels couple to lattice vibrations, and here e.p.r. is of much less value.

A variety of impurities and hosts have been studied. Vanadium ions in various states of ionization have been studied in MgO, and what is thought to be the chromous ion has also been observed in Al_2O_3 (ruby). Our group has done little with rare earths and higher transition groups, but something is known from the work of others. Where new spectra have been seen the interpretations appear to be incomplete.[9,10] Another promising area is the study of R-centres (clusters of f-centres) and pair spectra, as well as the usual iron group ions in other host crystals.

4. Propagation of Pulses in Crystals

Turning now to a consideration of the propagation of the pulses it is immediately seen that the experiments deliberately tune the spin systems to be in resonance with the ultrasonic waves. That is, the propagation is in the vicinity of an absorption line, and it is to be expected that phenomena associated with anomalous propagation will occur. Further, by using acoustic waves the time intervals involved are comparatively long, particularly when compared with similar e.m. experiments, and a number of experiments which one would like to see done with e.m. waves can much more easily be done using acoustic waves. Another useful feature is that not only does the magnetic field provide a way of tuning the resonant systems, but by varying its orientation relative to the direction of propagation the strength of the coupling can also be altered.

Suppose that a pulse, with frequency near resonance, is propagating through a medium containing two-level spin systems, and that it is approaching a spin which is in its lower energy state. When the pulse arrives the spin begins to respond, rather like a tuned circuit shows forced oscillations when driven slightly off resonance. Energy is thereby stored in the spin oscillation, which can only have come from the front of the pulse. The front is therefore attenuated. The whole process can alternatively be regarded as follows. The 'ringing' motion of the spin is coherent with the pulse and launches a secondary pulse into the medium. Interference takes place between the primary and secondary pulses, resulting in a weakening in the front of the pulse, and a phase change as measured by an observer deeper into the medium. A similar effect takes place at each such spin, the front is successively eroded, and the pulse appears to be late arriving, or slowed down. Its phase is also changed relative to a reference pulse. When the primary pulse has passed over a spin the ringing does not immediately cease, and the secondary wave continues for a short while. In this way the end of the pulse is built up, so that the overall duration of the pulse appears to be unchanged. In our experiments the quantum of acoustic energy is less than kT, so that in a given sample there will be an appreciable proportion of the spins in the upper state when the pulse approaches. They will also respond, but their associated secondary pulse will differ in phase by π radians from ground-state spins, and the front is reinforced. Unless the initial populations are reversed there will always be more spins in the lower state than the upper, and a pulse will be slowed and changed in phase by amounts which are proportional to the difference in numbers of down and up spins, that is, to the magnetization. Thus as the temperature of a sample is changed, the populations alter and so does the dispersion.

The above argument is only valid if the effect of the pulse on a given spin can be regarded as a small perturbation. That is, it is a weak pulse, or if it is of high intensity it is of short duration. When a strong pulse is used, which is certainly possible, the

propagation characteristics can be quite different. Then a given ground-state spin may be excited to its upper state and back again many times during the passage of the pulse. Energy is then alternately taken from and delivered to the pulse, and the emergent pulse can be quite different in shape from the incident one. Exactly what happens depends on the various relaxation processes which occur in the spin system, but a theoretical study of a similar problem with optical radiation suggests that a sequence of short pulses may emerge, each one containing just enough energy to make any given spin make precisely one round trip.[11] Apart from relaxation losses such a pulse should propagate without change of shape. This is a phenomenon of some interest to us, for in many of our experiments the pulses do not appear to be delayed, even though strong absorption occurs. A limitation arises because to optimize the sensitivity the bandwidth for detection is deliberately restricted, and information about changes in the pulse shape may be lost. It may be noted that it is not necessary to begin with a thermal population, and the distributions are readily disturbed by e.m. radiation. Indeed, if the populations are reversed it is possible to have a phonon maser, as was reported by Tucker.[12] He used a ruby sample, but this is probably not the best material; others are being examined. Developments in this direction could transform the position with regard to generation and detection.

5. Travelling-wave Phenomenon

Another area of interest is that in which free charge carriers move with nearly the same velocity as the acoustic wave, and exchange energy with it. The phenomenon is similar to that which takes place in a travelling-wave tube, the main difference being that whereas in a travelling-wave tube it is easy to see that the coupling is between charge and the electric field of the wave, it is less easy to see for a charge and an acoustic wave. The simplest case is that of a piezo-electric material, when an electrical wave accompanies the acoustic wave. Amplification of acoustic waves in the region of 10^8 Hz has been quite successful, but as the frequency increases so do the difficulties.[13]

Extending these ideas it seems probable that any sort of disturbance which travels with a velocity near that of an acoustic wave may exchange energy with it, and lead to an amplifier. For this reason there is a good deal of interest in the coupling of magnetostatic and spin wave disturbances in magnetic materials with acoustic waves.[14] It is important that the spin-wave velocities can be adjusted by means of an applied magnetic field.

Adjustment of velocity by a magnetic field is also exploited in experiments on frequency multiplication. If an intense acoustic wave passes through an ionic crystal, non-linearities will produce higher harmonics. For the process to be efficient it is necessary to have the phase velocities of the various harmonics the same. Dispersion in the sound velocity prevents this. However, if the crystal is doped with a suitable paramagnetic impurity some adjustment of the velocity of a particular frequency can be obtained by a magnetic field. Shiren[15] used this technique to demonstrate that there was conversion of power into second harmonic, by observing loss from the fundamental as a magnetic field was varied.

It may be remarked that it is not always necessary to apply a magnetic field to obtain split spin-levels, for they can exist due to zero field splittings. The dispersion thus produced will be most noticeable near resonance, but the theory suggests that there may be measurable effects well away from resonance.[16] As the dispersion depends on the population differences, the velocity of sound should then be temperature-dependent. There are, of course, other reasons for temperature variations, such as changes in force constants, and this effect does not seem to have been observed.

6. Incoherent Acoustic Waves and Thermal Conductivity Measurements

While the purpose of this paper is to give an account of some of the recent work which uses coherent high frequency acoustic waves, it does seem of value in conclusion to emphasize that the possibility of using incoherent, broad-band sources should not be overlooked. Such waves can be conveniently

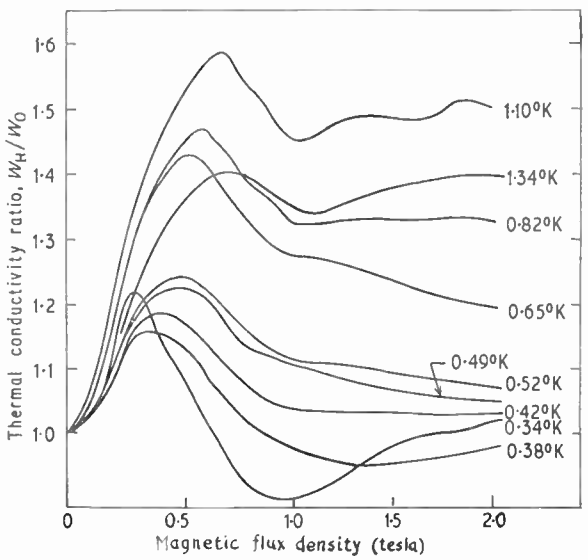

Fig. 3. Variation of thermal conductivity with magnetic field at different temperatures.

launched, and detected, by thermal techniques. A standard Searle's bar thermal conductivity experiment is carried out at low temperatures, using instead a non-metallic specimen. The hot end launches, into the bar, a black body spectrum of acoustic waves. As the waves travel down the bar they may be absorbed, scattered, etc. At helium temperatures the absorption is usually very weak, and the main scattering, which includes mode conversion, occurs on the sides of the bar. If the crystal contains a suitable paramagnetic scatterer, the thermal conductivity can be changed very considerably by the application of a magnetic field, which tunes the energy levels of the impurity into resonance with the lattice modes which are carrying the bulk of the heat (Fig. 3). This peak is usually at a higher quantum than can readily be generated coherently; it is of considerable value to have thermal conduction measurements made on all our specimens. It is also possible to use heat pulses[18] in which case the technique becomes very similar to our monochromatic experiment.

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Manuscript first received by the Institution on 5th December 1967 and in final form on 29th August 1968. (Paper No. 1225.)

(See opposite page for the Discussion)

DISCUSSION

Under the chairmanship of Mr. A. E. Crawford

Mr. A. E. Crawford: Does the wave-front occupy the whole of the cross-section area of the quartz rod or are these areas of inactivity? Since there is a possibility of variable axis excitation with the propagation of transverse waves, is the measured acoustic velocity the same at lower frequencies?

Professor K. W. H. Stevens (*in reply*): I don't think we really know the answer to the first question. We suspect that the amplitude of the wave does vary over the cross-section of the rod. In one set of experiments the far-end of the rod was roughened in patches, so that good reflections were only to be expected from small areas. This didn't seem to make much difference to the echoes, though it is not possible to give a quantitative assessment as the experiment had to be dismounted between the two runs, without and with roughening. It would be interesting to know something about the effects of masking the launching end.

In reply to the second question, most of our results have been obtained with longitudinal waves, for these are most easily generated. As far as I know there is very little dependence of velocity on frequency for any type of wave as one goes to lower frequencies.

Dr. K. W. H. Foulds: What was the microwave power level used in the cavity excitation experiments?

Have you ever adjusted the pulse repetition frequency of the microwave oscillator to correspond to the transit-time of the acoustic signals in the rod, and if so, does this have any interesting results?

Professor Stevens (*in reply*): The power into the microwave cavity was of the order of 200 mW. The acoustic power is difficult to measure, but it is probably of the order of 10^{-3} to 10^{-4} lower.

Our pulse repetition rate is 1000 pulses/second, so the adjustment you suggest would be a considerable one, and we have not made it. We have though considered the complications which can arise due to the multiple echoes coming from a single pulse. Ions in one part of the rod may be still disturbed by a previous echo when a second echo arrives. Alternatively, near an end the same spins may be simultaneously subjected to the end of a pulse and its front, which is returning following reflection.

Mr. P. G. Heath: Has Professor Stevens any actual figures for attenuation (at 10 GHz) in CdS or MgO? As he is working at 4·2°K, does he know what the attenuation would be at liquid H_2 and liquid air temperatures? We have an application where 150 dB of attenuation is tolerable.

Secondly, an entirely different point. When the lattice is pumped, the electron goes 'round-the-loop', giving a burst of energy, and then pauses, before going round again. Is there any significance or mathematical reason for the length of the pause? Why should the electron pause at all?

Professor Stevens (*in reply*): I do not know where the attenuation figures you need can be found. A certain amount of information is given by de Klerk (Reference 1 of the paper).

On your second point, I think you are referring to the high intensity pulse. When the ion goes from one state to another and back again, its total energy change is zero. If it does not quite get round during the pulse, and if it starts in the low-energy state, it continues to radiate, thus effectively lengthening the pulse. On the other hand, if it more than gets round, near the end of the pulse it is effectively shortening the pulse. Thus the pulse in either case tends towards having a fixed duration. The mean energy transported by the acoustic wave does not change when it breaks up into short bursts. Each such short burst contains a definite amount of energy, so there must be 'breathing spaces'.

A New Award for Engineers

On 7th November an announcement was made by the Council of Engineering Institutions and the MacRobert Trusts of their joint intention to establish a new award for engineers to be known as the MacRobert Award. This will have an impressive monetary value and will be made each year for notable achievement in engineering.

The MacRobert Trusts were formed by Lady MacRobert of Douneside and Cromar and give donations to a large range of charities. (Lady MacRobert was the wife of Sir Alexander MacRobert, Bt., founder of the British India Corporation.) The Trusts have made many significant contributions to new ventures, particularly in Scotland. In recent years donations have been given for welfare of the Services, particularly for ex-servicemen, agricultural research, education, medical research and youth enterprises. Three recent examples which may be of interest are the MacRobert Hall at the new University of Stirling, the restoration of Old Aberdeen within the precincts of Aberdeen University, and the Erskine Centre for the disabled.

The Trustees of the MacRobert Trusts have wished for some time for some of the funds they administer to be used in a manner which would enhance the economic well-being of the United Kingdom. They also considered that a major award in the fields of engineering and the technologies would provide a balance, at least in the United Kingdom, to the already renowned Nobel Prizes for Chemistry, Literature, Medicine, Peace and Physics.

The outcome is thus the MacRobert Award. This will consist of an annual presentation of £25 000 and a gold medal to an individual or a small team of up to five people who made an outstanding contribution, by way of innovation, in the fields of engineering or other physical technologies or in the application of physical sciences, which has enhanced or will enhance the national prestige and prosperity of Great Britain.

The Council of Engineering Institutions will administer the MacRobert Award Scheme and are now ready to receive applications for the first award scheduled to be made in 1969. Lord Hinton of Bankside is to be Chairman of the Selection Committee which will include nominees of the Royal Society (Sir Charles Goodeve, Professor M. J. Lighthill and Professor T. M. Sugden), the MacRobert Trusts (Mr. D. M. Heughan), and member Institutions of the Council of Engineering Institutions (Sir Leonard Drucquer, Mr. E. Le Q. Herbert, Mr. G. S. C. Lucas, Professor Sir Alfred Pugsley and Mr. R. Ratcliffe). The last four C.E.I. representatives will also be Assessors and Chairmen of Group Committees which will be formed to effect preliminary selection; the four further members of each of these four Committees have not yet been named.

The establishment of the MacRobert Award will certainly arouse considerable interest as indeed will the announcement at the end of next year of the first recipient.

Conditions of *The MacRobert Award*

1. The Award will consist of a gold medal and a prize of £25 000.

2. The Award will be made annually by the Council of Engineering Institutions, on behalf of the MacRobert Trustees, to any individual, or independent team or to a team working for a firm, organization or laboratory where in the opinion of the Council, an outstanding contribution has been made by way of innovation in the fields of engineering or the other physical technologies or in the application of the physical sciences, which has enhanced or will enhance the national prestige and prosperity of the United Kingdom of Great Britain and Northern Ireland.

3. The prize winners shall be selected by the Council of Engineering Institutions in conjunction with the MacRobert Trusts. In making their selection they shall be advised by a committee consisting of a Chairman and nine members. The Chairman and six of the members will be nominated by the Council of Engineering Institutions and the remaining three members by the Royal Society.

4. If the Council decides in any year that two of the innovations considered for the Award are of equally outstanding merit the Award for that year may be divided but it shall not be split into more than two parts which shall be of equal value. The Award will be withheld if in any year the Council so decides.

5. When the Award is given to a team working for a firm, organization or laboratory the medal shall be awarded to the firm, organization or laboratory and the money prize shall be divided between not more than five employees nominated by the organization as having played a leading part in the team responsible for the innovation. Each of these individuals shall be given a replica of the medal and the division of the prize money shall be determined by the Council in consultation with the organization. Where the Award is given to an independent team, the decision of the Council of Engineering Institutions as to the membership of that team and as to the sharing of prize money shall be conclusive. Each member of the team shall have a replica of the medal.

6. Applications for the Award may be made to the Council of Engineering Institutions by firms, organizations, laboratories or individuals, but the Council reserves the right to consider innovations in connection with which no application has been made.

7. Applications should be submitted to the Council in the period January to April inclusive each year and must give the following information:

(a) Particulars of individual or independent team giving full name, age and address.
(b) In the case of applications by a team working for a firm, organization or laboratory, list of the individuals to be considered as a party to the application giving full name, age, status in the firm or laboratory, and address.
(c) An appropriate description of not less than 200 words nor more than 500 words of the achievement in relation to the purpose of the Award, supported by any published or other relevant evidence.
(d) The names of at least two referees from whom further supporting statements could be sought.

Entries should be addressed to:

MacRobert Award Office,
Council of Engineering Institutions,
2 Little Smith Street, London, S.W.1.

8. The presentation of awards will take place at the end of each year.

U.D.C. 621.319.42

Capacitors Compatible with Thick Film Circuit Technology

By

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A.R.I.C.†

Reprinted from the Proceedings of the Joint I.E.R.E.–I.E.E.–I.S.H.M. Conference on 'Thick Film Technology', held at Imperial College, London, on 8th to 9th April 1968.

Summary: The paper describes three approaches to the problem of manufacture of capacitors by methods compatible with thick film technology. In the first, the capacitor is regarded entirely as a discrete component and is manufactured or purchased independently. The problems of integration become those of surface bonding and of the protection of devices with irregular outlines.

The second approach is to produce the resistor network on a high permittivity ceramic substrate, and manufacture capacitors *in situ* by the printing of appropriate electrode regions. This technique has the advantage of simple processing and produces co-planar components, but it necessitates a compromise on thermal and mechanical properties of the substrate material.

The third and probably the best approach is to produce the capacitor by printing and firing of a suitable dielectric glaze. This introduces no compromise on substrate, no design allowances for strays, the component is co-planar and is produced by identical processes to the resistors. Multi-layer techniques offer the prospect of significantly wider range of values, and adjustable capacitors may eventually permit close tolerances to be achieved. This approach involves complexity of the process sequence for active R-C networks, possibly with multi-layer capacitors.

1. Introduction

In the last few years there has been an increase in interest in the screen-and-fire process as a means of economically producing the passive components in hybrid microcircuits. A number of cermet resistor systems has emerged, notably those based on palladium oxide and silver,[1] on ruthenium or its dioxide,[2] on thallous oxide[3] and on indium oxide.[4] The technology associated with the manufacturing processes and the properties of the components produced have been well characterized and documented in many of these cases.

By comparison, relatively little work has been reported on associated materials for capacitor dielectrics, and as a consequence the integration of capacitors into hybrid microcircuits has proceeded along three entirely separate routes. In this paper an attempt is made to review these alternatives and to present the merits and shortcomings of each.

2. Requirements

In the author's company the bulk of the customer requirements for hybrid microcircuits calls for general purpose capacitors within the range 10–50 000 pF, to a tolerance of $\pm 10\%$. A much smaller volume requirement is for a higher quality capacitor suitable for use in timing or delay circuits. In this latter case the need is more commonly for capacitors in the range 10–5000 pF, with a selection tolerance to $\pm 2\%$ and occasionally with a temperature coefficient of 20–30 parts per million.

Each of the three approaches to be discussed is easily capable of providing the general-purpose capacitor, but the higher quality capacitor is of more limited availability at the present time.

2.1. *Outline of the Possible Approaches*

The three possible approaches are:

(a) Discrete components.
(b) Dielectric substrates.
(c) Printed dielectric glazes.

In (a) the capacitor is regarded as a discrete component and is manufactured or purchased separately. In the tubular- or rod-type with axial leads the available choice is very wide and there is little problem in acquiring a capacitor appropriate to the circuit requirements. Integration problems are reduced to those of establishing suitable methods of attachment and of protection. Similar problems occur if the

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discrete component is of the flake or monolithic face-bonded chip type, but the choice of capacitor is rather more restricted in these cases.

In (b) the capacitor is produced by manufacturing the circuit on a high-permittivity substrate, and printing appropriate electrode regions on either surface. An extension of the technology (described later) eliminates the need to use both faces, but the process has several limitations. The range and quality of the capacitors obtained are more restricted than with the alternative approaches, although there are some compensations by virtue of simpler processing.

Method (c) involves producing capacitors in a very similar manner to that used for resistors. A small number of proprietary dielectric glazes are available, and various formulations are reported in the literature[5] for preparation of similar materials. These have not, in general however, been as well characterized as their resistive counterparts. The advantages of this process are its natural compatibility with the resistor process and its potential to produce high values by multi-layer techniques and close tolerance capacitors of high quality by careful trimming of components prepared from selected low permittivity dielectric glazes. Against this one must offset the complexity of processing required to produce such components as part of a complete circuit. Methods (b) and (c) both permit the processing of all capacitors in the circuit to proceed simultaneously.

3. Discrete Capacitors for Use in Hybrid Circuits

These can be classified into three groups:

(a) conventional tubular or rod types with wire terminals,

(b) thin dielectric ceramic wafers with metallized (usually silver) electrodes on opposite faces,

(c) single or multi-layer monolithic chips with both electrodes on the same face.

3.1. *Cylindrical Capacitors*

Those most commonly used in hybrid circuits are the miniature versions of the tubular ceramic type (50–5000 pF) polyester or polycarbonate film and foil (or metallized film) type for 5000 pF–0·5 μF and epoxy-moulded tantalum types for 0·1–100 μF.

These are attached to the circuit by soft-soldering the terminal wires on to appropriate regions on the substrate or directly on to the external terminals of the module.

3.2. *Metallized Wafer Capacitors*

The second type is available in two principal versions, in which the difference is the nature of the ceramic dielectric. The first version offers a limited range of capacitance per unit area (capacitors of greater than 1 cm^2 in area can rarely be tolerated in hybrid circuits) but offers high insulation resistance, high Q values, low frequency coefficient, low drift and high dielectric strength. Controlled temperature coefficients of capacitance (t.c.c.) make it possible to compensate for operating conditions at the design stage. Very low t.c.c. is associated with $K \sim 20$, but temperature compensating dielectrics with K up to about 500 are available. The second version offers a much wider range of value (high-permittivity ceramics) but the other parameters are frequently poorer by comparison. Materials with K of up to 10 000 are readily available.

This type of capacitor is usually secured into the circuit by soft-soldering the lower electrode on to an appropriately prepared contact island, and contact is made from the upper electrode to the circuit by means of a link wire. Although link wires are considered an undesirable feature from a process standpoint they do permit the designer to use them as a crossover should this be necessary in the circuit. Capacitors of this type are usually fragile, as maximum capacitance is obtained with materials of 0·005 to 0·010 in (0·125–0·25 mm) thick.

3.3. *Monolithic Chip Capacitors*

The third type of discrete capacitor, the monolithic chip, is a more recent arrival. This is prepared from stacked tapes formed from dielectric powders and suitable organic binders. The tapes have electrode regions printed before a sequence of stacking, punching, pressing and firing operations converts them into sintered blocks. Appropriate interconnection of electrodes permits terminations to be brought on to one face, which eliminates the need for link wires. Sintered palladium is frequently the preferred termination material. Typically 20 to 25 layers of 0·001 in (0·025 mm) thickness can be used, thus giving a very wide potential range of values. One projected range of such devices[6] includes values up to 1500 pF in an area of 0·4 cm^2 with zero t.c.c. (basic material has K of 35). With the highest permittivity material ($K \sim 8000$) capacitors of 0·2 to 0·3 μF are said to be possible in a similar area.

Capacitors of this type are expected to lend themselves to face bonding techniques similar to some of those employed for the mounting of LIDS and chip semiconductors (e.g. hot gas bonding), although material compatibility may not permit the use of others (e.g. ultrasonic bonding).

3.4. *Protection of Hybrid Circuits with Discrete Capacitors*

For the cheapest type of hybrid circuit the final protection is usually a conformal coating of organic lacquer. With attached discrete components this can

be difficult to achieve because of the irregular outline. Frequently voids or holes occur in the lacquer coating due to air which is trapped during the application of the lacquer being subsequently expelled during stoving. Care during the lacquer application is required to prevent such occurrences; the application of the coating under vacuum also greatly assists.

As the final product in the conformal coated form is often aesthetically unpleasing, customers frequently prefer a device with a regular outline. This can be achieved in two ways:

(a) by encapsulation in resin in a suitable box or case,

(b) by transfer moulding.

Encapsulation is the preferred method of protecting modules with polyester, polystyrene or polycarbonate capacitors as they are not always able to withstand the temperature of transfer moulding. Encapsulation can give rise to problems in choosing the appropriate resin, not because of the capacitors, but because the associated thick film resistors may not be compatible with all types of resin. This is certainly true of the palladium oxide-silver cermet resistors, and the resin must be chosen with regard to both chemical and mechanical compatibility with all components present. Similarly, the choice of the box material may need consideration; low power film circuits suitable for modest operating temperatures have frequently been housed in thermoplastic resin boxes, but these materials are no longer necessarily appropriate for the higher power, higher temperature thick film hybrids. Boxes made from epoxy or diallyl phthalate polymers are more satisfactory in these instances.

In transfer moulding, the device is mounted in a suitable cavity in a moulding tool, and the moulding material (a specially formulated resin which is converted from powder to mobile liquid form by the action of modest temperatures and pressures) is forced into the cavity around the device. After 1–2 minutes the material cures into a solid mass around the device, providing it with an adherent conformal coating of regular outline. With devices of irregular outline it is of great importance to design the tool with correct gating to the cavity, such that a continuous flow of material is possible and that no discrete component significantly impedes this flow. In most instances it seems desirable to provide an intermediate barrier layer over the top of discrete components such as flake or chip capacitors and chip semiconductors. This layer can provide a mechanical buffer but it must be sufficiently adherent to prevent itself being scoured off during the moulding operation. Without such a layer it is observed that the wave front of the liquid resin, which may be curing as it is being forced into the cavity at elevated temperature, can disturb or even completely remove attached components.

4. Dielectric Substrates

Two principal categories of standard dielectric ceramics are available. These are the low permittivity, higher quality, temperature compensating type and the high permittivity type. They are basically similar materials to those referred to in Section 3.2. These materials can be used as the substrates for conventional thick film resistor circuits and where capacitors are required they are usually obtained by printing electrode regions in normal thick film conductor materials and relying on the permittivity of the substrate to provide the required capacitance. Two types of electrode configuration can be used, as shown in Fig. 1.

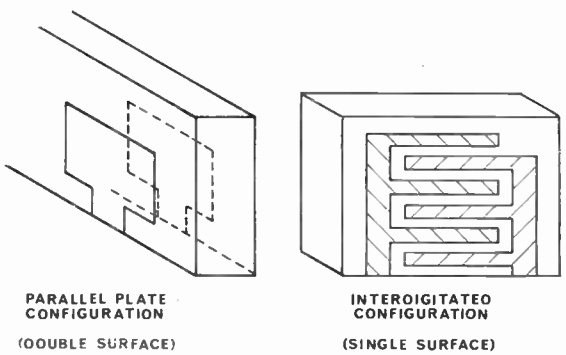


Fig. 1. Electrode configurations on dielectric substrates.

The relative merits of the parallel plate (i.e. opposite face) and interdigitated dispositions have been examined, and the following reasons can be given for preferring the interdigitated version.

(i) Printing can be restricted to one surface of the substrate only.

(ii) Terminals need to be fitted on one surface of the substrate only.

(iii) If desired, the entire reverse face of the substrate can be used for capacitors. This increases the available practicable substrate area, but the advantages in (i) and (ii) are forfeited.

(iv) The capacitor is produced in a single printing operation, therefore no registration problems are encountered.

(v) The capacitor value is virtually independent of substrate thickness, therefore the substrate dimensions can be chosen with regard to other factors, such as strength, flatness and availability.

(vi) Although theoretically a significantly higher capacitance per unit area is available by the parallel plate type, this is only true if very thin substrates are used. Substrates below 0·025 in (0·635 mm) in thickness are too weak for use in mass production and a convenient thickness compatible with other hybrid circuit processes is 0·040 in (1·0 mm). At this thickness the capacitance per unit area for the interdigitated and the parallel plate types is approximately equal.[7]

The advantages of the dielectric substrate approach are that processing the capacitor is extremely simple, and that the resulting component is co-planar with the substrate. This means that R-C networks can have a simple outline and there are no problems in coping with irregular shapes during protection. The capacitor can also be readily trimmed to value by similar techniques to those used for the resistors, i.e. removal of part of an electrode limb by air-abrasive trimming, or possibly by laser machining.

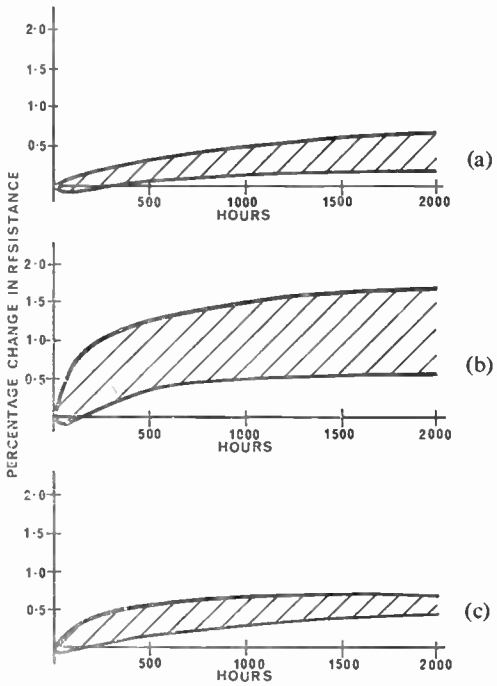
There are, however, several drawbacks to the dielectric substrate approach, and these must not be overlooked. The range of dielectric materials is still somewhat limited, and those with higher permittivity (2000–10 000) make capacitors which have high power factors and temperature coefficients. The substrates are mechanically much weaker than alumina, and the present state of art of their manufacture seems to be poorer than that for alumina, in particular with regard to dimensional tolerances and flatness. The poorer mechanical strength and surface hardness necessitate that conventional thick film resistor adjustment is carried out with a modified abrasive powder to reduce substrate damage. This affects the rate of resistor adjustment and hence slows down production output.

Two other factors merit consideration here. Firstly, in addition to poorer mechanical properties, dielectric substrates have universally poorer thermal properties than alumina. As a consequence it has been found that derating of resistors is necessary to ensure the same drift rate on load. Figure 2 illustrates the average drift over 2000 hours of similar thick film resistors on load at 70°C ambient on (a) alumina at 2 W/in² dissipation, (b) typical high-K ceramic at 2 W/in² dissipation, (c) typical high-K ceramic at 1 W/in² dissipation. The results indicate that similar drifts can only be achieved by running the resistors at about half the rating used for alumina.

Secondly, it must be recognized that in using the dielectric substrate method, other components of the circuit give rise to stray capacitance for which it is necessary to make an empirical design allowance. In general terms it has been possible to use the following approximations:

(a) Circuit on same side as capacitors: increases the capacitance by 5–10%.

(b) Circuit on opposite side to capacitors: increases the capacitance by 20–25%.



(a) 3 kΩ/sq. alumina substrate (2 W/in²);
(b) 3 kΩ/sq. high-K substrate (2 W/in²);
(c) 2 kΩ/sq. high-K substrate (1 W/in²).

Fig. 2. Load drift of thick film resistors at 70°C ambient.

It has also been found possible to modify the value of interdigitated capacitors by printing a 'reflecting' electrode on the reverse face of the substrate, but as yet no guiding rules for using this have been established. Note that this does not need to be electrically connected to the circuit in any way to achieve this effect. However, the fact that these stray effects exist indicate the problem of producing capacitors to close tolerance. It is mainly for this reason that the dielectric substrate approach is considered the least likely of the three methods to offer higher quality capacitors to the desired tolerance.

5. Printed Glaze Capacitors

The printed glaze approach is the most closely related to the technology of thick film resistors. Screen printable pastes of ferro-electric powders mixed with glassy binders are available on a commercial basis,

and these are printed and fired in a similar manner to thick film resistors. Three successive printing operations are required to form respectively the base electrode, the dielectric and the counter electrode, and in many cases it is considered advisable to increase this number to four by depositing the dielectric layer in two separate stages. This is considered to minimize the danger of failure at a point defect in the layer, on the premise that two such points are most unlikely to coincide in successive prints.

As in the case of the resistor, capacitor values are very dependent upon the thickness of the printed dielectric layer, therefore this parameter must be kept under close control. A range of glaze dielectrics with permittivities from 10 to about 500 can be achieved, which with a typical fired dielectric thickness of 0·001 in (0·025 mm) can give a range of values from about 300 to 18 000 pF/cm^2.

It has been observed that K appears to increase with firing temperature, such that a material with $K \sim 150$ when fired at 850°C might have $K \sim 500$ when fired at 1050°C. It is not yet established whether this is a true change in K (due to structural modification of the dielectric material) or simply an apparent increase as a result of electrode material migration (giving a smaller electrode spacing) at the higher temperature.

The printed glaze system can be seen to have some advantages over the discrete or dielectric substrate approaches. The resulting capacitor is effectively co-planar, but there is no need to compromise on substrate as it is readily produced on alumina. There is also no necessity to introduce allowance for stray capacitance. In addition there are two potential features which are of interest. These are the facilities to trim to close tolerance and to produce higher values by multi-layer techniques.

5.1. *Adjustment of Printed Glaze Capacitors*

There are several ways in which the glaze capacitor may be trimmed to value. This could be achieved by:

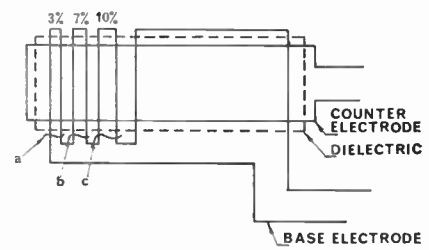
(i) Selectively eliminating part of the counter electrode by powder abrasion or by spark erosion.

(ii) Removing an entire portion of the capacitor, i.e. cutting through all three layers by either of the methods given in (i) or possibly by laser machining.

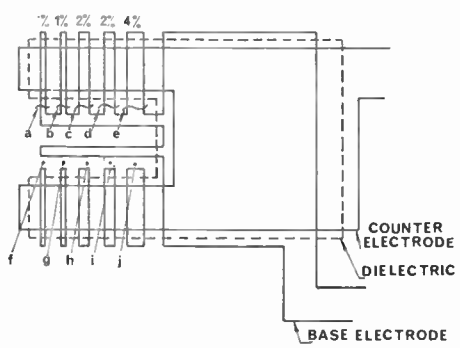
(iii) Refiring the capacitor at an appropriate temperature for a selected time (K is dependent upon firing conditions).

(iv) Printing a suitably designed capacitor array which incorporates trimming limbs. Such limbs can represent small increments of capacitance (e.g. 3%, 7% and 10%) in parallel with the main capacitor (Fig. 3(a)). With this combination, any capacitor falling within the limits of nominal value to +20% can be trimmed to within 2% of nominal by cutting the appropriate limbs at a, b or c. An alternative approach using similar principles, is shown in Fig. 3(b). This array allows any capacitor falling within the limits of ±10% from nominal value to be trimmed to within 1% of nominal. Decrease in value is achieved by cutting the appropriate limbs at a, b, c, d or e, and increase achieved by applying and stoving conductor pastes to add extra limbs at f, g, h, i or j.

A design for very low capacitors which permits adjustment to close tolerance is discussed in detail elsewhere.[8]



(a)



(b)

Fig. 3. Adjustable printed glaze capacitors. (Two approaches are shown.)

5.2. *Multi-layer Capacitors*

The printed glaze technique can obviously be used to produce multilayer capacitors by successive printing and drying operations with carefully controlled registration of patterns. There is evidence that the capacitance obtained by this process is very close to the appropriate multiple of the single layer that would ideally be expected, and with the correct materials it may be possible to use only a single firing operation.

Thickness measurement constitutes a problem, and thickness control is essential. It will be appreciated that the greater the number of layers, alternating between metallic and dielectric materials, the greater is the risk of disruption on firing and cooling unless expansions of the constituent layers and the substrate are very carefully matched. In particular trouble can arise by cracking of the electrodes over the step edge, which in a ten-layer capacitor is likely to be about 0·012–0·013 in (0·3 mm) high. If a wide range of values is being proposed, capacitors of at least ten layers would be required. It is perhaps worth noting that this would necessitate twenty-one printing operations for the manufacture of the capacitor alone.

5.3. *Processing of Printed-glaze R-C Networks*

This last point focuses attention on the practicalities of making R-C networks entirely by the new screen-and-fire process. There seems on occasion to be too little appreciation of the length and complexity of processing sequences which are involved. One can use the following circuits as illustrations.

(a) A simple resistor-capacitor circuit—single resistivity, single layer capacitor. This could probably require five printing operations as follows:

(i) base electrode and conductors
(ii) dielectric
(iii) counter electrode
(iv) resistors
(v) protective glaze coating.

It could also require three firings, e.g.

(i) base electrode
(ii) dielectric + counter electrode + resistors
(iii) protective glaze.

This example has assumed that the base electrode and conductor material is the same, and that the dielectric can be achieved in one print.

(b) A more typical example, which would make use of a wider range of the technology of thick films, would be a circuit which required three resistivities and a single layer capacitor whose '*K*' necessitated a high firing temperature. Selective soldering would be required thus leaving some conductors free for attachment of discrete components by microbonding techniques. Such a circuit could need eight printing and four firing cycles, as follows:

Printing:

(i) base electrode and conductors
(ii) dielectric
(iii) counter electrode
(iv) resistivity 1
(v) resistivity 2
(vi) resistivity 3
(vii) protective glaze
(viii) solder resist (for dipping) or solder paste

Firing:

(i) base electrode
(ii) dielectric
(iii) counter electrode and resistors
(iv) protective glaze

Neither of the examples quoted uses multi-layer capacitors and it is obvious that when the technology is extended to include these and crossover dielectrics, an extremely laborious and complex processing sequence can ensue. In addition, there are many possible interactions, particularly as a result of different firing temperatures for the various materials, which can govern the choice of manufacturing sequence. These include the ability of R and C elements to withstand re-firing without loss of solderability or adhesion to the substrate.

It is evident from the foregoing that to make such a complex process amenable to acceptable production yields, a comprehensive and detailed programme of development work must be pursued. Until the outcome of such a programme has been ascertained, a more practical approach to R-C networks by the printed glaze process would be to accept the advantages offered by a double substrate system. Capacitors would be processed on one substrate and resistors on the other, and inter-connections would be made by external terminals of appropriate shape or by simple link wires. Such an approach is somewhat restrictive to the designer, is less than satisfactory and in fact represents a retrograde step to the purist, but can probably be commended on the grounds of simplicity and economy as a practical alternative until more knowledge on process interactions has been acquired. Even then it may still represent the most economic approach to making printed glaze R-C networks.

6. Conclusions

The merits and shortcomings of the three possible approaches to thick film R-C circuits have been outlined and discussed. Where active devices other than conventional transistors and diodes are to be attached, there would seem to be a strong case for selecting the use of monolithic face-bonded capacitors as the preferred technique. These offer a wide range of component values and types and use similar bonding methods. If conventional active devices with terminals are to be used, then tubular capacitors would be the

logical choice. Where capacitor quality is of less importance, and particularly where no active devices are concerned, the dielectric substrate approach may be the most economic for passive R-C networks.

The printed glaze capacitor, however, has several advantages over the dielectric substrate, and is to be preferred for passive networks where price is not the first criterion. Future developments in this field may permit the technique to challenge the monolithic capacitor, but at the present time it can only compete over a limited value range. Over this range it is probably more economic, particularly if several capacitors are required in the same circuit, but this situation may change if the manufacturers of monolithic chips progressively reduce prices as their product lines become established.

7. References

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Manuscript first received by the Institution on 6th February 1968 and in final form on 5th March 1968. (Paper No. 1226/CC28.)

STANDARD FREQUENCY TRANSMISSIONS

(Communication from the National Physical Laboratory)

Deviations, in parts in 10^{10}, from nominal frequency for **November 1968**

November 1968	24-hour mean centred on 0300 U.T.			November 1968	24-hour mean centred on 0300 U.T.		
	GBR 16 kHz	MSF 60 kHz	Droitwich 200 kHz		GBR 16 kHz	MSF 60 kHz	Droitwich 200 kHz
1	— 300·1	— 0·1	— 0·1	16	— 300·1	— 0·1	0
2	—	0	— 0·1	17	— 300·1	— 0·1	0
3	—	0	0	18	— 300·0	0	0
4	—	— 0·1	0	19	— 300·0	— 0·1	0
5	— 300·0	— 0·1	0	20	— 300·2	— 0·1	0
6	—	0	0	21	— 300·1	0	0
7	—	— 0·1	0	22	— 300·0	— 0·1	0
8	— 300·0	— 0·1	0	23	— 300·1	0	0
9	— 300·1	— 0·1	0	24	— 300·1	— 0·1	0
10	— 300·1	0	0	25	— 299·9	0	0
11	— 300·1	— 0·2	0	26	— 300·1	— 0·1	0
12	— 300·0	0	0	27	— 300·1	— 0·1	0
13	— 300·1	— 0·1	0	28	— 300·1	— 0·1	0
14	— 300·1	— 0·1	0	29	— 300·1	0	0
15	— 300·1	— 0·1	0	30	— 300·2	0	0

Nominal frequency corresponds to a value of 9 192 631 770·0 Hz for the caesium F,m (4,0)–F,m (3,0) transition at zero field.

Statistics of the British Electronics Industry

The Electronics Economic Development Committee set up by the British National Economic Development Office has just published a new edition of 'Electronics Industry Statistics and their Sources'.* This is a continuation of similar series of statistics begun by the Ministry of Aviation and continued by the Electronics E.D.C. in their 1967 publication 'Statistics of the Electronics Industry'. This latest publication represents a considerable advance on the quality and detail of the statistical information hitherto available to the industry. The E.D.C. has received considerable assistance from the Ministry of Technology and the trade associations of the industry in gathering the statistical material. Some of the facts and conclusions, tentative and otherwise, emerging from the statistics are given below.

Production

Capital Equipment. The output of capital equipment has expanded strongly over the last three years, most notably in the field of electronic computers and related equipment where output has risen from £35M in 1965 to £94M in 1967. This reflects increasing awareness among British industry of the potential usage of computers in a wide variety of fields. The other major factor in the capital equipment sector is the demand of defence policy. Defence purchases have dropped from just under 50% of all capital equipment purchases in 1961 to 25% of all deliveries in 1967.

Consumer Goods. The total deliveries of electronics consumer goods rose between 1961 and 1964 but have since fallen by more than one-fifth. These statistics reveal the sectors' sensitivity to changes in fiscal policy, particularly to the 'squeeze' of July 1966. The most important factor in this sector is likely to be the future demand for colour television. Production of colour sets is building up rapidly but the industry has to face a problem withstanding foreign competition in the U.K. market as well as achieving success in export markets.

Active Components. This sector is characterized by a strong increase in demand for semiconductors. The figures available in this publication do not reveal the changes in the pattern of demand within the active component sector, i.e. the increasing importance of integrated circuits relative to discrete components.

Passive Components. In the long run the demand for passive components is likely to be reduced by the increasing use of integrated circuits and sub-assemblies, but at present the market is slowly expanding.

Telecommunications Equipment. Demand in the telecommunications sector is dominated by the British Post Office. The proportion of this which is electronic is currently very small—surprisingly, in view of the publicity attending the electronic exchange, this represented £0·43M against £65·5M for electromechanical public telephone exchange equipment in 1967. The Post Office does not anticipate any dramatic shift from electromechanical to electronic equipment in the next two or three years but, in the long run, the advantages of electronic telecommunications equipment are beyond question and in the medium term there will probably be a significant shift in the composition of demand.

Overseas Trade

Capital Equipment. Capital equipment accounts for about half the overseas trade of the electronics industry and is, if anything, under-recorded due to the fact that many capital equipments are exported as components of larger products, e.g. aircraft, ships, vehicles, etc. It nevertheless remains true that imports of capital equipment are rising much more rapidly than exports and even after the devaluation of sterling the volume of orders for imported computers still seems to be very high (£16·6M against £14·2M for exports).

Telecommunications Equipment. In this sector there is a large favourable balance of trade with steady but unspectacular increases from year to year. There was a deterioration in 1967 but this was probably a temporary fluctuation.

Consumer Goods. The consumer goods sector has exhibited a progressively deteriorating trade balance. The succession of selective 'squeezes' on this sector of the industry have had no beneficial effect on exports, neither indeed have they managed to stem the rise in imports. The conversion to 625 lines and colour television will increase export opportunities for British manufacturers, but the reduction of the *de facto* protection arising from the 405 lines standard may open the way to a rapid rise in imports.

Active Components. In this sector the change from an export surplus to an import surplus reflects the structural and technological change referred to above. The increased use of semiconductors, particularly integrated circuits, accounts for the rapid rise in imports relative to exports.

Passive Components. The passive components sector shows a respectable and consistent export surplus.

Employment and Productivity

The electronics industry only employs a very small proportion of the national labour force. Figures for 1966 indicate that electronics other than telecommunications accounts for 1·3% of all employees in employment or 3·4% of those in manufacturing industry. Nevertheless, numbers employed in electronics increased at an average rate of 6% per annum from June 1959.

In contrast with the rate of increase in employment, the rate of increase in production has been more than 12%. At first sight this appears to be an increase in productivity, but there are some qualifications. It is difficult to be sure that the figures for employees and production are in fact

(*continued on page 372*)

* Published by H.M. Stationery Office for N.E.D.O., Millbank, London, S.W.1. (11/68 1834).

U.D.C. 621.374:681.32

A High-speed, Asynchronous, Digital Multiplier

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Summary: The digital multiplication of two numbers of any sign by the successive addition of partial products is critically examined for the purpose of reducing the time of computation. The theory of Booth's method is reviewed and extended to show its validity for use with numbers of any radix. Multiple digit multiplication algorithms can then be derived and the quaternary algorithm for the multiplication of binary numbers two digits at a time is presented. Using this algorithm, computed results for numbers of varying size confirm that the carry propagation time, averaged over the whole multiplication, is very nearly one-half that obtained by either Booth's or Robertson's method.

A further significant decrease in computing time can be achieved by using asynchronously-operated circuits and a three-bit multiplier, using Booth's algorithm, was constructed, using R-T micrologic elements, to check stability; a maximum multiplication time of 650 ns was achieved together with wide stability margins.

A design for a multiplier using the faster quaternary algorithm is presented and it is envisaged that by using high-speed logical elements in its implementation a multiplication time of less than 1 μs should be achieved for 16-bit numbers.

1. Introduction

The design of the central processor of a digital computer has evolved in many ways due to the varying requirements of the system in which it operates, but in general, all designs are attempts to produce a central processor having elements which are compatible in timing. Although memory referencing still remains the slowest of the central processor operations, it seems probable that in the near future the logical nets within arithmetic units may be replaced by integrated arithmetic function generators since machines with parallel memories and arithmetic units have already been designed.[1]

In addition to the use of parallel logical nets an increase in computing speed can be achieved by operating logic asynchronously rather than synchronously. The penalty paid for this approach is the difficulty experienced in designing a system with sufficient stability margins. Existing parallel adders are in fact partially asynchronous in that carry propagation is itself essentially an asynchronous process; multiplication (and division) however are normally achieved by successive addition (subtraction) under synchronous microprogram control.

This paper investigates the increase in speed possible with a fully asynchronous multiplier which uses as its principle a generalized form of Booth's algorithm.

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2. The Generality of Booth's Algorithm

2.1. *The Use of Complements in Arithmetic Processes*

A register, capable of storing a number of any radix, r, has no mechanism for sign control other than by use of numbers and, as such, can be defined as a device which stores only a group of numbers. However, it can be shown that if the complement to the base r of a number is used to represent the negative of that number, the most significant digit, represented by $(r-1)$, can be interpreted as the sign digit. A positive number is then one which has a sign digit of zero.

Appendix 1 shows that if a positive fractional number, A, is defined by

$$A \simeq \sum_{k=0}^{k=-n} a_k r^k \text{ where } 0 \leqslant a_k \leqslant r-1 \text{ and } a_0 = 0$$

and a negative fractional number, B, by

$$-B = (r^m - B)$$

where

$$0 \leqslant m < \infty$$

or

$$-B = r^m - \sum_{k=0}^{k=-n} b_k r^k \text{ where } 0 \leqslant b_k \leqslant r-1 \text{ and } b_0 = 0$$

then all cases of addition (and hence subtraction) of two numbers are satisfied if the sign digit is treated arithmetically.

Appendix 2 indicates the problems associated with the multiplication of sign digits and shows that correct answers are given provided the following correction

is made. If the sign digit of the multiplier is $(r-1)$ subtract the multiplicand once from the final partial product, if the sign digit is zero do not subtract the multiplicand, i.e. the final partial product is the true product.

This correction forms the basis for Robertson's multiplication algorithm.[2]

2.2. *Speeding-up the Basic Multiplication Process—Use of Half-range Multiplication Tables*

Multiplication comprises repetitive addition and shifting. The number of shifts to be performed is fixed but if the amount of repetitive addition can be halved then a corresponding reduction in multiplication time will be achieved. The principle of the use of half-range multiplication tables is basically that of rearranging the multiplier so that the maximum value of the multiplier never exceeds $r/2$, for r even, $(r+1)/2$ for r odd. Appendix 3 gives the derivation of the modified multiplier and Table 1 below shows the necessary rearrangement for any radix r.

Table 1

For r even

Multiplier digits b_{-k}	$b_{-(k+1)}$	Modified multiplier digit b'_{-k}
$< r/2$	$< r/2$	b_{-k}
$< r/2$	$\geqslant r/2$	$b_{-k}+1$
$\geqslant r/2$	$< r/2$	$-(r-b_{-k})$
$\geqslant r/2$	$\geqslant r/2$	$-\{r-(b_{-k}+1)\}$

One possible computational algorithm would be to re-write the multiplier in this form as an initial step, and then proceed normally. A second and better algorithm can be derived by logically deducing the modified arithmetic operations without forming the modified multiplier digits.

Table 1 indicates, however, that the two least significant digits require inspection and to enable the first multiplier to be derived the zero to the right of the least significant bit (l.s.b.) must be considered. The correct multiplier is then derived and used as the algorithm of Table 2.

It remains to be proved that it is acceptable to apply this algorithm to the sign digit as well.

Let the multiplier be defined by

$$B = b_0 b_{-1} b_{-2} \ldots b_{-n}$$

where

$b_0 = 0$ for a positive number

$b_0 = (r-1)$ for a negative number

Table 2

For r even

Multiplier digit b_{-k}	Less significant bit $b_{-(k+1)}$	Algorithm
$< r/2$	$< r/2$	add multiplicand to partial product (p.p.) b_{-k} times; shift right one place
$< r/2$	$\geqslant r/2$	add multiplicand to p.p. $(b_{-k}+1)$ times; shift right one place
$\geqslant r/2$	$< r/2$	form complement of $b_{-k} \simeq (r-b_{-k})$ and subtract the multiplicand from the p.p. this number of times; shift right one place
$\geqslant r/2$	$\geqslant r/2$	form complement of $(b_{-k}+1) \simeq r-(b_{-k}+1)$ and subtract the multiplicand from the p.p. this number of times; shift right one place

If b_0 is being investigated as the final multiplier digit applying the algorithm of Table 2 gives Table 3.

Table 3

	b_0	b_1	b'_0	Interpretation
(i)	0	$< r/2$	0	multiplication correct
(ii)	0	$\geqslant r/2$	1	add multiplicand once
(iii)	$(r-1)$	$< r/2$	$(r-1)$	subtract multiplicand once
(iv)	$(r-1)$	$\geqslant r/2$	0	multiplication correct

Entry (iv) is correct since the subtract multiplicand correction from the final partial product, demanded by the rules of complement arithmetic, is nullified by the 'add multiplicand' due to $b_1 \geqslant r/2$. Thus (i), (iii) and (iv) agree with the rules of complement arithmetic and (ii) must be considered as an additional rule to be employed when operating half-scale multiplication.

If the radix 2 be considered as an example, the algorithm which naturally develops is given in Table 4, and the correction for the sign is as given in Table 3, i.e. the algorithm is uniform and includes the sign bit.

It should be noted that this is the algorithm first proposed by Booth[3] to deal with binary complement multiplication whilst avoiding special corrections due to sign. It is however only single digit multiplication radix 2 and, since its generality has been proved, an extension of the algorithm to two-bit and three-bit multiplication is possible since any quaternary and octal number can be expressed in binary form.

Table 4

b_{-k}	$b_{-(k+1)}$	Correction	Algorithm
0	0	none	shift p.p. right 1 bit
0	1	add multiplicand once	add multiplicand; shift p.p. right 1 bit
1	0	subtract multiplicand once	subtract multiplicand; shift p.p. right 1 bit
1	1	none	shift p.p. right 1 bit

2.3. *The Quaternary Algorithm*

It has been shown that for a binary system the sign digit may be included as part of the number when applying the multiplication algorithm. Thus the binary point placed immediately to the right of the most significant bit has no meaning and integer arithmetic may be used. This being so the algorithm for two-bit-at-a-time multiplication can be derived directly.

The binary multiplier given by

$$B = b_0 b_{-1} b_{-2} \ldots b_{-n} \text{ (with } b_0 \text{ the sign digit)}$$

can be expressed as a quaternary number by grouping digits in pairs and re-writing each pair as a quaternary group so that

$$B = c_0 c_{-2} \ldots c_{-n}$$

where

$$C_{-2k} = (b_{-2k}2^1 + b_{-(2k+1)}2^0).$$

Note that this process must be operated from l.s.b. towards m.s.b. the leading binary digit being duplicated if necessary.

The algorithm for C_{-2k} and $C_{-2(k+1)}$ of the quaternary group, together with its binary equivalent is given in Table 5.

The binary interpretation of this algorithm can be expressed in more than one way depending on the logical operations that are available in the multiplier. In Table 5, for instance, the restriction of equal shifts of the partial product after each addition has been applied with the consequence that the facility to add or subtract twice the multiplicand has to be included. An alternative to this would be to perform the latter add/subtract operation by means of a two-part shift and add process. In general, the algorithm must include either the ability to add/subtract the multiplicand up to $r/2$ times to the partial product, or if the restriction of a single add/subtract operation is

Table 5

Quaternary			Binary equivalent				
Multiplier digits		Algorithm	Multiplier digits				Algorithm
C_{-2k}	$C_{-2(k+1)}$		b_{-k}	$b_{-(k+1)}$	$b_{-(k+2)}$	$b_{-(k+3)}$	
< 2	< 2	add multiplicand to p.p. C_{-2k} times; shift one place right.	0	0	0	0	shift p.p. two places right.
			0	0	0	1	
			0	1	0	0	add multiplicand to p.p. once
			0	1	0	1	shift p.p. two places right.
< 2	$\geqslant 2$	add multiplicand to p.p. $(C_{-2k}+1)$ times; shift one place right.	0	0	1	0	add multiplicand once; shift two
			0	0	1	1	places right.
			0	1	1	0	add multiplicand twice; shift two
			0	1	1	1	places right.
$\geqslant 2$	< 2	form complement $(4-C_{-2k})$ subtract this number of times; shift one place right	1	0	0	0	subtract multiplicand twice; shift
			1	0	0	1	two places right.
			1	1	0	0	subtract multiplicand once; shift
			1	1	0	1	two places right.
$\geqslant 2$	$\geqslant 2$	form complement $4-(C_{-2k}+1)$; subtract from p.p. this number of times; shift one place right.	1	0	1	0	subtract multiplicand once; shift
			1	0	1	1	two places right.
			1	1	1	0	shift two places right.
			1	1	1	1	

applied more than one shift and add/subtract cycle is required per group of multiplier digits. The logic controlling the shifts becomes more complex as the radix is increased as will also the form of adder required and the difficulties of applying Booth's algorithm in the form of multiple digit multiplication to numbers of large radix become increasingly severe.

3. The Practical Asynchronous Multiplier

3.1. *Hardware Requirements*

The introduction of multiple adders and variable shift control will increase the cost and complexity of a multiplier and the higher capital outlay may not be matched by a corresponding faster multiplication time because of the longer logic paths. For this reason a single adder multiplier was preferred for the preliminary investigation.

Every step in the multiplication may be considered to take the form of an addition/subtraction with the partial product obtained from one operation being fed back on to itself shifted by the appropriate amount. An asynchronous adder and shift register thus form the nucleus of the multiplier. An analogy of the overall asynchronous operation is a multi-start spiral having one start per bit with the arithmetic operation determined by the multiplier being carried out every time the spiral has completed one revolution; the total number of revolutions is determined by the algorithm chosen.

3.2. *The Asynchronous Adder*

Gilchrist, Pomerene and Wong[4] have demonstrated that an adder with double rail carry can be used to generate a 'finish' signal when the carry propagation, resulting from an addition, has been completed. Synchronization problems within the computer control unit often prevent the increase in speed possible with this adder from being realized, but in a multiplier where a number of additions must be performed before returning to the computer control it is possible to make better use of the asynchronous properties of the double rail adder. The finish signal from one addition can initiate the start of the next, thereby allowing the time saved at each step to accumulate over the whole multiplication process.

Table 6 shows the truth table for a single adder stage where a_{-k} is the augend, b_{-k} is the addend, $c_{-(k+1)}$ is the carry into the stage, c_{-k} is the carry out of the stage and s_{-k} is the sum.

For cases *a*, *b*, *c* and *d*, c_{-k} is independent of $c_{-(k+1)}$ and the carry from that stage need not wait for the carry into it to arrive before propagating to the next stage. For cases *e*, *f*, *g* and *h*, $c_{-(k+1)}$ determines c_{-k} and the adder stage must wait for the carry to propagate from the previous stage. The information to be transmitted to the next stage for *a* and *b* is c_{-k} = '0', for *c* and *d* is c_{-k} = '1' and for *e*, *f*, *g* and *h* whilst the adder is waiting for $c_{-(k+1)}$ to arrive it is 'c_{-k} not yet determined'; let this last state be called 'indeterminate'.

Table 6

Truth table of single adder stage

	a_{-k}	b_{-k}	$c_{-(k+1)}$	c_{-k}	s_{-k}
a	0	0	0	0	0
b	0	0	1	0	1
c	1	1	0	1	0
d	1	1	1	1	1
e	0	1	0	0	1
f	0	1	1	1	0
g	1	0	0	0	1
h	1	0	1	1	0

There are thus three possible states for the carry from one adder stage to the next and if these are transmitted as binary information two rails X and Y

Table 7

Double rail carry state assignment

X_k	Y_k	
0	0	C_{-k} = indeterminate
0	1	$C_{-k} = 0$
1	0	$C_{-k} = 1$
1	1	not allowed

are required. A possible state assignment is then that of Table 7. The Boolean equation for the finish signal is given by

$$\text{finish} = \prod_{k=1}^{k=n} (X_k + Y_k)$$

The finish signal can be used to inhibit the whole logic until a new half sum is transferred from HA1 to the mid-adder buffer register.

4. Possible Asynchronous Systems

4.1. *Single-bit-at-a-time Multiplication plus Sign Correction*

This is the most straightforward of methods and is included to allow the principles of asynchronous operation to be simply explained.

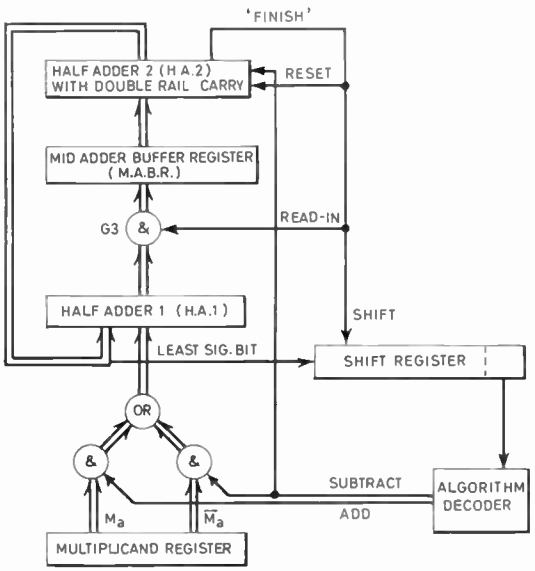

Fig. 1. Basic multiplier system.

Figure 1 shows the block diagram of an asynchronous multiplier. Consider the system set to zero with the multiplier in the shift register and the multiplicand in the multiplicand register. If the least significant bit in the shift register is a '1' the multiplicand is fed into the parallel half-adder HA1. If the least significant bit is '0' then the inputs to HA1 from the multiplicand are all '0' i.e. add zero. Gate G3 is opened, and the parallel partial addition of HA1 is fed into the buffer register. Half-adder 2 (HA2) computes the result and on completion generates a finish signal. Concurrently the shift register has been shifted one bit to the right for the control to examine the next multiplier bit, and as the partial product comes through from HA2, HA1 prepares the data for the next sequence; feedback from HA2 to HA1 is connected so as to produce a right-hand shift of one bit.

The finish signal (a) opens gate G3 and reads the new data from HA1 into the buffer register, (b) shifts the shift register one bit to the right and in doing so puts the least significant bit of the partial product into the most significant end of the shift register, (c) moves the counter on by one and (d) resets the carry logic. The latter operation would remove the partial product from HA1 but for the propagation delay of the elements comprising HA1 and HA2.

The resetting of HA2 removes the finish signal and the cycle repeats until the counter reaches its first preset limit. At this point the counter changes the control logic so that the remaining multiplier digit, which is the most significant bit, is subjected to the appropriate algorithm. If the bit is '0' then zero is added to the partial product and if the bit is '1' the 2's complement of the multiplicand is added to the partial product. To obtain the 2's complement the 1's complement is fed into HA1 and when the HA1 data is fed into the buffer register an extra carry is put into the least significant stage of HA2. At this point the counter stops the system and the result is available with its most significant portion as the outputs of HA2 and its least significant portion in the shift register.

4.2. *Single-bit-at-a-time Multiplication using Booth's Algorithm*

Only slight modifications to the control of the system of Fig. 1 are necessary to convert it to use Booth's algorithm, namely,

(i) the shift register must be increased in length by one bit,

(ii) since the algorithm holds for all multiplier digits, no change of rules during the multiplication are necessary,

(iii) the multiplicand function to be added into HA1 is now determined by the two least significant digits in the shift register.

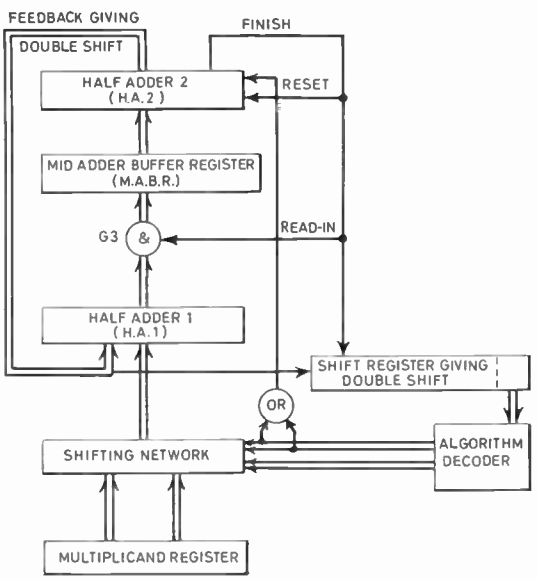

Fig. 2. Multiplier using quaternary algorithm.

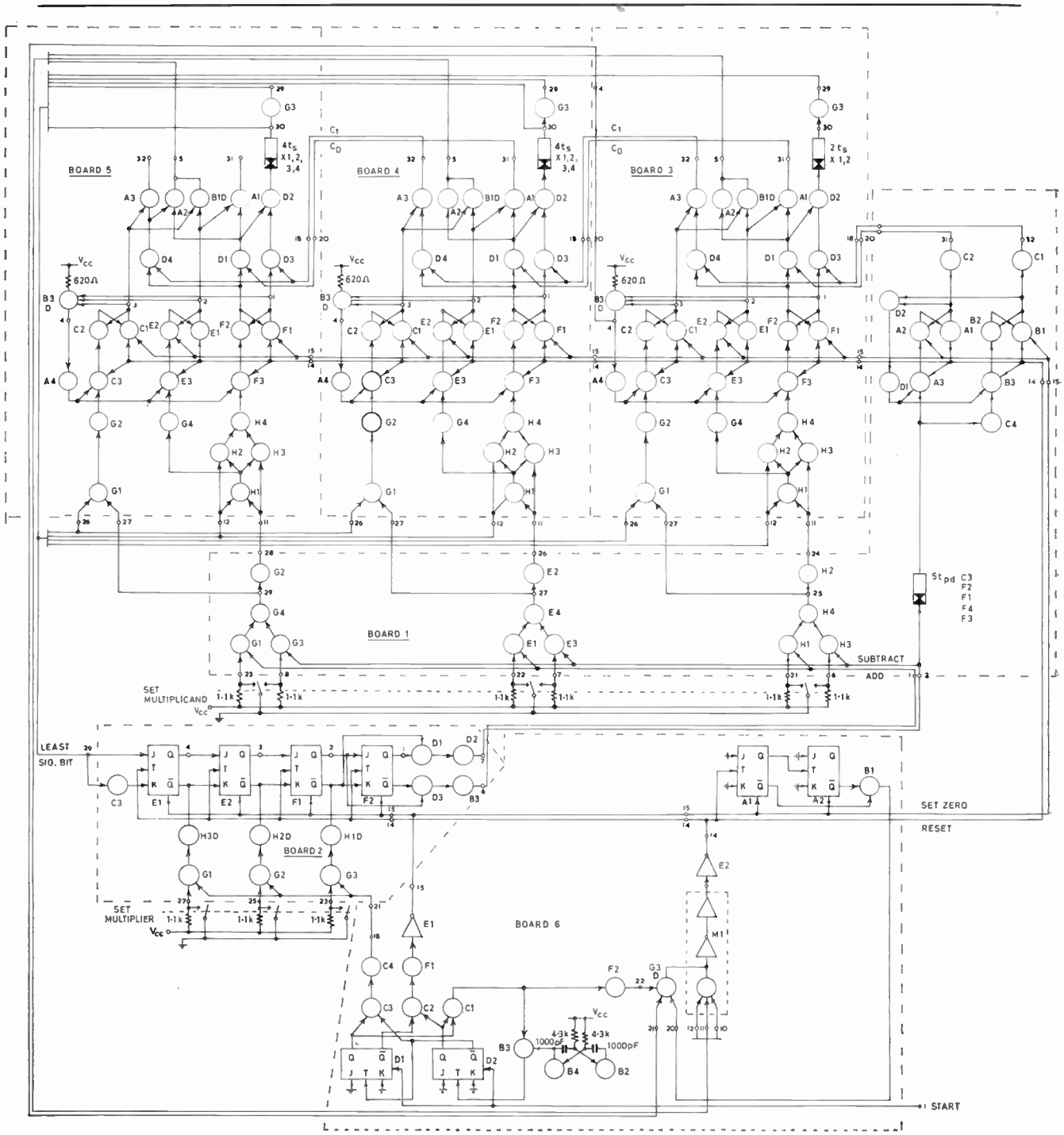

Fig. 3. Experimental asynchronous multiplier.

4.3. *Two-bit-at-a-time Multiplication using the Quaternary Algorithm*

The system of Fig. 1 is modified further to allow the use of the quaternary algorithm.

(i) The feedback is connected to produce a shift of two places instead of one as with the two previous methods.

(ii) An extra stage is added to HA1, HA2 and the buffer register.

(iii) The control must now examine the three least significant bits of the shift register.

(iv) The functions of the multiplicand to be furnished are the multiplicand itself, its 1's complements, twice the multiplicand and twice

the multiplicand 1's complement: these are provided by the gating system between HA1 and HA2.

The modified system is shown in Fig. 2.

5. Practical Results

To verify that the basic multiplier system was viable, a three-bit machine using Booth's algorithm was constructed with R-T micrologic elements, the logic of which is shown in Fig. 3. The limiting factor in speed is the rate at which the 'mid-adder buffer register' can be controlled. R-T micrologic buffer elements, used to give a high fan-out are, unfortunately, relatively slow and are not really suited to the application, nevertheless the maximum multiplication time was 650 ns. Given suitable high-speed logic elements and using the quaternary algorithm it is anticipated that it should be possible to achieve an average multiplication time of less than 1 μs for a 16-bit machine.

A measure of the efficiency of the algorithm used for multiplication is the value of the average total carry propagation delay. Computer programs were written to simulate asynchronous multipliers using the three algorithms derived in Section 4. For the cases of machines with sizes up to eight bits the average total carry propagation delay was determined by considering all possible combinations of multiplicand and multiplier. For longer word lengths a sample of 5000 randomly generated multiplicands and multipliers was used. Figure 4 is a graph of P_t against word size where P_t is defined as

$$P_t \simeq \text{average} \frac{\sum_{\text{no. of additions}} \text{longest carry sequence/addition}}{\text{word size (bits)}}$$

and shows quite clearly that the quaternary algorithm is very nearly twice as fast as either Booth's or Robertson's algorithms.

6. Conclusions

The design of high-speed combinational digital circuits is limited by the finite propagation delay which occurs in practical elements. This delay creates 'memory' in the system and the circuit under investigation must be considered not as combinational but as sequential in operation. Although these sequential characteristics may be effectively masked, and stability ensured by operating the system synchronously, this reduces the maximum operating speed. This paper has not attempted to set out the theory of such asynchronous design as much work remains to be done in relating existing sequential switching theory to complex circuits having multiple inputs and outputs, together with feedback. It has however, shown that by looking closely at algorithms and techniques used in current digital systems considerable speed advantages, without sacrifice of stability or complexity, are possible and that considerable potential exists for further development.

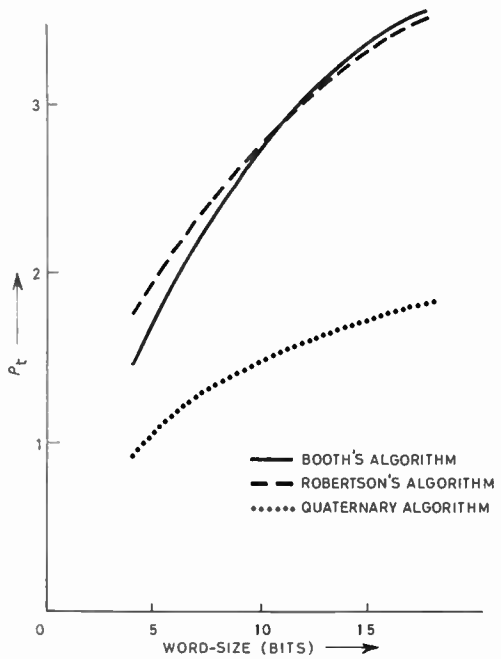

Fig. 4. Variation of P_t against word size.

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8. Acknowledgment

The authors wish to acknowledge that the above work was carried out in the Department of Electronic and Electrical Engineering, of the University of Birmingham.

9. Appendix 1

9.1. *Definitions*

(i) A number, A of radix, r is defined such that

$$A \simeq \sum_{k=0}^{k=-n} a_k r^k$$

where

$$a_0 = 0 \qquad 0 \leqslant A < 1 \qquad 0 \leqslant a_k \leqslant (r-1)$$

(ii) The radix complement, $\bar{A}_r$, of a number A is given by

$$\bar{A}_r = (r^m - A) \quad \text{where } 1 \leqslant m < \infty$$

or

$$\bar{A}_r = r^m - \sum_{k=0}^{k=-n} a_k r^k$$

For a register of fixed length a lower bound of unity can be placed on m giving

$$\bar{A}_r = (r - A)$$

when

$$\bar{A}_r + A = r$$

which for the number system defined gives zero in all digit positions together with a carry out of the most significant digit (m.s.d.).

Hence, if all additions in the m.s.d. position are made modulo r, then

(i) the complement of a number can be used to represent the negative form of the number,

(ii) the m.s.d. can be used to represent the sign of the number, 0 for a positive number, $(r-1)$ for a negative number.

9.2. *Addition of Numbers in Complement Form*

Consider the addition of the numbers A and B defined as in Sect. 9.1. Depending on the sign and magnitude of the addend and augend three different cases of addition arise.

(i) $(+A)+(+B)$

Let

$$A \simeq \sum_{k=0}^{k=-n} a_k r^k \qquad B \simeq \sum_{k=0}^{k=-n} b_k r^k$$

Then,

$$A+B = \sum_{k=0}^{k=-n} a_k r^k + \sum_{k=0}^{k=-n} b_k r^k$$

$$= \sum_{k=0}^{k=-n} (a_k + b_k) r^k$$

which is correct provided $(A+B) < 1$.

(ii) $(+A)+(-B)$

Let

$$A \simeq \sum_{k=0}^{k=-n} a_k r^k \qquad -B \simeq r - \sum_{k=0}^{k=-n} b_k r^k$$

$$\simeq (r-B)$$

Then,

$$(+A)+(-B) = A+(r-B)$$

$$= r+(A-B)$$

If $|A| > |B|$, $r+(A-B) > r$ and the sign digit is zero.

If $|B| > |A|$, $r-(B-A) < r$ and the sign digit is $(r-1)$.

(iii) $(-A)+(-B)$

Let $\quad -A \simeq r-A \qquad -B \simeq r-B$

Then, $\quad (-A)+(-B) \simeq 2r-(A+B)$

$$\simeq r+r-(A+B)$$

Now since addition is modulo r

$$(-A)+(-B) = r-(A+B)$$

which is the true sum in complement form.

10. Appendix 2

10.1. *Multiplication of Numbers in Complement Form*

Four cases need to be considered.

(i) Multiplicand (A) and multiplier (B) both positive

Let

$$A \simeq \sum_{k=0}^{k=-n} a_k r^k \qquad B \simeq \sum_{m=0}^{m=-n} b_m r^m$$

Then,

$$(+A)\times(+B) = \sum_{m=0}^{m=-n} b_m \times \sum_{k=0}^{k=-n} a_k r^{k+m}$$

$$= A \times B$$

(ii) $(-A)\times(+B)$

Let

$$-A \simeq (r-A) \qquad B \simeq \sum_{m=0}^{m=-n} b_m r^m$$

The first partial product, P_1, is given by

$$P_1 = -A \times b_{-n}$$

$$= (r-A) b_{-n}$$

$$= (b_{-n}-1) r + r - b_{-n} A$$

From Sect. 9.2 it can be seen that

$$(b_{-n}-1) r = 0$$

Thus,

$$P_1 = r - b_{-n} A$$

Shifting the partial product one place to the right must still maintain the result in complement form, so that,

$$P_1 r^{-1} = r - b_{-n} A r^{-1}$$

The final product P_n is then given by

$$P_n = r - A \sum_{m=0}^{m=-n} b_m r^m$$

$$= r - AB$$

(iii) $(+A)\times(-B)$

Let

$$A \simeq \sum_{k=0}^{k=-n} a_k r^k$$

$$-B \simeq (r-B)$$

$$(r-B) = (r-1)+(1-B)$$

and the right-hand side is now a representation of the number in sign-plus-fractional-part form.

The $(n-1)$th partial product, shifted one place right, will give by the result of the preceding paragraph,

$$P_{n-1}r^{-1} = A(1-B)$$
$$= A-AB.$$

Adding r to both sides gives,

$$(P_{n-1}r^{-1}+r) = P_{n-1}r^{-1} = A+(r-AB)$$

so that to obtain the correct product, $(r-AB)$, it is not necessary to multiply by the sign digit of the multiplier but merely to subtract the multiplicand once.

(iv) $(-A)\times(-B)$

Let

$$-A \simeq (r-A) \qquad -B \simeq (r-B)$$

Applying the reasoning of the preceding paragraph gives for the $(n-1)$th shifted partial product,

$$P_{n-1}r^{-1} = r-A(1-B)$$
$$= (r-A)+AB$$

and to obtain the correct answer it is only necessary to subtract the multiplicand once, i.e. add $|A|$.

11. Appendix 3

11.1. *Half-range Multiplication Tables*

In the decimal system it is well known that multiplication may be executed for any number provided multiplication tables from 0 to 5 are available.

For example the multiplier 6357 may be written as:

$$[1.10^4-(1.10-6)10^3]+[3.10^2]+[5.10]+$$
$$+[1.10-(1.10-7)1]$$

which can be reduced to

$$[1.10^4-4.10^3+3.10^2+(5+1)10-3.10^0]$$

and writing negative numbers in the form

$$-3.10^0 \simeq \bar{3}\ 10^0$$

gives a further simplification to

$$6357 \simeq 1\bar{4}4\bar{3}$$

Any multiplier to any radix can be reduced to this form.

Manuscript received by the Institution on 12th July 1968. (Paper No. 1227/Comp. 109.)

Letter to the Editor

Papers for the Practising Designer

SIR,

I was very glad to see a plea made, in your Editorial last July, for 'interpretive' papers, aiming to be as helpful as possible to intelligent but hard-pressed design engineers.

I have advocated this type of paper for a long time, or, at least, the inclusion of a preliminary interpretive section in a paper also containing some novel material.[1] Whilst good interpretive papers do seem to be rather rare, I do not feel that the general notion of this type of paper is really anything new.[2,3,4]

I understand, from discussion with Dr. Robinson, that the distinction intended between a 'tutorial' paper and an 'interpretive' one is that the former will be aimed primarily at students and will consequently tend to present a somewhat idealized theoretical approach, in which technological difficulties are largely ignored, whereas the latter will be aimed more at practising engineers who have become somewhat disillusioned with ideal theory but are very much concerned with technological difficulties.

Now, whilst I appreciate the above viewpoint, I feel there is, perhaps, a danger in drawing too sharp a distinction between the kind of guidance appropriate for a designer and the kind appropriate for a student. It is sometimes said that syllabuses are so full nowadays that there just isn't time to inculcate much of the creative and practical outlook that is so desirable in later life, but my own opinion is that if a good deal less time were spent teaching purely analytical aspects, and a good deal more were spent discussing the nature of the real problems that have to be solved in research, development and production engineering, we would turn out better equipped students and improve the standards of British engineering technology. It is, surely, a bad thing that there should tend so often to be a schism between practical designers on the one hand and 'university academic types' on the other, when a combination of attitudes—which fortunately sometimes occurs—can so greatly enrich both.

If the above considerations were to lead to certain analytical tools having to be dropped from the syllabus, their existence could, nevertheless, be pointed out to students, accompanied by good references, so that the student who later found he needed these techniques in his job could then study them—with, incidentally, a much more effective incentive than mere examination-passing.

It seems to be sometimes overlooked that engineering is basically concerned with *how to make things and solve practical problems*, and I think this ought to be emphasized throughout an engineering training course, as it is in some enlightened places. Of course, a really thorough grounding in basic theoretical fundamentals is absolutely essential, but too much concentration on the accompanying purely analytical aspects is liable to blind students to the fact, for example, that whilst it is virtuous to be able to analyse a circuit, it may be even more virtuous to be

able to see that a detailed analysis is unnecessary, or to invent a better circuit whose behaviour is more easily predicted.

Whilst it is probably a mistake to discourage too strongly a youthful tendency to indulge in matrices and computer programs at the slightest pretext, I am sure it is equally a mistake to believe that these are the proper modern tools for dealing with everything that comes along. Indeed, it is sometimes amusing to observe how uninventive and generally unbalanced in outlook some of the enthusiastic supporters of such techniques can become when faced with a practical problem, and how they can fail to see—as happens so often nowadays in the field of active filters, for example—what the really significant physical limitations involved are.

Over the years, like many other people, I have covered hundreds of sheets of paper with circuit calculations. Looking back, it is evident that though many of these calculations were sensible and necessary, quite a lot of them were done unnecessarily and because of an insufficient physical understanding of the problem at the time. I have also found that, in most electronic circuit design work I have done, the major part of the time has, in actual fact, been spent *not* on the specific design calculations, but (a) on the creative phase of considering the problem to be solved in its most fundamental form, the broad lines along which alternative solutions could go, and the resulting possible circuit arrangements (often no mathematics at all is involved, or just rough order-of-magnitude calculations) and (b) considering various unexpected subtleties arising during the experimental work on the prototype. These latter may involve, amongst hundreds of other possibilities, parasitic oscillations, peculiar overload effects, unwanted stray-capacitance and common-impedance couplings, failure to start in the right mode when switched on, dielectric loss effects in printed circuit boards, etc. Investigating and explaining such effects, and deciding what to do about them—they are seldom mentioned in books and articles—often occupies 90% or more of the total effort required to reach a fully satisfactory prototype, and I do not believe there is an engineer anywhere who has sufficient foresight, except occasionally, to avoid getting involved in such matters, which can, at times, be extremely perplexing and worrying and can lead to late evenings spent considering possible explanations and what to do next day to resolve the puzzles. All this involves thinking very hard and deeply about the problem and the theory involved, but sometimes quite non-mathematically. It is by solving such difficulties that the good engineer continuously educates himself and is able, in later designs, to allow in advance for some of the effects which might trouble a less experienced designer.

Thus the path along which the competent engineering designer travels in order to end up with a first-class design, whose final theory is properly understood and in which the effects of component tolerances are known, is often very different from that implied in many text books and published articles, and I feel that, as authors, we ought to be more ready to admit this in print.

Another point is that I think more discussion, in high-grade papers, of such practical matters as parasitic oscillation, earthing techniques, minimizing hum, etc., would be a good thing, and would help the less experienced design engineers to become aware of some of the things that have been found out the hard way by others. Millions of pounds must be spent annually by industry paying for the man-hours occupied in sorting out such 'mundane' matters.

While it is obviously very important to avoid going into print too hastily and saying unsound or misleading things, we should, perhaps, be more ready to submit material which, though sound and potentially helpful to others, is thought to need tidying-up and rounding-off. So often—and I confess to having transgressed badly in this respect myself—the result is that it never does get published! It seems to be a sad but true fact that much of the best material accumulated by busy practical engineers never reaches the light of publication, while the world's technical journals are swollen with hundreds of not-very-helpful contributions from people who evidently have more time for writing.

Perhaps also those of us who act as referees for papers submitted for publication should bear more fully in mind, when recommending that an otherwise excellent contribution should be shortened, or otherwise substantially modified, that the task may seem so overwhelming to the author, now trying to make up for the time he lost for other jobs while preparing the original version, that the outcome may easily be that nothing at all will actually get published.

An important thing in all papers is the choice of references, and many of us are probably guilty of taking insufficient care in the selection of these. A few very carefully-selected references will usually be of much more help to the reader than a large list of all the references the author happens to have come across. It is also very helpful sometimes to include, in brackets, after appropriate references, some brief remarks, such as 'This gives a good account of the basic principles, but the designs given are not representative of the best recent practice'; 'This is highly mathematical, but presents the conclusions in a form easy to use for design purposes.'

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Malvern, Worcestershire. *4th November 1968.*

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U.D.C. 621.3 7/9.002

A Multi-layer Thick Film Interconnection System

By

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AND

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Reprinted from the Proceedings of the Joint I.E.R.E.–I.E.E.–I.S.H.M. Conference on 'Thick Film Technology' held at Imperial College, London, on 8th to 9th April 1968.

Summary: The paper describes a multi-layer interconnection system suitable for 50–100 unencapsulated integrated circuit elements of the type used in high-speed computers. The power and earth planes with their associate dielectrics are made using the thick film technique. Methods of producing the conductor and dielectric films are discussed. Two additional conductor planes, forming the signal matrix in which the logic connections are made, are deposited by the thin film technique.

1. Introduction

During the past decade there have been many descriptions of vacuum deposited film microcircuitry in which various combinations of conductor, resistor and capacitor films have been used to produce electronic sub-systems.[1] These techniques have not supplanted the conventional printed circuit form of interconnection system because of the high capital cost of the semiconductors and the technical difficulty of producing pinhole-free layers of inorganic dielectric by vacuum deposition.

Some of these difficulties have been overcome by the appearance of the flip-chip transistor and capacitor which can be mounted directly on the substrate carrying the conductor system. The chief remaining technical obstacle is the provision of crossover insulation for a second conductor plane which is unavoidable in complex high density circuitry. Most of the attempts to produce this film by vacuum techniques have been unsuccessful because of the difficulty of depositing adequate film thickness to insulate the near vertical sides of the underlying conductors. Dielectric films produced by the thick film technique are highly mobile during the deposition and subsequent firing cycles. They are less prone to pinhole failures and by virtue of their thickness will coat the edges of the conductor patterns.

Conductive and insulating inks for deposition on ceramic substrates are now commercially available so that the development of a microcircuit equivalent to the printed circuit board appears to be justified. Such a board also has the advantage of small dimensions necessary for high-speed circuitry, compatibility with unencapsulated semiconductor circuits, and potentially low manufacturing costs. However, thin-film evaporated circuitry still retains the advantage of high definition which is at present beyond the 'state of the art' of screen printing and must be used for conductors of 0·005 in (0·13 mm) or less in width. It is for this reason that the interconnection system described in this paper combines the advantages of both thick and thin film techniques.

2. Substrates

The choice of substrate for thick films is limited by the high firing temperatures required to give good film adhesion and remove the organic carriers used to transfer the material. Thus the conventional glass substrates used for vacuum evaporated films are unsuitable.

Alumina or beryllia substrates have the combined advantages of better thermal conductivity and adequate smoothness necessary for film thicknesses of 12–20 μm. The cost, although negligible in the system described here, has fallen over the past three years whilst surface finish and flatness have improved. The alumina substrate used in these investigations was $2 \times 1 \times 0{\cdot}020$ in with a surface camber of 0·004 in/inch.

3. Conductors

Pre-cleaning of the substrates is not essential before the application of the conductor films. The printing apparatus shown in Fig. 1 was used to deposit both the conductor and dielectric films. With the exception of the substrate holder the equipment is standard. For the first layer, carrying a set of duplicate registration marks, the printed pattern is centralized on the substrate. For subsequent conductor planes the lamps located in the transparent substrate holder provide back illumination of the pre-printed registration marks on the substrate assisting with alignment of the screen.

To obtain the maximum possible print resolution necessary for the power plane, a duplex metal stencil

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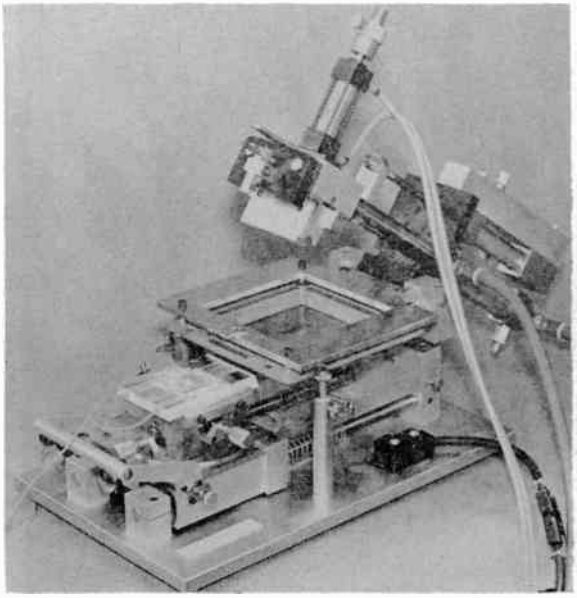


Fig. 1. Thick film printing apparatus.

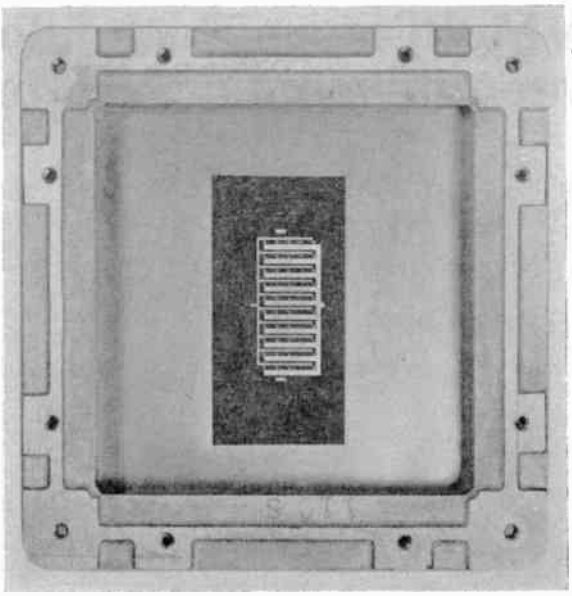
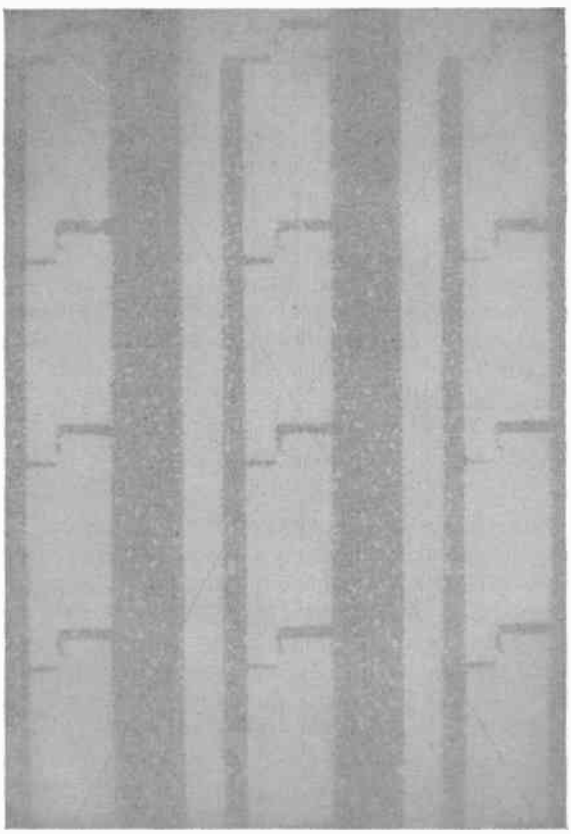
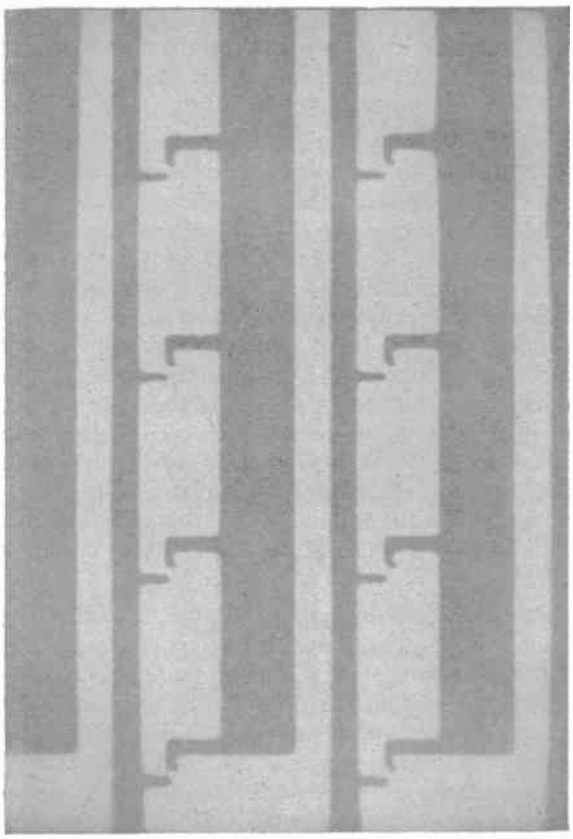


Fig. 2. Etched metal stencil screen.



(a) Discontinuous screened gold deposit (magnification ×10).



(b) Uniform screened gold deposit (magnification ×10).

Fig. 3.

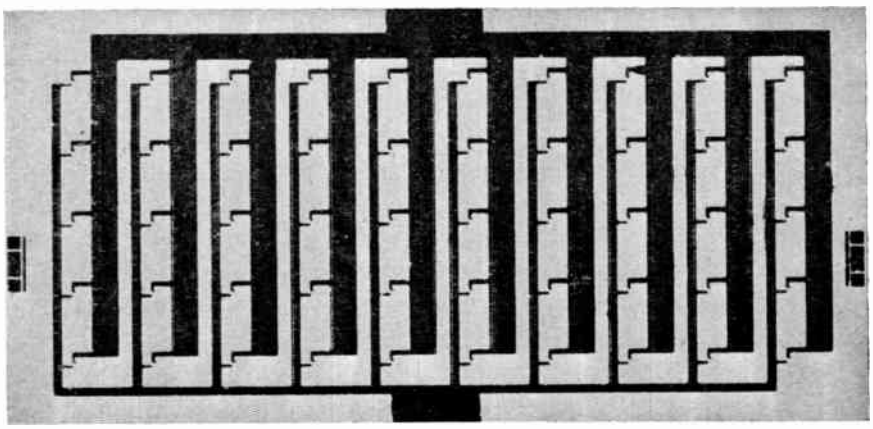


Fig. 4. Power plane.

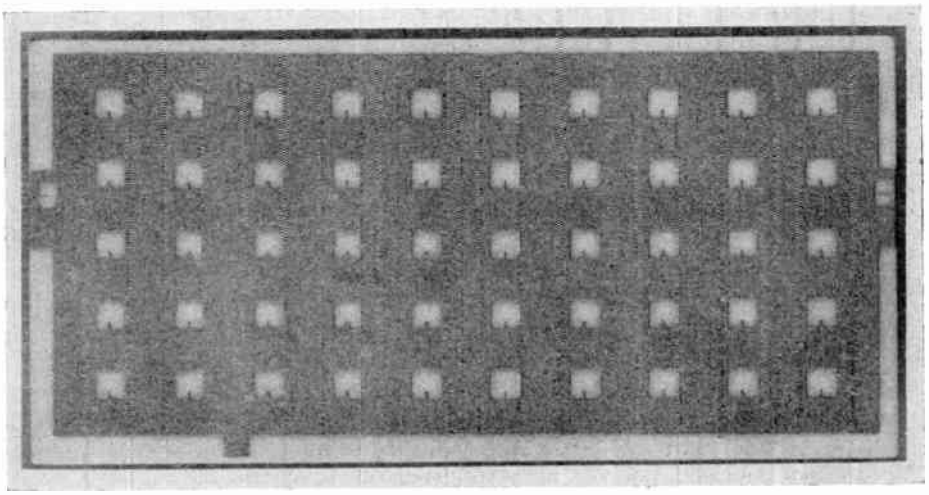


Fig. 5. Earth plane.

mask, shown in Fig. 2, was used. This is formed from a 0·005 in (0·13 mm) molybdenum sheet in one side of which is etched the conductor pattern and the other side is perforated with 0·005 in (0·13 mm) holes with 0·003 in (0·075 mm) separation coincident with the pattern. Although its cost is higher than the customary stainless steel screen its durability and resolution is substantially improved.

The choice of metallization inks for the power and earth planes is determined by the need to obtain the highest conductivity free from fissures and discontinuities, (unlike the deposit shown in Fig. 3(a)), and compatibility with the superimposed dielectric glazes. For these reasons a gold paste was chosen which gives uniform films shown in Fig. 3(b) of post-dried resistivity of 15 mΩ/square for a thickness of 15 μm when deposited through a 325-mesh screen. The printed substrates are dried on a hot plate at 400°C and then transferred to a muffle furnace. The power plane, shown in Fig. 4, is fired at 900°C and the earth plane, shown in Fig. 5, is fired at 775°C; both use the same gold paste. Firing of the earth plane at this temperature gives an adequate margin below the distortion temperature of the intermediate glaze layer. The resultant films are normally firmly adherent both to the substrate and the glaze layer.

4. Selection of Glaze Dielectrics

4.1. *Glaze Specification*

Glaze frits were originally developed for use by the vitreous enamelling and pottery industries. Their composition was empirically chosen to match metal and ceramic surfaces used in this field. Table 1 shows typical frit compositions and those in the classes A, B and C are found to be suitable for electronic applications.

Table 1

Typical glaze compositions

Glaze	PbO	SiO_2	Ca	Zr	Al_2O_3	Ti	Na	K	Ba	B_2O_3
A	major	major	ND	major	ND	ND	ND	ND	ND	ND
B	major	major	0·1%	ND	ND	ND	ND	ND	ND	ND
C	major	major	0·1%	ND	2%	ND	ND	ND	ND	ND
D	2%	major	5%	ND	major	ND	3%	ND	major	5%
E	major	major	0·1%	1%	ND	1%	0·1%	0·1%	ND	0·3%

Specifications for glazes suitable for multi-layer thick film circuitry can be summarized as follows:

(a) Well-defined softening temperature, permitting the use of glazes with different compositions and firing temperatures for several planes in a single structure.

(b) Freedom from gross defects such as bubbles, blisters, etc.

(c) Ability to form smooth uniform layers with a surface finish better than 10^{-6} in c.l.a.

(d) Alkali freedom to minimize ion migration.

(e) Non-reactive with the available conducting inks.

(f) Ease of dispersal in suitable carrier mediums for deposition by screen printing.

(g) Ease with which the fired films are etched for interplane connections.

(h) Correctly matched thermal coefficient of expansion with 99·5% alumina to ensure that the glaze films remain in compression over the temperature range 20–100°C.

(i) Range of permittivities from 5 to 500, the former for low-capacitance crossovers and the latter for decoupling between the power and earth planes.

As there is little documented information on the performance of commercially available glazes for microcircuits, it was necessary to study their behaviour at temperatures in the range 500–950°C. A small pot furnace was assembled in which an alumina substrate coated with the experimental glaze or a crucible containing the frit could be observed throughout its firing cycle. In this way the approximate melting temperature of the bulk frit could be obtained together with information on the evolution of gas bubbles and film reactivity with metallized patterns.

The results of these tests have shown that many glazes offered by the manufacturers are unsuitable, the chief failing being the excessive bubble formation within the glaze, unsuitable surface finish, and the incompatibility with gold. Extension of the heating time at the firing temperature does not reduce the incidence of the bubbles in the majority of the glazes examined. Another characteristic defect is the crawling of the glaze over the substrate surface frequently leaving the gold conductors uncoated.

4.2. *Multiple Glaze Layers*

For multi-layer applications the main requirement was the selection of two glazes having substantially different softening temperatures, compatible with each other, the conductor materials and the substrate. From the results of the single layer investigations discussed above several promising combinations were selected, but were later rejected on account of their incompatibility and inferior surface finish.

When the final choice was made, multi-plane assemblies were produced to ascertain their combined electrical and mechanical properties. Fault-free modules were made with three coats of the preferred glazes through 165-mesh screens giving thicknesses of 50 μm each.

The combined firing schedules for the assembly were:

Power plane Au	fired at 900°C
Dielectric glaze	fired at 870°C
Earth plane Au	fired at 775°C
Dielectric glaze	fired at 775°C

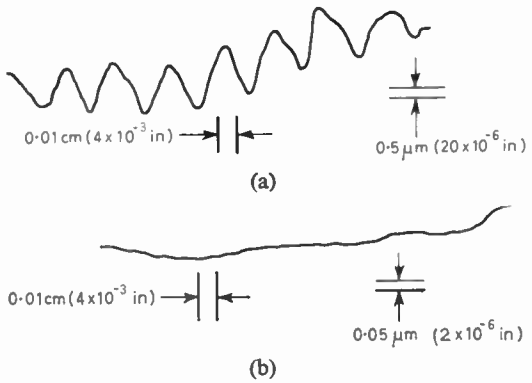


Fig. 6. Typical surface finish of (a) first glaze, (b) second glaze.

Table 2

Electrical properties of the glazes used

Glaze	Capacitance (pF/cm²)	tan δ	Thickness ($d \times 10^{-3}$ in)	Insulation resistance (ohms)	Firing temperature (degC)	Firing time (minutes)
1	150	0·01 to 0·02	2	10^{10}	870°	5
2	100	0·01	2	10^{10}	775°	90

Figure 6(a) shows the first glaze surface finish and (b) shows the second glaze surface finish, as obtained from Talystep measurements. The first glaze which is commercially offered as a crossover dielectric for thick film application is sintered at 870°C and therefore retains the screen pattern even when two or three coats are applied through a 165-mesh screen.

5. Electrical Properties

No suitable high-permittivity materials meeting the specification for the power/earth plane insulation in a multi-layer structure were found. Our work has shown that although glazes for capacitor applications are available their adhesion to both metal and substrate were inadequate.

Some typical electrical properties of glazes used are shown in Table 2.

6. Interplane Connections

Provision must be made in all multi-plane structures for interplane connections. For microminiature boards intended for use with unencapsulated silicon circuits these through connections must be 0·005 in (0·13 mm) or less in diameter and spaced less than 0·005 in (0·13 mm) apart. The printing tolerances for holes in glazes do not meet these requirements, not only due to screen stencil difficulties but also due to the mobility of the glaze during the firing cycle. The present dimensional limit is 0·020 in (0·5 mm). Chemical etching of the glazes permits better tolerances and adequate registration of holes in several planes is achieved with the photo-resist process.

The interplane connections are produced by electrolytically depositing pure gold until they are level with the surface of the surrounding glaze as shown in Fig. 7. Using this technique the connections required for mounting the semiconductor chips are raised to the surface of the earth plane dielectric which supports the thin film signal matrix.[2]

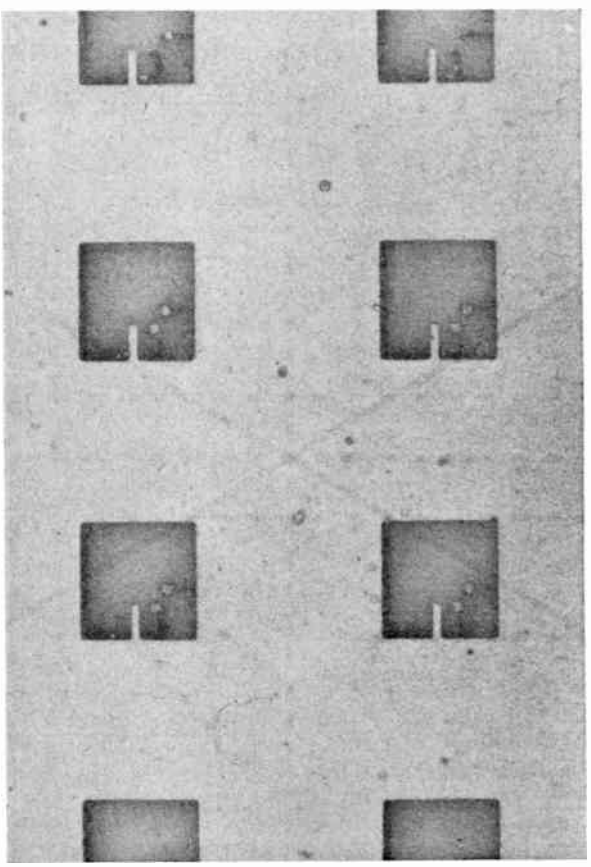


Fig. 7. Interplane connections in chip mounting zones.

7. The Signal Matrix

No concentrated attempts have been made to print the 0·005 in (0·13 mm) conductors used for the logic connections. That such attempts would be unjustified is apparent from the quality of the conductors shown in Fig. 3, for which a specially formulated ink was used in conjunction with an etched metal stencil. Difficulties could also be encountered in firing the conductors at a sufficiently high temperature to obtain the necessary adhesion without distortion of the underlying glaze layers. For these reasons we have to revert to the thin film technique for which the earth plane glaze forms a smooth surface which can be cleaned by using normal processes.

For compatibility with design automation techniques the signal connections are made in two orthogonal conductor planes insulated from each other by strips of an organic dielectric. The conductors 0·5 μm thick are etched from continuous sheets of evaporated gold on chromium. The dielectric film is comparatively hard and unlike evaporated films of silicon monoxide is deposited on the edges of the conductor strips. The capacitance of crossovers is 0·2 pF.

At this stage pillars are electrolytically deposited at the ends of the conductors in the chip mounting areas in readiness to receive the silicon semiconductor circuits which are mounted using an ultrasonic bonding technique.[3]

Finally, conductor routes between the semiconductor elements are made by the deposition of aluminium links at selected crossover points in the signal matrix.

8. Conclusions

It has been shown that the low-cost thick film process can be used to produce miniature multi-layer circuit boards. Suitable dielectric glazes can be selected for use in such a system and pinhole-free insulating layers are obtained using a screen printing technique.

Although thin film and electroplating techniques are used to complete the module because of the present limitations in obtaining very narrow lines, the continuing development in the 'state of the art' and materials will no doubt make it possible to produce the entire system by the thick film process.

9. Acknowledgments

The authors gratefully acknowledge the assistance given by their colleagues at I.C.L. and thank the Directors of I.C.L. and the Ministry of Technology for permission to publish this information which resulted from work supported by a normal cost-sharing contract under the Ministry's Advanced Computer Technology Project.

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Manuscript received by the Institution on 15th February 1968. (Paper No. 1288/CC29.)

Statistics of the British Electronics Industry (*continued from page 356*)

comparable. Then, as the industry is subject to very rapid technological change, it is possible that the increase in production represents a switch from labour-intensive to capital-intensive methods. On the other hand, however, the industry employs a higher than average number of qualified personnel; 2·4% of the total employees in the electronics industry are qualified against 0·4% of those in manufacturing as a whole.

Another interesting feature of the industry is its geographical distribution. The overwhelming concentration is in the South-East, particularly in Greater London, although the proportion employed there has remained stable after a decline in 1966. There is a steady growth in Scotland which now employs more than 6% of the labour force. Scotland has attracted several of the largest firms in the industry, many of these being expatriate subsidiaries of U.S. corporations. The increased proportion of employment in the electronics industry in Scotland is a direct result of expansion of these expatriate firms which in some cases have retrained part of their existing labour force.

Notwithstanding the maintenance of the rate of growth in employment in the electronics industry, the pattern of unemployment in the most recent period gives cause for comment. Briefly, whereas in June 1966 the ratio of wholly unemployed to unfilled vacancies was 1 : 4·6 overall, a year later it had fallen to 1 : 1·6. Most probably the reason is to be found in technological changes. It is known that there has been an increase in personnel in the computer industry and also that new productive capacity, e.g. for integrated circuitry and for colour television sets, has been established in the period. This could well have been accompanied by a run-down of capacity for more conventional items.

U.D.C. 621.372.22

Exact Solutions of Generalized Non-uniform Lines and their Classifications

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Summary: A system for general classification of non-uniform transmission lines—by transforming the independent variable x (representing distance) of the telegraphists' second-order linear differential equation to another independent variable $w = F(x)$ which is some function of x and then by constraining the transformed telegraphists' equation to simulate a standard second-order linear differential equation (the solution of which is well-known) expressed in terms of the same independent variable, w—is introduced. On the basis of this classification, two sets of generalized expressions for non-uniformity corresponding to each of the classes of the non-uniform lines have been derived. One set is in terms of the new independent variable w which may be any arbitrary function of x and the other set is in terms of another arbitrary function $f(x)$ [or $g(x)$] of x where $f(x)$ [or $g(x)$] characterizes the series impedance $Z(x)$ [or shunt admittance $Y(x)$] per unit length of the line in the form $Z(x) = Z_0 f(x)$ [or $Y(x) = Y_0 g(x)$] with Z_0 [or Y_0] being a constant of impedance [or admittance]. Corresponding to each set of generalized pattern of non-uniformity, one general solution for voltage for each class of line has been worked out. It is shown that the two sets of non-uniformity, derived for each class, are the most general ones and they require no further generalization.[3] Most of the non-uniform transmission lines, for which solutions are hitherto available, are found to be the members of the general classes introduced here. In addition, the generalized patterns of non-uniformity of certain new classes of non-uniform lines are derived and the applicability of this basic principle of classification for obtaining a number of transformable sub-classes is illustrated.

1. Introduction

The modern trend in electronic instrumentation towards microminiaturization has aroused considerable interest in the study of various patterns of non-uniformity of transmission lines. In consequence, a number of papers dealing with non-uniform lines have been published.[2–21] A comprehensive survey of the previous work shows that there is a general lack of attempt in introducing a realistic classification of solvable non-uniform lines. Certain classes of lines with specific patterns of non-uniformity, considered earlier,[4–7] have been shown recently[3, 7, 8] to be members of some more generalized classes of non-uniform lines leading to the merging of several old families of lines into a few general classes of recent origin. The classification, proposed in this paper, is the most general one and this particular feature of the classification enables one to identify any line with specified solvable non-uniformity as a member of one of the generalized classes.

The telegraphists' equation governing the behaviour of a non-uniform line is given by

$$\frac{\partial^2 V}{\partial x^2} - \frac{1}{Z(x)} \cdot \frac{\mathrm{d}Z(x)}{\mathrm{d}x} \cdot \frac{\partial V}{\partial x} - Z(x)Y(x)\frac{\partial V}{\partial t} = 0 \qquad \text{.....(1)}$$

where V is the voltage across the line at a distance x and $Z(x)$ and $Y(x)$ represent the series-impedance and shunt-admittance per unit length of the line at a distance x respectively. The restrictions imposed over $Z(x)$ and $Y(x)$ are that the former must have continuous first derivative and the latter must be continuous. When referred to the frequency-domain alone, eqn. (1) reduces to an ordinary linear second-order differential equation, namely,

$$V'' - \frac{Z'(x)}{Z(x)} V' - Z(x)Y(x)V = 0 \qquad \text{.....(2)}$$

where the prime over the symbol on its right-hand side signifies differentiation with respect to x only.

Defining

$$Z(x) = Z_0 f(x) \qquad \text{.....(3a)}$$

$$Y(x) = Y_0 g(x) \qquad \text{.....(3b)}$$

where Z_0 and Y_0 are impedance constant and admittance constant respectively, and $f(x)$ and $g(x)$, both being some functions of x, represent the pattern of non-uniformity,

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and denoting

$$P(x) \equiv \frac{f'(x)}{f(x)} \qquad \text{.....(4a)}$$

and

$$Q(x) \equiv f(x)g(x) \qquad \text{.....(4b)}$$

Equation (2) can be put in the form,

$$V'' - P(x)V' - Z_0 Y_0 Q(x) = 0 \qquad \text{.....(5a)}$$

For arbitrary $f(x)$ and $g(x)$, with no inter-relationship between them, a closed formula for the general solution of eqn. (5a) is not available.[14] Consequently, solutions in closed-forms[4, 6-12] and in terms of known functions of analysis[17, 19, 21] for certain special cases of transmission lines have been given in the literature.

2. Principle of the Proposed Classification

The proposed classification of non-uniform lines consists in (i) transforming eqn. (5a) from x-domain to some other domain by changing the independent variable x to some other new independent variable $w = F(x)$[1, 9, 10] and then (ii) equating the coefficients of the transformed equation with the corresponding coefficients of like-terms of a chosen standard equation (with well-known solution) expressed in terms of the same independent variable $w = F(x)$. From the relations obtainable from (ii), two separate sets of expression for $f(x)$ and $g(x)$, as defined in eqns. (3a) and (3b) are found out, one set being in terms of arbitrary w and the other set in terms of arbitrary $f(x)$ (or arbitrary $g(x)$ because of the applicability of the principle of duality for the patterns of non-uniformity of lines[2]). The name of the standard linear second-order differential equation chosen for comparison with the transformed telegraphists' equation is given to that class of non-uniform lines associated with the patterns of non-uniformity derived from this comparison. The examples that follow make the system of classification self-explanatory.

2.1. *Mathematical Formulation*

If the independent variable of x of eqn. (5a) written as

$$V'' - \frac{f'}{f}V' - Z_0 Y_0 f g V = 0 \qquad \text{.....(5b)}$$

is changed to a new independent variable $w = F(x)$, then (5b) reduces to[10, 21]

$$\ddot{V} + \frac{w'' - (f'/f)w'}{(w')^2}\dot{V} - Z_0 Y_0 \frac{fg}{(w')^2} V = 0 \qquad \text{.....(6a)}$$

Since,

$$\frac{w'' - (f'/f)w'}{(w')^2} = -\frac{1}{f}\cdot\frac{\mathrm{d}}{\mathrm{d}x}(f/w')$$

(6a) may be put in the form

$$\ddot{V} - \frac{1}{f}\cdot\frac{\mathrm{d}}{\mathrm{d}x}(f/w')\dot{V} - Z_0 Y_0 \frac{fg}{(w')^2} V = 0 \qquad \text{.....(6b)}$$

where the dot over the symbol denotes differentiation with respect to w only.

If the chosen standard linear second-order differential equation associated with the name of the proposed class is taken to be

$$\ddot{V} - P(w)\dot{V} - Z_0 Y_0 Q(w) V = 0 \qquad \text{.....(5c)}$$

with its general solution

$$V = A_1 M(w) + B_1 N(w) \qquad \text{.....(5d)}$$

where $M(w)$ and $N(w)$ are some functions of w, and A_1 and B_1 are constants to be determined from the imposed boundary conditions of the line then constraining eqn. (6b) to simulate eqn. (5c) yields

$$\frac{1}{f}\cdot\frac{\mathrm{d}}{\mathrm{d}x}(f/w') = P(w) \qquad \text{.....(7a)}$$

and

$$\frac{fg}{(w')^2} = Q(w), \quad \text{i.e., } g = \frac{(w')^2}{f} Q(w) \qquad \text{.....(7b)}$$

Relation (7a) shows that $f(x)$ may be obtainable in terms of w which may be any arbitrary function of x or alternatively w can be made available in terms of arbitrary $f(x)$. Thus, corresponding to an arbitrary value of w, one set of non-uniformity may be obtained by expressing $f(x)$ and $g(x)$ in terms of w and the substitution of this arbitrary w in solution (5d) gives the general solution for this set of non-uniformity. Corresponding to arbitrary $f(x)$, the other set of non-uniformity may be derived by finding out w in terms of $f(x)$ using (7a) and then expressing $g(x)$ in terms of $f(x)$ as given in eqn. (7b). The substitution of this value of w in terms of arbitrary $f(x)$ into solution (5d) yields the general solution of voltage for the second set of non-uniformity.

Example 1. *Generalized Standard Bessel Lines:* Substitution of

$$P(w) = -\frac{1}{w} \qquad \text{.....(8a)}$$

and

$$Q(w) = \left(k^2 - \frac{n^2}{w^2}\right) \qquad \text{.....(8b)}$$

where n is any constant and k is a constant $\neq 0$, reduces eqn. (5c) to the form

$$\ddot{V} + (1/w)\dot{V} + [(\mathrm{j}k\sqrt{Z_0 Y_0})^2 - (n\sqrt{Z_0 Y_0}/w)^2]V = 0 \qquad \text{.....(8c)}$$

which is Bessel's equation of order $n\sqrt{Z_0 Y_0}$ having its general solution

$$V = A_1 \mathrm{J}_{n\sqrt{Z_0 Y_0}}(\mathrm{j}k\sqrt{Z_0 Y_0}w) + B_1 \mathrm{Y}_{n\sqrt{Z_0 Y_0}}(\mathrm{j}k\sqrt{Z_0 Y_0}w) \qquad \text{.....(8d)}$$

where J and Y are Bessel functions of first-kind and second-kind respectively and $j = \sqrt{-1}$.

A comparison of eqns. (7a) with (8a) and (7b) with (8b) gives

$$\frac{1}{f}\cdot\frac{d}{dx}(1/w') = -\frac{1}{w} \qquad \text{.....(8e)}$$

and

$$g = \frac{(w')^2}{f}\left(k^2 - \frac{n^2}{w^2}\right) \qquad \text{.....(8f)}$$

Case (i): in terms of an arbitrary value of w.

Equation (8e) may be written as

$$\frac{\frac{d}{dx}(f/w')}{(f/w')} = -\frac{w'}{w}$$

which, on integration with respect to x, gives

$$\log_e(f/w') = -\log_e w + \log_e k_1$$

where k_1 is a constant of integration. This may be simplified to

$$f(x) = k_1(w'/w) \qquad \text{.....(8g)}$$

Inserting this value of $f(x)$ in eqn. (8f) gives

$$g(x) = (1/k_1)ww'\left(k^2 - \frac{n^2}{w^2}\right) \qquad \text{.....(8h)}$$

Thus, corresponding to non-uniformity defined by eqns. (8g) and (8h), the telegraphists' equation reduces to Bessel equation giving its solution represented by eqn. (8d) where $w = F(x)$ is an arbitrary function of x.

Case (ii): in terms of arbitrary $f(x)$ where $f(x)$ is given as

$$Z(x) = Z_0 f(x) \qquad \text{.....(8i)}$$

Writing eqn. (8g) as

$$(w'/w) = (1/k_1)f(x)$$

and then integrating, we get

$$\log_e w = (1/k_1)\int f(x)\,dx + k_0$$

where k_0 is a constant of integration whence

$$w = k_2 \exp\{(1/k_1)\int f(x)\,dx\} \qquad \text{.....(8j)}$$

where

$$k_2 = \exp(k_0)$$

is a constant.

Substition of this value of $f(x)$ into eqn. (8f) gives

$$g(x) = (1/k_1^2)f(x)[(kk_2)^2 \exp\{(2/k_1)\int f(x)\,dx\} - n^2] \qquad \text{.....(8k)}$$

Thus, for the pattern of non-uniformity characterized by eqns. (8i) and (8k), the voltage-solution is eqn. (8d) where w is given by eqn. (8j) in terms of $f(x)$.

Example 2: Generalized Transformable Bessel Lines

Starr[5] showed that the solution of eqn. (5a) with

$$P(w) = (\alpha/w) \qquad \text{.....(9a)}$$

and

$$Q(w) = w^{\alpha+\beta} \qquad \text{.....(9b)}$$

is obtainable as

$$V = A_1 w^{\frac{1+\alpha}{2}} J_{\frac{1+\alpha}{2+\alpha+\beta}}\left[2j\frac{\sqrt{Z_0Y_0}}{2+\alpha+\beta}w^{\frac{2+\alpha+\beta}{2}}\right] + B_1 w^{\frac{1+\alpha}{2}} J_{-\frac{1+\alpha}{2+\alpha+\beta}}\left[2j\frac{\sqrt{Z_0Y_0}}{2+\alpha+\beta}w^{\frac{2+\alpha+\beta}{2}}\right] \qquad \text{.....(9c)}$$

where $j = \sqrt{-1}$, α and β are arbitrary constants. Comparison of eqns. (7a) with (9a) and (7b) with (9b) leads to

$$\frac{1}{f}\cdot\frac{d}{dx}(f/w') = (\alpha/w) \qquad \text{.....(9d)}$$

and

$$g = \frac{(w')^2}{f}w^{\alpha+\beta} \qquad \text{.....(9e)}$$

Case (i): in terms of arbitrary w.

Writing eqn. (9d) as

$$\frac{\frac{d}{dx}(f/w')}{(f/w')} = \alpha(w'/w)$$

and then integrating with respect to x, we get:

$$\log_e(f/w') = \alpha\log_e w + \log_e k_1 = \log_e k_1 w^\alpha$$

which may be simplified to

$$f(x) = k_1 w' w^\alpha \qquad \text{.....(9f)}$$

where k_1 is a constant of integration. Putting this value of $f(x)$ in eqn. (9e) gives

$$g(x) = (1/k_1)w'w^\beta \qquad \text{.....(9g)}$$

Hence, corresponding to the non-uniformity described by eqns. (9f) and (9g), the voltage-solution is given by eqn. (9c) where $w = F(x)$ is an arbitrary function of x.

Case (ii): in terms of arbitrary $f(x)$ where

$$Z(x) = Z_0 f(x) \qquad \text{.....(9h)}$$

Writing eqn. (9d) as

$$w\frac{d}{dx}(f/w') = \alpha f$$

and then integrating,

$$(w/w')f = (\alpha+1)\int f\,dx + a_0$$

where a_0 = a constant of integration. Putting this as

$$(w'/w) = \frac{f}{(\alpha+1)\int f\,dx + a_0}$$

and then integrating once more, gives

$$\log_e w = \int \frac{f}{(\alpha+1)\int f\,dx + a_0}\,dx + \log_e k_2$$

where k_2 is another constant of integration. This may be reduced to

$$\log_e w = \log_e \left\{\int f\,dx + k_1\right\}^{\frac{1}{\alpha+1}} + \log_e k_2$$

where

$$k_1 = \frac{a_0}{\alpha+1}$$

giving

$$w = k_2\left\{\int f\,dx + k_1\right\}^{\frac{1}{\alpha+1}} \qquad \text{.....(9i)}$$

Substitution of the value of w into eqn. (9e) gives

$$g(x) = k_3 f(x)\left[\int f(x)\,dx + k_1\right]^{\frac{\beta-\alpha}{\alpha+1}} \qquad \text{.....(9j)}$$

where

$$k_3 = \frac{k_2^{\alpha+\beta+2}}{(\alpha+1)^2}$$

Thus, the voltage-solution is given by eqn. (9c) where w is defined in eqn. (9i) when the pattern of non-uniformity is characterized by eqns. (9h) and (9j).

Following the same procedure as illustrated in the above examples, patterns of non-uniformity for several classes of transmission lines with well-known solutions are evaluated and the results are displayed in Table 1.

In Table 1, k_1 and k_2 are arbitrary constants unless otherwise stated, and $k_1 \neq 0$ and A_1, A_2, B_1 and B_2 involved in voltage-solution are constants to be determined from the end-constraints of the line.

Examination of the two sets of generalized pattern of non-uniformity, obtained in this paper, reveals that the first set of non-uniformity in terms of some arbitrary value of w is in agreement with the results obtainable by the application of Berger's technique of generalization,[3] and the form of the second set of non-uniformity in terms of arbitrary $f(x)$ resembles that of the generalized expression of non-uniformity derived earlier by Dutta Roy[10] and Swamy and Bhattacharyya.[15] Since Table 1 contains the most generalized expressions of non-uniformity, Berger's generalization[3] is redundant for the results of this

Table 1

Classification, generalized pattern of non-uniformity and solution of transmission line

Nomenclature of classification and associated standard linear 2nd-order differential equation	Pattern of non-uniformity and voltage-solution $Z(x) = Z_0 f(x)$, $Y(x) = Y_0 g(x)$	
	in terms of arbitrary $w = F(x)$	in terms of arbitrary $f(x)$
1. Generalized proportionate line $\frac{d^2V}{dw^2} - Z_0Y_0V = 0$	$f(x) = (1/k_1)w'$, $g(x) = k_1 w'$ $V = A_1 \exp(w\sqrt{Z_0Y_0}) + B_1 \exp(-w\sqrt{Z_0Y_0})$	$g(x) = k_1^2 f(x)$, $w = k_1\int f\,dx + k_2$ $V = A_2 \exp\{\sqrt{Z_0Y_0}(k_1\int f\,dx + k_2)\} + B_2 \exp\{-\sqrt{Z_0Y_0}(k_1\int f\,dx + k_2)\}$
2. Generalized exponential line $\frac{d^2V}{dw^2} + 2k\frac{dV}{dw} - Z_0Y_0V = 0$ k is a constant for exponential taper	$f(x) = k_1 w' \exp(-2kw)$ $g(x) = (1/k_1)w' \exp(2kw)$ $V = A_1 \exp\{(-k+m)w\} + B_1 \exp\{(-k-m)w\}$ $m = \sqrt{k^2 + Z_0Y_0}$	$g(x) = \frac{f(x)}{(k_1 - 2k\int f\,dx)^2}$ $w = (1/2k)\log_e(1/F_x)$ $V = A_2(1/F_x)^{-\frac{1}{2}+m} + B_2(1/F_x)^{-\frac{1}{2}-m}$ $F_x = k_1 - 2k\int f\,dx$ $m = (1/2)\sqrt{1 + (Z_0Y_0/k^2)}$, $k \neq 0$
3. Generalized Euler line $\frac{d^2V}{dw^2} + \frac{p}{w}\cdot\frac{dV}{dw} - \frac{Z_0Y_0}{w^2}V = 0$ p is a constant	$f(x) = k_1 w' w^{-p}$ $g(x) = (1/k_1)w' w^{p-2}$ $V = A_1 w^{-m_1+m_2} + B_1 w^{-m_1-m_2}$ $m_1 = \frac{p-1}{2}$, $m_2 = \sqrt{m_1^2 + Z_0Y_0}$	$g(x) = f(x)/(m_1F_x)^2$ $w = F_x^{-1/m_1}$ $V = A_2F_x^{\frac{1}{2}+m_2} + B_2F_x^{\frac{1}{2}-m_2}$ $F_x = \int f\,dx + (k_1/m_1)$ $m_1 = p-1$, $m_2 = \sqrt{(1/4) + (Z_0Y_0)/m_1^2}$, $p \neq 1$

Table 1 (*contd.*)

Nomenclature of classification and associated standard linear 2nd-order differential equation	Pattern of non-uniformity and voltage-solution $Z(x) = Z_0 f(x)$, $Y(x) = Y_0 g(x)$	
	in terms of arbitrary $w = F(x)$	in terms of arbitrary $f(x)$
4. Generalized pseudo-exponential line $\frac{d^2V}{dw^2} + k\frac{dV}{dw} - Z_0Y_0V\exp(2kw) = 0$ k is a constant $\neq 0$	$f(x) = k_1 w' \exp(-kw)$ $g(x) = (1/k_1)w' \exp(3kw)$ $V = A_1 \exp\left\{-kw - \frac{\sqrt{Z_0Y_0}}{k}\exp(kw)\right\} + B_1 \exp\left\{-kw + \frac{\sqrt{Z_0Y_0}}{k}\exp(kw)\right\}$	$g(x) = k_1^2 f(x)/F_x^4$ $w = (1/k)\log_e(k_1/F_x)$ $V = A_2F_x(1/k_1)\exp\left(-\frac{mk_1}{F_x}\right) + B_2F_x(1/k_1)\exp\left(\frac{mk_1}{F_x}\right)$ $F_x = k_2 - k\int f\,dx$ $m = (\sqrt{Z_0Y_0}/k)$
5. Generalized Su's hyperbolic line $\frac{d^2V}{dw^2} + 2\tanh w\frac{dV}{dw} - Z_0Y_0V = 0$	$f(x) = k_1 w' \operatorname{sech}^2 w$ $g(x) = (1/k_1)w' \cosh^2 w$ $V = A_1(\cosh mw/\cosh w) + B_1(\sinh mw/\cosh w)$ $m = \sqrt{1+Z_0Y_0}$	$g(x) = \frac{k_1^2 f(x)}{[k_1 - (\int f\,dx - k_2)^2]^2}$ $w = \tanh^{-1}\left(\frac{\int f\,dx - k_2}{k_1}\right) = \log_e(F_1/F_2)^{\frac{1}{2}}$ $V = A_2\frac{(F_1/F_2)^{m/2}}{(F_1/F_2)^{\frac{1}{2}} + (F_2/F_1)^{\frac{1}{2}}} + B_2\frac{(F_2/F_1)^{m/2}}{(F_1/F_2)^{\frac{1}{2}} + (F_2/F_1)^{\frac{1}{2}}}$ $F_1 = k_1 - k_2 + \int f\,dx$ $F_2 = k_1 + k_2 - \int f\,dx$ $m = \sqrt{1+Z_0Y_0}$
6. Generalized Bessel's line $\frac{d^2V}{dw^2} + (1/w)\frac{dV}{dw} - Z_0Y_0\left(k^2 - \frac{n^2}{w^2}\right)V = 0$ n is any constant and k is a constant $\neq 0$	$f(x) = k_1(w'/w)$ $g(x) = (1/k_1)ww'\left(k^2 - \frac{n^2}{w^2}\right)$ $V = A_1 J_{n\sqrt{Z_0Y_0}}(j\sqrt{Z_0Y_0}kw) + B_1 Y_{n\sqrt{Z_0Y_0}}(j\sqrt{Z_0Y_0}kw)$ $j = \sqrt{-1}$	$g(x) = \frac{1}{k_1^2}\cdot f(x)\left[\left\{kk_2\exp\left(\frac{\int f\,dx}{k_1}\right)\right\}^2 - n^2\right]$ $w = k_2\exp\{(1/k_1)\int f\,dx\}$ $V = A_2 J_{n\sqrt{Z_0Y_0}}(j\sqrt{Z_0Y_0}kw) + B_2 Y_{n\sqrt{Z_0Y_0}}(j\sqrt{Z_0Y_0}kw)$ $j = \sqrt{-1}$
7. Generalized transformable Bessel's line $\frac{d^2V}{dw^2} - \frac{\alpha}{w}\cdot\frac{dV}{dw} - (Z_0Y_0w^{\alpha+\beta})V = 0$ α and β are arbitrary constants	$f(x) = k_1 w' w^{\alpha}$ $g(x) = (1/k_1)w' w^{\beta}$ $V = A_1 w^{\frac{1+\alpha}{2}} J_n(q) + B_1 w^{\frac{1+\alpha}{2}} J_{-n}(q)$ where $n = \frac{1+\alpha}{2+\alpha+\beta}$ $q = 2j\frac{\sqrt{Z_0Y_0}}{2+\alpha+\beta} w^{\frac{2+\alpha+\beta}{2}}$ $j = \sqrt{-1}$	$g(x) = k_3 f(x)[\int f\,dx + k_2]^{\frac{\beta-\alpha}{\alpha+1}}$ $w = k_1[\int f\,dx + k_2]^{\frac{1}{\alpha+1}}$ $k_3 = \frac{k_1^{\alpha+\beta+2}}{(\alpha+1)^2}$ Solution is same as in the adjacent column except that w is here as given above.

Table 1 (*contd.*)

Nomenclature of classification and associated standard linear 2nd-order differential equation	Pattern of non-uniformity and voltage-solution in terms of arbitrary $w = F(x)$ $Z(x) = Z_0 f(x)$, $Y(x) = Y_0 g(x)$
8. Generalized confluent hypergeometric line $\frac{d^2V}{dw^2} + \frac{\gamma - w}{w} \cdot \frac{dV}{dw} - \frac{Z_0 Y_0}{w} V = 0$ γ is any constant $\neq 0$, integers.	$f(x) = k_1 w' w^{-\gamma} \exp(w)$ $g(x) = (1/k_1) w' w^{\gamma-1} \exp(-w)$ $V = A_1 \, {}_1F_1(\alpha, \gamma, w) + B_1 w^{1-\gamma} \, {}_1F_1(\alpha+1-\gamma, 2-\gamma, w)$ $\alpha = Z_0 Y_0$
9. Generalized transformable hypergeometric line $(w-\gamma_1)(w-\gamma_2)\frac{d^2V}{dw^2} + \frac{b}{a}(w-\gamma_3)\frac{dV}{dw} + \frac{c}{a}V = 0$ γ_1, γ_2 and γ_3 are constants and $\gamma_1 \neq \gamma_2$ $\frac{c}{a} = -Z_0 Y_0$	$f(x) = k_1 w' \left[\frac{(w-\gamma_2)^{\gamma_2-\gamma_3}}{(w-\gamma_1)^{\gamma_1-\gamma_3}}\right]^{\frac{b}{a(\gamma_1-\gamma_2)}}$ $g(x) = (1/k_1) w' \left[\frac{(w-\gamma_1)^{\frac{a}{b}(\gamma_2-\gamma_1)+(\gamma_1-\gamma_3)}}{(w-\gamma_2)^{\frac{a}{b}(\gamma_1-\gamma_2)+(\gamma_2-\gamma_3)}}\right]^{\frac{b}{a(\gamma_1-\gamma_2)}}$ $V = A_1 \, {}_2F_1\left(\alpha, \beta; \gamma; \frac{w-\gamma_1}{\gamma_2-\gamma_1}\right) + B_1\left(\frac{w-\gamma_1}{\gamma_2-\gamma_1}\right)^{1-\gamma} \times$ $\times \, {}_2F_1\left(\alpha-\gamma+1, \beta-\gamma+1; 2-\gamma; \frac{w-\gamma_1}{\gamma_2-\gamma_1}\right)$ $\alpha+\beta+1 = \frac{b}{a}, \quad \gamma = \frac{b}{a} \cdot \frac{\gamma_1-\gamma_3}{\gamma_1-\gamma_2}, \quad \alpha\beta = \frac{c}{a} = -Z_0 Y_0$ This solution is, however, valid so long as $\left\lvert\frac{w-\gamma_1}{\gamma_2-\gamma_1}\right\rvert \ll 1.$ For solutions beyond this range, consult Refs. 21 and 23.
10. Generalized Hermite line $\frac{d^2V}{dw^2} - 2w\frac{dV}{dw} - Z_0 Y_0 V = 0$	$f(x) = k_1 w' \exp(w^2)$ $g(x) = (1/k_1) w' \exp(-w^2)$ (a) $V = A_1 H_\nu(w) + B_1 H_\nu(-w)$ for $\nu = -\frac{Z_0 Y_0}{2} \neq 0$, positive integers;[22] (b) $V = A_2 H_\nu(w) + B_2 \exp(w^2) H_{-\nu-1}(jw)$, $\nu = -\frac{Z_0 Y_0}{2}$, for ν arbitrary;[22] $H_\nu(w)$ is the Hermite function.[22]
11. Generalized transformable Hermite line $\frac{d^2V}{dw^2} + (\alpha+\beta w)\frac{dV}{dw} - Z_0 Y_0 V = 0$ α and β are some constants and $\beta \neq 0$.	$f(x) = k_1 w' \exp\{-\alpha w - (\beta/2)w^2\}$ $g(x) = (1/k_1) w' \exp\{\alpha w + (\beta/2)w^2\}$ (a) $V = A_1 H_\nu(t) + B_1 H_\nu(-t)$ for $\nu \neq 0$ and positive integers; (b) $V = A_2 H_\nu(t) + B_2 \exp(t^2) H_{-\nu-1}(jt)$ for ν arbitrary,[22] where $\nu = \frac{Z_0 Y_0}{\beta}$ and $t = j(\alpha+\beta w)/(2\beta)^{\frac{1}{2}}$ and $j = \sqrt{-1}$.

tabulation. This paper illustrates that the two different sets of non-uniformity corresponding to each class of solvable lines are obtainable from the application of the fundamental principle of changing the independent variable x of the telegraphists' equation to another independent variable w which is some function of x. The generalized expressions for the distribution of $Z(x)$ and $Y(x)$ in terms of arbitrary $f(x)$, for proportionate line, derived here, are found to agree with the results evaluated by Hellstrom.[12] The non-uniformity pattern for generalized exponential line, obtained in terms of arbitrary w, is found to conform to that derived by Jacobs[8] from the definition of generalized exponentiality of transmission line.[13] Moreover, the expression for $g(x)$ corresponding to arbitrary $f(x)$, derived in respect of generalized exponential line, resembles the expression obtained earlier[10,15] for certain solvable non-uniformity. Dutta Roy's generalized Bessel's line[10] with non-uniformity given by

$$f(x) = (1+mx)^{\alpha} \quad \text{and} \quad g(x) = (1+mx)^{\beta}$$

where α and β are some constants, is, in fact, a subclass of the generalized transformable Bessel's line, in terms of arbitrary w, displayed here. The distributions of non-uniformity for 'Hermite line', discovered by Swamy and Bhattacharyya,[17] are found to correspond with the generalized pattern of non-uniformity evaluated in this paper. Besides deriving expressions for generalized distributions of non-uniformity for certain new classes of non-uniform lines, it has been established well that all the generalized distributions of non-uniformity of solvable lines, obtained earlier by different methods,[3,8,12,15,17] may be derived from the application of the basic principle illustrated in this paper.

It is known that by transforming from one domain to some other domain[20] by discrete substitutions many non-standard equations may be reduced to the forms of some standard solvable equations, as was done by Starr[5] for the case of transformable Bessel's line. In fact, many patterns of generalized non-uniformity, for non-standard equations reducible to standard equations, may be evaluated by applying the principle followed here. Hence, several transformed families of lines, corresponding to each standard class, may be derived.

3. Acknowledgment

The authors have pleasure in thanking Professor R. L. Russell for his interest and encouragement. They appreciate the help of Mr. P. Bowron in the discussion and in the preparation of the manuscript. One of the authors (K. U. A.) gratefully acknowledges the financial support of the Government of Assam, India.

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Manuscript received by the Institution on 5th June 1968. (Paper No. 1229.)

Of Current Interest . . .

New North Sea Cables

Three submarine cables with the largest capacity in the world are to be laid between Kent and East Anglia and Belgium, the Netherlands and West Germany in 1971 and 1972 under the G.P.O.'s current £2000 million five-year plan for expansion. They will more than double the number of U.K.–European cable circuits in operation today. The new cables will run between Broadstairs and Ostend (64 nautical miles); between Aldeburgh and Domburg (82 nautical miles); and from Winterton to the Friesian island of Spiekeroog (285 nautical miles).

Decisions to lay the new cables followed the seven-nation London conference held in May 1967 on the initiative of the British Post Office. Each will carry 1260 circuits, with two-way transistor repeaters at intervals of just over seven miles. At the end of 1967 there were just over 1900 cable circuits in operation between Britain and the Continent; cables completed since then have brought the present total to 2880 circuits giving United Kingdom customers communication with Europe (in addition to 1200 microwave radio circuits). With telecommunication traffic between Britain and the Continent—including telephone calls and data-transmission and telex messages—growing at about 14% annually, the three new cables are expected to cover expansion over the next five years.

All the deep-sea sections will probably be laid by G.P.O. cableships. Contracts for manufacturing the cables and repeaters, and all terminal equipment, have been placed with Submarine Cables Ltd. The overall cost of the three projects—in the region of £3¾ million—will be borne *pro rata* by the British, Belgian, Dutch and German administrations.

Annual Report of the British Council

'It is a sign of the times that there are now more post-graduate than undergraduate overseas students in British universities', says the British Council's annual report for 1967–68. The report adds that the total number of overseas students in this country dropped from 73 000 in 1966–67 to 69 000 in 1967–68—the first recorded decrease.

The Council's scientific work has continued to be closely associated with that of the Royal Society, whose development of its international relations, specially in Europe, has done much to stimulate those scientific exchanges with which the Council is concerned. The report points out that more British scientists have visited the Soviet Union and the East European countries; there have been more exchanges with other Commonwealth countries and with Latin America where the Council now has a science officer in Argentine, as well as in Brazil, Chile and Mexico; and more overseas specialists have attended short courses arranged by the Council in Britain.

Educational work abroad concentrated on the training of teachers of English, the use of television in schools, and new methods of teaching science. The report underlines the Council's close collaboration in these fields with the Ministry of Overseas Development, the Centre for Educational Television Overseas, the Centre for Curriculum Renewal and Educational Development Overseas, and the Nuffield Science Project. More than half the 750 overseas tours by British specialists were concerned with science and technology, medicine and agriculture.

The Council maintains 122 libraries overseas, and is associated with 80 more. With the assistance of the Publishers' Association and the Book Development Council, 122 exhibitions of British books and periodicals were held in 53 countries. They included the annual display of 4000 volumes at the Frankfurt Book Fair and an exhibition of technical and scientific books in the National Library of Sofia—the first public showing of British books in Bulgaria since the war. Among the many publications of the Council itself probably the best-known to scientists and engineers is the annual 'Scientific Research in British Universities and Colleges, Vol. I: Physical Sciences'. This is prepared in collaboration with the Department of Education and Science and forms a valuable guide for industry as well as the universities themselves.

Changes in Primary Standards of Measurements

Changes are to be made to the values of some of the United Kingdom primary standards of measurement maintained at N.P.L., Teddington. Such changes are made from time to time in order to ensure consistency with the international standards of the metric system. (The last occasion was in 1948.) The changes are sufficiently small that they will affect only manufacturers and users of extremely precise instruments. Most of the instruments and meters used in commerce will not be affected.

The quantities concerned are the unit of electrical resistance, the unit of electrical potential, the acceleration due to gravity, and the international practical scale of temperature.

(1) The magnitude of the N.P.L. unit of resistance (ohm) will be increased by 3·7 parts per million from 1st January 1969.

(2) The magnitude of the N.P.L. unit of potential (volt) will be reduced by 13 parts per million from 1st January 1969.

(3) There will be no change in the value of gravity at Teddington adopted by N.P.L., but in consequence of a change in the international reference value at Potsdam, the difference between g at Teddington and the international reference value at Teddington will be reduced from 14 to 0 milligals.

(4) Changes in the thermodynamic temperatures of fixed points and coefficients of interpolation formulae used in the international scale of temperature will be made with effect from 1st January 1969. Information about the precise nature of these changes may be obtained on application to the Director, National Physical Laboratory, Teddington, Middlesex.

These changes are the consequence of resolutions passed at a meeting of the Comité International des Poids et Mesures, held in Paris on 14th to 17th October 1968 to which the United Kingdom was a party.

U.D.C. 621.319.4:666.29

The Development of Glaze Capacitors for Thick Film Circuits

By

J. P. HOLDEN†

Reprinted from the Proceedings of the Joint I.E.R.E.–I.E.E.–I.S.H.M. Conference on 'Thick Film Technology' held at Imperial College, London, on 8th to 9th April 1968.

Summary: For low-value capacitors (tens of picofarads) glass dielectrics have been chosen, whereas for higher values it has been necessary to use a mixture of a high-permittivity ceramic and a binder material. Existing thick-film conductor compositions have been used for electrodes. In the work on the low-value systems, a large number of combinations of different dielectric and electrode materials and their processing conditions have been assessed, and several usable systems have been determined. The reasons for the poor performance of other systems have been studied and are described.

The need to use multi-phase dielectrics for higher values, and the behaviour to be expected from such systems are discussed. Dielectrics have been made from mixtures of high-permittivity ceramics based on barium titanate and various glasses or bismuth oxide, and the various materials and processing parameters have been varied to attain the optimum performance. Data on the performance of high- and low-value capacitor systems are included.

1. Introduction

In the manufacture of thick film integrated circuits it is normal practice to print and fire only conductors and resistors, and to add discrete capacitors and active devices afterwards. However, it is possible to produce thick film capacitors[1] and even transistors,[2] and this should have two distinct advantages:

Reduction in cost due to the avoidance of individual handling, and the possibility of making several capacitors simultaneously.

Increased reliability, as such capacitors would be firmly bonded to the substrate.

The capacitor developed is a three-layer device in which glazes for lower electrode, dielectric and upper electrode are successively deposited on a ceramic substrate. Work on such devices has been reported by other authors[1, 3] and proprietary glazes for capacitors are now being marketed, but these are still at a comparatively early stage of development. This paper describes the independent development of suitable materials and the determination of appropriate processing conditions for dielectric and electrodes in order to obtain the desired electrical performance from the capacitors. The means of achieving these ends are largely dictated by existing practice in thick film technology in the following four ways:

(i) It is desirable to use conventional conductor compositions in order to simplify interconnections with other components of the circuit. Most of these compositions are fired in the temperature range 700–1000°C, and consequently the dielectric glazes should also mature in this range. Firings at temperatures above 1000°C would result in melting of the lower electrodes, and a glaze maturing at lower temperatures would become excessively fluid during the firing of the upper electrode.

(ii) As little variation in dielectric thickness can be obtained by screen printing and as the surface area available is restricted, the range of capacitance values required must be achieved by employing a range of dielectrics with differing permittivities. For typical dielectric thicknesses of 0·001 in and convenient plate areas of about 0·01 in^2 a range of permittivities from about five up to several hundreds is desirable. At the low end of the scale a homogeneous glass will suffice to give capacitors of a few tens of picofarads, whereas for high values a high permittivity ceramic would be required. As such ceramics will not sinter at the firing temperatures employed, it is necessary to include in the composition a certain amount of glass binder.

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(iii) As with other thick film glazes, it is desirable that the glazes employed should have thermal expansion coefficients similar to those of the substrate up to the annealing point of the glaze, to prevent excessive strains being set up on cooling. Throughout this investigation, high alumina substrates have been used, with thermal expansion coefficients of about $7{\cdot}3 \times 10^{-6}$ per degC over the range 20–600°C.

(iv) The materials used in the capacitor should be such that undesirable chemical reactions do not occur during the firings. In addition they should have low alkali content to reduce the dielectric losses.

The development work has been divided between capacitors with low-permittivity glassy dielectrics and those with high-permittivity composite dielectrics. These two aspects are dealt with separately in the subsequent sections.

2. Capacitors with Low-permittivity, Glassy Dielectrics

A number of possible glasses for dielectrics were selected according to the criteria listed above, and a number of popular conductor compositions were selected as electrode materials. A large number of combinations of these materials was assessed by making trial capacitors using a variety of processing conditions. Figure 1 shows the screen stencils employed for the capacitor test pattern and Fig. 2 shows a fired test substrate. Each combination of materials and processing conditions was assessed according to the number of capacitors free from short-circuits obtained on the test substrate. The most satisfactory combination was selected for further development and evaluation.

Five types of glass were chosen for detailed investigation namely:

A. Electroscience 4747

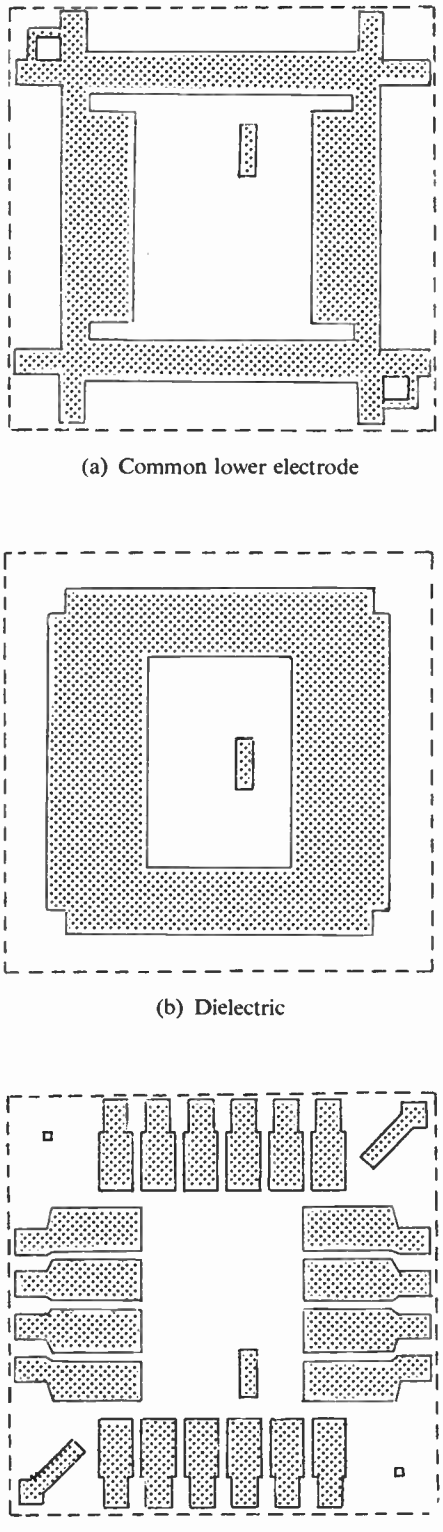
B. Lead zirconium silicate (Ramsden's F1169)

C. Barium borosilicate

D. Zinc borosilicate

E. Lead zinc borate

Glass A was a proprietary material supplied in screen printing form for producing insulating layers between crossing conductors. The other glasses were made into screen printing form by milling, sieving and dispersing in a proprietary organic medium using a triple roll mill. In order to obtain a reproducible print thickness the composition and rheology of the inks were standardized. An ink with 45 vol. per cent inorganic solids was found to give good printing behaviour and inks with this composition had similar viscosity shear rate characteristics, as measured on a cone and plate viscometer, irrespective of the dielectric



(a) Common lower electrode

(b) Dielectric

(c) Upper electrodes

Fig. 1. Screen stencils for capacitor test pattern (2·2 : 1).

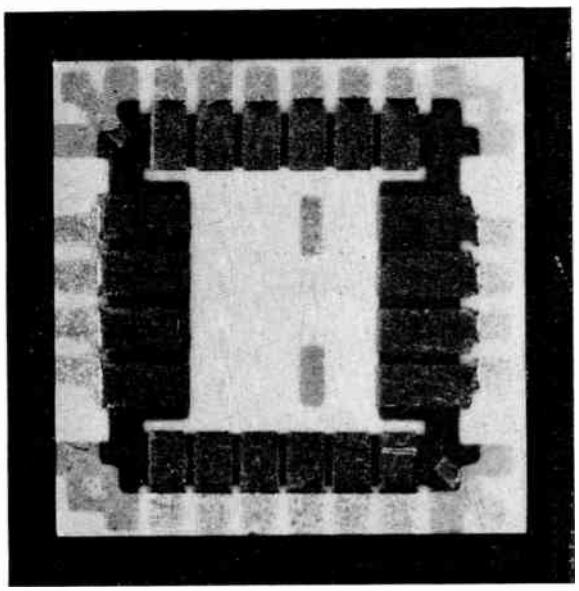


Fig. 2. Fired test substrate.

powder used. Some inks needed to be adjusted using a smaller amount of thinner.

The metals in thick film conductor formulations are present either as particles in suspension, or in solution as organo-metallic compounds. The former type are more commonly used on account of their good solderability. In the present investigation, suspension type inks of platinum-gold, palladium-gold and palladium-silver alloys, and solution types of silver and gold have been included.

In carrying out the processing, the printing was performed on a Rondec FP 560 machine, and the firings in a four-zone belt furnace. Lower electrode, dielectric and upper electrode were fired separately. The processing of each electrode material was kept constant during the investigation, i.e. a single print through a 325-mesh screen followed by a firing as recommended by the manufacturer. The dielectric was varied in thickness by applying either one or two prints through either 200- or 150-mesh screens, and in addition a number of firing schedules at different temperatures were carried out. The required firing schedules were roughly determined by continuously observing a trial specimen with a hot-stage microscope. The firing was judged to be sufficient when a smooth, void-free glaze had been produced.

The results of this initial stage of the investigation can be summarized as follows:

(i) Of the glasses used, Electroscience 4747 and the lead zirconium silicate F1169, were satisfactory. The 4747 gave good results when fired in the temperature range 800°–850°C whereas the F1169 could be fired in the range 750°–950°C.

(ii) Of the other glasses, the barium borosilicate had a tendency to craze, the zinc borosilicate was too refractory and the lead zinc borate reacted strongly with most electrode materials.

(iii) The surface profile of the electrode materials was investigated with a Talysurf machine. The suspension-type inks were shown to give a rough layer when fired, of about 0·0125 mm (0·0005 in) thickness. These electrodes had isolated peaks which tended to short-circuit the capacitors, and consequently two prints of dielectrics were always necessary in order to give a sufficient thickness. When only one of the electrodes was of this type, two prints through 200-mesh screens would give 99% good capacitors, but with both electrodes of the suspension type, two prints through 150-mesh screens were necessary.

(iv) The solution-type inks gave thinner, smoother electrodes, and using these materials it was possible to obtain 100% good capacitors employing only one print through a 200-mesh screen of the dielectric. As these electrodes are rapidly dissolved by solder, it was found necessary to apply a solder resist, or an encapsulant glaze before flow soldering.

(v) All of the electrode materials proved satisfactory except the PdAg, which tended to react with the dielectrics and become detached from the substrate.

(vi) Investigation of the capacitors using the Talysurf, sectioning and direct observation in the hot stage microscope revealed several mechanisms of short-circuiting. Using suspension-type lower electrodes, the dielectric printed thinly over the 'shoulders' of the electrode. This gave a line of short circuits along the shoulder if the dielectric thickness was insufficient. During the firing of the dielectrics, bubbles bursting at the surface left craters which in some cases extended down to the lower electrode. The firing time needed to be long enough for such craters to heal over. Firings at too high a temperature caused depressions to form near the edges of the glaze. In extreme cases, these depressions extended down to the peaks of the lower electrode. Finally, any dust or unevenness of the substrate prior to applying the lower electrode or dielectric could lead to a short-circuit. This latter failure mechanism is shown in Fig. 3, a section through a capacitor, in which a PtAu lower electrode is bowed upwards towards the upper electrode.

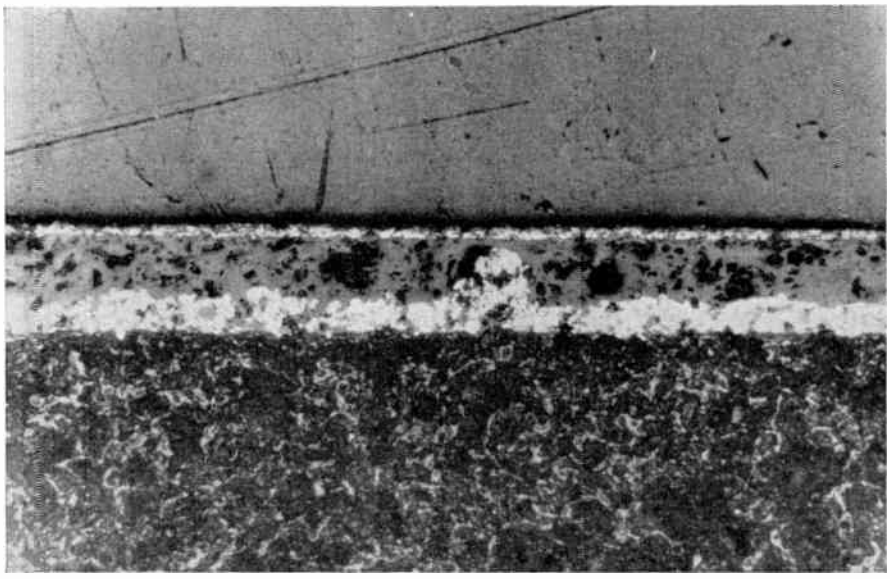


Fig. 3. One failure mechanism in a low-value capacitor.

As a result of this initial work the capacitor system chosen for further assessment was as follows:

Lower electrode: Du Pont 7553 PtAu fired at 850°C

Dielectric: two prints of Ramsden's F1169 fired at 750°–950°C

Upper electrode: Hanovia 7251 Au fired at 700°C

It was convenient to use the popular 7553 PtAu conductor for the lower electrode, as this material had already proved satisfactory for conducting paths, resistor terminations and pads for the attachment of discrete devices, and consequently a single print would suffice for all. The dielectric was chosen because of the wide range of firing temperatures that could be employed, and the solution type upper electrode was chosen because it gave a low incidence of short circuits.

Several hundred capacitors were constructed using this system, and the results obtained are summarized in Table 1.

Table 1

Performance of low-value capacitors

Capacitance:	
With two prints through 200 mesh	2000 pF/in²
With two prints through 150 mesh	1100 pF/in²
tan δ: 0·020 falling to 0·005 on ageing	
Temperature coefficient:	
(20°–150°C) 200 parts/10⁶/degC maximum	
Shelf ageing: +1½% in 6500 hours	
Reproducibility (coefficients of variation):	
(i) on single substrate	2%
(ii) on several substrates	4½%
(iii) batch to batch (including printing occasion, ink batch, glass batch)	10%

Further assessment is required of temperature coefficients below room temperature; stability under load, elevated temperature and humidity; breakdown voltage and frequency variations. Of particular interest is the high degree of reproducibility that has been obtained with relatively simple printing apparatus.

3. Capacitors with High-permittivity, Composite Dielectrics

As mentioned in the Introduction, a composite dielectric must be employed in order to obtain high permittivities and at the same time, adequate sintering when using conventional thick film conductor materials as electrodes. The composite must contain a high permittivity ceramic and one or more materials to act as binding agent. Two different approaches have been attempted by other workers. The ceramic has been mixed with the binder in the formulation of the printing ink.[1, 3] Alternatively, the ceramic has been incorporated in a thermodynamically unstable glass, which is used in the dielectric glaze, and which devitrifies during the firing.[4] The former approach is being investigated by the author.

The composite is a mixture of high- and low-permittivity phases. The permittivity obtained will be intermediate between those of the components, and a number of theoretical treatments have been carried out to predict the value from the concentrations of the components.[5] These treatments generally assume idealized microstructures but in practice the properties obtained depend markedly on the particular microstructure present, and in particular, on whether or not the phases form continuous networks.

In the present instance high permittivities can only be obtained if either the high permittivity ceramic forms a continuous network or if the gaps between the ceramic particles, occupied by the low-permittivity binder, are very small.

Statistical treatments of the structure in which the phases form random arrays predict that the ceramic will form a continuous network as long as the volume concentration of the binder does not exceed a certain value. The particular value depends on certain geometrical assumptions in the statistical treatment. However, the formation of these networks will be hindered if the ceramic is well wetted by the molten binder, since the binder will then tend to flow round each ceramic particle and isolate it from its neighbours. Nevertheless, it is evident in both cases that minimizing the quantity of glass, consistent with good sintering, will lead to high permittivities. Further uncertainties concerning the microstructure of the composite ensue from the chemical reactions which have been shown by x-ray diffraction analysis to occur between the phases.

Work carried out so far has been confined to mixtures of ceramics based on barium titanate with binders or either glass or bismuth oxide. Both pure barium titanate and a solid solution of barium titanate and barium stannate have been employed. The glass used was the lead zirconium silicate (F1169) used for the low permittivity dielectrics. The quantity of binder has been varied from 8% up to 50% of the total volume of solids in the ink. As with the low permittivity glazes, a number of general results were noted:

(i) In order to obtain a strong, well-sintered dielectric glaze, it is evident that sufficient binder must be present to form a continuous matrix containing the network of ceramic particles. Using such a quantity of glass (about 50 vol. per cent) it was observed in the hot stage microscope that, as with purely glassy dielectrics, pinholes formed during firing which extended down to the lower electrode. In the present case, however, the pinholes did not heal over on extending the firing. This inability of the dielectric to flow sufficiently was probably due to the increase of viscosity caused by the ceramic particles in suspension, and also to the loss of some glass by chemical reaction. Capacitors using such glazes had a high incidence of short-circuits.

(ii) Using smaller quantities of glass, pinholes were unable to form in this manner, but a semi-permeable dielectric was obtained. However, on account of the length and tortuosity of the paths between the electrodes short-circuits were very seldom encountered. It was possible to obtain short-circuit-free capacitors using suspension-type inks for both electrodes when employing two prints of the dielectric through 200-mesh screens, whereas 150-mesh screens were needed when using purely glassy dielectrics.

(iii) The glassy phase in the suspension-type electrodes flowed into the dielectric during the firings, thus reducing its permeability and increasing its strength.

(iv) The glassy phase from the suspension-type conductors had a marked effect on the electrical properties of the capacitors. The use of one such conductor (Du Pont PtAu 7553) gave capacitance values ten times those obtained using a glass-free, solution-type conductor. In addition, the major peak in the permittivity temperature curve moved from 125°C, characteristic of $BaTiO_3$, to about 55°C.

(v) Higher permittivities were obtained when bismuth oxide was substituted for glass as the binder material. This was probably due to the relatively high permittivity (about 40) of bismuth oxide, and also its ability to form a number of compounds of elevated permittivity by reaction with the barium titanate (e.g. $Ba_2Bi_4Ti_5O_{18}$). Bismuth oxide also promoted sintering, possibly because it readily forms glasses on dissolving small amounts of other oxides.

(vi) The upper electrode and dielectric could be co-fired or fired separately with little effect on the final properties of the capacitor.

The properties of the capacitors are summarized in Table 2.

Table 2

Performance of high-value capacitors

Capacitance: 10 000–70 000 pF/in²
tan δ: after ageing, 1–2%
Temperature variation of capacitance (20–90°C): maximum deviation 5%
Stability: typically −1% change in 500 hours at 100°C off-load (after initial settling period of 24 hours after manufacture)
Reproducibility: coefficients of variation 1·7–5·6%

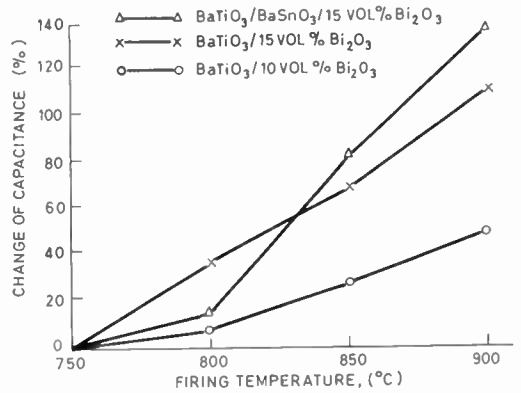


Fig. 4. Variation of capacitance with dielectric firing temperature.

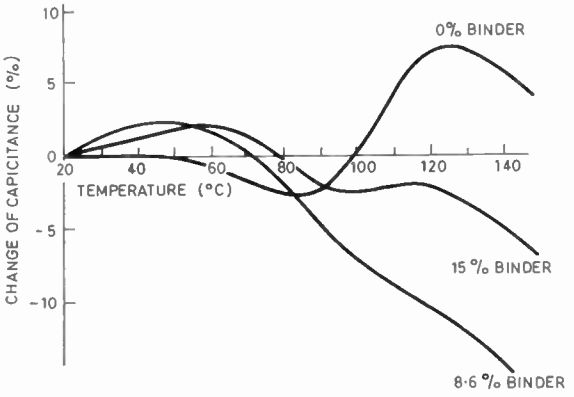


Fig. 5. Variation of capacitance with temperature.

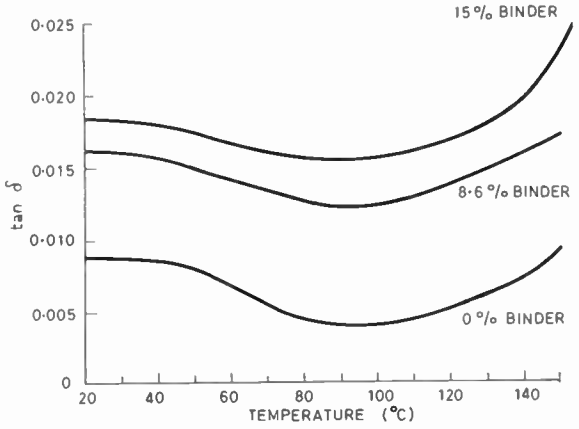


Fig. 6. Variation of tan δ with temperature.

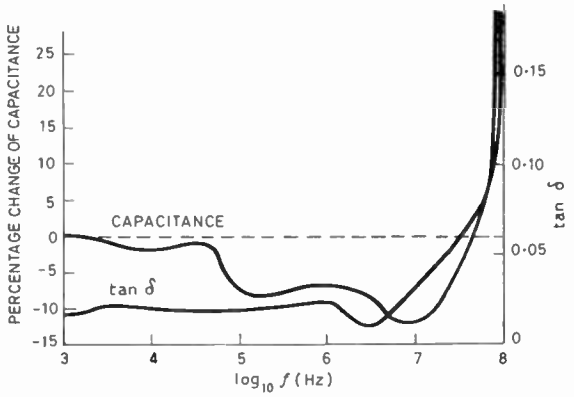


Fig. 7. Variation of capacitance and tan δ with frequency.

The capacitance value obtained depended on composition, dielectric firing temperature and electrode materials. Figure 4 shows the percentage change of capacitance with firing temperature for three different compositions. The variation is smooth, and the firing temperature has been used to control the final capacitance value. Tan δ was high immediately after manufacture (5–25%) but decreased rapidly to 2% or less. The capacitors are not especially stable, but as with the dielectric losses, the major changes occurred within the first 24 hours after manufacture. It is hoped that studies of the mechanisms of these ageing phenomena will yield more stable capacitors. Figure 5 shows the temperature variation of capacitance for compositions containing 0, 8·6 and 15 vol. per cent bismuth oxide and Fig. 6 shows the variation of tan δ with temperature for the same compositions. Figure 7 shows the variation of capacitance and tan δ with frequency for a capacitor containing 15 vol. per cent Bi_2O_3. The reproducibilities obtained are similar to those for capacitors with purely glassy dielectrics. This is surprising in that chemical reactions were taking place between the constituents of the dielectric during the firings whereas previously the dielectric remained inert. Further testing of the capacitors remains to be carried out.

4. Conclusions

It has been shown that thick-film capacitors can be produced with a high degree of reproducibility and with high yields. A wide range of capacitance values has been achieved using glassy or composite dielectrics. The dielectric losses obtained after an initial rapid ageing are similar to those occurring in the raw materials used for the dielectrics. The stability of electrical properties is not very good at present and further work is to be carried out to investigate the ageing phenomenon.

The investigation has so far been confined to a limited range of materials and processing conditions. However, further work on the use of other ferroelectric materials in the composite dielectrics, including those of the niobate type, is to be carried out.

The work described in this paper formed part of a Ministry of Defence contract on the use of non-conducting glazes in thick film circuits.

5. Acknowledgments

The author wishes to thank Mr. B. Walton for helpful advice on the work, and the authorities of A.S.W.E., Portsdown, and the Directors of Morganite Research and Development Ltd. for permission to publish this paper.

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Manuscript received by the Institution on 23rd February 1968. (Paper No. 1230/CC30.)

Conferences in 1969

Symposium on Position Measurement and Instrumentation

A two-day Symposium on 'Position Measurement and Instrumentation' is being organized by Plymouth College of Technology. The Symposium, which will take place on 14th and 15th January 1969 at the College, will be supported by an exhibition of equipment.

Further information may be obtained from Mr. R. T. Macdermott, Department of Electrical Engineering, College of Technology, Plymouth, Devon.

Computer Science and Technology

The Institution of Electrical Engineers, together with the I.E.R.E., the Institute of Mathematics and its Applications and the Institute of Physics and The Physical Society, is sponsoring a conference on 'Computer Science and Technology'. This is to be held at the University of Manchester Institute of Science and Technology from 30th June to 3rd July 1969.

The computer design problem can be represented as an interaction between new developments in technology and the requirements of the user. The conference will emphasize this relationship with sessions on the following topics:

Impact of high-level languages, etc.; store hierarchies: future requirements, engineering developments; multi-computer systems; requirements of particular applications, such as large scientific problems, information banks, multi-access, etc.; special purpose machines and systems; modern solutions of logic design problems: cellular arrays, l.s.i.; design automation; education of computer scientists and engineers; storage technology; display methods.

Contributions of up to 2500 words are invited. Full texts will be required by 24th February 1969, but intending authors are asked to submit a 250-word synopsis of their papers, without delay, to the Conference Secretariat, Institution of Electrical Engineers, Savoy Place, London, W.C.2.

Radio and Microwave Radiation Hazards

An International Symposium on 'Applications and Potential Hazards of Radio and Microwave Radiations' will be held at the new campus of the University of Surrey, Stag Hill, Guildford, on 2nd–3rd January 1969. The programme will include papers under the following headings:

Applications and hazards (radio communications, radar, food preparation and sterilization, print drying, medical, etc.);

Far and near electromagnetic fields (far fields under laboratory conditions, monitoring);

Biological effects of non-ionizing radiation;

Explosive hazards;

Discussion of hazard levels.

Further details and registration forms may be obtained from Dr. D. S. Allam, Department of Chemical Physics, University of Surrey, Stag Hill, Guildford.

Radio Engineering Overseas . . .

The following abstracts are taken from Commonwealth, European and Asian journals received by the Institution's Library. Abstracts of papers published in American journals are not included because they are available in many other publications. Members who wish to consult any of the papers quoted should apply to the Librarian giving full bibliographical details, i.e. title, author, journal and date, of the paper required. All papers are in the language of the country of origin of the journal unless otherwise stated. Translations cannot be supplied.

ION IMPLANTATION TECHNIQUES FOR SEMICONDUCTOR DEVICES

Ion implantation is becoming increasingly significant as an alternative process to conventional doping technologies. The potentialities and advantages of ion implantation as a technology for the fabrication of various semiconductor devices, particularly m.o.s. field-effect transistors, bipolar transistors and read-diodes, are discussed in a paper from the Institut für Technische Elektronik, Munich. A summary of theoretical fundamentals, which allows a description of the experimental impurity distribution profiles and the 'channelling' phenomenon is given. Radiation damage and its effect on the electrical characteristics of the ion-implanted device are discussed.

'Technology of semiconductor doping by ion implantation', I. Ruge and H. Müller, *Nachrichtentechnische Zeitschrift*, **21**, No. 10, pp. 625–30, October 1968.

TELEVISION INTERFERENCE MEASUREMENT

Although many data are available concerning random noise visibility in various television systems, no reference is made to interpretation of the results in terms of a particular television standard.

By assuming a linear summation of the noise visibility with the individual frequency component of the noise spectra, a Japanese paper studies the weighting function from the horizontal and vertical spatial spectra of television raster displaying random noise over a uniform background, and shows that the horizontal spectrum of such raster is similar to the video spectrum of input noise, but is converted to the spatial frequency scale and modified by the beam aperture response of the picture tube. The conversion factor of the video frequency to the spatial frequency is inversely proportional to the line frequency of the television system.

The vertical spectrum of the raster is composed of the line spectrum and the continuous noise spectrum. The envelope of the continuous noise spectrum has no connection with the input noise spectrum or with the television standard, but it is similar to the beam aperture response.

The beam aperture response of the picture tube and the response of human vision to random noise will not change at the spatial frequency scale for various television systems. Consequently, the video weighting functions for random noise in different television standards must be identical except that its reference frequency is varied in proportion to line frequency.

The validity of the above analysis was supported by subjective experiments on the relative visibility of octave-band random noise in twelve television standards.

For the measurement of the random noise a new method is devised and described in the paper. First, a patch of uniform brightness from the picture was selected; the size of the patch may be as small as one hundredth of the whole picture area. Then, the waveform of this sample was displayed at line or field sweep on a wideband oscilloscope sandwiched between the adjustable reference noises to compare the two noise powers.

Since brightness and quasi-peak-to-peak amplitude of the two displayed waveforms are compared simultaneously, the matching of the two noise patterns is fairly simple and reasonably accurate (about 0·5 dB). The adjusted level of the reference noise indicates the noise power in the picture signal in the selected small area.

The instrument developed is a convenient means to measure the noise level of an individual head of a four-headed television tape-recorder, as a function of the signal level. It is claimed that the present instrument's ability to measure a very small sample area is a big advantage over conventional methods.

'The visibility of monochrome television random interferences and its measurement', Y. Yamaguchi, *NHK Technical Monograph* (Japan Broadcasting Corporation), No. 11, pp. 3-19, February 1968.

PHOTOMULTIPLIER REVIEW

The photomultiplier is a particularly useful instrument for the study of weak or rapidly occurring effects in which light is produced, and it has proved indispensable for many investigations in the field of nuclear physics. The improvement of this device during the last twenty years has been accompanied by the development of a great diversity of types to suit the various different applications.

After a description of the general principles underlying the design of photomultipliers and their characteristics, a paper from the Laboratoires d'Electronique et de Physique Appliqueé Company at Limeil-Brévannes in France, examines the statistical effects which limit the performance of photomultipliers, in relation to the introduction of noise and speed of response. The study of these effects gives a better understanding of the relations existing between the various parameters and leads to an overall optimization of performance. Thus, the appropriate use of high electric fields which give a high speed of response but which tend to increase the dark current, has resulted in a pulse response of nearly 1 ns in the fastest photomultipliers, and a transit-time fluctuation of nearly 0·1 ns. The paper gives a description of heterodyne detection of modulated light, and the concluding section indicates the probable trends of future development.

'Design and characteristics of present-day photomultipliers', G. Pietri and J. Nussli, *Philips Technical Review*, **29**, No. 8/9, pp. 267–87, 1968.

SUBJECT INDEX

Papers and major articles are denoted by printing the page numbers in bold type

INDEX OF PERSONS

Names of authors of papers published in the volume are indicated by bold numerals for the page reference.

Authors of papers which are given in abstract form are denoted by A

Biographical references are denoted by B Contributors to discussions are indicated by D

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Canadian Aeronautics and Space Journal

Electronics and Communications in Japan (English language edition of *Denki Tsushin Gakkai Zasshi*)

Fujitsu Scientific and Technical Journal (Japan)

NHK Technical Monograph (Japan)

Nachrichtentechnische Zeitschrift (Germany)

L'Onde Electrique (France)

Philips Technical Review (Holland)

Proceedings of the Institution of Radio and Electronics Engineers, Australia

Radio Engineering and Electronic Physics (English language edition of *Radiotekhnika i Elektronika*) (U.S.S.R.)

Slaboproudý Obzor (Czechoslovakia)

Telecommunications and Radio Engineering (English language edition of *Elektrosvyaz* and *Radiotekhnika*) (U.S.S.R.)