

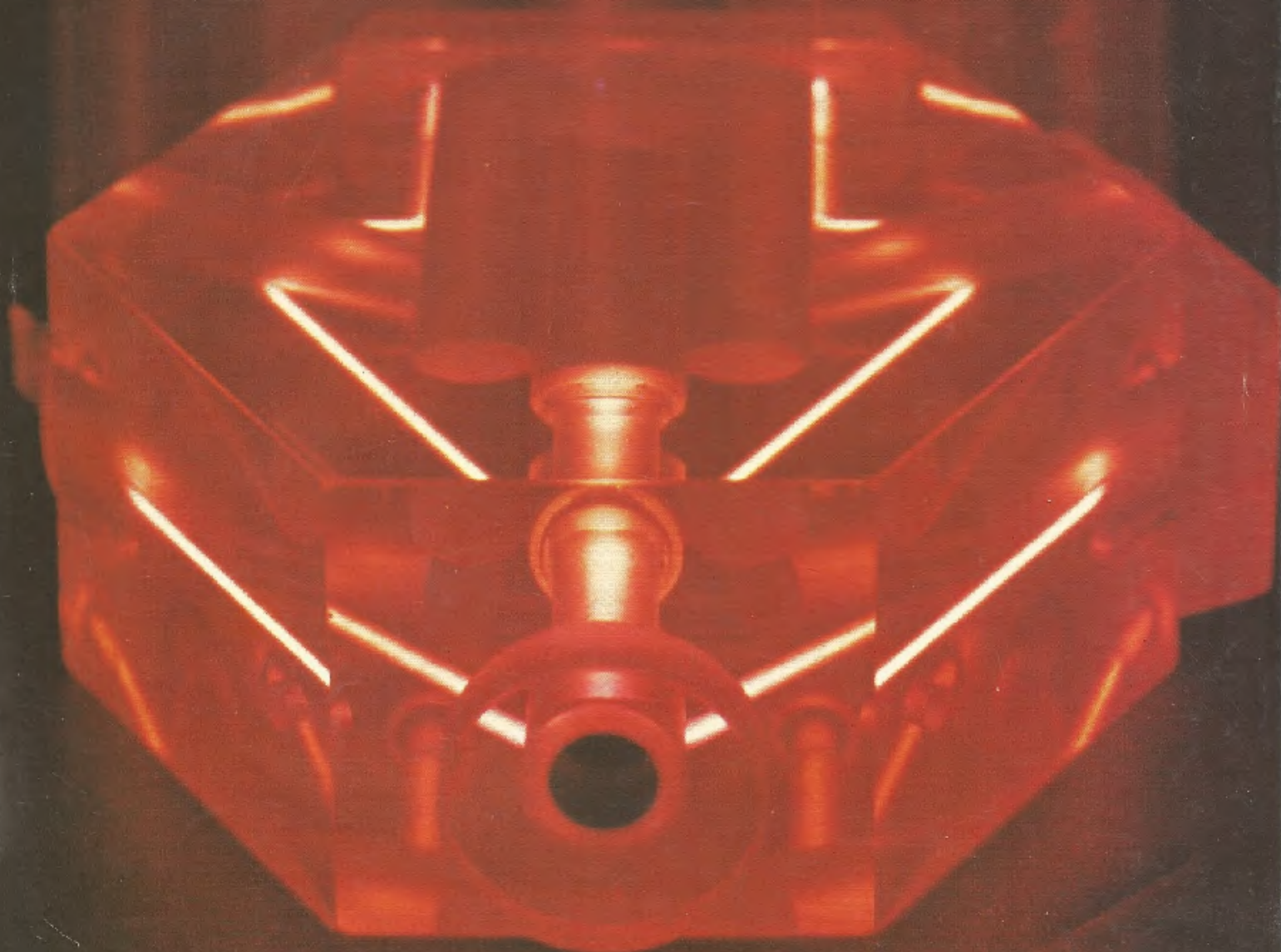
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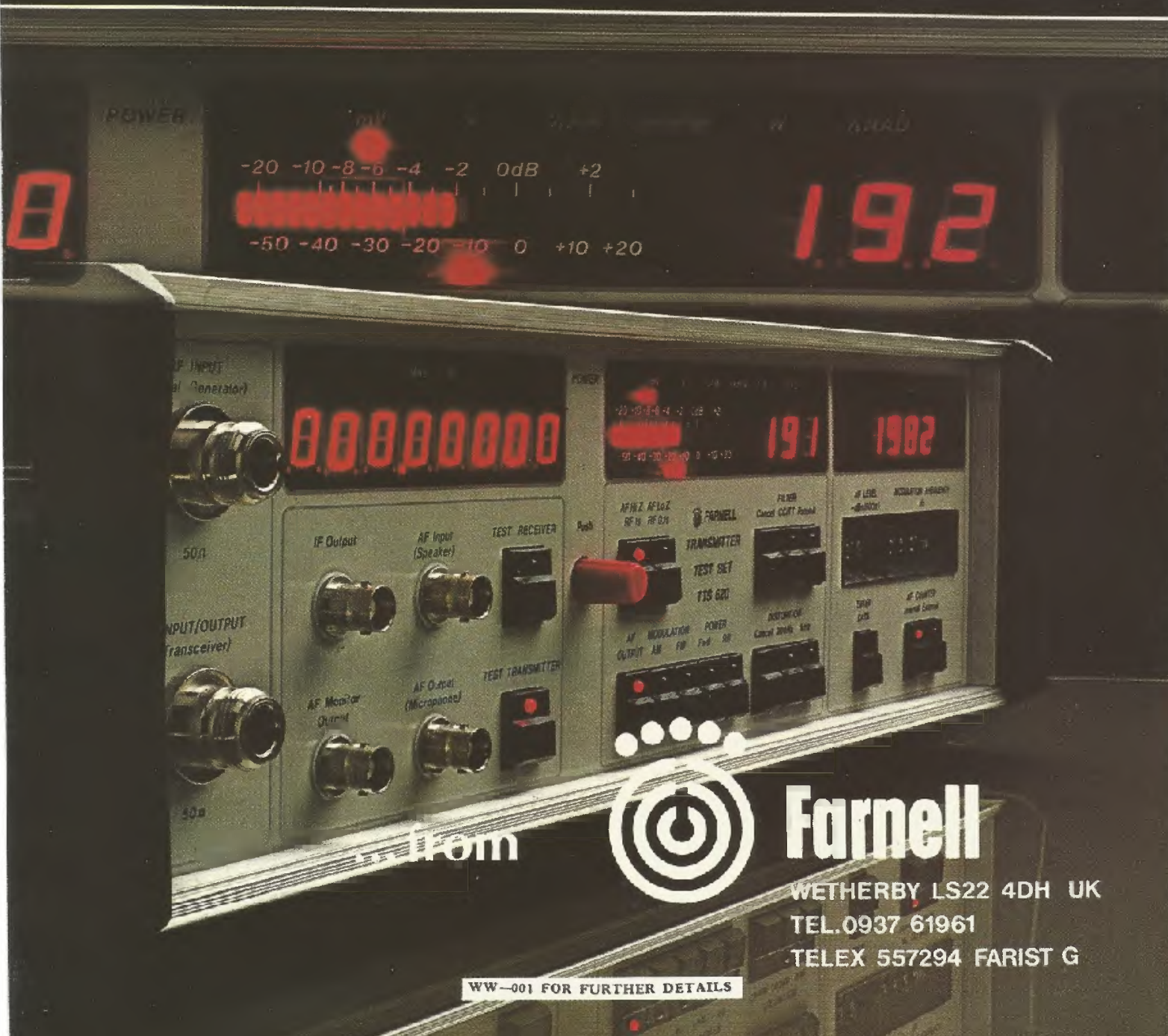
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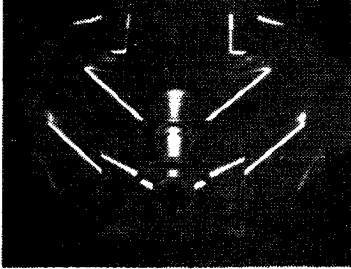
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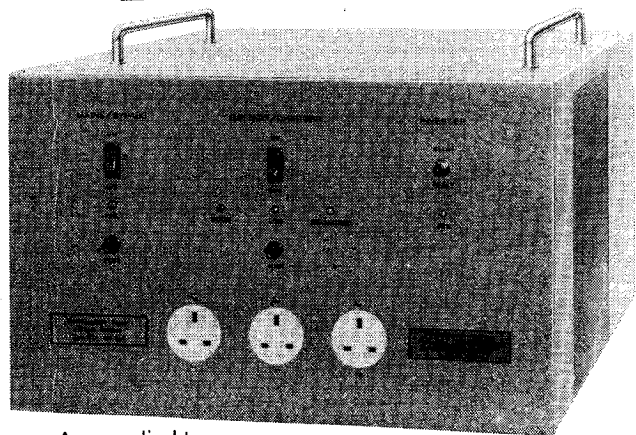
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## I.T. and M.I.S.S.

One of the aims of Information Technology Year and the Microelectronics Education Programme is to involve schoolchildren in the use of microcomputers and related electronic devices. There are the M.E.P., the Micros in Schools Scheme, exhibitions and events throughout the year and beyond. It is, perhaps, fortunate that Mr Callaghan happened to be watching television on the evening the programme "Now the Chips are Down" was broadcast and was spurred into action then, or we would probably find the propaganda even more frenetic than that now being put out by the energetic Mr Baker, the prophet of IT.

Information Technology is a curiously diffuse name for a Year. The official definition, "the acquisition, processing, storage, dissemination and use of vocal, pictorial, textual and numerical information by a microelectronics-based combination of computing and telecommunications" appears to encompass most of the activities of the average person, except eating and one or two other processes, although the use of a computer is not often considered essential to the more basic of these.

So far as its involvement of schoolchildren is concerned, the publicity is decidedly shrill, the Minister's aim being to have a computer in every secondary school by the end of the year and even to think about providing them for primary schools.

There can be no argument that young people must be aware of computers and how to use them, but it does seem possible that the present blaze of publicity tends to obscure the point that computers are a means, not an end. There is also the question of how the micros are to be used in schools.

According to the fifth edition of the Concise Oxford Dictionary (now, admittedly, modified), a computer is "a calculator — an electronic calculating machine" — an unfortunate description, taken too literally by at least some of those responsible for introducing youngsters to

computing, with the result that the school micro is often given to the senior maths teacher to guard with his life, presumably on the grounds that computers are electronically mathematical and possess no relevance to any other subject.

In other schools, the computer is treated as a kind of totem, and the pupils are taught "Computer Studies". As a subject, computing (meaning programming) is a singularly empty one, unless the pupil learning it intends to become a programmer. A computer is an aid to the process in which it is used — in this instance, learning — and an element of transparency to the user rather than an obscuring of the subject by undue attention to the computer must be the aim.

Clearly, an overnight transformation, after which every teacher would be using a micro as to the manner born, is hardly feasible. But, until the school micro (or one of its terminals or even a micro owned by a pupil or teacher) can be used naturally, as is a dictionary or pocket calculator or a video recorder, it will dominate the learning process. Utmost priority should be given to teachers from all disciplines, from home economics to athletics, to use the computer as an aid, rather than as a distraction, so that pupils who are not to specialize in science or engineering can see that it is of advantage to them to be at ease with computers, but no more than that.

The Inner London Education Authority is aware of these problems and is educating teachers in the use of computers so that, even though there may be only one micro or terminal in the classroom, the pupils will learn the place of a computer by, to use ILEA's word, "osmosis". However, there is evidence aplenty that education authorities in other areas are either hypnotized or revolted by the new equipment and, accordingly, either enshrine it or pass it to the school computer fanatic to impress people with.

In short, a computer is a useful tool, but that is all it is: it can help or it can dangerously hinder learning, and only the education of teachers in its natural use as an aid can decide which.

# DIGITAL FREQUENCY STABILIZATION OF A V.F.O.

Using a single crystal, the unit stabilizes the output of a variable-frequency oscillator at a large number of points by means of a counting technique. This article traces the development of the design and points out further avenues to explore

by W. Trapman, jr.

Most radio receivers and transmitters use at least one variable oscillator, coupled with the turning dial. Such an oscillator, usually called a v.f.o., must be easily tuned, exhibit high frequency stability and provide a pure sinusoidal output. For s.s.b. communication, the stability requirement cannot be met with LC oscillators, at least not in the higher h.f. bands or the v.h.f. frequencies. Use is often made of a mixing scheme, the variable oscillator running at a lower frequency, but purity of output and simplicity suffer with this method. Ease of tuning has always been the hall-mark of good communication receivers, leading to the familiar looks and appreciable cost of a very long tuning dial, with very fine divisions, coupled to the tuning capacitor by means of slip-free reduction gear without backlash.

Of course, a digitally-set frequency is very useful in a test-oscillator, but useless when one wants to tune in with the 'handwheel'.

## A simple stabilizer

Proposals have therefore been made to accomplish the old-fashioned continuous tuning while stabilizing the generated frequency at discrete spots. A simple method, now well known to amateurs, is given in Fig. 1. Since we are not interested in displaying the frequency digitally, only the first decade from the usual chain of counters is needed and its output used to correct the v.f.o. frequency.

To get a good mental picture of what happens, consider an example. The measuring period is exactly one second, the v.f.o. frequency is about 5 MHz, say, 5,123,456.78 . . Hz. The counter, being reset before the measuring time starts, contains after one second a 6 or 7. Because the digital output is taken from the fourth flipflop, a 1 only results when the counter contains an 8 or a 9, all other numbers giving a 0 at this point. The 1 may be regarded as the 'too high' signal, the 0 standing for 'too low'. This digit is stored in a buffer, so the counter can be reset and a new measurement initiated. A large time-constant smoothes the control signal from the buffer to the Varicap v.f.o. In the working system, the frequency of the oscillator is kept around 5,123,457/8 MHz and wobbles around this value. The next points for stabilization are 5,123,467/8 when tuning upwards and 5,123,447/8 when going downwards. Any drift of the v.f.o. is taken care of by changing the ideal equal number of ones and zeros to some

other proportion, for instance five ones against four zeros in a sequence like 01010110101, etc. (To say *any* drift is compensated for is fine, so long as it is taken to mean 'any small drift'. A very bad oscillator equipped with the stabilizer will not 'creep' but 'jump'. It is a very simple system, compared with other possibilities.

Besides a crystal-controlled (one-second interval) time-base, few i.cs are required and its elegant simplicity appeals to constructors.

There are drawbacks, however, all connected with the long measuring time: to get a reasonably smoothed control signal, the integrating time-constant has to be very large. A further point to think about is the delay in the system — even if the large RC product could be avoided, the information about the frequency becomes available every second and this is a somewhat elusive way of saying that some of it is almost one second old. The system just described needs at least several seconds to stabilize after the tuning knob is touched.

So, the first thing one tries to do is to shorten the measuring time to 0.1s. This is

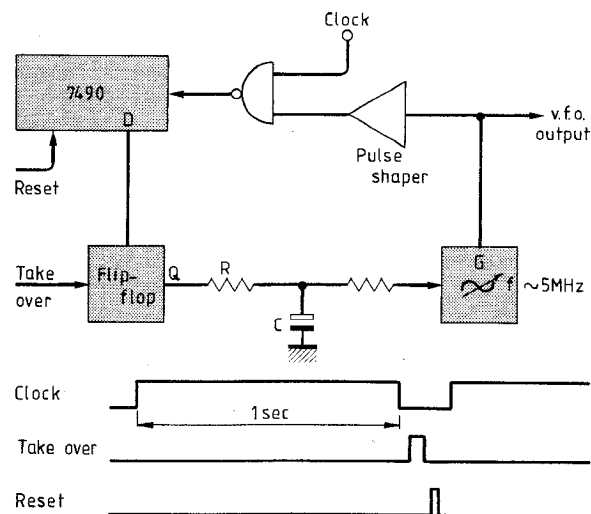


Fig. 1. Simple frequency-stabilized v.f.o.. When crystal-derived one-second period ends, 'high' or 'low' information from the decade counter is stored in the flip flop until next measuring period is completed. Clock and logic to provide the timing and controlling pulses not shown. R and C give large time constant.

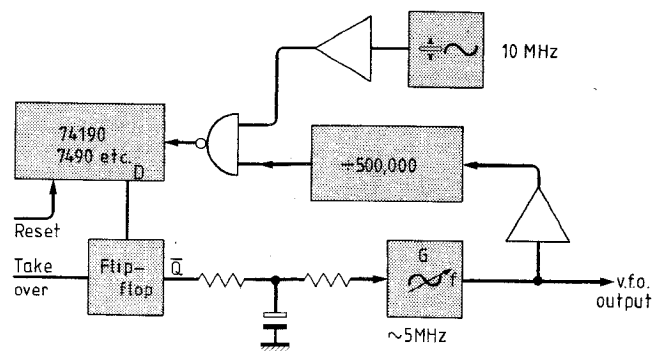
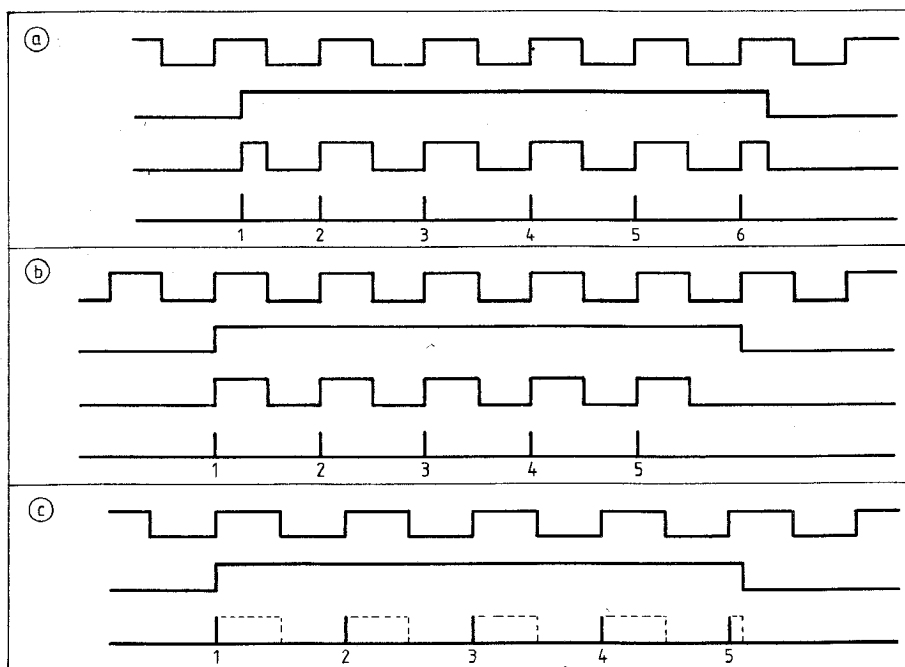


Fig. 2. Connecting high-frequency clock directly to gate and dividing v.f.o. output down gives a varying distance between successive stabilized frequencies on the dial. Because high-frequency crystal oscillators give no problems, resolution and stability can be high. Integrator is now connected to  $\bar{Q}$  on storage flip flop. Speed of logic elements forms limit for higher clock frequencies.



**Fig. 3.** (a) Shows 5 Hz square wave giving six positive going slopes per second, seen as pulses by the counter. In (b) only five pulses are seen. With some regularity this situation may alternate or not with (a). All depends on the relative position of the two waveforms. (c) shows that even an input frequency of 4.1 Hz gives five pulses to counter.

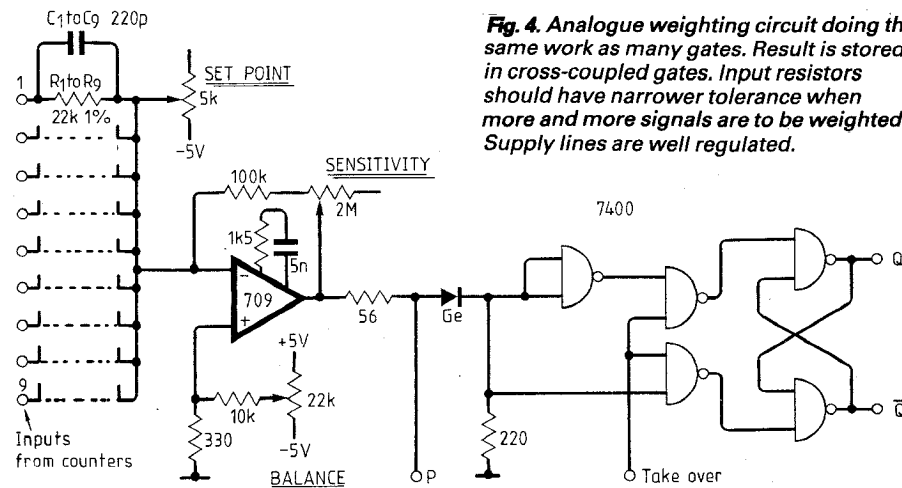
not a good idea, however, because the digit now contained in the buffer store represents not Hertz but tens of Hertz. In our example, with an initial frequency of 5,123,456.789... Hz, the counter contains that five and the feedback will arrange to make it alternate between 7 and 8 as before. The next higher stabilization (centre) point will be 5,12357/8, which is no less than 100 Hz from the previous one. The resolution of measurement is ten times reduced and the 'ripple' on the v.f.o. frequency is the same factor enlarged. The integrator time-constant can be ten times smaller now and the speed of response is subjectively very much improved — the only benefit of the change in measuring time.

The problem still remains: how to improve the resolution without lengthening the time for each measurement. When discussing this point with friends (one of them the prototype of *Homo digitalis*) one answer came up again and again: raise the frequency, so that the relative accuracy remains high enough when you shorten the gate time. In theory this is a way-out, because the high and stabilized frequency of, say, 51 MHz is divided by ten to get our original 5.1 MHz and the frequency variations are divided too. In practice, if you can build an oscillator that does not drift 10 Hz in 0.1 second at 50 MHz, frequency stabilization is probably not necessary. This approach did not seem attractive. Instead I pondered for some time, wondering whether it is at all possible to measure a frequency with an accuracy of 1 Hz in less than a second.

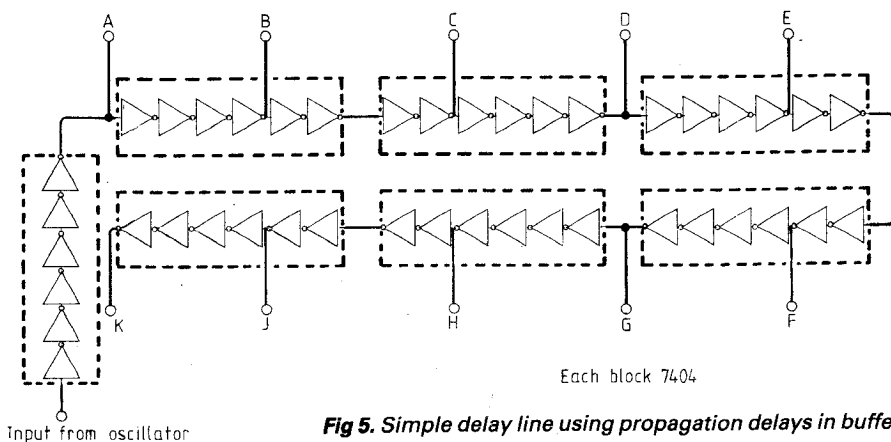
### Period counting

Just to be complete, one may recall the 'period counting' method of measuring low frequencies. When the rôles of the clock and the unknown frequency in a

frequency counter are reversed the unknown period is measured in units of the clock period and this takes only one period of the unknown frequency. If the unknown is about 5 MHz we could count off 500 000 periods in about 0.1 second, during which time the gate would be open. The single decade connected to its output would receive the clock signal, let us say 10



**Fig. 4.** Analogue weighting circuit doing the same work as many gates. Result is stored in cross-coupled gates. Input resistors should have narrower tolerance when more and more signals are to be weighted. Supply lines are well regulated.



**Fig. 5.** Simple delay line using propagation delays in buffers.

MHz. The resolution is still plus or minus one pulse in (about) a million and the grid of stabilization frequencies is now nonlinear: the distance between grid points at 5 MHz is 50 Hz. This is twice as good as the 100 Hz grid obtained with 0.1 second measuring time when counting the frequency direct and solely due to the clock frequency being twice as high as the v.f.o. frequency: a block diagram is given in Fig. 2. This is a good set-up when high-speed logic is used and the clock frequency can be raised to 20 or preferably 50 MHz (no prescaling; the gate and the counter following it must discriminate between those fast pulses).

To conclude the period-counting line of thought, the change of the distance between stable points over the dial is often not important. The ratio of the divider between oscillator and gate might well be a power of 2. Frequencies like  $f/2$ ,  $f/4$  are then available, all stabilized.

### Counting reviewed

The above stabilizations work well, but there is an extra irregularity not yet described, which is caused by the counting process itself. The specifications of commercial counters usually give the measurement error as  $\pm 1$  count + time base error. The time base is not important for this discussion: the reference crystal oscillator drifts a little, but presents no problem. The real problem is with the last digit of the counter, which in successive counts (if it were provided with a display) would show two values — it would 'jitter'. The stabilizing counter does the same thing,

even when the incoming frequency is perfectly stable since there is no phase relationship between the reference oscillator and the v.f.o. This is most disturbing and leads to noise on the correcting voltage to the oscillator.

To get a clear picture I drew a few pulses on graph paper, as in Fig. 3, which represents a 5 Hz signal as it appears before and after the gate of a frequency counter. The flip-flops in the counter toggle on the positive-going slope. When a window of exactly one second moves over the 5 Hz pulse train, we see immediately what happens: half a pulse has just the same positive-going slope, which is what is counted,

when the two waveforms glide past each other. Only when the situation is exactly stable (no gliding) do we get consistent answers from the counting process. Figure 3 (c) shows that stretching the pulses out (by lowering the frequency to 4.5 Hz) does not produce a different result; even 4.1 Hz does not make the fifth pulse 'fall out of the window'.

The only way to make this one-pulse ambiguity less important is to count more pulses, for instance by counting during ten seconds or by making ten, separate, one-second counts and averaging the answers. The last method was used very often when counters had no switch position for

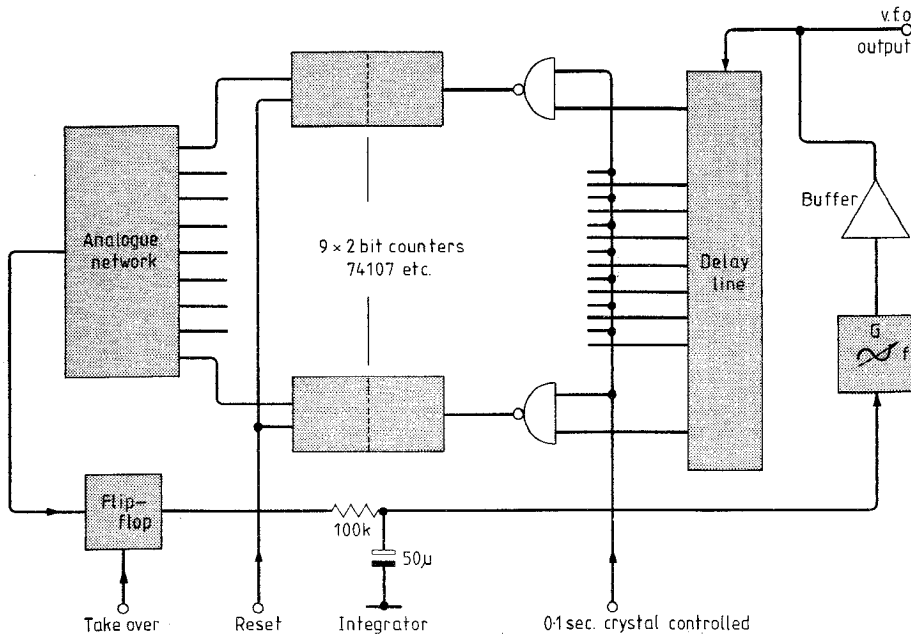


Fig. 6. Block diagram of frequency-stabilized v.f.o. Each of odd number of counters gets a slightly different 'cut' from continuous pulse train from the oscillator. Counters work simultaneously.

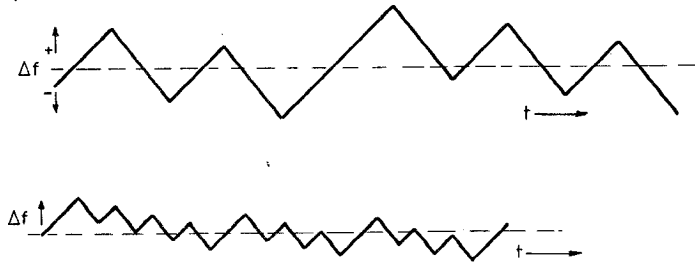


Fig. 7. Frequency variation of output is reduced when corrections come faster, drift being equal in both cases. Even a three times faster correction rate is a worthwhile improvement.

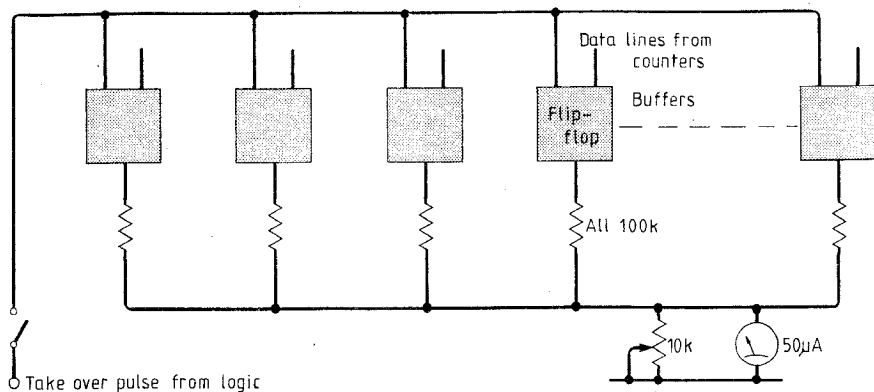


Fig. 8. Adding digital information without clipping is much better. Digital store is 'frozen' when switch is open.

'multiple frequency' and the resolution was just one decimal place too low.

### A new method

All this may be interesting but does not look very promising for our v.f.o., until a new idea is brought in. It is not necessary to do the individual one-second measurements one by one: the measuring times may overlap. The aim is to average out the one-pulse variation and obtain the high resolution that may be expected from a long counting time, but before placing endless rows of decades on the breadboard it might well be asked why one should use four flip-flops to get a single 0 to 1 out of them? Well, it depends largely on the stability of the oscillator when the controlling loop is disabled, and on the nature and magnitude of any impulsive noise that might enter the system. With a simple four-bit counter there is plenty of margin on both sides of the dividing line between 7 and 8, but with a decade counter one side is limited; two pulses extra make a zero from that 8 to give a 'correction' in the wrong direction.

Because the decade on the breadboard worked well once the starting time was over, I decided that two-bit counters were all I needed. There were times I wished I had used the SN 7493 four-bit counter, but some of the problems turned out to be hardware-oriented and not so much a system fault.

### Voting logic

The majority-vote is taken by the analogue circuit of Fig. 4, which works easily with 21 inputs — an odd number to get a majority in all situations. The input resistors are of the carbon-film type, selected for close tolerances for a larger batch with the circuit of Fig. 4 itself (without R<sub>1</sub>-R<sub>9</sub>). A voltmeter at point P indicates output voltage during the selection; the setpoint and sensitivity potentiometers are partly incorporated for this occasion. Even this circuit is a simplification from the breadboard circuit, where the digital outputs of the counters were stored by 'buffer' flip-flops. These buffers are not required if a reasonable amount of time is available for the voltage at P to take on the proper value. If take over and reset must take place in 1 or 2 µs, it becomes necessary to use the buffer store.

Counting in the parallel, but delayed, counting operation, it is immaterial

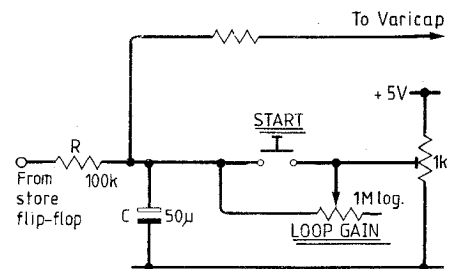


Fig. 9. Push button is pressed 10 seconds after power is switched on, reducing loop gain while charging capacitor to average value. H.f. decoupling of control line not shown.