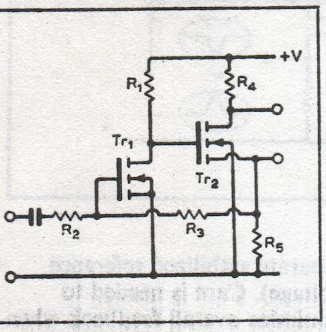
wireless world circard

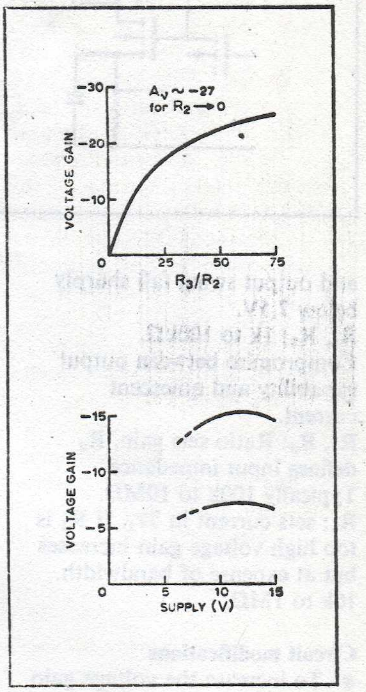
D.C. feedback pair



Typical performance
IC CD4007AE
2 n-channel devices
Supply +10V
R_1 1.2MΩ
R_2 470kΩ
R_3 5.6MΩ
R_4 10kΩ
R_5 4.7kΩ
C 100nF
Voltage gain output 1 −10.7
output 2 −21.8

Circuit description
This classic form of circuit has proved so flexible in bipolar designs that it is worthwhile to consider its behaviour in m.o.s. form. It can be constructed using either n-channel or p-channel devices, and complementary forms are also possible. If R_1 is large, the current in Tr_1 is low and it will require a V_{GS} little more than its threshold voltage i.e. around 2V. Input current is negligible and hence the p.d. across R_3 is zero. This defines the p.d. across R_5 and the corresponding current in Tr_2 and R_4. This in turn fixes the V_{GS} of Tr_2 and the drain potential of Tr_1 ($V_{GS1}+V_{GS2}$). Provided the supply voltage is much greater than this value the current in R_1 is well-defined. For a.c. signals the gate of Tr_1 is an imperfect virtual earth—the open-loop voltage gain is around −20 to −40 and so closed-loop gains of −5 to −10 can be defined with moderate accuracy. The input impedance is then $\sim R_2$ and as R_3 and R_2 can be very large, loading of any preceding stage is small. Outputs from source and drain of Tr_2 are anti-phase and can be equal in magnitude or in any desired ratio, since the currents in R_4, R_5 are almost identical (differing only due to the small current in R_3). The frequency response is controlled by shunt capacitance across R_1 (internal plus strays).

Component changes
IC: Access needed to individual devices—hence CD4007, CD3600 or equivalents.
Supply: +5V to +15V. Gain



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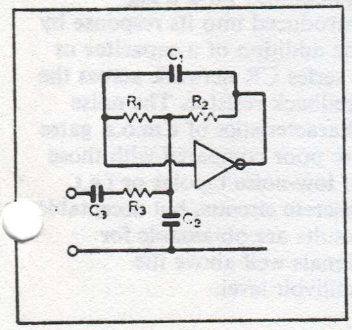
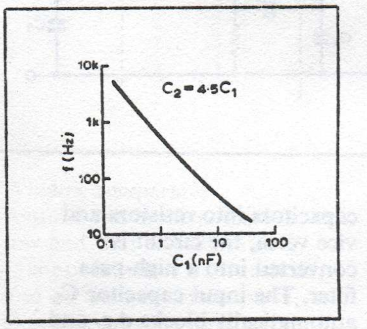
Low-pass/high-pass filters

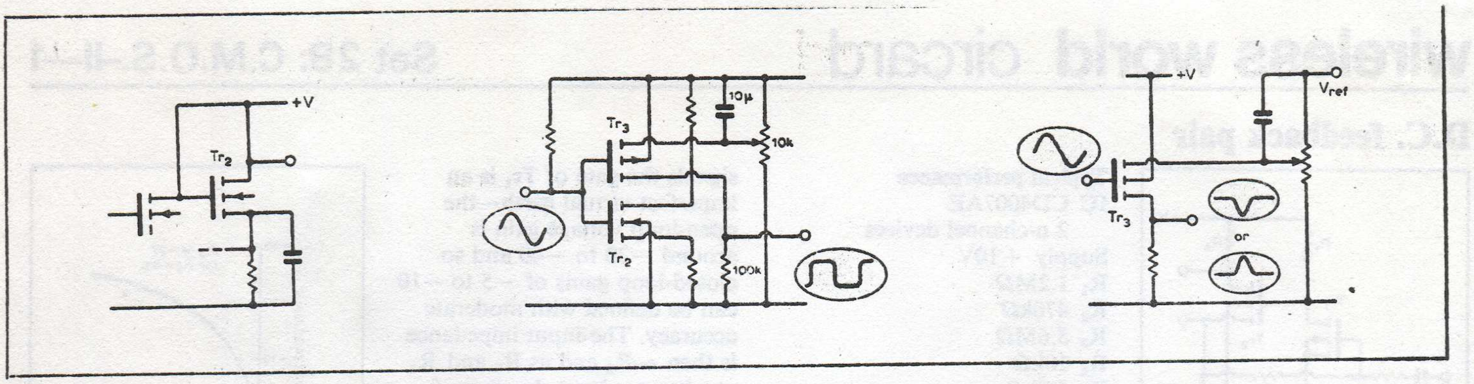


Typical performance
IC $\frac{1}{4}\times$CD4001AE
Quad NOR gates
Supply +10V
C_1 1nF
C_2 4.7nF
C_3 100nF
R_1, R_2, R_3 100kΩ
Cut off frequency 750Hz
Q 0.7
i.e. Butterworth response low-pass filter.



Theoretical relationships
$f_0=1/2\pi\sqrt{C_1C_2R^2}$
where $R_1=R_2=R_3=R$ and f_0 is the cut-off frequency of the resulting low-pass characteristic. Damping factor ζ is related to Q by $Q=1/2\zeta$ and Q is controlled by the ratio of C_2 to C_1. Accurate control is not possible because of low amplifier gain but $C_2=C_1\times 9Q^2$ i.e. for $Q\sim 1/\sqrt{2}$, $C_2\sim 4.5C_1$.

Circuit description
Low-pass filters normally have a flat response up to a given frequency, a rapid fall-off at much higher frequencies, and very little if any increase in amplitude during the transition from the pass-band to the stop-band. This corresponds to damping-factors of the order of unity and Q-factors which are normally equal to or less than one ($Q=1/\sqrt{2}$ is the condition for one standard filter the Butterworth type). Such a characteristic places no great demands on the amplifier used to implement it unless the accuracy required is high as in multi-order filters. For routine attenuation of hum, noise, and other unwanted signals a voltage gain of −20 to −100 is more than adequate, and c.m.o.s. inverters can be used. In the circuit shown, C_3 is a large value coupling capacitor that allows the d.c. feedback via R_1, R_2 to provide self-bias for the inverter. It rolls off the response at low frequencies but can easily be set to a value that does not affect the normal pass-band. By keeping the resistors constant, the cut-off frequency is inverse to the product C_1C_2, while the Q is controlled by the ratio C_2/C_1. The very high impedance of the c.m.o.s. input makes it possible to use very large values for R_1, R_2 and hence drop the cut-off frequency below, say, 50Hz while using

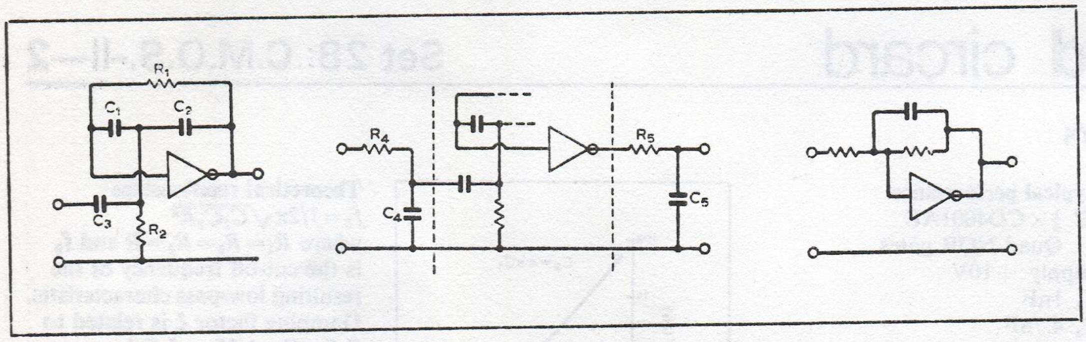


and output swing fall sharply below 7.5V.
R_4, R_5: 1k to 100kΩ. Compromise between output capability and quiescent current.
R_2, R_3: Ratio sets gain, R_2 defines input impedance. Typically 100k to 10MΩ.
R_1: sets current in Tr_1. If R_1 is too high voltage gain increases but at expense of bandwidth. 10k to 1MΩ.

Circuit modifications

- To increase the voltage gain, the source of Tr_2 may be decoupled to ground, removing the a.c. negative feedback. Stray coupling between output and input can cause instability because of the high input impedance. Frequency dependent networks may be used in parallel with or replace resistors in the system to produce a controlled frequency response provided d.c. feedback path remains.
- If the complementary transistor to Tr_2 has its source taken to a decoupled potential divider across the supply, then its output current changes sharply at a particular level of the a.c. signal. Biasing it as shown can produce an approximate square wave without disturbing the normal operation of the amplifier or requiring an extra stage. Because the gate voltage of Tr_2 is defined in potential with respect to the ground line, the squaring action can be made almost independent of supply by deriving the voltage from (or replacing it by a separate stabilized reference voltage). Care is needed to minimize overall feedback when switching stages are operated close to a.c. amplifiers. If the reference voltage is raised or lowered the output transitions occur near to the negative or positive peaks of the input giving pulsed outputs as shown.

Cross references
Set 27, cards 3, 4, 5, 6
Set 20, card 10
Set 12, cards 7, 9



small capacitors. The output has a d.c. content that would make a coupling capacitor necessary in most cases.

Component changes
C_1: 47p to 10µF
C_2: Typically 4 to 5×C_1 or can be varied to change the Q.
R_1, R_2, R_3: 10k to 10MΩ.
C_3: Must be large enough to avoid attenuating lowest frequency signal. 100n to 10µF.
IC: Any c.m.o.s. inverter, gate.
Supply: +5V to +15V

Circuit modifications

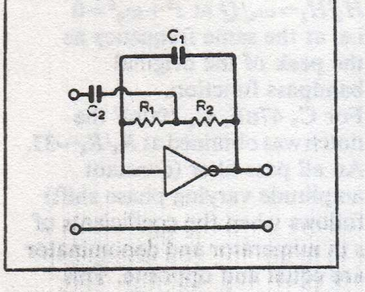
- By transposing all the capacitors into resistors and vice versa, the circuit is converted into a high-pass filter. The input capacitor C_3 automatically blocks d.c. and this reduced the component count by one. If a high Q is required, then the ratio R_1/R_2 has to be increased. For $C_1=C_2=C_3=C$, the cut-off frequency is $f=1/2\pi\sqrt{R_1R_2C^2}$ $=1/2\pi C\sqrt{R_1R_2}$ The value of Q is given by $R_1/R_2=4Q^2$ for an amplifier with infinite gain. In practice it would be difficult to obtain a Q of more than 5 while the usual range of Q-values needed in high-pass filters (say 0.5 to 1) is achieved with reasonable accuracy. Higher order filters can be constructed by cascading individual second-order filters. The presence of C_3 at the input simplifies the coupling because each inverter is then self-biasing. It is unlikely that high-order filters would be sufficiently accurate and independent of supply etc to be worth designing by this technique.
- If precise control of the form of filter characteristics is not needed (i.e. Butterworth, Bessel etc) the order of the filter can be increased by adding separate RC sections at input and/or output.
- Any separate inverter in a system may have a lag introduced into its response by the addition of a capacitor or a series CR network across the feedback resistor. The noise characteristics of c.m.o.s. gates are poor compared with those of low-noise bipolar or f.e.t. discrete circuits, but acceptable results are obtainable for signals well above the millivolt level.

Further reading
Sedra, A. S., Generation and classification of single amplifier filters, *Circuit Theory and Applications*, vol. 2, 1974, pp. 51-67.

Cross references
Set 1, cards 4, 5
Set 16, card 9

Band-pass/notch filters

Band pass 1



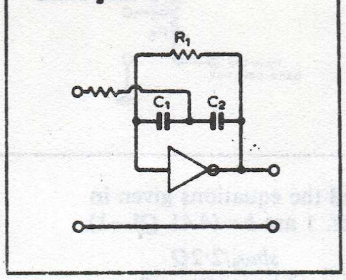
Circuit description

Band-pass filters commonly require differential input amplifiers or multiple amplifiers. This remains true if high Q is needed, particularly if sensitivity to gain and passive component changes is to be minimized. Where a low value of Q is sufficient then simple band-pass filters can be based on single inverting amplifiers. At very low frequencies, the impedance of $C_2 \to \infty$ and the gain $\to 0$. At very high frequencies the impedance of $C_1 \to 0$ and the gain→0. At some intermediate frequency, the gain has a maximum value. The theoretical centre-frequency is $1/2\pi \times \sqrt{R_1R_2C_1C_2}$ and commonly, $R_1 = R_2 = R$ giving $f = 1/2\pi R\sqrt{C_1C_2}$. Considerable departures from the predicted Q-values occur because of the low gain of the amplifier. The centre frequency lay within the tolerance range of the passive components in the samples tested. At the centre frequency, the output is anti-phase to the input. This leads to a simple means of obtaining a notch-characteristic as indicated over. The high values of resistors that can be used make it easy to obtain a very low-frequency band-pass characteristic, while on the high-frequency side operation to beyond 100kHz is possible.

Typical performance

IC ¼×CD4001
(quad NOR gates)
Supply +10V
C_1 100pF
C_2 10nF
R_1 R_2, 100kΩ
f_0 1490Hz
Q 2.5
(For an ideal inverter, $C_2/C_1 = 4Q^2$ but with the very limited gain the theoretical Q of 5 is reduced to 2.5, see Ref. 1.)

Band pass 2



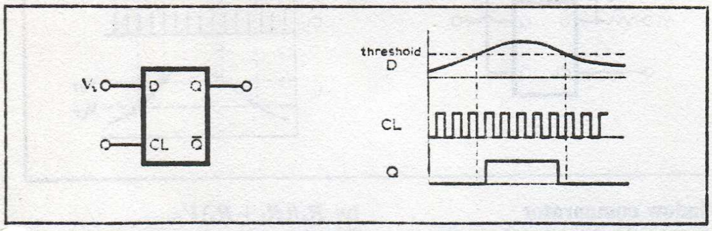
Typical performance

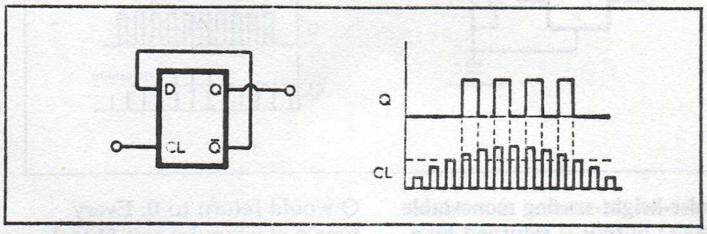
IC ¼×CD4001
(quad NOR gates)
Supply +10V
R_1 220kΩ
R_2 2.2kΩ
C_1 15nF
C_2 15nF
f_0 460Hz
Q 2.1
$f = 1/2\pi\sqrt{R_1R_2C_1C_2}$
& $4Q^2 = R_1/R_2$.
In practice $Q > 5$ difficult to achieve.

Alternative circuit

The second form of the band-pass filter has comparable performance, and no significant differences were observed. The input impedance will presumably differ from the

D-type analogue circuits-1





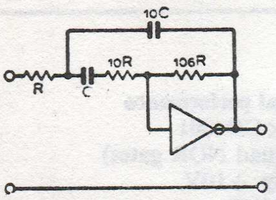
D.C. level sensing

The D-type flip-flop has a data input which responds to a 0 or 1 input by transferring these to the Q output when the device is clocked. The threshold between these two regions varies from device to device, but varies little with temperature. For moderate variations in supply voltage it is also a fixed fraction of that voltage and the transition between regions is sharp. If a varying d.c. voltage is applied to the data input, and the flip-flop is continually clocked, then each time the voltage passes through this threshold region, the output changes state on the next clock-pulse. The threshold remained between 44.7% and 45.0% of the supply voltage for V_s 4 to 7V and the effect of temperature was of the order 1mV K^{-1}. If the unknown voltage is derived from a common supply rail regulation would not be required since both it and the device threshold would vary together. The output is 1 for $V_D > V_T$ and 0 for $V_D < V_T$.

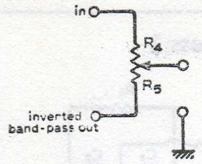
Pulse height detector

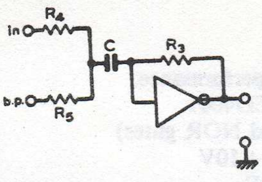
The flip-flop is set up as a ÷2 circuit by returning the data input to the Q output. For each normal clock pulse the Q output is thus set to the previous state held on the Q̄ output i.e. the state of Q (and hence of Q̄) is reversed. If the clock pulses fall below the threshold value of the C_L input they are ignored and the output retains its previous state. This threshold level is controlled by gates similar to those at the D input and hence the threshold level is of the same order —45/55% of the supply, but with the same well-defined characteristics for any given device. The output is a square wave of half the input frequency for $V_{CL} < V_T$ and either 0 or 1 for $V_{CL} > V_T$. A small amount of inherent hysteresis appears to exist in such applications as these. The input amplitude has to reverse itself by up to about 1% after effecting a change in the output in order to reverse that change.

Band pass 3



Notch/All pass filters





first circuit, but both impedances can be made high enough for differences to be unimportant.

Component changes

IC: Any c.m.o.s. inverter, buffer, gate.

Supply: +5 to +15V. At low voltages the available voltage gain is too far reduced by loading effects.

R_1, R_2: 10k to 10MΩ. Lower values possible if source impedance is low.

Circuit modifications

The third band-pass filter is based on that of Sallen & Key and the equations given in Ref. 1 are $b=(4.41\,Q^2-1)$.

$$T_V=\frac{s b\omega_0/2\cdot 2Q}{s^2+s\omega_0/Q+\omega_0^2}$$

where $s=j\omega$

Notch filters are often based on band pass networks, in which a bridge or other balancing system is arranged such that the output tends to zero at the centre-frequency of the band pass. In this case, taking the first circuit overleaf, the input and inverted output are applied to the ends of a potentiometer. As the potentiometer setting is varied, a point is reached where the two signals exactly cancel at the original centre frequency. The principle can be extended to obtain a low impedance output by applying the signals via two resistors to the summing junction of a second inverter as shown. The overall transfer function is then of the form

$$T_V=\frac{H_2 s}{s^2+s(\omega_0/Q)+\omega_0^2}-H$$

allowing for the inversion due to the second amplifier. ($H_1 \propto 1/R_4$, $H_2 \propto 1/R_5$)

$$T_V=\frac{H_2 s-H_1[s^2+s(\omega_0/Q)+\omega_0^2]}{s^2+s(\omega_0/Q)+\omega_0^2}$$

$$=-H_1\left[\frac{s^2+s\left(\frac{\omega_0}{Q}-\frac{H_2}{H_1}\right)+\omega_0^2}{s^2+s(\omega_0/Q)+\omega_0^2}\right]$$

For a notch characteristic, there must be a frequency at which the output goes to zero. This is achieved for $H_2/H_1=\omega_0/Q$ at $s^2+\omega_0^2=0$ i.e. at the same frequency as the peak of the original bandpass function.

For C_2 47nF, C_1 100pF the notch was obtained at $R_5/R_4\sim 33$. An all pass filter (constant amplitude varying phase shift) follows when the coefficients of s in numerator and denominator are equal and opposite. This implies $2\omega_0/Q=H_2/H_1$ and corresponds to $R_5/R_4\sim 16$.

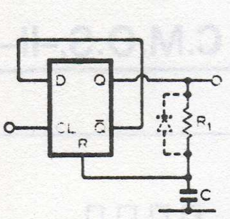
Further reading

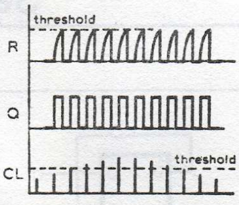
Sedra, A. S. Generation and classification of single amplifier filters, *Circuit Theory and Applications*, vol. 2, 1974, pp. 51-67.

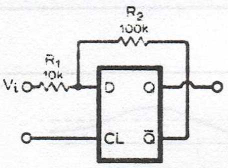
Cross references

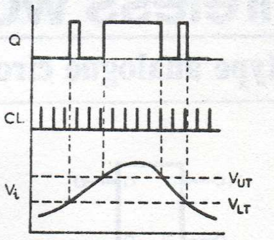
Set 1, card 8

Set 16, cards 7, 8









Pulse-height-sensing monostable

The Q output is returned by a short time-constant circuit composed of R_1C_1 to the re-set input. If the input pulse rate becomes too rapid, an additional diode across R_1 shortens the recovery time of the monostable and allows the output pulse-width to remain independent of pulse-rate. Provided the input pulses, applied to the clock input exceed the threshold then the circuit attempts to toggle. The rest state of the system must be $Q=0$, since for $Q=1$ the reset input would be activated after a short charging period and Q would return to 0. Every time a clock-pulse sets Q to 1, this is what happens, and Q remains on for the time it takes the reset input to reach its threshold value via the charging of C_1 through R_1.

There is one output pulse of defined height and width for every input pulse exceeding the threshold voltage. If a further clock pulse is received during the on-period, the output pulse is terminated. If this is not desired, the D input can be returned directly to logic 1 when such pulses are ignored.

Window comparator

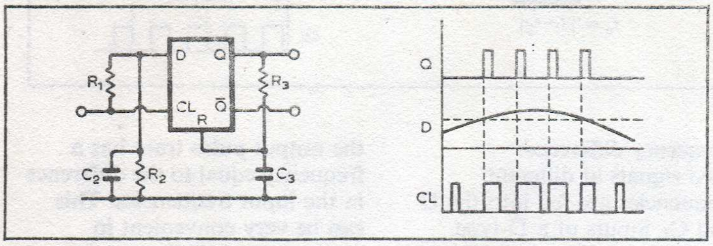
Assume the input voltage is low and that $R_2 \gg R_1$. The D input is below its threshold, and on the next clock pulse, Q is driven to (or held at) 0, and $\bar{Q}$ to 1. This change is insufficient to shift the D input above its threshold and Q stays permanently at 0. Conversely if V_i is high, Q is held permanently at 1. When V_i is close to the threshold, each transition of $\bar{Q}$ shifts the D input across the threshold and the circuit toggles. There are now two effective threshold points V_{LT} and V_{UT}, the lower and upper thresholds, separated by $R_1/(R_1+R_2)V_S$.

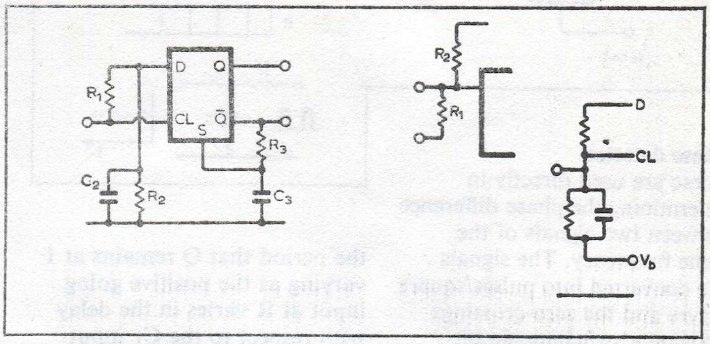
For $V_i < V_{LT}$ Q is 0.

For $V_i > V_{UT}$ Q is 1, and for $V_{UT} > V_i > V_{LT}$, Q toggles at $f/2$. For a steady clock rate (f constant) the output mark-space ratio is unity.

A moving-coil indicator at the Q output would read zero, $V_S/2$ and V_S respectively for V_i below between and above the thresholds. Alternatively a l.e.d. would be off, flashing at $f/2$ or permanently on for these three ranges of input volts (this would require a slow-speed clock if the flash rate is to be visible).

D-type analogue circuits-2

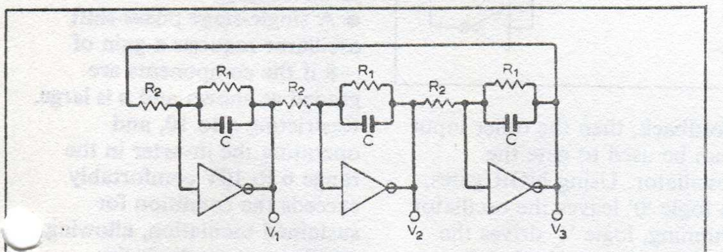




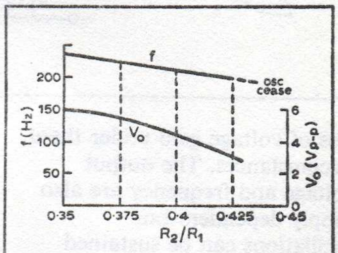
Mark-space detector
If the input pulse-train has a large mark-space ratio, its mean value may be $\approx 50\%$ of V_s, provided the input pulse height is equal to V_s. If the voltage at D is smoothed by C_2 across the potential-divider formed by R_1, R_2, the threshold will be exceeded and an output pulse-train is obtained. When the mark-space ratio falls below the critical level, the monostable relaxes into its quiescent state with $Q=0$. The circuit basically detects the mean level of the input pulse train and can be used to detect any of the separate variables that affect the area provided that all the others remain constant. Thus for height and frequency constant the circuit detects pulse-width, for height and pulse-width constant it detects a rise in frequency and so on. The pulse-height is well-defined if the previous stage is a c.m.o.s. gate/inverter.

Space-mark detector
The complementary nature of the circuit allows the reversal of the outputs, letting $\bar{Q}$ activate the set input. In each of these circuits the monostable period has to be less than the period of the incoming pulses. As shown, the output at $\bar{Q}$ remains low until the mean value on the D input falls below its threshold, when the $\bar{Q}$ output becomes a pulse train. To adjust the range of mark-space ratios that can be dealt with, a bias current can be provided from the supply or the CR network can be returned to a variable bias voltage. This would need to be supply proportional if using an unregulated supply for all other functions.

Three-phase oscillator

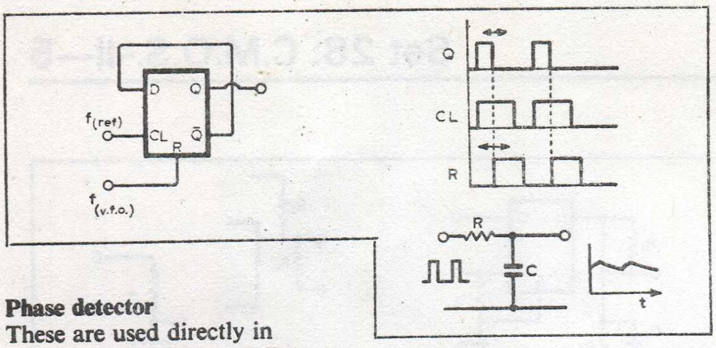


Typical performance
IC $\frac{3}{4}\times$CD4001AE
quad 2-input NOR gates
Supply +10V
R_1 100kΩ
R_2 40kΩ
C 15nF
f 213Hz
Amplitudes 3.6, 3.4, 3.5V pk-pk
Distortion 2.2%, 0.4%, 1.1%

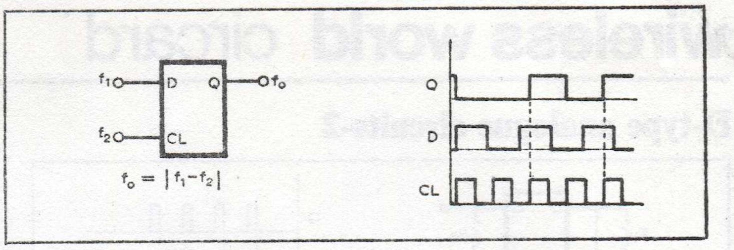


Circuit description
Each inverter has a high input impedance and an inverting voltage gain of magnitude <1. The CR network in the feedback path introduces a lagging response. If the system is to oscillate, the loop phase shift must be zero while the overall gain should just exceed unity. If the system is to be symmetrical then each stage must contribute the same phase shift and must separately have unity gain. If the inverter gain is large then with the three inversions, the sum of three equal phase shifts must equal 180° to meet the overall phase condition. This requires a 60° lag from each of the sections. To maintain the magnitude condition at unity, the magnitude of the impedance of R_1 in parallel with C must equal the resistance of R_2. This gives $R_2=R_1/2$ as the maintaining condition with $f=\sqrt{3}/2\pi CR_1$.
In the practical case the amplifiers have gains ranging from 10 to 50, inverting and with little phase-shift in the audio band. The inherent matching of these inverters because they are formed on a common chip means that provided the resistors R_2 are reduced by the same amount to accommodate this finite gain, then the phase relationships between the outputs are maintained. Non-linearity of the gain provides a coarse form of amplitude limiting.

Two effects stem from any change in supply voltage, each controlling the voltage gain of an inverter. The trans-conductance of each device increases as the current increases, while its output slope resistance falls. The voltage gain into open-circuit is higher at low supply voltages making it easier to define the required ratio of resistances; the increased output impedance makes it necessary to use higher value resistors to prevent

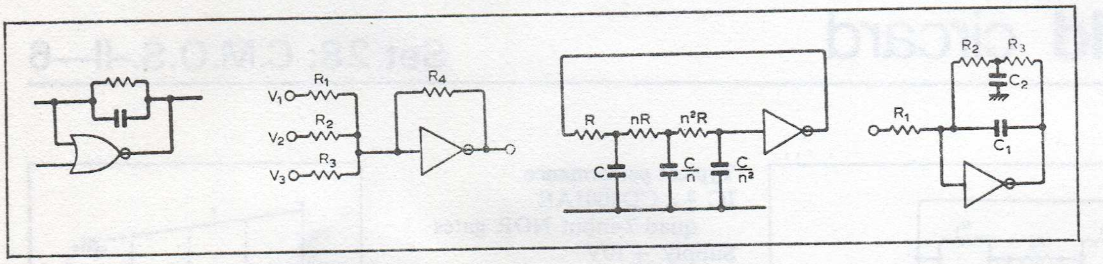


Phase detector
These are used directly in determining the phase difference between two signals of the same frequency. The signals are converted into pulses/square waves and the zero-crossings activate a switching circuit such that an output is on only for the interval between the zero-crossings of the two signals. If the output is filtered by an RC circuit the resulting direct voltage is a measure of the phase difference. Assume that the D-type flip-flop is clocked at an instant when $\bar{Q}=0$. This causes Q to go to 1, a state it retains until the reset goes to 1. The following clock pulse again drives Q to 1 with the period that Q remains at 1 varying as the positive going input at R varies in the delay with respect to the C_L input i.e. according to their phase-difference. The unit is one example of phase-detectors used in phase-locked loops. As the variable frequency oscillator drifts it causes a progressive change in the phase difference between it and the reference oscillator. The resulting change in the mean output is used to control the v.f.o. returning it into synchronism with the reference oscillator.



Frequency differencer
Two signals at different frequencies are fed into the D and C_L inputs of a D-type flip-flop. At each clock instant the D input may have either 0 or 1 and hence the output state may or may not change depending on its previous state. When the frequencies are very close it takes a large number of cycles, before a clocking instant coincides with a different value on the D input, i.e. the output rarely changes. When the frequencies are identical the D input always has the same value at the clocking instant and the output never changes. These results are consistent with the claim that the output pulse train has a frequency equal to the difference in the input frequencies. This can be very convenient in measuring small changes in a high frequency signal. It is compared by such a flip-flop with a stable frequency close to its value, and the result can be monitored on simple counters, or analogue frequency meters, on audio frequency amplifiers or displayed on an oscilloscope.

Cross references
Set 28, card 4
Set 19, card 8
Set 21, card 7



loss of voltage gain under these circumstances. The output voltage and frequency are also supply dependent but oscillations can be sustained over the range 5V-12V with a broad peak in the output in the 7 to 10V region with the samples used. The phase differences are held to 120° with a deviation of only one or two degrees except where distortion is severe. With R_2 increased to 42.5kΩ, the point at which oscillations are just sustained one output had a t.h.d. of 0.18%.

Component changes
IC: Any set of three matched inverters: CD4007, $\frac{1}{2}\times$CD4049 $3\times$CD4001 with unused inputs taken to '0', $\frac{3}{4}\times$CD40 with unused inputs taken to '1'.
Supply: In theory any supply voltage within device rating. In practice, at high voltages the open-circuit voltage gain falls; at low voltages the output impedance becomes too high. Best range 5 to 10V.
R_1: Circuit requires relatively high resistance values to reduce loading on output—typically 10k to 10MΩ.
R_2: $R_1/2$
C: can be relatively small even for low frequencies since R large—100p to 1μF.

Circuit modifications
- If the inverters are replaced by logic gates using one input for feedback, then the other input can be used to gate the oscillator. Using NOR gates, a logic '0' leaves the oscillator running, logic '1' drives the output of that gate low i.e. to logic '0'. This via the inverting action of the following stages drives their outputs to '1' and '0' respectively. If all free inputs are taken to '1' all outputs are driven to 0. The converse is true when using NAND gates.
- Most see-saw amplifier circuits can be implemented though at reduced performance because of the low open-loop gain. The outputs of the three-phase oscillator can be summed in any desired proportion by scaling R_1, R_2, R_3, $_4$ to give an output at any other phase angle. Note that all outputs are at the same d.c. potential, which will vary from device to device but will be about 50% of the supply.
- A single-stage phase-shift oscillator requires a gain of −8 if the components are graded as shown and n is large. Restricting n to 10, and operating the inverter in the range 6 to 10V comfortably exceeds the condition for sustained oscillation, allowing non-linearity to limit the amplitude. Other combinations of networks and inverting stages can be used (see Set 26).
- An approximately 90° phase-shift can be introduced by passing the signal through the circuit shown. Provided R_2, $R_3 > R_1$ and $R_3C_2 \approx R_1C_1$, the circuit approximates to an integrator? If all the inverters are well matched, R_2, R_3, C_2 can be omitted.

Cross references
Set 26, cards 3, 4
Set 21, card 5

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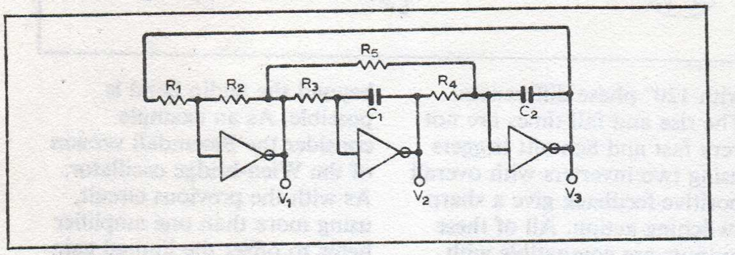
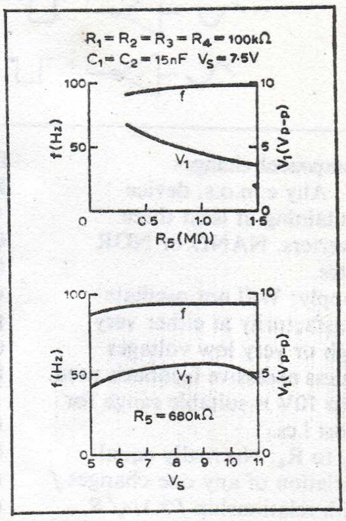
Two-integrator oscillator



Typical performance
IC $\frac{3}{4}\times$CD4001AE
NOR gates
Supply +7.5V
R_1, R_2, R_3, R_4 100kΩ
C_1, C_2 15nF
R_5 1.5MΩ
Amplitudes
V_1 3.5V pk-pk 1.1% t.h.d.
V_2 3.6V pk-pk 0.6% t.h.d.
V_3 3.9V pk-pk 0.75% t.h.d.



Circuit description
Assume initially that the inverters have a high voltage gain and that the network impedances are high enough to avoid significant loading of the inverter outputs. The system is then a two-integrator oscillator (as described in Set 26). The integrators produce a total phase shift of 180° which combined with three inversions gives an overall phase shift of zero. The finite gains and output impedances of the inverters reduce the effective Q of the system, and a separate positive feedback path is introduced via R_5 to initiate oscillation. Amplitude control is via the non-linearity of the inverters—as R_5 is reduced in value, the amplitude increases until distortion reduces the average loop gain over the cycle to accommodate the increased feedback. An alternative method of controlling the oscillation is to increase the ratio of R_2:R_1 while maintaining R_5 constant (or omitted in some cases). The three outputs are of different phase and somewhat different amplitude. The phase differences are of the order of ±90° with V_1 lagging and V_3 leading on V_2 (strictly these voltages lead and lag but with an additional inversion in each case). The resistor values may be large without the inverter inputs loading the network; the values should be large to minimize loading on the amplifier outputs. N.B. The low distortion obtained above is because only a small amount of positive feedback was used i.e. the output was not driven into its very non-linear region. For guaranteed oscillation more distortion would have to be accepted.

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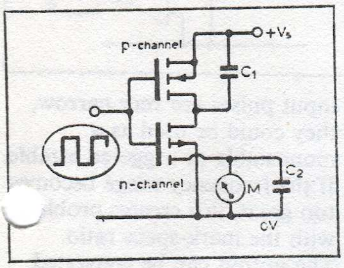
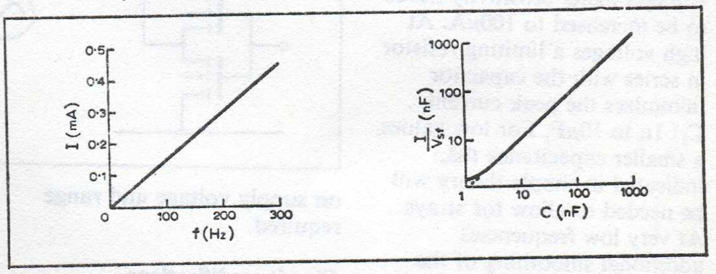
Frequency-voltage converter

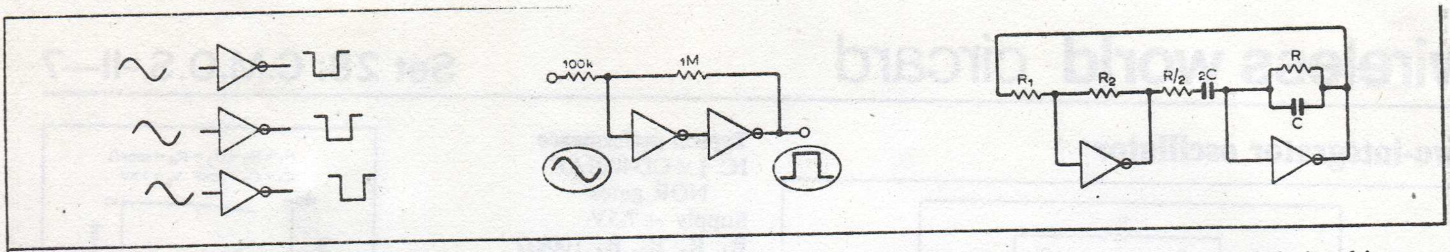


Typical performance
IC CD4007AE
Supply +10V
C_1 0.1μF
Meter 500μA, 200Ω
Input Logic level pulse train
0 to 300Hz
C_2 100μF
I fC_1V_s



Circuit description
The circuit is simple in concept and exploits the characteristics of c.m.o.s. very well. The two devices are switched alternately in and out of conduction. When the p-channel device conducts it completely discharges the capacitor provided that it is left in conduction for a long enough period. When the n-channel device conducts, it charges the capacitor fully to the supply voltage. The current flows through the meter with the shunt capacitor limiting transient effects due to meter inductance. The total charge flow per pulse is C_1V and if this occurs at a frequency f, the charge per second is fC_1V. This is by definition the mean current flow, the parameter to which the moving-coil meter responds. A small non-linearity occurs when the meter p.d. increases, since this reduces the p.d. to which the capacitor charges on the following pulses. The effect at these levels is to reduce the full scale value by less than 1%. In addition to the external physical capacitance, various strays internal and external to the circuit add to the meter reading. For a 15V supply and a meter full-scale sensitivity of 1.5mA, the meter reading was 9% high at 100kHz with a 1nF capacitor. Removal of that capacitor confirmed the presence of strays by leaving a meter reading of just over 9% of full-scale at the same frequency. The full-scale frequency range is then inverse to the value of capacitance used. This is verified up to 1μF, where the full-scale reading corresponds to 100Hz. Using a 10V supply, a 1mA movement gives the same overall sensitivity.

Component changes
IC: Any pair of complementary enhancement mode m.o.s.f.e.t.s. Other manufacturers equivalents of this i.c. may vary in respect of minimim/maximum supply voltage, frequency range cost

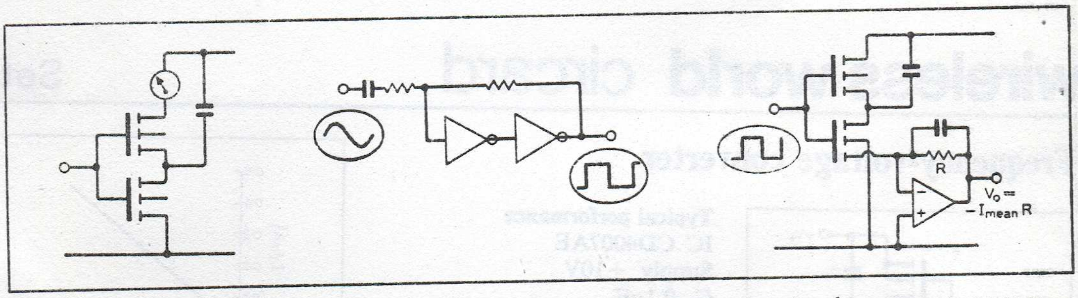


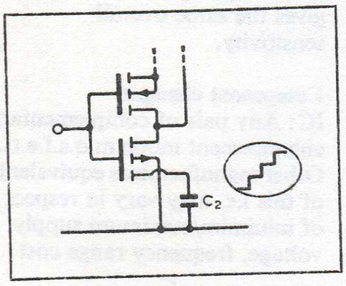
Component changes
IC: Any c.m.o.s. device containing at least three inverters, NAND or NOR gates.
Supply: Will not oscillate satisfactorily at either very high or very low voltages unless excessive feedback used. 5 to 10V is suitable range for most i.cs.
R_1 to R_4: Normally equal; variation of any one changes f with relationship $f \propto 1/\sqrt{R}$. For continuous variation in frequency with less change in amplitude, replace R_3 and R_4 by a twin-gang pot. Range of values for R_1 to R_4 typically 10k to 10MΩ. With high values it is more difficult to provide controlled positive feedback.
$R_5 \gg R_1$ etc typically $R_5/R_4 \approx 5$ to 20.
C_1, C_2: 1n to 10μF. (To obtain very low frequencies use large capacitors but not polarized units. The leakage currents may restrict the Q and inhibit oscillation.)

Circuit modifications
- Spare gates/inverters can be used to provide anti-phase outputs. If used with a pair of resistors as in the first amplifier overleaf an inverted sine wave output can be obtained from any of the three outputs. If the outputs are fed directly to the gates of three inverters, then three square-waves are obtained with 120° phase differences. The rise and fall times are not very fast and Schmitt triggers using two inverters with overall positive feedback give a sharp switching action. All of these outputs are compatible with normal c.m.o.s. logic circuits operated from the same supplies.
- Most other RC oscillators based on inverting amplifiers, op-amp see-saw circuits etc can be constructed using c.m.o.s. gates/inverters. Because the gain is already low any further losses at high frequency worsens the performance, increasing the distortion to unacceptable levels. Nonetheless oscillation to beyond the audio band is possible. As an example consider the Baxandall version of the Wien-bridge oscillator. As with the previous circuit, using more than one amplifier helps to offset the limited gain of each stage. The RC values are scaled so that the outputs are antiphase and approximately equal in value. The maximum gain of the frequency-dependent stage is a little less than unity. Hence $R_2 > R_1$ is needed.

Further reading
Good, E. F. Two-phase low-frequency oscillator, *Electronic Engineering*, vol. 29, 1957, pp. 164-9 and 210-3.

etc but the same principles apply.
Supply: 3 to 15V. At low voltages meter sensitivity needs to be increased to 100μA. At high voltages a limiting resistor in series with the capacitor minimizes the peak current.
C_1: 1n to 10μF. For low values, a smaller capacitance than indicated in simple theory will be needed to allow for strays. At very low frequencies additional smoothing of the output is needed to reduce meter fluctuations.
C_2: Used to suppress transients and/or reduce meter fluctuations at low frequencies. Not critical —may be omitted.
Meter: 50μA to 5mA depending on supply voltage and range required.





Circuit modifications
Omitting the meter and any other resistive load, produces a simple staircase generator. The output becomes non-linear as it becomes a significant fraction of the supply. A simple threshold detector using a D-type flip flop (see card 4) operated from a lower supply voltage, could be used to discharge the capacitor and restart the cycle after the end of the monostable period. The high impedances would allow a simple pulse-counting approach to be implemented at low frequencies since there would be negligible capacitor discharge. The locations of meter and capacitor can each be altered to either of the supply lines i.e. the meter can be used to measure the mean current of either charge of discharge cycles. The mark-space ratio of the input should not deviate too far from unity since the charge and discharge times of the capacitor should each be long enough for the action to be effectively completed before the changeover.
The i.c. contains two other complementary pairs that can be used as a Schmitt trigger for converting smaller sinusoidal or other inputs into a logic-level output. Alternatively if the input pulses are very narrow, they could be used as a monostable or triggered astable. If the frequency range becomes too great, this creates problems with the mark-space ratio.
The output can be converted, into a large linear voltage swing by feeding the current pulses into the virtual earth of an op-amp. Smoothing is eased by virtue of the high feedback resistor e.g. 100kΩ if a 10V output is required from an input averaging 100μA.

Further reading
Johnson, P. A. Complementary MOS Integrated Circuits, *Wireless World*, 1973, pp. 395-400.

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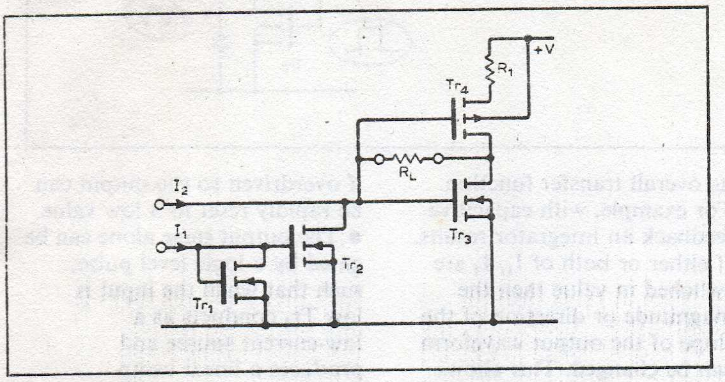
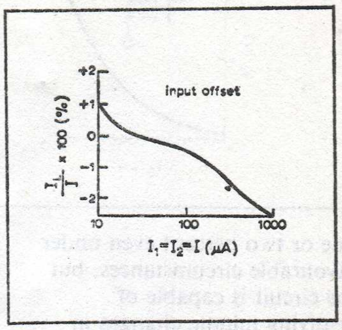
Current-differencing amplifier



Circuit description
It is possible to duplicate bipolar circuits in m.o.s. form, but a flexible approach is needed if existing c.m.o.s. packages are to be adapted. As an example, consider the current-differencing amplifier (c.d.a., or Norton amplifier). In bipolar form this uses a current-mirror at the input such that the first transistor of the amplifier proper is fed with a current equal to the difference between the input currents. Substituting a pair of n-channel transistors the current-differencing action is still obtained but the p.d. is larger. Assuming the drain-source voltage on Tr_2 is above the pinch-off level, its drain current is comparable with I_1 (net current in R_L is then I_1-I_2). If R_L becomes too large, the output stage saturates and a large voltage change at the gate of Tr_3 disturbs the relationship. The inverting amplifier, Tr_3 has a constant-current load provided by Tr_4 and R_1, since the small voltage swing at the commoned gates of $Tr_{3,4}$ produces a very small fractional change in the p.d. across R_1. Thus R_1 reduces the quiescent level of current and makes the system operate as a defined transconductance (Tr_3) operating into the feedback resistor R_L. This gives the very high output resistance indicated above. The current transfer-ratio of the current mirror remains close to unity over a wide range of currents—a total change in the imbalance of 3% over a 1000:1 range. The absolute accuracy cannot be expected to be better than

Typical performance
IC CD4007 (Tr_{1-4})
Supply +15V
R_1 100kΩ
R_L 1kΩ
I_1, I_2 100μA
I_L ±1μA
$I_L = I_1 - I_2$
Output resistance ≈ 100MΩ
at I_L = 10μA
Max. R_L ≈ 0.5MΩ
at I_L = 10μA for good linearity



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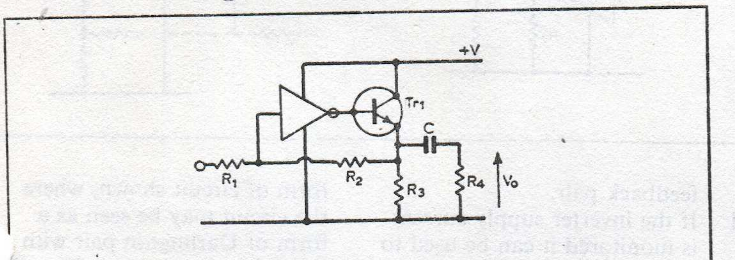
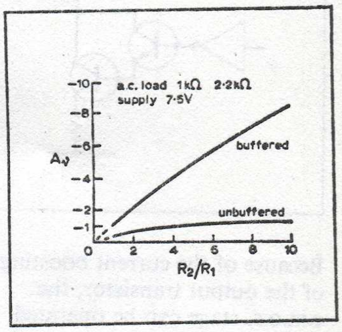
Transistor outputs

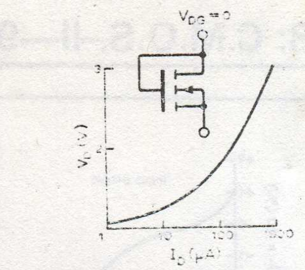


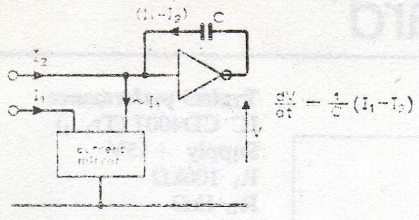
Circuit description
At low supply voltages the c.m.o.s. inverter carries a low current and has a high output resistance. Each of these facts restricts operation to high load resistances. By adding an emitter follower, the effective output impedance can be reduced and the output current increased, both by a factor of 100 or more with a suitable transistor. In the example shown, a peak current of up to 10mA was available for the load while the normal inverter quiescent current under these conditions would be about 1mA. To demonstrate the effect the resistor ratio defining the gain was varied from 1:1 to 10:1 with the c.m.o.s. device driving a 1kΩ load (i) with RC coupling to the load i.e. unbuffered (ii) with a transistor having R_3=2.2kΩ, circuit diagram as above. In the unbuffered case, the maximum value of voltage gain obtained was almost independent of the feedback values. This showed that the 1kΩ load was an effective short circuit i.e. that the gain without feedback would have been restricted to −1.3. This corresponds to a g_m of 1.3mS, while the presence of the transistor would increase this to 130mS assuming a current gain of 100. This is enough to allow a practical gain of −8.3 for a resistive ratio of 10:1 even with the a.c. load being represented by R_3 in parallel with R_4.
Another advantage is that the c.m.o.s. output is buffered from the shunt-capacitance of the load plus strays, and the gain-bandwidth product is increased.

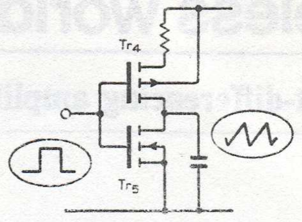
Typical performance
IC ¼ CD4001AE
(quad NOR gates)
Supply +5V
R_1, R_2 100kΩ
R_3 100Ω
R_4 100Ω
C 100μF
V_o 2V pk-pk without heavy distortion
Tr_1 BFR41
Supply current 20mA



Component changes
IC: Any c.m.o.s. inverter, gate
Supply: +5 to +15V







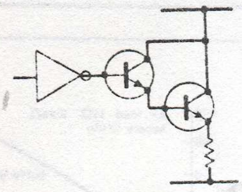
one or two percent even under favourable circumstances, but the circuit is capable of resolving minute changes in current i.e. with I_2 as the unknown current, I_1 is adjusted until the output voltage is at some reference level. Any change in I_2 produces an output voltage swing $\Delta I_2 R_L$. Alternatively R_L may be a meter, reading the current difference directly.
The p.d. across Tr_1 is more strongly dependent on current than the V_{be} of a bipolar transistor, but at low currents the rate of change for a given fractional change in current is low enough to allow the assumption of a constant p.d. ($\Delta V \approx 80$mV for a 2:1 range of currents). Hence the current can either be derived from a true current source or from a voltage source and a high series resistance.

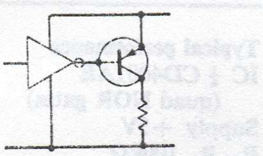
Component changes
IC: Requires access to individual devices
Supply: +10 to +15V
R_1: 10k to 220kΩ

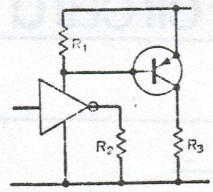
Circuit modifications

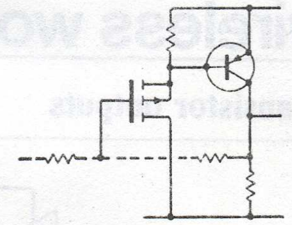
- The circuit can be used with any feedback element to define its overall transfer function. For example, with capacitive feedback an integrator results. If either or both of I_1, I_2 are switched in value then the magnitude or direction of the slope of the output waveform can be changed. This allows various triangular and ramp waveforms to be generated. When $I_1=I_2$ the net current is zero and the output voltage holds its last value.
- Because the currents can be extremely small, long integrating periods can be controlled and it could be the basis of a simple long-period timer. Tr_3 can conduct heavily if overdriven so the output can be rapidly reset to a low value.
- The output stage alone can be gated by a logic level pulse, such that when the input is low Tr_4 conducts as a low-current source and produces a linear ramp (Tr_3 is off). When the input goes high Tr_4 is cut-off and Tr_3 rapidly discharges the capacitor to ground. A source-follower could be used to buffer the resulting triggered ramp.

Cross references
Sets 16, 17, 18









Because of the current boosting of the output transistor, the c.m.o.s. stage can be operated at lower voltages than is usual for linear operation.
R_1, R_2: Not critical as R_2 no longer loads the output.
R_3, R_4: For class A operation, R_3 has to carry a quiescent current equal to or greater than the peak current required by R_4. This may be up to 100mA with a power transistor.
Tr_1: Current/power rating to suit load. Not critical.

Circuit modifications
As usual, any compound pair of transistors may be added to increase gain-complementary versions if load is to be referred to positive supply rail.
An alternative configuration is to drive the base of a common emitter amplifier (a base limiting resistor may be added at higher voltages). The output is now in phase with the input and the combination is not suitable for the direct application of overall negative feedback. Shunt feedback over the inverter together with series feedback in the transistor (emitter resistor) would be another possibility with overall feedback from the emitter to the input—a form of d.c. feedback pair.
If the inverter supply current is monitored it can be used to switch an output stage; R_2 the peak current in the c.m.o.s. stage while R_1 holds the transistor off at lower inverter quiescent currents. In addition to the load current, the c.m.o.s. pair pass through a peak of current as the output swings through its linear region and this complicates the calculations.
Over a large part of the range, the n-channel device can be assumed to be non-conducting particularly when R_2 is low. This leads to the simplified form of circuit shown, where the circuit may be seen as a form of Darlington pair with a p.m.o.s. input stage. Overall negative feedback is possible as shown since the complete stage remains an inverter albeit with a higher output current.

Cross reference
Set 27, card 5