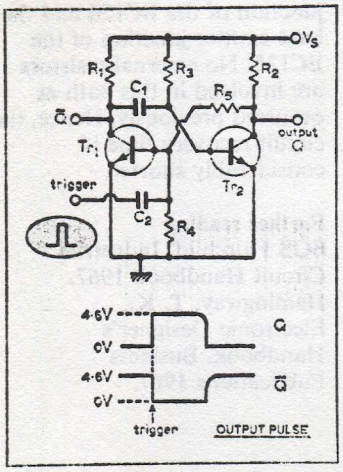
Basic discrete-component circuits



Typical performance

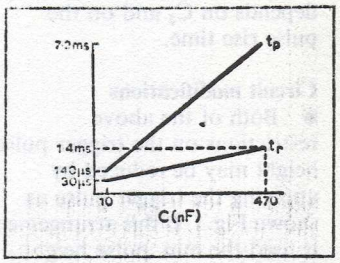
Tr_1, Tr_2: BC125
R_1, R_2: 1kΩ
R_3: 22kΩ
R_4: 4.7kΩ
R_5: 10kΩ
C_2: 100pF
V_s: 5V

Min. trigger pulse width 0.5μs
Trigger pulse height in range 1.4 to 3.6V

Output pulse width t_p depends on C_1R_3—see graph

Recovery time t_r depends on C_1R_1—see graph

Output pulse height 4.6V

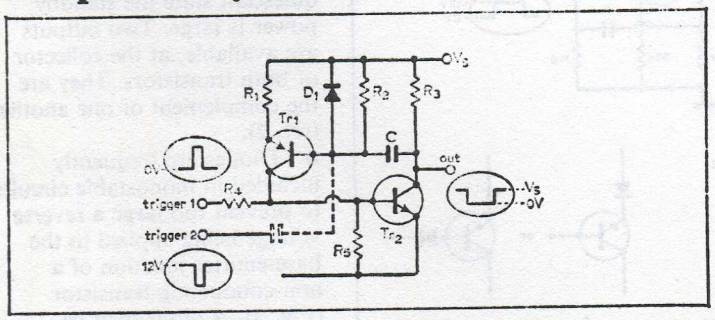


Circuit description

In the quiescent state with the trigger at 0V, Tr_2 is held on due to base drive via R_3. Point Q is therefore at zero volts and hence Tr_1 is off, its base being at 0V. In receipt of the trigger pulse the base of Tr_1 is forced positive, Tr_1 conducts and its collector voltage drops. This is transmitted via C_1 to the base of Tr_2 and hence Tr_2 is forced off, raising its collector voltage.

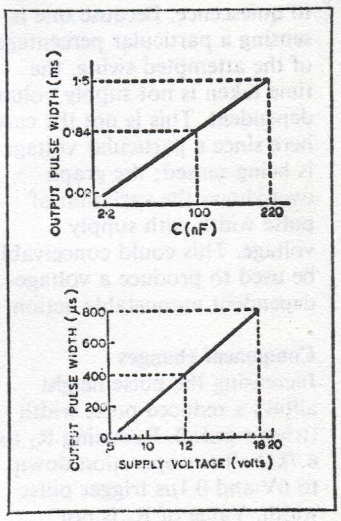
By potential division via R_5 and R_4, the base of Tr_1 is forced positive, thus forcing Tr_1 further into conduction. This positive feedback action forces a rapid change in state of both Tr_1 and Tr_2. C_1 then has one side at 0V, point $\bar{Q}$, and the other side connected via R_3 to V_s. It thus commences to charge towards V_s. This continues until the potential at the base of Tr_2 reaches a value which causes Tr_2 to start conducting. Point Q then starts to fall in potential causing the base of Tr_1 to fall. This causes $\bar{Q}$ to rise, forcing the base of Tr_2 even higher and rapidly the two transistors change back to the quiescent state. Length of the output pulse depends on C_1R_3. See graph.
The original quiescent state is not reached until C_1 has returned to its original uncharged state. The discharge path is via R_1 and the base-emitter junction of Tr_2. Discharge time is what accounts for the recovery time, t_r + the minimum time after the output pulse trailing edge at which a further trigger pulse will give correct operation; see graph above.
Maximum trigger pulse height is fixed by the negative-going voltage applied to the base of Tr_1 on receipt of the trailing edge of the trigger pulse. If this

Complementary circuits



Typical performance

Rr_1: BC126, Tr_2: BC125
R_1, R_2: 33kΩ
R_3: 1.2kΩ, R_4, R_5: 10kΩ
D_1: 1N914
With V_s=12V, trigger frequency is 500Hz, trigger pulse width and height 10μs and 2V respectively graph opposite of output pulse width against C was obtained.
With C=47nF and pulse width of 10μs, minimum trigger pulse height about 1.3V.
With pulse height at 2V, minimum pulse width about 2μs.
Output pulse height about 12V; maximum mark-space ratio is 10: 1 at this frequency.



Circuit description

Monostable circuits using complementary transistors allow one to trigger either with respect to the positive supply line.
In the circuit shown both transistors are non-conducting in the quiescent state. On receipt of a positive-going pulse at trigger point 1, Tr_2 starts to conduct, dropping its collector voltage. This drop is transmitted via C to the base of Tr_1 and hence Tr_1 starts to conduct. This produces further base drive to Tr_2 and pushes it further into conduction. Very quickly both transistors are fully conducting and the output, initially at V_s drops to 0V approximately.
Capacitor C, uncharged in the quiescent state, then begins to charge towards V_s via R_2 and Tr_2. When it reaches $V_s - V_{be}$, Tr_1 is cut off, Tr_2 is cut off and the capacitor discharges via D_1 and R_3 principally. Insertion of D_1 provides a low resistance discharge path giving a fast recovery time.
When Tr_2 is cut off the output swings back to V_s so the output pulse period is determined by the charging time of the capacitor.
With the basic monostable circuit (card 1) the capacitor is, in the quiescent state, charged in one direction and this direction is reversed when triggered. Ignoring V_{be} effects, the capacitor during charging

is greater than the bias set by R_4 and R_5 then T_1 is switched off immediately and monostable action is prevented.
Minimum trigger pulse height depends on C_2 and on the pulse rise time.

Circuit modifications

- Both of the above restrictions on the trigger pulse height may be reduced by applying the trigger pulse as shown Fig. 1. If this arrangement is used the min. pulse height should be about 0.7V and the maximum should be the breakdown voltage of the triggering transistor.
- A general-purpose diode e.g. 1N914 should be inserted in the base line of Tr_2 as shown Fig. 2, if the supply voltage used is above 6V or so which is the base-emitter breakdown voltage of most planar transistors. If this is not done the linearity of t_p with respect to C is lost.
- If short recovery times are required between consecutive output pulses the circuit of Fig. 3

Fig. 1

Fig. 2

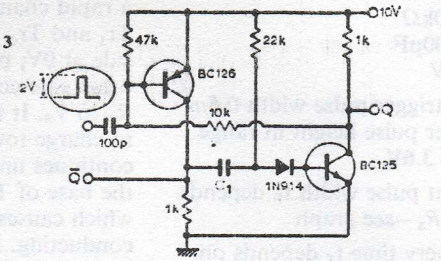


Fig. 3

may be used. In the quiescent state both transistors are conducting, Q is low and $\bar{Q}$ is high. On receipt of the trigger pulse the p-n-p transistor (BC126) is switched off causing the base of the BC125 to fall in potential, thereby raising the voltage of Q and, via the 10kΩ resistor, the base of the BC126. The circuit thus latches into a condition where both transistors are off. Capacitor C_1 then charges via the 22k and 1kΩ resistors toward the supply and eventually turns the BC125 on and with it the BC126. Discharge of C_1 occurs more quickly in this case because the discharge path is through the collector-emitter junction of the BC126 and the base-emitter junction of the BC125. No external resistors are involved in this path as occurred previously. Hence, the circuit recovery time is considerably shorter.

Further reading

SGS Fairchild. Industrial Circuit Handbook 1967.
Hemingway, T. K., Electronic Designer's Handbook. Business Publications 1967.

is going from $+V_s$ to $-V_s$ and the 0V or 50% point is sensed to bring the circuit back to quiescence. Because one is sensing a particular percentage of the attempted swing, the time taken is not supply voltage dependent. This is not the case here since a particular voltage is being sensed; the graph over shows the variation of pulse width with supply voltage. This could conceivably be used to produce a voltage-dependent monostable action.

Component changes

Increasing the pulse height allows a reduced pulse width (trigger pulse). Reducing R_1 to 4.7kΩ allows operation down to 6V and 0.1μs trigger pulse width. Value of R_2 is not critical; R_3 depends on Tr_2; R_4 and R_5 not critical.

Similar circuits

- The circuit of Fig. 1 will have zero stand-by power consumption but in this case has a positive-going output pulse. Again the output pulse

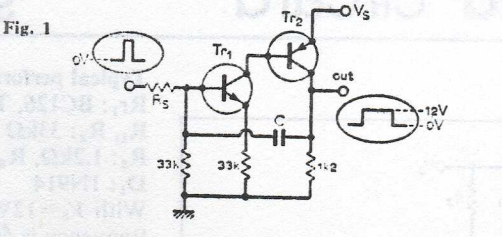


Fig. 1

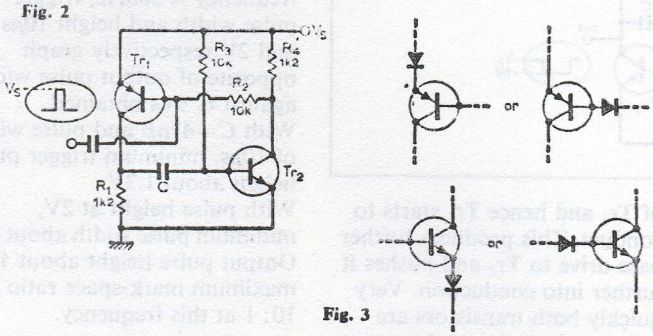


Fig. 2

Fig. 3

width will depend on V_s, since in the quiescent state of C is uncharged. In addition the V_{CEsat} of Tr_2 will affect the height of the pulse which should be $V_s - V_{CEsat}$. The 0V level should be well defined. In the circuit over the V_{CEsat} affects the 0V level but not the peak value (ref. 1).

- The circuit of Fig. 2 has a pulse width given by $t_p = 0.69(R_1 + R_3)C$ and a recovery time given by $t_r = R_3C/\beta$. As recharging current is supplied by Tr_1, this recovery time is short. Pulse width is not supply dependent but since both transistors conduct in the quiescent state the standby power is large. Two outputs are available, at the collector of both transistors. They are the complement of one another (ref. 2).
- Diodes are frequently included in monostable circuits to prevent too large a reverse voltage being applied to the base-emitter junction of a non-conducting transistor (Fig. 3). A diode may be inserted in the emitter lead or in the base lead. The last-mentioned is generally preferred in that it will not affect the output pulse levels.

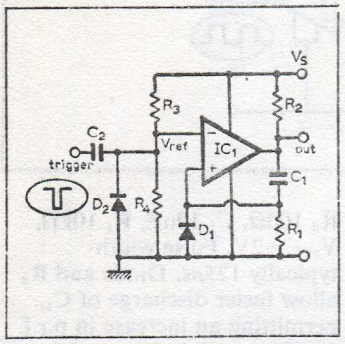
References

1 Electronic Circuit Design Handbook, Tab. p.174.
2 Electronic Circuit Design Handbook, Tab. p.85.

Cross references

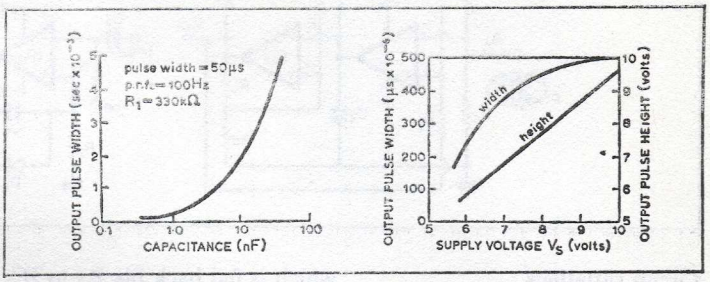
Set 18, card 1
Set 10, card 4

Op-amp / comparator circuits



Typical performance
IC_1: ¼ LM139
V_s: +10V
C_1: 1nF
C_2: 470pF
R_1: 330kΩ
R_2: 10kΩ
R_3, R_4: 1MΩ
D_1, D_2: 1N914
Trigger pulse width: 30μs
Trigger pulse level: 6V
Output pulse width: 190μs
Output pulse level: 9V

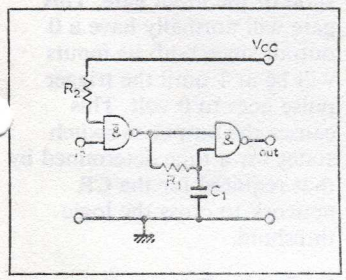
Circuit description
This comparator features an open-collector output, and may be used with pull-up resistor R_2 and a separate supply to give a wide switching range. Resistors R_3 and R_4 set the reference voltage equal to $V_s/2$, but also determine the trigger pulse level necessary for switching. Resistor R_1 should be much greater than R_2 to avoid loading the output. With $V_{ref} = V_s/2$ and the non-inverting input near 0V, the output transistor of the comparator is conducting and the output is at V_{CEsat}.
A negative trigger pulse at the input causes this transistor to switch off and hence the voltage at the output rises to almost V_s. Capacitor C_1 now charges at a rate mainly determined by R_1 and C_1, which also control the width of the output pulse. The potential of the non-inverting input now falls exponentially from V_s and the comparator switches to its original condition when the non-inverting comes below $V_s/2$. Diodes D_1 and D_2 prevent the inputs from being driven below zero volts, and D_1 also provides a low impedance discharge path for C_1.



Component changes
IC_1: ¼ × MC 3302P
Useful range of C_1: 220p to 22nF
Useful range of R_1: 47k to 470kΩ
Minimum trigger pulse width: 5μs
Minimum trigger pulse height: 5V (for V_s = +10V)
Range of V_s: up to 28V.

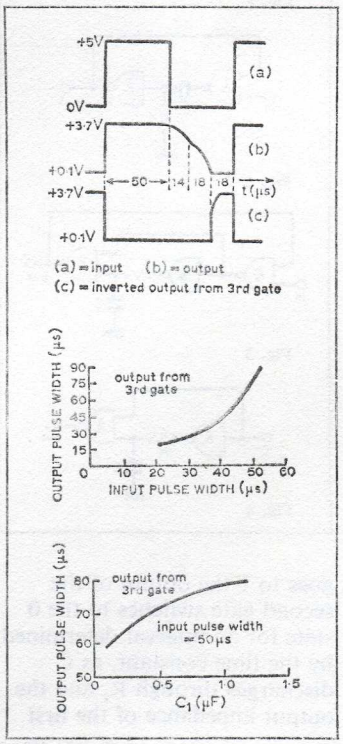
- Increasing trigger pulse height of 8V decreases pulse width by 150 to 200μs.
- Variation of pulse width with capacitance shown, for trigger pulse 5V.
- Output pulse is supply dependent, see graph above. (For C_1 = 1nF, R_4 = 330kΩ, p.w. is 50μs.)

Monostable using t.t.l. gates

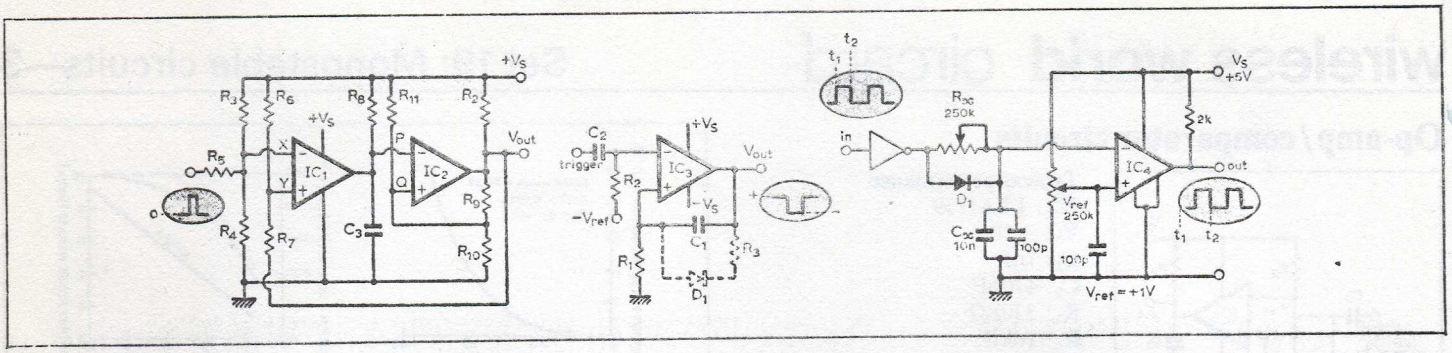


Typical performance
Logic gates: ¼ × 7400
Supplies: +5V; 8mA
R_1: 100Ω, R_2: 1kΩ, C_1: 1μF
Input pulses: amplitude +5V
Width: 50μs, p.r.f. about 10 kHz
Output pulse width about 74μs

Circuit description
The circuit above uses two of the four NAND gates available in the integrated circuit package. Positive trigger pulses are applied to the first gate which is connected as an inverter, the unused input being taken to the positive supply rail (logic 1 state) via a 1-kΩ resistor to prevent the gate being damaged by a supply line transient. With the trigger input in the logic 0 state (0V), the output of the first gate is at 1, as are both the inputs to the second gate in the steady state, causing its output to be at logic 0. A positive trigger pulse causes the output of the first gate to go to its logic 0 level. One of the two inputs to the second gate immediately goes to the logic 0 level but its other input receives the voltage across C_1 which cannot change its charge instantaneously. The inputs to this gate are thus at logic 0 and 1 respectively, causing its output to switch to 1 where it remains until the trigger pulse returns to the 0-volt level. During this interval, capacitor C_1 discharges towards 0 volt through R_1 and the output impedance of the first gate and is recharged to the 1 level after the trigger pulse has returned to the 0-volt level.



Circuit changes
Useful range of V_{cc}: +4.5V to +5.5V
Maximum useful R_1: 470Ω
Maximum useful C_1: 1.5μF
Minimum trigger pulse amplitude: +3V
Minimum trigger pulse width: 40μs
Output pulse shape improved by cascading a third gate (see waveform and graphs above). Cascading the fourth gate in the package provides a pair of complementary outputs.



Circuit variations

● Circuit shown left gives a pulse width that is supply independent, and is capable of a high duty cycle. Capacitor C_3 is initially charged to $+V_{cc}$ and V_{out} is at almost zero volts. Potentials at X and Y are defined by associated divider chains. A positive input trigger pulse to make $V_X > V_Y$ causes IC_1 to switch (output driven low). Capacitor C_3 rapidly discharges, and IC_2 will switch when the voltage across C_3 falls below V_Q, defined by R_{11}, R_{10}. Output voltage is now equal to V_{cc}, which is fed back bia R_7 to IC_1 which again switches to off condition. Hence C_3 now charges up via R_8. Output pulse width is defined by the time for the voltage across C_3 to just exceed that of point Q; IC_2 then reverts to its on, or low-output state. IC_1, IC_2 ¼ LM139, R_5, R_4 100kΩ, R_6 1MΩ, R_7 62kΩ, R_8, R_9 10MΩ, R_{10} 220kΩ, R_{11} 560kΩ, C_3 0.1nF.

Note that retriggering is not possible while IC_2 output is high—a useful lock-out feature.

● Circuit centre, using an op-amp, has a similar action to the comparator network. A negative reference voltage on the inverting input, with the non-inverting input tied to ground, gives a stable condition where $V_{out} = +V_s$. A positive input trigger sufficient to cause the differential input polarity to change, the output switches to $-V_s$. At this instant the potential of R_1 with respect to ground is $-2V_s$. As C_1 charges, the potential across R_1 rises towards $-V_{ref}$, when switching again occurs, and circuit resets to initial condition.

Component values: IC_3 MC1530/1531, C_2 23pF, R_2 100Ω, C_1 10nF, R_1 10kΩ, V_{ref} = 2V. Pulse width typically 125μs. Diode and R_3 allow faster discharge of C_1, permitting an increase in p.r.f.

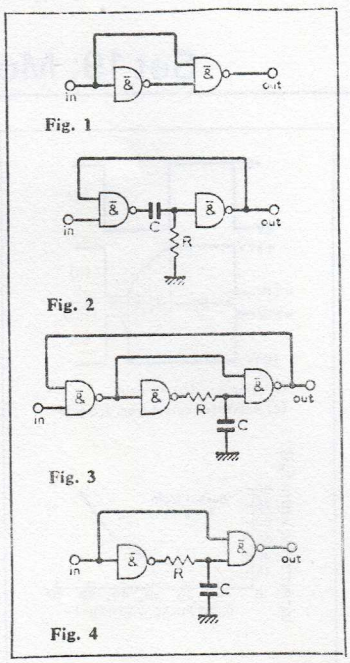
● Circuit right is a useful interface for delaying logic signals. When logic level is 1, capacitor charges quickly via diode, discharges via R_x wher logic level is 0, allowing V_{out} to rise when $V_{Cx} \rightarrow +1V$. Using LM311, claimed delay is typically 0.04 to 370ms.

Cross reference

Set 17, card 8.

Circuit modifications

● The simple two-gate circuit shown in Fig. 1 has positive trigger pulses fed simultaneously to one input of each gate. These pulses appear at the output of the first gate inverted and delayed by the propagation time of the gate. Both of the inputs to the second gate are therefore at the 1 level for a short period, providing a narrow negative-going output pulse, delayed by the propagation time of one gate. This circuit has two defects: the output pulse is very narrow and non-adjustable and the trigger pulse must be wider than the output pulse.



● The circuit shown in Fig. 2 overcomes the first defect but still requires a trigger pulse wider than the output pulse. When the trigger input is at logic 0 the output of the first gate is at 1. Inputs to the second gate are at logic 0 and 1 since C is charged from the first gate, hence the output is at 1. When the trigger pulse goes to 1 the output of the second gate switches to the 0 state for an interval determined by the time constant, as C discharges through R, and the output impedance of the first gate. When C has discharged to a level where its voltage crosses the switching threshold of the 1 to 0 transition the output from the second gate switches back to its 1 level. Trigger pulse width must still be greater than the output pulse width, as the output of the second gate will always return to the 1 state whenever the trigger pulse returns to 0 volt.

● To overcome this problem the trigger pulses can be fed to the monstable via a third gate which has an output logic state determined by the monstable output, as shown in Fig. 3. Addition of this gate causes the monostable to be triggered when the input transition is from the 1 to the 0 state and the width of the input pulses is only that required to cause the input and output gates to change state. Since the same time constant controls the charge and discharge rates of C both circuits have relatively low maximum duty cycles, typically around 25%.

● Circuit of Fig. 4 uses only two gates but has a very similar mode of operation, the output pulses controlling the state of the input gate. This gate will normally have a 0 output since both its inputs will be at 1 until the trigger pulse goes to 0 volt. This causes the output to switch states for a time determined by that required for the CR network to cross the logic threshold.

Further reading

Malmstadt, H. V. and Enke, C. G., Digital Electronics for Scientists, Banjamin 1969, pp. 213-5.

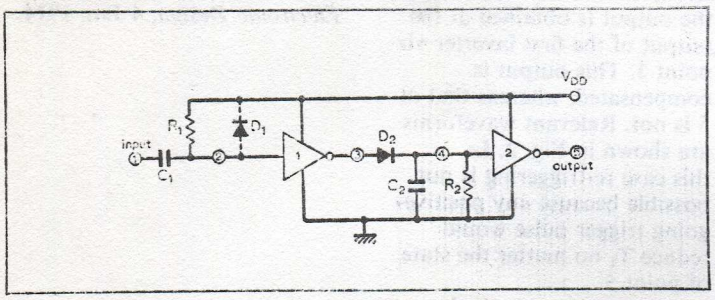
Wilke, W., Operating a logic gate as a flip-flop, *Electronics*, 21 March 1974, pp.120/1.

Kaniel, A., Digital delay circuit for one-shot controls timing interval programmable integer steps, *Electronic Design*, 18 Jan. 1974, p.94.

Cross reference

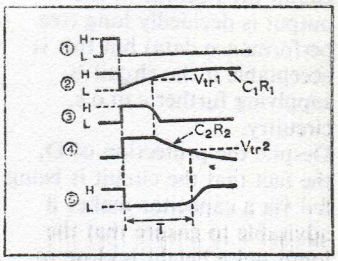
Set 11, card 3.

Compensated c.m.o.s. circuits



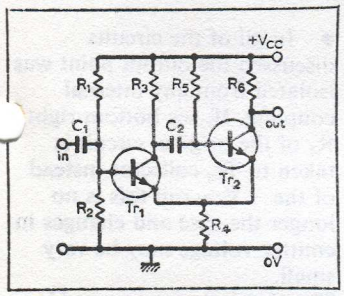
Components
D_2: general-purpose diode
Inverter 1 and 2:
$\frac{1}{3} \times$ CD4007AE

Performance
$R_1C_1 = R_2C_2 = RC$
$T \approx 1.4RC$; tested in range
$10\mu s < T < 1ms$
With clock rate of 1kHz and pulse width 400μs, T remains within 4% of the nominal value over supply range 5V to 10V. With T of 330μs fall time is minimal but rise time is 120μs.

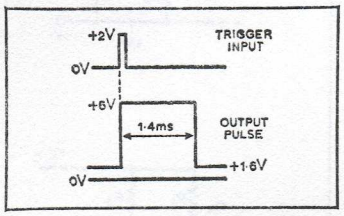


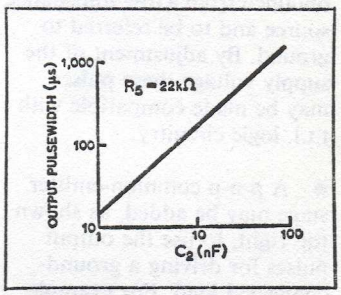
Circuit description
Complementary m.o.s. monostables using one time constant suffer from the fact that the transfer voltage (V_{tr}) of i.cs can vary by as much as ±33% so that replacement of an i.c. by another can result in a considerable change in the output pulse width. This defect can be removed by using two identical time constants with two inverters on the same chip. In this case the transfer voltage of both inverters is almost identical and the effect is cancellation of the variation in transfer voltage. This is taken advantage of in the circuit shown.
In the quiescent state with the input pulse low (ground), point 2 is high (V_{RR}), points 3, 4 and 5 are therefore low, low and high respectively. Capacitor C_1 is therefore in a charged state. On receipt of the input pulse this charge is removed rapidly via the source resistance and D_1 which is an internal protection device to prevent the input rising beyond V_{DD}. On the negative-going edge of the input pulse point 2 is taken down to ground and C_1 commences to charge towards V_{DD} via R_1. Point 3 will go high and remain in this state until C_1 passes through the transfer voltage of inverter 1. When point 3 goes low C_2 will commence to discharge via R_2, D_2 acting to prevent discharge into inverters. When point 4 passes through the transfer voltage of inverter 2 point 5 will go high and the operation is complete.
The graphs show that there are two possible outputs—at points 3 and 5. The output at point 5 is the only one in

Emitter-coupled circuits



Typical performance
Supply: +6V, 4mA
Tr_1, Tr_2: BC125
R_1: 6.8kΩ
R_2: 1.8kΩ
R_3: 2.7kΩ, R_4: 330Ω
R_5: 22kΩ, R_6: 1kΩ
C_1: 100pF, C_2: 100nF
Input pulse amplitude: +2V
Input pulse width: 1μs
p.r.f.: 1kHz
Output pulse—see waveform below





Circuit description
In the stable state Tr_2 is on and saturated due to the base drive via R_5. The emitter current of Tr_2 causes the common emitter voltage to be at approximately 1.5V. Thus Tr_1 is held off by the R_1R_2 potential divider which maintains its base at about 1.3V, slightly reverse-biasing the base-emitter junction. Output voltage at Tr_2 collector is at approximately 1.6V in this stable state. The C_1, R_1, R_2 network differentiates the input trigger pulses and, if these have a positive-going transition large enough to exceed the emitter voltage by V_{BE}, Tr_1 will switch on and saturate. The collector voltage of Tr_1 falls by about 4.5V and this negative-going transition passes to Tr_2 base through C_2 so this transistor switches off. Output voltage rises to +Vcc and Tr_2 remains in the off state while C_2 charges via R_3, Tr_1 and R_4. As C_2 charges, the base voltage of Tr_2 rises exponentially towards +Vcc but when it exceeds the emitter voltage, Tr_2 rapidly turns on and saturates. Current in R_4 increases, producing a corresponding rise in the emitter voltage which reverse-biases the base-emitter junction of Tr_1, which switches off, and the circuit returns to its stable state.

Circuit changes
Minimum trigger pulse width 0.5μs. Output pulse width could be varied by R_5 but this would also change the d.c. conditions. Larger supply voltages may be used but then a silicon diode should be included in series with Tr_2 base to prevent reverse breakdown of its base-emitter junction by the switch-off transient.

▶

which there is compensation for transfer voltage variation. Due to lack of feedback in the circuit the risetime of the output is decidedly long (see performance data) but this is acceptable if the circuit is supplying further c.m.o.s. circuitry.

Despite the protection of D_1 the fact that the circuit is being fed via a capacitor makes it advisable to ensure that the input pulse height is close to V_{DD}. This can be done if the pulse is fed via further c.m.o.s. supplied from V_{DD}.

This circuit can be re-triggered, i.e. the output 5 can be maintained in its low state by feeding in a succession of pulses, provided each pulse occurs before point 2 reaches the transfer voltage of the first inverter.

Fig. 1

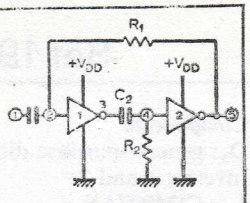


Fig. 2

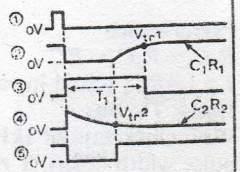


Fig. 3

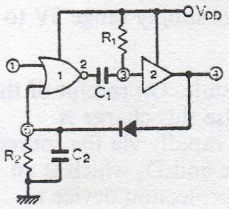
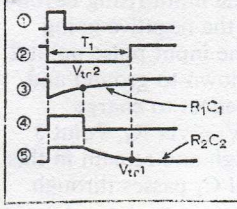


Fig. 4



Circuit modifications

● A positive-going output pulse, again triggered by the negative-going edge of the input is obtainable with the circuit shown top. In this case the output is obtained at the output of the first inverter viz point 3. This output is compensated, whereas that at 5 is not. Relevant waveforms are shown in Fig. 2. In this case re-triggering is not possible because any positive-going trigger pulse would reduce T_1 no matter the state of point 5.

● A negative-going pulse triggered on the positive-going edge of the input pulse is obtainable from the circuit shown in Fig. 3. For compensation, the output is taken from point 2 in this diagram. Relevant waveforms are as in Fig. 4. With this circuit re-triggering is also impossible because point 2 will stay low so long as point 5 is high, the trigger signal having no effect due to the normal NOR gate action.

Further reading

RCA applications note ICAN6267.

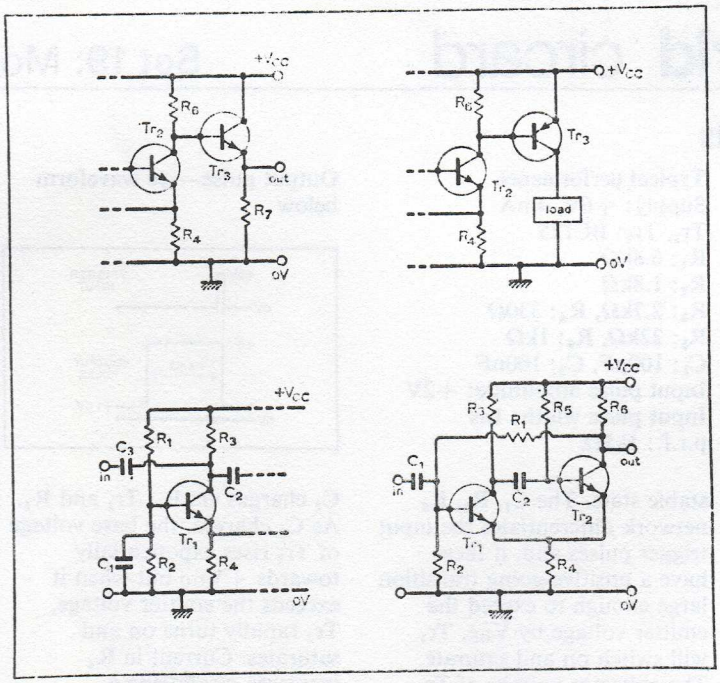
Murphy, C. Simple reconnection reduces rise time of CMOS delay circuit. *Electronic Design*, 4 Jan. 1974.

Circuit modifications

● Adding an emitter-follower to the original circuit, as shown in the top left diagram, allows the output pulses to be obtained from a low-impedance source and to be referred to ground. By adjustment of the supply voltage these pulses may be made compatible with t.t.l. logic circuitry.

● A p-n-p common-emitter stage may be added, as shown top right, to use the output pulses for driving a ground-connected load. For example, the load could be in the form of a filament lamp for alarm or monitoring purposes and as collector currents of at least 50mA may be obtained, the load could be a relay coil to provide control of some other circuitry. The inductive load provided by the relay coil should be shunted with a protective diode.

● The original circuit may be modified to be triggered by negative-going pulses as shown in the circuit shown bottom left. In this arrangement the trigger pulses are applied to the collector of Tr_1 via the small coupling capacitor C_3.



The negative-going trigger pulse edge is passed to Tr_2 base through C_2 switching this transistor off. Tr_1 turns on and the remaining cycle of operations are as described previously. The circuit will function with C_1 omitted but the transition to the quasi-stable state will be more rapid when it is included in the circuit.

● In all of the circuits discussed the output point was isolated from any internal coupling. If, see bottom right R_1 of the original circuit is taken to Tr_2 collector instead of the $+V_{CC}$ rail this is no longer the case and changes in emitter voltage may be very small.

The simplest way to provide faster switching is to prevent Tr_1 and Tr_2 from saturating by increasing R_4.

Further reading

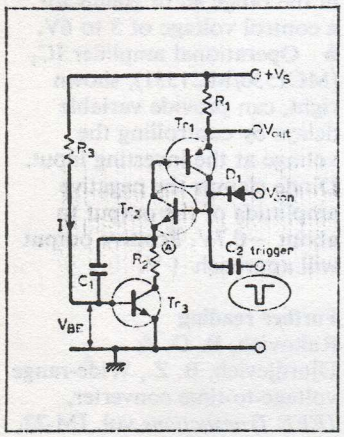
SGS-Fairchild, Industrial Circuit Handbook, 1967, pp.51/2.

Budinsky, J., Techniques of Transistor Switching Circuits, Iliffe 1968, pp.486-91.

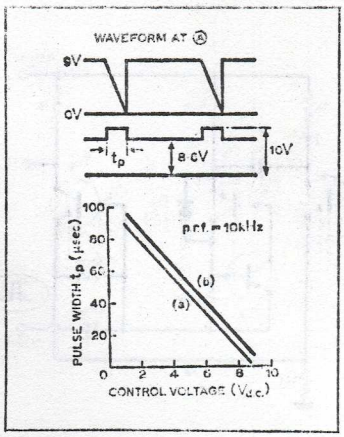
Cross references

Set 18, cards 1 and 7.

Voltage-controlled monostables



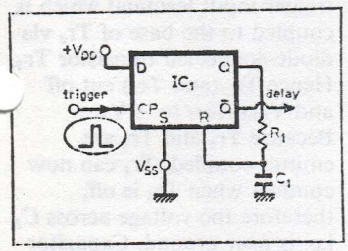
Typical performance
Tr_1: BC126
Tr_2, Tr_3: BC125
R_1: 22Ω, R_2: 1.2kΩ
R_3: 10kΩ
C_1: 1nF, C_2: 100pF
$+V_S$: +10V
D_1: 1N914
Trigger pulse magnitude: −13V
Trigger pulse width: 0.1μs
$V_{control}$: 8V
Output pulse duration: 7μs
Waveforms and timing graph shown opposite, curve (a)



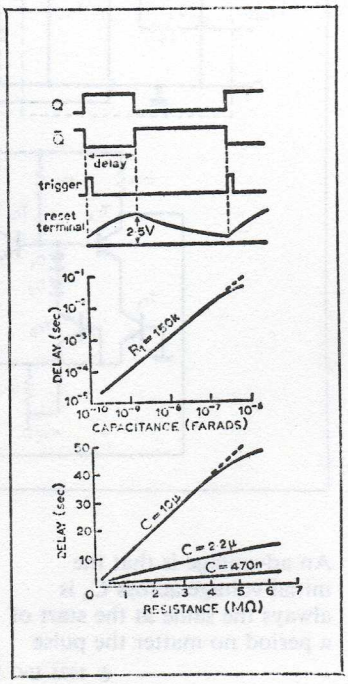
Circuit description
Transistors Tr_1, Tr_2 form a complementary-pair positive feedback switch, and are either both off or both on. In the rest state, this switch is closed, Tr_3 is on, D_1 is non-conducting, and C_1 is charged. A negative trigger pulse applied at the trigger terminal causes the regenerative switch (Tr_1, Tr_2) to open. Collector current of Tr_3 is now αI, where α is common base current gain and $I=(V_S-V_{BE})/R_3$. Hence C_1 discharges at a constant rate giving a run-down linear sweep at point A. This sweep continues until the potential of point A is less than $V_{control}-V_{D_1}-V_{BE(Tr_2)}$, when the complementary switch again conducts. The switch also acts as a comparator, besides providing a low impedance path for recharging capacitor C_1.
Notice that the sweep termination depends on the level of the control voltage, which therefore controls the width of the output pulse.

Component changes
Tr_2, Tr_3: BSX28, Tr_1: BSX29
Useful range of C_1: 1 to 47nF
Useful range of R_3: 10k to 100kΩ
Useful range of control voltage is in the range 10% to 90% of $+V_S$.
To minimize inductive and stray capacitive effects, this circuit was constructed on a p.c.b. to obtain above measurements.
Rise and fall times of output pulses less than 0.5μs.
Control voltage may be obtained from potential divider connected across supply.

Long-delay circuits using c.m.o.s. and unijunction devices



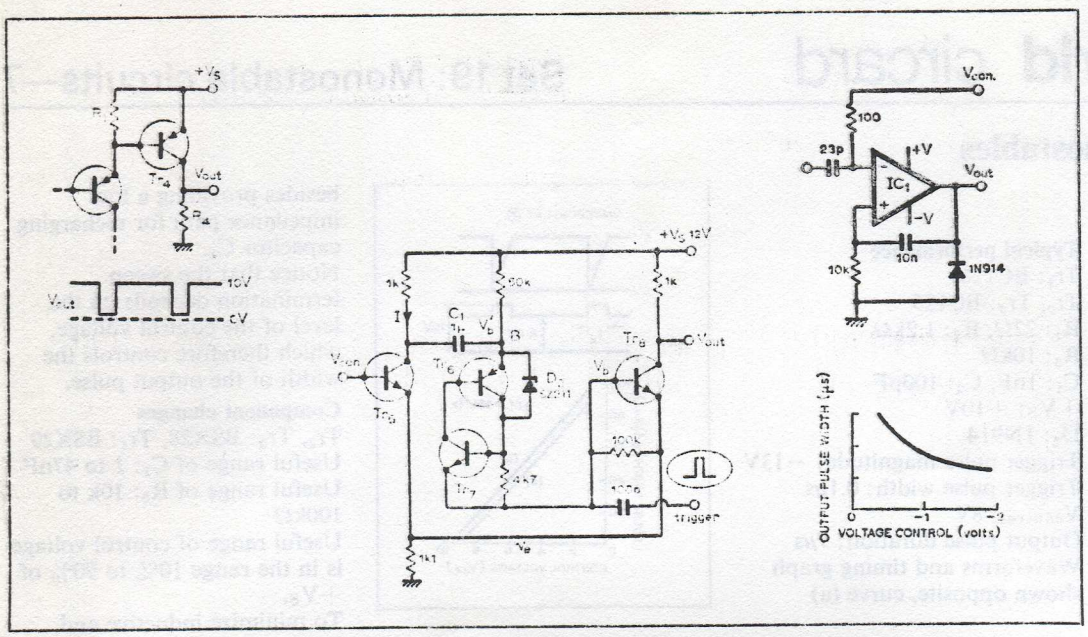
Typical performance
IC_1: ½ × CD 4013AE
V_{DD}: +5V, Vss: 0V
R_1: 470kΩ, C_1: 10μF
Trigger pulse width: 1μs
Trigger pulse height: 4V
Delay: 9s
Typical waveforms and delays shown opposite.



Circuit description
The high input impedance of c.m.o.s. integrated circuits offers a low leakage path for capacitor C_1, and thus allows a wide range of delays from this D-type flip-flop configuration. The D-input is permanently connected to the positive supply rail, hence Q goes high when a positive trigger pulse is applied at the clock input. A positive voltage (approximately 50% $V_{DD}-V_{SS}$) at terminal R will reset Q to its initial condition of 0V.
On the occurrence of a trigger pulse, the reset threshold will be reached in a time defined by C_1 and R_1, which in turn defines the delay available at $\bar{Q}$. This circuit is fairly insensitive to supply voltage change, because the threshold level for reset will alter pro-rata. However it should be noted that this level is not well defined, and hence the accuracy of time delays will depend on specific measurement with the components used.
Unused inputs should be tied down to ground.

Component changes
Useful range of R_1: 100k to 10MΩ
Useful range of C_1: 47pF to 32μF
(For long time delays, low-leakage capacitors must be used)
Supply voltage range: $(V_{DD}-V_{SS})$ 3 to 15V
Minimum pulse width: 0.1μs
Minimum pulse height: 2 to 4V
Alternative IC: MM74C74

UJT transistor monostable
The circuit shown over (top) employs a discrete transistor flip-flop, with the timing controlled by the firing of the unijunction transistor Tr_1. The normal rest condition of



Circuit modifications

● Connect additional buffer stage Tr_4 (BC126) and R_4 (390Ω) for increased output pulse amplitude (above). Trigger pulse amplitude is 7V, when coupling capacitor C_2 increased to 1nF; provides

timing graph shown over at (b).

● Circuit (centre) is basically an emitter-coupled monostable circuit. Time duration may be extended by the inclusion of a complementary pair (Tr_6, Tr_7) with breakdown fixed by zener diode D_2. This effectively increases the cut-in voltage, V_b, of Tr_8. Tr_8 is normally on. Trigger pulses cause Tr_5 to conduct (Tr_8 off), and circuit returns to its stable state when the voltage at B brings the regenerative switch into conduction. Pulse duration depends on I, which is controlled by voltage applied to base of transistor Tr_5. Output pulse duration typically in the range 40 to 200ms for a control voltage of 3 to 6V.

● Operational amplifier IC_1 (MC1530/MC1531), shown right, can provide variable delays by controlling the voltage at the inverting input. Diode clamps the negative amplitude of the output to about −0.7V. Positive output will approach +V.

Further reading

Rakovich, B. D. & Djurdjevich, B. Z., Wide-range voltage-to-time converter, *IEEE Transactions* vol. IM-22, no. 2, June 1973, p.162.
Time delay circuit for SCR control, *Electronic Eng.* June 1974, p.14.
Motorola application note AN-258.

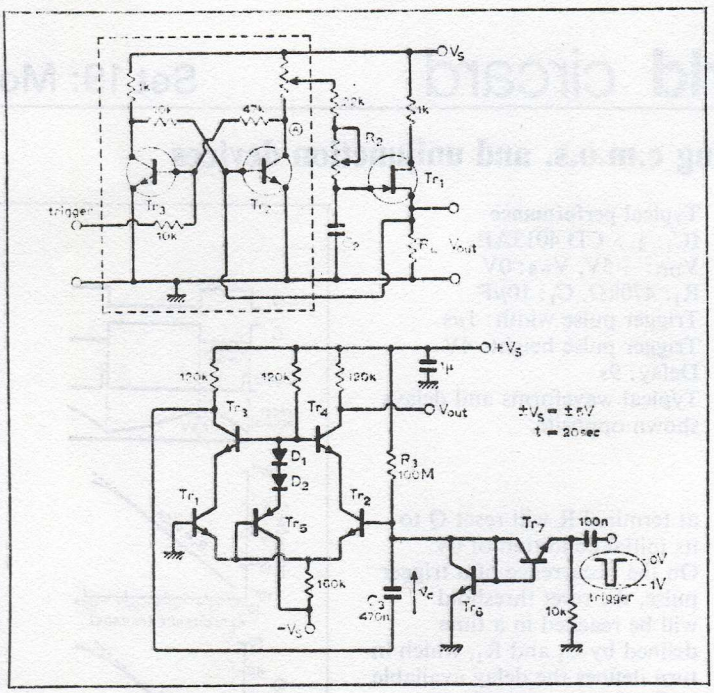
Cross references

Set 18, card 3, 6.

bistable FF1 is Tr_3 off and Tr_2 conducting. Hence the available voltage at point A is approximately V_{CEsat} of Tr_2. This is much less than the firing voltage V_P of the unijunction transistor which therefore is non-conducting, and the output voltage is at zero volts.

A positive pulse applied at the trigger input brings Tr_3 into conduction, and due to positive feedback Tr_2 is rapidly switched off. Hence the potential of point A rises. Voltage across C_2 now rises exponentially toward $+V_S$. When it reaches V_P in a time determined by R_2C_2, Tr_1 will conduct and discharge C_2 via the emitter and the resistor R_E. The output pulse developed across R_E is applied to the base of Tr_2 to turn it on again and hence reset the bistable, and turn off Tr_1. Well-defined output pulses are also available at the collectors of Tr_2 and Tr_3.

R_2 1MΩ, C_2 1μF, R_E 27Ω, Tr_1 2N4853, Tr_2/Tr_3 2N4123, V_S +10 to +30V.



An advantage is that the initial voltage across C_2 is always the same at the start of a period no matter the pulse repetition frequency. It is claimed that with the supply voltage variation noted above, pulse duration changes are 2%.

Circuit (bottom) uses the transistor array CA3095E. Diodes D_1, D_2 and Tr_5 act as a voltage-limiting network. Quiescent condition is with transistors Tr_1 and Tr_3 off, Tr_2 and Tr_4 on. A negative-going pulse at the trigger-input terminal which is coupled to the base of Tr_3 via diode-connected transistor Tr_7. Hence Tr_2 (and Tr_4) cut off and V_{out} rises to $+V_S$. Because Tr_2 and Tr_1 are emitter-coupled, Tr_1 can now conduct when Tr_2 is off, therefore the voltage across C_3 i.e. is near ground. Capacitor C_3 now charges via R_3. When the base potential of Tr_2 is high enough to bring it into conduction, Tr_1 again goes off and V_{out} drops to its normal value of about 1.8V.

Time duration is $t \approx 0.47R_3C_3$.

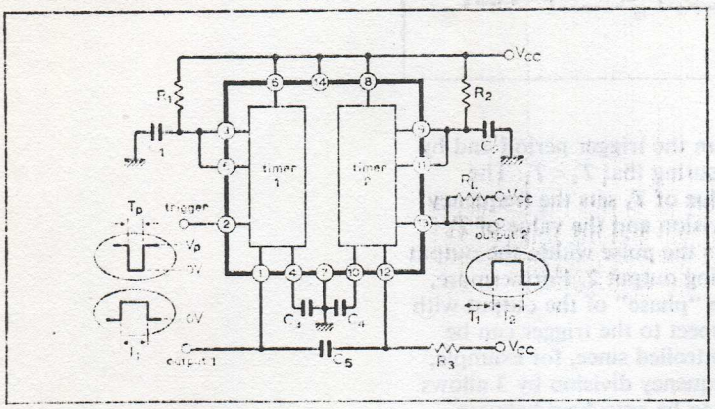
Cross references

Set 18, cards 5, 9.

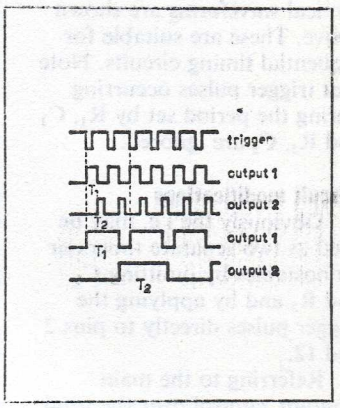
Further reading

Unijunction Transistor Timers and Oscillators. Motorola application note AN-294.

Dual monostable applications using 555 timer

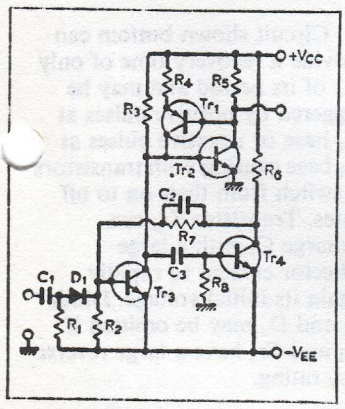


Typical performance
Vcc: 10V (range 4.5 to 16V)
Output pulse height: 9.3 to 9.9V
C_3, C_4: 10nF
C_5: 1nF
R_L: 470Ω
R_3: 33kΩ
T_1: $1.1R_1C_1$
T_2: $1.1R_2C_2$
V_p: Vcc
IC: XR2556

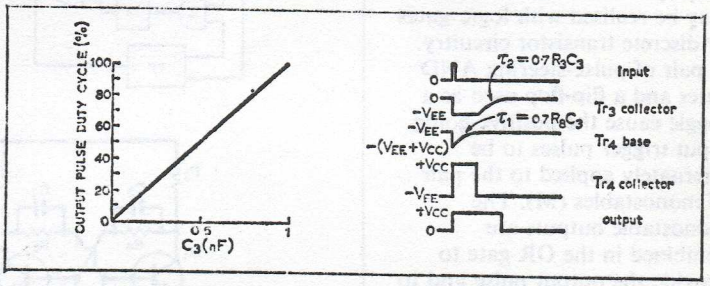


Circuit description
The i.c. shown is a dual 555-type timer (internal details of which are shown in cross references 1 and 2). In this application the output of the first timer is capacitively coupled via C_5 to the input of the second. Both timers are triggered when the input to each drops below $\frac{1}{3}V_{CC}$. In this case the trigger pulse operates timer 1 and the output of timer 1 triggers timer 2. Both timers are connected in their monostable mode. Formulae for T_1 and T_2 quoted are valid for all conditions and are fixed entirely by the external R_1, C_1 and R_1, C_2. Any succeeding trigger pulses are ignored. Both T_1 and T_2 can be anywhere in the range 10μs to 100s with two provisos: T_1 cannot be reduced below T_p, but since T_p can be less than 3μs this is not serious. Secondly low values of T_1 and T_2 should not be obtained by reducing R_1 and R_2 to a level at which current drain from the supply is serious. A minimum value of 1kΩ is

High duty-cycle monostable



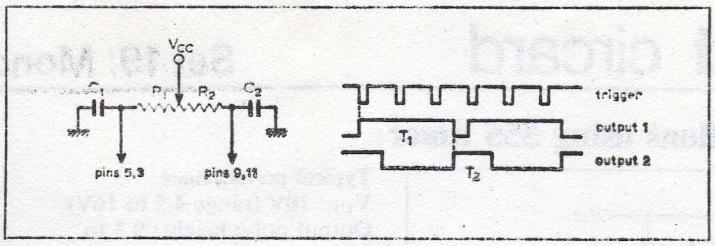
Typical performance
Vcc: +6V, 6 to 18mA*, V_{EE} −6V, 6 to 12mA*
Tr_1: BC126, Tr_2, Tr_3, Tr_4 BC125
R_1: 10kΩ, R_2, R_7: 56kΩ
R_3, R_8: 47kΩ, R_4: 1.8kΩ
R_5, R_6: 1.2kΩ, C_1, C_2: 100pF
C_3: see graph opposite; D_1 PS101
Input: 4V positive pulses, pulse width 1μs, p.r.f. about 10kHz
Output rise time: 0.5μs
Output fall time: 0.2μs
*depending on value of C_3.



Circuit description
In this circuit the timing capacitor C_3 not only determines the width of the output pulse obtained from Tr_2 collector but also delays the setting-up of the circuit in readiness for the next cycle of operations. This prevents an early trigger pulse from producing an output pulse having too short a duration. Because the circuit may be re-triggered immediately after completing its cycle, an output-pulse duty cycle approaching 100% may be obtained. The conventional "cross-coupled" monostable allows only about 95% duty cycle, even when its timing capacitor is rapidly recharged from a low-resistance source. In the stable state, Tr_3 is biased off and Tr_1, Tr_2 and Tr_4 are on. Input trigger pulses are differentiated by C_1 R_1, the positive component passing to Tr_3 base via D_1. If of sufficient amplitude, these overcome the reverse bias on Tr_3, which switches on, Tr_1, Tr_2 and Tr_4 switching off. Transistor Tr_4 remains off for approximately 0.7τ, as its base potential rises under the control of C_3. When Tr_4 turns on again, Tr_3 collector potential rises as C_3 recharges with time constant $\tau_2 = C_3 R_3$ until it exceeds approximately 0 V. Transistor Tr_2 and hence Tr_1 then switch on regeneratively and the circuit returns to its stable state and may be re-triggered immediately.

Component changes
Minimum useful supplies ±2 V
Useful range of R_1: 1k to 100kΩ
Useful range of R_2: 1k to 470kΩ
Minimum trigger pulse amplitude approximately 2.5 V
Minimum trigger pulse width less than about 0.1μs
Maximum useful p.r.f.: 200kHz.

recommended for both R_1 and R_2.
The only restriction on R_L is that it must not be so low as to exceed the current rating (200mA) of the i.c.
Typical waveforms are shown above. These are suitable for sequential timing circuits. Note that trigger pulses occurring during the period set by R_1, C_1 and R_2, C_2 are ignored.



Circuit modifications

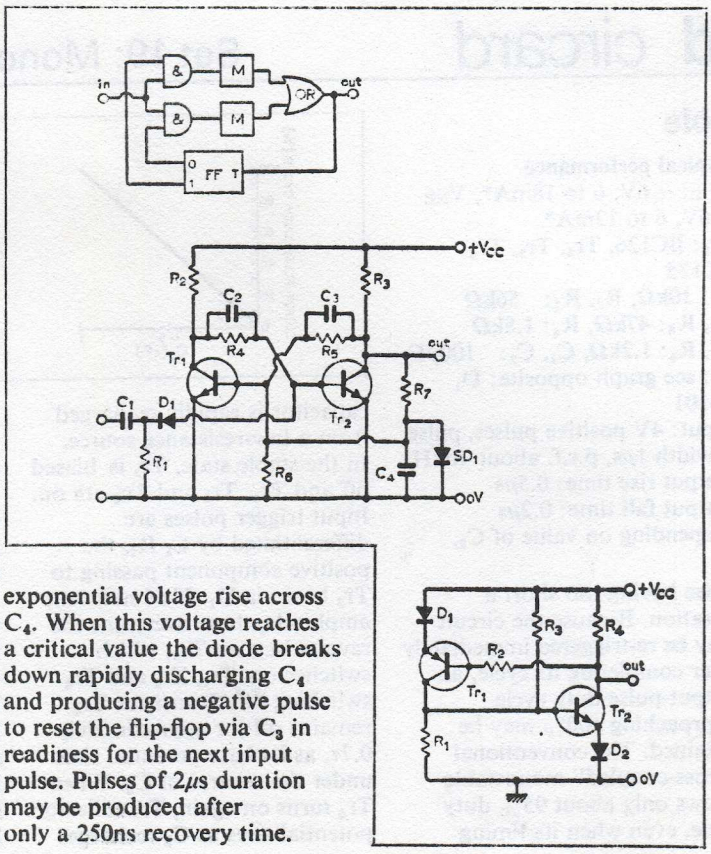
- Obviously the i.c. may be used as two separate timers or monostables by omitting C_5 and R_3 and by applying the trigger pulses directly to pins 2 and 12.
- Referring to the main diagram, control over the total period ($T_1 + T_2$) can be achieved by connecting the arm of a potentiometer to Vcc and the ends to pins 3 and 9, R_1 and R_2 being now the two segments of the potentiometer shown above. If $C_1 = C_2 = C$ then $(T_1 + T_2) = C(R_1 + R_2)$ which is constant no matter the individual T_1 and T_2.
- Each individual timer can be regarded as a frequency divider in its own right. For example, in the waveforms shown over, the lower two graphs indicate that output 1 is running at half the trigger pulse frequency and output 2 is running at half the frequency of output 1. By correct choice of T_1 one can make output 1 run at any submultiple frequency of the trigger and likewise with correct choice of T_2 output 2 can run at any submultiple frequency of output 1.
- A combined frequency divider and pulse width controller can be achieved by setting T_1 so that it is greater than the trigger period and by ensuring that $T_2 < T_1$. The value of T_1 sets the frequency division and the value of T_2 sets the pulse width, the output being output 2. Furthermore, the "phase" of the output with respect to the trigger can be controlled since, for example, frequency division by 3 allows T_1 to lie anywhere between two and three trigger periods. See waveforms above.

Further reading
XR-2556 Dual Timing Circuit, data sheet/application note, Exar Integrated Systems Inc.

Cross references
Set 3, card 9
Set 13, cards 3 and 5

Circuit modification

- The circuit shown top is a logical representation of a high duty-cycle monostable which may be realised with logic gates or discrete transistor circuitry. A pair of pulse-steering AND gates and a flip-flop used as a toggle cause the positive-going input trigger pulses to be alternately applied to the pair of monostables (M). The monostable outputs are combined in the OR gate to provide the output pulse and to toggle the flip-flop which changes state when the output pulse is completed. Hence, the start of the next output is only delayed by the time taken for the flip-flop to change its state, which can be a small percentage of the output pulse duration. A discrete version produced 700ms pulses every 705ms.
- Circuit shown next uses a flip-flop in conjunction with a Shockley diode (SD1) to achieve a high duty cycle. An input pulse causes the flip-flop to change its state producing an exponential voltage rise across C_4. When this voltage reaches a critical value the diode breaks down rapidly discharging C_4 and producing a negative pulse to reset the flip-flop via C_3 in readiness for the next input pulse. Pulses of 2μs duration may be produced after only a 250ns recovery time.



Typically, R_1, R_6 1MΩ, R_2, R_3 10kΩ, R_4, R_5 150kΩ, R_7, 2.2MΩ, C_1, C_2, C_3 20pF, C_4 500nF, D_1 1N914, SD1 4E20-8, with Vcc +25V.

- Circuit shown bottom can provide a recovery time of only 1% of its period and may be triggered by positive pulses at Tr_1 base or negative pulses at Tr_2 base causing both transistors to switch from their on to off states. Transistor Tr_1 can recharge C_1 with a large collector current to rapidly regain its initial voltage. Diode D_1 and D_2 may be omitted if Tr_1 and Tr_2 have a large reverse V_{BE} rating.

Further reading
Shagena, J. L. & Mall, A. Single-shot multivibrator has zero recovery time, *Electronics*, 27 Nov., 1967, p. 83.
Electronic Circuit Design Handbook, 4th edition, Tab, 1971, pp. 85, 96, 342/3.

Cross reference
Set 19, card 9.