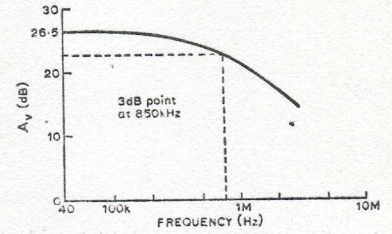
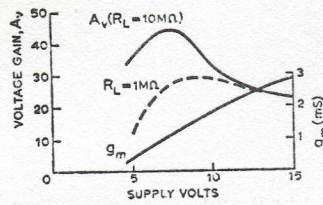
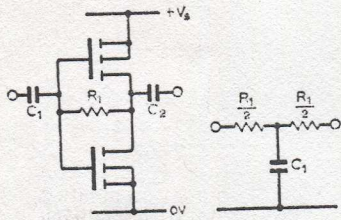


High input impedance c.m.o.s. amplifier



Circuit description

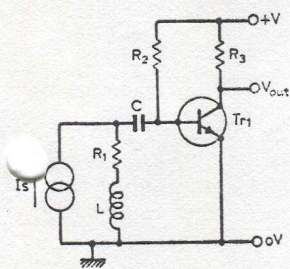
C.m.o.s. circuits have been designed for digital systems. Basic building block is the inverter consisting of a complementary pair of enhancement-mode m.o.s. devices with threshold voltages in the region of 1.7V and peak current capabilities of a few tens of milliamperes at maximum forward bias. Input resistance is extremely large with the leakage currents of the junction diodes as the limiting action. The individual device g_m is around 1 to 2mS for forward gate-source voltages in excess of 5V. Biased in the linear mode, the devices each have $|V_{GS}| \approx V_s/2$, so maximum forward bias is $\approx 7.5V$ for the rated supply voltage of 15V. This restricts the upper value of g_m that can be attained. In the absence of an external load resistance the voltage gain is limited by the finite slope resistance. An unusual property of this circuit is that the voltage gain falls

with increasing supply voltage, as the relatively small rise in g_m is more than offset by the fall in output slope resistance at the higher resulting currents. The disadvantage of operating at low supply voltages (and hence currents) is that the voltage gain is more load-dependent and the upper cut-off frequency falls sharply. To maximize the input resistance while using d.c. negative feedback to stabilize the operating point, the feedback resistor is decoupled to ground. Gate current is negligible and the input and output quiescent voltages are equal.

Other c.m.o.s. devices using different technologies, e.g. silicon gate, ion implantation, offer greater bandwidths and/or lower threshold voltages. Complementary m.o.s. circuits designed for the linear market have been recently announced.

Wireless World Circard

Shunt-peaked wideband amplifier

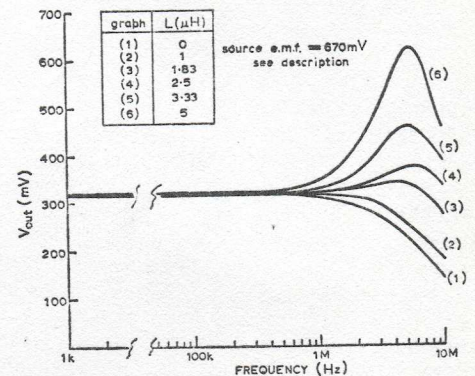


Circuit data/
 Supply: +6V, 4.5mA
 Tr_1 : 1/5 CA3046
 C: 10 μ F tantalum
 R_1 : 68 Ω ; R_2 : 100k Ω
 R_3 : 680 Ω
 L: 1.83 μ H (38 turns 28 swg, close wound on 0.2in dia.)

Circuit description

Bandwidth of a common-emitter amplifier may be extended by including an inductor in shunt with its input producing a shunt-peaked amplifier. The circuit is fed from a current source, or alternatively in a cascaded amplifier R_1 and L may be used as the collector coupling network of each stage which is loaded by the input impedance of the following transistor.

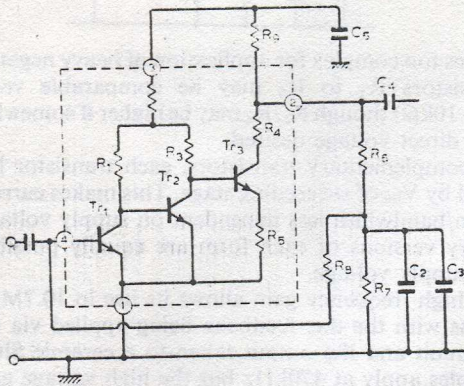
Because the gain-bandwidth product of a transistor varies with its collector current, R_2 was chosen to maximize the gain-bandwidth product for the device used. Resistor R_3 was chosen to make $V_{CE} \approx +V/2$ and R_1 to provide the desired low-frequency current gain. Source resistance was 100 Ω , so a current source was simulated by a chain of ten 1-k Ω resistors in series to reduce the effect of the shunt capacitance of a single 10-k Ω resistor on the measured high-frequency response.



With $L=0$, amplifier input voltage falls with increasing frequency due to transistor input (and Miller effect) capacitance. With L in circuit, low-frequency response is the same but a low-Q resonance occurs between L and C_{in} of the transistor, causing the response to peak as the frequency is raised towards its original cut-off value.

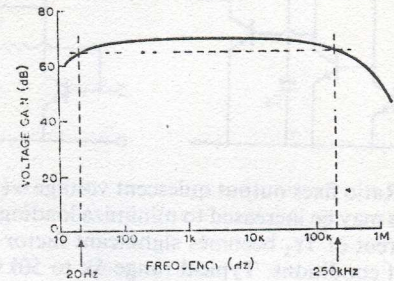
By designing L on the basis of available transistor parameter data and the required current gain, it is possible to produce a maximally-flat gain response while maximizing stage gain-bandwidth product. Alternatively, a good starting point is to use the measured low frequency input resistance and upper cut-off frequency with $L=0$ to estimate C_{in} and then design L to resonate with this value in the region of the desired cut-off frequency with the peaked response. (See curve 3 above.)

High-gain wideband amplifier



Circuit description

This amplifier uses an integrated circuit developed for consumer applications. It is simple in design, consisting of three common-emitter transistors directly coupled so that the collector potentials of Tr_1 , Tr_2 are defined by the base potentials of Tr_2 , Tr_3 respectively, i.e. they are at $\approx 0.6V$. Resistor R_5 has a low value with only a marginal effect on these potentials. Output potential is forced by the feedback effect via R_6 , R_7 , R_8 to be some defined multiple of the base potential of Tr_1 . If $R_5 < R_6$, R_7 then the output p.d. to ground is $\approx (R_6/R_7 + 1)V_{be1}$ and would typically be set near the supply mid-value. Current in each stage increases with increasing supply voltage, and as a result both open-loop gain and bandwidth increase. In-

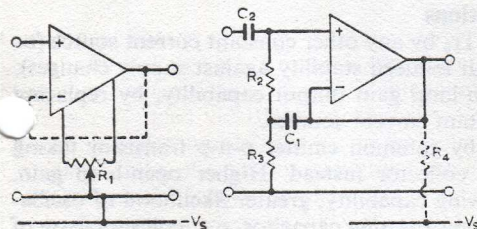


creased current also reduces the input impedance. Resistor R_9 determines quiescent output current provided output voltage has been fixed by feedback as outlined above. As there are three stages all contributing phase shift, the total phase-shift is in excess of 180° before the magnitude of the gain falls towards unity. Hence it is difficult to apply heavy negative feedback to extend the bandwidth at the expense of gain as can be done with amplifiers single common-emitter stages. (For audio frequency applications it is possible to control the feedback to produce defined characteristics as for tape recording/playback amplifiers.) As the high gain extends to high frequencies, $A_v \approx 100$ at $f=4MHz$, proper grounding, decoupling and use of short leads, screened where appropriate are all important.

Component changes

IC: No direct replacements but groups of three transistors from CA3046 and similar multi-transistor packages may be used.

Wideband voltage followers



Circuit data
 IC: LM310
 R_1 : $1k\Omega$
 R_2, R_3 : $100k\Omega$
 R_4 : $3.3k\Omega$
 C_1 : $2.2\mu F$
 C_2 : $0.01\mu F$
 Supply: $\pm 15V$

Circuit description

A specially-designed monolithic voltage-follower, the 310 has a combination of highly desirable parameters: high input impedance, low output impedance, and wide frequency range. The negative feedback is connected internally but some modifications to performance that can be made externally include offset zero by means of R_1 , increased output current capability by preloading with R_4 at the expense of increased dissipation, and a.c. coupling to source, bootstrapping the bias resistors R_2 , R_3 to minimize loading effects.

Slew-rate limitations imposed by the maximum charging rate of an internal compensation capacitor, mean that the large signal bandwidth is much less than small signal bandwidth—true of amplifiers having heavy negative feedback in general.

Performance

Upper cut-off frequency for small signals. 15MHz for zero source resistance, 2MHz for $10k\Omega$. At 1MHz, output impedance is 25Ω , output voltage swing is $\pm 3V$, and input impedance is $3pF$ plus strays.

Component changes

IC: Direct replacements from many manufacturers. Any op-amp compensated for 100% negative feedback may be used. In general it will not be possible to achieve the same spread of parameters, i.e. high input impedance may preclude wide bandwidth.

R_2, R_3 : Increase for higher Z_{in} at expense of increased offset.
 C_2, C_1 : Determine lower cut-off frequency (with R_1, R_3). Combination gives inductive term to input impedance at low frequencies. 0.1 to $10\mu F$.

R_4 : Increases negative current capability at expense of dissipation.

V: ± 5 to $\pm 15V$ (down to $\pm 3V$ in extreme cases).

Further reading

LM110—An Improved IC Voltage Follower, National Semiconductor Linear Applications Handbook, 1972, p.LB11-1 and 2.

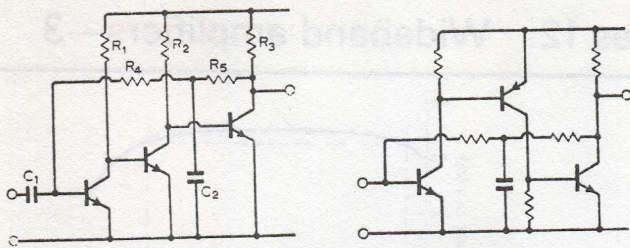
Campbell, T. C. Application note ICAN-5213, in RCA Databook SSD-202, 1972, pp.203-4.

Markus, J. Electronic Circuits Manual, McGraw-Hill p.13.

Cross references

Series 12, cards 1 & 11.

Series 7, card 3.



R_6, R_7 : Ratio fixes output quiescent voltage $\approx (R_6/R_7 + 1)0.6V$. Resistors may be increased to minimize loading on output, but base current of Tr_1 becomes significant factor in determining quiescent conditions. Typical range 5k to 50k Ω .

R_8 : Also limited by base current effects, but may be increased up to 10k Ω to maximize input resistance of circuit if required.

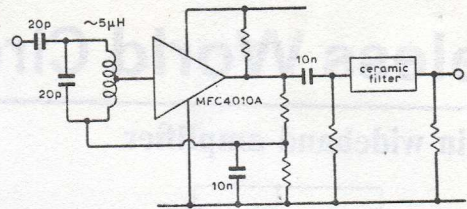
R_9 : Determines output stage quiescent current and hence maximum load current. No advantage to making too high since current in preceding stages fixed by internal resistors. 2.2k to 22k Ω .

$+V_s$: 2 to 18V. At low voltages, gain falls sharply. Choose R_6, R_7 in conjunction with V_s to bias output near mid-point of supply for maximum output swing.

C_1, C_3, C_4 : Determine low frequency cut off. Maintain ratio increasing values for pro rata fall in cut-off. C_4 may be reduced greatly if feeding high impedance load.

Circuit modifications

Any group of three transistors may be used in similar configurations. Simple arrangement shown for low-voltage applications where output quiescent voltage of 0.6V would be adequate. Again decoupling of feedback essential since gain/



phase properties too complex for application of heavy negative feedback. Resistors R_1 to R_5 may be comparable value resistors (1k to 10k Ω) though R_4, R_5 may be higher if somewhat higher output direct voltage desired.

- By using complementary transistors, each transistor has current defined by V_{be} of succeeding stage. This makes current and hence gain/bandwidth less dependent on supply voltage. Complementary versions of each form are equally possible, reversing the supply voltage.

- The good high frequency gain allows its use in 10.7MHz i.f. applications with the d.c. feedback being applied via the input tuned circuit and the output taken to a ceramic filter. Similar principles apply at 470kHz but the high voltage gain makes careful design obligatory. In all r.f. applications drive from a 50 Ω source is normal, but the output impedance of the circuit is relatively high.

Further reading

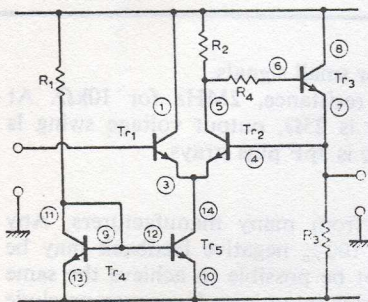
Motorola Linear Integrated Circuits Data Book, 2nd edition 1972, pp.7-561 to 7-564.

CA3095E Wideband Amplifier, RCA Databook SSD-201A, 1973, p.249.

Cross references

Series 12, cards 5, 10 & 11.

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Circuit data

Tr_{1-5} : CA3046

R_2 : 3.9k Ω

R_1 : 4.7k Ω

R_3 : 1k Ω

R_4 : 1k Ω

Supply: $\pm 2.5V$

Circuit description

Using the five transistors in an i.c. package (CA3046), this is a simple wide-band voltage follower. A similar circuit could be used with discrete transistors replacing current mirror Tr_4, Tr_5 by a similar current source or by a single resistor particularly if the supply voltages were higher. Transistors Tr_1, Tr_2 are the differential pair comparing input with output, the use of a monolithic pair giving good temperature drift. Transistor Tr_3 is an emitter follower within the feedback loop. Resistor R_4 may be required to suppress very high frequency oscillations (dependent on circuit layout). Not shown, but generally important, is the decoupling of the supply voltages as close to the i.c. as possible—typically 0.01 to 1 μF .

Performance

Upper cut-off frequency $\approx 4.5MHz$

Output impedance $\approx 10\Omega$

Input impedance: $\approx 100k\Omega$

Output voltage swing $\approx 2.5V$ pk-pk at 100kHz

Circuit modifications

- Replace Tr_4, Tr_5 by any other constant current source (or even resistor, with reduced stability against supply changes).
- Increase open-loop gain output capability, by replacing R_2, R_3 with constant current sources.
- Replace Tr_3 by common emitter p-n-p transistor taking signal from Tr_1 collector instead. Higher open-loop gain, greater output swing capability, greater likelihood of oscillations requiring compensating capacitor, e.g. collector-base of Tr_3 .

Component changes

IC: CA3546, CA3045, CA3586.

R_1 : 1k Ω to 100k Ω . Lower values increase bandwidth and dissipation.

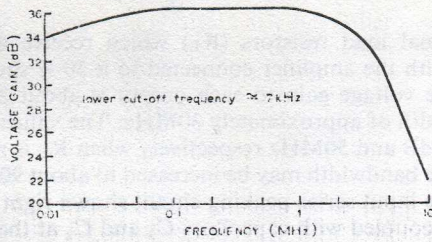
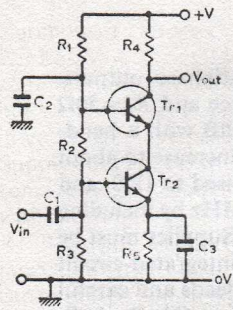
R_2 : Set to carry half current in R_1 (assuming unity ratio for current mirror). Typically $R_1 \approx R_2$.

R_3 : Low values maximize output swing and dissipation 330 Ω to 33k Ω .

V: ± 2 to $\pm 7\frac{1}{2}V$. Higher voltages possible if discrete transistors used.

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Bipolar cascode wideband amplifier



Circuit description

The bipolar transistor cascode amplifier offers very good isolation between its input and output ports, so that the possibility of instability is virtually non-existent for all types of load. Input transistor Tr_2 acts as a common-emitter stage which is loaded by the upper transistor connected in the common-base configuration and having a very low input impedance. Thus the common-emitter stage has a current gain approaching h_{fe} and the voltage swing at its collector is very small, producing a significant reduction of the internal feedback between collector and base. Bandwidth of the common-emitter stage approaches f_β and as that of the common-base stage is much larger, the complete circuit behaves like a common-emitter amplifier as far as voltage gain and current gain are concerned, but has a wider bandwidth than is achiev-

Circuit data

Supply: +6V, 1.2mA
 Tr_1, Tr_2 : $1/5 \times CA3046$
 R_1 : 39k Ω ; R_2 : 3.3k Ω

R_3 : 33k Ω ; R_4 : 2.2k Ω
 R_5 : 1k Ω
 C_1, C_2, C_3 : 1 μ F
 V_{in} : 10mV r.m.s.

able with a simple common-emitter stage providing the same high voltage gain.

A reasonable estimate of the 3-dB bandwidth obtainable with the cascode amplifier may be made using available data and the relationship: gain-bandwidth product (f_T) $\approx h_{fe} \cdot f_\beta$ if it is assumed that h_{fe} and f_β are the approximate current gain and bandwidth values for the whole circuit. Each of the transistors in the integrated circuit array has typical h_{fe} and f_T values of 110 and 450MHz respectively, with $I_C \approx 1.2mA$ giving $f_\beta \approx 4.1MHz$. (Measured upper 3dB cut-off frequency was approximately 3.7MHz for the circuit.)

Component changes

Useful range of supply +2 to +30V.

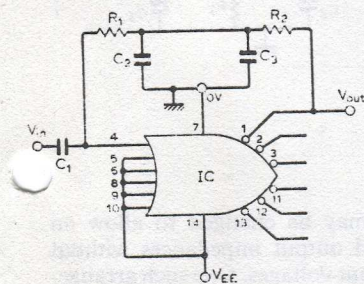
$V_{in(max)} \approx 40mV$ (pk-pk).

Midband gain falls by 3dB when output is loaded with approximately 6.8k Ω (capacitively coupled).

Upper cut-off frequency largely determined by R_4 for given transistors.

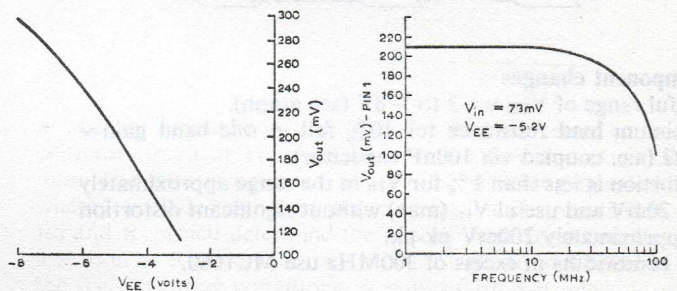
Lower cut-off frequency adjustable by changing C_1, C_2 and C_3 . Tr_1 and Tr_2 may each be replaced by $1/4 \times CA3018$ or equivalent discrete devices e.g. 2N706-type.

Wideband amplifier using e.c.l.



Circuit description

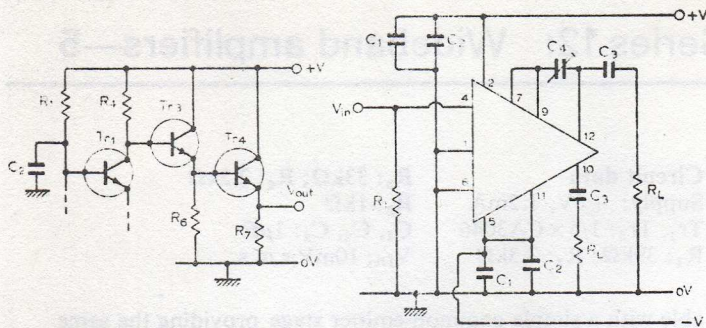
The integrated circuit is an emitter-coupled logic gate designed for high-speed digital applications. This type of gate has an input stage consisting of a long-tailed pair with multiple inputs to one half of the pair via separate transistors having their collector-emitter paths in parallel. Each half of this differential stage feeds an emitter follower output stage, a number of which may be paralleled within the package. Thus, at least one inverted and at least one non-inverted output is available and the logic gate may be used as a linear, wideband amplifier provided it is correctly biased, for example by means of R_1 and R_2 as shown above. This simple arrangement of connecting one of the logical NOR outputs back to the input provides self-biasing of the gate that ensures that the d.c. input and output voltages are the same except for the small drop



across R_1 and R_2 . This is only possible if the gate is operating in the middle of its transfer characteristic, the arrangement automatically compensating for changes in bias and offset voltages.

Only the d.c. component of the output signal is fed back to the input, C_2 and C_3 decoupling the a.c. component. Capacitor C_1 prevents any d.c. component of the input signal from disturbing the self-biasing conditions. The a.c. signal voltage available at the NOR output being used to derive the feedback, is typically 3 to 4% lower than that obtainable from other NOR outputs is approximately 9 to 10%, higher than at the unloaded NOR outputs.

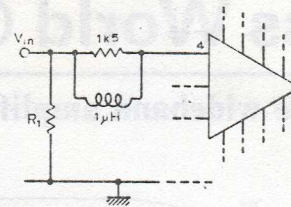
Careful printed circuit layout is required if a smooth, high-frequency roll-off is to be obtained in the frequency response.



Circuit modifications

- One of the differentially-connected pair of transistors in the CA3046 package may be connected as an output emitter-follower stage to provide a low output impedance cascode amplifier. If a CA3018 package is used, all four transistors may be used by following the cascode with a pair of cascaded emitter followers as shown left. In this form, with $R_6=3.3k\Omega$ and $R_7=2.7k\Omega$ a voltage gain of about 36dB is obtainable with an upper cut-off frequency of approximately 11MHz.
- A pair of cascode stages with a common tail resistor may be used as a differential cascode amplifier. This arrangement is the basis of the CA3040 integrated circuit wideband amplifier, which employs high-input-impedance emitter-follower buffer stages between the input terminals and the common-emitter sections of the cascodes. Outputs from the cascode common-base stages are fed to the output terminals via emitter followers to produce a reasonably low output impedance.

- Centre circuit shows the CA3040 connected to a pair of



equal load resistors (R_L) which receive antiphase outputs. With the amplifier connected to a 50Ω source and $R_L=50\Omega$ the voltage gain to each output is about 22dB with a bandwidth of approximately 30MHz. The values increase to about 32dB and 50MHz respectively when R_L is raised to $1k\Omega$ and the bandwidth may be increased to about 90MHz by including the input series peaking circuit shown right. Supplies must be decoupled with capacitors C_1 and C_2 at the integrated-circuit package pins and ferrite beads on the supply leads and careful printed circuit layout are necessary. Supply $\pm 6V$, R_1 50Ω , C_1, C_3 100nF, C_2 1nF, C_4 is a small trimmer to adjust high-frequency gain and phase balance.

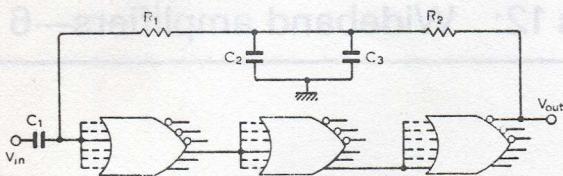
Further reading

- Theriault, G. E. et al. Application of the RCA-CA3018 Integrated-Circuit Transistor Array, RCA Databook SSD-202 1972, pp.68-70.
- Austin, W. M. Principal Features and Applications of the RCA-CA3040 Integrated-Circuit Wideband Amplifier, RCA Databook SSD-202, 1972, pp.171-81.
- Ghausi, M. S. Electronic Circuits, Van Nostrand, 1971, pp.271-3.

Cross references

- Series 12, cards 2, 3, 7 & 12. Series 7, card 5.

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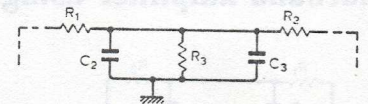
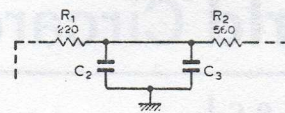


Component changes

- Useful range of $V_{EE} \approx -3$ to $-8V$ (see graph).
- Minimum load resistance for 10% fall in mid-band gain $\approx 270\Omega$ (a.c. coupled via 100nF capacitor).
- Distortion is less than 1% for V_{in} in the range approximately 1 to 20mV and useful V_{in} (max) without significant distortion is approximately 200mV pk-pk.
- For bandwidths in excess of 300MHz use MC1660.

Circuit modifications

- More than one input of the gate may be used to increase gain by connecting others in parallel, but the offset voltage between output and input rises as the number of paralleled inputs increases. This may not be a severe disadvantage in certain applications.
- The simple self-biasing arrangement may be applied over several e.c.l.-gate amplifying stages, as shown left.
- A given total bias network resistance (R_1+R_2) may be decoupled asymmetrically. For example, if it is required that the bias-network loading of the output be reduced without changing (R_1+R_2), values such as those shown centre may be used. This will cause the input impedance of the amplifier to fall from about 390Ω to about 220Ω .



- The biasing arrangement may be changed to allow an increase in both the input and output impedances without changing the d.c. input and output voltages. One such arrangement is shown right, where the junction of R_1 and R_2 may be returned to the 0-volt rail through a suitable-value, additional bias resistor R_3 . For example, with R_1, R_2 $2.2k\Omega$, a suitable value for R_3 would be around $47k\Omega$. This arrangement slightly increases voltage gain.

Further reading

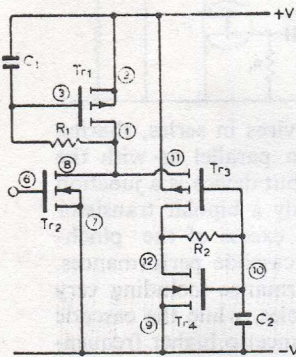
- Using e.c.l. gates as wideband amplifiers, *Electronic Engineering*, June 1973.
- MECL Integrated Circuits Data Book, Motorola, 2nd edition, 1972, pp.5-3 to 5-6 and pp.4-17 to 4-20.

Cross references

- Series 11, card 7.
- Series 12, cards 8 & 10.

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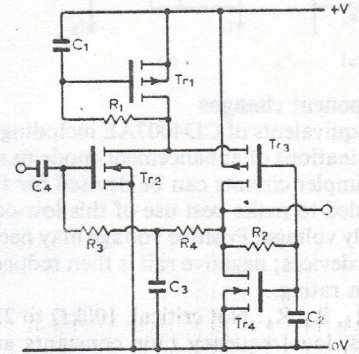
FET cascode amplifiers



Circuit data
 Supply: $\pm 7.5V$
 IC: CD4007AE
 $R_1, R_2: 1M\Omega$
 $C_1: 0.1\mu F; C_2: 0.33\mu F$
 Voltage gain: ≈ 26
 Cut-off frequency:
 320kHz
 Alternative bias for single supply: $R_3, R_4: 1M\Omega$
 $C_3: 1\mu F; C_4: 0.01\mu F$

Circuit description

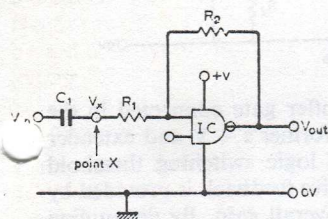
The basic principle of a cascode stage is that of a common-emitter or common-source amplifier feeding directly into a common-base or common-gate stage, so that the first stage feeds into a near short-circuit. This allows it to develop its maximum current gain or transconductance, but more important the voltage swing at the collector or drain is small. Large voltage swings produce relatively large currents in the inevitable feedback capacitance, with a corresponding heavy shunting effect at high frequencies. This reduction in feedback (commonly called the Miller effect though first discussed by Blumlein) is of particular importance in wideband and r.f. amplifiers. In particular, the better the isolation between input and output the higher the gain that can be achieved



consistent with stability. The devices need not be in series for d.c. purposes though this is more common. In the circuit shown, based on a low-cost c.m.o.s. i.c., Tr_2 is a common-source stage whose output signal current is diverted into Tr_3 provided that Tr_1 has a high dynamic impedance at a.c. (see circuit modifications). The voltage gain of the cascode pair is equal to or greater than the highest voltage gain obtainable from a single stage, while coupling between output and input is minimized.

An alternative version is shown in which a decoupled d.c. feedback path via R_3, R_4 gives self-biasing (with a.c.-coupled source). The high input resistance of the m.o.s. devices together with the possibility of operation at $V_{dg}=0$ allows for simple biasing networks and offsets the disadvantage of the wider tolerance on m.o.s. devices as against bipolar transistors.

Wideband amplifiers with t.t.l., r.t.l., d.t.l.

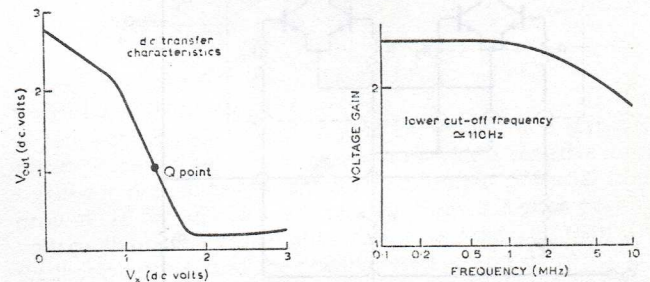


Circuit data
 Supply: 5V, 19mA
 IC: $1/4 \times SN7400$
 $C_1: 10\mu F$ tantalum
 $R_1: 220\Omega; R_2: 560\Omega$
 $V_{in}: 50mV$ r.m.s.

T.t.l. gate description

Without the use of negative feedback, the normal transfer characteristic of the t.t.l. gate is designed to provide well-defined logic levels with a high-gain transition region between them causing the gate normally rest in either the on or off condition. Compared with the static on or off state, the supply current drain increases sharply as the gate is switched through the narrow transition region. Although designed for medium-speed digital switching applications a t.t.l. NAND gate can be converted into a linear wideband amplifier. By addition of R_1 and R_2 , as shown, the shunt-derived shunt-applied negative feedback has the effect of linearizing the overall d.c. transfer characteristic, eliminating the well-defined logic states, widening the transition region, reducing the gain, and increasing the standing supply current.

Thus, a suitable operating point may be established, with a quiescent supply current of about 19mA, which will allow



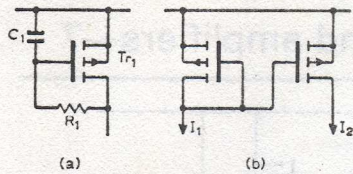
linear amplification of input signals having levels up to about 800mV pk-pk in the frequency range of approximately 100Hz to 12MHz. Unused gate inputs may be paralleled with the used input rather than being left open-circuit. Alternatively, a logic signal may be applied to the unused input to provide a gating facility on the used input's signal.

Component changes

Useful range of supply +3 to +5.5V.

Changing R_2 varies gain, shape of the transfer characteristic, and signal-handling capability.

In principle, all four gates in the package may be used simultaneously for linear amplification but the package dissipation is then far in excess of that when used for logic operation.



Component changes

IC: Equivalents of CD4007AE including MC14007, etc. Other combinations of enhancement-mode m.o.s.f.e.t.s may function but simpler circuits can be devised for these. This circuit was intended to make best use of this low-cost i.c.

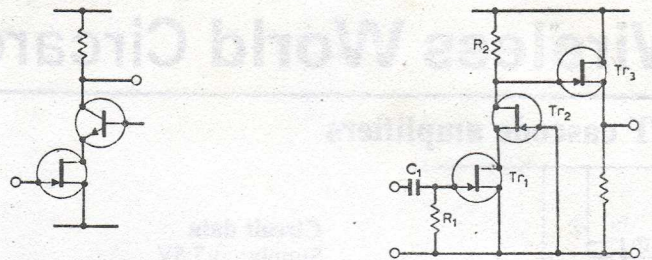
Supply voltage: Positive voltage may need to be increased with some devices; negative rail is then reduced accordingly to stay within rating.

R₁, R₂, R₃, R₄: Not critical. 100kΩ to 22MΩ. With low resistances, low-frequency time constants are raised unless large capacitances used, while input impedance falls for second version. Very high resistances bring noise/hum/leakage problems.

C₁, C₂, C₃, C₄: High values to improve low-frequency response if required.

Circuit modifications

• The high impedance of the circuit is possible because the p-channel enhancement-mode m.o.s.f.e.t. can still have the drain well beyond the knee of its characteristics if biased with drain and gate at equal quiescent potentials. Provided the a.c. applied to the drain is adequately decoupled by R₁C₁, the dynamic impedance approaches that of the drain-source (R₁ may be very large and still achieve correct bias). The current mirror approach retains the high dynamic resistance down to d.c. at the expense of a second m.o.s.f.e.t.



• Cascode circuits may have the devices in series, sharing the same d.c. current (rather than in parallel as with the complementary stage above). If the input device is a junction f.e.t., the simplest circuits demand only a bipolar transistor with base potential set to a value in excess of the pinch-voltage of the f.e.t. to achieve good cascode performances. The f.e.t. determines the input performance including very high input impedance at low frequencies, while the cascode configuration extends the high impedance to higher frequencies while allowing higher overall gain.

• All f.e.t. circuits are equally possible provided Tr₂ has a higher V_p than Tr₁. Transistor Tr₃ is a source follower to isolate the load R₂ from stray and load capacitances, i.e. increasing bandwidth of output circuit.

Further reading

FET Circuit Applications, National Semiconductor Linear Applications Handbook, 1972, p.AN32-2.

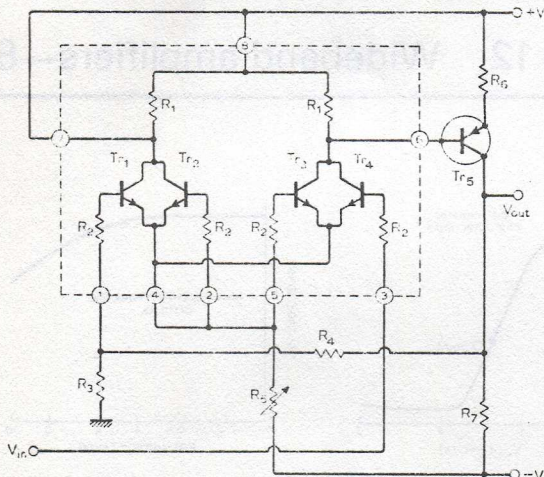
Schade, O. H. Jr. Application note ICAN-6080, in RCA Data Book SSD-203A, 1973, pp.299-300.

Cross references

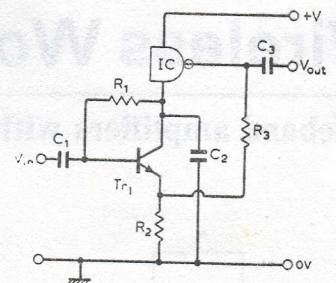
Series 12, cards 1 & 5, series 11, cards 5 & 6.

Series 7, card 5.

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R.t.l. and d.t.l. gate descriptions. A dual NAND/NOR r.t.l. gate, contained in a single 914 package (shown dotted), has Tr₁, Tr₂ and Tr₃, Tr₄ connected as a long-tailed pair with R₅ returned to the -V rail and serving as an approximation to a constant-current source (left). Transistor Tr₅ is used as an inverting output stage having a gain of two, with the output at its collector fed back to Tr₁ via R₄ and R₃. Thus, a non-inverted output is available for signals applied to Tr₄ base. The d.c. output voltage can be set to zero with the input grounded, by adjusting R₅. A gain of 10 with bandwidth greater than 10MHz is obtainable with a supply of ±6V, Tr₅ 2N3702, R₁ 640Ω, R₂ 450Ω (internal to 914), R₃, R₅, R₆, 1kΩ, R₄ 10kΩ, R₇ 2.2kΩ.



• Circuit right shows a d.t.l. buffer gate connected in the collector circuit of Tr₁ using the former's +V and extender pins. The gate is operated at its logic switching threshold where it provides high gain. Negative feedback is provided by R₂ and R₃ which determine the overall gain. By decoupling a section of R₂, the gain may be increased without affecting the d.c. operating conditions. A gain of 10, a bandwidth in excess of 500kHz and a load-driving capability of 1 volt into 300Ω is achievable with a supply of +5V, IC ½×932, Tr₁ 2N2222, R₁ 120kΩ, R₂ 120Ω, R₃ 1.1kΩ, C₁ 10nF, C₂ 100pF, and C₃ 10μF.

Further reading

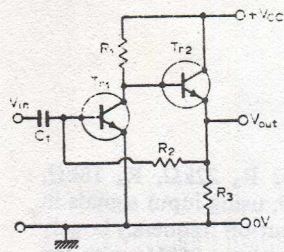
Kolataj, J. H. Linearize your t.t.l. gates—then build useful circuits with them, in 400 Ideas for Design, Hayden 1971, pp.2-3.

Klipstein, D. L. Build an operational amplifier from a dual NAND/NOR gate, in 400 Ideas for Design, Hayden 1971, p.21.

Jones, D. Wideband amplifier uses a single d.t.l. gate, in 400 Ideas for Design, Hayden 1971, p.23.

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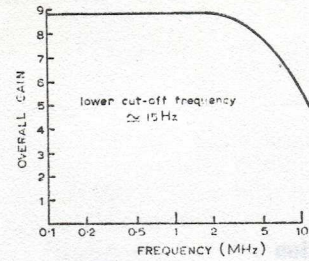
Amplifiers using d.c. feedback pair



Circuit data
 Supply: +5V, 6mA
 Tr₁, Tr₂: 1/5 × CA3046
 C₁: 10μF tantalum
 R₁: 3.9kΩ; R₂: 10kΩ
 R₃: 150Ω
 V_{C1}: 1.5V; V_{B1}: 0.67V
 V_{B2}: 0.77V
 Source e.m.f.: 50mV r.m.s.

Circuit description

Transistor Tr₁ is connected in the common-emitter configuration and feeds the emitter follower Tr₂ with overall shunt-derived shunt-applied feedback via R₂, which allows the overall gain and input impedance to be adjusted. If the circuit is supplied from an ideal voltage source the gain will be high and the bandwidth relatively small. Such a source could be heavily loaded when connected directly to the circuit shown above. This is due to the equivalent load on the source of h_{ie} of Tr₁ in parallel with R₂/(1 + |A_v|), where |A_v| ≈ g_mR_{L1}; R_{L1} is the equivalent load resistance seen by Tr₁. The signal generator available had an output resistance of 100Ω which approximately matched the input resistance of the amplifier. This can be seen to be reasonable assuming h_{ie} of Tr₁ to be approximately 2.5kΩ and |A_v| ≈ 80 with R_{L1} ≈ 3kΩ. To define the overall gain and input impedance and to provide a wider bandwidth a resistor may be included in series with C₁. Response shown applies with a 900-Ω resistance included and



the overall gain = V_{out}/source e.m.f. If it is desired to match the amplifier input resistance to a defined source resistance, this can be achieved using the circuit as shown above and adjusting the value of R₂.

The integrated-circuit package used contains a five-transistor array, two connected as a long-tailed pair. One of the single transistors has its emitter connected to the integrated circuit substrate which must be connected to the most negative supply rail, hence this transistor can be conveniently used as Tr₁ and any other as Tr₂. A discrete component version of the circuit is also viable.

Component changes

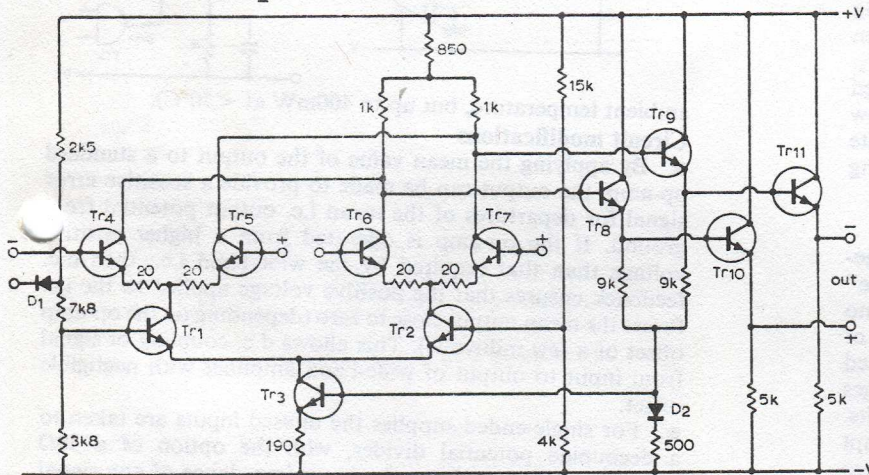
Useful range of V_{cc} ≈ +3 to +15V.

Maximum source e.m.f. 72mV r.m.s. with V_{cc} = +5V.

R₂ adjustable to provide desired overall gain, bandwidth of input impedance e.g. with R₂ = 47kΩ and circuit as shown above; overall gain ≈ 22 and bandwidth ≈ 3.4MHz.

Resistance values may be scaled by a given factor, e.g. increasing values by factor of 10: overall gain ≈ 28 and bandwidth ≈ 1MHz.

Gated video amplifier



Circuit description

The long-tailed pair is the key to the operation of this circuit, as of so many linear i.c.s. The V_{be}/I_C characteristic of a bipolar transistor is given by I_C = I_S exp(qV_{be}/kT). Transconductance is obtained by differentiating I_C with respect to V_{be}, and is found to be proportional to I_C. Thus controlling I_C gives proportional control of the voltage gain of an amplifier provided that the collector load is low enough to allow the full transconductance to be developed. Used with a single transistor an output signal may be gated on and off by such a

Circuit data

Supply: ±5V, 8mA

IC: MC1445L

Voltage gain: 19dB

Bandwidth: 60MHz

Output attenuation: 60dB with input gated off

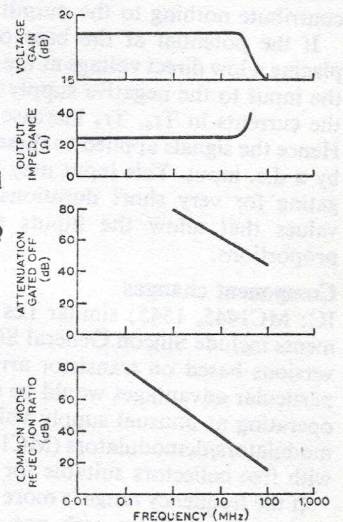
Input impedance: ≈ 8kΩ

Output impedance: ≈ 22Ω

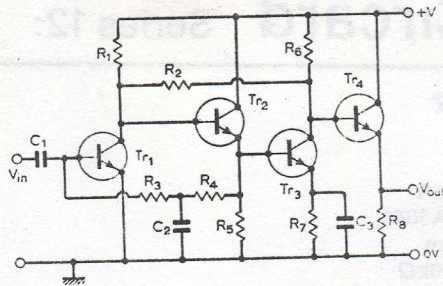
Input common-mode range: ±2.5V

Quiescent output voltage: ≈ 0.18V

Gate voltage range: 0.35 to 2.0V



means, but the shift in d.c. level carries the gate signal through into the output circuit. With long-tailed pairs as shown, Tr₃ sustains a constant total current using common-mode feedback via the emitters of Tr₈, Tr₉. If Tr₃ conduction increases the collector potentials of Tr₄, Tr₆ must fall regardless of which the current is channelled through. This fall in potential at each collector is coupled via the emitter followers Tr₈, Tr₉ to close the d.c. feedback loop and stabilize operating conditions. The base of Tr₂ is fixed while that of Tr₁ is normally more positive,



Circuit description

Another amplifier based on the configuration shown over, and also using an integrated-circuit transistor array is shown above. Transistors are contained in a single CA3018 package with Tr_2 emitter and Tr_3 base internally connected. The circuit arrangement of Tr_1 , Tr_2 serving as a common-emitter common-collector pair followed by Tr_3 , Tr_4 in the same configuration is designed to reduce internal capacitive feedback. The Tr_2 -emitter follower acts as a low output impedance source to drive the Tr_3 common-emitter stage and also provides a low-capacitance high-impedance loading on the Tr_1 common-emitter stage.

All stages are d.c. coupled with two negative feedback paths. Feedback from Tr_2 emitter to Tr_1 base is effective at d.c. and low frequencies while that from Tr_3 collector to Tr_1 collector functions at all frequencies. Feedback provides stability of d.c. operating conditions and allows a gain-bandwidth tradeoff to be made. When supplied from a 50- Ω source, a voltage gain of 49dB with a bandwidth of approximately 32MHz is obtainable with a supply of +6V, C_1 , C_2

$1\mu F$, C_3 470nF, R_1 3.5k Ω , R_2 8.2k Ω , R_3 22k Ω , R_4 18k Ω , R_5 1.8k Ω , R_6 2.5k Ω , R_7 1k Ω , R_8 2.7k Ω , using input signals in the range 7 μV to 4mV (r.m.s.). Lower cut-off frequency largely depends on the capacitors used and is about 800Hz with the above values.

Further reading

RCA Application note ICAN 5296, in Databook SSD-202, 1972, pp.68/9.

Cherry, E. M. and Hooper, D. E. Design of wide-band transistor feedback amplifiers, *Proc.I.E.E.*, vol. 110, 1963, pp.375-87.

Tuil, J. Transistor-equipped aerial amplifiers—wideband amplifiers, *Electronic Applications*, vol. 28, 1968, pp.75-8.

Cross references

Series 12, cards 2, 8 & 12.

Series 7, card 9

Series 4, card 4.

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ensuring that Tr_4 , Tr_5 are the conducting transistors, i.e. having sufficient g_m to give an overall voltage gain of 18 to 20dB. Transistor Tr_2 has negligible current and Tr_6 , Tr_7 contribute nothing to the output.

If the potential at the base of Tr_1 is lowered, either by placing a low direct voltage at the gate input (D_1), or by taking the input to the negative supply rail through a resistor, then the currents in Tr_6 , Tr_7 increase at the expense of Tr_4 , Tr_5 . Hence the signals applied to these differential inputs are gated by a d.c. input. This input may be changed rapidly to allow gating for very short durations or may have intermediate values that allow the inputs to be summed in varying proportions.

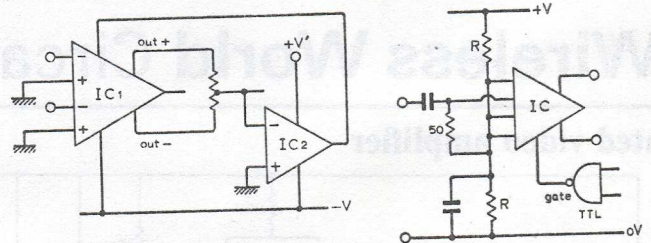
Component changes

IC: MC1445, 1545; similar i.c.s with different bias arrangements include Silicon General SG1402/2402/3402. "Discrete" versions based on transistor arrays are also possible but no particular advantages would be expected except possibility of operating at unusual supply voltage/current levels. Balanced modulators/demodulators (MC1496) have similar input stages with free collectors suitable for coupling into tuned circuits.

If the frequency range is more limited, it is possible to adapt analogue multipliers with one input switched between zero and some finite value. This also allows reversal of phase of the output if the control input polarity is reversed.

V_s : ± 3.5 to $\pm 12V$.

R_L : At low supply voltages the output quiescent current may be increased by placing external resistors in parallel with the 5.0k Ω internal resistors. This increases the signal current that may be capacitively coupled into a load, while lowering the output impedance. 10k to 1k Ω at $\pm 5V$ supply. Observe maximum dissipation limits of device (dependent on package,



ambient temperature, but up to 400mW at $< 50^\circ C$).

Circuit modifications

- By applying the mean value of the output to a standard op-amp, the output can be made to provide a sensitive error signal for departures of the mean i.c. output potential from ground. If the op-amp is operated from a higher positive voltage than that required by the wide-band i.c., then d.c. feedback ensures that the positive voltage applied to the i.c. forces the mean output close to zero (depending on the op-amp offset of a few millivolts). This allows d.c. coupling of signal from input to output of wide-band amplifier with negligible offset.

- For single-ended supplies the unused inputs are taken to a decoupled potential divider, with the option of a 50 Ω resistance added to define the input impedance of any signal input, e.g. capacitively coupled as shown. The gate terminal then becomes compatible with a t.t.l., c.m.o.s. logic gate sharing a common ground line.

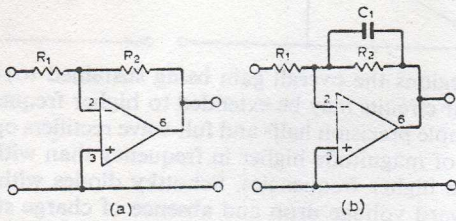
Further reading

Welling, B. and Russell, R. Using the MC1545: Monolithic Gated Video Amplifier, Application note AN-475, Motorola 1969.

Cross references Series 12, cards 3 & 6.

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High-speed operational amplifiers

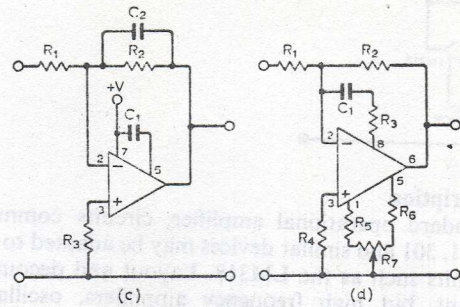


$R_1, R_2: 10k\Omega$
Slew rate: $80V/\mu s$
Small-signal
bandwidth 14MHz

$R_1: 5k\Omega, R_2: 10k\Omega$
 $C_1: 5pF$
Voltage gain: -2
Comparable figures to (a)

Circuit description

The bandwidth available from operational amplifiers has been extended by many manufacturers to the level where they can be applied to problems previously requiring specially-designed wideband amplifiers. The circuits shown use a monolithic i.c. LM318, showing how manufacturers are able to provide compensation points to modify the high-frequency characteristics—trading in stability margins for increased slew rates, minimum settling times, etc. The internal structure of any particular i.c. at this level of performance is immensely complex and most users will have to treat them as black boxes.

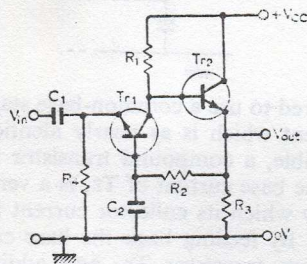


$R_1, R_2: 10k\Omega, R_3: 5k\Omega$
 $C_1: 0.1\mu F, C_2: 5pF$
Shortens settling time to
 $1\mu s$ for 0.1% accuracy
after 10V step

$R_1, R_2: 4.7k\Omega$
 $R_3: 3.3k\Omega, R_4: 1k\Omega$
 $R_5, R_6: 27k\Omega, R_7: 2.5k\Omega$
Slew rate: $150V/\mu s$

Using hybrid techniques as well as discrete circuitry, amplifiers are available with slew rates in excess of $1000V/\mu s$ and bandwidths greater than 100MHz. Methods of construction are more costly than monolithic circuits and they are relevant to specialized applications. In general to achieve such very high bandwidths, the open-loop voltage gain has to be restricted to the range 1 to 5000, while the monolithic amplifier above is optimized for best bandwidth consistent with voltage gains $> 100,000$.

Common-base wideband amplifier



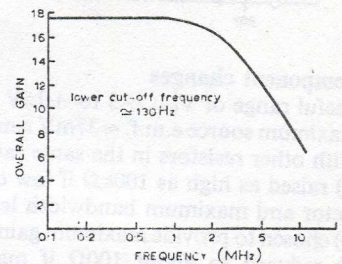
Circuit description

The input stage consists of Tr_1 in the common-base configuration with this transistor feeding Tr_2 acting as an emitter follower with overall shunt-derived shunt-applied feedback through R_4 . This arrangement is similar to the circuit shown on card 9, except that the source feeds the emitter instead of the base of Tr_1 , indicating that the d.c. feedback pair is a convenient method of biasing a common-base stage.

Capacitor C_1 prevents any d.c. component present in the input signal from affecting the biasing, or it may be thought of as necessary if the source cannot sink current from Tr_1 emitter. Capacitor C_2 grounds the base of Tr_1 to a.c. signals. The input impedance of the circuit is low and may be adjusted or matched to a source, by means of R_1 which controls the collector current and hence the emitter current of Tr_1 . This type of circuit is useful for applications where the common-

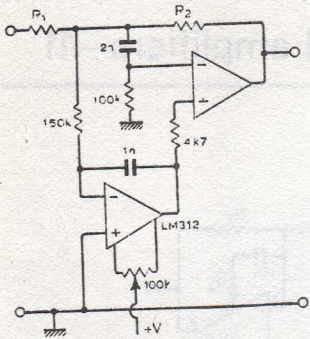
Circuit data

Supply: +5V, 8mA
 $Tr_1, Tr_2: 1/5 \times CA3046$
 $C_1, C_2: 10\mu F$ tantalum
 $R_1: 3.9k\Omega; R_2: 10k\Omega$
 $R_3: 150\Omega; R_4: 470\Omega$
Source e.m.f.:
30mV r.m.s.
Source res.: 100Ω



base configuration offers advantages such as small non-linearity of its transfer characteristic and relatively constant gain with frequency, while providing moderate gain due to the impedance transformation between input and output.

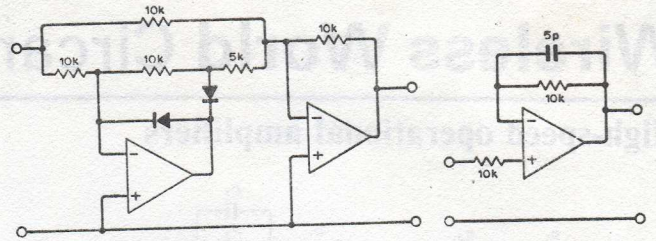
The integrated circuit used is the same as that for card 9 where one transistor has its emitter connected to the substrate which must be connected to the most negative supply rail (0V in this case). Because neither Tr_1 nor Tr_2 has its emitter grounded in the above circuit the substrate-connected transistor cannot be used but its emitter must still be grounded.



Circuit description

● As a standard operational amplifier, circuits commonly used with 741, 301 and similar devices may be adapted to high frequency units such as the LM318. Layout and decoupling are important, but high frequency amplifiers, oscillators, filters and the like follow similar configurations, generally with comparable resistance values and reduced capacitances. To combine the wide frequency range with high input resistance the technique shown may be adopted. At very low frequencies the high input impedance amplifier—LM312 or similar—develops its full gain applying its inverted output to the non-inverting input of the high-frequency amplifier. The overall characteristic is inverting and the feedback is negative, while the minimal input current of the high-impedance unit permits R_1 and R_2 to have megohm values. At high-frequencies the integrator configuration of the LM312 leaves the non-inverting input of the LM318 virtually grounded. The signal appears on the inverting input via the CR network and the feedback remains negative. The two time constants define the

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cross-over regions the overall gain being sustained to 1MHz. ● Non-linear circuits may be extended to higher frequencies, and for example precision half- and full-wave rectifiers operate to an order of magnitude higher in frequency than with 741, etc. At these higher frequencies, Schottky diodes with their smaller forward voltage drop and absence of charge storage are worthwhile alternatives to even high-speed conventional diodes.

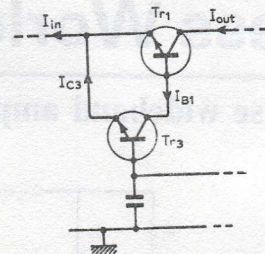
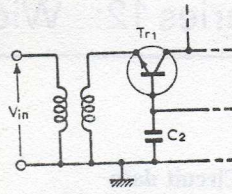
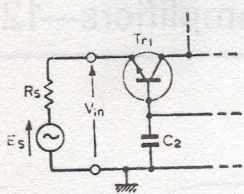
● Component values for the voltage follower mode are similar to those for the unity-gain inverter. Not all amplifiers are compensated for 100% feedback, but may be optimized for higher gains instead.

Further reading

LM318 data sheet, National Semiconductor Linear Integrated Circuits Databook, 1972, pp.185-9.
Young, R. L. Lift i.c. op-amp performance, *Electronic Design*, vol 4, no. 21, 15 Feb, 1973, pp.66-9.
Motorola application note—AN276, 14MHz wideband amplifier using the MC1530 op-amp.

Cross references

Series 12, cards 3 & 4.



Component changes

Useful range of V_{cc} : +3 to +15V.
Maximum source e.m.f. $\approx 37\text{mV r.m.s.}$ (with $V_{cc} = +5\text{V}$).
With other resistors in the same ratios R_1 may be:
(a) raised as high as $100\text{k}\Omega$ if low quiescent power is a major factor and maximum bandwidth less important.
(b) chosen to provide maximum gain-bandwidth product in Tr_1 .
(c) reduced to about 100Ω if maximum output current is required.
 R_2 may be reduced towards R_1/h_{FE} and R_2 increased towards $h_{FE}R_1$.

Circuit modifications

● If the signal source can sink direct emitter current of Tr_1 , C_1 and R_4 may be omitted and the source connected directly to Tr_1 emitter as shown left, the rest of the circuit remaining the same.
● Where d.c. isolation of the source and Tr_1 emitter is required, an alternative input arrangement to the original circuit using a transformer may be adopted as shown centre, again the remaining circuitry being unchanged. This input transformer may be used to match the source to the input impedance of Tr_1 if desired.

● If it is required to use a common-base stage that provides an output current which is as nearly identical to the input current as possible, a compound transistor may be used as shown right. The base current of Tr_1 is a very good measure of the extent by which its collector current falls short of its emitter current. By feeding back the base current of Tr_1 to the common-base transistor Tr_3 and adding its collector current to the input current, the output current more nearly approaches I_{in} . This technique also raises the output impedance from Z_{out1} to approximately $Z_{out1} \cdot h_{rb1} / (1 - h_{rb2})$ and reduces the distortion from $D_1\%$ to approximately $D_1(1 - h_{rb2})\%$ compared with Tr_1 alone.

Further reading

Miller, J. R., *Solid-State Communications*, McGraw-Hill 1966, chapter 15.
Boxall, F. S. Base current feedback and feedback compound transistor, *Semiconductor Products* vol. 1, no. 5, 1958, pp. 17-24.

Cross references

Series 12, cards 2, 5 & 9.
Series 7, card 9.

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