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Designing a better sweep generator

TECHNOLOGY

Analogue storage on silicon

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FEATURES

REGULARS

In next month's issue: Spectrum analysis on the cheap. The best electronics engineers don't need the most expensive test equipment. It is possible to conduct useful RF spectral analysis using little more than a low cost oscilloscope and a few scrap TV components proving that necessity is the mother of invention.

For humans... by design

The inability of ordinary, intelligent people to master the complexities of consumer electronics has become a cliche. How can it be that thousands of pounds spent on market research followed by billions of yen poured into product development result in products which are virtually unusable.

One can unravel much of what passes through the mind of the designer by looking at the almost unlimited power which the typical video remote control gives to the unfortunate user. Who else but an electronics engineer would require that the viewer adjusts fine frequency tuning, tracking adjustment, sharpness and hue? Who else but a cryptographer would have the user counting fingers and toes in order to record a programme for the third day of next week bearing in mind that: the programme actually starts just after midnight which makes it four days into next week, not three; that the time to be set should be AM not PM; that the channel selection for the recorded event has been correctly adjusted (see above) and allocated; that February of this year has 29 days requiring that the event to be recorded is actually five days into next week rather than four... or was it three?

Once upon a time medical schools selected students on a combination of entry examination results coupled with the opinion of an interview board. The function of the interview was to determine the applicant's perceived suitability for a caring, sympathetic profession. This largely resulted in a generation of doctors who, apart from being technicians, listened to and dealt with the needs of the patients.

Medical schools now select almost entirely on academic achievement: their graduates often fall short of the communication skills required for the job.

This shortcoming in medical training illustrates the way in which professionals can lose touch with their consumers. The stupidity of Japanese designers – I mention "Japanese" because I suspect that the Europeans are better, although not immune in this respect – derives from their insistence that technology is the goal rather than the means. What might be satisfying by design to a bunch of engineers who feel the need to adjust chrominance phase angle, tracking sync, luma bandwidth and IF centre frequency, etc is just a pain in the posterior to everyone else. How much better to harness the undoubted ingenuity of the design department towards making products which are intuitive and certain of their purpose?

The best example of design with ordinary people in mind comes from the computer world. Until Xerox developed the X-Windows interface for business computers, their machines, like everybody else's, required a cryptographic insight on the part of the operator. Apple quickly followed the Xerox example with a user presentation on a desktop computer so simple that its users boast of being able to use application software without ever reading the manuals.

A successful design takes the human factor into account. This is as important to computer installations as it is to domestic videos. After all, if technology can't be harnessed effortlessly and to real purpose, it loses purpose which eventually costs both you and me our jobs.

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Change of telephone numbers
From Monday February 24th our exchange number will change from 661 to 652. So, for example, a telephone number that is currently 081 **661** 1234 will become 081 **652** 1234.

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UPDATE

EC backpedalling on the big screen

Wide screen D2MAC will not become a compulsory satellite TV standard until 1995, according to a last-minute revision of the EC's draft directive. However, the standard – which offers consumers the benefit of wide-screen pictures – is expected to be widely adopted on a voluntary basis before then. One broadcaster, Filmnet, has already started using it.

The directive, which technically came into force at the beginning of this year, is considerably watered-down from the draft proposed earlier in 1991. New broadcasters will still be able to use PAL up until the beginning of 1995, and PAL services existing at that date will be able to continue indefinitely. There is no reference to compulsory D2MAC compatibility for sets.

The draft, which was unanimously adopted by telecommunications ministers after 15 hours of negotiations on December 181, also omits direct mention of EC subsidies to start-up D2MAC services. These, amounting to a possible £700m (Ecu 1bn), will be the subject of separate proposals to be tabled by the end of April.

The new directive, which runs until 1998, provides for regular reviews, and for the possibility of adopting a digital approach to a European HDTV standard, as an alternative to D2MAC.

Although the element of compulsion has diminished, the industry is confident that D2MAC will take off quickly, driven by demand for wide-screen movies. "By the end of this year there should be at least one channel for each territory in Europe, a Philips spokesman said, "We expect 15 to 20 broadcasters to be doing D2MAC in the next two years."

First in the field was Filmnet, which transmits movies to the Benelux countries and Scandinavia. It is now transmitting on Astra in D2MAC/EuroCrypt, with receivers provided under contract by Philips, in addition to existing PAL services. Part of Filmnet's impetus may derive from its existing encryption which, unlike Sky's, is notoriously insecure.

BSkyB, with over two million PAL receivers in the UK, has welcomed the directive and expressed cautious interest in D-MAC's "market opportunity". It too is understood to be in discussions with Philips.

No laughing matter for Europe's setmakers who hoped for less PAL and more compulsion towards HDTV

Viewers with 16:9 TV sets, plus D2MAC receivers and suitable aerials (90cm aimed at the Olympus satellite, 18.8°W) will be able to enjoy the wide-screen ratio (but not the 1250-line definition) of HDTV transmissions of this year's Olympic Games.

Peter Willis

The engineering model of satellite-borne microwave radiometer AMSU-B – Advanced Microwave Sounding Unit – is pictured at Bristol prior to initial radio frequency testing at Queen Mary & Westfield College, London. The instrument is being developed by British Aerospace Space Systems Limited, Earth Observation and Science Division as prime contractor to the UK Meteorological Office.

AMSU-B, which will initially fly on future NOAA series weather satellites, is principally designed to monitor temperature and humidity profiles in the upper atmosphere. It will help weather forecasters to greatly improve the accuracy and detail of their weather predictions.

Since 183.31GHz is a water vapour absorption line, outdoor testing of AMSU-B was ruled out.

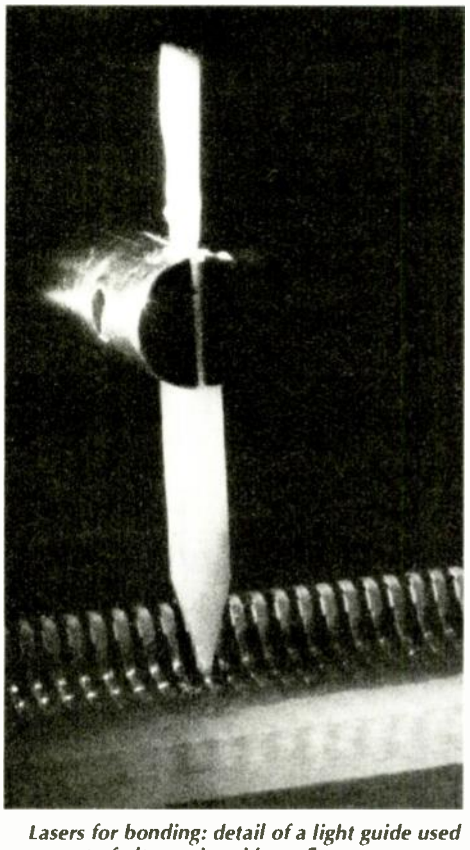
New packages for euro-technology

Work is beginning in a pan-European Eureka project to develop advanced design and manufacturing techniques for multi-chip modules (MCMs).

MCMs, incorporating a number of VLSI and other less complex chips, may be the only feasible solution for future complex system integration. The project, called Pepite, has been costed at about £11 million over three years.

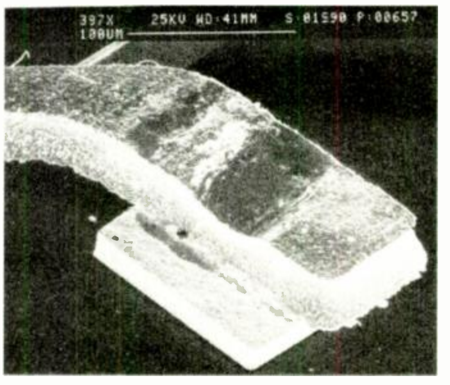
Consumer and telecom electronics rely on the compactness of silicon chips to make them light and portable. But with the way chips are packaged at the moment, only one tenth of the package is actually taken up by the chip. Simply by changing the way devices are connected together, the amount of space they need could shrink up to fivefold within the next three years.

Several European electronic companies already have experience with MCMs but effective exploitation of the devices depends on developments to overcome performance and price barriers inherent in current interconnection and packaging technologies.



Lasers for bonding: detail of a light guide used as part of ultrasonic solder reflow process

MCMs need to be made smaller and to have guaranteed high reliability and durability at reasonable cost for applications such as automotive engine management systems. This requires a greater understanding of heat dissipation and the high frequency behaviour of the interconnections.



PErformance Packaging and Interconnection TEchnology: scanning electron micrograph of copper tab interconnect bonded to aluminium pad

Most aspects of MCM technology are already used in conventional hybrid manufacture. The task behind the Pepite programme is to do what is already being done but at a fraction of the cost.

Dave Pedder, a researcher at GEC Plessey Semiconductors says that they are seen as an alternative to the ultimate in chips – wafer-scale integration – in which all the circuitry for something like a laptop computer is made on a single chip.

The collaborators have already shown two new ways of making ceramic substrates.

Martin Lockyer a researcher at the University of Warwick, has developed a machine similar to a crepe maker, called a tap caster. He pours a mixture of glass particles which look like a mixture of icing sugar and an oily solvent onto a plastic sheet on a platform, making a thin sheet of ceramic which hardens as the solvent evaporates. The ceramic is known as green tap. It can be cut and punched, and connections printed on it, before it goes into the kiln for firing at up to 900°C.

Researchers at the Welding Institute have developed a device which spray-coats ceramic onto metal plates with a gun rather like an oxyacetylene cutter. Acetylene, oxygen and powdered ceramic are mixed in a combustion chamber and ignited, shooting a white-hot flame out of the end of the gun The particles melt at about 2000°C in the flame, where they stay for a microsecond. The design of the gun is 35 years old although it has never been used to deposit ceramic on metal.

Meteor showers go commercial

Bouncing radio signals off meteor showers is one of the 16 telecommunications proposals being considered by Peter Lilley, the secretary of state, for a new UK service licence.

Meteor Communications plans to offer telemetry services to remote stations and moving vehicles throughout the UK.

US company Broadcom developed the system called *Meteorburst* where 30MHz to 70MHz radio waves are reflected from the ionised dust created by meteors in the earth's atmosphere. Data rates of 1Mbit/s are achievable says the company.

Another licence application, which is creating some interest, is the proposal by a small unknown Cambridge company to create a national a public switched telephone service in competition to BT and Mercury Communications. The company called Ionica L3 plans to use radio technology.

The other applications are dominated by existing mobile licence holders wishing to offer fixed and international services. Three of the UK's four mobile data licence holders, Hutchison Mobile Data, Cognito and RAM Mobile Data want licences to offer fixed services.

National Transcommunications has applied for a licence to offer broadband voice, data and video services on its national network. Vodafone and United wish to offer fixed services.

Richard Wilson, Electronics Weekly

Capacitor keyboard

A new keyboard switch system uses membrane capacitance change rather than membrane contact for its action. When a key is pressed, its associated charge changes. By measuring the level of charge on each switch, a drive circuit can then detect not only that a switch has been pressed, but precisely when it was pressed during the cycle. Simultaneous key-presses can be distinguished from several keys pressed in quick sequence during a single scan. The technology was developed by UK company NFI Electronics located in Newport, Isle of Wight.

Dishing out high level interference

Eutelsat II-F3 is the first satellite to be located so close in orbit to an existing craft that trouble-free reception with small dishes cannot be guaranteed. This might happen because Eutelsat and Astra share frequencies. Up until now, physical separation coupled with highly directional receiving aerials have ensured enough isolation for frequency reuse. When Eutelsat switches on alongside Astra, satellite broadcasters will find out whether engineers were right to warn that environmentally friendly 60cm dishes will mean that viewers will suffer interference from adjacent satellites. The marketing people maintain that larger dishes would slow sales.

Initially Eutelsat II-F3 won't cause interference. Broadcasters will use the craft to relay high definition TV signals from the Winter Olympic games in Albertville, France. Prototype widescreen HDTV receivers, made for the Eureka HD-mac project and installed in shops and public places round Europe, will screen the pictures.

Jean Grenier, Director General of Eutelsat, the consortium which operates satellites on behalf of 28 European countries, warns that interference between some channels of Eutelsat II-F3 and Luxembourg's Astra satellite is now inevitable if viewers of either satellite try to use 60cm dishes. The two satellites share some of the same channel frequencies, transmit at the same power (50W) and are located only 3° apart in orbit (II-F3 at 16° East, Astra at 19° East). The 60cm dishes already sold to two million British viewers, and as many again elsewhere in Europe, need a separation in orbit of 6° to guarantee freedom from mutual interference.

Viewers with small, badly made or poorly aligned dishes will receive pictures from different satellites or fuzzy images whenever the two satellites are working on the same frequency.

Eutelsat is advising all viewers to use a minimum dish size of 80cm. Astra advises 55 or 60cm. The Department of the Environment has set a limit for UK homes of 70cm.

Physics, not politics

Astra says that people in the UK who currently watch BSkyB's programmes should not be affected. There is now some doubt about this. In any case, there can be no guarantee of a trouble-free future.

All the channels on Astra's first satellite, 1A, are safe because Eutelsat does not use these frequencies (11.2-11.45GHz). Astra's second satellite 1B operates on a higher band (11.45-11.7GHz) and the lower third of 1B's channels are safe because Eutelsat's working band starts at 11.536GHz (between channels 21 and 22 on Astra). This puts the other two thirds of channels on 1B, up to 11.685GHz (Channel 32), at risk.

The current risk band includes BSkyB's Comedy Channel, and the Children's' and Japanese Satellite TV Channels. The risk band also includes all the channels at the top end of 1B which are not yet being used for broadcasting. It is now easy to see why these channels remain unused. Astra has been nervous about leasing them and potential broadcasters have been worried about hiring them.

Astra's next satellite, 1C, will operate on the band below 1A (10.95-11.2GHz). By the time 1C is launched, in a year or so, Eutelsat will be working on the same frequencies. So there will be a role reversal. Whereas Eutelsat's F3 is currently cast as the intruder in 1B's territory, Astra's 1C will be cast as the trespasser on F3's patch.

Astra cannot afford to play safe permanently, leaving channels on 1B, and later 1C, unused. Each is worth several million pounds a year in rent and broadcasters want them. Broadcasters will need them too, because the European Commission is planning a Directive which will pay broadcasters up to £750 million of taxpayers' money to transmit the same satellite programmes in both the old PAL system and new MAC, thereby creating a shortage of channels.

Eutelsat is no more happy about the clash than Astra. Interference works both ways. Eutelsat has already sold channels on II-F3 to six countries, the UK and Netherlands, Spain, Finland, Italy and Yugoslavia, for TV transmission. If Eutelsat's viewers use small dishes, they will suffer from interference from Astra.

But whereas Eutelsat can specify a minimum dish size of 80cm from Day One, Astra has already built its marketing strategy on 60cm dishes.

Eutelsat cannot co-locate several satellites in the same orbital position as Astra is doing. To allow co-location, Astra ordered satellites which operate on different frequencies. When Eutelsat ordered its satellites, the monopoly consortium of 28 European Postal and Telecommunications authorities asked for extra orbital slots for single satellites instead of planning for co-location of several satellites at the same location. So Eutelsat ordered six,virtually identical satellites from maker Aerospatiale. Because these all operate on the same fixed frequencies, they would interfere with each other if co-located at the same orbital positions.

Eutelsat says that the orders were placed before Astra's plans became clear. But Eutelsat was far less flexible in those days and would probably have ordered identical satellites anyway. Certainly Eutelsat seems to have made no effort to modify the order even after it became clear that Astra would be a viable commercial competitor.

Because some of Eutelsat's transponders work over a 72MHz FM bandwidth instead of the usual 36MHz (for a 27MHz signal), Eutelsat can offset the carrier frequencies of at least some channels to reduce interference risks – provided that ground users are willing and able to tune onto shifted frequencies. The practical result will depend on the accuracy of the dishes used on the ground and their ability to reject signals of one polarisation in favour of signals of opposite polarisation. It is also likely that MAC signals will cause only noise interference on PAL signals, whereas PAL on PAL will give double images.

There are so many variables that engineers at both Astra and Eutelsat agree that no-one will know until services begin.

Barry Fox

Solid state to match hard discs

Solid state discs containing 40Mbytes of memory – the same density as the average PC hard disc – are on the way from Hitachi within the next two years.

"When we have 16Mbit, flash device out in 1993, SSDs will take the disk market by storm", reckons Hitachi's Nick Jeffries.

With Hitachi's memory cards holding ten chips per side – 20 chips in all – a card offering 320Mbits of memory becomes useful. Until then, "1 and 4Mbit flash will develop the market. That's why we're not offering sector erase... we're going to drive down chip size and cost so we can replace UV eprom."

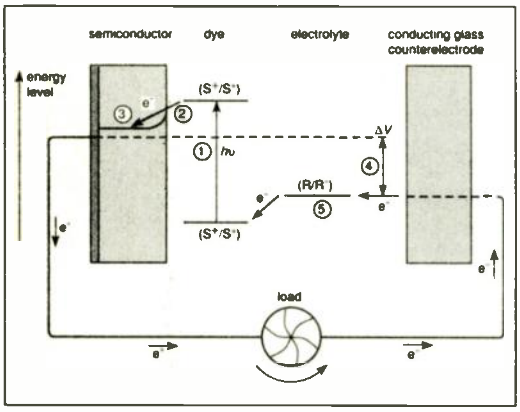
REGULARS

RESEARCH NOTES

Cheaper solar cells mimic nature

Reports of unlimited "green" energy from sunlight, using a process looking remarkably like photosynthesis, are how the media has greeted one recent scientific announcement. The scientists themselves prefer to describe it as a low-cost, high-efficiency solar cell based on dye-sensitised colloidal TiO_2 films (Nature, Vol 353, No 6346) and its significance is demonstration of the practicality of a low-cost alternative to silicon cells.

What Brian O'Regan, currently at the University of Washington in Seattle, and



Schematic representation of the principle of the dye-sensitised photovoltaic cell.

Michael Grätzel of the Swiss Federal Institute of Technology in Lausanne have done is to separate the light-collecting process from the energy conversion process. In a normal silicon photocell these two are combined. The new cell uses a monolayer of a charge-transfer dye – a complex ruthenium compound – deposited on a microscopically roughened 10μm layer of transparent titanium dioxide. Current is generated when photons absorbed by the dye inject electrons into the conduction band of the TiO_2 semiconductor. At a conducting glass counter-electrode a chemical reaction occurs in the electrolyte which then regenerates the dye.

The physical chemistry may be complex, but Grätzel says these cells could almost be made in the kitchen, given the right kind of oven. They are also, potentially, much cheaper and more efficient than amorphous silicon cells with which they are designed to compete. Already the overall light-to-electricity conversion yield is around 8% in simulated sunlight.

Dye-sensitised photocells are not a new idea, but without the latest developments in dye chemistry and the effective increase in semiconductor surface area by roughening, most researchers had written them off as hopelessly inefficient. The work of O'Regan and Grätzel, together with the acknowledged long-term stability of these cells, demonstrates clearly the potential for further development.

Physics through a beer glass, darkly

Pour a pint of beer and watch the bubbles stream up from the bottom. Notice that they get larger and are spaced farther apart as they rise. What's going on? When Stanford University chemistry professor Richard Zare and post-doctoral researcher Neil Shafer asked themselves that question, it led to a whole series of investigations into the interplay among gases, liquids, solids, temperature, pressure and gravity.

It seems that beer bubbles begin as tiny clusters of molecules that grow on rough spots called nucleation sites - usually scratches on the glass. The bubbles form from carbon dioxide, which is dissolved in the beer.

Zare and Shafer debunk a theory that bubbles double in size as they rise because of a change in hydrostatic pressure. This would require a pressure difference of two atmospheres from the bottom to the top of the glass - a rise of nearly 30 feet. Not even EW&WW staff at Hogmanay could manage a beer that big.

Zare and Shafer have shown instead that the bubbles act as nucleation centres for themselves, accumulating more carbon dioxide as they rise through the beer.

As the bubbles get bigger, their buoyancy becomes greater relative to the beer. A simple application of Archimedes' principle:

$$F_{bubble} = V_{bubble} (p_{beer} - p_{bubble}) \cdot g.$$

(F is the force on the bubble; V is its volume, p is density, g is the gravitational constant.)

Drag on the surface holds the bubble back from rising, but drag increases less rapidly than buoyancy. So, the bigger the bubble, the faster it rises. Thus, higher bubbles race away from lower ones in the stream, spacing bubbles farther apart at the top of the glass.

Zare says that the fluid dynamics of this process turn out to be much more complicated than they seem.

For example, there is no simple method to predict the drag on a particle moving in a viscous medium, and when Zare and Shafer tested the two most likely theories, their observations did not match either one.

Surfactants – the slippery substances that give staying power to the head of foam at the top of the glass – affect the ascent of the bubbles. If the bubbles rise in a tall enough glass, even their shape changes, from a sphere to an ellipse that oscillates and travels in a zigzag path.

The two chemists say that most of their insights into beer could also apply to other carbonated beverages such as mineral water or champagne - though add that a serious study of the latter might be beyond their budgets. Bottoms up!

Accelerator magnets attract world record

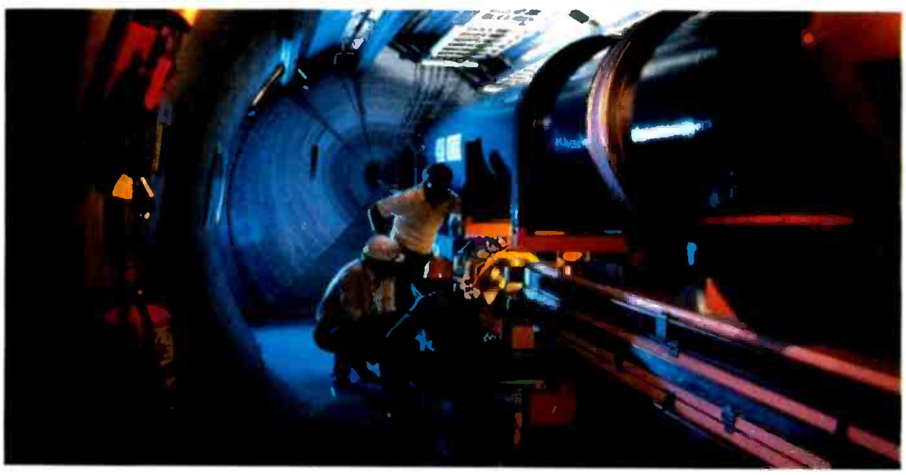
An important step in development of the high field superconducting magnets for the proton collider proposed by Cern, the European Laboratory for Particle Physics, took place recently. A 1m-long model of the twin-dipole magnet produced a field of 10Tesla in its two beam apertures at the design temperature of 1.8K – a new world record for accelerator magnets. The peak field seen by the superconductor was 10.3Tesla.

Cern is carrying out an intense programme of research and development on the LHC (large Hadron collider) project. The LHC is a particle accelerator that will bring protons into head-on collisions at higher energies than ever achieved before. It will enable physicists to penetrate further into the structure of matter and will recreate the conditions that prevailed in the universe around 10^{-12}s after the Big Bang.

The LHC is expected to be installed above Cern's LEP (large electron-positron) collider in the same 27km tunnel. (The tunnel was designed to accommodate two rings.) To subject the quarks and gluons hidden deep inside protons to the 1TeV collision energy at which new physics should show up, the LHC designers have to plan for 16TeV proton beams. Confining these very high energy particles to the right track of the 27km LEP tunnel will require the strongest magnetic bending power ever used in a particle accelerator.

The LHC ring will consist of nearly 1800 superconducting magnets, each 9m long. To save space and cost, the plan is to install the separate magnetic channels for the twin proton beams of LHC in the same iron yoke.

The twin aperture is a special and novel feature of these magnets. It allows the two counter-rotating beams to travel in twin magnetic channels. The channels are incorporated in a single yoke kept at extremely low temperatures inside a cryostat and for the LHC to work correctly, a magnetic field of 9.5 Tesla is needed. The results from the prototype magnet thus represent a positive step in overcoming the technological problems such a machine presents.



A mock-up of the Cern LEP (large electron-positron) tunnel with the LHC (large Hadron collider).

Venus unveiled

85% of the surface of Venus has now been mapped with a resolution approaching 150m – a higher percentage than Earth, whose southern oceans have not been observed in the same detail. Venus, moreover, is revealing a geological history that is stranger and more mysterious than anything previously seen.

Credit for all this work goes to the space probe, Magellan, which was launched on May 4, 1982 from the shuttle Atlantis. After a few initial nail-biting hitches, it has now produced pictures and data more complete but more puzzling than anything astronomers could have dreamed of.

That spectacular mission is ironic in view of the fact that Magellan is a mission that was cancelled in 1982 and then resurrected in a stripped-down form using second-hand parts. Its Synthetic Aperture Radar (SAR) was inherited from the inter-planetary Voyager project; other flight-qualified parts needed for testing were borrowed from the Smithsonian Institution's national air and space museum in Washington!

Since August 10, 1990, Magellan has been hanging around in what amounts to an almost Venus-stationary orbit, while the planet revolves slowly beneath it. Mapping takes place for 37 minutes per orbit and can theoretically be completed in one Venus day (243 Earth days).

Magellan uses the same 4m high-gain antenna for radar mapping of the Venusian surface as it does for sending data back to Earth. The data is received at 268.8kbit/s by the Deep Space Tracking Network, which consists of 70m dishes at Goldstone, Madrid and Canberra. Power for the spacecraft - some 1.2kW - comes from two solar panels of around 6m^2 each.

To achieve its 150m resolution at the surface of Venus, the spacecraft makes use of multiple images taken on overlapping passes. These are combined on Earth using computer image-processing to synthesise the effect of an antenna very much bigger than 4m. A third dimension, that of height, is added from an independent radar altimeter, pointing vertically downward towards the Venusian surface.

Now that Venus is all but mapped, geologists are trying desperately to make sense of the arrays of volcanos and craters that adorn her surface. These features, all in pristine condition, suggest that around 500 million years ago, all geological activity ceased abruptly. There have been no recent volcanic eruptions and no continental drift of the sort seen on Earth and other planets in the solar system.

We may never discover the reasons for Venus' differences from elsewhere in the solar system. Few spacecraft have ever withstood the crushing atmospheric clouds of boiling acid for more than a few moments, to study the surface in detail.

One possible theory for the planet's inhospitable atmosphere is that it represents the consequence of thermal runaway due to the greenhouse effect. Which might make us think still more seriously about the vapours we continue to pump into our own atmosphere.

CIRCLE NO. 107 ON REPLY CARD

HOT FUSION GETS HOTTER

The inside of the JET torus in which plasma is heated up to 300million°C and confined with magnetic fields.

Prospects for a workable fusion reactor took a significant step forward at the beginning of November following an experiment at Culham in Oxfordshire. Culham is the home of Jet, the Joint European Torus, where fusion research has been conducted ever since 1983 with an international team from the EC, Switzerland and Sweden.

To make hydrogen atoms fuse together in a controlled fashion would mean creating a mini-sun on Earth. However, the enormous pressures and temperatures of the sun are both difficult to create and even more difficult to contain.

The fusion experiment used at Culham – similar to others in Japan, the USA and the USSR – makes use of a doughnut-shaped container, a torus, in which hydrogen is both heated and contained. Huge heating currents, up to 7million A, and huge magnetic fields take hundreds of Megawatts from inertial generators in the process of converting a few grams of gas into a plasma at over 10^8°C. If the plasma can be kept in a stable, sufficiently dense state, away from the walls of the torus, a small number of light atoms will fuse to form heavier ones with a release of energy.

Until a few months ago, this type of experiment had only been conducted using deuterium, a form of hydrogen. However, deuterium has a low reaction rate and the fusion process is hard to ignite. This means that the energy produced has been virtually nil.

What the Jet team has now done is to use a reaction mixture containing 10% tritium. This has a lower ignition temperature and fuses to form helium, neutrons and thermal energy. The reaction is:

$$^2_1H + ^3_1H \rightarrow ^4_2He + n + 17.6MeV$$

Using this mixture of deuterium and tritium, Jet generated over a Megawatt for two seconds. Not huge by any means, but a significant step forward in understanding the behaviour of hydrogen plasmas. Experiments planned for 1996 will use a much more potent 50:50 mixture of the two isotopes.

Jet itself will never generate self-sustaining fusion power because it is too small and was not designed to do so. A practical reactor would require a means of extracting and processing the thermal energy (from the neutrons which carry 80% of the output power) from the reaction.

Europe, Japan, the USSR and the USA have now agreed in principle to develop a $5 billion successor to their fusion experiments. Known as ITER (international thermo-nuclear experimental reactor), this machine might possibly generate 1000MW for up to an hour at a time. Even if the technical challenges of ITER can be successfully overcome, most scientists believe that a successful commercial reactor is still at least 40 years away.

Microwave power monitor

A team from the department of electrical and electronic engineering at the University of Newcastle-upon-Tyne has developed a novel method of detecting microwave power in free space using optical fibres. Unlike all-electronic methods, it is robust and capable of omni-directional response.

Details of the technique (*Electronics Letters Vol 27 No 22*) indicate that suitably prepared fibres can detect power densities as low as 2mWcm^{-2}, well below the permitted maximum for human exposure.

LJ Auchterlonie *et al* experimented initially with a continuous length of fibre configured as a planar grid structure within a 16 x 16cm window cut in a perspex frame. This length of fibre formed one arm of a Mach-Zehnder interferometer designed to detect phase changes in the light from an He-Ne laser operating at 632.8nm.

Tests were conducted in an anechoic chamber using a 2.45GHz microwave source with the fibre grid orientated normally to the direction of propagation and with the fibres parallel to the electric field. Three different tests were undertaken: one with the fibre uncoated, one with the fibre coated with silver paint and the third with the fibre coated with a proprietary carbon-based microwave absorber.

Effects on the optical phase changes in the fibre - presumed to be thermal in origin - were shown to be significantly greater in the silver painted fibre than in either of the other two experiments.

The Newcastle group went on to construct an isotopic detector consisting of three separate planar fibre grids, carefully coated to match each other within 2%. The unit, which consisted of 50-fibre windows measuring 50 x 100mm, was shown on test to have a uniform angular response with ±5%.

Given its ruggedness against burn-out, its useful sensitivity and its good polar response, the team expects this optical fibre microwave detector to form the basis of a robust protective monitor.

Research Notes is written by John Wilson

Frustrated by problems with the 8038's sine purity David Bridgen builds an audio frequency sweep generator using the XR-2206.

SWEEP GENERATOR

pure and simple

It was the 8038's inability to maintain sine purity over a 1000:1 sweep[1], and encouraging results of tests with an *XR-2206* that provided the driving forces behind this development of an audio frequency sweep generator.

Oscillation frequency of the *XR-2206* is determined by the capacitor between pins five and six and the resistor, either on pin seven (if pin nine is high), or on pin eight (with pin nine low). Specifically it depends, linearly, on current drawn from pin seven.

Since pin seven is a low impedance point and internally biased at 3V with respect to pin 12, and as the maximum safe current which may be drawn is 3mA, the obvious action is to apply a voltage – ramping from nominally 3-0V – to the other end of a 1k resistor connected to pin seven.

Obtaining a linear ramp?

Whatever means is used to generate the ramp, a glance at the oscilloscope can easily suggest that it is linear. But at lower sweep rates this assumption can be far from true, especially if tantalum capacitors are used; just measure the time to full amplitude and compare that with the time to half amplitude.

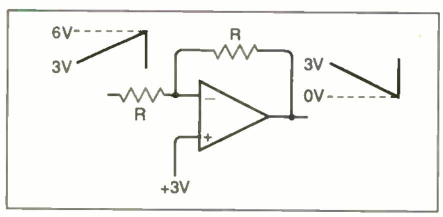


Fig. 2. Shifting the ramp level.

The problem lies in relatively high leakage. As voltage increases, leakage current follows suit and can approach, or even equal, the charging current – encapsulated metallised polyester film types are far superior in this respect.

Perhaps the easiest solution which comes to mind when a voltage ramp is required is to use the *555* timer with a constant current source in place of the normal timing. Given a 15V supply, the ramp from a *555* is 5-10V. This could be scaled and inverted (**Fig. 1**), the LF end of the sweep being adjusted with the 1k pre-set and the HF end with the 2k2.

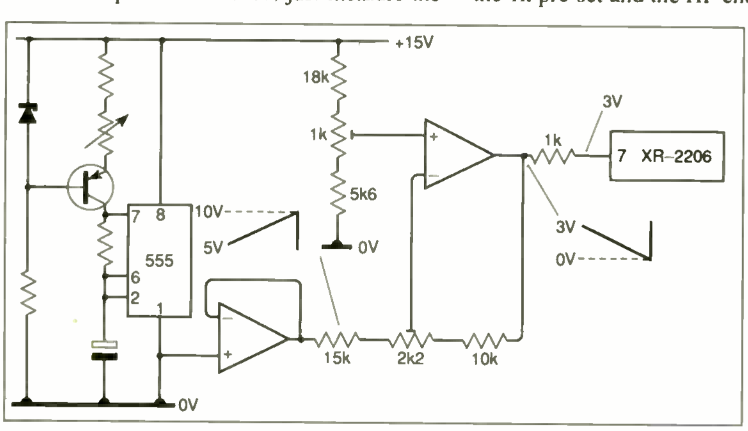


Fig. 1. Using the 555 timer with a constant current source in place of the normal timing to obtain a voltage ramp, scaled and inverted.

We want to supply only a 3V ramp, so we could run the timer from a 9V rail; the ramp would go from 3V to 6V. Its level could be shifted (**Fig. 2**), or, sticking to 15V supplies, we could use something like **Fig. 3** where pin five is maintained at 3V and pin one at –3V with a resultant ramp of 0-3V. Better still would be to generate a –3 to 0V ramp and invert it (**Fig. 4**). All the approaches could be made to work but they each require that sweep limits be defined by pre-sets, and none lends itself to easy changes in sweep ratio.

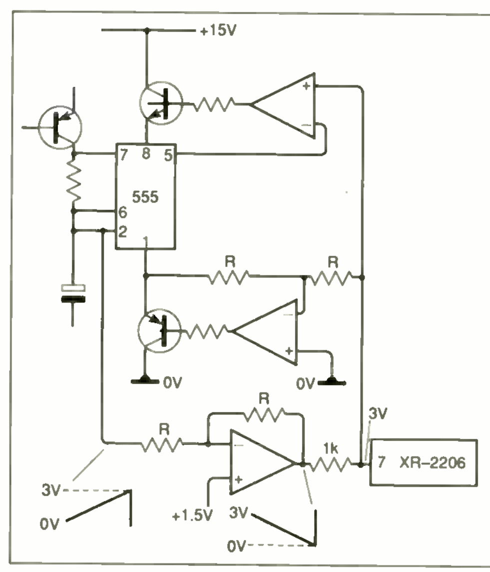


Fig. 3. Maintaining pin five at 3V and pin one at –3V to obtain a ramp of 0-3V.

As design objectives included the avoidance of awkward level shifts and adjustments which inevitably interact, and the start and end of the sweep could easily and independently be changed, the methods have been discarded.

A 3V ramp sweeping the frequency from 20Hz to 20kHz has a sensitivity of 6.6Hz/mV. Any offset in the control circuit can easily be accommodated. More important is stability, so op amps which have particularly good control of offset drift should be specified; *OP-07* is quite satisfactory.

Sensitivity to drift can be further reduced by the simple expedient of increasing ramp amplitude and proportionally increasing the resistor. As long as the 3mA limit is observed it pays to employ as large a ramp as possible. With 15V supplies, and with output voltage-swing limits in mind, a reasonable ramp would be around 10-12V. The 10V ramp chosen, going from +3 to −7, results in a sensitivity of 2Hz/mV, auguring well for stability.

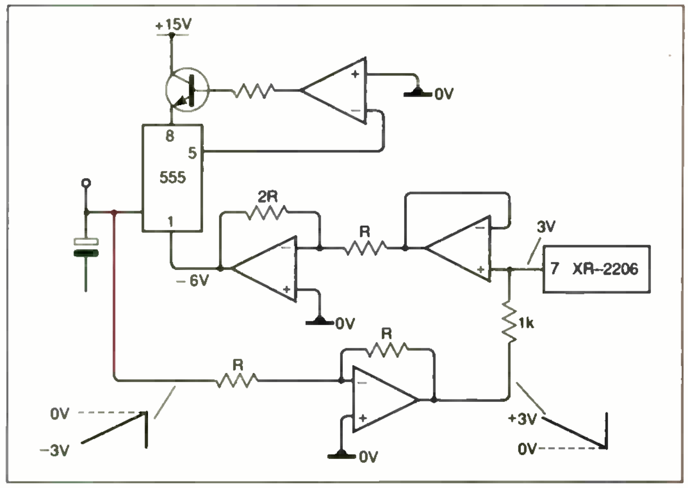


Fig. 4. Best solution is to generate a −3 to 0V ramp and invert it.

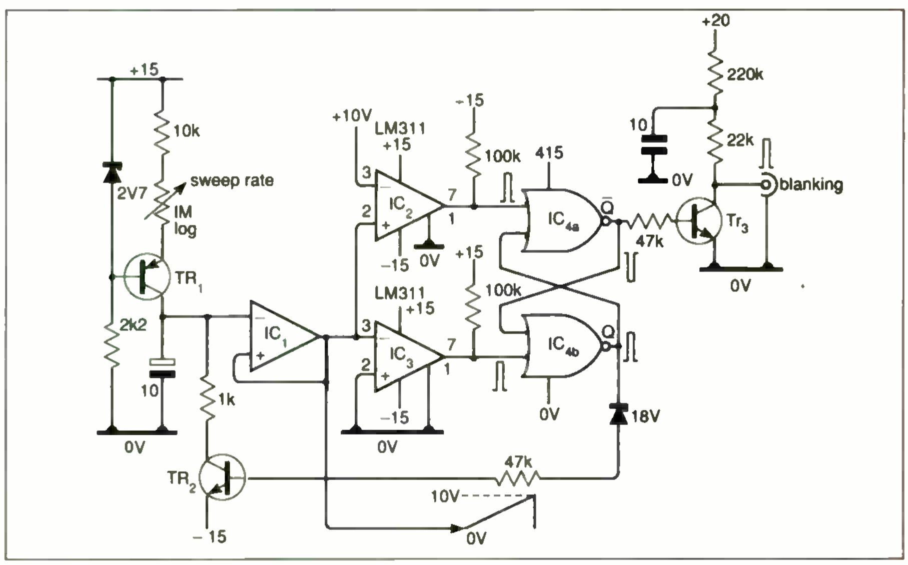


Fig. 5. Basis for a successful circuit.

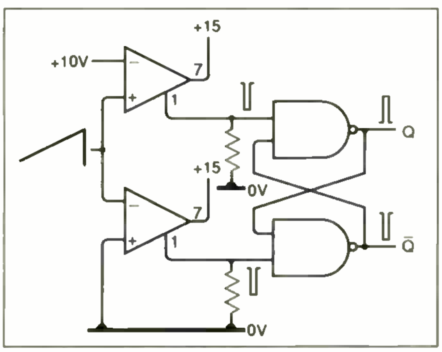


Fig. 6. Changing the circuit to allow Nand gates to be used.

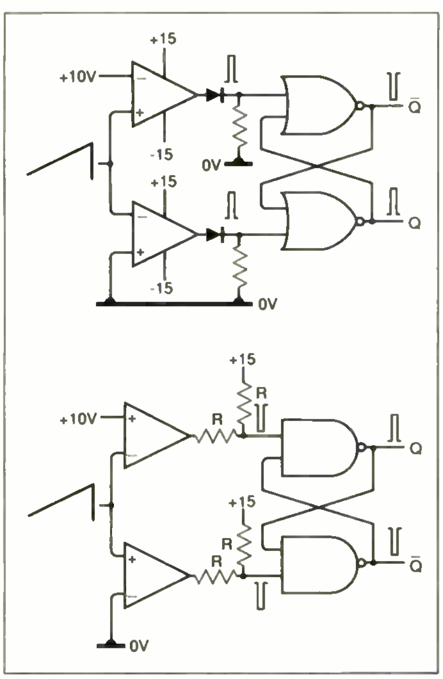


Fig. 7. Circuits suitable if op amps are used as comparators

Towards a successful circuit

In view of ramp amplitude limitations of the *555*, any off-set in a subsequent amplifier would be multiplied by the same factor. Not only would this be self-defeating, it would also mean having to tackle the problems mentioned earlier. The circuit eventually employed overcomes these worries (**Fig. 5**).

A constant current source, TR_1, linearly charges the capacitor at its collector. The ramp, buffered by IC_1, rises to the trip point of comparator IC_2. SR flip-flop, $IC_{4a/b}$, is then set. TR_2 conducts, to discharge the capacitor, and TR_3 goes off, producing a blanking pulse for the scope. The capacitor will discharge to the trip point of comparator IC_3 whereupon the flip-flop is reset. If the TR_2 emitter was at 0V rather than −15V, then $V_{ce(sat)}$ would prevent the capacitor from being sufficiently discharged.

Note that the comparators have to accommodate a 10V input differential and not all types can do this. Nand gates can be used as the flip-flop – if the changes in **Fig. 6** are made: if op amps are used as comparators, the arrangements in **Fig. 7** would be suitable.

The remainder of the control circuit is shown in **Fig. 8**. The 10V reference is obtained from a standard chip, such as *LM369*, *LH0070* or *REF-01*, and buffered by IC_5. The ramp is applied, via IC_6, to the junction of the START and STOP controls. Output from IC_7 will always end up at 10V

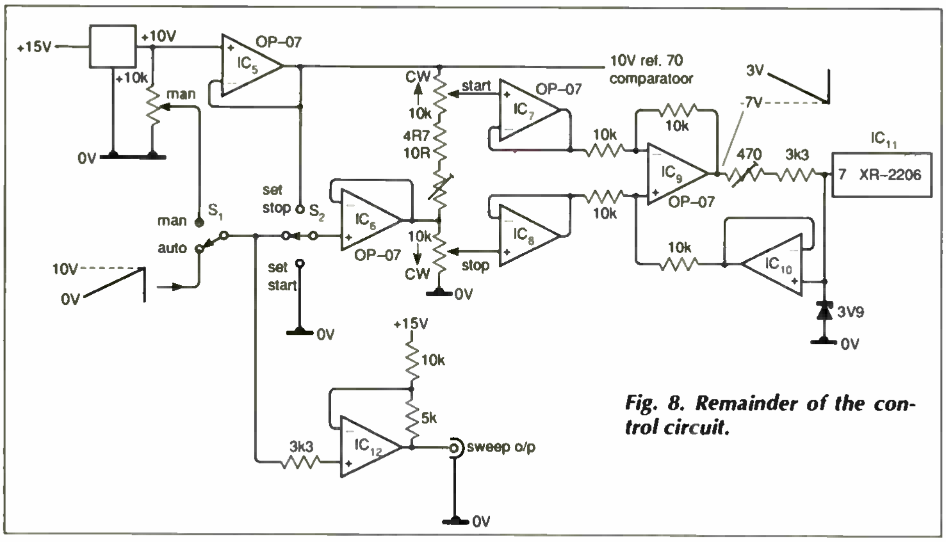


Fig. 8. Remainder of the control circuit.

but will start at a voltage set by the START pot. Output of IC_8, however,always starts at 0V but ends at the voltage set by the STOP pot. These two ramps are subtracted and inverted in IC_9. Without any other input this would give a ramp, at full span, from 0V to -10V. By adding the voltage which appears at pin seven of the *XR-2206* the desired +3 to -7V range is obtained.

Exar fails to mention a reverse bias limit for pin seven in its data sheet but it seems prudent to include the zener to protect against positive spikes which can occur on switching when the input of IC_6 would be briefly floating.

S_1, at the input of IC_6, switches control between AUTO and MANUAL sweep, while S_2 allows the start and stop frequencies to be set without the hassle of having to crank the MANUAL control from one end of its (ten turn) travel to the other. IC_{12} provides the X-axis drive for the scope.

Ten-turn pots used on their own for the START and STOP controls would give a resolution of 2kHz/turn which is rather coarse. The arrangement shown in **Fig. 9** overcomes this by allowing each control to cover a selected 2kHz section of the range, improving resolution to 200Hz/turn.

Output amplitude, at pin two of the *XR-2206*, is controlled by the value of the resistor on pin three.

Exar quotes a relationship of 60mV/k but in practice it is nearer 100mV/k. As the DC at pin two is "approximately the same as the DC bias at pin three", then the resistor should normally be returned to around mid rail. Difference in voltage between these two pins can be 200mV or so but any embarrassment which this may cause is easily overcome with the integrator[2] IC_{16}.

Some published circuits[3, 4, 5] use a variable resistor on pin three to set the amplitude, but this lacks versatility. **Figure 10** shows the circuit adopted. To meet a design requirement of 3V RMS across 600Ω from a 600Ω source, an unloaded level of 6V RMS is required. It is just possible to squeeze 3V RMS from the *XR-2206* with a 15V supply, but allowing for possible variations between samples it seems better to limit this to 2V. IC_{13} has a gain of two and also shifts the DC component of the output from 7.5 to 0V. The follower, IC_{14}, provides an impedance high enough, compared to the resistance of the pot, for the latter's calibration to be linear. The attenuator gives switched ranges from 1mV to 3V in a 1:3 sequence. The riaa position is a leaf taken from Ainslie's book[1]. IC_{15} provides the remaining gain necessary to bring the level to 6V.

Due to slew rate limitations the *OP-07* is unsuitable for $IC_{13,\ 14,\ 15}$. The *LF351*, *TL071* and *5534* were tried, simply because they

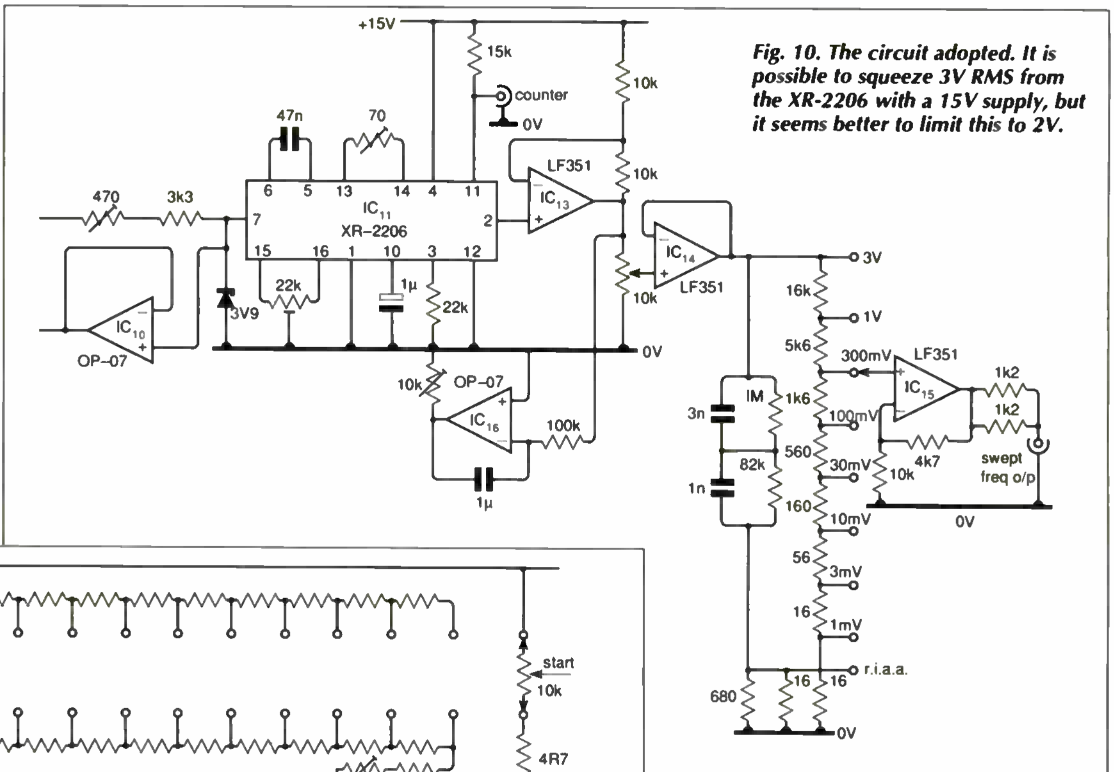
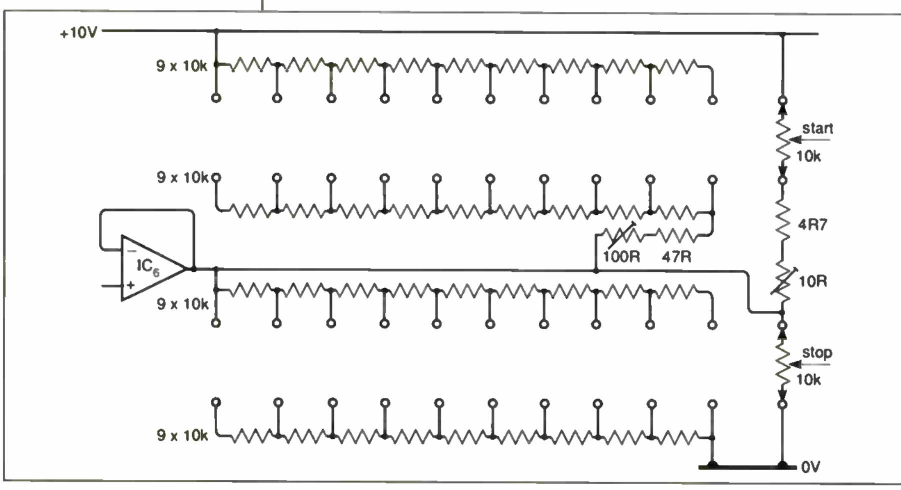


Fig. 10. The circuit adopted. It is possible to squeeze 3V RMS from the XR-2206 with a 15V supply, but it seems better to limit this to 2V.

Fig. 9 (below). Ten-turn pots used on their own for the start and stop controls would give a resolution of 2kHz/turn which is rather coarse. The arrangement shown improves resolution to 200Hz/turn by allowing each control to cover a selected 2kHz section of the range.



were to hand, and work satisfactorily. There must be many more which are equally suitable. Any off-set which would otherwise appear is compared with 0V in the integrator which drives pin three in the correct sense to null the output to zero.

Sine purity is adjusted by first setting the variable on pins 15 and 16 to its mid point, adjusting the variable on pins 13 and 14 for minimum distortion and finally trimming on pins 15 and 16.

Pin 11 is an open collector output from which a square wave may be obtained.

Frequency calibration is simple. With the START and STOP controls at their minimum and maximum positions respectively, S_2 is set to read the stop frequency. With S_2 then set to read the start frequency, the 10kΩ variable at IC_6 output is adjusted to give the stop frequency divided by 1000.

Since the variable on pin seven serves to shift the whole frequency range up or down it is then used to set the start frequency to 20Hz. If range switching of the start frequency is incorporated, then the 100R variable too would need to be set for 20Hz.

Other frequency sweep ranges may be added simply by switching in different values of C on pins five and six and a separate set of identical valued R on pin seven for each range required. A logarithmic sweep[1] was not a design requirement but it should be relatively easy to incorporate such a facility, switching it in after IC_6. A useful addition would be a peak hold circuit. That proposed by Wannamaker has a dynamic range of 40dB[5].

Alternative ramp generation

Finally, some thoughts on applying similar dimensioning techniques to a rather different method of ramp generation, suggested by Wannamaker, may be of interest. His method uses a 555 to clock a 12-bit counter whose outputs feed a D-to-A converter. The D-to-A converter output is the ramp which is scaled in subsequent stages, whose adjustments interact. Something on the lines of **Fig. 11** would be easier.

Start voltage is subtracted from the stop voltage and applied as V_{ref} to the D-to-A which produces a ramp whose absolute amplitude is the difference between them. The start voltage is then added, as is the voltage at pin seven, and inverted before being applied to the timing resistor. Given a D-to-A with a separate analogue ground pin it should be possible to simplify even further on the style of **Fig. 12**. ■

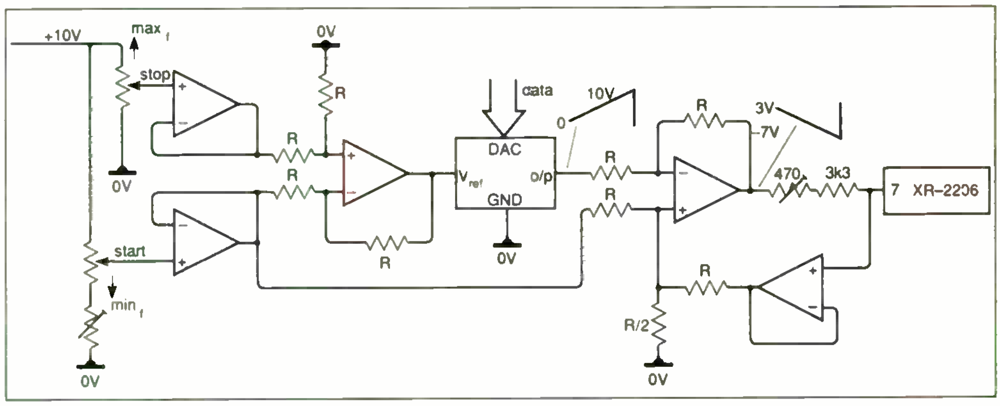


Fig. 11. Alternative method of ramp generation.

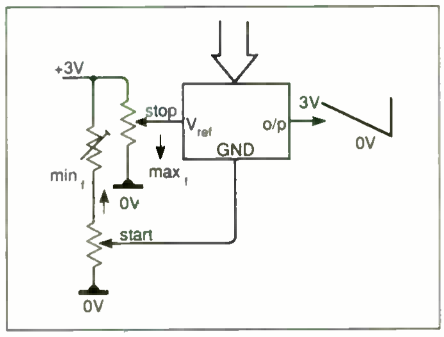


Fig. 12. Simplified circuit for alternative ramp generation given a D-to-A with a separate analogue ground pin.

References

1. AC Ainslie, *Wireless World*, September 1979, pp. 42-47.
2. DM Bridgen, *EW + WW*, March 1991, p. 240.
3. XR2206 Data Sheet, Exar Integrated Systems Inc, May 1977.
4. Exar Application note.
5. J Wannamaker, *Radio Electronics*, Feb 1991, pp. 43-49+70, Mar 1991, pp. 55-62.

BOOK REVIEW

Dished! The Rise and Fall of British Satellite Broadcasting: Who killed BSB? Or, more accurately, what? Britain's "official" satellite TV station transmitted for little over six months, before being consigned by its shareholders to a "merger" in which it was all but obliterated by its supposedly-equal partner and former rival, Sky.

Dished! The Rise and Fall of British Satellite Broadcasting, chronicles the extraordinary events in which a massive capital project (second only in size to the Channel Tunnel), funded by some of Britain's bluest of blue-chip companies - Granada, Reed, Pearson - went horribly wrong.

Technology emerges at an early stage as the most likely culprit. Not so much the D-mac transmission system, required by the IBA, as the interface, which had to be designed to go between the D-mac chip in the receivers and the scrambling system. (Eurocypher, developed in America by General Instruments, in a bizarre sideline, was ruled "too secure" by Britain's GCHQ which claimed the right to hack it, but found it couldn't).

It was the endless "iterations" (ITT-speak for the process of development, and a word which BSB chief executive Anthony Simonds-Gooding was to say was written across his back) of the interface chip 2285 which forced the postponement of BSB's launch. Originally scheduled for September 1989, it had already been upstaged by Rupert Murdoch's launch of Sky in February. The move had been fairly disastrous, with low receiver availability and little consumer interest.

Had BSB been able to start on time, the situation might have been retrievable. As it was, it lost the first peak selling season.

But at least when it did start in April, it reasoned the four specially-chosen manufacturers would have plenty of sets ready in the shops. They didn't. Wary of BSB's financial situation, they had held fire, and then had been plagued by chip failures. It was the Sky launch all over again, only worse, because BSB had been hyping itself for so long.

The famous squarial, incidentally, was a red herring. Although only a wooden dummy at its own launch, it could have been replaced at any stage, and eventually was – by an ordinary dish.

Surrounding all this was a management team whose conspicuous profligacy – both in programme deals, status and enhancing accoutrements (such as Marco Polo House itself) – was outshone only by a total ignorance of the technology it was dealing with. There is a school of thought which holds that BSB was just coming good in the autumn of 1990 when the shareholders threw in the towel and saw the chance of a merger with the cash-strapped Sky. Perhaps.

Dished! is long on detail, on this and most other matters – the history is inevitably in part one of Sky's development as well - but is short on analysis, and avoids drawing conclusions. The facts are there, conveyed with restrained humour, but this is a do-it-yourself whodunnit.

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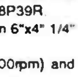

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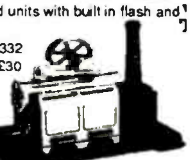

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Opto-bias basis for better power amps

Ivor Brown describes how the opto-bias system can set DC biasing current to a predetermined level in the class AB stage of the amplifier

Operation in class AB retains advantages of both class A and class B systems. Techniques such as negative feedback are often used to attain linear operation, as assessed by harmonic distortion measurements. But for controlling DC biasing current I_q, near enough is usually felt to be good enough. Device tolerances mean it will probably have to be set up for each individual amplifier. Unfortunately inclusion of adjust-on-test components increases production costs as well as being a potential source of error. I_q also varies as devices heat up, so some "thermal compensation" is normally found in class AB circuits, using a sensing device operating at the same internal temperature as other transistors in the circuit. Typically changes in a forward junction voltage drop are used to reduce the variation in I_q, as in the well known V_{be} multiplier circuit. But owing to physical separation of the devices, thermal time constants etc there is no way that this process can be accurate.

Compared to class A, class AB designs do not require large heat sinks as I_q contributes little to the overall power dissipated in the devices. Obviously it is uneconomic to use larger heat sinks than necessary. But if I_q increases and its contribution becomes significant, the system may become thermally unstable and destroyed – not an unknown occurrence in my experience.

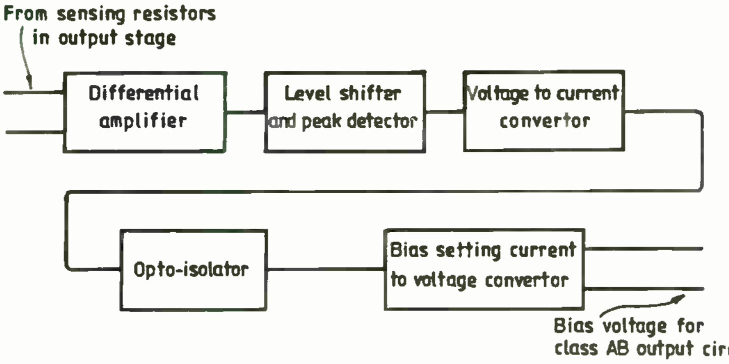
The need to keep I_q within bounds places restrictions on output stages. As each half of the circuit operates in a non-linear manner, local negative feedback cannot be applied.

In general, having a high gain in each half of the circuit – which could usefully be employed to improve signal performance – also indicates a sensitivity to temperature effects and a poor bias stability.

I_q will also vary as the supply rail voltages alter with signal level, variations that can be rapid and introduce distortion products into the amplifier[1] so must be considered in the amplifier design process.

Long term stabilisation of I_q is unlikely to play a significant part in improving a design that suffers power supply related distortions.

Fig. 1. In the opto-bias system a wide band differential amplifier is followed by a fast peak detector enabling I_q to be sensed independently of the signal. Current through the led in an opto-isolator is controlled by the resulting DC level and the photo-transistor current controls the bias.



Opto-bias capabilities

In the opto-bias system, **Fig.1**, a wide band differential amplifier is followed by a fast peak detector enabling I_q to be sensed independently of the signal. Current through the led in an opto-isolator is controlled by the resulting DC level and the photo-transistor current controls the bias of the class AB stage in the amplifier, setting I_q to a predetermined level.

The essential component is the isolator, providing a coupling into the amplifier down to zero frequency, without affecting voltage level at the coupling-in point. Some component values are specific to the amplifier being controlled, so a universal design is not possible. But given that the circuit is correctly designed for a given amplifier, there is no need for adjust-on-test components.

Immediately after switching on, the amplifier must have a low or zero I_q. After a suitable delay, allowing conditions in the amplifier to settle, the control circuit then increases I_q to the operating value. The circuit must not be affected by the audio signal

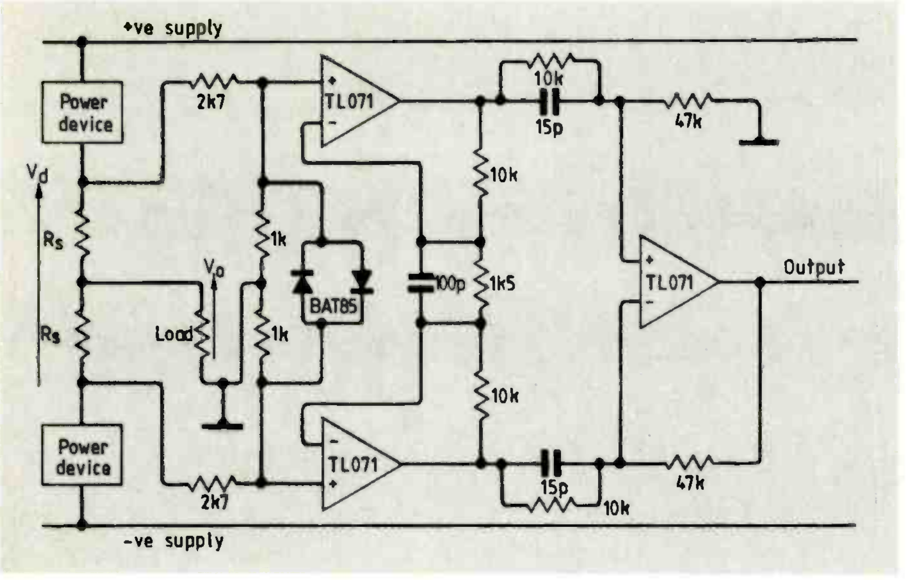


Fig. 2. The differential circuits fed from a typical amplifier output arrangement with resistors (R_s) in series with each power device.

so it must incorporate a long time-constant and operate slowly. Systems reducing I_q to its working value from some higher value are most unlikely to be successful.

Differential amplifier and attenuators

All the operational amplifier integrated circuits used in the system operate from stabilised ±15V rails, limiting the peak signal that can be handled to about 13V.

Figure 2 shows the differential circuits fed from a typical amplifier output arrangement with resistors (R_s) – small compared to the load – in series with each power device.

With no audio signal present the voltage across the two resistors (V_d) is a DC level. When the output voltage (V_o) is sinusoidal, V_d approximates to a full wave rectified sinusoid. But the troughs will not fall to zero, or be sharply pointed due to I_q flowing in the resistors at the zero crossings of the signal. If I_q remains the same, the troughs will be at the "no signal" DC level.

Common mode signal is virtually the same as amplifier output, so attenuation will be necessary between the power amplifier and the current sensing circuit – the amount depending on the amplifier's maximum power output. (Gain equations for the basic amplifier circuit are derived in the appendix.)

The V_d waveform contains components well above the audio frequency range so wide bandwidth and high slew-rate are required. Low offsets and low noise are necessary because the system is DC coupled with a small differential input. But output of around a volt is required as the following circuit incorporates a fast op-amp – not a low noise and lowoffset device. The conflict makes compromise necessary.

With high frequency-boosting capacitors added to the basic circuit the components shown are satisfactory up to 100W in 8Ω, with an R_s of 0.47Ω. Assuming I_q remains the same, increasing the power above this figure may require faster devices as the troughs of the V_d waveform will be sharper.

The wanted signal is much smaller than the unwanted common mode one, so a good common mode rejection is essential. To preserve the balance of the circuit, accurate components must be used and inexpensive 1% metal film resistors are now widely available. The resistive attenuators avoid overload by the common-mode-signal of the two input *TL071*s; the Schottky diodes between the attenuators avoid V_d saturating the third one for outputs approaching the maximum.

Differential gain of the system shown is 16.9. Neglecting offsets, a quiescent current of 50mA gives a trough and "no signal" output level of 796mV.

Level shifting peak detector

The detector is an inverting circuit built round an *LM6361* fast op-amp (**Fig. 3**). To appreciate its operation, suppose that it were simply connected as a unity gain inverting stage with a single 10K feedback resistor. It has two input currents, one the output of the differential stages and the other DC from the negative supply rail. The former by itself would give an output always below ground with the I_q sensing troughs appearing as the positive limit of the waveform. But the DC input raises the level of this waveform so that these peaks are above ground.

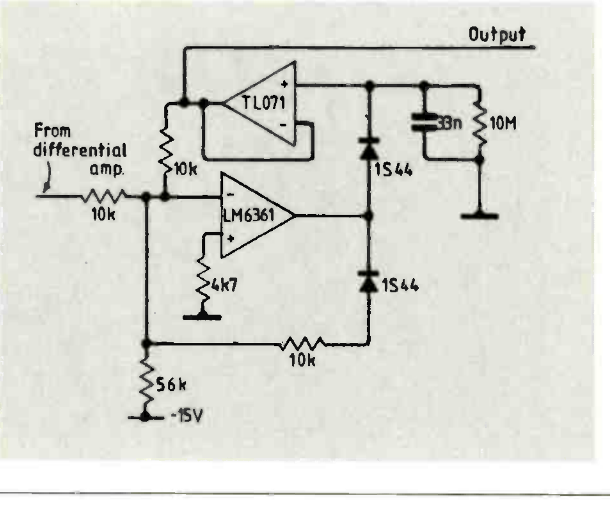


Fig. 3. The detector is an inverting circuit built round an LM6361 fast op-amp.

In the actual circuit, when the output is positive, feedback is via the upper diode, the *TL071* buffer stage, and 10K resistor. The lower diode and 10K resistor ensure that the output cannot be driven into negative saturation. The circuit must respond to peaks of short duration, so the charge storage capacitor must be small; but these peaks may occur infrequently, so a long storage time constant is required.

The time constant plays a part in determining stability of the loop and it must be defined – values shown are suitable compromises. Output is taken from the buffer.

Opto-isolator and biasing circuit

The opto-isolator and biasing circuits are shown in **Fig 4**. For the present ignore the components round T_1. Detector output feeds a *TL071* voltage to current convertor via the first order low-pass filter made up from R_{1a}, R_{1b}, and C_1 (why this has a pole and a zero in its response will be explained later). Resistor R_3 defines the current in the isolator's led and its phototransistor sets the current through transistor T_2 and T_3 and hence the voltage across R_2 (V_b), which is used to bias the amplifier.

C_2 is across R_2 to avoid variations in V_b due to noise rom the isolator. Note that R_2 is between two collectors so its DC level can be defined by other parts of the amplifier circuit. No component values are given for this part of the circuit as they depend on the amplifier being controlled.

After switch-on, transistor T_1 is saturated while the 33μf capacitor charges, and holds the input voltage to the isolator driving circuit close to zero. This allows amplifier conditions to settle before the biasing circuit slowly takes control. Rapid discharge of the capacitor after switch-on and that the circuit will work again or an immediate switch-on is ensured by the diode. After T_1 has come out of saturation, rate of change of voltage across R_3 can be used both to inhibit the input until the correct operating conditions have been established, and to indicate when the amplifier is ready for use.

Loop time constants

As previously discussed, the circuit must contain a long time-constant. But the one involving the storage capacitor in the detector is non-lin-

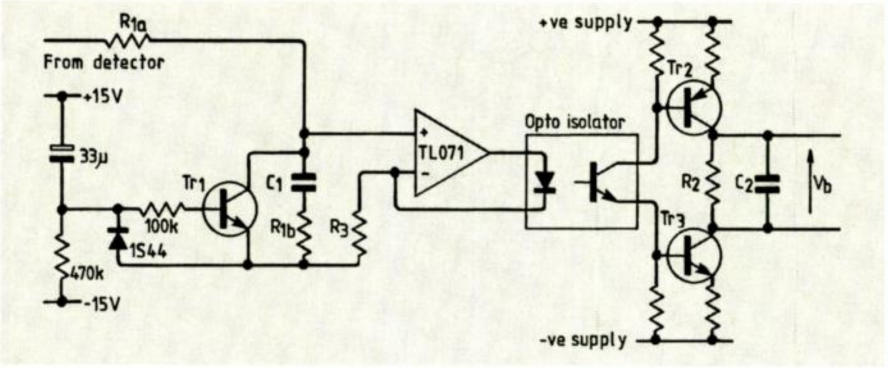


Fig. 4. Opto-isolator and biasing circuits. The detector output feeds a TL071 voltage to current convertor via the first order low-pass filter made up from R_{la}, R_{lb}, and C_l.

ear: when I_q falls the capacitor will quickly charge; when I_q rises the charge can only leak away slowly. If all the additional low-pass filtering were done by C_2 and R_2, the capacitor would have to be very large. A better method is to do some filtering before the voltage to current converter at a higher impedance level. This R_{la}-R_{lb}-C_l filter has a zero at about the same frequency as the pole of the R_2-C_2 filter, so obtaining an overall first order roll-off, with a time constant much greater than the discharging one in the detector.

The ratio necessary between these time constants depends on the amplifier being controlled.

Test conditions.

It is clear that the circuit can perform as intended for only a limited range of waveforms, so the choice of valid test signal is important. The time taken for signals to traverse the region where both power devices are conducting is a vital consideration. A full-power sinusoid at 20kHz has the fastest transitions likely to be encountered in practice. But the zero crossings are only 25µs apart and the signal will not test the low frequency capability of the circuit. A better choice is a maximum amplitude 50Hz square wave passed through a first order 20kHz low-pass filter. The zero-level rate of change of voltage is the same as that of the full-power 20kHz sinusoid, although the zero-crossings are separated by 10ms.

Voltage across the storage capacitor will sag by about 3% with this waveform. However provided the sag is small, and that the fall can be assumed linear, the circuit is self compensating. First order filtering will reduce the variation of I_q to a very small amount and average I_q will be unaltered.

Opto-bias amplifiers operating successfully with this test waveform have given no problems when used to reproduce music. If a waveform is used with transitions that are too fast, the system is fail-safe; the output waveform of the differential amplifier will not fall far enough and the detector will sense that I_q is too large.The result is that I_q will be reduced and distortion will be present in the amplifier's output. Removal of the offending conditions will allow the opto-bias loop to recover.

Further developments.

As regular readers will know my research at Brunel University is concerned with the optimum use of mosfets in audio power amplifiers. An area where design[2, 3] can be improved is the thermal compensation arrangement involving a secondary heat sink. The biasing control circuit has been designed with this in mind. Practical work confirms that the opto-bias system does not impair audio performance.

What is more, free from thermal constraints it is likely that even better, and higher power, output circuits can be designed.

Initial work suggests that wideband class AB output stages with distortion figures of around 0.1% are possible. As the distortion products are mainly low order, these power stages should form the basis of very high quality power amplifiers. ■

Amplifier basics

Most audio power amplifiers operate in class AB, with two active devices, bipolar transistors or fets, connected in series between the symmetrical positive and negative power supply rails and the load taken from their common point to ground.

For large output voltages only one device is conducting, passing a controlled current into the load; polarity of the signal determines which device is conducting. When output approaches zero both devices conduct so that transfer of current between them is relatively gradualto reduce cross-over distortion.

Under quiescent conditions, ie no signal, a DC biasing current (I_q) flows in both devices.

In class A amplifiers I_q is large so that both devices are always conducting, the difference between their currents appearing in the load. In class B circuits I_q is zero – so cross-over distortion is to be expected – but class B are more efficient than class A.

References

1. Ball. "Distorting Power Supplies", *Electronics World and Wireless World*, December 1990.

2. Brown. "Feedback and fets in Audio Power Amplifiers", *Electronics World and Wireless World*, February 1989.

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Appendix

The basic differential amplifier is given in **Fig. 5** with voltages indicated at points in the circuit. When analysing linear op-amp circuits it is important to realise that the voltages between the inputs will tend to zero. (If the gain tends to infinity, and the output is infinite, then the input must tend to zero.)

Using the super-position theorem, consider the common (V_c) and differential (V_d) components of the inputs separately. With just V_c at the non-inverting inputs, there is no current in the R_a-R_b-R_a chain and all pins of A_1 and A_2 are at the same voltage. With $+V_d/2$ at one input and $-V_d/2$ at the other, there is a current of V_d/R_b in the chain. Hence the voltage across the chain is $V_d(2R_a+R_b)/R_b$, with equal and opposite components appearing at the outputs of A_1 and A_2. Summing the V_c and V_d components gives the voltages shown.

Super-position can be used again for the rest of the circuit. Call the previous outputs V_x and V_y. Let $V_y = 0$; V_x is attenuated by $R_d/(R_c+R_d)$ before being amplified by $(R_c+R_d)/R_c$, hence the output is V_xR_d/R_c. Now let $V_x = 0$ so that the non-inverting input of A_3 is at zero.

The circuit behaves as a simple inverting amplifier with an output of $-V_yR_d/R_c$. Summing these components gives an output of $(V_x-V_y)R_d/R_c$, and substituting for these voltages gives the output indicated.

The A_3 part of the circuit is, in theory, a perfect differential stage by itself, but in reality its performance will suffer from the practical limitations of the amplifier and component mismatch. A_1 and A_2 provide appreciable differential mode gain but only unity common mode gain, thereby easing the task of the differential stage.

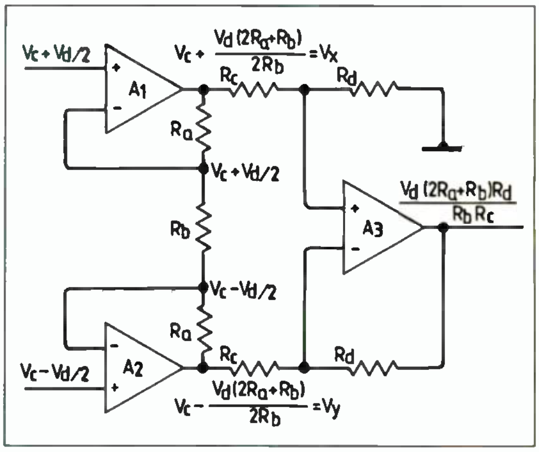


Fig. 5. Basic differential amplifier with voltages indicated at points in the circuit

Analogue data storage – speaking of the future?

Phone callers 'on hold' could be greeted with a real voice on the end of the line thanks to a new technique for storing analogue data. Andy Wright looks at a new type of silicon chip which provides long term storage of analogue signals in analogue form.

At the International Solid State Circuits Conference held last year in San Francisco, details were given of a new semiconductor process for storing analogue rather than digital data. The technology could open up a whole new generation of electronic products designed to store and play back natural voice data.

Analogue data storage has been around for a long time. The first programmable machines used metal templates to turn out products that were identical every time. The invention of the phonograph allowed analogue wax cylinders to store sound from a horn microphone; the cylinders were later replaced by shellac and vinyl discs (remember vinyl?) as the primary means of storing large amounts of audio data. Today the market is dominated by analogue audio tape and has been further extended with the introduction of compact discs.

These examples all suffer the obvious disadvantage that they rely on mechanical parts, which break and wear out. Electronic components are less likely to. In the solid-state field, digital storage has dominated since the advent of the magnetic core device.

Audio data needs to be quantized in two dimensions - amplitude and time - before it can be recorded or stored. This means that one storage cell is needed for each bit of the digital amplitude sample. Eight bits corresponds to a reasonable representation of voice amplitude, giving 256 levels and a minimum quantization error of around 0.4%.

Clearly, better signal quality could be gained if each sample were stored as one of an infinite number of levels. In the early 1960s there were unsuccessful attempts to do this with magnetic core memory. However it wasn't until February 1991 that the US company, Information Storage Devices, succeeded in making solid-state analogue storage a commercial reality.

ISD's first product is capable of recording and playing back a 16 second analogue signal, with signal-noise ratio of better than 35dB, a 3dB 3400Hz bandwidth and total harmonic distortion better than 2% at 1kHz. All this from a single IC.

In 1987, Richard Simko, a physicist and inventor of integrated circuits, had the idea that floating gate devices - the basic transistors of an eeprom - are inherently capable of analogue storage. Together with Michael Geilhufe, a long-time associate, who worked on manufacture of the technology, he formed Information Storage Devices in December 1987. It took more than two years of development before they could show working silicon for the first time.

Today there is a range of devices to suit various message lengths and bandwidths. The ISD1012, 1016 and 1020 handle various requirements by programming the sampling rate into silicon during manufacture. A 6.4kHz sample rate is used to give a recording duration of 20 seconds, providing the 1020 with a 2700Hz pass band.

With the 1012, an improved signal quality (4500Hz pass band) is gained at the expense of reducing recording time to 12 seconds. The ISD1016 is a compromise solution: 16 seconds of recording with a telephone-grade pass band of 3400Hz and a sampling rate of 8kHz.

Theory

What all three devices have in common is an array of 128,000 patented analogue storage cells. Where traditional eeproms use the floating gate to store a high or low value corresponding to a 0 or 1, the analogue storage cell applies the programming and erase voltages in a more controlled fashion so that floating gate charge values represent the true analogue level.

Using this process, the amount of charge on a floating gate can be retained for many years, and the cell's voltage can be sensed without disturbing the charge. By measuring the cell's conductivity, a reading can be taken that corresponds to the value of the analogue level stored.

While there are variations, especially over time (as charge decays), ISD's process ensures that these can be compensated for between different ICs and between different cells in the same IC. Variations caused by aging, process variables and thermal characteristics are all calibrated out.

The eeprom-based process brings the additional major advantage of non-volatility. Retention time is claimed to be 10 years, and the devices are specified for up to 10,000 read/write cycles. However, this is necessarily subjective. Failure of one or two cells will only show up as lower fidelity - unlike digital RAM where single bit errors can be catastrophic.

Techniques for monitoring the device's integrity are very different in comparison with those for digital alternatives. Failure of a digital storage cell can be detected by - for example - checksum errors, whereas the analogue cell lends itself to tests more closely allied to traditional audio methods. Factory testing makes use of methods such as signal-noise and SINAD (signal/noise + distortion).

Architecture

As the block diagram (**Figure 1**) shows, the inventors had many more engineering problems than the simple transformation of eeprom storage from digital to analogue. The technology involves a great deal more.

Incoming signals are first conditioned with an automatic gain control and anti-aliasing filter. An on-chip sampling clock then enables the input signal to be put through special transceivers into the analogue storage array. Play back is through an integral smoothing filter and amplifier, providing direct drive for loudspeakers with impedances down to 16Ω. Also on-chip is a smaller eeprom array - this time digital - for storing addresses and reconfiguring chip control functions. To keep silicon real estate to an acceptable level, address space is just 256 bits, catering for 160 analogue addresses. External pins allow the user to access control functions such as power down, playback/record, chip enable and end of message. There is also a test pin reserved for factory operations.

Solid-state tape recorder

The simplest and most obvious application is as a solid state tape recorder with manual operation. The only external parts required are a microphone, loudspeaker, and switches (see diagram, **Fig. 2**).

For practical applications some more thought and circuitry is required, to reduce noise and distortion. For example, it is necessary to decouple the microphone power supply from the chip, bias the microphone and set the audio attack and release time constants. A typical circuit design is shown in **Figure 3**.

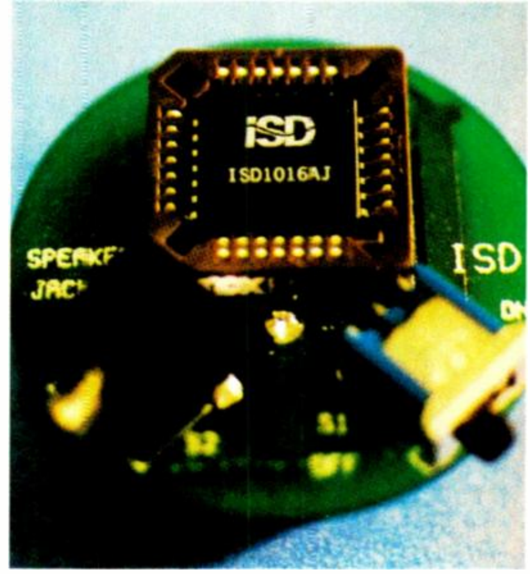
Pulling pin PD low powers-up the chip, which requires a single 5V supply. To record, pin P/R is set high and then, when the CHIP NOT ENABLE pin is made low, recording begins. It is ended by pulling that pin high. Play back is essentially the same procedure, this time setting the device into play back mode by setting pin P/R low.

This type of implementation gives a good demonstration of the chip's capabilities, and it can have practical real applications. For example, it could be used to record and play back outgoing messages on an answering machine, although it will have to provide more than 16 seconds of telephone-quality speech before it can handle incoming messages.

Part of the solution to this limit is a simple facility for cascading two or more analogue storage devices. No complex circuitry is required. To record, all designers need to do is connect the analogue out pin of the first ISD chip to the analogue in pins of the others via a capacitor (see **Fig.4**).

The speaker output pin of each device is connected to the **Aux In** pin of the previous one in the chain - except in the case of the first chip, which drives the speaker. During both recording and play-back, the END OF MESSAGE output is connected to the chip enable pin of the next device in the chain.

As one device reaches its analogue storage capacity, the voltage on the end-of-message pin goes low, selecting the next chip auto-



A practical solid-state tape recorder that incorporates ISD analogue storage devices (photo courtesy of Sequoia Technology).

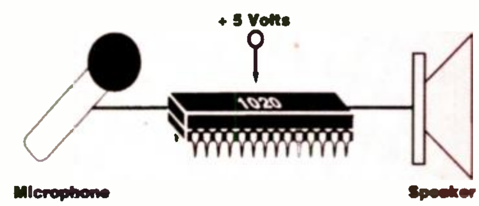


Figure 2. A simple solid-state tape recorder represents the most obvious application for the technology.

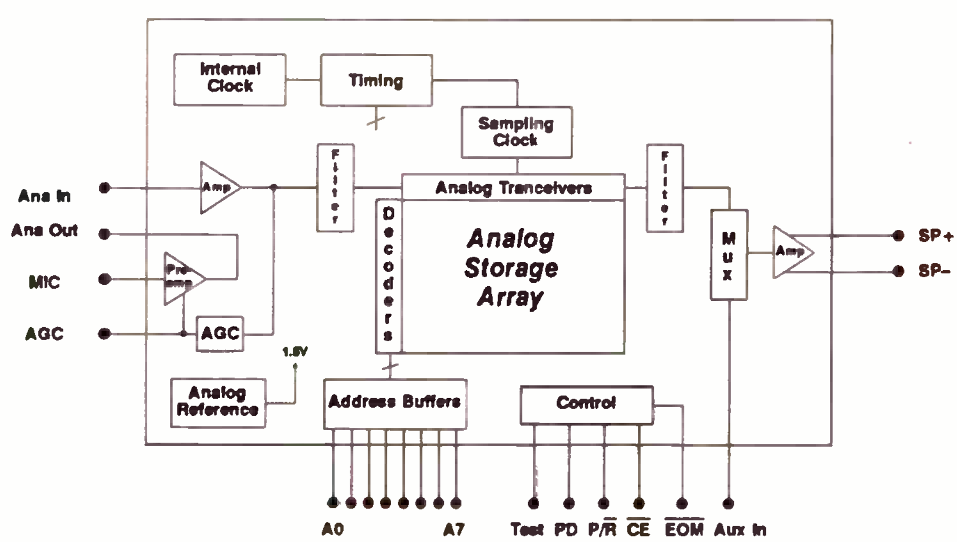
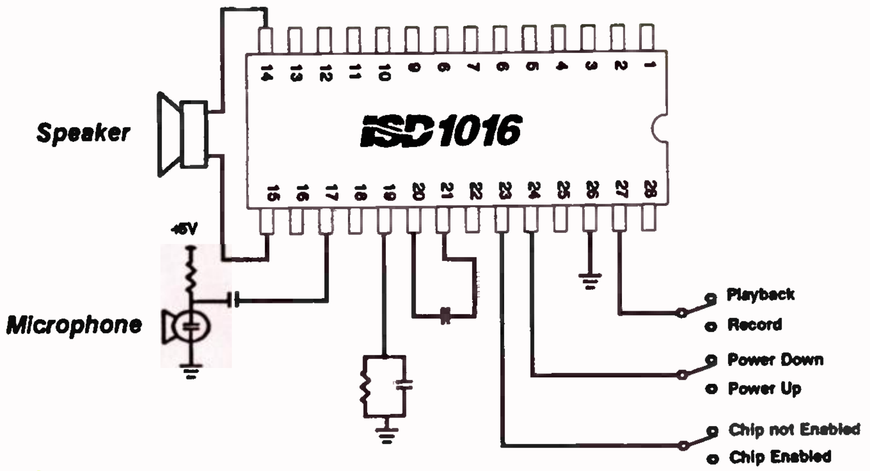


Figure 1. Schematic of the ISD1016 architecture - a compromise device that gives 16 seconds of recording at an 8kHz sampling rate.



matically. This digital handshaking is immediate and prevents noise and message gaps during chip-to-chip transitions. ISD reckons that up to 10 devices can be daisy-chained in this way without analogue buffering. This gives around three minutes of speech with the 20-second ISD1020.

A further feature to widen the applications of this technology is the ability to loop the 'tape' continuously. This makes it suitable for applications such as music- or message-on-hold machines. The advantages to the end-user - the caller waiting for someone to answer - are obvious: he or she hears real music or a natural voice instead of synthesized 'musak'.

The compact size and low power consumption of the device are already creating wide interest with designers of portable equipment such as mobile phones or pagers. One application that has already benefitted is the hand-held line-of-sight FM transceivers being built by a US company for civil defence and emergency services. Here it serves as a cache in voice store-and-forward systems.

Another way in which the new device really scores over conventional magnetic tape systems is that its designers have made

Figure 3. Using the solid-state tape recorder under manual control requires a little more thought and circuitry to reduce noise and distortion.

it truly random access. This allows the recording to be divided into chunks, each instantly and individually replayable.

Random access

The ISD1016 divides its 128,000 cell array into 160 segments, each storing a 100ms signal. The start address of a recording is set via eight external pins. When the recording is stopped, an end-of-message marker is written to mark the final location in the analogue array. Play-back begins from the relevant addressed location and normally continues until end-of-message is detected.

This means that several short messages can be stored in the same chip and accessed instantly. The technique could therefore be used for playing back single word commands or alarms. For example, in a telephone it could give verbal feedback of the number dialled.

An obvious development from this is to store the appropriate DTMF dialling tones as audio signals alongside each digit. Being able to store short phrases or words suggests that these could be combined under software control to provide simple messages such as instructions or directions. Messages like: 'take the Central line to Oxford Circus then change to Bakerloo' or: 'phone the office' could be constructed from basic words stored in the device.

Sampling clock

It is perhaps worth mentioning how important it is for the on-chip sampling clock to be accurate. A difference as small as 2% between the sampling frequency during playback and recording can be perceived as a change in the speaker's mood, which is particularly important when the device is used to convey critical voice messages.

Speech researchers and psychologists tell us that frequency is important in conveying urgency, alarm or reassurance, so an alarm message played back too slowly may not have the desired effect. Not surprisingly therefore, ISD's on-chip clock - accurate to ±1% - is the subject of a number of patents.

Such accuracy is one of the keys to overcoming consumer resistance. Early attempts at building synthetic speech, for example into automotive applications, were dogged by accusations that the 'voice' sounded too patronising or nagging. Better solid-state reproduction could make voice output much more acceptable.

As the public gets used to machines that talk, they could soon be everywhere - from microwave ovens and TVs, ECG machines and vending machines, to hand-held computers and toys.

Alternatives

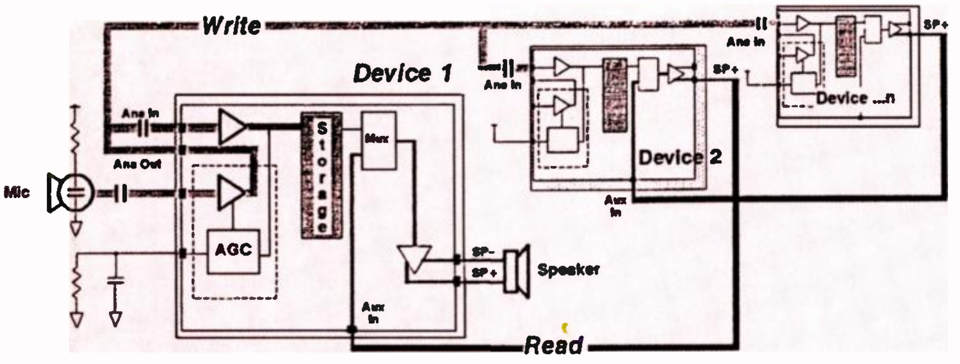
The demand for speech input and synthesis technology has been so great that several alternative solutions were developed before the advent of analogue signal storage. One of them is from Texas Instruments, which has developed a single-chip speech synthesizer using conventional memory technology.

To overcome the problem of storage density, it compresses the data by a technique known as linear predictive coding. The result is that up to 1.5 minutes of speech can be stored on-chip. Where larger amounts of speech data are required, they can be stored in adjacent speech memory.

As to speech quality: that is in the ear of the beholder. The only test is to try it for yourself. For my money, give me the analogue sound any time.

Moving on from the myriad voice applications, the uses of this new technology spill over into a huge market for analogue, audio frequency data storage and playback. In industry, the chips could be used as local storage for data loggers, monitoring or

Figure 4. The analogue storage devices can be easily cascaded by connecting the analogue in and out pins of separate devices to one another.



acquisition systems. Remote geophysical stations could use the device to record transient seismic events, or electricity distributors could use them to store voltage fluctuations. They could even be used in analogue storage oscilloscopes!

As playback devices, they could find their way into waveform generators and signal sources. By storing DC instead of AC signals, such devices could become the heart of a new programmable voltage source, with up to 160 DC levels available instantly.

Even wider possibilities can be envisaged for systems based on multiple devices. By synchronizing the record/playback start time, there are potential applications in X-Y positioning systems, robot controllers and CNC machines. The list is so long that the phrase 'only limited by the imagination' is no longer a mere cliche.

Future developments

Looking to the future, the growth and development of this technology depends to a large extent on where the market takes it. It may be that most people want to use the devices as annunciators - a kind of worm (write once read many) device. For them, the front-end AGC circuitry, designed to accommodate microphone input, would be superfluous. Direct analogue input appropriately conditioned would provide a better quality signal.

Others may see their application as solid-state tape recorders, with no requirement for sophisticated addressing. Yet another group would be looking for alternative sampling rates, and multi-chip modules for longer recording times. Emerging refinements could therefore include cut-down parts with fewer addresses, one-time programmable or read-only devices and other application-specific devices. All these are options; which of them reach fruition will be dictated by market economics, rather than technology.

One thing is certain, however. The current offerings from ISD are based on conservative manufacturing processes, leaving plenty of room to meet demand for higher storage density, without breaking new ground.

A 2μm cmos process is currently being used but it will not be long before the process is scaled to quadruple the recording time. This next generation of analogue storage devices should be able to store around a minute of speech. Improvements in the existing process could quickly bring sampling rates as high as 100kHz and improve signal-noise ratios to around 48dB.

Even further ahead, chips with four million storage cells, sampling at 10MHz and with signal-noise ratios better than 60dB are on the horizon. ISD's Richard Simko believes that his invention will make many multi-chip systems with digital memory obsolete. If he's right, talking systems based on analogue storage will be commonplace by the end of this century.

Crystal ball gazing aside, it's clear that there are plenty of uncharted applications for this embryonic technology. According to ISD, the most interesting – and profitable – uses for analogue storage have yet to be discovered. Designers with imagination: over to you!

References

'IC holds 16 seconds of audio without power.' *Electronic Design*, Jan 31 1991.

Acknowledgements

This article was prepared with the gratefully-acknowledged help of John Culver, Applications Engineer at Sequoia Technology, and Raj Gunawardana of Texas Instruments.

ISD analogue storage devices are distributed in the UK by Sequoia Technology; phone 0734-311882, fax 0734-312676.

Texas Instruments can be contacted on 0234-270111.

RECEIVING TELETEXT ON THE PC

The teletext broadcast service provides a wealth of information in digital form. Importing selected pages into a desktop computer system opens up all sorts of possibilities for information management. Laurence Cook explains how to go about it.

It seems like a lifetime ago that, while adjusting a colour television built from a magazine article, I saw a couple of lines of twinkling dots at the top of the screen and wondered what these signals were. A few phone calls later and I was hooked. Some 120 TTL chips and many late nights later there emerged a monstrous box full of veroboard and rats' nests which eventually burst into life as a set-top teletext adaptor.

Since nothing can stop an idea whose time has come, there were soon many such designs in existence, all using similar techniques.

Advances in technology render earlier designs obsolete and the hot box (all those chips produced more heat than processing power) was subsequently replaced by a neater construction using a patented technique. In this, a 6800 microprocessor examined each data line, which had been DMA'd into memory while the processor was halted during TV frame blanking. A boardful of LSTTL and cmos logic generated the display.

Many readers will be familiar with using PCs to access Viewdata services such as Prestel. The display is handled by standard graphics adaptor cards and appropriate terminal emulation software; the link to the chosen database is provided by a modem.

The teletext adaptor to be described connects to the PC via a serial port. Terminal software on the PC handles teletext style displays and passes page requests from the keyboard to the adaptor itself.

Most households will have one or more devices with a video output (eg. a scart socket on a TV or video recorder) and so the cost and complexity of a tuner can be dispensed with. The adaptor therefore has a video input, RS-232 output, and low voltage AC power input to make a simple design which can be sited near the source of video and linked to the PC using data cable. The circuit board measures around 6 x 4in and has only ten chips on it, making it quick to build.

The task facing a designer of such equipment is essentially simple. Data must be extracted from off-air video, examined to see if it is required by the host PC, and if so captured for onward transmission over a serial link. In hardware terms, the task is fairly simple:

i) Data is transmitted on a row-by-row basis at 6.9375Mbit/s, with one display row per TV data line, on up to 16 lines per frame . Logic 0 is roughly equivalent to black level, and logic 1 to approximately 66% of white level.

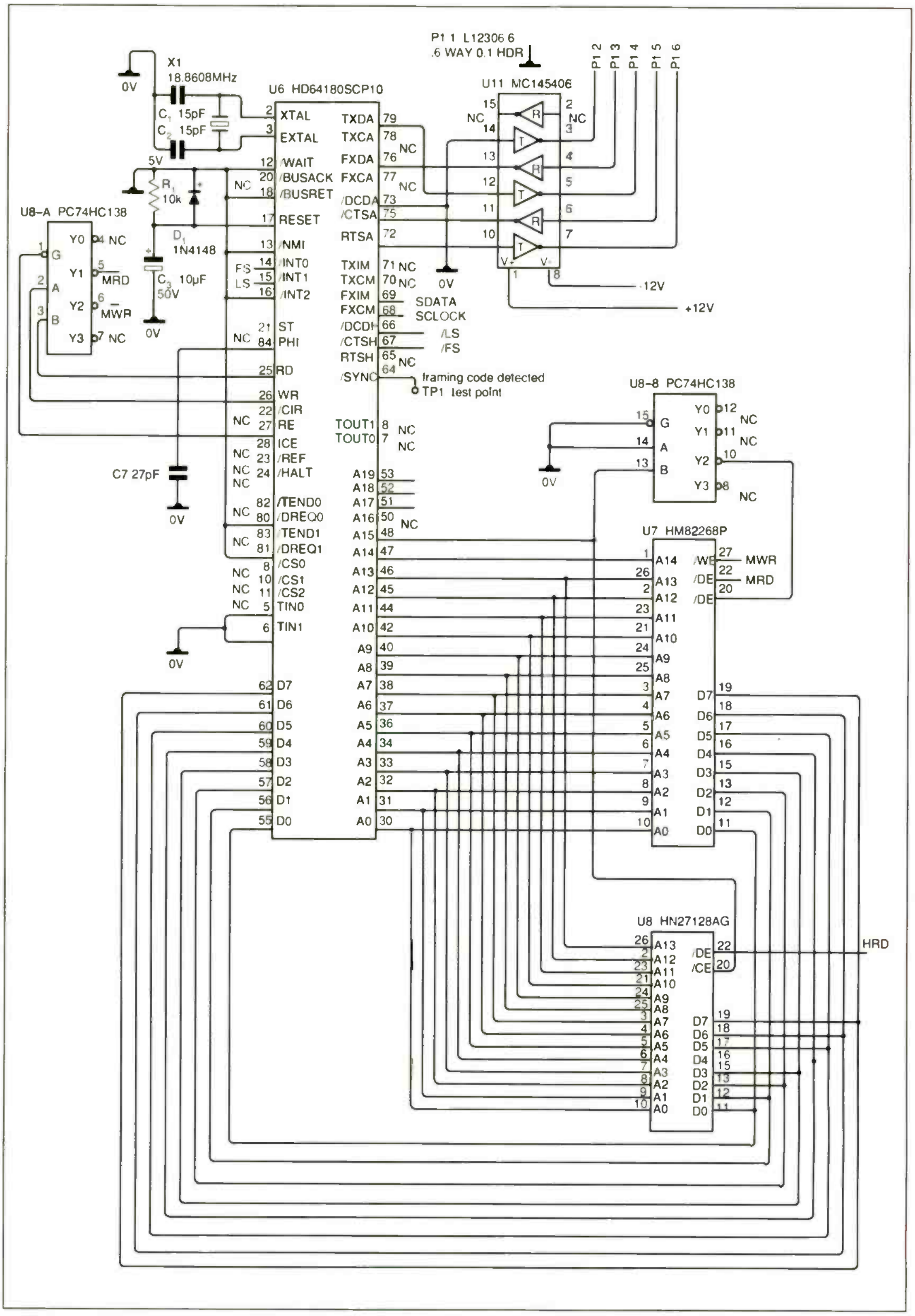
ii) The fastest serial port supported on a PC is 9600 baud, which sets the speed between the adaptor and PC and equates to roughly 1 page per second (four times faster than V.22bis). Buffering in the adaptor is suggested so as not to lose wanted pages.

iii) Each data line starts with a 'framing code' to define byte synchronisation: this is a simple 8-bit pattern which is fixed. This suggests that a high speed SCC could be used to detect framing code and thus achieve byte synchronization, instead of the more usual sipo shift register and pattern detecting logic.

This means that we need a microprocessor, rom, ram, uart (to the PC) and some means of turning off-air video into data and then into ram for later processing. In fact the processing has to be over before the next TV frame arrives with more data since there is no handshaking off an aerial.

One way of doing this might be to halt the processor and use external DMA hardware to do the processing. This design does neither, yet achieves the same result.

The heart of the design is the extraordinary HD64180S Network Processing Unit from Hitachi which contains a 64180 CPU core (running Z80 code). It also includes a two-channel DMA controller capable of cycle-



stealing or burst mode, a multi-protocol serial communications interface (MSCI) capable of operating at 7Mbit/s, a uart easily capable of operating at 9600 baud, two general-purpose timers and a built in clock oscillator circuit able to run at 20MHz.

This sledgehammer will easily crack the problem; all that is needed is some hardware to accept video and turn it into TTL-compatible data and clock and to extract line and frame sync pulses. The solution chosen is a combination of the Philips SAA5231 data slicer and two Nat Semi fast comparators.

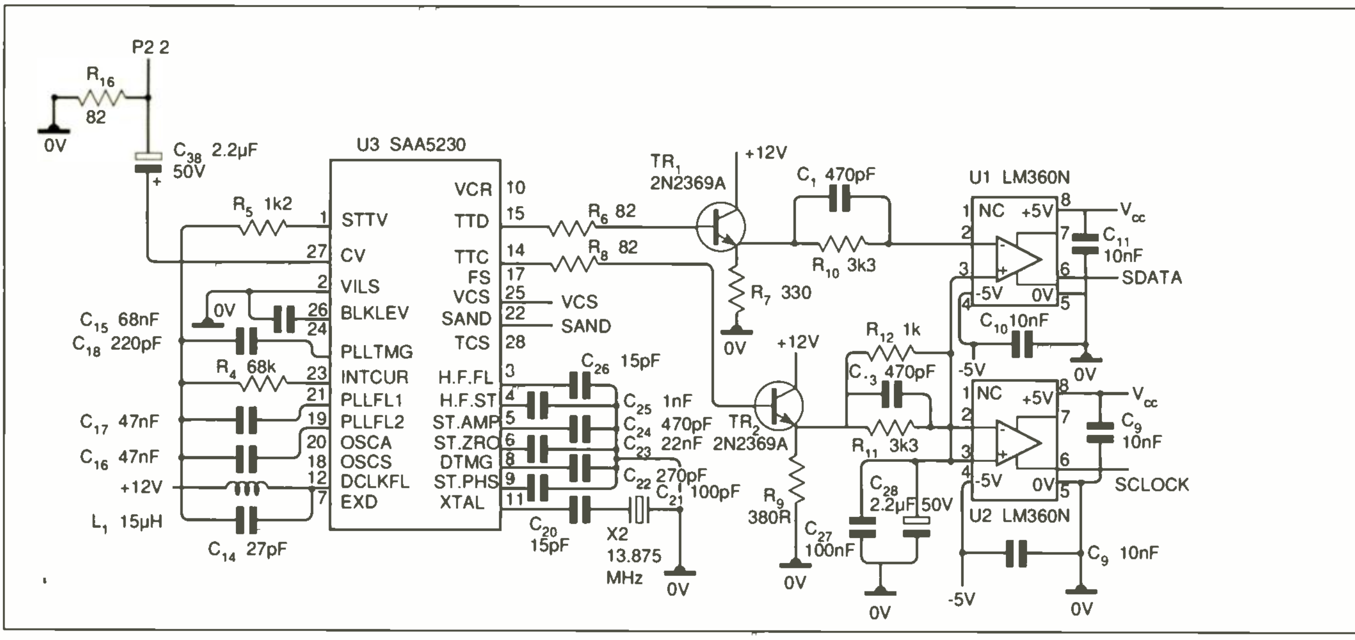
The comparators are needed because the data slicer does not produce TTL-compatible outputs but signals intended to feed other Philips chips in adaptors built into TV sets.The SAA5231 outputs composite sync, which is integrated by a CR network to get frame sync.

U_6 is the NPU which has a 19.6608MHz crystal across its oscillator pins. This might seem odd when the processor can run at 20MHz, but it was chosen to allow exact baud rates (eg 9600), while not compromising the MSCI performance. In fact Hitachi quote a maximum data rate of 7.1Mbit/s at 20MHz. Scaling this for a 19.6608MHz crystal gives a maximum rate of 6.9795Mbit/s which exceeds the 6.9375Mbit/s teletext data rate by a small margin.

The system memory map is unspectacular, with ROM at zero (just as well, since a reset begins executing code from zero) and ram at 32K. This map was chosen to simplify the address decoding so that A_{15} low selects ROM and A_{15} high selects ram. One half of U9 serves as a simple inverter; unusually, the other half serves as a pair of OR gates (logically) to qualify RD and WR signals from the NPU with ME so as to access external memory only for true memory access cycles, not for internal I/O operations such as timer and MSCI accesses.R_1, C_3, and D_1 are a conventional power-on reset circuit. There are no external devices requiring resetting.

U_3 and its directly-connected components

The heart of the device is U6, the HD64180 network processor. It provides a Z80 type CPU core, a DMA controller, a serial comms interface capable of running at 7Mbit/s and a UART.



This part of the circuit takes raw video, strips out the teletext data which it retimes and delivers to U6, the network processing unit.

are responsible for taking off-air video and producing data at pin 15, clock at pin 14 and sync at pin 25. This circuit is taken almost directly from the Philips data sheet on the SAA5231; the only quirk is that, every line sync, the chip expects an 8.5µsec pulse on pin 22 from other members of the chipset. This is provided by U_{10}, a precision monostable, triggered from sync itself.

R_3 and C_4 integrate the composite sync signal to give a frame sync pulse every 20msec. This is fed to the INT0 pin on the MPU to give an interrupt as well as to CTSM, an MSCI handshake line, which is used here as a general purpose input so the firmware can sample this pulse. U_{4B} cleans up the pulse before it is fed to the NPU.

U_1 and U_2 are high performance comparators which serve to produce TTL-compatible data and clock signals to the MSCI in the NPU. Their inputs are buffered by Tr_1 and Tr_2 respectively, C_{12} and C_{13} providing correction for slight HF losses therein. It is essential not to degrade the phase relationship between data and clock as the MSCI requires a clock edge to be nominally central to the data bit period. The comparators should therefore not be substituted unless you know what you are doing!

R_{12} and C_{28} set the DC reference for the comparators at the mid-point of the clock from U_3, so compensating for any DC drift here. This means that any distortion of the data and clock mark/space ratios are avoided. The latter should of course be 1:1.

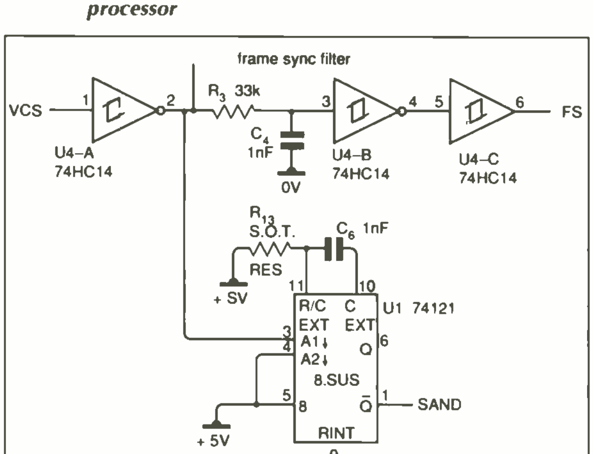
U_{4D}, *E* and *F* were essentially spare inverters, pressed into service as led drivers to aid in firmware development, but now retained, as the leds give a useful indication of signal presence, data quality and PC traffic.

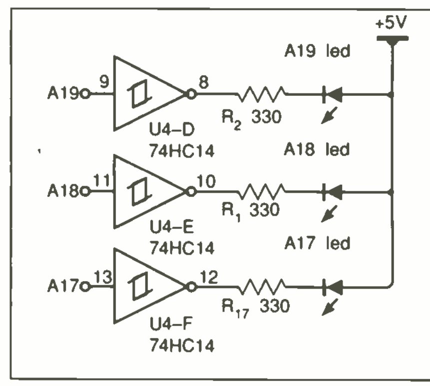
In a real sense this facility 'fell out' of the design; the only trick here was to use high order address lines as parallel output pins by using the MMU in the chip to remap the memory as required. This may seem an odd use of the MMU but it is cheaper than an external latch in I/O space, and the MMU would have been markedly under-used otherwise.

U_{11} provides signal level translation between the logic on board and the real world of RS-232 links to the host PC. The MC145406 is a nice chip for this job and although slightly dearer than the more usual 1488/89 pair it is only one chip and requires no external response-shaping capacitors, unlike its forebears. The ASCI uses TxD, RxD and RTS/CTS handshaking to the PC to avoid loss of characters in either direction.

The only other part of the circuitry that remains to be described is the power supply, although there is little to mention here. The 12V regulator gets quite warm and requires a small heatsink; the 5V regulator also gets warm but runs quite happily within its ratings without a heatsink.

The Frame synchronisation filter takes composite sync from the video signal and feeds a conditioned pulse to the main processor





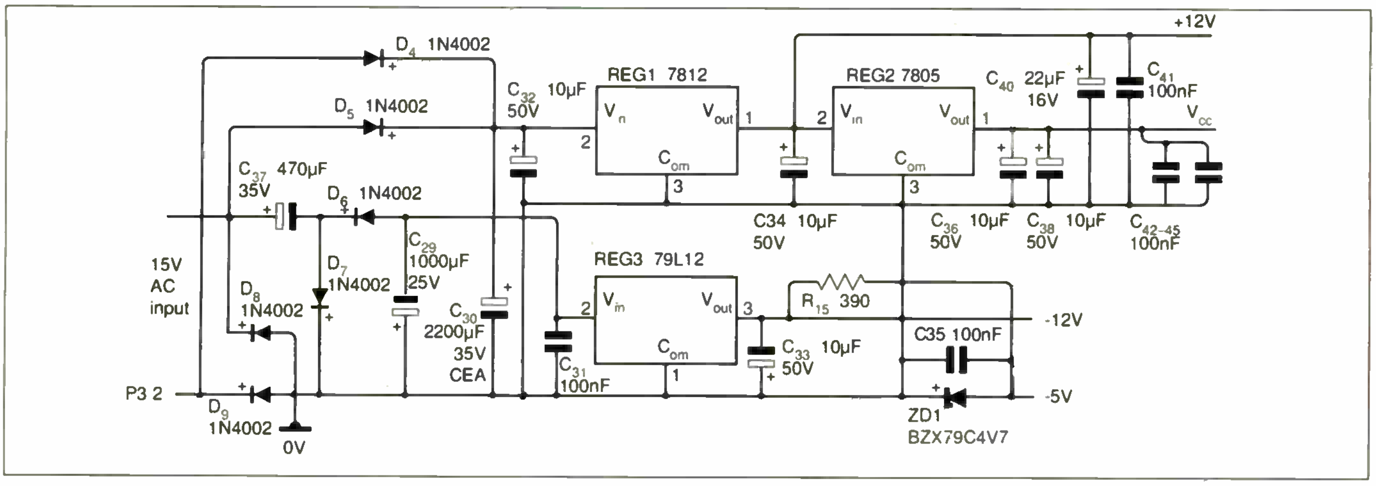
These leds provide indication of signal presence, data quality and PC traffic.

External power requirements are just 15V AC at 200mA max. This can readily be supplied by a plug-top type transformer. Alternatively a small chassis type transformer could be fitted with the circuit board in a small box.

A circuit board has been designed to accommodate the entire circuit. At the time this was being produced the author decided to make provision for an alternative clock source for the microprocessor. This was in case the crystal proved to be erratic if an emulator were to be used to debug firmware.

Note that the NPU is socketed. Anyone who has ever tried to hand-solder such a big PLCC chip will appreciate this luxury, although it also makes it possible to use an emulator pod. X1A is a footprint of a 19.6608MHz crystal oscillator module which need not be fitted unless X_1, C_1 and C_2 are omitted.

Test point TP_1 was provided to monitor whether the SCC was detecting framing code; it too can be omitted



Power supply circuit. The 15V mains transformer, which has to deliver around 200mA, isn't shown.

when building the unit. This circuit board is available, along with a ready programmed eprom and plug-top power supply from the address at the end of this article. A copy of the PC software can be provided if a formatted blank disc (5.25in) is supplied too.

Firmware considerations

The protocol between the adaptor and the PC has been chosen so that is it compatible with proprietary terminal software for an earlier range of adaptors. These used a different processor and a gate array to implement external DMAing of data into memory. This software is available to run the adaptor from a PC with CGA, EGA and Hercules graphics adaptors or 100% emulation.

The teletext data is transferred from the MSCI, which is mapped into I/O space, into memory by the DMA controller within the NPU. This can occur on up to 16 TV lines per frame. The NPU creates a window, during which data can be received by counting TV lines after frame sync.

The presence of off-air syncs is indicated by a steady flashing of led *A17*; if this led is off then you should check your video feed to the adaptor. The MSCI is set up with the teletext framing code (27hex) as its sync byte, and the DMA controller set up for transfer of 42bytes, which it does on a cycle-stealing basis. This means that the processor is not halted during DMA transfer, only slowed down somewhat.

This data is stored on a row by row basis, then examined to see if any rows are required for transmission to the PC. The adaptor maintains several data buffers for this purpose; the main ones are six 'page' buffers and a global output buffer.

The page buffers are used to assemble incoming rows on a page basis until either a timeout (4s) occurs or the page is terminated properly. The timeout is to prevent endless waiting for a page to complete if the terminating row is absent - for example, due to noise.

The teletext transmissions consist of data on a row by row basis; each display row is transmitted in a single TV line of data. The rows are essentially similar, the exception being Row 0, known as the header row. This row has just 32 displayable characters instead of 40. The extra 8 bytes are used to convey information about the relevant page. The magazine (= page hundreds) and row addresses are heavily protected by Hamming codes; using this scheme allows single errors to be detected and corrected, and even errors to be detected and rejected. Odd numbers of bit errors correspond to such severe noise that the data is likely to be unreadable in any event.

The presence of noise, or indeed bad data for any reason (more usually 'ghosting' caused by aerial problems), is indicated by the illumination of led *A18*. This led is pulsed whenever a 'hamming error' is detected at the start of a data line.

Once filled, the buffers are loaded into the global output buffer to make room for more incoming pages. There is a special buffer area set aside for 'headers'. These are simply the top row (row zero) of teletext pages.

This adaptor behaves in the same way as teletext TVs, which 'roll' headers while any given page is awaited, in that it sends headers to the PC. In this way the time is kept updated in the top right corner of the screen.

Incoming data from the PC is handled under interrupts and commands are processed to amend the list of required pages in an orderly fashion. Each data transmission from the PC causes led *A19* to flash. ■

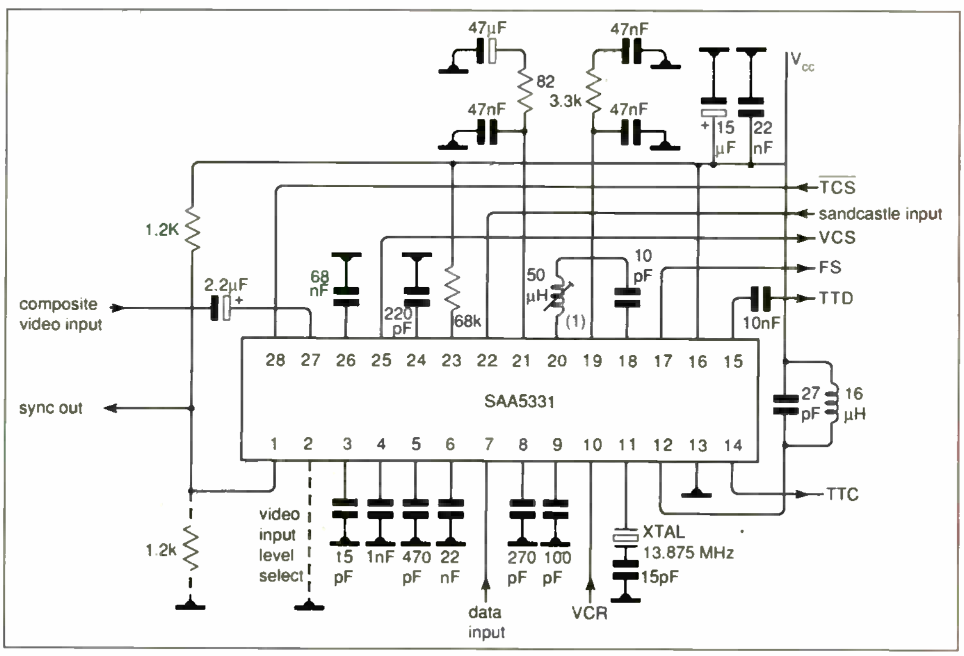
Laurence Cook is a design consultant with a number of patents relating to teletext decoding to his credit.

Fig.6. Synchronisation and Hamming codes at the start of the page header and row transmissions.

References

Figs.1, 2 3 and 6 are taken from the September 1976 Broadcast Teletext specification published jointly by the BBC , IBA and BREMA. ISBN 0 563 17261 4.

PCB, ROM, PSU and PC software from Citifax Ltd. 9 Goose Cote Hill Bolton BL7 9UQ Lancashire at £25 per set.Phone 0204 57293 Please enclose blank disc!



FOLLOW THE ASIC ROUTE

Whether to go, when to go and how to go: the three questions that the small size company needs to ask itself when thinking about going down the asic route.

by Julia King

For companies considering using an asic in their next design, there are two main approaches to take. One is to entrust the full design to a company that specialises in designing in silicon; the other is to use a PC-based design toolset that does not lock them in to a particular silicon foundry. However, the choice of vendor does need to be made at the gate level.

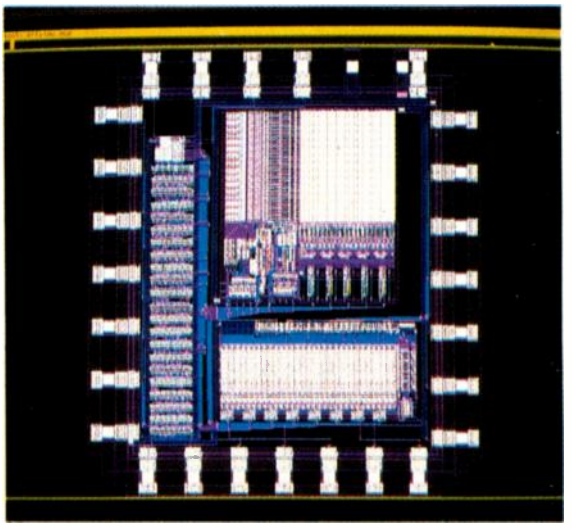
(Asic vendors fall into one of two camps: there are those that also act as a silicon foundry (such as ES2) and those that select their silicon vendor according to the design that is to be implemented (eg, MCE). Given the costs of setting up a silicon foundry (around $500,000, according to Chris Butler of Mogul Electronics' field applications group) it is easy to see why the number of 'silicon jobbing shops' exceeds that of asic vendors with foundries attached.

"Asics should be considered by any engineer starting a new design", says Alistair Dalrymple of Micro Circuit Engineering, "although not many companies would wish to commit to a standard cell approach". Standard cells, which typically require 13 or 14 mask levels to be fully implemented only start to be practical around the 20-25,000 gate level.

Below this number of gates, the gate array approach (which uses a master wafer with a matrix of pre-ordained logic devices, with customisation only completed during the final stages of production) should be considered. Although designs with as few as 20 gates can be economically viable, says Gareth Jones of European Silicon Structures (ES2), particularly for a part that is obsolete, MCE's experience is that it is unusual to follow the asic route with so few gates.

"Most people start from around 1000 gates", says Dalrymple. "We do a lot of pin-compatible replacements," he says, "but we don't do many at a few hundred gates." Industrial, military and aerospace designs that become obsolete are obvious candidates for going the gate array route, even though they may not use many gates. In the USA, the DoD has funded Hughes to found a department concerned solely with the production of obsolete parts.

Obviously the gate array approach is less efficient in terms of silicon usage than the standard cell approach.



ES2's 1400 design package is aimed specifically at the inexperienced asic user. The easy to use package offers him design integrity checking, sequencing, checks for correctness of manufacturing and documentation, provides test vectors, checks that the package selected is large enough for the end product, etc.

One approach

As a repping agent, Mogul Electronics offers customers a variety of strategic alliances with third party design houses such as MCE and Walmsley. It is currently expanding these relationships to include foundry agreements with companies such as Harris and Philips.

Customers can buy standard cell or analogue array design kits for £50. After schematic capture and simulation, MCE will carry out a post-layout design review before generating GDS II tapes which are shipped to the foundry.

The foundry carries out customisation of the wafer and parametric probe testing; MCE carries out die probing, packaging and testing. Mogul says that the service is viable down to 5,000 pieces per annum. It is likely to be enhanced shortly with a "fast turnround prototyping service with the option of multi-project wafers".

Primarily it represents a trade-off in terms of cost and of time. "A gate array is quicker to market", says Dalrymple. He quotes a typical time of three months development time for a gate array and six months for a standard cell - although complexity of the design obviously affects this.

Tim Ellis, marketing manager for northern Europe with ES2, believes that asics have shifted the whole focus of silicon over the last five years. Originally, asics were used to 'board crunch' – reducing whole PCBs to one asic, while silicon 'gurus' dealt with more complex systems design.

Now, board crunching is more the realm of FPGAs (field programmable gate arrays). Typically these are used for quantities of 5 - 10,000 parts with 2 - 3000 gates that the designer "can blow on his desk". Asics, on the other hand, are now used to do more complex systems design. NRE and piece part count tend to be the deciding factors on asic – particularly NRE.

"People need to be more original with their designs", says Ellis, to provide them with adequate market thrust. Asics can help them achieve this market differentiation.

There is a problem with smaller companies going down

Triangle's path

Triangle Digital Services manufactures a Eurocard-based control computer based on the Hitachi H8 microprocessor and using the high level language, FORTH.

Four or five years ago, the company was looking to reduce the size of its computer while keeping it low-powered enough for use in hand-held general purpose applications. Triangle opted to go down the asic route: "we couldn't have done it any other way", says Triangle's MD, Peter Rush.

The only other way that the problem could have been solved would have been to have used a multilayer board, which "would have pushed the price up", says Rush. "and there's great pressure on price".

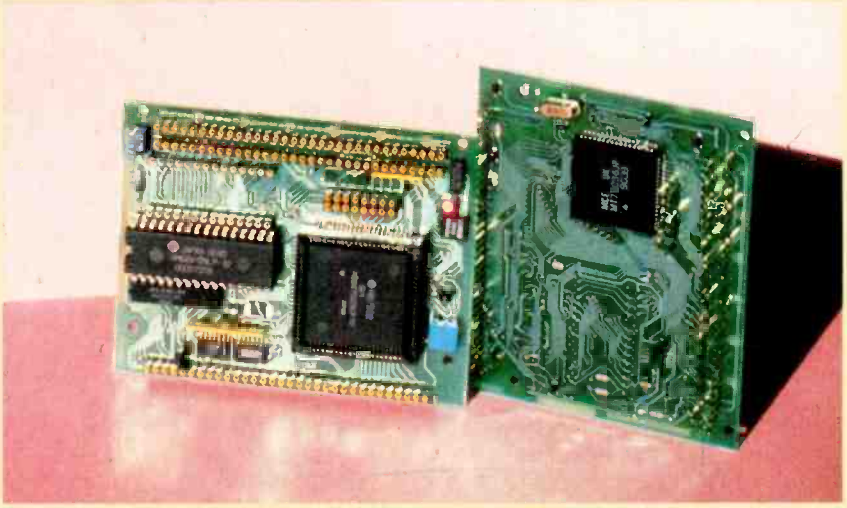
Going the asic route enabled Triangle to reduce the length of its TDS 2020 control computer from 160mm to 80mm while leaving it as a fairly simple two-sided board.

Rush points out that asics are difficult to test: "you have to simulate in software", he says. That includes parameters such as "timing analyses and tolerancing". However he says that the board worked first time having gone through all the simulation processes offered by Micro-Circuit Engineering. "My background was in custom silicon", he says, "but if you're prepared to put in enough time and effort, you can probably get it right first time".

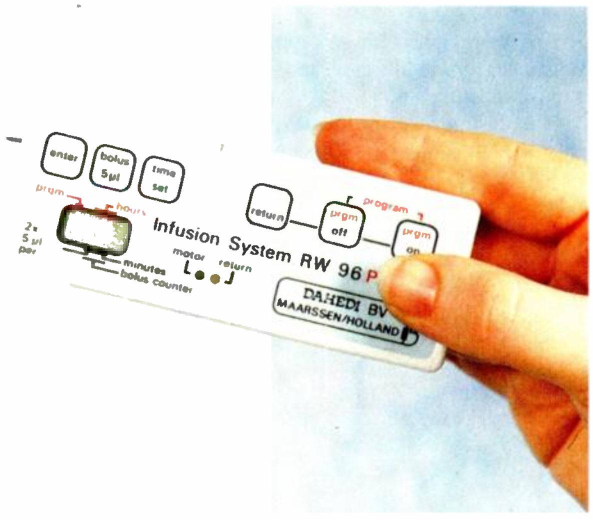
Rush warns against going the field programmable gate array route "it's very expensive except for small numbers", he says. He also points out that some designs might be better served by the use of masked microprocessors. "You can put inputs in and get outputs out, which is all that is required for some asics", he says "and relatively cheaply".

For Triangle, the ASCI route worked to perfection. As well as helping it to offer small size and low power, "we built some protection into the asic so that the board won't work without the asic features", says Rush. The asic also deals with address decoding for features such as the keyboard and an LCD and incorporates a watchdog timer, satisfying applications where users want a timer to be separate from the microprocessor.

The Triangle asic consists of around 2,000 gates and is implemented using a 5μm process.



The TDS2020 16-bit control computer from Triangle Digital Services shows the two sides of the board. The asic is housed on the board's underside.



ES2 worked with Dutch medical equipment manufacturer, Dahedi to develop a portable medical infuser capable of delivering a measured dose of a drug. An asic helped provide redundancy and added self-test features.

the asic route, however desirable it is, Ellis believes. "There is no true low cost route to silicon", he says, "but the payback can be quite vast."

First time users are asked to pay a lot of money up front to do prototyping, Ellis believes. Their natural reaction is to look around and select their vendor on the basis of price. The problem with this approach may be that going for the lowest price may mean that the small asic user is not supported adequately.

A better introduction to asics, Ellis believes, would be to offer companies a minimum-cost access route. These companies want vendors to participate in the risk with them: they're not venture capitalists, says Ellis.

Instead, they tend to find that the bigger vendors subject them to a minimum order in terms either of value or of quantity. "The problem is that the cost of supporting 1000 little customers is not economically viable", says Ellis.

Small users always want vendor independence, Ellis believes, because they believe, erroneously, that this will give them maximum flexibility. "Asics are not like standard products", he says. Asic means sole sourcing and requires design support.

Nevertheless, "process portability is a goal that everyone's been running after for years", he says. The risks are high, however: if the end product doesn't work, they will lose market share. "The best solution is to take the vendor's software", he says. That means that the vendor has to take responsibility for the end results.

PC platforms are adequate for doing schematic capture, says Ellis, but are not good enough for simulation. As Triangle's Peter Rush says, "the simulator is the most important tool in gate array design. Only 10% of the time is spent in drawing the pretty coloured pictures – ie, entering the circuit design – and 90% poring laboriously over yard after yard of simulator output".

In the final analysis, asics do not represent a cheap path to production but their use can pay handsome dividends. Where FPGAs offer inherent problems of large die size and architectural restriction, asics enable the designer to achieve what he sets out to achieve – without having to compromise too much along the way.

Unless users have significant analogue expertise, however, it is probably inadvisable to attempt complex linear circuit designs in asics. Mixed technologies are too complex for most small customers, Ellis believes, although "simple analogue is capable of being done". The moral is to keep analogue elements to a minimum. ■

Government incentive

The government is trying to encourage the use of asics with incentives such as that offered by the DTI's Link project. Essentially this acts as a 3-way agreement, says ES2's Jones, between the end user, a university and the silicon vendor. Funding of up to 50% is available if developments fulfil all the criteria set out by the DTI.

Tim Ellis of ES2 believes that 1992 will see the start of a European programme designed to encourage the use of silicon by smaller companies. Such programmes exist already in a number of European countries; the European single market will ensure that no project can be funded locally and that participation will be more widespread

The Eurochip project for universities, which provides funding at the level of around 20 ecus per square millimetre of design, has been highly successful in raising universities' awareness and use of asics, says Ellis. Eurochip was originally planned to last one year and was extended; it is now in its third year. The consensus on Eurochip is that "price should be no barrier", says Ellis. Industry would be well-served by the same type of approach.

Micro AMPS

ICE 751	An emulator/programmer for the Philips 24-pin skinny DIP 8051; the 87C751. The ICE751 provides the cheapest way to emulate and program these devices.
ICE51™	A low-cost emulator for the industry standard 8051. This product is also available in kit form.
PEB552	The official Philips 80C552 evaluation board for this highly integrated 8051 variant. Optional debug monitor and 87C552 programming adapter are available.
BASIC COMPILER	A PC-based cross-compiler that enables code written for the 8052AH-BASIC processor to be compiled for the standard 8051 or 8052. Interpreted Basic is also available on the ICE51.
8051 BOOK	8051 Architecture, Programming and Applications. A recommended book for readers who require a text on the 8051 and interfacing techniques. This book is supplied with a PC-based cross-assembler and simulator for personal or educational use only.
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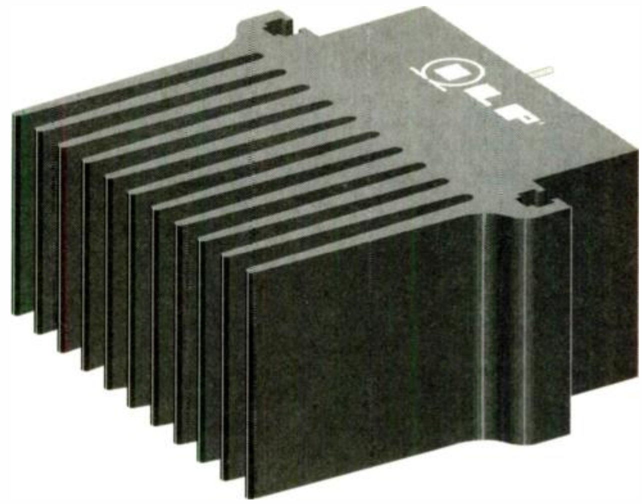

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REGULARS

LETTERS

Common basic reply

Replying to the queries raised by Frank Smith's letter (*EW + WW*, November, 1991), an explanation of the origin of any set of bipolar junction transistor (BJT) DC characteristics presents few difficulties if we resort to an appropriate device model, for example Ebers-Moll or Gummel-Poon. However, such a model is inappropriate at a basic electronics level.

The following approach (which does not appear in any text book) is suggested. **Figure A** shows a convenient practical test set-up.

Figure B shows a common-base (CB) characteristic for one value of I_E and the associated base electron density profiles for a uniformly-doped base npn BJT in which base-region recombination is neglected. These make clear the minimum physical-electronics background and first-order approximations required for an intelligent qualitative appreciation of device operation.

In Region 1 (active), at a quiescent point such as Q_1, the condition $V_{CB} = V_{CB1}>0$ causes $n(w)<n_o$. All electrons diffusing across the base to the collector are extracted at the collector-base junction. There is no bottleneck. The magnitude of the diffusive current flow is proportional to the carrier density gradient and electrons flow down the gradient. I_{E1}, fixed externally, controls I_{C1} and $n(o)>0$ corresponding to $V_{BE}>0$.

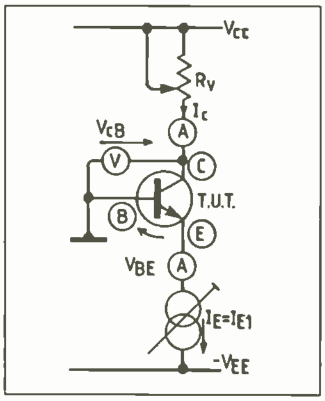
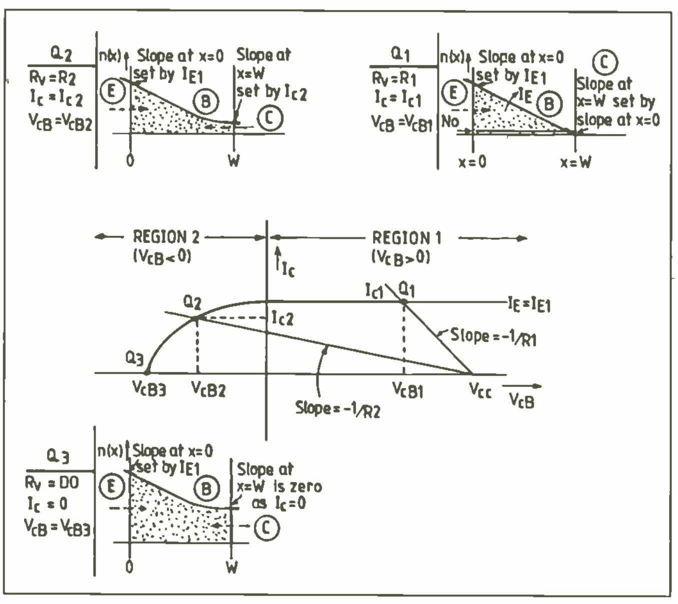


Fig. A. Common-base characteristics test set-up for NPN BJT. R_v can be a resistance box. For a fixed I_E, vary R_v, measure pairs of values I_C, V_{CB} and plot curve in Fig. B. For $I_C<0$ reverse the polarity of V_{CC}.

Fig. B. Common-base characteristics and associated base charge patterns for a uniformly-doped base npn BJT. n(x)=base electron density; nx(w)=nC for $V_{BE}=0$, $V_{CB}=0$. Dots show electron charge in blue region, extending from x=0 to x=w. Horizontal dashed lines, with arrow heads, show electron injection at a junction



In Region 2 (saturation) at quiescent point Q_2, all the carriers injected into the base at the emitter cannot be extracted at the collector. This is because I_{C2} is effectively circuit-determined; thus $I_{C2}=V_{CC}/R_2$. Balance is only restored at the collector-base junction by carriers being injected back from the collector into the base. This necessitates a forward bias: n(w)>n$_o$ corresponding to $V_{CB}<0$.

Note that the CB junction is acting simultaneously as a carrier injector and extractor. This accounts for the ability of the junction to pass significant current the wrong way when forward biased. With respect to the base resistance, r_x (typically 100Ω), this is something of a red herring in the explanation of CB curves.

r_x is a parasitic element, not necessary for essential BJT operation, and arguably best ignored in a basic study. Its effect can be assessed by a simple theoretical argument and practical test.

If I_{E1}=0.1mA, then the PD across r_x is only some 10mV for I_c=0. This is negligible compared with the PD across a forward-biased PN junction.

Delayed credit

Reading once again Arthur Clarke's remarkable 1945 prediction of satellite communications (Extra-terrestrial relays, reprinted *EW + WW*, November) I came across the statement: "We have as yet no direct evidence of radio waves passing between the surface of the earth and outer space", and later: "Given sufficient transmitting power, we might obtain the necessary evidence by exploring for echoes from the moon".

But I recall that shortly afterwards, I think it was the Spring of 1946, the American magazine *Electronics* carried an article detailing how they had adapted a high power dish radar to do just that.

A year or so ago I bought David Pritchard's fascinating book "The Radar War", subtitled "Germany's Pioneering Achievement 1904-45". On page 118 he describes a Telefunken radar known as the Wurzmann, which was "erected on the island of Rugen in the Baltic, and during tests, ranges of 200km against aircraft were easily achieved. Air battles over Berlin could also be easily observed. But these distances pale into insignificance when compared to the 385,000km distance to the moon which the system covered easily. By switching off the power to the transmitter the echo returned two and a half seconds later, and this 'party trick' was often demonstrated to astonished visitors". This, one gathers, was as early as 1941-42.

The book comes as something of a revelation to people like myself who had always regarded "radio location" as a British idea of the 30s. Here we learn that a German demonstrated centimetric radar at sea in 1904; it was used by Germany in the First World War; Yagi type aerials were developed decades before Yagi "invented" them; their wartime long range Wassermann M4 could observe Allied aircraft taking off well beyond the Midlands; over-the-horizon radar was locating convoys at ranges of 2000 to 4000km by August 1944... Post war attempts to get some of this work recognised, including letters to Winston Churchill, fell on stony ground – even the book seems to have received surprisingly little recognition.

Geoffrey Horn
Oxford

For a practical demonstration simulate the effect of r_s by inserting a 100Ω resistor in the base lead of the TUT, in the circuit of Fig A, and compare the resulting characteristics with the 100Ω in-circuit and then shorted-out.

Finally, Mr Smith's Fig 2 shows the correct general relationship for a set of characteristics. Fig 3 is incorrect: the curves do not coalesce.

The reason for this may be appreciated by referring to my Fig B. There is a separate point Q_3 for each I_E because n(w) changes with I_E and is related to $|V_{CB}|$.

Bryan Hart
Essex

Magnetometer on line

Constructors building the magnetometer (Fluxgate magnetometry, *EW + WW*, September) should not rush to recalibrate their instruments as a consequence of the letter from Terry Arnold and George Pickworth (December).

The Helmholtz equation is fairly easy to derive from first principles using the Biot-Savart law. The first step is to find the flux density at a distance x along the axis of a single coil of *N* turns. Integration around the coil circle of radius *r* will readily yield, for a current, the formula:

$$B = \frac{\mu_0 NIr^2}{2\left(r^2 + x^2\right)^{3/2}}$$

where $\mu_0 = 4 \times 10^{-7}$, the permeability of a vacuum.

The field at the centre of two such coils at separation *r* is simply the sum of two identical contributions from this formula for $x = r/2$, one from each of the N-turn coils.

This makes the Helmholtz equation:

$B = (4/5)^{3/2}\mu_0 NI/r$ or $B = 0.716\mu_0 NI/r$

It is clear, however, that *N* is still the number of turns in each coil and not the total number of turns.

The approximate value of the earth's field which I quoted as 47,000 gamma is the magnitude of the total vector, which is inclined at around 67° to the horizontal in the UK.

The field affecting a compass needle is only the horizontal component of this which differs by a multiplying factor of cos(67°), giving a value of around 18,400gamma. Using the coil constant quoted in the original article requires 125mA for 50,000gamma or 46mA for 18,400gamma.

The apparent "times two" error does not really exist but there now seems to be a discrepancy of some 30% in the current required to balance the earth's field and the error is in the opposite direction to that suggested. I would consider this to be much too large an error to result from such simple and straightforward equipment and it warrants further investigation. (Perhaps my figure of 47,000gamma which I confess is based on ten year old information is now wildly out.)

The reference to core permeability affecting calibration seems irrelevant since, in the experiment being conducted, there is no permeable core in the coil system to influence the Helmholtz equation.

I am also unable to understand the reference to a misplaced decimal point and the correction of the coil factor to 0.395gauss/ampere since I calculate

9.1/1000 x 24/0.055

to be definitely greater than one. In passing I should say that I am a great enthusiast for simple equipment and agree wholeheartedly that the instrument constructed would make an excellent educational project, with the added benefit of being low cost, with hands-on experience and the satisfaction of personally building something.

Richard Noble
Gwent

If only

We (engineers) have done it again. I read, sit back and wonder in amazement how so much can be missed by so many in such a short space of time. I am referring to the recent crop of letters on software quality and the confusion over IF...ENDIF, IF-THEN-ELSE and IF...GOTO etc.

I would like to suggest that we are missing the obvious. It is not the if statement that causes problems, rather the IF ONLY statement; if only the requirements specification were more detailed, if only the functional specification was realistic, if only users did not keep changing their minds – if only things were different!

A recent survey published in *Computer Weekly* indicated that 99% of software failed. In an earlier survey (USAF GAD 1979 FGMSD) it was stated that 2% of software was usable as delivered, and a massive 47% was delivered but never used.

All of which indicates something is very wrong. But when talking of software quality, are we not in danger of not seeing the wood for the trees?

I am not suggesting that we should ignore software quality issues, far from it; they are very important. However, I would like to change our perspective. For every one line of text concerning software quality should we not have ten lines considering the broader issues, specification issues and the methods of generating those specifications?

This is not a subject that has gone unnoticed and there are several papers and other documents that address the point. It has even been taken up by the DTI under the banner of their "Usability Now" programme, (a copy of a particularly relevant case study is available from HCS Limited, Tel: 0442 210191) and by the IEE (Colloquium on Human and Organisation aspects, January 12, 1990) amongst others and has, of course, been mentioned in *EW + WW* (July 1990 p.602).

I feel that if a broader view is taken great strides in the quality area can be made and great benefits achieved at both a personal level as well as a commercial level. If only we (engineers) would not concentrate on the detail, IF ONLY ...!

Andrew Ainger
Herts

Synchrotron star

Every schoolboy knows that a neutron star is so called because it is like a soup of neutrons held up only by a degenerating pressure, due to the law which forbids any two particles to occupy exactly the same state.

The matter in the star actually consists of an equal number of protons and electrons. Because of the sharing of energy levels the electrons are highly mobile and the star is highly conductive.

Currents in the star collect and maintain the magnetic field of the original star of which the neutron star is the remnant. The field is concentrated to such an intensity that charged particles falling towards the star spiral fast enough to generate radiation (synchrotron radiation) directly.

Nicholas Taylor
Berks

Scattering arguments

The Doppler effect can be seen as a special case of Compton scattering. Let $c = \lambda f$ be the velocity of the outward pulse of light toward a reflective target where *f* is proportional to the signal's energy content with respect to an inertial frame.

Now consider the return pulse of light from the target, where the target is stationary in the same inertial frame:

$$c_i = \lambda_i f_i = c = \lambda f$$

Because the target is stationary, no change occurs and the wavelength of the return pulse equals the wavelength of the outward pulse. However, if the target now moves with velocity *v* toward the source of the pulse and assuming ideal reflectivity of the target material so that no dissipation of the wave's energy occurs, then the wave will absorb an amount of energy *E*, from the electrons in the moving target, proportional to:

$$h\Delta f = mv^2/2$$

where h is Plank's constant and *v* the velocity of the target electrons.

According to SR the relative velocity *v* of the bound electrons on the target's surface must approach relativistic velocities before a detectable change in the wavelength occurs.

Doppler effect might be explained as a special case of Compton scattering via interaction of the surface electrons of the reflective medium. Compton scattering differs from Doppler in that the scattered photons must interact a second time with the detector to register the change in hf; in Doppler the interaction occurs only once from the emission, at the source, to the interaction point where the change is registered and dependent on the relative velocity v between the source and detector. From this it can be seen how the Doppler effect appertains to the classical wave interpretation of electromagnetic interactions and the Compton effect clearly belongs to the quantum-mechanical interpretation.

Photons have a momentum expressed in quantum mechanical or wave-mechanical terms only by virtue of their lack of rest mass and their constant velocity $v = c$. Although fermions, ie electrons, protons, neutrons and their anti-particles can have a momentum expressable in terms of a wave function, this occurs only at relativistic energies or velocities and can also have a kinetic energy of momentum by virtue of their inertia or intrinsic rest mass.

Bosons always conserve $v = c$ while fermions require energy, and never attain c. Furthermore, in their interaction with matter, photons acquire or relinquish energy of frequency or wavelength while, in contrast, fermions have a kinetic energy of mass which is interchangeable with their quantum energy of wavelength:

$E_0 = mc^2 = m(\lambda f)^2$

Frank La Tella
Australia

8 bitter

I'm sorry to say that Mr Balasubramanian's neat idea of simply extending the resolution of 8-bit convertors by analogue subtraction of partial conversions will not work with off-the-shelf parts (*EW + WW* Circuit Ideas, December). If it did we could all do fast 16-bit A-to-D conversions with cheapo 8-bit A-to-Ds like the Texas *TLC549* and save a lot of money compared to expensive "real" 16-bitters like Crystal Semi's excellent products .

The idea is the basis of the half-flash convertors sold by many manufacturers, but it does require that the remainder from the first conversion process is as accurate as the whole final accuracy required. A manufacturer making conventional convertors will only guarantee his accuracy to 1/2 or 1/4 least significant bit (around 10-bit accuracy at best for an 8-bit convertor). Hence even with a "perfect" convertor turning this back to analogue the 2nd A-to-D has an extremely inaccurate value to convert when it is subtracted from the input and amplified up – the 8 bits from this stage would be near meaningless.

Pity – it would be nice if it worked.

Allan Hurst
Cambs

Ether drift

It was encouraging to see from Paul Dunnet's letter (*EW + WW*, December) that, despite establishment hostility, the ether has not yet ceased to drift. There are two points that could be of interest in this connection. Firstly the reported values of drift velocity appear to increase linearly with time: in 1887 Michelson and Morley[1] showed a value of about 10^3m/s, Dayton Miller[2] refined their experiment in 1933 getting a value of 2 x 10^5m/s while Silvertooth[3] in 1986 reported 4 x 10^5m/s, the three values apparently showing a steady increase of about 4000 m/s each year.

Secondly, the velocity of light is increased by an amount $v.(1-1/\mu^2)$ when the medium in which it is travelling is given a velocity v; μ being the refractive index.

This increase, which was demonstrated separately by Fizeau, Michelson, Fresnel and Airy, and subsequently by countless students, seems difficult to explain without invoking a medium having some of the properties of an "ether".

HC Wright
Northants

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2. Miller, DC *Rev. Mod. Phys*. 5, 203 1933.
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Dual quantities

Wave-particle duality has been with us for a long time now. It is well established that emission and absorption of electromagnetic energy are quantised, but I have not seen any evidence showing that e-m propagation is a process that preserves the identity of individual energy packets between emission and absorption. That it is also supposed to be a wave surely suggests the opposite. Suppose atoms absorb quanta from the e-m field they find themselves in whenever it becomes strong enough and has the right frequency, direction, polarisation and phase, in relation to the momentary states of the orbiting electrons. Suppose also there is always e-m wave energy, or "noise" chaotically buzzing about everywhere. Where the level of this noise is too high atoms will apparently randomly absorb quanta until a residual e-m wave level is reached. Below the residual level absorptions will not occur, or at least will become extremely infrequent, so the background "noise" level settles to just below absorption threshold.

Every quantum emitted will add to the background wave energy, so later the energy density at a receiver somewhere is more likely to be momentarily high enough for absorption to be triggered. It could then be said that a "photon" was passed, but the transfer happened by waves, and the energy packet absorbed was not exactly the same as the one emitted. Emission added to the residual wave energy and the absorption restored it back to its previous level, but the photon had no identity of its own during transmission.

The wave-like behaviour of individual photons demonstrated in interference experiments is then explained. Where waves, however small in energy, reinforce each other on top of the background noise, absorption of a quantum is more likely to happen. Where they cancel, there is only background noise present, so absorption is unlikely. The chaos of the system, however, makes events more or less likely, not certain, which is why wave-like probability distributions are shown by discrete events.

My conjecture is that emission and absorption of e-m energy are quantised, but the quanta themselves do not have an identity which is preserved during transmission. The quagmire (or whatever they call it) of "virtual" photons postulated by quantum mechanics is really just this background noise. The probability distributions of apparently "random" absorption of quanta do not result because God plays dice with the universe, but because the whole thing is so chaotic. The whole problem of wave-particle duality is not so much solved, as ceases to exist, because light is not a particle.

The background noise exists at all frequencies. Like most noise it can produce occasional peaks far higher than the normal level. At the higher energies it can, on very rare occasions, even produce "random" peaks of energy big enough and in just the right time, place, frequency, polarisation etc to trigger the disintegration of large, marginally stable nuclei.

If this conjecture is wrong, I expect there will be a bag full of responses, some involving all sorts of mathematics I won't understand, but all explaining why it is wrong. If on the other hand the conjecture is right, I expect exactly the same kind of thing, except in much greater quantity.

Alan Robinson
York

Mind games

Putting words on paper, without many references to objects (in contrast to the sciences) has often been a hazardous or sometimes trivial procedure.

With reference to such words as universe, time and space I would suggest, for example, that we could quite reasonably say that: at the beginning of space and time, there was present in the universe everything necessary to produce the universe as it has evolved and as we know it today. We could conveniently give logical priority to calling this the "imagination" which we have subsequently found to consist of atoms: protons, electrons, neutrons and other pieces still to be identified.

In perception then, for example, the eye is used simply as a controlling seeing lens in conjunction with the rods and cones of the retina and neurons in the brain so that we may respond and control, aurally, tactually, and kinaesthetically, to the objects seen in the imagination outside us. This is in contrast to the camera, where the lens is only used to focus pictures on to photographic film. The apparent mystery about the process of seeing, therefore, has been due to a logical misuse of the concepts of mind and imagination, wrongly supposing that they refer to a kind of theatre or cinema inside the brain, where pictures of objects outside us are reproduced. It is my contention that it would be putting the cart before the horse if we say that the imagination is a part of the brain; fundamentally, the brain is a part of the imagination.

Peter GM Dawe
Botley

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SC110A miniature portable oscilloscope

SC110A miniature portable oscilloscope

The SC110A from Thurlby-Thandar is a full feature, single trace analogue oscilloscope packaged into the size of a benchtop multimeter. Fitted with a 32mm x 26mm screen miniature CRT, the bright, sharp image provides resolution and detail associated with much larger instruments. UK designed and built, the internal switch mode power supply draws just 195mA from four C sized batteries (not supplied). The instrument will operate from 4 to 10V DC.

The specification includes a Y bandwidth of DC to 10MHz, 10mV/div sensitivity and an adjustable brightline trigger with AC/DC/TV coupling from both internal and external sources. The X timebase is adjustable from 500ms/div to 100ns/div in 24 steps. The case measures 25 x 5 x 15cm and the instrument weighs about 1kg. SC110A £249+VAT (£292.58).

1021 general purpose oscilloscope from Leader Electronics

1021 general purpose 20MHz oscilloscope

The Model 1021 general purpose oscilloscope from Japanese instrument maker Leader Electronics more than meets its published specification and is of exceptional build quality. Features include 20MHz dual channel operation, 8cm x 10cm display area, 5mV/div Y1/Y2 sensitivity at 20MHz, DC to 500kHz X-amplifier response, variable trigger response, multiple sync conditioning and an overall accuracy better than 3%. 1021 £299+VAT (£351.33)

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PL320K laboratory triple power supply

TS3022S laboratory dual power supply

PL320K laboratory triple power supply

This power supply from Thurlby-Thandar combines three, totally independent power supplies within a single unit: 0–30V at 2A, 0–30V at 1A and 4–6V at 7A for logic supply. The 30V supplies will operate in a bipolar tracking mode for ±30V operation or in a series mode to provide 0 to 60V output. Both supplies incorporate independent remote sensing and independent precision voltage/over-voltage/current-limit preset. Three 3 3/4 digit led panel meters indicate current and voltage to an accuracy of 0.05% fsd. Output stability is typically 0.01% for 90% load change. PL320K £359+VAT (£421.83).

TD201 digital storage adaptor

The TD201 digital storage adaptor from Thurlby-Thandar is a low power, single channel digital storage unit which adds digital storage capability to ordinary analogue oscilloscopes. The maximum sampling rate of 200kHz permits fast transients to be captured while the lowest rate can extend the sampling period to over an hour. The unit stores over a thousand points on the X axis with 256 levels in the Y axis. The internal batteries (not supplied) allow data retention for up to four years.Other features include an AC/DC sensitivity down to 5mV, selectable pre-trigger, roll and refresh modes and a plot mode. The case measures 25 x 5 x 15cm and the unit weighs about 1kg. The TD201 provides the ideal solution for those wanting a well specified and easy-to-use DSO at the lowest possible cost. TD201 £195+VAT (£229.13)

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TS3022S laboratory dual power supply

This laboratory quality power supply from Thurlby-Thandar provides two fully floating 0–30V 2A outputs for parallel, series or independent operation. Each supply has its own metering of voltage and current by LCD display; with the output switch to off, the display can be used to preset the voltage and current limits prior to connection of the load. Coarse and fine controls permit output voltage adjustment to within 5mV of a predetermined value. The current limit control employs a log law for precise adjustment down to 1mA. Load regulation is typically within 0.01%. Both supplies incorporate remote sensing. TS3022S £299+VAT (£351.33).

TD201 digital storage adaptor

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Circuits, Systems & Standards

First published in the US magazine EDN and edited here by Ian Hickman.

Voltage divider switch adds range to DPM

Accuracy maintained

Here is another brilliantly simple idea. It lets you use solid state switches to select ranges on a DPM, without incurring inaccuracies due to switch resistance on the more extreme division ratios.
IH

The range of many currently available digital panel meter (DPM) chips and modules can be extended by adding a voltage divider switch to the DPM's input (**Fig. 1**). If mechanical switches are used, the contacts' resistance won't affect the divider's ratio. However, if solid-state switches are used, the switch resistance needs to be included in the voltage-divider equations. Unfortunately, an analogue switch's exact resistance varies with temperature and power-supply voltage.

Fig. 1's circuit overcomes this problem by using the differential inputs of the DPM to remove the analogue switch's IR drop which is in series with the divider resistor.

The second analogue switch in each pair carries no current. This switch connects the INPUT LO pin to the bottom of the precision voltage divider resistor, and causes the divider to ignore the voltage drop in the companion, current-carrying switch.

The analogue switch, in this case the *DG509A* analogue multiplexer, must be supplied with both a positive and negative voltage if it is to pass positive- and negative-going voltages. Fig. 1 generates the negative voltage using the *Max138*'s internal charge-pump; the V⁻ pin can supply as much as 0.5mA. You can build the precision divider with discrete 1% resistors, or purchase a precision resistor network. As Fig. 1 shows, the voltage-divider switch can be controlled by using a microprocessor and the select pins of the multiplexer.

***Don Sherman**, Maxim, Sunnyvale, CA.*

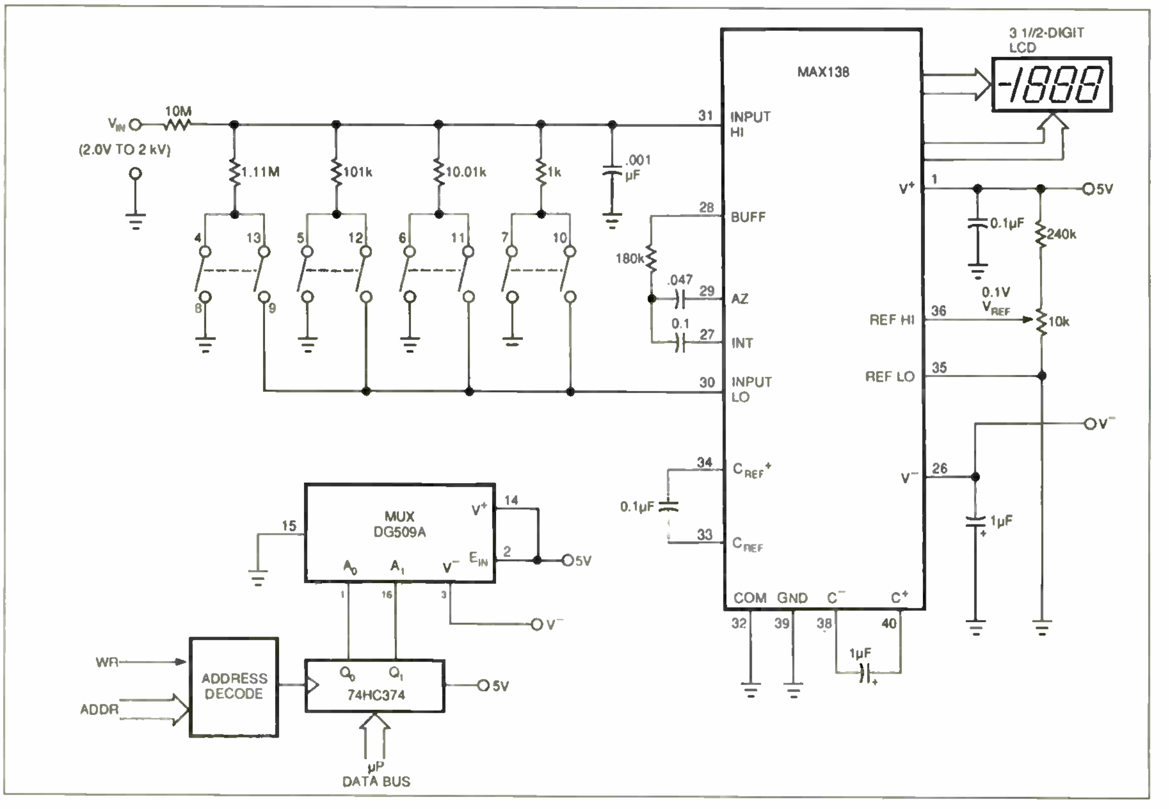


Fig. 1. To extend the range of a digital panel meter chip or module, you can add a precision voltage divider to the device's input.

Amplitude-locked loop speeds filter test

> ## ALL tests filter cut-off frequency
>
> Before reading this article, I had never heard of an ALL - an amplitude logic loop – and I guess that goes for a lot of other people. Here it is used as the basis of a useful item of production test equipment, enabling a completely unskilled worker to check filter cut-off frequencies.
> **IH**

The circuit shown in **Fig. 1** finds, locks to, and displays the cut-off frequency of an audio-frequency low-pass filter. The circuit compares the RMS input to the filter under test with the filter's RMS output. Based on the results of this comparison, the circuit adjusts a VCO to achieve a null at the desired input-to-output attenuation of the filter. Hence, its operation is similar to that of a phase-locked loop.

The *AD536* RMS-to-DC converter connected to the filter input acts as a reference to the *LT1013* servo amplifier. You set the null-voltage potentiometer to the desired input-signal attenuation, such as -3dB. The servo loop adjusts the VCO's frequency until the output of the filter's RMS-DC converter equals the null voltage.

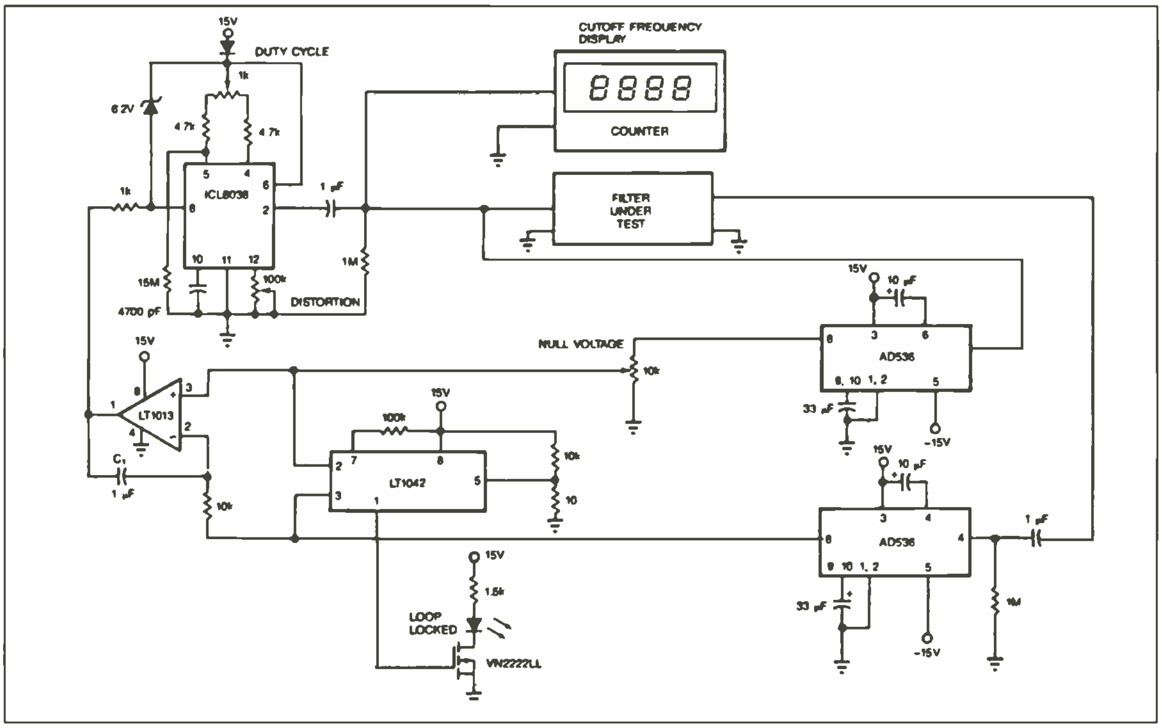
The *ICL8038* waveform generator is connected as a sine-waveoscillator with a wide-sweep input-range of 1000 to 1.

The values given in Fig. 1 provide a sweep range of 2Hz to 20kHz. The *LT1042* window comparator senses when the null voltage and the filter output voltage are within ±15mV of each other and causes the loop-locked led to turn on. When the loop reaches lock, the filter's cut-off frequency can be read from the frequency counter.

The loop's bandwidth is 16Hz, and it has 50° of phase margin. The circuit acquires lock in less than 1s with frequency repeatability of better than 0.1%. You can increase the loop bandwidth – at the expense of accuracy– by reducing the value of the integration capacitor, C_1, and the values of the averaging capacitors around the RMS-DC converters.

***Steven C Hageman**, Calex Manufacturing Co Inc, Pleasant Hill, CA*

Fig. 1. This amplitude-locked-loop circuit can be used to find the cut-off frequency of a low-pass filter.



Transistor clipper provides flat-top output

Using the diode clipper shown in **Fig. 1a** to clip a sine wave will not give a perfect flat-topped waveform because of the diode's forward characteristic. A simple transistor circuit (**Fig .1b**) does a much better job because the transistor's base gets its signals from the circuit input and output.

The transistor circuit's operation can be understood by looking at the effect of each base signal separately. **Figure 2a** shows the circuit with the base signal coming only from the output – a configuration that provides the same result as Fig la's diode clipper.

On the other hand, **Fig. 2b** shows the circuit with the base signal coming only from the input. With this configuration, the output actually sags, because as the transistor's base gets driven harder as a result of the input pulse's rounded top, the collector saturates harder.

Combination of the two base signals thus provides the flat-top characteristic. For different transistor types, the optimum resistor values might vary.

Add one component – another transistor – to Fig. lb's circuit, and you have a symmetrical clipper, shown in **Fig. 3a** along with its diode counterpart. Add another resistor, and you can raise the clipping-voltage level (**Fig. 3b**). This latter circuit functions at levels into the tens of volts. However, at higher voltage levels, it's more efficient to use zener diodes.

A waveform modifier

Here is an ingenious circuit in search of an application – can you think of one? I have used a version intermediate between Fig. l(b) and Fig. 2(b) in experiments with electronic organs. This provided alternative outputs, containing even harmonics, to the primary outputs of sine-wave type tone-generators, on a per note basis, in a free phase organ.

IH

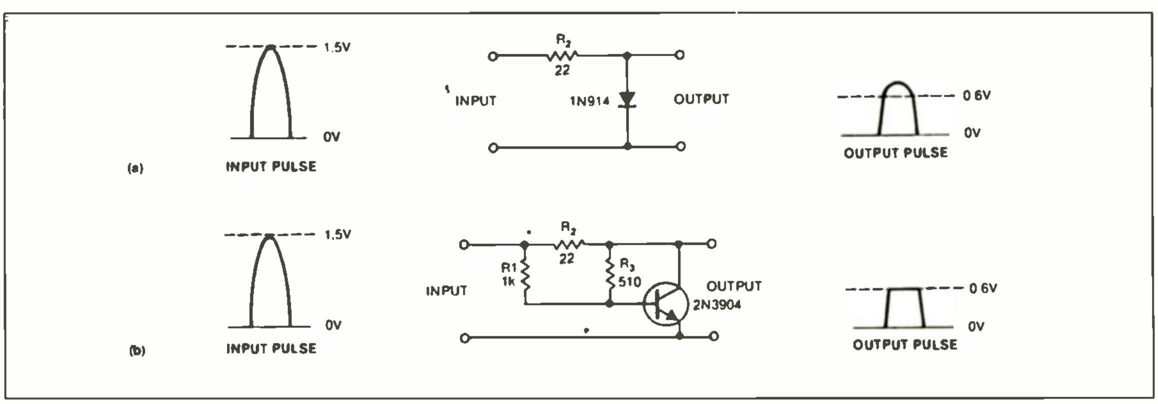


Fig. 1. A simple diode clipper (a) provides a signal with a rounded top when driven by a sine wave. Substituting a transistor whose base accepts two input signals (b) results in a flat-top characteristic.

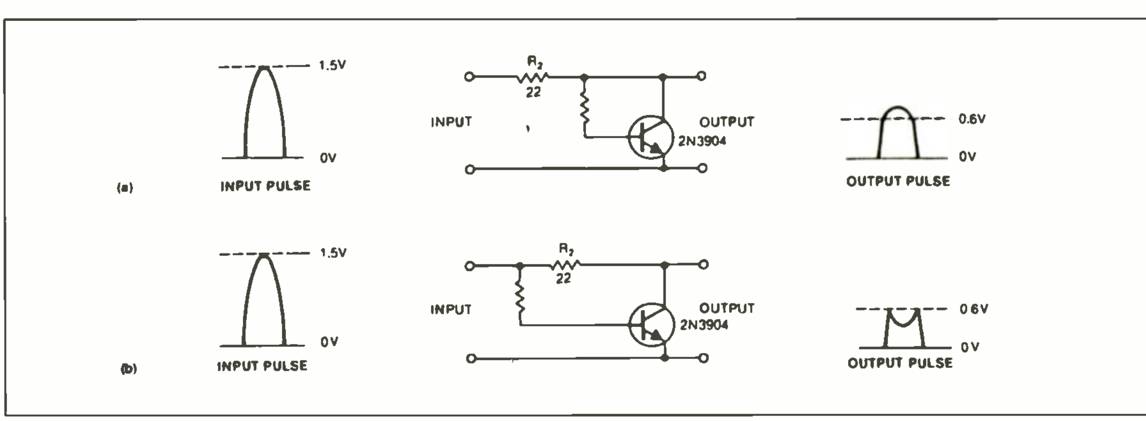


Fig. 2. Without the resistor from the input to the transistor base (a), action of the Fig. 1b circuit is the same as that of Fig.1a's diode clipper. And with the resistor from the output to the base removed (b), a sag appears in the pulse's centre because the transistor is driven there.

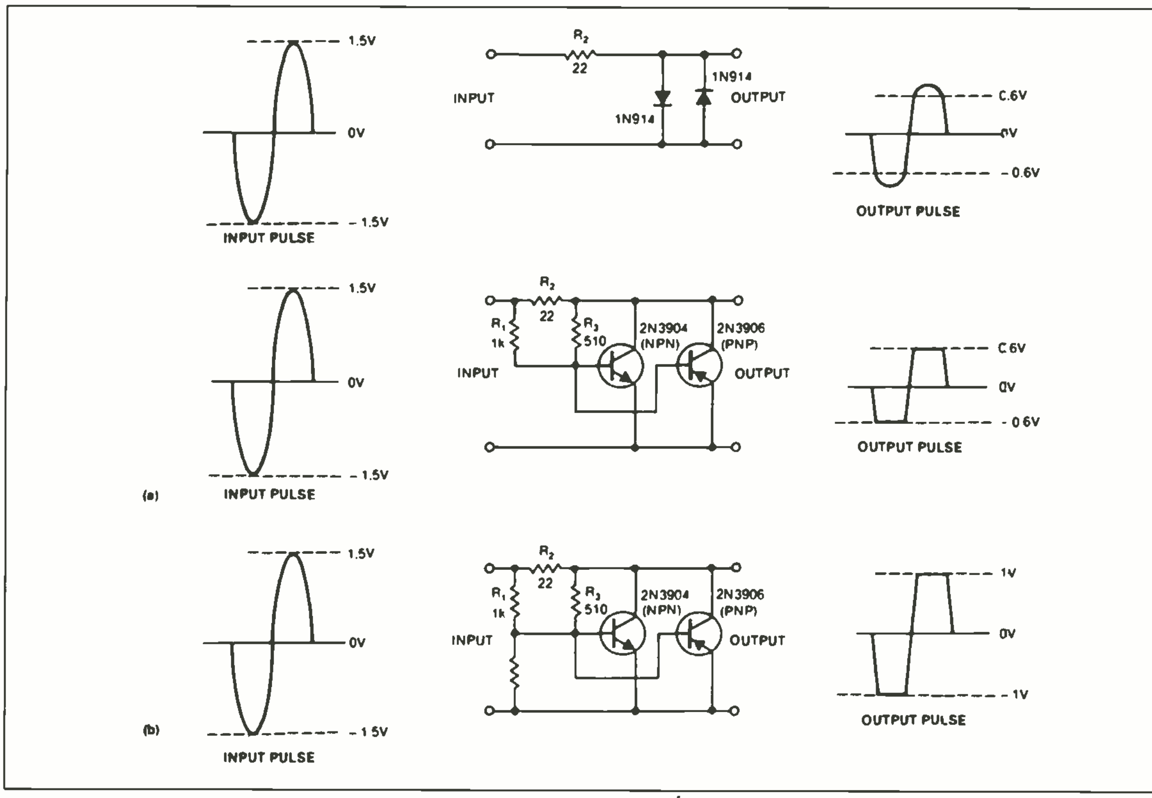


Fig. 3. Symmetrical action results when a complementary transistor is added to Fig. 1b's design (a). Adding a resistor (b) raises the complementary circuit's clipping level.

Hard decision by fuzzy computing

Neural Desk from Neural Computer Sciences makes accessing neural network technology less daunting. Stephen Franks looks at the technology

One of the drawbacks with neural networks has been the difficulty of applying them to real problems. There are many situations that might conveniently be addressed through a neural network, but the effort of creating a program has been too high. Neural Desk is designed to provide simple access to neural network technology. With it, you can create a suitable network, train it to solve your problem, and, if desired, provide a packaged solution that needs no special understanding on the part of the user.

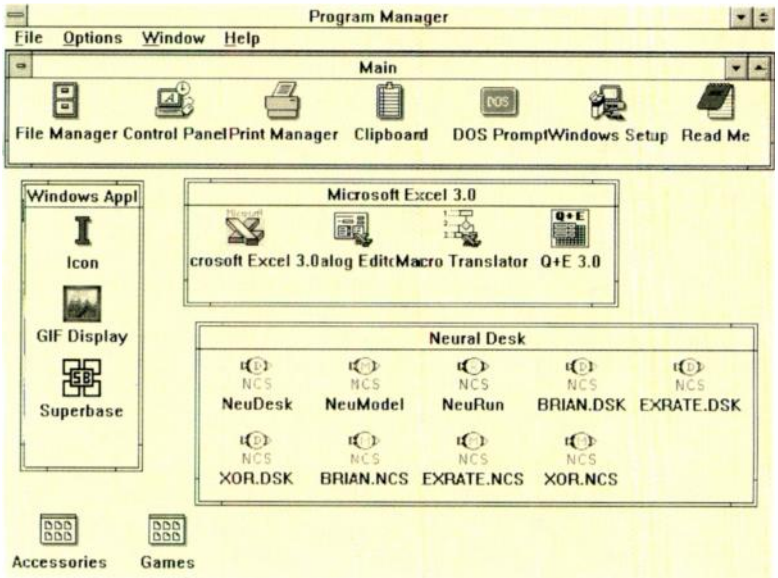
A good example of the sort of problem suited to neural networks lies in duplicating the skill of a mortgage loan assessor. By providing the results of a number of decisions already made, together with all the factors considered (eg income, age, amount requested, etc.) the network can learn to make similar decisions on future applications based on the history and outcome of previous ones.

The crucial point is that you do not need to know the exact connection between the input factors and the final result: the network creates a suitable algorithm during the training sessions. In fact, the algorithm the network develops is not readily accessible, and would be very difficult to discover.

Neural Desk can output the results of the training (the "weights"), but interpreting them for anything but trivial cases is very difficult. This is, of course, inherent in the way that neural networks operate, and does not detract from their usefulness in many applications.

The Neural Desk software is intended to bring the benefits of neural networks to the normal computer user (if such a creature exists!). The manual assumes no previous experience of neural networks, and all terms are explained as they occur. The software requires Microsoft Windows and is very easy to use. It would make a good learning tool in its own right, although is perhaps a little expensive for this purpose.

While Neural Desk can be used in isolation, one of its most useful features is the ability to link to other Windows applications using DDE (Dynamic Data Exchange). This is Windows' mechanism to allow completely separate applications to share data, and is used to good effect by Neural Desk.



Using a Super-VGA card in 1024x768 mode makes the system easier to use, but make sure that your screen is up to it: the 14in screen I used was too small for lengthy sessions.

The user never needs to be aware that Neural Desk is being used if he so wants: all that is seen is the familiar Excel spreadsheet or Superbase database, with the network filling in some of the blank spaces as if by magic.

All this can be done without writing a single line of code, although setting up a DDE link comes very close to the definition. It also does not require a deep knowledge of neural network theory: the ability to experiment is a very useful substitute. However, a powerful PC is

System Requirements
Absolute minimum hardware requirements are:
MS-dos or PC-dos 3.1 or later
Microsoft Windows 3.0 or later running in standard or enhanced mode
286 processor
1Mbyte ram
1.5Mbytes free hard disk space
One high density floppy drive (1.2 or 1.44Mbytes)
Windows-compatible graphics display
Windows-compatible mouse
Despite this, I would not like to use the software on anything less than a full 386 (not SX) with a Super-VGA display (**Fig. 7**), 4Mbytes ram and a co-processor. NCS also have dedicated accelerator cards for the really serious user.

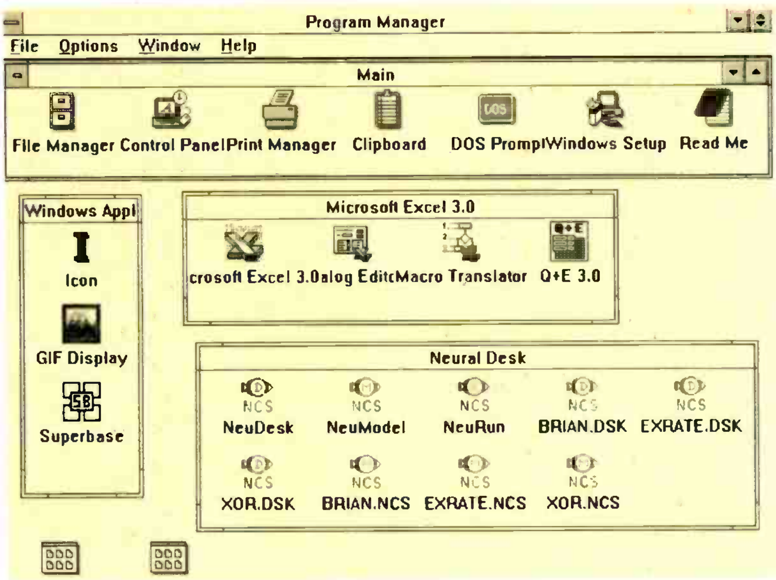


Fig. 1. On installation, a Neural Desk group is created and some of the examples are given icons of their own.

Fig. 2. The XOR example shows training inputs, target outputs and the automatically-generated network.

required, and a similar degree of intelligence is expected from the person in front of it.

Installation

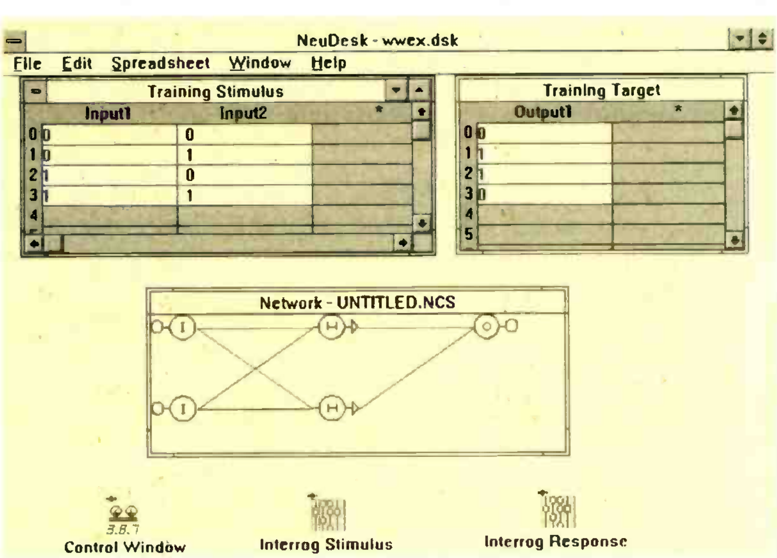
Installation follows the usual Windows pattern: use RUN APPLICATION from the Program Manager to run setup from the floppy disk. Unusually, the default directory tree is placed under C:\WINDOWS, although you are given the opportunity to change this.

Once copied on to the hard disk, you need to re-start Windows before running Neural Desk. The manual explains how to install the software manually, from which I deduced that no changes are required to any Windows files (such as WIN.INI or SYSTEM.INI).

Once installed, you should repress your natural desire to get started straight away, and read the manual instead. Although this is standard advice, it is not always advisable: some manuals are so bad they confuse rather than help - not the case with this one.

The "Introduction to Neural Nets" that follows "Installation and Setup" provides a wealth of practical information on applying networks to actual problems. The next chapter, "Getting Started with NeuDesk" teaches all the controls available in the software very painlessly by walking through a couple of very simple practical examples.

Anyone who has followed the manual this far will probably not need the next section, which takes the form of a reference manual for each command available. However, anyone wishing to use Dynamic Data Exchange will probably wear out the DDE chapter - this is by far the hardest part of the system.



Using Neural Desk

Installation creates a Neural Desk group, (**Fig.1**) inside which are icons for NeuDesk, NeuModel and NeuRun, and four of the example networks (XOR, Exrate, Adder and MortApp).

The obvious place to start would be the network design tool, which allows you to design your network graphically. However, the system can generate the network automatically from the definition of the inputs and outputs, and I found that I could not improve on the designs thus generated.

A large and complex design might need to be optimised by hand, and hints are given in the manual on how to do this. However, I doubt that this would be required often. This is fortunate, for I found the graphical editor rather clumsy: despite the help of a grid, it was difficult to lay out the neurons neatly, and editing the individual connections was awkward.

Here again, the manual is vital: the editor makes use of both mouse buttons and its conventions for selecting and editing are not immediately obvious.

The real place to start is NeuDesk, which provides a workspace for the other parts of the system. These consist of spreadsheet-like windows for training stimulus, training target outputs, interrogation stimulus, and interrogation outputs. There is also a window for a diagram of the network, a control panel and (while training the net) a moving graph of the error value. Not all of these windows need to be visible at once, but I found the extra resolution gained from switching from a standard VGA screen to Super-VGA made the package significantly easier to use.

The input spreadsheets define the number of input neurons in the net and each column corresponds to one input. Columns can be named, created and deleted, and all changes are reflected in the rest of the system. The outputs are defined by the output spreadsheets in exactly the same way.

This makes the whole thing very easy to use, and allows changes to be made with the greatest simplicity.

Each row of the training spreadsheet represents a set of data to be presented to the network. So, for example, if you want to train your network with five example inputs with their required outputs, you would have five rows in your training stimulus spreadsheet. The required output would also have to have five rows. Adding or deleting a

CONTINUED OVER PAGE

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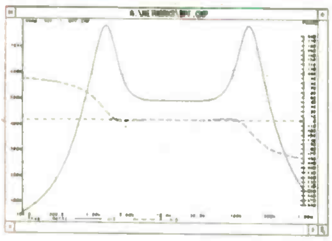
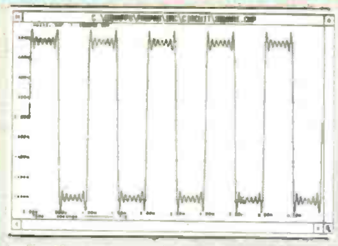


Impedance sweep

1 Frequency response
SPICE•AGE provides a clever hidden benefit. It first solves for circuit quiescence and only when the operating point is established does it release the correct small-signal results. This essential concept is featured in all Those Engineers' software. Numerical and graphical (log & lin) impedance, gain and phase results can be generated. A 'probe node' feature allows the output nodes to be changed. Output may be either dB or volts; the zero dB reference can be defined in six different ways.

2 DC Quiescent analysis
SPICE•AGE analyses DC voltages in any network and is useful, for example, for setting transistor bias. Non-linear components such as transistors and diodes are catered for. (The disk library of network models contains many commonly-used components – see below). This type of analysis is ideal for confirming bias conditions and establishing clipping margin prior to performing a transient analysis. Tabular results are given for each node; the reference node is user-selectable.

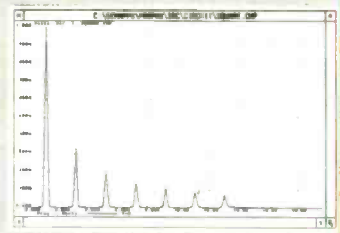
DC conditions within amplifier circuit



Square wave synthesis (transient analysis)

3 Transient analysis
The transient response arising from a wide range of inputs can be examined. 7 types of excitation are offered (impulse, sine wave, step, triangle, ramp, square, and pulse train); the parameters of each are user-definable. Reactive components may be pre-charged to steady-state condition. Up to 13 voltage generators and current generators may be connected. Sweep time is adjustable. Up to 4 probe nodes are allowed, and simultaneous plots permit easy comparison of results.

4 Fourier analyses now with Hanning window option
SPICE•AGE performs Fourier transforms on transient analysis data. This allows users to examine transient analysis waveforms for the most prevalent frequency components (amplitude is plotted against frequency). Functions as a simple spectrum analyser for snapshot of transients. Automatically interpolates from transient analysis data and handles up to 512 data values. Allows examination of waveform through different windows. Powerful analytical function is extremely easy to use.



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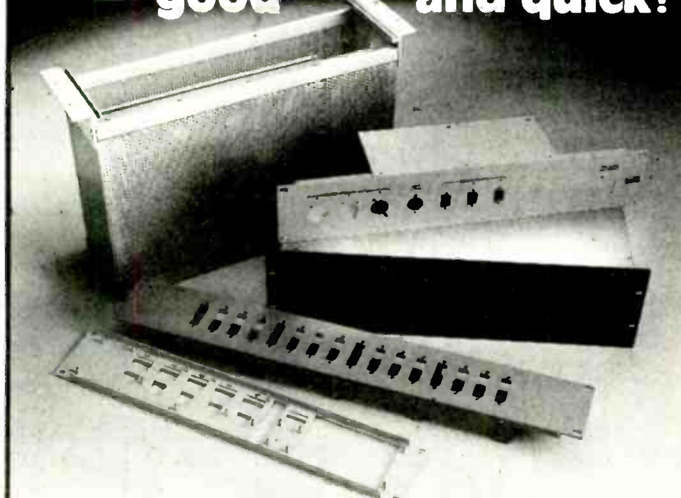

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CONTINUED FROM PAGE 136

row in one spreadsheet automatically changes the other.

Neural Desk follows the common neural network convention that all numbers are between 0 and 1. The spreadsheets have automatic scaling options that makes this easy (but not automatic), and the outputs are always in that range. If you have numeric input, it is easy enough to scale it to the 0-1 range using the built-in scaling function, and logical or yes/no inputs can be coded as 0 and 1.

A suitable network can be generated by entering the training stimulus and target outputs (**Fig. 2**), or you can design it yourself. Once designed, using either method, it can be edited as often as you wish, although this is best not attempted until you have some experience.

The system is supplied with four training algorithms (standard back-propagation, quick-propagation, Haffner modified back propagation, and stochastic back-propagation), and is designed to allow others to be added at a later date. While training, a window pops up showing a cumulative graph of the error value versus iterations of the training algorithm. The error value represents how near the net is to being trained, and can be defined as either the average or maximum difference between the current network outputs and the target outputs.

The graph window is useful, as it shows very quickly if the net is not going to converge to give the required results (**Fig. 4**). The shape of the curve is also very useful when trying to optimise training, or find out why a net is not converging. The manual briefly covers the interpretation of this curve, and with a little experimentation most users would be able to do this without having to refer to more formal texts on the subject.

Training can continue indefinitely, or you can set either an acceptable error value, or a maximum number of iterations ("Epochs"), or both. It is also possible to randomise the network values to start again.

Selecting good sets of training and test data requires some skill. There is an optimum amount of training for any given net: too little and the net cannot derive the rules connecting the inputs and outputs; too much and the net is less able to handle unknown data. Again, the manual provides useful guidance.

Once trained, you can test the network using the interrogation stimulus and results spreadsheets. These are just like the training spreadsheets, except that the net fills in the answers (**Fig. 5**).

It is possible to save the entire state of NeuDesk, allowing you to pick up where you left off last time. The network itself is stored separately, which makes it possible to try out several training stimuli and algorithms while keeping the results of each for comparison.

One further capability of Neural Desk is its ability to bolt several pre-trained networks together to produce a much larger system. It is possible (but not required) to fix the state of the sub-networks so that final training can be done on the complete system. This should be done with care: it is inherent in neural networks that they do not provide an exact output, and it is better to train each subnet using artificially precise values before several are connected together.

Dynamic Data Exchange

Setting up a DDE link is probably harder than creating the model in the first place, although this is mainly due to the way that DDE was defined by Microsoft. At present, few applications support DDE, but many more are due to be released in the near future.

Two of the most popular applications that can use DDE are Superbase (Fig.5) and Excel (**Fig.6**), and examples for both are contained on disk and in the manual. With the aid of these examples anyone familiar with Excel or Superbase could set up their own links, but you should be prepared to have to work at getting it right. Neural Desk can be very nearly completely controlled using the DDE link. This allows a working system to be created in such a way that the user never sees any of the Neural Desk screens.

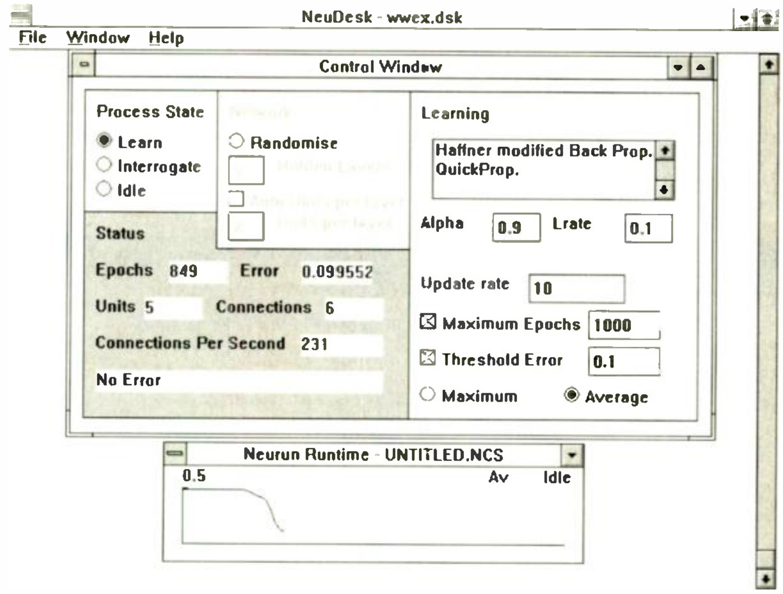


Fig. 3. XOR example: using the Control Window to train the network. Note the error value graph, which re-scales itself as necessary during training.

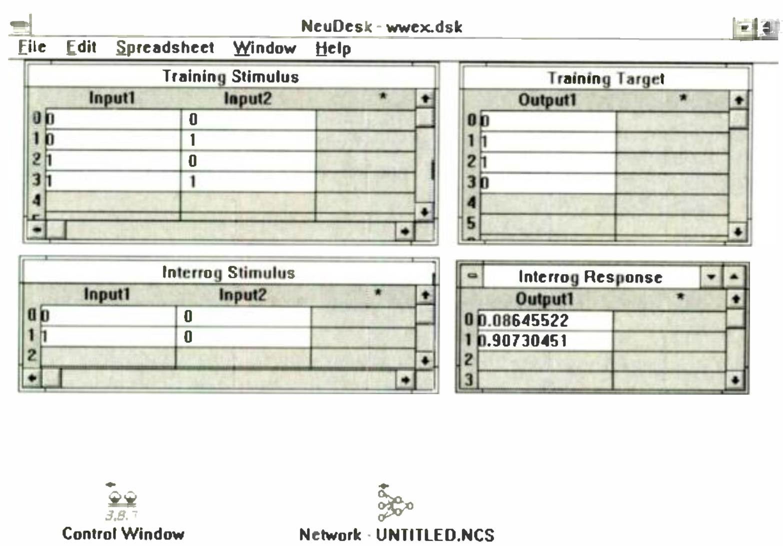


Fig. 4. Interrogation stimulus and results from the XOR example, showing the network implementing the learned function correctly.

The examples

The first example is an extremely simple one, to produce an exclusive-OR function. This is the sequence shown in the figures.

The network is trained with all possible inputs; in a real situation this is unlikely to be possible, but it makes a good starting point. An output greater than 0.9 is considered to be 1, and similarly 0.1 or less is assumed to be 0. The network is thus considered to be trained when the error is 0.1 or less, and this is set as the threshold error. It

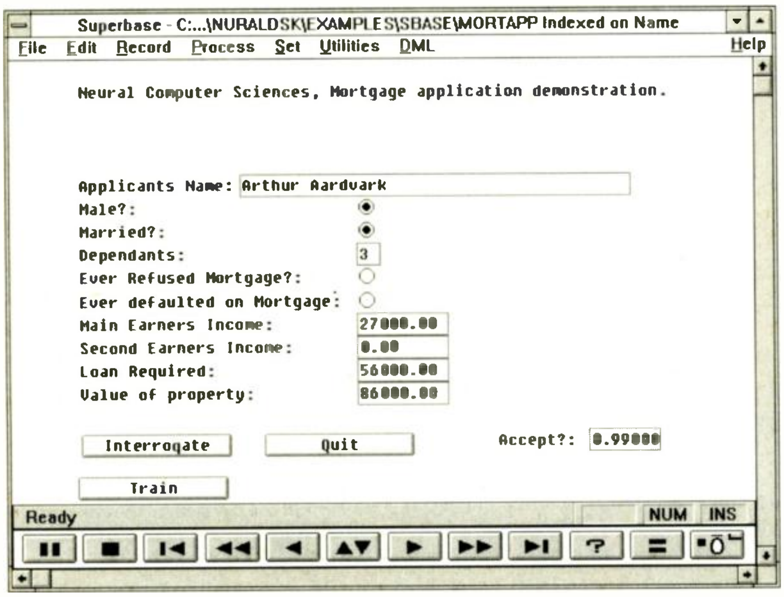


Fig. 5. The Superbase example. After the user has filled in the other information, the Decision box is filled in by the invisible network task.

is then a simple matter of selecting the "learn" button on the control panel, and watching the error value drop to 0.1.

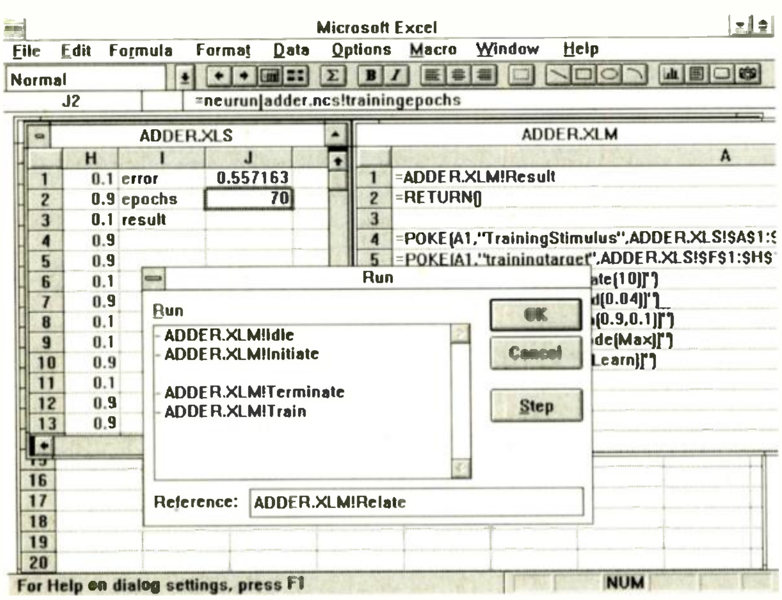
Once trained, you can apply whatever inputs you like, and see what the net produces. The outputs will never be precisely 0 or 1, but will be as near as you set the threshold error to be.

Perhaps surprisingly, you cannot set the threshold arbitrarily low; below a certain value, the network either loses generality (ie, it invents some peculiar connection between input and output that is not obvious), or never finishes training.

The other examples are designed to demonstrate DDE links to either Excel or Superbase. The Superbase example is the Mortgage Application Assessment described earlier. The single output is coded into NO (0.0-0.3), MAYBE (0.3-0.7) or YES (0.7-1.0). The network is trained from an existing database presumed to have been created from the decisions of a skilled assessor, and new additions to the database get the decision of the network as soon as the details are filled into the Superbase database.

The Excel examples include a prediction of the exchange rate between the Pound and German Mark. This one is interesting because the only inputs are the rate for the previous nine weeks, and the net is expected to find a pattern in the way that the rate has varied over that period.

Fig. 6. One of the Excel examples implements a binary adder.



Using the system

I found the software quite addictive; since there is never a perfect solution, it is very tempting to continue to fiddle with the various bits to improve the result. It is also very tempting to change things just to see what happens. However, it is time-consuming, particularly training.

To start with, a 20MHz 386DX computer with no co-processor was fast enough to go through the examples and start experimenting, and would be suitable for fairly simple applications. Once I had transferred to a 486, however, the software really began to show what it could do, and I would recommend this if at all possible. Note that this only applies to development: running a network is much less CPU-intensive than developing it, and even a 286 may be sufficient. In either case, a co-processor makes a significant difference.

The software is in general easy to learn and use. It follows all the Windows conventions, although there were a few areas where I would have preferred a slightly different approach. Overall, it is well-built and I found no "undocumented features" (ie bugs). The software provides excellent control over all stages of creating and using the networks.

Neural networks are the latest idea to be described as a solution looking for a problem. This software goes a long way toward making networks accessible: all that needs to be done is to provide the problem! ■

SUPPLIER DETAILS

Price is £895 for the development system. Licences for run-time systems are £99 per site (unrestricted number of users per site). Educational discounts are available, as is a demonstration disk.

For further information, contact: Neural Computer Sciences, Unit 3, Lulworth Court, Westwood Business Park, Nutwood Way, Totton, Hampshire SO4 3WW. Tel: (0703) 667775 Fax: (0703) 663730

Run your PC on DSP power

Allen Brown plugs two new TMS320C30 expansion cards into his PC and likes the result – but first-time users beware.

As an established product with proven performance the C30 is becoming an attractive option for the many processing needs making use of its floating point facility.

Two PC expansion cards now available, hosting the Texas Instruments *TMS320C30* digital signal processor, are the *TMS320C30* evaluation module (*EVM30*) distributed by Quarndon Electronics of Derby and the *TMS320C30* system board from Loughborough Sound Images. Both cards host a 33MHz version of the *C30* and have analogue I/O features, and though they are quite different, a discussion of their respective merits is useful when assessing suitability for specific applications.

TI TMS320C30 evaluation module

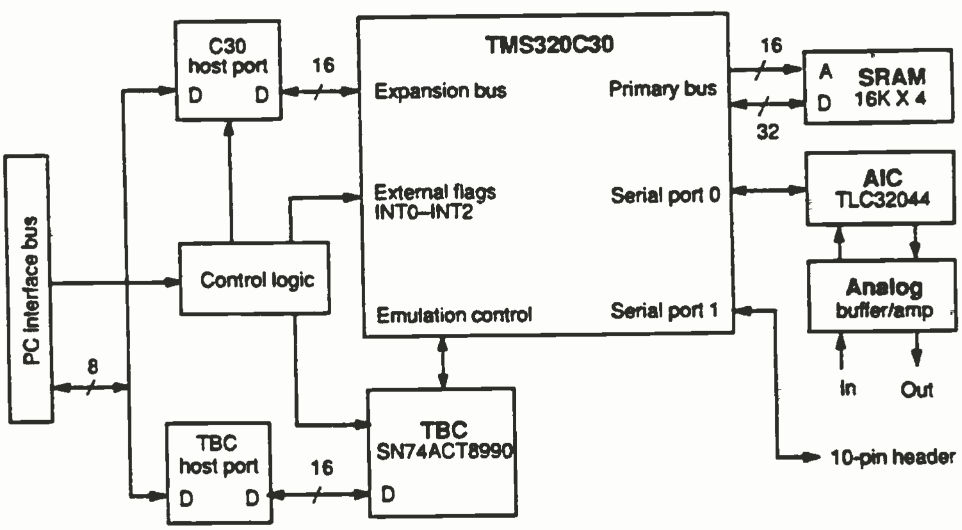
Texas Instruments has launched the low cost evaluation module (EVM), hosting a TMS320C30 with 16K words of zero wait state memory, in a clear attempt to promote acceptance of the *TMS320C30* floating point DSMP. Full details of its architecture can be found in references[2] but key features of the EVM are (**Fig. 1**):

- •33Mflops TMS320C30 floating point processor
- •16K words of sram on the primary bus
- •Analogue acquisition via a TLC32044
- •16-bit bidirectional PC host communications port
- •Embedded emulation support via a 74ACT8990 test bus controller (TBC).

The TBC allows operation to be emulated from a high level language (HLL) – which happens to be C – and the user can monitor, line by line from the C language source, execution on the *TMS320C30*. To match the expansion board buses with the PC host, two bidirectional bus transceivers are used (*SN74ALS652*) converting the host 8-bit accesses to the TBC to 16-bit word accesses. 8-bit access is required because, surprisingly, the board is furnished with an 8-bit ISA edge connector to make it compatible with the expansion bus on 8086 based PCs.

The EVM in a host PC is intended to be a suitable environment for evaluating algorithms, and Texas Instruments supplies a range of application routines[3] – including a program for implementing linear predictive coding based on a lattice filter design. The analogue I/O facilities consist of a 14-bit A-to-D and a 14-bit D-to-A which operate at 8kHz. I/O channels can be loaded direct-

Fig. 1. Key features of TI's TMS320C30 EVM.



ly onto an audio system, but the limited frequency range offered by the I/O does an injustice to the *TMS320C30* processor potential.

As part of the software support tools for the EVM, TI supplies an optimised C compiler[4], a cross assembler, a linker and a debugger application program (EVM30.EXE) – all of which run under MS-dos. **Figure 2** shows a screen display of the debugger and, to the credit of TI, a separate user's manual is also provided[5].

With the debugger, the user is able to monitor the register contents of the *TMS320C30* while following progress of the program from the source code written in C. TI also supplies a number of short routines for initialising the EVM and downloading code and data to the board.

It is at this point that the product begins to fail. There are no easy-to-use routines to help a new user to transfer data between the EVM and the host PC memory – an all too common problem in complex products of this nature. It is all very well having a full technical specification, but no-one can learn a language from reading a dictionary – a fact often ignored by technical authors writing user manuals for advanced products.

Loughborough Sound Images system board

LSI has been manufacturing PC expansion cards hosting DSP chips for a number of years and produces many good quality products. The TMS320C30 system board (**Fig. 3**) has two separate 16-bit I/O channels and is socketed to carry 256K words of sram. There are 192K words of zero wait state memory, with the remaining 64K words having one wait state and serving as dual ported memory, shared with the PC. 64K words are used as a post-box to transfer data between PC and card, so there is no compromise in performance when executing out of local memory. The card has an ISA 16-bit expansion bus (for AT and 386 PCs) and to enhance data transfer between other DSP expansion cards it is also furnished with the LSI DSPlink interface, negating the need for the PC expansion bus. The I/O components consist of two 16-bit A-to-Ds and two 16-bit D-to-As which have a maximum sampling performance of 200kHz. These are complemented by sample and hold amplifiers and fourth order filters on the analogue I/O to effect anti-aliasing and signal reconstruction (sync response) respectively. The sampling period is adjusted through software control by writing an appropriate word to a memory mapped address.

Support software

An area where LSI excels is the quality of support software for its DSP expansion cards – often the make or break for many expansion board products. C is clearly an important aspect of the *TMS320C30* system and LSI provides libraries for allowing Microsoft C programs (running on the PC) to interface with the expansion card. Functions (call routines) can also be used to great effect in operation of the expansion card.

Programming the *C30* in C for real-time application has been made somewhat easier by introduction of spox (signal processing operating executive) and LSI has a version of spox which runs on its C30 system board (to be reviewed in greater detail in a future issue).

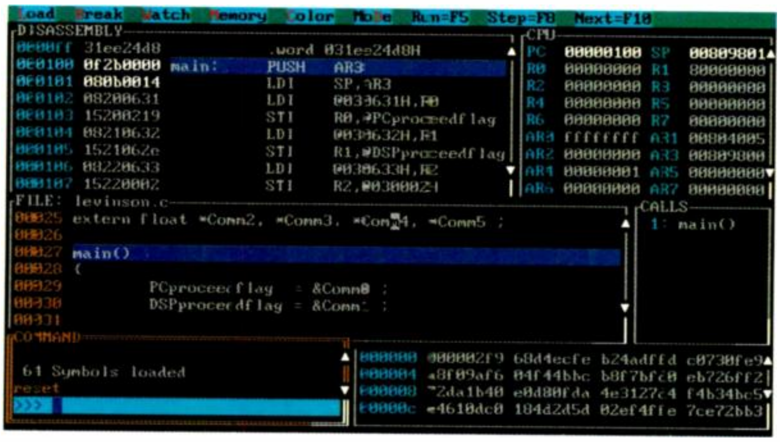


Fig. 2. Screen display of the debugger allowing the user to monitor the register contents of the TMS320C30 while following progress of the program from the source code written in C.

Two facilities for amending errors can be selected, the choice depending on whether the user works at assembler level or with a high level language (HLL).

For observing the architecture at assembler level an engineer can use C30MON – a mouse driven expansion board resident monitor offering considerable flexibility (**Fig. 4**).

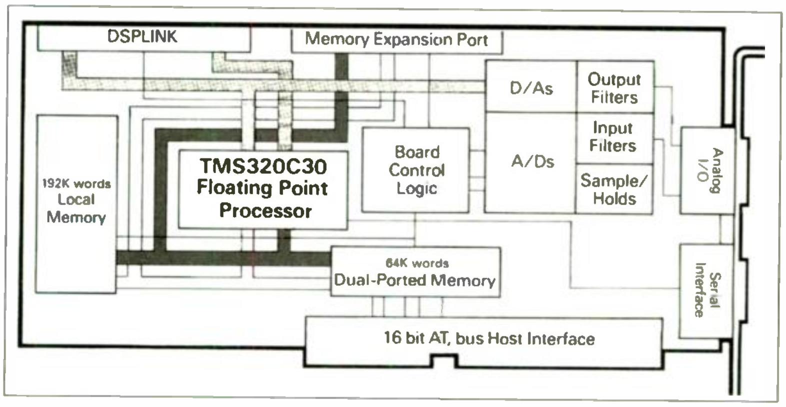


Fig. 3. LSI's TMS320C30 system board has two separate 16-bit I/O channels and is socketed to carry 256K words of sram.

DB30 (also mouse driven) is more likely to appeal to the HLL programmer and is almost identical to the Texas Instruments debugger (Fig. 2) which is also capable of showing the main register contents memory contents.

The package comes with a few sample programs in C and in assembly language. But perhaps a little weakness starts to show here – a first-time user learns much more from short easy programs than from long ones in the early learning stages of a new product.

If you are a first-time user this means that learning to use the product can be a bit of a struggle. The shortcoming is one which LSI would do well to address since DSP products are finding applications in other areas besides signal processing and the expertise is likely to be quite different in these other sectors.

System requirements
TI C30 EVM:
PC
Hard disk
MS-dos 3.x or higher
Microsoft mouse
Text editor

LSI TMS320C30 system board:
AT or 386-PC
Hard disk
Microsoft mouse
Text editor
TMS320C30 C compiler - optional

TMS320C30 architecture

TMS320C30, from the third generation of TI's range of signal processors, is housed in a 180-pin grid array (PGA) package and is TI's first floating point design.

Parallel architecture[1] has enabled a high performance of 33Mflops to be achieved and the machine cycle duration is 60ns. DMA can be carried out concurrently with floating point operations.

Performance means the processor is quickly gaining the reputation as the floating point workhorse DSP chip – an appearance in future PC designs such as the Multimedia engine is quite likely.

There are two members of the TMS320C3x family, the *C30* and *C31* (*C31* has a slightly reduced architecture and is available in a 132-pin plastic quad flat pack).

The package's pipeline architecture is made up of five main units: a fetch unit "fetches" instruction from memory; a decode unit decodes the instruction; and a read unit reads operands from memory if required. The execute unit reads operands from register file and executes, where necessary, and the DMA channel transfers data to and from memory.

The level of concurrency can be demonstrated by considering the structure of the package's assembly language coding. A single line of code can contain up to four sub-instructions – one for each of the first three units. During a single machine cycle the units will be working on four separate instructions according to pipeline operation. Main features are the CPU, memory organisation, bus structure, peripheral controller and the DMA facility.

Both 1K * 32-bit ram blocks can be accessed in a single machine cycle. Instruction words are 32-bit wide and the processor has an address space of 16M locations. As expected an extensive instruction set reflects the

EXTENDED PRECISION REGISTERS	AUXILIARY REGISTERS
R0=+5.877472452e-039 80FFFFFFFF	AR0 = 0003F6FF
R1=-2.000000000e+000 0080000000	AR1 = 00804005
R2=+5.877471754e-039 8000000000	AR2 = 00000000
R3=+1.000000000e+000 0000000000	AR3 = 00809800
R4=+1.000000000e+000 0000000000	AR4 = 00000001
R5=+1.000000000e+000 0000000000	AR5 = 00000000
R6=+1.000000000e+000 0000000000	AR6 = 00000000
R7=+1.000000000e+000 0000000000	AR7 = 00000000

SYSTEM REGISTERS		
DP = 00000003	BK = 00000000	IE = 00000000
IR0 = 00000000	SP = 0003F7C0	IF = 00000000
IR1 = 00000000	ST = 00000000	IOF = 00000080
RS = 0003F479	RE = 0003F479	RC = 00000000
	PC = <UNDEFINED>	

***Fig. 4** For observing the architecture at assembler level, the C30MON mouse driven expansion board resident monitor offers considerable flexibility.*

Favourable impressions

Both products create favourable impressions and though their prices are quite different each has to be judged on its own merit.

Availability

TI C30 EVM: Quarndon Electronics, Slack Lane, Derby. DE3 3ED. Tel: 0332 32651. £602.97 + VAT

LSI TMS320C30 system board: Loughborough Sound Images Ltd., The Technology Centre, Epinal Way, Loughborough, Leics. LE11 0QE. Tel: 0509 231843. Board £3295 + VAT. C30-SP high level C language development support package comprising MON30/SDS30 debug monitors and C interface library, TI assembler/linker and C compiler tools, spox application programming interface £1500 + VAT. Prices applicable from February 1.

Low cost of the EVM (£600) certainly makes it appealing for investigating the potential of the C30, and when bundled with all the software support tools it can be regarded as a bargain.

But as a learning tool for the *TMS320C30* the first-time user is likely to experience a tough climb and Texas Instruments would be well advised to add more easy-to-use-programs when it brings out the next edition of the EVM application book[3].

The LSI board is a well engineered product and is eminently suitable for development and testing of *TMS320C30* software whether at C level or at assembler. Documentation is detailed and well explained, but LSI could speed learning by providing easy examples of how to use the many library functions. The two channel I/O facilities allow the board to be used in real-time applications with a minimum degree of fuss.

The ever increasing catchment area for DSP processor applications now means that engineers and users with widely differing backgrounds will be looking to use PC expansion cards hosting DSP chips. Their ease of use for the first-time user will be a major selling point and this consideration must be accommodated when promoting the product.

References

1. TMS320C3x User's Guide, Texas Instruments (1988)
2. TMS320C30 Evaluation Module, Technical Reference, TI (1990).
3. DSP Applications with the TMS320C30 Evaluation Module: Selected Application Notes, TI (1991).
4. TMS320C30 Optimised C Compiler, Reference Guide, TI (1990)
5. TMS320C30 C Source Debugger User's Guide, TI (1990).

architecture, and the high degree of parallelism in the device means instructions can be grouped together to be executed in the same machine cycle. Several sections compose the CPU and a wealth of buses services each one.

The multiplier performs either 24-bit integer or 32-bit floating point multiplications and the 40-bit result can be added to the contents of one of the extended precision registers (R0-R7) – all within a single 60ns clock cycle.

Working in parallel with the multiplier is the arithmetic logic unit which can act as a 32-bit barrel shifter. Normal arithmetic operations (add, subtract – fixed and floating point) are performed by the ALU along with the standard logical operations (And, Or Not and Eor). Two auxiliary register arithmetic units (ARAUs) in the CPU can generate two simultaneous addresses with the necessary displacement, indexing, circular or bit-reversal addressing options. Again these operate in parallel with the multiplier and ALU.

As part of the general architecture, a register file contains 28 registers scattered throughout the chip, with a number contained within the CPU. For example the eight extended precision registers will maintain extended floating point precision and these act as accumulators in the normal sense of a microprocessor. Eight auxiliary 32-bit registers (AR0-AR7) support a variety of addressing modes and can be used to generate a 24-bit address. To support other system functions, twelve more 32-bit registers cater for stack management, processor status, interrupts, block instruction repeats and more addressing modes. Components in the CPU are serviced by two 32-bit register buses, REG1 and REG2, and two 40-bit CPU buses, CPU1 and CPU2. Combined, these enable the CPU to achieve its high degree of parallelism – one of the principal attributes of the *TMS320C30*.

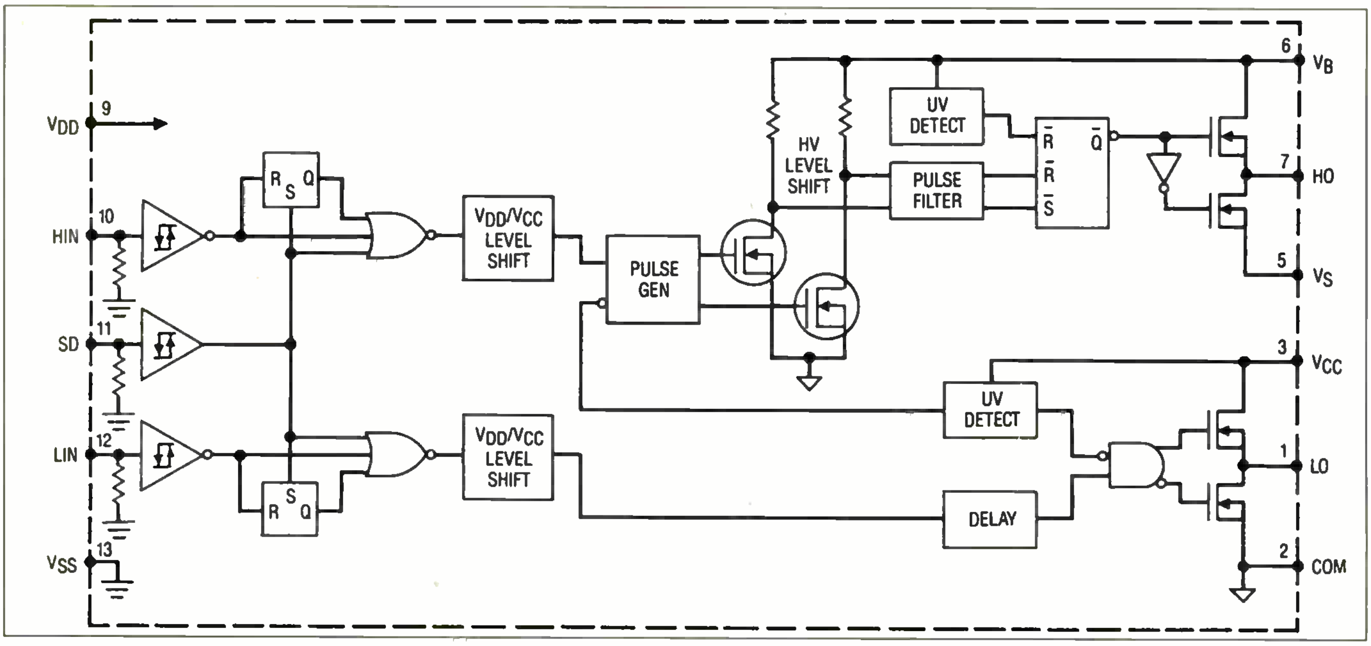
To service the rest of the chip's architecture there is a complex arrangement of separate buses; Program buses (PADDR and PDATA), data buses (DADDR1, DADDR2 and DDATA) and DMA buses (DMAADDR and DMADATA). Two interface bus pairs, primary and expansion, are used for accessing external address areas. The primary address bus is 24-bits wide but the expansion address bus is only 13 bits wide; both data buses are 32-bits wide.

Slow memory devices are accommodated by a RDY pin used to insert wait states. Program memory, data memory and I/O locations are mapped within the 16M address space. Since the data bus is 32-bits wide all instructions are either 24-bit or 32-bit depending on whether fixed point or floating point precision is required.

Memory is organised in four separate memory elements. Two ram blocks, 0 and 1, both have a depth of 1K and can be accessed by the CPU simultaneously in the same machine cycle. A cache block, consisting of 64 words (long words) 32-bits wide, enables efficient repeat instructions to be performed – of course when instructions are being executed from the cache memory the external buses are free for the DMA.

The cache controller uses the least-recently-run algorithm for maintaining address segments. Peripherals are controlled through a set of memory mapped registers via a dedicated peripheral bus (address and data). The peripheral modules consist of two serial ports (0 and 1) and two timers.

The serial ports work quite independently of each other and can be used for 8-bit, 16-bit, 24-bit or 32-bit data transfer. The timers act as event counters for either internal or external clocking requirements. Every location in the address map of the processor can be accessed by the DMA controller without disrupting operation of the CPU. To support the DMA controller there are separate address (DMAADDR) and data (DMADATA) buses together with a set of sixteen dedicated registers. Certain specified registers in the C30 are used to configure the DMA and set the start and end addresses and the amount of data to be transferred during an DMA operation.



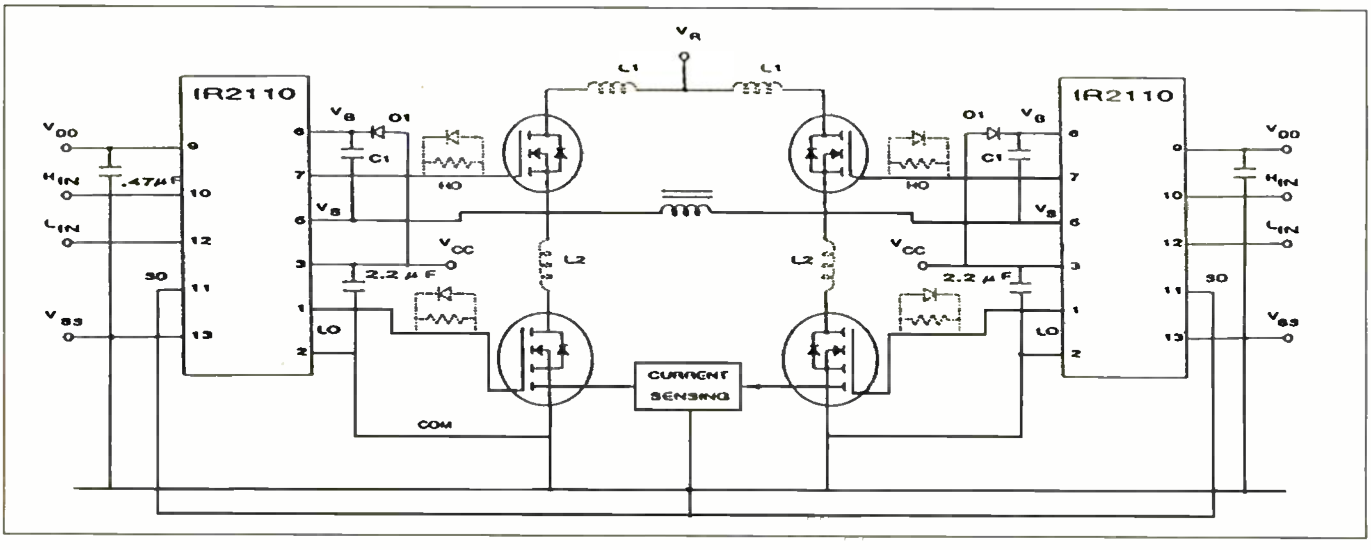
Floating mos-gate driver

Fig. 1. Block diagram of International Rectifier IR2110 floating mos-gate driver IC for both high-side and low-side mosfet or insulated-gate bipolar power switches.

Power mosfets used as high-side switches pose a number of problems for the gate driver: the gate voltage has to be higher than the drain (rail) voltage, which is usually the highest voltage available; gate drive derived from logic signals must be level-shifted towards the source voltage, which lies somewhere between the rails; and power taken by gate drive circuitry should not be high.

Figure 1 shows the principle adopted by International Rectifier in the *IR2110* gate driver, operating in either the bootstrap mode or with a floating power supply up to several hundred kHz. It contains most of the circuitry needed for one high-side and one

Fig. 2. H bridge with current control on a cycle-by-cycle basis. Stray inductances shown dotted must be reduced by decoupling and good board layout to avoid erratic high-side operation.



low-side power mosfet or insulated-gate bipolar transistor; both drive circuits, level translators and input logic circuit.

Each channel can be driven independently, gate drive following input command within the propagation delay (t_{on}= 120μs, t_{off} = 95μs), although a dead-time requirement can be arranged simply. High noise-immunity level translators are used, an increased immunity being conferred by a pulse-width discriminator which eliminates very short pulses.

As regards the high-side channel, the isolation tub in which it is built will float from +500V to -5V with respect to power ground. It floats at the potential of V_s set by the voltage of V_b, which is normally connected to the high-side source, so that if an isolated supply is connected between these two, the channel switches the output between this supply positive and its ground.

Since a mosfet possesses a capacitive input characteristic, the isolated supply can be replaced by a capacitor, charged by the 15V supply through the bootstrap diode during the off time. Power consumed is quite small.

Figure 2 is the circuit of an H bridge with cycle-by-cycle current-mode control, provided by current sensing and the shutdown input. Shutdown is latched, so that the power devices stay off while load current decays through their internal diodes, coming on again when the latch is reset at the next cycle. Turn-on and turn-off propagation delays are matched to within 10ns to ensure that no conduction overlap occurs, even if the on and off commands occur simultaneously. To further increase the safety margin, the diode/resistor networks delay turn-on without affecting turn-off to give even more dead time.

***International Rectifier**, Hurst Green, Oxted, Surrey RH8 9BB. Telephone 0883 713215.*

1GHz receiver front end

Application AN117 from GEC Plessey describes the *SL6442* in its role as amplifier/mixer working at 950MHz.

Figure 1 is a basic block diagram of the device, which contains a low-noise amplifier, gain controlled by a DC level, and two identical mixers for direct-conversion I and O receivers or image-cancelling superhets. Battery economy is provided and the *SL6442* works from 5V at around 4mA.

Figure 2 gives details of the illustrative circuit, which is optimised for maximum gain and low input-reflection coefficient at 950MHz, and gives a printed-board layout.

RF input is matched by means of a shorted stub in stripline form, matching of amplifier to mixer being by series inductor and mixer to 50Ω output by a variable LC network. Quadrature phase shift at the local oscillator input is accomplished by RC lead and lag networks, the inductor L_3 serving to resonate with the parasitic C between the two inputs and cancel it out. It is not easy to reconcile theory with practice in calculating the phase-shift component values in the presence of strays and these were found "empirically", according to the note — a very useful word, on occasion. At any rate, the values settled on give imbalances of around 1dB in amplitude and about 4° of phase.

Trimmers VC_1 and VC_2 give maximum output at an IF of 20MHz; other IFs will need a change in trimmer value or different inductors. Direct-conversion, zero-IF operation needs no change.

Overall power gain is 7dB; voltage gain 33dB into 100kΩ; overall double-sideband noise is 8.2dB; local oscillator drive is –5dBm and terminations are 50Ω.

***GEC Plessey Semiconductors**, Cheney Manor, Swindon, Wiltshire SN2 2QW. Telephone 0793 518000.*

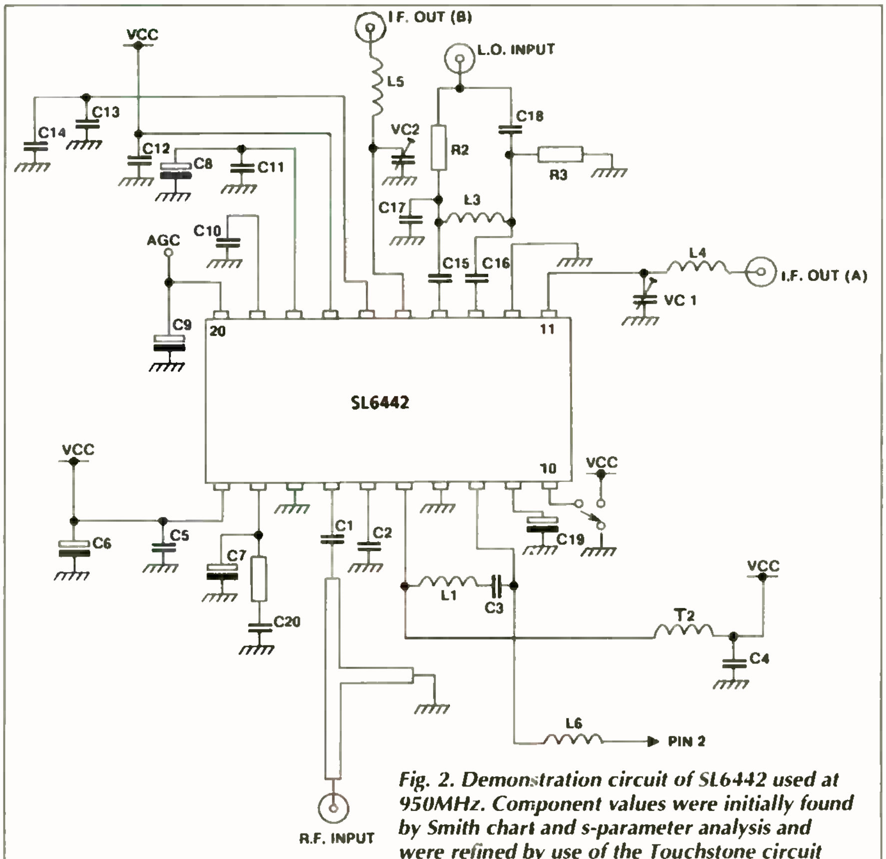


Fig. 2. Demonstration circuit of SL6442 used at 950MHz. Component values were initially found by Smith chart and s-parameter analysis and were refined by use of the Touchstone circuit simulator to achieve maximum gain and lowest input reflection at 950MHz.

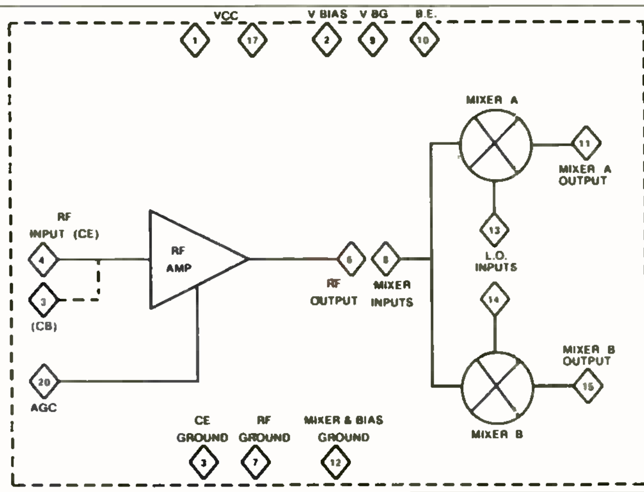


Fig.1. SL6442 from GEC Plessey, a low-noise amplifier/mixer front end for use at 1GHz.

Power regulators

Motorola's *MC34165* switching regulators contain the main functions for DC-to-DC conversion and are intended for step-up, step-down and inverting use with only a very few external bits and pieces.

Figure 1 shows the internals which, in essence, are a pair of voltage feedback comparators, a temperature-compensated reference, oscillator, driver and a current output switch which will handle more than 1.5A. There is current limiting and thermal shutdown, and an output for use by associated microprocessor-based systems as a reset controller. A high-voltage process renders the devices suitable for telecomms application and the cost is low enough to make them interesting to makers of cars and domestic products.

As the waveforms in **Fig.2** show, the *MC34165* operates with a fixed on-time, its off-time being determined by a comparator output. When output voltage is far too low, the output switches on and off at a rate set by the oscillator to "pump" the output filter capacitor. As the output reaches its nominal value, feedback to the comparator causes a latch to be set and stop the output switch conducting; the cycle is terminated early, duty cycle now being controlled by both oscillator and output voltage. From then on, the output voltage decays to below nominal and pumps up again past nominal continually, although the ripple shown in **Fig.2** is grossly exaggerated to show what is happening; in fact, ripple in step-up mode is 125mVp-p, 50mVp-p in the inverting configuration and 20mVp-p in step-down.

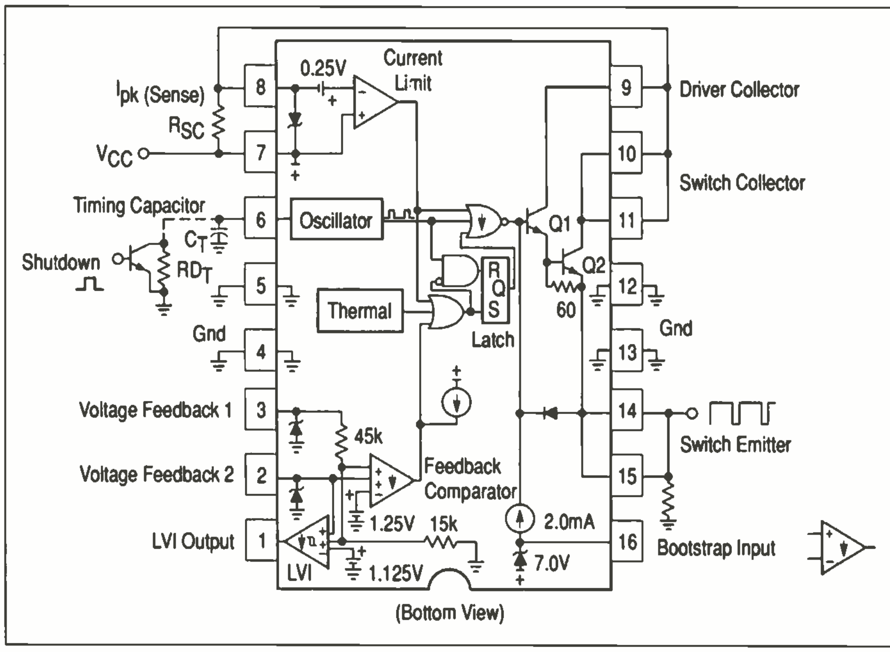
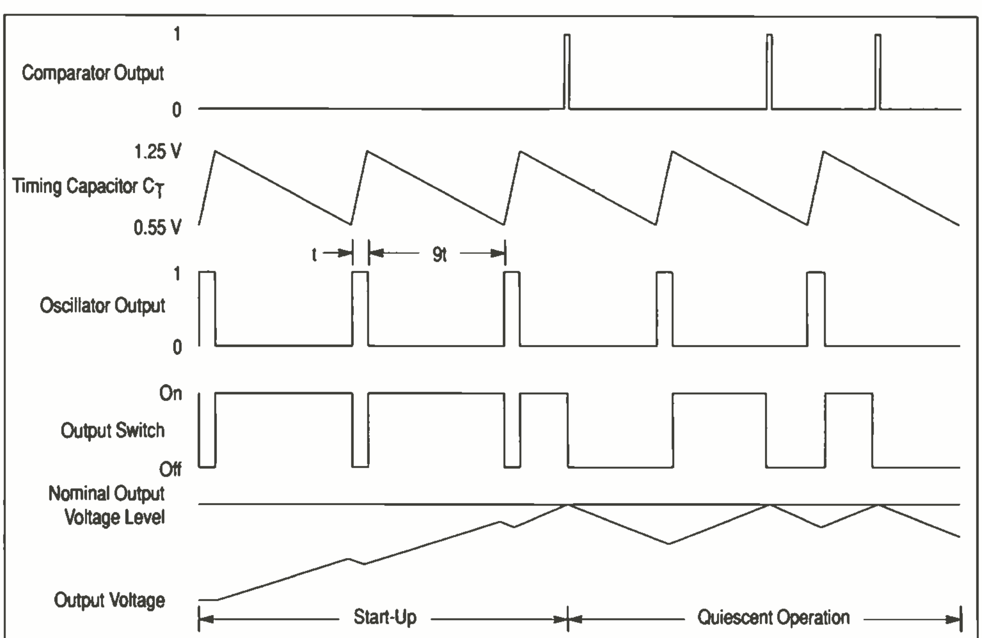


Fig.1. Internal block diagram of Motorola's MC34165 power switching regulator, which is capable of 1.5A with up to 65V output voltage.

Fig. 2. Waveforms of MC34165, showing ripple-current regulation. Oscillator determines switch-on time, while voltage feedback comparator sets switch-off, depending on voltage at output.



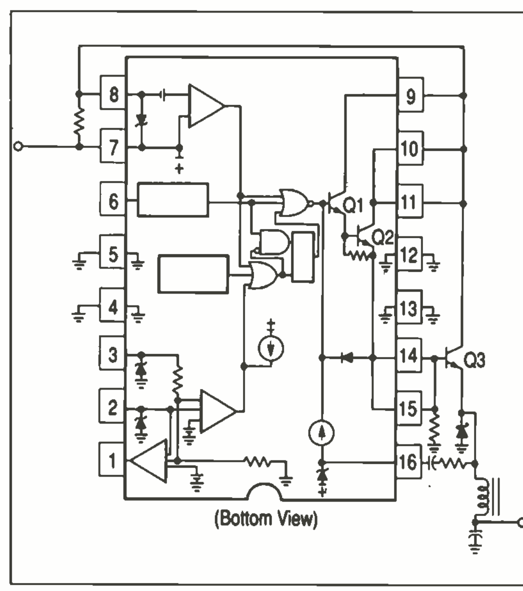
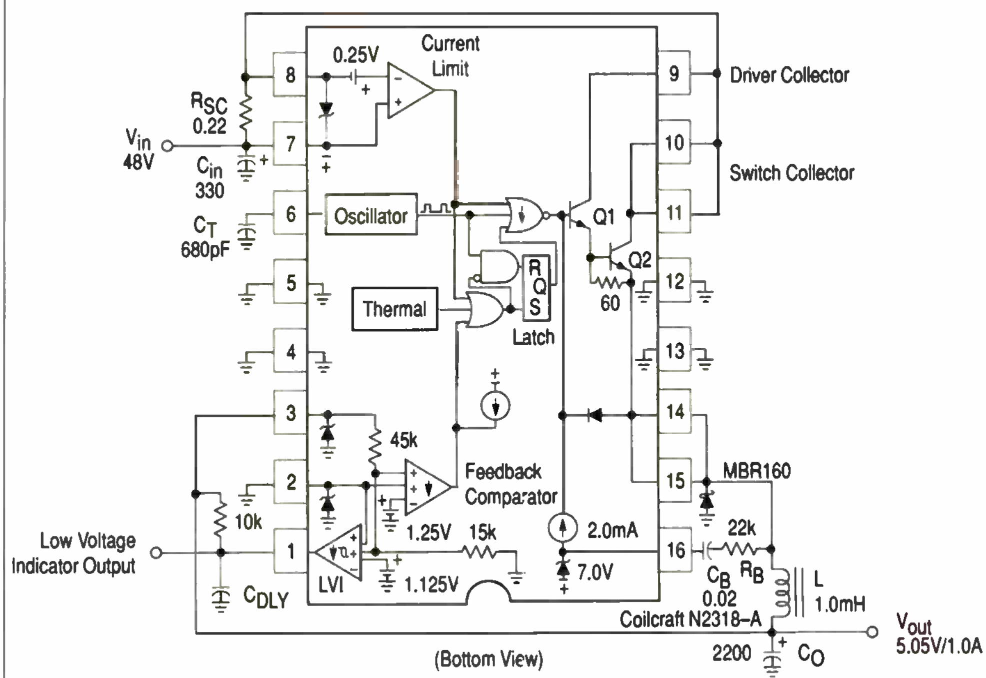


Fig. 3. If current requirement exceeds 1.5A, an external transistor can be used.

Capacitor C_T determines oscillator frequency and on time when output is below nominal. Current source and sink for C_T are internal and in a 9:1 ratio, the sawtooth shown being the result. Output is disabled during ramp-up by a pulse to the Nor gate from the oscillator. In some applications, a shorter discharging time to give a reduced duty cycle might be called for and the external R_T increases discharge current for this reason. A small transistor across C_T shuts the converter down.

Fig. 4. Step-down application of regulator, providing 5V at 1A. Low-voltage indicator output is for reset control of associated microprocessors.



A very low-value resistor R_{SC} from V_{CC} to the collector of the output transistor senses output current for the current limit circuit, needed if abnormal conditions such as overload or loss of feedback occur. Voltage across R_{SC} is monitored by the current limit comparator which, if voltage drop is more than 250mV, sets the latch and ends output switch conduction on each cycle.

Output driver current source and collector and output emitter and collector are taken out to separate pins, so that a choice of near-saturated darlington connection or saturation with a selected gain is offered. Collector-to-emitter maximum at the output transistor is 65V at 1.5A, but external current-boost transistors can be connected, as shown in **Fig.3**. **Figure 4** is a step-down application of the device, giving 5V, 1A at a line regulation (stabilisation) and load regulation of 9mV at 75% efficiency. ■

***Motorola Literature Centre**, 88 Tanners Drive, Blakelands, Milton Keynes MK14 5BP. Telephone 0908 614614.*

ACTIVE

A-to-D & D-to-A converters

16bit DAC. The AD669 Dacport is a monolithic 16bit d-to-a converter which integrates an on-board reference, span-programmable output, and double buffered latches. The output amplifier is pin programmable for unipolar or bipolar settable spans of 0 to +10V or -10 to +10V. Applications include multichannel industrial and laboratory automation and control equipment, precision analogue signal general circuitry, and simultaneous sampling instrumentation. It has a 30ns bus access time and 40ns write time, 15nV/s glitch energy (impulse), and 10µs output voltage settling time to within 0.0008% of full scale. Analog Devices, 0932 253320.

8bit ADC. The HI5700 is a monolithic cmos 8bit a-to-d flash converter with a 20Msample/s conversion rate. Typical specification is ±0.75 LSB integral and differential nonlinearity while consuming 550mW from a 5V supply. Typical differential phase and gain are 0.8° and 2% respectively at four times NTSC. Output latches coupled with an internal pipelined data bus structure lets the output data be updated every clock cycle after the initial conversion. Harris Semiconductor, 0276 686886.

14bit ADC/DAC. The Philips PCF5012 is a monolithic IC that implements full linear 14bit a-to-d and d-to-a conversion using delta-sigma conversion techniques. Designed for codec-type applications, this device is suitable for use in G722 wideband speech codecs. Sampling rate is from 8 to 16kHz and it provide a bandwidth (analogue) of 7kHz when sampling at 16kHz. The 28-pin dil version has serial I/O ports and the 44-pin QFP unit has parallel and serial ports. Macro, 0628 604383.

Video star: the Sony video ram available from Hakuto

12bit DACs. The Max501 and 502 are 12bit four-quadrant d-to-a converters that combine a bicmos amplifier with ±10V drive capability, and a laser trimmed thin-film resistor DAC on a single chip. The Max507 and 508 are 12bit voltage output d-to-a converters that combine a laser trimmed DAC, a bicmos output amplifier, and a 5V ±30ppm buried zener reference on a single IC. The 502 and 507 have 12bit wide interfaces and the 501 and 508 are in 8+4 formats. Maxim Integrated Products, 0734 845255.

Discrete active devices

HV mosfet. The Supertex TN2540NS mosfet has a drain-to-source breakdown voltage of 400V minimum, on resistance of 12Ω, and gate threshold voltage of 1.8V maximum. It is TTL logic level compatible and comes in a SOT89 (TO243AA) package. Applications include solid-state relays, telecommunications, and medical equipment. Kudos Thame, 0734 351010.

Power mosfets. The 2SK1380 power mosfet has an on-state resistance of typically 6.5mΩ and is for high-current switching applications such as motor drives and DC-DC converters. It comes in a TO-3P package and has maximum continuous ratings of 60V and 60A with a low associated maximum leakage current of 100µA. It can operate from a gate drive as low as 4V. Toshiba Electronics, 0276 694600.

Linear integrated circuits

Comms controller. The Zilog Z80C30 and Z85C30 serial communication controllers are cmos versions of the industry standard nmos units. The dual channel multi-protocol data communications controllers can be easily interfaced to CPUs with multiplexed or nonmultiplexed address and data buses. Each has a 10 by 19bit fifo and a 14bit byte counter to support high speed SDLC transfers using DMA controllers. Daisy chain interrupt hierarchy is supported. Celdis, 0734 585171.

Charger IC. The Teledyne TC675 battery charger control IC includes facilities for safely fast charging NiCd and Ni-hydride batteries directly from AC mains supply. It is suitable for use in battery powered applications such as notebook computers and portable instruments as well as power tools and emergency lighting systems. It has automatic overcharge protection and temperature and time controlled shut offs. Hunter Electronic Components, 0628 75911

Video amplifiers. The LT1193 and 1194 are differential input single-ended output DC-coupled amplifiers. The inputs have common mode rejection of 50dB at 10MHz. Both slew at 450V/µs, have bandwidths more than 35MHz, and more than 50mA of output drive current. They are specified driving 100Ω loads while operating from a single 5V supply as well as ±5 to ±8V supplies. Low offset voltage in 2mV, input bias current 500nA, and inputimpedance 100kΩ. The 1193 is optimised for a gain of two or more and the 1194 has a fixed gain of ten. Linear Technology, 0932 765688.

Real-time clock. The TC8521 real-time clock provides a low operational current drain of 250µA from a 5V supply. It comes in a 300mil 20-pin SO package. The 26 by 4bit on-chip ram needs 5µA to retain its data. The device incorporates a crystal oscillation unit, counter for the clock and calendar, and an alarm function. Toshiba Electronics, 0276 694600.

Video switch. The TA8639P is a five-channel monolithic video switch for use in televisions and videocassette recorders. It comes in a 16-pin plastic dip and will accept any five full-bandwidth video inputs and switch between them with a guaranteed maximum -60dB crosstalk. Three further control inputs are provided for selecting between the channels and also for switching between low and high impedance drive output. There are output amplifiers on each of the low and high impedance drive outputs, providing a typical 6dB gain. Toshiba Electronics, 0276 694600.

SCSI active terminator. The Buss Boss UC5601 is an active terminator with SCSI connection capabilities for the data processing and telecommunication industries. It terminates all 18 channels in an SCSI interconnecting bus through on-board thin-film resistors to an internal regulated voltage source. It has a disconnect feature which, on a single activation command, connects or isolates any terminators distributed throughout the network. It also reduces the supply current to less than 150µA, effectively putting the circuit into sleep mode while the cable lines are open. Unitrode, 081-318 1431.

Memory chips

64Mbit sram. The WS-XMxX comprises 64 1Mbit srams in a hermetically sealed 120-pin ceramic flatpack. It can retain data at voltages down to 2V and it can be configured as 8M by 8bit, 4M by 16 bit or 2M by 32bit. Because only an eighth of the memory is active during operation, the rest in stand-by mode, power consumption is 120mA at 5V. The stand-by current is 15mA. The read/write access time from address change or chip enable is between 100 and 150ns including buffer and decoding logic. Bowmar Instrument, 0932 851341.

128Kbit vram. The CXK1206M is a three-port (one write and two read) vram that can handle NTSC and Pal data. It is in a 960 column by 36 row by 4bit structure with asynchronous control of the three ports. The chip can be used in recursive mode for field display, TBC, noise reduction, and double scan, and in nonrecursive mode for picture-in-picture, zooming, multi-picture, and printer outputs. It runs on a 5V supply and comes in a 38-pin sop. Hakuto International, 0992 769090.

1Mbit flash eproms. The Intel 28F001BX-B and BX-T flash eproms use separately erasable blocks. They are organised as 128K by 8bit, and the architecture is divided into four blocks: one 8K boot block with lock out; two 4K parameter blocks; and one 112K main area. They use an integrated command port and state machine for simplified block erasure and byte reprogramming. They come in 32bit plastic dip, 32-lead PLCC, and 32-lead TSop packages. Jermyn Distribution, 0732 743743.

1Mbit sram. Sampling has begun for a 10 and 12ns 1Mbit sram. The unit can be an ECL I/O device organised as 1M by 1bit or 256K by 4bit, or it can be a TTL I/O device at 1M by 1bit, 256K by 4bit or 128K by 8bit. They are made with 0.8µm silicon gate bicmos technology. The pinout has centred paired Vcc and Vss pins and centred I/O pins that provide reduced inductance due to shortened leadframe paths. The added pair of Vcc and Vss pins also shortens the internal power and ground busing. Motorola, 0908 614614.

Microprocessors and controllers

30MHz transputer. Production volumes are available of the 30MHz version of the IMS T805 transputer which gives 30Mips and 4.3Mflops peak performance, 50% more than the 20MHz version. The T805 is a 32bit chip with an interrupt response time of 630ns, average power consumption of 660mW, programmable external memory bus with dram control, and pin count of 84. An external 5MHz clock is all that is needed to drive the on-chip phase locked loop. Inmos, 0454 616616.

Optical devices

Plastic leds. Three GaAs plastic leds provide a minimum radiant intensity of 45mW/Sr rising to 120mW/Sr at a forward current of 100mA. The OPE5594 and 5694 are available in T1.75 5mm plastic packages with respective half angles of ±10° and ±17°, and the OPE5794 comes in a T1 3mm package with a half angle of ±17°. The 5594 and 5694 have a typical 1.4V forward voltage and an operating range from -30 to +70°C, and the 5794 has a typical 1.2V forward voltage and operates from -20 to +70°C. All have a peak wavelength of 940nm at a forward current of 40mA, a capacitance of 25pF, and a maximum reverse current of 10μA. Pacer Components, 0734 845280.

Infra-red leds. The SFH474, 475 and 476 infra-red led emitters have emission angles of ±11°, ±17° and ±28° respectively. Rise and fall time is 100ns at 100mA and the devices can be modulated at speeds up to 5MHz. Total radiated power is 10mW at 100mA with a peak wavelength of 830nm. The SFH414, 415 and 416 have the same respective emission half-angles as the figures above. Their total radiated power is 22mW which results in a minimum intensity of 63mW/Sr at 100mA. Siemens, 0932 752616.

Fibre optic modules. Toslink fibre-optic modules for digital audio applications include transmitters and receivers, as well as optically matched cables and connectors. The transmitters and receivers work from 5V power supplies and can be directly interfaced with standard TTL circuitry. Transmission distances up to 10m are possible and they can handle data rates up to 6Mbit/s and exhibit pulse width distortion figures down to ±20ns at full rated speed and distance. Toshiba Electronics, 0276 694600.

Oscillators

Clock oscillators. The E500 Connor-Winfield ECL clock oscillators are available in half-height packages in through-hole and surface mount versions. Frequency range is from 24 to 180MHz. Operating temperature is from 0 to 70°C but an industrial -40 to +85°C version can also be supplied. Frequency stabilities are available to 25ppm. Supply voltage can be -5.2, -4.5 or +5V DC. Litton Precision Products, 0628 486060.

Programmable controllers

Stripped controller. The Microcontroller programmable controller is available in a stripped down version. It can handle monitoring or supervision functions from 16 to 192 inputs and outputs. It has built-in counters, timers and shift registers that give a processing speed of 4.25μs per instruction step. Programming is via a hand-held control or an IBM compatible PC. Its footprint is 200 by 130mm. Matsushita Automation Controls, 0908 231555.

PASSIVE

Passive components

Chip capacitor. A 50V multilayer ceramic chip capacitor is available in an 0603 package style. The dielectric can be either NPO (1 to 220pF) or X7R (270pF to 6.8nF). Terminations are of nickel barrier. Although it is more difficult to pick and place and is not so easily reworked as the larger 0805 size it replaces, it is more resistant to thermal and mechanical shocks. AVX, 0252 336868.

Transformers. The Avel PT short-circuit proof transformers have an internal thermal device which protects them from overload or short-circuit conditions. They automatically revert to normal use when the cause of the overloading is removed and normal operating temperature is achieved. They operate from a 240V 50 or 60Hz mains supply and have 4.5, 7.5 and 13VA ratings. Dual output windings can be operated in series or parallel with 6, 8, 9, 12, 15 and 18 secondary voltages (and times two) being available. ESD Distribution, 0279 626777.

Tantalum caps. Available taped and reeled for automatic placement, the SVH surface-mount tantalum capacitors can withstand soldering temperatures up to 260°C for 10s fully immersed. There are 30 devices in the series covering capacitances from 0.1 to 33μF in four moulded-resin package sizes. Temperature cycling tolerance is -55 to +125°C for 1000 cycles, and 1000h at 85°C with 85% relative humidity. Working voltages are from 10 to 35V DC and standard capacitance tolerances are ±10 and ±20%. NEC Electronics, 0908 691133.

Palm reader: hand-held digital storage scope from Tektronix.

Electrolytic caps. The Panasonic SU radial and axial electrolytic capacitors are available from 1 to 4700μF. The axial versions have five voltage ratings from 10 to 450V and the radial types have four ratings from 16 to63V. Operating range is from -40 to +85°C except for the 450V axials whose minimum temperature is -25°C. All have a minimum life of 2000h at 85°C. Capacitance tolerance is ±20%. RS Components, 0536 201234.

Chip capacitors. High Q chip capacitors are for use between 20MHz and 1GHz in communications and alarm systems. Capacitances are from 0.47 to 680pF at rated voltages of 50, 63, 100 or 200V. Operating temperature is between -55 and +125°C. There is a choice of nickel barrier or silver palladium terminations. Environment classification is 55/125/56 and they are available on tape or reel or in bulk packaging. Vitramon, 06285 24933.

Connectors and cabling

Subminiature Ds. Harting subminiature D connectors are MILC24308 and DIN41652 compliant and have a contact range of between 9 and 50 ways. Row spacings are 2.54 or 2.84mm. Ground continuity is via dimples on the body of the connectors. Terminations include solder buckets for discrete wiring, straight solder pins with or without grounding contacts, wrap posts for automated wiring techniques, and IDC. Contact ratings are 7.5A turned, 6.5A stamped, and 2A IDC. Gothic Crellon, 0734 788878.

Wire connectors. A range of P-Conn screw-on wire connectors is for use up to 600V and is available in nut and wing styles. Nut connections are for 12 and 20AWG wire sizes, have contoured ribs to improve grip, and a funnel entry that guides wires into the connector. Wing connectors have more torque and come in three sizes from 6 to 22AWG. Both come in industry standard colours although a green grounding wing style is available which allows a through wire between device and ground. Panduit, 0634 660811.

IDC assemblies. An IDC system has been introduced for mating with terminal strips on 1.27 by 2.54mm centres. The FCSD socket female strips have dual beam tuning fork style beryllium copper contacts for gas tight connections. The FCMD terminal male strips also have BeCu contacts and both can be specified from 5 to 40 positions per row. Assembled height of the male is 8mm and the female 11.05mm. Samtec Electronics, 0236 739292.

Displays

Led cluster. China Semiconductor has introduced an led cluster display product for use in illuminated signs. Each device forms a single dot in the finished sign giving the constructor freedom to design his or her own matrix. The clusters are weather-proof and available in 1 or 2in diameters with 14 or 15 individual lamps respectively. They come in single colour red or green or dual colour each of which can be illuminated separately or in combination to give a

Lost is space: Panasonic electrolytic capacitors from RS Components.

three colour red, green and yellow palette. Clere Electronics, 0635 298574.

Supertwist lcd. A VGA compatible black-and-white supertwist LCD module, the LMG5160XUFC, is 8.5mm thick including CFL backlight and associated light guide. It uses an antiglare upper polariser, a transmissive bottom polariser, and a plastic optical phase shift retardation film which cancels out less desirable colour effects. Resolution is 640 by 480 and the unit measures 255 by 172mm. Hitachi, 0628 585000.

Hardware

Quad flat pack. A ceramic quad flat package for surface mount asics is claimed to dissipate heat better than plastic packs yet costs less than conventional ceramic packs. It measures 3 by 3.2mm and has a typical specification of 38°C/W for a 208-pin pack without heatsink. Fujitsu Microelectronics, 0628 76100.

ABS enclosures. PacTec enclosures can be customised with EMI and RFI shielding, flame retardant coating, and screen printed customer logos. They are made from impact resistant ABS in moulded-through colours. They have moulded-in bosses, card and panel guides, and the availability of customised panels. OK Industries, 0703 619841

ABS boxes. Hammond enclosures, instrument cases and die-cast boxes are supplied in kit form and made from flame retardant ABS. The option of a nickel acrylic coating is available for EMI/RFI shielding. The enclosure kit contains base, lid, four M4 fixing screws, and four guide cards that accept horizontal or vertical 1.6mm PCBs on a 5mm grid. An IP65 sealing kit with gasket and four O rings is a further option. Radiatron Components, 081-891 1221.

Instrumentation

Multifunction generator. The 2030 20MHz multifunction generator uses a direct digital synthesis technique and a phase-slip clock to generate waveforms with amplitude and frequency resolution of 0.01% and 0.1ppm respectively. Standard function waveforms include sine, square, triangle, pulse, ramp, and noise. Modulated waveforms include AM, FM, OM, exponential decay, sinX/X, and linear and log sweeps. Up to four waveforms can be combined. Analogic, 0344 860111.

Coaxial cord tester. A battery-powered coaxial cord tester can be used for continuity and vibration testing. Leads are checked for open or short circuits and for insecure connections. It checks that inner and outer conductors are fully connected without opens and shorts. The connections are continuously scanned using a pulse stretching technique. The vibration test reveals bad connections which have become microphonic but which still pass a continuity test. An amplitude demodulator drives an audio amplifier and a loud speaker. Faults are perceived as crackles from the speaker as the cord is moved and flexed. Brantham Engineering, 0376 518384.

Solderability tester. The Must System II is a solderability tester with integral computer control for surface mounted and leaded through-hole components. It works on the wetting balance principle and its features include: storage and recall of component data, test parameters, and results; colour graphic display facilities; automatic components alignment; multi-lead component testing capability; and automatic pass or fail analysis. Multicore Solders, 0442 233233.

Digital analysis. The Palmoscope is an instrument that can convert an oscilloscope into a digital analysis tool. It has three instruments in a single probe - logic analyser, signal multiplexer, and trigger probe. It fits in the palm of a hand and will connect to any oscilloscope. It has eight channels which can be increased to 24 by connecting three instruments together. External clock frequency is DC to 20Mhz and internal is about 800kHz. Symmetron, Athens (1) 7751 488.

60MHz scope. The dual-channel 224 is a 60MHz hand-held digitising oscilloscope. It has a TV field trigger, weighs 4.4 lbs, and meets MILT28800D standards for shock and vibration. Its two rechargeable batteries provide3h of operation. It has an isolated channel architecture for making safe floating measurements. It is programmable from the RS232C port. Tektronix, 0628 486000.

Interfaces

Instrument control. Two interface kits can turn HP Apollo 9000 series 400 workstations into instrument controllers. e GPIB-A/AT and GPIB-A/PC kits include an IEEE488.2 controller board and the GPIB11 Domain/Os software. The AT board uses the Nat4882 and Turbo 488 custom chips and has data transfer rates of 1Mbyte/s for reads and writes. The PC kit is slower at 400Kbyte/s. Domain/Os includes a high speed driver, C interface, application debugger, and screen based configuration utility. National Instruments, 0635 523545.

Sun gateway. Etherbit is an interface between Sun workstations and industrial Bitbus I/O modules. Each Bitbus network can comprise up to 250 multi-tasking modules, each with multi-channel I/O capability, linked by a single twisted wire cable which can be up to 13.2km long. This means clusters of I/O can be distributed over a wide area. Each module can run up to eight tasks such as concurrent scanning, local data storage, and Bitbus communication. Quin Systems, 0734 771077.

Literature

Surface mount devices. The sixth edition of the Flint surface mount devices user guide has 132 pages including functional selection guides and technical specifications. For production engineers there are component outlines, footprints and tape and reel specifications. It is in full colour and costs nothing. Flint Distribution, 0530 510333.

Production equipment

Solder pack. By using flexible sealed Flexpak pouches, singly or in various weight combinations, screens can be properly charged with fresh solder cream without pre-weighing from jars. The pouch design prevents worker contact with the solder cream improving safety in handling. The polypropylene aluminium nylon laminate package comes with a dispenser that empties the entire package with no solder waste. Stenciling and screening grade creams come in 50 and 150g packs. Various alloys and flux systems are also available. ESP, 0234 211582.

Power supplies

200W supply. With a 86 by 140 by 150mm footprint, the SA201 200W power supply uses universal input technology to sense the applied input voltage level and automatically strap the unit for 115 or 230V AC operation. Outputs are +5V at 20A, +12V at 8A, -12V at 0.5A, and -5V at 0.5A. It operates in ambient temperatures up to 50°C and protection is provided for overvoltage, overload, and overtemperature conditions. Astec Standard Power, 0246 455946.

Plug-in supply. The Trivolt EC50 is a single fixed frequency 50W converter that accepts 93 to 262V AC input and gives 5V at 5A (9A peak), 12V at 0.8A (4A peak for disc drive start up), and -12V at 0.8A. Ripple and noise are less than 40mV peak-to-peak for all outputs. It measures 3U by 8HP by 160mm deep. Optional front panels are available. BICC-Vero Electronics, 0489 780078.

Switch mode supplies. The Omega range of switch-mode power supplies has been extended with the introduction of 1 and 1.5kW versions. Input voltage range is 85 to 265V AC. The footprint is 279 by 203mm for both and the 1kW is 80mm high and the 1.5kW 127mm. Power factor is

0.99. There can be single or multiple outputs of 5, 12, 24, or 48V all of which are adjustable. Coutant Lambda, 0271 863781.

DC-DC converter. The LT1109 is a 5 or 12V fixed output step-up DC-to-DC converter from Linear Technology.It needs a surface-mount inductor, diode and capacitor to construct a complete step-up converter. It has a 12V output at 60mA which can be generated from a 5V ±10% supply. It can also be used for a 3 to 5V converter. There are eight pins including a shut-down pin which reduces supply current to 320µA. Micro Call, 0844 261939.

Radio communications products

HF-SSB radio. The TW2000S is a HF radio with a programmable capability that eliminates the need for channel crystals. It has a ten channel capability over the 2 to 20MHz frequency range. Output power is 125W and it operates directly from standard 12V DC sources. A separate AC mains supply is available. All channel frequencies are phase-locked to a single high-stability reference oscillator. Channel programming and radio configuration can be done using the RS232 port of a PC. A password protected program ensures only authorised users can reconfigure the radio. Trans World Communications, 0101 619 747 1079.

Programmers

Gang programmer. The PL800 module is for gang programming waferscale integration programmable system devices such as the PSD301. The module is for use with the L9000 modular programmer. PSD301 provides eprom, sram, and port expansion while catering for 8 or 16bit data buses and multiplexed or non-multiplexed address buses. Lloyd Research, 0489 574040.

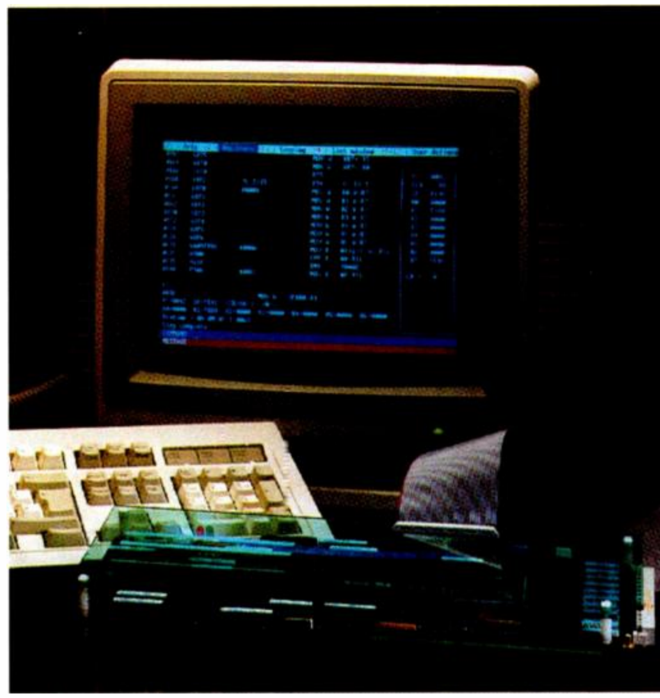
Switches and relays

Keyswitch. A three position keyswitch offers a choice of mounting configurations including flush mounting in a mosaic tile. Called Swisstac, it has three normally open, normally closed or changeover poles, with two polesselected in one position and one in the other. The centre position is off. A modular range of bezels is available including 18mm diameter, 18 by 18mm, 18 by 24mm, 24 by 24mm, and 24mm diameter. The 18 by 18mm version can be flush mounted in a 24 by 24mm mosaic tile with the aid of an adaptor. It can be supplied with IP40 or IP65 protection. Highland Switch, 0444 245021.

Micro relay. The TK micro relay has a footprint of 10.6 by 9mm and an off-the-board height of 4mm. It can withstand a shock of up to 50g and full load ambient temperature of 70°C. It is sealed to IP67 and has a mechanical life of more than 100 million operations. Surge voltage withstand between contacts and coil is 2.5kV for 20µs. It has a single changeover contact rated at 60W and consumes less than 140mW at nominal coil voltage. Matsushita Automation Controls, 0908 231555.

Transducers and sensors

Displacement transducer. The D5/AW displacement transducers can be used fully submerged in liquid and are made from stainless steel, electron beam welded to give hermetic sealing up to pressures of 2000psi. Working ranges from ±12.5 to ±50mm are available with either separable or spring return probes. They operate from a 6 to 12V DC supply and provide an output of typically 3.5V/25mm. RDP Electronics, 0902 457512.



On the circuit: Hitachi's PC based in-circuit emulator.

COMPUTER

Computer board level products

DSP option. A digital signal processor option, the 683DSP, has been added to the 6100 waveform analyser so that it can perform real-time signal processing and spectral analysis. The plug-in DSP board has a 25Mflop processor increasing the 6100's performance by a factor of 300. This makes real time processing possible in time and frequency domains on records up to 32K data points. Analogic, 0344 860111.

Extender card. This PC extender card raises a daughter board above the microcomputer case while maintaining electrical continuity with the backplane, facilitating calibration, development or testing of the board. Unlike theearlier version, it is a four layer board so it can operate at higher clock speeds. It has internal ground and power planes to minimise voltage drop and minimal track lengths to reduce signal skew and timing delays. All signal lines are protected by a guard tracking technique to minimise crosstalk between adjacent lines. BICC-Vero Electronics, 0489 780078.

Ethernet controller. The CL486/296 is a 486-based Multibus Ethernet controller board using the 82596 32bit lan coprocessor which supports data rates up to 57Mbit/s synchronous or 76.8Kbaud asynchronous communications. Further I/O expansion is achievable through the iSBX interface. On-board processing is performed by a 25MHz 486 CPU and a 32bit 82380 DMA controller. It has a choice of 2 or 8Mbyte of fast page mode dram and up to 4Mbyte of eprom. The user's operating system can be either downloaded to the board via message passing or stored in local memory. Concurrent Technologies, 0206 752626.

DMA link. The CC386/11W Multibus II board with a DR11W interface provides a parallel DMA link between Multibus II systems and DEC computers at transfer rates up to 1.1Mbyte/s. It can also operate as a parallel communications link at transfer rates up to 4Mbyte/s. DMA with fifo support is provided on transmit and receive channels. Access to the interface is via two 40-way connectors on the front panel. The board has a 16MHz 386SX CPU supporting local data rates up to 16Mbyte/s with zero wait state memory access. Either 1 or 4Mbyte of fast page mode dram is provided and up to 2Mbyte of eprom. Concurrent Technologies, 0206 752626.

Bus extension. The PCL757 is a switchable 16bit PC-bus extender with complete signal buffering as well as on-board power rail fuses. The extender has an on-board on/off switch to let cards be plugged in and removed from the extender without disturbing PC operation or requiring the PC to be powered down. It is suitable for testing, repair and trouble shooting of PC add-on cards and can also be used as a development tool for prototype testing. Integrated Measurement Systems, 0703 771143.

Digital I/O. The MPV920 digital I/O board for the VMEbus has 64 input channels arranged in eight banks, the MPV921 has 16 input and 64 output channels, and the MPV922 has 40 inputs and 32 outputs. On each board interrupts can be asserted by any one of 16 input channels in response to a change of state. Each board has four 24bit counters. Anti-bounce protection is included on all inputs. Delays are jumper selectable to 70µs, 1ms or 7ms. Pentland Systems, 0506 464666.

Computer systems

Rack-mount PC. A 48V version of the TMI3014 rack-mountable PC has been introduced. It uses a 19in rack mountable chassis and has a 14-slot passive backplane. It can be configured with an optional split backplane for dual processing. The steel chassis is 7in high and 22in deep, is nickel plated to reduce EMI and RFI susceptibility, and has a positive-pressure filtration system to

Beam me up: Digitran's infra-red unit boldly takes keyboards where they have never gone before.

protect against dirt and dust. Four half-height peripheral slots are available. Crellon Microsystems, 0734 788878.

Development and evaluation

In-circuit emulator. A PC based in-circuit emulator has been introduced for use with the H8/330 microcontroller. At its heart is the PCE8330 board which can be used for software development and for debugging user hardware when connected remotely to a target system. The software can control and interrogate the emulator hardware through a command line on the host PC. A complex breakpoint system, using dynamic, program counter and static breakpoints, allows various conditions that can stop real-time emulation. It also has a real-time trace facility. Hitachi, 0628 585000.

PLD development. PLDshell Plus from Intel is a complete development menu-driven environment for designs based on programmable logic devices. It will run on an IBM PC or compatible. The user can choose each of the steps in the design flow - text edit, compile, view, program, and so on - from the access screen. It has device libraries for popular PLD types. The PLDasm compiler is syntax compatible with Palsm-2 software. Jermyn Distribution, 0732 743743.

Mass storage devices

Optical drive. Optistore 128 is a rewritable 3.5in optical storage subsystem that can store 128Mbyte on asingle removable ISO disk. Rotational speed is 3000rev/min and average access time is 28ms. It can be supplied with interfacing hardware and software drivers for Apple Mac, PC AT, PS/2 or compatible computers. Other interface options are available. Each unit has two 50-pin SCSI sockets for chaining devices. With the aid of a 64Kbyte buffer, data is transferred over the SCSI-2 link at 4Mbyte/s synchronous or 1.5Mbyte/s asynchronous. Data Peripherals, 0785 57050.

SCSI drives. The CDR1750SY and 1750SZ SCSI drives are for multimedia CD-rom applications. Also available is the CI4000 two, three or four-drive subsystem using the CDR3600 and 3650 built-in CD-rom drives to provide more than 2.2Gbyte of integrated text, graphics and stereo sound storage. It has a built-in power supply, cables, software, and AT or MCA adapter cards. A dip switch lets two subsystems be interlinked side by side or one above the other. Hitachi New Media, 081-849 2092.

Computer peripherals

Infra-red control. An infra-red interface option can be incorporated into custom keyboard designs. It can be used to connect keyboards with computers or host systems for example at a restaurant where the order is taken at a table and beamed to the computer. Output circuitry can be configured to provide PC-AT, PS/2, Apple Mac, DEC VT-220, RS232, RS242, or Ascii protocols. Digitran, 0763 261600.

SCSI adapters. AT and MCA SCSI adapters have been introduced that let the CDR1700S and 320ms 1750S SCSI drives be connected to PCs and Apple Macintoshes. Hitachi New Media, 081-849 2092.

REGULARS

CIRCUIT IDEAS

Electronic balance for differential inputs

A true instrumentation amplifier possesses truly differential input with good common-mode rejection and defined input impedance. Simpler op-amp differential inputs, however, exhibit an input impedance that is signal-dependent, affecting CMRR and output balance. While input impedance of the positive input is constant, the negative input has different input impedances for differential and common-mode inputs. For fully equal resistor values, impedances are:

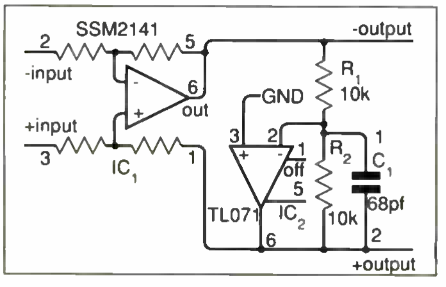
+ve Z_{in} (balanced) 2R
+ve Z_{in} (common-mode) 2R
-ve Z_{in} (balanced) 67R
-ve Z_{in} (common-mode) 2R.

In the "Superbal", invented by Ted Fletcher and myself in 1978, the impedance problem is solved by applying feedback to both inputs of the first op-amp, so that the circuit acts as an instrumentation amplifier, but uses fewer components. Results are

+ve Z_{in} (balanced) R
+ve Z_{in} (common-mode) 2R
-ve Z_{in} (balanced) R
-ve Z_{in} (common-mode) 2R.

Using the new PMI *SSM2141*, input CMRR is in excess of 80dB with no trimming. The tolerances of R_1,R_2 and C_1 affect input impedance but not CMRR.

M Law
Acrone Ltd
Windsor
Berkshire



"Superbal" input stage, with feedback to both inputs to avoid input-impedance dependence on input signal.

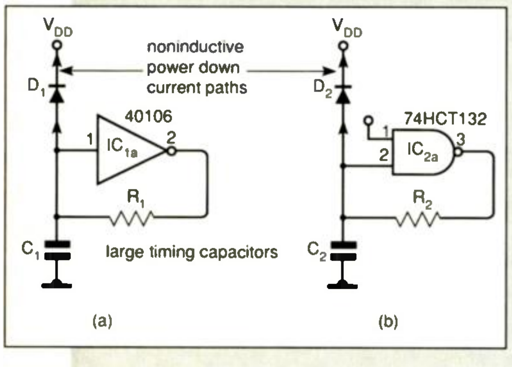
FRESH IDEAS
While we are not short of Circuit Ideas to publish, it would be agreeable to see some fresh input from the vast, untapped bank of talent that our thousands of readers represent. We pay a moderate fee for all ideas published. So send them to Circuit Ideas, Quadrant House,The Quadrant , Sutton, Surrey,SM2 5AS.
We will be happy to consider them.

Diode protection for cmos

Low-frequency oscillators using cmos logic gates commonly need a large timing capacitor and resistor. As a result, on switch-off, an excess voltage can exist on the input terminal, although it has no effect during operation. The oscillators shown in the diagram incorporate the *CD40106* and *74HCT132*, which contain internal diodes on the input terminal to protect against overvoltage, but these diodes are only capable of passing a limited current. Permanent damage would be the result of too high a current through the diode.

To avoid such damage, diodes D_1 and D_2 are connected externally to increase current handling; low-leakage types must be used to avoid a parallel path to the timing capacitor during normal operation. On switch-off, voltage on the input pin will not exceed the safe rating for the majority of cmos circuits.

Ms Railesha
World Friends Design Group
Tamilnadu
India



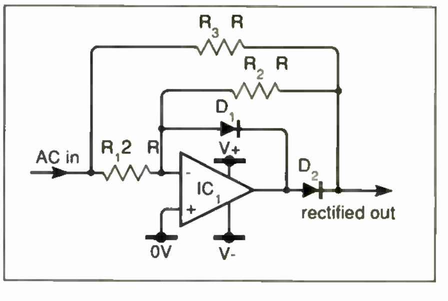
Precision full-wave rectifier

Full-wave rectifiers usually need two op-amps; this circuit uses one.

Negative inputs force D_2 to conduct and the op-amp acts as an inverter with a gain of 0.5 (R_2/R_1). On a positive input, D_2 disconnects the op-amp from the output, which becomes the input multiplied by $R_2/(R_2+R_3)$ – again, half the input.

Disadvantages are the high output impedance (R_2) on positive inputs, and a varying input impedance. Choose the value R so that it is much higher than the source impedance and much lower than the load impedance.

A H Millar
Witney
Oxfordshire



This precision full-wave rectifier uses only one op-amp instead of the usual two.

One-pin interface for an 8051

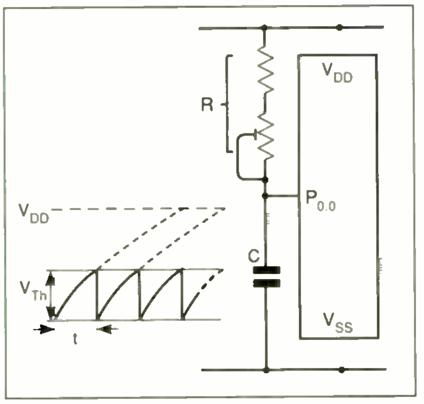
You can interface a variable resistor to a microprocessor using one pin.

An RC network is connected to an i/o-configurable microprocessor port that has either a high-value internal pull-up resistor or none at all. When the port is configured as an output and driven to logic 0, a short delay allows the capacitor to discharge through the port line. If the port is now configured as an input and an internal timer started, the capacitor charges through *R*; when the voltage on the port reaches logic 1, the timer is stopped.

Charge time is $t = CR\log_e[V_{DD}/(V_{DD}-V_{th})]$, so that timer contents are proportional to the value of *R*, assuming that the port takes negligible current, and if the cycle is allowed to repeat there is a sawtooth at the port pin of a frequency proportional to *R*.

A program suitable for the Intel *8051* is given below.

K Kirby
Burnley
Lancashire



The value of R is obtained using only one pin of the microprocessor. The resistor can take the form of a thermistor, constant-current source or any resistive device.

8051 program

```
START: CLR      P0.0         :SET PORT LINE LOW
       MOV      R7,#$40      :SET DELAY TIME TO ≈180µs
DELAY: DJNZ     R7,DELAY     :ALLOW CAPACITOR TIME TO DISCHARGE
       SETB     TCON.6       :START HARDWARE TIMER
       SETB     P0.0         :CONFIGURE PORT AS INPUT (HIGH-Z)
READ:  JNB      P0.0,READ    :LOOP UNTIL INPUT = 1
       CLR      TCON.6       :STOP TIMER
       RTS/JMP START         :EXIT HERE OR LOOP BACK
```

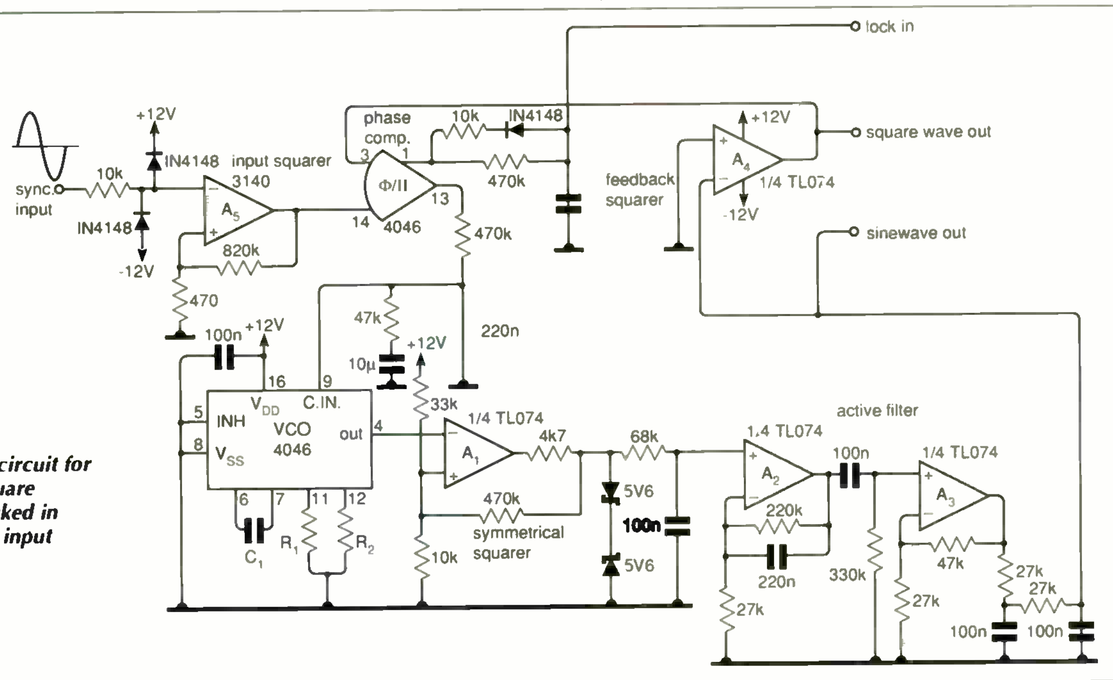
Phase-locked function generator

Three MSI chips will form a synchronous square/sine waveform generator. Sine output is locked to the input signal with no phase error and the square is normally in anti-phase, but the circuit is adaptable to produce zero phase error for this too.

A National Semiconductor *CD4046* VCO chip, together with op-amp A_1, generates a symmetrical square wave at a frequency determined by C_1, R_1 and R_2, values for 50Hz operation being 100nF, 330kΩ and 1MΩ. Active filter A_2/A_3 extracts the fundamental to give the sine output.

Since the filter introduces a phase delay between VCO and sine output, a further squarer, A_4, is interposed in the feedback path to the phase comparator in the *4046* to give zero phase error. "Lock in" going high when lock is achieved. Op-amp A_5, a *3140* bifet type, functions as a squarer for untidy input sync signals.

Hernán Tacca
University of Buenos Aires
Argentina



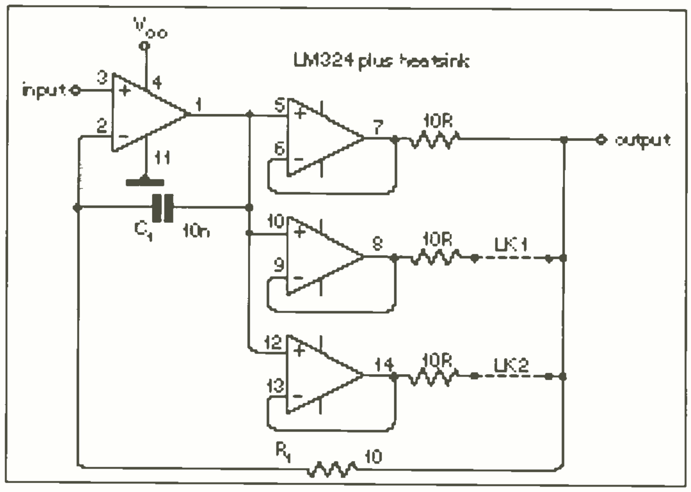
Three-chip circuit for sine and square outputs, locked in phase to an input signal.

85mA op-amp output

Output current from op-amps is commonly between 20 and 40 mA. In this *LM324* quad op-amp circuit, a parallel connection of three amplifiers gives up to 85mA and retains short-circuit protection.

This is a unity-gain circuit providing a bandwidth of 200kHz, R_1 and C_1 taking care of loop stability. Current-sharing resistors of 10Ω avoid the effect of inherent differing input offsets, which would otherwise cause different output currents from each op-amp. For long-term, high output current, a bonded heat sink will probably be needed.

A M Wilkes
Brentwood
Essex



This parallel connection of the op-amps in one package will give up to 85mA output current. Bandwidth of this circuit is 200kHz at unity gain.

Eight-bit data sender with no micro

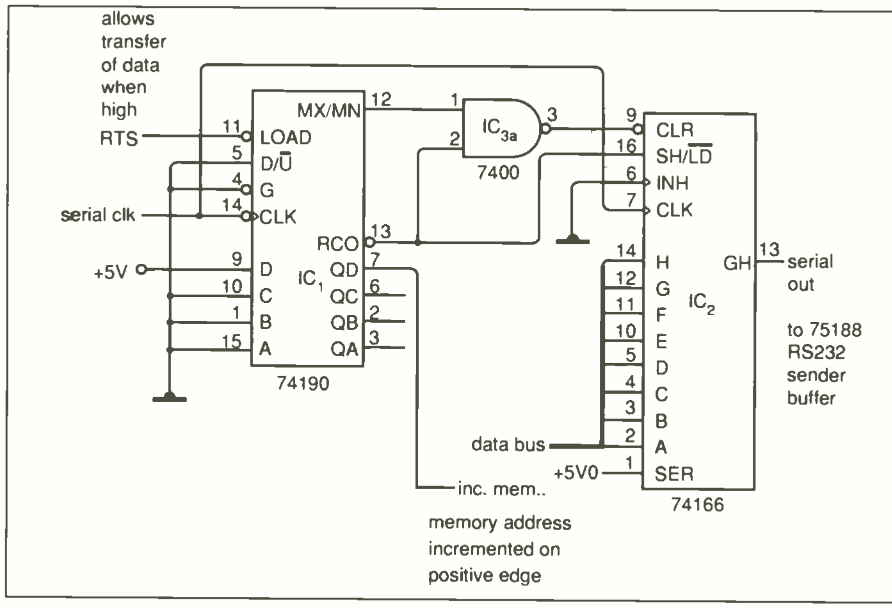
Transferring parallel data from a unit that uses no microprocessor to the *RS-232C* port of a PC in serial mode requires a little trickery, interface circuits such as the *8251* not being of much help. I needed to pass data from an external system's memories to a PC.

A *74190* up/down counter and a *74166* parallel-in/serial-out shift register, with a quarter *7400* Nand, will do the job, converting parallel data to serial 8 bits plus a stop bit, although there can be no handshake between transmitter and receiver.

I have successfully built the circuit using TTL, LS and AS devices, but have had no such luck with HC types.

Arash Ayel
Tehran
Iran

Simple circuit for transference of data to a PC from a unit with no microprocessor on board.



Guard the vegetables without frying the cat

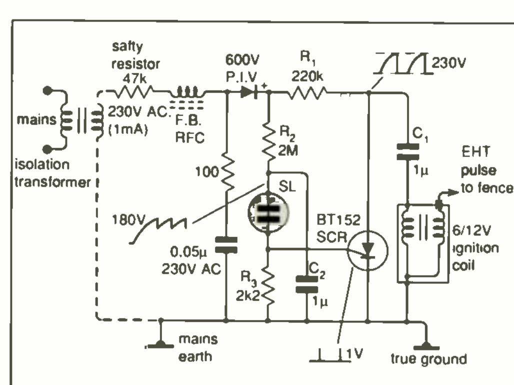
This electric fence generator is designed to keep out the squirrels without resorting to excessive violence.

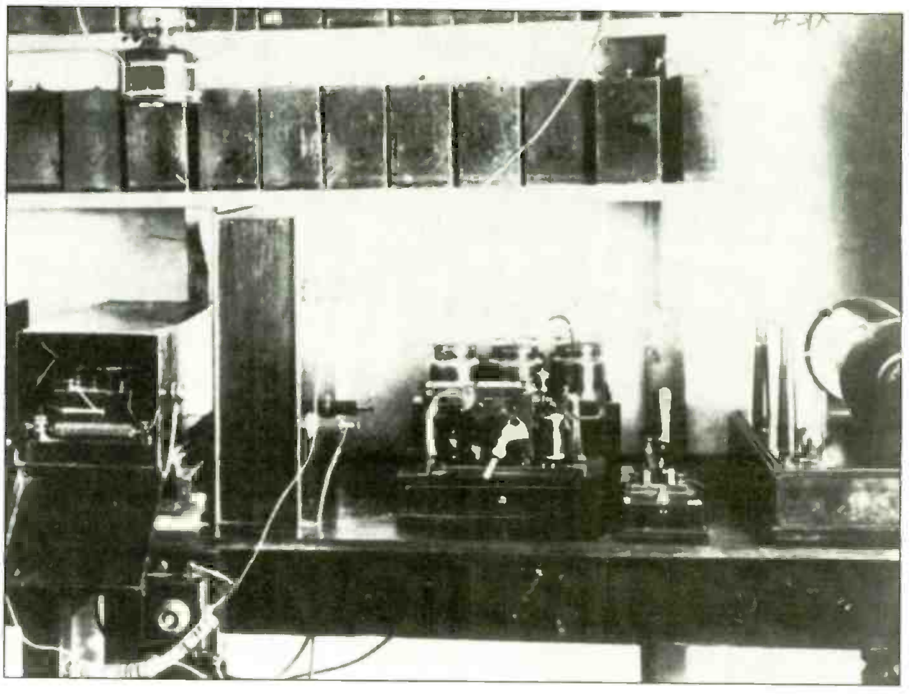
Capacitor C_1 charges through the ignition coil primary and R_1 in around 250ms, C_2 charging through R_2 in a longer time. Gas discharge tube *SL* strikes at 180V, develops a voltage across R_3 and turns the SCR on. This discharges C_1 through the coil primary and the SCR goes off.

In the original circuit, only mains live and earth were used, since current is tiny. It is possible that this may cause tripping of an ELCB and an isolating transformer might be better, as well as offering safer operation – a 47kΩ resistor is used instead of a fuse to limit current to a safe value. The ferrite bead, 100Ω resistor and 50nF capacitor are for RF suppression, the capacitor possibly being taken from the same source as the discharge tube – a fluorescent-lamp starter. Capacitors C_1 and C_2 should be rated for AC or 600V DC.

J E Cronk
Prestatyn
North Wales

Generator for electric fences uses salvaged components and will leave the rabbits relatively intact.





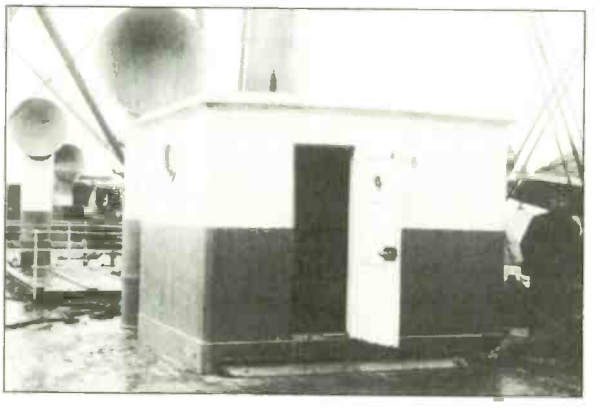
Interior at Holyhead, one of Marconi's first shore stations. The coherer (receiver) in a screened box is on the left; the ink writer and morse key in the centre, with Leyden jars behind, and on the far right the induction coil (spark generator). The shelves above carry rows of accumulator batteries for power.

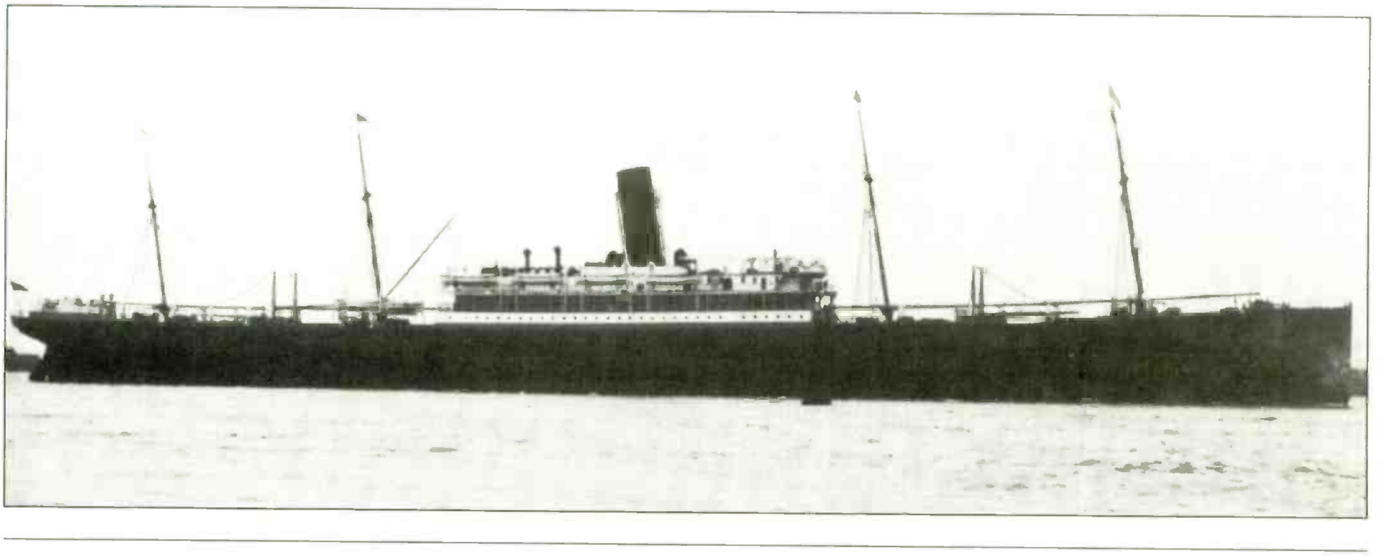
Wireless at sea and the Titanic disaster

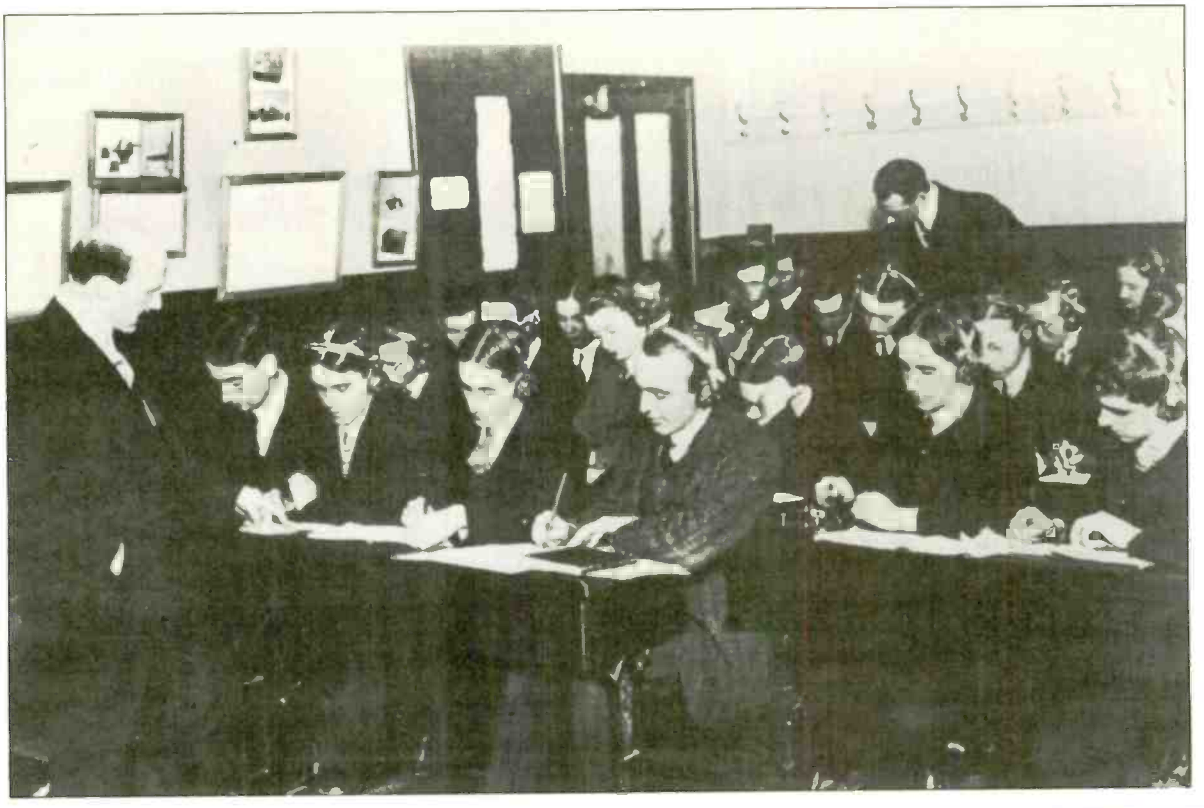
One of Marconi's primary intentions in developing wireless telegraphy was to end the isolation of ships at sea. His first commercially active company, founded in 1900, was the Marconi International Marine Communication Company, and the first Marconi-equipped vessel, the German transatlantic liner Kaiser Wilhelm der Grosse, sailed on February 28, 1900. By the end of the year, the company's seven coastal stations were being built, and by the close of 1902, seventy ships had been equipped with wireless.

Shipboard wireless installations were leased from Marconi as part of a service. The service also included wireless officers who were all Marconi employees – a stratagem necessary to circumvent the British Post Office's

By the end of 1902, seventy ships had been equipped with wireless, including the SS Minneapolis, below. Its deck-housed Marconi cabin is shown right.







Training school for Wireless operators 1912 (94893)

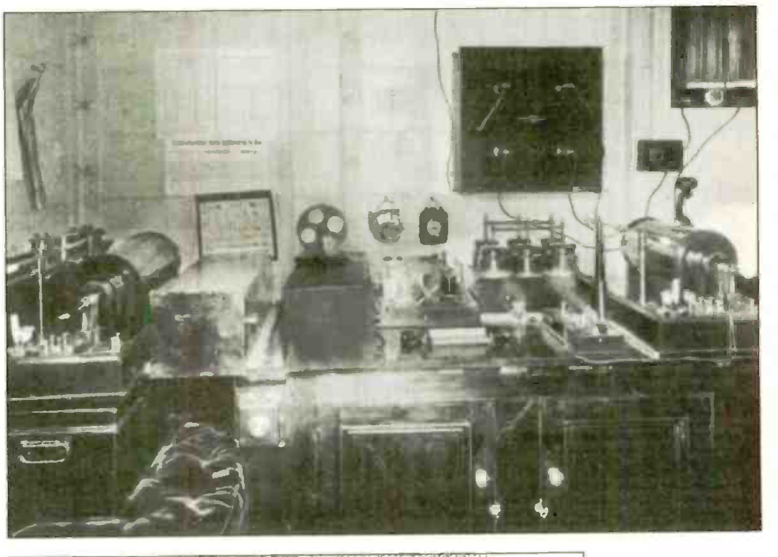
Marconi provided ships' wireless operators as well as the installations. Training became a major part of the company's activities and several training schools were set up for operators. This photo, believed to be from Liverpool, dates from 1912.

monopoly on paid messages. Several training schools were set up for operators.

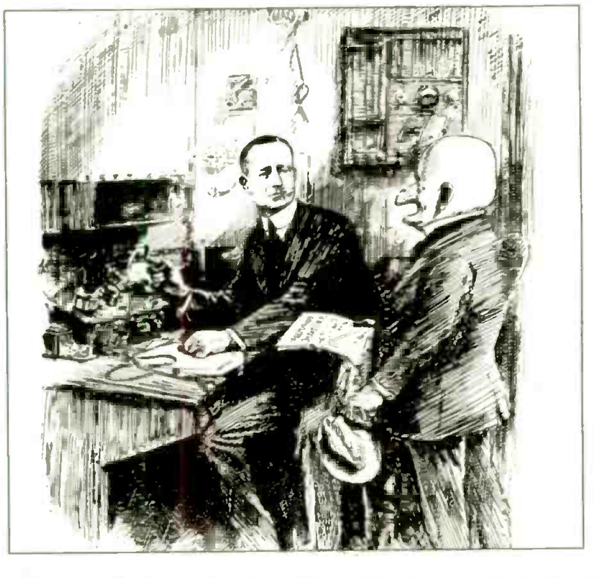
Soon the use of ships' wireless spread rapidly. The 712 survivors of the Titanic disaster in 1912 owed their lives to it – though the loss of 1517 souls could to some extent be blamed on shortcomings in operating practices at the time. The nearest ship, within sight of the Titanic's lights all that night, failed to respond to wireless distress calls because her sole operator was asleep. Then, when rescue attempts eventually got underway, they were hampered through uncontrolled use of wavebands by well-meaning amateurs.

The resultant inquiry and an international conference led to international regulations which made wireless mandatory for all ships above a certain size, and stipulated more secure procedures. These included alarm systems, and continuous watch-keeping - if necessary by other than the Marconi-employed radio officers - and reserved emergency wavebands.

Use of wireless to report icebergs, and weather in general, was also increased as a result of the disaster.



Inside the Minneapolis' Marconi cabin. The equipment is much as at Holyhead, above, but doubled-up, as a fail-safe measure. Two induction coils, for instance, can be seen, one on either side, with two coherer boxes on the left. On the wall is a jigger (transformer).



The successful rescue of passengers and crew from the burning liner Volturno in the year following the Titanic disaster made a great impression on the public and was commemorated in this famous Punch cartoon.

Stabilising the mains with ferro-resonant technology

Microprocessor-based computer systems are very sensitive to power line disturbances. In almost every location, there is some form of power line irregularity; ferro-resonant devices can solve this problem. By Frantisek Michele.

The ferro-resonant transformer has been around for years. Although this device has a number of characteristics that give it the potential for being an excellent power conditioner, it also has a number of characteristics that limit its application, especially for computer use.

However, it is possible to overcome these limitations and create a power conditioner that is suitable for a wide variety of microcomputer and other applications involving sensitive equipment.

The easiest way to describe a ferro-resonant transformer's operation is to compare it to an ordinary power transformer (**Fig. 1**). Applying voltage to the primary of transformer sets up a magnetising current that generates flux lines that link to the secondary which develop a voltage because of mutual inductance. The secondary voltage only remains constant if the flux and the primary current stay constant. The output voltage is therefore determined by the flux density, the primary current and the turns ratio.

If a typical transformer operates at a high enough primary current, its core becomes saturated with flux lines. Increasing the primary current will not then increase the secondary voltage. Consequently, operating an ordinary power transformer in saturation will create a voltage regulator, though such operation is impractical because primary saturation current is very close to a short circuit. Normal current in the I_1 - I_2 region shown in **Fig. 2** causes a linear change in flux, but once the current reaches I_4 - I_5 saturation region, the resulting flux changes are small. To the left of the point I_3, flux changes are in direct proportion to primary current; to the right of the I_3, the curve becomes non-linear and changes in current have less effect on flux.

The ferro-resonant transformer, on the other hand, is designed to operate in saturation (**Fig. 3**). However, since it is the secondary coil that operates in saturation, not the primary, more flux must be produced in the secondary core leg than in the primary. The core structure is modified by the addition of a magnetic shunt to loosen the coupling between primary and secondary. Because of the air gap in the shunt, the core section has a high reluctance and the main path for magnetising flux is through the outer core. As the input voltage increases, the magnetising flux through the core section increases, and with it, the inductance of the secondary winding. The addition of an output capacitor alters this. Once the reactance of the winding equals that of the capacitor, the two resonate, producing a higher output than the turns ratio voltage alone. This effect is similar to a series resonant circuit in that controlling the point of resonance increases the voltage across the capacitor substantially above the impressed voltage.

The output waveform of a basic ferro-resonant transformer looks like a square wave and is suitable for many loads, but it does not satisfactorily provide power for computer installations and their electronic loads without the addition of a harmonic filter choke (**Fig. 4.**). With this filter, a large part of the output harmonic content is cancelled, producing a sine wave voltage that meets the requirements of microprocessor based equipment. When shopping for a line conditioner regulator, consider performance price, and reliability. A properly designed conditioner will regulate the output voltage to ±2% or ±3%. With the input varying as much as ±20%, the output distortion should be no greater than 5% or 6% total harmonic distortion.

One of the advantages of ferro-resonant transformers is their ability to attenuate normal mode noise voltage transients. This attenuation is up to 10 times more than con-

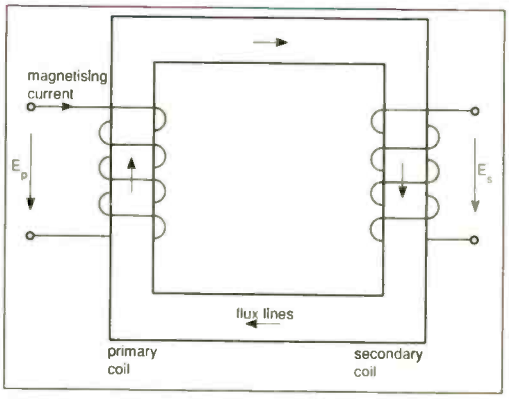


Fig. 1. In a conventional transformer, flux lines link the primary to the secondary; a voltage develops through mutual inductance.

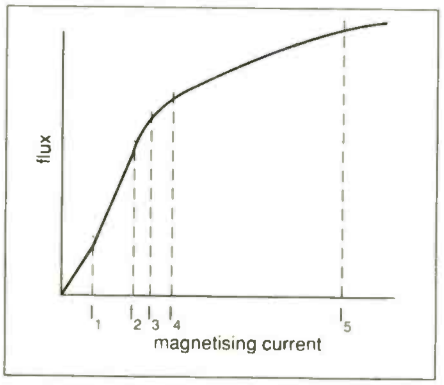


Fig. 2. Normal current between I_1 and I_2 causes a linear change in flux. A transformer has to operate in the saturation region I_4-I_5 to regulate voltages.

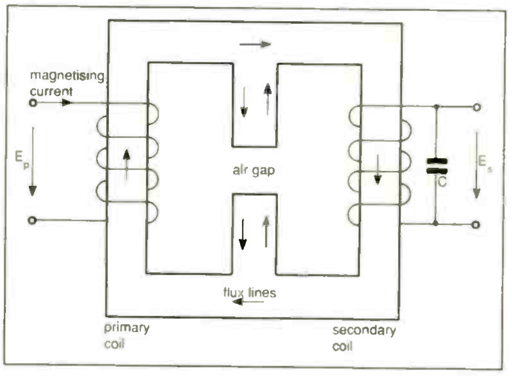


Fig. 3. A capacitor in parallel with output and a gapped magnetic shunt between the two cores improves transformer design.

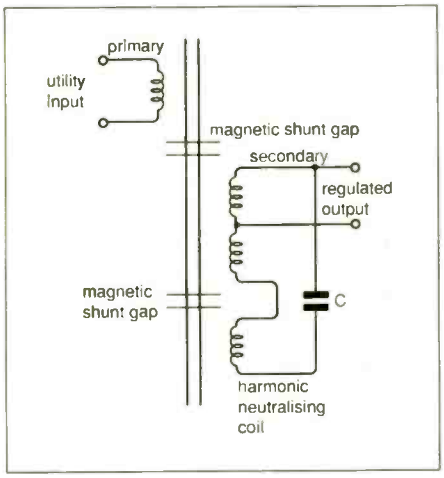


Fig. 4. Adding a harmonic neutralising coil reduces the transformer's distortion to 3-5%

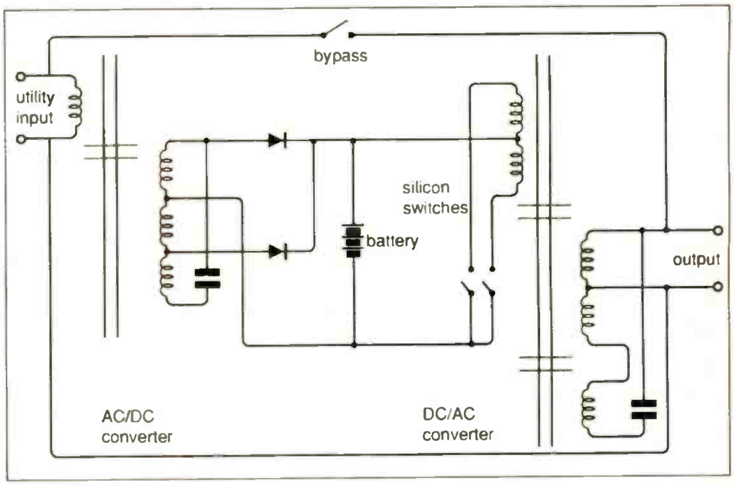


Fig. 5. Transformers in UPS provide a high degree of lightning immunity.

ventional tap changer regulators provide. Since the secondary winding operates in saturation, transients and spikes are clipped.

At 80dB, a transient with a peak of 10,000V will only generate 1V on the output. Ideally, 120dB of common mode noise protection should be available, which is noise common to both line and neutral and generated between those to lines and ground. Most of this type of noise can be eliminated by using proper grounding techniques. Note that the ferro-resonant transformer is a tuned circuit, frequency sensitive. Typically, a 1% change in frequency produces a 1.5% change in output voltage.

On the other hand, a ferro-resonant transformer has some very desirable overload characteristics. If the output is short circuited, the current increases by only about 80%. A well designed ferro-resonant transformer can maintain a short circuit indefinitely.

Line conditioners using amplifiers and feedback networks must add circuitry to protect the output from over-voltage failure modes. Most voltage regulators provide little normal mode noise rejection, so a ferro-resonant line conditioner is likely to be the best solution for severe power line disturbance conditions where common mode noise rejection, normal mode noise rejection and output voltage regulation are all required.

Using a ferro-resonant transformer in the AC/DC conversion process provides many distinct advantages. Because its output, minus the filter choke, is squarewave, fewer filter capacitors are required after rectification. When converting an AC wave to a DC level, the DC is much easier to filter if the AC is a square wave instead of a sine wave. Since current flows through the diode rectifier at the peak of the cycle, the diode heating is also reduced.

The ferro-resonant transformer also has some important advantages in the front end stage of uninterruptible power systems (UPS). For example, when a battery is placed on the DC output, the only semiconductors used are the diode rectifiers. All the voltage regulation and the current limitation are designed in and accomplished at the ferro-resonant transformer. Because of this low parts count, the MTBF is quite high, typically 250,000 hours or more. More important, the incorporated battery cannot be overcharged. In most cases, the battery is likely to be the most expensive part in the DC front end of the UPS. Another consideration is that with a ferro-resonant transformer, the harmonic feedback (noise coupled back into the utility power line) is quite low. Typically, only about 3% total harmonic distortion is fed back into the power line. This compares with anything from 10 to 30% harmonic feedback using phase controlled SCR type front ends. This feedback may affect other equipment operating on the same utility power line.

The ferro front end stage has a drawback: efficiency is usually 88-90%. However, the advantages far outweigh the disadvantages. In its most basic form, an UPS consists of three elements: the rectifier/charger, the battery, and the inverter. A UPS containing these elements is a true online continuous run system (**Fig. 5**). ■

Uninterrupted benefits

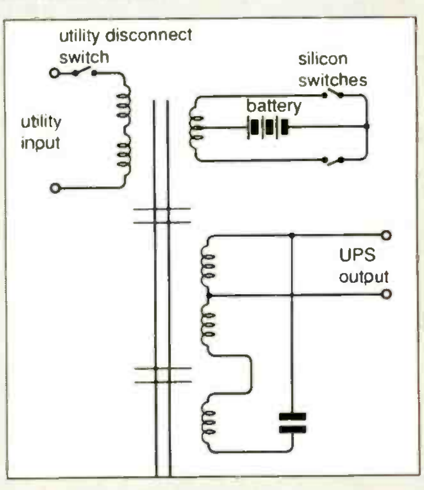
The ferro-resonant transformer has become extremely popular for UPS systems. The active parts count is quite low, as it is in the DC/AC inverter. The ferro-resonant transformer's ability to regulate voltage means that feedback loops are not necessary in the inverter.

Because of the transformer's inherent current limit, output current sensing is not required either. As a result, the only control circuitry required is the oscillator that turns the silicon switches on and off. The oscillator operates at the line frequency, which in turn controls the flow of battery current through the silicon switches and into the primary of the ferro-resonant inverter transformer.

The square voltage waveform that is generated is filtered into a low distortion sine wave by the inverter transformer. This type of UPS design has long been a proven workhorse for the UPS industry. The 90% efficiency UPS design has become popular over the last few years not only for its high efficiency, but because of its reduced size and weight (**Fig. 6**). In this design, the utility operates the primary of the ferro-resonant transformer through a switch. At this point, the inverter which drives another primary winding is off.

The instant the utility is sensed to be out of specification, the utility switch opens and the inverter is started in phase. It takes approximately 10ms to accomplish this. During that time, the energy storage filter capacitor supplies current to the load. If the utility returns within spec before the battery is fully discharged, the control circuit locks onto the utility phase and transfer takes place with the utility switch closing and the inverter simultaneously turning off. With this technique, the input to output efficiency of the UPS ferro-resonant transformer is approximately 90%.

This technique also provides all the filtering advantage described earlier because the ferro-resonant transformer acts as a line conditioner in the normal mode. Again, simplicity plays a major part in this technique, with no need to incorporate complicated voltage and current feedback networking. Because of the reduced parts count on all the ferro-resonant techniques, this type of design is one of the most reliable.



GOING BEHIND BARS

Bars are all around us, from supermarket check-outs to security systems. Nic Burkinshaw looks behind the bars to decode barcodes.

Barcodes have a number of obvious advantages for data recording, with two of the biggest being fast data entry and security.

To give an idea of speed, a 12 character code can be located and read in under 2s, while, for security, barcodes can be printed using infra-red reflective ink (appearing black in white light) on a black background to avoid duplication by photocopiers.

Barcodes used in security entry systems avoid the possibility of accidental erasure of the code and do not suffer wear of head and card, unlike magstripe readers which need the read head to be spring-loaded onto the card. Swipe barcode readers are able to read across an air-gap, having a focal length of 2-4mm. Also when a barcode is read characters cannot be transposed or missed – 0s and Os, 1s and Is are not confused – and the data can be quickly recognised when inverted, at an angle, in reverse and at a distance.

Not to be forgotten at the practical level, barcodes can be covered in grease and grime and still be read (using infra red illumination).

Four main types of code

There are many ways to encode data using bars and spaces, but there are only four main types currently in use: Code39, EAN, Interleaved 2 of 5 and Codabar.

Code39, sometimes called 3 of 9, is found everywhere – with the exception of retailing – and can represent the upper case alphabet, digits 0-9 and eight special characters. It is most commonly seen as a stock or serial number on electrical items and automotive parts.

The code is two level, meaning that the bars and spaces can only be narrow or wide, and the ratio of narrow to wide is nominally 1:2.5.

Each character is represented by nine elements of five bars and four spaces. Three of these nine elements are wide; wide bars or spaces are equal to a binary 1 and narrow are equal to binary 0.

There is a narrow space between each character.

Although there are 512 combinations of nine binary bits, only 44 combinations are valid - so the code is inherently self-checking.

Code39 is the most widely used barcode – except for retailing.

0123456789

For extra security a check character can be added to each message, thecheck-sum calculated by adding the check values of each character in the message and then dividing by 43 to give a remainder. Extended Code39 is an extra complication of the code, using certain characters to start a two character sequence allowing representation of the full ascii code set, including control codes. For example carriage return is $M.

Table 1 shows the binary code for each character and its check character value. Note that '*' has no check value because it is used to indicate the start and end of all Code39 messages.

To code the message 98PQ, with the check-sum, first sum the check-sum values of all characters in the message, 9 8 P Q (9 + 8 + 25 + 26 = 68). Divide the result by 43 (68/43) giving 1 remainder 25, then look up the character that has a check-sum value of 25 – the letter P. So, the message to code, including check-sum and start and stop characters is :

98PQP
0100101000001100100010010010000010
1 0 0 1 0 0 0 0 0 0 0 1 1 1 0 0 1 0 0 1 0
100

Table 1. Code39 character set

Character	Binary word	Check-sum
0	000110100	0
1	100100001	1
2	001100001	2
3	101100000	3
4	000110001	4
5	100110000	5
6	001110000	6
7	000100101	7
8	100100100	8
9	001100100	9
A	100001001	10
B	001001001	11
C	101001000	12
D	000011001	13
E	100011000	14
F	001011000	15
G	000001101	16
H	100001100	17
I	001001100	18
J	000011100	19
K	100000011	20
L	001000011	21
M	101000010	22
N	000010011	23
O	100010010	24
P	001010010	25
Q	000000111	26
R	100000110	27
S	001000110	28
T	000010110	29
U	110000001	30
V	011000001	31
W	111000000	32
X	010010001	33
Y	110010000	34
Z	011010000	35
-	010000101	36
.	110000100	37
SPACE	011000100	38
*	010010100	
$	010101000	39
/	010100010	40
+	010001010	41
%	000101010	42

Note that each character of the message is made up of nine elements and that characters are separated by a narrow space (0).

European code

The EAN (European article number) barcode comes in several styles to provide for stock codes of five and ten digits and a two or five digit supplement. Only digits 0-9 are represented, and being a four level code, each bar or space can be one, two, three or four elements wide. Bars represent binary 1 while spaces represent binary 0.

EAN8 provides for a code length of five digits and...

Every character is made up from a 7-bit word and all codes have start, centre and end guard bars. These sequences of narrow bars enable determination of nominal narrow bar width across each code. Characters to the left of the centre guard bars are encoded using either of the left hand columns of **Table 2**, those to the right use the right hand column. The difference between the two left hand columns is that A is encoded with odd parity and B with even parity.

Note that 00011 would be represented by a space three elements wide followed by a bar two elements wide.

EAN8 provides for a code length of five digits and EAN13 for ten. Each has start, middle and end guard bars, two flag characters and may also have a supplemental two or five digit code.

EAN8 barcodes have left hand guard bars, encoded as 101, two flag characters, encoded as left hand A, and first two data characters, encoded as left hand A. Centre guard bars are encoded as 01010. Last three data characters are encoded as right hand. Check character is encoded as right hand, and right hand guard bars are encoded as 101.

Table 2. EAN character set

Number	Left Hand A	Left Hand B	Right Hand
0	0001101	0100111	1110010
1	0011001	0110011	1100110
2	0010011	0011011	1101100
3	0111101	0100001	1000010
4	0100011	0011101	1011100
5	0110001	0111001	1001110
6	0101111	0000101	1010000
7	0111011	0010001	1000100
8	0110111	0001001	1001000
9	0001011	0010111	1110100

EAN13 barcode has left hand guard bars-encoded as 101 and a second flag character, encoded as left hand A or B. The first five data characters are encoded as left hand A or B. Centre guard bars are encoded as 01010 and the last five data characters are encoded

Table 3. Code for first flag character in EAN13

No.	Flag 2	Data 1	Data 2	Data 3	Data 4	Data 5
0	A	A	B	B	A	B
3	A	A	B	B	B	A
4	A	B	A	A	B	B
5	A	B	B	A	A	B
6	A	B	B	B	A	A
7	A	B	A	B	A	B
8	A	B	A	B	B	A
9	A	B	B	A	B	A

Printing barcodes

Every barcode is made up of the same components: a blank area of light colour (quiet zone); a set of bars and spaces that make up the data, and another quiet zone. Recommended width for the quiet zone is >10 x narrow bar width.

Currently, the practical minimum width for a bar or space used in any code is 0.13mm. The ratio of wide to narrow for two level codes is at least 2:1, more usually 2.5:1. Four level codes have bars and spaces that are simply 1, 2, 3 or 4 narrow units wide.

Care must be taken when printing barcodes, since ink spreading through the paper or faint lines in what should be a solid bar can produce a useless barcode.

Carbon-based inks give the best contrast between bars and spaces for both visible and infra-red readers. When dye-based inks have to be used, eg in the food industry, problems can be avoided by not using infra-red readers.

Barcodes may be printed in a variety of sizes, so there are a range of sensitivities of reader. Obviously, if the sensitivity (active area) of the reader is closer to a wide bar width than narrow then misreads will occur. For a barcode wand, there may be a choice of low, general purpose or high resolution referring to nominal narrow bar widths of 0.33mm, 0.19mm or 0.13mm.

Table 4. EAN 2 digit supplement parity pattern

A - A	A - B	B - A	B - B
00	01	02	03
04	05	06	07
08	09	10	11
12	13	14	15
16	17	18	19
20	21	22	23
24	25	26	27
28	29	30	31
32	33	34	35
36	37	38	39
40	41	42	43
44	45	46	47
48	49	50	51
52	53	54	55
56	57	58	59
60	61	62	63
64	65	66	67
68	69	70	71
72	73	74	75
76	77	78	79
80	81	82	83
84	85	86	87
88	89	90	91
92	93	94	95
96	97	98	99

as right hand. Check character is encoded as right hand, and right hand guard bars are encoded as 101.

The first flag character of an EAN13 code is encoded using the parity pattern of the second flag character and the first five data characters (**Table 3**).

Binary representation of an EAN 8 barcode of 80123453 would be:

10101101110001101001100100100110100 1 0 1 0 0 0 0 1 0 1 0 1 1 1 0 0 1 0 0 1 1 1 01000010101

The check character can be created by supposing that the right-most character is odd, adding all characters in odd positions and multiplying the result by 3. Then all the characters in even positions must be added together, and that total summed with the "odds" calculation.

The check character is the smallest number that, when added to the total, results in a multiple of ten.

The barcode on the front of every issue of *EW + WW* is one example of this coding.

Flag characters are 97 and the message characters are 7095983300. So characters to check are 9 7 7 0 9 5 9 8 3 3 0 0. Positioning (even/odd) is E O E O E O E O E O E O so the sum of all odds multiplied by 3 is 69 ((7 + 0 + 5 + 8 + 3 + 0) x 3).The sum of all evens is 37 (9 + 7 + 9 + 9 + 3 + 0): added to the above this gives a total of 106. Four added to 106 gives 110 as a multiple of 10. So the check character is 4, giving a full message of 9770959833004.

0 123456 789012

...EAN13 allows ten digits

The barcode on the front cover also features a two digit supplement indicating the month number starting from 01 for January. The supplement is made up from guard bars encoded as 1011; first data character encoded as left hand A or B; character delineator encoded as 01, and second data character encoded as left hand A or B. The data characters are encoded using either of the left hand columns, according to the digits that are coded. (For example if the supplement is 13 then, referring to **Table 4**, the left hand A column is used for 1, and 3 is encoded from the left hand B column).

Five digit supplements are seen most often on books, as a machine readable version of the selling price. In a five digit supplement, guard bars are encoded as 1011, the first data character is encoded as left hand A or B and the character delineator is encoded as 1. Second data character is encoded as left hand A or B and the character delineator as 01; the third data character is left hand A or B and the character delineator,1; fourth data character is left hand A or B and the character delineator, 01. Fifth data character is encoded as left hand A or B.

Table 5. EAN five digit supplement parity pattern

No.	Data1	Data 2	Data 3	Data 4	Data 5
0	B	B	A	A	A
1	B	A	B	A	A
2	B	A	A	B	A
3	B	A	A	A	B
4	A	B	B	A	A
5	A	A	B	B	A
6	A	A	A	B	B
7	A	B	A	B	A
8	A	B	A	A	B
9	A	A	B	A	B

Once again, the characters are encoded using the left hand columns – the column to be used is decided from a check-sum arrangement similar to the check character of the main message. Assuming that the right most character is odd, then all of the characters in odd positions are added and the result multiplied by 3. All of the characters in even positions are added and the result is multiplied by 9. The two totals are then added. (The units digit of the result is the number of the parity pattern in **Table 5**). For example, in the five digit supplement

Table 6. Interleaved 2 of 5 code character set

ASCII	binary word
1	10001
2	01001
3	11000
4	00101
5	10100
6	01100
7	00011
8	10010
9	01010
0	00110

International equivalents UPC/EAN/JAN

There is another group of codes similar to Code39 called UPC (universal product code) and EAN/JAN (European/Japan article number). UPC was developed first in the USA; the equivalent specifications in Europe and Japan are EAN and JAN, which are the ones seen on magazines, books, and every item in the supermarket.

To ensure that different items are not printed with the same barcode, companies must apply for a unique number to their Article Number Association (ANA) in their country.

UPC A is a 12 digit code split further by the first digit into :

0, basic codes, no specific use; 2, random weight items, marked in-store; 3, National Health items; 4, to indicate non-food items, and 5, used on coupons.

UPC E is a six digit code, used for marking small items.

EAN/JAN13 is a 13-digit code where the first two characters define the country of origin, eg 50 = U.K.

EAN/JAN8 is an eight-digit code for small items. When used on books and periodicals, the first two characters of the code are set to 97, regardless of country of origin, because the ISSN classification was developed before UPC/EAN/JAN.

12345, position (even/odd) is O E O E O, sum of all the odds x 3 is 27, and sum of all the evens x 9 = 54. Adding together both sums gives 81, so the number of parity pattern is units digit, 1.

Code for packaging

Interleaved 2 of 5 is used for coding transit packaging, such as Royal Mail Parcel's Trakback labels. It is also the same code that appears in *Radio Times* and is being used by Panasonic to allow setting of their VCRs for recording films.

The code is numeric only (**Table 6**), and two level, so that both bars and spaces in between are significant; each bar and space can only be narrow or wide. The wide to narrow ratio is between 2 and 3 to 1.

Characters are represented by two wide elements out of a total of five, and narrow bars and spaces are recognised as binary 0; wide as binary 1.

A bar/space pattern of 0000 starts the code and a pattern of 100 ends it. The message contained between these start and stop codes is interleaved, so that the first character is encoded as the five bars following the start code and the second character is encoded in the spaces.

Interleaved 2 of 5 is high density, due to the small number of elements per character. The fact that characters are interleaved also means that separators are not required (the code is said to be "continuous"). Characters are self-checking in that they must consist of 2 wide and 3 narrow elements.

The code has an optional modulus 10 check-sum character. For the example message of 57654823 the check-sum is calculated (similar to above) by assuming the right-hand-most character is even so the sum of the odd characters is 17. Summing the even characters and multiplying by 3 gives 69, and a total for both calculations of 86.The check-sum is 4 – the smallest number which added to the total results in a multiple of 10 (86 + 4 = 90).

So the message with check character is 576548234. However, because the characters are coded in pairs a non-significant leading zero must be added to leave an even number of characters in the message; the message to be coded is 0576548234.

To code the message 2345, with no check-sum, take the first pair of characters, 23. Code for 2 is 01001 and for 3 is 11000. Interleave these to give 0111000010.

For the second pair the code for 4 is 00101 and for 5 is 10100. Interleaving these gives 0100110010. Adding start code 0000 and stop code 100, gives:

000001110000100100110010100

Codabar

Codabar is a two level numeric code with six special characters and a choice of four stop/start characters. There are seven elements in each character (**Table 7**) with only two or three wide elements. Each is separated from the next by a narrow space. Binary 1 is encoded as a wide bar or space and 0 as narrow.

Table 7. Codabar character set

ASCII	binary word
0	0000011
1	0000110
2	0001001
3	1100000
4	0010010
5	1000010
6	0100001
7	0100100
8	0110000
9	1001000
-	0001100
$	0011000
:	1000101
/	1010001
.	1010100
+	0011010
A	0011010
B	0101001
C	0001011
D	0001110

Having only 20 valid combinations out of a possible 128 makes this code inherently self-checking and there is no provision for a check-sum.

The message can be coded with any of the four start and stop characters (A, B, C or D), so for example 2345 with A as the start/stop character (A2345A) is coded as :

0011010000010010110000000010010010
0001000011010

ABC Codabar is also known as NW7 and was probably the first barcode to be widely used. ABC is an acronym for American Blood Commission and the code is the internationally accepted standard for barcoding in the blood transfusion service and is mostly used in the medical field.

1234567890

Interleaved 2 of 5 is often found on transit packaging, and also in the Radio Times.

01234567

Codabar allows only 20 valid combinations out of a possible 128, so is self-checking.

Choosing the appropriate code

Choice of code is usually constrained by what is already in use for the particular application.

If the application is new or unique then the codes to consider should really be Code39 for alphanumeric or Interleaved 2 of 5 for purely numeric data.

Interleaved 2 of 5 also gives the highest code density. Both are two level codes allowing a greater variation in size and print quality than four level codes such as EAN. Both are inherently self-checking, by virtue of having few valid combinations from a large set of possibles, and can also have a check-sum added.

Disadvantages are that Code39 is a long code - each character consists of nine elements - and that data for Interleaved 2 of 5 must have an even number of characters.

Hardware

Barcode readers, like those used at supermarket check-outs, use oscillating visible red laser beams to cover the surface of a package with a wide angle scan pattern of approximately 40 lines at various angles rapidly repeated. The optics allow a depth of field of around 30cm and these features enable rapid reading of barcodes on all sorts of packages, at any orientation, without contact.

Contact CCD scanners, now seen in most high street shops, are read by flooding the barcode with light from a strip of visible red leds and detecting the bar-space pattern with a charge coupled line array sensor. Although termed "contact" these readers can recognise a barcode at a distance of up to 1cm, enabling the reading of codes through the clear plastic of cassettes and CD cases.

There are also laser scanners available in a pistol-type design to read barcodes at a distance (less than 200cm). These scan horizontally using a rotating polygon of mirrors to deflect the beam, and rely on the user to align correctly across the barcode.

Wand type readers rely on the user to scan the code and are used either on the basis of least cost or lowest power requirement. Most wands use a broad field emitter and a focused detector, but for even lower power consumption some swap this around and use a focused emitter and a wide area detector.

Wands can also create problems; scanners provide a fast, repetitive and constant speed data stream, while wand output is subject to variations such as the user moving the wand across the barcode in an arc and changes in speed due to the flick-of-the-wrist action. ■

DESIGN

Oscillator tails off lamely?

Ian Hickman looks at how a long-tailed transistor pair circuit can be used in conjunction with switching action to produce an effective oscillator

Transistor sinewave LC oscillators tend to exhibit a worse waveform than their valve forebears. The problem is particularly marked with single transistor versus single valve circuits for a number of interesting reasons.

On the other hand, it has long been known that a very pure sinewave output can be obtained if one goes to the expense (not too serious nowadays) of using two transistors in a symmetrical arrangement. One of the first applications of this scheme appeared in a *Wireless World* article many years ago. A dredge through the cuttings file unearthed a host of interesting articles; the article I sought was one on a self-balancing push-pull circuit for use as an erase bias oscillator in a tape recorder.

Its great virtue was its low level of even harmonic distortion, an important point to consider for use in a tape recorder design. In this application, due to the non-linear magnetisation characteristic of the recording medium, even order harmonics can result in different levels of residual magnetisation on opposite half cycles of the bias or erase drive. This represents a residual DC component of magnetisation on the tape, with its attendant increase in no-signal noise level.

The circuit described itself as a class D (current-switching) oscillator and was based upon a long-tailed pair whose bases, driven by a feedback winding, steered the fixed tail current through each transistor alternately to one end or other of the centre-tapped 100kHz tuned tank circuits.

By setting the tail current to a value appropriate to the loaded Q of the tank circuit, the transistors (I used GET116s) operated as pure switches without bottoming at the collectors. The result was a bias/erase oscillator with very little distortion; what there was entirely odd harmonic.

Since then, many push-pull oscillator circuits based upon the long-tailed pair have become popular, for both AF and RF applications. A good example of the latter is the Vakar oscillator popular with RF designers.

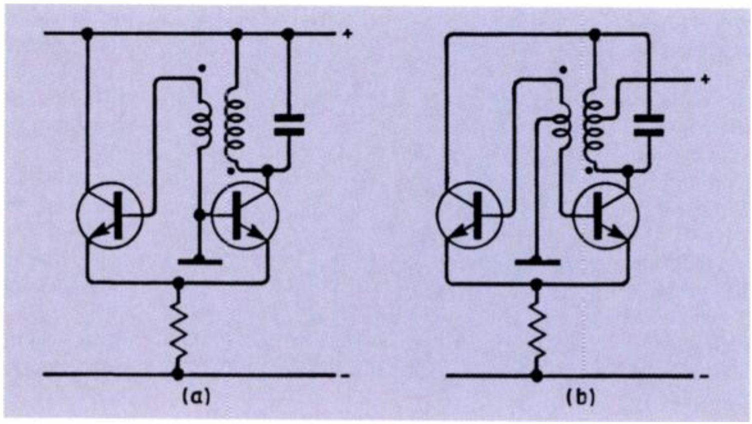


Fig. 1. 1a differs from 1b only in its location of the ground and positive rail feed points although 1a is not obviously fully symmetrical.

Many different feedback arrangements are possible and it is sometimes thought-provoking to decide whether a particular circuit is truly symmetrical, or whether it just uses a two transistor maintaining amplifier.

For example, an oscillator which used a cascode stage as the maintaining amplifier is definitely a single-ended design, the two transistor approach notwithstanding. **Figure 1a** looks very much like an oscillator with a maintaining amplifier that consists of a common collector stage driving a common base stage.

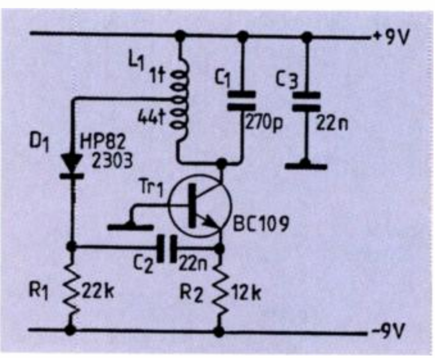


Fig. 2. Long-tailed pair circuits share the current switching action to maintain good amplitude control without bottoming at the collectors.

Apart from a minor relocation of the ground and positive rail feed points, it is the same as **Fig. 1b**, however, which is definitely a fully symmetrical oscillator. If the tail were infinitely long and the transistors had zero output admittance and no internal feedback, there would indeed be precious little difference between the circuits, but alas this is far from the case.

If one wants the purest possible output, then a fully symmetrical circuit is advisable; for RF circuits, this symmetry should extend beyond the circuit diagram to the actual physical layout.

When it comes to oscillators, the long-tailed pair lends itself to many variations on a theme. For example, the feedback can be via a coupled winding as in Fig. 1, or by capacitive cross-coupling. Alternatively, the bases can be connected to the tuned circuit, with the collector(s) going to the coupled winding(s). Whatever the circuit arrangement selected, there is always the choice of bipolars or FETs for the active devices.

If an asymmetrical arrangement such as that in Figure 1b is acceptable, then an interesting variant on the circuit is possible, as shown in **Fig. 2**. If you don't mind a terribly mixed metaphor, it could be called a long-tailed pair with one lame leg.

Although there is more than enough gain available from a single transistor to maintain oscillation, the circuit shown shares the current-switching action with true long-tailed pair circuits. These maintain firm amplitude control without bottoming at the collector, which is very difficult to achieve in conventional single transistor oscillator circuits.

An approximation of the circuit can be designed with little more than mental arithmetic. Having decided the working Q of the tuned circuit, taking into account any loading imposed by coupling energy to the outside world via a take-off point, the dynamic resistance at resonance R_d will be known.

The feedback winding must provide enough voltage to force the necessary current into the emitter of the transistor. The

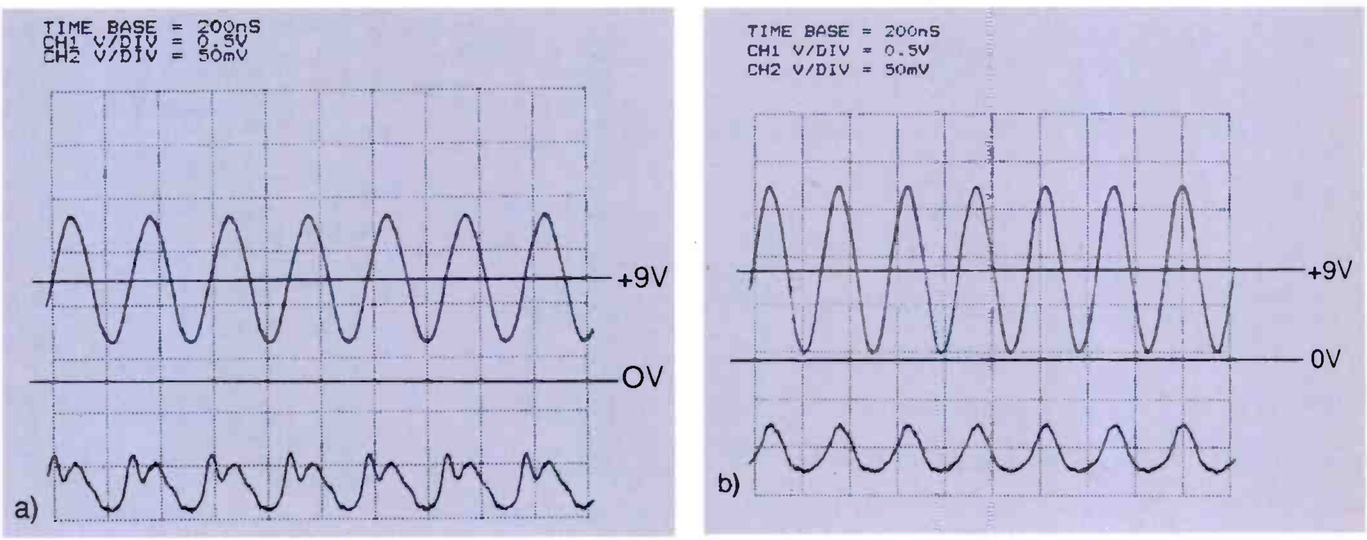


Fig. 3a. The collector and (horrible) emitter waveforms of the circuit shown in Fig. 2.
Fig. 3b. Substitution of the 2S131 by the BC109 results in a more rapid turn-off. The emitter waveform is more pleasing and the output amplitude is increased while still not bottoming.

resistance to be overcome is the emitter slope resistance $r_e = (25/I_e \Omega)$, where I_e is in milliamps, plus a similar allowance for the diode (assuming it carries the same tail current as the transistor).

Assuming the common base current gain of the transistor to be unity, the ratio of the collector voltage to the voltage at the tap feeding the diode is thus simply $R_d/(2r_e)$. This fairly cavalier approach to circuit design gives a (somewhat optimistic) figure for the required tapping ratio.

In practice, the ratio should be less extreme by a factor of two or three, to provide a safe margin of overdrive. This will ensure that the combined total tail current is chopped up into something closely approaching a squarewave, from which the desired fundamental component is then sorted out by the tank circuit. Incidental variations in loop gain from device to device and over temperature etc will then have little effect on the amplitude, merely affecting marginally just how square the squarewave of collector current is.

Figure 3a shows the collector and emitter waveforms of the circuit shown in Figure 2. The collector waveform (*CH 1*, 5V/division, allowing for a x10 probe) is DC-coupled, and the 0V level has been marked in. The emitter waveform - *CH2*, 0.5V/div - is AC-coupled, so the vertical position of the trace is immaterial.

A Schottky diode was used in the first instance, in the interests of fast switching; a 1N4148 was then substituted with no observable difference at all in the waveforms. The transistor, however, is another matter entirely. The BC109 is billed as an AF transistor, although with its 300MHz typical f_t, it is often useful as a small-signal RF transistor. It is used as a switching transistor in this circuit, and as such it performs very poorly as can be seen by the horrible emitter voltage waveform in Figure 3a).

A switching transistor like the 2S131 has a gold-doped base region. The gold doping results in a lowish h_{FE}, about a tenth that of the BC109, but provides recombination centres for the stored charge in the base region when the device is reverse-biased, resulting in a much more rapid turn-off. π

The result is shown in **Fig. 3b**: not only is the emitter waveform much more like what we would hope for, but the output amplitude is increased, although still without bottoming.

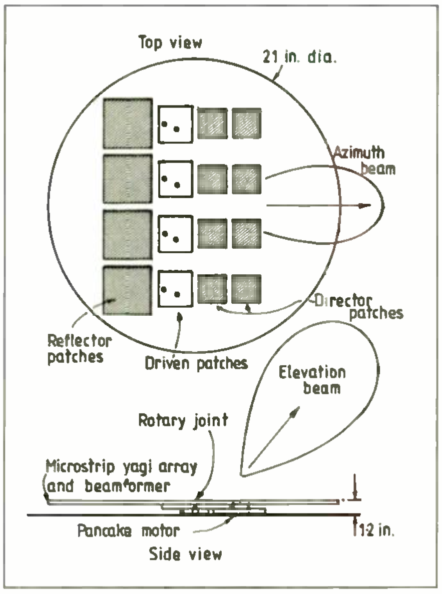
With a suitable modern alternative to the 2S131, the circuit of Figure 2 can form the basis of a useful VCO. For operation over a wide frequency range, the tap must be chosen to ensure oscillation at the lowest output frequency, where R_d is lowest. As a further refinement, the tail current can then be varied inversely as the frequency, thus maintaining a constant output amplitude over the whole tuning range. ■

Microstrip Yagi for mobile satellite service

A novel combination of Yagi-Uda and microstrip patch techniques, developed at the US Jet Propulsion Laboratory, California for Nasa could be used as a vehicle antenna for the 1.6GHz mobile satellite (MSAT) communications service. The array, described by John Huang and Arthur C Densmore in *IEEE Trans on Antennas and Propagation* (July 1991, pp.1024-1030), is claimed to provide a low-profile, relatively low-cost, medium-gain, land-vehicle mechanically-steered antenna. With four rows of microstrip patches, the antenna betters the MSAT required gain of 10dBi within the angular region between 20° and 60° elevations. The developers consider that the design overcomes the high costs and/or high profiles of both electronically steered phased arrays and mechanically-steered tilted microstrip patch arrays previously developed for MSAT for JPL.

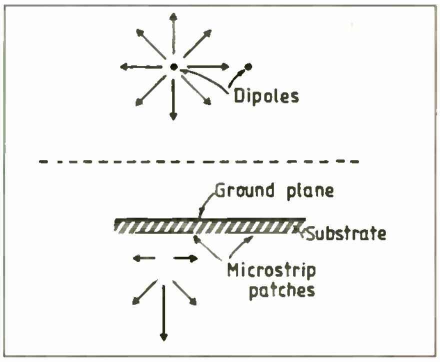
Since two of the major components of the system, the microstrip Yagi array and the beamformer, can be manufactured by simple etching processes, manufacturing cost based on a 10,000 units/year production is expected to be around $450/unit. Major component costs are the dielectric circuit board material, open-loop angular rate sensor, pancake motor, rotary joint, and assembly labour costs.

The microstrip Yagi uses the same principles as a conventional Yagi-Uda

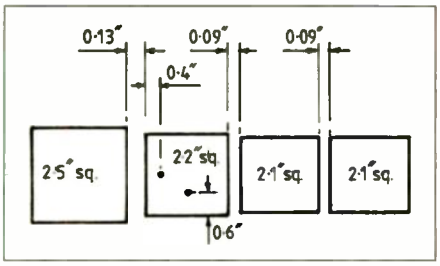


Using the planar mictrostrip Yagi for Msat.

dipole array, where the RF energy is coupled from the driven element dipole through space into the parasitic dipoles. But with microstrip patch elements, energy is coupled not only through space but also by surface waves in the substrate. The patch elements radiate primarily in a broadside direction and very little along the direction of the ground plane. This means that adjacent patches need to be placed very closely to

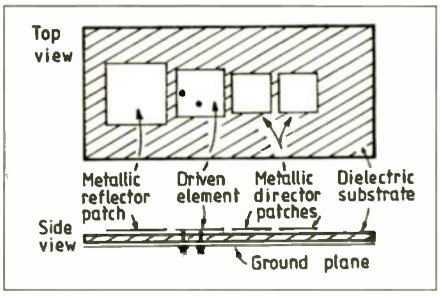


Adjacent patches need to be very close to achieve significant coupling through the surface waves.



Gap distance should be equal to or less than the dielectric substrate thickness.

achieve significant coupling through the surface waves. Experimentally, the gap distance between patch edges should be equal to or less than the dielectric substrate thickness.



Microstrip Yagi configuration – basis of a low-cost mecahncially-steered antenna.

Giant 14MHz Yagi-Uda fixed array

Three Californian amateurs have designed, constructed and demonstrated a giant 100m long, 25m high split-boom Yagi antenna, designed for a centre frequency of 14.150kHz and providing a free-space gain of 15.8dBi. Directivity at low-angle elevations (over low-conductivity earth) is over 21.5dBi.

For this ambitious project, Jack Haeten, Bud Ansley and Dan Bathker (W6TSW, W6PH and K6BG) have drawn on their professional expertise and Mininec-type method of moments aerial design software in building this gain-optimised 13-element, divided-boom array mounted on six towers in an area 10 by 100 metres with a boresight at 15° East of true North. This gives a great circle bearing covering selected parts of Europe and Asia, with an azimuth beamwidth to -3dB points of slightly less than plus and minus15°

The array elements have been designed for a considered balance between forward gain, sidelobe level, impedance level, bandwidth and structural wind survival and constructional economics. using the MN-software written by Brian Beezley, G6STI. Some 1000 machine-aided design iterations were made, backed up by "indispensable human judgement, experience and strategy." They consider that without NEC analysis such a complex array could not have been approached with high confidence.

The design provides a 30Ω feed-point resistance with an impedance bandwidth (vswr = 1.5) rather more than 2%. Each element is built with heavy-wall aluminium tubing starting in the centre with 32mm diameter, stepped twice, and ending with 19mm diameter at the tips. Each of the six 75mm diameter boom segments measure 9m. The topmost tower guys are dielectric to assure EM field purity.

Aspects of the Yagi-Uda story

When Professor Hidetsugu Yagi died in 1976 at the age of 90 years, it was recognised that he had left his memorial on countless millions of rooftops in the form of TV receiving aerials. But few of the millions of viewers could have had any idea of the involved story behind the development and use of the Yagi-Uda array.

The basic concept of directional antennas comprising a driven element with a number of parasitic elements: elements as reflectors slightly longer than a half-wave (single or trigonal) and a series of directors slightly less than a half wave in length was first described in English text by Professor Yagi of Tokoku Imperial University, Sendai, Japan in the June 1928 issue of Proc IRE (Beam Transmission of Ultra Short Waves).

There had been earlier papers and presentations from 1926 onwards by Shintaro Uda (1896-1976) who was then an assistant professor (Instructor) in the College of Engineering working under Professor Yagi, who in Part 1 of the IRE paper makes it clear that the experimental work on the 4m (75MHz) Yagi array was carried out by Uda. Indeed, the longer Part 2 of this paper is concerned with the use of early UHF magnetrons at wavelengths down to 10cm (3GHz). In this case the experimental work was carried out by E Okabe who continued to work with Yagi for many years.

The Proc IRE paper, based on an oral presentation, deals quite briefly with the principles of directional antennas using parasitic elements) with little or no mathematical analysis of the interactions between the elements. Nevertheless the value of such high gain arrays was recognized in the 1930s both in America and Europe.

An important contribution was made by Dr George Brown (RCA) in describing his work on directional medium wave broadcast antennas (monopole Yagi arrays) when he showed that a single close-spaced parasitic element could yield an array gain of over 5dBd, appreciably greater than with quarter-wave spacing. This led directly to the development of rotary flat-top HF Yagi antennas for Amateur Radio in 1937-38 (driven arrays by John Kraus, W8JK and Yagi arrays by Walter Van Roberts. The late Dr Brown once told me how his important section on Yagi close-spaced elements hadoriginally been submitted to the IRE in the early 1930s but had been rejected by referees - only subsequently he had slipped it into his long paper "Directional Antennas" (Proc IRE, January 1937, p78 to 145) where referees passed it without comment!

By the early 1940s multi-element HF Yagi arrays were being adopted secretly for a number of radar systems including searchlight control (SlC) radars and gun-laying radars in the UK. Surprisingly, however, although Yagi and Okabe worked on early Japanese radar experiments in the 1930s, the Yagi-Uda array was overlooked in Japan.

Professor Sato (Sophia University, Tokyo) has recently published a detailed account of how the Japanese "rediscovered" the Yagi-Uda antenna in 1942 after the fall of Singpore. This was as a result of finding a copy of notes and a manual on the British searchlight control radar system in a wastepaper basket in Singapore barracks after the surrender. The notes included sketches of a 4-element 210MHz antenna (plus reflector screen) captioned as a "Yagi aerial array". The Japanese did not connect "Yagi" with Professor Yagi and his 1928 paper but recognized that the radar required a highly directional antenna and instituted a search for further information. The notes and manual had belonged to a Corporal Newmann, a radar operator. They traced him to Shinagawa POW Camp in Tokyo. Under interrogation, they discovered he had little knowledge of the design principles but he does seem to have shown surprise that his captors had not realised that "Yagi" was a Japanese name.

When Professor Yagi was contacted, he is reported to have remarked that it was a very lamentable and ironical fact that the Yagi array "was not used in his country where it had been invented, but found use as a weapon by the enemy accounting for many victims". This seems to have happened too late for use in wartime Japanese radar; apparently the Yagi array was only used by the Japanese before 1945 for two inter-island links.

It has taken some 60 years to come to grips with the Yagi, and there are prospects of still further developments arising from the discovery by F M Landstorfer in the late 1970s that properly-shaped wire antennas, longer than a wavelength, could yield a higher directivity than straight dipoles. He found that a 3-element Yagi-Uda array of shaped wires, each 1.5λ long, could yield a maximum gain of 11.5dB.

David Cheng (Syracuse University) who has done much work on the optimization of gain of Yagi arrays has pointed out: "Although the geometrical arrangement of a Yagi-Uda array appears simple, its optimization is a difficult problem, mainly because there are many interdependent variables. Since all the elements are electromagnetically coupled, the adjustment of any one of these variables changes the current distribution on all the elements. Since the optimization process cannot follow a one-variable-at-a-time procedure, all variables must be adjusted at the same time... "

Many early studies of Yagi-Uda arrays made the basic assumption that the current distribution along all the array elements were sinusoidal. This assumption is not true, and the deviation from sinusoidal current distribution is critical in the calculation of the conditions for optimum gain.

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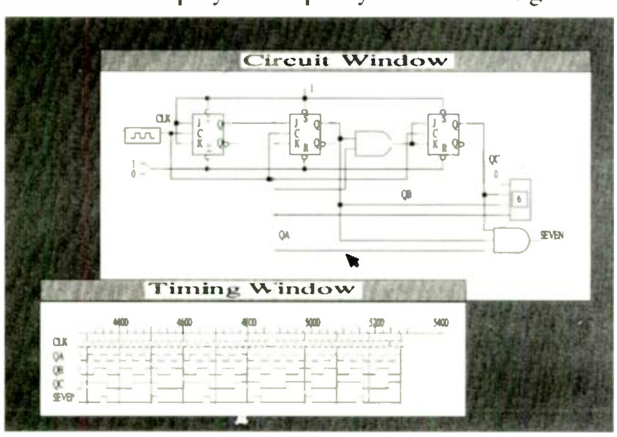

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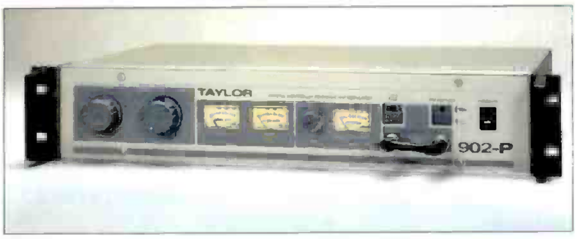

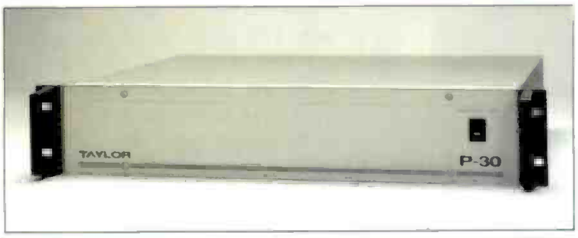

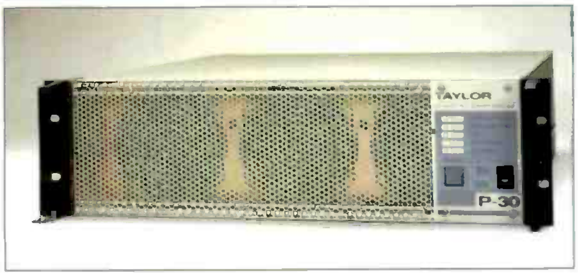

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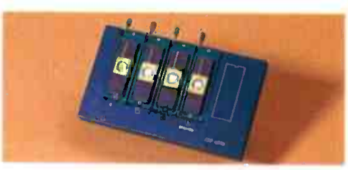

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The programmer comes with an interface card that plugs into any free slot of your PC. There is no DMA channel to worry about and it occupies limited I/O space. The programmer socket box is connected via a ribbon cable to the back of the interface card so that the socket box is external. After the interface card is installed the PC never need be opened again.

SUITS ALL PC's

The programmers will run on any compatible IBM machines such as XT's, AT's, '386 and '486. Whether it be AMSTRAD or COMPAQ the programmers will work. The software is text only monographic so is compatible with any machine.

SOFTWARE DRIVEN

All software for the programmer is supplied on 5¼" low-density disks. The software can be copied onto hard disk using the DOS copy command. Programs are supplied for the various features and are menu-driven. All programming is done from the menu, no hardware switches are needed. Just select the type and manufacturer and the programming is done automatically.

Save to disk and load from disk allows full filing of patterns on disk, to be saved and recalled. Device blank check, checksum, program, verify, read and modify are all standard features. Hex to bin file conversions included for popular file formats including Intel Motorola etc. 2 ways/4 ways bin file splitter for 16/32-bit file data. Selection of speed algorithm for FAST, FLASH, INTELLIGENT, INTEL. Free software updates available for new devices.

PC86 HANDY POCKET TESTER £99

Tests all popular TTL 74/54, CMOS 40/45 & DRAM types, can search and display type number of unknown/house marked types. Simple operation. 9 volt battery operated with LCD display.

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NO MORE WAITING FOR EPROMs TO ERASE. New advanced UV source gives under 2 minute erasure time on most types of modern EPROM. Digital down counter & display plus added features for simple operation in use. Large capacity e.g. 13×28 pin devices. Small footprint. Designed for heavy industrial/workshop use. UK design & manufacture.

PC84 EPROM PROGRAMMERS
1-GANG £139, 4-GANG £199 &
8-GANG £299

PC84 -1, -4, -8 Eprom programmers only. The variant is only gang size. The -4 and -8 gang will program multiple EPROMs simultaneously. Device are from 2716 to 271000 both C and NMOS & EEPROM from 2816 to 2864. ZIF (zero insertion force) sockets are used on all models

ORDER INFORMATION

Please include £7 for carriage by courier, plus VAT on all UK orders. (£20 for exports.) All pricing for programmers includes software, interface card, socket box and full instructions. (Prices do not include VAT or carriage). ACCESS, VISA or CWO. Official orders welcome from Government bodies & local authorities.

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