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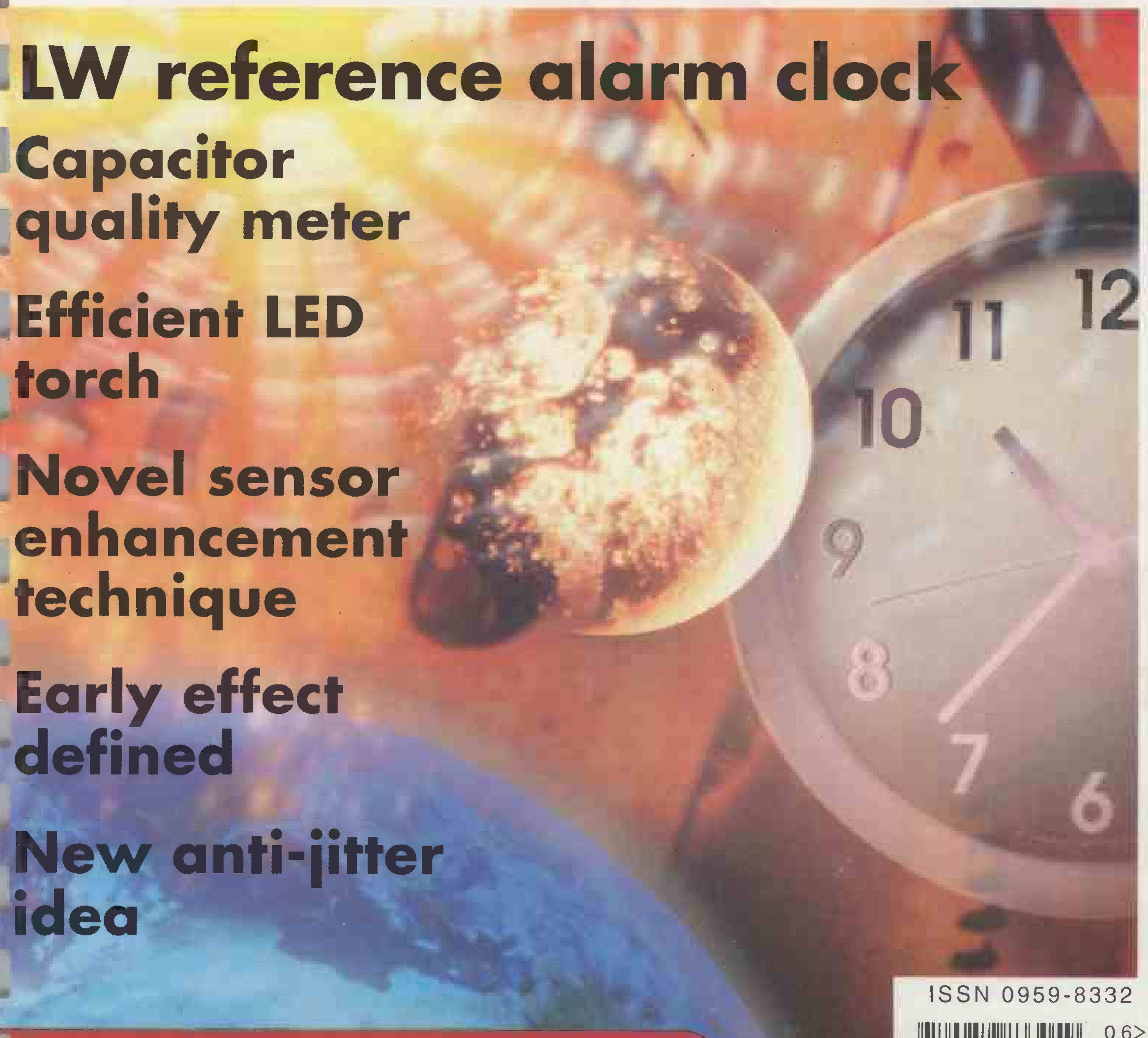

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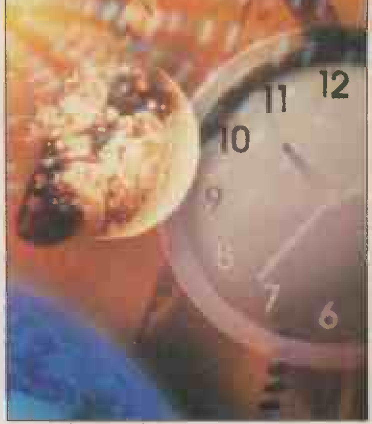

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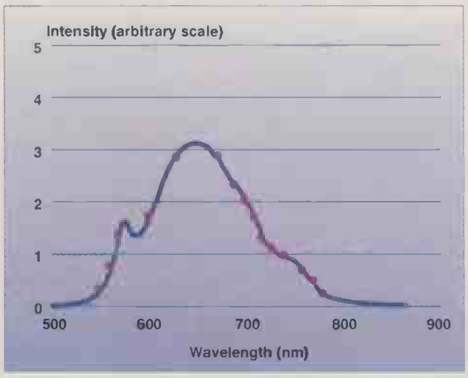
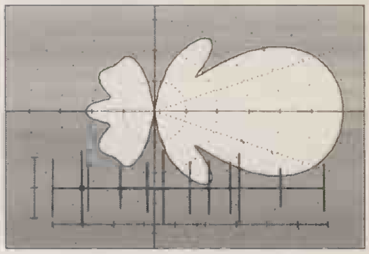
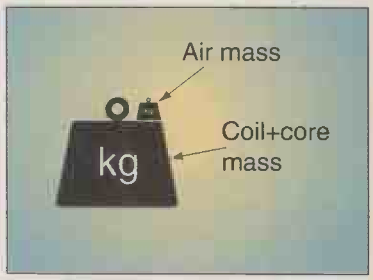


Researchers at Toshiba have for the first time managed to produce silicon LEDs operating below 5V, but quite how the light is being produced is a bit of a mystery. See page 445.



Can a 300Ω VHF antenna with open wire pair cable perform better than its low-impedance counterpart? Richard Formato shows that it can on page 505.



Why does the average 100W moving coil loudspeaker only deliver two or three watts of sound? John Watkinson explains why on page 493.

July issue on sale 27 May

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REED BUSINESS INFORMATION

What goes around...

Who would ever think that the Japanese electronics majors would ever seek to model themselves on US and European companies? But they are.

It seems only yesterday that US and European companies were being urged to adopt the Japanese business model. In the mid-eighties, as kings of consumer electronics and semiconductors and bidding to overtake the Americans in computing, the Japanese electronics industry seemed unstoppable.

Japanese quality was a byword. Western businessmen were urged to adopt Japanese practices such as 'quality circles' and pre-competitive consortia. Western politicians abased themselves in pursuit of Japanese inward investment.

It was a period in which the Japanese expanded overseas and when Japanese restaurants, gardens and art galleries sprouted in the world's cities. That was a time of great self-confidence; now is a time of great self-doubt. The Japanese don't seem inclined to moderation.

The reason for the change is the huge corporate losses being recorded by the big companies, a depressed home market and a stock exchange which collapsed a decade ago and has stayed collapsed.

The most outward and visible symptom of change is the abandonment of the lifetime employment tradition. The week before last, Sony announced job losses of 17 500; the week before that NEC announced plans to lay off 15 000.

In a country with only four per cent unemployment, reducing blatantly overstuffed work-forces may seem acceptable. But in a country where social service provision for the unemployed is rudimentary, it could trigger social revolution. Behind-the-scenes, the companies are adopting Western accounting standards.

Broadly speaking these practices will promote transparency to allow the outside world to see how profitable, or not, companies are, how indebted or not they are, how much their assets are worth in current market value rather than book value, and how great are their liabilities for future retirement benefits and pensions.

In the boardroom, the accent is now on profits rather than on increasing turnover and market share. "To comply with global standards of management we have to focus on cash-flow," says Yoshihide Fujii, general manager of Toshiba's semiconductor business planning division, "Japanese companies now appreciate P&L more. To run the business more healthily we have learnt that P&L management is more important."

The new thinking of Japanese businessmen is towards seeking out new global opportunities, encouraging an entrepreneurial mind-set in their managements, and even thinking the previously unthinkable – takeovers and mergers.

The new chairman of NEC who took over on 26 March, Dr Hajime Sasaki, says: "We should be more transparent both internally and externally".

As well as adopting Western financial conventions Japan feels it has to accelerate its adoption of the new digital technologies – PCs, the Internet, LANs.

It seems surprising that, in the country that the world perceives as a high-tech stronghold, there is a feeling among the industrial elite that they have missed the digital bus.

"Japan is now lagging behind the direction in which the rest of the world is heading, especially in the digital revolution which has changed lifestyles," says Dr Tsugio Makimoto, Hitachi's Chief Corporate Technology Officer.

Language is another problem.

"In the US there are many start-up companies with good ideas using the digital revolution very effectively, particularly the Internet," says Makimoto, "such companies can do worldwide marketing via the Internet. That is a big change in favour of small companies."

"The way of management is changing because of e-mail and information flows which makes for flat organisations," he says. "But most of the Japanese industries have hierarchical, bureaucratic styles of management and it's very difficult to move them very quickly. So the digital revolution is making it very difficult for big companies in Japan."

What goes around comes around. ■

David Manners

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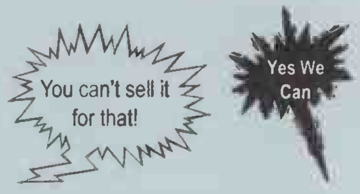

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UPDATE

Strong pound is stifling industry

The unusually high strength of the pound is making life difficult for the UK's electronics manufacturing industry, according to managers and industry bodies.

The Sterling Index, which gauges the relative strength of the UK's currency, reached 103.9 points – a six-month high – at the end of March.

"It has probably had a significant influence on us," said Jeffrey Davis, Viasystems' European president. "From our point of view it is a long term problem; we are not so much influenced by peaks and troughs."

The six month high, however, is part of a larger trend, said Elaine Barnett, an economic advisor at the Foundation for Manufacturing and Industry. "The Index was at 80 in January 1996, a 20 per cent rise is quite a startling increase. [For electronics] I think there must be immense competition from Asia. The depreciation of their currencies could have an enormous detrimental impact on the electronics sector," she said.

What concerns the Federation of the Electronics Industry (FEI) is that when the pound is too strong, it curtails UK manufacturers' ability to take advantage of inherent strengths. "It can severely curtail manufacturing. The electronics industry operates on a global basis. International organisations are ready to move manufacturing from one place to another when this happens," said John Park, the FEI's deputy director general.

"We felt the Budget didn't address the strength of sterling. About 52 per cent of UK engineering [including electronics] manufacturing is exported. If UK growth slowed down and European growth sped up, it would help the situation," said Barnett.

"When there is a problem with a currency, there is a trend to find continental based manufacturing," said Davis. "The PCB industry is complicated by the fact that a customer will approve only one or two plants. Generally it makes the PCB industry less flexible and it tends to hit harder."

Davis added: "Viasystems' main production assets are in the UK, about 65 to 70 per cent of our production. Therefore most of our production is influenced by the pound."

Alex Mayhew-Smith
Electronics Weekly

Silicon LEDs show a promising light – but why?

Exotic compound semiconductors have been needed to produce LEDs ever since General Electric used gallium arsenide (GaAs) to make the first practical one in 1962.

Since then, the materials and structures have become ever more complex. Today's LEDs often also include aluminium, nitrogen, indium and phosphorus and owe more to laser manufacture than to older LED processes.

All this complexity adds to cost. For some time, researchers have been hunting for a way to make LEDs using silicon on standard silicon processes.

There have been some successes, although none comes close to matching compound semiconductor devices for brightness or efficiency. This situation is unlikely to change for a while yet.

Porous silicon, for instance, has been shown to emit light, but making it requires processes not compatible with chip manufacture.

Silicon nanocrystals can also be persuaded to emit light. However, according to LED maker Toshiba, they have, up to now, required between 10 and 25V to operate; excessive for today's chips.

The latest announcement comes from the Advanced Research Laboratory of Toshiba in Japan. Scientists there have pushed nanocrystal device operating voltage below 5V while using formation methods broadly compatible with current integrated circuit production.

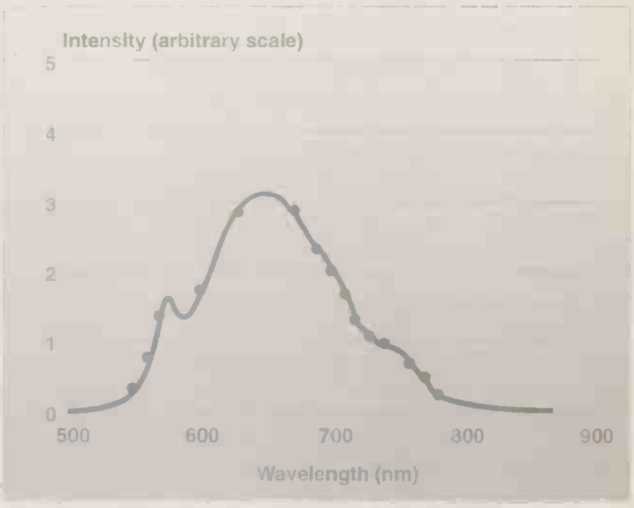
Making Toshiba's devices involves depositing a layer of amorphous silicon around 2nm thick onto a silicon wafer. This wafer is then heated to between 700 and 850°C in an oxygen or nitrogen atmosphere for a few minutes.

During this heating, silicon nanocrystals grow on the wafer surface inside the amorphous silicon.

Once cool, the nanocrystals emit visible light at room temperature when reverse biased through a Schottky contact.

The crystals are hemispherical and, by altering the amorphous silicon layer thickness, processing temperature, atmosphere and heating duration, the researchers have made different sizes.

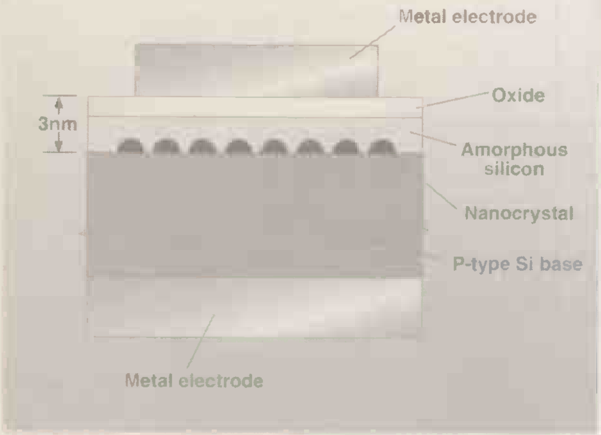
Orange emission came from samples processed at 700°C in nitrogen or oxygen.



Over the hump... Weak but definitely red. Toshiba is producing visible light from silicon.

Red came from 800°C processing in nitrogen (at 3.5-4V), but an oxygen atmosphere at these high temperatures caused the nanocrystals to oxidise away. Similar destruction of the nanocrystals happened with nitrogen above 850°C where they were converted to polysilicon.

The experiments have narrowed down the source of the



electroluminescence, but not identified it.

It is not due to defects in the amorphous silicon, or defects at either of its surfaces, or the amorphous silicon-nanocrystal boundary. However, it only happens in nanocrystals less than 2nm across and 1.5nm high, and wavelength is related to crystal size.

The team's best guess at the moment is that the light is coming from within the nanocrystals themselves and that emission is due to "the quantum confinement effect" within them. More specifically, "the recombination of confined electrons and trapped holes".

Hot technology... Baking thin amorphous silicon layers produces the essential nanocrystals.

The team's report says that efficiency, at the moment very poor, can be improved by increasing the number of nanocrystals and strengthening the carrier confinement. It concludes that: "The LEDs that have been demonstrated are promising devices for realising monolithic optoelectronic ICs".

Steve Bush *Electronics Weekly*

UK engineering skills shortage highlighted

Two-thirds of the UK's electronics companies consider a shortage in engineering skills to be one of the most serious problems affecting their business, a survey has found.

The survey by the Federation of the Electronics Industry (FEI) has found that the shortages are not confined to specific jobs, disciplines or industry sectors but includes all skilled activities in the electronics industry.

Telecommunications operator BT confirmed that there is an industry problem. "We do notice problems in recruiting in technical areas," said a BT spokesman. "But we obviously have a bit of an advantage in that BT is a well known company." The company recruited 540 graduates last year.

Pace Micro Electronics is seeking to recruit 100 R&D engineers this year to work on its digital TV products. "We're fortunate that we're in a rapidly growing business so we can attract engineers," said Tim Fern, director of engineering, broadcast, at Pace.

However, the shortage of suitable graduates is putting pressure on pay and conditions as companies like Pace compete to recruit the best engineers. "We're offering increasing benefits and salaries," said Fern.

The UK education system is currently producing fewer than 3000 software engineers a year and an increasing number of them are going into IT. It is a situation that the government is well aware of, according to Fern, who has already lobbied DTI ministers, John Battle and Barbara Roche in his quest for action on the problem.

Melanie Reynolds

In brief

Interactive TV turned on

The UK's first interactive TV service is now available via NTL's TV-Internet set-top box.

The communication company's service, delivered via a BT phone line, offers customers access to shopping, news, sport, travel and local information through their TV. A keyboard is available for sending e-mail. The service will be offered via digital terrestrial TV and NTL's own cable network later this year.

The service has been designed for ease of use. "The whole essence of what we're doing is making the content feel like television," said Jason Rogers, technology director. "It doesn't look like small text and a million different frames like an Internet page."

The company intends to add games over its network from the autumn. "We've been developing relationships with a number of providers to develop games onto our set-top platform," said Rogers. The network connection offers the prospect of multi-player games.

NTL is already looking for enhanced set-top box performance next year to better display graphics and content. It is also seeking to improve the box's connectivity using greater bandwidth ISDN, ADSL and cable modem lines. "We're trying to drive the whole level of functionality up by exploiting the power of these boxes along with increased Mips and richer graphics," said Rogers.

CRTs have a bright future, researchers conclude

CRTs remain the dominant display technology, despite the rapid growth of flat panels such as LCDs and plasma displays, claims Reed Electronics Research in its latest analysis of the European display market. Over 60 per cent of sales are down to CRTs. The European market was worth \$3.8bn last year, and is expected to exceed \$5bn by 2003. LCDs dominate the flat panel sector, accounting for over 82 per cent of sales. www.rer.co.uk

UK business costs are lowest

According to a survey by KPMG Consulting, the UK has the lowest business costs in Europe for the manufacture of electronics and telecommunications equipment.

The survey, which compared the cost of doing business among 64 cities in eight countries, saw the UK leading the way in Europe, with France second and Italy third. Charles Thomas, a consultant with KPMG, said: "The results of this study are extremely good news for the UK's prospects of attracting inward investment, particularly for non-EU companies looking for a European base."

The survey, which included the G7 countries and Austria, showed the UK to have the lowest labour costs in electronics and telecoms manufacturing and the smallest corporate income tax rates along with Austria.

The three UK cities included in the survey – Cardiff, Manchester and Telford – were found to be lower cost locations than all but one US city: San Juan.

Comms antenna health probe call

A Commons call for new research into the health effects of telecommunications masts has been backed by 28 MPs.

A special Parliamentary motion expressed concern about the possibility of short-term memory loss and other illnesses caused by "low energy electromagnetic fields". It urged the DTI, and the Department of the Environment, Transport and the Regions to commission the research and, if necessary, introduce planning guidelines to stop the siting of the masts in populated areas such as on school roofs.

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The four integrated virtual instruments give lots of possibilities for performing good measurements and making clear documentation. The software for the HANDYSCOPE 2 is suitable for Windows 3.1 and Windows 95. There is also software available for DOS 3.1 and higher.

A key point of the Windows software is the quick and easy control of the instruments. This is done by using:
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Some quick examples:
The voltage axis can be set using a drag and drop principle. Both the gain and the position can be changed in an easy way. The time axis is controlled using a scalable scroll bar. With this scroll bar the measured signal (10 to 32K samples) can be zoomed live in and out.

The pre and post trigger moment is displayed graphically and can be adjusted by means of the mouse. For triggering a graphical WYSIWYG trigger symbol is available. This symbol indicates the trigger mode, slope and level. These can be adjusted with the mouse.

The oscilloscope has an AUTO DISK function with which unexpected disturbances can be captured. When the instrument is set up for the disturbance, the AUTO DISK function can be started. Each time the disturbance occurs, it is measured and the measured data is stored on disk. When pre samples are selected, both samples before and after the moment of disturbance are stored.

The spectrum analyzer is capable to calculate an 8K spectrum and disposes of 6 window functions. Because of this higher harmonics can be measured well (e.g. for power line analysis and audio analysis).

The voltmeter has 6 fully configurable displays. 11 different values can be measured and these values can be displayed in 16 different ways. This results in an easy way of reading the requested values. Besides this, for each display a bar graph is available.

When slowly changing events (like temperature or pressure) have to be measured, the transient recorder is the solution. The time between two samples can be set from 0.01 sec to 500 sec, so it is easy to measure events that last up to almost 200 days.

The extensive possibilities of the cursors in the oscilloscope, the transient recorder and the spectrum analyzer can be used to analyze the measured signal. Besides the standard measurements, also True RMS, Peak-Peak, Mean, Max and Min values of the measured signal are available.

To document the measured signal three features is provided for. For common documentation three lines of text are available. These lines are printed on every print out. They can be used e.g. for the company name and address. For measurement specific documentation 240 characters text can be added to the measurement. Also "text balloons" are available, which can be placed within the measurement. These balloons can be configured to your own demands.

For printing both black and white printers and color printers are supported. Exporting data can be done in ASCII (SCV) so the data can be read in a spreadsheet program. All instrument settings are stored in a SET file. By reading a SET file, the instument is configured completely and measuring can start at once. Each data file is accompanied by a settings file. The data file contains the measured values (ASCII or binary) and the settings file contains the settings of the instrument. The settings file is in ASCII and can be read easily by other programs.

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Will printed FEDs replace plasma panels?

There's a number of up-and-coming emissive display technologies emerging at the moment.

The first is from Oxfordshire's Printed Field Emitters (PFE). It has been working on an electron-emissive material to go at the back of field emission displays (FEDs) as an alternative to micromachined Spindt cathodes, diamond films and diamond-like carbon films.

The advantage of its material, claims the company's Dr Richard Tuck, is that it can be applied using a printer rather than chemical vapour deposition or other 'high-tech' process.

So keen is the company on printing that it is also looking at printing the spacers essential for preventing FEDs from imploding.

Other FED companies are investigating at more elaborate schemes. Candescent, for instance, is using short glass fibres stood on end. Printed spacers are not necessarily as fine as fibres, but large area displays – where PFE is aiming its technology – have big pixels which can accommodate fatter spacers.

According to Tuck, the only non-printing process is a single self-aligning whole-panel lithographic stage used to open-up emission sites.

Tuck reckons that the 1m diagonal hang-on-the-wall TV market is the one to go for and claims printed FEDs will undercut the price of similarly-sized plasma panels. He says panel costs will not differ between types, but drive electronics will be considerably cheaper for printed FED panels as lower voltage, lower frequency signals are required.

At the other end of the size scale, the confusingly named FED Corporation has just licensed organic light emitting diode (OLED) technology from Kodak.

FED Corp began life five years ago as a field-emission display company. Three years ago it changed horses to LCD and OLED technology when it realised FEDs were less suitable as micro-displays – its target market.

Micro-displays are predicted to be a fast growing market as games head sets and wearable computers become more popular.

Now FED Corp aims to sample silicon-backplane miniature LCDs this year and silicon-backplane miniature OLED displays soon afterwards.

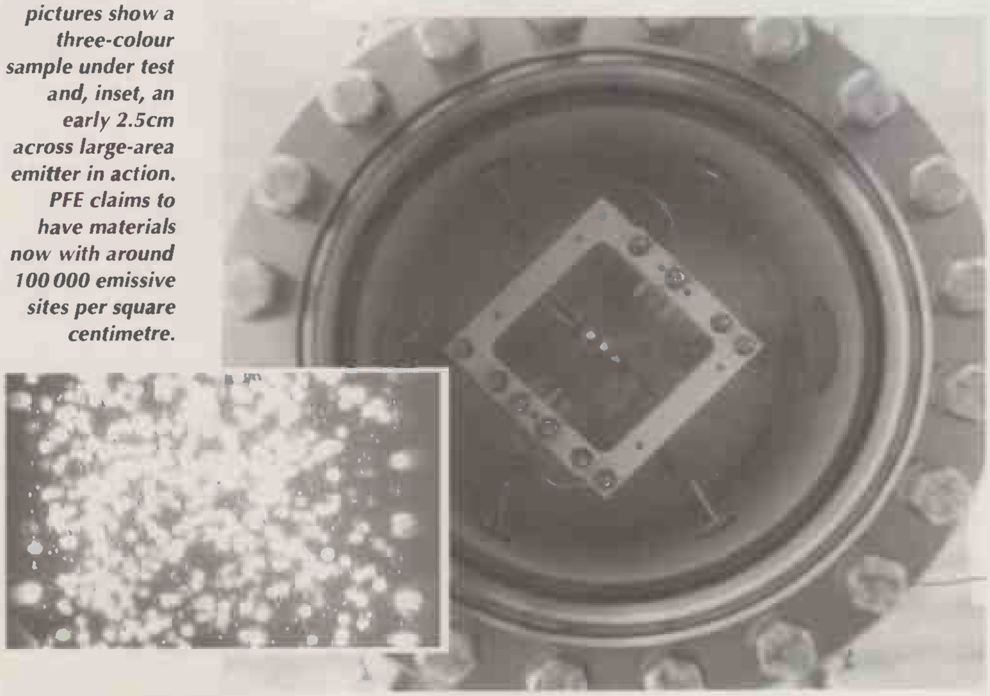
Many companies are in production or close to production with silicon LCDs, but FED Corp sees an advantage in moving to silicon-backed OLED displays. "We think an LCD headset display will use around 2W of power. An OLED version will probably get down to 0.5W," said company executive v-p Susan James.

OLEDs are sometimes called molecular emitters, or small molecule emitters, to differentiate them from light-emitting polymer (LEP) displays of the type that Cambridge Display Technology (CDT) is working on and licensing.

OLEDs and LEPs have broadly similar characteristics and both CDT and Kodak have licensees who are making equipment with their technology. In the OLED case it is Pioneer which is using organic LEDs in car radio displays.

OLEDs, from Kodak, have been around the longest. The company is banking on this to promote its technology in the market. OLEDs can also provide a long-life blue emitter – something that the LEP brigade is only just testing. On the other hand OLEDs need to be vacuum deposited, whereas LEPs can be printed.

Steve Bush



Printed light... Oxfordshire company Printed Field Emitters (PFE) is developing electron-emissive materials for use in field emission displays that can be printed. As with all FEDs, electrons hit a phosphor to create light. The pictures show a three-colour sample under test and, inset, an early 2.5cm across large-area emitter in action. PFE claims to have materials now with around 100 000 emissive sites per square centimetre.

Young engineers are getting better off

The starting salary for engineering graduates is rising as a result of growing competition, according to the latest pay survey from the Institution of Electrical Engineers (IEE).

"We noticed that of the younger people who did respond, their salaries seem to have gone up quite a lot in certain areas," said Beryl Gurney, IEE professional development section. "Computer linked industry starting salaries seem quite high."

The survey based on 8510 responses from IEE members found that its Associate Members i.e. engineers with degrees, enjoyed the sharpest rise in salary at nine per cent, bringing their median wage to £28 800. But the IEE believes that this result was skewed due to younger associate members, traditionally having lower wages, failing to respond while the older ones with higher wages did.

Chartered Engineers' salaries increased by 4.7 per cent to a median of £38 000 while Associates – engineers without degrees – achieved a rise of 2.8 per cent taking them up to £29 600.

HSE plans PC health study

A year-long study to investigate the potential health risks of using portable and handheld computers is being funded by the Health and Safety Executive.

The study will be carried out by ergonomics consultancy, System Concepts, and will look at the issues arising from the extended use of portables.

"A lot of these things are issues which we can do something about if we know about them," said Tom Stewart, managing director of System Concepts.

According to Stewart, several manufacturers have contacted him since the study was announced and are keen to include any improvements needed in their designs.

As an alternative to MSF, VHF broadcast data can be used for precise clocks – if you don't mind retuning as you move around the country. But relying on Radio 4's often overlooked RDS-type signal on long-wave, Peter Topping's reference alarm clock works anywhere in the UK without retuning.

LW off-air reference clock

Radio 4's long-wave transmitter on 198kHz carries data as well as the audio signal. This data has some similarities with the RDS data included in VHF radio signals in many European countries, but it has a much lower data rate and is used for a different purpose.

There are 16 data-block types. Type 0 is used for time, date and 'filler' data. The other blocks are used commercially. Each one is available to the company leasing it for use in a specific application. Typical uses are electricity tariff switching, foreign exchange rate board updating and lighting control.

The whole of the UK is covered by a 500kW transmitter at Droitwich in England, with a little help from two 50kW transmitters at Westerglen and Burghead in Scotland. All three transmitters use the same frequency. The specification of LF radio data is described in a BBC document[1].

Time data is transmitted every minute on the minute and provides a very accurate clock traceable to national standards. Local time variation, for example BST, is also transmitted.

In this application, time and date can be permanently displayed, while all incoming data can be displayed in hexadecimal form. The microprocessor converts the transmitted date information – day-of-week, week number and year type – into day-of-month and month.

The year is not transmitted and cannot be uniquely determined from the available data. The position in the 28-year leap year/year-start-day cycle can, however, be worked out and this can be used to calculate a year in the range 1995 to 2022. It is not possible to distinguish between 1995 and 2023.

Peter is an MCU applications engineer at Motorola's East Kilbride plant.

Table 1. Structure of clock-time blocks used in Radio 4 long-wave's RDS-like service.

Bit	Function	
1	Prefix (1)	Used only for synchronisation and error detection
2-5	Block type no	0000
6	Time/filler flag	0
7-8	Leap year cycle	00; this year leap 01; last year leap 10; leap year 2 or more years away 11; next year leap
9-11	Year start day	Day-of-week on 1 January (1: Monday, 0 not used)
12-17	Week number	Week number (1-53, 0 & 54-63 not used)
18-20	Day of week	Current day of week (1: Monday, 0 not used)
21-25	Hours	0-23 UTC (24-31 not used)
26-31	Minutes	0-59 UTC (60-63 not used)
32-37	Local offset	Local deviation from UTC in 2's complement form in increments of 30 minutes (BST=CET=000010)
38-50	CRC	Used only for synchronisation and error detection

Hardware involved

Figure 1 shows a block diagram of the design: the microprocessor used for decoding is the *MC68HC(7)11* while an *MC3371* is used for the radio receiver. Unlike RDS, where demodulation chips are available, the capability of retrieving the data bits has to be included in the hardware design.

The *3371* is a superheterodyne receiver including a mixer and limiting IF amplifier. It also has an FM demodulator intended mainly for dual-conversion VHF communication equipment. The radio-data is modulated so the *MC3371* is suitable, even though it works at an unusually low radio frequency.

The RF of 198kHz is converted to a standard 455kHz IF. Operational amplifiers are used to amplify, filter, integrate and limit the signal into a form that can be used by the microprocessor. Four keys control the decoder and a 16-character dot-matrix LCD module displays the data, time, etc.

This design incorporates an alarm clock similar to that described in application note AN460[2]. If the clock is permanently powered, the alarm can be used to switch on the radio supplying the data at the required alarm time. This control could be to the power supply of the radio, or to the audio stage only.

If an audio mute is used, radio-data time information can be updated even when the radio is 'off'. Alternatively the decoder can be used simply to display time and date with its power being supplied from the radio and manually switched on and off.

Radio data on long wave

Transmitted data is conveyed using linear phase-modulation of the carrier by a shaped and bi-phase-encoded waveform. This is applied to the main carrier as there is insufficient space in the ±4.5kHz low-bandwidth AM signal for a subcarrier.

In order not to interfere with normal modulation, the data rate is a very low, at 25Hz. Bi-phase coding and a small deviation of ±22.5° are used so that the transmission's use as a frequency standard is retained.

The data stream is partitioned into 50-bit blocks but, like RDS data, there are no gaps between blocks. Additional cyclic-redundancy check word, or CRC, bits are added to allow synchronisation.

The bit rate of 25Hz and the block length of 50 bits mean that a block takes 2 seconds, hence 30 blocks are transmitted every minute.

Each 50-bit block contains a single-bit prefix – which is always logic 1 – a 4-bit application code or 'block number', 32 bits of data and 13 extra CRC bits used for synchronisation and error detection and correction, **Table 1**.

The particular code used is the 49, 13 shortened cyclic code ($G(x)=36365_8$) described by Kasami[3]. It is modified though by the addition of the fixed prefix to address the cyclic code's poor block-synchronisation capability.

The CRC is the remainder calculated in the transmitter by dividing the 36 data bits – including the application code – by the generator polynomial.

As this remainder is then used as the 13-bit check word, the 49 received bits should give a remainder of zero when divided by the generator polynomial. Looking for a zero 13-bit remainder thus carries out synchronisation.

Multiplication of the 49-bit received data by the matrix shown in **Table 2** is equivalent to this polynomial division and is the method used here. During synchronisation this calculation has to take place after each bit is received, using the last 50 bits – actually 49 as the first fixed bit is not used – until a valid zero remainder is found.

Once the valid remainder is found, the check need only be done after another 50 bits have been received, as this is when the next valid block would be expected. If, at that point, a zero remainder is not found the bit-by-bit check is re-started.

The CRC bits make error correction possible, but this application does not include that facility. They are only used for synchronisation and error detection.

Burst error correction

Use of burst error-correction can allow good data to be received in the presence of errors, but it also increases the undetected error rate. This is because blocks with more errors than the code is capable of correcting – a single burst of up to 6 bits – may be deemed correctable and thus pass through undetected.

Blocks of type zero are used for transmitting the time and date information and for 'filler' codes. All other types, i.e. 1 to 15, are user blocks. Their data is meaningless in this context, but it can be displayed in hexadecimal form as it comes in.

The first of the 32 data bits in a type 0 block determines whether it is a time-code block, in which case the first bit a zero, or simply a filler, when the first bit is a one. Time-code blocks are transmitted immediately prior to the

Table 2. 13 by 49 decoding matrix used to process the 49 bits of incoming data.

Hex.	Binary	Octal
17 3B	1 0111 0011 1011	13473
15 E7	1 0101 1110 0111	12747
14 89	1 0100 1000 1001	12211
14 3E	1 0100 0011 1110	12076
0A 1F	0 1010 0001 1111	05037
1B 75	1 1011 0111 0101	15565
13 C0	1 0011 1100 0000	11700
09 E0	0 1001 1110 0000	04740
04 F0	0 0100 1111 0000	02360
02 78	0 0010 0111 1000	01170
01 3C	0 0001 0011 1100	00474
00 9E	0 0000 1001 1110	00236
00 4F	0 0000 0100 1111	00117
1E 5D	1 1110 0101 1101	17135
11 54	1 0001 0101 0100	10524
08 AA	0 1000 1010 1010	04252
04 55	0 0100 0101 0101	02125
1C 50	1 1100 0101 0000	16120
0E 28	0 1110 0010 1000	07050
07 14	0 0111 0001 0100	03424
03 8A	0 0011 1000 1010	01612
01 C5	0 0001 1100 0101	00705
1E 98	1 1110 1001 1000	17230
0F 4C	0 1111 0100 1100	07514
07 A6	0 0111 1010 0110	03646
03 D3	0 0011 1101 0011	01723
1F 93	1 1111 1001 0011	17623
11 B3	1 0001 1011 0011	10663
16 A3	1 0110 1010 0011	13243
15 2B	1 0101 0010 1011	12453
14 EF	1 0100 1110 1111	12357
14 0D	1 0100 0000 1101	12015
14 7C	1 0100 0111 1100	12174
0A 3E	0 1010 0011 1110	05076
05 1F	0 0101 0001 1111	02437
1C F5	1 1100 1111 0101	16365
10 00	1 0000 0000 0000	10000
08 00	0 1000 0000 0000	04000
04 00	0 0100 0000 0000	02000
02 00	0 0010 0000 0000	01000
01 00	0 0001 0000 0000	00400
00 80	0 0000 1000 0000	00200
00 40	0 0000 0100 0000	00100
00 20	0 0000 0010 0000	00040
00 10	0 0000 0001 0000	00020
00 08	0 0000 0000 1000	00010
00 04	0 0000 0000 0100	00004
00 02	0 0000 0000 0010	00002
00 01	0 0000 0000 0001	00001

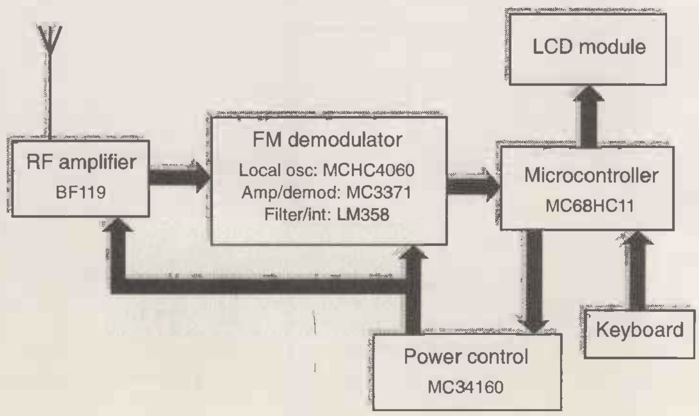


Fig. 1. Outline of the long-wave Radio 4 data decoder. Although the radio data on long-wave is similar to that on VHF broadcasts, there are no specific hardware solutions for the long-wave version so the decoding needs to be done by a microcontroller.

minute epoch so that the exact time is indicated, although only hours and minutes are included in the data.

Structure of the time-code block is shown in Table 1.

Hardware details

The microprocessor used is the *MC68HC811E2*. A *711E9* or *E20* could also be used. An *MC3371* is used for the radio receiver. The *3371* is a superheterodyne receiver including mixer, limiting IF amplifier and FM demodulator.

The radio frequency of 198kHz is converted to the standard 455kHz IF. This would normally require a crystal of 653kHz, which is not a standard frequency and would be difficult and expensive to obtain. To avoid an expensive crystal, higher standard frequency types were investigated to find one suitable for dividing down to approximately the correct frequency.

Two suitable crystals were found. One was a 10.5MHz type intended for 14MHz to 3.5MHz amateur-band conversion. Divided by 16, 10.5MHz gives 656.25kHz. The other was a 20.945MHz type intended for 21.4MHz to 455kHz conversion. Divided by 32, this one gives 654.53kHz. An *MC74HC4060* forms an oscillator and divider providing the signal for the *3371*'s mixer.

The complete circuit diagram of the analogue board is shown in **Fig. 2**. Radio-frequency signal is derived from a ferrite rod whose coil can be either a standard LW winding, or can be flat-wound with thin insulated wire. On a standard 0.25in ferrite rod using 36SWG wire, this winding is about 3.75in long, i.e. 190 turns.

The easiest way to get the winding to the correct inductance is to wind it on a paper former so that it can be slid along the rod. If a 4.25in winding of around 210 turns is made and the 330pF capacitor and trimmer connected, resonance will be found by sliding the winding partially off the end of the rod.

Finding antenna resonance

Resonance of the antenna can be observed on an oscilloscope, but is most easily found by holding the rod close to a radio – preferably one with a signal strength meter – tuned to 198kHz. The radio's signal will be noticeably affected as resonance is achieved.

The winding is then adjusted by slowly sliding it fully onto the rod, maintaining resonance by removing turns. If this is done with the trimmer in the mid position, the antenna can be completed and finally adjusted using the trimmer without any specialised equipment.

The output winding consists of a further 20 turns at the earthed end of the main coil. An antenna made this way worked satisfactorily but the prototype performed better and was less sensitive to orientation when using a Litz-wound rod taken from an old radio.

RF amplification

The signal is amplified by a *BF199* with a tuned load employing a Toko *CAN1A350EK* long-wave RF coil and 220pF. The coil should be tuned for maximum output.

Additional selectivity is provided by the 198kHz crystal, available from AEL.[7] The application works without this crystal, but with a much reduced sensitivity and tolerance to interference.

This signal goes into the mixer of the *MC3371*. As this design operates at a single frequency, it is not strictly necessary to use a superheterodyne arrangement. However, it allows the use of an off-the-shelf high-Q 455kHz demodulator coil (Toko *RHCS45328AC2*) rather than using a separate coil and capacitor at 198kHz. With a separate coil and capacitor, it would be very difficult to achieve a Q value as high as 180.

Local oscillator

The local oscillator is fed by a *4060* as described above. A Murata *CFU455D2* filters the intermediate frequency. At 20kHz, this ceramic filter's bandwidth is far wider than necessary in this design, but its selectivity is not required and this width allows the use of the less precise local oscillator frequency.

Adjustment of the demodulator coil needs care due to the coil's high Q.

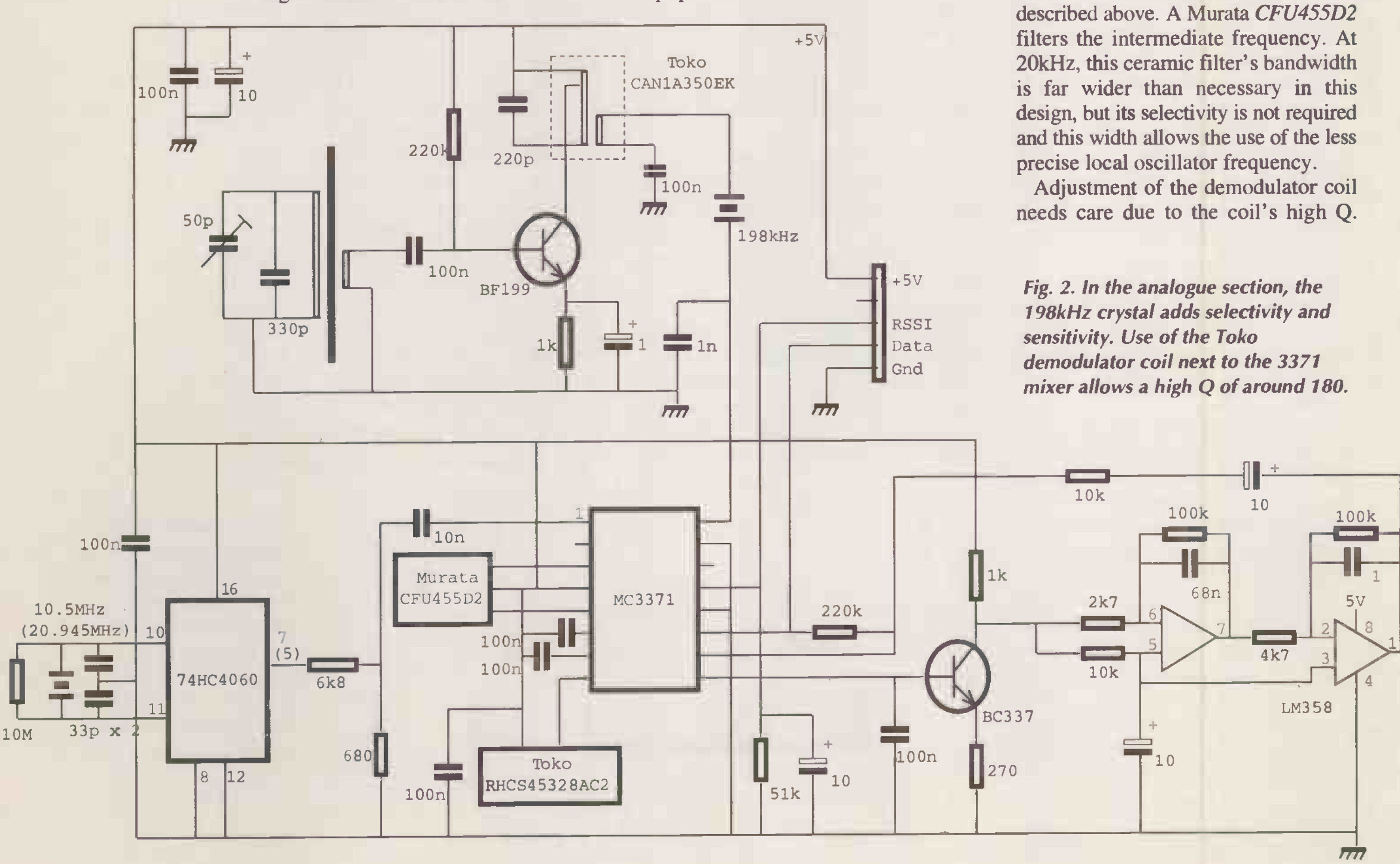


Fig. 2. In the analogue section, the 198kHz crystal adds selectivity and sensitivity. Use of the Toko demodulator coil next to the 3371 mixer allows a high Q of around 180.

The Q is kept as high as possible by omitting a damping resistor. High Q is necessary because the 9mV pk-pk output signal, which is small due to the low deviation employed, is proportional to it.

The voltage at the collector of the *BC337* can be used to adjust the demodulator coil. It will jump from about 1.4V to close to 5V as the correct IF is passed. The coil should be adjusted for a collector reading of 2.5V. The DC working voltage of the first two op-amps is derived from this voltage so any drift is cancelled.

The only other adjustment that may be needed is to the amplifier gain, but the two prototypes I tested worked well with the values shown. Overall gain – including that of the *BC337* and the first low-pass filter op-amp – is 110. This gives a peak-to-peak signal of about 1V at the op-amp's output.

The peak-to-peak signal at the output of the second integrating op-amp is also nearly a volt, but the DC level at this point is not well defined. As a result, AC coupling is used to pass the signal to the comparator. The op-amp in the *MC3371* is suitable for use with this type of coupling and is used as a comparator.

The digital side

Figure 3 shows the circuit diagram of the digital board. It incorporates a parallel high-contrast LCD module based on an *HD44780* driver with an *HD44100* expansion chip.

A lower-contrast module using only a *44780* could be used. With this option, you will need to include additional code shown as comments in the listing discussed later.

The only link between the two

Software

The object-code listing shown can be obtained as a text attachment by e-mailing jackie.lowe@rbi.co.uk. The annotated source code can be obtained on disk for £10 to cover copying, administration and postage. Send a postal order or cheque payable to Reed Business Publishing Group to Precise Clock, Jackie Lowe, Electronics World, Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS.

Please note that this listing will not be e-mailed due to network bandwidth limitations. A photocopy of the listing is available by sending £1 and an A4 self-addressed and stamped envelope to the same address.

Object code for the long-wave RDS alarm clock

```
S121F8008E00FF8640B7102486B0B71039860BB710268634B7103018CE1000CC003C45
S121F81E18ED084A18A707186F04BDFF32C605BDFFE15A26FABDFF32BDFFE1BDF97A95
S121F83CBDFF32BDFF40860CBDFF340E181F0E1F0220F91301010796532603BDF927A6
S121F85A13000806BDFCD015000813011023DC214C813C26074F5CC11826015F1A9394
S121F87855261096lB81DA260A181D0820BDF95C7C00541301020B965426071501O218
S121F896181C0820181F3480028D0220A5181C0008181D001018A60085032613181C7F
S121F8B40010181D000818A600850326047F005739841B9157270597577F00587C0072
S121F8D2589658810326EB9657800926037EF9504A26037EF97680072603 7EF92E4AD4
S121F8F026D2130108lD1301101912012007140160862820451201400515012020F325
S121F90E15014020EE8D1215010218lF082005181D082039181C0820391501AD7F00EB
S121F92C59391301080E130110051501102 00A14011020058DE51401081501208 60CE3
S121F94A97531401013912012057120104121201020786 3C97541401028DC214010467
S121F968200896548005975 42BEA8DD420A712012010140180150l2D7C00599659815E
S121F98604279E391201400E7C00559655813B2F117F0055200C7C005696568 1172FBF
S121F9A4037F00567EF9011201400B7A00552AF4863B975520EE7A00562AE9861797D4
S121F9C25620E318CE1000181D25BF7C001C961C810227013B7F001C7A00531400080 7
S121F9E07C001BD61B961D2604C1E42002C1E526E57F001B7C001F7A00547C001D96F6
S121F9FE1D810926037F001D961F813C26577F001F7C00209620811826 4B7F00207C77
S121FA1C000896088107233FC601D7087C00099609D60BC1042709C10326097D000C1C
S121FA3A2604813520028134231FC601D7097C000B960C26037C000BDC0AC10723045C
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S121FA941E4F009E003C017802F004E009C013751B1F0A3E148914E715FC100EDD4AF9
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S121FAD0423B1500808D3F20EB81C8240B130080071500808D3020E7130080051500l3
S121FAEE802003140080150001 3B9750860897519652760050240 4A800E80108087A20
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S121FBA2397900137900127900117900107900 0F79000E39DC170505843F813B22F503
S121FBC09723DC1604545454C11722E9D72496164684072 7E09725DC1504045454279l
S121FBDED6C13522D2D726840727CC970BD6154F050505970C9618843F970D7F001B8D
S121FBFC7F001CDC25DD08DC23DD1F12004006BDF913140040DC1FDD219609D60BC1BC
S121FC1A0524014AC6073DD307C30020930ADD02D60D130D202354CAF0240F96218B48
S121FC381E813B2305803C7C00229721DB222507CB18DE0209DF02C41F201F54240F17
S121FC5696218B1E813B2305803C7C00229721DB22C1172307C018DE0208DF02D7229D
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S121FD28FF40181C0420A600A710BDFF34088C003A26EC398D177EFDC2CEFFBEBDFE95
S121FD46A19656BDFF09DD2A9655BDFF09DD2C96228D0EDD359621BDFF09DD38863AD3
S121FD64973739BDFF0981302602862039 8DE2120110CAD608CEFF6E8D22DD2AA60226
S121FD82972C8620972D9730973496068DD7DD2ED604CEFF868D07DD31A6029733391B
S121FDA086033D3AEC003986209735973796 1ABDFF1AD736961B5FCE03D2028F17BD31
S121FDBEFF09DD38CC2D20D730D73413010202C62EDD2A13000111961E26081215801A
S121FDDC04C6742003BDFF1AD72A9615BDFF1ADD2C9616BDFF1ADD2E9617D635C1201D
S121FDFA260DBDFF1ADD319618BDFF1ADD3339BDFF1ADD309618BDFF1ADD3239CEFF87
S121FE18B3BDFEA1960C8B30972C960B8B30972E960B2721D60C86073DDB0B5ACEFED7
S121FE36553AE600861337C10423014CBDFF09DD30328B5FBDFEBE9609BDFF09DD3850
S121FE5439010D1909150511061202 0E1A0A16170713030F1B0B0C180814041000CE0B
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S121FE90131B020C8620161201400 3DD3739DD3439C61018CE002AA60018A700081800
S121FEAE085A26F518CE100039CEFFD18DE596548D49DD3239CEFF608DD9B610314C98
S121FECCC6C88D298D37972ED7309650260286F08B30972DB610324CC6FA8D11780023
S121FEEA50488D0F8D19DD3896508B309736393D7F0050816425077C005080642 0F57E
S121FF083916840FC4F08B0019C01025058B161920F7160D460D464444813923028B24
S121FF2607C40FCB30C139230 2CB0739863018A703181C0480181D048039181D04A0BF
S121FF44181C0440186F07181C048018A603181D04802BF3186307181D044039423A95
S121FF62202D2D2E2D2020543A202D2E2D2D2D4D6F6E547565576564546875 4672690E
S121FF8053617453756E2D2D2D4465634A616E4665624D61724170724D61794A756EB1
S121FF9E4A756C4175675365704F63744E6F764465634A616E593A202F20282D2D2DA2
S121FFBC2D2920573A2020416C61726D202D20204F6666202020536C6565702020208E
S116FFDA30206D696E2E20CE00006F00088C005A26F839AC
S113FFF0F9C5FAADF800F800F800F800F800F800C8
S9030000FC
```

boards is the four-wire connector shown in both diagrams. With the arrangement shown, this interface provides the 5V supply to the analogue board.

Two signals are returned; the demodulated radio data signal and the signal level, or RSSI. The data signal goes directly into the IRQ interrupt-request input on the *HC11*.

As edge timing is used to decode the data, a timer-input capture scheme would be more appropriate. But the IRQ alternative works as well in this application, where the required accuracy is measured in milliseconds.

The IRQ was used simply because debug hardware – an *HC11K4* running *PCbug11* – was available and it used the *K4*'s port A for the LCD.

Conditional assembly, using the *Introl* assembler, enabled differentiation between the *K4* and the intended target microcontroller, an *811E2*. The link shown on the MODB pin is to allow the use of the bootstrap mode to program the *811E2* or *711E9/20*.

If you are using bootstrap mode, remember to use a baud rate appropriate to the crystal being used. If the crystal is in a socket, it may be easier to change to an 8MHz crystal and use the standard *Pcbug11* rate of 9600 baud.

The *MC34160* is used as a 5V regulator to supply the analogue board. The regulator is switched off when the software is in standby mode. This arrangement requires a second regulator for the microcontroller and display.

If standby mode is not required then a single, simple regulator will suffice. The 10kΩ and 3.3kΩ resistors divide the battery voltage by four before the *HC11*'s a-to-d converter reads it.

As the RSSI level is always in the range 0-5V it goes directly into an a-to-d input.

How it works

Table 3 shows the various functions available in each mode via the four-key keypad. Operation of the keys and modes is derived from the RDS application described in Motorola's note AN460.[2]

The 'on/off' key uses a subroutine in my software called ONOFF to toggle between 'on' and standby. Details of how you can obtain this software are given on page 453.

Port pin PD5 controls power to the analogue section and can also switch a radio or other external hardware. In standby mode, time is displayed with the date if the alarm is disabled. If the alarm is enabled, the display shows the alarm time. In 'on' mode, the time is displayed with the current hexadecimal data. **Table 4** shows these display formats.

The 'alarm' key calls the subroutine ALARM, which displays the current alarm status. A second press changes the alarm armed status.

When the alarm is armed, the alarm time is displayed. In this mode the on/off key can be used to select either hours or minutes – indicated by flashing – and the 'sleep' and 'display' keys used to increment and decrement the settings.

The alarm display has one of the two alarm formats shown in Table 4, according to whether or not the alarm is armed. All the keys have a special function in the alarm mode. If the alarm is armed, the only way to exit this mode is to wait for a timeout. If no keys are pressed, the mode returns to normal in ten seconds.

The alarm time can be entered as described above. When the alarm is enabled, the alarm time is displayed on first press of the 'alarm' key and permanently displayed in standby mode.

If the alarm is enabled, then at the alarm time the auxiliary control line PD5 goes low, activating the sleep timer for an hour. This takes place whether the decoder was previously on, off or running the sleep timer. It has the effect of switching the auxiliary line high again an hour after the alarm time, regardless of its condition prior to the alarm.

Table 3. Four multi-purpose keys control all functions of the alarm and clock.

Mode	Key On/off	Sleep	Alarm	Display
Standby (off)	Normal mode (on)	Sleep mode (on)	Alarm mode	Data display
Normal (on)	Standby mode (off)	Sleep mode (on)	Alarm mode	Data display
Alarm (off)	Standby mode (off)	Sleep mode (on)	Alarm on mode	Data display
Alarm (on)	Alarm set-up mode	Sleep mode (on)	Alarm off mode	Data display
alarm (set-up)	Toggle hr/min	Decrement hr/min	Alarm off mode	Increment hr/min

Table 4. Display formats. In 'standby' mode, time and date are displayed, but in 'on' mode, the date is replaced by a display of the data currently being received, in hexadecimal form.

Display mode		Format
Normal (on):		`t 74D32942 19:37`
	No radio data	`- 0000 0000 0:00`
Standby (off):	Alarm Off	`Mon 29 Mar 19:37`
	No time-code block	`--- 0 --- 0:00`
	Alarm armed	`0659 Alarm 19:37`
Alarm:	Alarm off	`Alarm - off`
	Armed/set up	`Alarm - 6:59`
Sleep:		`Sleep 60 min`
Alternative displays	1	`t 74D3 2942 F 59`
	2	`Y:3/5(1995) W:22`
	3	`B: 9.0 T: 3.45`

Sleep and display

The 'sleep' key controls the sleep timer. If the decoder is in standby mode, the first press of 'sleep' switches it on and initialises the sleep time to 60 minutes. When the sleep timer is running, this is indicated by a decimal point in the second character of the display module while the display mode is 'normal'.

Subsequent presses of 'sleep' decrement the time remaining by five minutes. When the sleep time has elapsed, the decoder returns to standby mode. In the alarm set-up mode this key decrements the alarm time.

The 'display' key selects the alternative displays of transmitted data, year and week information and battery and tuning voltages. In the alarm set-up mode, this key increments the alarm time.

The 'normal' display comprises the block identifier, the data in hexadecimal form split into two groups of four digits if there is room, and the time. If the block identifier indicates a time-code block, 't' is displayed.

The 'standby' display replaces the block data with the date, as the intention is that in this mode the analogue circuitry is switched off.

The three alternative displays are available whether or not the unit is in standby mode. The first is similar to the normal display except that the time is replaced by the 'confidence' value and time seconds. When a good block is received, the confidence value is incremented up to F. If a block fails the CRC check, the value is decremented.

The second display alternative shows the year type as leap-year cycle and year starting day, the actual year and the week number. The year is assumed to be in the range 1995-2022 and is the 'week-number' year. This means that the year does not usually change at the transition between 31 December and 1 January, although it did, however, do this at the 95/96 transition. Instead, it advances to the next year when the week number goes from 52 or 53 back to 1.

While the local time offset adjusts the time and, if necessary, the date, it does not adjust the year. The method of adjusting the date can also use non-standard week numbers during the time when the local offset causes a change from 31 Dec to 1 Jan or *vice versa*. During this time, a week number of 54 or 0 is possible. These non-standard week numbers will not happen though as long as the current practice of using GMT in the winter in the UK continues.

The third display indicates battery voltage up to a maximum of 19.9V, and the SSSI level up to 4.98V.

Software

The complete source code for the software is available by post. There is only room here to show the object code.

The reset routine, START, sets up the registers and i/o ports. External interrupts are enabled on negative edges so that the signal from the demodulator can interrupt the microprocessor on each falling edge.

The real-time interrupt timer, RTI, is enabled to cause an interrupt every 133ms to run the real-time clock. Correct operation of this clock in the absence of continuous data requires that a 2.0MHz crystal be used. A trimmer on pin 7 could be added to adjust for accurate timekeeping.

The main free-running timer's prescaler is set up to divide by 1. The reset routine also enables interrupts, clears the RAM, initialises the LCD module and sets the mode to 'on' with alternative display 1. When a valid time-code block is received the mode switches to standby.

The idle loop, IDLE, uses the main free-running timer to loop at 64Hz. It regularly reads the keyboard for a key press, updates the display module, compares the current time with the alarm time and performs other time-dependent functions related to the display module and the sleep and alarm functions.

To ensure that the radio is switched on prior to a time signal, the alarm operates two seconds before the set time. This is why the displayed time is incremented by a minute before the comparison is made.

The capabilities of stopping keyboard scanning using PE7 is included in case it causes interference on a connected, or nearby, radio.

Keyboard subroutine KBD scans the four-key matrix for a key press every 16ms. If the same key is pressed on three successive scans, it executes the appropriate key function by calling the

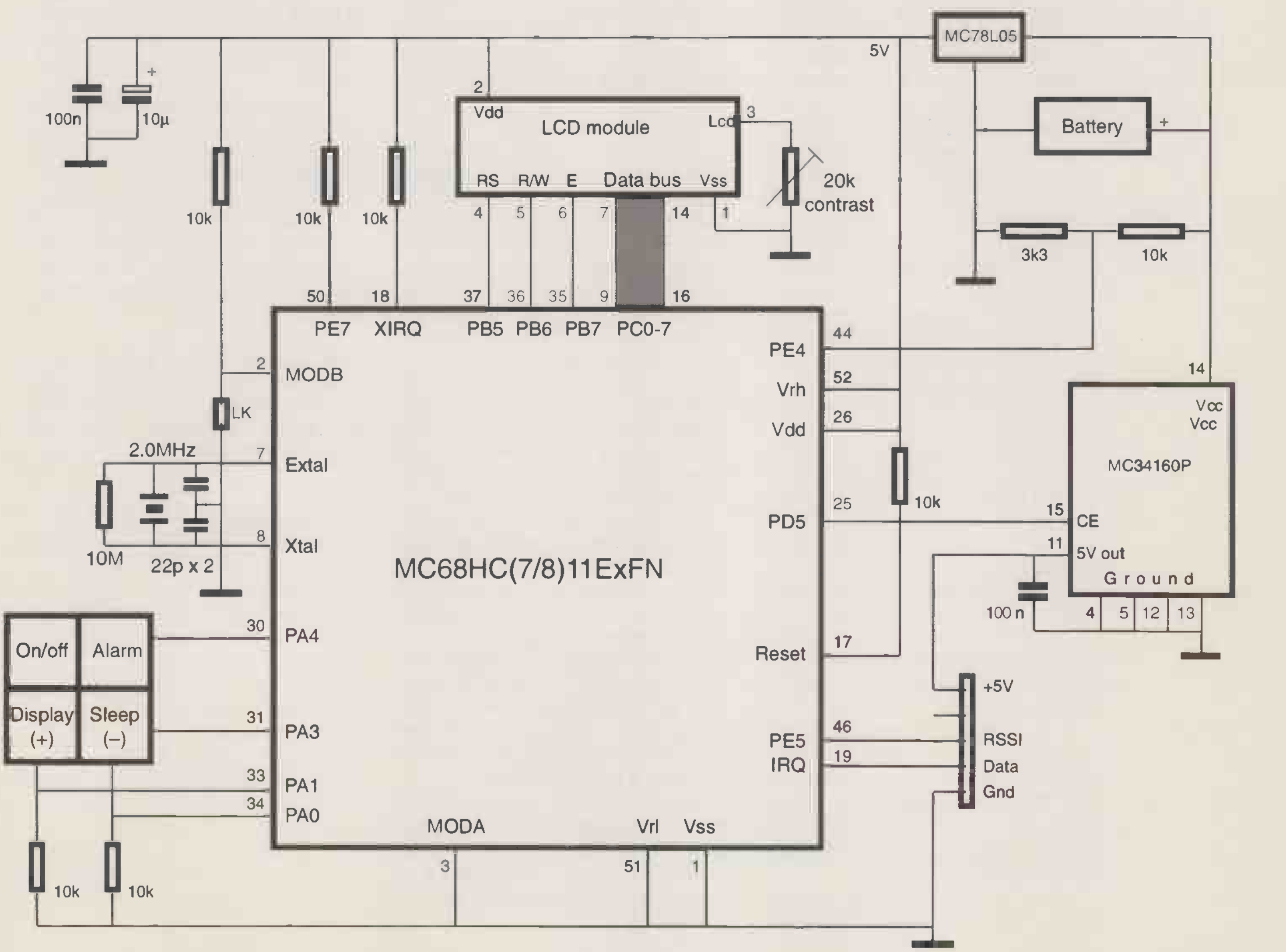


Fig. 3. The clock's digital-processing section. Although the hardware is relatively simple, the clock provides precise electronic alarm switching and displays battery status and signal level.

Table 5. Bi-phase decoding.

Previous bit	1 bit time	1.5 bit time	2 bit time
0	0	1	Illegal
1	1	00	01

relevant subroutine – ALARM, ONOFF, SLEEP or DCK. Table 3 shows the various functions available in each mode.

The timer interrupt routine TINTB decrements the sleep timer. It also updates the RAM locations used to store hours, minutes, seconds and eighths of seconds so that the time and date remain valid in the absence of regular time information.

Keeping time with no signal

As the 2.0MHz crystal used does not give exact eighth of a second ticks, the software compensates by counting 458 'eighths' of seconds in all but every ninth minute and 456 in the ninth minute.

The day of the week – and if necessary week number and year-type numbers – are also updated. This is done in case the clock is required to keep track of the date as well as the time in the absence of radio data. It is not the easiest way to organise a calendar, but it is necessary, as this is the form in which the time-code block provides the information.

There are 53 weeks if the year starting day was a Thursday or, in the case of a leap year, a Wednesday. The year starting day is incremented twice at the end of a leap year to allow for the extra day and wraps back from 7 to 1. The year type simply increments and wraps from 3 back to 0. The sequence repeats every 28 years until the year 2100 – which is not a leap year.

Hardware interrupts are vectored to jump to SDATA when a negative edge is received from the demodulator. This edge causes an interrupt and the data is calculated from the time interval from the previous edge.

The bi-phase coded data bit, or bits, also depends on the value of the previous bit, **Table 5**. The bits are shifted into a seven-byte RAM register – DAT to DAT+6 – and the matrix multiplication performed.

The state of flag STAT2,$01 determines if the multiplication is to take place after every bit or only after all 50 bits have arrived. The multiplication is performed using exclusive-or instructions for every bit.

As the bottom of the matrix, Table 2, is a unity matrix, the first 13 bits are transferred directly into the accumulators. The matrix multiplication is done in the loop MULT. This reduces the code required but increases the execution time of the algorithm.

In the source-code listing, the table B5-B1 represents the decoding matrix, Table 2. In this case the execution time penalty is not a problem as the bit rate is very low. I carried out the same procedure using in-line code in the RDS application mentioned earlier[2] as the bit rate was too high for a loop to be workable.

Because the interpretation of an edge depends on the previous bit, an error or a wrong guess at the start can cause all subsequent edges to be misunderstood. The illegal entry in the table is thus used to invert the current – perhaps the first guessed – previous bit, preventing decoding from getting stuck in this mode.

When a valid remainder is found, CONF is incremented and the 36 data bits saved in the four bytes of BLOCK. The confidence level CONF is used to decide when to switch to checking the CRC only every 50 bits. This is done once CONF has reached F_{16}, i.e. 15.

Processing valid data

If a valid block has been received, the data can be processed. A time block is used to initialise or update time, local time difference and date information. Any other block is meaningless in this application and so is displayed in its raw hexadecimal form.

The broadcast time is Universal Coordinated Time. Commonly referred to as UT0, this is effectively the same as GMT.

Time differences relative to UTC, including summer (daylight saving) time, are sent as a two's complement offset of up to ±12 hours in half-hour increments. The time block is checked before it is used although most errors should have been detected by the CRC check.

If the minutes are over 59, the hours over 23, the day-of-week a zero, etc., then the block is not used.

The first successful receipt of a time-code block after power-up or a reset switches the mode to standby, switching off the analogue section. The time data is transferred to other RAM locations for local offset adjustment and display.

After this adjustment is made the date, i.e. month and day of month, are calculated by first working out a day-of-year number and then converting to the usual month format using tables. A separate table is used for leap years.

The software drives a parallel LCD module based on an *HD44780* driver with an *HD44100* expander. Display routine MOD is executed in the idle loop if the STAT2 flag is set. It is set every 266ms by RTI timer interrupts.

The LCD module is updated with new data only if there has been a change since the last time the routine was executed. This reduces the likelihood of unnecessary i/o activity interfering with a radio.

Before anything is written to the module, the subroutine WAIT is used. This ensures that the controller in the module is not busy, as indicated by a low on bit 7 of the LCD's bus.

The listing is for use with a divide-by-8 multiplexing LCD module. To use a divide-by-16 module using only the *HD44780*, the subroutine LCD16 should be enabled.

Selecting display formats

The different display formats are selected by checking the various flags and the relevant routine executed. As the locations in RAM used for hours and minutes contain binary numbers, they are converted to ASCII BCD using the subroutine CBCD before being written to the display buffer.

If this subroutine is entered at the label SPLIT, then the data is simply split into nibbles and converted to ASCII. This is used for the display of the raw hexadecimal data. If the alarm is not armed, the standby display converts the day of the week and day of the month numbers into three character strings using the tables at the end of the listing.

Subroutine MNAME has an additional month at each end to facilitate a correct display when the local time offset causes a transition to the next or previous year.

Year and week display routine ALTD2 calculates a year in the range 1995 to 2022 from the year type (leap year) and year start day information. This is done using the table YRTAR, which consists of the offsets from the start of the 28 year cycle – arbitrarily taken to be 1995 – according to the values of year type listed down the table and year start day listed across the table. ■

Peter is currently trying to find time to write a short piece on programming the controller, which I will to publish as soon as it arrives. The process is said to be fairly straightforward – Ed.

References

1. LF Radio Data: Specification of BBC phase-modulated transmissions on long-wave, BBC, RD1984/19.
2. Application note AN460, 'An RDS Decoder using the MC68HC05E0.
3. Tadao Kasami, 'Optimum Shortened Cyclic Codes for Burst-Error Correction,' IEEE Transactions on Information Theory. April 1963, pp. 105-109.
4. M68HC11 Reference Manual (M68HC11RM/AD rev. 3).
5. M68HC11 E Series Technical Data.
6. Data sheets for the MC3371 and MC34160.
7. AEL Crystals, Module D, Genner Rd., Crawley RH10 2GA, 01293 524245 (Part No X198K000L001).

Once widely used in applications ranging from radar sets to televisions, the blocking oscillator is little remembered today. But here, Ian Hickman demonstrates that it still has its uses. His discussion includes a blocking-oscillator-based long-life emergency light using bright LEDs.

Is the blocking oscillator dead?

Back in the fifties and sixties I, like many designers, had occasion to use that very useful circuit arrangement known as the blocking oscillator. At its simplest, a blocking oscillator was just a wildly overcoupled oscillator of the Hartley variety, usually with separate feedback-coupling winding.

As normally designed, the Hartley oscillator was clean source of a continuous sinewave output. But if overcoupled, the heavy class-C operation would bias the device back to cut-off and the rf output would cease.

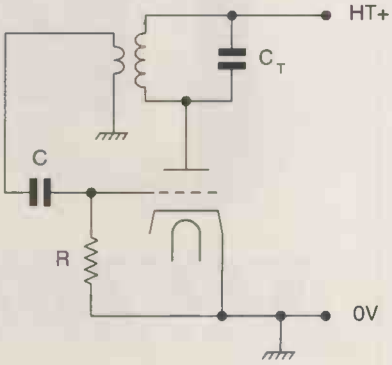


Fig. 1. Continuous-wave oscillator, squegger or blocker? It all depends.

There then followed a recovery period during which the grid bias returned to the point at which anode current could flow once more, and another burst of rf followed. This was known as a squegging oscillator, and apart from making an excellent source of general interference, it was not of a great deal of use.

If the feedback coupling were made even tighter, then the device would bias itself back, by virtue of the heavy flow of grid, gate or base current, during the very first cycle of the rf. This, then was the blocking-oscillator circuit.

The blocking-oscillator was a popular pulse generator in the days of valves, and well into the transistor era. It was described in nearly all books on electronics, and a quick trawl through my limited library turning up several articles on the topic.

If you have, or come across, any of the references 1 to 5, you can read all about it.

What is a blocking oscillator?

Figure 1 shows a valve continuous-wave oscillator, where *C* and *R* would typically be 100pF and 10kΩ. The triode might be the oscillator portion of a triode-hexode frequency changer in short, medium and long-wave table radio.

If *R* were raised to 330kΩ, then the radio would still operate normally on medium and long wave, but the oscillator would squegg at around 100kHz on short wave, due to the excessive grid-bias time constant.

This dodge was sometimes used by unscrupulous radio dealers to 'rejuvenate' a set that no longer worked well on short wave, due to tired valves. The delighted customer would find that dozens of stations could be received again on short wave – just like when the set was new.

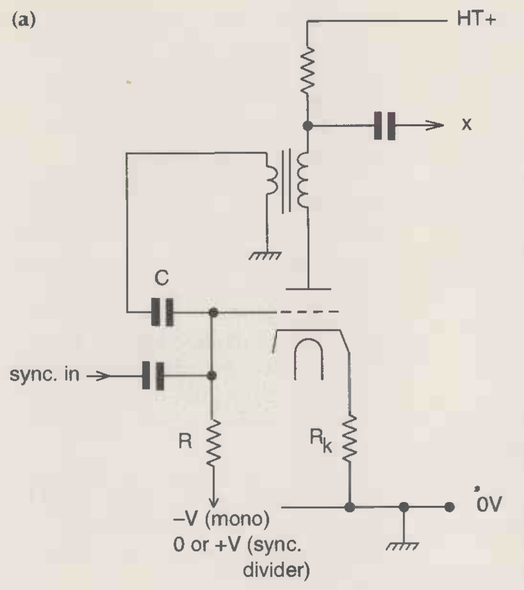
As the time constant *CR* is made longer, relative to the period of the oscillation, and the coupling of the feedback made tighter, the number of cycles in each burst of oscillation becomes smaller and smaller. Finally with very tight coupling, the circuit biases itself back to cut-off during the first cycle of oscillation following each recovery period: it becomes a relaxation oscillator.

Figure 2a) shows how the grid may

be returned to a negative voltage just below cut-off, so that the circuit is monostable. It then only responds when it receives a trigger pulse.

Another common use for the blocking oscillator was as a frequency divider, Fig. **2b**). Here, small positive-going trigger pulses of defined amplitude were applied to the grid of a blocking oscillator. The oscillator was designed to free run at just below the desired frequency, and thus fired slightly earlier when the appropriate *N*th trigger pulse appeared.

With valves running on stabilised supplies, values of *N* up to about 5 were practical. Thus with one blocking oscillator dividing by two and another by five, a double triode implemented a decade divider.



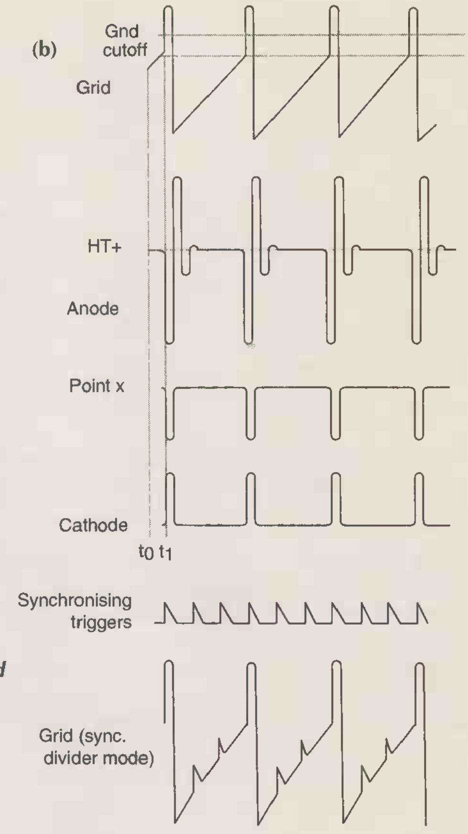


Fig. 2a) The monostable blocking oscillator may be used as a triggered pulse generator, while b) shows how the astable blocking oscillator can act as a synchronised divide-by-N stage.

Transistor blocking oscillators

Figure 3 shows the circuit of a particularly brutal transistorised version of the blocking oscillator. When the transistor cuts off, the collector voltage flies up positive, and the base voltage is driven negative.

Note that as is the common – but not invariable – practice with blocking oscillators, a closed magnetic path core was used to ensure tight coupling between the collector and base windings. In this case, the core was an *FX2754* two-hole balun core with an A_l of 3500nH/turn^2.

At switch-off, the current in the inductor cannot be instantly interrupted, and the collector voltage rises, in an attempt to maintain it. The collector voltage in fact reached +65V, higher than the minimum C_{cbo} rating of the *BC107*.

Due to the tight coupling, the voltage across the collector winding is reflected into the base winding as per the turns ratio. The base voltage reached –10V. This is well in excess of the rated V_{ebo} minimum of –6V, where it was clamped by the base emitter breakdown. Consequently, the voltage across the capacitor reached +25V before the stored energy was dissipated, the circuit recovered and the cycle repeated.

The on pulse width was 1.5µs and the off period, due to the very rapid dumping of the energy in internal breakdown of the device, was 300ns. Thus the pulse repetition frequency, or PRF, was 550kHz.

This is not a nice way to use a transistor, which is quite unlike a valve; that robust device can support enormous voltage excursions on anode and grid when cut off. The performance of the Fig. 3 circuit was therefore rendered more sanitary by connecting a diode to the collector, its cathode being returned to the +10V rail. Now, the operation of the circuit is completely changed. At no time does the voltage across the 100pF capacitor exceed +0.6V.

At 1.5µs, the on period was unchanged, but during the off period, the voltage across the collector winding was now just the small forward volt-drop of the diode. Consequently, the negative di/dt in the collector winding was also small, and the off period now extended to 15µs.

At the start of the on period, the voltage across the capacitor is driven negative, charge being drawn from it to supply the base current, charging it negative. However this source of base current soon becomes exhausted, and the available base current via the 330kΩ resistor is inadequate to keep the collector bottomed as the collector current continues to rise.

So the collector voltage starts to rise. This is reflected at the base as a negative excursion, rapidly cutting the collector current off completely. The base is now left at almost the negative voltage to which *C* was charged during the on period, since there is little voltage across the feedback winding.

The base voltage then rises, following a very linear ramp, as *C* is charged via *R*. This continues until it reaches about +0.6V, when the transistor starts to turn on and the cycle repeats.

With the circuit as described, the current in the collector winding does not quite have time to fall to zero before the base voltage reaches +0.6V and the cycle repeats. With two *1N4148* diodes in series, the higher off-period collector volts gives a larger *–di/dt*, and the voltage across the collector winding collapses from two diode drops to zero after 7µs.

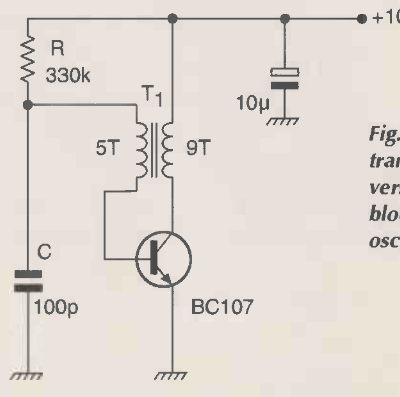


Fig. 3. A brutal transistorised version of the blocking oscillator.

Blocking-oscillator uses

Some of the blocking oscillator's uses have been mentioned already. But one characteristic of the circuit largely explains its popularity in the days of valves. For a given rail voltage, the period is determined by *C*, *R* and the transformer. In other words, it is determined by passive components of good long term stability.

The same goes for the transistorised version of Fig. 3, provided the diode is included, although the gain of the transistor has a second order effect on the period. For this reason, a popular version of the blocking oscillator for transistor applications applied the feedback

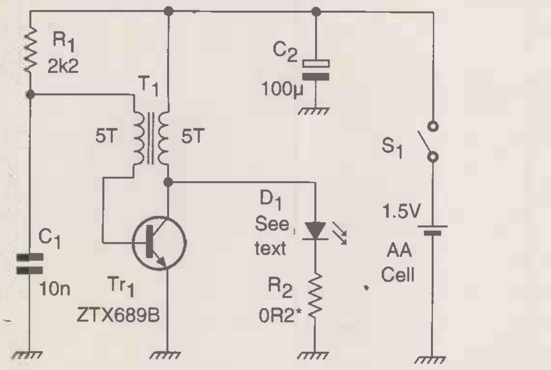


Fig. 4. Circuit of a blocking oscillator or self-excited flyback converter, arranged as a pocket emergency light.

to the emitter, using the device in the grounded base mode.

Even considering only the grounded emitter versions, however, there are various ways in which the blocking oscillator can operate. One of these, namely whether or not the current in the collector winding falls to zero in the off period, has already been mentioned. The other major factor is what causes the termination of the on period.

In the circuit of Fig. 3, it is the limited available base current. When the required collector current rises to a value beyond what this can support, the collector voltage must rise and the off transient follow. But if enough base current is available, the collector current can continue to rise until the core saturates. At this point, the voltage across the collector winding must fall.

However great $+di/dt$ may be, the increase in flux $d\phi/dt$ – and hence the back EMF – becomes negligible. In this entirely different mode of operation, the on period is determined by the core saturation characteristics.

This latter mode of operation gives a blocking oscillator which is in many ways similar to a currently much used circuit, the fly-back inverter. In the circuit of Fig. 3, with diode, instead of dumping the current back into the supply rail, the diode could be used to deliver it somewhere else. It could deliver it into a load, the other end of which is connected to ground for example.

Further, the voltage at which the energy is delivered to the load could be greater than the supply voltage: the blocking oscillator becomes a boost or flyback-inverter.

Efficient LED torch

I used a Zetex *ZTX689B* switching transistor in just such a blocking-oscillator/self-oscillating flyback inverter circuit as a handy compact emergency light. Two of these transistors were given away with the January issue of *Electronics World.*

In the interests of compactness, a single AA cell was used as the power source, and in the interests of efficiency, an LED was used as the light source.

The voltage of the cell is too low to power the LED directly. But even if two cells were used, there would be the problem of defining the current, given the variation of supply voltage over the life of the battery. The blocking oscillator action solves the problem, maintaining a constant efficiency over the supply voltage range 1.5V down to 1V.

Figure 4 shows the circuit diagram. Compared to Figure 3, the base drive resistor is very low, despite the high gain of the transistor. The reason is twofold: firstly the low supply voltage, not greatly in excess of the transistor's V_{be}, and secondly the mode of operation. This is an example of a blocking oscillator, where the on period terminates due to saturation of the transformer core.

Figure 5, lower trace shows current through the LED, monitored across a 0.2Ω resistor. Given the 20mV/division Y sensitivity, the peak current is seen to be 280mA, while its average value measured 27mA – well within the 50mA dc maximum rating of the device used.

Just before the end of the off period, LED current falls to zero. This is indicated by the small ringing on the collector voltage trace, Fig. 5, upper trace 2V/division vertical, 5µs/division horizontal.

Note that when the transistor switches off, the current continues to flow unchanged through the transistor as the collector volts rise, until the point at which the LED conducts. Thus there is a turn-off switching loss in the transistor. This is unavoidable, but small, due to the fast switching speed of the transistor, the characteristics of which were published in the January issue.

However, with the LED current having fallen to zero just before switch-on, there is no corresponding turn-on loss. Note also the transistor's very low saturation voltage – only some 200mV at 300mA collector current shown in the upper trace of Fig. 5.

The upper trace of **Fig. 6** illustrates the base voltage at 2V/division being clamped at the transistor's $V_{be(on)}$ during the active part of the cycle, and being driven to –3.8V peak at switch-off. The lower trace of Fig. 6 shows the voltage across the 10nF capacitor.

Given the transformer's 1:1 ratio, during the active part of the cycle, this voltage sits negative with respect to the base by the same voltage as appears across the collector winding. Following switch-off, the capacitor charges up via the 2.2kΩ resistor.

During the latter part of this process, the LED current having terminated, the voltage across the feedback winding is zero. So when the voltage across the 10n capacitor reaches +0.6V, the transistor turns on and the cycle repeats.

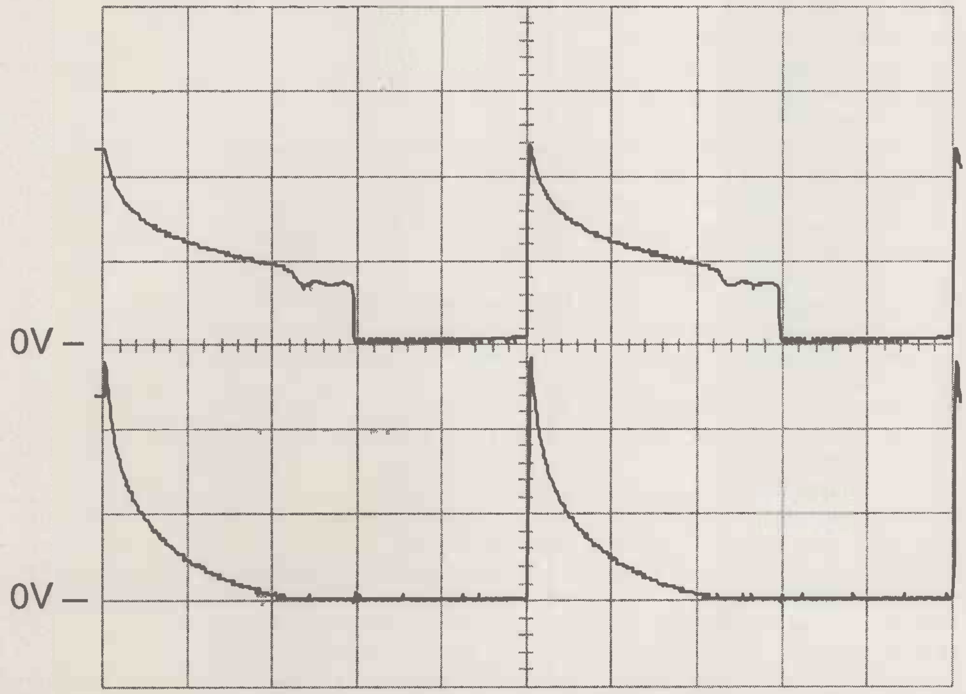


Fig. 5. Collector voltage, upper trace, 2V/div vertical, 5µs/div horizontal. Lower trace shows current through the LED, monitored across a 0.2Ω resistor, 20mV/div, 5µs/div.

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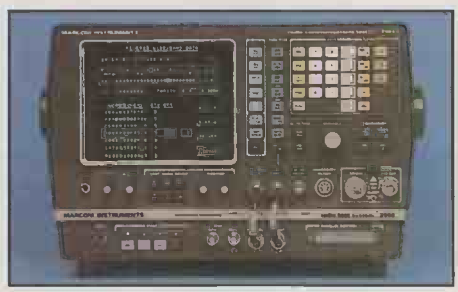

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Table 1. Comparison of three torch 'technologies' – two using LEDs, the other an incandescent lamp.

	Current	Brightness*	Power (mW)	Efficiency††
Red LED torch	91mA	100	126	0.79
Amber LED torch†	70mA	500	96	5.2
2.5V bulb torch	250mA	8500	643	13.2

† at 1.37V – the AA cell being used was not new.
* EAU, equivalent arbitrary units. 100 = full scale on range 1 – the most sensitive – range 2 has a tenth of the sensitivity, range 3 one hundredth, etc.
†† Relative values, calculated as EAU/mW.

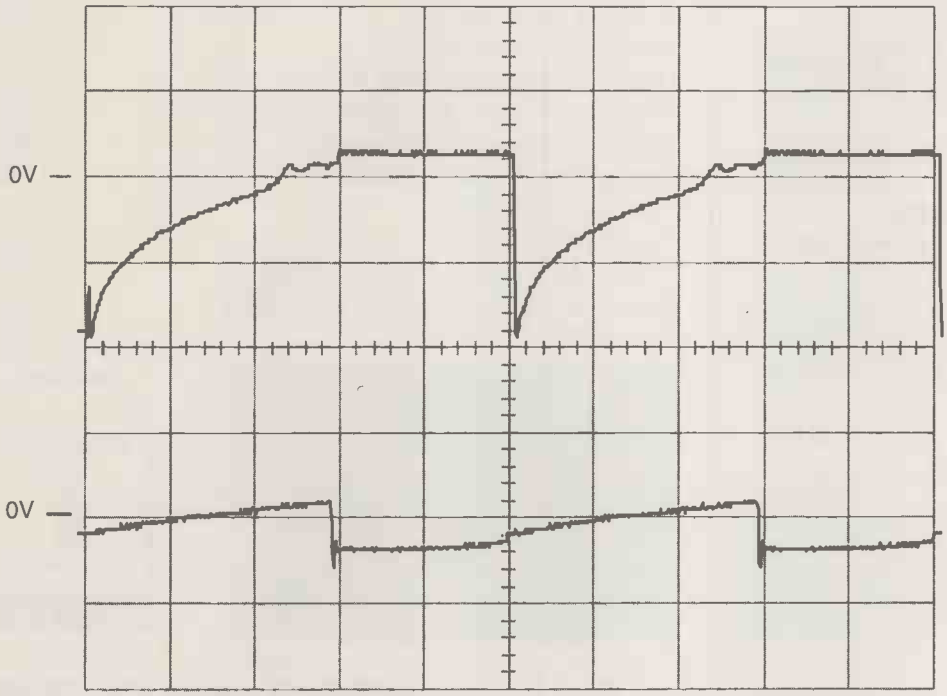

Fig. 6. Base voltage, 2V/div vertical, 5μs/div horizontal, lower trace and voltage across the 10nF capacitor, upper trace, 2V/div, 5μs/div.

TLOH 190P amber coloured LED, a InGaAlP device with a very narrow beamwidth of less than 10° at half intensity. The on-axis luminous intensity of this is rated as 20000mcd typical – 8500mcd minimum – at 20mA.

I constructed an earlier version of the torch in one of the small transparent plastic boxes used by semiconductor manufacturers for supplying samples. However, 'transparent' is a relative term, and tests with my light meter[6] showed that although water clear to look at, such a box passed only about 90% of the available light. So the new version was built in a similar box – black, as it happens – but with the lens body of the device projecting through a hole in the end of the box.

I carried out some simple tests with the light meter, to compare the new version as per Fig. 4 with two earlier torches. One of the earlier designs used a red LED rated at 3000mcd at 20mA, the other had two NiCd C-type cells and a 2.5V 250mA prefocus bulb.

The tests were carried out with the three torches, each at 1m from the lightmeter, and the results are in **Table 1**. Performance of the amber LED torch with supply voltage is shown in **Table 2**. You can see that at 1.0V, the unit provided 57% of the light for 51% of the power, compared with a supply voltage of 1.5V

Finding a matching hat

The results quoted above should be interpreted with caution, for the light meter was fitted with an unfiltered silicon photodiode detector. For true photometric measurements, indicating apparent brightness to the human eye, a photometric filter would be needed. This has a greenish tinge when viewed against daylight, and so the red LED torch would have fared somewhat worse.

But some conclusions can be drawn. For efficiency, the incandescent bulb wins hands down – at least with fresh batteries. But to get that efficiency, you have to supply over half a watt. Scaling down lamp performance is simply not possible.

It is very difficult to obtain any reasonable bulb efficiency at much less than 250mA. Thus while the amber torch gives only one seventeenth of the brightness at one seventh of the power, you would get even less light than the amber LED gives if you tried to run a filament bulb at 96mW.

Furthermore, as shown above, the light output of the LED torch is proportional to the power drawn. But with the conventional torch, as the battery voltage falls, the lamp dims very rapidly. The cooler filament not only emits less light, but its resistance falls, so the current does not fall in proportion to the reduction in voltage. The result is a drastic reduction in both light output and efficiency as the battery ages.

There is a wide choice of LEDs for a small torch of the type described. If brightness is the chief criterion, a LED such as the Toshiba *TLOH 190P* or a high brightness type from another manufacturer is ideal. However, these devices concentrate the available light into a very narrow beam. If total light output, measured in lumens, is more important than brightness, measured in candelas, then a high-efficiency LED is more appropriate. Hewlett-Packard's *HPWT-DL00* is a good example.

On this basis, the red-LED torch described was not so poor as might seem from the results. Its beam was a good deal broader than that of the amber LED, so its total light output, relative to the amber LED with its narrow beam, was probably not inferior.

But comparing total light output between devices is a much more complex task than merely comparing brightness, and quite beyond the capability of my equipment. ■

Table 2. Benefits of using a LED relative to using an incandescent lamp become clear when battery voltage starts to fall. These figures are for the amber LED torch.

Supply	Current drawn	Power	Light out*	Light/power
1.5V	72mA	108mW	35	0.32
1.0V	55mA	55mW	20	0.36

References

1. Ridenour, L N, 'Radar System Engineering,' McGraw-Hill 1947.
2. Williams, E, 'Thermionic Valve Circuits,' Pitman 1955.
3. F E Terman, F E, 'Electronic and Radio Engineering,' McGraw-Hill 1955.
4. 'The Encyclopaedia of Radio and Television,' Odhams 1957.
5. Martin Jr., T L, 'Electronic Circuits,' Prentice Hall 1959.
6. Hickman, I, A look at light, *Electronics World*, June 1997, pp. 466-471.

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Switch position 1

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Input resistance	1MΩ – i.e. oscilloscope i/p
Input capacitance	40pF+oscilloscope capacitance
Working voltage	600V DC or pk-pk AC

Switch position 2

Bandwidth	DC to 150MHz
Rise time	2.4ns
Input resistance	10MΩ ±1% if oscilloscope i/p is 1MΩ
Input capacitance	12pF if oscilloscope i/p is 20pF
Compensation range	10-60pF
Working voltage	600V DC or pk-pk AC

Switch position 'Ref'

Probe tip grounded via 9MΩ, scope i/p grounded

CIRCUIT IDEAS

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Hysteresis in a digital circuit

It may be useful to arrange digital hysteresis, whereby an event occurs at a certain digital input number in an 'upward' direction and at a lower digital input in the reverse direction; digital hysteresis, in fact.

This circuit performs that function.

Imagine that input nibble A_{1-4}, i.e. DA, to the *4019* quad switch is fixed at eight, say and the input on B_{1-4}, i.e. DB, is six.

When the input nibble DI at the top of the diagram is 0, o/p OUT12 of the *4585* comparator is high. On the switch, select inputs G_1 and G_2 are 1 and 0 respectively, so nibble DA, i.e. 8, is fed to the comparator's B input nibble.

When the input counts reaches 8, OUT12 goes low. Now DB is feeding the comparator so OUT12 only goes high again when input DI decreases to less than DB – i.e. 6.

Figure 2 shows the timing involved.

W Dijkstra
Waalre
The Netherlands
C67

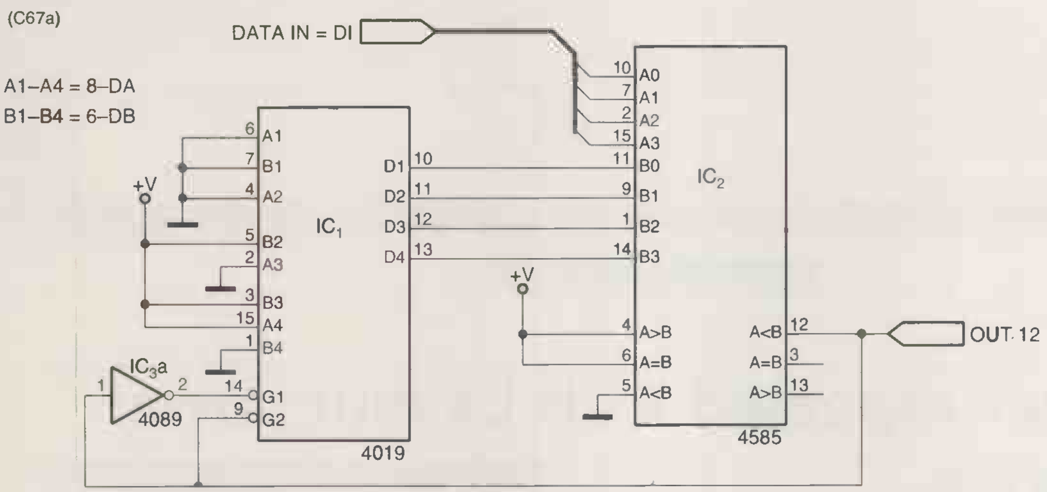

Fig.1. Digital circuit changes state at one count going up and at a lower count coming down – 8 and 6 as shown here. It is a form of digital hysteresis.

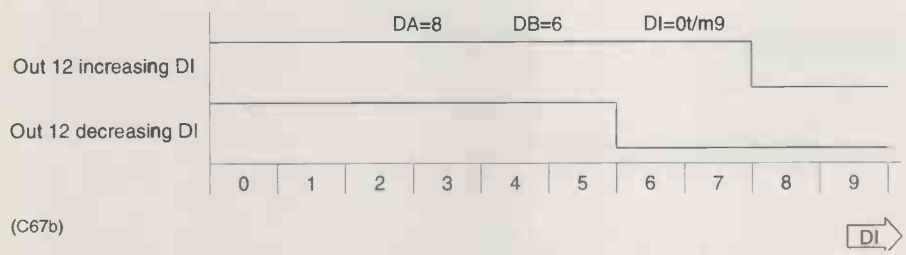

Fig.2. Timing diagram of the hysteresis switch, with switching points at 6 and 8.

Fact: most circuit ideas sent to *Electronics World* get published

Like life, *Electronics World* may seem surreal at times, but it is certainly not exclusive. Clearly, the best circuit ideas are ones that save time or money, or stimulate the thought process. This includes the odd solution looking for a problem – provided it has a degree of ingenuity.

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Clear hand-written notes on paper are a minimum requirement: disks with separate drawing and text files in a popular form are best – but please label the disk clearly.

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Programmable precise one-shot covers microseconds to hours

Listing for a PIC-based one shot that provides precise programmable pulse widths anywhere between 9µs and three hours long.

Traditional one-shot circuitry uses a resistor and a capacitor to determine the pulse width.

If the capacitor is fixed, a potentiometer can adjust the width within a certain range. For a longer pulse width, the capacitor becomes bulky and its leakage current could be an issue.

Figure 1 circuit uses a *PIC16C84* to form a one-shot. Not only can the pulse width be programmed from 9µs to more than 3 hours, but it also maintains high accuracy – an error of less than 0.3% within a –20°C to 85°C temperature range.

Since the *PIC16C84* has built-in EEPROMs, The pulse width information is stored in the PROM and is retrieved at power on.

An input trigger signal generates an interrupt for the microcontroller. In the interrupt service routine,PB5 is set to high before going into a delay loop. In the delay loop, a 32-bit counter that is formed by four 8-bit registers must decrease to zero before PB5 is set to low and then returns. Thus, the larger the number in the 32-bit counter, the wider the output pulse will be. The pulse width in

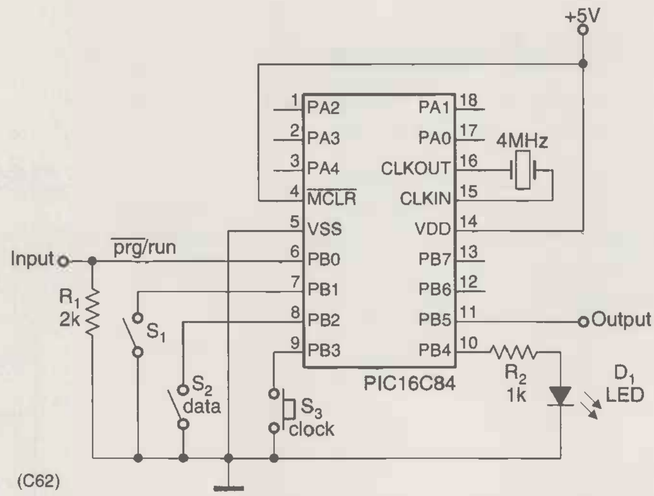
```
LIST   p=16C84
#include "P16C84.INC"
cnt_1     equ      0x10           ;
cnt_2     equ      0x11           ;
data_1    equ      0x12           ;
data_2    equ      0x13           ;
data_3    equ      0x14           ;
data_4    equ      0x15           ;
bit_num   equ      0x16           ;
temp_1    equ      0x17           ;
temp_2    equ      0x18           ;
temp_3    equ      0x19           ;
temp_4    equ      0x1a           ;
temp_5    equ      0x1b           ;

org       0x0      ;
          goto     main           ;
          org      0x4            ;
          bsf      PORTB, 5       ;
loop      decfsz   temp_1, F      ;
          goto     loop           ;
          decfsz   temp_2, F      ;
          goto     loop           ;
          decfsz   temp_3, F      ;
          goto     loop           ;
          decfsz   temp_4, F      ;
          goto     loop           ;
          bcf      PORTB, 5       ;
          movf     data_1, W      ; re-load data
          movwf    temp_1         ;
          incf     temp_1, F      ;
          movf     data_2, W      ;
          movwf    temp_2         ;
          incf     temp_2, F      ;
          movf     data_3, W      ;
          movwf    temp_3         ;
          incf     temp_3, F      ;
          movf     data_4, W      ;
          movwf    temp_4         ;
          incf     temp_4, F      ;
          bcf      INTCON, INTF   ;
          retfie                  ;
                                  ;
main                              ;
          clrf     PORTA          ;
          clrf     PORTB          ;
          bsf      STATUS, RP0    ; bank 1
          movlw    0x40           ;
          option                  ;
          movlw    0x00           ;
          movwf    TRISA          ;
          movlw    0x0f           ;
          movwf    TRISB          ;
          movlw    0x10           ;
          movwf    INTCON         ;
          bcf      STATUS, RP0    ; bank 0
          clrf     EEADR          ;
          bsf      STATUS, RP0    ; bank 1
          bsf      EECON1, RD     ;
          bcf      STATUS, RP0    ; bank 0
          movf     EEDATA, W      ; read data_1 from eeprom
          movwf    data_1         ;
          movwf    temp_1         ;
          incf     temp_1, F      ;
          incf     EEADR, F       ;
          bsf      STATUS, RP0    ; bank 1
          bsf      EECON1, RD     ;
          bcf      STATUS, RP0    ; bank 0
          movf     EEDATA, W      ; read data_2 from eeprom
          movwf    data_2         ;
          movwf    temp_2         ;
          incf     temp_2, F      ;
          incf     EEADR, F       ;
          bsf      STATUS, RP0    ; bank 1
          bsf      EECON1, RD     ;
          bcf      STATUS, RP0    ; bank 0
          movf     EEDATA, W      ; read data_3 from eeprom
          movwf    data_3         ;
          movwf    temp_3         ;
          incf     temp_3, F      ;
          incf     EEADR, F       ;
          bsf      STATUS, RP0    ; bank 1
          bsf      EECON1, RD     ;
          bcf      STATUS, RP0    ; bank 0
          movf     EEDATA, W      ; read data_4 from eeprom
          movwf    data_4         ;
          movwf    temp_4         ;
          incf     temp_4, F      ;
                                  ;
loop_1                            ; endless loop
          bsf      INTCON, GIE    ;
          btfsc    PORTB, 1       ;
          goto     loop_1         ;
          call     dly_1          ;
          btfsc    PORTB, 1       ;
          goto     loop_1         ;
prog                              ; programming routine
          bcf      INTCON, GIE    ;
          clrf     bit_num        ;
          bsf      PORTB, 4       ; flash once
          call     dly_1          ;
          bcf      PORTB,4        ;
          call     dly_1          ;
          clrf     data_1         ;
          clrf     data_2         ;
          clrf     data_3         ;
          clrf     data_4         ;
loop_2                            ;
          btfsc    PORTB, 1       ;
          goto     finish_prg     ;
          btfsc    PORTB, 3       ;
          goto     loop_2         ;
          call     dly_1          ;
          btfsc    PORTB, 3       ;
          goto     loop_2         ;
shift                             ;
          movlw    0x08           ;
          subwf    bit_num, W     ;
          btfss    STATUS, C      ;
          goto     shift_1        ;
          movlw    0x10           ;
          subwf    bit_num, W     ;
          btfss    STATUS, C      ;
          goto     shift_2        ;
          movlw    0x18           ;
          subwf    bit_num, W     ;
          btfss    STATUS, C      ;
          goto     shift_3        ;
          goto     shift_4        ;
shift_1                           ; load into data_1
          bcf      STATUS, C      ;
          btfsc    PORTB, 2       ;
          bsf      STATUS, C      ;
          rlf      data_1, F      ;
          goto     finish_sft     ;
shift_2                           ; load into data_2
          bcf      STATUS, C      ;
          btfsc    PORTB, 2       ;
          bsf      STATUS, C      ;
          rlf      data_2, F      ;
          goto     finish_sft     ;
shift_3                           ; load into data_3
          bcf      STATUS, C      ;
          btfsc    PORTB, 2       ;
          bsf      STATUS, C      ;
          rlf      data_3, F      ;
          goto     finish_sft     ;
shift_4                           ; load into data_4
          bcf      STATUS, C      ;
          btfsc    PORTB, 2       ;
          bsf      STATUS, C      ;
          rlf      data_4, F      ;
finish_sft                        ;
          incf     bit_num, F     ;
          bsf      PORTB, 4       ; flash once
          call     dly_1          ;
          bcf      PORTB,4        ;
          call     dly_1          ;
loop_3                            ;
          btfsc    PORTB, 1       ;
          goto     finish_prg     ;
          btfss    PORTB, 3       ;
          goto     loop_3         ;
          call     dly_1          ;
          btfss    PORTB, 3       ;
          goto     loop_3         ;
          goto     loop_2         ;
finish_prg                        ;
          movf     data_1, W      ;
          movwf    temp_1         ;
          incf     temp_1, F      ;
          movwf    EEDATA         ;
          clrf     EEADR          ;
          call     write_eeprom   ;
          movf     data_2, W      ;
          movwf    temp_2         ;
          incf     temp_2, F      ;
          movwf    EEDATA         ;
          incf     EEADR, F       ;
          call     write_eeprom   ;
          movf     data_3, W      ;
          movwf    temp_3         ;
          incf     temp_3, F      ;
          movwf    EEDATA         ;
          incf     EEADR, F       ;
          call     write_eeprom   ;
          movf     data_4, W      ;
          movwf    temp_4         ;
          incf     temp_4, F      ;
          movwf    EEDATA         ;
          incf     EEADR, F       ;
          call     write_eeprom   ;
          movlw    0x03           ;
          movwf    temp_5         ;
flashes                           ; flash 3 times
          bsf      PORTB, 4       ;
          call     dly_1          ;
          bcf      PORTB, 4       ;
          call     dly_1          ;
          decfsz   temp_5, F      ;
          goto     flashes        ;
          goto     loop_1         ;
dly_1                             ; delay 0.2 seconds
          clrf     cnt_1          ;
          clrf     cnt_2          ;
lp_1      decfsz   cnt_1, F       ;
          goto     lp_1           ;
          decfsz   cnt_2, F       ;
          goto     lp_1           ;
          return                  ;
write_eeprom                      ;
          bsf      STATUS, RP0    ; bank 1
          bsf      EECON1, WREN   ; enable to write eeprom
          movlw    0x55           ;
          movwf    EECON2         ;
          movlw    0xaa           ;
          movwf    EECON2         ;
          bsf      EECON1, WR     ; start write
write_dly                         ;
          btfsc    EECON1, WR     ;
          goto     write_dly      ;
          bcf      STATUS, RP0    ; bank 0
          return                  ;
                                  ;
          end                     ;
```

microseconds can be calculated using,

3*data_1+770*data_2+197,122*data_3+50,463,234*data_4+9

The minimum pulse width of 9µs happens when all four registers are set to zero. The maximum pulse width occurs when four registers are all set logic high, which is about 3 hours 35 minutes and 19 seconds.

Three pins of the microcontroller are used to program the pulse width. PB1 selects either programming or normal one-shot function. Port PB2 is the data input and PB3 is the programming clock input.



(C62)

Once PB1 is connected to the ground, a LED flashes once to indicate that all registers are cleaned up and programming starts. The 32-bit counter number is programmed into the microcontroller in a serial format with the lowest bit first.

For instance, assume the number is 00000000 00000000 10000000 00000000. First of all, connect PB2 to the ground. Then push the button on PB3 15 times.

Note that each time the button is pushed, the LED flashes once to show that one bit of the data is accepted.

The next step is to release PB2 from ground. Since the microcontroller has built-in pull-up resistors, PB2 will become logic high.

Push the button one more time and the 16th bit – logic high – will be sent. It is not necessary to program the rest of the bits since they are all zeros.

The last step is to release PB1 from ground. The LED will then flash three times to indicate the programming is finished and data have been stored into the EEPROM.

Yongping Xia
Torrance, CA
USA
C62

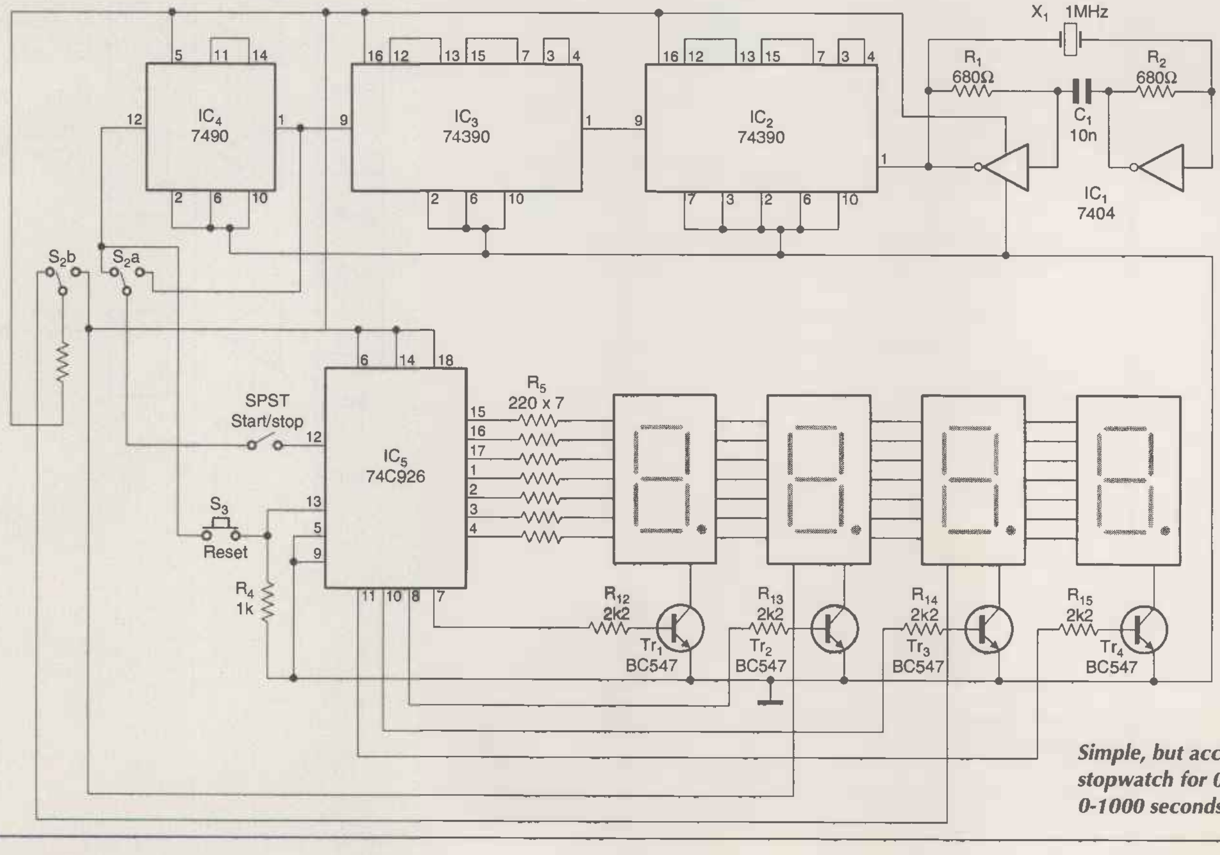
Accurate stopwatch measures to within 0.01s

To crystal accuracy, this circuit measures time to a resolution of 0.01s or 0.1s on 100s or 1000s ranges.

A 1MHz crystal oscillator drives a chain of two *74390* dual decade counters and a single 7490 decade, a switch selecting the latter to give a total division of 10^4 or 10^5, i.e. 100Hz or 10Hz.

The selected output of the divider chain is counted in the 4-digit counter, which provides a multiplexed seven-segment display driver for low power consumption.

Raj K Gorkhali
Katmandu
Nepal, C51



Simple, but accurate stopwatch for 0-100 or 0-1000 seconds.

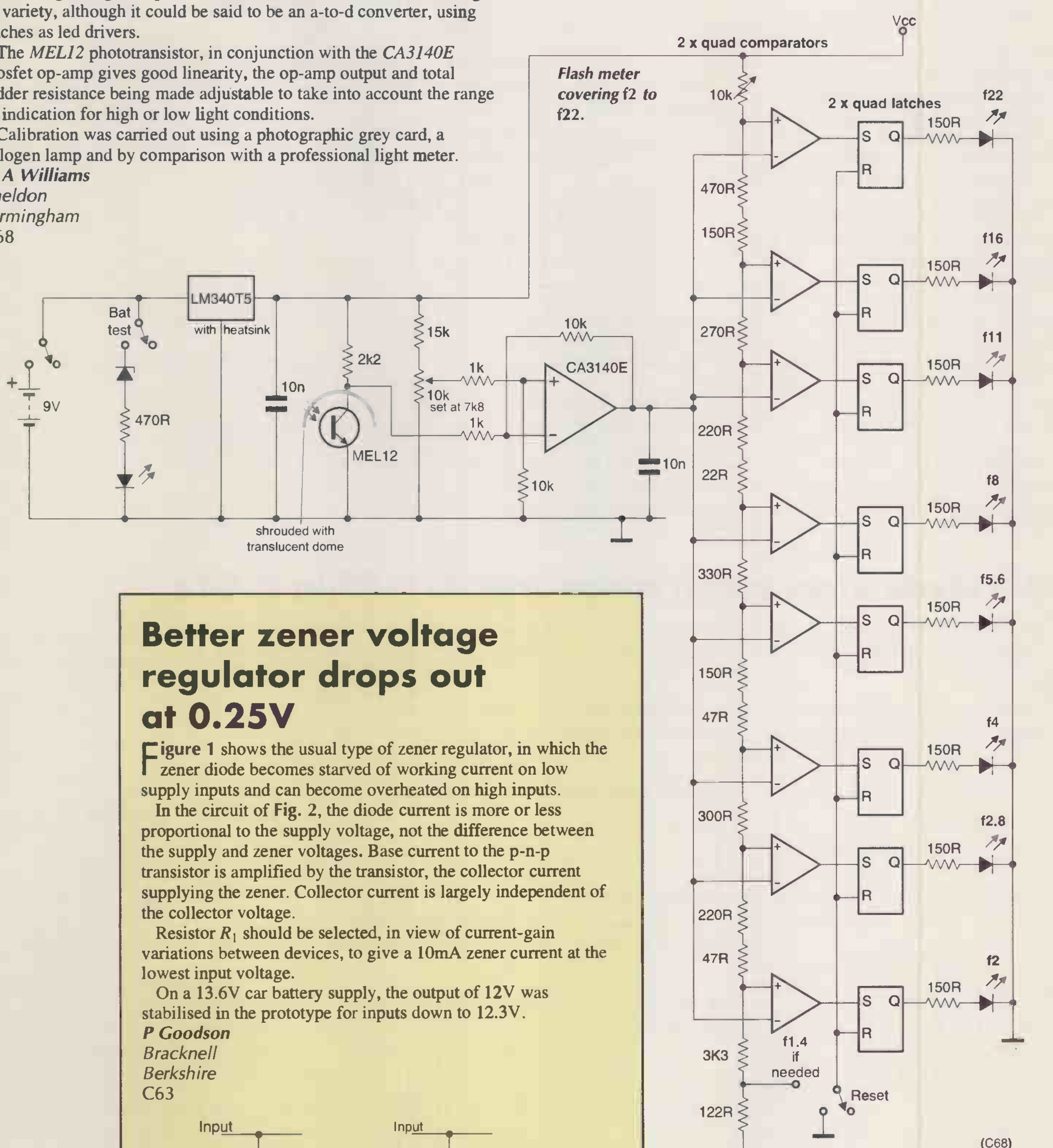
Photographic flash meter

Providing an eight-stop indication, this flash meter is of the analogue variety, although it could be said to be an a-to-d converter, using latches as led drivers.

The *MEL12* phototransistor, in conjunction with the *CA3140E* mosfet op-amp gives good linearity, the op-amp output and total ladder resistance being made adjustable to take into account the range of indication for high or low light conditions.

Calibration was carried out using a photographic grey card, a halogen lamp and by comparison with a professional light meter.

D A Williams
Sheldon
Birmingham
C68



***Flash meter covering** f2 **to** f22.*

Better zener voltage regulator drops out at 0.25V

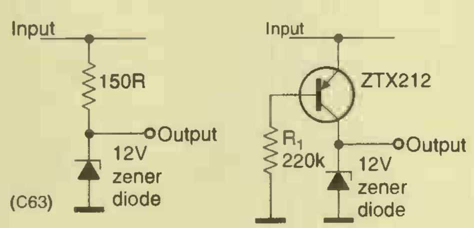
Figure 1 shows the usual type of zener regulator, in which the zener diode becomes starved of working current on low supply inputs and can become overheated on high inputs.

In the circuit of **Fig. 2**, the diode current is more or less proportional to the supply voltage, not the difference between the supply and zener voltages. Base current to the p-n-p transistor is amplified by the transistor, the collector current supplying the zener. Collector current is largely independent of the collector voltage.

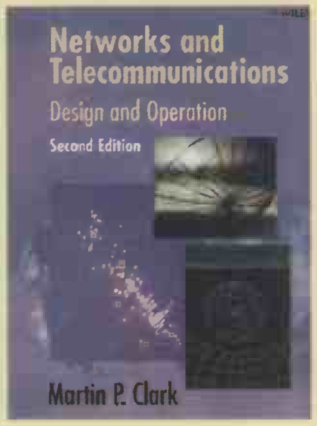
Resistor R_1 should be selected, in view of current-gain variations between devices, to give a 10mA zener current at the lowest input voltage.

On a 13.6V car battery supply, the output of 12V was stabilised in the prototype for inputs down to 12.3V.

P Goodson
Bracknell
Berkshire
C63



Three-component voltage regulator has a drop-out voltage of only 0.25V.



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Yoshihiko Akaiwa is a leading researcher in the digital mobile communication field. Currently a professor at Kyushu University, he worked as a researcher for over twenty years at the NEC Corporation

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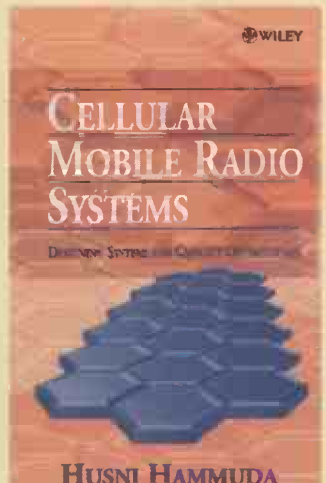

the evaluation of combinations of modulation and multiple access techniques
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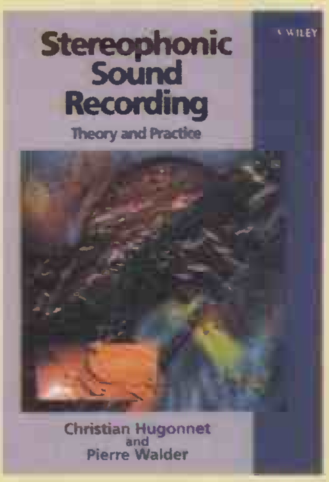

engineering theory.

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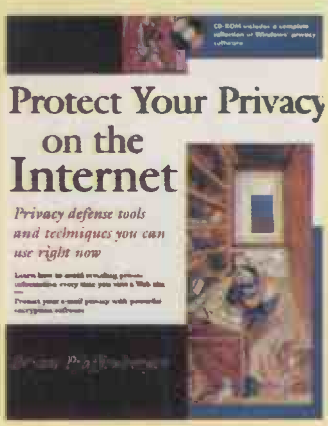

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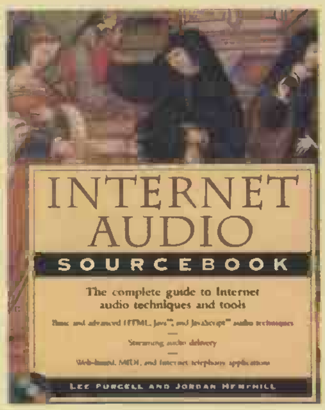

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Lee Purcell and Jordan Hemphill

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Web Security Sourcebook

A Complete Guide to Web Security Threats and Solutions

Aviel D. Rubin, Daniel Geer, and Marcus J. Ranum

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Bryan Hart explains the Early effect – an important phenomenon not always well understood by analogue circuit designers.

Early definition

What is a reasonable estimate for the maximum theoretical small-signal, low-frequency voltage gain that can be obtained with a single low-power silicon bipolar junction transistor (bjt) operating at room temperature in the common-emitter configuration?

To be able to answer that question with confidence you will need to know about a parameter that, in my opinion, has not been covered sufficiently well in the general literature of circuit engineering. This parameter, which usually appears as if by magic, is the 'Early voltage'.[1]

This pair of articles sets out to remedy this situation. The first article introduces a coherent explanation of the origin of this parameter and its role in device characterisation and modelling.

The second article, to be published later, considers its importance in the design of a range of widely used analogue circuits. These include the common-emitter and common-base configurations, the current mirror and the long-tailed pair.

Early origins

Figure 1a) shows a low power n-p-n silicon bjt biased for analogue operation and Fig. **1b)** shows a schematic cross-section of it. For clarity, this greatly exaggerates the width of the base compared with the widths of the emitter and collector regions.

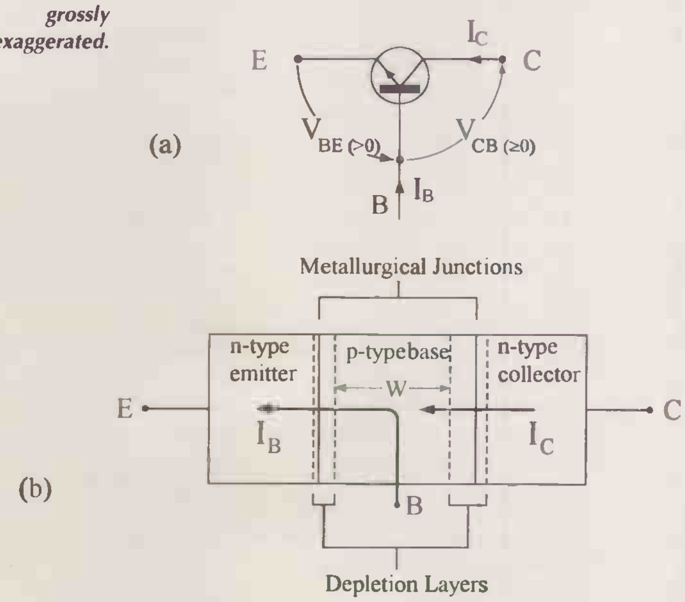

Fig. 1a). An n-p-n bipolar transistor biased for analogue operation and b), idealised cross-section of the device – base width grossly exaggerated.

Layers depleted of mobile charge carriers exist near the metallurgical junctions, i.e., where the doping polarity changes from p to n and *vice-versa*. In the absence of externally applied junction voltages these layers establish themselves to ensure that the net current flowing across each junction is zero.

The application of external bias voltages V_{BE} and V_{CB} changes the widths of these layers and the densities of minority carriers at their boundaries. The way that the resulting terminal currents are related to these changes can be deduced from an extension of the work of Moll and Ross.[2] They were the first to consider the transport of minority carriers across the base of a bipolar transistor with arbitrary base doping.

Assuming zero recombination of minority carriers crossing the base and operation with V_{BE} greater than 100mV, it can be shown that,

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \qquad (1a)$$

where,

$$I_S = \frac{K_B}{Q_B} \qquad (1b)$$

In these equations, K_B is the product of the diffusion constant in the base and the squares of the electronic charge, the emitter area and the intrinsic carrier concentration. It is independent of current but dependent on temperature.

The parameter Q_B is the magnitude of the charge associated with the net number of acceptor impurities contained within the effective base width, W, and is thus a function of the doping process.

Parameter V_T is the thermal voltage, i.e. kT/q, k being Boltzmann's constant, q the magnitude of the charge on an electron, T the absolute temperature in kelvin (°C+273); at room temperature, V_T is around 25mV and this is the value assumed throughout this article.

Equation (1) is valid provided the total minority carrier charge in transit across the base is much less than Q_B – the 'low-level injection' condition. The neglect of base region recombination is normally valid for a modern low power bjt. This is because the base width and doping levels are such that the transit time of minority carriers across the base is negligible compared with the time taken for a carrier to recombine in it.

The same is not necessarily true for high power transistors having relatively wide bases and it certainly was not true for alloy junction transistors.

If base region recombination is neglected how does a finite base current arise? The answer is, solely from holes injected from the base into the emitter. The equation for I_B is similar to that for I_C, the differences being that K_B and Q_B are replaced by their emitter counterparts K_E, Q_E.

Thus,

$$I_B = \frac{K_E}{Q_E}\exp\left(\frac{V_{BE}}{V_T}\right) \quad (2)$$

The common-emitter direct current gain is β and from eqns (1) and (2),

$$\beta = \frac{I_C}{I_B} = \frac{K_B Q_E}{K_E Q_B} \quad (3)$$

How we proceed from this point depends on the assumptions made for Q_B. A first-order model of the bipolar transistor assumes Q_B to be constant, independent of V_{CB}, for a fixed V_{BE}. A second-order model, considered from now on, takes into account the dependence of Q_B on V_{CB}.

The physical mechanism is this. The collector and base doping profiles fix the electrostatic field in the collector depletion layer. An increase in V_{CB} – dimensionally, the product field multiplied by distance – can only be accommodated by an increase in junction layer width. This is at the expense of base width ('base-width modulation') and a reduction in Q_B.

Referring to eqn (1), this leads to an increase in I_C. Since I_B does not change – K_E, Q_E are not dependent on V_{CB} – this means β increases with V_{CB}.

The effect is quantified by taking logarithms of each side of eqn (1) and then differentiating with respect to V_{CB}.

$$\frac{1}{I_C}\times\frac{dI_C}{dV_{CB}} = -\frac{1}{Q_B}\times\frac{dQ_B}{dV_{CB}} \quad (4)$$

When V_{CB} increases by an increment δV_{CB}, Q_B decreases by the same amount that the depletion layer charge Q_D increases: thus,

$$\delta Q_B = -\delta Q_D \quad (5a)$$

But, the collector depletion layer capacitance C_{JC} is defined by,

$$C_{JC} = \frac{dQ_D}{dV_{CB}} \quad (5b)$$

Hence, from eqns (4), (5),

$$\frac{1}{I_C}\times\frac{dI_C}{dV_{CB}} = \frac{C_{JC}}{Q_B} \quad (6)$$

Considering conditions at V_{CB}=0, for which $Q_B=Q_{B0}$, $I_S=I_{S0}$, $I_C=I_C(0)$, $\beta=\beta_0$, $C_{JC}=C_{JC0}$, we attach a meaning to the right hand side of eqn (6) by making the following definition,

$$V_A = \frac{Q_{B0}}{C_{JC0}} \quad (7)$$

Furthermore, dV_{CB}/dI_C is identified as the incremental resistance r_o.

Now, eqn (6) can be re-written,

$$I_C(0)r_o = V_A \quad (8)$$

I will now show this result graphically.

Characteristics and models

Figure 2 is a sketch of the observed characteristics of a bjt. The bold lines, for V_{CB} zero or greater than 0, correspond to the region under discussion; the feint lines, for V_{CB} less

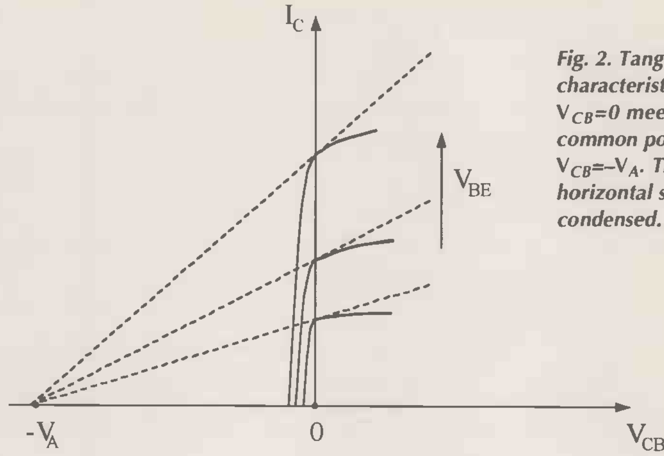

Fig. 2. Tangents to the characteristics at V_{CB}=0 meet at a common point, V_{CB}=–V_A. The horizontal scale is condensed.

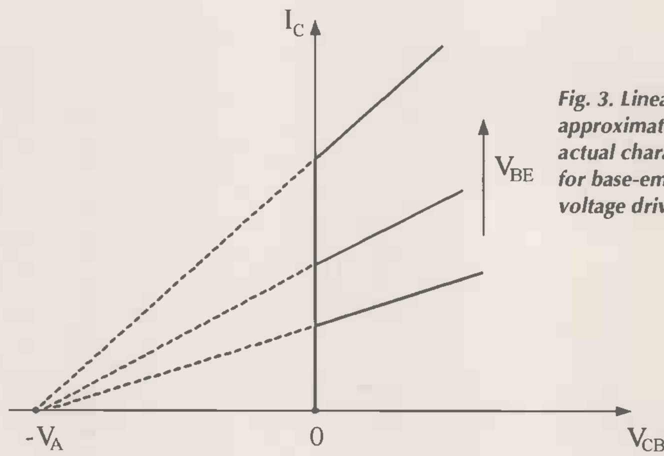

Fig. 3. Linearised approximation to actual characteristics for base-emitter voltage drive.

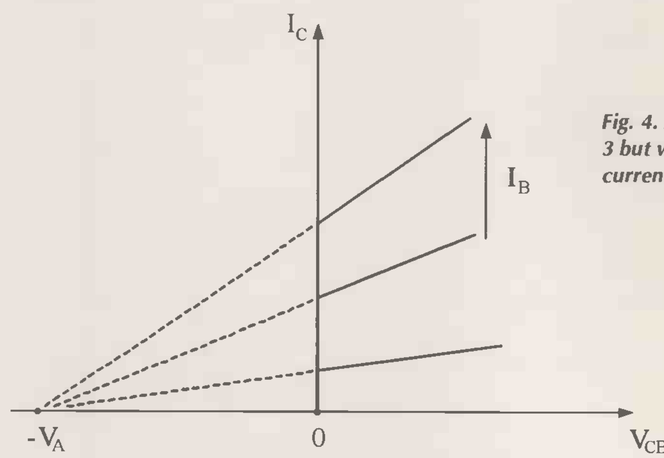

Fig. 4. As for Fig. 3 but with base current drive.

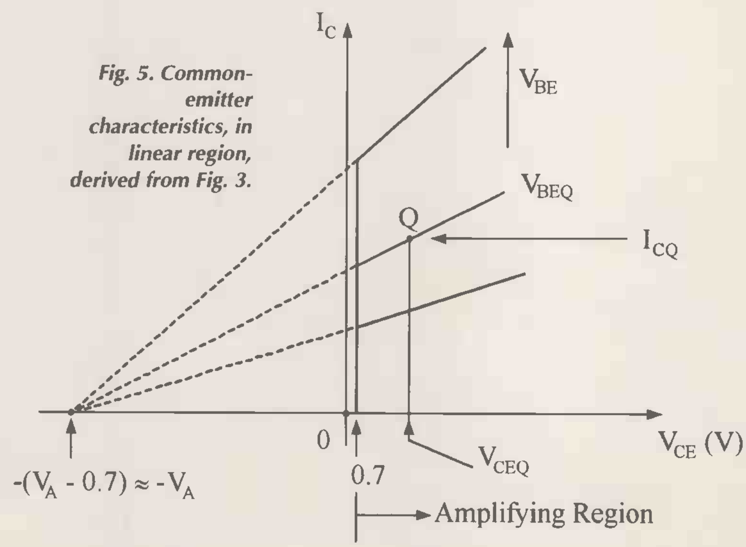

Fig. 5. Common-emitter characteristics, in linear region, derived from Fig. 3.

than zero describe the saturation region.

The saturation characteristics do not follow from eqn (1). Different equations apply. They are only indicated for completeness: they are ignored from now on.

Equation (8) states that the tangents to the output characteristics at V_{CB}=0, when extrapolated back, have a common point of intersection on the horizontal axis at $V_{CB}=-V_A$.

In honour of J. M. Early, who carried out pioneer work on bjt output conductance[3] that led to the description 'Early Effect' for base-width modulation, V_A is known as the 'Early' voltage.

The choice of the relatively uncommitted subscript letter *A* rather than *E* saves possible confusion with an emitter voltage. Typically, V_A is around 100V for an n-p-n bipolar transistor. This a useful default figure when none is deducible from manufacturers' data. For an n-p-n device V_A is around 50V.

What happens when V_{CB} is greater than zero? As a result of current device design and fabrication technology the ratio Q_B/C_{JC}, in eqn (6), is not a strong function of V_{CB} over a practically useful range of V_{CB} ($<<V_A$). So, for simplicity in characterisation and modelling, it is assumed that Q_B/C_{JC} remains constant at the value, V_A, that it has for V_{CB}=0.

Now, equation (6) becomes,

$$\frac{1}{I_C}\times\frac{dI_C}{dV_{CB}}=\frac{1}{V_A} \tag{9}$$

Integrating with respect to V_{CB},

$$I_C = I_C(0)\exp\frac{V_{BE}}{V_A} \tag{10}$$

or,

$$I_C = I_{S0}\exp\frac{V_{BE}}{V_T}\times\exp\frac{V_{CB}}{V_A} \tag{11}$$

Equation (10) is only valid while V_{CB} is much less than V_A so using the following approximation is justifiable,

$$\exp\frac{V_{CB}}{V_A}\approx 1+\frac{V_{CB}}{V_A} \tag{12}$$

Then,

$$I_C = I_{S0}\left(1+\frac{V_{CB}}{V_A}\right)\exp\frac{V_{BE}}{V_T} \tag{13}$$

This equation describes a family of straight lines, each of which passes through V_{CB}=0 with a slope $I_C(0)/V_A$. These linearised approximations to the actual characteristics for V_{CB}>0, **Fig. 3**, are the tangents to the characteristics at V_{CB}=0 that were mentioned earlier.

For a given V_{CB}, equal increments in V_{BE} do not produce corresponding equal increments in I_C because of the exponential relationship between I_C and V_{BE}.

With V_{BE} constant – and, hence constant base current – collector current increases by a factor $[1+(V_{CB}/V_A)]$ as V_{CB} increases from zero, so β must increase by the same factor.

Thus,

$$I_C = \beta I_B = \beta_0 I_B\left(1+\frac{V_{CB}}{V_A}\right) \tag{14}$$

For a given V_{CB}, the relevant output characteristics with I_B the controlling parameter, are now equally spaced, **Fig. 4**. Rather than I_C as a function of V_{CB}, we are often more interested in I_C as a function of V_{CE}. To determine this we substitute $V_{CB}=(V_{CE}-V_{BE})$ in eqn (13).

$$I_C = I_{S0}\left(1+\frac{V_{CE}-V_{BE}}{V_A}\right)\exp\frac{V_{BE}}{V_T} \tag{15}$$

A popular assumption in biasing a bjt for linear operation is V_{BE}=constant=0.7V, so a safe lower bound to the linear region is also V_{CE}=0.7V.

In that case the output characteristics are shown in **Fig. 5**. They are those of Fig. 4 shifted horizontally to the right by 0.7 V. **Figure 6** is derived, similarly, from Fig. 4.

The I_{BQ} of Fig. 6 is chosen to correspond to V_{BEQ} in Fig. 5. Incremental resistance at operating point Q is given by,

$$r_O = \frac{V_{CEQ}+V_A-0.7}{I_{CQ}} \tag{16}$$

or,

$$r_O \approx \frac{V_A}{I_{CQ}} \tag{17}$$

Figure 7a) is a general view of two of the transfer characteristics and Fig. **7b)** is an expanded view of them in the

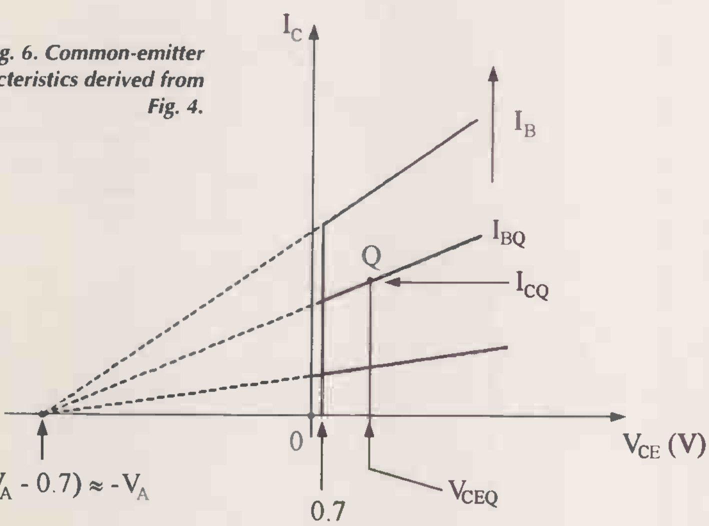

Fig. 6. Common-emitter characteristics derived from Fig. 4.

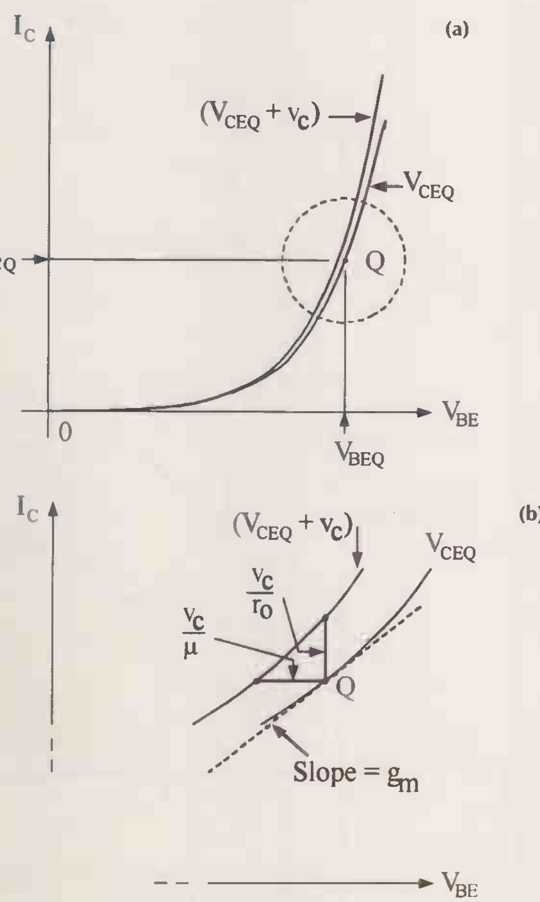

Fig. 7a). Two of the family of mutual characteristics: $V_{CEQ}>>v_C$. Fig. 7b) is its detail in vicinity of Q point, showing parameter relationships.

vicinity of Q. For small changes – $\delta V_{CEQ}=v_c$ etc. – the curves can be considered straight and parallel.

The parameter $r_o=(v_c/i_c)$ characterises the vertical spacing. The horizontal spacing is calculated by combining the exponential terms in equation (11).

If I_C is constant,

$$\frac{V_{BE}}{V_T}+\frac{V_{CB}}{V_A}=\text{constant} \tag{18}$$

$$\therefore \frac{v_b}{V_T}+\frac{v_c-v_b}{V_A}=0 \tag{19}$$

It is now convenient to make the definition,

$$\mu=\frac{V_A}{V_T} \tag{20}$$

Then,

$$v_b\approx\frac{-v_c}{\mu} \tag{21}$$

The approximation $\mu>>1$, made in obtaining eqn (21) from eqn (19), is also used in determining the slope of the characteristics.

Differentiating eqn (15) with respect to V_{BE}, with V_{CE} constant, gives the mutual conductance g_m.

$$g_m=\frac{I_{CQ}}{V_T} \tag{22}$$

From eqns (17) and (22),

$$\mu=r_O g_m \tag{23}$$

Older readers might remember this relationship first appearing with valves and μ being dubbed the 'amplification factor'.

The input characteristic is shown in **Fig. 8**. It is a single curve for $V_{CB}\geq0$.

The incremental input resistance termed r_π is given by,

$$r_\pi=\frac{dV_{BE}}{dI_C}\times\frac{dI_C}{dI_B} \tag{24}$$

or,

$$r_\pi=\frac{\beta}{g_m}=\frac{\beta V_T}{I_{CR}} \tag{25}$$

Three choices for the small-signal low-frequency equivalent circuit of the bipolar transistor are shown in Fig. 9. These are constructed from the parameters, already defined, by standard model building procedures as, for example, in ref. 4. Thus, the output circuit of **Fig. 9a)** is developed from Fig. 5 by considering small changes about the point Q and the output circuit of Fig. **9b)** is similarly related to Fig. 6.

Fig. **9c)** is derived from Fig. 9b) by the use of Thévenin's theorem. The input circuit of each model derives from Fig. 8. Resistance r_x has not been mentioned previously because we have considered only the idealised structure of Fig. 1.

A more practical structure is shown in **Fig. 10**. Here, r_x is typically 50Ω and represents the equivalent lumped resistance of the semiconductor material between the base terminal and the active base region. This region is that part in the vertical shadow of the emitter, i.e. inside the cylindrical region bounded by the vertical dotted lines.

As the junction areas are unequal, the Early voltage is V_A, as defined by equation (7), multiplied by the factor collector-junction area/emitter-junction area.

In my next article, I will show how to apply the characteristics and models to the solution of some circuit design problems, starting of with that mentioned at the beginning of this article. ■

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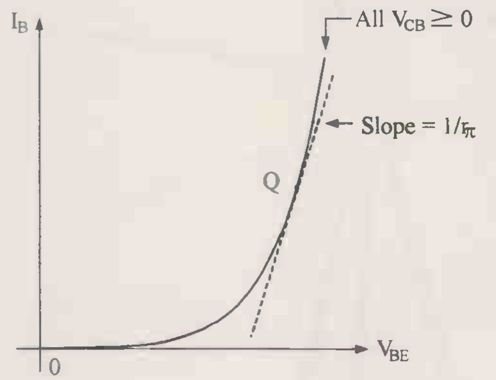

Fig. 8. Input characteristic curve, when V_{CB} is zero or greater.

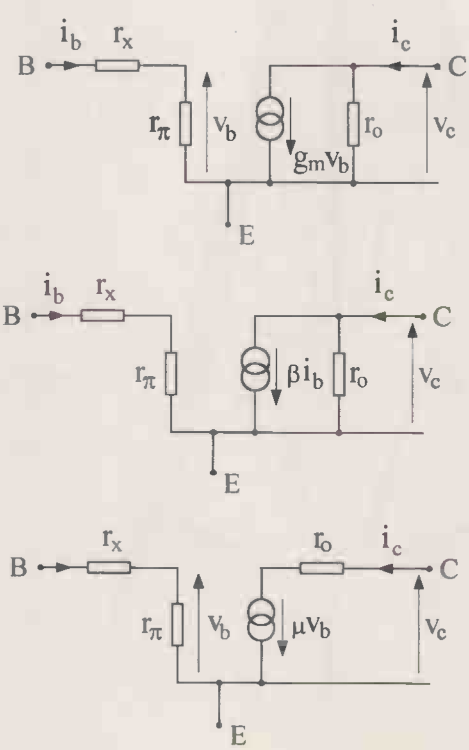

Fig. 9. Showing three choices for a small-signal low-frequency equivalent circuit of the bjt.

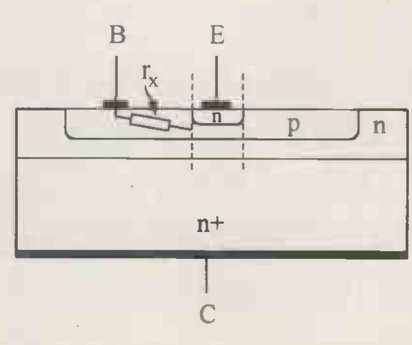

Fig. 10. Practical cross-section of a discrete bjt showing the existence of base bulk resistance (r_x) and unequal junction areas.

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Who needs a degree?

It seems nothing short of BEng will do if you want to succeed as an engineer. Someone should have told last year's award winning electronics engineers Kim Dennis and Amanda Box. Richard Wilson reports

A point of view expressed during last year's *Recognising the Engineer* campaign was that you need to have spent at least three years at a university obtaining a degree before you could rightly call yourself an 'engineer.' It seems that for some engineers desperate to maintain their status, nothing short of a BEng – and probably one from a red brick university – will do if you want to succeed as an engineer.

This view of the world is surely misguided. If you still need convincing then look no further than the career paths of two award-winning electronics engineers, Kim Dennis and Amanda Box.

Kim Dennis, IT specialist skills group manager at Marconi Communications beat off stiff competition to take the title of 1998 Young Woman Engineer of the Year.

Dennis, who is responsible for career development resource management and work load scheduling, received her award and a cheque for £1000 in January from Her Royal Highness The Princess Royal.

Twenty-six year old Dennis started her association with the telecoms manufacturer, formerly known as GPT, straight from leaving school in 1988. Under a technical apprenticeship with GPT she studied for her Ordinary National Diploma (OND) in electrical and telecommunications engineering at Coventry Technical College.

On completion of that course, Dennis studied for a further two years at college as a sponsored student with GPT. In 1992 she qualified with a Higher National Diploma (HND) in electrical and telecoms engineering.

The real benefit of being a sponsored student was that Dennis walked straight into the job she wanted at GPT. For Dennis the career ladder started as a systems support specialist with GPT's IT department. Within three years she became a team leader and by 1998 she was managing a team of 20 IT specialists within the company.

As a project manager Dennis is involved in planning and monitoring IT programmes. But she also accepts the importance of her role in managing and monitoring the career development of her team

Amanda Box, a senior software engineer with Thomson Marconi Sonar, was another electronics engineer commended in the awards.

She took an HND in software engineering and was sponsored by GEC Marconi Avionics in Rochester. Box spent three years with GEC before transferring to Thomson Marconi Sonar where she worked as a software engineer in the airborne anti-submarine warfare group.

With experience working on systems for the Royal Navy's Sea King and EH101 Merlin helicopters (pictured) under her belt she was promoted to a senior software engineer leading a team of ten staff.

As a team leader Box is involved in data processing software design and implementation, but she also has management tasks such as budget control for her area and the selection of training courses for all the project engineers. ■

Dennis... Started as a technical apprentice at GPT.

Checking C in situ

Cyril Bateman presents possibly the best ever general-purpose meter for checking electrolytic capacitors without removing them from the board.

Diagnosing a failed aluminium electrolytic capacitor mounted on a printed circuit board is more difficult than for other capacitor types, which fail as short circuits.[1]

Normally, when an aluminium electrolytic capacitor fails, it exhibits a higher than normal impedance. But its capacitance value may be little changed, and usually stays well within tolerance so measuring capacitance does not help.

Aluminium electrolytic capacitors are self repairing. Defective areas in the oxide dielectric are replenished by new oxide growth, consuming some of the oxygen available from the electrolyte. This self-repairing action ultimately becomes the wear out mechanism.[2]

An aluminium electrolytic capacitor's service life ends when oxygen needed to maintain or repair the oxide dielectric cannot be provided by the electrolyte. Electrolyte conductivity is reduced, increasing the capacitor's equivalent series resistance, or ESR, and hence its impedance at all frequencies. There's more on this in the panel entitled 'Electrolytic capacitor ESR.'

This increase in impedance is analogous to inserting a resistor in series with the capacitor, affecting the phase angle of applied signals and lengthening the device's time constant.

Increased ESR, or impedance, of an aluminium electrolytic capacitor at room temperature indicates a failure or pending failure. The ESR and impedance of unused capacitors varies widely with capacitance value and voltage. So a change in impedance or ESR is almost impossible to diagnose reliably, except by comparing the capacitor being tested with an identical unused one, **Table 1.** This is discussed further in the panel entitled 'Impedance or ESR?'

By comparison, the measured tangent δ of unused capacitors at 100Hz is a relatively constant number, regardless of value or voltage rating of the capacitor. Tanδ is a direct indicator of capacitor quality, **Table 2.**

At any chosen frequency, a capacitor's tanδ relates the capacitor's ESR and capacitance value. Any increase of ESR results in a corresponding, easily identified, increase of tanδ.

What is tanδ?

The tanδ of a capacitor at any frequency, is directly related to its capacitance value and ESR at that frequency.[3]

$$\tan\delta = \frac{ESR}{X_c} \qquad (1)$$

where,

$$X_c = \frac{1}{2\pi FC}$$

Alternatively $ESR = X_C \times \tan\delta$ and $\tan\delta = ESR \times 2\pi FC$.

You might find it easier to visualise these relationships by looking at a capacitor's current, voltage and impedance vector drawing, as in **Fig. 1**. As you can see, with the X_c vector unchanged, increasing the ESR vector reduces the loss angle θ, increasing the complementary angle δ. On the other hand, increasing the ESR vector only slightly increases |Z|, the impedance vector.

As δ increases, so does its tangent. Known as tanδ, this figure indicates the quality of a capacitor. The smaller tanδ, the better the capacitor. Any increase in tanδ directly indicates a degraded component. The panel entitled 'Capacitor quality and tanδ' expands on this aspect.

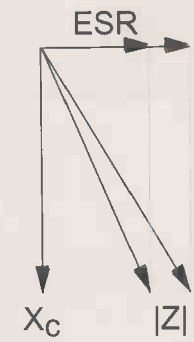


Fig. 1. Illustrating the effect an increase of ESR has on measured impedance and tanδ. The 37.5% increase of ESR shown, must, according to Pythagoras, result in a 37.5% increase in tanδ. The impedance magnitude, |Z| however, only increases by 6.9%.

Why measure tanδ at 100Hz?

All aluminium electrolytic capacitors are tested in production for tanδ at 100Hz or 120Hz, according to the frequency of the maker's mains supply. While many capacitor makers also table high-frequency impedance values, these are not production tested. To maximise yields, the measured tanδ of typical new capacitors will be around 50% of the stated limit value.

The range of 100Hz tanδ measured for new, good capacitors, is extremely small, changing little with capacitance values and voltage ratings.[4] Tanδ of typical commercial aluminium electrolytic capacitors ranges from a low of 0.02 to a high of 0.3 for large low voltage parts, **Table 2**.

Aluminium electrolytic capacitor tanδ increases rapidly as the capacitor wears out. It provides a sensitive, easily interpreted measurement. As a general guide, tanδ for typical good board-mounted capacitors should be less than 0.1. Capacitors with a tanδ of greater than 0.2 should be replaced in the interests of reliability.

Good quality commercial electrolytic capacitance bridges measure tanδ, but they can be expensive and not easily portable. In addition, test voltages used may turn-on adjacent semiconductor junctions, invalidating the measurement.

Measuring the tanδ of a board-mounted capacitor requires a low cost, easily portable meter with four terminal contact probes. It also requires a suitably low test voltage and a quick unambiguous measured result. Unable to identify such an instrument I resolved to build one.

Measuring tanδ on a pcb

How then could the tanδ of a board-mounted capacitor be measured?

From equation 1, it is clear that the ratio of the capacitor's ESR to its capacitive reactance is needed. You do not need to know the true value of either, only the relative values. This simplifies the task.

Accurate measurement of individual values requires accurate control of the measurement current used and its exact frequency. Since ratios are being evaluated, circuit current is common to both

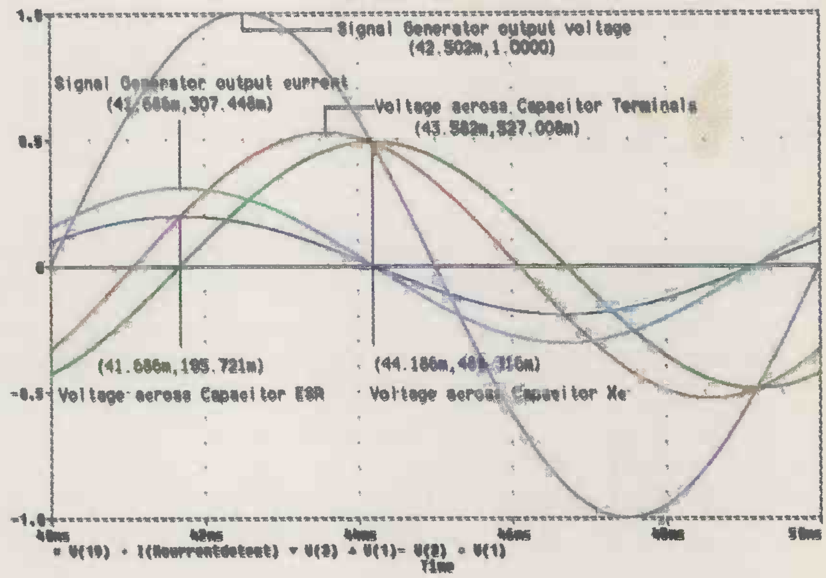


Fig. 2. PSpice plot of a simple series CR circuit representing a 'bad' 1000µF capacitor having a tanδ of 0.4 at 100Hz. Generator source impedance is 2.2Ω. This 0.4 tanδ is represented by a 0.6366Ω series resistance. The phase angle between the generator current (cyan) and the voltage across the capacitor terminals (red), is not 90°. However the phase angle between the voltage developed across the capacitor's ESR (blue) and across the capacitor's reactance (green), is exactly 90°.

Table 1a). Typical impedances measured at 100kHz – low capacitance values.

Capacitor	1µ	2.2µ	4.7µ	10µ	22µ	47µ	100µ
50V bipolar Al.	4.0Ω	3.2Ω	1.4Ω	0.9Ω	0.35Ω	0.3Ω	0.22Ω
63V polar Al.	4.3Ω	3.5Ω	1.8Ω	1.4Ω	0.5Ω	0.4Ω	0.28Ω
450V polar Al.	24Ω	11Ω	5Ω	3.8Ω	1.5Ω	1.0Ω	

Table 1b). Typical impedances measured at 100kHz – high capacitance values.

Capacitor	1000µ	2200µ	4700µ	10 000µ
25V polar Al.	0.090Ω	0.07Ω	0.045Ω	0.022Ω
63V polar Al.	0.050Ω	0.025Ω	0.015Ω	0.010Ω

Table 2a). Typical tanδ values of new capacitors measured at 100 Hz – low capacitance values.

Capacitor	1µ	2.2µ	4.7µ	10µ	22µ	47µ	100µ
50V bipolar Al.	0.05	0.05	0.05	0.05	0.05	0.05	0.06
63V polar Al.	0.04	0.04	0.035	0.035	0.035	0.045	0.04
450V polar Al.	0.1	0.1	0.08	0.05	0.05	0.05	

Table 2b). Typical tanδ values of new capacitors measured at 100Hz – high capacitance values.

Capacitor	1000µ	2200µ	4700µ	10 000µ
25V polar Al.	0.06	0.075	0.09	0.1
63V polar Al.	0.03	0.05	0.06	0.07

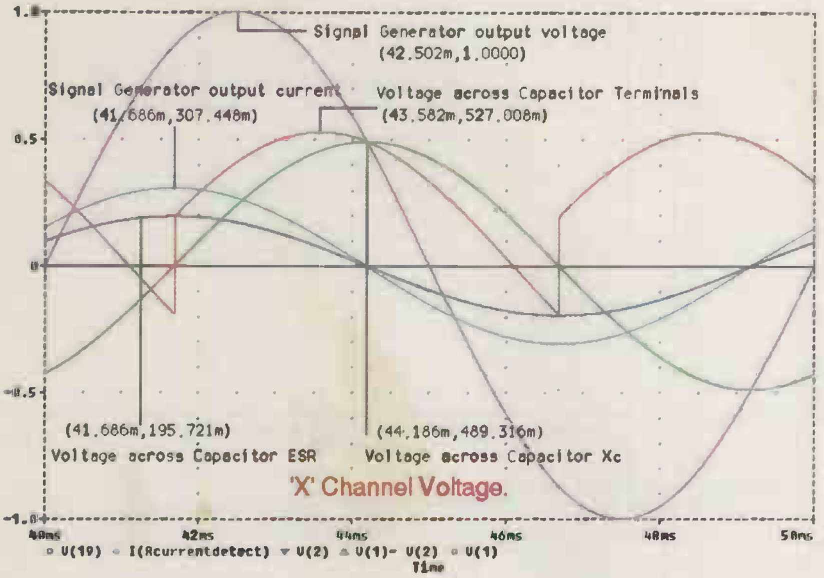


Fig. 3. Figure 2 repeated except the red trace now shows the synchronous detector voltage for the 'X' channel, which represents the capacitor's reactance. This trace must be integrated to a steady average voltage before it can be used

parameters so its value need not be known.

Capacitance and ESR are treated as separate components in the simulations that follow. With a practical capacitor, neither parameter is available at the capacitor terminals. Circuit simulation ignores such constraints. By means of a series *CR* circuit, a capacitor's internal voltage, current and its relative phases can all be explored.

Using PSpice and a series CR equivalent circuit, I plotted the current and voltage waveforms for a variety of capacitor tanδ values. To illustrate a failed capacitor, I assumed a 1000μF component with a tanδ of 0.4. A low generator source impedance was used to plot generator current, **Fig. 2**.

The phase angle between the voltage developed across the capacitor terminals and the source generator current, is clearly not 90°. It varies with capacitor tanδ or ESR and with generator source impedance, so it cannot be defined.

Current from the generator source is exactly in phase with the capacitor's through current and the voltage developed across its ESR. The voltage developed across the capacitor's reactance remains displaced in time by exactly 2.5ms, representing a quarter cycle, or 90° of phase.

The problem now is how to measure these two voltages. The only accessible voltage that can be measured is that across the capacitor terminals – i.e. its impedance.

Initially I planned to use two synchronous rectifiers. One would be timed to coincide with the generator current, representing the voltage developed by the ESR. The second would be delayed by a quarter cycle to measure the voltage developed by the capacitor's reactance. Averaging both then dividing the results would derive the capacitor's tanδ.

Further PSpice simulations show this simple approach was not practicable. Both sampled voltages contain large negative-going elements, requiring long integration times. Illustrated is the waveform of the capacitor's reactance voltage, labelled as 'X' channel, **Fig. 3**.

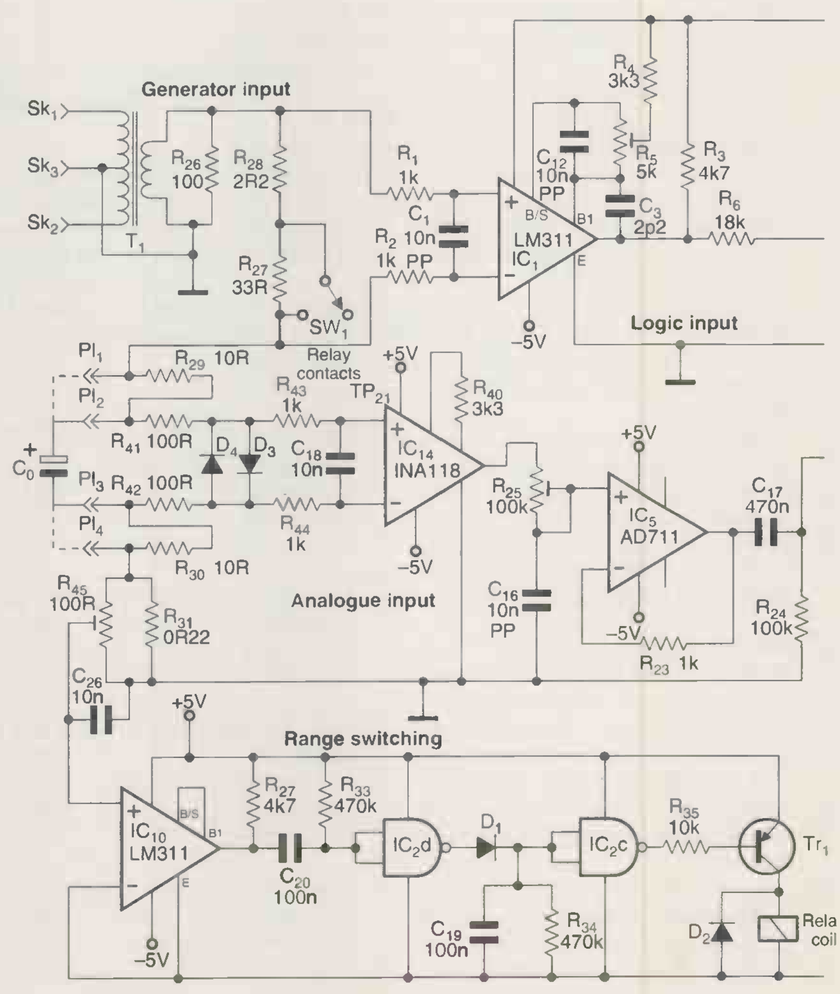
Towards faster results

Looking at **Fig. 4**, the curve for the capacitor's ESR in particular has nearly equal positive and negative elements and needs a long time constant to average. For the instrument to be useful as a diagnostic tool though, it is desirable for it produce results in less than a second. Assuming the standard electrolytic test frequency of 100Hz and using PSpice simulations, I was unable to achieve satisfactory averaging in an acceptable time.

A better plan

While this basic timed sampling concept was obviously correct, a means to expedite averaging was required.

From further simulations, I found a reduction of the sampling periods to 90° or less was beneficial. It was even more



Full measurement schematic, less decoupling capacitors, used in my prototype meter. Additional circuitry is included, but not shown here, for the test signal source generator and the dry battery powered, stabilised switched-mode ±5V supplies. The small modification needed to my PM128/7106 display module is described in the text.

Readers interested in PCB and parts details please send an SAE marked 'Capacitors' to Electronics World's editorial offices, from where it will be forwarded to Cyril.

as sampling time was reduced. Short sampling periods require a sample-and-hold circuit together with timing and control logic. My original concept of a simple tester had suddenly become more complicated.

My first task was to generate two sampling waveforms, exactly 90° apart, one coinciding exactly with the peak of the generator's output current. I decided to use a *4046* CMOS phase-locked-loop. While locked to an input signal, the 'phase-comparator 1' phase detector of a *4046* is claimed to have a 90° phase difference between the input signal and its VCO output.[5]

Initial trials confirmed that this figure of 90° only applied while the input signal and the PLL centre frequency coincided. Small component changes – even ambient temperature drifts – affected this phase difference. Time for a rethink.

I evaluated several options, and eventually decided to double the signal's frequency, then halve it to ensure equal mark:space ratios. Application of some decoding logic to both frequencies could produce exactly 90° phases, as needed.

As before, the *4046* phase locked loop was used, but this time, its 'phase-comparator 2' detector output was fed into a 4018 configured to divide by two. I obtained two square-wave signals, both having equal mark:space ratios. The first was at 100Hz and phase locked to the generator's current waveform. The second was at 200Hz and had rising edges coincident with the 100Hz waveform transitions.

These signals were easily decoded to identify the 90° and 180° points of the generator's current waveform using a pair of dual input Nand gates, IC_{6a} and IC_{9a} in the schematic. The rising edges of these decoded outputs were used to trigger two monostable multivibrators, **Fig. 5**.

Sample and hold circuits need a short time to track then hold the input waveform. Any change in voltage during the sample period causes errors. From my PSpice plots, I decided to sample this changing waveform for a minimal time of, say, 5° of the waveform maximum, **Fig. 6**.

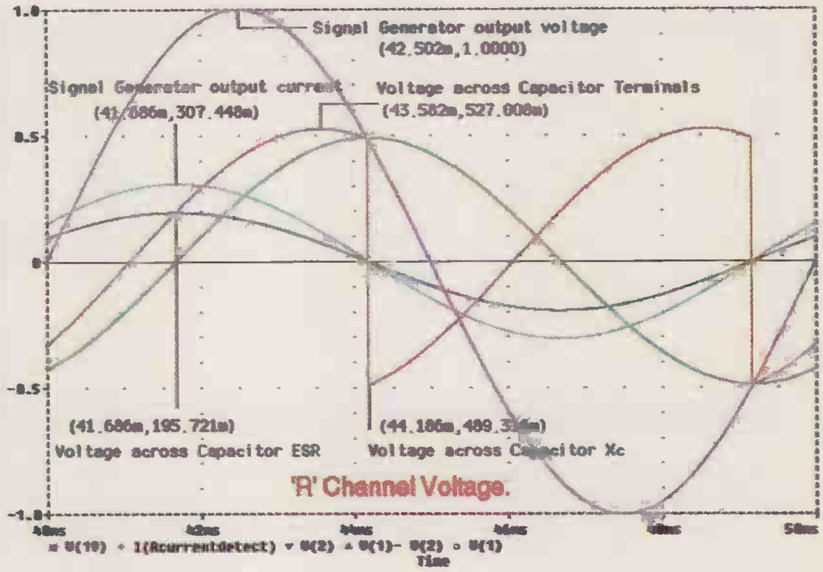
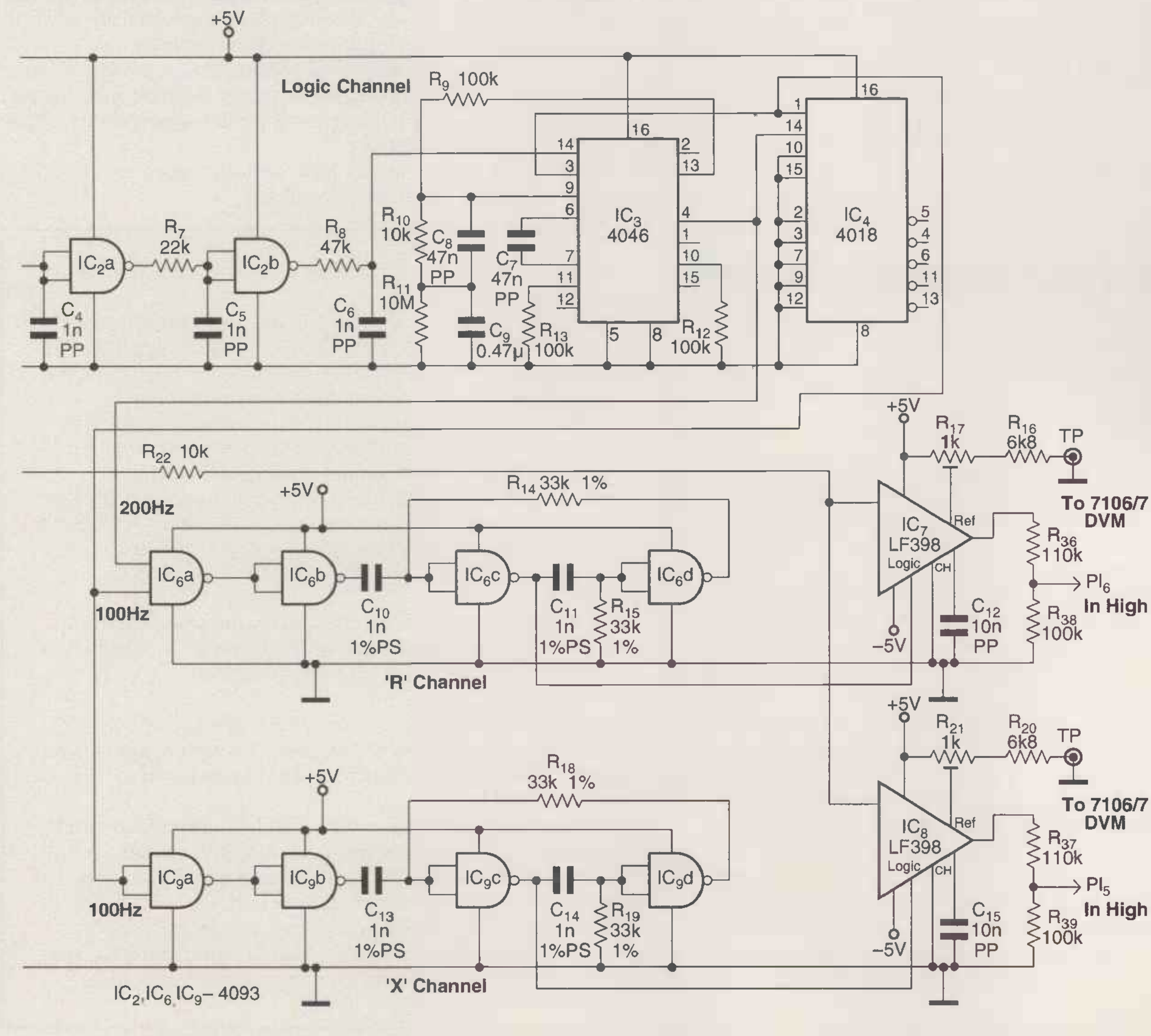


Fig. 4. Figure 2 again, but this time the red trace shows the synchronous detector voltage for the 'R' channel, representing the capacitor's ESR. This waveform requires excessive integration time for use in my meter. Testing unused, small tanδ capacitors, this trace after integration results in a very small output of just a few millivolts.



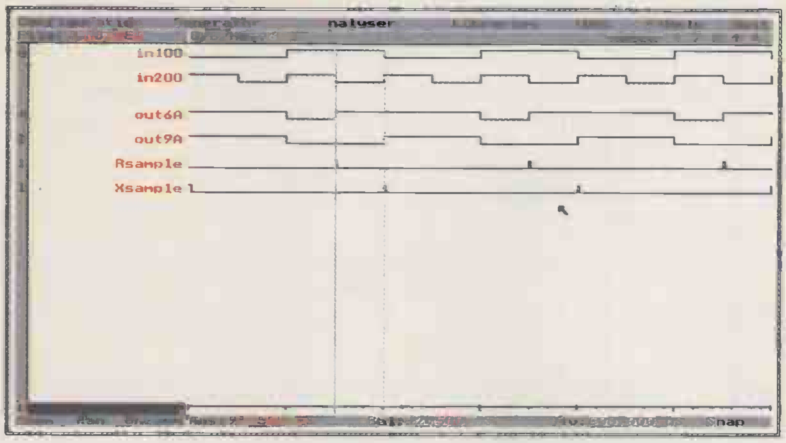


Fig. 5. This Pulsar simulation illustrates the method used to generate the logic control signals from the original 100Hz and its doubled frequency. These brief sampling pulses are used to control the 'R' and 'X' sample and hold integrated circuits.

The *LF398* sample-and-hold chip requires at least 20μs to acquire the sampled signal. Practical experiments using an *LF398* and test capacitors of varying tanδ indicated that 3°, or around 80μs sampling time, gave good results.

Having a method to sample the ESR and X_c components in the capacitor voltage waveform, I could now design the generator and current sensing circuits.

Generator problems

One particular difficulty was the wide range of capacitance values. I wanted to include everything from 1μF to 10000μF.

At 100Hz, a 1μF capacitor's impedance is around 1600Ω, but a 10000μF component only exhibits around 160mΩ at the same frequency. A constant test current was not possible.

To avoid turning on any semiconductor junctions connected to the capacitor, a low test voltage is essential. Some *HP5082-2080* low voltage Schottky barrier diodes were found to conduct at 200mV AC. From experiments measuring tanδ of capacitors with and without a parallel *HP5082-2080* diode, I determined the maximum test voltage to be 150mV. At this voltage, any effects on capacitor tanδ value from semiconductor junctions in the same circuit as the capacitor being measured are negligible.

Allowing a low generator source impedance and a 2.2Ω current-sensing resistor, this 150mV signal requires some 50mA of generator current. With the unfavourable voltage/current phase angles needed, this proved difficult using battery powered op-amps.

Having tried various options – including high current or booster op-amps and low power audio output amplifier chips – I decided to trade voltage for current. A low-cost miniature *LT700* audio transformer needing only ±1.5V push-pull drive at negligible current improves battery life.

Current sensing

Using the above generator and an *LM311* comparator for the logic channel input stage, I could finalise the values of the current sensing resistors. Ideally one would ensure the test capacitor's impedance was within a factor of ten of the sensing resistance used. Experimentation confirmed that a 2.2Ω sense resistor was usable for test capacitances of 100μF or more.

Lower capacitance values proved more difficult. Ideally, three sense resistor ranges were needed but having only two would be more economical. Sense resistors larger than 100Ω were prone to trigger the comparator by noise picked up on the test leads.

Testing 1μF capacitors with a 10Ω sense resistor the comparator did not provide reliable triggering. A compromise of 35Ω was chosen, allowing good measurements down to 2.2μF – and even 1μF with reduced accuracy.

As a final refinement, two Schmidt trigger Nand gates were used to clean up and slightly delay the comparator output. This was done to prevent comparator noise from triggering the phase locked loop.

My current-sensing logic circuits, needed for the sample and hold stages, were completed.

Impedance or ESR?

The impedance of any capacitor is easily measured. Simply subject the capacitor to a known current and measure the voltage developed across the capacitor terminals. Impedance

$$|Z| = \frac{voltage}{current}$$

using Ohm's law, much like measuring a resistance value.[6]

Searching Internet and trade publications revealed a few high frequency 100kHz capacitor impedance testers, but not one single low cost meter to measure tanδ.

While many of these were labelled as ESR testers, this is a misnomer since all the meters I found measured impedance. Based on the mistaken belief that at 100kHz capacitive reactance is zero, they thus claimed to measure ESR.

This presents a problem with smaller capacitance values of, say, 100μF and below. Brand new, many makes exhibit 100kHz impedances greater than 0.5Ω, simply because their capacitive reactance approaches this value. Regrettably these are the values most used on circuit boards.

When measured, the capacitance value of all aluminium electrolytic capacitors reduces substantially as frequency increases. Typical values at 100kHz are perhaps 50% – and frequently much less – of the 100Hz value.

One brand-new 100μF capacitor I measured at 100kHz using a precision bridge had an impedance of 570mΩ. Its capacitance at 100kHz was only 37.5μF. By comparison, a better make had an impedance of 170mΩ, and 64μF capacitance. Both these capacitors were new and well within their makers' specifications.

Capacitors of 1000μF or more will be above self-resonance by 100kHz and thus behave as DC blocking inductors. Good and bad capacitors then have an impedance of less than 0.5Ω.

These are just two of the problems met measuring impedance at 100kHz. Measured results need interpretation. Impedance values cannot simply be read as good or bad, they must be compared with a similar and unused capacitor.

Some meters incorrectly claim to be able to distinguish between good and bad capacitors in circuit. I have seen them with scales marked 'good' for values below 0.5 to 1Ω, 'compare' for values up to 10Ω and 'bad' for all higher impedances.

I have measured 100kHz impedance values ranging from 0.01Ω to 24Ω for known good, unused aluminium electrolytic capacitors. Clearly it is not possible to pre-define specific good/bad impedance values.

If their readings require interpretation, why then do these meters measure impedance? The answer is simply that it is an extremely easy measurement to perform, compared to measuring tanδ or ESR.

The results of these 'ESR' meters require interpretation and comparison against known good capacitors. Measuring a suspect capacitor's high-frequency impedance however is better than simply guessing at good or bad.

As a long time capacitor engineer also experienced in designing and repairing circuits, I have learned that what is really needed is in-circuit measurement of tanδ at 100Hz.

Capacitor analogue voltage waveform

For my prototype, I wanted to provide two capacitor test methods, flexible four-terminal test leads and a four-terminal component jig.

Typical commercial test leads have a resistance of 0.1Ω. Since it is necessary to measure ESR down to 0.010Ω, a four terminal measurement system is essential. For those of you who are not familiar with this technique, four-terminal measurement involves supplying the test current along one pair of leads and measuring capacitor voltage via a second pair.

True four-terminal measurement requires complete separation of the current and voltage leads. Contact is made to the capacitor lead wires, using 'Kelvin' clips. This is not practicable when probing printed board mounted capacitors though.

As a compromise I found some test prods that could be wired four terminal except for the final 30mm long brass probe points, which each measured 0.45mΩ. As a result I was forced to accept 1mΩ of common contact resistance, resulting in a small but acceptable error when measuring the largest value capacitors.

The resistance of the earthy probe lead, together with the range sense 0.22Ω resistor, means the test capacitor's voltage is effectively floating. This necessitates the use of an instrumentation amplifier as the first input stage of the analogue measurement channel.

The 150mV generator voltage, fed via the 2.2Ω sense resistor, means large test capacitance values develop very small voltages. To minimise sample and hold errors, these low level test signals were amplified in the *INA118* in-amp, taking care to stay within the working range of the *AD711* amplifier and *LF398* sample-and-hold circuits.

The small delay deliberately built into the comparator and logic channel circuits is offset using an adjustable *RC* delay at the *INA118* output. This delay is adjusted as part of the meter calibration.

Range switching

An adjustable, voltage-sensing comparator and reed relay was used to short out the 33Ω current sensing resistor when measuring capacitors bigger than 47μF.

Having completed the circuits needed to measure the voltages relating the test capacitor's ESR and reactance, all that remains is to divide the 'R' channel voltage by the 'X' channel voltage and display the result.

Various options including multiplier/divider chips and log/antilog circuits were considered. Following some practical experimentation, I found that they could be dispensed with.

The *7106* DVM integrated circuit compares the measurement voltage against its pre-set reference voltage. This reference voltage is set to 50% of the desired full scale. Removing two resistors, R_2 and R_3, I managed to disconnect this reference voltage from a *PM128* pre-packaged display module.

An adjustable voltage was fed to the REF-HI input terminals, a second to the normal IN-HI terminals. Both commons went to the input ground. I found this package could divide and display the result extremely accurately, provided both voltages were within the meter's maximum 2V input range.

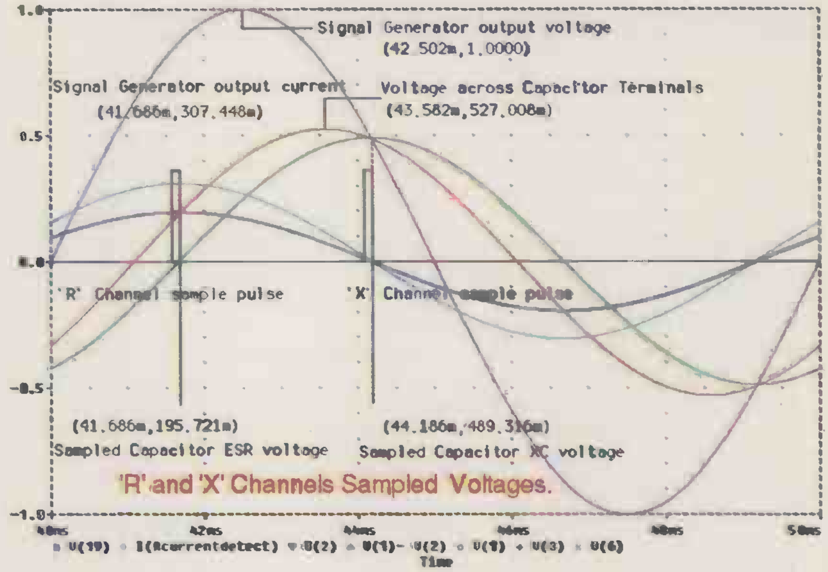


Fig. 6. Sample-and-hold logic control voltages, superimposed onto the Fig. 2 plot. The logic decoding circuitry, which permitted the successful design of my meter, occupies over 70% of the measurement section of the 140mm by 74mm printed board.

Electrolytic capacitor ESR

Aluminium electrolytic capacitor electrolytes are conducting solutions, usually a neutralised weak acid in a solvent. This electrolyte must not freeze or boil at the extremes of the capacitor's working temperature range, or attack pure aluminium at any temperature. Most modern electrolytes are made without adding water, but a small water content, as water of crystallisation in some of the ingredients, is inevitable.

In a capacitor, some of this electrolyte is contained within the minute voids and channels in the anode and cathode foils oxide coating. These channels can be tenuous and very long relative to their cross section.[2] The effective electrolyte resistance in them increases with frequency.

Most of the electrolyte however will be absorbed in the separator, usually a paper tissue, interwound with the anode and cathode foils during assembly. The resistivity of the electrolyte/paper separating tissue is increased, compared to the bulk electrolyte, depending on paper type and thickness used.

The aluminium oxide films on the anode and cathode foils both contribute frequency dependent dielectric losses. A parallel loss resistor could represent these losses, but for aluminium electrolytic capacitors, equivalent series loss resistance is used.

The aluminium metal foils together with connecting leads, etc., contribute a small metallic resistance element.

At any frequency the capacitor's ESR is the combined effect of the foils series loss resistance and these metallic resistances, added to the electrolyte paper resistance.

Consequently a capacitor's ESR varies with measurement frequency, tending initially to reduce as frequency increases. At intermediate frequencies it becomes nearly constant. Then at frequencies where the capacitor has become inductive, it increases more rapidly.

An aluminium electrolytic capacitor's ESR is strongly influenced by its internal temperature. An increase in temperature reduces ESR. Below 0°C the capacitor's ESR increases rapidly. The viscosity of the solvent in the electrolyte increases as it approaches its freezing point.

Most of all, ESR depends on the capacitance value and to a lesser extent its voltage rating. At a particular voltage rating, all other things being equal, doubling a capacitor's value will halve its ESR.

A particularly common mistake is to consider a capacitor's ESR as having a fixed value. Clearly from the above, that is not possible.

ESR for any particular aluminium electrolytic capacitance value and voltage rating, is a combination of many effects, especially measurement frequency, temperature, physical size of the capacitor element, and details of its construction.

Setting up

I tried to make this meter as free from calibration as possible. Calculating the ratio of the 'R' and 'X' channel voltages, the sense resistor value, and test current or voltage being common to both need not be accurately known. Only one adjustment using a known or relatively loss free capacitor is needed to calibrate the meter.

First, connect a stabilised power supply delivering +5V and –5V. With a capacitor connected to the test terminals of the meter to ensure the sample and hold circuits are triggered, temporarily remove the analogue input signal to both sample and holds. This is easily done by grounding the junction of their common inputs with R_{22}.

Measuring the DC output voltages of both sample and holds in turn, trim both to 0V then unground R_{22}. Remove the test capacitor and adjust the offset of the current sensing comparator, IC_1, for maximum output noise, then back off to just remove all noise while ensuring that the comparator output remains 'low'.

Apply a 47µF capacitor to the test leads or jig and adjust the range switching comparator input voltage pre-set to just turn off the relay, extinguishing the range LED. Replace the capacitor with a 100µF type and ensure the relay and LED just turn on when connecting the capacitor.

None of the above adjustments are particularly critical but they do help ensure consistent operation of the meter. This final adjustment sets the meter's accuracy.

Apply a 10µF polycarbonate, polypropylene or P.E.T. metallised-film capacitor of known tanδ to the test leads or jig. Monitor the output voltage of the 'R' sample and hold. Turn the delay-adjusting pre-set resistor on the *INA118* output until the display reads the correct tanδ while ensuring the output from the 'R' sample and hold remains a small but positive voltage. If you don't know the tanδ of the 10µF capacitor, then adjusting the display to read 0.006 should ensure acceptable accuracy.

Supplying power. Standing idle or measuring low-value test capacitors, the meter consumes around 21mA from the negative supply and 26mA from the positive supply. Consumption increases with large capacitors to a maximum of 23mA from –5V and 45mA from +5V, but only for the few seconds while connected to a test capacitor.

Some 12mA of this additional +5V current is needed for the range switching reed relay and its indicator LED.

In practice, 6AA cells provide some 40 hours use. The prototype's power supply used a low drop-out linear +5V stabiliser and a switched capacitor inverter for the –5V side. A transistor switching stage provides the ±9V floating supply for the display. To conserve batteries, a 20 minute 'auto-switch-off' timer circuit disables the +5V stabiliser, removing all power.

The *LF398* sample-and-hold chips, fed with the test capacitor's amplified voltage, provide a maximum output of about 4V. A simple attenuator, halving these voltages, completed my design.

Compared with the very simple circuits using two quad op-amps to measure capacitor impedance at say 100kHz, this circuit is obviously larger and much more complex. Its setting up and calibration however is extremely simple, as described in the panel entitled 'Setting up.'

How does it perform?

In practice, this meter performs extremely well, returning a steady measured value within three display meter counts, or less than a second. As to its accuracy, this more than suffices to distinguish between good and bad board mounted capacitors.

With the exception of measurements on capacitors near 1µF and 10 000µF, where accuracy reduces, it is hard to tell whether my laboratory capacitor bridge or this meter is the more accurate.

If pressed to give a number, I would guess that this meter reads tanδ to within about ±0.005 of the true value, except at the extremes of its capacitance range.

While I now only trouble-shoot new prototype designs, repair my own workshop equipment and the usual family TV, videos and satellite systems, I wish I had built this meter years ago. Being well equipped with laboratory capacitance bridges though, I had not seen the need.

I only built it now because when examining a 100kHz impedance 'ESR' meter, I suddenly thought 'there must be a better way'. This meter is the result of that simple desire.

As a bonus, the meter could also be used as a circuit tracer. Presented with a resistance of less than 20Ω, the high range LED lights and the tanδ display shows over range. ■

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Capacitor quality and tanδ.

The quality of many high-frequency components, such as RF inductors and very low loss capacitors, is often defined by their 'Q' factor. Q is the result of dividing a component's measured AC reactance by its AC resistive losses.

The reciprocal of 'Q' is tanδ, which is defined as the capacitors ESR/reactance. Tanδ is used to describe the quality of almost all general-purpose capacitors.

All practical capacitors exhibit losses. There is a small DC leakage current and there are resistive dielectric losses, which combined dissipate some of the applied energy as heat. These losses reduce the theoretical 90° phase difference between the applied current and the capacitor's voltage.

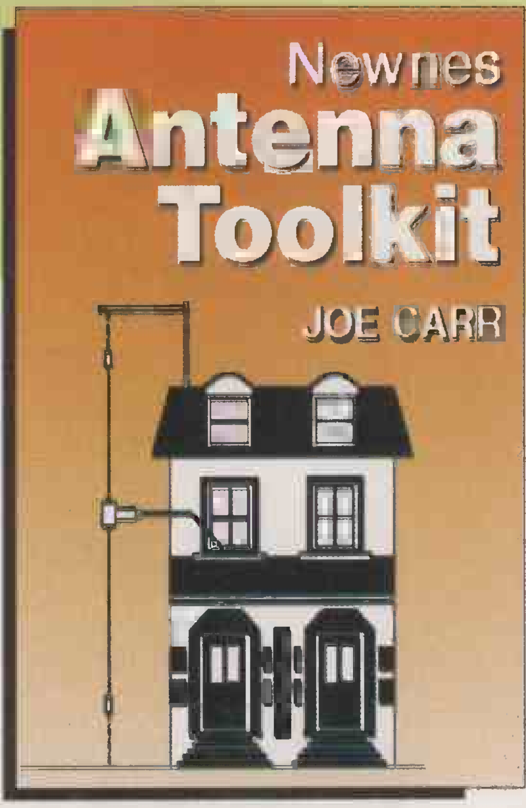
At 1kHz for example, the measured phase angle of a typical 1000µF 25V radial electrolytic capacitor was 67°, substantially less than the theoretical 90° of phase.

This phase angle could be reproduced in a circuit by using a high value resistor in parallel with the capacitor. Electrolytic capacitors however, use the phase equivalent circuit of a low value resistor in series with the capacitor. The series resistance for the above 1000µF 25V capacitor was measured at 1kHz and found to be 71mΩ, X_c was 169mΩ and tanδ was 0.42.

At 100Hz, the ESR of this capacitor measured 104 mΩ, X_c was 1.62Ω and tanδ was 0.064. This series resistance is the equivalent series resistance, or ESR, of the capacitor.[7]

The capacitor's reactance reduces in proportion to its capacitance value and frequency. Being a combination of fixed and variable losses, ESR also reduces with frequency but to a lesser extent. Having reached its minimum value, ESR then usually increases at some higher frequency.

The measured tanδ of an aluminium electrolytic capacitor is frequency dependent. It always increases as frequency increases. From equation 1, tanδ has no upper limit and can exceed unity – especially for a failed aluminium electrolytic capacitor.



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by Joe Carr

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SPEAKERS' CORNER

Why does the average 100W moving-coil loudspeaker only deliver two or three watts of sound? John Watkinson looks at why the moving coil loudspeaker is so inefficient, and explains the trade-offs.

The efficiency of a moving coil loudspeaker is doomed from the outset to be very low. The reason is that the density of air is low and so the acoustic impedance is correspondingly low.

To deliver power into a low impedance requires a high diaphragm or cone velocity. This in itself isn't a problem. The difficulty is that any practical cone and coil which isn't going to fall apart must have some structural mass and the impedance presented by this mass dwarfs the acoustic impedance in a real speaker.

Figure 1 shows that effectively we are transporting a massive cone in order to carry with it a tiny air mass. Its the equivalent of delivering pillows in an eight-wheeler; not very efficient.

The efficiency of a speaker is defined as the ratio of the acoustic power coming out to the electrical power going in. The electrical power is used in three ways. One is the ohmic heating of the coil. The second is the mechanical damping of the drive unit structure and the absorbent in the enclosure, which is very small above resonance and can be neglected. The third is the acoustic power transferred.

In practice, because the efficiency is so low, the acoustic power can also be neglected, leaving the input power as simply the ohmic loss in the coil. This is a great simplification. Coil dissipation is easy to calculate as it is the square of the current times the coil resistance.

Next we need to calculate the acoustic output power. In electricity, the power would be the square of the current times the resistance. In acoustics, it's the square of the cone velocity times the acoustic impedance.

Acoustic impedance

Figure 2a) shows the expression for the acoustic impedance. I'm asking for this to be accepted for the moment, but I intend to explore it further in a future article.

The expression for acoustic impedance can be simplified by taking out the fixed values and replacing them with a constant, K, which we can't change whatever we do to the drive unit. These fixed values are things like the density of air, the speed of sound and the correction factor for the kind of baffle. Note that the acoustic impedance is a function of frequency squared.

Figure 2b) shows how the cone velocity is obtained. Clearly it is proportional to the motor force, *Bli*. Because the system is mass controlled, the velocity is inversely proportional to frequency and mass.

In **Figure 2c)**, the acoustic power is derived by multiplying the acoustic impedance by the square of the velocity. Note that when this is done, the frequency term cancels out. This is the principle of the mass controlled speaker: the power is independent of frequency. In other words, there is a flat frequency response.

The efficiency is derived in **2d)**. Note that the current disappears from the expression. Thus an efficient speaker is simply a matter of using a strong magnet with plenty of wire in the gap and a large cone area, while keeping the weight and the coil resistance down. Unfortunately those requirements are contradictory because the more powerful we make the motor, the heavier it gets. Not so simple after all.

Expressing efficiency efficiently

A better approach is to express the efficiency in a different way so that the effect of the mass of the motor is easier to interpret. This is the approach taken in **Fig. 3**. If you assume a speaker whose coil is the same length as, or shorter than, the gap, then all of the coil is contributing to the motor force.

The mass of the voice coil, M_c, is given by its volume multiplied by the density of the coil material. The resistance of the voice coil also follows from its dimensions and resistivity.

With the efficiency re-expressed, it is easier to see what to do. Firstly a powerful magnet helps, but as was shown last month, this can't be taken too far in a passive speaker because the result is an overdamped system. It is also clear that when choosing a coil material, the product of the density and the resistivity is what matters, hence the superiority of aluminium.

It should be appreciated that M_m, the

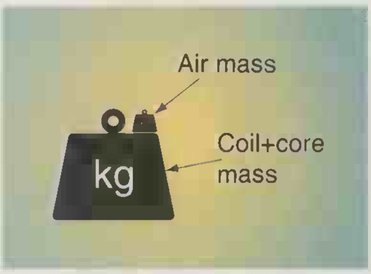


Fig. 1. Moving-coil speakers are doomed to be inefficient.

Fig. 2. Loudspeaker efficiency calculations.

$$R_m = 1.57\frac{p}{c}\omega^2 r^4 = K\omega^2 r^4 \qquad (a)$$

where R_m is acoustic impedance, 1.57 is the baffle factor, ω^2 is frequency in rad/s, r_4 is cone radius.

$$v = \frac{Bli}{\omega M_m} \qquad (b)$$

Here, v is cone velocity, ω is frequency, B is magnetic flux density, l is the length of motor coil inside the gap, i is current and M_m is the moving mass. Below, W_a is acoustic power,

$$W_a = v^2 \times R_m = \left(\frac{Bli}{\omega M_m}\right)^2 \times K\omega^2 r^4 = Kr^4\left(\frac{Bli}{M_m}\right)^2 \qquad (c)$$

so,

$$Eff = \frac{Kr^4 B^2 l^2 i^2}{M_m^2 i^2 R_E} = Kr^4 \times \frac{B^2}{M_m^2} \times \frac{l^2}{R_E} \qquad (d)$$

moving mass, incorporates M_C, the coil mass. The most striking result of the efficiency expression – which is counter intuitive – is that making the coil heavier without changing the total moving mass increases the efficiency. As a result, for efficiency we want the cone to be as light as possible so that the largest proportion of the moving mass is concentrated in the coil. The epitome of this is the ribbon speaker where the diaphragm is the coil.

Working together

The above expressions fail when the speaker coil and cone no longer move as a rigid body. In woofers, the cone and coil are certainly rigidly coupled over the useful frequency range. So the approach is useful except for the assumption that all of the coil was in the gap which is generally not true for woofers.

In order to have sufficient travel, woofers generally use overhung coils so that the *Bl* product remains constant as the coil moves.

If the coil length is described as *L* times the gap length, then *L* can be called the overhang factor. If the coil is simply extended by putting more turns above and below the gap, the coil is obviously *L* times as heavy and has *L* times as much resistance.

Figure 4 shows that the efficiency expression now contains *L* squared in the denominator, suggesting that a large overhang factor is bad news.

This is one of the reasons why really long throw woofers are rare. They are simply very inefficient because so little of the coil is producing thrust and the rest is adding to the mass and resistance. In practice, to obtain a given SPL it may be more efficient to put two normal woofers side by side rather than trying to engineer a long throw device. ■

Fig. 3. Efficiency considering motor construction.

$$M_C = lad \qquad R_E = \frac{\sigma l}{a}$$

$$a = \frac{\sigma l}{R_E}$$

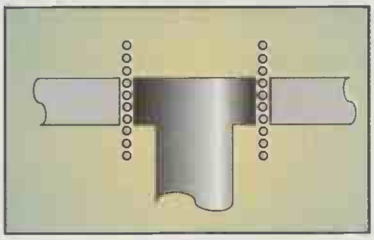
and

$$M_C = \frac{l\sigma l d}{R_E} = \frac{l^2\sigma d}{R_E}$$

$$\therefore \frac{l^2}{R_E} = \frac{M_C}{\sigma d}$$

$$\therefore Eff = \frac{Kr^4B^2}{\sigma d} \times \frac{M_C}{M_m^2}$$

Fig. 4. Overhung coils in woofers cause inefficiency



Thus $M_C = Llad$ and $R_E = \frac{L\sigma l}{a}$

Efficiency becomes $\frac{Kr^4B^2}{L^2\sigma d} \times \frac{M_C}{M_m^2}$

495

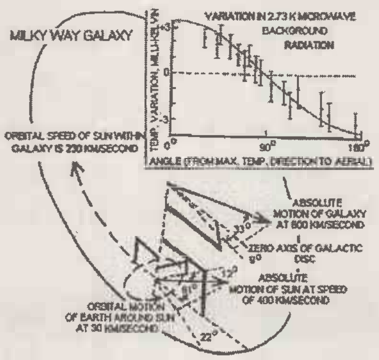
Science World Discovery Book

ADVERTISEMENT: Some details are hereby given from the above book which will be published as soon as possible. Nigel Bryan Cook, publisher.

The BBC2 Horizon programme on 28 Jan 98 showed how astronomers have recently used constant-energy supernovae at different distances to discover that there is no long-range gravitational retardation in the big bang expansion. Gravity seems to be localised, not a universal law.

This was predicted by the mechanism of gravity based on I. Catt's measurements of capacitor discharge speeds and the Catt Anomaly, and their implications for Maxwell's light "theory" and the true c-speed spinning electron, eg see *Catt's March 1983 WIRELESS WORLD article "Waves in Space", his 2-vol "Electromagnetic Theory", his paper in IEEE Transactions on Electronic Computers, EC-16 (Dec 67), and especially SCIENCE WORLD magazine (ISSN 1367-6172) February 1997-current.*

The old (incorrect) quantum theory of gravitons has the 377Ω dielectric of free space/vacuum/ether filled with a sea of colliding virtual particles which exert a pressure by hitting objects from all sides, except sides which face large objects which shield us from them. For example, the earth in graviton theory absorbs gravitons coming from below us, so we would be pushed down from gravitons from above, but not pushed up so much because we are walking on a massive shield (the earth). This theory, considered geometrically, gives the Newtonian inverse square equation. The two errors are that (a) gravitons would cause drag on moving objects, thereby slowing down the planets and causing them to spiral into the sun, and (b) gravitons, causing the measured deflection of starlight during eclipses, would scatter photons about instead of smoothly deflecting them as actually occurs.



To correct this theory, we must take space to be a continuous medium. Einstein in his 5 May 1920 lecture at Leyden University, Ether and Relativity (reprinted in Einstein's *Sidelights on Relativity*, Dover, New York 1952, 1983) said (pages 15, 16, 23): "The special theory of relativity forbids us to assume the ether to consist of particles... To deny the ether is ultimately to assume that empty space has no physical qualities whatever... Recapitulating, we may say that according to the general theory of relativity, space is endowed with physical qualities... therefore, there exists an ether. According to the general theory of relativity space without ether is unthinkable."

The continuous nature of the ether is demonstrated to readers of EW by the fact that electron (particle)-filled cables have an impedance in Ω/metre (thus depending on the number of discrete electrons), but ether has an impedance of 377 Ω (*not* Ω/metre).

Aristotle in *Physics* (350 BC), and Louis de Broglie in *Non-Linear Wave Mechanics: A Causal Interpretation* (Elsevier, Amsterdam, 1960) argued respectively that the momentum of objects and that particle-wave duality can be explained by a model which basically has particles moving through space like a fish or submarine in a frictionless, non-particulate water (the ether). The inertia to start motion is that of setting up a flow of ether around moving particles, hence an arrow continues to move after being released from the bow, and an electron sets up a motion-sustaining wave of ether around it in the ether so that it diffracts through slits. I create a sideways wave of air from front to back as I move, or a vacuum would form behind me. Since all matter is made of sub-atomic particles, the ether waves are similarly small. Ether is a continuous, frictionless, medium which flows around moving sub-atomic particles.

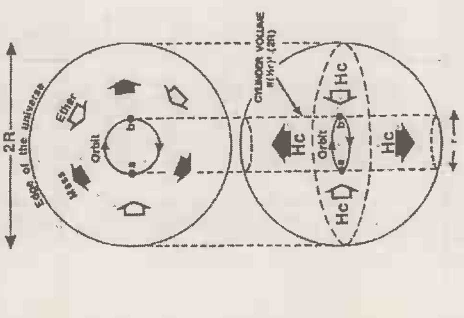
Hubble showed that the Doppler shift of light spectra from stars at increasing distances gives v/d = constant, where v is the recession speed of the star from us, and d is the distance of the star from us *at the time the light was emitted*, which is a time into the past with increasing distance because starlight travels at c = 300 mega-m/s. In reality, the distance D that the stars are really at now (15 gigayears after big bang) is equal to: D = d + (the distance the star has travelled in the time t = d/c since the light was emitted). Hence: D = d + vd/c. Hence, the true Hubble ratio is not v/d, but v/D or v/(d + vd/c). This is not constant. We can get a constant form of the original Hubble ratio only by dividing the speeds v into the travel times of the light, t, so v/t is a true constant, and is equal to vc/d or "Hc". This, Hc, has units of acceleration. Acceleration is significant because multiplied with mass it gives force, such as force of gravity.

The big bang universe has known mass and size, with an energy of 10^{56} megatons of TNT equivalent. A nuclear explosion in an air medium produces a supersonic shock wave in air which pushes outwards in a dense, wall-like compressed air shock front. Behind the shock front (Dr Harold Brode of the Rand Corporation calculates, Ann. Rev. Nuc. Sci., v 18, pp 153-202, 1968) the air density drops to as little as just 1% of normal air density. In other words, a *near vacuum* is created *near the middle*. The phenomenon you see is the afterwind. This is a wind of air pushing back towards ground zero, filling in the partial vacuum.

The afterwinds of ether from the big bang may be calculated simply from a consideration of Einstein's proof that all that exists in volume V is matter M and ether A, or: V = M + A. When the big bang occurred, the matter M moving outward reduced the matter density in the inner volume V. This has to be compensated (according to the equation V = M + A) by an *increase* in the ether. *Hence, ether flows in as matter moves outwards.* (Using calculus, dV/dt = dM/dt + dA/dt, which simplified to -dM/dt = dA/dt, because dV/dt = 0, since V is a constant.)

There is a + and - 3 milliKelvin cosine variation in the 2.734 K microwave background radiation (diagram on left). This, from Doppler energy shift theory, shows our absolute motion in space relative to the microwave backround radiation. It turns out that the Milky Way as a whole has an absolute speed of 600 km/s, so given the 15 Gyr since the big bang it will have travelled 30 million light years from the point of origin of the big bang, which is only 0.3% of the radius of the universe, so we are probably very near the middle of the universe, which would explain why it looks fairly similar in all directions around us.

Physically combining the findings above (see diagram below), we begin by setting Newton's second law and universal law equal: $F = ma = mMG/r^2$. Dividing out by mM we obtain: $a/M = G/r^2$. The ratio a/M represents the true Hubble constant, "Hc", divided by the mass of the universe concerned (the cylinder inscribing the universe in the diagram). Hence, $a/M = Hc/(\frac{1}{2}\pi r^2.R\sigma)$, where σ is the density of the universe. As Newton says, $a/M = G/r^2$, so we find: $G/r^2 = Hc/(\frac{1}{2}\pi r^2 R\sigma)$. Since the simple estimate of the radius of the universe is given by R = c/H, we see that $G = 2H^2/(\pi\sigma)$, which implies: $\sigma = 2H^2/(\pi G)$. If we take H to be 73 km/s/Mparsec, $H = 2.4\times10^{-18}\ s^{-1}$, and our predicted density of the universe (all matter, visible stars + invisible dust and neutrinos) is $5.3\times10^{-26}\ kg/m^3$. Since the nearby density of illuminated matter in space is about $4\times10^{-28}\ kg/m^3$, it is predicted that most of the matter in the universe is non-illuminated (agreeing with results from the rate of rotation of galaxies and the physics of neutrinos).



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Amplitude scale	Logarithmic, 10dB/div
Amplitude linearity	Typically ±2dB
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Calibration marker	–30dBm ±1dB at 50MHz
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Enhancing sensing

Joe Carr looks at an easy to apply and general-purpose technique for improving sensor resolution.

There's a number of different forms of spatial sensor that are used to either detect the presence of some other object, or perform imaging of objects. All of these sensors have some sort of response curve that reflects their sensitivity to a target at varying distances or angles off centre.

In **Fig. 1**, the sensor is defined as some sort of generic electro-optical sensor, for example a photo-transistor or photo-op-amp. It could just as well be an ultrasonic imaging sensor, a radio antenna, or a radar set. When researching this article, the electro-optical sensor was easily at hand, so was used.

The response of the sensor in Fig. 1 is highest immediately opposite the lens, at point X_o, as indicated by the peak voltage V_p. If the sensor and target translate relative to each other along the X axis, then the signal voltage V will rise from near zero, to V_P, and then decrease to near zero again as the target passes through the field of view.

Although the curve in Fig. 1 looks suspiciously like a bell-shaped curve, actual curves might be shaped a bit differently, but the general form is correct.

Figure 2 shows a somewhat more practical situation found in many circuits. The response curve is the same, but there is a *sensitivity threshold* below which there is little or no output. This threshold might be generated by the brightness or size of the target, by ambient lighting, or be an intentionally set circuit value. In the latter case, it is common to use such thresholds to combat the effects of noise.

In essence, the threshold level is a signal-to-noise ratio issue. The effect of the threshold is to improve the field of view, increasing the resolution, by narrowing the range of values of V that will be accepted. Even as improved by threshold detection, however, the field of view may be too great to provide adequate spatial resolution.

The *resolution* of the sensor is a measure of its ability to separate two equal targets. If the resolution is not matched to the objects being measured, then an ambiguity occurs. This is seen in popular films such as *Top Gun* where what the F-14 aircrew thought was two enemy fighters suddenly broke out to four dirty smelly bad guys – much to the dismay of the good guys. The radar resolution apparently wasn't able to distinguish two fighters flying close together.

Why improve resolution?

There's a number of practical situations where sensor resolution can cause problems. For example, if a photo sensor is used to count manufactured products coming down an assembly line, poor resolution means the items being counted would have to be further apart in order to avoid a miscount. In imaging systems the resolution can deter-

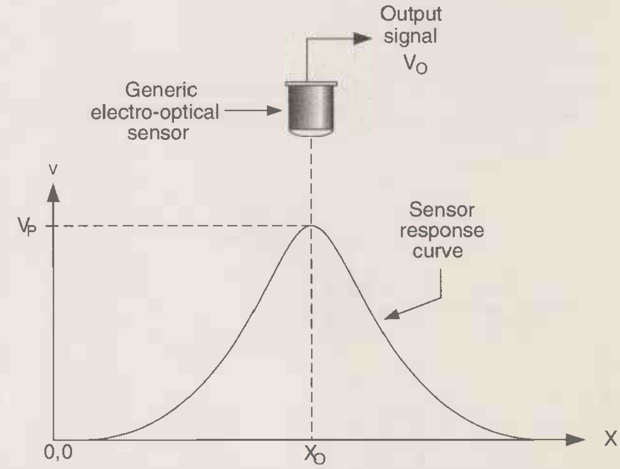

Fig. 1. A generic electro-optical sensor and its response curve.

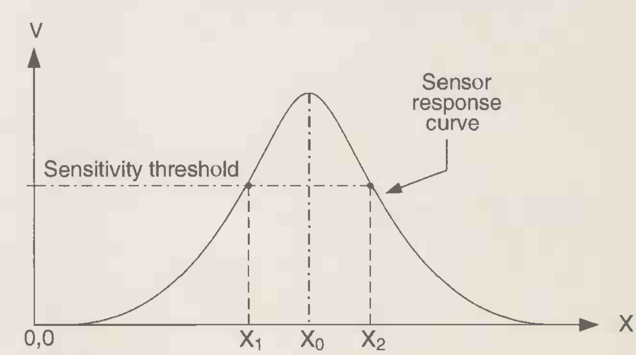

Fig. 2. Sensor response curve. A practical threshold limit narrows the field of view, but not sufficiently for high resolution operation.

mine the smallest object that can be properly displayed.

Poor resolution might cause a distortion of the object being imaged, or completely miss some important feature. It simply wouldn't do for a medical imaging system to miss your kidney stone!

In robotics, if an electro-optical sensor is used as the eyes of the robot device, then poor resolution can hamper its ability to perceive and negotiate its environment. I recall one smart lad who built a robot that tooted around the room, and when its internal battery dropped below a certain point, then it would search the walls of the room for an electrical outlet.

The robot searched by comparing a pattern of an outlet stored in memory with what it saw in the room. Poor resolution might have caused it to mistake Aunt Annie's belt buckle for the outlet, and wouldn't that have caused a family row?

Figures 3 and **4** show these effects in graphical form. In Fig. **3** a single target is in the field of view of the optical sensor. Assume that the sensor moved left to right across the target, producing the output voltage shown.

It doesn't matter whether the sensor or target moves, so long as there is relative motion between the two along the X axis. Unfortunately, the sensor field of view, which determines the resolution, is too broad, so the target appears to be smeared in the X axis. The size and exact location data are thus distorted.

The situation in Fig. 4 shows two targets in a similar situation. Again we suppose that the sensor translated left to right across the two targets. Because both targets fall inside the field of view simultaneously, they will appear smeared, but maybe with a small dip to indicate the space.

If the dip is too small to detect, then it will not be seen.

Towards better sensor resolution

Sensor resolution cannot be improved without re-designing the device. In some cases, the laws of physics might prohibit further improvement. But there is something that can be done to correct the problem.

This method is derived from a radar technique called monopulse resolution improvement, also known as MRI. There are two versions of the circuit. One uses analogue methods, but requires two sensors – a case of two being much better than one. This first approach can also be implemented in a computer version. A related method can be implemented using a digital computer, but it proves difficult in analogue circuitry.

In radar the target is illuminated with two adjacent co-planar antennas, and the returned signal processed in a special way. Assume that the two signals are V_1 and V_2. If we create sum, V_1+V_2, and difference, V_1-V_2, signals from this raw signal, then we can accomplish a tremendous resolution improvement. The equation is:

$$V_0 = \frac{V_1 + V_2}{k + \mathrm{abs}(V_1 - V_2)} \qquad (1)$$

Where V_0 is the resolution-improved signal, V_1 and V_2 are the input signals, abs indicates the absolute value of V_1-V_2 and k is a small full-scale constant

By dividing the sum by the absolute

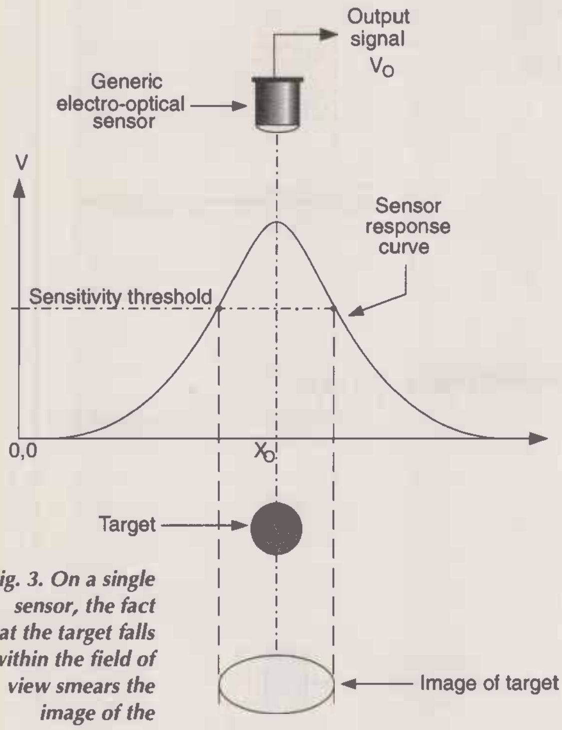

Fig. 3. On a single sensor, the fact that the target falls within the field of view smears the image of the target.

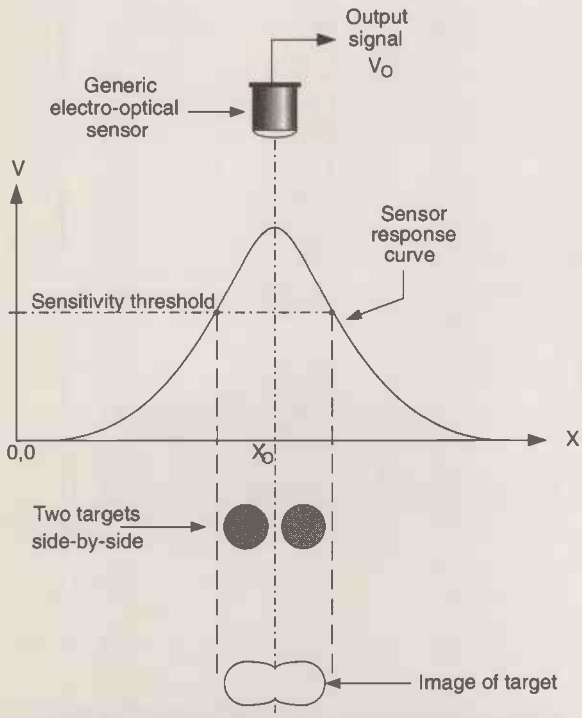

Fig. 4. Resolution problems prevent breaking out the two targets, both of which fall within the sensor's field of view.

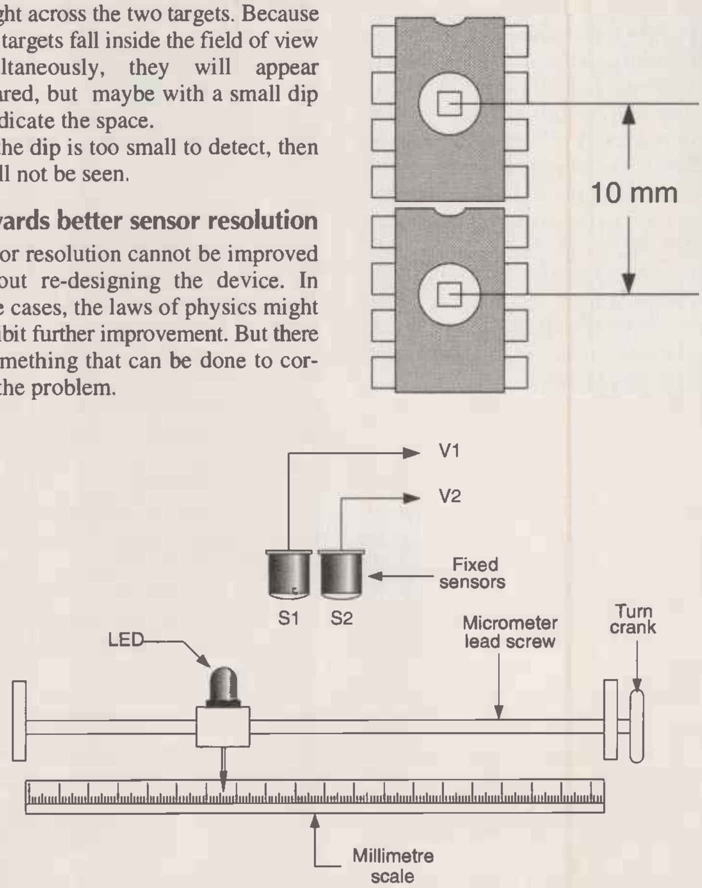

Fig. 5a) Two-sensor test device made by mating a pair of Burr-Brown OPT-101 *devices; b) test fixture that allowed the LED target to be translated along the X-axis in front the sensors.*

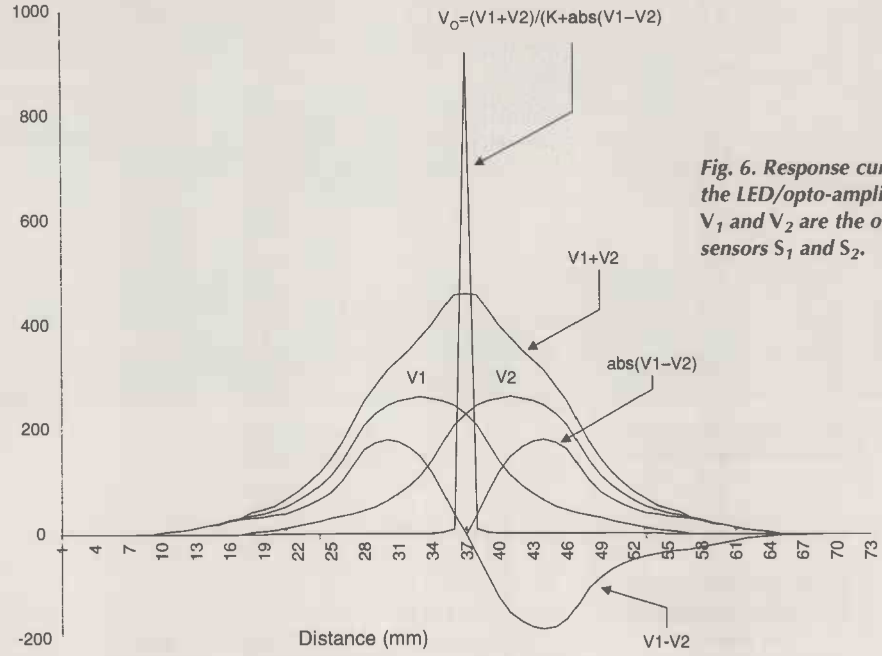

Fig. 6. Response curves of the LED/opto-amplifier trial. V_1 and V_2 are the outputs of sensors S_1 and S_2.

value of the difference at each point along the X-axis you create the resolution-improved signal V_0. The factor k is a small value constant, that is set to prevent a divide by zero error when $V_1=V_2$, or an extremely high value when V_1 and V_2 are very close in value. The value of k is set to produce a full-scale output when $V_1-V_2=0$.

Initial trials

The two-sensor approach was modelled first in an Excel spreadsheet. For the first attempt a curve similar to those in Figs 1 through 4 was converted to numbers and entered in successive cells of a single column.

Each cell represented another increment along the X-axis, while the value in the cell represented the signal voltage V at that point. When the method was applied, and graphed, there was a tremendous improvement in the resolution of the hypothetical sensor. The time came to 'cut metal' and build a real circuit model.

Figure 5 shows the actual test set-up used to acquire data. Two electro-optical sensors were obtained. The optical sensors were Burr-Brown *OPT-101* devices. These sensors are operational amplifiers with a photodiode device built-in to the transparent 8-pin DIP IC package.

The two *OPT-101* devices were spaced 10mm apart so that their cones of acceptance overlapped – which is also the minimum possible X-axis separation due to the size of the IC packages. This mounting was convenient because the two devices would fit nicely end-to-end in a single 16-pin DIP socket.

The mid-point between the two *OPT-101* devices corresponds to X_0, while the distance between them corresponds to ΔX; any particular point along the path between S_1 and S_2 is designated X_i.

The target was a red light emitting diode mounted on a movable stage on a micrometer gear rack device that measured distance of travel in millimetres. The initial position of the LED target was set so that it was outside the field of view of both S_1 and S_2.

The LED was then advanced 1mm at a time until it had traversed the entire distance from the left-most extent of the field of view of S_1 to the right-most extent of the field of view of S_2. Output voltages V_1 and V_2 from S_1 and S_2 were measured with a $3^1/_2$-digit digital voltmeter at each 1mm interval.

Those data were then entered into an Excel spreadsheet and plotted on a chart. Curves shown in **Fig. 6** represent actual results from this experiment, rather than simulated results. The experimental and modelled results were the same.

All of the curves are shown in Fig. 6: V_1, V_2, V_1+V_2, V_1-V_2, abs(V_1-V_2) and the resolution improved V_o. The V_1 and V_2 curves represent the normal field of view of the *OPT-101* devices, and therefore the effective resolution of the devices.

Note how much narrower V_o is compared with either V_1 or V_2. This response curve would resolve much finer separations and produce superior images than either S_1 or S_2 alone.

A single-sensor solution

The two-sensor method of sensor resolution improvement produces startling results – but at the cost of two sensors. It is easy to implement in analogue circuitry, and can also be implemented in digital circuitry.

Another approach uses a single sensor and a look-ahead technique to synthesise V_2. It is easily implemented digitally, but is quite difficult to implement in analogue circuitry.

Assume that the values of V_1 from the sensor are a series V_i in which each value represents the signal amplitude at sequential locations along the X-axis: $V_1\ V_2\ V_3 \ldots V_{ith}$

Each value of V_i represents a value of V_1 in eqn 1 above. The corresponding value of V_2 in eqn 1 is found by taking a subsequent value of V_1 that is displaced a distance N, which is an integer, from V_i. Thus, in terms of eqn 1, $V_1=V_i$ and $V_2=V_{i+N}$.

Equation 1 can be rewritten to the form:

$$V_0 = \frac{V_i + V_{i+N}}{k + (V_i + V_{i+N})}$$

When the V_1 data from the experiment are plotted, the resultant curves are very similar to those of Fig. 6 and demonstrate very nearly the same degree of resolution improvement.

I also found that a limited amount of 'tuning' of resolution can be done by selecting values of N. However, with the 1mm spacing used in the experiment, values of N that were greater than 5 showed essentially the same curves.

In both the single-sensor and two-sensor methods there exists the possibility of creating a selectable beam width sensor system. Signal V_0 could be the narrow beam-width signal, V_1+V_2 can be the wide beam-width signal, and V_1 or V_2 can be the medium beam-width signal.

In summary

This sensor resolution improvement method is a variant on the monopulse-resolution improvement, or MRI, method used for many years in radar technology. It appears to have applications in ultrasonic imaging – which resembles radar in basic approach – and in any instrumentation problem where sensor resolution is an issue.

Perhaps one day I will try it on a metal detector and go searching for artifacts on an American Civil War battlefield near my home in Virginia. ■

Further reading

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Skolnik, Merrill, 1980, 'Introduction to Radar Systems,' New York: McGraw-Hill.

Stimson, George W., 1983, 'Introduction to Airborne Radar Systems,' El Segundo, CA: Hughes Aircraft Co.

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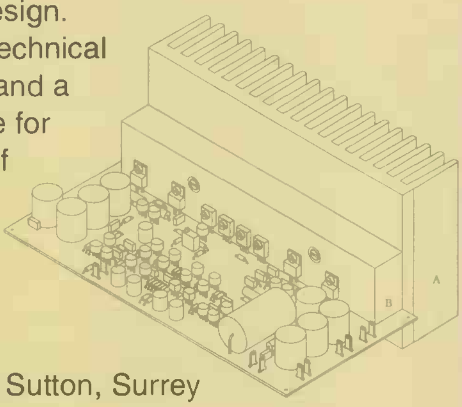

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Power into 8Ω load	100W
Small-signal bandwidth before the output filter	20Hz (–0.1dB), 1.3MHz (–3dB)
Unity gain frequency before the output filter	22MHz
Output noise (BW=80kHz, input terminated with 50Ω	42µV rms
Measured output offset voltage	+32mV

Distortion performance

V_{out}, pk-pk	1kHz	20kHz
5	0.0030%	0.0043%
10	0.0028%	0.0047%
20	0.0023%	0.0061%
40	0.0028%	0.0110%
80	0.0026%	0.0170%

Slew rate

Positive slew-rate	+320V/µs
Negative slew-rate	–300V/µs

Improving VHF Yagis

With the aid of a 300Ω 12-element design example, Richard Formato explains how high-impedance Yagis improve VHF antenna system performance, and why a 300Ω pair performs better than coaxial cable.

One of the reasons why building good antennas is a challenge is that key parameters are often incompatible. This note examines the incompatibility between very efficient transmission lines, which have a high characteristic impedance, and typical Yagis, which have low input impedance.

Antenna optimisation often ignores the transmission line. The line is selected only after the Yagi design is complete, and it is almost always coaxial. The antenna/transmission line system is then made to work by adding a matching network.

But this approach is not necessarily the best. Designing the antenna and transmission line together may provide better overall performance, a point which is illustrated by the 12-element Yagi discussed below.

Feed-system-loss at VHF

The problem at VHF is that coaxial cable loss increases dramatically with frequency, often robbing the antenna system of its full potential.

On 2 metres, for example, the matched-line attenuation of widely used RG-8 foam-dielectric coaxial cable is about 2.1dB/100 feet[1], which is quite substantial. And this is the minimum value, because attenuation increases as SWR goes up – which also reduces system bandwidth.

Another source of attenuation is the required matching network and balun. Even the simplest network introduces some loss in its electronic components and coax connectors, and these losses are usually much higher at VHF than at lower frequencies.

At VHF, where fractions of a decibel can make a difference, using a transmission line with the lowest possible loss is obviously very important. The best transmission line is air-insulated open wire (not 'window' line).

An open wire line made with #12 AWG conductors has an attenuation of only 0.25 dB/100 feet on 2 metres[(1)]. For comparison, 200 feet of open wire line delivers 89% of the input power to the antenna, while the same length of RG-8 delivers only 38%.

But there are problems with open wire line. Practical conductor spacings result in high characteristic impedance, which is difficult to match to a low impedance Yagi. **Table 1** shows the centre-to-centre conductor spacing to achieve different line impedance with common wire sizes. The impedance is computed from the formula $Z_0=276\log(2S/d)$, where S is the centre-to-centre spacing and d is the conductor diameter, both in the same units.[2]

High-impedance Yagis

The easiest way to take advantage of the extremely low attenuation of open wire line is to design a good Yagi with a *high* input impedance. One approach is to use a half-wave folded dipole as the driven element[(3)]. Another is to increase the input impedance of the usual centre-fed linear dipole driven element (DE) by proper placement of the array's parasitic elements. The feasibility of this design approach will be demonstrated by a 12-element Yagi that provides a nearly perfect match to 300-ohm open wire line and excellent overall performance. An added advantage is that the antenna and transmission line are both balanced, so that the balun connecting the unbalanced transmitter output to the line can be placed at the transmitter instead of at the antenna.

Free modelling software – YGO2

The high impedance array was

designed using *Yagi Genetic Optimizer* version 2, which is a freeware program available on the web.[4] *YGO2* models Yagis using NEC-2D (Numerical Electromagnetics Code, Ver. 2, Double Precision). This is also available on the web[4] or directly from ACES.[5] Essential data from the YGO2 configuration file, and the NEC-2D input file for the final optimised array, are in the panel entitled 'Yagi modelling data'.

The optimisation was done iteratively. The initial runs optimised only the input impedance by setting the coefficients *d*, *e* and *f* to zero, and by assigning a low value to coefficient *a*.

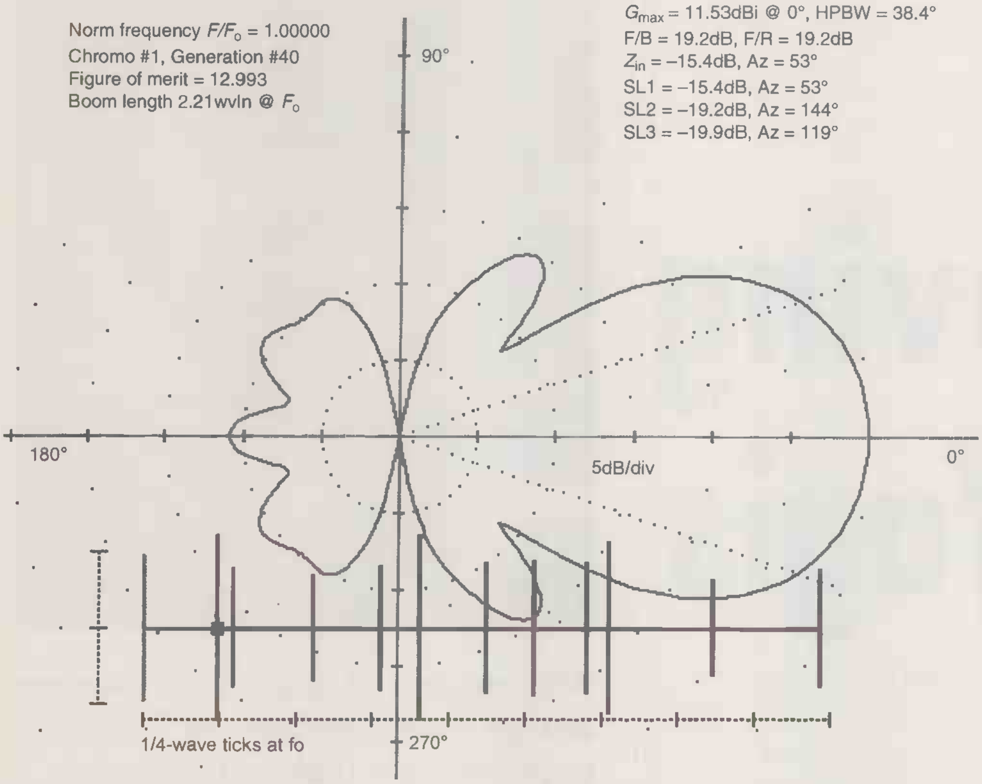


Fig. 1. Azimuthal pattern for the genetically-optimised 12–element Yagi using the NEC file YGO_1.40 listed later.

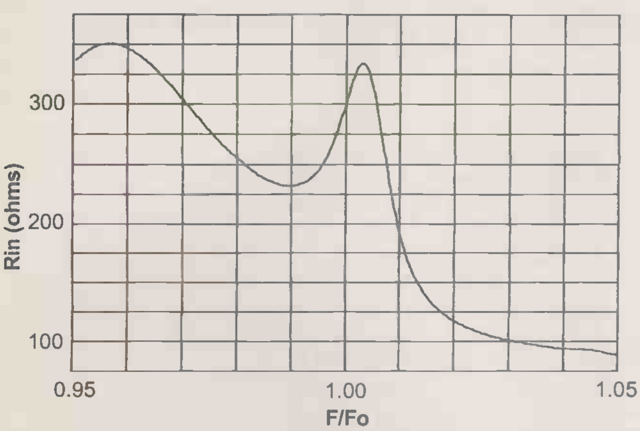


Fig. 2. Input resistance of the 12-element high-impedance Yagi around the centre normalised frequency.

Once a geometry was evolved that was a good match to 300Ω, the corresponding chromosome was used to seed subsequent optimisation runs in which coefficients *a*, *d*, and *e* were gradually increased (*f* was always zero).

This process was repeated until the desired balance between Z_{in}, gain, FB and FR was achieved. All runs were at one frequency, i.e. 146MHz. The element diameter of 0.0122 waves is equal to 1in (25.4mm) divided by the wavelength at 144MHz (299.8/frequency in megahertz).

Somewhat fat elements were chosen to broaden the Yagi's response. Smaller diameter elements – but not too small – should provide more gain at the expense of bandwidth, but this was not investigated in detail.

A 12-element, 300Ω Yagi

The geometry of the YGO2-optimised Yagi appears in **Table 2**. I refer to this antenna as the 'high-Z' Yagi because it matches 300Ω line. All dimensions are in wavelengths at the design frequency F_o.

Length is the end-to-end element length. *Spacing* is the separation along the boom from the previous element. *Position* is the distance along the boom from element No 1 – the reflector. Element No 2 (DE) is driven at its centre – i.e. it's a centre-fed linear dipole. All elements have the same diameter of 0.0122 wave at F_o.

Figure 1 shows the YGO2 output screen, which plots the E-plane azimuthal radiation pattern and provides a scale representation of the array. The display is annotated with key performance data. The radiation pattern is very clean, and its structure is typical of well-designed Yagis.

One interesting aspect of this Yagi is its unusual geometry. Unlike 'standard' designs having progressively shorter directors with increasing spacing away from the DE, the element lengths do not follow any pattern. Some of them are quite out of the ordinary.

The DE, for example, is the second-longest element at 0.5992 wave. The reflector, REF, is much shorter, at 0.4839 wave, and the longest element is element No 6, D4, which is 0.6 wave. Usually, the reflector is the longest element, DE is less than half-wave and the directors become progressively shorter.

Table 1. Conductor spacing in inches for various wires sizes and characteristic impedances.

AWG	Zo (Ω) 300	350	400	450
10	0.622	0.945	1.434	2.176
12	0.494	0.749	1.137	1.725
14	0.392	0.594	0.902	1.369

Table 2. High-Z Yagi geometry. Dimensions in wavelengths at F_o. Note that all elements are 0.0122 wave diameter.

El #	Length	Spacing	Position
1 (REF)	0.4839	0.0000	0.0000
2 (DE)	0.5992	0.2397	0.2397
3 (D1)	0.3865	0.0500	0.2897
4 (D2)	0.3453	0.2635	0.5532
5 (D3)	0.4094	0.2229	0.7761
6 (D4)	0.6000	0.1224	0.8985
7 (D5)	0.4306	0.2212	1.1197
8 (D6)	0.4412	0.1559	1.2756
9 (D7)	0.4271	0.1700	1.4456
10 (D8)	0.5647	0.0729	1.5185
11 (D9)	0.3141	0.3482	1.8667
12 (D10)	0.3824	0.3447	2.2114

Not quite a director

Another unusual feature is the position of director No 1, or D1, which is very close to DE, separated only by 0.05 of a wave. This director appears primarily to function as an impedance matching parasitic, rather than as a true director. Even though it contains 12 elements, this Yagi looks more like an 11-element array.

The similarity to an 11-element array is even more apparent when the 12-element high-Z Yagi is compared to the 144MHz family of designs in The ARRL Antenna Book.[6]

The ARRL 11-element array has a boom length of 2.2 waves and a gain of 14.15dBi, i.e. 12dBd. It has a front-to-back ratio, shortened to FB, of 19dB, an input resistance of 38Ω, and an unspecified input reactance. This is presumably tuned out by a matching network. Because this array is intended to operate with a low-impedance transmission line, I will refer to it as the 'low-Z Yagi'.

The high-Z array in Fig. 1 is the same length as the low-Z antenna (2.21 waves), and has a gain of 11.53 dBi, and FB and front-to-rear (FR) ratios of 19.2dB. The high-Z array is essentially resonant at F_o (Z_{in}=299.3+j2.9Ω), which provides a nearly perfect SWR of 1.01 on 300Ω open-wire line with no matching of any kind. In contrast, the low-Z Yagi's SWR relative to 50Ω is 1.32 without matching, assuming the antenna is resonant – almost certainly not the case.

Relative performance

The performance of the high and low-Z arrays is similar in many respects, but there are differences. It appears that the extra element in the high-Z Yagi increases the DE input impedance while contributing little to the gain. In fact, taken together, DE and D1 look much like a folded dipole.

It is interesting that YGO2's solution places D1 as close as possible to DE – at 0.05 waves. Had the minimum spacing in YGO2.CFG been lower, say 0.025 wave, YGO2 might have placed D1 even closer, which would make DE/D1 look even more like a folded dipole. There's more on YGO.CFG in the panel entitled 'Yagi modelling data'.

Another (and more important) difference is that the high-Z Yagi's gain is lower than the low-Z's by 2.62dB. But, while this gain reduction would be significant if realised, it will not occur in practice because of the different levels of transmission line loss.

If the high and low-Z *systems* are compared, taking into account line loss, then the high-Z Yagi may well be the better antenna. It provides more overall gain than the low-Z array for any transmission line longer than 142 feet – comparing #12 AWG open wire and foam-dielectric RG-8. This result excludes matching network and connector losses. These are likely to be much higher for the coaxial cable than for the open-wire line, which again gives the high-Z Yagi an edge.

Another advantage of the high-Z design is that open-wire line is easily coupled to an unbalanced-transmitter output. Simple, very low loss air-core inductive circuits that act as balun and impedance matching transformer are readily available.[7] This circuit can be located at the transmitter, which is not possible with coaxial cable because the balun must then be at the antenna input.

Placing the network in the shack reduces the weather-related losses and maintenance that are inevitable with devices mounted outdoors.

Open-wire line is also favoured because of its effect on signal-to-noise ratio. In a receiver-noise limited system, SNR is reduced by the amount of transmission line attenuation.

At VHF, the extremely low attenuation of open wire line is advantageous both for receiving and transmitting. Open-wire line provides better SNR than coax, and it delivers more power to the antenna.

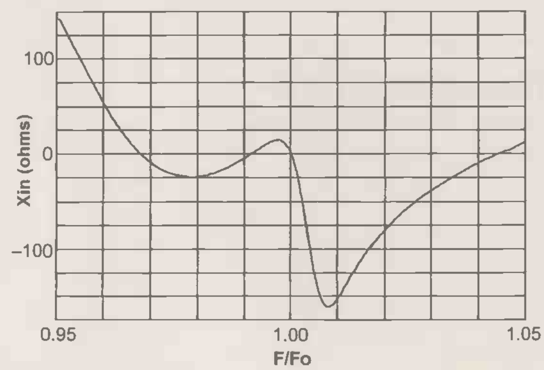
Input impedance and SWR

Figures 2-7 provide detailed performance data for the high-Z Yagi computed by NEC-2D. On each plot, the abscissa is the normalised frequency, F/F_o, where F_o is the design frequency at which the array dimensions are computed.

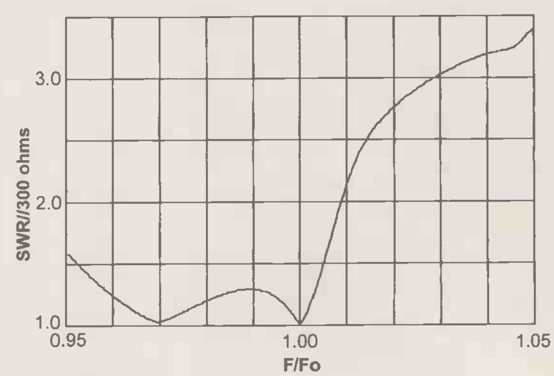
For convenience, the ratio F/F_o is denoted by a lower case, italic f. Each parameter is plotted over a 10% bandwidth ($0.95 \le f \le 1.05$).

Figure 2 shows the input resistance. The design value of 300Ω is achieved at three frequencies, f=0.97, 1.00, and 1.006. Maximum resistance is 350Ω at f=0.957, with a secondary peak of about 330Ω at f=1.003. The resistance is between 200 and 350Ω for frequencies from 0.95 to just below 1.01.

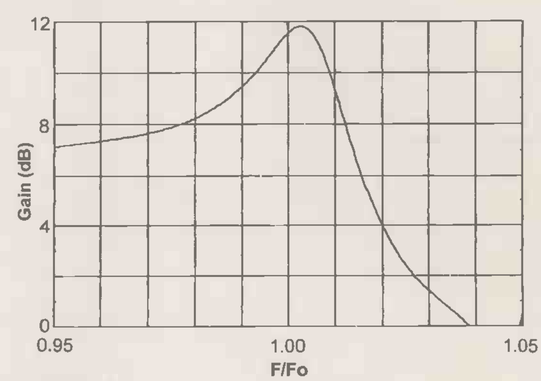
Input reactance is plotted in **Fig. 3**.



Input reactance.

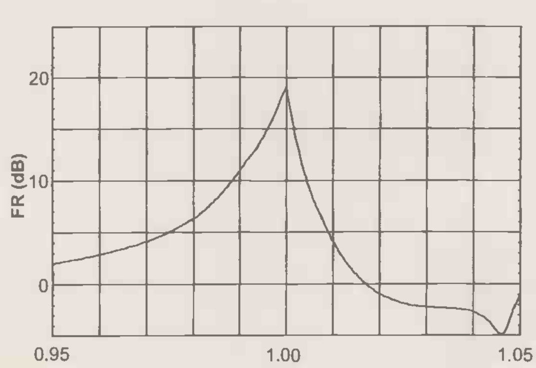


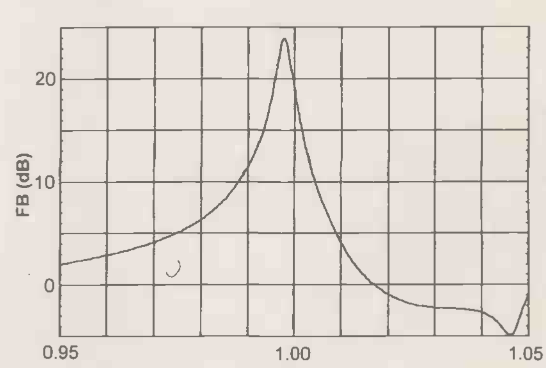
Standing-wave ratio.



Forward gain

Figs 3-7. Performance curves for the 12-element Yagi.





Front-to-back ratio.

Four resonances, i.e. where X_{in}=0, occur at f=0.968, 0.992, 1.00, and 1.044. The maximum reactance of about +140Ω (inductive) occurs at f=0.95, while the minimum of −161Ω (capacitive) is at f=1.008.

Reactance is less than 10% of the desired 300Ω input resistance from f=0.963 to 1.002 (3.9%). For practical purposes, the high-Z Yagi may be considered resonant over this entire range of frequencies.

The most important antenna impedance parameter is SWR, which is plotted in Fig. 4. At the lower band edge, the SWR is just over 1.5. It is below 1.5 from f=0.953 to 1.005, yielding a 1.5:1 SWR bandwidth of 5.2%. The 2:1 SWR bandwidth is more than 5.9%, which is quite good.

Gain and FB/FR Ratios

Forward gain in dBi – i.e. decibels relative to an isotropic radiator – appears

Yagi modelling data

Essential Data from File YGO2.CFG

Name of NEC executable file	NEC2D100.EXE
# NEC input files/gen in output	5
starting with generation number	20

Number of Elements in Array	12
Number of Segments per Element	7
Feed System Zo	300 ohms resistive
Assume Feed Reactance Tuned Out?	NO

Population Size	10 (# chromosomes)
Max # Generations	1
Save Percentage	2.0 (% best chromos/gen saved)
Crossover Probability	0.8000
Mutation Probability	0.0200
Max Mutation Rate	2 bits/chromosome

Selection method # 1
(1-binary tournament, 2-proportionate)
Minimum Fitness [0-1] 0.5 (proportionate only)

FoM Terminology

Gfwd	Forward Gain (dBi)
FB	Front-to-Back Ratio (dB)
FR	Front-to-Rear Ratio (dB)
Rin	Feed Point Input Resistance, ohms
Xin	Feed Point Input Reactance, ohms
MaxSLL	Maximum Sidelobe Level (dB//Gfwd)
^	Exponentiation
*	Multiplication
/	Division
ABS	Absolute Value

Figure-of-Merit (averaged over all frequencies):
FoM={a*Gfwd–b*ABS(Zo–Rin)
–c*ABS(Xin)+d*FB+e*FR–f*MaxSLL}/(a+b+c+d+e+f)

——— FREQUENCY TABLE ———

FREQUENCIES USED - 1

Freq #	Freq(MHz)	DE	a	b	c	d	e	f
1	146.00	2	260.0	4.0	6.0	1.0	85.0	0.0
2	144.20	2	40.0	2.0	3.0	0.0	0.0	0.0
3	144.30	2	40.0	2.0	3.0	0.0	0.0	0.0
4	144.40	2	40.0	2.0	3.0	0.0	0.0	0.0
5	144.50	2	40.0	2.0	3.0	0.0	0.0	0.0
6	144.60	2	40.0	2.0	3.0	0.0	0.0	0.0
7	144.70	2	40.0	2.0	3.0	0.0	0.0	0.0
8	144.80	2	40.0	2.0	3.0	0.0	0.0	0.0
9	144.90	2	40.0	2.0	3.0	0.0	0.0	0.0
10	145.00	2	40.0	2.0	3.0	0.0	0.0	0.0
11	145.10	2	40.0	2.0	3.0	0.0	0.0	0.0
12	145.20	2	40.0	2.0	3.0	0.0	0.0	0.0
13	145.30	2	40.0	2.0	3.0	0.0	0.0	0.0
14	145.40	2	40.0	2.0	3.0	0.0	0.0	0.0
15	145.50	2	40.0	2.0	3.0	0.0	0.0	0.0

Target FoM - 9999 (not normalised)

Crossover allowed only at gene boundary? YES
Print Percent - 20 (% chromos/gen printed in output file)

Use Seed Chromosome? YES
Seed Chromo:
011000010000000000000000001011011000000000000000011111100000000
000000000100001000000000000000100110111010000000000100011011111
1111000000000100101001111011000000000100001100001111000000000000
111100001101100000000000100010100001110000000010110000000110000
000000001001010101100010000000011100101

Print Chromo Sequences in YGO.DAT? NO

——— GENE TABLE ———

Gene #	Name	Length (bits)	Min (wvln)	Max (wvln)
1,	"Refl_Length ",	8,	0.3000,	0.6500
2,	"Refl_Radius ",	8,	0.00610,	0.00610
3,	"Refl_Spacing ",	8,	0.0000,	0.0000
4,	"DE_Length ",	8,	0.3000,	0.6500
5,	"DE_Radius ",	8,	0.00610,	0.00610
6,	"DE_Spacing ",	8,	0.0500,	0.428
7,	"D1_Length ",	8,	0.3000,	0.6500
8,	"D1_Radius ",	8,	0.00610,	0.00610
9,	"D1_Spacing ",	8,	0.0500,	0.428
10,	"D2_Length ",	8,	0.3000,	0.6500
11,	"D2_Radius ",	8,	0.00610,	0.00610
12,	"D2_Spacing ",	8,	0.0500,	0.428
13,	"D3_Length ",	8,	0.3000,	0.6000
14,	"D3_Radius ",	8,	0.00610,	0.00610
15,	"D3_Spacing ",	8,	0.0500,	0.500
16,	"D4_Length ",	8,	0.3000,	0.6000
17,	"D4_Radius ",	8,	0.00610,	0.00610
18,	"D4_Spacing ",	8,	0.0500,	0.500
19,	"D5_Length ",	8,	0.3000,	0.6000
20,	"D5_Radius ",	8,	0.00610,	0.00610
21,	"D5_Spacing ",	8,	0.0500,	0.500
22,	"D6_Length ",	8,	0.3000,	0.6000
23,	"D6_Radius ",	8,	0.00610,	0.00610
24,	"D6_Spacing ",	8,	0.0500,	0.500
25,	"D7_Length ",	8,	0.3000,	0.6000
26,	"D7_Radius ",	8,	0.00610,	0.00610
27,	"D7_Spacing ",	8,	0.0500,	0.500
28,	"D8_Length ",	8,	0.3000,	0.6000
29,	"D8_Radius ",	8,	0.00610,	0.00610
30,	"D8_Spacing ",	8,	0.0500,	0.500
31,	"D9_Length ",	8,	0.3000,	0.6000
32,	"D9_Radius ",	8,	0.00610,	0.00610
33,	"D9_Spacing ",	8,	0.0500,	0.500
34,	"D10_Length ",	8,	0.3000,	0.6000
35,	"D10_Radius ",	8,	0.00610,	0.00610
36,	"D10_Spacing",	8,	0.0500,	0.500

——— End of Gene Table ———

**************** End of File YGO2.CFG *************************

NEC-2D Input file for YGO2-optimised array

```
CM NEC File: YGO_1.40 (Run ID: 11-16-1998, 23:40:45)
CM Chromosome #1, Generation #40
CM Figure-of-Merit = 12.993
CM Feed System Zo = 300 ohms resistive
CE
GW 1,7,0.,.241961,0.,0.,–.241961,0.,.0061
GW 2,7,.239741,.299608,0.,.239741,–.299608,0.,.0061
GW 3,7,.289741,.1932355,0.,.289741,–.1932355,0.,.0061
GW 4,7,.5532,.172647,0.,.5532,–.172647,0.,.0061
GW 5,7,.776141,.204706,0.,.776141,–.204706,0.,.0061
GW 6,7,.898494,.3,0.,.898494,–.3,0.,.0061
GW 7,7,1.11967,.215294,0.,1.11967,–.215294,0.,.0061
GW 8,7,1.275552,.220588,0.,1.275552,–.220588,0.,.0061
GW 9,7,1.445552,.2135295,0.,1.445552,–.2135295,0.,.0061
GW 10,7,1.518493,.282353,0.,1.518493,–.282353,0.,.0061
GW 11,7,1.866728,.157059,0.,1.866728,–.157059,0.,.0061
GW 12,7,2.211434,.1911765,0.,2.211434,–.1911765,0.,.0061
GE
GN–1
FR 0,1,0,0,299.8,0.
EX 0,2,4,0,1.,0.
RP 0,1,181,1001,90.,0.,0.,1.,10000.
XQ
EN
```

in Fig. 5. Maximum gain is 11.8dBi at f=1.003. The gain is above 10dBi from f=0.993 to 1.009 – a 10dBi gain bandwidth of 1.6%. The half-power –3dB frequencies are 0.986 and 1.011, yielding a –3 dB bandwidth of 2.5%.

The FB ratio in Fig. 6 peaks at 23.9dB at f=0.998. FB is above 20dB from f=0.996 to 1.00 (0.4%), above 15dB from 0.993 to 1.002 (0.9%), and greater than 10dB from 0.988 to 1.004 (1.6%).

The FR in Fig. 7 shows similar behaviour, but its peak value is lower. Maximum FR is 19.2dB at f=1.00. It is above 15dB from f=0.996 to 1.002 (0.6%), and greater than 10dB from 0.988 to 1.004 (1.6%).

In summary

The high-Z Yagi is a high-performance antenna. It directly matches extremely low loss, balanced 300Ω open wire line. As a system, this array fed by open wire line outperforms an optimised 11-element array of the same boom length fed by RG-8 coaxial cable, as long as the transmission line is longer than 142 feet – ignoring matching network and balun losses.

The 12-element high-Z system provides more overall gain and better SNR. If the coaxial matching network/balun has higher losses than the open wire network – which is very likely – the high-Z Yagi provides better performance even for lines shorter than 142 feet.

This design example shows that there are compelling reasons for designing high-Z Yagis to operate directly with high impedance open wire lines. The resulting antenna system can provide excellent performance which may well exceed that of more conventional designs.

High-Z Yagis merit serious consideration by any amateur who is concerned about optimising antenna system performance – especially at VHF where small differences are significant. ■

References

1. 'The ARRL Antenna Book,' 17th ed., R. Dean Straw, editor, American Radio Relay League, Inc., Newington, CT 06111, USA, 1994, Fig. 22, p. 24-16.
2. *ibid.*, Eq. (20), p. 24-14.
3. 'Antennas,' 2nd ed., John D. Kraus, McGraw-Hill Inc., New York, 1988, p. 483.
4. Ray Anderson, WB6TPU's, 'NEC Archive' website, URL: http://www.qsl.net/wb6tpu.
5. Applied Computational Electromagnetics Society (ACES) Attn: Dr Richard W. Adler, ACES Executive Officer, ECE Dept., Code ECAB, Naval Postgraduate School, 833 Dyer Road, Room 437, Monterey, CA 93943-5121 USA.
6. 'The ARRL Antenna Book,' 17th ed., R. Dean Straw, editor, American Radio Relay League, Inc., Newington, CT 06111, USA, 1994, Table 11, p. 18-25.
7. *ibid.*, Figs. 2(A), 2(C), p. 25-3.

NEW PRODUCTS

Please quote Electronics World when seeking further information

Chip inductors

Pulse has announced 0603-sized wirewound chip inductors in 20 values from 1.8 to 120nH. The

PE-0603CD is compatible with Coucraft's 0603 series. RF applications include phase lock loop circuits and RF amplifiers in GSM mobile phones. They have a flat surface for pick-and-place compatibility, and tin-lead side metallisation.
Pulse
http://www.pulseeng.com
Tel: 01483 401700
Enquiry No 501

Fast boot block flash

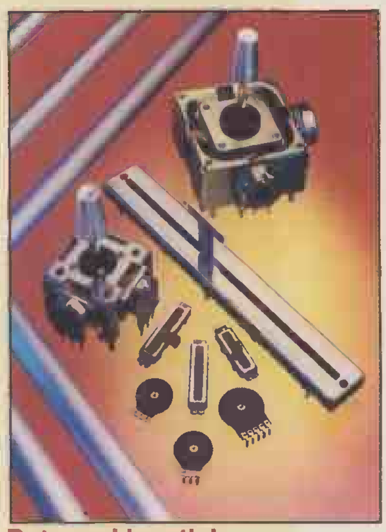
Supporting both Asynchronous Page Mode (21ns) and Synchronous Burst Mode (54MHz) operation, Intel's fast boot block memory is claimed to provide up to five times the system performance of standard low-voltage 80ns asynchronous flash memory. The interface provides glueless connection to the leading high performance processors.
The asymmetrically blocked architecture is supported by Intel's flash data integrator (FDI) software, to enable both code and data to be contained in the same fast boot block device. Suitable for pager, set-top box, handheld GPS, and automotive applications, the flash memory is available from Thame Components in 8- and 16-Mbit densities in industry standard 56-lead SSOP, 56-ball BGA packages.
Thame Components
Tel: 01844 261188
Enquiry No 502

Transceiver chipset

Analog Devices has announced the Softcell multicarrier transceiver chipset for use in cellular, PCS, wireless local loop, micro and pico cell, and smart antenna base stations. It is a functionally complete end-to-end, IF-to-digital transceiver that lets software radios be deployed for wireless infrastructure applications. Base stations containing the chipset can be modified by adding services and channels, and changing wireless standards incrementally. Operators can use and move between air interface standards, for example GSM, PHS and D-Amps. The architecture eliminates redundant channel radios for transmitters and receivers. The chipset is optimised for four RF carrier channels but is expandable.
Analog Devices
http://www.analog.com
Tel: 01932 266014
Enquiry No 504

Sensor subsystem

Wolfson has launched the WM8181 CIS and CCD sensor image processing subsystem for low power scanners. Available in a 14-pin SOIC, it operates from single 5 or 3.3V or split 5V analogue and 3.3V digital supplies. It has a 12-bit, 2Msample/s a-to-d converter with internal reference generation and a differential input. An optional clamp is available for linking to CCD linear image sensors. The serial output has a maximum data rate of 24Mbit/s. Requiring two clocks and supply decoupling, the product typically consumes 23mW at 3.3V operation and less than 1μW in power down mode.
Wolfson Microelectronics
http://www.wolfson.co.uk
Tel: 0131 667 9386
Enquiry No 505



Pots and joysticks

Quiller Electronics has introduced potentiometers and joysticks from Tsubame Radio. The slider and rotary potentiometers are for use as faders and volume controls. Both types are available in SMT versions.
Quiller Electronics
http://www.quiller.com
Tel: 01202 436770
Enquiry No 503

TFT flat panel controllers

Philips Semiconductors has introduced video and graphics controllers for TFT flat panel displays. For use in multisync flat-panel colour monitors and LCD projectors, the SAA6712, SAA6712A (XGA resolution) and SAA6721 (SXGA resolution) RGB to TFT graphics engines perform horizontal and vertical scaling, colour adjustment, and on-screen display generation and insertion. Pixel and timing signals are generated to display the resulting images on various TFT displays. The SAA6712A and SAA6721 also accept 48-bit YUV video inputs, making them suitable for multimedia display applications. All three accept RGB data in 24-bit single-pixel format or 48-bit double-pixel interlaced format. They are packaged in 292-pin PBGAs.
Philips Semiconductors
Tel: 00 31 40 272 2091
Enquiry No 509

Video multiplexer

Linear Technology has introduced the LT1675-1 single 2:1 video multiplexer by combining a two-channel multiplexer with a fixed gain amplifier. It eliminates the need for an external buffer amplifier and two gain setting resistors. Channel switching time is 2.5ns and it can toggle between sources over 100MHz with a slew rate more than 1100V/μs and a –3dB bandwidth of 250MHz. A disable function lets the output be put into a high impedance state for cascading stages, so multiple inputs can be multiplexed to one output. This function reduces power dissipation to nearly zero in the off parts.
http://www.linear.com
Tel: 01276 677676
Enquiry No 510

Audio accelerator

Atmel subsidiary Dream has added a PCI audio accelerator to its sound synthesis IC family. The Sam9777 delivers up to 64 streaming audio voices at up to 48kHz sampling frequency. It provides interactive full bandwidth sound positioning on two to six speakers. Reverb, chorus, echo, pitch shifting, four band equaliser and surround sound 3DMidi have been combined with a GS compliant sound set under Roland licence.
Atmel
Tel: 01276 686677
Enquiry No 508

CAN bus microcontroller

Fujitsu has launched a CAN bus microcontroller for automotive and industrial control systems. The MB91360 is based on a modular building block idea and uses as its nucleus the firm's FR 32-bit Risc microprocessor core and CAN bus macro. Triple full-CAN bus interfaces are combined with onboard single voltage flash or ROM. The first device, the MB91F361, is fabricated in 0.35μm technology and has a CPU that clocks at 64MHz internally, with 512kbyte flash memory, 1kbyte instruction cache and 16kbyte RAM. The device integrates

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on-chip stepper motor controllers, real-time watch timer, sound generator, LED drivers and PPGs for light dimmers.
Fujitsu
http://www.fujitsu.com
Tel: 01628 504600
Enquiry No 507

SM package

International Rectifier has introduced the SMD-0.5 package, which weighs 1g and measures 7.5 by 10.1 by 2.9mm. For power supply, motor drive and linear regulator applications, it can be used with any Rad-Hard MOSFET, Hexfred diodes, Schottky or standard Hexfet power MOSFET device.
International Rectifier
Tel: 01883 732020
Enquiry No 506

LCD controller

Epson has introduced the SED1374 colour and monochrome LCD graphics controller with an embedded 40kbyte SRAM display buffer. Hardware portrait mode supports virtual display, allowing panning of larger images than panel size. Split screen display mode provides multiple images on screen simultaneously. Display formats supported including 4 and 8-bit mono and colour LCD, 16-bit colour LCD, single panel and dual panel passives, and active matrix TFT and TFD. Display modes allow for up to 16 levels of grey scale and 256 level colour. Power saving capabilities include hardware and software suspend modes and LCD power down sequencing. Operating voltage is 2.7 to 5.5V.
Epson Electronics
http://www.epson-electronics.de
Tel: 0 49 89 140 05-349
Enquiry No 511

BGA sockets

Actel has announced ball-grid array sockets for use with its field programmable gate arrays. The sockets suit the prototyping environment and are compatible with the firm's MX and SX devices as well as upcoming reprogrammable FPGA families. The sockets have zero insertion force so the device is not stressed before, during or after testing. They use the same pad layout on the PCB that the device will eventually occupy. This avoids changes to the PCB during the crossover between prototyping and production.
Actel
Tel: 01256 305600
Enquiry No 512

Connector cover

A nine-way D-subminiature connector cover from Stadium Cables has an inner area large enough to hold a small PCB. The PCB can be double sided if required. The two-part cover snap locks together using internal latches to give a finish similar in appearance to a moulded single-piece hood. The hood can be supplied in black plastic or be metallised for resistance to EMI and RFI. It is supplied in kit form, with two thumbscrews, grommet and strain relief. The grommet can be customised if required.
Stadium Cables
Tel: 01622 690470
Enquiry No 514

Capacitors

Pedoka is supplying Tokin capacitors with values from 0.022 to 5.0F. For use as non-battery reserve power sources, they provide currents from 1 to 100mA and protect microcomputers from power shutdowns of several seconds. They can maintain the contents of low-dissipation CMOS volatile memories for several months. Each capacitor consists of an electric double layer at the interface between activated carbon particles, and sulphuric acid solution as an electrolyte. The two electrodes are separated by an ionically conducting but electrically insulating porous membrane. Conductive rubber membranes contain the electrode and electrolyte material and make contact to the cell.
Pedoka
Tel: 01462 422433
Enquiry No 513

Multi-banked DIMM module

Ambar Cascom has introduced a multi-bank synchronous and synchronous burst, flow-through SRAM module from White Electronic Designs. Made on the dual-key 168 DIMM format, the 3.3V device supports densities from 1 to 8Mbyte and has a maximum height of 3.8cm. Clock to data access times of 10, 12 and 15ns are available. Electrical characteristics include byte write, global write and global reads, and linear and sequential burst is supported via the mode pin. The multi-banked synchronous burst flow-through architecture alleviates additional propagation delays at address boundaries that can occur with address mapping schemes.
Ambar Cascom
Tel: 01296 332264
Enquiry No 515

LCD controller

Harting has introduced sensors and actuators using the company's Harax termination system. The axial insulation displacement termination system is claimed to combine the advantages of connectors and screwed cable glands.
Harting
Tel: 01604 766686
Enquiry No 516

LED lamps

QT Optoelectronics has announced surface mount chip type LED lamps. The QTLP600C and QTLP601C come in 0603 packages. They have a 100° viewing angle and moisture-proof packaging. Applications include panel illumination, push-button back lighting, LCD back lighting, and membrane switches. The QTLP600C is 0.8mm and the QTLP601C 0.6mm high. Both have water clear optics and come in four colours.
QT Optoelectronics
http://www.qtopto.com
Tel: 01296 394499
Enquiry No 517

LCDs

Trident Displays is distributing Hexa-Chain video LCD products including component form modules from 6.4 to 16.3cm at resolutions up to 0.25 VGA (960 x 234) and housed displays from 10.2 to 16.3cm using the same modules. Features include input from typically 10 to 30V, brightness up to 300cd/m^2, temperature range typically −30 to +80°C, Pal and NTSC input auto-switching, and antiglare screens.
Trident Displays
http://www.tridentdisplays.co.uk/
Tel: 01737 780790
Enquiry No 518

Embedded SBC

The EM-520 embedded single board computer from Steatite Systems combines sound and display features with a 10Mbps Ethernet LAN. The integrated graphics and audio sound package has VGA and LCD functionality with an NTSC and Pal TV output interface and sound blaster compatibility. It is for multimedia applications and is year 2000 tested. The graphics and audio features are supported by an onboard Cyrix Media GXi processor and Cx5520 companion chip. The processor is custom designed for multimedia applications supporting 1280 x 1024 x 8 and 1024 x 768 x 16 BPP, and including unified L1 cache memory.
Steatite Systems
http://www.steatite.co.uk
Tel: 0121 678 6888
Enquiry No 519

DCP boards

Transtech DSP has announced a family of boards ready for the introduction of Analog Devices' Sharc II DSP for applications such as radar, sonar and imaging. The Analog Devices ADSP-21160 is a floating-point DSP with six link ports for scalability. It has up to 600Mflops performance and 100Mbyte/s datacomms per link port. Power consumption is 2 to 3W. The boards include formats for PCI, VME, CompactPCI and PMC mezzanine, and are capable of up to 4.8Gflops performance per board slot.
Transtech
http://www.transtech-dsp.com
Tel: 01494 464432
Enquiry No 520

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Development kit

Toshiba has launched a development kit for embedded applications using the company's TX 32-bit Risc microcontrollers based on the MIPS R3000A architecture. The Topas TX Risc starter kit includes an evaluation board and an evaluation version of the MULTI development environment from Green Hills Software with C and C++ compiler and a PC utility for flash programming.
Toshiba Electronics
Tel: 01276 694730
Enquiry No 522

EMC analysers

Hewlett-Packard has introduced automated in-house precompliance measurement systems to help manufacturers meet EMC regulations. The E7400 A series analysers are for EMC testing throughout the design and evaluation processes. Users require no special knowledge or training to perform precompliance measurements.
http://www.hp.com/
Tel: 00 49 6441 92460
Enquiry No 523

3V SiGe power amplifier

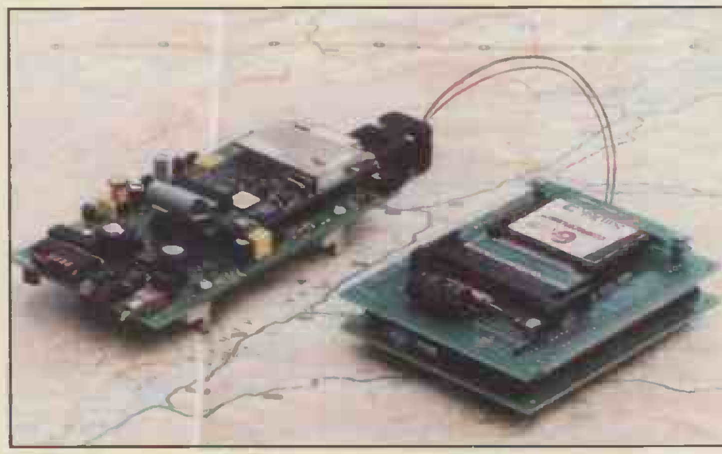
Temic Semiconductors has announced a 3V silicon germanium (SiGe) power amplifier, the TST0912, for GSM mobile phones. It is for single-band operation in the 900MHz range (GSM900), and allows the use of single-cell Li-ion or three-cell NiMH batteries. SiGe does not require negative supply voltage. The amplifier has 35dBm maximum output power. Its power-added efficiency value is 50 per cent.
Temic
http://www.temic-seml.com
Tel: 01270 252209
Enquiry No 524

LEDs

Surface-mount chip-type LEDs with integrated lenses have been introduced by Hewlett-Packard. These lenses concentrate the emitted light into a typical 70° viewing angle. Applications include illuminating buttons and switches on panels, transferring light to optical light pipes used to illuminate panel legends, backlighting legends on car radios and dashboard devices, and as status indicators on computers, datacomms equipment and other office systems.
Hewlett-Packard.
http://www.hp.com/
Tel: 00 49 6441 92460
Enquiry No 525

PSUs

Astec has Introduced four 250W switched mode PSUs. Housed in a 51mm high case, the LPS250-CEF models let the single rail output be configured by the user from 3 to 6, 6 to 12, 12 to 24 and 24 to 48V DC. There are two supervisory outputs of 5 and 12V DC at 100 and 500mA respectively. The single wire current sharing feature supports the use of multiple units in parallel. This parallel capability also allows n+1 redundant configurations.
Astec
Tel: 01384 842211
Enquiry No 535



Data logger

The TDS2020 data logger from Triangle can collect information such as pressure, temperature, rotation rate and doors open or closed in Excel spreadsheet compatible format. Applications include agriculture, security, transport and shipping. Using GPS satellites, information on latitude, longitude, date and time can be incorporated. The storage medium is a PCMCIA or CompactFlash card for transfer to a PC. The module measures 100 by 80 by 30mm. The recording format on the CompactFlash card is Windows compatible.
Triangle
http://www.triangledigital.com/
Tel: 01845 527437
Enquiry No 536

Processor board

The Microbus MAT 900 combines two 450MHz Pentium II processors, SCSI, 10 and 100Mbit autoswitching Ethernet, and AGP video on a board that fits into a slot in a PICMG backplane. The processors share a common sink-tunnel, creating a rigid box structure for secure retention of the processor assembly. This also allows fitting of the DIMMs above the processors, so OEMs can fit half-length cards in the slot next to the processor card in the PICMG backplane. The AGP video is based on the 3DLabs Permedia Two chipset and supports 4 or 8Mbyte SGRAM video memory. The PCI SCSI-3 supports transfers up to 40Mbyte/s.
Microbus
Tel: 01628 537333
Enquiry No 521

LED bulbs

Switchtec has introduced Sirena LED bulbs to replace low voltage filament bulbs in panels where it is difficult to change dead bulbs. Life time is claimed to be 100 000 hours. They

are resistant to vibration. There are six colours to choose from, including blue and bright green, and two sizes, 3 and 5mm diameter.
Switchtec Electronics
Tel: 01785 818600
Enquiry No 526

24-bit ADC

The LTC2400 24-bit analogue-to-digital converter. Its accuracy with total unadjusted error is less than 10ppm and it operates without external crystals, software and additional circuitry. Integral non-linearity is 2ppm at 2.5V reference, with offset of 1ppm and drift of 0.01ppm/°C. Full-scale error is within 4ppm with drift 0.02ppm/°C. RMS noise is 0.3ppm at 1.5μV.
Linear Technology
Tel: 01276 67676
Enquiry No 527

64-bit PCI compliant PLD

Thame Components is shipping fully 66MHz, 64-bit PCI compliant programmable logic devices. Recent enhancements to Altera's FLEX10KE family of PLDs means that the this 2.2V device family is specified to meet the required timing specifications contained within PCI Rev 2.1. In addition Thame has announced the availability of two intellectual property (IP) cores to support the 66MHz, 64-bit master/target function. One was developed by Altera's in-house team and the other by a member of the Altera Megafunction Partners Program (AMPP). These cores provide designers with a 100 per cent soft implementation of the PCI Rev 2.1 specification. The range comprises five devices. The EPF10K50E contains 2880 logic elements, with 40kbits of memory contained in the patented EAB structure
Thame Components
Tel: 01844 261188
Enquiry No 529

Chip capacitors

Syfer has introduced 0805 feed-through chip capacitors for EMI

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suppression, broadband i/o filtering and DC power line applications. They are rated at 100 or 50V. Capacitances are from 22 to 820pF in COG and 470pF to 47nF in X7R dielectrics. Current rating is 300mA and DC resistance less than 0.6Ω. Applications include power supplies, automotive, and multimedia add-on cards.
Syfer Technology
Tel: 01603 629721
Enquiry No 530

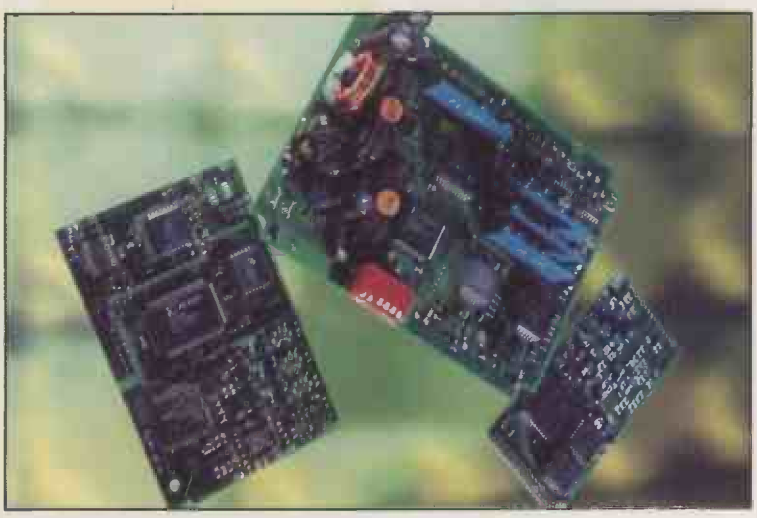
Broadcast interface

Faraday's extended range of interface cards provides a small, convenient pre-designed solution to common conversions required between broadcast equipment.

Each card is a modular solution for a particular function, allowing easy addition of differing output and input options. This can ease design and production costs and logistics with guaranteed performance simplifying test procedures.

All relevant SMPTE and ITU specifications are adhered to. Each card contains all the filtering and buffering required to interface to external equipment and therefore require only the minimum of external components. They provide a complete drop in solution to conversion.

Common applications include the production of analogue outputs for video monitoring in digital equipment by the addition of a single card as specified by the end customer, or a permanent SDI input for different grade broadcast monitors or LCD displays.
Faraday Technology Ltd.
Tel.,01782 661501; fax 01782 630101
Enquiry No 534



Schottky diode

Zetex has introduced a Schottky diode in the SOD323 surface mount package. The ZHCS400 supports a continuous forward current of 400mA for a typical forward voltage of 425mV. This Superbat device has continuous, average and pulsed current performance providing 400mA, 1A and 6.75A respectively. Power dissipation at an ambient temperature of 25°C is 250mW. Forward voltage is 270mV at 50mA and 440mV at 500mA.
Zetex
Tel: 0161 622 4422
Enquiry No 531

Microchip

Microchip Technology has expanded its PIC16F87x family of 8-bit flash microcontrollers with the 28-pin PIC16F873 and 40-pin PIC16F874. To support these devices, the company has also introduced the MPlab in-circuit debugger evaluation kit that uses the MCU family and the firm's in-circuit serial programming to debug source code in the application, debug hardware in real-time and program a target PICI6F87x device. Operating under the MPlab integrated development environment, the kit provides real-time code execution, in-circuit debugging, built-in programmer and 3.0 to 5.5V operating range.
Microchip Technology
Tel: 0118 921 5858
Enquiry No 533

Debugger

The Huntsville BMD background mode debugger from Great Western Microsystems is for use with PowerPC, 683xx, 68HC12 and Coldfire devices and works with 3 or 5V systems, with power supplied by the target or the included external power supply. It interfaces with Motorola debug or IBM JTAG port connections and has flexible breakpoints, flash programming support, control over target resources and the CPU, multiple compiler support, and HMI's Sourcegate II source level debugger.
http://www.gwg.co.uk/
Tel: 01179 830333
Enquiry No 532

Valve data

For restorers of vintage radios, G C Arnold Partners has re-introduced the Wireless World Valve Data Booklet at £2.95.
Tel. 01202 658474
Enquiry No 533 ■

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HP New Colour Spectrum Analysers LAST FEW ONLY
HP141T+ 8552B IF + 8553B RF -1KHZ -110Mc/s - £500.
HP141T+ 8552B IF + 8554B RF -100KHz -1250M - £600.
HP141T+ 8552B IF + 8556A RF - 20Hz-300KHz - £400.
HP141T+ 8552B IF + 8555A 10 MC/S-18GHzS - £1000.
HP8443A Tracking Gen Counter 100KHz-110Mc/s - £200
HP8445B Tracking Preselector DC to 18GHz - £250.
HP8444A Tracking Generator • 5-1300Mc/s - £450.
HP8444A OPT 059 Tracking Gen • 5-1500Mc/s - £650.
HP35601A Spectrum Anz Interface - £300.
HP4953A Protocol Anz - £400.
HP8970A Noise Figure Meter + 346B Noise Head - £3k.
HP8755A+B+C Scalar Network Anz PI - £250 + MF 180C - Heads 11664 Extra - £150 each.
HP3709B Constellation ANZ £1,000.
HP11715A AM-FM Test Source - £350.
FARNELL TVS70MKII PU 0-70V 10 amps - £150.
MARCONI 6500 Network Scaler Anz - £500. Heads available to 40GHz many types in stock.
Mixers are available forANZs to 60GHz.
HP6131C Digital Voltage Source + -100V½ Amp.
HP5316A Universal Counter A+B.
Marconi TF2374 Zero Loss Probe - £200.
Racal/Dana 2101 Microwave Counter - 10Hz-20GHz - with book as new £2k.
Racal/Dana 1250-1261 Universal Switch Controller + 200Mc/s PI Cards and other types.
Racal/Dana 9303 True RMS Levelmeter + Head - £450.
TEKA6902A also A6902B Isolator - £300-£400.
TEK CT-5 High Current Transformer Probe - £250.
HP Frequency comb generator type B406 - £400.
HP Sweep Oscillators type 8690 A+B + plug-ins from 20Mc/s to 18GHz also 18-40GHz.
HP Network Analyser type 8407A + 8412A + 8601A - 100Kc/s - 110Mc/s - £500 - £1000.
HP 8410-A-B-C Network Analyser 110Mc/s to 12 GHz or 18 GHz - plus most other units and displays used in this set-up - 8411a-8412-8413-8414-8418-8740-8741-8742-8743-8746-8650. From £1k.
Racal/Dana 9301A-9302 RF millivoltmeter - 1.5-2GHz - qty in stock £250-£400.
Racal/Dana Modulation Meter Type 9009-9008 - 8Mc/s - 1.5GHz - £150/£250 – 9009A £350.
Marconi RCL Bridge type TF2700 - £150.
Marconi Microwave 6600A 1 sweep osc., mainframe with 6650PI - 18-26.5 GHz or 6651 PI - 26.5-40GHz-£750 or PI only £600. MF only £250.
Gould J3B test oscillator + manual - £150.
Marconi 6155A Signal Source-1 to 2GHz - LED - £400.
Barr & Stroud Variable filter EF3 0.1Hz-100Kc/s + high pass + low pass - £150, other makes in stock.
Racal/Dana 9300 RMS voltmeter - £250.
HP 8750A storage normalizer - £400 with lead + S.A. or N, A
Marconi mod meters type TF2304 - £250 – TF2305 - £1,000.
Racal/Dana counters-99904-9905-9906-9915-9916-9917-9921-50Mc/s-3GHz - £100 - £400 - all fitted with FX standards.
HP180TR. HP181T, HP182T mainframes £300 - £500.
HP432A-435A or B-436A-power meters + powerheads to 60GHz - £150 - £1750 - spare heads available.
HP3586A or C selective level meter - £500.
HP86222A+B Sweep PI -01-2.4GHz + ATT £1000-£1250.
HP86290A+B Sweep PI-2 - 18GHz - £1000 - £1250.
HP8620C Mainframe - £250. IEEE £350.
HP8615A Programmable signal source - 1MHZ - 50Mc/s - £1k.
HP3455/3456A Digital voltmeter - £400.
HP5370A Universal time interval counter - £1k.
HP5335A Universal counter - 200Mc/s-£1000.
HP3552A Transmission test set - £350.
TEKTRONIX 577 Curve tracer + adaptors - £900.
TEKTRONIX 1502/1503 TDR cable test set - £400.
HP8699B Sweep PI YIG oscillator .01 - 4GHz - £300. 8690B MF-£250. Both £500.
Dummy Loads & Power att up to 2.5 kilowatts FX up to 18GHz - microwave parts new and ex equipt - relays - attenuators - switches - waveguides - Yigs - SMA - APC7 plugs - adaptors etc. qty. in stock.
B&K Items in stock - ask for list.
Power Supplies Heavy duty + bench in stock - Farnell - HP - Weir - Thurlby - Racal etc. Ask for list. Large quantity in stock, all types to 400 amp - 100Kv.
HP8405A Vector voltmeter - late colour - £400.
HP8508A Vector voltmeter - £2500.
HP8505A Network Anz 500KHz-1.3GHz - £1000.
HP8505A + 8502A or 8503A test sets- £1200 - £1500.
HP8505A + 8502A or 8503A + 8501A normalizer - £1750-£2000.
Phillips 3217 50Mc/s oscilloscopes - £150-£250.
Phillips 3296 350Mc/s IR remote oscilloscope - £500.
R&S APN 62 LF S/G 0.1Hz – 260KHz with book - £500.
Wavetek–Schlumberger 4031 Radio communication test set

LIGHT AND OPTICAL EQUIPMENT
Anritsu ML93A & Optical Lead Power Meter - £250.
Anritsu ML93B & Optical Lead Power Meter - £350.
Power Sensors for above MA96A - MA98A - MA913A - Battery Pack MZ95A.
Anritsu MW97A Pulse Echo Tester.
PI available - MH914C 1.3 - MH915B 1.3 - MH913B 0.85 - MH925A 1.3 - MH929A 1.55 - MH925A 1.3GI - MH914C 1.3SM - £500 + one P.I.
Anritsu MW98A Time Domain Reflector.
PI available - MH914C 1.3 - MH915B 1.3 - MH913B 0.85 - MH925A 1.3 - MH929A 1.55 - MH925A 1.3GI - MH914C 1.3SM - £500 + one P.I.
Anritsu MZ100A E/O Converter.
+ MG912B (LD 1.35) Light Source + MG92B (LD 0.85) Light Source £350.
Anritsu MZ118A O/E Converter.
+MH922A 0.8 O/E unit + MH923 A1.3 O/E unit £350.
Anritsu ML96B Power Meter & Charger £450.
Anritsu MN95B Variable Att. 1300 £100.
Photo Dyne 1950 XR Continuous Att. 1300 - 1500 £100.
Photo Dyne 1800 FA. Att £100.
Cossor-Raytheon 108L Optical Cable Fault Locator 0-1000M 0-10kM £200.
TEK P6701 Optical Converter 700 MC/S-850 £250.
TEK OF150 Fibre Optic TDR – £750.
HP81512A Head 150MC/S 950-1700 £250.
HP84801A Fibre Power Sensor 600-1200 £250.
HP8158B ATT OPT 002+011 1300-1550 £300.
HP81519A RX DC-400MC/S 550-950 £250.
STC OFR10 Reflectometer – £250.
STC OFSK15 Machine jointing + eye magnifier – £250.

COMMUNICATION EQUIPMENT
Anritsu ME453L RX Microwave ANZ – £350.
Anritsu ME453L TX Microwave ANZ – £350.
Anritsu MH370A Jitter Mod Oscillator – £350.
Anritsu MG642A Pulse Patt Gen. £350.
System MS02A Timer & Digital Printer – £500.
Complete MS65A Error Detector.
Anritsu ML612A Sel Level Meter – £400.
Anritsu ML244A Sel Level Meter – £300.
W&G PCM3 Auto Measuring Set – £300.
W&G SPM14 Sel Level Meter – £300.
W&G SPM15 Sel Level Meter – £350.
W&G SPM16 Sel Level Meter – £400.
W&G PS19 Level Gen – £500.
W&G DA20+DA1 Data ANZ £400.
W&G PMG3 Transmission Measuring Set – £300.
W&G PSS16 Generator – £300.
W&G PS14 Level Generator – £350.
W&G EPM-1 Plus Head Milliwatt Power Meter – £450.
W&G DLM3 Phase Jitter & Noise – £350
W&G DLM4 Data Line Test Set – £400.
W&G PS10 & PM10 Level Gen. – £250.

MISCELLANEOUS ITEMS
HP 3852A Data Acquisition Control Unit + 44721A 16ch input £1,000.
HP 4261 LCR meter – £650.
HP 4274 FX LCR meter – £1,500.
HP 4951A Protocol ANZ – £500.
HP 3488 Switch Control Unit + PI Boards – £500.
HP 75000 VXI Bus Controllers + E1326B-DVM-quantity.
HP 83220A GSM DCS/PCS 1805-1990MC/S convertor for use with 8922A – £2,000.
HP 1630-1631-1650 Logic ANZ's in stock.
HP 8754A Network ANZ 4-1300MC/S + 8502A + cables – £1,500.
HP 8754A Network ANZ H26 4-2600MC/S + 8502A + Cables – £2,000.
HP 8350A Sweeper MF + 83540A PI 2-8.4GHZ + 83545A PI 5.9-12.4GHZ all 3 – £3,500.
HP MICROWAVE TWT AMPLIFIER 489A 1-2GHZ-30DB – £400.
HP PREAMPLIFIER 8447A 0.1-400MC/S – £200. Dual – £300.
HP PREAMPLIFIER 8447D 0.01-1.3GHZ – £400.
HP POWER AMPLIFIER 8447E 0.01-1.3GHZ – £400.
HP PRE + POWER AMPLIFIER 8447F 0.01-1.3GHZ – £500.
HP 3574 Gain-Phase Meter 1HZ-13MC/S OPT 001 Dual – £400.
MARCONI 2305 Modulation Meter-50KHZ-2.3 GHZ – £1,000.
MARCONI 2610 True RMS Meter – £450.
MARCONI 893B AF Power Meter (opt Sinad filter) – £250-£350.
MARCONI 6950-6960B Power Meters + Heads – £400-£900.
MARCONI SIGNAL SOURCE-6055-6056-6057-6058-6059 – FX Range 4-18GHZ– £250-£400.
RACAL 1792 COMMUNICATION RX – £500 early – £1,000 – late model with back lighting and byte test.
RACAL 1772 COMMUNICATION RX – £400-£500.
PLESSEY PR2250 A-G-H COMMUNICATION RX – £500-£900.
TEK MODULE MAINFRAMES – TM501-502-503-504-506-TM5003-5006.
TEK PI 5010-M1 – Prog Multi Interface – £250. FG Prog 20MC/S Function Gen – £400 – S1 Prog Scanner – £250 – DM Prog DMM – £400.
TEK 7000 OSCILLOSCOPE MAINFRAMES – 7603-7623-7633-7834-7854-7904-7904A-7104 – £150-£1,000.
TEK 7000 PI's – 7A11-7A12-7A13-7A18-7A19-7A22-7A24-7A26-7A29-7A42-7B10-7B15-7B53A-7B80-7B85-7B92A-7D15-7D20.
TEK 7000 – 7S11-7S12-7S14-7M11-S1-S2-S3A-S4-S5-S6-S51-S53-S54.

RADIO COMMUNICATION TEST SETS
BULK PURCHASE ONLY FROM JOHNS RADIO
HP 8920A RF Communication Test Set – Opts 003-004-007-011 unit contains Syn Signal Gen-Distortion Meter-Mod Meter-Digital Oscilloscope etc. 1000MC/S – £1,500 each.
MOTOROLA R2600A plus RLN4260A RF Test Set – £3,000.
MARCONI 2955 RF Test Sets-1000MC/S – £1,200 each.
MARCONI 2958 RF Test Sets-1000MC/S – £1,300 each.
MARCONI 2960 RF Test Sets-1000MC/S – £1,400 each.
MARCONI 2955A RF Test Sets-1000MC/S – £2,000 each.
MARCONI 2960A RF Test Sets-1000MC/S – £2,500 each.
ANRITSU MS555A2 Radio Comm Anz-1000M/Cs – £1,200 each.
MARCONI 2019A SYNTHESIZED SIGNAL GENERATORS – 80KC/S-1040MC/S – AM-FM all functions tested off the pile as received from Gov – in average used condition – £650 each or in original Gov cartons 1st class condition each fitted with IEEE plus added protection front cover lid containing RF-IEEE-mains cables + N to BNC adaptor – Attenuator etc. + Instruction Book – fully checked to high standards in our own workshop – £1k.
MARCONI 2022E SYNTHESIZED SIGNAL GENERATOR – 10KC/S-1.01GHZ AM-FM – made small and light for portability being the naval version – all functions tested off the pile as received from Gov – in average used condition – £1,000 each or in original Gov cartons as new condition – each fitted with IEEE + added protection front cover lid containing RF-IEEE – mains cables-N to BNC Adaptor – Attenuator-50-75OHM adaptor etc. + Instruction Book – fully checked to high standards in our own workshop – £1,250 each.
WE KEEP IN STOCK HP and other makes of RF Frequency doublers which when fitted to the RF output socket of a S/Generator doubles the output frequency EG.50-1300MC/S to 50-2600MC/S price from £250 – £450 each.

SPECTRUM ANALYZERS
HP 3580A 5HZ-50KHZ – £750.
HP 3582A Dual 0.2HZ-25.5KHZ – £1,500.
HP 3585A 20HZ-40MC/S – £3,500.
HP 3588A 10HZ-150MC/S – £7,500.
HP 8568A 100HZ-1.5GHZ – £3,500.
HP 8568B 100HZ-1.5GHZ – £4,500.
HP 8590B 9KC/S-1.8GHZ – £4,500.
HP 8569B 10MC/S (0.01-22GHZ) – £3,500.
HP 3581A Signal Analyzer 15HZ-50KHZ – £400.
TEK491 10MC/S-12.4GHZ + 12.4-40GHZ – £500.
TEK492 50KHZ-21GHZ OPT 2 – £2,500.
TEK492P 50KHZ-21GHZ OPT 1-2-3 – £3,500.
TEK492AP 50KHZ-21GHZ OPT 1-2-3 – £4,000.
TEK495 100KHZ-1.8GHZ – £2,000.
HP 8557A 0.01MC/S-350MC/S – £500 + MF180T or 180C – £150 – 182T – £500.
HP 8558B 0.01-1500MC/S – £750 – MF180T or 180C – £150 – 182T – £500.
HP 8559A 0.01-21GHZ – £1,000 – MF180T or 180C – £150 – 182T – £500.
HP 8901A AM FM Modulation ANZ Meter – £800.
HP 8901B AM FM Modulation ANZ Meter – £1,750.
HP 8903A Audio Analyzer – £1,000.
HP 8903B Audio Analyzer – £1,500.
MARCONI 2370 SPECTRUM ANALYZERS – HIGH QUALITY – DIGITAL STORAGE – 30HZ-110MC/S Large qty to clear as received from Gov – all sold as is from pile complete or add £100 for basic testing and adjustment – callers preferred – pick your own from over sixty units – discount on qtys of five or more.
A EARLY MODEL GREY – horizontal alloy cooling fins – £200.
B LATE MODEL GREY – vertical alloy cooling fins – £300.
C LATE MODEL BROWN – as above (few only) – £500.

OSCILLOSCOPES
TEK 465-465B 100MC/S + 2 probes – £250-£300.
TEK 466 100MC/S storage + 2 probes – £200.
TEK 475-475A 200MC/S-250MC/S + 2 probes – £300-£350.
TEK 2213-2213A-2215-2215A-2224-2225-2235-2236-2245-60-100MC/S – £250-£400.
TEK 2245 4ch 150MC/S + 2 probes – £450.
TEK 2245A 4ch 150MC/S + 2 probes – £600.
TEK 2245B 4ch 150MC/S + 2 probes – £750.
TEK 468 D.S.O. 100MC/S + 2 probes – £500.
TEK 485 350MC/S + 2 probes – £550.
TEK 2465 4ch-300MC/S – £1,150.
TEK 2465A 4ch-350MC/S – £1,550.
TEK 2465ACT 4ch-350MC/S – £1,750.
TEK 2465B 4ch-400MC/S – £2,000.
TEK D.S.O. 2230 -100MC/S + 2 probes – £1,000.
TEK D.S.O. 2430 -150MC/S + 2 probes – £1,250.
TEK D.S.O. 2430A -150MC/S + 2 probes – £1,750.
TEK D.S.O. 2440 -300MC/S + 2 probes – £2,000.
TEK TAS 475-485 -100MC/S-20MC/S-4 ch + 2 probes – £900-£1.1K.
HP1740A – 100MC/S + 2 probes – £250.
HP1741A – 100MC/S storage + 2 probes – £200.
HP1720A – 1722A - 1725A - 275MC/S + 2 probes – £300-£400.
HP1744A – 100MC/S storage - large screen – £250.
HP1745A – 1746A - 100MC/S - large screen – £350.
HP54100A – 1GHz digitizing – £500.
HP54200A – 50MC/S digitizing – £500.
HP54501A – 100MC/S digitizing – £500.
HP54100D – 1GHZ digitizing – £1,000.

MICROWAVE COUNTERS – ALL LED READOUT
EIP 351D Autohet 20Hz-18GHz – £750.
EIP 371 Micro Source Locking – 20Hz-18GHz – £850.
EIP 451 Micro Pulse Counter – 300MC/S-18GHz – £700.
EIP 545 Microwave Frequency Counter – 10Hz-18GHz – £1K.
EIP 548A Microwave Frequency Counter – 10HZ-26.5GHz – £1.5k.
EIP 575 Microwave Source Locking – 10Hz-18GHz – £1.2K.
EIP 588 Microwave Pulse Counter – 300MC/S-26.5GHz – £1.4K.
SD 6054B Micro Counter 20HZ-24GHZ – SMA Socket – £800.
SD 6054B Micro Counter 20HZ-18GHZ – N Socket – £700.
SD 6054D Micro Counter 800MC/S-18GHz – £600.
SD 6246A Micro Counter 20Hz-26GHz – £1.2K.
SD 6244A Micro Counter 20Hz-4.5GHz – £400.
HP5352B Micro Counter OPT 010-005-46GHz – new in box – £5k.
HP5340A Micro Counter 10HZ-18GHz – Nixey – £500.
HP5342A Micro Counter 10HZ-18-24GHz – £800-£1K – OPTS 001-002-003-005-011 available.
HP5342A + 5344S Source Synchronizer – £1.5K.
HP5345A 500MC/S 11 Digit LED Readout – £400.
HP5345A + 5354A Plugin – 4GHz – £700.
HP5345A + 5355A Plugin with 5356A 18GHz Head – £1K.
HP5385A 1GHz 5386A-5386A 3GHz Counter – £1K-£2K.
Racal/Dana Counter 1991-160MC/S – £200.
Racal/Dana Counter 1992-1.3GHz – £600.
Racal/Dana Counter 9921-3GHz – £350.

SIGNAL GENERATORS
HP8640A – AM-FM 0.5-512-1024MC/S – £200-£400.
HP8640B – Phase locked – AM-FM-0.5-512-1024MC/S – £500-£1.2K. Opts 1-2-3 available.
HP8654A – B AM-FM 10MC/S-520MC/S – £300.
HP8656A SYN AM-FM 0.1-990MC/S – £900.
HP8656B SYN AM-FM 0.1-990MC/S – £1.5K.
HP8657A SYN AM-FM 0.1-1040MC/S – £2K.
HP8657B SYN AM-FM 0.1-2060MC/S – £3K.
HP8660C SYN AM-FM-PM-0.01-1300MC/S-2600MC/S – £2K.
HP8660D SYN AM-FM-PM-0.01-1300MC/S-2600MC/S – £3K.
HP8673D SYN AM-FM-PM-0.01-26.5 GHz – £12K.
HP3312A Function Generator AM-FM 13MC/S-Dual – £300.
HP3314A Function Generator AM-FM-VCO-20MC/S – £600.
HP3325A SYN Function Generator 21MC/S – £800.
HP3325B SYN Function Generator 21MC/S – £2K.
HP8673-B SYN AM-FM-PH 2-26.5 GHz – £6.5K.
HP3326A SYN 2CH Function Generator 13MC/S-IEEE – £1.4K.
HP3336A-B-C SYN Func/Level Gen 21MC/S – £400-£300-£500.
Racal/Dana 9081 SYN S/G AM-FM-PH-5-520MC/S – £300.
Racal/Dana 9082 SYN S/G AM-FM-PH-1.5-520MC/S – £400.
Racal/Dana 9084 SYN S/G AM-FM-PH-.001-104MC/S – £300.
Racal/Dana 9087 SYN S/G AM-FM-PH-.001-1300MC/S – £1K.
Marconi TF2008 AM-FM-Sweep 10KC/S-510MC/S – £200 Fully Tested to £300, as new + book + probe kit in wooden box.
Marconi TF2015 AM-FM-10-520MC/S – £100.
Marconi TF2016A AM-FM 10KC/S-120MC/S – £100.
Marconi TF2171/3 Digital Synchronizer for 2015/2016A – £50.
Marconi TF2018A AM-FM SYN 80KC/S-520MC/S – £500.
Marconi TF2019A AM-FM SYN 80KC/S-1040MC/S – £650-£1K.
Marconi TF2022E AM-FM SYN 10KC/S-1.01GHz – £1K-£1.2K.
Farnell ESG1000 AM-FM SYN 10Hz-1GHz – £500.
R & S SMPD AM-FM-PH 5KHz-2720MC/S – £3K.
Anritsu MG3601A SYN AM-FM 0.1-1040MC/S – £1.2K.

ITEMS BOUGHT FROM HM GOVERNMENT BEING SURPLUS. PRICE IS EX WORKS. SAE FOR ENQUIRIES. PHONE FOR APPOINTMENT OR FOR DEMONSTRATION OF ANY ITEMS, AVAILABILITY OR PRICE CHANGE. VAT AND CARRIAGE EXTRA. ITEMS MARKED TESTED HAVE 30 DAY WARRANTY. WANTED: TEST EQUIPMENT-VALVES-PLUGS AND SOCKETS-SYNCROS-TRANSMITTING AND RECEIVING EQUIPMENT ETC.

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CIRCLE NO. 128 ON REPLY CARD

515

Jitter buster

Claimed to be at least as big a breakthrough as the PLL, this new anti-jitter technique does not suffer from recovery problems when its input frequency changes.

A new class of circuits, designated 'anti-jitter circuits,' or AJCs for short, has been identified by Professor Mike Underhill at Surrey University.

The most important function of an AJC is to reduce phase noise, or equivalently time jitter, in pulse streams used to carry data in communications systems. But since the concept in its current form has been shown to be capable of working from low frequencies to 5GHz, potential applications are numerous.

The AJC involves feeding a series of pulses into an integrator then passing the result through a comparator after DC level adjustment. The pulses emerge with leading edges equally spaced and phase noise is reduced by as much as 30dB.

A key benefit of the AJC is that it recovers from a frequency change much more rapidly than a PLL, **Fig. 1**.

In drawing attention to the simplicity of the basic idea, Prof Underhill comments: "The AJC is as fundamental, and is likely to be as useful, as the phase locked loop. Many of the applications for which PLL circuits are currently used might, with advantage, use a variation of the AJC instead."

Advantages of the AJC include lower phase noise and/or faster frequency switch time – the latter being key in mobile communications where the cellular principle and frequency hopping demand frequent frequency switching.

In its basic form, the AJC only de-jitters the leading edges of pulses, so the output has to be half the input frequency. But with simple enhancements, AJCs allow two pulse edges to be de-jittered, enabling output at the input frequency.

In many circuits, the AJC could simply be a 'drop-in' enhancement.

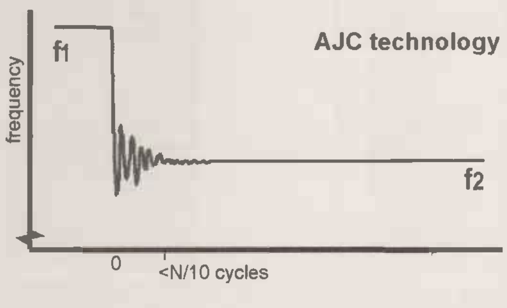
How does it work?

The concept behind the anti-jitter circuit is to feed a series of pulses into an integrator, then pass the result through a comparator, **Fig. 2**.

The pulses emerge equally spaced. This approach is applied to incoming signals that have 'jitter' or phase noise errors to achieve a large reduction in that noise – as much as is achieved by present techniques.

The approach adopted in AJC technology is very different from that of PLL technology. In PLLs a voltage-controlled local oscillator is made to track the average frequency of the incoming signal.

When the incoming clock hops to a new frequency there is inherently a time delay before a PLL circuit can stabilise to the correct tuning. AJCs adopt the new frequency



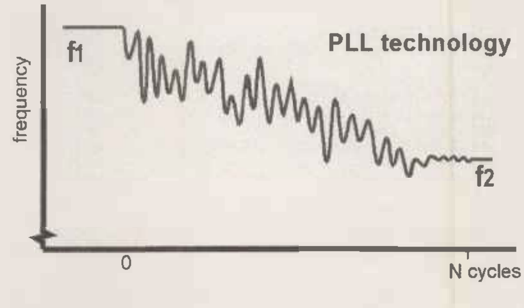


Fig. 1. Anti-jitter circuits inherently recover from an input frequency change much more rapidly than a pll.

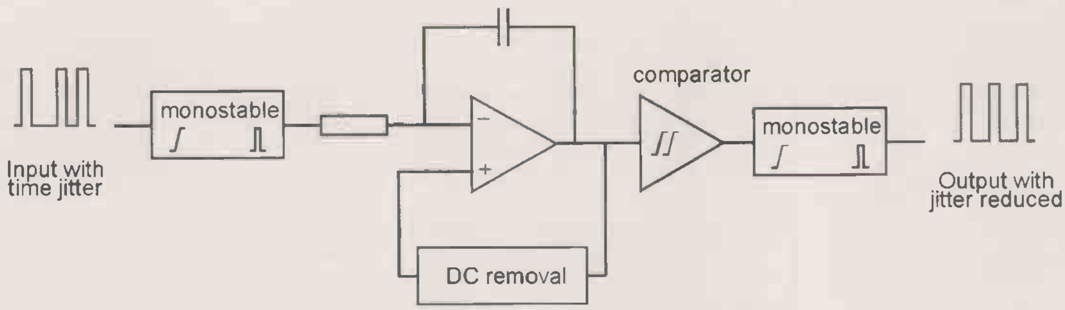


Fig. 2. Anti-jitter circuit outline. Note that there is no oscillator in this circuit. Output is derived directly from the input, having been governed to the average input frequency by the action of the integrator and comparator.

immediately. This is a significant advantage in channel-hopping systems, such as mobile telephones, where the output signals delivered by AJCs promise better reception at each frequency and much more stable reception when moving from cell to cell.

Wherever the capacity of communication systems is limited by the minimum frequency spacing at which PLL technology will reliably operate, the use of AJCs in combination with PLL circuits will multiply the utilisation of available frequencies.

The core of circuits adopting the AJC approach is shown in Fig. 2. Note that there is no oscillator in this circuit. The output signal derives directly from the input, having been governed to the average input frequency by the action of the integrator and comparator. This yields many advantages.

The core circuit just reduces phase noise. Circuits based on this core have been developed to achieve additional functions such as insertion of missing pulses, deletion of spurious pulses, fractional-N synthesis and high frequency operation.

Applications`

Anti-jitter circuit technology is expected to be of value to manufacturers of all modern communications systems and their system designers.

In mobile telephone systems, the new circuit technology will deliver high noise reduction with faster lock-on and fewer dropped connections. Its use will enhance overall system utilisation and performance. It can be applied to digital cellular systems operating to any protocol, including GSM and next-generation UMTS systems.

Anti-jitter circuit technology applies widely to many other communications systems, including high speed modems and ISDN connectors, wireless LANs, GPS, wireless local-loop telephony, satellite telephony, analogue cellular telephony, short wave radio, FMCW and hopping radar, and general electronics applications such as high performance analogue-to-digital converters and frequency synthesisers.

Circuits based on the technology are straightforward to use and can be deployed in discrete components, or in standardised ASIC cells, without any adjustment to the wider circuit environment. They will operate from less than 1kHz to above 5GHz and are fully cascadable to achieve noise suppression in excess of 20dB per stage.

Anti-jitter circuit modules can be used wherever phase noise is a problem. They can be used in place of phase-lock loop circuits, or as an enhancement to allow them to operate at much narrower frequency spacing, for example. They will also replace or enhance direct digital synthesis designs.

AJC is the subject of a family of six separate patent applications that are now available for licensing for first manufacture.

Key features

Frequency limit. AJC technology has been laboratory tested in discrete component circuits operating at low frequencies – up to 10MHz – and modelled in high frequency circuits – up to 5GHz – using component specifications that match current silicon chip fabrication standards. Maximum operational frequency has been shown to be limited only by component performance.

Frequency range. Simple AJCs operate down to approximately 30% of their maximum operational frequency. Modifications that provide either 'adaptive' or 'self-programming' modes allows this range to be extended to just 1% of the maximum where required.

Noise removal. AJCs have already achieved better than 20dB reduction in phase noise, and greater reductions can be achieved by cascading. Remaining time jitter can be reduced to subpicosecond levels. Unlike some other techniques, AJC technology achieves the reduction of total

Who needs anti-jitter?

Maintenance of accurate clock pulses is a widespread requirement in electronics. Errors in the arrival time of pulses constitute 'phase noise' or 'time jitter'.

Phase noise is a particular problem in communication systems, where large phase deviations can arise from such effects as mutual interference between transmitters, fluctuations in propagation, changes in polarisation due to Faraday rotation, weather conditions, movement of antennas or reflectors, and movement of objects in the signal path. This noise degrades the signal considerably and can cause its complete loss when the receiver can no longer track the pulse train on which the signal is encoded.

Even in compact systems, phase noise can place a limit on speed or performance. Thermal noise and 'flicker' generated by semiconductor components can produce phase noise in both analog and digital circuits. Digital circuits suffer phase noise where circuit loading and fan-out vary, and asynchronous digital circuits are prone to phase noise from unwanted cross-coupling.

To alleviate these problems a number of approaches are presently available. Careful tailoring of key circuits can minimise the generation of phase noise at source. Complex phase-lock loop and direct digital synthesis circuits allow sophisticated RF receiver strategies, but suffer from phase noise problems.

Some circuits spread or dither the noise to other frequencies. Each has disadvantages in performance, spurious effects on – or loss of – the signal, design time and manufacturing cost.

AJC technology provides a fresh approach which promises to match or outperform other methods in most respects, and is considerably easier to deploy.

Need more information?

For more information, contact Dr Neil Downie, Maran & Co Ltd via fax on +44 (0)1483 302112 or via e-mail using n.downie@maran.co.uk. Below are four references giving more information on this topic.

'The anti-jitter circuit for low spurious DDS square waves and low cost fractional-N synthesis,' MJ Underhill, S Stavrou, M Blewett, N Downie. European Frequency Time Forum, Warsaw, 1998

'Performance assessment of a delay compensation phase noise and time jitter reduction method,' MJ Underhill, M Blewett. European Frequency Time Forum, Neuchatel, 1997.

'Spectral improvement of direct digital frequency synthesisers and other frequency sources,' MJ Underhill, M Blewett. European Frequency Time Forum, Brighton, 1996.

'The Anti-Jitter Circuit for suppression of wide band phase noise,' MJ Underhill, Microwaves and Millimetre-wave Oscillators and Mixers, IEE, London December 1998 (to be published).

noise, rather than spreading the noise to other frequencies. It offers good wideband noise reduction – a unique feature – without increase in close-to-carrier noise. Good suppression of highest sideband frequencies is also achieved.

Tuning and locking. AJC technology is inherently self-tuning to lock on the average frequency of the pulse train. It tracks abrupt changes in frequency instantly, if they are small, or within typically 5 cycles if the changes are large. Very importantly, the output signal remains useful throughout – a major advance over other technologies and a valuable contribution to better performance in cellular communication systems. Noise is reduced by typically 10-15dB while the change is tracked, full noise reduction is then progressively reasserted. Under typical conditions full noise reduction is restored within a few microseconds of the change in frequency.

Frequency spacing. AJCs should allow better use of the radio spectrum. By use of AJC technology, for example for fractional-*n* synthesis, operational frequencies are not limited in precision by the step size of a PLL analogue synthesiser, for example.

Circuit environment. The AJC normally needs an input to be in the form of pulses of equal length, which is the case in many applications. Simple variants can be adopted to deal with unequal pulse lengths. Its function is independent of its circuit environment, and so can be incorporated in almost any circuit as a 'drop-in' component or ASIC cell. Multiple AJCs can be cascaded for demanding applications.

Robustness. The tested designs are well-behaved, do not lock to the wrong frequency or stop completely, always provide phase continuity, and do not generate glitch pulses.

Wide performance envelope. In its high frequency form AJCs have been modelled at 5GHz and beyond with an operational frequency range of up to 1000:1. Frequency jumps of up to 50% are tracked, as are phase jumps of up to ±150°.

Manufacturability. AJC circuits are MSI type circuits: relatively low in complexity and manufactured at low cost. Due to its wide performance envelope, only a small number of AJC design variants is needed to serve almost every application.

Extra capabilities. As well as noise reduction, AJC circuits have been designed which insert missing pulses and delete spurious pulses. AJC variants have been developed for tasks such as multiphase clock distribution and fractional-*n* synthesis.

The underlying technology is also capable of development to deliver other related functionalities: for example, clean-up of DDS spurious frequency outputs.

AJCs can be used to enhance existing PLL and DDS technology and they are compatible with existing PLL and DDS technologies. This opens up the possibility for adding AJCs to conventional PLL circuits to make them effective at much narrower frequency spacings – an important benefit in communications.

Added to DDS circuits, AJC technology produces cleaner output signals with improved spurious sidebands. ■

New work
Mike Underhill is currently working on a new implementation of the AJC in which the comparator is replaced by a simple logic gate and the integrator is replaced with a passive charge accumulator. This will make the circuit much easier to use and manufacture.

Comparison between the AJC and PLL.

	Anti-Jitter Circuit	Phase Lock Loop
Maximum frequency	5GHz (high speed version)	5GHz (specialised designs)
Frequency range	down to 30% of maximum (standard) down to 1% of maximum (adaptive)	Down to 50% of maximum
Noise (far out)	–160dBc possible (improved 20db/stage)	–160dBc
Noise (close in)	–80dBc	–80dBc
Spurious noise	None so far detected	Generally minimal (some microphonic)
Switching delay	5 cycles typical	>20 x $f_o/\Delta f$ (e.g. 200 cycles for typ. 100MHz operation)
Output while switching	Usable output – half normal noise reduction	Unusable output, spurious signals
Self-locking	Yes	Yes, but only over narrow range
Circuit environment	Drops-in to 'any' circuit	May require tailoring to circuit environment
Cascadable	Yes, simple	No
Cost/complexity	single MSI chip	MSI chip + typically 10 external components

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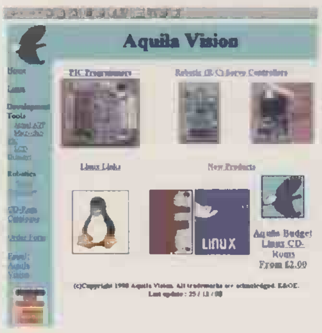

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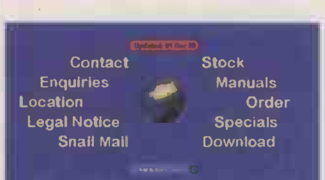

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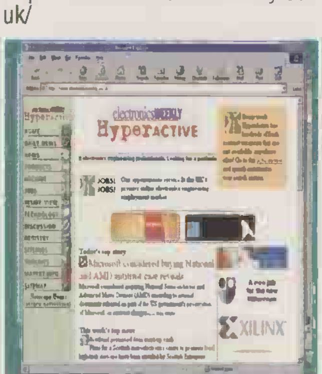

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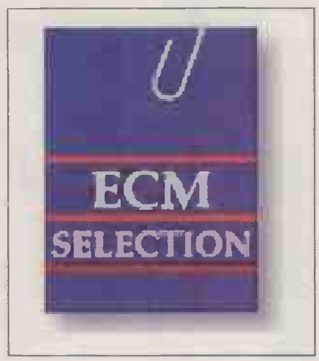

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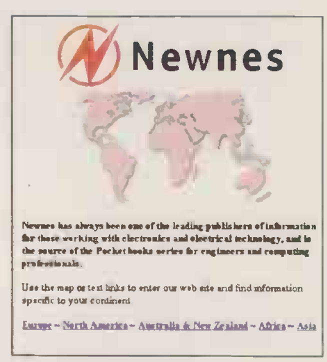

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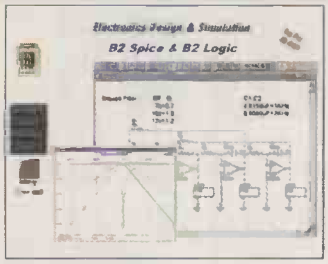

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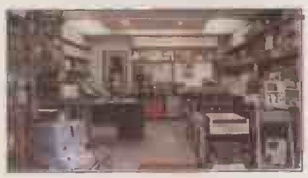

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LETTERS

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Horse play?

The letter from Mr Cahner in the April 1999 issue of *Electronics World* – if it was not an April Fool – is easily answered because third-order Butterworth designs were indeed very common in the early seventies, in both passive and active form.

The problem, however, is not how to realise particular filter shapes with passive or active filters, but, how the sounds from the two drive units add up in a 3D acoustic environment.

In general, the output from a drive unit mounted in a box is not flat, so there will always be a requirement for some equalisation as well as the 'crossover' function of the filters.

The outputs of high and low pass third-order Butterworth filter sections are in quadrature – i.e. 90° phase difference. As the listener moves off axis, in one direction the summed output at crossover will rise and in the opposite direction there will be a dip. This led to some designs with the tweeter below the woofer in order to point the best listening axis upwards on floor standing models.

The desire to eliminate this effect fuelled a move towards 'in phase' squared Butterworth, or Linkwitz-Riley, crossover design in the late seventies. Later efforts went into getting the HF and LF voice coils co-incident rather than just in the same plane.

E. Cecconi
Principal Electroacoustics Engineer
KEF Audio (UK) Ltd.

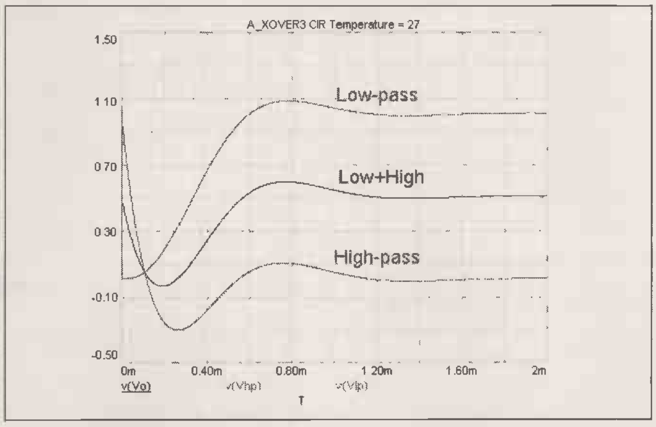
The transient response plot of Jim Cahner's crossover network shown here explains why the circuit is not 'perfect' – whatever that means.

To find out why the crossover circuit is not perfect, one should run the transient response simulation to see that the sum of the low and high-pass section is far from the step response at the input – apart from being 6dB down.

In fact it is more like a notch-filter response, although no notch is seen in the frequency response magnitude.

The phase diagram shows part of the story, but the envelope delay would show even more.

An ideal transient would have a flat envelope delay, meaning that the phase is a linear function of frequency – the envelope delay is a phase-derivative *versus* frequency.



Doing the maths, you can see that the sum of the two filters,

$$H(s) = 0.5 \times \frac{s^3 + w^3}{s^3 + As^2 + Bs + w^3}$$

and for H(s)=0.5, the first and the second power-of-s terms are missing from the numerator.

Instead of using Butterworth tuning, you could try Bessel, or linear-phase, tuning and shift one of the filters in frequency to minimise the magnitude wiggling around the crossover point.

The result would be much better, but still not perfect

Erik Margan
Ljubljana
Slovenija

Newer logic

Some readers will have read my article 'New Logic' in the February 1999 issue of *Electronics World*. The article was on the subject of Boolean algebra.

If you have discovered the significance of this article you might like to read the second part of it. This part concludes my demonstration that Boolean algebra based on the exclusive-OR in place of the more familiar inclusive-OR is actually quite a useful and practical addition to the stock in trade of the digital circuits design engineer.

I have gone to some trouble to make the articles readable. I have now revised my web site at: http://users.senet.com.au/~dwsmith/ to include an html version of the second part of the 'New Logic' article.

Readers might like to take a look at this site. I would appreciate any feedback via my e-mail link which will be found on some of the pages, from serious readers, particularly if they have read the New Logic article.

You might find that html, in one of the up to date internet browsers, is a very practical way of reading an article. Html documents can have hyperlinks that make navigation easy.

The whole article can appear on one scrollable page with diagrams seamlessly incorporated.

David Warren-Smith
Elizabeth
South Australia

Phase sensitive

I was interested to read the article entitled 'The phase-sensitive detector' in the April issue of electronics World. However I note that the reference information has accidentally been omitted.

The omitted reference is 'Lock-in Amplifiers: Principles and Applications' by M L Meade, 232 pp, published by Peter Peregrinus, 1983.

The book is out of print but copies are held in many technical libraries. I'm sure there are some readers who would appreciate this information.

Fraser Robertson
Open University

Flash in the pan

Regarding the circuit idea '4-bit flash makes 16 bit flash a-to-d' in the May issue, for this approach to work you have to make the assumption that the 4-bit a-to-d converter has perfect 16-bit linearity – which it will not.

Any linearity errors will show up as errors on the d-to-a converters, which must also be linear to 16 bits.

Also, the resistors used would have to be accurate to 0.001% to retain 16-bit accuracy.

If you are lucky you may get 5 bits of performance out of this design. If it was this easy then both IC manufacturers and companies like ours would have done this long ago

I seem to remember a similar design was published a few years ago that made the same mistake – the author references Dec 91, but I think there was a more recent article than that.

Alan Tong
Pico Technology
Cambridge

Heater debate

John Norman – Letters p. 286 April issue – was a little naive in relying only upon steady-state conditions in recommending the use of a 2μF capacitor to feed 0.15A valve heaters from the 230V 50Hz main supply.

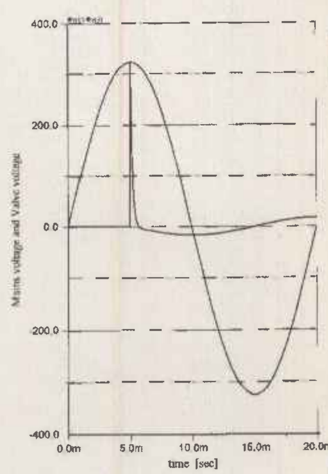
In the worst case, when switching on when at a peak instant of the supply voltage, approximately 325V will suddenly be applied to the heater chain.

If feeding only one 12V 0.15A filament, this would cause a peak current of over 3.8A – though admittedly, the pulse has a time constant of only about 170μs

Why not use an inductor, instead of a capacitor, I hear some of you ask? Another problem arises here, but now the worst case is switching on as the mains voltage goes through zero.

These were 'heated' topics of discussion when I was a lad.

Bob Pearson
Bourne Lincs



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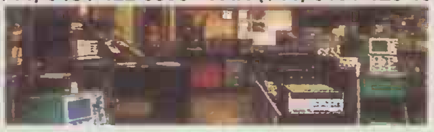

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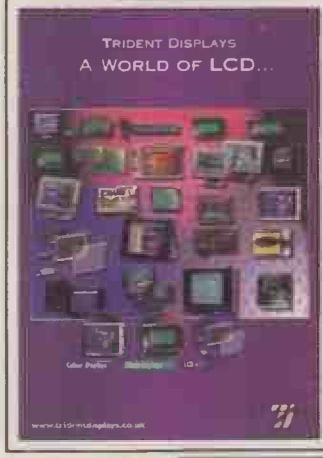

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