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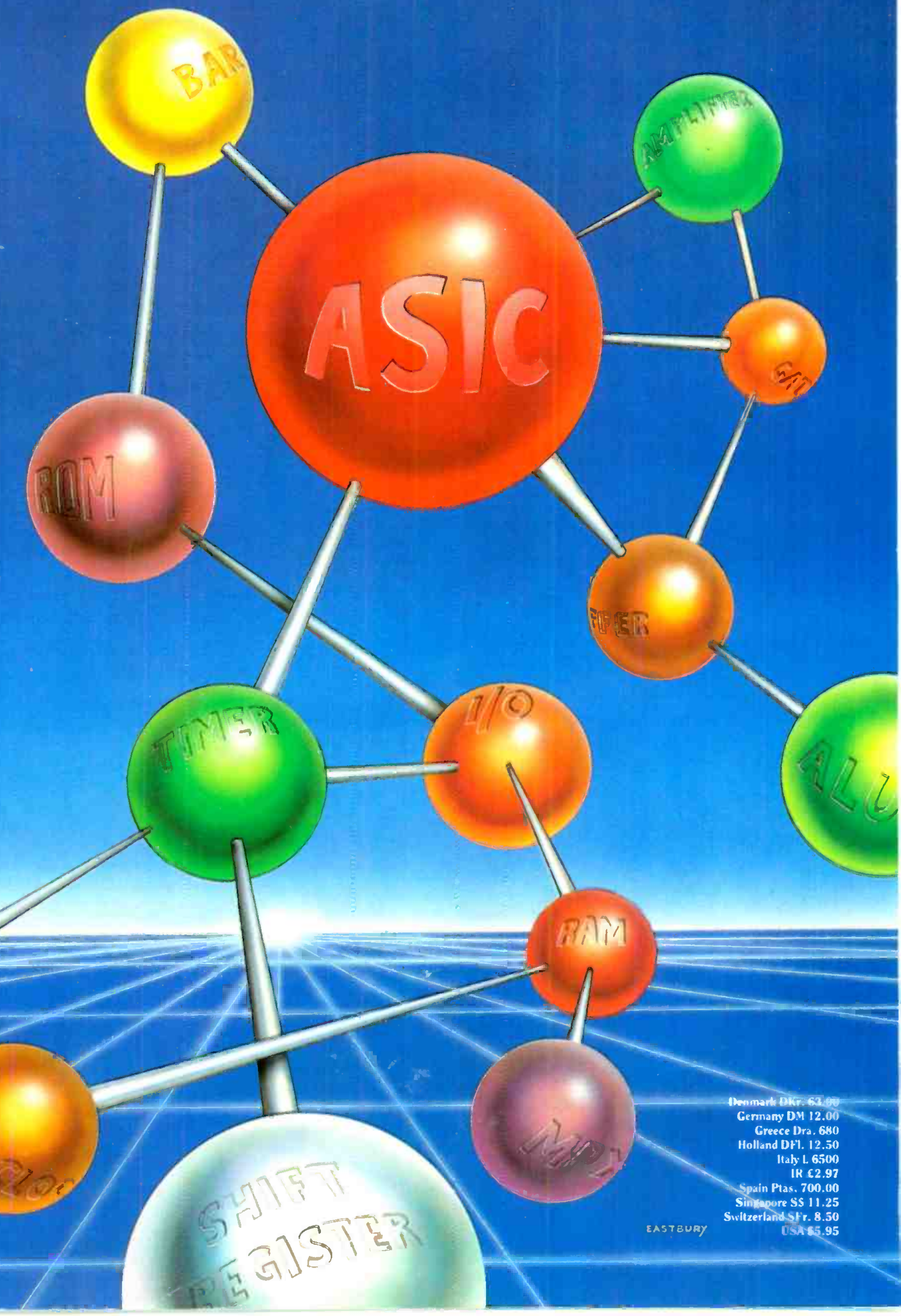

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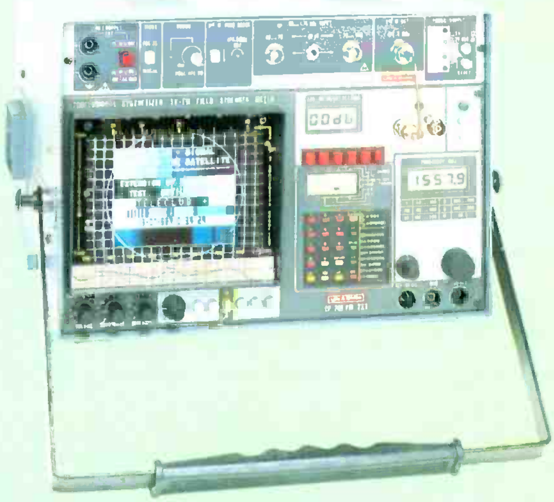

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MAY 1989 VOLUME 96 NUMBER 1639

June issue on sale 18th May

Designing low noise audio front ends. The first stage of an audio amplification system must always be a compromise between noise performance and headroom made more difficult by the low voltage, low impedance characteristics of modern transducers. We examine the matching of semiconductor device parameters to this demanding application.

The PC graphics maze. Recent market research indicates that IBM architecture accounts for some 90 per cent of professional personal computer usage. Despite being commonplace the mechanisms for the various types of screen display are not always well understood. We offer a technical programmers' guide for all the major display modes. A task fit for Hercules.

Alpha torque forces. There are still mysteries contained in the outwardly simple passage of an electric current. Why should a copper conductor shatter rather vaporize when subjected to a massive pulse current? The mostly undocumented magnetic force responsible for the phenomenon has applications in propulsion, drilling and in the manufacture of magnetic guns claims author Dr Peter Graneau.

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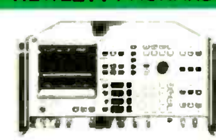

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Looking through the technology window

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REED BUSINESS PUBLISHING

The integration of a million transistors into a single chip microprocessor represents a technological milestone by any definition of the cliche. Yet it was just nine years ago that a semiconductor designer named Gordon Moore got up before an IEEE solid state circuits conference in San Francisco and stated quite categorically that he couldn't begin to imagine a use for a million transistors on a chip except in the building of a memory device.

This designer had wider responsibilities. He was at the time chairman of Intel and still is to this day. And the company with a million transistor micro? Intel, naturally.

The same company invented the single chip microprocessor concept back in 1971, a brilliant piece of general purpose eccentricity connected with the development of a digital alarm clock. Those involved instantly appreciated that the four bit device with its ALU, control logic, and the most minimal of register sets could do a lot more than make clocks tick. The 4004 microprocessor, with a few bits of program memory, was a indeed a microcosm of period mainframe computers. It was only later that the pretentious started to add expressions such as "Harvard architecture" and "classic von Neumann processors" to this wonderful new way of thinking.

Intel rapidly followed up with microprocessors of greater complexity: the 4040 and the 8-bit 8080 series. It does the original microprocessor design teams much credit when one considers that most, if not all of the original 8-bit designs are still in production somewhere in the world.

Other manufacturers responded rapidly with effective, if not better micro families: Z80 from Zilog, 6800 series from Motorola and the 6500 from Rockwell were all very successful. Enterprising companies took to the micro concept creating a personal computer market along the way. One should note that the traditional computer industry regarded microprocessors with interest and personal computers with absolute scorn.

IBM was no exception. Apple, the most successful of the personal computer entrepreneurs, was in business at least four years before Big Blue gave birth to its first. The progeny was powered by an 8-bit 8088 Intel processor of none too spectacular performance.

The IBM badge gave respectability to the PC business and an enduring meal ticket to Intel. It is interesting to speculate on what the semiconductor industry would now look like if IBM had used either the Zilog 16-bit Z8000 or the Motorola 16-bit 68000 as it very nearly did. The PC business would certainly have taken a different shape. Software would generally have been written in 16-bit code and double byte data would have been the rule rather than the exception. Programs would have beer faster and more powerful while the PC world would have have moved considerably beyond horrible MicroSoft operating systems and the equally limiting IBM graphics standards.

The real world is an interesting place. The indifferent IBM PC architecture currently accounts for around 90 per cent of business personal computer sales, the indisputably better Apple Mac based on the 6800 micro has eight percent while the remaining two percent are unlikely to become three percent.

IBM has already declared its interest in Intel's million transistor beast, a processor aimed at Unix-alike operating systems. Even taking into account the amazing bells and whistles which the processor incorporates and the astonishing performance in comparison to existing Intel products, the device represents an architecture as old as the computer industry itself. A wonderful piece of technology, most certainly, but the IBM connection could well impose a straitjacket on the new generation of personal super computers. The computer industry could benefit by experimenting with distributed architectures such as super parallel processor, distributed memory, neural networks or whatever.

It seems short-sighted to endorse an essentially elderly architecture without considering the options in full.

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Motion through the ether

Using a novel interferometer, the author claims to have demonstrated the existence of the ether and to have disproved the principle of Relativity.

E.W. SILVERTOOTH

This article presents an account of a new electronic device that has proved conclusively that our motion at speeds of some 400 km/s or so in space can be measured in the confines of a laboratory. The experiment proves that there is an ether and disproves the principle of Relativity.

It does so because it measures the speed at which the laboratory is moving in a fixed direction in space, and that means that something is flowing through the laboratory at that speed. That something is the ether.

The famous Michelson-Morley experiment failed to detect our translational motion through the ether. It did not establish that the speed of light was referred to the observer moving with the apparatus. What it did was to prove that the average velocity of light for a round trip between a beam splitter and a mirror was independent of motion through space. The author supposed that the one-way speed of light, or more specifically its wavelength, did depend upon that motion, but in a way that satisfied the exact null condition of the Michelson-Morley result.

However, the Sagnac experiment, as embodied in the ring laser gyros now used in navigational applications, showed that if a light ray travels one way around a circuit, and its travel time is compared with that of a light ray going the other way around the circuit, the rotation of the apparatus is detectable by optical interferometry. Here the result is just as if there is an ether and the speed of light is referred to that ether.

Readers will have great difficulty finding a book on Relativity that even discusses the Sagnac experiment or the later experiment by Michelson and Gale that detected the Earth's rotation.

In the modern version of the Sagnac experiment a single laser divides its light rays and sends them around a loop in opposite directions, but the resulting standing waves are not locked to the mirror surfaces as they are in the Michelson-Morley experiment.

It was my assumption that the different wavelengths presented by rays moving in opposite directions along that path would allow a detector to sense a modulation or displacement of the standing wave system along the common ray path. The secret was to move the detector or the optical system along a linear path, rather than rotate the optical apparatus, as in the Sagnac experi-

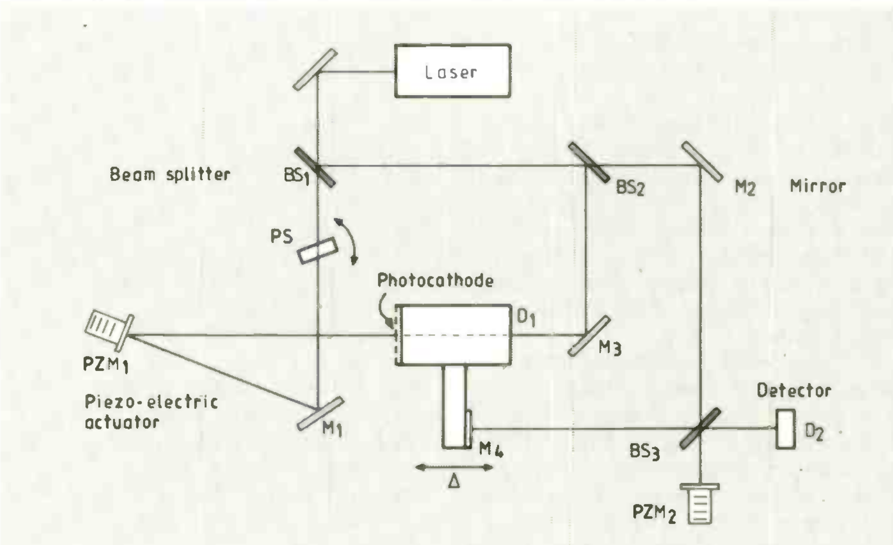


Fig.1. Beam from a HeNe laser is divided into two portions which then pass through D_1 in opposite directions. By this means a standing wave is set up in the region of D_1. Piezo actuators PZM_1 and PZM_2 are fed from a common AC source at a frequency of a few hundred hertz. A part of the beam impinging upon the beam splitter BS_2 passes through and feeds the conventional Michelson interferometer PZM_2, BS_3 M_4, and detector D_2. In operation D_1 and M_4, on a common mount, are moved to get a maximum signal from D_2. Then phase-shifter PS is rotated to get a maximum signal from D_1, and in the same phase as D_2. The assembly D_1M_4 is then moved a distance Δ such that the signals from D_1 and D_2 are again at a maximum, but now 180° out of phase with respect to each other. Note that the round trip path BS_3M_4 is independent of v, the velocity of our motion through space.

THE ETHER CHALLENGE

The progress and welfare of our modern society depends upon scientific advancement on a global scale. In this sense 'global' has not only a geographical meaning. There is a need for global thinking over the whole scientific spectrum. The developing world that was once colonized has become independent, but a new kind of empire domination has crept into our society. It pervades the world of science, a world that has become progressively larger but less responsive to change. It is that world which influences the governmental funding and academic research that is expected to create new technology.

There are techniques of savage conquest in this academic life amongst the ivory towers. These are very effective in discouraging independent scientific initiative, particularly in the countries that command high research funding.

"Suppress, ignore and ridicule" are the weapons that are used to block the insurgent scientist seeking a hearing for his own theories and even his experimental discoveries. The only existence allowed in scientific society is one which is subservient to accepted doctrines.

The imperialists dominating the field that matters to those interested in electronic communication serve under the flag of Einstein. For many, this service is mere lip service because Relativity does not affect what they are doing on a daily basis. Nevertheless, the hordes involved in the Einstein army follow that flag blindly, even though their quest has no apparent destiny. Whatever they accomplish is viewed in exactly the same way by all those observing their efforts. That is in accord with the principle of Relativity; all physical laws are seen to be the same in any frame of reference. There is no room for dissent or anomalous observation. Powerful missiles are hurled into space under the control of navigators that use charts drawn up in four-dimensional space-time. They serve for satellite communication and position location. Errors do occur that would not occur in three-dimensional space independent of time, but a blind eye allows these to pass without notice, because those who control these activities cannot challenge that Einstein 'flag'.

Ten years ago Dr Louis Essen, famous for his pioneer research on the caesium clock and the measurement of time and the speed of light, wrote an article in *Wireless World* that spoke of the suppression of the truths concerning Einstein's theory[7]. He was not following any other flag than the flag of truth. Scientists should know only that flag and conduct their research with an open mind. If serious argument of a dissident nature stands in the way, that is a basis for parley rather than a vanquishing attack.

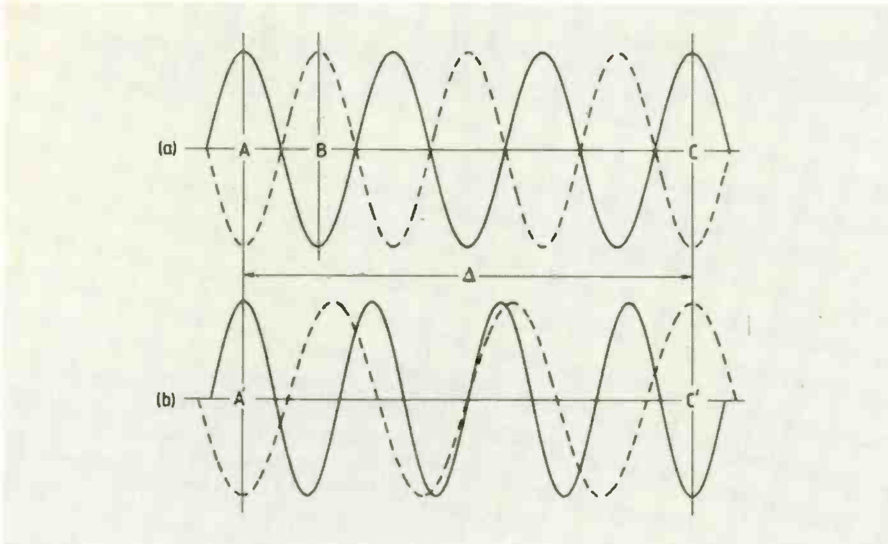


Fig.2. In (a) $\lambda_1 = \lambda_2$. In (b) $\lambda_1 \neq \lambda_2$. When the dotted curve is jittered in phase with respect to the solid curve, it is seen that there is a phase reversal between (a) and (b) in the vicinity of C and C′. (The intensities add.)

ment. A little analysis showed that such effects would exhibit a linear first-order dependence on v/c and that the detector would need to scan through a distance that was inversely proportional to v/c in order to cycle through a sequence of that standing wave pattern.

This was exactly what I found when the experiment was performed.

THE STANDING-WAVE SENSOR

The one-beam interferometer or standing wave sensor consists of a photomultiplier tube comprising two optically flat windows, with a semitransparent photocathode of 50nm thickness deposited on the inner surface of one window. The tube also contains a six-stage annular dynode assembly such that a collimated laser beam can pass through the tube.

In the application described in reference 1 the beam was reflected back on itself by a mirror to set up standing waves. The performance of the wave sensor was tested by incorporating a tiltable phase-shifter between the sensor and the mirror. This provided an adjustable displacement of the standing wave relative to the sensor.

The object of the test was to measure the effective thickness of the photosensitive surface, to estimate the precision available from the sensor for making measurements on standing waves.

Signal-to-noise ratio for the photocathode when positioned at an antinode compared with that at a node was measured as approximately 20 000 to 1. This was shown to correspond to detection of photoelectrons in the 50nm thickness of the photocathode, which assured us that position measurement within a standing wave could be made to within 1% of the laser wavelength.

Three such wave sensors were fabricated at Syracuse, New York, by the General Electric Company of the USA from standard parts of image orthicons. For this experiment, the sensor was connected as shown in the arrangement of **Fig. 1**.

If we write the wavelength of light moving one way as λ_1 and the wavelength of light moving the opposite way as λ_2, then

$$(\lambda_1 - \lambda_2)/\lambda \simeq \lambda/\Delta$$

where λ is the nominal wavelength of the laser output and Δ is the displacement distance that was measured as corresponding to a phase reversal in the standing wave oscillations. In a typical measurement Δ as defined in the equation above was 0.025cm at its minimum; and since the nominal laser wavelength λ was 0.63μm, and the wavelengths depending upon the spatial orientation were $\lambda_1 = \lambda(1+v/c)$ and $\lambda_2 = \lambda(1-v/c)$, it is clear that the maximum value of v is given by $2v/c = (0.000063)/(0.025) = 0.00252$.

Since c is 300 000km/s this gives v as 378km/s on the day when this particular test was performed. The axis of the photodetector making the linear scan through the standing wave was directed towards the constellation Leo when this maximum value of v was registered. Six hours before and after this event the displacement of the detector revealed no phase changes, meaning that the photodetector was then being displaced perpendicular to its motion relative to the ether.

The experiment has been repeated in a variety of configurations over the past several years. Values of Δ measured have all ranged within ±5% of the cited value. The micrometer is graduated in increments of 0.0025 millimetres. However, a micrometer drive is too coarse to set the interferometer on a fringe peak. This is accomplished by means of a third piezo actuator supplied from a DC source through a ten-turn potentiometer which provides conveniently the finesse for setting on a fringe peak.

Since the author first disclosed this discovery[2,3] there has been a great deal of effort by a number of individuals in different countries, including USA, West Germany, UK, Italy, France and Austria, all aimed at theorizing as to why the experiment works or why it should not work[4].

The Sagnac Effect

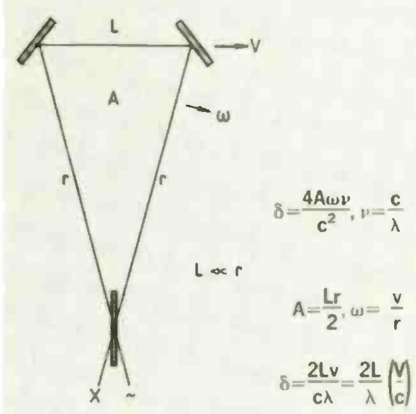
A monochromatic light beam impinges upon a beam splitter. The transmitted beam proceeds anticlockwise round the closed path and returns to the vicinity of the source. The reflected beam proceeds clockwise and rejoins the first beam to establish a fringe pattern. If the assembly rotates at an angular velocity ω the fringe pattern shifts an amount δ as shown in the equation. A is the area enclosed by the paths, v is the tangential velocity along the line element L, and ν is the frequency of the source. The fringe shift is independent of the shape of the area or of the centre of rotation. It is further seen that δ, the difference in the number of wavelengths in the two paths is independent of r, and hence the equation holds when L is in pure translation. δ may be written as

$$\delta = \frac{L}{\lambda_1} - \frac{L}{\lambda_1} = \frac{2L}{\lambda}\left(\frac{v}{c}\right)$$

When this is solved simultaneously with the equation for one leg of the Michelson-Morley experiment

$$\frac{L}{\lambda_1} - \frac{L}{\lambda_2} = \frac{2L}{\lambda}$$

we have the values for λ_1 and λ_2 as given in the text; λ_1 and λ_2 are, of course, the wavelengths in the reciprocal directions along the path L. The Sagnac effect is well known and proven: nearly all long haul airliners and modern submarines navigate with laser gyros based on G. Sagnac's discovery (1913).



The author, however, declines in this article to go into the mathematical argument that underlies the theory involved, simply because that itself becomes a topic of debate and it tends to detract from the basic experimental fact that appears in the measurement.

Further reading

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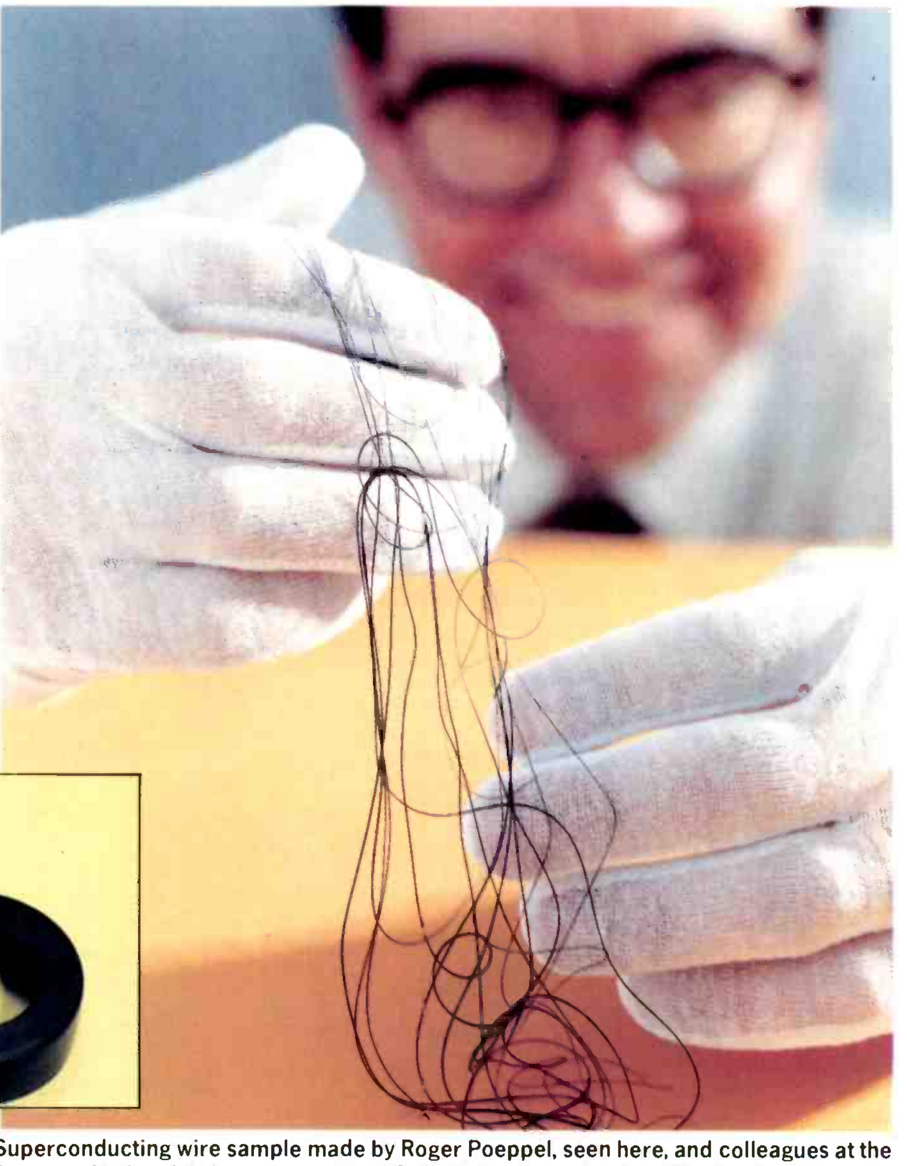
7. L. Essen. *Wireless World*, October 1978, p.44.

RESEARCH NOTES

All quiet on the superconductor front?

With all the media hype (not of course from Quadrant House) it's scarcely surprising that most of us are thoroughly muddle-headed on what's happening in the rather esoteric world of high temperature superconductivity. Gone it seems are the almost daily claims to have found that holy grail, the room-temperature superconductor. But silence also seems to reign when it comes to everyday practical applications of the ceramic superconductors we've had around now for almost two years. Nowhere do we see the lossless motors, generators and transmission lines that everyone was suggesting were just around the corner. Indeed, looking at the world of practical superconductivity, the main workhorse materials are still the low-temperature metallic superconductors such as niobium-tin that have been around for decades.

Taking an objective look at the overall scene, it's perhaps not surprising that things have gone rather quiet. Two years after the splitting of the atom or the invention of the laser, things were similarly quiet, as if the froth needed to settle before it was possible to assess the value of the pint!



Superconducting wire sample made by Roger Poeppel, seen here, and colleagues at the Argonne National Laboratory in the US. Left: Superconducting $YBa_2Cu_3O_{7-\delta}$ ceramic samples suitable for microwave resonators (Plessey Research Caswell Ltd).

In the case of high temperature superconductivity the dissipating froth has now revealed a number of steadily maturing areas of research such as the discovery of new classes of materials, the formulation of a theoretical framework and progress in realistic practical applications.

On the applications front, three main problems have beset the present generation of high temperature superconductors. Being ceramic materials, they can't easily be formed into flexible conductors of the sort that might replace copper wire. Tapes and wires produced by researchers in institutes like the Argonne National Laboratory in the USA are very brittle and only mildly flexible.

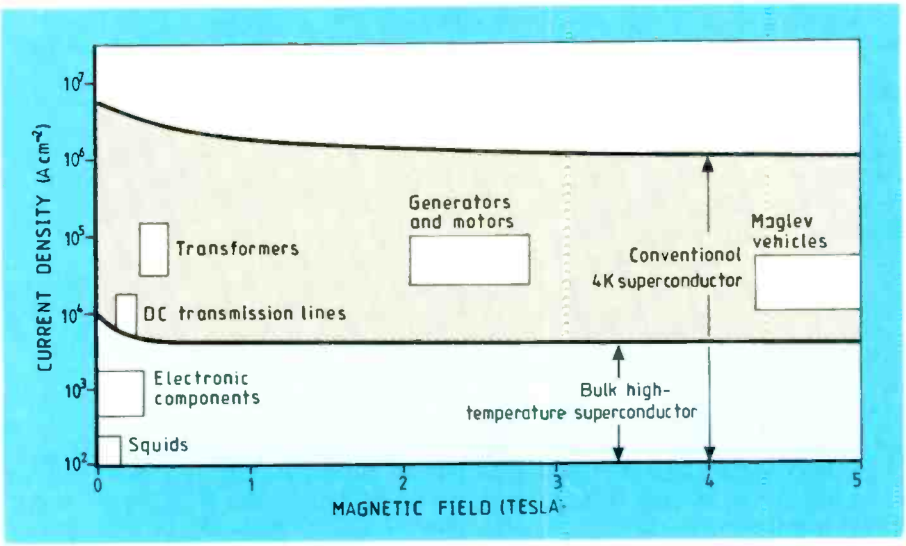
The other major problems are that the new generation of materials lose their properties in the presence of large currents or large magnetic fields, thus minimizing their usefulness for the very sorts of applications that had all the visionaries excited. Thus existing materials are limited either to around $5kAcm^{-2}$ or 1 tesla or both, putting them beyond the reach of currently-envisaged uses such as motors and transmission lines. So why all the excitement if conventional materials such as niobium-tin can carry $1MAcm^{-2}$ and co-exist with fields of more than 5T? The answer is simply a matter of temperature: cooling a material to 4K is roughly 2000 times more expensive than cooling it to 77K.

Of the few practical applications that are emerging for today's high temperature superconductors, Squids are, if anything, more fascinating than lossless motors or maglev trains. Superconducting quantum interference devices, to give them their full title, consist of Josephson junctions inserted into loops of superconducting wire. They are by far the most sensitive devices yet devised for measuring magnetic fields and electric currents. A typical Squid can measure 10^{-18} amperes (a few electrons per second!) or a magnetic field 10 times smaller than the Earth's field. And far from being useless laboratory curiosities, they're now being used for everything from mineral prospecting to medical diagnosis in which they can detect the faint magnetic signals associated with the electrical activity of the human heart and brain.

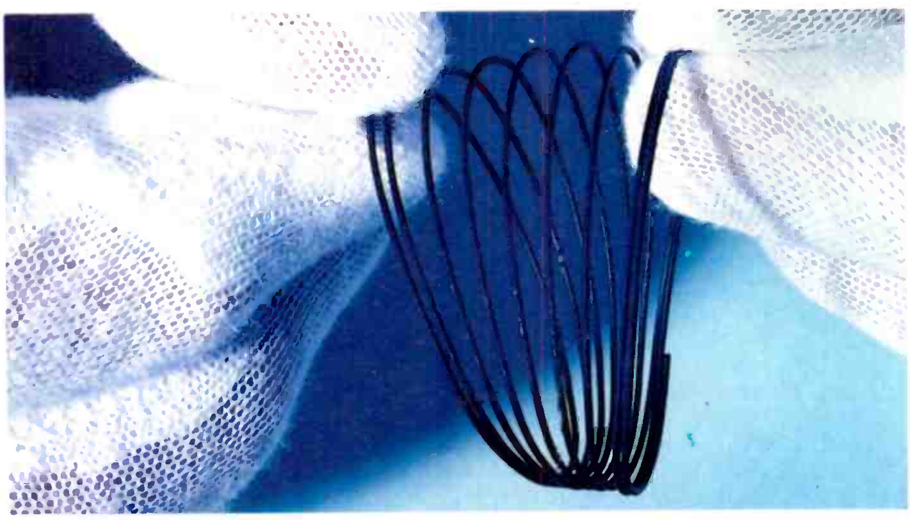
Other practical applications of high temperature superconductors that are beginning to emerge are high-Q microwave resonator cavities, miniature antennas (see Research Notes last month), radiation detectors and chip interconnects.

On the materials front research has also

RESEARCH NOTES



Despite the high level of research activity in high-temperature superconductors, applications in motors and transmission lines remain tantalisingly beyond their reach.



Sintered superconducting coil made at the Argonne National Laboratory.

settled down to a less frenetic but nonetheless exciting pace. Most of the work still concentrates on the so-called rare earth cuprates – materials in which one or more rare earth elements such as yttrium or cerium is combined with copper, oxygen and assorted other elements such as thallium and barium. The material exhibiting the highest transition temperature so far (T_c = 125K) has the approximate chemical composition $Tl_2 Ca_2 Ba_2 Cu_3 O_x$.

Of more importance to basic research, however, have been two recent announcements, one of a high temperature material that appears to superconduct using electrons – rather than holes – and one that substitutes nickel for copper. The first of these (*Nature* Vol. 337 No 6205) describes Japanese work using a material of the composition $Ln_{2-x}Ce_xCuO_{4-y}$ where Ln is one of the lanthanides (rare earths). Like earlier materials it can be thought of as an insulator to which a dopant is added to supply or remove electrons. It isn't a record-breaker in terms of superconductive transition temperature, but it does create a new basis for the construction of fundamental theories.

The second piece of progress, the use of nickel instead of copper, is reported (*Science* 10 February, 1989) by a Polish team working at Purdue University in the USA. This ceramic, of composition $La_{2-x}Sr_xNiO_4$, is the first copper-less superconductor to be discovered with a transition temperature above 40K. Again, by extending the range of elements, this work should help to narrow down the numerous competing theories of high temperature superconductivity and give theorists one more ingredient to work with. 'Ingredient', incidentally, isn't just a casual use of language; when asked about formulation of some of the new materials, one researcher observed, "The properties of puff-pastry are determined not only by the ratio of flour to butter but by the proper formulation of the layers" – a reference to the extreme difficulty of producing consistent results.

Why is the ocean floor visible from space?

Having visited numerous Soviet research institutes I'm in no doubt as to the high quality of much of the work currently being undertaken in the USSR. Yet, in spite of that, I'm still often left wondering how clearly the Russian publicity machine can distinguish fact from fantasy.

We're still waiting for example to see concrete evidence of a laser-amplified television tube (see *E&WW* June 1988 page 622). Ditto element 110, etc. etc. So with a mild degree of scepticism I present the latest Soviet answer to a frequently-observed cosmonautical phenomenon: the fact that the ocean floor can sometimes be seen from space when the depth of water would normally absorb all light.

A team of Moscow physicists, Valerian Tatarski, Yuri Kravtsov, and Alexander Vinogradov is reported by the Novosti Press Agency to have developed a theory that confounds the normally-observed phenomenon that as waves propagate they are also scattered. Thus we're all taught that sound, light, radio and other waves bounce off the inhomogeneities that exist in all media. Obstacles are present everywhere, because the ideal medium does not exist. In the atmosphere, for example, turbulence causes poor seeing for astronomers.

Now the Russians claims that quite the opposite may occur under certain conditions. The average intensity of the wave reflected back and running into inhomogeneities again can – they say – be several times that of waves propagating in a homogenous medium. To put it differently, inhomogeneities may sometimes intensify the signal, instead of weakening it.

Other Soviet researchers, Alexander Gurvich and Sergei Kashkarov, now claim to have proved this theory experimentally and their effort has, moreover, been rewarded by inclusion in the USSR State Register of Discoveries. Gurvich and Kashkarov explain that "occasional inhomogeneities, inevitably occurring in any medium, chaotically alter the wave speed and the wave, going forward and back, passes through the same inhomogeneities, which act as lenses, now dissipating, now focussing it." They claim to have proved the universality of such behaviour – which goes, they say, for all waves no matter what their physical nature – electomagnetic, acoustic, seismic, etc.

As for the practical applications of this discovery, the Russians point out that it will be possible to eliminate errors arising from misinterpretation of remote sensing data. Such as the position of military installations, perhaps?

Research Notes is written by John Wilson of the BBC World Service science unit.

RESEARCH NOTES

Unsuspected lighting hazards

Protecting electronic equipment against lightning surges is a long-established art, especially in situations where the vulnerable components are connected to aerial systems or transmission lines. But it seems that lightning still has a few tricks up its sleeve to

A powerful electrical storm produced this spectacular discharge at the Space Shuttle complex only hours before the launch of STS-8 (August 30, 1983). Picture by NASA.

defeat even the best engineered system, and nowhere more so than high in the atmosphere.

For those of us brought up on the notion that the greatest danger arises when you poke an earthed structure skywards into a black cloud, it's instinctively hard to understand why aircraft and spacecraft are so often struck, especially when there's no thunderstorm in progress. Yet the incidence and severity of strikes on flying objects are much greater than hitherto suspected, according to a team of US scientists working on how to safeguard future space shuttle missions.

Philip Krider and his group from the University of Arizona in Tucson have been firing small rockets into electrified clouds to try and understand the conditions under which discharges are initiated. They have also been measuring the characteristics of the discharges with a view to designing better protective systems for spacecraft that have to survive them. Already there have been cases of space missions wholly or partially lost as a result of attracting lightning strikes from a benign-looking sky.

Dr Krider's studies have revealed some alarming statistics, hitherto unsuspected. First of these is the fact that discharge pulse rise time can reach a staggering 400kA/μs, about 20 times greater than is allowed for in conventional lightning arrestors. Even with ground-based installations, Dr Krider believes that many arrestors work far too slowly to provide adequate protection against some of the super-fast pulses he's encountered in practice.

One further consequence of these high-speed pulses is that the inherent self-inductance of lightning conductors prevents them from acting like the earthed devices they're meant to be. So even if a conductor can handle a steady current of say 400kA, it may still present a sizeable impedance to the rising edge of a fast pulse. As a result, says Krider, there's a distinct possibility that the tip of a lightning rod will simply shower sparks in all directions. (Your columnist has seen a case where a lightning discharge jumped off a well-earthed conductor through one metre of air, preferring an alternative earth route*.)

Back in the air, however, Dr Krider and his team are still working on why lightning discharges can be triggered so easily by spacecraft. Given a better understanding of the conditions in which this can occur, it will be much easier to make safety decisions, especially when it comes to launching future space shuttle missions. But the real lesson from all this is that critical electronic systems must be protected to a far greater degree that has ever been done hitherto.

A million degrees of resistance

Any schoolboy (or girl) knows that the resistance of a conductor varies with temperature. Thus the variation of a standard platinum element forms the basis of the well-known platinum resistance thermometer. Most of us don't, though, have much experience of what goes on beyond the 3000°C or so of an incandescent tungsten lamp filament where the resistance is about an order of magnitude greater than its cold value.

When, therefore, a team from AT&T Bell and the Lawrence Livermore National Laboratories published a paper (*Phys. Rev. Lett.* 61 2364) entitled 'Resistivity of a Simple Metal from Room Temperature to 10^6K', even physicists were persuaded that it was a typographical error. But no, the team had indeed tracked the resistivity of aluminium all the way to a million Kelvin. Not, I hasten to add with a heat-proof Avo, or even a flame-resistant Wheatstone bridge.

The actual experiment consisted of firing extremely short (0.5ps) pulses of laser light on to aluminium films coated on a glass substrate. The pulses, with an energy of 7mJ, focussed on a target area of only 10^{-5}cm^2, created an incident intensity of around 10^{15}Wcm^{-2}.

To calculate the effect on resistance of the temperature rise caused by this enormous blast of energy, the physicists used an indirect approach based on a well-known relationship between refractive index and resistance. What they were actually looking for was an upward shift in the spectrum of the laser light as it was scattered from the million-degree aluminium plasma. This modulation due to the changing refractive index then had to be carefully distinguished from Doppler shift due to the sudden expansion of the target. Previously this Doppler factor had always precluded accurate refractive index measurements at ultra-high temperatures, but in this latest work it was effectively eliminated by the use of ultra-short laser pulses.

After performing the necessary calculations and eliminating a variety of other possible sources of error, the AT&T and Lawrence Livermore scientists believe they now have reliable figures for the DC resistivity of aluminium over a range of temperatures up to 10^6K. In practice, it rises steadily to around 4.6×10^5K where its value (200μΩcm) is around a hundred times the cold value. Then the value drops by about 20% as the temperature rises further to 10^6K.

This latter downturn is, say the team, consistent with the behaviour of a high temperature plasma, though the upward part of the curve is not quite in agreement with the classical picture of resistivity being proportional to temperature. This discrepancy is explained on the basis of the atomic lattice temperature being less than that of the electron gas.

All this is extremely fascinating, but at first sight of little practical value. Yet the very parentage of this work gives a useful clue to its most probable application in the search for sustainable nuclear fusion. The Lawrence Livermore National Laboratory is one of the world's foremost institutes working on the two essential pre-requisites: ultra-high temperatures and huge pressures. How materials behave under these extraordinary conditions is therefore of vital importance.

* See Lightning Strike, John Wilson, *Electronics & Wireless World*, October 1984 p.44.

RETURN OF THE VACUUM VALVE

Researchers at GEC are leading the way in the creation of whole families of new microelectronic devices based on a technology that electronics had almost forgotten.

ROSEMARY A. LEE

Until the 1950s, all active electronic functions were performed by the vacuum valve. In general, these were made up of metal electrodes suspended in a vacuum sealed glass envelope. Their sizes varied, but even the Nuvistor, one of the latest valves to be brought out in a metal ceramic envelope, had a volume of more than one cubic centimetre. It was not surprising therefore that when solid state devices were invented, one of their main attractions was their small size. As the technology developed, individual elements became smaller and smaller, until complete circuits could be designed on a single piece of silicon. This exciting development resulted in the gradual displacement of vacuum valves in receivers and low-power electronic systems. In high power transmitters vacuum valves continue to survive; and thermionic emitters are still used where a free source of electronics is required as in cathode-ray tubes. In addition, the high impedance of valves led to the production of high quality hi-fi and radio systems, and indeed many audio enthusiasts still insist on their superior performance.

Semiconductor devices are poorly equipped to survive certain environments and there is a need for devices which can work at high temperatures, withstand high voltage pulses and have the potential to provide high frequency operation. Vacuum valves offer such properties. Ironically, it is the semiconductor fabrication technology which has been developed over the past few years which now offers the opportunity of producing vacuum valves as small as transistors.

ELECTRON EMISSION

The operation of any vacuum valve depends on obtaining electrons from the cathode surface and attracting them to a positively-biased electrode known as the anode. The old type of valve operated with a thermionic cathode which was heated to give the electrons sufficient energy to surmount the surface barrier, escape into the vacuum and be attracted to the anode by a positive potential. The cathode was coated with an oxide layer to reduce the work-function and thus the energy required for an electron to escape (and it was heated to over 1000°C).

An alternative means of obtaining an electron discharge in vacuum is with field emission. This relies on a very high electric field being applied to a cold cathode which has the effect of thinning the surface barrier and making it triangular in shape. Electrons then have a finite probability of tunnelling through the barrier and being attracted to the anode (**Fig. 1**). Field emission is quite well characterized by the Fowler-Nordheim relation:

$$J=\alpha F^2 \exp\{-\beta\phi^{3/2}/F\}$$

where J = current density, ϕ = work function and
F = surface field.

Current density increases with increasing electric field and a reduction in work function. Electric fields of the order 10^9V/m are necessary before an observable current may be obtained; this is equivalent to 1000V across 1μm (1×10^{-6}m). Since most solid dielectrics can withstand little more than 10^8V/m, clever lithographic techniques are used to construct devices which enhance the electric field around the emitting area only.

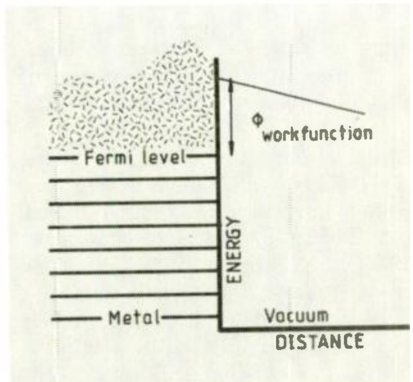


Fig.1a: thermionic emission. At high temperatures electrons are excited above the Fermi level and some gain sufficient energy to surmount the surface barrier and escape into the vacuum. Emission is increased by increasing the temperature or decreasing the work function.

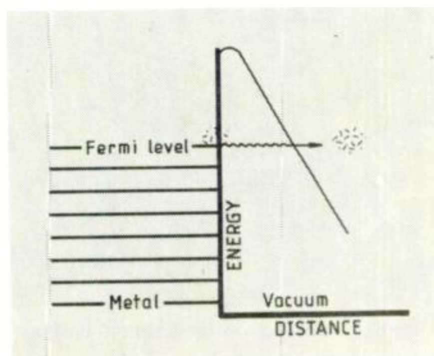


Fig.1b: field emission. At high electric fields the surface barrier is distorted to a triangular shape. This allows electrons to tunnel through the barrier. Emission is increased by increasing the electric field or decreasing the work function.

APPLICATIONS

There are many potential applications of vacuum microelectronics, but they all centre on the properties of field emitting devices. For example, raising the temperature of such a device will result in simply increasing its efficiency – for in addition to tunnelling electrons, the process will be combined with a proportion of thermionically-excited electrons escaping from the cathode surface. Technology can therefore be directed towards producing sensors and controllers in environments which are subjected to quite harsh temperature fluctuations such as those in boreholes, oil wells, nuclear reactors and jet engines.

For many years a great deal of effort has been directed towards finding a cold electron source to replace the thermionic cathode in such devices as cathode ray tubes, travelling wave tubes and microwave power amplifiers since this would be beneficial in terms of operating power and heat dissipation. Most of these efforts have been disappointing, through short lifetimes and erratic emission. Only recently has our fabrication technology allowed dimensionally accurate reproduction of sub-micron structures, and it has brought totally new opportunities in the control of cold emission.

There has been a growing concern over the malfunctioning of electronic components in space and defence systems when exposed to both ionizing and electromagnetic radiation. Semiconductor devices rely on the excitation of minority carriers for their operation. When exposed to ionizing radiation, they are bombarded by both neutral and charged particles, which cause fluctuations in current leading to failure of the device. The result may be transient upset or permanent damage. Vacuum valves are far more immune to such environments since

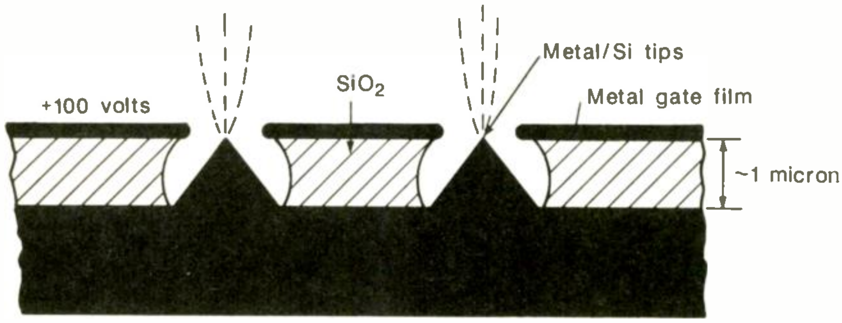


Fig.2. A typical field-emitting device consists of a metal or silicon substrate, with a number of small sharp tipped structures about 1-2µm high and 10µm apart. These have tip radii of about 50nm and are separated from an integral grid by 1-2µm of silicon dioxide. The structure is operated by applying a positive voltage of 100-200V to the metal grid, which creates a high electric field around each of the emitting tips from which electrons are emitted. These can be collected either on the grid itself of by an external anode held in close promixity to the tips. At SRI International, Menlo Park, structures such as these have given currents of 100µA/tip leading to current densities of 100A/cm^2 and lifetimes of over 60 000 hours.

the source of electrons is that of either a metal or highly-doped silicon cathode.

Vacuum valves work at much higher voltages than semiconductors which makes them far less sensitive to the large voltage pulses experienced, for example, during a lightning strike. The limitation is the current carrying capability of the electrodes themselves. In addition, the speed of a semiconductor device is basically limited by the time taken for an electron to travel from the source to the drain which in itself is limited by the number of collisions within the lattice of the solid. Vacuum valves, however, operate by electrons passing from cathode to anode within a vacuum and their passage is therefore unimpaired by molecular collisions. With dimensions of 1µm transit time of less than 1ps can be expected.

In any protection device which operates by short-circuiting the delicate components, it is necessary that the initiation takes place before the transient pulse causes the damage. Current surge arrestors exploit a discharge in an ionized gas which for certain applications does not operate rapidly enough. The combined properties of speed and survivability in hostile environments lead to the applications of very fast protection devices in communication systems, high-integrity logic elements and radiation-hard integrated circuits.

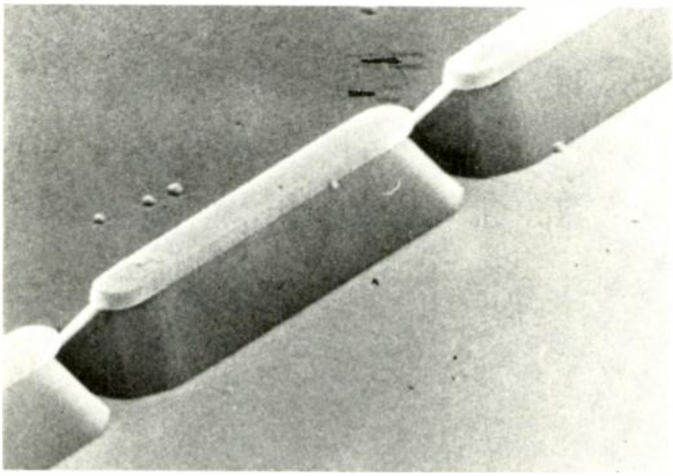
Since this same technology can also be applied to the realization of large area, full-colour, high brightness flat panel displays, a separate section of this article will be dedicated to this subject.

ELECTRON SOURCES

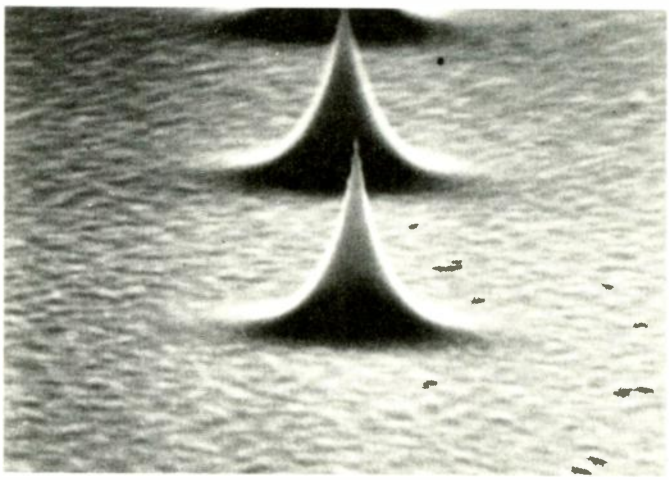
Most research programs in this field are concentrating on cold cathodes to take advantage of the small device size, instant start, low power consumption and high current densities which in turn will lead to high operating frequencies and fast switching.

Until last year, however, there was a major research programme at Los Alamos which produced miniature thermionic electronic components. This technique used thin-film deposition and photolithographic techni-

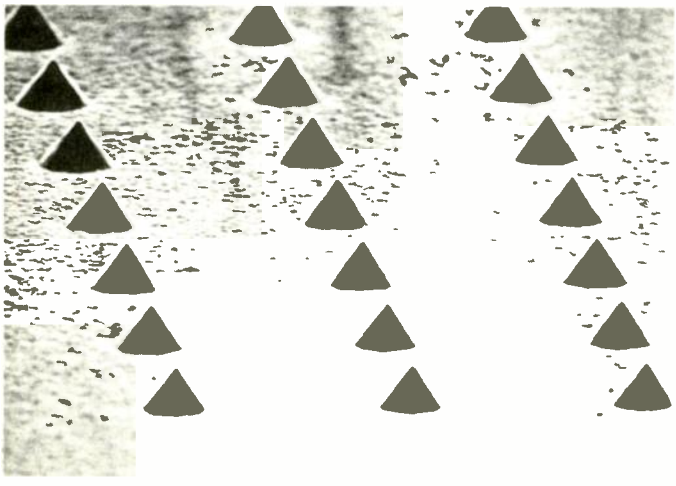
Fig.3. Silicon, niobium and gold emitters. These and the other photographs were produced at the GEC Hirst Research Centre.



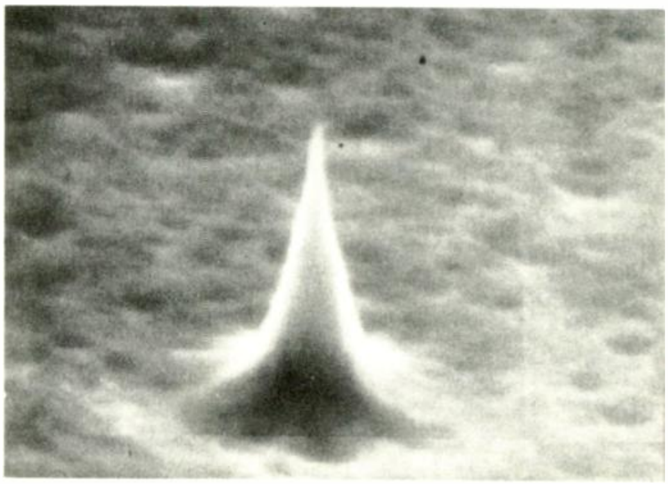
A partially etched wedge-shaped emitter 10µm long.



2µm high silicon emitter with 30nm tip radius.



Array of gold emitters 2µm high.



Niobium emitter 1.7µm high.

ques to produce integrated structures consisting of a grid and an oxide-coated cathode on one substrate, with an anode on a separate substrate directly opposite.

A different approach has been reported by the Philips Research Centre in Eindhoven which has exploited the strong internal electric field in a semiconductor with a reverse-biased p-n junction. A preliminary investigation was undertaken on various cathode geometries, but efforts were finally concentrated on a design which produced high current densities when the 1μm diameter emitter was about 10nm below the surface and parallel to it. In 1987 these cathodes were producing 1500A/cm^2 with 1.5% efficiency[1].

When a p-n junction is reverse-biased a very strong field is created in the depletion region. Electrons coming from the highly doped p-region are therefore accelerated and gain energy. Although much of this energy is lost in collisions with other electrons or optical phonons, a percentage of electrons have sufficient energy to surmount the potential barrier at the surface and escape into the vacuum. To improve the efficiency of the device, the work function is reduced by covering the surface with a monolayer of caesium. The complete structure consists of the p-n junction, as described, with an overlying gate above it separated by silicon dioxide. Such structures have already been incorporated into small cathode ray tubes to give clear, bright and well defined black and white and colour pictures.

The major area of interest in other groups is in lithographically defined sharp-tipped structures, which are incorporated into a diode configuration, and make use of a grid about 1μm away to create a very high field around the tip, which will then emit electrons. The typical structure is shown in **Fig. 2**, and is made up of small cathodes 1-2μm in height, with sub-micron (~50nm) emitting tips. These are separated from a metal grid 0.5μm thick by a layer of silicon dioxide.

A number of techniques may be used to produce such structures and these include the anisotropic etching of silicon, etching of a unidirectionally solidified eutectic system and the use of deposition techniques and UV or electron beam lithography.

The well-established team at SRI International in Menlo Park, California, USA, has published details of both fabrication procedures and the electrical characterization of field emission structures. To construct the diodes, they deposit on a substrate material first silicon dioxide and then molybdenum. Electron beam lithography is used to define the grid holes and the silicon dioxide removed down to the substrate. The next process is to evaporate aluminium at an angle whilst rotating the sample, which has the effect of reducing the diameter of the grid hole. This is followed by molybdenum deposition perpendicular to the substrate, and a lift-off procedure to remove the aluminium and excess molybdenum[2]. This produces very fine-tipped conical cathodes between each grid hole. At gate voltages in the region of 120V, current densities of over 100A/cm^2 have been obtained and lifetimes of over 60 000 hours.

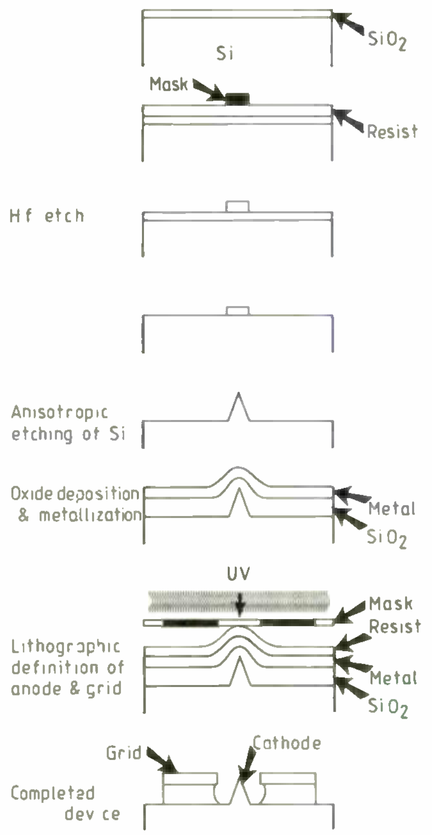


Fig.4: Processing sequence for the fabrication of silicon field emitting diodes.

DEVELOPMENTS AT GEC

GEC Hirst Research Centre is undertaking a research programme to investigate electron emission from novel structures with the long-term aim of producing a new range of micron-sized vacuum electronic devices. The programme began as a small feasibility study in July 1986 and has grown rapidly over the past two years because of the encouraging results obtained and the increasing need for such devices. GEC's is now the largest team in Britain.

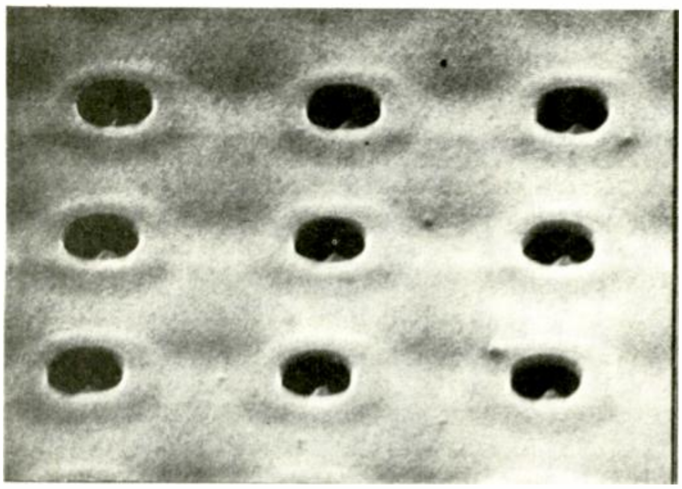
The programme consists of two projects running in parallel. The first concentrates on using lithographic definition of electrodes to create the high fields necessary for field emission, while the other is a longer-term programme to examine the fundamentals of electron emission in greater depth, with particular reference to noise, stability and reproducibility. In addition, methods are being explored whereby electrons are emitted from planar, chemically-modified surfaces, at electric fields some two orders of magnitude less than those conventionally associated with field emission. Preliminary results[3] have already shown that a cathode covered with a thin layer of organic film will produce emission sites at 10^7V/m. Research is being undertaken to clarify the mechanisms involved in such a process.

Significant progress has been made within Hirst Research Centre in developing a method of fabricating field emitting diodes suitable for a manufacturing process. A variety of wet and dry etch techniques have been perfected to form micron-sized cathodes in both metals and semiconductors (**Fig. 3**). The latter have been incorporated into a triode configuration consisting of an interdigitated anode/grid structure, using the 2μm-high miniature cathodes with sub-micron emitting tips and attaining packing densities of up to 2.5×10^7tips/cm^2. The procedure exploits standard semiconductor fabrication technology on four-inch silicon wafers; and one method by which the silicon structures are produced is depicted in **Fig.4.** A thin layer of silicon dioxide is thermally grown on a wafer of single crystal silicon, and patterned using standard UV lithography and etching techniques to form small pads of SiO_2 (1-2μm square). A wet anisotropic etch then attacks the different planes of silicon at different rates which results in the formation of pyramidal shaped structures which may be sharpened in a number of different ways. Dielectric deposition and planarization is then followed by metallization and the definition of gate electrodes. The final process step is the cavitating etch to remove dielectric from around the emitting tips. Each 2mm chip is mounted in a 16 pin dual-in-line ceramic package using a gold/silver eutectic and tested within a vacuum system capable of attaining 10^{-9} torr.

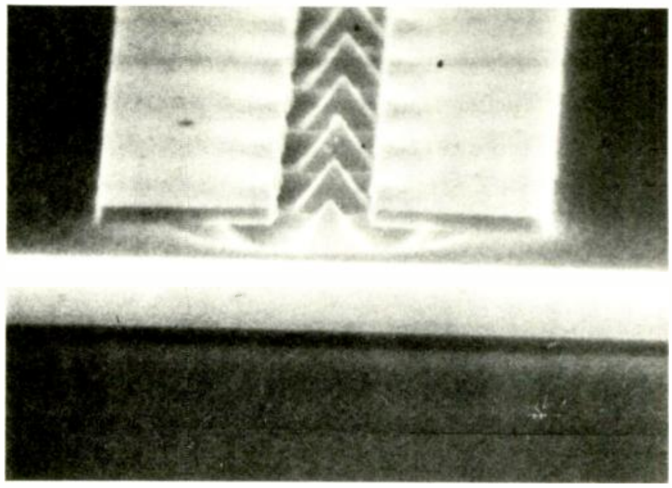
Preliminary results are very encouraging, with true diode characteristics observed (**Fig. 5**) and currents of up to 10μA obtained at 200-300V grid voltages from 80 n-type silicon emitters. Work is progressing rapidly towards the incorporation of metal emitters with the hope of attaining still higher current densities. Results from the SRI International programme show a realistic long-term aim of 100μA/tip or 100A/cm^2 at operating voltages of 100-200V.

Considerable electrode damage may be caused by a switch-on process during the initiation of electron emission but this can be much reduced by surface cleanliness. To study the effects of surface contamination, an ultra-high vacuum system with surface science facilities is being used (**Fig. 6**). It is important to clean the cathode surface thoroughly before making electrical measurements and this is achieved using fast atom bombardment and sample heating. Since monolayers of contaminants will form quite rapidly over the cathode surface the residual gases are analysed by a mass spectrometer and the chemical integrity of the surface is monitored by Auger analysis. An electron microscope with 200nm resolution is used to observe the device during and after operation, for detecting defects; this accelerates design optimization. The system itself can be evacuated to 10^{-11} torr and filled with a variety of gases so that operation under different environments may be examined. It has already been demonstrated that stable emission may be obtained at atmospheric pressure in inert gases.

It is important to remember that these devices have electrode separation of about 1μm, which is much smaller than the electron mean free path at 10^{-3} torr. This is of utmost importance when final packaging of devices is undertaken, since evacuation to 10^{-11} torr would be impossible in packaged isolated devices.



Part of a 10×8 array of emitters at 10μm pitch with an Al/Si integral grid.



Pyramids at 2μm pitch in a grid channel.

FLAT-PANEL DISPLAYS

Cathode-ray tube technology is 86 years old. It allows inexpensive black and white and colour display screens of varying sizes; but for many years there has been a demand for less bulky and portable flat panel displays having lower power consumption, improved contrast, brightness and full-colour definition. The three main contenders for replacing the CRT are the liquid crystal, gas plasma and electroluminescent displays. The liquid crystal displays (LCD) rely on the properties of aligned molecules which turn in an electric field. In the simplest form the liquid is held in a thin cell between two polarizers. In the off state, light is reflected, but in the on state an applied voltage realignment allows light to be absorbed by one of the polarizers. The LCD fulfils the requirements for size, weight and low operating power, and 14-inch diagonal displays have been successfully made with 960×1284 pixels. The main problems associated with LCDs are those of poor yield and high manufacturing costs when large screens are considered. Nevertheless they have already captured over half the total market for flat panel displays.

Gas plasma displays (GPD) rely on gas excitation between two electrodes which cause light to be emitted. Although there is no need for backlighting, the required power is still greater than that of LCDs. Substantial progress has been made, however, and while existing displays are confined to 16 levels of grey, there is a promise of 15-inch full-colour screens having 256 000 pixels. However, previous attempts to make full colour displays have had mixed success.

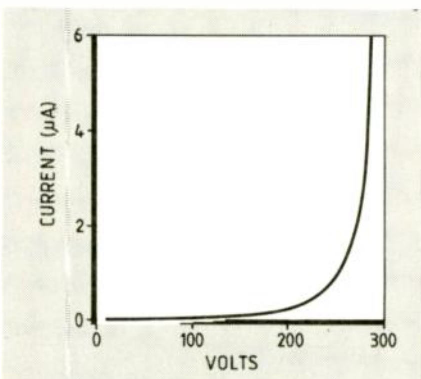
Electroluminescent displays (EL) use phosphors which emit light in the presence of an AC field. These give better contrast and broader viewing angles than other flat panel displays, and require less power than both CRTs and GPDs. These lightweight, compact displays are stated to be more reliable than CRTs with predicted lifetimes of 40 000 hours, though this has not yet been confirmed. In addition they are reliable in hostile environments, and are therefore important in military applications.

At present EL displays are quite expensive, four times the cost of an equivalent-size CRT display, but this is expected to drop to 50% by 1990. Displays of 12×14 inches have been made, with 640×400 pixels. The low level of brightness and the lack of a full-colour screen are the main disadvantages; and while good colours have been achieved with both red and green phosphors, it is difficult to produce bright blue emission. Both EL and GPD have the disadvantage of a lack of full colour. Furthermore they use expensive high-voltage devices.

FIELD-EMISSION FLAT PANELS

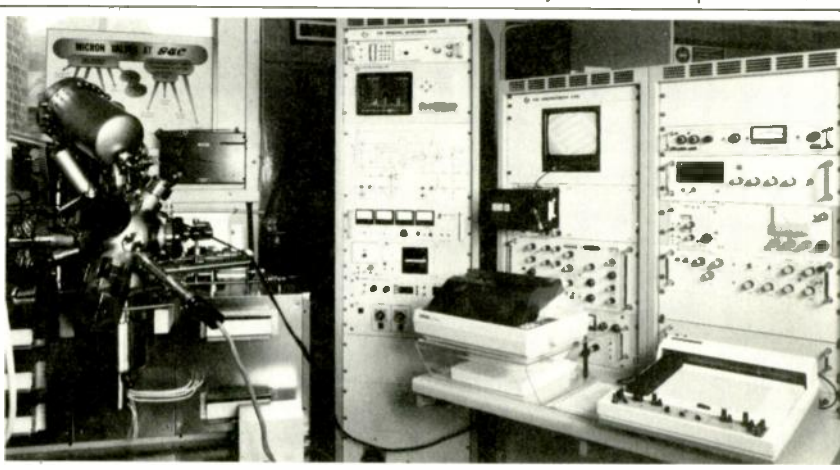
Field-emission flat panel displays have the advantages of high brightness, good contrast, low power consumption and full colour. In addition they are expected to be reliable in hostile environments. With each tip giving 10μA, a 10×10 array provides sufficient current for one pixel. The large number of emitters in one pixel tends towards a uniformity in emission and the fabrication is suitable for large areas of individually-addressable pixels. Cathodes

Fig.5: n-type silicon emitter incorporated into a diode configuration (above), and its corresponding electrical characteristics.



I/V plot for 10×8 emitting diode.

Fig.6. Ultra-high vacuum system for surface and electrical characterization.



COMPONENT	FUNCTION
Ultra high vacuum	6×10^{-11} torr, clean environment
Auger analysis	Surface chemical analysis
Fast atom bombardment	Sample clean Atom implantation
Heating	Sample clean
Heating, cooling (−150°C to 950°C)	Variable temperature characterization
High voltage lead-throughs	Electrical connections
Electron microscope (200nm resolution)	Sample observation E-beam irradiation
Mass spectrometer	Residual gas analysis Outgassing detector End point detector
Manipulator	x,y,z linear displacement 1 and 2 rotation
Large cold trap	For vacuum integrity

have been shown to operate well in vacuums of 10^{-5} torr and since the average electron mean free path is greater than the electrode separations, the life expectancy is long since the cathodes will not be plagued by erosion from ion back-bombardment. The team at SRI has already produced a full-colour display using this technology on a five-inch silicon wafer baseplate[4] with three colour elements and 114 244 individually-addressed pixels.

The screen is coated with indium tin oxide and patterned with strips of colour phosphor, each 60μm wide. The cathodes with integral grid are separated from the screen by small pillars about 75μm high which allows a voltage of up to 1000V to be applied. Each 250μm pixel is addressed by contacting the cathodes from a molybdenum backplate 175μm wide in one direction, and the three 40μm gate electrodes orthogonal to this. The matrix is operated by sequentially addressing one line at a time in the horizontal direction while simultaneously driving all the gate lines in the vertical direction. Very high brightness has been achieved with green phosphors at 200V, but so far the red and blue phosphors require 500V. Dimensions are therefore quite critical in terms of voltage for optimum brightness without precipitating the onset of vacuum breakdown. The whole plate is vacuum sealed after baking at 125°C for 12 hours which achieves a pressure of 10^{-10} torr. If emissive flat panels are to take a significant fraction of the market this relatively late starter looks very promising, and while many major assembly and processing problems have been overcome, there are many technical issues to be addressed before a useful display is placed in production.

THE FUTURE

Reproducibility, stability and noise level are amongst the problems associated with field emitting devices. Solutions must be found before we shout "*eureka*" and sail forward into production. Expectations are high, however, as we look forward to the understanding and control of electron emission emerging from our research programmes.

● The First International Conference on Vacuum Microelectronics was held in Williamsburg last year, with over 200 attending from France, Holland, Japan, Russia, USA and UK. Britain is hosting the Second Conference in Bath in July and is already attracting much interest from both academic and industrial organisations world-wide.

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Dr Rosemary A. Lee is at the GEC Hirst Research Centre, Wembley, Middlesex.

UPDATE

Research profile – NPL

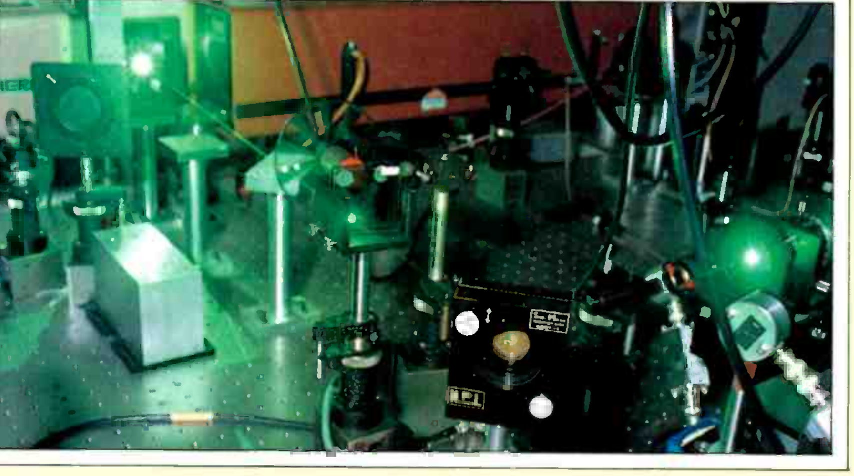
MARTIN ECCLES

For the National Physical Laboratory, keeping ahead of industry in areas so diverse as determining references for the country's ever-advancing measurement needs and providing new standards for testing in the information-technology field is an enormous task. As a result, the way the NPL at Teddington works has been gradually changing over the past few years.

In the early days, the laboratory was full of boffins creating mechanical, electrical and electronic devices that were at the forefront of technology. Although there are still a lucky few who get their hands on a soldering iron at NPL, increasingly the work of scientists there involves creating ideas for tools and instruments to be implemented by outside specialist organizations.

Looked at in cold financial terms, this situation is sensible. Just to build a tool like the ultrasound beam calibrator outlined here would require at least C and Forth programmers, 68000-processor hardware and software engineers, an ECL designer and ultrasonics expert. And what do you do with these specialists when the project is finished?

But don't get the impression that NPL is just a site of offices full of paper scientists. Round every corner you'll find superconductors, lasers, cryogenic installations and computers – an exciting experience for any engineer.



In order to characterize wide bandwidth instruments such as sampling oscilloscopes, transient digitizers and transmission lines, pulses with fast well-defined rise times are needed.

Here, an argon-ion laser pumping a dye laser produces light pulses of around 1ps. These pulses feed a fast photodiode, resulting in an electrical pulse of sound 10ps that is suitable for calibrating oscilloscopes capable of around 25ps rise time.

Width of the 10ps electrical pulse is measured to a resolution of 1ps using a lithium tantalate crystal with a 50Ω transmission line upon it. As the pulse travels down the transmission line its electrical field causes a non-linear effect in the crystal that allows the pulse width to be measured optically using birefringence (Pockles effect).

Growth in the fibre-optical equipment market is running at about 20-30%. Another area of high activity in the Division of Electrical Science is in optical-fibre measurement. NPL has facilitates for bandwidth measurement in multimode fibres to over 1.5GHz at both 850nm and 1300nm.

An increasing proportion of resources will be applied to anticipating new measurement problems like those in heterodyne and wavelength-multiplexed systems, and novel types of fibres and devices.

Accurate measurement ensures the safe and effective use of ultrasound in medicine. The NPL ultrasound beam calibrator shown here is a multi-element piezoelectric polymer hydrophone connected to a fast data-acquisition and microcomputer-based presentation system.

Both the ultrasonic beam profile and the captured acoustic pressure waveform for any selected hydrophone element are presented in real time, as are peak acoustic pressure and the pulse repetition rate. Other important parameters such as pulse, temporal and spatial average quantities are presented typically within three seconds.

In the UK, there are no regulations regarding power output from medical ultrasound imagers. Until recently, this was not a problem since technology did not allow high-power transducers to be produced.

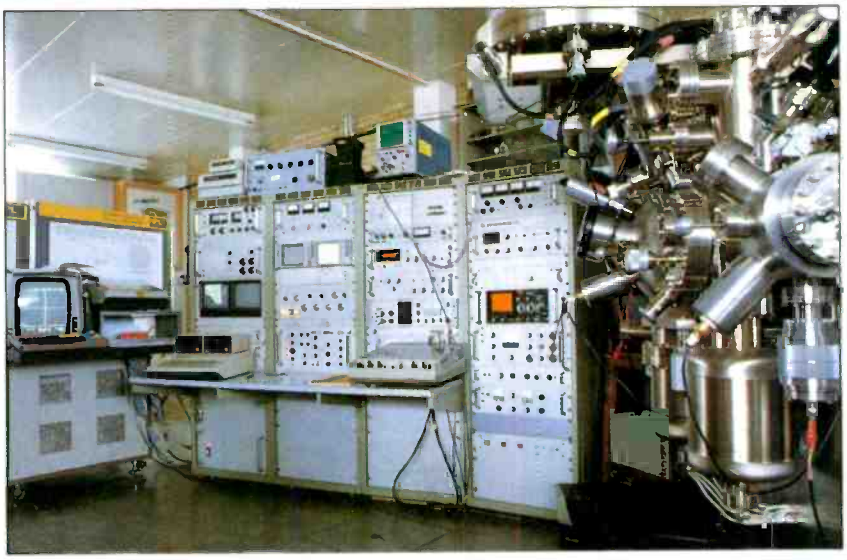
Now though the power of ultrasound imagers has increased to such an extent that a scanner for Doppler blood-flow measurement can produce the same output as an ultrasound diathermy unit.

In essence, the National Physical Laboratory functions as the standards laboratory for the UK, being one of the research establishments of the Department of Trade and Industry; it operates the base of physical metrology needed by any industrial economy. The NPL is the originator and steward of the National Measurement System, using national standards and those of our trading partners and undertaking the required research and international comparison. The laboratory provides calibration, laboratory accreditation and consultancy services throughout industry.

There's little point in having a highly accurate standard resistor of an ohm if its value cannot be accurately translated into higher values. Using a superconducting transformer, this computer-automated apparatus allows resistors with a ratio of 10:1 to be compared very accurately.

Supercooled by liquid helium in the vessel on the left, the 10:1 ratio superconducting transformer works at DC. Combined with a squid – a superconducting quantum-interference device – acting as a null detector, this lead-based-foil transformer forms a highly accurate cryogenic current comparator.

UPDATE



This electron-spectroscopy equipment designed for material surface analysis is one of the tools available to NPL's Soldering Science and Technology Club. On the CRT display you can see a minute grid used for calibrating the equipment's electron microscope.

As researcher Colin Lea points out, the laboratory's services to the UK PCB assembly industry are much more active than those relating to the country's semiconductor manufacturing industry. This highlights the fact that the country's *forte* is in circuit-board assembly rather than ic production.

One recent problem researched at NPL is that of PCB 'outgassing' which, during wave soldering, causes tiny bubbles resulting in unsoldered areas of PCB. These areas are of particular concern since they have to be manually checked and repaired at the end of the production line.

Since these pits often contain oxides and other contaminants, the post-production soldering temperature has to be high. Added to that disadvantage is the fact that manual soldering is expensive and difficult to control, resulting in decreased circuit reliability. These bubbles cost money.

Soldering is not the only area of PCB manufacture that NPL's Division of Materials Applications gets involved with. Judging by current Government murmurings, there are likely to be drastic changes in the way that circuit boards are cleaned after soldering.

Currently, chloro-fluorocarbons provide the best solution; but, being unfriendly to the ozone layer, they are likely to be replaced. Trichlorethane is an obvious replacement since it doesn't yet fall under the category of an ozone damager – but it could. Provided that the problems of removing residues can be solved, high pressure water jets could provide an answer. When looking into cleaners, NPL's Division of Material Applications has to take into account such eventualities.

In integrated-circuit manufacture, there is increasing demand for higher accuracy in measuring sizes and positions of features on masks and wafers, film thickness and wafer flatness. NPL works on standards for all of these measurements.

Equipment shown here makes use of a standard mask produced at NPL for microscope calibration. On the standard mask – part of the Alvey project – are calibrated lines of various thicknesses down to 1μm.

At the left-hand side of the monitor display is a waveform relating to the light-versus-dark portion of the microscope image to the right of it. This waveform has sloping sides; the real edge of the microscope image lies somewhere on that slope.

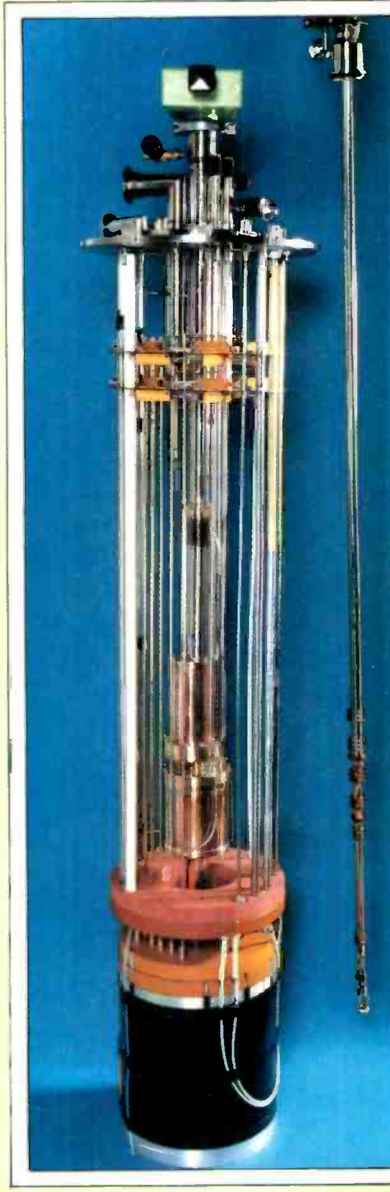
Image shearing is commonly used to determine exactly where the real image edge occurs. Two identical waveforms representing the same light or dark area are slid alongside each other until any peak or valley between them disappears; at this point, the waveform edges cross at 50% intensity.

In combination with an accurately calibrated standard, image shearing provides a sensitive method of edge location with a repeatability of 0.01μm.

There are indications that the ohm standard used for the past fifty years is decreasing at about 75nΩ per year. Left alone, the standard ohm – actually an average value of five one-ohm standards – would be a short circuit in about 13 million years. Periodically though the ohm standards are corrected using a calculable capacitor and a series of complex AC and DC bridges.

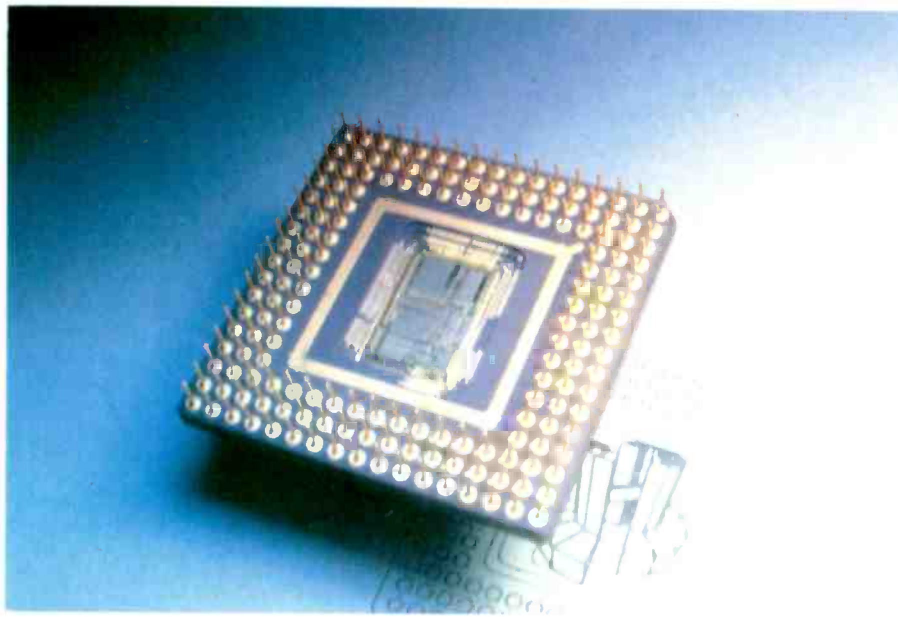
Very soon, the standard ohm will probably be derived from references of 6453.2Ω and 12906.4Ω. These rather strange values are those produced by a recently-discovered effect called quantized Hall resistance.

Hall resistance in certain semiconducting devices has quantized values that depend on only two fundamental physical constants – electron charge and Planck's constant. Work is underway to determine whether or not these values can become the basis of a quantum standard of resistance similar to that of the Josephson superconductivity effect used for the direct-voltage standard since 1973.



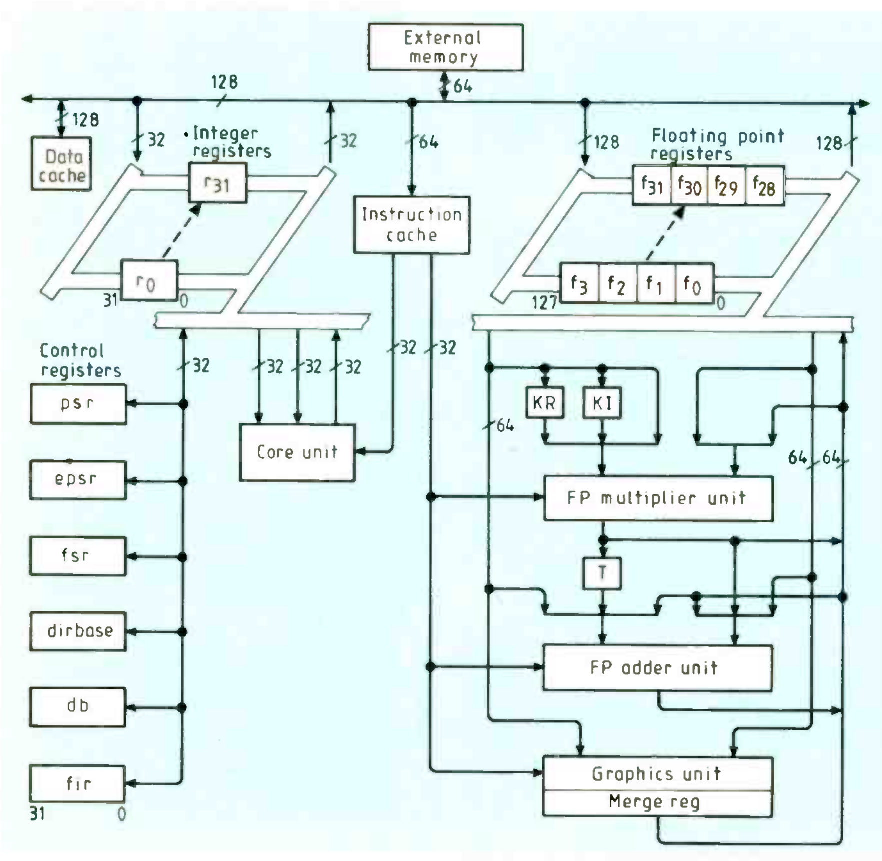
Intel's biggest by far

Intel's designers were given a budget of "a million transistors" to work with when they began engineering on the 80860 general purpose processor. Their efforts have resulted in the world's most powerful microprocessor capable of churning over at least 120 million instructions every second. The device has already received a degree of endorsement by IBM, a matter of profound significance to the computer industry.



Every figure associated with the device is superlative. It can load four 32-bit registers simultaneously within a single clock cycle producing an internal bus bandwidth of 1Gbyte/second. The external bus can receive and transmit 64-bit words at a 20MHz word rate while remaining compatible with the 80386-based microchannel bus structure. The risc based integer core – that's the part of the processor which normally handles standard computing functions such as string comparison, database operations, etc. will process 40Mips. This is around eight times as fast as an 80386 running at 25MHz.

The integer performance is all the more surprising if one considers the separate floating point facilities which run in parallel. These comprise a full 32-bit floating point unit which runs in conjunction with a full 64-bit adder. Both structures can be made to run concurrently using a double instruction fetch/clock. The FPU section can notch up 80 million operations per second in this mode. For instance, this would allow shading operations at 50 000 triangles per second in 3-D graphics applications. The performance amounts to 86 000 dhrystones/second compared with around 17 000 dhrystones/second attainable with a 386/387 combination. Intel reckons that the 80860 will provide double the performance of a Mips Computers R3000 risc chip set, the most powerful currently available.



The graphics facilities are augmented by an integral decoder which will execute an extra 15 instructions dedicated to 3-D replots directly within the FPU section. And don't forget that none of this greatly affects the integer processor which can be performing other tasks at the same time.

Unlike any other Intel processor, this one includes on-chip instruction and data caches which, although relatively small in comparison to standard multi-chip systems, substantially improve loop execution speeds. Accounting for some 30 per cent of chip area – the device measures 15mm on a side – the caches work much faster than the off-chip variety because the signals don't have to leave the chip. Buffering and I/O nearly always involves substantial speed penalties.

A device like this is nothing without software. The company has declared its intention of "creating a standard architecture" which will be based on Unix. It has announced a jointly with AT&T, Olivetti and Prime Computer the development of an operating system based on Unix V release 4.0 for multiuser systems. This will open up a wide variety of minicomputer applications in the power workstation market.

The first 80860 applications are likely to be hung on the back of 386-based systems as specialized accelerators, for instance 3-D modelling. The sharing of data types, page tables and bus structure with the 386 will make this relatively easy. Intel will eventually produce specialist hardware to allow multiple 80860 devices to operate within parallel processing systems.

ISSCC report

FRANK OGDEN

The International Solid State Circuits Conference, organized by the IEEE, which took place in New York in February proved quite conclusively that the semiconductor industry can find uses for a million transistors on a chip for more than just memory, despite the predictions made just a few years ago. The Intel 80860 (dealt with elsewhere in this issue) with its promise of a single chip supercomputer stole the show. But there were plenty of laudable offerings from other manufacturers presented in a lower profile.

PROCESSORS

The Intel design offers a peak processing performance of 33 Vax Mips within its risc processor core handling integer instructions. An experimental MPU architecture from the mini-maker DEC can execute an integer 32-bit instruction every 20ns, notching up a peak performance of 50Mips from around 300 000 transistors. Like the Intel part, DEC's architecture relies heavily on internal cache for both instructions and data to keep up the processing rate. The internal data bus bandwidth of the DEC chip can reach 400Mbyte/s. The equivalent value for the 80860 is 1Gbyte/s, mainly due to the on-chip floating point facilities.

The cacheing system recognises the data snarl-ups which occur when the main processor core has to go off-chip to fetch either instructions or data. On-chip cache provision will become the hallmark of next generation processors. Intel's successor to the 386, the 486, is said to run DOS applications at three times the speed of the existing part largely through the use of on-chip cache and floating point facilities.

Specialist processors can be built for out-and-out speed over the few instructions which they are required to process. Plessey's 1024 point FFT processor works at a rate of 200Mips allowing a complete 1K transform in less than 100μs. The processing rate takes on even more astonishing proportions when devices are connected in parallel. Six devices connected in this manner will compute the 1024 point transform at 40MHz sample rate. To put this performance into perspective, Plessey quotes an equivalent process time of 1ms for a high-end general DSP chip and a figure of 250μs as applied to building block solutions.

The memory architecture within the FFT processor allows data to be loaded and dumped concurrently while a transform is being executed. Since the memory bandwidth requirement for the Radix-4 algorithm used in the device is half that required by the more usual Radix-2 algo, it becomes possible to spend more time on memory transfers than the 40MHz internal clock rate suggests.

BICMOS

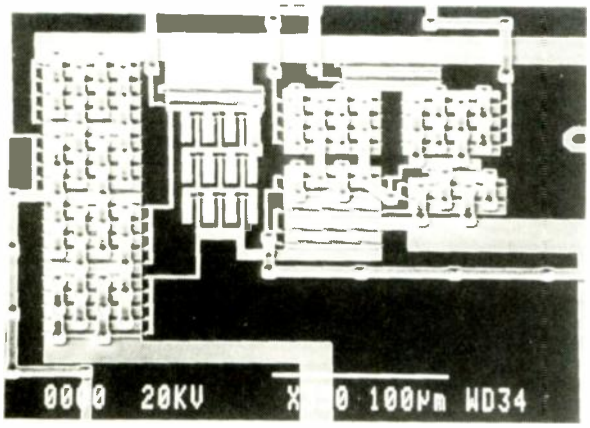
It is widely acknowledged that silicon bipolar transistors have higher transconductance, better tracking and greater output drive capability than their fet counterparts. Cmos technology offers lower power consumption and higher density than bipolar. A combination of the two would appear to deliver the best of both worlds. However, mixing the two technologies forces some undesirable compromises, particularly in the extra masks required for the manufacturing processes.

The voltage sensitivity of bipolar ECL has prevented its integration on to large cmos chips with their variable and spiky power rails but the IC manufacturers now appear to have effected an interesting marriage. By using a fet strapped as a constant current source in the collector of a bipolar current amplifier/switch, most of the advantages of ECL can be realised without the voltage sensitivity. This is the essence of the bicmos process. A Hitachi experimental 32-bit microprocessor with 521 000 fets and just 8000 bipolar transistors located at strategic nodes such as I/O and clock lines has shown itself capable of running at 70MHz clock rate. The silicon has been written with 1μm design rules and dissipates just over two watts at full speed.

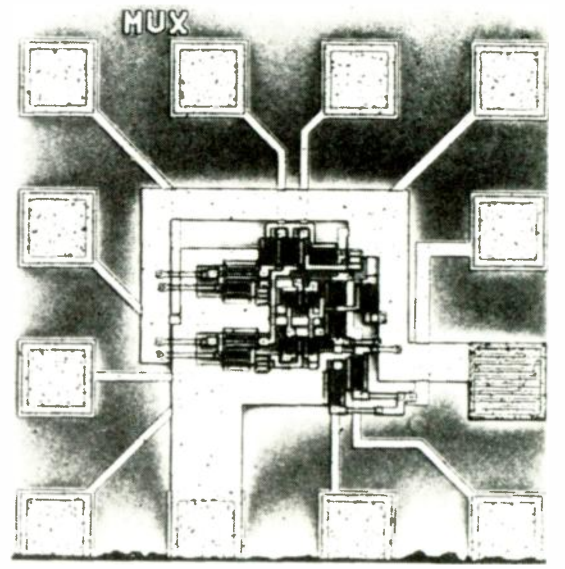
STATIC RAM

Operating speed has always been the principal benchmark for static memory, now becoming so important for fast cache applications in risc processors. The speed and power of bicmos readily lends itself to dense memory designed to operate at the highest possible speed. Hitachi gave details of a 512Kbit static ram which could address any of its locations in just 5ns representing an effective gate propagation delay of just 150ps. This memory was made with a triple-level polysilicon process on 0.8μm geometry. The bipolar devices used in the driver and skew-critical placements returned f_T values of 11GHz.

A second paper from the same company detailed an ECL/cmos 16Kbit memory with a quoted access time of 3.5ns, the device being written in 0.5μm rules. It makes one wonder



Above: An experimental GaAsfet operational amplifier with a unity gain bandwidth of 10GHz. The Electrical arrangement is shown on the opposite page.
Right: Silicon still has much to offer. This divider chip from Siemens will accept an input clock of 15GHz.



if GaAs technology will ever make it to the big time when bulk silicon can be pushed to these limits.

The highest static ram densities demonstrated at this year's conference were built into one megabit parts typically returning an access time in the 8ns region. Hitachi, Texas and Toshiba were the sponsoring companies.

DYNAMIC RAM

Dynamic ram technology is generally accepted as the driving force behind the semiconductor industry's process development. The d-ram sessions are regarded with great importance and are always well attended. The dynamic ram session was dominated by the Anamartic paper which gave details of the industry's first workable waferscale serial memory (see last month's issue page 413). Providing 200Mbit, 20µs worst case access to anywhere on the wafer, it has an ingenious system of redundancy which will make use of even partially functioning individual 1Mbit ram dice. Papers on devices at the 16Mbit level concentrated on the problems of manufacturing test without adding much of material interest to potential users. However, power dissipation and rail voltages have more significance.

The use of dynamic rams in battery-based equipment was tackled in a paper from Hitachi. The company proposed a 16Mbit device running from a 1.5V power rail. Naturally such a low operating voltage poses all sorts of problems in maintaining logic level thresholds within the chip. It also results in a low amount of stored charge making the device susceptible to soft errors caused by alpha particle strikes originating in the packaging material. Even so, eight of these devices arranged as a 16Mbyte memory bank will operate, Hitachi says, for a total of 500 hours from eight 2Ah dry batteries.

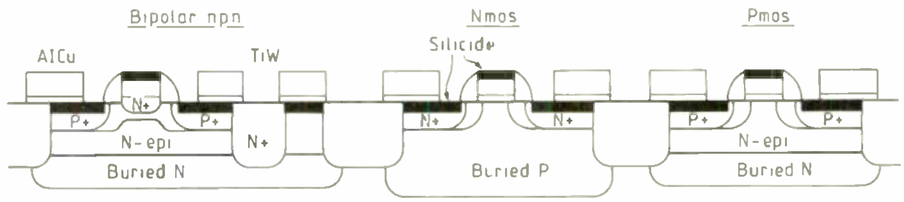
The 1.5V d-ram may or may not turn out to be a practical device. Either way, it seems likely that the standard operating voltage of 16Mbit and beyond memory devices will be reduced to 3.3V in a bid to keep down potential gradients in the shrunk device elements. Mitsubishi published a paper on such a part which could return an access time of 60ns.

NON-VOLATILE MEMORY

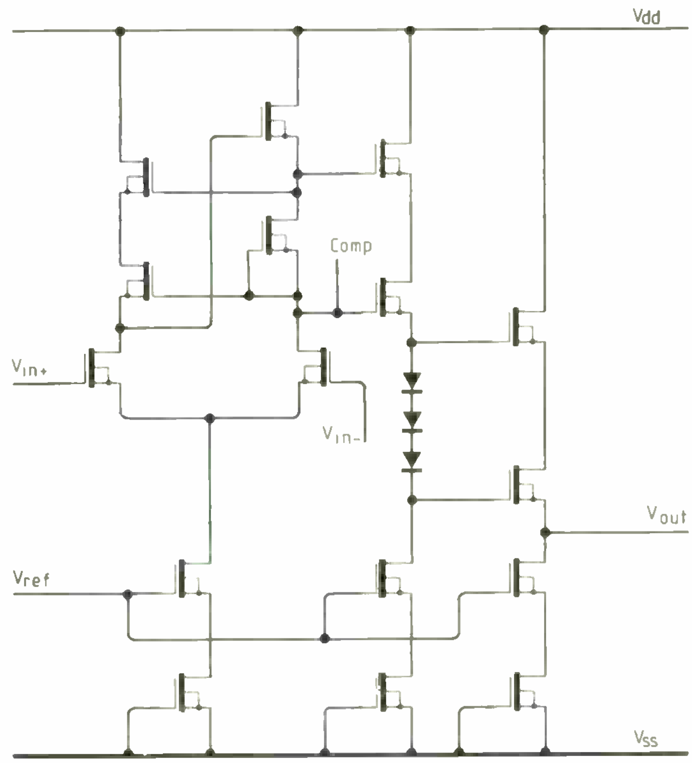
System designers look to semiconductor non-volatile memory to provide a replacement for mechanical hard drives. The wafer scale memory outlined earlier seems like a contender until the power gets removed. Electrically erasable non-volatile devices provide readability, re-write and, in the case of Intel and Seeq's "flash" technology, one shot device erase.

Intel discussed a 1Mbit device with a access time of 90ns, an active power consumption of 40mW and just 20µW in standby. The company reports a durability of 10^7 write/erase cycles. The finite limit to the number of times which a memory location can be re-written results in eventual deteriorat on in the storage transistor tunnel oxide where trapped charge is injected to decide the cell logic level. This applies to all current eprom technologies though.

A similar 1Mbit device from Seeq exhibited a 120ns access time.



Bicmos comprises both bipolar and cmos devices on the same chip to provide the best combination of power and speed. Devices cost more to make. The drawing shows a Signetics bicmos structure.



Circuit diagram of the Hughes 10GHz operational amplifier.

GATE ARRAYS

Big gate arrays are certainly the driving edge of asic technology. There can be few bigger than the experimental 1.4 million transistor array from Hitachi which offers a potentia of 130 000 gate equivalents together with 38Kbit of static ram. The 0.8µm production process results in 350ps propagation delay per gate and an access time of 4ns for the static ram section. Programmability of such a large array is another question. The company says that several designs have demonstrated a gate utilisation 40 to 50 percent.

The fastest experimental gate arrays are once again those fabricated in GaAs technology. The individual heterojunction bipolar transistors which make up the modest array designed by an IBM research team show an f_t of over 40GHz. Arranging individual cells as flip-flop structures has demonstrated a toggle rate of 7.5GHz. But as fast as its devices are, GaAs technology never seems to result substantially in commercial LSI and the same is probably true for gate arrays made using the material.

MISCELLANEOUS

The same fate will probably befall a GaAs operational amplifier device presented at the amplifier sessions. The mesfet technology provides a unity gain bandwidth of 10GHz with approximately 40dB of gain available at 500MHz. Produced by a research team from Hughes, individual transistors are constructed with 0.2µm gate lengths.

A 15GHz divider chip emphasised the speed potential of standard silicon processing. Looking for all the world like a standard ECL input stage, the Siemens bipolar device consumed a mere 250mW to implement the divide-by-16 function. A relatively cheap component such as this is likely to make direct synthesised microwave systems much more accessible.

Picture enhancement on a chip

C-mos asic chip house LSI Logic has produced a single chip processor which provides one of the main ingredients of a picture enhancement process.

The device is a DSP which puts the histogram/Hough Transform to work. It plots a histogram of grey level occurrences within a frame of an image. The L64250 will work on pixel array sizes of up to 4096 × 4096 at data rates of 20MHz. The calculated histogram can tell a computer where to expand the contrast range within a low contrast image.

The Hough transform section implements an algorithm which can determine edge location. The image is divided into parallel lines which are projected on to a point defined by the slope and the Y-axis intercept of the line. The presence of an edge in the image coincident with one of these lines will result in a high value for that point.

Portable satellite phone

The satellite phone link shown here mounted on a yacht was developed by British Telecom to provide the ultimate in cordless telephones for people who want to be seriously distanced from civilization.

Making use of Inmarsat, the terminal uses a small, omnidirectional aerial which requires no pointing or set-up.

Flat TV glass plant

In a statement of confidence about the optimistic future for flat screen television, Corning Glass is to invest $40 million in a substrate glass plant in Shizuoka, Japan.

The ultra-flat product must be able to accommodate up to one million transistors formed on a polysilicon-on-glass layer. This requires a surface smoothness of the glass substrate comparable to a silicon wafer. The low alkali baria-borosilicate glass is produced directly from a melt in large sheet areas. The company uses both laser and ultrasound techniques to confirm the smoothness of 0.2μm.

Hot sensor

Philips has designed a capacitive transducer designed to measure the running clearances between engine casing and turbine blade tips in aero engines. The company says that the device will work at up to 600°C under the highly stressed conditions found in this type of application.

Optical phone line

This is the first part of an optical telephone cable connecting Windermere to Coniston and all places between. It is being installed by British Telecom at a cost of £1 million.

Top DOS processor

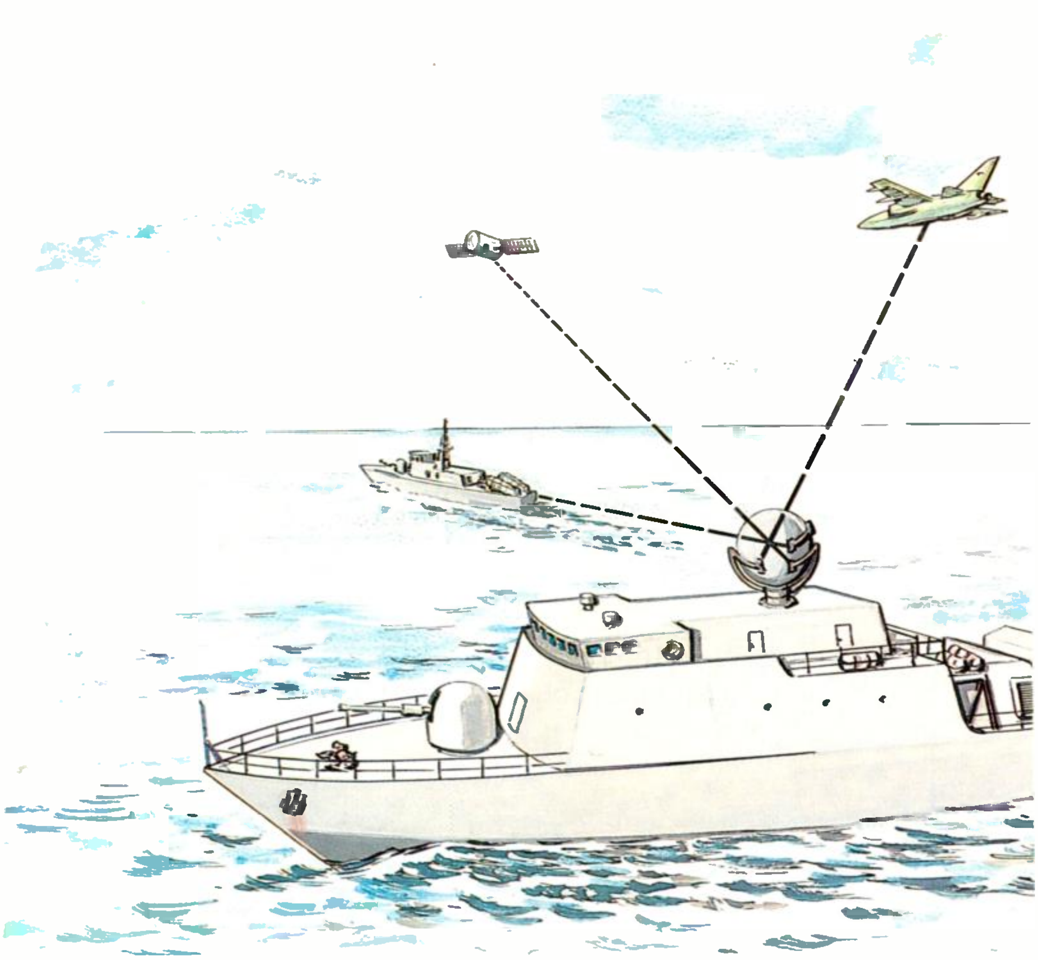
Although at the time of writing the official Intel announcement has yet to be made, more details have emerged about the successor to the 80386 chip, the 80486. It is projected to run at least three times faster than a 386 and will incorporate both instruction and data caches using one million transistors.

The device will be totally code compatible with 386 but it won't carry an on-chip floating point unit: this will be made available as a separate chip along the lines of an 80387. The cache facilities on the 486 are expected to account for at least half the chip area allowing very fast DOS operations.

● There are persistent rumours that Sinclair Research is working on a high performance risc processor set which effectively emulates 80386 instructions. This would allow the building of IBM compatible architecture with improved performance over Intel-based versions. Sir Clive Sinclair told *Electronics & Wireless World* "We are working on all sorts of things which I am not able to talk about."

The concept of the spherical Luneberg lens has been with us for decades, but has seen only limited practical application. In the late 1950s and early 1960s the concept received considerable attention because of its capability of supporting multiple beams and covering a very large scan region. The advent of phased arrays – which can rapidly scan many beams and cover a relatively large scan region – quickly dulled the interest in the spherical lens. However, in the light of present-day military communications needs, there is renewed interest in the lens.

Rapid communication of accurate information between military ground, sea, air, and satellite stations is essential. Military communications links involve a large number of frequency bands and targets can be present in a vast array of geometries. For these reasons, multiple object tracking and communication through a shared aperture over a broad range of frequencies and a hemisphere of angular coverage are desired. Phased arrays cannot do this because they can be made to operate at only one or two frequencies. However, a spherical Luneberg lens with several different feeds can accomplish the task; such a system concept for naval application is shown in **Fig. 1**.



LUNEBERG LENS REVIVAL

The needs of military communications have brought renewed interest in the spherical microwave lens

MARK A. MITCHELL and JOHN R. SANDFORD

LUNEBERG LENS

In principle, the ideal spherical Luneberg lens is fairly straightforward. The dielectric constant of the lens varies from a value of 1 at the outside to 2 in the center the exact variation of dielectric constant with the radius from lens centre being given by

$$\epsilon_r = 2 - \left(\frac{r}{r_o}\right)^2$$

where r is the radius from the lens centre, r_o is the outer radius of the lens and ϵ_r is the dielectric constant (or relative permittivity) of the lens. Such a lens will perfectly focus a plane wave to a point on its surface, the result being comparable to the focusing of a perfect parabolic dish. In fact, an entire family of the lenses exists in which the radius of the focal point can be chosen arbitrarily to be inside or outside the lens. As the maximum inner dielectric constant decreases, the focal radius increases. This is illustrated by the trivial case of a lens of entirely unity dielectric constant, whose focal radius is infinite.

The concept of a multiple-beam antenna based on the Luneberg lens is also fairly simple. A spherical lens presents the same focusing aperture for all directions, so that a plane wave incident on the lens from any direction will be focused precisely to a point on the opposite side of the lens. Many different signals can therefore be received (or conversely transmitted) through the lens at once by simply placing numerous feeds opposite the respective signal sources. In principle, the ideal lens works equally well at all frequencies, but of course in practice there are limitations on the usable frequency bandwidth.

No method of fabrication which will produce the continuous permittivity variation of the ideal Luneberg lens is known. Instead, a number of concentric shells of constant permittivity give a quantized approximation to the ideal lens. The number of shells determines the bandwidth of the lens, with a greater number of shells providing a larger range of operating frequencies although, since there is a small reflection loss at each dielectric interface, more shells are not necessarily better. A number of test lenses have been constructed and analysed, the largest of which is 120 cm in diameter and is shown under test in **Fig.2.** It consists of 15 concentric shells of constant permittivity, each shell being approximately 4 cm thick, and performs adequately over a frequency range from 2 to 20GHz. A single hemisphere of the lens is shown in **Fig. 3**, in which the individual dielectric shells can be seen.

COMPONENT TECHNOLOGY

A number of advances in technology since the early 1960's have made an antenna system based on a large spherical Luneberg lens more feasible. The most notable are improved polystyrene expansion capabilities, the advent of microstrip arrays, development of mechanical robotic arms, and the emergence of sophisticated numerical computers. The exact role of each component technology on the overall system will

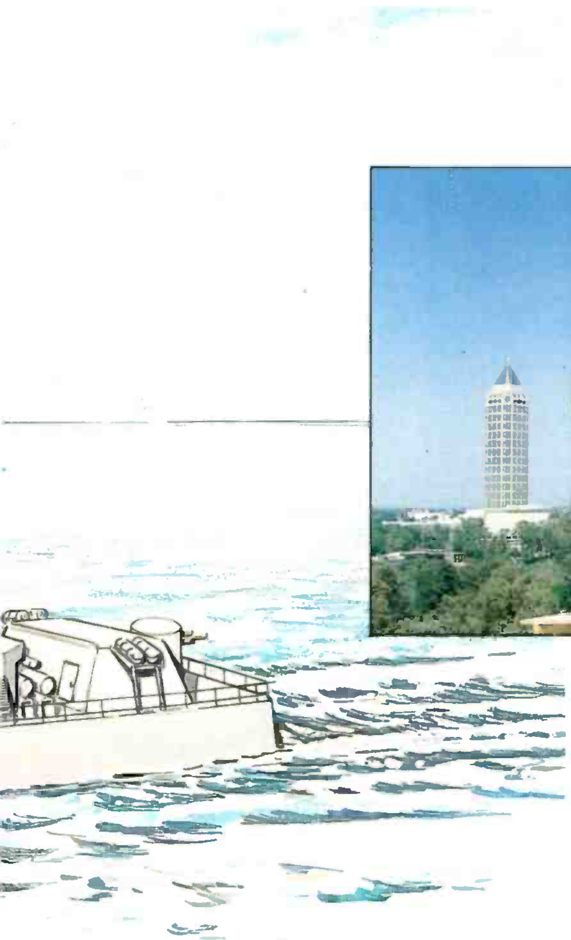


Fig.1. The spherical antenna enables propagation in many directions simultaneously.

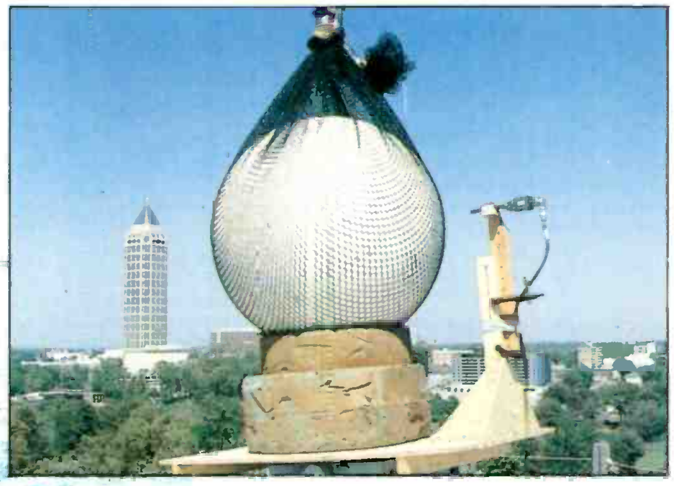


Fig.2. Spherical antenna under test at Georgia Tech.

Fig.3. Half a Luneberg lens, showing the shells.

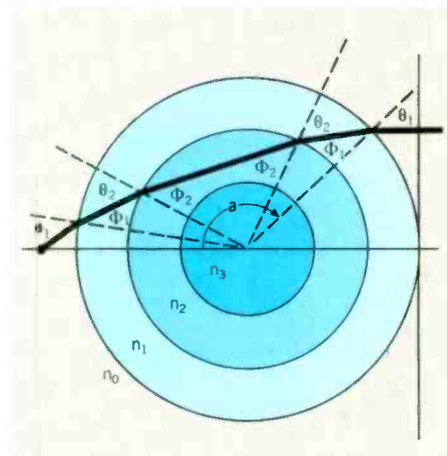


Fig.4. Path of a ray through the lens. Layer construction is practical alternative to continuously varying density of material.

be examined in detail.

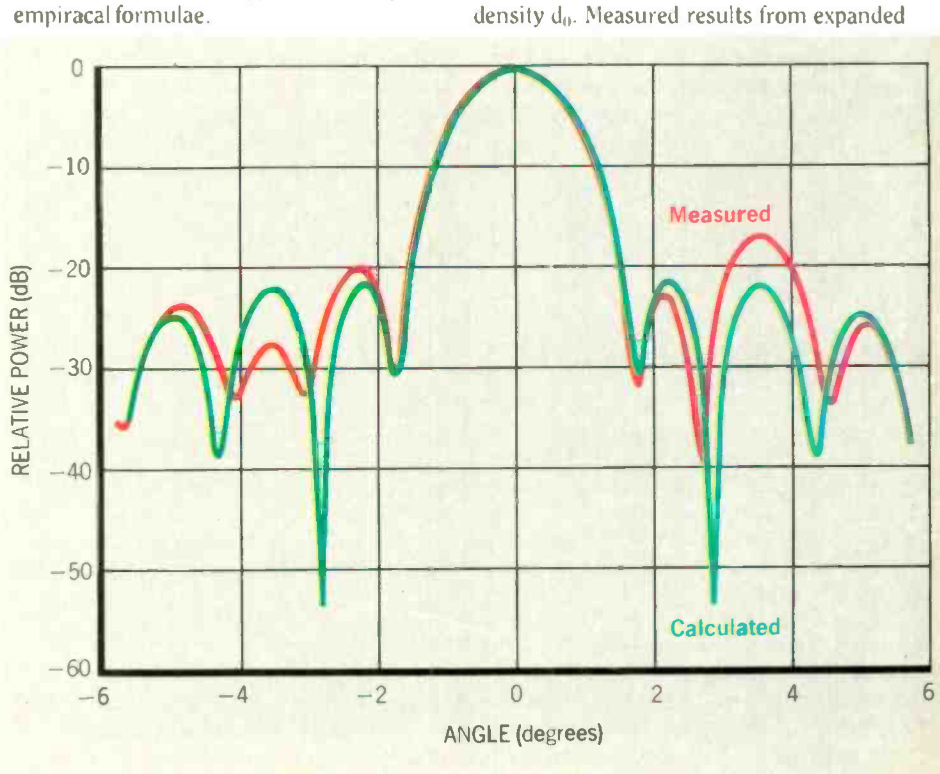
When quantized Luneberg lenses were initially studied some thirty years ago, no method for analysing their performance theoretically was available. It is now a relatively simple task to predict the gain and far-field radiation pattern of quantized lenses using numerical analysis. First, geometric optics (ray tracing) is used to determine the field in the aperture of the lens/feed system. Rays are traced from the feed through the lens, taking into account the refraction and reflection at each dielectric interface, to an aperture plane opposite the feed. An example of a ray traced through a small lens is shown in **Fig.4**. The far-field radiation at any angle may be computed from the resulting aperture field by means of the Fourier transform. When circular polarization and a circularly symmetric feed are used, circular symmetry exists for the feed/lens system. In this case the aperture field will be circularly symmetric as well, and the Hankel transform (see box) may be used to compute the far-field pattern, saving considerable computation. **Fig.5** shows a comparison of measured and computed radiation patterns for the aforementioned 120 cm diameter test lens.

The dielectric material (or materials) used to construct a quantized Luneberg lens must have a low loss tangent (typically <0.01) to avoid excessive ohmic losses in the lens and variability in dielectric constant to provide the necessary discrete shells. Polystyrene is typically used because of its low loss tangent (about 0.0043) and dielectric constant in solid form of 2.54. Dielectric constant generally varies with density, and raw polystyrene in bead form may be expanded to different densities to yield dielectric constants from near unity to two. The exact variation of dielectric constant with density is not known, but it can be approximated by two empiracal formulae.

$$\epsilon_r = \epsilon_{r0}^{\frac{d}{d_0}}$$

$$\epsilon_r = 1 + \frac{d}{d_0}(\epsilon_{r0} - 1)$$

where ϵ_r is the dielectric constant at density d, and ϵ_{r0} is the dielectric constant at solid density d_0. Measured results from expanded



The Fourier Transform is very well known by circuit and communications engineers. It turns up in transformations from the time domain to the frequency domain, and vice-versa.

Not quite so well known is the fact that taking the transform of the spacial distribution of the field across a dimension in an aperture aerial yields the angular pattern of the distant radiation field. Two such FTs relate according to

$$F(\theta) = \int_{-\infty}^{\infty} f(x)e^{-j\theta x}dx$$

$$f(x) = \frac{1}{2\pi}\int_{-\infty}^{\infty} F(\theta)e^{j\theta x}d\theta$$

Aerials are often distributed in two dimensions. Other similar distributions include optical components such as lenses, and TV pictures. FTs can be extended to cover two-dimensional distributions:

$$F(p,s) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} f(x,y)e^{-j(px+sy)}dxdy$$

$$f(x,y) = \frac{1}{4\pi^2}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} F(p,s)e^{j(px+sy)}dpds$$

For the special case when the distribution is circularly symmetrical, which is true for many aerials, the variation with angle is constant. Transforming the Cartesians to polar coordinates; $x = r\cos\alpha$, $y = r\sin\alpha$, and $p = q\cos\beta$, $s = q\sin\beta$. Also from this, $r^2 = x^2 + y^2$ and $q^2 = p^2 + s^2$, so that $f(x,y)$ can be written $f(r)$. The element of area dxdy in the two-dimensional plane transforms to $rdrd\alpha$ (see Fig.1) and the first of the two-dimensional FT expressions looks like

$$\int_0^{\infty}\int_0^{2\pi} f(r)e^{-jqr\cos(\alpha-\beta)}rdrdx$$

As $f(r)$ is independent of angle, this equals

$$\int_0^{\infty} f(r)\left[\int_0^{2\pi} e^{-jqr\cos(\alpha-\beta)}d\alpha\right]rdr$$

Now, in a definite integral, the symbol under the integral sign doesn't matter. It is often termed a "dummy variable".

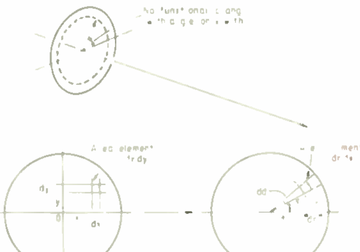
$$\text{put } \alpha-\beta=\theta$$

$$d\alpha=d\theta$$

because α and β are orthogonal (i.e. not functions of each other). Therefore the integral, written now as **F**(q), is,

$$F(q) = \int_0^{\infty} f(r)\left[\int_0^{2\pi} e^{-jqr\cos\theta}d\theta\right]rdr$$

The standard integral for the zero-order Bessel function $J_0(qr)$ appears in the square brackets[1]



$$\therefore \quad F(q) = \int_0^{\infty} rf(r)J_0(qr)dr$$

with

$$f(r) = \int_0^{\infty} qF(q)J_0(qr)dq$$

as its "mate".

These are the zero-order Hankel Transforms, arising when the circular symmetry is present. Therefore they are likely to appear in the geometry of symmetrical aerial and optical problems. Finally, corresponding to all the Bessel functions J_n, a whole series of Hankel transforms exist for the higher orders.

Reference

1. 'Joules Watt' Bessel and his Functions *E & WW*, p1101, November 1987.

polystyrene samples agreed well with a compromise between the two formulae; namely, a weighted average using 60% of the linear approximation and 40% of the exponential approximation.

A set of hemispherical moulds is used to form the individual shells of the lens. Expanded-polystyrene beads are packed between the appropriate male and female moulds in a steam-heated pressure chamber. After a designated amount of time in the chamber, the high temperature and pressure bond the beads together to form a hemisphere shell. Pairs of these shells are fitted together for form a complete spherical lens.

A number of small feeds supported by independent robotic arms produces the desired antenna system, interference between arms being avoided by using thin feeds at slighly varying radii or by computer control of the robotic arms. Theoretical and experimental investigation has shown that a small four- to twelve-element array can feed the lens from radii slightly different from the focal radius with little loss in performance. In particular, an X-band microstrip patch-array of twelve elements was used to feed a small test lens (approximately twelve wavelengths in diameter), and the gain varied by less than one decibel over the range of feed radii from 6.8 to 8.3 wavelengths. The element phase settings are varied with the radius in order to optimize gain. A microstrip array of this type can be made quite thin, easily allowing room for three separate feeds within the range of usable feed radii. **Fig.6** shows how the far-field radiation pattern of a lens with a feed one wavelength away from its focal radius is improved by the use of a defocused array feed.

REMAINING QUESTIONS

There remain some questions about the applicability of spherical Luneberg lens antennas to a wide range of communication tasks, the most critical being the mass of the lens. The outer shells of the lens have about the same density as a polystyrene cup or ice chest, and are therefore relatively light. Towards the centre of the lens, however, the shells' density increases, as does the weight. As a point of reference, the 120 cm diameter prototype lens has a mass of about 230 kg – fairly heavy, but still probably manageable. Unfortunately, mass varies with the cube of the diameter, so a large communication lens of 240 cm diameter would have about eight times the mass or 1840 kg. It will be necessary, therefore, to find a lighter alternative to the polystyrene used to construct the prototype lens. Some possibilities in this area are already being explored.

If a suitable lightweight dielectric material can be found, it is conceivable that the lens might find its way into many other communication roles. A single lens antenna could, for instance, be used to communicate via many different satellites at once. This is a particularly appealing possibility, since the many feeds would be stationary – eliminating interference problems – and could all be located exactly at the focal radius.

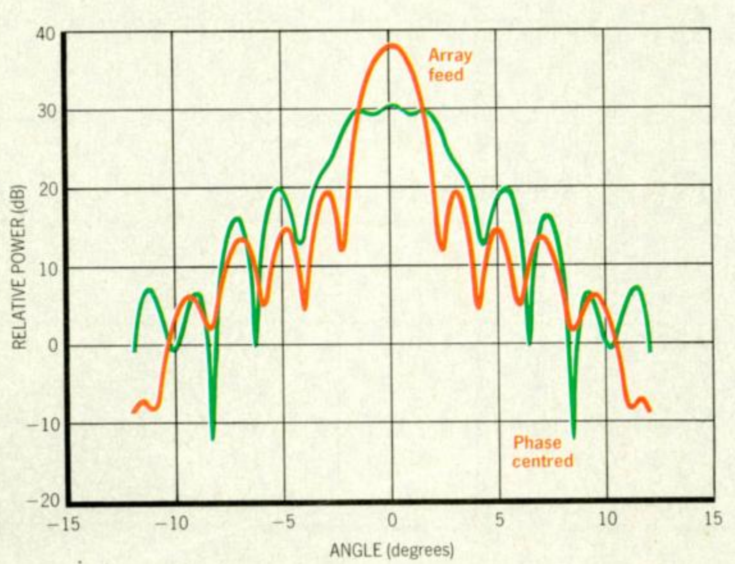


Fig.6. With the feed one wavelength away from the focus, an array gives an improvement over a single feed.

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6. M.A. Mitchell and J.R. Sanford, "Design and Analysis of Multi-shell Spherical Microwave Lens Antenna", *ANTEM '88: Symposium on Antenna Technology and Applied Electromagnetics*, August 1988.

Both authors are at Georgia Tech Research Institute, Atlanta, Georgia

APPLICATIONS SUMMARY

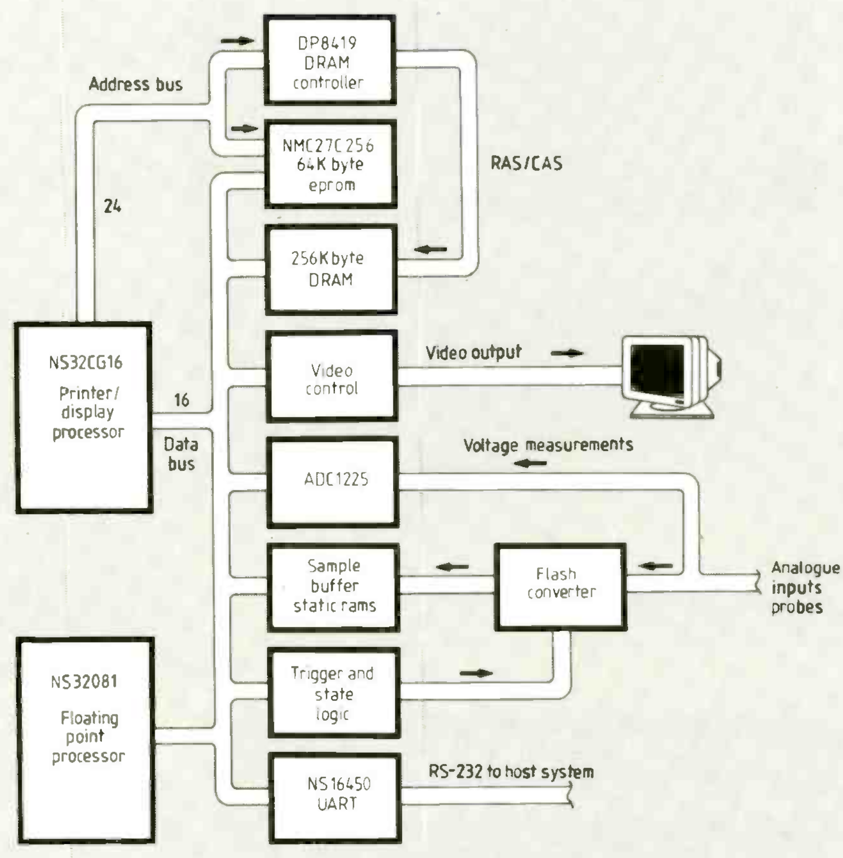
32bit processor for peripherals

One application suggested for the new NS32CG16 32bit peripheral processor is an instrumentation oscilloscope. According to the device's brochure, the CG16 is ideal for video displays in instruments since it can function both as a CPU and a graphics controller, eliminating the need for separate devices.

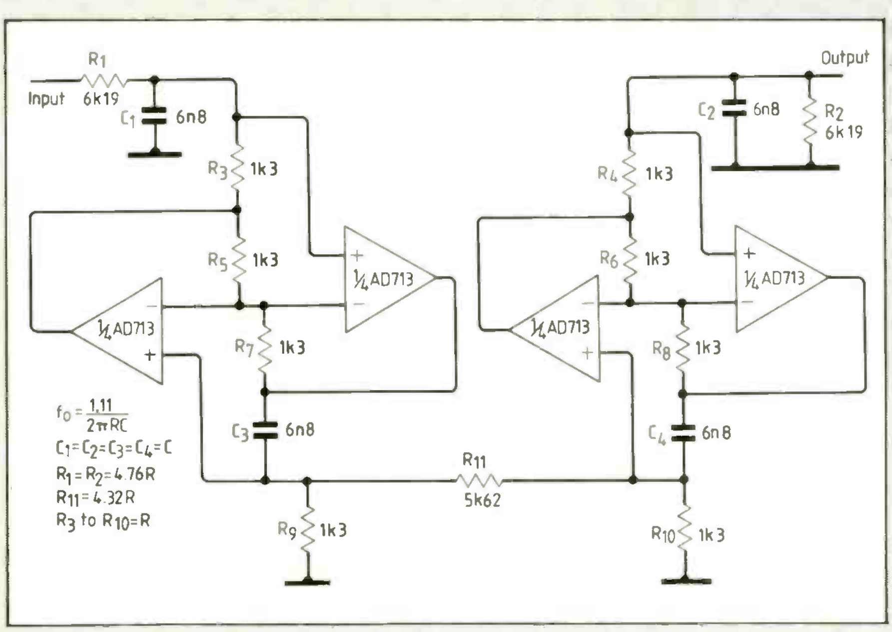
In this proposal, the 32801 floating-point unit provides the support needed by the CG16 to perform FFTs for spectrum analysis, mathematical functions, digital-cursor control, extrema and smoothing. Being designed for high-speed intelligent image processing in facsimile machines, laser printers, etc., the CG16 lends itself to the vector graphics processing that would be required in an instrumentation oscilloscope. According to National, Dataquest predicts that by 1993 there will be twice as many 32bit processors used in office-equipment peripherals as there will be office computers.

A number of applications are outlined in the brochure. More detailed application notes, including software, are given in NS32CG16 Technical Design Handbook. They include line/circle drawing routines, an introduction to Bresenham's line algorithm and image rotation.

National Semiconductor, 301 Harpur Centre, Horne Lane, Bedford MK40 1TR. 0234 270027.



Instrumentation scope



Third octave filter

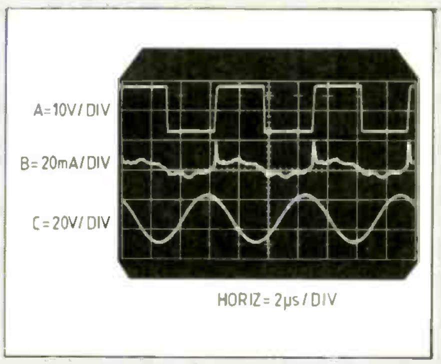
Quad op-amps save board space, reduce inventory and assembly operations, and have inherent tracking of the four amplifiers. Even so, in some applications their use is prohibited because of crosstalk and poor matching between each amplifier.

An outline of a new Bifet quad op-amp with local crosstalk is given in volume 22 of Analog Dialogue from Analog Devices. The AD713, a quad 711, has had its crosstalk minimized by careful design as the graph shows. Matching is also good; input offset voltage, drift and bias current are matched to within 0.8mV, 25μV/°C and 25pA respectively.

Having a THD figure of 0.0003% and a slew rate of at least 16V/μs, the 713 is ideal for audio applications. In this circuit a gyrator is used to produce a ⅓-octave bandpass filter such as is used in audio spectrum analysers.

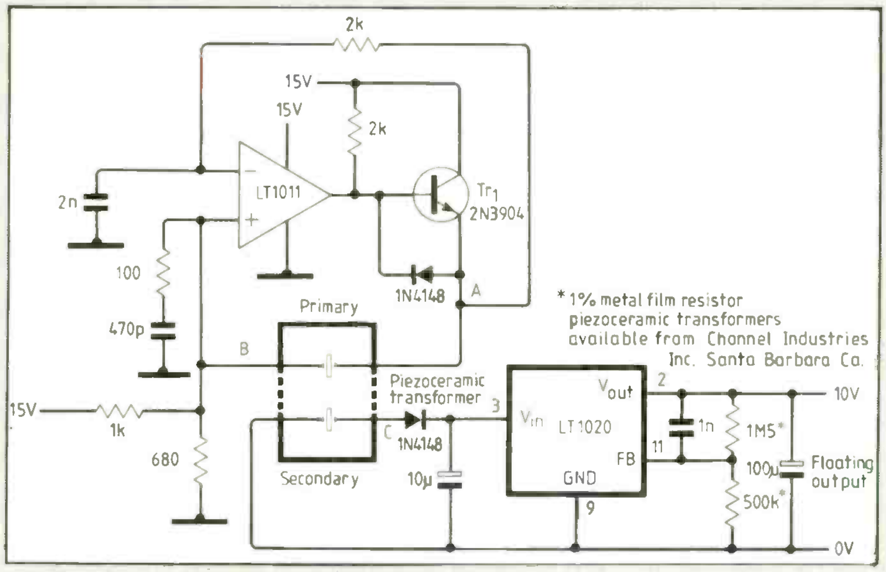
The filter can handle a 7.07V RMS signal

DC converter with 20kV isolation



Precise floating measurements and transducer measurements at high common-mode voltages require very low leakage to ground.

Magnetic transformers normally provide galvanic isolation in these applications but acoustic transformers are simpler and can provide higher isolation, as in this circuit producing 10V at a few milliamps with 20kV isolation. According to Linear Technology's Application Note 29, insulation resistance of the piezo-electric transformer is $10^{12}\Omega$ and its primary-to-secondary capacitance is between 1 and 2pF.



Driving the piezo-electric transformer – which may be considered as a high-Q resonator – is covered in the circuit's discussion. There are around 30 other circuits in note 20, which is entitled "Some thoughts on DC to DC converters".

Linear Technology, 111 Windmill Road, Sunbury, Middlesex TW16 7EF. Tel: 0932 765688.

If you are interested in piezo-electric transformers you should see Research Notes on page 752 of the August issue. Ed.

Electromagnetic scattering calculations

One of a number of application notes sent to us recently on the Intel iPSC supercomputer outlines the calculation of electromagnetic scattering. Professor Don Wilton and his team at Houston University has developed a Fortran program for calculating electromagnetic scattering and radar cross section of objects of arbitrary shape in three dimensions.

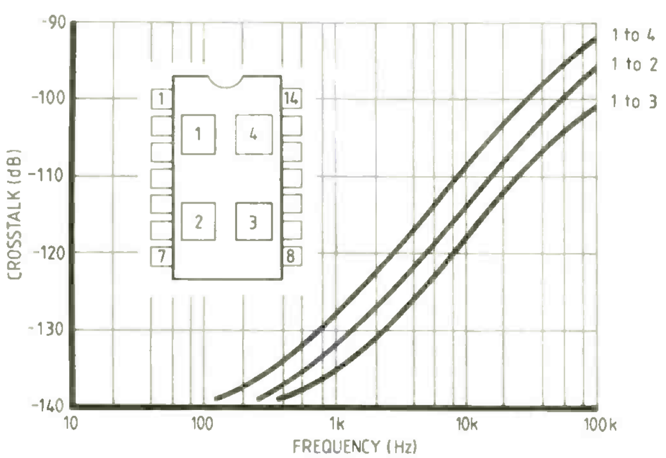
The program finds approximate solutions to Maxwell's equations using a finite element applied to the electric-field integral equation.

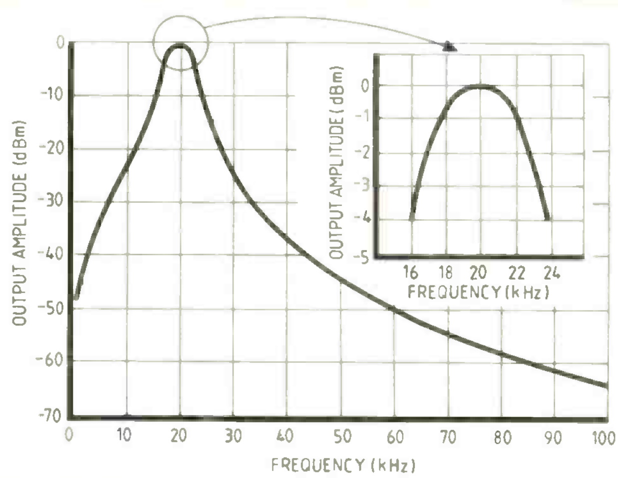
Intel Scientific Computers, Pipers Way, Swindon, Wiltshire SN3 1JR. Tel. 0793 696000.

with a THD of less than 0.002% from 20Hz to 20kHz. Performance meets ANSI Class II specifications for roll-off smoothness, shape factor and pass-band flatness.

Other items discussed in Analog Dialogue include an 8bit 200 megasample/s flash converter, a four-channel video multiplexer and an 18bit audio d-to-a converter.

Analog Devices, Station Avenue, Walton-on-Thames, Surrey KT12 1PF. Tel. 0923 232222.





ACTIVE

ASIC

Cmos asic family. CMOS-5V is a new range of asics which is compatible with the CMOS-5 5A family and is suitable for use where low gate counts and high I/O requirements are combined. Toggle frequency is 100MHz. NEC Electronics (UK) Ltd 0908-691133

A-to-D and D-to-A converters

Analogue I/O port. The AD7669 analogue I/O port combines an eight-bit A-to-D converter and two eight-bit D-to-A converters. The on-chip A-to-D converter provides a maximum conversion time of 2μs to ±2LSB. Analog Devices 0932-232222

10 bit flash converter. The Comlinear CLC920 is a 10 bit, high-speed A-to-D converter with full flash architecture. It is a bipolar device with a 25Msample/s throughput, but dissipates only 3.65W. SINAD is 58dB for an input of 1MHz at 20Msample/s. Integral linearity is within 1LSB and dynamic range is over 55dB. Anglia Microwaves Ltd 0277-630000

Linear integrated circuits

Eight-bit A-to-D converters. ML2252 and 2259 are additions to the Microlinear range of SAR A-to-D converters, which have a 6.6μs conversion rate (including sample and hold), enabling them to digitize a 50kHz, 0V to 5V sine wave with 47dB s/n ratio. No separate crystal is needed. Ambar Cascom Ltd 0296-434141

Quad sample-and-hold amplifier. The AD684 quad sample-and-hold amplifier samples at rates near 100ksample/s with true 12 bit performance. Each channel has a maximum acquisition time of 600ns to within 0.1% and 1μs to within 0.01% for a 10V step. Analog Devices Ltd 0932-253320

Cmos timer. The Samsung KS555 cmos timer provides a higher performance than the standard 555. Improvements are on 80μA supply current; 2-18V supply voltage, 20pA threshold trigger and reset current; 500kHz operation, and no need for crowbar protection for the supply. Kord Distribution 0276-685741

Switching regulators. The PSR and NSR families provide non-isolated positive and negative outputs of 5, 12, 15, 24 and 36VDC at currents of 3A to 8A (12A for 5V types). An external voltage or resistor will control output voltage over the range 0 to 108% of nominal. Melcher Ltd 0425-474752

Analogue multiplexers. The DG408 and DG409 offer an on resistance of 40Ω, with a maximum of 100Ω. They are direct replacements for DG508A and 509A devices, but with reduced leakage currents and faster switching. Siliconix Ltd 0635-30905

Microwave devices

Directional coupler. The WR28 10dB coupler offers better than 50dB directivity over the waveguide band of 26.5 to 40GHz. Model 22134-10 is suitable for use in reflectometer measuring systems. Flann Microwave Instruments Ltd 0208-77777

Optical devices

High-power optical ICs. Pilkington Guided Wave Optics introduces a range of high-power circuits based on lithium niobate. Single-mode waveguide chips which can handle over 500mW have been developed. Configurations include travelling-wave modulators, low-drive-voltage devices for 500MHz operation, beam splitters, polarizers and others. Barr and Stroud Ltd 041-954 9605

IR-emitting diodes. The Philips CQY90A high-intensity IR GaAs diode is designed for remote control. Radiant power is 21mW and the half angle of intensity is 60°. Peak wavelength is 940nm at 50mA. Gothic Crellon 0734-788878

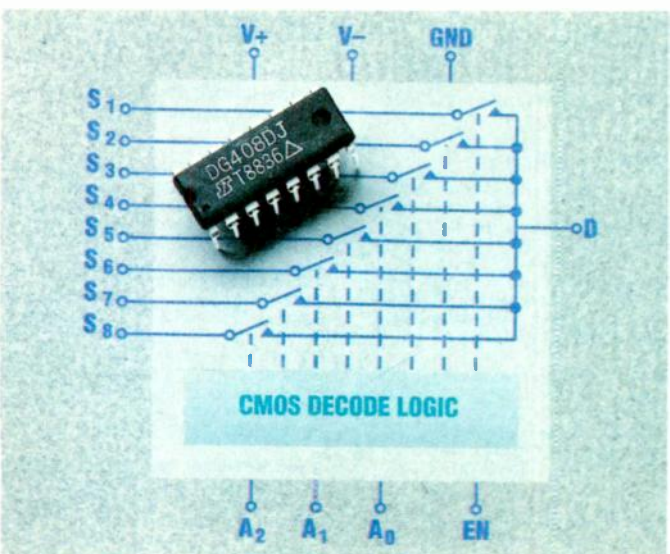
Infrared emitter. The OD-148W is an extremely small emission-area IR diode operating at 880nm. The led has a minimum output power of 8mW at 880nm and a spectral bandwidth of 80nm. Rise and fall times are around 500ns. Hero Electronics Ltd 0525-405015

1550nm emitters. Telecom introduces its 1550nm range of surface emitting leds in T046, ST and SMA packages. Power output is 20μW into 62.5/125μm GI fibre. Rise and fall times are 10ns and spectral width is 100nm. Hero Electronics Ltd 0525-405015

Carbon dioxide lasers. Two RF-excited waveguide lasers, LGK8000 and LGK8100, provide continuous output power of 5W and 25W respectively. Both have a beam purity of better than 95% and a beam diameter of less than 2mm at the exit point. Siemens Ltd 0932-752323

Programmable logic arrays

Erasable PLD. Altera Corporation has introduced the largest erasable programmable logic device, the EPM5128, built with the Altera MAX architecture. It is fabricated in 0.8μm cmos technology and has 128 macrocells, replacing over 50 TTL chips or up to 20 low-density PLDs. Propagation delay is 30ns. Ambar Cascom Ltd 0296-434141



Power semiconductors

100A, 100V fet module. Two high-current power mosfets by Ixys are available in TO-238. A 100A, 100V, 0.013Ω device and a 64A, 200V, 0.033Ω type provide the highest current ratings now obtainable says Kudos Thame. Kudos Thame Ltd 0734-351010

Mosfet power booster. The APEX PB50 power booster can form the output stage of a composite amplifier, the drive amplifier being selected by the user to optimize input performance. It can be considered as a mosfet output stage with gain. Output swing is 180Vpk-pk with ±100V supply. Microelectronics Technology Ltd 084468781

Uninterruptible power supply. The Vestale UPS combines 85% efficiency with a clean sine-wave output and is available in free-standing or rack-mounted form with ratings of 300VA to 10kVA. Units can be paralleled to give greater power output. Nighthawk Electronics Ltd 0799-40881

Power mosfet modules. Siemens has introduced a range of parallel-connected, multi-chip mosfet power modules for applications that need low switching times and simple drive circuits. All devices in the Simopac range will switch efficiently at frequencies over 200kHz. Siemens Ltd 0932-752323

PASSIVE EQUIPMENT

Passive components

Surface-mount potentiometers. The 3203 is a stable cermet device in a 3mm package. It has a power dissipation of 50mW at 70°C and withstands element voltages of up to 15V. The device survives all kinds of soldering and washing, including the dual-wave immersion process. BICC-CITEC 0793-487301

High-current filter inductors. IHM-2 inductors cover the 1μH, current rating is 17.8A and resistance is 5mΩ, while at 15 000H, the figures are 0.26A and 21.9Ω. Tolerance is 10%. Dale-ACI Components Ltd 04427-72391

Electrolytic chip capacitors. With maximum dimensions of 7.3 by 6.6 by 6.3mm, the AL CHIP-MV series of aluminium capacitors is available in values from 0.1 to 220μF over the voltage range 4-50V. Tolerance is 20% at 20°C and 120Hz. EEC Electronics Ltd 0628-810727

Direct-current shunts. Guildline Instruments Ltd have a series of current shunts which have low self-heating, low temperature coefficient, low thermal EMFs and better than 10 p.p.m. long-term stability. The 9230 series comes in the three models with values of 0.1Ω, 0.01Ω and 0.001Ω. Lyons Instruments Ltd 0992-467161

Miniature RF inductors. Two ranges of miniature axial RF inductors have values of 0.1μH to 1000μH. The EC-24 and EC-36 devices have current ratings of 60-1150mA. Tolerances of plus or minus 5%, 10% and 20% are produced. Magna Frequency Management Ltd 0223-892015

Chip filters. A range of surface-mount filters provides a method of suppressing EMI at source in digital circuits. The NFM41R chip filters are 4.5 by 1.6 by 1.0mm, have a voltage rating of 100V DC and have values in the range 22 to 22 000pF. Murata Electronics (UK) Ltd 0252-522111

Miniature ceramic filters. CFUM and CFWM are miniaturized versions of Murata's earlier resin-moulded filters for 455kHz applications. They are four and six-element units with minimum stop-band attenuations from 25dB to 35dB and 35dB to 55dB. Murata Electronics Ltd 0252-523232

Chip resistors. The CRG series of thick-film resistors by Neohm is available with resistance tolerance of 1% in the range 10Ω to 3.3MΩ. Element voltage is 200V maximum and temperature coefficient is either 100 or 200 p.p.m./°C. Surtech Interconnection Ltd 0256-51221/2/3

Connectors and cabling

Miniature circular connectors. A range of connectors by Amphenol feature reliable contact at low voltage and current, low and constant resistance and long life. The range includes screw-locking and split-shell versions. Celdis 0734-585171

Circuit protection

Hybrid mains protection. The TPU9980 series provides both primary transient protection and RFI filtering in the same enclosure. A maximum pulse input current of 20kA can be sustained. The filters give 100dB performance from 100kHz when tested in a 50Ω system at full current. EEV 0245-493493

Transient protection. TPU11 is a fast, bulkhead-mounted unit for use in 50Ω coaxial line. It is intended for EMP application and is fitted with female type N coaxial connectors at each end. EEV 0245-493493

Ferrite mains filters. A range of current-compensated chokes, the CU15/d3 and CU20/d3 families, are small, high-permeability ferrite chokes based on U15 and U20 cores with currents up to 2.5A. Philips Components Ltd

Displays

Temperature and process monitor. Rex AF-4 is an indicator with an analogue output option for connection to a computer or other equipment for data acquisition. It can also be used as a thermocouple signal converter. Two alarms may be incorporated. TC Ltd 0895-52222

Hardware

Brushless DC fan. The 125DH fan is a 48v unit, which is 120mm square by 38mm deep and is available in both ball and sleeve bearing versions. It delivers 48 litres of air per second. Accoustic noise level for the sleeve-bearing version is 46dBA at full output. Etri Fans 0403-814646

Instrumentation

Spectrum analyser. A range of spectrum analysers combine an overall level accuracy of 1dB with a displayed range of 120dB. The R3261/3361 instruments are available for frequency ranges of 9kHz-2.6GHz and 9kHz-3.6GHz, the 3361 versions also incorporating a tracking generator. Centre-frequency resolution is 1Hz. Advantest UK Ltd 01-336 1606

Microwave sweepers. Two microwave sweep generators from Boonton are claimed to have the highest spectral purity in instruments of their type. Models 20900 and 2100 cover 2 to 20GHz and provide full-range sweeps, sweeps from entered F1 to F2 and symmetrical sweeps about a given frequency. Aspen Electronics Ltd 01-868 1311

Surge and transient probe. For accurate monitoring of high-voltage transients up to 6kV, the PK 1001D has low EMI sensitivity, needs no earth at the probe tip and no compensation adjustment. Eaton Ltd 0734-794717

Digital multimeter. Series 50 multimeters have a full sealed, separately enclosed battery and fuse compartment, which is accessible only when test leads are detached. Features include resolution up to 5000 counts and an LCD bargraph display. ITT Instruments 0753-824131

Digital temperature meter. The LABCAL is based on a 16 bit microprocessor and is digitally configured for Pt 100 sensors and all major thermocouples. Cold-junction compensation is incorporated. Resolution is 0.01°C for thermocouples. Labfacility Ltd 01-943 5331

Communications testers. The Componedex Fakerscope is an active and passive RS232 tester/analyser, offering synchronous and asynchronous operation. It has a four-line by 20 character LCD with a tri-state breakout box for data review and provides terminal emulation. STC Instrument Services Ltd 0279 641641

250MHz probes. Two spring-contact probes allow board testing in bed-of-nails fixtures at spacings of 50mils. P6515 and P6517 possess 1MΩ and 4pF input and 50Ω output impedance. Tektronix UK Ltd 06284-6000

Power supplies

Universal-input SMPS. A 50W switched-mode power supply accepts any input voltage between 85 and 264V AC without any adjustment and works down to zero load with no loss of output regulation. The Computer Products Power Conversion Ltd XL50-7601 provides +5V at 7A, +12V at 2.5A and −12V at 0.7A. Amplicon Electronics Ltd 0273-608331

Single-output SMPS. Todd Products SC series of switchers have output power ratings of 150W and output current ratings of up to 100A. Voltages are 5V, 12V, 24V, 28V and 48V, each being adjustable. Amplicon Electronics Ltd 0273-608331

Power supplies. The STK series of cased, switched-mode supplies are rated from 10W to 100W and, with inputs of 85V AC to 264V AC or 240V DC, provide single, dual or triple outputs in combinations of 5V, 12V, 15V and 24V. Calex Electronics Ltd 0525-373178

DC-DC converters. A 5W DC-DC converter range, the PT 4900 series by Powertrade GmbH, has a 2:1 input voltage range and is packaged in the standard 51 by 51 by 9.6mm module. Units are available with 9-18V, 18-36V and 36-72V inputs, each range has three single-output and two dual-output versions. Gresham Powerdyne Ltd 0722-413080

Radio communications products

High-power termination. KDI/Triangle T1100N is a 0 to 800MHz convection-cooled termination rated at 100W. It can handle up to 150W when force-cooled at 100CFM from −55°C to +25°C. Maximum VSWR is 1.3:1 up to 800MHz. Anglia Microwaves Ltd 0277-630000

RF switching matrices. Two switching matrices from K and L Microwave handle signals from zero to 18GHz. Model 110 is in 1 by 18, 1 by 6, 1 by 12 or 1 by 21 configurations, with isolation of better than 60dB and insertion loss of 0.5dB. Model 120 is a 10 by 10 matrix. Aspen Electronics Ltd 01-868 1311

Switches and relays

Surface-mount switch. Series 224 SMD is for surface mounting, its lower half being mounted on the PCB, either manually or automatically, and the whole board cleaned in the normal way. The top half is then snapped into place without the need for tools or worry about orientation. ITW Switches 0705-694971

Transducers and sensors

Low-profile sounder. The AT-124 sounder is 4.5mm in height, wave solderable and PCB mounted. Sound pressure level at 30cm is 88dBA at 60kHz with a current consumption of 2.5mA. Alan Butcher Components 0258 840011

Local cell. Accuracy of the JP range of cells is better than 0.07%, with a repeatability of 0.05%. Output is 150mV at an excitation of 5V. The cells measure up to 2000 pounds in eight calibrated ranges and withstand 50% overload. Dimensions are 39.7mm(H) by 28.6mm(W) by 18.2mm. Control Transducers 0234 217704

COMPUTER

General microprocessors

16 bit ralu. From Logic Devices is a 16 bit register-file ALU, which has pin and software compatibility with the Am29C101. The L29C101 uses cmos technology to provide a 35ns clock period (28Mips) and a supply current requirement of 60mA at 10MHz. Abacus Electronics Ltd 0635 36222

Microcontroller. The Siemens 80515/80535 is fabricated in n-channel, silicon-gate MYMOS and is a stand-alone single-chip device based on SAB8041 architecture. It incorporates eight analogue/digital channels. ITT Multicomponents Ltd 0753 824212

Z84C00 CPU. The Zilog Z84C00 is a pin compatible version of the Z8400 CPU. Operating at 4, 6 or 8 MHz, it needs only 15µA for operation and less than 10µA on standby. Microlog Ltd 04862 29551

Microcomputer with LDC driver. The eight-bit MC68HC05L6 has an on-chip LCD driver and has an on-chip oscillator. CPU 6Kbyte of rom, 176byte of ram, a synchronous serial peripheral interface, a 16 bit timer and an audio tone generator. Motorola Ltd

Interfaces

Data acquisition front end. AD1362 combines an input multiplexer, differential amplifier, sample/hold amplifier, output buffer and control logic in a 32 pin dil package. Users can select either sixteen single-ended input channels or eight differential ones. Analog Devices 0932-232222

Memory chips

Static rams. Three standard-cell static rams in 2µm double-metal cmos are available as separate cell elements from AMS. Configured as 128 by four bits (RA47085), 512 by four bits (RA49325) and 1K by four bits (RA80645) the devices need 4.5V to 5.5V, providing a cycle time of 26.3ns or 46ns with 1pF load. Austria Mikro Systeme International Ltd 0793-37852

2Mbit cmos static ram. The WS-256K8-120 from White Technology is claimed to be the first in a 32 pin dip. It operates on 5V and is hermetically sealed. All control logic decoding and I/O circuitry is in the one package. Bowmar Instrument Ltd 0932-851341

High-speed static ram. Siemens type GxB 100474A has a 1K by 4 organization and a 3.5ns access time. It is claimed to be the only device available which can operate in the conventional mode and in the synchronous mode. It is compatible with ECL devices. Siemens Ltd 0932 752323

Task oriented processors

Single chip for DSP. The PDSP16488 is a high-speed two-dimensional convolver for image and digital processing. The chip is claimed to provide the highest pixel rate available. The multipliers can produce 64 valid results in a single input pixel period, providing a computational rate of more than 10^9 operations per second. Plessey Semiconductors 0793-36251

Video compression/expansion processor. The AM95C71 is a cmos processor which compresses and expands binary image data using the international standard CCITT Group 3 and 4 algorithms. It provides the means of reducing the amount of data stored in memory or transmitted on a network and expanding it when necessary. Rapid Silicon 0494-442266

Programmable controller. TPC8500 offers up to 64 I/O lines or a mixture with up to 16 analogue I/O. Other features include 32K of user memory, 16K of data memory in a multi-tasking format with full maths and real-time clock. The controller comprises a processor module which is fitted with a range of associated I/O cards. Tempatron Ltd 0734 596161

Vibration sensors. Trolex has the GP series of sensors which are particularly suitable for monitoring machine vibration in the range 5 to 10kHz, with a linearity of better than 1%. The sensors can detect accelerations from 0 to 7g R.M.S. Trolex Ltd 061-483 1435

Data communications products

Smart modem chip. Rockwell's R96MFX IC can transmit half duplex at up to 9600bit/s. It is intended for Groups 2 and 3 fax machines. The chip conforms to V.29, V.27*ter*, T.30, V.21 Ch2, T.4 and T.3 standards. It uses only 0.5W. Abacus Electronics Ltd 0635-36222

Protocol converter. A high-speed parallel/serial/parallel protocol converter with an internal 8K or 32K buffer supports all common data rates and serial interface protocols from 300 to 38 000 baud and offers data rates of 40 000byte/s on its parallel interface. Ringdale Peripherals 0903-213131

Mass storage devices

SCSI disc controller. The CL-SH250 made by Cirrus Logic is a VLSI component providing the functions needed to build a SCSI winchester controller. It contains an advanced winchester disc formatter, a dual-port buffer memory manager and hardware support including 48mA open-drain drivers for the Small Computer Systems Interface. Amega Electronics Ltd 0256-843166

Disc drive sub-system. The Legend data-storage sub-system combines the reliability of winchester with the flexibility of a removable cartridge. The SQ500 allows users to remove data for more secure storage, and a formatted capacity of 44Mbyte permits large independent data bases in shared systems. HTEC Ltd 0703-581555

Hard card. The 8450 hard card for the IBM PC/XT/AT and compatibles provides 40Mbyte of expansion memory. It takes the form of a 3.5 inch hard disc on a card. Ideal Hardware Ltd 01-390 3090

SCSI and floppy controller. FSC1 is a multiple disc controller module which can control up to seven SCSI devices and up to four floppy discs. It offers a versatile interface between the VMEbus and a variety of disc drives. The single-height Eurocard includes on-board 64Kbyte ram and MC68540 DMA controller. Syntel Microsystems Ltd 0484-535101/2/3

Disc drive testers. The telematic range of Microtest floppy disc drive testers for the repair, calibration and diagnosis of all types of drive is used in conjunction with a standard PC or compatible. TAP Systems Ltd 0276-685761

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If any of this appeals, then I would like to discuss the possibilities with you. Please contact Frank Ogden, Editor, on 01-661 3128. I shall then be able to give you an unbiased assessment of your potential as an E&WW reviewer.

ENTER 26 ON REPLY CARD

Inside S-VHS

VHS video recorders were introduced to the UK just over a decade ago. Now the format has been upgraded to provide pictures which approach broadcast quality.

PETER H. DOLMAN

The Video Home System (VHS), developed by JVC, has become the leading domestic VCR format. It provides reasonable performance and meets the consumer's conflicting requirements of flexibility, affordability and reliability. During its lifetime it has been extended and refined, without compromising compatibility, to include such features as long play, hi-fi sound and "HQ" picture enhancement. Machines have evolved which are more user friendly, employing wireless remote control, tape index systems and bar-code timer programming.

In the price-conscious consumer electronics industry, the constraints of affordable technology and those of tape head manufacture were fundamental in creating the original VHS specification. Now progress in these key areas has enabled JVC to develop 'Super-VHS' (S-VHS), which has the potential to extend picture display quality well beyond VHS's limitations.

LIMITATIONS OF VHS

The main factors limiting VHS picture quality can be summarized as follows;

- **Horizontal resolution is limited to around 240 lines as a consequence of restricting the Y bandwidth. A 1MHz video signal yields 80 lines horizontal resolution. However, colour receivers degrade off-air broadcast signals from a possible 440 lines down to some 350 lines, because of a notch in the receiver's luminance response centred on 4.433MHz. This is necessary to prevent the appearance of dot patterning effects (cross luminance) on coloured areas of the display. Furthermore, the pitch of the shadowmask CRT limits resolution.**
- **The small deviation range of the FM carrier limits signal-to-noise ratio and impairs the reproduction of subtle graduations of grey-scale values.**
- **A marked overlap of luminance and chrominance signals occurs around the 1MHz region, causing undesirable crosstalk effects (Fig. 2).**

VHS PRINCIPLES

To make efficient use of the available spectrum, the luminance (Y) and chrominance (C) components of the video signal to be recorded are separated by band-pass filtering. The Y signal cannot be directly recorded because its frequency range of 20Hz-5.5MHz, occupying a span of some 19 octaves, exceeds the maximum of 10 octaves possible from the magnetic medium **(Fig.1)**.

Octave compression provides the solution. The Y signal is frequency-modulated on to an HF carrier, the deviation limits now determining the octave range. The VHS specification is 3.8MHz for sync-tip, 4.8MHz for peak white. Sidebands of the replayed luminance signal extend from around 1.4MHz to 5.5MHz, indicating compression to less than two octaves (**Fig.2**).

The use of FM ensures the best possible signal-to-noise ratio, since the tape is driven toward saturation for all luminance signal values. In addition, no bias is necessary to offset the non-linearity of the tape transfer characteristic. System ruggedness is good because effects such as poor head-to-tape contact, tape dropouts and head wear primarily cause amplitude disturbances rather than frequency variations.

To recover luminance successfully, the significant sidebands (those greater than 1.5% of unmodulated carrier amplitude) must be recorded by the system. Figure 2 indicates that the FM carrier is, by necessity, close to the highest modulating frequency. The Y signal is, therefore, tailored by a low-pass filter with a roll-off at 3.5MHz of − 20dB; this ensures that components produced in the lower sideband do not, by 'mirroring' at 0Hz, re-appear as folded sidebands in the wanted spectrum. This would give rise to moiré patterning on replay.

The penalty for this 'narrow band' FM technique is degradation of noise performance in comparison to that of wider band systems. The loss of information in the upper sideband reduces the signal-to-noise ratio at HF and must be compensated for by pre-emphasizing the Y signal prior to driving the modulator **(Fig.3)**. On replay, de-emphasis is applied.

The increase in amplitude of the Y signal HF component following pre-emphasis must be limited to prevent over-deviation of the modulator. Dark and white clip circuits restrict the drive signal excursions to 40% and 90% respectively (Fig.2).

The chroma component of the composite video input is extracted by selective filtering centred on 4.43361875MHz. It is recorded as a QAM signal, down-converted to 626.9kHz and occupies ±500kHz bandwidth. This represents less than four octaves and it can therefore be recorded directly. However, a

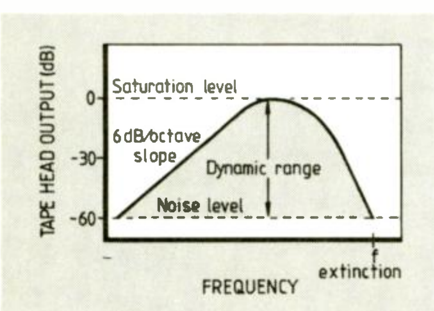


Fig.1. Tape replay characteristic. In video recording, the medium can pass a frequency range of 10 octaves.

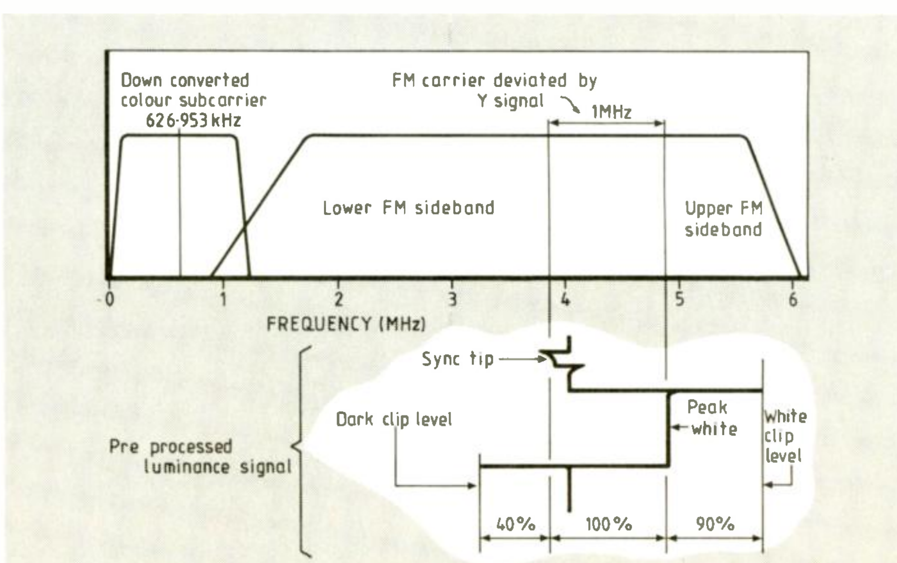


Fig.2. VHS recording spectrum: note the "colour under" arrangement.

source of AC bias is required to overcome the tape transfer non-linearity. Bias is conveniently provided by the FM luminance signal, with which the chroma signal is matrixed prior to its application to the recording heads. Since amplitude modulation is involved, good head-to-tape contact is essential to achieve a reasonable chroma signal-to-noise ratio during replay.

S-VHS

Advances in the field of video head and recording tape manufacture have made possible significant improvements over the VHS specification. In domestic television systems, the emphasis is now very much on improved picture and sound quality. Anticipating an increase in consumer keenness for better technical quality, JVC has developed Super-VHS, the PAL version of which was announced in January 1988.

S-VHS enables a wider luminance signal bandwith to be recorded through repositioning the FM carrier. As a result, horizontal resolution is increased to 400 lines **(Fig.4).** The revised FM frequencies are 5.4MHz corresponding to sync-tip, 7.0MHz for peak white. Extended white and dark clip levels are 110% and 70% respectively and the overall pre-emphasis characteristic is changed to reduce the adverse effect on noise performance of broadening the recording spectrum.

HEAD AND TAPE DEVELOPMENT

To maintain compatibility with standard VHS, linear tape speed, writing speed and track pitch remain unaltered. Thus for S-VHS an increase in recording density takes place. Newly developed amorphous metal video heads are employed to record wavelengths down to 0.7μm. By the use of laser technology a head gap of 0.15μm is possible. The laminated construction technique **(Fig.5)** has the advantage of improved efficiency at high frequencies, through a reduction in eddy current losses. In addition, noise generated by head-to-tape contact is reduced by 2-3dB over conventional single-crystal ferrite heads by low-friction design of both head and lower drum assemblies. Friction noise becomes significant above 5MHz, and particular care must be taken to minimize it.

The increased recording density places stringent demands on the recording tape specification. Although a move to metal tapes (like those used in the Sony 8mm system) may seem logical, JVC decided to stay with a more familiar cobalt gamma ferric oxide coating to secure compatibility between the two systems and their tape families. Accordingly, for S-VHS tapes, particle size is reduced to decrease modulation noise and achieve the required short wavelength recording characteristics. However, the effect of self-demagnetization (caused by the pole proximity of the individual domains) becomes a significant factor. The solution is to employ closely controlled production techniques which result in an increased area of the tape B-H curve **(Fig.6)**.

The increase in the loop broadness indicates greater coercivity of the order of 30%, reducing self-erasure and thus improving the ability to store short wavelengths in the medium. Carrier-to noise (c/n) ratio is improved by increasing the remanent point to 175mT. C/n ratio is of particular concern in the wider bandwidth S-VHS system: signal disturbances which would be considered unimportant for VHS now become significant. Spacing loss between the tape and rotary heads has to be minimized; higher consistency and smoothness of the magnetic layer, together with an ultra-flat base film and improved tape handling within the cassette are areas where attention to detail can yield substantial benefits. This applies not only to luminance but also to the AM chroma signal, particularly when highly saturated colours are to be displayed.

The use of anti-static material for the cassette shell is desirable because dust and dirt are maior causes of drop-outs.

Comparison of the two tapes of Fig.6 indicates an improvement in RF output and luminance of 1dB, whilst chroma signal-to-noise is raised by 1.5dB and output by 2dB.

Auto-selection of VHS/S-VHS recording mode is made possible by an ident hole in the base of the cassette body, which aligns with a sensing switch on the VCR mechanism. Manual override of this feature is possible should the user wish to record on S-VHS tape in the VHS mode; for example, where this tape is subsequently to be transferred to a VHS machine for replay.

At this point it is worth considering the question of making recordings with a standard VHS VCR using S-VHS tape. S-VHS tapes *can* be used in this situation, although erasure of previous recordings may not be entirely satisfactory on some machines because of the higher coercivity level. And an SE-180 cassette costs around £13.80, compared to £5.30 for a high grade E180 VHS tape

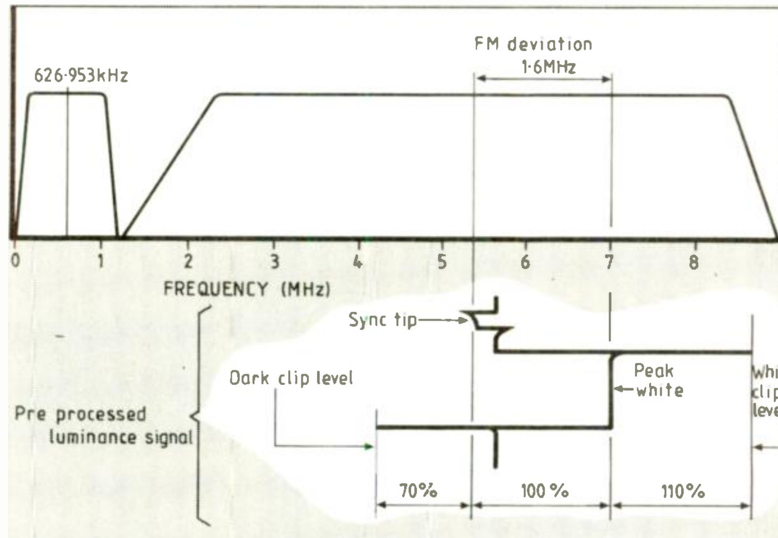


Fig.4. S-VHS recording spectrum. Horizontal resolution extends to 400 lines.

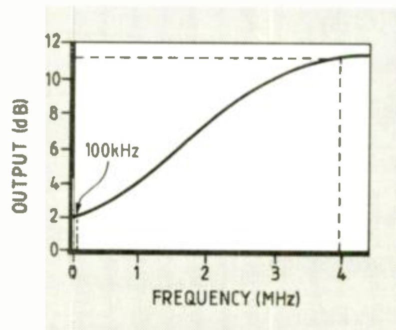


Fig.3. Pre-emphasis characteristic of the luminance signal (VHS).

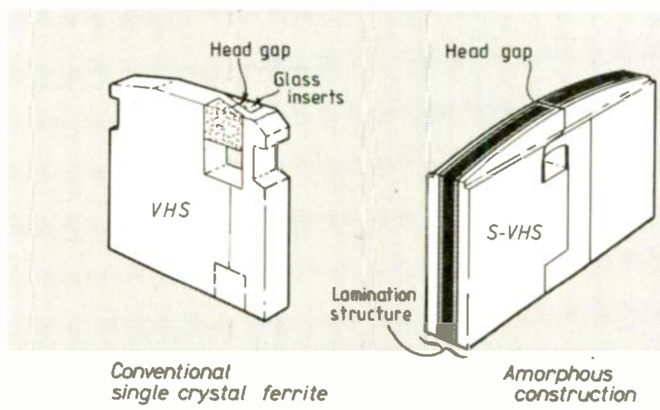
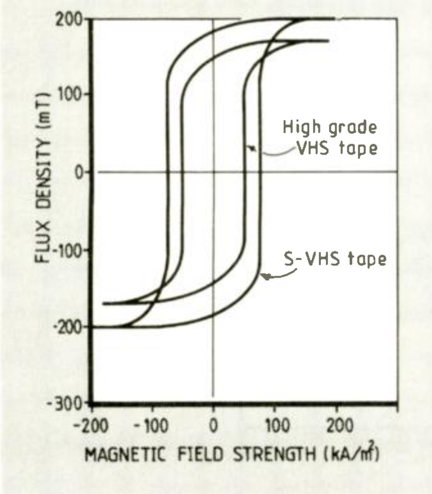


Fig.5. Video head construction. Improved head design has been an important factor in creating the S-VHS format.



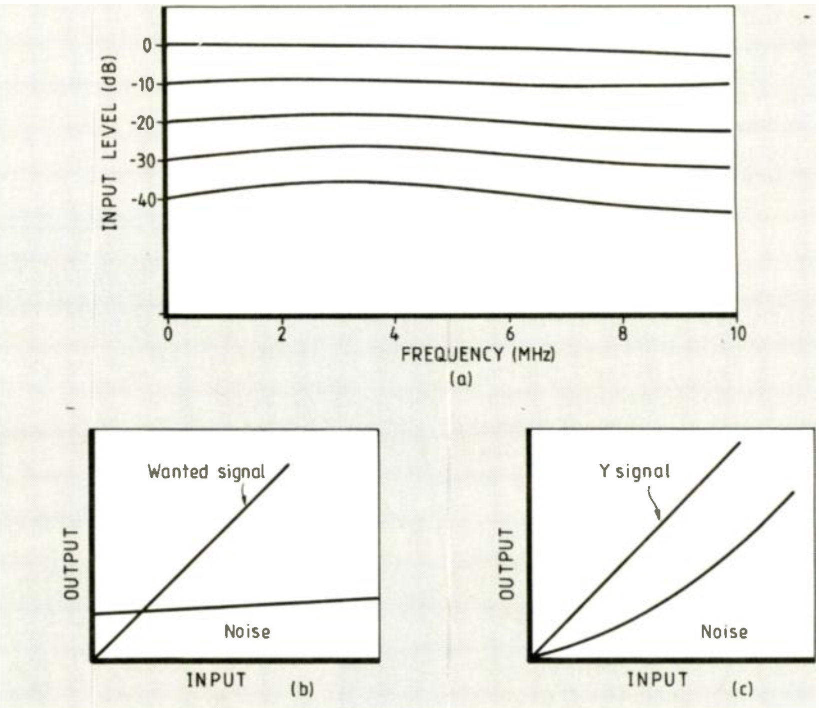


Fig.6. Magnetic properties of VHS and S-VHS tapes. For compatibility, S-VHS uses a similar formulation but with smaller particle size.

Fig.7. On record, sub-emphasis is added to the luminance signal in the 2-3MHz range to overcome noise.

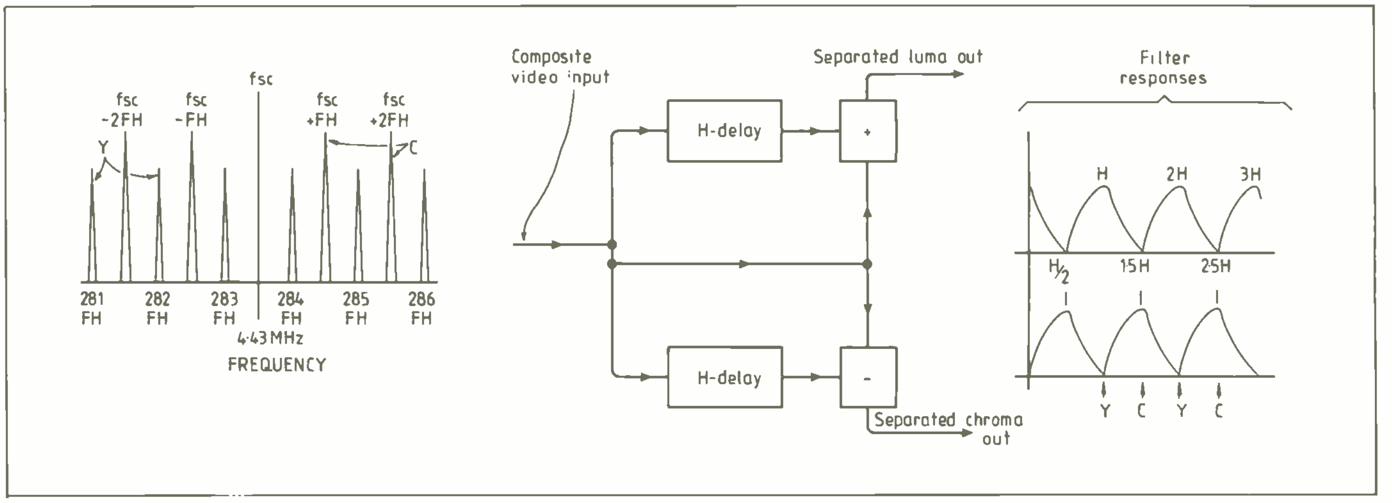


Fig.8. Left: static chrominance and luminance clusters in the composite video signal. The two can be separated by comb filtering (right).

SIGNAL PROCESSING

From Fig.4 it can be seen that FM deviation has been increased to 1.6 times that of VHS. This produces a significant improvement in noise performance and will enable the home movie enthusiast to produce edited recordings far superior – at least in technical terms – to that hitherto possible with any domestic system. A further important advantage is that a more gentle graduation of grey-scale tones is achieved.

The higher frequencies involved in S-VHS make for improved immunity to adjacent-track luminance crosstalk, owing to the frequency-dependent action of the familiar 'offset azimuth' technique employed in domestic VCRs.

In addition to the standard pre-and de-emphasis stages employed in VHS record/replay, S-VHS features sub-emphasis, designed to minimize the effect of higher noise levels inherent in a higher-resolution system. The technique provides a lift to the recorded luminance band in the lower frequency region of 2-3MHz **(Fig.7)**. The degree of lift is dependent on signal level, for a given frequency. The characteristic is applied prior to the standard VHS pre-emphasis during record. Complementary de-emphasis is carried out on replay.

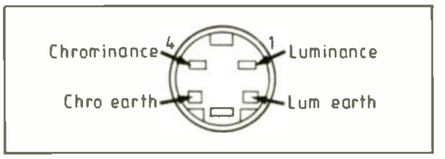


Fig.9. Four-pin S-socket for portable S-VHS units.

Figure 4 also shows an improvement in Y/C separation in the region of 1.2MHz. For S-VHS, the HF luminance sidebands contained in this region should be better than 20dB below chrominance level. Not only does this overcome the undesirable crosstalk effects I mentioned in discussing the off-tape spectrum of the VHS signal, but it lays the foundation for a recording system in which the two signal components merit separate processing within the VCR, making the elimination of cross-colour quite achievable.

COMPONENT CODING

The broadcast television signal contains Y and C components which are grouped together by frequency-division multiplex on to a common carrier. For VHS purposes, separation of the two can be achieved by simple ceramic filters.

With S-VHS and its wider luminance bandwidth capability, a more comprehensive technique is necessary: comb filtering. Examination of the composite signal spectrum reveals that energy relating to the Y and C components is distributed in clusters centred on harmonics of the horizontal scanning frequency. The choice of chroma subcarrier frequency is such that the two elements interleave, thus making efficient use of the available bandwidth whilst minimizing mutual interference (**Fig.8**).

With delay-line matrix and summing arrangement (**Fig.8**), the wanted spectral components can be separated; unwanted components are cancelled. For PAL, a quarter-line offset relationship exists between luminance and chrominance. The practical comb filter arrangement employs 4H glass delay lines.

Setting up the filter is critical, separation being dependent on accurate balancing of the signal paths. A typical S-VHS machine has six variable resistors and two inductors in this section.

The wider-bandwidth Y signal places extra demands on the design of the preceding tuner and IF/demodulator stages in the receiver section. In cases where the source of video is deficient in HF, the comb filter may not provide an enhanced resolution, but instead will increase the Y noise level. Manufacturers therefore provide 'comb off' or 'edit' switches on their S-VHS VCRs, which insert an early roll-off of the Y response, to provide an improvement in noise performance at the expense of resolution.

The full recording potential of S-VHS can be achieved only with a source which offers the individual Y and C signals in their original, full-bandwidth form. Such a system will offer horizontal resolution in excess of 400 lines, free from cross-colour and cross-luminance effects. . . a specification which exceeds that of current UK broadcast transmissions when displayed on conventional domestic receivers.

S-VHS camcorders with their internally-derived Y and C signals represent the ultimate record/replay system at present. For external connection, the 'S-socket' (**Fig.9**) is provided; this is also featured on table model S-VHS VCRs to permit high grade dubbing between machines, and to provide a means of recording from alternative component-coded sources, e.g. MAC signals.

An alternative means of connecting separate Y/C signals has been made possible by a modification to the standard Euroconnector pin assignment. Pin 15, normally red channel input, may now be designated for separate chrominance. Similarly, pins 19 or 20, currently composite video out/in respectively, may be used for separate luminance out/in.

Advantages of this method are that existing leads may be used and that the common connector provides not only Y/C but also audio signals. However, some confusion can be expected by the effect of no colour when playing Y/C signals via a receiver Euroconnector that conforms to the original 1984 SCART standard; a cure would be to select composite output from the S-VHS VCR.

RECORD/REPLAY OPTIMIZATION

Consider an S-VHS machine, set to record in the S-mode from any composite video source. After separation of the video into Y and C, some degree of residual 4.43MHz chroma can be expected in the Y signal because of filtering limitations. This would be recorded on tape and would produce unwanted sidebands in the 1MHz region on replay. To minimize the crosstalk effects which would be apparent under these conditions, a trap centred on 1.2MHz is automatically switched into circuit following the head amplifier to ensure separation of the recovered Y and C components.

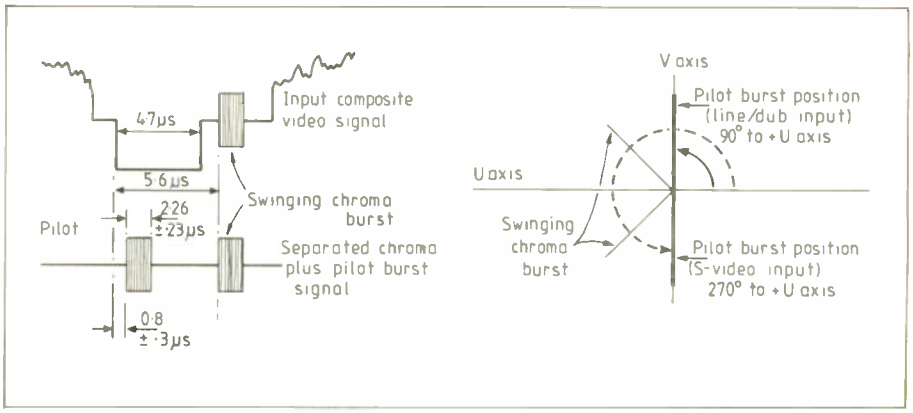


Fig.10. A pilot burst is inserted in the record signal to identify the video source. Its purpose is to reduce Y-C crosstalk by switching in a notch filter when signals of composite origin are being replayed.

Since resolution and HF phase will be unnecessarily compromised should the trap operate on signals previously recorded via the S-socket, or on pre-recorded tapes which were made from a true Y/C source, a method of signal source recognition is used to enable the trap (**Fig.10a**, left).

The pilot burst, consisting of 10 cycles at 4.43MHz, is gated into the record chroma signal prior to down-conversion. Its phase angle relative to that of the chroma U-axis is arranged to provide the necessary source ident during subsequent replay (**Fig.10b**, right). The pilot burst is not passed through the replay chain, but is gated out of the replay chroma signal to control the filtering action. In addition it may be used as a reference for jitter compensation, as an alternative to the off-tape swinging chroma burst signal.

INTERCHANGEABILITY OF FORMATS

Like VHS, S-VHS can be operated in the standard play mode (tape speed 23.4mm/s) or in long play mode (11.7mm/s). Tapes are available in C cassettes as well as the normal size.

A single European format is proposed for the S-VHS recording system. This "Eurosystem" means that S-VHS machines of the future will convert SECAM-encoded signals into the same on-tape signals as those for the PAL system. On replay, a choice of PAL or SECAM outputs will be available from the same cassette.

S-VHS tapes can be used for record and replay in VHS machines. Standard VHS recordings can be replayed on a S-VHS machine by automatic detection within, which makes the necessary changes in demodulation and frequency characteristics. VHS recordings can be made on an S-VHS machine if required, either by deliberate selection of this mode by the user, or by automatic sensing of the presence of a VHS cassette; but it is not possible to play back an S-VHS recording on a VHS machine.

Fresnel antenna

Satellite receiving antennas costing as little as £5 could become a reality soon through a development being pioneered by a British company, Mawzones Ltd. Not only is the antenna cheap to make, it is flat too: a version designed for receiving the Astra direct broadcast satellite is printed on a window-blind and can even be rolled up when not in use.

The Mawzones antenna consists of concentric Fresnel rings screen-printed on a transparent plastics sheet. These can be of silver for a reflective antenna, or of graphite for a transmissive antenna; and if the rings are elliptical rather than circular, they can focus signals arriving at an angle to the zone plate and an offset feed may be used.

Mike Wright of Mawzones demonstrates two reflective antennas: the one on the left has a painted finish.

Antennas can be flush-mounted on walls, roofs or windows, and in the latter case the feed-horn and head amplifier can be sited indoors. Typical positioning tolerance for DBS reception is ±5°, which would mean that for a given satellite the same zone plate could be used at locations within 300 miles of the optimum position. At other sites, or for other mounting positions, an alternative pattern could be selected from a range of masters.

Plessey and the Economic League

To many, the Economic League is an unsavoury organization. Founded in 1919 by the ex-chief of the Naval Intelligence Department. Its job is to supply tit-bits of information to employers about potential employees during the recruitment stage. From the employer's viewpoint the object is simple: the League helps them to spot troublemakers.

Since MPs are nature's troublemakers, the League's activities have drawn continual fire. A motion before Parliament, supported by over 90 MPs, "condemns those secret, back-stabbing operations of the Economic League which blacklist innocent people without their knowledge, deprive them of the right to reply, and damage their job prospects; and calls upon the Government to outlaw all such activities".

Such political activity seems to have paid off; Max Madden MP has amended the motion to refer to a letter from Stephen R. Wallis, Managing Director of Plessey PLC, dated January 26, 1989, "announcing that all Plessey Company sites have been advised to discontinue using the services of the Economic League". One wonders whether other electronics companies have the courage to make a similar public statement.

Mum's the word!

Many readers of *Electronics & Wireless World* are trusted to work in the sensitive areas of defence electronics, and are aware that a breach of trust could be very damaging to national security. But suppose an instruction is given to you by your employer, with the approval of Government, that results in secrets being given away? What would you do?

This was the problem facing one senior research scientist who was working for Plessey in January 1977. He discovered that Lucas Aerospace was to supply a digital fuel control system for a Soviet jet engine, and Plessey a variable-geometry jet nozzle. Although these were ostensibly for the ill-fated Russian civil aircraft, the "Concordski", the scientist realised that the same technology would double the range and radius of action of the Soviet backfire bomber so that it could strike at the heart of the United States.

Consequently, the scientist leaked classified information to Winston Churchill MP, whose famous grandfather received many such leaks in the 1930s. Armed with this information, Churchill ensured that the £10 million contract was cancelled.

According to Churchill, if that happened in future, all the thanks the scientist would receive would be a criminal record. During a debate on the new Official Secrets Bill, he complained that the Bill's attempt to restrict leaks of official papers actually equated Government interest with the national interest. Thus, any future research scientist could not claim that the disclosure, although damaging to the Government of the day, was vital to the good of the nation.

So now you know, whatever you thought you would have done, don't!

Reliability of defence equipment

A stinging report from the National Audit Office (NAO)[1] complained that the Ministry of Defence does not pay sufficient attention to the reliability and maintainability (R&M) of defence equipment. Such is the scale of neglect that, according to the NAO, there could be savings of some £1000M a year.

The report does not mince words. It complains that "R&M has consistently been sacrificed to performance, and initial purchase cost", that for the most part there was "a lack of commitment in this area, ineffective management, inadequate resources, a need for better information and a scope for tighter contracting" and that "there must be a will to delay or halt projects where R&M has not been fully considered". There was even a lack of information as to when or if defects occurred in equipment, which equipment had faults, or even how long equipment was used (important for scheduling routine maintenance).

This, according to the report, has led to specific problems. For example, up to 50% of the RAF's fast jet fleet is not available for training because of servicing, and reliability modifications to jets account for an additional 70% to the basic unit costs. One reason why the Nimrod airborne early warning system was cancelled was that R&M would be a further large expense.

The NAO hints that a major problem is Whitehall itself. There was "a lack of sufficient top-level commitment by the Department and industry to the rigorous implementation of agreed R&M principles at project level" and that the MOD "may plan minimal R&M programmes in order to reduce costs". Out of 30 000 staff and an annual budget of £900M only 30 full time staff work in areas covered by the report.

The report is very enthusiastic about the Pentagon's approach, which calls for R&M incentives and warranties to be an integral part of procurement policy. Clearly, the auditors think that the same should improve the value for money obtained for the taxpayer, the next time the MoD signs a major contract.

Reference

1. National Audit Office, Report by the Comptroller and Auditor General; Ministry of Defence: Reliability and Maintainability of Defence Equipment, £4.90, HC 173.

Marconi and fraud

Dale Campbell-Savours, a Labour MP who has a formidable reputation for finding the dirt that surrounds the misuse of public money, has his teeth into Marconi. It appears that it was his activity in Parliament that forced the hand of the Director of Public Prosecutions (DPP) to prefer charges after 24 months of silent investigation.

Five days before the DPP announced the prosecution of four senior Marconi employees, the MP had implied that he would 'name' the men under the cloak of Parliamentary privilege if nothing happened. Also accusing the DPP of using the Plessey/General Electric Company takeover battle as an excuse for delaying large scale prosecutions, (GEC is the parent company of Marconi), he said that the takeover bid conveniently kicked an embarrassing issue into touch.

Now the DPP has begun the legal process, a different muzzle applies. Parliamentary procedure forbids many activities that relate to matters before the Courts.

Notes on the House are by Chris Pounder.

CIRCUIT IDEAS

Multi-channel data logger

This circuit was designed to provide portable data-logging in medical research. It has eight analogue channels each sampled at 100Hz and can capture about a minute's worth of data from each channel. When its memory is full, the logger is connected to a microcomputer i/o port so that its data can be processed and stored.

Input limits are 0V and 5V. At power up, the counters are reset and the ram is held in read mode. On pressing of the start button, a bistable device removes reset from the address counters and enables the 550Hz system clock. At the clock's falling edge, $\overline{CS}$ and $\overline{RD}$ of the a-to-d converter are pulled low and data on channel one is converted.

On completion of the conversion, the converter's interrupt line goes low causing one of the monostable ICs to produce a 300µs chip-select pulse at the ram; at this point, data is written into the ram. At the end of the chip-select pulse, the second monostable IC outputs a 10µs pulse to increment the address counters. Now the system waits for a new clock pulse.

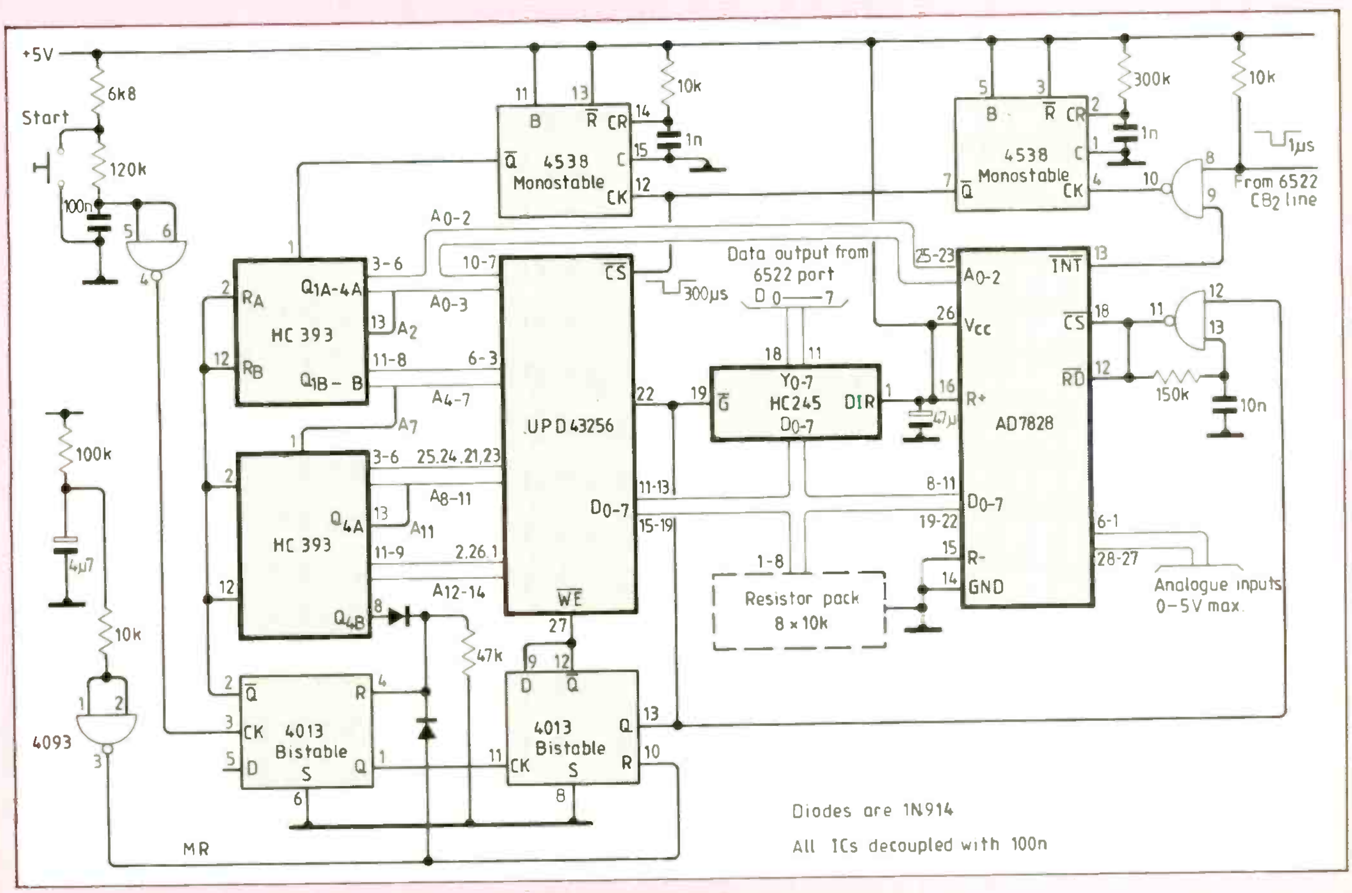
Converter channel sequencing is done by the three lowest address lines. When the top of the address range is reached, the most-significant line of the counters goes high to reset the counters via the bistable IC. Both the clock and the converter continue to operate, which means that the last byte in the ram is unusable; in practice this should not be much of a problem.

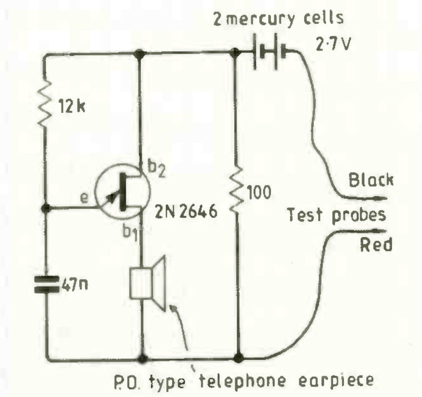
Pushing the start button again disables the clock and the converter. Both monostable multivibrators can now only be triggered by the application of an external pulse.

At this stage, data can be retrieved from the ram. Eight data i/o lines and one control line from a microcomputer connect to the logger. The control line, for example CB_2 of a BBC microcomputer's 6522 interface adapator, is pulled low to trigger the monostable IC pulse. Data is now held on the output bus for the duration of the 300µs pulse so that it can be read by the computer. At the end of the pulse, the second multivibrator triggers to increment the address counters.

Since the data is only available for 300µs, a machine-code program will probably be required to read it.

A.G. Birkett
London





Improved continuity tester

At supply voltages less than about 3V, frequency of a unijunction transistor oscillator becomes highly supply-voltage dependent. This property can be used to make a continuity tester whose audible output clearly indicates the resistance difference between a short circuit and a cold-filament lamp.

Oscillator frequency and amplitude decrease with increasing resistance: there is no output for probe resistances higher than about 100Ω.

P.A. Dowie
Kidderminster
Worcestershire

CIRCUIT IDEAS

1Mbyte address bus for Z80

Traditional methods for extending the address space of eight-bit processors rely on latches to switch a memory device into or out of a particular area of address space.

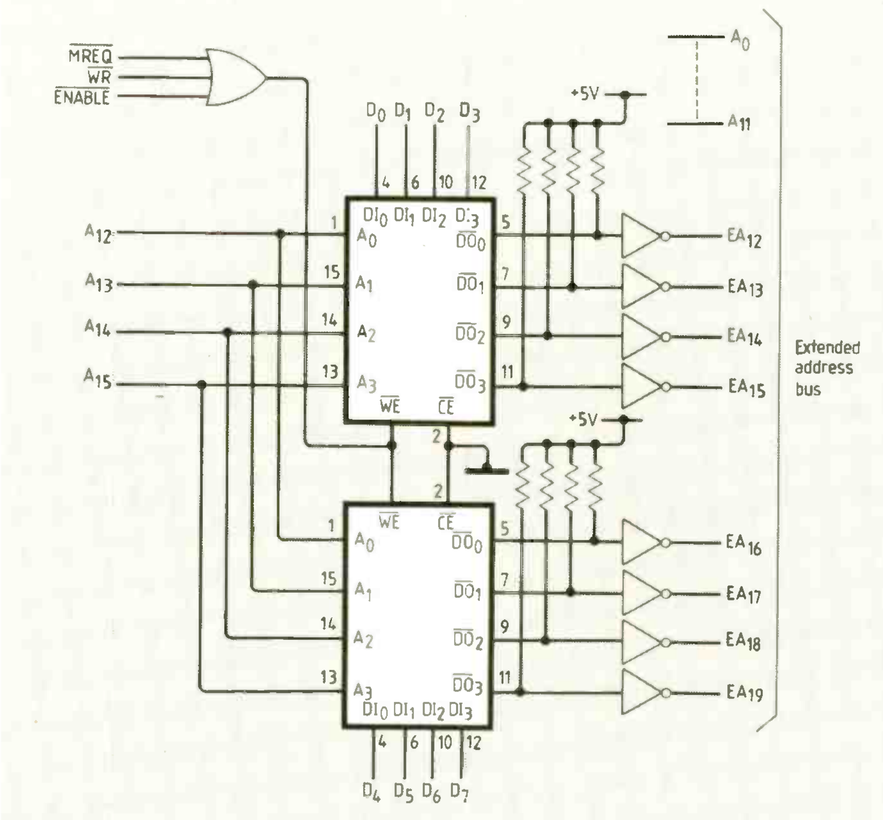
My approach divides the Z80 address space into blocks of 4Kbyte and any 16 of these blocks from a selection of 255 can be selected for the Z80 address space. This allows areas of memory to be repositioned so that, for example, screen images can be switched in and out of a memory-mapped VDU.

Two ram ICs work as one 16-by-8bit ram which is used as a page table by the top four bits of the Z80 address bus. The 8bit page address is written to this table by simply loading it into any part of the 4Kbyte block using LD instructions.

To use the paged ram, it must be possible to disable the circuit. This is done by setting a flag bit connected to ENABLE. Any bit of an output port could be used as the flag.

There should be no problems when crossing page boundaries since the rams are TTL devices with 25ns access times: if 7489s are used, their outputs will need pull-up resistors.

S.R. Monk
Sileby, Leicester



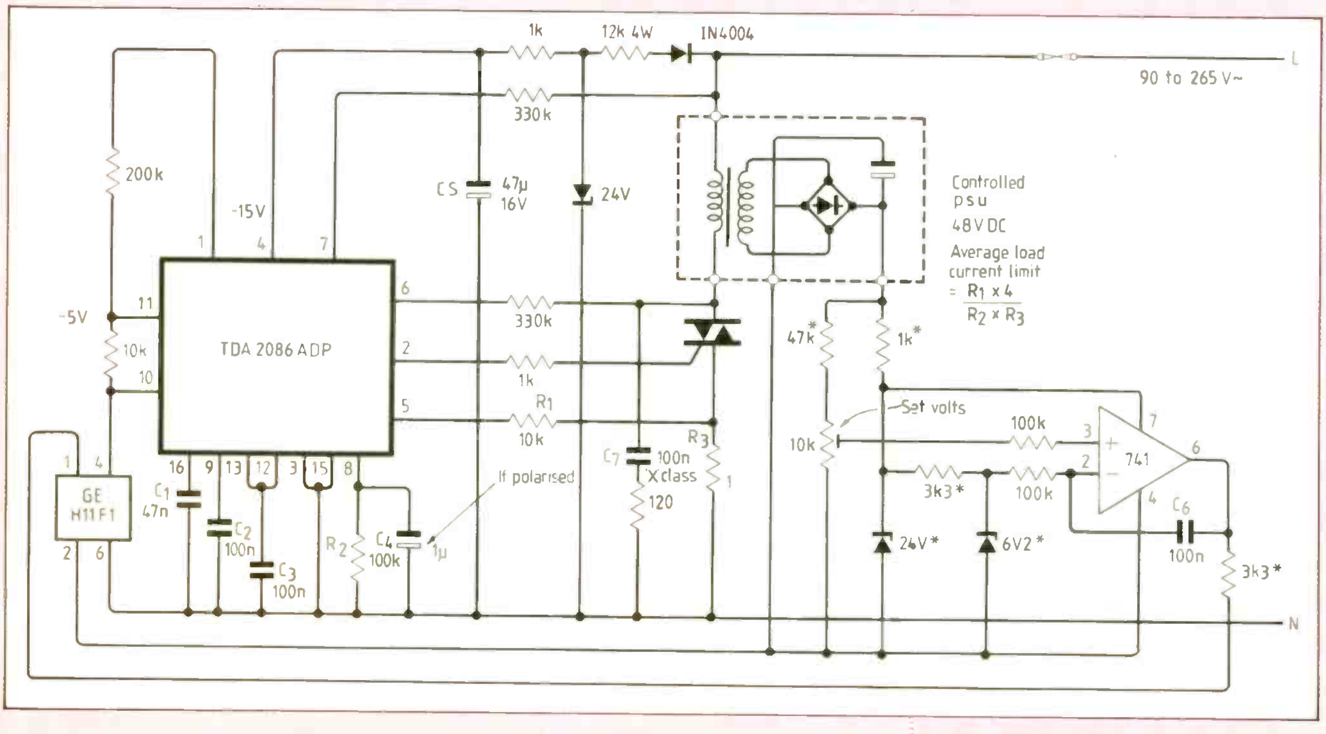
Power controller with wide input range

Alternating input voltages from 90V to more than 265V can be used with this current and voltage adjustable DC regulator. As shown, the circuit produces an output of 48V, but it can be modified to produce other voltages by adjusting components marked with an asterisk.

Isolation between the output voltage sensing circuit and input control is provided by an opto-resistive coupler such as the led-cadmium-sulphide MCD521 or the led-bilateral fet H11F1; I chose the latter on the grounds of cost.

G.N. Amos, Sheffield

Don't attempt to build this unless you are familiar with the practices and regulations relating to mains-carrying circuits. Note that the triac needs to be suitable for inductive loads. Ed.



Circuit Ideas

Electronic switching for musical-instrument applications

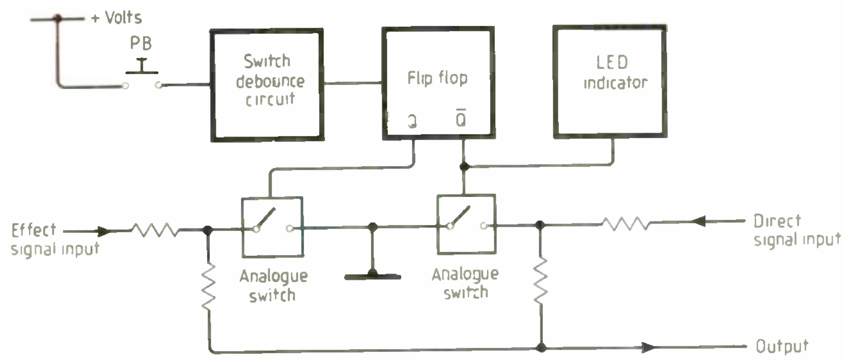
There is a vast range of musical-instrument effect pedals available and most of them feature discrete circuits to switch the effect in and out. Although some manufacturers include a DPDT foot switch, the more popular and reliable method is to use a push-to-make switch connected to a trigger circuit.

Such a trigger circuit, the first of those shown here, consists of debouncing, a bistable element, two analogue switches and a led indicator. Components are reduced considerably by a circuit based upon 4016 or 4066 quad analogue switches as shown in the second diagram. Remote control of up to four effect pedals is possible using four of the circuits in the third diagram. One 4001 or 4011 IC could be used as an inverter and the circuit could easily be extended.

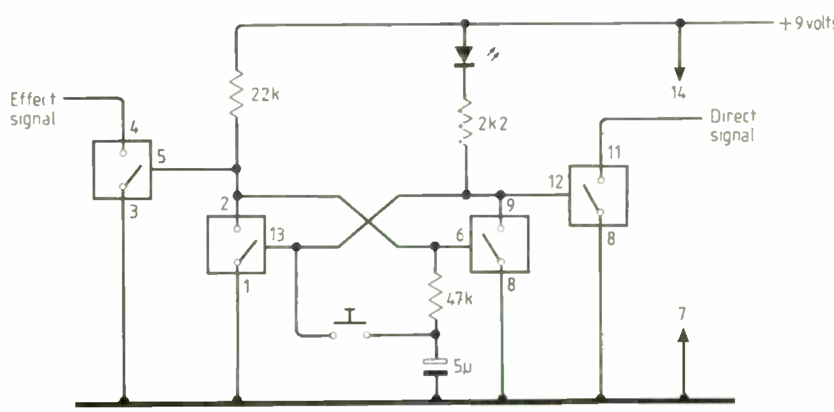
While all modern rhythm units incorporate Midi control, many have no facility for footswitch operation, which is an essential feature for live performers. A modification of the second circuit shown in the fourth circuit has been used to control the start/stop function of various rhythm units.

Each time that the foot switch is pressed, a brief pulse turns on alternative analogue switches. With the foot switch open, both analogue switches present a high resistance across the start/stop switches, enabling manual control.

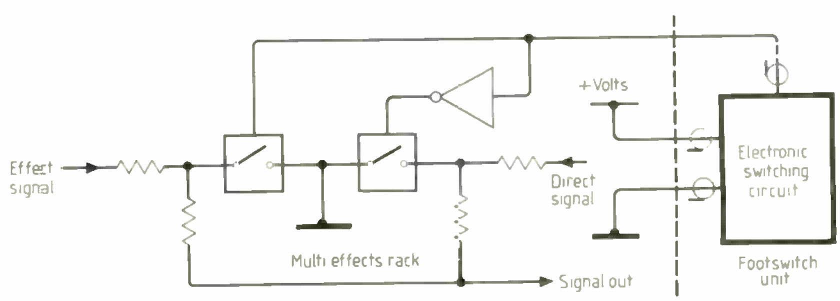
C. Evans
C. Evans Electronics
Liverpool



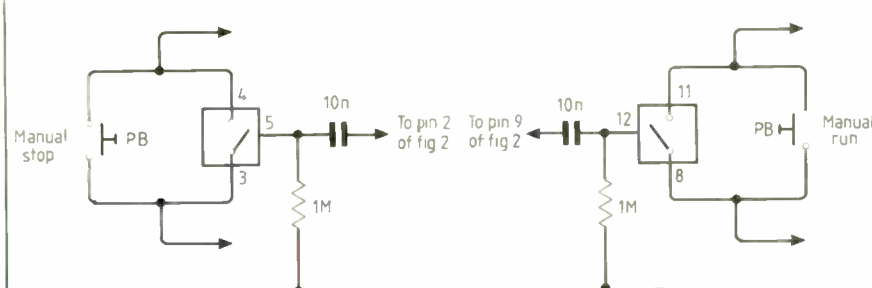
Block diagram of electronic switching circuit



Circuit for block diagram using a 4016 or 4066 IC



Remote footswitch operation of multi effects rack (1 circuit shown)



Modification of 4016 circuit providing footswitch operation of rhythm unit

Digital delay unit

Two minor errors appeared in A.G. Birkett's digital delay circuit published in the November 1988 issue. Resistor R_{27} is shown connected to 0V; it should go to −5V. The equivalent of the LS124 is the LS624, not the LS629.

SHANNON, CODING AND SPREAD SPECTRUM

To conclude this short series, the author describes the use of soft decision coding for error correction and some methods of countering bursts of noise or signal fading.

L. C. WALTERS

One of the important results of the work on information theory carried out by Shannon and others is what I term the Bureaucrat's Delight Principle. In simple terms it states that one should always delay making decisions for as long as possible. Information theory makes it clear that every time a decision is made information is destroyed. This is a very reasonable idea, since any signal may convey some amount of information which may be relevant, however remotely, to other information separated from it in time, or frequency, or space.

An obvious example is the effect of dispersive channels on binary data streams, where the actual signal received at any instant is a sum of the corresponding transmitted signal (possibly distorted) and delayed versions (probably also distorted) of earlier transmitted signals. This can give rise to what is known as inter-symbol interference and is usually considered a nuisance. However, it is intuitively apparent that, if sufficient were known about the dispersive mechanism, one might use the dispersed energy constructively to *improve* the quality of reception. Indeed many techniques, some of them adaptive, are described in the literature for achieving such equalisation as it is often called.

That information is destroyed by making decisions is also apparent if we consider a simple "deciding" equipment receiving binary signals. At the decision point it typically interprets positive voltages as 1 and negative voltages as 0. It therefore treats a $+1\mu V$ output and a $+1V$ output as equally indicative of a 1. It is obvious that the former decision is much more suspect that the latter, yet once the decision is made this information has been destroyed.

In the case of error correction/detection block coding one must in any case wait until the entire block has been received before attempting to decode it. A delayed decision is inevitable so far as output data is concerned. Why then should we destroy information by making hard decisions on each "bit" of the codeword?

Before attempting to answer this question we first consider the nature of soft decision decoding and the extent to which it is superior to hard decision decoding.

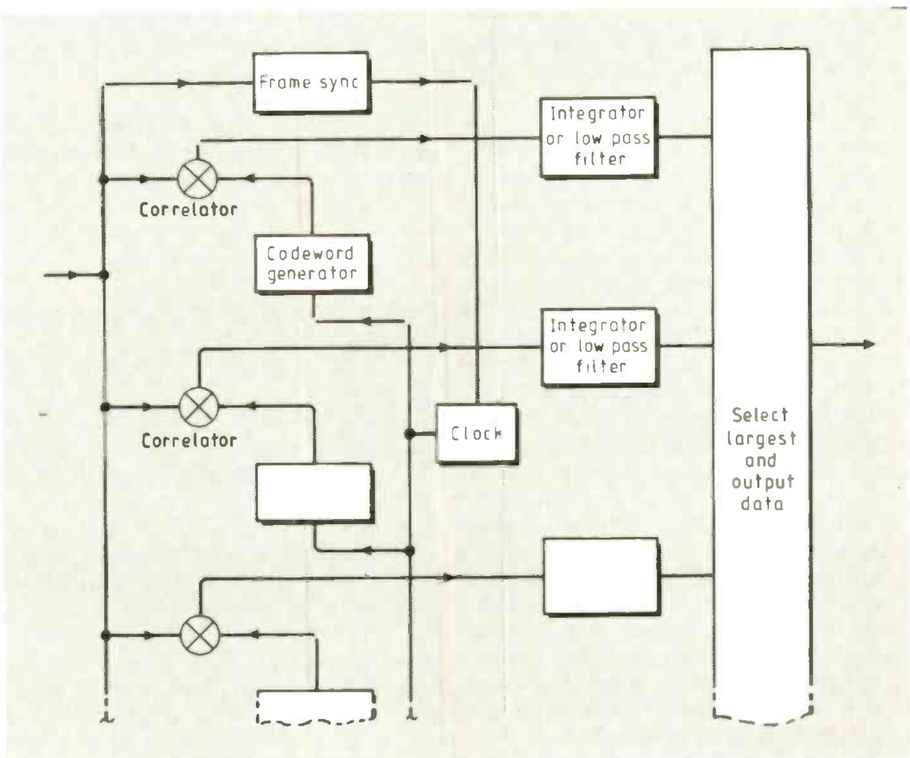


Fig.9. Outline of a soft decision receiver. Correlation can be implemented largely in software if the data rate is low enough.

SOFT DECISION DECODING

The soft decision process consists in attempting to answer the following question: "Given the exact waveform that we have received, what is the most likely waveform to have been transmitted?" Clearly, this question is unanswerable unless there are constraints on the waveforms which are *allowed* to be transmitted. Such a constraint could be that the transmission must comprise one of a known set of error-correction code blocks. We then wish to deduce from the received waveforms which of these is most likely to have been sent.

The bureaucrat's delight principle: always delay making decisions for as long as possible.

Many techniques are described in the literature for attempting this; but in the case of a waveform which is undistorted apart from the addition of white gaussian noise, it may be shown that the optimum detection technique is "matched filtering" – or, equivalently, correlation with each of the possible transmitted waveforms and the selection of that one which gives the greatest correlator output. Most soft decision techniques are, in fact, some sort of approximation to this, but in those cases where such correlation is genuinely achieved the receiver is described as a maximum-likelihood receiver: it is the best receiver which is theoretically possible in these circumstances. Note that such a system is identical in concept to DSSS receiving systems, though not normally applicable at such low signal-to-noise ratios because one rarely uses error correcting codes having very large redundancy factors.

Thus, an ideal receiver would comprise a limited.

Coding techniques conceptually similar to (though more complex than) those discussed in this series of articles have nevertheless permitted such communications to be maintained at ranges corresponding to the limits of the solar system, and, it is expected, beyond.

CODING *VERSUS* BANDWIDTH REDUCTION

Error correction encoding can be valuable in improving performance. But in the absence of jamming, spread spectrum performance can do no better in theory than a correspondingly reduced bandwidth system without such coding.

However, as the data rate gets lower and lower, it can become increasingly difficult or expensive to implement the bandwidth reduction. Consider, for example, a transmission at 0.05baud (such systems *can* be of interest!). That is to say, a transmission for which each data bit has a duration of 20 seconds. If this is to be conventionally implemented and to use an efficient modulation scheme such as phase modulation, then not only will there be severe problems in implementing the very narrow bandwidth filters required (often demanding very good phase response also!) but there will also be severe demands on the phase stability required of the transmitter and receiver oscillators. Both of these problems can be avoided by using very low rate coding and/or spread-spectrum to achieve the same performance (or better), using less demanding precision.

EPILOGUE

In this series of articles I have attempted to indicate some of the general principles of communication theory and to outline means of exploiting them.

The foundations of the subject were laid many years ago, arguably as early as the 19th century, with formidable names such as Lord Rayleigh appearing amongst the credits. Nyquist and Hartley in the 1920s certainly made substantial contributions and Shannon subsequently built on these to erect a coherent theoretical framework of great significance.

For many years the concepts of spread-spectrum systems were subject to national security constraints because of their potential performance as anti-jamming and/or low probability of intercept (LPI) schemes. However, for about two decades the principles have been increasingly publicized and are being applied to civil as well as military and other governmental applications. Error correction schemes of enormous diversity have also been employed or proposed, Hamming playing a pioneering role over thirty years ago but ably succeeded by an army of mathematicians and engineers.

Readers who wish to learn more of any of these topics are referred to the now vast literature which is expanding (in content as well as quantity!) at a high rate. For the more mathematically inclined, the reference below is an early exposition of error correction code design and is still considered as a bible on this topic. The historical developments and the latest ideas can, for the most part, be followed in the numerous volumes of the *IEEE Transactions on Information Theory*.

There is an attraction about a system which does not merely say "I'm not very confident" but which firmly states "There are errors".

I hope, however, that this series may have served to fill a gap in the knowledge of some whose main interests lie elsewhere and to whet the appetite of others. It may also serve to reduce the number of attempts to achieve the impossible!

Reference

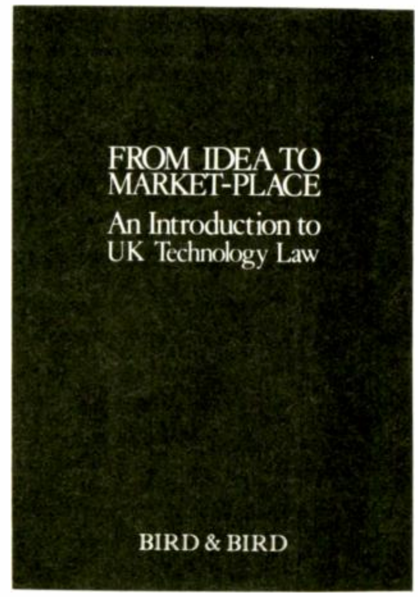
Error Correcting Codes, W. Peterson, M.I.T. Press, 1961.

After graduating from Cambridge University, Len Walters was directed under wartime regulations into the Ministry of Supply. He left in 1947 to take up a short service commission as an instructor lieutenant in the Royal Navy after which he became a research engineer with the Plessey Company at Ilford in 1951. In 1954 he joined the research laboratories of Decca Radar as a microwave engineer, returning to Plessey in 1955 as a group leader working on radar countermeasures and counter-countermeasures. At this time he evolved, together with colleagues, the idea of direct sequence spread spectrum, only to learn that others had had the idea earlier and that it was a highly classified topic.

He continued to work in this and many other areas at the Roke Manor research laboratories of the Plessey Company, where, following the successful crash development of a prototype main store for the then state-of-the-art Atlas computer he became chief engineer in 1961. He also worked on sonar, radar, ECM, ECCM and many aspects of communications including spread-spectrum and error correction systems and was a member of the communications sub-committee of the Electronics Research Council prior to its dissolution in 1982. He was also a major contributing member of its working party on ECM-resistant communications.

The author of some 20 patents, he retired as a senior consultant at Roke Manor in 1985. He has served on a number of IERE committees over many years and is currently a member of the IEE Professional Group E18 (electromagnetic compatibility).

● An informative 44-page booklet entitled **From idea to market place – an introduction to UK technology law** has been produced by a London firm of solicitors, Bird & Bird. In their foreword, the authors point out the importance of properly-secured technology rights – the neglect of which can occasionally lead to spectacular consequences, as in the withdrawal of the Kodak company from the instant film and camera market as a result of Polaroid's successful US lawsuit for patent infringement. This second edition of the guide follows the passage of the Copy-



right, Designs and Patents Act, 1988, which overhauled UK copyright and design law. Among the topics it touches upon are patent procedures, know-how, design rights (including semiconductor product topographies), computer software; domestic and EEC competition law, data protection, product safety; procedures for financing technology, including preparing a company for investment; commercializing technology; and intellectual property litigation, with sections on costs and remedies. Copies are available free of charge from Bird & Bird at 2 Gray's Inn Square, London WC1R 1AF; contact Karen Bohling on 01-242 6681.

Passport to World Band Radio, edited by Lawrence Magne and Tony Jones. Catalogue of HF broadcasts, both domestic and international. Main feature is a 260-page charts section, tabulating stations frequency-by-frequency and hour-by-hour, and based on monitoring observations as well as published schedules. Codes and notes are used to distinguish languages, power levels and the presence of jamming etc. Feature section contains 19 articles on international broadcasting, including a list of best and worst programmes: how does "The Future of the Marxist Leninist Movement is Growing in Scope and Strength", a five-minute slot on Radio Tirana, Albania, grab you? Extensive receiver buyer's guide covers 90 sets. Published by International Broadcasting Services Ltd (P.O. Box 300, Penn's Park, Pennsylvania 18943, USA), 416 pages, soft covers, £14.95 in the UK, ISBN 0-914941-17-8.

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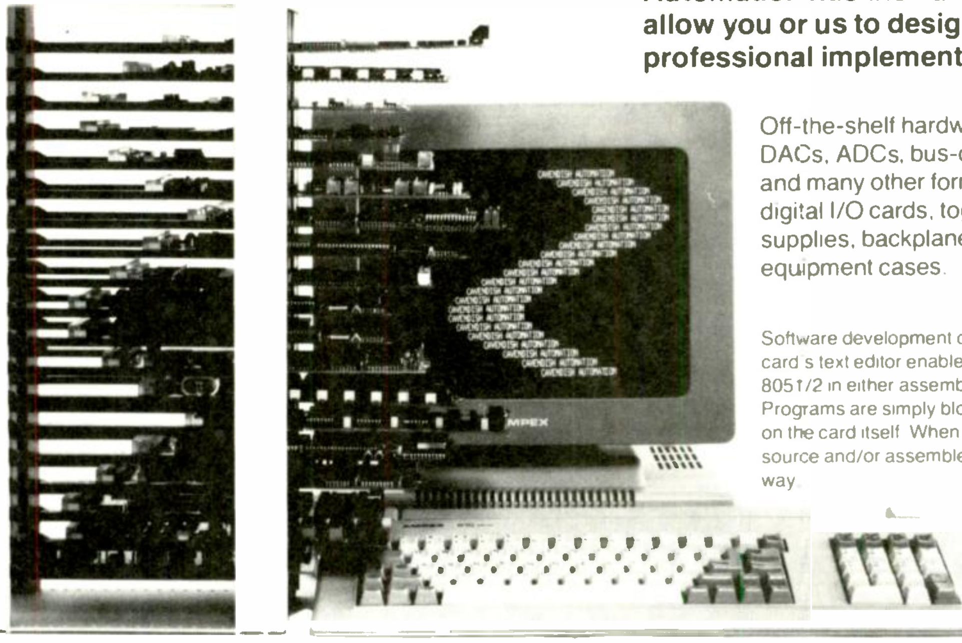

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Analogue Action

Reports and topics from the linear world by John Lidgey of Oxford Polytechnic.

John Lidgey discusses topics from the analogue world.

Analogue electronics is alive and kicking. It is the purpose of this column to remind the reader of this fact, to preview new ideas and techniques and to review some important aspects of analogue circuits.

It can be argued that there is no such thing as a true logic gate: they are really non-linear analogue circuits with sufficient gain that the output voltage is high or low, depending upon the particular function of the gate and the value of the inputs. But it is often necessary to consider the true current-voltage behaviour of these circuits, rather than a simple Boolean description, to fully identify the performance features, including limitations. So the term analogue should be taken in its broadest sense.

Single-chip VLSI systems are now a reality due to the shrinking feature size of state-of-the-art c-mos processing. With the increasing complexity on a single chip there is growing demand for lower power supply working voltages; 3.3V is likely to become a new industry standard. Digital processing dominates such chips, leaving only signal conditioning and A-to-D conversion functions to the analogue domain. Process parameters are optimized for digital performance, and so it is necessary to look for alternative analogue techniques that can operate well when built on a standard digital process.

Current-mode rather than voltage-mode circuits seem particularly attractive when voltage headroom is being reduced and this is confirmed by recent research reports on current-mode A-to-D converters[1] and switched current techniques for analogue sample-data signal processing[2], both techniques making extensive use of current mirrors.

CURRENT MIRROR A-TO-D

The single bit cell needed to provide a one-bit algorithmic conversion is shown in **Fig.1**. Input current, I_{in}, is first doubled by the current-mirror Tr_1 to Tr_3, then inverted with a second current-mirror Tr_4 and Tr_5. This $2I_{in}$ current is then compared with a reference current, I_{ref}, appropriately mirrored to a current comparator through another current-mirror Tr_{10} and Tr_7. Should $2I_{in}$ be less than I_{ref}, the digital output goes low and Tr_9 is held off and the analogue output is simply $2I_{in}$. But, should $2I_{in}$ exceed I_{ref} then the digital output is high, Tr_9 conducts and the analogue output becomes $2I_{in} - I_{ref}$.

To implement an N-bit converter, the basic cell of Fig.1 is cascaded as in **Fig.2**. The converter is referred to as algorithmic because of the successive doubling of the output of the jth cell and comparison of this current with the reference. The current comparator, **Fig.3**, is simply a cascade of two c-mos inverters.

The particular advantage that this circuit design has over and above more conventional analogue techniques is that there are no capacitors, op-amps or control logic. It is physically small and consequently ideal for VLSI where silicon area is at a premium; and because of its simplicity and small size it promises to be fast. This research has been reported by Nairn and Salama[1] of the University of Toronto, Canada.

SAMPLE-DATA SIGNAL PROCESSING

Switched capacitor techniques are essentially a means of providing analogue signal processing by manipulating sampled voltages. An alternative technique based on

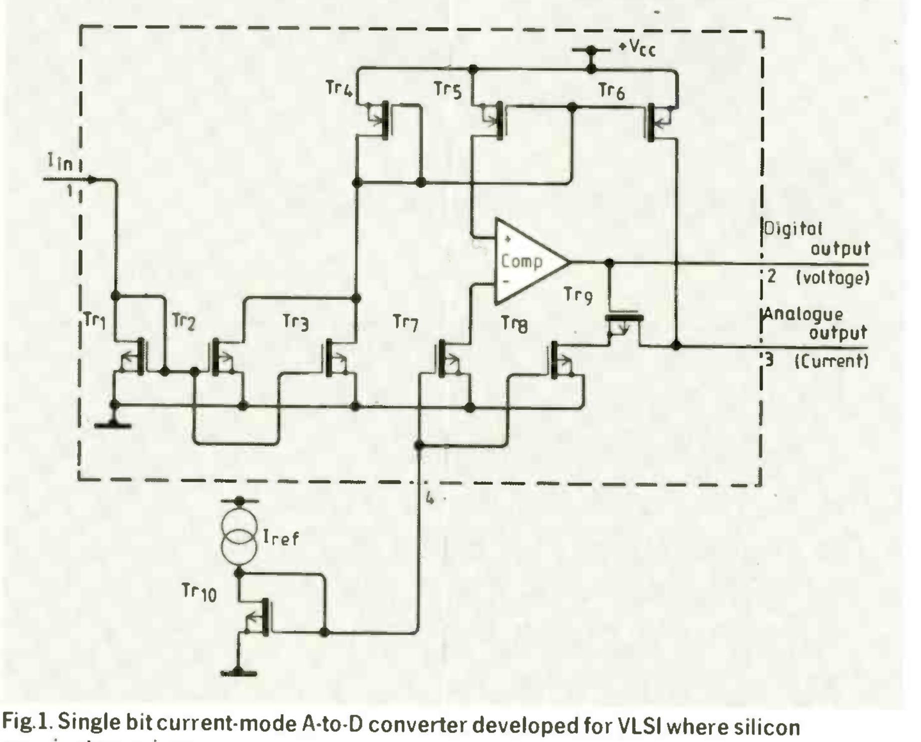


Fig.1. Single bit current-mode A-to-D converter developed for VLSI where silicon area is at premium.

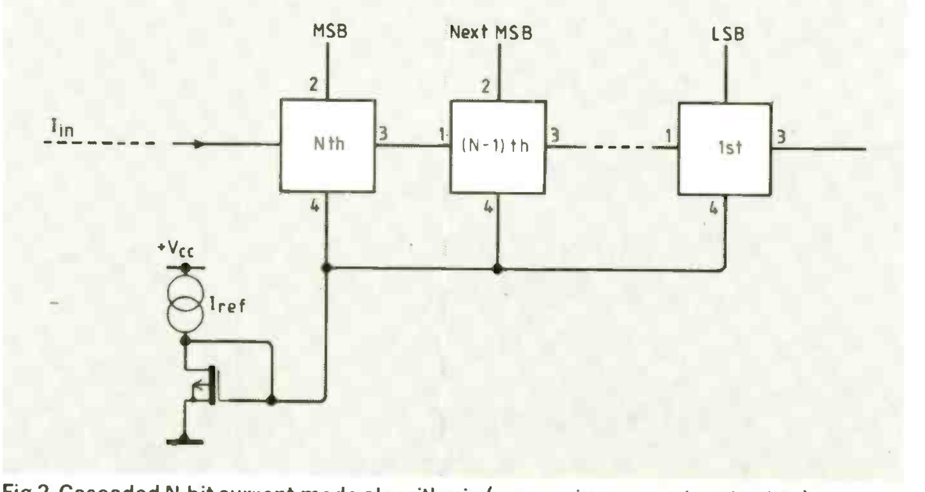


Fig.2. Cascaded N-bit current-mode algorithmic (successive-approximation like) A-to-D converter.

switched currents has been proposed by Hughes *et al.*[3] In much the same vein as the current-mode A-to-D converter, the technique is being developed to enable analogue signal processing to be achieved simply and economically on a standard c-mos VLSI digital process.

The functional blocks that are needed to provide a similar repertoire to those used in switched capacitor circuits are summation, inversion, scaling and memory of analogue inputs. Based once again on the current-mirror, the principles have been demonstrated by the Philips Research team[3].

Figure 4 shows a current-mirror capable of providing inverting summation and scaling. The bias current source, I_0, forward biases Tr_0, which allows bidirectional input signals to be handled. Scaling is achieved by appropriate choice of aspect ratio (W/L) of the transistors.

Analogue sampled-current memory is achieved using the switched current-mirror of **Fig.5**. When the switch S is closed the parasitic gate-source oxide capacitance of Tr_1 charges to V_{gs} of Tr_0 and whilst that charge is retained the output current is equal to the sampled current, with phase inversion. The circuit behaves like a sample-and-hold but in the current domain. Performance is linear despite non-linearities in C_{gs} because the capacitor is used only to store V_{gs} of Tr_0. A current delay circuit is shown in **Fig.6**, where the two switches are fed with non-overlapping clocks Φ and $\overline{\Phi}$. The output current i_0 at the Nth clock period is the analogue sampled input current at the (N−1)th clock period.

Using these building blocks, with some added sophistication to improve inaccuracies, practical current-mirror matching of 0.1% has been achieved with current memory distortion of −80dB. Also the feasibility of the technique has been further explored by simulation of a switched-mode sixth order Chebyshev low-pass filter.

References

1. Nairn, D.G. and Salama, C.A.T., Algorithmic analogue/digital convertor based on current-mirrors. *Electronics Letters* April 14, 1988, Vol. 24 No. 8 pp 471-2; High-resolution current-mode A/D convertors using active current-mirrors. *Electronics Letters* October 13, 1988 Vol.24 No.21 pp 1331-2.

2. Hughes, J.B., Bird, N.C. and Macbeth, I.C., Analogue sampled-data signal processing for VLSI using switched currents. IEE Colloquium on Current-Mode Analogue Circuits, February 17, 1989 Digest No 1989/25 paper 5.

Dr F.J. Lidgey is a principal lecturer at the Oxford Polytechnic.

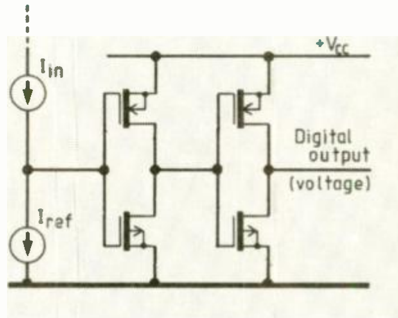


Fig.3. Double inverter c-mos current-input comparator for use in the current-mode A-to-D converter.

These two related techniques may well herald a new approach to analogue design for VLSI chips, since the current-domain appears to offer some significant advantages – particularly at the reduced voltages expected for future sub-micron processes. The research reported here is very current, in both senses; and the two research teams will be reporting their latest results at ISCAS 89*. This column will bring news of developments in these exciting areas just as soon as it breaks.

*** IEEE International Symposium in Circuits and Systems (ISCAS 89) Portland, Oregon, May 9-11, 1989.**

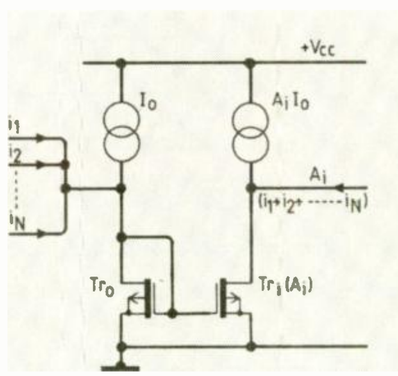


Fig.4. C-mos weighted current-mirror summing for current-mode analogue sampled-data VLSI.

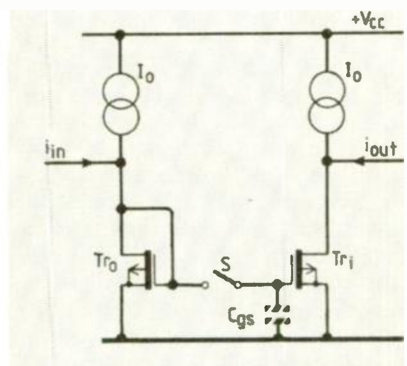
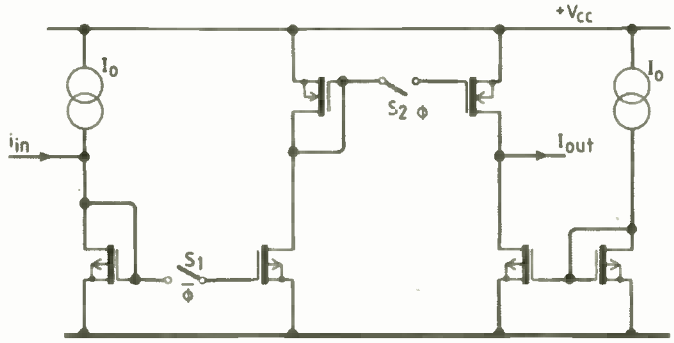


Fig.5. Switched analogue current-mirror current-memory cell uses gate-source capacitance to memorize the value of Vgs and so retain input current memory.



subroutine level, since there are three sets of return addresses and register data stored on this stack. Additionally, sitting at the top of STACK_B are data reflecting the state of Coroutine_B just prior to when c.p.u. operation switched over to Coroutine_A. This state data includes the working register contents together with the address of the next instruction that was to have been executed within Coroutine_B. Accordingly, when operation within Coroutine_A stops and c.p.u. execution is required to switch back to Coroutine_B, continuation can be simply invoked by POPping the state data back into the respective registers. Note, though, that the data is in STACK_B and the SP is addressing STACK_A prior to switching. Therefore, before switching, it is first necessary to save the current STACK_A SP value and replace it with the last STACK_B SP value. To this end, memory storage locations are required to hold the inactive coroutine SP values when execution is within another coroutine.

Listing 1 is an example, written in Z80/280 mnemonics, of possible software pathways linking Coroutines A and B. In general, entry to a pathway would be made via an interrupt request or CALL instruction; however, when a CALL is used, as is assumed with Listing 1, it is necessary to start the pathway with a DI (Disable Interrupt) instruction. This avoids any possible system interrupt complications during coroutine switching.

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In each RESUME routine, following the DI instruction, the current register contents are first saved on the stack; after which, the SP value itself is saved for use later. Thus with the coroutine state saved, the c.p.u. registers are reloaded with the parameter and stack-pointer values associated with the new working coroutine. Then with interrupts enabled and a RETurn instruction, c.p.u. execution is able to continue within the new coroutine.

Note that in the pathway example of Listing 1 it is assumed that storage locations are reserved at memory addresses ASPSTO and BSPSTO for the A and B coroutine SP values respectively.

Unfortunately PUSH and POP instructions are a significant switching time overhead; however, when using a Z80/Z280 microprocessor this time can be reduced if one of the coroutines has exclusive use to the alternate register set. Under these circumstances, the very short instructions EXX and EX AF, AF' can be invoked to achieve fast register switching – see later example Listing 2.

EXAMPLE OF COROUTINE STRUCTURING

To appreciate coroutine structuring, consider the system example illustrated in **Fig. 4**.

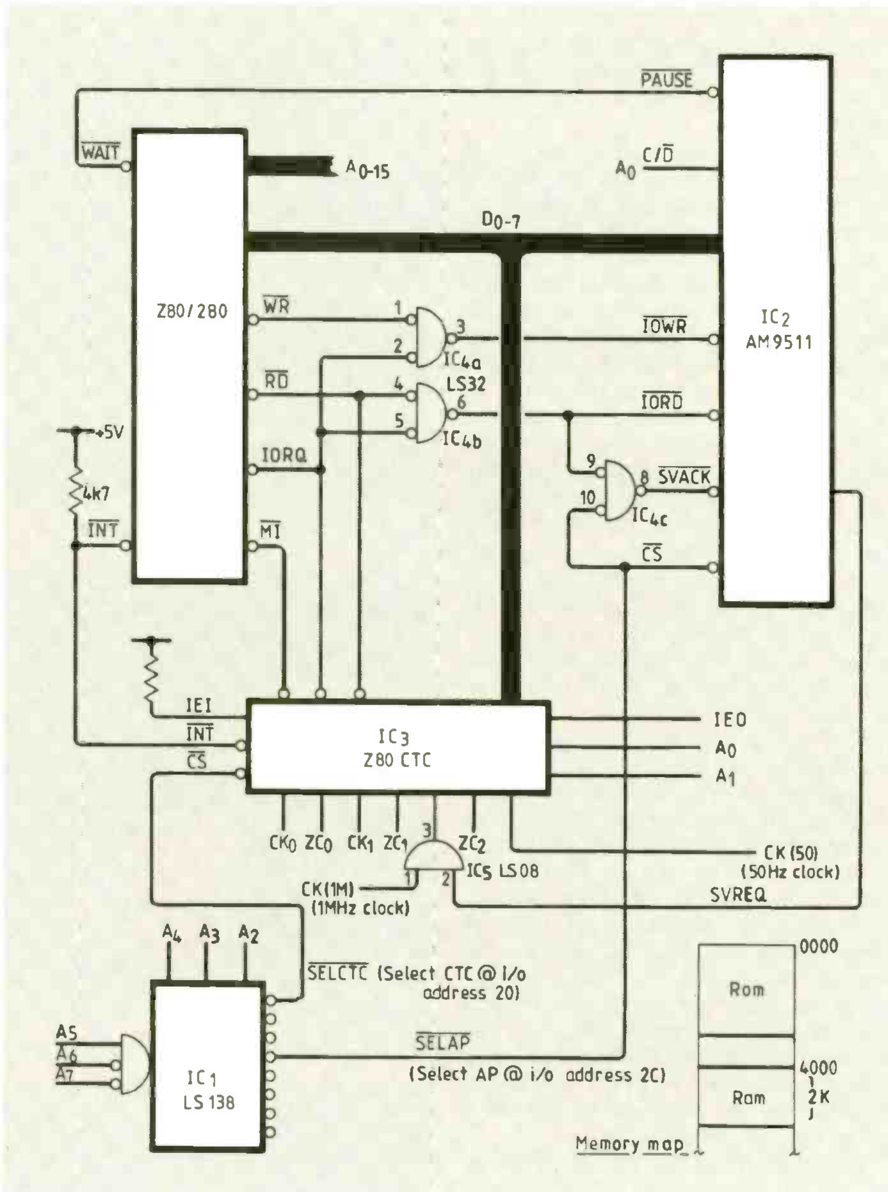

Fig.4. A system to illustrate the use of coroutines.

Listing 2a AP coroutine example – Preamble

```
                                :Define system I/O addresses

CNT0    EQU     20H             :Z80-CTC Counter #0
CNT1    EQU     21H             :Z80-CTC Counter #1
CNT2    EQU     22H             :Z80-CTC Counter #2
CNT3    EQU     23H             :Z80-CTC Counter #3
                                :-------------------------

APDAT   EQU     2CH             :AP Data
APCON   EQU     2DH             :AP Control
                                :--------------------------------------

                                :Define AP constants -

SVREQ   EQU     7               :Service request bit in AP command word
SV      EQU     80H             :Service request command
BUSY    EQU     7               :Busy-bit in AP Control word
                                :-------------------------

FADD    EQU     SV+10H          :Define a limited samole of 9511 Arithmetic Processor
FMUL    EQU     SV+12H          :commands.
FDIV    EQU     SV+13H          :All commands with a long execution time have the
SQRT    EQU     SV+01H          :service request (SV) bit set high (i.e. bit 7 of
NOP     EQU     00H             :the command byte).  This will assert SVREQ discrete
FIXS    EQU     SV+1FH          :high at the end of the AP calculation and so allow
FLTS    EQU     SV+1DH          :resumption of the AP coroutine via the interrupt
PTOF    EQU     17H             :request generated by Z80-CTC channel #2.
APEND   EQU     0FFH
                :etc.           :--------------------------------------

                                :Define ROM/RAM allocation
ROM     EQU     0               :Assume start of ROM at 0 Hex
RAM     EQU     4000H           :Assume start of RAM at 4000 Hex
RLTH    EQU     2048            :Assume a RAM length of 2k bytes
SPAIC   EQU     RAM+RLTH        :Define Stack_A initial SP value
SPBIC   EQU     SPAIC-256       :Define Stack_B initial SP value  i.e. Stack_A is
                                :assumed to be 256 bytes long
                                :-------------------------
```

```
                                  ;Define storage for -
ASPSTO  EQU     RAM+0             ;Coroutine_A stack pointer value
BSPSTO  EQU     RAM+2             ;Coroutine_B stack pointer value
                                  ;---------------------------

XVAL    EQU     RAM+4             ;X value in AP calculation example
YVAL    EQU     RAM+6             ;Y value in AP calculation example
XYMAG   EQU     RAM+8             ;Store for SQRT(XVAL**2 + YVAL**2)

                                  ;***************************

        ORG     ROM               ;Z80 reset point

RESET   DI                        ;Disable interrupts and jump to start of
        JP      CORTNA            ;Coroutine_A i.e. General Computing Module
                                  ;---------------------------------

        ORG     *6                ;Start of Interrupt Table
                                  ;Note that CTC interrupt addresses must start on
                                  ;an even address and be a multiple of 8

INTAB   DEFW    0                 ;Counter #0 - not used here
        DEFW    0                 ;Counter #1 - not used here
        DEFW    RESCOB            ;Counter #2 - Resumes AP calcs after SVREQ is asserted
        DEFW    APCORO            ;Counter #3 - Initiates AP calculations every 20 ms.
                                  ;etc
```

Listing 2b AP coroutine example – Coroutines A and B

```
        ORG     100H              ;Start of Coroutine_A - General Computing Module

                                  ;General initialisation -
CORTNA  LD      SP,SPAIC          ;Load SP with Coroutine_A initial stack pointer value
        IM      2                 ;Set up CPU for interrupt mode 2 operation
                                  ;---------------------------------------------

                                  ;Z80-CTC initialisation

        LD      A,11010101B       ;Channel #2 programmed for counter mode, interrupts
        OUT     (CNT2),A          ;enabled, +ve edge triggering with time constant
        LD      A,1               ;value of "1" following.  Counter #2 resumes operation
        OUT     (CNT2),A          ;of AP coroutine every time SVREQ is asserted.
                                  ;-------------------------

        LD      A,11010101B       ;Channel #3 programmed for counter mode, interrupts
        OUT     (CNT3),A          ;enabled, +ve edge triggering with time constant
        LD      A,1               ;value of "1" following.  Counter #3 requests
        OUT     (CNT3),A          ;start of AP coroutine every 20 ms. (50 Hz)
                                  ;-------------------------

        LD      HL,INTAB          ;Load CTC with interrupt table base-address
        LD      A,L
        OUT     (CNT0),A          ;-------------------------

        LD      A,H               ;Load I register with interrupt-table page-address
        LD      I,A               ;-------------------------

        IN      A,(APCON)         ;Perform dummy status read from AM9511 in order
                                  ;to Reset SVREQ bit.

        ;EI                       ;Enable CPU interrupts

        ;At any point within coroutine-A the Z80-CTC channels #2 and #3  can request
        ;an interrupt: whereupon, execution will switch to coroutine-B

        ;Coroutine-A other instructions etc.

        JP      RESET             ;At end loop back to start of coroutine-A and repeat

                                  ;*****************************

                                  ;Coroutine_B (AP Coroutine) entry point - initiated
                                  ;by Z80-CTC Channel #3 interrupt every 20 ms.

APCORO  EXX                       ;Exchange registers.  It is assumed that this coroutine
        EX      AF,AF'            ;has exclusive use to the alternate register set.
                                  ;and that IX and IY are not used.
                                  ;-------------------------

        LD      (ASPSTO),SP       ;Save CPU's present SP value
        LD      SP,SPBIC          ;Load SP with AP-coroutine stack initial value
                                  ;-------------------------

        EI                        ;Enable higher level interrupts and begin AP calculations.

        CALL    MAG               ;Determine Magnitude

        Other AP routines etc.    ;-------------------------

        DI                        ;At end of AP coroutine disable interrupts in order
                                  ;to avoid potential hazards during SP switch-over.
                                  ;-------------------------
        EXX                       ;Recover original parameter and stack pointer values
        EX      AF,AF'
        LD      SP,(ASPSTO)       ;-------------------------

        EI                        ;Enable interrupts and return to point in program
        RETI                      ;prior to Channel #3 interrupt request
```

where a AM9511 arithmetic processor AP IC_2, at I/O address 00101100B, and a Z80 counter-timer-circuit (c.t.c.) IC_3, at I/O address 0010000B, are assumed to be operating within a Z80/Z280 microcomputer system. For the system, two programming tasks A and B have been written, with A being a general computing module, and B a module that performs arithmetic processing calculations, aided by IC_2. Module A is assumed to loop continuously, whilst Module B is initiated by an interrupt request every 20 ms, using the 50 Hz clock CLK (50) at the input to channel_#3 of the Z80 c.t.c.

Software modules A and B could be made to run sequentially; however, the total execution time would then be quite long, since many of the AM9511 AP function calculations can take over 2000 clock cycles to implement. Therefore, to improve operating efficiency, the two modules are designed to run concurrently with each other under interrupt control. That is, the program is organized to execute instructions within Coroutine_A whilst the AP is busy and only return to Coroutine_B when the calculation is complete. In **Fig. 4**, this return mechanism is realised by connecting the AP service-request line SVREQ to the Z80-c.t.c. channel_2 clock input and arranging for the channel interrupt to be enabled. Thus, as the AM9511 arithmetic processor i.c. asserts the discrete SVREQ at the end of a calculation, an interrupt will be requested, allowing a resumption of Coroutine_B. Note that SVREQ is only asserted if the SV bit (i.e. bit 7) of the AP op-code commanding the calculation has been set high.

Regarding software for the system, listing 2 provides a possible skeletal solution written in Z80 mnemonics. Coroutine_A uses the standard c.p.u. register set; however to expedite coroutine switching, it is assumed in the example that Coroutine_B has exclusive use of the alternative c.p.u. register set.

Within Coroutine_B, AP calculations are performed by entering routine APCALC with the c.p.u. register DE pointing to the appropriate AP command string address. APCALC then fetches the commands in turn from the string, determines their type and outputs them, if appropriate, to the arithmetic processor i.c. for subsequent execution. APCALC distinguishes between three types of AP commands as characterized below –

APEND — this is a string terminator command and invokes an immediate return from subroutine APCALC.

SV-bit reset — These commands have a short execution time >30 clocks. Whence, when detected, the c.p.u. simply idles and tests the BUSY bit of the AP status byte until the calculation is complete.

SV-bit set — These commands have a long execution time, therefore when detected a call is made to the pathway entry point at address RESCOA in order to allow c.p.u. operation within Coroutine_A.

Listing 2c AP coroutine example – Coroutine-B entry and exit

```
                        Arithmetic Processing Tasks -
                        where TOS = AP Top-of-Stack
                        and   NOS = AP Next-on-Stack
                        --------------------------

                        Determine Magnitude

MAG     LD      HL,XVAL     Load 16 bit data at XVAL onto AP TOS
        CALL    LAPSM       On completion of LAPSM HL points to YVAL
                        --------------------------

        LD      DE,SQUAR    Point DE to command string and evaluate TOS**2
        CALL    APCALC
                        --------------------------

        CALL    LAPSM       Load 16 bit data at YVAL onto AP TOS
                        --------------------------

        LD      DE,SQUAR    Point DE to command string and evaluate TOS**2
        CALL    APCALC
                        --------------------------

        CALL    APCALC      After previous command DE points to ADDSRT whence
                            evaluate XYMAG = SQRT(XVAL**2 + YVAL**2)
                        --------------------------

        LD      HL,XYMAG+1  Store resulting TOS value in memory at XYMAG
        CALL    LMSAP

        RET
                        --------------------------

                        AP command strings -

                        Convert TOS from 16 bit fixed point to floating
                        point format then square TOS

SQUAR   DEFB    FLTS PTOF FMUL APEND
                        --------------------------

                        Add TOS to NOS take SQRT of TOS then convert to
                        fixed point 16 bit number

ADDSRT  DEFB    FADD SQRT FIXS APEND

                        **************************

                        Load memory with 16 bits of data from AP
LMSAP   PUSH    BC          On entry HL points to memory location MS byte

        LD      C,APDAT

        IND                 Transfer two bytes of data from AP to memory
        IND

        POP     BC          On return HL = HL(entry) - 2
        RET
                        **************************

                        Load AP with 16 bits of data from memory
LAPSM   PUSH    BC          On entry HL points to memory location LS byte
        LD      C,APDAT

        OUTI                Transfer two bytes of data from memory to 9511 AP
        OUTI

        POP     BC          On return HL = HL(entry) + 2
        RET
```

Listing 2d AP coroutine example – AP computation

```
                        ;Implement arithmetic calculation.  On entry DE
                        ;points to start of AP operand string in memory

APCALC  LD      A,(DE)      ;Read AP operand
        INC     DE          ;Increment AP operand pointer
        CP      APEND       ;Check whether operand is a command string end - APEND
        RET     Z           ;If true exit, otherwise
                            ;--------------------------

        BIT     SVREQ,A     ;Test service request bit
        JP      Z,APWAIT    ;If not set loop via APWAIT until 9511 busy bit
                            ;is cleared
                            ;--------------------------

        CALL    RESCOA      ;When here SV-bit is set, hence resume operation
                            ;in Coroutine_A
                            ;--------------------------

                            ;When calculation is complete SVREQ bit will be asserted
                            ;and CTC channel #2 will then request an interrupt.  Whence
                            ;operation will revert back here via RESCOB pathway.

        JP      APCALP      ;Thus loop via APCALC and read next command.
                            ;**************************

APWAIT  OUT     (APCON),A   ;Perform AP calculation

        IN      A,(APCON)   ;Read 9511 status.

        BIT     BUSY,A      ;Check activity of AP by testing status BUSY bit
        JP      NZ,APWAIT   ;If busy, loop via APWAIT until calculation complete

        JP      APCALP      ;Read next AP operation code

                            ;**************************


                            ;Coroutine_A Pathway - entered with a CALL command
RESCOA  DI
        OUT     (APCON),A   ;Perform AP calculation

        EX      AF,AF'      ;Exchange registers and stack pointer
        EXX
        LD      (BSPSTO),SP
        LD      SP,(ASPSTO)
        EI
        RET                 ;Resume operation in Coroutine_A i.e. General Computation
                            ;-----------------------------------------


                            ;Coroutine_B Pathway - entered via an interrupt
RESCOB  EXX
        EX      AF,AF'      ;Exchange registers and stack pointers
        LD      (ASPSTO),SP
        LD      SP,(BSPSTO)

        IN      A,(APCON)   ;Dummy read to reset AP Service Request (SV) bit
        EI
        RETI                ;Resume operation in Coroutine_B i.e. AP calculations
```

After an AP command of the latter type has been issued and operation is within Coroutine_A, the interrupt routine RESCOB, associated with Z80-c.t.c. channel_2 will eventually be requested when the calculation is complete. As this is a pathway entry point, c.p.u. control will transfer back to Coroutine_B and so allow further AP calculations to be performed. In **Fig. 4**, the Z80-c.t.c. channel_2 acts essentially as a positive edge-triggered interrupt mode with a count value of '1'. Thus, whenever the SVREQ line of the 9511 goes high the counter decrements to zero and generates an interrupt.

Note that in a larger system, with additional higher priority interrupts, the rising edge of SVREQ might be missed. Therefore, to guard against this possibility, SVREQ is used to enable a repeated 1MHz edge until the interrupt is accepted. In **Fig. 4**, this is realised by using IC_{5a} and gating SVREQ with the 1MHz clock CLK (1M).

Note also, within pathway RESCOB, that the AP status register is read after exchanging the coroutine parameters and stack pointer values. This is simply a dummy I/O read statement to the AP and made to clear the SVREQ control line by asserting control input $\overline{\text{SVACK}}$ low. In Figure 4 $\overline{\text{SVACK}}$ is generated during the IN A,(APCON) instruction by using IC4c and gating $\overline{\text{IORQ}}$ with $\overline{\text{SELAP}}$.

References

1. Stone H.S. Microcomputer Interfacing. Addison-Wesley, 1982.
2. MOS Microprocessors and Peripherals Data Book. Advanced Micro Devices. (AMD) 1984.
3. Components Data Book, Zilog, 1987

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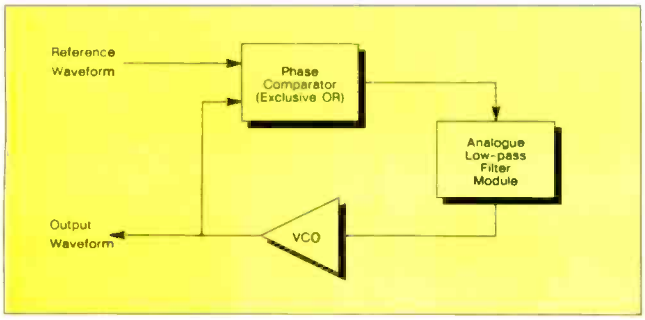
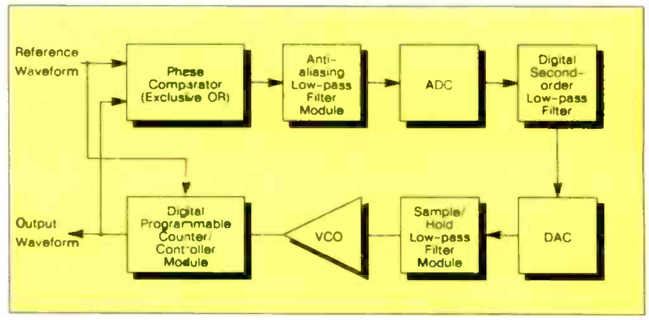
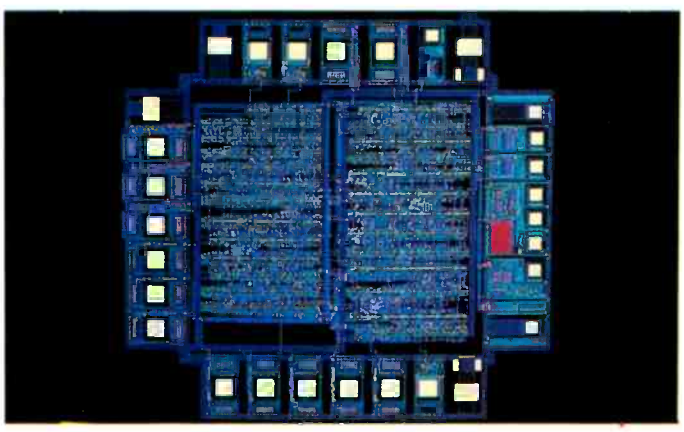


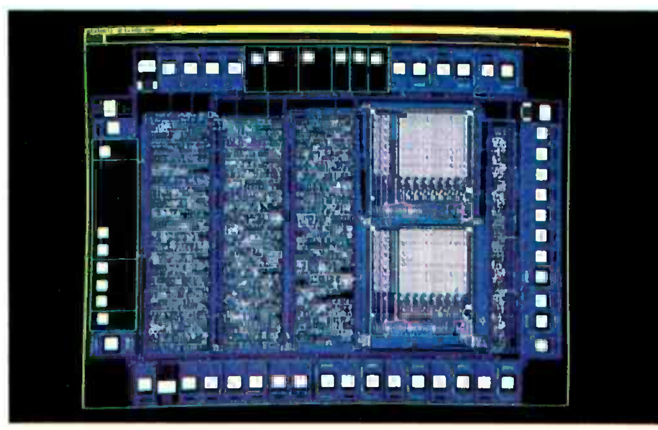


A typical example of the benefits of analogue/digital integration is in the implementation of a phase-locked loop (above). An all-analogue first-order loop can easily be implemented using ES2 analogue elements (above). For more advanced functionality, such as a greatly increased capture range, or the time division of outputs, an intelligent PLL, incorporating mixed analogue/digital elements, can be formed on a single asic (below). This chip replaces 12 discrete MSI components – including a microprocessor – resulting in significant performance benefits: high gain, no V/I drift, wide tracking/acquisition bandwidth and potential reduction to zero phase error.

This pioneering example (below left) of mixed analogue-/digital functionality is a chip design for a fighter aircraft oil-level indicator required to withstand high vibration levels and severe temperature changes. It is supplied by BAe for use in the Tornado fighter aircraft. Product represented the first venture of the designer into asics, and was prototyped in a very short time. It replaced a design using discrete components, offering enhanced capabilities beyond the original specification while fitting the same confined space.

As another example, New German safety regulations required Dahedi Electronics to redesign its portable continuous infusion pump for automatic injection of measured quantities of a drug at periodic intervals. The need to duplicate the control electronics to ensure fault-tolerant operation made an asic solution imperative within the constraints of size and power supply. In addition, there was a self-test requirement. The solution uses two crystal cells for the clock time standard. The die is mounted directly onto a hybrid substrate to minimise unit size. By integration in a single analogue/digital asic, a performance improvement factor of around 50 is achieved over a discrete logic Implementation.





Solo 1200 design with two generated ram blocks and three columns of random logic. Layout is optimised to match the height of the columns with the size of the ram blocks.

MULTI-PROJECT WAFER

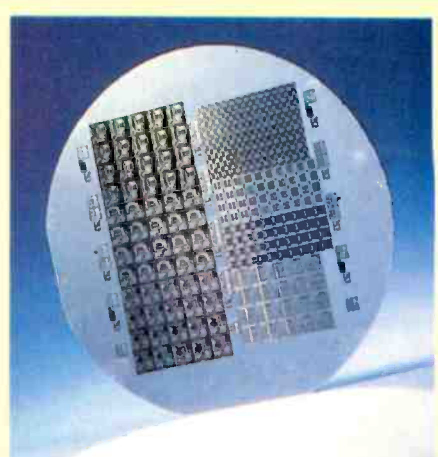
In wafer manufacture at ES2, the method of patterning a 5in wafer with designs used depends on the number of each specific device needed. When manufacturing prototypes and small quantities of an asic design the ability to place several different designs on one wafer is essential. For higher quantities normal optical methods are used.

Since ES2 supplies quantities as low as ten, flexibility provided by electron-beam direct writing techniques to mix designs on wafers is essential. The technologies used are 2μm and 1.5μm n-well, double-metal c-mos with a 1.2μm service being introduced in late 1989.

A separate database for each design is maintained in the e-beam system – in our case an Aeble 150. The e-beam writer exposes areas of optical resist, both positive and negative, using a vector scan technique. Lithographic quality of each written layer is checked automatically by an in-process optical wafer inspection system which digitizes the layer image for comparison with the design layout database.

Design layer information can be put on to the wafer as strips or blocks of designs. Thus a design requiring more than the normal number of prototypes will find itself beside different designs on a number of wafers.

Most designs are supplied by ES2 packaged and tested. However, if need be, probed or un-probed dice or parts of wafers an be provided. Electron-beam techniques also lend themselves to fabrication of continuous or repeating structures; several "wafer scale" devices for customers are currently being evaluated.



This wafer, with five different designs, represents an average example of the four to six designs/wafer normally run. Three strips, along two sides and the middle, are process-control monitors, i.e. standard designs like a duart, used to test conformance to ES2 specifications for that wafer.

rication and test procedures, and is applicable to all products which follow this design and manufacturing flow;
- electron-beam fabrication process is geared to low volumes at competitive cost.

The ES2 approach to analogue integration – placing standard c-mos analogue cells around the periphery of the asic – is a simple, low-cost solution which gives ease of access to analogue cells via pads, and ensures isolation of analogue and digital elements and their separate power supplies. The analogue cell library, currently implemented in double-metal, two-micron geometry, includes ADC, DAC, op-amps, comparators, oscillators, voltage reference, multiplexer and analogue I/O pads. Like their digital counterparts, analogue cells are an all-layer implementation – they are placed and aligned precisely where required on the asic, and are not restricted to a fixed cell position.

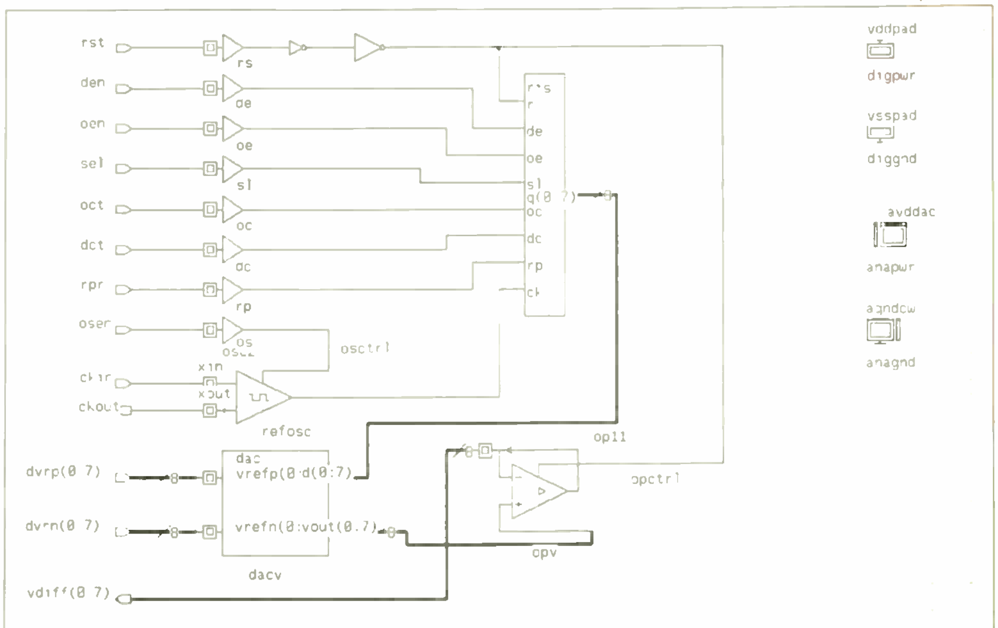
All analogue cells operate on a 5V supply, with an operational range within 0 to 5V. There are two guard rings on the core side to minimise digital noise, and input and output protection as required.

The ES2 integrated switch-level simulator and waveform display utility cover both digital and analogue elements. Analogue cells are simulated functionally to an 8-bit resolution, giving a 20mV step. Analogue channels are represented as 8-bit buses for simulation and schematic entry. This combined approach brings significant benefits, providing complete system simulation in a single operation. Benefits include the elimination of the problems when using separate, and often incompatible, digital and analogue simulators, and a great reduction in simulation time compared with such simulators as Spice.

Placement and routeing is simplified by the inclusion of analogue cells in the pad ring. Analogue cells are placed in an adjacent sequence between dedicated power and ground pads. These break the digital power and ground rings, ensuring isolation of the analogue elements from the digital elements. The designer has complete control of the positioning of the pad ring cells; routeing is automatic and guaranteed – the ES2 routeing utility iteratively widens routing channels until all connections are established.

DESIGNING ANALOGUE DIGITAL

The sequence of steps when designing an analogue/digital component is a simple variation on the all-digital sequence. Taking advantage of ES2's hierarchical schematics package:
- the digital processing elements are specified as a hierarchy of parts;
- at the top level of digital functionality, a single hierarchical element is formed, represented as a symbol;
- this digital element, together with the analogue cells and the digital and analogue power supply pads, is instanced in the top-level schematic of the asic hierarchy.



At the top level of ES2's hierarchical schematics package, a single digital element is represented as a symbol, together with analogue cells and power supply pads.

As part of the schematic entry routine, pad placement is specified. This gives the designer complete control of the positioning of analogue cells and digital pads.

When schematic entry is completed and the design compiled, the circuit is simulated. The resulting waveforms can be analysed, with analogue waveforms represented as 8-bit digital signals. The physical placement of the design is not different from the all-digital case. Using the automatic placement and routeing facilities, analogue parts are placed according to the pad placement specifications entered with the schematic.

The final stages of package selection, loaded simulation, validation and design sign-off are no more complex than with a digital-only design.

TESTING ANALOGUE PARTS

Because analogue cells are in the pad ring, they easily satisfy the two prime conditions for testability: observability and controllability. Most connections to the analogue cells are pads in themselves; those leading into the chip core can be connected to test pins if required. The main requirement for testing is that all analogue-enable signals are probed during simulation, and, if possible, connected to a dedicated test pad. This pad can be common to all analogue cells in a circuit, reducing the test pin count.

Simulation test vectors should exercise all analogue cells through their operational range. The test vectors used to validate fabricated die need to have a fixed time period of 10μs between input changes, for all circuits to have settled completely before sampling of outputs by the Sentry test equipment.

FUTURE DEVELOPMENT

The current implementation is ECDM20 two micron geometry, which is being superseded by the ECPD15 1.5 micron process. This will bring significant speed and power consumption benefits, and a reduction in area of all digital elements in a circuit. A longer-term plan is to improve the resolution of analogue signal representation to 10-bit, allowing finer-grain simulation and higher operational accuracy.

Further details of ES2's process are contained in 'The 1990 approach to custom silicon', by Chris Gare FIEE, in Industry Insight *on* semiconductors, Electronics & Wireless World, *June 1988, pages 588-91. European Silicon Structures UK business centre is at Mount Lane, Bracknell, Berkshire RG12 3DY, tel. 0344 525252.* ■

The £8000 asic

If you have a PC you could design your own asic, according to Colin Doré of Matra-Harris UK.

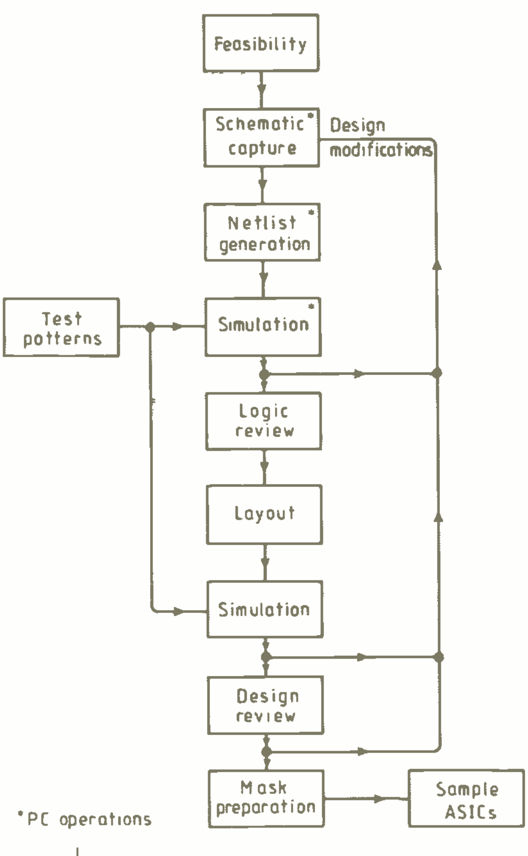
Asics have traditionally been regarded as an expensive option for the manufacturer who has the time and money to invest in dedicated CAE workstation. However, the humble PC has gained a lot of computing power over the last few years and a configuration which would not have shamed a multi-user system in the late 1970s (resident hard disk, 640K ram, high resolution colour graphics), is now commonplace. This is more than adequate for the design of small- to medium-sized asics, from design capture to logic simulation. Although it is not possible to produce a 50 000-gate array on a standard PC, the volume market for asics is currently in the sub-1500 gate region, and this size of IC is readily accommodated. The 400- to 800-gate sector has been particularly busy of late as PAL users convert their n-mos arrays into low-power c-mos asics.

Naturally, there are a few limitations on the complexity of a design which can be developed in its entirety using 640K of user ram; and the upper limit, depending on manufacturer and the software package, is around 2000 equivalent gates. Larger designs can be produced by partitioning, but the user will not be able to run a simulation on his design. However, netlists for arrays of up to 10 000 gates can be produced on a normal PC.

MORE COMPLEX ASIC DESIGNS USING A PC

On a standard PC the user is restricted to approximately 2000 gates if he wishes to carry out design capture, netlist generation and simulation for the whole design. The reasons for this are twofold: 640K is insufficient ram to run the simulation, and even a 386-based machine is really too slow for the complex "number crunching" involved. The obvious option is to transfer to a more powerful computer, such as a VAX or Apollo, with the associated high acquisition cost (around £10 000 per Mips for a MicroVAX). There is a large middle ground between this and the £1500 PC; and so MHS developed, in association with French software house Aptor, a boosted version of the PC which is capable of running designs of up to 40 000 gates. Hardware changes involve fitting a dedicated board designed around three Inmos T414 transputers, which adds up to 20Mbyte of ram to the machine and accelerates the processing speed up to 20Mips (as fast as the VAX 8600 using in-house test). A simpler version of the accelerator, using a single transputer, will process asic designs of up to 10 000 gates and costs about £18 000 (subject to availability) including the software. The user is tied to the Aptor software on this system, but design capture uses the well-known Silvar-Lisco front end. Because of the higher hardware costs compared with a basic PC, smaller users will normally rent this package rather than acquire it permanently.

Fig.1. Asic design process.



HARDWARE

The author's company has two principal c-mos channelled gate array asic processes which are supported by PC design packages. The MA series is a well-established (and hence high yield) process with a cell size of 3μm; cells are interconnected by a single metallization layer. Four die sizes cover the range from 228 to 1139 gates. Larger designs can be produced using the MB process, a 2μm double metal array with nine dies ranging from 810 gates to 7260; the maximum size which can be designed on a PC is 1920 gates. MA asics can be driven at up to 25MHz and draw from the 5V supply some 5μA/gate/MHz; MB types can be toggled at up to 400MHz and 3μA/gate/MHz.

Both processes have a high utilization ratio, up to 95% for an average design, because each gate cell incorporates one or two dedicated feedthrough channels. This makes interconnection through the cells in a "vertical" direction almost as simple as using the metal interconnects which run between rows of cells in a "horizontal" manner.

The design capture stage of an MA or MB array uses Gateaid Plus, a low-cost package based on the familiar OrCAD software. OrCAD was chosen because it is hierarchical in nature and user friendly; typically, only one day is necessary to gain familiarity with the package. Also included in this £2000 package is a netlisting routine, design rule checker and simulation driver. Boolean expressions may be converted directly to a netlist, a facility aimed primarily at users who are converting from pals to asics.

DESIGN PROCESS

Following the initial feasibility study (**Fig.1**), the designer carries out design capture on the PC. A netlist is then generated and a basic simulation run to verify the design. If the design is large, it will have been partioned and simulation can be carried out on the individual partitions. There then follows a logic review with the ASIC supplier, to verify that the design capture and simulation has been done correctly and the design is feasible on that manufacturer's particular process. After any modifications have been made, the netlist is transferred to a more powerful machine (in MHS's case a VAX 8600) and the layout generated for the asic itself.

A full-scale simulation follows, identifying any problems which have not so far surfaced; and, after a final design review with the user, the tapes are sent to the fabrication plant where masks are prepared for the metallization layers. Some asic suppliers use electron-beam direct etching rather than a photographic mask-and-etch process. Finally, samples are supplied for final test and, if these are satisfactory, production commences. With masked chips, changes at this stage will mean a new mask or masks, and so it is advisable to use a single metal process if at all feasible, since this involves only one mask.

COSTS

Apart from the PC itself and the software package, there are non-recurring expenses, i.e. set-up charges, to be considered. For the Matra MA process, these amount to around £5000 for a 250-gate array, rising to £7500 or so for a 1200-gate design. If no changes are made to the masks after pre-production testing, there are no further set-up costs and the user will pay for each asic at a unit cost depending on size, quantity, quality approval level (e.g. commercial, military or satellite) and package style. It is certainly possible to design and place into production a 250 gate device for around £8000 if the user already has a suitable PC.

EXPERIMENTAL ASICS

Once the design package has been acquired, one-off experimental designs may be produced at relatively low cost. Many fabrication plants run a multi-project wafer line in which a number of different one-offs are incorporated on the same wafer. The MHS version costs around £1000 per design, and is currently being used by M.Sc. students at Nottingham University. The only drawback of this approach to development is that if the design is found to be successful and is to be placed into production, re-engineering charges must be paid. ■

● For further information, contact Rod Oldfield or Colin Dore at Matra Harris Semiconductor Ltd, Easthampstead Road, Bracknell, Berks RG12 1LX. Tel: 0344 485757.

Non-volatile digilin asic

Electrically-erasable proms have uses not only in digital circuits but in mixed analogue/digital designs too, as Gordon Lindsay of Sierra Semiconductor shows here.

That analogue circuitry plays a major part in circuit design is demonstrated by the increasing number of vendors offering analogue integration. Many gate array vendors offer an A-to-D or 741 equivalent op-amps as integral devices in their gate arrays. However, these offerings cover only a limited numbre of functions with limited performance. Sierra's analogue cell library has over 70 functions including a variety of op-amps and comparators, and also complex devices like a 70MHz PLL or a 12-bit A-to-D converter or switched capacitor filters.

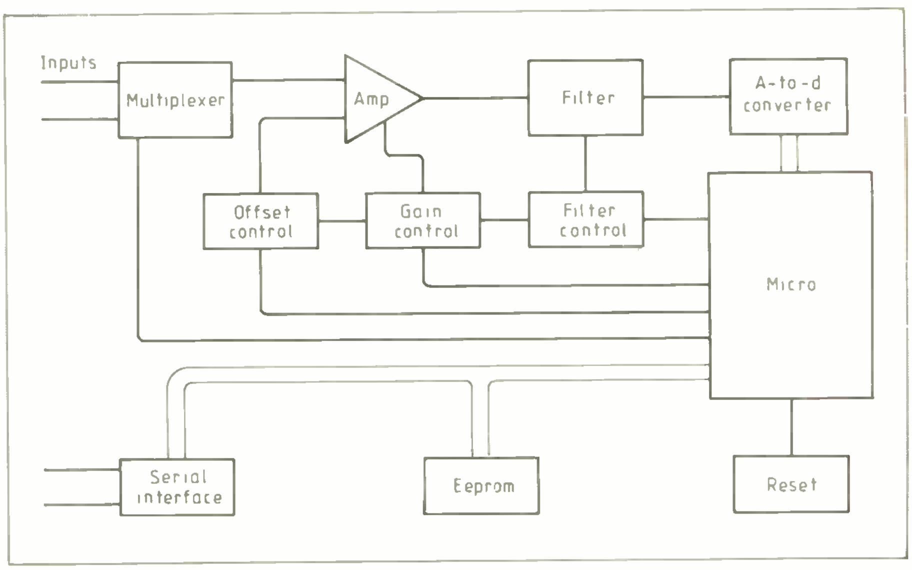
In developing its process technology, Sierra included a third component, the eeprom. There are 30 E^2 functions currently available. They range from single-bit D-types to n-bit registers up to 4K-bit arrays.

The ability to include E^2 elements with analogue and digital functions in one single c-mos chip will allow the non-volatile storage of digital variable data for all kinds of applications. But the availability of E^2 also offers many opportunities to control analogue circuits too.

The availability of E^2 adds an interesting dimension. A high percentage of boards contain potentiometers to make tolerance trimming adjustments and many boards will contain jumpers, links, or options on certain components for different models. With E^2 in the asic it becomes possible to customize the chip on an individual basis.

As well as allowing changes of component, E^2 offers the IC designer the ability to compensate for some of the problems inherent in IC design. In most ordinary c-mos processes the material polysilicon is used to implement resistors. However, processing tolerances mean that the value of a single resistor may only be accurate to ± 15 per cent. This can now be controlled to a greater degree of accuracy by chaining several individual resistors and switching different values in the chain according to the desired accuracy.

One major difference between c-mos and bipolar circuitry is that the offset voltage of an op-amp is higher for a c-mos design than for the bipolar equivalent. A "potentiometer" on chip can nullify this offset and store the compensating value in E^2. This allows the periodic calibration or compensation of the circuit in fluctuating environmental conditions. ■



The standard cell approach

Once, designing an asic meant juggling with individual components. Alan Cartwright of VLSI Technology outlines how libraries of standard definitions make life much easier for the design engineer.

A silicon compiler is a design tool which produces function blocks on silicon with a minimum of definition by the user. For example, compiling ram, rom, PLA, multiplier, etc. means to assign parameters for a ram (i.e. word width and word depth – 8×1024 etc.) and produce automatically the following: a symbol with electrical connections such as address, data busses, control signals, which is the connection to other function blocks by using a schematic editor; a model, which describes the function and timing behaviour, referenced during logic simulation when the circuit is simulated; and a physical layout block which is produced according to the selected technology (standard cell, gate array or c-mos process). This physical layout is correct according to process design rules and corresponds to the parameters, the symbol and the model as described above. The compiled layout is put together with the remaining function blocks to complete a circuit.

Asic design is closely associated with silicon compiling. In the past it was necessary to go down to single transistors when doing IC designing. Today, high-level system definition works with chip complexity of 100 000 gates (one gate corresponds to four transistors) and more.

A library of elements is necessary for effective IC design. These can be added to the compiled blocks. The library, which contains elements of small complexity such as gates, flip-flops, latches, etc. can be put together to form high-complexity circuits. The megacell library offers building blocks of high complexity: for example microprocessor and peripheral components. The megacells are generally industry standard component equivalents used for designing a digital system on a single chip. Examples include CRT controllers, DMA controllers, Z80 microprocessor, etc.

VLSI Technology's software tools not only offer high-level silicon compiling but also make it possible to work at transistor level. ■

Channelled gate arrays

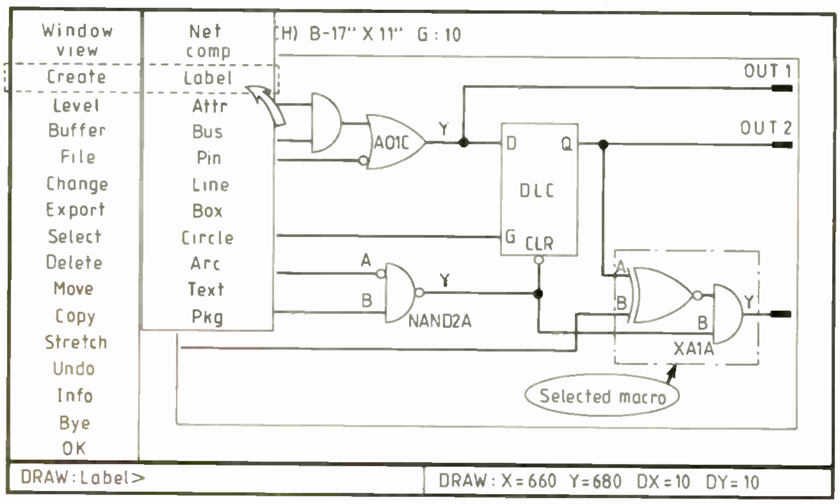
One of the problems with asic is turnaround time – you often have to wait weeks even before you know whether or not your design works. But now you can turn out a working device within hours on a PC, says Andy White of Gothic Crellon.

This asic approach has been likened to "desk top publishing" in gate array form.

These field-programmable gate arrays can be designed, programmed and tested from a 386-based PC in a matter of hours. Conventional gate arrays can take up to eight weeks for prototype manufacture, with costs of up to £15 000. The increased speed of development and lowered cost of implementation is thought-provoking. Virtually all electronics engineers should be able to design appropriate gate arrays on their desk top.

At the heart of the product is what its makers, Actel, call the Plice antifuse. An antifuse makes an interconnection when subjected to a programming voltage. Since an antifuse has the same width as the interconnection circuitry of a standard Actel device, they are placed wherever interconnections cross. Up to 168 000 of fuses on a part gives the user freedom in applications and permits completely automated placement and routeing.

On the standard device the basic building block is a configurable logic module, equivalent in complexity to a conventional gate array micro. Logic modules are arranged in rows, alternating with routeing channels. Vertical wiring connects the logic modules with the routeing channels, which contain further horizontal and vertical wiring segments. Antifuses can be activated to join wiring segments wherever they intersect



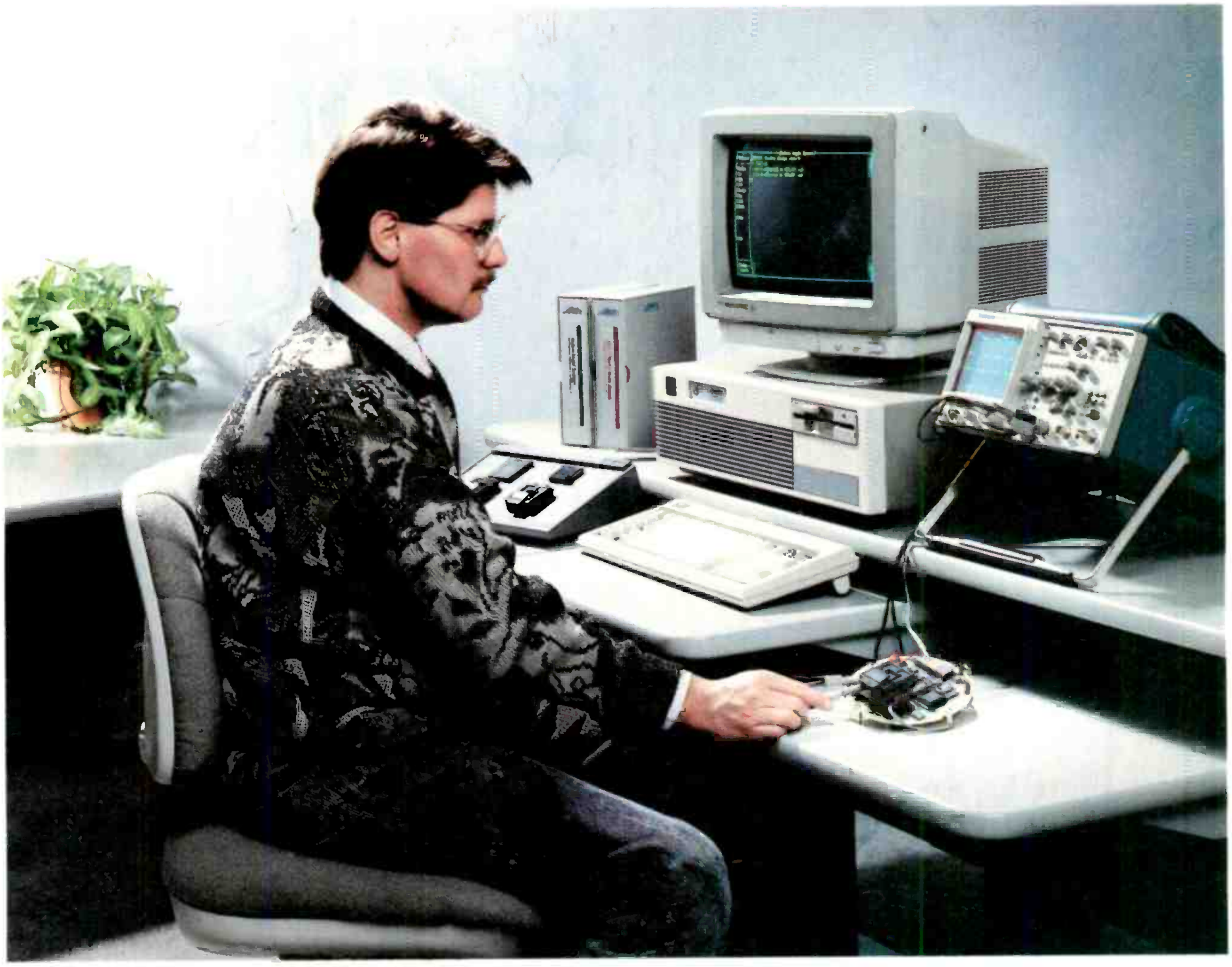
Example of schematic entry. This particular one – called ALS – integrates into a CAE system.

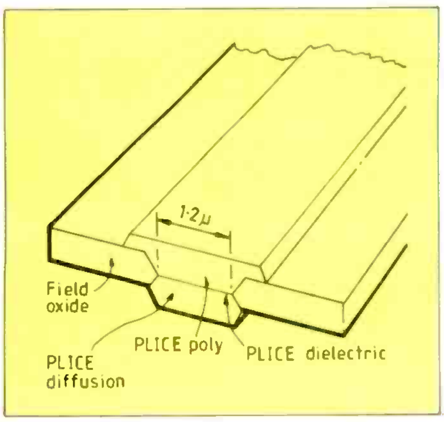
providing flexibility in layout.

The software design program incorporates Viewlogic Systems' Viewdraw and Viewsim schematic capture and simulation software. A library of over 200 standard logic functions includes gates, flip-flops and latches and TR functions. Once a design has been captured, Actel's proprietary place-and-route software automatically implements the design at 85% to 95% gate utilisation.

The Action Logic software system also checks devices before it programs them. Before removing a device from the programmer, the user can run Debug simulation software. Once a device is incorporated in a system, Actionprobe diagnostics can be used to observe any two nodes on the chip, in real time.

Using channelled gate arrays with the antifuse programming elements means that gate array prototypes can be created in a matter of hours. It also means that an asic solution can be considered without fear of



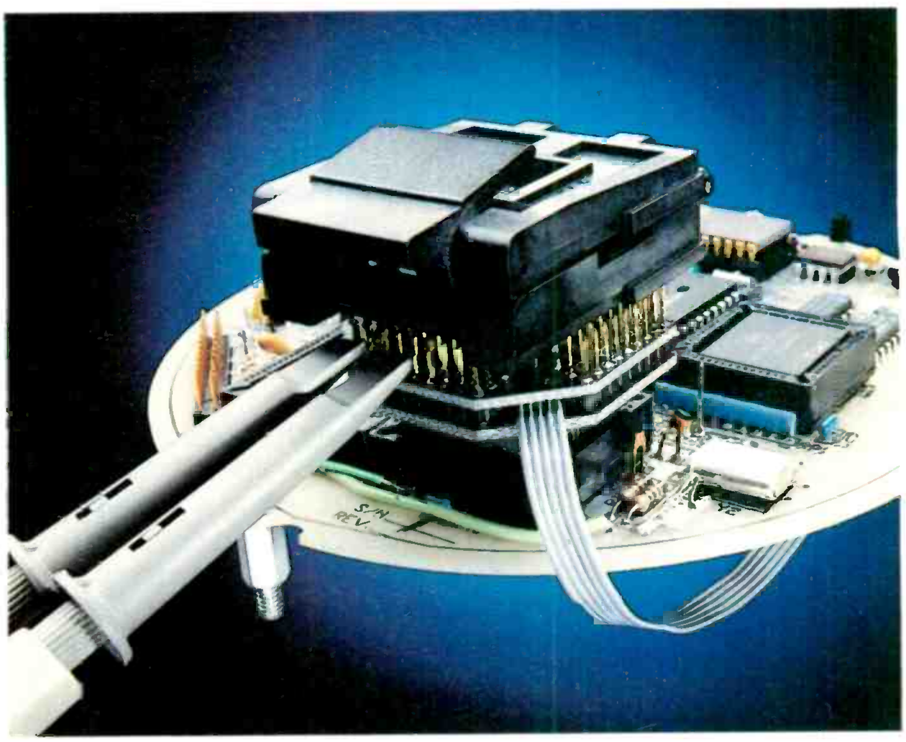


PLICE antifuses in user programmable asics are 50 times smaller than a static ram cell.

incurring costly, time-consuming mistakes.

This type of logic array is currently available in 1200 and 2000 gate form with larger arrays for release at the end of the year. The c-mos process allows toggle rates of up to 70MHz. Device pricing has initially been pitched at £30 in 100-up quantities.

UK distributor Gothic-Crellon says that Actel designs can be ported to other higher volume asic technologies using the design netlist. The reverse also applies, allowing prototyping of other technology gate arrays in the Actel form. ■



For small runs, it can pay to design and make your own asics using a PC compatible and programming/test fixtures.

Exploding custom

1. THEY'RE EXPENSIVE

"Custom Silicon is certainly too important to be ignored by any company now contemplating or already involved in the manufacture of products incorporating electronics".

These aren't the words of some high-tech guru, but a recent quote from the DTI.

So it's practical advice. Vital for Great Britain. Vital for you.

MCE are the pioneers of "Falcon", a route into Micro-Circuitry which is cheaper than anything else on the market, simply because it's better organised. The design programme incorporates easy cut-off points so you are never financially committed beyond the work actually in hand. It's so efficient, that you can get delivery of prototype devices for as little as £600.

Yes, £600.

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Fast.

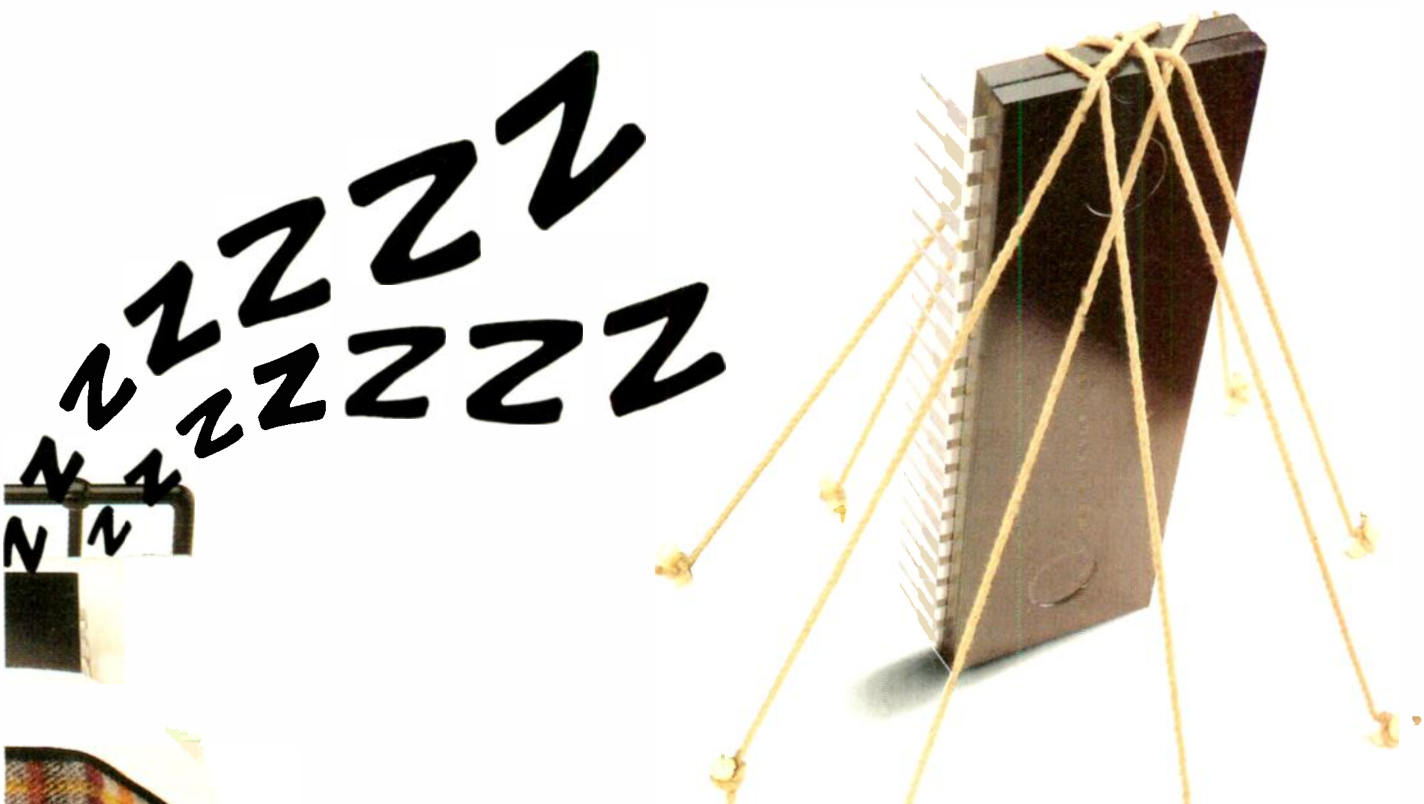
From design through to delivery of production parts it's a very speedy operation.

Your design is marked "Urgent" right from the moment it is received by MCE. We supply you with a highly optimised suite of software which, running on a PC, enables you to debug and validate your logic on your own premises. So there's no costly time wasted sending designs and amendments to and fro.

Then, once you provide us with design data, we'll put it on our regular 'Silicon Shuttle', and deliver prototype devices to you within 30 days.

Yes, 30 days.

some myths about micro-circuits.



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We control costs by leaving you, the customer, in control of your own development.

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Phone Mike Goodwin on (0684) 297277

Working in asics

What personal qualities should an asic designer possess? Degree level engineering certainly, but a basic appreciation of board layout and board level chip systems are equally important says Dom Pancucci of our sister publication, Electronics Weekly

Commercial knowledge, presentation skills and an ability to deal with all kinds of customers are qualities needed to be a successful asic engineer in the UK. Technical expertise is taken for granted by companies looking for engineers able to provide clients with the best possible custom design every time.

The market for asics involves small-volume, crucial orders for chips made to do a complex job. An asic engineer needs to meet the customer's timetable for a product which can bear little similarity to previous work. And knowing the precise demands of the technology depends upon getting the information out of the user in the first place. A taciturn, shy or over-technical engineer will not find asics easy to work with because they bring you face-to-face with people as often as a workstation.

Libraries exist in a company's database to make asic work a little easier, but an applications engineer must have varied qualities, according to Alistair Greenhill, UK applications manager with NEC Electronics in Milton Keynes. "A definition of an applications engineer is a design consultant with specialist product knowledge", he said.

NEC runs a design centre for asics at Milton Keynes, with all its designs realised in Japan. The six consultants at NEC spend a lot of time with the customer. "You have to structure time on the road and assign yourself specific goals", Greenhill explained. "But the customer appreciates that the same person will support a design. Much of the selling is in support of technical issues."

Like other chip suppliers, NEC does not claim that it is simple to find all the right ingredients in an engineer for this task. "Many engineers know a great deal of detail, but it's difficult to get someone to take a step back and explain something clearly", said Greenhill.

Naturally the asic engineer must have a strong technical aptitude. Most applications-specific methodologies are digital – although analogue devices may be on the horizon – and so an engineer must be versed in this type of technology. Understanding how on-board chip systems work together, a good qualification in electronics engineering (usually to degree level) and software skills make up the profile of an asic designer.

Chip giant Toshiba operates a design centre in Camberley, and the company's marketing manager for asics, Michael Edwards, believes that the trick is having the broads skills to prepare a specification. "You could get a raw graduate to do an asic design with the right specification," Edwards said. "But people come out of university having done a gate design and talking about nanoseconds, yet not consider other factors like PCB tracking."

Getting the design right first time is the key goal at Toshiba. The ideal recruit going into the company will have experience of at least two or three asic designs to be able to meet quality and turnover standards. People from a systems engineering or partitioning background are also employed by Toshiba.

Strong commercial awareness is also required of the Toshiba asic consultant, who has to be conscious of the overall cost and performance of a project. Most of the engineers employed in the company's UK operation work on asics and Edwards reports the familiar problem that there are relatively few good people available. Toshiba makes c-mos gate arrays and standard cells, with a one micron process using 70 000 gates at the top end of its technology. Typical products fall in the 10 000 to 15 000 gate range.

Pushing the gate count up for larger arrays is beginning to reinstate older skills into the asic engineer's portfolio, according to Brian Knight, c-mos semi-custom marketing manager with Plessey Semiconductors in Swindon. "As complexity increases, typically into the 50 000 to 60 000 gate territory, you have to bring back the integrated circuit skills", Knight said. Computer-based libraries can only offer half the solution as there is no substitute for a working knowledge of issues such as clock line and where to place buffers.

To help keep the libraries up to date, Plessey has several software specialists based in the design team. These engineers also improve the software interfaces between the design workstations, such as Daisy and Mentor machines.

Unlike most asic suppliers with UK operations, Plessey makes its devices in this country. In addition to the design centre at Swindon, the company employs asic specialists at its Roborough fabrication plant.

"The Roborough asic people tend to be materials experts, working on die and wafer manufacturing processes", Knight said. Asic processors can need replacing every two years or so and another facet of this work is developing processes for the next generation of products. Shrinking the geometries is one of the main goals.

EXPERIENCE OR FRESHNESS?

Where most companies, such as Toshiba and NEC, seek experienced engineers for their design business, Plessey will also take on raw graduates with materials science qualifications. Around 10 percent of the engineers are graduate level. Plessey employs up to 100 people in total on the asic side, including engineers in the cad group. Some work is also carried on at the Oldham site, formerly Ferranti's semiconductor business.

One company to go for a blend of experience among its asic engineers is National Semiconductor in Scotland. "We take people at all levels from graduates through to experienced asic engineers", said Llew Aviss, personnel and finance director with National. "You have to take on graduates to get the right stock of trainees. Every organization has to take on this responsibility."

National employs 60 designers at its European centre in Greenock, working on designs for the world market in asics. Taking on engineers from industry has the advantage of adding experience to the company's collective ability, though these older engineers know nothing about how the organization works. With new graduates, what is lacking on the experience front can be made up for through easy adaptation to National's way of doing things, according to Aviss.

Most of National's engineers come from the North, usually because they did not want to go to the high-tech areas in the South. This factor gives the National workforce a great degree of stability, Aviss said. There is also the opportunity to move between divisions at the company, so that an engineer is able to get a vast range of experience.

Because of the acknowledged shortfall of young people over the next few years and a shrinking reserve of good technologists anyway, the companies are now addressing the issue of bringing graduates into asics more quickly.

"We are not yet taking on raw graduates, but we recognize we should be doing our bit to train them up", said NEC's Greenhill. It is nonetheless difficult to compensate for the obvious lack of experience in a fresh graduate. And asics represent one of the most demanding sectors in the industry.

Plessey's Knight calls the current labour scene for applications engineers a "seller's market" and admits it is not always easy to find the people. Plessey's staff tend to come from the South, and this regional recruitment emphasis compares to National's pool coming from the North where that company is based. One exception to this trend is NEC, which relocated to Milton Keynes from Scotland to be near its customers' base. Many of the engineers employed in Silicon Glen came down South. ■

DIY PLD

Brian J. Frost introduces PLDs that replace blocks of conventional TTL-type devices. To enable objective comparisons, it deals with their evolution, their differing technologies and their relative capabilities.

One of the first problems facing an engineer new to the subject of programmable logic is to identify what the term means. A "bingo card" ticked in the trade press advertising a PLD will bring a data sheet from one of 20 different manufacturers each supplying up to 50 different parts. In addition, the term is often used in connection with the vast subject of full-custom and semi-custom devices for which manufacturers offer complete design and layout services to your specification.

"Programmable logic device" is a generic term covering any device that can be programmed by the end user. There are a number of implementations of such devices in various technologies: for example, the abbreviation pal tends to apply to devices of a certain layout which use a metal fuse technology.

The attraction of PLDs is that your logic design can be written on silicon rather than shaped only by the numbering and pin connections of TTL devices — a capability that has always been within the reach of those who were prepared to pay for a semiconductor manufacturer to lay out a custom chip for a specific application. However, more recent is the concept of the end user programming a general-purpose device to achieve a specific logic function in a similar manner to the well-established technique of installing software in an eprom.

Users have been sluggish in taking to programmable logic, and for several reasons. Available devices have been slower than conventional logic, have required significant supply current, and have called for an investment not only in programming tools but in a changed way of thinking. But all aspects save the last have now been improved to the extent that they no longer constitute serious objections.

However, the changed thinking process is still required. This problem is akin to the revolution that swept electronics during the 1970s when microprocessors showed how sequential software instructions could replace dedicated hardware at the expense of speed. Logic designers had to realise that there was no absolute conversion from, say, a TTL D-type to a piece of software code. Following this sometimes painful learning process through, most engineers went on to discover vastly increased creative and equipment capabilities whilst appreciating those areas where hardware still remains indispensable.

Fortunately the new thinking process required for PLDs is not quite so radical, and is softened by the availability now of mature tools and examples. During my own on-the-job learning about PLDs I found that the only real hurdle was that of getting a feel for these new devices in terms of just how much TTL circuitry they can contain and how they actually do it. Once these mental tent-pegs have been hammered in, the rest, as they say, is easy.

First, it is necessary to realise that, at present, the popular pals rarely replace an entire TTL design, let alone with just one device unless it is very simple – like my logic probe (*Electronics & Wireless World*, September 1988, page 867). As I shall show later, the creative part of the design process is to replace only those parts of your design which lend themselves to it, and often to partition your design to suit it to the limitations of the PLDs that you wish to use.

PLD TECHNOLOGIES

Through sharing their development with memory technology, PLDs show many similarities. The first PLDs were based on early bipolar proms and used the same fuse technology, where the internal connections were defined by rupturing a very small fuse during programming. Devices based on this technology – such as the bipolar 16L8 pal considered in detail later – are still the most common in general use.

Reliability problems marred some of the very early products. Blown fuses were liable to grow back by metal migration under the influence of the intense electric field set up across the blown-fuse gap, but this has been cured by improved manufacturing methods and quality assurance techniques.

More recently, with the development of eprom technology, PLDs have emerged which can be erased by exposure to UV light and thus offer repeated erasure, programming and evaluation. As with eproms, this is ideal for the development cycle where a finalized design can be implemented with a non-erasable device after all changes have been made.

Erasable PLDs have been slow to emerge, however, since eprom technology has not been fast enough to produce logic devices that could compete with the established TTL families. With present IC technology this propagation delay limit has now been overcome, and present UV-erasable PLDs offer delays below 30ns.

Once these mental tent-pegs have been hammered in, the rest, as they say, is easy.

The most recent PLD technology to emerge is the eeprom technology where the device is electrically erasable as well as programmable. This has the advantage that reprogramming can be carried out within seconds and no labels need to be changed. Packaging the device costs less since there is no need for a quartz window.

Much data is now available on the electrically erasable "floating-gate" process that generates eeprom memories: it appears to hold the greatest promise for the wide acceptance of programmable logic in the future.

Many devices are also appearing in low-power c-mos form, with very low quiescent current and a power consumption pro-

Getting to grips with PLDs

Programmable logic assumes a greater importance in digital logic design as every day passes and is now being taught in colleges as a matter of routine. Often it is accompanied by the formal logic design that some of us may remember as textbook exercises but have had little cause to use since: rather, we have built up a practical experience of logic design using the elements of the TTL or c-mos families and we naturally think in these shapes.

This article aims to take such a reader on a walk through the subject of programmable logic with the intention of conveying a good engineering feel for its capabilities and limitations and building a bridge between existing TTL experience and new concepts without going deeply into logic design principles.

I shall also try to give some ideas of the trade-offs of the various applications, technologies and manufacturers involved, and low-cost means of getting started with your own designs.

portional to toggle frequency. By comparison, the bipolar devices are often quite power-hungry, with a 50mA requirement at 5V not unusual; but fortunately they are often used where a large enough supply current is available.

As a founder of the architecture of many of these newer devices the pal is a good starting place for a more detailed look at those PLDs work.

PAL DEVICES

PLDs have been around for many years in the guise of the simple bipolar prom represented in Fig.1. Input address lines (top left) are available as both true and complement forms. Using fixed links, they activate one unique And gate for each of the 16 possible input address codes. The activated gate places the contents of the user's programmed data fuse links on the output data lines via the Or gates and so to the outputs (top right).

A prom is generally regarded as only a memory device; but if its address lines are used as general logic inputs and its data lines as general logic outputs, obviously any dependence of the output states on an individual input code word can be programmed as a data entry into that prom location.

This coding is already partly done in the prom by the fixed addressed decoding that activates a unique And gate to produce a unique data word for each input address, leaving the user to program the data content of that word by "blowing" its fusible links. However, this fixed-address organization limits its use as a general-purpose logic element to only those applications with few inputs, since increasing the input quantity causes the device to grow physically large and slow.

In the mid 1970s, Monolithic Memories Inc. developed this architecture into that of the present-day pal (Fig.2). Here there are more inputs (top left), each made available in true and complement forms to a programmable And fuse array, but with a fixed output Or array. Here there is no intention to relate the inputs to the output in any "binary" manner and so this organization permits a large number of input lines on a physically small and fast device.

It may not yet be clear how the repeated array layout of Fig.2 leads to a flexible logic device, and so it is worth working backwards to this organization from a typical application. A very common requirement for TTL "glue" logic is that of address decoding for processor memory mapping.

A SIMPLE EXAMPLE

Figure 3 shows the memory map of three chips that are required to be mapped within a processor's memory space and to appear at the addresses shown. The example chips are an 8253 timer which has four registers, all to be "read" or "write", and two other octal parts, one output latch and one input buffer.

To keep the TTL solution simple, we shall assume that only eight low address lines ($A_0 - A_7$ inclusive) need decoding. One such TTL solution is shown in Fig.4 and uses one 74LS138 three-to-eight line decoder, and a 74LS139 dual two-to-four line decoder.

This design would function correctly, but has the peculiarity that the octal chips can be read and written at higher addresses as well as those intended, although this redundancy from $1C_{16}$ to $1F_{16}$ usually does not matter. Possibly more of a problem is that the 74LS138 can only select one of eight possible input combinations and so there are many addresses for which this TTL design cannot be used; it is clearly not a general solution. Of course a truly general solution could be bought at the expense of octal comparators and/or greater circuit complexity.

Let us examine how this same requirement would be met with a pal.

At this point clear your mind of the TTL implementation, since the problem can now be examined in a fresh way without the constraints of available TTL functions and pinouts. To start with, some simple rules are created that define the control signals of our three chips in terms of their dependence on the address lines.

Firstly the 8253 timer. We know that address lines A_0 and A_1 go directly to it and are not decoded for its address selection. Inspecting the memory map, we can see that it is required only at addresses 18 to 1B, and writing these addresses out in bit form shows a fixed pattern of

A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0
0 0 0 1 1 0 X X

where A_0 and A_1 are shown as "don't care" because they control the chip directly. To select the 8253 over these four addresses then, it is only necessary to provide a line that goes low when the pattern above appears on the six lines $A_2 - A_7$.

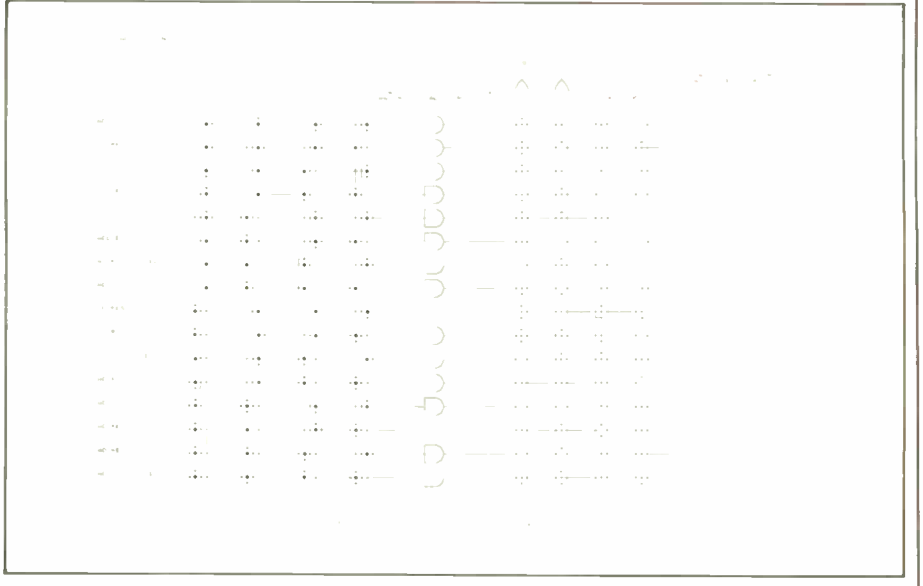


Fig.1. Prom architecture: one type of programmable logic device.

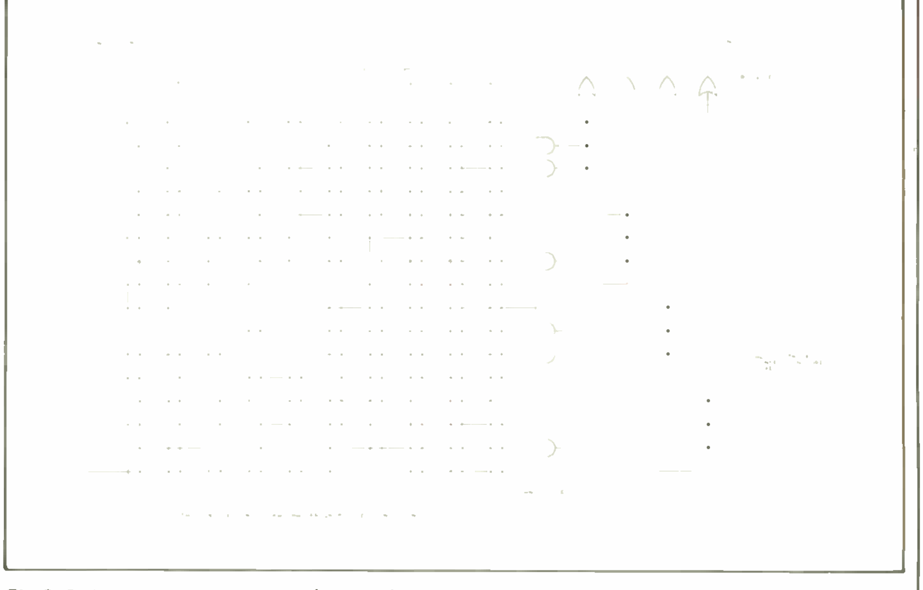


Fig.2. Pal architecture. Inputs (top left) are available in true and complement forms to a programmable And fuse array. There is a fixed output Or array.

Fig.3. This address decoder memory map can be implemented in a pal without the pecularities such as address redundancy shown by the TTL implementation of Fig.4.

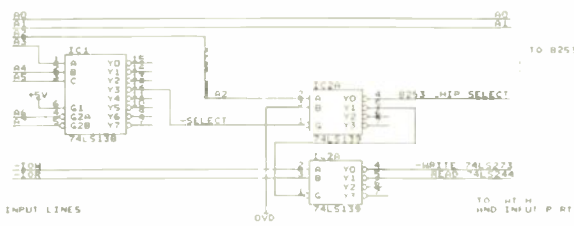


Fig.4. TTL implementation of the address decoder has about twice the propagation delay of the pal version.

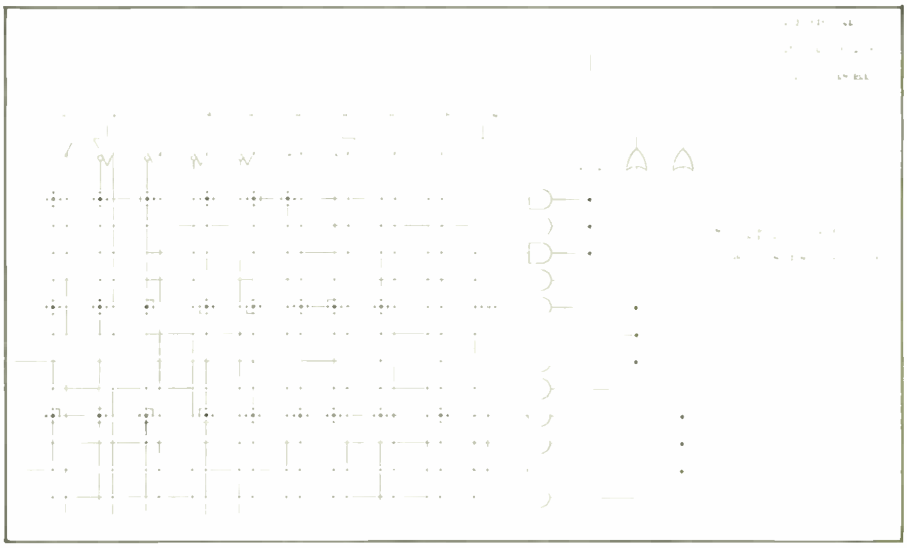


Fig.5. Address decoder using a pal.

Figure 5 shows the organization of a pal taken from Fig.2 but with our address and read/write lines connected to the inputs and the device chip selects connected to three outputs. For the 8253, the top And line is programmed to be joined to the inputs in such a manner that all the junctions are true – and the And-gate activated – when the address inputs are the required select pattern 000110 ($A_7 – A_2$). This output then becomes the 8253 chip select.

For the input buffer and output latch the situation is very similar, except that in these cases the full eight bits of the address, plus the read or the write line, are used to define the device chip select. The output latch clock is required when the input pattern:

$\overline{IOW}$	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	1	1	1	0	0

exists. This is shown coded as array links in the centre of Fig.5.

The input buffer is very nearly identical to this, with its enable signal active for the pattern

$\overline{IOR}$	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	1	1	1	0	0

and occurring on a read operation, instead of a write. This pattern is shown at the bottom of Fig.5.

With these patterns programmed into the one pal device, usually by selective blowing of tiny fuse links, the device will function as an address decoder with exactly the characteristics required by the map in Fig.3 and with no peculiarities such as the address redundancy I mentioned for the TTL design. In fact the pal provides other advantages too. Not only can it easily be altered to generate a completely new address for any of the three chip selects, but it has a propagation delay for the input and output ports that is about half that of the TTL solution shown.

DESIGNING WITH PALS

This address decoder example is straightforward because address decoding fits quite nicely into the architecture of pal devices. Since the correspondence is so close, it has been possible here to generate the required fuse descriptions simply by inspection. This simply-to-generate fuse map would at one time have been followed by an equally simple programming method where the device was programmed by manual toggle switches and a "zap" button, but now there are new software tools to provide both design and programming support.

The designing and the programming of a logic device remain quite separate tasks in much the same way that an eprom is programmed after software has been written and compiled, with tools available for each task. The logic design tool, or logic compiler, is used like a software assembler and allows the designer to specify equations in the manner outlined above and using real names for signals. For example the 8253 chip select line might be entered for compilation as:

8253_select = !A7&!A6&!A5&A4&A3&!A2;

This notation is taken from the CUPL PLD logic compiler where! means active-low and & means And. The line can be read aloud by the interpretation

8253_select is true when A7 is low,
and A_6 is low,
and A_5 is low,
and A_4 is high,
and A_3 is high,
and A_2 is low.

Again as with software assemblers, a feature of logic compilers is that they permit device pin numbers to be given names such as

pin 19 = !8253_select;

which means that pin 19, an output pin, is defined as "8253_select" and will go low when true. This is a very convenient feature when pin numbers are re-assigned later to suit a PCB layout.

Device logic equations typed in this manner, together with information about the device type, provide the logic compiler with enough information for it to check that your design fits within the device, and that your pin number requirements are legitimate. If not, some compilers can suggest alternative PLD devices – but more about the compilers and their features later.

Assuming a successful compilation of your design, the compiler provides you with a specially formatted "JEDEC" file, which is simply a defined method of specifying to PLD programming equipment exactly which fuses must be blown in the device. This file looks very similar to the crosses on the pal fuse map in Fig.2. This JEDEC file is loaded into the programming equipment and the device is blown, checked and is ready for use.

continued over ▶

SIMULATION

Many of us have been involved with eprom-based software and few have not had that sinking feeling when the new software eproms are plugged into the PCB and nothing works – and yes, they *are* in the correct way round. The same problem can affect PLDs. For example, you program the device, the programming equipment verifies that the device has programmed correctly and it agrees with the JEDEC fuse map file. Yet when you use it, the PLD does not operate correctly. Worse, design faults can be rather more difficult to diagnose within a PLD when it is in circuit than with software in an eprom.

To avoid this problem, tools have evolved which enable the PLD design to be simulated before the device is actually programmed. This allows even very complex designs to be exercised at an early stage, it avoids the need to diagnose design faults at the hardware level and it provides an even higher level of confidence during device programming.

It is not essential to perform a simulation on a PLD device. Nobody will stop you from simply typing the previous address decode equations into a logic compiler and programming a device – it will quite likely work! However, experience teaches us that fast and accurate "worked first time" designs are more often those designs that have been simulated as a matter of course – the method used by the processor and gate-array designers – and let's face it, if the design is a doddle, the simulation is going to be pretty easy too.

SILLY MISTAKES

To simulate a design, you construct another "simulation file" alongside the file that contains your actual device design equations. It contains 1s and 0s to represent your inputs, and blanks to represent your outputs. You run this file though the logic compiler together with your design file and it produces a "simulation output file" of the output pin states for you to inspect. In this way it acts as though you had actually connected up your programmed device using toggle switches and leds and had monitored each output whilst running through the required input patterns. However, from these simulation results, silly mistakes (such as getting a pin definition inverted) are easily spotted.

More complex mistakes such as incorrect device logic operation (possibly because an equation has been typed incorrectly) are also evident by inspection. Most logic compilers also allow you to specify what you expect the output states to be. Should this not agree with the simulation result, an error message highlights the error.

Not only does simulation greatly raise the confidence level surrounding a new design, but it adds confidence to the programming process too. If such a simulation has been performed, the JEDEC fuse file that will be sent to the programming equipment contains additional data termed "test vectors". These are one-for-one copies of the 1s and 0s that you specified during your simulation togther with the expected PLD output states, and they are loaded into the programming equipment together with the fuse information. After the device has been programmed, the programming equipment compares the device fuses with the JEDEC fuse information to verify correct programming (although of course this does not check for correct functioning of the logic).

Successful completion of the test vector check gives a very high degree of confidence that the programmed device will perform in the final circuit as intended. These tests are so comprehensive that any subsequent PLD fault must either be related to speed or be evident simply by re-inspection of the design or simulation listings.

Part 2 next month

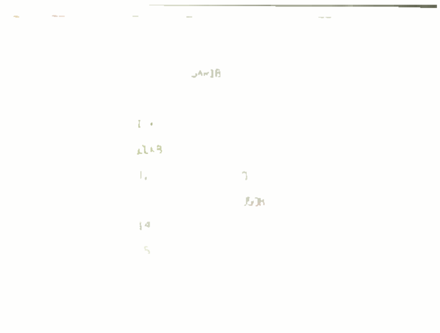
Designing on screen

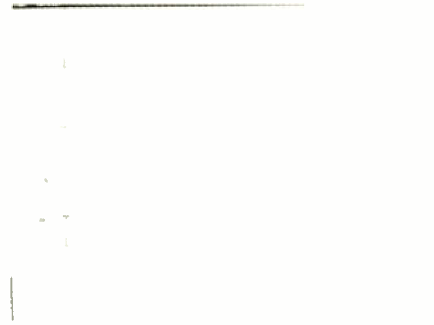
Without the right software, even the best asic process is useless

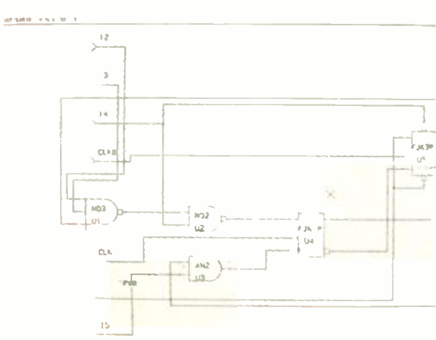
The key to providing support for engineers who need to develop a complex asic is a cad environment with training and good application backup. This enables the engineer with little previous experience to undertake simulation, layout, testing and even package choice of a highly specialized device.

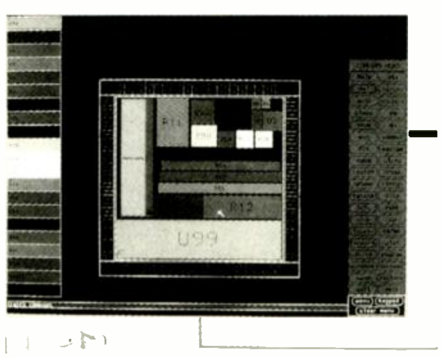
In LSI Logic's case, most of the design tools are part of a software system called LDS. This software runs on most work stations including Sun 4, Vax and Apollo, and is available at design centres throughout Europe. Some large asic users run the software at their own location.

These photographs take you through the stages of designing an asic using LDS. Normally, devices like the successive-approximation register shown here would normally be called up as a module but it is here broken down to gate level to give you an idea of what is possible.



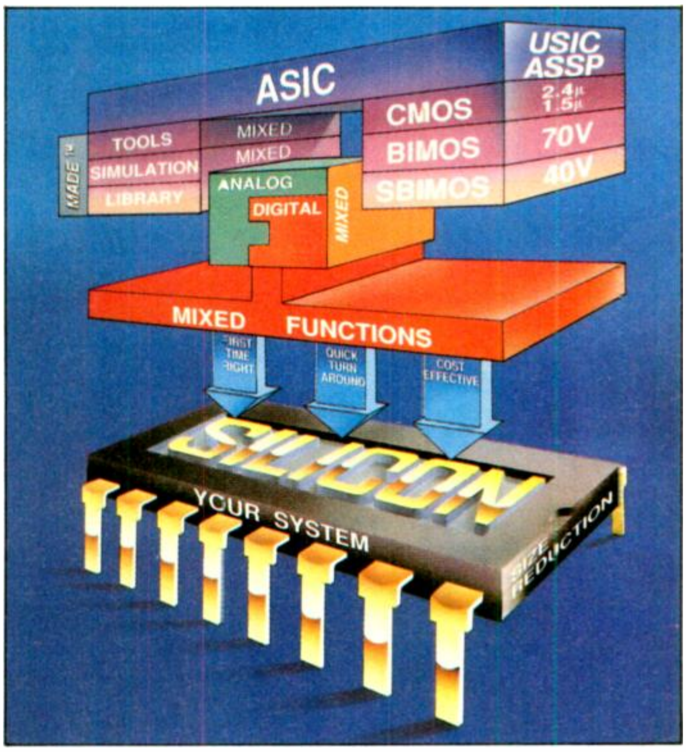






Flexible entry-level for mixed analogue/digital functions

The best asic processes should be able to accept many types of input data but the appropriate customer training should be given says John Umney of Mietec.



In assessing the capability of an asic manufacturer, it is important to judge companies against a number of criteria – available technologies, cell libraries, simulation tools, production facilities, and turnaround times. Training is also an important element. In each of these areas Mietec say they can demonstrate leadership.

TECHNOLOGY

Committed to mixed-mode analogue /digital design and production, Mietec's technology capabilities are concentrated on c-mos for low-power and high-density applications in 2 and 1.5 micron bimos, which combines the best features of c-mos and bipolar technologies on the same die, optimised for high voltage applications, and standard-cell bimos, a multi-purpose technology. Each is supported by an extensive cell library of analogue and digital cells, macroblocks and software-generated cells such as ram, rom and switched-capacitor filters. Each predeveloped cell is optimised for area, speed and electrical characteristics resulting in a reduction in unit costs over gate arrays whilst maintaining comparatively low development costs and a relatively shortt development schedule.

The Made* cad system which includes a proprietary, true mixed-mode simulator, provides a highly-structured design approach which eliminates errors in translating a design into silicon. Once the schematic has been captured or the network listing entered, the system will ensure that the circuit that is simulated is the circuit that will be fabricated, through on-line checking and by passing data from one module to another using a central database.

* Mietec Analogue and Digital design Engineering software.

ENTRY LEVELS

Mietec offers a flexible entry-level structure into mixed-mode asic. If you already have integrated circuit design capability, Mietec can supply libraries and simulation systems free of charge for use on Daisy, Vax and Unix machines. Alternatively, simulation can be accessed by an X25 link to the Brussels-based design centre. If, on the other hand, you have a requirement for integrated analogue/digital functions in on asic, but require Mietec's design expertise, the company works from your initial design specification.

TRAINING

Training courses, ranging in duration from three days to four weeks, are available at the Brussels Design Centre. The three-day introductory course presents the Made system and covers topics from semi-custom libraries, mixed-mode simulation, layout tools and compilers, with work on practical examples. The complete four-week course, working alongside experienced circuit designers, allows the design engineer to complete the first part of a design as part of the training.

COST CONSIDERATIONS FROM DESIGN TO PROTOTYPES

The cost of producing silicon normally depends on the complexity and functionality of the final device, but balanced favourably against the potential benefits of savings on usable board space, system security, functional integration, product reliability and so on. At the same time, however, Mietec offers a low-cost prototyping service to eliminate commercial risk considerations. Through an agreement with Invomec, a division of IMEC, recognised as one of the leading research centres in microelectronics, customers will receive 20 packaged prototypes for a total cost of about £2,000. From customers' tapes and using Mietec's fabrication facilities, IMEC schedules a multi-project chip every two months, ensuring delivery of prototypes within about 12 weeks.

Mietec's own prototyping facility will reduce timescales to about eight weeks. Prototypes are normally supplied in ceramic dual in-line packages whilst production devices are available in JEDEC-standard packages, surface mount, plastics and ceramic chip carrier packages in a wide range of pin counts.

APPLICATION-SPECIFIC STANDARD PRODUCTS

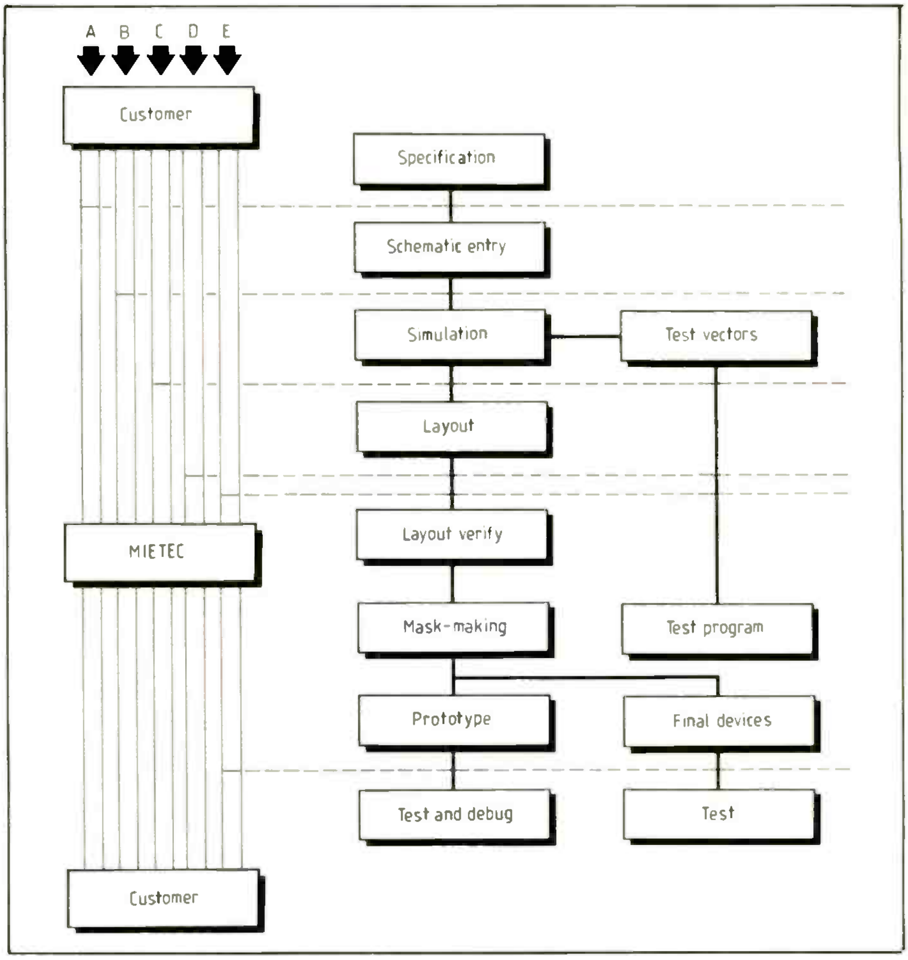
In addition to custom-built integrated-circuit services, the company can also offer a number of devices for off-the-shelf delivery.

Mietec offers its highly flexible entry-level for application in the world of mixed analogue/digital asics, as depicted in the diagram. If you are a company with internal IC design capability (entry Levels B to E), or a company with a requirement for integrated analogue/digital functions in one asic, but require Mietec's design experience (entry Level A), Mietec can accommodate your needs.

These standard products are devices which address specialised applications in a variety of fields such as telecommunications and light industrial control. Such devices considerably reduce design cycle times and are available in any quantity with short delivery times. Examples of standard products include interface circuits for ISDN, a thermal printhead driver, and stepper motor driver/controllers.

Mietec's focus is on those application areas which most strongly benefit from the technologies and design tools available – the automotive, general industrial and telecommunications sectors. This activity is supported in the field with sales offices in Paris, London, Munich and Brussels where expert commercial and technical advice is available to customers.

Mietec was set up in 1983 by Bell Telephone, Alcatel and Flanders Investment Company. Its UK sales office is at Easthampstead Road, Bracknell, Berkshire RG12 1NF, tel. 0344 53974.



TEN STEPS TO ASIC

Tips and a ten-step guide for potential asic users from Mike Inglis of Texas Instruments.

Expense, particularly the initial cost, is a major concern for newcomers to asics. So is the efficacy and user-friendliness of design tools: the amount of extra knowledge needed to gain maximum benefit; and the degree of control over design-to-production flow. But the first questions designers can ask may be even more fundamental: "How do I decide which asic route is best?": and "What do I need to get started?"

The answer to the 'best asic route' question hinges on volume and complexity. Even small-volume devices can take cost-effective advantage of asics if they are complex. Similarly, asics may still be the best technology at very high volumes if the gate-count is low, and especially if fast turn-around is required.

Gate arrays are generally appropriate for circuits with hundreds to thousands of gates, in volumes up to 50 000. Above this, a standard cell may be the solution, or at very high volumes (200 000-plus) the full custom route may be attractive.

FIRST STEPS

Naturally, the definition of these edges is somewhat blurred. Asic vendors will give advice, but to do so they need the best information about the circuit under consideration. The first question they will ask is: "Why are you doing the design in the first place?" This is an important, if obvious, question, because it affects how the circuit should be optimized, and which technology should be used. A cost-saving design needs to minimize silicon, a performance improvement to reduce gate delays, whilst a space reduction may be needed to keep packaging options open.

The second question is: how suitable is the design for asics? Whilst any primarily digital circuit with more than 100 gates is suitable to be implemented in asic, elements such as advanced logic devices on-chip will require early attention.

Similarly, it is important to identify critical paths, so that conformance with the intended specification can be ensured.

All these can be discussed most sensibly if a clear circuit diagram is available. This will help also in the initial estimate of circuit size. There are two aspects to this: gate count and I/O requirements.

It is fairly simple to do a rough gate count, either direct from data sheets of the various components, or from figures of transistor equivalents. A two-input Nand gate corresponds to around four transistors. Don't forget to add 10% to the final figure – extra gates are often needed during the course of a design.

In estimating the number of inputs and outputs, it is important to remember physical considerations such as V_{cc} and ground.

It is also helpful to have some feel for whether the design is likely to be core-bound, with logic area dominating, or I/O bound with many inputs and outputs. Another important factor is what parts of the core the I/O need to communicate with.

System speed is of course a consideration, for upon it hinges the choice of technology, geometry and so on. Current asics are unlikely to be helpful for very fast circuits, above 200MHz.

Packaging is a key issue because not all asic dice will fit every leadframe or package. Early identification of the package can avoid later problems.

It is equally important to provide information on commercial requirements – target price and projected volumes. Asic vendors are well-used to receiving guarded answers to this question, but they will always respect commercial confidences and write them into joint development contracts. For this reason, it can be helpful for designers to enlist the support of senior management, and involve them in discussions with the asic vendor.

TEN POINT ASIC CHECKLIST

- **Why do the design?**
- **How suitable is it for asics?**
- **What are the critical paths?**
- **How clear is the circuit schematic?**
- **How complex is the circuit?**
- **How many I/O does it have?**
- **What is the system speed required?**
- **What kind of packaging is best?**
- **What are the commercial constraints?**
- **What production volumes do you expect?**

Asic without fear

The semiconductor industry now has an asic process for almost every conceivable tradeoff between development cost and delivery volume. The advent of friendly software tools has made nearly all of them easier to use says Adrian Hudd of Austria Mikro Systeme.

Ever since the first commercially available transistors, engineers have wanted to include greater and greater functionality into their products. The availability of more complex standard parts and techniques has gone a long way to advance this.

With recent developments in technology it is possible to include not just simple logic but microprocessor, memory, complex functions and even analogue functions onto a single silicon chip. The techniques required to extract and reproduce the function of a custom integrated circuit are out of reach of all but the most tenacious competitor, to the extent that such an exercise is rarely economic. Nothing is perfect; even asics have a few disadvantages. Initially, their use requires a high level of commitment both financially and technically. Also, the customer often gets the impression that when the design reaches the manufacturer, he loses contact over costs and time scales. Panic not! Savings are usually evident when the project reaches the production stage. Just as important, engineers, particularly those who have only limited electronic systems design experience, often feel that to use an asic will require a level of design expertise they do not possess.

Hardware and software tools are so well designed that the vast majority of the design tasks are hardly different from designing a system for implementation on a PCB.

AMS feels that it has contributed particularly to this area. Super SCEPTRE is a complete low-cost system that can take a design from schematic capture through to logic simulation and place and route for standard cells. It can also go to the validated netlist stage for gate arrays.

Spice SCEPTRE is essentially the same package but with the inclusion of P-SPICE from Microsim. This means that analogue as well as digital circuitry can be designed at the transistor level and simulated prior to the start of any layout work.

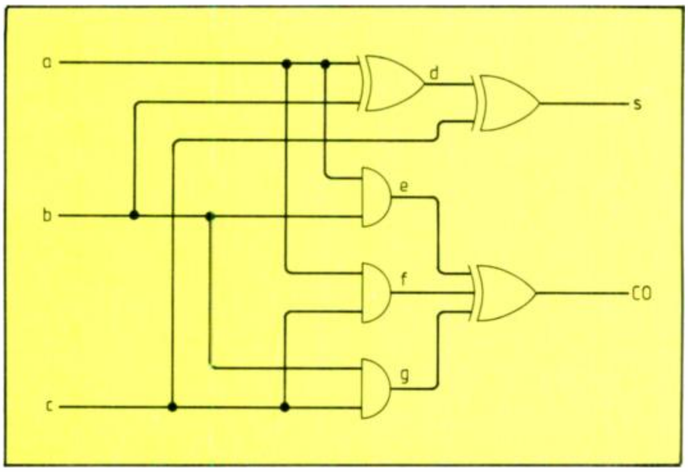
Another area of concern among potential users of asics is the risk involved should the chips not work or be seriously delayed. This stems to a large extent from the early days of asic technology when the quality of both the design software and the manufacturing process was often found to be wanting. The fact that thousands of designs are completed every year with no problems at all stands as testament to the maturity of this technology. This puts the probability and delays at the level of those experienced when using standard products, with the added advantage of the design carried out by the end-user himself.

The term asic can be applied to a wide range of device technologies ranging from simple programmable devices like the prom or PLA to highly sophisticated and specialised chips designed for use in calculators, digital watches or electronic ignition systems. The most common asic architectures are explained in the following paragraphs.

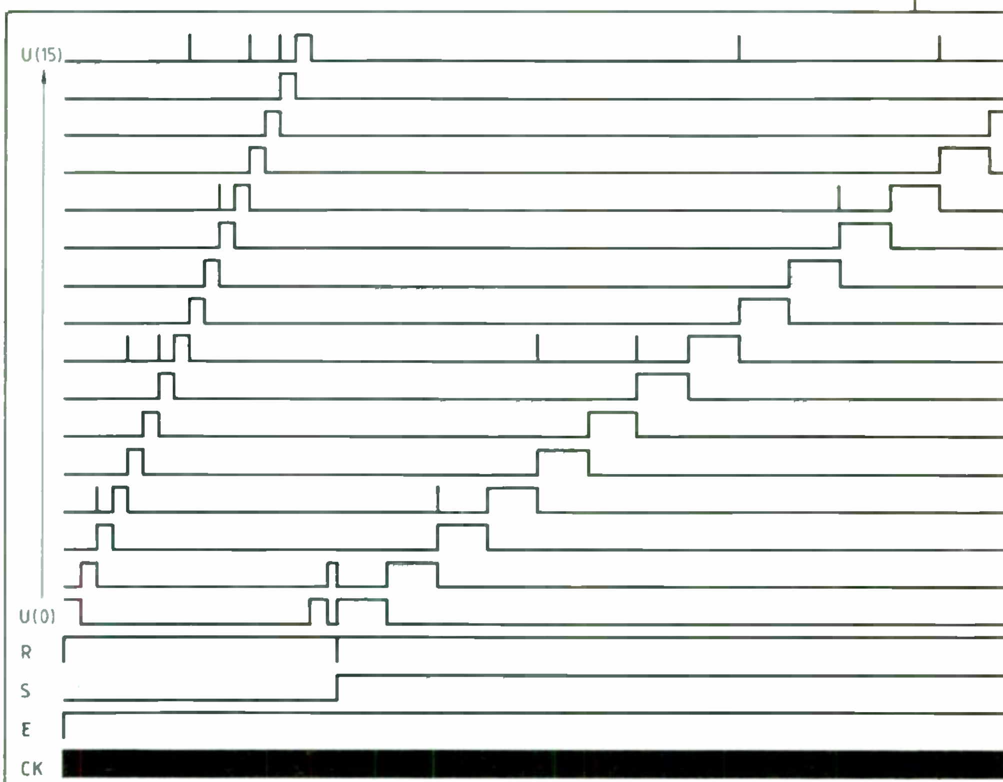
Gate arrays, standard cell and custom ICs comprise the three major types of asic. All can deliver real benefits but each has tradeoffs in design flexibility, development span, development cost and production prices.

Gate arrays have a fixed architecture which typically consists of pre-designed rows of uncommitted logic gates separated by interconnection routeing channels. For a given array size, these base layers are identical for all applications. The only difference from one application to the next is the metal interconnections between gates.

Biggest advantage of gate arrays is the short development time compared to stan-



In the old days, logic design software required data entries in the form of Boolean equations so design engineers used to dealing with logic symbols were frightened off. Now, schematic capture is almost universal.



ASIC simulation results are displayed as waveforms.

dard cell circuits and cell-based custom circuits. Through using common base layers, gate array wafers can be partially fabricated prior to customization for a given use. Once the logic is defined, metallization is all that need be carried out.

Standard cells are really circuit building blocks which have been previously designed, characterised and subsequently stored in a computer data-base. Cells can range from simple digital circuit elements such as logic gates to more complex digital sub-systems such as ALU, uart, CPU, PLA, ram and rom memory cells. The cells can also include basic analogue circuit elements such as operational amplifiers and comparators, as well as the even more complicated analogue sub-systems, such as ADCs and switched capacitor filters.

Because each standard-cell integrated circuit requires a unique fabrication mask set, the development cost and time spans are higher than gate arrays. However, standard cell circuits offer significant advantages in unit pricing, design flexibility, circuit performance and analogue and digital functional capabilities.

Compared with optimized full custom circuits, standard-cell circuits offer lower development costs, reduced development time and a greater probability of first-time IC success.

In exchange for these benefits, the production unit prices of a standard-cell circuit are slightly higher than those of a comparable optimized custom circuit.

Within custom design, cell-based custom design has largely replaced full-custom design, which requires that each transistor be individually designed and manually connected to the rest of the circuit. In a cell-based approach, only critical parts of the circuit are designed in a full custom mode for particular applications, while a major part of the design consists of previously available standard cells.

Advantage of cell-based custom is that optimum performance and minimal die sizes can be achieved while minimizing design risks, development costs and development time compared to a full custom circuit.

By deciding on a cell-based asic, a system design engineer needs to pay for high performance only where it is required. In other portions of the circuit, pre-designed standard cells are used to obtain the desired reductions in cost and development times.

The technologies described so far involve the function of the asic being defined in the factory by the supplier; by contrast, programmable devices are all manufactured to the same specification and have their function defined on a designer's bench.

Recent developments in the architecture of electrically programmable devices have broadened the range of the applications for which this technology can be used. The earliest form of EPLD was the prom (progammable read-only memory) but a much higher degree of logical functionality can now be obtained by the adoption of more advanced architectures. These are similar in many ways to the gate array but with the interconnections made by electrically fusible links.

The availability of high powered software tools such as the SuperSceptre package shown here has brought down the cost of entry into asic design.

Such devices are now capable of replacing sizeable amounts of standard logic in a form that can be programmable via a personal computer in a matter of seconds. This means that the design can be evaluated and changed many times very quickly.

BEGINNING A PROJECT

A number of design consultancies around the country have links to one or more asic suppliers and are experienced and equipped to evaluate your design. They will be able to carry out all the necessary work for you, starting from either a basic functional description of the required part or a more complete specification, including schematics and a test program. Beware! Make sure the design house fully understands the application area in which you are working.

An alternative approach is to do the design work yourself. This will require both training and access to a design system. Both of these can be provided by the asic supplier you have chosen (possibly with the help of a consultant in the early stages) and this has the advantage of giving total control over the design cycle.

Many suppliers of asics or their distributors provide on their premises design facilities which can be hired by the week. Most will be more than willing to talk about ways of spreading the cost of your project to suit your budget.

Attending a training course is a great idea. As some training schedules give you the chance to make a start on a design during the course, it may well be worthwhile having your design evaluated before the training starts. In this way you can ensure that the general concept, partitioning and implementation are suitable. This allows time for you to make changes before you start in earnest.

Using asics in project prototypes requires a slightly different approach to project management from conventional techniques and allowance should be made in the project plan for the time required to complete the design, plus a possible over-shoot and then the manufacturing time of between four and twelve weeks before the prototype chips are delivered. This may be followed by a further, similar time period for the manufacture of the first production units. Some suppliers offer fast delivery times for a higher price and it is worth knowing whether such an alternative is available, particularly if you have tight deadlines to meet.

Multi-project wafers provide one method of reducing time scales and costs. AMS calls its version "shared silicon technology". The company's multi-product wafers (MPW) allows the parallel processing of several devices on one wafer.

MPW development charges are reduced by about 50 percent through reduced mask and fabrication costs. Furthermore, MPWs allow, for very little extra cost, the parallel study of design options which lowers the risk of redesign.

Until recently asic technology has been out of reach of many smaller companies because of cost and the required levels of expertise. This has now changed, and with the latest generation of CAE tools and modern low-cost workstations, the use of asics can be justified for even relatively simple projects. Never before has such powerful technology been so accessible to the small business. ■

Gateway to semi-custom

Before jumping into asic with both feet John McNally of Philips suggests a few questions that all prospective users should ask themselves

There are three major reasons why designers are discouraged from semi-custom. One is the perceived cost, the second is a fear that the devices, when delivered, will not work in the circuit and the third is that a company may not consider that it will want enough devices to make the choice of semi-custom cost-effective.

The first two reasons are closely linked. Devices which don't work in the circuit may incur more cost to the user as a second attempt is tried. However, the chances of devices not matching the simulation is very small. As for the third, as silicon geometries become smaller and silicon wafers become bigger then the number of good dice in a production batch become, larger and minimum order quantities will, therefore, increase.

The cost reason seems uppermost in smaller companies; device problems dissuade the larger companies. Programmable logic allows a move into semi-custom fairly easily and without a great deal of cost.

Programmable devices can be split into two main categories. The term 'programmable logic device' is used mainly to cover smaller devices with complexities of up to about 1000 gates; the term 'programmable gate array' includes devices with gate-equivalents from about 1000 gates to currently over 10 000. One gate-equivalent corresponds to one two-input nand gate. Two input gate-equivalents are used with accuracy in gate and cell arrays but should be treated with caution when associated with programmable devices.

Programmable devices normally have multiple-input gates, which could be counted as N inputs divided by two equivalent gates, but if one multiple-input gate is used as an inverter then all the other inputs are lost to the user. Similarly, a D-type flip-flop in a gate array can be counted as between six and twelve gates and could be used as individual gates if a D-type is not wanted, but in a programmable logic device it must be used as a D-type. Since there is no other easy way of telling relative sizes of programmable devices the safest way is to ask the programmable gate array manufacturer what size and types of circuits can fit into his devices.

A company considering a programmable gate array as a prototyping device should ensure than an easy migration path exists from programmable gate array to masked gate or cell array. This may be difficult because most programmable gate array manufacturers do not make masked gate arrays. Therefore, after designing and prototyping with the programmable gate array the designer will then have to transfer his design to the design tools of the masked gate array vendor. These tools may involve different hardware and most certainly different software to that of the programmable gate array manufacturer. Also the circuit being transferred may have to be redefined to suit the architectural differences of both types of device with the added possibility of errors creeping in.

If migration from programmable to masked gate array is considered it makes sense to choose a vendor who makes both sorts of device.

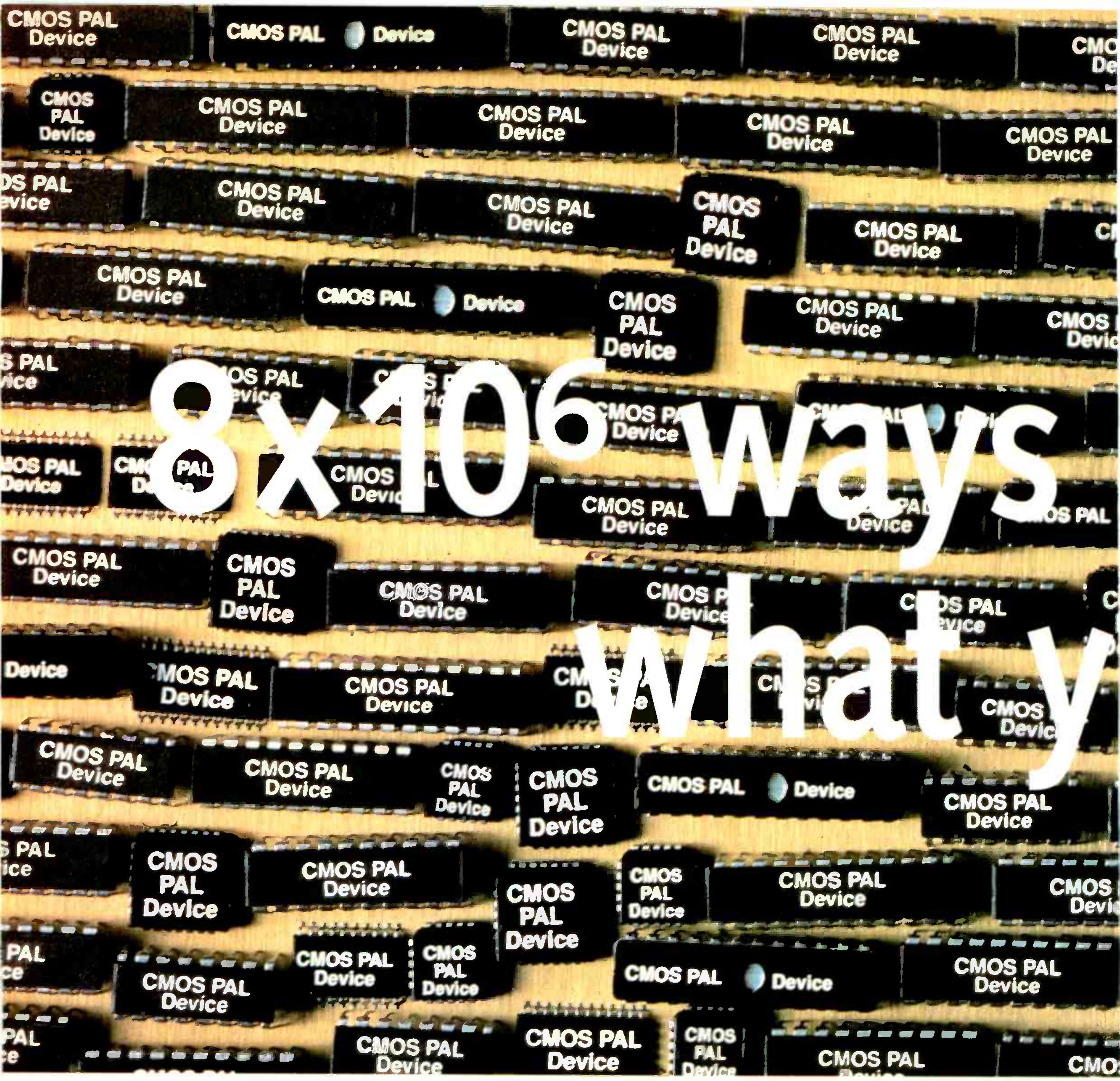
Production testing of TTL does not usually enter the designer's mind. However, gate arrays and higher complexity PLDs such as sequencers, which have buried registers and multiple feedback paths, do require specialised testing.

Fault grading provides an effective test basis. Each node is stuck at zero and then one in turn, and the simulation run to ensure that the effect of the stuck node can be seen on an output. After all nodes have been stuck at both levels the fault grader will then show the degree of testability as a percentage of the total number of indicated faults. It will also show which nodes are testable and which are not. The designer can then modify the design, test logic or stimulus inputs to increase the test coverage of the circuit. A gate array vendor who has a fault grader in his software should be considered for complex circuits.

Potential users of programmable gate arrays should know the limits on toggle rates. The rate specified is a measure of how fast a D-type flip flop will toggle when its Q output is fed back to its D-input. However, since most circuits comprise more than just toggle flip-flops and have logic gates between the flip-flops, the maximum system speed is usually very much slower than the specified toggle rate. It becomes more complicated when the routeing between gates is not fixed and has to be generated by the software. The lengths of the interconnections can greatly affect the propagation delay through a circuit.

As with masked gate arrays, programmable gate arrays, where the interconnection is not fixed, have a finite number of routeing channels. This leads to the problem where not all the gates in a device can be used because insufficient routeing channels are available. Other types of programmable gate arrays have fixed interconnections where every gate is connected to every other gate in the virgin device. In this type of device every gate can be used. ■

High volume gate arrays rely on on a one or two layer metalisation to effect the customisation. These photos, taken at LSI Logic's Sidcup facility, show some of the manufacturing steps



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ENTER 34 ON REPLY CARD

Multi-standard MAC decoder

Philips, Plessey and Nordic VLSI are now well advanced with their multi-standard MAC decoder. The first silicon from this co-operation has been producing pictures and sound in Philips Components' applications laboratories at Mitcham.

MIKE BRETT

Current work on the design centres on checking the second round of silicon, which is generally operating fully satisfactorily and will form the basis of large-scale production of integrated circuits in the second half of this year.

This decoder is aimed at maximum flexibility. It is compatible with the two adopted European MAC systems (D and D2) as well as with C-MAC, and also with both Eurocrypt and Eurocypher encryption techniques.

Processing of the vision, sound, and teletext/data parts of the transmitted signal is assigned to physically separate ICs; this architecture means that capability can be extended as necessary. For instance, one MV1730 sound chip permits two sound services to be obtained (where each could be either a mono or stereo transmission). A second device may be clipped on to the end of the packet bus to obtain a further two sound services if transmitted.

The decoder uses the output from the receiver's F.M. demodulator as its input. The time-multiplexed MAC signal is applied to the video and data inputs of the TDA8734 "MACAN" IC via low-pass filters (8.4MHz, except for D2-MAC data, which is 5MHz). From this point on, the signals follow separate paths.

The video signal is grey-level clamped and AGC adjusted in MACAN. The AGC action is based on measurements of the data signal amplitude, and a further fixed gain trim is possible to match the absolute value of the video signals to the a-to-d conversion which follows.

Clock timing information as well as clean sliced data are extracted from the data part of the multiplex within the same MACAN IC. This process is rather more complicated than it might at first seem, because both binary and duo-binary modulation may be encountered depending on the standard being received. A 40.5MHz master oscillator on the IC is eventually locked to the incoming sliced data, and its output is divided and buffered to provide outputs at 10.125 and 20.25MHz which are used as clocks throughout the rest of the decoder.

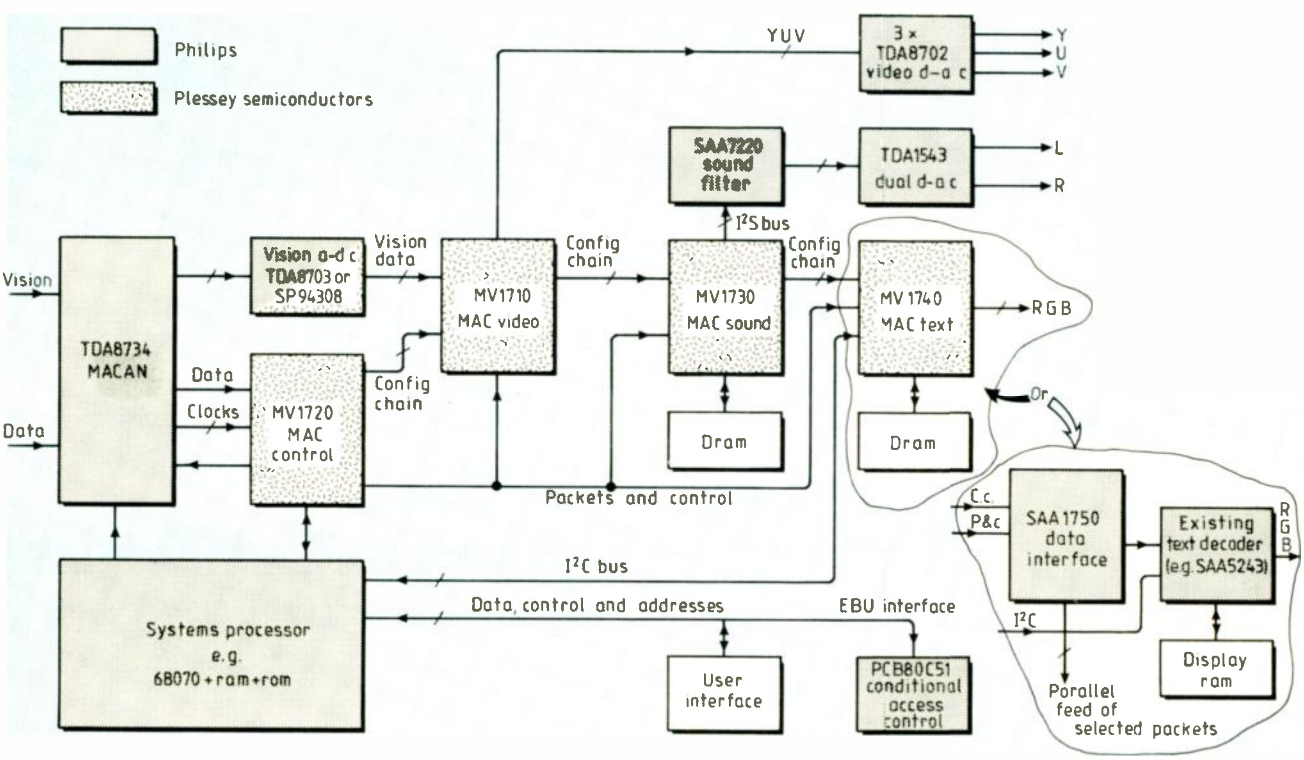
VIDEO PROCESSING

Video information (a chrominance signal followed by a luminance signal, occupying together nearly 54 μms of each television line) is next converted into the digital domain by sampling at 20.25MHz in the TDA8703 a-to-d convertor. The eight-bit data is received into the MAC video IC MV1710 as 349 and 697 samples for chroma and luma respectively. They are stored in ram in different sequences, depending on whether the transmission is scrambled or unscrambled.

The cut-and-rotate method of scrambling defined by the EBU MAC specification makes descrambling straightforward matter. You merely write to this ram from a different starting point in each line: straightforward, provided you know these different points! The re-recorded luma and chroma data can now be time-expanded by the simple ploy of clocking the data out towards the display device at a slower rate than it was clocked in.

Video expansion can be arranged in the device to suit either the existing 4:3 aspect ratio display devices or the 16:9 options for the future. To enable feature films to be broadcast from the start of services in the wide-screen format, it is possible for this decoder to respond to panning vectors sent within the data signal which determine which part of the 16:9 picture you see on your 4:3 present-day tv. The process can be

Half-Eurocard laboratory evaluation layout of a multi-standard MAC decoder.



compared to that done when optical prints of wide-screen films are created for tv today.

Some interpolation of the chrominance information is required before it may be used, because each line of chroma contains only one half of the necessary information (i.e. U on odd-numbered lines, V on even). This interpolation is done within the MV1710 before the three streams of Y,U,V data are fed out to the D/A convertors. After some simple filtering and buffering, analogue Y,U,V signals may be taken away to a conventional video control combination as already used in colour receivers. Alternatively, depending on the nature of the complete equipment, it may make more sense to convert to RGB before feeding the signal away, perhaps via a SCART connector.

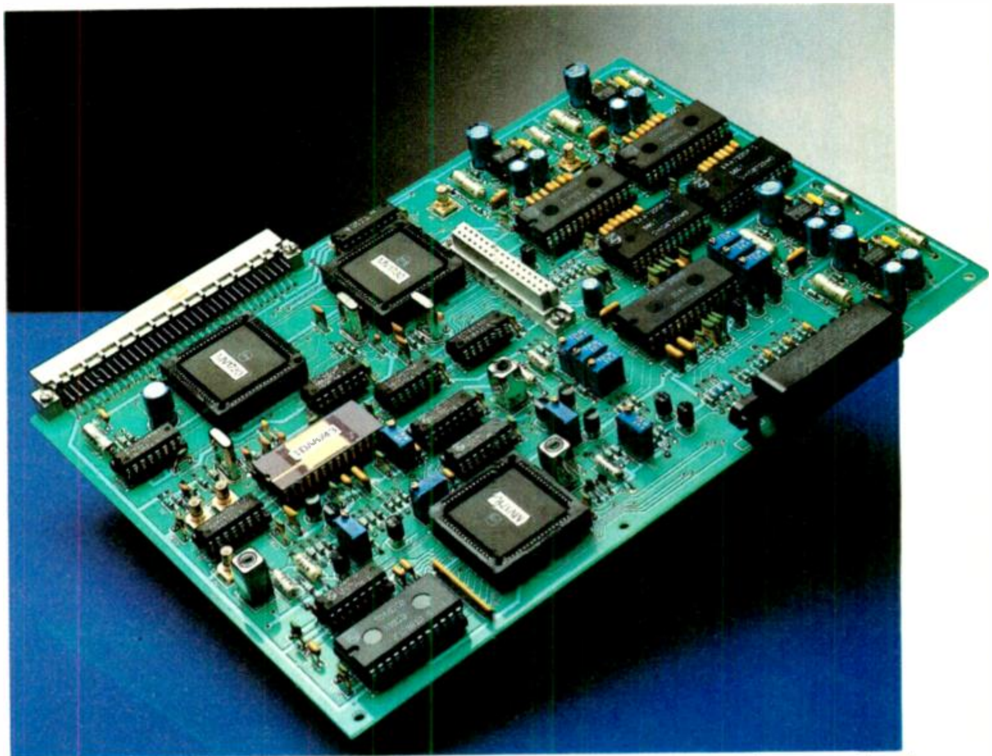
DATA CONDITIONING

Next in the decoder comes the MAC Control IC, MV1720. This device performs the majority of the data-conditioning functions within the hardware of the decoder. Data arriving from MACAN is not yet in intelligible form, and several processes are necessary before it is possible to make use of the packet data. Firstly the data has been spectrum-scrambled by modifying it with a pseudo-random bit stream before transmission, and this process must be undone.

In the case of a D-MAC transmission, the packet data will have been structured into two subframes by the broadcaster; in practical terms this results in each tv line carrying data from two different packets. These subframes must be "de-interleaved" so that the individual packets may be reconstituted as separate entities. This being done, the next task is to remove the error-protection data from the packet header, which constitutes the first 23 bits of each 751 bit data packet.

In the header is vital information on the identity of the data within the packet. This is used by the decoder to determine which IC needs to use it, and thus needs a high measure of security. A system called Golay protection has been adopted which adds 11 protection bits to a 10-bit packet address and two bits for a 'continuity index'. This technique permits up to three errors to be corrected. This decoder design is also capable of handling certain packets where Golay protection is used on the whole of the packet.

Before the now clean and tidy data is routed out of the device, a few packets which are of special significance are copied into buffers which have been programmed to watch out for their particular addresses. The arrival of these packets is signalled to the system control microprocessor, and the data is copied into the controller for further use. These special packets contain either housekeeping data needed to ensure the correct operation of the decoder (they tell the decoder about the nature of the services being broadcast at that instant and in the immediate future), or may contain information involved in conditional access operations. Another essential source of knowledge for the decoder is tv line 625, which is totally devoted to data in a specific non-packet format. Amongst the data carried in this form is the TV frame number. This too is automatically collected for use by the decoder.



This is a complete multistandard MAC decoder evaluation board providing an optional second channel of stereo sound. The board accepts the output from the receiver FM demodulator.

ENCRYPTION

Access to encrypted services is arranged by providing the appropriate vision, sound or teletext IC with periodic updates of digital data. This data is used to seed pseudo-random number generators having exceedingly long cycles whose outputs are used in various ways to 'unscramble' the wanted service provided the user is authorised. The necessary seed words are provided by a conditional access control module (or modules if more than one encryption system is used). These conditional access control modules sit outside the Philips/Plessey/Nordic decoder, and appropriate data is passed out and accepted back as necessary.

SOUND AND DATA

A two-wire serial bus known as the configuration chain is the way that the MAC Video, MAC Sound and teletext devices are advised by the control system of what service(s) they may look out for the packets with a particular address. The device sees the whole packet stream going by and ignores all those packets which it has not been told about.

The MV1730 sound IC is capable of interpreting the nature of the sound data for which it has been programmed. It examines certain special packets carrying its programmed address which are called EI packets. This means that the sound is autoamtically configured for any of the possible alternative transmission modes (e.g. 15KHz or 7KHz bandwidth, linearly coded or Nicam coded, first or second level error protection). The output from this IC is in the form of 12 S digital data which is fed into an oversamp ing digital filter and finally through the TDA1543 stereod d-to-a converter. The 12 S feed can of course be routed away to other d-to-a options if required.

Two alternative devices are planned for teletext; these will both give access either via vertical blanking interval broadcasts (much as in existing terrestrial services), or via the preferred packet teletext method. The VBI is intended to be kept clear for future use as a carrier of enhancement data to improve the MAC picture even further to high definition tv.

More than one teletext service may be included in a MAC transmission (data space permitting); each service would be assigned a different packet address, thus allowing the teletext IC to distinguish between them. Two levels of protection for teletext data are specified; one in which the equivalent of one terrestrial text line or packet is sent per MAC packet, the second having two terrestrial equivalents per MAC packet.

It is expected that while MAC services find their feet, text services will be limited to World System Test Level 1. Further expansion is possible in the future, both to teletext services and non-teletext data services, for which MAC with its wide flexibility in packet allocation is admirably suited. ■

Mike Brett is with Philips Components.

FEEDBACK

Mosfet audio output

Ivor Brown's thought-provoking piece on mosfet power amplifiers in the February 1989 issue jarred slightly. It may be "generally accepted" in the introverted world of the hi-fi magazines that a lot of feedback is inherently bad, but nowhere else. The only "undesirable effect" that comes to mind is poor slew-rate capability stemming from heavy dominant-pole compensation, made necessary by over-generous provision of open-loop gain. However, since no one ever seems to be able to point the finger at any commercial design that suffers from slew-limiting in use, it would seem that this is rather a non-problem, though no doubt constant repetition will keep the concept alive.

To be more positive, I agree with him completely on the many drawbacks of power mosfets – initial exposure to mosfet power-amp design tends to make you thoroughly grateful that bipolar power devices exist. The worst snags with the conventional type of output stage, as shown at Fig. 1, are certainly the poor g_m, giving a gain of significantly less than 1 (about 0.8 in Fig. 1) and the high gate capacitances. The usual mosfet complementary pairs – and these are few and far between – yield poor output swing capability for a given rail voltage.

Figure 1, with ± 32V rails, yields 40W RMS into 8Ω, as against the 64W theoretically possible. The high quiescent current required (around 100mA here, but as high as 500mA in some designs) makes the overall efficiency worse. Bipolar output stages typically require much less, say 20mA, and their setting is a more precise business, as the point between where crossover spikes disappear into the THD residual, and g_m doubling starts, is better defined (though whether you can keep it there is a matter between you and your thermal compensation arrangements).

I can also confirm that mosfet quiescent current stability is definitely an issue. Figure 1 is a conventional output stage, driven by emitter-follower Tr_2. With generous heat-sinks but no thermal compensation, this increased its quiescent current from 70mA to 90mA after 15 minutes at full drive. Part of the problem here is that optimistic engineers (surely a contradiction in terms) have been beguiled into using a simple variable resistance to set the bias voltage. This is unwise, if only because current source Tr_1 runs warm and drifts in value.

Another problem which is even worse than it looks is the driving of the mosfet input capacitances; these are not only large but also vary wildly with V_{ds}, often over a 2:1 range. Although point A in Fig. 1 is at a low impedance (a condition unlikely to exist in a real closed-loop amplifier) the distortion measured there rises rapidly above 5kHz, though not enough to affect the output THD, which remains absolutely flat 20Hz-20kHz at 0.7 percent for 12VRMS out.

At this point people may be wondering why anybody would wish to use these truculent devices at all. There is, despite the above, a powerful attraction in the great electrical and thermal robustness, and the absence of the high-frequency switching artefacts that plague power bipolars.

Like Ivor Brown, I considered that wrapping negative feedback around the output devices looked promising, and in 1979 I evolved the hybrid circuit in Fig. 2, in an attempt to combine the good qualities of bipolars and mosfets. Stage gain increases to 0.94, half of this loss being due to the 0.22Ω source resistors, and quiescent stability is excellent since Tr_3 and Tr_4 remain almost cold; note that V_{be}-multiplier Tr_7 is not thermally coupled to anything. Also, the optimal quiescent current is reduced to about 45mA. Open-loop THD falls to 0.04 percent at 12VRMS, and remains flat with frequency as the bipolar drivers are fast TO-5

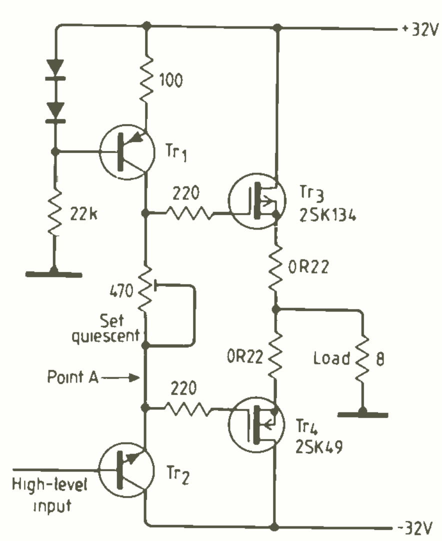


Fig.1

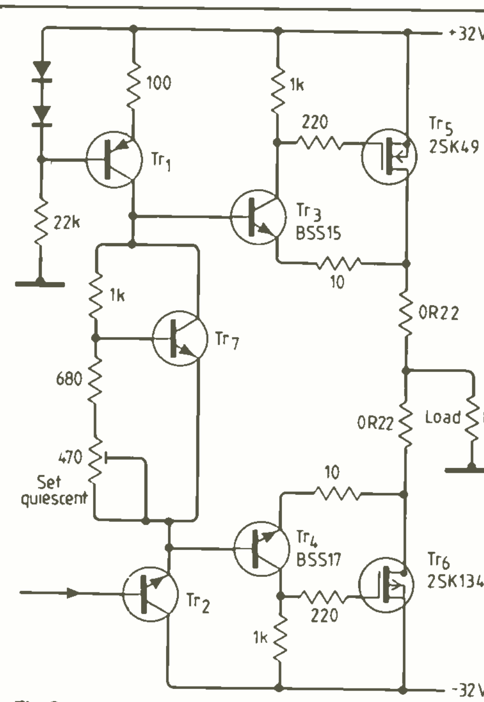


Fig.2

FEEDBACK

devices. This seems an excellent basis for a complete closed-loop amplifier, and the stage combines very happily with the usual differential-pair and common-emitter-gain-stage topology. THD drops to 0.004 percent at 12VRMS and 1kHz, though it rather disappointingly fails to disappear altogether. At present I am not sure whether this is because negative feedback has trouble coping with the transfer-of-control in Class AB, or if it is due to loading the vulnerable high-impedance collector of the voltage-gain transistor that replaces Tr_2.

One of the most intriguing points in Mr Brown's article was the possibility of improving output swing by operating the output stage at a gain of more than one, allowing elbow-room for large V_{gs} swings. The bipolar/mosfet configuration works well at a gain of 1.8, which should be ample for a large V_{gs} to be developed on the driver collectors, though THD worsens to 0.1 percent open-loop. Unfortunately no output increase at all was visible since, as with the devices shown, V_{gs} never exceeded 3V peak and all the output limitation appeared to be due the high on-resistance. It may be significant that R_{on} does not appear on the device data sheet. . . .

Douglas Self.
London E15

Bouncing gyro check

It is amazing what colourful ideas a little gravity in the region of a precessing gyro can engender. Dr Aspden's anti-gravity (January 1989) or Mr Jones' vanishing mass (January 1987) which fortunately failed to vaporise Professor Laithwaite and quite a bit of the local countryside, may be rather more prosaically described as acceleration.

The clue lies in Dr Aspden's diagram (b), combined with a little imagination. Turn it onto its side, and the forces F′ disappear. For the same rate of precession the forces F are much greater since there is no gravity to help them, for which reason fixed links are needed to transmit them, and so P is larger. Reverse the direction of precession and you reverse the direction of P. Demonstrations such as Professor Laithwaite's never show this second aspect for severely practical reasons! But if we do not oppose P, the assembly would accelerate away along the axis of precession, and this could be easily demonstrated by mounting the whole thing on a light trolley. Of course a suitable source of torque would have to accompany it, and in this case the torque would be transferred to the ground and reacted out by altering the load on the wheels on either side, giving us another problem to get confused about. We could eliminate this if we wished by mounting a second pair of gyros on the same shaft, rotating in the opposite sense to the first pair and balance out the torques against each other, thus producing an independent system which will "disobey" the Third Law of Motion. Something of this sort will produce a "lift force" if stood on its end, and even levitate.

From what has been said here and adding the appropriate conclusion from the absence of centrifugal force that Mr Jones refers to, we can see that the action of a precessing gyro can be quite simply described as generating two accelerations, one along the axis of precession and one at right-angles to and towards it.

The great problem seems to be how to "explain" all this in terms of Newtonian theory. I suggest that we are wrong to try. Newton himself would be the first to point out that he limited his theory strictly to Galilean inertial reference systems. These neither rotate nor accelerate. The reference system of the pressing gyro does both. What would give Newton a lot more sleepless nights, I think, was the 19th century discovery that mass varied with motion. The complete invariance of mass is axiomatic to Newton's theory. Whatever any of those "classical" theories that satisfactorily explained that variability are, the one thing they cannot be is Newtonian.

Alan Watson
Mallorca
Spain

Bradley, not Einstein

Long before Relativity was invented – even before it was generally accepted that light had a finite velocity – James Bradley (preceding Albert Einstein by 200 years) invented Stellar Aberration.

The fact that the idea came to him through sailing his dinghy (up-wind) on the River Thames is a measure of his tenacity as a scientific observer. The fact that he was able to confirm his idea by measuring the displacement of stars as the Earth moved round its orbit (and to deduce a new value for the velocity of light) is a measure of his stature as a scientist.

Yet how could he have since been so completely forgotten? In spite of the (now) commonplace observation of the displacement of the 'acoustical' position of a high-speed aircraft, few present-day 'experts' on relativity experiments appreciate the corollary that dawned on Bradley 250 years ago.

Were it not for the high velocity of light, coupled with the low acuity of the human eye and brain, the average new-born babe could not help but notice that, as it lunged towards its mother's breast, its destination appeared to jump momentarily away from it, causing the brighter infant to exclaim not "Mummy" nor "Einstein" but "Bradley"!

Robert V. Harvey
Grasmere

Computers are too slow

I must rise to the support of the wind tunnel as a solver of the fluid flow equations (The Kernel Logic Machine, *EWW*, March 1989). As pointed out elsewhere (Letters, *New Scientist*, 10 December 1988), calculating the flow even at a million points around a car provides extremely poor resolution; something like 64 billion would be needed to model the flow in correct detail. A real wind tunnel will model the flow at the equivalent of perhaps two billion points, and all in parallel, a considerable improvement on even the most optimistic forecasts of computer development.

Most wind-tunnel testing is not hampered by the lack of a moving-ground floor; aircraft performance, wind loads on structures, pollutant dispersion, for instance, do not require it. Those that do, such as high-performance cars, and especially racing cars, often use one of the five tunnels in the UK.

Longer-term weather forecasting is not amenable to modelling. Many meteorologists and mathematicians believe that supercomputers are approaching the limit of 'look-ahead', in the sense that after about seven days, further prediction becomes so sensitive to the starting conditions that the problem requires an impossibly high-resolution grid of measured atmosperic parameters to work on. In the classic phrase, 'the flap of a butterfly's wing' is enough to trigger a hurricane. Computers will continue to do well on average quantities such as predicting climatic changes due to man's alterations of his environment, but don't hope for

FEEDBACK

too much in predicting whether it will rain in Brighton next August Bank Holiday!
John Willis
British Maritime Technology,
Teddington.

Circuit symbols

Symbols used in electronic circuits are intelligently chosen. For example, a switch is shown by drawing its essential parts. But less obvious examples also carry a meaning. Thus the first transistors were made by taking a good, thick base and infusing two small electrodes.

But what about the BSI imposition of the rectangle symbol for the resistor, to replace the traditional 'wiggly line'? The rectangle has achieved recognition in the rather conformist educational world, but design engineers (and their journals) appear to have rejected it.

BSI should be a little more cautious. Circuit symbols are a truly international language, whose domain greatly exceeds that of the English language itself. Further, this language of symbols is the basis for international exchange of information. BSI is not competent to decide on these symbols. Its authority is too local.
Michael McLoughlin
Haberdashers' Aske's School

Switch-off

Following recent articles in the press regarding the shortage of engineering graduates and the 'oily rag' image that engineers command, I feel I should write to bring to your attention a further reason why engineering isn't a more popular career for graduates.

I am currently in the penultimate year of a four-year sandwich electronic engineering degree and am about to embark on the second of two six-month periods in industry.

The major problem my colleagues on the course and myself have found is in finding a suitable industrial placement. Far from welcoming undergraduates with open arms, as you might expect of an industry so short of manpower, many companies have been far from helpful. Letters written to companies enquiring about a possible placement regularly meet with no reply or an abrupt letter saying that they do not operate undergraduate placements of any kind. Those more fortunate to receive an encouraging reply normally attend an interview only to find that the company has little idea of what work the undergraduate will be required to do.

A further problem which is common to almost all such placements are the wages offered. They can rarely be described as little more than appalling For example, one undergraduate last year was employed by a very large international company in Watford. This company paid him the equivalent of £125 a week before deductions. After paying £50 a week for accommodation, the food, transport and clothing coming out of the remainder, he could rarely afford to visit his home in Birmingham, let alone save any money.

Many of the jobs themselves have been equally poor, with undergraduates finding themselves doing odd jobs and being left to tie up loose ends of projects rather than being set a project of their own or being included as part of a team working on such a project.

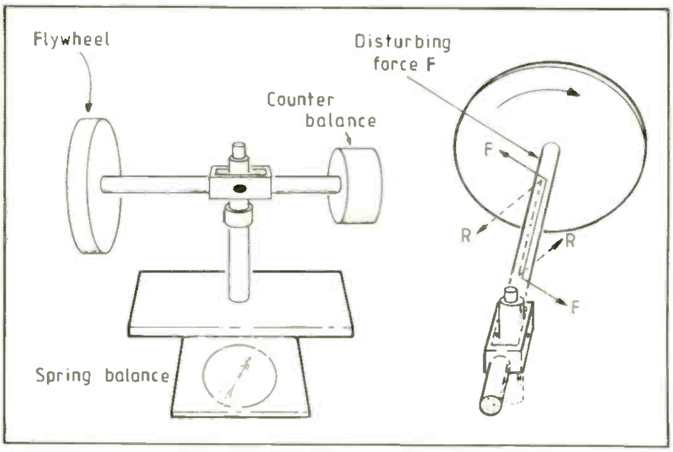
With employers showing so little interest in their future work force, is it really such a surprise that nearly 50% of engineering and science undergraduates opt for a different career on completion of their degrees? Until industry provides more encouragement to undergraduates and those about to select their degree courses, the future for British industry must surely look a little shaky.
Malcolm Holmes
Barton le Clay
Bedford.

Anti-gravity

By 1970, I had predicted and observed the vertical behaviour of the gyroscopic top described by Harold Aspden. During 1971, I built machines of two types, both well documented as having worked.

So there are two types of inertial drive and we are faced with a dilemma: which path to follow? My scant knowledge of the work of other workers indicates that the tendency of researchers is to follow, yet again, the wrong path; the one deemed acceptable by the establishment. That this is so is evidenced by the description of the machine in Aspden's article.

Class 1 machines are entirely non-Newtonian and the spin axes of the gyros maintain a constant attitude with respect to the main drive axis. There are no gyrocouple loads on the rotor bearings. If these machines are tested



in a Newtonian fashion, that is to say, by trying to measure a drive force F against the local frame, then they conform to Newton and appear not to work; also, gyro couple forces appear in the bearings. This behaviour is a direct consequence of the nature of precession.

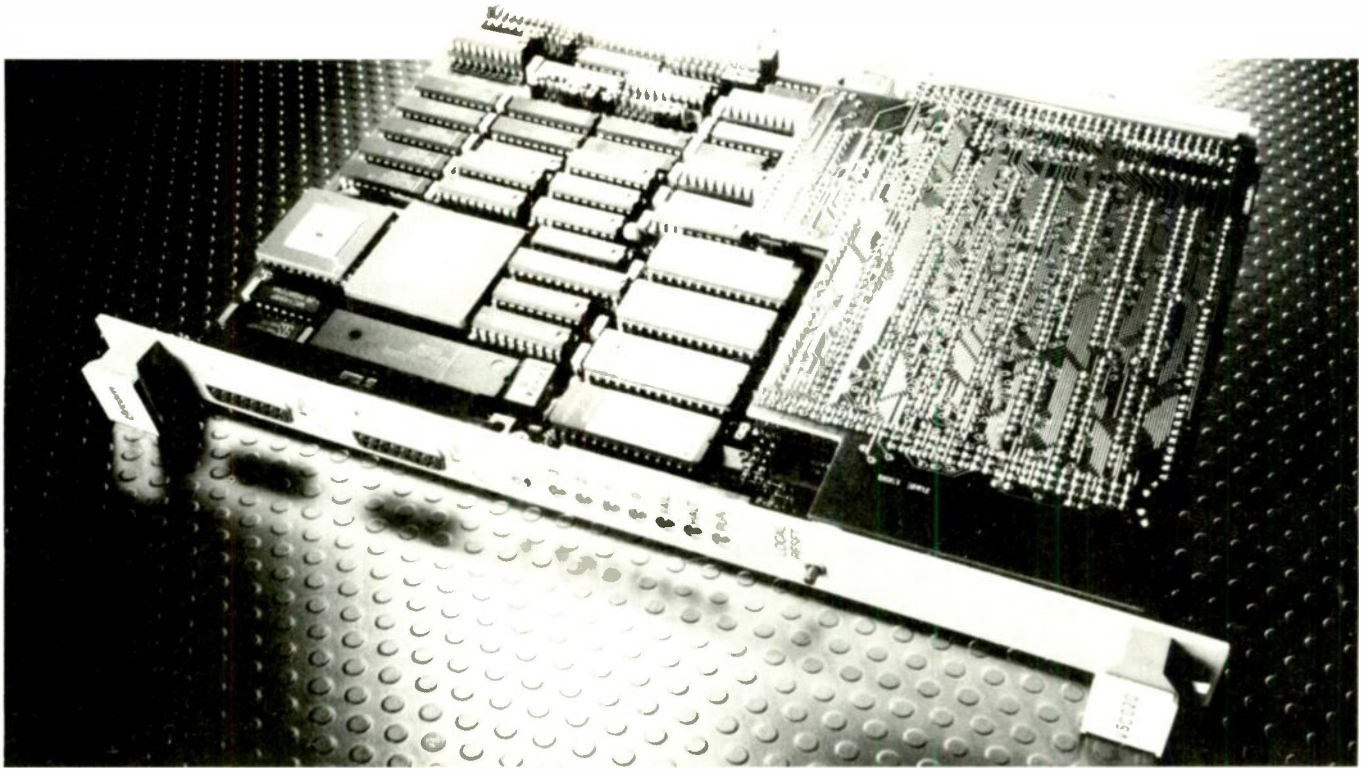
Class 2 machines are partly Newtonian with a constantly varying spin-drive axis relationship. The gyro-couple forces on the rotor bearings can be considerable, as is the vibration.

There are also machines which appear to be Class 1, but which are, in fact, Class 2: these devices would seem to involve nutation, together with a slight flexibility in construction.

A top may be set into precession without nutation and experiment confirms certain things: it *accelerates* into precession without an impressed force in the horizontal plane; it pursues an orbital path without horizontal centripetal restraint; and there is no angular momentum about the tower. These are clear violations of the three axioms of motion and present the "experts" with the problem of explaining how classical mechanics can claim to account for a phenomenon which violates its own axioms. If the contradiction appears, we may be sure that there has been faulty logic or false assumption inserted into the system at some stage.
Alex Jones
Alderney
Channel Islands

High-resolution frequency counter

The author points out some corrections to the January article: Pins 4 and 6 of gate F should be transposed; Capacitor C_1 is 15pF; Resistor R_5 is 100Ω not 100kΩ; and +5Va appears on the wrong side of L_1. And in Fig.4, for pin 17 of IC_6 and IC_7 read pin 7.



Dual buses for industrial I/O

Anthony Winter of Arcom Control Systems outlines some of the cost-saving options provided by the use of VME/STE mixed-bus architectures

It seems that the vast majority of complementary bus developments over the past few years have been aimed at increasing or optimizing overall system throughput. Typical examples are buses to provide fast local memory accessing or message passing between semi-independent intelligent subsystems. This is good news for the designer of, say, CAE workstations whose foremost concern is handling as many microinstructions per second as possible, but what about the more down-to-earth engineer developing a medium-complexity industrial control system? This type of project needs a reasonable amount of computing power and, perhaps because of this, the engineer initially opts for a bus like VME. But when it comes to implementing the I/O scheme, which might run into hundreds of channels, cost reduction becomes the major driving force. Unfortunately, this need is generally incompatible with the interfacing requirements of the VMEbus scheme and also, it has to be said, with the apparent high-profit business objectives of the majority of VMEbus board manufacturers.

This makes industrial I/O an area ripe for exploitation by multiple-bus architectures, which allow significant reductions in costs. It is now possible to achieve this result using a standard bus*. The bus in question is IEEE-1000 STEbus: a single-Eurocard scheme which is closely matched to the needs of the industrial control designer. Its 'limitation' of an 8-bit data path is, in fact, a benefit for industrial I/O applications, because it makes interfacing both simple and cheap and there is little or no performance penalty for the majority of tasks, because most I/O chips are designed for 8-bit buses. With more than 50 suppliers now in the STEbus market, there are hundreds of modules to choose from and, moreover, the members of the STEbus industry have co-operated to adopt a further informal 'signal-conditioning' standard which has resulted in a very wide range of complementary, single-Eurocard, real-world interface functions with screw terminals for easy connection to plant.

The concept of integrating the VME and STE buses was designed into STE from the start. It can be achieved by either adding an interface to a VME processor board and porting the processor's memory to both the VME and STE buses, or by building VME I/O boards with dual-bus interfaces and some latching circuitry to allow very low-cost (STEbus) processors to be used for adding intelligence to an I/O subsystem. Both these approaches are embodied in Arcom's VMEbus board line. The easiest way to understand the concept is to consider a CPU board which has dual-bus interfaces.

ONE BOARD, TWO BUSES

The VSC020 CPU board illustrated is a conventional double-height VMEbus 68020 processor module with an expansion connector to accept a single Eurocard containing the STEbus interface; the 68020's memory is linked to the VMEbus, STEbus and 68020. The interface to STEbus memory and I/O space appear as windows in the CPU's memory map. All the system designer needs to do to access the STEbus is write into this portion of the memory map – in the same manner as if defining the width of VMEbus memory access, for instance – and the command is transferred. The memory map opposite illustrates this.

With two bus interfaces available, the designer is free to partition the system for optimum cost-effectiveness, choosing VME modules for computation and memory, but selecting STEbus modules for the industrial

*See, for example, 'STE bus as an i/o bus in VME systems' by Tim Ellsmore, *Electronics & Wireless World*, February 1987, pages 143-6.

The VSC020 board with dual VME and STEbus interfaces. The STEbus interface is a daughter board, connected to the outer rows of the P2 connector. The board contains a 68020, a socket for a 68881 floating-point unit, 1Mbyte of ram, four 32-pin eprom sockets and two serial I/O channels. It costs £1250 in its 12MHz form

I/O. This approach to system design changes the economics drastically. For example, a typical VMEbus I/O board, say a digital I/O function, costs around £500. Implementing the equivalent function via STEbus – which requires a simpler bus interface – works out at around £250. The larger the system, the greater the savings. VSC020 also provides a powerful upgrade path for STEbus users: some simple software changes allow an existing STEbus system's processing power to be multiplied around tenfold (this figure is taken from benchmarks of an 8MHz 68008 STEbus CPU against the 16MHz version of this 68020 board), whilst retaining all the basic programs and OS-9 operating system environment.

This facility to migrate the design either up or down in processing power is an additional and powerful capability. When a design cycle starts, unless you possess some similar detailed experience or have undertaken extensive feasibility studies, it is usually not clear how much processing power you need. The result can be a 32-bit VMEbus system performing a control task that is well within reach of a Z80 running on STEbus (at say one-quarter of the cost), or an STEbus system designer resorting to techniques such as rewriting sections of code in assembler or adding another CPU, offloading a computing task to get the system functional. An STEbus system configured in this manner has nothing left in reserve to cope with any future system expansions. The VMEbus designer has to pay a very high price for the system, whilst the STEbus designer's costs and development time have mounted out of proportion – and with the possibility of a redesign.

The dual VME/STEbus concept changes this situation. Provided that you choose a 68K-family processor running under the OS-9 operating system, you can start with an STEbus CPU and upgrade the computer power at a later date, or start on VME with STEbus I/O and downgrade to, say, a 68008 for the target-system versions. This flexibility also extends to the field, and consequently offers a considerable benefit to people who have started to outgrow their original STEbus systems as the I/O workload increases. This is a particular issue with STEbus systems running OS-9, the industry-standard operating system for real-time multi-tasking systems based on Motorola processors. OS-9 has a complicated and rigidly-defined I/O structure and imposes a considerable computing penalty on I/O operations. If the processor is only 8- or 8/16-bits wide, as is almost invariably the case with STEbus, then an expansion of I/O

STEBUS BASICS

STEbus is now approved as a full world standard by the American IEEE. The 1987 standard, IEEE 1000, brings major benefits to the systems-building community, offering designers a powerful, fast and above all cost-effective means of implementing systems for applications such as control and instrumentation systems.

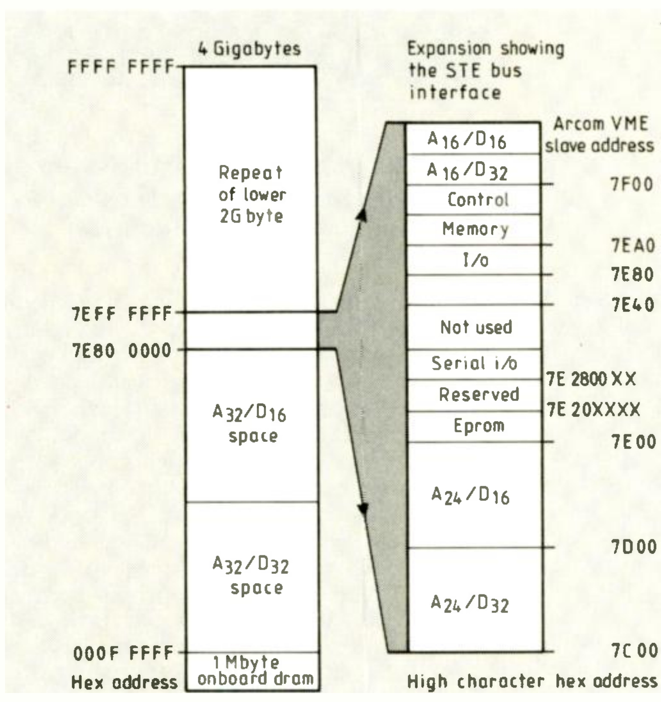
The bus was designed by a group of engineers independently of commercial interest, and now has a major following, with dozens of suppliers and hundreds of users. STEbus' main features are

- an 8-bit bus embracing the Eurocard standard and designed for low cost
- independence of processor manufacturers, giving the widest choice of processor on any 8-bit bus
- provision for future requirements through asynchronous, non-multiplexed data transfers at over 5Mbyte/s
- a full 1Mbyte addressing range
- up to 4Kbyte I/O space
- a position-independent, non-daisy-chained bus
- multiprocessor capability
- high-speed burst transfer mode
- eight attention-request lines
- vectored or non-vectored interrupts
- interrupt-acknowledge cycle
- read-modify-write cycle
- fully buffered signals and terminated backplane for data integrity

For many designers, one of the key design choices influencing bus selection is processor type. STEbus gives virtually unlimited freedom in this respect. Arcom alone offers no less than 12 choices of CPU embracing nine different processor families: Z80A, 64180, Z280, 80188, 8052, 6809, 68008, 8088 and 68020.

Information on STEbus is available freely via an independent manufacturers' and users' group – STEMUG. This organisation provides a number of helpful services including a document which describes the bus in considerable detail for prospective users. Free copies may be obtained from Arcom on request (Units 8-10, Clifton Road, Cambridge CB1 4WH).

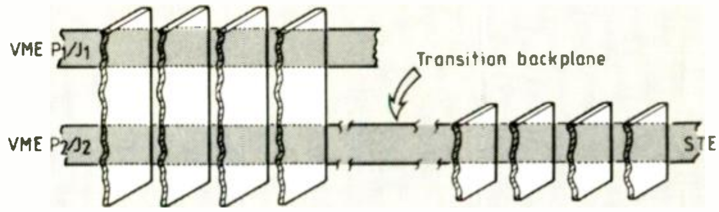
In the UK, the bus has over the last 3-4 years, literally changed the face of the UK's board-level computer market, sweeping aside STD and dozens of proprietary single-Eurocard bus standards to become the dominant 8-bit board-level standard. Its main application area is in small-to-medium size data acquisition and control systems, and its standardisation as IEEE-1000 has resulted in widespread user acceptance and a fast-growing following of manufacturers. The result is a UK STEbus market currently running at some £7M pa and growing at around 50% pa.



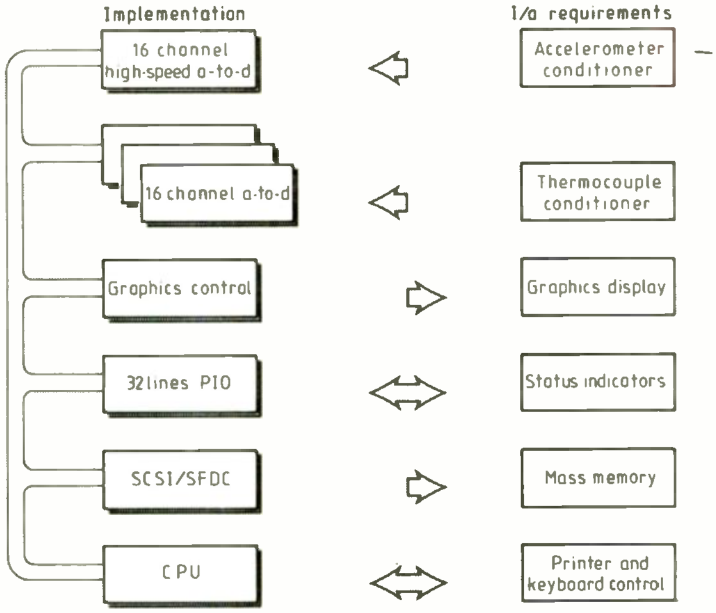
VSC020 memory map, showing how the module's memory is ported to VMEbus, STEbus and the 68020 microprocessor.

Example application demonstrates costs savings by using STEbus boards

Board function	Typical VMEbus implementation costs (£)	Typical VMEbus/STEbus implementation costs (£)
A-to-D conversion (×3)	1000 [2×1/2-height]	567 (3 boards)
High-speed A-to-D	535 [1/2-height]	372
Graphics controller	525 [1/2-height]	485
Parallel I/O	295 [1/2-height]	125
SCSI/FDDC	595	341 (2 boards)
Backplane (J1/STE)	165	98
Total	£3095	£1988



Physical connection of dual-bus systems. A full 32-bit double-height VMEbus system needs a simple transition backplane to connect STEbus to the two outer rows of P2. A 16-bit system can use an STEbus backplane directly as VME J2



An example application, illustrating the system's input/cutput requirements

can outgrow the system's processing capabilities. The dual-bus concept allows an upgrade to be implemented while retaining all the installed I/O and wiring. The final computer, as well as costing less can look identical to a pure VMEbus system, since both buses are based on Eurocards and can easily be integrated in standard 19-inch racks.

Physically, the STEbus interface appears on the two outer rows of the lower P2/J2 connector – the two rows unused in standard VMEbus pin assignment. This allows STEbus I/O boards – with CPUs if required – to be connected very easily: a small transition backplane takes the signals from VME to STEbus, allowing the use of two backplane systems in one cabinet. If only one 32-bit VMEbus CPU is required in the system, as it might be if the system designer started out on STEbus and is now purely upgrading the CPU power, then the position is even easier: you simply use a standard STEbus backplane on the bottom and a standard, half-height 16-bit VMEbus backplane on the top row if the VMEbus needs expanding. It is worth pointing out that not all single-Eurocard buses can work with VMEbus in this way. The G64 scheme, for example, is implemented on the a/b rows of the DIN connector, and therefore cannot work with a full 32-bit specification VMEbus system.

Adopting this approach to industrial control design does not restrict the use of either bus in any way. The VME 'side' of the VSC020 has an arbiter and mailbox circuitry, allowing it to function with other VMEbus CPUs, so that the full multiple-processor capability of VME can be exploited. Similarly, the STEbus side can also incorporate intelligence and this bus allows you to run systems with up to three processors communicating over the bus (see the box for background on STEbus).

EXAMPLE SYSTEM

The most obvious way to understand the benefits of this approach to systems design is to look at an example application. The hypothetical system shown in the diagram performs high-speed data acquisition, monitoring real-time vibration and temperature data from an engine test-bed. Even in this relatively simple system, multiple sensor in-puts demand a reasonable amount of I/O.

Accelerometers acquire the vibration data, their outputs being taken to a high-speed A-to-D converter. Less than 16 channels are needed, but rapid conversion and analysis are needed to provide a real-time graphic display of the resultant data, with signal processing using fast fourier Transforms to analyse the harmonic levels of the signal. This requires a substantial amount of computing power, so a 68020 processor board, with the built-in option of adding a floating-point processor device, is chosen.

Forty thermocouples measure temperature, the signals being digitised via three 16-channel 12-bit A-to-D converter boards. Low-cost boards are suitable for this part of the system because high-speed conversion is unnecessary.

A colour monitor presents the temperature information, some led bargraphs show the vibration levels and lamps indicate the test bed status. The hardware requirement is a high-resolution graphics board, plus 32 lines of parallel digital I/O, SCSI and floppy-disk drive.

In this example, we have not ignored the use of low-cost 'half-height' VME boards, where they are relevant. However, in general, this approach suffers from two key problems. Firstly, although the half-height VMEbus interface circuitry is simpler than for a 32-bit system, it still imposes a significant relative cost and size penalty; in systems for process control, which require low cost per channel there is still an appreciable difference compared to STEbus.

Secondly, and more fundamentally, a totally half-height VME system only allows you to upgrade to 16-bit processors – a relatively small advance in processing power, particularly when you consider some of the combined 8/16-bit chips that are readily available on STEbus. The feeling is that most designers would like to make a large jump in processing power all the way to 32 bits. Half-height VMEbus seems to be coming to an end; it fulfilled a temporary market niche whilst VMEbus was on its early curve, lowering the cost of target systems for 16-bit users, and will now begin to fade away.

The example system – despite its relatively modest I/O needs, clearly demonstrates the costs savings that can be achieved by using lower-cost STEbus boards for I/O. In this case, as can be seen from the cost breakdown shown in the table, there is around £1000 saving in I/O cost on a £3000 system. The CPU boards were not included in the figures – Arcom's VSC020 complete with dual bus interfaces, 12.5MHz 68020 and 1Mbyte ram costs £1250.

OTHER ARCHITECTURES

The dual-bus concept in this article has been introduced by looking at it on a processor board, but the system is just as easily applied to a VMEbus I/O board. Taking a 'dumb' board called VSP80 – an 80-channel parallel I/O module – as an example, the STEbus interface again appears on the two outer rows of the P2 connector, and is linked to the VMEbus via two 16-bit wide data latches, which can cause interrupts when written to. This somewhat simpler kind of inter-bus allows VMEbus users to implement their I/O systems with the benefit of low-cost STEbus CPUs as intelligent controllers. The latches provide a mechanism for controlling the use of the board between the host VMEbus CPU and the slave STEbus I/O controller.

In a further article, Jeremy Bentham will outline the software considerations of dual bus systems.

Data storage by silicon file

Traditional data-storage media have their limitations. The silicon "disk" provides a solution to most of them.

ANDREW MURPHY

Possibly the most versatile – certainly the most ubiquitous – storage medium is the floppy disc. Faster than audio compact cassettes, the floppy disc provides the added advantage of random data retrieval. During operation, the read/write head is brought into intimate contact with the surface of the disc. To minimize wear on both the head and the disc, the drive motor is switched off between accesses, causing delays while the drive achieves the correct operating speed for the next access.

In the hard-disc drive, the disc rotates continuously, reducing delays to the time necessary for the head to be indexed to the appropriate track or cylinder. Delays are further reduced by the use of multiple head designs; the head 'flies' just a few microns above the surface of the disc, minimizing disc and head wear. A hard-disc drive can store tens or hundreds of megabytes, which can be changed at will or retained indefinitely. In large systems, multiple-disc drives can provide almost limitless storage capacity.

Both floppy-disc and hard-disc drives are susceptible to vibration and shock, and a 'head crash' in which the read/write head is brought into contact with the surface of a hard disc can render megabytes of data unreadable. Current technology makes such occurrences extremely rare.

Optical discs, similar to the now-familiar 'compact disc', are scanned by a laser beam which also eliminates any mechanical contact with the disc. These provide even higher storage densities than the hard-disc drive but, once the data has been written to the disc, it cannot be changed. This 'write once, read many' (WORM) technique is particularly suitable for archival storage: a typical WORM disc can store in excess of two gigabytes of data on a single removable disc.

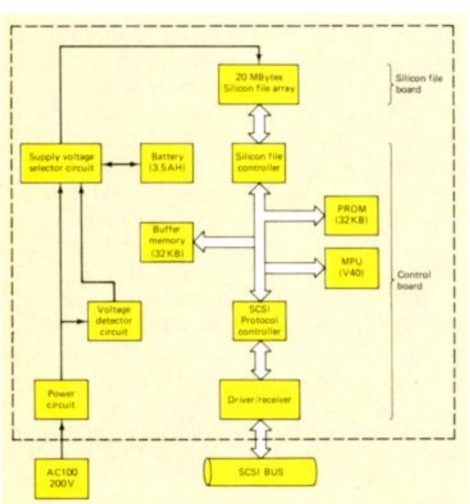
New optical-disc systems with multiple read/write capability are just becoming available. As yet, their operational reliability is unproven, but this technology seems promising. Access times and data-transfer rates indicate that improvements can be expected but, at present, speeds are currently well below those of hard-disc standards.

Mechanical equipment, however sophisticated, is prone to wear and head misalignment during normal everyday use and therefore requires regular servicing if it is to maintain peak performance and reliability. Power failures, 'brown-outs', micro-disconnection and over-voltage transients on the mains supply can wreak havoc during disc operation unless special precautions such as uninterruptible power supplies and mains filters are installed.

A new solution to most of these limitations is provided by the solid-state "disc" – a revolutionary concept with no moving parts and hundreds of times faster to access than conventional hard discs.

A solid-state unit, no larger than a 5¼-in disc drive, can provide a 40 Mbyte capacity with an access time of only 0.1 ms and a data-transfer rate of up to 20 Mbytes per second with a 32-bit data word.

Internal block diagram of silicon file disk, which provides an access time of 0.1ms.



SILICON DISCS

In addition to the faster access times, higher data-transfer rates and improved reliability, silicon discs must also offer reasonably high data capacity and the ability to retain data in the event of the power being interrupted.

Until recently, dynamic ram (dram) was the only high-capacity semiconductor memory available for use in auxiliary storage sytems. These devices, however, would require inordinately large batteries to maintain the high refresh currents necessary to retain data.

To overcome this problem NEC has developed the μPD42061 silicon-file chip, which combines high storage capacity and exceptionally low power consumption. The new device employs the latest trench capacitor, 1.0 μm c-mos technology and some advanced design techniques to achieve a 1 Mbit capacity with a standby current of only 30 μA over the temperature range 0°–50°C.

The μPD42061 differs from standard dram in the amount of power necessary to maintain data in power-down mode. This is achieved by holding the refresh input pin low and clocking the RAS input at a frequency determined by the ambient temperature.

COMPARISON OF HARD AND SILICON-DISC DRIVES

The most important factor in the performance of a disc drive is the access or 'seek' time. In conventional mechanical disc drives this is made up of two components: the time it takes to access the current track and the time to find the correct sector. This second component is dependent upon the rotational delay of the disc drive – the time it takes to rotate to the correct sector once the correct track has been found. For the fastest hard discs, these access and delay times are 15ms and 8ms respectively, where 8ms is an average time based on these drives taking 16ms for one full rotation. (Table1).

For a silicon file the seek time is greatly reduced and the rotational delay is completely eliminated, since there is no mechanical movement.

Table 1. Silicon "disk" operation compared with that of hard discs.

	access time	average rotational delay	total
ESDI H/disc drive	15ms	8ms	23ms
silicon disc drive	0.1ms	0	0.1ms

The solid-state disc concept has opened the way to more efficient long-term updatable storage. Short term usage can also achieve substantial benefits by exploiting the much faster access times available. High-volume 'virtual disc' use, in which hard-disc based data is dumped to solid-state disc for instant access and returned to hard disc at the end of the session, is no longer limited by available memory size. ■

Gauss (left) and Weber. Picture by courtesy of the Institution of Electrical Engineers.

PIONEERS

29. Gauss and Weber: an unlikely partnership.

W. A. ATHERTON

Gauss has been described as "a queer sort of fellow", ambitious and "glacially cold". Weber is said to have been friendly, modest and unsophisticated. One twice the age of the other, they seem to be an unlikely pair to have established a scientific partnership – one which, even today, a century-and-a-half later, is still recalled as epoch making: Carl Friedrich Gauss, the father figure, one of the great mathematical geniuses of all time; and Wilhelm Eduard Weber, a young and brilliant experimental physicist. Together they introduced absolute units to magnetic science, discovered Kirchoff's laws fifteen years before Kirchhoff, organized measurements of the Earth's magnetism which set a precedent for international scientific collaboration, and produced the first operational electromagnetic telegraph. Their exceptional scientific partnership of six years was broken only by politics.

GAUSS

C. F. Gauss has been hailed as one of the greatest scientific virtuosos of all time. At mathematics he was supreme and is compared with Archimedes and Newton. It was he who originated the statistical technique known as "least squares", which he then used to established his reputation as an astronomer by calculating the orbit of Ceres as if by magic.

Gauss was a giant amongst mathematicians and had been established in his university post at Göttingen since 1807. In 1828 he was persuaded to attend a scientific convention in Berlin. It was the only one he ever went to and he hated it. However, it was to be a turning point in his life for it was there that he was introduced to Weber. Gauss was already interested in geomagnetism and saw Weber as a suitable collaborator.

Though financial speculations were eventually to make him wealthy, Gauss was born into a poor family on April 30, 1777 at Brunswick in Germany. His father, whom he described as "domineering, uncouth, and unrefined", held various labouring jobs. His mother is said to have been intelligent but semi-literate.

It is claimed that Gauss learned to calculate before he could talk! Certainly he was a arithmetical prodigy who astonished his school-teacher. His father was persuaded to allow him to study instead of working to support the family, and at the age of 15 he became financially independent thanks to a stipend from the Duke Ferdinand. He entered the Brunswick Collegium. In 1795 he entered the University of Göttingen, having already made some independent mathematical discoveries previously made by others. Three years later he was back in Brunswick, living alone, and working intensely on mathematical ideas which came thick and fast.

Cold and uncommunicative, hating controversy, he was ambitious yet deeply conservative and staunchly nationalistic. When the duke raised his grant in 1801 Gauss remarked, "But I have not earned it. I haven't yet done anything for the nation." Perhaps in order to do something for the nation he set his mind to astronomy and became the director of the Göttingen observatory in 1807.

Ten years later he turned to geodesy and in 1820 began a triangulation survey of the state of Hanover which he completed 27 years later. For the first few years he did most of the field work himself, tolerating poor transport and inadequate facilities. Early in the work he invented a new surveying instrument, the heliotrope, a device which coupled mirrors to reflect the Sun's rays with a telescope. At 15 miles, the image in the telescope was as bright as a first magnitude star[1]. There was now, he said, a method which could communicate with the Moon.

Gauss married twice and fathered six children. His first wife died in 1809 shortly after giving birth to their third child. Gauss "closed the angel eyes in which for five years I have found a heaven". The baby died soon afterwards. Gauss married again in less than a year, choosing his wife's best friend for his second wife. He quarrelled with his sons and his second wife later suffered from tuberculosis. She died on September 13, 1831. Two days later, Weber arrived in Göttingen to join him. Gauss was 54, Weber almost 27.

WEBER

Wilhelm Eduard Weber was born in Wittenberg on October 24, 1804, one of twelve children of the professor of theology at the local university. His childhood home was therefore quite different from that of Gauss. Of his three brothers and a sister who survived to adulthood, one brother became a minister and the other two became professors at Leipzig. For six years from 1837 Weber was also a professor at Leipzig. Three brothers being professors at the same university must be close to being unique.

Weber entered the University of Halle in 1822 and completed his doctoral thesis on the theory of reed organ pipes in 1826 under J. S. C. Schweigger. Schweigger was the inventor of the "multiplier", the coil used in magnetic needle current detectors and the forerunner of the ammeter. Up to that time Weber's work had concentrated on wave oscillations in water and air. Two years later he gave a talk at the Berlin convention about his work on oscillations in organ pipes, and met Gauss. In April 1831 he was offered the professorship of physics at Göttingen.

In the six years of the partnership at Göttingen, from September 1831 to November 1837, the two worked on absolute magnetic units (i.e units based on mass, length and time and not involving any specific instrument or standard) and were interested in terrestrial magnetism and in establishing international co-operation in geomagnetic measurements.

Weber's partnership with Gauss, however, was severed by politics. In 1837 a new king came to the throne of Hanover and at once revoked the previous liberal constitution. Weber was one of seven Göttingen professors who bravely signed a protest and, like the other six, was sacked on order of the king. Attempts to have him reinstated failed. He continued to work on the magnetic measurements and the international collaboration and visited London and Paris, but in 1843 he left Göttingen to join his brothers in Leipzig. When the political scene in Göttingen changed in 1848 Weber was able to return and resume his career but it was then 1848, Gauss was 71 years old, and their collaboration was never renewed.

In 1840 Weber defined the absolute electromagnetic unit of current and determined the amount of water dissociated by the flow of a unit of charge. For a time a commonly-used unit of electric current was named after him until displaced by an international congress held in Paris in 1881 which adopted the ampere. (The weber became the name of a unit of magnetic flux in 1935.) In 1852 he defined an absolute unit for electrical resistance. Three years later, with his close friend Rudolph Kohlrausch he established the ratio between the electrodynamic and electrostatic units of charge as part of their test of Weber's ten-year-old law of electrical force. The result, published two years later and the only one available, was used by Maxwell in support of his electromagnetic theory of light. If converted to a ratio of electromagnetic to electrostatic units their result gave the figure of 3.1074×10^8 metres per second, very close to the measured velocity of light.

THE GÖTTINGEN TELEGRAPH

By the early 1830s there had been many suggestions for electric telegraphy though no fully operational system had yet been built. In Russia, Baron P. L. Schilling had developed instruments from about 1825 and received government approval to build a line in 1836. The Cooke and Wheatstone partnership in Britain began in 1837; and not until 1844, after frustrating delays, did Morse open his first line. But it was in 1833 that Weber constructed an electric telegraph. It remained in use until 1838.

Originally Weber's line was for scientific use, but Gauss soon realised the military and

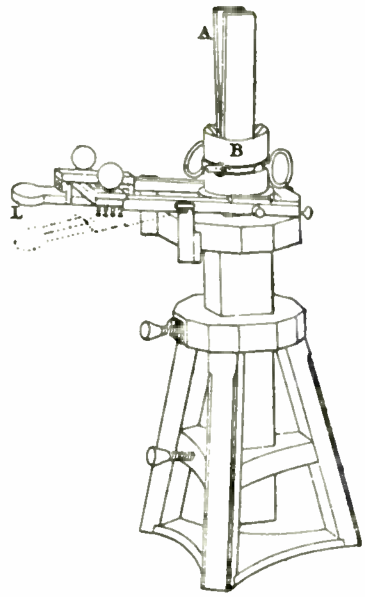


Fig.1. Gauss and Weber's telegraph transmitter[2] showing the two-bar magnet (A), the coil on a bobbin (B) and the lever for moving the bobbin up and down.

commercial value. Not having time to develop it commercially themselves they invited Steinheil of Munich to do so. In the long run the Gauss and Weber telegraph did not contribute significantly to the rise of electrical telegraphy in the nineteenth century. Its importance lies in its rightful claim to being the first to be operated on a regular basis.

Early in 1833 Weber strung two uninsulated copper wires on posts over houses and two towers from the university physics department to the astronomical observatory. The wires broke "uncountable" times. The next year they were extended to the geomagnetic observatory, a total distance of about two kilometres. The line was improved over the years but was eventually destroyed by lightning in 1845, by which time it was no longer in use.

At first the telegraph was operated from a battery but in the second or third year this was replaced by an "inductor" – an ingenious electromagnetic generator **(Fig. 1)** designed by Gauss[2]. This was simply a heavy (34kg) compound two-bar magnet around which was a 3500-turn insulated copper-wire coil on a bobbin. Later the number of turns was doubled. For signalling the bobbin could be moved up and down the magnet by a lever. This movement produced a short pulse of current in the coil, the direction of which depended on whether the bobbin was going up or down. The coil was connected to the line by a commutator which could reverse the connections to the line. By moving the bobbin up or down, and controlling the position of the commutator, positive or negative pulses could be sent at will.

The receiver was equally ingenious, though few instrument makers would want to copy the size and weight of its moving parts. On a large copper frame was wound a coil of 3000 feet of insulated copper wire. Inside this a heavy permanent magnet, 18 inches long, was suspended by silk threads so that it was free to move[2]. The small currents effected only a tiny movement of this hefty magnet. A small mirror was fixed to the supporting threads. A telescope with a scale placed above it was positioned a few feet away. Viewed in the telescope, the reflection of the scale in the mirror provided detection of the movement of the magnet.

Messages were coded as to whether the pulses caused the reflected scale to move to the right or to the left, and a coded alphabet was designed (Fig. 2). An alarm was added to summon the operator at the receiver when a message was about to be sent. A larger movement of the magnet set off the alarm either by striking a bell or by tripping a leaver which operated a clockwork alarm. Though their telegraph system was used for several years it was never adopted commercially. Steinheil had some success with a redesigned version which printed dots on to a moving roll of paper.

Both Gauss and Weber received appropriate honours, not least the naming after them of magnetic units. Gauss had always treated himself for any illnesses, with success; but in the end, with increasing heart disease, he came under a doctor's care. By autumn of 1854 he was very ill and became increasingly bedridden. He died in his sleep, in Göttingen, on February 23, 1855, aged 77, after 24 years as a widower.

Weber never married. He also died in Göttingen, peacefully in his garden on October 24, 1891, at the age of 86. Though perhaps an unlikely partnership, between the glacially cold and ambitious Gauss and the friendly and modest Weber, the fruits of that partnership live on today, 150 years later.

Fig.2. The Gauss and Weber telegraph code. Messages were coded as pulses which moved a reflected scale to the left or to the right.

r	=	a	rrrl	=	r
l	=	e	rrlr	=	s
rr	=	i	rlrr	=	t
rl	=	o	lrrr	=	w
lr	=	u	rrll	=	z
ll	=	b	rlrl	=	0
rrr	=	c, k	rllr	=	1
rrl	=	d	lrrl	=	2
rlr	=	f, v	lrlr	=	3
lrr	=	g	llrr	=	4
lll	=	h	lllr	=	5
llr	=	l	llrl	=	6
lrl	=	m	lrll	=	7
rll	=	n	rlll	=	8
rrrr	=	p	llll	=	9

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Next in this series of pioneers of electrical communication will be the British mathematician Alan Turing.

Tony Atherton is a principal lecturer at the IBA Harman Engineering Training College, Seaton, Devon.

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Twin-rail, dual-output, stabilised power supply

A 0V to 35V variable supply giving 50mA and 4A outputs

J.L. LINSLEY HOOD

ALTHOUGH this power supply design is intended specifically for use with the Class A/AB mosfet power amplifier circuit described in *Electronics and Wireless World*, March 1989, it could equally well be used as a general-purpose, variable-output bench power supply unit, covering the range 0–35V at up to 4A output.

In this case, those features such as the speaker-output direct-voltage-sensing trip circuit, included to protect the speakers in the event of an amplifier component failure, could be deleted. The design itself, with a few modifications, is based on an earlier circuit which I decribed in *Wireless World* in January 1975, and which has been in daily use in my own laboratory since 1974.

A particular feature of this 1975 design which I have retained in the current circuit is the ability to wind up the voltage on both positive and negative rails slowly and symmetrically. This is a most welcome facility when one is initially testing a newly built unit, since it allows one to check that all is well before applying full power. For this reason, I have retained a dual-gang potentiometer as R_{34}/R_{134}, whereas a couple of preset pots would otherwise have been used.

I have shown the basic circuit of this PSU in simplified form in **Fig.1**. For the sake of clarity, only one half of the design is illustrated. The other half is a mirror image of this.

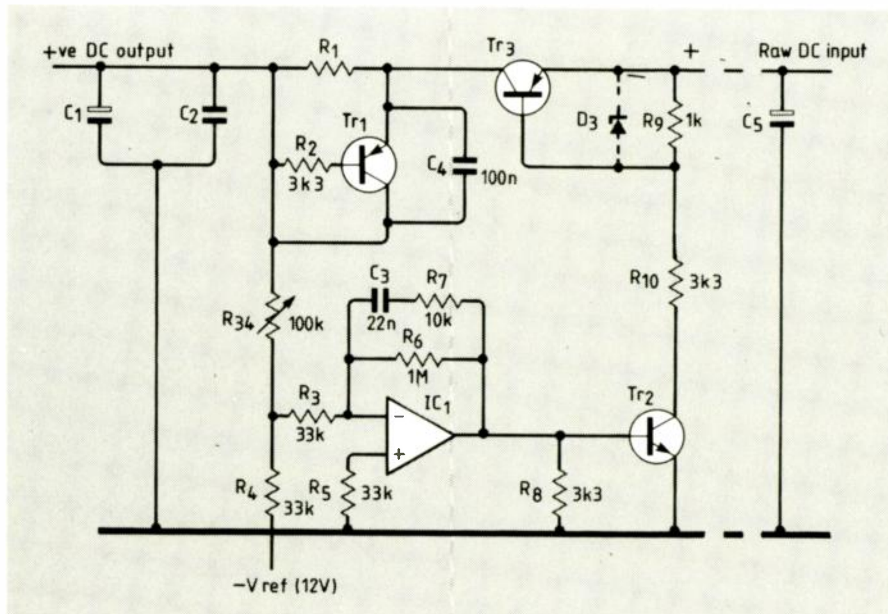


Fig. 1. Basic circuit of one stabiliser. Four circuits of this general type are used

METHOD OF OPERATION

This is a fairly conventional layout, with the 'pass' transistor, (Tr_3), used in the common-emitter mode, with the output taken from its collector circuit. This gives a higher output impedance than if it had been used in the rather more conventional common-collector mode, shown in **Fig.2**, when the output would be taken from the emitter circuit, but it offers several compensating advantages.

These are that the base current of Tr_3 is drawn from the 0V rail rather than from its own collector circuit as in Fig. 2, which allows the minimum voltage drop across Tr_3 to be a good bit less, which is helpful in minimising mains transformer cost. It also lessens the dissipation in Tr_2, since this is now only required to turn on as much current as Tr_3 demands, rather than having to pass more, in the quiescent state, than the maximum base current likely to be required by Tr_3 at full power output.

The method of operation of the circuit of Fig.1 is straightforward. The negative end of R_4 is taken to a reference voltage supply of some convenient value, such as −12V, and the positive end of R_{34} is taken to the power supply positive output rail. The operational amplifier IC_1 then acts to sense the potential at the junction of R_{34} and R_4, and adjust the voltage fed to the base of Tr_2 in such a way as to cause Tr_3 to increase or reduce its output current to bring the inverting input of IC_1 back towards the required 0V level.

In the circuit layout of Fig.1, over-current protection is given by Tr_1 since, if the voltage drop across R_1 exceeds the base-emitter turn-on voltage of Tr_1, this will conduct and effectively short-circuit R_{34}, causing the output voltage to collapse to a level at which the current demand falls to the level set by R_1.

Because of the very high gain of IC_1, the output impedance of the power supply system is very low at DC and very low audio frequencies. The output impedance rises at higher frequencies due to the action of the stabilising capacitor (C_3) across IC_1, but at these frequencies the impedance of the supply line decoupling capacitors C_1/C_2 is adequately low anyway.

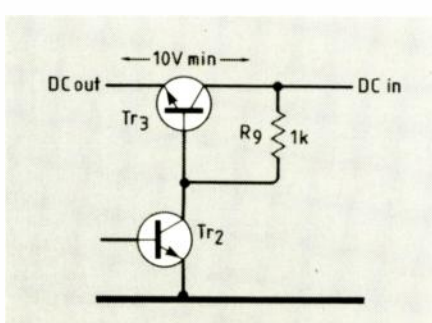


Fig. 2. Conventional "pass" transistor stabiliser connection, which gives less output current than the arrangement of Fig. 1

SPEAKER DC-OFFSET TRIP CIRCUIT

A major problem with 'direct coupled' audio amplifiers is that, in the event of a component failure, it is possible for the DC potential at the speaker output terminals to swing to the full value of the positive or negative supply lines, which can be destructive of expensive speaker units.

The conventional answers to this problem are either to include a suitable 'slow-blow' fuse in each of the speaker output channels, or to include a pair of relay contacts in the speaker circuit which will be opened by the relay mechanism if a DC offset is detected by the relay control circuitry.

The second of these alternatives is preferable, provided that the relay contacts are plated with some noble metal, or otherwise protected against tarnishing. Fuse holders are seldom of an adequate quality to ensure a reliably low contact resistance, and oxidised contacts may introduce asymmetrical resistance paths in the speaker leads which could have a much worse effect on THD than errors in component values or quiescent current settings.

A much better alternative is to monitor the speaker DC-offset potential electronically, and switch off both power supply lines if any excess offset voltage is detected. The circuit used for this purpose is shown in **Fig.3**, and is based on the simple two-transistor 'thyristor' layout of **Fig.4**.

In this, a pair of p-n-p/n-p-n small-signal transistors is interconnected so that the collector current of each feeds the base of the other. In the normal (quiescent) state, neither of these is conducting, but if some DC input signal is applied, say to the base of Tr_b, then both Tr_a and Tr_b will be forced into conduction, and the DC potential at point 'x' will fall from V_{cc} to around 0.7V.

If a pair of these 'thyristors' is set up, operating from positive and negative rails, as shown in Fig.3, then capacitatively cross coupling the outputs to inputs, by C_2 and C_3, will cause the collapse of the potential across either one to trip the other half of the circuit as well. Additional capacitors C_4 and C_5 are essential in this case to reduce the sensitivity of this trip action, or it would be nearly impossible to have both pairs of transistors non-conducting simultaneously.

The speaker DC-offset sensing is provided by the two input emitter followers Tr_1 and Tr_2, which allow a sensible value of input AC bypass capacitor (C_1) to be employed. Since the likely DC offset could be either positive or negative, a non-polar capacitor is indicated; the time constant of R_2C_1 must be large enough to bypass the audio signal present at the amplifier output terminals, and prevent spurious triggering of the trip circuitry by large, though legitimate, audio signals.

In practice, Tr_1 and Tr_2 are duplicated to allow simultaneous sensing of both speaker output channels, and, obviously, this replication of Tr_1/Tr_2 with D_1/D_2 could be extended, if perhaps the same PSU were to be used for a four-channel system.

The high-current power-supply shutdown action of the trip circuit is achieved by coupling the points 'A' and 'B', of Fig.3, to the reference voltage supply to the op-amp IC_1, so that if the 'thyristors' are tripped, the effective reference voltage is reduced from +/–12V to +/–1.2V, which lowers the power supply voltage output by a factor of 10. A supply line voltage of some +/–3.5 to 4V is too low to cause damage to either speaker units or other components.

COMPLETE PSU CIRCUIT

Because the maximum output current of 4A and the total supply voltage would, if they appeared simultaneously across the devices, exceed the safe operating area specification for the chosen output transistors, a re-entrant overload current characteristic is provide by modifying the circuit layout of Fig.1 in the manner shown in **Fig.5**. In this arrangement a larger value of current limit resistor (R_1) is employed and the emitter of

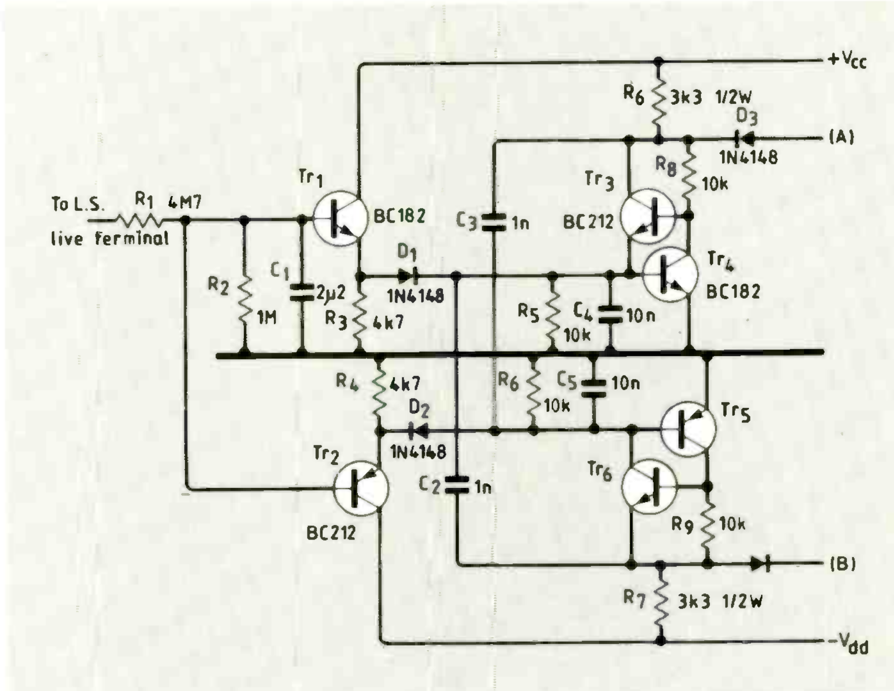


Fig. 3. Loudspeaker DC-offset protection circuit. An offset sensed at the speaker terminal collapses the voltages at A and B

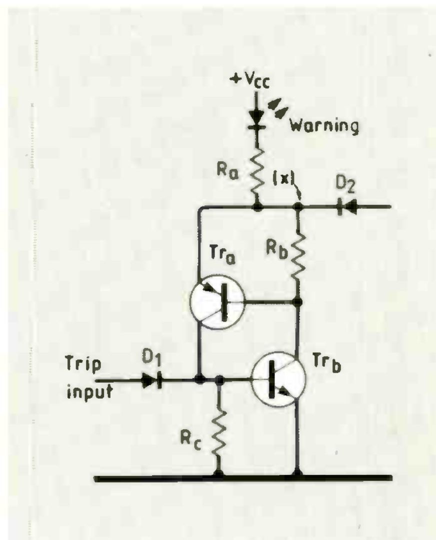
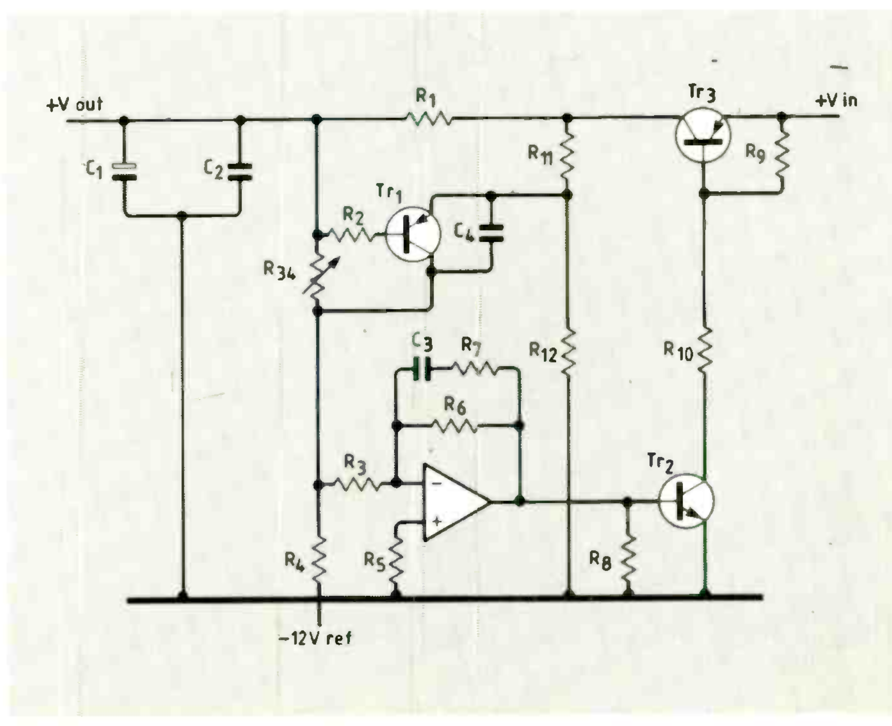


Fig. 4. P-n-p and n-p-n transistor pairs used in the circuit of Fig. 3 simulate thyristors to switch off the power supply lines

Tr_1 is taken to a less positive potential to compensate for this. This leads to the final PSU layout shown in **Fig.6**.

If the direct output voltage collapses, as would happen on an output short-circuit or low-impedance load, then the limit current setting is also reduced. With the component

Fig. 5. Modification of Fig. 1 circuit to provide re-entrant current overload protection



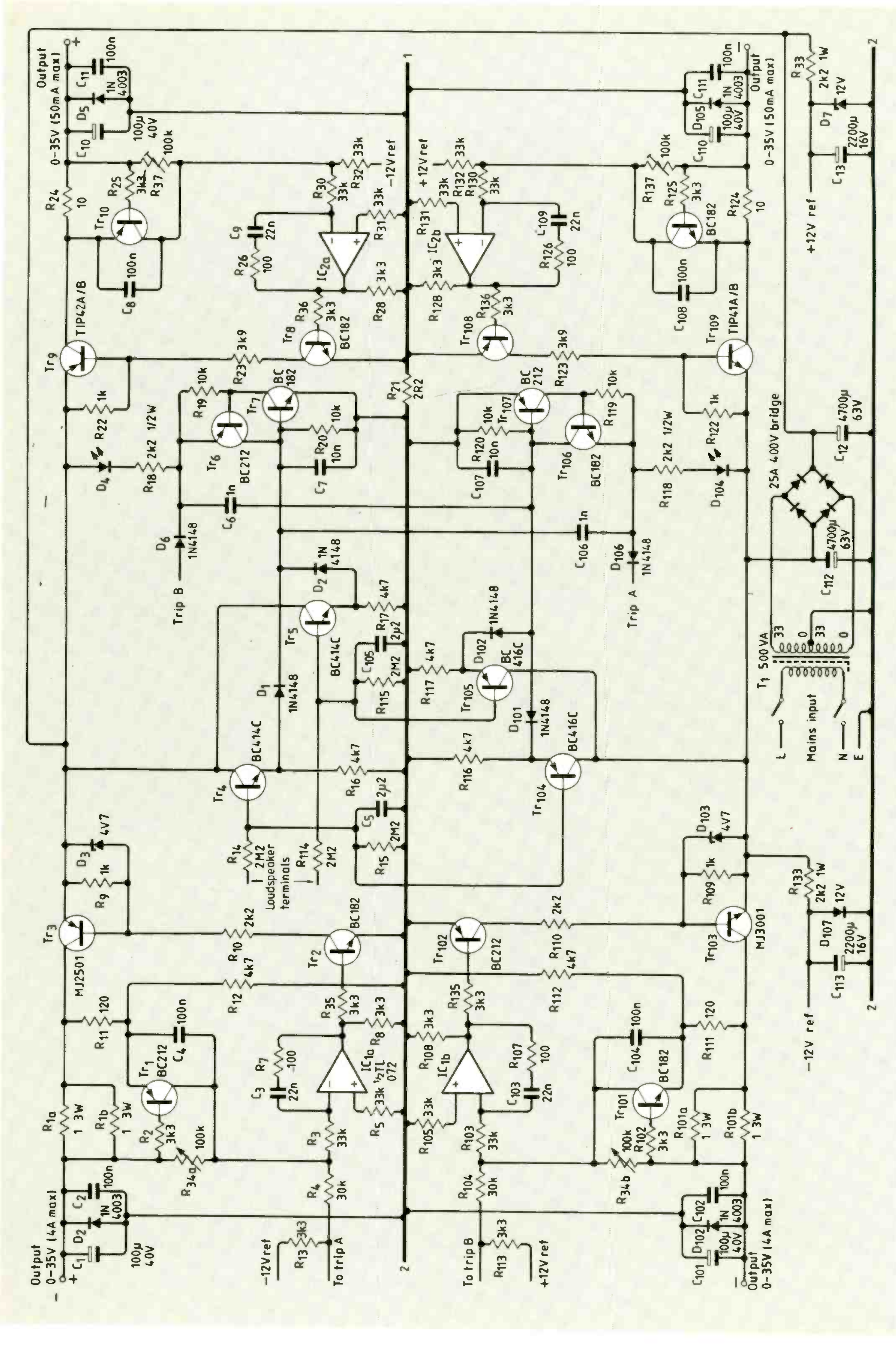

Output 0–35V (4A max)
Output 0–35V (50mA max)
Output 0–35V (50mA max)
Output 0–35V (4A max)
Tr9 TIP42A/B
Tr109 TIP41A/B
Tr3 MJ2501
Tr103 MJ3001
Tr1 BC212
Tr101 BC182
Tr2 BC182
Tr102 BC212
Tr4 BC414C
Tr5 BC414C
Tr6 BC212
Tr7 BC182
Tr8 BC182
Tr10 BC182
Tr104 BC416C
Tr105 BC416C
Tr106 BC182
Tr107 BC212
Tr108
Tr109
IC1a ½TL072
IC1b
IC2a
IC2b
Loudspeaker terminals
Trip A
Trip B
To trip A
To trip B
−12V ref
+12V ref
T1 500VA
Mains input
L
N
E
25A 400V bridge
C12 4700μ 63V
C112 4700μ 63V
C13 2200μ 16V
C113 2200μ 16V
R33 2k2 1W
R133 2k2 1W
D7 12V
D107 12V
R34a 100k
R34b 100k
R1a 1 3W
R1b 1 3W
R101a 1 3W
R101b 1 3W
R21 2R2
D1 1N4148
D2 1N4148
D6 1N4148
D101 1N4148
D102 1N4148
D106 1N4148
D3 4V7
D103 4V7

Fig. 6. Complete circuit of twin-rail power supply

values specified, this short-circuit current level is set at approximately 1.5A, which keeps the 'pass' transistor within its rating. However, the heat sinking for (Tr_3/Tr_{103}), must be adequate to allow for a static worst-case device dissipation of 63W, though the more normal dissipation under maximum amplifier output conditions would only be 32 watts.

The pass transistors (Tr_3/Tr_{103}), can be replaced with DMOS or TMOS devices such as the Hitachi 2SK and 2SJ series mosfets, which are much more resistant to secondary breakdown than bipolar devices, provided that R_9 is increased in value to 10kilohms, and bypassed by a 4V7 gate-protection zener diode. The resistor R_{10} is there simply as a safety precaution to limit the maximum current which could flow in this line under fault conditions.

TRIP WARNING AND RESET

With the circuit shown, the only way to reset the power supplies if they are tripped by an excessive DC offset at the speaker terminals (and it is probably prudent, after construction of the PSU, to test this action by deliberately applying a direct voltage to the speaker ends of R_1/R_{101} to make sure that it does trip) is by switching off the input AC mains supply to the power transformer.

It is possible to reset the trip circuit by the simultaneous connection of the bases of Tr_4/Tr_5 (of Fig. 3, or Tr_7/Tr_{107} of Fig. 6), to the 0V line, but if a genuine fault condition existed, damage could occur during the resetting operation. Also, if the action of the switch released one of these bases from the 0V line sooner than the other, it is possible that only one supply line would return to the required operating potential, which would again produce a fault condition.

I have only provided simple current limiting action on the 'low-current' part of this supply since, at the current levels required for the class-A driver stages of the audio amplifier, for which this part of the PSU is intended, no great harm is likely to follow a fault condition.

> **PERFORMANCE SPECIFICATION**
>
> **Output voltages**
> 0 – 38V for both main and low-current supplies.
>
> **Output currents**
> 50mA and 4A respectively.
>
> **Load regulation**
> Better than 2mV, zero to full load.
>
> **Output hum, noise and ripple**
> Approximately 150μV, not significantly affected by load.
>
> (These figures were obtained with a bipolar 'pass' transistor. Those for the circuit modified to use mosfets are similar.)

The low current part of the supply should be set to a slightly lower output voltage than the main (output) supply since, if the amplifier is driven into clipping, it is preferable that this should occur in the low-current class-A driver stages, where the clipping action is cleaner than in the output devices.

As I said at the beginning, although this PSU is intended for use with the mosfet amplifier described earlier, it could also be used to upgrade the performance of other audio amplifiers, in which a simple transformer/rectifier/reservoir-capacitor system is used, or in which the output stages and the earlier class-A stages are operated from common supply lines.

Because of the very low output impedance of the two systems, there will be no significant inter-channel breakthrough if the two low power class-A parts and the two output stages (L and R channels) are parallel connected to their respective supplies, so the extra cost of the components needed for a fully stabilised PSU system can be offset against the provision of two completely independent transformer/rectifier/reservoir-capacitor layouts of the kind now advocated by the purists.

COMPONENTS

While most of the components required should be readily available from normal stockists, Hart Electronic Kits Ltd, of Oswestry, often seem able to supply unusual or hard to come by items.

Countering mobile fading

A basic problem affecting VHF and UHF mobile communications – and FM broadcast reception on car radios – is fast and deep fading due to the constantly changing summation of multiple multipath signals brought about by local scattering. Since in an urban environment the mobile antenna will usually be lower than the surrounding structures, the direct signal from a base station will be bounced off nearby buildings and many reflected signals generated (**Fig. 1**). The sum of these signals will constantly change as the vehicle moves along the streets.

This can result in frequent signal drop-outs (during which speech and particularly data can be lost), distortion and noise bursts when the signal drops below the threshold level. As Steven E. Turner (Universal Data Systems) writes in Multipath interference in FM data transmission (*RF Design*, December 1988): "The effects of multipath interference can be crippling to FM data radio transmission, especially if the desire is to establish a network of mobile radios in a sprawling urban environment. . . Numerous solutions have been proposed. The most promising techniques that have appeared to date include diversity transmission and several forms of received signal equalization."

Steven Turner suggests that an answer for mobile FM-FSK systems may be found in adaptive channel equalization, preferably in the form of decision feedback adaptive equalization which gives good protection against the serious inter-symbol interference found in slow multipath interference.

Diversity reception can materially reduce the depth of fading. A technique that has been field-tested in Copenhagen is based on the use of a compact circular array of outward-sloping monopoles mounted on the vehicle roof which forms an "infinite" ground plane. Such a system is described by R.G. Vaughan (DSIR, New Zealand), J.B. Anderson (Institute of Electronic Systems, Denmark) and M.H. Langhorn (ESTEC, Holland) in *IEEE Trans. on Ant. & Prop.*, October 1988, pages 1365-1374. It is shown that an advantage of such an array over conventional space diversity is that the feedpoint spacing can be made almost arbitrarily small even for a large number of elements. The trials included the use of a three-element array with element lengths of 0.6 λ and feedpoint spacing 0.1λ used at 463 MHz (**Fig. 2**). Whereas received signal-to-noise ratio (dB) on the individual elements, compared to minimum value s:n (dB), was 39.88/15.18; 40.45/14.48; and 34.88/20.00, the combined maximal ratio signal power was 43.78/32.40.

There is the possibility of using arrays comprising many elements: "Some configurations which gave low correlations between adjacent elements are four-, six- and eight-element circular arrays with feedpoint spacing 0.05λ, element length 0.6λ and element elevation angle 30° to 40°; 12- and 24-element arrays require elements larger than 0.6λ or feedpoint spacing greater than 0.15λ to achieve low signal correlations between adjacent elements." The IEEE paper indicates that the trial results are in good agreement with the theoretical analysis.

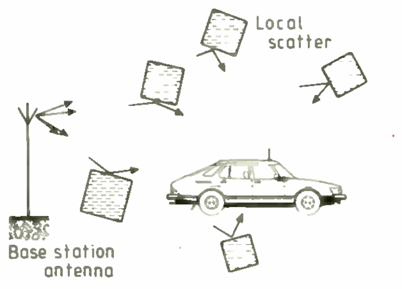


Fig. 1. Fast fading to below the FM threshold level in mobile VHF/UHF operation results from the constantly changing summation of many signals reflected from buildings, ground etc. The changing path loss due to hills and other major obstructions results in pronounced, but slower long-term fading. Ideally the receiver needs to cope with fast fading superimposed on a slower fading signal.

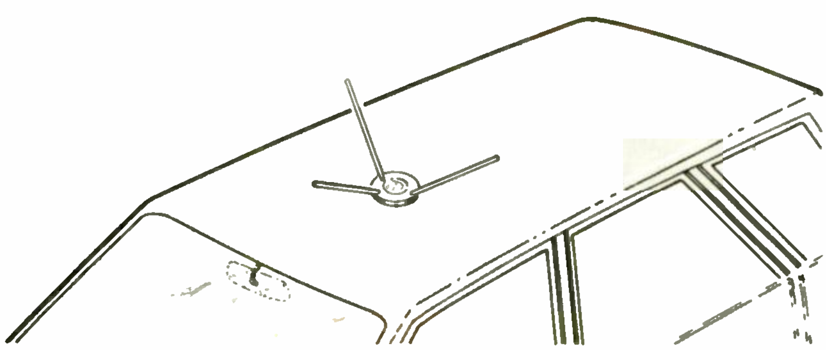


Fig. 2. Outward-sloping monopoles provide the advantages of space diversity even though the feedpoint spacing can be made almost arbitrarily small.

The combination of fast and slow fading inherent in mobile operation also has serious effects on SSB systems and has led to investigation of improved AGC. Dr Joseph McGechan has been prominent in the UK in advocating feed-forward signal regeneration (FFSR) in conjunction with an optimized form of SSB called phase-locked transparent tone in-band. In a paper published in 1985 (*IEEE Trans. on Vehicular Technology*, February 1985) these systems were compared to 25kHz FM and it was suggested that the improved speech quality and lower error rates for data "clearly demonstrate that pilot tone companded SSB should be considered as a suitable modulation form for mobile radio over all operational frequency bands up to 1GHz".

Mobile stereo with FMX

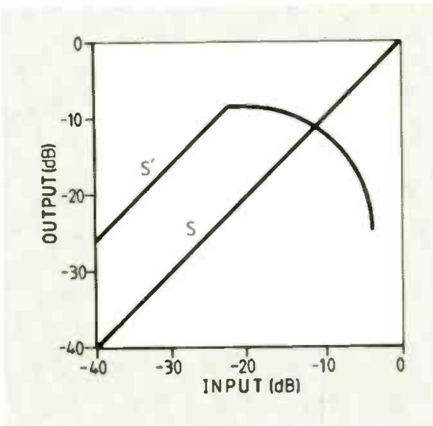
European broadcasters have devoted much time and resources to the introduction of the Radio Data System (RDS) even though its appeal is likely, for a considerable time, to be largely restricted to the top-end of the car radio market. Much less interest seems to have been shown in investigating the potentially much more significant FMX system, first announced in 1985 as a joint project by CBS Technology Center and the National Association of Broadcasters. FMX was described in detail by Emil Torrick (CBS) and Thomas Keller (NAB) in the *Journal of the Audio Engineering Society*, December 1985.

By then, early field tests had suggested that FMX could largely overcome the problem with conventional pilot-tone FM that noise-free reception of stereo requires a very much stronger signal than is needed for satisfactory monophonic reproduction. This means that any pilot-tone FM transmitter has a much larger coverage area in mono than in stereo.

It is usual to specify the limit of stereo as a signal strength of 60dB (relative to 1μV) whereas for mono this is 48dB. Even this is rather misleading since listeners are advised to use an outside antenna array for stereo and the real difference is roughly 20dB. Torrick and Keller claim that FMX can suppress stereo hiss by some 20dB and would result in a stereo service area roughly equal to that for mono, and thus represents the first major improvement to stereo radio reception since the standardization of the pilot-tone system in 1961.

CBS made attempts to interest European as well as American broadcasters and BBC Research offered to evaluate the system if

Fig. 3. Compression characteristic of the FMX system for extended stereo coverage. The compressed signal s′ is transmitted in quadrature with the normal stereo difference signal s on the 38kHz subcarrier.



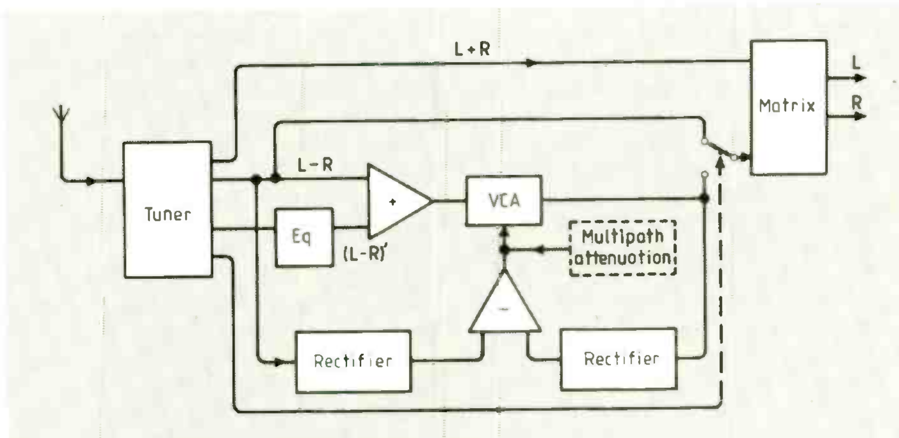


Fig. 4. Outline of FMX receiver/expander. Decoder ICs are already available.

provided with an FMX encoder, but there was something of an hiatus when CBS closed down the CBS Technology Center a few years ago.

Emil Torrick has continued work on FMX, which is now a registered trademark of Broadcast Technology Partners of Greenwich, Connecticut. There already exist FMX IC decoders (Sanyo LA3440 and Sprague ULN3800).

FMX reduces noise in stereo reception by compressing the stereo-difference signal before transmission in quadrature to the regular stereo-difference signal on the 38kHz suppressed carrier. Compression provides linear operation with 14dB gain over much of the dynamic range of the broadcast material; at high modulation levels the companded s′ signal is attenuated to avoid reducing the modulation power of the regular compatible broadcast service (**Fig. 3**). To receive FMX, the compressed s′ signal is expanded using the regular stereo-difference signal envelope as a control model (**Fig. 4**).

FMX was demonstrated at the 1988 NAB, at which time CBS announced that the system would be used on the CBS radio network. The BBC is still interested in evaluating the system but has so far not received the promised encoder and remains concerned at the possible effect of the extra companded signal on normal stereo reception under multipath conditions. There is also a belief that the system has been modified to some extent since it was originally announced in 1985.

A recent paper by Thomas E. Rucktenwald and Emil Torrick of Broadcast Technology Partners (in which CBS and NAB retain an interest), FMX mobile reception (*IEEE Trans. on Consumer Electronics*, November 1988, pages 921 to 928), discusses the performance of FMX under the fast fade multipath conditions encountered in moving vehicles. They point out that while normal FM broadcast reception provides good quality audio free from the degradations of static, sky-wave fading and overlapping coverage by other stations, it suffers degradation where there are multipath conditions. At fixed sites this can be alleviated by the use of directional antennas, a palliative not available in moving vehicles. VHF/FM stereo car radios often incorporate a "blend" function that reduces multipath noise bursts at the expense of reducing stereo separation.

In contrast, it is now claimed that, with FMX, receivers can reduce background and multipath noise without a loss of stereo separation. It is admitted that during multipath disturbances the regular stereo-difference signal cannot provide normal adaptive control of the FMX expander. It is necessary to arrange when multipath is detected to hold the last known correct control voltage and preferably to apply a small supplemental control factor derived from the multipath detector, proportional to the severity of the multipath (**Fig. 5**). This increases the attentuation of the s′ signal, resulting in further reduction of multipath noise.

The authors reveal that two new techniques for the detection of multipath have been investigated and successfully incorporated into experimental FMX car radios. The first detects low frequency (under 500Hz) amplitude modulation on the 19kHz pilot. The second compares the audio polarity of s with s′, since during multipath events the usual phase relationships are disrupted. Both techniques can be applied with a minimum of additional circuitry to the existing FMX IC decoders.

The paper does not discuss the question that worries European broadcasters; the degree, if any, to which the presence of the extra s′ quadruture signal would, in some circumstances, affect quality on existing stereo sets not incorporating an FMX decoder.

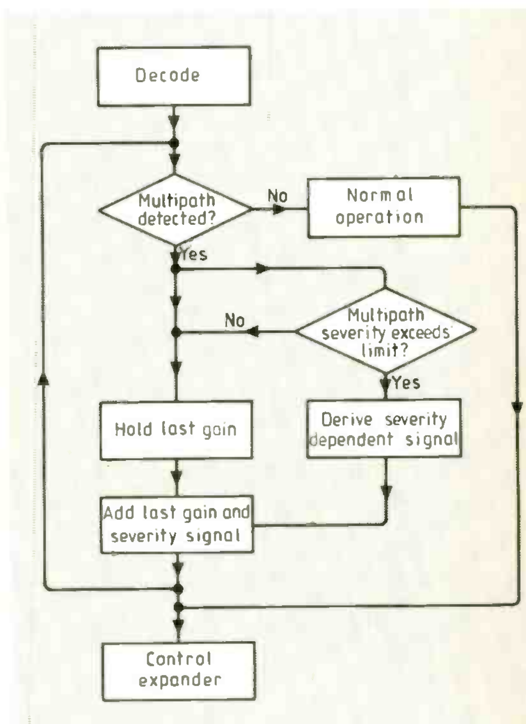


Fig. 5. Flow chart for FMX multipath noise attenuation for car radios.

Video standards challenged

The difficulties that continue to face the introduction and interconnection of new video techniques and waveforms – digital and component-video – have led to some dissatisfaction with the way in which broadcast technical standards and codes of practice are established. In Europe this is primarily done by national broadcasters or internationally through the slow-moving EBU committees with their drafts later submitted to the CCIR. For many years EBU committees have been drawn from engineers of the member organizations, although more recently there has been some participation by the broadcast equipment industry, making the process a little more like the North American SMPTE standardization procedures. But with independent production and facilities houses now aiming to play an increasingly important role in Europe, voices are being raised against the present system, which excludes them, advancing the view, apparently shared by the British Government, that technical standards and codes of practice are hamstringing the industry and that technical quality should be left primarily to the market place.

An outspoken critic of the present state of affairs is Andrew Vere of SVC Television. In a keynote address to a joint IEE/RTS colloquium ("Video standards and their interconnection – the studio standards challenge") he expressed the view that the broadcast engineers have got it all wrong: "Too much attention has been given in television to the technical side at the expense of the financial and creative side. . .for far too long, technical standards have been dictated by engineers – worst – by broadcasting engineers. For years programme makers have been frustrated by such people whose only function seems to be to tell producers and directors what they cannot do."

He sees the present era of change as "an opportunity to break with established standards; opportunity to provide a better service; opportunity to provide a better, cheaper product. . . technology only exists to make the impossible possible, not to satisfy engineering purism, or any other dogma."

Andrew Vere strongly attacked the existing broadcasting duopoly of BBC/ITV: "It is as a direct result of standards and manufacturers supplying that duopoly, whose only interest was their own (technical) standards, which is in part responsible for the pathetic position we have today. . . it's an absolute tragedy that we now produce not a single British camera or a single British VTR – a direct result of standards and of manufacturers supplying that duopoly, whose only interest was their own standards and requiring equipment which in the main had no international market."

He believes that multi-channel television will bring new opportunities, ending an era of high audiences for bad programmes. "No longer will programme makers need to own their own studies – independent facilities companies could do it all cheaper and faster, with their talent in specialized areas and providing equipment to cope with every conceivable recording format and technical goody – disc and tape recorders, D1, D2, components, composite, MII: there are no problems, no challenges, there are only opportunities."

The largely engineering audience seemed uncertain how to respond to this forthright, highly political denouncement of their cherished belief in the vital importance of international technical standards. Ken Barratt (Sony Broadcast), as chairman, commented that Andrew Vere's remarks "were fighting talk", although he readily admitted that, "A standard designed to meet all future eventualities will be over-designed and will not meet all eventualities". His colleague John Ive spoke convincingly in favour of standards, insisting that manufacturers as well as broadcasters needed the commitment and protection they provided. But he questioned whether, in an era of fast moving technology, committees meeting only once or twice a year could respond quickly enough to changes. Digital television made it far more difficult to modify the basic parameters of a standard and greatly increased the "need to get it right first time."

Even the much-acclaimed "universal" 4:2:2 digital standard (CCIR Rec 601/656) is not without its problems. It is now recognized that, for front-end processing, 10-bit rather than 8-bit encoding is desirable; only a degree of imprecision in the wording of the standards permits 10-bit operation without breaching them. Mike Cox (Cox Associates) commented that the International Association of Broadcast Manufacturers has recently set up a technical sub-committee looking at standardization procedures: "EBU takes forever – we want to speed things up for the benefit of the market".

Most of the colloquium speakers avoided the controversy, concentrating on the technical aspects of interconnecting television studio equipment in a mixed composite and component, analogue and digital environment. Mike Croll (BBC Research) concluded that "The technical challenge is to maintain control of the way facilities and their integration develops. The price for getting it wrong could be expensive both in cash terms and in being stuck with limited technical quality at a time when viewers' perceptions of picture quality may be increasing." Without safeguards, he suggested, as many artefacts could be introduced into analogue-component systems as are found in PAL.

David Bradshaw (BBC) described various options in routeing digital signals. For short distances a bit-parallel mode is common but for longer inter-studio connections a serial format can reduce costs. As the costs of parallel/serial conversion fall, serial formats may become attractive even within studios or technical areas.

Paul Dubery and Lionel Durant (Tektronix) described the new techniques developed for measuring analogue-component and digital-composite (D2) formats including the use of "bowtie" test signals and "lightning" displays.

Here and there

Keith Roberts, acting manager of BBC Essex, points out that it is *his* station and not Essex Radio (ILR) that is taking part in the BBC's experimental RDS traffic information service (*E&WW*, March 1989, page 316). My mistake, but after all Essex Radio (born September 1981) was using the county name long before latecomer BBC Essex, not even to be found in my 1986 BBC Handbook!

● Radio Communications (*E&WW*, March 1989, page 314) quoted accurately from a DTI/RIS open letter on the EC EMC Directive that could be read as implying that amateur self-built transmitters might have to be submitted for the expensive process of type acceptance. Inquiries show that this was due to an unfortunate ambiguity in the drafting of the RIS letter and that fortunately there is no intention to impose type acceptance on amateur home-built equipment. The component parts of commercially-marketed kits and commercially marketed equipment will need to comply with the Directive. It is also possible that a technical specification for amateur transmitters/transceivers may be drawn up.

● According to the *New Scientist* Japan is now the world's leading scientific nation in effort if not always in achievement. More than a quarter of all scientists in the developed world are now Japanese. They outnumber the combined scientific establishments of the UK, France, West Germany and Italy.

● The IBA has begun test transmissions in Nicam digital stereo in the London area. They are being transmitted from Crystal Palace and its dependent television relays on both ITV and Channel 4. Full Nicam test transmissions have just started also from Emley Moor and the dependent relays in the Yorkshire region. A preliminary service is due to start in September. Until then, transmissions may include material that is not related to the normal television sound. Many Nicam television sets and VCRs automatically select the Nicam output; and until September, if test tones are received, it will be necessary for viewers to de-select the Nicam signal.

Nicam's originator, the BBC, is now to start its long-delayed stereo tv sound service in the autumn of 1991. The initial service on both the BBC-1 and BBC-2 networks, will be from seven principal transmitters on the UK mainland, plus many of their dependent relays, and will be available to 60-70% of the population. In the meantime, test transmissions in the London area will continue with programme sound, mono or stereo, in the digital channel.

Direction-finding update

Some of us still tend to associate direction-finding with the pioneering days of "wireless": simple rotating loops, Bellini-Tosi loops, HF Adcock systems with the receivers underground in large tanks etc. The progress made with enormous circular Wullenweber arrays, Doppler interferometers and the like has tended to come under military or sigint security umbrellas. It is noticeable that since the "ABC" trial at which Duncan Campbell was able to point out that much of his information came from published conference papers, few papers (on any subjects) have been launched into the public domain from such establishments as GCHQ.

Looking in at an IEE colloquium on "Passive direction-finding" recently, the interest appeared to be almost exclusively in the military field. I soon discovered that D/F has become a technology dependent on sophisticated computer algorithms used with adaptive multi-element arrays; even familiar terms such as Adcock systems seem now to be dominated by mathematical analysis.

STL in association with RSRE have shown by means of a systolic array demonstrator that it is possible to use an adaptive array designed to null out several jamming sources to provide also bearing information on the jammers.

Graham Stott (Racal-Decca) noted that electronic support measures (ESM) face an increasing requirement to achieve greater elevation coverage with the capability of measuring a signal direction vector (i.e. azimuth and elevation simultaneously). High performance military aircraft require complete spherical coverage and vector D/F information for countermeasures.

Dr Richard Haemmerie (Rohde & Schwartz) gave a mathematical analysis of the factors limiting the accuracy of Doppler and Adcock systems, concluding that both introduce system-inherent and statistical errors so that the choice of which system to use depends on the particular application.

A comparison of algorithms for multi-element D/F techniques, given by D.S. Hill (Plessey), was based on five representative algorithms: Adcock (digital implementation); scanned fixed beam (SFB); scanned adaptive beam (SAB); MUSIC (eigenanalysis of the covariance matrix estimate); and noise space projection (NSP).

A paper on a "precision multitarget tracking system" due to be presented by S. Rehnmark (Anaren Microwave) had to be withdrawn as it had not received US clearance – a further demonstration of the sensitivity that now surrounds the art of D/F.

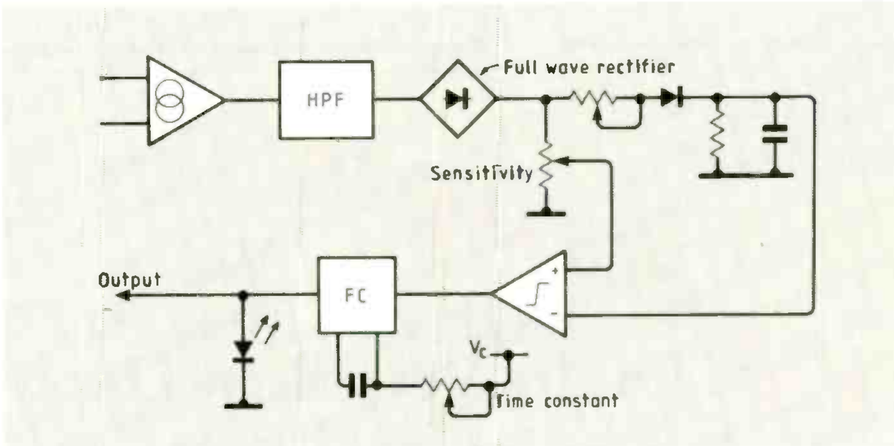


Fig. 6. Scratch detector. The high-pass filter has cut-off frequency of 500Hz and a slope of 12dB/octave.

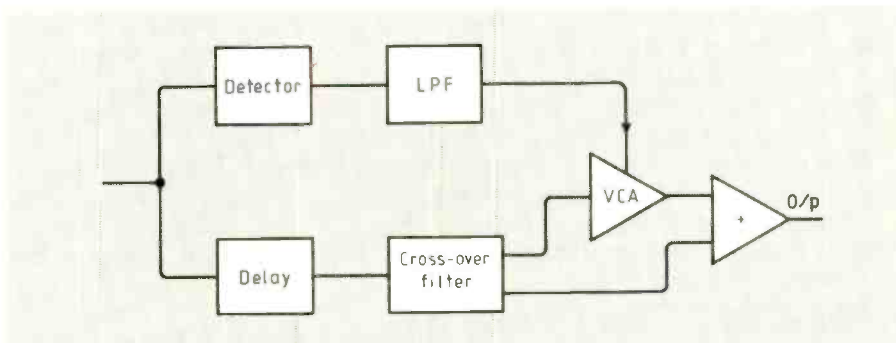


Fig. 7. Outline of the Polish "sound cleaner". VCA is a Polish WRN-03 temperature-compensated device providing up to 90dB attenuation with very low distortion.

Analogue "sound cleaner"

Miroslaw Królewski of the Polish Radio Laboratory for Recordings Reconstruction, Warsaw, is convinced that despite the growing acceptance of new digital audio techniques, there will remain for many years a need both for broadcasters and listeners to play out analogue recordings. This is not only because of the large libraries of recordings built up over many years but also because the great majority of recorded material is, and is likely to remain, available only in analogue form.

He believes that the major disadvantage of analogue recordings is that the quality deteriorates with age and is susceptible to mechanical damage. For professional play-out there exist systems which can considerably reduce the noise level of old recordings (e.g. the EMT 258 noise filter). Dynamic range expanders and several techniques for reducing clicks and pops have also been devised.

In OIRT's *Radio & Television* (1988/6, pages 40-45) Krolewski describes an electronic system he calls a "sound cleaner" which, he claims, reduces clicks and pops to a useful degree although capable of being further developed in a form where it could be attached to any record-player as a standard facility. His prototype unit achieves a time delay by the use of two recorders; but these could be replaced by, for example, a SAD1024 chip.

His sound cleaner is, in effect, a form of noise-blanker that operates only on the higher audio frequencies, leaving frequencies below about 500Hz unaffected. It comprises an electronic scratch detector (**Fig. 6**) and a "deleter" (**Fig. 7**). When a scratch is detected, the device blocks only the high-pass branch and the continuity of the low-frequency components is maintained. Since lower frequencies tend to predominate in music, this approach eliminates fluctuations in the output signal even in the presence of a large number of scratches. The envelope detector-follower has its time-constants adjusted so that it follows the envelope of the musical programme with reasonable accuracy without reacting to short impulses, permitting the comparator and associated circuitry to work properly over a large range of input voltages.

RF Commentary is written by Pat Hawker.

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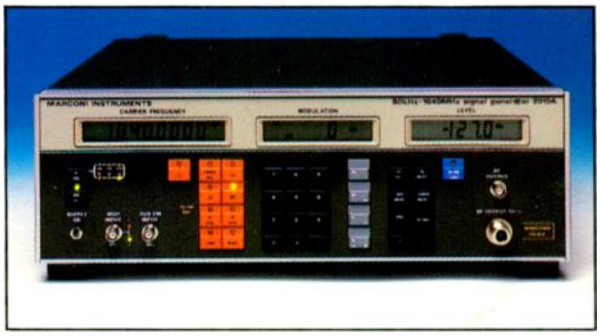

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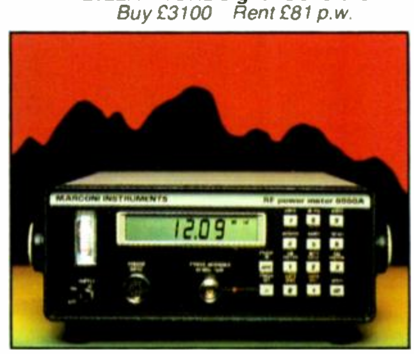

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