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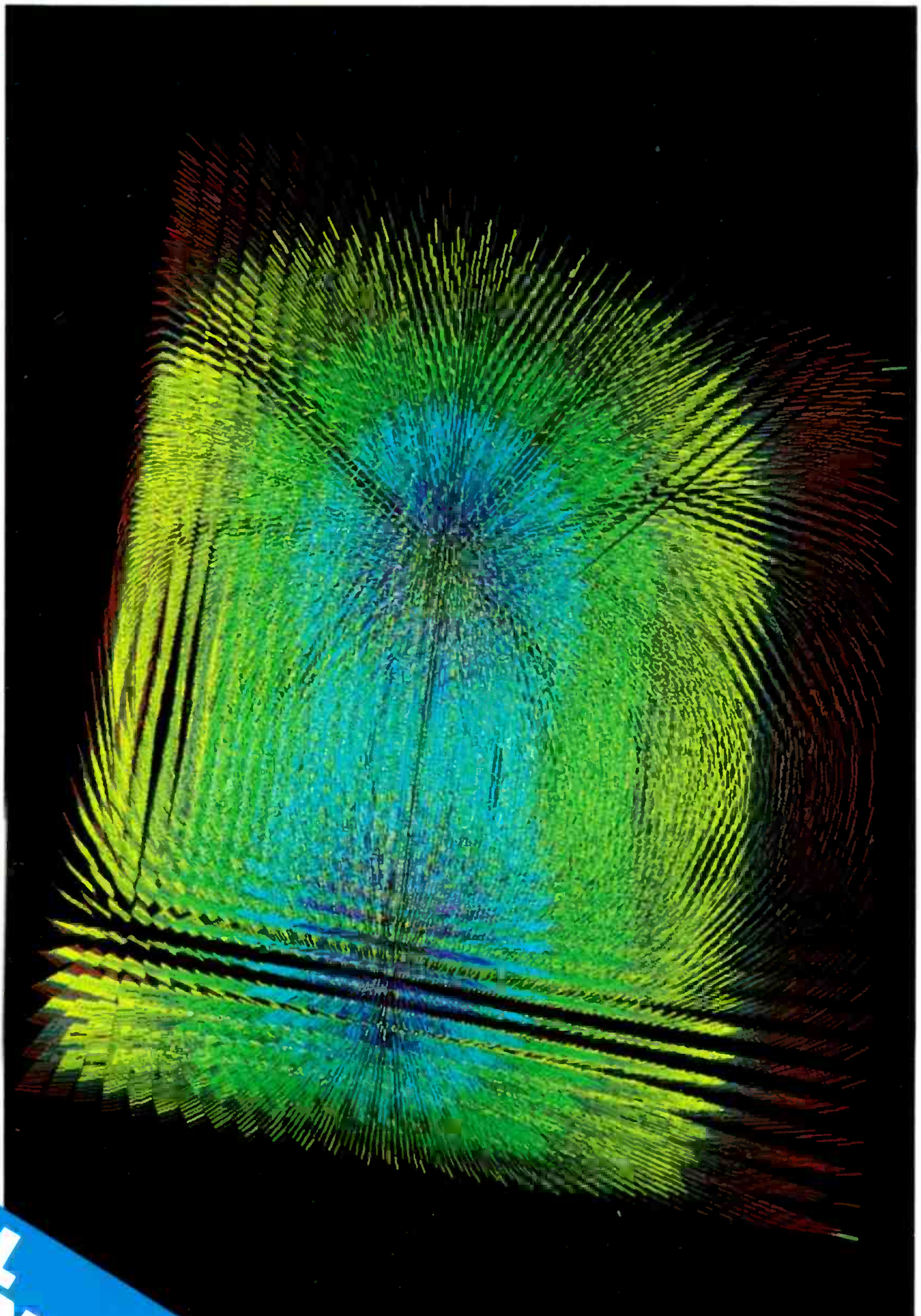

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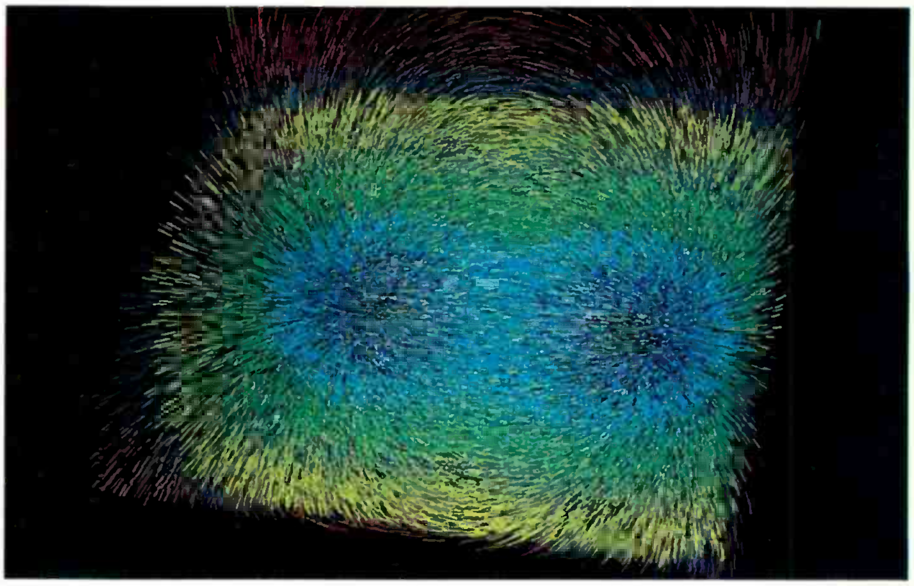

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The calculations were done on a 1000-processor DAP computer by Active Memory Technology of Reading.

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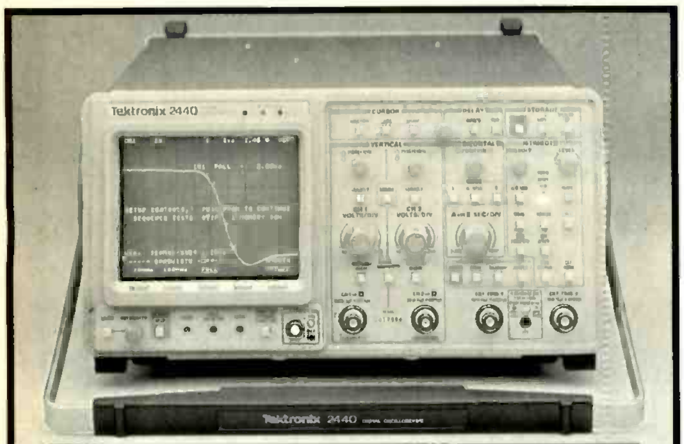

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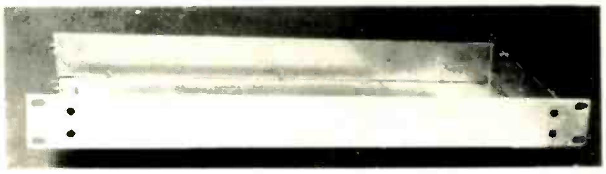

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COMMENT

Rupert and his PALs

For all save those connected with Rupert Murdoch's Sky Television, its decision to adopt PAL transmission represents a disappointment – if not a full-scale technical calamity. Provided that the launch in November is successful, the Astra satellite's f.m. carriers will relay Sky's four-channel package using the existing terrestrial encoding standard. Never mind the Europe-wide agreement to use MAC for future services: MAC decoder chips may not be available in quantity until this time next year, and the commercial interests who will finance d.b.s. television cannot wait. So they are using their commercial muscle to force the issue. Receiving terminals will go on sale in the high-streets at a mere £199 – a price which may well find our entertainment-hungry public thronging the pavements outside Dixons six deep, so long as the pictures it is offered are coloured sufficiently brightly.

But what does this development mean for the future of d.b.s. television? To an already confused situation, Sky has contributed a sizeable helping of further uncertainty. At some stage the public will discover that the Amstrad terminals it has lugged home are incapable of receiving any of the other proposed d.b.s. services. Most of these will be in the 12GHz broadcast band, while Astra is in the 11GHz links band. And no-one has yet promised us a wideband front-end which can cope with both. Many channels will come from satellites at other orbital stations, calling for a complex steerable dish or even a separate terminal altogether. Many, including those originating in mainland Europe, will be in the D2MAC format; and very likely some of the remaining 12 services on Astra will be among them. A rival Astra passenger could be the newly-announced BT-Maxwell-W.H. Smith consortium, which has allied itself with DMAC. Other programmes, including British Satellite Broadcasting's three DMAC channels, will be encrypted and will be unwatchable without a decoder approved by the broadcaster.

It is hard to imagine what viewers will make of all this. Certainly it will prove both complicated and costly for the public to equip itself fully to enjoy the broad spectrum of programme choice which the British Government seeks to foster.

It remains just conceivable that Sky will some day find itself alone in a world of MAC broadcasting; and, putting on a brave face, will decide to conform. But in the meantime British audiences will have suffered an unnecessary, destructive and expensive standards battle – along the lines of the VHS-versus-the-rest v.c.r. wars of the last decade, where the winning system is not necessarily the best one and the public gets left with a lot of redundant plant. Murdoch, who is either laughably misinformed about MAC's advantages or else afflicted with a Nelsonian eye, dismisses MAC as a conspiracy among European manufacturers to make everyone buy another television set (by which he presumably means an additional r.f. front end). But that is what Sky will do too.

Whatever happens, Britain may well have been cheated of a unique opportunity for a worthwhile yet relatively painless improvement to its television system. Better colour pictures were only a part of the MAC package. By locking us into PAL for the foreseeable future, Sky is also snatching from us the benefits of multi-lingual sound channels, auxiliary digital radio services, expanded teletext and data capacity, and the prospect of an easy path to compatible high-definition television.

In the meantime, how's this for easy money? Murdoch's partner Alan Sugar of Amstrad has offered £1M in cash to anyone who can show him a better picture than you get on a PAL set. Readers who work for Plessey, Philips, ITT, Nordic VLSI, the BBC or IBA should contact him care of Amstrad Consumer Electronics.

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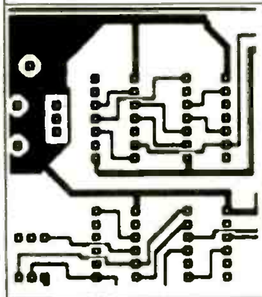

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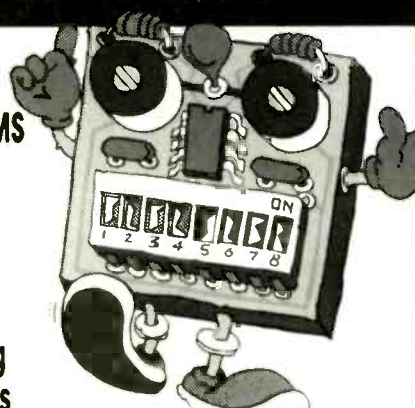

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Introduction to d.s.p.

This article raises and answers some of the questions asked by those working in digital signal processing for the first time.

ALAN SEWARDS

ABOUT DIGITAL SIGNAL PROCESSING

By d.s.p. here we mean sampling an analogue signal and converting it to digital form with an analogue-to-digital converter, forming the samples into blocks of fixed length (such as 512 or 1024 samples), and processing the resulting time series by means of a fast Fourier transform. This article discusses the principal problems associated with each of these stages. Illustrated in the graphs are the effects of sampling, quantization into a number of bits, clock jitter and sampling aperture time. The text is non-mathematical and explains the various effects in simple terms. The examples use single sinewaves of different frequencies and the power spectra produced by FFTs of 1024, 512 256 and 128 samples. Notional sampling frequency is 19200Hz and the signal frequencies displayed are 131kHz, 150Hz, 262.5Hz, 1106Hz, 2381Hz, 4781Hz, 9125Hz, and 9469Hz. Similar effects will be obtained with any proportional set of frequencies: for example, sampling at 19MHz, with signal frequencies of 131kHz, 2.381MHz etc. Except where stated, the graphs of power spectrum plot decibels relative to the maximum value against frequency, with the x-axis covering 0-9600Hz. Vertical grid lines are 1200Hz apart; horizontal lines 20dB apart.

Most engineers are used to thinking of waveforms in terms of continuous functions: sinewaves produced by a signal generator, for example, which can be assumed to have started an infinite time ago and to continue for an infinite time into the future. Everyone knows that when you switch on a signal, a transient is produced, which results in a wide spectrum for a short time. Similarly, if the signal is switched on and off periodically, such as by pulse modulating a carrier, we see the spectrum of the signal modified by the effects of the pulsing. However, few realise when getting into digital signal processing that very similar effects are implicit in the processing, effects which result in modifications to the original signal and hence to the output of the digital processor.

The two most important effects of this type arise as follows: the fact that the signal is not continuous, but sampled, and the implicit assumption that the signal outside the collected block repeats what is in the block from past to future infinity.

Sampling of the continuous signal results in a series of numbers that fully define the signal according to the Nyquist theorem, provided that at least two samples are taken of the highest frequency contained in the signal. For real number sampling, the highest signal frequency for which this relationship is maintained is called the Nyquist frequency. We will return to the sampling frequency in a moment. Owing to the sampling process, we see the input signal as through an opaque fence with narrow gaps between the boards. For frequencies low compared with the sampling frequency, we get many samples per cycles, and the shape of the waveform is preserved as seen through the fence. As the frequency gets higher, the number of samples per cycle decreases until, near the Nyquist frequency, it is difficult to recognize by eye the input signal through the fence (Fig.1,2).

The second effect is more subtle and far-reaching in its impact. We noted that the signal samples are collected into blocks and then processed. These blocks are usually powers of two if the fast Fourier transform (FFT) or its derivatives are used (but do not have to be). If the sampling is such that a complete integer number of cycles of the input signal is contained in the block, it is easy to see that copying the block and placing the copies before and after the current block will result in smooth transitions at the block boundaries. However, if there is exactly an odd integer number of half cycles of the input signal in the block, there will be a strong discontinuity at the block boundaries (Fig.3,4).

Since the FFT process assumes continuity, in the latter case it thinks it is dealing with a signal with a periodic half-cycle discontinuity. Clearly such a signal will have a spectral content not present in the original signal, and this content appears in the FFT output, as we shall see. Another aspect of the block arises from the fact that, even though we have assumed the signal is continuous, in fact we have no knowledge of it outside the block.

WINDOWING

The effects discussed above produce some interesting results. First, the fence appears in the output of the FFT, meaning that we can only see the spectral content of the input time series as through the fence. Second, because of the finite time window which the block of data represents, the spectral content of the signal is spread. Third, the discontinuity resulting from any condition other than that where an integer number of full cycles of the input signal is present in the block results in spectral spreading, whose magnitude and appearance depends on how bad the discontinuity is. Figure 5 shows the power spectrum of the signal of Fig.3. (150Hz), which has no discontinuity, and Fig.6 the spectrum of a similar signal (Fig.4) with the maximum discontinuity (131Hz). Note the vast differences in the power spectra.

These spectra were obtained by using the raw time series sampled data in the block. As

Fig.1. Sampling a low-frequency signal (150Hz).

Fig.2. High-frequency signal (9125Hz): the sampling frequency makes it difficult to see the waveform.

Fig.3. With this 150Hz signal, the blocks of sampled data represent a whole number of cycles.

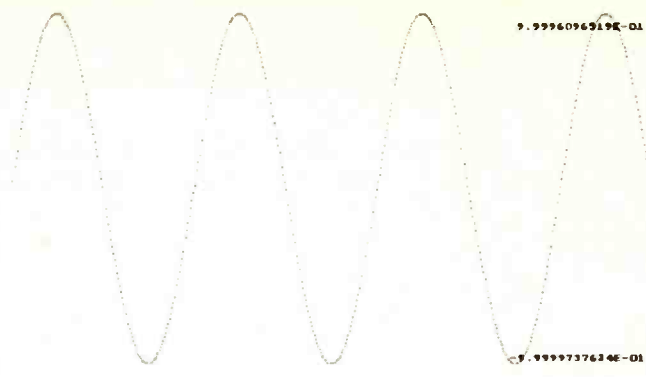


Fig.4. Changing the signal frequency to 131Hz results in an odd number of half-cycles per block, and a marked discontinuity at block boundaries.

each of the samples has the same weight as any other, this is called a rectangular window (also known as the Dirichlet window), meaning that the input signal is seen as through a window which is zero outside the sampling period and unity within the block. Because the discontinuity has its worst effect at the beginning and end of the block, one can effect an improvement in the spectral spreading by using a window which reduces the influence of the beginning and end data samples. A large number of these windows have been devised[1].

One of the windows commonly used is the Hann window. Although far from being the best window in terms of minimizing spectral spreading, it has the merit of being exceptionally easy to generate. It is a (cosine) squared window applied to the input signal (i.e. in the time domain), being zero at the start and finish of the block (Fig.7).

The window can also be applied in the frequency domain by a simple smoothing process – each spectral value is replaced by the sum of −0.25 times its neighbours plus 0.5 times itself. The effect on the spectrum of Hann weighting on the signal of Fig.7 is shown in Fig.8. There are many much better windows than the Hann, but few as easy to implement.

Spectral leakage of the signal due to the discontinuity also depends on the number of samples in the block. This is because the width of the spectral peak and hence of the sidelobes is dependent on the number of samples. The more samples in the block, the longer the time duration of the signal processed, the narrower the peak, and the closer to the signal frequency cell the asymptotic fall-off of the window begins. This fall-off is 6dB per octave for the rectangular window, and 18dB per octave for the Hann window. Figures 9 to 16 show the spectral leakage plots for a signal with maximum discontinuity (1106Hz) for rectangular and Hann windows for 1024, 512, 256 and 128 samples per block. Note that the last line visible on the right of the Hanned examples has a high value because it has not been averaged.

SAMPLING FREQUENCY

According to the Nyquist criterion, if the signal of interest is to be fully recovered from the samples, there should be at least two samples per cycle of the highest frequency contained in the signal. Shannon showed that any band-limited signal can be represented by its samples, provided that the sampling frequency is at least twice the frequency of the highest Fourier component contained in the signal of interest. These reduce to the same thing except when I and Q sampling is done: the signal can be fully described if one I and Q sample are taken per cycle, meaning the sampling frequency can be the same as the highest frequency in the signal.

Another way of looking at this is that with normal time sampling, only the real array of values is filled with samples, the imaginary array being filled with zeroes. Thus there are 1024 actual values in the 2048 slots of the

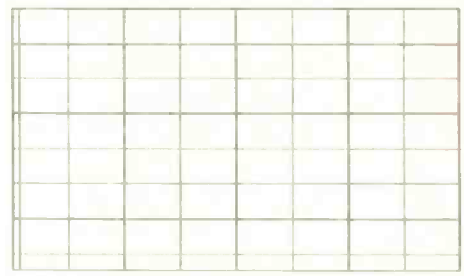


Fig.5. Power spectrum of the 150Hz signal in Fig.3. Vertical intervals are 20dB.

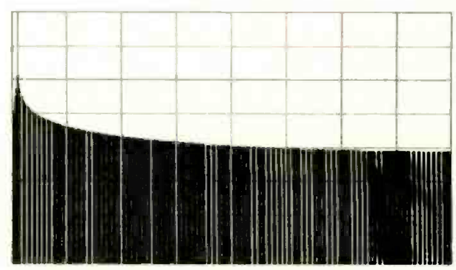


Fig.6. Power spectrum of the signal of Fig.4. The striking difference between this and Fig.5. is due to the discontinuity at block boundaries.

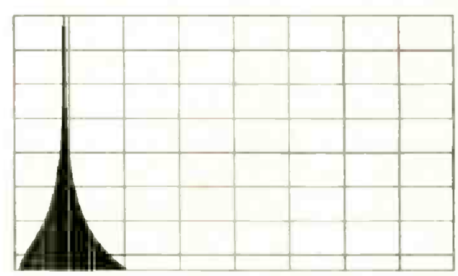


Fig.8. Spectrum of the Hanned signal, below left.

Fig.7. Using windowing to reduce the effect of discontinuities: a Hann window applied to an 1106Hz signal, seen in the time domain.

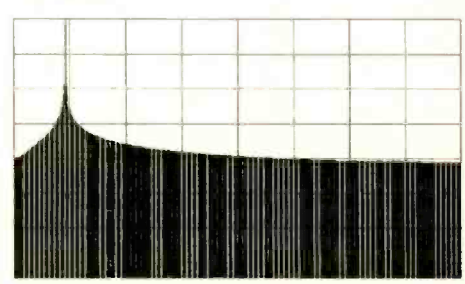


Fig.9. 1106Hz signal (i.e. maximum discontinuity): 1024 samples, rectangular window.

Fig.10. 1106Hz signal (as Fig.9), Hann window.

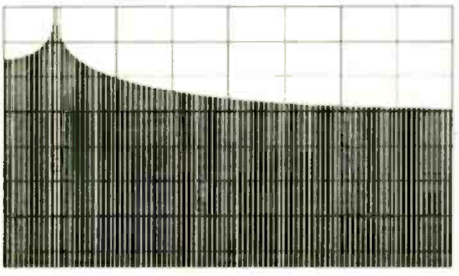


Fig.11. Rectangular window, 512 samples.

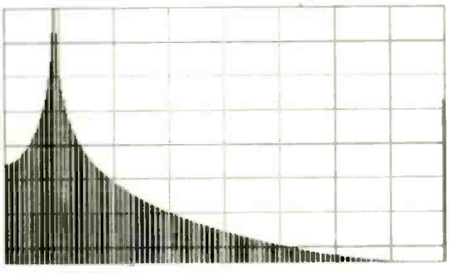


Fig.12. Hann window, 512 samples.

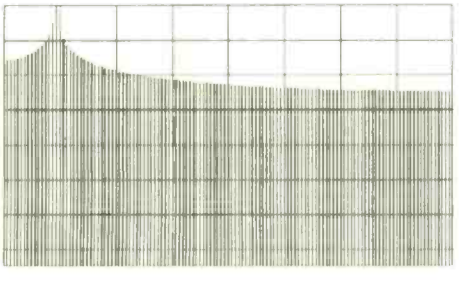


Fig.13. Rectangular window, 256 samples.

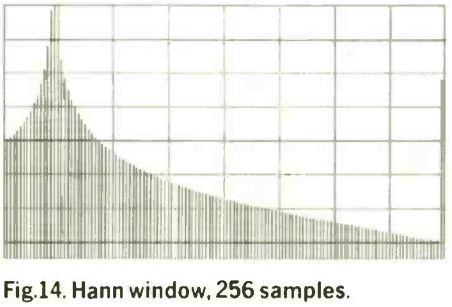


Fig.14. Hann window, 256 samples.

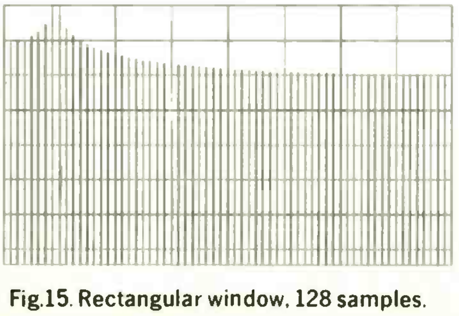


Fig.15. Rectangular window, 128 samples.

real and imaginary arrays. If I and Q sampling is used at half the above sampling frequency, every other element of both the real and imaginary arrays will be zero, but, at the sampling times, both a real and an imaginary value will be obtained. We finish with 512 pairs of values, amounting to 1024 as before.

In practice, it is necessary to filter the signal to remove components above the Nyquist frequency which would otherwise be undersampled and folded down into the range of interest, appearing as phantom non-existent components. The need for this analogue filter before the a-to-d converter, and its finite cutoff slope, means that the Nyquist frequency must be typically 10-20 percent higher than the maximum frequency of interest: and for real sampling, the sampling frequency must be twice the Nyquist frequency. Figures 17, 18 show how a frequency above the Nyquist frequency is folded down into the baseband spectrum. The higher frequency signal is actually at a frequency 15 times the lower frequency rather than the three times it appears, but is still less than the sampling frequency.

RESOLUTION

While the windowing procedures discussed above do result in reduced spectral leakage, this is not obtained without cost. As might be imagined, the width of the signal peak in the frequency domain depends on the length of time represented by the signal in the block of samples. (To a first approximation, the resolution is given by the reciprocal of the time represented by the samples in the block.) If weighting is used, this effectively throws away samples at the beginning and end of the block, reducing this time. Thus the width of the main lobe of the response increases. As compared with the rectangular window, the Hann weighted signal will have a main lobe width about 1½ times as wide. This can be seen in Fig.19, 20, for a block of 1024 samples of 131Hz. In these figures, only the first 64 spectral lines are plotted in order to show the main lobe widths.

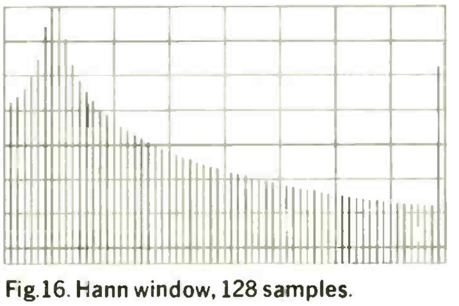


Fig.16. Hann window, 128 samples.

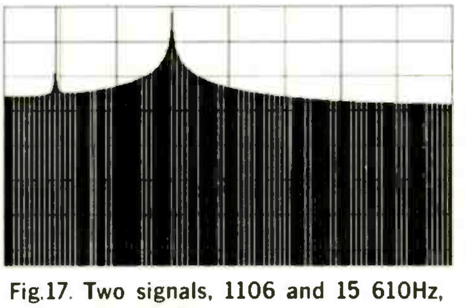


Fig.17. Two signals, 1106 and 15 610Hz, rectangular window.

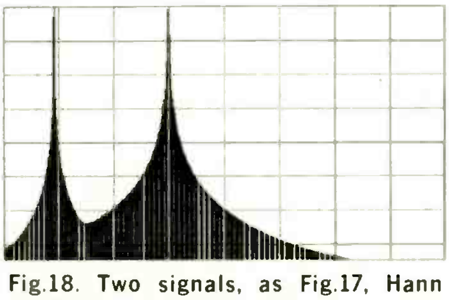


Fig.18. Two signals, as Fig.17, Hann weighting.

The width of the main lobe is also affected by the number of samples in the block, and hence the length of time of signal represented in the block. The effect on the main lobe width of reducing the number of samples can be seen in Fig.9-16.

Resolution is important in the detection of a signal close to another signal. If the signals are of comparable amplitudes and close together, it may be possible to see the two spectral peaks in the frequency domain if a rectangular window is used; if the Hann window is used the peaks may merge and blur. In contrast, if the second signal is much weaker than the first but a little further away in frequency, spectral leakage from the rectangular window from the strong signal will obscure the weaker, while the Hann weighted process will allow the weak signal to be seen. This is well covered in reference 1, where descriptions can be found of windows which do a better job of obtaining narrow peaks and small spectral leakage.

PICKET FENCE EFFECT OR SCALLOPING

As we have seen (Fig.19, 20 and elsewhere), with a rectangular window the peak of a favoured signal (one with no discontinuity) occurs in one spectral line while that of a non-favoured signal is shared between two spectral lines. Not obvious from the figures (as the plots are normalized) is the power loss that results. Figures 21 and 22 show graphs of the first 50 points of two signals, one favoured and one not, for rectangular and Hann windows. The maximum spectral power of the non-favoured signal can be seen to be about 4dB less than that of the favoured signal for the rectangular window case, and about 1.5dB for the Hann case.

The smaller loss in the Hann window is due to the spectral averaging that occurs. As the input signal frequency is varied, the spectral power fluctuates up and down, going from a peak on one line, to be equally split between two lines and then back to a single line again. The effect is due to the sampling property discussed above, resulting in the viewing of the sinc x response (in the case of the rectangular window) through the fence used as an analogue earlier. When the sinc x peak is aligned on a gap in the fence (i.e. on a spectral line), only the peak is seen, as the sinc x function is zero at all the other gaps in the fence. When the sinc x function is aligned centrally on a board of the fence, one sees the two −6dB skirts of the peak in the two adjacent gaps. Intermediate positions produce different relative amplitudes of the two skirts. For the Hann window, the response function is broader and a different shape, but the same principles hold.

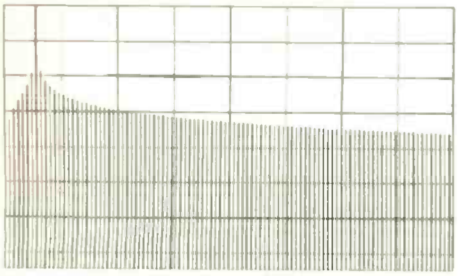


Fig.19. Spectrum, 1024 samples, rectangular window.

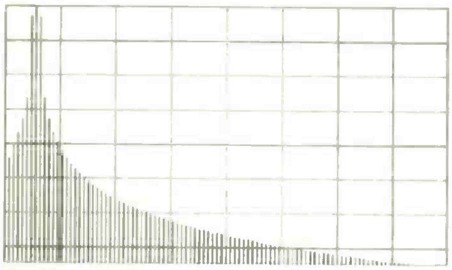


Fig.20. Spectrum, 1024 samples, Hann window.

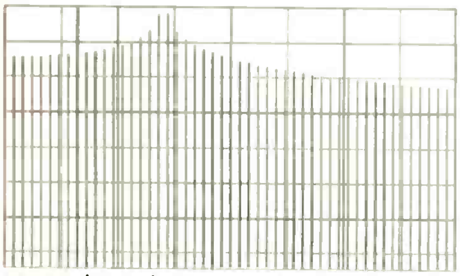


Fig.21 (above). Frequencies 150Hz and 382.5Hz, rectangular window.

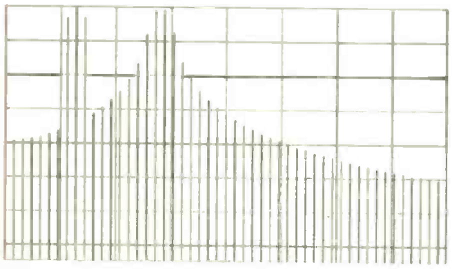


Fig.22 (above). Frequencies as Fig.21, Hann window.

QUANTIZATION

Analogue-to-digital converters sample the signal, theoretically at least, at equally spaced instants of time, and quantize the signal into one of a number of levels, this number depending on the number of bits produced by the converter. Thus a 10-bit a-to-d has 1024 possible levels for the signal, provided the full dynamic range of the converter is used. A one-bit a-to-d has only two levels. Since the input signal is continuous, quantization means that the sample which represents the signal at the sampling point will not in general be exactly the same as the actual signal value. This error, which gets larger as the number of bits is reduced, is called the quantization error, and the resultant spectral effects are called quantization noise. A signal at 131Hz, quantized by a four-bit a-to-d is shown in Fig.23.

Obviously it is desirable to use as many bits as possible to reduce the quantization noise. But as before, this has a penalty: more bits mean a more complex and expensive a-to-d and in general a slower a-to-d. Even if the a-to-d can produce the bits, more bits in processing cost memory space in storing the data and time in manipulating it. There is always a compromise here.

Figures 24 to 30 illustrate the spectral effects of reducing the number of bits on a signal consisting of a sine wave with the worst discontinuity (131Hz). It can be seen that for more than about four bits the effect is to raise the noise floor. For four bits or fewer, the effect is to produce harmonically related lines of such quantity that they resemble noise.

To understand why so many harmonics are produced, it is necessary to remember that the spectrum is folded back at both ends. This can be seen in Fig.30, but is clearer in Fig.31, where a sinewave signal at 262.5Hz is quantized to one bit, producing the familiar spectrum of a square wave (⅓ third harmonic, ⅕ fifth, and so on). At the

Fig.23. Four-bit quantized signal (131Hz).

DO NOT BE MISLED...

The examples shown in this article illustrate how important it is to understand what it happening when digital processing of signals is attempted. Those who do not understand may find the results difficult to interpret, and may draw quite misleading conclusions. For example, on the basis for Fig.6, it would be easy to conclude that there was a continuum of signals right across the band or an underlying noise spectrum, in addition to the single frequency signal. Similarly, failure to appreciate that some sampling jitter might be present could lead to the belief that an inadequate number of quantization bits was being used (Fig.38). Digital processing of signals, used properly and with knowledge, can produce remarkable results. When in doubt, consult some of the excellent authorities quoted in the references given at the end.

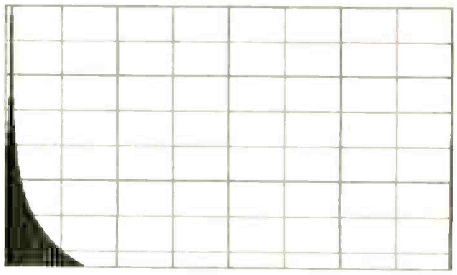


Fig.24. This and Fig.25–30 show the effects of reducing the number of bits on a sine-wave signal with the worst discontinuity (131Hz).

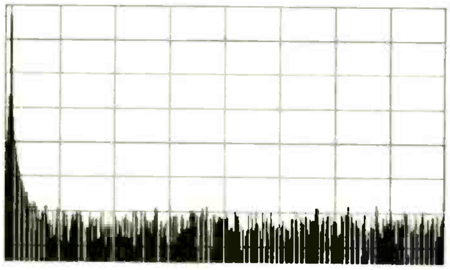


Fig.25. 16-bit quantization.

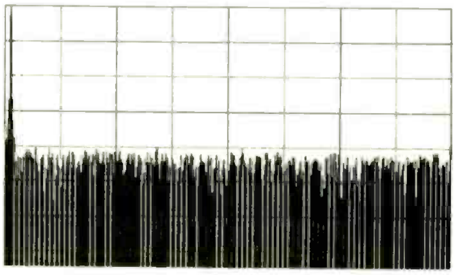


Fig.26. 10-bit quantization.

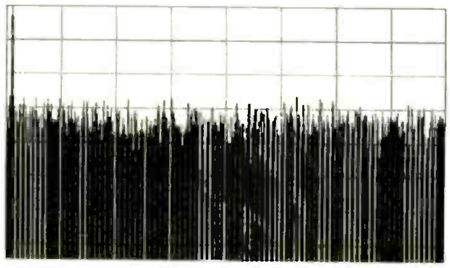


Fig.27. Six-bit quantization.

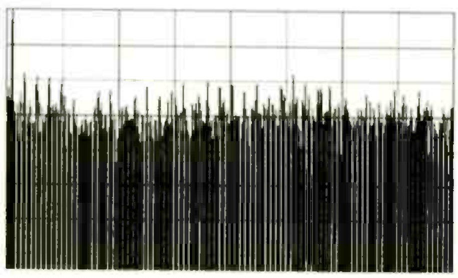


Fig.28. Four-bit quantization.

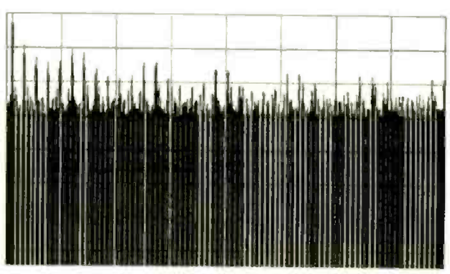


Fig.29. Two bits, Hann window.

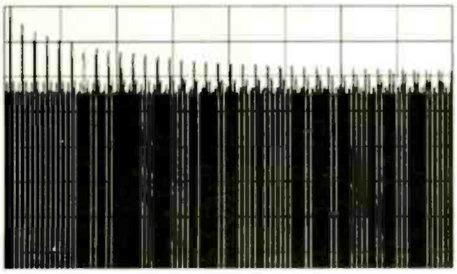


Fig.30. One bit, Hann window.

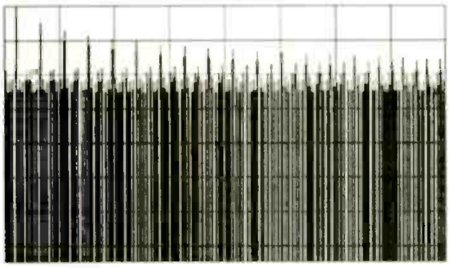


Fig.31. Sine-wave signal (262.5Hz), quantized to one bit, showing spectrum fold-back.

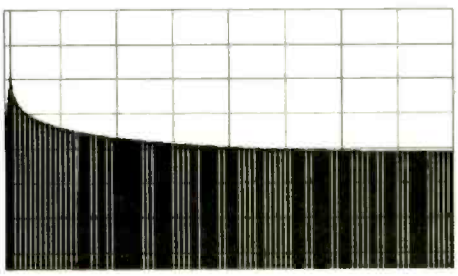


Fig.32. This and Fig.33–37 show the same spectra as Fig.24–30 for rectangular-windowed signals.

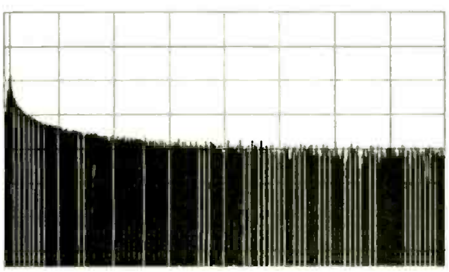


Fig.33. 10-bit quantization.

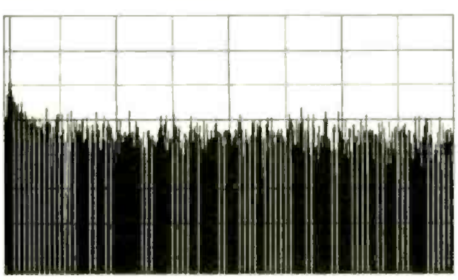


Fig.34. Six-bit quantization.

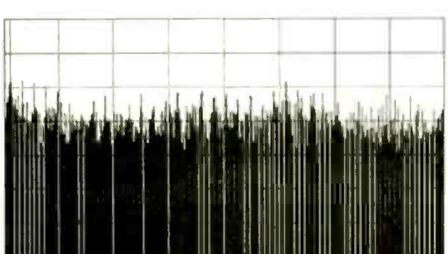


Fig.35. Four-bit quantization.

upper frequency limit (Nyquist frequency), however, the harmonic spectrum can be seen to fold back, and again at the low limit (zero frequency). Figures 32 to 37 show the same spectra as Fig.24–30 for rectangular windowed signals; and it can be seen that, once the leakage floor is crossed, the effects (as would be expected) are the same. It is interesting to note that the spectral leakage is such for this window that leakage dominates over noise effects resulting from sampling with 10 or more bits of quantization. Of particular interest is the prominent line visible for the four-bit quantization case some two-thirds across the band. This is the 45th harmonic.

A formula is often quoted to relate the quantization noise to the number of bits, viz. s:n = $6m+3n-1.25$dBm where m is the number of quantization bits and n the number of bits of signal enhancement (e.g. FFT) or processing gain. Using 10-bit quantization and an FFT of 1024 points ($n=10$), s:n works out at 88.75dB, quite close to what can be seen on Fig.26.

In considering quantization noise, we must bear in mind that the noise is harmonically related to the signals, and processing through integration or other techniques may not achieve the gain effects expected. This will certainly be the case for small numbers of bits; but for larger numbers of bits, the noise will behave more like true random noise in this respect.

SAMPLING JITTER

As mentioned above, the a-to-d is supposed to take samples at exactly equally spaced intervals of time. If this does not happen, the result is a distortion of the signal being sampled, with consequent spectral effects. In practice, the interval between samples often has a jitter with noise-like properties. In this case the effects is to raise the noise floor. However, there is one important difference between this case and that of quantization, both of which have an increased noise floor. The difference is that sampling jitter affects the higher frequencies more than the lower, because a high-frequency signal will change more in a given time than a low frequency. Figure 38 shows the effect of a small amount of jitter (modelled as a random noise shift about the correct sampling points) for a high-frequency signal, and Fig.39, 40, 41 for progressively lower frequencies.

Such jitter can occur when the a-to-d sample is triggered by a software process: software timing can easily be off by a few microseconds. Other causes can lie in poor design of digital logic. The giveaway is usually that the effect is worse for the higher frequencies.

Although the amount of jitter in this example is rather high (mean of 0.5% of the sampling interval), it corresponds to about one part in 100 000 of the time of one cycle of the lowest frequency shown (Fig.41) and produces a noticeable increase in the noise floor. Even one part in 1 000 000 of jitter produces a noise floor of approximately −120dB. A good goal to aim for is that the jitter shall be no more than the time corres-

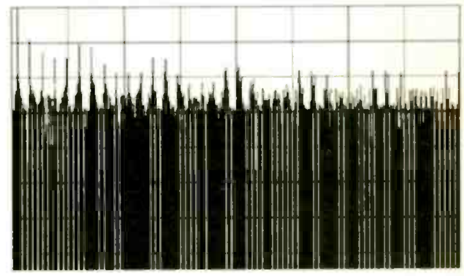


Fig.36. Two bits, rectangular window.

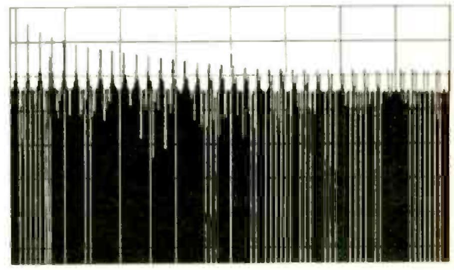


Fig.37. One bit, rectangular window.

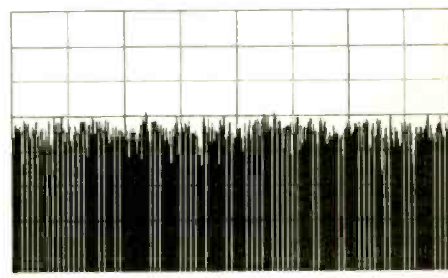


Fig.38. Effect of sampling jitter on high frequency signal (9649Hz).

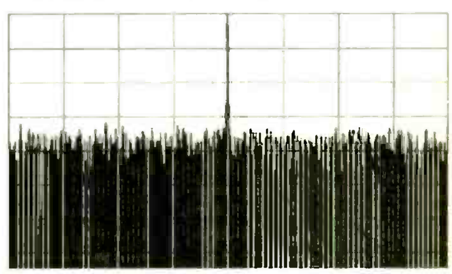


Fig.39. As Fig.38, but with a mid-frequency signal (4781Hz).

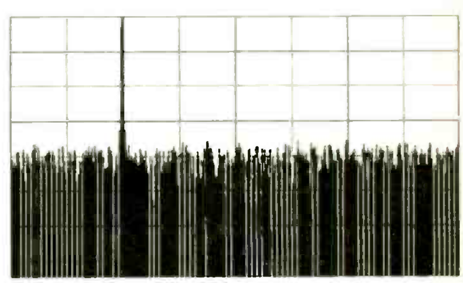


Fig.40. As Fig.39, but with a lower frequency signal (2381Hz).

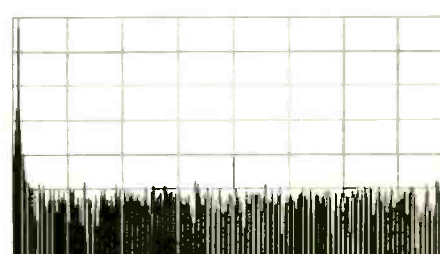


Fig.41. As Fig.40, but with a low frequency (131Hz).

HOW IT WAS DONE

The illustrations in this article were produced by a program (Digproc) written in Turbo Pascal Version 4.0 running on a Compaq Portable II (AT equivalent) computer, and displayed on an EGA display. The graphs (which appeared in colour) were captured by a ram resident program called Inset and written to disc.

Digproc uses a floating-point fast Fourier transform (FFT) which takes about ten seconds to perform a 1024-point complex transform. The program starts by requesting the signal frequency to be simulated, the number of bits to be used in quantization, whether or not a Hann window is to be used, the amount of jitter in the sampling time, and a parameter controlling the sampling aperture time. This is followed by a section which generates the desired signal and modifies it as specified, writing the resulting signal values into the X array and calling the Plot routine to display the sampled time series on the screen. The FFT is then called, doing an in-place transform. If a Hann window has been specified, the averaging process is then applied separately to both X and Y arrays. The power spectrum is the computed by squaring and adding. Finally, the power spectrum is displayed in dB relative to the maximum value, and plotted as lines to emphasize the line nature of the results.

It is of interest to note that the FFT is capable of using a fast sine routine which employs a table look-up process rather than calling the trig. functions. When Digproc is started, the sine table is filled, and thereafter can be used instead of sin and cos. This has dramatic effects on the computation time involved – the FFT time is approximately halved if this routine is used.

ponding to the highest frequency signal changing amplitude by one bit.

APERTURE TIME

Analogue-to-digital converters are specified with an aperture time associated with their sample-and-hold circuit on the input. This circuit opens a switch for a brief period (the aperture time), during which the voltage of the signal is transferred to a capacitor. The switch then opens, isolating the capacitor from the signal. At some later time, the a-to-d starts to convert the voltage on the capacitor to a digital number. If the aperture time is too long, the signal voltage can change significantly during it, resulting in a capacitor voltage which may not represent the signal voltage at the desired sampling instant. As in the case of sampling jitter, the aperture time should be chosen such that the highest frequency component in the signal does not change by more than one bit during the time. Effects from this cause can be difficult to track down, as different a-to-d designs do different things during the aperture interval.

References

1. On the use of windows for harmonic analysis with the discrete Fourier transform, Fredric J. Harris, *Pro. IEEE* vol.66, 51-83, January 1978.
2. Spectrum analysis – a modern perspective, Steven M. Kay and Stanley Lawrence Marple Jr., *Proc IEEE*, vol.69, 1380-1419, November 1981.

The Mosmarx voltage multiplier

A d.c.-d.c. converter with excellent efficiency.

P.E.K. DONALDSON

Two voltage-multiplying arrangements, originally designed by physicists for use in the laboratory and which work by switching charged capacitors, are shown in Fig.1. Both are presented in sextupler form. Figure 1(a) shows the Cockroft-Walton multiplier, configured for a unidirectional square wave input; the circuit is familiar to electronics engineers, who have adopted it for use in power supplies. There it provides a simple, if less flexible, alternative to voltage-changing circuits based on the charging and discharging of an inductance (switching regulators). Figure 1(b) shows a Marx high-voltage impulse generator[1,2], in which the capacitors are charged in parallel, via resistors, from a d.c. supply, and discharged in series via a string of spark gaps. I have often thought that the Marx configuration ought to be more satisfactory than the Cockroft-Walton for small d.c.-d.c. converters; to feed charge direct to each capacitor in the stack seems more elegant than pumping it all up from the bottom; yet I have never seen the Marx used. Recently the opportunity arose to compare the two arrangements: we needed a small, efficient device to make about 40mA at 44 volts from a 9 volt battery.

Figure 2 shows, in idealized form, the two phases of operation of a Cockroft-Walton multiplier. In 2(a) the generator, assumed to give unity mark-space ratio and be of low output resistance, supplies charge to the bottom capacitor on the right: simultaneously, the other left-hand capacitors supply charge to their opposite numbers on the right. In 2(b), the generator has zero output and is effectively absent. The right-hand capacitors supply charge to their opposite numbers up one storey on the left. The currents in the various branches, in terms of the output current i, are as indicated.

When a capacitance C_1, charged to a voltage V_1, is suddenly connected to another capacitance C_2, charged to a voltage V_2, current will flow until the voltages are in equilibrium, but the process is always accompanied by a loss of energy, however much or little resistance there is in the circuit. The loss is easily shown to be $(\frac{1}{2}).(C_1.C_2/[C_1+C_2]).(V_1-V_2)^2$. If a stabilized power supply of voltage E is suddenly connected to a capacitance C previously charged to V, the battery or power supply counts as a very large capacitor, so that the energy lost becomes just $(\frac{1}{2}).C.(E-V)^2$.

The Cockroft-Walton n-tupler carries out $2n-1$ such charge-transfers per cycle of operation, so it is important to minimize the rate of loss of energy at each transfer site. That implies that the capacitors should be large; for if C_1, charged to V_1, is periodically

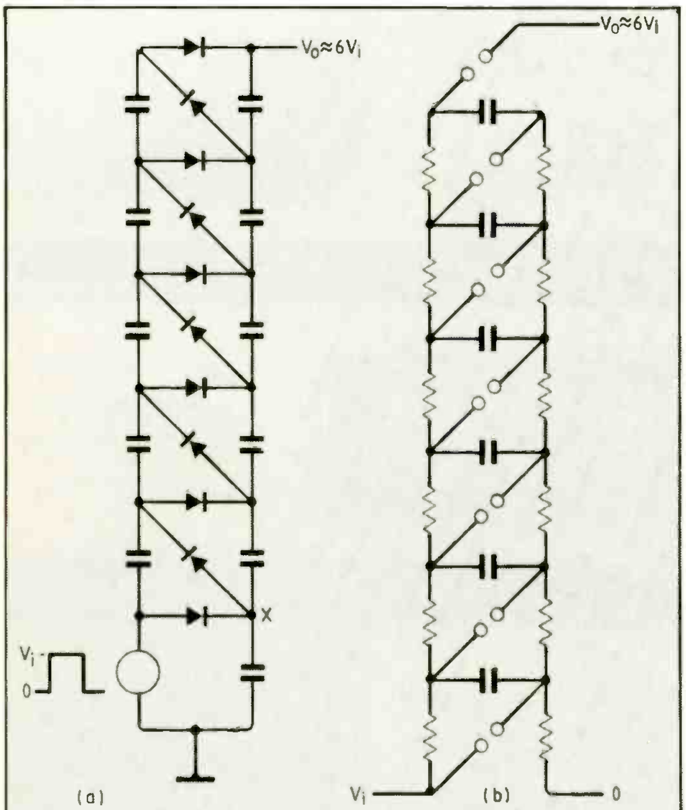
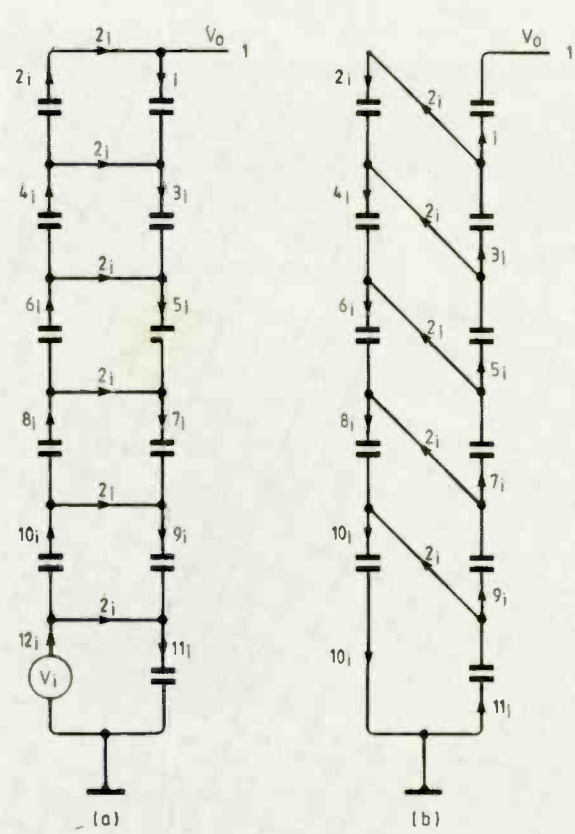


Fig.1(a) shows a Cockroft-Walton sextupler. At (b) is the Marx impulse generator. The spark gaps are arranged to break down under $2V_1$ but not, normally, under V_i. If the bottom gap is forced to break down by the firing of an auxiliary local discharge, the other gaps break down in quick succession from the bottom upwards, briefly connecting all capacitors in series. An impulse rather less than $6V_i$ in amplitude is available from the top of the machine.

Fig.2(a) shows the idealized current flow in the Cockroft-Walton multiplier when the generator output is 'high'. The idealized current flow when the generator output is 'low' is seen at (b).



connected to C_2, which is supplying current to a load and whose voltage had fallen to V_2 just before the connection is made, then doubling C_2 will halve V_1-V_2 and quarter $(V_1\text{-}V_2)^2$. $(C_1.C_2)/(C_1+C_2)$ cannot more than double, so the energy loss per cycle at the site of that transfer will be at least halved.

Granted that the capacitors should be large but that microfarads cost money and take up space, how large should they be? A reasonable basis is to let the ripple voltage across all capacitors be the same. For a converter working from about 10 volts input, a ripple of 100mV per capacitor is sensible. For the top right capacitor in Fig.2, the current is 40mA. For a 20kHz drive (a convenient frequency, see below) the duration of each phase is 25 μsec and

$$C = (i.t)/(\delta V) = 40\times10^{-3}\times 25\times10^{-6}/10^{-1}$$
$$= 10\,\mu F.$$

The other capacitors will be in the ratio of the currents through them; for the bottom right-hand capacitor, for example, the value would be 110 μF.

Figure 3 shows the two phases of operation of a multiplier in the Marx configuration. In 3(a), all the capacitors are separately charged by a current 2i, while the reservoir capacitor supplies the load current, i. In 3(b), the capacitors discharge in series with current 2i, of which i goes to the load, and i tops up the reservoir. Again, the capacitors are made proportional to their currents (apart from the reservoir) so they are all 20 μF.

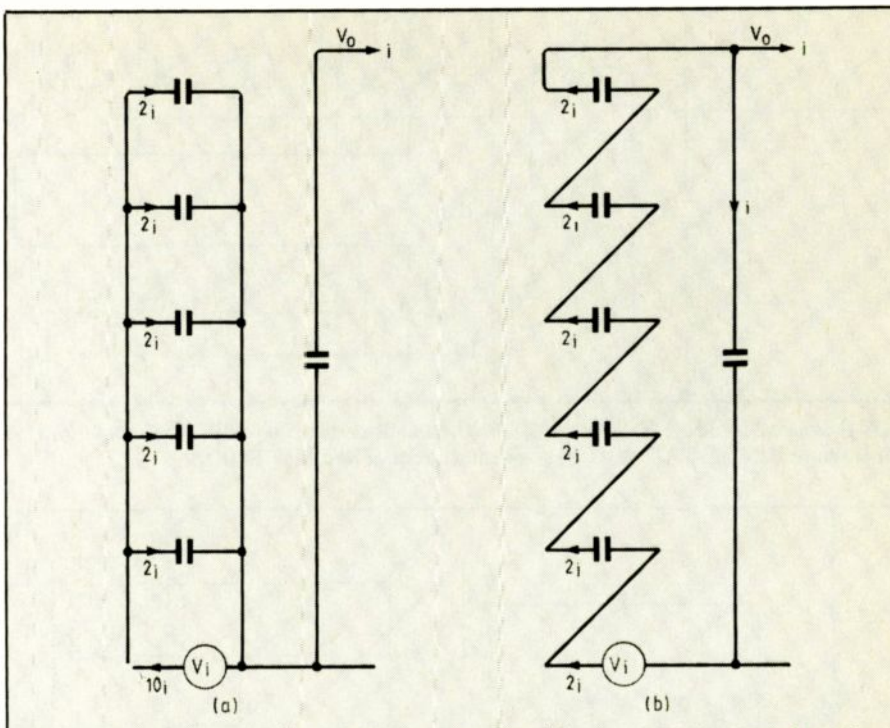


Fig.3. Charging phase (a) and discharge phase (b) of a multiplier based on the Marx configuration. Note the more uniform current flow, compared with that of Fig.2(a).

COCKROFT-WALTON CONVERTER

Figure 4 shows a practical d.c.-d.c. sextupler in the Cockroft-Walton configuration. Since there is a supply rail available at $+V_i$, the circuit dispenses with the bottom diode and bottom capacitor in Fig.1(a), connecting the point X instead to the positive rail; the sextupler is actually a quintupler standing on its supply rail. The reason for the strange arrangement of five p-channel fets in parallel, and five n-channel fets in parallel, to drive the diode capacitor network, will become clear in due course. Both types of fet have an R_{on} of 2.5 ohms. The measured performance of the converter is:

voltage in = 8.5V, current in = 230mA
voltage out = 41.8V, current out = 37.2mA
power in = 1.96W, power out = 1.55W
The efficiency at full is load = 79%

In considering the losses in this converter, it is convenient to refer them to the output voltage. That is, to assert that a completely efficient sextupler supplied with 8.5 volts ought to make an output voltage of 51, then to enquire why this one only makes 41.8.

Charge transfer losses. Charge transfer losses are probably quicker to measure than to calculate. One builds the converter in lash-up form, noting the on-load output voltage with the capacitors wired in that one expects to use. One then increases all the capacitors by some factor m, which might conveniently be 2, and notes the output again; it should be a little larger than before. Increase all the capacitors again, m=4, say, then m=8. Note the further small increases in output voltage, V_o. If one then plots V_o against (1/m), the points should lie on a straight line. The value of V_o for which this line crosses the "y" axis gives the output voltage the converter would have if the capacitors were infinitely large, and there were no charge transfer losses. The difference between this voltage and the voltage one actually gets with the capacitors one proposes to use is the voltage drop due to charge-transfer energy losses for the design. For the circuit discussed here, it comes to 3.5 volts.

Ohmic losses. These result from the appreciable R_{on} of the mos transistors. The consequent loss in output voltage is given by

$$2(n-1).I_o.(R_{on,\ p\ channel} + R_{on,\ n\ channel})$$
$$= 2\times5\times37.2\times10^{-3}\times(2.5\Omega+2.5\Omega)$$
$$= 1.86\ \text{volts}.$$

Voltage drop across Schottky diodes. There are ten of them. Assuming a loss of 0.35 volts across each, the total drop is 3.5 volts.

The total of output volts lost is therefore 8.9. Subtracting this from the ideal output voltage of 51, we see that the expected output voltage is 42.1, in tolerable agreement with the observed figure of 41.8.

Oscillator current. This is a loss which does not reduce the output voltage. It is a necessary evil, increasing slightly the current drawn at the input. The oscillator draws 4mA, so the expected input current is six times the output current plus 4 milliamps. That comes to 227mA, again in reasonable agreement with the measured value of 230mA.

THE MOSMARX CONVERTER

Figure 5 shows a practical d.c.-d.c. sextupler in the Marx configuration, in which mos transistors replace the spark gaps and half the resistors; the remaining resistors are replaced by Schottky diodes. This circuit is also arranged as a quintupler standing on its supply rail. When the oscillator output is high, n-channel fets Tr_6 to Tr_{10} turn on, allowing charge to enter their respective capacitors via their respective diodes. When the oscillator output goes low, Tr_{6-10} turn off again and p-channel fet Tr_1 turns on, connecting the bottom plate of C_1 to the supply rail and cutting off D_1. The source of Tr_2 is now at approximately $+2V_i$ while its gate is at V_i; therefore Tr_2 turns on, taking the bottom plate of C_2 to $+2V_i$ and cutting off D_2. In like manner, $Tr_{3,4,5}$ turn on in quick succession, putting the top plate of C_5 at approximately $6V_i$, whereupon the power supply and C_1-C_5 supply charge to the reservoir capacitor via D_6. The process is terminated by the oscillator output going low again. Tr_1 turns off and Tr_{2-5} follow in succession. The turn-on of the n-channel transistors is delayed slightly to allow the turn-off of the p-channel devices to complete; the simple delay network, comprising one resistor and one small diode, greatly reduces the no-load input current.

The converter will work with any input voltage between 6V and 10V. Below 6V there is insufficient voltage to switch the fets properly; above 10V, there is risk of destroying D_5, which is a 60 volt device. Used as intended, its measured performance is

V_i=8.5V	I_i=250mA.
V_o=46.2V	I_o=41.1mA.
hence P_i=2.13 watts	P_o=1.9 watts

Efficiency at full load: 89.4%

Charge transfer losses. The measured loss in output attributable to transferring charge is 1.5 volts.

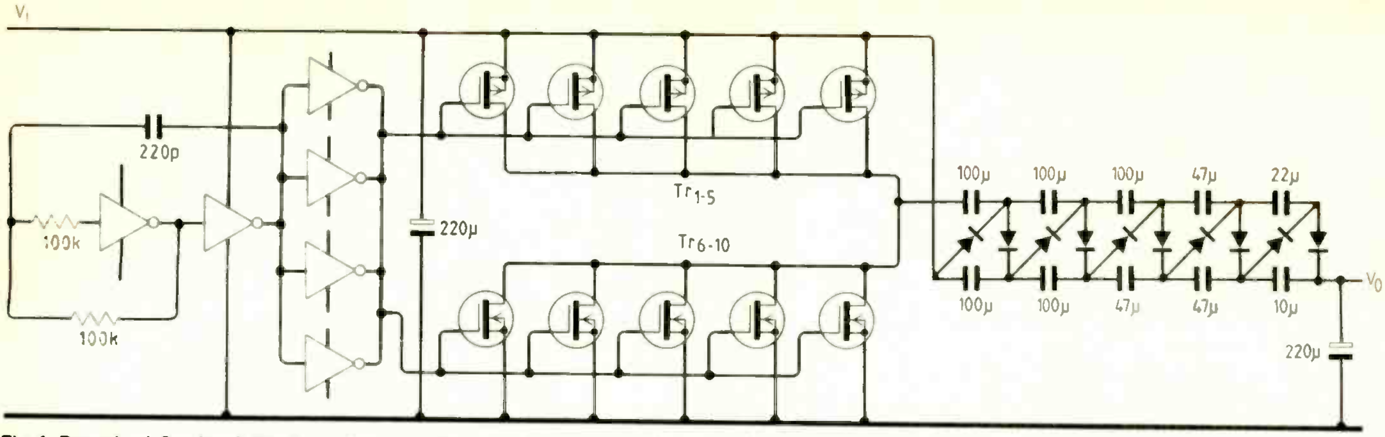


Fig.4. Practical Cockroft-Walton sextupler. The hex inverter is a 4049. P-channel fets 1-5 are Siliconix VP 0030 M. The n-channel fets are Ferranti ZVN 2106 A. The diodes are International Rectifier 11 DQ 06.

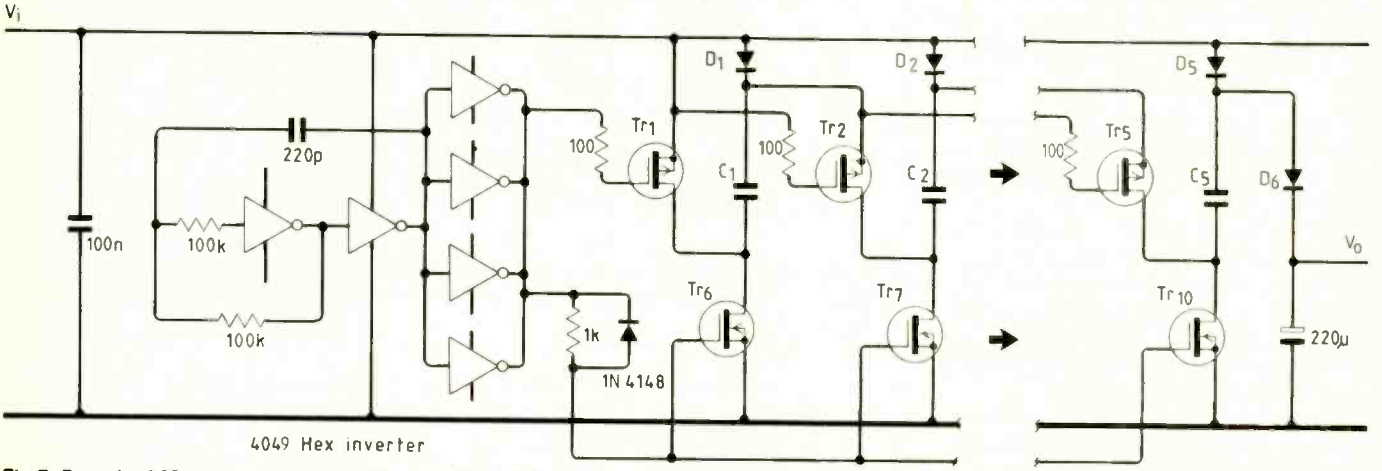


Fig.5. Practical Mosmarx sextupler. D_{1-6} are IR 11 DQ 06. C_{1-5} are 22µF. P-fets 1-5 are Silicon VP 0030 M. N-fets 1-5 are Ferranti ZVN 2106 A.

Ohmic losses. The expression for ohmic losses in this circuit is

$$2(n-1).I_o.(R_{on.\ p\ channel} + R_{on.\ n\ channel})$$

and is the same as that for the Cockroft-Walton circuit. It was to exploit this identity that the Cockroft-Walton converter was built with batteries of 5 parallelled fets of each type, to make it easier to compare the protagonists. In practice, the numerical value is not quite the same, because the Mosmarx gives more I_o into the same load. It is 2.06 volts.

Voltage drop across Schottky diodes. There are six of them. At 0.35 volts each, the total drop is 2.1 volts.

The total of output volts lost is therefore 5.7V. Subtracting this from the ideal output voltage of 51V, we see that the expected output voltage is 45.3V, a little less than my model actually gave.

Oscillator current. 4mA as before. The expected input current is six times 41.1mA + 4mA, or 251mA, in excellent agreement with the observed figure.

The Mosmarx converter is clearly the more efficient, and the analysis confirms what one would guess from looking at the circuit diagrams, that it is more efficient because there are fewer diodes and fewer charge transfer operations. Small gains in the efficiency of both converters are achievable by various methods, all but one of which involve some cost. One may choose fets with lower R_{on}, which could result in a converter with greater overall size.

To increase the value of the capacitors would, again, mean larger size. The Cockroft-Walton version is already overburdened with capacitors, needing (neglecting reservoirs) $n-(\frac{1}{2})$ times as much capacitor as the Marx for the same ripple.

Increasing the frequency will certainly raise the output voltage slightly, but one must bear in mind that the oscillator current is proportional to frequency, so there will be a corresponding rise in input current. The total effect of increasing the frequency is therefore liable to be disappointing, particularly when the converter is lightly loaded; in the latter case, the efficiency may actually decline.

None of these strategems can raise the efficiency of either converter beyond a certain point, because the effect of the diode drops imposes a fundamental limitation. The only way to gain any further improvements is to raise the input voltage (and therefore all other voltages) so that the effect of diode drops is proportionately less. In our application, unfortunately, this strategem was ruled out.

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BOOKS

An introduction to satellite television by F.A. Wilson. Bernard Babani, £5.95.
A good deal of this book is taken up with material not strictly relevant to the subject, as if the author wants to tell us all he knows rather than to stick rigidly to his task. Much of the first half of his text is taken up in describing the SI units of measurement, the atom, the nature of radio waves, television basics and even the principles of rocketry. Mysteriously, Ariane and Arianespace are mis-spelled every time they crop up. Despite an approachable style pitched at the absolute beginner, there is quite a bit of maths. A final chapter outlines the technique of setting up a receiving terminal. Equipment is described in general terms, with no mention of brand-names or programme services. Among the appendices are tables, formulae and a glossary. The book's scientific content might recommend it as an appealing way of presenting some practical physics to sixth-formers. Soft covers, large format 193×263mm.

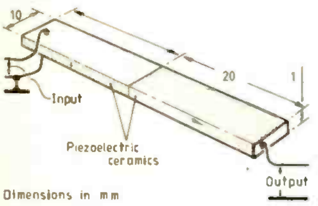
RESEARCH NOTES

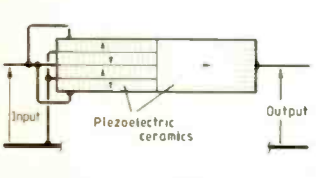
Ceramic transformers

Researchers at the Laboratoire d'acoustoelectricité of the Université Pierre et Marie Curie in Paris report some interesting experiments with piezoelectric transformers (*Electronics Letters* Vol. 24 no 7). The idea of using piezoelectric materials to produce an electromechanical analogue of a transformer is itself about 30 years old, but despite numerous patents having been issued, very few practical devices have emerged.

The theory is essentially very simple: if two piezoelectric resonators are bonded together, then an input voltage to one of them causes mechanical movements which in turn induce a voltage in the second resonator.

What the French group have done is to build ceramic transformers which, by ingenious design, are able to step up a small input voltage by at least 1000 times. The basic structure is as shown below:





The vital part of the construction is the orientation of polarization. In the case of the input plate this is across the thickness (as shown by the arrows) while in the output plate polarization is longitudinal. With this layout the transformation ratio is approximately equal to the ratio of inter-electrode distances, i.e. 200.

As it stands however this basic design is not very practical, the transformation ratio becoming drastically reduced as the output plate is loaded. By analysing the equivalent electrical circuit, the French researchers have been able to apply their resulting theory to developing an improved transformer which is much less sensitive to capacitive loading. This they've achieved by paralleling a number of identical input resonators and carefully bonding them all together to the output element (lower diagram).

This second device, when fed with an input voltage of 5V at between 80 and 160kHz, is able to sustain a 2mm spark at its secondary terminals.

The team concludes that, whilst this represents a very creditable step-up ratio of at least 1000, even better results could be achieved using a monolithic substrate.

High-speed superconducting bearing

Cornell University engineers have developed a high-speed bearing that depends on the levitating effect of high-temperature superconducting materials. The bearing, which has achieved speeds of 66 000 revolutions per minute, could make possible the development of superior rotors for gyroscopes, servo-motors and computer disc drives, according to Professor Francis Moon, who heads the team.

High-speed magnetic bearings now in use can achieve speeds of more than 100 000 rev/min in a vacuum, but require complex feedback circuits to maintain stability. However, the superconducting bearing will be able to achieve speeds of up to 300 000 rev/min and perhaps even one million rev/min in a vacuum because the levitating effect of the superconductor is self-stabilizing, needing no feedback control. Such higher speeds would permit the use in gyroscopes of smaller rotors with lower friction and fewer wear and heating problems.

The new device consists of a bearing made of an yttrium-barium-copper oxide superconducting ceramic cooled to liquid nitrogen temperatures. This bearing will levitate and propel a rotor containing rare-earth permanent magnets and is not affected by the high rotation speeds.

This levitation phenomenon, in which superconductors repel magnetic fields, is known as the Meissner effect. Moon and his colleagues have measured the magnetic forces generated by the new superconducting materials to a high degree of accuracy and have designed the system so that the Meissner effect provides extremely stable levitation forces between the bearing and the rotor.

They are now experimenting with differently-shaped bearings and suspension designs to enhance the levitating force and achieve even higher speeds.

Superconductor recipe book

Researchers at the Carnegie Institution of Washington's Geophysical Laboratory believe that they can now predict which materials will behave as high temperature superconductors. At a meeting of the American Physical Society Dr Robert Hazen challenged other teams to act on his predictions and end the cookbook mentality that has hitherto pervaded superconductivity research. In fact with due deference to those in the catering profession, he believes that the search for ever-higher temperature superconductors is more like cooking aimlessly *without* a recipe.

That recipe may now be forthcoming if Dr Hazen and his colleagues are right. They've been analysing a whole range of currently available materials, all of which are ceramics based on layers of copper atoms, oxygen atoms and a variety of different metal atoms. The best materials also contain thallium, calcium or barium.

In the course of analysis, one general conclusion seemed to emerge: the more layers of copper atoms there are in the lattice structure, the higher the temperature at which superconductivity occurs. On this basis Hazen predicts that if materials are synthesized with more than the three layers of copper atoms found in today's best materials, then the goal of room-temperature superconductivity might become that much closer. He believes that four- or five-layered materials are perfectly possible and is offering a case of beer to the first laboratory to succeed.

String pulling in space

String, as an engineering material, has never had a particularly good press. Even when wet its conductivity is not usually considered ideal even for telephone lines. But the ultimate insult, that of being 'tied together with string' may soon have to be revised in the light of a theory put forward by cosmologists at the Los Alamos National Laboratory. At its simplest this theory proposes that 'cosmic strings' – infinitesimally thin but hugely massive loops of energy – are responsible for the strange movements of some of the galaxies.

According to Y. Hoffman and W. Zurek (*Nature* vol.333 no.6168) the galaxies are being pulled by the gravitational attraction of loops of cosmic string that were left over as remnants of the Big Bang, now thought to have marked the beginning of the Universe.

Cosmic string – if it exists – has the weirdest of properties. More than 10^{12} times thinner than the diameter of an atomic nucleus, it is nevertheless incredibly massive. One metre of it could have a mass of 10^{12} tonnes. Or, expressed another way, a piece 10^{4} light-years in length would weigh in at something like the total mass of our Galaxy.

But mind-boggling though this one-dimensional material is, its bizarre properties don't end there. According to the most recent theories, the early stages in the creation of the Universe must have witnessed what amount to huge tangles of cosmic string. But because the theories don't allow for loose ends, the pieces of 'string' must have existed either as endless loops or as lengths spanning the whole Universe – conceptually not much different.

Much of this cosmic string may have ended up losing energy and turning into black holes. The remainder could have exerted so much gravitational energy that it acted as 'seeds' around which galaxies formed. Or, according to other theories, the loops of cosmic string may act as superconductors, carrying in excess of 10^{20} amperes. Such currents would have the opposite effect of

RESEARCH NOTES

gravitational attraction and repel any nearby material.

This 'push' and 'pull' may explain many of the irregularities that are observed in both the velocity and distribution of galaxies. It may also, if Hoffman and Zurek are right, explain a finding last year by a group of Cambridge astronomers that some of the closest galaxies are all heading towards an apparently empty area of the sky.

Obviously this could be a mere random irregularity in the Universe, though the odds against it are huge. A loop of cosmic string is a neat alternative, but that stretches credulity in different ways. So what are ordinary mortals to believe?

The answer may come from practical attempts to find cosmic string. Although it would be much too thin to observe directly, it would bend light rays by its immense gravitational force. So a search in likely areas of the sky could well come up with a long row of double images of more distant galaxies.

If cosmic string is ever found it will undoubtedly provide a tremendous boost for theoretical cosmology. But for those of us accustomed to derogating the properties of string it may be something of a shock to discover that our Universe is organized much as W. Heath Robinson might have conceived it!

Potential progress

Two recent developments, one technical and the other political, may in future make it easier to define and measure our everyday unit of potential.

Taking these in reverse order, it may be of interest to know that there are four different 'volts' around the world: an American one, a Russian one, a French one and a 'rest of the world' volt. It's not that there's any disagreement over definitions; merely that our practical standards are based on slightly different experimental values of the Josephson constant.

By international agreement, the volt is now defined in terms of the output of a superconducting Josephson junction when exposed to microwave radiation of a precisely defined frequency. So, given that frequency can easily be measured to one part in 10^{12}, the only practical limit on measuring potential is the value of the Josephson constant. Recent experiments have shown that some of the values on which present standards are based are in error by as much as eight parts in 10^6. International agreement is therefore being sought to specify a new worldwide volt that will be as acceptable in Moscow as it is in Washington, Paris or London.

One (electro-) motivating force is the parallel development of hardware capable of many times this order of accuracy. Physicists at Britain's National Physical Laboratory are, for example, able to calibrate secondary voltage sources accurately to five parts in 10^8 with relative ease. Such secondary sources are usually the 1.018V Weston cells beloved of O-level physics textbooks.

Until relatively recently, however, the limiting factor in making accurate comparisons has been the considerable disparity between the p.d. of a Weston cell and that of a Josephson junction. The latter is of the order of 2.5mV when driven with a 10GHz microwave source.

One obvious solution would be to fabricate a large number of series-connected Josephson junctions, though the lithographic problems and those of ensuring uniform microwave irradiation have made it an extremely difficult task in practice. Until a few months ago a chip with 2000 junctions was considered a major achievement.

Now comes news of a 19 000-junction chip fabricated by the US National Bureau of Standards in Boulder, Colorado. This chip, in which niobium/lead alloy junctions are integrated into a microwave stripline, operates in a dewar at liquid helium temperatures. Total microwave input is around 100mW, though each junction receives only fractions of a microwatt.

By varying the microwave frequency, the NBS team, led by Richard Krautz, are able to vary the terminal p.d. from 0.1V to 14V. In this way they can precisely match the p.d. of the source being calibrated, hence obviating another possible inaccuracy. Overall calibration accuracy is claimed to be of the order of three parts in 10^{10}.

Now the NBS plans to make available the basic chip for around $6000 or a complete voltage standard for $100 000. Demand is said to be considerable.

Molecular wire

Attemps to shrink integrated circuits and even the computers they comprise tend to be limited not by the active elements but by the pieces of 'wire' that form the links. Dismantle any i.c. and it's instantly obvious that the lead out wires are the largest bits. Even the inter-element connections on the chip itself can be such as to slow down the inherent speed capability. So any attempt to produce faster or smaller transistors will only ultimately succeed if the wiring can be improved as well.

In the bizarre world of nanotechnology, where physicists are envisaging circuit elements the size of a molecule that will process single electrons, wire is an acute embarrassment. It's therefore intriguing to learn (*Journal of the Chemical Society* 1988, p84) that a team at the University of Minnesota has created linear molecules that could act as interconnections between molecular electronic components. These linear molecules, which have been synthesized in lengths up to 7.5 nanometres, are based on chemical building blocks called imides and polyacenequinones. When chemically reduced they become effective conductors of electricity. They are also soluble in a variety of ordinary organic solvents, which allows them to be purified easily.

Just how they will fit into the rapidly developing molecular electronics scene is of course the key question. But in a world where components are likely to be synthesized rather than etched, the idea of self-growing wire is attractive. So also is something at least three orders of magnitude smaller than the finest wire that can be produced by existing lithography.

Assuming that such molecular wire can be successfully integrated with the other circuit elements currently being envisaged, the notion of molecular computers may not be as fantastic as we often imagine. And if a reduction in size by three orders of magnitude can be carried through an entire system, then a pocket-sized supercomputer is a perfectly reasonable forecast.

Go home Columbus!

Those of us who bemoan the widespread public ignorance of engineering may gain some solace from a study undertaken recently by Alan Lightman and Philip Sadler and published by the U.S. National Science Teachers' Association. Lightman, a physicist at the Smithsonian Astrophysical Observatory and Sadler, a Harvard lecturer, have discovered that over 95% of second grade (primary) schoolchildren in the USA are convinced flat-earthers.

The two researchers discovered during a survey of 65 school classes that most six or seven-year-olds draw the Earth either as a giant pancake or as a round ball with a flat portion inside on which people live.

Whilst this latter picture may demonstrate Man's unlimited ingenuity to fiddle the evidence, Lightman and Sadler were curious to know why, in spite of Columbus, Gagarin *et al.*, the overwhelming majority of young children still think two-dimensionally, at least where *terra firma* is concerned. The answer appears to be that children (only children?) tend to construct naive theories based on common-sense experience – in this case that the school playground is flat. Therefore by extrapolation...

Lightman and Sadler (who would clearly have found Einstein a kindred spirit) believe firmly that one important role of education is to convince people that things aren't always what they seem to be. Kenneth Baker please note.

Research Notes is written by John Wilson of the BBC External Services science unit at Bush House, London.

FEEDBACK

Relational analysis

'Relational Analysis' – developed by J.A. Corbyn in your December 1987 issue – is to me very interesting but I find the traditional approach easier. It may be that I am lazy and resistant to ideas which depart from those we have grown used to over the years; but for a given problem it is easy to look up the tables that give the MLT dimensions of the quantities involved and then carry out the conventional calculation. Furthermore I find that the problems resulting from the non-dimensional groups of quantities (which express the fact that particular physical laws are not important or their effects can be dealt with by keeping the physical parameters in a certain relation to one another in the problem concerned) can normally be avoided by a careful choice of variables.

The point made by J.A. Corbyn that the MLT system and related units are an 'artificial' basis for physics and dimensional analysis is not taken up because such deviations from 'received truth' are difficult to teach or to operate in practice. Although the computerisation suggested makes the new method easier to introduce, the old method too is, surely, equally amenable to computer solution, is it not?

I would, however, recognise that the paper does provide new insight into units and dimensions and is a useful reminder that in any given problem a greater *physical* understanding of what is going on may well be achieved by dispensing with MLT as 'fundamentals' and using whatever quantities are suggested by the problem.

Richard Collins,
London, N4.

The observer in science

I would like to thank B.E.P. Clement and C.F. Coleman (June letters) for bringing out some points which were not dealt with explicitly in my article on the observer in science (April 1988), namely, the brain's proclivity to make and detect patterns; the limits for perceptual resolution at low stimulus intensities; and that the observer sometimes operates through the medium of quite complicated apparatus.

Regarding modern physics experiments, Mr Coleman is quite right to emphasize that interaction takes place "between the equipment used for the measurements and the system observed." But he seems to dispute the fact that there can be an interaction between the human observer and the system observed. To amplify my brief and cursory remarks on this interdependence perhaps I could quote from a contribution by the American physicist J.A. Wheeler (University of Texas) to a book The Physicist's Conception of Nature (Reidel, Dordrecht, Netherlands, 1973). Discussing how the quantum principle has affected our understanding of nature, he writes:

"Even to observe so miniscule an object as an electron [the experimental physicist]... must reach in. He must install his chosen measuring equipment. It is up to him to decide whether he shall measure position or momentum. To install the equipment to measure the one prevents and excludes his installing the equipment to measure the other. Moreover, the measurement changes the state of electron. The universe will never afterwards be the same. To describe what has happened, one has to cross out that old word 'observer' and put in its place the new word 'participator'."

T.E. Ivall,
Staines,
Middlesex.

Defence mechanisms

With reference to your June editorial "Defence mechanisms". I am not a pacifist, but the moral implications of sitting behind the argument you propose: 'If I did not do this work, somebody else certainly would. So it really doesn't make any difference whether I, personally, am involved: the work would get done in any case', are clearly outrageous. This may be easily seen if we replace 'work' by some specific action 'If I did not commit murder, somebody else certainly would...'. Whilst this is a truism, as an argument it cannot begin to justify the action. If we are to maintain any moral integrity in whatever we do then we must be able to justify all our actions on their own merits and not on what other people might or might not do. And if 'murder', who shall we begin with?!

C.P. Oates,
Newcastle-upon-Tyne.

If Mr Oates would care to re-read the leader in question, he will find that he has misunderstood it. The argument proposed was the exact opposite of that he suggests. – Ed.

Moving-coil head amplifier

I would like to express thanks to Douglas Self for injecting a little bit of sense into the world of audio electronics (December, 1987). I would also like to express my dismay at seeing an experienced engineer like Graham Nalty spouting such utter nonsence.

Why is it that engineers, highly trained in the use of logic and experimentation, should resort to superstition, unsupported by experimental evidence, when discussing or designing hi-fi? Mr Self's approach, involving sensible and logical design techniques, and making high-specification components unnecessary, can be justified purely on the grounds of listening to equipment designed in this way (which is after all what hi-fi is for). If an amplifier really does benefit from the use of bulk foil resistors at £10 a pair, then I strongly recommend that you throw the design away and start again (who needs 4ppm K^{-1} in an amplifier anyway?). There is enough nonsense around concerning hi-fi design (gold-plated 13A mains connections apparently being a good idea, for instance) without engineers who really ought to know better joining in.

Duncan Kitchin,
Peterhouse,
Cambridge.

I read with some interest Mr Self's letter in *EWW* (June) which commented on my previous letter (April). The distortion mechanism to which I referred is 'dielectric absorption' and in simple terms is the absorption from an electrical signal into the dielectric and the release of that energy over a period of time after the original signal has passed. Methods of measurement of dielectric absorption have been published in *The Audio Amateur* and *HiFi News*.

Mr Self states that anyone who spends £10 on a resistor is a fool. I suppose he reaches this conclusion from the famous saying "a fool and his money are soon parted". Certainly many of Audiokits customers have been prepared to part with £10 or more on a pair of bulk-foil resistors. A number of these people have later commented on the improvement in sound quality they have enjoyed as a result. I could give several valid reasons why bulk-foil resistors are superior but this is fully covered in an article in *Practical Electronics*[1].

I have written many articles which cover the distortions in audio circuitry with applicable technical backup and these are listed in the references [1-7] below.

I have indeed made measurements on capacitors in real-life circuit situations with the best instrumentation of all – my own ears. Whilst the human ear is not as constant as a metre of platinum in its measurement, it is the final arbiter by which any judgement can be made. Any measurements made using scientific equipment of higher consistency are only valid provided they reinforce the judgements made with our own ears.

If any readers of EWW have the slightest doubt that passive-component quality is a very important factor in audio design, I recommend them to read the June issue of *HiFi Choice*. Audiokits submitted to review two pre/power amps with identical electronic circuitry and specification: differing only in cables, resistors, capacitors and a few semiconductors. These were tested both in the laboratory and in a hi-fi system for sound quality.

Finally, I was of the belief that it was man's determination to explore that got us to the moon. Scientific achievement only provided the means. Similarly it is my determination to improve the standard of audio reproduction that has led me in the direction of better passive components.

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Graham Nalty,
Audiokits,
Borrowash,
Derby.

The Catt Anomaly

I have come to regret the description "The Catt Anomaly" (*EWW* September, 1987), which is a question about the minutiae of classical electromagnetic theory. IEE officials are refusing to comment on the question on the grounds that they are being asked to pass judgement on some revolutionary theory of Ivor Catt's. What we should rename "The TEM Charge Question" has nothing whatever to do with any new or revolutionary theory.

My reply in January, 1988 to Alex Wilding did not relate directly to the Catt Anomaly. I pointed out that he had a forward E field and so was not even discussing a TEM wave, much less the Catt Anomaly.

The TEM Charge Question asks where the new charge comes from, to terminate the lines of electric flux which now exist between the top and bottom conductor. Wilding's last paragraph, January 1988, contradicts Gauss's Law (Electricity and Magnetism, by S.G. Starling, Longmans, 1924, p.126), which says that rearrangement alone will not provide the negative charge needed to terminate the electric flux lines. Similarly, when John Matthews, *EWW* March, 1988, says "This will happen if all the electrons in the surface move up a little bit,..." he contradicts Gauss's Law. A modernized version of Starling's statement of Gauss's Law is:

> The total electric flux across a closed surface is equal to the total amount of electric charge within the surface.

Describe a closed surface just outside the lower conductor. Since we are discussing a transverse electromagnetic wave, all electric flux is in the plane normal to the wires. The total electric flux entering this surface equals the total charge within the surface, however it might be rearranged. Rearrangement of charge in/on the wires is irrelevant to the TEM Charge Question.

In his February, 1988 letter, Wilding says:

> "....the speed of the [charge] can be far below .... the speed with which [the electric flux propagates]."

This seems to directly contradict Gauss's Law.

Wilding and Matthews are in good company when they (wrongly) think that rearrangement of charge within the conductor has a bearing on The TEM Charge Question. In his first (private) response to the question, Dr J. Brown, then Professor at Imperial College, thought that somehow, negative charge would find its way out from the inner recesses of the lower conductor to terminate the electric flux which appeared as the TEM step travelled by. Brown's published reply in *EWW* November, 1982, is on other lines.

In his January, 1988 letter, when R.J. Sharp writes, "... the effect is to concentrate...." the charge, he seems to contradict Gauss's Law, which of course is one of Maxwell's Equations, div $D = \rho$.

The TEM Charge Question is about the detail of classical electromagnetic theory. It was first asked in *WW* August 1981. It has nothing to do with any new or revolutionary theory. I have decided that if during the ensuing ten years, by August 1991, no generally approved answer to the question arises, then classical electromagnetism will have to relinquish its role as a credible theory. Until some coherent answer is delivered by accredited experts in e-m, classical electromagnetic theory is incomplete, lacking a feature which is essential in this age of digital electronics. Casual waffle like that from text books writers Robinson and Brown (*WW*, October 1982) is insufficient. Digital electronic designers are entitled to a clear, reasoned statement as to where the charge comes from which switches their high-speed gates.

As to the early part of Sharp's letter (*EWW*, January 1988), I present a totally different view on the performance of a capacitor. See for instance *WW* December 1978:

> "no mechanism has ever been proposed for an internal series inductance in a capacitor."

Such internal series inductance does not exist, and the so-called self-resonant frequency of a capacitor is a myth.

Turning to the Joules Watt letter, February 1988, T.S. Kuhn is actually discussing the conservatism of the scientific community in the part of his book that J.W. quotes from. It is descriptive and not prescriptive, but by quoting very short segments, J.W. makes it appear otherwise. I am very willing to agree that Theory C (*WW* December 1980) has been blocked by the conservatism of the scientific community. Nearly ten years after its publication, there still does not exist one written comment on it by an accredited academic.

Ivor Catt,
St Albans,
Hertfordshire.

Gyroscopes

Alex Jones in the May letters questions my interpretation of his dramatic gyroscope demonstrations. To lift a big, stationary gyroscope by one end of its shaft while keeping the shaft horizontal one must use both hands to exert a large torque, pressing hard downwards with the hand at the end of the shaft, and pulling upwards even harder with the hand closer to the rotor. However when one attempts to lift a spinning gyroscope by one end it begins to precess, the torque virtually disappears, and only its weight is left to be supported. I have used kitchen scales with a sliding balance weight to weigh a toy gyroscope, first at rest together with its tower, and secondly spinning and precessing with one end supported on the tower. There was no visible change in weight, and any actual change must have been less than 20%. If any of your readers wishes to try for himself he should check that his gyroscope rotor is reasonably balanced. Until I filed its rim my gyroscope vibrated too much to stay reliably on its tower.

Standard kinetic theory shows that the motion of the centre of gravity of a rapidly spinning gyroscope is accounted for completely by the sum of external forces acting on it. However if there is in addition a residual torque about any axis perpendicular to the shaft of the gyroscope and it is free to do so it will precess about the direction perpendicular both to the shaft and to the torque axis. Thus if a gyroscope is supported at one end it precesses about the vertical through the point of support. However if the support produces any thrust horizontally and at right angles to the axis of the gyroscope it will tilt either progressively upwards or progressively downwards. That I believe accounts for the phenomenon of the upwards tilting gyroscope Alex Jones described in the January 1987 letters.

C.F. Coleman,
Grove,
Oxfordshire.

Damped circuits

B&J Sound, of Kirkby Lane, Tattershall, Lincoln LN4 4PD, have sustained extensive flood damage to their premises, which has ruined hundreds of their archive publications. Among these were copies of this journal for 1981 and 1982. If any reader has copies for sale, B&J would be glad to hear from them. The telephone number is 0526 42869.

Philip Smith's chart

J.W. asserts that the Smith chart is alive and well and living on the front of all those exotic network analysers.

JOULES WATT

My excursion into transmission lines[1] from the point of view of guided electromagnetic waves, inevitably caused a flurry of comments about impedance charts.

"Are they still used?" I was asked. Someone else mentioned he used charts often, but enquired how they worked. Students wondered why they had to study them, when "computers and automatic test equipment solve all the problems now, right?". The answer is, of course, not always. To illustrate, I dug out an overlay transparency that fits the front of an expensive network analyser screen and, in passing, booted up a personal computer which ran an r.f. circuit-analyser program. In both cases, a Smith chart[2] appeared on the screen – either as the overlay or directly on the v.d.u.

In other words, although automatic equipment often computes solutions, we get them presented on a Smith chart. Therefore, to interpret the picture, r.f. engineers need a thorough grasp of the mathematical principles behind it.

I suppose a short way of saying all this is to point out that the mathematical modelling of transmission lines must yield the same equations that plot the chart. Because the analysis of other circuit elements turns up similar equations, we can plot their characteristics on the chart as well. From this view, as you look further into the graphical tradition handed down to us by electronic engineers, the ramifications become wider and more subtle. Therefore you can present on a Smith chart much more than transmission-line problems, although I carry through that classical approach here. Lumped-impedance matching circuits, gain and stability circles for amplifiers, impedance-to-admittance conversion, the presentation of S (scattering) parameters and others all become clear on the overlapping co-ordinates of the chart.

Currently, however, as the earlier geometrical tradition in our maths teaching declines, visual imagery becomes neglected, to the detriment of learning. Shame on those who fail to exhort the next generation to see this beauty.

A LITTLE FURTHER ALONG TRANSMISSION LINES

Electromagnetic waves on r.f. lines travel both ways. We usually work in terms of voltage and current waves, so that the forward voltage wave, which has a complex amplitude V^+, arises from the transmitter supplying r.f. energy. Waves travelling the other way usually result from reflection at a mismatch and we denote them by the complex amplitude V^-. The sum $V^+ + V^-$ gives

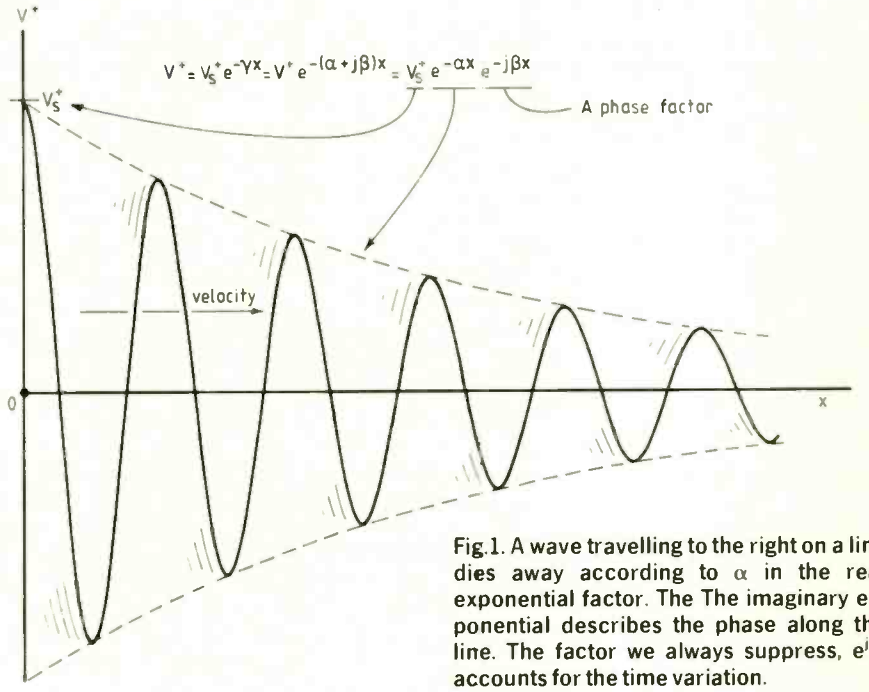


Fig.1. A wave travelling to the right on a line dies away according to α in the real exponential factor. The The imaginary exponential describes the phase along the line. The factor we always suppress, $e^{j\omega t}$ accounts for the time variation.

the total voltage at any point. A closer look shows standing waves now present; the voltage standing wave ratio (v.s.w.r.) is a significant talking point in line-matching problems. If you want to calculate the v.s.w.r., also defined as S, then take the voltage maximum, V_{max}, measured at appropriate points along the line and divide by V_{min}, measured at intermediate points. V_{max} and V_{min} turn out to be the sum and difference of the forward and reflected wave amplitudes respectively,

$$\therefore\ V_{max} = |V^+| + |V^-| \text{ and } V_{min} = |V^+| - |V^-|.$$

This means you can write

$$S = \frac{V_{max}}{V_{min}} = \frac{|V^+| + |V^-|}{|V^+| - |V^-|}$$

You probably expect the characteristic impedance Z_0 to enter the scene any moment now – and it does, to give the current waves,

$$I^+ = \frac{V^+}{Z_0} \text{ and } I^- = -\frac{V^-}{Z_0},$$

giving the total current

$$I = I^+ + I^- = \frac{V^+ - V^-}{Z_0}$$

In common with complex number theory, all these voltages and currents possess real and imaginary parts.

The *propagation constant* also figures prominently and Fig.1 shows that by using it, we can write down the voltages (or using Z_0, the currents) anywhere along the line including the termination – all in terms of the sending end values.

$$V^+ = V_s^+ e^{-\gamma x}$$
$$V^- = V_s^- e^{\gamma x}$$

and at the load, distance l away,

$$V_L^+ = V_s^+ e^{-\gamma l}$$
$$V_L^- = V_s^- e^{\gamma l}$$

You will find one other number important for further discussion, namely, the *voltage reflection coefficient* whose symbol nearly everyone agrees to take as ρ. The definition of ρ is,

$$\frac{\text{reflected wave complex amplitude}}{\text{forward wave complex amplitude}}$$

at any point.

This yields immediately at the sending end,

$$\rho_s = \frac{V_s^-}{V_s^+}$$

at the load,

$$\rho_L = \frac{V_L^-}{V_L^+}$$

and generally,

$$\rho = \frac{V^-}{V^+}.$$

Because the voltages are complex, ρ is

complex too. Therefore it has a phase and amplitude like any other complex number.

$$\therefore \qquad \rho = |\rho|e^{j\varphi} \text{ (see Fig.2).}$$

All the ρs relate to one another, because all the voltages do

$$\rho = \frac{V^-}{V^+} = \frac{V_s^-\ e^{\gamma x}}{V_s^+\ e^{-\gamma x}} = \rho_s e^{2\gamma x}$$

In a similar way we find the load reflection coefficient

$$\rho_L = \frac{V_s^-\ e^{\gamma l}}{V_s^+\ e^{-\gamma l}} = \rho_s e^{2\gamma l}$$

You can ring some changes on all these at will. For example, by dividing ρ_L by ρ, this turns up

$$\frac{\rho_L}{\rho} = \frac{\rho_s}{\rho_L} e^{2(\gamma l - x)}$$

$$\therefore \qquad \rho = \rho_L e^{-2\gamma d}$$

where $d = l - x$ is the distance measured *back* along the line from the termination in Fig.3.

The total voltages anywhere also relate easily through the reflection coefficient

$$V_s = V_s^+\left(1 + \frac{V_s^-}{V_s^+}\right)$$

$$= V_s^+\,(1 + \rho_s).$$

Also $\qquad V = V^+\,(1 + \rho)$

and $\qquad V_L = V_L^+\,(1 + \rho_L)$

So do the currents

$$I = \frac{V^+}{Z_0}(1 - \rho),$$

and so on.

I have just shown that all the wave amplitudes simply require you to know the forward wave voltages, given the reflection coefficients.

But now comes the *pièce de résistance*. We obtain all the *impedances* at any point along the line as well. You have to understand the definition first. The impedance z at any point appears from Ohm's Law as the quotient of the total voltage to the total current at that point.

$$\frac{V}{I} = Z, \frac{V_s}{I_s} = Z_s \text{ and } \frac{V_L}{I_L} = Z_L$$

So straightaway,

$$Z_s = \frac{V_s}{I_s} = \frac{V_s^+(1+\rho_s)}{\frac{V_s^+}{Z_0}(1-\rho_s)} = Z_0\left(\frac{1+\rho_s}{1-\rho_s}\right)$$

In a similar way, at the other positions,

$$Z_L = Z_0\frac{1+\rho_L}{1+\rho_L} \text{ and } Z = Z_0\ \frac{1+\rho}{1-\rho}$$

By transposing, you can get expressions for the ρs, for example,

$$\rho_L = \frac{Z_L - Z_0}{Z_L + Z_0}$$

Authors seem to be fond of writing everything in terms of the *load* reflection coefficient, ρ_L, so that using $\rho = \rho_L e^{-2\gamma d}$ as an example, we can write the impedance z at

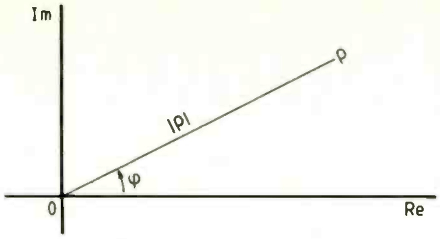


Fig.2. **ρ is here represented as a phasor in the complex plane. The axes correspond to those upon which the Smith chart centres (see later).**

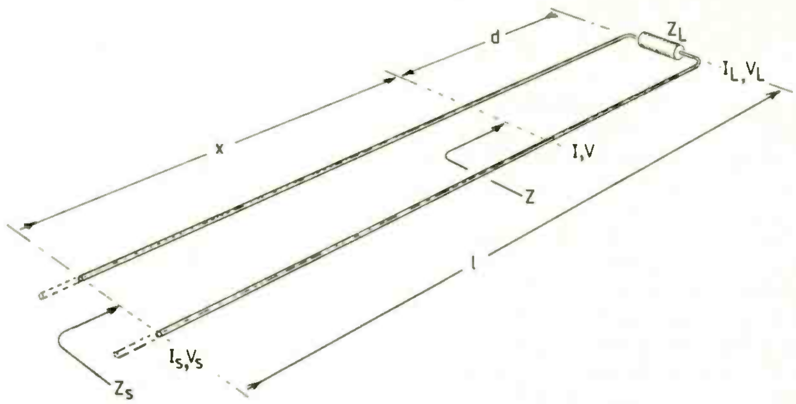


Fig.3. **As in all good geometry, you should keep track of your coordinates. The impedances are those seen "looking in" at the points shown.**

any point on a line at a distance d back from the load towards the transmitter as,

$$Z = Z_0\left(\frac{1+\rho_L e^{-2\gamma d}}{1-\rho_L e^{-2\gamma d}}\right)$$

You can see from the definition that ρ is dimensionless and because the reflected wave amplitude $|V^-|$ arising from a forward wave reflecting at a passive termination cannot exceed the incident amplitude $|V^+|$, then

$$|\rho| = \frac{|V^-|}{|V^+|} < 1$$

Now we are in a position to write the standing wave ratio S in terms of $|\rho|$.

$$S = \frac{|V^+| + |V^-|}{|V^+| - |V^-|} = \frac{1 + \frac{|V^-|}{|V^+|}}{1 - \frac{|V^-|}{|V^+|}} = \frac{1+|\rho|}{1-|\rho|}$$

ENTER THE COSH, SINH AND TANH

By substituting

$$\frac{Z_L - Z_0}{Z_L + Z_0}$$

for ρ_L in the above equation for Z we obtain

$$Z = Z_0\left(\frac{(Z_L+Z_0)e^{\gamma d} + (Z_L-Z_0)e^{-\gamma d}}{(Z_L+Z_0)e^{\gamma d} + (Z_L-Z_0)e^{-\gamma d}}\right).$$

Rearranging,

$$Z = Z_0\left(\frac{Z_0(e^{\gamma d} - e^{\gamma d}) + Z_L(e^{\gamma d} + e^{-\gamma d})}{Z_0(e^{\gamma d} + e^{\gamma d}) + Z_L(e^{\gamma d} - e^{-\gamma d})}\right).$$

You may be familiar with the hyperbolic functions,

$$\cosh x = \frac{e^x - e^{-x}}{2},\quad \sinh x = \frac{e^x + e^{-x}}{2},\quad \tanh x = \frac{\sinh x}{\cosh x}$$

If not, a quick look in ref. 3 should put you right. This means that you can write the equation for Z in terms of the hyperbolic functions, and it looks like,

$$Z = Z_0\frac{Z_0 \sinh\gamma d + Z_L \cosh\gamma d}{Z_0 \cosh\gamma d + Z_L \sinh\gamma d}'$$

or

$$Z = Z_0\frac{Z_0 \tanh\gamma d + Z_L}{Z_0 + Z_L \tanh\gamma d}$$

at any point a distance d back from the load.

The last discussion assumes that some general propagation constant γ describes the waves on the line. This complex γ has real and imaginary parts,

$$\gamma = \alpha + j\beta$$

where the attenuation constant α measures how rapidly the wave dies away because of losses. The phase constant β yields how quickly we go through cycles of phase-angle change while travelling along the line. You pass through 2π radians if your journey takes up one wavelength along the line.

LOSSLESS LINES

Radio frequency line made with low-loss materials such as coaxial cables with p.t.f.e. dielectric, possess very small α's. To a very good first approximation we call these lines *lossless*. In that case, $\gamma = j\beta$ and the sinh, cosh and tanh become transformed to the more familiar form of the sin, cos and tan, which means we can write down the impedance Z back along such lines in the simpler form,

$$Z = Z_0\frac{jZ_0 \tan\beta d + Z_L}{Z_0 + jZ_L \tan\beta d} \qquad (1)$$

You can do many interesting things with this equation. For example, short circuit the end of the line – in other words, put $Z_L = 0$, then,

$$Z = jZ_0 \tan \beta d$$

This shows that you obtain an *inductive reactance* varying as tan βd until at $d = \lambda/4$ $Z \rightarrow \infty$. This is the famous shorted quarter-wave stub behaviour, of course. Put $d = \lambda/4$ into (1) and you obtain the *quarter wave transformer*,

$$ZZ_L = Z_0$$

You can obtain many other results. For example, ask yourself what happens with an open circuit at the end, or with a lumped Z_0 placed on as a load.

All this shows that we have an equation that models and predicts all the behaviour of lines and stubs carrying sinusoidal waves, for which the impedance concept holds.

CHARTING A NEW COURSE

As you know, all impedances possess real (resistive) and imaginary (reactive) parts. If you study the graphical plot of this, you find yourself on the *complex plane*[4]. One particular transformation of this plane gives considerable new insight: the discussion in the box gives a brief outline of this *geometric inversion*, which, in our context, amounts to a transformation from impedance to admittance,

$$Y=\frac{1}{Z}$$

Before I look into this a little further, one tricky point that needs a brief word or two involves something called *normalization*. You will find a number of occasions on which a scale factor change simplifies everything. The important quantity in any problem – it could be the resonant frequency of a system, or, in the present context, probably the characteristic impedance Z_0 – is the one that takes over the job of acting as the unit. Using the characteristic impedance as an example, we divide everything by Z_0 so that all other impedances become multiples or fractions of it.

Doing this can be a little dangerous in that, as Z_0 divides everything, the units (ohms) disappear and you have to watch the dimensions. Some authors (including myself) use upper-case symbols for unnormalized quantities and lower-case letters for normalized ones. Thus, for a pure resistance on the end of a line,

$$r_L=\frac{R_L}{Z_0}$$

and so on. If you write equation (1) with a terminating resistance on the end in normalized form, it means you have divided by Z_0 and the result looks like

$$z=\frac{j\tan\beta d+r_L}{1+jr_L\tan\beta d}$$

This is a simpler version of the most general form,

$$z=\frac{a+by}{c+dy}$$

which in complex number theory has the grand title, the *bilinear transformation*. You could rearrange it into a suitable form for a transformation from the y to the z plane. Fortunately you can write the simpler, normalized equation (1) directly into the form

$$z=\frac{A}{y}+B$$

The A/y term transforms easily by means of the geometric inversion as discussed in the box. The B term is a shift along the axis.

Beady-eyed readers probably noticed that I slipped in a pure resistance r_L as a termination, instead of the more general z_L in the normalized equation (1). I intended this, since it means we can start and finish some plots on the complex z-plane along the real axis, not out at some hard-to-find point z. We do not lose any generality, because the plots go right round the circumference of circles in any case and therefore encompass every relevant impedance.

Add, then subtract $1/r_L$ to the right-hand side of the normalized equation (1),

$$z=\left(\frac{r_L+j\tan\beta d}{1+jr_L\tan\beta d}-\frac{1}{r_L}\right)+\frac{1}{r_L}$$

$$\therefore\quad z=\left(r_L-\frac{1}{r_L}\right)\left(\frac{1}{1+jr_L\tan\beta d}\right)+\frac{1}{r_L}=r+jx$$

which yields the precise form we require for the geometric transformation.

DRAWING THE CIRCLES

Step by step handling of each term and factor in the expression for z builds up an impedance chart. Start by inverting the plot of $1+jr_L\tan\beta d$ in Fig.4(a) to get the circle in Fig.4b. Then magnify this circle by the factor

$$\left(r_L-\frac{1}{r_L}\right),$$

thus arriving at Fig.4(c). Finally, shift the circle along the axis by the amount of the term $1/r_L$ to obtain the result in Fig.4(d).

Notice that a journey round the circle corresponds with a shift back along the transmission line through half a wavelength, because $\tan\beta d$ goes through one cycle as d changes by λ/2. From this you can see that voltage, current, phase and impedance conditions go through the whole cycle of possibilities, every half-wave shift back along an unmatched transmission line. A semicircular journey on the chart corresponds to a quarter-wave shift along the line and shows a reciprocal relationship. Where we start at high impedance, we end at low. High-voltage points become high-current points λ/4 away and so on. This confirms that quarter-wave sections of transmission line behave as transformers.

Every point on a given circle possesses the same r_L, so as you choose different r_L, a whole family of circles – the *constant resistance circles* – appear on the plot. The standing wave ratio S remains constant on any one of these circles. In fact, because S equals the normalized resistance r_L, you can read off S as the value of r_L at the intersection of the circles with the resistance axis. From this, many authors use the alternative name "the S circles". Figure 5 shows them.

The other circles. A move around a constant S circle takes you on a journey back along the line, or forward along it, if the move goes round the other way. Each point, therefore, represents a fixed position on the line. It looks as though we need another set of circles upon whose circumferences all the fixed points lie.

You can derive these circles in a similar way to the S circles. This time, add and subtract $1/\tan\beta d$ to the normalized equation (1)

$$\therefore z_{in}=\left(\frac{r_L+j\tan\beta d}{1+jr_L\tan\beta d}+\frac{j}{\tan\beta d}\right)-\frac{j}{\tan\beta d}$$

$$=\left(\tan\beta d+\frac{1}{\tan\beta d}\right)\left(\frac{1}{r_L\tan\beta d-j}\right)-\frac{j}{\tan\beta d}$$

$$=r_{in}+jx_{in}$$

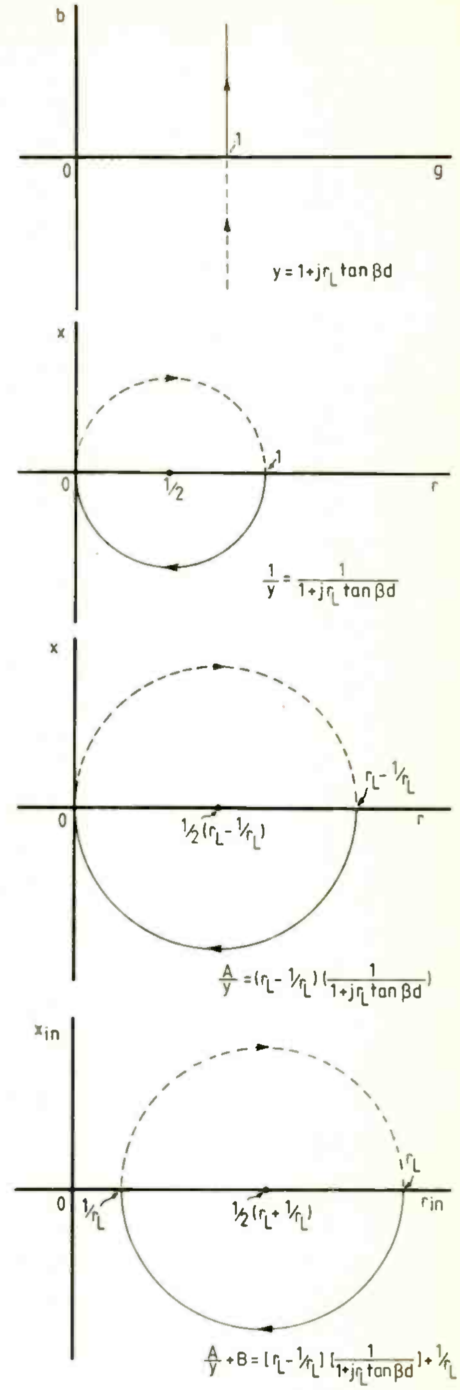


Fig.4. Here we have a series of steps building up one set of circles on the rectangular impedance chart as discussed in the text.

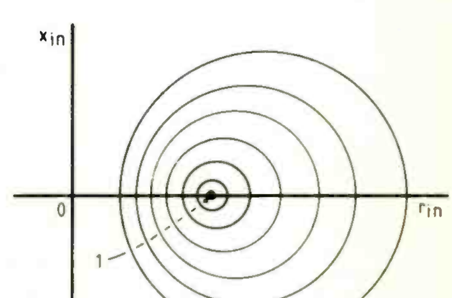


Fig.5. The result of the transforming operation shown in Fig.4, yields a set of circles all encircling and related to the point "1".

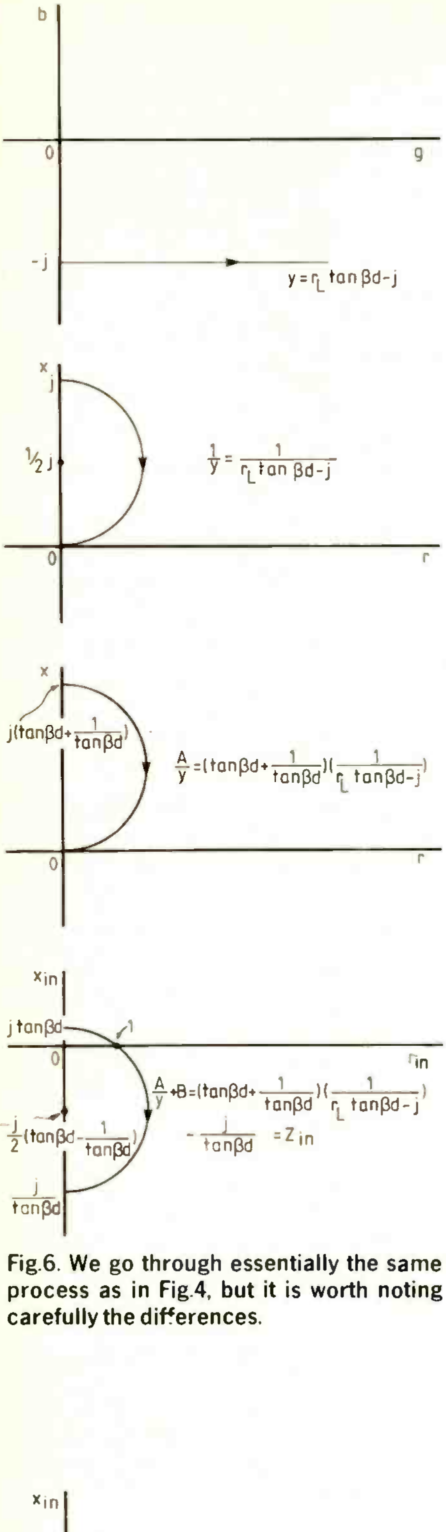


Fig.6. We go through essentially the same process as in Fig.4, but it is worth noting carefully the differences.

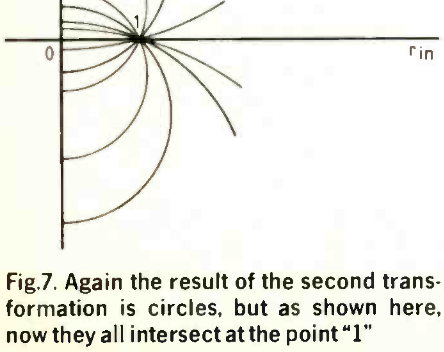


Fig.7. Again the result of the second transformation is circles, but as shown here, now they all intersect at the point "1"

on the z-plane.

Put $y = r_L \tan\beta d - j$ and plot it, but only for positive r_L as in Fig. 6(a). Invert it, to give Fig.6(b). Now magnify it by the first factor, giving Fig. 6(c). Finally, shift along the imaginary axis by

$$-\frac{j}{\tan\beta d}.$$

Figure 6d shows the final result.

As you chose different values for d, or rather for d, you get another whole family of circles, all cutting the S circles at right angles, as in Fig. 7. They can sensibly carry the name *constant d*, or probably better, *constant d circles*.

Figure 8 illustrates the final *rectangular impedance chart* we have fairly rigorously obtained. You can apply it straight away, but notice how it goes off to infinity for some values. This requirement for a very large sheet of paper set people thinking of alternatives.

THE POLAR CHART

Quick thinking readers might already have begun to realise that the geometric inversion carried out in the box packs the whole of the infinite half plane, $z = r \pm jx$ from 1 on the "r" axis to ∞, into the unit circle on the transformed complex plane. But note, r has to be 1 or greater. Between 0 and 1, all the other circles out to infinity appear. You might wonder how, by excluding all interesting values of normalized resistance r_L less than 1 (i.e. $R_L < Z_o$), anything of value would accrue by further transformations.

The answer is that values of r_L less than 1 are not excluded, but *negative* values are. Negative resistive parts imply active devices – amplifiers, say – and we leave these out of the argument for now. The geometry that requires a plot from *unity* outwards means we start by shifting the axes so that $r_L = 0$ begins at 1. You might think doing that is too much of a wangle, but surprisingly the mathematics of transmission lines automatically fulfils this requirement. Also, the rectangular chart fails to bring in the important reflection coefficient ρ. You could write the complex number ρ in its rectangular components form $\rho = \rho_r + j\rho_i$. But we can do better for the present purpose by looking at the other representation – its magnitude and angle.

$$\therefore \quad \rho = |\rho|\underline{/\phi - 2\beta d} = \frac{z_{in}-1}{z_{in}+1}$$

Notice that the 1 in the denominator adds to z_{in} to give just the start we require. The left-hand side represents a family of circles centred on the origin, radius $|\rho|$ which has a maximum value of 1, however large or small $|z_{in}|$ becomes. The angle $\phi - 2\beta d$ steps out round the circumference according to values of d. In other words, the picture is a plot of ρ in polar coordinates; see Fig.2.

The right-hand side contains z_{in}, which is $r_{in} \pm jx_{in}$, the rectangular axes of our earlier impedance chart, so that when inverted, these axes form the curves obtained. To geometrically invert $(z_{in}-1)/(z_{in}+1)$ add and subtract 1

$$\rho = \frac{z_{in}-1}{z_{in}+1} - 1 + 1$$

$$= -\frac{2}{z_{in}+1} + 1$$

As I mentioned, the 1 in the denominator of the first term means everything transforms into the unit circle. Figure 9(a) shows this denominator plotted. Do the geometric inversion, as in Fig. 9(b). Now magnify by 2, the numerator value, and rotate about the origin (because of the minus sign), so as to arrive at Fig. 9(c). Finlly shift the whole picture to the right by +1, as instructed by the remaining term. The final result shown in Fig. 9(d) presents us with the Polar chart which, in its modern commercialised form, everyone calls the Smith chart[2].

I find it interesting that, as early as 1930, A.C. Bartlett derived and used the chart in his book on artificial transmission lines[5], as his Fig.144, reproduced here as Fig.10, shows. This in no way detracts from the clarity with which Philip Smith rendered it as a tool for direct use as a saleable commercial item but shows that, yet again, there is nothing new under the sun.

INTERPRETATIONS

Success with the chart definitely improves with practice. You will find a large number of books with many practice examples at the ends of the chapters containing details of the Smith chart[6,7]. So if you are rusty with its use, or if you have yet to master it, now is the time to have a go.

But if you scrutinize the chart, a great deal comes out of it before approaching even the first example. The complete circles – the ones converging down to the point 1 on the right – come from the transformed lines parallel to the positive r_{in} axis corresponding to fixed reactance values. They form the *constant resistance circles* on Smith chart. The other set of the partial circles cutting all the first ones at right angles, come from the transformed vertical lines through fixed resistance values, parallel to the $\pm x_{in}$ axes. This means that all the points of intersection of the circles yield or correspond to the various values of z_{in} with a positive real part. *Negative* real parts would drive the point of interest *outside* the circumference of the chart. Indeed, you can obtain special charts with some of these outer regions plotted, to handle some of the reflection-amplifier analysis that turns up in microwave systems. $|\rho|$ occurs with values greater than 1, which means negative resistance – or *gain* – has appeared on the end of the line.

Journeys round the chart correspond to travelling along the transmission line. One complete trip round corresponds to a half wavelength. Half way round naturally means a journey of a quarter wavelength. The value of z_{in} at the start of a quarter wave journey, transforms to the diametrically opposite point, which an examination of the chart shows to be its reciprocal. From this, you can see the transforming action of a quarter wave stub again. The fraction cut off along the radius line through z_{in} gives the value of $|\rho|$ and the angular position yields ρ. The rectangular values of ρ, ρ_r and ρ_i could be found by reinstating the discarded rectangu-

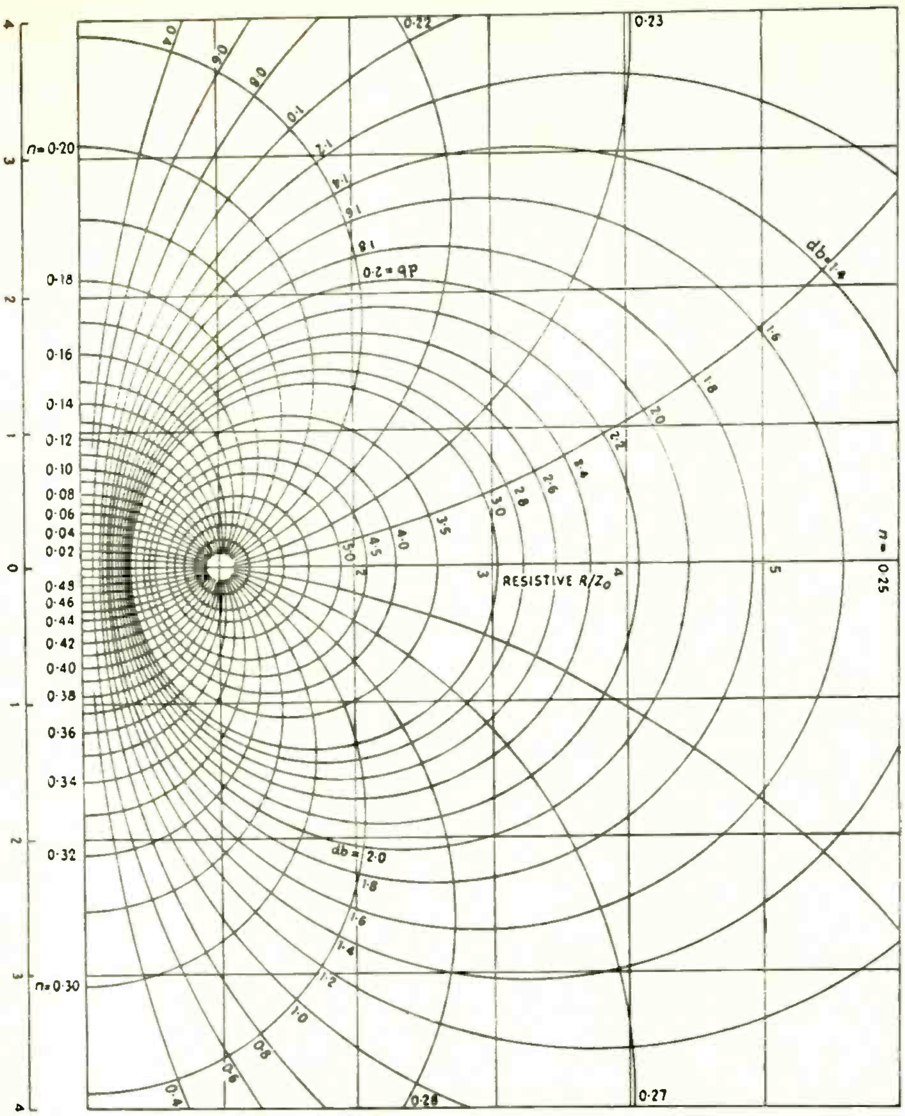
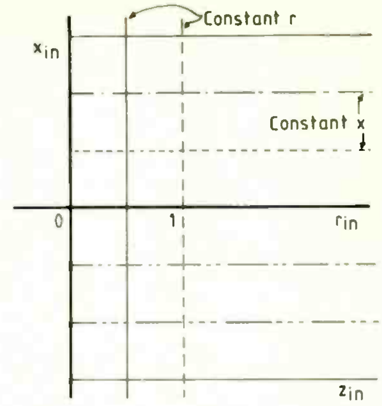
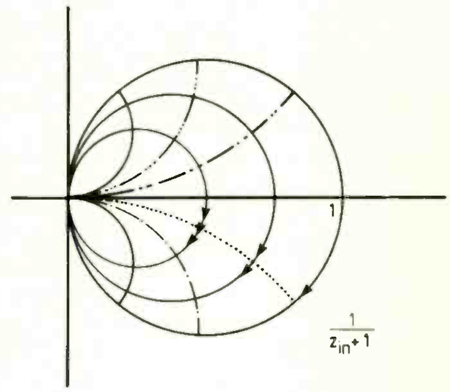


Fig.8. The final result is a the once popular Rectangular Impedance Chart which you can still use in its calibrated form shown. (Acknowledgements to "Services Textbook of Radio" 1966, HMSO and *Wireless World*)





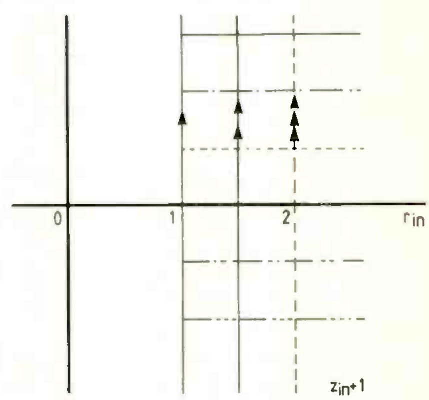
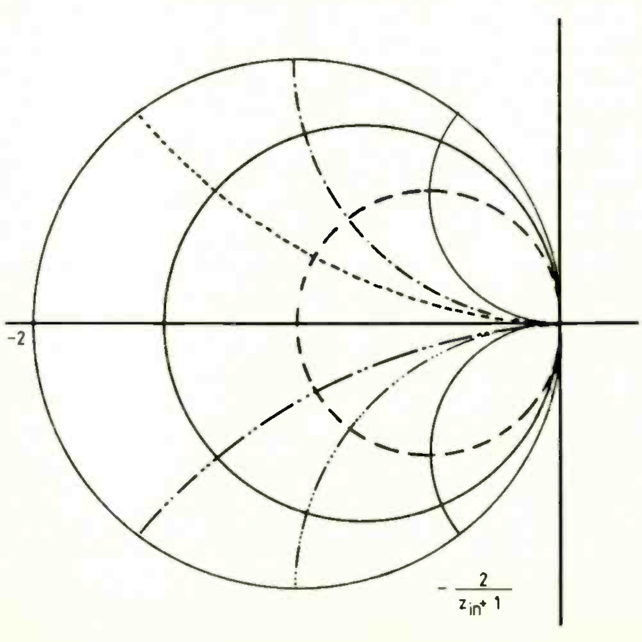
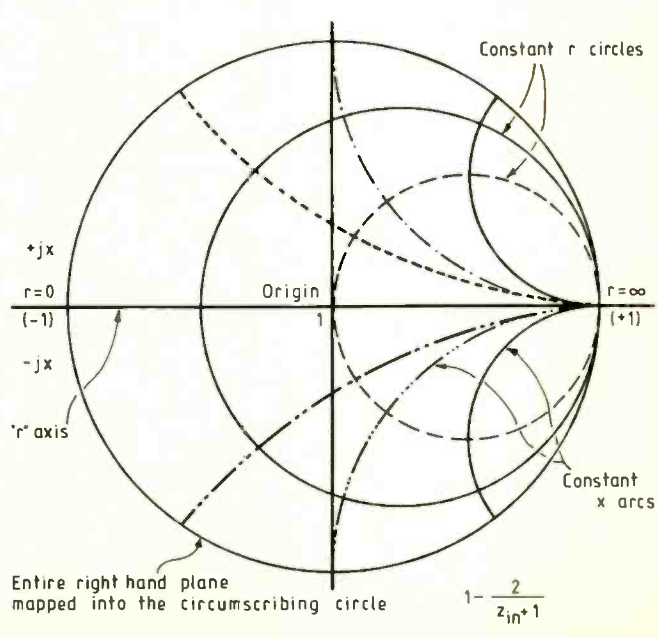


Fig.9. In reality, these transformations amount to similar inversions already illustrated in Figures 4 and 6. But there are a few more interesting stages, such as the "rotate" operation. The final result is the Smith chart in d. (Acknowledgements as Fig.8)





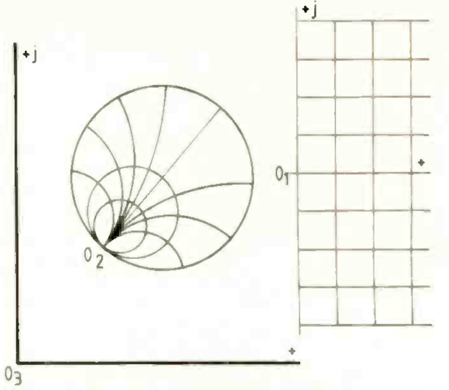


Fig.10. This Figure and discussion can be found in Bartlett's book of 1930[5]. His Fig.144 clearly shows the derivation of the Polar chart.

lar axes on the chart, but you will find this rarely done. On the other hand, drawing a circle round the centre of the chart through the point z_{in} cuts the horizontal (resistance) line to the right of the centre at a value r_L and, as the standing wave ratio S, as we have defined it, equals r_L ($r_L > 1$), you can read off the v.s.w.r. directly. For this reason, the cirlces round the centre are called the S circles. They correspond to the rectangular chart S circles.

You soon get used to journeying arond the chart on constant-S circles, constant-x circles and constant-r circles. In whatever way you have journeyed, the point of arrival gives you z_{in} straightaway, plus all the information about the reflection coefficient and the v.s.w.r. We make the journeyings on the chart for some design or analysis purpose. The normalized value of 1 (at the centre) very often forms the terminus, because the matching condition of your system occurs there. So all the arcs and twists tend to home onto 1 and if you manage to do it, then your stub positions, lengths, capacitor and inductor values have all combined to match the system, whatever your starting impemdance point was. *To be continued*

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Wireless World carried an interesting article on the Smith chart by R.A. Hickson in the January 1960 issue, who discussed the meaning the circles and hinted the method of derivation I adopted here.

The book, "Microwave Circuits" by V.F. Fusco, Prentice Hall, 1987, contains a discussion of the chart and gives a program listing (BBC Micro) to plot the chart and enter impedance points via the keyboard.

Geometric inversion, or transformation $Y = 1/z$

The general *bilinear transformation* from the complex y-plane to the corresponding complex z-plane is,

$$z = \frac{a+by}{c+dy}$$

But simpler versions of this, based on the form $y = 1/z$ always turn up in the present context. There may be a real scale factor multiplying this equation. A real term might be added to z, which will be a shift in that plane. Finally, a term might be added to the whole of the right hand side. This would correspond to a shift on the y-plane. The result, generalized as far as we ever want to go in understanding charts, looks like,

$$y = \frac{A}{z+B} + C$$

and to transform this, one relies only on knowing how to handle the interpretation of $1/z$. Whether we go z to y, or y to z involves the same reasoning.

If y is the complex number of g + jb and similarly z equals r + jx then the transformation from the z-plane to the y-plane involves taking the reciprocal of complex numbers. Traditionally in this subject the reciprocation is called an *inversion*.

Consider the z-plane. If r remains constant and x varies, we get all the vertical lines, as in Fig. A1. Similarly, all the horizontal lines come from keeping x constant and varying r. Study the geometry in Fig.A2. Construct the circle OBAO so that OA = 1/OC. The problem is to obtain the relationship between any point D on the vertical line and the corresponding point B on the circle. In other words, how does B vary as D varies?

Angle OBA is a right angle. O is common to triangle OAB and triangle OCD, therefore these triangles are similar. In particular,

$$\frac{OB}{OA} = \frac{OC}{OD}$$

Using the condition that OA = 1/OC we obtain OB.OD = 1. This means that OB = 1/OD for *any* D, indicating that the transformation $y = 1/z$ maps any point z on the vertical line in the z-plane to a corresponding point y on the circle, which lies in the y-plane. All the vertical lines on the z-plane maps onto the various circles on the y-plane.

Applying this to admittance/impedance transformations shows that

$$y = \frac{1}{z} \text{ or } |y| \angle\phi_y = \frac{1}{|z|\angle\phi_z}.$$

$$\text{Therefore } |y| = \frac{1}{|z|},\ \phi_y = -\phi_z, \text{ and}$$

and the upper semi-inifinite line segment on the z-plane maps onto the lower semicircle on the y-plane, because of the sign change in ϕ. The more remote vertical lines – produced as r tends to infinity, map into smaller diameter circles shrinking onto the origin – as y tends to zero, see Fig.A4.

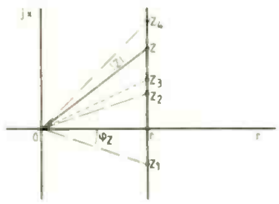
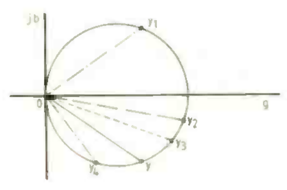


Fig.A1. This shows that for a fixed r, as jx varies the phasor drawn from the origin to point z varies through all lengths |z| and in angle ϕ_z, from $-\pi/2$ to $+\pi/2$ radians.



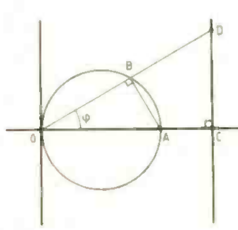
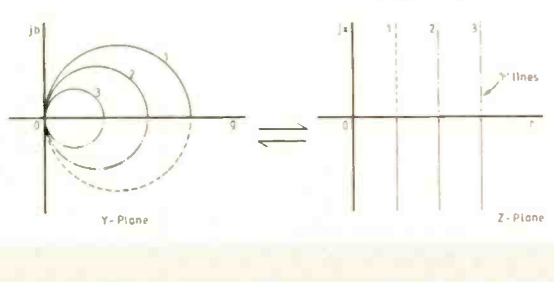


Fig.A2 By similar triangles, point D on the perpendicular through C inverts to point B on the circle. The higher D travels, the further B moves round the circle towards the origin.

Fig.A3 The actual inversion of all the sample phasors on Fig.A1 appear as corresponding points on the circle shown here. A phase reversal places the *top* segment of the constant "r" line in Fig.A1 onto the *lower* semicircular arc, as shown.

Fig.A4 The whole family of constant "r" lines on the z-plane map into a family of circles on the y-plane. The more distant "r" lines map into the smaller circles.



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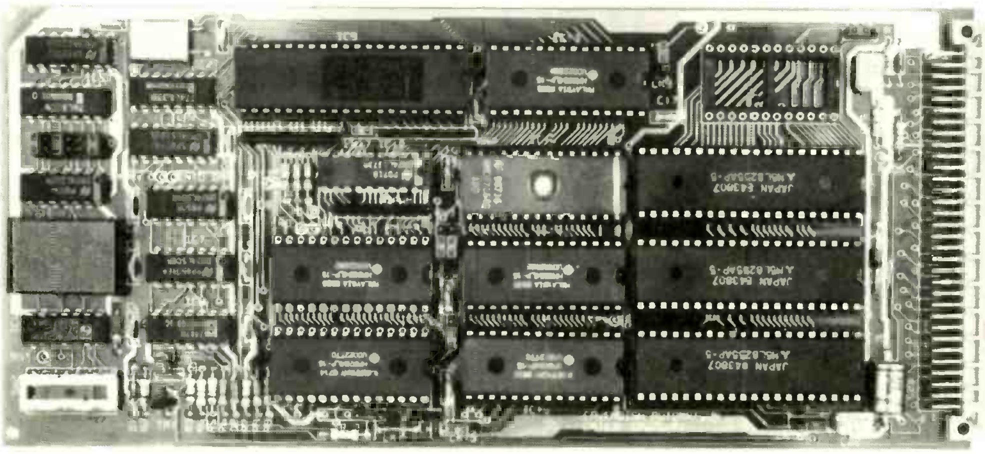

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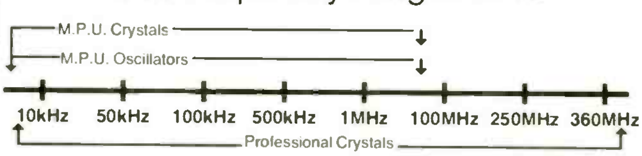

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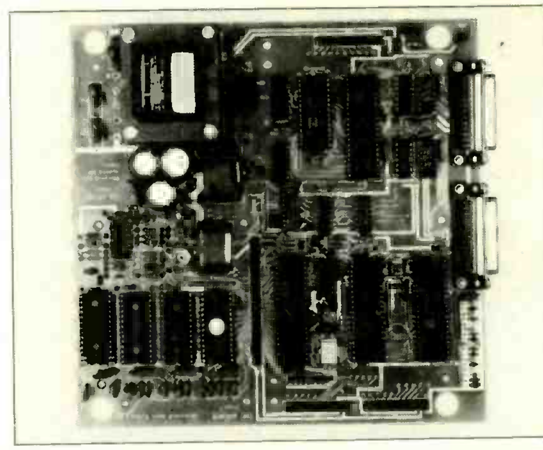

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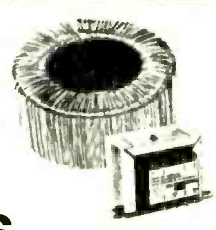

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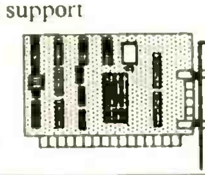

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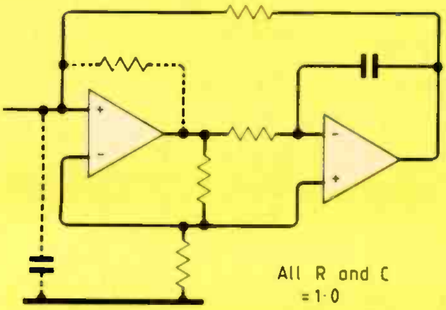
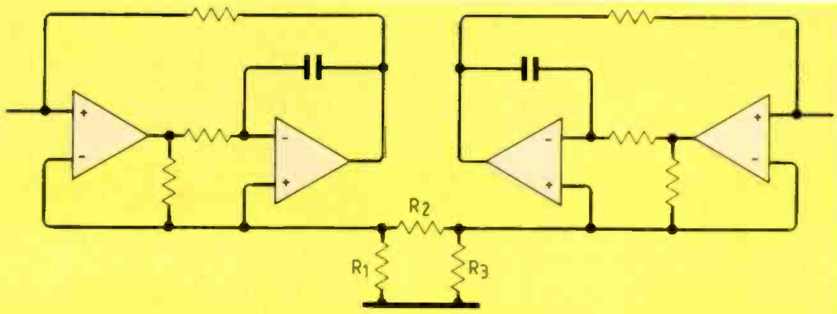




Inductance synthesis

Theoretically, this circuit for synthesizing inductance to ground has no loss, and it does not need matched resistors. In practice, it can be used to produce low-frequency resonant circuits with a Q of about 1000, its loss depending on capacitor loss and amplifier characteristics.

Adding the capacitor and resistor shown dotted turns the circuit into a sinewave oscillator. Because Q is high, the resistor, which provides, negative loss, can have a very high value. This high value results in a waveform better than might be expected, but of course not as good as one produced using some form of quasi-linear amplitude control.

Negative loss can alternatively be obtained by moving the non-inverting terminal of the second amplifier upwards slightly on the divider, which may avoid the need for an awkwardly high-valued resistor.

In the second diagram, two of these circuits are shown connected back-to-back. This arrangement synthesizes an inductance pi, in which $L_1=R_1$, $L_2=R_2$ and $L_3=R_3$. Its main application is very narrow bandpass filters with very low centre frequency. It is curious that only two capacitors are needed to simulate three inductors.

For wider pass bands requiring Q of only 20 or so, other circuits are probably less expensive. See 'A handbook on electrical filters', White Electromagnetics Inc., 1963, p. 175 for design data on passive filters of this type.

McKenny W. Egerton, jr.
Owings Mills USA

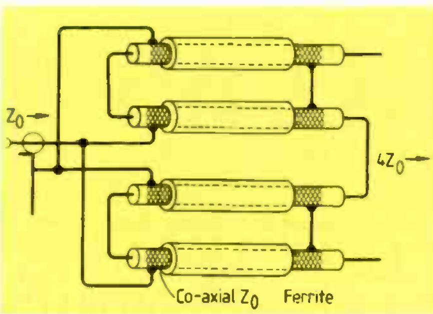
Isolating wideband balun

It is well known that a wideband balanced-to-unbalanced transformer of 4:1 impedance ratio may be realized using two equal-length transmission lines having characteristic impedance $2Z_0$. These two lengths of transmission line must be surrounded with high-permeability ferrite, or wound onto two separate ferrite cores.

It is not possible to have d.c. isolation with this type of balun but it is possible with the arrangement shown here using four lengths of transmission line of characteristic impedance Z_0. They are connected in series/parallel on one side to give impedance Z_0 and are all connected in series on the other side to give impedance $4Z_0$.

This type of d.c.-isolating wideband balun does not appear to have been described previously. I have tested the idea using four 150mm lengths of RG178B/U 50Ω coaxial cable. Instead of the ferrite tubes shown in the diagram, 16 Mullard FX2633 beads of A13 ferrite were threaded onto each cable. These beads are a sliding fit on the cable.

I assessed the balun's performance by observing the pulse response at the input with a good quality 200Ω termination connected across the output. Rise-time measurements showed that high-frequency performance was much better than the 250MHz bandwidth of the oscilloscope being used for the tests. Low-frequency performance, determined by the number of ferrite beads, was assessed by observing the decay time constant on the amplitude of a long-duration pulse input. The result was a decay time constant of 2μs.



A second version of the balun was made from four 1.5m lengths of RG178B/U cable wound on four separate high-permeability ferrite toroids. This gave an inductance of 3mH to each cable and resulted in a much longer decay time constant of 100μs. However, the high-frequency performance of this second version was very poor due to the self-capacitance of the toroidal windings.

It is clear that the linear layout shown here is essential for really good high-frequency performance.

T.H. O'Dell, London

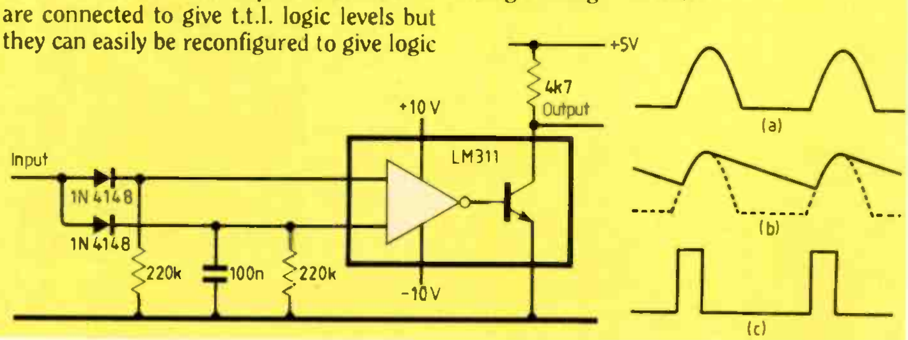
Interrupt generation

I needed a circuit to interrupt a processor at precisely the positive peak of a low-frequency sinusoidal signal. Here is a novel, inexpensive solution that produces an appropriate pulse with timing insensitive to typical amplitude and freqency changes.

Input to the circuit is a sinewave voltage proportional to the voltage of interest and scaled to approximately 10V pk-pk. Output is a squarewave whose negative-going edge occurs at the input waveform's peak.

Component values shown are for a 50Hz sinusoidal waveform and result in 0.1ms error in 20ms. The circuit is suitable for higher frequencies provided that the capacitor is reduced inversely with frequency. Emitter and collector outputs of the LM311 are connected to give t.t.l. logic levels but they can easily be reconfigured to give logic levels suitable for the inputs of any microprocessor.

G.D. Bergman
King's College London



CIRCUIT IDEAS

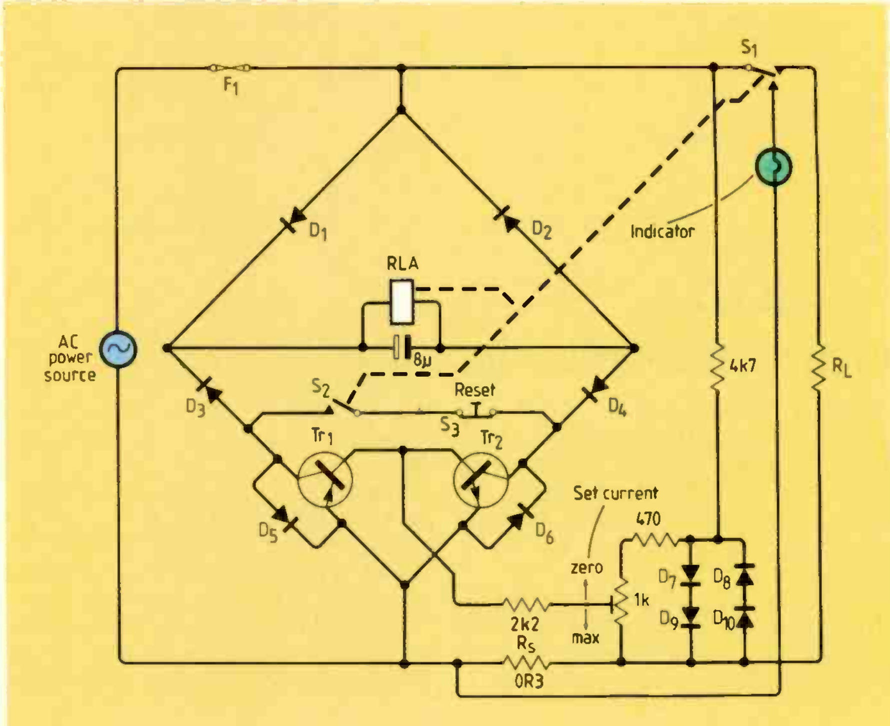
Overload cut-out for a.c. supplies at waveform peak

Tired of replacing fuse wire in a heavy-duty alternating supply, I designed this electromechanical cut-out. It has a continuously variable current threshold level, adjustable from about 1mA, and it works when the overload is caused by a rectifier.

Diodes $D_{3,4}$ are switched in and out by $TR_{1,2}$; normally these transistors are off. When an overload occurs during a positive half cycle, voltage across sensing resistor R_s switches Tr_2 on, causing current to pass through D_1, the relay coil, D_4 and Tr_2. Relay switch S_2 causes the relay to latch on and switch S_1 cuts out the supply. Bypass diodes $D_{5,6}$ now come into play, and conduction is through D_1, RLA, D_4, S_2 and D_5. The relay remains latched on until the reset push-button is pressed. Operation during negative half-cycle overloads is similar since the circuit is symmetrical.

Note that the 8µF smoothing capacitor must be initially charged through the transistors. Light-emitting diodes could replace $D_{3,4}$ to provide an alternative overload indication, provided that their current ratings are not exceeded. A 470Ω resistor in series with the potentiometer will remove the dead band.

P.J. Ratcliffe
Stevenage
Hertfordshire



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NEXT MONTH

European h.d.tv standard. Tom Ivall describes the events leading up to the September demonstration in Brighton of the 1250-line television system which is a step towards a compatible European, and possibly worldwide, production standard. The equipment is described in detail.

Efficient step-up switching regulator. Integrated circuits for switching regulation exist, but have their drawbacks. Messrs Chaffey and Perkins of the Medical Research Council present a 90+% efficent design to provide 44V at currents from 1.5 to 60mA from a 8.5V NiCd battery.

Microcomputer-controlled keyboards. Many keyboards, for many purposes, are controlled by microcomputers. Jeff Wright of Motorola describes the pros and cons of several types and details the software and hardware techniques employed.

Probing for fast pulses. Another logic probe, but different. This design is able to capture "glitches" that are normally difficult to find by oscilloscope. The design lends itself to realisation by programmable logic, which makes for small size and allows pulse analysis for only a few extra components.

IEEE488 interface. John Adams' SC84 microcomputer, the design for which appeared in this journal some time ago, is adaptable and can accept extra facilities as plug-ins. This IEEE488 interface has been in use in a satellite instrument testing facility at Oxford, performing control and data-collection activities.

Pioneers – Alec Reeves. This month's subject in W.A. Atherton's series on the pioneers of communications is Alec Reeves, perhaps best known for his work on pulse-code modulation, although he was also the originator of Oboe, the bombing aid used by the RAF in WWII.

Wires plus switches equal digital circuits

The Calculus of Indications applied to digital circuit design.

A. MEDES

Prompted by the continuing articles in this journal on the application of logic to digital circuits, together with my own recent criticisms of logic[1] I shall present here not another notation for logic symbols but rather an original and self-contained method that can be applied to the design of digital circuits. The method is called the Calculus of Indications and is rigorously developed by Spencer-Brown in Laws of Form[2].

Before I start with the calculus I would like to comment on some aspects of digital circuits that are not always made clear. Some confusion seems to arise from the way logic symbols are drawn, or rather from what is omitted from the symbols. For instance all silicon-chip gates (74 series t.t.l., 4000 series c-mos, etc.) have power and ground connections, but since all such gates have these two connections it is redundant to show them on the specific symbols. It is because only the input and output connections are shown on the symbols that it is sometimes, wrongly, assumed that the output is derived via some switching network from the inputs. Hence the problem of how an inverter can generate a high (5V) at its output when there is nothing (−0V) at its input.

There is a similar omission in the symbols used for switches. Here, the switch is usually drawn as a two-terminal device, the signal line that does the switching being omitted. With this extra signal added, be it someone's finger, relay coil current or transistor base current, the simple switch becomes less simple. Also, bistable on-off switches and toggle switches are quite complex (even in their mechanical construction) compared with, say, a momentary contact switch. This complexity renders traditional logic useless for their description. In what follows I shall try to show how the Calculus of Indications can resolve these problems.

According to William of Occam, if we have two descriptive systems of equal scope, then the preferred system is the one with the simpler initial assumptions.

Considering logic, we find that it is a system originally intended for determining the truth or otherwise of verbal arguments. Developments by Boole, Pierce, Whitehead and Russell, Sheffer, Nicod and others generally tidied up the framework of logic and gave it a rigorous mathematical appearance.

In Sheffer's representation we take as given the concepts: there is a class with at least two elements (say 0 and 1): there is a binary rule of combination (say a Nand gate with two inputs and one output): if the binary rule is applied to the same element, say A, then we define the result as Not (A); there are some initial (unprovable) equations such as Not (Not (A)) = A, A Nand (B Nand Not (B)) = Not (A) and Not (A Nand (B Nand C)) = Not (B) Nand A) Nand (Not (C) Nand A). From the above axioms we can then derive the rest of logic.

But there is also the unwritten notion that logical arguments must sound correct. So when Whitehead and Russell arbitrarily introduce the Axiom of Reducibility and its attendant Theory of Types, in Principia Mathematica[3] they do so because "it has a certain consonance with common sense which makes it inherently credible". We shall return to this "common sense" later.

The Calculus of Indications takes only two axioms for its foundations and these axioms are of an arithmetical nature rather than the algebraic nature of logic's axioms. The algebraic theories of the calculus are then derived from the two axioms. Furthermore, the scope of the calculus can be extended beyond the scope that is allowed of traditional logic. So by Occam the calculus should definitely be preferable to traditional logic.

In what follows I shall present a practical interpretation of the calculus that should be more familiar to digital circuit designers than the formal presentation in Laws of Form. The names I use in describing the calculus shouldn't be taken too literally. The calculus is a mathematical construct and so we can name its parts in whatever way we choose; here I have chosen names that I think will give the reader the best feeling for the way the calculus works.

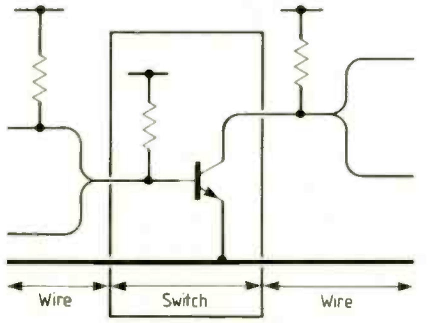


Fig.1. Open-collector n-p-n inverter. The transistor is effectively a two-terminal device.

The two axiomatic elements are the passive wire and the active switch.

The undisturbed wire will float at its recessive state until a point on it is actively driven to the dominant state. This dominant state will then propagate to all points on the wire. The usefulness of the wire is its ability to propagate a signal throughout its space.

The switch can be thought of as a two-terminal device that, while undisturbed at its input, will emit the dominant state from its output. In the formal description, the undisturbed switch is equated to the dominant state. When the switch is actively driven at its input then it emits nothing from its output. The usefulness of the switch is its ability to cause change.

So the wire and the switch can be compared to the open-collector inverter in Fig.1. In an n-p-n implementation, the wire floats at the positive voltage, the recessive state, until it is pulled down to ground, the dominant state. The switch with a floating input pulls its connector to ground, while the dominant ground state at the input will effectively disconnect the output. The emitter is connected to ground for all the switches so it may be thought of as an internal property of the switch. Thus the emitter is not a third terminal.

For n-p-n t.t.l and n-mos the ground line is seen to represent the dominant state, explaining the term "current sinking logic", the floating high of unconnected inputs and the ubiquity of active-low signals. If we use p-n-p or p-mos, then the positive rail is dominant and the ground rail recessive.

Not too much should be made of this correspondence between the calculus and the practical implementation of t.t.l. In mos circuits, the transistors act as three-terminal switches and mos gates with equivalent functions to t.t.l. gates have different circuit arrangements. For instance, c-mos uses n-mos transistors to pull the output signal down and a complementary (not mirror image) arrangement of p-mos transistors to pull the output signal high. Nevertheless, the calculus can still give a full theoretical description of the c-mos circuit functions.

Figure 2 is a circuit of an open-collector Nand gate. Here, the signals on the wires that connect to the two inputs are separated by the input diodes. The fan-in of signals thus occurs within the gate whilst the wire connected to the output will fan-out to connect to several other gates.

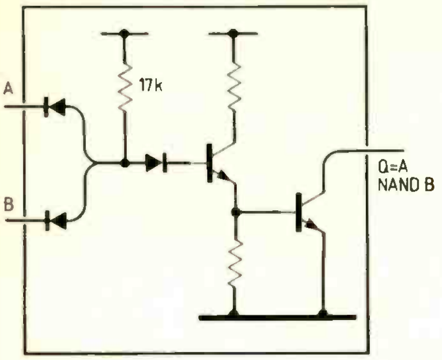


Fig.2. Open-collector Nand.

Figure 3 shows that the opposite case is equally valid: a gate can have a single input and multiple outputs by simply sliding each diode along its wire to the previous gate. We do not have to introduce the concept of a diode into the calculus (or the circuit), since we can replace each diode with a switch (the transistor), with the switch inputs tied to the common input wire. In practice, diodes are used as they are more economical than transistors.

So, as Fig. 3(c) shows, the wires do all the fanning-in and fanning-out, having many switch inputs and outputs tied to them while the switches are all simple, two-terminal devices which interconnect the wires.

From Fig.2 we see that while the circuit is on the chip the pull-up resistors are relatively large, here 17 kΩ. Once the signals travel off the chip, then to maintain speed the pull-up resistors have to be matched to the wire's transmission line impedance which is around 100-200 ohm (the signals actually travel between the wires and the ground rail that is common to all switches). With a 5V power rail this means that each switch would have to be capable of sinking 25-50 mA (i.e. a lot) and hence the development of the totem-pole output. The totem-pole uses a second transistor between the pull-up resistor and the wire, disconnecting the pull-up while the output is in the low state. This in turn has led to the development of the tristate output since, if we have two totem-pole outputs connected to the one wire, with one pulling up and the other pulling down, then the result is a disheartening puff of smoke.

Totem-pole outputs are best suited to circuit topologies such as that in Fig. 3(a) where the gate drives a single output wire and there is less chance of connecting the gates on the circuit board so that a wire is being simultaneously pulled up and down.

The high power cost of the pull-up resistor circuit can be lessened by using high-value resistors (most microprocessors available today use n-mos switches and pull-up resistors of about 40kΩ) or by reducing the supply voltage, power being proportional to V^2/R. Alternatively the c-mos approach can be used to reduce power drain (to virtually zero in the static case) but at the expense of using twice as many switches and more complex circuits. Since silicon switches are small compared with their interconnecting wires and the 5V supply voltage is well standardized, the trend today is towards more c-mos circuits.

Figure 4 shows the basic elements of a neuron, or nerve cell. Signals received at the input synapses are passively propagated via the dendrites to the soma where, when they cross some threshold value, the soma generates an output signal that propagates and is regenerated along the axon and out at its synapses. So here we see the similarity between the wires and switches of the calculus and another practical and very useful circuit device.

Now the neuron is a much more intricate device than, say, a Nand gate. The input synapses can be activating or inhibiting, an activating synapse being analogous to a non-inverting buffer and compensating for any signal loss, while the inhibiting synapses act as inverting buffers or as the switches of the calculus. Also, the output signal is not steady but pulsing and forms in a sense a switched mode power supply. The biochemical energy is supplied at about 0.1V (in the form of varying ion concentrations across the cell wall) but to conserve effort the axonal current only flows in short pulses of a few milliseconds every few tens of milliseconds. The chemical lag of the synapses together with the resistance and capacitance of the dendrites then combine to smooth the signal.

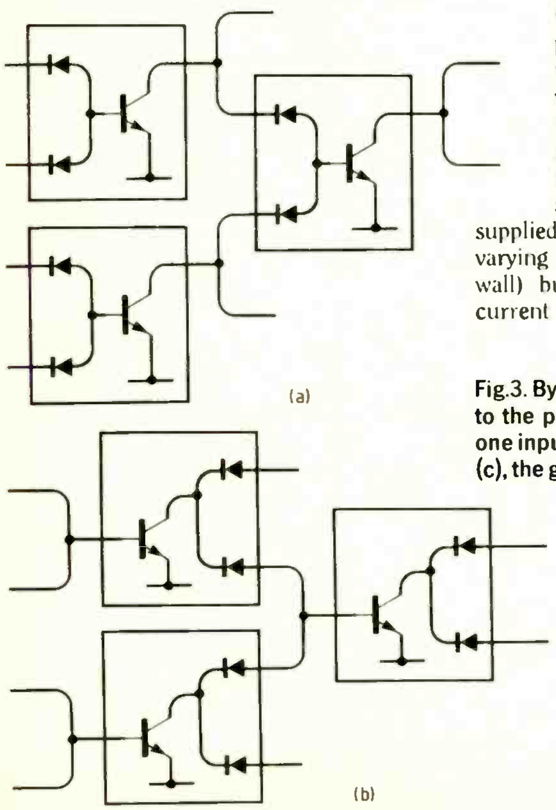


Fig.3. By 'sliding' the diodes along the wires to the previous gate, as in (b), a gate with one input and multiple outputs emerges. At (c), the gates are all simple switches.

And, most importantly, since the neuron is alive it can grow and so change its shape. This enables a neuronal network to effectively rewire itself by the selective attenuation of signals. This happens when the dendrite grows larger in volume and so smaller in electrical impedance under a preferred synapse, thus allowing more of that synapses' signal into the dendrite and thence to the soma, or else the dendrite atrophies under an undesirable synapse causing that synapse to see a greater impedance to its signal and become to an extent disconnected.

Despite these intricacies of the neuron's workings there is a strong correspondence at the fundamental level between the wires of the calculus and the neuronal dendrites which passively propagate the signals. And the switch and the soma with axon which are either at rest or can actively supply an energetic signal dependent on the state of their input. This correspondence is seen clearly by comparing Fig. 3(c) with Fig.4.

Returning to the calculus, we have in Fig.5 the arithmetical initials, essentials the two axioms of the system.

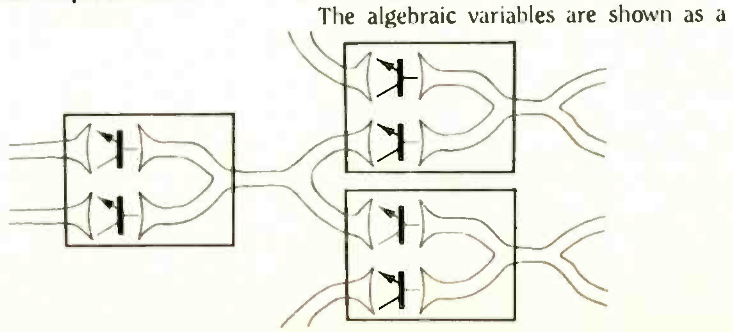
The notation uses our usual convention that the signal flow is from left to right. The vertical bars represent the inverting switches with their inputs to the left and their "open-collector" outputs to the right. The lines connecting the switches are the wires, assumed to be suitably pulled to their recessive states. A circuit topology such as that in Fig. 3(c) will be used from here, since it is closer to the formal representation of the calculus. That is, each inverting gate will be shown with a single input but may have multiple outputs.

Figure 5(a) shows that if two switches are actively driving a wire to the dominant state then the result is the same as if only one switch is actively driving it. That is, two dominant states on a wire is the same as one dominant state. The switches are emitting the dominant state since their inputs are not connected to anything and so must be floating at the recessive state.

Figure 5(b) tells us that if a switch has the dominant state at its input then its output is unaffected. That is, two inversions equals no inversions.

From the arithmetical initials we can derive the two algebraic circuits of Fig.6 which become the initials of the algebra. In Boolean notation 6(a) is $\bar{A}+A = 0$, and 6(b) is $(A+C).(B+C) = A.B+C$.

The algebraic variables are shown as a



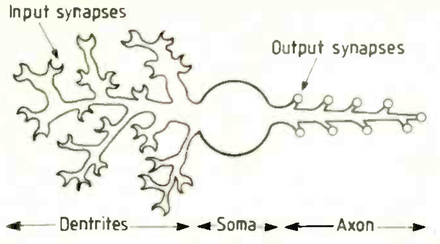


Fig.4. Elements of a neuron, composed of 'wires' and 'switches'.

letter inside a circle. Each variable represents an unknown circuit of wires and switches, the output of which (either recessive or dominant) is the state of the wire attached to the variable. Variables can have multiple outputs or, to improve the clarity of complex circuits, the variables can be written down in several places around a circuit.

From the algebraic initials we can derive numerous consequences, some of which are shown in Fig.7. We can also prove theorems (for these feed-forward circuits) such as "any circuit can be rearranged so that it is no more than two switches wide" (that is the signals need pass through at most two switches) and "any circuit can be rearranged so that there are not more than two connections to each variable".

We are now at the stage where we can rearrange circuits as easily as we can rearrange the more usual algebraic expressions. For instance, in algebra we use cross-multiplication to add two fractions whereas in the calculus we might use crosstransposition as a "short cut" in the manipulation of a circuit. Naturally, to do this easily we would have to do our homework, just as was the case with our primary school algebra.

This ease of manipulation becomes useful when we have a circuit such as the left side of Fig. 7(e) and we want to speed up the signal from A relative to B. With a few strokes of our pencil we have the right side of 7(e) and now A has a shorter delay than B.

To solve the same problem with traditional logic we first rewrite the circuit in the Boolean notation, say $(A+B)+C)$ the start rearranging the expression, not forgetting that logical '+' and '.' behave differently to numerical + and ×, and ending up with $(\bar{A}.\bar{C})+(\bar{B}.\bar{C})$, which does not make the propagation delays of A, B or C very apparent.

Alternatively, we can use Karnaugh maps; that is, draw a grid covering every possibility for the variables involved, fill in the spaces corresponding to the given expression, and then try to extract another expression that suits our design goals. To me, the Karnaugh method is about as sophisticated as doing sums on your fingers; easy to learn but slow and nearly impossible when the numbers become large (more than about five variables).

Figure 8 shows some circuits with their sentential logic equivalents (true equated to the dominant state).

The Or gate shows that we can have a gate without any active elements. The active elements, the switches, are within A and B but we note that, if A is emitting the dominant state, then any change in the signal from B will not be noticeable. A must be recessive to allow the signal from B to pass. This is the reason for naming the two states "dominant" and "recessive".

The complementary nature of And and Or is made obvious by the circuit notation. Inverting the inputs and outputs of either produces the other.

Figure 8(e), assuming a fast switch or slow wire, is an oscillator. The sentential logic equivalent is the liar paradox or "this sentence is false"; something that is just not allowed in logic according to the Theory of Types (which in essence says that the inputs and outputs of expressions must be of different types).

In digital circuit design this is called sequential logic, but if we look behind the name we find precious little theoretical backup. About the best that sequential logic can do is to break the circuit up into its combinatorial components and then, with much hand waving, say that the outputs are fed back to the inputs and everything starts again.

It is in this area that I believe that the calculus holds the greatest promise. It has a good formal and rigorous foundation and the step from the first-degree circuits, that is, without feedback, to the higher-degree circuits is a natural one. The situation is analogous to the step from real numbers to complex numbers[1], and it is the methods of manipulating complex numbers that make a lot of engineering design possible. To my knowledge there has not been much theoretical work done on this aspect of the calculus so, for those interested in the mathematics of circuits, here lies an opportunity for original research.

The importance of these feedback circuits goes even deeper. If you ask a professional mathematician what is the foundation of mathematics they will probably tell you, wrongly, that it is logic. That is, they prove theorems by using logical arguments. This leads to the ostrich posture, namely a head-first dive into the sand, that many mathematicians adopt when you mention Godel's Incompleteness Theory[4]. Though suitably obfuscated, this is just another example of the good old liar paradox. It is a well formed (and so true?) theory, that proves itself unprovable, or vice versa.

The gist of the liar paradoxes is that although they are embedded in a system that is supposed to give constant and unchanging results, the paradoxes are put in such a way that they must give different answers under

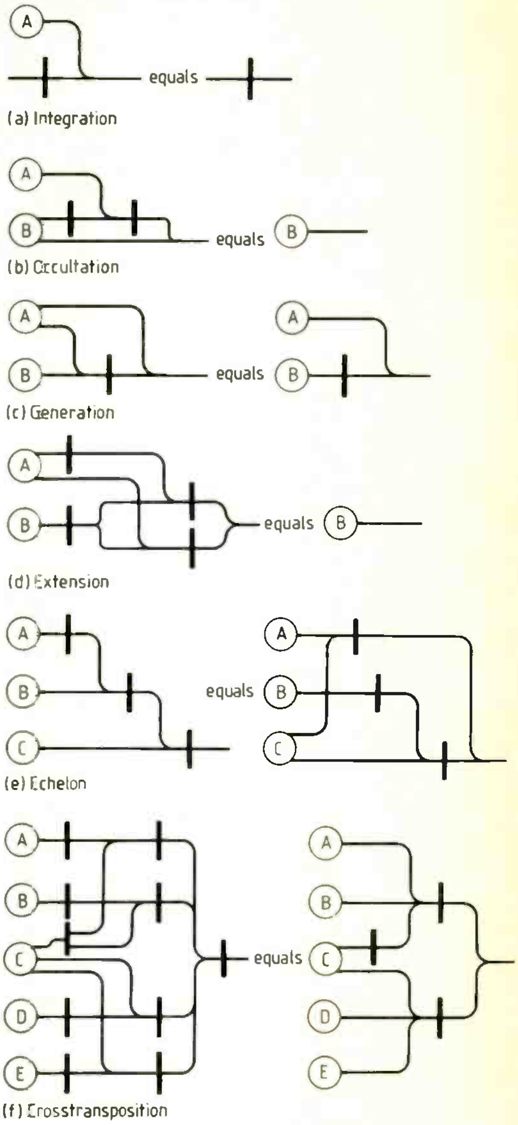


Fig.7. Consequences of the algebraic initials.

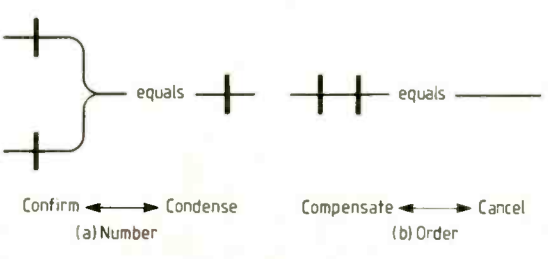


Fig.5. Arithmetical initials.

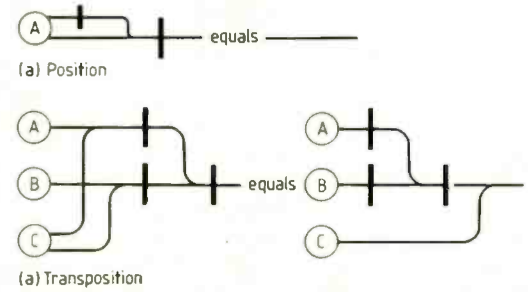
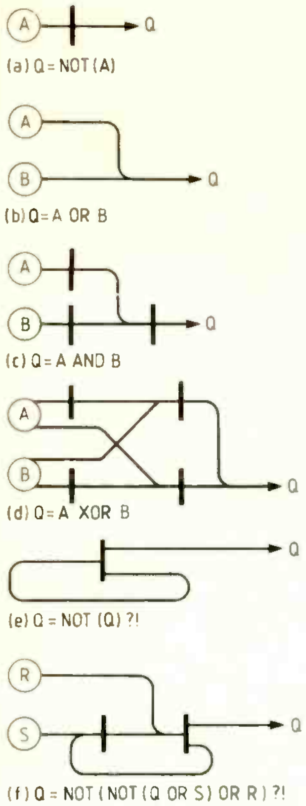


Fig.6. Algebraic initials.



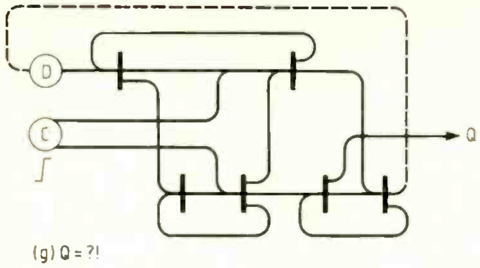


Fig.8. Circuits with their normal logic equivalents.

different initial conditions, that is at different times. Now, since nature doesn't seem to mind us building contradictory and time-changing circuits as in Fig. 8(e), perhaps there is nothing wrong with contradictory and time-changing theories in mathematics, especially as mathematics is often thought of as a model of nature. And perhaps these theories will even be useful, just as the oscillators in grandfather clocks and digital watches are useful in helping us count time.

Figure 8(f) is a bistable switch or R-S flip-flop or memory element. This is usually drawn as a figure eight but I think that the circular format makes the feedback more obvious. The sentential form is again seen to be self-referential but now, with the double inversion, it is not so contradictory. Rather the circuit is affirmative, which gives it its memory-keeping property.

Figure 8(g) is a D flip-flop, or with the dashed wire connected a toggle switch. The sentential form is by now long, incomprehensible and definitely self-referential, so I omit it. The circuit notation is also getting a bit much to draw every time we want to use a D flip-flop, so for this and more complex circuits I think it sensible to adopt the rectangular box notation.

In summary, we see that by starting from only two simple and naturally appealing axioms we can develop a descriptive framework that covers all possible digital circuits. Taking a subset of the calculus that has no feedback we have a complete model of traditional logic, yet we are not fettered by the (common sense?) restrictions of logic and can go on to investigate circuits of higher degrees.

In practice, we find that once we have done our homework we can use the calculus to rearrange circuits as easily as we can arrange algebraic expressions. And due to the close correspondence of the notation and physical devices we can easily implement a given circuit.

Should this calculus become popular enough that it is made available to engineering students I am sure that it would catch on and displace logic as an engineering subject, allowing logic to return to its rightful place amongst the social sciences. I hope this article will be a step towards the end.

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BOOKS

The art of digital audio by John Watkinson. Focal Press (Butterworth), £37.50. Thorough survey of digital techniques by the author of this magazine's long-running series on Compact Disc technology. Opening chapters supply an introduction to the principles of digital audio, and its pros and cons. Then the author describes in some detail the theory behind digital processing and recording and the complex methods of error correction used to ensure reliability. In the second half of the book, he analyses various practical digital audio systems, dealing at length with their hardware and software: rotary-head recorders (covering both ordinary video recorders and the new R-DAT consumer format), stationary-head recorders (including the DASH family of formats for the studio), digital audio in professional video recording and in the Video 8 format, disc drives for digital audio, and of course the Compact Disc. A clearly-written, comprehensive handbook for the engineer; expensive, but could well become the definitive work. Hard covers, 489 pages.

Introducing digital audio by R. Sinclair. PC Publishing, £5.95. Basic, non-mathematical treatment of digital techniques and systems, aimed at the technician, student or enthusiast. A section devoted to practical applications covers studio digital methods and the R-DAT and CD consumer systems. Also touched upon is digital sound synthesis and the MIDI system. Soft covers, 103 pages.

Mobile radio telephones in the UK by Dr R.C.V. Macario. Glentop Press, £9.95. In this comprehensive yet readable book, the author covers the basics of radio communication, the types of mobile radio systems and equipment in use today, digital technology and systems being developed for the future, and the current British regulatory set-up. Throughout, the approach is very practical, giving the reader a clear understanding of how everything works. The text is full of informative detail and is extensively illustrated with photographs and diagrams. This could be just the sort of book the mobile radio industry needs for the much-needed technician courses it is beginning to set up. Soft covers, 194 pages.

Shortwave frequency list by C.J. Both. De Muiderkring, The Netherlands, ISBN 90-6082-289-7 (available in the UK direct from PC Publishing at £4.95). Frequency-by-frequency table of h.f. broadcasting in the range 2260-21810kHz, giving country of origin, station name and (where known) transmitter power. The impression made by the author's painstaking work is spoiled a little by the quaint language of the English introduction, which ought to have been translated better. Soft covers, 96 pages, reproduced from draft-quality dot matrix print-out. PC Publishing is at 22 Clifton Road, London N3 2AR, telephone 01-346 0627.

68020, 68030 microprocessors and their coprocessors by P. Jaulent, L. Baticle and P. Pillot; translated from the French by Aidan Loyns (Department of Computer Science, University of Manchester). Macmillan Computer Science Series. £12. Practical guide to these advanced devices, intended for students of computing and electronic engineering who have to design with them as part of their courses. Section headings include signals description, bus operation, addressing modes, new instructions, exception handling, cache memory, pipes, barrel shift register and virtual memory. All three authors are concerned with microprocessor training in a French i.t. company. Soft covers, 205 pages.

An introduction to satellite television by F.A. Wilson. Bernard Babani, £5.95. A good deal of this book is taken up with material not strictly relevant to the subject, as if the author wants to tell us all he knows rather than to stick rigidly to his task. Much of the first half of his text is taken up in describing the SI units of measurement, the atom, the nature of radio waves, television basics and even the principles of rocketry. Mysteriously, Ariane and Arianespace are mis-spelled

TELECOMMS TOPICS

MPT 1327 for Europe?

The UK MPT 1327 trunked radio signalling protocol could be employed in other countries of Europe now that the French Ministry of Posts and Telecommunications has declared its intentions to license both public and private trunked mobile radio systems. Moves are also taking place in West Germany towards the licensing of public systems.

Band Three Radio Ltd has been operating a public trunked radio system in the UK since last October using MPT 1327. This protocol is being contemplated for one or other of the French networks. If adopted, it will put pressure on Germany to achieve "contiguity". Furthermore, if frequency allocations are sensibly the same in all countries, manufacturing economies of scale could be obtained.

By 1992, the date for a European common market, networks could be linked. This would permit roaming and allow contact to be maintained with bases in another country.

According to Andrew Robb, Band Three's managing director, his company has no European ambitions. It is looking to international traffic i.e. roaming, but not to international subscribers. Well-established formulae exist to handle the splitting of tariffs.

Government Data Network

Racal-Scicon, a wholly-owned subsidiary of Racal Electronics, has been selected to build and operate the Government Data Network (GDN) – Europe's largest private data network. Racal estimates that this business, together with other network services contracts, will be worth more than £1G over the next 10 years.

GDN is a pioneering project initiated by four Government departments and the Central Computer and Telecommunications Agency (CCTA). It is intended ultimately to handle most of the Government's civil data communications traffic on one low-cost, high-efficiency secure system. Racal-Scicon will finance, build, operate, manage and maintain the UK-wide network while the Government will only pay as capacity is used on the system, saving the initial capital outlay otherwise needed for network infrastructure.

Initially, four Government departments – the Department of Health and Social Security, HM Customs and Excise, the Home Office and Inland Revenue – have committed to join the GDN service, with other departments expected to switch over to the network as communications demands rise.

Initially it will serve some 85 000 terminals at more than 4000 Government locations. The system will employ packet switching to international standards and will incorporate high levels of in-built security. Individual departments will be prevented from obtaining unauthorized access to each other's data.

BT&D sampling at 2.4Gbit/s

BT&D Technologies, the British Telecom and Du Pont joint venture, has developed high-performance components for optical communications systems and test gear such as optical time domain reflectometers (t.d.rs) capable of working at 2.4Gbits/s.

The transmitter is a distributed feedback laser with a narrow spectral width of 0.1 nanometers, developed by British Telecom's research laboratories at Martlesham. It may be modulated up to 2.4Gbit/s over a wide temperature range and it provides 1mW of optical output. The source is based on InGaAsP buried heterostructure technology and is fabricated using BT&D's proprietary version of the metallo-organic vapour phase epitaxy process for high reliability.

The receivers are InGaAsP/InP planar avalanche photodiodes. Offering high responsivity at 1.3 and 1.55 microns, the devices feature a guard ring stucture to produce a high signal to noise ratio. The structure provides low multiplied dark currents of less than 1nA at room temperature and gain-bandwidth suitable for high performance operation at speeds up to 2.4Gbit/s.

Competition in public payphones

Mercury Communications has placed an initial order with GEC Plessey Telecommunications (GPT) for telephones which will accept various methods of payment for use in its public payphone service. Another company, International Payphones Ltd (IPL) plans to install 49 000 public payphones over the next five years.

The Mercury service will be launched later this year and the company has stated that it will introduce a service which accepts a range of payment methods which will provide customers with a flexible, modern, high quality, reliable service.

It is believed that the initial order from GPT is for card-only machines but subsequent units will allow coins to be used.

Operating from eight regional centres throughout the British Isles, IPL claims that it will maintain a level of working payphones hitherto never experienced in Britain. Not being tied to either BT or Mercury, it will be in a strong position to purchase capacity competitively to the advantage of both itself and its customers.

DMC sets up in Scotland

Digital Microwave Corporation, a leading manufacturer of high performance short-haul communications systems, has opened a British subsidiary, DMC Telecom UK Ltd, in East Kilbride, Scotland to capitalize on substantial sales in the UK and Northern European communications markets. Using thin film microwave integrated circuits operating at 18 and 23GHz, DMC claims to be a pioneer in the use of GaAs fets, instead of Gunn diodes, in its amplifiers.

The parent company was formed in 1984 with the objective of taking advantage of the swing towards digital systems. While there was a proliferation of digital customer premises equipment (e.g. digital p.a.b.xs), the short-haul connection for the "last mile" was missing.

DMC won its first major UK contract, with Mercury Communications, in October 1985. Now the two companies have signed a two-year master purchasing agreement. The minimum value of the first year's procurement is expected to be in excess of $18 million with releases to date totalling $11 million for microwave and fibre optic equipment.

According to Ted Stocker, managing director of the newly-formed company, British Telecom could become a major user of DMC systems, its potential being at least ten times that of Mercury. In addition, "the UK forms the springboard for the rest of Europe".

Orbitel looking abroad

Orbitel Mobile Communications, the Plessey and Racal joint venture, and Matra Communication SA of France have entered into an agreement regarding the development and marketing of network equipment for pan-European digital telephone systems.

Orbitel also confirmed that it has now submitted proposals to operators in a number of European countries to supply digital cellular equipment, ranging from validation systems to operational networks.

Mike Pinches, Orbitel's managing director, said: "Our agreement with Matra Communication is complementary to the one we have with Ericsson announced last October. This latest development enables us to present the pan-European network operators with a powerful grouping of companies which lead the field in mobile communications".

Start of Scandinavian link

The UK-Denmark 4 undersea cable got under way when the UK coast section of this £32 million system was successfully brought ashore at Filey in Yorkshire. The system will provide the first direct signal cable link between

TELECOMMS TOPICS

Scandinavia and the UK, doubling existing cable capacity.

The system will be jointly owned by British Telecom and the telecommunications administration in Denmark, Finland, Norway and Sweden. It will provide Scandinavia's link, via BT, into TAT-8, the first transatlantic optical fibre cable, due to be completed later this year.

UK-Denmark 4 contains four single-mode fibres operating at a wavelength of 1300nm. Each fibre pair will operate at 280Mbit/s, the equivalent of 3840 telephone circuits. The complete system will incorporate 11 undersea repeaters spaced approximately 56km apart.

Opto link to France

British Telecom, France Telecom and Mercury Communications have signed an agreement to provide the first optical-fibre submarine cable system between UK and France. The system, due to be in service in early 1989, will be supplied by the French company Submarcom.

When it opens it will add direct optical fibre links to France to those already provided by BT via its UK-Belgium cable, put into service in July 1987.

Telecomms Topics is compiled by Adrian Morant.

Towards i.s.d.n.

I.s.d.n. the integrated services digital network, is the long-term goal being striven for by telecommunication authorities all over the world. Many countries are moving from a pilot service and are now starting to offer a commercial service. But what is i.s.d.n.? Or really, what will it be?

When fully implemented it will be a universal digital network that will be used to deliver telecommunication services, be they voice, data or image. At present, for example, the telex network is different from the p.s.t.n., the public switched telephone network. In addition, being digital, it will offer significant improvements in transmission quality together with a wide range of additional features.

It will enable network operators to achieve economies of scale because they will no longer need separate networks for separate services. In addition, both they and users will have the infrastructure necessary to allow new and innovative services to be introduced without delay.

It is, however, a long uphill struggle extending at least to the end of the century to make i.s.d.n. universally available. Not only must the digitalization of the whole network have been completed, this conversion must have been completed in an appropriate manner right through to the subscriber's premises.

BT is moving ahead rapidly with the modernization of its network. All 53 digital trunk exchanges are now operational and 60 percent of originating trunk traffic has been loaded on to the digital trunk network. BT is not dragging its heels. According to data prepared by CEPT (the European Conference of Posts and Telecommunications), 100 percent of UK traffic will be carried digitally by 1990 as compared with 75, 25 and 36 percent respectively for France, Germany and Italy.

This digital infrastructure, together with digital telephone exchanges, is a pre-requisite of i.s.d.n. However, even though nearly half of BT's subscribers will be connected to a suitable digital exchange by 1990, a large proportion of them, and in particular the domestic ones, will not be able to enjoy the advantages of i.s.d.n. This is because the necessary digital terminating equipment will not have been installed on their premises or in the corresponding locations in the telephone exchange. Thus, these subscribers will still have to use traditional analogue telephones.

What will occur is that signals from their telephones will travel, still in analogue form, to the exchange where they will be converted to digital form and transmitted via pulse code modulation through the network until they arrive at the called party's exchange. They will then be converted back to analogue form in the subscriber's line card prior to travelling the last few kilometres.

Nevertheless, there are underlying benefits for all subscribers in the digital network. These include greater inherent reliability and, by the use of d.t.m.f. (dual tone multi-frequency) signalling instead of pulse-dialling, much faster call set-up. In addition, the use of d.t.m.f. signalling allows easy access to computer-related services such as voice mail. These systems are command-oriented and thus the user needs some simple method of keying in the required command numbers. (Where d.t.m.f. phones are not available at present the user has to hold a d.t.m.f. tone generator over the phone mouthpiece.)

British Telecom introduced its IDA (integrated digital access) pilot service in 1985 prior to any internationally agreed i.s.d.n. standards. Consequently, its pilot service does not conform to the standard that was subsequently adopted. This should not be interpreted as BT being 'out of step' with all the other countries; rather that it took a lead instead of just sitting on the fence.

Before the end of this year BT will be starting to provide a commercial i.s.d.n. – still known as IDA – and will expand it as rapidly as possible. It will, however, not withdraw support from early users who committed themselves to the interim 80kbit/s service. However, it is to be expected that those forward-looking organizations which originally embarked on this service will decide to migrate to the full standard as soon as possible.

USING I.S.D.N.

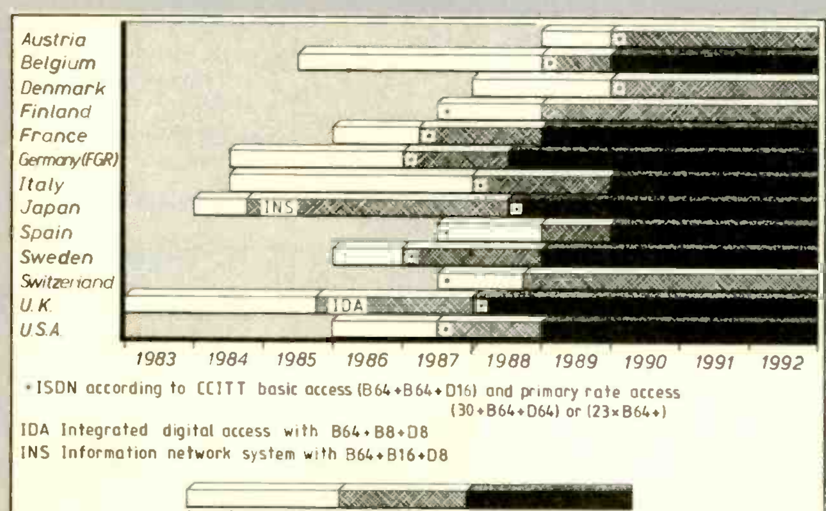
I.s.d.n. will be offered as a 144kbit/s Basic Rate Access (BRA). This, otherwise known as single line access, will provide two 64kbit/s "B" channels for voice or data plus the 16kbit/s "D" channel for signalling and lower speed data. While the majority of domestic subscribers will have no use for the additional capacity that this provides as we move, albeit slowly, into the information age, business users will want to enjoy the benefits of the higher quality and additional facilities that it will support.

For example, even the smallest business will rapidly come to appreciate the convenience of 64kbit/s transmission speed for electronic mail and other computer-delivered services as compared to the 1200bit/s or so widely used today.

While domestic and small business users will use BRA, connections to p.a.b.xs will use Primary Rate (otherwise multiline) Access. In Europe and most countries of the world this consists of "30B+D" on a 2Mbit/s digital trunk. In the USA and Japan, where the digital transmission "T1" standard is 1.544Mbit/s, the equivalent is "23B+D".

Private networks, where the p.a.b.xs at each of a company's sites are interconnected, will be able to install i.s.d.n.-compatible terminal devices in the appropriate places within their organizations. After all, the strength of a chain is that of its weakest link. Consequently, the most sophisticated i.s.d.n. terminal device is reduced to the lowest common denominator (if it will operate at all) if the receiving end is not suitably equipped.

This is a vital aspect. Today, a telephone in one part of the world can connect through to any other no matter where it is. Similarly, as and when i.s.d.n. rolls out, inter-working must continue.



Measuring by ultrasound

Using ultrasonics for the measurement of gas flow

R.J. REDDING

Many measurements in industry and science are based on beams and wave motion. Radio and light beams hold sway for surveying and navigation, and movement is often best detected by the Doppler shift. We control aircraft and guide space craft, but at the domestic level control and measurement poses problems, possibly caused by the nature of electromagnetic radiation. Sound waves, which are almost a million times slower, are more appropriate.

The application of sound as a scientific measuring tool seems open to further development in the practical, everyday sphere and has much to commend it. It does not have the aura of danger possessed by nucleonics and lasers and, if confined to the ultrasonic region, is non-intrusive. The range of frequencies available for use is from a few tens of kilohertz to gigahertz, where the acoustic microscope out-performs the optical type.

One reason for the unpopularity of sound for measurement purposes is that the attenuation varies widely, roughly as the square of distance and as the square of the frequency. Further, the speed of sound changes greatly between gases, solids and liquids and hence is much less dependable than electromagnetic waves. On the other hand, it is easy to use comparator systems to show changes in composition, temperature or pressure, by a built-in reference or sample.

Perhaps the biggest impediments to the use of sound are the confusing effects of resonance, standing waves and reverberation that can occur. Large, low-frequency amplitudes can build up in structures with dramatic results!

This explains why almost all ultrasonic measurement and imaging is done on an intermittent or "pulse-echo" system, by a band of frequencies or a form of sharp-edged pulse: one endeavours to read the returned signal from some distant interface. Such "time-of-flight" sonar is the basis of distance imaging and flow measuring techniques and, whilst continuous-wave measurement is inherently superior, it is undeveloped at present.

This article suggests that pulse-echo ultrasound is on a par with "spark" radio transmitters and that the techniques and components we now use are directly applicable to sound waves to provide much-needed digital measurement systems for industrial and domestic purposes. Some techniques, frequency modulation for example, seem particularly applicable to sound waves because the attenuation varies as the square of the frequency.

A POTTED HISTORY OF CONTROL

In the late 1940s there was a move to apply servo-control to the automatic control of process plants. Originally, this used hydraulic and pneumatic power but, as a young electrical instrument engineer, I felt that electronics must be superior and joined a company that pioneered the use of electronic process control. This involves the risk of fire and explosion from electric sparks and led me to specialize in intrinsically safe design. Essentially, this means keeping the energy level so low that any sparking is innocuous. This was a major headache in the early days (and still is in some traditional industries), but electronic engineers have learnt that the lower the energy level, the better in many ways. Now it can be said that miniaturization and integration results from reducing the energy level and heating effects in the electronic circuitry. The blessing to me has been the improvement in reliability from eliminating the mechanical bugs!

However, the performance of control equipment is entirely dependent on the quality of the input, and it is *measurement* that determines the performance of any control system. Here again, the meaning of quality has changed with time, since accurancy, which takes seconds to acquire, is useless to control a plant; sometimes, all we really need is to know quickly when something is changed and in what direction.

A control system endeavours to counteract any disturbances, either intentional instructions or ambient or random input changes. The aim is to defeat time delays within the plant, so the essence of control is to detect that something has changed and to continuously counteract such changes. The performance is therefore related to how sensitively we can measure and how fast we can get the result into a form we can use.

MEASUREMENTS AND TRANSDUCERS

Traditional measurements provide an analogue output and one can use a transducer to turn such a movement into an electrical signal. The standard signal in process control is a current of 4-20mA d.c. (corresponding to the earlier, pneumatic 3-50 p.s.i.) and to this day the bulk of electronic control equipment in computer-controlled plants uses such signals, to represent flow, pressure, temperature as the input information. Hence the vital links between the plant and the solid-state control equipment are analogue-to-digital converters.

Many measuring systems now give an electrical output, for example temperature sensors and pH monitors. Modern flow-measuring systems give a digital output in terms of frequency, but there is still a tendency to convert these back to analogue 4-20 mA to conform with standard practice.

There has always been a few stalwarts extolling the use of frequency signals, but invariably when such instruments have been produced they have not caught on against the "industry standard" analogue signals. The position is now changing because of the accent on information technology.

The purpose of this article is to show how frequency signals for process measurements can be easily obtained without physical transducing; therefore without the mechanical imperfections that make analogue measurement a slow, intrusive representation of the information we desire.

GAS DETECTION IN THE NORTH SEA

In the 1970s, the oil and gas installation in the North Sea stretched engineering practice and the design of instrumentation was crucial to the protection of personnel from fire and explosion hazards. Not only had the equipment to withstand the harsh climate, but any electrical equipment had to be protected against the explosion hazard: flame-proof enclosure was not always convenient, for example on the smoke detectors for the fire alarm system! I became involved in making such equipment intrinsically safe and reducing the power level from kilowatts down to a few milliamps at low voltage.

One intractable problem area was gas detection. There may be thousands of detectors, each comprising a hot wire, electrically heated so that any gas in the atmosphere would be oxidised on it, raising its temperature and so indicating its presence. These had to work even after power had been shut down, so the battery and wiring of the system was horrific. An incautious remark led to a challenge to do something better.

I felt we needed a beam system to detect change anywhere in the atmosphere and settled on a sound wave as the most innocuous and simple for the purpose (later, lasers were used, but have since gone into a decline). The trouble with sound waves was reflection and the effect of standing waves. The principle used was that of the organ pipe, i.e. the note changes with the humidity, etc. The distance between a microphone and loudspeaker determines the frequency at which the air path will resonate, but any changes in the density of the air will show as a change in this frequency. A series of parallel microphone-and loudspeaker paths covering the area of an oil rig could show when anything fresh happened anywhere in that volume of space, and in general we are looking for instrusion by lighter-than-air gases.

To avoid the nuisance of audible sound and the known effects of acoustic feedback, etc. I tried modulating an ultrasound beam. The work was being carried out in a "radio shack" with the chatter of a two-metre f.m. repeater as background. Suddently, I realized the special properties of f.m. transmission should be equally applicable to a sound wave, and a direct answer to the problem of multiple paths and reflections.

By employing a high carrier frequency, the beam becomes narrower and directional, and the signal-capture feature of detectors further helps in masking everything that is 3dB below the intended signal path. Further, the standard v.h.f. chips are directly usable, and in fact the system looks like a v.h.f. transceiver for speech in which the aerials are replaced by piezoelectric transducers to convert the electric wave into the mechanical vibrations of sound.

By 1978 patents had been granted in the UK and the USA, and these showed that the use of frequency modulation on an ultrasonic carrier was novel, even if not unmarketable. I went to the USA, intent on selling or dropping the idea at the Instrument Society of America's annual show in Philadelphia. I choose a suitable company which faced the problem and also had a strong interest in gas detection, but the manager of the stand was preoccupied with a flowmeter leaking water on the floor of the stand. I remarked that it would be safer to use air instead, and he said "That's an ultrasonic one and they won't work on air". I realised that flow measurement was a better proposition and quite quickly made a deal with an old friend. Unfortunately his company was in the process of a patent battle involving ultrasound for detecting vortices for flow measurement. Though we made progress for a while, my insistence that I had a novel measurement and nothing to do with vortex shedding led to a rift. However, by that time separate patent applications detailing the specialities of flow measurement were well advanced in the USA and in Europe, so the theme lived on.

It had become clear that I had a basic transducer system which, having no moving or physical parts, obviated the hysteresis and intrusion by which traditional transducing devices are rated. I believe that inventors should stick to simple mousetraps and not invent novel rodent exterminating systems, but radical and unorthodox ideas can be difficult to get published. Academics don't want to revise their lecture notes, and industrialists feel unsure unless they have a mathematical backup from some learned organisation, so the best hope is – DIY!

However, I also believe that "what isn't there can't go wrong," and since the only possible mechanical interface to cause trouble was the crystal itself, I felt this must be better than gears, levers and bellows. I therefore proceeded with the development of an idea which now looks promising, namely, an electronic gasmeter.

The principle of the domestic gas meter has been virtually unchanged for well over 100 years and performs well as a dispenser, but has many practical disadvantages today. After years of internal research, British Gas PLC in 1987 presented industry with the problem of evolving a modern gas meter. Without going into detail, I give below an outline of one of the proposals that has just been accepted for proceeding to a "proof of concept" stage. Such a development takes at least five years and I hope there will be earlier usage in other areas, for example in the measurement of mass air flow for cars and fuel/air ratio for combustion purposes.

THE LIMITATIONS OF SONAR AND PULSE ECHO OPERATION

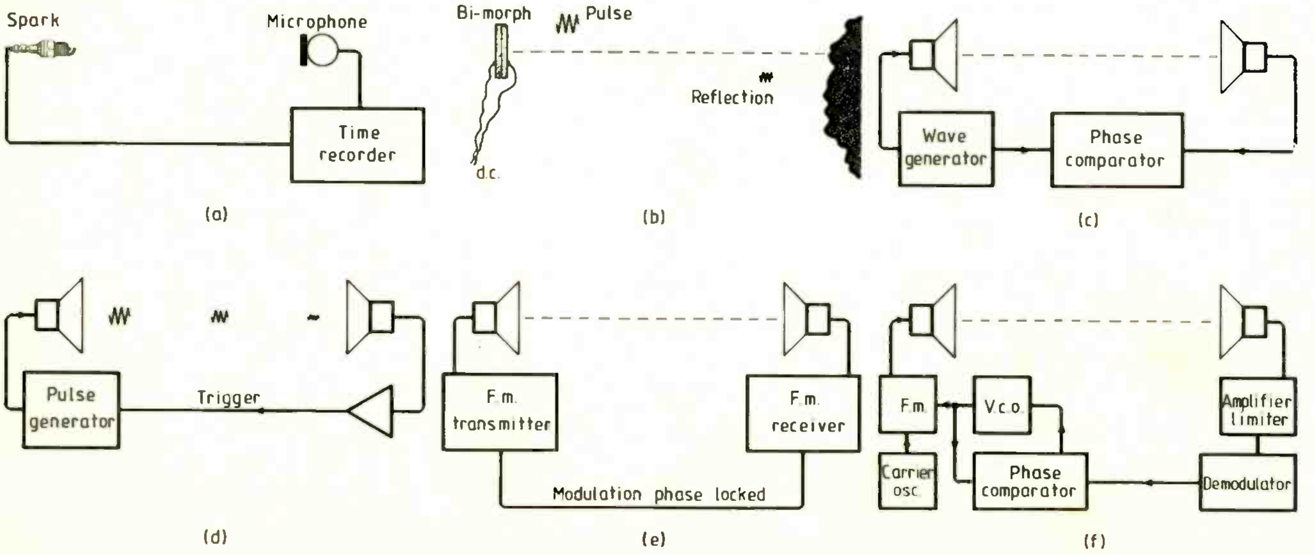
Traditional measurement by sound uses a sharp pulse front and endeavours to measure the time interval until its echo is received, usually by the same transducer. The main limitation to performance is the attenuation of sound, which is high in the case of air. In particular, the attenuation of the sound wave varies roughly as the square of the frequency. As a result, only the lower frequencies get through and the received pulse front is rounded, timing becoming indefinite.

There are many practical tricks to improve the performance, such as resonating the crystal at a particular frequency, so that a pulse train is transmitted. One can also work on one of the later cycles of a pulse train or even measure the phase of the sent and received train. Thus, virtually all the technology is concentrated the resonant design of the piezo ceramic transducer, particularly if this is used for both transmitting and receiving.

The sequence of change from an intermittent to a continuous operation system is perhaps best shown succinctly in the 10 year old diagram Fig.1. One uses the highest frequency that will maintain a signal along the path and modulates it with the phase-locked loop so that the difference between the ends of the path is kept constant. This means that the frequency in the path is a very sensitive and continuous measure of the transit time. Further, because it is a frequency, it is independent of the speed of sound in the medium. The significance of this is that if one has beams in opposite directions, then the frequency will be the same in the absence of movement. If the fluid moves, then the velocity is turned into an electrical signal equalling 2Hz m/s irrespective of all other considerations. Therefore, it is a fundamental method of turning movement into frequency and hence its significance for flow measurement.

It is by no means limited to flow measurement, being in effect a comparator system, where if one has a sample, or a known reference, then the system can provide accuracy in terms of that known value, and the quality of the measurement is a function

Fig.1. Sequence of change from an intermittent pulse system to one using a continuous train of pulses. At (a) the basic, one-way timing method is shown, while (b) is the pulse-echo "sonar" system. Shown at (c) is a singaround measurement and at (d) a pulse repetition rate system. The system at (e) uses f.m. and the final COHMOD (coherent modulation) method is seen at (f).



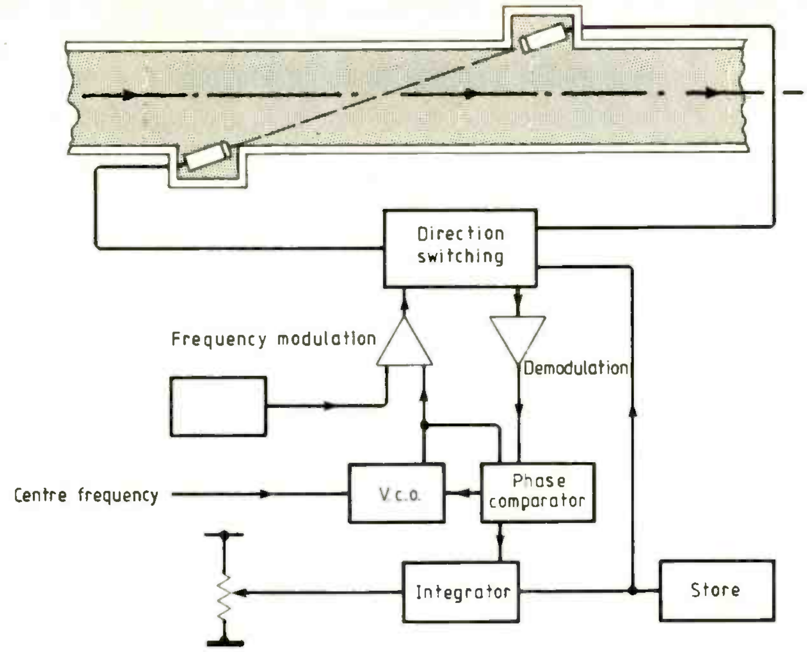


Fig.2 Flow measurement by the coherent modulation method.

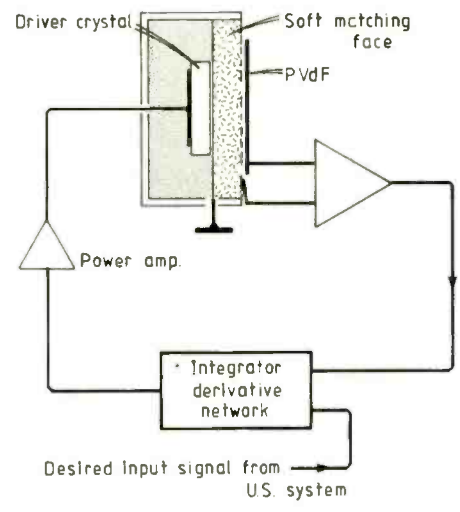


Fig.3. Broadband feedback transducer.

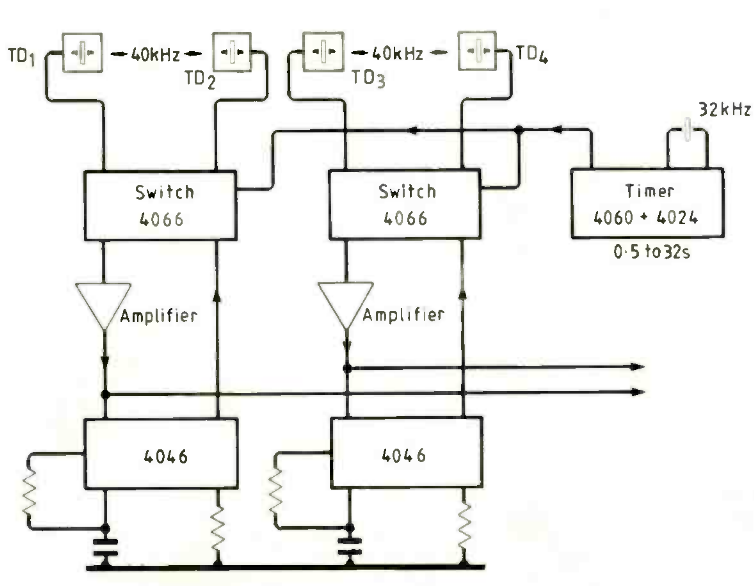


Fig.4. Proposed wind-speed meter.

of the ingenuity with which the frequency measuring system is applied.

The elegance of a frequency as a signal instead of the usual 4-20 mA d.c. analogue signals and d-to-a converters, etc., has long been recognised but has been difficult to implement because of the need to conform to industry standards. However, the advent of IT and the use of so-called smart transducers using digital techniques to overcome the basic limitations of analogue measurement is now such that a move to frequency signals seems inevitable. The fact that the cost of cabling and wiring is now a very large part of industrial process control makes the move towards frequency operation and eventually to radio use even more pertinent.

THE DESIGN OF COHMOD MEASUREMENT SYSTEMS

Electronic circuits for the COHMOD principle can follow radio, digital and analogue practice with little difference in performance. The main problem is invariably the transducer itself or rather its linearity in translating an electric signal into mechanical vibrations. The majority of previous ultrasound work used pulse-echo techniques and hence resonance techniques have enhanced the performance. Although these can be used over narrow bandwidths, the true operation of f.m. requires a linear bandwidth of at least a few per cent of the carrier frequency. The sensitivity of the COHMOD system is many times higher since it is not influenced by the amplitude of the signal. We only need a signal of the order of a microvolt to give a fully limiting f.m. signal. Consequently, the operating frequency is 10-100 times higher than would be practicable with pulse operation and herein lies the clue to the performance of the system.

Thus the design philosophy of the system, shown in Fig.2, is easily stated.

1. Select the path to be measured and determined the highest frequency which will give a received signal of the order of 10 microvolts.
2. The length of the measured path and the speed of sound in the medium concerned determines the COHMOD resonance frequency. The working frequency can be a fraction or multiples of this.
3. The deviation should be not less than the COHMOD resonance frequency and preferably many times more; 5% of the carrier frequency would seem ideal.

It is the bandwidth of the transducer which is the vital point, since one must keep the deviation within the linear range, otherwise spurious products and particularly lower-frequency, minor-mode vibrations will occur in the medium and result in the reverberations and standing waves at frequencies not present in the electronics!

THE PRESENT COMMERCIAL POSITION

There are many transducers available for remote control and intruder detection in the range of 25-75kHz, but these are highly resonant and cannot be frequency modulated over a significant range. Hence, their use is fraught with difficulty.

A few transducers designed for industrial proximity purposes operate around 200kHz and employ a soft matching face to efficiently communicate into air. Such units have been used with success for flow measurements in pipes of several inches diameter. The only units known to work at higher frequencies, says 1MHz, are specially made in Japan for robotic purposes and are very expensive. For liquids and solids, of course, much higher frequencies and direct contact is possible. Units designed for pulse operation will operate with the continuous wave circuitry, but the performance improves greatly when the frequency can be increased by a factor of at least ten.

There is, therefore, a chicken-and-egg situation which requires a large mass market to cause the production of transducers in the range of 1MHz and matching into gases. A new plastics material, polyvinyl dichloride (PVdF), is ideal for the purpose, but the know-how of manufacture is lacking or jealously guarded, and it is hoped that the British Gas meter initiative will result in some positive move.

A servo transducer has been mooted, using the "fly-by-wire" philosophy as shown in Fig.3. An amplifier drives the crystal so that the output measured by the PVdF film makes the "demand".

MEASURING GAS AND WIND WITH 40KHZ

To break the impasse on the supply of transducers, a colleague, M.H. Miessler, attempted to use the 40kHz units which are very cheaply available. By using digital filter techniques, we avoid some of the problems. This resulted in a demonstration gas meter which showed promise of economy and low energy consumption, both of which are of vital importance to be domestic gas meter.

The carrier frequency plays no part in the COHMOD system and can vary widely without significant effect, provided the carrier is much higher than the modulation frequency to avoid quantization effects. Therefore, we can move the carrier frequency and keep the number of actual cycles within the path constant over a small range. By exploiting the resonant properties of the 40kHz transducer and the limited range required in a gas meter, it is shown practicable to make such a unit. In the analogue form of the circuit the power consumption is extremely low, e.g. 1mA at 5V d.c.

A DEMONSTRATION

As an illustration of the principle in another application, Fig.4 shows a possible arrangement for a wind-speed indicator, using available components.

The unit is, in effect, two flow meters operating in the open air at right angles, with direction switching by means of an analogue switch 4066. It measures the wind velocity in two directions at right-angles. How one turns this into a display or utilizes it when sailing a boat, or to give the wind effect of wind on a microlite aircraft is up to the ingenuity of the experimenter. Pythagoras chips are available from Plessey but, at the moment, the price is prohibitive.

ITT satellite chips for BSB

British Satellite Broadcasting, the company which is to provide a direct satellite television service for the IBA, has placed an order with ITT Semiconductors for four million DMAC chip-sets. These components will form the basis of decoders for the complex DMAC transmission format in which BSB's programmes will be transmitted.

The chip-set, consisting of the DMA2280 decoder i.c. and the DMA2285 descrambler, will give access to the four programme services to be carried on BSB's satellite. Prototypes of the chips are to be made available to BSB in the autumn, with bulk production following next spring. This timetable should enable the manufacturers nominated by BSB to produce receivers in large numbers ready for the first programmes: the three-channel Hughes HS376 satellite is due for launching in August 1989. The ITT chips, in 1.5μm c-mos technology, will be housed in 68 pin p.l.c.c. packages.

DMAC, the transmission standard to be used for the new services, was developed by the Independent Broadcasting Authority. It provides a component-coded vision signal (YUV) for high-quality picture reception free from the crawling patterns to which present day systems are prone, plus digital stereo sound and extensive data capacity for teletext and related services, and an easy upgrade path to E-MAC high-definition television. D.b.s. programmes from the BT Vision-Maxwell-W.H. Smith consortium will also be transmitted in DMAC; but those from Rupert Murdoch's Sky Television, via the Astra satellite, will be in PAL.

A descrambler will be needed for BSB's programmes because the company has decided to transmit even its advertising-supported services in encrypted form: UK viewers will not be asked to pay to receive these programmes (only the *Screen* channel, specializing in cinema films, will involve a subscription), but the system enables BSB to save money by buying only the UK transmission rights.

The other European d.b.s. standard, D2MAC, is tackled by ITT with a decoder in a single chip. D2MAC, a cut-down version of DMAC with reduced data and sound capacity, is favoured by French and German interests because its restricted bandwith is compatible with their existing cable television networks. But the private venture Astra satellite, expected to begin a service around Christmas, could end up carrying services in both MAC formats. Receivers may therefore need to have multi-standard decoders. However, even with all three MAC chips fitted, decoders using the ITT devices look as though they could be significantly less complex to manufacture than those with the rival Plessey-Philips chip-set (described in the May issue, pages 504-505).

ITT's D2MAC decoder i.c., DMA2270, is designed for integration into the company's Digit 2000 digital receiver system, but with suitable analogue-digital conversion could be used in any receiver chassis.

The decoder is able to treat different sound services automatically by decoding the address field of the packet header. Up to eight different sound channels are available for each television service. The sound processor section converts all types of sound packets into a sequence of 14-bit samples. Medium-quality channels are converted up to the 32kHz sampling frequency of the high-quality channels, so that subsequent stages deal with a single data format. Storage capacity for buffering the sound packages during processing is provided by an external 64K d-ram.

One packet address is reserved for service and network identification data. This information is protected by a c.r.c. code and by repetition. Up to 720 bits of packet 0 data can be buffered within the i.c. and can be read for processing by an external controller through a three-line serial bus.

Further information is available from ITT Semiconductors, 145-147 Ewell Road, Surbiton, Surrey KT6 6AW. Other new chips announced at the same time by ITT are the TPU2734 single-chip teletext processor, which now includes a Fastext capability, and the PIP2250 picture-in-picture processor. This overlays a secondary, one-third size picture on to the main television picture.

SATELLITE SYSTEMS

Data relay satellite

When NASA's space shuttle gets back into service – possibly in August this year – its first task will be to launch a tracking and data relay satellite owned by the American company Spacecom. The TDRS, or 'Tea-dress' as it's known in the trade, will first be taken into low Earth orbit. Here the doors of the shuttle orbiter's payload bay will open and the satellite will be ejected by a mechanical arm. A booster rocket attached to the TDRS will be fired and will propel the satellite from its low altitude into a geostationary orbit.

This spacecraft, called TDRS-C, is the second in a system of data relay satellites which Spacecom is leasing as a service to NASA. TDRS-A was launched in April 1983, but TDRS-B was lost in the Challenger disaster of January 1986. The main purpose of the whole system is to provide better and cheaper communication with the many low Earth orbiting (LEO) satellites which hitherto have been working to ground stations.

Since the LEO satellites typically have an orbital period of about 100 minutes they pass overhead quite rapidly and so need an extensive chain of tracking ground stations around the globe to keep in contact with them. NASA's existing ground station network is now over 20 years old and due for renewal. The cost of re-equipping this ground network would be considerable, so the TDRS system has been adopted as a cheaper alternative.

Thus the geostationary TDRS spacecraft 'look down' on the LEO satellites, and because of their advantageous positions in space can see them for much longer periods than is possible from Earth stations in a ground tracking network. There is just one Earth station for the whole TDRS system, at White Sands, New Mexico, USA, and this handles all the data communications, including text and graphics, between the LEO satellites and their respective mission control centres. Altogether the system, developed by TRW Space Communications, can deal with up to 2400 LEO satellite passes a day, and with data rates up to 300Mbit/s.

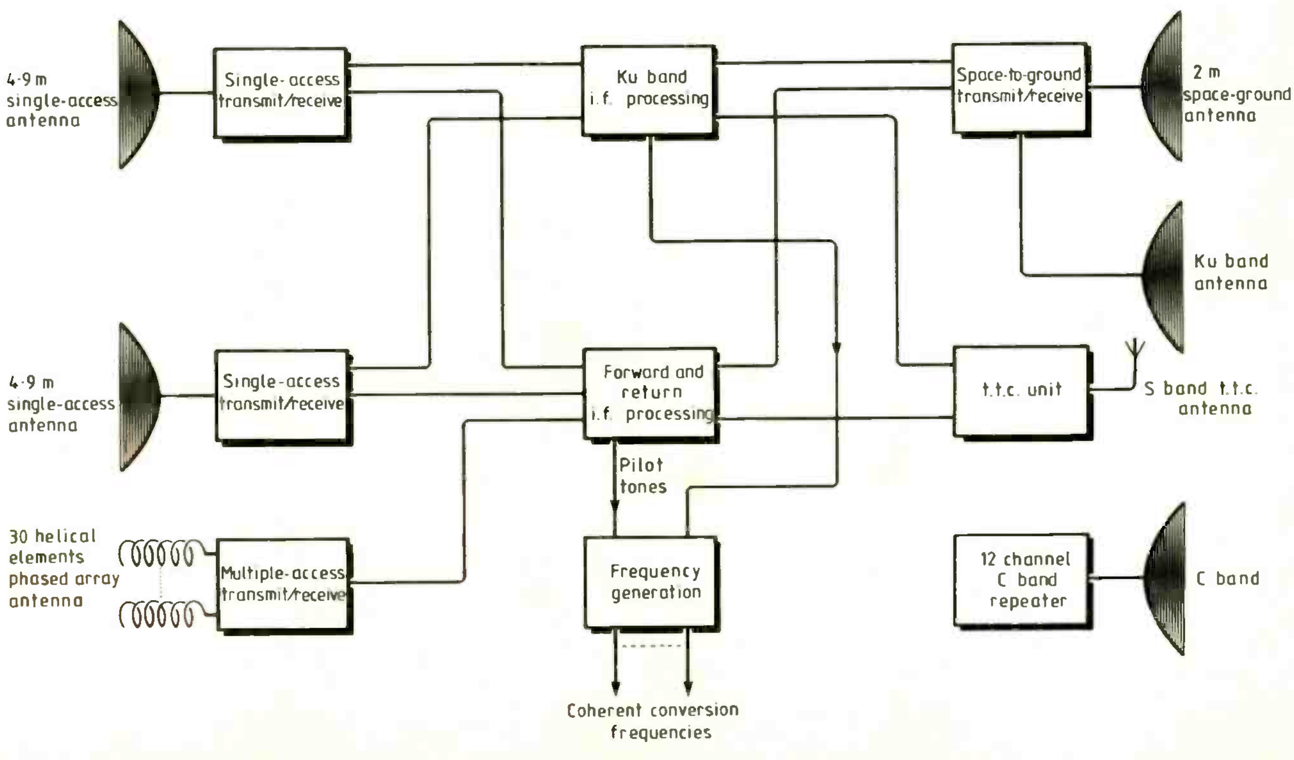
So each TDRS must be designed to relay data to and from many user satellites. In fact the TDRS-C can serve up to 32 spacecraft simulaneously, including the shuttle orbiter itself. This entails two-way radiocommunication, multiple frequencies and multiple antenna beams. The accompanying block diagram of the TRW communications payload gives an outline of how the relay system is arranged. Altogether the satellite carries seven antennas and operates in three frequency bands, S, C and Ku.

There are two large antennas, with main reflectors of 4.9m diameter, designed for single-access working with the user satellites. These big reflectors fold up like umbrellas for launching in the shuttle and are opened when the TDRS gets into orbit. A phased-array antenna of 30 helical elements forms and steers beams for up to 20 multiple-access users. The fourth and fifth antennas are for C- and Ku-band communications respectively.

Tracking, telemetry and command signals are handled by an S-band antenna, while the TDRS link with the White Sands earth station is provided by the seventh antenna, which has a two-metre reflector and works at Ku-band frequencies (downlink 13–14GHz, uplink 14–15GHz). Because they handle the total data from a number of user satellites, these links with the ground must have large bandwidths to cope with the overall data rate – actually 650MHz for the downlink and 625MHz for the uplink.

When the TDRS-C is deployed in space it measures 17.3m from tip to tip of its two solar arrays. On the ground the spacecraft weighs 2130kg. It has an expected operational life of ten years.

The European Space Agency has plans for setting up a data relay satellite system for its own LEO operations. This will have two spacecraft in geostationary orbit, each capable of relaying data continuously to and from user satellites for more than half of each low Earth orbit.

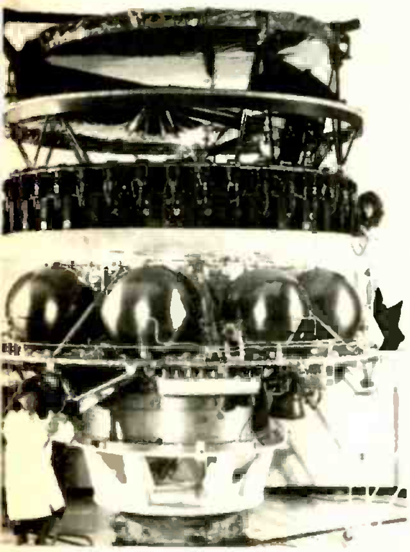


System for relaying data to and from user satellites, in the communications payload of the TDRS-C multi-beam, multi-frequency tracking and data relay spacecraft.

Radio telescope baseline in space

One of the most successful radio astronomy techniques for locating and measuring emissions from radio stars has been the interferometer array formed by spaced receiving antennas. The late Sir Martin Ryle (who eventually became Astronomer Royal) did extensive mapping of cosmic radio sources with this technique at Cambridge University in the late 1940s and early 1950s. He used very simple horizontal dipoles laid out in a field and war surplus radar equipment

SATELLITE SYSTEMS



Thirty-two 27MHz transponders are carried in Japan's first commercial comsat, soon to be launched. The t.w.ts of these 20W transponders can be seen level with the head of the upper technician standing on a platform. Built by Hughes, the HS393 Ku-band spin-stabilized satellite has an antenna with a 2.4m main reflector and multiple-horn feed that will give a shaped beam to cover the four Japanese main islands and Okinawa island with a high e.i.r.p. of 50dBW in the most densely populated areas. Frequency re-use is obtained by polarization diversity. The antenna system includes two offset reflectors, one sensitive to vertical polarization and the other to horizontal polarization. Also, the 32-channel repeater system actually consists of two 16-channel repeater sections, one for each direction of polarization.

Hughes are building two of these HS393 spacecraft for Japan Communications Satellite Company, a joint venture between themselves and two Japanese partners, C. Itoh and Mitsui. When deployed in geostationary orbit, with antenna reflector and cylindrical solar arrays fully extended, the 3.7m diameter satellite will be 10m high. Power from the two cylindrical solar arrays is in excess of 2kW. The HS393 is similar to the HS376 to be used for Britain's d.b.s. service but very much bigger. It is expected to have a life of 10 years.

(see *Wireless World*, July 1951, pages 275-278). The heavens were scanned for radio sources by the rotation of the Earth, which moved the interference patterns of lobes and nulls across the sky.

Then in 1971 the Mullard Radio Astronomy Observatory was built near Cambridge and this used fixed and movable spaced paraboloid antennas to provide 16 interferometer pairs. These dishes can be programmed to track particular radio sources. Over the years a number of interferometer radio telescopes have been built around the world.

Since the resolving power of this technique rises with increasing distance between the spaced antennas, it makes sense nowadays to try and put one of the two antennas way out in space on a satellite. The result should be an angular resolution and radio image quality far superior to that obtained from Earth-based interferometers, where the maximum possible spacing is of course the Earth's diameter. This is the principle of a long-term ESA scientific project called Quasat (Quasar satellite).

As the name implies, one of its principal aims will be to study in greater detail the highly energetic radio sources in quasars (quasi-stellar objects). Originally Quasat was to have been a joint NASA-ESA project, but the Challenger space shuttle disaster put paid to all that because the satellite was planned to be launched by a shuttle. Now, ESA is preparing to go ahead alone, using the new Ariane-4 rocket to launch the spacecraft.

Essentially the Quasat spacecraft will be a 10m offset-fed paraboloid antenna orbiting the Earth in an elliptical path with an apogee of 36 000km, a perigee of 5000km and an inclination of 30°. Such a large dish in conventional construction could never be stowed in the nose of an Ariane rocket. It will therefore be an inflatable type, folded up for launching then blown up like a balloon and made rigid when in space. Observation frequencies will be mainly in the 22.21–22.5GHz, 4.8–5.0GHz and 1.66–1.67GHz radio astronomy allocations. A much lower frequency, 327MHz in another radio astronomy allocation, will be used for observing pulsars.

Emissions from the radio sources thus received will be sent as analogue signals through a downlink to a network of telemetry stations on the ground. In this ground system they will be recorded digitally on magnetic tape and transported to a central processing station, which will also get similar tapes from ground-based interferometer arrays that had simultaneously observed the same radio sources. An atomic clock will be used for synchronizing the two sets of signals. After correlation and calibration the resulting data will be sent to radio astronomers for further analysis.

Such observations should tell the astronomers more about the massive black holes which are considered to be at the heart of quasars, providing their energy by enormous gravitational force. They should also give information on the origin of the jets which convey power from the central objects at relativistic speeds.

So far, ESA has established that the Quasat project is technically feasible. An experiment using an American TDRS satellite (see item elsewhere) and ground-based radio telescopes in Japan and Australia has proved the principle. By the end of 1988 model spacecraft and payloads are expected to have been defined and cost estimates obtained. The next steps will be industrial system design and hardware development and testing. On present progress, Quasat could be launched some time in the period 1996 – 1997.

OTS-2 still working

The European experimental satellite launched in May 1978 as a test-bed and pre-operational spacecraft for the Eutelsat communications system is still in operation (see *WW* reports, July and December 1978). It is being used by the ESA to provide information for improving the design and operational techniques for the whole family of European comsats that have followed in its wake.

The experimental satellite was built for the ESA by a European group of firms headed by British Aerospace (Hawker Siddeley Dynamics) and including as major partners ANT, ERNO, MATRA, SAAB and SELENIA. Called the Orbital Test Satellite-2, it was in fact the second flight model. An OTS-1 was built but was lost in the first launch attempt in September 1977, when the NASA Delta launching rocket failed shortly after lift-off from Cape Canaveral, USA.

After its first year in orbit, when most of ESA's experimental objectives had been achieved, the OTS-2 communications capacity was handed over to Eutelsat to develop the services planned for the operational ECS satellites. ECS-5, the last in the series, is due to be launched soon.

Eutelsat continued to use the experimental spacecraft till 1984, when all traffic was transferred to the ECS system which had then become operational. Since then, OTS-2 has been kept working by the ESA for the purposes mentioned above.

Aeronautical satcoms nearer

Mobile communication services to aircraft through the Inmarsat system have been on the cards for a long time. The project has moved one more step nearer to reality now that the USA has formally accepted amendments to the Inmarsat convention and operating agreement that will allow this to happen. America is actually the 21st country to agree, out of the 54 member-countries in the international co-operative.

The planned range of aeronautical services, the first of which is due to come into operation on commercial airline flights later this year, will include cockpit data and voice communications, as well as direct-dial telephone services for passengers.

Satellite Systems is written by Tom Ivall.

Intelligent power devices

Recent developments in integrated circuits combining control circuitry and high-power driver stages.

SUE CAIN and RAY AMBROSE

While chips integrating both signal and power elements have been in use for several years, recent developments have greatly expanded the capabilities of these technologies. With the latest processes, designers can integrate many circuits that were previously uneconomic or simply impossible. Moreover, the enlarged horizons of 'intelligent' power technology and packaging are prompting new trends in the partitioning of systems.

Not only are intelligent power i.cs becoming more common, they are also becoming more intelligent, to the point where designers can aim to integrate a complete power subsystem. Moreover, the current and voltage capabilities of these technologies have increased dramatically, enlarging the field of applications.

Since systems designers are often responsible for partitioning electronic systems and specifying new devices, it is important for them to understand the capabilities of the latest technologies. This is now more true than ever, both because i.c. technology has advanced so rapidly and because the latest generation of power i.cs have a much greater 'system' content.

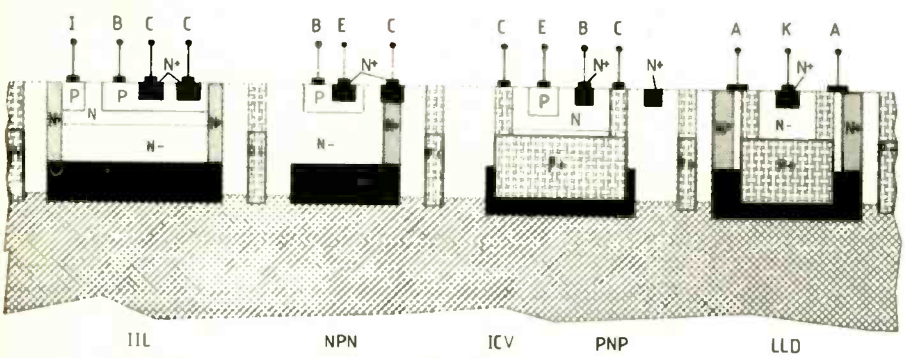


Fig.1. The SGS 60V bipolar process combines linear, logic, isolated-collector vertical p-n-p power transistors and low leakage diodes.

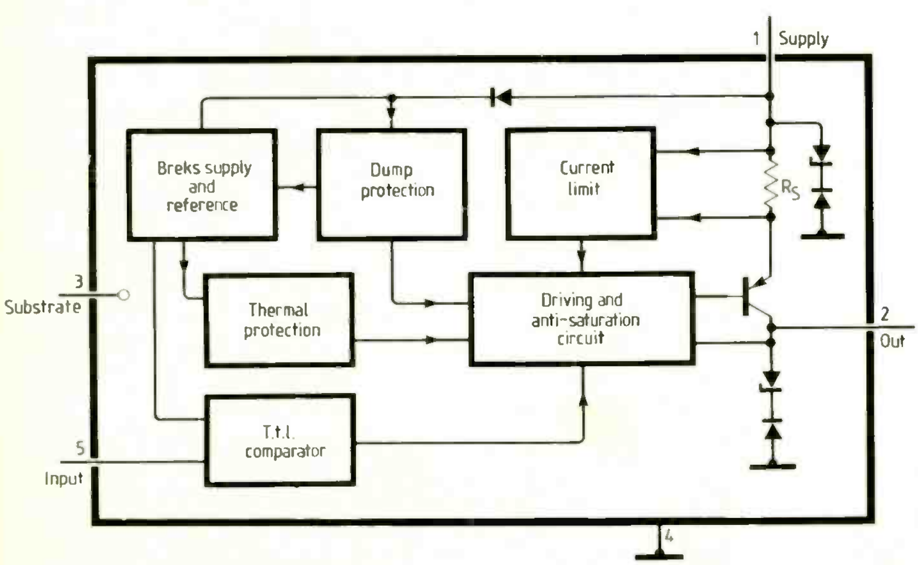


Fig.2. Designed primarily for automotive applications this high-side solenoid driver exploits the structure of Fig.1 to obtain very low saturation voltage.

NEW TECHNOLOGIES

Intelligent power technologies have evolved from two earlier types: linear i.cs and discrete transistors.

Processes of the first type are enhancements of the basic planar i.c. structure, where all the connections are on the top surface of the chip. In contrast, those intelligent power technologies that have been developed from discrete transistor processes have a collector, or drain, contact on the lower surface of the die. A funadamental consequence of this structural difference is that, with processes of the first type, such as the Multipower, it is possible to integrate any number of isolated power transistors and interconnect them in any configuration.

Where a bottom contact is used, it is only possible to integrate a single power transistor, or several with common collectors (or drains). Therefore, configurations such as the H-bridge cannot be integrated but higher current and voltage capability of several hundred volts is possible. This process is known as the SGS-Thomson VIPower™ (Vertical Intelligent Power). Both technologies can be further sub-divided into those which are pure bipolar, and those which contain a mixture of bipolar and mos structures. In both fields significant progress has been made recently.

PURE BIPOLAR

Just how far bipolar technology has advanced is illustrated by the SGS Multipower-S^2P^2 and Multipower-HDS^2P^2 processes.

The first of these, shown in Fig.1, is a 60V process that integrates bipolar linear, i.i. logic, n-p-n and p-n-p power transistors, and a new low-leakage diode structure. A characteristic of this process is that it offers a new isolated-collector vertical p-n-p structure which is much closer to discrete p-n-p transistors in performance terms than the usual lateral p-n-p type. These transistors provide a current density of $0.8A/mm^2$ at $V_{sat} = 1V$, compared to $2A/mm^2$ for n-p-n types, and a cut-off frequency of 20 to 30MHz.

The possibility of integrating high-performance power p-n-p transistors on an intelligent power i.c. allows designers to choose any output configuration. Moreover, the transistor's low voltage drop can be exploited for applications where drop-out is a critical parameter. Such an output stage can also withstand battery reversal indefinitely - an important requirement in automotive application.

The process provides for the inclusion of a new, low-leakage diode structure that has a parasitic p-n-p gain about four orders of magnitude lower than conventional structures, which is convenient for the recirculation diodes in high power i.cs driving inductive loads.

The first device to be produced with this process is a relatively simple, high-side driver, originally designed to the specification of a customer in the automotive electronics market (Fig.2). A vertical p-n-p output transistor is used in this device to obtain very low saturation, high gain (about 30 with 1A output current) and the ability to withstand load dump transients.

The second process is a similar pure-bipolar process which offers e.c.l. logic. However, the most important characteristic of the process is high density. Dimensioned for 20V capability, it is aimed at low-voltage applications where more complex signal processing circuits are needed – up to 270 i.i.l. gates can be contained on one square millimetre of silicon. Current density is $6A/mm^2$ for n-p-n transistors and $2A/mm^2$ for p-n-p (at V_{sat} = 1V and H_{fe} = 10).

MIXED TECHNOLOGY

Considerable progress has also been made in mixed bipolar/mos technology. Several mixed technologies of the 'vertical' type are already available but a significant development is the recent Multipower-BCD process seen in Fig.3, which combines linear, c-mos logic, and double-diffused mos power transistors without placing any limit on the number and connection of the power devices.

Because d.mos power transistors are used, the mixed process enables efficiencies of above 95% and switching frequencies up to 500kHz. In addition, there are no secondary breakdown limitations, paralleling of devices is simpler and there is an intrinsic 'fast' recirculation diode in the power d.mos structure which is adequate for most applications.

The process allows the mixing of low voltage and medium voltage elements on the same chip: lateral d.mos transistors with a breakdown voltage of 60V can be produced in an epitaxial layer dimensioned for 20V linear and c-mos circuits.

The first product to be developed using this process is a motor driver (Fig.4), which uses four d.mos power transistors in a H-bridge output stage. Assembled in a powerdip package this device can deliver 1.5A at 54V with no external heatsink.

VERTICAL PROCESSES

Other recently developed processes include bipolar and mixed vertical technologies known as VIPower-M1 and VIPower-M2. VIPower-M1 (Fig.5) combines 400V n-p-n power transistors and bipolar low voltage (up to $30V_{CEO}$) drive circuits, while VIPower-M2 (Fig.6) will offer 80V d.mos power transistors and mixed c.mos/bipolar drive circuits.

Though these processes cannot be used for devices with bridge and half-bridge output stages, they offer higher voltage capability and the vertical technology features a lower on resistance than the mixed bipolar/mos type.

CHOOSING THE RIGHT PROCESS

The choice of process depends on the output stage configuration, current, voltage and the

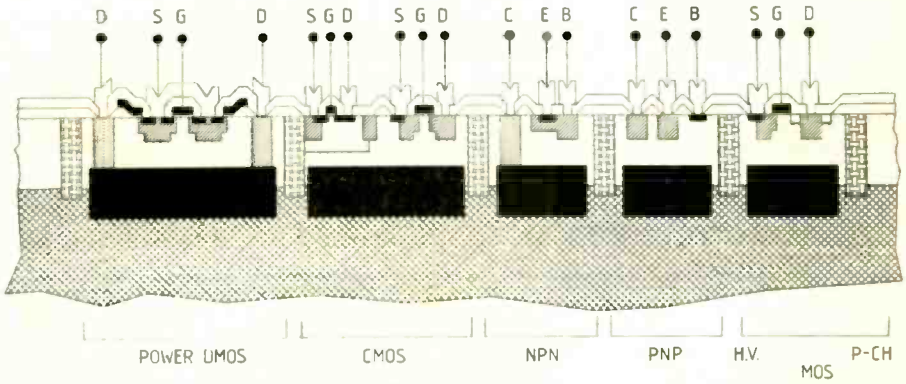


Fig.3. A mixed technology, Multipower-BCD integrates linear, c-mos logic and power d.mos devices on the same chip. Unlike other mixed technologies, it places no limit on the number or connection of the power transistors.

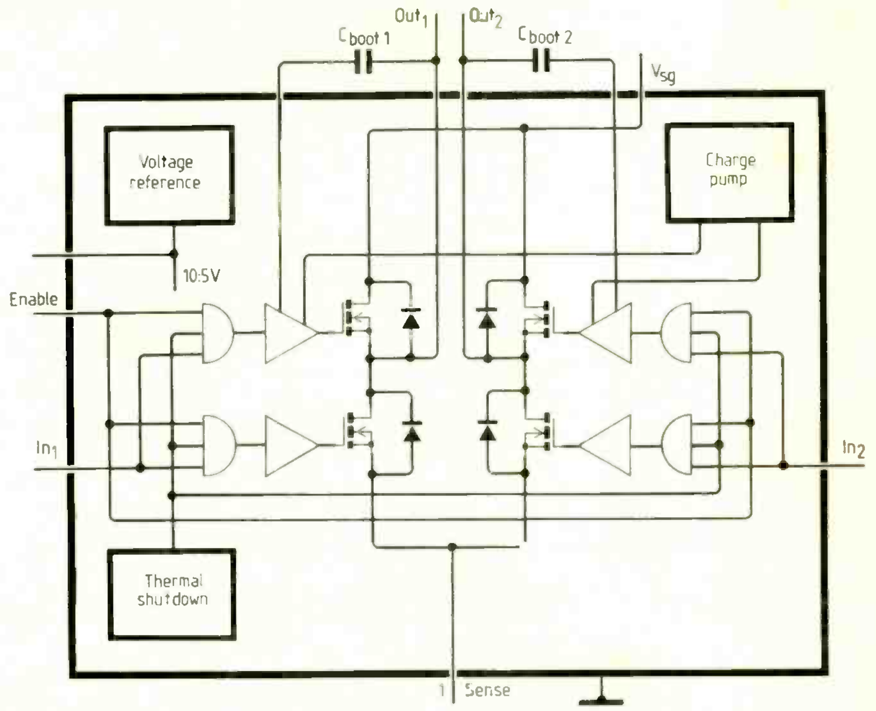


Fig.4. A motor driver chip, is the first product to be made using the technology of Fig.3. The d.mos H-bridge output of this chip delivers 1.5A at 54A but needs no heatsink.

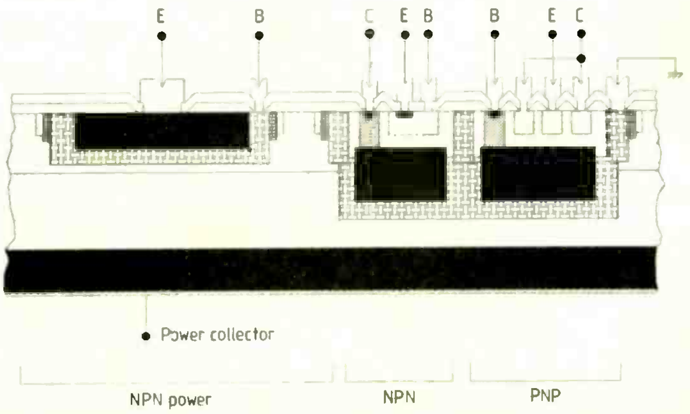


Fig.5. A bipolar process integrating 400V n-p-n power transistors and 30V drive circuitry.

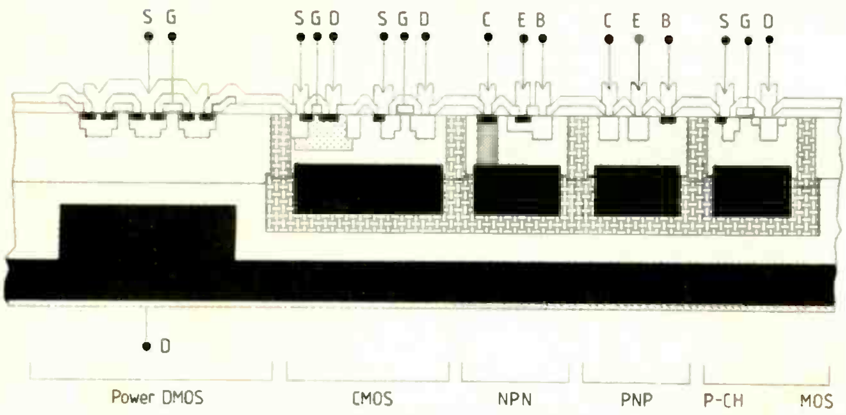


Fig.6. Another 'vertical' power process, this combines 80V d.mos power transistors and mixed c-mos/bipolar drive circuits.

complexity of the signal processing section.

Mixed bipolar/d.mos is the best for lower-current devices where the signal-processing circuitry is very complex. Pure bipolar processes, in contrast, are better for low-voltage, high-current applications, because the current density is much greater. However, future developments in mixed bipolar/mos are likely to erode this advantage in a few years.

One area where mixed technology will not replace the pure bipolar processes completely is automotive electronics, where high-energy load-dump transients occur on the battery rail. To withstand these transients, a d.mos technology must have a BV_{dss} breakdown voltage greater than the peak dump voltage, while a bipolar n-p-n transistor can be turned off to take advantage of the BV_{cbo} breakdown voltage, which is much greater than the BV_{ceo} breakdown voltage.

Mixed bipolar d.mos technology will become increasingly important in very complex power devices. In the near future it will be applied to produce specialized peripheral drivers, optimized for one load type.

POWER PACKAGING

For a power i.c. the package is extremely important, since it determines both the power capability and the cost. At present, most high-power i.cs of the Multipower type are assembled in power-tab packages which are attached to a heatsink, or in special dual-in-line packages with a leadframe designed to reduce thermal resistance. All of these packages are 'insertion' types. However, several trends have now emerged which call for the design of completely new power packages.

First, the increasingly widespread use of surface-mounting techniques and automatic assembly has required new power packages. For medium power (up to 2W) one solution is a plastic chip carrier with a special leadframe. Derived from the 44-lead plastic chip carrier, this package uses 33 leads for connections and the remaining 11 leads to transfer heat to the substrate. It has a junction -to-case thermal resistance of less than 7°C/W, allowing dissipation up to 2W.

For higher-power devices, development is concentrated on a new generation of packages. One package family being studied has a junction-to-case thermal resistance of less than 5°C/W, 3-17 pins, and a lead spacing of 50mils. These packages will have a Small-Outline-width body and gull-wing leads, allowing the use of SO package handling equipment. The low thermal resistance of these packages is obtained by a copper heat spreader on the lower surface of the package which, when the package is soldered in place, is in contact with the substrate. The amount of power that can be dissipated in the device depends on the conductivity of the substrate.

In view of this trend there is now considerable interest in high-conductivity substrates and the various alternatives, such as a plastic board bonded to an aluminium or copper sheet. Plated-through holes in the p.c.b. reduce the thermal restistance between the package and the metal sheet.

Another development is the inclusion of a copper heat spreader on the under-side of plastic chip carriers. These power chip carriers will, like many new packages, be pre-moulded types, which eliminate stress on the die caused by polymerization shrinkage of the moulding resin.

** Sue Cain is with BA Electronics and Ray Ambrose is with SGS Thomson Microelectronics (STM).*

Ernst Ruska – pioneer of the electron microscope

The death was announced recently at the age of 81 of Ernst Ruska, Nobel prizewinner and co-inventor of the electron microscope. Ruska, whose work was only latterly recognised (he shared the 1986 Nobel Prize for Physics), began his experiments in the late 1920s as a student in Berlin and continued them as a sideline of his main work on television technology in the 'thirties.

Ruska and his colleague Max Knoll realised that if they could make an electronic analogue of the glass lens, it would then be possible to build a microscope capable, in theory, of magnifying up to a million times. This compares with an upper limit of about 2,000 times for the traditional light microscope. (The improvement is due to the short wavelength of a beam of electrons compared to that of light. Electron waves are small even on the atomic scale, whilst light is unable to detect less than half a micron.

By 1933 Ruska and Knoll had devised a practical electron lens and constructed a microscope capable of magnifying 10,000 times. By modern standards it was a crude assembly consisting of an electron gun, a series of large electromagnets, and e.h.t. supply, a vacuum chamber and a fluorescent screen. Specimens had to be coated in carbon or metal and maintained under a high vacuum.

In the immediate post-war years, Ruska and other physicists around the world developed the electron microscope into a practical laboratory tool capable of magnifying half a million times. Its belated recognition by the Nobel Committee is therefore no reflection on the quality of that early technology. Ruska himself blamed no-one for failing to take it seriously. What has latterly assured him of a place among the great names of physics is not the technology but the window he opened on the world of the infinitesimally small, but infinitely important. Thanks to the electron microscope we can now 'see' viruses and atoms. **J.W.**

Reader questionnaire

May I thank all those readers – several thousands of them – who took the trouble to complete the recent questionnaire. We have scanned them all, with the considerable assistance of a computer, and intend to make the changes that seem feasible after everyone concerned has had a chance to discuss the results. If I can gather the findings together in a readable form, I will try to summarize them in a future issue. The hardest part, of course, is analysing the comments which weren't computer-readable.

Meanwhile, the "small token" I promised in the note accompanying the questionnaire form will go off to respondents as soon as can be managed, but please give us a few weeks to sort ourselves out. Ed.

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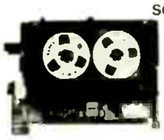

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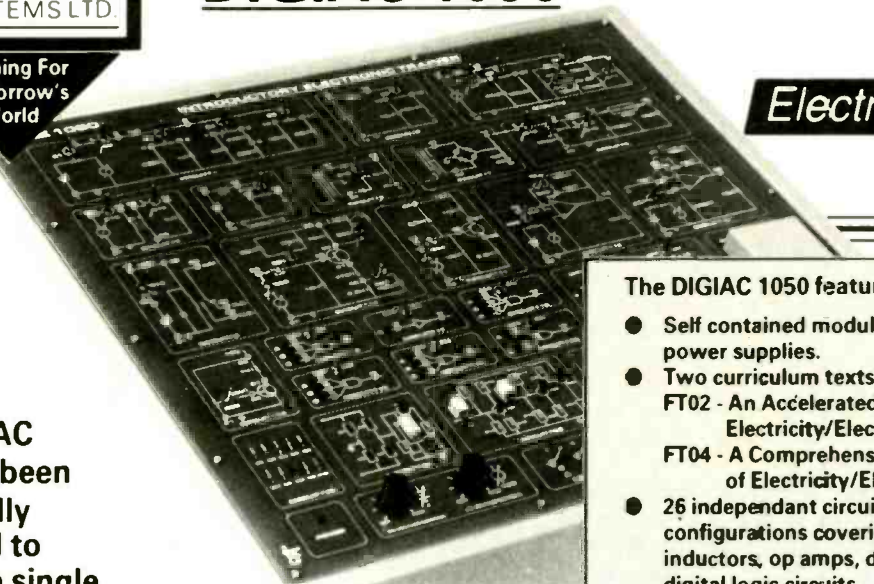

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NEW PRODUCTS

Three-pronged wire twister

A wire twisting machine from Rush Wire Strippers should save users from the sore fingers associated with twisting stranded wire by hand before tinning or termination. The DCFT wire twister can be hand held or bench mounted with footswitch control and has three prongs mounted on a centrifugal head to twist stranded wires neatly and precisely. Rush Wire Strippers. Unit M, Hunting Gate, Andover SP10 3LU. Tel: 0264 51347.

Keyboard size reduced

A keyboard system which reduces the total surface area of a standard ASCII keyboard to 78 by 163mm while retaining the feel of individual 19 by 19mm keys and providing the same functions has been introduced by Radiatron Components.

These keyboards operate on what the manufacturer calls a 'half step' principle by which the operator perceives two distinct 19 by 19mm keys although his finger has only moved half the distance. Each key is divided into four smaller sub keys; if the noticeably raised centre point of the key is pressed then all four sub-keys make contact to make a combined signal. By moving his finger only 10mm the operator presses the new group of four sub-keys (two of the previous ones and two new ones) to produce a different combined signal. In this way each group of four keys has nine functions. Radiatron Components Ltd, Crown Road, Twickenham, Middlesex TW1 3ET. Tel: 01 891 6839.

Interference protection for computers

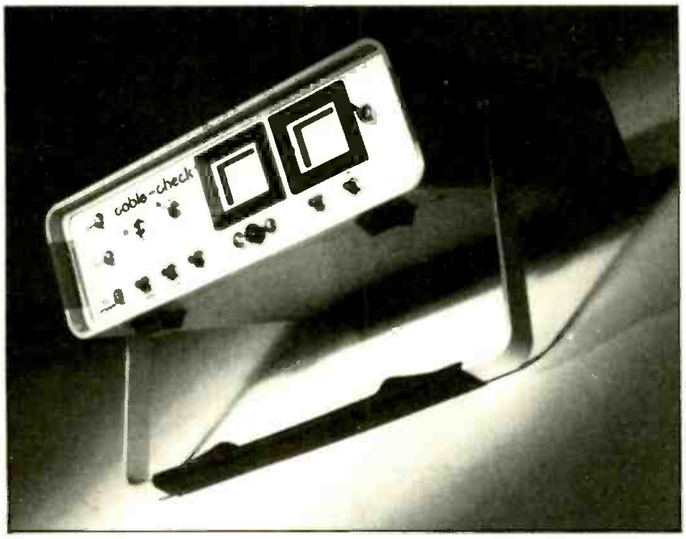
Inlet filters which combine an integral switch, indicator lamp and fuse within a single unit protect office computer equipment and business machines from interference.

The filters are designed to protect sensitive circuits against high-frequency transients, including both symmetrical and asymmetrical power line interference in the frequency range 100kHz to 100MHz. Available with 2, 4 or 6A current ratings, the Belling Lee L2790 filters have a choice of snap-in or screw fixing. Belling Lee Ltd, 540 Great Cambridge Road, Enfield, Middlesex EN1 3RY. Tel: 01 363 5393.

Automatic cable tester

All wires in a cable assembly are automatically tested for open and short circuit using Cable Check 1.

The unit tests individual conductors for continuity and isolation from other wires in a cableform, and gives audio/visual indication of any fault. The front panel has two l.c.ds. to indicate the type of fault. Ideal for loom manufacture and testing, and for field testing multicore and ribbon cables, the tester is powered by rechargeable batteries. Cable Check Systems, 18 Quay Lane, Gosport, Hants PO12 3LJ. Tel: 0705 528396.



Acoustics and vibration measurement

A comprehensive new system of spectral analysis equipment for noise and vibration measurement in real time, together with post-processing power and storage capacity is available from Bruel and Kjaer.

The basis of the 2133 system is the single channel 2123 narrowband analyser for conventional noise measurement. A second channel has been added to offer two-channel and cross channel functions for measurement of sound intensity, particle velocity and the complex cross-spectrum, making the instrument the most powerful intensity analyser in the company's range. Bruel & Kjaer (UK) Ltd, Harrow Weald Lodge, 92 Uxbridge Road, Harrow, Middlesex HA3 6BZ. Tel: 01-954 2366.

Led module for large displays

A 16 × 16 led dot-matrix display module designed for large-scale displays such as public information boards, monitors and as a replacement for c.r.ts has the ability to generate both moving pictures and static graphic images on the black background.

Designed by Toshiba, the module uses 256 lamps, which can display red or green with the addition of amber as a mixture of the two. Single-colour modules are also available from the distributer Dialogue Distribution. Fast scanning rates are obtained with the 20MHz clock frequencies. Dialogue Distribution Ltd, Wicat House, 403 London Road, Camberley, Surrey GU15 3HL. Tel: 0276 682001.

Detecting static charge

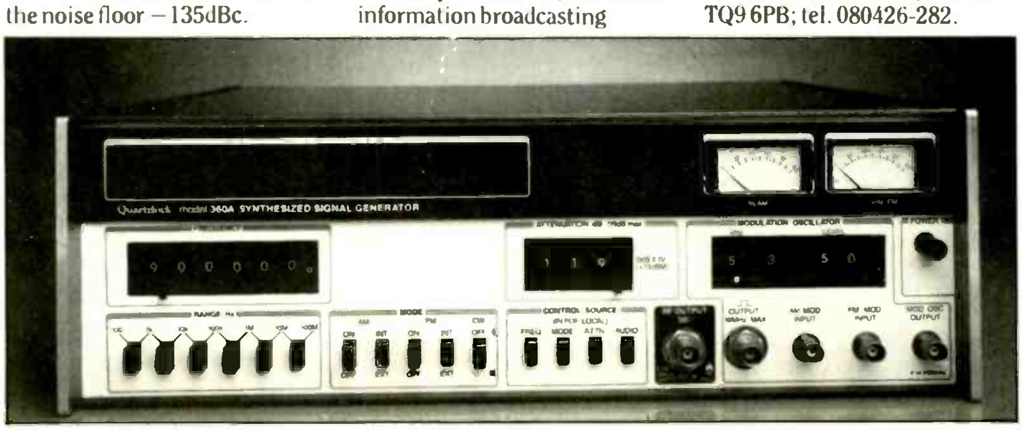
A lightweight, hand-held electrostatic meter manufactured by Chapman Corporation is ideal for detecting static charges in electronic and other manufacturing areas where electrostatic build-up can present problems.

The device has a reading accuracy of ±5% and a response time of 0.5s. It incorporates a clear full-scale deflection meter with four scale ranges from ±1000 up to 30,000V. Available from Teknis, it runs on a standard 9V PP9 battery and weighs only 257g. Teknis, Teknis House, Meadrow, Godalming, Surrey GU7 3HQ. Tel: 04868 5432.

Production test generator

A new general-purpose r.f. test generator from Quartzlock Instruments is claimed to offer lower modulation distortion and better signal purity than any rival instrument. Harmonic distortion is 40dBc down, non-harmonic distortion -80dBc and the noise floor −135dBc.

Quartzlock's model 360A also spans an exceptionally wide frequency range (100Hz to 100 or 110MHz), in a.m. or f.m. modes. A special feature is an optional enhancement for testing receivers for West Germany radio's ARI, the traffic information broadcasting system based on a 57kHz subcarrier. Quartzlock also intends to add a test facility for RDS radiodata receivers. Remote-controlled operation is possible and an IEEE-488 interface can be added. Price is £3850. Quartzlock Instruments, Moor Road, Staverton, Devon TQ9 6PB; tel. 080426-282.



New Products

Your picture on your presentation

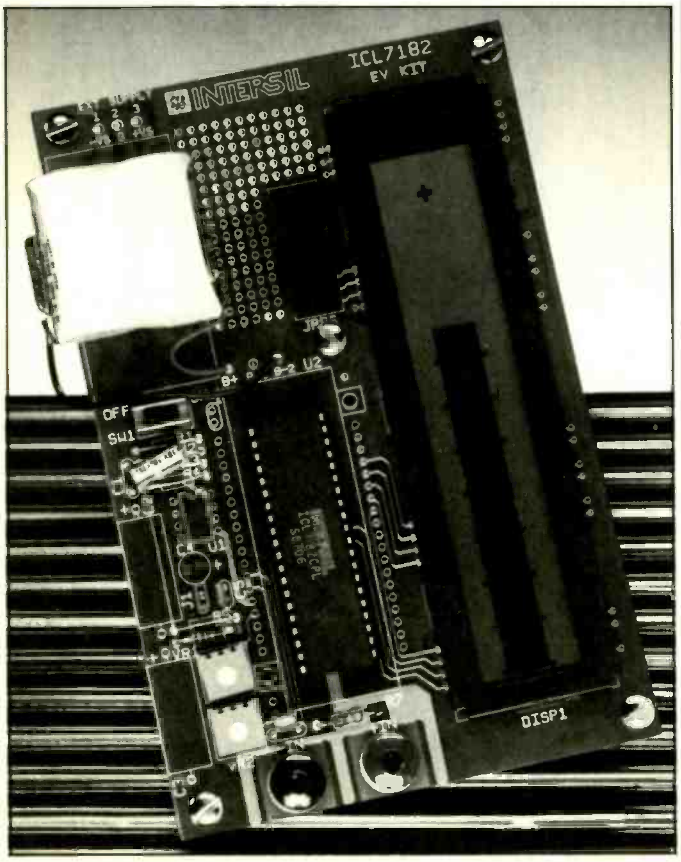
For personalized presentations Digithurst's MicroEye i.c. can be used to input images of personnel, products or company logos into the picture maker module of IBM's Storyboard plus.

The card can capture images from a colour video camera, a standard video recorder, or from any other video source. It works with IBM PC AT and compatibles, and IBM PC XT and PS/2 Model 30. Digithurst Ltd, 7 Church Lane, Royston, Herts SG8 9LG. Tel: 0763 42955.

L.c.d. for temperature measurement

A new liquid crystal bar-graph display with 101 elements is specifically designed to interface directly with an analogue-to-digital converter and display driver manufactured by G.E. Solid State (Intersil).

The l.c.d. is suitable for multimeter and temperature measurement applications. Made by Hamlin Electronics, it measures 1.3 by 4.5in. A complete analogue bar graph can be produced using the ICL7182 converter/driver in a 40 pin package, an l.c.d. and three passive components. Hamlin Electronics Europe Ltd, Park Road, Diss, Norfolk IP22 3AY. Tel: 0379 644411.



Testing telecommunications and data systems

Telecommunications and data systems can be tested with Seaward's LU250 hand-held multi-frequency oscillator.

The instrument has only two controls to master, enabling quick and accurate results to be achieved with the minimum of prior training. Specially built for use in the field, it is backed by a three-year guarantee. Standard frequencies range from 0.3 to 2.713kHz but alternatives are available to suit customer requirements. Seaward Electronic Ltd, Bracken Hill, South West Industrial Estate, Peterlee, Co. Durham SR8 2JJ. Tel: 091 5863511.

Message display

Most types of programmable logic controllers and industrial computer systems can use the DAA 288 series of low-cost alphanumeric message displays to show operator information, alarm or troubleshooting messages.

Up to 255 messages can be stored in each unit by the user with the aid of a simple terminal, programming unit or personal computer, or by plug-in eprom. All messages can include variable data superimposed in the standard text. The displays from ITT Instruments have green fluorescent figures with two rows of 40 characters. Longer messages, up to 175 characters can be shown as moving text. ITT Instruments, 346 Edinburgh Avenue, Slough, Berks SL1 4TU. Tel: 0753 824131.

Erasable c-mos pals

Four new Texas Instruments erasable, 20-pin, c-mos pals are compatible with t.t.l. and c-mos logic and program in t.t.l. levels.

The devices have virtually zero standby power requirement (I_{cc} = 100μA max) and lower operating power than is currently achieved by bipolar pal devices. In a variety of applications such as toys and mobile telephones, solar-powered systems and some telecommunications systems the devices can replace conventional t.t.l. and c-mos logic. Online Distribution Ltd, Melbourne House, Kingsway, Bedford MK42 9AZ. Tel: 0234 217915.

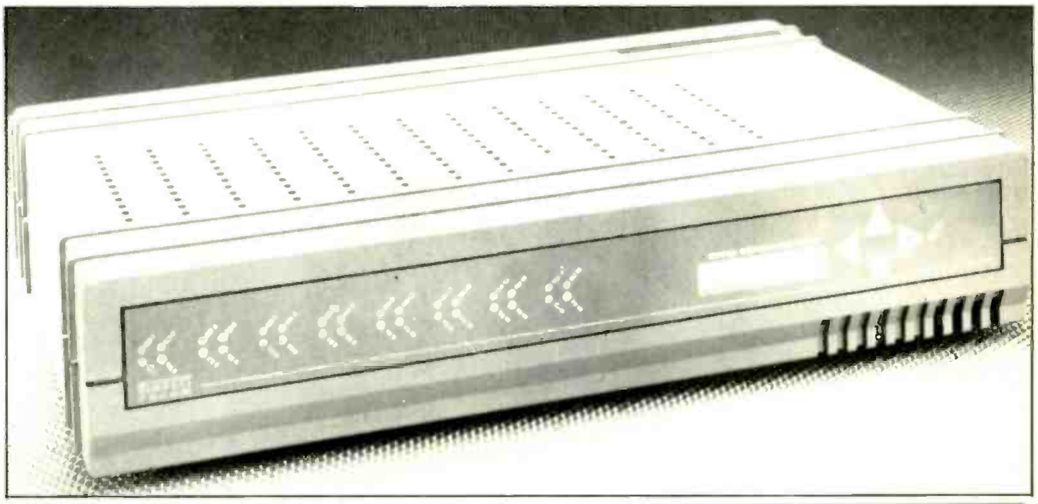
Ceramic chip capacitors

A complete range of miniature ceramic chip capacitors which is suited to surface-mounted applications on both p.c.b.s and hybrid i.cs is available from Bowmar.

Combining high performance and reliability with good frequency characteristics and low inductance, the series is available in preferred values from 0.5pF to 0.1μF. Tolerances are as low as ±0.25F and voltage rating can be 25, 50 or, on special request, 100V d.c. Bowmar Instrument Ltd, 43-45 High Street, Weybridge, Surrey KT13 8BB. Tel: 0932 851341.

NEW PRODUCTS

Optical-fibre multiplexer



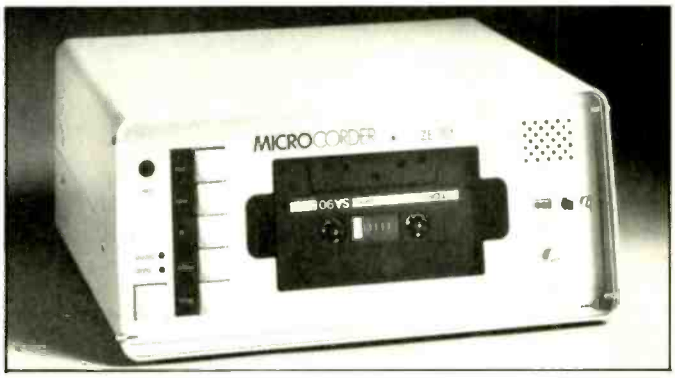
The V24 16 channel optical-fibre multiplexer can be expanded to provide up to 64 data channels over the same pair of optical fibres.

Pirelli Focum has combined the benefits of optical-fibre communications and a ready to use, simple to install and operate format in this model. Configuration is made easy by a menu-driven liquid-crystal display and touch-panel control. A non-volatile ram storage protects all configuration details against unexpected power failure. Pirelli Focum Ltd, Hunslet Trading Estate, Severn Road, Leeds LS10 1BL. Tel: 0532 775757.

Data storage in industrial conditions

The Microcoder mass data-storage device has been enhanced by Wenger of Switzerland for industrial applications.

The all-steel housing of the device is designed to withstand conditions in production environments. The model ZE 701 can be directly connected to a standard RS 232 (or optional current loop) interface for fast recording. Computer-generated operating instructions can be transferred to standard audio cassette tape at 2400baud and data blocks individually identified by spoken instructions. A volume control, three-digit mechanical counter, loudspeaker and microphone are all incorporated. Wenger Printers Ltd, Unit 10, The Valley Centre, Gordon Road, High Wycombe, Bucks HP13 6EQ. Tel: 0494 37372.



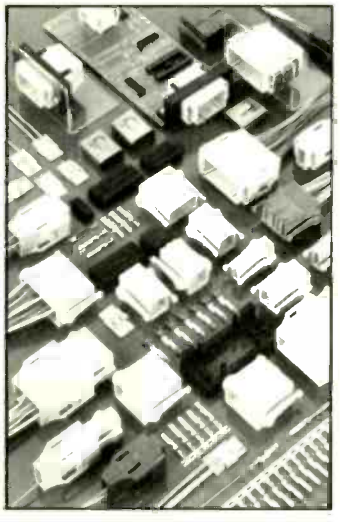
Surface-mounted potentiometers

Murata claims its POTO101 series of single-turn potentiometers is the only surface-mounted potentiometer series suitable for both flow and reflow soldering with a temperature coefficient of ±100ppm/°C. Measuring only 4.7 by 4mm with a height of 2mm, they are available with resistance values between 200Ω and 2MΩ. Murata Electronics (UK) Ltd, 5 Armstrong Mall, Southwood, Farnborough, Hants GU14 0NR. Tel: 0252 522111.

Modular connector system

The various connectors used in conventional automotive harnesses are replaced by just one simple contact crimped to every part lead with the Autocrat connector system from AB Controls & Connectors.

Up to 30 such contacts can be inserted into a single Autocrat shell. Simple accessories allow these shells to be mounted in sealed or unsealed applications. The connector consists of three main parts: contacts, contact carriers and housings. A range of sealing and mounting accessories is also available. AB Controls & Connectors Ltd, Abercynon, Mid Glamorgan CF45 4SF. Tel: 0443 740331.



Micro-controller range

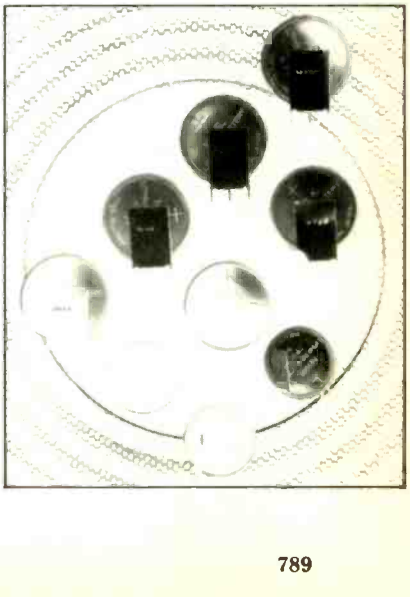
The new high-performance 6502 Plus c.p.u. is the main feature of Mitsubishi's 8 bit c-mos micro-controller range. Known as the M3 7450 series, the new parts are upwardly compatible with the 740 series of micro-computers.

The 6502 single chip micro-computer has improved processing power: the instruction set caters for high-speed 8 × 8 bit multiplication and 16/8 bit division. On board memory sizes are 4K × 8 bits of rom plus 128 × 8 bits of ram. External memory mode has an address space of 64K. 64 pin shrink d.i.p. or 80 pin q.f.p. versions are available. Both packages offer 48 programmable I/O line and two dedicated output ports. There are three input ports on the shrink dip version while eight are available on the quad flat package. Mitsubishi Semiconductors, Mitsubishi Electric UK Ltd, Electronic Division, Travellers Lane, Hatfield, Herts AL10 8XB. Tel: 07072 76100.

Miniature back-up cells

Equipment size can be reduced using a range of lithium batteries from Suvicon with heights of less than 5mm.

The batteries, which have a nominal voltage of 3V and capacities from 70 to 500mAh, are particularly suited for power-supply back-up for solid-state memories. The smallest of the batteries is the CR2016, which has a diameter of 20mm and weighs 1.8g. Suvicon Ltd, 2 The Square, Broad Street, Birmingham B15 1AP. Tel: 021 643 6999.



NEW PRODUCTS

Thumbwheel resistor array

Cermet thick-film resistors give a selected resistance value accurate to within ±0.5% of the indicated value of a precision thumbwheel decade resistance unit.

Resistance ranges from 10Ω to 1MΩ are available on the unit from Data Precision. Being modular, any number of switch elements can be assembled to give the required resolution, without affecting the accuracy. The unit is part of the T-Switch range made by Crameda in Switzerland. Data Precision Ltd. Fromson Building No.1, Canada Road, Byfleet, Surrey KT14 7JL. Tel: 09323 53879.

Co-axial patch panel

Neat termination of co-axial cables from control units and concentrators is possible using a patch panel marketed by Daturr.

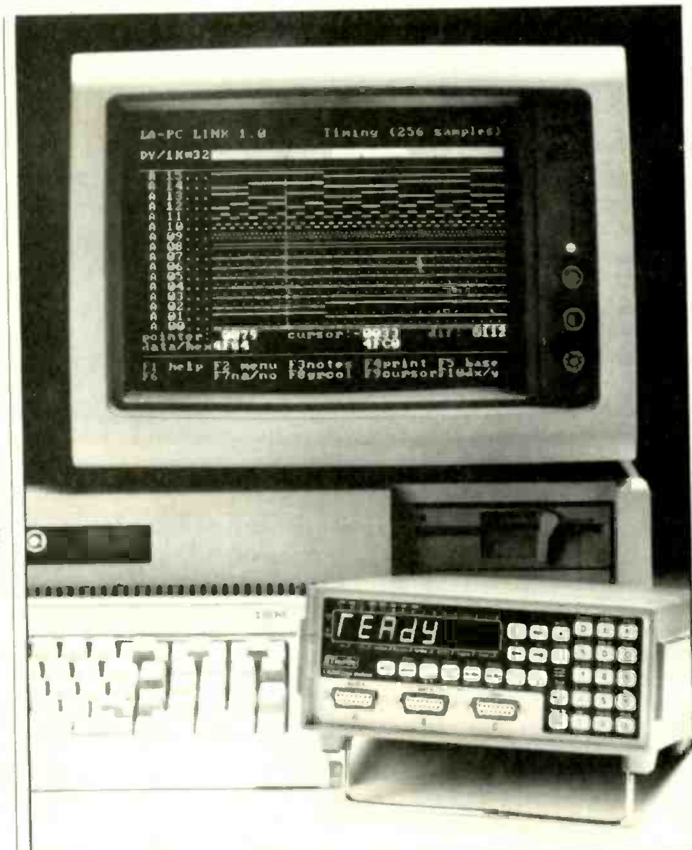
Made from 2mm mild steel to BS1449, it is equivalent to an IBM co-axial patch panel. There are 24 positions for the BNC bulkhead connectors, which should be fitted with standard isolation rings. Daturr can also supply the panel as a 32-way unit. Daturr Ltd. Albany Park, Camberley, Surrey GU15 2PL. Tel: 0276 681212.

Analogue-to-digital converters

Designed for high speed-data acquisition and medical instrumentation, Teledyne Philbrick's new series of 12 bit analogue-to-digital converters combine thick and thin film as well as fast converter technologies. The 4192 is the plug-in replacement for the Datel ADC500/505, while the 4193 and 4195, with a speed of 500nsec max., are the first plug-in replacements for the Micro Networks NM5345/46. Teledyne Philbrick Microcircuits, The Harlequin Centre, Southall Lane, Southall, Middlesex UB2 5NH. Tel: 01 571 9596.

Power supply is 30mm high

The 35W switched-mode power supply from Kepco is only 30mm high and has three outputs: +5V, 2.2A; +12V, 1.8A; and −12V, 0.1A. It can cope with mains voltages from 95 to 264V without tap or switch changes and is in the form of a p.c. card. An optional metal enclosure is available. Techmation Ltd, 58 Edgware Way, Edgware, Middlesex HA8 8JP. Tel: 01 958 1345.



Interface gives low-cost logic analysis

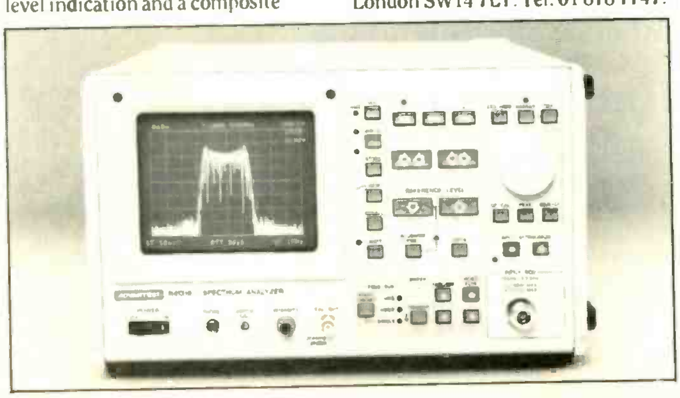
An interface package has been designed to allow a low-cost Thurlby LA160 16- or 32-channel logic analyser to be linked with an IBM PC/AT/AX or with most close compatibles.

It economically provides the facilities normally found in expensive logic analysis systems at a fraction of the cost according to Instrumex. Connection via the RS 232C interface package to the logic analyser eliminates the need for an oscilloscope for the display or timing diagrams or for any requirement for a specific serial interface printer. It also acts as a display terminal with printer echo for use with Thurlby disassembler roms. Instrumex Ltd, Dorcan House, Meadfield Road, Langley, Berks SL3 8AL. Tel: 0753 44878.

Portable spectrum analyser

Weighing less than 10kg, the new R4131 spectrum analyser from Advantest covers the frequency range of 10kHz to 3.6GHz.

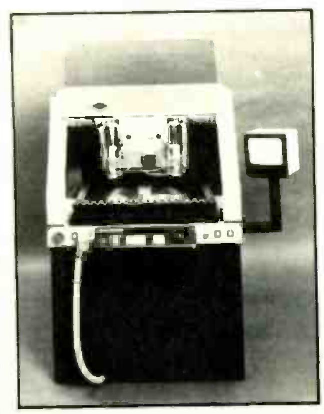
It has a measurement range of −116 to +20dBm with noise sidebands of −80dBc or better. A trace marker gives frequency and level indication and a composite video output allows external displays to be added or video plots to be made. Hard copies of screen displays can be plotted without the need of an external controller, using the standard IEEE bus. Chase Electronics Ltd, St. Leonards House, St. Leonards Road, Mortlake, London SW14 7LY. Tel: 01 878 7747.



Micro-drilling system

Accurate control of precision micro-drilling production applications is offered to p.c.b. manufacturers by a high-speed, automatic, two-spindle c.n.c. drilling and routing machine. It is manufactured by Wessel in West Germany and is available in the UK through Astro Technology.

The drill's air-bearing spindles can run at speeds up to 120,000rev/min and provide precision drilling to 0.1mm diameter. Control is by a new, small, high-performance Wessel CompacTrol control unit which features a hard-disc high-capacity storage unit and three processors, which undertake multi-processor/multi-tasking operation and allow up to six drilling machines to run from a single control unit. Astro Technology Ltd, Astro House, Little Park Farm Road, Segensworth West, Fareham, Hants PO15 5TD. Tel: 04895 77233.



Switch is vandal proof

Resistant to both water and dust, the Bulgin MP33 switch is designed to stand up to aggressive use. It is particularly suitable for applications such as security call systems in areas with a high incidence of vandalism. Operational within a temperature range of −20 to +85°C the switch is rated at 1A 50V. Gothic Crellon Ltd, 3 The Business Centre, Molly Millars Lane, Wokingham, Berks RG11 2EY. Tel: 0734 788878.

NEW PRODUCTS

Sub-miniature fuse family

A quick-acting subminiature fuse designed for automated assembly applications can be supplied in bandolier form at required spacing.

The TDC fuse family from Hunter Electronic Components is constructed with axial plated-copper leads and insulated ceramic body. It has eighteen types covering ratings from 1/16 to 15A. Hunter Electronic Components Ltd, Unit 3, Central Estate, Denmark Street, Maidenhead, Berks SL6 7BN. Tel: 0628 75911.

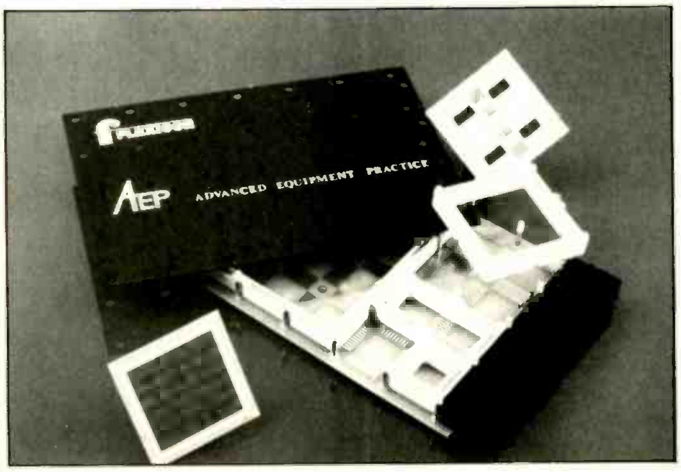
Millions of signal processing operations/s

Inmos don't only make transputers; another of its products is the A100 digital signal processing chip which, like the transputer, can be used in parallel or cascaded to multiply the coefficients. Four of them are used on a VMEbus card produced by T-Cubed. It offers the speed of 1280 million operations/s which translates to a throughput of data of 10M 16-bit words/s. Applications include high-speed digital filters, imaging for radar, sonar and ultrasonic scanning, speech processing, pattern matching, waveform synthesis, convolution, correlation and matrix multiplication.

The board (VME-T3A4) consists of the processor array, 64Kwords of static ram, and memory and control logic stored in non-volatile memory. This memory stores commonly-used configurations which may be implemented through program control. Several data paths into and out of the A100 array are available and can be selected under program control. VME signals are controlled through the bus. Front panel connectors give access to additional high-speed ports which allow continuous processing without any delays caused by the speed of the VMEbus. Use of these connectors allows further boards to be cascaded for even higher throughput.

Optional plug-in modules allow further functions to be implemented, such as analogue signal sampling, also programmed through VME. An additional output, the Cube-Bus, has been specifically designed to feed raw data at high speed to a mass storage device, such as a tape recorder.

The board may be run using a number of popular VME operating systems. T-Cubed Ltd, Lansbury Estate, Lower Guildford Road, Knaphill, Woking, Surrey GU21 2EP. Tel: 0483 797026.



Modular p.c.b. construction

Building a circuit from a number of sub-assemblies has always been an attractive idea, but in practice there is the problem of connecting the modules to the parent board. Flexicon think that they have found the answer in the grandly named Advanced Equipment Practice. Circuit carrier blocks, only 3.18mm high, contain elastomer connectors. The modules are clamped onto these without soldering. Metal posts support the circuits and align the conductors. Individual modules can then be rapidly dismantled and replaced in the field. An additional advantage is that a higher density of solder-free interconnections is possible — up to 6912 on a Eurocard. Flexicon Systems Ltd, Hitchin Street, Biggleswade, Beds SC18 8BN. Tel: 0767 312086.

Analogue input for VMEbus

A high-speed analogue input board for the VMEbus comes from Datel. An on-board 68010 microprocessor allows the DVME-601 a-to-d co-processor to collect automatically multiple samples for transfer to host memory through 64Kbyte of dual-ported ram.

The board accepts up to 16 single-ended or 8 differential analogue input channels. Up to 256 channel inputs are configurable with the addition of slave multiplexer boards in adjacent VME slots. Four a-to-d converter modules offer resolution choices of 12, 14 or 16 bits and conversion speeds as fast as 4μs. Sample rates to local memory of up to 170k samples/s are possible.

Conversions are started by a host command, local program, external t.t.l. trigger or by a local programmable timer. Full-scale inputs over the ranges of 0 to +5V, 0 to +10V, ±5 or ±10V are selected by links. The on-board instrumentation amplifier is programmed with a gain of 1 to 1000.

The board's local microcomputer includes an 8MHz 68010 processor, 64Kbytes of private ram, and 64Kbytes of dual ported ram, shared with the VMEbus. This memory is used for data blocks, command/status information, subroutine addresses, bi-directional interrupts and optional programs downloaded to local ram for execution. Controlling programs reside in a portion of on-board 64K eprom, expandable to 128K. The software caters for most applications and there is no need to write any local programs. The executive program may be controlled from the host, using any language compiled in 68010 code such as C, Basic or assembly. By programming the VMEbus interrupts, the board will operate with many popular host operating systems.

Many ways of managing data acquisition are included, such as writing to one buffer while the host reads the other. The DVME-601 does not have to stop sampling while the latest block of data is read, making it suitable for digital signal processing and other continuous recording applications. The DVME-601 may also be used for high-speed process control, analytical instruments, data acquisition and automated test systems. Datel UK, Intec 2 Business Park, Wade Road, Basingstoke, Hants RS24 0NE. Tel: 0256 469085.

Optical wavelength multiplexer

The function of Sifam's WDM (wavelength division multiplexer) is to allow two different wavelengths of light to be combined, subsequently separated and transmitted through a single optical fibre. In telecommunications it is used to double the signal capacity of existing fibres. It is designed to have a split ratio of 100% at a wavelength of 1300nm and 0% at 1550nm. Better than 20dB isolation between the two signals is claimed with less than 0.5dB or 0.8dB additional loss.

Sifam Ltd, Woodland Road, Torquay, Devon TQ2 7AY. Tel: 0803 63822.

Instrument control through computer windows

Control software for scientific and engineering instruments is provided by National Instrument's LabWindows. Programs are written in Basic or C and there is access to a built-in library of test procedures, graphics, data analysis and formatting, as well as extensive GPIB functions.

Instrument control is said to have been considerably simplified with menus in screen windows to select settings and generate the appropriate program code.

Standard library modules take care of most of the data analysis, formatting and presentation problems. Data analysis functions include array handling, statistical functions and matrix manipulation. Graphics programs includes line graphs, bar graphs, scatter diagrams with linear or logarithmic axes.

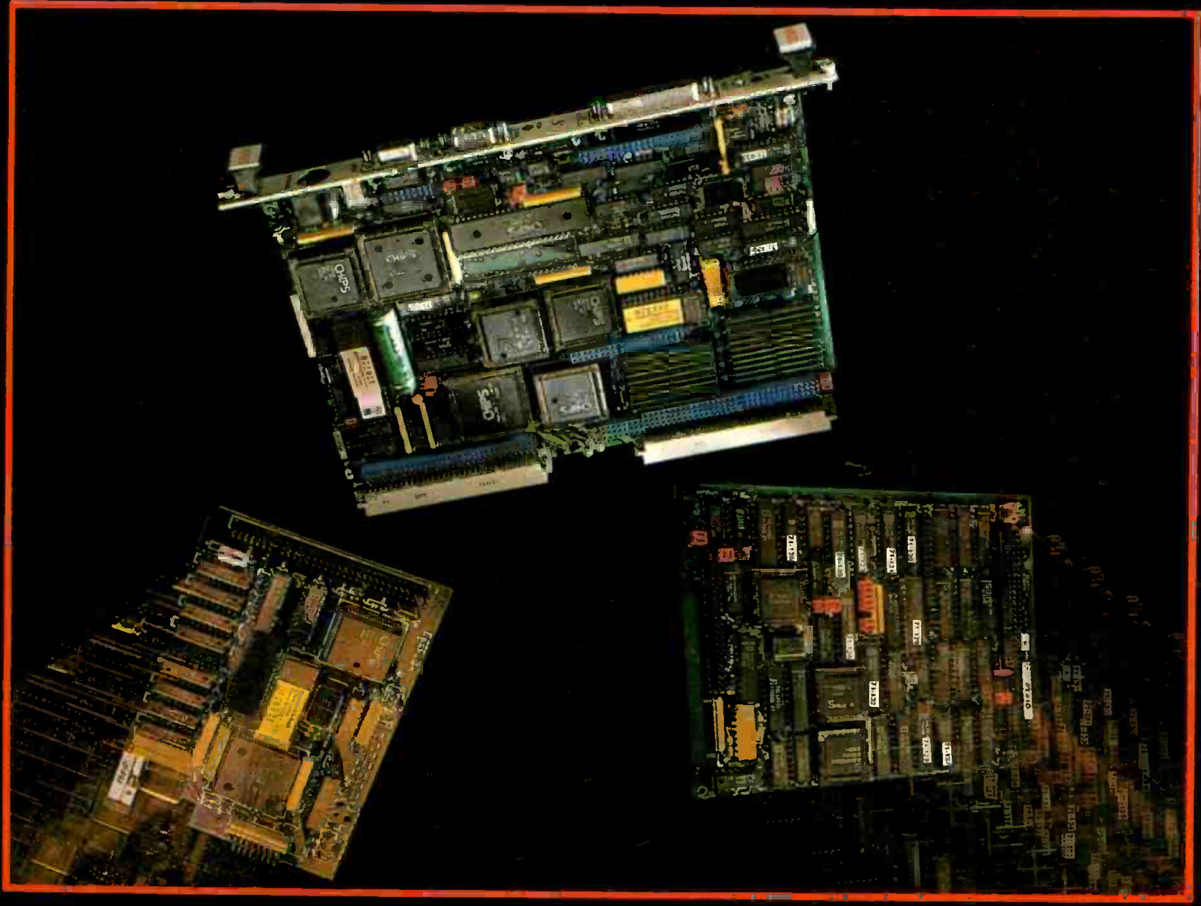
All-in-all the package is claimed to offer a quick and easy means of writing efficient programs for data acquisition, analysis and presentation. Integrated Measurement Systems Ltd, 306 Solent Business Centre, Millbrook Road West, Southampton SO1 0HW. Tel: 0703 771143.

Optical fibre couplers

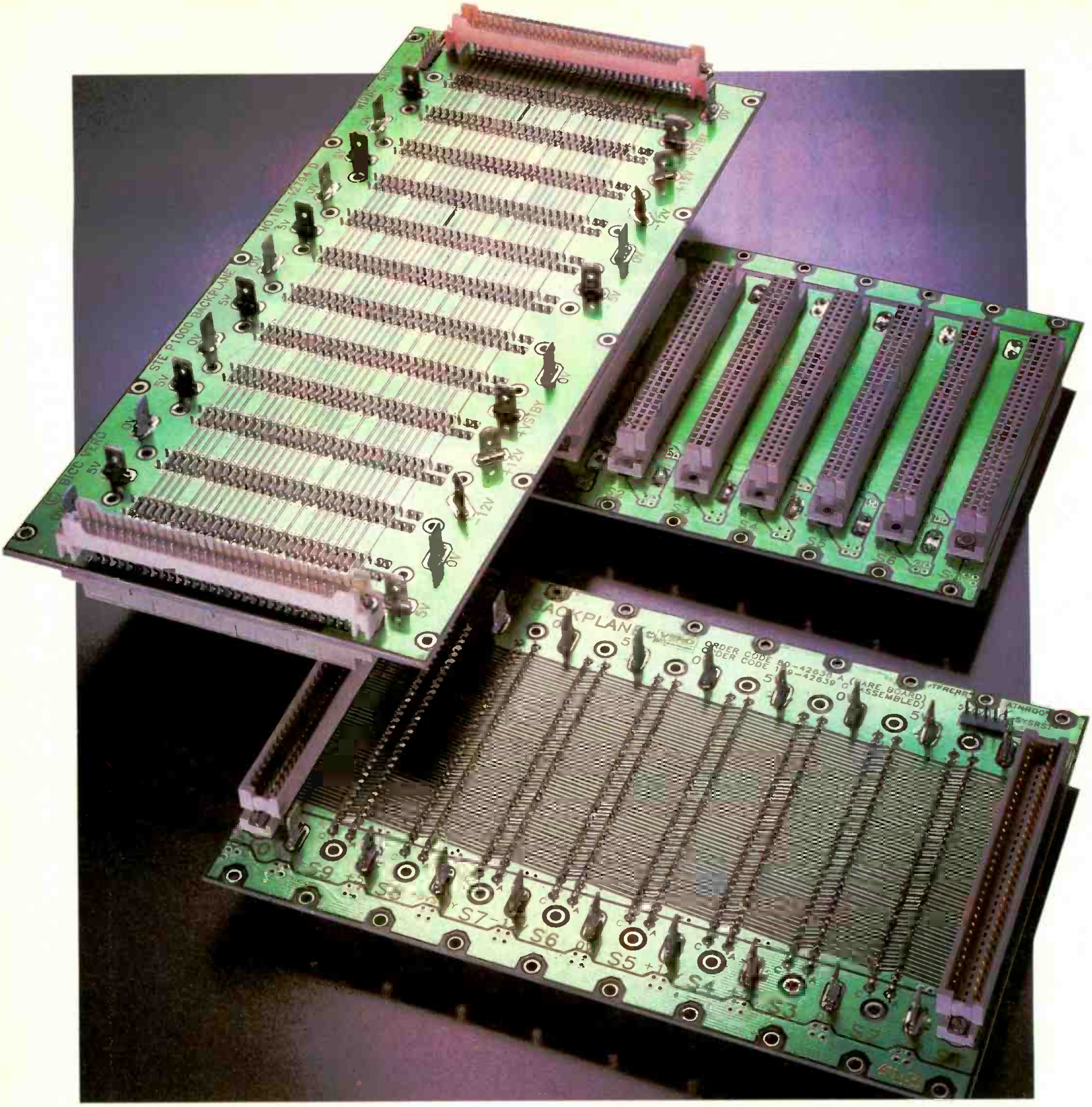
Techniques developed by Corning have dramatically reduced the cost of passive optical components. Etching processes, similar to those used in the production of silicon i.cs, are carried out on wafers of glass and result in the production of highly refractive waveguide channels within the body of the glass substrate. Fibre pigtails are aligned with the channels and bonded into the glass. A 'Y'-shaped channel makes a two-way splitter or combiner and Corning's first 'Photocor' products were indeed tree couplers with one input and up to 32 outputs. On show for the first time at BEW were a series of star couplers which have the same number of inputs and outputs, i.e. 4 by 4, 8 by 8 and 16 by 16. Combined with the tree couplers these will find applications particularly in optical Ethernet and other computer networks. Corning products are available in the UK from Opora Ltd, 21 Victoria Avenue, Harrogate HG1 5RD. Tel: 0423 69307.

AUGUST 1988

INDUSTRY INSIGHT



Bus wars – the cartoon documentary account of behind-the-scenes IEEE standardization battles • Market acceptance of Multibus I, VME, Multibus II • Automotive serial bus set for wider application • Field narrows for factory fieldbus • Interface asics shrink VME systems • Peripheral interface bus evolution • VME board design philosophy • STE, VME dedicated boards replace logic analysers • Three-bus concurrency for Siemens system buses • IEEE896 for beginners • Future of Futurebus



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THE FUTURE OF FUTUREBUS

IEEE896, also known as Futurebus, grew up alongside VMEbus. Both gained their final endorsement as standards by the IEEE last December. Yet, while its sibling has attracted a mass following as the dominant bus for 32-bit systems, Futurebus is hardly off the mark. So far, not one Futurebus board is commercially available.

This is not surprising for several reasons. Firstly, Futurebus is aimed at very high performance. Most system builders have been happy enough with VMEbus, with only a few designing the ultimate in 32-bit systems for which Futurebus is intended. The major board makers, whose interest is vital to any bus standard, see little merit in being first. And for them an uncertain and restricted Futurebus market contrasts sharply with the booming VMEbus business.

Secondly, the board producers expect silicon. No chip maker has yet announced firm plans to implement Futurebus' sophisticated bus protocol and caching mechanisms. Unlike Multibus II, Futurebus does not theoretically need highly integrated devices – the protocols can be implemented in programmable logic – but they would help enormously.

Thirdly, no major sponsor has emerged to put its muscle behind Futurebus to start the band-wagon rolling. The creators of the bus took great pains to maintain manufacturer independence, unlike the designers of VME-bus and Multibus II who enjoyed heavyweight support for, and influence on, their efforts from the start.

Futurebus shows no favouritism amongst processor families. This is good news for builders of multiprocessing systems, but not for the standard. There was no obvious advantage to the major microprocessor makers in backing it. Indeed, with Motorola and Intel firmly behind VMEbus and Multibus II, there were reasons why two of the main forces would not.

Nevertheless, there are also strong reasons why Futurebus may yet come good. Systems continue to get faster and more powerful. Many engineers working some way off the leading edge are now pushing VMEbus to its limits. For their next generation they need another bus. Futurebus is a ready-made and tested alternative to designing their own and has few competitors.

Multiprocessing with cache memories between the processors and bus, the system approach envisaged by Futurebus' creators, is now very much in vogue. And Futurebus offers a clear future upgrade path. There are already firm plans to extend the bus to 64 and even 128 bits using exactly the same protocols and maintaining full compatibility with boards designed now for 32-bit systems.

The long-awaited silicon will soon be here. Industry sources have revealed that the bus protocol and caching mechanisms will be in single-chip devices by the end of the year. This may be enough to spur the board makers into action. If not, the weight of a major processor maker almost certainly will.

National Semiconductor has head-hunted key Futurebus figures – including the standards committee chairman and the inventor of the caching mechanisms – and is preparing a major board and system level strategy embracing Futurebus.

Further endorsement may also come from the VMEbus International Trade Association (VITA), currently discussing adopting Futurebus as VME II. Though some of the Futurebus pioneers may talk of a bus hijack, VITA's backing of the bus as heir apparent to VMEbus would give it a major impetus, whatever it happens to be called.

Before other standards emerged to cloud the issue, the IEEE had envisaged a family of just three buses for 8, 16 and 32-bit systems STEbus, VMEbus and Futurebus. The IEEE has played an almost god-like role in establishing the bus standards of the eighties. Perhaps it too moves in mysterious ways...

Brad Turmaine

INSIDE

Cover. 80286-based microprocessor module from HTEC of Southampton is designed to combine the advantages of VMEbus power, form factor and performance with the broad software support of the IBM PC/AT.

 Industry Insight is edited by Geoffrey Shorter and designed by Alan Kerr. Potential contributors should make contact on 01-661 8639, send an outline by fax on 01-661 8913, or mail articles to Industry Insight, *Electronics & Wireless World*, Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS. Potential advertisers contact Martin Perry on 01 661 3130 or James Sherrington on 01-661 8640.

MULTIBUS THE STANDARD STANDARD

Four years after its launch, how does Multibus II compare in market acceptance with Multibus I and VME?

There are many instances when it is wrong to use a standard bus. Ultra high volume products or special one-off customized products are often better implemented when the processor board and systems bus are hand-crafted. However there has been a clear trend from the late 1970s onward for systems designers to choose a standard bus and standard bus products to get a product to market fast, and take advantage of someone elses manufacturing economies of scale. Normally, a major criterion in choosing a bus has been its 'openness' – how clear, non-proprietary and popular its specification is.

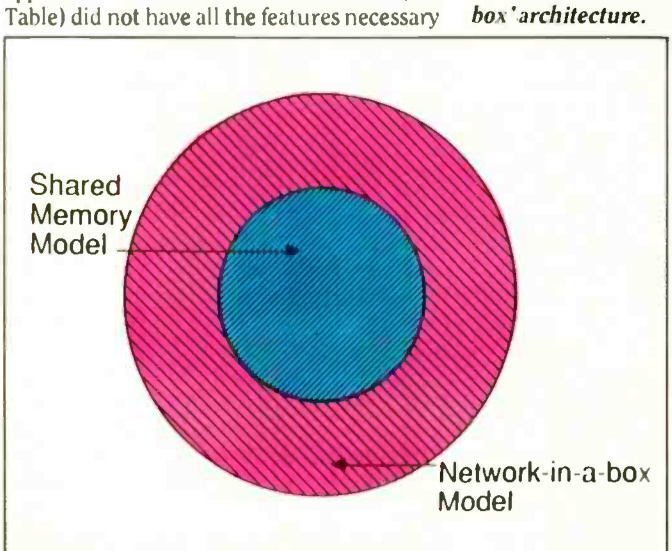
The first of the really open buses, and now the most popular, was Multibus 1. In 1976 Intel produced the first commercially available single board computer, the iSBC 80/10, that integrated on a single board i/o, memory and c.p.u. The specification was made open and hundreds of competitive and complementary products followed from across the industry. Later on, Intel's specification was reviewed and clarified by an IEEE task group, and became the IEEE 796 standard, well known today.

In the UK, as elsewhere, Multibus I is still growing fast despite (or maybe because of) its ten years of history and development. Shipments of Multibus boards have now set record levels for ten successive quarters, and new Multibus products have the latest and highest speed c.p.us as well as state-of-the-art peripheral and communications technology. However in the early eighties it became apparent that the 'traditional' buses (see Table) did not have all the features necessary to build future multiprocessing systems; such as message passing, geographic addressing and virtual interrupts. Computer scientists and researchers reached a remarkable degree of agreement on these features, hence the similarities between Multibus II, Futurebus and Nubus. (As BI bus has remained largely proprietary to DEC, its use as a standard will be strictly limited.)

The only one of the advanced buses to have achieved volume revenue is Multibus II. So four years after launch, how does it compare in market acceptance to Multibus I and VME? There are four success factors for industry standard buses: specification standardization, multi-vendor support, market revenue and profitability, and adoption by users.

Multibus II became IEEE1296 in June 1987, just three years after submission. This compares with seven years for Multibus I and five years for VME. The speed of adoption was testimony to the clarity and unambiguity of the specification, produced by Intel with contributions from 18 other companies, including from Europe: ICL, Bull, Ericsson, Matra, Siemens and Nixdorf. The lack of ambiguity is essential to someone wishing to mix boards from different vendors, which

As well as supporting the shared-memory single-cycle protocol similar to that used by MB1, VME and PC-AT buses, IEEE1296 includes protocol for handling the two address spaces not found in traditional buses – interconnect space and message space – thus supporting the 'network-in-a-box' architecture.



has been a well-documented complaint from users of other 32-bit buses.

In 1987 MBII single-board computer revenue was approximately $50 million, with total MBII revenue $80 million. This compares with $40 million for MBI and $25 million for VME in their third year. There are also a number of public major corporations launching MBII products; NCR and Prime, with departmental computers, Singer Link Miles and McDonnel Douglas, in flight simulation, Westinghouse, Siemens and Seiko for factory automation, and numerous others with projects underway. Despite its rapid takeoff, MBII is a new bus, and does not yet have the market share of its publicity perceived competitor bus, VME. So what makes the Multibus community so certain that it will become the bus of choice by the 1990s? The answer lies in the features that differentiate an advanced bus from a traditional bus.

Multibus II can support two different architectural models; the shared-memory model and the 'network-in-a-box' model. The shared-memory model is the traditional method of bus intercommunication, dating from when the c.p.u. and support functions would take a whole board. Typically several other boards would also be needed, to hold the memory for an average system and its i/o requirements. These restraints were essentially caused by limitations in v.l.s.i. that no longer apply. With today's denser silicon one can build c.p.u. boards with i/o and eight or more Mbytes of data. Modern systems will be increasingly made up of intelligent boards, each with their own c.p.u., with the need to communicate at a very sophisticated but convenient level. These v.l.s.i. developments were foreseen by the specifiers of MBII, and new facilities were added.

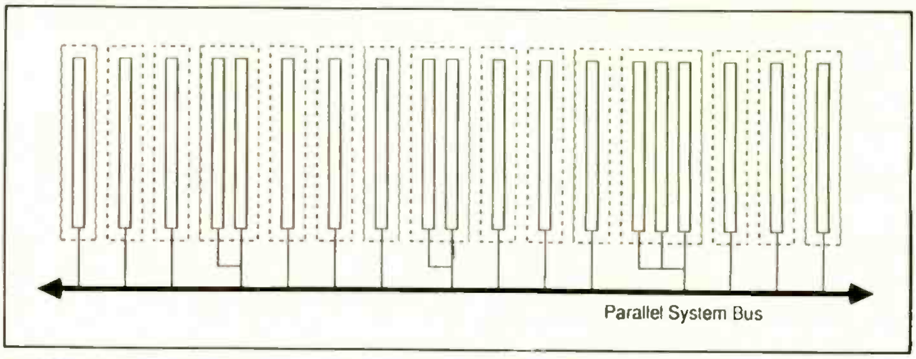
IEEE1296 parallel system bus defines a number of protocols detailing how to use the bus. The simplest is the shared-memory single-cycle protocol, similar to that used by MBI, VME and PC-AT bus. There is also a sequential burst transfer protocol added for higher performance. It also includes the protocol for handling the two address spaces not found in traditional buses, interconnect space and message space. It is these two spaces that allow the 'network-in-a-box' model so necessary in a multiprocessing environment. To understand why these additions were made, look at what advanced systems now require.

Local area networks have become popular because they allow autonomous, intelligent units to intercommunicate and send data when required. High-level protocols like Transport are used to avoid unnecessary detail and complexity. This has also been recognised by systems designers as a desirable approach within the box, for builders of multiprocessing products. What one really wants to do is send messages between tasks running on different intelligent boards, without getting bogged down in detail. This requires a software protocol, or programmable interface, for the transport level and above. Somebody who wishes to build a mass storage board, for example, should have a command level interface to the system bus, which logically sits between the operating system device driver and the i/o hardware. This way, one could upgrade to a higher performance board without having to change the device drivers. This also applies to other types of boards, for example lan boards and communications boards. What we are really saying is that future systems will require within them the equivalent of the ISO 7-layer model.

The good news is that this was all fundamental to the design of MBII, and has now been defined in a body of documents that will be openly available and distributed. Multibus Systems Architecture will allow construction of both simple and highly complex systems, with communications between different boards at a transport command-type level rather than at the bits and bytes level of existing buses. This is fundamental to the current success of MBII. It is not possible to graft these features onto existing buses and come up with a clean solution. The reason why MBII was described as late by its opponents is because of the massive amount of work necessary to reach industry-wide agreement on these complex matters.

Specifying this level of detail up-front means that the silicon interface is also extremely clean. The message passing controller is a single-chip interface to the MBII PSB. It supports the full 32-bit address and data, with a sustained burst transfer rate of 32Mbyte/second. The controller decouples the local bus from the systems bus using high speed on chip fifo buffers. Multibus Systems Architecture takes full advantage of this device. It has been shipping for 18 months now, and was designed here in the UK.

By Sean Maloney, technical marketing manager for Intel (UK) Ltd.



Multiboard subsystems communicating using defined protocols are treated as a single board, while boards within a subsystem communicate using shared memory methods.

TRADITONAL AND ADVANCED MICROCOMPUTER BUS COMPARISON

Bus characteristics	Traditional buses Q-BUS	Multibus	VME bus	Advanced buses Future bus	Nubus	Multibus II
Timing:						
edge sensitive	✓	✓	✓	✓		
level sensitive					✓	✓
Pin usage:						
non-multiplexed		✓	✓			
multiplexed	✓			✓	✓	✓
Arbibration:						
centralized	✓	✓	✓			
distributed				✓	✓	✓
Interrupts:						
dedicated	✓	✓	✓			
virtual				✓	✓	✓
Parity				✓	✓	✓
Geographical addressing				✓	✓	✓
Message passing						✓
Address width (bits)	20 or 22	20 or 24	24 or 32	32	32	32
Data width (bits)	8 or 16	8 or 16	8,16,or 22	8,16,24, or 32	8,16 or 32	8,16,24 or 32
Form factor (in)	9 × 10½	7 × 12	6½ × 9*	11 × 14½*	11 × 14½*	9 × 9*
Connector type	Edge	Edge	Pin and socket**	Pin and socket**	Pin and socket**	Pin and socket**

* Eurocard Dimension ** DIN

WHAT IS THE IEEE896 BUS?

Dubbed 'Futurebus', the processor-independent 896 bus may have suffered in the market place precisely because of its independence. A DTI awareness campaign is set to change that. Here's a résumé of what it's about.

Thirty-two bit microprocessors are forcing designers to leave behind the old standards and seek new ones that will not hold back the performance these devices can achieve. Yet buses such as VME and Multibus II are subject to the same law of diminishing returns with time as their predecessors. Already their limitations are apparent to designers of high speed and performance multiprocessor systems.

The IEEE896 standard set out to satisfy the demand for a bus system that overcomes this technological obsolescence. It is the only standard that will allow significant advances in system performance with improved silicon technology. It favours no microprocessor type over any other and contains a host of features to ease the development of a diverse range of multiprocessor architectures.

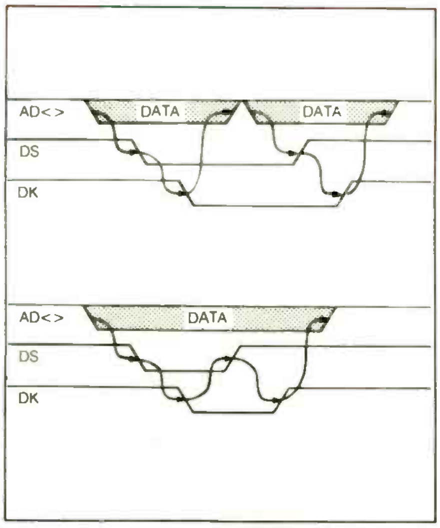
The 896 bus is specified using 'cause and effect' definitions rather than explicit timing constraints to allow designers to take advantage of improvements in devices. Specific synchronization delay figures, for example, are not given. Instead, the standard stipulates that all data lines must be available before the synchronization signal arrives on the bus. As boards with less skew become possible, the bus system can take advantage of them while still allowing older and slower designs to run alongside. Specified in this way, the bus will eventually be able to carry data at close to its theorectical maximum of 280Mbyte/s. Data rates of over 100 Mbyte/s are achievable now.

Buses sponsored by microprocessor manufacturers are naturally biased toward certain processor types. IEEE896 is not. Systems using differing types and makes of processor are therefore easier to implement.

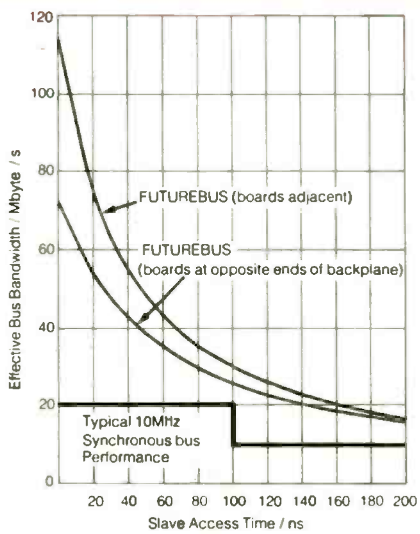
The bus fully supports all the data alignment operations required by the latest generation of 32-bit processors. To avoid favouring some processors over others, it does not justify or sideways shift the data on the bus when operands of smaller width than the bus are transferred.

Both message passing and cache handling features are supported. A tag bit on all data transfers to memory also allows system architectures that need to identify between data and address objects.

The standard specifies a 32-bit multiplexed address/data bus using a single standard 96/96 pin connector to IEC 603-2 (DIN 41612) on a triple-high 280mm-deep Eurocard format (366.7×280mm). It uses a true asynchronous protocol as the means to preserve technology independence (A synchronous protocol would have had a fixed

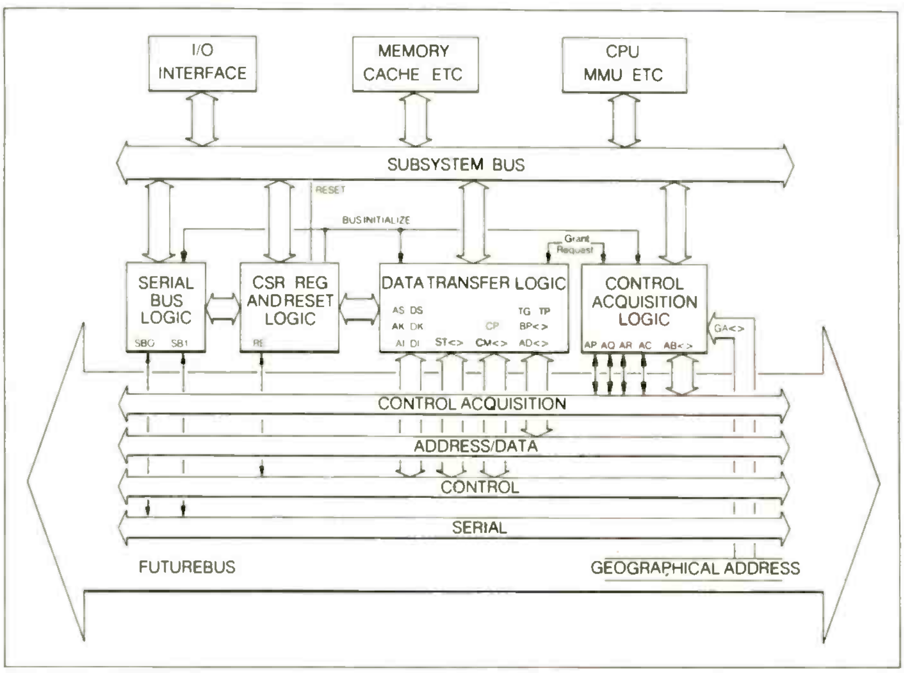


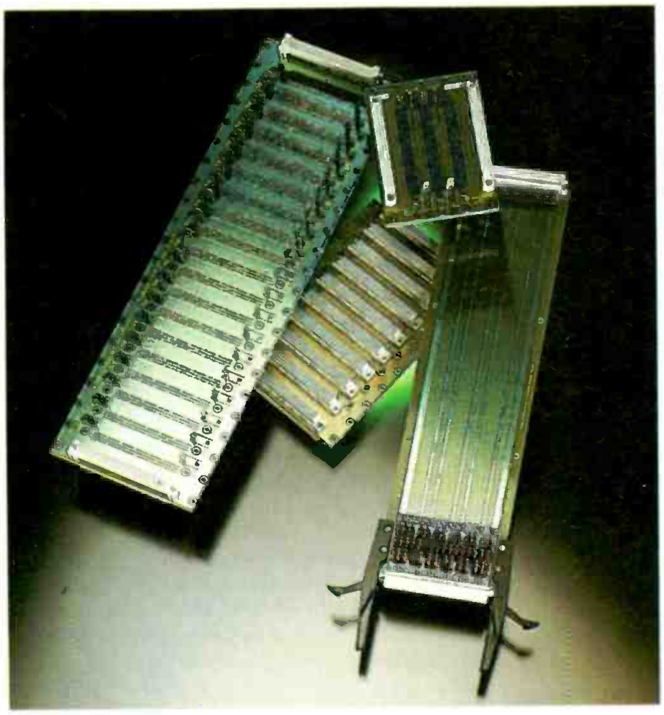
The 896 two-edged handshake for block transfers (top) is twice as fast as the more traditional four-edged handshake, used for single transfers.



This plot of effective bus bandwidth versus slave access time illustrates the speed advantage of the 896 asynchronous protocol for a typical well-designed implementation. Still higher performance may be possible in the future.

Elements of Futurebus are detailed in the 896.1 specification available from FMUG Unit 2, Rowan Close, St Peter's Parkway, Brockley, Northants, NN13 5UP, price £25. A Futurebus Tutorial costs £10.





clock rate and hence a limited future performance.)

It is specifically designed for 32-bit data transfer but supports 8, 16, and 24-bit transfer equally well. It has a 4 Gbyte address space, with expansion capability built-in for future definition.

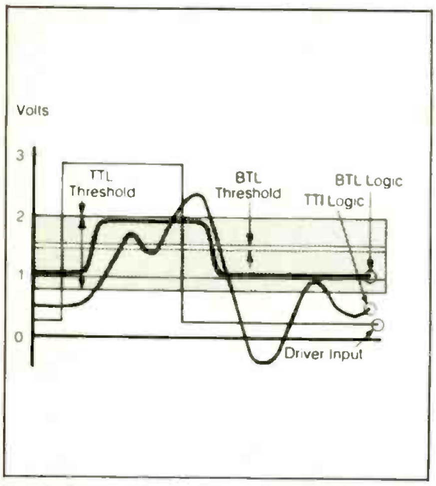
Four types of handshake are provided within the protocol. The two-edged handshake for block transfers provides the biggest boost to performance. This is twice as fast as the more traditional four-edge handshake.

Handles multiple processors

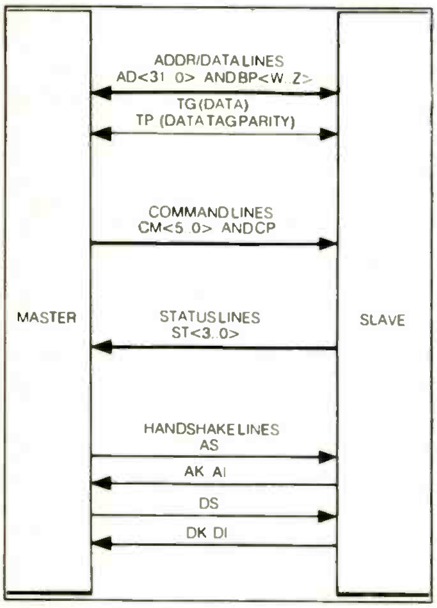
Unlike some buses, 896 does not rely on a single permanent master to allocate control. The system is fully distributed in that all modules capable of exerting control over the bus participate in the control acquisition process. The two schemes widely used for deciding which module should next use the bus are 'priority', in which the most important module always wins, and 'fairness', in which all modules take equal turns. Some systems, such as those for real-time control, will demand the first scheme while others, particularly those performing computing-intensive tasks, may be better served by the fairness algorithm. The 896 bus provides both schemes within a single arbitration mechanism. In addition, modules may dynamically switch between the two algorithms.

Arbitration takes place in parallel with data transfers, so little or so no time penalty is involved. If the next module to use the bus has already been decided before the current master has finished, this can be pre-empted by a higher priority module which can then force re-arbitration. If no other modules

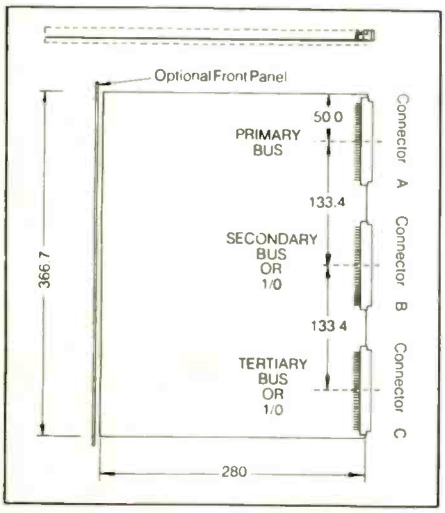
The early definition of the 896-Futurebus backplane format and connector pin-out enabled BICC Vero Electronics to first market backplanes two years ago. Now the range has increased to include 5, 10, 15 and 21-slot versions as well as extender boards and rear-pluggable terminators. "A number of big names are ordering 896 product" says Ray Barnard BICC Vero's marketing manager. "We're unable to name them but FMUG say they expect announcements later this year." "The 896 Workshop in October should attract significant interest in this bus structure" says Alan Timmins of FMUG, who manage the DTI-funded awareness programme.



Backplane transceiver logic settles much faster than t.t.l. and is guaranteed to trigger the receiver without reflections, radically improving the bandwidth of the bus.



The triple height Eurocard format allows dual and triple bus systems for higher total bandwidth or fault tolerance.



want the bus after a module finishes its transaction, the same module may continue to use the bus without arbitration.

Error detection on the arbitration process and the ability to broadcast an emergency signal to all processors without taking control of the bus are also provided. These facilities, along with the flexible arbitration mechanism itself, give the bus a higher performance and wider application than other bus systems.

Backplane transceiver logic

As processor speeds have increased, so too has the difficulty of propagating signals along the bus backplane. To avoid backplane bottlenecks in the future when boards run even faster, a new approach to bus driving was needed.

The key to sending signals quickly down the backplane lies in providing the transmitters with enough output current to cause the initial voltage step on the line to exceed the receiver threshold, otherwise the receiver will only be triggered after the signal has been reflected at least once by the backplane terminations, reducing the effective speed at which signals propagate. As circuit boards are added the characteristic impedance of backplanes falls due to the extra capacitance and increases the current demand on the bus drivers. The traditional way to provide this additional drive capability has been to use bigger output transistors. Unfortunately, these present a larger capacitance to the bus making the driving problem worse.

And as the characteristic impedance of the backplane should be low to help minimize noise and possible data errors, this makes the transmitters task still harder. In a 32-bit system, 40 or more lines may often be switched simultaneously, so if the transmitters' output currents are high, large e.m.i. and ground shifts could affect reliability.

The new approach to these problems is to reject the t.t.l. totem-pole drivers commonly used for bus driving in favour of open-collector drivers in 'backplane transceiver logic' technology. A reduced voltage swing (1V) lowers power consumption and a low-capacitance series diode reduces quiescent capacitance to 5pF, about a third of t.t.l's. Drive current is therefore kept down to 50mA.

Since no reflections are needed, b.t.l. drivers have no setting times; propagation delays are thus much shorter than t.t.l. devices. Though the voltage swing is much less than b.t.l. so is its receiver threshold region (100mV against 1.2V for t.t.l.) and noise margins are maintained. Indeed, the most sensitive noise margin (in the low state) is greater in b.t.l. than t.t.l.

This backplane transceiver logic greatly improves the bandwidth that can be achieved on a backplane bus, especially when an asynchronous handshake is used. At the same time, data transfer integrity is increased due to the proper matching of the transceiver to the backplane physics.

Cache handling facilities

Cache memories are the best way to boost the performance of systems with many processors sharing access to a system-wide address space. Yet 896 is the only bus standard to provide substantial support for implementing them. Other bus systems simply do not support protocols for maintaining consistency of data between multiple caches and main memory.

A highly efficient protocol allows various types of cache and non-caching masters to coexist on the same bus and share memory space while guaranteeing the coherence of the shared memory image. The bus provides a superset of all existing cache coherence protocols.

Write-back caches, in which the main memory is not updated until the data inside the cache is removed or flushed, generally create less bus traffic than write through caches which update the memory each time the data in them is overwritten.

Both types require that the address is broadcast on every cycle, but write-back caches demand several other mechanisms to ensure that a processor does not use data from its cache that has previously been modified in another cache. The 896 bus supports these other mechanisms to allow the highest performance cache systems to be implemented.

Message passing

All the hooks required for message passing are included in the IEEE896 specification, but it is by no means the dominant approach to operating the bus.

Message passing encourages block transfers between modules which make better use of the bus since transaction overheads are reduced. However, the efficiency of many systems can be hindered by message passing and task partitioning; the processing overhead can be many times that of a comparable address-architecture system. Furthermore, since objects are generally much larger than pointers, the transfer of objects between modules can produce significantly more bus traffic, unless programmers design their software to overcome these constraints.

Allowing many processors to share a large public memory resource is intuitively easier to understand and manage and can offer a higher performance if fast cache memories are placed between the processors and the bus. These reduce the bus traffic and help the processors avoid delays in accessing the system memory directly. Moreover, shared memory systems using caches are transparent to the programmer.

Fault tolerant attributes

The standard includes functions to ease the design of fault-tolerant systems. Only one of the three 96-pin connectors on a board is

	a	b	c
1	**0V d.c.**	**0V d.c.**	**0V d.c.**
2	**+5v d.c.**	**+5v d.c.**	**+5v d.c.**
3	AD0	AD1	AD2
4	AD3	**GA0**	AD4
5	AD5	AD6	AD7
6	**0V**	BPZ	AD8
7	AD9	AD10	**0V**
8	AD11	AD12	AD13
9	AD14	**GA1**	AD15
10	BPY	AD16	AD17
11	**0V**	AD18	AD19
12	AD20	AD21	**0V**
13	AD22	AD23	BPX
14	AD24	**GA2**	AD25
15	AD26	AD27	AD28
16	**0V**	AD29	AD30
17	AD31	BPW	**0V**
18	CM0	CM1	CM2
19	CM3	**GA3**	CM4
20	CP	CM5	ST0
21	**0V**	St1	ST2
22	AS	AK	**0V**
23	A1	DS	DK
24	D1	**GA4**	AP
25	AQ	AR	AC
26	**0V**	AB0	AB1
27	AB2	AB3	**0V**
28	AB4	AB5	AB6
29	SB0	RE	SB1
30	TG	S13	TP
31	**+5V d.c.**	**+5V d.c.**	**+5V d.c.**
32	**0V d.c.**	**0V d.c.**	**0V d.c.**

initially used by the system. The spare connectors, along with built-in support in the protocols, allow dual or triple-redundant buses to be realised.

Parity bits are provided on each byte of the addresses and data, and on the control and arbitration signals. These are not needed for the electrical reliabilty of the bus but for fault detection in fault-tolerant systems. Live insertion and withdrawal of boards is another unique feature.

Target applications

- IEEE 896 bus allows rapid access to, and operations on, large bit-mapped graphics displays due to its asynchronous protocol, inherentr high performance, and range of facilities to support advanced workstation architectures.
- Tasks such as logic simulation and modelling can also benefit from the speed and high performance of 32-bit processors combined with cache memory.
- Fault-tolerant system designers can take advantage of the many facilities 896 offers in this area.
- The rapid block-transfer mode and extensive task synchronization when reading and writing to buffers make the bus suitable for communications nodes.
- Real-time systems can be added to the list because of the high performance and dynamic priority allocation of the bus and its versatile event mechanism.

Silicon support

National Semiconductor has a range of transceivers, drivers and receivers for production and second sourced by Texas Instruments. National is also developing control devices for the bus protocol. Plessey Semiconductors is defining a transceiver with latch parity.

Backplanes, prototyping boards and packaging products are already available from a number of suppliers including BICC-Vero Electronics. Dedicated prototyping boards are under development. A considerable number of board and systems companies are known to be developing Futurebus products; announcements are expected over the coming months.

DESIGNING 68030 INTO VME

VME board design should use and further the techniques of the microprocessor, says Radstone's Colin Davies

A high performance bus system such as VME provides an ideal vehicle to take the 68030 into the market place and separate the system integrator from the complex task of ensuring that the processors immediate environment supplements its natural strengths. Such a board design is of course possible, but it is the design that has been done in sympathy with the original processor design goals which will yield the best and most versatile solution.

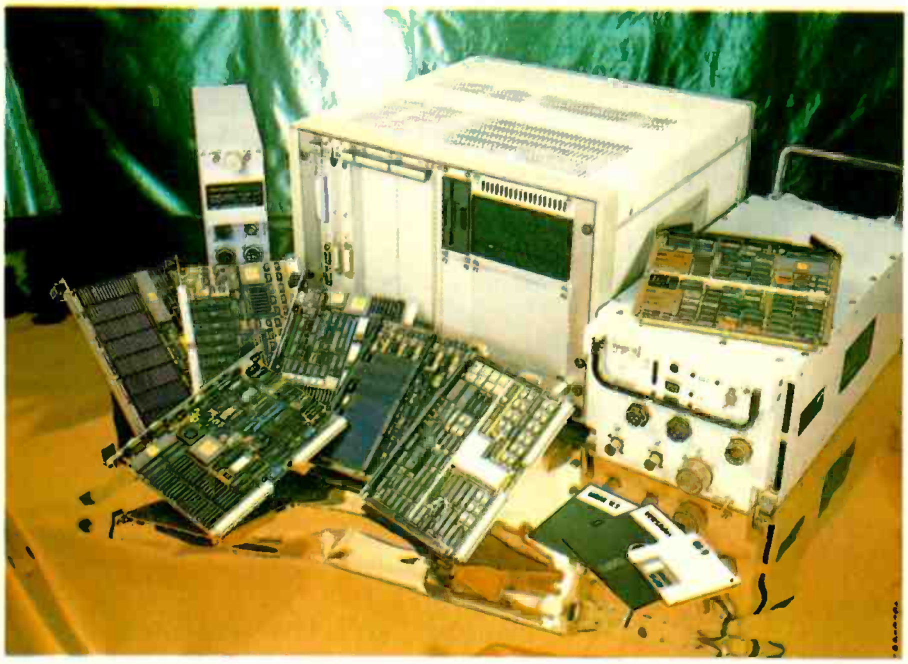
As a member of the 68000 family the 030 brings with it a wealth of software and only the most outrageous hardware design would not be able to take advantage of this. However the ease of porting existing software must be supported by hardware, which itself provides an upgrade path. For example, it must be possible to fit faster processors, or increase memory capacity as devices become available.

On-chip caches are the only way to ensure that a microprocessor's true performance can be realised economically. Typically the 68030 instruction cache achieves a hit rate of up to 82%, whilst the data cache can satisfy up to 48% of all data movement requirements. This corresponds to approximately 33% of processor cycles using its external bus. High performance can therefore be achieved with relatively low-cost dynamic rams and this allows useful quantities of local ram to be provided (the current explosion in dram capacities as been matched only by the ability of operating systems to consume it!).

The 68030 echoes this philosophy and a technique known as cache burst filling has been incorporated into the microprocessor to take advantage of the fast access modes provided by most drams and improve the cache hit rate. Radstone Technology wished to take advantage of this technique in their PME68-30 series of boards and actually achieved burst fill access times of less than 25ns, comparable to small, high power static rams. Indeed, Radstone were able to take this a stage further by simultaneously accessing four banks of dram and taking advantage of the fast output enable times provided by modern devices.

Provision of on-chip caches can mean that the 68030 will spend less than 50% of its time using its local bus. This allows our local dram to be dual ported between the processor and VME, simplifying the task of system integration.

The microsystems division of the Plessey Company was recently sold to its management, with financial backing from venture capital specialists 3i. Called Radstone Technology, the new company produces over 5000 boards a month, mainly VME, Multibus and bubble memory systems.



Even though the VMEbus allows a relatively simple and easily optimized interface to be provided, care must be taken to understand the design philosophy of the 68030. The dynamic bus sizing allows it to read byte, word, three-byte or long word quantities over the VMEbus. However the 68030 cache expects data on its data lines to be valid for the entire width of the port being addressed. Thus a byte read from a 32bit VME port would result in 32 bits of cache data being stored. Clearly hardware on the processor card must detect such situations and generate VME read cycles of the width of the port being addressed.

Increased integration reduces the board area required by the processor and its support chips. This allows more peripheral devices to be provided on a processor card. With careful choice and shrewd design these should not restrict processor performance. Polling such devices can be interesting; after the first access the data cache could easily service all future reads. It is of course possible to define areas of memory space as being non-cacheable but a hardware link to achieve this goal can save many hours of software development time!

Once the design has taken shape we have the framework of a high performance processor card. However the user's application must remain paramount and scope must be provided for value to be added to the product. Radstone Technology address this problem by allowing for firmware expansion and providing a custom peripheral expansion bus (Pexbus). Processor chip caches make it imperative that a simple method of observing software operation be provided. Truly dual-ported rams help or here in that the process should be able to read its own ram locally or over the VME bus, with all VME address and data lines being driven correctly. Now all that is required is to plug a standard VME bus monitor into the backplane and run code over the VME bus.

Thus we have the blueprint for a VME-based product, but the design techniques used are important. The board design must always further the techniques used in the microprocessor that forms its heart. Only then will the design succeed and the user find it worthwhile taking advantage of the good support and documentation which any vendor must provide.

Colin Davies is leader of the processor design group at Radstone Technology (ex Plessey Microsystems), Towcester, Northants.

IEEE microprocessor standards committee projects

Title	IEEE standard	Project number	Active	Notes
Assy lang.	694			
Mufom	695	P695	√	Universal format for object modules
S100bus	696	P696	√	32bit, 5V revision
SBC		P697		Small business computer
FPA	754			Floating point arithmetic
HLL ext	755			
Multibus 1	796	P796		
FPA-RFI	854			Radix, format independent
MOSI	855	P855	√	Operating system interfaces
EMP		P856		Evaluating micro performance
Futurebus	896.1	P896.2	√	32bit multiprocessor bus
MIIT	949	P949	√	Media-independent information transfer
SBX bus	959			I/O extension bus
STD bus	961			8bit single-processor bus
Versabus		P970	√	Larger board than VME
PC bus		P996	√	
STE bus	1000			Eurocard STD-like
VMEbus	1014			Versa Modules Europe
VSB	1096			VME subsystem bus (IEC47B)
Mechanical	1101			Mech. core specs (896.1196,1296)
VMS bus		P1132	√	US adaption of IEC47B VMS
Forth		P1141	√	
Modula		P1151	√	Relates to ISO w.g.
Smalltalk		P1152	√	
Pilot		P1154	√	
I Bus		P1155	√	Instrumentation bus
Rugged i/o		P1156	√	Concurrent with P1496
Scheme		P1178	√	Lisp-like language
Nubus	1196	P1196.2	√	Simple 32bit systems
Multibus II	1296			32bit multiprocessor bus
Serial bus		P1394	√	
TDM i/o		P1395	√	Physical i/o configurations
TDM bus		P1396	√	PBX communications
Rugged bus		P1496	√	Concurrent with P1156

Study groups:
Superbus
Relational data
Graphics language interface
Block structured tape formats
System architecture

Compiled from information supplied by Clyde Camp, IEEE Computer Society MSC chairman

STEBUS LOGIC ANALYSER SPEEDS SYSTEM DEVELOPMENT

Backplane buses speed system implementation... unless you encounter a bug. Then their key advantage – one common interconnection highway – becomes a debugging liability, says Anthony Winter.

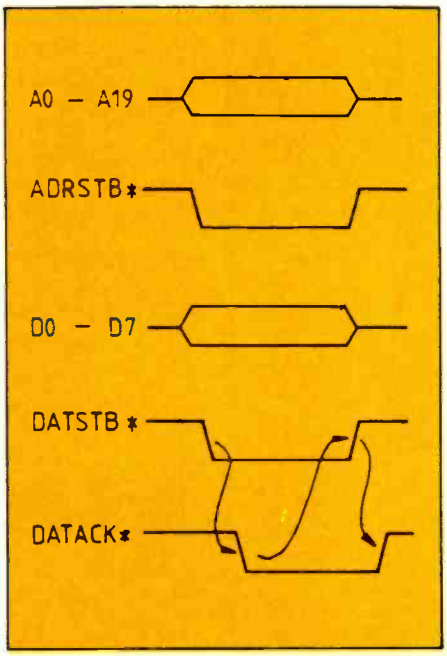
The electronics manufacturing world has quickly latched on to the time-saving benefits to be gained by designing systems around buses such as STE. Thanks to word standardisation, you can have a product idea and be half way to implementing it within just a few days.

But there's a catch. Even though your hardware components are, in theory, fully tested and functional, the designer often faces very complex problems when integrating the final system. The software is typically unproven, nearly every board in the system needs to be set up using dip switches or jumpers to function properly, and there is often a small element of custom hardware, perhaps some special interface. Several different highly complex elements – perhaps even multiple processors – are coming together for the first time, and more often than not, the first thing that happens when you switch on is ... *nothing*. But where's the problem? You check the power, waggle the cards, but still the system is dead. With everything connected on a common interconnection highway, here starts a problem that could take anything from a few minutes to a few days to resolve. Since the major factor behind buying ready-made computer modules is to speed project completion, it rather defeats the object of the game.

This scenario might seem unusual, but it is in fact, pretty typical. Arcom's STEbus applications engineering desk for instance, deals with probably 25 queries a week on just these kinds of issues, and this situation led us to define a simple analysis tool which fits the style and budget of board-level system design.

What we felt the system builder needed was a low-cost tool that would track activity on the bus, allowing attention to quickly be focussed on the cause of the problem: a logic analyser seemed the ideal instrument, but they are designed primarily for the board development market, and are generally too powerful, costly and cumbersome to set up for the system integrator. The solution was to design a stripped-down analyser with functions dedicated to bus lines, giving the systems engineer at-a-glance indication of bus status, with features that allow him to quickly track faults down to specific causes. That's the concept behind the development of Stela, a logic analyser for the widely-used STEbus board system

How Stela could be used to capture data. In this STEbus data transfer operation – a write cycle is shown – data will be latched by Stela after the falling edge of the data acknowledge signal.



STEbus analyser

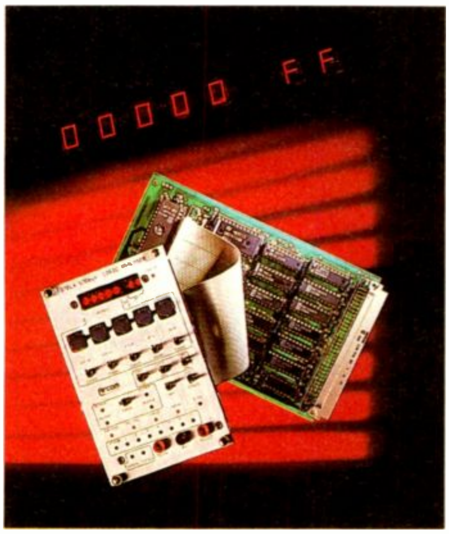
Just like any other STEbus board, Stela is a plug-in. It performs four basic functions: monitors, latches, triggers and displays. Almost every STEbus line is monitored and converted to a meaningful display on the front panel. It is – in the parlance of logic analysers – a 'state' analyser rather than a timing analyser; it has no means of indicating that a particular STEbus transfer was marginal, but it will tell you, for example, what address you were trying to access.

You can set up the analyser to trigger on any kind of STEbus access for instance, to any specific memory or i/o address, or range of addresses, or combination of these parameters. You can also trigger on particular STEbus cycles qualified with 'bus-acknowledge', and switches allow you to set the instrument to recognise or ignore any command modifier. Further useful led displays constantly monitor STEbus' special signal lines, allowing an engineer to quickly recognise that an event is tied to say, a power glitch, but time-out, transfer error, system reset or some activity on the attention request lines. Data capture can be set for single-shot mode, or continuous trigger on every occurence, with results shown on seven-segment displays. And if this level of information is not adequate to resolve the problem, as it may not be in the development environment, a trigger-output signal is provided to activate a more sophisticated analysis instrument such as a timing analyser.

How useful is such a tool in practice? Here's an example of a typical debugging situation, to give you an idea. In this imaginary case, there are two hardware faults.

Problem: the system starts to work and then halts.

Solution: hit the system reset switch; Stela's reset led will flash in response. The 'bus time-out' led lights, indicating that a transfer did not occur within the maximum time allowed. Set Stela to single-shot acquisition



mode, press the arm button and reset the system. As the system halts, Stela now indicates that the timeout occurred at address 00FC0. From here it's a simple matter to discover what board ought to reside at this address, remove it, and find that the fault is merely incorrect jumpering.

But the system still does not work. Bus activity takes place, but once again the system comes to a halt. Re-arming Stela, in case there is some useful information on the bus, you discover that one of the 'attention request' leds is on. In our imaginary system, this line is used for d.m.a., so you conclude that a link on the c.p.u. connecting bus attention requests to d.m.a. inputs has not been made.

The system now runs, but Stela's usefulness does not stop here. In single-shot acquisition mode, the instrument's displays change whenever there is a bus access – unless Stela has triggered. In continuous acquisition mode, the display is updated whenever a trigger occurs. Our imaginary system is operating some code across STEbus. You can find out where this is, by setting the system for continuous acquisition and all the other switches to 'ignore'.

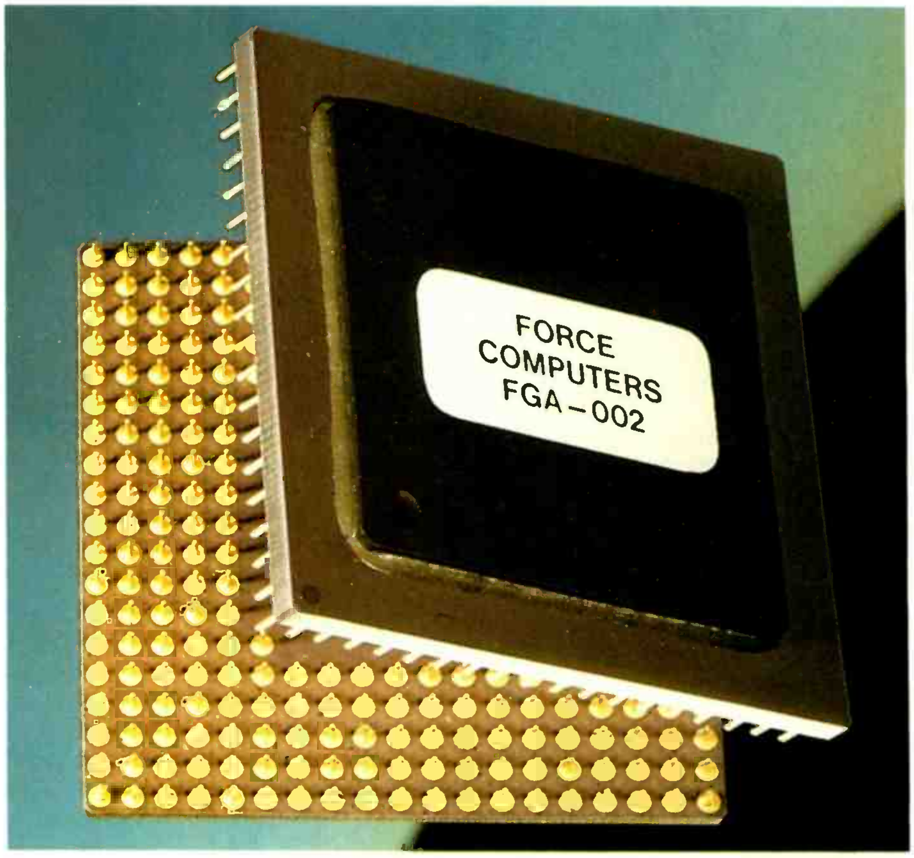
Stela now triggers on every bus access. Starting with the highest order address switch, push the ignore switch upwards (ie, to the 'do not ignore' position). Then rotate the address switch until the triggered led flashes again. Repeating this simple action for all the other addresses switches, you can quickly find the exact address being accessed. Similarly, by using the 'command modifier' switches, you can tell what type of bus access is taking place.

Once you've proved that the basic hardware works, you can turn your attention to the software. Stela can also be used to debug i/o-intensive programs written in a high-level language. For example, let's assume that you have a C program that seems to be looping on an incorrect status bit in a register on a STEbus i/o board. If you rewrite the C routine to print the value out for inspection, it will take some while to recompile and link. Instead, you set Stela to trigger on accesses to that i/o address and the display immediately shows you the data byte.

These examples give you an idea of the utility and power of a bus-specific logic analyser. At a cost of £355, this simple instrument could pay for itself in a single debugging session. With the fast-accelerating trend toward using bus-based components for systems design, tools like this will find a ready market and fuel further growth. And as the general complexity of systems grows – as is the case with STE – we expect that the availability of such tools will in some cases influence the bus selection process, being a further factor in the demise of the many unstandardized proprietary buses.

For further details contact Anthony Winter at Arcom Control Systems Ltd, Units 8-10 Clifton Road, Cambridge CB1 4WH. Tel: 0223 411200.

VMEBUS INTERFACE ASICS



Key features of a VMEbus interface circuit being developed by a US asic manufacturer were released to the US bus community at Buscon 88 West earlier this year. Dubbed VIC, the chip will let VME product designers reduce board space required for interface and control functions by 25%, releasing space for other functions. The chip is designed using a full standard-cell approach and includes embedded programmable logic arrays. The 12,000 gate-equivalent one-micron c-mos device will be housed in a 144pin array and become a standard part in VTC's product line from the fourth quarter 1988.

The VIC features high current drive output and control logic on the same chip. It includes a bus arbiter and requester, interrupt handler and generator, system controller, and data transfer-bus controller. Other features are block transfer capability with a local d.m.a. controller at up to 40Mbyte/s, incorporation of buffers, interprocessor communication, a local bus for dram compatibility and optional use of Motorola, Intel or National processors. See diagram below.

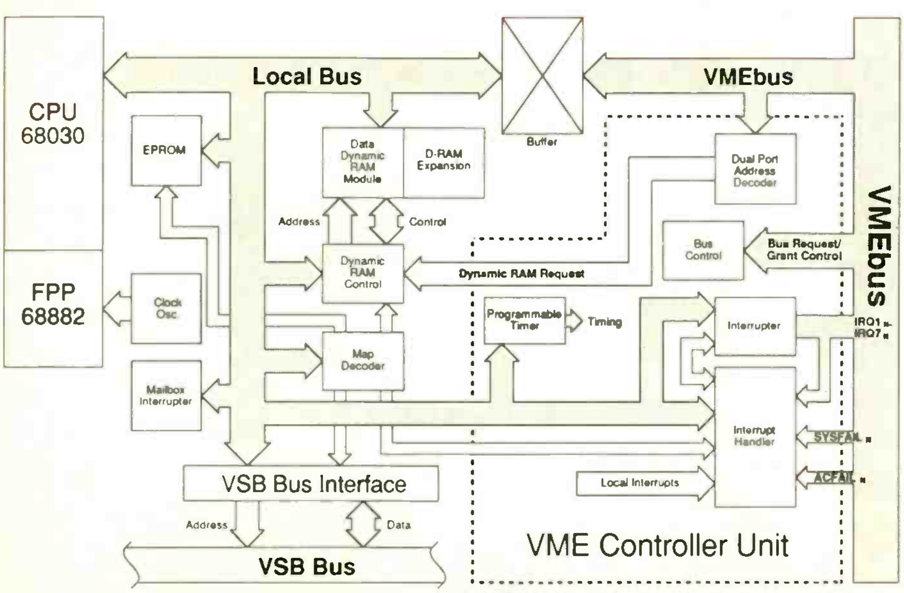
The design initiative came from the VME Technology Consortium, a grouping of 23 US and European manufacturers formed to sponsor development of standard VMEbus interface hardware and who share chip development and production costs. VTC was chosen, says the consortium chairman Jo Ramunni, because it was the only company to meet the timing and cost objectives, as well as agreeing to add the part to its standard product line.

The concerted effort by arch competitors should improve the competitiveness of each of them, says John Hodgson VTC's vice president: "We think the VIC development is the route more manufacturers should consider when costs are beyond each of them."

Application-specific i.c. manufacturers are set to shrink VMEbus circuitry

In their VME/PLUS family, Force Computers has included two cmos gate arrays to increase functionality as well as save on board space. Their first, a 132pin array used on CPU29 and 32 boards, comprises 1600 gates to simply interface between processor, memory and i/o devices, but the second array is a 1.5μm 20,000 gate device with 280 pins. It includes a 32bit dma controller with maximum data transfer rate of 30Mbyte/s using a 32byte fifo for burst transfer whilst a 020 or 030 processor accesses the local system memory or i/o devices.

The chip also includes address map decoding for local processor and dual-ported ram, 16 location monitors, software-controlled handling of interrupts, i/o interface, control of master/slave interface and message broadcast. The message broadcast function allows interrupts of one, some or all boards in a system, by sending the addressed boards an eight-bit message from an eight-stage fifo. Data transfers are completed in less than 330ns which means that maximum theoretical bandwidth is 20 × 3Mbyte/s.



THE EVOLVING PERIPHERAL BUS SCENE

Interfaces resisted change for many years. Until the introduction of small Winchester drives. The storage-module drive interface, first introduced by control data in the early 1970s, ruled supreme in the o.e.m. market. SMDI has changed and adapted since its introduction to increase transfer rate up to 3Mbyte/s and improve status reporting, but it took place at a leisurely pace. Contrast this with the hurly-burly of today, where the pace has picked up to the point where it is hard to keep track of their status.

A device interface has no buffering and it is timing-critical, thus it requires a controller to make it useful to the host system. Controllers may be integrated into the host bus adapter as in open-bus systems such as Multibus and VMEbus, or appear as stand-alone boards, often referred to as bridge controller, packaged in near proximity to the discs to form a storage subsystem.

Three years ago, the chart of interface applications was straightforward. Device interfaces showed a progression of capability from the microprocessor support chips for floppies through ST506/ST412 on small Winchesters. The enhanced Small Device Interface picks up and extends the performance of ST506/ST412. High-performance edsi for 5¼in drives overlaps the s.m.d. interface used on 8in and larger diameter disc drives.

SMD has a transfer rate limitation of 3 Mbyte/s so IPI-2 (intelligent peripheral interface device, specific level 2), which is capable of 10 Mbyte/s was being groomed in the US approved standards committee X3T9.3 to take over the arena for discs with the higher transfer rates.

The situation for control interfaces between host and disc controller was similar at the low end. It was Shugart Associates Systems Interface that was being used to attach the ST506/ST412 drives, and the ASC X3T9.2 standardization effort for the small computer systems interface picked up and bridged the gap to IPI-3 (generic level 3). IPI-3 extends the range and functionality of the block multiplexer channel, which was first introduced on IBM mainframes back in 1964 and has since been adopted by other mainframe manufacturers. This all made for a very tidy picture and it was easy to predict which interface should be used in an application by looking at its application environment.

A lot can change in three years and the picture in 1988 looks significantly different. Three new categories have appeared, all are embedded. The Shugart interface market has been overwhelmed by the progressive application of embedded host bus interfaces and embedded SCSI on desktops – this is a direct result of the dramatic reductions in the cost of l.s.i. protocol chips.

In the search for ever-lower costs on desktop systems, every characteristic of an interface gets looked at. The easiest way to find an interface is to look for a cable and connector. Find a connector and you have found an interface, and a cost item. The pressure to reduce cost on personal computers means that everything gets examined closely.

Incorporating the controller function into the disc drive provides a very real benefit by eliminating cables and connectors. Compaq was the first to introduce a disc drive with the embedded AT bus and IBM has followed suit by adopting the same approach in the PS/2. The Quantum Hardcard is a prime example of how to solve the same problem in the aftermarket.

The explosion in SCSI usage has been fueled by the ready availability of protocol chips. Intense competition between controller companies designing silicon has led to vast improvements in the performance and functionality provided for only a few dollars. The low-cost led SCSI to expand into the lowest end of the market, and the improved functionality resulted in its expansion into higher performance ranges, and increased suitability on midrange computer systems.

IBM introduced IPI-3 on its system 36, 38 and 9370 series, with the device generic command set embedded in its half-gigabyte dual actuator 8in drives. One result of the expansion of embedded drives is a likely reduction in the application of IPI-2 discs in the market. Another factor supporting this is the extended life of SMD. Large discs have not progressed in transfer rate improvements as had been expected – discs with transfer rates of 4.5 Mbyte/s and higher are not expected until Comdex fall.

So the waters are muddied – instead of a simple progression in performance on device interfaces. There are embedded control interfaces to choose from. Embedded drives cover a wider range of performance than device interfaces so they are more suitable to a wide range of applications. Unless a system needs several drives per controller, the embedded drive is an attractive alternative to a separate controller and drives.

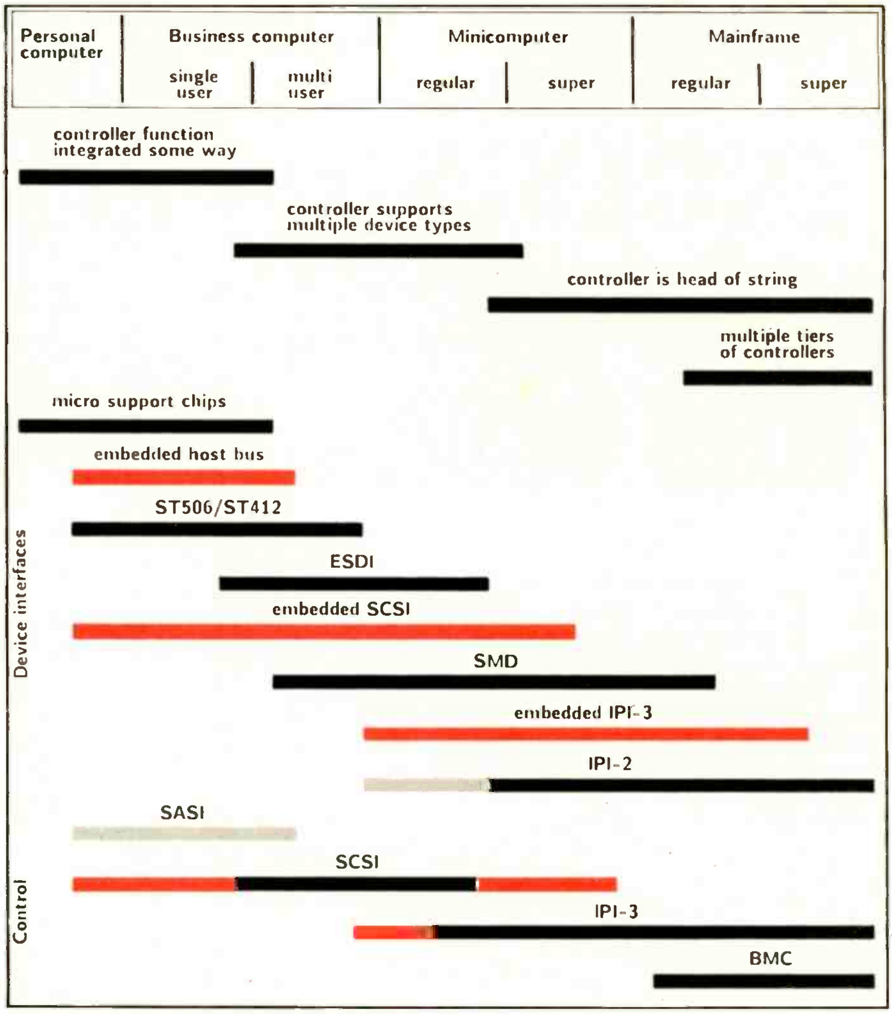
In the area of control interfaces, SASI boards have disappeared in terms of market influence, to be replaced by SCSI. At the opposite end, the dramatic improvements in SCSI performance have extended its application to the top of the mid-range, and this has resulted in reduced expectations of IPI-3 applications in midrange systems.

An analysis such as this is sweeping in its statements and exceptions can be found to disprove almost every one. It is meant only to describe the overall drift of events in the marketplace, and indicate relative rather than absolute progression.

The selection of the most suitable interface for an application was once relatively straightforward, but no more. The range of choices which must be faced and decided upon can be overwhelming to one who is not familiar with the both the application need and the alternatives that are suitable.

If you are going to select peripherals for a minicomputer, take a look at the choices – almost every interface is suitable. Each has its own merits of backwards compatibility, ease of use, future growth potential. Deciding which is best for a particular application requires a thorough examination of the alternatives.

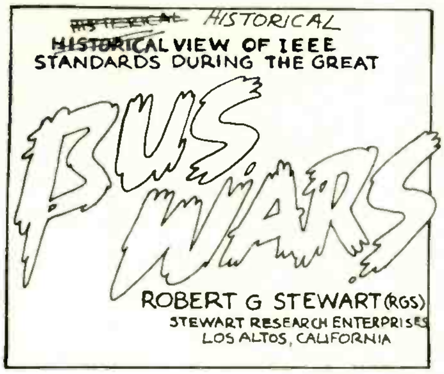
Expedience is the worst basis upon which to make a decision. Interfaces have extended lives, because their integration into a system affects not just hardware, but the operating system, device drivers, utilities support, diagnostics, training, spares, and so on. Once a decision is made it is hard to change because of the costs involved.

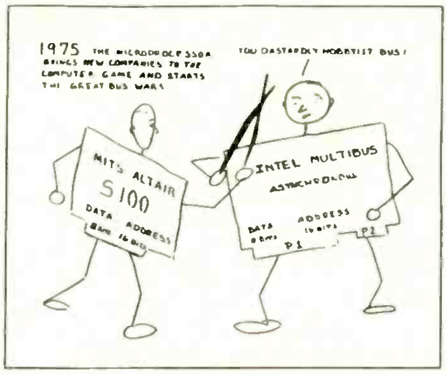


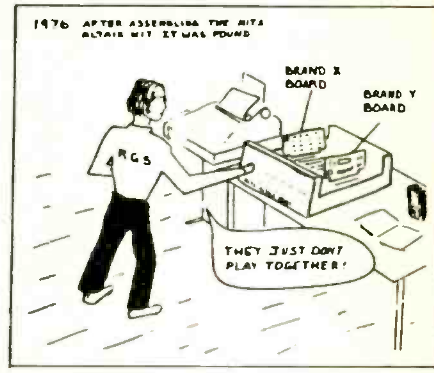
Source: ENDL Consulting. Red indicates growth, grey indicates market shrinkage relative to 1985

Dal Allan, publisher of the ENDL letter and the Busbooks is vice chairman of the U.S. ASC X3T9.2 (SCSI), past vice-chairman of X3T9.3 (IPI) and chairman of the ESDI steering committee.

ENDL is at 14426 Black Walnut Court, Saratoga, CA 95070 (TX: 650-250-1752). The above material was extracted from a presentation to be made at Buscon East, being held in New York 4-6 October. Further details from Buscon, 200 Connecticut Avenue, Norwalk, CT 06856-4990. Tel 203 852 0500. Tx 284997.







WAR AND PIECE

R.G. Stewart, who has followed numerous bus proposals through IEEE's microprocessor standards committee, introduces his pictorial history with an unhappy look at the current scene.

Tolstoy's book dealt with the drama of Russian life in the period of conflict engendered by Napoleon's invasion. The Bus War cartoons presented in *IEEE Micro* two years ago dealt with a decade-long period of conflict between various American and European firms and the IEEE Computer Society's standardization committees. However, in the latter case, the piece at stake was the piece of the action in the microcomputer bus business.

After a period of struggle, peaceful repose restores one's sense of balance. What happened? What will happen? The efforts of the Microprocessor Standards Committee and its working groups have now evolved a long list of bus standards (reproduced on page 805 – ed).

Also, the Computer Society's Computer Communications Technical Committee's working groups, ably guided by Maris Graube, established the widely used IEEE 802 family of local area network standards. In addition to the bus efforts, other standards developed by the MSC include:

Assembly Language	IEEE 694
Relocatable Code Format	IEEE 695
Floating Point Arithmetic	IEEE 754 & 854
Microprocessor Operating Systems Interface	IEEE 855

The 754 floating-point arithmetic standard, embodying many of the ideas of Prof. W. Kahan of the University of California at Berkeley, has been incorporated into most of the fast microchip maths processors developed in the last decade. The high-quality arithmetic provided by IEEE 754 is a breath of fresh air to computer users, who suffered so long from arithmetic asphyxiation caused by the poor subroutine libraries provided by vendors.

Notably missing from the above list of bus standards is the IBM PC bus, a leading *de facto* bus today. Living in Silicon Valley, where many of the earliest personal computers originated, I witnessed the death of many firms when Big Blue decided to get a piece of the action. My sadness was heightened by the realisation of the gross technical inadequacies of the IBM PC: the limited addressing space of the 8088 microprocessor has burdened its users needlessly. The incompatibility problems of many clones or plug-in boards was basically due to the poor bus-transaction protocol. Most buses are either synchronous, using a clock to time transactions, or asynchronous using a strobe – acknowledge handshake between master and slave; the IBM PC bus has a clock, but (and I'm sure you'll think I'm kidding) it was not used to control bus transactions! Rather, a fixed time period was set to time-out transactions. Thus when clones upped the bus crystal frequency, and timed transactions to it, they were no longer compatible with Big Blue's piece of the action. There was no IBM bus specification published to let them know better.

Apple selected Nubus as the backplane bus for its Macintosh II computer using a 68020 microprocessor with 16MHz clock, but Nubus is limited to a 10MHz clock, so off-card transactions must run at half speed. Developed at MIT in 1979 Nubus is older than the other 32-bit buses; I'm sure some of you will think that it should be called Oldbus.

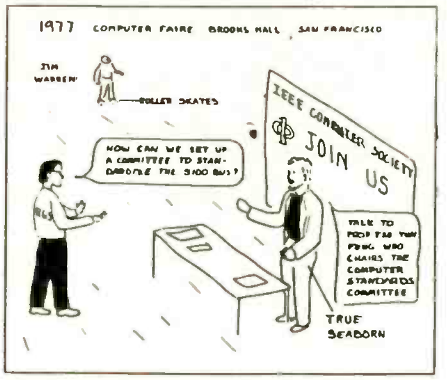
The latest bus being considered for development in the Microprocessor Standards Committee is called Superbus. The leader of a preliminary study group, Dr David Gustavson, is a veteran of the 696 and 896 battles shown in the cartoons, as well as of the efforts which created Fastbus IEEE 960 and IEEE 754. The Superbus group hopes to create a bus with a 1 gigabyte/second data transfer rate, and able to support bus repeaters, distributed caches, and passive or active backplanes.

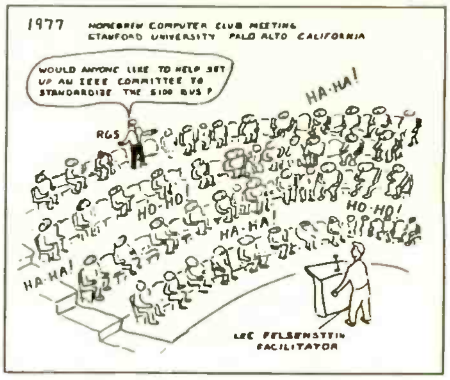
Finally, let me tell you why I am unhappy about aspects of the MSC's standards activities.

- Lack of support by vendors for user-oriented standards, or standards they didn't originate. This is shown by the absence of significant support for the assembly language standard. What does MOVE A,B mean?
- Inability to bring vendors together in 1983 at Wilsonville, Oregon to form a single bus from the Futurebus, Nubus, and Multibus II efforts.
- MSC acceded to virtually every request from industry to promulgate a company bus as a standard. This has led to a proliferation of buses rather the creation of fewer, but more universal buses.
- Significant features of Futurebus are still not widely used. National Semiconductor inadequately advertised its new bus drivers developed by Balakrishnan.
- The MSC Computer Society, IEEE, and even the US Government don't have anything like the clout of the market place. The good don't necessarily win.

But then, I have personally benefitted! This article was prepared on the MITS Altair which led to the IEEE 696 standard. It still works. In fact, it works far better than it did initially! It crashes maybe once a year, not once every ten minutes. I think that getting the infant mortalities out of the chips, together with the 64Kbyte memory card, helped greatly. The change in the bus master-slave transition protocol called for by IEEE 696, wherein one bus cycle is held in a predefined low state to allow driver glitches to settle, also helped to eliminate spurious disc erros. Further, I love the front panel if you have a hardware problem to resolve. My first memory card held 256 bytes, just about enough for a bootstrap loader. I also have an IEEE 696 system with a 68010 processor which has three memory cards, each containing two megabytes and using Dr Matthew Taub's bus arbitration method. So there is progress!

Peace. May a piece of the piece be yours.





VME BUS LOGIC ANALYSER

Single-board VMEbus tracer outperforms general-purpose logic analysers for VMEbus development

State analysis in 32-bit VME bus systems requires an instrument with characteristics found only in a very few instruments on the market, with a prohibitive high price for many development projects. A logic state analyser capable of collecting data on more than 90 channels simultaneously at speeds of at least 10MHz is required, together with powerful trigger conditions and store qualifiers. Features like this, found only in instruments with a price tag of around $30,000, are provided by a new single-board VME bus tracer from VMETRO A/S of Oslo for less than $5,000. The bus tracer eliminates the time-consuming task of connecting more than 90 probes from a general-purpose instrument to the target system. Configuring an instrument with signal names is also eliminated.

The interesting feature of the bus tracer is that it does not require a separate terminal; by means of two RS232 serial ports the instrument may be operated from a terminal normally connected to the system. When the tracer is not needed, it may be placed in a transparent mode, which means that the on-board 68008 microprocessor routes all data directly from one serial port to the other. There is no need for physical connections of measurement probes, having some appeal for non-hardware engineers.

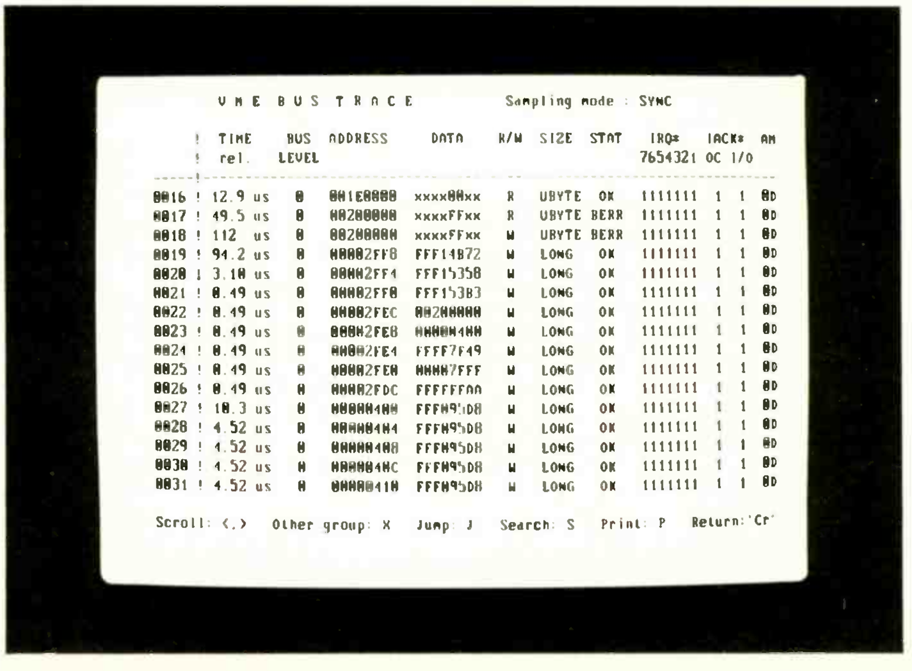
Integrating a logic analyser into the system offers potential for more efficient use of development resources, say VMETRO. If several engineers have to share one expensive instrument, this often leads to situations when a lot of time is spent guessing what is wrong before one takes the trouble of connecting a logic analyser. If this has to be disconnected from another system still more time is wasted, and perhaps another engineer is left with the guesswork.

The module is principally a state analyser with synchronous sampling of bus traffic up to 16MHz. This gives good speed margin, since the maximum practical transfer rate of the VMEbus is 10MHz (40Mbyte/s). Activity on 95 bus signals is sampled, and when a predetermined trigger condition is met, the collected samples are presented to an ASCII terminal. The module contains its own processor and software, and gives 2K words of real-time trace of the data, address and control signals on the VMEbus.

Rather than displaying ones and zeros, many of the control signals are decoded into readable form. This is particularly useful for showing the bus master, transfer size and cycle status. The actual transfer size in each cycle is given by the values of the A_{01}, $\overline{DS_1}$, $\overline{DS_0}$ and $\overline{LWORD}$ signals, and all the different combinations may be difficult to remember. The tracer decodes these signals and presents the transfer size as LWORD, WORD, UBYTE or LBYTE, or in the case of unaligned transfers as $UNAL_3$ or $UNAL_2$.

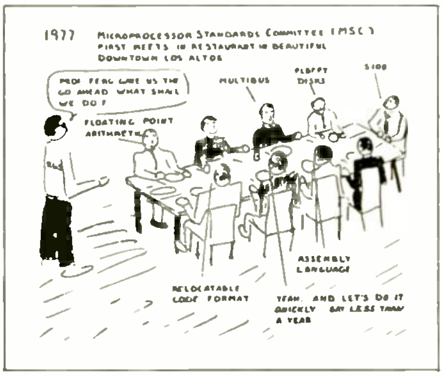
The bus tracer is equipped with an on-board oscillator for asynchronous sampling at 16MHz to provide an expanded, detailed view of each cycle. This does not replace high-speed timing analysers for all hardware debugging, but is very useful for measuring the access time of memory boards and interrupt response time. To a limited extent this may also be used to detect timing errors on the handshake and control signals.

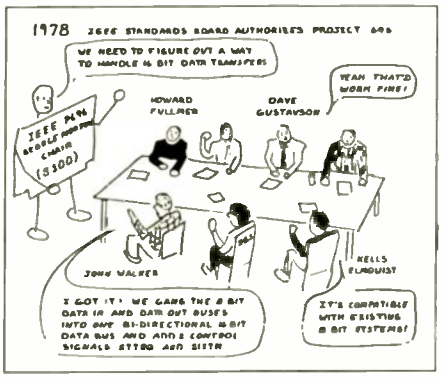
The trigger conditions available are specially tailored to the characteristics of the VME bus. The trigger menu includes the bus master level, a 32-bit address window, a 32-bit data word where any byte may be don't care, and 32 control signals where any signal may be included as 1, 0 or don't care. The inclusion of the bus master level is possible because the bus-grant signals are clocked separately during each cycle. The bus grant lines are valid only during a very short period immediately after the bus arbitration process is finished. If the bus is sampled only when the address and data is valid, this important information would be lost. The VME tracer clocks the bus grant signals


V M E B U S T R A C E Sampling mode : SYNC

	! TIME rel.	BUS LEVEL	ADDRESS	DATA	R/W	SIZE	STAT	IRQ* 7654321	IACK* OC	I/O	AM
0016	! 12.9 us	0	001E0000	xxxx00xx	R	UBYTE	OK	1111111	1	1	0D
0017	! 49.5 us	0	00200000	xxxxFFxx	R	UBYTE	BERR	1111111	1	1	0D
0018	! 112 us	0	00200000	xxxxFFxx	W	UBYTE	BERR	1111111	1	1	0D
0019	! 94.2 us	0	00002FF8	FFF14B72	W	LONG	OK	1111111	1	1	0D
0020	! 3.10 us	0	00002FF4	FFF15358	W	LONG	OK	1111111	1	1	0D
0021	! 0.49 us	0	00002FF0	FFF153B3	W	LONG	OK	1111111	1	1	0D
0022	! 0.49 us	0	00002FEC	00200000	W	LONG	OK	1111111	1	1	0D
0023	! 0.49 us	0	00002FE8	00000400	W	LONG	OK	1111111	1	1	0D
0024	! 0.49 us	0	00002FE4	FFFF7F49	W	LONG	OK	1111111	1	1	0D
0025	! 0.49 us	0	00002FE0	00007FFF	W	LONG	OK	1111111	1	1	0D
0026	! 0.49 us	0	00002FDC	FFFFFFAA	W	LONG	OK	1111111	1	1	0D
0027	! 10.3 us	0	00000400	FFF095D8	W	LONG	OK	1111111	1	1	0D
0028	! 4.52 us	0	00000404	FFF095D8	W	LONG	OK	1111111	1	1	0D
0029	! 4.52 us	0	00000408	FFF095D8	W	LONG	OK	1111111	1	1	0D
0030	! 4.52 us	0	0000040C	FFF095D8	W	LONG	OK	1111111	1	1	0D
0031	! 4.52 us	0	00000410	FFF095D8	W	LONG	OK	1111111	1	1	0D

Scroll: <.> Other group: X Jump: J Search: S Print: P Return:'Cr'



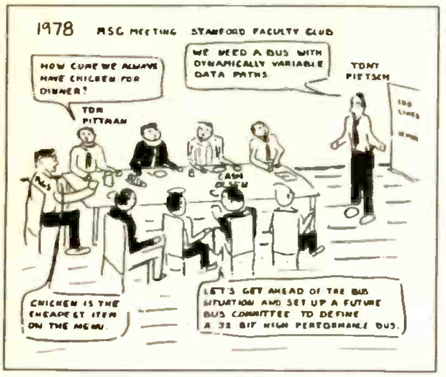


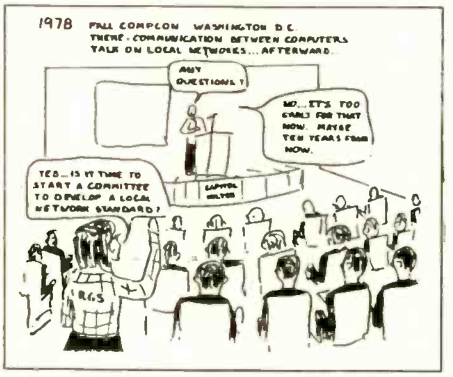
when BBSY goes low so that the actual bus level is available later in the cycle together with the address, data and cycle control signals.

The address on the VMEbus does not include the least significant bit, instead data strobes are used to identify the valid bytes in a cycle. By using the data strobe $\overline{DS_1}$ as the least significant address bit, the VMEbus tracer represents odd byte addresses correctly.

The tracer provides powerful store qualifiers, using the address window, the granted bus level, or a combination of both as qualifier on the collected data. This means that the capturing of bus data is conditional on a valid qualifier so that the trace memory is not filled with uninteresting information. This is particularly useful in multi-processor systems if activity of only one c.p.u. is of interest. By using the bus level of this c.p.u. as store qualifier, only cycles generated on this bus level are stored in the trace memory.

VBT-320 VME bus tracer is equipped with a timer for measuring elapsed time between each sample. This time is stored together with each sample and is presented in a separate column in the trace display. This is particularly useful when a store qualifier is used, since the time between each qualifier sample may be long.





FIELDBUS THE FIELD NARROWS

It is essential that there is a convergence to a single International Standard in the shortest possible timescale to make field bus a success, says Peter Burton of ERA Technology.

The field bus is the lowest level in a vendor-independent industrial networking hierarchy. It allows real-time digital communication between sensors, actuators and local controllers in the process plant or on the factory shop floor. There are currently five contenders for an international standard bus, all using screened twisted-pair cable and all recognising the existence of a bus controller or master. However, there are major differences particularly in respect of media access and modulation/encoding methods. This article provides a brief comparison of the contenders, highlighting both the similarities and the irreconcilable differences between them.

A complete hierarchy of networks in a large industrial process plant might consist of the following levels.

- Plant level; broadbend MAP, communicating between computers, providing video links etc
- Cell level; carrierband MAP, linking controllers and consoles e.g. in the process control room
- Field level; field bus, communicating with sensors, actuators and local controllers in the process plant or manufacturing shop floor.

The higher level networks are of limited value without the field bus, leading to a variety of organisations and groups taking part in the development and standardization activities. Five reached the stage of presenting contenders for adoption as the International Standard, all using screened twisted copper conductors as the physical medium. In alphabetical order these are:

ERA Technology	leading a mainly UK group of vendors and users
FIP Club	a predominantly French group led by EDF and CGEE-Alsthom
Foxboro	US-based control and instrumentation company
Profibus Group	from Germany, led by Siemens
Rosemount	US-based company with military and process industry products.

Comparison of field bus contenders shows use of existing or special solutions

	ERA	FIP	Foxboro Process discrete	Profibus Process discrete	Rosemount Process discrete
Application Layer	MIL-HDBK-1552	FIP	Foxboro	None Published	Rosemount
Logical link Control	MIL-STD-1553B	FIP	Foxboro Extended HDLC	Proway IEEE 802.2	IEEE 802.2
Medium access	MIL-STD-1553B	MIL-STD-1553B (approx)	1553B/Bitbus (approx)	Profibus (token passing)	IEEE 802.4
Physical layer	MIL-STD-1553B (modified for process applications)	MIL-STD-1553B (modified)	1553B (approx) Bitbus (approx)	Profibus f.s.k. Bitbus (approx)	Rosemount f.s.k. phase continuous phase coherent

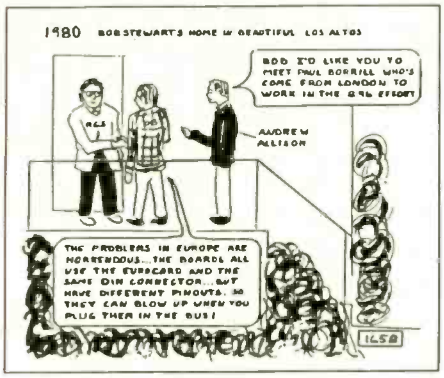
All recognise the existence of a single bus controller or master with back-up as the normal situation in process industries. All agree that MAP is for higher level networks and is not suitable for field bus. There are some variations in bit rates but all have rates of between 200K and 1Mbit/s for a shorter manufacturing industry bus and rates of between 9.6K and 62.5Kbit/s for a longer process industry bus. All make some attempt at providing power via the communication medium with the simultaneous option of use in flammable atmospheres, although the emphasis on these options varies from one to another.

The major irreconcilable differences between contenders lie in two distinct areas

- medium access methods, and
- modulation/encoding techniques.

Media access methods

The ERA, FIP and Foxboro proposals all use central control by command/response time-



division multiplexing. This gives true real-time capability for periodic data transfer, which is the normal situation for a field bus. Time jitter, the major limitation for control applications, is negligible with this approach as periodic timings are pre-determined. For aperiodic transfers, access times are bounded rather than preset.

The Profibus and Rosemount proposals use distributed control by token passing as their base standard and then offer a single initiator sub-set to fit more closely to the field bus application. Token passing is an efficient approach for transferring large blocks of data between computers or controllers, as in its use for higher network levels. In real-time control applications the variations in access time, even for periodic data transfers, is a major limitation.

The IEC field bus working group have recently agreed that only central control is acceptable for a field bus, primarily because of the real-time issues. Token passing can only be considered in single initiator form, which offers no advantage.

Modulation/encoding

The ERA and FIP proposals together with the Foxboro process industry variant, all use baseband signalling with Manchester encoding. This has three major advantages:

- no d.c. component, allowing transformer coupling at the bus
- self-clocking
- inherently high immunity to electrical interference.

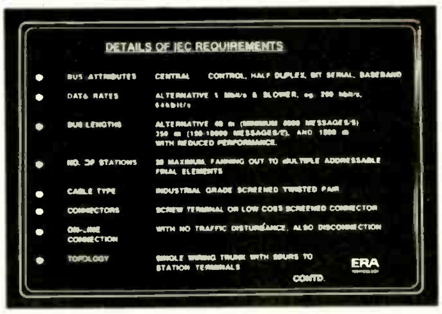
The Foxboro and Profibus manufacturing variants use baseband signalling with NRZ or NRZI encoding. These have the advantage of lowest signal frequency components for a given bit rate, but carry two major disadvantages:

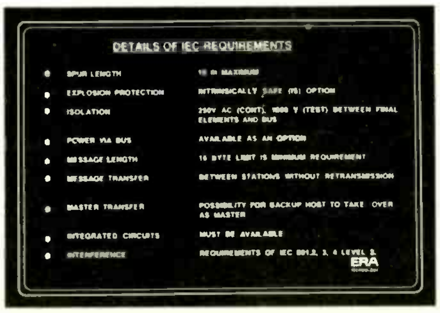
- a d.c. component, and
- no guaranteed clock recovery time.

The field bus provides the lowest level of an industrial network hierachy. It provides communication to sensors, actuators and local controllers on the factory shop floor or in the process plant. It differs from cell-level and plant-level local area networks such as MAP in three ways:

- **true real-time opeation**
- **harsh industrial environment, e.g. electrical interference, flammable atmospheres, and no remote power available**
- **short messages**
- **low cost per node.**

To achieve high component volumes, and therefore low cost, together with interoperability between vendors, requires a common international standard. This is presently in the hands of IEC sub-committee 65C, working group 6, who are due to report on their work in September 1988. Various national committees of the IEC, such as BSI AMT/7 are providing information to the working group. The USA input has been delegated by ANSI to the Instrument Society of America (ISA) committee SP50, who have solicited proposals from the five major development groups.





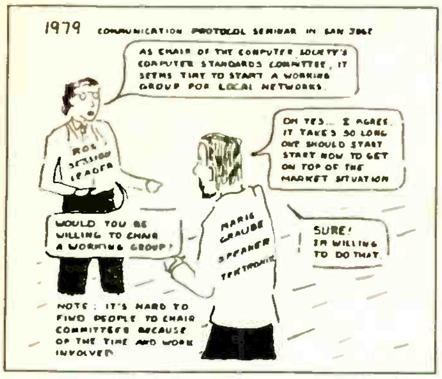
The Profibus proces variant and the Rosemount proposal both use frequency shift keying in either phase-continuous or phase-coherent form. This has the advantage of minimum low frequency component, allowing minimum size of coupling transformer if low bit rates are used. Interference immunity can be equivalent to that achieved by Manchester encoding with good choice or ratio between high and low signalling frequencies. A simple 2:1 ratio will result in much degraded performance in this respect. The disadvantages are

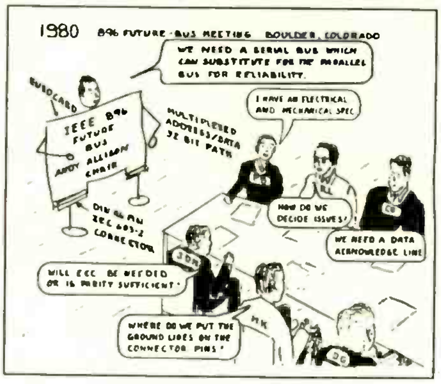
- highest frequency component for given bit rate
- greater component count (requires a modulator).

The IEC field bus working group has agreed that only baseband signalling with Manchester encoding is to be included in the standard. Alternative approaches for process and manufacturing applications have been deemed unacceptable.

It is essential that there is a convergence to a single International Standard in the shortest possible timescale to make field bus a success, says Peter Burton of ERA Technology. At the present stage of preparation of the IEC working groups recommendations for a field bus standard, only two of the contenders are still fully compliant. The others are already in need of modification to follow the progress to an International Standard. It may well be that in the more detailed IEC work at the meetings in June and September, further changes will be required, affecting at least one of the two currently static proposals.

Contenders are progressively developing with the standards activities. Although the information on which this paper is based was obtained through direct participation in the relevant standards committees, the author cannot accept responsibility for any details which have been changed since the last published documents or verbal presentation.





CONTROLLER AREA NETWORK

Bosch's automotive serial bus may find much wider application in the future, according to semiconductor manufacturers

Every car manufacturer in the world is investigating the practicalities of multiplexed wiring. This may mean anything from basic load switching, through medium-complexity communication between sensors and modules, to the high-speed data exchange required between engine management, transmission control and anti-lock brakes.

In its simplest form multiplexed wiring can be used for basic load switching so that only a small number of low current cables will be routed around the car along with one large power cable and the switching is performed at the load itself. In this form, it is debatable whether the system is economical compared to the standard harness due the large number of relays and solid-state switches involved. A more economical solution in vehicles with a high electronic content is to use a high-speed serial bus between modules, intelligent data collection and intelligent load switching. This requires a serial bus which can guarantee passing messages quickly and reliably.

Controller Area Network overview

Controller Area Network is a system developed by Bosch which unlike existing LAN protocols has been optimized for interrupt-driven, real-time environments like automotive. CAN is the main contender to becoming the industry-standard automotive serial bus in Europe. However, for CAN to become an industry standard, the semiconductor companies have to develop the CAN interface chips and to this end Bosch have granted licences to Intel, Philips and Motorola.

The Society of Automotive Engineers have for many years been discussing serial communications for vehicles and have divided the requirements into three classes.

Class A: body control applications such as lights, power windows, mirrors, etc. where speed and integrity of data are not critical.

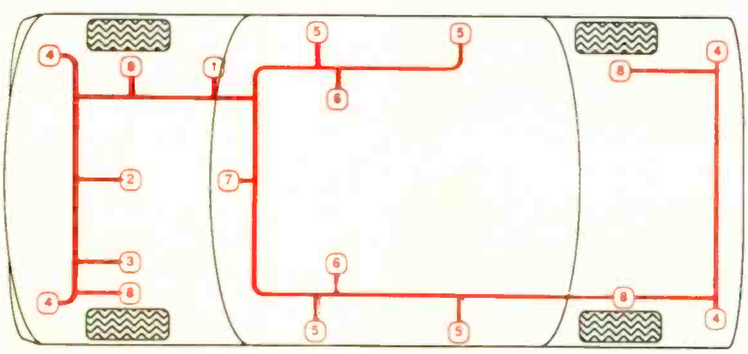
Class B: information transfer between modules and sensors such as temperature or speed sensors to instrument cluster. In this case speed and integrity of data are moderate.

Class C: real-time communication between controllers such as engine management to transmission or anti-lock brakes. In this case high speed and high integrity of data are essential.

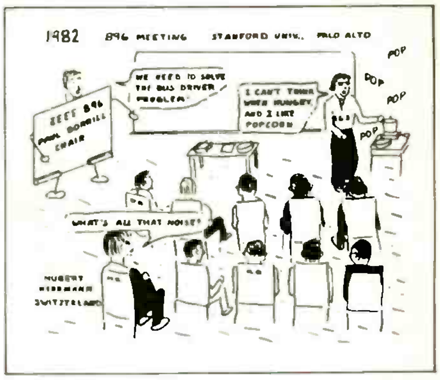
Table 1 shows the SAE definition of the protocols with data rates and latency times. The CAN protocol meets the requirements of all three classes.

The protocol is a multimaster protocol where messages are randomly transmitted on a serial bus. Contention between masters is determined on a bit-by-bit basis in a non-destructive arbitration which results in the highest priority message gaining access to the bus. The protocol supports 2032 different messages of up to eight bytes of data and the highest priority message is guaranteed a maximum latency of 150µs at the maximum bit rate of 1Mbit/s. Other message priorities depend on the level of serial traffic and their relative message priority. Integrity of data is guaranteed through complex mechanisms such as bit stuffing, cyclic redundancy check algorithms and automatic retransmission of erroneous data.

Controller Area Network (CAN) enables the linking of all the control modules within the vehicle by means of a single high speed serial bus which guarantees a maximum latency and a high integrity of data transfer.



1. Driver information centre
2. Engine management system
3. Transmission control
4. Lamp cluster outstations
5. Door outstations
6. Seat control
7. Air conditioning
8. Anti-lock Brakes



CAN protocol

Unlike many serial communication protocols the CAN message contains no information relating to the destination address. Instead the message contains an identifier which indicates the type of information contained in the message. This has several important implications. Firstly, any nodes can be added or removed from the network without any change to the software. Secondly, this means that each node can then decide on the basis of the type of information whether the message is of interest to that particular node. Broadcasts to many nodes are therefore inherent in this system and the data will be consistent in that either none or all of the nodes will receive the message. An additional benefit is that the message may be prioritized on the basis of the type of information it contains. This allows for a multimaster system where any node may send data on the bus when the bus becomes free, and an arbitration scheme will ensure that the highest priority message will always succeed. In addition a node may send a remote frame" which will request another node to return a data frame. The bit-rate of the bus may be any value up to a maximum of 1Mbit/s but must be the same for all nodes on the network and the messages may be of different lengths, as defined by a parameter within the message, up to eight bytes.

Arbitration

As a multimaster protocol the CAN interface must be able to resolve conflicts on the bus due to two nodes attempting to gain access at the same time. This is resolved by means of 'dominant' and 'recessive' bits. In a open-collector network with a pull-up resistor a zero would be the dominant level; the CAN electrical interface does not rely on pull-up resistors but must accommodate electrical conflicts with a given dominant level. A node which requires to transmit will monitor the bus until it becomes free, at which point the node may begin transmission. If two nodes begin transmitting at the same time each will monitor the bus level and compare it

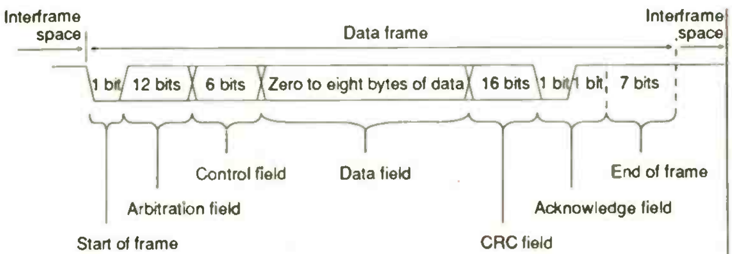


Fig. 1. One data frame consists of seven different fields and can transmit up to eight bytes of data in each frame at 1Mbit/s.

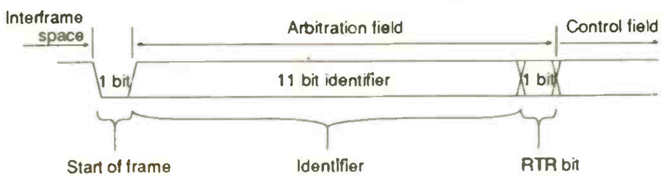


Fig. 2. Arbitration field contains identifier control priority.

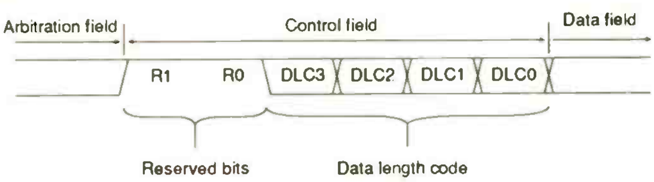


Fig. 3. Control field specifies the number of bytes in the message.

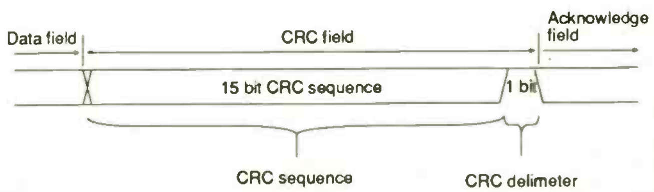
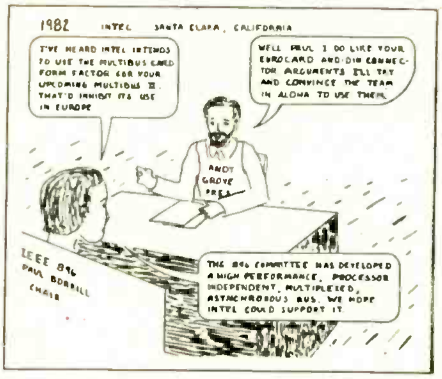
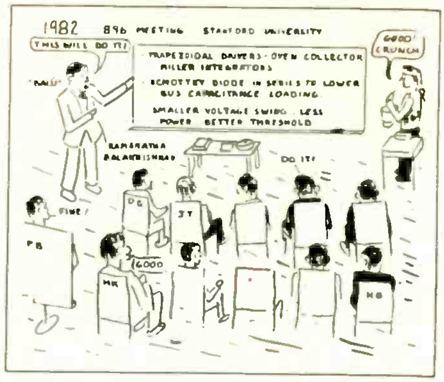


Fig. 4. Crc sequence ensures high integrity of data.





against the transmitted level. If a recessive bit is transmitted and a dominant bit detected then that node will immediately release the bus allowing the other node to continue undisturbed. In this manner the message with the most significant dominant bits will always take priority.

Error detection

In addition to the arbitration technique already described integrity of data is guaranteed by several error detection mechanisms in the form of a c.r.c., bit stuffing, and message frame checks. These ensure that all global and local errors at transmitters are detected as well as most forms of random errors resulting in a probability of undetected errors of less than 1 in 32,000. Any corruption of the message is flagged by the node detecting the error, the message is aborted and is automatically retransmitted.

Data frame

The format for the transmission of a data frame consists of seven fields as shown in Fig. 1. The start-of-frame marker consists of a single dominant bit and serves to synchronize all nodes in the system. This is followed by the arbitration field which contains an eleven-bit message identifier plus a remote-transmission-request (r.t.r.) bit, Fig.2. The message identifier will decide the priority of the message by means of the most significant dominant bits. In a system where zero is the dominant level the lowest binary number would be the highest priority. There is one restriction on the identifier in that the seven most significant bits cannot all be recessive as this signifies an end mark. This allows for 2032 possible message identifiers (000 hex to 7EF hex). The r.t.r. bit merely serves to signify whether the transmission is a data frame (dominant) or a remote frame (recessive).

Next is the control field which consists of

FIRST MOTOROLA BASICCAN DEVICE

Both Motorola and Intel are designing single-chip microcontrollers with a subset of the full CAN implementation on the same chip called BasicCAN. BasicCAN is optimized for class A applications and requires that much of the message handling is performed in software, but it can support classes B and C where the data rate or number of messages is low. One of the first of these to become available from Motorola will be the MC68HC04.

The architecture of BasicCAN is identical to the full CAN with the exception that the management processor is removed and communication between the c.p.u. and the CAN interface is via a dual register with context switch. This means that all bus timings are the same but only a limited number of messages could be received at the full data rate. BasicCAN could therefore communicate on the same bus as a Class C full CAN but is optimized for the Class A applications.

MC68HC04CAN is only the first of many single-chip processors that will be available from Motorola with the CAN interface. It is a low-cost device intended for use in the remote units for intelligent load switching. So that the main controller may communicate with these remote units it also requires a CAN interface and this will be implemented on Motorola's high performance m.c.u. families within the next few years.

– Motorola

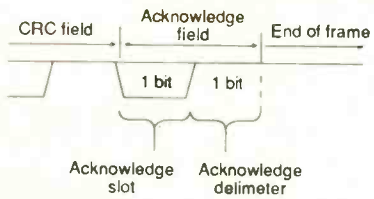


Fig.5. Acknowledge field enables the receiving nodes to indicate receipt.

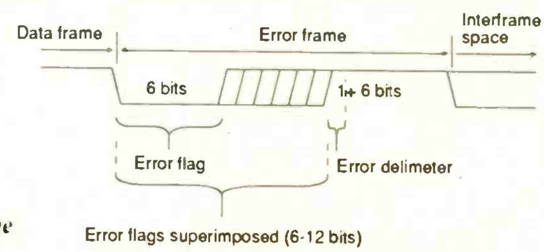
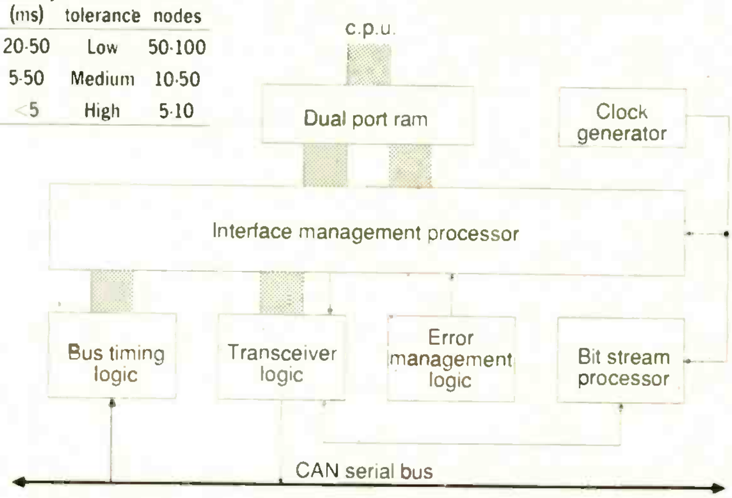


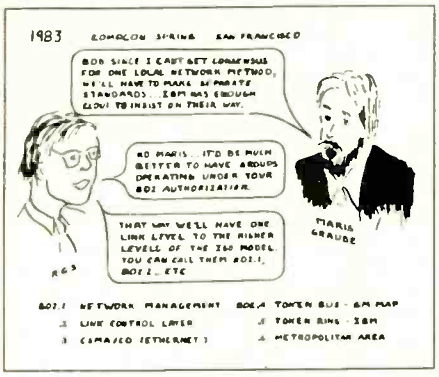
Fig.6. Error frame enables any node to indicate that an error has been detected.

SAE serial bus classification into three levels

	Speed (bit/s)	Latency (ms)	Error tolerance	No. of nodes
Class A	1K	20-50	Low	50-100
Class B	10K-100K	5-50	Medium	10-50
Class C	1000K	<5	High	5-10



CAN architecture: The full implementation consists of six main blocks – Fig.7. The interface management processor is the control device between the CAN interface and the main processor with which it communicates via the d.p.r.a.m. The i.m.p. computes the addresses for communications buffer accesses and manipulates the appropriate control bits required to execute the c.p.u. transmit and receive commands. The bus timing logic provides the synchronization to the line and controls the timing for the sampling of the receive data. The bit stream processor controls the transfer of parallel to serial data and controls the transceiver logic in reception, transmission, arbitration and error flagging.



CAN MAY CHALLENGE 1553BUS

The recently announced CAN v.l.s.i. interface chip from Intel, type 82526, handles the interface between microcontrollers and the serial bus, taking care of transmission, reception, error detection and correction. The 82526 integrates three major blocks on chip: The interface management processor, a quasi-dual-port ram, and the serial interface unit. The 82526 supports programmable transfer rate to 1Mbit/s, broadcast message transfer, up to 2032 different messages, a guaranteed latency time for high priority messages, non-destructive bit-wise arbitration and error handling.

The 82526 implements the three-layer structure of the CAN protocol in hardware to keep the host free from Communications work. The *physical layer* specifies signal level and bit representation. The *transfer layer* offers logic, fault confinement, acknowledgment, message framing and abitration. The *object layer* provides prioritized message handling, acceptance filtering, message buffering and automatic retransmission.

To date, CAN has achieved widespread adoption by car manufacturers and components suppliers and will start to appear on models rolling off the production lines in the early 1990s.

Because of its simple implementation, CAN is now being seriously investigated in other areas of industry. Large companies, who appear unwilling to announce their adoption of CAN, are taking up the network for industrial automation, avionics and defence work.

It is likely that CAN will replace certain uses of 1553 and link up electronics in applications that currently have the wiring complexity problems of the automobile industry. – Intel

six bits. Fig.3. The two leading bits are reserved and are transmitted as dominant bits while the next four bits indicate the number of data bytes to follow (zero to eight). The data field then contains the corresponding number of data bytes and is followed by the "CRC field" (Fig. 4). The c.r.c. sequence consists of 15 bits and the polynomial calculation includes the start-of-frame, the arbitration field, the control field and the data field. The c.r.c. sequence is then followed by the c.r.c. delimiter consisting of a single recessive bit. The next two bits are the acknowledge field and are both transmitted as recessive bits by the transmitter. Fig.5.

Remote frame

The remote frame is a means for one node to request information from another node. One example might be where the dashboard controller requests information on engine temperature from the engine management system. In this case the dashboard controller would send a remote frame to the engine controller which would respond with a data frame.

Bit stuffing

In addition to the afore mentioned rules for error detection any data frame or remote frame is further coded by a method of bit stuffing. This process applies only to the start of frame, arbitration field, control field, data field and c.r.c. sequence. If the transmitter detects more than five consecutive bits of the same level the sixth bit is automatically complemented. Conversely when decoding the data the reverse is applied. This technique allows the error flag to be implemented in the form of six consecutive dominant bits and all nodes will recognise this as an error.

Error frame

The error frame is a means by which any node in the system may indicate to all others the detection of an error condition. The error flag consists of six consecutive dominant bits and is recognised by all other nodes as an error condition due to violation of the bit-stuffing rules. Due to different error flags being superimposed the flag may consist of up to a maximum of 12 dominant bits. On detection or transmission of an error flag, all nodes will monitor the bus for a recessive bit and will then transmit a further six recessive bits before continuing (Fig. 6).

Overload frame

An overload condition will occur if a node in the system does not have time to process the data received before the next frame is received or if one of the nodes does not behave the rules on interframe spaces. Under these conditions an overload frame will be generated which looks very similar to the error frame.

Interframe spacing

To control and synchronize transmissions all data frames or remote frames must be separated by an interframe space. Conversely error frames or overload frames may start immediately after the end-of-frame marker. The interframe space consists of an intermission and a bus-idle condition. The intermission comprises three recessive bits and the bus will then remain idle until one of the nodes begins a transmission.

By Pat Jordan, systems engineering manager for single-chip m.c.us at Motorola's European Semiconductor Group.

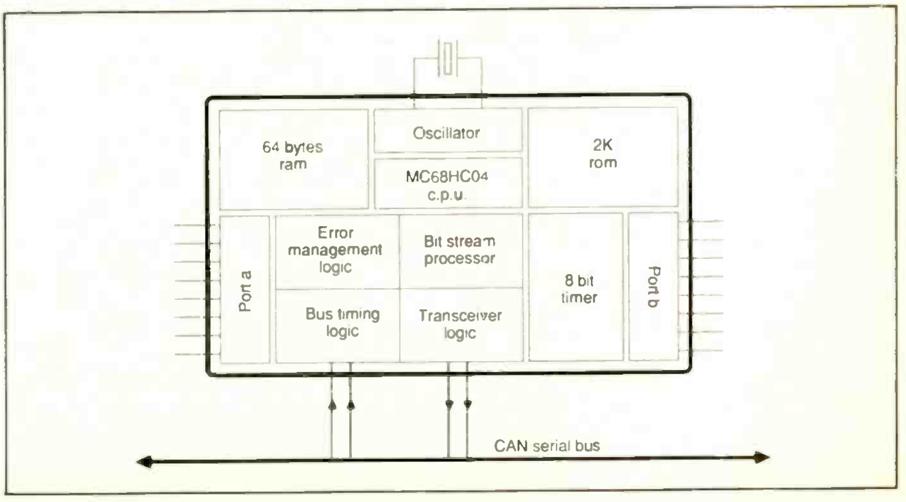
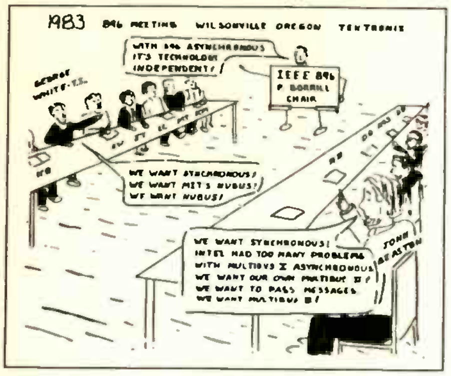
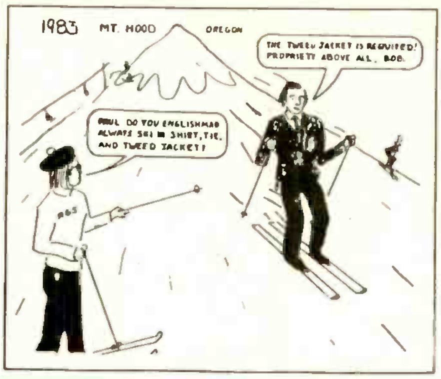


Fig. 7. Architecture of the CAN interface minimizes processor overhead by implementing in hardware all address recognition, c.r.c. calculation and formatting.





SINGLE CONCEPT UNIFIES THREE SYSTEM BUSES

Based largely on Multibus, Siemens approach provides not only a migration path along its 8, 16 and 32bit structure but also three-bus concurrency, writes Andrew Tompkins

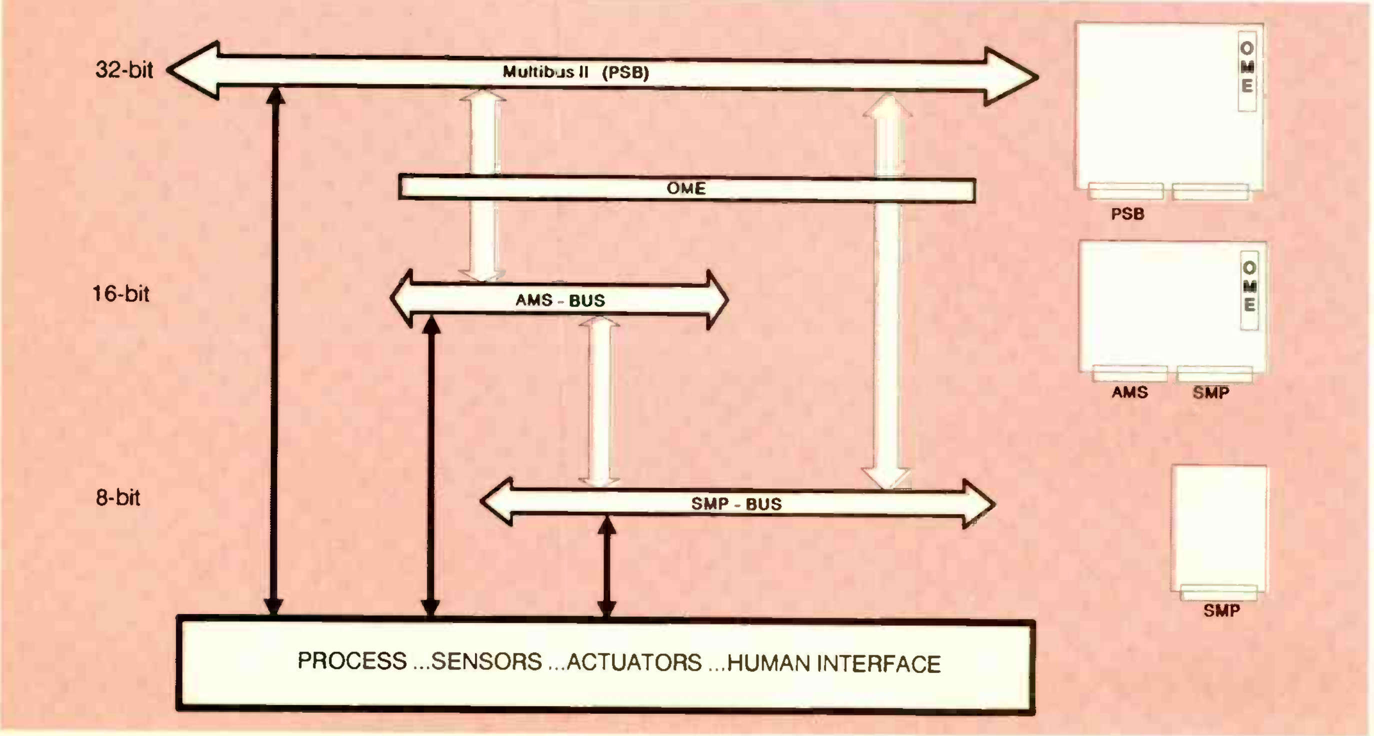
The system designer has a number of difficult choices ahead when designing a new system based on standard buses. Can I find a solution to my problem from available board products? Will the cost of the system be acceptable? Will boards from different vendors interpret correctly? Will all the vendors offer support for their boards and will they be around to support their products in ten years time? Will the chosen configuration be easily upgradable as new facilities are required? Can I find software which will run together on the system to drive all the peripheral and i/o cards.

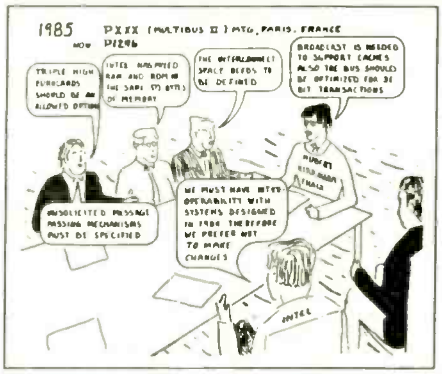
These sorts of questions provide a lot of unknowns to the designer which can seriously affect the timescales for a project. As a systems user for both data processing and industrial automation applications, Siemens is well aware of these potential problems and as a supplier has provided a multiple bus hierarchy which overcomes most of these uncertainties. As a 60 billion DM company, established in 1842 it can offer stability and a range of products difficult to match from any other supplier.

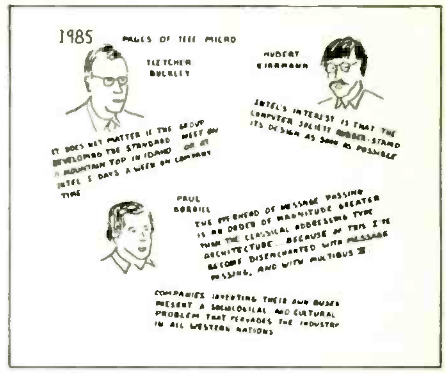
Three Eurocard buses have been incorporated to provide the backbone to the system architecture: 32-bit Multibus II, Siemens 16-bit AMS (Multibus I based) and 8-bit SMP buses, see panel.

A common theme runs through all three bus systems. Physical, hardware and software compatibility are necessary for trouble free interoperation. All the buses are based on Eurocard from factors with 96-pin DIN connectors and racking allows all types of

Triple backplane hierarchy gives freedom of choice for interfacing at any level.







board to be intermixed in the same chassis. This explains the reasoning for adopting Multibus I electrically but physically changing it to a Eurocard format and getting it standardized. The hardware is based on Intel c.p.u. architectures, predominantly based on processors and microcontrollers. Many peripheral components are as complex to use as the c.p.u. itself and so there is also a common range of v.l.s.i. peripheral chips used throughout to simplify interfacing. A common hardware base enables a common software platform to be achieved. For real-time systems RMOS can be used on any of the three buses, with message passing support available for Multibus II. A universal monitor can run on all the c.p.u. cards and device drivers are available for the peripheral cards.

There are about 150 boards available from a single source. All the buses are based on open standards so special boards can either be obtained from other vendors or, if necessary, designed in house. This flexible system approach based on some common standards enables the system designer to choose freely amongst the available products to achieve his desired system, knowing that the products are hardware and software compatible.

The ability to freely migrate across bus structures means that the most economical solution can be found to a particular problem. The broad base of SMP boards brings a wide range of i/o functions to the AMS or Multibus II buses which would take many years to develop if the i/o capability was placed on the board directly. Additionally, the cost to the vendor of manufacturing and stocking a multitude of different types of complex Multibus II boards would increase the price of the board prohibitively as well as increasing the cost of spares holding to the end user. Hence it makes sense to keep the i/o part of the system in small modular units which can be readily tailored to meet specific requirements.

Two examples show how the AMS bus uses the SMP bus as an i/o bus and how the Multibus II bus may interface to the AMS and/or the SMP bus.

AMS to SMP link

The AMS bus fits completely within one 96-pin DIN connector allowing the second connector to be used for the SMP signals. All the AMS c.p.u. boards have the SMP bus interface allowing further memory and i/o boards to be connected for exclusive use by the host. As the SMP bus can be accessed without bus arbitration the boards can be addressed directly as an extension of the host board with memory, i/o, and control functions. The example below shows the AMS bus in a multimaster configuration with one AMS board linking into the SMP bus as a local bus extension.

TRIPLE BACKPLANE HIERARCHY

● Multibus II (IEEE 1296) provides the highest capability with 32-bit support for up to 20 bus masters and using a synchronous 10MHz bus clock to enable a reliable 40Mbyte/s (32Mbyte/s sustained) transfer rate. In addition to performance, Multibus II, also offers many features such as automatic configuration, built-in diagnostics, parity checking and recovery, and message passing all of which increase reliability and reduce system downtime.

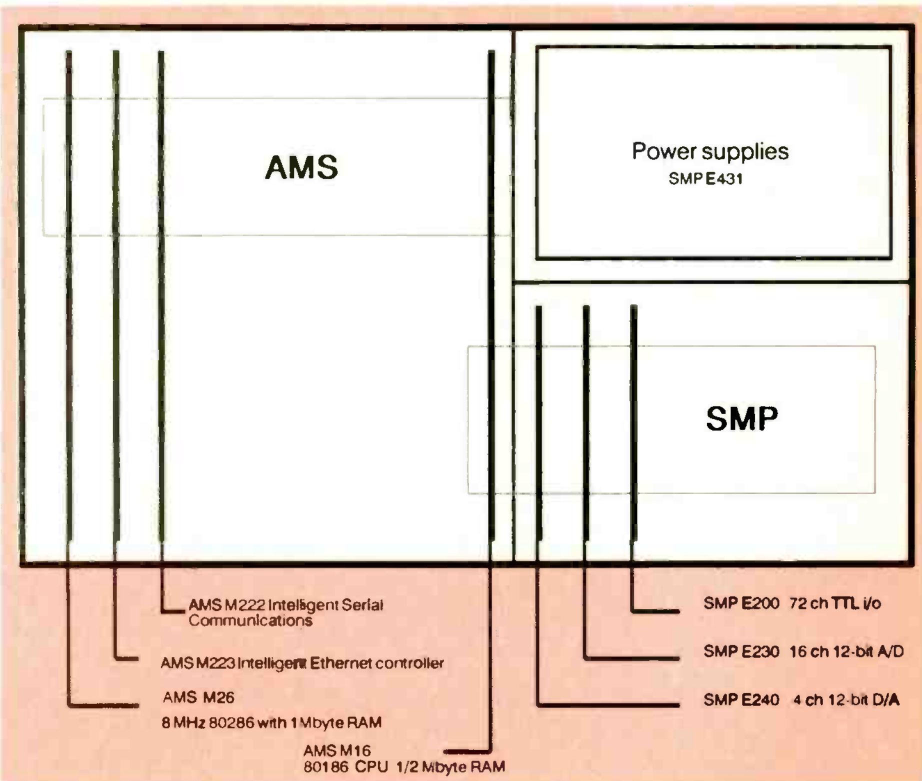
● The Advanced Microcomputer System bus is electrically identical to Multibus I but was repackaged onto a double-height Eurocard standard. In 1984 the bus was accepted as the IEC standard 47B.

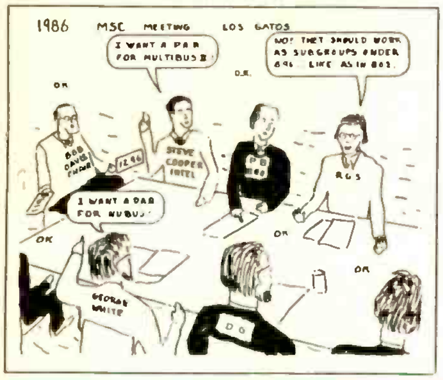
● SMP bus is a mono master synchronous bus with eight-bit data and 1Mbyte address capability based on a single-height Eurocard. The bus is now 12 years old with over 100 different products available from Siemens alone and around 25 other European manufacturers making boards.

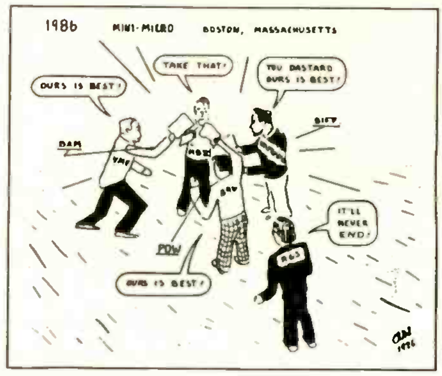
Multibus II AMS and SMP

The Multibus II bus can be linked to the AMS and SMP buses in a functionally similar fashion but the interconnection needs to be more complex so that the performance of the Multibus II c.p.u. is retained. The Multibus II signals are heavily multiplexed and all fit onto one DIN connector thus providing the potential to bring the SMP bus out onto the second connector. However, the high performance processors available today such as the 20MHz 80386 will require many wait states to be inserted when communicating

The AMS bus is used as a multiprocessing system bus whilst the SMP bus acts as a local bus to the AMS M16.







with a relatively slow i/o device which will adversely affect the c.p.u. performance.

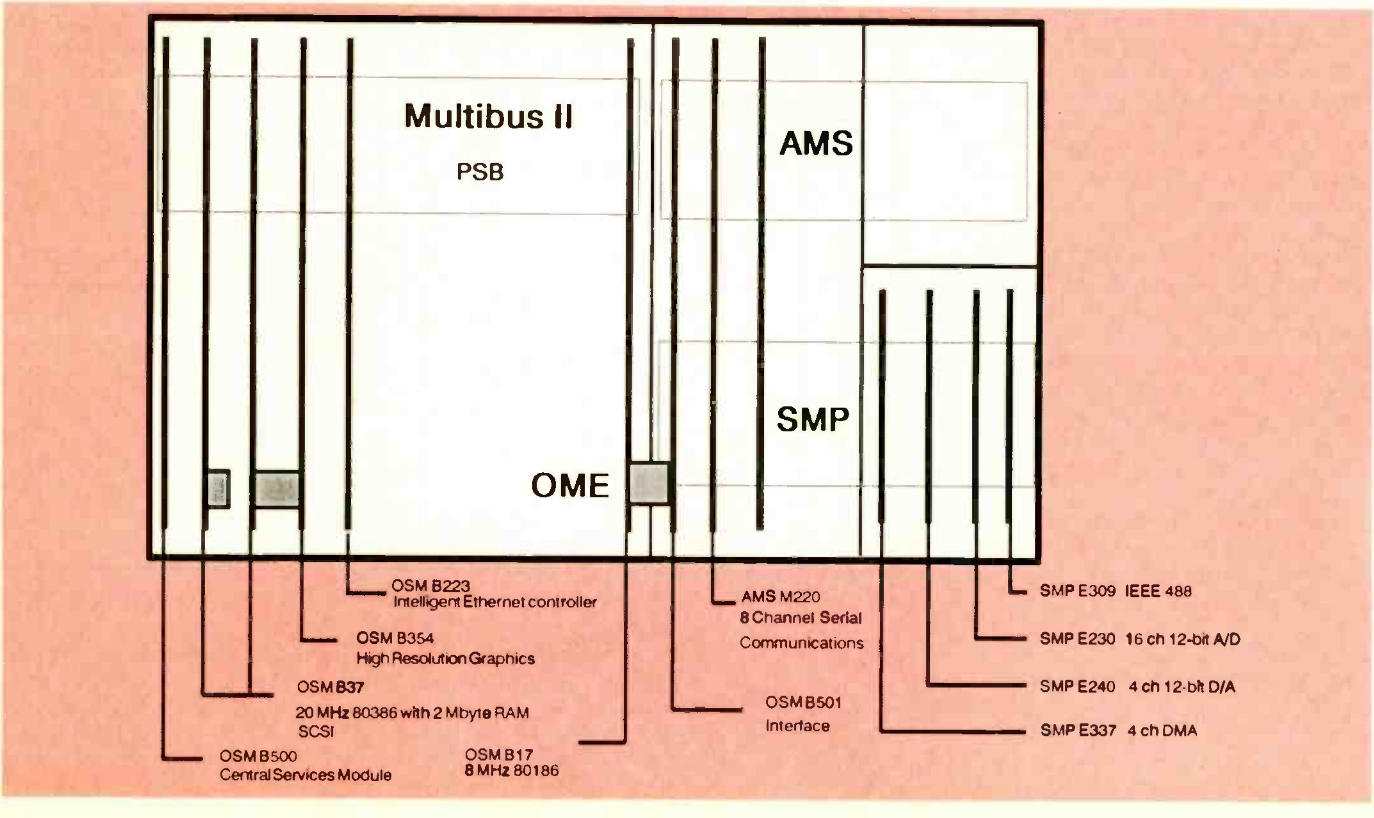
To overcome this, the Multibus II board is linked through the OSM-B501 board with a triple ported 64Kbyte communications memory in the AMS and our buses, which enables the Multibus II board to run at optimum speed with memory mapped i/o. The Multibus II c.p.u may access the AMS and SMP buses directly, while accesses to the Multibus II c.p.u. are performed via the communications memory. The SMP bus may contain a master such as a d.m.a. controller to provide a zero wait state interface to the communications memory. The OSM-B501 additionally offers interrupt controllers to handle up to 16 non-vectored interrupt requests from the SMP and AMS buses to provide full interrupt support for each bus. The memory and i/o mapping are also controlled by jumpers and board specific registers on the OSM B501.

Extending Multibus II with the OME bus
The Multibus II host board is linked to the OSM-B501 via the OME interface. This is a 96-pin DIN connector mounted directly on the new generation of Multibus II OSM B17 (8MHz 80186) c.p.u. and OSM B37 (20 MHz 80386) c.p.u. cards. The OME was designed to provide a high performance local bus extension with up to 64Mbytes of direct memory access and as an interface to high performance modules such as high resolution graphics. The bus contains RAS and CAS signals for dram access, four d.m.a. and interrupt request and acknowledge signals as well as a demultiplexed address and data bus with the usual handshake signals. This powerful interface allows up to four daughter boards to be cascaded together.

Real-time operating system
The RMOS real-time multitasking multiprocessing operating system unites the 8086/186/286/386 c.p.us on all three buses with a standard modular and easily configurable software platform which is available in both real and protected modes for the 80286 and 80386. Message-passing support is available for both real and protected versions of RMOS to support unsolicited and solicited transfers thus allowing the full bus bandwidth to be exploited on Multibus II.

The standardization and degree of interoperability of software with multiple buses can currently only be achieved by buying through one vendor who can provide support in all areas. The Multibus II IEEE 1296 standard already incorporates some software standards to ease board recognition and configuration which are essential for geographic addressing to be performed between different manufacturers.

Standardized software interfaces for device drivers to the operating systems are currently being developed, but software standards for peripheral controllers that will satisfy the requirements of the many manufacturers and users of Multibus II will need careful consideration and agreement.



The OSM B37 board uses the OME bus to interface, via the OSM B501, to both the AMS and SMP bus. The SMP bus is used with a d.m.a. controller for fast transfer of data to the host c.p.u. of up to 16 channels.

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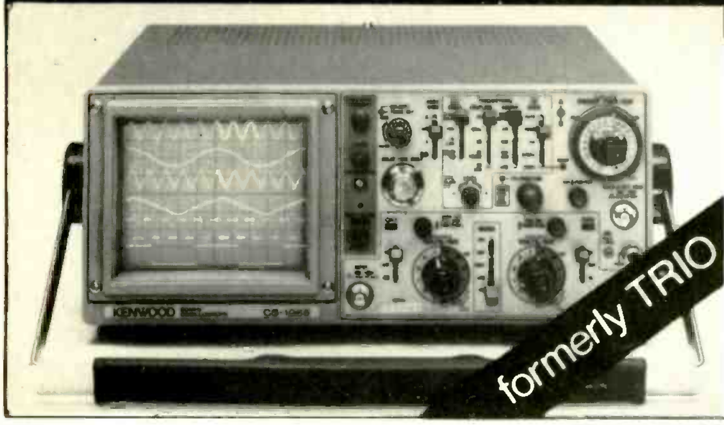

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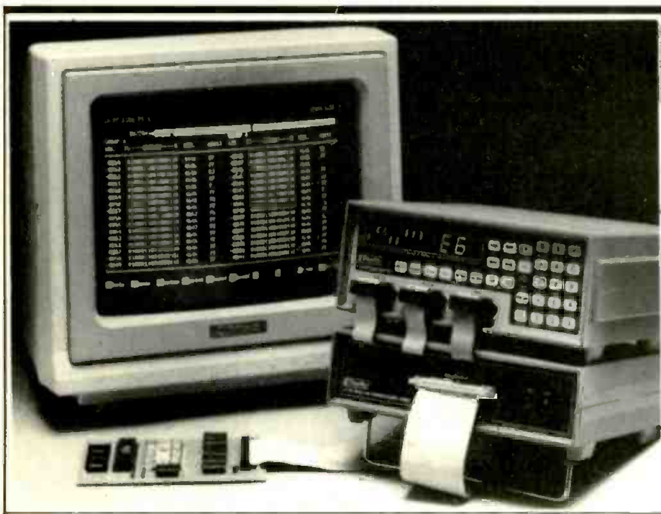

low-cost logic analysis

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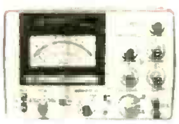

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Pioneers

20. Michael Faraday (1791-1867): 'patron saint' of electrical engineers.

W.A. ATHERTON

He had only an elementary education, "little more than the rudiments of reading, writing and arithmetic at a common day school", as he himself described it. Yet the Encyclopaedia Britannica has called him "possibly the greatest experimental genius the world has known". Many equally generous tributes have been paid to this unique man. He has been called the patron saint of electrical engineers and Humphry Davy's greatest discovery. The testimonial I like best, though, was spoken by a German professor, F.W. Kohlrausch, and contains just four words: "He smells the truth". The "he", of course, was Michael Faraday.

Most of Faraday's long list of scientific discoveries lie in the fields of chemistry and electricity, and they took him into some odd corners. Of his 158 published papers, about half relate to electrical science and a third to chemistry. The rest range over a variety of topics and include one, "On holding the breath for a lengthened period". Another, "Change of musket balls in shrapnel shells: Action of gunpowder on lead", almost sounds like a defence contract. Trinity House asked him to judge the viability of arc lights for lighthouses, the National Gallery in London sought his advice on the preservation of art treasures, and he was even consulted over an idea for using hydrogen sulphide for gas warfare.

His contemporaries said he was a kind, gentle and proud man who had a simple manner and attitude.

As well as being one of the world's greatest scientists he was also a committed Christian and that must say something about those who profess that science and religion do not mix. His personal faith helped shape his philosophy and led him to accept the unity of the universe and the fallibility of men. Together these encouraged him to speculate and to publish what were virtually scientific heresies – including his famous curved lines of force. From such speculations came the beginnings of electromagnetic field theory. In 1852 his agnostic friend John Tyndall wrote, "I think that a good deal of Faraday's week-day strength and persistency might be referred to his Sunday Exercises. He drinks from a fount on Sunday which refreshes his soul for a week."[1].

It would be nice to think that all electrical and electronic engineers know that Faraday made what is possibly the most important discovery in electrical science: that of electromagnetic induction. (It was discovered almost simultaneously by Henry in America.) Many know that he established the basic laws of electrolysis. But his great experimental skills and persistence, and his non-mathematical reasoning, also led him

Institution of Electrical Engineers.

to electromagnetic rotation (the basis of electric motors), proof that the different 'types' of electricity (frictional, electrostatic, voltaic, etc.) are manifestations of the same basic phenomena, to a new theory of electricity, the dielectric constant, the rotation of the plane of polarization of light, and the start of classical field theory and the electromagnetic theory of light. He established several of our common terms, including electrode, anode, cathode, electrolysis, electrolyte, paramagnetism and diamagnetism (which he discovered) and, I believe, dielectric. True to his character he chose these terms very carefully and with the help of William Whewell of Cambridge University.

Faraday played a major role in a pattern of experimentation and reasoning on electromagnetism and related sciences which began with Oersted and culminated with Einstein and Planck.

Besides that, chemical engineers are proud of him too – for producing higher-grade steels (1818), for making the first compounds of carbon and chlorine (the first "substitution" reactions, 1820), and for discovering benzene (1825). He was also an outstanding public lecturer: the annual IEE lecture to young people is named in his honour.

A PLEA FOR PLAIN LANGUAGE

In 1857 Faraday, aged 66, wrote to the 26-year old James Clerk Maxwell as follows:

"There is one thing I would be glad to ask you. When a mathematician engaged in investigating physical actions and results has arrived at his conclusions, may they not be expressed in common language as fully, clearly, and definitely as in mathematical formulae? If so, would it not be a great boon to such as I to express them so? – translating them out of their hieroglyphics, that we also might work upon them by experiment. I think it must be so, because I have always found that you could convey to me a perfectly clear idea of your conclusions, which, though they may give me no full understanding of the steps of your process, give me the results neither above nor below the truth, and so clear in character that I can think and work from them."

EARLY LIFE

Michael was the third of four children of James and Margaret Faraday. He was born on 22 September, 1791, at Newington, now part of Southwark in London but then in the country. His father, a blacksmith, had moved south from Yorkshire in search of work in the year that Michael was born. His ill health meant that the family was poor. Michael later recollected that he was once given a loaf of bread to sustain him for a week.

At 13 the young Michael became a newspaper delivery boy for a Mr G. Riebau, a French *émigré* who had fled the Revolution. Riebau sold books as well as newspapers, and he bound books too. Faraday was soon an apprentice bookbinder and so gained access to a large and ever-changing library.

Some of those books fired his love for science. One, Jane Marcet's "Conversations on Chemistry", remained a life-long favourite. Another, the Encyclopaedia Britannica, introduced him to electricity through an article by James Tytler, a "scientific heretic" who saw electricity as a vibration rather than as a flow of particles[1]. How much this unorthodox viewpoint influenced Faraday's later approach to scientific reasoning is a matter for interesting conjecture.

Meanwhile, while Faraday bound books, a group of young men had begun to meet in London to discuss scientific topics. They called themselves the City Philosophical Society. Faraday came across them early in 1810 and their lectures extended his education. In 1812, he was able to attend public lectures given by the great Humphry Davy. The tickets were a gift from one of the bookshop's customers – someone to whom electrical engineers should be grateful, for he provided an opening which Faraday turned into a career.

In October 1812, Davy was temporarily blinded in a laboratory explosion and Faraday was recommended as a temporary help. In December Faraday sent Davy a bound volume of the notes he had taken of Davy's lectures. The next March, when the Royal Institution, at which Davy was employed, sacked a laboratory assistant for fighting, Davy recommended Faraday for employment. So began, on 1 March, 1813, an association which was to last all of Faraday's working life[1].

Thus Faraday became assistant to Davy, one of the greatest scientists of the day. The respect Davy commanded may be judged by the welcome he received in Paris when he toured the continent in 1813-14, accompanied by his wife and by Faraday. Despite the conflict between Britain and France he was given safe passage and warmly received.

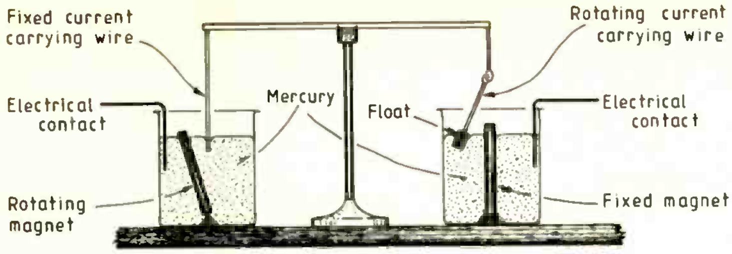

Fig.1. Faraday's apparatus for demonstrating electromagnetic rotation (simplified).

Faraday's early work at the Royal Institution was mainly concerned with chemistry. But in 1821 the editor of *The Philosophical Magazine*, a major scientific journal, asked him to review the flood of theories and experiments which had followed Oersted's discovery of electromagnetism and to separate fact from fiction. Somewhat reluctantly Faraday agreed.

His enthusiasm was soon aroused however; and, as usual, he repeated others' experiments with great care rather than merely accept their results. Whilst tackling Oersted's experiments he used a small magnetic needle to plot the pattern of the magnetic force around a current-carrying wire. He soon realised that a single magnetic pole should rotate around the wire. Figure 1 shows his elegant experiment which showed the truth of this – the first conversion of electrical energy into mechanical motion and the basis of the electric motor (3, 4 September, 1821). On Christmas Day he showed his wife Sarah (they had married that year) and his brother-in-law that a wire could be made to rotate using only the Earth's magnetism. "Do you see, do you see, do you see, George?" asked Faraday in his excitement[2]. "I shall never forget the enthusiasm expressed in his face and the sparkling in his eyes", his brother-in-law wrote later.

This, his first great success, also brought him the unpleasant and unjust charge of stealing the idea without acknowledgement. W.H. Wollaston, with Davy, had tried a somewhat similar but futile experiment some months earlier. Two years later Faraday further aroused Davy's jealously by liquefying chlorine, something at which Davy had failed. In 1824 Davy unsuccessfully opposed Faraday's election to the Royal Society, but Faraday never repaid even this slur.

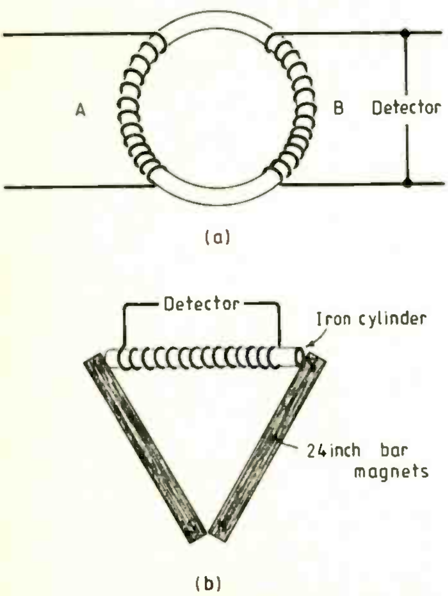

Fig.2. (a) The ring experiment, electromagnetic induction; (b) conversion of magnetism into electricity. Both 1831.

ELECTROMAGNETIC INDUCTION

Two years after Davy's death, in 1831, came Faraday's discovery of electromagnetic induction and the culmination of an 11-year search by scientists to find the reverse of Oersted's discovery: to produce electricity from magnetism.

Two coils of wire had been wound on opposite sides of a soft iron ring six inches in diameter. One coil was connected to a battery and the other to a simple galvanometer (a wire passing over a magnetic needle). Nothing happened whilst the battery was either in circuit or out of it, as others had observed previously, but the needle was deflected whenever the battery connection was made or broken. Whenever the primary current started or stopped it induced a current in the secondary. Faraday's breakthrough was the outcome of great mental exertion and very careful observation. It was 29 August, 1831.

One 24 September, magnetism was converted into electricity. A wire helix was wrapped around an iron cylinder and the wires led off to a current detector. Two 24-inch bar magnets were placed so as to magnetize the iron cylinder. Whenever the magnetic circuit was made or broken a momentary current was generated. Later a current was generated by pushing a bar magnet into and out of a wire helix.

Faraday reported his results to the Royal Society in London and to the Academy of Sciences in Paris. Soon small hand-driven magneto generators were being produced by others. Gauss and Weber used one to power their experimental electromagnetic telegraph from 1835.

Precisely what process of thought led Faraday to near-perfect experiments for these discoveries is a matter for historical detective work.

It is known that Faraday was unhappy with the contemporary theories of electricity and magnetism and in particular with the concept that electric current is a simple flow of particles. He believed that the presence of what we now call electric or magnetic fields put the conducting medium into a state of strain. His lines of force represented the lines of strain. Vibrations in those lines would somehow transfer energy without transferring matter. In parallel with this he took an interest in acoustics, especially in making flat plates vibrate in resonance to other vibrating plates – a sort of acoustical induction. He studied this topic up to just six weeks before his discovery of electromagnetic induction. Almost certainly he saw an analogy between acoustics and electricity.

Later he developed his ideas into a general theory of electricity and even extended them into a probing attack on the transmission of light though a vacuum ("Thoughts on ray vibrations", 1846). Here he saw radiation as a "high species of vibration in the lines of force". Later (1852) he speculated that lines of magnetic force existed as strains, not in material bodies, but in "the condition of space free from such material particles". Many historians of science see Faraday's "Thought on ray vibrations" as the embryonic form of Maxwell's electromagnetic theory of light. Indeed Maxwell's first paper of the series which led to his theory was a mathematical treatment of Faraday's lines of force.

Faraday, whose education equipped him with almost no mathematical skills, commented, "I was at first almost frightened when I saw such mathematical force made to bear on the subject, and then wondered to see that the subject stood it so well". He even wrote to the young Maxwell praising his skills at translating mathematics into clear everyday English.

By the late 1830s Faraday himself had been strained to the limit by his mental exertions and he suffered what has variously been called exhaustion or a nervous or mental breakdown. It has also been suggested that he was being slowly poisoned by the mercury he used for electrical connections. It was five years before he fully recovered, if indeed he ever did fully recover.

Between 1861 and 1865 Michael Faraday retired from his various duties and spent his remaining years under royal patronage in a house provided by Queen Victoria near Hampton Court. Since his illness of the late 1830s he had suffered increasingly from intermittent loss of memory. His last few years were spent in a state of mental confusion. He died on 25 August, 1867.

His ability to "smell the truth" led him to search without success for other physical phenomena which he believed to exist. Many of these have since been found, including magnetostriction and the Kerr and Zeeman effects. Another, a link between electricity and gravity, we have yet to find. Maybe one day it will become yet another Faraday Effect!

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Next in this series of pioneers of electrical communication: Alec Reeves, inventor of pulse code modulation.

RADIO COMMUNICATIONS

Rural radio projects

Low-cost radio systems, both satellite and terrestrial, are emerging in new forms to provide thin-line communications for rural areas for both developed and developing countries in circumstances where more conventional telecommunications are often ruled out on grounds of costs and lack of technical support. A major problem with sophisticated new technology is that systems have to be paid for in "hard" currencies whereas the resulting revenues are collected in "soft" currency.

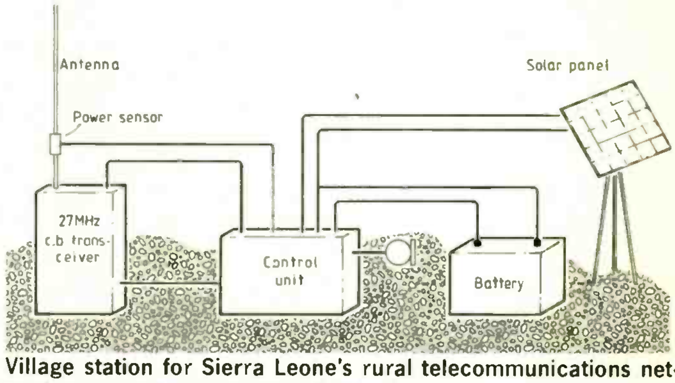
The IEE's first International Conference on Rural Telecommunications, attended by over 200 delegates from more than 30 countries, underlined the problem of providing telecommunications for the extensive rural areas of such countries as Canada, Sweden and Ireland, where rural or remote areas may depend on domestic satellites, multiplexed optical fibres or conventional microwave radio relay systems, with costs subsidized by the major urban centres; and the more difficult task in vast areas of Africa where telecommunication facilities are still largely confined to the main towns, and not always these.

Competing ever more successfully with microwave trunks are the increasing number of optical fibre systems by which paths of 50 miles or more can now be covered without intermediate repeaters. It seems increasingly likely that optical fibres will emerge as the dominant technology for international telecommunications, taking over from geostationary satellites with their inherent time-delay problems for two-way telephony, although satellites continue to be attractive for point-to-multipoint distribution of data and television channels. It was evident at the conference that there is now a distinct coolness towards satellite systems for rural coverage, mainly on grounds of costs which have not reduced to the extent confidently predicted a few years ago.

However, a means of providing a low-cost global electronic mail service by means of one or more low Earth orbiting satellites using store-and-forward packet-radio technology was proposed by Jeff Ward (University of Surrey) in a paper written jointly with Dr Martin Sweeting. The feasibility of such a system has been shown by the results achieved on the university's amateur-radio satellite Uosat-2 in conjunction with Volunteers in Technical Assistance (VITA). A third University of Surrey satellite, due to be launched early next year, is being designed to use experimental as well as amateur radio frequencies in order to permit demonstrations of third-world commercial applications.

Jeff Ward suggested that a single dedicated satellite could provide an "overnight" electronic mail service to and from anywhere in the world, based on technology costing £1M-£5M for the space segment, £200 000 for launching as a secondary payload, with the Earth terminals costing £2000-£10 000. He recognizes that "in developed countries, where businessmen are accustomed to instantaneous telephone communications, the delay inherent in low Earth orbiting store-and-forward communications may be viewed as intolerable. On the other hand, those who communicate via telex and electronic mail services rely on "near-enough real-time delivery". This often means that messages sent before the close of business one day must reach their destination by the start of business the next morning. Using certain sun-synchronous orbits, a single LEO store-and-forward communications satellite could provide such overnight electronic mail on a global basis." Packet switching using the amateur-modified (AX.25) protocol has proved well suited to such systems. Store-and-forward techniques were first used in the original communications satellites more than thirty years ago, and it is widely believed that operational systems have been or are being used by American and Russian military and intelligence agencies on account of the minimal ground-station requirements.

Jeff Ward pointed out that "it is well within the current state-of-the-art to build a portable, solar-powered terminal using a lap-top portable computer, a 10-watt v.h.f. transmitter, a single-channel u.h.f. receiver, and collapsible vertical or helical antennas all capable of fitting into a suitcase, and invaluable to technical, agricultural or medical workers who need to communicate with their support bases from remote, rural areas".



Village station for Sierra Leone's rural telecommunications network. Even a thin-line facility is better than none.

Dr A.P. Gallois (Coventry Polytechnic) described how satellite television channels carrying PAL, NTSC or SECAM-encoded pictures could be used to transmit (one-way) large quantities of data on low-level sub-carriers without significantly degrading the primary video or audio signals. His paper included an analysis of rain-fade margins in different parts of the world. The data, like teletext, would ride piggy-back on existing television distribution or direct-broadcast channels, but the data stream would be continuous at say 300kbit/s using q.p.s.k. modulation of the sub-carrier rather than in teletext bursts. The use of geostationary satellites would eliminate the need for tracking antennas.

An extremely low-cost communal "village" system has been successfully set up in Sierra Leone, based on 27MHz c.b. transceivers under microprocessor control. This was reported to the conference by Dr S.A.G. Chandler (University of Warwick) who noted that in many remote areas of developing countries, "postal services are far from comprehensive and telephone services non-existent. The only way to send a message is usually for someone to travel in person". A village network based at Bonthe began as a three-station experiment, has recently been extended, and it is hoped that eventually it could comprise 1000 to 2000 village stations bringing the entire population of about 3.5 million people within about 5km of a station. Users are expected to contribute to the capital costs, pay a minimal message charge and are being involved in the operation and maintenance under guidance from a technician at the base station. The control units provide selective calling and automatically close down the network overnight. Cost of a village station is roughly as follows: solar panels £96; c.b. type transceivers £53; microprocessor control units £110; antenna components £20; battery £25; a total of £304 plus shipping costs. The controllers also provide remote monitoring, log performance and supervise the power system. Amorphous silicon solar panels rated at 20W peak provide a maximum charging current of about 1.2A into a 12 volt double-separation lead-acid battery. The wire antennas are mounted on bamboo canes. Selected villagers are given a one-week training course covering a smattering of electricity and radio, operation, installation and basic maintenance. Many are clerks or police officers as these have some primary education, but even illiterate operators quickly became surprisingly competent, according to Dr Chandler.

He reports that "the commitment and enthusiasm of most of the Sierra Leonians involved, and the backing of the Bonthe Development Committee, are some of the most encouraging aspects of the project. It contrasts so markedly with the apathy and indifference sometimes described by expatriate experts, and augurs well for the final outcome".

Radio Communications is written by Pat Hawker.

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Fitting sound to pictures

Two months after the IBA symposium on "the implications of dual-channel sound for Independent Broadcasting" (see Television Broadcast, June 1988) a wider-based and even more ambitious two-day "Sound with pictures conference", organized by the British section of the Audio Engineering Society, again brought more than 100 delegates to the IBA's London conference hall.

This brought out the paradox that the BBC with its considerable experience of stereo production (over 1700 programmes) and Nicam 728 digital transmission of about 500 programmes from Crystal Palace since July 1986, has now postponed *sine die* its operational introduction.

This decision, due to financial constraints, has not dimmed the enthusiasm of Jeff Baker (BBC), with his belief that "the cost increases that were assumed [in deciding to postpone the service] are not an inevitable accompaniment to stereo sound [production]". He firmly rejected the idea that there is an inherent disparity between a small screen and a wide sound stage, pointing out that our eyes are more narrowly focused than our ears. He believes that the public does not want (and is unlikely to have in the foreseeable future) television screens covering one side of their rooms. But this does not mean that we should be satisfied with monophonic sound for television. He noted that several episodes of *EastEnders* have been successfully recorded in stereo with little additional time available for post-production sound editing, and at little extra cost.

Malcolm Johnson (BBC) outlined the steady development of audio post-production techniques since the milestone introduction of the SMPTE/EBU time code almost twenty years ago. He saw this as the key to modern "off-line" full-facility master/slave sound dubbing on to recorded video. He stressed the importance of modern non-destructive sound editing: "at every stage if you make a mistake you can always go back and try again". For the future, he foresaw further interesting developments in the field of hard-disc editing systems such as Audiofile and DAR's Soundstation II (described at the conference by Guy McNalley). These offer new opportunities for the manipulation of multitrack sound, held in the digital domain, with much quicker synchronization than earlier systems. Digital Audio Recording Ltd also exploits digital-sound techniques for its "Wordfit" automatic dialogue dubbing process which expands or compresses the duration of speech without changing its pitch, to improve apparent lip-synchronization with foreign languages.

It is clear that sound, so long considered the poor relation to all-important video, has now become one of the hottest topics in television. Cinderella, it seems, is now engaged to Prince Charming.

The question remains whether the set-makers, cast by some in the role of the Ugly Sisters, will provide good stereo receivers – and whether viewers really want and are willing to pay for first-class sound. In the USA, stereo sets currently amount to more than a quarter of sales. In a discussion period, R. Hoffner (NBC) commented that NBC had introduced stereo (analogue) sound in July 1985 and currently all new prime-time broadcasts were in stereo, transmitted in stereo by 141 out of its 208 affiliate stations; 11% of US homes with television had acquired stereo capability within three years – a positive reaction and a faster build-up than US colour. CBS intends to provide full primetime stereo in September. ABC's stereo policy is not finalized but seems likely to follow the other main networks; PBS is transmitting 30-40 hours of stereo per month. NBC has found the Dolby centre-channel concept helpful. On costs, Hoffner pointed out that NBC relied mainly on independent production and was not paying any premium for stereo.

Malcolm Johnson (BBC) showed an extract from *Casualty* that impressively demonstrated the degree of sophistication achievable in enhancing the sound recorded during field production, though he recognized that care needs to be taken not to degrade dialogue intelligibility, particularly for hearing-impaired viewers. He noted that a 50-minute mono programme can require some 18-19 hours of audio dubbing time, and warned that stereo will in some situations expand the time requirement.

Fritz Sippl (AKG, Vienna) described systems based on the M-S (mono-surround) pick-up techniques used with or without transformation into the X-Y format and combined with reproduction of on-screen sound from front-centre plus surround sound from sides and rear. He believes that home reproduction can be simplified greatly with M-S techniques as receiver manufacturers learn to incorporate decoders and projection loudspeakers (which can bounce the "surround" sound off the room walls, from positions on the side of receivers).

Andrew Vere (SVC Television), in a controversial presentation, explained why his facilities house has decided to leave the production of digital stereo sound (for commercials) to others, insisting that "clients will have to produce their sound track before they come to us or complete it after they have finished their editing. The cost of producing a digital audio system to complement our digital pictures facility would be so horrendously expensive that no would be prepared to use it". He pointed out that packages such as Quantel's Paintbox combined with a 90-second digital disc store ("Harry") plus an audio editing package cost in the region of £400 000. This would meet the requirements of graphic artists, video tape editors and sound mixers; but he insisted that these represent different skills: "From an operational viewpoint it represents a very expensive paint box, a very expensive edit suite and the most expensive sound mixing desk ever devised". He considers that the industry has allowed the work force to dominate its cost structure and its equipment purchasing policy: "Not enough thought has been given to the function of new equipment and the long-term effects of its purchase. Fundamental questions need to be asked each time a new piece of kit is evaluated: does it do the job quicker, does it do it cheaper – if the answer to either is no then a third question must be asked – does it do something that the market place wants that cannot be done any other way?". Later he conceded that it might sometimes have to be asked whether it does the job better. But he warned: "We must prevent the introduction of stereo sound increasing the cost of the job. The only way to do this is to leave the production sound to the experts rather than the facility houses".

Chris Daubney (IBA) noted that the Nicam 728 system, by retaining the mono analogue f.m. channel, provides broadcasters with a new degree of freedom that could be used to provide a superior mono channel that would not suffer the phase cancellations at some frequencies inherent in a straightforward balance of L and R channels. He demonstrated the difference between normal L+R and the situation where one channel is delayed by, for example, 90° by means of an all-pass phase-shift network. However in the acoustics of the conference hall, the differences appeared to be too subtle to be readily appreciated by most of the audience. No decision had then been taken on the precise way in which the Nicam and mono channels will be established.

John Watkinson (Ampex) described the differences between the D1 (component) and D2 (composite) digital videotape formats. It is clear from recent Ampex announcements that the more economical D2 formats (May issue, 437-438) is proving attractive to some major users: AME Inc. of Burbank, California, the largest full-service video post-production company, is purchasing 50 Ampex VPR-300 D2 machines at a cost of about $5 million. Today some 300 VPR-300 and ACR-225 automatic cassette players, both with D2 format, have been ordered, including 38 VPR-300 machines for the Canadian Broadcasting Corporation, eight ACR-225 cartridge machines for Cosmos of Greenville, and some VPR-300 machines for the BBC for operational evaluation as a possible replacement eventually for C-format machines. PAL customers, regarded as the main supporters of the component D1 format, have ordered more than 70 composite digital machines.

Television Broadcast is written by Pat Hawker.

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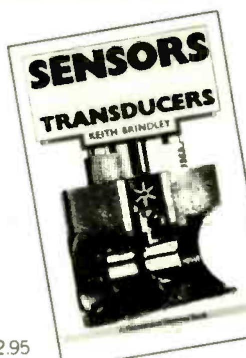

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Radials – buried or elevated?

For 50 years, medium-wave broadcast antenna systems have depended on monopole or T-wire radiators tuned against an extensive system of buried radials extending all round the mast(s).

This form of ground-plane, with copper (or in some cases aluminium) wires buried with aid of a mole plough, stems directly from the classic June 1937 *Proc. IRE* paper "Ground systems as a factor in antenna efficiency" by Dr George Brown, R.F. Lewis and J. Epstein of RCA. This showed conclusively that extensive radial systems resulted in higher radiation efficiency in sites of good, average and poor earth conductivity and sounded the death knell for simple earth spikes and single-wire counterpoise systems. In one test, at 3MHz, the authors noted that radials laid on the surface were about as good as an equal number of wires buried to depths of about six inches. However, since buried wires permit agricultural use of the large sites needed to accommodate m.f. antennas with many radials, in practice the wires are almost always buried.

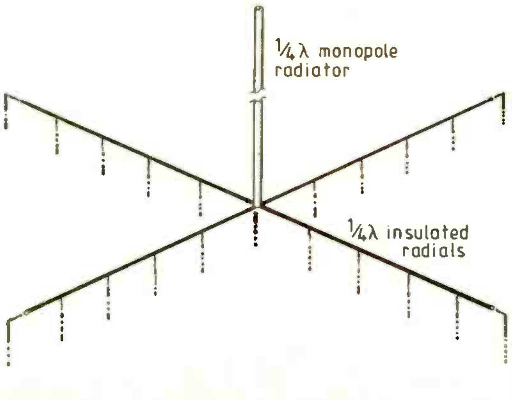
In the early 1980s, a small group of retired engineers who were also radio amateurs – Archibald Doty, John Frey and Harry Mills of Fletcher, North Carolina – recognized that, owing to the almost universal adoption of buried radials, there had been little recent investigation into the characteristics of antenna systems based on elevated (insulated) counterpoises and ground screens for use with electrically short vertical antennas.

Following some thousands of measurements they reported that the return currents of insulated radials of an elevated counterpoise system tend to be better distributed than with buried or surface radials. The group suggested that, for equal efficiency, a counterpoise system should be able to operate with fewer radial wires than the more conventional approach of burying the wires. A recent computer study "AM broadcast antennas with elevated radial ground systems", by Al Christman and Roger Radcliffe (Ohio University), Dick Adler (US Naval Postgraduate School), Jim Breakall (Lawrence Livermore National Laboratory) and Al Resnick (Capital Cities/ABC Radio) in *IEEE Trans. on Broadcasting*, provides further evidence that the use of elevated radials would provide superior performance than buried radials, allowing the collection of electromagnetic energy in the form of displacement currents rather than forcing it to flow through lossy earth in the form of conduction currents. So far this work has depended upon computer modelling antenna systems, using the NEC-GS "Methods of Moments" software developed at the Lawrence Livermore National Laboratory, although field measurements are being planned.

The computer studies indicate that a radiator elevated several metres above earth and having only four elevated horizontal radials should theoretically outperform a ground-mounted antenna with 120 buried radials over any type of soil. A typical elevated radial system would comprise (for 1MHz) four 75 metre radials supported along their length at 15m intervals by a mast which extends upwards to within 0.5m of the radial. The height of the end mast for each radial is equal to the elevation of the radial above ground, but separated laterally from the tip of the radial by 0.5m. The centre mast supports the monopole. Each mast is attached to a 2m earth stake driven full-length into the ground. Masts and ground stakes of steel, radials of copper wires, and the monopole antenna constructed of aluminium. The four radials are bonded directly to the top of the central mast, but insulated from all other support structures. The whole arrangement is thus similar electrically to the popular h.f. and v.h.f. "ground-plane antennas" originally also developed by Dr George Brown.

The authors conclude that, if the theoretical results are confirmed in practice, the construction cost and complexity of m.f. vertical monopole antenna systems could be reduced significantly. The elevated monopole antenna should also provide increased groundwave field intensity while attenuating skywave radiation.

According to an American computer study of m.f. transmitting antennas, elevated radials work better than buried ones. They should also cost less to construct.



Cycle 22 will see m.u.f. soar

The extreme difficulty of making accurate medium- and long-term prediction of optimum frequencies has long haunted h.f. broadcasters – particularly during the early years of a new solar cycle, owing to the large and unpredictable variations in the maximum magnitude of successive cycles. Solar cycle 22, now recognized as having begun in September 1986, has seen solar activity rising rapidly in fits and starts. It now seems likely to rise to record or near-record heights despite a number of earlier predictions that this cycle would have a low maximum (much the same was predicted in the early days of Cycle 21 and subsequently proved wrong).

Writing in *Nature* (12 May, 1988) Dr Geoffrey Brown (University College of Wales, Aberystwyth) suggests that there is now good evidence, based on the use of precursors such as the number of geometric abnormal quiet days (a.q.ds) during the declining period of the preceding cycle, to predict a high peak sunspot number of 174±35 with a maximum in 1990±1. The relationship between a.q.ds and the magnitude of the following peak has been found to hold good back to 1885, the earliest year for which data is available. If this prediction holds good it would make the peak of Cycle 22 one of the highest on record, and should provide broadcasters with many hours' use of the highest frequency h.f. allocations at 21.4 and 26MHz, and maximum usable frequencies rising well above 50MHz at times.

However, listening to h.f. broadcasts in western Europe is "on the way out", although still important in some parts of the world according to some observers at the recent International Radio Days 1988 conference at Antwerp – the conference formerly known as the European DX Conference. Other forms of international communications, including satellite-delivered television and high-quality sound for rebroadcast or cable distribution, and personal computer electronic mail are seen as bidding to diminish the h.f. radio audience, of which only a tiny minority now represents the short-wave enthusiasts interested more in receiving unusual or low-power transmissions than in listening to programmes.

According to a Russian representative at Antwerp, interference (jamming) with the reception of h.f. broadcasts to the USSR is now confined to broadcasts from two propaganda services (presumably the American-funded Radio Liberty and Radio Free Europe). The USSR has agreed to observe international agreements relating to satellite broadcasting.

Radio amateurs throughout the world have welcomed the cessation after many years of all Chinese broadcasts on frequencies within the world-wide exclusive amateur allocation of 7000 to 7100kHz, now officially confirmed as having stopped in December 1987.

Radio Broadcast is written by Pat Hawker.

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TDA2581	2.95
TDA2582	2.95
TDA2593	2.95
TDA2600	6.50
TDA2610	2.50
TDA2611A	1.95
TDA2640	3.50
TDA2655	4.95
TDA2680A	2.75
TDA2690	2.45
TDA3310	2.95
TDA3510	3.50
TDA3560	3.95
TDA4050	2.95
TDA4600	2.50
TDA9503	3.15
TEA1009	1.35
UPC41C	3.50
UPC566H	2.95
UPC575C2	2.75
UPC1001H	1.95
UPC1020H	2.95
UPC1024H	1.50
UPC1025H	1.95
UPC1028H	1.95
UPC1032H	1.50
UPC1158H	0.75
UPC1167C2	1.95
UPC1181H	1.25
UPC1182H	2.95
UPC1185H	3.95
UPC1191V	1.50
UPC1350C	2.95
UPC1353C	2.45
UPC1360	2.95
UPC1365C	3.95
UPC2002H	1.95
UPD2114LC	2.50
555	0.35
556	0.60
723	0.50
741	0.35
747	0.50
748	0.35
7808	0.60
7805	0.65
7812	0.65
7815	0.65

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Ferguson 3V29/JVC HR7200	2.75
Ferguson 3V31/JVC HR7650	2.75
JVC HR3330/3600	2.75
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National Panasonic NV300/333/340	2.95
National Panasonic NV2000B	3.75
National Panasonic NV777	2.75
National Panasonic NV3000B	3.75
National Panasonic NV7000	2.75
National Panasonic NV8600/8610/8620	3.75
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Sanyo VTC5300	1.75
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Sanyo VTC9300	3.75
Sanyo VTC9300P	3.90
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Sharp 7300	3.50
Sharp 8300	3.50
Sharp 9300	3.50
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Sony SL8000/8080	4.50
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DECCA 120	6.95
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ITT CVC20/25/30	6.35
ITT CVC45	6.95
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PHILIPS G9	6.00
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PYE 713 5 LEAD	8.50
PYE 731/25	8.50
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RANK A823	6.95
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THORN 3500	7.95
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TV18 STICK	1.10
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ELC1043/06 MULLARD	8.65
U321	8.25
U322	8.25
U324	11.00

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VA1056S	0.23
VA8650	0.45
VA1097	0.25

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ITT CVC20	8.20
ITT CVC25/30/32	8.20
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THORN 8000	23.50
THORN 8500	17.50
THORN 9000	19.50
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THORN MAINS TRANSFORMER 3000/3500	9.70

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AA119	0.08
BA115	0.13
BA145	0.16
BA148	0.17
BA154	0.06
BA156	0.15
BA157	0.30
BA244	0.75
BA301	0.75
BA302	0.85
BA313	0.75
BA318	2.95
BA328	2.95
BA521	1.75
BAV21	0.30
BAW62	0.19
BAX13	0.04
BAX16	0.12
BB105B	0.30
BT151	0.79
BY126	0.10
BY127	0.11
BY133	0.15
BY164	0.45
BY176	1.20
BY179	0.63
BT182	0.55
BY184	0.35
BY187	0.45
BY199	0.40
BY206	0.14
BY208-800	0.33
BY210-800	0.33
BY223	0.90
BY298-400	0.22
BY299-800	0.22
BYX10	0.20
BYX25-600	1.25
BYX36-150R	0.20
BYX38-600R	0.60
BYX55-600	0.30
BYX71-600	1.75
BZX61	0.15
BZX88	0.10
BZY95C30	0.35
CS4B	8.00
CS10B	16.50
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MR512	0.65
OA47	0.15
OA90	0.10
OA91	0.15
OA95	0.10
OA202	0.40
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IN23B	2.95
IN23C	4.95
IN23ER	4.95
IN23WE	2.95
IN4001	0.04
IN4003	0.04
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IN4007	0.06
IN4148	0.02
IN4448	0.10
IN5401	0.12
IN5402	0.14
IN5403	0.12
IN5406	0.13
IN5407	0.16
IN5408	0.16
ITT44	0.10
ITT923	0.15
ITT2002	0.10

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D13-611GH	59.00
D13-630GH	59.00
D13-630GM	59.00
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D14-181GM	53.00
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F31-12LD	75.00
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M14-100GM	45.00
M17-1512GVR	175.00
M23-112GV	55.00
M24-120LC	59.00
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DET18	28.50
DET20	2.50
DET22	35.00
DET23	35.00
DET24	27.50
DET25	22.00
DET29	32.00
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DF92	0.60
DF96	1.25
DF97	1.25
DG10A	8.50
DH63	1.50
DH77	0.90
DK91	1.20
DK92	1.50
DL35	2.50
DL63	1.00
DL70	2.50
DL73	2.50
DL91	3.95
DL92	1.25
DL93	1.10
DLS10	13.50
DLS16	10.00
DM70	2.50
DM160	4.50
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E80F	18.50
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E81CC	5.50
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E82CC	4.50
E83CC	4.50
E83F	5.50
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E88CC	3.50
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E90CC	7.95
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E91H	4.50
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E99F	6.95
E130L	18.50
E180CC	9.50
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E182CC	9.00
E186F	8.50
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E235L	12.50
E280F	19.50
E283CC	12.00
E288CC	17.50
E810F	25.00
E1148	1.00
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EA52	55.00
EA76	1.95
EA79	1.95
EABC80	1.50
EAC91	2.50
EAF42	1.20
EB34	1.50
EB41	3.95
EB91	0.85
EBC33	2.50
EBC41	1.95
EBC81	1.50
EBC90	1.95
EBC91	1.95
EBF80	0.95
EBF83	0.95
EBF89	0.70
EBF93	0.95
EBL1	4.50
EBL21	4.50
EC52	0.75
EC70	1.75
EC81	7.95
EC86	1.95
EC88	1.95
EC90	1.50
EC91	5.50
EC92	1.95
EC93	1.50
EC95	7.00
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ECC32	3.50
ECC33	3.50
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ECC81	1.50
ECC81 SPECIAL QUALITY	2.25
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ECC83 PHILIPS	1.95
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ECC88	1.00
ECC89	1.50
ECC91	2.00
ECC189	2.50
ECC801S	6.95
ECC803S	6.95
ECC804	0.60
ECC2000	7.95
ECF80	1.15
ECF82	1.15
ECF86	1.70
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ECF202	1.85
ECF801	0.85
ECF804	6.50
ECF805	2.50
ECF806	10.25
ECH3	4.50
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ECH35	3.50
ECH42	1.50
ECH81	1.75
ECH83	1.00
ECH84	1.00
ECH200	1.50
ECL80	0.60
ECL82	1.00
ECL83	2.50
ECL84	0.74
ECL85	0.95
ECL86	0.95
ECL805	0.95
EF37A	2.50
EF22	3.50
EF39	1.50
EF40	4.50
EF42	3.50
EF50	2.50
EF54	4.50
EF55	4.95
EF70	1.20
EF73	3.50
EF80	0.55
EF83	3.95
EF85	0.50
EF86	2.25
EF86 MULLARD	4.50
EF86/CV4085	5.00
EF89	1.50
EF91	195
EF92	2.15
EF93	1.50
EF94	1.50
EF95	1.95

EF97	0.90
EF98	0.90
EF183	0.75
EF184	0.85
EF731	4.50
EF800	11.00
EF804S	19.50
EF805S	25.00
EF806S	25.00
EFB12	0.65
EFL200	1.50
EFP60	3.50
EH90	0.72
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EL33	5.00
EL34	2.95
EL34 MULLARD Matched per pair	15.00
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EL36	2.50
EL36 MULLARD	3.95
EL37	9.00
EL38	9.00
EL41	3.50
EL42	2.00
EL71	4.50
EL81	6.95
EL83	7.50
EL84	0.95
EL84 MULLARD	3.50
EL84 SIEMENS	2.50
EL85	4.50
EL86	1.75
EL90	1.75
EL91	6.00
EL95	1.75
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EL360	6.75
EL500	1.95
EL504	1.95
EL506	5.95
EL509	5.25
EL509 MULLARD	7.50
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EM83	1.65
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EM87	2.50
EN32	15.00
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EY51	0.80
EY70	7.50
EY81	2.35
EY82	1.15
EY83	1.50
EY84	5.95
EY86/87	0.50
EY88	0.85
EY91	5.50
EY500A	1.50
EY802	0.70
EZ35	1.00
EZ40	2.75
EZ41	2.75
EZ80	0.75
EZ81	0.75
EZ90	1.50
FW4-800	2.95
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G180/2M	6.95
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GN4	6.00
GN10	15.00
GR10G	4.00
GS10C	16.50
GS10H	12.00
GS12D	12.00
GT1C	14.00
GU20	35.00
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GXU1	13.50
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GXU50SS	14.50
GY501	1.50
GY802	1.50
GZ32	2.50
GZ33	4.50
GZ34	2.50
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H8C90	1.95
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KT33C	3.50
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KT66 GEC	25.00
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KT67	9.00
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KT81	7.00
KT88 USA	10.95
KT88 Selectron	15.00
KT88 Gold Lion	22.50
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KTZ63	2.50
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LS9B	6.95
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M5143	155.00
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M8082	7.50
M8083	3.25
M8091	7.50
M8096	3.00
M8098	5.50
M8099	5.00
M8100	5.50
M8136	7.00
M8137	7.95
M8161	6.50
M8162	5.50
M8163	5.50
M8190	4.50
M8195	6.50
M8196	5.50
M8204	5.50
M8223	4.50
M8224	2.00
M8225	3.95
ME1400	3.50
ME1401	29.50
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MHLD6	4.00
MP25	195.00
MS4B	5.50
MU14	3.50
N37	12.50
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OA2	1.50
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ORP43	2.50
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P41	2.50
PABC80	0.75
PC86	0.75
PC88	0.75
PC92	3.50
PC97	1.10
PC900	1.25
PCC84	0.40
PCC85	0.55
PCC88	0.70
PCC89	0.70
PCC189	0.70
PCC805	0.70
PCC806	0.80
PCE82	0.80
PCF80	0.65
PCF82	0.60
PCF84	0.65
PCF86	1.20
PCF87	1.25
PCF200	1.80
PCF201	1.80
PCF801	1.35
PCF802	0.85
PCF805	1.25
PCF806	1.00
PCF808	1.25
PCH200	1.50
PCL82	0.85
PCL83	2.50
PCL84	0.75
PCL85	0.80
PCL86	0.85
PCL805	0.90
PD500	5.95
PE1-100	69.00
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PEN40D	3.00
PEN45	3.00
PEN45DD	3.00
PEN46	2.00
PFL200	0.95
PL36	1.75
PL38	1.50
PL81	1.25
PL82	0.60
PL83	0.52
PL84	0.78
PL500	1.10
PL504	1.15
PL508	1.75
PL509	4.85
PL519	4.95
PL802	6.00
PL802T	3.50

PL820	2.95
PY32	0.60
PY33	0.50
PY81	0.70
PY82	0.70
PY83	0.70
PY88	0.65
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PY800	0.79
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QB3-300	72.00
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QQV02-6	19.50
QQV03-10	5.50
QQV03-10 MULLARD	15.00
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QQV06-40A MULLARD	39.50
QQV07-50	55.00
QQZ03-20	42.50
QQZ06-40	45.00
QS75/20	1.50
QS95/10	4.85
QS108/45	4.00
QS150/15	6.95
QS150/30	1.15
QS150/40	7.00
QS1205	3.95
QS1213	5.00
QU37	9.50
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QV05-25	2.50
QV06-20	29.50
QV08-100B	145.00
QY3-125	72.00
QY4-250	72.00
QY4-400	85.00
R10	4.00
R18	2.50
RG1-240A	14.50
RG3-250A	6.50
RG3-1250A	35.00
RR3-250	15.00
RR3-1250	35.00
S11E12	38.00
S104-2K	10.00
SC1/1300	6.00
SP61	3.50
STV280/40	11.95
TB2-5/300	85.00
TB2-300	195.00
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TD03-10/D/E/F	35.00
TT15	45.00
TT21	45.00
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TT100	69.00
TY2-125A	85.00
TY4-400	85.00
TY7-6000A	600.00
TY8-600W	365.00
U19	9.50
U26	0.90
U35	3.50
U37	9.00
U41	6.95
U50	2.00
UB2	3.00
U191	0.70
U192	1.00
U193	1.00
U251	2.50
U801	3.50
UABC80	0.65
UAF42	1.00
UBC41	3.95
UBC81	1.50
UBF80	0.60
UBF89	1.00
UBL21	1.75
UC92	1.20
UCC84	0.70
UCC85	0.60
UCF80	1.00
UCH21	1.20
UCH41	2.50
UCH42	3.95
UCH81	1.00
UCL82	1.75
UCL83	2.50
UF41	2.25
UF42	2.25
UF80	1.75
UF85	1.20
UF89	2.00
UL41	7.50
UL44	3.50
UL84	1.50
UL85	0.85
UU5	3.50
UU6	6.00
UU7	8.00
UU8	9.00
UY41	3.50

UY85	0.70
V235A/1K	250.00
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W21	4.50
W61	4.50
W77	5.00
WB1M	4.50
W739	1.50
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ZM1001	12.00
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ZM1041	14.00
ZM1082	9.00
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1A3	4.50
1AE4	3.50
1AX2	3.50
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1B63A	75.00
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1P28	25.00
1R5	0.90
1S5	1.50
1T4	1.00
1U4	1.75
1U5	1.00
1X25	2.50
2A3	16.50
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2B7	2.50
2B22	69.50
2C36	70.00
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2C39BA	39.50
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3A/110B	12.00
3A/141K	11.50
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3A/167M	10.00
3A3A	3.95
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3A5	4.50
3AT2	3.35

3B22	25.00
3B24	12.00
3B26	24.00
3B28	15.00
3BZ6	1.50
3C45	24.00
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6AQ8	1.00
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6AS6	2.50
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6AT6	1.95
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6AU4GT	2.00
6AU5GT	4.50
6AU6	0.95
6AV6	1.95
6AW8A	3.50
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6AY3B	1.95
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6B8G	1.50
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6BA7	4.50
6BA8A	3.50

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6BE6	1.50
6BG6G	3.00
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6BK4	4.00
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6BL8	1.15
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6BW6	5.35
6BW7	1.50
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6BZ7	2.95
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6C5	1.95
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6CBG	1.50
6C9	4.95
6CA4	4.95
6CA7	3.50
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6BC6	1.95
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6DT6A	1.50
6DW4B	21.5
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6EA8	2.50
6EB8	1.75
6EJ7	0.85
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6EM7	2.50
6EU8	1.75
6EV7	2.95
6EW6	1.50
6EW7	4.50
6F1	2.00
6F5	5.50
6F7	5.50
6F13	3.00
6F14	1.00
6F17	2.75
6F23	0.60
6F24	1.25
6F25	1.25
6F28	1.25
6F32	1.25
6F33	12.50
6FH5	6.50
6FH8	5.95
6FL2	4.50
6FQ7	3.50
6GE5	3.95
6GH8A	2.50
6GJ7	0.85
6GM6	2.65
6GS7	21.5
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6GW8	2.50
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6GY6	2.50
6H1	9.50
6H6GT	1.95
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6HF8	2.50
6HM5	2.50
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6HS8	2.95
6HZ6	3.50
6J4	2.15
6J5GT	2.50
6J6	2.00
6J7	4.15
6J7G	4.15
6JB6A	6.50
6JE6C	7.50
6JM6	7.50
6JU8A	2.50
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6K7G	2.00
6K8G	3.00
6KD6	7.50
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6L6GC USA	6.50
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6Q7GT	1.50
6R7	3.15
6RHH8	10.00

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6SC7	1.50
6SH7	1.35
6SJ7GT	1.20
6SK7	1.35
6SL7GT	1.95
6SN7GT	1.95
6SQ7GT	1.50
6SS7	1.95
6T8	1.50
6U6GT	3.50
6U7G	3.50
6U8A	1.50
6V6G	1.25
6V6GT	1.95
6W4GT	1.95
6Y6G	3.95
6X2N	1.00
6X4	1.50
6X5GT	1.00
6X5GTY	1.00
6X8A	2.25
7A6	4.50
7AU7	1.50
7B6	3.50
7B7	2.50
7D8	4.50
7J7	5.50
7K7	7.50
7L	1.50
7Q7	4.50
7Y4	2.50
8B8	2.50
8B10	2.50
8BQ5	1.95
8CW5	1.50
8EB8	1.50
8FQ7	1.50
10D2	1.25
10DE7	2.50
10DX8	2.50
10EB8	1.95
10EW7	2.95
10F1	0.75
10GK6	1.95
10IP4	2.50
11E3	55.00
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12AT7	1.15
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12AV7	2.50
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12AX7	0.95
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12AX7S	7.95
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12K8	1.95
12KU7	1.95
12S7GT	1.50
12SA7GT	1.95
12SG7	4.75
12SK7	1.95
12SJ7	1.50
12SN7GT	1.85
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12SY7	4.50
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13D7	3.20
13DE7	2.50
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16L	0.40
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17DW4A	2.95
17EW8	0.95
17JZ8	4.50
18D3	6.00
18GB5	3.50
19AQ5	3.50
19AU4GT	2.50
19BG6	3.50

19G3	19.50
19G6	9.00
19H4	35.00
19H5	33.50
20CV	9.50
20D1	0.70
20LF56	7.95
20L1	0.95
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20P4	1.95
20P5	1.15
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24B9	39.50
25BQ6	1.75
25DQ6B	2.95
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29C1	19.50
29KQ6	6.50
30C15	0.50
30C17	0.40
30C18	1.48
30FL2	1.35
30FL12	0.95
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30FL14	1.25
30L1	0.45
30L15	0.60
30L17	0.60
30P4MR	1.00
30P12	1.00
30P18	0.60
30P19	1.00
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30PL13	0.60
30PL14	1.75
31JS6C	5.50
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80	4.50
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812A	35.00

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829B	14.50
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845	45.00
866A	8.50
872A	20.00
873	60.00
954	1.00
955	1.00
1849	315.00
1927	25.00
2040	25.00
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4471	35.00
4687A	9.50
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5559	55.00
5636	5.50
5642	9.50
5643	9.50
5651	2.50
5654	1.95
5670	3.25
5675	28.00
5678	7.50
5687	4.50
5696	4.50
5702	3.50
5704	3.50
5718	6.15
5725	2.50
5726	2.50
5727	2.50
5749	2.50
5750	1.85
5751	2.95
5763	6.50
5814A	3.25
5823	9.50
5829WA	6.50
5840	3.50
5842	11.00
5847	10.95
5863	95.00
5879	9.50
5886	13.95
5894	39.50
5899	4.50
5963	1.75
5965	2.15
6057	3.75
6058	2.50
6060	2.25
6072	6.95
6080	8.50
6080WA	9.50
6132	10.50
6136	2.50
6146B	9.50
6155	72.00
6156	72.00
6157	2.50
6158	3.20
6201	6.45
6350	3.50
6360	4.50
6386	14.50
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6550	8.50
6550A GE	10.95
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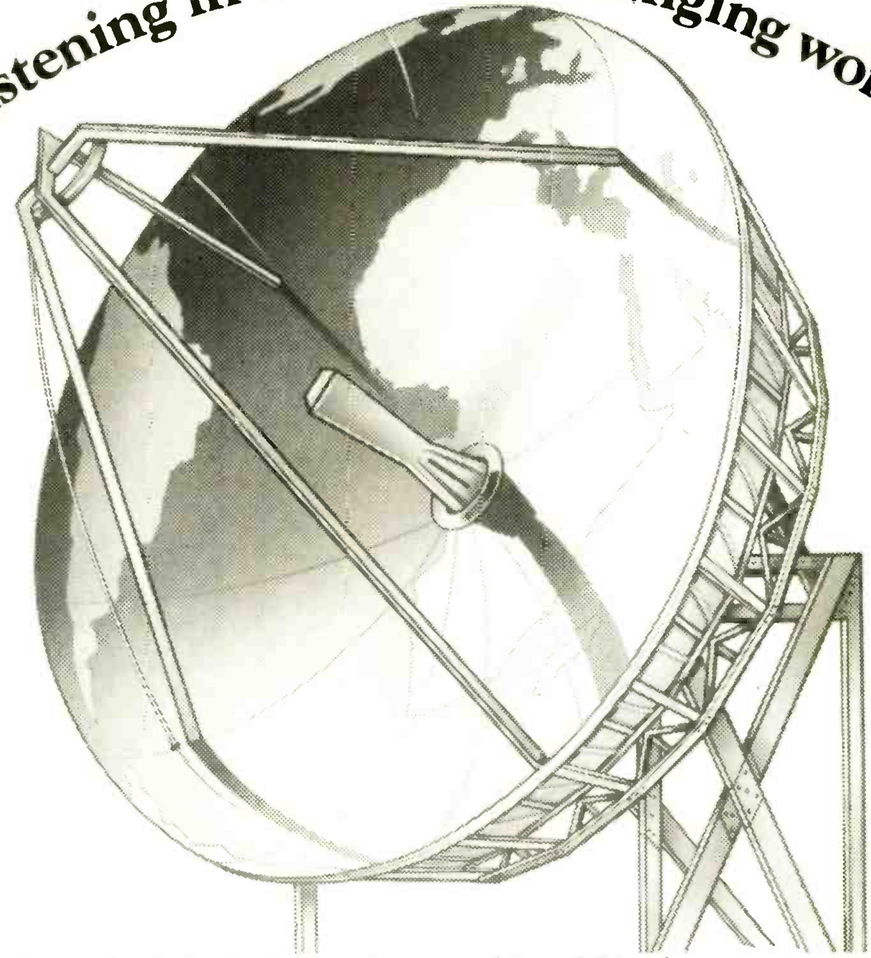

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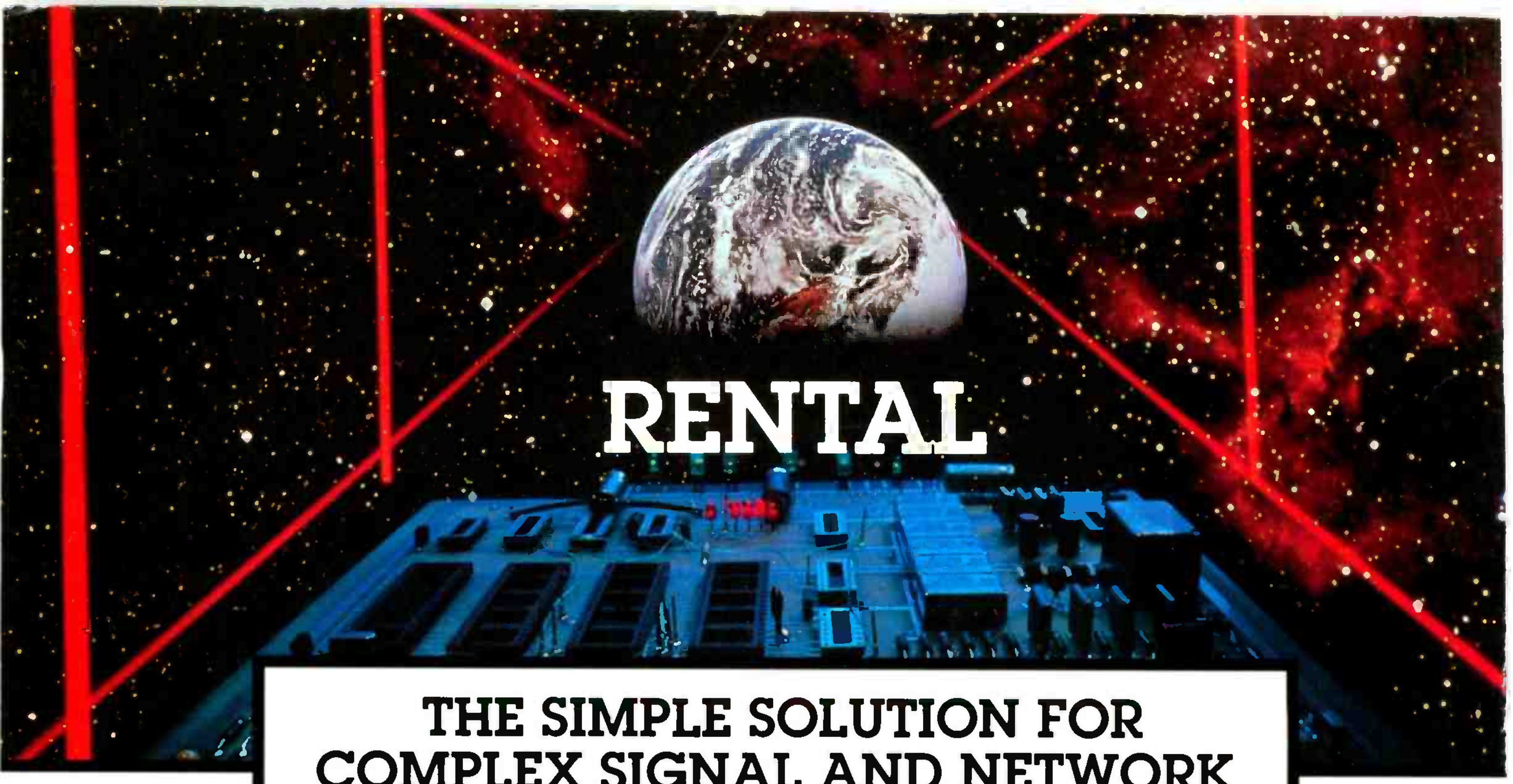

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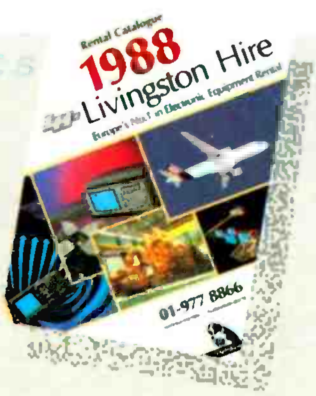

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