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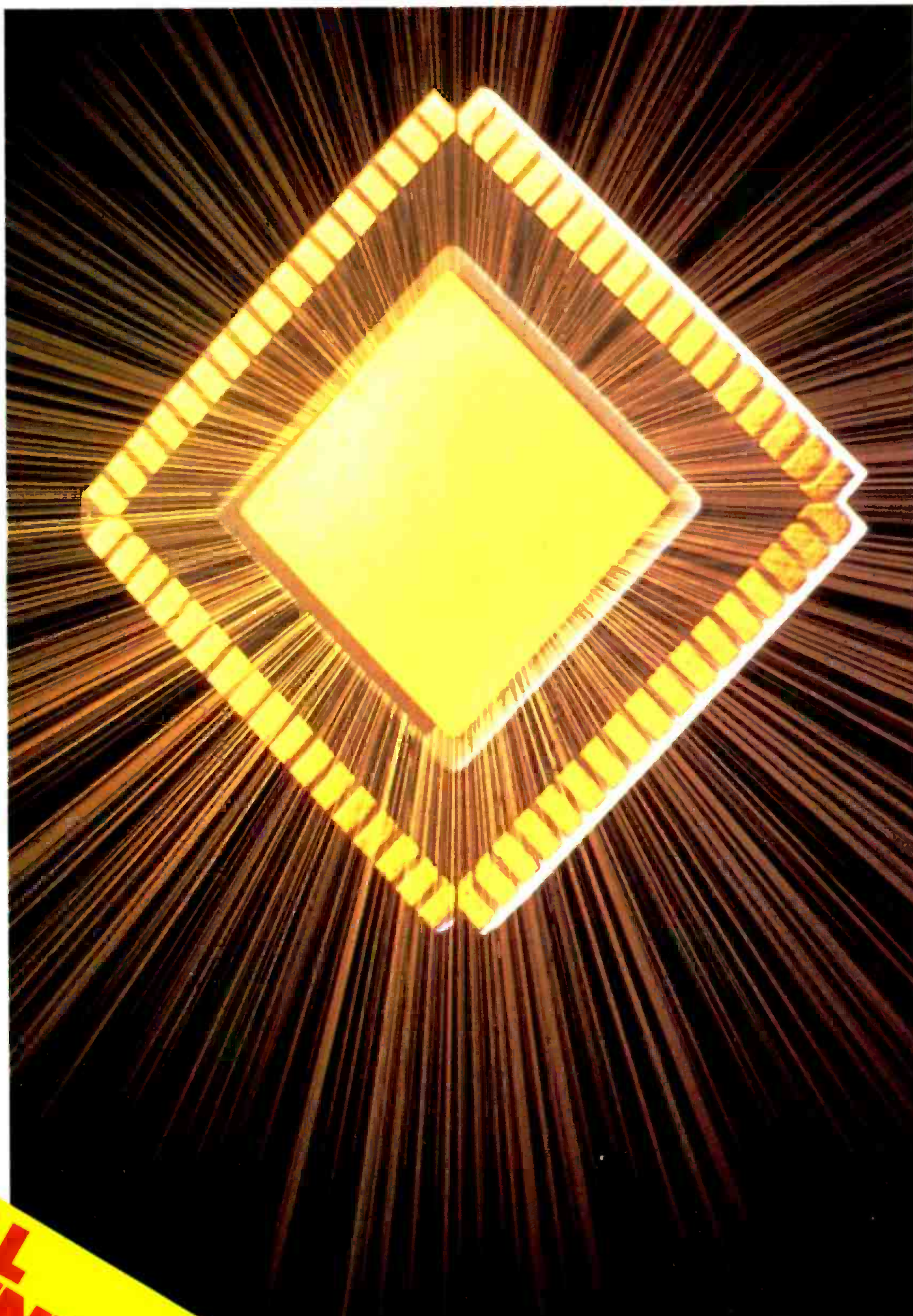

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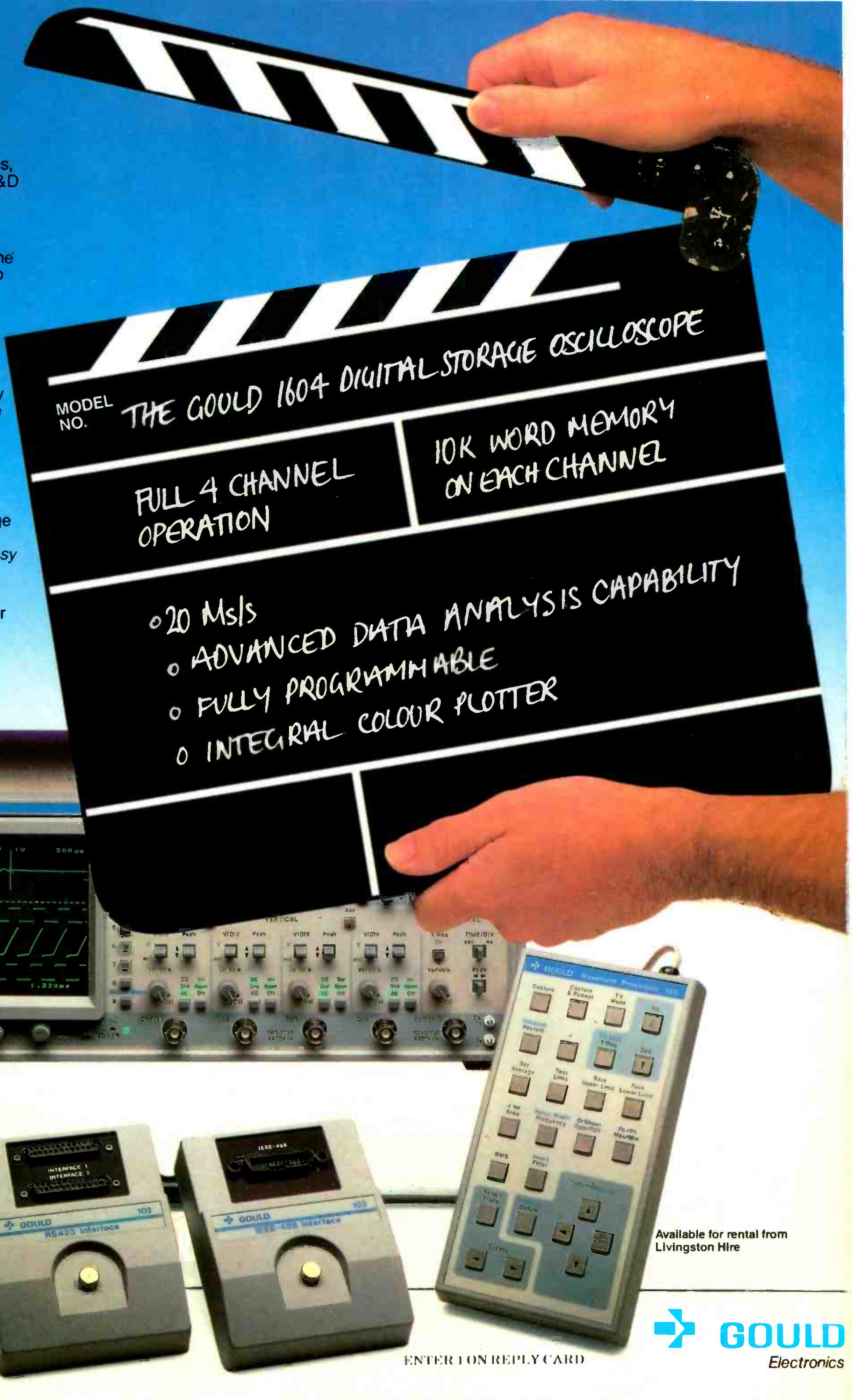

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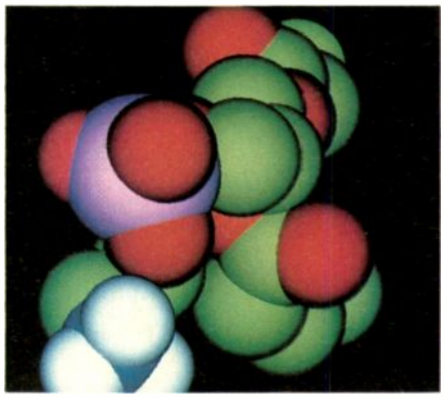

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COMMENT

Defence mechanisms

There must be many engineers, in many countries East and West, working in the weapon business whose attitude to their daily occupation lies uneasily between two extremes. At one end there is complete acceptance. This may result from a variety of sentiments and conditions ranging from sincere patriotism through economic necessity to moral indifference. At the other extreme is complete rejection, possibly stemming from religious, ethical or other such convictions. Here the engineer either leaves the military electronics business if he is employed in it or refuses any job he may be offered in this field.

Those in the middle are probably intelligent people who are well aware of the purpose of the electronic equipment they are helping to make. Intellectually, they know it is part of the armoury designed to threaten, on the principle of defence by deterrence, or in the final instance to destroy, other human beings. But because of the many persons employed in the work and the highly specialized nature of individual contributions, these engineers do not feel that they are directly engaged in a hostile activity. If pressed on the moral implications, an engineer in this situation might well argue, apparently reasonably: "If I did not do this work, somebody else certainly would. So it really doesn't make any difference whether I, personally, am involved: the work would get done in any case."

But just how reasonable is this utilitarian argument? As a pragmatic analysis purely in terms of man-hours it is perfectly sound. In terms of actual human behaviour and its social consequences, however, the rationalization is not conclusive. If, for example, an engineer prompted by conscience leaves a weapons job specifically to do socially beneficial work, say in the medical field, the person who subsequently fills the weapons vacancy is not likely to be one who suffers unduly from moral dilemmas. So it's not highly probable that the newcomer has left socially beneficial work to make this change. In other words, the switch of particular individuals can make a net difference.

There is another way in which a decision by a morally or socially concerned engineer on whether to do military work can make a difference. If he decides to take, or stay in, a weapons job, he is thereby helping to make it respectable among those colleagues and friends who know and value him as a decent person. Thus his decision is not confined to himself: it can influence others. If he does the reverse, either refusing or leaving military work on ethical/social grounds, his decision has two human consequences. First, his action has a small but real effect on the moral climate in electronics engineering employment. Second, he is free to campaign from outside against other engineers going into such work.

Finally, looking at the personal rather than social consequences, if the engineer with this particular uneasiness of conscience stays in work which he finds in some degree morally repugnant, he will probably – being that sort of person – damage his own psychological integrity and self-esteem. In addition, his willingness to live such a lie, or be at war with himself, could infect his relationship with other people, particularly his family or persons very close to him. So this individual remaining in a weapons job could cause distress, whereas a less concerned person probably would not. Again, a difference is possible.

Thus the rationalization: "It doesn't make any difference whether I, personally, do the work" is not universally true, and one cannot hide behind it with complete safety. The action taken by the individual engineer can certainly make a difference in its human consequences. In the end, if we can't rely on the utilitarian argument we may have to make an absolute moral choice.

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Multiprocessor systems

In this, the first of three articles, Alan Clements looks at various multiprocessor architectures and discusses their advantages and disadvantages.

ALAN CLEMENTS

In this series of articles I will look at multiprocessor systems in general and then discuss how multiprocessor systems based on the 68000 microprocessor can be implemented. Two approaches to multiprocessors are described: one based on shared or dual-port memory and the other based on a common bus (the VMEbus). This first article provides an overview of multiprocessor systems and considers some possible multiprocessor topologies.

Multiprocessing is, of course, a vast subject and here I only scratch the surface of this topic. I am more interested in the way in which the 68000 interfaces with other 68000 microprocessors than with specific applications of multiprocessors.

In a multiprocessor system two or more processors work together to achieve a greater throughput than is possible with one processor alone. I use the word 'processor' in the previous sentence rather than microprocessor or c.p.u., because it is not necessary to combine identical processors to create a multiprocessor system. Indeed, there is sometimes an advantage in using several different types of processor, each optimized for the tasks to be run on it.

Generally speaking, the term processor can be applied to any device with the characteristics of a central processing unit, or c.p.u. That is, a processor should be able to read instructions from memory and then execute them (although some processors do not themselves read instructions from memory but rely on some other device to transfer data to them). A true multiprocessor system contains two or more processors in the *same* housing: the processors are separated by no more than a few tens of centimetres. The physical distance between the processors making up a multiprocessor system is important, because there is a world of difference between a multiprocessor system and the distributed computer system (called a local-area network).

Individual processors in a multiprocessor system operate together on a 'logically coherent' task. That is, the various processors of the multiprocessor system cooperate to solve a specific task and are not simply operating on a number of unrelated tasks, as you might find in a typical local-area network. The processors communicate intimately with each other and often share the same facilities (either hardware or data).

In contrast to the multiprocessor system, the individual processors of a distributed system are separated by distances ranging from a few metres to many kilometres and communication between them is minimal. The local-area network is designed to enable users to share resources such as discs and printers that are geographically distributed.

OVERVIEW

Multiprocessor systems exist only because a given task can be carried out by means of several low-cost processors operating in parallel, rather than by a single high-cost high-performance processor operating alone. For example, suppose an application requires a throughput equivalent to a single 68000 operating at a clock rate of 60MHz. Clearly, such a device does not exist and the cost of constructing a system from emitter-coupled logic or buying a super minicomputer may be prohibitive. It may be possible to partition the task into subtasks in such a way that, say, ten 68000s operate on the subtasks simultaneously to give an effective throughput equal to that of a single high-performance processor.

Even when a multiprocessor system is not mandatory in a particular arrangement, multiprocessing can provide an economic advantage by increasing the power of a computer for very little additional cost. The economic benefits of multiprocessing arise because the cost of computer hardware lies almost entirely in its memory and peripherals. Often the microprocessor itself represents no more than one to less than 0.01% of the retail price of the system. Therefore, adding extra processors has little effect on the overall cost of the hardware. Unfortunately, an extra processor cannot just be plugged into an existing system. The global implications for the system hardware and its software are not trivial, because the individual processors have to share the available resources (i.e. memory and input/output). As with people, a one-person job is dispute-free, while a two-person job introduces the possibility of conflict. An effective multiprocessor system must be able to allocate resources to contending processors without seriously degrading the performance of the system.

Another reason for the interest in multiprocessor systems springs from their potential reliability. It can be argued that, if the probability of failure over a given time of a processor is p, then the probability of the simultaneous failure of two processors is p^2. Thus, if p is 1% per 10^4 hours for a given microprocessor, reliability of a dual-processor system is 0.01% per 10^4 hours. Similarly, the reliability of a triple-processor system is 0.0001% per 10^4 hours.

Alas, life is not as simple as the above figures would suggest. The processor represents only a tiny fraction of a computer's total hardware and there is little point in replicating this relatively reliable component alone. A realistic implementation of a highly reliable system replicates memory, control and peripheral elements. To make matters worse, the extra logic needed to detect, report and deal with the failure of a processor reduces the reliability of the system. Consequently, multiprocessor systems can be designed to be highly reliable, but are not necessarily cheap. Such systems are said to offer a 'high level of availability' and display 'graceful degradation'. The latter term implies that the failure of part of the system results in a reduced level of performance, but not necessarily its total shut-down.

Some multiprocessor systems are termed *reconfigurable*, which means that the structure of the hardware itself can be modified by the operating system. For example, the way in which memory is distributed between the individual processors can be changed dynamically under software control. Similarly, interrupt handling can be dynamically partitioned between the various processors to maximize efficiency. We do not discuss reconfigurable architectures further here.

While the architecture of a stored-program computer (i.e. a Von Neumann machine) can be defined quite precisely, there is no similar definition of a multiprocessor system. Multiprocessor systems come in many different forms and a configuration suitable for one particular application is almost useless for another. The only really universal characteristic common to all multiprocessor systems is that they have more than one processor! We shall soon examine the various classes of multiprocessor system.

Along with the advantages of multiprocessor systems come the disadvantages. To be more precise, the disadvantages are really the problems that the systems designer must consider. These are: the distribution of tasks between processors, the interconnection of the processors (i.e. the topology of the multiprocessor system), the management of the memory resources, the avoidance of deadlock and the control of input/output resources.

The distribution of tasks between processors is of crucial importance in selecting the architecture of the processor system itself. In turn, the distribution of tasks is strongly determined by the nature of the problem to be solved by the computer. In other words, the architecture of a multiprocessor system can be optimized for a certain type of problem. Conversely, a class of programs that runs well on one multiprocessor system may not run well on another.

A classic problem that often involves multiprocessing belongs to the world of air-traffic control. A radar system receives a periodic echo from the targets (i.e. aircraft) being tracked. Each echo is a function of the bearing and distance of the target. Due to imperfections in the system, there is an uncertainty associated with the echo. Moreover, a new echo is received every few milliseconds. From this constantly changing input, the computer connected to the radar receiver has to calculate the current positions of the targets and then to estimate the future track of each target and report any possible conflicts. Such a system requires very large amounts of computer processing power with relatively little i/o activity or disc access. Obviously it is not unreasonable to try to solve the problem by means of multiprocessing. For example, as one processor is updating a target's current position, another processor can be calculating its future position.

The preceding problem is described as classic, because it is so well suited to multiprocessing. There are several ways of allocating the mathematics involved in the radar calculations to the various processors. It is, unfortunately, much less easy to decompose a general task into a number of subtasks that can be run in parallel. Often it is necessary for the programmer to write programs in such a way that they involve the greatest amount of parallel activity.

TOPICS IN MULTIPROCESSOR SYSTEM DESIGN

The most important characteristic of a multiprocessor system is its topology, which defines how the processors are arranged with respect to each other and how they communicate. Another important characteristic is the degree of coupling between the various processors. I will discuss processor coupling first and then look at multiprocessor topologies.

Processors with facilities for exchanging large quantities of data very rapidly, are said to be tightly-coupled. Such computers share resources like buses or memory blocks. The advantage of tightly-coupled systems is their potential speed, because one processor does not have to wait long periods of time while data is transferred from another. Their disadvantage stems from the complexity of the hardware and software necessary to coordinate the processors. It they share a bus or memory, some arbiter is needed to determine which processor is permitted to access the resource at any time. Arbitration may require both complex software and hardware.

Loosely-coupled processors transfer data via an i/o channel such as a parallel (or even a serial) port, which offers a much slower data interchange but which simplifies the hardware design.

Although not a problem associated entirely with multiprocessors, the avoidance of deadlock must feature in the design of some classes of multiprocessor. Deadlock is a term most frequently used in the world of multitasking systems and describes the situation in which two tasks are unable to proceed because each task holds something needed by the other. In a real-time system, the sequential tasks (i.e. the software) require resources (memory, disc drives, i/o devices etc), while in a multiprocessor system these resources are required by the individual processors.

Suppose a multiprocessor system has two processors X and Y. To complete its task, processor X needs resources P and Q, and processor Y also needs resources P and Q. If X seizes resources P and Q before Y, there is no problem because X continues and Y must wait for the resources to become available. If, however, X seizes P and at the same time Y seizes Q, we have a deadlock. X is waiting for Y to release Q but Y will not release Q until it has used P. Similarly, Y is waiting for X to release P. Therefore, the system halts and goes into an infinite waiting loop; a situation also called the 'deadly embrace'.

When designing multiprocessor systems, the problem of deadlock cannot be overlooked and ways of avoiding the situation in which no processor has all the resources it needs must be considered. The avoidance of deadlock falls within the scope of the operating systems designer and is not considered further here.

Every multiprocessor system, like every single processor system, has facilities for input or output transactions. We therefore have the problem of how i/o transactions are to be treated in a multiprocessor sytem. Does each processor have its own i/o arrangements? Is the i/o pooled between the processors, with each processor asking for i/o facilities as they are needed? Finally, is it possible to dedicate one or more processors solely to the task of i/o processing?

In a similar vein, the designer of a multiprocessor may need to construct an appropriate interrupt-handling system. When an i/o device interrupts a processor in a single-processor system, there is not a lot to decide. Either the processor services the interrupt or it is deferred. In a multiprocessor system you have to decide which processor will service an interrupt, which in turn begs the question, 'Do we pool interrupts or do we allocate certain types of interrupt to specific processors?' If interrupts are pooled, the interrupt-handling software must also be pooled, as processor A must deal with an interrupt from device X in exactly the same way that processor B would deal with the same interrupt. In addition to interrupts generated by i/o devices, it is possible for one processor to interrupt another processor.

Like any other computer, the multiprocessor requires an operating system. There are two basic approaches to the design of operating systems for multiprocessors. One of the simplest arrangements is the master/slave operating system in which a single operating system runs on the master processor and all other processors receive tasks that are handed down from the master. The master/slave operating system is little more than the type of operating system found in conventional single-processor systems.

Distributed operating systems provide each processor with its own copy of the operating system, or at least a processor can access the common operating system via shared memory. Distributed operating systems are more reliable than their master/slave counterparts because the failure of a single processor does not necessarily bring about a complete system collapse.

The problems I have just highlighted serve to emphasize that a multiprocessor system cannot easily be built in a vacuum. Whenever you are faced with the design of a multiprocessor system, it is necessary to ask, 'Why do I need the multiprocessor system and what are its objectives?', and then to configure it accordingly. In other words, almost all design aspects of a multiprocessor system are very much problem dependent.

MULTIPROCESSOR ORGANIZATION

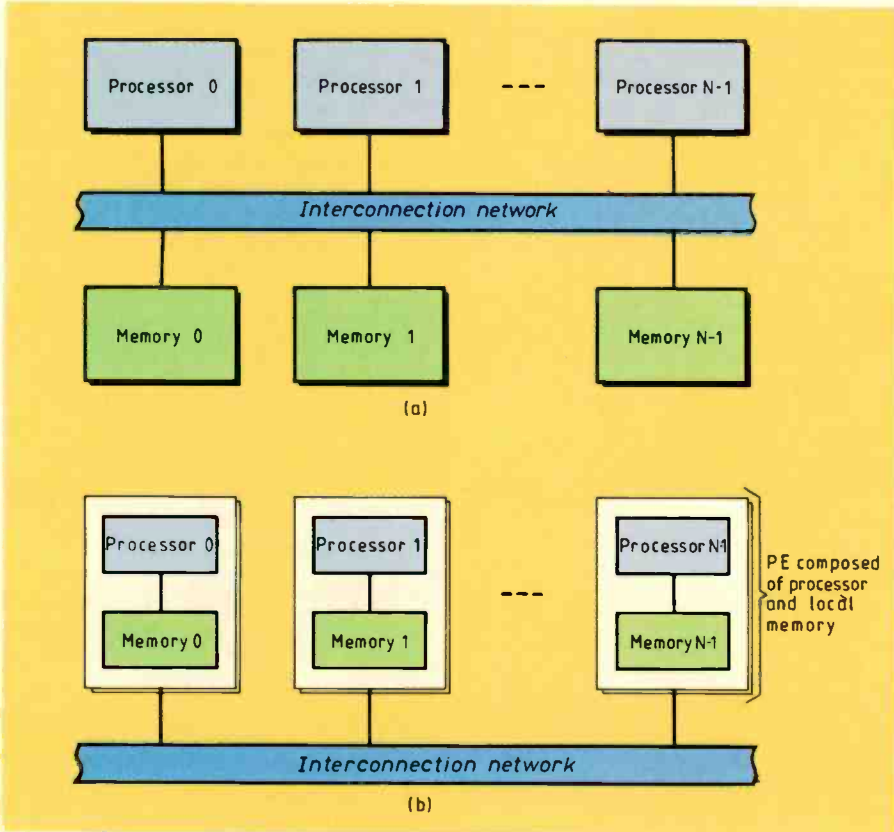
Although there is an endless variety of multiprocessor architectures, you can identify broad groups whose members have certain features in common. One possible approach to the classification of multiprocessor systems, attributed to Flynn, is to consider the type of the parallelism (i.e. architecture or topology) and the nature of the interprocessor communication. Flynn's four basic multiprocessor architectures are referred to by the abbreviations: s.i.s.d., s.i.m.d., m.i.s.d. and m.i.m.d. and are described later. However, before continuing, I must point out that Flynn's topological classification of multiprocessor systems is not the only one possible, as multiprocessors may be categorized by a number of different parameters. One broad classification of multiprocessors depends on the processor's relationship to memory and to other processing elements. Multiprocessors can be classified as processor-to-memory structures or as processing-element to processing-element structures. Figure 1 describes these two structures. A processor-to-memory architecture has N processors, an interconnection network and N memory elements. The interconnection network allocates processor X to memory Y. The more general processing-element to processing-element architecture uses N processors, each with its own memory, and permits processing element X to communicate with processing element Y via an interconnection network. The multiprocessors described in this series best fit the processing element to processing element model.

SINGLE-INSTRUCTION-SINGLE-DATA STREAM

The s.i.s.d. computer is nothing more than the conventional single processor system. It is called single instruction because only one instruction is executed at a time, and single data-stream because there is only one task being executed at any instant.

SINGLE-INSTRUCTION/MULTIPLE-DATA STREAM

The s.i.m.d. architecture is designed to execute instructions sequentially, but on data in parallel. The idea of a single insruction operating on parallel data is not as strange as it may sound. Consider vector



mathematics, where, for example, the calculation of the inner-product of two n-component vectors, A and B, is frequently required. The inner product of vectors A and B is defined as,

$$s = AB = \sum_{i=0}^{n-1} a_i b_i$$

The inner product is expressed as single operation, i.e. s=AB, but involves multiple-data elements $a_i.b_i$. One way of speeding up the calculation of an inner-product is to assign a processor to the generation of each of the individual elements $a_i.b_i$. The simultaneous calculation of $a_i.b_i$ for i=0 to n–1 requires n processors, one for each component of the vector. Such an arrangement generally consists of a single controller that steps through the program, i.e. the single instruction-stream and an array of processing elements acting on the components of vector, i.e. the multiple data-stream in parallel. Often, such processing elements are really number crunchers or high-speed arithmetic and logic units, rather than general-purpose microprocessors.

Fig.1. Two main multiprocessing structures are the processor-to-memory configuration and the processing-element-to-processing-element configuration.

The s.i.m.d. architecture, or array processor as it is frequently known, has a very high performance/cost ratio, together with a great degree of efficiency, as long as the task running on it can be decomposed largely into vector operations. Consequently, the array processor is best suited to the air-traffic control problem discussed earlier, to the processing of weather information (this involves partial differential equations) and to tomography where the output of a body-scanner is processed almost entirely by vector arithmetic. As s.i.m.d. architecture is generally built around a central processor controlling an array of special-purpose processors, the s.i.m.d. architecture is not discussed in any further detail here.

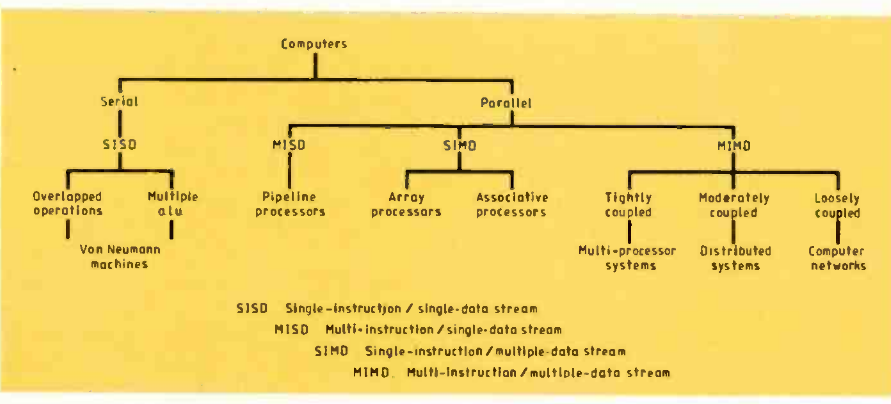


Fig.2. Graphical illustration of the classification of multiprocessor systems according to Fathi and Krieger.

MULTIPLE-INSTRUCTION/ SINGLE-DATA STREAM

The m.i.s.d. architecture performs multiple operations concurrently on a single stream of data and is associated with the pipeline processor. A pipeline processor is best described in terms of an analogy with an automobile assembly line, where a single stream of components is operated on by a number of sequential processes to produce the finished automobile.

For example, four cars may be in the pipeline at any instant with a different operation being applied to each car. A complete car is produced after a car has passed through each of the stages in the pipeline and has been operated on at each stage.

In multiprocessor terms, the various processors are arranged in-line and are synchronized so that each processor accepts a new input every t seconds. If there are n processors, the total execution time of a task is nt seconds. At each epoch, a processor takes a partially completed task from a down-stream processor and hands on its own task to the next up-stream processor. As a pipeline processor has n processors operating concurrently and each task may be in one of the n stages, it requires a total of nt+(K-1)t time slots to process K tasks.

Reduced instruction-set (risc) microprocessors use pipelining to achieve a high throughput. At each clock cycle, one stage of the pipeline of the processor is fetching an instruction, one stage is decoding an instruction, one stage is executing an instruction and one stage is storing the operand from the previous execution stage. Multiple-instruction/single-data-stream systems are highly specialized, requiring special-purpose architectures, and are not discussed further here. In fact, m.i.s.d. architectures have never been developed to the same extent as s.i.m.d. and m.i.m.d. architectures.

MULTIPLE-INSTRUCTION/ MULTIPLE-DATA STREAM

The m.i.m.d. architecture is the most general-purpose form of multiprocessor system and is represented by systems in which each processor has its own set of instructions operating on its own data structures. In other words, the processors are acting in a largely autonomous mode. Each individual processor may be working on a subsection of the main task and does not necessarily need to get in touch with its neighbours until it has finished its subtask, Fig.1.

Because of the generality of the m.i.m.d. architecture, it can be said to encompass the relatively tightly-coupled arrangements discussed in my next article, and the very loosely-coupled geographically distributed local-area networks. Figure 2 provides a graphical illustration of the classification of multi-processor systems according to Fathi and Krieger (*IEEE Computers*, March 1983, Multiple Microprocessor Systems: What, Why and When).

Alan ...Clements, BSc., PhD., is... a reader in the School of Information Engineering at Teesside Polytechnic.

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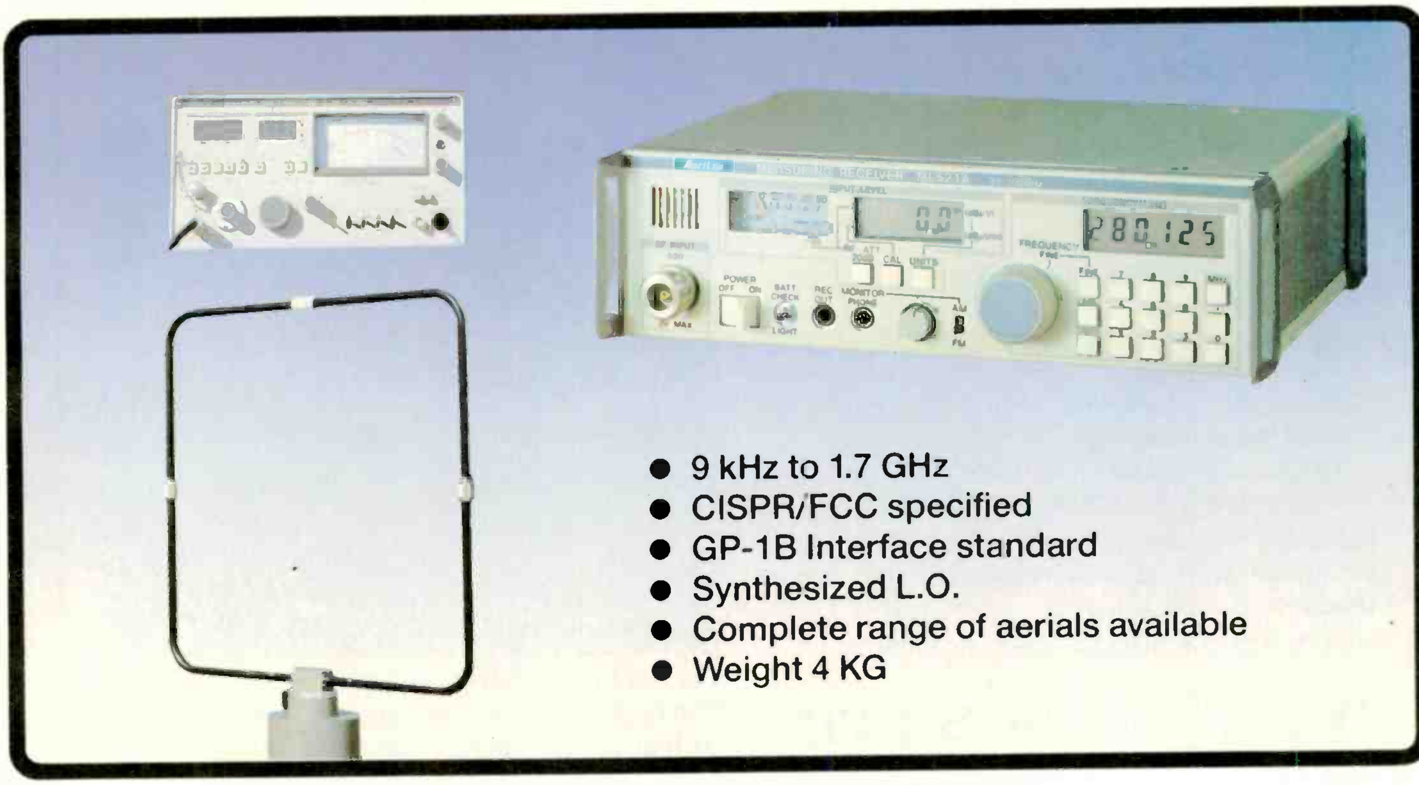

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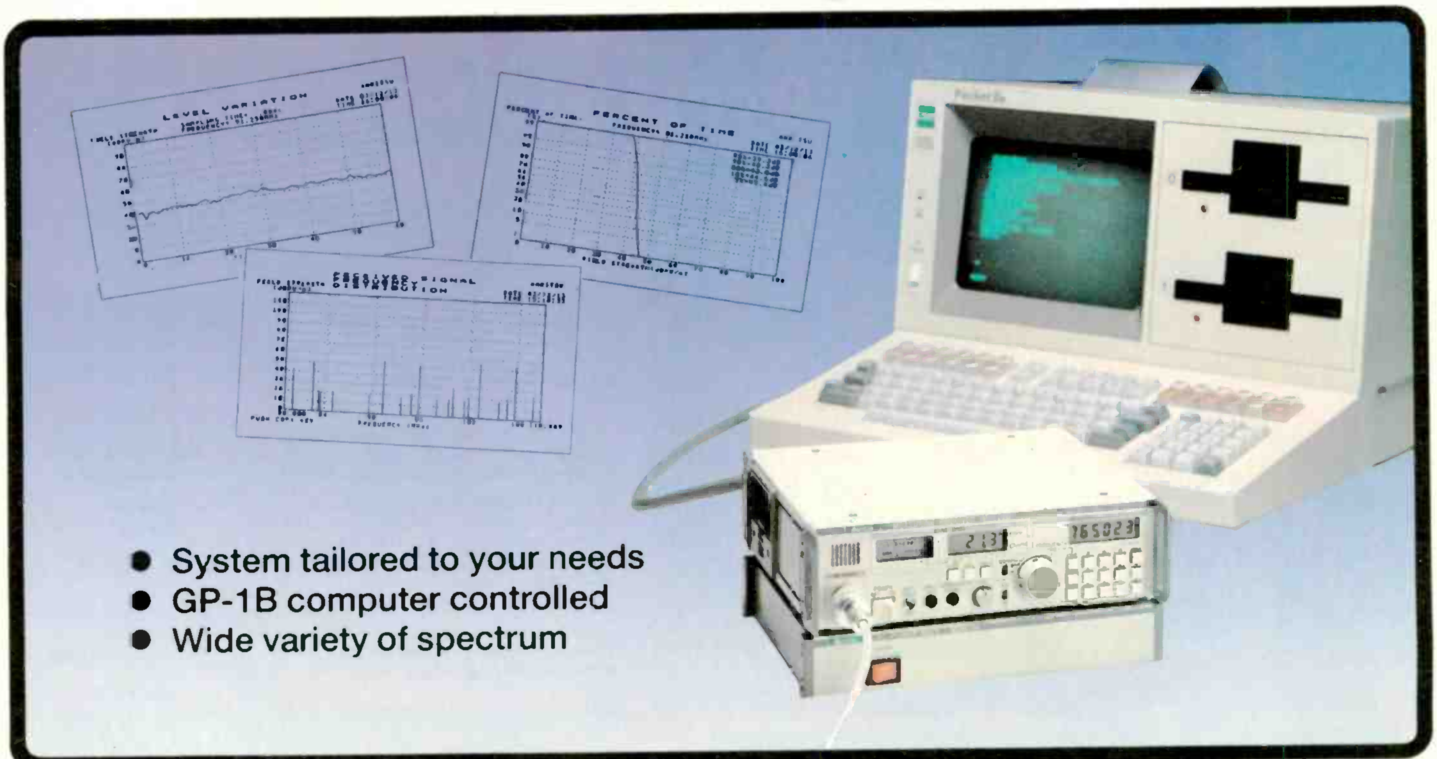

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FEEDBACK

Confessions of a frustrated inventor

Who ever thought that an article in a technical journal could move me this way? And still that is what happened when I read "Confessions of a frustrated inventor" by Heinz Lipschutz in your March issue. To be honest, my emotions were mainly the product of self pity, because a lot that Mr Lipschutz wrote about was recognized by me from personal experience. The way he described his case was impressive and piteous as well, starting with a cool account of the facts, and ending with a hardly hidden outburst of rage. The subject of technology may seem to be down-to-earth and emotionless to most people, but when a man devotes the best hours of his day, and the best years of his life to a technical subject, then it becomes a real part of his reason for living. If it then appears that "the world" denies his brain-child or even does not want to know it at all, then something breaks inside. And believe me: cool reasoning in this case will not help a bit.

Mr Lipschutz wanted to do a favour to a whole country, England. My objectives were a little smaller. I work in the i.c. department of a big Dutch firm, and now and then I am plagued by some brain-wave, concerning the design or the simulation of i.cs. For instance, two years ago I discovered a new design method for c-mos standard-cell ics, which would make them about half the size. I wrote an article about it, well-documented and polished qua writing style, and sent it to some group leaders. But reactions were nearly absent. Then I remembered that people in industry are not interested in plans but only in complete solutions, so I started to work out the ideas myself, which was not easy because I had to retrain myself to be a software writer. I did the work mainly in spare time. Some people might think that I am crazy, but I'm unable to stop when I have a good idea.

I took a part of an existing i.c. and implemented it in two ways: the old way, and by means of the program I had written. I depicted the implementations on the same sheet of paper, so it would be clear to everybody that there was indeed a big area difference. I wrote some accompanying text, sent it to several people, and started to wait until everybody would begin 'phoning, writing and asking for further information! As you may guess, I'm still waiting. Now and then a colleague asks how the project continues, and somebody has done a half-bred investigation on it, but that's all.

This case is only one example of many similar experiences; however, sometimes the reaction was not lack of interest, but aggression. I always tried to find out what were the mechanisms behind the rejection of my ideas. One problem is that the persons who are important for the appreciation of new ideas are exactly the ones that are responsible themselves for the generation of such ideas. So personally they have nothing to earn with it. The managers, supposed to be interest in earning money for the company, do not like new ideas too, because they cannot judge them, being no technicians. And the average designers, my dear colleagues, do not like new ideas at all, because then they have to learn new things or make choices, and life is too difficult already.

As you may understand, I have become a little cynical about the nature of people in organizations. That however does not stop me from being surprised or disappointed occasionally, especially when I find out that nothing helps: writing, talking, explicitly asking questions. Working for an idea and bringing it to a good end is a very exciting experience, but you never get really used to apparent lack of interest in the things you have put your heart in.

W. Boeke
Hilversum
Holland.

I confirm from decades of experience that the plight of the inventor and his invention is quite as bad as Heinz Lipschutz asserts in *EWW*, March, 1988.

I quote from his article;

"A major problem I discovered was the inability to get a fair hearing. The reason was a 'Catch 22' situation in that nobody wanted to know, having never before even heard of me, and that most of the media did not want to publish anything by me for the same reason, so that as a consequence nobody heard of me."

I have all the credibility he feels he needs. The British Government has spent £100,000 on my invention (*WW*, July, 1981). I have received hundreds of thousands of pounds for my patents. Millions have been spent on my ideas. However, I am absolutely sure that I would not receive a fair hearing, or any hearing at all, for my next invention. This is in spite of the fact that everyone seems to have heard of me. No one, including myself, will ever gain credibility in Britain as an inventor.

References.
Management against innovation, *The British Business Graduates' Association Journal*, Summer 1977.
The NRDC – failing in its duty? *WW* May 1978, page 48.

Ivor Catt
St Albans
Hertfordshire

Instrumentation amplifiers

In the April edition of *EWW* you published two letters criticizing some aspects of my February article on instrumentation amplifiers and I would like the opportunity to reply.

It is quite clear in the analysis that I presented that both the differential gain and common mode gains refer to the output voltage of each amplifier in relation to the input terminal voltages, and in so doing there is a tacit assumption that the source impedances of the signals applied to the inputs are negligible with respect to the input impedances. When processing any voltage information from a signal source, it is clearly important to ensure that the input impedance is very much greater than the driving source impedance. The input buffering action in the three-op-amp circuit does indeed give the instrumentation amplifier some advantages in this respect and I touched on this aspect in the final paragraph of my article.

To evaluate the effects of non-zero and imbalanced driving source impedances on the single op-amp differential amplifier, the values of R_2 and R_3 need to be modified to R_1' and R_3', given by

$$R_1' = R_1 + R_{S1}$$
and $$R_3' = R_3 + R_{S3},$$

where R_{S1} and R_{S3} are the Thévenin equivalent source impedances driving the inverting and non-inverting inputs respectively. With this substitution the rest of the analysis remains the same and the effects of R_{S1} and R_{S3} only degrade the single op-amp differential amplifier.

The purpose of my article was to focus on the less obvious aspects of enhanced c.m.r.r. offered by the three op-amp instrumentation amplifier that accrue significance only when the gain-bandwidth product of the complete differential amplifier cannot be achieved with a single op-amp circuit, such as the standard differential amplifier.

Both critics misquote my concluding remarks. I do not claim without qualification that the three op-amp instrumentation amplifier offers no significant advantages over the single op-amp differential amplifier; the qualification being, as stated above, when the specified gain-bandwidth product of the complete amplifier can be achieved with a single op-amp circuit.

John Lidgey
Oxford Polytechnic
Oxford

Convolution

Howard Hutchings points out the difficulty of visualizing the process of analogue convolution in his excellent article in the February issue. The following explanation should be more helpful than the standard method based on sliding two graphs across each other.

Consider a system with a response h(t′) to a unit impulse where t′ *is the time after the impulse is presented to the input.* A unit impulse or delta function has an area of 1; therefore an impulse with an area A will produce a response of Ah(t′).

If a series of pulses is applied to

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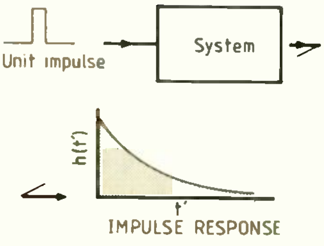
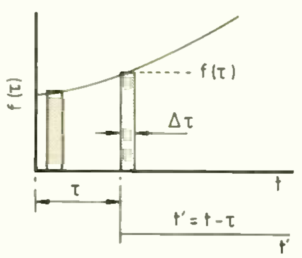


the input, then each one will contribute its own Ah(t') to the response.

Now, a continuous function applied to the system can be considered as a series of narrow pulses. Note that t is real time. A



pulse occurring after a time τ with width $\Delta\tau$ will have an area $f(\tau)\Delta\tau$ and for this pulse $t' = (t-\tau)$.

So the contribution of this pulse is

$$Ah(t') = f(\tau)\Delta\tau \times h(t-\tau)$$

The contribution for all pulses will then be

$$\sum_{-\infty}^{+\infty} f(\tau)h(t-\tau)\Delta\tau$$

or, in the limit, the response r(t) is then

$$r(t) = \int_{-\infty}^{+\infty} f(\tau)h(t-\tau)d\tau$$

This is the convolution integral. It should be remembered that the unit impulse contains all frequencies, so that when transformed to the frequency domain, the impulse response h(t) gives the system frequency response H(ω). Thus, if the input signal is F(ω), then the output response R(ω) will be

$$R(\omega) = F(\omega)H(\omega)$$

This is the immediate result if the convolution integral is transformed to the frequency domain.

I hope this will be helpful to readers.

T. Green
Bicester
Oxfordshire

Seven per cent

I am afraid Mr Catt (April) has not made any new discovery, but has merely expressed in a different form the well known Zipfs Law of word occurrence. This was originally published in 1949 in the book Human Behaviour and the Principle of Least Effort.

This law states that the number of occurrences of a word in a long length of text is the reciprocal of the order of frequency of occurrence. For example, the tenth most frequent word occurs about 1/10 as many times as the most frequent word.

Applying this law to Catt's text of 16384 different words gives the following –

Let N = frequency of the most common word.

Then

N + N/2 + N/3 + N/4 + ... N/16384 = 16384.

Therefore

N(1 + 1/2 + 1/3 + 1/4 + ... 1/16384) = 16384.

Therefore

10.2813N = 16384

and

N= 1594

From this, the frequency of word ranking can be calculated.

Rank	Frequency	Cumulative percentage
1	1594	9.729
2	797	14.594
3	531	
4	399	20.270
5	319	
6	266	
7	228	
8	199	26.447
9	177	
10	159	
11	145	
12	133	
13	123	
14	114	
15	106	
16	100	32.898

Thus it will be seen that each binary doubling of ranking increases the percentage frequency by approximately 7%, as Catt suggests.

It can easily be shown, by adding together the reciprocals in the Zipf series, that each binary doubling will give an equal increase in frequency.

It will thus be seen that Catt's 7% rule can be derived from Zipf's Law.

Benoit B. Mandelbrot, who was later to achieve fame

Rank	Reciprocals	Sum of reciprocals
5-8	1/5-1/8	0.6345
9-16	1/9-1/16	0.6629
17-32	1/17-1/32	0.6777
33-64	1/33-1/64	0.6854
65-128	1/65-1/128	0.6892
129-256	1/129-1/256	0.6912
257-512	1/257-1/512	0.6922
513-1024	1/513-1/024	0.6926
1025-2048	1/1025-1/2048	0.6929
2049-4096	1/2049-1/4096	0.6930
4097-8192	1/4097-1/8192	0.6931
8193-16384	1/8193-1/16384	0.6931

through his work on fractals, suggested a theoretical basis for the law.

Zipf found the law applied in many other areas besides word frequencies, such as the populations of cities within a given country.

G.R. Turner
Stourbridge
West Midlands

The observer in Science

Tom Ivall's article 'The observer in science' (April) leaves the impression that many philosophers, once they have formulated a model of scientific and technological activity, don't question too closely whether scientists actually behave according to the model. The empiricists at least could not have been expected to appreciate that the brain's forte lies in imposing patterns on arrays of objects, in detecting systematic changes in these patterns, especially periodic changes, and above all in detecting moving objects. These facilities, which are essential for any animal that wishes to find its way around, to find things to eat, and to avoid being eaten, represent a big advance on Locke's 'white paper'.

With them an alert shepherd, watching over his flock at nights for months or years in the same area, can discover for himself the regular rotation of the pattern of stars, the cycles of the moon, the seasonal changes in the position of sunrise and sunset, and even the erratic motion of some 'stars' ('planet' is derived from a Greek word meaning wanderer). This knowledge of astronomy he acquires in the way foreseen by the empiricists. The experiences of shepherds may be unfamiliar to modern city dwellers, but they form the backcloth to life in biblical times. However the complex pattern of planetary movements is unlikely to be unravelled except by someone who first assumes that such a pattern exists, and then deliberately looks for it.

Anyone attempting to codify planetary movements may well produce some sort of 'model' to act as a mnemonic. For this purpose even a tale of the goings-on of gods and goddesses may serve. In fact our notions of 'red', of 'animal', etc. are no more than models, to be adjusted as we gain increasing experience of the outside world. If anything they are less absolute than the models of the physicist, otherwise why so many arguments about the colours and patterns of carpets, clothes and curtains?

Philosophers may have persuaded themselves that an observer and the system he observes are interdependent, but it is far from obvious to those actually engaged in physics experiments. Nowadays the details of the experimental configuration and the way in which the experiment is to be run will as likely as not be entered into a computer, and subsequently set up automatically. If the experimenter were to be killed in a road accident before the experiment began, that would hardly affect its outcome. In fact the interaction between the observer and the system observed is immaterial: what really matters is the interaction between the equipment used for the measurements and the system observed.

It is even possible to make a random choice of the measurements to be performed. Aspect's experiments demonstrating violations of Bell's inequality (deduced from Special Relativity) come very close to this, and provide some of the clearest experimental evidence for the quantum mechanical predictions that in certain cases the system used to make measurements must inevitably affect the state of the system measured.

C.F. Coleman
Grove
Oxfordshire.

A. Aspect, J. Dalibard, and G. Roger, 'Experimental Tests of Bell's Inequalities Using Time-Varying Analyzers', *Phys. Rev. Letters* 49 (1982) 1804-1807

One aspect of observation not discussed in Tom Ivall's other-

FEEDBACK

wise excellent article in the April issue of *EWW* is that the capabilities of human senses are restricted in just the same way that there is a limit of detection for all experimental procedures and the instruments used in them. At very low intensities of stimulus, a human observer is unable to tell with certainty whether an event external to the body has happened or not. Psychologists call this the limen of perception and assign a probability of 0.5 to all sensory experiences at this level. This constraint will, therefore, also apply to all human knowledge that has been acquired by accumulation of sensory experience within an evolutionary context.

Since, in addition, nervous activity depends on electrical pulses ('action potentials') and an 'all-or-nothing' mechanism, it follows that all events in the Universe will be perceived as being quantized, whether or not they are in terms of 'objective reality'. The implications of this are far-reaching and, unless they are recognized by physicists and others, will continue to provide stumbling blocks to the rational solution of problems. The ultimate truth is that all procedures in logic end in paradox, resolveable only by arbitrary toss of a coin. Curiously, this makes fitting conceptual models to experimental data much easier.

B.E.P. Clement
Crickhowell,
Powys.

Frequency changes

We are very pleased to hear that your correspondent Mr West (May Letters) is generally able to enjoy Radio 4 long wave in Villereal, and that the sound quality is good.

Radio 4 long wave moved to 198 kHz at 0100 on 1 February, 1988 to come in line with the International Frequency Plan referred to by Mr West. This change follows from an agreement at the 1979 World Administrative Radio Conference which assigned frequencies in the long-wave band to a 9 kHz spacing. This agreement will also extend the band, eventually, to 283.5 kHz.

The change has been co-ordinated internationally in three stages. Whilst most broadcasters concerned changed frequency on 1 February as required under stage 2 of this process, the 1 MW Algerian transmitter is still on 200 kHz. Depending on the propagation conditions, this can cause a 2 kHz heterodyne when listening to any service on 198 kHz. This is the most probable source of Mr West's problem.

We have asked the Algerians to come into line and adopt 198 kHz too, and hope they will soon change.

Mick Gleave
Asst Head, Engineering
Information Department
BBC
London

Flow charts

Mr Medes (April Letters) shows that thinking which will do for hardware design may well be too sloppy to work when programming. His Fig.1 shows something inherently impossible and which cannot exist. If both inputs R and S are low, then both outputs are high and *cannot be Q and not Q*. Also, if R and S change simultaneously from low to high, the outputs are indeterminate. Of course, in the world of hardware there are unwritten conventions for dealing with these awkward situations, but in programming everything relevant must be stated explicitly. It is silly to compare the diagram of the RS flip-flop with code that does more than the diagram. If you remove the absurdity and call the outputs X and Y, and if you ignore the awkward case of indeterminate outputs, you then get

```
IF NOT (R AND S)
  THEN
    X: = NOT R;
    Y: = NOT S
  END;
```

That should make it perfectly clear what the flip-flop does, even to someone who doesn't already know! I can't think why Mr Medes should take such evident pride in having produced the bad code in his Fig 2. No, Mr Medes; hardware and software *are* such different things that you can't get away with mixing them as you have tried to do.

Mr Sweeney rightly disparaged his little piece of code on the grounds that its straight left margin made it unclear. Now Mr Medes tells us that wavy lines are the bane of the computer industry. I must learn to program in Arabic (so as to get a wavy right hand margin) in the hope that that is less offensive than waves on the left.

Mr Medes makes me chuckle at his attempt to merge into one person ROss and praTT; ROTT? I hope Mr Ross doesn't mind!

J.G.D. Pratt
Leatherhead
Surrey.

It's not often that I need to reply to a magazine article, but A. Medes of Australia's letter, in your "Feedback" column in the April issue, contained many statements about computer science which are not accurate, especially concerning flow charts. His comparison of them with circuit diagrams is very misleading and as someone reading a joint degree in both fields I feel I must correct him.

Circuit diagrams, as you must realise, show all the physical information about a circuit, with the exception of the actual p.c.b. lay out and are generally the best representation of a circuit, whereas flow charts in no way show all the program details. For example such important issues as data structure and scope are not shown on any flow chart which I've seen, but even worse the programme structure itself may be changed in representing it in a flow chart: for instance consider the recursive program segment:-

```
fac(x)<=(1  IF  x=0  ELSE
         fac(x-1) * x);
```

This is closer to the circuit diagram than a flow chart in that it completely describes all the information about the function, it could even be used to define the factorial function. It is also like a circuit diagram, in that does not contain the actual implementation details.

I would like to see a flow chart which comes as near to representing the program as well as the above line, without converting it to a iterative version first. Flow charts were used, when the languages about were flat and all the under-laying workings of the computer were apparent to the programmer. In the above segment the cogs of the program are hidden, like in most modern languages but unlike in older "Fortran"-like languages.

Finally, flow charts like pseudo-code are only programming aids: in the future, languages will become more natural to write and the workings of the computer will be hidden from the programmer, as in the case of the new massively parallel computers being made, where we will not have any choice but to hide the implementation details and whether we use diagrams or text to represent the new highly structured languages being written for them, is only "syntaxic sugar", but flow charts as they stand, come no way near to being expressive enough.

D. Celano
Swindon
Wiltshire

Moving-coil head amplifier

I would like to thank Mr Nalty (April) for his generous praise of my moving-coil preamp design. However, I winced to read his next sentence "Every competent engineer knows that the inclusion of electrolytic capacitors in the signal path will seriously distort its sound quality" This is quite untrue.

Mr Nalty blames 'dialectric absorption' (*sic*). Perhaps he means 'dialectic absorption', which my dictionary defines as testing the truth by logical disputation. Nothing would please me better, so long as we can keep both sides of the disputation logical.

The use of electrolytics in audio paths sets two major traps for the unwary, neither of which Mr Nalty addresses. The first is a slight tendency to microphony, which is unlikely to be detectable at the signal levels found in pre and power-amps. The second, and more important, is the possibility of a sharp rise in non-linear distortion at low frequencies if a signal voltage across the capacitor is allowed to develop. This point was thoroughly explored, if not actually beaten to death, in EWW two years ago[1]. Neither of these tediously practical consid-

FEEDBACK

erations seem to have caught the imagination of the Subjectivist Tendency.

My design makes no reference to component specifications (of the sort that Mr Nalty means) because they have no basis in reality. Any well-brought-up electronic circuit should be insensitive to tolerances in conventional parameters; in my professional capacity the circuitry I design is reproduced by the thousand, and so any other approach would be disastrous.

The cartridge loading resistor is just a resistor – 5% carbon film is quite adequate – and to put it bluntly, anyone in audio who spends £10 on a resistor is a fool.

The root of the problem is that Mr Nalty, as a hard-line Subjectivist, feels free to put forward as facts assertions that are lamentably devoid of a shred of supporting evidence. He dare not even hint at what sort of mechanisms are involved, or describe their effects on a signal, for fear that a quick experiment will show that they are illusory. Has Mr Nalty made any measurements on capacitors in real-life circuit situations? I think we should be told.

One of the few definite statements that Subjectivists have been tempted into making is that electrolytics (and indeed, copper wires) suffer from a sort of low-level crossover distortion that can be heard but not measured. It did not take me long to prove that if any such effects exist they are well below the −150 dBu level, and if that is not audible I should like to know what is[2].

I therefore bluntly challenge Mr Nalty to be more specific in his speculations so that they can be subjected to the ruthless duo of logic and experiment. The scientific method got us to the moon; it is unlikely that it cannot cope with audio.

Douglas Self
Forest Gate
London.

References
1 Letters, *E&WW* Feb. 86, pp43,44.
2 Self. "Ultra-Low-Noise Amplifiers and Granularity Distortion." *JAES* Nov. 1987.

Relativity and engineering

J.C.G. Field quotes an accuracy for Navstar (GPS) of 18 metres. Perhaps engineer Field could put relativity aside for a moment and consider the 18-metre error.

The earth turns on its axis one revolution each 24 hours. Hence the signal from the satellite to the ground observer suffers a phase shift resulting from the Sagnac effect (principle of the laser gyro). Since the satellite is in a 12-hour orbit, the distance between the satellite and the ground observer is continually changing, that is, there is a time rate of change of the Sagnac phase shift, which is a frequency. That frequency should be added to the Doppler in the algorithm but is not.

For a numerical example, consider an observer on the equator in the plane of a polar satellite. His ground position error, as a function of the satellite elevation angle is, then,

elevation angle (degrees)	error (meters)
0	14.15
10	14.4
20	15.25
30	16.7
40	19.0
50	22.7
60	29.9
70	56.7
78.182 (horizon)	infinite
80	−49.7
90	0

The beauty of this observation is that the noted phase shift is compatible, according to the establishment, with both the Special[1] and General[2] Theories of Relativity. Is there an Establishment "cover-up" of this error? You bet!

References
J.C.G. Field, *Electronics and Wireless World*, March 1988.
1. F.C. Michel, *Phys. Rev. D*, vol.19, No.4, 1271, 15 February, 1977
2 J.M. Cohen and H.E. Moses, *Phys. Rev. Lett.*, vol.39, No.26, 1641, 26 December, 1977

E.W. Silvertooth
Olga,
USA

In *EWW* for March, 1988 J.C.G. Field comments on Einstein's theory of relativity on the basis of physical effects of moving bodies and clocks. Referring to such effects is a common method when defending this theory instead of answering the criticism.

The mass-increase phenomenon was initially discovered by Kaufmann in 1901 in cathode-ray experiments, and not predicted by Einstein's theory. It is known that H.A. Lorentz and Abraham Pais had suggested a theoretical formula for it, the formula which the particle physicist uses today.

The relation $E=m.c^2$ was also known and suggested by Poincaré, Hasenöhrl and Langevin independently of Einstein and before him. It is even known that the time-dilation effect was suggested by Larmor in 1900 and the hypothetical length-contraction effect by Lorentz and Fitzgerald some years before. Poincaré was the inventor of "the principle of relativity" as reported from an international congress of Physics at St. Louis, USA, in 1904. The mathematics of space and time was developed by Lorentz.

Obviously, the adduced effects as referred to in the theory of relativity can be deduced from other starting points having nothing with to do relativity and not necessarily erroneous. Hence, we may ask: "What have these physical effects to do with relativity?"

The theory of relativity has been criticized mainly on the basis of its invariant light hypothesis, the hypothesis constituting the base of the theory. Einstein himself said: "If the speed of light is in the least bit affected by the speed of the light source, then my whole theory of relativity and theory of gravity is false". Dedicated relativists try to muddy the water by talking about other things when this criticism appears, neglecting what the critics are trying to say: if the base hypotheses of a theory are not correct, the predicted imaginary physical effects of the theory cannot be correct. Dedicated relativists seems to have real difficulties in accepting this simple and obvious fact.

Ove Tedenstig
Märsta
Sweden.

Atomic fission

There is a certain sacerdotal smugness to the assertions proffered by Hankey and Coleman (Letters, March): we are told that "experiments have failed to determine a size for the electron", but that "the two particles do, in fact, have drastically different sizes"; and I did not deny an internal structure for them, as a more careful rereading will show. I warned that the article was "simplistic" in order to dissuade any reader from assuming that the diagrams were scaled, thereby to infer that gamma frequencies need be involved, but some are so fond of the taste of shoe leather that they must perforce open their mouths.

Should any biologist offer an analysis of a cell nucleus which completely ignored its environment, he would be roundly condemned; yet physicists model the atomic nucleus with no reference whatever to the intense, complex, and dynamic electromagnetic field surrounding it, and demand absolute authority for their deductions. Since noone to my knowledge has ever seen a sub-atomic particle (the above gentlemen possibly excepted) our understanding of them must rely on many steps of inference and reasoning, any of which may at some future date be proved faulty or incomplete. As a more cautious commentator observes, "How a particle sits in equilibrium with the aether in a quiet background can be very different from how it appears in our mammoth machines in reacting to high-energy collisions". By investigating the relationship that exists between the e.m. field and the nucleus, there is every chance that we may be able to influence the nucleus indirectly by manipulating the field, and this involves readily obtainable energies, such as from ordinary lasers. My reason for not quoting any numerical values was not that they might be "too complex for EWW readers", but simply because the research needed to establish them has not been done.

Carl Adams
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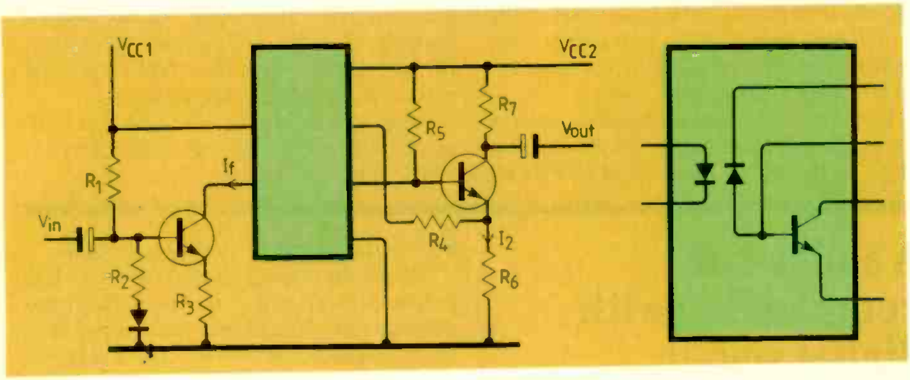
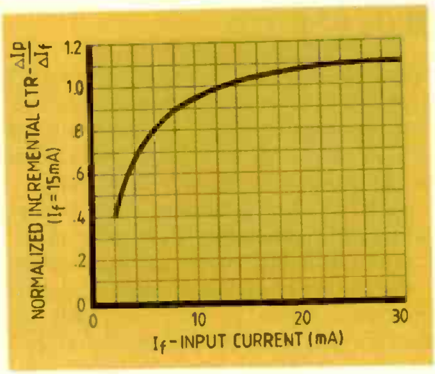
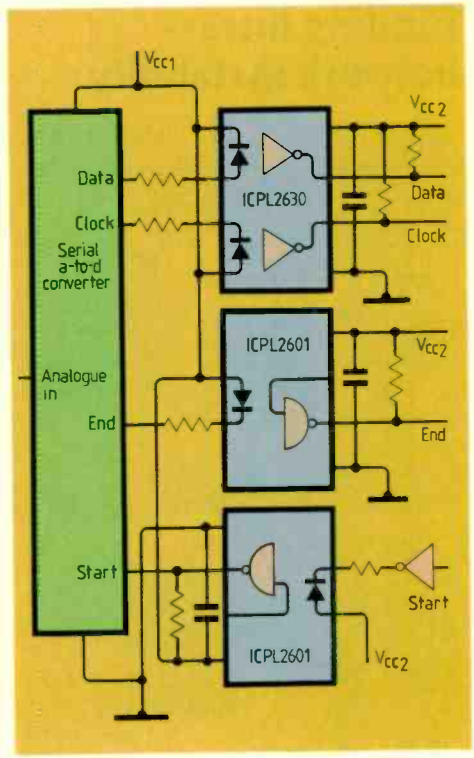
APPLICATIONS SUMMARY



Digital opto-coupling for analogue signals





Direct transfer of analogue signals through opto-couplers, shown in the left-hand illustration, is adequate for many applications but higher linearity and stability can be achieved by passing the analogue information through the opto-coupler in digital form.

With analogue techniques, the smallest achievable linearity error is typically between 0.5 and 1%.

Isocom's Application note No.1 details methods of connecting digital inputs and outputs to opto-couplers to improve linearity and stability. It does not discuss digital encoding techniques but it does give a good description of switching considerations for opto-couplers.

Included in the three-sheet note is a brief outline of the computer interface shown on the right. The graph shows that, for analogue coupling, linearity improves as input current rises.

Cordless telephone receiver

Audio amplification, second conversion and second i.f. demodulation sections form the ULN3883A dual-conversion receiver i.c. This low-power device, designed for narrow-band f.m. i.f., is used here as part of a cordless telephone.

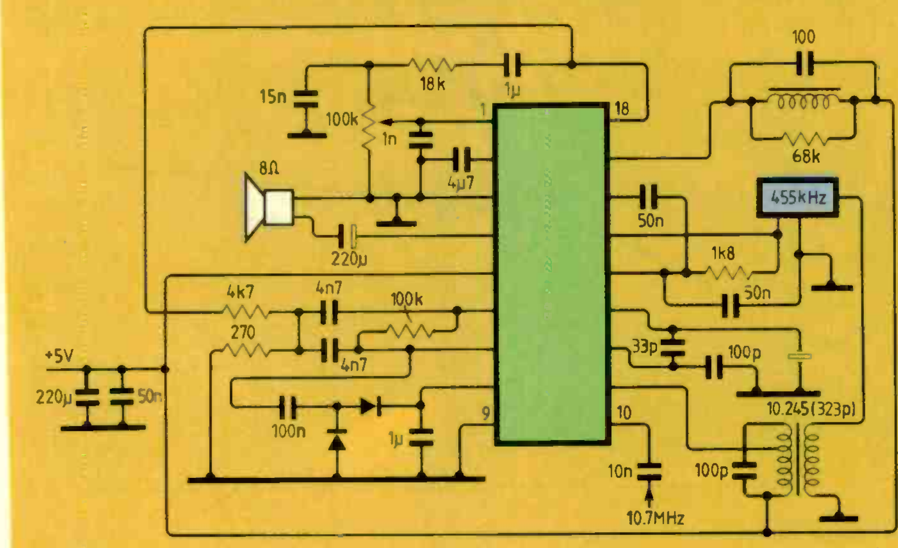
Conversion of the 10.7MHz first i.f. to 455kHz is done by the 10.245MHz crystal. A tuned transformer matched to a ceramic filter with 15kHz bandwidth forms the 455kHz filter.

Output of the ceramic filter is matched with a 1.8kΩ resistor at the i.f. amplifier input. Loading the detector coil with 68kΩ gives a Q of about 25 to produce an audio output of around 170mV r.m.s. for a 3kHz peak deviation. Since this is more than enough to drive the audio amplifier, an RC network can be inserted between the detector output and volume control to provide de-emphasis.

Muting is accomplished by amplifying noise present at the detector output in the absence of a signal, rectifying it and applying the rectified signal to the mute input. When voltage at pin 8 exceeds 0.6V, the audio amplifier turns off.

The internal op-amp between the detector output and rectifier circuit forms an active bandpass filter with 7kHz centre frequency. This filter should be designed to respond to the guard-tone signal being transmitted.

Also in the Sprague ULN 3883 data/applications sheet are test circuits and a circuit similar to this one but taking advantage of the good signal-handling capability of the i.c's mixer.



Addresses

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Jack 17
Spaceheights Ltd
6 Prospect Place
Chapelhay, Weymouth
Dorset DT4 8JY
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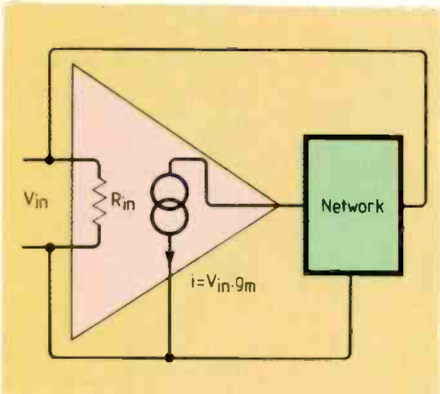
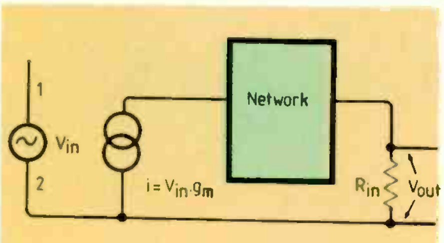
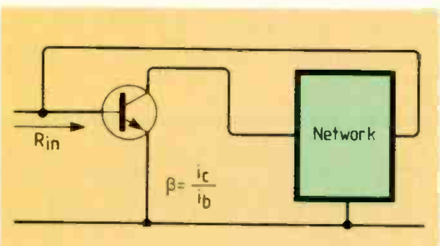
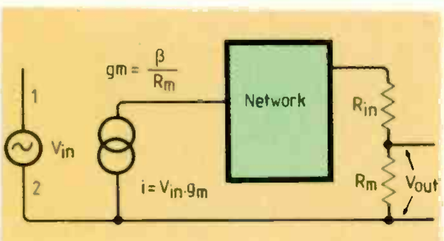
Applications Summary

Finding linear-network instability









The 'Practical guide to the analysis of linear electronic circuits using a personal computer' is specifically written with the Jack 17 analysis program in mind, but much of its information could be helpful to users of other analysis programs.

One example from the Spaceheights guide, case study 13, is concerned with tracking down instability. In Jack 17, amplifying devices can be specified in terms of mutual conductance. To track down instability, the guide suggests that after finding the offending loop, you break it immediately before the mutual conductance in the amplifying device. Next, the conductance is driven with a signal and the resulting voltage between the nodes that normally drive the conductance is measured. If the measured voltage ratio is greater than or equal to one at every frequency where the phase is zero degrees then the network is unstable. If the ratio is less than unity at zero degrees, the network is stable regardless of how large the ratio may be at other phase angles.

In the two uppermost diagrams, gain of the amplifying device is expressed in terms of g_m so the device input resistance forms the load over the output. In the second example, current gain is specified. Output of the loop is taken across current-measuring resistor R_m through input resistor R_{in}.

Other case studies in the guide are concerned with procedures for creating circuits and devices.

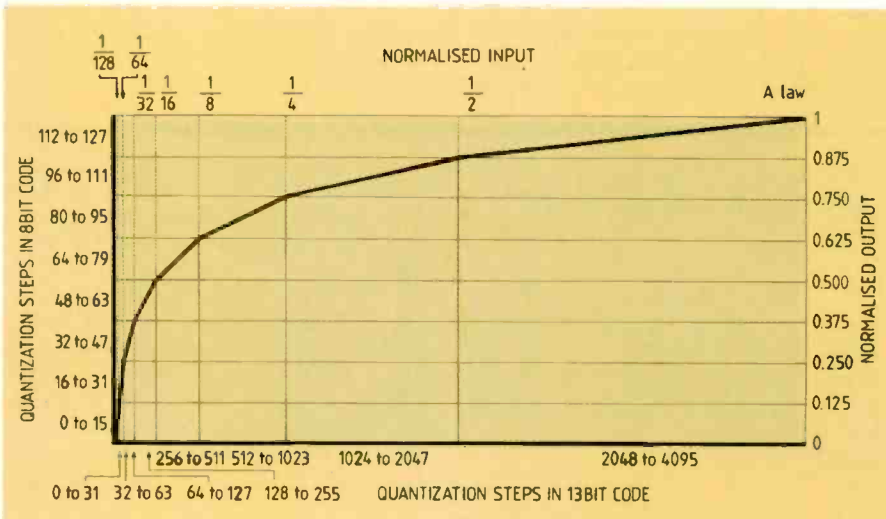
A and μ-law companding with digital signal processors

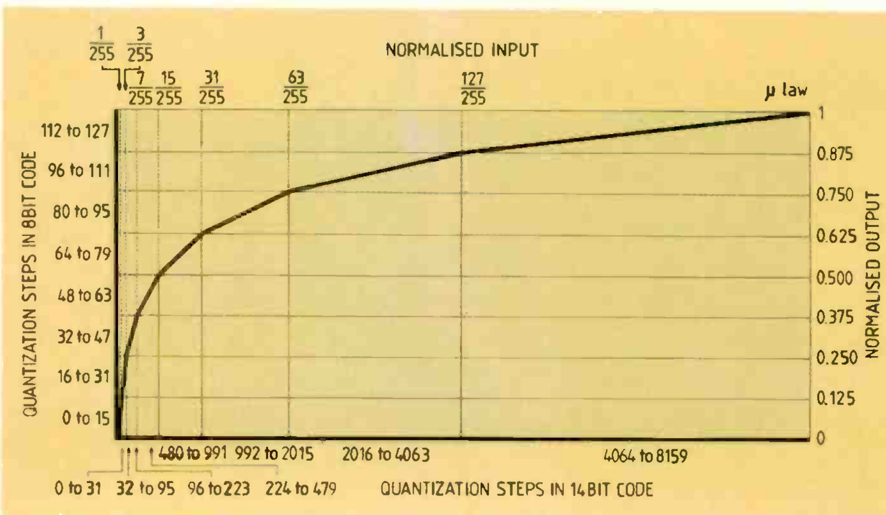
Pulse-code modulation is used to transmit voice signals over digital communications networks since it allows analogue signals such as speech to be reliably transmitted with a relatively low signal-to-noise ratio.

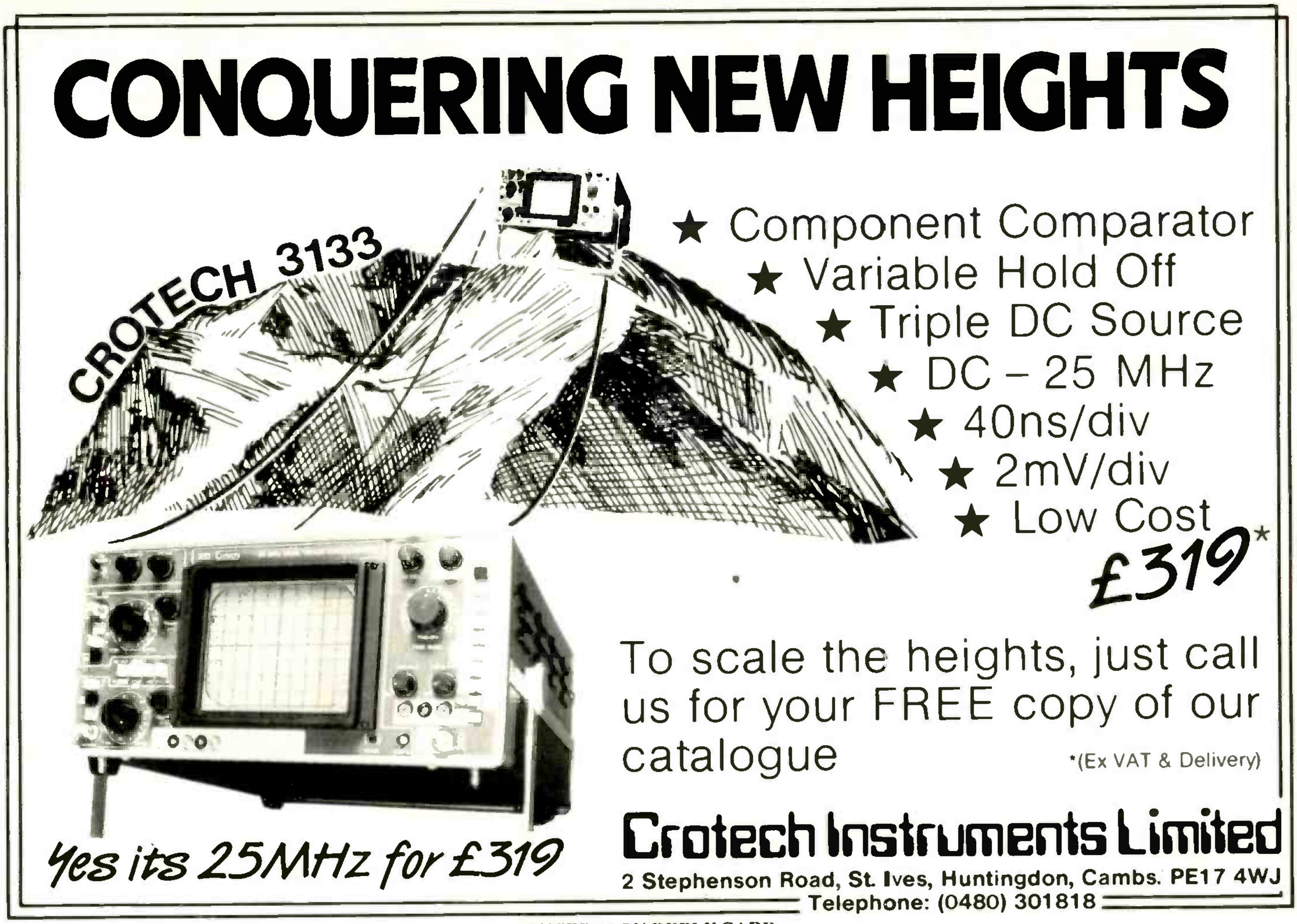
Transforming continuous band-limited signals into p.c.m. requires sampling, quantization and binary encoding. Quantization errors occurring during analogue-to-digital conversion appear as distortion, and the effect of this distortion depends on two factors: quantization step size (resolution) and characteristics of the analogue signal.

Simply decreasing quantization step size reduces distortion but increases the transmission rate. Non-linear characteristics of the analogue signal however can be compensated for by companding, with relatively few disadvantages. Companding provides a constant signal-to-noise ratio over a large dynamic range.

Digital companding is the subject of an application note from Philips called 'μ and A-law companding with the PCB5010 and PCB5011'. The PCB devices are signal processors so the note obviously contains specific information on how to produce companding software for these i.cs. But it also contains good descriptions of A-law companding, which is essentially logarithmic, and μ-law companding, which gives better s-to-n ratio at lower levels.







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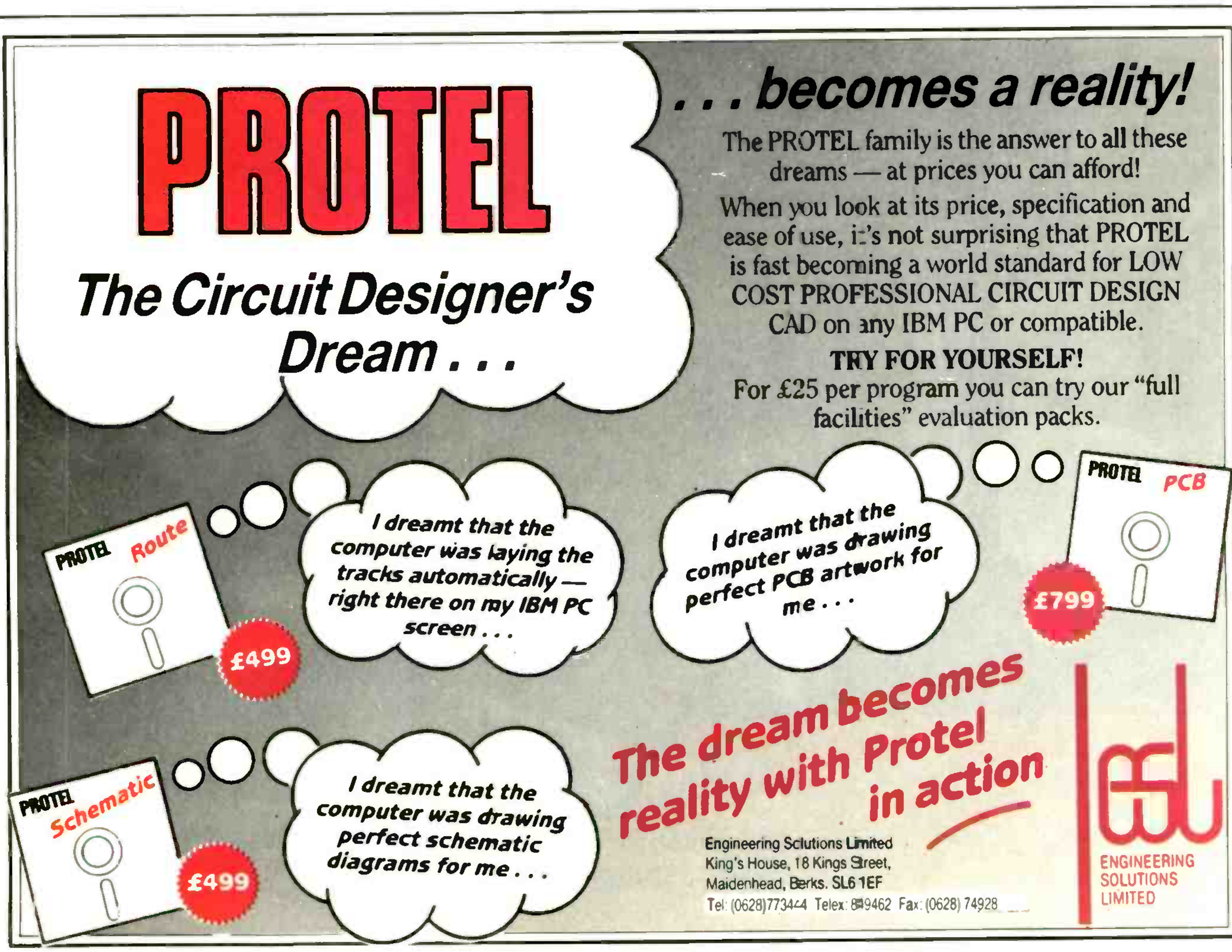

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Phase from amplitude

A numerical method for determining phase response of a network when the amplitude is known.

D.V. MERCY

It is possible to derive the phase response of a network from details of its amplitude response, and vice versa, provided that the network in question is a minimum phase-shift type. Two similar conditions relate the real and imaginary components of a network function. Consequently, no one parameter can be specified independently of the others and this was shown by Bode[1] to be very relevant to feedback amplifier design. The relationships are also useful when determining other properties of minimum phase-shift networks, such as their transient behaviour, if data on only one parameter, say the amplitude response, is initially available.

The equations which relate amplitude and phase can be expressed in several ways. However, the derivation of these equations is not discussed in detail, since this work is well covered elsewhere. (For example, the results have been obtained directly by means of contour integration in the complex plane[1,2,3,4], and as special cases of Hilbert transform relationships[5]).

A common problem with these results is that they contain integrals which cannot be evaluated analytically except for a few special cases. Even then, the calculations are not trivial and are time consuming if great accuracy is required.

Bode demonstrated how to find the phase response from the amplitude response by a graphical method, making use of an amplitude characteristic which he called the "semi-infinite characteristic of attenuation". This is shown in Fig.1(a), which indicates zero loss up to frequency ω_0 and an attenuation above this frequency which increases at 6dB per octave or at 20dB per decade or, using a unit favoured by Bode, at 1 neper per e (=2.718) times increase in frequency. The phase curve corresponding to this attenuation chracteristic has been calculated and is shown in Fib.1(b). It was given by Bode in his book, with more accurate tables published subsequently by Corrington[6] and Thomas[7]. Incidentally, it should be noted that the phase curve uses ω_0/ω as the independent variable for ω less than ω_0 and ω_0/ω as the independent variable for ω greater than ω_0. This follows the practice of Thomas and proves to be useful later.

With the graphical method, a suitably scaled combination of "semi-infinite characteristics" is chosen which closely approximates to the amplitude response. The corresponding phase response is derived by summing similarly scaled versions of the phase curve in Fig.1(b).

An alternative attenuation characteristic, for which the phase curve can be calculated, is given in Fig.2. This curve, called the "finite line segment characteristic" was also used by Bode and later investigated by Murakami and Corrington[4]. It is derived by summing two semi-infinite, constant-slope characteristics which have different cut-off frequencies ω_1 and ω_2, but equal slopes. As above, the output result is obtained by summing data from scaled graphs or tables. Murakami and Corrington give a large number of curves for various values of the ratio ω_2/ω_1 which allow the phase to be derived from amplitude and, in addition, they give curves which allow amplitude to be derived from phase.

More recently, Sekey[8] has demonstrated a numeric method, suitable for computer evaluation, which avoids the use of graphs or tables. However, the procedure obtains group delay rather than phase from the attenuation data. The results were estimated to be accurate to about 10%.

In 1980, in unpublished work, S. Blake developed a direct numeric procedure with which to obtain phase from amplitude, while carrying out an investigation into permissible tolerances for radar receiver parameters. The solutions in this article are based on his methods, although the detailed development and results differ somewhat. In addition, the inverse problem (that of deriving amplitude from phase) is also solved numerically here.

RELATING AMPLITUDE AND PHASE

If f(s) is the input impedance, input admittance, transfer impedance or transfer admittance of a network, then the general expression for the response function to be considered in this paper is

$$f(s) = K.s^L \frac{(s+a_1)(s+a_2)............(s+a_M)}{(s+b_1)(s+b_2)..........(s+b_P)} \quad (1)$$

The following constraints are to apply to the expression:

(i) There are Z zeros in total, with L zeros at the origin and M in the left half plane. No zeros exist in the right half plane.

(ii) There are P poles, all in the left half plane and $P \geq Z$.

(iii) All the a's and b's occur as real numbers, or if complex, in complex conjugate pairs. Figure 3 gives a general schematic of f(s), showing an typical group of poles and zeros in the s plane.

The function f(jω), the value of f(s) along the jω axis, can be expressed as

$$f(j\omega) = u(\omega) + jv(\omega) \quad (2)$$

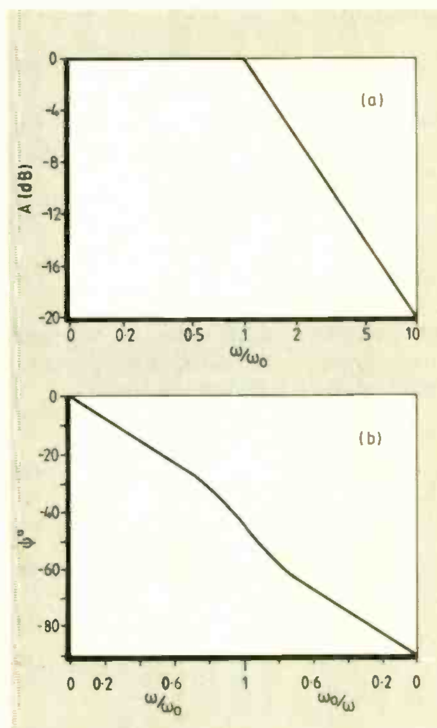


Fig.1. Bode's 'semi-infinite characteristic of attenuation' and accompanying phase curve, derived graphically.

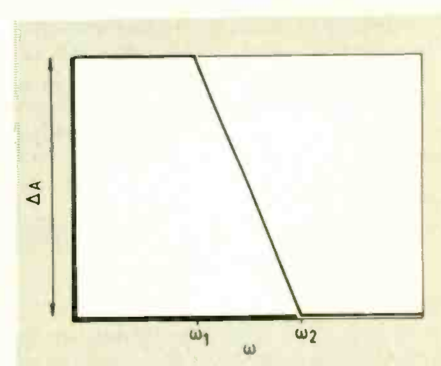


Fig.2. 'Finite line segment characteristic' enables phase curve to be calculated.

where $u(\omega)$ and $jv(\omega)$ are the real and imaginary parts of the function f, defined along the $j\omega$ axis. It is the relationship between u and v, among others, that are of interest here.

Bode and others (see reference 4 for an extensive list) have derived the relationships between the real and imaginary parts of $f(j\omega)$. Equations (3) to (5) are those to be evaluated below, although other versions of the relationships exist.

$$v_x=\frac{2.\omega_x}{\pi}\int_0^{\infty}\frac{u-u_x}{\omega^2-\omega_x^2}.d\omega \qquad (3)$$

$$u_x-u=\frac{-2.\omega_x^2}{\pi}\int_0^{\infty}\frac{v/\omega-v_x.\omega_x}{\omega^2-\omega_x^2}.d\omega \qquad (4)$$

$$u_x-u_\infty=\frac{-2}{\pi}\int_0^{\infty}\frac{v.\omega-v_x.\omega_x}{\omega^2-\omega_x^2}.d\omega \qquad (5)$$

where u_x and v_x are shorthand methods of writing $u(\omega_x)$ and $v(\omega_x)$, and so on.

An alternative expression for $f(j\omega)$, given in terms of amplitude and phase rather than real and imaginary parts is,

$$f(j\omega)=A(\omega).e^{j\psi(\omega)} \qquad (6)$$

where A is the amplitude (magnitude) response and ψ the phase response of the function f, defined along the $j\omega$ axis.

By taking logarithms of both sides of equation (6), it becomes

$$\ln f(j\omega)=\ln A(\omega)+j\psi(\omega) \qquad (7)$$

and expressions which relate the real and imaginary parts in this equation are similar to equations (3), (4) and (5) given above: i.e.

$$\psi_x=\frac{2.\omega_x}{\pi}\int_0^{\infty}\frac{\ln A-\ln A_x}{\omega^2-\omega_x^2}.d\omega \qquad (8)$$

$$\ln A_x-\ln A_0=\frac{-2\omega_x^2}{\pi}\int_0^{\infty}\frac{\psi/\omega-\psi_x/\omega_x}{\omega^2-\omega_x^2}.d\omega \qquad (9)$$

$$\ln A_x-\ln A_\infty=\frac{-2}{\pi}\int_0^{\infty}\frac{\psi.\omega-\psi_x\omega_x}{\omega^2-\omega_x^2}.d\omega \qquad (10)$$

For the two sets of equations above, i.e (3) to (5) and (8) to (10), the same numeric solutions can be used, provided that the correct units are chosen. In particular, the amplitude should be expressed in nepers and the frequency in radians/sec in the equations. (The neper was a unit used frequently by Bode and his contemporaries. It is applied to a result when the natural logarithm of a voltage or current ratio is taken. It is easily changed to the more familiar decibel by means of the conversion 1 neper = 8.686 dB).

PHASE RESPONSE FROM AMPLITUDE RESPONSE

Equation (8) is relevant here but, before proceeding, some general comments can be made about the behaviour of the magnitude of the expression given in (1).

If $|f(j\omega)|$ is plotted against log (ω) then the resulting curve can be considered to have

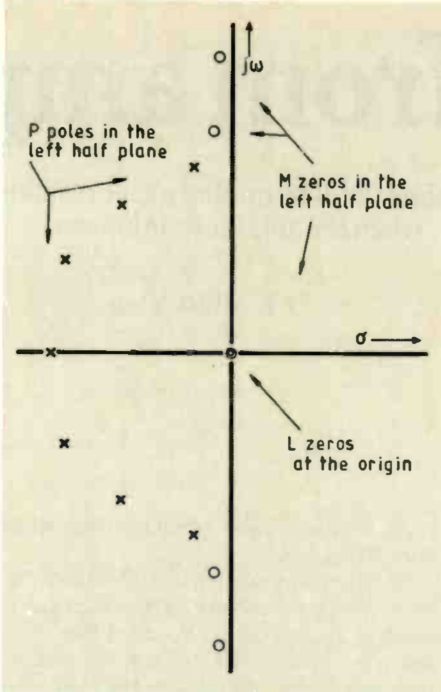


Fig.3. General diagram of input characteristic of a network, F(s), showing typical grouping of poles and zeros in the s-plane.

three regions. Firstly, there is a high-frequency region where the response falls linearly at 6(P-Z) dB per octave, where (P-Z) is the difference between the total number of poles and zeros in f(s). Secondly, there is a low-frequency region where the response falls linearly at 6L dB per octave as ω approaches zero, where L is the number of zeros at the origin. Thirdly, there is the important mid-frequency region, where the particular characteristics of the response are dependent to the specific pattern of all the poles and zeros of the function. (The precise arrangement is actually unknown, of course, only the resultant amplitude response is known).

The solution of equation (8) can now be broken down into three parts, one for each of the regions just mentioned.

High-frequency contribution. If a frequency ω_h is chosen in the high-frequency attenuation region of the response, then the integral I_h, for the frequency range ω_h to ∞, can be written

$$I_h=\frac{2.\omega_x}{\pi}\int_{\omega_h}^{\infty}\frac{\ln A-\ln A_x}{\omega^2-\omega_x^2}.d\omega \qquad (11)$$

Now, at high frequencies,

$$A(\omega)\Big|_{hf}\approx\frac{K.}{\omega^{P-Z}} \qquad (12)$$

where P is the total number of poles and Z is the total number of zeros.

therefore

$$I_h\approx\frac{2.\omega_x}{\pi}\int_{\omega_h}^{\infty}\frac{\ln(K/\omega^{P-Z})-\ln A_x}{\omega^2}.d\omega$$

provided that $\omega_h \gg \omega_x$ (i.e. for the expression to be accurate, it is necessary to have the value of ω_h at least an order of magnitude greater than ω_x).

Expanding the right hand side,

$$I_h=\frac{2.\omega_x}{\pi}\int_{\omega_h}^{\infty}\frac{\ln K-(P-Z)\ln\omega-\ln A_x}{\omega^2}.d\omega$$

so finally

$$I_h=\frac{2.\omega_x}{\pi.\omega_h}\Big\{\ln K-\ln A_x-(P-Z)(1+\ln\omega_h)\Big\} \qquad (13)$$

Before equation (13) can be evaluated it is necessary to obtain values for ln K and (P-Z). To do this, two frequencies ω_{h1} and ω_{h2} are chosen in the high frequency region of the response, with $\omega_{h2}>\omega_{h1}$ and with attenuation values A_{h1} and A_{h2}, respectively.

Since, at high frequencies, from equation (12)

$$\ln A=\ln K-(P\text{-}Z).\ln\omega,$$

then

$$\ln A_{h1}=\ln K-(P\text{-}Z).\ln\omega_{h1} \qquad (14)$$

and

$$\ln A_{h2}=\ln K-(P\text{-}Z).\ln\omega_{h2} \qquad (15)$$

Solving equations (14) and (15) gives

$$(P-Z)=\frac{\ln A_{h1}-\ln A_{h2}}{\ln\omega_{h2}-\ln\omega_{h1}} \qquad (16)$$

and

$$\ln K=\frac{\ln A_{h1}.\ln\omega_{h2}-\ln A_{h2}.\ln\omega_{h1}}{\ln\omega_{h2}-\ln\omega_{h1}} \qquad (17)$$

Equations (16), (17) and (13) are sufficient to allow the evaluation of I_h for the frequency ω_x. However, the computational work can be simplified if, first of all, equation (13) is written as

$$I_h=C_h.\omega_x.(D_h-\ln A_x) \qquad (18)$$

where

$$C_h=2/\pi.\omega_{h2}$$

and

$$D_h=\ln K-(P-Z).(1+\ln\omega_{h2})$$

and where ω_h is replaced by ω_{h2}, a frequency already chosen.

Following the determination of (P-Z), K, C_h and D_h during preliminary calculations, it is only necessary to work with equation (18) thereafter when evaluating the value of I_h at each frequency ω_x.

Low-frequency contribution. For the frequency range 0 to ω_l, where ω_l is a frequency in the low-frequency region of the response, the integral expression is

$$I_l=\frac{2.\omega_x}{\pi}\int_0^{\omega_l}\frac{\ln A-\ln A_x}{\omega^2-\omega_x^2}.d\omega \qquad (19)$$

Now, from equation (1) the expression for $f(j\omega)$ as $\omega\longrightarrow 0$ becomes

$$f(j\omega)\Big|_{lf}\approx K.\frac{\prod_{i=1}^{m}a_i}{\prod_{i=1}^{P}b_i}.\omega^L$$

so the logarithm of the magnitude can be written

$$\ln A(\omega)=\ln K_l + L.\ln \omega$$

where

$$\ln K_l=\ln K+\sum_{i=1}^{m} \ln a_i-\sum_{i=1}^{n} \ln b_i \qquad (20)$$

and so, provided that $\omega_x \gg \omega_l$

$$I_h \approx \frac{2.\omega_x}{\pi} \int_0^{\omega_l} \frac{\ln K_l+L.\ln \omega - \ln A_x}{-\omega_x^2}.d\omega$$

and finally

$$I_h=\frac{-2.\omega_l}{\pi.\omega_x}\left\{\ln K_l-\ln A_x+L(\ln \omega_l-1)\right\} \qquad (21)$$

To determine the values of K_l and L, which are required for the evaluation of equation (21), consider two frequencies ω_{l1} and ω_{l2} in the low frequency region of the response, with $\omega_{l2}>\omega_{l1}$.

Then

$$\ln A_{l1}=\ln K_l + L.\ln\omega_{l1} \qquad (22)$$

and

$$\ln A_{l2}=\ln K_l + L.\ln\omega_{l2} \qquad (23)$$ gives

Solving equations (22) and (23)

$$L=\frac{\ln A_{l2}-\ln A_{l1}}{\ln \omega_{l2}-\ln \omega_{l1}} \qquad (24)$$

$$\ln K_l=\frac{\ln A_{l1}.\ln \omega_{l2}-\ln A_{l2}.\ln\omega_{l1}}{\ln \omega_{l2}-\ln \omega_{l1}} \qquad (25)$$

Thus, the value of I_l, for a frequency ω_x, can be evaluated by means of equations (21), (24) and (25).

For convenience of computation, equation (21) can be rewritten

$$I_l=-\frac{C_l}{\omega_x}\left\{D_l-\ln A_x\right\} \qquad (26)$$

where

$$C_l=\frac{2.\omega_{l1}}{\pi} \text{ and } D_l=\ln K_l+L.\omega_{l1}(\ln\omega_{l1}-1)$$

and where it is convenient to put $\omega_l=\omega_{l1}$, since this is a frequency already chosen. Values of C_l and D_l are obtained as part of the preliminary calculations, so that only (26) needs to be used in subsequent calculations.

Mid-frequency contribution. The expression that requires evaluation is

$$I_m=\frac{2.\omega_x}{\pi} \int_{\omega_l}^{\omega_h} \frac{\ln A-\ln A_x}{\omega^2-\omega_x^2}.d\omega \qquad (27)$$

It is necessary to resort to numerical integration to evaluate this expression, since it is not normally possible to find an analytic solution. However, it is an integral between finite limits and, provided proper care is taken when $\omega=\omega_x$, a straightforward procedure is possible.

Amplitude values are known at a number of frequencies. These are the points (nodes) chosen originally adequately to define the response. In the first instance, it is convenient to calculate the values of phase at these same frequencies. (The value of phase at any other frequency can be derived, as required, but it is first necessary each time to determine the amplitude value at the chosen frequency. This can be done by interpolation between the appropriate pair of nodes on the amplitude plot.)

It is possible to carry out the numerical integration by means of the trapezium rule, as this is easily implemented; it copes well with the non-linear frequency scale and it gives adequate accuracy. If, first of all, the frequency interval between two adjacent nodes is subdivided into a number of logarithmically equal intervals (eight or more subdivisions give good results), then corresponding amplitude values may be obtained by interpolation. For example, if point 1 has a gain value A_1 at frequency ω_1 and point 2 has values A_2 and ω_2, and if the frequency interval is divided into n logarithmically equal subsections, then the intermediate frequencies are calculated using

$$\omega_m=\omega_1.e^{(\ln\omega_2-\ln\omega_1)\frac{m}{n}} \qquad (28)$$

for $o \leq m \leq n$

and the corresponding amplitude values are

$$\ln Am=\ln A_1+(\ln A_2-\ln A_1)\frac{m}{n} \qquad (29)$$

for $o \leq m \leq n$

If the phase value is currently being calculated at frequency ω_x (with amplitude value A_x) then the value of Bode's function at each point is

$$BD_m=\frac{\ln A_m-\ln A_x}{\omega_m^2-\omega_x^2} \qquad (30)$$

for $o \leq m \leq n$

The area of each sub-interval, using the trapezium rule, is

$$\text{Area}\Big|_m^{m+1}=\frac{(BD_{m+1}+BD_m)(\omega_{m+1}-\omega_m)}{2} \qquad (31)$$

and the total area between two adjacent nodes is the summation of the sub-areas as m is stepped through from zero to n-1.

This process is repeated for all the segments in the mid-frequency range.

However, whenever $\omega_m=\omega_x$ equation (30) cannot be used directly, so it is necessary to find separately a value for BD whenever this occurs. It can be found as the limiting value of the right hand side of (30) as $\omega \rightarrow \omega_x$ and is given by

$$BDx=\lim_{\omega\rightarrow\omega_x} \frac{\ln A-\ln A_x}{\omega^2-\omega_x^2} \approx \frac{1}{2\omega_x}\frac{d}{d\omega}(\ln A). \qquad (32)$$

There is an additional complication because the function being considered for integration is not a smooth curve, but consists of a series of straight line segments (i.e. the function is not analytic at the nodes). So each time $\omega \rightarrow \omega_x$, it is necessary to find two limiting values of BD, one as $\omega \rightarrow \omega_x$ from the low-frequency side and one as $\omega \rightarrow \omega_x$ from the high frequency side.

Therefore, two values of the gradient of the amplitude response are required, each time $\omega \rightarrow \omega_x$, for the evaluation of equation (32). To obtain them, choose two frequencies very close to ω_x, one on the low-frequency side at, say, ω_{xl} and one on the high-frequency side at, say, ω_{xh}. Values of the amplitude, A_{xl} and A_{xh} respectively, can be obtained at these frequencies by interpolation in much the same manner as discussed previously, using an expression similar to equation (29). Then on the low-frequency side

$$\frac{d}{d\omega}(\ln A)\Big|_{\omega_x^-} \leq \frac{\ln A_{xh}-\ln A_{xl}}{\omega_x-\omega_{xl}}.$$

and similarly on the high-frequency side

$$\frac{d}{d\omega}(\ln A)\Big|_{\omega_x^+} \leq \frac{\ln A_{xh}-\ln A_x}{\omega_{xh}-\omega_x}.$$

With these results, the two outstanding values of BD can be calculated, using equation (32), and the calculation of areas can be completed through the range ω_{l1} to ω_{h2}.

Then

$$I_m=-\frac{2.\omega_x}{\pi}\sum_{\omega_{l1}}^{\omega_{h2}} \text{areas}$$

Summation of contributions. The final answer, at a given ω_x, is the sum of the three contributions calculated as described above, i.e.

$$\psi_x=I_l+I_m+I_h$$

This answer is in radians and can, of course, be easily converted to degrees if required.

The calculations are repeated for other values of ω_x, as required. The frequencies chosen for the initial calculations are normally the other nodes of the response, as mentioned above, with additional frequencies chosen later, if they are needed.

Examples. Three examples are given below to illustrate the results achievable by the procedure. In these cases it is possible to obtain the answers by analytic means, to allow the accuracy of the method to be checked.

In the examples, the interval between adjacent nodes is subdivided into ten parts, as this is considered to be a good compromise between accuracy and computing time (taking, say, 16 subdivisions certainly increases the accuracy of the results a little, but the program takes 50% longer to run). In any case, the final accuracy is much more dependent on how well the initial data points are chosen, when first characterizing the response.

Results so far obtained agree well with the predictions given by Thomas, i.e. if the straight line segments are chosen to approximate the true response with errors that do not exceed 0.5dB, then the resultant phase plot will not deviate by more than 3 degrees from the correct value.

Although the work in this article concentrated on obtaining phase from amplitude, the same procedure is applicable to the derivation of the imaginary part of a network function from the real part and this is demonstrated in the third example.

Example 1. The amplitude plot is shown at (a) in Fig.4. It is a low-pass filter characteristic and is a third-order Chebyshev with 3dB ripple. The phase response of this filter obtained by analytic means is shown by the full line at (b).

The triangles shown on the amplitude curve are the points chosen to define the

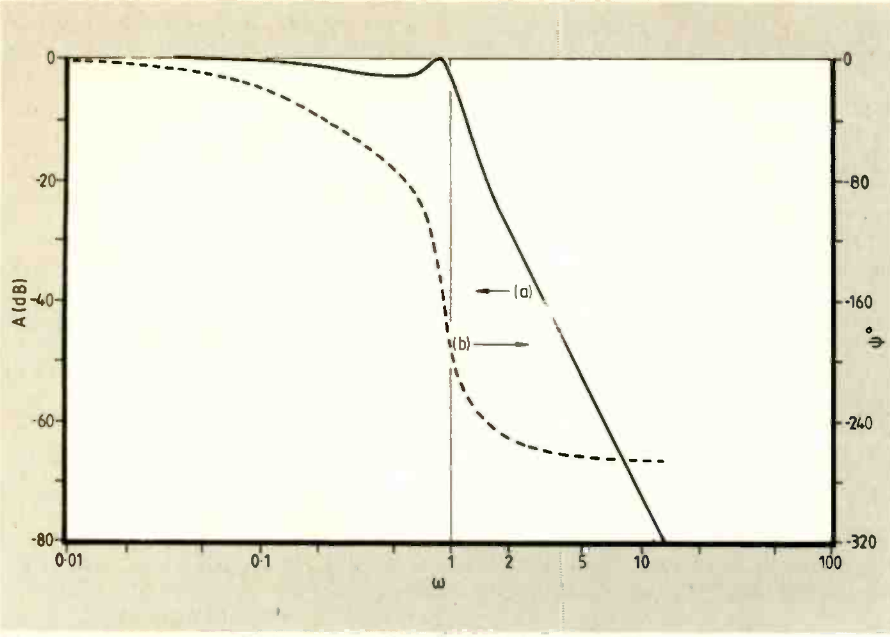


Fig.4. Phase response (b) from amplitude (a) of a low-pass filter.

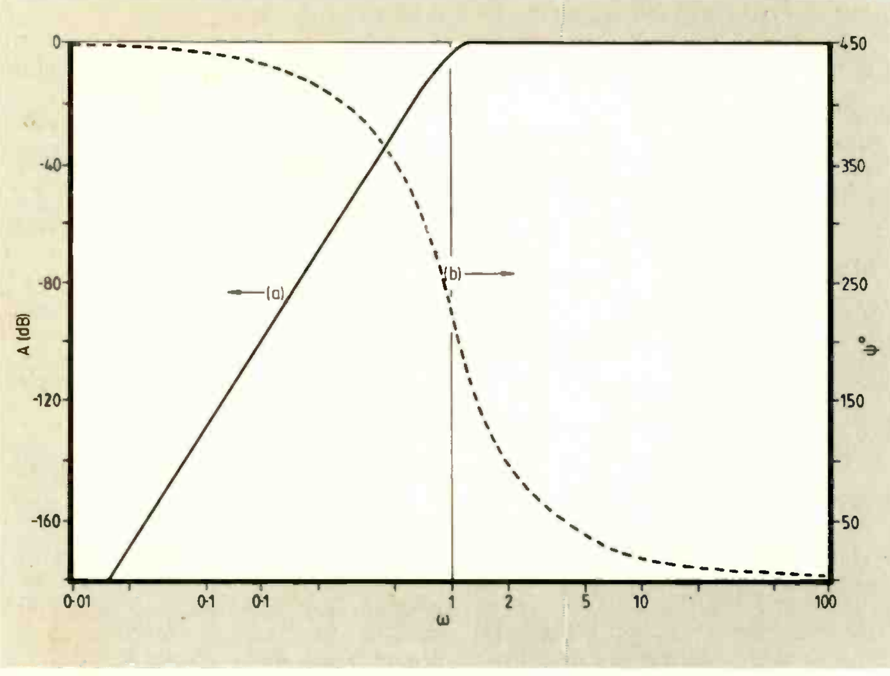


Fig.5. High-pass filter phase response (b) calculated from amplitude response (a).

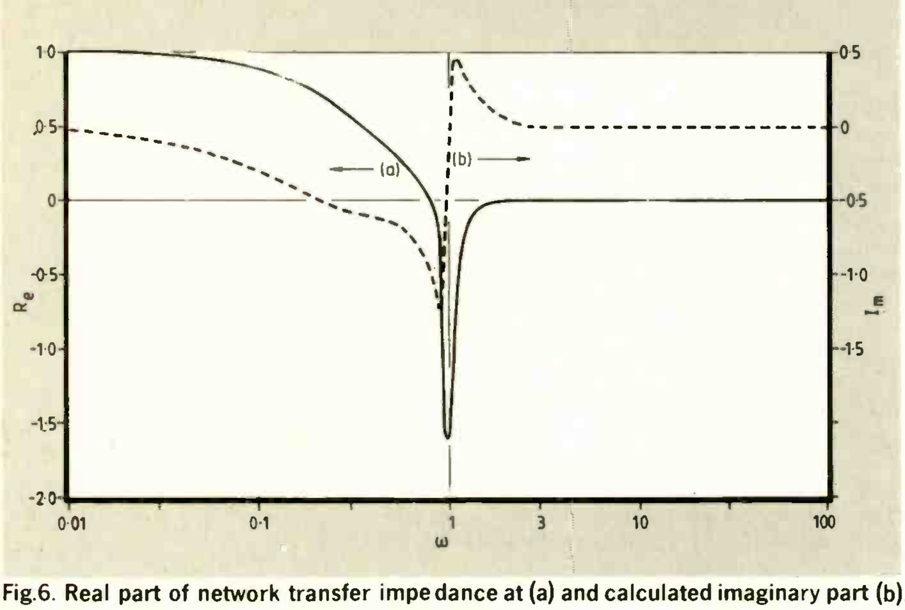


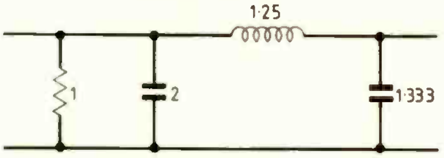
Fig.6. Real part of network transfer impedance at (a) and calculated imaginary part (b).

amplitude response. In the first instance, the numeric procedure obtained the phase at the same frequencies as the input data and the results are shown as circles on Fig.4(b). Additional points, shown as squares, were obtained by interpolation of the same input data.

Example 2. In this example the amplitude response, that of a 5th order Butterworth high-pass filter, is shown at (a) in Fig.5 and the phase response, obtained by analytic means, is shown at (b).

As in example 1, triangles on (a) indicate the points chosen to characterise the amplitude response and the circles and squares on (b) are the results of the numeric procedure.

Example 3. Here a network real part is the input data and is shown at (a) in Fig.6. This is the real part of the transfer impedance of the network shown in Fig.7. The imaginary part, obtained by analytic means, is shown at (b).



As in the previous examples, triangles define the input data and circles or squares show the calculated results.

BOOKS

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Newnes radio amateur and listener's pocket book by Steve Money. Heinemann Professional Publishing, £8.95. Compendium of reference data for the radio operator. Subject headings include antennas, transmitters and receivers, radio frequencies, digital communication, picture communication, utility stations, space communication, propagation, operating data. Hard covers, 160 pages 95×195mm. (Despite the similar outward appearance of volumes in this series, it is notable that there is relatively little overlap in the contents.)

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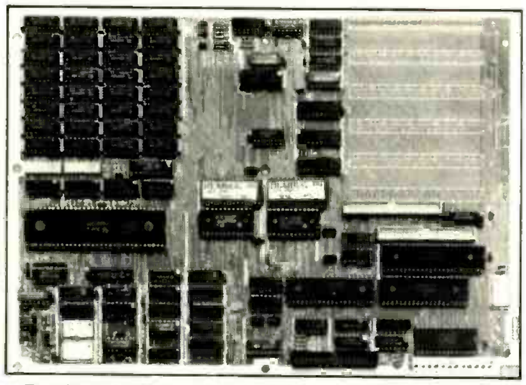

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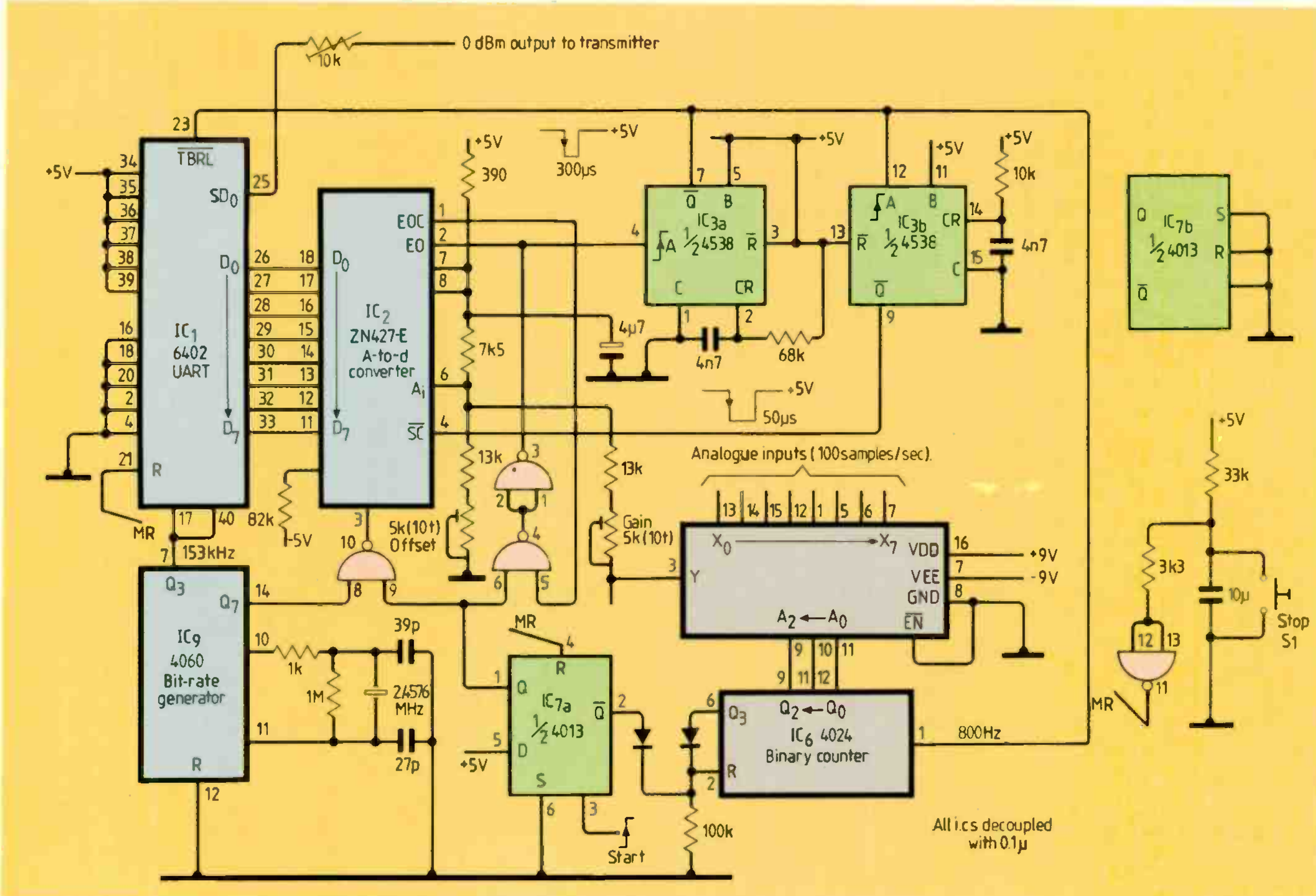


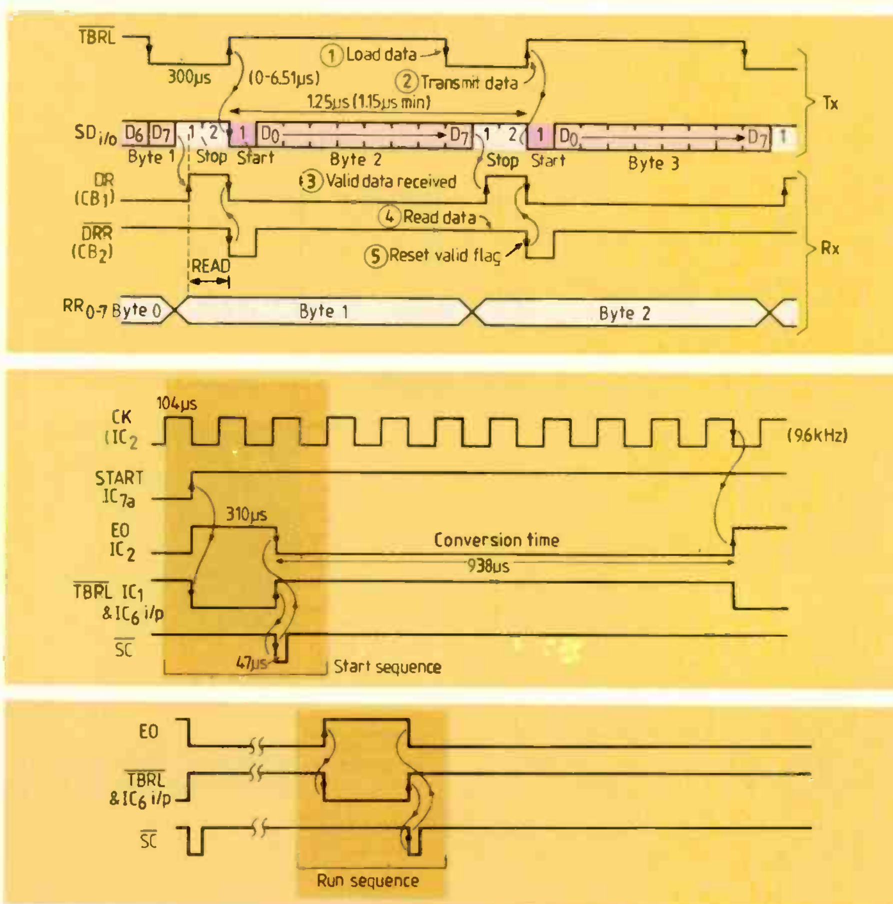
Digitally-multiplexed telemetry link

These circuits were developed to provide remote monitoring of physical and physiological quantities in ambulant patients. Eight analogue channels are provided at the transmitter and a parallel interface at the receiver allows direct connection to the user port of a BBC microcomputer. A modified radio-microphone system operating at around 147MHz provided an r.f. data link.

Multiplexer IC_5, sampling at 100Hz, feeds each of the eight ±5V analogue channels sequentially to a-to-d converter IC_2. When conversion is complete, monostable multivibrator IC_{3a} triggers loading of the data into the 6402 uart and increments the multiplexer address counter. Serial output is attenuated to about 0dBm before being fed into the transmitter. When IC_{3a} times out, IC_{3b} is triggered to start conversion of the next sample.

A pulse on the clock input of bistable device IC_{7a} starts the system. Converter and uart clocking signals, at 9600Hz and 153kHz respectively, are produced by IC_9 and a 2.45MHz crystal. These frequencies give a 950µs conversion time and 9600 baud data.

Since a-to-d converter input is not sampled and held, the unit is only suitable for signals with a low slew rate. For one l.s.b. error, the slew rate should be <40V/s.



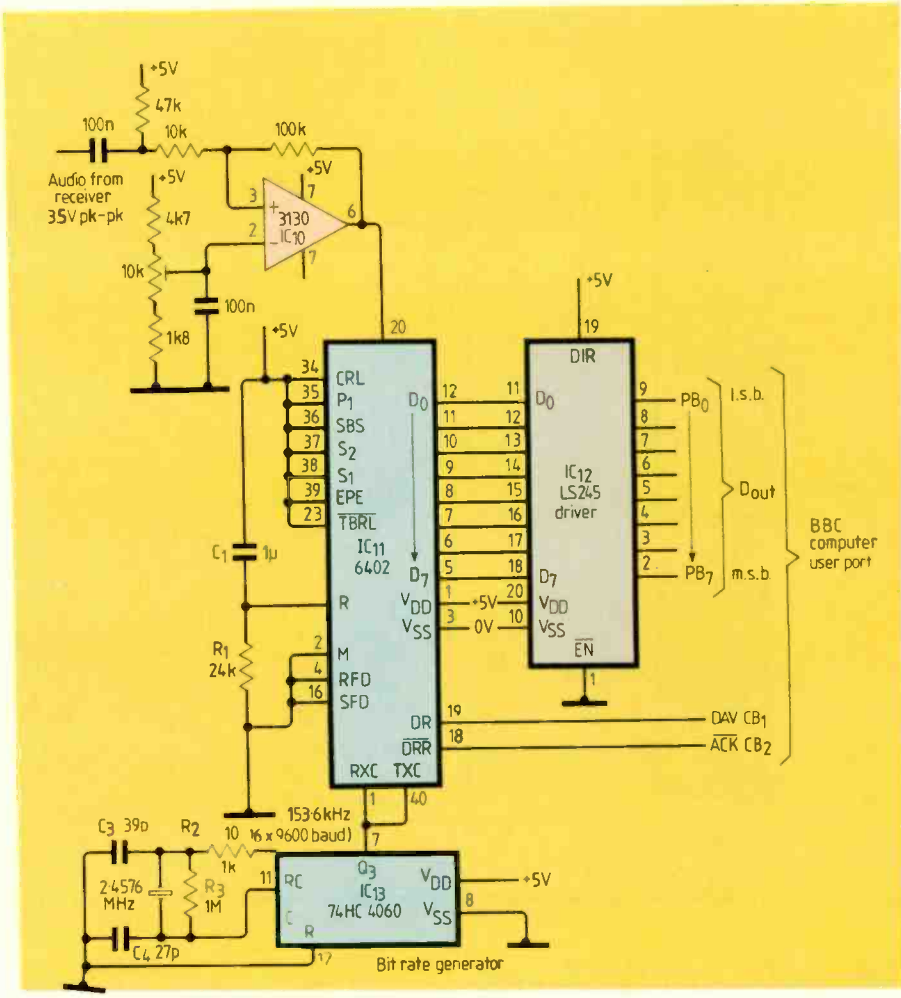
CIRCUIT IDEAS

At the receiver, recovered audio at about 3.5V pk-pk feeds a comparator whose reference is set using a potentiometer to give error-free data. Data is converted from serial to parallel form by a second uart then buffered by IC_{12} for feeding to the computer. Simple handshaking for the microcomputer interface is provided by uart lines $\overline{DR}$ and $\overline{DRR}$. A machine-code routine is needed to read the data from the uart. An example of assembly language that might be used is,

```
.READY LDA #&F0    ) Pulse CB2 low
       STA &FE6C   | (DRR) to reset
       LDA #&D0    | flag from
       STA &FE6C   ) uart CB1 (DR)

.TEST  LDA &FE6D   ) Test CB1
       AND #&10    | if high ' read
       BEQ TEST    | data else
       LDA &FE60   ) test CB1
                     etc.
```

Handshaking line CB_1 goes high on receipt of the first valid character. This provides transmitter/receiver synchronization since channel one is the first transmitted after a start pulse. It is advisable to use ferrite beads on the power supply lines; the transmitter needs ±5V supplies and the receiver 5V.
A.G. Birkett
London



Don't waste ideas

We prefer circuit ideas contributions with neat drawings and widely-spaced typescripts but we would rather have 'scribbles on the back of an envelope' than let good ideas be wasted.

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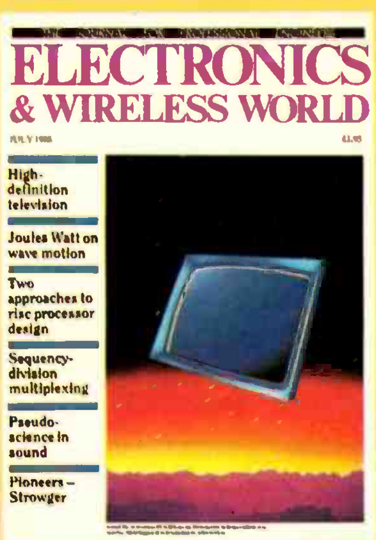
NEXT MONTH

High-definition television. There is currently a great deal of activity directed towards the establishment of one or more standards for enhanced television systems with higher definition. We present an article explaining the factors which will influence the choice.

Waves. Joules Watt has come to the conclusion that many youngsters reading electronics at university possess only a nodding acquaintance with the subject of wave motion. This month's JW piece should help with the introductions.

Pioneers – Strowger. One of the great names in communications, Almon B. Strowger is the subject of this part of W.A. Atherton's historical series.



Pseudo-science in audio. As a professional audio engineer, Doug. Self has lost patience with the "subjectivist tendency" in audio. He attempts to remove some of the mythology that has permeated the subject in the last few years.

Sequency-division multiplexing. The use of Walsh functions offers an alternative to frequency-division or time-division multiplex, with a reduced sensitivity to noise. C.H. Langton explains.

Risc processors. Approaches to the architecture and design of risc processors are described by authors from two of the companies engaged in this development.

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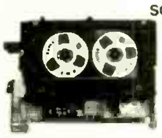

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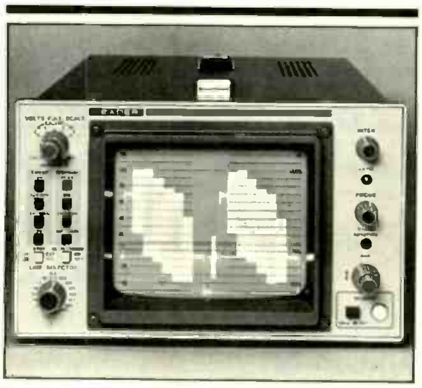

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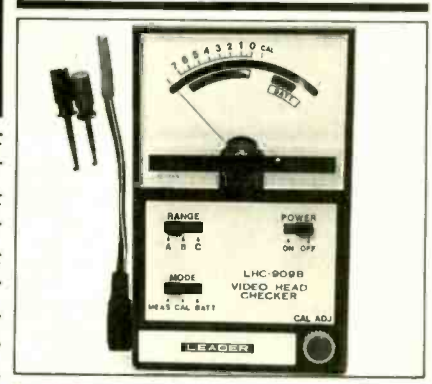

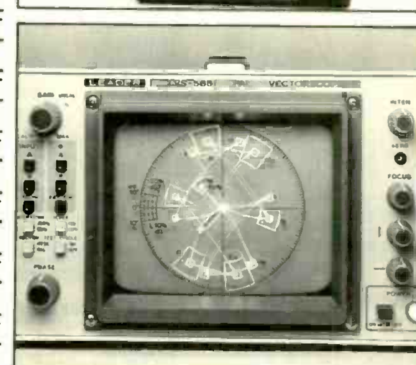

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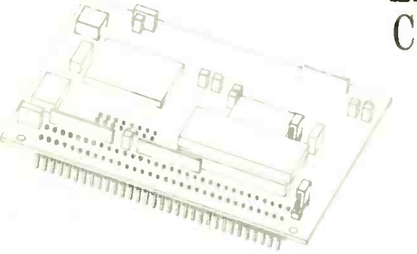

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A new technique in o.t.d.r.

A new correlation technique for fibre o.t.d.r. measurements, described last month, gives readings 64 times faster than conventional single-pulse methods. This second article discusses practical advantages.

STEVE NEWTON

Performance advantage of a complementary-correlation o.t.d.r. over a conventional single-pulse o.t.d.r. using the same laser, receiver, and other components can be summarized as follows. When coded probe signals consisting of L bits are used to probe a fibre, a two-way dynamic range increase of $\sqrt{L/4}$ is achieved relative to a conventional single-pulse measurement in a given averaging time, while maintaining the response resolution corresponding to the width of a single bit. Alternatively, the same result obtained with a single-pulse measurement can be obtained a factor of L/4 times faster using complementary codes. The way in which this improvement is obtained in theory was described last month. This article describes how these performance improvements were demonstrated in practice.

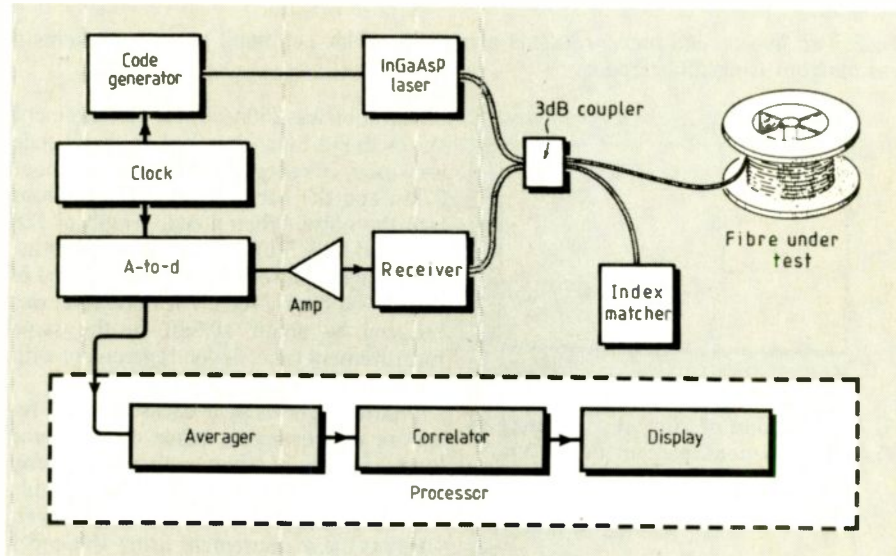


Fig.1. Block diagram of the complementary-correlation o.t.d.r. experiments.

EXPERIMENT

A block diagram of the experimental arrangement used to make the complementary-correlation o.t.d.r. measurements is shown in Fig. 1. A code generator was used to drive a commercially available inGaAsP laser diode ($\lambda = 1.3\mu m$) with the appropriate Golay-codes and their one's complements. The shot-to-shot repetition rate of the code bursts was approximately 700Hz. A peak power of 6mW was coupled from the laser into its single-mode fibre pigtail. The laser power was coupled into the fibre under test using a fibre directional coupler whose second output was index matched to suppress reflection. Peak power coupled into the fibre under test was approximately 2mW.

Approximately half of the return signal from the fibre under test was coupled to the receiver via the directional coupler. The receiver consisted of a pigtailed InGaAs p-i-n photodiode followed by a transimpedance amplifier. Bandwidth of the receiver was approximately 3.5MHz, and its noise equivalent power was 400pW (–64dBm).

The amplified signal was then digitally sampled, averaged, and processed to reconstruct the fibre backscattering impulse response. In the first experiments, the averaging, correlation, and display were performed using a desk-top computer (HP9836). For later experiments, including many of those described in this article, the functions of the clock, code generation, averaging, and correlation were performed by a single piece of digital circuitry, essentially a specialized 32bit 10 Mips signal processor. This high-speed processing capability allowed the reconstructed data to be displayed on a c.r.t. with updates of the averaged data approximately every 250ms.

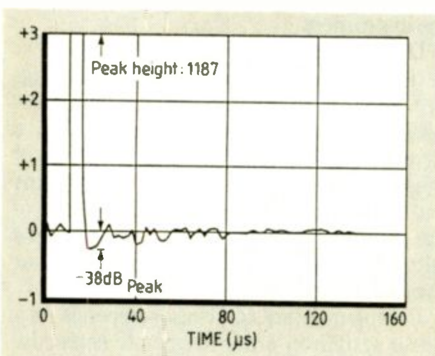


Fig.2. Measured reconstruction of a large reflection. Most side lobes are more than 40dB down from the peak.

EXPERIMENTAL RESULTS

A variety of fibre configurations were used to test the performance of the complementary-correlation o.t.d.r. The fibres used in these experiments had attenuation coefficients ranging between 0.34 and 0.4dB/km. Elastomeric splices were used to make most of the connections, although measurements made on side-lobe deviation using connectors yielded similar results. The results presented here represent the main performance advantages of this complementary-correlation technique: strong side-lobe suppression, signal-to-noise improvement without compromising resolution, improved dynamic range, and greatly reduced measurement time.

Figure 2 shows a measurement of an extremely large reflection made using 32bit codes consisting of 4μs bits. This result, plotted on a linear scale, shows autocorrelation side lobes which occupy a fraction of one division to the right of the peak. However, since the height of the peak is 1187 of these divisions, the worst side-lobe deviation (which could also be interpreted as receiver undershoot) is 38dB down, with the rest of the structure more than 40dB below the peak. It should be noted that this is a typical and not a best result; in some cases, side lobe suppression approaching 45dB has been observed. This is the best side-lobe suppression reported to date for a correlation o.t.d.r. and is 20-30dB better than what is possible using Barker or finite pseudo-random codes, even under ideal conditions.

Figure 3 shows two measurements of a 5km span of fibre centred at 25km after five seconds of averaging time. In both cases, the bit duration was 125ns. In Fig.3(a), a 4bit code was used to represent the result that would be obtained using a conventional o.t.d.r. Figure 3(b) shows the result of using 256bit codes in the same five-second measurement time. In this case, the noise is greatly reduced and the backscattered signal is visible. This result is obtained without sacrificing resolution, as evidenced by the fact that in both cases the 3dB width of the reflection peak is only 16m.

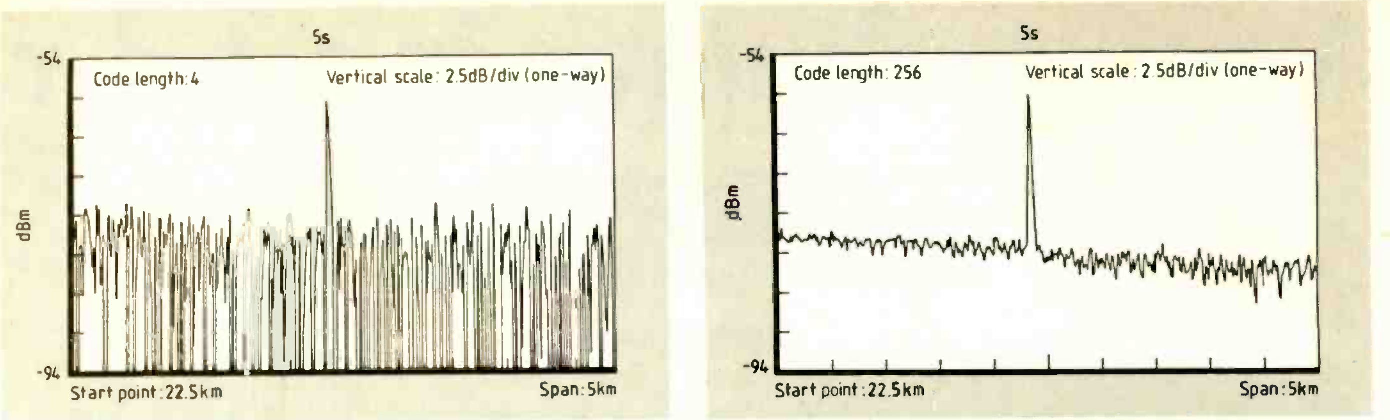


Fig.3. Two five-second measurements using 125ns bits. Left-hand curve represents a conventional measurement, right-hand curve results from using 256bit codes.

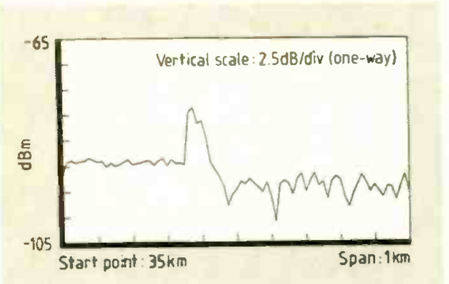


Fig.4. Resolution of 26m at a distance of 35.4km with a measurement time of 20s.

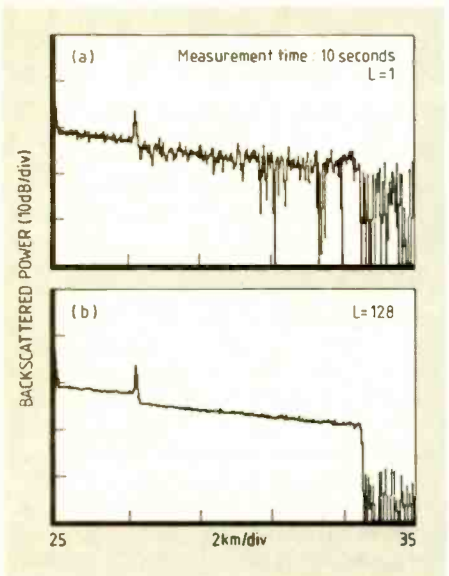


Fig.5. Two ten-second measurements using 250ns bits. Graph (a) is a single-bit measurement and (b) is a measurement using code length 128.

An example of high resolution at long range is shown in Fig.4. The reflection feature is located at a distance of 35.4km. It contains not one, but two peaks that are separated by only 26m and clearly resolved. These peaks are the result of reflections from both ends of a 26m segment of fibre which is spliced into the cable at that distant point. Whereas a conventional o.t.d.r. might take well over 20 minutes to obtain such a result, this measurement, which used 256bit codes, took only 20 seconds.

Figure 5 shows two measurements of a 10km span of fibre centred at 80km after ten seconds of averaging time. In both cases, the bit duration was 250ns. In the measurement shown in Fig. 5(a), wherein a single-bit code was used, a reflection is visible at about 27km and the backscattering signal drops into the noise. When a code length of 128 was used, Fig. 5(b), however, the backscattering signal is free of noise and the end of the fibre is clearly seen. The noise level was reduced by about 10.5dB in the same measurement time, in good agreement with theory (seven octaves × 1.6dB/octave).

Figure 6 shows two backscattering response measurements made on the same 20km segment of a fibre recirculating delay line[12]. Both measurements exhibit roughly the same signal-to-noise ratio. However, whereas the measurement using 1bit codes required 256 seconds of averaging to obtain this result, the same result was obtained using 32bit codes in only eight seconds, or 32 times faster.

Finally, Fig. 7 shows three measurements of a 20km span of fibre between 20 and 40km from the input. In each case, 500ns bits were used. The measurements shown in Figs 7(a,b,) were made using 4bit codes to represent the performance of a conventional single-pulse o.t.d.r. After 15 seconds of averaging, Fig. 7(a), a single reflection is visible at 25km, and the backscattering signal descends into the noise. After 16 minutes of averaging, Fig. 7(b), the backscattering signal is largely free of noise, a second reflection is visible at 313km, and the end of the fibre at 35.5km is clearly seen. However, by using codes of length 256, Fig.7(c), the same result was obtained after averaging over only 15 seconds. Relative to the 15 second measurement made with 4bit codes, Fig. 7(a), the two-way dynamic range is improved by 9dB.

These experiments verify each of the major performance advantages predicted by the theory of the complementary correlation o.t.d.r. They demonstrate low autocorrelation side lobes, improved dynamic range in a fixed measurement time, and dramatically reduced measurement time at a given range. Furthermore, these improvements are accomplished without any sacrifice in response resolution.

THE HP 8145 OTDR

The Hewlett-Packard 8145, shown on p.560, is the first commercially available o.t.d.r. to realize the full advantage of a spread-

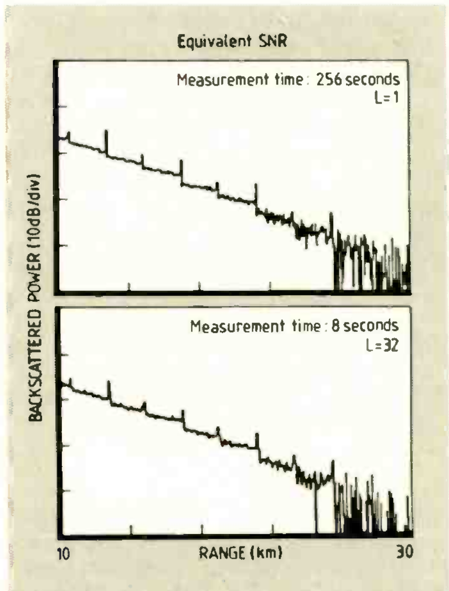


Fig.6. Two measurements with equivalent signal-to-noise ratio, both using 500ns bits. The 32bit measurement was made 32 times faster.

spectrum technique. It employs every aspect of the new technique, but in a more sophisticated way. As a result, it is able to equal (and occasionally exceed) the results of the laboratory experiments described earlier and reported in the scientific literature.[13] In fact, some of those results were obtained using systems that were basically laboratory prototypes of the finished product, operated under controlled test conditions and without any of the automatic or user features of the instrument.

Developing a state-of-the-art experimental measurement system into a rugged, portable instrument without compromising performance is neither an easy nor a frequently accomplished task. In the case of the HP 8145, a number of practical problems had to be solved in order to make full use of the complementary correlation technique without compromising either the quality or the integrity of the measured data.

Complementary correlation depends on a linear system in order to operate correctly. Unfortunately, real measurement situations can present the o.t.d.r. receiver with an extremely wide range of optical-power levels. For example, any receiver sensitive

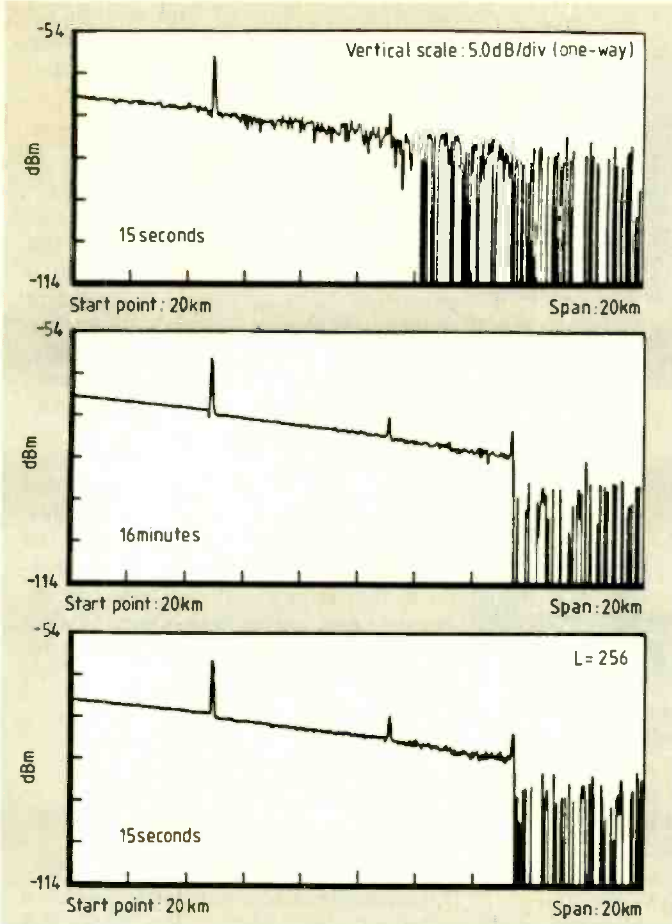
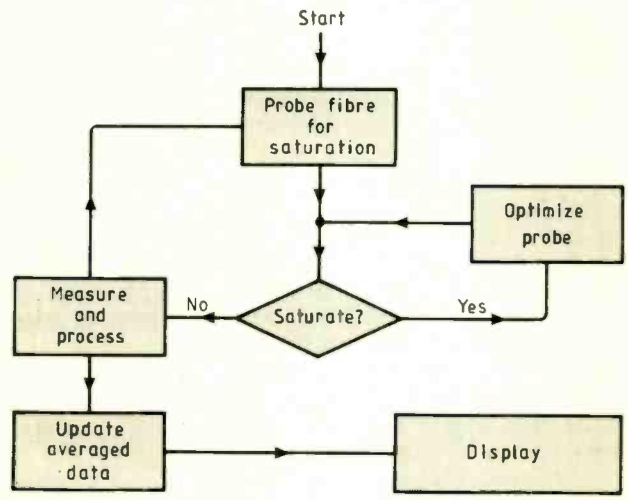


Fig.7. Three measurements using 500ns bits. The top two are conventional measurements are 15 seconds and 16 minutes of averaging respectively. The complementary-correlation measurement using 256bit codes shown in the lower curve is averaged over just 15 seconds.

Fig.8. Simplified probe-signal optimization algorithm.



enough to measure minute backscattering levels at great distances may have trouble staying within its linear range of operation when confronted with very high power levels due to strong reflections. Waker reflections may not saturate the receiver, but they may saturate some other component, such as the analogue-to-digital converter.

Non-linearities are highly undesirable in any o.t.d.r. because they lead to distortion and uncertainties in the measurement of the backscattering impulse response. In a complementary-correlation o.t.d.r non-linearities have an additional effect. When events such as a-to-d converter saturation or receiver saturation occur, the complementary nature of the Golay-code autocorrelation functions is destroyed. The result is that, unless such situations are avoided, autocorrelation side lobes may appear on the measured backscattering curve that are large enough to distort or even mask the signal surrounding a large reflection.

Although the a-to-d converter and receiver circuitry of the 8145 are designed to handle a wide range of optical signal levels, very large reflections can occasionally occur that will saturate these components. Fortunately, a number of solutions have been devised to deal with these and other measurement situations which might otherwise lead to distortion of the measured result.

The 8145 is designed to operate at maximum averaging efficiency under all measurement conditions, including when both saturating and non-saturating power levels are present. All of its analogue circuitry is linear over a wide range. When that

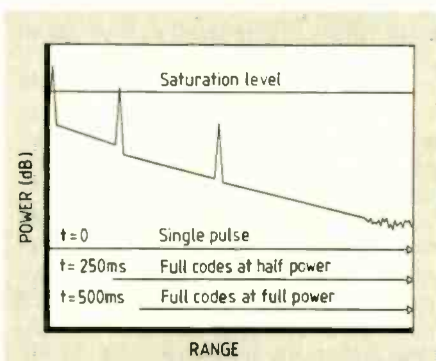


Fig.9. Piece-by-piece measurements of a fibre. First group of shots uses a single probe pulse. Second group measures beyond first reflection using full codes at half power. Once the range just past the last saturating reflection is measured, full codes and full power are used.

range is exceeded, the instrument automatically compensates to insure that all of the recorded data is valid.

Several factors contribute to the linear behaviour of the instrument.

– A fast, linear laser driver is used to provide coded probe signals that are extremely uniform over a large range of power levels and environmental conditions.

– A proprietary technique is used to extend the range and linearity of the a-to-d converter.

– The receiver is extremely linear over a wide range of input-power levels, and can saturate only when very strong reflections are present near the input of a fibre under test.

As a result of these and other proprietary features and techniques, the instrument is able to reproduce the backscattering impulse response with excellent fidelity, and to suppress autocorrelation side lobes to the –40dB level, where they do not distort the signal.

The instrument is also able to operate in this linear range when using codes because it can automatically sense and avoid saturation when data is being taken. This is accomplished using a probe signal optimization algorithm of the kind shown in Fig. 8. Before each new set of data is measured, the fibre is probed to determine the highest probe power level and the longest code length that can be used without causing saturation. This probe signal is used to measure the next set of data, thereby guaranteeing that the data will be valid.

Coupled with this automatic optimization of the probe signal is the ability of the 8145 to make piece-by-piece measurements of the fibre under test. This capability allows the complementary correlation technique along with all of its signal-to-noise advantages to be used even when the backscattering impulse response contains large saturating reflections.

Figure 9 shows how the piece-by-piece measurement capability combined with probe optimization allow the instrument to adapt to the fibre response and produce an efficient measurement. If a saturating reflection is so large that it can only be measured without distortion by using a single pulse, the instrument temporarily resorts to L=1. However, as soon as the data up to a given range has been averaged enough so that any further signal-to-noise improvement would

Table 1. Performance specifications of the 8145 optical time-domain reflectometer.

Parameter	Specification	Condition
One-way dynamic range	28dB @ 1300nm 26dB @ 1550nm	s-to-n ratio = 1 (r.m.s. noise) after 40min with 4μs pulses
Response resolution	26m	125ns pulses
Amplitude sensitivity	±0.05dB	all measurements
Measurement time	10s	s-to-n ratio = 1 (r.m.s. noise) at 22dB one-way range with 4μs pulses
Range resolution	± 3m ± 6m ± 10^{-5} × measured value	spans ≤2km all other measurements
Linearity	0.05dB/dB	all measurements

be undisplayable, no more measurements of that segment of the fibre need to be made. Once this range is beyond that of the offending reflection, the measurement is no longer limited and more energetic probe signals are automatically used. The piece-by-piece measurements are carefully combined to produce a measurement that contains no instrument-induced distortions.

In practice, this adaptive measurement process requires only a very small (and often undetectable) performance sacrifice. At close range where the saturation reflections are most likely to occur, the backscattering impulse response can be measured in real time (less than a second) using a single pulse anyway, so the performance penalty is minimal. As soon as the backscattering signal becomes weaker, however, even the largest reflections lie within the linear range of the instrument, and the instrument automatically throws the full power of the correlation technique at the part of the measurement where the s-to-n ratio advantage is needed most. The net averaging-time penalty for making part of the total measurement like a conventional o.t.d.r. is seldom more than one second. In summary, the HP8145 has adaptive measurement capabilities that result in optimized performance and effective use of the new complementary-correlation technique.

In addition to the correlation gains described previously, the resulting measurements have three further properties. All displayed data is valid and contains no correlation-induced distortions. The probe signal is always optimized to inject the maximum energy into the fibre under test. And thirdly, the 8145 actually accelerates its signal-to-noise ratio improvement due to its adaptive capability that increases the probe energy by increasing code length for longer range measurements. By contrast, the rate of signal-to-noise ratio improvement slows down in a conventional o.t.d.r. measurement, where each 1.5dB improvement requires a doubling of the measurement time.

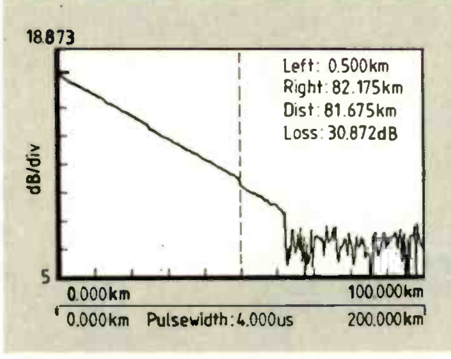


Fig.10. 30dB one-way dynamic range using an HP 8145 32bit, 4μs codes.

PERFORMANCE

The minimum performance specifications of the HP 8145 o.t.d.r. reflect the advantage of using the new complementary correlation technique, Table 1. They greatly exceed those of conventional o.t.d.rs that are presently available, and are on a par with the best results that have been reported in the literature to date.

Recently, a unique result was obtained using a complete 8145 at HP's Böblingen Instruments Division, Fig. 10. A 62km length of fibre was measured using 32bit codes with 4μs bits. One-way dynamic range of this system was measured to be slightly greater than 30dB, as measured from the initial backscattering level to the level of the r.m.s. noise. Previously, the best performance reported for a practical system[10] was observed using a coherent o.t.d.r. with 30dB one-way dynamic range after 10^6 averages, with a response resolution of 500m (using 5μs pulses) and an amplitude sensitivity of 0.2dB. The correlation result for the incoherent 8145 was obtained after only 8×10^5 averages, with a response resolution of 400m (using 4μs bits), and an amplitude sensitivity of ±0.05db.

CONCLUSION

In summary, the performance of an o.t.d.r. can be dramatically improved using a new correlation technique that employs codes having complementary auto-correlation properties. Using this technique, equivalent results were obtained 64 times faster than what is possible with a conventional single-pulse measurement using the same laser, receiver, and coupling optics. Alternatively, a 9dB two-way range improvement was obtained in the same measurement time.

This technique has been successfully employed and improved upon in a reliable, portable instrument, the 8145 o.t.d.r. The performance of this instrument is far superior to that of previously available conventional o.t.d.rs, and has been shown to exceed the best performance reported to date for any practical measurement system of its kind.

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3. J.P. King, D.F. Smith, K. Richards, P. Timson, R.E. Epworth, and S. Wright, Development of a coherent OTDR instrument, *IEEE J. Lightwave Tech.* LT-5, 616 (1987).

Steve Newton received his BS degree in physics, summa cum laude, *from the University of Massachusetts, Amherst in 1976. He received MS and Ph.D degrees in applied physics from Stanford University, Palo Alto, California, in 1978 and 1984, respectively.*

From 1978 to 1982, he was a part-time member of the technical staff at Hewlett Packard Laboratories, Palo Alto, where he was engaged in research involving optical design, metal-vapour lasers, and optical data storage. Since 1988, when he became a full-time member of the Technical Staff at HP Labs, his research activities have involved photonic measurement systems, optical-fibre components and circuits, and integrated optics. Since 1986, he has been in his present position of Project Manager of the fibre-optics group in the wave-technology department of HP's Instruments and Photonics Laboratory. He has been project manager of the o.t.d.r. effort at HP Laboratories and is a co-inventor of the technique described in this article.

Acknowledgements

The author would like to acknowledge the efforts of many of his colleagues, in particular that of co-inventor Moshe Nazarathy.

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Using programmable logic

By designing a circuit and later converting it into programmable logic as an afterthought, you lose one of the main benefits of programmable logic devices.

NEIL KELLETT

Programmable logic devices, p.l.ds, can provide designers with an efficient, compact means of producing digital circuits. However, this efficiency is impaired by poor design techniques.

Most digital design engineers are familiar with standard logic families and tend to design circuits with these devices in mind. Only when a circuit has been proven is an attempt made to convert the design into programmable logic. Not only is this an inefficient use of programmable logic, but it negates one of the major benefits of these devices – their programmability.

A more efficient way of designing programmable logic is to consider the desired system as a black box with a number of inputs and outputs (complex systems may comprise more than one of these black boxes). The system is then defined as the relationship between the inputs and outputs, either as Boolean or state equations. Once these equations have been derived it is a simple matter to produce the desired system function using one or more programmable logic devices.

This method does not preclude the possibility of direct conversion from standard logic to programmable logic where design time is of the utmost importance and a discrete circuit solution already exists. Software called Amaze, mentioned later, contains a schematic-to-Boolean conversion routine to do just this, but generally this method will lead to a non-optimal p.l.d. solution.

This article shows the design process involved in producing a programmable logic device to provide a reasonably complex system function.

SYSTEM DEFINITION

An alarm-system controller is used here to illustrate the design methology. The alarm provides three basic functions. Firstly, it should deter intruders. Secondly, should an intrusion take place the system must give an alarm. And thirdly, an alarm should be given as a result of any other alarm condition such as fire, personal attack or injury.

Deterrence is generally achieved by mounting a large box clearly marked as being part of an alarm system in a prominent position. A programmable logic device can be designed to provide the second and third functions and could form the basis of a range of alarm and security systems.

Implementing the alarm controller in user-programmable logic increases the controller's versatility. By altering slightly the program table of the programmable logic devices, it is possible to configure the system to suit any alarm transducer without altering any of the external circuitry or circuit board.

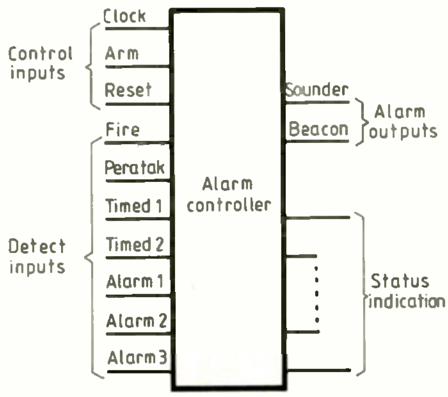


Fig.1. A basic alarm controller can be considered as a black box with several inputs and several outputs. Some inputs are used for detection and others for control.

A basic alarm controller can be considered as a black box with several inputs and several outputs, Fig.1. Some inputs are used for detection and others for control. Detect inputs are driven from a variety of alarm transducers such as reed switches, smoke detectors, pressure mats etc. An ARM input switches the system into a state which allows detection of the various alarm conditions and a RESET input is used to reset the system after an alarm has been triggered and dealt with or on re-entering the protected area. Outputs from the system include a sounder, a beacon and status indicators.

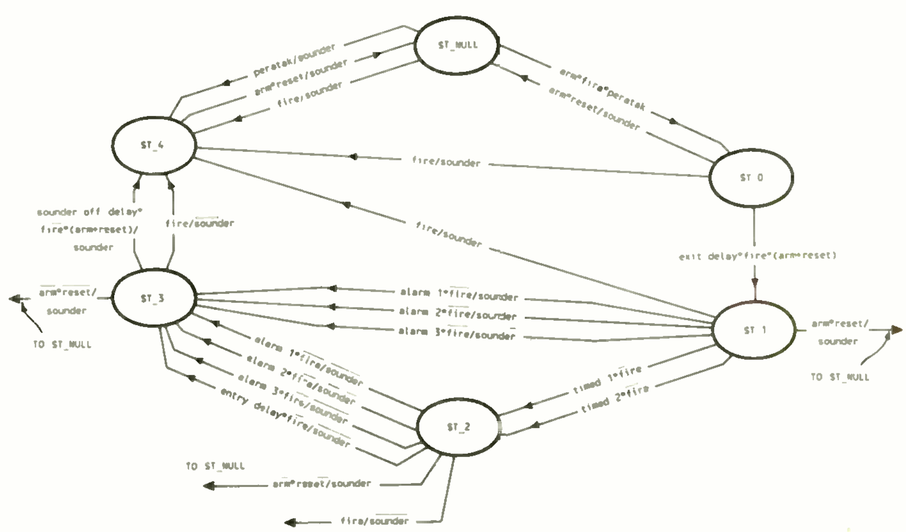


Fig.2. This state diagram for the alarm controller derived from the verbal system description shows that the controller can be in one of six possible states.

Detect inputs can be divided into timed, untimed, fire and personal attack inputs. Timed circuits allow entry/exit delay circuits for front and rear doors, say, to delay operation of the alarm for approximately 16 seconds. Untimed circuits cause the alarm to operate immediately when an alarm condition occurs. These would be used to protect non-usual means of entry, such as windows. Both the timed and untimed circuits should operate only if the system is armed.

The personal attack circuit is a special-case untimed circuit and should operate only when the system is disarmed. The fire-detect circuit is again a special case untimed circuit and should operate regardless of whether the system is armed or not.

Outputs from the controller drive an external sounder and beacon. After 128 seconds, the sounder should turn off if the alarm has been triggered by either a timed or general untimed circuit. However when a fire or personal attack triggers the system, the sounder should not turn off until the system is reset and the alarm condition removed.

STATE-MACHINE IMPLEMENTATION

A design such as this is best implemented as a state machine. The state diagram is derived from the verbal system description. As you can see from Fig.2, the controller can be in one of six possible states. Examine the transitions from ST_NULL as an example. If a personal attack or fire condition occurs while in this state, a transition to ST_4 takes place as indicated by the arrows on the diagram. Also at this time, the sounder and beacon are activated, thus giving the alarm. If the fire and personal attack conditions have not occurred and the ARM switch is set, then a transition to ST_0 takes place.

Similarly, other arrows on the state diagram represent transitions between other states when specified input conditions occur. Output parameters are shown to the right of the slash line. Where there are no output parameters specified in a transition term, this indicates that no output changes are desired during this transition. That is, an output will hold its present value until told to change.

PLD IMPLEMENTATION

Having defined the desired system operation it is now time to select the required device to implement the desired system function from a p.l.d. databook[1]. In this case, the device selected is the PLS168, Fig.3. It allows up to twelve inputs (plus clock and enable) and provides up to eight registered outputs. Additionally, the device contains six embedded registers with feedback which means the device is particularly suited to state-machine applications.

Internally, the 168 consists of fully programmable And and Or arrays. This fully programmable And/Or architecture makes this type of device functionally superior to the programmable-And/fixed-Or architecture of Pal type devices. Fusible NiCr links are used to configure the device to a particular pattern. The programmability means it is possible to configure the alarm controller in several ways while retaining the basic system i/o structure.

AMAZE SOFTWARE

Having selected a device, the system function must be programmed into it. This is done very easily using Mullard's Amaze software running on an IBM PC compatible or a VAX computer under the VMS operating system. It allows designers to define a p.l.d. in terms of Boolean or state equations and from these generate a fuse pattern which can then be sent to a p.l.d. programmer. Other features of the software include a fuse table editor to allow direct modification of the fuse pattern, a functional and a.c. timing simulator to test the device, a schematic-to-Boolean converter to develop Boolean equations from a schematic diagram of a desired circuit, a Pal-to-p.l.d. converter to convert Pal designs to p.l.d. designs, and a device-programmer interface to allow downloading of the fuse pattern to a programmer through an RS232 link.

PIN INFORMATION

Firstly, the Amaze software labels the device using a routine called the pin-list editor. Figure 4 shows the pinning information for the alarm controller. A 10bit counter within the controller produces the entry/exit and sounder turn-off delays since this makes more efficient use of the p.l.d. facilities than implementing the delays as part of the state machine. This counter uses seven internal registers with feedback and three without. For those registers without feedback, external wiring feeds their outputs back into the device to complete the 10bit counter. Pins five to ten are used for this purpose. Output T7 also forms part of the counter.

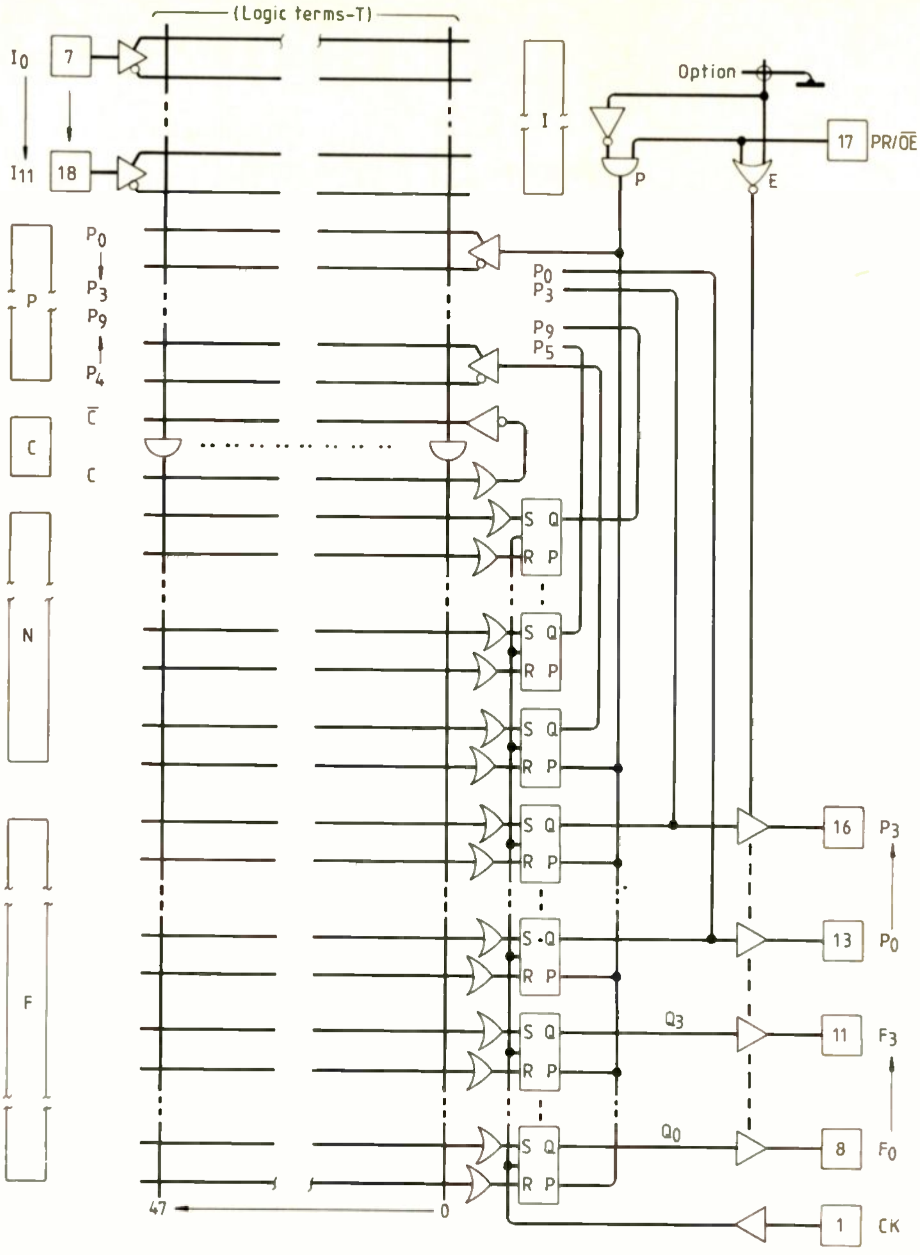


Fig.3. The device selected for the alarm controller is the PLS168 with up to twelve inputs, eight registered outputs and six internal registers.

Three other registers form state registers and are labelled SR0, SR1 and BEACON. State vectors for these registers have to be chosen with care to ensure that the beacon output is activated at the correct time. Other inputs and outputs are as already discussed. Note that the PR/OE pin is not used. This pin must be tied to ground in the final circuit.

BOOLEAN EQUATION ENTRY

Once the pin information has been entered, any Boolean equations desired can be defined using the Boolean equation entry (.BEE) file of Amaze. List 1 shows the .BEE file for the alarm controller. Any internal registers used in either the Boolean equation or state equation entry file are given names in this file, in this case t1 to t6. Equations for the 10bit counter are entered after the title line @LOGIC EQUATION, using registers t1 to t10in. Register SR0 halts and clears the counter while the controller is in certain states. This needs to be considered when defining the state vectors.

STATE EQUATION ENTRY

The state equation entry (.SEE) file of Amaze uses a state-transition language, parameters of which are taken directly from the state diagram. Information is entered into this file in a free format. The only points to remember are that square brackets should be used throughout to define the state registers and transitions, semi-colons should be used to mark the end of a vector definition and apostrophes should be used to indicate a registered output.

State vectors can be defined in the state equation entry file as shown in List 2. State vectors are simply a means of labelling an arrangement of state registers which can be used later to define state transitions. Because we are using the BEACON output register as a state register also and SR0 is being used to halt and clear the 10bit counter, particular care must be taken in defining the state vectors in this instance.

From the state diagram, the counter must begin counting during states ST_0, ST_2 and ST_3 and it must be cleared during states ST_1, ST_4 and ST_NULL. State ST_NULL represents the power-up state of the PLS168 in which all register outputs are at logic one. Thus the inactive state of the counter is defined as being when SR0 is at logic one, therefore SR0 must be at this level during states ST_1 and ST_4 and at logic zero during other states. The alarm beacon is considered to be activated by an active-low signal and must be activated during states ST_3 and ST_4. Register SR1 must therefore be chosen to ensure mutual exclusivity between state vectors.

Input and output vectors can be defined in the same manner in terms of input and output label names. In this case, however, the label names are used directly.

State transitions can now be derived directly from the state diagram. This is done using a Pascal-like state transition language and can clearly be seen in List 2. Note that multiple IF statements can be implemented as such or as CASE statements as shown.

Entry/exit and sounder turn-off delay times are represented as a decoding of the 10bit counter states. Thus to get the desired 16 second entry/exit delay, t7 must be decoded and to achieve the 128 second sounder turn-off delay t10in must be decoded.

DEVICE PROGRAMMING

With the system fully defined it is now simply a matter of assembling the design information using the Amaze assembler to produce the fuse pattern for the desired device. Should any design changes need to be made to a device, the fuse pattern may be modified directly using the program table editor of Amaze. However, this course of action is not recommended since the Boolean equation and state equation files are not altered correspondingly.

Functioning of the device can be verified with the Amaze simulator, which can also be used to check a.c. timings before downloading the pattern to a device programmer, such as a Stag ZL30A or Data I/O 29B, to program the device. Test vectors are produced either automatically or interactively by the simulator.

PROGRAMMABILITY

The PLS168 device could now be used as the controller of an alarm system. As it stands, the device assumes that all the alarm inputs indicate an alarm condition when in the high state, logic one, and that the alarms are activated when the alarm outputs are active low, i.e. at logic zero.

Should an alarm input transducer be used which indicates an alarm condition as a low state, this can be catered for by altering the .SEE file. For example, consider a smoke detector which outputs logic zero on detection of an alarm condition and assume that this transducer is driving the 'fire' input of the device. By changing all references to 'fire' in the .SEE file to '/fire' and all instances of '/fire' to 'fire' then the activation of the alarms will occur when logic zero is applied to this input and not when logic one is applied, as in the original case. Pin-list and .BEE files do not need to be altered.

Polarity of the output signals cannot be altered so easily as the device will always power-up with the outputs at logic one. This should not prove a problem since the outputs simply drive output transistors and these can be used to produce the correct polarity signal for the beacon and sounder.

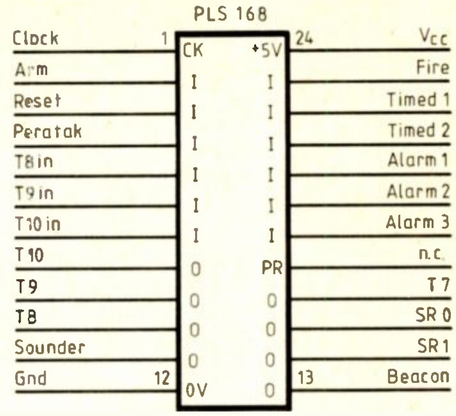


Fig.4. Pinning information for the alarm controller is used in the programmable-device software for labelling.

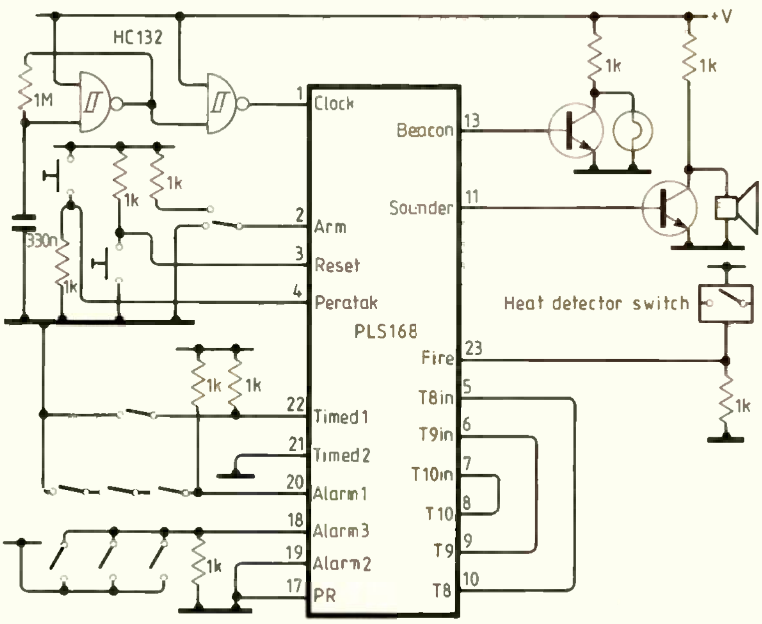


Fig.5. Alarm system based on the PLS168 programmable logic device. Entry/exit and sounder turn-off delays are modified either by changing the external oscillator circuit or by decoding a different internal counter state.

```
State machine and timer for
burglar alarm.
@INTERNAL SR FLIP FLOP LABELS
t6 t5 t4 t3 t2 t1
@LOGIC EQUATION
t1:   s = /t1*/sr0;
       r =  t1*/sr0
          + sr0;
t2:   s =  t1*/t2*/sr0;
       r =  t1* t2*/sr0
          + sr0;
t3:   s =  t1* t2*/t3*/sr0;
       r =  t1* t2* t3*/sr0
          + sr0;
t4:   s =  t1* t2* t3*/t4*/sr0;
       r =  t1* t2* t3* t4*/sr0
          + sr0;
t5:   s =  t1* t2* t3* t4*/t5*/sr0;
       r =  t1* t2* t3* t4* t5*/sr0
          + sr0;
t6:   s =  t1* t2* t3* t4* t5*/t6*/sr0;
       r =  t1* t2* t3* t4* t5* t6*/sr0
          + sr0;
t7:   s =  t1* t2* t3* t4* t5* t6*/t7*/sr0;
       r =  tl* t2* t3* t4* t5* t6* t7*/sr0
          + sr0;
t8:   s =  t1* t2* t3* t4* t5* t6* t7*/t8in*/sr0;
       r =  t1* t2* t3* t4* t5* t6* t7* t8in*/sr0
          + sr0;
t9:   s =  t1* t2* t3* t4* t5* t6* t7* t8in*/t9in*/sr0;
       r =  t1* t2* t3* t4* t5* t6* t7* t8in* t9in*/sr0
          + sr0;
t10: s =  t1* t2* t3* t4* t5* t6* t7* t8in* t9in*/t10in*/sr0;
       r =  tl* t2* t3* t4* t5* t6* t7* t8in* t9in* t10in*/sr0
          + sr0;
```

List 2. State vectors, shown here, are simply a means of labelling an arrangement of state registers which can be used later to define state transitions.

SYSTEM IMPLEMENTATION

Figure 5 shows a typical alarm system based on this device. The system clock is produced by a relaxation oscillator built from 74HC132 schmitt triggers. Values of R_1 and C_1 shown result in a frequency of approximately 4Hz which will provide the desired entry/exit and sounder turn-off delays. These delays can be modified either by changing the external oscillator circuit or by decoding a different internal counter state. For example, to increase the entry/exit delay change all references to t7 in the .SEE file to t8.

Both normally-closed and normally-open loop implementations are shown. Due to the distances involved in an alarm system, the open-loop configuration may cause problems, being driven by the positive supply. To avoid this problem, input-detect polarity of the open-loop circuit can be changed by altering the .SEE file.

Status indication can be provided by connecting leds as in Fig.6. When the reset button is pressed, any led being lit will indicate an alarm condition for that input. Note, this will not reset the alarm system unless the arm switch is off.

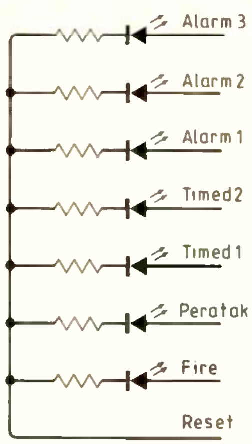


Fig.6. Leds connected to the alarm controller as shown provide status information. At reset, any led lit indicates an alarm condition at its corresponding input.

SYSTEM EXPANSION

The system can be expanded to allow more inputs and different status indication provisions by adding further p.l.ds. These devices are Mullard PLS153's used as simple decoders to allow a number of input loops or single inputs to be grouped. Timed and untimed circuits should not be mixed on these expansion devices. Figure 7 shows the pin list for one such device.

Figure 8 shows how such a device can be incorporated into the alarm system. Note that the status indication can be provided as previously or by connecting DLED, WLED1, WLED2 and OLED outputs as shown. Pin label names are given as a guide only, to indicate how the device could be used. These devices can be concatenated, allowing an almost infinite variation in i/o structure.

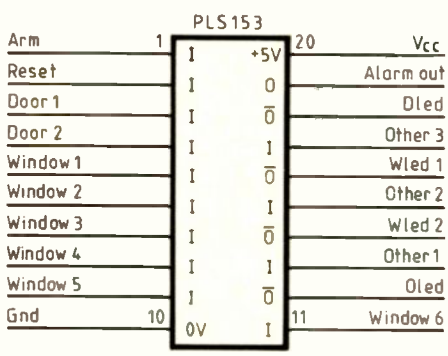


Fig.7. Adding PLS153 devices to form simple decoders allows a number of input loops or single inputs to be ignored. This is an example of a pin list for such a device.

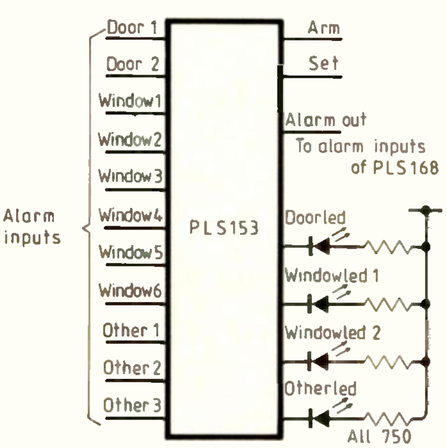


Fig.8. Expanding the system by adding programmable decoders allows more inputs and different status information provisions. Status indication can be provided as previously or by connecting the led outputs as shown.

Reference

1. Programmable Logic Devices, Mullard Technical Handbook, Book 4 Part 7a.

PAL is a trademark of Monolithic Memories Inc.

An assembled fuse pattern for the alarm controller and a Boolean equation file for the additional PLS153 decoder can be obtained by sending an s.a.e. marked 'Alarm' to *Electronics & Wireless World* Editorial, Room L303, Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS.

List 2. State vectors, shown here, are simply a means of labelling an arrangement of state registers which can be used later to define state transitions.

```
[sr0, sr1, beacon]

st_null = 111b;
st_0    = 001b;
st_1    = 101b;
st_2    = 011b;
st_3    = 010b;
st_4    = 100b;

@TRANSITIONS

while [st_null]
        case
            [arm * /fire * /peratak]            :: [st_0]
            [peratak]                           :: [st_4] with [/sounder']
            [fire]                              :: [st_4] with [/sounder']
        endcase

while [st_0]
        case
            [t7 * /fire * (arm + reset)]        :: [st_1]
            [/arm * /reset]                     :: [st_null] with [sounder']
            [fire]                              :: [st_4] with [/sounder']
        endcase

while [st_1]
        case
            [timed1 * /fire]                    :: [st_2]
            [timed2 * /fire]                    :: [st_2]
            [alarm1 * /fire]                    :: [st_3] with [/sounder']
            [alarm2 * /fire]                    :: [st_3] with [/sounder']
            [alarm3 * /fire]                    :: [st_3] with [/sounder']
            [/arm * /reset]                     :: [st_null] with [sounder']
            [fire]                              :: [st_4] with [/sounder']
        endcase

while [st_2]
        case
            [t7 * /fire]                        :: [st_3] with [/sounder']
            [alarm1 * /fire]                    :: [st_3] with [/sounder']
            [alarm2 * /fire]                    :: [st_3] with [/sounder']
            [alarm3 * /fire]                    :: [st_3] with [/sounder']
            [/arm * /reset]                     :: [st_null] with [sounder']
            [fire]                              :: [st_4] with [/sounder']
        endcase

while [st_3]
        case
            [t10in * /fire * (arm + reset)]     :: [st_4] with [sounder']
            [/arm * /reset]                     :: [st_null] with [sounder']
            [fire]                              :: [st_4] with [sounder']
          endcase

while [st_4]
        if [/arm * /reset] then [st_null] with [sounder']
```

TELECOMMS TOPICS

Co-operative effort at CeBIT

CeBIT 88 at Hanover, the largest event in the world for office automation, information technology and telecommunications, attracted 480 000 visitors to see the products and services of 2730 exhibitors, of which 980 came from 35 other countries. Because of CeBIT's wide attraction it is frequently used by companies and organizations to stage major launches. For example, Fujitsu Europe, subsidiary of Japan's largest computer manufacturer, used CeBIT as the launch pad for a range of **facsimile** machines – even though the company is not selling the products under its own name in Germany. They will be sold into the UK with a major push into the office equipment dealer market in what is the company's first venture into fax in Europe under its own name. The three Group 3 fax machines and a Group 4 fax will be supported by activity aimed at establishing a nationwide dealer network in the UK by the end of 1988.

The 17 companies and administrations participating in the current **X.400** message handling system initiative at CeBIT presented the actual application of X.400 as a highlight of their stand displays and presentations. They demonstrated the electronic exchange of messages from one stand to another, i.e. among systems made by diverse manufacturers, using the public infrastructure provided by Deutsche Bundespost and AT&T. Users were therefore able to see how electronic messaging works in practice and the benefits of this concept offers in business, trade, industrial and administrative applications.

Companies which joined forces in the X.400 initiative at the Fair were: AT&T, CAP, DEC, Deutsche Bundespost, Hewlett Packard, IBM, NCR, Nixdorf, Olivetti, Philips, Retix, Siemens, SPAG, Sun Microsystems, Systems Designers, Triumph Adler and Tandem Computers.

Another of the common standards coming to the fore is **Office Document Architecture** (ODA). This allows the connection of incompatible systems. Bull, Olivetti, ICL, Siemens and OCE had a joint stand to provide information on the current implementation. The latter company, best known for high-volume and high-reliability photocopiers, is mainly concerned with output devices. The objective of this working group is to ensure a true-to-original exchange of all kinds of documents among diverse systems, thus allowing for their further processing.

The project is supported by the EEC Commission as part of its Esprit programme. It now appears likely that ODA will be approved as ISO Standard 8613 before the end of this year.

It was at CeBIT 87 that Bull, ICL, Olivetti and Siemens demonstrated that it was possible to interchange word processed text documents between different systems, and continue processing the documents without the need for partial or total rekeying. Reactions to this first demonstration were encouraging and proved that there is ample demand for the concepts.

The presentations at CeBIT 88 extended to cover the interchange of mixed text, graphics and image documents. The interchange preserves the integrity and processibility of the document, meeting the expectations of more and more users, and overcoming the current restrictions of being able to interchange complex documents only in paper or in non-reprocessible form.

Digital Communications Inc. (DCA) of the USA used CeBIT to stage the worldwide launch of some **networking** products: the DCA LAN Gateway and DCA LanServer, which link wide area (wan) and local network (lan) users through a DCA Series 300 network processor; and an enhanced version of the company's Protocol Processor II.

A key feature of this new version, Protocol Processor II/ST, is its multiplexed slave trunk (ST) link which connects asynchronous terminal users in a DCA Series 300 network to IBM 3270 compatible mainframes or IBM System 3X hosts.

Like the earlier Protocol Processor II, the enhanced ST model allows the use of inexpensive asynchronous terminals in an IBM environment.

DCA's LAN Gateway is claimed to be the first wan processor gateway to use the TCP/IP networking protocol for accessing Ethernet-based lans. Its software resides on a datacard with a DCA series 300 processor.

TCP/IP enables terminal users on a lan to enter a simple command to get into the wan, through the wan processor, to access other resources outside his or her immediate lan, or another lan in the network. TCP/IP is considered the industry's most widely-used local area networking protocol, and is gaining acceptance in the European marketplace. In practice its throughput is of the order of 100 000 characters per second on a 10Mbit/s bus. However, DCA offers its own proprietary protocol, LanPro, claimed to offer four times the throughput.

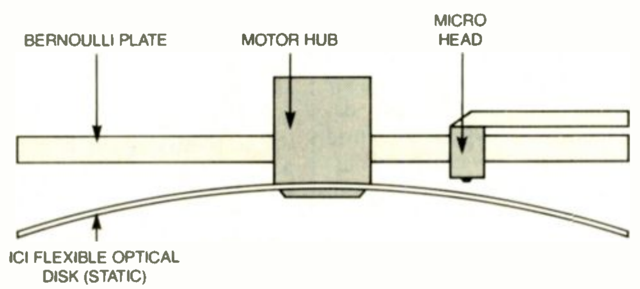
X/Open, the international consortium of 13 of the world's major computer system vendors committed to the implementation of **open systems** had a major presence at CeBIT. All 13 members were exhibiting: AT&T, Bull, Digital Equipment, Ericsson, Hewlett-Packard, ICL, Nixdorf, NCR, Olivetti, Philips, Siemens, Sun and Unisys.

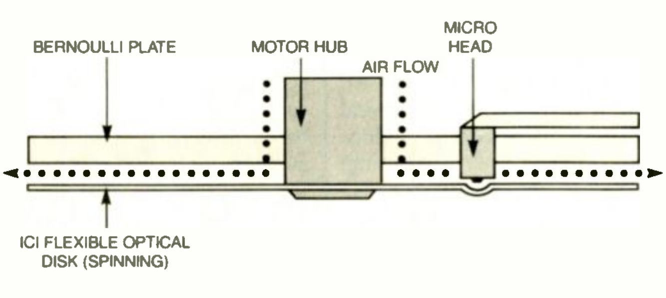
Geoff Morris, president and chief executive officer, said, "We see CeBIT as the most significant and influential event in the IT calendar. It offers a unique forum for X/Open to communicate its strategy and progess to an audience of almost three quarters of a million users and members of the worldwide computer community. The activities that we are undertaking will ensure that the X/Open messages of freedom, flexibility and long term investment that can be achieved through the X/Open computing standard are more widely understood and acted upon."

X/Open, founded in 1984, is an independent non-profit consortium of international computer system vendors. These companies are investing business, technical and marketing resources in the development of an open, multi-vendor Common

A new optical drive technology designed to handle a flexible optical disc was announced at CeBIT by ICI Electronics. It is being developed by Bernoulli Optical Systems (Bosco) of Boulder, Colorado, USA. While Bosco will be marketing its own drive units in the near future, its partner ICI was at CeBIT to promote the technology, which will also be available for licensing to other drive manufacturers.

Operating on the Bernoulli principle of fluid technology (when air above a surface moves faster than the air below, it causes 'lift' as with an aeroplane wing) the disc rotates in close proximity to the read/write head. Because the medium is flexible it is able to take up a highly planar form to a greater degree of precision than is possible with a moulded rigid optical disc. In addition, it can deform to follow the head more closely. This allows a small low-mass head which obviates the need for focussing servos. See also this month's 'Update'.





Applications Environment based on international and *de facto* standards. Specification of the Common Application Environment is achieved through close co-operation with users, independent software vendors and standards organisations worldwide. All members of X/Open are committed to supporting the environment defined.

Northern Telecom used CeBIT to make its worldwide announcement that it has significantly extended its range of **data switches** (DPNs) downwards so as to meet the needs for small to medium switches. This family of packet switches, the DPN-100 networking system, is based on the DPN-100 architecture introduced in 1987, and enables Northern Telecom to serve a wider packet data communications market. Various models offer from 8 to 30 000 access lines and a throughput rate ranging from 64 to 30 000 data packets per second.

NT can now address the needs of a market that ranges from large telephone operating companies to corporations, government, and small businesses. Northern Telecom (and its associated German company, AEG) is one of the two contenders for the second phase of the German public packet switched network. Test systems from NT and Siemens have been installed, used and evaluated by the Deutsche Bundespost. Now both companies are waiting to learn which has been awarded the contract.

Northern Telecom was also demonstrating **ISDN networking** between private branch exchanges (p.b.xs) which conform to the CCITT recommendation for Primary Rate Access, known as Q.931. Primary Rate Access is the ISDN link between p.b.xs 'in-company' as well as the interface between a p.b.x. and the digital public telecommunications network. NT believes that it is the first company to be able to provide such a demonstration even though other companies have indicated their support.

Prior to Q.931 there was no internationally agreed specification for inter-p.b.x. operation, the protocol attracting most attention being the DPNSS (digital private network signalling system). This is a British Telecom protocol that has been implemented by manufacturers supplying switches to the UK market.

In the demonstrations, NT's Meridian SL-1 p.b.xs showed a range of networking features that can be offered with Q.931. This standard is defined in the CCITT 'Blue Book', to be ratified later this year, and is expected to supersede the various national, pre-ISDN standards now supported by European public and private network operators.

Called Meridian Network Services, the demonstrations included: identification of the calling party's number; the name of the calling party, displayed across the network; the ability to forward calls network-wide from one extension to another; ring again, also across the network, whereby a user asks the network to complete a connection to a busy line once it becomes available; and a centralized message facility, providing fully digital recording and transmission of messages.

Joint venture goes ahead

The joint venture formed by the merger of the telecommunications activities of GEC and Plessey has been formally launched with the slogan "Linking up to link the world". In size GEC Plessey Telecommunications Ltd (GPT) is within the world's top ten, with a turnover of £1.2G.

With a product range embracing almost the whole field of telecommunications, GPT is established as the leading UK manufacturer. Sales levels will create the necessary funding for continuous research and development of products for world markets. Mr Richard Reynolds, managing director of GPT, said: "Over the past few years the structure of the industry has evolved to a stage where only the largest companies can provide the complex advanced products customers require in a competitive market.

"Individually Plessey and GEC have both shown the technical skills and the vision to produce these products. By combining, GPT can harmonize these strengths and give Britain a powerful, coherent voice on a truly world scale."

GaAs space switch

Bell Northern Research (BNR) has developed a gallium arsenide 4×4 space switch circuit capable of handling signals at 5GHz.

Dr Paul Jay, manager of GaAs device design at BNR, Ottawa, Canada, said that the 5GHz bandwidth "means that each channel on the chip can reliably move digital information at rates as high as 2.4Gbit/s. Any one of the four input channels may be connected to any, or all, of the four output channels", explained Dr Jay.

"As well as the ability to handle extremely high volumes of data, a major benefit of the new chip is that it can change the destination of information in the circuit in one nanosecond, enabling the device rapidly to redirect data to a given destination", said Dr Jay.

The circuit achieves its extremely high speed through the use of a BNR chip design employing GaAs and air bridge technologies.

GaAs is particularly suited to high-speed applications because electrons travel through the material faster than through more conventional silicon based circuits. Air bridges form a complex network of highly conductive metal pathways which direct information through the circuitry on the chip. Made of gold, the air bridges are supported above the circuit on posts to avoid contact with the surface of the chip, explained Richard Streater, manager of advance processing.

"This arrangement limits the interference between adjacent signal routes and preserves the integrity of the signals as they race at high-speed through the GaAs circuitry", he said.

• *See also Satellite Systems, page 583.*

DIY pilot briefing

The Civil Aviation Authority has awarded a contract valued in excess of £1.5M for a computer-based briefing system for civil aviation pilots. The contract, for the MARS system, the Meteorological and Aeronautical Information Services Retrieval System, has been awarded to Systems Designers, a major UK consultancy.

The aim is to provide pilot self-briefing terminals, initially at 12 major UK airports, plus three CAA units, by the spring of 1989. The former are all airports at which the CAA provides air traffic services.

However, the system will have the capability to provide a direct access to additional UK users, including airports, airlines or individual users. Access arrangements for these users will depend on the telecommunications that are available and the type of data retrieval required by the user.

MARS will change the way in which pilots are briefed for flights, replacing the current methods whereby each pilot may have to sift through unwanted data in order to obtain the appropriate information. Instead, pilots will have access to computer terminals and printers from which they will be able to select specific meteorological charts, forecasts, actual weather reports and aeronautical information that they require for pre-flight planning and in-flight use.

UK trunked radio agreement

GEC, Motorola and Philips have signed an Intellectual Property Rights co-operation agreement concerning the manufacture of equipment which complies with the UK standards for trunking systems. By 1992, all equipment operated on the new networks will need to have been approved to this specification.

The co-operation agreement relates to the standards defined in specifications MPT 1327, MPT 1343, MPT 1347 and MPT 1352 and to patent rights owned by the three companies which may impact these specifications. The companies have agreed to make available licence rights to users and manufacturers on a defined basis.

Detailed provisions also exist to ensure that any modifications to the standards which become necessary over time are published and available to all participating manufacturers.

Telecomms Topics is compiled by Adrian Morant.

Reversing a 'constant' current in an inductor

A need to reverse 'constant' d.c. current through a coil can only be a recipe for trouble; David Griffiths offers a guide to some of the 'funnies'.

D. GRIFFITHS

If capacitors were very much more cumbersome and difficult to make than inductors, then we would use LR networks around our transistors and op-amps without batting an eye-lid – well, maybe. The little inductive monster that caused this reflective mood was virtually *air-cored* too, forsooth, so I could not even blame non-ideality of its core for my puzzlement.

For the reader who might be engaged in a similar electronic skirmish, I relate the story using rounded numbers for the parameters. I know many consider it 'low-brow' not to use algebra at every opportunity but I strongly believe that an initial presentation is best done numerically, so that one can sort out what quantities are "big" or "small" in some unfamiliar situation.

The design requirements all seemed as innocuous as they often do at the beginning. There was this little coil, said to be some 25 mm in diameter, totally encapsulated in epoxy resin, through which a constant 30mA was to be passed and the direction of flow was to be reversed as abruptly as possible at around 1kHz. Considering what the switched-mode power people do, this ought to be simple.

Closer enquiry revealed that the 30mA had to be constant within 0.3% long term at modest ambient temperatures and that a 1% tolerance had to be maintained on the 30mA from unit to unit, despite production variations of the circuitry and the aforesaid little monster.

The coil resistance was a nominal 250Ω and so it seemed likely that the 7.5V.d.c. drop across it at 30mA could be easily accommodated within the ±15V supply lines available. By tickling the coil with a square wave voltage applied through a few 100kΩ, pretty ringing was observed at 20kHz, which dropped to 3½kHz with 10nF across the coil. Because the resonant frequency goes as the square root of the circuit capacitance, this frequency ratio of 20/3.5≈6 meant that the 10nF was some 36 times larger than the coil self-capacitance. Thus, I could get an adequate estimate of the inductance by using $C=10nF$ and $\omega=2\pi\times3.5\times1000$ radians/s in $\omega=1/\sqrt{LC}$; this gave $L=0.2H$.

This surprisingly hefty inductance, for such a small 'air-cooled' coil, indicated that there may be much more inductive energy to dissipate at each current reversal than might be supposed. Plugging values into $LI^2/2$ gives 90 microjoule; with two reversals per cycle and a possible 1kHz repetition rate, this gave 180 milliwatt which looked reasonable. As it turned out, I could not get near the proposed 1kHz rate, so inductive dissipation worries were even less.

There was, though, the worry about the voltage spike that occurs when current reverses, as the following figures show. The coil self-resonant frequency of 20kHz, noted above, together with L=0.2H, gives a coil self-capacitance of 300pF. The energy stored in a capacitor is given by $CV^2/2$ and thus, if the 90 microjoule of inductive energy were allowed to swing across into the self-capacitance, there would be some 700V generated – if nothing gave way. Clearly, zener clamping across the coil would be needed.

Because of the voltage spike just calculated, it is easy to be trapped into thinking that there will be a correspondingly massive current surge into a voltage clamp across the coil and that a heftily rated zener will be required. Fortunately, this is not the case at all; the 30mA in the inductor can only decay (and go to −30mA in this case) and so any circulating currents in the zener (from the coil) cannot exceed 30mA, all nicely well defined. Thus one can hang surprisingly small diodes and zeners directly across relay coils without any series resistor.

From previous experience, I had little doubt that a three-terminal voltage regulator connected as a current generator would be a satisfactory source of the constant 30mA, and provide it without using up too much of the voltage headroom of the ±15V supply lines. In Fig.1, the LM317 and R_1 provide this function, with R_2 and R_4 providing fine adjustment of the sensing resistance value. The output pin of the National LM317 will take up whatever voltage will cause a nominal 1.25V to appear across R_1, provided the output current has some lower voltage to go to. At the current level used here, the data sheets show that a minimum of 2V between 'in' and 'out' on the 317 is required, so the device will stay in its linear regime if the bottom end of R_1 is always at least 4V below +15V, by suitably clamping the coil voltage transient.

The 317 is a particularly good choice of device to use in this way, for which hint I am indebted to that invaluable compendium of lore 'The Art of Electronics' by Horowitz and Hill (Cambridge U.P.) In the 317 the current out of the 'adj' terminal is very small (50μA nominal) and astonishingly independent of load current (and input/output voltage and temperature), so that the output loading by the 'adj' pin does not greatly impair the servo action, which is now striving to give a high output resistance in this configuration. The 'third-pin' current is made so low and constant by steering all the 'return' currents of the amplifiers in the 317 to the 'out' pin; thus, this regulator must be used to provide a minimum output current of 10mA (worst case), which is no problem in this application.

The output resistance of the LM317 was assessed by unhitching the bottom end of R_1 from the circuitry and connecting it via a milliammeter successively to the 0V and −15V lines; the nominal 30mA current increased by some 30μA for this change of compliance voltage of 15V, implying a z.f. output resistance of 15V/30μA = 500kΩ. It is sobering to reflect that, if the various feedback tricks had not yet been thought of, then this current generator performance could only have been attained by feeding 15kV to a 500kΩ resistor.

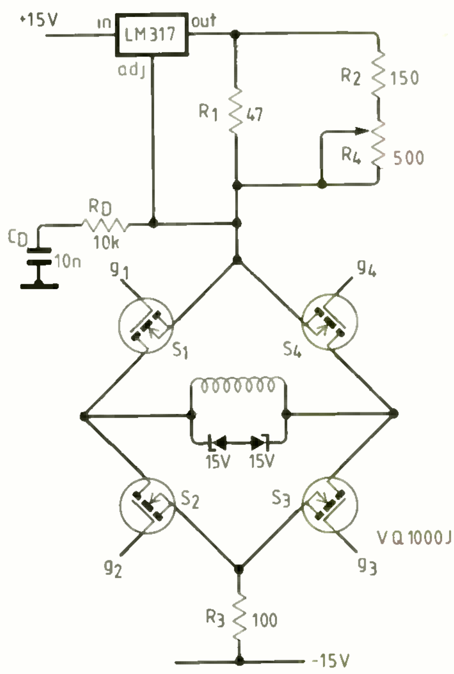


Fig.1. Current regulator and bridge switching circuit.

The circuit is almost completed by hanging a bridge of switches around the coil. The four mosfet switches in the ubiquitous little VQ 1000J from Siliconix handle the prospective coil current very easily, their typical 5 ohm resistance giving negligible power dissipation or voltage drop. Since their gate-source rating is ± 40V, they can be controlled directly by the op-amp comparators in the LF353 as shown in Fig.2. For half a cycle S_1 and S_3 are 'on' with S_2 and S_4 'off', then the switch drive conditions change to reverse the direction of current flow in the coil. Due to slew-rate limitations in the op-amps, there is some time skew in this switching, but it is trivial compared with the time taken for the inductive transient to decay to a negligible level.

To ensure that the VQ1000J switches are definitely 'off', their gates must not be significantly positive with respect to the corresponding sources. Since it would be unwise to assume that the LF353 op-amp outputs will swing more than ±12V about 0V, the bottom of the switch bridge thus needs to be at least 3V above −15V. This voltage drop is provided by R_3, which also makes a convenient monitor of the current generator output: if R_3 = 100Ω, of 1% tolerance, then the circuit current can be set up to the specified precision by adjusting R_4 until there is 3.00V across R_3.

A pair of 15V zeners back-to-back across the coil gives a nominal 16V clamp level, since one or other zener must be forward biased. As will be shown, a quicker reversal of the coil current could be obtained by using higher zener voltages, but a 15V pair does allow the circuit to operate off ±12V supplies, which was a useful option in the present application.

Now, both reader and writer must be brave and try to visualize what goes on while the coil current is reversing. First, in an effort to simplify, let us re-label the constant voltage at the top of R_3 as 0V, as in Fig.3, and mark the coil ends as 'x' and 'y'. This gives us sketch 3(a), showing 30mA flowing through the coil from 'y' to 'x', with the zeners 'off' since there is only 7.5V across them.

Still looking at Fig.3(a), consider which way the voltage will go at point 'y' when the current generator supply is interrupted (as it is in effect when the bridge switches reverse). In getting point 'y' up to +7.5V, the current must have been changed, thereby involving a particular sense to dI/dt, the rate of change of coil current. Whether or not we label this sense as positive or negative, it is certain that, as the coil current decays, then the sign of dI/dt must change – and cause point 'y' to go zooming off in the opposite sense, trying to take 'y' negative with respect to 'x' by the 700V or so calculated earlier.

Taking a deep breath, we see that clamping then occurs with 'x' 16V *positive* with respect to 'y' when the current generator is in effect disconnected.

Taking another deep breath, we tell ourselves that 30mA is *still* flowing in the *same* direction from 'y' to 'x' at this time. I think that this is the sticky bit about inductors – the voltage has whistled off in the other direction, but the current is still flowing in the same sense.

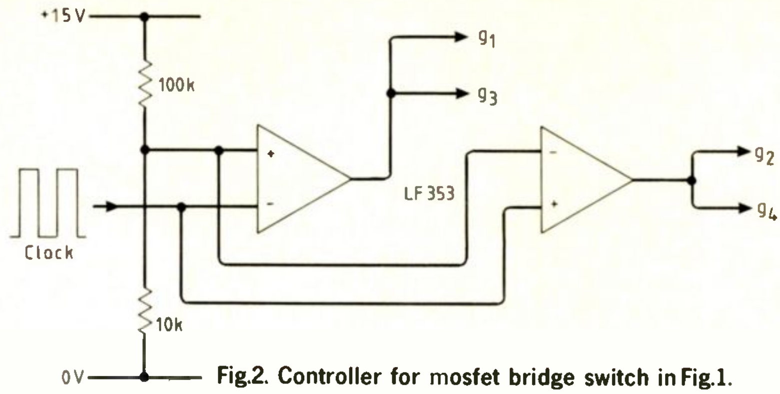


Fig.2. Controller for mosfet bridge switch in Fig.1.

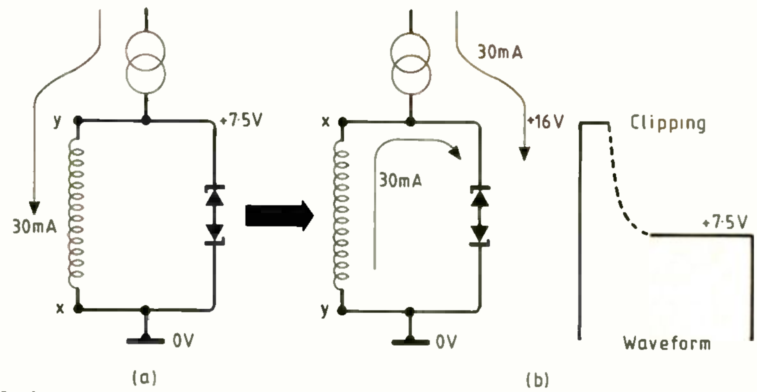


Fig.3. Switch-over conditions in the coil, with the steady voltage at the top of R_3 re-labelled as 0V.

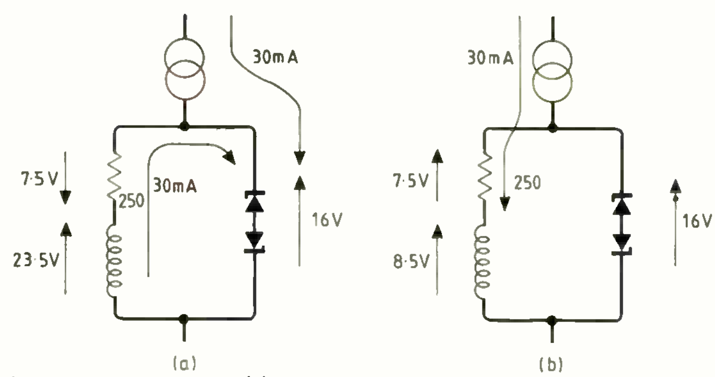


Fig.4. Voltages at the beginning (a), and end (b) of the current-reversal transient.

If you agree to the story so far, then you will have to concede that, immediately after the switches reverse the coil connections, the conditions must be as shown in Fig.3(b), improbable as it may seem at first glance. Because the LM317 regulator is clearly not going to accept the unwanted gift of 30mA pushed back towards its output (since there is enough voltage across it to keep it pumping *out* 30mA), then there must inevitably be no less than 60mA through the zeners at this stage.

These currents can be monitored quite easily if one has a dual channel oscilloscope with the invert-one-channel and add-channel facilities, giving the user a differential amplifier, in effect. Then one puts a low value resistor, say 22Ω, in series with the coil and then in the zener arm and differentially monitors the voltage across it, finding this 30mA 'upwards' in the coil and 60mA in the zeners just after switch reversal.

The oscilloscope traces show that the coil current decreases from 30mA 'upwards', passes through 0mA and finally taking up the steady value of 30mA 'downwards'. When the coil current is zero, the zeners take the 30mA from the LM317. When the coil finally accepts the full 30mA from the current generator, there is no current for the zeners and they come out of conduction, the coil voltage taking up its steady value of 7.5V due to its ohmic drop.

Bitter experience over many years has shown that it is remarkably common for a newly developed circuit (or complete instrument) to seem quite satisfactory, but for some aspect of it to be working in an unforeseen and unperceived way – giving rise to premature breakdown or inexplicable failure to pass apparently properly toleranced test schedules in production runs. By definition, of course, there can be no procedures guaranteed to find the as yet 'unthought of' but a powerful counter-measure is to estimate as many as practicable of the secondary features of a new circuit or instrument and check the correspondence with bread-board behaviour. If only you could know which were the aspects to check!

With these thoughts in mind, it was prudent to try to estimate the time the coil voltage should be clamped by the zeners. Of course, a modest home computer could solve the circuit equation easily enough, but I feel that the use of pencil and paper whenever possible is more likely to force one to ponder the details more carefully, which is the object of the exercise.

I think the clipping situation is best viewed thus. First, consider that the coil resistance and zener slope resistances are negligible. In this simplified case, Fig.3(b) shows that the coil back e.m.f. must be a constant 16V during the whole clamping cycle. That is L.dI/dt = 16, which, with L = 0.2H, gives dI/dt = 80A/s. With a current change of 60mA during reversal, this leads on to expect a clamping time of 0.06/80s = 750μs, which is close to the observed value – praise be.

Thus encouraged, one can now consider the effect of the internal resistance of the coil, shown by the 250Ω resistors in Fig.4. Just after coil reversal, Fig.4(a), the current is flowing 'upwards' which means that the 7.5V ohmic drop *adds* to the zener voltage seen by the coil inductance. Thus, at this instant, L.dI/dt = 16 + 7.5 = 23.5V, giving dI/dt = 118A/s.

At the end of the reversal phase, with the 30mA now flowing 'downwards', Fig.4(b) shows that the coil has only to push out a back e.m.f. of 16 – 7.5 = 8.5V, giving dI/dt = 43A/s, which is much less than the initial value.

The oscilloscope showed the coil current waveforms to be 'exponential ramps', so to speak, with slopes (dI/dt) at the beginning and end of the reversal period consistent with the expected ratio of 118/43. Since the ohmic drops successively add to and then gradually subtract from the zener voltage seen by the inductive part of the coil, it is not unreasonable that taking a mean back e.m.f. of 16V gave a clamping time comparable to that observed.

Having found nothing suspicious under that stone, attention could be turned to the problem of finding the source of the ferocious 20kHz ringing voltage across the coil that started at the end of the zener clipping period (the dashed region in Fig.3(b)).

Here I fell, yet again, into that trap to which we electronic toilers seem particularly prone: "When in difficulty, unhesitatingly blame the component which you are most scared of, and stick to your convictions – regardless!" It thus only took me milliseconds to be quite certain that this ringing was due to the LM 317 regulator, because it had such complicated internal circuitry; what better reason could one want? and anyway 'there was nothing else to blame'.

The price of such emotional "thinking" is usually a trip in the wilderness. I was eventually forced on to the right track by the serendipitous observation that a 10kΩ resistor *alone* from the output of the regulator to 0V (R_D in Fig.1) stopped the oscillations, giving a fast smooth decay from the +16V to +7.5V level. But how could a resistor alone 'stop an amplifier oscillating'? That it was not due to the piffling extra direct current flowing was readily confirmed by placing a 0.1μF capacitor in series with R_D (impedance only about 80ohm at 20kHz) and finding no significant change in the smooth, fast decay after clipping.

But who said 'the amplifier was oscillating'? Just because the voltage at the top end of the (inductive) coil is ringing does not necessarily mean that the *current* waveform from the *current* generator LM317 must be ringing. So that was it – and painfully self-evident as these things inevitably appear in retrospect. When the coil current has almost steadied at 30mA 'downwards', the zeners go 'off' and present a very high resistance; the coil is fed by a *current* generator of some 500kΩ output resistance, at least at z.f.; when the coil voltage tries to decay from +16V to 7.5V, the coil is thus virtually open-circuit and therefore its *own* lightly damped self- oscillations are only to be expected. Of course, of course.

Putting the damping resistor R_D in the position shown is just the same, as far as damping is concerned, as putting it directly across the coil, since the top of R_3 is held at a steady voltage (i.e. at a.c. ground) due to the 30mA steadily flowing through it from the current source. In the commercial design I left R_D in the position shown, where its relation to the coil is not so obvious; no need to make life too easy for the 'opposition', is there? The capacitor was added so that R_D did not affect the steady value of current received by the coil. The value of C_D was chosen so that the resulting time constant $R_D.C_D$ was as short as possible without the impedance of C_D being too large at the ringing frequency.

With a transient time around the 1 millisecond mark, a clock frequency of 110Hz was chosen in the application of this circuit. We have seen that, during the clipping period, the average zener current is about 30mA, so the mean zener dissipation is 15V × 30mA × 750μs × 110Hz = 37mW when reverse biased; we can safely ignore the dissipation in the zeners when they are forward biased, as their voltage drop is then so much smaller.

In production, it was desirable to burn-in the p.c.bs without the coils connected and it turns out that it is this requirement which sets the required power rating of the zeners; 15V and 30mA can be relied upon to give 450mW during the whole of each half-cycle in this case and it was thus prudent to select 1.3 watt types in case the clock should fail.

The main design details were just about completed by looking at the worst case dissipation in the LM317; with 3V across R_3, 7.5V across the coil and 1V across R_1, the maximum possible drop across the LM317 is (30 + 5%) – 11.5 = 20V, giving 600mW at 30mA, which is easily handled.

These little misadventures perhaps emphasize how important it is to think in terms of *currents* when an inductance dominates a circuit and to keep remembering that voltage drops will probably be much more influenced by inductive L.dI/dt than by ohmic I.R, giving voltage and current waveforms that can be very different indeed.

Dr D. Griffiths is at the Physics Department, Imperial College, and concerned with applying analogue circuitry to instrumentation problems.

Win our writing competition and spend a week in Japan

You have until 30 June 1988 to let us have your entries for our writing competition, the initial announcement of which appeared March. Three and a half months might seem ample time in which to compose 4500 words or so, but if you are of the same persuasion as the majority of writers the only compelling stimulus to the start of the pen-scratching or keyboard-tapping process is the sudden awareness of a deadline a couple of days away.

We reproduce here the March leader, which might provide some food for thought.

In the eighty-odd years since radio and the wider area of electronics began to develop, we have all been beneficiaries in one way or another. There is hardly any field of human activity which has not been affected, where it is entertainment, communication, travel, medical research or industry in general.

All this is obviously greatly to be desired and the benefits of using electronics for these purposes cannot be gainsaid. But, nevertheless, one is sometimes conscious that there is, perhaps, an imbalance in the efforts applied to development. In recent years, the ingenuity of electronic engineers and capital investment have been directed to a constantly increasing extent to the development of space electronics, communications and 'defence' equipment which, if it achieves its aim, will never be used.

Communications apart, the majority of effort is wasted so far as direct benefit to mankind is concerned in the foreseeable future. In a world that is beset by deprivation of many kinds from the fundamental needs of life itself to the luxury of education, one could fairly hold the opinion that further developments in exotic electronics might at least be restrained in favour of a wider provision of more basic requirements.

The application of effort in our field of electronics might not seem immediately relevant to the alleviation of famine and pestilence but the attitude of mind that impels continuous investment of indulgent or lethal hardware is questionable. To expect companies throughout the world to turn down profitable development and production contracts would be naive, but a subsidized programme of development directed at more fundamental needs is perhaps possible.

Elsewhere in that issue appeared the announcement of a competition in which readers are invited to set down their views on the way forward in engineering development. It may be that the admittedly idealized throughts expressed above will be considered too ingenuous to be true, or that the existing regime is completely satisfactory. In any event, we expect to see a large number of thoughful essays which should give rise to an interesting discussion, if nothing more useful than that.

Bear in mind that engineering is international: narrow, nationalist politics are, of course, important but the aim of the competition is to elicit opinion on the larger question of the direction in which international effort in electronics might most usefully be directed.

Our intention is to publish a selection of the best essays, so that the length should not exceed about 4500 words, or three printed pages in *EWW*. Diagrams can be used if necessary, but the space they occupy will have to be deducted from the 4500 words.

NEC Electronics (UK) Limited have joined *EWW* in sponsoring the competition and have provided the first three prizes.

Pioneers

18. The Siemens brothers: Werner, William and Carl – they founded an empire.

W. A. ATHERTON

For a man born a German to be considered for burial in Westminster Abbey is a most singular honour. Though in the end William Siemens was not buried there, his funeral service was held in the Abbey, in November 1883. Two years later, an Engineers' Memorial, a window depicting his work, was unveiled there. It was to be destroyed as a result of war between his native and adopted countries.

William Siemens came from a very large family, being the seventh of fourteen children born to Ferdinand and Eleonore Siemens. Three of these, Werner, William (Wilhelm before he anglicized his name) and Carl built the dynastic empire that became the House of Siemens.

The father of this brood was a tenant farmer near Hanover, and it was there that Werner (1816-1892), the first son, and Wilhelm (1823-1883), the fourth son, were born. Soon after Wilhelm's birth the family moved some 120 miles to the Lübeck area north-east of Hamburg where the father managed a large estate. There Carl (1829-1906), the sixth son, and six other children were born.

WERNER SIEMENS

Ernst Werner von Siemens was the true founder of the Siemens engineering fame and fortune. Lack of finance thwarted his desire to study architecture and so in 1834 he joined the Artillery Corps as an officer cadet. In Berlin his military training gave him a thorough grounding in mathematics and science. Once out of training he used his spare time to continue his studies and to experiment.

He also took a keen interest in the education of his brother, Wilhelm, in whom he saw great potential as an engineer. With his parents' consent, Wilhelm entered an 'industrial school' close to where Werner was stationed. Werner taught him mathematics early in the morning, before school, so that he could omit the subject at school in favour of English, which Werner considered important.

This concern for one brother was soon to be extended to the rest of the family. Their mother died early, in 1839, and their father the next year. Responsibility for the clan now fell to Werner as eldest son, at a time when the youngest was still under five.

Spurred by the financial requirements of his brothers and sisters, of whom ten survived to adulthood, Werner pursued his experiments and invented and patented an improved method for electroplating gold and silver. In 1843, at the age of 21, Wilhelm was given the job of selling the process. In Hamburg he sold the design of a powerful battery to a window-frame maker (for copper plating) and so financed a trip to England, the voyage costing £1.

Once in London Wilhelm Siemens looked around for help. Seeing a sign for an undertaker he, perhaps not unnaturally, entered to see if they could 'undertake' to help in

Main picture: Sir William Siemens (1823-1883). Below, left to right: Werner Siemens (1878), Carl Siemens (1900), Johann Georg Halske (1865). All by courtesy of Siemens Ltd.

selling his electroplating process. Eventually he found what he was looking for – a patent agent – who put him in touch with Richard Elkington of Birmingham. Elkington helped "the German" take out a British patent and then bought the lot for £1600, less the £110 cost of the patent. Wilhelm returned home a hero, the financial saviour of the family.

The following year he was back in England with new inventions and high hopes. But hopes and money were squandered pursuing lost causes. Then in 1848 a novel steam engine, invented by Wilhelm, secured an income of £400 a year. This helped settle him in Britain and banished thoughts of joining the California gold rush. Werner had advised that it was "better to make gold than to seek it".

SIEMENS & HALSKE

Even whilst in the Army, Werner had determined to devote his life to science and technology, as we now call it, and had set his goal as building a great business firm. The foundation was to be the electric telegraph.

About 1842 some early Wheatstone telegraphs were brought to Berlin for examination by a man whose son was an army colleague of Werner. Werner Siemens was soon involved. He produced a new design which was to be manufactured by a clockmaker. The poor clockmaker was out of his depth and their agreement was scrapped in 1846. Instead Werner entrusted the construction of a prototype to two mechanics, Boettcher and Halske. After many modifications this prototype gained the approval of the Prussian Telegraph Commission and a Prussian patent was issued on 7 October, 1847, six days after the foundation of the Telegraphen-Bau-Anstalt von Siemens & Halske.

Johann Georg Halske (1814-1890) had spent a long time in Berlin as a precision instrument maker and was well respected at the University. It was his craftsmanship as well as Werner's design that made the Siemens telegraph a success. With money advanced by a cousin of Werner's (a very sound investment as things turned out), premises were rented in Berlin and a factory employing ten men was equipped on the first floor. Halske, the works manager, moved in above and Siemens below.

The next year political events underlined the usefulness of the electric telegraph. In March there was a revolution in Berlin, after which the first German National Assembly gathered in Frankfurt-am-Main. The little firm had its work cut out to construct a telegraph line between Frankfurt and Berlin. For part of the year Prussia was at war with Denmark and Second-Lieutenant Siemens found himself on active service at Kiel. Meanwhile the Morse telegraph had arrived from America and proved much faster than the Siemens equipment but Siemens and Halske were invited to manufacture it.

By 1850 the firm of Siemens & Halske was busy with orders for the Prussian State Telegraph, and for railway and fire brigade telegraphs. They had made very healthy profits, had 32 employees (including brother Friedrich) and were about to appoint Wilhelm as their agent in England. In 1851 they won a bronze medal at the Great Exhibition in London. But medals do not make profits, and what Werner and his partner wanted were orders not medals.

Despite trips by Werner to London and Paris, plus Wilhelm's agency in London and Carl's being stationed in Paris, it was from St Petersburg in Russia that the first big foreign order came. And it came at the right time to rescue the young firm from a financial crisis. By 1852 the healthy profits of the two previous years were history. Wilhelm in London and Carl in Paris had used up funds but had produced no orders. In Berlin, Halske frequently had to borrow money to pay the staff. Worse, the firm had just lost its best customer and some of its reputation.

In building the Prussian State Telegraph network, buried wires insulated with guttapercha had been used in preference to overhead wires. Guttapercha, a rubber-like substance, had recently been introduced from the Far East. It was to have a long career as an electrical insulator, especially in submarine cables. But in the Prussian system the guttapercha had been vulcanized, and that was a mistake.

Vulcanizing meant adding sulphur. In time the copper wire reacted with the sulphur and destroyed the insulation. "Out of order" became the state of play on the Prussian system. Of course Werner Siemens was blamed. He replied that unvulcanized guttapercha would have been ideal and that all would have been well if the lines had not been laid in the hurried cost-cutting way they were. The director of the Prussian State Telegraph took umbrage, severed relations with the firm, cancelled all orders and invited others to copy the equipment.

This could have been a fatal blow. However the firm had sold 75 printing telegraphs to Russia for the St Petersburg to Moscow line. This was followed by a massive order for a state system which extended from Finland to the Black Sea, and from Moscow to what is now western Poland. A long-term fixed-price maintenance contract tied to the huge order meant financial security for the firm. Even the European financial crisis of the late 1850s did not shake it. To manage the business Carl took up residence in St Petersburg, where he married a Russian girl.

With business now booming, the cousin who had put up the original capital was paid off and Carl now joined Werner and Halske as the third partner in 1854.

THE INDO-EUROPEAN LINE

Meanwhile Britain could have no long-distance telegraph links with her empire until the sea had been conquered.

The first submarine cable across the English Channel was laid in 1850, but that was soon cut by a French fisherman who, it has been said, thought he had killed a sea monster. More likely he was after the reputed gold (actually copper) at its centre. A successful cable was laid the next year.

Other submarine cables followed quickly, as shallow, and then deeper, waters were crossed – and much expensive cable was lost through poor insulation and breakages. Two unsuccesful attempts were made in the 1850s in heroic attempts to span the Atlantic, though the second cable worked for a short time.

Like many others William Siemens turned his attention to submarine telegraphy. At first cables were made with Newall & Co., but in 1858 a British subsidiary of Siemens & Halske was formed under William and a cable-making factory built at Woolwich. The first two attempts at cable laying were disastrous and William and his new wife were nearly shipwrecked. Eventually things were sorted out but Halske had just about had enough of this risky entrepreneurship. Though he remain friendly he announced that he would retire from the business in 1867. In 1865, therefore, the British subsidiary changed its name to Siemens Brothers.

William by now was pushing hard for a direct line from England to India. Forming links between existing lines did not hold the same political appeal as a single British-owned venture. Such links had been possible since 1865 but the slow and unreliable service meant that "anyone cabling to India had to be lucky".

Siemens & Halske and Siemens Brothers now proposed what, in its day, was one of the technical wonders of the world, an 11 000km automatically-operated line from London to Calcutta. It was driven by punched paper tape and had only one interconnection, in Tehran. It remained in use until 1931. Some parts of it are thought to be still in use today.

The line was completed by the end of 1869 and its construction was quite an adventure story involving storms at sea, construction gangs protected by Russian soldiers, natives amusing themselves by taking pot shots at the insulators, disease, fever, and even one native servant being beheaded by his fellows.

The Indo-European line was William's greatest success, the equal of any of his other exploits in electrical and mechanical engineering. With a man so talented, in fact with a family of brothers so talented, it is of course possible to write, not one, but many books about their exploits; and many do exist. Werner Siemens was one of several inventors of the self-excited dynamo. (That other great telegraph inventor, Charles Wheatstone, was another.) An electrical unit, the siemens, is named after Werner; originally it was a unit of resistance before being up-ended to become the unit of conductance.

In Britain, Siemens Brothers had a chequered history. Up to about 1910 the company was marginally bigger than its German brother, but in 1914 its assets were sequestrated, parts going to what became AEI and English Electric, now GEC. In 1966, when Siemens proper re-started in Britain, the name Siemens had to be bought back. The parent company, Siemens AG of Germany, now employs over 350 000 people worldwide. Those ten men originally employed by Siemens and Halske would never have believed it. But Werner would. That was his dream.

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NEW PRODUCTS

Emitter-coupled logic array

High speed is built into Motorola's e.c.l. bipolar arrays. MCA1500M contains 1708 gates and 1152 bits of ram, each internal gate having a typical propagation delay of 0.3ns and the output gates 0.75ns. Rise and fall time of 1ns can be slowed down optionally to 1.5ns for applications where lower edge speeds are desirable. Ram access time is typically 3.5ns.

Three metal layers are used to define the functions of the device and distribute the power. Additional features are high-value pull-down resistors on all input pins, two strobe generators to simplify internal timing, and on-chip ram-test circuits which are independent of the configuration actually in use. Internal voltage regulation is also included.

The i.c. interfaces with other e.c.l. devices: up to 64 outputs can drive 50Ω loads and 55 outputs can be used with 25Ω loads.

The device has been provided with a cad system. Other details from Motorola Ltd, 88 Tanners Drive, Blakelands, Milton Keynes, Bucks MK14 5BP.

Electronic mail on a PC

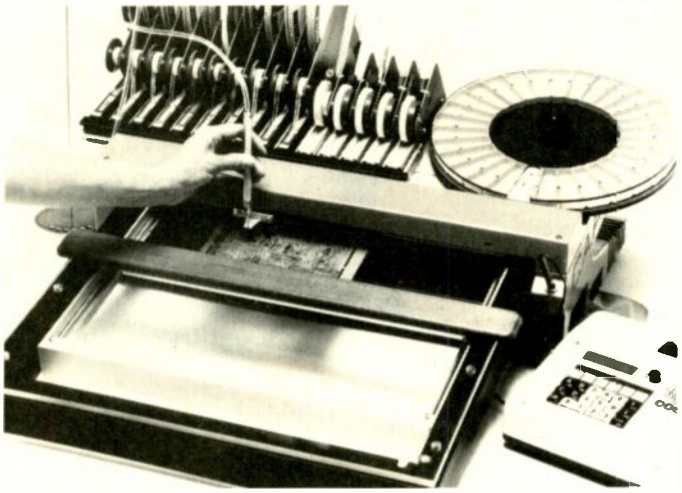
New software will enable IBM PC users to link in to an electronic mailbox service. The system was one of the first to conform to the international X.400 standard, and was previously available for use on the BBC micro (the design was published in *E&WW* 1985).

Mail is prepared at any time, using the software and stored in a file called 'OutTray'. It is automatically transmitted down a telephone line overnight when prompted by the Interspan host computer. Similarly, any mail addressed to you is delivered to your 'InTray' file and may be read the next day.

Interspan makes a charge of 2p per 1000 characters but out of that they also pay for the phone calls and claim that this is cheaper than sending letters.

The convenience and low cost make the system especially suitable for groups of small businesses, for example, a chain of shops. It can handle plain text or documents, programs or other files.

The software includes a number of utilities, including mailing lists, standard letters and 'address-book' files for saving details of correspondence. On-screen menus and help messages make the system easy to use. Interspan Electronic Mail Ltd, Intercell, 1 Coldhams Lane, Cambridge CB1 3EP.



Semi-automatic pick-and-place for surface-mounts

Short runs of complex boards are usually not suitable for manual assembly, but are not worth the complicated set-up and progamming for a fully automatic machine. Some automation is provided in the Sohlberg-Surtech Caps system which has an operator to actually pick up the components and position them. Sequences of l.e.ds indicate which component is the next to be selected. The component is picked up with a vacuum tube which is then placed in a notch on a movable bar. The bar positions the component.

Programming the work station is carried out by a light pen for the component selection sequence and joystick for the XY coordinates on the p.c.b. During assembly a foot-switch is used to indicate the completion of each step. Memory in the system can hold up to 1000 program steps.

No external vacuum line is needed for the system, which is self-contained. It can cope with all the packages that components are supplied in as well as loose components in carousels. Board sizesup to 12in by 16in (300mm by 400mm) can be accommodated. Sohlberg-Surtech Ltd, Unit 4, Intec 2 Wade Road, Basingstoke, Hants RG24 0NL. Tel: 0256 470848.

Gaussmeter now has GPIB

Applications for the Bell 615 digital gaussmeter have been extended by the introduction of a GPIB link. More than 100 different magnetic field measurement probes, with differing physical and electrical characteristics, are available and can match the instrument to almost any measurement requirement. Hall-effect sensors are combined with a modulated-carrier amplifier system and the meter can be calibrated internally or by reference to some external standard.

Magnetic flux densities are measured in five ranges from 10G (0.001tesla) to 100KG (10t) with a full-scale accuracy of 5%. T.t.l.-level b.c.d. signals are available as an output and the IEEE interface is 'talk only'. Livingston Technical Sales Ltd, 2 Queens Road, Teddington, Middlesex TW11 0LR. Tel: 01-977 0055.

Integrated modem for mains communications

Data communication over a power line is provided by Mullard's NE5050 modem i.c. The device can detect broadcasts from other transmitters and can also verify its own transmissions. This gives it the advantage of being used on complex networks that require collision detection and avoidance.

Circuitry is included to overcome power-line impulse noise and line impendance variations. The transmitter includes a continuously running Colpitts oscillator and a carrier on/off switch. This allows line-driving with a varying impedance lines.

Serial protocols are used with the device up to a limit of 100kbit/s data rate; the characteristic of the power line may restrict the data rate to as low as 1kbit/s. Available through Gothic Crellon Ltd, 3 The Business Centre, Molly Millars Lane, Wokingham, Berks RG11 2EY. Tel: 0734 788878.

Signals for current-loop testing

Simulated signals emanating from a pocket-sized instrument are used for testing 20mA loop circuits. I-Sign, as it is called, is a signal generator with five levels, selected by a single push button. The instrument is hooked into the circuit in place of the system's sensor, or in series elswhere. By stepping through the five currents it is possible to test the accuracy of the system.

Five l.e.ds are the only displays necessary to indicate that the circuit is working; when lit, each indicates that the circuit is complete and the resistance sufficiently low to carry that signal level. Normal signals and two-wire transmissions are simulated by the instrument with an accuracy of 0.1%. Seaward Electronic, Bracken Hill, South West Industrial Estate, Peterlee, Co. Durham SR8 2JJ. Tel: 091 586 3511.

NEW PRODUCTS

Computer interface is twice as fast

A controller i.c. for the small computer system interface (SCSI) is fully compatible with, but twice as fast as the widely-used NCR 53C80. Logic Devices' L53C80 transfers data between computer and peripheral at up to 4MByte/s. Such a doubling of speed needs no changes to software since such interfaces use asynchronous protocols.

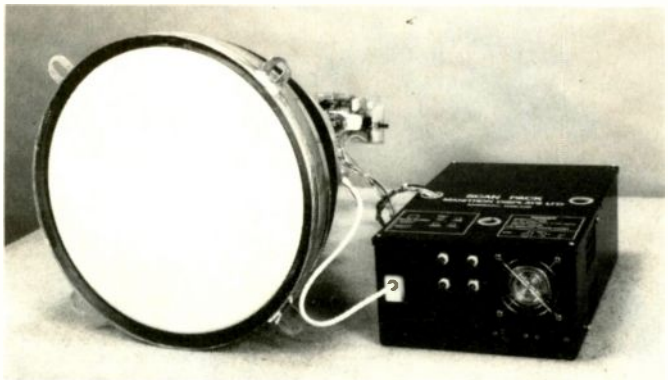
The chip has been designed to

eliminate all eight bugs known to affect the performance of the NCR part, the most serious of which was the inability to use the 'block' mode direct memory access function. Removing such bugs and retaining compatibility with ANSI X3T9.2 protocol have been the main design objectives for the new chip; the extra speed came from techniques used in the company's range of signal processing i.cs. Available through Abacus Electronics Ltd, Bone Lane, Newbury, Berks RG14 5SF. Tel: 0635 36222.

Wire wrapping made easy

Wiring a circuit can be as easy as copying the circuit diagram in components, claims BICC-Vero, who has launched a simple wiring system called Circuigraph Easywire.

Connections are made by winding the wire, fed from a special pen, tightly round the pins of each component. All the parts needed to construct an electronic circuit are included in a kit, first is the wiring pen itself which has a built-in-wire cutter and carries a reel of wire. The 'breadboard' is an injection moulded board with tapered holes to locate and retain the components. An 'unwrap' tool also acts as an anchor at the start of wiring and may be used to widen the holes of the board. Double-sided adhesive sheets are used to hold down the wires and support insulators where needed. The kit is completed by spring terminals and jacks for power connections and an instruction book which provides guidance for the novice. Such a kit offers an introduction to wiring and circuitry and will find uses in education. BICC-Vero Electronics Ltd, Flanders Road, Hedge End, Southampton SO3 3LG. Tel: 04892 88774.



Raster-scanned c.r.t. for radar

Special applications, such as radar, are catered for by the Scanpack, now available in an enhanced version. This consists of a single unit with all the scanning, video amplifier and e.h.t. generation circuits needed to drive the c.r.t. and scan coil at line rates of up to 70kHz. Input signal handling allows the unit to accept either separate horizontal or vertical sync, combined sync or composite video sync.

A number of different c.r.ts may be used, including round (up to 508mm diameter), rectangular (up to 257mm by 195mm) or square (up to 762mm diagonal). The display tubes can have high resolution with low-voltage focussing, or high brightness and high resolution with high-voltage limiting aperture focus electrodes. Scanpacks are made up to specific requirements and are mounted in the user's own chassis, if required. It is also possible to buy just the unit and scan coil for use with other c.r.ts. Manitron Displays, Sandy Lane, Moston Road, Sandback, Cheshire CW11 9HT. Tel: 0270 764171.

Clamp probe for oscilloscope

Waveforms from a.c. lines can be displayed on an oscilloscope with the help of a Kenwood PC-80 clamp-on probe. Three measuring ranges cover 2mA/mV, 10mA/mV and 100mA/mV; Error is between 3% and 4% depending on the range selected; frequency bandwidth up to 100kHz. Maximum voltage on the cable under test is 500V, while current measuring maximum is up to 120A r.m.s. or 560A peak-to-peak. Thurlby Electronics Ltd, New Road, St Ives, Huntingdon, Cambs PE17 4BG. Tel: 0480 63570.

Battery back-up for rams

Sixteen c-mos ram chips can be connected to the 28-pin controller decoder from Dallas Semiconductor which works in conjunction with a back-up lithium cell. If the supply voltage drops below a programmed level, the battery is automatically connected. It also prevents any further writing to the memory and sets a 'power failure' flag which acts as a signal. Two back-up batteries can be used and the one with the highest voltage supplies the memory.

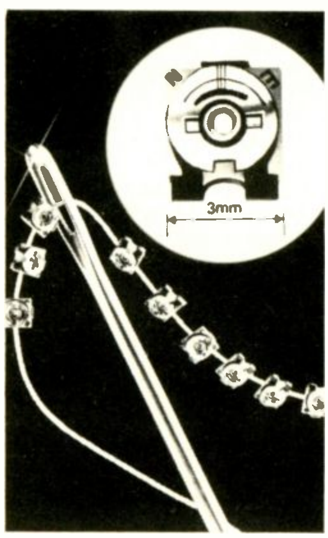
On power up, the DS1212 checks the battery voltage and can also initiate a 'low battery' signal. The combination of DS1212 and a lithium battery can protect c-mos memory for ten years. Joseph Electronics Ltd, 2 The Square, Broad Street, Birmingham B15 1AP. Tel: 021 643 6999.

Precise desolder pump

Solder removal is made easier by the spring-action of Ceka's 6103 pump, in which suction power is variable. Made from glass-filled nylon with a carbon-fibre tip, the pump is conductive and therefore anti-static. Ceka Works Ltd, Pwllheli, Gwynedd, North Wales LL53 5LH. Tel: 0758 612254.

Tiny potentiometers

Surface-mounting potentiometers measure only 3mm by 3.7mm and have resistance values of 100Ω to 2.2MΩ. The CVR-32 series made by Kyocera is compatible with all standard soldering processes. The rotor has been designed to eliminate air gaps and provided maximum wiper contact. This gives the device a linearity to the industry 'B' standard. Temperature coeficient is within 250p.p.m/°C. Rated power is 0.1W at 70°C and operating temperature is from −40°C to +100°C. This is claimed to be the smallest potentiometer in the world. House of Power, Electron House, Gray Avenue, Orpington, Kent BR5 3AN. Tel: 0689 71531.



NEW 8051 DEVELOPMENT CARD

The new Cavendish Automation development card carries a full symbolic Assembler and text editor as well as the MCS-BASIC 52 package. It will allow the user to write applications programmes in either BASIC or Assembler.
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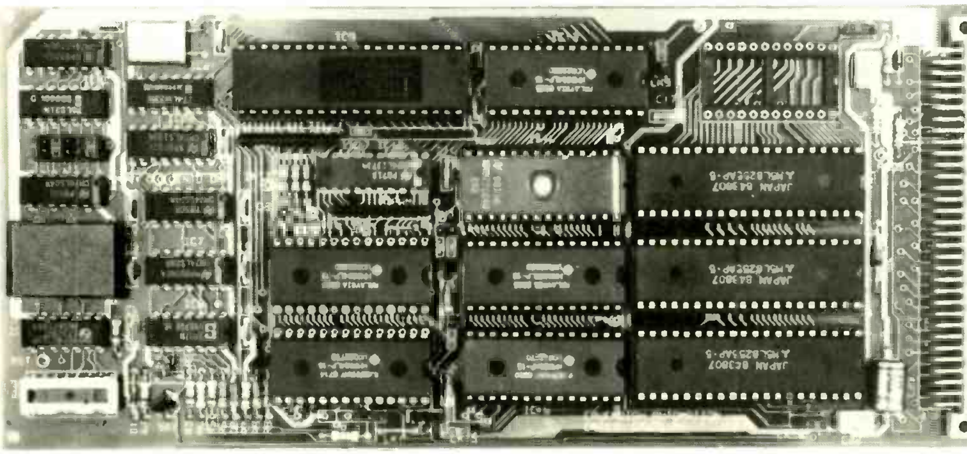

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Vacuum fluorescence is used in a 640 by 400pel display module from Futaba. Like most v.f. systems it provides a blue-green readout but many colours can be achieved through the use of filters.

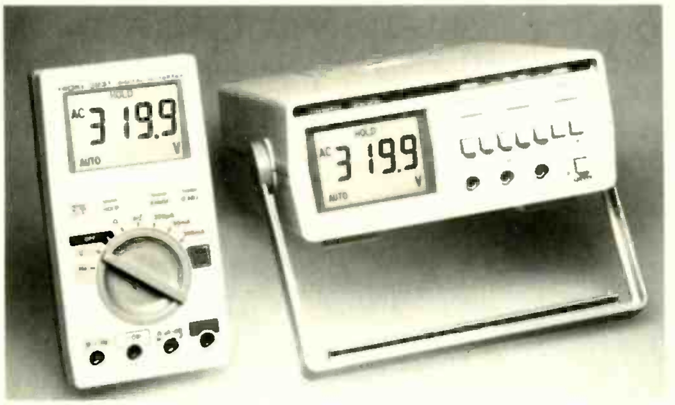
In addition to the display itself, the GP 1004C03B module consists of a display controller and driver, and an optional supply to provide the 134V and 12V lines used to drive the screen. Dots are 0.2 by 0.3mm and are so arranged on a 0.28mm pitch to give high resolution. Regisbrook Group, Units 1 & 2, Suffolk Way, Drayton Road, Abingdon, Oxon OX14 5JY. Tel: 0235 554433.

Laser diodes for high-speed communications

Bit rates in excess of 2Gbit/s can be achieved by Toshiba's distributed feedback (d.f.b.) by the use of diffraction gratings to produce a very narrow spectrum with minimum dispersion. Two wavelengths are provided – 1300nm and 1550nm – to suit the fibre in use, and the solid-state lasers come in a variety of packages for different applications. In addition to the d.f.b. series, Toshiba produces Fabry Perot lasers which are lower in cost and suitable for local-area networks and short-haul applications. The lasers are matched by a series of photodiode detectors, tuned to the same wavelengths. Toshiba (UK) Ltd, Electron Tube and Device Division, Frimley Road, Frimley, Camberley, Surrey GU16 5JJ. Tel: 0276 62222.

Fast a-to-d for instruments

Ultra-fast 15 and 16-bit analogue-to-digital converters from Eikontech have five channels each. They are particularly designed for use on the G-64 bus in electronic instrumentation applications and have a maximum data rate of more than 70k 16 bits words per second. The error is better than ±2 l.s.b. at 15bits and ±4 l.s.b. at 16 bits. Each converter is provided with a single sample-and-hold circuit or with a separate s/h circuit for each channel, allowing all five channels to be sampled simultaneously. Other features include direct memory access and a buffer for 64 data bytes. Triggering is achieved through the G-64 bus or through an external trigger input. Eikontech Ltd, Minalloy House, 18 Regent Street, Sheffield S1 4DA. Tel: 0742 755037.



Big-display d.m.ms

'Largest display currently available' is the boast for the Hioki 3231 digital multimeter. It also counts up to 3199, which gives it a greater measuring range than the more normal 3½ digits available on such meters. A single rotary switch selects the measurement modes and the meter is autoranging. Six direct voltage ranges measure up to 1kV, or 750V for a.c. Current ranges for both a.c. and d.c. go up to 10A and there are a number of resistance ranges, including continuity checks with an audible signal, and diode testing. A low-power ohms test can be used for testing in-circuit components. Frequency measurement is also included; up to 300kHz with 0.1Hz best resolution.

Similar features are available on the 3232 bench meter which adds an output for an external printer to record test results. Universal Instrument Services Ltd, Unit 62, GEC Site, Cambridge Road, Whetstone, Leicester LE8 3LH. Tel: 0533 750123.

Resistors in integrated packages

Having a number of similar resistors in the same package ensures that they are subject to the same environmental conditions and therefore change by the same proportion when subjected to changes in temperature. The TOMC range from Dale-ACI offer thin-film networks with resistors ranging from 100Ω to 100kΩ, made with tolerances of 1%, 0.5%, 0.25% and 0.1%. Resistors within a package are matched to within 0.1% and a temperature coefficient of 25p.p.m/°C is standard.

Resistors are arranged within the surface-mount pack with one end common for all 13 or, 15, or seven or eight isolated resistors, depending on whether the 14 or 16-pin version is used. Dale-ACI Components Ltd, River Park Industrial Estate, Berkhamstead, Herts HP4 1HL. Tel: 04427 72391.

Any waveform you like

An arbitrary function generator does not create waves arbitrarily. It's just a way of saying that it can synthesize waveforms to almost any specification. One from Tektronix, the 5101 combines two instruments; a digital waveform synthesizer and an analogue signal generator. The digital arbitrary generator operates between 1MHz and 5MHz and features two 5K waveforms memories with a 12-bit vertical resolution. This translates as a matrix of over 33 million point (8192 by 4096) with which to plot out a waveform. This may be done manually, entered through the instrument's front panel, or downloaded, through the GPIB, from computer-generated waves which may be produced by mathematical formulae, graphics programs or by digitizing recorded waveforms.

The analogue function generator can produce the usual menu of sine square, and triangular waveforms. These can be between 0.012Hz and 12MHz at amplitudes from 10mV to 9.9V peak-to-peak into 50Ω. The instrument offers a full range of triggering and sweep modes with a.m. and f.m. Internal memory can hold up to 99 front-panel settings in addition to the two waveform memories.

Two versions are available: one is a module that plugs into a Tektronix 'mainframe' and may be used in combination with other instruments to form a complete test system; the other is a stand-alone instrument. Tektronix UK Ltd, Fourth Avenue, Globe Park, Marlow, Bucks SL7 1YD. Tel: 06284 6000.

Programmable active filters

Butterworth and elliptic filters are available in eight-pole high-pass versions. Within the frequency range of each model the corner frequency can be selected by programming the internal logic interface: each of the 878P8 series are tunable over a 256:1 frequency range. Five models are available for each type of filter, covering the ranges 0.1Hz – 25.6Hz to 200Hz – 51.2kHz.

The filters are complete in themselves and require no external components. Filters from Frequency Devices Inc. are available through Lyons Instruments, Hoddesdon, Herts. Tel: 0992 467161

Power diodes for rectifiers

Currents up to 160A can be rectified by SKKD 162 diode modules from Semikron, which are intended for use in power supplies and as line rectifiers for a.c. motor control. Reverse voltage ratings of 800V, 1200V, and 1600V are covered in three versions. Each has an isolated baseplate and several modules are mounted on a single heatsink. Connectors are at the top of the package to make it easy to connect busbars. High temperatures are tolerated. Semikron Ltd, 4 Marshgate Drive, Hertford SG13 7BQ. Tel: 0992 584677.

Graphics software for SC84

A graphics controller for use with the HD64180 processor (as in the SC84 computer from the same designer, John Adams) was described in our May 1987 issue. It offered high-speed and high-resolution images in full colour. Now a reader, Keith Wood, has written a suite of programs for the SC84 with the graphics board. Data to drive the colour monitor is set up by the software, which also enables the creation and editing of images on the display. Mathematical processing of fractal images such as the Mandlebrot set is included, with interactive creation of hue and colour arrangement. Setting up is menu-driven with the menu appearing on the monochrome monitor. A new character set has been designed for high-resolution monitors. These programs are available from the author, Keith Wood, 33 Glan Aber Park, West Derby, Liverpool L12 4YP. He would be grateful for a large stamped/addressed envelope in which he will return further details.

Switchboards in the sky

The days of the 'transparent' comsat transponder are numbered. Payload system designers are looking at various ways of processing signals on board the satellite instead of on the ground. Although this approach means greater complexity in the spacecraft it offers important operational and commercial advantages. Communications capacity can be increased (thus helping to solve the problem of the limited geostationary orbit – see May issue, p.488); greater operational flexibility can be obtained; and, as a result of these two factors, the commercial efficiency of satellite communications can be improved.

Two on-board processing techniques are now being developed. One is the regeneration of digital bit streams, as in terrestrial repeaters, to clean up any pulse waveform distortion introduced by the uplink. This entails demodulation of the received signal in the satellite to recover the baseband digital waveform. The second technique, which seems to have advanced more quickly, is the switching of digital data signals between uplinks and downlinks in large-capacity satellites with multiple spot beams. In other words, any receiving spot beam(s) can be connected within the comsat to any transmitting spot beam(s).

So if there are M receiving beams and N transmitting beams, an on-board switch allows M×N interconnections between these beams. In contrast, the simple 'transparent' comsat only permits a number of straight-through connections set by the number of transponders (M×N) in the spacecraft. Although the communications capacity of each transponder, determined by bandwidth, power and s/n ratio, is no different, the overall effect of introducing switching between uplinks and downlinks is as if the spacecraft were carrying M×N transponders instead M (=N) transponders.

To make this principle work without confusion the individual signals must obviously be kept separate from each other. In practice this separation is achieved by time division of digital signals, using a version of the established time-division multiple access (t.d.m.a.) digital modulation system introduced in 1985 (see April 1987 issue, p.833). This is called satellite switched t.d.m.a. and its first use will be with the new Intelsat VI comsat due to be launched next year (January 1988 issue, pp.25-27). Intelsat VI will carry a microwave switch capable of making interconnections between six beams.

Current development of on-board switches aims to reduce their size and weight by using monolitic integrated circuits. These are made in GaAs to achieve the fast switching speeds necessary for handling high data rates. The general principle of interconnection is based on the matrix, analogous to the crossbar switch of terrestrial telecomms exchanges. For example, NEC has developed a GaAs l.s.i. chip for Intelsat providing a 16×4 switching matrix. It contains 1292 fets and 212 diodes in a monolithic device measuring 3.3×2.8mm.

The GaAs fets not only give high switching speed but also good isolation and a low drive power requirement. The logic circuitry is designed to switch fast enough for bit streams at the Intelsat s.s.t.d.m.a. data rate of 120Mbit/s. Four of these chips, which are housed in 40-lead packages, are to be combined to produce a 16×16 switch matrix working at baseband signal frequencies.

An alternative method, where pulse regeneration is not required, is to do the switching between receivers and transmitters at the transponders' intermediate frequency. This is being pursued by the NTT company for experimental operation on board the Japanese ETS-VI test satellite due to be launched in 1992. Engineers from NTT Electrical Communication Laboratories described their i.f.-band 16×16 switch matrix at the 38th congress of the International Astronautical Federation held in Brighton last year. Using s.s.t.d.m.a., it is intended not only to connect any input to any output but also to connect any input to multiple outputs (distribution) or multiple inputs to any one output (combination).

The matrix switches signals in the i.f. band 900–1100MHz. It is made up of 64 modules, each of which contains two i.c. switches and two i.c. drivers. The basic i.c. switch is a 2×2 matrix (Fig.1a). There are two reasons for this particular arrangement. One is to avoid the r.f. coupling that would occur between input and output lines at cross-over points in a straightforward matrix: an input-output isolation of at least 40dB is required. The second reason is a need for redundancy to achieve good reliability. Each cross-point interconnection switch in the overall matrix in fact uses two of the Fig.1a chips which back up each other and are separately operated by an on-board programmable controller in the s.s.t.d.m.a. system.

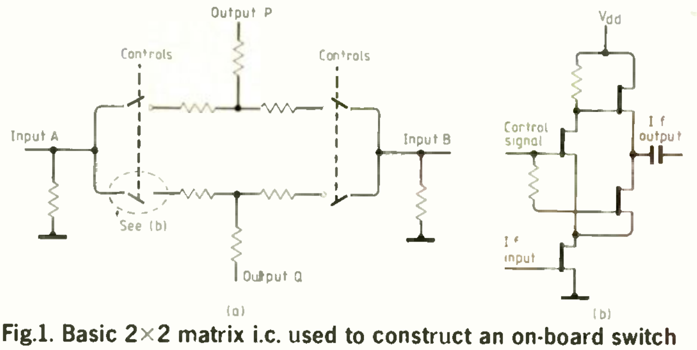


Fig.1. Basic 2×2 matrix i.c. used to construct an on-board switch for interconnecting spot beams in the ETS-VI test satellite: (a) functional diagram of the GaAs matrix i.c.; (b) circuit of each of the four s.p.s.t. switches in the matrix.

Functionally the 2×2 matrix switch i.c. is composed of four single-throw switches. Within the chip, each of the equivalent s.p.s.t. switches is made up of four GaAs fets, two of them forming an i.f. buffer amplifier and the other two performing the on-off switching in response to control signals (Fig.1b). To achieve a high on-to-off ratio and good isolation performance the two buffer amplifier fets are well separated from the two switching fets. Power consumption is kept low in this circuit because in the s.p.s.t. off-state the current is cut off simultaneously in the switching fets and in the buffer amplifier. Altogether the 2×2 matrix of Fig.1a is integrated into a GaAs chip measuring 3.9×2.9mm.

The four s.p.s.t. switches (Fig.1a) are opened and closed by voltages from a further chip (2.7×1.3mm) which integrates four corresponding driver circuits. So the complete switching module mentioned above contains two of these driver chips and two matrix chips. Overall the module package measures 30×21×6mm. It is claimed to have a switching time of less than 10ns and an on-to-off signal ratio of more than 60dB. Insertion gain at 1GHz is about 2dB.

Sixteen of the switch modules are mounted in a four-by-four pattern on a single-plane sub-assembly, then four of these sub-assemblies are piled up to form the complete 16×16 matrix of 64 modules altogether. This final unit measures 270 × 222 × 130mm. Within this box, electrical connections are mechanically arranged to keep the input signal lines in one layer and the output signal lines in another layer, thus separating them physically and avoiding r.f. cross-coupling. Here the signal isolation is claimed to be greater than 40dB.

Initially this kind of on-board switching unit will be used with fixed spot beams. But in later generations of comsats it may well be combined with scanning spot beams, which hop from place to place on the Earth's surface, to give even greater operational flexibility. Such a system will be part of the Advanced Communications Technology Satellite (see January 1987 issue, p.32), though here the switch will be operating at digital baseband frequency.

Telecom 1-C launched

The third French domestic comsat, Telecom 1-C, was one of the two spacecraft successfully launched by an Ariane 3 rocket from Kourou in March this year. It is part of the French national satcoms programme run by Direction Générale des Télécommunications (DGT), the telecomms operating unit of the French PTT. Placed in a geostationary slot at 3°E, this new spacecraft carries on the telecommunication and broadcast signal distribution functions started by Telecom 1-A (stationed at 8°W in 1984) and Telecom 1-B (placed at 5°W in 1985). Its arrival is fortunate, as the 1-B spacecraft has now gone out of control.

These Telecom satellites have Ku-band spot beams covering the whole of France (and parts of adjacent countries) and also semi-global beams providing C-band communications with French overseas territories and nearby areas. The last-mentioned coverage includes the eastern seaboards of Canada and the USA, the entire Caribbean area and the northern part of South America. Like its predecessors, Telecom 1-C carries ten 20W civil transponders. Six of these operate in Ku band (downlinks 12.5–12.75GHz) and four in C band (downlinks 3.7–4GHz).

The telecomms network carries both low-speed and high-speed digital data (2.4kbit/s to 2Mbit/s) and uses about 320 small earth terminals with 3.5 metre antenna dishes. Network access is provided through a demand-assigned t.d.m.a. system. Both sound and television broadcast signals are distributed. In addition Telecom 1-C has a military communications payload working at s.h.f. with 8GHz uplinks and 7GHz downlinks.

All these spacecraft have been built for DGT by a European group of contractors which includes the UK's British Aerospace.

The second satellite launched on the same Ariane 3 rocket was the American Spacenet III domestic comsat. Built by RCA Astro Electronics, this carries twelve 72MHz t.w.t. transponders, six for C band and six for Ku band, plus twelve 36MHz solid-state C-band transponders.

● TV-Sat 1, the German direct broadcasting satellite launched on the previous Ariane flight, V20, has now been written off as a complete loss. One of its two solar arrays failed to unfold properly and obstructed one of the antennas. Cost of this failure to the owners, the Deutsche Bundespost, is estimated as about £100 million.

Seminar on intersatellite links

Results of current studies on both intersatellite and inter-orbit communication links will be presented by European aerospace firms at a seminar to be held at the Royal Garden Hotel, London, 29-30 June. Speakers from international space organizations will cover the technology, including microwave and optical systems, and there will be an associated exhibition.

The event is organized by the independent r&d organization ERA Technology Ltd, Cleeve Road, Leatherhead, Surrey KT22 7SA; tel: 0372-374151. Contact: Laura Christie, ext. 2290 or 2488.

Nigeria joins Inmarsat

The latest country to become a member of Inmarsat – actually the sixth African country – is Nigeria. Represented by Nigerian Telecommunications Ltd, it already has two ships using the Inmarsat system and generates considerable shore-to-ship traffic. The international co-operative now has a total of 54 member countries.

Satellite solarium

As part of their pre-launch testing, all satellites have to be subject to simulated space conditions to see if they will stand up to the rigours of this harsh environment. Broadly speaking, it is a high vacuum, with temperatures ranging from –200°C to +100°C.

ESA's new scientific satellite Hipparcos has recently been taking this treatment in a large space simulator at the agency's European Space Research and Technology Centre (ESTEC), Noordwijk, in the Netherlands. This simulator is claimed to contain the world's most powerful artificial sun. Inside a cylindrical vacuum chamber, a 7.2 metre mirror built up from hexagonal elements directs radiation from a battery of xenon lamps on to the spacecraft. Mechnical positioning equipment orientates and moves the satellite to simulate as closely as possible to the angle at which the sun's rays will strike the spacecraft in a given orbit.

Hipparcos, named after the ancient Greek astronomer, is a geostationary satellite designed for astrometry – making astronomical measurements. It will be used for accurately determining the positions of stars and their motions in space. ESA says that, over the mission lifetime of 2½ years, about 120,000 stars will be measured, to an accuracy of 0.002 of a second of arc.

Satellite Systems is written by Tom Ivall

Radio engineering terms in satellite links

Field strength

The received power P_R can be calculated from the power flux density at the earth station if this is known. It is common practice for satellite operators to specify it by contours in the satellite's footprint. From the p.f.d. in dBW/m^2 and the area in metres of the receiving antenna reflector the theoretical incident power can be calculated. The actual received power, however, depends on the gain (including efficiency) of this antenna.

Field strength in volts per metre can be calculated from power density values on the analogous Ohm's law principle of $V^2 = RP$. In the satellite case the V here is analogous to the field strength E (volts/metre), the R is analogous to the *characteristic impedance of free space* Z_0 (=376.6Ω), while the P is analogous to the radiated power (e.i.r.p.). The relationship is

$$E^2 = \frac{Z_0 \times (\text{e.i.r.p.})}{4\pi r^2}$$

where E is field strength (V/m), e.i.r.p. is power (W) and r is the distance between satellite and receiver (m). This takes account of the spreading loss but not the other losses mentioned above.

The same general principle involving Z_0 is used to convert received p.f.d. into field strength. Here

$$E^2 = Z_0 \times (\text{p.f.d.})$$

where E and Z_0 are as defined above and p.f.d. is in W/m^2. As an example, if the p.f.d. is –103dBW/m^2 (=2×10^{-10}W/m^2) as specified for beam centre under the WARC 1977 d.b.s. plan, then E=137μV/m. To calculate directly in dBW, a useful formula is

$$E\,\text{dB}(1\mu\text{V/m}) = \text{p.f.d. dB}(1\text{W/m}^2) + 145.76$$

remembering that the decibels on the left hand side of this equation represent a voltage ratio and not a power ratio.

Noise power

The channel capacity of the satellite downlink is, of course, partly dependent on the noise power in the link. Noise power is normally expressed as *noise temperature* on the absolute scale, to which it is proportional – that is, the temperature in K of a resistor that would generate the same thermal noise power per unit bandwidth as the noise power produced by the actual device concerned (e.g. a receiving antenna). Standard noise temperature is taken as 290K, as this corresponds to normal room temperature of 17°C.

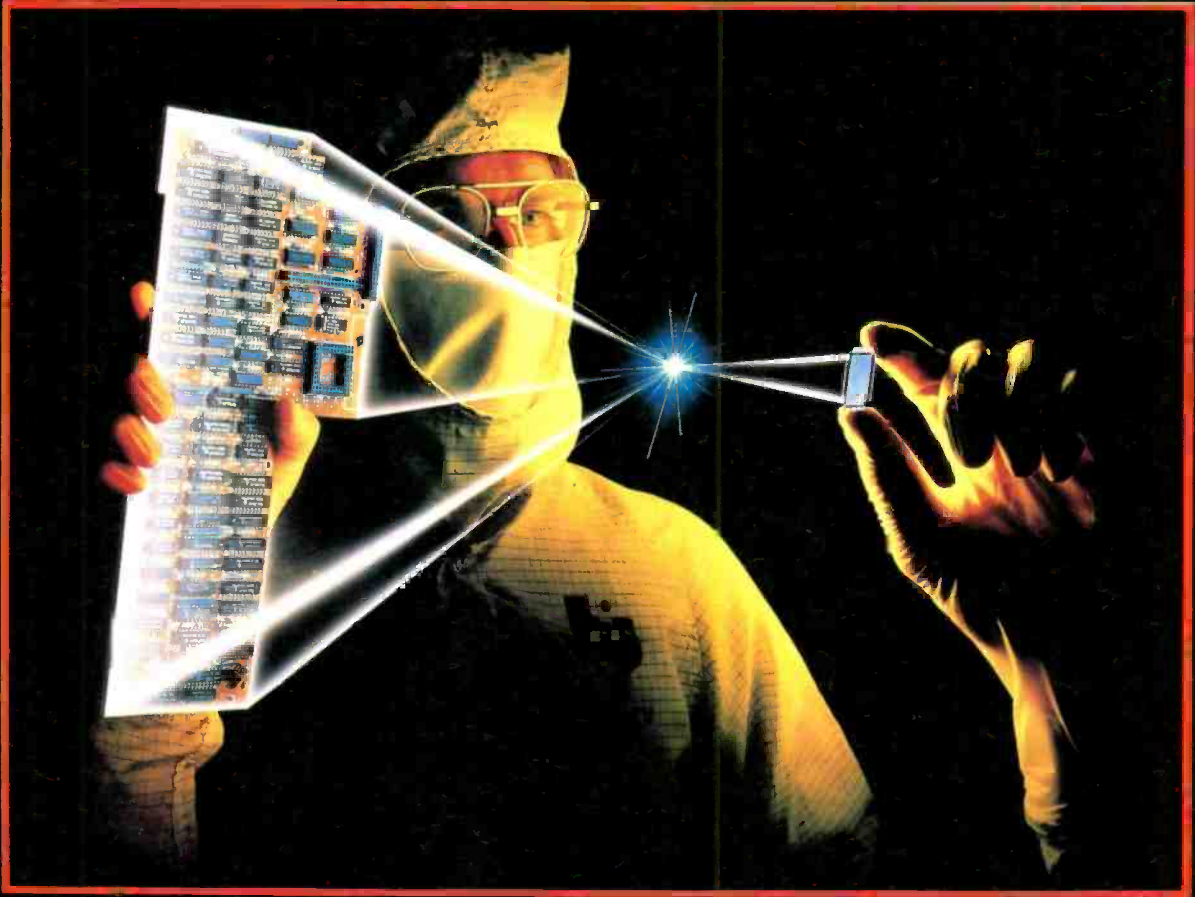
Noise power N at some point in a communications link can be calculated from the formula: $N = kTB$, where N is power in watts, T is noise temperature in K, B is the *noise bandwidth* of the link in Hz and k is Boltzmann's constant. The expression kTB has the dimensions of power because, although Boltzmann's constant is a number (1.38×10^{-23}) of joules per kelvin (J/K), when this is multiplied by temperature in K it becomes an energy value in J and when, in turn, this is multiplied by frequency bandwidth (1/s) it becomes a value in J/s, which is another way of expressing power in W.

The expression $N = kTB$ indicates that the noise power in a channel is also proportional to the bandwidth, described for this purpose as the noise bandwidth. As mentioned above, communications engineers express this bandwidth in dB relative to 1Hz, so a noise bandwidth of 27 MHz = 74.3dBHz.

To be continued

JUNE 1988

INDUSTRY INSIGHT



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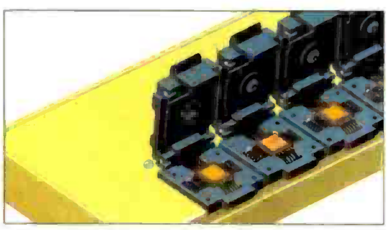

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UK SEMICONDUCTOR LIFELINE?

A new £250 million, five-year research plan is taking shape to provide a range of advanced semiconductor technologies, design tools and techniques to satisfy UK electronics systems company needs into the 1990s.

The collaborative research programmes of Alvey and Esprit have provided a sound base of technology and computer-aided design capability that was badly needed to keep our firms competitive. With these programmes due to end early next year, plans are well advanced for an ambitous new programme of research and development aimed at technologies with minimum dimensions as small as 0.3 microns.

The new plan, Silicon Towards 2000, describes for the first time the targets for UK efforts in this area viewed within the context of Europe. The plan proposes a national programme together with UK involvement in the major European Esprit II initiative scheduled to begin within the next year. Funding for Esprit II amounts to £2.2 billion of which the European Commission will provide half. In fact, implementation of the European aspects of the plan has already started with the submission of proposals for the first round of Esprit II in April this year. The plan will also be bidding for UK Government support under the new national i.t. research programme being run jointly by the DTI's Information Engineering Directorate and the Science and Engineering Research Council.

Workplans have been prepared for three major i.t. areas: systems architectures, systems engineering and devices (including Silicon Towards 2000), and these are currently being refined prior to final issue of a call for proposals, due this month. The DTI has allocated £29 million over three years in support of the new programme, with SERC earmarking £55 million over five years for academic work in the same area, mainly in collaboration with industry.

Our semiconductor industry is smaller relative to the major commodity suppliers than it was at the beginning of the decade. However, with its important European research links and improved efficiency, it is well positioned for strong growth to take full advantage of the Single European Market.

Silicon Towards 2000 is intended to provide the technological base on which this growth will be based. The life of our industry may depend upon it.

Robert J Morland is Director of Devices, Information Engineering Directorate, Department of Trade and Industry, on secondment from PA Technology.

INSIDE

Cover – Breadboarding in Silicon. With direct write-on-silicon e-beam facilities – offered for TI's one-micron gate arrays next year – the cost and time involved in masking is eliminated.

THE 1990 APPROACH TO CUSTOM SILICON

It is the obligation of every conscientious design engineer to evaluate the use of custom silicon as a means of attaining improved product specifications. Those who seize the opportunity early will be among the first to experience the benefit of more innovative and competitive products; it might not be as difficult as you think, says Chris Gare.

Custom silicon, or application-specific integrated circuits as they have become commonly known, is not a new technological marvel to arrive in recent years. The basic technology dates back to the earliest days of the semiconductor industry when many multinational companies saw the benefits of integrating systems into silicon. The widespread use of this design approach was cut short prematurely by the advent of the microprocessor which enabled an approach that provided flexibility, high functionality and the ability to effortlessly redesign up to the day of product release.

Custom silicon for most engineers was relegated to a secondary position whose use was only chosen when a microprocessor solution placed severe constraints on a product specification or when the applications performance demanded the use of integration. Today, even though the benefits of using asics have been widely promoted and obviously rank highly on the wish list of any equipment specification, fewer than 30% of companies in the UK have taken the plunge and used them.* The reasons for this are intrinsic in the technology itself and how it is marketed by semiconductor vendors.

What are the factors that have held back the widespread use of custom silicon? Firstly, the detailed knowledge essential to design integrated circuits only resided within the semiconductor supplier community itself. It is almost considered to be a 'black art' with only a few engineers being given the opportunity to learn this exacting trade. Even now it is commonly estimated that there are only 10,000 design engineers in the world capable of designing a chip from scratch. Good i.c. design engineers require several years of experience before they are capable of designing chips on a standalone basis.

Secondly, the computer-aided design tools used to design chips were really quite crude. Chips were designed manually with each transistor and interconnect string being laid down by hand on a graphic editor. This led to development times that were measured not only in man-years but in millions of dollars as well. As a systems manufacturer, if your products had potential sales in the high thousands and could support sufficient margin for such high development costs then you could afford to become involved with custom chips. If not, access to the technology was practically denied.

Users and vendors of custom silicon came up with radically different approaches to providing lower cost solutions. Users, that is large users, invested in in-house technology to the extent of not only hiring experienced i.c. design engineers but also building foundries (the industry name for i.c. manufacturing factories) for themselves. For example, nearly every single household-name Japanese electronics corporation owns a fabrication plant to support internal consumption. The vendor approach, which was the epitome of compromise, was the development of the 'gate-array' concept.

The gate array was a singular concept that endeavoured to rationalise the disparate requirements of suppliers and users. All major semiconductor vendors are orientated to producing standard parts in high volume measured in hundreds of thousands. The problem with most custom silicon designs however is that they are mainly low-volume in nature as they are associated with a single customer. This is not the sort of product that motivates production directors of traditional semiconductor suppliers!

With gate array technology, complete wafers are preprocessed with an array of unconnected gates separated by wiring channels. When a user completes a design the vendor takes these 'base wafers' off the shelf and adds the final metallization layers that define the function of the chip i.e. personalise it. The gate array is a compromise nevertheless and in itself not capable of reducing the cost barriers to a sufficient level to encourage the widespread use of custom silicon. Let us take a look as to why this should be so.

The need for masks

The traditional method of making integrated circuits is to use photolithography. Each layer of an i.c. is built up by placing a film of photoresist on the surface and exposing it by illuminating it with u.v. light via a mask that is stepped over the whole wafer surface. The unexposed resist is washed away and the exposed surface etched. A complete i.c. consists of up to thirteen of these masks. For a gate array, where only final metal layers need to be formed to personalize the chip, only one to four masks are required. The making of these masks is an expensive process, close to $2,000 a mask.

The above cost and the underlying manufacturing technology require that a significant non-recurring expense is needed to finance a vendor tooling up prior to a

*According to a 1987 DTI study, see page 593 footnote production run. More often than not the vendor demands a significant production order before doing so. A typical UK manufacturer who has neither the cash nor a sufficient production run to interest the vendor has little chance of getting past this first step.

The design process

The nature of the gate array has placed severe constraints on the way the design process is accomplished. Whereas the development of microprocessor-based systems has passed completely to the electronics engineer through the emergence of the desk-top microprocessor development system and in-circuit emulation; this has not happened with custom silicon designs. The reason is inherent in the structure of gate array itself: columns of uncommitted gates interdigitated by wiring channels. These wiring channels are of finite width, and as such, present a challenge to any automatic place-and-route software.

A gate array 'p. and r.' program needs a powerful mainframe computer to handle the complexities of routing a chip. This is because the fixed-width wiring channels can only accommodate so many wires across its width and once this limit is reached the router needs to find an alternate path, possibly via another layer. If this is not possible and an alternate path is not located, the routing needs to be completed through manual intervention. It is only after a chip is laid out that an accurate simulation of chip performance can be achieved because the precise loading of each individual gate output is needed before accurate delay predictions can be calculated.

The accepted design methodology for gate arrays is that the customer only undertakes the entering of the schematic on the cad system and the pre-layout functional simulation of the design. This schematic database and the simulation vector table is then shipped to the gate array vendor who lays out the chip and conducts the post-layout timing simulation. The results are then shipped back to the customer who

SECRET OF DESK-TOP DESIGN

A new approach to the design of custom silicon is afforded by writing all layers of a custom chip rather than just the final metalization layers as with a gate array. This provides the assurance that all designs can be 100% automatically routed on the designer's desk-top cad system. Once layout has been accomplished, full back-annotated simulation of the design can be run to ensure that the design meets required timing specifications. Back annotation means that actual interconnect and fan-in loading data is fed back to the simulator so the simulation is as near 'real-life' as possible. The diagram on page 590 shows the particular software programs in the Solo 1000 package a design engineer needs to run to produce a design database. The first step is to enter the schematic diagram into the editor, Draft. The logic diagram is then automatically converted to a high-level descriptive language, Model, which drives the place and route programs.

The first of these programs positions individual transistors as required by the design in a columnar fashion while the second determines how they are interconnected. The Draw program enables a paper plot to be produced, page 590. The next task undertaken is functional simulation using actual gate-loading data supplied by the place and route programs run earlier. The Exert simulator is driven by a set of vectors created by the designer which at a later stage are used again to test the prototypes and production parts. At this stage the designer has complete freedom to not only correct discovered errors but change the basic design as required. Before the design is sent to be manufactured the Design Manager ensures that all the design steps have been correctly run and that the design will fit in the selected package. Using this design methodology a typical small design consisting of 2,000 gates should take only between one and four weeks to complete.

DIRECT WRITE-ON-WAFER WITH E-BEAM TECHNOLOGY

Directly writing patterns onto wafers is a technology that introduces a new degree of freedom into the manufacturer of custom silicon. Removing the dependence on masks allows a manufacturer more freedom to place multiple designs on a wafer and to specialise in the production of small quantities of parts. All the steps of producing an integrated circuit are the same as conventional techniques except that instead of placing a mask over an optical resist to produce a layer image on the wafer, a resist that is sensitive to electrons is used. A beam of high-energy electrons then writes the design direct on the resist itself.

The e-beam machine as used by ES2, opposite, is specified to produce features of minimum size 0.5 micron but features down to 0.1 micron have been regularly achieved. There is no limit to die size other than what is considered to be acceptable time to process the design data.

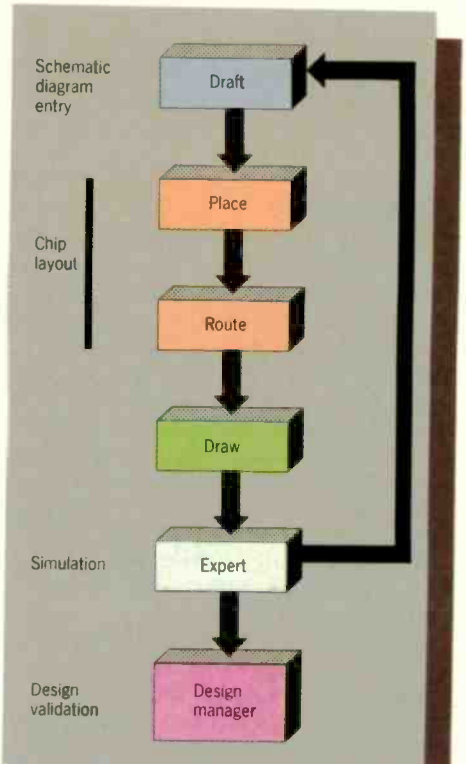
On receipt of a design database from a customer it is 'fractured' on a pre-processor computer. This procedure entails the breaking up of complete design elements into fundamental polygons. The fractured design is then submitted to the e-beam computer that then proceeds to load a wafer covered with a thin coating of e-beam resist. The computer then controls the writing of a complete layer of the design by a narrow electron beam scanning the wafer at high speed. Once one design layer is completed the e-beam goes on to write similar design layers over the whole surface of the wafer or alternatively, if more than one design is being placed on the wafer, over a section. The wafer is then removed and etched in the conventional manner ready to go through the complete cycle repeatedly until all the layers of a design have been built up.

corrects any discovered faults in the design.

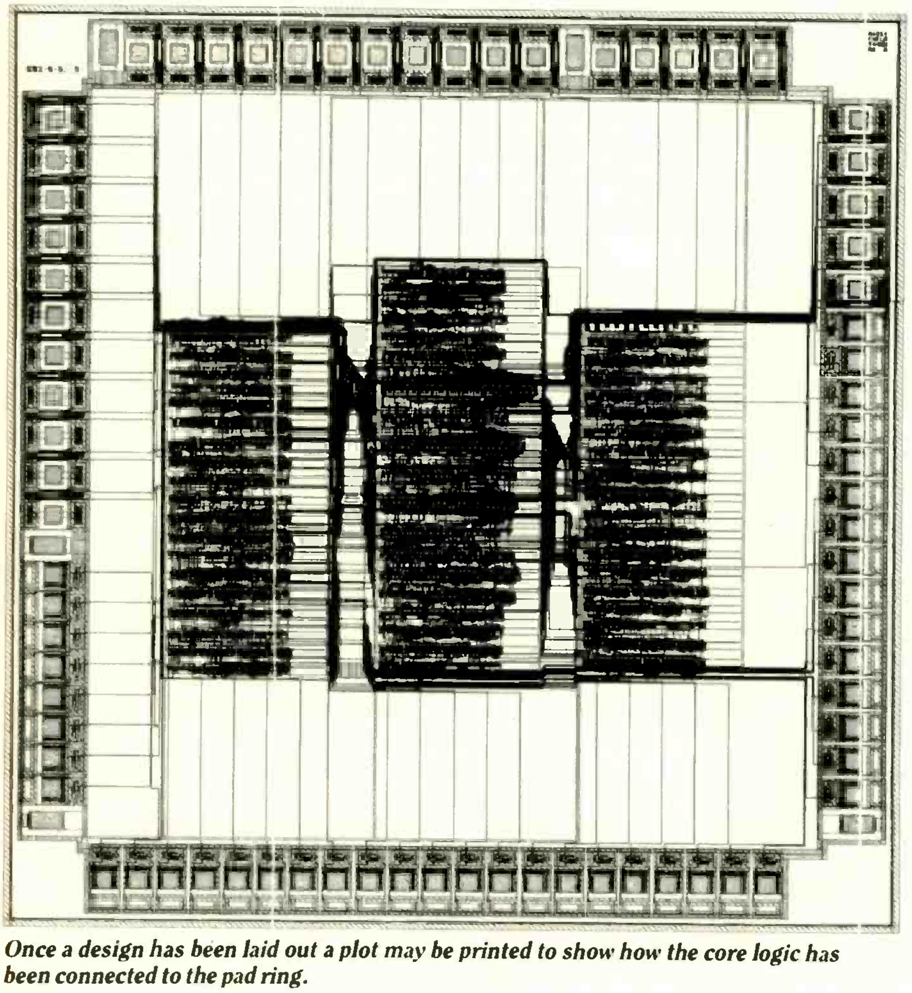
The hitch is that most vendors, because of the expensive computer needed, need to set high charges for this job. Also, the time taken to complete this cycle can be lengthy and can as a rule be measured in weeks rather than days. Design iterations are definitely frowned upon by vendors and the users' bank manager alike!

The alternate approach

As gate arrays have the seeds of their own limitations embedded in the technology a different approach was required if the use of asics was to be made available to a wider base of users. The Shortland report indicates that the principal reasons why so few manufacturers are benefiting from the use of asics are:



By using a desk-top design system engineers can layout chips on their desk – formerly only performed by semiconductor vendors. See panel on page 589.



Once a design has been laid out a plot may be printed to show how the core logic has been connected to the pad ring.

- design costs and up-front payments are too high
- they require small quantity production runs
- no application for custom silicon
- no second-source for chips.

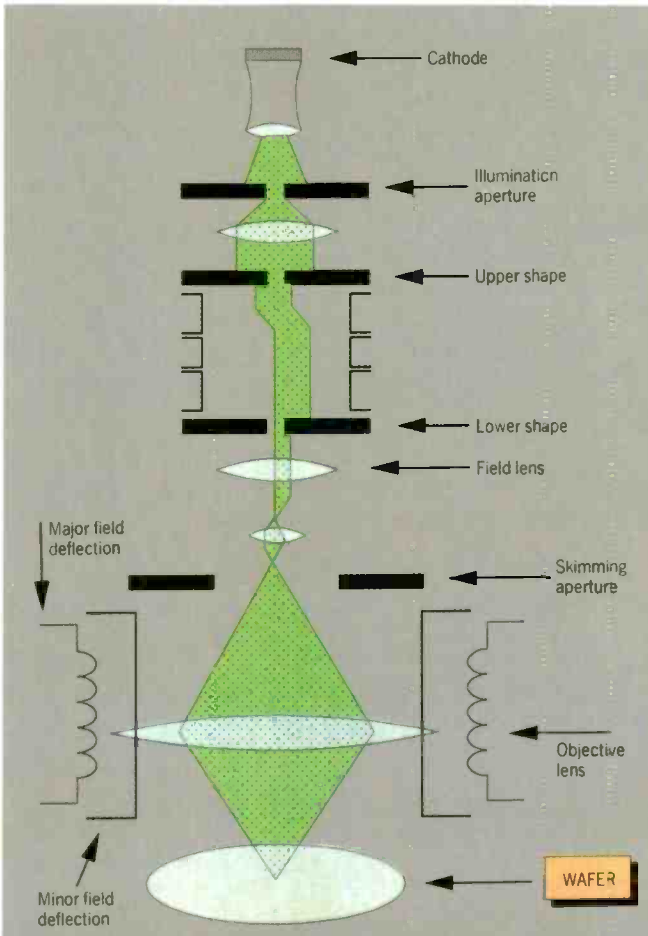
It is from recognising the deficiencies in the current technologies that European Silicon Structures was formed. In several innovative ways, the company took a radical position in a mainly traditional market and put together an integrated software and manufacturing policy that could provide a practical means of reducing the barriers to using custom silicon. These principal innovations lie in two areas, firstly, i.c. design tools that are analogous to the microprocessor development system, and secondly the removal of the need to use masks by writing direct onto the silicon wafer by means of an electron beam.

Desk-top design approach to custom silicon

If the designer of a microprocessor-based system needed to dispatch every design to a semiconductor vendor to verify whether a program has been correctly coded, the wide-scale use of microprocessors would have been severely curtailed. This is the very situation engineers have to contend with now if they want to utilise custom silicon. Although in-circuit emulation is not available for custom silicon designs it is possible to complete the *whole* design of a custom chip on an engineer's desk if a different approach is taken.

The principal reason preventing the layout of chips on smaller desk-top machines is the computing power required to support gate array router software. If the manufacturing process encompasses the writing of *all* layers, when the router runs out of space in a clogged channel instead of eventually abandoning the run the software can stop, increase the width of the channel, and reroute that wire in the channel. In this way it is possible to guarantee 100% routing on a small desk-top workstation. A design engineer can enter the schematic diagram into a schematic editor, carry out an initial functional simulation (without real loading data), lay out the chip and resimulate the design with real loading data.

Once the logic diagram has been entered the complete layout cycle can be executed in hours rather than days or weeks. The principal benefit of this style of design is flexibility. In the same way the use of an in-circuit-emulator in conjunction with a native compiler or assembly code editor allows more or less instant redesign, chip logic can be changed, logic or wiring errors can be corrected, extra or fewer pads selected or aspect ratios of the final chip modified just as quickly. All this without indeterminate external computer charges.



This cross-section of the Aeble 150 shows the 0.5 micron beam focused in a similar manner to that of an electron microscope.

In coming years the use of custom silicon to enhance the functionality and individuality of electronic products will become widespread as barriers to using the technology are removed.

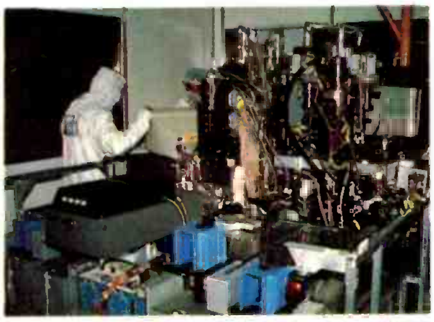
The ES2 Fab – an alternative approach

An innovative method of manufacturing was needed if ES2 was to support the criteria by which the widescale use of custom silicon will be ensured in coming years. These are the ability to support prototype production without an undertaking from the customer that the design will go to high-volume production. These objectives can only be met by the removal of the straightjacket caused by the need to use masks. Electron beam write-on-wafer is probably the only viable technology for accomplishing this.

The Aeble 150 e-beam machine used by ES2 is manufactured by Perkin Elmer and is essentially an inverted electron microscope. A very narrow beam of electrons, of less than 1 micron across, writes the pattern of polygons into an e-beam-sensitive photoresist without the intervention of a mask. The only limit to maximum die size the maximum number of different designs on a wafer is the software preprocessing time needed prior to physically writing a wafer.

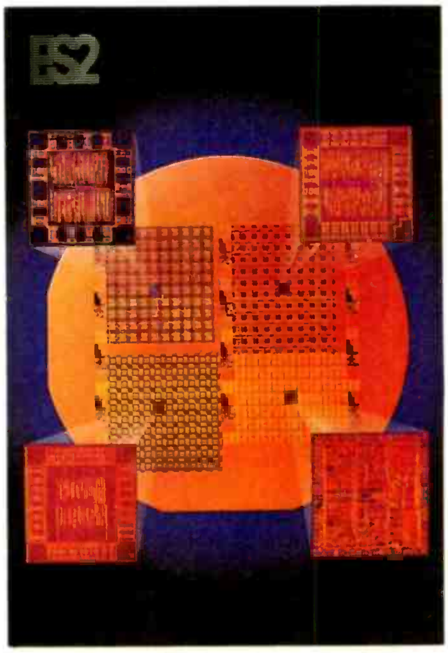
The use of e-beam technology is not the only change required of a fab dedicated to small volume production. The conventional fab is oriented to processing many wafers in an individual production run, as many as 50. For example, if a wafer contains a die of 3 by 3mm this means that approximately 940 die per wafer could be expected to funciton after yield considerations; this means a total of over 47,000 die per run! A fab that is dedicated to supplying low-volume must be able to run as few as two wafers per lot. The ES2 fab is operated in this manner and actually assigns a technician to see an individual wafer through the complete production cycle to ensure that the design will be right first time.

Chris Gare, F.I.E.E., is corporate marketing manager at European Silicon Structures, Bracknell, Tel 0344 52 52 52.



Perkin Elmer's Aeble 150 electron beam machine is capable of writing designs direct onto a wafer without the need of a mask.

May's front cover showed 28 2 micron designs on one ES2 wafer.



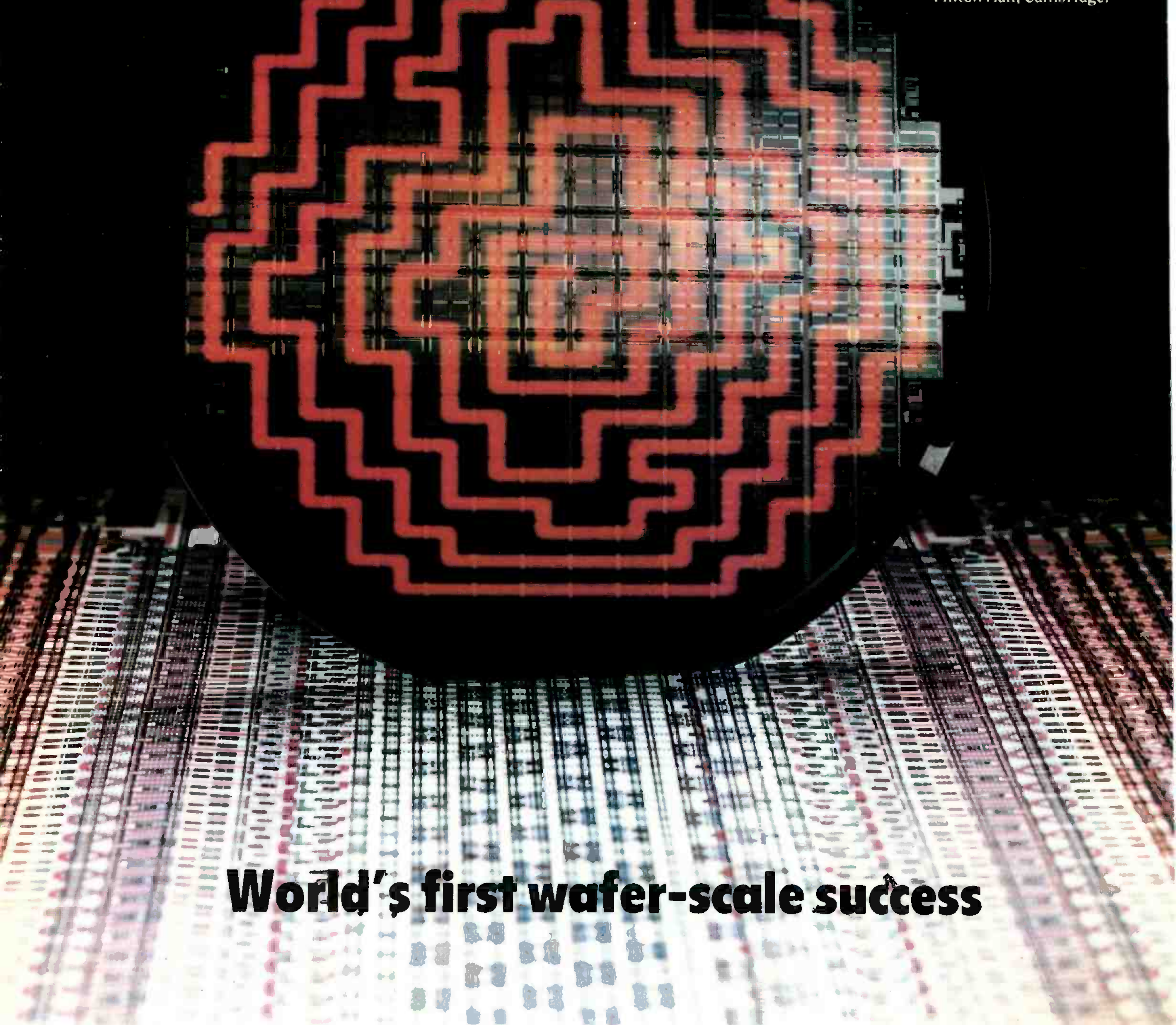
It is now possible to write more than one individual design onto a wafer, which enables semiconductor vendors to support small production runs.

WHATEVER HAPPENED TO WAFER SCALE?

Pictured here is the first product to use what in the wafer scale community has become known as the Catt Spiral. It is an array of devices on one 6in wafer connected in such a way as to eliminate faulty devices and is the only known successful approach to wafer-scale integration. Both Texas and Trilogy in the US abandoned work in this area after huge amounts of money had been spent. British company Sinclair Research came close to marketing a half-megabyte memory based on a 4in wafer around three years ago but the w.s.i. work was transferred to Anamartic, who are believed to be about to market a product with at least 20Mbyte of memory. A stack of ten such wafers would form a memory – a 'solid state disc' – of 200Mbyte in a space smaller than a floppy disc drive, yet with an access time of the order of 100μs.

And what looks to be a 'first' for Britain's semiconductor industry is based on technology first described in this journal. Though patented as long ago as 1972 by Ivor Catt, the Catt Spiral algorithm, as it has since become known, was first disclosed in 1981 in an article entitled simply 'Wafer scale integration' (July issue) describing his spiral – an algorithm for producing a fault-tolerant wafer array of perfect 'chips' from an imperfect wafer. Catt had previously tried to interest UK learned journals in the work, but they all rejected his paper.

The photograph is a superposition of a wafer and c.r.t. tracing of the algorithm, based on an idea by Neil MacDonald and Gordon Neish of Anamartic Ltd, of Milton Hall, Cambridge.



World's first wafer-scale success

SEMICONDUCTORS

CUSTOM SILICON NOW

By continuing to design using only standard parts in increasingly obsolescent configurations, and thus failing to exploit the latest asic technologies, the majority of UK small/medium electronics companies are losing their competitive edge against foreign asic users.

This potentially damaging asic gap between small/medium British companies and their foreign competitors has now spurred the UK's Department of Trade and Industry to launch a new nationwide awareness campaign that will stress the vital new factor in current asic technologies: their accessibility to even the smallest electronics manufacturing company. In spite of all the publicity given to recent developments in programmable logic,devices, gate arrays, standard-cell designs and full-custom chip production, the DTI say a worryingly high proportion of British electronics companies still have not 'got the message' about these application-specific integrated circuits.

According to computer-aided engineering consultant Mike Shortland, who headed DTI research into the subject, what is needed is a way of convincing companies on an individual basis – especially small firms – that custom-i.c. technology has something to offer and that it is relevant to their businesses. "Detailed research we carried out a year ago showed that over 70% of all small/medium British electronics companies were still not aware of this relevance then" says Shortland "and more recent research has shown just as surprisingly that the situation has not materially changed."

The use of application-specific i.cs in electronics design has been an essentially big-company preoccupation. While the largest British electronics companies – those with >500-employee have almost all been intensive users of asics for up to a decade, only 60% of medium-sized companies and less than 25% of small companies (<200 employees) have yet begun to exploit even the simplest forms of asic, such as programmable logic arrays.

This dominance of the British asic market led by large companies has not been unduly worrying. In fact, the readiness of the British majors to adopt asic-based designs has so far been responsible for giving the UK the clear European lead in their exploitation; Dataquest for instance forecasting almost 20% of this year UK consumption of integrated circuits as being in asic form, as opposed to only 10% worldwide.

The DTI's new custom silicon campaign should benefit the asic supply industry, as well as the 3000 potential users in manufacturing industry.

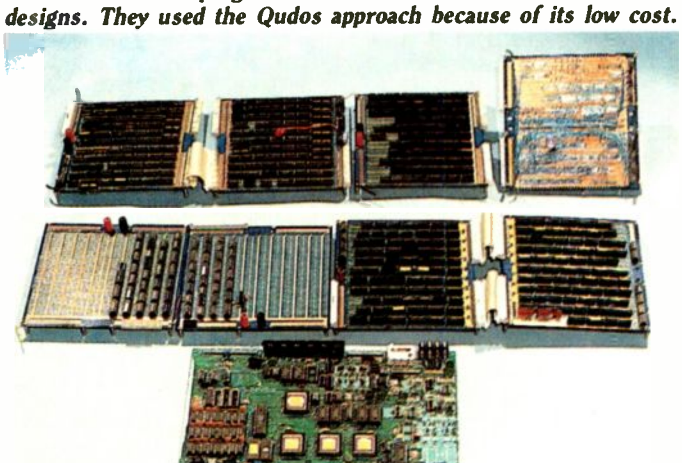
Nevertheless, this commendable UK lead in taking advantage of asic technology is now showing signs of fading, as other countries prove themselves better at promoting the take-up of asic technology by companies of all sizes. Several countries with the fastest-growing rates of asic usage have already implemented government-sponsored asic-promotion schemes, stressing the way in which the latest technologies are just as appropriate to the smaller companies as to their larger rivals.

In fact, as research sponsored by the DTI among British companies shows*, company size need no longer be a barrier to the successful use of custom i.cs, even the most complex devices. For example, the 30% of small/medium companies who were already using asics reported a generally marked level of success in doing so, covering everything from typical savings of 10 to 40% of manufacturing costs to smaller physical size of products (e.g. one p.c.b. instead of four) and higher performance (e.g. ten times the speed of a random-logic alternative). Enhanced reliability, shortened design cycles, increased security of proprietary designs, and the ability of originate whole new product concepts were also commonly reported.

These small-company users also proved successful at exploiting the full range of 'technologies'. While the most commonly used devices are the relatively simple p.l.as as would be expected (used by 60% of the small companies, 80% of medium size), the more complex gate-array devices were used almost as frequently (50% of small users, 60% of medium). Even the most complex standard-cell and full-custom asics proved to be relatively widely used even by the small companies – 25% of which used cell-based devices and no less than 20% full custom.

As these figures show, the idea that small electronics companies simply do not have

The photograph from Flare Technology shows how a very large breadboard can be reduced to a manageable size by using custom chips. The bottom card is the equivalent of the eight above. Flare, all ex-Sinclair employees, designed two custom processors into this home computer to give it natural graphics and quality sound. Flare are hoping to interest manufacturers in this and other designs. They used the Qudos approach because of its low cost.



*UK Custom Integrated Circuit Market: The User Company Perspective. Michael Shortland Associates, Guildford, 1987. £15.

the technological background to exploit current asic technology just does not hold water. Nor do the other reasons generally put forward by the non-users among the small/medium companies as explanations why the new 'custom-silicon' technologies are not for them – high engineering costs, low production volumes, etc.

These arguments for not using asics are directly contradicted by the research finding that the markets, products and size of the non-user companies are not dissimilar from those of the succesful user companies. About the only difference that could be found in the objective circumstances of the user and non-user companies was the proportion of graduate designers employed in each – over 80% of the user companies employed graduates for over half of their designer posts, compared with under 50% of the non-user companies.

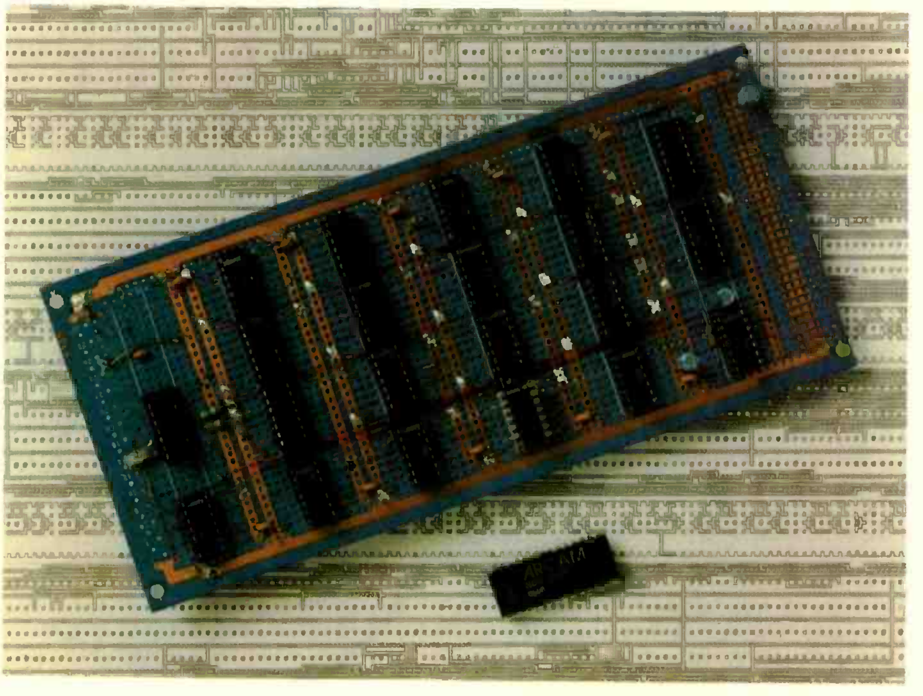
As this factor suggests, the real difference between user and non-user companies maybe more one of in-company attitudes and awareness than of external factors. In fact, even companies operating in similar ways in similar markets were shown to have very different attitudes about the relevance of asics. These included the fact that the asic users were more than twice as likely as the non-users to be able to identify the extent to which their foreign competitors were moving over to asic-based designs. "A dangerous complacency among non-users" the report notes.

The survey concluded that most of the non-user companies are out of touch with recent developments in custom-i.c. supply, and are basing their opinions on obsolete information. In particular, many have preconceived and outmoded ideas of asic economics, and when discussing their potential use of asics with suppliers lack the ability to put over their requirements in terms that the supplier can act on.

Reinforcing this conclusion of a lack of up-to-date awareness, the survey found that 80% of the asic non-users responded that they would "welcome and exploit" a new DTI awareness scheme. On the other hand, neither the non-users nor their asic-using counterparts put much emphasis on the importance of other government initiatives such as support grants in influencing their attitudes to custom silicon. Concentrating resources on improving awareness has therefore been the key aim of the DTI's new initiative 'Custom Silicon Now'.

The campaign will benefit most directly all the 3000-odd potential users of asics among the small/medium electronics manufacturers, but beyond this it also aims to benefit the rest of the UK electronics industry, including the large companies who rely on their smaller counterparts for a great deal of subcontracted design and manufacturing.

Perhaps most of all, it should also benefit the asic supply industry, for which the smaller companies offer a potentially very



CAMPAIGN DETAILS

Aimed at providing a quick but comprehensive update on all aspects of current asic technolgy, the DTI's Custom Silicon Now! seminars tour the UK over the next two months. Directors, managers and other senior personnel of small and medium-sized companies will be given three seminar sessions and the opportunity to talk to specialist consultants and suppliers of asic devices and support systems and services, together with seminar material, suppliers guide, information on training and finance, and a video cassette.

Dates and venues

London – Queen Elizabeth 2 Conference Centre, Westminster	25 May
Peterborough – Moat House Hotel	7 June
Edinburgh – Caledonian Hotel	14 June
Manchester – Holiday Inn Crowne Plaza Midland Hotel	21 June
Cardiff – Holiday Inn	5 July
Swindon – Blunsdon House Hotel	12 July

Further information from the campaign office on 01-261 8400.

As well as providing comprehensive briefings on current asic technologies, the campaign will also be providing an opportunity to see the latest asic products and support systems, as exhibited by some of the leading suppliers in the field. Among them will be low-cost asic starter deals specifically for participants in the DTI campaign. Following each seminar the special exhibitions will include displays by European Silicon Structures, Marconi Electronic Devices, Micro Circuit Engineering, Mullard, Newmarket Microsystems, Plessey Semiconductors, Qudos, Silicon Microsystems, Swindon Silicon Systems, and Wolfson Microelectronics.

Particularly notable in the design of the A&R Black Box – an outboard digital-to-analogue converter for compact disc sound reproduction – is the use of an A&R-designed and custom-made asic manufactured by Newmarket Microsystems. The 1000-gate array replaces the 25 standard m.s.i. cmos chips shown, with substantial improvements in power consumption, digitally radiated noise, reliability and cost. A&R believe this to be the first genuine piece of custom silicon design carried out and put into a British-made hi-fi product.

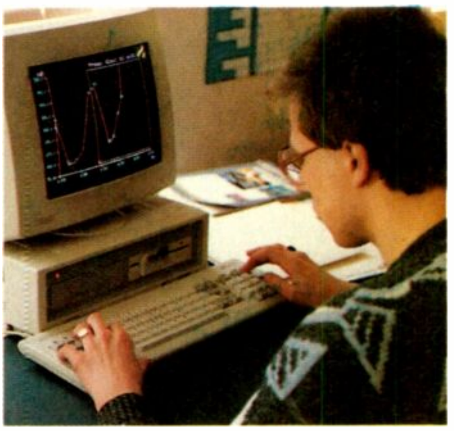
Custom silicon is a natural for use in heart pacemakers where small size, reliability, and low power consumption are essential.

useful extra market. With small/medium companies already buying some 20% of all electronics components, there seems no reason why they should not eventually account for a similar proportion of new asic design starts. And with total UK asic design-starts already running at 2500 per year, this could provide extra business for the growing number of suppliers concentrating on lower-volume asic applications.

These low-volume specialist suppliers include not only the well-publicised new generation of asic manufacturers such as ES2 and Qudos, but also a whole range of associated companies including distributors, design houses, silicon brokers and consultants, cad suppliers, and suppliers of p.l.a. programmers, and all types of asic-oriented a.t.e. For these asic-supply companies, the main problem in exploiting the potential new market offered by the small/medium electronics manufacturers is the additional support they will inevitably have to provide to this type of user. All the evidence is that both suppliers and small/medium users have experienced real difficulties with the supplier/user interface. Suggestions on reducing these difficulties are a key part of the study's conclusions, and the new DTI campaign is likely to be of considerable interest to potential new suppliers of asic services as well as their users.

If the DTI initiative succeeds in helping UK asic suppliers to cater more positively for the small/medium user, the benefits may also provide a boost to the international competitiveness of the suppliers.

Whether the UK electronics industry – as either suppliers or users of asics – actually succeeds in meeting these new challenges of the custom silicon markets will inevitably depend on its own efforts. However, by providing a new focus for the industry's efforts, the DTI Custom Silicon Now! campaign promises to provide a key starting point.



After using a simple terminal on-line to a Plessey computer to design the gate arrays in their 1281 digital multimeter, Datron Instruments have since invested in a Mentor Graphics System for all their c.a.e. including future chip design (top). Cell-based technology enabled this telephone-cable gas pressure monitoring system (right) to be reduced in both size and cost.

"For ASICs I need a company with experience in all parts of the process."

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SEMICONDUCTORS

GETTING TO GRIPS WITH ASICS

Jonathan Kimmit and Claire Ruskin of Cambridge Consultants introduce the first-time user to the technologies and the choices and over the page Claire Ruskin offers down to earth advice on how to choose a vendor

The last few years has seen the introduction of an extraordinary variety of new components which fall under the broad category of application-specific integrated circuit. Many electronic products can benefit from the use of asics by reason of reductions in cost, size, weight or power consumption, or improvements in performance or reliability, or just extra bells and whistles to help persuade a customer to buy. In parallel with this explosion of choice, a whole new vocabulary of jargon has been invented to keep the uninitiated at bay. To make matters worse, supplier's catalogues often lump all these devices, along with the humble transistor, under the bland title of 'semiconductors'.

Choosing an integration approach

One decision that must be made by a designer who is keen to make use of the latest techniques is what level of customizatoin to go in at, or to put it a better way, how much work needs to be done to adapt what is available to the problem in hand. This work can vary from simply designing a p.c.b. full of standard chips (obscurely known as board level customization) to a full-custom single-chip system. For more complex problems a p.c.b. full of specially designed devices may be the solution. The decision as to how much function to pack into each individual asic may be made either for economic reasons (bigger chips give lower yields) or simply out of a desire to divide a problem into smaller parts. A common, powerful combination is a microprocessor, asic and perhaps external memory. It is technically feasible to pull all these into a single chip but unlikely to be worthwhile because of the extra complexity and high unit cost, unless size is paramount. For most applications, design time and effort will be the limiting factor rather than technology capability.

We make no attempt in this article to make a value judgement on the various technologies available. Each particular technique has attendant advantages and disadvantages. Hybrids are more flexible than monolithic devices, but are also more costly. Cmos would seem to be superior to nmos due to the low power capability but it cannot achieve such high densities. Even metal-gate cmos, treated as obsolete by most manufacturers, has important advantages in higher voltage applications.

Levels of customization

Standard (t.t.l. cmos, e.c.l.)

Programmable (eprom, e.p.l.d., p.i.d.)

Mask programmable (rom, single-chip microcontroller)

Gate array (e-beam, single-layer masked, multi-layer masked)

Cell based (full custom, but mostly predefined blocks)

Full custom (user-designed transistors, capacitors, resistors)

In general costs and timescales for development rise going down the list, as the user comes in at a lower level of function. But flexibility and unit cost savings also increase. Each of the options result in a compromise of one sort or another. When designing with standard parts, a frustratingly large number of packages is often needed to perform a specified function, however the final result is relatively easy to debug the modify.

Using proms and p.l.ds will often simplify combinational logic, but the internal structure is too rigid to solve a general problem economically. In particular, storage elements tend to be very sparse. Recognising this problem, manufacturer's have produced a plethora of different devices, with varying degrees of success. More seriously, because of the once-only programming capability of standard p.l.ds, it is not possible to fully test these devices prior to programming. Hence the user is left with the responsibility to verify each device individually after programming. This is normally done by means of a series of test vectors, which are simply columns of numbers specifying the conditions at each input and output of a known good chip. Most development systems will have facilities to aid generation of these vectors, which are non-trivial if the device incorporates feedback from storage elements that do not come out to an external pin.

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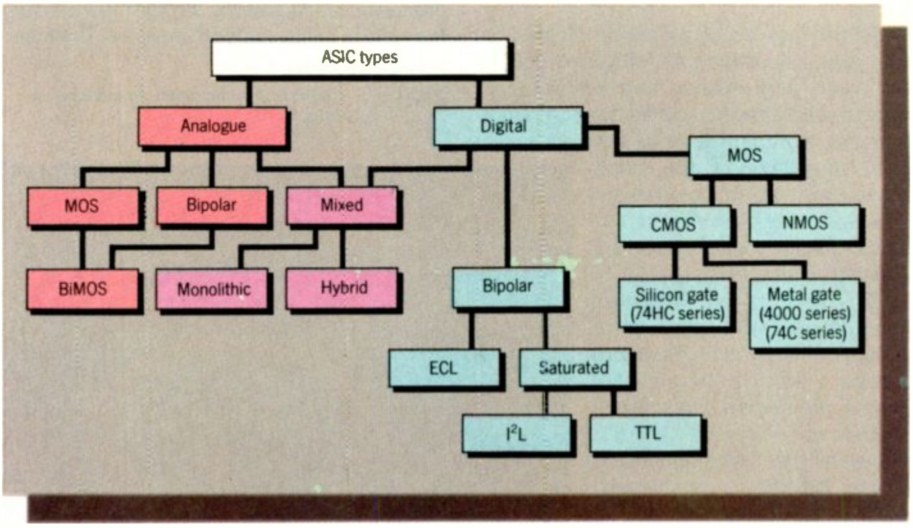
There are as many different processes for asics as there are for standard circuits.



SEMICONDUCTORS

CUSTOM ICS FOR THE FIRST TIME BUYER

Though custom integration techniques have been available for many years now it is only recently that the technology has matured to become commercially feasible for small and medium-sized companies. Suppliers are meeting an increased demand by providing design tools that are easy to use and by reducing the investment needed to customize circuits.

This article outlines the products and technologies available and gives guidelines on choosing between the custom devices and on selecting a supplier.

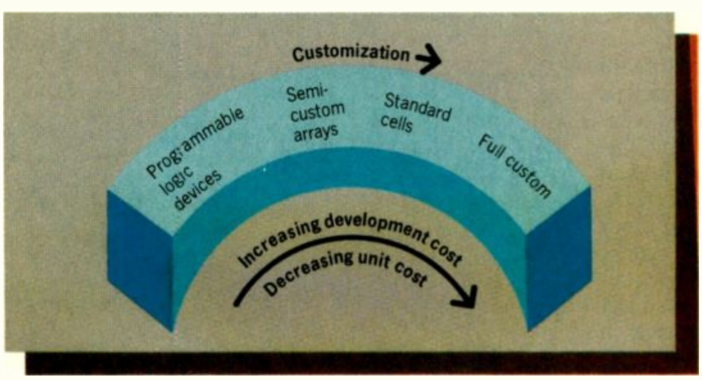
The benefits of integration

The 'custom i.c.' label covers a range of products which are used for a wide variety of reasons. They include

- ★ reduction of component costs
- ★ reduction of assembly time and cost
- ★ miniaturization of a product size and weight
- ★ improved performance in terms of speed and e.m.c. properties
- ★ increased reliability (having no internal solder joints makes a significant improvement)
- ★ automatic testability (devices are tested by the manufacturer before shipping), and
- ★ design security (difficult for competitors to copy).

As with most developing technologies, the first users of custom integration wanted the improved performance and reduced size offered with little regard to the cost. Commercial companies can now take advantage of the experience built up in the industry to achieve real benefits of cost reduction to make better and less expensive products.

At the moment, procuring custom silicon still requires a bigger investment than procuring a printed circuit board, but if production runs are in volumes of more than a thousand per annum then it is worth keeping a close watch on the integration industry.



Products available today

The spectrum of custom integrated circuits can be characterized by the trade-off between the final cost of a device and the time and money involved in tooling up for manufacture. At one end of the spectrum are the expensive products that can be bought off the shelf and programmed in minutes; at the other end are the full custom devices which may take months to develop and weeks to tool up but which can save pounds in eventual costs. The production cost depends on the used silicon area and on the process yield in terms of good dice on a processed wafer. (Hybrids are sometimes included in the custom range, but I view hybrid technology as an advanced implementation technique, akin to printed circuits, and they are not covered here.)

Today's asics can be categorized into four main groups with products listed in order of increasing customization.

Programmable logic devices are specialized memory chips used to implement logic algorithms. A p.l.d. consists of a predetermined pattern of nand or nor gates and registers which can be configured to give the required function. They are available off the shelf in families giving different complexities, and can be programmed in-house using low-cost equipment – very similar to programming memory chips for microprocessor applications. Programmers can use truth tables, algorithms or Boolean algebra for input.

[redacted] low-cost development, immediate results.

[redacted] inflexible, constrained design, high cost in volume.

USE low volume products with a design which fits efficiently into an available device and which is likely to need modification.

Semi-custom arrays are available for logic (gate arrays) and analogue circuits. Gate arrays are the most popular and widely used form of asic. They are easy to use and have demonstrated wide-ranging benefits to numerous small and medium-sized companies. A gate array is programmed by the manufacturer by adding, usually, two layers of metal tracks to configure the transistor array already deposited on the substrate. A semi-custom analogue chip has arrays of pre-defined components including resistors, op-amps, comparators that are linked up to meet specific requirements. These metallization processes for semi-custom can be compared with a printed circuit board connecting components to make the required function. The circuit is described by the designer in components ranging from the simplest logic gates up to complex blocks as found in standard l.s.i. data books.

[redacted] good compromise of unit cost, low risk and short development time.

[redacted] few suppliers of analogue parts.

USE for most logic circuits.

A standard cell device is, to the user, similar to the array design just described and, to the manufacturer, similar to a full custom chip. Cells may be analogue or digital and are likely to be more complex than the components used in arrays. The cells are characterized by the manufacturer and used as a library of components by the designer: this library makes the difference between standard cell and full custom design. Tooling involves building up all layers of the i.c. in the same way as for a full custom chip.

[redacted] very flexible design, supported by supplier's software.

[redacted] fairly expensive and lengthy tooling time.

USE for mixed analogue/digital or integration of l.s.i. components; often used to reduce unit cost of a successful array.

A full-custom device is designed laboriously by hand from the transistor level up. Each component must be characterized by the designer and shapes and sizes must be described in detail for the manufacturer. Full-custom i.cs are not cost effective for most companies – production volumes need to be very high for sensible amortisation of the development costs.

optimized performance, minimized silicon cost.

very expensive to develop.

USE small, specialist circuits not available as standard cells.

Technologies and processes

To assess the *'technology'* required for each application, the key issues are

★ type of circuit (analogue/digital/high power/mixed)
★ performance (clock frequency or analogue character)
★ product application (power supply, working conditions).

The major technology split is between cmos and bipolar devices. In line with standard electronic design, cmos is particularly good for low or variable power applications (particularly battery-driven products) and bipolar is better for very high speed design and many analogue functions.

Complementary m.o.s. is the most popular technology for gate arrays and standard cells; programmable logic devices are predominantly bipolar although an increasing number of cmos families are becoming available. Mixed analogue/digital integration frequently has to be a compromise.

The *process* used will affect the performance of the device and the unit cost. The feature size is important the smaller the feature size the faster the circuit will run. In practice the standard products now available will run fast enough for most commercial applications. As smaller feature sizes become proven and give a high yield in manufacture, their prices are reduced due to the smaller area of silicon used. The processes in common use today for semi-custom and cell products can be grouped into three

- 3-5μm cmos processes, with double or single-layer metallization, are old and becoming more difficult to buy. They are still useful for high voltage, low power applications – for example, a product powered directly by a 9V battery.
- 2μm, double-layer metal processes are the most widely available this year and will usually give the lowest cost device.
- 1μm processes, some with three layers of metallization, are available but are still unusual and therefore more expensive than the standard 2μm device.

How to choose a device

Most of the points need to be considered iteratively with others, as the implications of each decision can be widespread. Some decisions will lead to obvious and fast conclusions; for less straightforward applications previous experience is invaluable.

★ Analyse the complete system before partitioning.
★ List any desirable new features, with priorities
★ Outline a performance and functional specification.
★ Partition the functions for the most cost-effective components.
★ Set a target production cost.
★ Predict sales volumes.
★ Define a development timescale and budget.
★ Decide a policy for managing the risk.

After partitioning, analyse the sections to be customized. Functions will often benefit from a review of the system architecture to allow for the constraints of asic design: the usual circuit has too high a ratio of i/o to content. Outline design will be needed for a gate count or list of components to be integrated, with contingency especially for test circuitry. Pin and component counts are needed before a device can be selected or quotes can be extracted from suppliers.

The choice of technology is determined by the partitioning between analogue/digital and the performance specification.

The process is often transparent to the user and can be chosen by the manufacturer. If there is no reason for choosing something special, leave the decision to the supplier.

To reduce the risks involved in trying asic techniques for the first time it is prudent to start with a small device (fewer than 3000 gates of logic) and to separate analogue and digital functions, mainly for reasons of test confidence. Allow perhaps 30% contingency above an initial estimate of size and choose a supplier with larger devices available in the same family. To start the integration process with a gate array and discrete analogue components and then upgrade to a mixed standard cell design can be a worthwhile low risk approach in some cases.

How to choose a vendor

Most asic vendors are in the business of selling silicon. As in other businesses, suppliers will be very helpful – to the point of providing 'free' design work – if you can promise to buy large quantities of their product. When in this position, make the most if it and find the best deal by talking to many vendors. Around 60 companies advertise products under an asic label in the UK. Not all are credible and the area is still a jungle for the first time buyer.

For a programmable logic device, choose a family of chips that suits your design, that is well supported by programming equipment, ideally compatible with prom programmes you may already have, and experiment.

For the other asics, the manufacturer and your relationship with him are important. Vendors are widely different in all the usual ways: costs, timescales, reliability and expertise. *In many cases the technology is less important than the vendor's ability to meet your expectations.*

When selecting a vendor, consider

★ technologies and processes offered
★ design interfaces possible
★ vendor's track record and competence
★ unit price and non-recoverable costs
★ delivery timescales
★ communications and location
★ company's likely future and financial position.

If you are buying an unusual technology the choice of vendor can be narrow, making the selection relatively easy. If, however, you are buying a cmos gate array of moderate size and performance, there are very many competing products and the choice is more difficult. The market can change very rapidly and it is effective to survey the major contenders for each chip design started. Loyalty is comfortable but the details of each design can lead to surprising cost differentials for a range of companies.

The design interface is important when the design task is split between companies and if it is planned to do most of the work in-house the point of data transfer must be defined at the outset.

Some manufacturers offer a low-cost entry to asic technology by means of a regular multi-project wafer scheme. These can be a low risk introduction to integration, with up-front investment being as little as a few hundred pounds. Options are usually limited but if the application is appropriate confidence can quickly be built up, and marketing prototypes can be made without rigorous testing and optimization. Second sourcing is a contentious issue with asic suppliers. A true second source will almost certainly involve a new set of masks produced from flexible source code.

To be the first customer or the first to use a new process carries a high risk; to use a mature technology, with both larger and smaller devices available in the same family, will give a good chance of success. As this is not a one-off purchase business it is wise to avoid small companies which tend to disappear as quickly as they arrived.

Tooling for production will cost anything between £500 and £50 000; component costs will normally be between 50p and £10. The Table on pages 601/2 gives an outline summary of companies in the UK. For your own applications, talk at length to several vendors and assess all the options...

Claire Ruskin is leader of the electronic product design group at Cambridge Consultants.

THE DISTRIBUTOR'S ROLE

Phil Goodman of Rapid Silicon explains why you should go to a distributor's asic design centre.

The three main options open to a prospective asic user are to

- purchase the appropriate design equipment and do-it-yourself (including the communication and interface with the silicon vendor).
- go direct to the silicon vendor and have them do it all for you.
- go to an independent design centre.

As an independent design centre I'll describe some of the benefits of this approach.

One of the first considerations has to be capital investment. We are all aware that the cost of hardware, and for that matter good software, has significantly reduced in recent years, however, a good usable system providing full breadboard simulation facilities, will still cost around £40K. A company just starting out on the asic route will be loath to spend such a capital sum until they are convinced of its value to their own environment and, perhaps more important, until they are able to justify such an investment and realistically judge the payback period. This will depend on the number of designs going through the system in a typical accounting period. Therefore smaller companies, or even the larger companies who have few new designs per year, can benefit from hiring time on a well-equipped design centre system.

Another consideration has to be skill and equipment familiarity. However simple a system is to use, there is always a re-learning time. Using the skills and resources of a design centre will mean maximum utilisation of the equipment whilst allowing the design engineer to exploit their own specialist knowledge and skill.

In an ideal environment, we recommend that the infrequent user of asic design environment employs a design centre that will give access to the equipment whilst at the same time devoting dedicated technical assistance to ensure maximum system usage. In this way the customer gets the best of both worlds – a fast, efficient design cycle and the hands-on experience that will let the user fully learn and appreiate what asic designs can offer. When skill levels are sufficient and the appropriate usage is achieved, the customer should seriously consider purchasing equipment for their own use.

Looking at the choice of asic design facilities, the customer must also acknowledge that product development in terms of hardware and software is leaping ahead almost daily. A progressive design centre will keep pace with this and, because of the throughput and usage of the system, should be able to cover the costs involved.

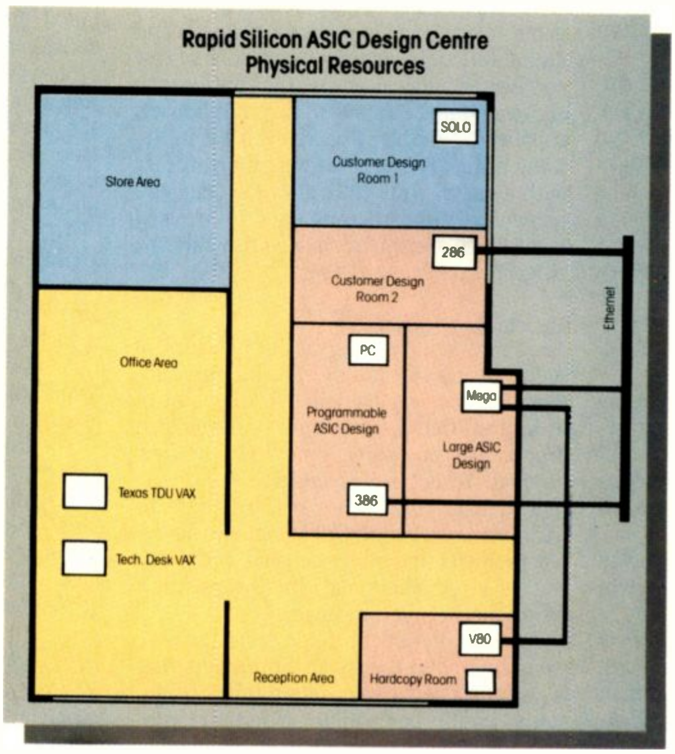
Let's now examine the asic design centre offered by traditional semiconductor distributors. The word distributor in this context is unfortunate and should be replaced by 'a supplier of products and services'. The services part of this description has been explained, but let's examine the product side.

A customer going direct to a manufacturer of custom silicon will be restricted by those products actually manufactured and supplied by that manufacturer. At Rapid we have a number of suppliers, each market leaders in their own sectors. A customer coming to us looking to put a design into a semi-custom device may well be advised that a programmable logic (i.e., p.l.a., e.p.l.d. or l.c.a.) would more than suffice even though it meant sourcing the actual silicon from a different manufacturer. The same may also be true in reverse.

The same can be said for the design equipment. At Rapid we have a number of systems networked together to allow very cost-effective utilisation. Individual chips can be designed and developed in isolation (and indeed in parallel if time is of the essence) and then brought together on a system-level simulation to not only test the individual designs but also how they will perform with each other.

I would dispute the myth that high volume is necessary before asic designs become cost-effective. Our experience has shown that production runs as low as a few hundred off can be of lower overall cost than traditional design and production methods. I therefore recommend that any prospective design engineer or company question their design centre to establish the break-even point for their particular design. An investment of a few hundred pounds on a feasibility study early on could well save thousands when that product goes to market.

A 'distributor' is able to offer customers advice and products ranging from c.a.e. equipment to asic systems and designs with minimal risk and outlay together with ability to become involved with asics at any level. A further advantage is that the traditional semiconductor distributor will combine asic services with true distribution. For example, customers requiring 4,800 pieces of an asic design can negotiate to have 400 pieces shipped monthly over 12 months, thereby minimizing cash flow. This will probably not be available from manufacturers.



Application specific integrated circuits manufacturers represented in UK

Manufacturer (parent)	Technologies offered	Product type: gate array	Product type: a/d array	Product type: cell-based	Feature size (µm)	Customizing process	Gate array sizes	Analogue cells	Multi-project wafers	Design engineers (UK)	Past UK customers (designs)	Geography: Nationality	Geography: Fab. line	Geography: Design centres	Typical n.r.e. cost for 1000 gate tooling	Comments
AMD Inc	bipolar	✓	–	✓	2 1(4Q88)	photolith	up to 3k (3-27k 4Q88)	no	no	none	20	US	US	–		
Analog Devices Inc	Lc.²mos bimos	–	–	✓	3 4	full mask design	–	✓	no	8		US	Eire	Newbury	$40-200k	includes design, layout masks, characterisation, prototypes
Applied Micro Circuits	bipolar bicmos	 ✓	–	✓ ✓	2 1.5	dlm/tlm	up to 5k up to 14k	discuss	no	2	(400)	US	US	Cambridge	$25-55k	Macro Matrix design kit
Atmel Corp	cmos	e.p.l.ds	✓	✓	1	–	500,750,2.5k 2.5k	no	no	2	GEC, Smiths Plessey	US	US	–	nil	programming in ABEL or CUPL
AT&T Micro electronics	cmos bicmos bipolar	–	✓	✓	1.75, 1.25 0.9 (4Q88)	dlm/slm	–	✓	✓	10	–	US	US, UK, Sp	Bracknell		
Austria Mikro Systeme Int	cmos	✓	✓	✓	5,3 2	dlm/dlp e-beam	300-2k 1000-10k	✓	✓	2		Aust	Aust.	Swindon		
Cherry Semi-conductor Corp		–	✓	–	4	slm	–	✓	no	6	AB,Ford Datalogic VDO	US	US	Portsmouth		
European Silicon	cmos	–	✓	✓	2 1.5	e-beam	not fixed	✓	✓	10	150	Eur	Fra	Bracknell		Solo 1200 cad suite for new users
Exar Corp	cmos bipolar i²l	✓	 ✓ ✓	✓	3,2 8.5	slm/dlm	up to 3k	 ✓	no	nil	(1000)	US	US	–	$8-12k gates $5-15k analogue $40k std cell	Rohm in Japan
Fujitsu Microelectronics Ltd	cmos bicmos bipolar	✓	 ✓	 ✓	1.2,1.5, 1.8,2.3	dlm/tlm	330-100k 400-2k 350-10k	✓	no	35	50(N.Eur)	Jap	Jap US 4Q88	Manchester Maiden-head	£7.5k 10 samples	Approval to sample 4 weeks. 120 pin flatpack £5.27
GE Solid State	cmos bimos	✓	✓	✓	1.2 3	dlm	250-50k	✓	✓	3	100(Eur)	US	US	Camberley		Compiled ram, p.l.a. eprom, rom Pronto Electronic Systems
Gigabit Logic	GaAs	–	–	✓	0.8	mask	5k-10k	✓	✓	1	(200)	US	US	–	$50-75k	includes 20 tested
Hitachi	cmos bimos	✓ ✓	– –		1 1.8 2 2	dlm	450-2.5k 4k,7k 800-24k 630-2.5k	no	no	5		Jap	Jap	Watford Hinckley Reading		'Variable size cell 'silicon module to be announced
Hughes	cmos	–	–	✓	3.6	9-14masks	–	✓	no	15	>100	UK	UK	Weybridge		
IMP Europe	cmos p-well cmos n-well nmos	1	✓	✓	2,3,5 1.2,2 2,3,5	d/m/s/m, dlp/slp, dlp dlm	up to 75k	✓	✓	24		Eur	US	Swindon	£15k	
Innovative Silicon (SGS-Thomson)	cmos	✓	✓	✓	1.2,1.5, 2,3,5	slm/dlm	272-128k	✓	no	9	200(ww)	[illegible]	Italy	Marlow		
Intel	cmos	✓	–	✓	1.5	dlm	5k-15k	no	no			US	US	Swindon		80C51 controller in standard cell lib.
International Microcircuits	cmos	✓	–	–	1.5,2	contact masks	60-10k	✓	no	5		US	US	Basingstoke	£10k any gate count	
LSI Logic	hcmos bicmos	✓	✓	✓	1,1.5 1.5	dlm	700-100k	✓	no	25	(350)	Eur	UK Ger	Bracknell Livingstone Sidcup		
Marconi Electronic Devices Ltd (GEC)	cmos sos	✓	✓	✓	2,3 2.5	dlm	400-10k	✓	✓	40	96	Br	UK	Lincoln Wembley		
Matra Harris Semiconductor (Matra, Harris)		✓	✓	2	2 0.8 1.2,3	dlm dlm s/m	850-7.5k 3000-35k 250-12k	✓	✓	3	(400)	Fr	Fra	Bracknell	£15k	
Mietec NV	cmos	–	✓	✓	var.	dpdlm	–	✓	✓	none		Belg/Fra	Bel	Belgium		
Microcircuit Engineering Ltd (Smiths Ind. plc)	cmos bipolar	✓	✓	✓ ✓	2,3,5 2,3	dlm/slm	5µ300-1440 3µ2100-3400 2µ1100-9800	✓	✓	12(25³)	175+ (275educ)	Br. Br.	UK, Can, US, Aust Ger	6	£1.5k (5,3µ2,500g) £4k (2µ.3000 gates)	Prototypes (10): gates £350-£1250 full custom £120/mm²
Micro Power Systems	cmos bimos	– –	full custom	✓	2,3	full mask set(10.12)	–	✓	no	?	see comments					Pacemakers, multi-meters, SLR camera chip, hearing aids (1V)
Motorola	e.c.l. bimos hcmos	✓	✓	✓	2,3 1(.75min)	photolith 1,2,3 layer metal	600- 105k	✓	no	6	750 <100	US	US	Aylesbury	£5k 2µ	Bipolar series 10,000 gates 1.2GHz 650MHz i/o
Mullard (Philips)	cmos	✓	✓	✓	1.5,2,4	dlm	800- 12.7k	soon	via ES2	8	telecom edp, security	Dutch	Neth Ger Tai	London	£6k + design	Second sourcing with TI on 2µ
Nat Semiconductor	cmos ecl	✓ ✓	– –	✓ ✓	1.5,2 1.5	dlm	600-8.7k 400-15k	✓	✓			US	US, UK	Swindon		
NCR Corp	cmos	✓	–	✓	1,1.5,2,3	dlm	650-8.5k	✓	no	✓	–	US	US	Maidenhead UK: Manhattan Skyline		
NEC Electronics	cmos bicmos ecl	✓	✓	✓	1.2,1.5	dlm	320- 45k	✓	no	8		Jap	Jap	Milton Keynes	£7k design inc	Complex macros available
Newmarket Microsystems (CEI)	cmos bipolar	✓	✓	✓	1.25,3	dlm	up to 21k	✓	no	4		Br	UK	Newmarket	£1k	
OKI Semiconductors	cmos	✓	–	✓	1.5,2,3	dlm	300-10k	no	no	✓	–	Jap	Jap	Maidenhead UK: Manhattan Skyline		
Panasonic (Matsushita) – to be announced																
Plessey Semiconductors	cmos bipolar (ecl) bipolar (cdi)	✓	✓	✓	1.5,2 1.5 emitter 1.5,2.5	slm/dlm std cell mask set	600-110k 600-4.5k 130-10k	✓	no	80	1000	Br	UK (3)	Swindon Oldham	£7-23k £1.7-35k £4-20k	

Manufacturer (parent)	Technologies offered	Product type			Feature size (μm)	Customizing process	Gate array sizes	Analogue cells	Multi-project wafers	Design engineers (UK)	Past UK customers (designs)	Geography			Typical n.r.e. cost for 1000 gate tooling	Comments
		gate array	a/d array	cell-based								Nationability	Fab. line	Design centres		
Qudos	cmos bipolar	✓	✓[1]	–	1.8,3,5	e-beam	600, 11k 2.5k	✓[3]	✓	8	100 Olivetti Lucas	Br	UK	Birmingham Liverpool Henley	£2k none[5]	layout by customer samples £500 (5) Educ. discount
Raytheon Semiconductor	cmos bipolar	✓	✓	–	1.25	e-beam	1-20k 7k,14k	✓	no	1	14 years production	US	US	–		36V array
Ricoh Semi-conductors	cmos bicmos	✓	✓	✓	1.5,2 2.5	dlm	500-82k	✓	no	3	Philips, Sony Nintendo	Jap	Jap	– Maidenhead		UK: Semi ICs Ltd, Manhattan Skyline
SGS-Thomson	cmos bipolar	–	✓	✓	1.2,3 2.5	dlm electromask	– –	✓	no	12	20-25	Fr,It	Fr,It	Marlow	£11k a/d	£20k std cell
STC Semiconductors	bipolar cmos	6	✓	– 7	2	slm	268,384 415,2430	variable	no	16	15	Br	UK	Footsoray	£15k 25 samples	Arrays up to 1GHz good noise linearity cmos telecom library
Semefab Scotland Ltd (Semelab)	cmos pmos bipolar photodiodes	✓	✓	✓	3.5	slm	500-3k		✓	none	8	Br	UK	Glenrothes		£150-200 per 4in wafer; gate array finishing at reduced cost
Siemens	cmos ecl	✓ ✓	✓ ✓	✓	1.2,2,3	2,3 level metal	2.5k	✓	no	t.b.a.	100+	Ger	Ger Aust	t.b.a.	£10k	Unit-price from 90p
Tektronix Tri Quint (Tek)	bipolar Ga As	– ✓	✓ –	– ✓	1 1.6	dlm	200-500tr 500-6000g	✓	✓ no	2		US	US	Marlow	£20k £20k	6.5GHz tv toggle 1, 2, 4GHz
Texas Instruments	cmos	✓	–	✓	1,2,3	e-beam (2,3μ)	3μ 1k 2μ 2k 1μ 8k	at 3μ node	✓		major o.e ms	US	US Jap	Bedford		Second sourcing with Philips 2μ
Toshiba	cmos	✓	–	✓	1.2	dlm	540-50k	no	no	3-5		Jap	Jap	Camberley		
United Micro Circuits Corp	cmos	✓	–	✓	5,3,2	dlm	200-3k	no	no	✓	–	Tai	Tai-wan	Maidenhead UK: Manhattan Skyline		
VLSI Technology	cmos	✓	✓	✓	1,2	dlm mask set for cells	1-50k	✓	no	8	Acorn STC, Intel	US	US	Milton Keynes	£6.6k	Design centres at PA-Technology Quarndon

Monolithic Memories – see AMD. Ferranti – see Plessey. Fairchild – see Nat-Semi. Philips – see Mullard. RCA – see GE. Signetics – see Mullard.
1-Second source agreements with Nat-Semi, VTI. 2-compiled circuits. 3-franchised outlets. 4-second sourced by arrangement. 5-Under DTI Custom Silicon scheme, see page 593.
6-Transistor arrays. 7-Telecom library in cmos.
Abbreviations: dlm etc. double layer metallization, dlp. double layer polysilicon.

from page 597

Mask-programmed microcontrollers are really a type of full-custom device, but the only user-input is in the form of software, which is well-suited to performing complicated tasks relatively slowly. The availability of programmable versions of most microcontrollers makes the process relatively hazard-free.

Gate array techniques offer the simplest route into full flexibility of digital design. The required arrangements of transistors which generate gates or storage elements are predefined. All the user need do is specify the types of elements needed and the interconnections by means of a netlist or schematic.

The fixed sizes and arrangements of transistors do not lend themselves to being used for analogue functions such as amplifiers and analogue-to-digital converters. For analogue and mixed analogue/digital chips cell-based or full custom techniques should be used. These techniques are similar in that all features are user-specifiable, but with the cell-based techniques most common functions are pre-defined items which can be included as needed. This obviously saves a lot of design work. Even if analogue circuitry is not needed a cell-based technique might be chosen to increase density and hence ultimately reduce unit costs.

Special considerations for asic design

Many asic vendors offer a conversion service which allows a logic function performed by a board full of standard parts to be converted into monolithic chip. However unless the original circuit was designed specifically with integration in mind considerable redesign is likely to be needed for a variety of reasons.

Board-level products frequently make use of asynchronous counters, delay lines and even capacitors to minimize component count. On-chip delays, set-up and hold times may be very different to the equivalent standard parts and also may vary hugely from chip to chip.

In mass production, up to 50% of chips on a wafer will not function due to defects in the silicon structure. To reduce costs these chips must be rejected before packaging. This is done using a wafer probe that is connected to each chip in turn and applies a series of test vectors and compares the chip outputs with what was expected from simulation of the logic function. This method only works if all internal storage elements can be set to a defined state, and the test inputs cause all internal costs to be exercised, with the results reaching the outputs. Usually extra logic has to be added to satisfy these requirements.

Most standard parts incorporate buffering to drive the outside world. On-chip geometries and drive capabilities are much less and extra buffers may be needed which will depend on lengths of routes on metallization layers.

If tri-state buses are in use, these may float to an undefined level internally and cause variable supply currents due to input thresholds being crossed.

Dense functions such as roms or rams may not be integrable economically. This may limit the amount of function obtainable per chip due to pin-count considerations.

Simulators

Because of the difficulty in testing and debugging chips simulators are used extensively to give confidence in a design before committing to the prototype stage. For gate arrays or cell-based designs around predefined digital cells, a digital simulator should be adequate. For full custom designs the simulator will need to model down to the transistor level, with a big increase in effort, time and cost. Hence a balance must be struck between simulation effort and confidence in the finished design. Most simulators do not model glitches and other hazards very well, so fully synchronous designs usually stand a better chance of success.

A simulator can also help with development of manufacturing test vectors, since the various fault conditions may be simulated to determine if a given set of test vectors will result in the fault condition reaching the output. Since simulation time goes up roughly with the square of gate count. This sets another constraint on the size of the chips that may comfortably be designed.

SEMICONDUCTORS

WILL FUTURE ICS BE METAL?

Researchers at AT&T Bell Laboratories have produced experimental single-electron transistors – devices so sensitive that just one electron produces changes in the current flowing through them. The devices are prototypes that operate only at very low temperatures. However, scientists there feel their performance may foreshadow a generation of all-metal transistors that are extremely fast and small and consume very little power. In their present form, they could be used as electrometers in experiments to measure induced charges as small as 1% of an electron.

Much engineering and development work would be needed before practical devices such as switches and computer elements could be made with the new transistors. In fact, Greg Blonder, group leader at AT&T Bell, would not come down from his ten year estimate for a ring counter type of device. But they show potential to change the way we think about a future generation of integrated circuits, he told us, because they use infinitesimal amounts of power and space, have an intrinsic speed of less than a picosecond, and use the smallest possible amount of charge transfer.

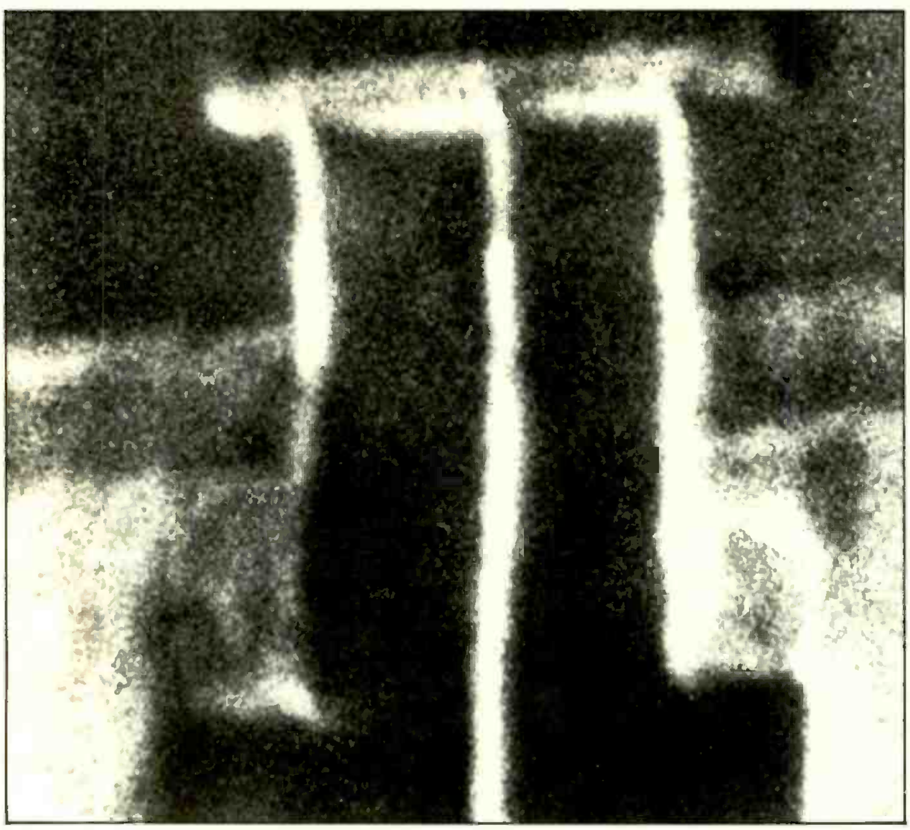
Even modern, miniaturized f.e.ts involve thousands of electrons in a similar voltage change, while these devices require just one, which is what leads to the high speed.

These devices can now be made through new fabrication techniques pioneered at Bell Labs by co-inventor Gerry Dolan. Researchers use electron-beam lithography to pattern a high-resolution organic film layer. Then they deposit the aluminium electrodes and an oxide barrier. A technique called edge lithography allows devices less than one-twentieth of a micron across to be made by making use of overhangs of deposited metal under which is deposited on insulating oxide. Metal is then evaporated under the overhang or bridge. This form of sandwich results in extremely small capacitance.

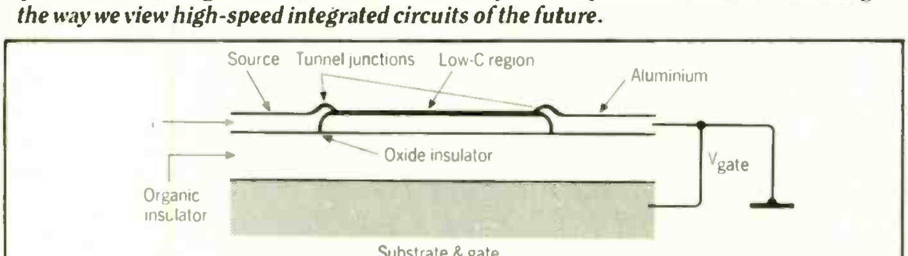
The transistors consist of three microscopic parts. The first is an island of aluminium a few hundred atoms across, see diagram. Connected to the edge of this central island electrode are two tunnel-junction electrodes separated by an insulating barrier only a few atoms thick. The substrate forms a remote "gate" junction that applies an electrical field, creating a steady-state bias – and thus a charge – across the junctions.

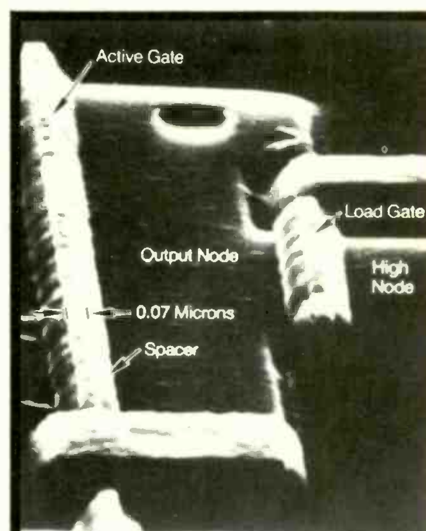
This charge controls the current passing through the central electrode via the tunnel junctions.

Such a single-electron charging effect in electron tunnelling was predicted a few years ago by K. Likhavev of Moscow University.



Scanning electron microscope picture shows new AT&T Bell transistor magnified 100,000 times, with electrodes connecting to either end of the central electrode and a test rod running down the middle. Metal-oxide-metal transistor (a 'mom'?) relies on quantum tunnelling and needs to be cooled to very low temperatures, but it could change the way we view high-speed integrated circuits of the future.





Researchers at the IBM's Research Center at Yorktown Heights, New York, have obtained the fastest silicon switching results from circuits designed to assess f.e.t. technology in the 0.1-micron gate-length region. Self-aligned and almost fully scaled devices and circuits were fabricated by direct-write electron-beam lithography at all levels, with gate lengths down to 0.07 microns and a switching speed of 13ps.

SEMICONDUCTORS

THE INDEPENDENTS APPROACH TO ASICS

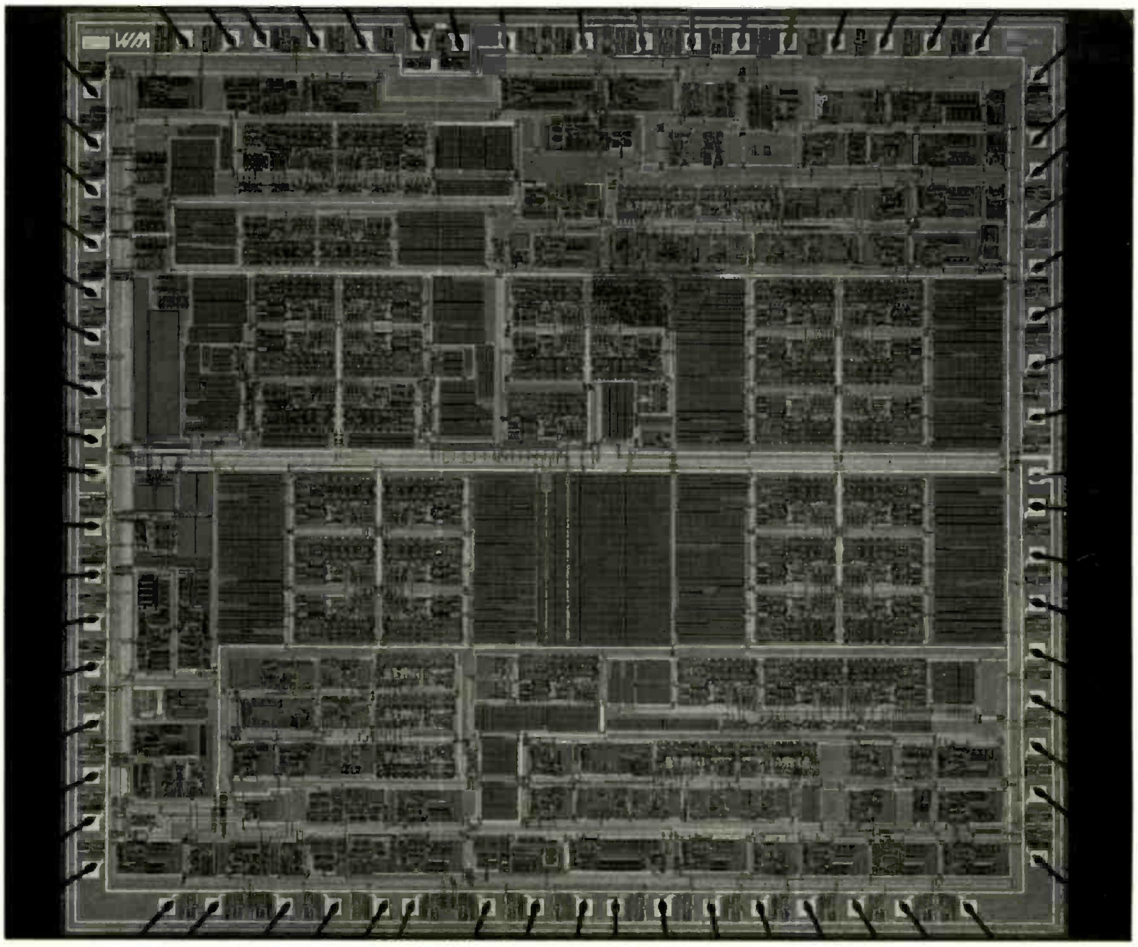
The manufacturers don't have all the answers, according to Dr David Milne, m.d. of Wolfson Microelectronics

The use of custom or application-specific integrated circuits is now becoming a reality for many companies. Gone are the days when they were viewed as esoteric artifacts of the military and computer industries, available only to people with large budgets and semi-infinite timescales. Asics are now being adopted widely throughout the electronics industry and are becoming essential to the successful production of cost-effective equipment. Many companies, however, remain uncertain about how to access the technology and are confused by the variety of claims made by the semiconductor companies.

The range of technologies, cad systems, and design styles can be bewildering and obviously each manufacturer is intent on selling their own-brand without reference to a competitor's alternative and perhaps more suitable capability. In the UK, however, potential users of asics have the benefit of a number of experienced "independent" suppliers of asics who undertake the necessary tasks to supply suitable products but who are independent from the semiconductor manufacturers.

These vendors, such as Wolfson Microelectronics, offer a wider range of assistance to companies looking at asic developments and are able not only to choose the most appropriate manufacturer for a particular asic but can ensure that alternative sources of production are available. This provides the user with an important control on the price of end products in this highly dynamic market. In addition, because the independents are not concerned with manufacture themselves they concentrate their efforts on

The photograph shows a full-custom asic which is mostly analogue intended for use in mobile communications products. The chip, which is manufactured in a 3μm double poly cmos technology for low power and high performance, integrates several high precision audio-band filters with other non-linear signal processing functions. The filters themselves make use of the continuous time transconductance technique pioneered by Wolfson Microelectronics.



optimizing the design to maximize the benefit of using an asic to the end customer. The independent asic vendors therefore provide much more than just an interface to manufacture and subsequent supply of customer-specific products.

One of the most difficult areas in the use of asics is translating the system or product requirement into a form which can be implemented in silicon. This will frequently require knowledge of both the customers system and silicon design technology, something that the semiconductor companies are unable to provide. One way round the problem that has been highly successful has been to restrict the type of circuit to be implemented, for instance, to digital logic for which a simple interface can be defined. An end user who is familiar with logic specification can then describe his circuit in terms of a functional netlist which can be mapped directly onto a regular silicon structure in the form of a gate array. In this approach of course, the manufacturer is only offering to supply products which are in accordance with the netlist and it is up to the end user to ensure through simulation or otherwise the suitability of the product for the system.

Many applications however require more variety of circuitry than simple logic and then the design is more complicated. It is essential to marry the total system requirement more intimately to the technology and this is where the independent vendors have to play a key role. Because of their service rather than manufacturing approach, the independents work closely at an engineering level with the end users to specify the asic from a systems-level functional requirement. This may involve considerable interaction and possibly engineering development work as the process is not simply one of simulation. A combination of partitioning of the system and synthesis of the wanted circuit functions is wanted. While existing cad tools are used for system simulation and circuit implementation at both the electrical and physical levels, little useful software exists for the intermediate stage.

For anything other than the most trivial of systems, engineering innovation and inventiveness are paramount in producing the cost competitive product. These skills are harmonised to effective circuit implementation using the latest cad techniques in the independent asic companies. Almost exclusively they are able to offer the combination of systems level consultancy with device implementation and subsequent supply using the optimum technology avaiable on a world wide basis. The ability to choose a high volume, a low-cost manufacturer in, say, the Far East for one product and for another, a manufacturer with the latest memory technology combined with low-power microprocessor and analogue-to-digital converter cells is essential to meet the needs of potential asic users. With the capitalization required to set up an advanced semiconductor production facility, manufacture has become a highly specialized business not suited to providing the variety of options necessary to service the asic market. An intermediary is required with access to a range of manufacturers and an ability to develop a systems level solution. Hence the importance and increasing role for the independent asic vendors with their freedom of action and service orientation.

Wolfson Microelectronics was founded in 1985 as a supplier of niche market integrated circuits and custom design house.

FEAR OF FLYING

Peter O'Keeffe, managing director of Qudos looks at prototype chip design and finds that many of its problems are more than simply technical

There are two principal reasons why more companies are not designing their own chips. Both are based on fear.

The first is fear of inadequacy. British designers in general are afraid they may not be up to it – that the technology will be too much for them and they will be swamped by the sales talk of over-enthusiastic suppliers.

Nothing is further from the truth. We have a wealth of technical talent in this country – well up to seeing through honey-tongued sales pitches. The fact is that application-specific integrated circuit design is straightforward. Any competent programmer, let alone an experienced hardware engineer, could learn to design a semi-custom chip in a matter of weeks.

The other reason is fear of high cost. Everybody 'knows' prototype chips must be expensive. They have at the back of their minds vague stories of great wads of money having to be absorbed or written off by the mass production run. Admittedly all costs are relative but does £100 sound too bad a starting price for your ideal custom-designed logic device? And having five cmos prototype gate arrays fabricated using electron-beam direct-write methods now costs as little as £500.

Over the past few years, asic technology has become very much cheaper and simpler to use. Despite this most British firms ignore it, preferring traditional methods of circuit design.

The two reasons can really be encapsulated in one – which I call the fear of flying. It is the fear of becoming a success, and its awful corollary, the worry of making a hash of things.

A recent report from the DTI* claims that most small-to-medium size companies are unaware of the advantages of asics and are not taking advantage of the opportunities available to them. It is for this reason that the DTI is launching its Custom Silicon campaign now (page 593), a travelling roadshow which aims to demonstrate to local businesses the benefits of using asics, in which companies such as Qudos will be participating.

The user of every new technique, every innovative system engineer, is likely to be made nervous by the realisation that he is taking some kind of chance, however small. In the case of Qudos's prototype chip production those chances have been reduced to a minimum. However, a company must do all it can to assuage fear.

So one reassuring service Qudos offers is a training course in which professional design engineers, programmers or even gifted amateurs, are invited to design their own chips. There is nothing like hands-on experience to put abstractly thinking minds at rest. Theory is kept to the minimum. At the end of the course, the chip each trainee has designed is put into production.

Another service is the establishment of a network of regional design centres around the country, the first of which is being run in conjunction with Birmingham Polytechnic. The design centres will run basic design

* *See footnote on page 593*

£500 CHIP DESIGN

In the 18 months since it commissioned its first e-beam machine in September 1986 Qudos have manufactured more than one new asic design per week, attracting customers such as Olivetti and Lucas Aerospace, Cambridge University, Birmingham Polytechnic and Essex University, as well as smaller ventures such as Flare, General Information Systems and Millenium. The company, who passed their 100th asic design last April, are offering small businesses the opportunity to have designs fabricated at a fixed price of £500 per chip design as part of the DTI's custom silicon awareness campaign. The offer extends until the end of 1988 and is limited to ten designs on three-micron chips per company. Qudos say it represents a minimum saving of 60% on current list prices.

In addition, Qudos' Quickchip software can be rented for three months for £500, compared to the normal list price of between £5,000 and £25,000 depending on the number of users. Limited numbers of workstations on which to run the software are available for an additional £500 for the three months. Quickchip design software runs under Unix on DEC's MicroVax, Sun, Apollo workstations, and IBM P.Ts and compatibles.

Also in support of the campaign is an award scheme for asic designers in industry or education for the team accumulating the most points for the most innovative and elegant asic design. Points may be accrued for multiple designs. Industrial design teams or individual departments wishing to enter must notify Qudos by the end of June 1988. Prize is a holiday for two in 'Silicon Valley', California.

Unwanted metal is etched off the wafer by dry-etch plasma machine.

courses for local firms, using Qudos' Quickship software, enabling these firms to have consultancy on their doorsteps. On top of the two major worries already mentioned is the idea that it probably takes forever to get delivery of customized items.

All this leads to the overall conclusion that the risks are just too high and the nearest standard item is bought instead, or the company sticks to outmoded technology. This is why the asic market is not growing as fast as it could.

And the worst aspect of the problem is that industry is in danger of missing the boat.

Any company who is sticking to conventional p.c.b. technology when there is the option of customized silicon chips is losing out. This is because of the recent great strides made in electron beam lithography and computer-aided design software, allowing chips to be produced at low cost within a short timescale. The new desk-top cad tools are easy to use and accessible to those without a great deal of technical knowledge.

"Any company that sticks to conventional printed board technology when there is the option of customizing silicon is losing out"

At Qudos the standard time from initial concept in a client's mind to delivered protype chips, say ten off, is commonly within a month and it can be much sooner.

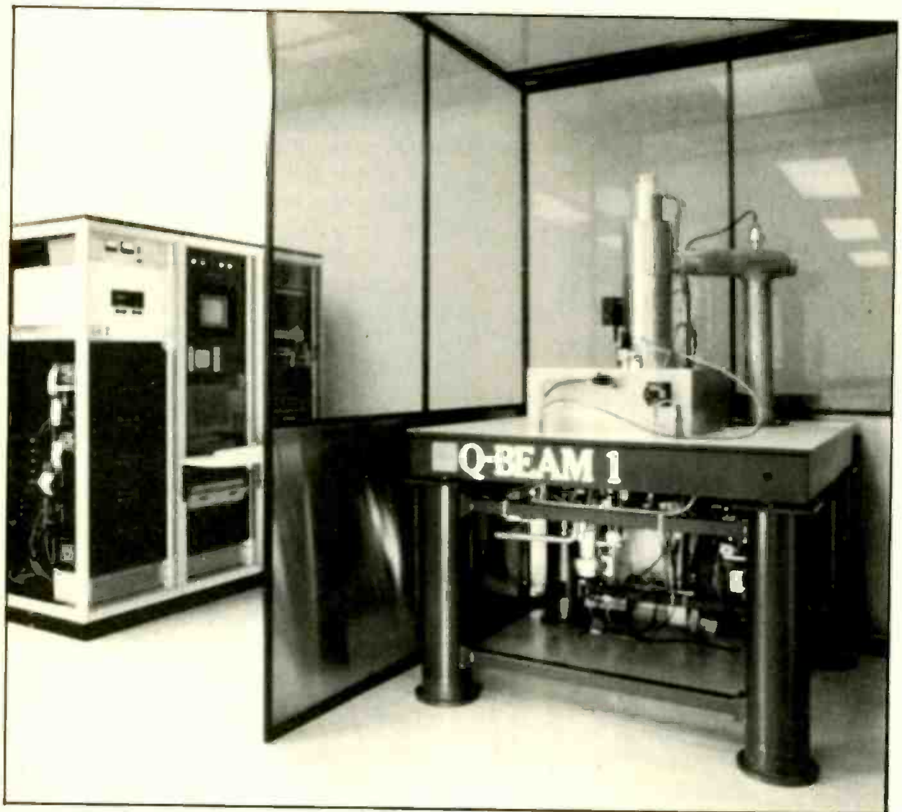
From the end-user's point of view e-beam means economy beam. Because expensive optical masks are dispensed with, the designer can afford to be more adventurous. Different designs can be experimented with at very little extra cost.

Most designers would agree the primary cost is not the main consideration – it is the cost of mistakes, iterations, which is more worrying. What if it doesn't work? Obviously no 'wonder technology' can make a bad design into a good one but with the simulations built into the Qudos system, the chances of an inadequate design slipping through the net is hugely reduced.

As for the software options available, they are designed to suit the end user at an level of complexity. At the 'gifted amateur'/cost-conscious academic level, a BBC Micro can be used. At a higher level IBM PCs or compatibles or almost any Unix-based workstations are required. A common database ensures easy swop over at the appropriate time.

The aim is for any engineer to be able to design a gate array at his own desk, wherever that is. The market for Qudos products and services is as much the rarefied research lab as the hurly burly of a busy commercial technical company or the groves of academia.

It is the person, department or company which doesn't have a fear of flying that will be able to make kudos out of companies such as Qudos!



'Q-beam' machine writes the specified pattern directly onto the wafer by electron beam.

SEMICONDUCTORS

CUSTOM DESIGN WITH A PC

How to design asics using standard PC hardware.

The emergence of the personal computer in the field of computer-aided design and engineering has had, in recent times, an important effect on the fortunes of workstation manufacturers. The popularity of IBM-compatible machines means that companies need to provide application software at a cost comparable to the hardware itself. It is this factor that led to the introduction of two software packages called Super Sceptre and Spice Sceptre.

Super Sceptre is a complete low-cost system that can take a design from schematic capture through to logic simulation and place and route for standard cells. It can also go to the validated netlist stage for gate arrays. Spice Sceptre is essentially the same package but with the inclusion of P-Spice from Microsim. This means that analogue as well as digital circuitry can be designed at the transistor level and simulated prior to the start of any layout work.

The basic hardware required to run the Super Sceptre package consists of one IBM-AT, or compatible, with 512K of ram, a graphics monitor and graphics adaptor. The adaptors currently supported are IBM PGA EGA and the Hercules monochrome adaptor. For the Spice Sceptre software a mathematics co-processor is also required. For transferring the completed database to the foundry it is only necessary to have a floppy-disc drive. Other peripheral devices – printer and plotters – are supported as standard.

Super Sceptre has been designed along hierarchical lines so that the designing task can be broken down into a number of sub-tasks. This is not just in keeping with a structured design methodology but it also enables a number of engineers to work simultaneously on different aspects of a design. The cell libraries that are currently supported include 2μm double metal, 3μm double poly and 5μm high voltage cmos gate arrays, and standard cells. The facility to create new cells is also available and together with a training course and continual design support this provides a complete system for asic design.

Schematic capture is normally the first step of any design process. The circuit can be entered graphically with just the cursor keys of the PC or with a mouse connected to a serial port. There is an easy to read menu that reacts instantly to any keyboard inputs. The software also checks as early as possible for any incorrect inputs or design infringements. This correct-by-construction method means that a valid design can be produced ready for simulation within a very short time.

The output from the schematics editor can be a netlist for either the logic simulator or the P-Spice program. Apart from the netlist output, the schematic can also be printed on dot matrix printers and also a range of graphics plotters which includes the Hewlett Packard range of HP-GL plotters.

If Spice simulations are currently being done on a Vax machine it is possible to use the schematics to first generate the graphical representation of the circuit and then, with the aid of the Sceptre utilities, to transfer automatically the data to the Vax host computer and invoke the Spice job submission.

The schematics capture programme supports full hierarchical design so, if necessary, the range of analogue and digital cells contained in the current AMS libraries can be simulated at the transistor level and the electrical characteristics can be modified to suit your own requirements.

A Netlist Extraction Trace program essentially checks the schematic for any errors that would cause the simulator to behave incorrectly. This includes checks for open circuits, outputs shorted together and so on. The files generated by the Trace programme are: CIRCUIT.BIN, the binary representation of the circuit, CIRCUIT.BLT, the netlist in ascii text format and CIRCUIT.PAT, a basic template file for controlling the simulator.

The AMS simulation programme includes unit delay and full timing delay modes. In the unit delay mode the individual propagation delays of each cell in the library is not taken into account. This results in a faster simulator run time and so enables the designer to de-bug the circuit functionally before progressing to the timing simulation mode. This second mode takes set up and hold times into consideration as well as extra delays due to interconnect obtained from the layout database. The input waveforms that are required to exercise the circuit are defined in the CIRCUIT.PAT file.

The format is similar to that of the testers resident in the factory in Graz. This means that it is easy to transfer the results of simulation to, say, a Sentry tester with very little effort.

Simulations can be performed under best and worst case conditions and also at various voltages and temperatures thus providing the designer with a good indication of the final device performance.

A post processor, Display, allows the designer to examine the simulation results either graphically in timing diagram format or in truth table representation. This can also be output on to plotters and printers in the usual way.

If the designer has drawn the schematic using analogue components there is the option to run P-Spice. This is a PC version of the popular analogue simulation package and is provided by Microsim. The only extra hardware that is required is a maths co-processor.

The input to the P-Spice program is in the form of a normal ascii netlist which is automatically generated from the schematic. The output results are displayed graphically using a user-friendly interface and, as with all software modules, can be plotted on dot matrix printers and pen plotters.

The layout for the i.c. can be performed on the PC or, if the database is large, it can be performed on the Vax machines in Austria. In this case it is still possible to load layout information back on to the PC if slight modifications need to be implemented. At all times the basis on which the layout is performed is that of netlist consistency. The layout can be checked for design rule violations, power supply shorts and layout to logic consistency.

Once the design has been completed and a test file has been produced it is just a simple matter of sending a floppy disc to a local design centre. This will then automatically be transferred in the factory to the photomask machines and production testers.

Further details: Colin Sutlieff at AMS, 0793 37852.

SEMICONDUCTORS

IN-HOUSE GATE ARRAY DESIGN

Whatever proportion of asic design is handled in-house, here are some points to consider when choosing design tools

There are a number of stages to the design process that can be performed either in-house or at the gate-array vendor's design centre, depending on the cost trade-offs and competence of the designer. The costs involved in these trade-offs differ widely from vendor to vendor and are not easily generalized.

The first stage of the process is schematic capture. It is possible to buy very cheap schematic capture systems for PCs – less than £500. Before considering such a purchase, designers and managers should review the availability of gate-array design kits that are supported by vendors on the system. Often designers need to select different arays for reasons of speed, capacity, cost or availability, and the schematic system needs the flexibility to support multiple vendors. Schematic entry is normally handled in-house by most designers, although vendors and design bureaux offer rental facilities on such systems. The system selected must be capable of handling hierarchy easily, otherwise the design task is made extremely difficult.

Once the design is entered and compiled, the more powerful systems offers design check software. This checks the design for such things as excessive fan-out, exceeding gate capacity, incorrect buffering to the outside world, and ensures that a lot of the time and money is not waste in debugging circuits that cannot be manufactured.

The output from the schematic/DRC steps is a netlist in the vendors specific format – although the emergence of EDIF as a standard interchange format will simplify this stage in the future. Today the designer still has to consider the ease with which the necessary netlist can be extracted from a system. Again, the availability of vendor-supported netlists should be carefully researched before investment in tools.

For companies on their first asic design, this is the point at which many prefer to hand over the design responsibilities to the asic vendor, and in conjunction with an engineer from the vendor, take the design through simulation on the vendor's mainframe. There is obviously a significant cost associated with this. For the majority of designers, the simulation is handled with in-house workstations. As with the schematic libraries availability of logic libraries – to include functional behaviour, timing and loading effects – from the vendor is critical. Libraries can sometimes be offered by the workstation vendor, but take care before adopting this path; confusion may arise if there are errors in the library, and the rate at which the library is updated with new features offered by the gate array manufacturer may be significant.

Most engineers adapt to the concepts of simulation easily, but be careful when reviewing different simulators. A demonstration of a simulator can make it look easy and foolproof to use, but a benchmark should be considered on a prospective purchase for the engineer to try the tool in anger. Ease of use, speed, accuracy and integration with the schematic (i.e. ease of debug) should all be examined, as should the capability of the simulator to handle the spread of delays through the various paths.

While the circuit is being developed, think about the testability of the design – this is an area that often causes the biggest problems in a first-time design. Many p.c.b. designs are completed without significant thought for the testability of the design, not normally a problem when the design is not tested on a.t.e. and all nodes are easily available to logic analysers to trace faults. With an asic design, this is not the case. Nodes are only visible from the pins of the asic, and the designer has to develop a set of test vectors that will give a high assurance that the manufactured product is free of defects. Fault simulation, testability analysis and design-for-test are concepts that are often new to the designer, so access to tools to help in this area are therefore very important.

When simulation is completed the design is laid out either at the vendor's design centre or using automatic tools supplied by the vendor. An important part of the design flow is then the post-layout simulation, so check this out before buying a simulation tool – the effects of the layout parasitics can often cause a seemingly good design to fail in reality.

The choice of design tool and the decision of when in the cycle to pass the design to the asic vendor will be different for each individual company. There are a range of cost/performance options available, together with the options of general-purpose c.a.e. software versus vendor-specific software. Experience has shown that going for the cheapest possible solution at the start may in fact cost more in the long term.

When considering tools for asic design, companies should carefully consider the areas of performance, integration, functionality and upgradability. Whilst it may not be economically justifiable to buy tools to cover the whole spread of schematic capture, simulation and test development at the beginning of the first asic design, the capability to add easily to the in-house toolset as required is very important.

Tom Carlstedt-Duke is N.European technical manager for Daisy Systems

1: SCHEMATIC CAPTURE

- Will the company be able to select a different asic vendor in the future should the need arise? What is the number of asic vendor kits available?
- Can the system support hierarchial design easily?
- What is the capacity of the system for large designs? Though the first asic design maybe small, later ones often build rapidly in size and a new tool may have to be purchased.
- Can the system be used for automating the schematic entry associated with the non-asic pieces of the design? Is there library support of commercial parts?
- How easy is the system to learn and use?
- How open is the system for users to access the database?
- Does the system support design rule checking and netlist generation?
- What local technical support does the company offer to assist the user on the system?

2: SIMULATION TOOLS

- Is there support for many different vendors with full simulation and timing information?
- Can the system support simulation of low-cost asic alternatives (p.l.d./l.c.a.)?
- Does the system cope with load-dependent and layout-dependent delays?
- Is there tight integration between schematics and simulation to make debug quick?
- How easy is it to learn and use the system?
- Is it easy to generate stimulus patterns?
- Can the simulator be expanded to handle multiple asics together with commercially available parts? This is important as most redesigns are caused not by mis-design of the asic to a given spec, but by the asic not working correctly either logically or in timing with external logic.
- Are there any expansion paths for accelerating the simulator speed? This is necessary when larger multiple asic designs are considered in the future.

SEMICONDUCTORS

GALLIUM ARSENIDE ON SILICON

For a long time silicon has been the only useful material for integrated circuits fabrication; its dominance in the world semiconductor market is illustrated by the proliferation of silicon v.l.s.i. circuits. Gallium arsenide has recently drawn the attention of semiconductor researchers because of its unique light-emitting properties and high-speed capabilities. However, combining the two materials in a form suitable for integrated circuits was not possible until the growth of device-quality gallium arsenide films on silicon substrates was successfully demonstrated.

For more than two decades researchers have been interested in the growth of GaAs layers on silicon substrates and the properties of GaAs-Si hetero-interface[1]. Early attempts were unsuccessful because the material properties of gallium arsenide and silicon differ. First, the spacing of atoms in gallium arsenide and silicon crystals is mismatched by around 4%. Although this difference may seem insignificant, the growth of high quality epitaxial films requires a precise alignment of atomic structures. Trying to align each gallium arsenide atom and silicon atom at the interface would leave an extra silicon atom for every 25 atomic pairs, which introduces material defects that can destroy the performance of electronic devices.

And second, whereas silicon crystal consists of a homogeneous array of silicon atoms, a gallium arsenide crystal contains two different atoms placed in alternating positions. These alternate positions must be precisely maintained at the interface. It is for these reasons that the growth of high quality gallium arsenide films on silicon substrates had to wait for the recent development of growth techniques – molecular beam epitaxy in particular – that allow precise control of the placement of atomic layers.

There have been two important findings in the last few years that have enabled growth of high quality gallium arsenide on silicon. One is a technique called two-step growth developed by Akiyama and others at Oki Electric[2]. In this, the first thin gallium

The marriage of the two most important semiconductors, silicon and gallium arsenide, is now possible in the form of device integration on a single wafer.

arsenide layer, typically 0.1 microns thick, is grown at a low temperature, around 400-500°C, compared to the growth temperature for the rest of the gallium arsenide layer which is around 600-700°C. The total film thickness is typically 3-5 microns. This two-step growth technique gives gallium arsenide films of good surface morphology.

The other important finding by Fischer and others at the University of Illinois[3] is the use of a silicon wafer whose surface is not exactly aligned to the crystallographic plane, but tilted by only a few degrees (3-5°). This tilting helps coordinate the stacking of gallium and arsenic atoms onto the silicon surface, although a detailed mechanism is not yet known.

With these techniques it is now possible to routinely grow high quality gallium arsenide films on silicon substrates. A variety of gallium arsenide-based electronic devices on silicon have been demonstrated by various groups in the U.S. and Japan. The performance of these devices is usually comparable to similar devices made on conventional gallium arsenide substrates. For example, a field-effect transistor which can operate up to 55GHz has recently been demonstrated[4].

But the real question was whether this material would be good enough for i.c. fabrication. This was answered by Texas Instruments[5] with the demonstration of the first large-scale i.c. using gallium arsenide-on-silicon wafers. This contained more than 7000 transistors, and showed that one can not only make working transistors using this material, but can expect them to simultaneously operate in a very uniform manner.

An even more significant achievement is the demonstration of a room-temperature continuous operation of a gallium arsenide-based semiconductor laser diode built on a silicon substrate by a team from the University of Illinois, Texas Instruments and Xerox[6]. Since silicon cannot inherently emit light, having a gallium arsenide light-emitting laser on a silicon substrate is paramount to giving silicon a totally new capability. This will be useful for applications such as optical fibre communication systems and integrated circuits where signals can be transmitted by lightwave.

The performance of light emitting diodes is very sensitive to material defects, and until this achievement researchers were not able to reduce the number of defects sufficiently to operate the gallium arsenide diodes on silicon substrates continuously at room temperature. The combination of gallium arsenide and silicon gives each material a new capability which cannot be obtained by single materials alone.

The successful growth of gallium arsenide films on silicon substrates has enabled many gallium arsenide-based electronic and optical devices to be fabricated on silicon substrates, and in the near future this will lead to the combination of integrated circuits and optoelectronics circuits made of gallium arsenide and silicon.

Dr Hisashi Shichijo, of Texas Instruments central research labs, Dallas, reported on developments on GaAs on silicon at the 1988 Americal Physical Society meeting in New Orleans.

GALLIUM ARSENIDE ON SILICON ATTRIBUTES

This new technology is obviously not without its problems but the significance of its attributes justifies worldwide research on this topic. In the UK Philips, GEC & Plessey are known to be working on it.

- It allows the integration of both digital and optoelectronic signal processing on a single chip.
- It allows the possibility of microwave and digital and/or optoelectronic signal processing on a single chip, provided the r.f. loss associated with a Si substrate can either be reduced or can be tolerated.
- Silicon has a better thermal conductivity than GaAs which may make GaAs on Si the preferred technology for power devices.
- Large area GaAs wafers (>4in) will become available quicker if formed on a Si substrate than if we have to wait for the development of large diameter GaAs boules (4" GaAs on Si wafers are commercially available now).
- Si is a lot less brittle than GaAs and hence GaAs-on-Si devices may be easier to process and have a higher yield than all GaAs devices.
- Si substrates are considerably cheaper and more consistent than GaAs.
- The last three reasons may make GaAs on Si devices cheaper than all GaAs devices.

1. T. Nakano, *Jap. J. Appl. Phys.* vol. 6, (1967), p.854.
2. M. Akiyama et al., *J. Crystal Growth*, vol. 68, 1984, p.21.
3. R. Fischer et al., *J. Appl. Phys.* vol. 58, 1985, p.374.
4. M.I. Aksun et al., *Appl. Phys. Lett.* vol. 49, 1986, p.1654.
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6. D.G. Deppe et al., *Appl. Phys. Lett.* vol. 51, 1987, p.637.

BBC portable radio project

Wanted: manufacturers to produce an RDS volksradio.

After the BBC Microcomputer, the BBC radio set. Proposals have been invited by BBC Enterprises, the commercial offshoot of the BBC, for the manufacture of a portable radio to carry the BBC's logo. If the project succeeds, the result will be the first badged BBC radios since the 1920s, when even headphones had to carry a BBC licence sticker.

A detailed technical specification for the new receiver has been drawn up by the BBC's engineers. Set-makers were given copies at a London seminar in April and are considering their response. BBC Enterprises hopes a prototype will be ready for demonstration to the public at the BBC Radio Show, a promotional event to be staged at Earls Court this autumn (30 September – 9 October) and it plans to have sets on sale next year.

Proposals from the industry will be assessed by the BBC not just on set performance, but on marketing, distribution and promotion criteria too.

Motivating the project is the BBC's belief that millions of listeners use radio less than they might because of difficulties with reception. Although some 11 million radios are sold in Britain each year (there is a total installed base of 88M), too many of these show serious deficiencies in performance, and come nowhere near meeting the CCIR specifications on which transmitter planning is based. They are difficult to tune, especially on v.h.f.; they lack sensitivity; they suffer from overloading by strong signals. And many give a sound quality which fails to do justice to the work of programme makers.

RADIO DATA SYSTEM

A key feature of the new specification is the use of the RDS radio data system, a programme-labelling scheme designed to eliminate the tuning difficulties which so perplex most listeners. The BBC's radio will have 12 or more push-buttons for instant access to the various networks and local stations: when a button is pressed, the receiver will decode the data signals and find the correct frequency without further intervention by the operator. If the transmission fades or fails, the set will automatically seek an alternative frequency carrying the same programme.

Receivers for RDS are already beginning to filter through to the market. Volvo has launched an RDS car radio and Grundig a hi-fi receiver, though apart from the BBC proposals there is little sign yet of portable RDS sets. Receiver chips for RDS are being produced by Blaupunkt-Werke of West Germany at a quantity price of about £5. Blaupunkt's hybrid device, which is also being used in the BBC's own monitoring receivers, accepts the multiplex signal containing the 57kHz RDS subcarrier and produces a bit-stream plus the recovered clock signal. But for anything beyond the most basic RDS functions, the decoder must also include a processor to control the tuning and manage the display.

In the BBC's proposed receiver, the display will show waveband and frequency, a programme service name of eight characters (for a station with RDS), and whether the programme is mono or stereo. RDS programme identification codes will have been pre-loaded into the set's memories during manufacture so that it will work as soon as it is unpacked. But conventional tuning or band-scanning facilities will ensure that, without RDS signals, it still works in the ordinary way.

RDS signals are now carried by all BBC f.m. stations in England and by stations in the IBA network; most countries in western Europe intend to install RDS within the next year or two. Since last year BBC stations have carried a basic set of RDS signals, including tuning information and clock time, but a pilot service of additional features began on Radio 2 in April. The system is managed by a DEC minicomputer at Broadcasting House in London.

R.F. PERFORMANCE

Frequency coverage of the BBC receiver will include the v.h.f./f.m., m.f. and l.f. broadcast bands. On v.h.f., sensitivity must be good enough to provide a weighted signal-to-noise ratio of 40dB (mono) for a signal of 30dBμV/m. To guard against the irritating 'birdies' which often mar reception, in particular that of Radio 3, the engineers have proposed 70dB of protection against interfering signals spaced 2.2MHz and 4.4MHz from the wanted carrier – the separations employed for the BBC national networks. Single-signal image rejection must be better than 50dB and in-band multiplex rejection (SCA) better than 55dB. Selectivity must conform to CCIR Recommendation 412.

On a.m., minimum sensitivity must be sufficient to achieve 30dB weighted s/n for a field strength of 54dBμV/m. No coverage of the h.f. spectrum is proposed, though it is known that the BBC External Services has considered separately the idea of a BBC-badged receiver aimed at World Service listeners abroad.

First RDS receiver to go on sale is the SR-701 stereo car radio (above) made by Volvo. This v.h.f./m.f./l.f. set also has a scan function by which it memorizes the six strongest stations on each band. Pressing the ck button displays clock time read from the RDS signal. The tp button makes the set search for a station which identifies itself as carrying traffic information. Price is £512 plus v.a.t. and installation.

AUDIO QUALITY

Although the receiver is aimed at the ordinary listener rather than the audiophile, an important part of the BBC specification deals with audio performance. The cabinet, which is likely to have a volume of at least four litres, will be of dense material and as airtight as possible. A bass-boost control giving up to 12dB of lift below about 80Hz is required, and a treble lift and cut control may be provided too.

A set designed to the BBC's specifications would be unlikely to be among the cheapest on the market; but BBC Enterprises believes a niche exists for it. Retail price could be £70-£100. Enquiries and business proposals should be addressed to BBC Enterprises' head of new business development, David Safir, at Woodlands, 80 Wood Lane, London W12 0TT; telephone 01-576 0555.

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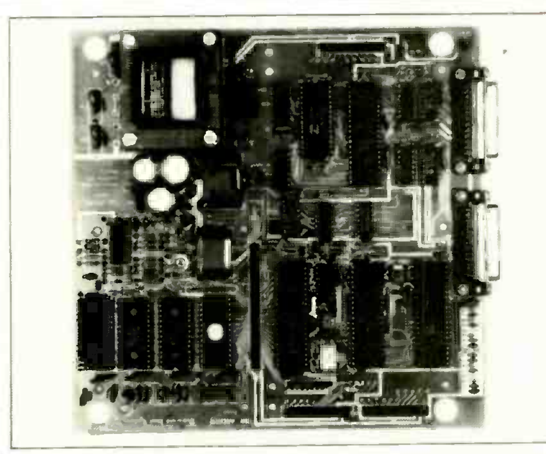

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Stretching the spectrum

Reports from the annual conference of the Mobile Radio Users' Association, held at the end of March at New Hall, Cambridge.

RICHARD LAMBLEY

At the Department of Trade and Industry, the policy of greater co-operation with the radiocommunications industry continues to show results. Senior staff from the Radiocommunications Division were once again present in force at the MRUA conference, and indeed formed the panel of speakers for the whole of the first session. But for the pressure of last-minute parliamentary business, they would have been led by their Minister, John Butcher. In his opening speech, read to delegates in his absence, Butcher opened the question posed in the conference's theme for this year: the matter of whether mobile radio was now enjoying a feast or bracing itself for famine.

With both Band I and Band III lately cleared of television broadcasting, with two national trunked mobile radio networks launched in the past few months, and with regional systems now opening, the supply of channels might appear sufficient to waft mobile radio into a golden age of an almost unlimited expansion. But the Minister warned, "You should not assume that there will be any less pressure to find more efficient ways of getting mobile radio across."

First of the speakers from RD was Mike Coolican, whose presentation examined the current level of occupancy of mobile radio channels. Despite heavy overcrowding, especially in the London area, he said that some channels were being wastefully misused: "Monitoring suggests that even at busy times, the actual message content of channels is not all that might be desired". Some calls occupied airtime without passing information, some were terminated before reaching the end of the message, leading to wasteful repeat transmissions, some were never answered at all. Foul language, c.b.-style abuse and music had all been heard by RD's monitors. Information provided by system operators had shown that only some 15 minutes of the busy hour were usefully employed.

But if operator discipline was often poor, so too was that of licensees. Coolican showed a slide containing results of 1400 inspections of mobile installations. Just over half had been found satisfactory; but among the others, inspection revealed 134 unused systems, 114 with equipment irregularities, 46 with frequency irregularities, 96 under-recorded mobiles, 133 base-stations which had been moved without authorization (by 25 miles in one case!) and 100 using unlicensed modes.

Coolican accepted that the present situation was in part due to previous regulatory policies. Even so, a potential shortage of spectrum faced the mobile radio industry because of the rapid emergence of new classes of user. Courier services had used up half a megahertz in only 18 months and needed more; their need would increase further if the Government deregulated letter carriage. In the US, a wristwatch radio-pager was to be launched at about $100. One could imagine the impact of such a product on the demand for paging spectrum. The telepoint service for second-generation cordless telephones would be launched this year, he said. "Virtually all telephone users might want cordless, 80% might want telepoint and that would mean 20 million domestic customers."

Coolican concluded his address by generating some agitation among the new Band III users. RD's policies for maximizing the use of the spectrum would not necessarily embody spectrum pricing as envisaged in last year's CSPI report (see *E&WW* July 1987, page 677), but they could well involve service providers charging for airtime. "Free airtime is not necessarily in the user's true interests", he said.

At present, only the GEC network charges for airtime. During a later session devoted to Band III, it was to become apparent that other operators have avoided charging up to now for reasons connected with marketing. A flat rate charge means that customers know exactly what the system will cost them to use; and by exacting payment in advance, network operators can avoid bad debts.

No decision on implementing the CSPI report has yet been made, though the DTI is understood to be assembling various options for consideration.

Next, Mike Goddard of RD discussed the question of where new spectrum would come from. Of the region most useful to mobile radio, 30-960MHz, 40% was occupied by broadcasting; 13MHz was aeronautical, 18MHz maritime; 276MHz was reserved by Government, largely for military use; and 152MHz was available for civil land mobile radio on a primary basis. The possibility of bandwidth-halving in television broadcasting (to 4MHz channels) had been considered, but might not be practicable: high-definition tv and high resolution video recorders [e.g. S-VHS] were just around the corner, apparently in response to user demand.

One apparently promising source of new channels was the extensive military allocation, consisting largely of valuable v.h.f. spectrum. Goddard said he had been through the channel plans in detail: he had begun very cynical, but was now partly convinced that they were reasonable. And it would take a long time to make any changes there.

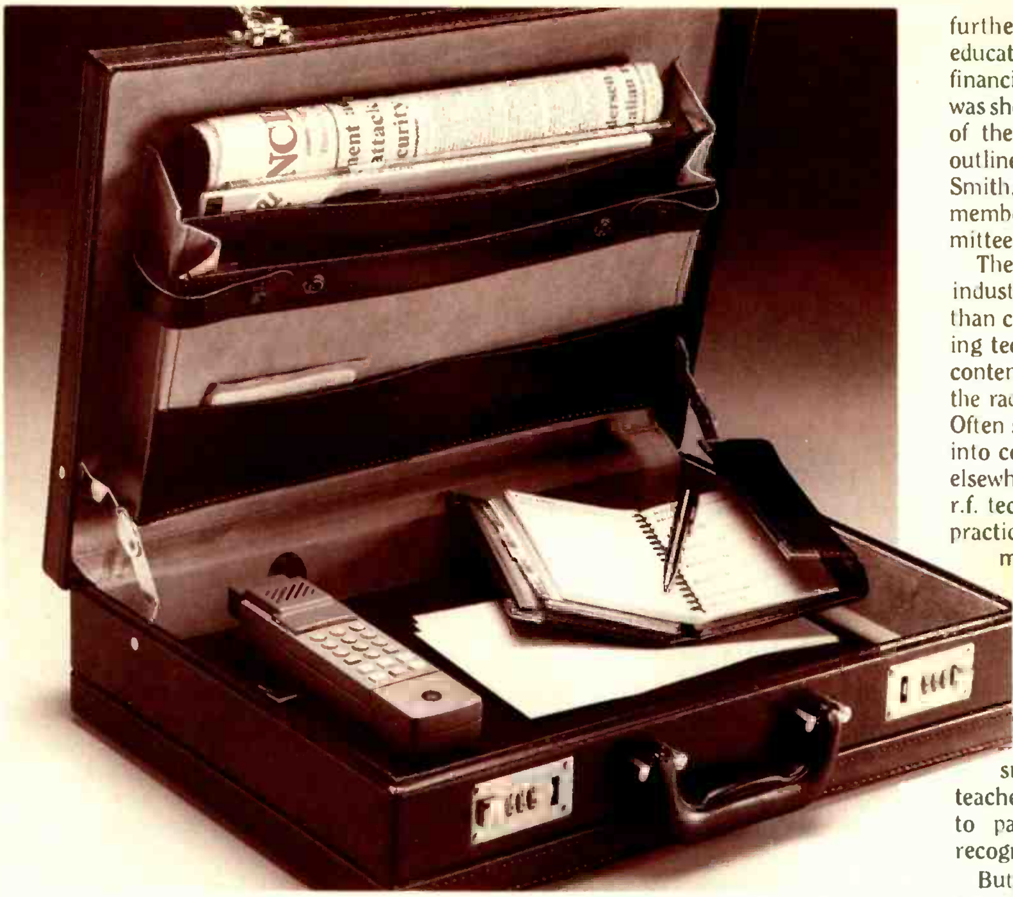
Another area where change would be difficult to contemplate was in the aeronautical and maritime bands, because of the huge number of installations.

Strategies for the future could therefore include using channels on a shared basis with the military; promoting greater spectrum efficiency; and the more effective loading of existing channels. This might mean favouring data rather than voice communication. In the longer term, moves towards personal radio communications and mobile satellite communications would mean we could not confine ourselves to bands below 1GHz.

Preparations were now afoot for a proposed World Administrative Radio Conference for 1992 to discuss allocations in the 1-3GHz region, following difficulties which had arisen at the 1987 conference out of conflicting demand for mobile satellite services at 1.5-1.6GHz. To make the most of this valuable opportunity it would be necessary to overcome some of the conservatism which existed internationally. A final decision on whether this meeting would take place would be made by the ITU in the summer of next year.

The technology of mobile radio, and the influence of regulatory activity, were examined by the third RD speaker, Olly Wheaton. "It is the DTI's policy", he said, "to minimize the burdensome regulatory constraint where possible, and to encourage competition in the market place to flourish". Through the DTI's work in developing standards, the UK now had a lead in trunking technology: "Other countries, Ireland, Germany, France, now wish to use the MPT1327 protocols for similar systems. We may end up with a *de facto* standard, who knows?"

But the creation of standards for trunked radio and the forthcoming pan-European cellular system had been hindered by problems over intellectual property rights: "Next



CT-2 cordless telephone by Ferranti Creditphone. Marketing people predict some three million CT-2 users by 1995.

time we will talk out IPR first, technology second". (See also Telecomms Topics, page 569.)

However, work on national telecommunications standards might increasingly be devolved to outside organizations. The Civil Service generally was considering the use of agency bodies, said Wheaton. "The lease on Waterloo Bridge House runs out in two years, and this could coincide with other organizational changes."

Among the technological possibilities Wheaton outlined was the prospect of sharing low-power applications with other services. Spurious emission limits for interference from microprocessors and so on were much higher than those for radio equipments. Permitted local oscillator radiation from television sets was also high: you could get 2mV/m three metres from a television, 8MHz wide. "If information equipment can radiate at this level, why not use these frequencies for broadband local communication?", he asked. Spread-spectrum techniques could help avoid interference.

During the panel session which followed, a questioner pointed out that, despite all the moves towards deregulation, the process of spectrum planning was still closed to users. Responding for RD, Mike Goddard said, "I fully accept the criticism". Spectrum planning, he added, had to be done more openly: users and operators had to be brought in. But it would still be necessary to harmonize with other European countries. RD was looking at the possibility of a forum or consultative committee to look at proposals before they were taken too far, but it was too early to give any details.

Other points from the floor dealt with more immediately practical matters. One was from an operator who had suffered interference problems, but had been told by a Radio Investigation Service inspector that frequencies used by adjacent sites were confidential and could not be divulged. Another speaker emphasized the need for more information, arguing that a list of who had what channel would promote the efficient use of frequencies. Coolican replied that the matter was now the subject of a ministerial decision; making a database available was an option that was seriously being considered. Goddard added that the DTI did not have overall charge of the whole spectrum; it could make Band III information available, but operators wanted confidentiality. In the US the FCC made its list public, but found tremendous difficulty in keeping it up to date – to the extent that private users made their own lists and the FCC was buying them.

EDUCATION

One issue which could well inhibit the growth of mobile radio is the serious shortage of trained technicians. Everyone in the radiotelephone business seems to have pet horror stories of installation problems caused by ignorance: radio units which work only at night through having been wired to the car number-plate lamp, or r.f. connectors where the coaxial cable has simply been pushed into the connector shell, and so on. A further conference devoted entirely to education, and staged by the MRUA with financial and other support from the DTI, was shortly to take place (4-5 May); but some of the problems the industry faces were outlined in a presentation by Dr Colin Smith, technical director of PMR Ltd and a member of the MRUA's management committee.

The vast majority of staff needed by the industry, he said, were of technician rather than chartered engineer status. But intending technicians found that too little of the content of their training courses related to the radio interest which had drawn them in. Often students ended up being side-tracked into computers and finding lucrative work elsewhere in the electronics. Even where r.f. technology *was* taught, courses had no practical content: test equipment for mobile radio was not available in colleges. Regulatory matters such as type-approval were excluded or disguised because academics regarded these as governmental rules rather than educational subjects. The emphasis on computers over the last few years had snowballed to the point where new teachers coming in had no knowledge of r.f. to pass on. There was no nationally-recognized qualification in mobile radio.

But now the MRUA had worked with the Association of Marine Electronics and Radio Colleges to produce course options which had been validated nationally and would be available from this September. These were only a start, but AMERC could expand them if they were well received. The MRUA also hoped to interest the City & Guilds Institute and other colleges.

DIGITAL TECHNIQUES

Looming on the cellular radio horizon is the pan-European cellular system, or GSM, which was described by Ted Beddoes, technical director of Racal Vodafone and lately seconded to the DTI to advise on Eurocellular matters. GSM will ultimately replace the seven existing systems in Europe, including the UK's TACS (though TACS is unlikely to be switched off before the years 2005-2010). Intensive activity is taking place within CEPT to define the system. "GSM is seen by the EC as important for its barrier-free policy for 1992", said Beddoes.

Basic features of the system, he said, would include the use of digital voice coding at 13kbit/s per channel; time division multiple access, with time-slots of slightly less than 1ms; eight channels per carrier with two-frequency duplex, and a gross bit rate of 270kbit/s (including sync, training-in and error checks); and a channel spacing of 25kHz per channel (200kHz overall), which would be the same as for present-day cellular. Frequency-hopping, together with the digital modulation scheme, would enable the system to tolerate a lot of interference and so make possible a high degree of frequency re-use. All channels would be usable at all sites, though not simultaneously. Satisfactory bit error rates would be achievable with a carrier-to-interference ratio as low as 8dB. A recording played to delegates of the speech quality obtained over an experimental link with a mobile test-bed being driven around London certainly seemed to support this prediction.

Provision has further been made for half-rate voice encoding, which could allow system capacity to be doubled. Data transmission will also be possible: GSM will handle data at rates from 300 to 9600bit/s with full error correction (FEC or ARQ modes), and without the need for modems. ISDN features including text and images will all be possible, as will facsimile – a group 3 system, buffered to avoid problems of synchronizing the transmitter to moving parts in the receiver.

Somewhat closer at hand is the emergence of CT-2 cordless telephones, expected to reach the UK market in just a few months' time. Barry Moxley of British Telecom Mobile Communications spoke of prospects for the new system, the first of its kind in the world.

CT-2 telephones neatly avoid the problems of having transmitter and receiver in the same small unit by the use of a ping-pong technique borrowed from military radio. Speech is time-compressed into brief packets, which are cross-fired alternately from either end on the same radio frequency. At the receiving end, the packets are stretched and reassembled to give full duplex speech.

Originally pitched largely at the domestic market, the CT-2 concept had grown into ambitious schemes for telepoints – short-range radio terminals situated in public places such as stations which will allow CT-2 users to make outgoing telephone calls as they pass by. Equipped with a CT-2 handset and one of the $100 pagers mentioned earlier, the subscriber on the move could have what amounted to a poor man's cellular telephone.

A problem, however, is that although several companies are involved in the CT-2 project, no standard air interface has been defined. Unless something can be done about this, it will mean that, say, a Ferranti telephone will not work through a BTMC Phonepoint, and *vice versa*. For cordless telephones in the executive suite or at home this will not matter, but as soon as telepoints begin appearing in public it will necessitate wasteful duplication. One example of the differences between the various manufacturers' specifications is in the length and data rate of speech bursts.

Research suggested a huge latent demand for CT-2 among those who used payphones, said Moxley. Prices would begin at £300 for a residential or office system; the handset alone might cost just £125. Some three million users were anticipated by 1995. Up to 5000 CT-2s could be supported per square kilometre, though interference might be a problem if 'incompatible' base-stations were present.

EQUIPMENT MAINTENANCE

Modern radio equipment has improved dramatically in its reliability; nevertheless the need for servicing shows no sign of fading away. A session of papers on the rather dull-sounding subject of maintenance yielded some interesting points.

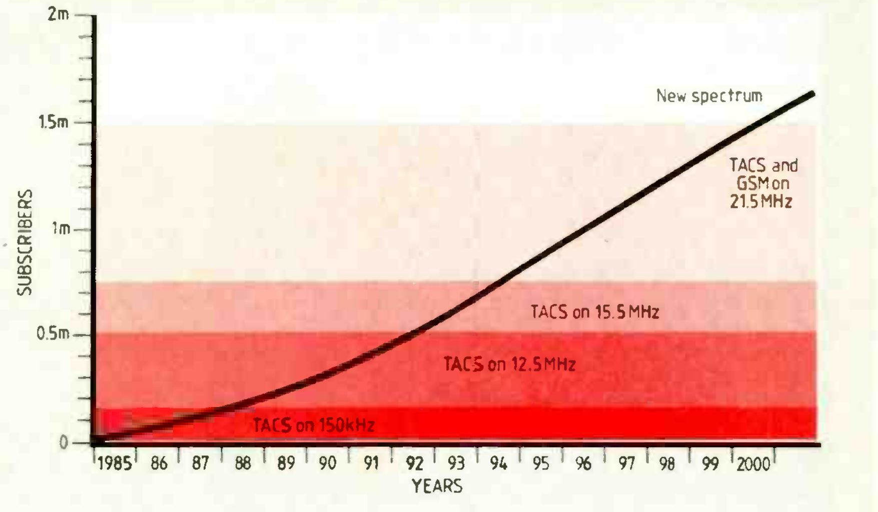
As Gary Fell of Motorola Communications International declared, servicing has increasingly become a question of how to repair a p.c.b. of surface-mounted devices when the board costs so much that throwing it away is not an option. Often the fault lay in a 15p resistor potted in a £100 sub-assembly. Field servicing was becoming a matter of changing a whole unit or sub-assembly; the fault itself could be dealt with later in the workshop. "What's important", said Fell, "is not how rapidly we fix broken things, but the equipment availability to the user."

A growing problem in mobile radio servicing was that of electrostatic damage to the complex semiconductors in today's equipment. "If you go into a service department, you should now expect to see the staff wearing some kind of strap", he said. Rarely did static cause a hard failure immediately in a semiconductor device. "But just walking across the carpet can set a time-bomb in that device... a tiny fuse-link waiting for the first small surge, minutes, hours or months later."

With hard failure rates approaching one in every ten years, many service calls now fell into the 'no trouble found' category. Reported faults were often of the 'finger trouble' variety – switches set in the wrong position. The proportion of such calls was bound to increase as equipment reliability improved.

One attractive prospect for the future was the use of remote fault diagnosis, using dial-up modems to interrogate the module directly. "This is a very powerful tool," said Fell; "the technician can then walk right in and put his finger on where the failure is."

• *Information about the Mobile Radio Users' Association is available from its secretary at 28 Nottingham Place, London W1M 3FD, telephone 01-400 1518. Further details of the educational conference mentioned in this article can be provided by Elke Hundertmark Associates, 01-938 2222 ext. 2101.*



Racal Vodafone's expansion plans for cellular radiotelephone service: much depends on the availability of further spectrum. Vodafone's rival, the Cellnet consortium, is equally ambitious.

Miniature broadcast receiver

This general-coverage receiver by Sony must be one of the most compact yet; certainly it is the smallest with synthesized tuning. Though scarcely larger than an audio cassette it provides continuous coverage from 150kHz to 30MHz (a.m. only) plus an f.m. range of 76-108MHz, with stereo listening on 'phones. The l.c.d. doubles as an alarm clock. Tuning is by direct frequency entry, by up/down buttons, band-scanning, or memory presets (ten of them). The ICF-SW1 comes as part of a

complete listening kit packed in a tough moulded carrying case, with a 120-page short-wave listening guide book, earphones, multi-voltage mains power unit, and an active antenna module with a lengthy reeled connecting lead. Internal power for the receiver comes from two R6 (AA) cells, which typically give 12-15 hours life; NiCd rechargeables work well too. Performance of the ICF-SW1 on h.f. is not up to big-set standards (strong signals can embarrass it), and the loudspeaker is – understandably – short on bass; but its sheer convenience for the travelling listener would easily outweigh any such drawbacks.

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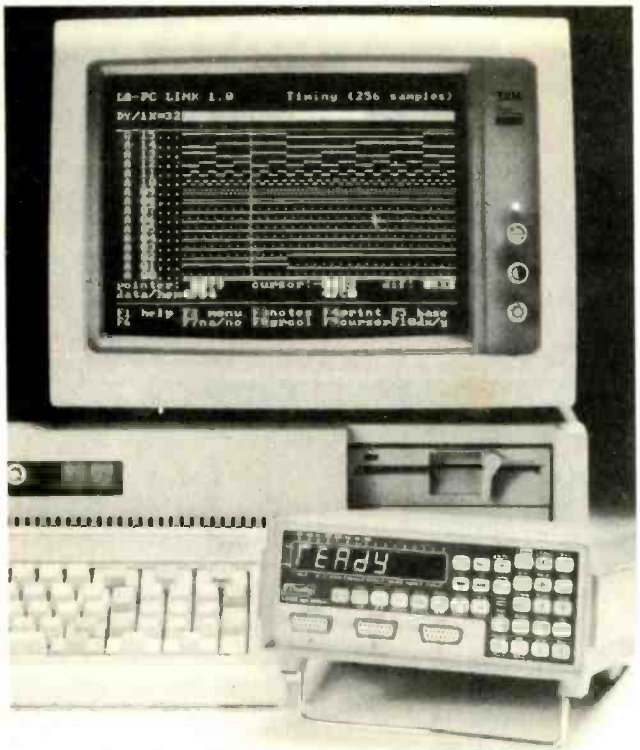

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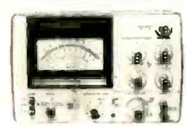

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TELEVISION BROADCAST

Preparing for dual channel sound

With the IBA expecting to be able to begin tests of Nicam 728 digital stereo sound early next year and to launch an operational service in the Crystal Palace, London and Emley Moor, Yorkshire service areas (together with those of their low-power relays) from autumn 1989, and with digital stereo also due on the BSB satellite by about Christmas 1989, it is clearly now time for the industry to begin producing programmes in stereo.

A one-day symposium 'The implications of dual-channel sound for Independent Broadcasting', organized by the IBA, provided a useful introduction to the technology of Nicam 728 and its advantages to the viewer, but also some indications that producing effective television stereo sound may not prove as easy as some people imagine. The hundred or so delegates were also left with an uneasy feeling that the receiver industry may emphasize to potential customers the high audio quality possible with the Nicam 728 system, without necessarily ensuring that their sets will do justice to digital stereo – much as in the past few receivers came anywhere near to providing the audio quality possible on plain, old-fashioned television mono. It is clear, also, that Nicam 728 decoders will add significantly to the additional cost of providing two audio channels and their associated loudspeakers.

Chris Daubney (IBA) said that while a technical working party is currently dealing with the technicalities of dual-channel sound on the ITV and Channel 4 terrestrial networks, it is important that programme makers, operations people and engineers recognize that it is the programmes that matter and that there exists a need for a sharing of thoughts on tackling stereo for the small screen.

Bob Wellbeloved (IBA) noted the competitive danger to the terrestrial channels posed by satellite channels where stereo is becoming the norm. Public awareness of stereo is marked by the success of CD records and the trend from a.m. to f.m. radio. The BBC had expected to begin an operational service using the Nicam 728 system this year until it was indefinitely postponed under its five-year plan, although tests were continuing occasionally from Crystal Palace. IBA had assumed that Independent Television would follow the BBC but now found itself in the lead and being pressed by the receiver industry to make the earliest possible start.

The entire ITV and Channel 4 transmission chain was at present geared to mono. The introduction of stereo involved changes in the studios, the distribution networks, the transmitters and the availability of Nicam 728 receivers. At present ITV's analogue intercity network used separate analogue audio distribution; Channel 4 had a digital sound-in-sync combined audio/vision network but this was mono only. "Conversion of these networks is a major and expensive undertaking" he said. The relatively new Channel 4 transmitters could be readily modified. New ITV transmitters being installed under Phase 1 of the current re-engineering programme were replacing the older high-power main transmitters unsuitable for stereo at the rate of six stations per year but the complete replacement of ITV transmitters would take several years.

By about 1990 it should be possible to provide stereo in all ITV regions, though not from all main transmitters. About 75 per cent of the population should by then be receiving Nicam 728 signals, but it will be the mid-1990s before full national coverage is possible, the actual date depending on the completion of the Phase 2 transmitter re-engineering project still in the early planning stage. Orders were being placed for stereo sound-in-sync equipments for both the ITV and Channel 4 distribution networks. Eventually it would be possible to abandon the present analogue sound links.

Peter Brice and Bernard Rogers, representing BREMA, outlined the implications of stereo for receivers and video cassette recorders, though it was unfortunate that Peter Brice used up most of the time allotted to BREMA with an over-the-top presentation that seemed geared to customers and dealers rather than broadcasters. Bernard Rogers, however, quickly described the design of decoder chip sets for Nicam 728 decoders while admitting that these seem likely to add some £12 to £15 (retail) to the cost of a stereo-sound tv receiver compared with the few pence of a decoder for the German two-carrier analogue stereo system.

It also appears that the industry generally is planning to provide sets with built-in rather than detachable stereo loudspeakers. This will inevitably limit the listening area for the optimum stereo effect, although possibly reducing some of the production problems in matching a wide sound stage to a relatively small picture.

As the independent producer Christopher Nupen (who has produced more than 50 music-based television programmes with stereo sound since 1972, for mono transmission) pointed out, stereo is not just a matter of adding width but also depth. He believes that the public is now more sophisticated in its appreciation of audio quality than it is generally given credit for. He warned that too little time is usually allotted in post-production for sound dubbing. For cinema film this may take weeks; in television it is often expected to be done in a day or a half-day. His presentations showed what can be done with care, and were the day's most convincing demonstration of the advantages of stereo reproduction.

Roy Drysdale (Limehouse) in considering the effects of stereo on studio practices commented: "After listening to the manufacturers I wondered why I wanted stereo. This afternoon I began to understand." The Limehouse studios were engineered for stereo five years ago. Stereo tolerances are low and he felt that "if you notice the audio on tv programmes it's wrong". The sound, he insisted, must be fitted to the picture. He agreed that dual channel sound will benefit some programmes, particularly music-based programmes, more than others. There was little to be gained from stereo for current affairs, etc. Discipline of operators had to be that much greater.

Mike Pontin (Thames) similarly agreed that while stereo benefits music, recording dialogue in stereo is debatable, although stereo can provide greater clarity. Stereo microphones with extended low-frequency response tended to be unsuitable for use in television studios where it is difficult to avoid studio noise. Additional production costs for stereo were an obvious concern to the companies; training in new techniques is very important. ITVA is arranging training courses.

Deryk Williams (S4C) spoke on dual-language opportunities provided by the time-multiplex of Nicam 728, although admitting that this is unlikely to take the place of good dubbing and subtitling and "does not of itself solve the problems of S4C".

Mark Yonge (Dolby) stressed that the dynamic range of sound and vision needed to be considered in relation to the different conditions in cinemas and homes. Material needed to be pre-viewed under suitable conditions.

During a discussion period, some of the practical problems in handling stereo sound effectively with existing technical facilities were aired, including the problems that might be involved in live broadcasting of snooker matches over several hours. There was also the feeling that broadcast managements, in their current drive for more economical production, would not appreciate the extra skill, care and time needed to get stereo sound right. "We know how to do it. The problem is that the industry has been a long time with mono. Getting the opportunity to do it right will need positive response from the top. Inventive people are feeling strangled. Getting sufficient time will be difficult."

In the second five years of stereo production for the cinema, productions were much better than in the first five years. In the early days there had been difficulties over preconceptions of what stereo ought to be – there had been expensive experiments that had often failed. The advantage to broadcasters, it was suggested, was that they now have a margin of time to experiment in private.

Television Broadcast is written by Pat Hawker.

Vehicle e.m.c.

The problem of interference to in-car-entertainment radios and to and from electronic subsystems in cars is increasing as the electronic complexity of motor vehicles rises sharply. The launch of such cars as the BMW 7 series, the Jaguar XJ6 and the Opel Senator has seen the European car industry move from a modest degree of electronics for engine management straight to cars routinely containing seven or more microprocessors.

Susceptibility to, and generation of, radio-frequency interference (r.f.i.) are still poorly understood by the vehicle industry and in the past have been largely ignored, with problems rectified only as they are experienced, at a stage too late to influence fundamental design considerations such as circuit-board layout and choice of logic families, etc. Understanding the mechanisms of r.f.i. requires a knowledge of antenna and transmission line engineering. Since the car radio is normally the component most sensitive to r.f.i., test methods that ensure there is no electrical interference to reception will automatically ensure that no on-vehicle electronic system is likely to interfere with any other.

These were among the points made by M.T. Crowther (Jaguar Cars) at an IEE colloquium 'Vehicle Electromagnetic Compatibility' chaired by Warren Gibbons of the Motor Industry Research Association. Even more vital from a reliability and safety viewpoint is that car electronic systems should be resistant to, and adequately protected from, strong electromagnetic fields from on-board carphones or when close to high-power broadcast, radar or communications transmitters. Keith Price (Jaguar Cars) described test methods for checking whole-car susceptibility based on a field of 50V/m at 30MHz, although he underlined the difficulties of making accurate whole vehicle measurements in test chambers.

K.L. Longmore (Lotus Engineering) similarly highlighted the problems posed by the increasing use of 'composites' such as glass-reinforced plastics rather than metal in vehicle construction. This is resulting in the need to use new techniques such as fillers (loading the resin with conductive particles), meshes/weaves (since composites are based on casing a strong mat in a resin, if the mat is made conductive it can form an effective screen) and surface coating, for example by making the gel coating of the g.r.p. conductive, or spraying with a conductive paint, or by sticking metal foil on the surface. Protection is needed against both electromagnetic interference (e.m.i.) and electrostatic discharge (e.s.d.) which he suggested "are probably the most effective killers of electronics modules in cars".

M.T. Crowther, in his tests on interference to sensitive, high-quality in-car entertainment equipment, has found that "most interference has proved to originate from clock harmonics, in some cases from the gate output, in others from the supply lines to the gate. In all cases interference has been reduced to acceptable levels by decoupling of i.c. devices and filtering of clock outputs or by reducing current rise time of the clocks by other means. Careful attention should be paid to the family of logic selected, the component layout, power supply busing and signal trace layout. The use of 'slow' logic such as c-mos 4000-series devices is recommended. If a faster logic, such as 74HC, is used, far more care must be exercised. It is not uncommon to see harmonics beyond the twentieth radiating from a module. In all cases of interference it was found that the system clock was responsible for narrowband interference, while data buses were responsible for broadband interference. Isolation of input/output lines from digital circuitry is important. Isolated digital and analogue power supplies should be used when mixing digital and analogue circuitry on the same board. Good power supply busing is characterised by low impedance and good decoupling over a wide bandwidth, achieved by maximizing the capacitance between the power lines and minimizing their self-inductance."

Keith Price noted that "Some components are susceptible [to r.f.i.] at relatively low power levels, but revert to normal operation as the power level is increased. No satisfactory explanation for this phenomenon has yet been found. The effect is sometimes referred to as 'windowing' and has been found to be much more common than would at first be expected".

K.L. Longmore reported that for shielding composites self-adhesive aluminium foil has proved effective for the low-volume production of Lotus cars. In the USA for high-volume production, an alternative approach has been to enclose the engine in its own metal box.

It should perhaps be noted that although 50V/m whole-vehicle tests should ensure adequate protection against fields likely to be encountered when driving in the vicinity of high-power broadcast or communications or radar transmitters, there could remain a need for caution when installing (or passing) high-power transmitters in vehicles (e.g. 400W p.e.p. output as permitted to UK radio amateurs for mobile operation). Isolated cases have been reported from the USA where r.f.i. disruption has created a serious safety hazard.

What happened to Picor?

While, as noted in the April issue, the idea that the restricted audio bandwidth of Region 1 a.m. medium-wave broadcasting could be extended by using a quadrature channel looks good only on paper, it is worth recalling an earlier proposal designed to improve quality within an unchanged bandwidth. This was Picor (pilot-controlled overtone reproduction) developed in the German applications laboratory of ITT's Component Group Europe, initially about 1972 but with later improvements described in 1974 (*EBU Review – Technical Part*, April 1974).

This divided the audio spectrum into a 'fundamental' band up to 4 or 6kHz, and an overtone band signalled to the receiver on a narrow low-level pilot (control) signal which, in a suitable receiver, controlled a generator to produce a series of discrete fixed frequencies at appropriate levels. The original system was effective on music but tended to result in speech sibilants; this defect was overcome by a control signal providing adjustment of the index of modulation depending upon the nature of the programme being transmitted. Compatibility with conventional receivers was achieved by taking advantage of the masking effect produced when the pilot signal controlling the receiver generator is placed adjacent to the upper extremity of the fundamental band.

It was claimed that test results "show a very appreciable improvement in quality, compared with a conventional broadcasting transmission having a bandwidth of 4kHz". In 1974 it was stated that work was in progress on a further modification of the transmission system, with a view to taking advantage of the possibilities of mos integration. The system was shown to be satisfactory not only for a.m. but also for s.s.b. and i.s.b. systems with bandwidths of only 4kHz, rather than the 9kHz of medium-wave a.m.

But little seems to have been heard of what happened to Picor since 1974. I cannot trace any papers on it having been given at IBC in the 1970s.

Erasable CD

Thomson Consumer R&D Laboratories in Villingen, FRG, have delivered to some professional recording studios and disc manufacturers working prototypes of their 'MOD' (magneto-optical disc) machines – a CD player that plays, erases and records. Thomson aims to become the first to market such machines although Sanyo Electric demonstrated a similar technique in 1984. With no physical contact between laser and disc, MOD is seen as an effective answer to DAT. Present playing time of each side of the double-sided discs is 54 minutes but Thomson aims to double this. An engineering production line is being set up at Villigen. If MOD is accepted as a world standard, so avoiding non-compatible machines, volume production will probably be in the Far East.

Radio Broadcast is written by Pat Hawker.

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RESEARCH NOTES

Glasnost, is it real? Well, what better way to find out than a fact-finding trip around the various institutes that comprise the USSR Academy of Sciences? To my surprise, the visit of a western journalist was not only tolerated but warmly welcomed, and wherever I went there was enthusiasm for improved East-West communication. Scientists and engineers talked freely about their hopes, their frustrations and the universal problem of resources.

Russian super television

Of the various institutes, one of the most prestigious is the Lebedev Physical Institute where, among other things, they are working on advanced opto-electronic projects. Head of the opto-electronics laboratory, Dr Yuri Popov, introduced me to one of his favourites, a laser television tube that could soon give projection tv the edge over 35mm film in terms of quality and projection screen size.

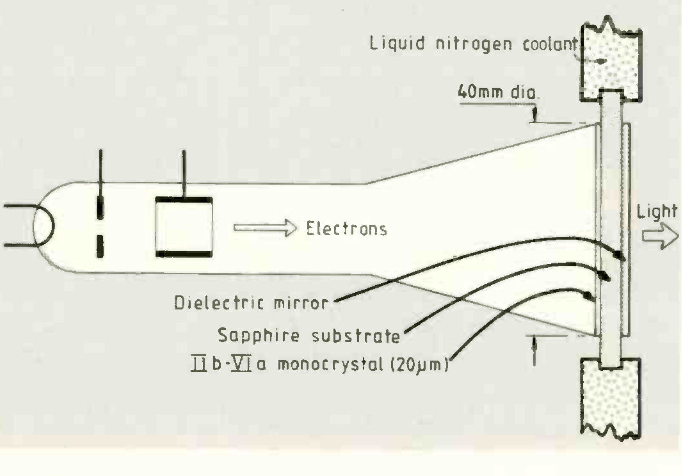
Long ago, working with British-made gallium arsenide (GaAs), Popov realised that it would be possible to make a laser screen to replace the conventional phosphor in a cathode ray tube. Such an electron beam-excited solid-state laser would have the potential to produce pictures of enormous brightness. There were two problems: first, the need to make the whole of the screen area from a single crystal of GaAs; and secondly, the fact that GaAs and other III-V compounds lase most efficiently only in the infra-red part of the spectrum – not much use for colour television!

A solution was eventually arrived at by using IIb-VIa compounds such as cadmium sulphide (CdS). Although needing new crystal-growing technology, Popov and his team created a laser tube with an effective screen area 4cm in diameter. The structure, as sketched out by him on a piece of scrap paper, is outlined on the right.

This CdS tube produces a red picture aproximately 10^4 times brighter than the red phosphor of a conventional projection tube. When projected through 35mm optics, the resulting $12m^2$ image can be as bright as a similar-sized cinema picture.

To produce a full colour picture, it is obviously necessary to have laser tubes for the other two primary colours as well. At the moment the Lebedev team have ascertained that laser tubes based on other IIb-VIa compounds will do the trick. Cadmium selenide and zinc selenide will produce reasonable green and blue images respectively. As yet, however, the crystal-growing technology still needs to be perfected for these colours.

Nevertheless the laser tube shows considerable promise, even if production is difficult and even if, at present, it's necessary to use inconvenient materials like liquid nitrogen to cool the faceplate. Dr Popov claims that with his existing red tubes, the electron optics are such that a resolution of 2500 lines can easily be achieved, much better than the performance of what he calls 'second generation' television.



Mendeleev, where are you?

At the other end of the scientific spectrum, far removed from the world of moving pictures, is the search for new elements – another area in which the USSR is pre-eminent. At the Institute for Nuclear Research at Dubna attempts are being made to create more of the so-called transuranic elements, artificial species with atomic numbers greater than 92 – that of uranium.

All the transuranics from neptunium onwards are inherently unstable and decay by spontaneous fission into lighter elements. In fact most of them have such a fleeting existence that their presence can only be inferred by a study of their breakdown products.

The creation of such superheavy elements, hitherto the province of US laboratories (whence berkelium, californium etc.), is now being actively pursued in a number of countries including France and West Germany. But the Russians are the only ones who now claim to have good evidence for the existence of element 110. Yuri Oganesyan and his colleagues at Dubna used a 265MeV cyclotron to accelerate ions of argon-40 and bombard a target comprising uranium-236. During such experiments all manner of reactions take place, often making it difficult to distinguish one species from another. Nevertheless the Russian team found a decay signature that was unlike that of any other element yet discovered and they now – two years later – firmly believe it to be element 110.

How far this process can go is an interesting question, because for many years physicists have predicted the existence of so-called 'islands of stability'. As atomic size increases, there is the possibility that rather than becoming increasingly unstable elements will last long enough to be useful. Where the first island of stability begins is a matter of some debate, but it could start with element 112. Clearly the Russian and others will be actively pursuing that goal. My only reservation is this: if transuranic elements of atomic number (say) 112-120 are stable, why haven't they been detected in some of those energetic regions of the universe where atomic nuclei are constantly being created in conditions far more aggressive than anything we can conjure up on earth?

Chips for frying

Over the last few years the spectacular development of high-temperature superconductors has obscured an almost equally important development, that of high temperature semiconductors. Hitherto virtually every solid-state device has had to be operated below 200°C, a constraint that not only keeps heat-sink manufacturers in business but which also causes enormous problems in inhospitable environments such as car engines, jet engines and much of industry.

The real problem is the small energy band-gap of silicon which means that, at high temperatures, electrons can jump from the valence band into the conduction band, destroying all semiconducting properties in the process. What is obviously needed is a material with a much larger energy band-gap, as well as physical properties that are compatible with the required application.

One such material, boron nitride, has already been used to construct diodes capable of operating at 530°C (Research Notes, March 1988), though the practical problem of attaching lead-out wires has not yet been satisfactorily overcome. Other possible materials being explored include pure carbon in the form of diamond films and silicon carbide, better known as the gritty material on emery paper.

Recently, reports have emerged of high-temperature silicon carbide transistors that will operate satisfactorily at temperatures up to 650°C. Robert F. Davis and his colleagues at North Carolina State University claim (*Science News* vol.132 no 25) that such devices have a performance comparable to more conventional silicon transistors operating at room temperature.

The secret of their success was to grow cubic crystals of silicon carbide on top of hexagonal crystals – the common sort used to make emery paper. Hitherto cubic silicon carbide had been deposited on a pure silicon substrate, leading to lattice defects because of the different inter-atomic spacings.

Transistors and diodes made from silicon carbide are now considered very close to com-

RESEARCH NOTES

mercialization; indeed Davis' group is said to have formed a company to develop and market high temperature diodes. They also intend to exploit their new ability to make high grade cubic silicon carbide in the direction of marketing that still-elusive device, the blue led.

One thing is sure: when high-temperature semiconductor devices become readily available in commercial quantities we shall see the application of electronic control systems in many environments that are now considered much too inhospitable. There is also the prospect of better high-frequency, high-power devices that don't go phut at the first sniff of mismatch.

Einstein rules O.K.

As any school-child knows, one of the tenets of Einstein's theory of Special Relativity is that the velocity of light is constant and does not vary with changes in the velocity or direction of its source. That view has however been challenged by some cosmologists who have suggested that the velocity of light could alter in some directions because of local variations in gravity or because of variations in the microwave background that permeates space. This radiation, first detected in 1965, is thought to be a remnant of the Big Bang that sparked off the creation of the universe some 17×10^9 years ago.

Sadly for avant-garde cosmologists, Einstein still remains inviolate, at least to judge from some experiments performed at Aarhus University in Denmark. Professor Ove Poulsen and his colleagues used a 10m particle accelerator to project atoms of the isotope neon-20 in a precisely controlled direction. Using a split laser beam, one half projected in the direction of the neon atoms and the other half moving against the stream, the team made simultaneous measurements of the velocity of the atoms, using changes in the frequency of the laser light re-emitted from them. From these figures they then calculated c, the velocity of light, to an accuracy roughly ten times greater than that of a satellite-based experiment performed in the USA in the late 1960s.

Of more importance than measuring absolute velocity, however, was the ability of this experiment to measure any changes that might occur in different orientations in space. This has never previously been possible because all the classic techniques from the famous Michelson-Morley experiment onwards have sent the light on a go-and-return path that cancels any directional effects.

In spite of this new opportunity to search for directional effects, Professor Poulsen reports that none has been found. He is however designing new equipment that will offer a further tenfold increase in sensitivity. If it is eventually found that c varies in different orientations in space, then the consequences for cosmology will be profound. Meanwhile it seems that Einstein can rest in peace.

... or can he?

Just over two years ago physicists at Purdue University in the USA publicized a paper in *Physical Review Letters* re-analysing the results of experiments carried out in 1922 by a Hungarian, Roland von Eotvos. The purpose of the experiments was to test the so-called equivalence principle – the proposition that all objects, regardless of their composition, experience the same effects of the earth's gravity. Eotvos concluded that gravitational acceleration was indeed constant, though he observed certain inconsistencies that he put down to experimental errors. To believe otherwise would be to challenge Einstein's Theory of General Relativity.

The Purdue analysis, conducted by Dr Ephraim Fishbach and his colleagues, suggested that far from being experimental errors, the discrepancies observed by Eotvos were in fact evidence of a newly discovered fifth fundamental force called hypercharge.

Physicists have up till now recognized the existence of four fundamental forces governing the behaviour of the universe: electromagnetism, gravity and the so-called weak and strong nuclear forces. The first two are mediated by massless particles – photons and gravitons – and can thus cross the immensity of the universe. The nuclear forces on the other hand are mediated by relatively massive particles such as pi-mesons and w-bosons and can hence operate only within the confines of the atomic nucleus. Nevertheless, in spite of the vast differences of scale, physicists have been striving in different ways to unite all the four known forces in a single mathematical description.

But what of the fifth force proposed by Fischbach? Hypercharge, if it exists, is a force intermediate in range between the nuclear forces and electromagnetism. Fishbach showed that it seems to have a maximum range of about 200m and – unlike gravity – operates on different materials in different ways. Also unlike gravity it manifests itself as a weakly repulsive force.

Since January 1986 when these findings were published there has been a flood of papers, all reporting similar experiments and all drawing slightly different conclusions. A somewhat sceptical editorial in *Nature* (vol.329 no 6137) asked: whatever has happened to the fifth force? But while the debate hotted up, another contender entered the ring. Experiments conducted by the US Air Force and reported at a meeting of the American Geophysical Union, suggest the existence of yet another force – an attractive though weaker one – that operates over a slightly greater range than the repulsive force. This could explain why different experimenters have arrived at different conclusions. It would obviously depend on the precise conditions that obtained in any given experiment.

So what are we to make of forces five and six, if indeed they exist? Conveniently, some new quantum theories of gravitation not only allow the existence of such forces, they actually require them. This of course does not constitute proof in the scientific sense and there are still some physicists who remain sceptical. Nevertheless an increasing number of experiments are turning up results that do seem to indicate something unusual. And with the possibility of missiles going ever-so-slightly off course there is no doubt that the US military will continue to maintain a keen interest in any deviations from common-or-garden gravity.

Word processing, human-style

Using a technique called position emission tomography, a team at Washington University School of Medicine in St Louis have been able to discover exactly what goes on in our brains as we speak words and phrases. By mapping changes in physical parameters in the cerebral cortex, they've shown that comprehension and the subsequent speaking of words require the use of widely scattered areas of the cortex. Areas involved in the reading and hearing of words have independent parallel access to the systems that generate spoken words or make associations between works such as nouns and verbs.

This finding (*Nature* vol.331 no 6157) is the result of experiments involving the precise measurement of patterns of blood in the brain, monitored by rapidly-decaying radio-isotopes in the circulation.

The conclusion that human 'word-processing' is a parallel activity differs markedly from the generally-accepted model developed in the nineteenth century. The latter assumed that during reading, words are always mentally converted into a silently spoken form before being understood. Only then – on this theory – is the data finally passed on to the brain's speech centre.

The new work done in St Louis now demonstrates clearly that the brain doesn't in fact process words in this roundabout sort of way. When we read something aloud, the visual centre recognizes the word and passes it straight to the speech centre without any mental 'hearing' or 'understanding' going on in between.

These findings are not only of theoretical interest to brain researchers, but also to doctors and therapists trying to understand disorders of speech and language. Maybe it will also be possible to adapt some of the resulting theory in the design of new architecture for electronic parallel processors.

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PS4B2S for Sony SLC20/30 etc	39.50
PS5B3S for Sony SLC8/C9 etc	49.50
Philips V2000	65.00

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Ferguson 3V16	2.75
Ferguson 3V22/JVC HR3360/3660	2.95
Ferguson 3V23/JVC HR7700	1.50
Ferguson 3V29/JVC HR7200	2.75
Ferguson 3V31/JVC HR7650	2.75
JVC HR3330/3600	2.75
Hitachi VT11/33	2.75
Hitachi VT5000	2.95
Hitachi VT8000	1.25
National Panasonic NV300/333/340	2.95
National Panasonic NV2000B	3.75
National Panasonic NV777	2.75
National Panasonic NV3000B	3.75
National Panasonic NV7000	2.75
National Panasonic NV8600/8610/8620	3.75
Sanyo VTC5000	1.50
Sanyo VTC5300	1.75
Sanyo VTC5500	2.75
Sanyo VTC9300	3.75
Sanyo VTC9300P	3.90
Sharp 6300	3.50
Sharp 7300	3.50
Sharp 8300	3.50
Sharp 9300	3.50
Sony C6	2.75
Sony C7	3.50
Sony T9	2.95
Sony SL3000B	3.75
Sony SL8000/8080	4.50
Toshiba 7540	3.50
Toshiba 9600	1.50

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UNIVERSAL TRIPLER	5.45
DECCA 30	6.35
DECCA 80	6.95
DECCA 100	6.95
DECCA 120	6.95
DECCA 1730	6.35
GEC 2040	5.45
GEC 2110	6.95
ITT CVC1-9	6.35
ITT CVC20/25/30	6.35
ITT CVC45	6.95
PHILIPS G8 (550)	6.95
PHILIPS G9	6.00
PYE 697	6.50
PYE 713 4 LEAD	8.50
PYE 713 5 LEAD	8.50
PYE 731/25	8.50
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RANK A823	6.95
RANK T20A	6.95
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SIEMENS EUROPA	7.50
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THORN 1600	5.45
THORN 3500	7.95
THORN 8000	6.95
THORN 8500	7.15
THORN 9000	8.50
THORN 9600	8.50
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TV13 STICK	1.25
TV18 STICK	1.10
TV20 STICK	1.40

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ELC1043/06 MULLARD	8.65
U321	8.25
U322	8.25
U324	11.00

THERMISTORS

VA1040	0.23
VA1056S	0.23
VA8650	0.45
VA1097	0.25

PUSH BUTTON UNITS

DECCA/ITT 6 WAY	7.95
DECCA 4 WAY	7.95
HITACHI 4 WAY	11.95
PYE 6 WAY	10.35
GEC 213 6 WAY	9.50
GEC 2110 6 WAY	10.50
GEC 6 WAY	10.50
G8 (LATE) 6 WAY	14.50
ITT 7 WAY	10.50
NEONS 7 WAY	12.50
RANK 4 WAY	10.50
RANK 6 WAY	10.50
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100MA 200MA 250MA 500MA 1Amp 1.25Amp 1.5Amp 1.6Amp 2Amp 2.5Amp 3.15Amp 4Amp

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100MA 150MA 160MA 250MA 500MA 800MA 1.25Amp 2Amp 3.15Amp 5Amp

1.25 inch Q/8 @ 0.06 each £4.00
250MA 500MA 750MA 1Amp 1.5Amp 2Amp 3Amp 7Amp 10Amp

1.25 inch A/S @ 0.15 each £10.00
50MA 60MA 100MA 150MA 250MA 500MA 750MA 1.5Amp 3Amp 4Amp 5Amp

SUNDRIES

MONO TAPE HEAD	2.50
AUTO REVERSE TAPE HEAD	3.95
STEREO HEAD	3.50
PYE IF GAIN MODULE	6.99
4.433 MHZ CRYSTAL (PAL)	0.45
5.5 MHZ CRYSTAL (SOUND)	0.45
DELAY LINE DL50/TAU82	1.15
FOCUS CONTROL GEC2110	1.50
FOCUS CONTROL PYE 731	1.50
FOCUS STICK	0.95
SAW FILTER	0.10
ANODE CAP 27KV	0.69
SOLDER MOP	0.64

TV MAIN SWITCHES

MAINS SWITCH CVC5	1.00
MAINS SWITCH DECCA/GEC	1.00
G8 SWITCH	1.00
G11 SWITCH	0.95
G11/12 WITH REMOTE	1.15
G11/12 WITH REMOTE AND MAINS OFF	1.50

WIREWOUND RESISTORS

4 WATT 2R0-10K	0.20
7 WATT R47-22K	0.20
11 WATT 1R-15K	0.25
17 WATT 1R-15K	0.30

LINE OUTPUT TRANSFORMERS

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DECCA 100	7.95
DECCA 1700 MONO	9.95
DECCA 1730	8.25
DECCA 2230	8.25
GEC 2040	7.50
GEC 2110	14.50
GRUNDIG 1500	15.45
GRUNDIG 510-6010, 2222, 5011-6011	13.45
ITT CVC20	8.20
ITT CVCZS/30/32	8.20
PHILIPS G8	8.50
PHILIPS G9	8.95
PHILIPS G11	13.95
PYE 691/697	11.50
PYE 713/715	11.50
PYE 725	10.95
PYE 731	9.95
RBM T20A	12.40
RANK MURPHY T18A	10.00
Y20A	12.50
A640	8.50
A823	11.50
TANDBERGE 90	11.15
TELEFUNKEN 711A	11.15
THORN 1500 (15KV)	15.45
THORN 1590	9.50
THORN 3500 (EHT)	9.50
THORN 8000	23.50
THORN 8500	17.50
THORN 9000	19.50
THORN 9800	22.40
THORN MAINS TRANSFORMER 3000/3500	9.70

DIODES

AA119	0.08
BA115	0.13
BA145	0.16
BA148	0.17
BA154	0.06
BA156	0.15
BA157	0.30
BA244	0.75
BA301	0.75
BA302	0.85
BA313	0.75
BA318	2.95
BA328	2.95
BA521	1.75
BAV21	0.30
BAW62	0.19
BAX13	0.04
BAX16	0.12
BB105B	0.30
BT151	0.79
BY126	0.10
BY127	0.11
BY133	0.15
BY164	0.45
BY176	1.20
BY179	0.63
BT182	0.55
BY184	0.35
BY187	0.45
BY199	0.40
BY206	0.14
BY208-800	0.33
BY210-800	0.33
BY223	0.90
BY298-400	0.22
BY299-800	0.22
BYX10	0.20
BYX25-600	1.25
BYX36-150R	0.20
BYX38-600R	0.60
BYX55-600	0.30
BYX71-600	1.75
BZX61	0.15
BZX88	0.10
BZY95C30	0.35
CS4B	8.00
CS10B	16.50
MR510	0.65
MR512	0.65
OA47	0.15
OA90	0.10
OA91	0.15
OA95	0.10
OA202	0.40
IN21DR	5.00
IN23B	2.95
IN23C	4.95
IN23ER	4.95
IN23WE	2.95
IN4001	0.04
IN4003	0.04
IN4004	0.05
IN4007	0.06
IN4148	0.02
IN4448	0.10
IN5401	0.12
IN5402	0.14
IN5403	0.12
IN5406	0.13
IN5407	0.16
IN5408	0.16
ITT44	0.10
ITT923	0.15
ITT2002	0.10

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BZX61 Series	0.15
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CRE-1400	35.00
D10-210GH	45.00
D10-230GH	35.00
D13-610GH	59.00
D13-611GH	59.00
D13-630GH	59.00
D13-630GM	59.00
D14-150GH	75.00
D14-173GM	53.00
D14-181GM	53.00
D14-200GM	75.00
D16-100GH/97	65.00
D18-160GA	69.00
DG7.32	45.00
DH3-91	45.00
F16-101GM	55.00
F21-130GR	75.00
F31-12LD	75.00
F31-13GR	75.00
M7-120W	10.00
M14-100GM	45.00
M17-1512GVR	175.00
M23-112GV	55.00
M24-120LC	59.00
M24-122WA	59.00
M28-13LG	49.00
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M31-190GR	55.00
M31-191GV	55.00
M31-195W	65.00
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DAF91	0.70
DAF96	0.65
DC70	1.75
DC90	3.50
DCX-4-5000	25.00
DET16	28.50
DET18	28.50
DET20	2.50
DET22	35.00
DET23	35.00
DET24	27.50
DET25	22.00
DET29	32.00
DF91	1.00
DF92	0.60
DF96	1.25
DF97	1.25
DG10A	8.50
DH63	1.50
DH77	0.90
DK91	1.20
DK92	1.50
DL35	2.50
DL63	1.00
DL70	2.50
DL73	2.50
DL91	3.95
DL92	1.25
DL93	1.10
DLS10	13.50
DLS16	10.00
DM70	2.50
DM160	4.50
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DY86/87	0.75
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E55L	49.50
E80CC	19.50
E80CF	12.50
E80F	18.50
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E81CC	5.50
E81L	12.00
E82CC	4.50
E83CC	4.50
E83F	5.50
E86C	9.50
E88C	7.95
E88CC	3.50
E88CC-01	6.95
E88CC MULLARD	4.95
E90CC	7.95
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E91H	4.50
E92CC	3.95
E99F	6.95
E130L	18.50
E180CC	9.50
E180F	6.50
E182CC	9.00
E186F	8.50
E188CC	7.50
E235L	12.50
E280F	19.50
E283CC	12.00
E288CC	17.50
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E1148	1.00
EA50	1.00
EA52	55.00
EA76	1.95
EA79	1.95
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EAC91	2.50
EAF42	1.20
EB34	1.50
EB41	3.95
EB91	0.85
EBC33	2.50
EBC41	1.95
EBC81	1.50
EBC90	0.90
EBC91	0.90
EBF80	0.95
EBF83	0.95
EBF89	0.70
EBF93	0.95
EBL1	4.50
EBL21	4.50
EC52	0.75
EC70	1.75
EC81	7.95
EC86	1.95
EC88	1.95
EC90	1.50
EC91	5.50
EC92	1.95
EC93	1.50
EC95	7.00
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EC8010	12.00
ECC32	3.50
ECC33	3.50
ECC35	3.50
ECC81	1.50
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ECC82 PHILIPS	1.95
ECC83	0.95
NEW ECC83 SELECTRON SPECIAL Low cross coupling, Low noise, Low microphony	£3.50
ECC83 BRIMAR	2.15
ECC83 PHILIPS	1.95
ECC83 SIEMENS	2.50
ECC85	1.00
ECC86	2.75
ECC88	1.00
ECC89	1.50
ECC91	2.00
ECC189	1.95
ECC801S	6.95
ECC803S	6.95
ECC804	0.60
ECC2000	7.95
ECF80	1.15
ECF82	1.15
ECF86	1.70
ECF200	1.85
ECF202	1.85
ECF801	0.85
ECF804	6.50
ECF805	2.50
ECF806	10.25
ECH3	4.50
ECH4	4.50
ECH35	3.50
ECH42	1.50
ECH81	1.75
ECH83	1.00
ECH84	1.00
ECH200	1.50
ECL80	0.60
ECL82	0.79
ECL83	2.50
ECL84	0.74
ECL85	0.95
ECL86	0.95
ECL805	0.95
EF37A	2.50
EF22	3.50
EF39	1.50
EF40	4.50
EF42	3.50
EF50	2.50
EF54	4.50
EF55	4.95
EF70	1.20
EF73	3.50
EF80	0.55
EF83	3.95
EF85	0.50
EF86	2.25
EF86 MULLARD	4.50
EF86/CV4085	5.00
EF89	1.50
EF91	195

EF92	2.15
EF93	1.50
EF94	1.50
EF95	1.95
EF97	0.90
EF98	0.90
EF183	0.75
EF184	0.85
EF731	4.50
EF800	11.00
EF804S	19.50
EF805S	25.00
EF806S	25.00
EF812	0.65
EFL200	1.50
EFP60	3.50
EH90	0.72
EK90	1.50
EL32	0.95
EL33	5.00
EL34	2.95
EL34 MULLARD Matched per pair	15.00
L34 MULLARD	6.50
EL34 SIEMENS	4.50
EL36	2.50
EL36 MULLARD	3.95
EL37	9.00
EL38	9.00
EL41	3.50
EL42	2.00
EL71	4.50
EL81	6.95
EL83	7.50
EL84 BRIMAR	0.95
EL84 MULLARD	3.50
EL84 SIEMENS	2.50
EL85	4.50
EL86	1.75
EL90	1.75
EL91	6.00
EL95	1.75
EL152	15.00
EL360	6.75
EL500	1.95
EL504	1.95
EL506	5.95
EL509	5.25
EL509 MULLARD	7.50
EL519	6.95
EL802	3.65
EL821	6.95
EL822	12.95
ELL80	22.50
EM34	12.50
EM83	1.65
EM84	1.65
EM85	3.95
EM87	2.50
EN32	15.00
EN91	1.95
EN92	4.50
EY51	0.80
EY70	7.50
EY81	2.35
EY82	1.15
EY83	1.50
EY84	5.95
EY86/87	0.50
EY88	0.55
EY91	5.50
EY500A	1.50
EY802	0.70
EZ35	1.00
EZ40	2.75
EZ41	2.75
EZ80	0.75
EZ81	0.75
EZ90	1.50
FW4-800	2.95
G55/1K	9.00
G180/2M	6.95
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GC10B	17.50
GC10D	17.50
GC10/4B	17.50
GC10/4E	17.50
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GD86W	6.00
GDT120M	5.00
GN4	6.00
GN10	15.00
GR10G	4.00
GS10C	16.50
GS10H	12.00
GS12D	12.00
GT1C	14.00
GU20	35.00
GU50	17.50
GXU1	13.50
GXU3	24.00
GXU50SS	14.50
GY501	1.50
GY802	1.50
GZ32	2.50
GZ33	4.50
GZ34	2.50
GZ37	4.50
HBC90	1.95

HL41	3.50
HL90	3.50
KT8C	7.00
KT33C	3.50
KT36	2.00
KT44	4.00
KT45	4.00
KT61	5.00
KT63	2.00
KT66 USA	9.95
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KT67	9.00
KT77 Gold Lion	11.95
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KT88 USA	10.95
KT88 Selectron	15.00
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KTW61	2.50
KTW62	2.50
KTW63	2.00
KTZ63	2.50
LB7-20	95.00
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M508	195.00
M5143	155.00
M5199	295.00
M8079	6.00
M8082	7.50
M8083	3.25
M8091	7.50
M8096	3.00
M8098	5.50
M8099	5.00
M8100	5.50
M8136	7.00
M8137	7.95
M8161	6.50
M8162	5.50
M8163	5.50
M8190	4.50
M8195	6.50
M8196	5.50
M8204	5.50
M8223	4.50
M8224	2.00
M8225	3.95
ME1400	3.50
ME1401	29.50
ME1402	29.50
MHLD6	4.00
MP25	195.00
MS4B	5.50
MU14	3.50
N37	12.50
N78	9.85
OA2	1.50
OA2WA	2.50
OA3	2.50
OB2	1.50
OB2WA	2.50
OC3	2.50
OD3	2.50
OM4	2.50
OM5B	3.00
OM6	1.75
ORP43	2.50
ORP50	3.95
P61	2.50
P41	2.50
PABC80	0.75
PC86	0.75
PC88	0.75
PC92	3.50
PC97	1.10
PC900	1.25
PCC84	0.40
PCC85	0.55
PCC88	0.70
PCC89	0.70
PCC189	0.70
PCC805	0.70
PCC806	0.80
PCE82	0.80
PCF80	0.65
PCF82	0.60
PCF84	0.65
PCF86	1.20
PCF87	1.25
PCF200	1.80
PCF201	1.80
PCF801	1.35
PCF802	0.85
PCF805	1.25
PCF806	1.00
PCF808	1.25
PCH200	1.50
PCL82	0.85
PCL83	2.50
PCL84	0.75
PCL85	0.80
PCL86	0.85
PCL805	0.90
PD500	5.95
PE1-100	69.00
PEN25	2.00
PEN40D	3.00
PEN45	3.00
PEN45DD	3.00
PEN46	2.00
PFL200	0.95
PL36	1.75
PL38	1.50
PL81	1.25
PL82	0.60
PL83	0.52
PL84	0.78
PL500	1.10
PL504	1.15

PL508	1.75
PL509	4.85
PL519	4.95
PL802	6.00
PL802T	3.50
PL820	2.95
PY32	0.60
PY33	0.50
PY81	0.70
PY82	0.70
PY83	0.70
PY88	0.65
PY500A	1.95
PY800	0.79
PY801	0.79
QB3-300	72.00
QB3-1750	139.00
QB3.5-700	72.00
QB5-3500	595.00
QE08-200	145.00
QQE02-5	19.50
QQE03-12	7.95
QQE03-20	35.00
QQE06-40	45.00
QQV02-6	19.50
QQV03-10	5.50
QQV03-10 MULLARD	15.00
QQV03-20	25.00
QQV06-40A	27.50
QQV06-40A MULLARD	39.50
QQV07-50	55.00
QQZ03-20	42.50
QQZ06-40	45.00
QS75/20	1.50
QS95/10	4.85
QS108/45	4.00
QS150/15	6.95
QS150/30	1.15
QS150/40	7.00
QS1205	3.95
QS1213	5.00
QU37	9.50
QV03-12	6.50
QV05-25	2.50
QV06-20	29.50
QV08-100B	145.00
QY3-125	72.00
QY4-250	72.00
QY4-400	85.00
R10	4.00
R18	2.50
RG1-240A	14.50
RG3-250A	6.50
RG3-1250A	35.00
RR3-250	15.00
RR3-1250	35.00
S11E12	38.00
S104-2K	10.00
SC1/1300	6.00
SP61	3.50
STV280/40	11.95
TB2-5/300	85.00
TB2-300	195.00
TB3-750	95.00
TB3-2000	450.00
TBL2-300	395.00
TBL2-500	495.00
TD03-10/D/E/F	35.00
TT15	45.00
TT21	45.00
TT22	39.50
TT100	69.00
TY2-125A	85.00
TY4.400	85.00
TY7-6000A	600.00
TY8-600W	365.00
U19	9.50
U26	0.90
U35	3.50
U37	9.00
U41	6.95
U50	2.00
UB2	3.00
U191	0.70
U192	1.00
U193	1.00
U251	2.50
U801	3.50
UABC80	0.65
UAF42	1.00
UBC41	2.25
UBC81	1.50
UBF80	0.60
UBF89	1.00
UBL21	1.75
UC92	1.20
UCC84	0.70
UCC85	0.60
UCF80	1.00
UCH21	1.20
UCH41	2.50
UCH42	2.50
UCH81	1.00
UCL82	1.75
UCL83	2.50
UF41	1.15
UF42	1.15
UF80	1.75
UF85	1.20
UF89	2.00
UL41	7.50
UL44	3.50
UL84	1.50
UL85	0.85

UU5	3.50
UU6	6.00
UU7	8.00
UU8	9.00
UY41	3.50
UY85	0.70
V235A/1K	250.00
V238A/1K	295.00
V246A/2K	315.00
V241C/1K	195.00
V453	12.00
VLS631	10.95
VP4B	9.50
VP41	4.95
VR101	2.50
VR105/30	2.50
VR150/30	2.50
VU39	2.50
W21	4.50
W61	4.50
W77	5.00
W81M	4.50
W739	1.50
X24	4.50
X41	4.50
X66/X65	4.95
X76M	1.95
XC24	1.50
XC25	0.50
XFW47	1.50
XFW50	1.50
XG1-2500	75.00
XL628FT	7.50
XNP12	2.50
XR1/1600A	49.50
XR1/3200A	79.50
XR1-6400A	149.50
Y65	6.95
YD1100	75.00
YJ1060	265.00
YL1020	42.50
YL1060	195.00
YL1070	195.00
YL1071	195.00
YL1290	65.00
YL1440	450.00
Z77	1.20
Z300T	6.00
Z302C	12.00
Z359	9.00
Z520M	4.00
Z700U	9.50
Z759	19.85
Z803U	18.95
ZA1000	12.50
ZA1001	1.50
ZM1001	12.00
ZM1005	8.00
ZM1020	6.00
ZM1021	8.00
ZM1023	7.95
ZM1041	14.00
ZM1082	9.00
ZM1084	10.00
ZM1175	6.50
ZM1177	9.00
ZM1202	55.00
ZM1263	4.00
1A3	4.50
1AE4	3.50
1AX2	3.50
1B22	10.00
1B27	55.00
1B35A	45.00
1B63A	75.00
1K3	2.50
1N5GT	2.50
1P28	25.00
1R5	0.90
1S5	1.50
1T4	1.00
1U4	1.75
1U5	1.00
1X25	2.50
2A3	16.50
2AS15A	11.50
2B7	2.50
2B22	69.50
2C36	70.00
2C39A	32.50
2C39BA	39.50
2C40	37.00
2C42	29.50
2C43	60.00
2C51	2.50
2CY5	1.50
2D21	1.95
2D21W	3.15
2E22	49.00
2E26	7.95
2J55	295.00
2K25	35.00
2K25 RAYTHEON	75.00
2K26	95.00
2K29	250.00
2K48	140.00
2K56	250.00
2X2A	5.00
3A/107B	12.00
3A/108A	9.00
3A/109B	11.00
3A/110B	12.00
3A/141K	11.50
3A/146J	7.50

3A/147J	7.50
3A/167M	10.00
3A3A	3.95
3A4	1.10
3A5	4.50
3AT2	3.35
3B22	25.00
3B24	12.00
3B26	24.00
3B28	15.00
3BZ6	1.50
3C45	24.00
3CX3000A7	650.00
3CYS	1.50
3D21A	29.50
3E22	49.50
3E29	39.50
3EJ7	1.95
3H	0.40
3J.170E	1450.00
3L	0.40
3Q4	2.50
4-65A	65.00
4-250A	79.50
4-400A	87.50
4-1000A	425.00
4B32	35.00
4B/551B	125.00
4BQ7A	1.75
4BZ6	1.95
4C28	25.00
4C35	145.00
4XC125C EIMAC	150.00
4CX250B	45.00
4CX250BM	65.00
4CX250K EIMAC	115.00
4CX250R AMPEREX	125.00
4CX350A	100.00
4CX350F	95.00
4CX1000A	425.00
4CX1500B	398.00
4CX5000A	1000.00
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4D32	125.00
4GS7	2.25
4GV7	2.25
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5A/102D	9.50
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5A163K	10.00
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5A-180M	9.00
5A-206K	10.00
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5B-255M	19.50
5B-256M	15.00
5B-257M	15.00
5B258M	14.50
5C22	125.00
5CL8A	2.50
5J180E	1950.00
5JL8	2.95
5R4GB	5.50
5R4GY	4.95
5T4	5.95
5T8A	1.95
5U4G	2.95
5U4GB	4.50
5V4G	2.50
5X4	4.95
5Y3GT	1.95
5Z3	4.50
5Z4G	2.50
6/30L2	0.70
6A/203K	9.00
6A7	4.95
6A8	1.50
6AB4	3.50
6AC7WA	2.00
6AG5	2.50
6AG7	1.95
6AH6	3.50
6AJ4	3.50
6AJ7	2.00
6AK5	1.95
6AK6	2.50
6AL5	0.60
6AM4	3.25
6AM5	6.00
6AM6	1.95
6AN5	4.50
6AN8A	4.50
6AQ5	1.75
6AQ8	1.00
6AR5	5.95
6AS5	1.50
6AS6	2.50
6AS7G	4.50
6AT6	0.90
6AT8	1.75
6AU4GT	2.00
6AU5GT	4.50
6AU6	0.95
6AV6	0.90
6AW8A	3.50
6AX4GT	1.95
6AY3B	1.95
6AZ8	4.50

6B4G	5.50
6B8G	1.50
6B10	1.95
6BA6	1.50
6BA7	4.50
6BA8A	3.50
6BC8	0.85
6BE6	1.50
6BG6G	3.00
6BH6	1.95
6BH8	1.50
6BJ6	1.50
6BK4	4.00
6BL6	85.00
6BL8	1.15
6BM6	115.00
6BN6	1.65
6BN8	3.95
6BQ5	0.95
6BQ7A	1.50
6BR7	4.95
6BS7	5.50
6BW6	5.35
6BW7	1.50
6BZ6	2.50
6BZ7	2.95
6C4	1.50
6C5	1.95
6C6	3.50
6C8G	1.50
6C9	4.95
6CA4	4.95
6CA7	3.50
6CB5	3.95
6BC6	1.95
6CD6GA	4.50
6CF6	1.95
6CG7	3.50
6CH6	6.95
6CL6	3.25
6CL8A	1.50
6CM7	2.95
6CS6	0.75
6CS7	0.95
6CW4	8.00
6DC6	2.35
6DJ8	1.00
6DJ8 SPECIAL	3.50
6DK6	1.50
6DQ5	8.50
6DQ6B	2.50
6DT6A	1.50
6DW4B	21.5
6E5	3.95
6EA7	2.50
6EA8	2.50
6EB8	1.75
6EJ7	0.85
6EM5	2.50
6EM7	2.50
6EU8	1.75
6EV7	2.95
6EW6	1.50
6EW7	4.50
6F1	2.00
6F5	5.50
6F7	5.50
6F13	3.00
6F14	1.00
6F17	2.75
6F23	0.60
6F24	1.25
6F25	1.25
6F28	1.25
6F32	1.25
6F33	12.50
6FH5	6.50
6FH8	5.95
6FL2	4.50
6FQ7	3.50
6GE5	3.95
6GH8A	2.50
6GJ7	0.85
6GM6	2.65
6GS7	21.5
6GV8	0.95
6GW8	2.50
6GY5	4.95
6GY6	2.50
6H1	9.50
6H6GT	1.95
6HB7	1.95
6HF8	2.50
6HM5	2.50
6HQ5	3.50
6HS6	4.95
6HS8	2.95
6HZ6	3.50
6J4	2.15
6J5GT	2.50
6J6	2.00
6J7	4.15
6J7G	4.15
6JB6A	5.50
6JE6C	7.50
6JM6	7.50
6JU8A	2.50
6JS6C	7.50
6K7G	2.00
6K8G	3.00
6KD6	7.50
6KG6A	6.95
6L1	2.50
6L6GC	2.95
6L6GC USA	6.50
6L6GAY	5.50
6L6GT	2.50
6L6WGC	5.50
6L7	3.50
6L15	3.15
6L19	3.95

6LJ8	2.50
6LD20	1.15
6LF6	7.50
6LQ6	7.50
6P28	2.00
6Q7GT	1.50
6R7	3.15
6RHH8	10.00
6S4A	1.50
6SA7	1.35
6SC7	1.50
6SH7	1.35
6SJ7GT	1.20
6SK7	1.35
6SL7GT	1.95
6SN7GT	1.95
6SQ7GT	1.50
6SS7	1.95
6T8	1.50
6U6GT	3.50
6U7G	3.50
6U8A	1.50
6V6G	1.25
6V6GT	1.95
6W4GT	1.95
6Y6G	3.95
6X2N	1.00
6X4	1.50
6X5GT	1.00
6X5GTY	1.00
6X8A	2.25
7A6	4.50
7AU7	1.50
7B6	3.50
7B7	2.50
7D8	4.50
7J7	5.50
7K7	7.50
7L	1.50
7Q7	4.50
7Y4	2.50
8B8	2.50
8B1C	2.50
8BQ5	1.95
8CW5	1.50
8EB8	1.50
8FQ7	1.95
10D2	1.25
10DE7	2.50
10DX8	2.50
10EB8	1.95
10EW7	2.95
10F1	0.75
10GK6	1.95
10P14	2.50
11E3	55.00
11R3	5.50
12A6	3.95
12AD6	1.50
12AE6	1.50
12AH7GT	4.95
12AL5	1.00
12AT6	1.25
12AT7	1.15
12AT7WA	2.50
12AU6	1.50
12AU7	0.85
12AV6	1.95
12AV7	2.50
12AX4GTB	1.50
12AX7	0.95
12AX7WA	2.50
12AX7S	7.95
12AY7	3.95
12B4A	4.50
12BA6	2.50
12BE6	1.95
12BH7A	3.50
12BL6	1.75
12BR3	1.95
12BY7A	3.50
12C8	2.50
12CA5	1.95
12CX6	1.20
12DQ6B	3.50
12DW4A	3.50
12BZ6	3.95
12E1	19.50
12E14	38.00
12FX5	1.95
12GN7	3.95
12GH7	3.95
12J5GT	3.95
12J7GT	3.50
12JZ8	2.95
12KGT	1.50
12K8Y	1.95
12KU7	1.95
12S7GT	1.50
12SA7GT	1.95
12SG7	4.75
12SK7	1.95
12SJ7	1.50
12SN7GT	1.85
12SW7	3.50
12SY7	4.50
12X4	1.95
13D7	3.20
13DE7	2.50
13DR7	2.95
13E1	145.00
13EM7	3.50
14B6	4.50
14R7	3.50
15E	5.50
16AQ3	1.95
16GY5	2.95
16H	0.40
16L	0.40
17AB	3.50
17AX4GTA	1.95
17BE3	2.50

17DW4A	2.95
17EW8	0.95
17JZ8	4.50
18D3	6.00
18GB5	3.50
19AQ5	3.50
19AU4GT	2.50
19BG6	3.50
19G3	19.50
19G6	9.00
19H4	35.00
19H5	33.50
20CV	9.50
20D1	0.70
20LF56	7.95
20L1	0.95
20P1	0.55
20P4	1.95
20P5	1.15
21JZ6	4.95
21KQ6	4.95
21LU8	3.75
24B1	39.50
24B9	39.50
25BQ6	1.75
25DQ6B	2.95
25L6GT	1.75
29C1	19.50
29KQ6	6.50
30C15	0.50
30C17	0.40
30C18	1.48
30FL2	1.35
30FL12	0.95
30FL13	1.10
30FL14	1.25
30L1	0.45
30L15	0.60
30L17	0.60
30P4MR	1.00
30P12	1.00
30P18	0.60
30P19	1.00
30P1	2.50
30PL13	0.60
30PL14	1.75
31JS6C	5.50
33A/158M	19.50
35A3	3.95
35A5	4.50
35C5	4.50
35L6GT	2.00
35Z3	1.95
35Z5GT	3.50
38HE7	5.95
40KD6	5.50
42	6.95
47	6.00
50A5	1.50
50B5	1.95
50C5	0.95
50CD6G	1.95
50EH5	1.50
50JY6	2.95
53KU	4.50
75B1	3.50
75C1	4.50
80	4.50
83	8.50
82A1	7.50
85A1	6.50
85A2	2.95
90AV	17.50
90C1	3.50
90CG	15.00
90CV	15.00
91AG	9.00
92AG	19.50
92AV	17.50
95A1	6.50
100E1	10.00
108C1	2.50
150B2	6.50
150C1K	9.00
150D2	2.50
150C4	2.50
185BT	1.50
211	25.00
230D	15.00
231D	15.00
250TH	150.00
307	5.00
328A	15.00
572B	65.00
723A/B	75.00
724A	275.00
725A	275.00
726A	75.00
801A	15.00
802	25.00
803	14.95

805	59.00
807 RCA	5.50
811	15.00
812A	35.00
813 Philips	35.00
813	27.50
829B	14.50
833A	95.00
845	45.00
866A	8.50
872A	20.00
873	60.00
954	1.00
955	1.00
1849	315.00
1927	25.00
2040	25.00
2050A	5.95
2050W	6.50
4212H	250.00
4471	35.00
4687A	9.50
5544	79.50
5559	55.00
5636	5.50
5642	9.50
5643	9.50
5651	2.50
5654	1.95
5670	3.25
5675	28.00
5678	7.50
5687	4.50
5696	4.50
5702	3.50
5704	3.50
5718	6.15
5725	2.50
5726	2.50
5727	2.50
5749	2.50
5750	1.85
5751	2.95
5763	6.50
5814A	3.25
5823	9.50
5829WA	6.50
5840	3.50
5842	11.00
5847	10.95
5863	95.00
5879	9.50
5886	13.95
5894	39.50
5899	4.50
5963	1.75
5965	2.15
6057	3.75
6058	2.50
6060	2.25
6072	6.95
6080	8.50
6080WA	9.50
6132	10.50
6136	2.50
6146B	9.50
6155	72.00
6156	72.00
6157	2.50
6158	3.20
6201	6.45
6350	3.50
6360	4.50
6386	14.50
6463	7.50
6550	8.50
6550A GE	10.95
6550 RCA	15.00
6870	11.50
6883B	9.95
6973	7.95
7025	2.50
7025S	6.95
7027A	8.50
7119	9.00
7189	5.50
7199	7.50
7247	4.95
7475	5.00
7486	155.00
7527	85.00
7551	8.50
7581A	9.95
7586	15.00
7591A	6.95
7815	59.50
7868	7.50
8156	9.95
8950	10.50
18042	10.50

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Memories are made of light

Important advances in the development of optical storage media have been made recently. Erasable optical discs and a new type of optical material are the major newcomers.

Magneto-optical storage. One system is actually on sale: the Asaca rewritable optical disc and its associated drive, which was on show at the NAB in Las Vegas in April. A prototype was shown last year and it is now in production. The system from Japan is specifically addressed at the video market and can be used to digitally record up to ten minutes of moving pictures with sound. A different drive is used to create a still picture library with one disc storing up to 2250 images, with 16-bit digital sound. A third machine can record and store 1200 h.d.tv still pictures: with a VME interface it is linked into image processing equipment and used for computer graphics, electronic publishing, medical images and many industrial applications.

Asaca's system uses a similar technology to one developed by 3M, in which the surface of the disc is subjected to a magnetic field while being heated by a laser beam, polarizing the magnetic material in the disc. When scanned by a lower-powered laser, the magnetized domains change the optical polarity of the reflection, which is picked up by a sensor with a polarized filter. Sectors of discs can be 'wiped' by repeating the process with the magnetic field reversed, or the whole disc erased by a combination of heat and magnetic field.

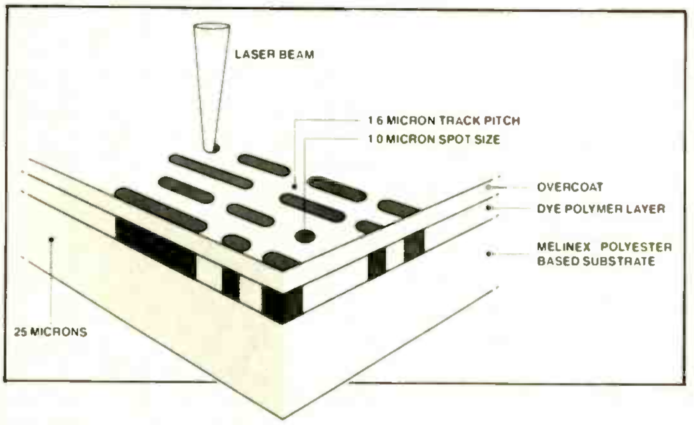
Because the method of recording causes the physical alignment of magnetic domains, rather than just magnetizing, recordings are much more stable than conventional magnetic recordings.

3M are concentrating on the computer applications and the discs will have a similar function to CD-rom with the additional advantage of being erasable. One 5.25in double-sided disc stores up to 500Mbytes of data or the equivalent of about 600 floppy discs. Drives are still being developed for 3M, and Olympus have working prototypes. The system has acquired the initials MO, for magneto-optical, which is likely to become as familiar as CD.

Digital paper. Perhaps DP for Digital Paper will become similarly familiar when the system developed by ICI becomes available. This also uses the heating properties of a 1μm diameter laser beam but this time, instead of changing the magnetic qualities of the medium, the beam alters the reflective characteristics of a dye polymer layer which changes in colour. This change allows the data to be read by a laser pick-up similar to that used in a CD player. The process is irreversible and permanent.

The other main difference is in the substrate material. In place of a rigid polycarbonate disc, Digital Paper uses a thin flexible polyester, similar to that used for magnetic tapes. This is easy to produce and very cheap. ICI quotes a price of "a third of a penny for a megabyte of storage."

The stability needed to focus a laser beam onto the medium seems to make the flexibility of the tape a disadvantage but drives are being developed. One was demonstrated at CeBit in Hanover (see *Telecomms Topics*). One advantage is that the material is easy to cut into any required shape, be it tape, disc or even identity or price tags, read by an appropriate pick-up. Storage capacity is phenomenal: one reel of ½in tape similar to the magnetic tape used by main-frame computers can store about 600Gbyte, the equivalent of 1000 hours of digital music or 300 full-length feature films.



Multi-processor parallel computing

More than a thousand processors are incorporated into the Distributed Array of Processors (DAP), made by Active Memory Technology. The company achieved a triumph when it sold its first system to Argonne National Laboratory in the USA within a year of the company's foundation. Universities and research establishments are queuing up to acquire this new computer. Its special virtue is speed, as the multiprocessor array can manipulate data between 10 and 100 times faster than rival systems. Essentially, the computer has a 32 by 32 grid of 1024 single-bit processors, each having 32K of memory over which it has control. This allows very short data paths and high-speed (1Gbyte/s) communication between the processor and memory. A master controller interprets the coded instructions and distributes the tasks to the processors. Processor arrays are duplicated, one to be used as a slave to the active set and all operations are checked by comparing the two. Single-bit processors have a word length of one but, since any combination of them are used in parallel, words can be of any length. Gone are constraints of specific 8, 16 or 32-bit words.

The system is used as a plug-in co-processor on a host workstation such as a DEC Vax or a Sun. Tasks can be assigned to the DAP from within the host's programs. Hence, most of the software available is in the form of sub-routines, although many of them are almost complete programs in their own right. Fortran-Plus is particularly suitable for the DAP as it takes full advantage of its array processing capabilities.

Some tasks like image manipulation are especially suited to the processor, as each element can be assigned to a specific pel. Single-bit processors might behave rather like brain cells and the Artificial Intelligence unit in Edinburgh University are investigating the similarity between the workings of the DAP and neural networks. Many other processing-intensive tasks are particularly suited to the DAP. A good example is data sorting: a demonstration program fills a video screen with a million pels; the program can sort them all into bands by hue and intensity and complete the task in a half to one second, depending on the sorting strategy used.

Although the company is still relatively new, many of the staff previously worked on the technology at ICL, where the first generation of DAPs was developed. ICL transferred the patents to the new company and now owns a quarter of it.

Automatic laser soldering

Micro-soldering of surface-mounted and thick-film circuits has been made much easier by the introduction of a laser soldering system. A working prototype was on display at the recent Internepcon show in Birmingham. A consortium of companies developed the system from work initiated at Hull University, who remained a partner in Hull Unico Ltd. Don Whitehead of Hull Unico said: "The advantage of using lasers in soldering applications lies in the ability to direct the energy beam accurately and precisely on to a target area without heating the surrounding parts. The minimal rise in substrate temperature reduces mechanical stress; the rapid melting and cooling of the solder prevents the formation of intermetallic compounds which can cause brittleness and lead to joint failure.

"The ability to control the amount of heat and its duration applied to a specific component or area makes reworking much simpler."

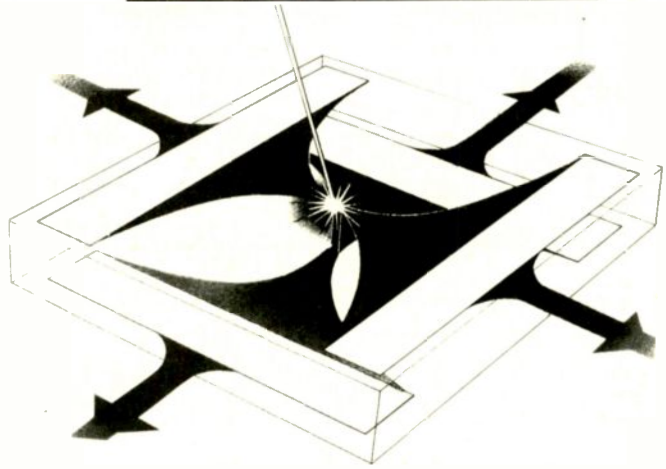
The success of recent field tests has encouraged the consortium to press on with commercial development of the system and with this in mind they approached Dynapert, who specializes in p.c.b. production machinery. Norman Hodson, product manager at Dynapert said that the consortium had already done a very good job: "The system can be sold as it stands and offers a sound base for further development."

Another member of the consortium is Laser Applications, who developed the CO_2 laser which features rapid power control up to 30W and generates a minumum spot size of 300µm.

Computer control is used for repetitive operations, but it is also possible to operate it by hand, with the aid of a joystick control and a high-resolution tv camera. These are also used to program a soldering sequence into the computer.

Cambridge Interconnection Technology is a member of the consortium and David Topham is particularly pleased that it is so self-contained: "It needs no cooling, no air, no vacuum – just a 13A plug!"

Optical position sensor



Take a thin slice of silicon, dope one side with boron and the other with phosphorus and you have a very special sort of solar cell. Output currents to the four electrodes at the edges vary precisely according to where on its surface light has fallen. The Optometer was developed at the Chalmers Institute and is being manufactured by SiTek Laboratories in Partille, Sweden. Maximum non-linearity of the output, relating to the position of a light spot on the surface, is about 0.05%, which means that it can measure a micron difference in position. It is also stable in varying temperatures and reacts in a few microseconds.

Sensors are combined with lasers to produce theodolites and other position-sensing instruments. If lights are attached to moving objects, even people, with their images projected through a camera lens onto the Optometer, it can give a direct readout of their positions, which is linked to a computer for movement analysis. Such analysis usually involves the painstaking study of the individual frames of a film or video recording.

Riscy business

Two major instrumentation manufacturers have issued statements that they are producing new generations of equipment incorporating reduced instruction set computing (risc) processors.

Hewlett-Packard have announced a number of new and upgraded computers incorporating H-P's own risc chip. It has also studied computer architecture in depth and come up with HP Precision Architecture. HP designers noted that mips is not as accurate a measure of performance as actual throughput of work done on a computer. They claim that the use of a risc processor only accounts for about a third of the improvements in the company's computers. Other measures include optimizing the compiler codes, enhancing the storage facilities, interfaces and addressing systems. Operating and data management systems have also received a facelift.

The designers stress that the system has applications throughout circuit technologies and offers advanced facilities for use in the future.

Risc technology is also the topic in a Tektronix brief. A new generation of graphics workstations will be based on Motorola's recently-announced 88000 risc processor. There are as yet no further details but Tek is "sticking with industry standards, such as Motorola hardware, X Windows and Unix.", according to Paul Morgan, a marketing manager.

Mips are still important to Motorola who quote 17mips as the speed of the 88000, which is three integrated circuits. These are an integer processor and a floating-point unit on one chip; the other two are both a combination of cache memory and a memory management unit. High-speed c-mos with 1.5µm geometry is used for the processors with sub-micron geometry promised for the future and even-higher-speed e.c.l. versions planned.

Scoreboarding is a technique used within the 88000 to simplify the design of compilers and other software. Instructions and registers are monitored automatically, so that software can make optimum use of the many registers without having to plot the exact progress of information as it is shunted round the registers. Motorola expects that the 88000 will find applications in telecommunications, artificial intelligence, graphics and animation, multi-user systems, parallel processing and supercomputers (and Tektronix workstations!).

There is no compatibility between the 68000 and 88000; however, Motorola have committed themselves to supporting both in the foreseeable future.

Engineering education proposals rejected by IEE

"There is little historical evidence to suggest that large-scale changes in education system are better planned by government or outside bodies rather than from within. The best course of action is to give positive encouragement to likely developments as they arise from within the system. This approach is much more likely to be successful than the imposition of outside and untested changes and is also likely to produce less disruption in a system that is already under considerable pressure." This is the gist of the IEE's reply to the Engineering Council's discussion document 'Restructuring of Engineering Higher Education'. Although the EC report says that a successful engineering industry is essential to the nation's economy, and that more qualified engineers and technicians are required, it accepts too readily that expenditure on such education will remain static or even fall. Dramatic restructuring and amalgamation of university and polytechnic departments, is not the answer, says the IEE.

In brief

A computer image was used as evidence in a British court of law for the first time recently. Two aspects of image processing were used in court; the enhancing of the criminal's face from a security video and the use of the built-in computer to measure and analyse the scene of the crime.

The equipment used was the Ikonos system from TCS Electronics in Hove.

What sort of transducers does British industry really want? The question will possibly be answered by a strategic survey to be carried out by ERA Technology. Microprocessors have the capability of responding to more precise sensors. New processes need additional measurements. The survey will attempt to identify those parameters or conditions for which sensors are not currently available, or in need of considerable improvement. Recommendations will be made on areas where there is sufficient demand for a particular type of transducer to make it commercially viable.

The survey is being commissioned by sensor suppliers and any not yet participating can contact ERA Technology, in Leatherhead.

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