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Cover picture illustrates David Whitehouse's piece on space exploration, starting on p.44. Photographs by courtesy of NASA.

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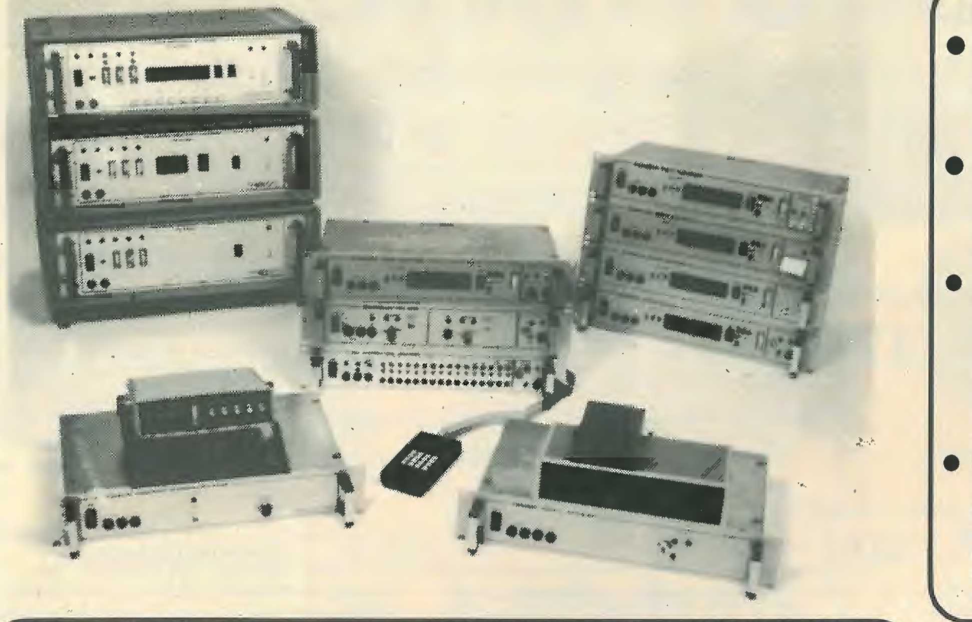

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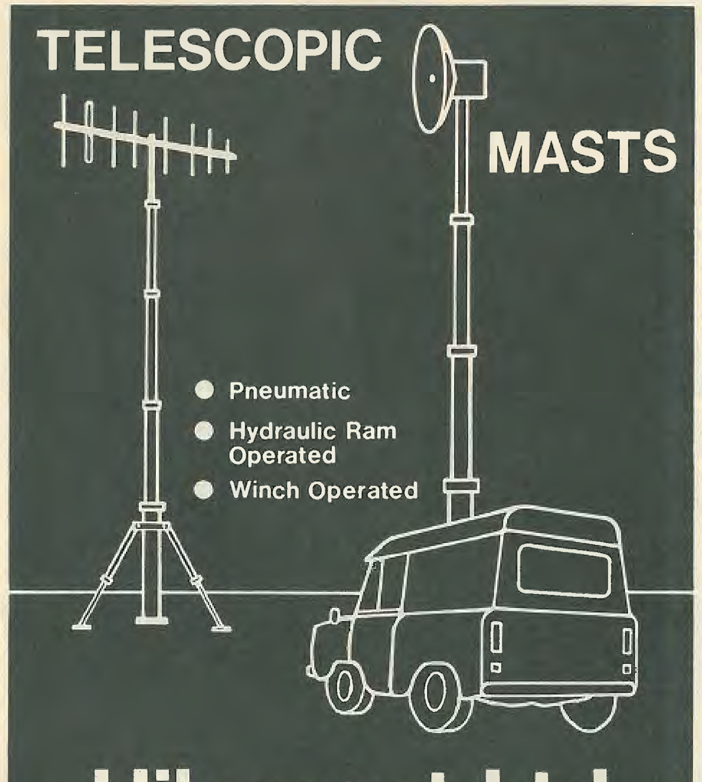

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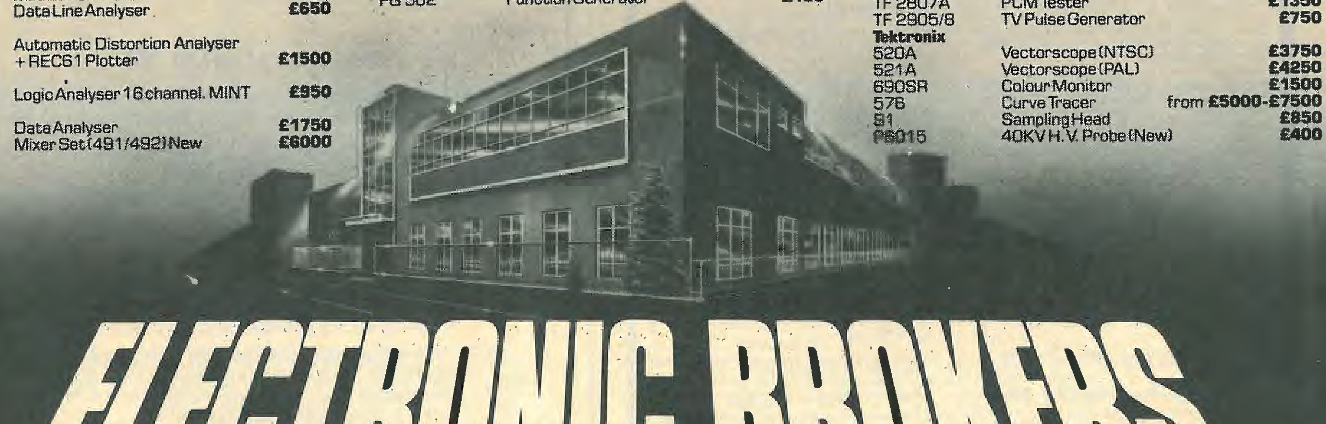

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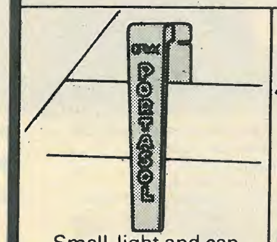

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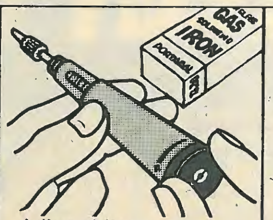

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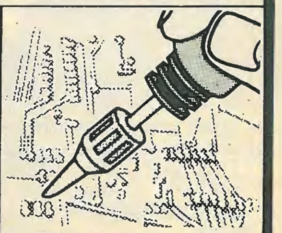
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If you're not really serious about Microprocessar development you can probably get away with using a "toy" assembler — like the one for the BBC that uses BASIC.

But for people who program for a living, meeting project deadlines and documentation standards is no game. A professional programmer needs fast, precision tools, not something that fell out of a Christmas cracker.

And there is no more powerful and professional Assembler available, within fifty times the price, than the UNIVERSAL DEVELOPMENT SYSTEM META Assembler.

Not only does this one Assembler, supplied on two 16K ROMs and two discs, allow you to write code for almost all the major Microprocessors (using the appropriate standard codes, eg LD (HL), A etc in Z80, MOVE.B DO, label (A2, D5.L) etc in 68000; see table for full list) but it also:

- ● Includes a fully integrated Editor, with features such as search, search/replace, block copy/delete and a list of other features specially designed with the Assembly programmer in mind
- ● is able to Assemble several MegaBytes of source and produce unlimited object code
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CIRCLE 68 FOR FURTHER DETAILS.

NEWS COMMENTARY

IC design in the universities

British universities are to integrate their computer-aided engineering facilities and have announced through the University Grants Committee, their commitment to five packages which will cover all their needs for c.a.e. facilities. The announcement follows a year of product evaluation by a universities' working party, chaired by Dr Peter Jones of Manchester University. Dr Jones says that the purchase of professional, high quality tools, worth about £25m in the commercial marketplace, represents "the biggest, co-ordinated step in the teaching of integrated circuit design anywhere in the world". Professor Erik Dagless, another member of the committee added that the purchase of the best tools available would ensure that the universities would produce the "kind of graduates required by British Industry."

The orders have been placed with a combination of British and US/European companies offering products able to run on a comprehensive range of micro, mini and mainframe computers.

The British contribution is by Racal-Redac, Qudos and Silicon Microsystems. GenRed are supplying their British-designed HILO simulator and Silvar-Lisco, with headquarters in California and Belgium, is contributing a variety of cad packages. All the companies have agreed to forego their licencing fees and make the systems available to all the universities wishing to participate. So far around 45 universities are adding or developing courses which will include the design of integrated analogue and digital circuits.

RACAL-REDAC

Racal-Redac are providing the Isis suite of software which integrates the entire design cycle for mos silicon devices. The processes of design capture, simulation, layout, verification and pattern generation are carried out on a single database ensuring total compatibility throughout the design stage. This database at the heart of the system encourages a well-structured hiearchical approach to design.

The design process begins by entering the data in a circuit schematic form or by means of a 'hardware description language' (HDL). This is linked directly to a simulator which can perform both logic and circuit analysis, individually or simultaneously. Functional level simulation can also be carried out by means of a high-level programming language.

Because a transistor has its full description in the HDL, not only its topological but also its electrical characteristics are assigned. The width, length, area, associated resistance and capacitance together with timing information must conform to the HDL description, allowing full on-line net list comparison between the physical design data and the physical layout topology. Real-time debugging is built in to assist the designer to correct any violation of the design rules. The combination of rule-checking and debugging ensures optimum use of silicon areai simplifies circuit modification; and removes many of the error message listings which occur with other post-design simulation and checking systems. Because the operation of some devices depend on specific violation of design rules, it is possible to manually over-ride the system with a conventional editor.

The Isis suite was originally developed by Inmos and used in the design of the Transputer.

Haroon Ahmed, Peter O'Keeffe and Andrew Hopper, directors of Qudos with their electron beam.

QUDOS

"Silicon for the people" is the slogan for Qudos (quick design on silicon) of Cambridge, who have an educational entry package that will run on the BBC Master Turbo micro. This is no coincidence; Qudos shares with Acorn many consultants and directors. The suite of programs (£500) provide a full design system for the Ferranti 9C ULA's. They enable the replacement of entire circuit boards of general-purpose i.cs with single devices. The chips are manufactured by Qudos using direct-write E-beam lithography and their system is called the Silicon Bus. The Bus runs according to demand, with a minimum frequency of once a month. At peak times it is possible to run the service daily. A fee is paid to book a slot in the queue and another for each manufactured device; total cost about £100 per device.

The design system has been optimized for use with devices having about 300 gates. However, the ULA9C chip has 990 matrix cells, so it is possible to design several circuits on the same chip. There are a few design constraints; the standard package used has 40 pins and Qudos reserve four of these for a test circuit which can be probed automatically when the device is manufactured and again when packaged. Two further pins are reserved for power and ground connections.

Qudos also produce 'professional' packages which may be run on the Acorn Cambridge Workstation or a DEC Vax or MicroVax II. A complete Qudos workstation with all required hardware and software costs £15,000. This system is designed to provide the metal connections for Texas Instrument's TAHC logic chips.

SILICON MICROSYSTEMS (SMS)

Silicon Microsystems offer a silicon brokerage — they can have wafers manufactured by a number of semiconductor processing houses and provide themselves the final testing and packaging. They can also provide a number of design tools including a library of five and three-micron c-mos macros. These are design-system and process-house independent. This means that they may be incorporated into a wide range of design systems and also provide multi-sourcing for any device developed under the SMS software system. SMS services range from semi-custom gate array devices through standard cell components to full custom i.cs.

GENRAD

Hilo is a logic simulator developed at Brunel University and further developed and supported by GenRad's Design Engineering Group in Fareham. The software is used for logic and timing verification, fault simulation and test-pattern generation. It has been adopted by many semiconductor houses in the design of full or semi-custom devices and by system manufacturers designing at p.c.b. level with standard devices. Hilo was designed to be portable and can be supported on a wide range of computer systems and workstations. These range for mainframe VAXs and IBMs to Apollo Domain and the UK manufactured Whitechapel workstation. A recent addition is the IBM RT PC. Hilo can also work in conjunction with software and hardware products from the cae suppliers. These include Silvar-Lisco, Mentor, Daisy, Racal-Redac, and many others. Valid, Tektronix/cae, Hewlett-Packard, Computervision and Intergraph all offer Hilo as the core simulator of their workstations and market it as part of their systems. Waveform patterns created during the design and simulation process can be used in the preparation of complete test programs for both VLSI and PCB ATE.

SILVAR-LISCO

Silvar-Lisco is the amalgamation of a Silicon Valley company with a software house of

▷▷

Eureka projects announced

Eureka is a European collaboration to develop high-technology products to compete in the world markets. Unlike Esprit or the Alvey project, which are undertaking long-term research into advanced technology, Eureka is aimed specifically at practical projects leading to marketable products.

At least 25 projects are under discussion, covering such technologies as pharmaceutical products, image processing, telecommunications, new engineering materials, environmental technology and advanced manufacturing.

Sixteen projects have been announced recently covering a wide range of technology and expertise.

1. Eurocim: the development of a flexible automated factory for the production of p.c.bs.

2. Cerise: European centre for image synthesis, to improve and market computer imaging technology.

3. ES2: Automatic design and production of integrated circuits using direct write-on-silicon.

4. GaAs: Development of design and manufacturing processes for the production of monolithic gallium arsenide microwave integrated circuits.

5; Mobile robot: Development of fast-moving robots for public safety applications such as natural disasters and anti-terrorism.

6. Expert system: for dealing with major plant failures and security control.

7. East: Eureka advanced software technology for the development of 'software factories' incorporating software engineering.

8. Paradi: Automatic production management system using artificial intelligence developments.

9. Diane: Automatic integrated system for neutronography. Non-destructive use of neutron beams in the quality control of large, complicated components manufactured from new materials.

10. Chemical waste destruction: the use of high-powered lasers for the detection and destruction of impurities in finished products and in waste products.

11. GTO thyristors: the development of a complete set of gate turnoff thyrsors for use in railway traction systems.

12. Chrome salts substitutes: the replacement of chrome by aluminium in the treatment of leather.

13. Galeno 2000: the development of non-invasive medical diagnostic equipment based on new sensors and artificial intelligence.

14. Vehicle noise identification : the development of new methodology to allow more accurate and automated identification of noise sources in transportation vehicles.

15. Apex: Advanced project for European information exchange, especially applied to the aerospace industry.

16. Car engines: the development of ceramic and new metallic components for car engines.

Each of the projects has a differing number of European participating countries and a timescale of between two and six years.

GenRad's HILO simulation system is used to verify an i.c. circuit.

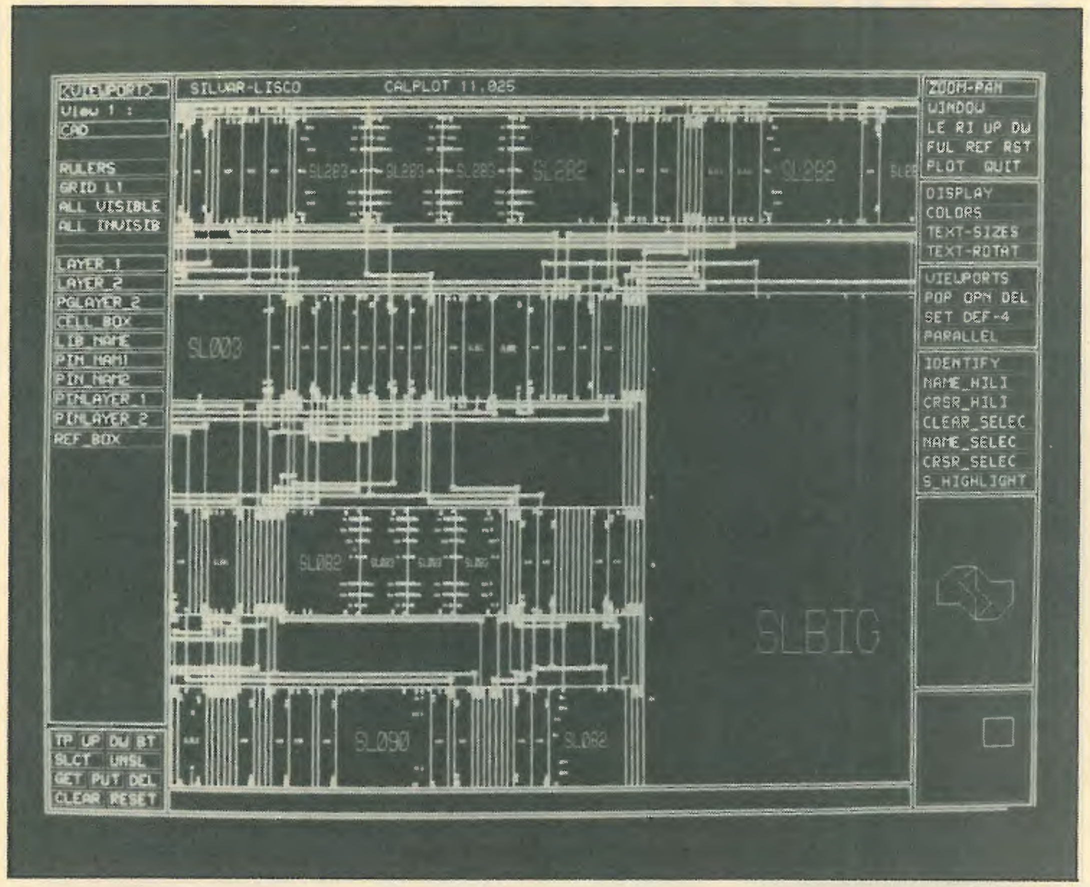

Image of a completed standard cell designed on Silvar-Lisco's CAL-MP system.

Leuven in Belgium. They specialize in computer-aided engineering software for automating the design of application-specific i.cs. As well as individual packages, its SL-2000 integrated design system canhandle the complete design cycle from data entry to final artwork. SL-2000 includes programs for architectural, logic and circuit schematic design along with behavioural, logic and circuit simulation. The system also provides automatic layout software for gate-array and standard cell i.c. design. In common with the other packages selected for use in universities, the system uses an hierarchical approach to electronic design from system level to VLSI circuit design. The programs run on IBM 43xx and 30xx computers as well as DEC, VAX, and Prime 50 c.p.us Apollo-based workstations, and a wide variety of graphics terminals.

All the systems are to be installed in the universities ready for courses commencing in October.

Some useful addresses:

Racal-Redac Ltd,
Tewkesbury, Glos GL20 8HE.

Qudos Ltd, Cambridge Science Park, Milton Road, Cambridge CB4 4FD.

Silicon Microsystems Ltd,
Gastons Road, Malmesbury,
Wilts SN16 0BE.

GenRad Ltd, Norreys Drive,
Maidenhead, Berks SL6 4BP.

Silvar-Lisco Ltd, Alpha House,
London Road, Bracknell,
Berks RG12 2HT.

Electrical engineering vital for Britain's future

An increased awareness of the contribution made by the electrical engineering profession to the national economy and greater emphasis on the education and training of young engineers for the future are essential if Britain is to compete successfully in world markets and redress its current unfavourable balance of payments.

This was the message given to MPs by IEE President Admiral Sir Lindsay Bryson. Sir Lindsay was speaking at a Seminar organised by the IEE in association with the Industry and Parliament Trust on 'Chartered Electrical Engineers and their place in Industry and Society'.

Sir Lindsay stressed the contribution made by the electrical, electronic and associated manufacturing industries to Britain's balance of payments. With annaul sales of nearly £20,000M in 1984 those industries provided more than half of all engineering sales. He also pointed out that as the industry moves into higher technologies the need for greater numbers of professional engineers will continue to rise.

"In order to meet this need", said Sir Lindsay, "we must devote much more of our efforts and resources to produce more highly qualified engineers of all disciplines".

Sir Lindsay pointed out that the number of applications from schoolchildren to take up electrical engineering at University had more than doubled over the last twelve years as had the quality of those accepted. However, he warned that the quality of teaching in mathematics and physics must be improved if this encouraging trend is to continue. "This" he said, "may well be the most significant shortcoming of all and we must seek ways to tackle it!"

The IEE President also highlighted another "potentially serious barrier to progress" — the difficulty in recruiting greater numbers of lecturers, ideally high achievers in their late 20's or early 30's, with good industrial experience. "Sadly" he said, "the rigid university salary scales do not provide competition with industrial salaries for these good people and some way must be found to solve this problem".

Sir Lindsay suggested that the "provision of industrial consultancies might bridge this gap and, in addition, build a link between universities and industry that will be of great benefit in future years". Sir Lindsay also disclosed that the IEE is willing to administer such a scheme and will be pursuing the idea with industry and Government.

Sir Lindsay ended his address with a warning that it would be at least 10 years before changes to the system of engineering education was reflected in improved industrial performance.

"I would ask you all to recognise the very long term scales involved . . . So please do not expect instant success from any changes which are made".

Videodiscs and Esprit

The development of a new interactive videodisc-based information system by four major European companies is to be funded by Esprit.

The project partners are BBC Enterprises Limited, Nederlandse Philips Bedrijven, Logica UK Limited and The Societe Europeene de Propulsion (Division Traitment d'Images).

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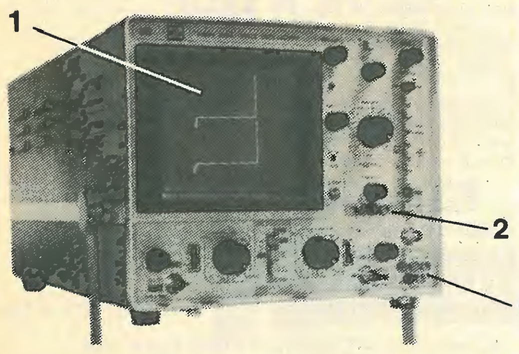

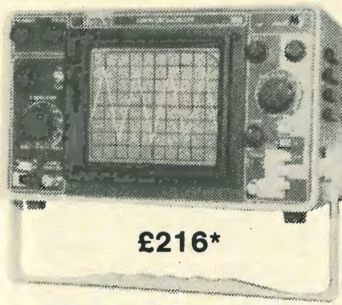

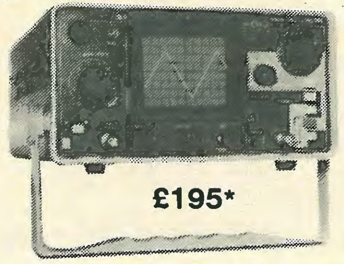

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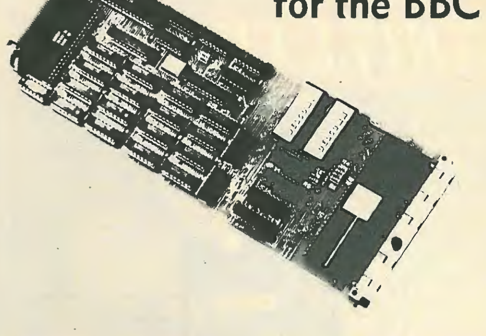

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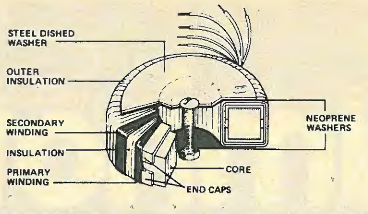

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15VA Regulation 19% 62 x 34 (See diagram) 0.35 Kgs Mounting bolt M4x12	03010	6+6	1.25
	03011	9+9	0.83
	03012	12+12	0.63
	03013	15+15	0.50
	03014	1+18	0.42
	03015	22+22	0.34
	03016	25+25	0.30
	03017	30+30	0.25
30VA Regulation 18% Size A B C 70 35 37 0.45 Kgs Mounting bolt M5 × 50	13010	6+6	2.50
	13011	6+6	1.66
	13012	12+12	1.25
	13013	15+15	1.00
	13014	18+18	0.83
	13015	22+22	0.68
	13017	30+30	0.50
50VA Regulation 13% Size A B C 80 40 43 0.9 Kgs Mounting bolt M5 × 50	23010	6+6	4.16
	23011	9+9	2.77
	23012	12+12	2.08
	23013	15+15	1.66
	23014	18+18	1.38
	23015	22+22	1.13
	23016	25+25	1.00
	23017	30+30	0.83
	23028	110	0.45
	23029	220	0.22
	23030	240	0.20
80VA Regulation 12% Size A B C 95 40 43 1.0 Kgs Mounting bolt M5 × 50	33010	6+6	6.66
	33011	9+9	4.44
	33012	12+12	3.33
	33013	15+15	2.66
	33014	18+18	2.22
	33015	22+22	1.81
	33016	25+25	1.60
	33017	30+30	1.33
	33028	110	0.72
	33029	220	0.36
	33030	240	0.33
120VA Regulation 11% Size A B C 95 45 50 1.2 Kgs Mounting bolt M5 × 50	43010	6+6	10.00
	43011	9+9	6.66
	43012	12+12	5.00
	43013	15+15	4.00
	43014	18+18	3.33
	43016	25+25	2.40
	43017	30+30	2.00
	43018	35+35	1.71
	43028	110	1.09
	43029	220	0.54
	43030	240	0.50

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	53012	12+12	6.66
	53013	15+15	5.33
	53014	18+18	4.44
	53015	22+22	3.63
	53016	25+25	3.20
	53017	30+30	2.66
	53018	35+35	2.28
	53026	40+40	2.00
	53028	110	1.45
	53029	220	0.72
	53030	240	0.66
225VA Regulation 7% Size A B C 110 50 55 2.2 Kgs Mounting bolt M5 × 60	63012	12+12	9.38
	63013	15+15	7.50
	63014	18+18	6.25
	63015	22+22	5.11
	63016	25+25	4.50
	63017	30+30	3.75
	63018	35+35	3.21
	63026	40+40	2.81
	63025	45+45	2.50
	63033	50+50	2.25
	63028	110	2.04
	63029	220	1.02
	63030	240	0.93
300VA Regulation 6% Size A B C 110 57 62 2.6 Kgs Mounting bolt M5 × 60	73013	15+15	10.00
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	73015	22+22	6.82
	73016	25+25	6.00
	73017	30+30	5.00
	73018	35+35	4.28
	73026	40+40	3.75
	73025	45+45	3.33
	73033	50+50	3.00
	73028	110	2.72
	73029	220	1.36
	73030	240	1.25
500VA Regulation 5% Size A B C 135 60 65 4.0 Kgs Mounting bolt M8 × 70	83016	25+75	10.00
	83017	30+30	8.33
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	83026	40+40	6.25
	83025	45+45	5.55
	83033	50+50	5.00
	83042	55+55	4.54
	83028	110	4.54
	83029	220	2.27
	83030	240	2.08

TYPE	SERIES NO.	SEC. VOLTS	R.M.S. CURRENT
625VA Regulation 4% Size A B C 140 70 75 5.0 Kgs Mounting bolt M8 × 90	93017	30+30	10.41
	93018	35+35	8.92
	93026	40+40	7.81
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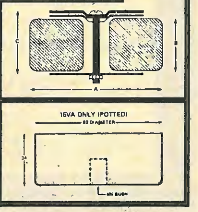

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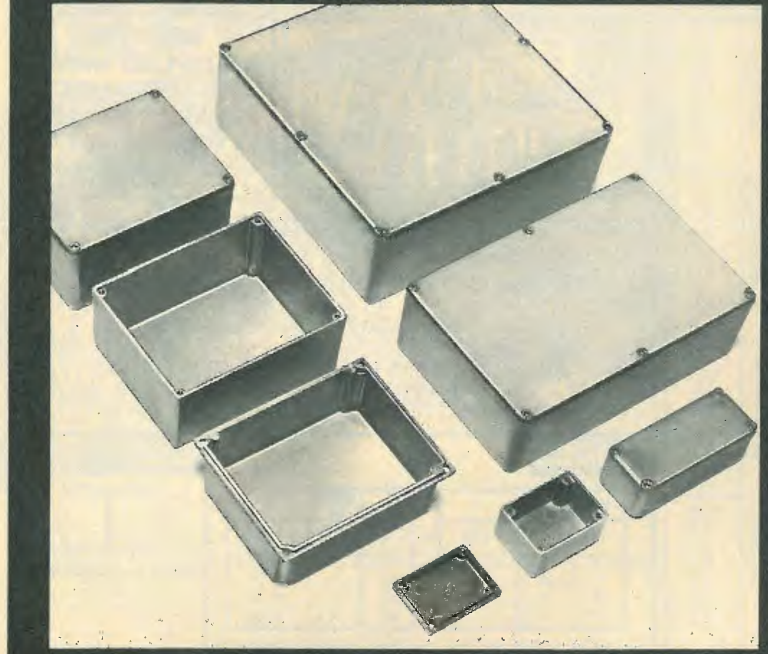

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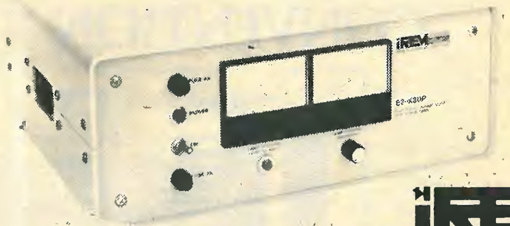

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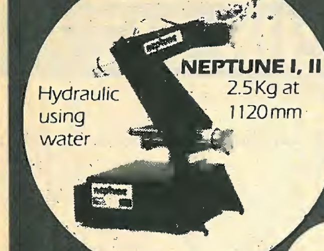
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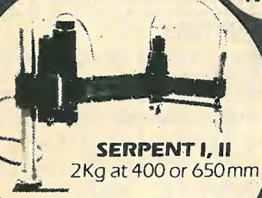
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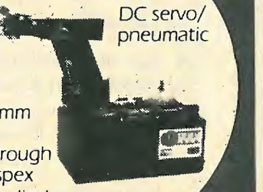
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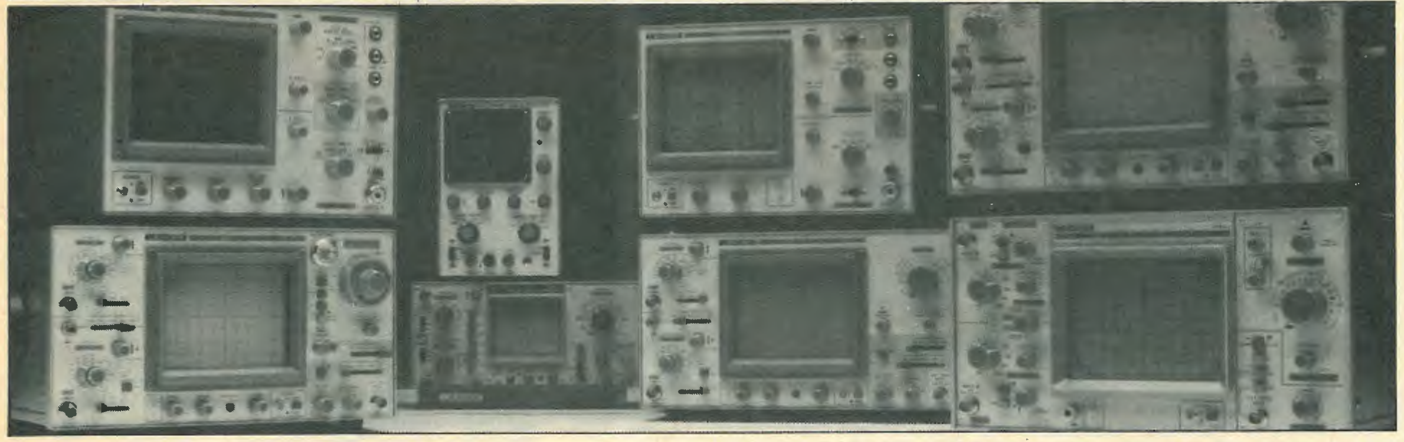

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META-ASSEMBLER. Both an editor and Macro-Assembler. Meta can assemble most 65xx, 68xx, 6804, 6805/6305, 6809, 8048, 8080/8085, Z80, 1802 and more. Please phone for comprehensive leaflet. **Meta-Assembler £126(c)**

We stock the full range of ACORN hardware and firmware and a very wide range of other peripherals for the BBC. For detailed specifications and pricing please send for our leaflet.

PRINTERS & PLOTTERS

EPSON: LX-80 NLO....................**£195 (a)** Optional Tractor Feed..................**£20 (c)**
EPSON FX RANGE
FX85 (80 col)..........................**£315 (a)** **f1431FX105 (136 col)**...............**£449 (a)**
EPSON JX80 4 colour printer..**£435 (a)**
EPSON LQ Range:
LQ800 (80 col)..........................**£595 (a)** LQ1500 (136 col) 2K buffer..........**£875 (a)**
32K buffer........**£950 (a)**
TAXAN KAGA:
KP180 (80 col)..........................**£195 (a)** KP910 (156 col).......................**£339 (a)**
DAISY WHEEL:
BROTHER HR15.......................**£295 (a)** JUKI 6100................................**£289 (a).**
CENTRONICS GLP (NLQ) Printer..**£109 (b)**
DOTPRINT + NLQ Rom for Epson...**£28 (d)**
Epson HI-80 PLOTTER..............**£345 (a)** Hitachi 672 PLOTTER.................**£465 (a)**

PRINTER ACCESSORIES

We hold a wide range of printer attachments (sheet feeders, tractor feeds etc) in stock. Serial, parallel, IEEE and other interfaces also available. Ribbons available for all above plotters. Pens with a variety of tips and colours also available. Please phone for details and prices.

Plain Fanfold Paper with extra fine perforation (Clean Edge):
2000 sheets 9.5″ × 11″ **£13(b)** 2000 sheets 14.5″ × 11″ **£18.50(b)**
Labels per 1000s: Single Row 3½″ × 1 7/16″ **£5.25(d)** Triple Row 2-7/16″ × 1 7/16″ **£5.00(d)**

MODEMS

MIRACLE WS 2000
The world standard BT approved modem covering all standard CCITT and BELL (outside UK only) standards upto 1200 baud. Allows communication with virtually any computer system in the world. Expandability to Auto Dial and Auto Answer with full software control enhance the considerable features already provided on the modem. Mains powered. WS 2000 **£125 (c),** Data Cable **£7(d),** Auto Dial Board/Auto Answer Board (awaiting BABT approved) **£30 (d)** Software Control Kit **£10 (d)**

NEW WS-3000 RANGE — the new professional series. All are intelligent and 'Hayes' compatible, allowing simply 'English' commands to control its many features. All models feature Auto-Dial with 10 number memory, Auto-Answer, Speed buffering, printer port, data security option etc. All models are factory upgradeable.

WS3000 V2123 (V21 & V23 + Bell **£295 (a) WS3000 V22** (as above plus 1200 baud full duplex **£495 (a) WS3000 V22bis** (as above plus 2400 baud full duplex **£650 (b)**
BBC Data Cable for WS3000 **£6(d).** Data Cables for other micros available
The WS3000 range all have BT approval.

GEC DATACHAT 1223: An economically priced BABT approved modem complying with CCITT V23 standard capable of operating at 1200/75bps and 75/1200bps and 1200/1200bps pseudo full duplex. It is line powered does not require external power source. it is supplied with software suitable for connecting to PRESTEL, Micronet 800, Telecom Gold and a host of bulleting boards **£86(b)**

SOFTY II

This low cost intelligent eprom programmer can program 2716, 2516, 2532, 2732, and with an adaptor, 2564 and 2764. Displays 512 byte page on TV — has a serial and parallel I/O routines. Can be used as an emulator, cassette interface.
Softy II ....**£195.00 (b)**
Adaptor for 2764/2564 ....**£25.00**

SPECIAL OFFER

2764-25 £2:00(d);
27128-25 £2:75(d);
6264 LP-15 £3:75(d);

ACORN IEEE INTERFACE £278(a)

INDUSTRIAL PROGRAMMER EP8000 £695 (a)

DISC DRIVES

PD800P (2 × 400K/2 × 640K 40/80T DS) with built in Monitor stand...£279(a)
PD800 (2 × 400K/2 × 640K 40/80T DS)..£249(a)
TS400 1 × 400K/1 × 640K 40/80T DS...£109(b)
PS400 with psu 1 × 400K 40/80T DS...£129(b)

3.5″ Drives
1 × 400K/1 × 640K 80T DS
TS35 1..........................£109 (b) **PS35 1** with psu...............**£129(b)**
2 × 400K/1 × 640K 80T DS
TD352..........................£199(b) **PD35 2** with psu...............**£209(b)**

3M FLOPPY DISCS

Industry Standard floppy discs with a lifetime guarantee Discs in packs of 10.

5¼″ DISCS				3½″ DISCS	
40 T SS DD	**£12(d)**	40 T DS DD	**£16(d)**	80 T SS DD	**£30(d)**
80 T SS DD	**£21(d)**	80 T DS DD	**£22(d)**	80 T DS DD	**£38(d)**

FLOPPICLENE DRIVEHEAD CLEANING KIT

FLOPPICLENE Disc Head Cleaning Kit with 28 disposable cleaning discs ensures continued optimum performance of the drives. 5¼″ **£14.50(d)**
3½″ **£16.00(d)**

DRIVE ACCESSORIES

Single Disc Cable **£6** (d) Dual Disc Cable **£8.50** (d)
10 Disc Library Case **£1.80** (d) 30 Disc Storage Box **£6** (c)
30/40 Disc Lockable Box **£14** (c) 100 Disc Lockable Box **£16**(c)

MONITORS

All 14″ monitors now avilable in plastic or metal cases, please specify your requirement.

14″ RGB 1431 STD Res **£179 (a); 1451** Med Res **£235 (a); 1441** Hi Res **£375 (a).**
14″ RGB with PAL & Audio 1431 AP Std Res **£205 (a) 1451** AP Med Res **£275 (a)**
Swivel Base for Plastic 14″ Microvitecs **£20 (c)**
20″ RGB with PAL & Audio 2030CS Std Res **£380 (a); 2040CS** Hi Res **£685 (a).**

KAGA TAXAN 12″ RGB

SUPERVISION III Plus £330 (a)

MITSUBISHI 14″ RGB Med RES IBM & BBC Compatible **£249 (a)**

MONOCHROME MONITORS:

SANYO DM8112CX Hi Res 12″ Green Screen **£95 (a)**
KAGA KX1201G Hi Res 12″ Etched Green Screen **£99 (a)**
KAGA KX1203A Hi Res 12″ Etched Amber screen **£105 (a)**
PHILIPS BM7502 12″ Hi Res Green Screen **£75 (a)**
PHILIPS BM7522 12″ Hi Res Amber Screen **£79 (a)**

BBC Leads RGB **£5(d)** Microvitec **£3.50m (d)** Monochrome **£3.50 (d)**

UVERASERS

UV1T Eraser with built-in timer and mains indicator. Built-in safety interlock to avoid accidental exposure to the harmful UV rays.
It can handle up to 5 eproms at a time with an average erasing time of about 20 mins. **£59 + £2 p&p.**
UV1 as above but without the timer. **£47 + £2 p&p.**
For Industrial Users, we offer UV140 & UV141 erasers with handling capacity of 14 eproms. UV141 has a built in timer. Both offer full built in safety features UV140 **£69,** UV141 **£85, p&p £2.50.**

PRINTER BUFFER

The buffer offers a storage of 64K. Data from three computers can be loaded into the buffer which will continue accepting data until it is full. The buffer will automatically switch from one computer to next as soon as that computer has dumped all its data. The computer then is available for other uses. LED bar-graph indicates memory usage. Simple push button control provides. REPEAT, PAUSE and RESET functions. Integral power supply. **£199** (a).
BBC Cable Set **£30.**

Serial Test Cable

Serial Cable switchable at both ends allowing pin options to be re-routed or linked at either end — making it possible to produce almost any cable configuration on site.
Available as M/M or M/F **£24.75 (d)**

Serial Mini Patch Box

Allows an easy method to reconfigure pin functions without rewiring the cable assay. Jumpers can be used and reused. **£22 (d)**

Serial Mini Test

Monitors RS232C and CCITT V24 Transmissions, indicating status with dual colour LEDs on 7 most significant lines. Connects in Line. **£22.50 (d)**

CONNECTOR SYSTEMS

I.D. CONNECTORS

(Speedblock Type)

No of ways	Header Plug	Recep-tacle	Edge Conn.
10	90p	85p	120p
20	145p	125p	195p
26	175p	150p	240p
34	200p	160p	320p
40	220p	190p	340p
50	235p	200p	390p

D CONNECTORS

No of Ways

	9	15	25	37
MALE:				
Ang Pins	120	180	230	350
Solder	60	85	125	170
IDC	175	275	325	—
FEMALE:				
St Pin	100	140	210	380
Ang Pins	160	210	275	440
Solder	90	130	195	290
IDC	195	325	375	—
St Hood	90	95	100	120
Screw Lock	130	150	175	—

TEXTOOL ZIF

SOCKETS 24-pin £7.50
28-pin £9.10 40-pin £12:10

EDGE CONNECTORS

	0.1″	0.156″
2 × 6-way (commodore)	—	300p
2 × 10-way	150p	—
2 × 12-way (vic 20)	—	350p
2 × 18-way	—	140p
2 × 23-way (ZX81)	175p	220p
2 × 25-way	225p	220p
2 × 28-way (Spectrum)	200p	—
2 × 36-way	250p	—
1 × 43-way	260p	—
2 × 22-way	190p	—
2 × 43-way	395p	—
1 × 77 way	400p	500p
2 × 50-way(S100conn)	600p	—

EURO CONNECTORS

DIN 41612	Plug	Skt
2 × 32 way St Pin	230p	275p
2 × 32 way Ang Pin	275p	320p
3 × 32 way St Pin	260p	300p
3 × 32 way Ang Pin	375p	400p
IDC Skt A + B	400p	
IDC Skt A + C	400p	

For 2 × 32 way please specify spacing (A + B, A + C).

MISC CONNS

21 pin Scart Connector 200p
8 pin Video Connector 200p

AMPHENOL CONNECTORS

36 way plug Centronics (solder **500p** (IDC) **475p**
36 way skt Centronics (solder) **550p** (IDC) **500p**
24 way plug IEEE (solder) **475p** (IDC) **475p**
24 way skt IEEE (solder) **500p** (IDC) **500p**
PCB Mtg Skt Ang Pin
24 way **700p** 36 way **750p**

GENDER CHANGERS

25 way D type

Male to Male £10
Male to Female £10
Female to Female £10

RS 232 JUMPERS

(25 way D)

24″ Single end Male	£5.00
24″ Single end Female	£5.25
24″ Female Female	£10.00
24″ Male Male	£9.50
24″ Male Female	£9.50

DIL SWITCHES

4-way	90p	6-way	105p
8-way	120p	10-way	150p

RIBBON CABLE

(grey/metre)

10-way	40p	34-way	160p
16-way	60p	40-way	180p
20-way	85p	50-way	200p
26-way	120p	64-way	280p

DIL HEADERS

	Solder	IDC
14 pin	40p	100p
16 pin	50p	110p
18 pin	60p	—
20 pin	75p	—
24 pin	100p	150p
28 pin	160p	200p
40 pin	200p	225p

ATTENTION

All prices in this double page advertisment are subject to change without notice.
ALL PRICES EXCLUDE VAT
Please add carriage 50p unless indicated as follows:
(a) £8 (b) £2.50 (c) £1.50 (d) £1.00

TECHNOLINE VIEWDATA SYSTEM. TEL: 01-450 9764

Using 'Prestel' type protocols. For information and orders — 24 hour service. 7 days a week

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74 SERIES

7400	0.30
7401	0.30
7402	0.30
7403	0.30
7404	0.36
7405	0.30
7406	0.40
7407	0.40
7408	0.30
7409	0.30
7410	0.30
7411	0.30
7412	0.30
7413	0.50
7414	0.70
7416	0.36
7417	0.40
7420	0.30
7421	0.60
7422	0.36
7423	0.36
7425	0.40
7426	0.40
7427	0.32
7428	0.43
7430	0.30
7432	0.36
7433	0.30
7437	0.30
7438	0.40
7439	0.40
7440	0.40
7441	0.90
7442A	0.70
7443A	1.00
7444	1.10
7445	1.00
7446A	1.00
7447A	1.00
7448	1.00
7450	0.36
7451	0.35
7453	0.38
7454	0.38
7460	0.55
7470	0.50
7472	0.45
7473	0.45
7474	0.50
7475	0.60
7476	0.45
7480	0.65
7481	1.80
7483A	1.05
7484A	1.25
7485	1.10
7486	0.42
7489	2.10
7490A	0.55
7491	0.70
7492A	0.70
7493A	0.55
7494	1.10
7495A	0.60
7496	0.80
7497	2.10
74100	1.90
74107	0.50
74109	0.75
74110	0.75
74111	0.55
74116	1.70
74118	1.10
74119	1.70
74120	1.00
74121	0.55
74122	0.70
74123	0.80
74125	0.65
74126	0.55
74128	0.55
74132	0.75
74136	0.70
74141	0.90
74142	2.50
74143	1.30
74144	2.70
74145	1.10
74147	1.70
74148	1.40
74150	1.75
74151A	0.70
74153	0.80
74154	1.40
74155	0.80
74156	0.90
74157	0.80
74159	1.75
74160	1.10
74161	0.80
74162	1.10
74163	1.10
74164	1.20
74165	1.10
74166	1.40
74167	4.00
74170	2.00
74172	4.20
74173	1.40
74174	1.10
74175	1.05
74176	1.00
74178	1.50
74179	1.50
74180	1.00
74181	3.40
74182	1.40
74184	1.80
74185A	1.80
74190	1.30
74191	1.30
74192	1.10
74193	1.15
74194	1.10
74195	0.80
74196	1.30
74197	1.10
74198	2.20
74199	2.20
74221	1.10
74251	1.00
74259	1.50
74265	0.80
74273	2.00
74276	1.40
74278	1.70
74279	0.90
74283	1.05
74742	3.20
74290	0.90
74293	0.90
74298	1.80
74351	2.00
74365A	0.80
74366A	0.80
74367A	0.80
74376	1.60
74390	1.10
74393	1.20
74490	1.40

74LS SERIES

74LS00	0.24
74LS01	0.24
74LS02	0.24
74LS03	0.24
74LS04	0.24
74LS05	0.24
74LS08	0.24
74LS09	0.24
74LS10	0.24
74LS11	0.24
74LS13	0.34
74LS14	0.50
74LS15	0.24
74LS20	0.24
74LS21	0.24
74LS22	0.24
74LS24	0.50
74LS26	0.26
74LS27	0.24
74LS28	0.24
74LS30	0.24
74LS32	0.24
74LS32	0.24
74LS33	0.24
74LS37	0.24
74LS38	0.24
74LS40	0.24
74LS42	0.50
74LS43	1.50
74LS48	0.90
74LS49	1.00
74LS51	0.24
74LS54	0.24
74LS55	0.24
74LS73A	0.30
74LS74A	0.35
74LS75	0.45
74LS76A	0.36
74LS78	0.42
74LS83A	0.70
74LS85	0.75
74LS86	0.35
74LS90	0.48
74LS91	0.90
74LS92	0.35
74LS93	0.54
74LS95B	0.75
74LS96	0.90
74LS107	0.40
74LS109	0.40
74LS112	0.45
74LS113	0.45
74LS114	0.45
74LS122	0.70
74LS123	o.80
74LS125	0.50
74LS126	0.50
74LS132	0.65
74LS133	0.55
74LS136	0.45
74LS138	0.55
74LS139	0.55
74LS145	0.95
74LS147	1.75
74LS148	1.40
74LS151	0.65
74LS152	2.00
74LS153	0.65
74LS154	1.60
74LS155	0.65
74LS156	0.65
74LS157	0.50
74LS158	0.65
74LS160A	0.65
74LS161A	0.75
74LS162A	0.75
74LS163A	0.75
74LS164	0.75
74LS165A	1.10
74LS166A	1.50
74LS168	1.30
74LS169	1.00
74LS170	1.40
74LS173A	1.00
74LS174	0.75
74LS175	0.75
74LS181	2.00
74LS183	1.90
74LS190	0.75
74LS191	0.75
74LS192	0.80
74LS194A	0.75
74LS195A	0.75
74LS196	0.80
74LS197	0.80
74LS221	0.90
74LS240	0.80
74LS241	0.80
74LS242	0.90
74LS243	0.90
74LS244	0.80
74LS245	1.10
74LS247	1.10
74LS248	1.10
74LS249	1.10
74LS251	0.75
74LS253	0.75
74LS256	0.90
74LS2457A	0.70
74LS258A	0.70
74LS259	1.20
74LS260	0.75
74LS266	0.60
74LS273	1.25
74LS279	0.70
74LS280	1.90
74LS283	0.80
74LS290	0.80
74LS292	9.00
74LS293	0.80
74LS295	1.40
74LS297	9.00
74LS298	1.00
74LS299	2.20
74LS321	3.70
74LS322A	3.90
74LS323	3.00
74LS324	3.20
74LS348	2.00
74LS352	1.20
74LS353	1.20
74LS356	2.10
74LS363	1.80
74LS364	1.80
74LS365	0.50
74LS366	0.50
74LS367	0.52
74LS368	0.50
74LS373	0.90
74LS374	0.90
74LS375	0.75
74LS377	1.30
74LS378	0.95
74LS379	1.30
74LS381	4.50
74LS385	3.25
74LS390	0.60
74LS393	1.00
74LS395A	1.00
74LS399	1.40
74LS445	1.80
74LS465	1.20
74LS467	1.20
74LS490	1.50
74LS540	1.00
74LS541	1.00
74LS608	7.00
74LS610	19.00
74LS612	19.00
74LS624	3.50
74LS626	2.25
74LS628	2.25
74LS629	1.25
74LS640	2.00
74LS640-1	3.00
74LS641	1.50
74LS642	2.50
74LS642-1	3.00
74LS643	2.50
74LS643-1	3.00
74LS644	3.50
74LS645	2.00
74LS645-1	4.00
74LS668	0.90
74LS669	0.90
74LS670	1.70
74LS682	2.50
74LS683	3.00
74LS684	3.50
74LS687	3.50
74LS688	3.50
74LS783	21.00

74S SERIES

74S00	0.50
74S02	0.50
74S04	0.50
74S05	0.50
74S08	0.50
74S10	0.50
74S11	0.75
74S20	0.50
74S22	0.50
74S30	0.50
74S32	0.60
74S37	0.60
74S38	0.60
74S40	0.50
74S51	0.60
74S64	0.45
74S74	0.70
74S85	3.00
74S86	1.00
74S112	1.50
74S113	1.20
74S114	1.20
74S124	3.00
74S132	1.00
74S133	0.60
74S138	1.80
74S139	1.80
74S140	1.00
74S151	1.50
74S153	1.50
74S157	2.00
74S158	2.00
74S163	3.00
74S169	5.50
74S174	3.00
74S175	3.20
74S188	1.80
74S189	1.80
74S194	3.00
74S195	3.00
74S196	3.50
74S200	4.50
74S201	3.20
74S225	5.20
74S240	4.00
74S241	4.00
74S244	4.50
74S251	2.50
74S257	2.50
74S258	2.50
74S260	1.00
74S261	3.00
74S283	2.70
74S287	2.25
74S288	2.00
74S289	2.25
74S299	4.50
74S373	4.00
74S374	4.00
74S387	2.25

74C SERIES

74C00	0.70
74C04	0.50
74C08	0.70
74C10	0.70
74C14	0.50
74C20	0.70
74C32	1.00
74C42	1.50
74C48	1.50
74C73	1.00
74C74	1.20
74C76	1.00
74C83	2.00
74C85	2.25
74C86	0.50
74C90	1.90
74C93	1.50
74C95	1.60
74C107	1.00
74C150	5.00
74C151	2.00
74C157	2.50
74C160	1.80
74C161	1.80
74C162	1.80
74C163	1.80
74C173	1.00
74C174	1.50
74C175	1.50
74C193	1.50
74C194	1.50
74C195	1.50
74C221	2.50
74C244	2.00
74C245	2.25
74C373	2.25
74C374	2.25
74C902	1.20
74C911	9.00
74C912	4.50
74C922	6.00
74C923	6.50
74C925	6.50
74C926	7.50

74ALS SERIES

74ALS00	0.45
74ALS02	0.45
74ALS04	0.50
74ALS08	0.50
74ALS10	0.45
74ALS20	0.45
74ALS32	0.45
74ALS74	0.70
74ALS138	1.50
74ALS139	1.50
74ALS244	4.00
74ALS245	4.75
74ALS573	2.60
74ALS574	4.50
74ALS580	2.60

4000 SERIES

4000	0.20
4001	0.24
4002	0.25
4006	0.70
4007	0.25
4008	0.60
4009	0,45
4010	0.60
4011	0.24
4012	0.25
4013	0.36
4014	0.60
4015	0.70
4016	0.36
4017	0.55
4018	0.60
4019	0.60
4020	0.80
4021	0.60
4022	0.70
4023	0.30
4024	0.48
4025	0.24
4026	0.90
4027	0.40
4028	0.60
4029	0.75
4030	0.35
4031	1.25
4032	1.00
4033	1.25
4034	2.50
4035	0.70
4036	2.50
4037	1.10
4038	1.00
4040	0.60
4041	0.55
4042	0.50
4043	0.60
4044	0.60
4045	1.00
4046	0.60
4047	0.60
4048	0.55
4049	0.36
4050	0.35
4051	0.65
4052	0.60
4053	0.60
4054	0.80
4055	0.80
4056	0.85
4060	0.70
4063	0.85
4066	0.40
4067	2.30
4068	0.25
4069	0.24
4070	0.24
4071	0.24
4072	0.24
4073	0.24
4075	0.24
4076	0.65
4077	0.25
4078	0.25
4081	0.24
4082	0.25
4085	0.60
4086	0.75
4089	1.20
4093	0.35
4094	0.90
4095	0.95
4096	0.90
4097	2.70
4098	0.75
4099	0.99
4501	0.36
4502	0.55
4503	0.36
4504	0.95
4505	3.60
4506	0.90
4507	0.35
4508	1.20
4510	0.55
4511	0.55
4512	0.55
4513	1.50
4514	1.10
4515	1.10
4516	0.55
4517	2.20
4518	0.48
4519	0.32
4520	0.60
4521	1.15
4522	0.80
4526	0.70
4527	0.80
4528	0.65
4529	1.00
4531	0.75
4532	0.65
4534	3.80
4536	2.50
4538	0.75
4539	0.75
4541	0.90
4543	0.70
4551	1.00
4553	2.40
4555	0.36
4556	0.50
4557	2.40
4560	1.40
4566	1.40
4568	2.40
4569	1.70
4572	0.45
4583	0.90
4584	0.48
4585	0.60
4724	1.50
14411	7.50
14412	7.50
14416	3.00
14419	2.60
14490	4.20
14495	4.50
145000	6.50
14599	2.00
22100	3.50
22101	7.00
22102	7.00
40014	0.48
40085	1.20
40097	0.36
40098	0.40
40100	1.50
40101	1.25
40102	1.30
40103	2.00
40104	1.20
40105	1.50
40106	0.48
40107	0.55
40108	3.20
40109	0.80
40110	2.25
40114	2.25
40147	2.80
40163	1.00
40173	1.20
40174	1.00
40175	1.00
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40244	1.50
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CA3085	1.50
CA3086	0.60
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LM308CN	0.75
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LM319	1.80
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LM335Z	1.30
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LM339	0.40
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TL064	0.90
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TL072	0.70
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6V 7808	0.50	7908	0.50
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18V 7818	0.50	7918	0.50
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12V 78L12	0.30		
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75109	1.20
75110	0.90
75112	1.60
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75121	1.40
75122	1.40
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75154	1.20
75159	2.20
75160	5.00
75161	3.50
75162	4.00
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75188	0.60
75189	0.60
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75451	0.50
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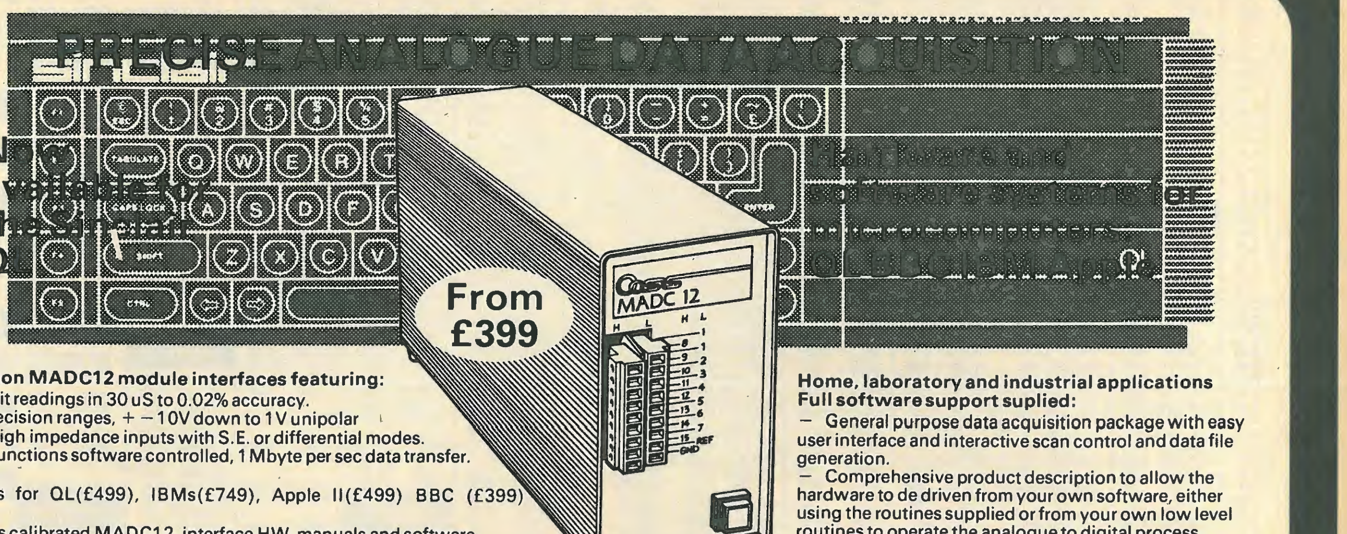

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CIRCLE 56 FOR FURTHER DETAILS.

Intelligent real-time clock

This real-time clock can be added to any 6502 computer. As an example, interfacing details are given for the Apple II.

by P.H. Unstead and A. Blunden

Dr Peter Unstead graduated in physics from Nottingham University in 1960. After gaining his Ph.D. there in 1964 he spent two years with International Nickel designing measuring equipment before moving to the department of physical sciences at the North East London Polytechnic.

Andy Blunden trained as a civil engineer. Since joining the physical sciences department at NELP as a technician he has studied digital electronic design and production.

This circuit is one of a range of interfaces designed to make the Apple II and other 6502 machines more useful in the laboratory. Within the 2K eprom which controls it is additional software to operate several of the other interfaces — among them a v.i.a., a serial interface and d-to-a and a-to-d converters.

The National Semiconductor 58174 real-time clock chip is a metal-gate c-mos circuit which requires a block of 16 consecutive locations in the system's memory map. The access time on a read cycle is typically 1.2μs; temperature and power supply changes may lengthen this time to 2μs. Consideration of the address and bus decoding requirements and timing constraints is therefore necessary if the circuit is to operate reliably.

The circuitry controls the ready pin RDY on the 6502 processor, delaying execution of the read cycle until data is available from the chip some 1.2μs after the address information becomes stable. A 74123 monostable sends RDY low during the ϕ_1 clock period for about 1μs so as to extend the address pulse. With the timing components shown in Fig. 2, the pulse width from the monostable is about 1μs and the read operation occurs after missing one ϕ_2 clock period.

Battery back-up allows timekeeping to continue when the microcomputer is switched off. The circuit trickle-charges the battery and protects against transients when the supply is switched over. Since variations in the supply may affect accuracy, the protection diode is a germanium device to keep the supply near 5V.

Timing is controlled by a 32.768kHz crystal. The variable capacitor at pin 15 (Fig. 1) may be adjusted to calibrate the clock: it runs slow with the plates fully meshed (maximum capacitance), fast with the plates disengaged. The range of control is about 60s per day. For better time-keeping in the battery-backed mode, a fixed capacitor of 10-15pF should be connected between pin 14 and the negative rail. This improvement is not mentioned in the 58174 data sheet.

Apple II interface

The 50-pin expansion slots at the rear of the Apple motherboard provide a variety of signals: data and address buses, power supplies, timing and control signals and in addition, three chip-select signals. Also accessible is pin 2 of the processor, the RDY signal. Unfortunately, the timing requirements of the clock chip make it necessary to derive the chip-select pulses by address-bus decoding and to lengthen the read pulse further by the use of the RDY signal.

The Apple memory-map reserves 16 bytes for input-output signals to devices at each slot (at locations $C0x0, where x=$8 to $F) plus a common area of 2K-bytes extending from $C800 to $CFFF for prom firmware. A further 256 bytes of address space are reserved for prom dedicated to slots 1 to 7, but these have not been used.

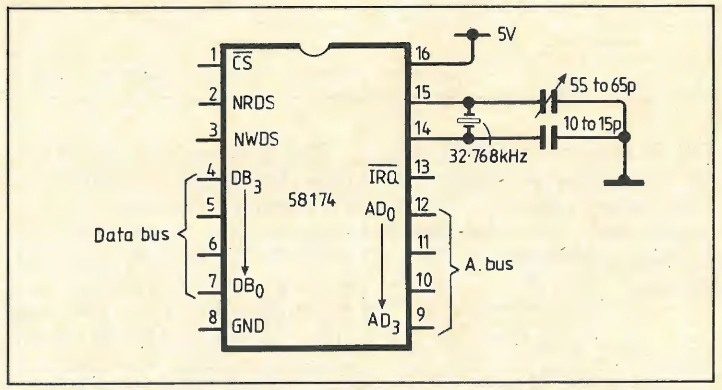

Fig. 1. The MM58174 is a metal-gate c-mos clock-calendar i.c. Features include low-power stand-by operation, an interrupt timer and automatic calculation of leap-years.

Table 1: internal registers of the 58174.

Register	$A_3 - A_0$	Mode
0 Test	0 0 0 0	Write only
1 Tenths of seconds	0 0 0 1	Read only
2 Seconds	0 0 1 0	Read only
3 Tens of seconds	0 0 1 1	Read only
4 Minutes	0 1 0 0	Read or write
5 Tens of minutes	0 1 0 1	Read or write
6 Hours	0 1 1 0	Read or write
7 Tens of hours	0 1 1 1	Read or write
8 Days	1 0 0 0	Read or write
9 Tens of days	1 0 0 1	Read or write
10 Day of the week	1 0 1 0	Read or write
11 Month	1 0 1 1	Read or write
12 Tens of months	1 1 0 0	Read or write
13 Years	1 1 0 1	Write only
14 Stop/start	1 1 1 0	Write only
15 Interrupt status	1 1 1 1	Read or write

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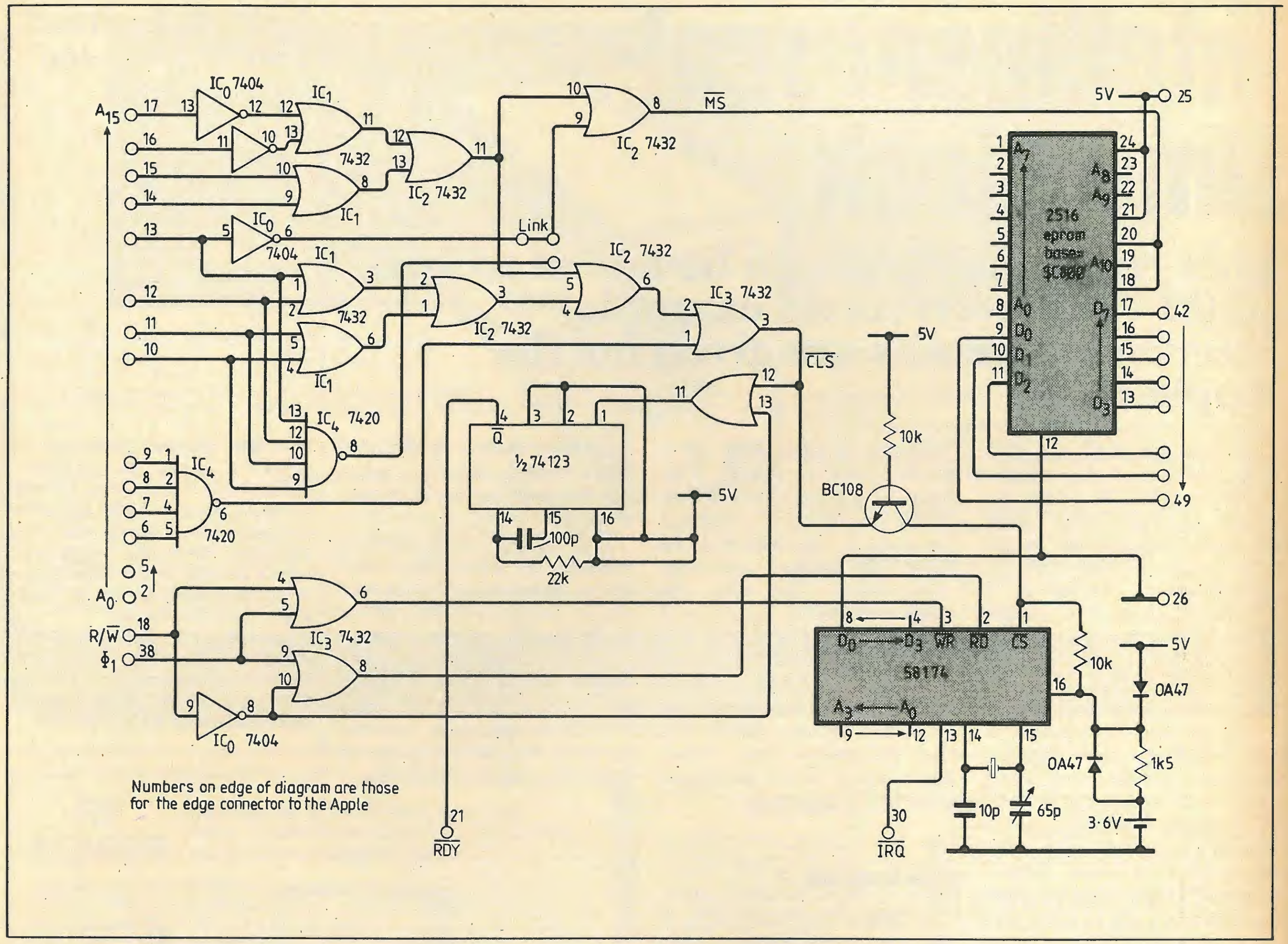

Numbers on edge of diagram are those for the edge connector to the Apple

Fig.2. Hardware interface for the Apple II computer. The unit gives a continuous time display at the bottom of the screen.

The firmware for the real-time clock occupies 256 bytes of 2K eprom, located in the common area from $CF00 to $CFFF. The i/o registers of the clock are situated at $C0F0-$C0FF. Thus the card should be inserted in slot 7 even though no use has been made of the input/output strobes dedicated to that slot.

The decoder is designed such that, if necessary, an eprom can be located on boards which are designed to occupy different Apple slots. The memory-select signal $\overline{MS}$, derived from A_{11} to A_{15}, drives the eprom's chip-select pin. The chip-select signal $\overline{CS}$, derived from A_8 to A_{11}, is combined with the output from pin 11 of IC_2 and a further signal $\overline{BS}$, derived from A_4 to A_7, to produce a clock select signal CLS to access the 16 memory locations $C0F0 to $C0FF. If required, the eprom can be confined to the 256 bytes from $CF00 to $CFFF by moving the link on the board to pin 8 of IC_4.

Software

The software consists of 256 bytes of machine code located at $CF00. Absolute addressing has been used throughout: the only ram locations affected are the text window limit ($23) and the vectors at the top of page 3. No registers are affected by interrupts.

The functions of the clock-chip's 16 internal registers are listed in Table 1. The first 13 of them keep the time: the shortest interval is a tenth of a second and the longest a leap-year.

At the bottom of the screen the time display shows months, day of the week, hours, minutes and seconds. The circuit generates the interrupts which update it.

When operated from a 5V supply, the clock can be programmed to generate interrupts at 0.5, 5 and 60s intervals. It cannot generate interrupts in the battery-backed mode. After an interrupt has been generated it must be cleared by reading register 15, the interrupt register, three times.

After powering the circuit, disable the display before enabling or setting. To set the clock, CALL (52992). Enter the date and time at the flashing cursor, pressing <return> each time. The clock starts with seconds at zero when minutes are entered.

In monitor mode, the time may be read by typing control-J <return> or CF5AG.

To disable the display, CALL (53071). The machine will operate normally whilst the clock continues to keep time. The display can be re-started by CALL (53053). IRQ is vectored via $03F8 to the clock.

To use the clock in machine-code programs use JSR C5FA and read digits from the display. Alternatively, use LDA C0F0,X followed by AND CFC8,X to read the clock directly. ■

The next article will describe an eprom programmer.

```
  1  META ASSEMBLER V3.01  (C) 1986 Andy Green/CRASH BARRIER    (0525) 717148
CLOCK1         Intelligent real-time clock


                     CLOCK1      MODULE
0000C0F0             clk         =          $C0F0
0000CFF7             lpyr        =          $CFF7
00000750             scrn        =          $750
000007D0             face        =          $7D0          clock-face
000007E4             face1       =          $7E4
0000009C             pos0D       =          $9C
0000CFD3             pos         =          $CFD3
0000CFBF             vectors     =          $CFBF
00000023             wndbtm      =          $23
0000CFC7             mask        =          $CFC7
0000CFE0             day1        =          $CFE0
0000CFE8             day2        =          $CFE8
0000CFF0             day3        =          $CFF0
0000C000             kbd         =          $C000
0000C010             kbdstrb     =          $C010
00000045             acc         =          $45
000000AF             stroke      =          $AF           Ascii /
000000BA             colon       =          $BA           Ascii :
000000B0             zero        =          $B0           Ascii 0
00000060             flash       =          $60
0000008D             rtn         =          $8D

0000CF00 78          entry       SEI
0000CF01 A900                    LDA        #0            initialize test
0000CF03 8DF0C0                  STA        clk+0         and interrupt
0000CF06 8DFEC0                  STA        clk+$E        registers
0000CF09 2062CF                  JSR        pronly        print clockface
0000CF0C A008                    LDY        #8
0000CF0E B9F7CF      prlpyr      LDA        lpyr,Y        set leap year
0000CF11 99E407                  STA        face1,Y
0000CF14 88                      DEY
0000CF15 D0F7                    BNE        prlpyr
0000CF17 A09C                    LDY        #pos0D
0000CF19 209DCF                  JSR        keyin
0000CF1C 2903                    AND        #3
0000CF1E AA                      TAX
0000CF1F E8                      INX
0000CF20 A910                    LDA        #$10
0000CF22 4A          loop1       LSR        A
0000CF23 CA                      DEX
0000CF24 D0FC                    BNE        loop1
0000CF26 8DFDC0                  STA        clk+$D
0000CF29 A20C                    LDX        #$C
0000CF2B BCD3CF      timein      LDY        pos,X         set time
0000CF2E 209DCF                  JSR        keyin
0000CF31 9DF0C0                  STA        clk,X
0000CF34 CA                      DEX
0000CF35 E003                    CPX        #3
0000CF37 D0F2                    BNE        timein
0000CF39 8EFEC0                  STX        clk+$E
0000CF3C EA                      NOP
0000CF3D A008        enable      LDY        #8            enable clock
0000CF3F B9BFCF      vctr        LDA        vectors,Y     initialize IRQ
0000CF42 99F703                  STA        $3F7,Y        and USR vectors
0000CF45 88                      DEY
0000CF46 D0F7                    BNE        vctr
0000CF48 C623                    DEC        wndbtm        lift text window
0000CF4A 58                      CLI
0000CF4B A909                    LDA        #9
0000CF4D D005                    BNE        clear
0000CF4F A918        disable     LDA        #$18          disable clock
0000CF51 8523                    STA        wndbtm        restore
0000CF53 78                      SEI                      text window
0000CF54 8DFFC0      clear       STA        clk+$F
0000CF57 8DFFC0                  STA        clk+$F        set interrupt mode
0000CF5A A203        prclk       LDX        #3            clear interrupt
0000CF5C 2CFFC0      loop2       BIT        clk+$F
0000CF5F CA                      DEX
0000CF60 D0FA                    BNE        loop2
0000CF62 A9BA        pronly      LDA        #colon        print clock face
0000CF64 8DD207                  STA        face+2
0000CF67 8DD507                  STA        face+5
0000CF6A A9AF                    LDA        #stroke       Ascii /
0000CF6C 8DDD07                  STA        face+$D
0000CF6F A20C                    LDX        #$C
0000CF71 BDC7CF      digitx      LDA        mask,X        mask out unwanted
0000CF74 F00B                    BEQ        skippr        bits
0000CF76 3DF0C0                  AND        clk,X         read clock
0000CF79 09B0                    ORA        #zero         convert to Ascii
0000CF7B BCD3CF                  LDY        pos,X         read position
0000CF7E 995007                  STA        scrn,Y        print
0000CF81 CA          skippr      DEX
0000CF82 D0ED                    BNE        digitx
0000CF84 ADFAC0                  LDA        clk+$A        print day of week
0000CF87 2907                    AND        #7
0000CF89 AA                      TAX
0000CF8A BDE0CF                  LDA        day1,X
0000CF8D 8DD807                  STA        face+8
0000CF90 BDE8CF                  LDA        day2,X
0000CF93 8DD907                  STA        face+9
0000CF96 BDF0CF                  LDA        day3,X
0000CF99 8DDA07                  STA        face+$A
0000CF9C 60                      RTS

0000CF9D A960        keyin       LDA        #flash        subroutine to
0000CF9F 995007      keypr       STA        scrn,Y        input Ascii
0000CFA2 AD00C0      keypoll     LDA        kbd           characters from
0000CFA5 10FB                    BPL        keypoll       keyboard and
0000CFA7 8D10C0                  STA        kbdstrb       output to screen
0000CFAA C98D                    CMP        #rtn
0000CFAC D0F1                    BNE        keypr
0000CFAE B95007                  LDA        scrn,Y
0000CFB1 60                      RTS
```

```
  1  META ASSEMBLER V3.01  (C) 1986 Andy Green/CRASH BARRIER    (0525) 717148
CLOCK1         Intelligent real-time clock


0000CFB2 8A          isr         TXA                      interrupt
0000CFB3 48                      PHA                      service routine
0000CFB4 98                      TYA
0000CFB5 48                      PHA
0000CFB6 20F803                  JSR        $3F8          user vector
0000CFB9 68                      PLA                      redirects to prclk
0000CFBA A8                      TAY
0000CFBB 68                      PLA
0000CFBC AA                      TAX
0000CFBD A545                    LDA        acc
0000CFBF 40                      RTI
0000CFC0 4C5ACF4C    data        EQUD       $4CCF5A4C
0000CFC4 07F9B2CF                EQUD       $CFB2F907
0000CFC8 000F070F                EQUD       $0F070F00
0000CFCC 070F030F                EQUD       $0F030F07
0000CFD0 03000F01                EQUD       $010F0003
0000CFD4 FF878684                EQUD       $848687FF
0000CFD8 8381808C                EQUD       $8C808183
0000CFDC 8B888F8E                EQUD       $8E8F888B
0000CFE0 C4CDD4D7                EQUD       $D7D4CDC4
0000CFE4 D4C6D3D3                EQUD       $D3D3C6D4
0000CFE8 C1CFD5C5                EQUD       $C5D5CFC1
0000CFEC C8D2C1D5                EQUD       $D5C1D2C8
0000CFF0 D9CEC5C4                EQUD       $C4C5CED9
0000CFF4 D2C9D4CE                EQUD       $CED4C9D2
0000CFF8 CCD0AFD9                EQUD       $D9AFD0CC
0000CFFC D2A0ABB0                EQUD       $B0ABA0D2

0000D000                         END
Assembly Complete
```

Editorial acknowledgement: our thanks to Andy Green of Crash Barrier for the use of his Meta assembler for the BBC Micro in preparing these listings.

Table 2: memory dump of the clock software.

```
CF00   78 A9 00 8D F0 C0 8D FE   x)..p@.~
CF08   C0 20 62 CF A0 08 B9 F7   @ bO .9w
CF10   CF 99 E4 07 88 D0 F7 A0   O.d..Pw
CF18   9C 20 9D CF 29 03 AA E8   .  .O).*h
CF20   A9 10 4A CA D0 FC 8D FD   ).JJP  .}
CF28   C0 A2 0C BC D3 CF 20 9D   @".<SO  .
CFCF   CF 9D F0 C0 CA E0 03 D0   O.p@J'.P
CF38   F2 8E FE C0 EA A0 08 B9   r.~@j .9
CF40   BF CF 99 F7 03 88 D0 F7   ?O.w..Pw
CF48   C6 23 58 A9 09 D0 05 A9   F#X).P.)
CF50   18 85 23 78 8D FF C0 8D   ..#x..@.
CF58   FF C0 A2 03 2C FF C0 CA   .@".,.@J
CF60   D0 FA A9 BA 8D D2 07 8D   Pz):.R..
CF68   D5 07 A9 AF 8D DD 07 A2   U.)/.].""
CF70   0C BD C7 CF F0 0B 3D F0   .=GOp.=p
CF78   C0 09 B0 BC D3 CF 99 50   @.0<SO.P
CF80   07 CA D0 ED AD FA C0 29   .JPm-z@)
CF88   07 AA BD E0 CF 8D D8 07   .*='O.X.
CF90   BD E8 CF 8D D9 07 BD F0   =hO.Y.=p
CF98   CF 8D DA 07 60 A9 60 99   O.Z.')'.
CFA0   50 07 AD 00 C0 10 FB 8D   P.-.@.{.
CFA8   10 C0 C9 8D D0 F1 B9 50   .@I.Pq9P
CFB0   07 60 8A 48 98 48 20 F8   .'.H.H x
CFB8   03 68 A8 68 AA A5 45 40   .h(h*%E@
CFC0   4C 5A CF 4C 07 F9 B2 CF   LZOL.y2O
CFC8   00 0F 07 0F 07 0F 03 0F   ........
CFD0   03 00 0F 01 FF 87 86 84   ........
CFD8   83 81 80 8C 8B 88 8F 8E   ........
CFE0   C4 CD D4 D7 D4 C6 D3 D3   DMTWTFSS
CFE8   C1 CF D5 C5 C8 D2 C1 D5   AOUEHRAU
CFF0   D9 CE C5 C4 D2 C9 D4 CE   YNEDRITN
CFF8   CC D0 AF D9 D2 A0 AB B0   LP/YR +0
```

by L.C. Walters, M.A., M.I.E.R.E.

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The 'out-phasing' method of s.s.b. modulation, using a Hilbert transformer, can be used for speech, since the ear is insensitive to phase

Single-sideband (s.s.b.) modulation can, in theory, be achieved by the so-called "out-phasing" method, which depends upon the identity

$$\Sigma a_r \cos(\omega_r t+\phi_r)\cos\omega t \pm$$
$$\Sigma a_r \sin(\omega_r t+\phi_r)\sin\omega t$$
$$=\Sigma a_r \cos[(\omega\pm\omega_r)t\pm\phi_r]$$

This last represents s.s.b. modulation of a carrier of frequency $\omega/2\pi$ by a waveform $\Sigma a_r\cos(\omega_r t+\phi_r)$ which can be any real waveform. (The upper sign corresponds to lower sideband, u.s.b., and the lower sign to lower sideband, l.s.b. modulation.) Thus, in order to implement an s.s.b. modulator using this principle, we require a device which will convert a given waveform $S(t) = \Sigma a_r\cos(\omega_r t+\phi_r)$ into a related waveform $\hat{S}(t) = \Sigma a_r\sin(\omega_r t+\phi_r)$. Such a device is called a Hilbert transformer, since $\hat{S}(t)$ is precisely the mathematical Hilbert transform of S(t) defined by

$$\hat{S}(t)=(1/\pi)\int_{-\infty}^{\infty} d\tau s(\tau)/(t-\tau)$$

In general, true Hilbert transformers present some difficulty in implementation but, fortunately from a practical viewpoint, a major application is to s.s.b. by speech where one can exploit the fact that the human ear is substantially insensitive to the phase of audio signals. Thus, for speech s.s.b., it is sufficient, given a speech waveform $S(t) = \Sigma a_r\cos(\omega_r t+\phi_r)$ to produce two waveforms:

$$g(t)=\Sigma a_r\cos(\omega_1 t+\phi_r+\psi_r)$$

and

$$\hat{g}(t)=\Sigma a_r\sin(\omega_1 t+\phi_r+\psi_r)$$

where the ψ_r can be arbitrary functions of the ω_r. Note that since $\hat{g}(t)$ is g(t) with a $\pi/2$ phase shift at all frequencies, the ear will not distinguish between S(t), g(t) and $\hat{g}(t)$.

Although the device which produces g(t) and $\hat{g}(t)$ from S(t) is not a true Hilbert transformer, for speech s.s.b. it is just as effective. It is such a device which we consider here and, in conformity with common usage, describe, albeit inaccurately, as a Hilbert transformer.

In practice, even this type of device cannot be realised with perfect precision over infinite bandwidths so that, as always, engineering compromises must be sought. The device considered here is a hardware analogue circuit implementation which, of course, can also be realised in the form of a hybrid circuit or a silicon chip. In such cases, the analysis given below permits the designer to select convenient component values, but the explicit circuit described was implemented in discrete components and in consequence uses preferred values of resistance and capacitance, using series or parallel combinations where necessary to achieve sufficient accuracy.

Basic circuit

Various circuit topologies can be considered to achieve the desired aim but one which has been widely used and which forms the basis of the present article is as shown in Fig. 1. This gives a phase shift which is a function of frequency and by suitable choice of components can be made to give an overall gain which, in theory, is constant for all frequencies and in practice is certainly substantially constant over the audio range.

A second such circuit, using different component values, can give different phase shifts and again, by suitable choice of these values, the gain can be made constant and equal to that of the first circuit, and more importantly the phase shift can be made almost 90° more (or less) than that of the first circuit. Thus by feeding both circuits with an input S(t), two outputs g(t) and $\hat{g}(t)$ can be obtained as desired.

The relative phase shift is precisely $\pi/2$ only at four frequencies and there is a trade-off between the maximum phase error within the operating bandwidth and the magnitude of that bandwidth.

A circuit of this type has been commonly employed in which the bandwidth is strictly confined to the nominal s.s.b. "speech" bandwidth of 300 to 3000Hz. Within this band it gives good performance, (perhaps better than can easily be exploited) but outside it, performance drops off quite rapidly.

Since, in many applications, filtering is also used to achieve adequate suppression of the unwanted sideband, a major function of the out-phasing technique can be to ease the specification requirements of the filter response, particularly in relation to the steepness of its "skirts".

It therefore occurred to the author that it might be desirable to extend the bandwidth of the device even at the expense of a small degradation of performance within that band. However, it was first necessary to define acceptable performance limits.

Phase and amplitude tolerances

A fully comprehensive analysis is highly complicated, but for present purposes it is sufficient to consider modulation by a single sinusoid of frequency $p/2\pi$ and to separate the effects of amplitude and the phase errors.

Suppose that we attempt to achieve s.s.b. by the out-phasing method but that our Hilbert transformer introduces a phase error δ and that in the addition (subtraction) process a practical amplitude error Δ occurs. (We may, of course, normalise nominal amplitudes to unity.) Thus our "s.s.b." output will be

$$X(t)=\cos pt\cos\omega t \pm (1+\Delta)\sin(pt+\delta)\sin\omega t.$$

Let

$$X(t)=A\cos[\omega\mp p)t+\phi]+B\cos[\omega\mp p)t+\psi]$$

and suppose A corresponds to the desired sideband, so that ideally B = 0. Then after some manipulation we obtain

$$A^2=1/2\,[(1+\Delta)(1+\cos\delta)+\Delta^2/2]$$
$$B^2=1/2\,[(1+\Delta)(1-\cos\delta)+\Delta^2/2]$$

Then

$$B^2/A^2=\frac{[1-\cos\delta+\Delta^2/2(1+\Delta)]}{[1+\cos\delta+\Delta^2/2(1+\Delta)]}$$

Let us now consider an amplitude error only and let $\delta = 0$. Then $B^2/A^2=\Delta^2/(2+\Delta)^2 \simeq \Delta^2/4$ if Δ is small.

Thus we may obtain Table 1 for unwanted sidelobe level (u.s.l.) compared with the wanted level

Δ	0.01	0.03	0.05	0.06	0.08	0.1
u.s.l.(dB)	−46	−36.6	−32.3	−30.7	−28.3	−26.4

Considering now a phase error only (i.e. $\Delta = 0$)

$$B^2/A^2=(1-\cos\delta)/(1+\cos\delta)\simeq\delta^2/4$$

if δ is small. Table 2 gives the corresponding u.s.l. values as a function of δ.

δ(deg)	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0
u.s.l.(dB)	−47.2	−41.2	−37.7	−35.2	−33.2	−31.6	−30.3	−29.1	−28.1	−27.2

Now a value of $\Delta = 0.03$ corresponds to an amplitude match to within about 0.25dB, which is probably as good as one could expect from a fairly cheap general-purpose design of s.s.b. modulator, while $\Delta = 0.06$ corresponds to a match within about 0.5dB. By reference to Table 1 it would appear that for general-purpose design, using discrete components, it is probably unrealistic to aim for a u.s.l. of better than 30 to 35dB below the wanted sideband level. (Note, however, that for designs where accurate matching can be achieved better performance is attainable. This might apply for example to hybrid implementations.)

With this limitation of aims in mind it appears from Table 2 that a phase error of 2° to 3° is unlikely to result in much degradation in practice. In fact a 3° phase error and a 0.8dB ($\Delta=0.04$) amplitude mismatch combined, theoretically still give a u.s.l. of −30dB.

Allowing for some small errors in design implementation due to component tolerances and/or setting accuracies it seems reasonable to set a design target of 2° maximum phase error. Since over most of the band the error will be substantially less than this, the u.s.l. achieved is then likely to depend as much upon imperfections in the rest of the s.s.b. system as upon the Hilbert transformer itself. (In fact, the performance of the transformer is still useful up to about 8° phase error, giving further bandwidth coverage.)

Discrete-component design

It is inevitable that performance will depend on the accuracy of component values. For the discrete component version it is recommended that silver-mica capacitors and high-stability resistors be used with not worse than 2% tolerance limits. (If higher accuracy components are available the designer can exploit this as shown later).

In addition, the operational amplifiers should have high input impedance and high open-loop gain over the audio band, as well as low offset currents. The author employed type CA3140 amplifiers. The experimental version also incorporated a resistor and potentiometer (to permit fine adjustment) in each half of the circuit. This is shown dotted in Fig. 2 where it replaces (when used) the 330Ω resistor.

The complete discrete-component circuit is shown in Fig. 2, and Fig. 3 shows the theoretical and measured phase performance on an expanded scale. The available test gear did not permit comparison of output amplitudes to better than 0.1dB (corresponding to $\Delta<0.012$) but any amplitude imbalance was certainly less than this from less than 200Hz to more than 8kHz. (Detailed measurement were not carried out outside this range.) The slight irregularities in the measured phase response reflect measurement inaccuracies.

It will be seen that the 2° maximum error criterion is substantially achieved over a band extending from 240Hz to 3.7kHz which, in conjunction with well designed balanced modulators and combiners, should permit attainment of u.s.ls of better than −30dB over that band. The extended bandwidth should also ease the roll-off requirements of filters used to enhance u.s.l. suppression.

In fact, for easing filter requirements, the lower frequency limit is probably more significant than the upper and a slightly different design may be preferable, as described later. However, the author's requirements at the time were not confined to attending to the lower frequency limit.

The analysis given below explains the derivation of the circuit and of its theoretical performance and also permits designers who so wish to implement different phase tolerance/bandwidth compromises.

No detailed tolerance analysis has been performed, but if the recommended components are employed it is thought unlikely that the maximum phase error will exceed 4° corresponding at worst to −29dB u.s.l.

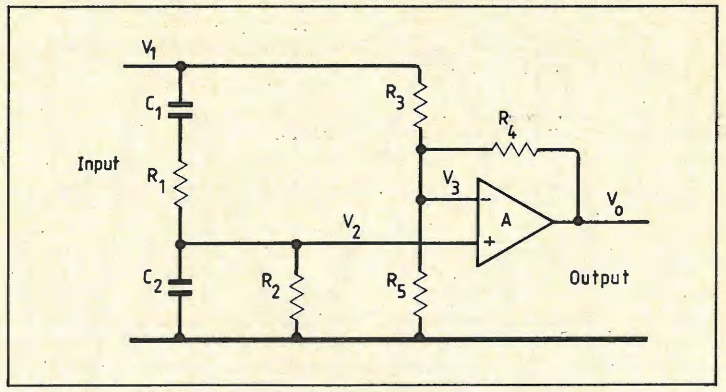

Fig. 1. Basic phase-shift circuit, giving constant gain over a range of frequencies.

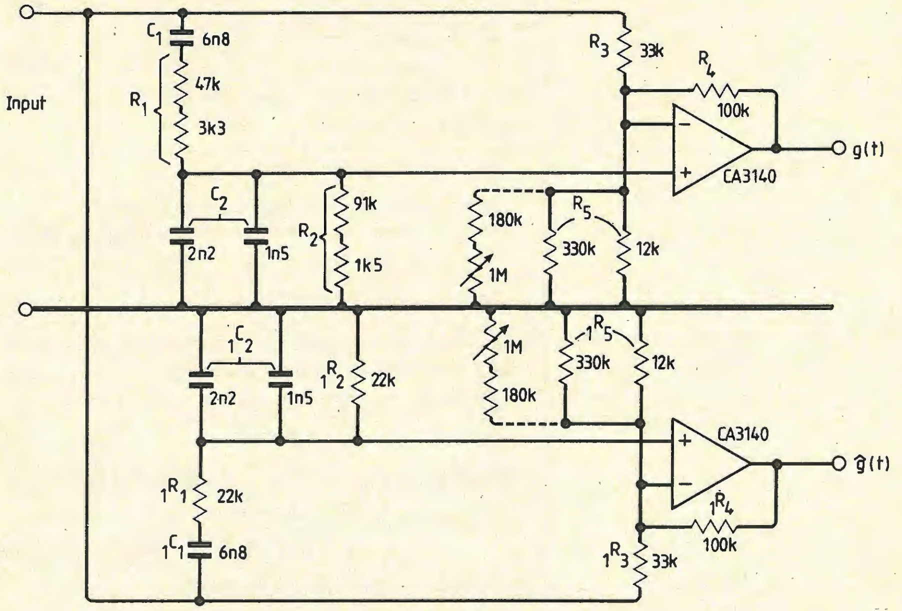

Fig. 2. Practical, experimental circuit. The IMΩ pot and 180k resistor can be incorporated to enable fine adjustment. Delete the 330k resistor to use the two extra components.

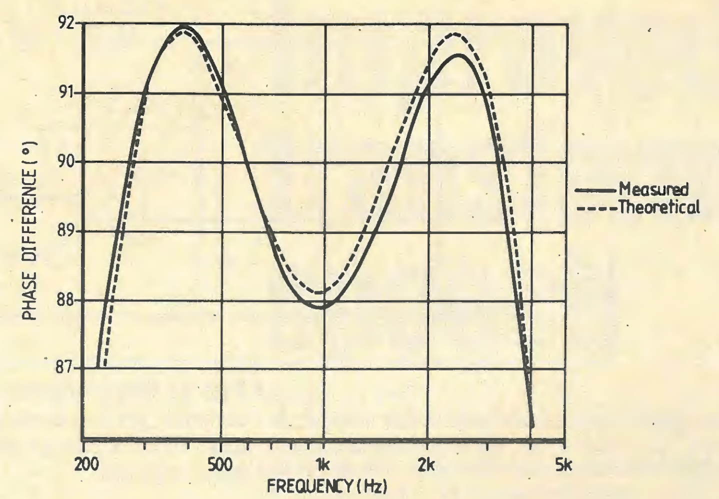

Fig. 3. Theoretical and measured phase performance of the Fig. 2. circuit.

Analysis

The basic circuit is shown in Fig. 1. Assuming the input impedance of the amplifier is very large

$$V_2 = Z_2V_1/(Z_1+Z_2) \tag{1}$$

where $Z_1=(1+j\omega C_1R_1)/j\omega C_1$

and $Z_2=R_2/(1+j\omega C_2R_2)$

Let $C_1R_1=T_1$, $C_2R_2=T_2=aT_1$; $R_2R_1=k$ and $\omega T_1=x$ (2)
(Clearly x is a "normalized" frequency).

Then $Z_1=R_1(1+jx)/jx$
and $Z_2=kR_1/(1+jax)$

$$Z_2/(Z_1+Z_2)=jkx/[1+jx(1+a+k)-ax^2]$$

i.e. $V_2=jkxV_1/[1+jx(1+a+k)-ax^2]$ (3)

Also $(V_1-V_3)/R_3$ + $(V_0-V_3/R_4$ = V_3/R_5 and V_0 = $A(V_2-V_3)$ where A is the open-loop voltage gain of the amplifier.

After some algebraic manipulation and making the assumption that AR_3R_5 is very much larger than $(R_3R_4+R_4R_5+R_5R_3)$ we obtain

$$V_0=(-V_1R_4/R_3)[1\text{-}ax^2+jx(1+a+k)-$$
$$jkx(1+R_3/R_5+R_3/R_4)]/[1-ax^2+jx(1+a+k)]$$

Let $R_3(1/R_4+1/R_5)=\mu$

Then

$$V_0=(-V_1R_4/R_3)\frac{[1-ax^2+jx(1+a-\mu k)]}{[1-ax^2+jx(1+a+k)} \tag{4}$$

Clearly, if we make $1+a-\mu k=-(1+a+k)$ (5)

then the transfer gain

$$|V_0/V_1|=R_4/R_3 \text{ for all x.}$$

Thus we achieve constant gain at all frequencies.

From (4), using conventional notation for phase shifts

$$V_0=(V_1R_4/R_3)\angle 2\theta \tag{6}$$

where $\tan\theta=x(1+a+k)/(1-ax^2)$ (7)

Now consider a second such circuit with component values indicated by the prefix 1 and let

$${}_1T_1=bT_1;\ {}_1T_2=cT_1;\ {}_1R_2/{}_1R_1=k_1$$
$${}_1R_3=R_3;\ {}_1R_4=R_4;\ {}_1R_5=R_5 \tag{8}$$

If this circuit is also fed with V_1 its output will be (from 4).

$${}_1V_0=(V_1R_4/R_3)\frac{[1-bcx^2+jx(b+c-\mu bk_1)]}{[1-bcx^2+jx(b+c+bk_1)]} \tag{9}$$

As before ${}_1V_0/V_1=R_4/R_3$ if we make

$$b+c-\mu bk_1=-(b+c+bk_1) \tag{10}$$

in which case

$${}_1V_0=(-V_1R_4/R_3)\angle 2\theta_1$$

where $\tan\theta_1=x(b+c+bk_1)/(1-bcx^2)$ (11)

We require $2(\theta-\theta_1)=\pm\pi/2$ i.e. $\theta-\theta_1=\pm\pi/4$ and tan $(\theta-\theta_1)=\pm 1$.
But $\tan(\theta-\theta_1)=(\tan\theta-\tan\theta_1)/(1+\tan\theta\tan\theta_1)$

$$=\frac{x[1+a+k-b-c-bk_1-x^2[bc(1+a+k)-a(b+c+bk_1)]]}{[1+x^2[(1+a+k)(b+c+bk)-a-bc]+abcx^4]}$$

Now let $k_1=k$

Then from (5) $2(1+a)=(\mu-1)k$
and from (10) $2(b+c)=(\mu-1)bk$
or $2(1+c/b)=(\mu-1)k$
where $c=ab$ (12)

$$\text{Then } \tan(\theta-\theta_1)=\frac{x(1-b)(1+a+k)(1+x^2ab)}{1+x^2[b(1+a+k)^2-a(1-b^2)]+a^2b^2x^4}$$

$$\text{Let } x\sqrt{ab}=y \tag{13}$$

so that y is also a "normalized" frequency.

$$\text{Then } \tan(\theta-\theta_1)=\frac{[(1-b)(1+a+k)/\sqrt{ab}][y+1/y]}{[y^2+1/y^2+(1+a+k)^2/a-(1+b^2)/b]}$$

$$\text{Put } y+1/y=Z \tag{14}$$

$$\text{Then } \tan(\theta-\theta_1)=\frac{[(1-b)(1+a+k)/\sqrt{ab}]Z}{[Z^2+(1+a+k)^2/a-(1+b^2)/b-2]} \tag{15}$$

From symmetry we clearly let $y=1$ at the geometric band centre since at this point $Z(y)=Z(1/y)$. Note that at this point $Z=2$.

We therefore need consider only $y\geqq 1$ and $Z\geqq 2$. Suppose the ratio of the maximum frequency required to the minimum frequency is n^2. Then we need consider only $2\leqq Z\leqq n+1/n$ and over this range we wish tan $(\phi-\phi_1)$ to equal unity as closely as possible. (Note that the alternative solution $\tan(\phi-\phi_1)=-1$ is merely equivalent to interchanging the two phase shift circuits which comprise the transformer.)

$$\text{Let } (1+a+k)/\sqrt{a}=\varrho;\ (1-b)/\sqrt{b}=\theta \tag{16}$$

$$\text{Then } \tan(\phi-\phi_1)=\varrho\theta Z/(Z^2+\varrho^2-\theta^2-4) \tag{17}$$

From (14), the values at y and 1/y are equal, so that for optimum performance we require tan $(\phi-\phi_1)$ to be approximately unity for all Z between mid-band $(Z=2)$ and the band edge $(Z=n+1/n)$, and to have a value $(1-\alpha)$ say at $Z=2$ and at $Z=n+1/n$ and a value $1/(1+\alpha)$ at the intermediate maxima.

Hence, from (17)

$$2\varrho\theta/(\varrho^2-\theta^2)=1-\alpha=\varrho\theta(n+1/n)/[(n+1/n)^2+\varrho^2-\theta^2-4]$$

$$\text{Giving } \varrho^2-\theta^2=2(n+1)^2/n \tag{18}$$

Now from (17),

$$d/dZ[\tan(\phi-\phi_1)]=0 \text{ when } Z=\sqrt{\varrho^2-\theta^2-4}$$

and at this point $\tan(\phi-\phi_1)=\varrho\theta/2\sqrt{\varrho^2-\theta^2-4}$. (This is clearly the point of maximum phase error.) Thus we require

$$\varrho\theta/2\sqrt{\varrho^2-\theta^2-4}=(\varrho^2-\theta^2)/2\varrho\theta$$

i.e. $$\varrho^2\theta^2=(\varrho^2-\theta^2)\sqrt{\varrho^2-\theta^2-4}$$

Hence from (18) $\varrho\theta=\sqrt{2/n}\,(n+1)[2(n+1)^2/n-4]^{1/2}$
$$=\sqrt{2/n}\,(n+1)[2(n^2+1)/n]^{1/2} \tag{19}$$

Table 3 on p.23 shows values of $\varrho\theta$, $\varrho^2-\theta^2$, ϱ, θ α and the peak angular error for a range of values of n. Note that the angular error is the total error of the transformer, i.e. the error in $2(\phi-\phi_1)$. This error is readily derived as 2 arc tan $[(n+1)/\{8n(n^2+1)^{1/2}\}^{\hat{}}-\pi/2$.

In this table, the values of the parameters are given with what may appear to be pedantic accuracy. However,

since, as will appear later, the circuit component values must be derived from these values by a rather devious process, it is desirable to minimize any approximations until these component values are obtained, especially since the *total* parameter variation over the whole range from $n=3$ to $n=4$ is only about 7% in some instances.

Now from (16) $\theta=(1-b)/\sqrt{b}$

or $b^2-(2+\theta^2)b+1=0$

i.e. $$b=1+\theta^2/2\pm\theta\sqrt{1+\theta^2/4} \tag{20}$$

From (16) also, $1+a+k=\varrho\sqrt{a}$

i.e. $a^2+a[\{2(1+k)-\varrho^2\}]+(1+k)^2=0$

or $$a=1+k-\varrho^2/2\pm\varrho\sqrt{\varrho^2/4-1-k} \tag{21}$$

At the "mid-band" point $y=1$ and $Z=2$

i.e. from (13) $x=1/\sqrt{ab}$

If the geometric mean "mid-band" frequency is $\omega_o/2\pi$ this gives

$$T_1=1/\omega_0\sqrt{ab} \tag{22}$$

For a given choice of k we can then obtain $T_2\,(=aT_1)$ from (2). From (8) we can obtain ${}_1T_1\,(=bT_1)$ and $T_2\,(=cT_1$ = abT_1 from (12)). From (5) we obtain the value of μ thus completing the design.

A commonly used circuit has $a=1$, $b=0.256$, $\varrho=3.58$, $\theta=1.47$ which accords well with Table 3 but corresponds to $n=3$ giving only a 9:1 bandwidth ratio, (usually 330Hz to 3000Hz).

For the rather wider band design the author also chose $a=1$ so that $\varrho=2+k$ from (16). It was decided to aim at $n\sim 3.8$ corresponding to a bandwidth ratio of about 14.4 as a compromise between this ratio and the peak probable angular error allowing for component tolerances.

From Table 3, for $n=3.8$, $\varrho\sim 3.8$ whence $k\sim 1.8$ Then choosing $C_1=6800$pF gives $C_2=6800/1.8$ from (2); i.e. $C_2=3777$pF. This can be approximated by a parallel combination of 2200pF and 1500pF giving $C_2=3700$pF and corresponding to $k=1.83784$ and $\varrho=3.83784$. From Table 3 this requires $\theta\approx 1.553$ or $b\approx 0.23969$ from (20) implying $n\sim 3.9$ or a 15.2 bandwidth ratio.

For the author's purposes a "mid-band" frequency of 950Hz was chosen (although for simple s.s.b. purposes aimed at alleviating filter requirements a rather lower value may be preferable). This corresponds to $\omega_0=5970$ and gives band "edges" at 243Hz and 3705Hz. From (22) we then obtain

$$T_1=1/5970\sqrt{0.23969}=3.421\times 10^{-4}$$

Thus for $C_1=6800$pF, $R_1=50.31$kΩ, approximated well by 47kΩ and 3.3kΩ in series.

Then $R_2=R_1k=92.462$kΩ, approximated by 91kΩ and 1.5kΩ in series.

${}_1T_1=bT_1=0.82\times 10^{-4}$ and if ${}_1C_1=6800$pF,
${}_1R_1=12.06$kΩ which is sufficiently close to 12kΩ.

Then ${}_1R_2={}_1R_11k=22.05$kΩ for which 22kΩ will suffice.

${}_1C_2=C_2$ approximated as before by 2200pF and 1500pF in parallel.

From (5) $\mu=3.1765$. The gain of each circuit is R_4/R_3 and if we make this about 3 we can use $R_3=33$kΩ, $R_4=100$kΩ.

Then $\mu=R_3(1/R_4+1/R_5)=0.33+R_3/R_5=3.1765$

Hence $R_3/R_5=2.8465$ or $R_5=11.593$kΩ which is adequately approximated by 12kΩ shunted by 330kΩ (giving a nominal 11.579kΩ).

However, in the experimental circuit the author wished to be able to adjust the value of μ empirically (and differentially in the two halves of the circuit) to enable the closest approximation to the theoretical performance to be achieved despite the inevitable deviation of components from their nominal values. To this end, the 330kΩ shunt in the implementation of R_5 was replaced by a series combination of 180kΩ and a 1MΩ potentiometer as shown dotted in Fig. 2.

Figure 2 shows the final circuit as implemented and Fig. 3 shows the measured and theoretical performance after optimal adjustment of the 1MΩ potentiometers. (Note that the variation attainable in the effective value of R_5 is 11.25kΩ to 12kΩ or −3% to +3.5% about the nominal. Such variation gave noticeable but small degradation of performance, tending to confirm that component values should be as accurate as possible and that 2% tolerance values are just about acceptable).

It should be noted that although the "limits" defined by the factor n give the range over which the specified performance can in theory be achieved, performance is still quite good over a much larger frequency range. Thus, u.s.ls should be less than −27dB at least from 173Hz to 5.2kHz.

Table 3

n	$\varrho^2-\theta$	$\varrho\theta$	α	ϱ	θ	angular error (deg)
3.0	10.6667	5.2479	0.016005	3.57990	1.46595	0.92
3.1	10.8452	5.3268	0.017669	3.60885	1.47603	1.02
3.2	11.0250	5.4057	0.019376	3.63775	1.48600	1.12
3.3	11.2061	5.4847	0.021123	3.66656	1.49586	1.22
3.4	11.3882	5.5637	0.022905	3.69528	1.50562	1.33
3.5	11.5714	5.6427	0.024716	3.72390	1.51527	1.43
3.6	11.7556	5.7217	0.026555	3.75241	1.52481	1.54
3.7	11.9405	5.8006	0.028416	3.78080	1.53423	1.65
3.8	12.1263	5.8795	0.030297	3.80905	1.54355	1.76
3.9	12.3128	5.9582	0.032194	3.83717	1.55276	1.87
4.0	12.5000	6.0368	0.034105	3.86515	1.56186	1.99

Second design

If the chief interest centres on the lower frequency limit, as in cases where relaxation of filter requirements is a major aim, it may be preferable to use components as given below. These should give a lower "limit" of 200Hz and an upper "limit" of 3040Hz for the same peak angular errors as above.

component	design value	suggested implementation
C_1 and, ${}_1C_1$	6800pF	6800pF
C_2 and, ${}_1C_2$	3700pF	2200pF shunted by 1500pF
R_1	61.3kΩ	68kΩ shunted by 620kΩ
R_2	112.66kΩ	300kΩ shunted by 180kΩ
${}_1R_1$	14.693kΩ	10kΩ and 4.7kΩ in series
${}_1R_2$	27.00kΩ	27kΩ
R_3	33kΩ	33kΩ
R_4	100kΩ	100kΩ
R_5	11.593kΩ	12k shunted by 330kΩ

Third design

In some applications, adequate u.s.l. suppression may be obtained by filtering alone at frequencies near the top end of the band, e.g. above say 2.5kHz. In such a case almost the sole purpose of the outphasing technique may be to ease the filter requirements at the lower end of the band. Using the analysis provided one can readily design for this case also, but the design in Table 4 may be of interest as an example.

Without further filtering it should give a u.s.l. of better than −30dB from less than 100Hz to almost 1.5kHz, better than −27dB from 70Hz to over 2kHz and better than −24dB from 55Hz to 2.6kHz.

Of course, in normal usage the audio coupling system will ensure a roll off energy below about 300Hz which combined with the natural spectrum of speech should make energy levels from 0 to 300Hz on the unwanted sideband very low compared with the main wanted sideband energy. Similar, when combined with suitable filters, excellent u.s.ls should be readily attainable over the range from 100Hz upwards.

component	design value	suggested implementation
C_1 and, ${}_1C_1$	4700pF	4700pF
C_2 and, ${}_1C_2$	2557pF	2200pF shunted by 330pF*
R_1	180kΩ	180kΩ
R_2	330kΩ	330kΩ
${}_1R_1$	43.4kΩ	68kΩ shunted by 120kΩ
${}_1R_2$	210kΩ	420kΩ shunted by 420kΩ
R_3	33kΩ	33kΩ
R_4	100kΩ	100kΩ
R_5	11.593kΩ	12kΩ shunted by 330kΩ

(*A further shunt component of 27pF gives precisely the nominal value rather than the nominal 1.25% error in the simpler implementation)

The design procedure is summarised as follows (with $a=1$).

Define operating bandwidth U as the ratio of the higher (f_u) frequency in the band over which optimum performance is required or is achievable.

1(a) If the bandwidth U is the prime interest, calculate $n=\sqrt{U}$ and find ϱ and θ from table 3, interpolating if necessary.

(b) If the maximum phase error is the prime interest, use this to determine n, ϱ and θ from table 3 interpolating if necessary. (The equations permit extensions of table 3 or precise interpolations to be calculated if required.)

2. Calculate $b=1+\theta^2/2-\theta\sqrt{1+\theta^2/4}$ and $k=\varrho-2$.
3. Find the "centre" frequency $f_0=\sqrt{f_u f_L}$ (if 1(a) applies f_u and f_L will be known. If 1(b) applies f_0 will be known approximately and $f_u=nf_0$, $f_L=f_o/n$ so that a "better" f_0 can be chosen.
4. Find $T_1=1/2\pi f_0\sqrt{b}$.
5. Choose a convenient value for C_1 (for most of the audio range C_1 will probably be selected in the range 1000 to 10,000pF).
6. Find $R_1=T_1/C_1$.
7. Find $R_2=kR_1$.
8. Find $\mu=1+4/k$.
9. Choose R_3 and R_4 (33kΩ and 100kΩ respectively are suggested) depending on gain requirements.
10. Find $R_5=R_3/(\mu-R_3/R_4)$ (=11.593kΩ for suggested values of R_3, R_4 and R_5).
11. Find $C_2=C_1/k$.
    This defines one half of the circuit.
12. Select suitable value for ${}_1C_1$ (The same value as for C_1 is often convenient).
13. Find ${}_1R_1=bT_1/{}_1C_1$.
14. Find ${}_1R_2={}_1R_1k$.
15. ${}_1R_3=R_3$, ${}_1R_4=R_4$, ${}_1R_5=R_5$.
16. Put ${}_1C_2=C_2$.
    This defines the other half.

Finally, it should be pointed out that if higher accuracy components can be employed (as in certain hybrid realisations) then the designer can achieve either better performance over the band or the same performance over a wider band.

The author is indebted to the Plessey Co. plc., for permission to publish this article.

The outphasing method

If a high frequency carrier $\cos\omega_0 t$ is amplitude modulated by a low frequency waveform S(t) the resulting high frequency waveform $s_1(t)=s(t)\cos\omega_0 t$ is a double-sideband (d.s.b.) signal in which essentially the same information s(t), is carried in frequencies above $\omega_o/2\pi$ (the upper sideband) as in those below it (the lower sideband).

Strictly s(t) represents a carrier-suppressed d.s.b. signal. Normally amplitude modulation (a.m.) includes a carrier component also and can be written as $[A+S(t)]\cos\omega_0 t$, where A is a constant usually chosen to exceed the peak negative value of s(t). However, the presence or otherwise of the carrier component is irrelevant to the following discussion). If

$$s(t)=a\cos(\omega_1 t+\phi) \text{ then } S_1(t)=a\cos(\omega_1 t+\phi)\cos\omega_0 t.$$

$$=\underbrace{a\cos\{(\omega_o+\omega_1)t+\phi\}}_{\text{upper sideband}}+\underbrace{a\cos\{(\omega_0-\omega_1)t-\phi\}}_{\text{lower sideband}}$$

Single-sideband (s.s.b.) signals comprise one or other of these two components and can be produced by filtering off the unwanted sideband or by the outphasing method of both.

To generate, say, the upper sideband by the outphasing method we merely note that the required signal is

$$a\cos\{(\omega_o+\omega_1)t+\phi\}$$

$$=a\cos(\omega_1 t+\phi)\cos\omega_o t-a\sin(\omega_1 t+\phi)\sin\omega_0 t$$

It can therefore be produced by combining *two* d.s.b. signals, one of which is obtained as previously by amplitude modulating $\cos\omega_0 t$ by $S(t)=a\cos(\omega_1 t+\phi)$ and the other by modulating a quadrature carrier $\sin\omega_0 t$ by $\hat{s}(t)=a\sin(\omega_1 t+\phi)$. Note that $\hat{s}(t)$ is s(t) shifted in phase by 90° or $\pi/2$. This is the outphasing method.

If we now generalize S(t) from a sine wave

$$S(t)=a\cos(\omega_1 t+\phi) \text{ to } S(t)=\Sigma_r a_r\cos(\omega_r t+\phi_r)$$

which can represent *any* wave-form, the same technique can be used by now $\hat{s}(t)$ is a waveform for which *each* frequency component has the same amplitude as in S(t) but is phase shifted by exactly $\pi/2$. A device which performs this function of converting s(t) into $\hat{s}(t)$ is called a Hilbert transformer.

In practice the filtering method involves very sharp cut-off crystal filters while the outphasing method is difficult to control to give better than 30 to 40 dB suppression of the unwanted sideband. It can, however, be used to ease the cut-off requirements of the filters in a composite system where the filter provides adequate suppression at frequencies remote from the carrier while the outphasing technique greatly improves suppression near to the carrier on the "skirts" of the filter response.

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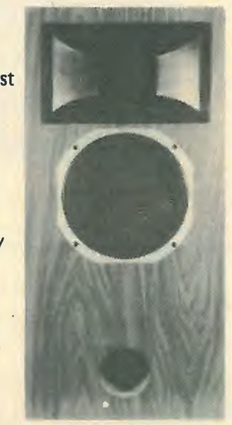

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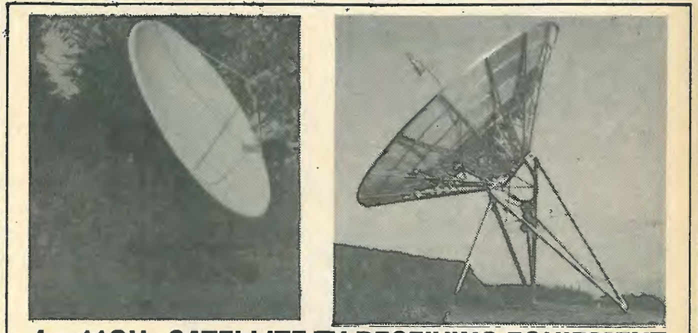

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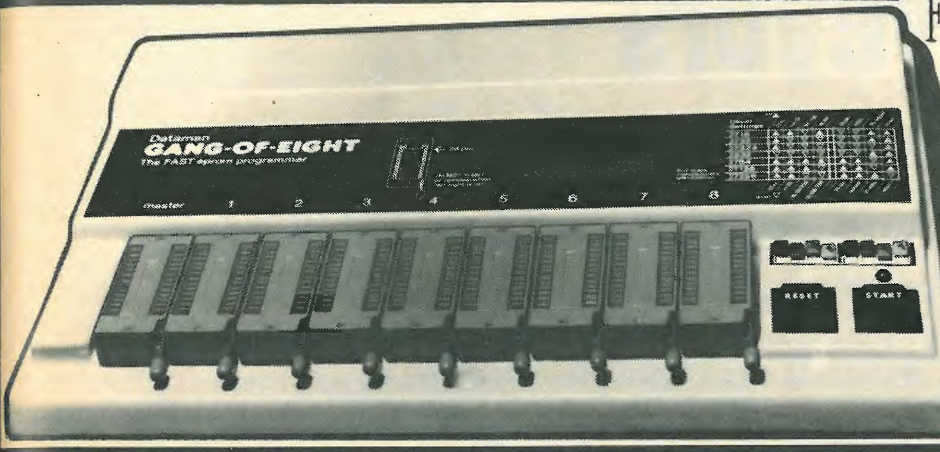

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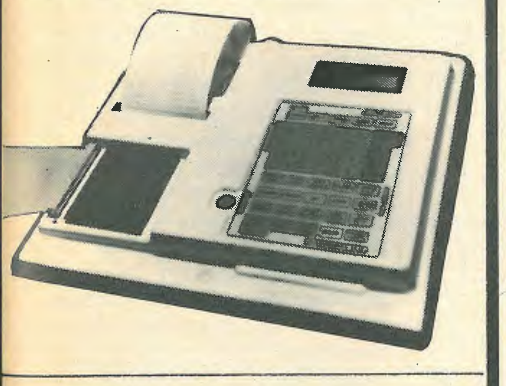

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VISA

by B. Wilson, Ph.D.

Using current conveyors

Produced from current mirrors and op-amps, current conveyors can be used in a wide range of circuits from oscillators to frequency-dependent negative resistors.

Brett Wilson now lectures at UMIST in Manchester after a three-year period teaching at Nottingham University. His two main interests are high-speed analogue electronics and fibre optic communications. He and his research students are currently investigating new designs of fibre optic receivers and the transmission of multiplexed video signals by optical fibres. His hobbies include cycling, swimming, climbing and sailing.

Over the years electronic engineers seem to have been subconsciously persuaded that the world is voltage dominated; that volts are somehow dominant over amps, and in many cases are far more convenient!

While there are good historical and engineering reasons why this feeling has grown up in the power distribution industry for example, there is less convincing evidence in light-current engineering and electronic circuit design. After all both thermionic valves and semiconductors may be best regarded as controlled-current components.

However, we quite happily design and assemble both valves and transistors into voltage amplifiers, or reach for a voltage oriented operational amplifier, usually without stopping to think whether using voltage as the controlled parameter is the most appropriate method for the task.

We are assisted in this by the fact that manufacturers produce a plethora of amplifiers whose aim is to reproduce a controlled voltage output from a voltage input. Circuits which manufacturers offer for controlling current are much less useful — compare the performance of a typical transconductance amplifier to that of a 741.

Are there good engineering reasons for this or can we in fact build current-activated circuits whose performance is comparable to voltage activated ones? After all there are many advantages to be gained in operating at low impedance levels where stray capacitance would produce shorter time constants and therefore fewer high frequency restrictions.

One of the first requirements for current activated circuits is to be able to make a direct copy of a current. This function is nearly always performed by matched transistors configured as current mirrors to produce a current transfer ratio of unity. Previous articles in *Wireless World* have looked in detail at the operation and performance of current mirrors[1,2] so the treatment here will only be in outline.

Figure 1 illustrates the form of the current mirror normally used for precision circuits. Transistors $Tr_{1,2}$ form the basis of the mirror operation with $Tr_{3,4}$ helping to equalize conditions for $Tr_{1,2}$ and buffer the current transfer ratio against output voltage swings.

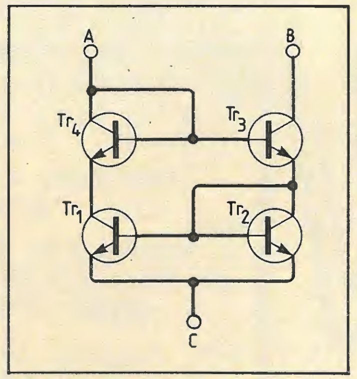


Fig.1. Four transistor current mirror produces transfer ratios accurate to better than 1%.

Using matched transistors in the CA3096AE i.c. package as a four-transistor mirror permits a current transfer ratio of unity to be obtained up to a current of 10mA over a voltage swing of 15V with an error of less than 1% and an output resistance approaching 50MΩ. Main parameters affecting mirror accuracy in a four transistor mirror are transistor current gain and base-emitter voltage mismatch for equal currents.

For p-n-p transistor mirrors overall performance is approximately the same, even though transistor current gain falls more rapidly with current, since it is compensated by the generally tighter tolerance on p-n-p V_{BE} matching. Unfortunately the relatively poor frequency response of p-n-p transistors restricts their usefulness beyond about 1MHz for the CA3096AE array, although there are special techniques available for synthesizing p-n-p mirrors from n-p-n transistors and an operational amplifier[3].

For applications where it is possible to tolerate lower accuracy, three-transistor mirrors ($Tr_{1\text{-}3}$) or even the basic two-transistor mirror ($Tr_{1,2}$) may be acceptable. The symbol used to denote a current mirror is as in Fig. 2, no matter how many transistors are used. The arrow indicates the input side of the mirror, which is held effectively at a fixed voltage.

Amplifier circuits with a controlled output current can be conveniently divided into voltage-controlled current sources (v.c.c.s., or transconductance amplifier) and current-controlled current sources (c.c.c.s. or current amplifiers).

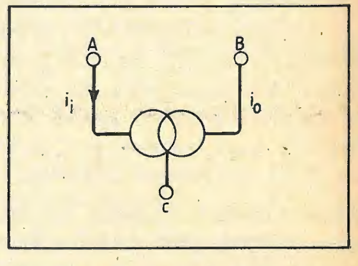


Fig.2. Current mirror circuit symbol.

Many published circuits have shown how operational amplifiers (op-amps) may be used to produce these two functions. Unfortunately nearly all of them suffer from problems of excessively tight resistor matching to balance negative and positive feedback, and any slight deviation from perfect balance results in seriously degraded performance.

The most useful technique is undoubtedly that of op-amp supply current sensing, as in Fig.3, where a copy of the op-amp current is reproduced at the output. Output current is therefore equal to the input voltage divided by R_T, thus producing a transconductance amplifier.

There is also a small component of output current due to the unequal bias currents of the op-amp. This can easily be nulled to around 50nA at the output using a 50kΩ variable resistor connected between the op-amp positive supply terminal and the positive supply.

If manufacturers were to produce a range of op-amps allowing access to the output transistor collectors then current mirrors could be connected at these points instead of the supply terminals, with a resulting lower offset current.

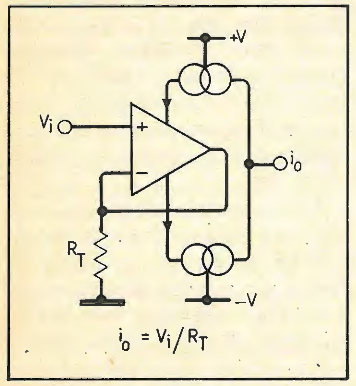


Fig.3. In a transconductance amplifier the output current is proportional to the input voltage.

In contrast to voltage-output circuits, current-output types are intended to operate into low load impedances. Just as an ordinary op-amp produces an increase in distortion at high output currents so will the circuit of Fig.3 produce an increase in distortion for large output voltage swings caused by high values of load resistance.

This distortion can be drastically reduced by operating the current mirrors in a feedback mode and tacking output direct from the op-amp as usual. Mirror outputs are then connected together at the op-amp inverting terminal with transconductance resistance R_T connected to ground. In this case lower distortion is bought at the expense of reduced output resistance.

A true current amplifier can be produced by the configuration shown in Fig. 4. Current fed back to the inverting terminal by the op-amp is reduced by resistors $R_{1,2}$ arranged as a current attenuator. Op-amp current is therefore an amplified version of the input current and this is reproduced at the current mirror outputs to give the gain shown. Circuits shown in Figs. 3 and 4 can both produce bipolar output currents; arrows in Fig.4 are there simply to show phase relationship between input and output currents.

By removing both R_1 and R_2 from Fig.4 and connecting op-amp output directly back to the inverting terminal 100% negative feedback is obtained, resulting in a current gain of unity — a current follower. Using an LM301 op-amp and CA3096AE mixed transistor arrays it is possible to obtain an input impedance of only a few ohms and an output impedance of around 5MΩ at 1kHz. By using the impedance transformation properties of a current follower within a voltage amplifier the usual constraints imposed by the amplifier's gain-bandwith product can be avoided[4].

Current conveyors

Current conveyors are a class of circuits whose operation is characterized by the matrix relationship

$$\begin{pmatrix} i_y \\ v_x \\ i_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \begin{pmatrix} v_y \\ i_x \\ v_z \end{pmatrix}$$

where x and y are input terminals and z is the output terminal. Output current i_z thus depends only on the input current at terminal x. This current may be injected directly at x, or produced by the copy of input voltage v_y from terminal y acting across the impedance connected at x.

In a class two conveyor, represented by the relationship above, input y draws no current, whereas for the older class one formulation the impedance connected at x was also reflected at y.

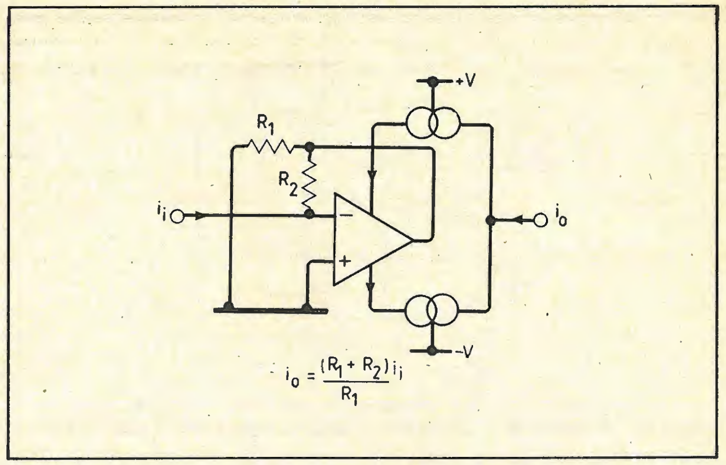


Fig.4. Introducing attenuation into the feedback path produces a current amplifier.

For all conveyors the phase relationship between i_z and i_x is indicated by the algebraic sign in their title, i.e. class II+ or class II−. By convention positive is taken to mean i_x and i_z both flowing simultaneously towards or away from the conveyor. Many different and useful circuit functions can be realised by different interconnections of one or more conveyors as demonstrated later.

A current conveyor may be thought of as similar to a transconductance amplifier, Fig.3, but where the resistance R_T may be replaced by a general impedance or even a separate injected current forming an additional input. This gives a useful clue as to how a current conveyor may be physically realized.

Earlier designs of conveyors suffered from an excessive number of op-amps, tightly matched resistances and very low bandwidths. Operational transconductance amplifiers have also been used, but again with poor bandwidths and output capability even into moderately low loads. Since a current conveyor is intended as a controlled current output it must be capable of driving a short circuit or very low load resistances, in contrast to voltage amplifier behaviour.

The best design of current conveyor produced so far[5] takes the circuit of Fig.3 and allows access to the op-amp inverting terminal as terminal x, as in Fig.5, producing a precision class II+ current conveyor. Input y is a short-circuit stable-voltage input of very high impedance that draws only the op-

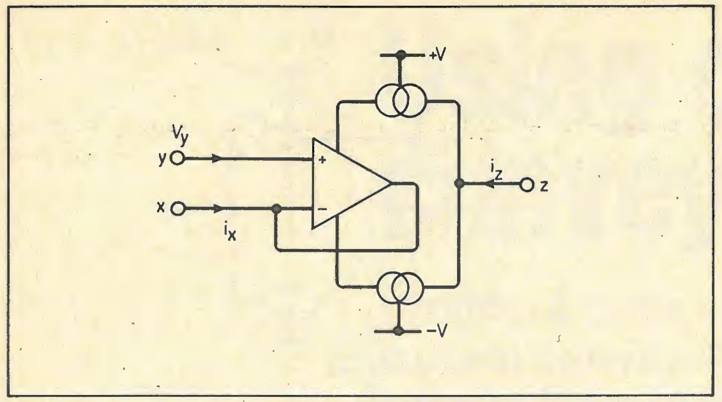


Fig.5. A class II+ current conveyor can be produced from a single op-amp and two current mirrors.

amp bias current and input x reflects the voltage at y and performs as an open-circuit stable current terminal. A class II− conveyor can be produced by simply adding a second pair of mirrors cross-coupled to produce a phase inversion between i_z and i_x, as in Fig.6.

How do they perform? Using the usual CA3096AE mixed transistor arrays and an LM301 op-amp with a compensation capacitor of 39pF results in a small-signal bandwidth greater than 1MHz, again restricted by the p-n-p transistor array performance beyond this region.

Transfer distortions of around −65 to −70dB can be expected, depending on loading conditions (ideally $R_L = 0\Omega$), with an effective capacitance to ground at terminal x of about 4pF. It is worthwhile employing good circuit layout techniques to minimize this value to avoid compromising conveyor performance at high frequencies.

If required current gain can be introduced into the conveyor by including a two-resistor current attenuator in the feedback loop, similar to that of Fig.4. A feedback connection of the current mirrors may also be used if extremely low distortion with unusually high load impedance are main requirements.

There is a little known but elegant circuit arrangement, known as a translinear circuit, due to Gilbert[6] that uses a set of transistors arranged in a ring. One version of this is shown in Fig.7.

Now, the relationship between collector current I_c and base-emitter voltage V_{BE} for a transistor may be written as

$$I_C = I_o \exp(V_{BE}/V_T)$$

where I_o is reverse saturation current of the junction and V_T is "thermal" voltage kT/q.

Assuming matched transistors at the same temperature and operating at normal current levels, the balance of collector currents in Fig.7 may be written as

$$I_1 I_3 = I_2 I_4$$

If I_2 and I_4 are held constant and equal at a value I_B by using current sources and the input current injected at A is I_i we can write simply that $I_i = I_3 - I_1$ for the polarity shown. This property can be used to good effect by adding a pair of current mirrors and a long-tailed pair, as in Fig.8.

Transistors Tr_1 and Tr_2 and current mirror CM_1 function as a voltage follower that accurately transfers input voltage V_y from point y to point x. At balance (V_y and I_x both zero) the translinear cell forces I_1 and I_3 to be equal and hence output current I_z to be zero.

If there is an input current I_x, either injected directly at x or as a result of a copy of V_y appearing at x connected to an impedance, then operation of the translinear circuit will ensure that $I_3 - I_1 = I_x$. Finally, output current I_z, being the difference in mirror currents I_3 and I_1, will be equal to I_x. These are just the properties of a class II+ current conveyor.

Using mixed transistor array CA3096AE to build the translinear conveyor circuit of Fig.8 results in a bandwidth of around 1MHz, again limited by the same shortfall in p-n-p transistor performance.

Accuracy of its performance is similar in other respects to the previous circuits of Figs 5, 6. The main difference is that in the translinear circuit care must be taken in choosing a value for current source I since it sets an upper limit indirectly on the maximum possible output current.

Current conveyor applications

By virtue of their flexibility current conveyors may be used to synthesize a great many circuit functions, some readily apparent, others more obscure. Obviously from their basic operating principles they may easily be used to configure v.c.c., v.c.v., c.c.v. and c.c.c. sources without additional components, except for a single additional resistance in the case of v.c.c. and c.c.v. sources to define the gain.

All the conveyor designs examined so far are suitable for monolithic fabrication, with the bonus of increased accuracy due to better device matching on the same chip.

The useful circuit property of a grounded negative resistance can be produced using only a single grounded resistance and a class II+ conveyor as in Fig.9. Because of the positive phase relationship between the currents at x and z, voltage applied at y will experience a resistance equal to −R. The resistor may of course be replaced by a general impedance Z. A fully floating negative resistance or impedance without any ground reference can by synthesized by the addition of a second conveyor to produce the symmetrical circuit of Fig.10.

An example of filter design using current activated circuits is shown in Fig.11. Making $Z_1 = Z_3 = R$ and using a capacitance for Z_3 produces an all-pass filter with a voltage gain of unity where the frequency at which phase-shift changes from 180° to 0° can be controlled by the value of C. Changing over the capacitive and resistive elements controls the phase shift from 0° to −180° as R is varied.

Conveyors may also be used to design oscillators whose frequency is determined by grounded capacitors with tuning from a single grounded resistive element, Fig.12 — both important considerations in monolithic circuit fabrication.

The circuit may be changed to that of a voltage controlled oscillator (v.c.o) by replacing R_x by the channel resistance of a fet. In addition low-frequency oscillation is possible without the use of large values of capacitance by controlling the term $R_x - R_1$ with nearly equal values of R_x and R_1.

Another interesting area of application for conveyors is that of analogue computation. Here the current output of the conveyor is a great advantage because numerous currents, representing processed information, can be summed together at a single point without the need for an extra summing amplifier as is the case with voltage controlled amplifiers.

The usual functions of integration and differentiation can of course also be performed. Complex driving wave-shapes may be readily synthesized by virtue of the ease with which currents can be summed at a point.

Gyrators and f.d.n.rs

One of the most useful functions of active circuit elements is the ability to synthesize an inductance without a physical coil. While it is possible to produce very low inductance values using monolithic fabrication methods, it is not feasible to produce the range of inductance values required in modern filter design, for example. This is where the general impedance transformation properties of current conveyors become very useful as gyrators.

Operation of the grounded impedance convertor shown in Fig.13 is straightforward. Voltage V at the input of the first conveyor results in voltage $-V\, Z_3/Z_1$ at the input of the second conveyor.

Current feedback from the second conveyor output is therefore $V\, Z_3/Z_1Z_2$, resulting in an effective impedance at the circuit input of Z_1Z_2/Z_3. If Z_1 and Z_2 are made resistive with Z_3 as a capacitance, then impedance presented by the circuit is

$$Z = R_1R_2/\left(\frac{1}{j\omega C_1}\right) = j\omega R_1R_2C_1$$

This is equivalent to an inductance of value $L = R_1R_2C_1$. Using the conveyors previously described to implement this grounded gryator inductances up to 1H can easily be synthesized using a capacitor of 100nF or less.

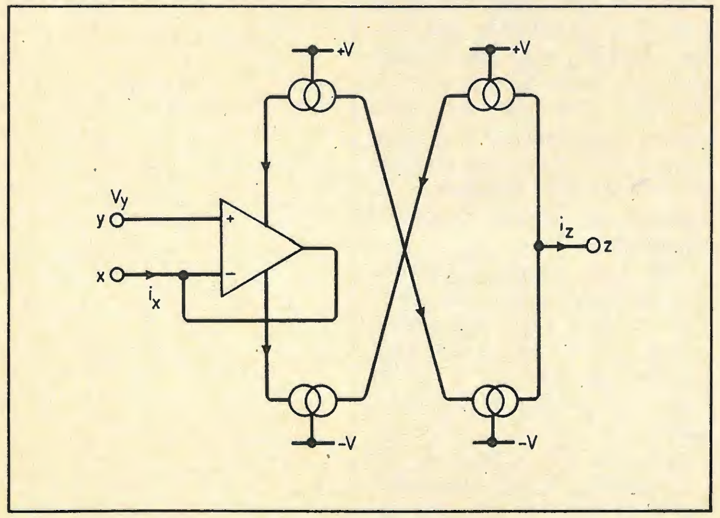
In many cases a floating inductor is required, for example in an active realization of some low-pass filters, and a more complex circuit is required. Several different formulations have been proposed for fully-floating gyrators requiring the use of at least three conveyors, but recently Senani[7] has proposed a design requiring only two, Fig.14.

It can be shown for this circuit that the effective impedance presented between terminals one and two is given by

$$Z = Z_1Z_3Z_5/Z_2Z_4$$

The circuit has wider uses than just as a gyrator. If either Z_2 or Z_4 is made capacitive with all other elements being resistive

Fig.6. The addition of a further two cross-coupled mirrors results in a class II− conveyor.



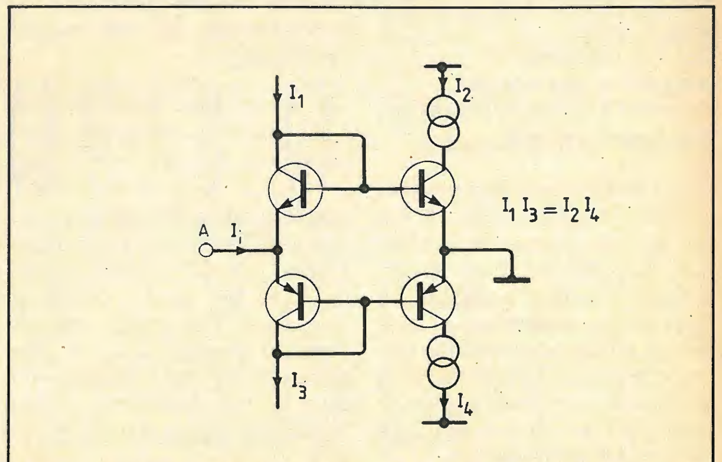


Fig. 7. Current relationships in a translinear circuit.

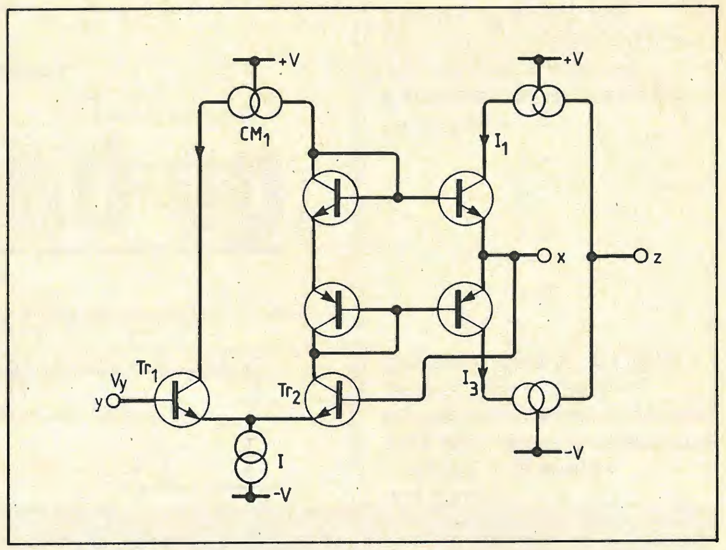


Fig.8. Introducing feedback enables a conveyor to be constructed from a translinear circuit.

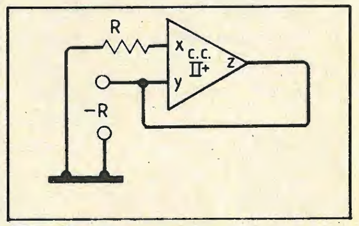


Fig.9. A negative resistance can be synthesized from a class II+ conveyor.

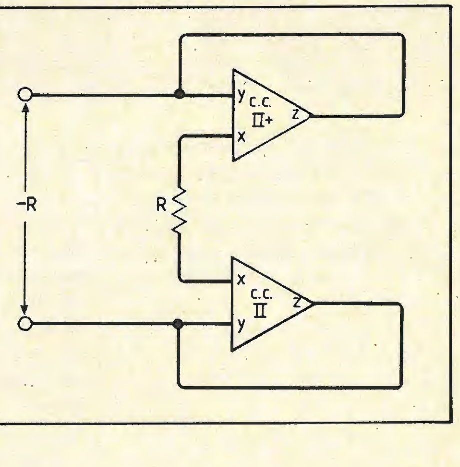


Fig.10. Two conveyors are required to produce a floating negative resistance.

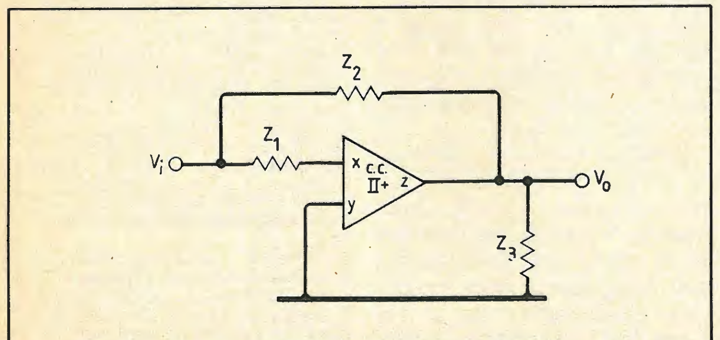


Fig.11. All-pass filter using single conveyor.

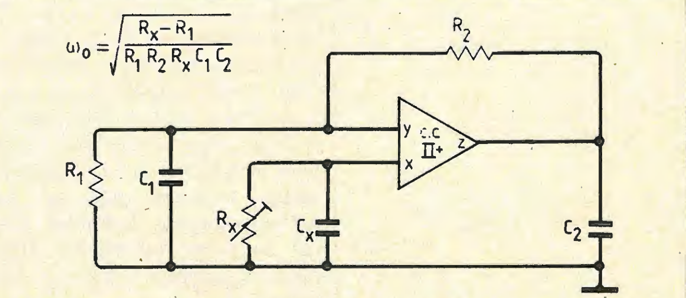


Fig.12. Conveyor RC oscillator can generate very low frequencies.

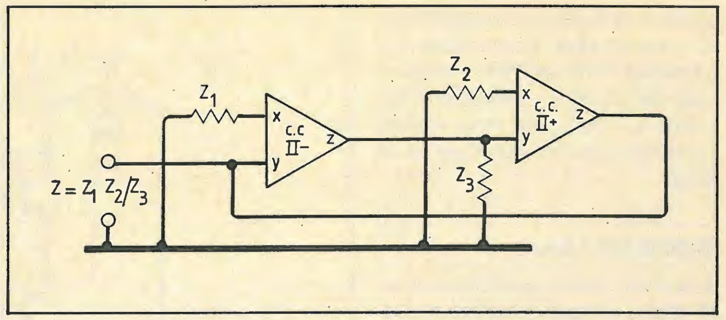


Fig.13. A grounded impedance converter and gyrator requires the addition of an inverting conveyor.

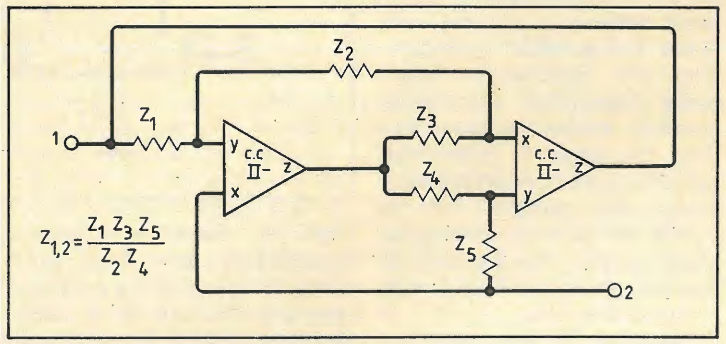


Fig.14. A fully floating frequency dependent negative resistance can be synthesized from only two class II – current conveyors.

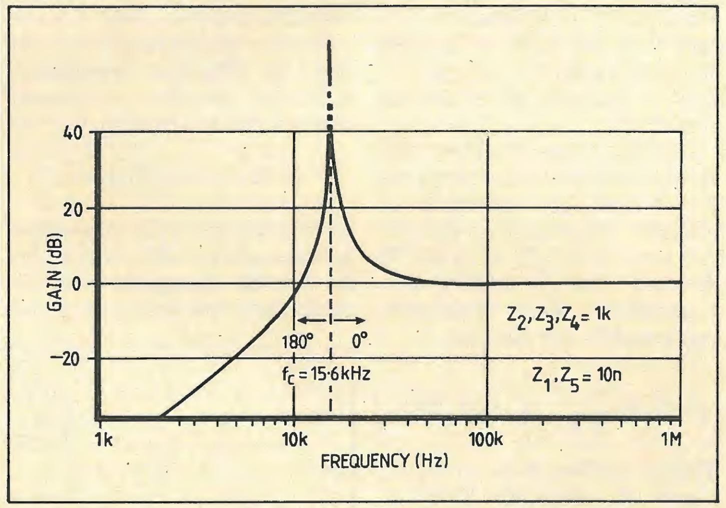


Fig.15. Typical f.d.n.r. frequency response curve showing steep resonance peak and sudden phase change.

then a fully floating inductance can be synthesized. Using moderate values of resistance (1kΩ) and a capacitor of up to 100nF as Z_2 allows an inductor of up to 1H to be synthesized, effective up to the high-frequency limitation of the conveyors at around 1MHz.

Owing to the finite slew rates of all op-amps, it is preferable to use Z_2 as the capacitive element in preference to Z_4 in order to respond correctly to a rapid step change input signal. The inductance simulated is fully floating with no ground reference, however best results are obtained by using terminal one as the actively driven terminal with the load, or subsequent filter elements, connected at terminal two.

One of the more obscure circuit elements that is sometimes required for active filter design is a frequency-dependent negative resistance (f.d.n.r.), or double capacitor. Whereas impedance of a capacitor falls at 20dB per decade, that of an f.d.n.r. is tailored to fall at 40dB per decade and has a negative sign.

A fully floating f.d.n.r. can be synthesized from the same circuit used for the floating gyrator, Fig.14., but this time capacitance elements are used for two of the impedances in the numerator, Z_1, Z_2 or Z_5.

Effective impedance presented between terminals one and two is then $Z = -1/\omega^2c^2R$ if both capacitors and all the resistors are of equal value. To obtain the best performance from the circuit it is advisable to use Z_1 and Z_5 as the capacitive elements and drive it from terminal one with the load at terminal two.

Using a 50Ω signal source connected at terminal one with 1kΩ resistors as Z_2, Z_3, Z_4 and Z_L and 10nF capacitors for Z_1 and Z_5 produces the results shown in Fig.15. At low frequencies the large negative resistance generated by the circuit produces 180° phase inversion between input and output with a very low gain.

As frequency increases, the synthesized negative resistance at some point becomes equal to the sum of the source and load resistance and the circuit exhibits a very high gain.

At resonance this gain is theoretically infinite but in practice is limited by the linear range of circuit operation or power supply voltages, in this example to a value of around 40dB as shown in the diagram. Excellent agreement is obtained between the theoretical resonant frequency and that obtained in practice up to about 500kHz, beyond which the resonance peak tends to reduce as limitations of the circuit frequency response are approached.

Conclusion

Current activated circuits form an alternative approach to the more usual voltage activated ones where lower load impedances and smaller voltage excursions may offer an operating advantage. They can be used to design a wide range of circuit functions from current amplifiers through to gyrators and frequency-dependent negative resistors for active filter design.■

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Cellular radio — a European round-up.

by Nigel Cawthorne, M.I.E.E.

Europe is adopting cellular radio very quickly, but compatibility seems to have been forgotten

The initial flurry of cellular radio activity in the UK is settling down. People are getting used to the sight of those neat little 900MHz cellular antennas mounted on everything from Rolls Royces to delivery vans! The two competing cellular network operators, Cellnet and Vodafone, continue their race to cover more and more of the country. As we celebrate the first birthday of cellular radio in the UK, we can take a quick look round Europe to see the state-of-play of cellular radio with some of our neighbours.

The first and most striking feature of the present generation of European cellular networks is the almost total lack of cross-border compatibility. There are today in Europe just three small pockets of cellular compatibility. The largest and most significant of these pockets is the Scandinavian NMT network, which allows cellular users to travel within Finland, Denmark, Norway and Sweden and to have continuous access to the network.

The second is the Benelux countries. The Netherlands switched on their ATF2 network at the beginning of 1985 and Luxembourg came on-air (albeit in a small way!) in August. In 1986 Belgium will be joining the same NMT 450 network, which will be compatible between the three Benelux countries.

It should be noted that even though countries may be using a common system such as NMT 450, this does not automatically imply that a mobile can roam freely from one country to another. The Benelux NMT 450 system is not operationally compatible with the Scandinavian NMT 450 system. Similarly the NMT 450 systems in Austria and Spain are not compatible with each other. The reasons for the non-compatibility include the use of different frequency allocations, channel spacings and protocols by different PTTs.

The UK and Ireland will also eventually be a small islet of cellular compatibility in a sea of European incompatibility. Both countries are using the TACS 900MHz system. Although the single-cell system in Dublin has been installed since the summer there are still some administrative problems to resolve before the service can com on the air.

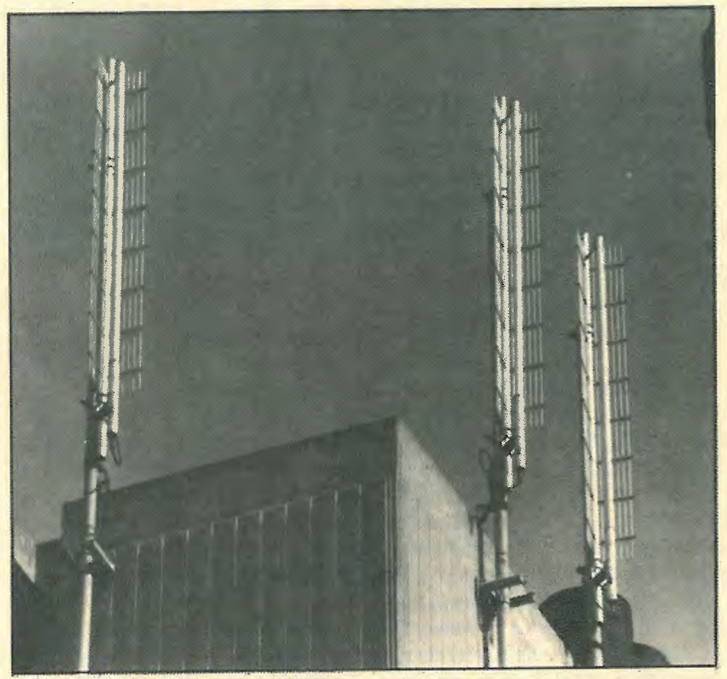
Having shown that there is virtually no cross-border compatibility with the present generation of cellular radio systems in Europe, different country's mobile radio and cellular networks can now be considered.

France

France, in common with several other European countries, has a first-generation automatic car-telephone service operating at around 160MHz. The French system, Téléphone de Voiture, was first introduced in Paris in 1973. At that time France was one of the few countries offering a direct-dial car telephone service in its capital. An old manual system which had first been put into service in 1956 was phased out soon after the automatic system came into service.

Even in its early days in Paris, the Téléphone de Voiture suffered from a shortage of channels. User demand was soon found to be greater than frequency availability. The Téléphone de Voiture system was progressively installed in major cities across France. Today there are ten regional areas with access to the network, but once outside these areas, a mobile cannot access the system. There is no national or even motorway coverage in this network. The capacity of the French 160MHz system totals 10,000 subscribers, 5,000 of whom are in Paris and between 500 and 800 each in Marseilles, Lyons, Rouen, Nice, Lille, Toulouse and Bordeaux. Capacity for a further 200 users is available in the European Parliamentary city of Strasbourg.

The frequencies available at 160MHz alone could not cope with the demands of the senior executive business market in France. U.h.f. (450MHz) extensions to the Téléphone de Voiture network began to be opened in 1983. By the end of 1984, the 450MHz facilities



As cellular coverage spreads across the UK, base site antennas are becoming a common site! Coverage of the Austrian cellular network.

could handle an additional 3,500 subscribers in the Paris area. During 1985, the French PTT have been installing 450MHz facilities in Lyons, Marseilles and Nice, which will provide room for another 150 users in each system.

Waiting lists for the now saturated car-telephone service in France are long. Despite the additional frequencies, the Téléphone de Voiture service could not be expected to cope with future demand and the lack of national coverage is a major drawback.

Aware of the severe capacity problems inherent in the Téléphone de Voiture networks, the PTT contracted with the French electronics company Matra in 1981 for a study project to find a nationwide solution. The new network, Radiocom 2000, resulting from the study started to come on-air in late 1985, providing two distinct types of service: it has facilities for both direct-dial car telephones operating on duplex as well as for private business networks (p.m.r.) operating on simplex.

Matra, the designers and constructors of the Radiocom 2000 system intend to satisfy these two different mobile radio markets with just one infrastructure. Radiocom 2000 provides both a carphone and a p.m.r. service (Réseau d'Entreprise) within the same switching and radio repeater network.

The French PTT have already ordered 200 Radiocom 2000 repeaters from Matra: a total of 500 repeaters are planned to give 80% population coverage by 1990. Although Radiocom 2000 is described as a 'cellular' system, it differs in several important ways from the cellular networks operating elsewhere. Radiocom 2000 uses a large 'cell' areas without any hand-off. Once a communication is established within the area of one repeater, the conversation cannot be automatically transferred to another repeater, as is the case in the UK and elsewhere. If communication is lost due to driving out the range, then the call has to be re-established by pressing a recall button.

The French PTT provide a number of options for subscribers. Subscribers on both the carphone (duplex, p.s.t.n. access) and p.m.r. (simplex, no or very limited p.s.t.n. access) can pay to have access to just a single repeater for local use. For regional coverage subscribers can pay a larger monthly subscription to access a number of repeaters in one area. If national coverage is required the subscriber can pay a still larger subscription which allows him to access all the repeaters in the national network.

Matra is responsible for the Radiocom 2000 infrastructure, but it is the French PTT that are selling the service to the public. Although in the early months of the Radiocom 2000 service, Matra will be the sole supplier of mobile sets, several other manufacturers are getting ready to take a share of this new mobile radio market in France.

Every Radiocom 2000 mobile is assigned a 'home' repeater. If a mobile is located away from his home repeater, the receiver will automatically scan to find the nearest repeater. A signalling exchange takes place between the mobile and the 'away' repeater, which in turn refers back to the mobile's home repeater for the purpose of veryifying authorised use of the away repeater. The p.s.t.n. is used for signalling between repeaters.

Another major difference between Radiocom 2000 in the UK cellular network is in the use of telephone exchanges. Each Radiocom 2000 repeater directly accesses a local telephone exchange. In this way the p.s.t.n. carries all repeater traffic and signalling. Since each repeater is tied to a local telephone exchange and each subscriber has his own 'home' repeater', the carphone numbers issued to the subscriber are ordinary local-exchange numbers and not one of a special series of numbers, as in most other countries.

The greatest operational difference between France's Radiocom 2000 and the UK systems lies in the mix of services provided. Radiocom 2000 provides both a carphone service with full duplex p.s.t.n. access for the public user and it also provides a private business radio network for fleets of vehicles. Both types of service operate through the same repeaters. This contrasts with the UK where p.s.t.n. access is currently restricted to the 900MHz cellular services and the Radiophone 4 services at 160MHz.

As well as the main Radiocom 2000 project, Matra also implemented the Radiocom service which opened in Paris in 1982. This pilot network was designed to provide urgently needed extra capacity in the Paris area. There are currently 11 Radiocom 200 8-channel repeaters in the Paris area and single repeaters in Lyons and Marseilles. The Radiocom 200 (analogue signalling) network operates on 200MHz Band III frequencies only and will eventually be phased out as a new Radiocom 2000 (digital signalling) network gets under way.

The national network on the Radiocom 2000 system is at u.h.f. (420MHz), but there are regional networks in the major cities on frequencies around 200MHz in Band III.

France, in common with several European countries, will be continuing tv transmissions in Band III for the forseeable future. Many of the 625-line colour transmissions of France's new fourth channel (Canal Plus) use Band III. The main city transmitters of France's new off-air Pay-TV service are on v.h.f. Band III, whereas Canal Plus repeaters are on u.h.f. In Paris Canal Pus uses Channel 06 (183-191MHz). The 200MHz channels used by Radiocoms 200 and 2000 are between 192MHz and 207MHz. Radiocom 2000 thus has to share band III frequencies with tv transmitters in other parts of France.

At just 120km from the centre of Paris there is a 10kW Canal Plus transmitter on Channel 07 (Vision carrier 192MHz) with an e.r.p. of several tens of kilowatts. The same frequencies will be used in Paris area for Radiocom 2000 mobiles. To minimize the risk of interference between the two different services (tv and mobile radio), guard bands have been established 500kHz on either side of the vision carriers and 125kHz on either side of the tv sound carriers.

European Cellular Radio Systems

On air	Country	System	Subcribers (Oct. 1985)	
1982	Denmark	NMT 450	39,000	
1982	Finland	NMT 450	29,000	Scandinavian NMT : 18i3,000
1982	Norway	NMT 450	49,000	
1982	Sweden	NMT 450	66,000	
1982	Spain	NMT 450	650	
Nov. 1984	Austria	NMT 450	7,500	
Jan. 1985	UK : Cellnet	TACS 900	18,000	UK total : 30,000
Jan. 1985	UK : Vodafone	TACS 900	12,000	
Jan. 1985	Netherlands	NMT 450	4,000	Benelux network
Aug. 1985	Luxembourg	NMT 450	20	
Sept. 1985	Germany	C 450	———	Operational tests commenced 9/85
Nov. 1985	France	Radiocom 2000	———	Quasi-cellular combined p.m.r. and carphone

Country	System	Target	Notes
Eire	TACS 900	late 1985	Single cell in Dublin ready 1985
Belgium	NMT 450	mid 1986	Compatible with Netherlands/Luxembourg
Switzerland	NMT 900	late 1986	Pilot system initially in Zurich

Notes:
1. Scandinavia, UK/Eire and Benelux are the three independent 'islands' of European cellular compatibility.
2. Although the systems in Scandinavia, Austria and Benelux are all NMT 450, they are not operationally not compatible.

The total capacity of Radiocom 2000 is projected as being about 300,000 mobiles. The v.h.f. repeaters were opened in the Paris area just before the end of 1985 and the first u.h.f. repeaters on the national network are scheduled to be operational in early 1986.

Spain

Spain has been keeping a low profile in cellular radio. Spain's NMT 450MHz cellular network which came into service in 1982 was one of the first on-air cellular systems in Europe. But despite being one of the first in the field, the network has been slow to develop.

The present system covers Madrid and Barcelona only and has around 600 subscribers. Additional systems are being aded to Cadiz, Seville and Malaga in late 1985. The new Andalucian network will be brought into service in early 1986.

Telefónica, who runs the Spanish cellular networks, is expecting a significant increase in the number of subscribers in the next few years, both because the network is being expanded and because mobile sets will soon be becoming available from a number of different sources. Currently cellular radio mobile sets in Spain are only available through Telefónica.

The numbers of cells in service including the new Southern Spanish network are: Madrid (3), Barcelona (2), Segovia (1), Toledo (1), Cadiz (2), Seville (1) and Malaga (3). There are three separate networks: Madrid/Toledo/Segovia with 57 channels, Barcelona with 12 channels and the Andalucian network with 35 channels.

Telefónica have plans to add further new cellular areas, but even with current plans, coverage by 1988 is not expected to exceed 50% of the population nor 15% of the land area of Spain. The present cellular networks in Spain cover less than 20% of the population.

Austria

Austria came on-air with its new cellular carphone network in November 1984. Called 'Autotelefonnetz C', the present network has capacity for 30,000 subscribers.

There are two mobile switching exchanges, one in Vienna and the other in Salzburg, each capable of handling 15,000 subscribers. The Austrian PTT already have plans to incorporate a third switch in Graz as an when demand requires.

The NMT 450MHz infrastructure was supplied by Motorola and mobile equipment is available from several suppliers. The PTT themselves are supplying a Siemens set made under licence in Austria by Kapsch. Ericsson, Mobira, Motorola, Storno and Philips are all present in the Austrian carphone market.

Present day demand for car telephone services in Austria greatly exceeds the capacity of the previous Netz B system, which has been in operation since 1972. With capacity for only 1,800 subscribers, the 150MHz Netz B network has been overloaded for several years.

In making a choice of system for the new cellular network, Austria faced a dilemma. The existing Netz B was compatible with networks in Germany and the Netherlands. An Austrian Netz B subscriber could use his car telephone while travelling in the other two countries. There were cross billing arrangements between the PTTs.

In selecting a cellular system, the Austrian PTT had to decide whether it was better to wait for the German C450 network to be fully developed, or to go it alone and opt for some more readily available system but one that would not be compatible with the new German cellular network.

The final choice of a Motorola NMT 450 system was made on two factors. Firstly, the price offered by Motorola was less than Siemen's bid for an uproven C450 system. Secondly, The Austrian PTT were eager to provide a cellular service as quickly as possible.

The Austrian decision to go it alone meant that an expanded carphone service was provided earlier than otherwise, but it was yet another nail in the coffin of 'European cellular cross-border compatibility'. The Austrian NMT 450 network is incompatible with systems in use in both of Austria's German speaking neighbours, Germany and Switzerland.

The Austrian PTT have allocated 222 duplex channels in the ranges 451.3 to 455.7MHz and 461.3 to 465.7MHz for the network. Frequency re-use will allow up to 1,200 active channels across Austria. A characteristic of the Austrian version of NMT is the use of 20kHz channels spacing as opposed to 25kHz.

For the Austrian subscriber, the new 'C' network is cheaper in both equipment purchase and in operating costs in the previous 'B' network. A mobile unit for the 'C' network costs around 40,000 OeS (£1,600) whereas an equivalent 'B' network set was 100,000 OeS (£4,000). The monthly connection charge is 400 OeS (£16) on the new service as compared to 1,800 OeS (£72) on the old 'B' system.

The Austrian PTT leases 'C' network mobiles around 830 OeS (£33) per month and daytime calls cost just under 7 OeS (28p) a minute. International calls are charged at the same rate as from an ordinary telephone with an additional radio channel usage charge of 1.40 OeS (6p) per minute.

The radio infrastructure required to achieve adequate coverage of the main towns and motorways all across Austria is complex. With its high mountains and deep valleys, Austria presents difficult challenges to the radio network planner. The Austrian PTT continues to extend Autotelefonnetz C coverage along all major trunk roads and into mountainous areas.

The Austrian PTT are budgetting annual investments in infrastructure of 100m OeS (£4m) over the next few years. This is in addition to the 260m OeS (£10.4m) that had been invested up to the opening of the new cellular radio service at the end of 1984.

Germany

The Deutsches Bundespost DPB commenced operational trials of the newly installed C-450 cellular system in September 1985 with 100 base stations. Full national coverage, including West Berlin, with 175 base stations is expected to be completed over the next few months in time for the public opening in May 1986.

It is Germany and France that have taken the cause of cross-border compatibility in cellular radio the furthest, but their original plans for a common analogue cellular system failed. Both countries are now working on proposals for a future pan-European digital network.

The Franco-German consortium of SEL/AEG/Thomson/SAT have recently revealed details of their CD-900 digital system which they hope will form the basis of Europe's next generation of cellular radio.

The proposed system represents a radical change from today's standards. Four important features which differentiate CD-900 from present day analogue techniques are:

- the use of time division multiple access (f.d.m.a.) instead of frequency division multiple access (f.d.m.a.) i.e. 'time channels'
- use of only one radio frequency channel for all subscribers on one cell base station.
- wideband transmission (4MHz channels instead of today's 25/12.5kHz spacing on analogue systems).
- use of multi-path to good advantage

Using the CD-900 techniques proposed, power requirements and equipment sizes will be dramatically reduced. The Franco-German consortium believes that the digital techniques proposed for the next generation of cellular radio will make consumer sets five times cheaper than at present. Base-station costs would decrease to about one third of those of conventional systems. As well as dramatically reducing cost, digital cellular radio would provide a degree of protection against eavesdropping not economically obtainable with analogue cellular systems.

Switzerland

The Swiss PTT decided early in 1985 to implement an NMT 900MHz cellular network with a potential capacity for 12,000 subscribers. A pilot scheme with 20 transmitters is scheduled to be installed in the

Zurich area in late 1986. In the meantime Swiss carphone users will continue to use the existing (NATEL A and B) 150MHz systems.

The Swiss national mobile NATEL radiotelephone systems was developed by R&D department of the Swiss PTT in the early 70's. However, due to economic reasons, installation work did not commence until 1976 and the NATEL 'A' network was finally put into operation in 1978 while NATEL 'B' came on the air in 1983.

As well as the two national NATEL networks there is also a smaller local mobile network in the Zurich area. In mid 1985, the 'A' and 'B' NATEL networks had 4,200 and 3,000 subscribers respectively and the Zurich regional network had 500 subscribers.

Holland and Benelux

The Dutch ATF2 cellular network came on the air on 29 January 1985 with 50 base stations giving national coverage. The 20km cells used in the first phase will be augmented in a second phase by 5km wide small cells. The capacity of the present system is between 15,000 and 20,000 subscribers, but it is expected to increase to some 60,000 when the small cell installation is complete. The total number of cells will be in the region of 200.

The Dutch PTT is using a single Ericsson AXE10 switch. As part of the Benelux expansion, Luxembourg was connected into the system in mid-1985. Belgium is expected to have its own switch in operation in 1986. The three Benelux countries will be one of the three small islands of cellular compatibility in Europe.

Compatibility

It is only with the second generation of cellular systems that a pan-European cellular system has a chance of becoming a reality. In the meantime, Europe has a patch-work of incompatible systems. The pan-European cellular dream of being able to drive from the North Cape in Norway down to Gibraltar while running up a phone bill all the way may one day come true! ■

Land Mobile Radio

Nigel Cawthorne reports on the IERE's third international Land Mobile Radio conference.

The three-day Land Mobile Radio conference, held by the IERE in Cambridge, was attended by over 250 delegates. Topics covered by the papers included paging, trunking, cellular radio, cordless telephones, digital and wideband techniques.

Band III protocol

A paper from the DTI explained how the new MPT 1327 signalling protocol standard for Band III trunked systems had been derived from the earlier MPT 1317. Ron Tridgell told delegates that the new f.f.s.k. signalling, 1200 bit/s standard "had been designed for the mobile industry by the mobile industry". Eleven manufacturers, two user associations, the DTI and BT had all contributed to the drafting of the new trunking signalling standard.

The signalling standard can handle up to one million subscribers in any one sub-band (the Band III spectrum for p.m.r. is split into three sub-bands), up to 32,000 systems, (where the likely size of system would be of the order of 20 channels) and up to 1,000 channel numbers. The actual specification document is now some 60 pages thick.

Peter Mabey of Pye described in detail the control channel signalling of the UK trunking system signalling standard MPT 1327, giving examples of the call set-up procedures.

Cellular data

Cellular radiotelephone networks will be used to carry data as well as voice traffic. Racal described the results of simulation and field trial tests using their cellular radio data transmission standard (CDLC).

Stig Kaspersen of the Norwegian PTT (NTA) outlined the experimental mobile data network in operation in the Oslo area. With over 60,000 NMT450 cellular telephone users in Norway after only four years of operation, the NTA sees a real demand for mobile data services. Norway has the highest per-capita cellular population in the world.

The NTA mobile data network uses radio channels close to, but separate from, the NMT450 channels. Both systems (cellular car-phone and mobile data) can use the same radio equipment in the vehicle. By 1988, the NTA plan to have national coverage with their mobile data network.

Digital cellular

Tony Potter, BTRL, discussed the principal issues under consideration in the current debate over standards for the next generation of cellular radiotelephones.

One estimate of the number of mobile communications users in Europe in the year 2000 is 20 million and at least 5 million of these could be using cellular mobiles, with the exact number depending critically on equipment prices.

Second-generation cellular has to cost no more than the mature first-generation systems, which will be in service in the early 1990s.

Adequate system capacity is vital for second-generation cellular. It will have to appeal to a much larger audience than the current generation. Potter explained that the TACS system, as operated by Cellnet, has a capacity of 3.3 channels/cell/MHz. This is based on the 12-cell repeat pattern, with 25kHz channel spacing. Potter argued that if the market for the next generation of cellular systems is not to be constrained by capacity, then there will have to be at least five times the capacity that is available on current cellular systems.

Co-existence

A primary CEPT requirement is that the pan-European system shall be able to co-exist with earlier, first-generation systems in the 900MHz band. With increased pressure from UK users for access to the pan-European reserve frequencies, there may eventually be no room at 900MHz even to start the second generation, let alone create a system having a capacity an order of magnitude greater than today's systems.

Although not aired in any of the formal papers, some delegates questioned privately whether, with the pressure for more frequencies at 900MHz, and with the capacity demands of a second-generation system, the whole idea of a pan-European system at 90MHz is not a deadduck from the start. An alternative might be to start gain spectrally with a clean sheet at 1.5GHz, where there would not be a problem of sharing with existing cellular systems and where there may be sufficient spectrum available to allow the next generation of cellular radio to develop into true 'personal communications'.

Cordless PABX

Dr Mike Carey of Mitel described how spread-spectrum techniques, operating at u.h.f. tv frequencies, could be used for an on-site mobile business communications system. The proposed system incorporates all the features of a voice and data PABX, but would also have the added advantage of handheld mobile telephone sets. Leaky cables would be used within the building.

Dr Carey proposed that the spread-spectrum wireless PABXs operate in those parts of the u.h.f. tv bands which are not used (in a given location) for their primary purpose.

Following computer simulation studies, Mitel claim that u.h.f. tv frequencies could be used without significant interference problems in either direction (i.e to the PABX user from distant u.h.f. tv transmitters or to the tv viewer from numerous distant spread-spectrum wireless PABXs).

FEEDBACK

BBC ENGINEERING

The BBC Designs Dept. is truly working for cost effectiveness (WW, December 1985) if they have managed to put themselves out of business. Had they worked on tv stereo, high-definition tv and all the other goodies people really want — and it is not too late yet — they would still be in business.

As for the a.m. dynamic carrier controller, this is the acme of folly. We overseas listeners only manage to pick out the BBC from all the hash because of the present 16dB compression and could wish for more. To weaken the carrier is suicide; rather cut the highest audio frequencies and give a little boost in the 2000Hz area for that brilliant effect most a.m. broadcast music requires. We purists will use f.m. for music in any case.

Peter Hirschmann
Romema, Haifa
Israel

AN ANSWER ABOUT 'Q'

I now have an answer to my question (Feedback, December, 1985). Estill I. Green in the *American Scientist* (1955) Vol. 43, 585-594, attributes its first use to K. S. Johnson in unpublished material in 1920 and in a book, Transmission Circuits for Telephonic Communication, Van Nostrand, 1925, Western Electric 1924.

He used it for the ratio of reactance to resistance because "The other letters of the alphabet had already been pre-empted for other purposes". "Quality factor" came later. What Green calls a "contagious symbol" has moved into a number of fields.

Bertha Jeffreys
Cambridge

PREAMPLIFIER DESIGN

I would like to comment on John Curl's interpretation of his measurements on electrolytic capacitors, reported in your November issue.

The 'residual', he says, is 'not level-dependent', which I take to mean that its amplitude is proportional to the input amplitude. In that case there is no evidence of non-linear distortion. The fact that there is a residual at all shows that the electrolytic capacitor cannot be represented by capacitance and resistance in series. It does not follow that it cannot be represented by a more complicated, but still linear, circuit. This would alter the frequency response, but whether the change would be audible, and indeed, whether it would be an improvement or an impairment, it is impossible to decide on the evidence presented.

Kenneth S. Hall
Bromley
Kent

LIGHT, DISTANCE AND TIME

In an earlier letter (September 1985) I introduced the idea that if full e.m. Doppler is allowed into the description of experiments that are *supposed* to support the Special Theory of Relativity, then it is found that those same experiments, now with a complete physical description, did in fact constitute an experimental disproof of the conclusions of the theory. I also put forth the idea that the paradoxes of STR had as their foundation a misconception concerning the scale of whole numbers *when applied to nature*. There have been but two replies.

I would thank E. Baird (November 1985) for his congratulations but, even by reading 'between the lines', I am still not sure whether those congratulations constitute as acknowledgement of the fact that STR is disproven by the Michelson-Morley experiment. Perhaps he would be so kind as to enlighten us?

The other, private, letter came from Alan Watson and he at least did touch upon some of the matters in hand. Since these things are of importance I am sure that he will not mind if I make my reply, at least in part, in public.

In response to the actual question Alan Watson states, with regard to the difference in arrival time of the rays of light, "I would prefer to use some sort of stop watch"; then somewhat later he says "In the case of M-M, any change would be detectable in the time taken for the light to travel along one arm when compared with the time taken along the other because such a difference would result in an alteration of the phase relationship between the two beams when they are compared in the interferometer". This statement is a summary of the accepted teaching on the subject *and it is wrong* for the following reason.

It is central to the teaching of electromagnetism that for all observers the product of frequency and wavelength shall be the constant c. A further aspect of the teaching, involving relative motion of source and observer, has it that whether light be blue or red shifted there is an additional Lorentz related red shift *in each case.* These last two elements of the teaching together with the null result of the M-M experiment are natural facts which may be used to test the validity of any theory concerning light; they were facts of nature, albeit unknown, long before Maxwell or Einstein. This being so, they represent axioms which are external to STR and as such may be used to test that theory for contradiction in accordance with Gödel's theorem.

It is beyond question, because it is an experimental observation, that the frequency of the light seen in both axes by the observer moving with the M-M experiment is the same, whatever the speed of the experiment. Because c is a constant in both axes the wavelength of the light will also be the same in each case and within classical concepts no phase alteration is to be expected at the interferometer when the experiment is rotated.

In the case of the stationary observer, he sees the additional Lorentz red shift in both directions in the longitudinal axis. Because of the constancy of c (product of frequency and wavelength) the wavelength of the light is increased by the Lorentz factor along the line of the motion. It is the light path that increases by the Lorentz factor and not the length of the experiment that diminishes.

There is one further thing to be considered. A neutral particle may be accelerated by a beam of light and when the particle is at rest relative to the light source then the pressure that it experiences is in direct proportion to the energy of the photons in the beam. When the particle is in motion away from the source the particle sees a Doppler reduced frequency which includes the additional Lorentz red shift. Since the radiation pressure felt by the particle is in direct proportion to the frequency that it "sees" then it becomes clear that it not the mass of the particle that increases with velocity but in fact the propulsive effect of the source which diminishes due to Doppler.

If we ignore terms of the second order we find that there is, in this particular case, a physical reason for the Newtonian energy equation since from rest:—

$$\frac{\text{E (at source)}}{\frac{1}{2}\text{V}} = \text{m.v}$$

Within present knowledge of e.m. Doppler, E is of course modified in its effect by the Lorentz factor and mass *is* velocity invariant.

I invite Prof. R. C. Jennison to tell us whether my descriptions are right or wrong; if wrong would he please explain why?

Alex Jones
Swanage
Dorset

NEW LOGIC SYMBOLS

Letters published to date do not reflect much enthusiasm for the 'new symbols'. I suspect that more problems will result from their introduction than there will be benefits gained. It does seem that all the implications of introducing this new 'standard', have not been sufficiently thought out. I wonder just what degree of involvement the British Standards Institute had.

There are three serious problem areas which should be considered by any persons involved with the documentation of electronics.

Firstly, no mention has been made of the cost of introducing the new symbols or of supporting their use thereafter. Engineers and managers should take a critical look at the financial implications for their product documentation and technical publications: I predict that the final cost to the nation will be enormous. The descriptive literature I have seen is extremely heavy going and frequently ambiguous and generally inadequate.

Secondly, there will be a dramatic increase in documentation errors, due to the over complexity of the new symbols. It has always been difficult to get engineers to sufficiently check their engineering documentation; the new standards will only make matters worse. Our electronics education system seems unable (or does not even try), to convey to engineering students, the importance of accurate documentation and the significance of initials in the CHECKED box on drawings. Many engineers seem to regard documentation as an unnecessary chore, an attitude which is aggravated by managements who consider documentation and technical publications as an expensive overhead, to be written off as cheaply as possible.

Finally, one must consider the trend for illustrations in technical manuals to be reduced in size, often to the point of unreadability (again to save on publication costs). Generators of documentation will have to be aware that essential detail in the new symbols will easily be lost, through size reduction, or by degraded definition through photocopying.

The traditional shaped symbols for basic gates immediately convey their function. The new symbols depend entirely on tiny characters to indicate the function: if these become illegible the entire symbol becomes undefined.

Boolean functions have for decades been ambiguously depicted by: + = OR, full stop = AND. So why in the space age are we burdened with new, equally ambiguous cyphers? V = OR, G and & = AND. Perhaps V and G make sense in French or some other language. This problem area has been covered in Ken Wood's letter to *E&WW*.

Perhaps the changeover period will be so prolonged (>10 years) that technological progress may have become able to eliminate any need for logic symbols. A decade ago, American CAD/E systems were creating t.t.l. logic circuit functions on the basis of only input and output parameters. The associated 'design' engineers were unable to offer explanation of circuit functions, because the CAD/E had done all the designing, but the machine was unable to generate corresponding circuit descriptions!

Maybe one day, CAD/E systems will solve all these and other problems, by producing lots of indescribable black boxes.

Denzil S. Roden
Lancing
West Sussex

MATHS PUSHERS

From a dictionary of the English language I find: MATHEMATICS (n) a group of related sciences, concerned with the study of number, quantity, shape and space . . . (from Greek: *mathema,* a science related to; *mantanein*, to learn). SCIENCE (n) a systematic study of the nature and behaviour of the material and physical universe . . . (from Latin: *scientia*, knowledge . . .).

So mathematics is grouped as a science since it forms a body of knowledge. Originally though, and to me still, it was most closely related to the learning of how nature works.

Contemporary mathematicians/scientists tell us that we *create* mathematics (James Jeans' words) and then apply it to the codification of our experiences of nature. We can do this, of course, since we are apart from, and indeed above, nature. This is arrogance in the extreme.

History shows us that once every few centuries someone is fortunate enough to find themselves in a frame of mind that allows them to gaze inwards at the nature that is themselves, and there learn a little more about nature herself. This, to me, is mathematics.

A. Medes
Dee Why
Australia

SHAFT ENCODERS

After reading A. J. Crofts shaft encoder interface scheme in WW CI Nov 85, I was perturbed to see yet another shaft encoder idea that will not work properly, appearing in your pages. Even more distressing is the fact that I apparently wrote this one. In fact this is not my letter pointing out the problems, but another exhibiting in full, exactly the same problems.

The circuits described in *EWW* for November 1985 (p.74) and February 1986 (p.36) will both give a continuously increasing count for a small mechanical oscillation of the shaft. An ideal shaft encoder interface must cause the counter to oscillate between two output counts, since this is a true reflection of the shaft position.

The February version, mistakenly attributed to me *(see note, March issue, p.53 — Ed.),* claims to get round this problem, but in fact does not. This can be seen by considering the effect of a reversal occurring 90 degrees later than the one shown in the diagram. In this case, the result is two counts in the same direction, instead of two opposing counts.

Not only may there be false counts with these interfaces on each change of direction, but this may also result from noise or mechanical inaccuracy inside the shaft encoder during continuous motion. It is not just a case of waiting for data to settle; the A and B signal outputs from the shaft encoder are derived by schmitt triggers from nominally triangular analogue signals from photo-cells. At the transition points, these are susceptible to noise, which may cause multiple transitions. In a correctly designed shaft encoder interface (see *WW* Circuit Ideas, May 1985 or *New Electronics* January 1982, p.27), this will result in a temporary indeterminacy of one count, but in the November and February *WW* CI, it results in a permanent and cumulative error.

Mark Winder
Reading University

WHATEVER HAPPENED TO THE SONIC PATHFINDER?

The Sonic Pathfinder, a spectacle-frame-mounted ultra-sonic guidance aid for the blind was the winning entry in the *Electronics and Wireless World Design Competition* in 1984.

Despite the considerable interest aroused by the competition, a manufacturer for the device was not forthcoming. Yet another setback was that, although the DHSS has continued to fund the Blind Mobility Research Unit at Nottingham University, no funds could be made available from current budgets for the purchase of devices for the field trials. The proposed field trials involve placing thirty devices with blind clients for a period of six months and monitoring the consequent impact on lifestyles.

The good news is that things are, at last, under way. Largely due to the efforts of the veteran blind traveller Walter Thornton, a new charity, MOBEL, has been created, the aim of which is to give financial help so that individual blind people may benefit from electonic mobility aids. MOBEL's first aim, that of raising the money to finance the field trials, has been accomplished due to a generous grant from St Dunstan's, the well known charity for the war blinded. The National Mobility Centre in Birmingham has agreed to take responsibility for training and my colleagues at the Blind Mobility Research Unit for the collection of field trial data.

At last we have a manufacturer: Portshel, the sheltered workshop at the Portland Training College for the Disabled in Mansfield. Portshel have established a good reputation for industrial assembly subcontract work. They also have a growing number of their own electronic products, several of which relate to the disabled.

Perhaps the most exciting development happened at the end of last year when, at the invitation of the Royal Guide Dogs for the Blind Associations of Australia, I took four Sonic Pathfinders out to Melbourne and set up a training and evaluation programme. The Australians have more experience than any other nationality of teaching electronic travel aids and I had the privilege of working with their two most senior instructors. What I learned about skills will prove invaluable when I set up the training programme in Birmingham. The Australian instructors, for their part, were delighted with the devices; I look forward to hearing how their blind clients have fared.

Anthony D. Heyes, Ph.D.
Blind Mobility Research Unit
Department of Psychology
University of Nottingham

HEARING

Recent research work into the mechanisms of human hearing, reported by Blakemore*, has shown that in addition to the so-called 'hair cells' attached to the basilar membrane within the cochlea (the inner ear), which are the basic sound transducer elements transmitting nerve impulses to the brain, there are additional flanking hair cells, receiving nerve signals from the brain, but which are not themselves sound receiver elements.

It has also been observed that the hair cells are much more sharply tuned than the structure of the cochlea, or of the hair cell itself, would allow and that damage to the flanking (non-receptor) hair cells due to disease or certain drugs will diminish both this sharpness of tuning and the ability of the listener to distinguish individual voices in a noisy environment, especially where there are competing voices.

To an electronics engineer with an interest in audio technology, these findings suggest several things, of which the first is that the inability of the ear to separate individual voices in a crowd is the result of intermodulation distortion due to non-linearity in the transducer, and if damage to the peripheral hair cells causes this problem or makes it worse, then it is likely that these flanking hair cells, connected to the brain (but only to receive signals, not to transmit them) are in fact part of a negative-feedback system employed by the ear to improve the linearity of the acoustic transducer mechanism.

If this is the case, then the sharpness of tuning of the hair cell acoustic transducer — inexplicable on purely mechanical grounds, but necessary if an adequate degree of frequency analysis is to be performed — is most probably accomplished by some form of frequency filter, within the brain, in the feedback path to the flanking hair cells.

Interestingly, it has been found that the cochlea also emits sounds, identical to those received, but with a small delay of a few milliseconds, presumably due to the response time lag of the feedback loop, and that in some cases of 'tinnitus' (ringing in the ear), the sounds due to this can be detected, emerging from the cochlea, by a sensitive microphone.

If there is indeed a negative feedback system in the inner ear, with the comparator element being the acoustically coupled central and flanking hair cells, then it seems plausible to the engineer that the problem of 'tinnitus', which usually causes ringing in the ear at one or more specific frequencies, could well be due, in some cases, to feedback loop instability, leading to continuous oscillation. Since an inadvertent increase in loop gain, at certain frequencies, appears unlikely, it seems possible that this could be due to damage to some of the hair cells, so that the projecting cilia were able to touch one another, giving a greater degree of mechanical coupling in the feedback path.

Also, the few milliseconds delay in the response of the feedback system, noted above, makes the cochlea seem unsuitable as a receptor for rapid acoustic transients. This lends support to the hypothesis — which arose from the observation that listeners are often able to distinguish differences in timbre between sounds reproduced from sine and square wave audio waveforms, when the harmonics were outside their ears frequency range — that there may be two separate hearing mechanisms operating simultaneously.

Of these, one is associated with the cochlea and is largely responsible for the detection and analysis of more or less steady state tones, and one is associated with the musculature and bone linkage between ear drum and the window of the cochlea and detects rate-of-change, or transient type pressure signals. This latter function is plausible since this bone linkage is already thought to be responsible for the protection of the inner ear from overload on sudden loud noises through the relaxation of the muscles associated with it.

J.L. Linsley Hood
Taunton
Somerset

*Professor Colin Blakemore, BBC Radio 3 lecture.

RELATIVITY

I fear that Mr Berriman (Feedback January 1986) may be in for a shock if he hopes that the process of tidying up will involve a straight choice between classical and relativity theory, with victory to the former.

That space and time are both absolute is axiomatic to classical theory. During the past fifteen or so years work at the US Naval Observatory, Washington, has unequivocally shown the existence of the phenomenon called time dilation. This finally destroys the logical basis of classical theory, leaving only relativity on the field, whether or not the dilation measured accords precisely with the predictions of that theory. We have got to find another champion if relativity is to be unseated.

With respect to the "basis of relativists' beliefs", in his 1905 paper "On the Electrodynamics of Moving Bodies" Einstein makes it quite clear. After pointing out that there was both theoretical and experimental evidence to suggest that the laws of physics might follow the same principles as do the laws of mechanics, he says: "We will raise this conjecture (the purport of which will hereafter be called the 'Principle of Relativity') to the status of a postulate," and then adds his second postulate. This latter is often condemned as being arbitrary and unjustified, but I have rehearsed elsewhere (Feedback June 1985) the very simple arguments which show that it is in fact implicit in Newton's principles. Relativists beliefs are therefore based fair and square on Newton's principles as laid down in his Principia Mathematica, and the idea that they apply to all of physics. Such things as the Principle of Covariance are merely the logical extension of these ideas.

This may give us a clue as to where to look to find the theory that is able to challenge relativity, because if that is wrong it would appear to be due either to Newton's principles being wrong, or it not being permissible to apply them quite so indiscriminately. I understand that in measurements of the 2.7°K background radiation in the universe some anisotropy has been detected. One interpretation or this is that it gives us a measure of our motion through that radiation. I am totally unqualified to judge whether this interpretation is sound, but if it is it may perhaps give us a pointer as to where to look in our attempts to tidy up.

Alan Watson
Pollensa
Majorca

RAKE'S PROGRESS

I feel bound to speak for the Estabishment against Mr Catt's recently expressed views on electromagnetism which are at best eccentric and at worst nonsense.

Mr Catt claims:

(1) that Maxwell's equations contain no more information about nature than the two constants c, the speed of light and Z_0, the impedance of free space.

(2) that the electric field E and the magnetic field H in an electromagnetic wave are not coupled as Maxwell's equations imply.

(3) Maxwell's equations are normally expressed in terms of unnecessarily abstruse mathematics like divs, curls and grads in order to keep 'knowledge brokers' in employment.

Taking point (1) first, the equations quoted represent a very particular case of Maxwell's equations i.e. the one-dimensional case with no sources (charges or currents). All the interesting physics of electromagnetism (radiation from aerials or even pulsars, refraction of light etc.) comes from including the usual source terms in Maxwell's equations. If Mr Catt leaves them out what does he expect?

Moreover, with regard to point (3), such problems are usually three-dimensional and therefore require the use of Maxwell's equations in their full three-dimensional form with all the divs, curls and grads that Mr Catt finds so abhorrent — or possibly doesn't understand. Each div, curl or grad of a field corresponds closely with a physical concept e.g. curl E is closely related to Faraday's induced e.m.f.; div $B=0$ succinctly states that there are no magnetic monopoles. Thus these mathematical constructs actually give physical insight into problems rather than being something to satisfy the egos of mathematicians as Mr Catt seems to think.

Regarding point (2), Mr Catt gives a nice, but inexact, analogy between a moving tapered plank of wood and a travelling plane-polarized electromagnetic pulse with a wedge profile. He claims that this analogy proves that E and H do not interact or are not coupled. The essential point here is that they are coupled as required by Maxwell's equations and this coupling determines that their ratio could be anything. Mr Catt gets his analogy by artificially imposing the requirement that the width to height ratio is an arbitrary constant. The fact that E/H is a constant of nature follows naturally as a consequence of Maxwell's equations and does not have to be imposed.

The mechanism of the coupling between E and H is well known. At any point, as H changes it generates a perpendicular E field (by Faraday's law which is an integral statement of Maxwell's equation $\text{curl}\,E = -\partial(\mu H)/\partial t$). As that E field changes, it in turn generates a perpendicular H field according to a second Maxwell equation $c^2\text{curl}\,(\mu H) = \partial E/\partial t$). Thus the electric and magnetic fields are mutually sustaining which is a million miles from being uncoupled!

I can only conclude that Mr Catt's view of Maxwell's equations stems from a poor understanding of mathematics and physics. He also displays an amazing arrogance in stating so boldly that he is right and most of the great 19th and 20th century physicists who believe in the conventional interpretation of Maxwell's equations, are wrong. Such arrogance would be forgivable if backed up by sound arguments but alas there are none. Stick to digital design Mr Catt, and you should be OK.

D.C. Hodgson,
Kidderminster

FFT

May I give a few words of comment on R B Hale's letter, in the December 1985 issue on the Fourier Transform and spectral analysis. Although he doesn't use Fourier "mathematics' to arrive at his algorithim, a few moments thought show that he is treading the same path as Fourier.

The Fourier transform is defined thus:

$$Y(f) = \int_{-\infty}^{\infty} y(t) \exp(-i.2\pi ft)\, dt$$

If a real function y(t) varies periodically with t, with a period T, then it can be written as a Fourier series,

$$y(t) = \frac{1}{2}A_0 + [A_n \cos (\frac{2\pi nt}{T}) + B_n \sin (\frac{2\pi nt}{T})]$$

and the coefficients A_n and B_n are given by

$$A_n = \frac{2}{T} \int_{t_1}^{t_2} y(t). \cos (\frac{2\pi nt}{T})\, dt$$

and

$$B_n = \frac{2}{T} \int_{t_1}^{t_2} y(t) \sin (\frac{2\pi nt}{T})\, dt$$

These integrals are both over one period (i.e. $T = t_1 - t_2$) I hope that even the least mathematically inclined (including myself!) can see that Mr Hale's algorithim is just a numerical evaluation of these integrals.

That he discovered the method without recourse to maths is a credit to him — demonstrating that new ideas can arise from playing with a micro.

I would recommend that Mr Hale, and anybody else interested in Fourier transforms and their applications, read two of the more lucid books on FT's. In particular 'Fourier Transforms in Physics' by D. C. Champewey (Adam Hilger) is a general introduction for the BBC micro. 'DFT/FFT and Convolution Algorithms' by C. S. Burrus and T. W. Parks (John Wiky 1984) is more advanced and surveys a wide range of algorithms with examples written in FORTRAN.

The Fourier transform seems to have a mystical status among those not comprehending it — but like most mathematical and computational methods it is only a tool — a highly useful one that should be understood before it is applied, or like picking up a soldering iron by the hot end, you'll get your fingers burnt!

K.G. Purcell
Donnan Laboratories
Liverpool

Having been interested in frequency transform programs for several years, I was intrigued by the program presented by R.B. Hale (Letters, Dec. 85). It operates by convolving the sample data with square waves instead of the usual sinewaves and then subtracting the spurious responses generated by the square wave harmonics from the final spectrum. This has the advantage that a table of sine and cosine values is not needed, but $O(n^2)$ divisions by reals are required instead of $O(n^2)$ multiplications for the DFT or O(n log n) for the FFT.

However, Mr Hale's program does not give the correct spectrum with data where the subtraction of the harmonics gives a non-zero result. This would be the case when, for instance, the input has a sine component at frequency F and a cosine component at frequency 3F.

The correct answer is always produced where there is no input component at a frequency which is an odd multiple of another input component, but this is because if

$$|z1 - z2| = 0'$$

(where z is a complex number), then it is true that

$$|z1| - |z2| = 0.$$

These two results are not the same in the general case. That is, we can have two complex numbers of the same modulus, but which when subtracted do not yield zero. The solution is to accumulate the real and imaginary frequency components in two separate arrays and perform a complex subtraction, before taking the root-sum-square.

The 'small spurious results' seen in the output spectrum result from cutting off the square waves half-way through a cycle, resulting in a non-zero sum. This occurs at any frequency which is not a factor of the number of input samples. The effect of this is very much accentuated when the above modification is applied, since performing a vector subtraction of the harmonics from the spectrum requires good phase accuracy for good cancelling.

Two other comments: The factor of 0.625 in line 250 would better be 1.5708 which is the reciprocal of the mean value of a sine wave and that line 290 effectively calculates terms in the Taylor series for sine.

David J. Greaves
St. John's College
Cambridge

BASIC PHYSICS

I have found the recent articles by Ivor Catt, like previous articles by him and those by Prof. Scott Murray, interesting and stimulating. Essentially, I identify with these gentlemen. But I feel that in their hostility to mathematical physics they do protest too much. I would like to suggest an alternative view.

Throughout the history of science there have been two approaches to its study, namely the causal and the phenomenological or analytic. Briefly causalists require a chain of cause and effect relationships for their understanding of nature, while phenomenalists have no such need, preferring to express and discuss their knowledge in abstract mathematical formulations.

You yourself referred to these two approaches in your editorial section last February *(E&WW* Feb. 85 p.6). You suggested then that the causal approach is appropriate for engineering, but not any longer for pure science. I disagree. I feel that the progress of science in the eighteenth and nineteenth centuries benefitted from both approaches and the rivalry between them, and could do again, if a coherent causalist theory could be developed to assimilate the advances made by phenomenalists in physics during this outcry.

Mr Catt and Professor Scott-Murray are trying to do this, and I applaud their efforts. But they make the mistake of assuming that theirs is the only valid approach to knowledge and that all honest scientists must have the same objective as themselves, namely to identify causal relationships. Hence bad faith and conspiracy are the only psosible explanations for the peculiar positions their opponents seem, to them, to adopt.

The facts are simply that phenomenalists do not have the same objectives and there is no way of deciding rationally which of the two is the one true approach (or indeed, whether there has to be only one approach). The choice is a subjective, personal decision for each scientist.

Surely, the way forward is by co-operation rather than by antagonism. Let us all recognize the equal validity of these two approaches, respect one another's good faith and avoid acrimony in debate.

L. Westhead
Scalby
Scarborough

COMPONENTS SUPPLIERS

A progress report on the components supply industry as experienced further by an ordinary customer is bound, unfortunately, to say that their handling of orders and complaints is worse now than when I wrote in *EWW* in June 1984. No company out of 32 dealt with in the last three years has an unblemished record — expectations of getting what you order and want are entirely unpredictable, and no firm has been discovered that is fully reliable (nor as fast as they all advertise).

That this is general is shown by the fact that at least one company now prints on the back of its despatch notes a tabulated list of complaints for the correct one to be ticked. The space is provided for comments, but little notice seems to be taken of them, as I received back further specimens of the same correctly coded but faulty items which I had told them were in fact out by a factor of 100. And morever suggested that they check their stock!

Until professionals and management of all companies, not only in electronics, from manufacturing to retailing and service recognise that they have real obligations to their clients and that there is increasingly no market for shoddy and faulty goods and services the nation's real trade internally and for export will continue to decline.

David White
Llangefni
Gwynedd

Letters

Letters for publication are always welcome, but the shorter and pithier, the better. I try not to edit original letters, but sometimes they are far too long, and therefore cut, and the writers upset. Please keep your letters short.

High-speed interface/buffer 2

Using a-to-d converter output as an address, this buffer interface stores 500 million words in 16Kbyte of memory.

by J.F. van der Walle M.I.E.E.

To produce an overflow indication use has been made of output RCO of the 74LS593 register-counter, which goes low when all eight counter outputs are high. When the data word 1FFF has been reached, pins 11 of $IC_{11,7}$ are low.

Gate pin 12 of IC_{22} now goes high, raising pin 6 of IC_{24}. This only happens during data acquisition when pin 5 of IC_{29} is high.

If pin 10 of IC_{22} is now connected to pin 6 of IC_{24}, the converter flag on pin 11 of IC_{22} will be locked out and data acquisition stops. If this feature is not used, the channel containing data word 1FFF will be incremented to zero so all data will be lost in this particular channel. Pin 10 of IC_{22} can also be used to stop the converter at any time. Overflow output pin 6 of IC_{24} goes low again with a reset signal on pin 1 of IC_{24}. Resetting of pin 1 of IC_{24} can be done either manually or by computer, see computer-to-buffer connections, Fig. 6.

Zeroing memory

As mentioned earlier, a data acquisition run starts with all memory locations containing zero. Large memory chips do not have reset input; the only way to clear them is to write zeros to each memory location.

Bistable circuits $IC_{27,28}$ (Fig. 5, over) are incorporated in the design for this purpose. When a low reset signal is applied to the buffer-interface the following happens:

- Register counter $IC_{13,14}$ and address latch $IC_{5,9}$ are cleared.
- Bistable devices $IC_{29,30}$ are cleared through pin 8 of IC_{20}
- Pin 6 of IC_{27} goes low and applies a permanent pseudo converter flag through pin 4 of IC_{26}.
- A permanent low is placed on pins 12 of $IC_{11,7}$ by pin 9 of IC_{28} going low.
- Pin 10 of IC_{28} goes high, enabling bistable IC_{27} and the counter of $IC_{14,13}$.

The pseudo converter flag generates the same 900ns sequence as a normal converter flag, but now the counter of $IC_{13,14}$ addresses all the memory locations in sequence. When $\overline{OE}$ is enabled, any value may appear after power-up. All these words are overwritten by data word zero; because of the clear signal on $IC_{11,7}$ this will be the only value appearing on the outputs of $IC_{11,7}$ when the bus-driver output is enabled.

This continues until $\overline{RCO}$ of IC_{13} goes low, when pin 6 of IC_{27} goes high and pin 7 sets a pseudo RDRQ signal. The same 600ns RDRQ operation follows and all of the memory locations are checked to make sure that they contain zero. This is done with the eight Nor gates $IC_{3,4}$.

If any location does not contain zero, bistable output pin 7 of IC_{28} goes high and stops pin 9 going high again. This pseudo read-request run is ended by a low on line $\overline{RCO}$ of IC_{13}. During the converter data-acquisition run, the test point must always be high. The entire reset/check procedure takes about 110ms.

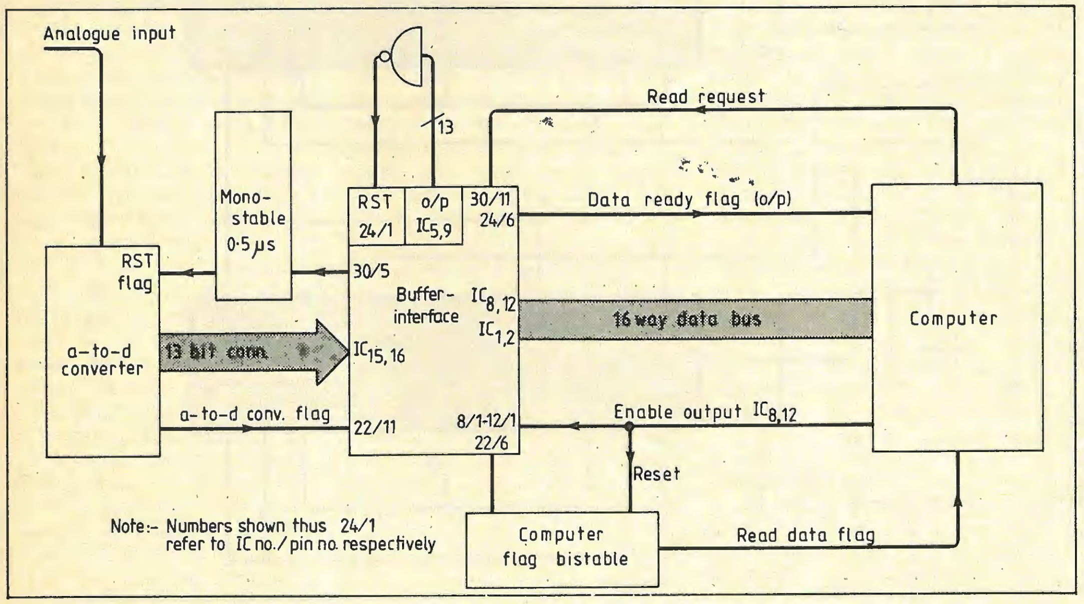


Fig. 6. Computer-to-buffer connections. Data is stored in the buffer without computer intervention.

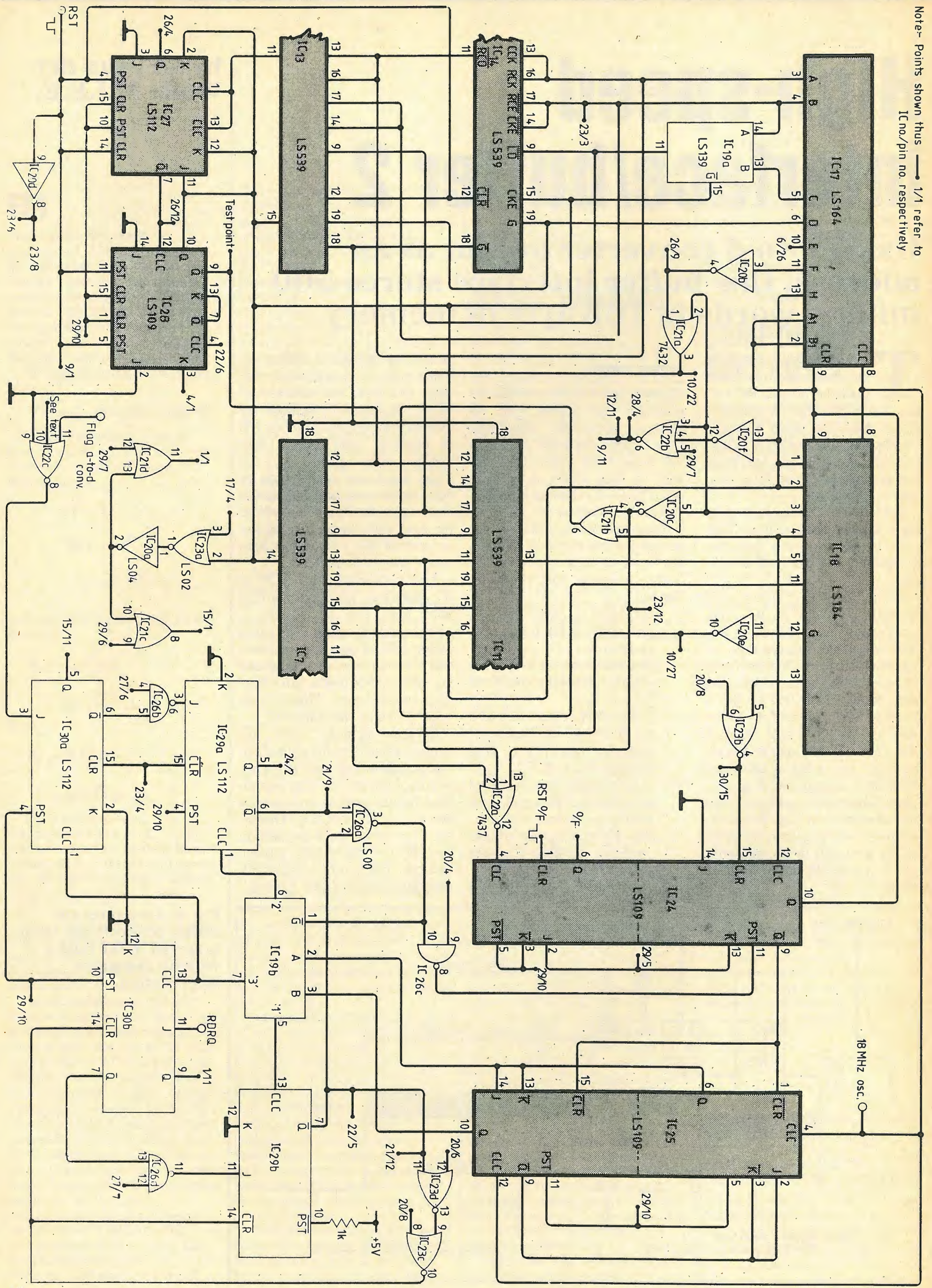


Fig. 5. Logic controlling the high-speed buffer/interface, left. Storing of an a-to-d converter data word takes about 900ns.

Computer-to-buffer connection

The illustration of external connections shows how to connect the buffer to the computer. Because of the great variety of computers this is only a general diagram.

If the computer wants to have access to data in the buffer it sends an RDRQ signal, to pin 11 of IC_{30} in the buffer and simultaneously places the address word in the 16-way data bus.

This read request is processed by the buffer logic (see Bus system — data out) and the data belonging to a specific address word is stored in $IC_{8,12}$ by clock signal pin 6 of IC_{22}.

Pin 6 of IC_{22} sets the computer-flag bistable device and a Read-data flag is sent to the computer. Immediately, the computer sends an Enable-output signal to $IC_{8,12}$ which also resets the computer flag bistable circuit. Now a data word from $IC_{8,12}$ is placed into computer memory through the 16-way data bus.

This procedure is only used for checking contents of a specific channel while data acquisition takes place, Fig 6.

Block transfer

When a channel in the buffer has collected 2^{16} counts the Data-ready flag is set through pin 6 of IC_{24}. Address-word zero and a Read-request signal to pin 11 of IC_{30} are sent back by the computer.

From here, the procedure is as above from the Read-request processing point, but pin 6 of IC_{24} still locks out the converter flag. Address-words 0000 to 1FFF are now sent sequentially, each followed by its own data-word, for storing in computer memory.

Address word 1FFF resets the Data-ready flag (pin 6 of IC_{24}) through address-word buffer $IC_{5,9}$ and a 13-input Nand gate. When the computer has taken in 8192 (2^{13}) data words the converter resumes its data-acquisition.

Conclusion

The buffer-interface has proved to relieve the computer to such an extent that it essentially becomes a stand-alone device. With direct memory-block transfer, the computer is only used for magnetic tape data dumping and display.

High Technology and Computers in Education '86

This year's exhibition, held at the Barbican in January, was well attended by both exhibitors and the public.

For electronic engineers, the star of the show was undoubtedly the Qudos silicon design system. This c.a.d. package, which runs on the new BBC Master series computers, is already being supplied to every university in Britain. The user lays out and tests his own i.c. on the screen (there's a choice of bipolar u.l.a. or high-speed c-mos families), then sends the disc to Qudos at Cambridge. Qudos (it stands for 'quick design on silicon') blast the design on to silicon with their electron beam lithography machine and post back the finished chips a few days later.

Peter O'Keeffe of Qudos believes his system brings chip design within almost everyone's reach, just as the BBC and Acorn brought computer literacy. With starter packs priced from about £500, the package should appeal to small companies and even to the well-off hobbyist: O'Keeffe points out that this compares reasonably with the cost of the hardware. Further details are in our news pages. EWW 247.

Elsewhere, Master series computers were receiving their first public showing on the Acorn stand. Educational computing and the BBC Micro are still almost synonymous, though the 16-bit Research Machines Nimbus, being demonstrated only a few yards away, seems likely to give Acorn quite a run for their money. With its 80186 processor, 576K ram, quick-as-lightning graphics and Microsoft Windows operating system, the Nimbus looks remarkable value for any educational or c.a.d. system. Prices start at £695 for a single-drive version. EWW 240

But the standard Model B BBC micro was still much in evidence at the show as the basis of a vast range of c.a.d. and control systems.

Among the more off-beat examples was a weaving loom for the student or private user. The loom, which is made of glowing, polished beech-wood, has a control-box on top which stores the weaving pattern and feeds in the chosen yarns. Data can be put in with a key-pad or from the computer design station, at which colour combinations and patterns can be tried out on the screen. The looms, by Harris Looms of Ashford in Kent, are priced from £540 for a 15 inch model. Software is from £150, and there are two tutor programs at £15 each. EWW 241

One of the most crowded stands was that of Lego UK, who were showing a series of educational packs based on their technical construction components. Several working models made from these were on display. One of them, unbelievably, was a small chart-plotter made entirely from Lego pieces; others included buggies and a conveyor-belt brick-sorting machine.

The packs include motors, lamps opto-sensors and computer interfaces and are intended to encourage the student to discover where and why automatic control is needed before trying to implement it. EWW 242

Experimental sets for a rather older age-group were to be found on the Flight Electronics stand. Their microelectronics applications board, designed by David Turner of the College of Further Education in Plymouth, is a double-sided p.c.b. about 170mm square and packed with leds, switches, controls, light and temperature sensors, a motor, multi-way connectors, i.cs and other components. It recalls irresistably those Activity Centre toys without which no tiny tot's cot is complete, but it comes with a full manual detailing 15 experiments in such areas as using a logic probe, making decisions, event counting, bit-masking, waveform generation, keyboard scanning and more.

A mains power supply and interface for the BBC Micro are included with the unit, which costs £175. Other versions suit Flight's Micro-Professor Z80 educational computers and their 16-bit MPF-1/88 system. EWW 243

Several other microprocessor trainers were shown. One interesting example was '3 Chip Plus' by Unilab of Blackburn and the MEP. This 6502-based set-up is a range of boards which can be daisy-chained together; besides the processor board itself, there is a program loader board (containing the monitor program), a ram board, plus eprom blower and i/o cards. EWW 244

A family of low-cost i/o boards by DCP Micro Developments includes units to satisfy a wide variety of control requirements. The boards plug together to make up the configuration required and can be interfaced to many types of computer by means of a replaceable personality module. EWW 245

For more complex control systems, Saab Automation showed an intelligent data and i/o control box which can be programmed from any terminal with an RS232 port. A feature of the programming language is its plain English commands (other languages are available); there are some 64 of them and they can cope with such applications as sequence controlling, bar-code reading and event recording. Various analogue and digital i/o modules can be fitted to the basic unit. The Saab Worker PCC930 is designed and made in Britain, and typical system starts at a little less than £500. EWW 246.

by David Whitehouse

25 years of man in space

A chronicle of man's achievements in space since Yuri Gagarin became the first man in orbit — and prospects for the future

Space shuttle lifting off

It is a bright April morning at the Tyuratam Cosmodrome, about 230 miles south-east of Baikonur in the Soviet republic of Kazakhstan. An ordinary-looking tourist coach pulls up beneath a skeletal steel tower, which supports a 125 foot rocket. Two men, dressed in orange flight suits and white helmets, emerge from the coach, shake hands and touch helmets. One of them climbs a small flight of stairs towards a lift and turns to wave. At the top of the rocket he enters, feet first, a cramped spherical capsule and the door is sealed behind him.

Yuri Alexeyevich Gagarin, born March 9th 1934 near Smolensk, the son of a carpenter and a cosmonaut trainee for only a year, was about to become the first man in space. In less than two hours he would be back on the ground and his name would be on everyone's lips.

After a short delay due to a faulty valve, the Vostok A1 rocket ignites at 9.07am Moscow time. The film of the lift-off, first seen in the west seven years later, shows the rocket's shadow moving over the flat steppe around Tyuratam. "Off we go!" shouted Gagarin.

Breathing a normal atmosphere Gagarin entered orbit a few minutes later. "The sky" he said, "looks very, very dark and the Earth is bluish." He said that zero gravity was very relaxing and a welcome change to the g-forces of lift-off. Two hundred miles about the Earth, retro-rockets fire during Vostok 1's first pass over Africa and re-entry begins.

The spherical capsule with Gagarin inside separates from the retro-package and plunges deep into the atmosphere, glowing red as its protective coating shields the first spaceman from the fiery heat of re-entry. At 13,000 ft, a drogue parachute is deployed, followed by the main parachute at 8,000 ft. In 108 minutes Gagarin has travelled 25,400 miles and lands in a field near Saratov, watched by a cow and two farm workers. Gagarin had been promoted to major during the flight as it had been announced to the world. The Russians had not only placed the first object in space, Sputnik-1 three and a half years earlier, they had also put the first man in space and to many it seemed inevitable that they would also land the first man on the Moon.

President Kennedy's Bay of Pigs fiasco coincided with Gagarin's flight and, less than two weeks later, western prestige was further eroded when an Atlas rocket exploded above Cape Canaveral while trying to get the first Mercury capsule into orbit for an unmanned test. Although the United States didn't know it at the time, their one-man Mercury capsule was rather more sophisticated than its Soviet counterpart.

Less than a month after Gagarin's pioneering flight, 38-year-old Alan Shepherd sat in a Mercury capsule called Freedom 7 atop a Redstone rocket. Unlike Gagarin's flight the world was watching. At 9.34 a.m., Mercury-Redstone 3 took off and sent Alan Shepherd into a 15 minute and 28 second sub-orbital flight. During his brief ride he tested the Mercury systems in preparation for an orbital flight.

Two months later Gus Grissom made a repeat performance of the mission. But in between the two flights President Kennedy made a historic speech. Against expert advice, and with the US having only 15 minutes of manned space experience, Kennedy said, "I believe this nation should commit itself to achieving the goal, before this decade is out, of landing a man on the Moon and returning him safely to the Earth." The stage was set, prestige was at stake and before space exploration had barely begun it had been turned into a race for the Moon.

In August, five months after Gagarin's flight, the Soviets made another leap. Gherman Titov, at 25 the youngest man ever to go into space, stayed aloft for over a day and made 17 orbits of the Earth. The massive leap from 1 to 17 orbits resulted from the need to land the Vostok 2 craft in the prime recovery zone which would be overflown every 24 hours or 17 orbits. Titov was the first man to sleep in space and also the first to be spacesick.

The second year of spaceflight, 1962, saw many barriers removed. In February, John Glenn became the first American to orbit the Earth in Friendship 7 after three launch postponements. It was a flight that attracted worldwide attention but, in fact, Glenn wasn't supposed to be the first American in orbit. After the chimpanzee Enos was recovered from the Atlantic Ocean in November 1961 NASA confirmed that the third, and final, Mercury sub-orbital flight was to be cancelled and the astronaut assigned to the orbital mission. So Glenn, instead of flying the most anonymous Mercury mission, got the flight that the original seven Mercury astronauts coveted most. It was a bitter blow for Deke Slayton who was to have flown the first orbital flight. Before the next Mercury flight he was grounded because of a heart flutter and had to wait until 1975 to go into space. In May, Scott Carpenter became the sixth man in space and the fourth to go into orbit, but meanwhile the Russians were planning a space spectacular.

At the time, the Vostok 3 and Vostok 4 missions, launched August 11th and 12th 1962, appeared to be a brilliant technical and propaganda success. But the West did not know much about the Soviet space programme and gave the dual Vostok flight more attention and significance than it deserved.

For a short time after Vostok 4 entered orbit, the two manned spacecraft were only four miles apart. But, despite an eminent British scientist predicting a Russian lunar landing by 1965, the close approach of the two Vostoks was not a true rendezvous, since neither had the ability to manoeuvre from orbit to orbit to effect a true rendezvous. The ability to rendezvous and dock in space, vital to any Moonflight, had yet to be demonstrated.

There were two more flights before the Mercury project officially ended on June 12th 1963. Six astronauts had spent a total of 2 days 5 hours 55 minutes and 27 seconds in space at a cost of 392 million dollars. The US space programme was to move onto the two-man Gemini project. The Russian space programme however, although the West didn't realise it at the time, was running into serious difficulties.

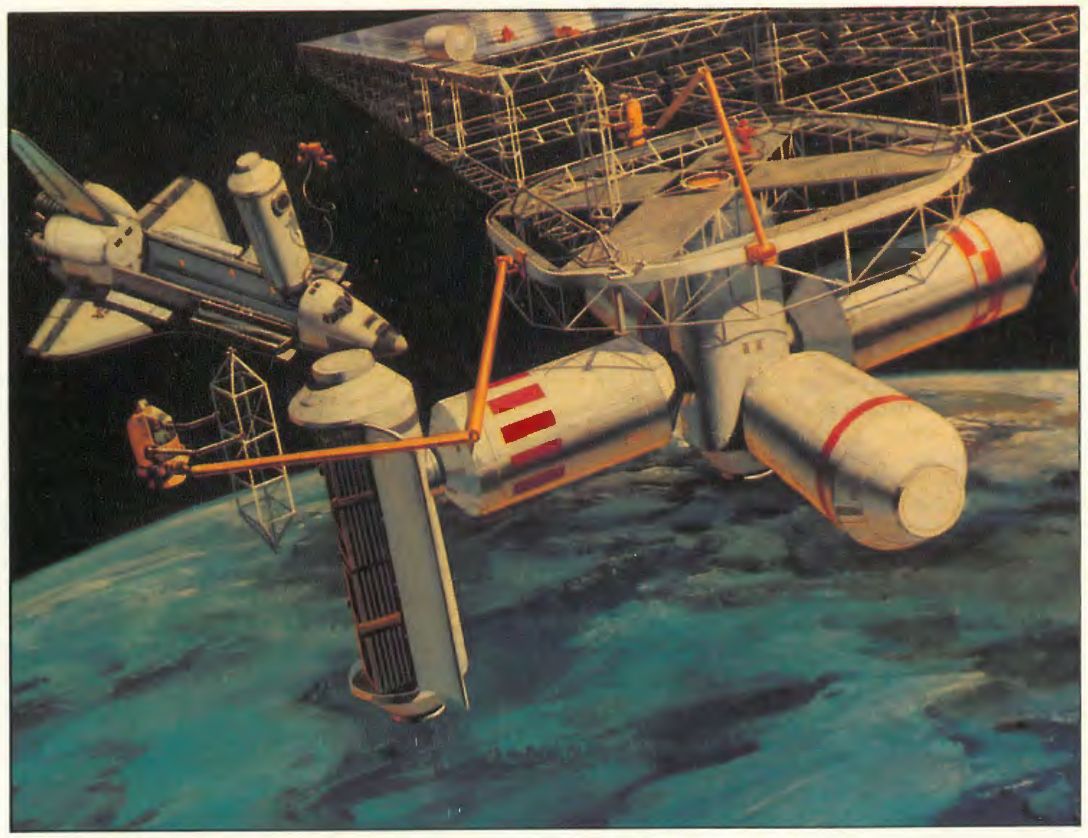
During the early days of June 1983, rumours emanating from Moscow spoke of the impending launch of a woman into space. More details emerged: a man was to be launched first, to be joined by a woman the following day. Valeri Bykovsky blasted off in Vostok 5 on June 14th to be followed two days later by the first woman in space, Valentina Tereshkova in Vostok 6. There is a rumour that Tereshkova was the back-up woman cosmonaut who flew after the prime candidate was incapacitated the day after Bykovsky's launch. True or not, Tereskova seems to have had a miserable flight; she is said to have pleaded to come home but was kept in orbit for three days. Bykovsky, on the other hand, stayed in space for 81 orbits and 2 million miles, equivalent to travelling to the Moon and back four times! He still holds the record for the longest solo spaceflight and in these days of multi-man missions seems unlikely to lose that honour.

Like Mercury, the Vostok programme ended after its sixth flight. Soviet manned spaceflight had clocked up 15 days 22 hours and 21 minutes, 13 days ahead of the US.

The fact that no other woman followed Tereshkova into orbit until Svetlana Savitskaya in 1982 lends weight to the suspicion that her flight was simply one more stunt in Premier Khruschev's series of space spectaculars. The next one was to be very dangerous and foolhardy indeed.

The newspapers of the West carried banner headlines of the flight of Voskhod 1 on October 12th 1964. Before any two-man crew had been into space, the Russians were launching three. Spectacular leap it seemed, but it wasn't. It was probably the most perilous space mission ever undertaken, and all because of Khrushev's quest for new space spectaculars to maintain the Soviet Union's psychological lead over the United States in the Cold War. Three men, two of them having begun cosmonaut training only six months earlier, were crammed into a stripped down, one-man Vostok spacecraft. There were no spacesuits or ejection seats. No spare fuel, parachutes or reserve oxygen. Fortunately the mission ended after 24 hours. This may have had something to do with the downfall of Nikita Khrushev, who talked to the crew by phone during the flight was was apparently ousted in mid-sentence. The only manned spaceflight of 1964 ended safely, but it could have easily been a very different story.

The last Russian space spectacular occurred in March 1965 when the two-man Voshkod 2 was



Artists impression of communications centre of the 1990s — an array of antennas for world-wide communications.

Yuri Gagarin entering the orbiter capsule on the Vostok rocket (Photo — TASS).

launched just five days before the scheduled launch of the first two-man Gemini mission. The mission lasted just over a day and during it Alexei Leonov became the first man to walk in space. His spacewalk gave the green light to astronauts performing useful work in space and ultimately the Moonwalks. But Leonov had great difficulty in returning to the spacecraft. His spacesuit had ballooned, meaning that he spent most of his 23 minutes 41 seconds outside trying to get back in. From now on Gemini was to steal the show.

The two-man Gemini missions were the secure foundations on which the Apollo Moonshots were built. The spacecraft became increasingly more sophisticated and the manouevring and docking techniques more refined. The first Gemini flight was in March 1965 and was Gemini 3 with Gus Grissom and John Young onboard at the start of a remarkable space career. Gemini 3 was the first spacecraft to simulate rendezvous in space by changing its orbit. The Gemini craft had the first ever onboard guidance computer and a 100% oxygen atmosphere. Later Geminis carried an onboard radar and a unique fuel-cell system. Ed White became the first American to walk in space during Gemini 4, which also rendezvoused with a Titan 2 second-stage rocket. During that mission the computer failed and White and McDivitt had to make a manual re-entry of 8 g, probably the most strenuous entry ever performed.

Geminis 4 and 5 took the lead in space exploration and technology away from the Russians. The motto for Gemini 5 was 'Eight days or bust.' It was also the first mission to try and get men to spy from space: the crew, however, failed to see specially constructed targets but did see a rocket lift-off and the wake of their recovery ship. As one newspaper said at the end of the mission, 'Now for the Moon shot.'

Geminis 6 and 7 were in space at the same time and practised rendezvous, the greatest hurdle for a Moon mission. With hindsight, the confidence and experience gained during the 14 day flight of Gemini 7 made it one of the most important missions prior to a lunar landing. Space travel was becoming routine, success was coming easily and it was time for the first emergency in space.

That emergency was provided by Gemini 8 with Neil Armstrong and Dave Scott onboard, who were both to later walk on the surface of the Moon. Their task was the first space docking, attaching their Gemini craft to an Agena target vehicle. This they did without a hitch, but when they tried to manoeuvre the combined Gemini-Agena the trouble began. A rogue thruster sent them into a spin. "We're backing off," said Armstrong. The two craft separated, but the trouble got worse. Though the Agena steadied, Gemini continued to spin once every second with the possibility of a catastrophic collision. Armstrong again: "We've got serious problems here . . . we're tumbling end over end . . . we can't turn anything off!" Analysis showed that the only way to control the spin was to use the re-entry thrusters, which meant an emergency return to Earth. Armstrong and Scott had been lucky.

'I believe this nation should commit itself to achieving the goal, before this decade is out, of landing a man on the Moon and returning him safely to the Earth'. John F. Kennedy 1961.

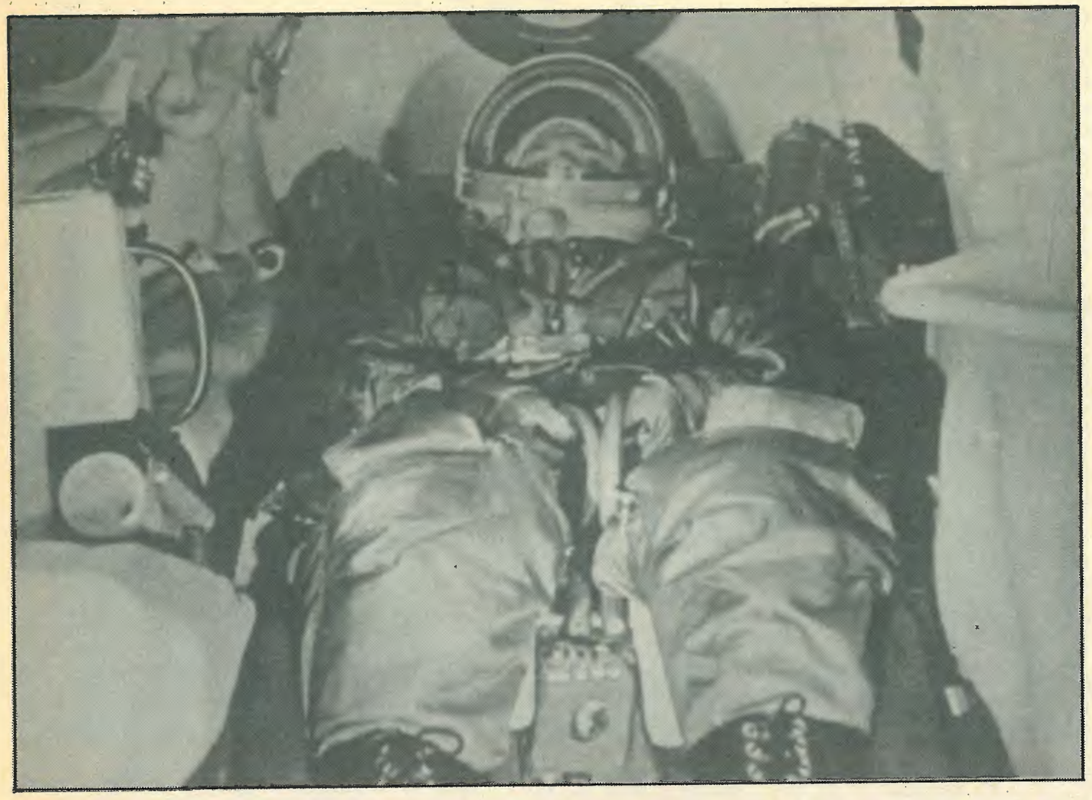
Between June and November 1966 there were the final four Gemini flights and with only minor problems they all went well: Eugene Cernan overheated during a spacewalk on Gemini 9; John Young, second time in space, showed with Michael Collins how to change orbit and rendezvous with two target vehicles; Collins made a spectacular intercraft spacewalk; Gemini 11 had a staggering view of the Earth from 850 miles up. When Lovell and Aldrin went on the final Gemini flight, Gemini 12, they wore cards on their backs saying 'The End': when they got to the spacecraft there was a sign fixed to it saying 'Last chance. No returns. Show will close after this performance.' Gemini had cleared the way to the Moon at a cost of 1,283 million dollars and over 80 man-days in space. It was now to be the time of Apollo and disaster.

The year 1967 was a tragic one for space exploration. Four astronauts were to die, three on the ground and one in space. Astronauts Grissom, White and Chaffee had been carrying out a ground run-through inside an Apollo Command Module atop an unfuelled Saturn 1B on pad 34. A fire, caused by a short circuit and nourished by the pure oxygen atmosphere, became an inferno in seconds. The disaster delayed the Apollo programme for two years but the extensive redesigning of the Command Module undoubtedly contributed to the future success of Apollo.

Disaster also occurred on the first Russian manned spaceflight for over two years. April 1967 saw the flight of Soyuz 1, the 25th manned spaceflight and the 23rd manned orbital mission. Soyuz was Russia's new spacecraft and is the Russian word for 'union'. It was the first night launch and the veteran cosmonaut Vladimir Komorov was alone on a mission that went well until an unlucky 13th orbit. The stabilization failed, causing a Gemini 8-like spin and then the computer failed. Komorov attempted to re-enter on the 16th orbit but failed and failed again on the next orbit. After this Komorov knew he was doomed and spoke to his wife and Premier Kosygin. On orbit 18 the retros were fired in a final attempt to re-enter. The main parachute tangled and failed at 25,000 ft. Komorov, who may already have been dead, could not have escaped from Soyuz 1, which smashed to the ground. The Soviet comeback in space had ended catastrophically and it would be a year and a half before the Russians tried again. With the aftermath of the Apollo fire the previous January there was to be an 18 month hiatus in manned spaceflight.

It was resumed by Apollo 7 in October 1968. Within a year, two men would walk upon the Moon. Apollo 7 was a 10-day engineering shakedown of every system, indeed every wire, of the Apollo Command and Service Modules to ensure their Moonworthiness. Activities and manoeuvres were designed to simulate and reproduce the en-route activities of an actual lunar mission. The mission was a great success and the way was clear for a non-landing trip to the Moon two months later. But before then the Russians were back in space.

The manned Soyuz 3 went aloft to try and rendezvous with the unmanned Soyuz 2. They only got within 700 feet of each other: evidently there had been problems with critical close-manoeuvring. Curiously, at that time the Soviets sent a Zond craft, essentially an unmanned, modified Soyuz, to loop around the Moon. Did they still have dreams of a manned lunar landing of their own?



Gagarin inside the capsule on April 12, 1961 (Photo — TASS).

It was now Christmas 1968 and Apollo 8 was to make the first manned flight to, and orbit of, the Moon. Just after lunar orbit insertion the crew looked back at Earthrise over the barren and airless limb of the Moon. The sight of the tiny and fragile blue and white Earth hanging in space changed many people's perception of the Earth. Spaceship Earth became a concept for a generation. After an eight-day flight they splashed down in the Pacific. America looked towards 1969, the year of the Moon.

In January 1969 the Russians launched Soyuz 4 and 5 with a one and three-man crew. Both craft docked in space, leading to Russia's claim of the first experimental space station. But all eyes were on the Americans and their final two rehearsals for the Moon landing.

In March, Apollo 9 tested the lunar landing craft, called the Lunar Module, in Earth orbit and in May, Apollo 10 carried out similar tests whilst in lunar orbit. At one time the Lunar Module, nicknamed Snoopy, fired its descent engine for 27.4 seconds and swooped only nine miles above the Sea of Tranquility. Just as they were about to fire the rocket to return to the Command Module, euphoria nearly gave way to disaster. The Lunar Module went into a spin and it took Cernan eight seconds to bring it under control, "I'll tell you there was a moment there," he said later. After 31 orbits of the Moon Apollo 10 returned to Earth after travelling 830,000 miles in eight days. Stafford, Cernan and Young had done everything — except make history.

That was left to Neil Armstrong, Edwin Aldrin and Michael Collins. The Apollo 11 crew weren't in any way special, they were just next in line. Their objective was quite simply 'to land two men on the Moon and return them safely to Earth' so achieving the national goal set by President Kennedy. The flight began at 9.32 am on July 16th as the now tried and trusted Saturn V rose ponderously from pad 39A to the cheers and prayers of a million spectators. In lunar orbit, Armstrong and Aldrin entered the Lunar Module and on the far side of the Moon, at 100 hours, 12 minutes into the mission, they separated from Collins in the Command Module.

A 30s engine burn put them in the first part of their descent trajectory, a 57.2 by 9.1 mile orbit. At the lowest part of this orbit the engine had to fire again. At 47,000 ft, 2 minutes 11 seconds into the burn, the alarm flashed, indicating that the computer was overloaded with commands. Mission Control told the astronauts to ignore it, "You are go to continue powered descent" they said. The Lunar Module, named Eagle, turned to begin its final approach to the Sea of Tranquillity. Another alarm sounded, but the brave decision was to ignore it; "You are go" said Ground Control "You are go." In the last few moments of descent Armstrong realised that they were heading for a rockfield and had to manually take over. With just seconds of fuel left they set down. It was 9.18 BST on July 20th 1969, man was on the Moon.

Armstrong placed his left foot on the surface of the Sea of Tranquility at 3.56 a.m. BST on July 21st. It was the end of an era, the prize had been won and the dream was beginning to fade.

Armstrong placed his left foot on the surface of the Sea of Tranquillity at 3.56 am BST on July 21st 1969. It was the end of an era, the prize had been won and the dream was beginning to fade.

Twelve men walked upon the surface of the Moon, spending 160 man-hours there. They covered 60 miles on foot and by Moon-buggy. 2,196 samples of rock, weighing 837 lb were collected. More than 30,000 photographs of the Moon were taken, there were 60 major experiments on the surface of the Moon and 30 in lunar orbit and it had become routine. Apollos 18, 19 and 20 were cancelled and the money-spinning US space programme was a prime target for cut-backs. America's space programme went into decline.

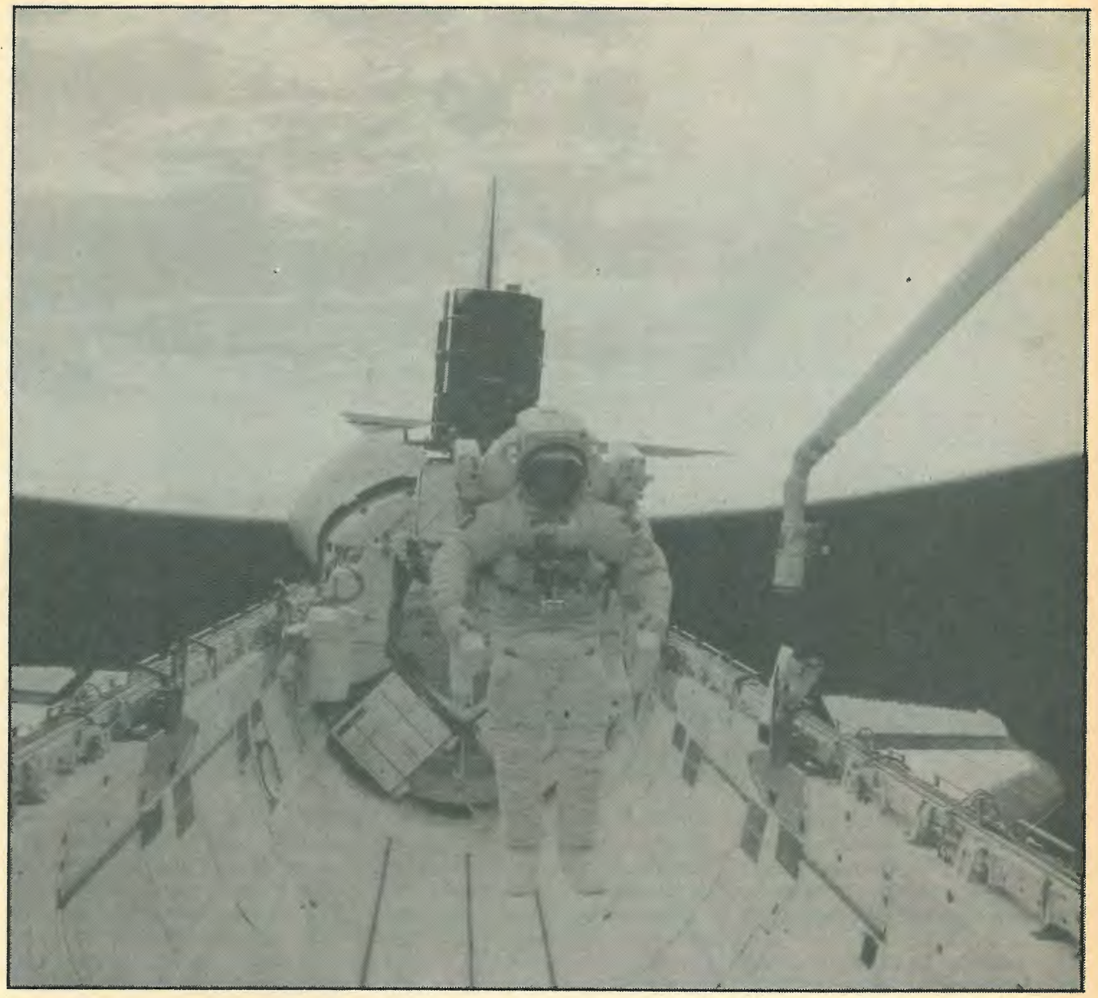
The only exception to the growing public indifference to the Moon landings came with Apollo 13. Nearly 56 hours into the mission, en route to the Moon and 205,000 miles from the Earth, a liquid oxygen tank in the service module exploded. Within two hours, the crew were without service module oxygen, water, electricity and propulsion. They would have died had they not been able to use the lunar module, Aquarius, as a liferaft during a circle of the Moon and return to Earth.

For the rest of the decade after the Moonshots there were to be only four more manned US spaceflights. During that same period there were 22 manned Soviet missions. The emphasis of space exploration was changing, America needed a new direction.

In 1973 Skylab became America's first, and so far only, space station. It started life in 1966 as the Apollo Applications Programme, designed to use Apollo hardware not used in lunar landings. Basically a converted Saturn stage, it had two docking ports, solar panels, a telescope mount and 13,000 cubic feet of working volume. It housed three teams of three astronauts for 28, 56 and 56 days respectively, who conducted the most comprehensive series of scientific experiments in space thus far. Skylab was launched on May 14th 1973, using the final Saturn V, and just 63 seconds into the flight one of Skylab's solar wings were ripped off and the other failed to deploy in orbit. Skylabs first crew had to carry out some complex, last-minute repairs and became the first space repair crew.

Aside from nine days spent in space when Apollo 18 linked up with Soyuz 19 in July 1975, the next manned US spaceflight was on April 12th 1981, 20 years to the day after Gagarin's epic flight. It was the 80th manned spaceflight, the 77th manned mission to orbit the Earth and the first flight of the Space Shuttle.

After Apollo it became clear that costly hardware could not be thrown away with each manned mission and that a re-usable, or at least partly re-usable, spacecraft was needed. And so the Space Shuttle was developed, a manned orbiter getting into space using fuel held in a large external fuel tank and assisted for the first two minutes of flight by two solid-fuel rocket boosters, all except the large external fuel tank being re-usable. Two days before, a computer failure cancelled the first flight with only minutes to go. But at 7 a.m. local time on April 12th, 1981, Space Shuttle Columbia blasted into



Shuttle mission 41C in April 1984. Astronauts Nelson and Van Hoften had just completed repairs on the Solarmax satellite in the background.

space for a two-day mission. It was the first time a space vehicle had been flown for the first time with men onboard. One of these men was John Young, who was entering space for the fifth time. Nine years earlier he had walked upon the Moon during Apollo 16. He has flown on the Space Shuttle more than once and will fly again.

When the fourth shuttle flight landed on Independence day 1982, President Reagan was there to greet it and declare the space shuttle operational. He went on to direct NASA to investigate a more permanent presence in space. It cannot have escaped his attention that, as he spoke, four Russians and a Frenchman were in orbit aboard the Salyut 7 space laboratory. Two of them were to stay in space for what was then a record 211 days.

Whilst America developed its space shuttle, the Soviets had other goals. The history of the development of the Soviet Space Station is not an altogether happy one. The world's first space station, Salyut 1, was launched in 1971, but the first crew failed to dock with it and it was left to the second crew to take up residence. But this mission ended in tragedy as they undocked. An open valve caused rapid decompression and the crew died within seconds. Salyut 1 was never used again and the redesign of the Soyuz craft took two years.

The next two space stations, Salyut 2 and Cosmos 557, failed to become operational. Salyut 3 had improved living and working quarters, but the rendezvous and docking problems remained, and the second crew aborted their mission, marking the end of Salyut 3.

Salyut 4 fared better, being occupied for 100 days. Salyut number 5 was both a scientific and spy platform. Salyut 6 was a much improved station over its predecessors, with two docking ports. Spacecraft called Progress, basically a stripped-down Soyuz flying on auto, could dock with it to deliver supplies. Salyut 6 lasted for three and a half years and was visited by 16 crews and 15 unmanned craft. It was occupied for 676 days, among which flight engineer Valeri Ryumin spent almost a year in space and travelled 150 million miles — further than the distance to Mars!

Salyut 7, the current station, was launched in 1982 and is even more improved, with strengthened docking facilities. In 1984 a crew spent a record 238 days onboard but there have been problems; fuel leaks, damaged solar panels and battery problems. Extensive spacewalks were conducted in 1984 to repair it and in 1985, following a malfunction whilst unmanned, a repair crew had to dock with an essentially dead station before bringing it back to life. In late-1985 it was abandoned when a crew returned to Earth in a hurry after one of them became ill. It seems unlikely that the ageing Salyut 7 will be visited again. On February 19 they launched a radically new space station, Mir, which means peace. It has six docking ports and individual cabins for each crew member and, although details are still sketchy, it is a major improvement on Salyut 7.

In the meantime the space shuttle had become operational, deploying satellites and carrying men and women into space to perform experiments. We have even seen atronauts flying free using backpacks to capture errant and malfunctioning satellites for repair in space or return to Earth. Even US Senators have hitched shuttle rides in space. Although there were problems with spare parts and an optimistic launch schedule, the shuttle programme was going well until its 25th flight which, after delays, blasted off from Cape Canaveral on the morning of January 28th 1986.

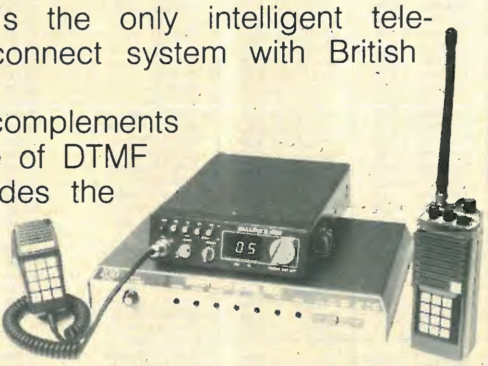
The sight of the fireball that destroyed shuttle Challenger with the force of a small nuclear weapon only 73 seconds into flight will be remembered by all who saw it. Following the death of the crew of seven, all space shuttles are grounded until the cause of the catastrophe is found. There is overwhelming evidence that a rupture of one of the powerful solid-fuel rocket boosters caused the fatal explosion.

And so, on the 25th anniversary of Gagarin's flight and the 5th anniversary of the first shuttle flight, where do we go? When shuttle flights resume we will see the construction of a space station during the mid-1990's on which six astronauts will work for up to four months at a time. It will be a quantum leap in space technology.

Beyond the year 2000, attention has turned to the type of space vehicle that will succeed the space shuttle — this time, a totally reusable craft called a transatmospheric vehicle capable of direct flight into space and pasenger flight across the world in an hour. Britain may even become a major spacefaring nation if its concept of a spaceplane with an air-breathing engine, called HOTOL (HOrizontal Take-Off and Landing) is developed.

The Soviets are also developing their own space shuttle, in two versions. The larger version is very similar to the US design, though less sophisticated. The smaller shuttle, called Buran (snowstorm), seems to be a quick response vehicle of some kind, possibly carrying anti-satellite weapons. The Soviets also have on the pad at their Tyuratam launch base a heavy-lift launch vehicle that will become the most powerful rocket in existence and will be used to place large and complex payloads into orbit. The problem is that the rocket at the core of this launch vehicle, called SL-X-16, which will also be used to launch the large Soviet shuttle, has encountered serious problems and is holding back their manned space programme. When these problems have been overcome, and there are recent rumours that they have, the Russians are poised for some remarkable space acitivity. It is not inconceivable that they will mount a manned mission to Mars as early as 1992, which is seven years before any possible US mission.

It is remarkable that we have come so far in so short a time. Just eight years separates Gagarin's flight from the first Moonwalk, and it is only nine years between the last Moonwalk and the first flight of the space shuttle. The advances in space technology during this time have been breathtaking and staggering. What will we have done when we celebrate 50 years of manned spaceflight in 2011 from bases on the Moon and on the red sands of Mars?■



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AD149	0.70
AD161	0.39
AD162	0.39
AD161/2	0.90
AF106	0.50
AF114	1.95
AF115	2.95
AF116	2.95
AF117	2.95
AF121	0.60
AF124	0.65
AF125	0.35
AF126	0.32
AF127	0.65
AF139	0.40
AF150	0.60
AF178	1.95
AF239	0.42
AFZ12	3.75
ASY27	0.85
AU106	4.50
AU107	3.50
AU110	3.50
AU113	4.50
BC107A	0.11
BC107B	0.11
BC108	0.10
BC108A	0.11
BC108B	0.12
BC109	0.10
BC109B	0.12
BC109C	0.12
BC114	0.11
BC116A	0.15
BC117	0.19
BC119	0.24
BC125	0.25
BC139	0.20
BC140	0.31
BC141	0.25
BC142	0.21
BC143	0.24
BC147A	0.12
BC147B	0.12
BC148A	0.09
BC148B	0.09
BC149	0.09
BC157	0.12
BC158	0.09
BC159	0.09
BC174	0.09
BC174A	0.09
BC177	0.15
BC178	0.15
BC182	0.10
BC182LB	0.10
BC183	0.10
BC183L	0.09
BC184LB	0.09
BC204	0.10
BC207B	0.13
BC208B	0.13
BC212	0.09
BC212L	0.09
BC212LA	0.09
BC213	0.09
BC213L	0.09
BC214	0.09
BC214C	0.09
BC214L	0.09
BC237B	0.09
BC238	0.09
BC239	0.12
BC251A	0.12
BC252A	0.15
BC258	0.25
BC258A	0.39
BC284	0.30
BC300	0.30
BC301	0.30
BC303	0.26
BC307B	0.09
BC327	0.10
BC328	0.10
BC337	0.10
BC338	0.09
BC347A	0.13
BC461	0.35
BC478	0.20
BC527	0.20
BC547	0.10
BC548	0.10
BC549A	0.10
BC550	0.14
BC557	0.08
BC557B	0.80
BC558	0.10
BCY33A	1.60
BD115	0.30
BD124P	0.59
BD131	0.42
BD132	0.42
BD133	0.40
BD135	0.30
BD136	0.30
BD137	0.32
BD138	0.30
BD139	0.32
BD140	0.30
BD144	1.10
BD150C	0.29
BD159	0.65
BD160	1.50
BD166	0.55
BD179	0.72
BD182	0.70
BD183	0.70
BD201	0.83
BD202	0.65
BD203	0.78
BD204	0.70
BD222	0.46
BD223	0.59
BD225	0.46
BD232	0.35
BD233	0.35
BD234	0.35
BD236	0.49
BD237	0.40
BD238	0.40
BD242	0.65
BD246	0.75
BD376	0.32
BD410	0.65
BD434	0.65
BD437	0.75
BD438	0.75
BD520	0.65
BD538	0.65
BD597	0.95
BD589	0.45
BD701	1.25
BD702	1.25
BD707	0.90
8DX32	1.50
BF115	0.35
BF119	0.35
BF119	0.65
BF127	0.39
BF154	0.20
BF158	0.22
BF160	0.27
BF167	0.27
BF173	0.22
BF177	0.38
BF178	0.26
BF179	0.34
BF180	0.29
BF181	0.29
BF182	0.29
BF183	0.29
BF184	0.28
BF185	0.28
BF194	0.11
BF195	0.11
BF196	0.11
BF197	0.11
BF198	0.16
BF199	0.14
BF200	0.40
BF241	0.15
BF245	0.30
BF257	0.28
BF258	0.28
BF259	0.28
BF271	0.26
BF273	0.18
BF336	0.34
BF337	0.29
BF338	0.32
BF355	0.37
BF362	0.38
BF363	0.65
BF371	0.25
BF394	0.19
BF422	0.32
BF457	0.32
BF458	0.36
BF459	0.36
BF467	0.68
BF494	0.45
BF495	0.45
BF595	0.23
BF597	0.25
BFR39	0.23
BFR40	0.23
BFR81	0.25
BFR8B	0.30
BFR90	1.50
BFR91	1.75
BFT42	0.35
BFT43	0.35
BFW92	0.85
BFX29	0.30
BFX84	0.26
BFX85	0.32
BFX86	0.30
BFX88	0.25
BFY50	0.21
BFY51	0.21
BFY52	0.25
BFY90	0.77
BLY48	1.75
BRY39	0.45
BR100	0.26
BR110	0.49
BR103	0.55
BRC4443	1.15
BT100A/02	0.85
BT106	1.49
BT116	1.20
BT119	3.15
BT120	1.65
BU105	1.95
BU108	1.69
BU124	1.25
BU125	1.25
BU126	1.60
BU204	1.55
BU205	1.30
BU208	1.39
BU208A	1.52
BU208D	1.85
BU3276	1.20
BU407	1.24
BU500	2.25
BU508A	1.95
BU526	1.90
BU80Y	2.25
BUY69B	1.70
MJ3000	1.98
MJE340	0.40
MJE520	0.48
MPSA13	0.29
MPSA92	0.30
MRF237	4.95
MRF450A	13.95
MRF453	17.50
MRF454	26.50
MRF455	17.50
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MRF477	10.00
MRF838	13.95
OC16W	2.50
OC23	1.50
OC28	1.50
OC29	2.25
OC32	2.25
OC42	0.75
OC44	0.75
OC45	0.55
OC70	0.45
OC71	0.55
OC72	0.85
OC75	0.95
OC81	0.50
OC171	3.50
R2008B	1.45
R2010B	1.45
R2322	0.58
R2323	0.66
R2540	2.48
HCA16334	0.90
RCA16335	0.80
SKE5F	1.45
TIP29	0.40
TIP29C	0.42
TIP30C	0.43
TIP31C	0.55
TIP32C	0.42
TIP33C	0.95
TIP34B	0.95
TIP41A	0.45
TIP41C	0.45
TIP42C	0.47
TIP47	0.65
TIP120	0.60
TIP125	0.65
TIP142	1.75
TIP161	2.95
TIP2955	0.85
TIP3055	0.55
TIS91	0.20
TV106/2	1.50
2N1308	1.35
2N2219	0.28
2N2222	0.29
2N2905	0.40
2N3053	0.40
2N3054	0.59
2N3055	0.52
2N3702	0.12
2N3703	0.12
2N3704	0.12
2N3705	0.20
2N3706	0.12
2M3708	0.12
2N3733	9.50
2N3773	2.75
2N3792	1.35
2N4427	1.95
2N4444	1.15
2N5294	0.42
2N5296	0.48
2N5298	0.60
2N5485	0.45
2N5496	0.95
2SA715	0.60
2SC495	0.80
2SC496	0.80
2SC1096	0.80
2SC1106	2.50
2SC1172Y	2.20
2SC1173	1.15
2SC1306	1.40
2SC1307	1.75
2SC1364	0.50
2SC1449	0.80
2SC1678	1.25
2SC1909	1.25
2SC1945	2.65
2SC1954	0.95
2SC1957	0.80
2SC1969	1.95
2SC2028	1.15
2SC2029	1.95
2SC2078	1.45
2SC2091	0.85
2SC2098	2.95
2SC2166	1.95
2SC2314	0.80
2SC2371	0.36
2SD234	0.50
3N211	2.95
3SK88	0.95
3SK88	0.95

DIODES

AA119	0.80
BA115	0.13
BA145	0.16
BA148	0.17
BA154	0.06
BA156	0.15
BA157	0.30
BAX13	0.04
BAX16	0.06
BB105B	0.30
BT151	0.79
BY126	0.10
BY127	0.11
8Y133	0.15
BY164	0.45
BY176	1.20
BY179	0.63
BT182	0.55
BY184	0.35
BY199	0.40
BY206	0.14
BY208-800	0.33
BY210-800	0.33
BY223	0.90
BY298-400	0.22
BY299-800	0.22
BYX10	0.20
BYX36-150R	0.20
BYX38-600R	0.60
BXY55-600	0.30
BYX71-600	1.10
BZY95C30	0.35
CS4B	4.50
CS10B	8.45
OA47	0.09
OA90	0.05
OA91	0.06
OA95	0.06
OA202	0.10
IN21DR	5.00
IN23B	5.00
IN23C	5.00
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IN4001	0.04
IN4003	0.04
IN4004	0.05
IN4005	0.05
IN4007	0.06
IN4148	0.02
IN4448	0.10
IN5401	0.12
IN5402	0.14
IN5403	0.12
IN5406	0.13
IN5407	0.16
IN5408	0.16
ITT44	0.04
ITT923	0.15
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BZX61 Series	0.15
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D14-173GM	53.00
D14-173GR	55.00
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D14-181GJ	55.00
D14-181GM	53.00
D14-181GM50	59.00
D14-182GH	59.00
D14-200BE	89.00
D14-200GA/50	85.00
D14-200GM	75.00
D14-210GH	75.00
D14-270GH/50	75.00
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D16-100GH/65	69.00
D16-100GH/67	65.00
D16-100GH/79	69.00
D16-100GH97	65.00
D18-160GH	69.00
D21-10GH	65.00
DG7-5	55.00
DB7.6	35.00
DB7.36	55.00
DG7.32	45.00
DG13.2	45.00
DH3-91	55.00
DH7.91	45.00
DP7.5	35.00
DP7.6	35.00
DN13.78	35.00
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F16-101LD	75.00
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F21-130LC	75.00
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M23-110GH	55.00
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M24-121GH	55.00
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M31-184W	65.00
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M31-184P31	65.00
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M31-270GY	65.00
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M36-170LG	75.00
M38-101GH	65.00
M38-103GR	65.00
M38-120W	65.00
M38-120WA	65.00
M38-121GHR	65.00
M38-121LA	65.00
M38-122GW	65.00
M38-140LA	65.00
M38-142LA	65.00
M38-341P31	65.00
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M40-120W	59.00
M43-12LG/01	65.00
M44-120LC	65.00
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M50-120GR	65.00
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S6AB	45.00
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DET23	35.00
DET24	39.00
DET25	22.00
DEt29	32.00
DF91	0.70
DF92	0.60
DF96	0.65
DF97	1.00
DH63	1.20
DH77	0.90
DH79	0.56
DH149	2.00
DK91	0.90
DK92	1.20
DL35	2.50
DL63	1.00
DL70	2.50
DL73	1.50
DL92	0.95
DL93	1.10
DL94	2.50
DL96	2.50
DLS10	13.50
DLS16	10.00
DM70	1.95
DM160	2.75
DY51	1.50
DY86/87	0.65
DY802	0.72
E80L	29.50
E81L	12.00
E82CC	3.50
E83CC	3.50
E83F	5.50
E86C	9.50
E88C	7.95
E88CC	3.50
E88CC Siemens Special	5.95
E90CC	7.95
E90F	7.95
E91H	4.50
E92CC	3.95
E99F	6.99
E130L	25.00
E182CC	9.00
E180F	6.50
E186F	8.50
E188CC	7.50
E1T	15.00
E280F	19.50
E283CC	10.00
E288CC	13.50
E810F	25.00
E1148	1.00
E1524	6.95
EA50	1.00
EA76	1.95
EA79	1.95
EABC80	0.70
EAC91	2.50
EAF42	1.20
EAF801	2.00
EB34	1.50
EB41	3.95
EB91	0.85
EBC33	2.50
EBC41	1.95
EBC81	1.50
EBC90	0.90
EBC91	0.90
EBF80	0.95
EBF83	0.95
EBF85	0.95
EBF89	0.70
EBF93	0.95
EBL1	2.50
EBL21	2.00
EC52	0.75
EC70	1.75
EC80	9.50
EC81	7.95
EC86	1.00
EC88	1.00
EC90	1.10
EC91	5.50
EC92	1.95
EC93	1.50
EC95	7.00
EC97	1.10
EC8010	12.00
ECC32	3.50
ECC33	3.50
ECC35	3.50
ECC81	1.15
ECC81 Special Quality	1.95
ECC82	0.65
ECC82 Philips	1.95
ECC83	0.65
ECC83 Brimar	1.35
ECC83 Philips	1.95
ECC83 Siemans	2.50
ECC83 Tungsram	1.50
ECC84	0.50
ECC85	0.75
ECC86	2.75
ECC88	0.95
ECC91	2.00
ECC180	0.72
ECC189	1.95
ECC801S	3.50
ECC803S	4.95
ECC804	0.60
ECC2000	12.00
ECF80	1.15
ECF82	1.15
ECF86	1.70
ECF200	1.85
ECF202	1.85
ECF801	0.85
ECF805	2.50
ECF806	10.25
ECH3	2.50
ECH4	3.00
ECH35	3.50
ECH42	1.00
ECH81	0.65
ECH83	0.78
ECH84	0.69
ECH2000	1.50
ECL80	0.60
ECL82	0.65
ECL83	2.50
ECL84	0.74
ECL85	0.69
ECL86	0.80
ECL805	0.69
EF37A	2.00
EF39	1.10
EF40	4.50
EF41	3.50
EF42	3.50
EF50	2.50
EF55	4.95
EF70	1.20
EF71	1.50
EF72	1.20
EF73	1.00
EF80	0.55
EF83	3.95
EF85	0.50
EF86	2.25
EF86 Mullard	4.50
EF89	1.50
EF91	1.95
EF92	2.15
EF93	0.95
EF94	0.85
EF95	1.50
EF97	0.90
EF98	0.90
EF183	0.65
EF184	0.65
EF730	1.80
EF731	3.50
EF732	3.50
EF800	11.00
EF804S	11.50
EF805S	13.50
EF806S	14.50
EF812	0.65
EFL200	1.50
EH90	0.72
EK90	0.95
EL32	0.95
EL33	4.00
EL34	2.25
EL34 Mullard/Philips	4.50
EL36	1.95
EL37	9.00
EL38	4.75
EL41	3.50
EL42	2.00
EL81	6.95
EL83	5.95
EL84 Mullard	2.95
EL85	4.50
EL86	0.85
EL90	1.75
EL91	6.00
EL95	1.75
EL153	12.15
EL183E	3.50
EL18P	3.50
EL360	6.75
EL500	1.40
EL504	1.40
EL509	5.25
EL519	6.95
EL802	3.65
EL821	8.50
EL822	12.95
EM1	9.00
EM4	9.00
EM80	0.70
EM81	0.70
EM84	1.65
EM85	3.95
EM87	2.50
EN32	15.00
EN91	1.50
EN92	4.50
EY51	0.80
EY81	2.35
EY83	1.50
EY84	5.95
EY86/87	0.50
EY88	0.55
EY91	5.50
EY500A	2.50
EY802	0.70
EX35	0.75
EZ40	2.75
EZ41	2.75
EZ80	0.75
EZ81	0.75
EZ90	1.50
F606	2.95
FW4/800	2.95
G55/1K	9.00
G180/2M	6.95
G240/2D	9.00
GC10B	17.50
GC10D	17.50
GC10/4B	17.50
GC10/4E	17.50
GC12/4B	17.50
GD86W	6.00
GDT120M	5.00
GN4	6.00
GN10	15.00
GR10G	4.00
GS10C	16.50
GS10H	12.00
GS12D	12.00
GT1C	14.00
GT1C S/S	13.00
GTE175M	8.00
GTR150W	1.00
GU20	35.00
GU50	17.50
GXU1	13.50
GXU3	24.00
GXU50SS	14.50
GY501	1.20
GY802	1.00
GZ30	1.00
GZ31	1.00
GZ32	1.00
GZ33	4.50
GZ34	2.15
GZ37	4.50
HAA91	1.00
HABC80	0.90
HBC90	0.75
HBC91	0.80
HF93	0.75
HF94	1.50
HK90	1.05
HL2K	4.95
HL23DD	4.00
HL41	3.50
HL42DD	3.50
HL90	0.70
HL92	1.50
HL133×DD	3.50
HT2	4.00
HY90	1.00
HVR2	3.00
JP9-7A	60.00
K311B	85.00
KR6/3	45.00
KT8C	7.00
KT33C	3.50
KT36	2.00
KT44	4.00
KT45	4.00
KT61	4.00
KT63	2.00
KT66 OSRAM	15.00
KT66 USA	9.95
KT66 GEC	14.95
KT 77 Gold Lion	10.95
KT81	7.00
KT88 USA	10.95
KT88 G Lion	18.95
KT67	9.00
KTGW61	2.50
KTW62	2.50
KTW63	2.00
KTZ63	2.50
L102/2K	6.95
L120/2K	12.00
LB7-20	95.00
LS9B	6.95
M502A	60.00
M537A	60.00
M5143	155.00
M8079	6.00
M8082	7.50
M8083	3.25
M8091	7.50
M8096	3.00
M8098	5.50
M8099	5.00
M8100	5.50
M8136	7.00
M8137	7.95
M8161	6.50
M8162	5.50
M8163	5.50
M8190	4.50
MB195	6.50
M8196	5.50
M8204	5.50
M8223	4.50
M8224	2.00
M8225	3.95
ME1401	29.50
ME1402	29.50
ME1501	14.00
MH4	3.50
MHL6	4.00
ML4	4.50
MS4B	5.50
MU14	3.50
MZ1-100	125.00
N37	12.50
N78	9.85
OA2	0.85
OA2WA	2.50
OA3	2.50
OB2	0.85
OB2WA	2.50
OC2	2.50
OC3	1.50
OD3	1.70
OM4	1.00
OM5B	3.00
OM6	1.75
ORP43	2.50
ORP50	3.95
P61	2.50
P41	2.50
PABC80	0.50
PC86	0.75
PC88	0.75
PC92	3.50
PC97	1.10
PC800	1.10
PC900	1.25
PCC84	0.40
PCC85	0.54
PCC8B	0.70
PCC89	0.70
PCC189	0.70
PCC805	0.70
PCC806	0.80
PCE82	0.80
PCF80	0.65
PCF82	0.60
PCF84	0.65
PCF86	1.20
PCF87	0.40
PCF200	1.80
PCF201	1.80
PCF800	0.40
PCF801	1.35
PCF802	0.60
PCF805	1.25
PCF806	1.00
PCF808	1.25
PCH200	1.50
PCL82	0.85
PCL83	2.50
PCL84	0.75
PCL85	0.80
PCL86	0.85
PCL800	0.80
PCL805	0.90
PD500	3.50
PD510	3.65
PE1-100	69.00
PEN25	2.00
PEN40DD	2.50
PEN45	3.00
PEN45DD	3.00
PNE46	2.00
PE06-4oN	42.00
PFL200	0.95
PL21	2.50
PL36	0.95
PL38	1.50
PL81	0.72
PL81A	0.72
PL82	0.60
PL83	0.52
PL84	0.78
PL88	1.00
PL95	1.75
PL302	1.00
PL345	12.50
PL500	1.10
PL504	1.15
PL508	1.75
PL509	4.85
PL519	4.95
PL802T	3.50
PL820	2.95
PL5557	29.50
PY32	0.60
PY33	0.50
PY81	0.70
PY82	o.70
PY83	0.70
PY88	0.65
PY500A	1.95
PY800	0.79
PY801	0.79
QB3-300	54.95
QB3-1750	139.50
QB5-3500	495.00
QE03-10	4.95
QE08-200	145.00
QF40	65.00
QP25	1.00
QQE02-5	19.50
QQE03-12	7.95
QE03-20	35.00
QQE06-40	45.00
QQV02-6	19.50
QQV03-10	5.50
QQV03-10 Mullard	15.00
QQV03-20	...............25.00
QQV03-20B	32.00
QQV06-40A	27.50
QQV06-40A Mullard	45.00
QQV07-50	63.50
QQZ03-20	42.50
QS75/20	1.50
QS75/40	3.00
QS92/10	5.00
QS95/10	4.85
QS108/45	4.00
QS150/15	6.95
QS150/30	1.15
QS150/45	7.00
QS1200	3.95
QS1202	3.95
QS1203	4.15
QS1205	3.95
QS1206	1.05
QS1207	0.90
QS1208	0.90
QS1209	3.15
QS1210	1.50
QS1211	1.50
QS1212	3.20
QS1213	5.00
QS1215	2.10
QS1218	5.00
QU37	9.50
QV03-12	5.75
QV05-25	1.75
QV06-20	29.50
QV08-100	145.00
QV2-2500	45.00
QY3-125	65.00
QY4-250	70.00
QY4-400	76.00
R10	4.00
R16	12.00
R17	1.50
R18	2.50
R19	2.50
R20	1.20
R1169	55.00
RG1-125	4.95
RG1-240A	14.50
RG3-250A	3.50
RG3-1250A	35.00
RK2K25	62.50
RK-20A	12.00
RL16	1.50
RPL16	12.00
RPY13	2.50
RPY43	2.50
RPY82	2.50
RR3-250	15.00
RR3-1250	35.00
RS613	45.00
RS685	54.95
RSS688	52.15
S6F17	5.95
S6F33	28.95
S11E12	38.00
A30/2K	12.00
S104/1K	10.00
S109/1K	15.00
S130	5.59
S130P	5.95
SC1/800	5.00
SC1/1100	6.00
SC1/1200	5.00
SC1/1300	6.00
SC1/200	9.00
SP41	5.00
SP42	3.00
SP4B	4.95
SS501	35.00
ST11	1.50
STV280/40	11.95
STV280/80	19.95
SU42	4.95
TB2.5/300	85.00
TB2-300	45.00
TB3-2000	395.00
TBL-2-300	275.00
TD1-100A	25.00
TD03-10F	35.00
TD3-12	4.00
TDD4	5.50
TP25	1.50
TSP4	7.00
TT11	1.50
TT21	45.00
TT22	45.00
TT100	57.00
TTR-31MR	65.00
TY2-125A	85.00
TY4.400	85.00
TY8-600W	365.00
TYS2/250	375.00
U18-20	2.75
U19	11.95
U24	2.00
U25	0.90
U26	0.90
U37	9.00
U41	6.95
U50	2.00
U82	3.00
U191	0.70
U192	1.00
U193	0.65
U251	1.00
U801	0.75
UA8C80	0.65
UAF42	1.00
UBF80	0.60
UBC41	2.95
UBC81	1.50
UBF89	0.60
UBL21	1.75
UC92	1.20
UCC84	0.70
UCC85	0.60
UCF80	1.00
UCH21	1.20
UCH41	2.50
UCH42	2.50
UCH81	0.65
UCL82	1.75
UCL83	2.50
UF41	1.15
UF42	1.15
UF80	1.75
UF85	1.20
UF89	2.50
UL44	3.50
UL85	0.85
UU5	3.50
UU7	8.00
UU8	9.00
UY41	3.50
UY85	0.70
V235A/1K	250.00
V238A/1K	295.00
V240C/1K	225.00
V241C/1K	195.00
V339	3.50
V453	12.00
VLS631	10.95
VP4B	4.50
VP133	2.00
VR75/30	3.00
VR101	2.00
V105/30	1.50
VR150/30	1.15
VT52	2.50
VU29	4.50
VU39	1.50
W21	4.50
W77	5.00
W729	1.00
W739	1.50
X24	4.50
X66/X65	4.95
X76M	1.95
XC24	1.50
XC25	0.50
XFW47	1.50
XFW50	1.50
XG2-6400	135.00
XG5-500	22.50
XI1-5V	1.50
XL628FT	7.50
XNP12	2.50
XR1-1600A	49.50
XR1-3200A	79.50
XR1-6400A	99.50
Y502	25.00
Y65	6.95
YD1100	75.00
YJ1060	265.00
YL1020	29.00
YL1070	195.00
YL1071	195.00
YL1290	65.00
Z77	1.20
Z302C	12.00
Z359	9.00
Z505S	15.00
Z520M	4.00
Z521M	8.00
Z700U	3.00
Z749	0.60
Z759	19.85
Z800U	3.00
Z803U	18.95
ZA1000	12.50
ZA1001	1.50
ZA1002	1.50
ZC1040	8.00
ZM1005	8.00
ZM1021	8.00
ZM1023	7.95
ZM1041	14.00
ZM1082	9.00
ZM1084	10.00
ZM1177	9.00
ZM1202	55.00
ZM1263	4.00
ZM1612	3.00
1A3	4.50
1AC6	1.20
1AE4	3.50
1B3GT	1.95
1B22	10.00
1B24	14.95
1B27	55.00
1B35A	29.50
1C1	2.50
1C5GT	2.50
1FD1	2.50
1G3GT	2.50
1J3GT	2.50
1N2	4.50
1N5GT	2.50
1P28	25.00
1R5	0.90
1T4	0.70
1U4	1.75
1U5	1.00
1X2B	1.40
1Z2	8.95
2AS15A	11.50
2B7	1.50
2B22	69.50
2C39A	32.50
2C39BA	39.50
2C40	37.00
2C42	29.50
2C51	0.75
2CY5	1.50
2D21	1.50
2D21W	2.50
2E22	49.00
2E26	7.95
2J42	93.00
2J55	350.00
2K25	27.50
2K25 Raytheon	75.00
2K26	95.00
2K29	250.00
2K48	140.00
2K56	250.00
3A5	4.50
3A/107B	12.00
3A/108A	9.00
3A/109B	11.00
3A/110B	12.00
3A/141K	11.50
3A/147J	7.50
3A/167M	10.00
3A2	3.95
3A3A	3.95
3A4	1.10
3AL5	0.95
3AT2	3.35
3B2	3.00
3B4	7.00
3B7	4.50
3B24	10.00
3B26	24.00
3B28	12.00
3BZ6	1.50
3C4	1.00
3C23	19.00
3C45	24.00
3CB6	1.50
3CN3A	2.50
3CS6	0.95
3CX3	2.50
3CY5	1.50
3D6	4.50
3D21A	29.50
3E22	49.50
3E39	39.50
3EH7	1.95
3EJ7	1.95
3V4	2.50
3W4GT	2.50
4B551B	115.00
4-65A	59.00
4687A	9.50
4-125A	72.50
4-250A	79.50
4-400A	87.50
4-1000A	425.00
4B32	35.00
4BQ7A	1.75
4BZ6	1.95
4C27	25.00
4C28	25.00
4C35	145.00
4CB6	1.95
4CX1000A	425.00
4CX4000A	1100.00
4CX250B	49.00
4CX250B	
4D32	125.00
EIMAC	59.50
4CX250BM	75.00
4CX250K EIMAC	95.00
4CX125C EIMAC	125.00
4CX350A	95.00
4CX350F	79.50
4XC1500B	398.50
4GS7	2.25
4GV7	2.25
4J52	75.00
4JC6A	2.95
4X150A	35.00
5A/102D	9.50
5A152M	9.00
5A163K	10.00
5A170K	6.25
5A-180M	9.00
5A-206K	10.00
5AMB	2.15
5ANB	1.20
5AR4	2.00
5AU4	1.50
5B.110M	10.00
5B-254M	14.50
5B-255M	19.50
5B-256M	9.00
5B-257M	9.00
58-258M	14.50
5C22	125.00
5J180E	2500.00
5R4GB	3.50
5R4GY	3.50
5T4	5.95
5U4G	2.50
5U4GB	2.50
5V4G	1.25
5Y3GT	1.95
5Z4GT	0.85
6/30L2	0.70
6A/203K	9.00
6A7	4.95
6A8G	1.50
6AC7	2.00
6AF4A	2.50
6AG5	1.50
6AG7	1.95
6AH6	2.50
6AJ4	2.00
6AJ7	2.00
6AK5	1.50
6AK6	2.50
6AL5	0.60
6AM4	3.25
6AM5	6.00
6AM6	1.50
6AN5	2.65
6AN8A	2.65
6AQ5	1.75
6AQ8	0.85
6AR5	5.95
6AR8	3.95
6AS5	1.50
6AS6	2.50
6AS7G	4.50
6AT6	0.75
6AT8	1.75
6AU4	2.00
6AU5GT	4.50
6AU6	0.95
6AV6	0.75
6AW8A	2.50
6AX4GT	1.95
6AY3B	1.95
6AZ8	5.95
6B7	2.80
6B8G	1.50
6B10	1.95
6BA6	0.95
6BA7	4.50
6BA8A	3.50
6BC8	1.00
6BD4	1.50
6BD6	2.50
6BE6	0.72
6BG6G	3.00
6BH6	1.95
6BH8	1.50
6BJ6	1.20
6BK4	4.00
6BK7A	1.95
6BL6	195.00
6BL8	1.15
6BM8	0.58
6BM6	155.00
6BN4	1.65
6BN6	1.65
6BN7	4.50
68N8	3.95
6BQ5	0.75
6BQ5	0.75
6BQ7A	0.72
6BL7GTA	3.95
6BR5	0.70
6BR7	4.95
6BR8	2.15
6BR8A	2.15
6BS7	5.50
6BW4	1.50
6BW6	5.35
6BW7	1.50
6BW8	4.00
6BX6	0.48
6BX7GT	3.50
6BZ6	2.50
6BZ7	2.95
6C4	1.10
6C5	1.95
6C6	2.50
6C8G	1.50
6C11	2.50
6C18	2.50
6CA4	4.95
6CA7	3.50
6CB5	3.95
6CB6	1.95
6CD6GA	4.50
6CF6	1.50
6CG7	2.25
6CH6	6.95
6CL3	3.95
6CL6	3.25
6CL8A	1.50
6CM5	1.60
6CM7	2.95
6CS6	0.75
6CW4	6.50
6CY5	1.00
6D6	2.50
6DC6	2.35
6DJ8	0.95
6DK6	1.15
6DQ5	5.95
6DQ6B	2.50
6DT6A	1.50
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6EV7	2.95
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6F5	4.95
6F6	2.50
6F6G	2.00
6F7	5.50
6F12	1.50
6F13	3.00
6F14	1.00
6F17	2.75
6F21	2.50
6F23	0.60
6F24	1.25
6F25	1.25
6F28	1.25
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gGE5	3.95
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6GK5	1.50
6GK6	1.95
6GS7	2.15
6GV7	2.50
6GW6	2.50
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6H1	9.50
6H3N	1.10
6H6	1.95
6H6GT	1.95
6HF5	5.50
6HF8	2.50
6HS6	4.95
6J4	2.15
6J4WA	3.15
6J5	2.50
6J6	2.00
6J7	4.15
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6JU8	2.50
6JS6C	4.95
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6P25	4.00
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8SK7	1.35
6SK7GT	1.35
6SL7GT	0.85
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7SQ7	1.35
6SS7	1.95
6U4GT	1.75
6U6WA	3.50
6U8	1.15
6U8A	1.50
6V6G	1.25
6V6GT	1.50
6VGG	1.00
6X2N	1.00
6X4	1.50
6X5GT	1.00
6X5GTY	1.00
6XBB	2.25
7A6	4.50
7A7	2.00
7AD7	1.75
7B6	3.50
7B7	2.50
7C5	3.50
7C6	2.50
7E7	2.50
7H7	3.50
7AU7	1.50
7J7	5.50
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6080WA	9.50
6132	10.00
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6156	65.00
6157	2.50
6158	3.20
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CIRCLE 44 FOR FURTHER DETAILS.

Digital audio editing — 2

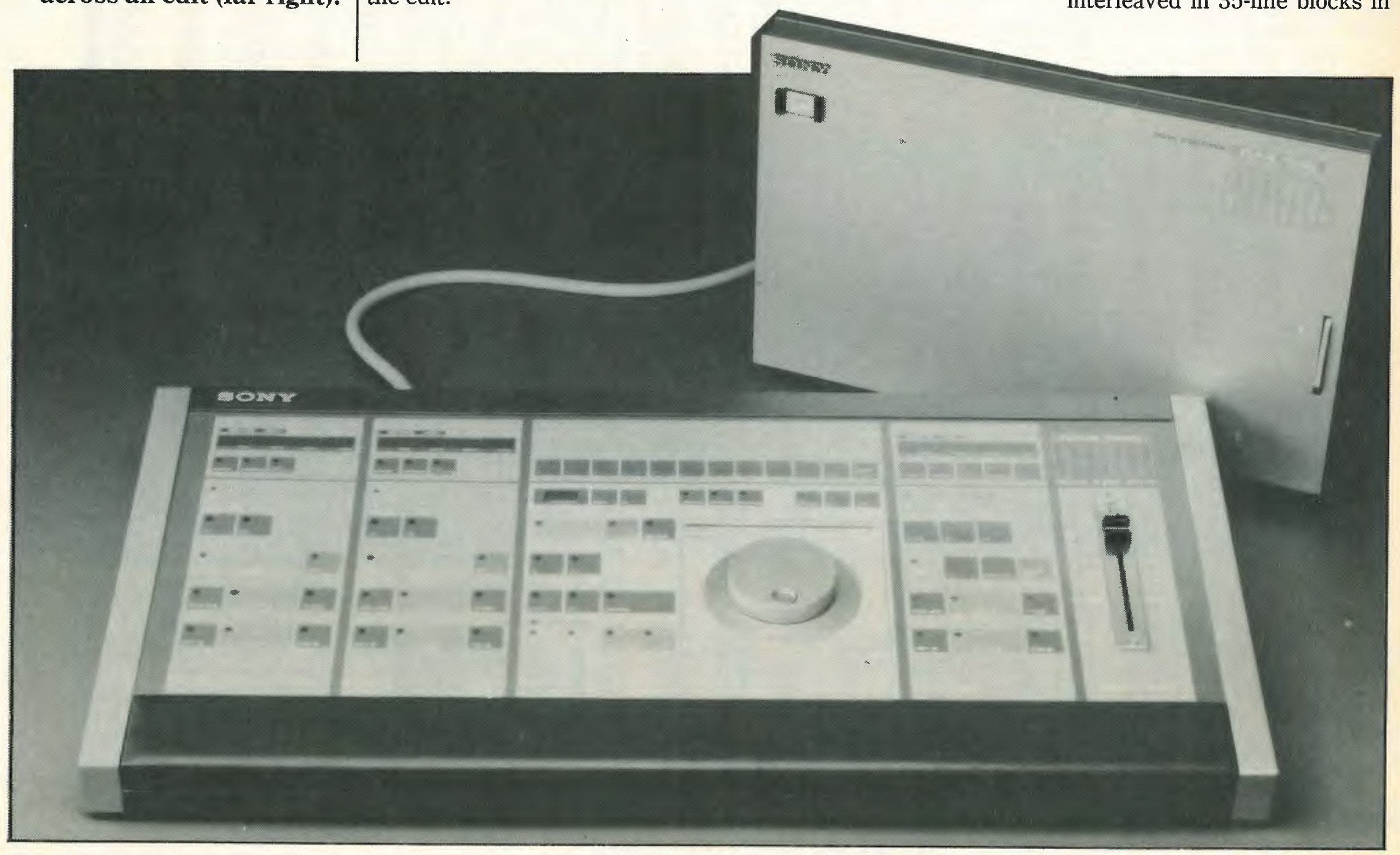
by John Watkinson

Penultimate article in this series outlines the mechanisms needed to assemble edits

Samples representing the waveform of audio signals are carried within a video-like waveform by the v.c.rs in the mastering system. Unlike real video signal, which is broken up into frames and will be edited at frame boundaries, the audio samples represent a continuous signal and it must be possible to perform an edit at any point within the frame. Fig. 1 shows that when the assemble takes place, the out-point of the old recording and the in-point of the new recording are brought together. It is not possible to record a discontinuous pseudo-video waveform on the v.c.r., so the solution adopted is to move the samples and the sync pulses can be continuous in the area of the edit.

The edit point may have any position within the video frame, but v.c.rs are designed to edit at frame boundaries. Fig. 2 shows that the desired effect may be obtained by setting the v.c.r. into record at a frame boundary, and re-recording what is already on the tape up to the edit point, where the new recording will commence. It is not possible to simply switch between the old and new sample streams, as this could produce an audible click at the edit point. Fig. 3 shows that a cross fade in the digital domain is carried out. Gain control in the digital domain requires a multiplier, which changes the sample values according to the gain coefficient supplied.

A cross fade can be achieved by multiplying the outgoing samples, by decreasing coefficients, and multiplying the incoming samples by increasing coefficients, then summing together the products. The slope of the coefficient generator can be controlled by the operator to determine the speed of the cross fade. To control the relative levels of the assembled recording the operator has a fader which can produce coefficients for a digital gain control stage in the player sample stream prior to the cross fader. As explained in an earlier article, data carried in the pseudo-video waveform are interleaved in 35-line blocks in the 1610 format. There will be an unavoidable delay caused by the interleave process in record, and by the de-interleave process on replay. When the recorder is required to begin at a frame boundary, it is necessary to supply the samples to be recorded in advance so that following the interleave delay, they will have the same timing as the recording. This advance of the samples to be re-recorded can only be achieved by playing back the end of the old recording in advance and storing the samples in a memory. The recorder will need to roll past the edit point twice for each edit, firstly to load the memory, secondly to perform the edit. This has the added advantage that only one p.c.m. adapter is required to decode and de-interleave the new recording because the old recording can be supplied by the memory. As the cross-fade period can be several frames, memory must be large enough to accomodate the old recording until it has completely faded out.



Spill-proof membrane switches on the Sony DAE1100 control panel remotely control the v.c.rs and start the edit sequences. A large rotor finely locates the edit point (centre right) and a digital fader allows matching of levels across an edit (far right).

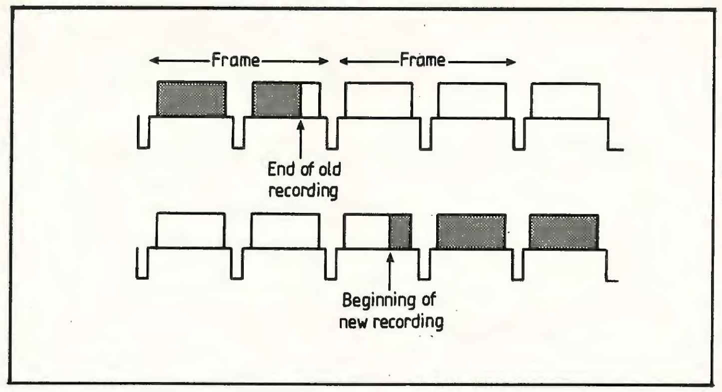


Fig. 1. Artificial frame structure imposed on continuous audio samples by the use of pseudo video cannot be allowed to restrict the time accuracy of edits. It is therefore necessary to slide data along with respect to the frame timing to prevent the potential gap shown here from being formed.

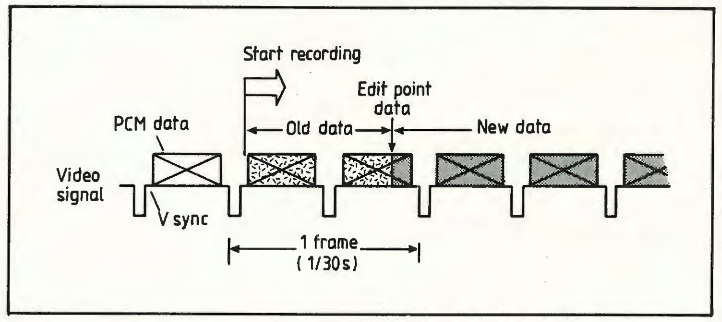


Fig. 2. As a v.c.r. can only begin to record at a frame boundary, an edit is positioned to sub-frame accuracy by re-recording the existing information from the beginning of the frame to the edit point. This old data is stored in memory prior to the edit taking place.

Samples of the new recording need to slip with respect to sync, achieved by using a further area of editor memory as a delay. The delay necessary is not immediately obvious for two reasons. Firstly, the samples from the replay of the new recording will be delayed by the de-interleave process, but they must be supplied in advance by an amount of time equal to the encode delay. Thus the delay needs to be reduced by one encode delay plus one decode delay. Secondly, the low cost industrial v.c.rs used cannot be relied on to accelerate to frame lock at the same rate when they are rolled by the editor. There is a possibility that the recorder and the player will lock up to reference with a one frame time error between them.

To overcome this problem, the editor deliberately rolls the player a few frames ahead of the recorder, and delays the playback samples by the corresponding amount. If the player locks up a frame late with respect to the recorder, the editor can detect the condition by comparing the timecodes from the two v.c.rs, and the delay can be reduced by one frame, or 1470 samples. Alternatively, if the player locks up a frame early, the delay can be increased by the same amount. As a consequence, the delay given to the samples from the player is a function of the relationship of the out-point and the in-point to the frame timing of the two v.c.rs, the encode-decode delay at the p.c.m. adaptor, and the state of lock achieved by the v.c.rs during the pre-roll. The editor's microprocessor takes care of the calculations, which do not concern the operator.

A tremendous asset of electronic editing is that the subjective effect of an edit can be assessed using a simulation without changing the recording on any of the tapes involved. The preview mode is identical to the real edit, with the exception that the recorder fails to record, and the operator can hear what would have been recorded via the d.a.c. in the p.c.m. adaptor. The in-point and out-point can be trimmed and the cross-fade time changed any number of times until the desired result is obtained by repeating the preview.

In the area of edit preview there is a detail difference between the Sony editor and the JVC editor. In the Sony machine, only one area of the recorder out-point is stored, and the editor must roll the player to rehearse an edit, whereas in the JVC unit, the recorder out-point samples and the player in-point samples are stored, and a rehearsal can be carried out from the memory without rolling the tape.

To permit correct monitoring of the rehearsal or at the edit by the d.a.c. in the p.c.m. adaptor, there is an additional complication. During the pre-roll prior to the edit, the p.c.m. adaptor supplies samples from the recorder which are delayed by the de-interleave process. When the samples from the recorder that were previously loaded into the memory are reached, these must be read out with an advance, to overcome the encode delay. To allow continuous monitoring in this transition, the samples from the pre-loaded memory are subjected to a delay equal to one encode delay plus one decode delay, so that they will be time-aligned with the delayed samples from the recorder, even though they are supplied in advance to the encoder. This delay function requires an additional area of memory in the editor. There are thus three main areas of memory required, the pre-loaded recorder data memory, the player timebase corrector memory and the monitor delay memory.

The complete sequence of events in an edit can now be described with reference to Fig.4. The in and out-points are located as per Part 1, and the edit process is enabled by the

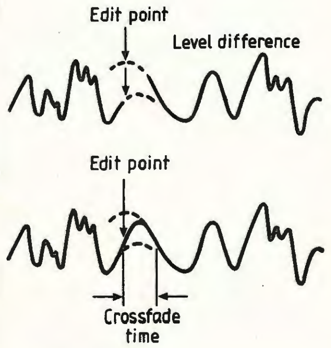


Fig. 3. It is not possible to simply switch between two sample streams because this risks the production of a step waveform. The correct procedure is a short crossfade in the digital domain.

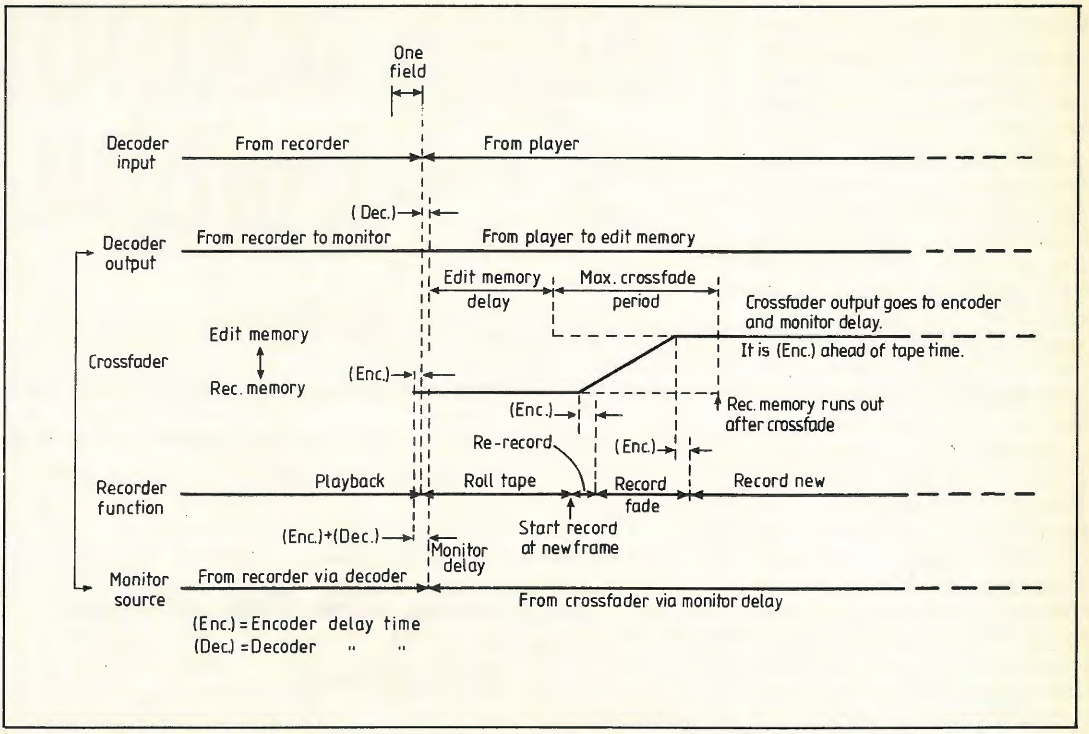


Fig. 4. Timing of an assemble sequence in a digital audio editor. There is only one decoder so this must be handed over from the monitor function of the recorder to the replay function of the recorder to the replay function of the player. The remainder of the recorder data came from the record memory. Crossfade output goes to the encoder which must be supplied one encode period in advance. A monitor delay is necessary so that the advanced crossfader output can be time aligned with the delayed decoder output at the time the monitor switches sources. Edit delay slides the player data along the video timing to close any gaps and compensate for frame slips in machine synchronisation. Edit delay output feeds the crossfader and must also be one encode period ahead of tape time.

operator. The first step is to pre-load the memory with samples from the area of the recorder out-point. The recorder is reversed away from the edit point, and put into play. The editor reads the timecode of the recorder, and at the appropriate point begins to store samples in the memory. There is no audio output from the d.a.c. during this pre-load, which can be disconcerting for the operator if he does not realise what is happening. Following the preload the recorder must again be reversed ahead of the in-point. The editor will then set both recorder and player into play mode, and will read the timecodes of both to establish the relative lock condition. The video multiplexer of the editor will select the video from the recorder, and send it to the decoder in the p.c.m. adaptor. After a decode delay, samples from the p.c.m. adaptor will be returned to the editor, which will route them to the d.a.c. for monitoring. It is necessary to switch over to the pre-loaded memory data prior to the edit point, so that the decoder of the p.c.m. adaptor will be free to decode the video from the player. The pre-loaded memory samples will be read out of the memory in advance by one encode delay period, and sent via the cross fader to the encoder of the p.c.m. adaptor. In addition, the cross-fader output will be delayed by one encode delay plus one decode delay in the monitor delay so that it aligns in time with the samples coming from the recorder during the pre-roll. The d.a.c. will then have its source of samples imperceptibly switched from actual replay of the recorders tape, to replay from the memory.

Once the monitor output is established from the out point memory, the video multiplexer select pseudo-video from the player and sends it to the decoder of the p.c.m. adaptor. One decode delay later the samples are returned to the editor, which must decide how much delay to apply according to the constraints discussed. Following this delay, the replay samples will form the other input to the cross fader via the gain control, although at this time the cross fader is set to pass only samples from the recorder. At this stage, the frame containing the edit point has yet to be reached. The samples from the pre-loaded memory are being sent to the encoder of the p.c.m. adaptor, which will be producing a pseudo-video waveform which goes to the recorder. The recorder, however, is still in play mode. At the beginning of the frame which contains the start of the cross fade, the recorder starts to record, and initially will re-record what is already on the tape. When the cross fade starts the sample stream from the player, which has been suitably delayed, will be 'faded up', and the sample stream from the pre-loaded memory will be faded down. After this the recorder continues to record indefinitely and dubs the player output until stopped by the operator. Further assembles may be performed as necessary until the master tape is complete.

The final article in this series deals with compact disc subcode

Our definitive compact disc series, introduced in January 1985 featured,
- **Principles of optical storage, March 1985 pp 70, 71 April pp 43-46**
- **Channel code and disc format, May on 27, 28, June pp 80-82**
- **Compact disc players, August pp 52-55, November pp 29-33**
- **Compact disc mastering, February 1986, pp 47-50 & 62**
- **Digital audio editing, March pp29-32, April pp 52-54.**

P.c.b. design on the BBC micro

A p.c.b. draughting program which runs on a £500 computer is a remarkable achievement: but Micronova's works on the BBC Micro (any model with more than the 32K ram of the basic model B) and is offered at the attractive price of £149.95. We tested it on a model B fitted with the Watford Electronics 32K ram card, which gives space for about 900 structures to be defined and printed. With a 6502 second processor or one of the newer 128K BBC micros, up to 5000 are possible.

The program allows a maximum board size greater than 600mm square, single or double-sided. On the screen the artwork is displayed in the conventional tape colours of blue and red against a white background.

A series of menus gives access to the main parts of the program, including a utility which allows finished artwork to be created on an Epson dot-matrix printer. Print-outs can be actual size, double or quadruple-size, in normal or mirror-image form. The utility also generates solder-resist patterns for either side of the board.

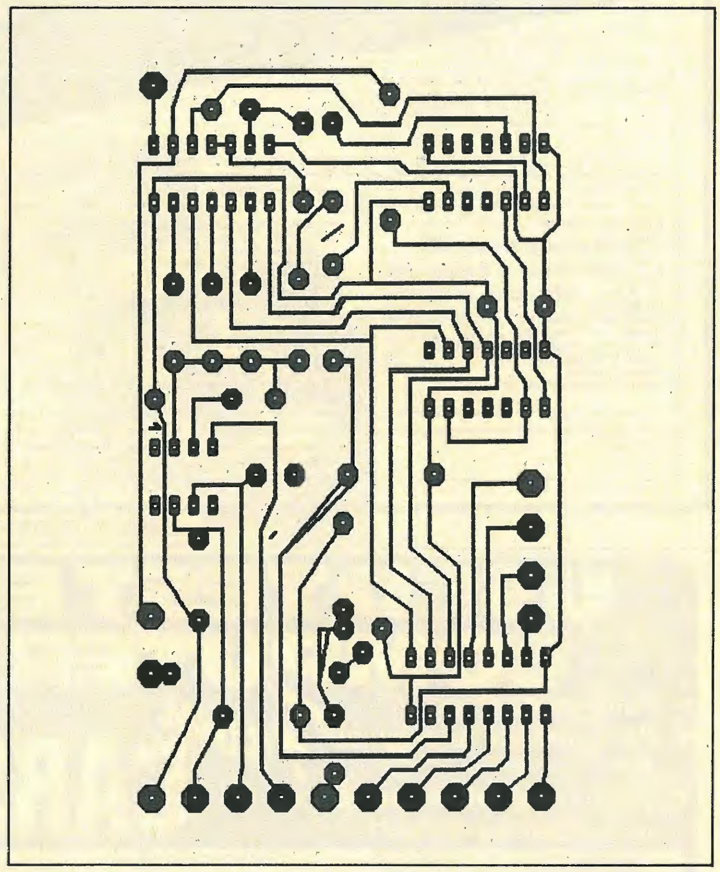
In 'design' mode, the monitor screen acts as a window which the user can move freely about the board. The degree of magnification can be altered in 2:1 steps; six settings are available and at the largest a 16-pin dil device almost fills the screen.

Pads are set on the board by positioning a cross-wire cursor and pressing an appropriate key. There is a choice of five ready-made octagonal pad sizes, but any diameter from 0.03 to 0.99in is possible. In addition, the program offers dual-in-line i.c. patterns with any even number of pins up to 98: again, five of the commonest are ready to use.

Tracks are laid by moving the cursor to the each end of the run and pressing return. On the screen they appear diagrammatically as thin lines, but are definable as any width from 0.01 to 0.99in, in 0.01in increments. The program does not offer automatic routing (which probably calls for a much more powerful computer), but it does have a useful bussing feature which can link corresponding pins of a set of dil packages.

The screen is updated by exclusive-or plotting and so any structure can be erased by re-drawing it on the same spot. However, with misplaced tracks it sometimes took persistence to rediscover their exact start and finish positions.

Each design is stored as a list of coded instructions (which the user can inspect). When a track is to be erased, the program does not delete the original instruction but instead adds another which countermands it. So every time the program replots the display (and his happens on each change of magnification and after each visit to the main menu), the design's entire past life flashes by on the screen. Re-plotting took around 20s to complete with the small design shown here.



This layout took just under 40 minutes to print as a 2:1 enlargement. Very large designs can be printed in sections.

The program is well-provided with traps to protect against user error. Nevertheless, in the course of a long session it proved possible once in a while to defeat the system and to end up with scraps of track which had been erased from the screen but which were still reproduced by the printer utility. Such mistakes could take a long time to detect, since the printer-dump was very slow: it took over half an hour to produce our example.

Many thoughtful touches have been put in by the author: the program remembers all your settings when you reload it, it has an auto-save option to reduce the risk of accidents, it puts a title and scale-marking on print-outs and has a timer which marks the passing hours and gives a warning when memory is nearly full. But if p.c.b. draughting by the pencil and indiarubber method is hard work for you, you're unlikely to find it very much less painful with this program. Once a component has been placed, you cannot re-site it without laboriously erasing and redrawing every structure associated with it. However, you should at least be able to get a tidy result which can be edited easily if anything goes wrong.

The original disc was accompanied by printed labels for two back-ups; no difficulty arose in transferring the program to our Kenda double-density system. A simplified cassette version is also available at £39.95 for the draughting program and £59.95 for the p.c.b. printing program. Prices given do not include v.a.t.

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Disc and cassette versions are available from Farnell Electronic Components; Verospeed stock the disc version only. ■

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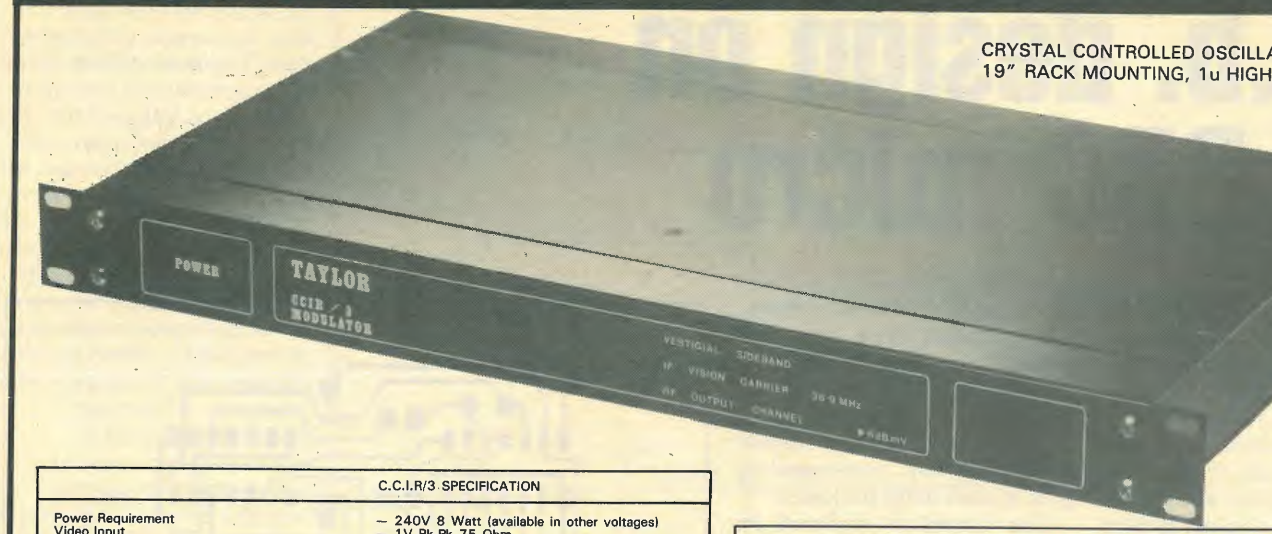

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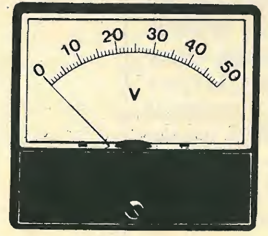

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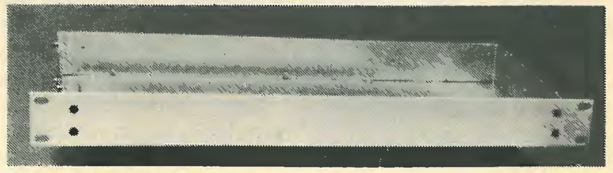

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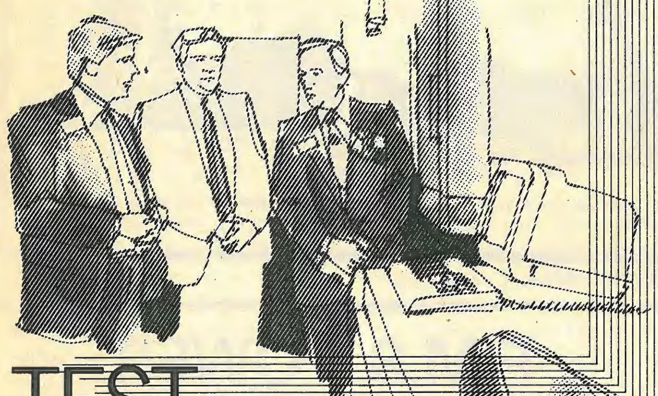

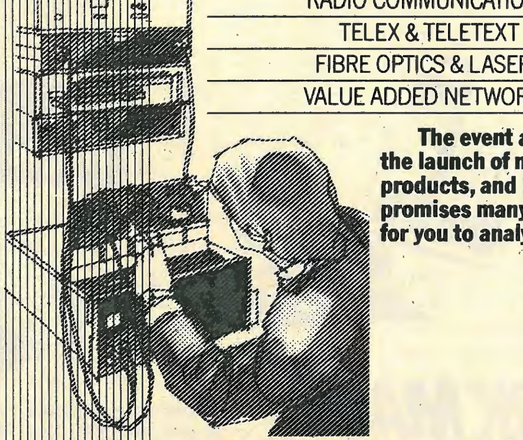

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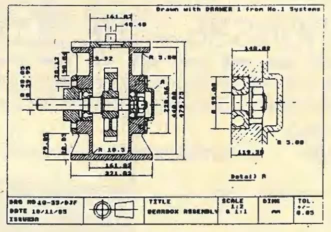

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A look inside: computer aided metallurgy – 2

by L. Paul Goodwin, B.Sc., A.M.I.E.E.

Video processing and computer technology combine to allow automatic analysis of metal crystals

Presentation is a critical part of any computer data display. The data printing format is controlled by the software of the analysis computer and can be designed to suit the needs of a variety of end users. An additional requirement is for the display of the video information forming the source of analysis as well as the final results produced by the computer. This would be easy using two video monitors, but this solution is costly and of limited effectiveness. There are then two alternative ways of showing the two pictures on the same monitor screen at the same time:

- superimpose the text onto the picture of the crystal structure
- split the screen into two parts, one part for the display of the structure and one part for the processing information.

Superimposition is usually not effective on a picture with a high white content, as can be observed by anyone who has watched a badly subtitled film on television. This can be overcome by putting a small border around each letter so that it stands out from the background, but this is a costly solution for only a limited effect.

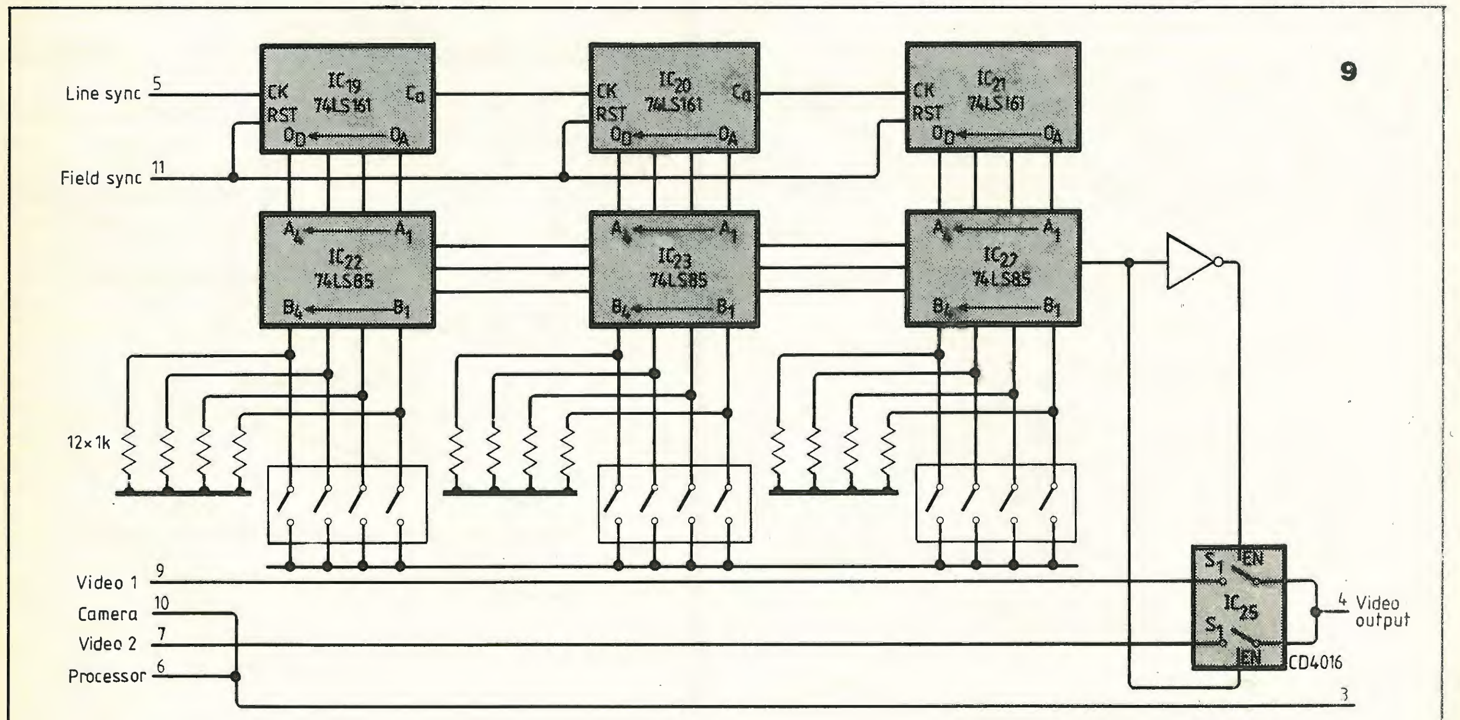
Because the picture of the crystal structure is aesthetic rather than functional, it is quite acceptable for only part of it to be displayed on the screen at any one time. In this case, the bottom of the picture has been given over to the display of data, achieved by video switching between camera and computer outputs. The first solution of total superimposition is easily implemented by the simple analogue mixing of the two video source outputs; quite acceptable as the signals are synchronized.

An interesting effect of the partial superimposition can be achieved by having the computer output displayed full-screen and gating the camera video output. This allows the processing computer a full screen output if any further information display is required, and also allows highlighting of important information by display within the screen area not used by the camera display.

The system was designed with a teaching environment in mind. It would be very useful to ahve this type of split-screen display so that the output could be fed to a lecture-room c.c. tv system for a class of students to witness results.

Split-screen generator

comprises a 12-bit counter (IC 19, 20 & 21) and a 12-bit magnitude comparator (IC 22, 23 & 24). The magnitude comparator is designed to indicate when a certain number of lines per frame have been displayed from source 1 and then to switch to source 2. For the time before the count exceeds the set value (again set by d.i.l. switches on the prototype), S1 on IC25 will be enabled, and the video from the camera will be displayed. After the set value has been reached, S2 on IC25 will be enabled, and the video form the processing system will be displayed.



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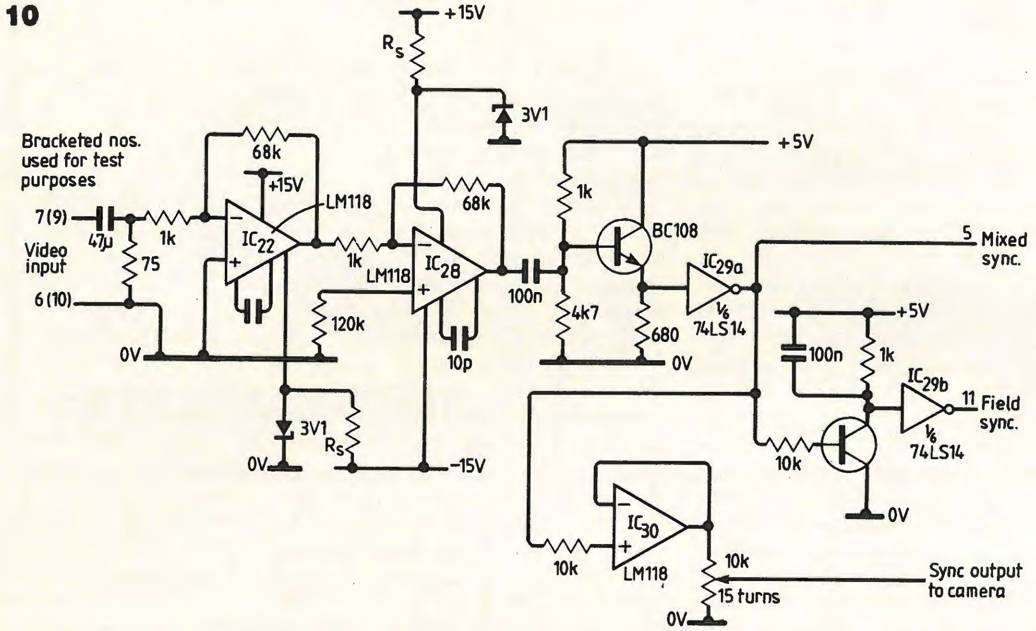
Video sync stripper. As outlined previously it is required to provide the video camera with sync pulses from the processor system video output. The type of camera to be used with the system will dictate the final form of the circuit. It would be acceptable to take the video sync information directly from the camera video output provided that the processor video display generator can be genlocked.

The extraction circuit uses two op-amps driven into clipping. The first inverts the video and also clips part of the signal. Because the device is powered by −3 volts on the negative rail, the video is further clipped. The second op-amp does the same while inverting the output of the first so that the video information is completely removed. The sync pulses are then clamped to 5V to be t.t.l. compatible. The mixed sync output of the circuit is then complete. Field sync pulses are extracted using the RC filter and are cleaned by IC29b.

Video level detector. Designed around a high-speed operational amplifier, circuit has a high enough slew-rate to cope with a 4MHz input signal (for maximum resolution). The levels of 'black' and 'white' will differ from application to application so the threshold voltage of the comparator can be set to any voltage likely to occur in the video signal. Any level above the threshold will be treated as peak white or logic 0 and any level below will be black or logic 1.

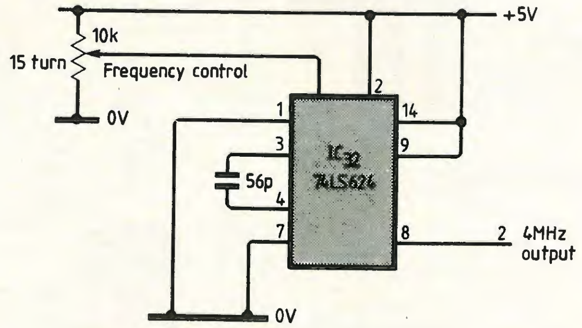
The circuit also registers sync pulses as black level but this is of no consequence because the output of the latch is not integrated during this period. The comparator responds to the video level continuously but the latch has been designed to latch the first black level it sees after it has been cleared. This detects the presence of black within the element. It also means that the latch has to be cleared immediately before the start of the element for meaningful data to be recovered.

10



System clock generator. All timing considerations of the circuit are based either on the vido sync information or on a 4MHz clock. This could conveniently form the clock signal for a dedicated processing system if required. For this system a v.c.o. has been used to provide the signal but it would be equally acceptable to derive the clock from whatever computer system is to be used. Clock frequency is not a variable parameter and any reduction in frequency results in a reduction in percentage of the video picture processed.

12



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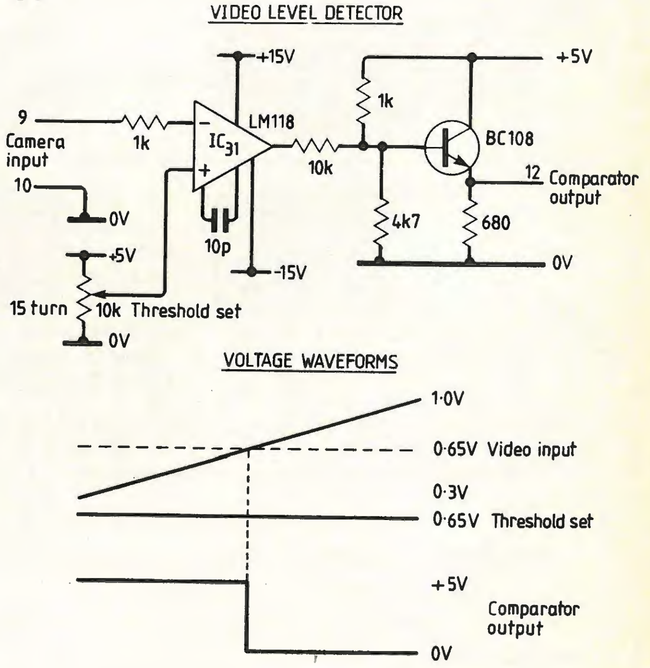

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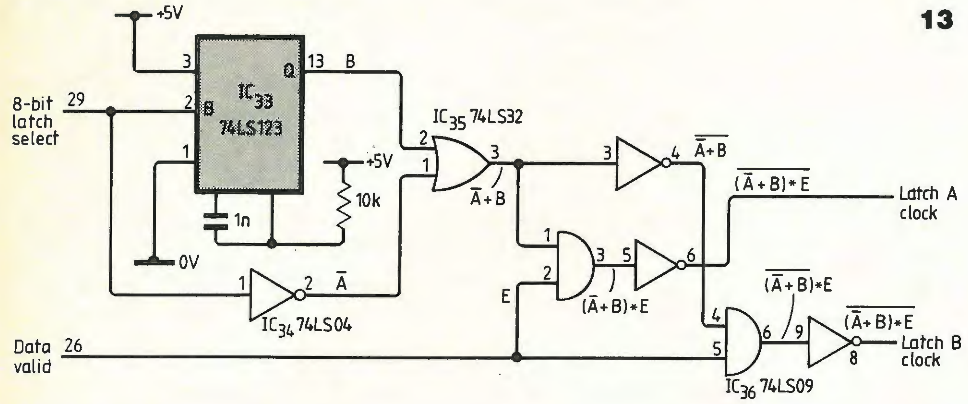
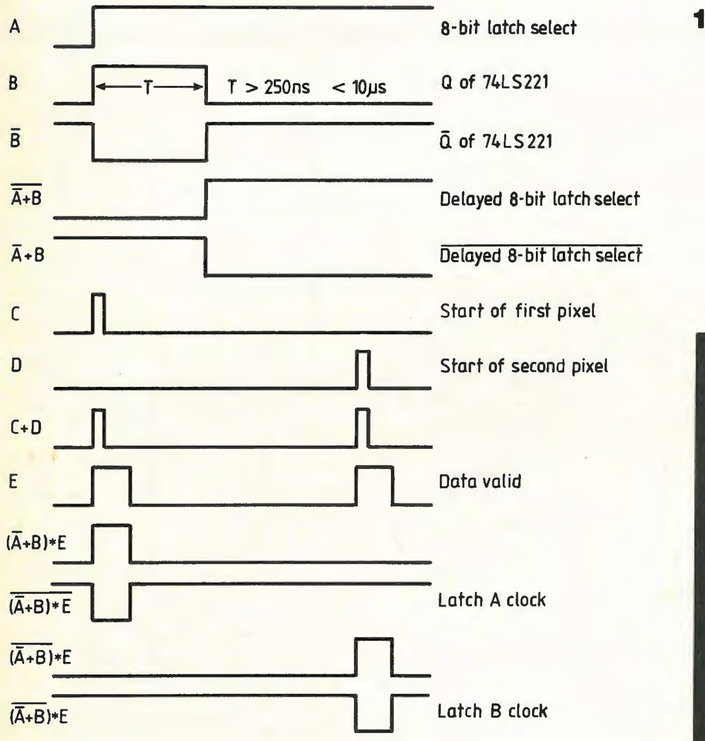


Latch select circuit. 'Eight-bit latch select' line goes high at the beginning of the first element. The signal needs to change state at some time between the end of the first element and the beginning of the second. To achieve this a retriggerable monostable is used to delay the change of state of this line, as shown in the timing diagram. This is then gated by various other logic circuits to produce the final data clocks for the two serial-to-parallel data latches. Latch A must be clocked when the data from the first sample is present and Latch B is to be clocked when data from the second sample is present.

14



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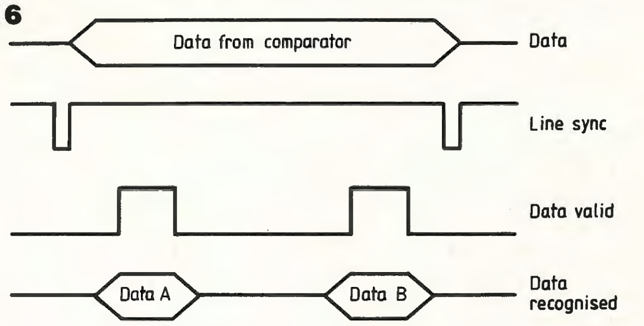
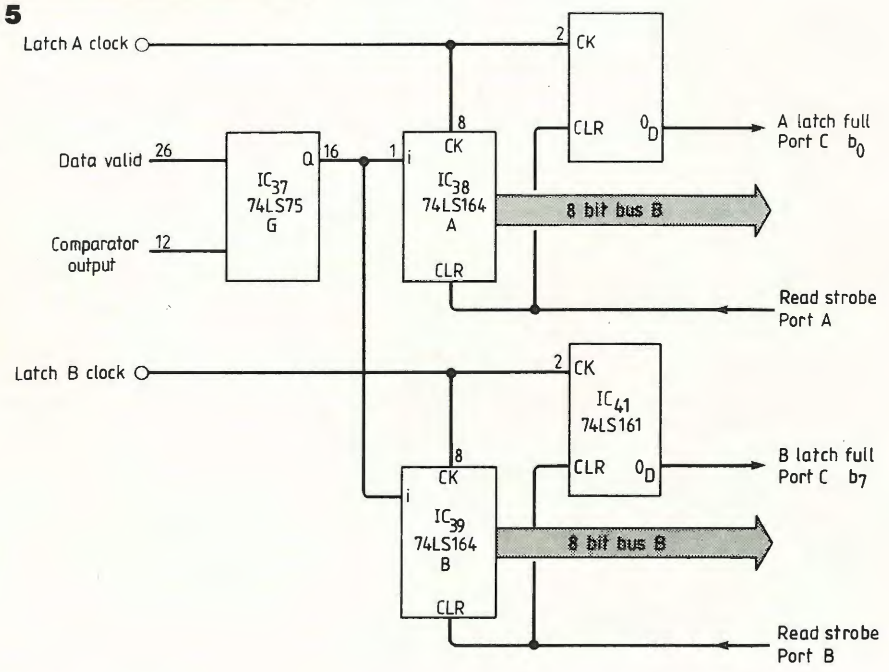
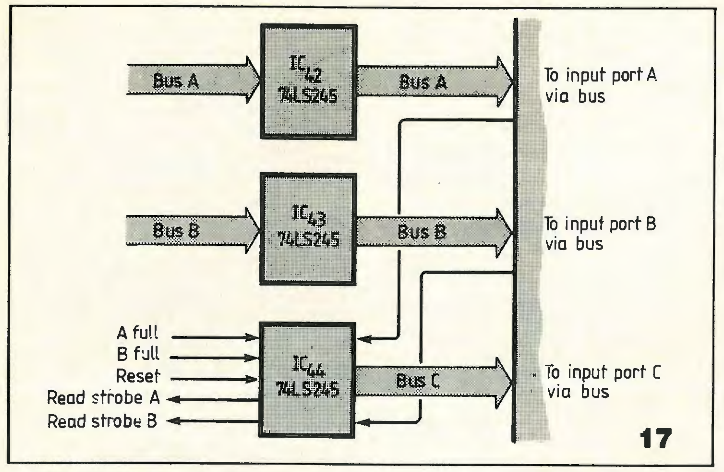


Serial/parallel converter. The circuit also contains the comparator output latch for the video circuit. The flip-flop D input is determined by the 'data valid' signal, which is only high when a valid element position is encountered. Thus the latch only recognises the presence of a black video sample when the data valid signal is high. The latch can then be interrogated by the appropriate serial-to-parallel converter.

15





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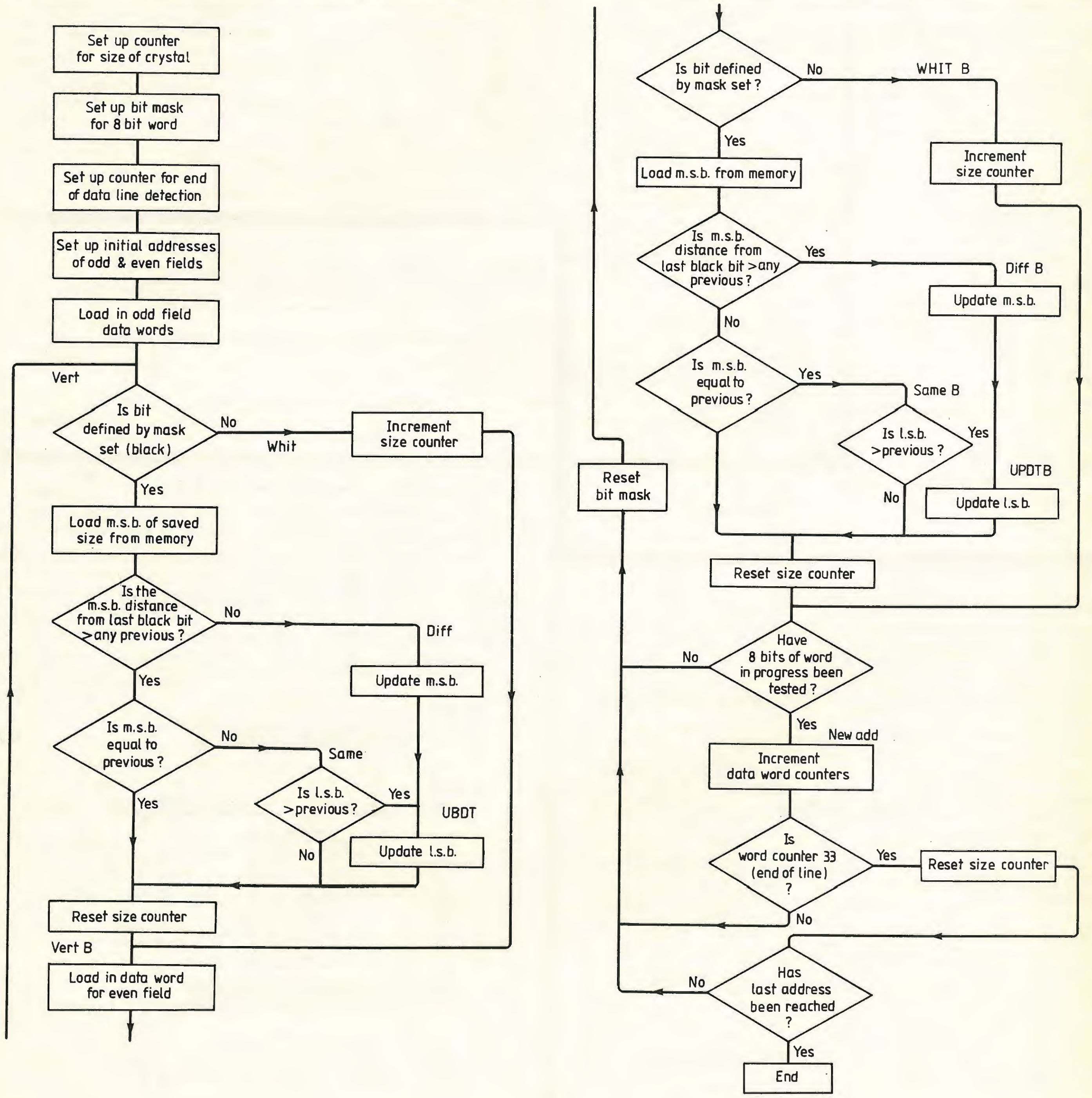
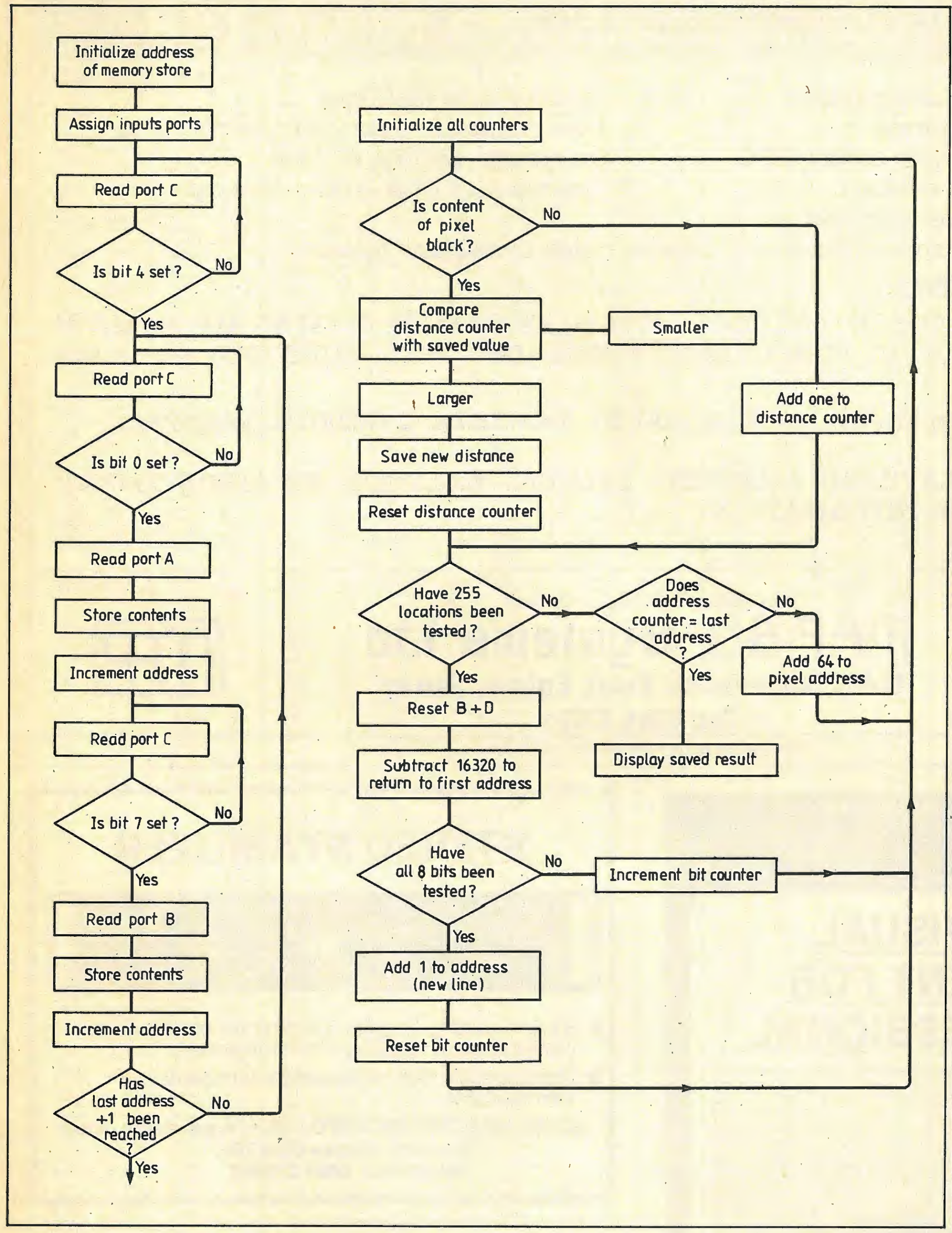
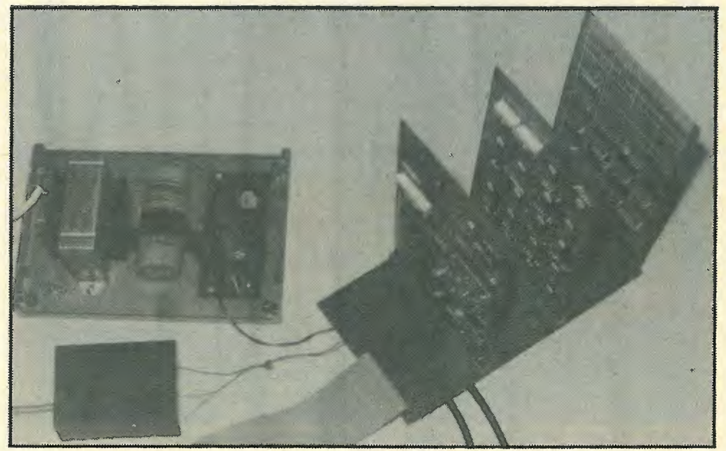
Serial-to-parallel latch builds up an eight-bit word, one bit at a time, on the event of each clock pulse to the device. The clock also increments a four-bit counter. The m.s.b. output from this counter will change state when the count reaches eight. The output is fed to the computer on bus C. Bus A and bus B are fed with data continuously but are only read after the latch full signal is active. On receipt of valid data at port A the 'read strobe' signal from the computer clears the latch and counter ready for the next eight-bit cycle. The same happens for port B. The 'read strobe' signals are buffered by the hardware before use.





Flow charts. Port C of the processor system acts as the control port, with different bits of that port indicating different control functions. Ports A and B are data transfer ports (one way only) and could easily be multiplexed at the hardware end to use only one eight-bit port.

The software written was for the Z80 microprocessor and although not published here, the three flow charts set out the two distance measurement routine structures and the input routine structure showing the polling of port C by the microprocessor system. The measurement software should be studied in conjunction with the hardware memory allocation shown in Fig. 1 (March issue). Results are obtained as percentage values of the total video screen area and must then be related to a scaling factor to produce an absolute reading.



Events

April 2
Electromagnetic interference problems in microprocessor systems; IEE symposium at the IEE, Savoy Place, London WC2 1030h. Tel: 01-240 1871 ext. 269.

April 3
Propagation in an urban environment; IEE colloquium. Details as above.

April 7
Where are satellite communications going? IEE colloquium, as above.

April 7 - 10
Low energy ion beams; Institute of Physics conference at Sussex University. Details from IoP, Tel: 01-235 6111.

April 7 - 10
Application of electronics in medicine and biology; IERE/IEE conference at Nottingham University. Details from IERE, Tel: 01-388 3071.

April 7
Transient eddy current fields; IEE discussion meeting, 1400h. Details as above.

All-electric aircraft of the future; IEEIE/ITEME Mon National Lecture by Prof. D. Howe. Details from IEEIE, Tel: 01-836 3357 ext. 212.

April 8
Image processing for automated inspection; IEE colloquium. Details as above.

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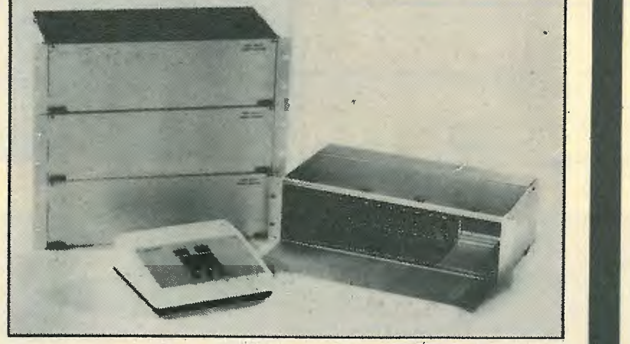

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½MBYTE MEMORY	(OCT 85 ISSUE)	1- ★	£16.00

BOARD CODE: ★ PLATED THROUGH HOLE ●SINGLE SIDED

All P.C.B.'s are supplied with component insertion diagrams. Prices are inclusive of Inland and Overseas Postage, Packing and V.A.T. C.W.O. TO:-

Combe Martin ELECTRONICS
KING STREET, COMBE MARTIN, NORTH DEVON EX34 0AD. TEL: 0271 88 2346

LANGREX SUPPLIES LTD

Climax House, Fallsbrook Rd., Streatham, London SW16 6ED
RST Tel: 01-677 2424 Telex: 946708 RST

SEMICONDUCTORS

AA119	0.10
AAY30	0.17
AAZ13	0.30
AAZ15	0.30
AAZ17	0.30
AC107	0.55
AC125	0.35
AC126	0.35
AC127	0.40
AC128	0.35
AC141	0.35
AC141K	0.45
AC142	0.40
AC142K	0.45
AC176	0.35
AC187	0.35
AC188	0.35
ACY17	2.25
ACY18	1.55
ACY19	1.80
ACY20	1.50
ACY21	1.55
ACY39	4.00
AD149	1.00
AD161	0.50
AD162	0.60
ADZ11	12.50
ADZ12	12.50
AF106	0.60
AF14	3.50
AF115	3.50
AF116	3.50
AF117	4.00
AF139	0.55
AF186	0.75
AF239	0.65
AFZ11	3.75
AFZ12	5.00
ASY26	1.40
ASY27	1.00
ASZ15	2.20
ASZ16	2.00
ASZ17	1.60
ASZ20	4.50
ASZ21	4.75
AUY10	3.50
BA145	0.13
BA148	0.15
BA154	0.06
BA155	0.11
BA156	0.06
BAW62	0.05
BAX13	0.05
BAX16	0.06
BC107	0.12
BC108	0.13
BC109	0.14
BC113	0.12
BC114	0.12
BC115	0.12
BC116	0.19
BC117	0.24
BC118	0.30
BC125	0.25
BC126	0.25
BC135	0.18
BC136	0.18
BC137	0.22
BC147	0.12
BC148	0.12
BC149	0.12
BC157	0.12
BC158	0.13
BC159	0.12
BC167	0.10
BC170	0.09
BC171	0.11
BC172	0.09
BC173	0.09
BC177	0.15
BC178	0.28
BC179	0.15
BC182	0.11
BC183	0.09
BC184	0.11
BC212	0.11
BC213	0.11
BC214	0.11
BC237	0.09
BC238	0.09
BC301	0.36
BC303	0.36
BC307	0.09
BC308	0.09
BC327	0.09
BC328	0.09
BC337	0.09
BC338	0.09
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BCY31	3.75
BCY32	3.75
BCY33	2.50
BCY34	2.50
BCY39	3.60
BCY40	3.00
BCY42	0.32
BCY43	0.45
BCY58	0.25
BCY70	0.21
BCY71	0.21
BCY72	0.21
BCZ1	3.50
BD115	0.35
BD123	2.30
BD124	2.50
BD131	0.42
BD132	0.42
BD135	0.27
BD136	0.27
BD137	0.30
BD138	0.30
BD139	0.30
BD140	0.30
BD144	2.00
BD181	0.75
BD183	0.75
BD237	0.35
BD238	0.35
BDX10	0.91
BDX32	2.00
BDY10	2.40
BDY20	1.50
BDY60	1.50
BF115	0.30
BF152	0.16
BF153	0.19
BF154	0.17
BF159	0.20
BF160	0.20
BF166	0.35
BF167	0.30
BF173	0.45
BF177	0.30
BF178	0.30
BF179	0.30
BF180	0.30
BF181	0.25
BF182	0.30
BF183	0.30
BF184	0.30
BF185	0.30
BF194	0.15
BF195	0.15
BF196	0.15
BF197	0.15
BF200	0.33
BF224	0.12
BF241	0.12
BF244	0.35
BF257	0.30
BF258	0.30
BD137	0.30
BD138	0.30
BD139	0.30
BD140	0.30
BD144	2.00
BD181	0.75
BD183	0.75
BD237	0.35
BD238	0.35
BDX10	0.91
BDX32	2.00
BDY10	2.40
BDY20	1.50
BDY60	1.50
BF115	0.30
BF152	0.16
BF153	0.19
BF154	0.17
BF159	0.20
BF160	0.20
BF166	0.35
BF167	0.30
BF173	0.45
BF177	0.30
BF178	0.30
BF179	0.30
BF180	0.30
BF181	0.25
BF182	0.30
BF183	0.30
BF184	0.30
BF185	0.30
BF194	0.15
BF195	0.15
BF196	0.15
BF197	0.15
BF200	0.33
BF224	0.12
BF241	0.12
BF244	0.35
BF257	0.30
BF258	0.30
Series	
CRS1 40	0.60
CRS3 40	0.75
CRS3 60	0.90
GEX66	3.00
GEX541	6.50
GJ3M	3.00
GM0378A	1.75
KS100A	0.45
MJE340	0.79
MJE370	0.73
MJE371	1.05
MJE520	0.75
MJE521	0.73
MJE2955	2.25
MJE3055	2.00
MPF102	0.55
MPF103	0.55
MPF104	0.55
MPF105	0.55
MPSA06	0.17
MPSA56	0.17
MPSU01	1.11
MPSU06	1.33
MPSU56	1.71
NE555	0.45
NKT401	4.00
NKT403	3.50
NKT404	4.00
OA5	1.75
OA7	0.75
OA10	0.55
OA47	0.15
OA70	0.22
OA79	0.21
OA81	0.21
OA85	0.21
OA90	0.08
OA91	0.08
OA95	0.08
OA200	0.15
OA202	0.15
OA211	1.00
OAZ200	1.50
OAZ201	1.50
OAZ206	1.50
OAZ207	1.50
OC16	5.00
OC20	6.00
OC22	4.50
OC23	10.00
OC24	3.00
OC25	1.75
OC26	1.50
OC28	5.50
OC29	4.40
OC35	4.00
OC36	4.00
OC41	1.20
OC42	1.50
OC43	1.50
OC44	1.25
OC45	0.85
OC71	0.65
OC72	2.20
OC73	1.45
OC74	1.40
OC75	1.40
OC76	1.60
OC77	2.75
OC81	0.90
OC81Z	1.20
OC82	0.95
OC83	1.40
OC84	1.40
OC122	6.50
OC123	6.50
OC139	12.00
OC40	18.00
IC141	18.00
OC170	4.40
OC171	4.40
OC200	4.00
OC201	5.50
OC202	5.50
OC203	5.50
OC204	7.00
OC205	10.00
OC206	8.50
OC207	18.00
OCP71	2.50
ORP12	2.40
R2008B	1.95
R2009	2.25
R2010B	2.00
TIC44	0.48
TIC226D	1.20
TIL209	0.29
TIP29A	0.35
TIP30A	0.36
TIP31A	0.25
TIP32A	0.25
TIP33A	0.53
TIP34A	0.60
TIP41A	0.38
TIP42A	0.42
TIP110	0.40
TIP117	0.45
TIP125	0.35
TIP130	0.45
TIP131	0.45
TIP132	0.48
TIP135	0.45
TIP137	0.48
TIP140	0.85
TIP141	0.85
TIP142	0.85
TIP2955	0.60
TIP2955T	0.45
TIP3055	0.60
TIP3055T	0.45
ZS140	0.25
ZS170	0.21
ZS178	0.54
ZS272	0.23
ZS278	0.57
ZTX107	0.12
ZTX108	0.12
ZTX109	0.12
ZTX300	0.13
ZTX301	0.14
ZTX302	0.14
ZTX303	0.14
ZTX304	0.14
ZTX311	0.13
ZTX314	0.25
ZTX500	0.14
ZTX501	0.14
ZTX502	0.14
ZTX503	0.14
ZTX504	0.20
ZTX531	0.20
ZTX550	0.25
1N914	0.03
iN916	0.03
1N4001	0.04
1N4002	0.04
1N4003	0.04
1N4004	0.04
1N4005	0.04
1N4006	0.04
1N4007	0.05
1N4009	0.06
1N4148	0.03
1N5400	0.10
1N5401	0.11
1S44	0.04
1S920	0.10
1S921	0.12
2G301	1.00
2G302	1.20
2G306	1.50
2N404	1.50
2N696	0.30
2N697	0.36
2N698	0.38
2N705	2.50
2N706	0.20
2N708	0.22
2N930	0.25
2N1131	0.35
2N1132	0.35
2N1302	1.80
2N1303	0.90
2N1304	3.00
2N1305	1.00
2N1306	3.00
2N1307	1.20
2N1308	4.00
2N1309	1.50
2N1613	0.30
2N1671	5.00
2N1893	0.30
2N2147	8.00
2N2148	2.75
2N2218	0.32
2N2219	0.32
2N2220	0.22
2N2221	0.22
2N2222	0.20
2N2223	7.50
2N2368	0.23
2N2369A	0.23
2N2484	0.24
2N2646	0.75
2N2904	0.30
2N2904A	0.30
2N2905	0.30
2N2906	0.22
2N2907	0.22
2N2924	0.12
2N2925	0.22
2N2926	0.12
2N3053	0.30
2N3054	0.55
2N3055	0.70
2N3440	0.60
2N3441	0.75
2N3442	1.00
2N3614	5.00
2N3702	0.11
2N3703	0.11
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2N3819	0.50
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2N3823	0.80
2N3866	1.00
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2N4058	0.12
2N4059	0.20
2N4060	0.12
2N4061	0.12
2N4062	0.15
2N4124	0.13
2N4126	0.13
2N4248	0.25
2N4288	0.15
2N4289	0.12
2N4400	0.12
2N4401	0.12
2N4402	0.12
2N5457	0.45
2N5458	0.40
2N5459	0.40
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2S019	25.00
2S024	35.00
2S025	35.00
2S026	40.00
2S103	2.50
2S302	5.50
2S303	5.50
2S322	5.00
2S324	4.00
2S701	12.50
2S745A	1.75
2S746A	1.75

VALVES

A1834	9.00
A2087	13.50
A2134	17.50
A2293	16.00
A2426	35.00
A2521	25.00
A2900	15.00
A3343	45.00
AZ31	2.75
AZ41	2.60
BK448	114.90
BK484	155.35
BS90	58.00
BS810	60.00
BT5	58.95
BT17	185.00
BT19	44.05
BT29	349.15
BT69	354.80
BT95	129.90
CBL31	4.00
CL33	4.00
CY31	3.00
C1K	20.00
C3A	22.00
C3JA	22.00
DA41	25.00
DA42	18.70
DAF91	1.75
DAF96	1.75
DET22	35.00
DET	49.00
DF91	1.75
DF96	1.75
DK91	1.75
DK92	2.00
DK96	1.75
DL92	2.00
DL94	1.75
DL96	1.75
DLS10	14.00
DLS15	12.50
DLS16	12.50
DLS19	12.50
DM70	2.00
DM71	2.00
DM160	4.75
DY87	1.50
DY802	1.50
E55L	50.00
E80CC	15.00
E80CF	11.27
E80F	14.19
E80L	13.73
E81CC	8.00
E81L	13.27
E82CC	8.10
E83CC	8.40
E86C	8.25
E88C	8.25
E88CC	10.33
E90CC	9.47
E90F	9.90
E91H	6.25
E92CC	8.75
E99F	9.10
E130L	18.50
E180CC	10.50
E180F	12.05
E182CC	13.25
E186F	11.50
E188CC	8.91
E280F	22.51
E283CC	12.00
E288CC	17.50
E810F	35.48
EA52	32.25
EA76	2.50
EA8C80	1.25
EAC91	3.50
EAF42	2.50
EAF801	2.00
EB41	4.00
EB91	1.50
EBC33	2.50
EBC41	2.50
EBC81	1.50
EBC90	1.25
EBF80	1.50
EBF83	1.75
EBF89	1.50
EBL31	10.00
EC90	1.25
EC91	8.00
EC92	1.75
EC157	440.00
ECC33	4.50
ECC35	4.50
ECC40	5.50
ECC81	1.75
ECC82	1.75
ECC83	1.75
ECC84	1.75
ECC85	1.75
ECC86	2.50
ECC88	3.50
ECC89	2.00
ECC91	8.93
ECC189	2.10
ECC807	1.75
ECC808	3.00
ECF80	1.50
ECF82	1.50
ECF86	2.50
ECH35	3.00
ECH42	3.50
ECH81	3.00
ECH83	2.50
ECH84	2.50
ECL80	1.50
ECL81	1.75
ECL82	1.50
ECL83	3.00
ECL84	1.50
ECL85	1.50
ECL86	1.75
EF37	5.00
EF39	2.75
EF40	5.00
EF41	3.50
EF42	4.50
EF50	2.50
EF54	5.00
EF55	3.50
EF80	1.75
EF83	4.00
EF85	1.70
EF86	3.50
EF89	2.50
EF91	2.95
EF92	6.37
EF93	1.50
EF94	2.50
EF95	5.99
EF98	2.00
EF183	2.00
EF184	2.00
EF804S	12.00
EF805S	15.00
EH90	1.75
EK90	1.50
EL32	2.50
El33	4.00
EL34MU1	4.00
EL36	2.50
EL41	2.80
EL42	2.50
EL81	5.25
EL83	6.00
EL84	2.25
EL86	2.75
EL90	3.25
EL91	7.39
EL95	2.00
EL156	30.00
EL360	8.50
EL500	3.00
EL509	10.00
EL821	13.00
EL822	13.97
ELL80	19.00
EM34	8.00
EM80	2,50
EM81	2.50
EM84	2.00
EM85	2.75
EM87	2.50
EN32	25.00
EN91	6.50
EN92	6.96
EY51	2.75
EY81	2.50
EY83	2.50
EY84	9.24
EY86	1.75
EY88	1.75
EY500A	3.00
EY802	1.75
EZ35	1.75
EZ40	2.50
EZ41	2.50
EZ80	1.50
EZ81	1.50
EZ90	3.00
FW4-500	3.50
FW4-800	3.50
G1.371K	35.00
G551K	12.00
G180.2M	17.50
G240.2D	12.00
G400.1K	17.50
GN4	9.00
GN4A	9.00
GN4A	9.00
GS16	16.00
GT1C	25.00
GU50	20.00
GU51	20.00
GXU1	15.35
GXU2	3.50
GXu3	25.40
GXU4	44.50
GXU50	20.00
GY501	3.00
GZ32	4.00
GZ33	4.75
GZ34	4.00
GZ37	4.75
KT61	5.00
KT66	15.00
KT77 Gold Lion	12.00
KT88 Gold Lion	20.00
KTW61	2.50
KTW62	2.50
KTW63	2.50
M8079	12.34
M8080	8.25
M8081	9.82
M8082	9.69
M8083	10.25
M8091	10.43
M8096	6.80
M8097	8.10
M8098	8.15
M8099	8.00
M8100	10.30
M8136	11.75
M8137	12.25
M8140	6.00
M8141	6.50
M8142	8.75
M9144	7.50
M8149	6.50
M8161	9.35
M8162	11.75
M8163	8.25
M8190	5.00
M8195	10.85
M8196	7.50
M8204	7.05
M8212	11.37
M8223	6.00
M8224	6.30
M8225	4.50
M8248	14.03
MD2901	115.00
MU14	2.50
MX119	55.00
MX123	76.00
MX145	56.70
MX151	17.25
MX152	131.25
MX161	152.25
MX163	20.25
MX164	25.52
MX166	147.00
MX168	50.00
N78	15.00
OA2	3.25
OA3	2.50
OA4	6.00
OB2	4.35
OB3	2.50
OC2	4.35
OC3	2.50
OD3	2.50
OZ4	3.50
PC86	2.50
PC88	2.50
PC95	1.75
PC97	1.75
PC900	1.75
PCC84	1.50
PCC85	1.50
PCC88	2.00
PCC89	1.75
PCC189	2.50
PCC805	1.60
PCC806	1.60
PCE82	2.00
PCF80	2.00
PCF82	1.50
PCF86	2.50
PCF87	2.00
PCF200	3.25
PCF201	3.25
PCF801	2.50
PCF802	2.50
PCF805	1.70
PCF806	1.70
PCF808	1.70
PCL82	2.00
PCL83	3.00
PCL84	2.00
PCL85	2.50
PCL86	2.50
PCL805/85	2.50
PD500	6.00
PE06-40N	45.00
PFL200	2.50
PL36	2.50
PL81	1.75
PL81A	2.00
PL82	1.50
PL83	2.50
PL84	2.00
PL504 5	2.50
PL508	5.50
PL509	6.00
PL519	6.00
PL801	1.50
PL802	6.00
PY802	6.00
PY33	2.50
PY81	1.50
PY82	1.50
PY83	1.25
PY88	2.00
PY500A	4.00
PY800	1.50
PY801	1.50
QF451	82.50
QQV02-6	34.00
QQV03-10	25.00
QQV03-20A	48.38
QQV06-40A	46.00
QQV07-50	
69, 74 QQZ20	
6-4QA	62.20
QU37	12.50
QV03-12	6.80
QV04-7	3.50
QV08-100	188.00
QY3-65	63.24
QY3-125	72.00
QY4-250	74.00
QY4-400	80.00
QY5-500	199.00
QY5-3000A	472.00
QZ06-20	32.70
R10	6.00
R17	3.00
R18	3.00
R19	9.24
R20	2.50
RG3-250	32.68
RG3-250A	32.68
RG3-1250	59.00
RG4-1250	61.60
RG4-3000	99.45
RR3-250	40.00
RR3-1250	45.75
SHE12	65.00
S130	6.00
S130P	6.00
STV280-40	14.00
STV280-80	21.00
SU41	5.00
SU42	10.00
TD03-10	35.00
TD03-10F	35.00
T15	50.00
TT21	37.50
TT22	37.50
TT100	60.00
TY2-125	75.00
TY4-400	84.00
TY4-500	110.00
TY5-500	225.00
TY6-800	220.00
TY6-500A	515.00
TY6-5000B	395.00
TY6-5000W	446.00
TY7-6000A	552.00
TY7-6000W	552.00
TZ40	25.00
U18.20	3.50
U19	13.75
U25	2.50
U26	2.50
U37	12.00
UABC80	1.25
UAF42	2.50
UB41	3.00
UBC41	2.25
UBF89	1.50
UCC84	1.75
UCC85	1.85
UFC80	2.00
UCH42	2.50
UCH81	2.50
UCL82	1.75
UCL83	2.75
UF41	2.00
UF42	2.10
UF80	1.75
UF85	1.75
UF89	2.00
UL41	5.00
UL84	1.75
UM80	2.00
UY41	2.25
UY81	2.25
VLS631	15.00
XG1-2500	55.00
XG2-6400	141.90
XG5-500	30.00
XG2-6400	185.00
XR1-1600A	53.75
XR1-3200	110.00
XR1-3200A	
XR1-6400	150.00
YD1120	395.00
YD1240	490.00
Z803U	25.00
Z259	25.00
ZM1001	8.00
ZM1020	9.00
ZM1021	9.00
ZM1022	9.00
ZM1023	9.00
ZM1040	19.36
ZM1041	16.66
ZM1042	17.77
1B3GT	3.00
1B24	25.00
1B35A	48.00
iB63	64.00
1R5	1.75
1S5	1.75
1T4	1.75
2AS15	11.50
2C39A	60.00
2C43	70.00
2D21	3.25
2E26	8.25
2J42	98.00
2J55	245.00
2J70A	383.00
2J70B	336.00
2K25	125.00
3400Z	115.00
3500Z	100.00
3A5	3.00
3B24	11.00
3B28	15.35
3B29	20.05
3B240M	17.50
3B241M	17.50
3C23	25.00
3C24	24.50
3CX100A	47.00
3E29	45.00
3S4	2.00
3V4	1.75
4-65A	60.00
4-125A	60.00
4-250A	80.00
4-400A	87.00
4B32	20.00
4C35	120.00
4CX250B	58;00
4CX350A	105.00
4X150A	60.00
4X150D	56.00
5B254M	35.00
5B255M	35.00
5C22	160.00
5J180E	1650.00
5R4GY	5.50
5U4G	3.00
5U4GB	2.50
5V4G	2.50
5Y3GT	2.50
5Z3	4.00
5Z4G	2.50
5Z4GT	2.50
6-30L2	1.75
6AB4	1.75
6AB7	3.00
6AC7	3.00
6AF4A	4.25
6AG7	3.00
6AH6	5.00
6AK5	5.99
6AK6	2.50
6AL5	1.50
6AM4	4.00
6AM5	9.69
6AM6	6.02
6ANS	4.75
6AN8A	3.50
6AQ5	3.25
6AS6	8.66
6AS7G	8.75
6AT6	1.25
6AU5GT	5.00
6AU6	2.50
6AV5GA	4.50
6AV6	1.50
6AX5GT	3.00
6B7	3.25
6B8	3.25
6BA6	1.50
6BA7	5.00
6BA8A	4.00
6BC4	4.00
6BE6	1.50
6BH6	2.50
6BJ6	2.25
6BK4	4.50
6BL6	85.00
6BL7GT	4.50
6BM6	115.00
6BN6	2.00
6BQ7A	3.50
6BR7	6.00
6BR8A	3.50
6BS7	6.00
6BW6	6.00
6BW7	1.50
6BX7GT	5.00
6BZ6	2.75
6C4	1.25
6CB6A	2.54
6CD6GA	5.00
6CG7	2.50
6CH6	13.00
6CL6	3.75
6CW4	8.00
6D2	1.50
6DK6	3.00
6DQ6B	4.75
6EA8	3.00
6EB8	2.50
6EW6	2.25
6F6	3.00
6F23	1.60
6F28	1.60
6F33	33.50
6H1	14.00
6H2N	2.75
6H3N	2.75
6H6	3.00
6J4	5.50
6J6	8.93
6J7	4.75
6JE6	7.50
6K4N	2.50
6K6GT	2.75
6K7	3.00
6K8	3.00
6KD6	7.00
6L6G	3.00
616GA	3.50
6L6GC	5.75
6L6GT	3.00
6L7	2.50
6N2P	2.50
6N3P	2.50
	2.50
6N7	3.00
6P225	4.00
6Q7	3.75
6K7	3.25
6RHH8 6KN8	10.00
6SA7	3.00
6SC7	2.75
6SF7	2.50
6SH7	3.00
6SJ7	3.25
6SK7	3.50
6SK7GT	3.00
6SN7GT	3.00
6SQ7	3.40
6SR7	4.00
6SS7	2.75
6U5G	3.50
6U8A	2.25
6V6GT	4.25
6X4	3.00
6X5GT	1.75
7B7	2.50
7C3	4.00
7C6	2.50
7H7	4.00
7R7	4.25
7S7	3.50
7Y4	2.25
7Z4	2.00
HE3	55.00
12AH8	5.00
12AT6	1.50
12AT7	1.75
12AU6	2.50
12AU7	1.75
12AV6	2.50
12AW7	3.50
12AX7	1.75
12AY7A	4.00
12B4A	3.50
12BA6	2.50
12BE6	2.50
12BH7	2.75
12BY7	3.00
12E1	20.00
12E11TT	28.00
12E14	65.00
12E1	170.00
19H4	27.50
19H5	47.50
24B9	67.25
30C15	2.00
30C17	2.00
30C18	2.00
30F5	1.60
30FL1 2	1.38
30FL12	1.80
30FL14	2.00
30L1	1.50
30L15	2.00
30L17	2.00
30P4	2.50
30P19	2.50
30PL1	3.00
30PL14	1.80
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150B3	8.35
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150C4	6.00
211	35.00
723AB	125.00
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805	45.00
807	3.75
811A	18.33
812A	35.00
813 vavle	65.00
833A	193.16
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872A	20.00
922	6.00
931A	18.50
1624	4.00
1625	3.50
2050	7.50
4212E	300.00
4212H	300.00
5544	110.00
5545	150.00
5551A	120.00
5552A	153.35
5642	9.00
5654	3.00
5651	4.45
5670	4.50
5675	28.00
5687	6.00
5696	4.50
5718	7.50
5725	5.50
5726	11.37
5727	7.05
5759	2.50
5751	4.00
5763	4.50
5814A	4.00
5840	4.00
5842	12.00
5876A	31.50
5879	5.00
586	17.50
5963	2.50
5965	3.50
6005	2.25
6021	4.50
6057	12.25
6058	12.34
6059	6.00
6061	6.00
6063	3.75
6064	10.25
6067	11.75
6072	6.00
6080	14.00
6097A	235.00
6097B	200.00
6146A	12.00
6146B	12.00
6159B	19.00
6189	9.50
6201	11.40
6442	20.00
6550	8.00
6883B	12.50
6973	7.50
7025	3.00
7027A	8.00
7551	6.25
7586	15.00
7587	23.00
7609	56.00
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3JP7	10.00
3KP1	15.00
3RP1	35.00
3WP1	20.00
5ADP1	55.00
5CP1	10.00
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5P15A	15.00
5UP7	25.00
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DG7-32	58.07
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7400	0.35
7401	0.36
7402	0.36
7403	0.36
7404	0.42
7405	0.42
7406	0.48
7407	0.55
7408	0.36
7409	0.36
7410	0.36
7411	0.40
7412	0.42
7413	0.36
7416	0.48
7417	0.48
7420	0.48
7422	0.36
7423	0.36
7425	0.36
7427	0.36
7428	0.36
7430	0.36
7432	0.36
7433	0.55
7437	0.36
7438	0.36
7439	0.36
7440	0.36
7441	0.48
7442	1.25
7450	0.30
7451	0.30
7453	0.30
7454	0.30
7460	0.30
7470	0.48
7472	0.30
7473	0.48
7474	0.36
7475	0.65
7476	0.48
7480	0.32
7483	0.48
7484	0.72
7486	0.54
7490	0.72
7491	0.36
7492	0.54
7493	0.54
7494	0.78
7495	0.65
7496	0.60
7497	3.90
74100	0.84
74107	0.36
74109	0.54
74110	0.48
74111	0.51
74116	1.50
74118	1.20
74119	1.50
74120	0.75
74121	0.54
74122	0.70
74123	0.60
74125	0.60
74126	0.54
74128	0.55
74136	0.70
74141	0.46
74143	1.30
74145	0.72
74147	1.50
74148	1.40
74150	1.60
74151	0.36
74154	1.40
74155	0.60
74156	0.48
74159	1.75
74170	1.20
74172	4.00
74173	0.72
74174	0.60
74175	1.00
74176	1.00
74180	1.48
74190	1.20
74191	1.20
74192	1.10
74193	0.60
74194	1.10
74195	0.72
74196	1.00
74197	1.00
74198	2.20
74199	2.20
TAA570	1.75
TAA630S	1.75
TAA700	3.00
TBA480Q	1.50
TBA520Q	1.50
TBA530	1.50
TBA550Q	1.75
TBA560Q	1.75
TBA673	1.75
TBA700	1.50
TBA700Q	1.75
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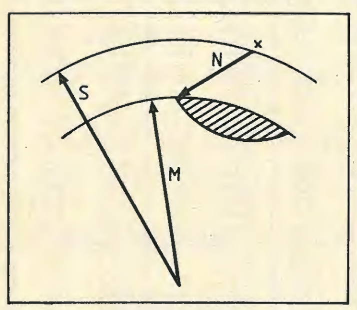
CIRCLE 43 FOR FURTHER DETAILS.

by Professor
D.A. Bell,
F.Inst.P.,
F.I.E.E.

Channel capacity:

the meaning of Shannon's formula

Shannon's well known theory is statistical in nature, and requires large numbers from which to derive an average result.



Part of section of concentric hyperspheres of 2TW dimensions and radii M, corresponding to the transmitted message, and S to the received signal.

"The communication capacity of a channel? That's simple. Shannon's formula is $C \leqq W \log_2(1+P/N)$ bits per second." This is all too common an attitude and ignores two important qualifications which are clearly stated in Shannon's original publication[1].

(i) "If the channel is noisy it is not in general possible to reconstruct the original message or the transmitted signal with *certainty* by any operation on the received signal E". (p.407)

(ii) "By sufficiently involved encoding systems we can transmit binary digits at the rate

$$W\log_2\frac{P+N}{N}$$

bits per second with arbitrarily small frequency of errors." (p.640)

The first qualification reminds us that Shannon's is a *statistical* theory, concerned not with individual events but with expected results on an average over large numbers. When the second qualification is added to the formula one must ask what is meant by "sufficiently involved encoding" and how the degree of complexity of coding is related (as one might reasonably expect it to be) to the smallness of "arbitrarily small" frequency of errors. In the light of this question, Shannon's channel-capacity formula looks similar to Carnot's heat-engine formula, which could be written as $W \leqq Q_i(T_1 - T_2)/T_1$ where W is the mechanical work obtainable from heat Q_i by an engine working between temperatures T_1 and T_2: the formula shows the most that could ever be obtained, but gives no clue as to how to obtain it.

Further understanding requires an examination of the derivation of the formula for channel capacity, and there is a geometric derivation[2,3] of which the accompanying diagram serves as a reminder. A model is constructed with lengths (radii) proportional to average amplitudes of signal or noise or in fact proportional to 2TW times the square root of TW times signal or noise average powers. The geometry is of 2TW dimensions, where T is the duration of the signal and W its bandwidth, because Shannon's sampling theorem indicates that the signal can be represented by 2TW independent samples (provided its spectrum is white) which can be regarded as orthogonal components of a vector.

It is natural to represent a quantity which has three component variables x, y and z by a three-dimensional model and similarly a quantity which has 2TW components can be represented by a model having 2TW dimensions. The geometry of such a model is, of course, non-Euclidean but has been evaluated by mathematics, so two key theorems can be used: (i) Pythagoras' theorem of the sum of squares can be extended to any number of orthogonal components of an n-dimensional vector and (ii) all the content of a hypersphere of many dimensions is near the surface*. The messages of power P are then spread over the surface of a hypersphere of radius $M=(2TWP)^{\frac{1}{2}}$, while the receiver may receive a signal (message plus noise) at any point X on the surface of a hypersphere of radius $S=[2TW(P+N)]^{\frac{1}{2}}$. The signal could have originated from any point in the shaded part of the message hypersphere in the diagram, the part swept out by the vector N rooted at the point X. (This assumes that the noise power N is known.) The content of the shaded region can be shown to be less than that of a circumscribing hypersphere in the ratio of at least $r = [N/(P+N)]^{TW}$. Then if there are m messages distributed at random in the M hypersphere, the probability of finding only one in the shaded region (i.e. the probability of the received signal being unambiguously related to a particular transmitted message) is found to be $p=(1-r)^{m-1} > 1-(m-1)r$. Assuming m large enough that log m may be written instead of log (m-1), the eventual result is

$$I = \log m \leqq TW\log_2(1+P/N) + (1/T)\log_2\epsilon \ldots\ldots\ldots \quad (1)$$

where I is the information content of the system and ϵ = 1-p is the probability of error. The channel capacity formula for *rate* of communication is obtained by dividing through by T:

$$C = I/T \leqq W\log_2(1+P/N) + (1/T)\log_2\epsilon \text{ bits/sec} \ldots\ldots \quad (2)$$

The usual form is obtained by dropping the $\log_2\epsilon$ term if T is very large. Symmetry would have been maintained by dividing by TW rather than by T:

$$I/TW \leqq \log_2(1+P/N + (1/TW)\log_2\epsilon \ldots\ldots\ldots\ldots\ldots \quad (2a)$$

(Since $\epsilon \ll 1$, $\log_2\epsilon$ is negative.)

The quantity I/TW can be regarded as "information per cycle", but it must be remembered that the formula is valid only as an average for large TW (for $TW \rightarrow \infty$ in mathematical terms, but TW > 100 would be usable approximation[4].) and in particular that the formula must not be applied to a single element of the signal, such as a single digit or a single pixel in a visual image. Detection must be by identification of the whole signal, rather than bit by bit decoding of a digital signal, for example. Many of the commonly used error-correcting codes are elaborations of the simple ideal of the check digit[5]. Interpretation of the received signal then depends on the check digit as well as the information digits; and the dependence on more than one digit is a first step towards use of all the digits simultaneously, which Shannon requires for 'ideal coding'. Sequential decoding[6], particularly of convolution-coded signals, provides dependence on a large number of digits without the need to compare the received signal with every one of the set in use, as would be needed for maximum-likelihood detection in block codes which use a distinct group of digits for each different 'message'. Every sharp threshold decision on a single bit destroys some information (the noise level on that bit), so the best results are obtained by the use of what is known as 'soft decision' decoding in which the decision on any single bit is not absolute but may be changed if that would lead to a closer overall approximation to a known code word, after later digits have been received. All the techniques of wide-band modulation and error-correcting digital codes are aimed at achieving an approach to the Shannon rate of communication through a channel and the performances of particular types of digital code are discussed in texts on error-correcting codes[7].

It must always be remembered that if TW is less than infinite there must be a *probability* of error, however small. The error rate represents an average over a large number of messages sent through the channel and may be presented as the number of errors per year of a digital channel. A channel transmitting continuously at 9·6 kbits/s would handle about 3×10^{11} bits/year so that, at an error rate (after code correction) of 10^{-9} per bit, it would be expected to produce about 300 errors per year. ■

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* Some of the rules of n-dimensional geometry differ according as n is even or odd; but in our case 2TW is necessarily even.

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D/f resurgent

The ability to detect accurately by means of directive antenna systems the direction of arrival of radio signals was discovered and exploited in the early days of radio communication. Early in World War I, d/f networks became a valuable adjunct to signal-intelligence. By the early 1920s, ship and shore installations were being used widely as maritime and aeronautical navigational aids. Although in more recent years d/f has tended to give way to radar and hyperbolic navigational systems, the classic d/f techniques have retained their importance for surveillance and, increasingly, as tactical aids for attacking battlefield communications and radar installations by artillery fire or guided missiles.

While conventional rotating-loop and goniometer (Bellini Tosi) systems can provide accurate daytime fixes on clear-path (ground-wave) l.f./m.f. signals, the sky-wave and multipath propagation of h.f. and v.h.f. signals has always incurred significant errors. Adcock arrays with vertical elements provide better results on h.f.

During WWII, the Germans pioneered the use of large circular arrays ("Wullenweber rings") that present a large aperture to incoming wavefronts and can often provide bearings accurate to well under 1° of arc. They were a significant advance on the Adcock installations and buried receiver tanks used by the British.

Circular arrays have been further improved by the use of computers. The latest h.f./v.h.f. d/f systems can provide "super-resolution" by means of adaptive array techniques with digital processing to permit multiple signal detection, the separation of wanted from unwanted co-channel inference and a reduction of the effects of local coherent multipath, which can otherwise result in rapid fluctuation of bearings of 1° or 2°.

There is also continuing investigation of h.f. propagation mechanisms that can give rise to longer-term errors due to ionospheric tilts, both static and travelling.

According to work carried out at Leicester University, reported at a recent IEE colloqium on "Direction-finding systems in their operating environment", the bearing errors associated with travelling ionospheric disturbances can last from about ten mintues to more than an hour.

Errors due to static tilts predominate during sunrise periods and can persist for two or three hours. Even on Wullenweber arrays, bearing errors of up to about ±5° have been measured on 10MHz one-hop signals from known locations in Austria and Czechoslovakia.

Recent work in relating v.h.f. and microwave d/f errors to their transmitting and receiving sites was also reported.

R.S.R.E. Malvern have shown that v.h.f. d/f for tactical battlefield situations can be significantly affected by typical sites, which in practice are likely to be screened by hills and with a heavily polluted spectrum. In such circumstances the main direct ray may be weaker than reflected signals. Some sites can preclude accurate bearings.

Philips Research Laboratories have developed accurate u.h.f./microwave d/f systems based on their "Miranda" electronic support measures vehicle, using interferometer techniques with twin antennas separated by 800mm. Interferometer techniques are also being used by American amateurs in New Mexico as part of a National Emergency Location transmitter network for finding downed aircraft. It is claimed that, with practice, the bearings of v.h.f. transmitters can be found to within one degree (i.e. less than 600m at 30km distance) by means of a receiver, two antennas and two lengths of coaxial cable that differ by an electrical halfwave, permitting the determination of a base line of from 9m to 15m long.

Optical progress

The development of low-attenuation optical fibres for broadband telecommunications provides an outstanding example of what concentrated research effort can do. Since work began on reducing losses in optical glass in 1966, it has been possible to reduce attenuation from around 1000dB/km to not much more than 0.1dB/km. This has resulted in something approaching a public-relations battle to claim high data rates over increasingly long distances without intermediate repeaters. The Japanese NTT, for example, are claiming to have transmitted 400Mbit/s optical f.s.k. experimentally over 270km of single-mode fibre (total loss 53dB at 1.546μm).

British Telecom, on the other hand, point out that their interest has lessened in achieving long distances under experimental conditions but emphasize that they can now transmit 2.4Gb/s over 32km of operationally installed optical cable, agreeing with a Corning Glass view that the primary focus is shifting to short-distance area-data networks with data rates of around 500Mbit/s. Amphenol claim that new connectors can cut installation time to just a few minutes. As optical systems become operational it should enormously reduce the demand for microwave spectrum for intercity links. The German Post Office, in its "Berlin IV" project, has an 18km route through West Berlin in which one single-mode fibre can be used to transmit two 140Mb/s and one 565Mb/s signals simultaneously over a 36km loop without any regenerators. The single-mode fibres (laid, spliced and terminated) show a mean loss of from about 0.25dB/km to 0.40dB/dm according to the laser wave-length.

Dangers of r.f.i.

The very real problems involved in electromagnetic compatibility and computer control is underlined by two items in a recent issue of *IEEE Spectrum*. In a letter to the editor, Raymond Roehrick complains that the American automobile industry refuses to recognize the danger implicit in computer-controlled engines. He states that should such an engine fail in a car that is going downhill, the driver will not be aware of this until he or she attempts to stop or steer the vehicle, a situation which he regards as "life-threatening".

The other item, introducing a detailed review of the problem of radio-frequency interference in microprocessor systems

("Taming e.m.i. in microprocessor systems", *IEEE Spectrum*, December 1985, pp.30-37), describes an accident during 1983 in an American steel plant when a new radio link was introduced to facilitate communications between the shop floor and the operator guiding ladles of molten steel from the blast furnace to the ingot moulds. Without warning the ladle suddenly tipped prematurely, pouring down hot steel on the workers below — one of whom was killed and four seriously injured. Investigations showed that the presence of temporary scaffolding reinforced the strength of the hand-held transmitter signals. These were rectified in the control system, producing a false signal that tipped the ladle.

The use of plastic enclosures without adequate screening and filtering of vulnerable circuitry including microprocessors and/or r.f-generating digital systems has spread the problems of e.m.i. far and wide. There has been little attempt in the UK to define realistic limits, particularly for consumer electronics, even to the extent of the American FCC and Germany VDE regulations. It can be extremely difficult to produce microprocessor equipment that neither radiates hash nor is itself vulnerable to r.f.i. without adding significantly to costs. Nevertheless, good design practice, the use of adequate filtering and metal or metallized-paint shielding and the recognition that good electromagnetic compatibility is becoming an essential requirement could produce a dramatic improvement to our much polluted spectrum and eliminate dangerously vulnerable systems.

30 years of "trannies"

In his recent IEE lecture (CC February), Dr Geoffrey Phillips mentioned that the first portable transistor radio appeared in the UK in 1956 when Pye marketed a set under its "Pam" brand name.

The story of the rush to put a pocket set on the American market by Christmas 1954 is told in the December 1985 issue of the *IEEE Spectrum*. This was the Regency TR-1 four-transistor radio developed by Texas Instruments in conjunction with the small manufacturing firm of Industrial Development Engineering Associates (Regency). It sold for $49.95 at a time when table radios with valves were selling at $15.

Bell Laboratories announced the development of the transistor on July 1, 1948 and offered licences to anyone prepared to pay $25,000 advance on royalties in Autumn 1951. Texas Instruments immediately mailed their cheque and by the end of 1953 were successfully manufacturing germanium transistors.

But the need was to find a major application for the strange and still unfamiliar devices in order to break the price barrier of around $100 per transistor. With low gain at high frequencies it was even necessary to adopt a 262kHz intermediate frequency. A six-transistor prototype was cut back to five and then four transistors by adopting the self-oscillating mixer (later patented by Richard Koch of TI). The set was announced publicly on October 18, 1954 before production started at the Regency factory. At first board failure rates were 50 per cent. The TR-1 dully appeared by Christmas, 1954, was featured on the cover of the December 1954 *Proc IRE* and sold about 100,000 during the first year. Raytheon marketed a six-transistor radio in February 1955. In January 1954 a small Japanese firm, Tokyo Telecommunications, headed by Masaru Ibuka and Akio Morita, took out a transistor licence from Bell, were producing transistors by June 1954 and in August 1955 marketed the first Japanese transistor radio under its brand name of Sony, adopted as the firm's name in 1957. By March, 1957, Sony produced its first pocket set and sold more than 500,000 of them.

Although the Pam receiver was the first on the market in the UK, it is believed that the first model to reach prototype stage was a Cossor receiver designed by Roy Vivian, now with the IBA, and this prototype was exhibited in the USA about 1955. Because of the limited r.f. performance of the early germanium transistors, record players tended to beat receivers to the UK marketplace.

Amateur Radio

Morse aids the disabled

B.J. Frost, G6UTN of Norwich was interested to read the comments about the special value of morse code to the deaf and very hard of hearing (CC January 1986) reporting the views of Nigel Neame, former G2AUB. Successful work in this field has recently been undertaken by the Great Yarmouth and Lowestoft branch of REMAP, a panel of engineers within a national group who construct mechanical and electronic aids for the disabled.

This work began when G6UTN developed an aid for the family of a totally deaf girl. The aid comprised a miniature, low-consumption 27MHz receiver (2V, 1mA) in conjunction with an indicating device mounted on the girl's spectacles. Her mother was then able to call her from a simple base transmitter using either simple pre-arranged codes or their existing knowledge of morse.

The aid aroused considerable local interest and the group have now developed a two-way aid, also suitable for use between two totally deaf people. This comprises two small transceivers with a wristwatch-mounted indicator and push-button. The push-button initially starts a motor-driven vibrating device to attract attention and then permits transmission of signals. A working prototype has been tested by the local social services but has run into licensing problems since "low-power, non-speech devices" have to use specific frequencies, require DTI type approval and require annual licence fees (shortly to be withdrawn). The 27MHz prototype is thus "illegal". At present such devices have no frequencies available for commercial equipment below 173MHz and although the DTI are considering permitting the use of 49MHz they have not yet issued a technical specification.

By coincidence, Prof. Alex Comfort recently emphasized, in a letter to the RSGB, the value of the morse code in the field of medical robotics, and regretted that he had seen no system that operated using morse code, adding: "Even an incoordinate patient who can manipulate an on-off switch could almost certainly form slow morse characters . . . it indicates a field of communication where amateur skills might make a very large contribution."

in brief

American amateurs are worried about the possible effects on their hobby of a proposed "Electronic Communications Privacy Act" that would make it illegal (as it is in the UK) to deliberately listen to public and private telecommunications services. Such an act would constitute a federal crime. Although amateur radio is an exempted service, the Act is seen as a potential threat to established practices . . . With the first session of a Region 2 (The Americas) planning conference for extending the American medium wave broadcast band up to 1705 kHz, radiolocation services are being shifted to 1900 to 2000 kHz, bringing the prospect of more broadband pulses in a band available to amateurs in both the USA and the UK . . . After two years in orbit UoSAT OSCAR 11 is in a healthy state. UoSAT OSCAR 9 is also working well apart from a few facilities . . . The RSGB National v.h.f. Convention is being held on Sunday, March 16 at the Sandown Park Racecourse, Esher, Surrey . . . The Society's National Amateur Radio Convention is at the National Exhibition Centre, Birmingham on April 5 to 6 . . . Among forthcoming mobile rally locations are: March 16 Carleton Community Centre, Pontefract and Paddocks Community Centre, Canvey Island. March 22 Parkwood Green, Rainham, Kent. March 23 Premier Market Hall, Tiverton, Devon; Patti Pavilion, county cricket ground near Swansea; University of Leeds. April 13 Killyherlein Hotel, near Enniskillen, Northern Ireland.

Pat Hawker, G3UA

CIRCUIT IDEAS

Efficient bridge inverter triggering

This is a triggering scheme for controlling a three-phase bridge inverter as shown in the first diagram.

There are two types of bridge inverter. In the 120° type, each s.c.r. conducts for 120° and two s.c.rs conduct at any instant. In the 180° type, each device conducts for 180° and three s.c.rs conduct at any instant.

More efficient of the two is the 180° type since use factor of the s.c.rs is greater in this mode. Triggering sequence for the s.c.rs in either mode is 1,6,3,2,5,4.

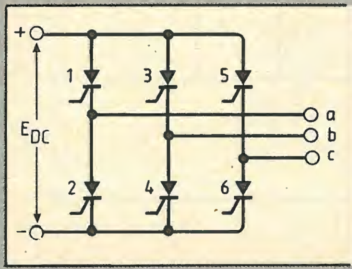
Output frequency depends on the rate at which the s.c.rs are triggered and output voltage on the d.c. input voltage. Inverter output is varied by having an auto-transformer at the output.

In the control circuit, used to determine firing sequence, a 555 timer in astable mode produces pulses at up to 1kHz. These pulses feed a 4bit binary divider connected as a modulo-6 counter (since there are six s.c.rs). Counter outputs are decoded by a 3-to-8-line decoder to select one line at a time at the output, zero to five.

Outputs of the decoder are active low so sequential negative transitions can be used to trigger the six monostable i.cs. Pulse width of each monostable output is adjusted by varying the potentiometer to obtain reliable triggering.

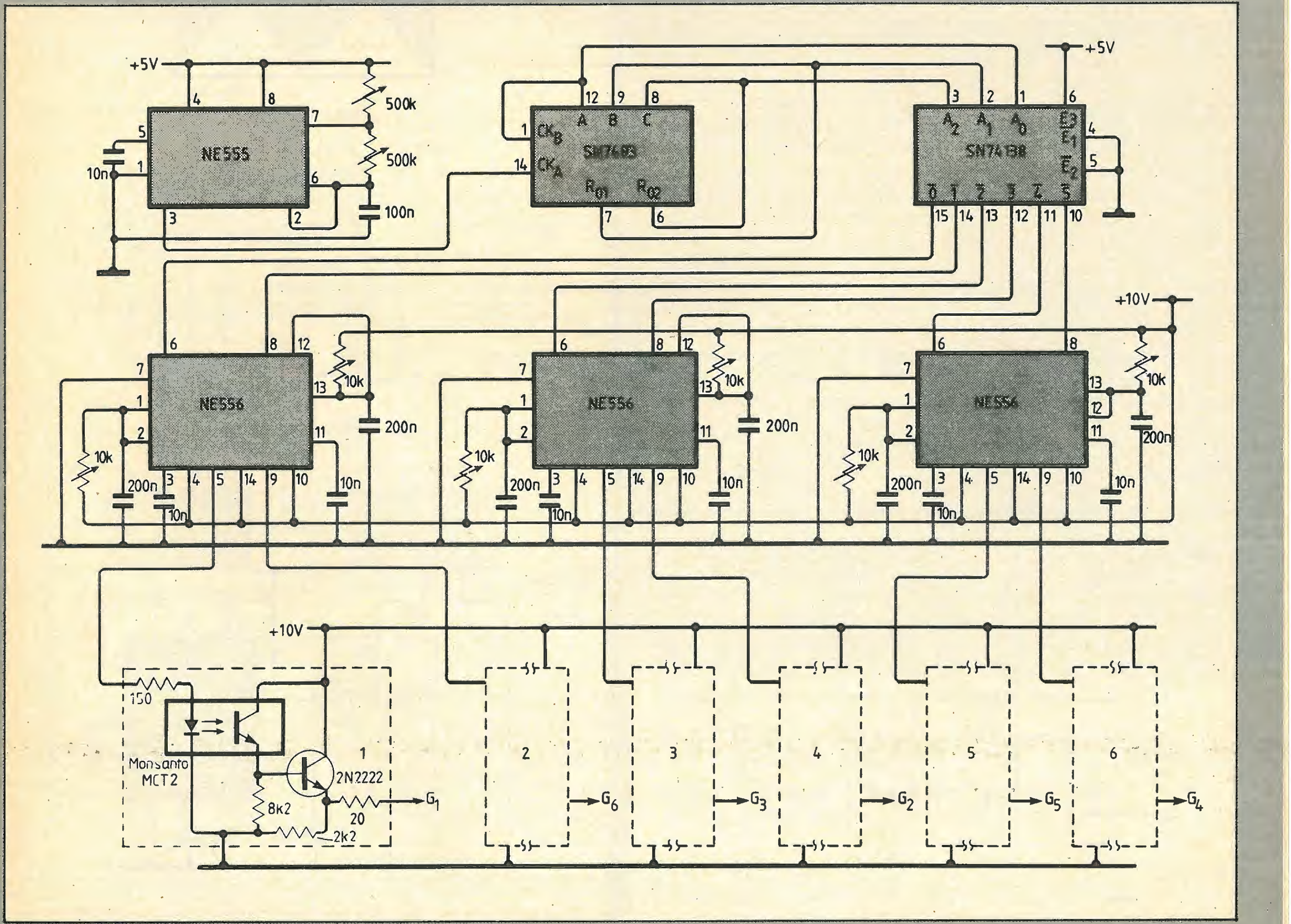
Opto-couplers provide isolation to prevent false triggering. Using optical devices instead of pulse transformers reduces cost and size of the circuit. Class-D commutation can be used for this type of inverter.

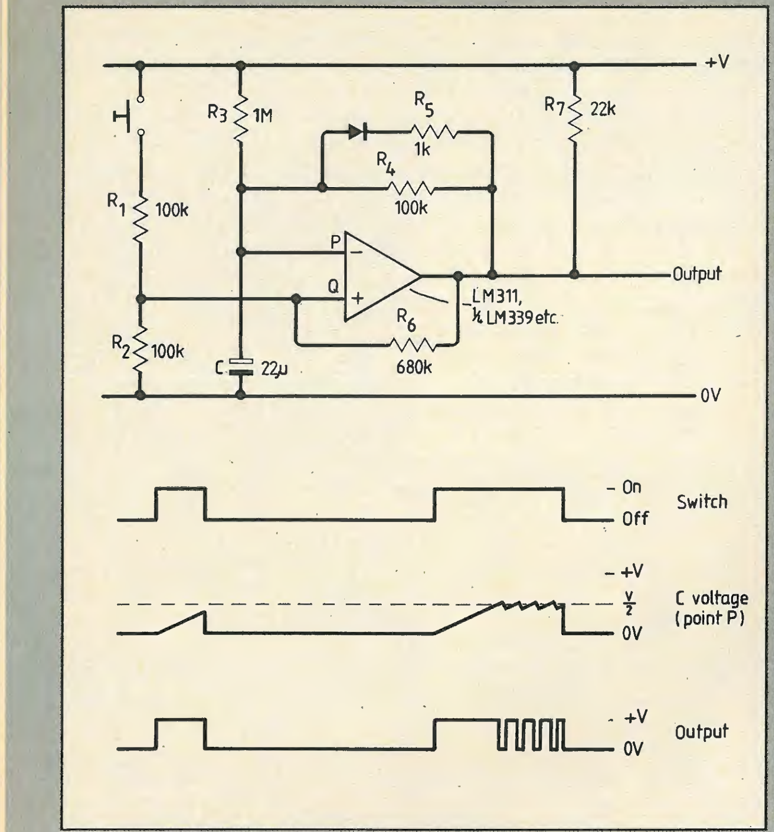
V. Lakshminarayanan
New Delhi
India



DON'T WASTE GOOD IDEAS
We prefer circuit ideas with neat drawings and widely-spaced typescripts, but we would rather have scribbles on "the back of the envelope" than let good ideas be wasted. Submissions are judged on originality and

Also mention how far your idea has been developed.





Automatic keyboard repeat

Closing the switch for a brief period causes a single pulse at the output, but closing the switch and holding it closed causes a single pulse followed by a delay then a stream of pulses.

When the switch is open, non-inverting input to the amplifier is held at ground and output is driven low. The diode and R_5 discharge the capacitor rapidly. Inverting input is held positive with respect to non-inverting input by R_3.

Closing the switch sends point Q positive to raise the output so that R_4 charges the capacitor and point P moves toward Q. Releasing the switch before point P reaches point Q results in only one pulse, but if the switch is held, a stream of pulses is produced.

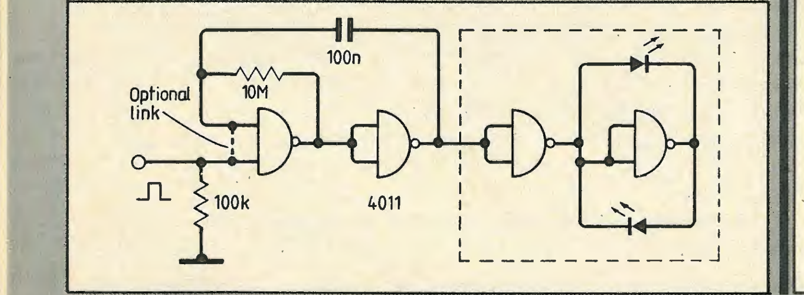
Time before auto-repeat starts is $0.74R_4C_1$ and repeat frequency is $R_6/R_1.(1/(R_4C_1))$. For values shown, delay is about 1.5s and repeat frequency is 3Hz.

S.J. Kearley
Wirral
Merseyside

Led flasher

I haven't seen leds wired this way before. Current is limited by internal resistance of the gates and total led series resistance is about 800Ω.

R. Kirwan
Wolverhampton
West Midlands



Phase-locked loops

Does the basic p.l.l. shown in the first diagram lock in a wide range when its v.c.o. runs at twice the input frequency? If you answer no then look at the second diagram.

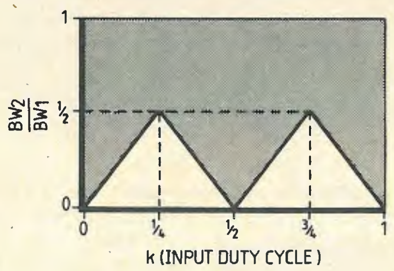
In this circuit, f_s can be set around 2MHz by the potentiometer. Free-running frequency of the v.c.o. is about 4MHz, which is twice input centre frequency f_s. Using an oscilloscope, you will find that lock range BW_2 is around 20% of $f_o/2$. Although this is less than the usual lock range of BW_1 when $f_o = f_s$, it is still wide enough for many uses.

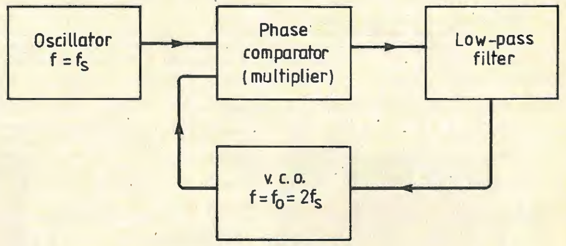
A second question arises — is BW_2 constant? The answer is no. Duty-cycle of the input frequency, k, determines BW_2, where k is $t_{on}f_s$ and t_{on} is the duration of the input signal above the average level.

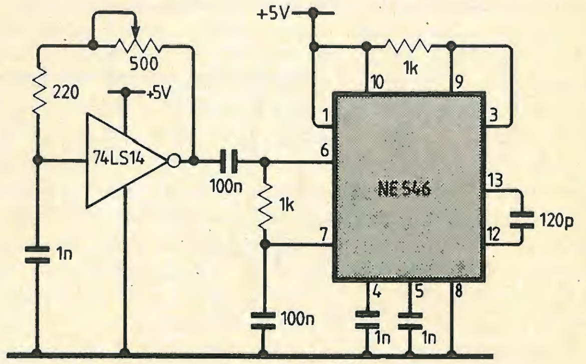
From the graph, BW_2 is zero for symmetrical sinewaves, when k is ½, and maximum when k is ¼ or ¾. Range BW_2 is half of BW_1 which is acceptable in practice.

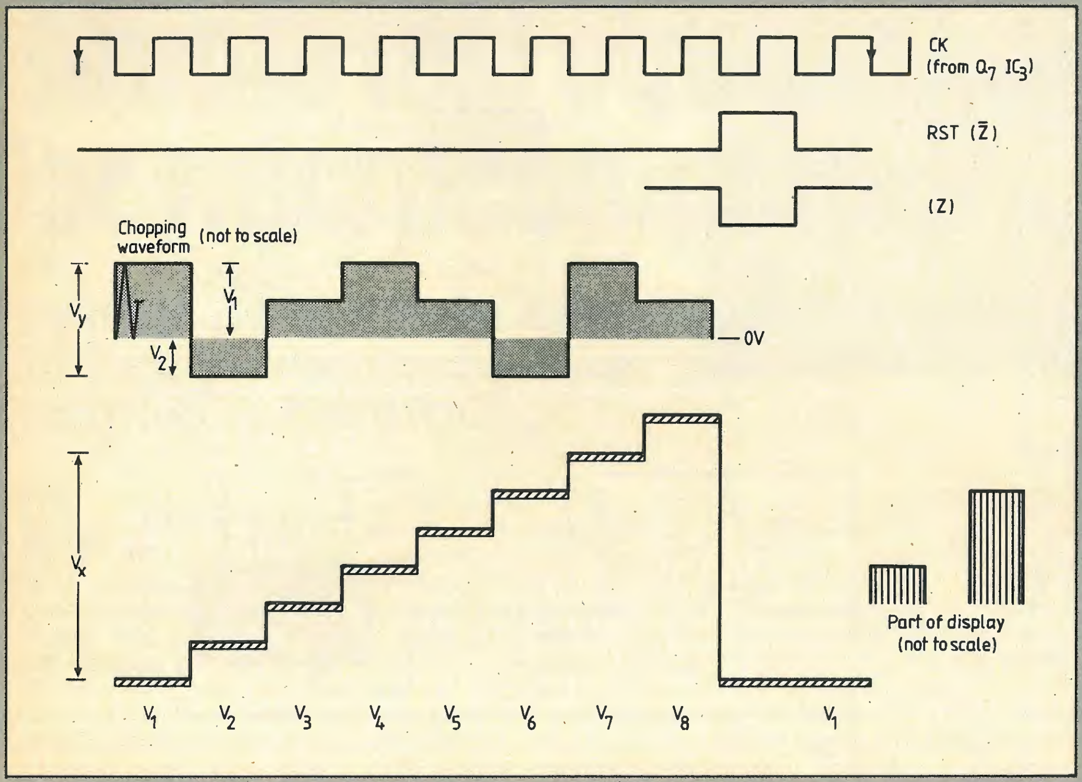
Importance of this special case is that the circuit will lock even if the input signal polarity changes continuously as in d.s.b.s.c. (180° phase shift).

A.R. Moubayed
Autolight
Aleppo
Syria









Oscilloscope bar display

Simple switching and a d-to-a converter make it possible to show up to eight analogue inputs simultaneously on an oscilloscope as a set of bar indications.

Multiplexer inputs are selected sequentially by the counter whose outputs feed a simple 3bit d-to-a converter consisting of three inverters and resistor ladder. Output from the converter provides x deflection for the oscilloscope.

Each multiplex input has an x deflection associated with it.

Mpx i/p	X o/p
0	5V
1	3.6V
2	2.2V
3	0.7V
4	−0.75V
5	−2V
6	−3.6V
7	−5.0V

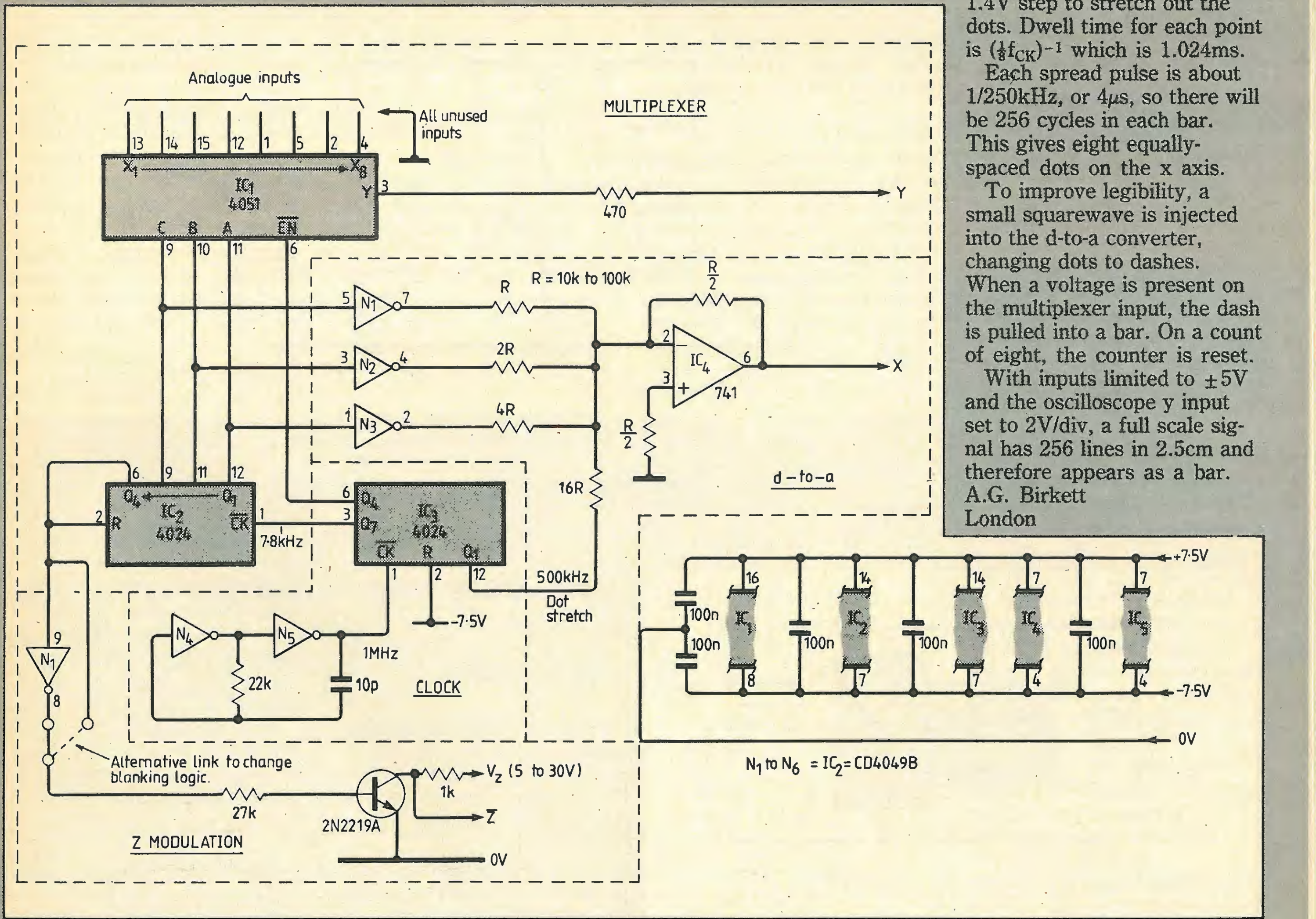
A small squarewave signal of about 140mV is added to each 1.4V step to stretch out the dots. Dwell time for each point is $(\frac{1}{8}f_{CK})^{-1}$ which is 1.024ms.

Each spread pulse is about 1/250kHz, or 4μs, so there will be 256 cycles in each bar. This gives eight equally-spaced dots on the x axis.

To improve legibility, a small squarewave is injected into the d-to-a converter, changing dots to dashes. When a voltage is present on the multiplexer input, the dash is pulled into a bar. On a count of eight, the counter is reset.

With inputs limited to ±5V and the oscilloscope y input set to 2V/div, a full scale signal has 256 lines in 2.5cm and therefore appears as a bar.

A.G. Birkett
London



Linear voltage-controlled resistance and conductance

Voltage-controlled resistances and conductances give versatility in electronic design. Applications include tuning elements in active filters and variable-gain attenuators.

They usually use intrinsic device characteristics like small-signal forward resistance of a diode, which is inversely proportional to junction current, or drain-source resistance of a j-fet; most such methods make use of a very small linear region and have disadvantages.

The first circuit is a linear and accurate voltage-controlled conductance using a four-quadrant analogue multiplier and voltage-to-current converter.

Assuming that the multiplier input resistance is high enough, circuit behaviour is expressed as follows.

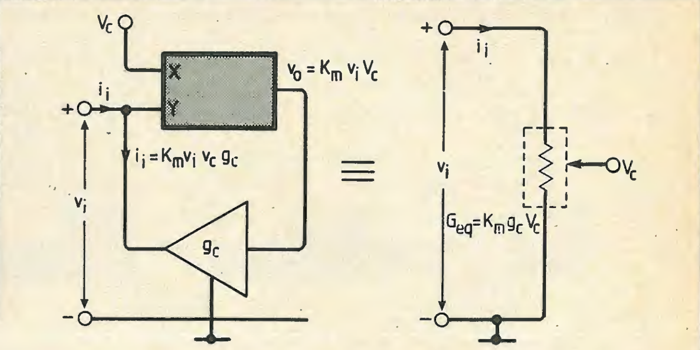
$$G_{eq}=\frac{i_i}{v_i}=K_m g_c v_c.$$

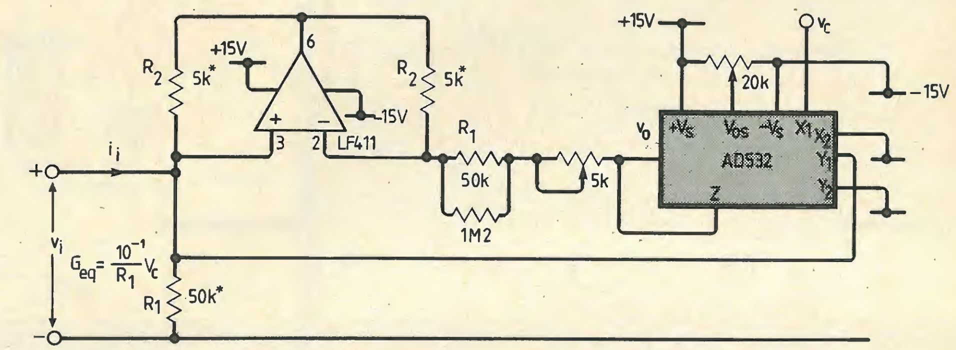
where K_m is the multiplier scale factor, usually 10^{-1} volt^{-1}, g_c is the converter v/i transconductance and v_c is the signal voltage control. In the top diagram, source current can be implemented by a Howland current pump, as shown in the first circuit.

Using $G_{eq}=(K_m/R_1)V_c$, a voltage-controlled resistor can be built by making use of a gyrator terminated at its output by a voltage-controlled conductance as described above. For this circuit, bottom, equivalent input resistance is

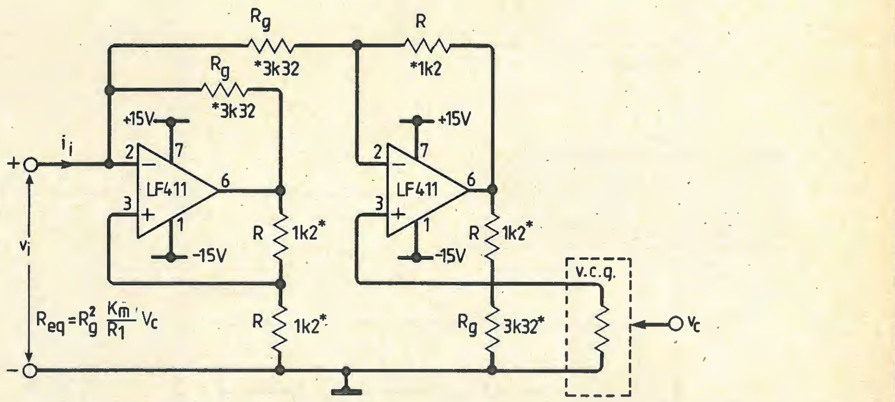
$$R_{in}=\frac{R_g{}^2}{Z_L}=R_g{}^2\frac{K_m}{R_1}v_c$$

José M. Miguel
Escola Tècnica Superior
d'Enginyers de
Telecomunicació
Barcelona
Spain

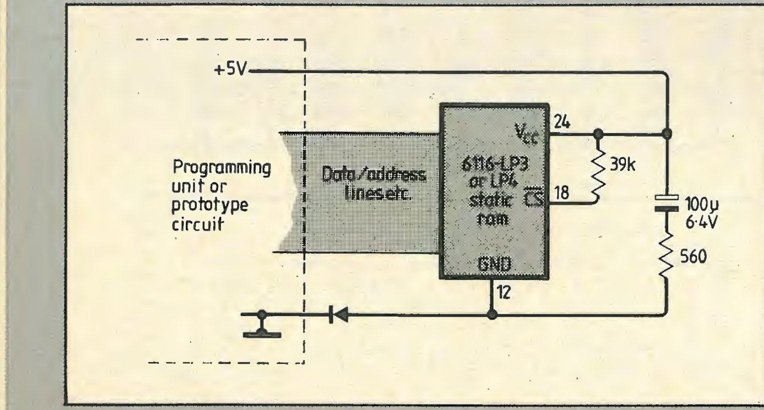




*RN55D or better metal film.
Use trimming to increase output impedance current source



* Metal film



Using static rams for rom development

When developing programs, flying leads and batteries can be avoided by using a 6116 static ram with a few passive components mounted on its back.

Once programmed and powered down, the ram may be removed from the programming unit and transferred to a new circuit without loss of data. Data retention time is more than 10min with LP3 suffix rams and good quality capacitors.

Note that the ram pins are floating while out of the socket so static electricity prevention measures are needed.

Stephen Theobald
Harboore
Denmark

Simple test equipment for microcomputers

by G. B. Williams M. Sc.

Two easily built test aids simplify fault finding in microprocessor, bus and peripheral hardware.

When a microprocessor-based system fails, the highly parallel nature of its organisation makes it difficult to test. Virtually all computer components connect directly to the data bus and many of the address bus lines, so a fault in one component can prevent the processor accessing other components in the system.

The problem is one of isolating the fault to one component, which in the absence of special test equipment can be difficult and time consuming.

Microprocessor-based industrial control systems are input/output intensive and provide little in the way of visual indicators. During commissioning of these systems, input and output connections have to be verified, a process which usually requires attaching specialized test equipment to the system and writing test routines to exercise the i/o ports.

Essential parts of a computer system, called the 'kernel' elements, have to be fully operational if the system is to function correctly. These elements can be tested using a simple piece of test equipment. My NOP tester forces the microprocessor to repeatedly execute a no-operation instruction, which causes the address bus to cycle through every possible value.

This free-run mode can be used to verify the power supply, address bus, microprocessor, system clock and control bus. After these essential elements have been verified, the rest of the system may be tested in the knowledge that any fault in the system is not in these key elements.

All operations carried out by a microprocessor involve transferring information over the data bus. Instruction op-codes or data are read by the microprocessor from memory, or data is written to memory by the processor. Similarly, data written to or read from input/output ports has to be transferred over the data bus.

To analyse these data-bus transfers, the address and control-bus contents have to be viewed simultaneously. The address represents either a memory or i/o port location while the control bus indicates the type of operation being carried out.

To capture and display data bus transfers, a logic state analyser is often used. These instruments have become the mainstay for testing computer systems despite being expensive and physically large.

For field-service or commissioning of an industrial system, simple test equipment often suffices for initial analysis of data bus transfers. As an example, the i/o stages of an industrial scheme may be verified by connecting a simple data-bus analyser to the system and executing either the main control program or a specially written test program.

This allows individual inputs from proximity detectors, control switches and analogue-to-digital converters to be read from the data bus and checked against their expected values. Similarly, values may be written to output ports, and values captured directly from the data bus compared against those detected outside the computer system.

This article describes two simple items of test equipment for use in verifying the kernel elements of a computer and capturing data bus values. The description is for Z80 and 6502 family microprocessors but the approach may be extended to any processor by studying their timing diagrams.

For many years, G. Williams was a Senior Research Officer in Electronics at the Welsh Laboratories of British Steel working mainly on microprocessor based measurement systems for the steel industry. He spent four years at Gwent College of Higher Education as Senior Lecturer in Microelectronics. Mr Williams is currently a Senior Lecturer in Microelectronics at the West Glamorgan Institute of Higher Education, Swansea and is the author of a recently published book Troubleshooting on Microprocessor based systems.

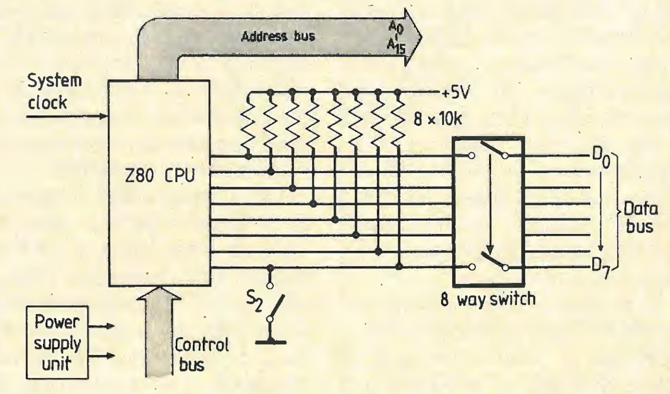


Fig. 1. This 'free-running' arrangement forces byte 7F onto the data bus when S_2 is closed. At reset the processor reads 7F, sees that it represents a no-operation instruction and steps to the next memory location to read the next data byte. This byte is also 7F so the processor steps to the next location, and so on, stepping address lines through every location sequentially. At address FFFF, the cycle repeats.

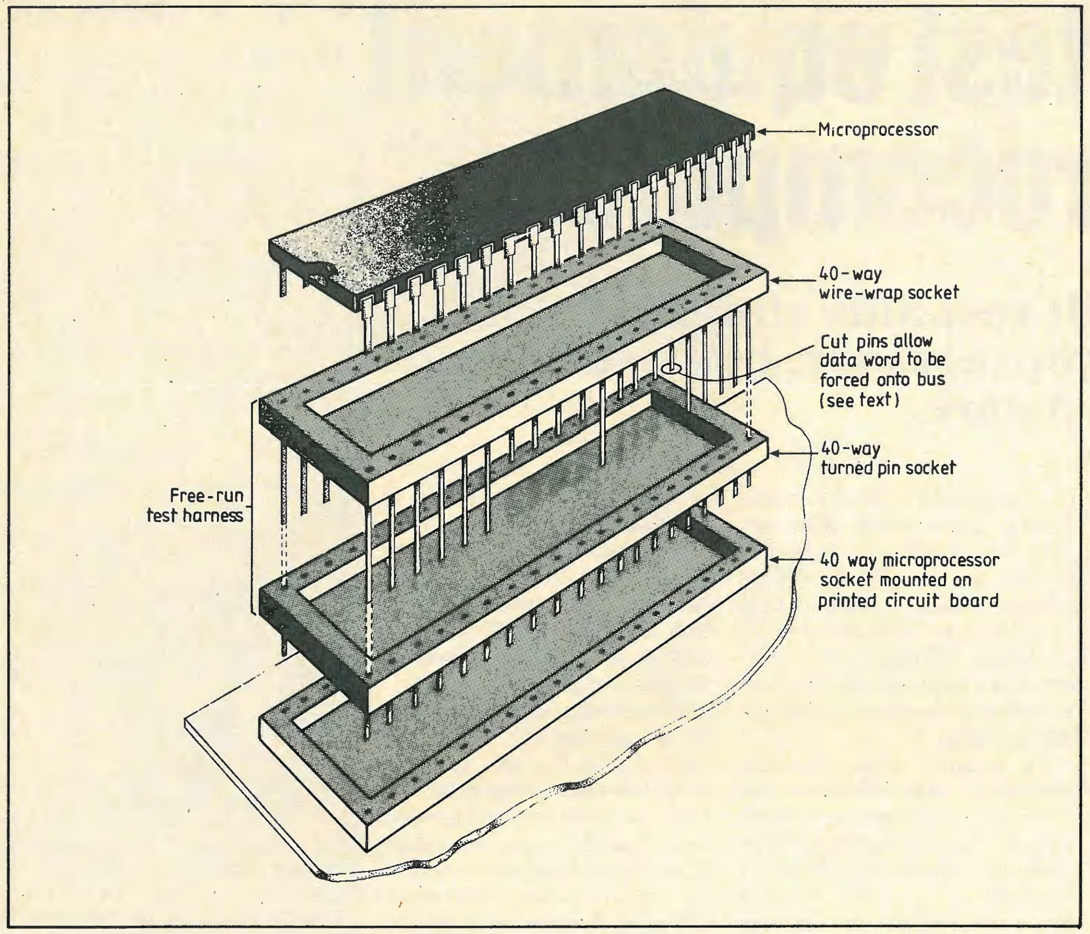


Fig. 2. As an alternative to building the NOP tester into a system, the processor can be removed from its socket and this adaptor inserted in its place. The processor then plugs into the adaptor.

Further reading

Troubleshooting on microprocessor based systems, G.B. Williams, Pergamon.
R6500 Hardware manual, Rockwell.
The Z80 CPU technical manual, Zilog.

The R6500 manual can be obtained through RCS Microsystems, 414 Uxbridge Road, Hampton Hill, Middlesex TW12 1BL for £8. Zilog's manual for the Z80 is available from Gothic Crellon at 3 The Business Centre, Molly Millar's Lane, Wokingham, Berkshire RG11 2EY for £12.

NOP tester

In a microprocessor, free-run mode involves disconnecting the data bus and forcing a no-operation type instruction into the processor as illustrated in Fig. 1.

For the Z80 the standard NOP instruction is represented by hexadecimal value 00; to implement this instruction for Fig. 1, all data bus lines into the microprocessor would have to be tied to ground.

An alternative, simpler scheme makes use of the LD A,A instruction which copies contents of the A register back into itself and consequently represents a 'do-nothing' type instruction. This instruction's code is $7F_{16}$, which may be implemented by pulling all the data bus lines high through a 10kΩ resistor network and pulling most-significant line D_7 low with switch S_2.

The data bus is disconnected from the microprocessor by an eight way dual-in-line set of slide switches; S_1 is opened and S_2 closed. This disconnects the Z80 from the external data bus lines and the LD A,A instruction is forced into it.

Operation of the circuit is best understood by considering the Z80 just after reset. Following reset, the Z80 attempts to read the first memory location by placing value 0000 on the address bus and pulling the RD control line low (active). Data read from the data bus becomes the op-code for the processor's first instruction.

With the tester attached, the processor is forced to read the LD A,A instruction, which it duly executes. Now, the Z80 program counter is incremented to address 0001 and its value is placed on the address bus. From this new location the processor expects to read the op-code of its second instruction. This instruction is again LD A,A so the processor issues address 0002 and executes another read-from-memory operation.

The overall effect is that the Z80 issues every possible address from 0000 to $FFFF_{16}$. When the processor issues address $FFFF_{16}$, the next increment sets its program counter back to 0000 and the cycle is repeated. The 16 address bus lines may be considered as outputs from a 16-stage binary counter with line A_0 exhibiting the highest pulse-repetition frequency and the most-significant address line A_{15} the lowest.

Kernel elements are tested with the processor in free-run mode. Power supply can be checked using a digital voltmeter; the V_{cc} supply should be 5V ± 0.25V and adjusted if outside these limits.

Using a frequency counter and oscilloscope, the system clock can be checked to determine its value and wave-shape. Most microprocessors are specified at their upper frequency limit but can run slower. A 4MHz Z80A should not be operated above this frequency limit but can run as low as 900Hz. As with the power supply unit, the system clock can be checked using conventional test equipment.

Control bus lines may be checked using a logic probe and oscilloscope. For the Z80, only MREQ and RD lines should show pulse activity, with the rest of the lines in their inactive states. Any fault such as a short to ground on the RESET input will be apparent from a simple test with a logic probe.

Address bus activity can be verified using an oscilloscope. Starting from A_0 line, a pulse-repetition frequency equal to a quarter of the system clock rate should be observed (LD A,A takes four clock periods). Line A_1 should show half the pulse rate of A_0 while A_2 should show a quarter. Each line can be tested and verified to be half the frequency of its predecessor.

Lines on the upper half of the address bus, A_8 to A_{15}, display slightly different behaviour to the lower half. Line A_{15} for example displays a low state for half the total address space but pulse activity when at logic one. This is due to the Z80's tendency to clear the upper half of the address bus between successive address-bus values. Provided the pulse activity is taken to represent logic one, the overall p.r.f of one line will be found to be half of its predecessor.

If two address lines indicate the same p.r.f., then a short can be assumed between them; similarly, a permanent logic one or zero on a line indicates a short to ground or V_{cc}.

A free-run test is probably the most fundamental test that can be applied to a processor and is used to verify correct operation of its kernal elements. The microprocessor itself is verified by implication; if it passes this test, then it is assumed to be functional.

Retrofitting the NOP tester

Most microprocessor systems do not include the hardware needed to implement the free-run test. Fortunately, in most systems, the microprocessor is in a socket and can be removed. By constructing a suitable harness, the free-run test can be applied to such a system. Figure two illustrates a harness suitable for Z80 or 6502 processors.

For Z80 microprocessors, the true NOP with a code of 00 can be used. This involves wiring all the pins from the wire-wrap socket directly to the turned pin socket with the exception of pins 7-10 and 12-15 which are the data bus lines.

Wire-wrap pins for the data bus are cut short and tied together; the common line from these pins connects to pin 29 on the wire-wrap socket (ground). Thus all data bus lines into the microprocessor are held low and the Z80 is forced to execute the NOP instruction.

The processor is unplugged from its socket on the printed circuit board and plugged into the wire-wrap socket. The complete harness then plugs into the vacant socket.

For 6502 processors, the only NOP instruction has the value EA_{16}. To make a NOP test harness, pins 26-33 are cut short on the upper wire-wrap socket, with the remaining pins connected across to the turned pin socket. Pins 29, 31 and 33 are wired to pin 1 of the wire-wrap socket (ground) and pins 26, 27, and 32 are wired to pin 8 (+5V). This forces the bit pattern for EA, the NOP instruction into the 6502 device.

A forty-way test clip attached to the processor gives access to the various bus signals for checking kernel elements.

Data bus analyser

Information present on the data bus during normal operation may be extracted using relatively cheap, home-built test equipment. This simple data bus analyser is portable and easy to use, and should prove beneficial when testing i/o sections of an industrial control scheme or for initial verification of bus activity from a system's components.

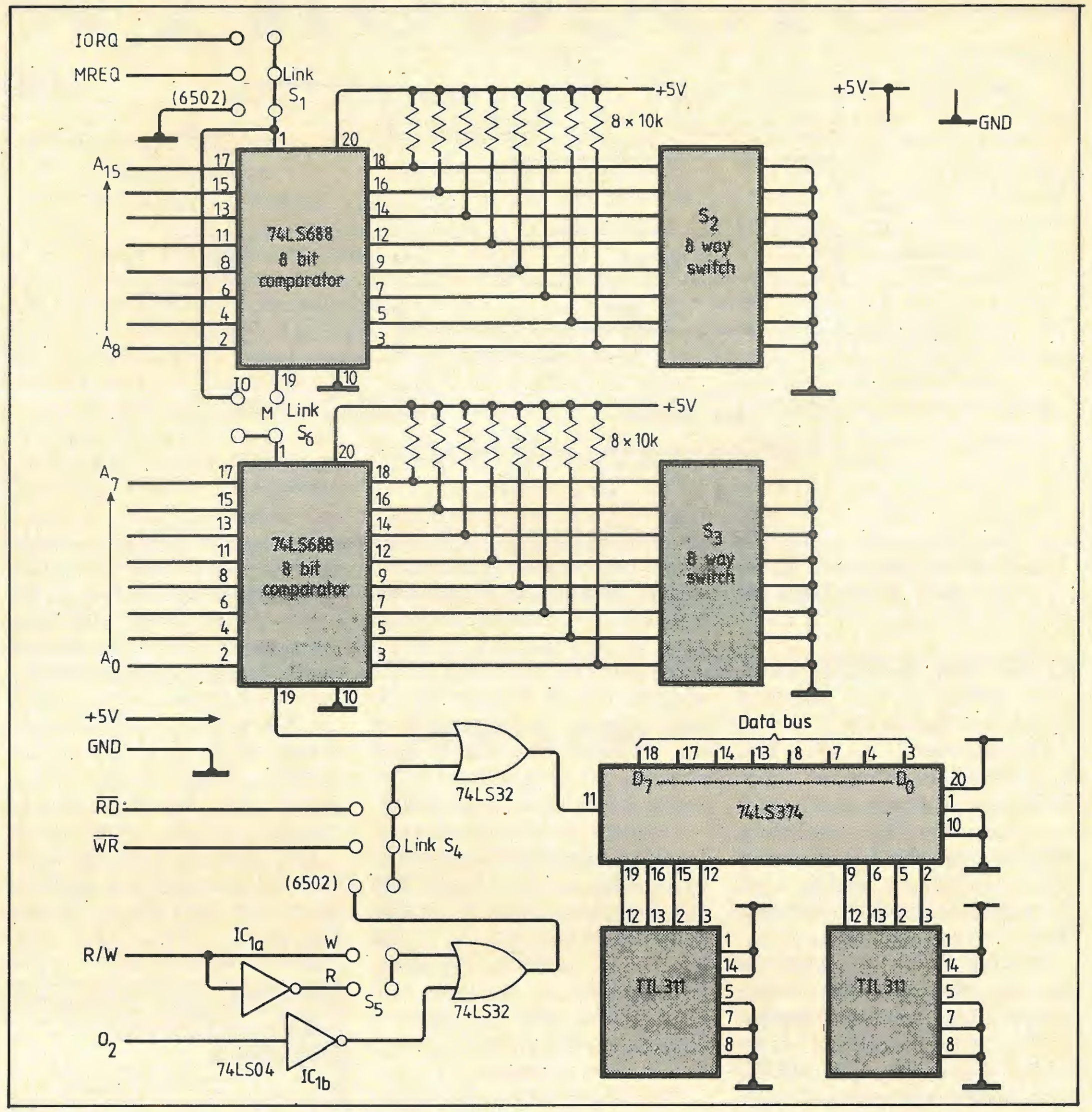


Fig. 3. Using the data-bus analyser, information on the data bus during normal operation is easily extracted.

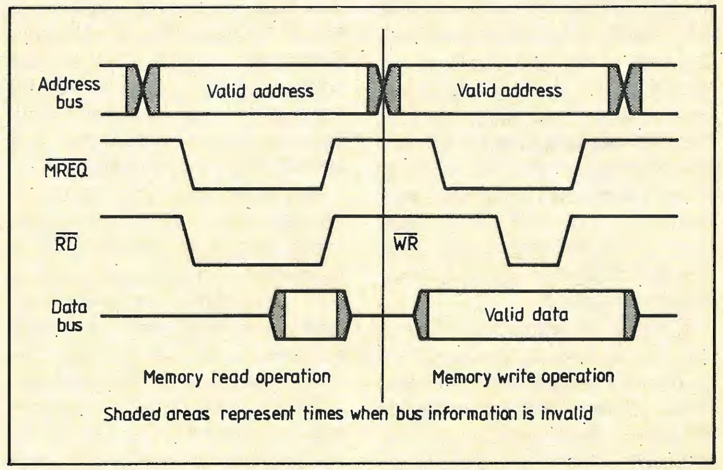
Figure 3 illustrates a simple data-bus analyser for extracting information from either a Z80 or 6502 based system. In the protoype, p.c.b. jumper links were used to select control-bus signals on the analyser while all the signals and power were taken from the microprocessor pins using a 40-way test clip.

I constructed an earlier version using s.s.i. exclusive-or and or gates in place of the m.s.i. octal comparators shown in Fig. 3. The circuit is designed to operate with either a Z80 or 6502 processor but for use on only one of these devices, redundant hardware can be omitted.

Action of the circuit is best illustrated using a timing diagram for the relevant microprocessor.

Z80 analysis

Timing for a Z80 read and write to memory operation is shown in Fig. 4. It is clear that data is always valid on the data bus for either a read or write operation at the rising edge of the RD or WR control-bus signal. For a given qualifying address, information on the data bus can be captured and subsequently displayed by using the rising edge of the RD or WR control lines as clock signals. Similar timing diagrams apply to input/output operations which



Shaded areas represent times when bus information is invalid

Fig. 4. Z80 memory read and write cycles. Read and write cycles for i/o ports are similar but slightly longer due to an extra wait state.

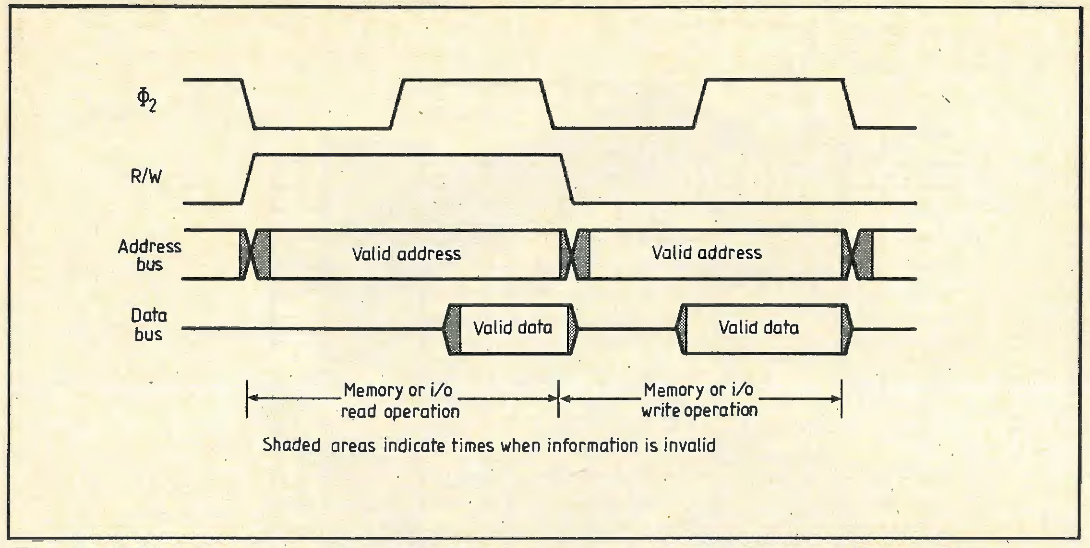


Fig. 5. 6502 memory read and write timing.

mainly differ in that an extra clock period (a wait state) is included in the timing.

The analyser is set for a Z80 by linking S_1 to either MREQ or IORQ to enable the upper octal comparator. The qualfying address is set onto the two eight way dil switches S_2 and S_3. Link S_4 is then selected for either a read or write operation.

Assume that we want to examine the data byte transferred from memory location 1000_{16} during a read operation. Switch S_1 is linked to MREQ enabling the comparators for a memory-request operation. Link S_6 is set to 'M' and address 1000_{16} is set on switches S_2 and S_3. Link S_4 is set to its RD position; incoming signals and power are taken directly from the microprocessor under test using a 40-way test clip.

When the incoming address agrees with setting of S_2 and S_3, and provided that MREQ is low (active), the lower comparator output will go low (active). This is qualified by the state of the RD control line which goes low during the memory read operation.

At the end of the transfer, data bus states are still valid and the RD signal can be used to latch information on the data bus into the 74LS374 octal latch. The information is then displayed on the TIL311 hexadecimal displays.

For a memory write operation, link S_4 is connected to the WR signal and the data value written to the selected memory location is subsequently displayed.

The Z80 has two simple input/output instruction forms. One transfers data from the accumulator of the processor to an i/o port using the lower half of the address bus to convey the i/o port address. The upper half of the address bus, lines A_{8-15} contains the accumulator value and is thus a variable quantity.

For this type of bus transfer, it would be beneficial to ignore the upper half of the address bus and link S_6 is included for this purpose. When link S_6 is put into its IO position, the upper comparator is ignored and IORQ from link S_1 connects directly to the enable input of the lower comparator.

The alternative form of i/o transfer uses the Z80 C register to hold the port address and contents of the B register are issued on the upper half of the address bus during an i/o transfer. Instruction format is either IN r,(C) or OUT(C),r where r is one of the Z80 internal registers.

If the contents of the B register are known during a bus transfer, then the data bus value transferred using this instruction form may be captured using all 16 address lines. Alternatively the upper half of the address bus may be ignored and the i/o address qualified using only the lower comparator and linking S_6 to its IO position.

Assume that you want to capture the value read from input port 80_{16}. Link S_1 is set to its IORQ position and S_6 set to IO. The upper comparator is now bypassed and the port address is set on switches S_3. Link S_4 is set to the RD position.

When the port address appears on the lower half of the address bus and an i/o operation is indicated by the IORQ control signal going low, output of the lower comparator would also go low (active). The rising edge of the RD control signal causes the data bus states to be latched into the 74LS374 and subsequently shown on the TIL311 display devices. When writing to an output port, link S_4 would be made to the WR control signal.

The analyser forms a small, low cost item of test equipment which can be used to capture and display data written to or read from memory locations and input/output ports.

6502 analysis

Unlike the Z80, the 6502 microprocessor, is a memory mapped device and as such does not provide explicit memory request or i/o request control signals. Separate RD and WR control signals of the Z80 are integrated into a single RD/WR control line which in a logic one state indicates a read operation while a logic zero state indicates a write operation.

Input and output ports are treated as memory locations which dictates that i/o ports form part of the total memory space of the 6502 based system. Timing for 6502 read and write operations is shown in Fig. 5.

Figure 5, shows that data is valid on the data bus for either a read or write operation on the falling edge of the ϕ_2 clock signal. This signal edge can thus be used to latch data off the data bus provided that the received address corresponds to that set onto the two eight way dil switches S_2 and S_3 and the correct sense of the combined R/W control line has been selected.

Referring to Fig. 3, for a 6502 system link S_1 is permanently made to ground to enable the comparators because no explicit memory or i/o request signals are available and all operations are taken to be memory transfers.

Link S_6 remains in its M position so that all 16 address lines are used to specify a memory or i/o address and link S_4 is put into its 6502 position. Link $S_5$is set for a read or write operation. The 74LS374 latch requires a positive going edge to latch the data on its inputs to its outputs and an inverter is hence required to change the sense of the ϕ_2 clock line.

To capture the value read from an input port located at address $EOFO_{16}$ for example, link S_5 would be set to 'R' and address $E0F0_{16}$ set on eight-way switches S_2 and S_3. Output of the lower comparator goes low (active) when these conditions are satisfied.

For a read operation, S_5 is in the R position and the signal sense is inverted by gate IC_{1a}. Control signal ϕ_2 is inverted by gate IC_{1b} which causes a positive going edge to appear at pin 11 of the 74LS374; this in turn latches the data bus value to the outputs of the 74LS374 which are then displayed.

A write to a memory location or output port is captured in the same way except link S_5 would be set to its W position.

Conclusion

The data bus analyser provides a cheap, small instrument for capturing data bus transfers from a Z80 or 6502 based system. The instrument requires about 100mA of current which in the event that it cannot be supplied from the system under test, can be obtained from a separate power supply. Usually however, the system under test has sufficient spare current capacity to power the unit and its supply is taken directly from the microprocessor's supply pins on the test clip attached the processor under test.

Both the NOP tester and the data bus analyser are simple instruments that can be carried around by field service and commissioning personnel and can provide valuable insight into the operations of a microprocessor based system. ■

NEW PRODUCTS

I.c. processing module

What amounts to a complete application-specific i.c. manufacturing plant has been encapsulated into a transportable container, delivered by lorry. Within the container is a computer-aided i.c. design station and a wafer processing area with all the necessary clean-room environmental seals, air-conditioning and filters.

The module consists of a silicon-compiler which supports design, simulation, automatic layout and testing.

The heart of the Lasarray Processing Module is their patented wafer masking system which uses a laser to write the mask pattern directly onto the wafer. The laser pattern generator can interconnect about half a million points on a $5mm^2$ chip. Processing a 4in wafer with 200 to 240 dies takes about two hours. Once the design has been completed on the 'silicon compiler', a complete prototype can be produced in a matter of hours. Up to four different designs can be implemented on a common wafer.

The wafer is provided with a metal 'grid' mask that interconnects all the cells in each die. It is covered with a positive photoresist. Line-by-line the wafer is moved in $1\mu m$ steps under a laser that produces a beam of blue light focussed to a spot diameter of $2\mu m$. The wafer moves at a speed of about 300mm/s. Under computer control the beam is turned on and off. This exposes the areas which represent unwanted connections. The width of the lines corresponds to the $2\mu m$ width of the beam.

A second laser beam, red, is used to aid in the positioning of the wafer it is focussed on the same spot as the blue beam but does not affect the photoresist. The wafer surface reflects the red light with different intensities and these variations provide the data for positioning the exposure beam.

When exposure is complete, the unwanted connections are etched away by a standard etching process. The wafer is cleaved into the individual chips which are then assembled in hermetic packages.

The benefits of the system are inherent in the use of application-specific i.cs. They can eliminate a large quantity of circuitry in almost any product that uses electronic or electrical control. This particular system also eliminates the need for other i.c. manufacturers to make the chips and can save a lot of time.

Lasarray claim that their system, costing 5 million Swiss Francs, is cost-saving because it is reduced in size and weight compared with other systems; it reduces power consumption; it offers proprietary designs which, with no third parties, are secure from possible copiers; it offers system reliability and transfers the i.c. design responsiblity to the development engineer, where the knowledge exists and control belongs.

The UK agent for this American system is QTL Limited, Unit 4, Heron Industrial Estate, Spencer's Wood, Reading, Berks RG7 1PG. **EWW 210**

CAD for p.c.bs

The Computamation range of cad tools for printed-circuit board design is available from GM Design. It comes in a variety of configurations and prices and GM have offered the following set-ups as examples. It is possible to mix and match the required facilities to satisfy the specific needs of a user.

At the initial level it is possible to have a simple mouse-driven electronic drafting system which can draw circuit diagrams and tape-up a p.c.b. design. It has a library of regularly-used components and produces an output for a dot-matrix printer or a pen-plotter. This costs about £1520. It can cope with a board size up to 800mm by 800mm with a resolution of 0.25mm (1thou.). It can also cope with multi-layer (up to eight) p.c.bs. There is no limit to the component size and each component can have up to 255 pins. Track width and pad size and shape are selectable from a wide range.

For £1500 more, auto-routing is added which can sort out the rat's nest produced by drawing straight lines between all interconnected points. Mechanical design-rules check ensures that there is the correct spacing between conductors, and connector pads.

At the next level (at about £7000), it is possible to add automatic creation of a rat's nest from a circuit diagram and thence to a p.c.b. pattern, and logical design-rule checking. This ensures, for example, that both ends of a signal line are connected and that the supply-voltage rail is not connected directly to earth!

The full configuration includes everything that is needed to design a circuit diagram on a computer and process it through to final artwork, with full documentation and additional drafting for front panels, chassis etc. This works out at about £8870.

All versions of the design system are menu driven and, it is claimed, easy to use with on-screen 'help' facilities. Among the other features and options available are step and repeat for any number of similar connections, the ability to 'zoom and pan' over the generated screen image, and to alter the aspect ratio or magnification to suit a particular paper size for drafting and plotting. There is a full text editor for the annotation of drawings. It is possible to see the 'before and after' effects of an alteration. All documentation and statistics can be automatically generated to give component lists, purchasing and manufacturing information on copper area, hole count etc.

The system may be used on a variety of computers including Compaq, Apricot, Zenith, Victor/Sirius, and IBM and its compatibles. It supports a wide range of printers and plotters and a photoplotter. The system is constantly being up-dated and GM Design recently responded to customers' requests to include surface-mounted p.c.bs. All the software is designed and written in the UK. GM Desigh, 104 Tanners Drive, Blakelands, Milton Keynes MK14 5BP. **EWW 211**

PC with Dash

Dash is the name of a circuit (schematic in U.S. parlance) design and documentation system. It enables circuits to be created quickly and because design data is automatically captured, a variety of key documents including net list, materials list and design check reports, can be printed at will, using Dash post-processors.

Features include a high-speed graphics editor, mouse-driven commands to move, copy, erase and draw signal and bus lines. It is possible to 'zoom' into an area for closer detail and even move a component about on the design area while still connected; dragging its connections behind. The system incorporates a library of over 1200 symbols (with pin-outs and pin functions) for discrete components, popular families of i.cs in t.t.l. c-mos and e.c.l. Symbols may be chosen and then directed to the display by single key-strokes. There is a text editing facility that allows full annotation of the diagrams.

If designs require gate-arrays or non-standard i.cs, libraries created by the semiconductor companies are available on Dash-compatible discs. Symbols for new components can be created easily; 16-pin block symbols can have their pins numbered with functions, power and ground connections in a few minutes.

The Dash system, with the aid of optional software, is capable of high-speed post-processing for the creation of net lists, materials lists and design checks. A large design file can be processed in about 30 minutes, which, claims FutureNet, is two to four times faster than rival systems.

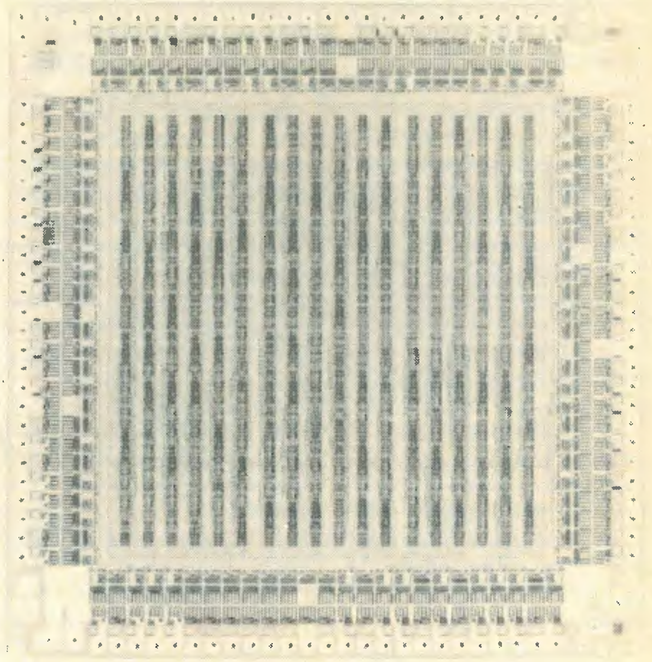
The system can be networked with other Dash systems or with larger computers for further processing and central data storage and can also be interfaced with most large c.a.d./c.a.e. system and so can be used as a 'front end' for Applicon, Cadam/France, ComputerVision, Sci-Cards, Racal/Redac, Spice, Tegas and others.

One version of Dash is available for the DEC Rainbow PC, Dash-3C is a full colour-display version for the IBM PC, XT or AT. UK Distributors: Microsystem Services, PO Box 37, Lincoln Road, Cresex Industrial Estate, High Wycombe, Bucks HP12 3XJ. **EWW 212**

Learn to make an i.c.

A training course in semi-custom design has been organized by Texas Instruments Ltd and Daisy Systems in which participants take a real integrated circuit design of their own choice all the way through layout and design to finished devices, which are produced using TI's electron-beam direct-write-on-silicon machine.

To help promote the use of c.a.e. in semi-custom circuit design, the two companies have set up seminars followed by workshops providing information and in-depth training on the design of semi-custom products. The Daisy workstation and TI E-beam combination can reduce the time to produce an i.c. from concept to samples to two weeks. For further details contact Anna Juliano, Semicustom PCC, Texas Instruments, Manton Lane, Bedford MK41 7PA. **EWW 213**



Fast c-mos gate arrays

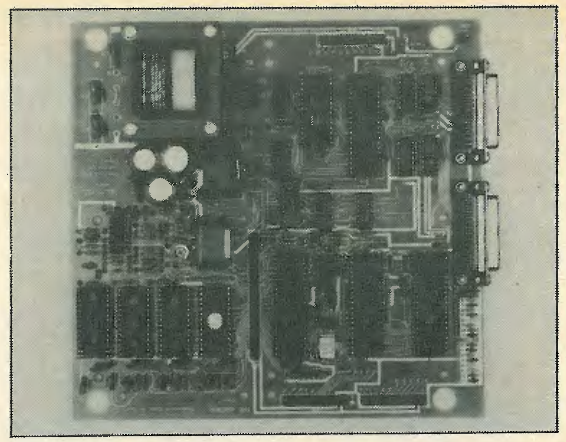
The AV family, three new series of high-speed c-mos gate arrays from Fujitsu, have a typical propagation delay time per gate of only 1.4ns, making them one of the fastest gate-array families available in volume production. The devices combine 1.8Ωm geometry and high gate-density with low poer consumption for optimized performance. There are 14 device types within the three ranges and all available.

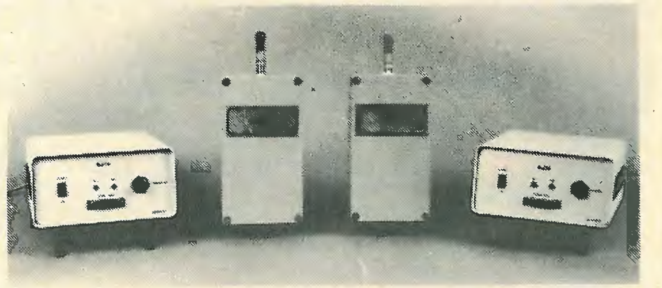
Features of the new series include a single 5V supply, typical ram access time of 26ns, and a wide variety of input level options: t.t.l. input/output levels, c-mos input level and Schmitt-trigger input. Package options include dip, flat-pack, pin-grid arrays amongst others.

The basic AV series comprises five devices with the number of gates ranging from 2640 to 8000 and up to 160 signal pins. The three devices in the AVM series incorporate blocks of ram with the gate arrays. They give 1000 logic gates and 2Kbit ram, 2375 gates with 1Kbit ram or 4000 gates with 2Kbit ram.

The special feature of the third series, AVB, is the high output drive capability of 10mA. It is designed with input pull-up/pull-down resistor options, a c-mos level input buffer and a Schmitt-trigger input, as well as t.t.l. level compatible input/output. Six devices range from 300 gates to 2056 gates with from 40 to 80 signal pins.

The AV family is fully supported by Fujitsu's c.a.d. system which automates l.s.i. design work for error-free fabrication with a short time-span. The system performs a complete logic simulation, incorporating a.c. parameters and capacitive loading. Software is available for use on such c.a.e. workstations as Daisy, Mentor and Valid, and a simplified customer interface which only requires logic and test information to complete the design stage. Fujitsu can provide a seven-week turn-around from design approval to completed samples. Fujitsu Mikroelektronic, Hargrave House, Belmont Road, Maidenhead, Berks SL6 6NE. **EWW 214**





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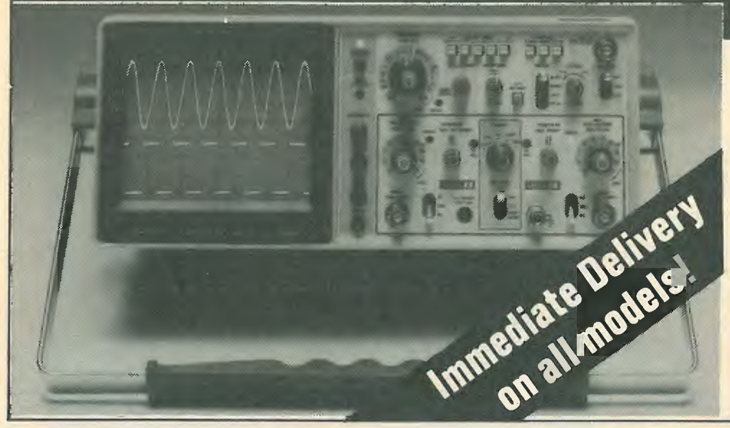

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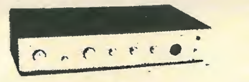

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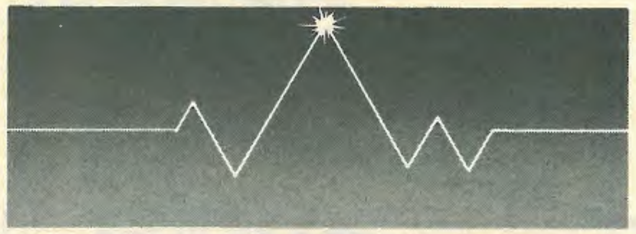
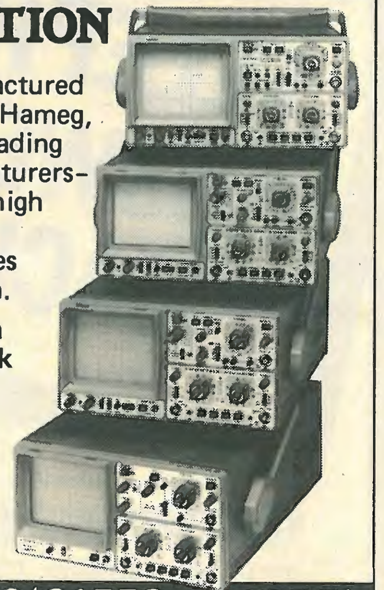


OF PERFECTION



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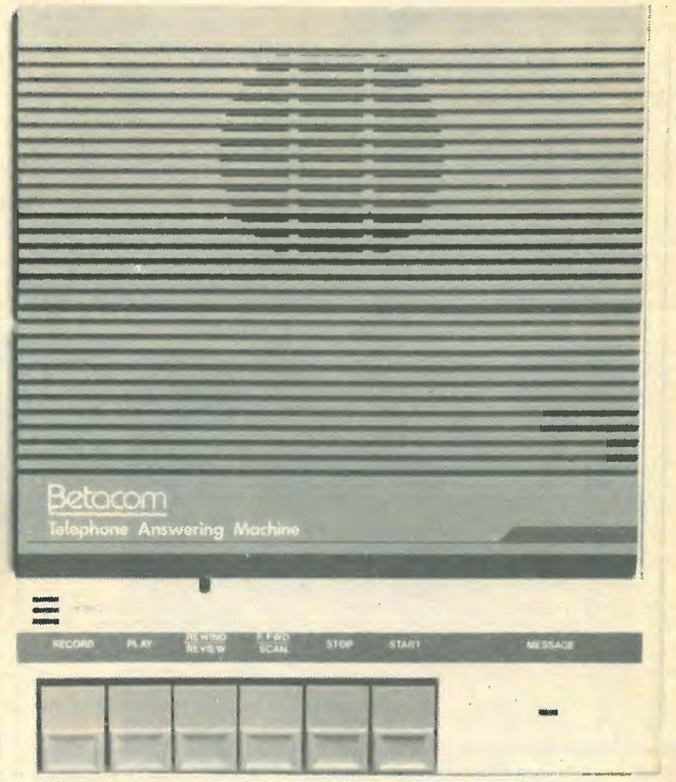


CAD/CAE

Continued from page 78

Semi-custom linear circuit

An analogue integrated circuit has been developed by Raytheon which contains a variety of pre-designed programmable circuit cells that can be interconnected by the addition of a second (top) layer of metal. The bottom layer of metal is used to fabricate the structural components, including: 12 "gain blocks", 55 independent small-signal transistors (16 p-n-p and 39 n-p-n) all capable of 36V operation, four n-p-n. 100mA switching transistors, 176 thin-film resistors with values ranging from 1.25Ω to 150kΩ and a tolerance of 5% and 148 aluminium crossunder feedthroughs, each with a resistance of only 0.05Ω.

The device is called RLA120 and can be used for a wide variety of linear applications. The macrocell gain blocks can be configured as any combination of 4558, 324 or 4304 type op-amps or as 339 or 365-type voltage comparators. The design method can be adapted to most types of c.a.d./c.a.e. workstations. Raytheon are adapting the Spice suite so that computer circuit simulation will be possible.

Other features of the macrocells are; a slew-rate to 15V/μs; unity gain bandwidth to 20MHz; and a selectable supply voltage between 2 and 30V. The temperature coefficient of the thin-film resistors is 100ppm. Further details from Raytheon Semiconductor, Ogilvie Road, High Wycombe, Bucks HP12 3DS. **EWW 215**

CAE physical modelling system

Chips may be tested and 'exercised' at vector rates of up to 16MHz, using the CDX7900, a modelling system from Cadnitex. The user can plug v.l.s.i. circuits into this physical modelling system without the need to develop structural and functional models of these complex parts. The new system can help to reduce investment costs by its ability to serve as a shared resource for design engineers working with the Cadnitex CDX9000 range of c.a.e. workstations.

The application-specific hardware can cope with 60 different devices and has a vector memory of up to 512K by 96bits.

CDX7900 can also accommodate v.l.s.i. devices requiring up to 95 input bits in parallel and can generate up to 256 output bits. A buffer of 256K by 96bits stores the 95bit vectors. After a part is initialized, the entire stack of inputs is executed to obtain the proper output for a particular step in the i.c's operation, ensuring that internal states within the circuit are correct at the time of measurement.

The instrument is based around a 68010 processor and has 3.5Mbyte of memory and a 40Mbyte hard disc. It costs about £45000. Cadnitex Ltd, Cherry Orchard North, Kembrey Park, Swindon, Wilts SN2 6UH. **EWW 216**

Engineering software

Amongst the new products available from Seasim, a company that specializes in software for circuit modelling and simulation, is Microspice, a comprehensive circuit simulator for use on the BBC Micro. It is used in assessing the performance of a circuit before manufacture. Microspice handles operating points, small-signal linear analyses, and noise (thermal, transient and flicker) performance. These may be used in conjunction with a sweep facility, which at a spot frequency (or d.c. operating point) allows the investigation of changes in performance caused by alteration of component values. The program can be used in engineering research, design and development, and could prove useful in education. Price, with a comprehensive operating manual, £99 (+ tax).

Another new product from the same supplier is Tatum's Logic Simulation System, this time for use on an MS-DOS or PC-DOS computer. A built-in editor can be used to build a digital logic circuit from a good variety of components. Groups of components can be defined as 'macros' and then incorporated into circuits as integrated components. These can be nested within other macros indefinitely. The command list is short and easy to remember and the simulation is fast. Four logic states are supported: "1", "0", high-impedance and floating, and a number of user-defined signal sources may be introduced. The output provides a timing diagram, loading report for fanout, and circuit listings. Full disc save and load facilities are included. The manual contains step-by-step tutorial instructions for the first-time user as well as a comprehensive guide to the system. Price £350 (+ tax). Details from Seasim Engineering Software Ltd, The Paddocks, Frith Lane, London NW7 1PS. **EWW 217**

CAD/CAM from PC to mainframe

Computervision have added a number of new products recently to their computer-aided design and manufacturing range. They give pride of place to the Personal Engineer, based on the IBM PC-AT, which is a circuit design and capture package fully compatible with other Computervision workstation software systems. The package enables the user to create hierarchical diagrams and display waveform graphics from simulations run on the CDS3721-E workstation.

Software enhancements to the range include: Hilo-3, an improved version of GenRad's Hilo-2 simulator. This can determine 15 levels of logic "strength", thereby allowing the simulator to eliminate uncertainty where circuit nodes may have conflicting driving elements and to provide better initialization capability.

HiPost processes the results of the automatic test generator and can also be used to convert user-designed test vectors into an input pattern for driving test equipment; Timver is a timing verifier that allows the user to determine worst-case propagation delays or maximum circuit speed in an i.c. layout.

Vale is an advanced layout editor for v.l.s.i. circuits, which contains a set of object and manipulation commands that allows the physical geometry of the i.c. to be edited, 'simply and efficiently'. The system includes Full-custom Design/3000 integrated layout and verification tools, cursor manipulation of objects, wire editing including bus routing; and a C-language interface. Symbolic Layout/3000 allows designers to produce i.cs using a symbolic virtual-grid layout.

ElectroCADDS/3000 is a p.c.b. design package for running on a Computervision 32-bit CDS3000 workstation. It is completely integrated with other engineering applications on the CDS3000, and includes integrated placement, routing and editing for optimum design speed and accuracy. All the system can be networked, with shared resources and linked to a mainframe computer for data storage and a common database. Computervision Ltd, Central House, New Street, Basingstoke, Hants RG21 1DP. **EWW 218**

Megacell from Plessey

A new application-specific i.c. design system has been introduced by Plessey to make full use of semiconductor design technology and c.a.e./c.a.d. Its called Megacell. Plessey claims that through its use, it is possible to minimize design time and costs while making the best use of the silicon areas.

Unlike some traditional cell-based methods, with Megacell, the circuit designer can compile large cell structures, such as memories, programmable logic arrays and arithmetical logic units if the precise performance needs are not already met from the Megacell library. The software has been developed by Plessey to specifications set by its own v.l.s.i. design engineers. They have insisted that the system can be addressed in plain language, is easy to learn, and may be used simply and straightforwardly by electronic design engineers.

To simplify design and to implement circuit function, Megacell uses four basic types of cell: Microcells are the low-level logic cells similar to those in other gate-array libraries: Paracells provide memory and logic functions created from parameters set up by the system designer; Supracells, from Plessey's own library, replicate standard l.s.i. functions and include some standard catalogue parts such as fifo memory buffers, or uarts, but optimized for integration within the Megacell parameters. The Supracell library is still expanding and will include a-to-d and d-to-a converters and a choice of a.l.us. Layout cells can be any combination of Microcells, Paracells and Supracells. A complete block of a circuit can be defined as a cell and then re-used in other locations. Using a hierarchical nesting facility cells can include other cells which can themselves include cells.

There are two methods of data capture. The circuit can be defined as a 'netlist' or can be input through the circuit diagram using one of the many graphic workstations, like Futurenet, that can handle the Megacell library.

Design verification and simulation and the automatic generation of test patterns is carried out by a suite of software called Classic. This is an event-driven simulator that uses parallel processing to enhance performance and shorten simulation times. It accommodates not only "1", "0", "don't know", and high-impedance states normally forced in simulators, but also rising and falling edge detection to help the designer identify possible "race" or "glitch" conditions. The Classic suite includes the ability to assist designers in developing test vectors and peforming fault simulation to ensure the testability of the design. Plessey has proven these tools by the successful production of over 200 designs during the development process.

Layout and routing are carried out using the Megacell Layout Editor (MLE). The designer can position the cells and MLE will check to ensure conformity with layout rules and the description of the circuit produced by Classic. Routing of the conductors between cells can be automatic, or, if any part of the circuit is especially critical it can be routed by the engineer, leaving the rest to autorouting. The system works on a graphics terminal with "mouse" control. Two layers of metallization are used, corresponding to x and y axes. Where they cross they may be joined through "via" holes.

Once the layout and routing is complete, checks can be carried out on the capacitance at each interconnection. This data is fed back to the simulator for further testing. The masks for producing the final chip are generated as well as test patterns for automatic test equipment.

There are different methods for using the system: the user can get the software and use it on a Vax computer system; the customer can also go to a third-party design house which has the system installed, or get the project designed by Plessey themselves. The final mask output and test patterns are forwarded to the Plessey silicon foundry for manufacture and testing.

Further details from Plessey Semiconductors Ltd, Cheney Manor, Swindon, Wilts SN2 2QW. **EWW 219**

Scientific and cad workstation

The Stride 440 is a low-cost desk-top workstation for Fortran programs made by Equinox. Built around the 6800 processor running at 12MHz, and with from 1MByte to 8MByte of ram, the unit cam have an optional floating-point maths co-processor, and features both flexible and hard disc drives; the latter with a capacity from 10 to 110MByte. A tape back-up unit is optional. Single-user or multi-user networked systems are available.

Suitable for fast maths processing or for cad/cae and other engineering applications, the workstation runs the full ANSI-standard Fortran 77. This system exploits the full addressing abilities of the 68000, allowing virtually unlimited size programs as well as data storage and mathematical structures. There are language extensions which makes it possible to convert programs written in Fortran 66 dialects.

The Stride 440 also supports Unix V, and has been used by Inmos in their development of Occam programming for the Transputer project. It costs about £4000. Equinox Computer Systems Ltd, 114 Curtain Road, London EC2A 3AH. **EWW 220**

Surface-mounting cam

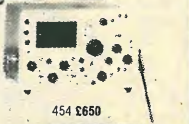
Prepared to share their knowledge of the design, development and manufacturing services for surface mount technology, is Surtech Interconnect, a company in Basingstoke. They are prepared to show groups from industry their surface-mounted assembly operation.

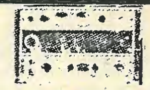
Visitors are given a presentation on the processes involved with particular emphasis on the factors affecting yield. These include processing, design, equipment and the quality of both p.c.bs and components. The equipment includes machines for automatic pick-and-place of components, guided assembly, and wave and vapour-phase soldering. The emphasis is on informality and Surtech staff are willing to discuss the problems likely to be encountered when introducing the technology and also their possible solutions.

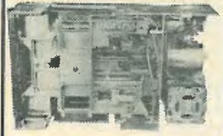
Visits are free and are organized by the Cadmat Office, Institution of Electrical Engineers, Savoy Place, London WC2R 0BL. **EWW 214**

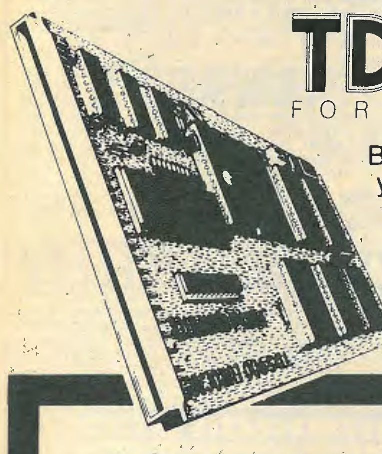
High-speed Compute Engine

A hardware accelerator can dramatically speed up the tasks of a c.a.e. workstation. Mentor Graphics have introduced the Compute Engine that uses some of the latest computer technology. It is a reduced instruction-set computer with parallel processing and has a throughput of 10mips. This, paradoxically, can provide up to 100 times the speed of processing of a 1mips workstation. The accelerator can be used in all workstation applications — simulation, placement, routing, design-rule checking on data formatting, unlike some single-purpose accelerators. The architecture of the Compute Engine is completed by a compiler which converts standard high-level language source code into an object code, fully optimized for the Engine's parallel processing. The software package includes a complete set of program development tools which allow rapid applications development in a standard high-level language. The Compute Engine is priced at £25800 and includes a c.p.u. board and a 4Mbyte memory board to fit the Apollo DN550 and DN560 workstations complete with the software application upgrade. 10Mbyte and 20Mbyte versions are available at £34100 and £47900 respectively. Additional software upgrades cost £3900 per application. Mentor Graphics plan to offer similar global accelerators for the entire range of Apollo workstations. Mentor Graphics (UK) Ltd, Western Centre, Western Road, Bracknell, Berks RG12 1RW. **EWW 222**









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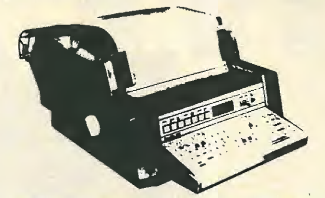

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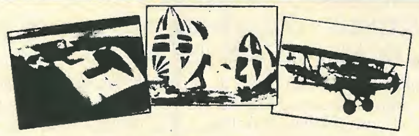

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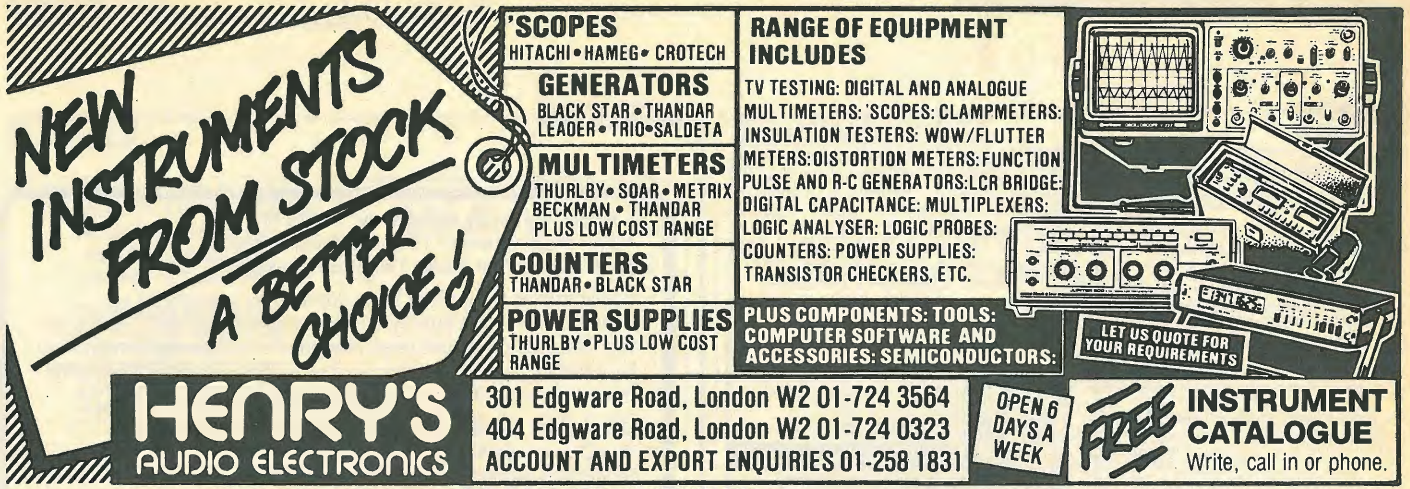

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